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intel®

memory design handbook

INTRODUCTION

The Intel Memory Design Handbook contains information on the use of Intel's memory components and support circuits in system application. It is intended to aid the system designer to gain a thorough understanding of the operation and characteristics of Intel memory components in a system environment.

The Handbook contains six major sections:

1. An overview, which discusses the evolution of various members of the semiconductor memory family.

2. Random Access Memories, which discusses the Intel 16K, 4K family of dynamic RAMs, and both high speed and low power Static 1K RAMs.

3. Read Only Memories, which discusses the Intel bipolar and MOS families of fusible link and Erasable Programmable Read Only Memories, including the newest 5V 16K device, the Intel® 2716.

4. Serial Memories, which discusses the operation of Charge Coupled Devices (CCD's) and the information necessary to design several systems with them.

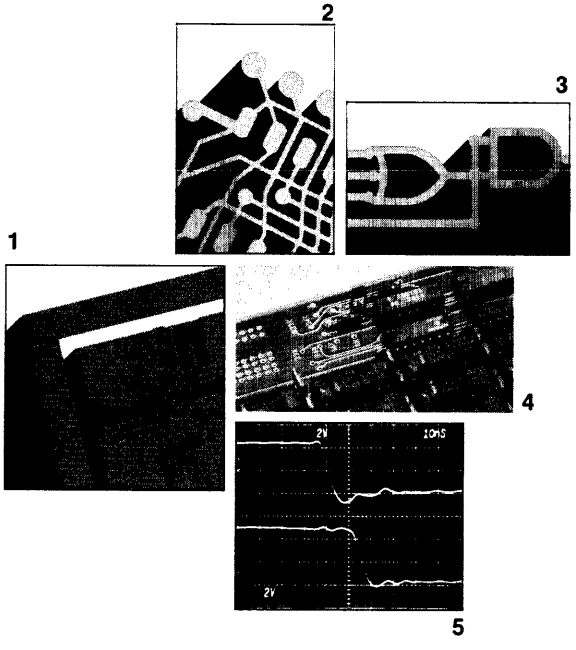
5. Support Circuits, which discusses the use of the various refresh controllers and drivers that are available as companion devices to the Intel storage devices.

6. Appendix, which contains reprints of several previously published articles that are pertinent to the devices discussed elsewhere in the handbook.

The Intel Data Catalog is intended to be a companion to the handbook, as it contains detailed specifications of all of Intel's storage devices. You may request a copy of the Data Catalog from the nearest Intel Sales Office or distributor listed on the inside back cover.

Bob Greene
Application Engineering

ON THE COVER:



The cover represents the entire process of designing a semiconductor memory.

1. During the process of manufacture, each semiconductor memory is "laid out" in a manner similar to that used in printed circuit boards, with a different mask used for each step to control etching, metal deposition, etc. This rendering illustrates a reduced segment of a mask used in manufacturing an Intel dynamic RAM.

2. In order to interconnect the storage and control devices to make an operational memory system, a printed circuit board must be designed. This photo represents the composite (component side and solder side) layout used by designers to check the electrical integrity of the circuit connections. Detailed memory storage card layouts are presented in several sections of this handbook.

3. No system is complete without a logic diagram of the control portion. The correct implementation of control logic is absolutely necessary to proper operation of any storage system. NOR gates, NAND gates, as well as other TTL logic elements are the building blocks used in designing the control and interface portions of a storage system.

4. The finished storage card will resemble this photo of the Intel in-1611 Basic Storage Module, designed and manufactured by the Memory Systems Division of Intel. The in-1611 uses the Intel® 2116 as the basic storage element. The card is available in either 64Kx18 bit or 128Kx9 bit configurations, and can be used in systems requiring up to 384Kx72 bit storage systems utilizing the Intel in-Unichassis.

5. The proof of any storage system is in its performance. Using a high speed oscilloscope, this photograph was taken of an access cycle on an Intel® 2115, a high speed 1K static RAM. The address is shown as the top trace, and the bottom trace is the Data Out signal. This particular device shows an access time of approximately 15 nanoseconds at room temperature.

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memory design handbook

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Overview

OVERVIEW

Developments in the semiconductor industry during the last six years have resulted in a major shift in the type of storage technology used in digital systems. Semiconductor memories used today are lower in cost, higher in density, faster in access and cycle time, higher in reliability and more modular in incremental size than the comparable core memory modules that are available. The advantages of semiconductor memories have been so widely accepted that semiconductor memory shipments will exceed core memory shipments in 1975. The curves shown in Figure 1 show this change in the memory market place and the increasing importance of semiconductor memory.

SEMICONDUCTOR MEMORIES

Semiconductor memories are divided into three broad categories as shown in Figure 2. With two exceptions, each of these three generic categories can be implemented with either of the two major semiconductor technologies: MOS or bipolar. These exceptions are the CCDs (Charge Coupled Devices) and EPROMs (Erasable Programmable Read-Only Memories) which are uniquely implemented with MOS technology.

Random Access Memories

No other area of semiconductor memory has grown as rapidly and as large as that of random access memories. Leading the way in the explosive growth of RAMs are the MOS devices. One of the reasons for the wide acceptance of such devices has been the increasing bit density of MOS devices. The density has been quadrupling on the average of every two years as shown by the graph in Figure 3.

In 1969, Intel introduced the 1101, a 256 x1 bit static MOS random access memory (RAM). This device was designed primarily for small buffer storage applications where 256 word modularity, low overhead support cost, and ease of use were important design objectives.

In 1971, Intel introduced the 1103, a 1K x 1 bit dynamic MOS RAM. The 1103 offered a 4:1 density improvement along with a 4:1 speed improvement over the 1101. The 1103 was the first semiconductor memory element to be speed and cost competitive with core memory systems, which explains the fact that the 1103 is the largest volume semiconductor memory device ever produced.

In 1973, Intel introduced the first 4K dynamic NMOS memory, the 2107. This product was subsequently improved and is known as the 2107B, which has become the industry standard for 4K RAMs in 22 pin packages. In addition, Intel now offers the 2104A, which has reduced the package size for a 4K RAM to a standard 16 pin package. The 2104A, in integrating many of the support circuits internal to the device, has produced an improvement in ease of use. P-channel 1K RAMs, with their MOS level inputs, required high voltage TTL-MOS drivers on all input pins. Their low level signal output required the use of external sense amplifiers. These overhead devices have been integrated onto the 4K 2104A chip such that all input and outputs are fully TTL compatible. The trend has been and continues to be toward denser, faster, and easier to use semiconductor memory devices.

In 1977 Intel introduced the 2116, a 16-pin 16K dynamic RAM with latched outputs, thus continuing the evolution shown in Figure 3. This RAM is also TTL compatible on all inputs and outputs, and can be plugged directly into 2104A sockets, providing a 4:1 increase in density.

While dramatic improvements have been made in MOS dynamic memories (such as the 1103 and

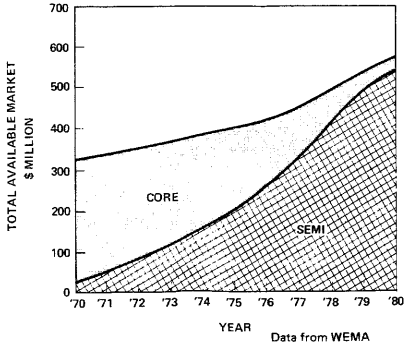


Figure 1. Total Available Memory Market.

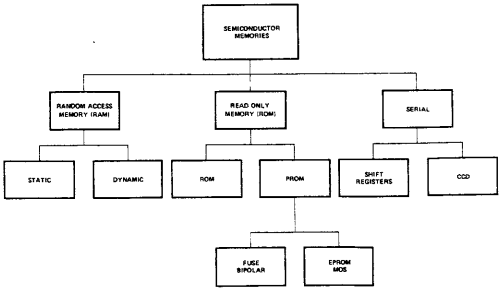


Figure 2. Semiconductor Memory Family Tree.

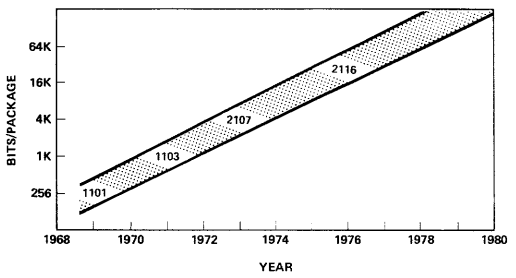


Figure 3. Dynamic RAM Evolution.

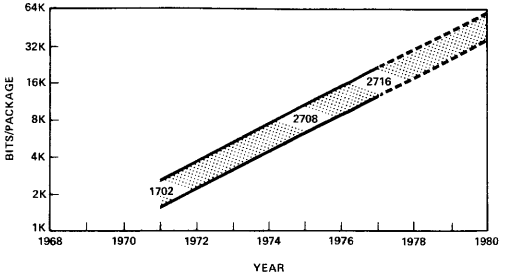


Figure 4. MOS EPROM Evolution

2107A, 2107B, 2104A), equal improvements have been made in high density static, TTL compatible memories. This family of devices, such as the 2102A, 2101A, 2111A, 2112A, 2114, 2115A, 2147, and the CMOS 5101 has greatly increased the ease of use of memories in systems which do not require a large amount of memory. These static RAMs (like the dynamic RAMs) are continuing to expand to include faster devices.

Read Only Memories

The Read Only Memory, like the random access memory, has gone through evolutionary changes in a short period of time. Innovations in bipolar and MOS technology have resulted in programmable and eraseable programmable ROMs, called PROMs and EPROMs respectively. These two types of devices have greatly increased the usefulness and acceptability of Read Only Memories in system applications.

One of the most unique devices in the ROM family is the eraseable PROM (EPROM) such as the Intel® 1702A, 2708, and 2716. These devices, which have bit densities of 2K, 8K, and 16K respectively, offer the system designer maximum flexibility in changing program instructions etc. in the development of their systems.

Other user programmable device types (not erasable) are the Intel® 3601, 3602 and 3604 family of bipolar PROMs. These devices offer the system designer very fast access times along with the ability to change programs "in-house" by merely replacing an old PROM with a newly programmed PROM.

Since their introduction in 1971, MOS EPROMs have undergone evolution similar to dynamic RAMs, only at a somewhat slower rate. Figure 4 indicates that their density doubles approximately every two years.

To maintain compatibility with the new generation of microprocessors which have a 5V technology, in 1977 Intel introduced the 2716, a 2K by 8 bit UV eraseable PROM, which requires only a single power supply for normal operation. In addition, programming was simplified and now resembles a bipolar PROM type of programming; after raising programming supply to +26 volts, addresses can be programmed in random order; with all signals being TTL compatible, including the address data and program pulse-inputs. Erasure requirements remain the same as the 2708–15w sec/cm^2.

In addition to the 2716, true mask ROM replacement is now available in the form of the Intel 2316E. When the programmable Chip Select inputs are selected in accordance with the suggested pinout in the Intel 1977 Data Catalog, the 2316E can plug directly into the 2716 socket, with no need to relayout the board. In addition, a system designed for use with the 2316E can be "customized" for OEM special systems by programming them with the custom data pattern and inserting them in the 2316E sockets, either at time of manufacture or in the field.

All of the Intel PROM family of devices has a counter-part in ROM (non alterable or mask programmable) form. These devices are generally used in systems which are in mass production.

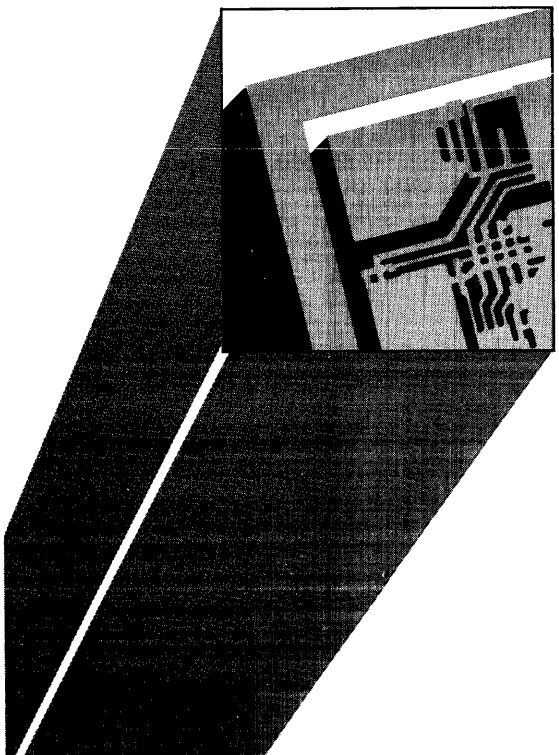
Serial Memories

One of the most exciting new memory products to be recently introduced is the Intel® 2416, a 16K charge coupled device (CCD). The high density and low cost of this device makes it very attractive for use in "drum" replacement type systems as well as terminal and minicomputer applications.

To facilitate the use of the 2416, Intel now offers the 5244, a clock driver that minimizes the problems of manipulating the 4 clock inputs by 1) providing TTL inputs and 2) providing output rise time control and 3) providing "cross coupling" control to minimize intercoupling between phases. One 5244 will drive 4 2416's or provide storage and transfer clock control for a total of 64K bits.

This handbook contains a detailed explanation of the use of the 2416 in a system environment. The significance of the unique organization of the 2416 is also fully explored so that the designer may take maximum advantage of its characteristics.

Random Access Memories



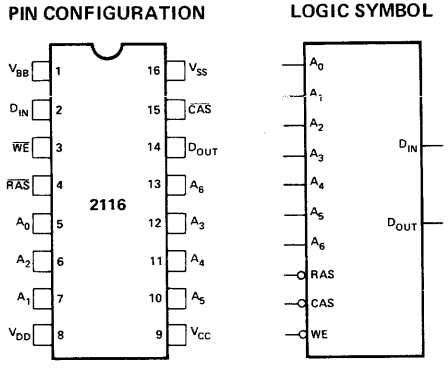
Application of the Intel® 2116 16K RAM

Jim Coe
Application Engineering

Contents

INTRODUCTION

The Intel® 2116 is a 16,384 word by 1 bit dynamic random access memory. The 2116 is fabricated using Intel's proven two-layer polysilicon, n-channel silicon gate MOS technology. The device is packaged in a standard 16-pin DIP. The pin configuration and logic symbol are shown in Figure 1.



PIN NAMES

A_0 - A_6	ADDRESS INPUTS	$\overline{WE}$	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

Figure 1. 2116 Pin Assignments

The 2116 operates with three power supplies relative to ground: V_{DD} (+12V), V_{BB} (-5V), and V_{CC} (+5V). The V_{CC} supply is connected only to the output buffer of the 2116 and may be turned off during power down (battery back-up) operation.

The 2116 is designed to be compatible with the industry standard 16-pin 4K RAM, the Intel® 2104A. This compatibility allows a single system design for both the 4K and 16K devices providing for memory expansion without additional engineering.

The use of the 16-pin package is made possible by multiplexing the 14 address bits (required to address 1 of 16,384 bits) into the 2116 on 7 address input pins. The two 7-bit address words are latched into the 2116 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

Data is stored in the 2116 in single transistor, dynamic storage cells. The storage cells require refreshing for data retention. Refreshing is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds.

The purpose of this Application Brief is to describe the basic internal operation of the 2116 and to outline the areas in design which allow a 2104A/2116 compatible memory system.

Device Internal Operation

Operation of the 2116 is most easily understood with the aid of the block diagram shown in Figure 2. As is shown in this figure, the 2116 is arranged as two 8192-bit storage arrays sharing a common set of column address decoders and a common I/O bus. Each array is arranged in a 64 row by 128 column matrix of storage cells with 128 sense amplifiers per array. Row address bit A_6 is decoded and selects one of the two arrays to be active during any given memory cycle. Thus, only one set of 128 sense amplifiers is active during a cycle maintaining low operating power.

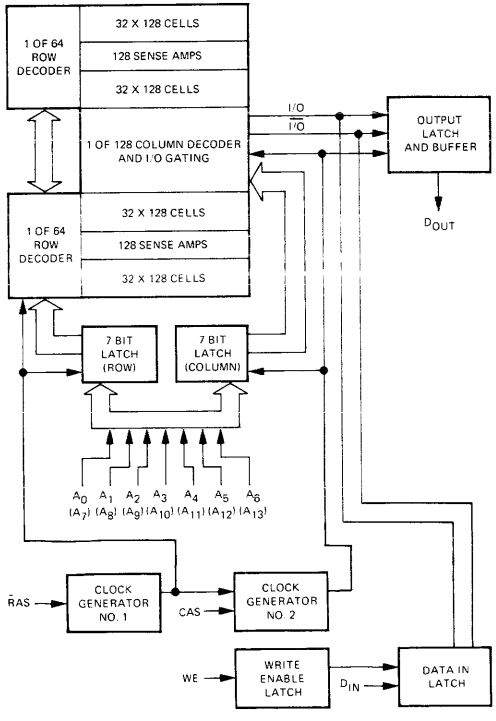


Figure 2. 2116 Block Diagram

The storage cells are implemented with a single transistor and a "storage" capacitor and are called single transistor cells. A cell is accessed by the coincidence of a row select (defined by address bits A_0 - A_6) and a column select (defined by address bits A_7 - A_{13}). On chip timing and control

generators provide the internal timing signals for decoding, data sensing, read/write strobing and I/O data gating. The timing circuits in the 2116 are activated by the negative going edges of the two TTL clocks, $\overline{RAS}$ and $\overline{CAS}$.

Data Sensing

Data is stored in the 2116 storage cells as one of two discrete voltage levels on the cell capacitor; a high is $\sim V_{DD}$ (+12V) and a low is $\sim V_{SS}$ (ground). These levels must be sensed by the data sense amplifiers and propagated to the Data Output (D_{OUT}) in order to fulfill the function of a RAM device. Sensing of the stored levels is destructive and automatic restoration (rewriting) of the sensed data must also occur.

The 2116 data sensing scheme is known as the Dummy Cell Reference technique. The reference level that the sense amplifier compares the stored level to is a level stored in a special, non-accessable storage cell. The level stored in this reference or "dummy" cell is less than the minimum allowable stored high level and greater than the maximum allowable stored low. Examination of the simplified sense amplifier schematic of Figure 3 will clarify the sensing operation.

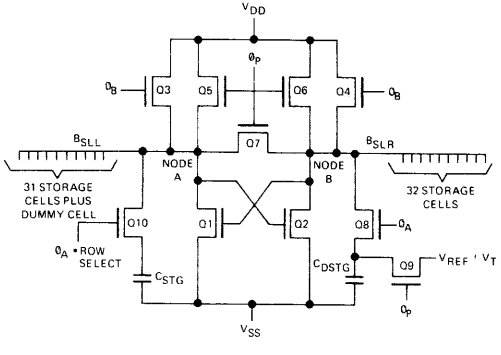


Figure 3. Simplified 2116 Data Sensing Schematic

During the $\overline{RAS}$ clock off time (high), ØP turns on devices Q5 and Q6 connecting nodes A and B to V_{DD} and precharging the nodes to V_X ($\sim V_{DD}$-V_T where V_T is the MOS device threshold voltage). Device Q7 is also turned on by ØP and connects nodes A and B together assuring that they reach the same precharge level. ØP also turns on device Q9 precharging the dummy storage cell capacitor (C_{DSTG}) to V_{REF}.

When $\overline{RAS}$ goes active (low), ØP turns off isolating nodes A and B and the dummy cell capacitor. When the row address bits have been decoded and the row select is valid, $Ø_A$ turns on Q8 and Q10, the dummy cell and storage cell transistors respectively.

This connects the cell capacitors to the bit sense lines (Bit Sense Line Left [BSLL] and Bit Sense Line Right [BSLR]). If the voltage stored in C_{STG} is greater than the voltage stored in C_{DSTG} (V_{REF}), node A will be higher than node B. This voltage inequality will cause the sense amplifier (a cross-coupled latch made up of devices Q1 and Q2) to switch when load devices Q3 and Q4 are turned on by $Ø_B$. The latch will switch node B to V_{SS} and node A to $\sim V_{DD}$ due to the regenerative action of the latch. $Ø_B$ is delayed from $Ø_A$ sufficiently to allow the voltages on nodes A and B to stabilize prior to enabling the sense amplifier. If the voltage stored in C_{STG} had been less than that stored in C_{DSTG}, the latch would have sensed a low and switched such that node A would be at V_{SS} and node B would be at $\sim V_{DD}$.

After the stored level has been sensed against the reference level, the sense amplifier will have forced BSLL to a level corresponding to the level originally stored in the storage cell capacitor (V_{DD} if $V_{CSTG} > V_{REF}$ or V_{SS} if $V_{CSTG} < V_{REF}$). Since the storage cell transistor (Q10) is still turned on, the storage cell capacitor will be charged to the BSLL level. This effectively restores the sensed data into the cell capacitor but at full levels, not leakage or noise degraded levels. This is also what occurs when a storage cell is refreshed, the data integrity is restored through the sensing function.

Note that the stored level only has to be greater than or less than V_{REF}, not full V_{DD} or V_{SS} levels. This is important because leakage currents from the storage cell capacitor degrades a stored high level toward V_{REF} while system ground noise degrades a stored low level toward V_{REF}. Leakage degraded high levels are the most serious design problem and V_{REF} is generally set closer to V_{SS} than to V_{DD} to counteract the leakage effects. Leakage of stored high levels is also the reason dynamic storage RAMs must be periodically refreshed.

Data Storage

The block diagram in Figure 2 shows that the two 8192-bit arrays in the 2116 share a common I/O bus and common column decoders. The simplified schematic of Figure 4 shows one set of corresponding columns from the two arrays with their sense amplifiers and I/O gating. As shown, the I/O bus consists of two parallel, opposite polarity data lines which connect the column(s) to the Data In and Data Out latches. Referring to the previous discussion of the operation of the sense amplifiers and storage cells, a "stored level" or data map may be developed for the 2116.

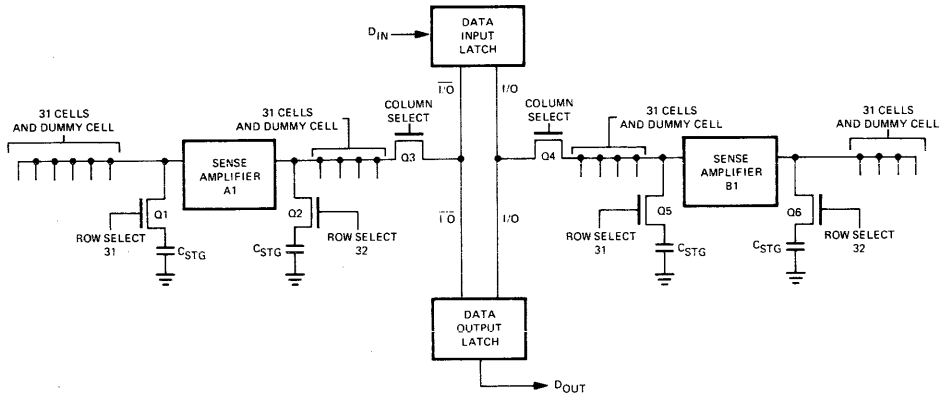


Figure 4. I/O Line and Data Column Schematic

Column select device (Q3) connects sense amplifier A1 and its related storage cells to the $\overline{I/O}$ line. Data stored in the cells on A1's BSLR will be inverted with respect to the data level at the Data Input (D_{IN}). Data in the cells on BSLL will be the same polarity as D_{IN} since the I/O bus data is inverted through the sense amplifier. Conversely, sense amplifier B1 and its related cells are connected to the I/O line by device Q4 and data on it's BSLL will be D_{IN} while data on it's BSLR will be $\overline{DIN}$. These data inversions are internal to the 2116 and are invisible to the user since D_{OUT} will be the same polarity as D_{IN}. The data map for the 2116 is therefore, as shown in Figure 5. This figure also indicates the address map for the 2116.

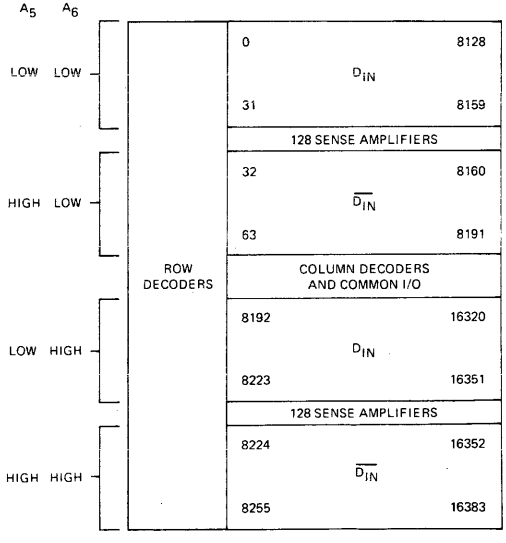


Figure 5. 2116 Address and Data Map

Address Latches

The 7-bit row and column address words are latched into internal latches by $\overline{RAS}$ and $\overline{CAS}$ respectively. These latches capture the TTL level address information on the shared address input pins and convert the TTL levels to the MOS levels (12V) required internally by the 2116.

Data Latches

Both the Data Input (D_{IN}) and Data Output (D_{OUT}) information is latched by the 2116. The input data is latched by the logical AND function of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$. When a data cycle is being performed ($\overline{RAS}$ low), D_{IN} will be latched by the falling edge of the last of the two control signals ($\overline{CAS}$ or $\overline{WE}$) to go low. In a "fast" write cycle,i.e., $\overline{WE}$ low before $\overline{CAS}$ goes low, the $\overline{CAS}$ edge will operate the latch. In a "late" write ($\overline{CAS}$ low before $\overline{WE}$ goes low) or read-modify-write cycle, D_{IN} is latched by the falling edge of $\overline{WE}$.

The Data Output (D_{OUT}) latch and buffer is controlled by $\overline{CAS}$. The leading (falling) edge of $\overline{CAS}$ in any cycle causes D_{OUT} to assume an open-circuit (HI-Z) state. At access time (t_{RAC} or t_{CAC}), D_{OUT} will assume a data state (high or low) dependent upon the type of data cyle performed or will remain in the HI-Z state if the cycle was a $\overline{CAS}$-only deselect cycle. The D_{OUT} state is latched and remains valid until the next cycle during which a $\overline{CAS}$ occurs. Table I summarizes the states the data output assumes for each type of 2116 cycle.

Refresh Modes

The data stored in the 2116 single transistor storage cells may be refreshed in any of three modes. The cells must be refreshed every 2msec.

Read Cycle Refresh: A read cycle at each of the 128 row addresses (A_0 - A_6) of the 2116 will refresh all the storage cells. This refresh mode is useful only when the memory system consists of a single row of devices (16K words X n-bits) and OR-tying of outputs is not necessary. Each device will access data during the refresh cycle and OR-tying of device outputs would result in conflict between devices for the output data bus. Write cycles also fulfill the refresh requirement but the selected cell (determined by the column address) on the row being refreshed will have new data written into it while the remaining 127 cells on the row are simply refreshed.

Table 1. Data Output Content

Type of Cycle	Data Latch Content (D_{OUT})
Read Cycle	Data from Addressed Memory Cell
Write Cycle	Input Data (D_{IN})
$\overline{RAS}$-Only Cycle	Data from previous Cycle or HI-Z if Device was Deselected in previous Cycle
$\overline{CAS}$-Only Cycle	HI-Z (CAS-Only Deselects Device and Turns Output Buffer Off)
R-M-W Cycle	Data Read from Addressed Memory Cell During Read Portion of Cycle
Page Mode Entry Cycle	Data from Addressed Memory Cell
Page Mode Read Cycle	Data from Addressed Memory Cell
Page Mode Write Cycle (or Page Mode Write and Exit Cycle)	Input Data (DIN)

$\overline{RAS}$-Only Refresh: A cycle with only the $\overline{RAS}$ clock active, performed at each of the 128 row addresses will refresh the 2116 storage cells. This mode is useful when the memory system consists of multiple rows of devices. The data outputs of the RAMs may be OR-tied when $\overline{RAS}$-only refresh cycles are performed since the D_{OUT} line of each 2116 will remain unchanged during the refresh cycle.

$\overline{CAS}$-Before-$\overline{RAS}$-Refresh: The 2116 storage cells may be refreshed with only 64 cycles each 2msec if the $\overline{CAS}$-before-$\overline{RAS}$ mode is used. In this mode, initiated by $\overline{CAS}$ being valid (low) when $\overline{RAS}$ goes low, both 8KX1 halves (see Figure 2) of the 2116 are turned on and one row in both halves is refreshed during each cycle. Since there are 64 rows of cells in each half, only 64 cycles are required to refresh all the cells. This refresh mode is also useful in systems with multiple rows of devices since receipt of a $\overline{CAS}$ before the $\overline{RAS}$ turns off all device outputs, thereby preventing OR-tied data conflicts.

APPLICATIONS INFORMATION

The Intel® 2116 is functionally compatible with the industry standard Intel® 2104A 16-pin 4K RAM. It is pin compatible with the 2104A with the exception of the seventh address bit (A_6) input pin. The 4K RAM uses that pin as the Chip Select ($\overline{CS}$) input pin. The $\overline{CS}$ signal on the 4K RAMs was essentially treated as a seventh column address bit and, therefore, there is considerable similarity between the 16K and 4K 16-pin RAMs.

The following applications information will concentrate on designing compatible 4K/16K memory systems rather than on just using the 2116. Additional basic applications information on the use of 16-pin, multiplexed address RAMs is contained in the next section of this Handbook.

Implementing Refresh

The 2116 may be refreshed in any of three modes. Read cycles and $\overline{RAS}$-only cycles refresh the row of storage cells (1 of 128 rows) addressed by A_0 through A_6 and, therefore, require 128 cycles each 2msec to refresh the stored data. The third 2116 refresh mode, $\overline{CAS}$-before-$\overline{RAS}$, refreshes two rows of storage cells during each cycle and, therefore, only requires 64 cycles each 2 msec to refresh the stored data.

The 2104A is compatible with all three 2116 refresh modes. A very simple compatible refresh system would perform 128 $\overline{RAS}$-only refresh cycles each 2 msec on both the 2104A and 2116. The 2104A would of course be refreshed twice as often as necessary but this is not a problem. The advantage would be that no logic or timing change would be necessary to differentiate between the 4K and 16K RAMs for refreshing.

Read cycles could also be used with 128 cycles each 2 msec but the 2104A $\overline{CS}$ input would need to be driven high (deselected) during each cycle to prevent data bus conflicts between OR-tied 2104A data outputs during refresh. This requires a logic control funtion of $\overline{CS}$ during refresh (and read cycles also dissipate more power than $\overline{RAS}$-only cycles) so most systems will use $\overline{RAS}$-only refresh.

Each of the first two refresh modes require 128 refresh cycles each 2 msec. Assuming a system cycle time of 500 nsec, 3.2% of the available memory time is required for refreshing. In many systems, this loss of memory availability is of no consequence. In the high throughput memory system environments found in many large and mid-sized computer systems, however, any loss of memory availibility is undesireable.

For these systems, the 64 cycle refresh mode is advantageous since it requires only 1.6% of the available memory line, a 50% savings over 128 cycle refresh. It is also compatible with the 4K RAM systems presently in use since the the 4K RAMs require only 64 refresh cycles each 2 msec.

The 2116 automatically goes into its 64-cycle refresh mode when $\overline{CAS}$ is low (active) at the time $\overline{RAS}$ goes low (active). When this $\overline{CAS}$-before-$\overline{RAS}$ condition is satisfied, the 2116 ignores address bit A_6 and refreshes one row in each half of the device, thus refreshing all 128 rows of storage cells in only 64 cycles. Address bits A_0 through A_5 determine which rows are refreshed. The 2104A will also accept the $\overline{CAS}$-before-$\overline{RAS}$ cycle and will simply perform a READ cycle on the row addressed by address bits A_0 through A_5, thereby refreshing the row of storage cells. The 2104A $\overline{CS}$ input should be driven high (unselected) during this refresh mode to prevent conflicts between OR-tied data outputs just as with normal read cycle refreshing.

Address Multiplexing/Refresh Timing

After the refreshing mode has been selected, the address multiplexer and refresh address counter/timer must be configured to support the selected operational mode. The simplest compatible mode (128-cycle $\overline{RAS}$-only refresh) will again be developed first. Figure 6 shows the detailed block diagram of the logic required to perform the multiplexing/refresh function for the 2104A/2116 compatible system. An implementation of the required logic using the Intel® 3222 and Intel® 3242 Schottky TTL memory support devices is shown in Figure 7.

The 2104A requires 12 address bits multiplexed into 6 address input pins plus a Chip Select ($\overline{CS}$) input. The 2116 requires 14 address bits multiplexed into 7 address input pins and no $\overline{CS}$ signal. Rather than requiring jumpers or strapping at each address multiplexer input pin, the address assignments shown in Figure 1 are "scrambled" to minimize the strapping requirements as much as possible. This address scrambling effects only the column addresses to the 2116. It results in the column address to the memory devices progressing in the order 0, 2, 4, 6, ... , 124, 126, 1, 3, 5, 7, ... 125, 127 as the column address bits (A_9 through A_{13}) from the processor progress in the order 0, 1, 2, 3, 4, ... , 125, 126, 127. This does not effect refreshing since only the column address bits are scrambled. No system effects will result from this technique but it is necessary to be aware of the addressing characteristics while troubleshooting the system.

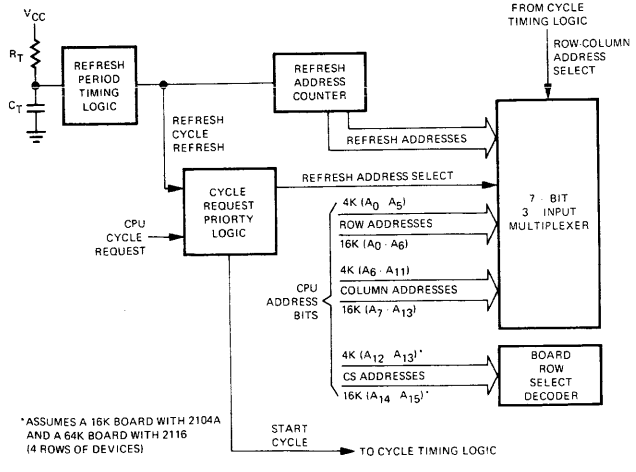


Figure 6. Detailed Block Diagram of Address and Refresh Logic

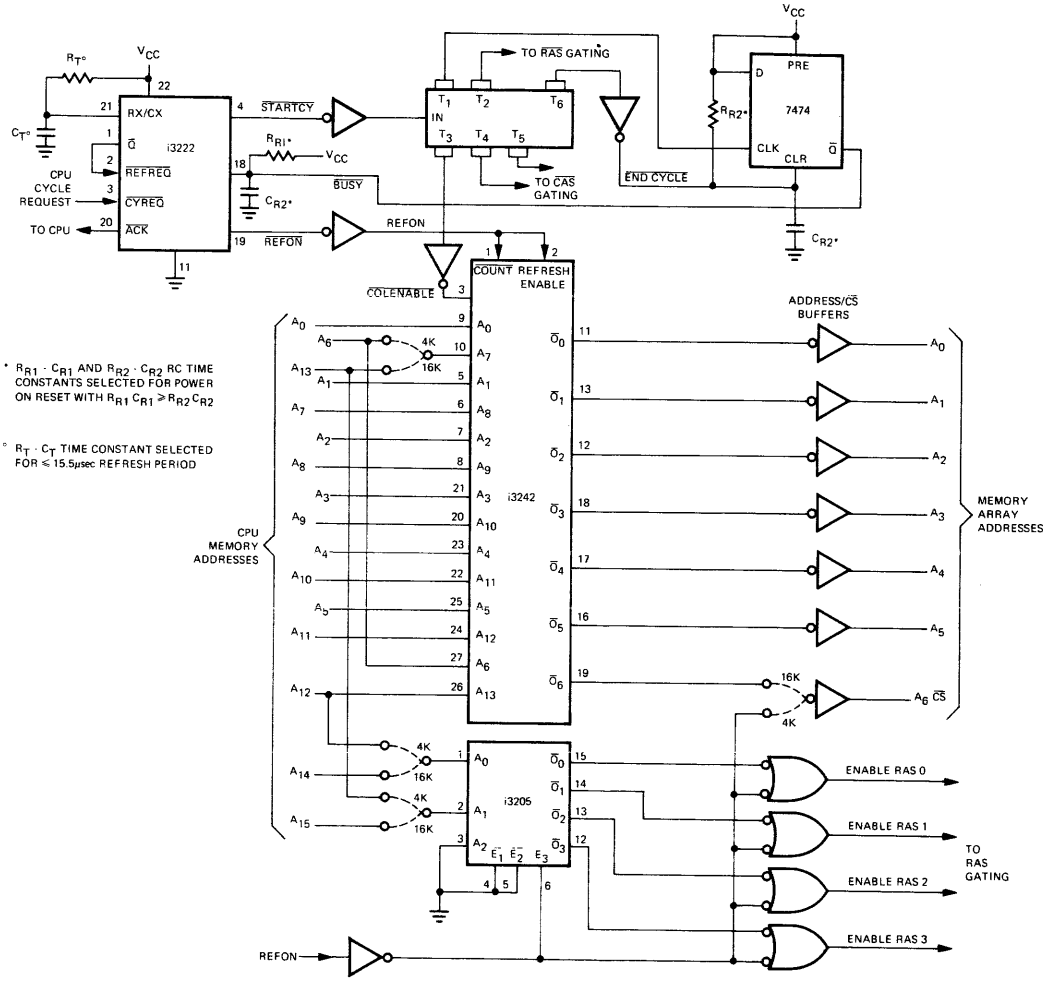


Figure 7. 4K/16K Memory System Control

The circuit of Figure 7 assumes a memory board configuration of four rows of memory devices (16K words X n-bits with the 2104A or 64K words X n-bits with the 2116). It also assumes that row selection will be via $\overline{RAS}$ gating for both the 2104A and 2116 and that the $\overline{RAS}$-only refresh mode will be used with both devices. The address decoding for row selection and $\overline{RAS}$ gating is performed by the 3205. Only address inputs A_0 and A_1 of the 3205 are used and the E3 enable input pin is used to inhibit the address decoding during refresh cycles.

Processor address bits A_{12} and A_{13} are decoded by the 3205 when the 2104A is used (14 system address bits total) and address bits A_{14} and A_{15} are decoded for row selection with the 2116 (16 system address bits total). This requires strapping of the proper system address bits into the 3205 as indicated in Figure 7.

A 74S00 quad Nand gate is used in an inverting OR gate configuration to provide either 1-of-4 $\overline{RAS}$ enables during data cycles or 4-of-4 $\overline{RAS}$ enables during refresh cycles to refresh all rows at once.

The 3242 includes the refresh address counter and the counter is incremented following each refresh cycle by the high-to-low transition of the REFRESH ENABLE signal at the 3242 $\overline{COUNT}$ input.

An optimization of the configuration of Figure 7 would be to select between 64-cycle refresh for the

2104 A and 128-cycle refresh for the 2116. This would optimize the memory availability for each device type while using $\overline{RAS}$-only refresh cycles. Figure 8 shows the modifications required on the circuit of Figure 7 to implement the refresh switching.

If 64-cycle refresh is desired for both the 4K and 16K RAMs, clock control logic is necessary to switch $\overline{CAS}$ low prior to $\overline{RAS}$ during refresh cycles.

The $\overline{CS}$ pin of the 2104A must also be driven high during refresh cycles to prevent data output bus conflicts. One possible logic configuration to perform the switching function is shown in figure 9.

Power Distribution/Decoupling

The recommended printed circuit board layout for the memory device array is shown in Figure 10. Notice that each power supply distribution system

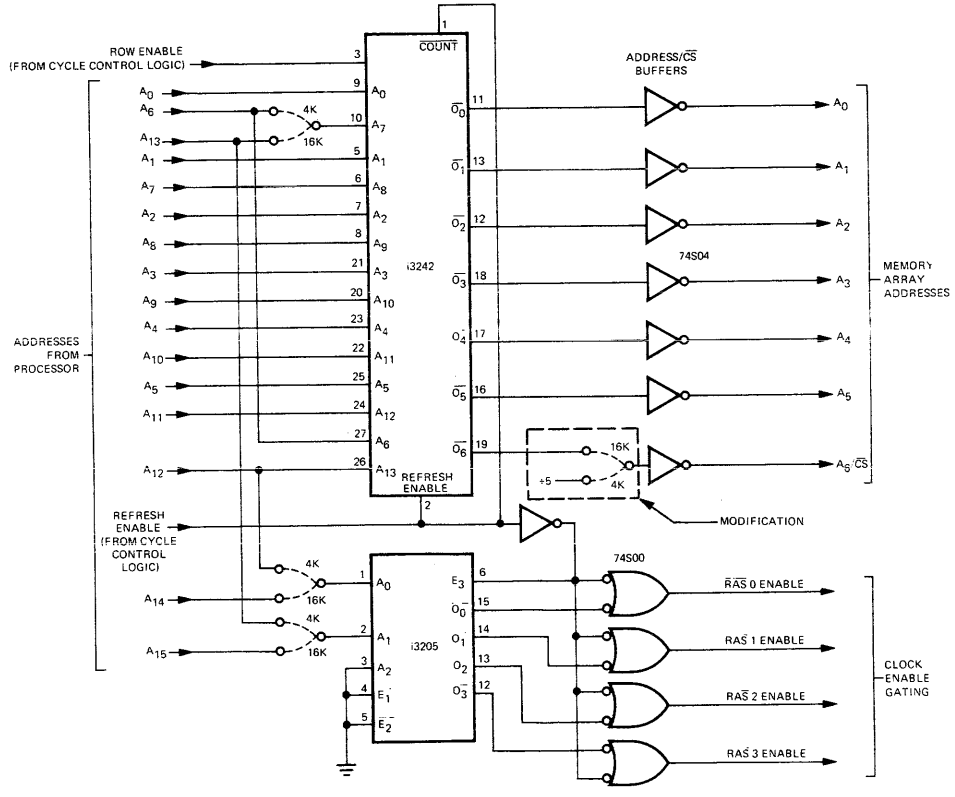


Figure 8. Refresh Timing Switching

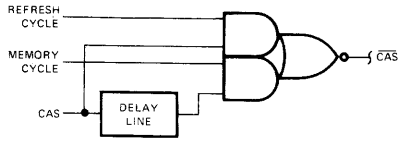


Figure 9. Multiplexed $\overline{CAS}$ for 64 Cycle Refresh

in this double-sided layout is gridded both horizontally and vertically at each device location. This technique provides a low inductance, high quality distribution system which performs as well as multi-layered layout techniques.

When the layout of Figure 2 and the following recommended decoupling capacitance values are used, power supply noise levels within the memory device matrix will be within the required operational limits for the 2104A and 2116.

Recommended decoupling for the 2104A is as Follows:

V_{DD}: A 0.1μF ceramic capacitor between V_{DD} and V_{SS} at every other device location.
A 10μF tantalum or equivalent bulk capacitor adjacent to the array for each 16 devices in the array.

V_{BB}: A 0.1μF ceramic capacitor between V_{BB} and V_{SS} at every other device location (preferably alternate devices to the V_{DD} decoupling).
A 10μF tantalum or equivalent bulk capacitor adjacent to the array for each 32 devices in the array.

V_{CC}: A 0.01μF ceramic capacitor between V_{CC} and V_{SS} for each 8 devices in the array.

Recommended decoupling for the 2116 is the same as for the 2104A with the following exceptions:

V_{DD}: Use 0.33μF ceramic capacitors rather than 0.1μF.
Use a 20μF tantalum rather than a 10μF.

A common configuration would be to use 0.33μF ceramics for V_{DD} decoupling with both the 2104A and 2116. Also use a 10μF tantalum on V_{DD} for each 8 devices in the array. The V_{BB} and V_{CC} decoupling would use the recommended values for the 2104A. This configuration would yield acceptable results with both the 4K and 16K devices and would most likely be more economical than using two different configurations.

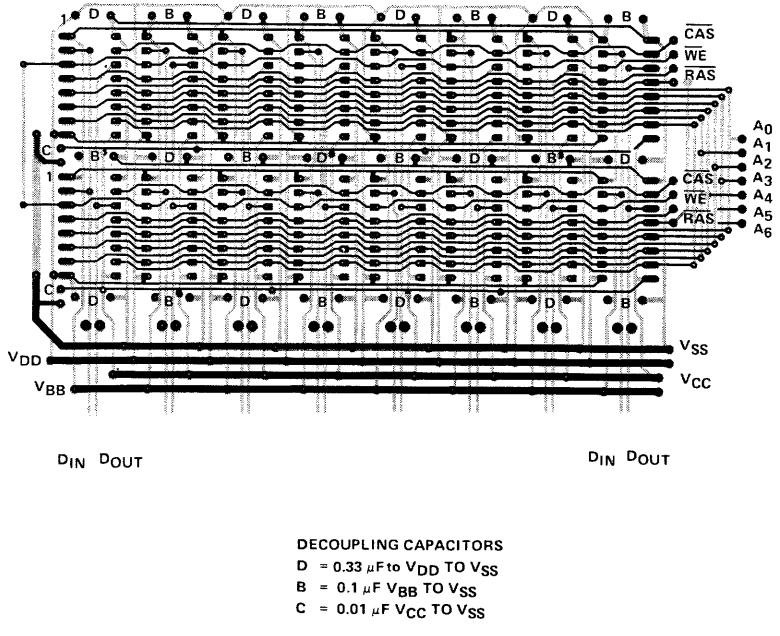


Figure 10. Recommended two-Sided Board Layout for 2116

Application of the Intel® 2104A 4k RAM

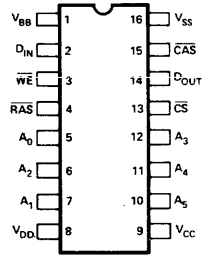
Jim Coe
Application Engineering

Contents

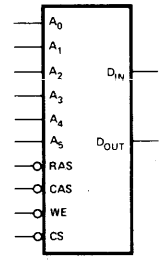
INTRODUCTION

The Intel® 2104A is a 4096 word by 1 bit dynamic random access memory. The 2104A is fabricated using Intel's proven n-channel silicon gate MOS technology. The device is packaged in a standard 16-pin DIP. The pin configuration and logic symbol are shown in Figure 1.

PIN CONFIGURATION



LOGIC DIAGRAM



PIN NAMES

A_0 - A_5	ADDRESS INPUTS	WE	WRITE ENABLE
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (-5V)
$\overline{CS}$	CHIP SELECT	V_{CC}	POWER (+5V)
D_{IN}	DATA IN	V_{DD}	POWER (+12V)
D_{OUT}	DATA OUT	V_{SS}	GROUND
$\overline{RAS}$	ROW ADDRESS STROBE		

Figure 1. 2104A Pin Assignments

The combination of Intel's n-channel silicon gate process and circuit design has resulted in a part that is fast, easy to use, and economically produced in large volume. In addition, the combination of process and device design has resulted in a small device using conservative layout rules. The small size offers advantages in both large volume production and increased reliability.

The 2104A operates with three power supplies relative to ground: V_{DD} (+12V), V_{BB} (-5V), and V_{CC} (+5V). The V_{CC} (+5V) supply is connected only to the output buffer of the 2104A and may be turned off during power down operations.

The unique design of the 2104A allows it to be packaged in the industry standard 16-pin dual-in-line package. The 16-pin package provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16-pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 2104A on 6 address input pins. The two 6-bit address words are latched into the 2104A by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

The dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention. Refreshing is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2 milliseconds.

The purpose of this application note is to describe the internal operation of the 2104A and outline those areas in system implementation to which the designer should pay particular attention.

DEVICE CIRCUIT OPERATION

Operation of the 2104A is most easily understood with the aid of the block diagram shown in Figure 2. As is shown in this figure, the memory array is arranged in a 64 row X 64 column matrix of storage cells. The storage cells are implemented with select transistors and "storage" capacitors. The operation of the storage cell will be discussed later. The cell is accessed by the coincidence of a row select (defined by addresses A_0-A_5) and a column select (defined by addresses A_6-A_{11}) signal at the desired address. On chip timing and control generators provide the internal timing signals for decoding, read/write strobing, data gating and output gating. All of the timing circuits in the 2104A are activated by the negative going edges of the two TTL clocks, $\overline{RAS}$ and $\overline{CAS}$.

BLOCK DIAGRAM

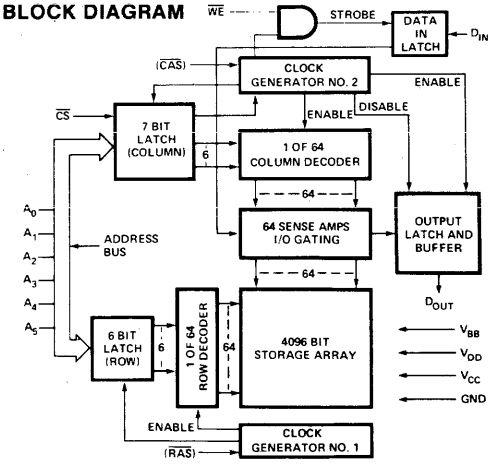


Figure 2. 2104A Block Diagram

Data Accessing

Prior to discussing the $\overline{RAS}/\overline{CAS}$ timing relationships, a discussion of the basic operation of dynamic 4K RAM devices is in order. Access of stored data from a dynamic memory device consists of two discrete retrieval operations. The first of these

operations is the selection of the desired row of storage cells (1 of 64 rows of 64 cells in the 2104A), sensing the data stored in each of the cells with sense amplifiers (64 sense amplifiers in the 2104A), and restoring the sensed data back into the cells since the readout is destructive. When this operation is complete, the sensed data (64 bits) is available at the output of the sense amplifiers. This operation may be completed with only the row address and a clock ($\overline{RAS}$ with the 2104A) having been supplied to the memory device. This first operation fulfills the refresh requirement on the selected row since data has been restored in the cells on the row.

The second operation consists of connecting the output of one of the sense amplifiers to the device data output via a multiplexer (64 to 1 in the 2104A) and latching the data into the output data latch. In essence, this is accessing data from the sense amplifier outputs rather than from the data cells. This operation requires a column address and a clock ($\overline{CAS}$ with the 2104A). This second operation is the characteristic which makes page-mode operation possible. Page-mode will be discussed in the Applications Information Section.

The two access operations may occur in parallel as in the 18-pin and 22-pin 4K RAMs or in a time sequential manner in a 16-pin 4K RAM such as the 2104A. With proper design techniques such as used in the 2104A, the sequential mode of operation may be used, saving package pins and with no performance loss as compared to the parallel mode RAMs.

In the parallel mode RAMs (such as the Intel® 2107B) all address information is applied to the RAM at the same time and both access operations occur simultaneously. The cell data access is the slower of the two operations and is the limiting factor in device speed. The selection of the proper sense amplifier output for connection to the device output is completed prior to the time it is necessary.

In the sequential mode 2104A RAM, cell data access is begun first by the latching in of the row address information (6-bits for 1 of 64 row select) by the $\overline{RAS}$. The access of data from the sense amplifier outputs is faster and thus may be started later without impacting overall access time [up to 70 nanoseconds ($t_{RCL(max)}$) later in the 2104A-2]. The 6-bit, 1 of 64 sense amplifier data address (column address) is latched into the 2104A-2 by the CAS. As long as the sense amplifier output data access is started prior to 70 nanoseconds into the memory cycle, the limiting access time is t_{RAC}, the data cell access time plus the propagation time through the sense amplifier data select multiplexer. This access time is the same as the parallel mode access time would be.

If the column address latching is delayed until later than 70 nanoseconds into the memory cycle, the limiting access time will become the sense amplifier data access time. In this instance, the access time will be t_{CAC} (access time from $\overline{CAS}$ which includes the sense amplifier output data multiplexer propagation time) plus t_{RCL} actual (the actual $\overline{RAS}$ to $\overline{CAS}$ delay time). It is obvious that it is desirable to latch the column address into the 2104A-2 at or prior to the 70 nanosecond point in the memory cycle to preclude lengthening of data access time.

In the 2104A-2, a 45 nanosecond window is provided during which $\overline{CAS}$ may be switched while maintaining device access time. In other words, the $\overline{CAS}$ leading edge may occur at any time between 25 and 70 nanoseconds following $\overline{RAS}$ and the access time will be t_{RAC}. Timing accuracy required between $\overline{RAS}$ and $\overline{CAS}$ is thus reduced. The advantages of this timing "window" will be discussed in the Applications Information Section.

Clock Input Buffers

The two device clocks, $\overline{RAS}$ and $\overline{CAS}$, are TTL compatible, active-low signals. The clock input buffers are inverters which convert the TTL levels to the MOS (12 volt) levels required within the 2104A. The major design consideration for these buffers is speed since it is desirable to respond to the clock inputs as quickly as possible to obtain minimum data access. The speed is obtained by implementing the inverters with high gain (large geometry) devices operating at relatively high current levels. The inverter circuit is shown in Figure 3.

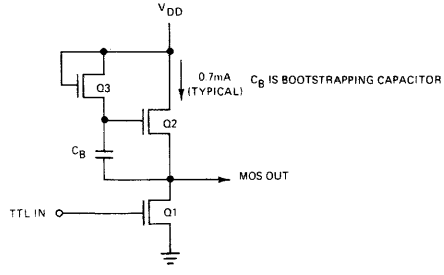


Figure 3. Simplified CLOCK Input Buffer

The inverter uses a bootstrapped, 0.7 milliampere (typical) load device. The bootstrapping is used to assure that the load device (Q2) is fully turned-on so that the drain voltage of Q1 reaches V_{DD}. Without the bootstrapping, the drain of Q1 would only reach V_{DD}-V_T where V_T is the load device threshold voltage. This would slow down the inverter operation and affect the response time to the clock(s).

The current requirement of the input buffer accounts for the difference in standby power levels between the 16-pin TTL clock devices and the 18 or 22-pin MOS clock devices. When the $\overline{RAS}$ clock is inactive (high), the 2104A $\overline{RAS}$ buffer is on and the inverter load current (2.0mA maximum) is drawn from The V_{DD} supply yielding the 26.4mW maximum standby power specification. MOS clock devices (such as the Intel® 2107B) have inactive low clocks and no buffer is on during standby, yielding standby power specifications under 3mW maximum (leakage currents only). This standby power reduction at the memory device level is offset at the system level by the larger power dissipation levels of MOS level clock driver devices versus TTL level drivers. The 2104A TTL clock inputs are lower in capacitance than the MOS clock inputs (7 picofarads versus 25 picofarads). At a given speed, this means a typical TTL driver can drive 32 2104A clock inputs while a typical MOS clock driver can drive only 10 2107B clock inputs.

Address Buffer/Latch

The TTL-level compatible address buffer/latch circuit is shown in Figure 4. This circuit senses the input TTL level, translates it to MOS signal levels, and latches the address information. There are two groups of six input buffer/latches in the 2104A; one for the six row addresses and one for the six column addresses. The operation of each group of latches is the same except for the clock signals which control their function.

The operation of the address buffer/latch is as follows: During the clock ($\overline{RAS}$ or $\overline{CAS}$) off time (t_{RP} or t_{CP}) both sides of the latch (Nodes A and B) are precharged to V_X (≈10 volts) by devices Q7 and Q9. Device Q8 is turned on during the precharge period to assure that the two nodes charge to the same potential. Internal signal ϕ_P controls the precharge devices and is on while the $\overline{RAS}$ and $\overline{CAS}$ clocks are off (at V_{IH}). When the appropriate system clock ($\overline{RAS}$ or $\overline{CAS}$) goes low (active), ϕ_P turns off isolating the two precharged nodes and internal clock phase ϕ_A turns on connecting the TTL address (A_{IN}) to Node C (the gate of the input buffer device Q_2 and capacitor C_1). Clock phase ϕ_A stays on for the address hold time (t_{AH}) and then turns off isolating Node C from the shared address input pin. The TTL level which was on the address pin during t_{AH} is still stored on capacitor C_1 allowing the address latch additional time to capture the address. This "sample and hold" technique allows short address hold times to be achieved.

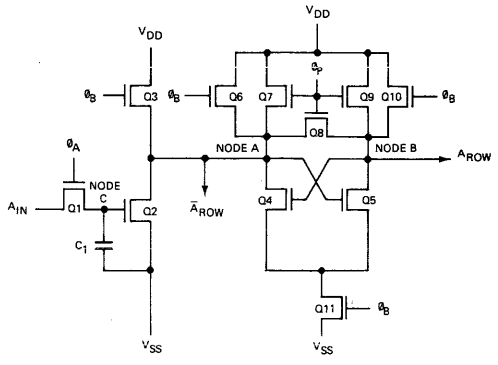


Figure 4. Simplified Address Buffer/Latch Schematic

Internal clock phase ϕ_B turns on after a slight delay from phase ϕ_A turning on. Phase ϕ_B enables the buffer/latch by turning on load devices Q_3, Q_6, and Q_{10}. The buffer (Q_2 and Q_3) converts the TTL level address input to MOS levels (V_{SS} and V_{DD}) and drives Node A of the latch. The delay between ϕ_A and ϕ_B is to allow the voltage at Node C to stabilize prior to enabling the buffer/latch.

A TTL high level at the address input will force Node A to V_{SS}. The cross-coupled latch devices (Q_4 and Q_5) will then switch driving Node B to V_{DD}. Conversely, a TTL low level at the address input will force Node A to ~V_{DD} and Node B to V_{SS}. Since the buffer/latch is isolated from the address input after t_{AH}, the latched address will remain in the latch even though the TTL level at the address input may change due to the multiplexing of the addresses.

Data Sensing

A major contributor to the operating margins of the 2104A is the use of two single-transistor storage cells per bit of storage. The effect of using two cells per bit rather than one is best understood by comparison of the data sensing function when used with one and two cells per bit.

Figure 5 illustrates the commonly used sense amplifier and reference voltage scheme for single cell per bit 4K RAMs. The sense amplifier in Figure 5 senses data stored in a storage cell by comparing the voltage level in the storage cell capacitor to the voltage level in the cell capacitor of a "dummy" storage cell. The dummy cell capacitor contains a voltage which is less than the minimum high level and greater than the maximum low level which may be stored in the storage cell capacitor. The sense amplifier then senses the differential level between the storage and dummy cell capacitor voltages. The level stored in the dummy cell would ideally be equal to one-half the difference between a minimum written high and a maximum written low as this would yield a maximum differential across the sense amplifier during sensing. Unfortunately, leakage currents from the storage capacitors degrade the written high levels toward the written low levels. This normally requires that the designer set the dummy storage cell level lower (closer to a low level than a high level) to compensate for leakage degradation of a stored high level. Although this "lower" reference level tends to compensate for a leakage degraded high level, it also makes it more difficult to sense a ground (V_{SS}) noise degraded low level. Thus, designs with dummy reference cells must necessarily be a compromise in the maximum differential level between the storage and dummy cells and can never have a differential greater than one-half the difference between a high and low level.

The dummy cell technique is used (rather than simply developing a reference voltage level with a resistive divider) because it contributes to the capacitive balance of the sense amplifier.

The sense amplifer of Figure 5 will operate with maximum margins only when the capacitance seen by Node B is the same as the capacitance seen by Node A, i.e., the capacitances are equal or balanced. The capacitances of the left (BSLL) and right (BSLR) bit sense lines as well as the dummy cell and storage cell capacitances can be made approximately equal by layout constraints. The effect of the I/O line connection to the right bit sense line is to add capacitance on the right bit sense line which is not offset or balanced by capacitance on the left bit sense line. The placement of the dummy cell on the bit sense line also contributes to capacitance imbalance since its location is not a mirror image of the accessed storage cell. The resistive effects of the bit sense line magnify the effect of this placement disparity during the data sensing process. The ideal situation would be a dummy cell mirroring the placement of the accessed data cell and a balancing capacitance to the I/O connection capacitance.

This is essentially the technique used in the Intel® 2104A. Instead of a dummy cell containing a reference level of one-half a minimum high level, the 2104A stores the full opposite data level in a mirror image storage cell physically located near the accessed storage cell as shown in Figure 6. Not only does this mean that the storage cell and "image" cell capacitance and location with respect to the sense amplifier are equal, but the data level is now being sensed against the full opposite level rather than one-half of the minimum high level. Thus, the sense amplifier is seeing the maximum possible differential signal during the sensing operation.

Also, notice in Figure 6, that there is an I/O connection to each bit sense line rather than only to one. The I/O capacitance contribution to the bit sense line capacitance is therefore equal, contributing again to the overall balance of the sense amplifier.

The 2104A sense amplifier sees essentially equal capacitances at nodes A and B and this contributes greatly to the margins of the sensing operation. This balance of the sense amplifier and the sensing of data against a reference of a full opposite level allows the cell capacitors to be a smaller value than with the dummy cell approach (for equal margins) and allows 8192 cells to occupy only slightly more chip area than 4096 cells previously occupied in the Intel® 2104.

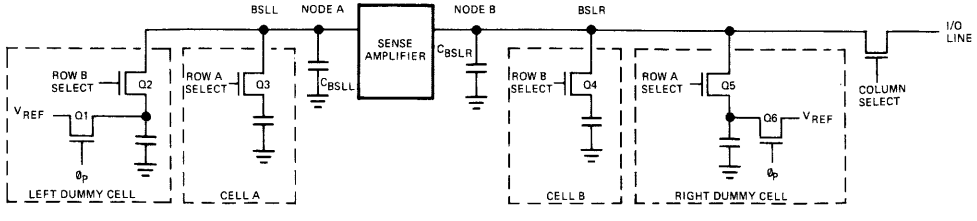
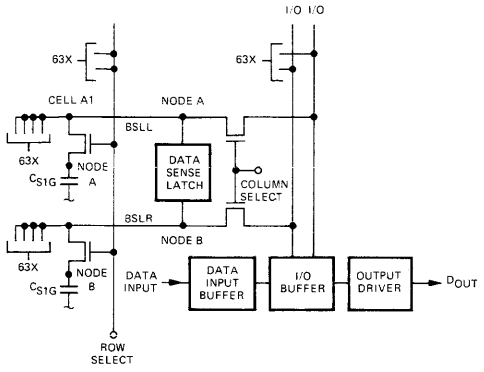


Figure 5. Old Dummy Cell Data Sensing Technique



- Each storage location consists of two cells. Each cell is formed by single transistor and storage capacitor as shown.
- At row select time, two cells are turned on simultaneously to gate the data to the data sense latch.
- Data is stored in a given address location as both a high and a low on each of the two respective data cells.

Figure 6. 2104A Image Cell Data Sensing Technique

Data Sense Amplifier

The data sense amplifier of the 2104A is a cross-coupled static latch as shown in Figure 7. The state

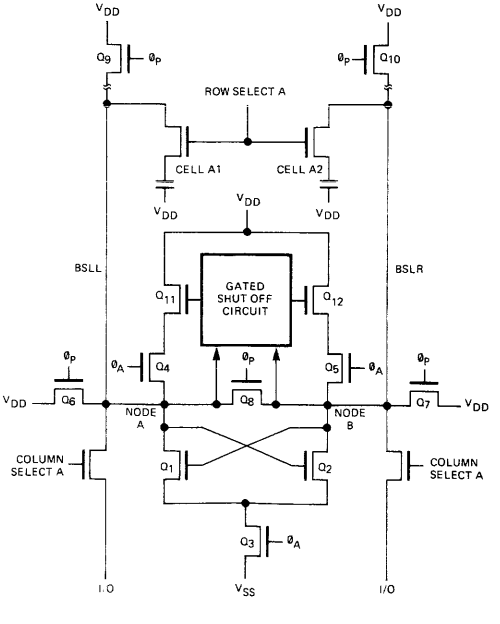


Figure 7. Simplified Data Sense Amplifier Schematic

the latch assumes during sensing of the stored data depends upon the differential voltage between nodes A and B. If the voltage on node A is higher than the voltage on node B, transistor Q_2 will turn on switching node B and the gate of transistor Q_1 to V_{SS} turning transistor Q_1 off. Conversely, if the voltage on node B is higher than the voltage on node A, transistor Q_1 will turn on while transistor Q_2 will be turned off. Devices Q_4 and Q_5 act as loads for the switching transistors Q_1 and Q_2, respectively. Additional transistors (Q_6 through Q_{10}) shown in the circuit diagram of Figure 7 serve to precharge nodes A and B to $\sim V_{DD}$ in preparation for the next memory cycle. This precharging assures that the sense amplifier and bit sense lines begin each memory cycle in the same known condition or state with no "history" or "memory" of data from previous cycles eliminating data pattern effects on the sensing function. Note that the 2104A has precharge transistors connected to both ends of the bit sense lines to speed up the precharging of the lines and sense amplifier. This increases the timing margin of the clock off time (t_{RP}) and enables the 2104A to run short memory cycles without degradation of the precharge function. The "folded", close proximity bit sense lines shown in Figure 6 and transistor Q_8 of Figure 7 assure that the precharge level of each pair of bit sense lines and the associated sense amplifier nodes reach the same precharge level contributing to the balance of the sensing function.

Transistor Q_3 in Figure 7 turns the sense amplifier on by completing the current path to V_{SS} when the row address bits have been decoded and the desired row of storage cells selected. The gated shutoff circuit controls transistors Q_{11} and Q_{12} to reduce the power dissipation of the sense amplifier following the sensing of the stored data. The shutoff circuitry senses the levels on Nodes A and B and turns off the load current to the switching transistor (Q_1 or Q_2) which is turned on to V_{SS}. This reduces the I_{DD} current drawn by the sense amplifier and contributes to the low power dissipation of the 2104A.

Output Data Latch/Driver

A simplified schematic of the 2104A output data latch/driver is shown in Figure 8. The three operational states for the output driver are:

1) "1" output (Q_1 on and Q_2 off)
2) "0" output (Q_1 off and Q_2 on)
3) Open output (Q_1 and Q_2 off)

Devices Q_1 and Q_2 are large geometry devices which allow the output of the 2104A to source and sink the relatively large current levels associated with TTL interfaces. Devices Q_3 through Q_6 control the output driver stage in conjunction with the data latch.

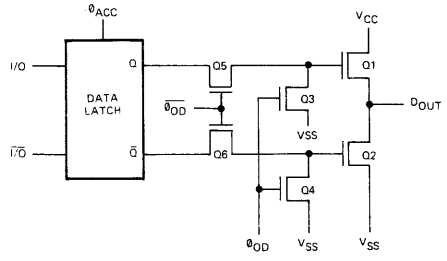


Figure 8. 2104A Output Data Latch and Buffer

The inputs to the latch are data from the selected cell and a clock phase (ϕ_{ACC}) which is related to access time from the cell matrix. At the proper time after the memory cycle starts, ϕ_{ACC} will go high, clocking the data from the selected cell into the latch. The Q and $\overline{Q}$ outputs of the latch then drive the gates of devices Q_1 and Q_2 controlling the output level. The accessed data will remain in the latch until the next cycle when new data will be clocked into the latch. During a write cycle, the data input to the latch is the data on the I/O lines which is the data to be written into the selected cells. The data latch will, therefore, contain the input data following a write cycle. The first two of the three possible output data states are, therefore, related to the data level stored in the latch.

The third or open-circuited state occurs when devices Q_1 and Q_2 are both off (gates at V_{SS}). Internal signal ϕ_{OD} turns on devices Q_3 and Q_4 connecting the gates of devices Q_1 and Q_2 respectively to V_{SS} from shortly after the $\overline{CAS}$ input switches low until data access time. This signal forces the data output to the open-circuited condition following $\overline{CAS}$ in every memory cycle guarantying that no two OR-tied data outputs in a system will be on at the same time.

The control clock phase ϕ_{OD} is a logic function of $\overline{CAS}$ and $\overline{CS}$. Table I lists the various combinations of $\overline{CAS}$ and $\overline{CS}$ and the corresponding states of ϕ_{OD}.

Devices Q_5 and Q_6 in Figure 8 are simply series switches which isolate the Q and $\overline{Q}$ outputs of the data latch from output devices Q_1 and Q_2 until the latch data has stablized. Q_5 and Q_6 are controlled by the inverse of ϕ_{OD} so that the latch is isolated from Q_1 and Q_2 when the gates of Q_1 and Q_2 are connected to V_{SS}.

Table I. Operational States of ϕ_{OD}

$\overline{RAS}$	$\overline{CAS}$	$\overline{CS}$	ϕ_{OD}	COMMENTS
LOW	LOW	HIGH	HIGH	Device Deselected by $\overline{CS}$ (D_{OUT} = HI-Z)
LOW	LOW	LOW	LOW	Device Selected by $\overline{CS}$ (D_{OUT} = Data)
HIGH	LOW	Don't Care	HIGH	Device Deselected by $\overline{CAS}$ (D_{OUT}=HI-Z)

APPLICATIONS INFORMATION

Addressing

The 2104A RAM combines the advantages of a very high speed RAM with the high packing density of the industry standard 16 pin dual-in-line package. The use of the 16 pin package is made possible by multiplexing the 12 address inputs (required to access 4096 words) on 6 external address pins. Two externally applied negative going clocks, Row Address Select ($\overline{RAS}$), and Column Address Select ($\overline{CAS}$), are used to strobe the two sets of 6 address bits into the internal address buffer registers. The first clock, $\overline{RAS}$, strobes in the six low order address bits (A_0-A_5) which select one of 64 rows. The second clock, $\overline{CAS}$, strobes in the six high order address bits (A_6-A_{11}) which select one of 64 columns and Chip Select ($\overline{CS}$).

Note that $\overline{CS}$ and $\overline{WE}$ do not have to be valid until the second clock, $\overline{CAS}$. It is, therefore, possible to start a memory cycle *before* it is known which device must be selected or what type of cycle is to be performed. This can result in a significant improvement in *system* access time since the decode time for chip selection does not enter into the calculation for access time.

Read Cycle

A memory cycle begins with addresses stable and a negative transition of $\overline{RAS}$. The data-out pin of the selected device will unconditionally go to a high impedance state immediately following the leading edge of $\overline{CAS}$ and remain in this state until valid data appears at the output (refer to the Data Output Operation Section). The selected output data is internally latched and will remain valid until a subsequent $\overline{CAS}$ is given to the device by a Read, Write, Read-Modify-Write or Refresh cycle. Data-out goes to a high impedance state for all non-selected devices ($\overline{CS}$ high) that receive $\overline{RAS}$ and $\overline{CAS}$.

Device access time, t_{ACC}, is the longer of two calculated intervals:

1) $t_{ACC} = t_{RAC}$

OR

2) $t_{ACC} = t_{RCL} + t_T + t_{CAC}$

Access time from $\overline{RAS}$, t_{RAC}, and access time from $\overline{CAS}$, t_{CAC}, are device parameters. Row to column address strobe lead time, t_{RCL}, and transition time, t_T, are system dependent timing parameters.

Substituting the device parameters for the 2104A-2 and assuming a TTL level transition time of 5nS yields:

3) $t_{ACC} = t_{RAC} = 200ns$ for $t_{RCL} + t_T \leq 70$ ns
OR

4) $t_{ACC} = t_{RCL} + t_T + t_{CAC} = t_{RCL} + t_T +$ 130ns for $t_{RCL} + t_T > 70ns$

Note that if $t_{RCL} + t_T \leq t_{RCLmax}$, device access time is determined by equation 3 and is equal to t_{RAC}. If $t_{RCL} + t_T > t_{RCLmax}$, access time is determined by equation 4. A 45ns interval ($t_{RCLmax} - t_{RCLmin}$) in which the falling edge of $\overline{CAS}$ can occur without affecting the access time is provided to allow for system timing skew in the generation of $\overline{CAS}$. This "designed in" skew window at the device level allows minimum access times to be achieved in practical system designs.

Note that both the $\overline{RAS}$ and $\overline{CAS}$ clocks are TTL compatible and do not require external level shifting to high voltage MOS levels. Internal buffers in the 2104A convert the TTL level signals to MOS levels inside the device. Therefore, the delay associated with external TTL-MOS level converters is not added to the 2104A system access time.

Write Cycle

A Write Cycle is performed by bringing Write Enable ($\overline{WE}$) low before or during $\overline{CAS}$. If Write Enable goes low at or before $\overline{CAS}$ goes low, the input data must be valid at or before the $\overline{CAS}$ falling edge. If Write Enable goes low after $\overline{CAS}$, Data In must be valid at or before the falling edge of WE. If Write Enable is low before $\overline{CAS}$ goes low, the data-out buffer will contain the written data at access time. However, if Write Enable goes low *while* $\overline{CAS}$ is low, a read operation may also be performed and data-out will go either high or low depending on the state of the accessed cell before the write takes place (refer to the Data Output Operation Section).

Refresh

Each of the 64 rows internal to the 2104A must be refreshed every 2 msec to maintain data. Any data cycle (Read, Write, Read-Modify-Write) refreshes the entire selected row (defined by the 6-bit row address). The refresh operation is independent of the state of $\overline{CS}$. It is evident, of course, that if a Write or Read-Modify-Write cycle is used to refresh a row, the device should be deselected ($\overline{CS}$ high) if it is desired not to change the state of the selected cell. $\overline{RAS}$-only cycles may also be used to refresh the 2104A at a savings in power dissipation over data cycles.

Page Mode Operation

Page mode operation with the 2104A allows faster successive memory data operations at the 64 *column* locations in a single address *row*. Receipt of a $\overline{RAS}$ and a 6-bit row address byte causes the RAM to access the 64 data cells on the addressed row.

At access time all 64 data bits are available at the sense amplifier outputs as long as $\overline{RAS}$ is held active. By cycling the $\overline{CAS}$ clock and addressing the desired data bit with the 6-bit column address byte all 64 data bits may be brought to the data output of the device. Data access and cycle time in this mode, called page mode, is faster than normal data cycles. Page mode is an excellent way to transfer blocks of data to and from memory at high speed, but it is impacted by refreshing.

The refresh requirements of the device limits the number of consecutive page mode cycles that may be performed. The device may remain in the page mode for a period no longer than the time required between refresh cycles. As an example, recall that the distributed refresh mode requires a refresh cycle every 31 microseconds. $\overline{RAS}$ may then remain low (active) for 31 microseconds maximum before it must be cycled high to precharge and then perform a refresh cycle. System page mode cycle times of 485 nanoseconds or less will enable all 64 data bits in the selected row to be examined or written between refresh cycles, maximizing the usefulness of page mode.

Power Dissipation/Operating

The power dissipation of a continuously operating 2104A device is the sum of $V_{DD} \times I_{DD}$ and $V_{BB} \times I_{BB}$. For a cycle time of 320 ns (including a t_{RP} of 100ns) the typical power dissipation of the 2104A-1 is 289 mW.

Standby Power-Refresh Only

The standby power-refresh only is calculated by the following equation:

1) $$P_{REF} = P_{OP} \left(64\frac{t_{CYC}}{t_{REF}}\right) + P_{SB}\left[1-\left(64\frac{t_{CYC}}{t_{REF}}\right)\right]$$

Where:

P_{REF} = Standby power-refresh only.
P_{OP} = Power dissipation-continuous operation.
t_{CYC} = Refresh cycle time.
t_{REF} = Refresh period.
P_{SB} = Standby power dissipation.

RAMs

Table II. 2104A Family Current Specifications

Symbol	Parameter	Limits Typ	Limits Max	Units	Comments
I_{DD1}	V_{DD} Standby Current	0.7	2.0	mA	V_{DD} = 13.2 Volts
I_{DD2}	V_{DD} Data Cycle Operating Current	24	35	mA	2104A-1 t_{CYC} = 320 ns
		22	32	mA	2104A-2 t_{CYC} = 320 ns
		20	30	mA	2104A-3,-4 t_{CYC} = 375 ns
I_{DD3}	V_{DD} $\overline{RAS}$-Only Cycle Operating Current	12	25	mA	2104A-1,-2 t_{CYC} = 320 ns
		10	22	mA	2104A-3,-4 t_{CYC} = 375 ns
I_{BB1}	V_{BB} Standby Current	5	50	μA	
I_{BB2}	V_{BB} Operating Current	160	400	μA	Minimum Cycle Time

The standby power dissipation P_{SB} is given by:

2) $P_{SB} = V_{DD} \times I_{DD1} + V_{BB} \times I_{BB1}$

The operating power P_{OP} is given by:

3) $P_{OP} = V_{DD} \times I_{DD2} + V_{BB} \times I_{BB2}$

for read and write data cycles or by:

4) $P_{OP} = V_{DD} \times I_{DD3} + V_{BB} \times I_{BB2}$

for $\overline{RAS}$-only refresh cycles.

Table II lists the pertinent current values for the 2104A family of devices.

Calculating the standby-refresh only power dissipation for the 2104A-1 using equations 1 through 4 above and the data from Table II yields:

a) For $\overline{RAS}$-only Refresh:

P_{REF} = 330mW (0.01) + 26.7mW (0.99) = 29.7mW maximum

b) For Read or Write Cycle Refresh:

P_{REF} = 462mW (0.01) + 26.7mW (0.99) = 31.0mW maximum

at V_{DD} = 13.2 volts, V_{BB} = -5.5 volts and the specified maximum current levels.

Table III. Data Latch Content at End of Cycle

Type of Cycle	Data Latch Content (D_{OUT})
Read Cycle	Data from Addressed Memory Cell
Write Cycle	Input Data (D_{IN})
$\overline{RAS}$-Only Cycle	Data from Previous Cycle or HI-Z if Device was Deselected in Previous Cycle
$\overline{CAS}$-Only Cycle	HI-Z ($\overline{CAS}$-Only Deselects Device and Turns Output Buffer Off)
R-M-W Cycle	Data Read from Addressed Memory Cell During Read Portion of Cycle
Page Mode Read and Entry Cycle	Data from Addresssed Memory Cell
Page Mode Read Cycle	Data from Addressed Memory Cell
Page Mode Write Cycle (or Page Mode Write and Exit Cycle)	Input Data (D_{IN})

Data Output Operation

The operation of the output data latch is controlled by the $\overline{CAS}$ clock. Figure 9 indicates the content of the data latch following access time during various types of 2104A memory cycles. Table III summarizes the information on data content shown in Figure 9.

POWER DISTRIBUTION/DECOUPLING

General

Typical I_{DD} and I_{BB} current waveforms for the 2104A are shown in Figure 10. Examination of these waveforms shows that transient current drawn from the memory circuit board power distribution system is a function of the two device clocks, $\overline{RAS}$ and $\overline{CAS}$. The peak amplitude of the V_{DD} current transients is approximately 60 milliamperes with rise and fall times in the 5 to 10 nanosecond range and widths of typically 20 nanoseconds. Rise and fall times of this magnitude generate significant harmonic noise components in the 10 MHz and above frequency region. The power distribution/decoupling techniques used to suppress these noise components must be effective at these higher frequencies. The series inductance of the circuit board traces and the decoupling capacitors must be minimized to reduce time constant response effects of the distribution/decoupling system.

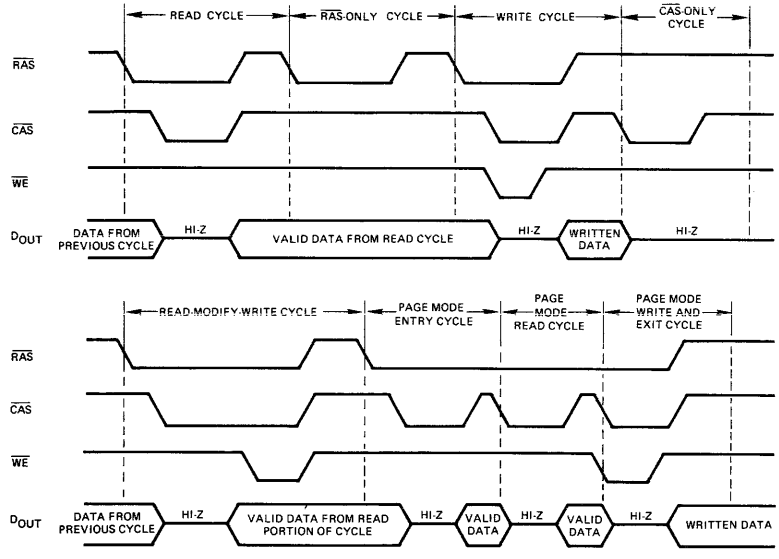


Figure 9. Operation of Data Output (D_{OUT})

Printed Circuit Board Trace Characteristics

Figure 11 shows the nominal lumped constant equivalent circuit of one-inch of 10 mil wide 2-ounce copper trace on a typical double sided printed circuit board with traces on both surfaces. The effect of the series resistance R_S is very small when compared to the series inductance L_S and can be ignored in practice. The series resistance is also non-reactive and its impedance is not frequency dependent. The following discussions will, therefore, not consider the minimal effects of R_S.

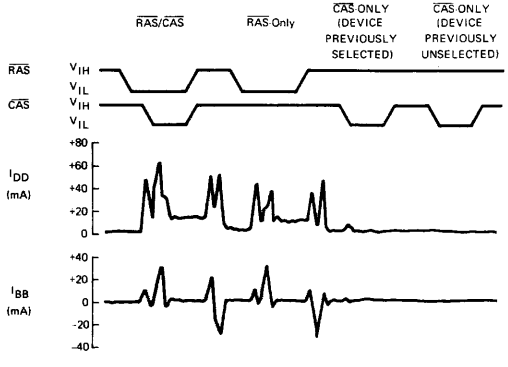


Figure 10. Typical Supply Current Waveforms

Decoupling Capacitor Characteristics

Capacitors used to decouple noise are not ideal devices and, therefore, exhibit inductive and resistive effects. Figure 12 shows the lumped constant equivalent circuit of a capacitor. The shunt resistance R_{SH} is a very high value (>10 MΩ) in capacitors of modern design and has minimal effects on the capacitor function. Therefore, the effect of R_{SH} will not be considered in the analysis of the decoupling capabilities of the capacitor.

The series inductance L_S in small disc ceramic and monolithic ceramic capacitors consists of lead inductance and is approximately 10nH/inch.

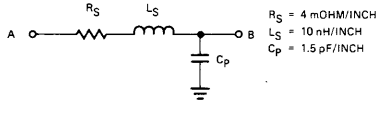


Figure 11. Lumped Constant Trace Equivalent Circuit

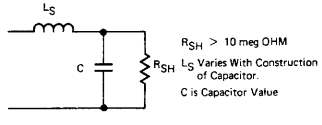


Figure 12. Lumped Constant Capacitor Equivalent Circuit

The series inductance in bulk capacitors such as tantalum and aluminum electrolytics is much larger due to the construction of the capacitors. The internal series inductance of the electrolytic units varies widely with capacitance value, physical size, and construction type and is generally much greater than the lead inductance. For this reason, the effectiveness of electrolytic type capacitors as decoupling components for noise frequencies above 10 MHz is minimal. Their use in the power distribution/decoupling network is to provide a bulk power storage element located on the memory array board. This placement eliminates the inductive effects of the system backplane wiring on the power distribution to the memory array board.

Power Distribution System Characteristics

Now that models for the printed circuit board traces and decoupling capacitors have been generated, various power distribution/decoupling schemes can be compared for effectiveness in minimizing power supply noise levels.

Figure 13 shows a V_{DD} decoupling technique often used with dynamic RAMs. Total lead length external to the 0.1μF decoupling capacitor is approximately 1-inch. Add to that the 0.5 inch internal lead length of a typical disc ceramic capacitor and the lead length in series with the capacitor is 1.5 inches. This equates to a series inductance of (1.5 inches) (10nH/inch) = 15 nH. The impedance of L_S as a function of frequency is shown in Figure 14. When a current pulse occurs, current is drawn from the capacitor through the series inductance L_S.

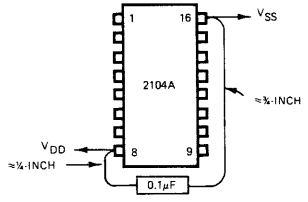


Figure 13. Commonly Used Capacitor Connection on V_{DD}

The impedance of the capacitor varies from 64 milliohms at 25 MHz to 16 milliohms at 100 MHz and is very small compared to the lead and trace impedance. Most of the impedance the current sees is in the inductance L_S and this is the impedance component of most concern to the system designer.

Fortunately, the energy spectrum of the current pulse is similar to that shown in Figure 15 which indicates that most of the energy is contained in the lower frequency components of the pulse.

Let's use Figures 14 and 15 as a hypothetical example and calculate the approximate noise generated by the leading edge of a 60 milliampere current pulse with a fast rise time. For simplicity, only the hypothetical components at 25, 50, 75, and 100 MHz will be included in the calculations. Also, the supply voltage will be assumed to be constant so that the vertical axis of Figure 15 represents current, I, as a percentage of total.

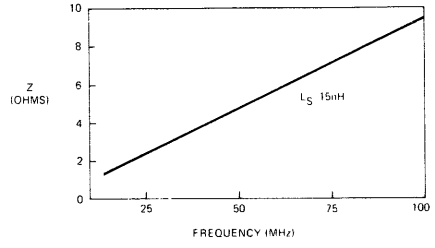


Figure 14. Impedance of L_S Versus Frequency

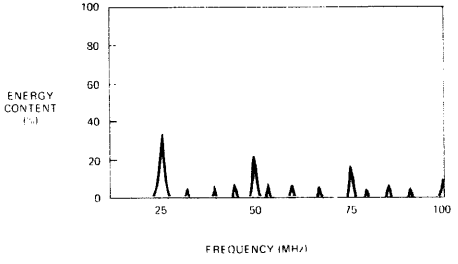


Figure 15. Hypothetical Energy Spectrum of Current Pulse

$$V_{noise} = (Z_{25})(I_{25}) + (Z_{50})(I_{50}) + (Z_{75})(I_{75}) + (Z_{100})(I_{100})$$
$$= (2.36)(35\times10^{-3}) + (4.71)(22\times10^{-3}) + (7.06)(15\times10^{-3}) + (9.4)(10\times10^{-3})$$
$$= 0.386 \text{ volts}$$

In other words, the voltage between the V_{DD} and V_{SS} pins on the memory device would drop by nearly 0.4 volt when the current pulse occurred. Considering all the current components would predictably increase this to 0.5 volt or more. Add to this the noise coupled into this LC circuit from the other similar circuits in the memory array and it becomes apparent that this memory device may see V_{DD} noise levels approaching 1.0 volt. While the device may operate with that noise level, operational margins of the device may well be reduced. Every practical effort should be made by the designer to reduce the overall noise level to 0.5 volts peak-to-peak or less.

One way this can be accomplished is by simply reducing the inductance in the circuit. Figure 16 shows a way to reduce the inductance. The equivalent inductance of the two traces from pin 16 to the capacitor is the parallel combination of the two paths since:

$$L_p = \frac{L_1 L_2}{L_1 + L_2} = \frac{(10nH)(10nH)}{20nH} = 5nH$$

Add that to the inductance of the capacitor lead length and the 0.25 inch trace from the capacitor to pin 8 of the device. The total inductance is then:

$L_S = 5nH + (0.75\ inch)(10nH/inch)$
$= 12.5nH$

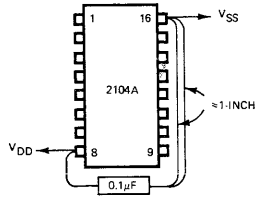


Figure 16. Reduction of Inductance by Paralleling Traces

The impedance of this inductance at 25 MHz and 100 MHz is 2.0-ohms and 7.8-ohms respectively. This compares to 2.4-ohms and 9.4-ohms for the original circuit at those frequencies and is a reduction in impedance of almost 17%.

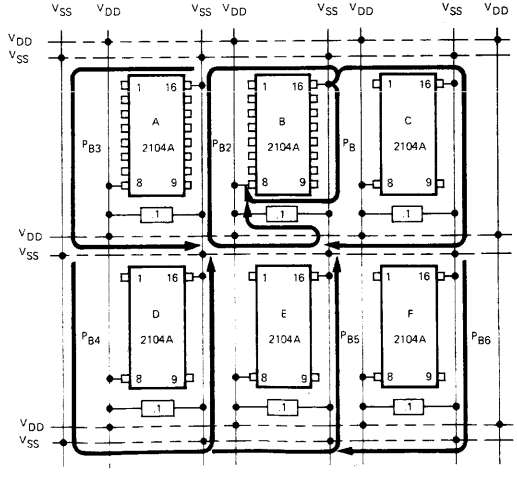


Figure 17. Gridded V_{DD} and V_{SS}

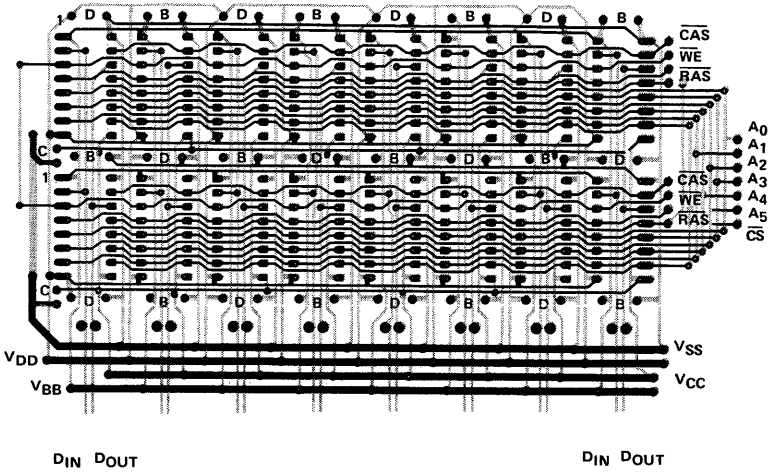
Additional reductions can be achieved by addition of more parallel traces or wider, lower inductance traces. Neither of these approaches is really practical, however, since board space is generally at a premium. A more practical, equally effective method of inductance reduction is the use of "gridded" power distribution. This involves bussing each power supply distribution network both horizontally and vertically on the circuit board. An example of this type of distribution for V_{DD} and V_{SS} is shown in Figure 17 for a matrix of six devices on a double sided printed circuit board. Consider the path of the current drawn by device B in Figure 17.

As indicated, in addition to the primary path P_B, there are no less than six other secondary, parallel paths (P_{B1} through P_{B6}) due to the gridding of the V_{SS} supply distribution system. Each of these secondary paths or traces is in parallel with the primary trace reducing the equivalent inductance of the current path between pin 16 and pin 8 of device B. Similar parallel paths exist for all the devices in the matrix.

Use of such a gridded power distribution network is recommended for all dynamic RAM systems due to the characteristics of the device current waveforms. Experience has shown the gridded distribution system to equal the performance of the more expensive multi-layer printed circuit board with internal power layers.

Additional power supply distribution traces may be added to the layout example of Figure 17 with only slightly greater side-to-side and end-to-end spacing between adjacent devices. It is recommended that V_{DD}, V_{BB}, and V_{SS} distribution systems be gridded. Figure 18 shows a recommended double-sided layout for 16-pin 4K and 16K RAMs. V_{CC} may be gridded but it is generally sufficient to distribute V_{CC} in one direction only since the 2104A itself does not draw power from the V_{CC} supply but only uses it to supply input levels to the peripheral TTL devices connected to the D_{OUT} pin (refer to the Device Circuit Operation Section).

Alternate power distribution layout techniques may be used with dynamic RAMs and some will show comparable results to the gridded system depending on memory array size, the number and placement of the decoupling capacitors, and the number of memory devices which are active in any given cycle. The gridded system has been proven in many production systems, however, and its use will result in predictable, workable power supply noise characteritistics. One commonly used distribution system is illustrated in Figure 19. This technique should definitely not be considered for use with dynamic RAMs simply due to the length of the current path between the V_{DD} and V_{SS} pins of any device in the matrix. As an example, device B



DECOUPLING CAPACITORS
D = 0.1 μF to V_{DD} TO V_{SS}
B = 0.1 μF V_{BB} TO V_{SS}
C = 0.01 μF V_{CC} TO V_{SS}

Figure 18. Recommended Two-Sided Board Layout for 2104A

in Figure 19 has an unnecessarily long and, therefore, high inductance current path between its V_{DD} and V_{SS} pins. Compounding the problem, it shares most of that current path with device C and all of it with device A. The magnitude of the noise between the V_{DD} and V_{SS} pins of device B is greatly dependent upon the noise generated by the other adjacent devices. This sytem is unacceptable at best and is to be avoided. Unfortunately, this is the power distribution scheme found on many of the "prototyping" printed circuit boards available on the market. Examine your prototyping boards carefully and avoid the use of this type for the memory array or add wiring to the board to grid the supplies.

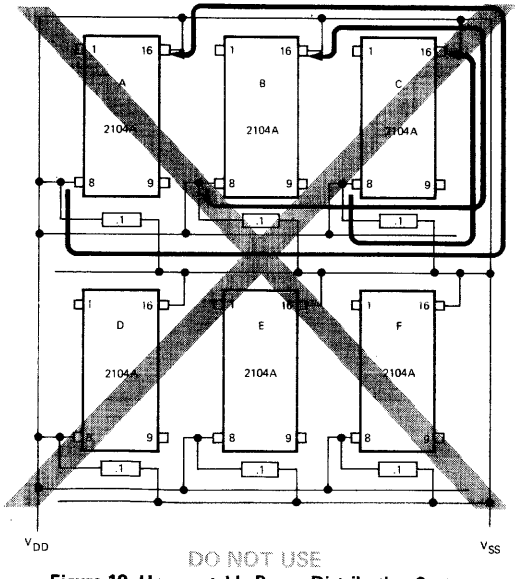


Figure 19. Unacceptable Power Distribution System

Recommended Decoupling Values

The decoupling capacitors used in the memory array should be types which exhibit good high frequency characteristics as discussed earlier. It is recommended that a 0.1μF ceramic capacitor be connected between V_{DD} and V_{SS} at every other device in the memory array. It is also recommended that a 0.1μF ceramic capacitor be connected between V_{BB} and V_{SS} at every other device in the array, preferably the alternate devices to the V_{DD} decoupling. Smaller capacitor values such as 0.01μF may be substituted but noise levels will increase with any given distribution scheme due to the higher capacitive impedance. Empirical comparative data should be taken and decoupling efficiency considered with the distribution system being used before the smaller capacitors are used. The small

cost difference between 0.1μF and 0.01μF capacitors may be negated by degradation of system noise margins.

A 0.01μF ceramic capacitor is recommended between V_{CC} and V_{SS} for approximately each eight devices in the memory array to prevent noise coupled to the V_{CC} line in the memory array from affecting the peripheral TTL logic in the system.

In addition to the ceramic capacitors in the memory array, it is recommended that a 10μF tantalum or equivalent capacitor be connected between V_{DD} and V_{SS} adjacent to the array for each 16 memory devices in the array. An equal or slightly smaller value bulk capacitor is also recommended between V_{BB} and V_{SS} for each 32 memory devices on the array. These bulk capacitors eliminate the inductive and resistive effects of the memory system backplane wiring connecting the memory array boards to the system power supplies.

I_{BB} Characteristics

The high performance of the 2104A results from advanced design and processing techniques developed by Intel. These techniques yield slightly different characteristics in the I_{BB} parameter than with the previous Intel 4K Dynamic RAMs. These changes have little effect on the V_{BB} power supply requirements of a typical system but they do require that I_{BB} be specified in a different manner and for this reason, I_{BB} will be discussed here in detail for clarification.

In a typical MOSFET integrated circuit the current from the V_{BB} (substrate) supply when the device is turned off is essentially the leakage from the source and drain diffusions into the substrate. This leakage current is in the nanoampere range for each individual MOS transistor but when multiplied by the 6000 or so transistors in a typical 4K RAM, the total leakage is typically 50 to 60 microamperes. When the device turns on and current is conducted between the drain and source, charge carriers flow between the drain and source through the gate voltage induced channel between the two terminals. As the carriers move through the region of high electric field close to the drain, they generate additional carriers by impact ionization. Most of these carriers join the initial carriers and move between the source and drain terminals due to the influence of the electric field created by the potential difference between the source and gate terminals. Some of these carriers however, are accelerated through the boundaries of the channel into the substrate and add to the leakage currents from the drain and source diffusions. This increases the I_{BB} current slightly during the time the device is operational. The number of these additional carriers is relatively low in typical 4K RAM and results only in a 15 to 20 μA increase in I_{BB} during the time the device clocks ($\overline{RAS}$ and $\overline{CAS}$) are active. This is because the energy, i.e. speed, of the carriers in the channel is not high enough to generate many additional carriers via impact ionization. The 2104 I_{BB} specification was 100μA maximum.

In the 2104A, shallow diffusions are used for the source and drain and thin gate oxide is used for speed/performance reasons. This results in much higher energy, i.e., faster, carriers in the channel due to the high electric field in the channel. These higher energy carriers are capable of generating more carriers than in previous 4K RAMs. The increase in I_{BB} during this action is significant, typically 100μA or more. Importantly, however, this increase is only during the time the clocks are active.

As a result of this difference in I_{BB} during inactive (standby) and active conditions of the clock, the 2104A has two I_{BB} specifications. I_{BB1} is the I_{BB} current during standby and I_{BB2} is the I_{BB} current during a memory device cycle. Interestingly enough, the standby I_{BB} current for the 2104A is lower than for the earlier 2104 due mostly to processing and design improvements. Due to these same improvements, however, the operating I_{BB} specification, I_{BB2}, is typically 160μA (400μA maximum).

What does this higher I_{BB} during operation mean in a typical 16K by 8-bit system? Assuming a 50% duty cycle due to data and refresh cycles and a cycle time of 500nsec, the average I_{BB} per device during any 2 msec refresh period will be:

$$I_{BBavg} = \frac{(I_{BB2_{max}})\,(1\text{msec})}{2\text{msec}} + \frac{(I_{BB1_{max}})\,(1\text{msec})}{2\text{msec}} = 225\mu\text{A max}$$

and typically:

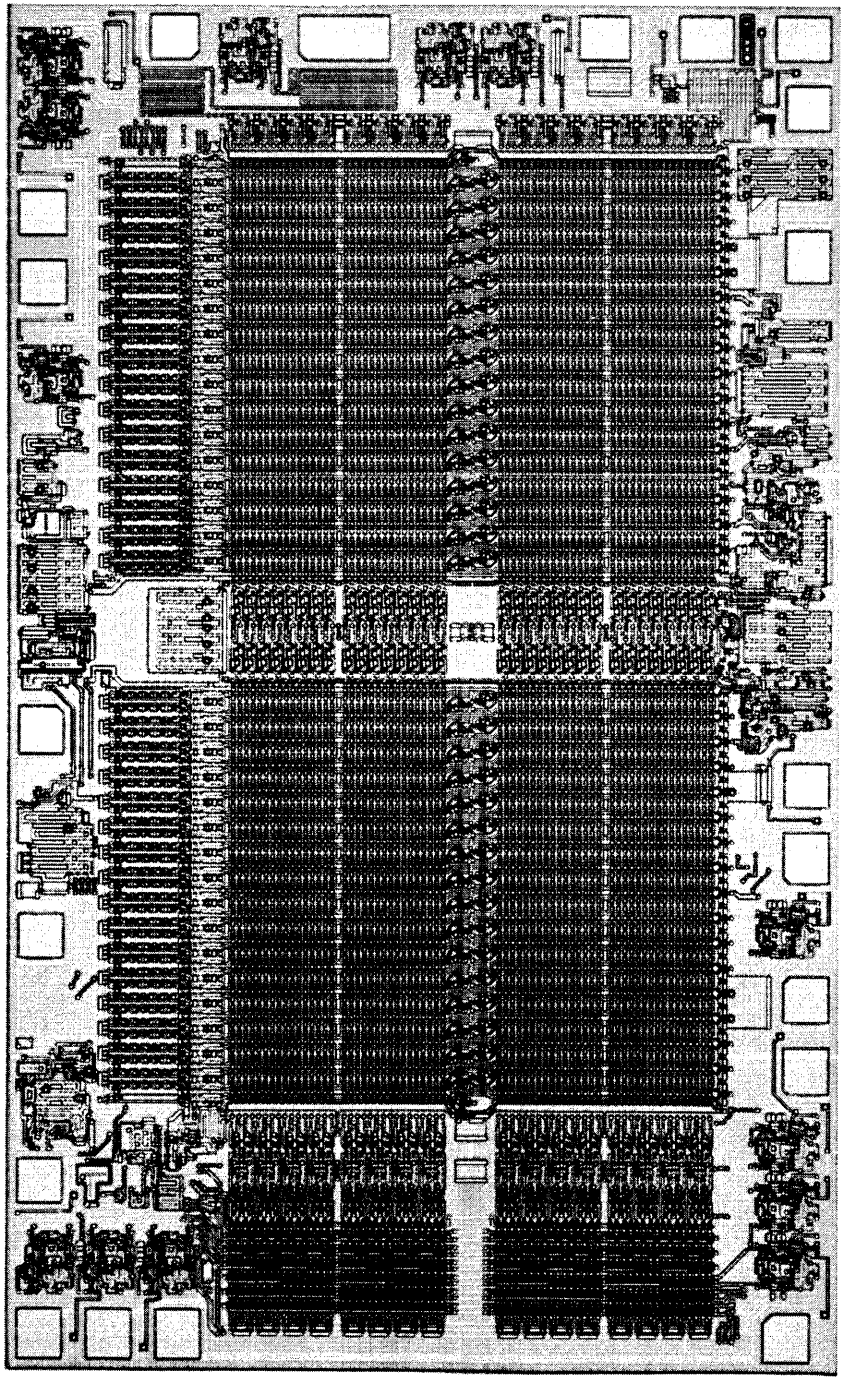
$$I_{BBavg(typ)} = \frac{(160\times10^{-6})\,(1\times10^{-3})}{2\times10^{-3}} + \frac{(5\times10^{-6})\,(1\times10^{-3})}{2\times10^{-3}} = 83\mu\text{A typ.}$$

Variations in duty cycle will decrease or increase these values but most systems will experience I_{BB} values not much different than with other 16-pin 4K RAMs. In the 16K X 8-bit system example, the total I_{BBavg} will be no greater than 7.2 milliamperes.

Memory System Design with the Intel® 2107B 4K RAM

Jim Oliphant
Application Engineering

Contents



Photomicrograph of the 4096 Word x 1 bit 2107B Dynamic RAM

INTRODUCTION

The Intel® 2107B is a 4096 word by 1 bit dynamic random access memory. The 2107B is fabricated using Intel's standard reliability proven n-channel silicon gate MOS technology. The device is packaged in a standard 22-pin DIP. The pin configuration and logic symbol are shown in Figure 1. Note that the 2107B can be used as a replacement for the 2107A.

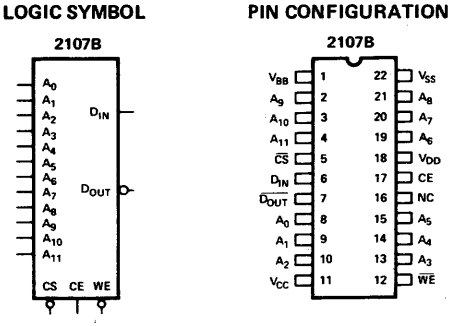


Figure 1. 2107B Logic Symbol and Pin Configuration

The combination of Intel's® n-channel silicon gate process and circuit design has resulted in a part that is very fast, easy to use, and economically produced in large volume. In addition, the combination of process and device design has resulted in a very small device (see Figure 2) using conservative layout rules (same as 2102A). The small size offers advantages in both large volume production and increased reliability. The 2107B operates with three power supplies relative to ground; V_{DD} (+12V), V_{BB} (−5V), and V_{CC} (+5V). The V_{CC} (+5V) supply is connected only to the output buffer of the 2107B and may be turned off during power down operations.

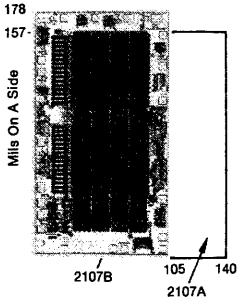


Figure 2. 2107B Comparative Die Size

The 2107B has one MOS level clock (Chip Enable) with all other inputs being low level TTL compatible (+2.4V V_{IH} minimum). The output is capable of driving 1 TTL load.

The purpose of this chapter is to describe the internal operation of the 2107B, outline those areas in system implementation to which the designer should pay particular attention and to discuss typical examples of the uses of the 2107B in systems environment. The chapter is arranged so that each of the above sections can be read independently of each other without having to go through any unwanted detail in the other sections.

INTERNAL DEVICE OPERATION

Internal operation of the 2107B is most easily understood with the aid of the block diagram shown in Figure 3. As is shown in this figure, the memory array is arranged in a 64 row X 64 column matrix of storage cells. The storage cells are implemented with a single transistor and a "storage" capacitor and are called single transistor cells. The operation of the storage cell will be discussed later. The memory cell is accessed by the coincidence of a row select (defined by addresses A_0–A_5) and a column select (defined by addresses A_6–A_{11}) signal at the desired address. An on chip timing and control generator provides for the internal timing signals for decoding, read/write strobing, data gating and output gating. All of the timing circuits in the 2107B are activated by the positive-going edge of chip enable.

Chip select controls the data I/O gating circuits internal to the 2107B. When chip select is high the output data buffer is in a high impedance state and

BLOCK DIAGRAM

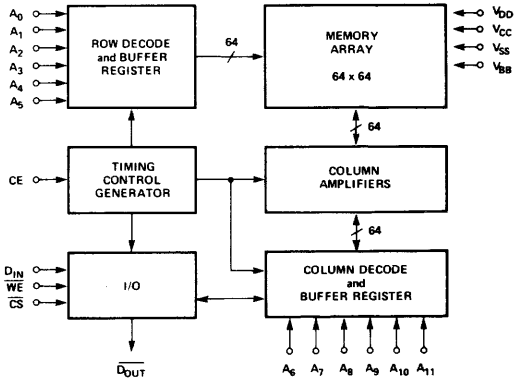


Figure 3. 2107B Block Diagram

the data-in buffer is electrically isolated from the data-in input pin. Since chip select controls only the internal data buffers and not the timing generators or address buffers internal to the 2107B, it is possible to refresh the 2107B with chip select high by initiating a read/refresh or write cycle.

The address buffer registers consist of latches activated at the leading edge of chip enable. Since the addresses are latched shortly after chip enable goes high, it is permissible to change the address long before the memory cycle is completed to set up for the next cycle.

The write enable input activates the data-in buffer gating data to the selected memory cell. Input data must be valid at the time write enable goes low to assure that the proper data is written into memory.

Circuit implementation and operation of each of the major input/output and storage portions are discussed below.

Storage Cell Operation

The storage cell used in the 2107B is implemented with a single transistor and storage capacitor as shown in Figure 4. From this figure it is shown that a charge on a storage cell is gated to the bit sense line by the MOS device connected to the column select line. (Note that for a given column select, 64 storage devices are gated to the respective 64 bit sense lines.)

Consider first a read operation and the case where the storage capacitor C_{STG} is discharged; i.e., node (1) is at V_{SS} (GND). Prior to chip enable going high, the bit sense lines have been precharged to V' by device Q_1. [V' is a voltage between V_{DD} (+12V) and V_{SS}.] After the address decoders have stabilized, the proper column select line is brought high, turning on device Q_2. The storage capacitor is then electrically connected to the bit sense line. At this time the charge on $C_{I/O}$ (proportional to the precharge voltage V') is redistributed between $C_{I/O}$ (parasitic capacitance of bit sense line) and C_{STG}. Since C_{STG} was initially discharged (node 1 at V_{SS}) the voltage will distribute between $C_{I/O}$ and C_{STG} according to the following relationship:

$$V_{BIT\ SENSE}(t_1) = V_{BIT\ SENSE}(t_0)\left(\frac{C_{I/O}}{C_{I/O} + C_{STG}}\right)$$

Since $C_{I/O}$ is very much larger than C_{STG} the change in the voltage on the bit sense line will be very small. The sense amplifier (S/A) is designed to detect very small changes in bit sense line voltage and to latch in a state near V_{SS} (GND) or V_{DD} (+12V), depending on the state of the storage cell.

Sensing an initial charge on C_{STG} (proportional to V_X where $V_X = V_{DD} - V_{TH}$, V_{TH} is the effective MOS threshold) is identical to the sequence described above. The only difference is that now the bit sense line is driven above the initial V' precharge voltage. Again the sense amplifier detects the small change in bit sense line voltage and latches in the appropriate state.

Note that during a read operation of the storage cell, the original charge (data) on the storage cell is changed (i.e., the read operation is effectively a destructive read). Data is rewritten back on the storage capacitor C_{STG} by the sense amplifier after it has latched in the proper state. For example, if C_{STG} was initially charged to V_X (~10V), the sense amplifier will latch the bit sense line to V_X and, since the column select line is on (high), the original data is automatically rewritten into C_{STG}. The entire operation is transparent to the user.

A plot of the voltage on the bit sense line for the two cases described above is shown in Figure 5.

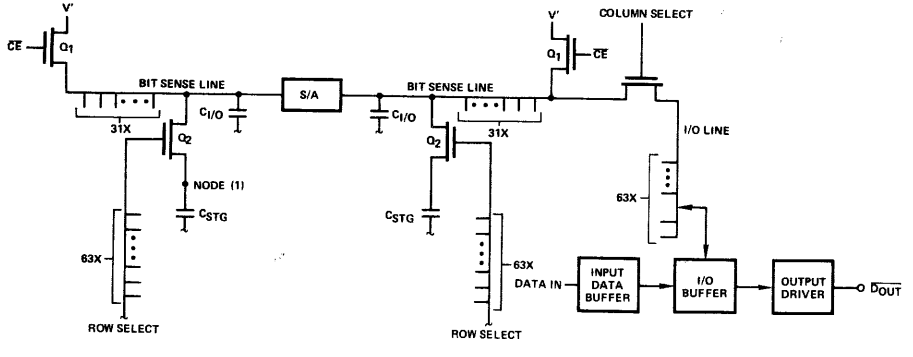


Figure 4. 2107B Memory Cell and Associated I/O Circuitry

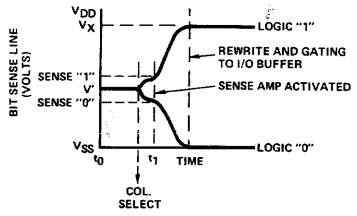


Figure 5. Bit Sense Line Voltage

A write operation is identical to the rewrite portion of a read cycle. In this case, however, the incoming data "overrides" the state of the sense amplifier (if different from the desired state) and writes into the selected cell. It is important to remember that the data-output at the output pin is the logical inverse of the data written into memory.

Data Sense/Latch

As discussed previously, a sense amplifier on the bit sense line is necessary to detect the low level data signals generated on the bit sense line during a read cycle. A simplified circuit schematic used for the sense amplifier is shown in Figure 6.

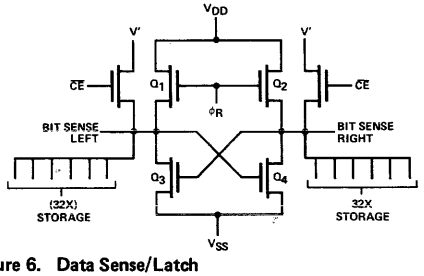


Figure 6. Data Sense/Latch

Before chip enable is brought high, both sides of the bit sense lines are precharged to V' (as discussed previously). At the proper time (after all data transients have subsided) devices Q_1 and Q_2 are turned on by ϕ_R going positive. At this time, the state of bit sense left is compared with bit sense right causing the latch to lock in the appropriate state. For example, if the right bit sense line is at a higher potential than the left bit sense line, device Q_3 will begin to conduct. The cross coupled latch will then fully switch with bit sense left going to V_{SS} and bit sense right to V_X.

Address Buffer/Latch

The address buffer/latch is shown in Figure 7. The input to the address buffer/latch is low voltage compatible which the circuit senses, translates to MOS level signals and latches.

Operation of the address buffers is as follows: During chip enable off time (CE low) both sides of the latch are precharged to V_X (~10V) by devices Q_1, Q_2, and Q_3. Device Q_3 is used to assure that the initial precharge on each side of the latch are equal.

When chip enable goes high, the input to the address buffer (A_{IN}) is gated to the cross coupled latch which latches the appropriate MOS level at A_I and $\overline{A_I}$. For example, if the TTL address input is high, then device Q_7 will turn on at ϕ_A time. The cross coupled latch then regenerates, turning Q_6 off. The quiescent state of the latch for this input is Q_6 off, Q_8 on, thereby setting A_I and $\overline{A_I}$ to MOS level high and low, respectively.

This type of latch is capable of triggering and latching at very high speeds which allows the addresses to be removed from the input as soon as possible. However, there are a few characteristics of this latch which have an effect when the device is placed in a system environment.

First note that node (1), Figure 7, has been precharged to a high MOS level of V_X (~10V). When

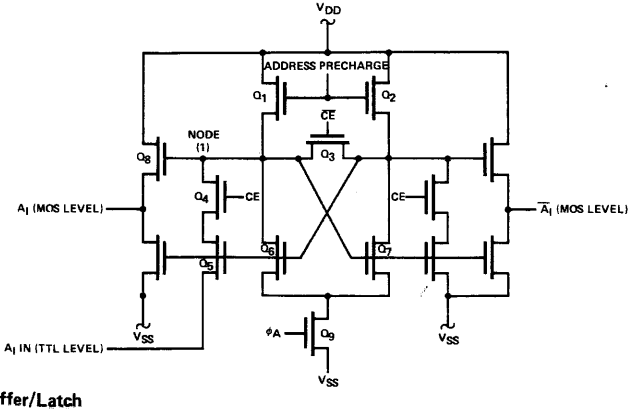


Figure 7. Address Buffer/Latch

chip enable goes high turning on Q_4, the charge on this node is connected to the address input node (A_{IN}) for a short period of time (until the latch switches). This results in a small positive voltage shift on the address input A_{IN}. It follows then that the more 2107B devices attached to a given address driver the larger the voltage excursion will be. This excursion has been found to cause no problem in any reasonable system environment (as described later) and amounts to no more than 9 mV positive shift for each 2107B. The amount of positive charge coupling depends upon the address driver and the address line impedance. As should be expected, the most sensitive address level is the low level (V_{IL}) since any positive coupling decreases the available noise margin.

Another characteristic to be aware of in this type address buffer is the input current drawn through the address driver when an address goes from a low state to a high state during chip enable high. This condition results from the latch being set in the state where Q_6 is on as well as Q_4 and Q_5. Current is then drawn through devices Q_4, Q_5, Q_6 and Q_9. This current is typically in the order of 0.5 mA. Note that although this may cause a load on the address driver and cause it to drop below 2.4V, there is no effect on the memory component since the desired address has been latched in. This current is drawn only as long as chip enable is high. When chip enable goes low, device Q_4 is turned off, opening the current path. This effect will be shown on various type drivers in a later section (Low Voltage Buffer/Drivers).

Output Driver

A schematic of the output buffer is shown in Figure 8. Note that the output is in a high impedance state if either chip select is high or chip enable is low. Further, the V_{CC} shown in Figure 8 is the only connection the V_{CC} makes on the 2107B. This allows V_{CC} to have a wide range of values (up to V_{DD}) if types of sensing other than TTL is desired.

2107B Bit Map

Figure 9 gives the location of each cell in the memory matrix for each address. As shown in this figure, the addresses run sequentially starting from the lower left corner (device oriented as shown).

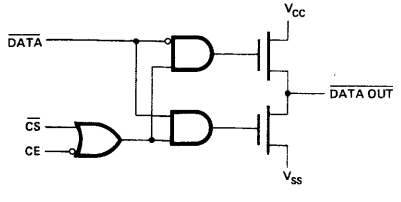


Figure 8. 2107B Output Driver

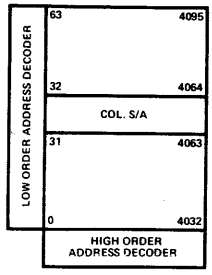


Figure 9. 2107B Bit Map

2107B SPECIFICATION

Although the device specifications for the 2107B are concise and self explanatory, some sections are included here to emphasize those areas of most interest to the designer. Consider first the DC and operating characteristics shown in Table I marked with a [5].

The V_{DD} supply current during chip enable off is specified at 200 μa maximum with chip enable no higher than 0.6V. It is important to hold the low level of chip enable at or below this value (to a maximum of −1.0V) to assure that devices internal to the 2107B do not turn partially on. Note that considering only the AC operating environment, chip enable can go as high as 1.0V above V_{SS} and the device will still operate properly. This requirement on chip enable off is most important in those systems being placed in a low power refresh only standby mode.

The V_{BB} supply current load (I_{BB}) is maximum at 100 μa and includes all leakages. It is not necessary to add the other leakage currents (e.g., I_{LI}, I_{LC}) to I_{BB} to calculate supply drain on V_{BB}.

The input low voltage (for low level signals) V_{IL}, is specified as a function of the chip enable rise time and is referenced to a transition with t_T = 20 nsec. It is recognized that in some system applications, the load on the chip enable driver may result in transitions of 30 nsec or higher (to a maximum of 40 nsec). If the chip enable transition in the system is not 20 nsec or faster (to a minimum of 10 nsec), then the typical low level for the low level drivers is shown by the graph in Figure 10. It is important to include any noise which may be on the address line during t_{AH} (address hold) time. An example of the noise expected on an address line when chip enable goes high (during refresh) is shown in Figure 11. The noise shown here is the result of 36 devices attempting to raise the address driver (see Address Buffer/Latch) level during refresh time. Refresh

Table I. D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±10%, V_{BB} [1] = −5V ±5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$ CE = V_{ILC} or V_{IHC}
I_{LC}	Input Load Current		.01	2	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
I_{DD1} [5]	V_{DD} Supply Current during CE off[3]		110	200	μA	CE = −1V to +.6V
I_{DD2}	V_{DD} Supply Current during CE on			60	mA	CE = V_{IHC}, $\overline{CS}$ = V_{IL}
$I_{DD\ AV}$ [5]	Average V_{DD} Current		38	54	mA	Cycle time=400ns, t_{CE}=230ns $\overline{CS}$=V_{IL}; T_A=25°C
I_{CC1} [4]	V_{CC} Supply Current during CE off		.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
I_{BB} [5]	V_{BB} Supply Current		5	100	μA	
V_{IL} [5]	Input Low Voltage	-1.0		0.6	V	t_T = 20ns — See Figure 10
V_{IH}	Input High Voltage	2.4		V_{CC}+1	V	t_T = 20ns
V_{ILC}	CE Input Low Voltage	-1.0		+1.0	V	
V_{IHC} [5]	CE Input High Voltage	V_{DD}-1		V_{DD}+1	V	
V_{OL}	Output Low Voltage	0.0		0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = −2.0mA

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.3V more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. During CE on V_{CC} supply current is dependent on output loading, V_{CC} is connected to output buffer only.
5. See discussion — 2107B specifications.

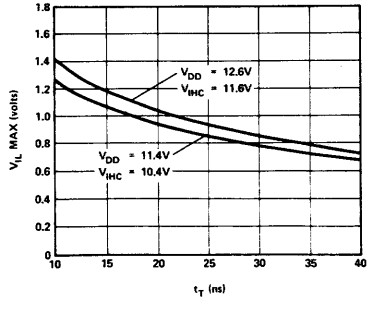


Figure 10. V_{IL} vs CE Rise Time

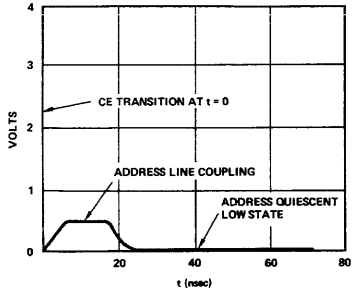


Figure 11. Coupling to Address Line Caused by Chip Enable Transition

is the worst case since all chip enable signals will be simultaneously decoded and driven at the same time.

The chip enable high voltage, V_{IHC}, can vary between V_{DD}+1.0 and V_{DD}−1.0 volts. This allows maximum flexibility in the driver design and provides for adequate noise margins.

The average V_{DD} current ($I_{DD\,AV}$) during a read/write cycle is specified to be a maximum of 54ma. This current is a function of both cycle time and temperature as shown in Figures 12 and 13, respectively. As shown by these curves, the maximum power occurs at low temperature and maximum duty cycle.

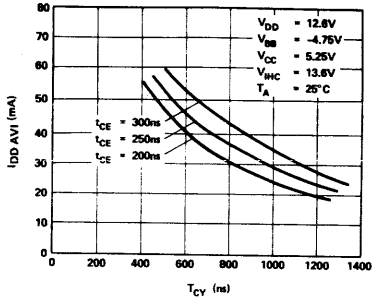


Figure 12. $I_{DD\,AV}$ vs Cycle Time

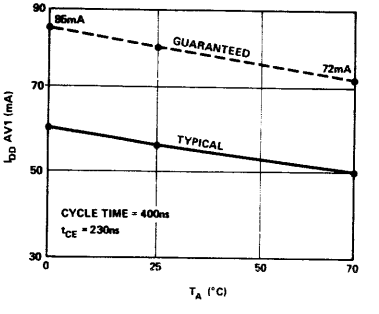


Figure 13. $I_{DD\,AV}$ vs Temperature

Timing

The timing relationship between the control, addresses, and data in/out is very straightforward as shown in the specification. For reference, the Read/Refresh, Write and Read-Modify-Write cycles are shown in Figures 14, 15, and 16, respectively, for minimum timing. Selected points are discussed which may cause the most problems if they are violated in a system environment.

For all cycles it is imperative to make certain that the address inputs are valid at or before chip enable reaches the V_{SS}+2.0V level (t_{AC}). The high speed of the 2107B address buffer/latches means that if the address inputs are not valid until just after chip enable goes high, the wrong address is likely to be latched in the chip. Likewise, the input data must not change after write enable goes low while chip enable is high (t_{DW}). Again, violation of this requirement may result in incorrect data being written into memory.

Note that for all cycles, the data-out output goes to a low state shortly after chip enable goes high. This prohibits the output from being tied directly to a clear or preset input of a latch.

Problems can occur when one or more parts of these specifications are violated.

Transient Currents

Although the transient currents in the 2107B are easily handled, proper attention should be paid to the peak values and adequate decoupling provided to handle the expected transients. Figure 17 shows the transient currents present in the 2107B.

Consider first the transient current supplied by the chip enable driver I_{CE}. It is noted that this current does not have a resistive component but is strictly a charging current represented by the relationship:

$$I = C\left(\frac{dv}{dt}\right)$$

As expected, the largest transient current drawn by the 2107B is the V_{DD} supply and is represented by I_{DD}. The first portion of this curve shown as A is the result of internal nodes charging up for operation. The section shown as B is the result of the address buffers/decoders turning off. Portion C is the "steady state" current drawn by all internal circuits while chip enable is high.

Portion D of the transient current is the result of feedthrough capacitance (internal to the chip) coupling to V_{DD} when chip enable goes low. Portion E is the precharging of selected internal nodes by the chip enable generator (e.g., precharging bit sense line. See section on Internal Device Operation).

The transients associated with the V_{BB} supply I_{BB} should be reviewed closely. Note that the peak values are approximately 20 ma during a cycle with a time base as shown. Special attention is called to this because even though the *average* DC current is very small (maximum 100 μa) the peak currents can be two orders of magnitude higher.

(Numbers in parentheses are for minimum cycle timing in ns)

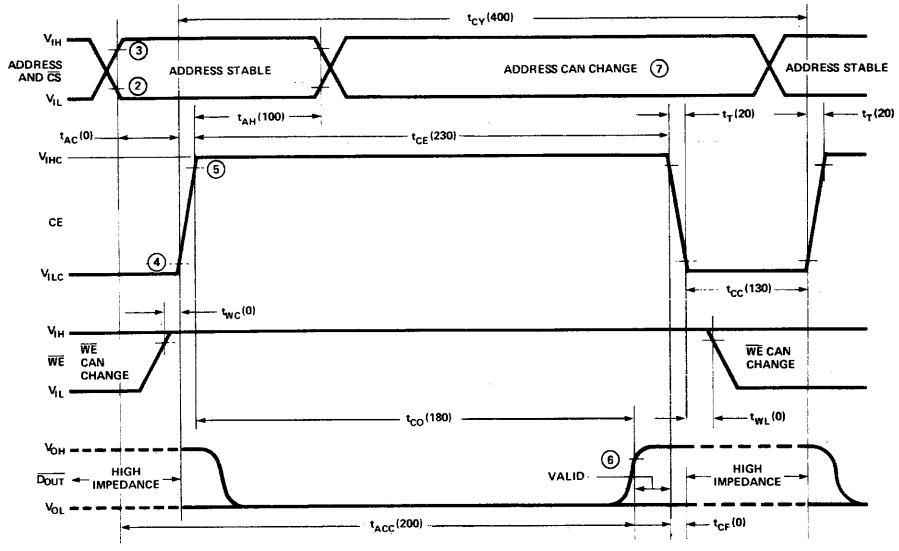


Figure 14. Read/Refresh Cycle[1]

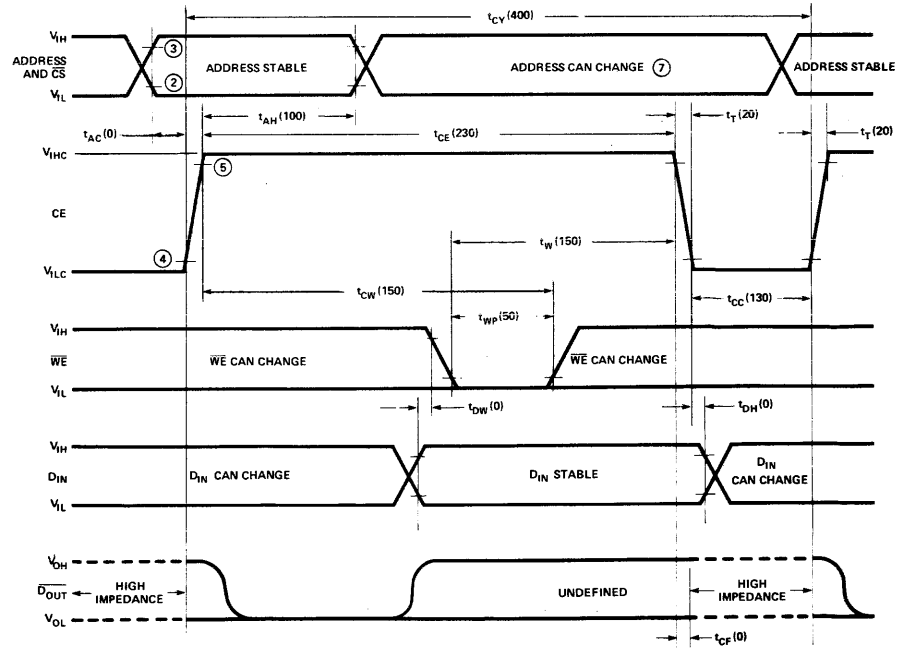
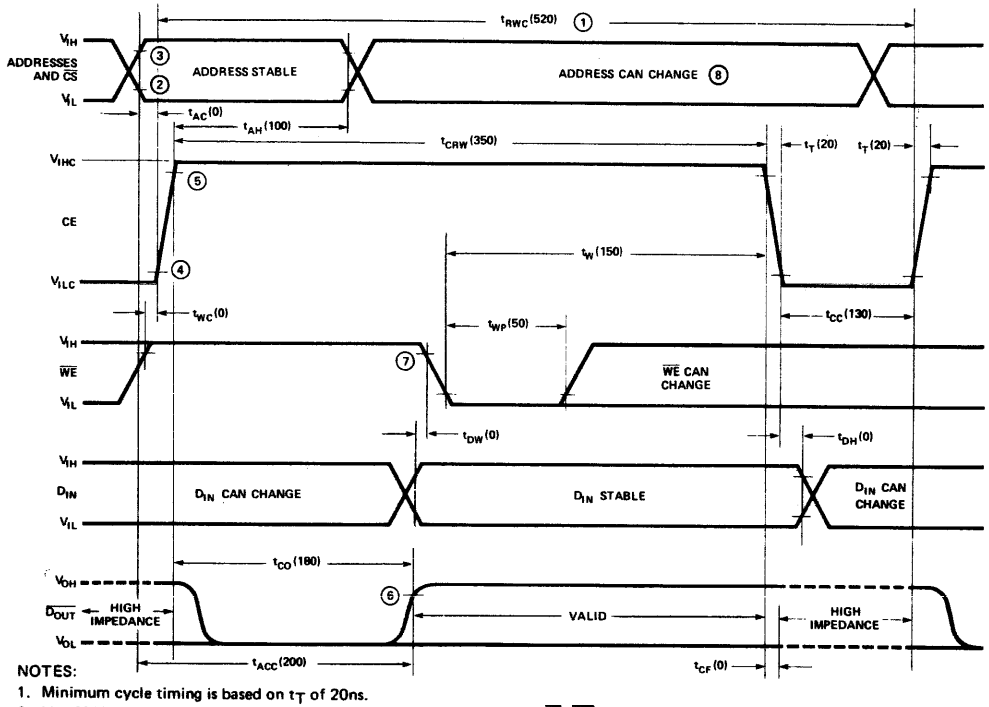


Figure 15. Write Cycle

NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

(Numbers in parentheses are for minimum cycle timing in ns.)



NOTES:

1. Minimum cycle timing is based on t_T of 20ns.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.
7. $\overline{WE}$ must be at V_{IH} until end of t_{CO}.
8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Figure 16. Read-Modify-Write Cycle

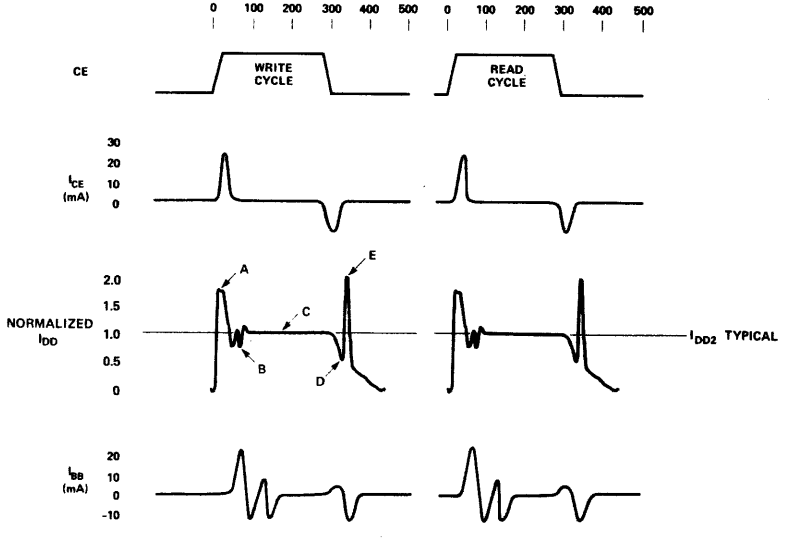


Figure 17. Typical Current Transients vs Time

These transients are characteristic of any dynamic RAM and are in part related to the density of the RAM. Again, if adequate decoupling measures are taken, very little noise will be generated on the V_{BB} system distribution.

Notice that the transient current for I_{CC1} is not shown. This is because the V_{CC} supply is connected only to the internal output device and its transient depends on the load placed on the output.

A full discussion on decoupling the power distribution in 2107B arrays appears in the decoupling section. As it is shown later, the use of a multi-layer memory board is not required by the 2107B.

SYSTEM CONSIDERATIONS

The previous sections of this application note have dealt with the characteristics of the 2107B as a stand-alone device. This section will outline the types of interface, system design considerations, power calculations and testing considerations when using the 2107B.

MOS Level Drivers

There are many types of drivers capable of driving n-channel RAMs such as the 2107B. The drivers can be used in one or more of the configurations as shown in Figure 18a, b, and c. Each of the driver types shown in Figure 18 has an optimum circuit load that it can drive and each has special design considerations. These drivers are catagorized in three general types; those which:

1. Require external drive transistors.
2. Require an additional power supply.
3. Require no special components or voltages.

In case (1) above, there is insufficient high level drive capability in the driver, hence a PNP external discrete transistor must be used to generate sufficient up-going transition (Figure 18a). Note that this transistor is driving in the saturated mode so the minimum high level criteria ($V_{DD}-1.0$) on the high level MOS clock are easily met.

Driver type (2), shown in Figure 18b, does not require external discrete transistors but does require an additional power supply. This extra supply is usually 3V higher than the V_{DD} supply for the RAM (e.g., using this type of driver with the 2107B would require V_{DD} = 12V and V_{DD1} = 15V). The additional supply is necessary to assure that the minimum up level ($V_{DD}-1.0$) requirement of the MOS clock is met.

The 3245, shown in Figure 18c, has been designed to maintain the $V_{IH\ MIN}$ requirements of the 2107B, while some other types of drivers using a single V_{DD} supply may not maintain a sufficient $V_{IH\ MIN}$ level. The 3245 is recommended for all new designs using the 2107B.

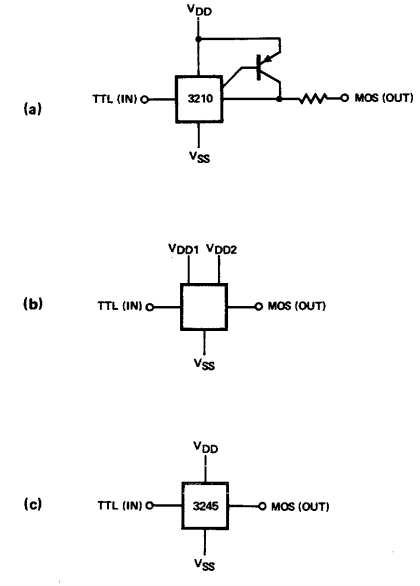


Figure 18. Three Types of MOS Level Drivers

It is important to remember to place the MOS level driver outputs physically as close as possible to the memory array. This will minimize any transmission line impedance mismatch between the unloaded stub and heavily loaded line in the memory array. The effect can most easily be seen with the aid of Figure 19. The impedance of the interconnect is:

1. $Z_{0(1)} = \sqrt{\frac{L}{C_1}}$

where C_1 is the capacitance per unit length of the interconnect

L is the inductance per unit length of the interconnect

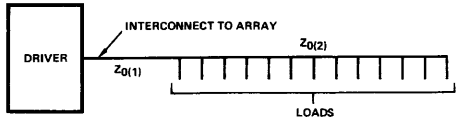


Figure 19. MOS Level Driver Loading

For all practical purposes, the inductance per unit length of the printed line is independent of the externally connected loads. Therefore, the impedance of the loaded section of transmission line can be represented as:

$$2.\quad Z_{0(2)} = \sqrt{\frac{L}{C_1 + C_2}}$$

where C_2 is the added capacitance per unit length to the printed transmission line.

For most practical systems, capacitance per unit length of an unloaded transmission line will be approximately 1–2 pF/in. (C_1). C_2 is the capacitance effect of the 2107B per unit length. Since the spacing between memory devices is approximately 0.5" the typical loading effect of C_2 is 30 pF/in. (i.e., 15 pF assumed for each chip enable input).

The ratio of the two impedances is calculated as follows:

$$\frac{Z_{0(1)}}{Z_{0(2)}} = \sqrt{\frac{C_1+C_2}{C_1}} = \sqrt{\frac{32}{2}} = 4$$

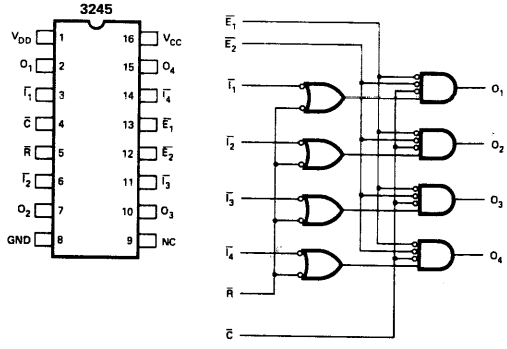
This means that the impedance of the stub is four times the impedance of the loaded section.

If the loads are placed close to the driver output the effect of the stub will be negligible and will cause no problem.

3245 MOS Level Driver

The Intel® 3245 is a quad MOS level driver, with each driver capable of driving 250 pF load with maximum delay of 30 nsec. The 3245 requires two power supplies; V_{CC} (+5V), and V_{DD} (+12V). The pin configuration and logic diagram of the 3245 is shown in Figure 20. For reference, input/output waveforms are shown in Figure 21, with delays given in Table II for worst case conditions.

Note that Table II gives the minimum input to output delay for a lightly loaded line (C = 150 pF) and the maximum delay plus rise time for a heavier load (C = 250 pF). The minimum delay time is given so the system designer can guarantee that the chip enable driven by a particular driver does not occur *before* the address lines have stabilized. The maximum delay plus rise time is given to guarantee



PIN NAMES

$\overline{I_1}$-$\overline{I_4}$	DATA INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{E_1}$, $\overline{E_2}$	ENABLE INPUTS	V_{CC}	+5V POWER SUPPLY
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
$\overline{C}$	CLOCK CONTROL INPUT		

Figure 20. 3245 Pin Configuration and Logic Diagram

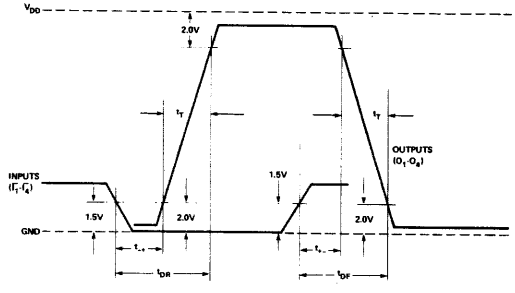


Figure 21. 3245 Input/Output Waveforms

Table II. 3245 A.C. Characteristics

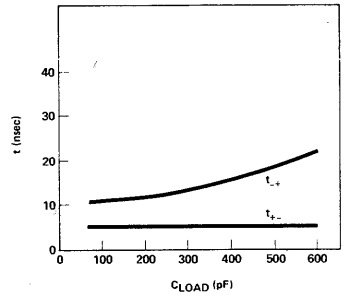
T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%

Symbol	Parameter	Min.[1]	Typ.[2]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	5	11		ns	R_{SERIES} = 0
t_{DR}	Delay Plus Rise Time		20	32	ns	R_{SERIES} = 0
t_{+-}	Input to Output Delay	3	7		ns	R_{SERIES} = 0
t_{DF}	Delay Plus Fall Time		18	32	ns	R_{SERIES} = 0
t_T	Output Transition Time	10	17	25	ns	R_{SERIES} = 20Ω
t_{DR}	Delay Plus Rise Time		27	38	ns	R_{SERIES} = 20Ω

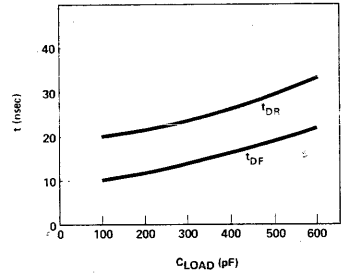
NOTES: 1. C_L = 150 pF 2. C_L = 200 pF & T_A = 25°C 3. C_L = 250 pF

a required system access or cycle time can be met. The capacitance values specified for the 3245 of C = 150 pF, C = 200 pF, and C = 250 pF are representative of the minimum, typical, and maximum capacitance, respectively, of nine 2107B Chip Enable inputs plus associated stray capacitance.

Graphs showing the effect of capacitance loads on delay and rise times are shown in Figure 22a and b.



(a) INPUT TO OUTPUT DELAY



(b) DELAY PLUS TRANSITION TIME

Figure 22. 3245 Delay and Transition Time as a Function of C_{LOAD}

The 3245 offers a great deal of flexibility in driving large arrays of 2107Bs. A sample of its logic capability is shown in Figure 23. A given card is selected by Card Enable i, byte control is maintained with Byte Enable, and the desired row selected by Row Enable i. The basic chip enable timing pulse is provided by CE timing.

At refresh time it is necessary to activate the Card Enable i, Byte Enable and Refresh Enable to refresh the entire card at one time. In most systems, it is desirable to refresh all cards simultaneously. If the cards are decoupled properly (see Decoupling section), the power supply transients during refresh will be minimal and are acceptable. The basic configuration of such a card is shown in Figure 24. For

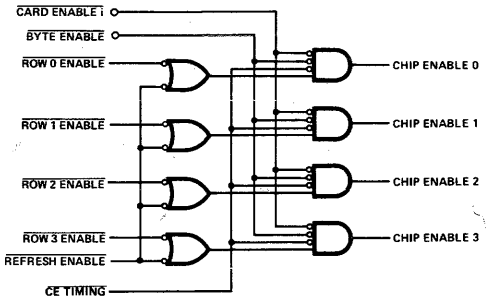


Figure 23. 3245 Enable Configuration

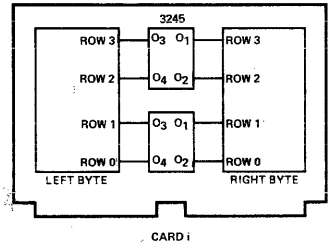


Figure 24. System Organization and Driver Placement

this system, the entire 16K X 16 memory array can be driven with two 3245s placed as shown between the two memory arrays.

Waveforms of the 3245 driver in a system similar to that shown in Figure 24 are given in Figure 25a–d. The driver configuration used is shown in Figure 26. Figure 25a and b shows the leading and trailing edge of chip enable at both the beginning and ending of the printed line for an added series resistance R of 10Ω. Note the transition time and overshoot for each of these edges. The overshoot is worst case at the leading edge at the driver end and on the trailing edge at the end of the line. The trailing edge overshoot is 2.2V while the leading edge overshoot is 1.5V. Both values are very marginal for system operation.

The effect of increasing the series resistance to 20Ω for the above driver is shown in Figure 25c and d. Note that the transition time has increased but is

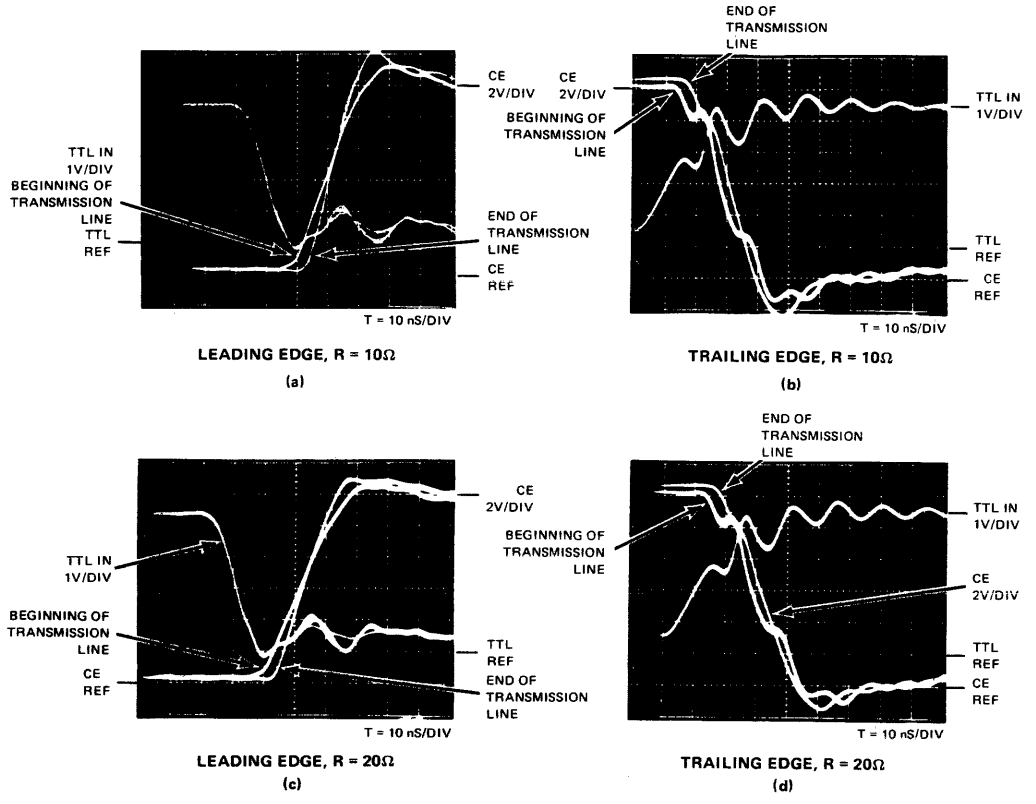


Figure 25. 3245 Typical Driver Waveforms

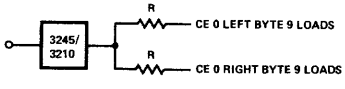


Figure 26. MOS Level Driver Configuration

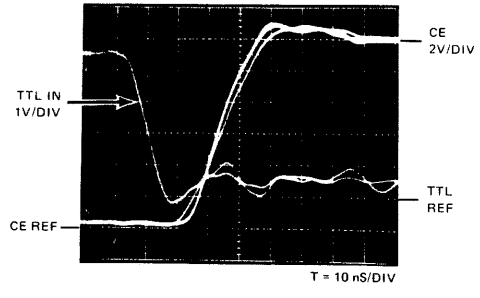


Figure 27. 3245 Driver Waveform with Temperature = 70°C

still within entirely acceptable limits and the overshoots have been cut in half. The driver is now operating in an acceptable mode with minimal overshoot.

The effect of temperatures on the 3245 is shown in Figure 27. A 20Ω series resistor is used with the driver.

The results of board measurements of a typical 3245 driver driving 18 loads and 9 loads is shown in Table III. Note that the delay does not change appreciably with temperature but the transition time increased approximately 2–3 nsec from 25°C to 70°C.

3210 MOS Level Driver

The pin configuration and logic symbol for the 3210 driver is shown in Figure 28. As shown in this figure, this driver consists of one MOS level driver and four TTL low voltage buffers. These low voltage buffers can be used to drive inputs which require a 3.5V high level (such as the 2107A address

Table III. Summary of 3245 Driver Board Delay Measurements

NUMBER 2107B LOADS AND CIRCUIT CONFIGURATION		MEASURED CONDITIONS INPUT TO OUTPUT DELAY				MEASURED DELAY[3] PLUS RISE		MEASURED DELAY[4] PLUS FALL	
		t_{-+}[1]		t_{+-}[2]					
		TYP.	WORST[5] CASE	TYP.	WORST[5] CASE	TYP.	WORST[5] CASE	TYP.	WORST[5] CASE
3245 18 LOADS[6]	R = 20Ω	12	12	10	10	34	37	33	35
3245 9 LOADS	R = 20Ω	11		10		30	33[7]	25	27[7]

NOTES:

1. TTL 1.5 to V_{SS} +1 volt
2. TTL 1.5 to V_{DD} −1 volt
3. TTL 1.5 to V_{DD} −1 volt
4. TTL 1.5 to V_{SS} +1 volt
5. Worst case driver on board at 70°C and 5% power supply variation.
6. 18 loads 20Ω split resistor (see Figure 26).
7. Projected from 18 load delay.

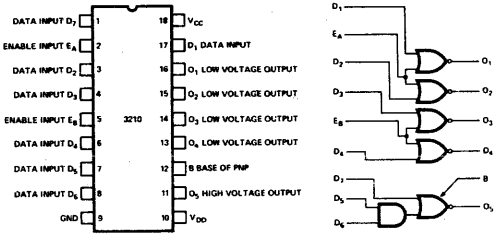


Figure 28. 3210 Pin Configuration and Logic Symbol

inputs) or they can be used to drive high capacitance loads with minimum delay. For reference, the input/output characteristics of the 3210 are shown in Figure 29 and table IV, respectively.

The driver configuration for the 3210 MOS level output is shown with the aid of photos in Figure 30a and b for series resistances of 10Ω and 20Ω. Table V summarizes the results of board measurements for the 3210 as a function of series resistance and temperature.

Low Voltage Driver/Buffers

The address, data-in, write enable, and chip select inputs on the 2107B are all low voltage TTL compatible requiring no special interface. This section will discuss the types of drivers which can be used to drive the low voltage inputs along with the advantages and disadvantages of the drivers.

The types of low level drivers capable of driving the 2107B are shown in Figure 31. Two observations are pointed out regarding the use of TTL drivers shown in Figure 31.

1. There are no pull up resistors.
2. Series 74S type gates are not recommended.

Table IV. 3210 A.C. Characteristics

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%

SYMBOL	PARAMETER	MIN.	TYP.[1]	MAX.	UNITS	TEST CONDITIONS
t_{LDR}	Delay Plus Rise Time for Low Voltage Drivers		17	25	nS	C_L = 200 pF
t_{LDP}	Delay Plus Fall Time for Low Voltage Drivers		16	25	nS	C_L = 200 pF
t_{H-+}	Input to Output Delay for High Voltage Driver	9	15		nS	C_L = 175 pF
t_{HDR}	Delay Plus Rise Time for High Voltage Driver		27	40	nS	C_L = 350 pF
t_{H+-}	Input to Output Delay for High Voltage Driver	4	8		nS	C_L = 175 pF
t_{HDF}	Delay Plus Fall Time for High Voltage Driver		18	30	nS	C_L = 350 pF
t_{DB}	Delay to Base Drive to External PNP (Pin 12)	4	8	17	nS	

NOTE: 1. T_A = 25°C

A.C. CONDITIONS OF TEST:

Input Pulse Amplitudes: 3.0V Input Pulse Rise and Fall Times: 5 nS between 1 volt and 2 volts Measurement Points: See Waveforms

RAMs

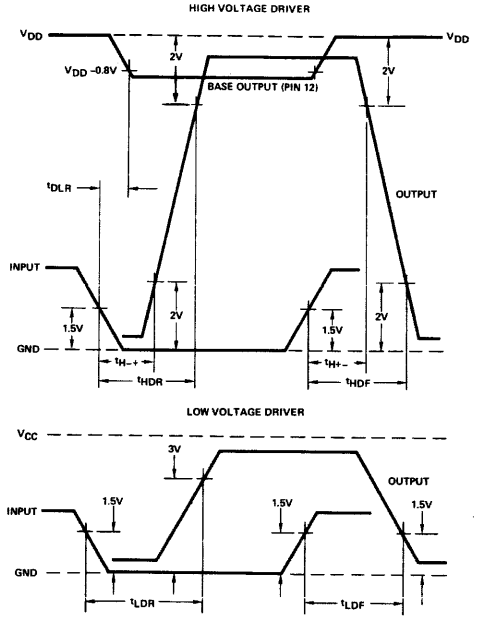


Figure 29. 3210 Input/Output Characteristics

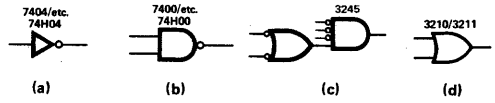


Figure 31. Low Level Drivers

TTL Drivers

Since TTL devices will typically pull up actively to 2.8V to 3.4V, which is well above the required minimum high level, pull up resistors are not needed. Standard Series 7400 type gates are specified to supply 400 μa up level current at 2.4V worst case. Since each address input of the 2107B has a maximum leakage current of 10 μa, this type of driver is capable of driving 40 2107B address lines. However, it should be noted that these 40 address inputs have a capacitance of 240 pF. This load will increase the delay through the series 74 gates.

When driving the 2107B address inputs with TTL gates it is advisable to use a NAND type circuit

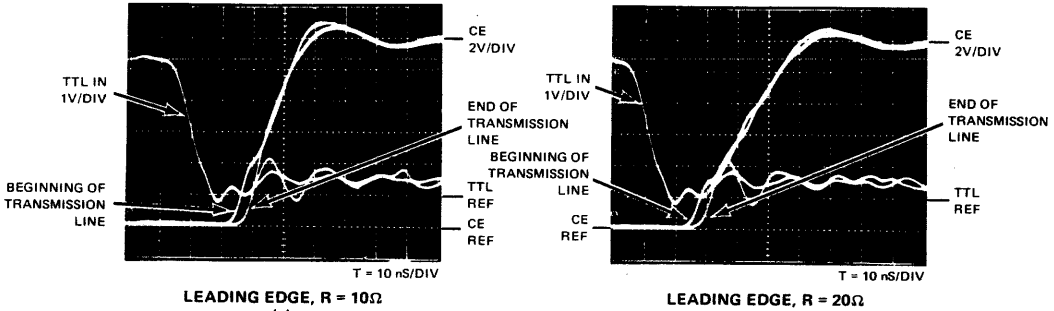


Figure 30. 3210 Typical Waveforms

Table V. Summary of 3210 Driver Board Delay Measurements

NUMBER 2107B LOADS AND CIRCUIT CONFIGURATION		MEASURED CONDITIONS INPUT TO OUTPUT DELAY				MEASURED DELAY[3] PLUS RISE		MEASURED DELAY[4] PLUS FALL	
		t_{-+}[1]		t_{+-}[2]					
		TYP.	WORST[5] CASE	TYP.	WORST[5] CASE	TYP.	WORST[5] CASE	TYP.	WORST[5] CASE
3210 18 LOADS[6]	R = 20Ω	16	16	10	10	48	50	35	35
3210 9 LOADS	R = 20Ω	14		8		30	32[7]	25	25[7]

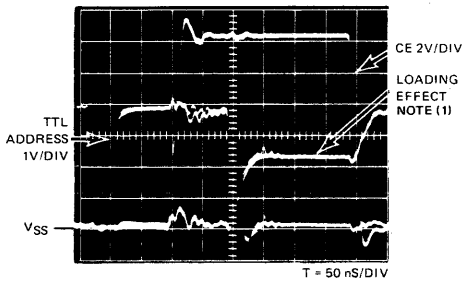
NOTES:

1. TTL 1.5 to V_{SS} +1 volt
2. TTL 1.5 to V_{DD} −1 volt
3. TTL 1.5 to V_{DD} −1 volt
4. TTL 1.5 to V_{SS} +1 volt
5. Worst case driver on board at 70°C and 5% power supply variation.
6. 18 loads 20Ω split resistor (see Figure 26).
7. Projected from 18 load delay.

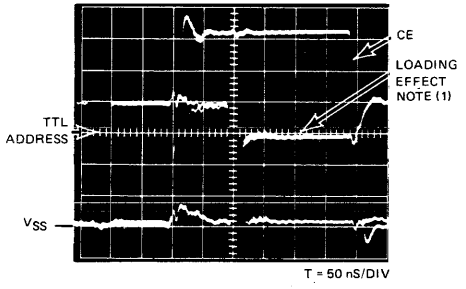
(such as shown in Figure 31) with an enable input. This will allow all addresses to be set up in a high state (above 2.4V) and be driven low when appropriate. Since TTL gates have much better drive capability in the high to low direction, the increase in delay due to the large capacitance is reduced.

It is not recommended that Schottky type TTL gates be used to drive the low level inputs of the 2107B. This is because under worst case conditions, the down level of the Schottky device is approximately 100 mv higher than for a regular or H series TTL gate. This higher level coupled with the address noise coupled from the 2107B (see Address Buffer/Latch section) might make some systems marginal in operation. In addition, the effect of chip enable transition on address low voltage reduces the maximum positive down level on the addresses. (See Device Specification section.)

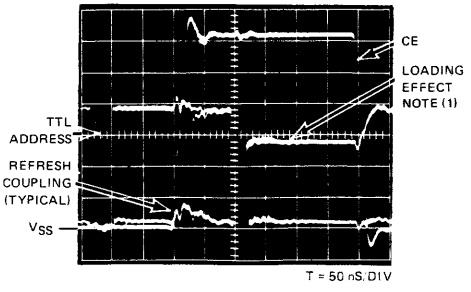
An example of TTL circuits (7400, 74H00, 74S00) driving 36 address inputs on the 2107B at refresh time is shown in Figure 32. Figure 33 shows the same TTL gate at "Read" time. Note the high level loading effect is greatly reduced because only 9 loads (2107B) are turned on at one time. Note that a Series 74S gate was used and is shown for reference only. From these photos the amount of overshoot present in driving high-low is clearly seen. Therefore, even with TTL drivers it is desirable to use series resistors to decrease the negative overshoot. This resistor value depends on the load on the driver and 20Ω is recommended when driving 36 address loads.



DRIVER TYPE 7400
(a)

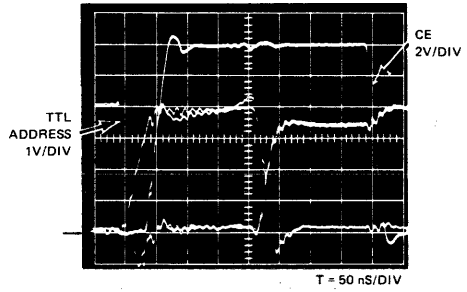


DRIVER TYPE 74H00
(b)

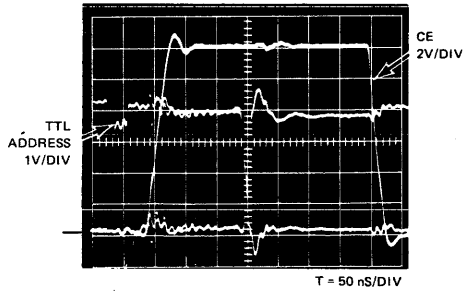


DRIVER TYPE 74S00
(c)

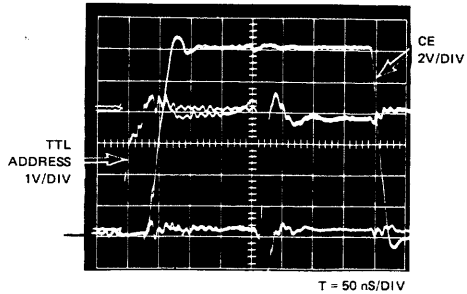
Figure 32. TTL Driver Waveforms (Refresh Cycle)



DRIVER TYPE 7400, R = 20Ω
(a)



DRIVER TYPE 74H00, R = 20Ω
(b)



DRIVER TYPE 74S00, R = 20Ω
(c)

Figure 33. TTL Driver Waveforms (Read Cycle)

In the discussion of the address latch circuitry (Address Buffer/Latch section) reference was made to input currents drawn by the address buffer when an address is switched from a low to high level during chip enable. The decrease in high level shown in Figure 32 is due to the 0.5 mA/2107B loading of the address line following the low to high transition while chip enable is on. (All photos from Figure 32 are taken at refresh time when all devices are on. This condition is worst case.)

Figure 32 also shows the effect of 36 memory devices coupling charge back to the address line [see Note (1) on photos]. This coupling limits the series resistance value which can be added to the address drivers to minimize overshoot. It also suggests that the address drivers be placed as close as practical to the memory array.

The photo shown in Figure 34 is the current associated with the low to high level address transition for 36 devices at refresh time. (Note the time delay of current relative to address voltage change. This is the result of delays associated with the current probe relative to the voltage probe.) For this example, the driver used is a 3210.

Other Low Voltage Driver/Buffers

When speed and high level drive capability is needed it is desirable to use drivers which are designed specifically for driving high capacitance loads with minimum delay. The 3245 and 3210 can be used to drive the 2107B low voltage inputs.

When operating the 3245 in a low voltage mode, the device is connected per schematic shown in Figure 35. As shown in this figure, the V_{DD1} pin (pin 1) is connected to V_{CC} (+5) and the V_{DD2} pin (pin 9) is connected to +12V. Photos of the waveforms of the 3245 in the low voltage drive mode are shown in Figure 36a and b. The circuit configuration is shown in Figure 35. As shown in the photo, the 3245 has very high drive capability in both the positive and negative directions.

For comparison, the low level buffer portions of the 3210 are shown in Figure 37a and b. As is shown, both the 3245 and 3210 make excellent low level buffer drivers for heavily loaded address lines.

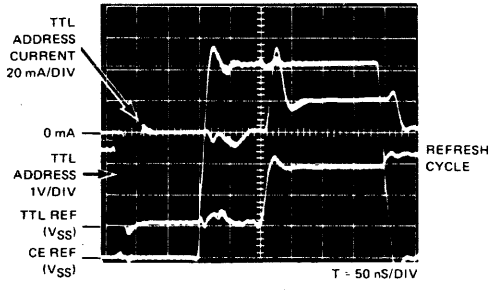


Figure 34. Typical Address Input Current

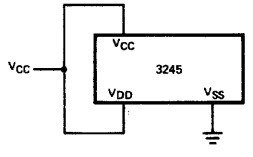


Figure 35. 3245 Connected in Low Voltage Drive Mode

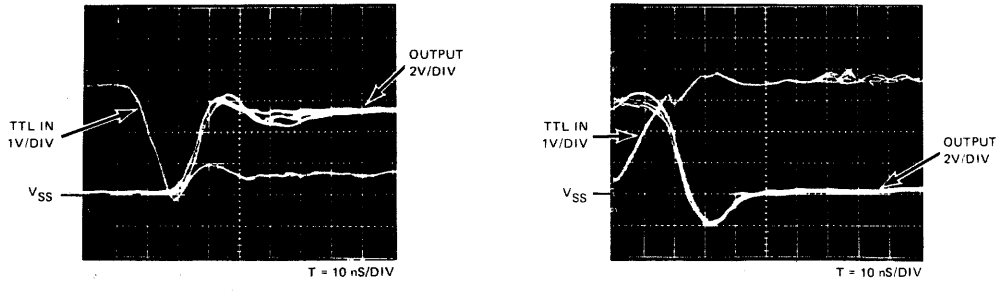


Figure 36. Typical Waveforms, 3245 Low Voltage Mode

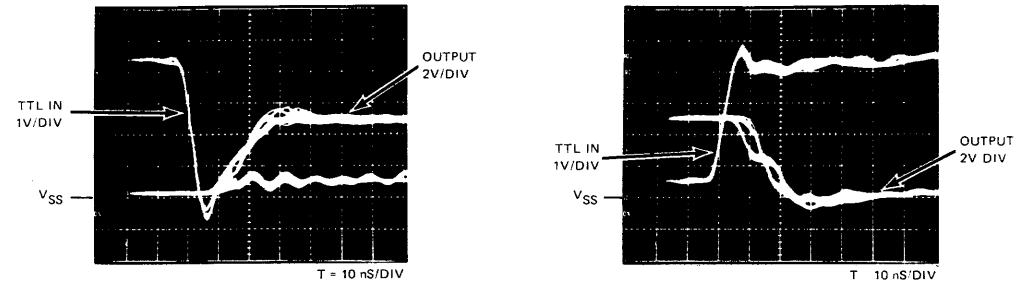


Figure 37. Typical Waveforms, 3210 Low Voltage Mode

Output Sensing

The output of the 2107B can be sensed with any TTL compatible series 74, 74L, 74LS or 74S gate. In addition, Intel provides a latch (3404) which features high speed and high density in a single package. The pin configuration for the 3404 is shown in Figure 38.

The V_{CC} input to the 2107B goes only to the output buffer as shown in Figure 8. This means that other types of outputs can be used instead of standard TTL devices if so desired. However, since there are many different ways to utilize this feature, do not exceed the maximum limits on voltage when using the 2107B in a non-standard manner.

Typical curves of output current as a function of output voltage are included in Figure 39a and b to facilitate the output interface of non-TTL loads.

System Timing and Control

The simplicity of design when using the 2107B memory component is shown by the schematic given in Figures 40, 41, and 42. The basic timing for this schematic is shown in Figure 43.

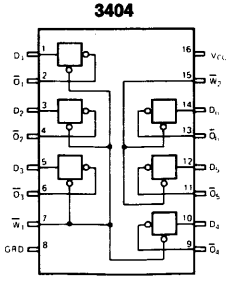
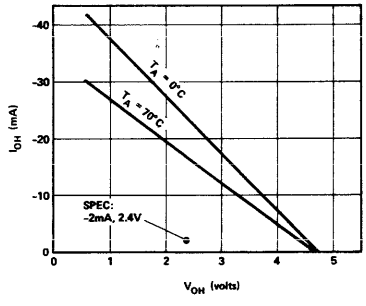


Figure 38. 3404 Pin Configuration

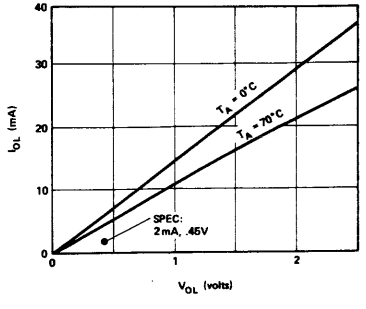
The design shown is for an expandable 16K X 18 system featuring:

1. Asynchronous memory requests/multiple ports
2. Free running refresh

The timing cycle consists of a start initiated by a memory request (MREQ) which triggers the busy latch and begins chip enable. The busy signal is used to disable other ports from requesting a memory cycle while the memory is being accessed from



(a) HIGH LEVEL OUTPUT



(b) LOW LEVEL OUTPUT

Figure 39. 2107B Output Characteristics

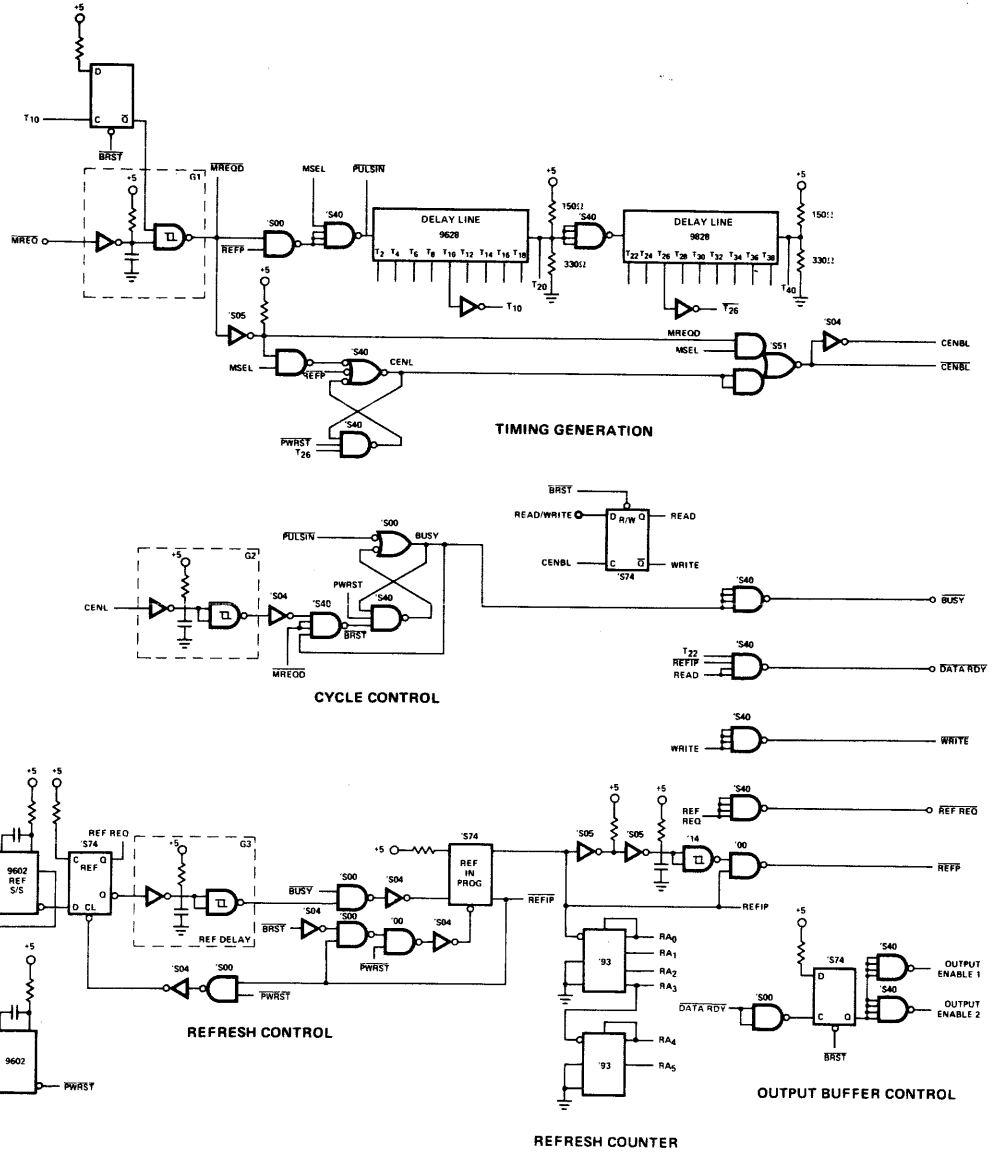


Figure 40. 16K X 18 Memory System Timing Generation

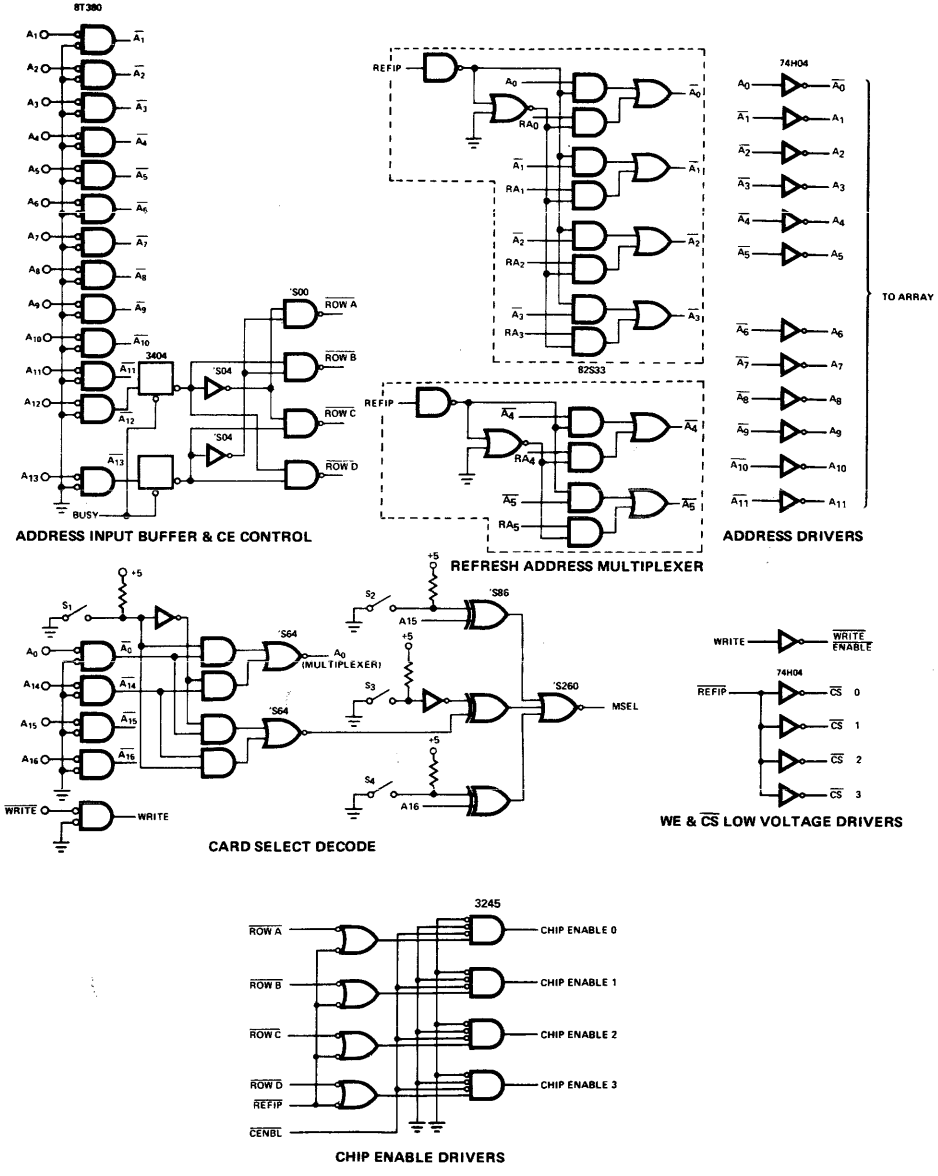


Figure 41. 16K X 18 Memory System Address Buffer Interface

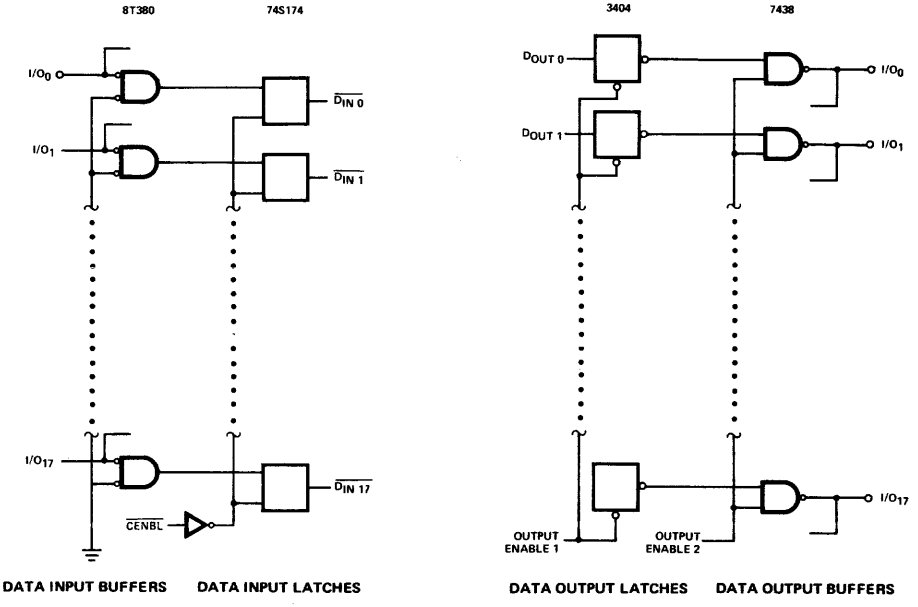


Figure 42. 16K X 18 Memory System Input/Output Interface

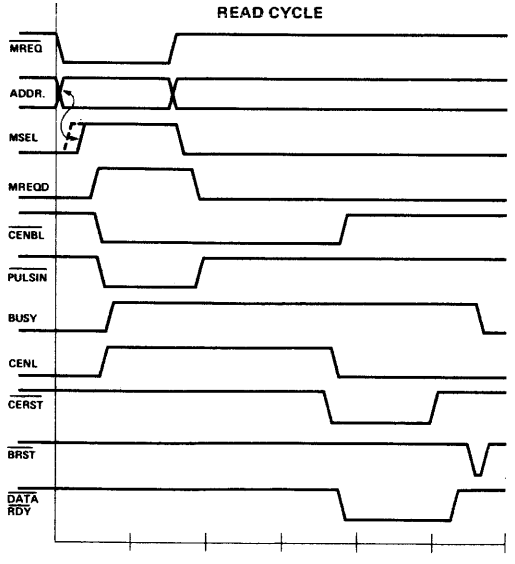


Figure 43. 16K X 18 Memory System Control Timing

another device. Since further timing signals for a read/write cycle are straightforward they will not be discussed further.

However, several things need to be said about the refresh circuitry. As many system designers know, when a memory system with asynchronous refresh runs into trouble in the checkout state, it is 99% sure to be refresh interference in one form or another in the control logic. The most likely cause of problems for asynchronous refresh is glitching between a refresh request and a normal cycle request resulting in false starts or the system not knowing whether or not it is in a refresh cycle or normal cycle.

To alleviate this problem it is necessary to determine that there are no possible requests coming from an external port to the memory when a refresh cycle is started. This will prevent the low order address line from making transitions at the wrong time (due to the multiplexer between the refresh and normal addresses) and taking excessive time to recover to the proper level.

The circuit which performs the function of delaying the onset of a refresh cycle is shown by G3 in Figure 40. Here, refresh is delayed for as long as necessary to assure that the refresh required latch (REF REQ) has had time to block further requests from all ports attached to the memory.

Attention is also called to the power on reset (PWRST) signal shown in Figure 40. This signal is necessary to assure that all latches have been reset (or set) to the proper state after power has been applied. In addition, note that the refresh/addresses RA_0 thru RA_5 are changed after the

refresh cycle is complete. This assures that the address will not be changing during refresh as chip enable goes high.

Memory Array Layout

The layout for the 2107B memory array can be identical to that used for the 2107A. An example of such a layout is shown in Figure 44. The layout in this example is constructed with grided power busing which minimizes power distribution noise. When using this technique it is important to remember to bus all power lines both vertically and horizontally through every memory component.

The effect of proper power distribution in the memory array cannot be over-emphasized. It is most desirable to bus the power lines both vertically and horizontally at every memory device location (even if it means running a 15 mil wide printed line to achieve the connection). If it is not possible to make such a connection at every location, then the interconnect should be done as much as possible throughout the array.

As a general rule of thumb, power distribution can be considered adequate if the distance from each power pin (e.g., V_{DD} to capacitor and V_{SS} to capacitor) to the closest decoupling capacitor is less than or equal to 1.5 inches.

For some layouts, particularly those which have all timing and control as well as the memory on a single board, it may be desirable to build multilayer boards. Attention should be paid to the construction of the internal planes to gain maximum effectiveness from these planes. If all the required power supplies cannot be distributed on internal

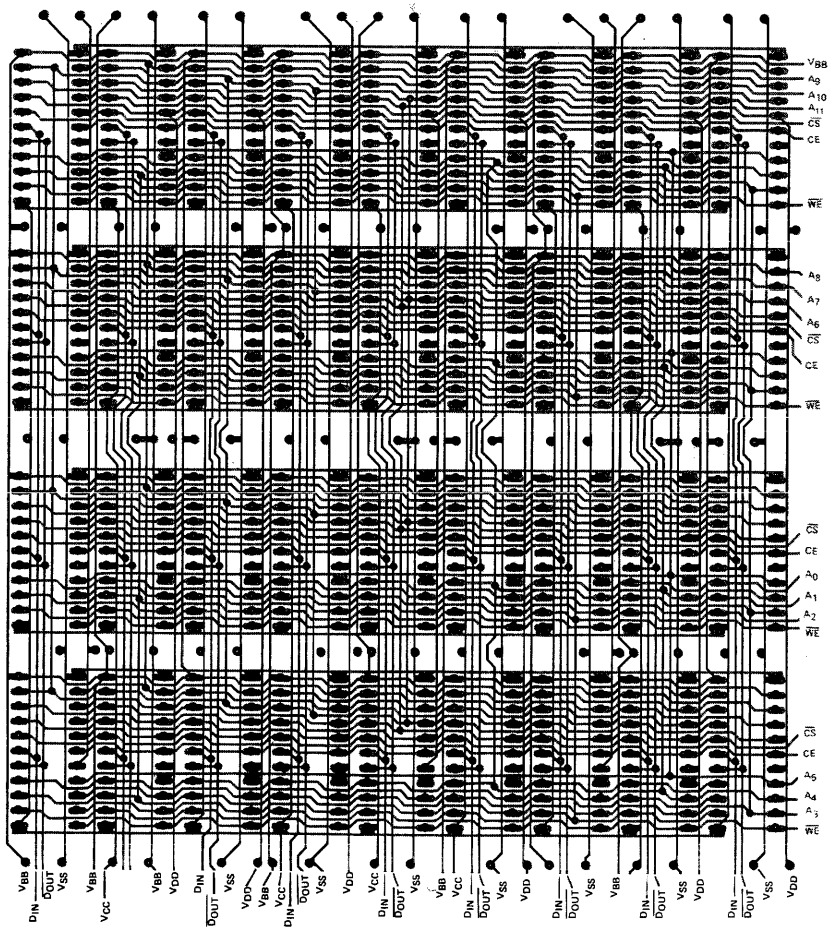


Figure 44. 2107B Memory Array Layout Using Grided Power Distribution

planes and any have to be left out and put on the upper surfaces of the board they should be removed from the internal plane in the following order:

1. V_{CC} 3. V_{DD}
2. V_{BB} 4. V_{SS}

Numbers 1 and 2 can be interchanged if there is a particularly heavy V_{CC} load due to timing, control, etc. circuitry on the board.

When constructing internal planes, care should be taken to obtain the most continuous plane possible. For example, the plane should have "fingers" between each IC feedthrough to minimize inductance.

Decoupling

As mentioned in the Transient Currents section, it is imperative to adequately decouple all supplies to the 2107B. The type and amount of decoupling recommended is most easily shown with the aid of the diagram given in Figure 45. In this figure, every other location for decoupling is V_{DD}–V_{SS} using a 1.0 μF capacitor. Alternate locations can be V_{BB}–V_{SS} or V_{CC}–V_{SS}. It is suggested that V_{BB}–V_{SS} be decoupled more heavily than V_{CC}–V_{SS} (as shown in Figure 45), because of the higher transients on V_{BB}. Noise on the V_{BB} distribution is shown in Figure 46.

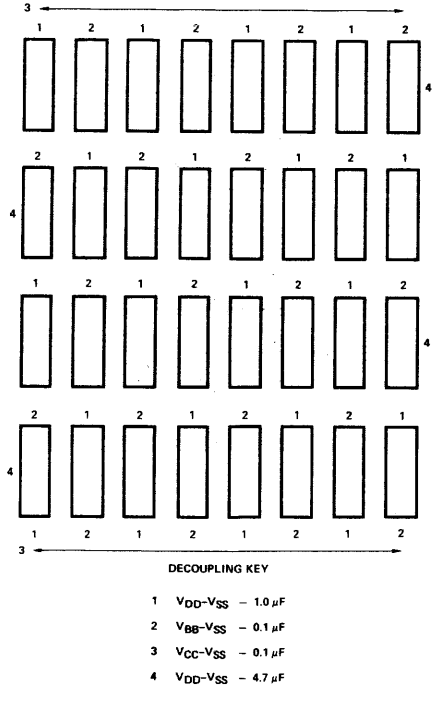


Figure 45. Recommended Memory Array Decoupling

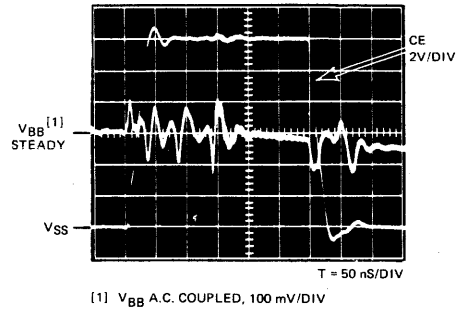


Figure 46. Typical V_{BB} Array Noise Decoupling per Figure 45

In addition to the 1.0 μF decoupling discussed above, it is necessary to provide a bulk of ~100 μF V_{DD}–V_{SS} per 36 devices located near the memory array. Also, placing 4.7 μF capacitors between V_{DD}–V_{SS} along the end of each row as shown will eliminate noise problems during refresh time.

The effect of changing decoupling capacitance in a system is shown in Figure 47a, b, c, and d.

These photos show the effects of different decoupling schemes on the V_{DD} supply and the effect of adding a more solid power distribution bus. (In this case #22 wire was paralleled with the existing power distribution of grided 15 mil printed line.) Each of the photos shown in Figure 47 were taken at the worst case location in the memory array at refresh time.

Figure 47a shows the V_{DD} supply with 0.1 μF spaced at every third device, no additional V_{DD} busing and no bulk capacitors (4.7 μF) at the end of each row. Note that the V_{DD} supply decreases to approximately 300 mv below desired setting with spikes driving the supply down a maximum of 440 mv. This excursion is not acceptable.

Figure 47b is for the condition of decoupling with 0.1 μF every third device and adding a 4.7 μF capacitor at the end of each row. Additional power busing on the V_{DD} and V_{SS} lines was added but was observed to have little effect on the noise, shown in Figure 47b. For this case, the V_{DD} supply is observed to decrease approximately 180 mv with spikes adding a further reduction to 240 mv. The major difference between this condition and the one shown in Figure 47a is the addition of the 4.7 μF capacitors at the end of each row. However, the decrease in V_{DD} voltage is still unacceptable.

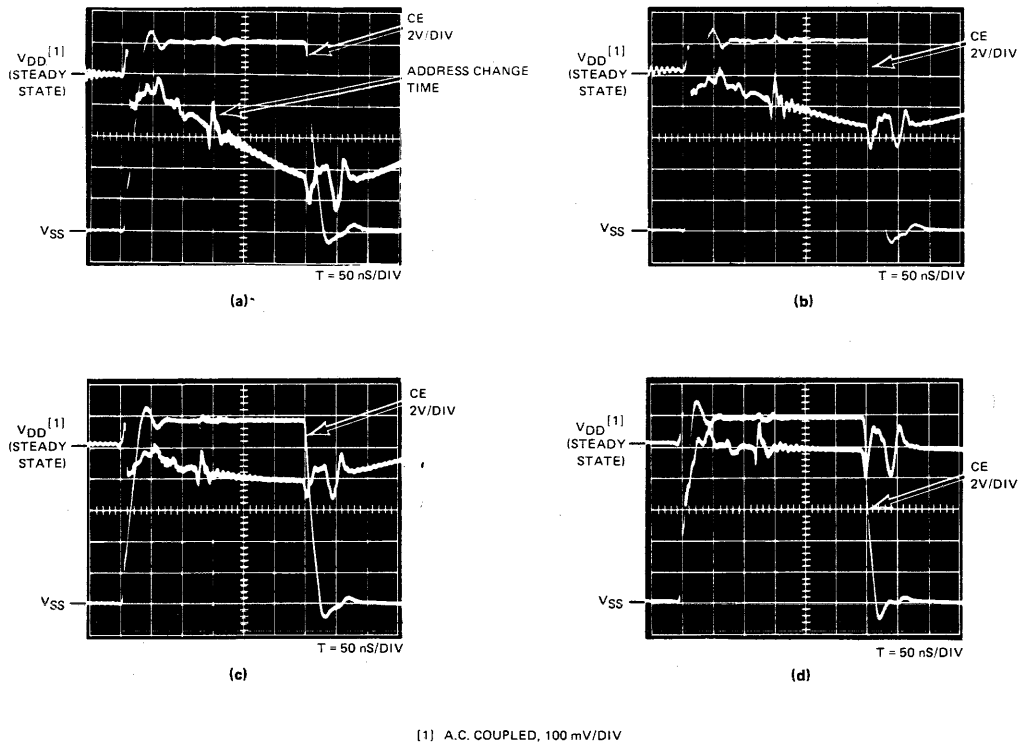


Figure 47. V_{DD} Noise as a Function of Decoupling

Figure 47c shows the V_{DD} supply where V_{DD} in the memory array is decoupled at every other memory device location. All other conditions are per Figure 47b. Note that the offset is now only 100 mv with spikes taking the supply down to 170 mv below nominal. Such decoupling results in adequate but marginally acceptable system operation.

Figure 47d shows the V_{DD} supply decoupled at every other memory device location with 1.0 μF ceramic capacitors. All other conditions are per Figure 47c. Note that the offset is approximately 20 mv with spikes lowering the V_{DD} to a maximum of 200 mv for the length of time shown.

The most desirable decoupling of V_{DD} to V_{SS} in a memory array is therefore 1.0 μF at every other device location with 4.7 μF at the end of each row.

The above recommendations on power distribution and decoupling will result in minimal memory array power noise. However, it is certainly not the only way to suppress power distribution noise. Adequate distribution and decoupling can be assumed if the following values are achieved:

1. $V_{DD}-V_{SS}$ 200 mv peak
2. $V_{BB}-V_{SS}$ 100 mv peak
3. $V_{CC}-V_{SS}$ 100 mv peak
4. $V_{SS}-V_{SS}$ 200 mv peak (corner to diagonal corner)

Debugging A Memory System

The design and build of memory systems using the newer, easier to use dynamic RAMs, usually results in minimum system debugging time. However, when this is not the case and the control and memory are not playing together well, life can be mighty miserable for the designer while the problem is being tracked down.

This section will deal with some of the more common problems that can affect dynamic memory systems in general, their characteristics and how to better identify them. An integral part of this section is the testing of the system to identify those conditions which cause the most problems for the memory system. In the following it is assumed that power supplies and timing are set to nominal values.

In debugging a memory system the most logical place to start is to determine that all specified criteria are met. This means looking at chip enable timing during each type of cycle both high and low

voltage level (read, write, read-modify-write, if used, and refresh). In all cycles make sure the addresses and chip select are set up at the proper time and are held for the minimum hold time. Check all other signals for proper levels (this especially includes the address down level at the time just after chip enable goes high). Remember that the maximum address down level is a function of the chip enable rise time. Erratic operation results from a slow transition and a marginal address down level. Next, check all voltage pins for excessive noise. It is usually desirable to check the power noise at refresh time since all memory devices will be on then and noise will be at a maximum.

After the above, sync on a read cycle and make sure that the system data strobe, if any, occurs before chip enable going low has a chance to reset the data. Also check to make sure no spurious write signals are getting through at read time. In a write cycle check the write enable waveform and make sure data-in is valid at or before write enable goes low.

In a refresh cycle, $\overline{\text{write enable}}$ should be held high unless chip select is high. Also, while in the refresh mode, make sure that all refresh addresses are being accessed. This is most easily done by syncing on the high order refresh address, A_5, and looking at the low order addresses for one cycle of A_5. Checking a read-modify-write cycle is merely a combination of the above discussion of read and write.

After confirming that the specification is met in all regards and that power supply noise is within tolerance in all cycles, the designer is probably tempted to harbor ill feelings toward the memory component and/or manufacturer of same. However, it is not yet time for such.

If the memory is failing most of the data and address patterns that are being used for the test, it is useful to inhibit refresh. When doing so, make sure that the test cycle is such that refresh is being done "automatically" by the normal cycles occurring at a fast enough rate. When inhibiting refresh it may be necessary to restrict the test addressing so that all cells can be "refreshed" by a normal cycle. If the problem goes away after inhibiting refresh, you are now in the army of people who have used dynamic RAMs to be caught with refresh interference.

The only thing that can be said about refresh interference is that refresh is coming in at the wrong time! In properly designed systems, the most likely culprit is a noise glitch getting into the refresh timing circuitry to cause the problem. One of the most common causes for other types of system design is the improper use of "D" type latches. For example, if an asynchronous input (relative to clock) is applied to the D input of a latch and clocked, there will be times where the change on the D input occurs simultaneously with the clock. In some latches this can cause an order of magnitude increase in delay instead of simply missing the D input (see Figure 48). This problem also exists when using a latch made of NAND gates (see Figure 49). The method of correcting the refresh interference problem of a system is left to the imagination and luck of the designer. If the problem is not refresh interference, do not harbor ill feelings yet!

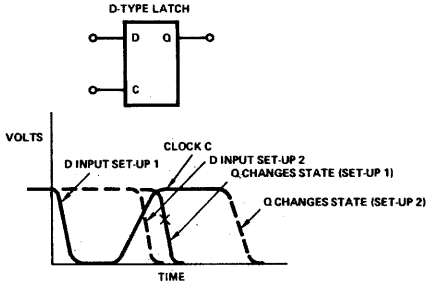


Figure 48. D-Type Latch

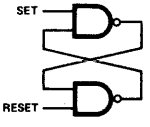


Figure 49. Cross-Coupled NAND Latch

After checking all of the above with no change in results, the next place to start is to determine whether the system is sensitive to addressing patterns. An effective test for evaluating address pattern sensitivity is Galpat. The structure of Galpat is shown in Figure 50. This test is time consuming and requires a careful monitoring of the failed data and its addresses.

Failures caused by a Galpat-only type test are most likely due to address line noise, address coupling to other signals, or refresh related. If address type noise is suspected a careful look at every point in each address path is in order. The best place to concentrate is around the address and its complement that failed.

Refresh related problems can occur during Galpat because this test takes a long time and may not "automatically" refresh the memory. (A sequential type test can refresh the memory automatically if it cycles faster than the maximum allowed

A "galloping" "1" or "0" thru memory consists of initializing the contents of memory (all "1s" or "0s") and implementing the following sequence at each successive memory location:

1. Write opposite data (from initialized state) into test address (A_{TEST})
2. Read next address (A_{TEST} + 1)
3. Read test address (A_{TEST})
4. Read A_{TEST} + 2
5. Read test address – continue read sequence for entire memory
6. Write test address back to initialize state
7. Go to next address for new A_{TEST}
8. Repeat steps 1–6 until entire memory tested
9. Complement initial data pattern and repeat steps 1–8

Figure 50. Galpat Flow Chart

refresh period.) If any address fails to get refreshed during the refresh period, Galpat will most likely pick it up.

If the above does not yield a clue, then a check of the data pattern across a word is in order. In many tests each bit in a word contains the same data. This can cause certain groups of data lines to couple into adjacent control or address lines. This problem can be tracked down by allowing only one bit in a word to change at a time.

If the memory system is having massive failures, it is very likely that the above debug procedure will reveal the problem. The second type of problem to be discussed is that of soft failures at frequent intervals. In general, these are problems caused by system noise, marginal timing, flaky peripheral device(s), or marginal memory component.

For soft failures, the first item to suspect is refresh interference. Proceed per above to isolate the problem.

A great deal of information on soft failures at nominal voltage settings can be obtained by shmooing the memory system. A shmoo consists of varying each voltage in a manner which is worst case for certain conditions.

The voltage points which emphasize certain tendencies in the memory are contained in Figure 51. The device failed address should be noted at each shmoo point to give a clue to the problem.

A broad guideline here is as follows:

Failure	Cause
1. V_{DD} low, $\|V_{BB}\|$ high	– timing marginal (memory tends to slow down).
2. V_{DD} high, $\|V_{BB}\|$ low	– noise in system. Look for V_{SS}, V_{DD}, V_{BB} noise.

Temperature variation can also reveal similar problems. For example:

Failure	Cause
1. High temperature	– timing should be suspected.
2. Low temperature	– noise should be suspected.

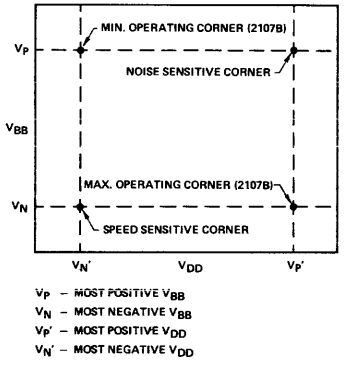


Figure 51. Example of Memory System Shmoo Plot

Power Calculations

The typical power dissipation for the 2107B with a chip enable on time of 230 nsec and a 400 nsec cycle is calculated as follows for a typical device:

Device Power

$$1.\ P_{DOP} = \begin{bmatrix} V_{DD} \times I_{DD\,AV} \\ +V_{BB} \times I_{BB} \end{bmatrix}$$

$$= \begin{bmatrix} 12.0 \times 38\ mA \\ +\ 5.0 \times 0.1\ mA \end{bmatrix} = 456.5\ mw$$

Since the calculation of standby power without refresh for dynamic memory is meaningless, the following calculations are for standby with refresh:

$$2.\ P_{DOP} = \begin{bmatrix} V_{DD} \times I_{DD1} \\ +\ V_{BB} \times I_{BB} \end{bmatrix}$$

$$= \begin{bmatrix} 12.0 \times 0.11\ mA \\ +\ 5.0 \times 0.1\ mA \end{bmatrix} = 1.82\ mw$$

3. $P_{DSB} = P_{DOP}\left(\frac{N\,T_{CY}}{T_{REF}}\right) + P_{NOP}\left(\frac{T_{REF}-N\,T_{CY}}{T_{REF}}\right)$

where: P_{DOP} = Operating power disspiation
P_{NOP} = Non-operating (chip enable low) power dissipation
P_{DSB} = Standby/Refresh power
N = Number of refresh cycles in refresh period
T_{REF} = Refresh period in μsec
T_{CY} = Refresh cycle time in μsec

For the 2107B, the following values apply:

N = 64
T_{REF} = 2000 μsec
T_{CY} = 0.40 μsec

4. $P_{DSB} = 456.5\left(\frac{64\,(0.400)}{2000}\right) + 1.82\left(\frac{2000-25.6}{2000}\right)$ mw

or

5. $P_{DSB} = (5.84 + 1.80)$ mw

6. $P_{DSB} = 8.6$ mw

The above calculations do not include V_{CC} power since it is dependent only upon the output load used. The output of the 2107B is in a high impedance state when chip enable is low or chip select is high and only leakage level currents flow under these conditions.

System Power

In most systems only a portion of the memory devices will be continually accessed. For example, in the system previously described (16K X 18) worst case power is a continual access of one row (the other three rows are dissipating power in the refresh only mode).

System power for the 16K X 18 system is calculated from:

1. $P_{SYS} = P_{DS} \times N + P_{DA} \times M + P_{DOP} \times D + P_{DSB} \times E$

where: P_{DS} = Power dissipated in drivers during standby (including refresh)
N = Number of drivers in standby
P_{DA} = Power dissipated in drivers during max. duty cycle operation
M = Number of drivers in max. duty cycle operation
P_{DOP} = Power dissipated by memory device max. duty cycle
D = Number of devices in P_{DOP}
P_{DSB} = Power dissipated by memory devices during standby (including refresh)
E = Number of devices in P_{DSB}

For this example, all drivers are assumed to be 3210s. Therefore:

P_{DS} = 387 mw N = 6
P_{DA} = 467 mw M = 2
P_{DOP} = 456.5 mw D = 18
P_{DSY} = 8.6 mw E = 54

or

$$P_{SYS} = \overbrace{387 \times (6) + 467\,(2)}^{\text{Driver Power}} + \overbrace{456.5\,(18) + 8.6\,(54)}^{\text{Memory Component Power}}$$

2. $P_{SYS} = \overbrace{2322 + 934}^{\text{Drivers}} + \overbrace{8217 + 464}^{\text{Memory Devices}}$

$P_{DRIVERS}$ = 3256 mw
P_{MEMORY} = 8681 mw

or

Total System Power:

3. P_{SYS} = 11.9 watts

The power dissipated by the drivers is approximately 26% of total system power in a max.–duty cycle operating environment.

Total standby power (including refresh is calculated from equation (1) where:

N = 8 M = 0 D = 0 E = 72

or:

4. $P_{SYS} = \overbrace{387\,(8)}^{\text{Driver}} + \overbrace{8.6\,(72)}^{\text{Memory}}$

$P_{SYS} = (3096 + 619)$ mw

or

$P_{DRIVERS}$ = 3092 mw
P_{MEMORY} = 619 mw

5. P_{SYS} = 3.7 watts

Note that in this case, driver power amounts to approximately 83% of total system power.

Power Supply Sequencing

The V_{BB} substrate bias supply must never be allowed to be more positive than 0.3V above V_{SS}, V_{DD}, or V_{CC} at any time. Catastropic device failure can result if these criteria are not met. To minimize this problem of power sequencing and inadvertent power shorts, it is recommended that V_{BB} be referenced to V_{SS}.

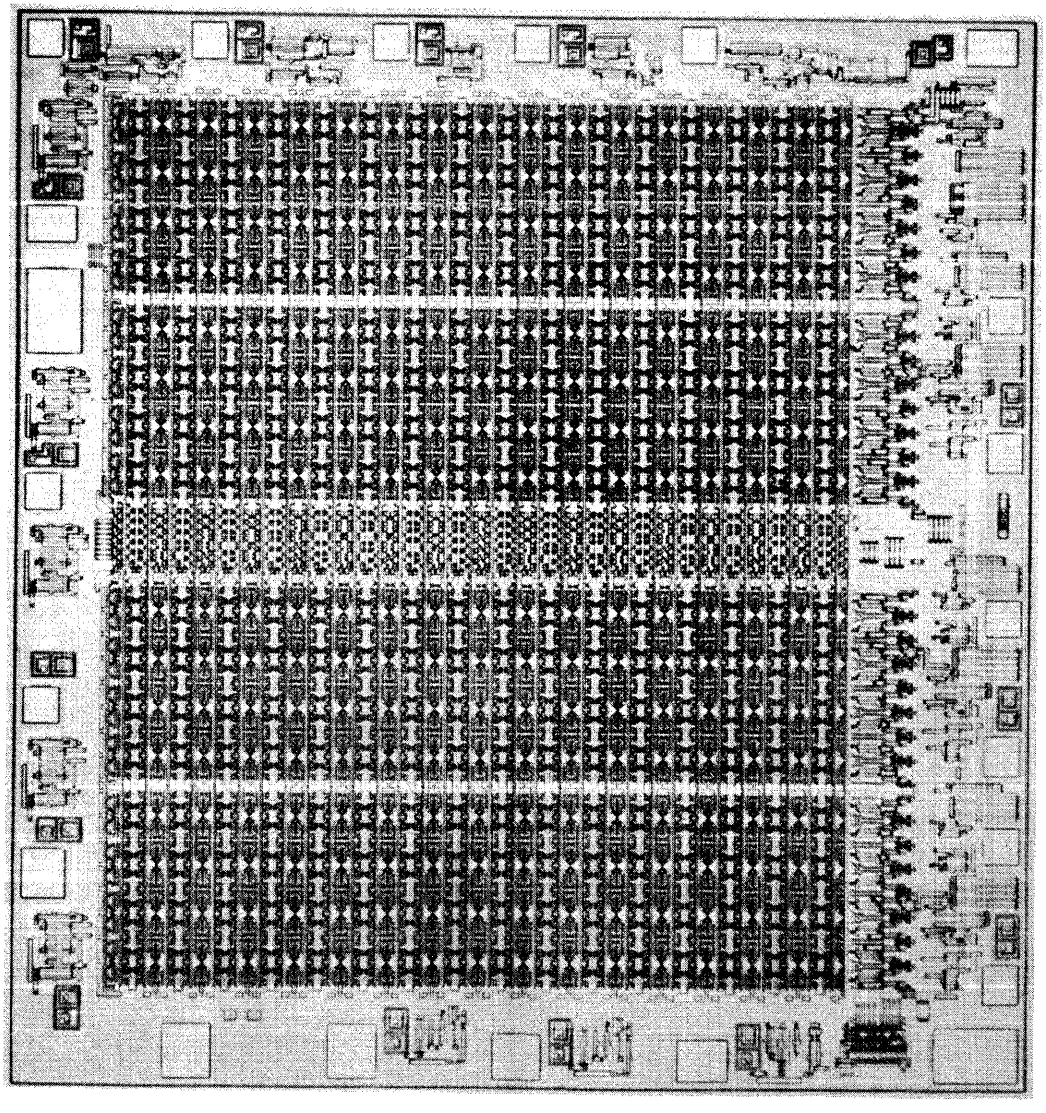
ACKNOWLEDGMENT

Appreciation is extended to R. L. Papenberg of the Application Engineering Department for his work on the 3245 and 3210 driver system evaluation.

Designing Non-Volatile Memory Systems with Intel's 5101 RAM

Jim Oliphant
Application Engineering

Contents



Photomicrograph of 5101 CMOS RAM

INTRODUCTION

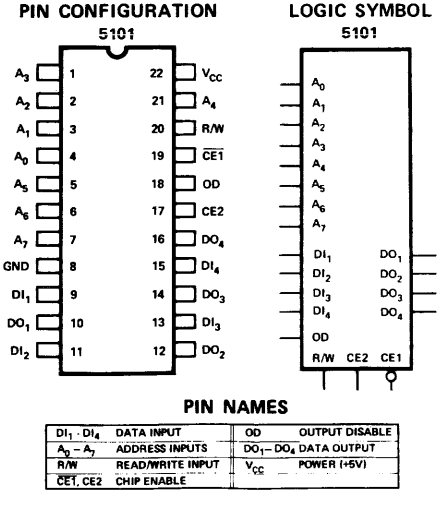
The Intel® 5101 is an ultra-low power 1024 bit static RAM organized as 256 words X 4 bits. It is fabricated with an advanced ion-implanted silicon gate CMOS technology. The 5101 is fully TTL compatible, uses only a single supply voltage V_{CC} (+5V) and does not require a clocking operation on the chip enable input. This device is ideally suited for low power and high speed applications where battery support for non-volatility is required.

The purpose of this application note is to describe the internal circuitry and operation of the 5101 and to outline various circuit techniques for battery supported non-volatile operation. In addition, designs using the 5101 will be described and the interface discussed.

DEVICE DESCRIPTION

The 5101 is pin compatible with the Intel® 2101 n-channel silicon gate static MOS RAM. The internal circuitry, however, differs from the 2101 in that the 5101 is implemented with CMOS technology and the 2101 is implemented with n-channel technology. (However, both the 5101 and 2101 are TTL compatible.) The pin configuration and logic symbol for the 5101 are shown in Figure 1. Memory expansion is simplified by the use of two chip enables $\overline{CE}_1$ and CE_2. CE_2 may be used to place the memory in the ultra low power standby mode completely independent of the state of *all* other inputs. In addition, an output disable pin is provided to place the internal data output buffers in a high impedance state. This is particularly useful in those systems which have a common data bus. Both the output disable and chip enable features will be discussed in more detail in the Systems Considerations section.

A block diagram for the 5101 is shown in Figure 2. The memory array is arranged in a 32 X 32 matrix. The five low order addresses A_0-A_4 select 1 of 32 rows; the three high order addresses A_5-A_7 select 1 of 8 column select lines. Each of the column select lines enable 4 of the 32 columns. Figure 3 shows a selection matrix for the selection of a given address to the 5101.



PIN NAMES

DI_1 - DI_4	DATA INPUT	OD	OUTPUT DISABLE
A_0 – A_7	ADDRESS INPUTS	DO_1– DO_4	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)
$\overline{CE1}$, CE2	CHIP ENABLE		

Figure 1. 5101 Pin Configuration and Logic Symbol

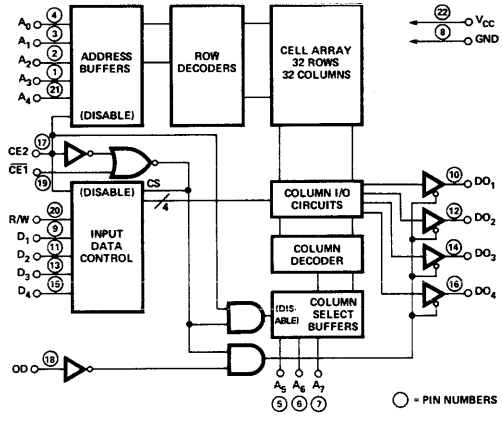


Figure 2. 5101 Block Diagram

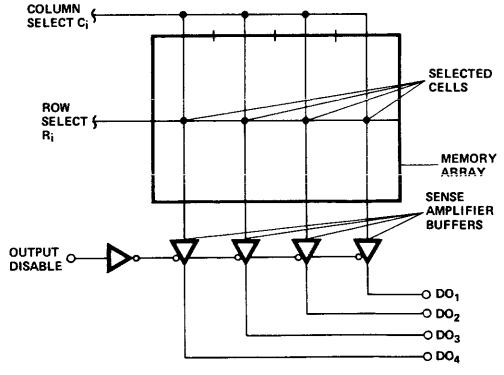


Figure 3. 5101 Selection Matrix

As shown in the block diagram, $\overline{CE_1}$ and CE_2 control the input data buffers and output data buffers. If either $\overline{CE_1}$ is high or CE_2 is low, the data-in and read/write buffers are disabled and the memory is isolated from the data in inputs. Likewise when either or both of the chip selects are in the non-select state (see Table I) the output buffers are placed in a high impedance state. When the chip is selected (i.e., $\overline{CE_1}$ is low and CE_2 is high), the output disable pin (OD) can be used to place the output buffers in a high impedance state.

Table I. 5101 Output State & Selection Matrix

OD	$\overline{CE_1}$	CE_2	Selection	Output
H	H	H	Deselected	High Imp.
H	H	L	Deselected	High Imp.
H	L	H	Selected	High Imp.
H	L	L	Deselected	High Imp.
L	H	H	Deselected	High Imp.
L	H	L	Deselected	High Imp.
L	L	H	Selected	Enabled
L	L	L	Deselected	High Imp.

Device Operation

STORAGE CELL

The storage cell used in the 5101 is implemented with 6 MOS transistors as shown in Figure 4. The six transistors are connected to form a cross-coupled latch which acts as the memory element. Note that the logic and gating transistors Q_1, Q_3, Q_5, and Q_6 are n-channel enhancement mode (normally off) MOS devices. The load transistors Q_2 and Q_4 are p-channel enhancement mode devices.

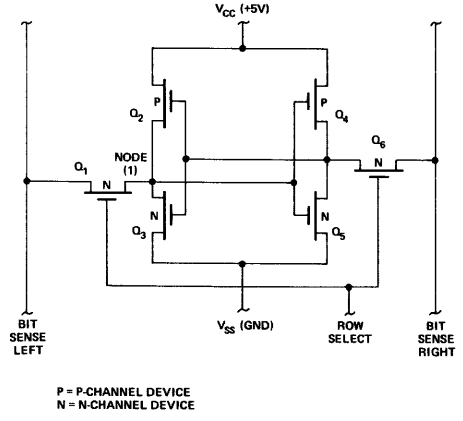


Figure 4. 5101 Storage Cell

In the following discussion of storage cell operation, remember that an n-channel device will be "on" if the gate is at a high level (~V_{CC}). A p-channel device will be "on" if its gate is at a low level (~GND). Operation of the storage cell is as follows:

Assume that the gate of Q_3 is at a high level (V_{CC}), device Q_3 is therefore turned on (it is an n-channel device) while device Q_2 is turned off (it is a p-channel device). Node (1) is therefore pulled to V_{SS} (ground) and cross-coupled back to the gates of devices Q_4 and Q_5. This low level on node (1) will turn device Q_4 on and Q_5 off. Since the output of Q_4-Q_5 is fed back to the gates of Q_2 and Q_3, an initial charge of V_{CC} on the gate of Q_3 will hold the latch in the above state. This logic state (node 1 at GND) is defined as a "1". The cell contains a logic "0" if the gate of Q_4 and Q_5 is high (V_{CC}) which puts node (1) at V_{CC}. Table II summarizes the state of the memory cell for a logic "1" and logic "0".

Table II. 5101 Memory Cell State

Cell State	Q_2	Q_3	Q_4	Q_5
Logic "0"	On	Off	Off	On
Logic "1"	Off	On	On	Off

Note that in the above discussion no mention was made of any d.c. currents flowing to set the proper voltage levels in the latch. This is because there aren't any. For the example given, the gate of Q_3 is held high (V_{CC}) by device Q_4 (the p-channel load). Since Q_5 is off there is no d.c. path for the current to take in the quiescent state. The only current flowing is the junction leakage currents associated with the source/drain of the MOS devices. This current is typically in the nano-ampere range.

The memory cell is accessed for a read or write operation by activating the appropriate row select line (i.e. row select is brought to V_{CC}). This turns on devices Q_1 and Q_6 and allows data on the bit sense lines to be written into the cell or the state of the cell to be interrogated (read) by a sense amplifier placed on the bit sense lines. For a write operation Bit Sense right is set high (V_{CC}) to write a "1" or Bit Sense left is set high (V_{CC}) to write a "0". The opposite Bit Sense line is held low (V_{SS}).

ADDRESS BUFFER

The address buffers translate the low level TTL address inputs (V_{IL} max. = 0.65V, V_{IH} min. = 2.2V) to a CMOS level (high = V_{CC}, low = V_{SS}) for internal use. The buffer configuration used is shown in Figure 5.

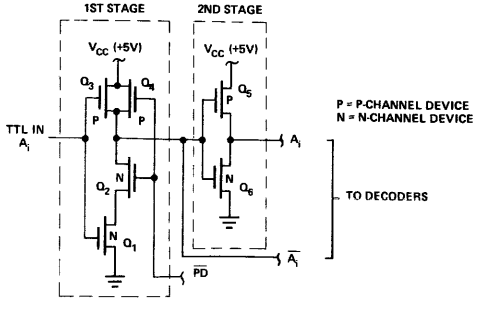


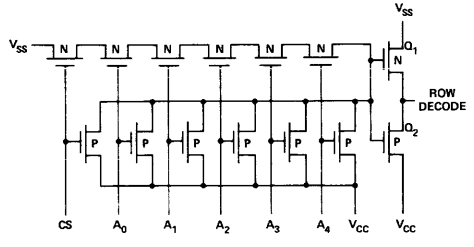
Figure 5. 5101 TTL Address Buffer

The first stage of the address buffer consists of a NAND gate (Q_1, Q_3) with control gates (Q_2, Q_4) added to *disconnect* the TTL address from the decoders when the device is not selected (that is, CE_2 is low). This places the address buffers in a standby mode (only leakage currents flowing) and eliminates the need to control the state of the addresses during standby. The internally generated signal $\overline{PD}$ which blocks the input addresses from the internal decoders is generated from CE_2. The second stage is an inverting buffer to provide increased drive for the A_i addresses.

Note that when the device is in a quiescent state no d.c. current is being drawn by the buffer. Therefore, the power dissipated during operation is very small and amounts to only the leakage current associated with the source/drain p-n junctions.

DECODERS

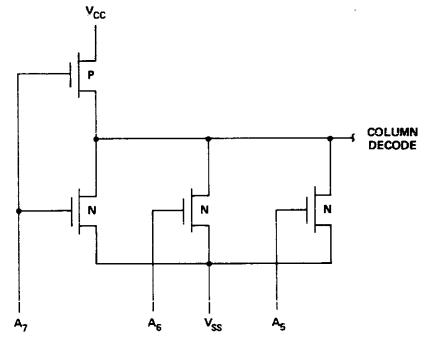
The row decoders (selecting 1 of 32 rows) on the 5101 use an AND gate of the type shown in Figure 6. To activate the selected row decode line, the five addresses going to that particular decoder must be at a high level and the internal chip select (CS) must be high. (Chip select is formed by the logical AND of CE_2 and $\overline{CE_1}$). If all address inputs to the decoder are high, a low is placed on the gates of the inverter buffer (devices Q_1 and Q_2) which will turn Q_1 off and Q_2 on. The selected row decode line is thereby brought high, turning on the appropriate gates in the selected memory cells. If the device is not selected, then CS forces all row decoder lines low which disables any access to all memory cells.



P = P-CHANNEL DEVICE
N = N-CHANNEL DEVICE
CS = $\overline{CE1} \cdot CE2$

Figure 6. 5101 Row Decode

The column decoders use a NOR type gate shown in Figure 7. The selected column decode line goes high if the 3 addresses (A_5-A_7) being decoded are all at a low level. Note that the internal column decoder uses only three address inputs. These three inputs select 1 of 8 separate decode lines. Each of the 8 decode lines select 4 columns for each word addressed.



P = P-CHANNEL DEVICE
N = N-CHANNEL DEVICE

Figure 7. 5101 Column Decode

INTERNAL DATA SENSING

A simplified schematic of the 5101 column sense amplifier is shown in Figure 8. The sense amplifier is constructed in an AND configuration with the I/O left line of each column of memory cells AND'ed with a particular column decode (devices Q_1 and Q_2). The line to the output buffer, O_B, is held at V_{CC} by device Q_3 unless both the I/O left line *and* the column decode line (for that particular column) are both high (logic "0" in the memory cell). In this case, the output of the sense amplifier O_B will be driven to a low level (slightly above GND). For example, if memory cell "M" shown in Figure 8 contained a "0" (I/O left high) then O_B would be low. However, if "M" contained a "1" (I/O left low) then O_B would remain high.

Devices Q_4 and Q_6 shown in Figure 8 are used as a load on the particular I/O line. The n-channel devices (Q_5 and Q_7) are used to limit the logic swing on the I/O lines.

Data is written into the memory cell by the circuitry shown in Figure 8. Note that the I/O right line goes high only when a logic "1" (high level) is applied to the data-in input on a selected device during a write cycle. The I/O left line, however, goes high when either a low is on the data-in input or the chip is non-selected. (Recall that for a non-selected device, all row selects are at the non-selected state, i.e. low level.)

OUTPUT BUFFER

A simplified schematic for the 5101 output buffer is shown in Figure 9. As shown in this figure the output buffer is implemented with complementary n-channel and p-channel drivers. For this type of driver, the gates of devices Q_1 and Q_2 must be at the same logic level (high or low) so that one of these devices is on while the other is off for a nor-

mal read operation. However, when the chip is deselected (the internal CS is low) or output disable is high, both Q_1 and Q_2 are turned off and the Data Out output goes to a high impedance state.

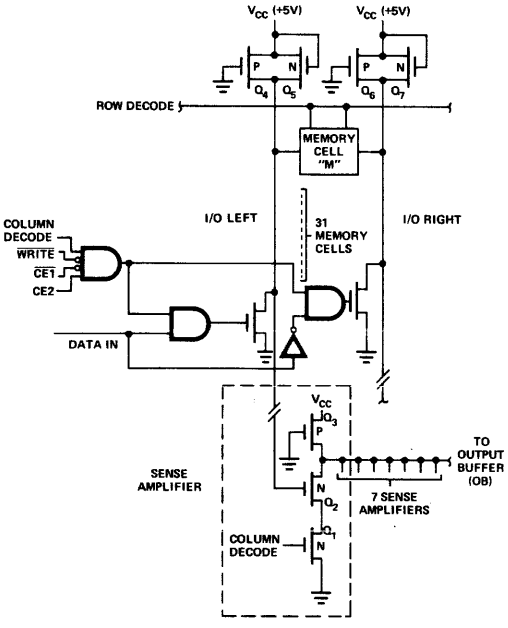


Figure 8. 5101 Column Sense Amplifier

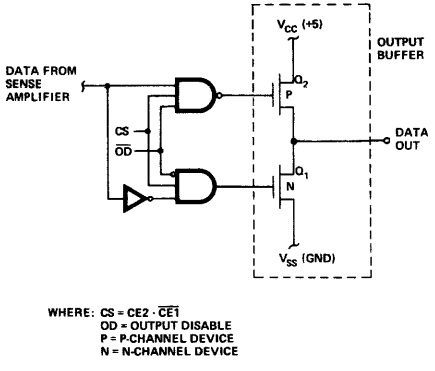


Figure 9. 5101 Output Buffer

Device Specifications

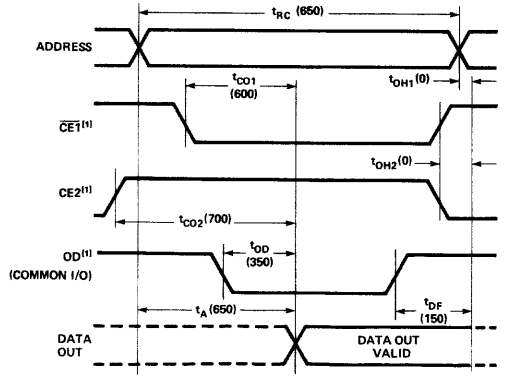
READ CYCLE

Minimum timing for a 5101 read cycle is shown in Figure 10. This timing diagram shows the relationship of all necessary control signals required for a read cycle and is for a general application. However, if the user has certain flexibilities in his system, other modes of operation are possible.

For those systems which have separate data inputs and outputs in the memory array, the output disable input (pin 18) may be tied low. Also, if the input and output pins of the 5101 are not OR tied to any other device both chip enable inputs may be held true (i.e. $\overline{CE_1}$ is held low and CE_2 is held high) while the addresses are being cycled in any order for a series of read cycles. For this case, the read/write input must be held high throughout the read operations. However, when operating the 5101 with CE_2 held high, it is necessary to control the voltage level of all inputs if ultra low power dissipation is desired. The ultra low standby power can be achieved with $\overline{CE_1}$ *only* deselected (i.e. at a high level) by holding all address, chip enable, data-in and read/write inputs to *one* of the following levels:

1. $V_{in} \leq 0.2V$
2. $V_{in} \geq V_{CC} - 0.2V$

Note that $\overline{CE_1}$ may be tied low, if so desired, and the ultra low standby power controlled only with CE_2 (i.e. $CE_2 \leq 0.2V$, all other inputs in a "don't care" state). The definition of terms outlined in Figure 10 is contained in Table III.



1. SEE TEXT "READ CYCLE".
2. NUMBERS IN PARENTHESES ARE IN NSEC.

Figure 10. 5101 Read Cycle

Table III. 5101 Read Cycle A.C. Characteristics. $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	650			ns	
t_A	Access Time			650	ns	Input Pulse Levels +0.65V to 2.2V.
t_{CO1}	Chip Enable ($\overline{CE1}$) to Output			600	ns	
t_{CO2}	Chip Enable (CE2) to Output			700	ns	Input Pulse Rise and Fall Times 20 nsec.
t_{OD}	Output Disable To Output			350	ns	
t_{DF}	Data Output to High Z State	0		150	ns	Timing Measurement Reference Level 1.5V.
t_{OH1}	Previous Read Data Valid with Respect to Address Change	0			ns	Output Load 1 TTL Gate and $C_L = 100pF$.
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns	

Table IV. 5101 Write Cycle A.C. Characteristics. $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	650			ns	
t_{AW}	Write Delay	150			ns	Input Pulse Levels +0.65V to 2.2V.
t_{CW1}	Chip Enable ($\overline{CE1}$) To Write	550			ns	
t_{CW2}	Chip Enable (CE2) To Write	550			ns	Input Pulse Rise and Fall Times 20nsec.
t_{DW}	Data Setup	400			ns	
t_{DH}	Data Hold	100			ns	Timing Measurement Reference Level 1.5V.
t_{WP}	Write Pulse	400			ns	
t_{WR}	Write Recovery	50			ns	Output Load 1 TTL Gate and $C_L = 100pF$.
t_{DS}	Output Disable Setup	150			ns	

WRITE CYCLE

Minimum timing for a 5101 write cycle is shown in Figure 11. The waveforms shown in Figure 11 are for a general application of the 5101 during a write cycle and may be modified to some degree depending on the users requirements. For example, if no other data inputs or outputs are OR tied to the 5101, $\overline{CE_1}$ may be held low, CE_2 held high and output disable held low.

However, it is *not* permissible to hold the read/write line low while cycling through addresses for a series of write cycles. Attempting to perform a series of write cycles in this manner will result in writing into multiple address locations during address transitions.

Although it is not necessary to conform exactly to the waveforms shown in Figure 11 for a write cycle, care should be taken to assure all minimum timing constraints, listed in Table IV, are adhered to. Particular attention should be paid to T_{aw} (address to write set-up time), T_{cw1} and T_{cw2}.

Since the 5101 is a completely static random access memory, it does not require an edge on any input line (e.g. chip enable or address) to initiate a cycle. Therefore, when a device is enabled (i.e. $\overline{CE_1}$ is low and CE_2 is high) and addresses are changed, time must be provided for the row and column decoders to settle (T_{aw}) before commencing a write to make sure undesired address locations are not partially rewritten by the data on the data input line.

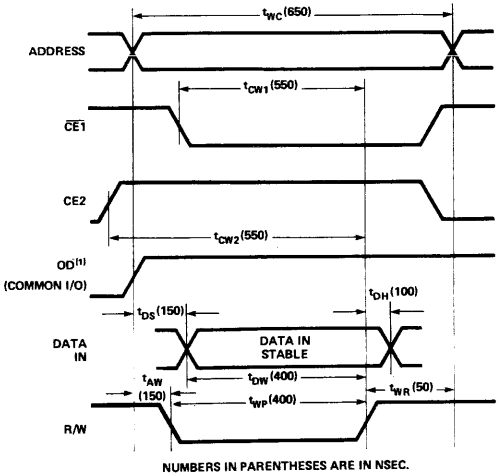


Figure 11. 5101 Write Cycle

Table V. D.C. Operating Characteristics. $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current		5		nA	$V_{IN} = 0$ to 5.25V
I_{LOH}	Output High Leakage			1	μA	$\overline{CE1} = 2.2V, V_{OUT} = V_{CC}$
I_{LOL}	Output Low Leakage			-1	μA	$\overline{CE1} = 2.2V, V_{OUT} = 0.0V$
I_{CC1}	Operating Current		9	22	mA	$V_{IN} = V_{CC}$ Except $\overline{CE1} \leq 0.01V$ Outputs Open
I_{CC2}	Operating Current		13	27	mA	$V_{IN} = 2.2V$ Except $\overline{CE1} \leq 0.65V$ Outputs Open
I_{CCL}[2]	Standby Current			15	μA	$V_{IN} = 0$ to V_{CC}, Except $CE2 \leq 0.2V$
V_{IL}	Input "Low" Voltage	-0.3		0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			0.4	V	$I_{OL} = 2.0mA$
V_{OH}	Output "High" Voltage	2.4			V	$I_{OH} = -1.0mA$

NOTES: 1. Typical values are $T_A = 25°C$ and nominal supply voltage.
2. Current through all inputs and outputs included in I_{CCL}.

Table VI. 5101L Low V_{CC} Data Retention Characteristics. $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions	
V_{DR}	V_{CC} for Data Retention	2.0			V	$CE2 \leq 0.2V$	$V_{DR} = 2.0V$
I_{CCDR}	Data Retention Current			15	μA		
t_{CDR}	Chip Deselect to Data Retention Time	0			ns		
t_R	Operation Recovery Time	t_{RC}[2]			ns		

NOTES: 1. Typical values are $T_A = 25°C$ and nominal supply voltage.
2. t_{RC} = Read Cycle Time.

D.C. OPERATING CHARACTERISTICS

The D.C. operating characteristics of the 5101 are given in Table V. I_{CCL} (standby current) in Table V is emphasized because of its importance in standby battery back-up operation. Note that the maximum value of the standby power supply current is an extremely low 15μA (and is typically only 0.2μA). If CE_2 is used to control the low power state (i.e. $CE_2 \leq 0.2V$), then the state of all other inputs is a "don't care." If $\overline{CE_1}$ is used to control the low power state, all inputs must be either high or low (as defined in Read Cycle section). As is shown later, (in the Systems Considerations section) this allows the designer maximum flexibility in the design of simple battery interfaces to implement a battery back-up system.

As shown in Table V, the 5101 is capable of driving a maximum TTL load of 2mA at an output voltage V_{OL} of 0.4V. Attempting to sink more than 2mA will result in an increased V_{OL}.

LOW V_{CC} DATA RETENTION

The 5101L family of RAMs has ultra low standby current and requires only that V_{CC} be between $2.0V \leq V_{CC} \leq 5.25V$ to maintain data. As shown, these devices are guaranteed to operate in a standby mode with V_{CC} a minimum of 2.0V. Table VI gives the low V_{CC} data retention characteristics of the 5101L. The waveforms for low V_{CC} data retention operation are shown in Figure 12.

As shown in Figure 12, CE_2 must be brought low ($\leq 0.2V$) at or before the V_{CC} supply drops to 4.75V. In addition, CE_2 must remain in the low

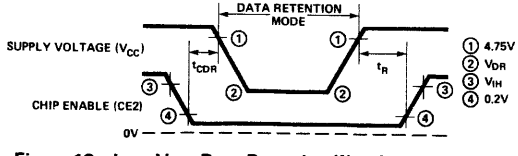


Figure 12. Low V_{CC} Data Retention Waveforms

state for a period equal to a read cycle time after V_{CC} has reached a minimum of 4.75V after power-up. It is important to note that the supply voltage V_{CC} does *not* have to be reduced below 4.75V as shown in Figure 12. Remember that the standby current I_{CCL} is a maximum of 15μA up to V_{CC} = 5.25V. The typical data retention current as a function of V_{DR} (V_{CC} in data retention mode) is shown in Figure 13.

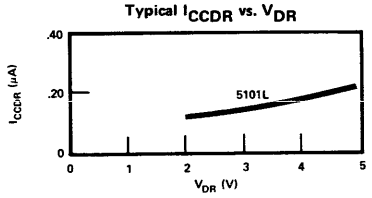


Figure 13. 5101L Data Retention Current Vs. V_{DR}

SYSTEMS CONSIDERATIONS

Since the 5101 is a completely static TTL compatible random access memory device requiring no clocks, refresh or special drivers/sense circuitry, the designer can treat the 5101 as any other TTL compatible device. Because of the ease with which the 5101 can be used, this section on Systems Considerations will concentrate on circuitry associated with battery-supported standby operation. Discussions of any interface buffers (if required) to a 5101 system will be relative to the effect these buffers have on the standby power source (e.g. battery) and what can be done to minimize the adverse effects of the buffers. Additional information regarding buffers for static TTL compatible RAMs can be found in the next section, "Designing with Intel's Static MOS RAMs".

Low Power Standby Operation

When designing a non-volatile semiconductor memory system, the basic requirements can be outlined as follows:

1. Maximum data retention time-battery back-up.
2. Maximum load current during standby-data retention mode.
3. Physical size requirement of battery.
4. Access/cycle time (operating mode).

Access time is important as it effects the selection of address and data buffers required by the system. If high speed operation is desired, it may be necessary to use series 74S type gates for the buffers. If speed is not of primary interest then CMOS type buffers may be used. Clearly, TTL type buffers will draw considerably more power than CMOS buffers if left connected to the battery supply during the data retention mode. The battery interface to both TTL and CMOS buffers will be discussed in the battery section.

The required data retention time for battery supported standby operation is of primary importance in the selection of a battery. The usual trade-offs associated with data retention time are:

1. Memory size (number of words that must be non-volatile).
2. Physical battery size desired (determines if the battery is to be placed on a printed circuit card or is external to the card).

Within reasonable constraints of memory size and data retention time, there are many types and configurations of batteries that can be used.

Power Switching

Two basic types of power switching circuits (switching between the main supply and the battery) are described which are simple and inexpensive.

These two types are:

1. Diode Coupled
2. Switch Coupled

These two types of switching circuits are shown in Figure 14. The diode coupled circuit requires the main d.c. supply to be above the required V_{CC} voltage by the amount of drop through the diode. The diode used should have a low forward drop (such as found in Germanium diodes) and low series resistance.

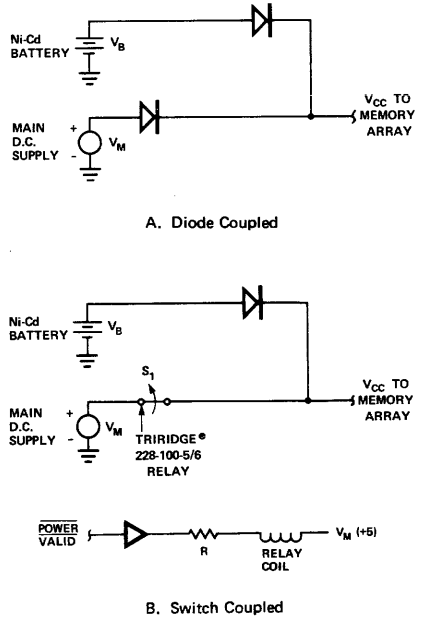


Figure 14. Power Switching Circuits

If it is not desirable to have a power supply voltage above V_{CC} (e.g. existing +5.0V supplies are to be used), then a normally open switch can be used in place of the diode. The switch is held closed by a simple TTL buffer gate as shown in Figure 14 as long as $\overline{\text{POWER VALID}}$ is held low. When power loss is detected (see Power Loss Detect Section) the switch is opened and the battery automatically supplies power to the memory array. (Note that if the memory is to be used for a short period to load memory, etc., after $\overline{\text{POWER VALID}}$ goes high a delay must be included in the switch line to take power from the supply before it drops below 4.75V).

Power Loss Detect

In memory systems which have TTL interface and other control circuitry, it is usually necessary to have advanced warning that A.C. power has been lost. This allows the orderly shut down on the system and can provide time to store data/records in the non-volatile portion of memory. Such a circuit is shown in Figure 15.

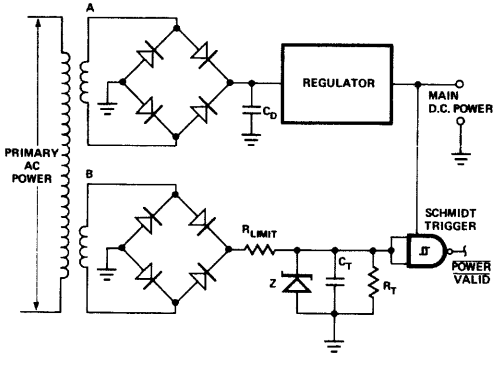


Figure 15. Power Loss Detect Circuit

The detect circuit uses a separate transformer winding (available on many power supplies) to provide a positive (≈+5V) voltage reference to a schmidt trigger. A separate winding is used so as not to interfere with the regulation of the main d.c. power source.

Operation of the detect circuit is as follows:
A high level (≈ 5V) is established at the input of a schmidt trigger (e.g. 7414) by the diode bridge network and zener Z. Resistor R_{LIMIT} is a current limiting resistor between the bridge and schmidt trigger input network. The R_T C_T combination controls the discharge rate of the input voltage to the schmidt trigger when reference power is lost. The time constant is used to prevent short (a few cycles) a.c. power loss from shutting down the system. The only restriction on the maximum value of the time constant is the $\overline{\text{POWER VALID}}$ signal must go high before the main d.c. power source drops below the minimum allowable operating voltage of the main d.c. source.

In general it is not desirable to combine the power loss detect circuitry with the main d.c. power source for two reasons:

1. Adverse effect on d.c. output regulation by R_{LIMIT} resistor, and
2. The large decoupling capacitor, C_D, on most d.c. supplies.

The large decoupling capacitor C_D will cause a time constant which is too large and may not allow sufficient time between $\overline{\text{POWER VALID}}$ going high and the main d.c. power dropping below acceptable minimums

Batteries For Non-Volatile Semiconductor Memories

The first place to begin in the selection of a battery for a particular application is to analyze those factors dictated by system requirements and fit the battery to the requirement. Some of these important criteria are:

1. Load current imposed on battery.
2. Battery voltage-full charge.
3. Battery voltage-end of life.
4. Life of battery under maximum load conditions.
5. Environment-temperature range (operating, non-operating).
6. Physical factors (size, weight).
7. Battery operation.

Of the seven criteria listed above, the one most likely to be overlooked is the effect of temperature on the capacity and life of the battery. For many batteries commerical grade temperature requirements (0°C to 70°C) may adversely effect both the capability and life of the battery.

Criteria seven, battery operation, refers to the operating schedule the battery is expected to meet. For example, if the battery is expected to maintain data *only* on a.c. power outages which are assumed to be rare, then a rechargeable battery (secondary cell) with a slow recharge rate may be selected. For this case, it may even be desirable to use a non-rechargeable battery (primary cell) with battery replacement scheduled at appropriate intervals (six months to 1 year).

However, if the system is operated in a mode where power is turned on in the morning and off in the evening then fast rechargeable batteries (with appropriate recharging circuitry) may be required.

In the evaluation of the seven criteria listed previously, one of the first things to be determined is what type of battery is to be used in the system. The chart shown in Table VII outlines the characteristics of various storage cell types. Consider first the primary type.

PRIMARY BATTERIES (NON-RECHARGEABLE)

The use of primary batteries in a memory system is usually limited to those systems which require standby data retention infrequently or where very high battery capacities (mA-hr) and very small battery physical size are required. For these cases, both mercury and silver-oxide batteries offer large capacity combined with very small phsyical size. The small size of these batteries is shown in Figure 16 for a silver-oxide battery (110mA-hr).

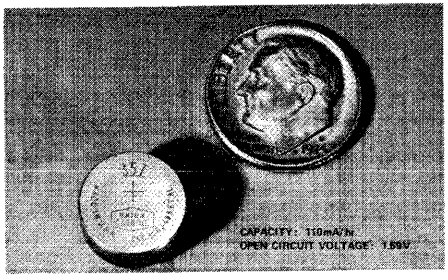


Figure 16. Silver-Oxide Button Cell

Typical voltage discharge curves for silver-oxide and mercury batteries are shown in Figures 17 and 18 respectively. Note that in both cells, the cell voltage remains nearly constant during discharge — a highly desirable characteristic. In addition, the mercury cell generally has greater capacity for a given size as compared with a silver-oxide battery.

Carbon-zinc batteries offer the lowest cost of any primary battery described, but suffer from a severe degradation of output voltage as a function of use. This characteristic makes carbon-zinc batteries undesirable for most standby power applications.

Alkaline batteries have a much better discharge characteristic than carbon-zinc, but are not quite as

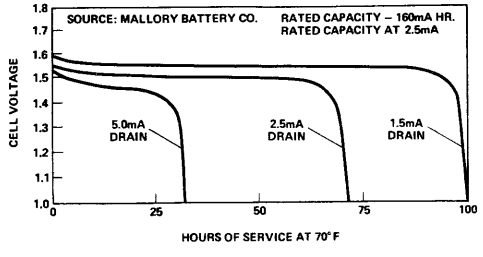


Figure 17. Silver-Oxide Cell Typical Voltage Discharge Characteristics

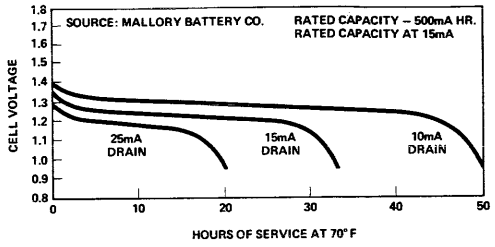


Figure 18. Mercury Cell Typical Voltage Discharge Characteristics

good as mercury or silver-oxide. The relative low cost of these batteries can make them attractive for use in some systems applications.

Both carbon-zinc and alkaline batteries are discussed in detail in the Eveready Battery Applications Engineering Data handbook (see Bibliography 3). It is emphasized that adequate attention should be directed to the output voltage characteristics of these two batteries before using them in a standby power application.

Because of printed circuit board area limitations small battery size is usually the reason for selecting a primary cell for battery support. In this case, it may be desirable to limit the number of cells in a particular system to one. However, this requires that a voltage boost circuit be used in the system to achieve a minimum sustaining voltage of 2.0V at end of battery life to operate the 5101. Such a boost circuit is shown in Figure 19.

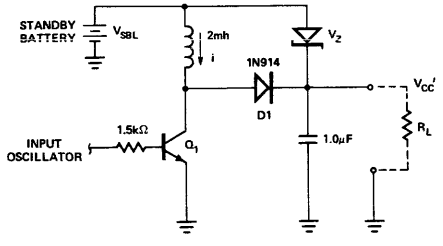


Figure 19. Basic Voltage Boost Circuit

Voltage Boost

Operation of the voltage boost circuit is as follows:

The input to Q_1 is a low duty-cycle signal. This signal turns Q_1 on forcing current through inductor L. When Q_1 is turned off, current i cannot change instantaneously and is diverted through diode D,

Table VII. Battery Characteristics

I. PRIMARY TYPE (NON-RECHARGEABLE)[1]

Cell Construction	Cell Voltage (Typ.)[2]	Comments
Carbon-Zinc (Leclanche)	1.5	Lowest cost; discharge characteristics may be inadequate for some systems
Silver-Oxide	~ 1.6	Good for low temperature operation, discharge characteristic excellent for most system requirements
Mercury	1.4	Good for high temperature operation, discharge characteristic excellent for most systems, long shelf life
Alkaline	1.5	Good efficiency for use with systems requiring total battery operation

II. SECONDARY TYPE (RECHARGEABLE)

Cell Construction	Cell Voltage (Typ.)	Comments
Nickel-Cadmium	1.2	Excellent all around characteristics for battery back-up, widely used
Lead-Calcium	2.0	Excellent all around characteristics for battery back-up

[1] Some information in this table condensed from "EVEREADY" Battery Applications and Engineering Data Handbook copyrighted 1971 by Union Carbide Corporation.

[2] Cells can be put in series to obtain multiples of basic cell voltage.

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charging capacitor C. The voltage to which C charges is a function of the capacitance C, load R_L and zener V_Z.

In order to minimize the load on the battery and to maximize the efficiency of the boost circuit, it is necessary to turn on Q_1 only for the minimum amount of time which will still maintain the desired output standby voltage. Such a circuit is useful only if there is a way to power the input oscillator required for Q_1 off the same battery V_{SB}. Such a circuit is shown in Figure 20. The 5801, shown in Figure 20, is a low voltage CMOS oscillator made by Intel (used extensively by Microma, an Intel subsidiary). The output of this oscillator triggers a CMOS single-shot which in turn drives the voltage boost circuit shown in Figure 19. Note that the 5801 is powered by the battery (Cell voltage = 1.5V) and the 4047 (CMOS single-shot) is powered by the boosted V_{CC}'. It is, therefore, necessary to assure that the standby voltage V_{CC} does not fall below 3V (minimum 4047 operating voltage) before starting the oscillator circuit. A power loss detect circuit can be used to warn of an impending power down condition and allow the boost circuit to be turned on in time to hold the V_{CC} voltage to $\cong$3V.

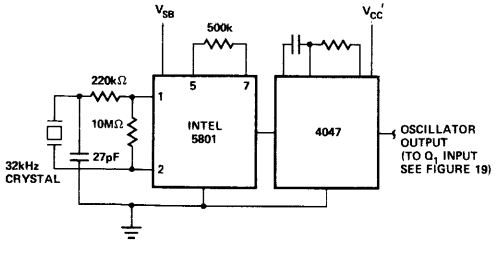


Figure 20. Voltage Boost Oscillator Circuit

As stated previously, the power conversion efficiency of the oscillator and voltage boost circuits should be maximized to minimize the current drain on the battery. The efficiency of these circuits is largely a function of the duty cycle of the oscillator. Figure 21 shows the waveforms of the input signal to the voltage boost circuit and the current i through inductor L. A summary of the data in Figure 21 is shown in the graphs of Figure 22. Note that the curve of V_{CC}' levels out at 4.0V, this is the result of the clamp zener V_Z (Figure 19). Also note that the efficiency is markedly decreased as the input pulse to Q_1 is lengthened. For a given duty cycle on Q_1, the efficiency of the voltage boost circuit will increase if the load current is reduced.

SECONDARY BATTERIES (RECHARGEABLE)

As outlined in Table VII there are two basic types of rechargeable batteries ideally suited for memory system standby power-down operation. Nickel-Cadmium (Ni-Cd) and Lead-Calcium (such as Gel/Cell®). This section will outline some of the salient features of each type. No attempt will be made to compare the two for general operation. It is recommended that the system designer interface directly with the battery manufacturer to obtain guaranteed specification data, operating limitations and safety precautions (if any).

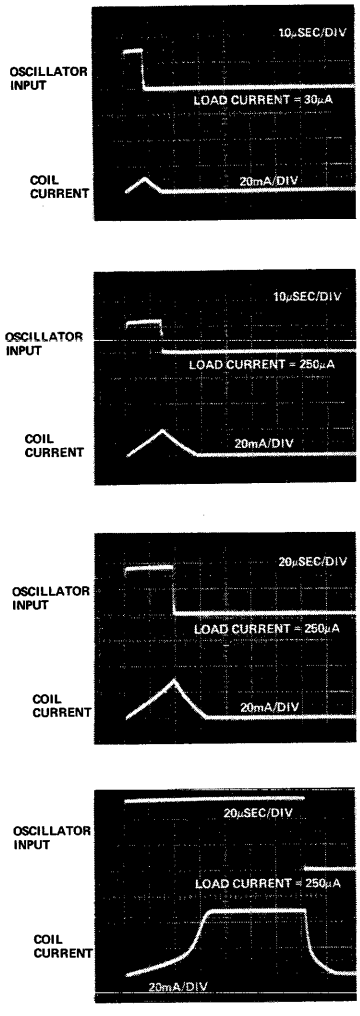


Figure 21. Voltage Boost Waveforms

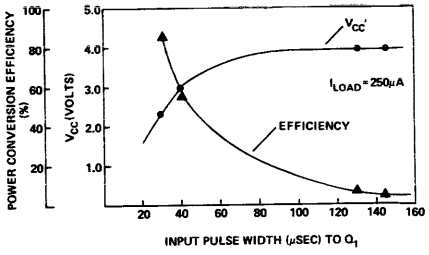


Figure 22. Boost Circuit Output Voltage and Efficiency Vs. Input Pulse Width

Photograph courtesy of General Electric Co.

Figure 23. Sizes of Selected Cylindrical Ni-Cd Batteries

RAMs

Nickel-Cadmium

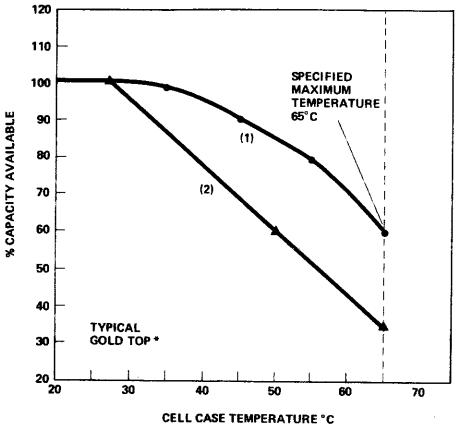
Nickel-Cadmium batteries are available in a wide variety of capacities (mA-hr) sizes and styles (see Figure 23). The styles include button, cylindrical and rectangular cells and may be placed on the memory printed circuit card or in the same enclosure as the main d.c. power supply. (Enclosing the batteries in with the main d.c. supply is usually done only in large back-up capacity systems.)

There are many manufacturers of Ni-Cd batteries who can supply the desired battery configuration. A useful place to begin looking for a battery supplier is Electronic Buyers Guide (McGraw-Hill publications.) (Also see bibliography.)

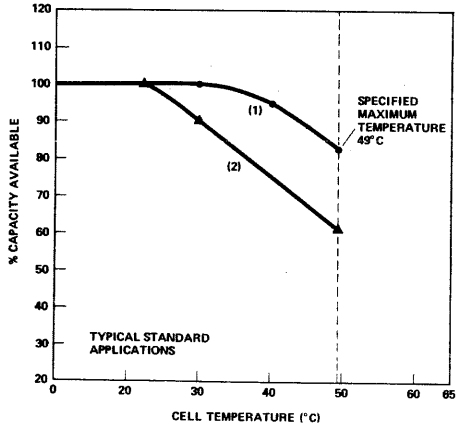
Electrical Characteristics

Electrical characteristics such as capacity (mA-hr) and cell voltage as a function of discharge rate for Ni-Cd batteries are temperature dependent. It is important for the designer to realize that high system operating temperatures may have an adverse effect on battery life and capacitance even though the battery is not expected to be called on to provide standby power at those temperatures.

An example of the effect of temperature on capacity (based on GE battery specifications) is shown in Figure 24 for two types of General Electric Ni-Cd batteries. Note that two types of usage are given: one for infrequent discharge with extended periods



* GOLD TOP IS A REGISTERED TRADEMARK OF GENERAL ELECTRIC.



NOTES:
(1) INFREQUENT DISCHARGE, EXTENDED PERIOD OF OVERCHARGE.
(2) FREQUENT DISCHARGE.

Figure 24. Ni-Cd Battery Capacity as a Function of Temperature

of overcharging, condition (1), the other for frequent discharge, condition (2). In most memory applications condition (1) will apply, which is the condition for maximum capacity as a function of temperature.

Ni-Cd batteries also have a self discharge characteristic which is a function of temperature. One result of this characteristic is that these types of batteries should not be stored in a charged condition for an appreciable length of time. Therefore, before inserting these batteries into a system or after the system has been powered down for an extended time (i.e. no trickle charge available and batteries disconnected from load) care must be exercised to assure that the batteries have sufficient charge to perform in a power down standby mode. In addition, when calculating the capacity of the battery for a particular load, the self discharge characteristic of the battery must be included. This self discharge rate can be as high as approximately 7%/day loss of capacity at 50°C to an average of 1%/day at room temperature (25°C) for Ni-Cd batteries.

The discharge characteristics of Ni-Cd batteries are flat, making them ideal for use in memory systems requiring standby power. The general shape of such characteristics is shown in Figure 25. Note that no scales are given in this figure because the output voltage as a function of time varies between manufacturers of Ni-Cd batteries. The curves are shown to demonstrate the flat voltage characteristics at end of battery capacity for Ni-Cd batteries.

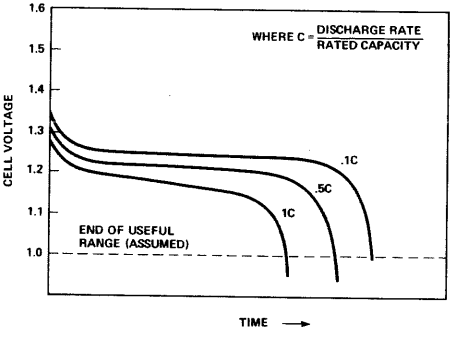
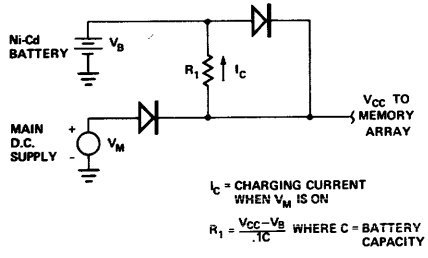


Figure 25. Ni-Cd Voltage Discharge Characteristic

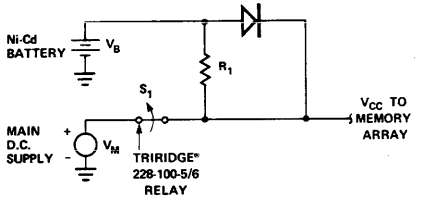
Since the single cell voltage of a Ni-Cd battery is approximately 1.2 volts (as shown in Figure 25), it is necessary to boost the voltage with external circuitry (discussed previously) or stack the cells in series to obtain the proper operating voltage for the 5101L. If it is desired to stack the cells in series to obtain a higher voltage, care should be exercised to assure that the cells are reasonably matched. Cells which are not matched can cause problems during charging when placed more than three in series. Most manufacturers will provide Ni-Cd stacks of the desired size which should be adequately matched to avoid any charging problems. It is important to discuss this phenomonon with the battery manufacturer if several Ni-Cd batteries are to be used in series.

Trickle Charge Nickel-Cadmium

Ni-Cd batteries used as standby support power for memory systems should be provided with a continuous charging current from the main power source. This assures that the self discharge characteristic of the battery does not deplete battery capacity. The trickle charge current should be a constant current at a rate of one-tenth the total battery capacity (e.g. a 400mA-hr Ni-Cd should be trickle charged with 40mA current). A simple trickle charger is shown in Figure 26. If the system is to be operated at high temperature, care should be taken to assure that the maximum battery cell temperature is not exceeded during charging.



A. Diode Coupled



B. Switch Coupled

Figure 26. Ni-Cd Trickle Charger

Fast Charge Nickel-Cadmium

Some Ni-Cds can be charged at a much faster rate than that described above. However, the charging current must be monitored and reduced to trickle charge when the battery is fully charged. Failure to properly handle the charging of Ni-Cd batteries can present safety problems. The manufacturer should be consulted for recommended fast charge techniques.

Lead-Calcium

Lead-calcium batteries are also ideally suited for use as a standby power source for semiconductor memories. A popular brand of lead-calcium cell is the Gel/Cell® made by Globe Battery (Gel/Cell® is a registered trademark of Globe-Union). These types of batteries have several highly desirable characteristics such as:

1. Small size-to-capacity ratio.
2. Low standby self-discharge characteristics.
3. Flat operating discharge characteristics.
4. No permanent cell reversal.
5. Good operating temperature range.

Several manufacturers supply lead-calcium type batteries. However, for the purpose of this application note only the characteristics of the Gel/Cell® will be discussed.

Gel/Cell® Characteristics

A small Gel/Cell® battery is shown in Figure 27. The nominal cell voltage of this type of battery is 2.0 volts (the capacity of the battery shown is 1 amp-hr). This battery is ideal for use in those systems having a relatively high discharge load (~1mA). The output discharge characteristics are shown in Figure 28.

Photograph courtesy of Globe Battery.

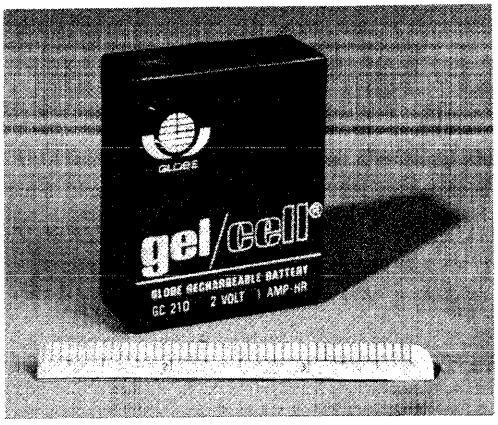
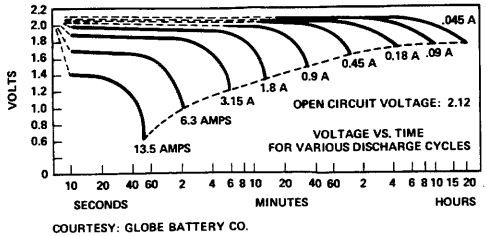


Figure 27. Gel/Cell® Lead-Calcium Battery



COURTESY: GLOBE BATTERY CO.

Figure 28. Gel/Cell® Voltage Discharge Characteristics

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Note that the minimum discharge rate shown in Figure 28 is a hefty 45mA. At this rate the battery can supply power for 20 hours. At the rate of 1mA, this battery will last 1000 hours or approximately 6 weeks. Lower discharge rates will of course increase the battery life time proportionally.

These types of batteries are optimally used in systems having a large current drain. Although the batteries are indeed very small for a given capacity, the cell voltage is a nominal 2.0 volts which is the minimum acceptable for maintaining data in the 5101L. Therefore, either two batteries are required (series connection) or the voltage boost circuit described earlier must be used. In those systems having very small current drains in standby, the addition of a second battery will most likely take up too much room on the p.c. board. For these systems other types of batteries are recommended (such as Ni-Cd, Mercury, etc.).

Capacity of a Gel/Cell® as a function of temperature is shown in Figure 29. As is shown in this figure, at low temperatures the battery loses a great deal of capacity. Therefore, when designing systems using this type of battery, proper attention will have to be paid to the environmental temperature extremes expected in the system and proper battery selection made.

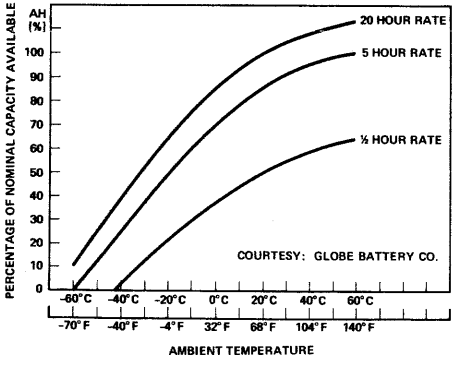

Figure 29. Gel/Cell® Capacity Vs. Temperature

Trickle Charge Lead-Calcium

Unlike Ni-Cd batteries, which accept a constant current trickle charge, the lead-calcium battery is trickle charged by a constant voltage source. The voltage required is 2.25 to 2.30 volts per cell. At this voltage, referred to as the float voltage, a Gel/Cell® will accept only the amount of charge necessary to maintain capacity.

The implementation of a trickle charger for lead-calcium batteries in a system is not as straight forward as for Ni-Cd batteries. A simple charger is shown in Figure 30. In this figure, the "float" voltage is maintained by zener Z, and potentiometer P. The potentiometer is used to adjust the voltage at node (1) to the proper level (2.25 to 2.30 volts per cell). Most zeners are accurate to no more than ±5% which is not adequate for the desired "float" voltage. Diodes D_1 and D_2 isolate the battery and power supply from each other.

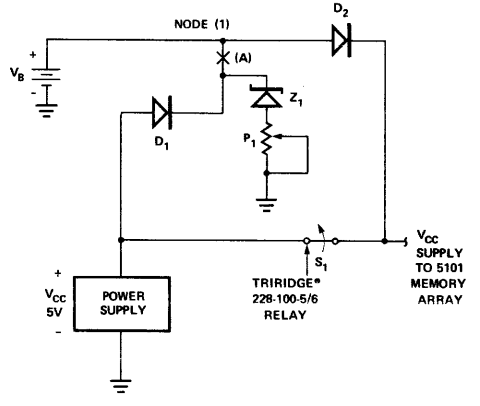

Figure 30. Lead-Calcium Trickle Charger

It is important to select a very low leakage zener (Z_1) to minimize the parasitic load on the battery during power down operations. Indeed, it may be desirable to insert a normally open switch at location (A), Figure 30, to disconnect the zener from the battery during standby operation. The switch would be controlled identically to S_1, as shown in Figure 30.

It is clear from the example given that providing a trickle charge to a lead-calcium battery and having the battery ready for instantaneous operation is more complicated than for Ni-Cd batteries. Other charging methods are available (see bibliography 4) but they all require that the battery and system voltage be identical and in 2 volt increments. Since operation of the 5101 is $4.75 \leqslant V_{CC} \leqslant 5.25$ and standby operation is $2.0 \leqslant V_{CC} \leqslant 5.25$, the charger/supply combinations described in the reference have limited value for the present applications.

Summary: Lead-Calcium

Lead-calcium batteries are particularly useful with those systems which have a relatively high standby discharge rate (greater than 1mA). The high energy density of these batteries also lend themselves to providing power in normal operation (taking into account V_{CC} requirements of the 5101L) of some systems.

The primary disadvantage of lead-calcium cells is the relative complexity of supplying a trickle charge to the batteries in those systems where the standby voltage is lower than the operating supply voltage V_{CC}.

System Implementation

The 5101 is an extremely easy to use static RAM. No refresh timing is required, only one power supply (+5V) is needed, and the device is fully TTL compatible. In addition, current transients on the V_{CC} (+5V) pin are minimal and require no special decoupling techniques. Therefore, this section will concentrate on interface techniques to the 5101 in order to minimize the power in power down/standby applications.

1K X 16 MEMORY SYSTEM

The discussion on interface techniques to the 5101 is illustrated with a 1024 word X 16 bit system shown in Figure 33. The memory array is configured as shown in Figure 33. Note that for a read/write access one of four columns is enabled by one CE_2 (CE_2A, CE_2B, CE_2C, CE_2D). The other chip enable ($\overline{CE}_1$) and the output disable pin are tied to ground to simplify the layout. All corresponding addresses are bused together and driven by one buffer as are the read/write inputs. Data in and data out pins are OR tied along a given row. Access is then simply a matter of providing the correct address (A_0-A_7), selecting a read or write function and enabling the proper row. Two simple methods for providing the proper CE_2 signals are shown in Figure 31.

TTL Interface

Interface circuits shown in Figure 33 can be implemented with either CMOS or TTL devices. If access/cycle time of the memory system is to be minimized, then series 74 or 74S type TTL can be used. However, for power down operations where a battery is used for back-up power the V_{CC} (+5V) supply to these TTL devices must be independent of the V_{CC} supply to the memory array. This is most easily accomplished by a slight modification to the power supply diagram shown in Figures 26 and 30 as modified in Figure 32. As shown, when the main supply V_m goes off, switch S_1 is opened (isolating V_m from the memory devices).

The state of the addresses, read/write, $\overline{CE}_1$, output disable and data-in to the 5101 memory array are in a "don't care" condition for standby/power down operation. Only CE_2 is required to be low ($\leq$0.2V) for the low power state. For CE_2 TTL interface drivers, a resistor to ground is required to maintain CE_2 at the proper level when power is removed from the series 74/74S gates. The resistor value required is calculated by considering two requirements:

1. CE_2 high ($V_{IH} \geq$2.2V) during operation.
2. CE_2 low ($V_{IL} \leq$0.2V) during standby/power down.

The first requirement above is determined by the maximum source current capability of the TTL drivers (I_{OH}) allowed which guarantees the proper high level output. Requirement 2 above is a function of the maximum leakage on the CE_2 line from the four 5101 devices driven by the CE_2 line. The range of values for the pull down resistor is 6.2kΩ $\leq R \leq$50kΩ for Series 74 drivers.

The POWER VALID input signal (shown in Figure 33) is derived from a power loss detect circuit. The power loss detect circuit should be able to detect a power loss before the output V_{CC} falls below 4.75V (lowest guaranteed operating power level for TTL circuits). A power loss detect circuit to implement the POWER VALID signal is discussed in the POWER LOSS DETECT section.

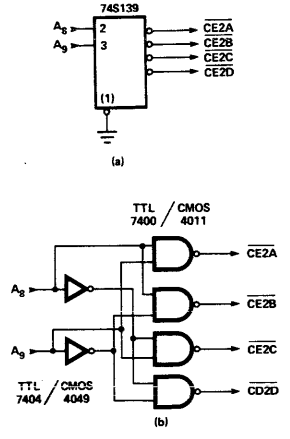

Figure 31. Chip Enable Generators 1K X 16 Memory

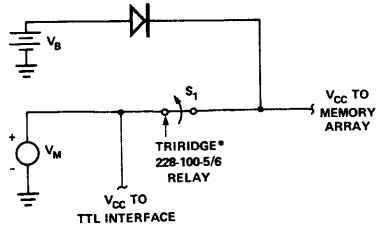

Figure 32. Power Distribution for TTL and CMOS Interface

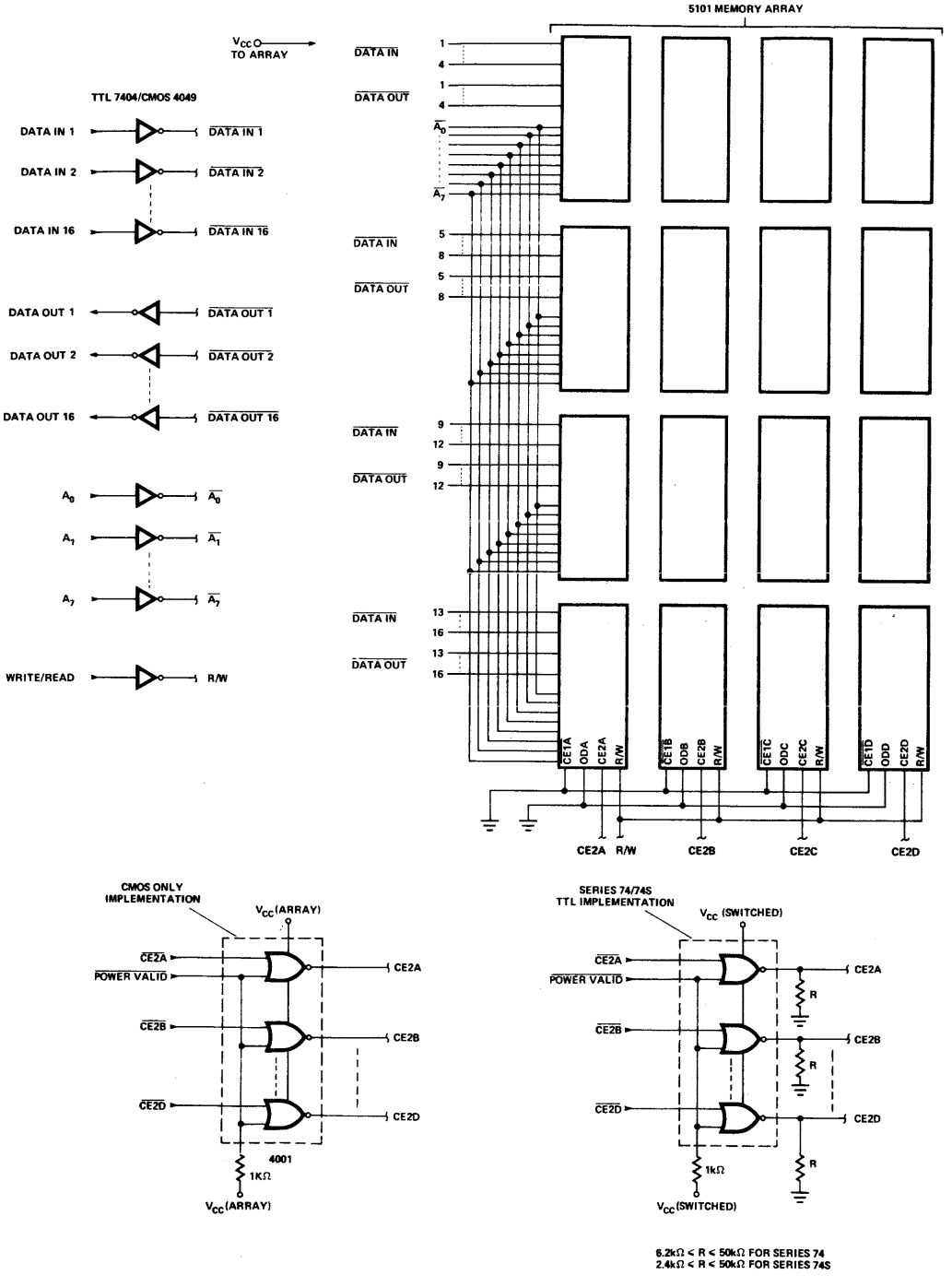

Figure 13. 1K X 16 5101 Memory System

CMOS Interface

Using CMOS circuits to interface to the 5101 memory array eliminates the need of switching out V_{CC} to the interface during power down/standby. The ultra low power CMOS interface will dissipate approximately the same power as the memory array (assuming 1K X 16) and can easily be handled by the back-up battery.

Photos of CMOS waveforms driving the 1K X 16 5101 memory array are shown in Figure 34. Also included in the photo is the noise generated on the V_{CC} supply during operation. As is shown, noise on the power line is virtually non-existent.

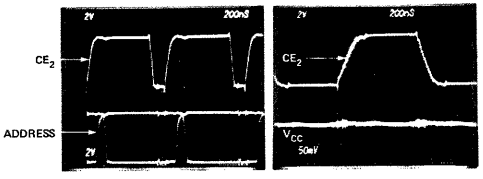

Figure 34. CMOS Interface Driver Waveforms

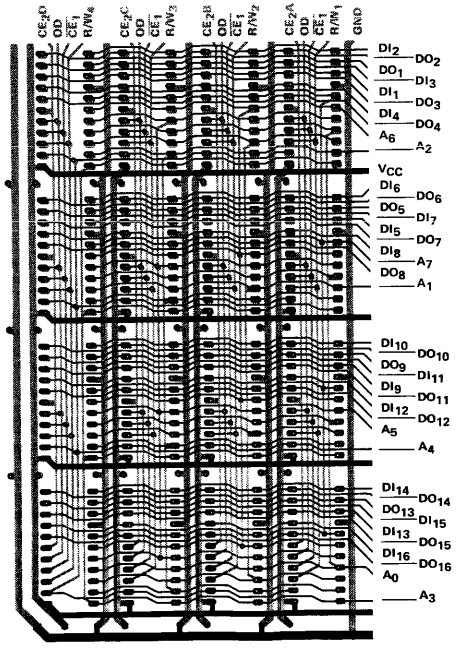

Figure 35. 5101 1K X 16 Array Layout

1K X 16 MEMORY ARRAY LAYOUT AND CARD ASSEMBLY

The layout used on the 5101 1K X 16 system described previously is shown in Figure 35. Note that V_{CC} and ground are distributed in a grided matrix and decoupled as shown. More decoupling was used in this system than is ordinarily required so the designer can use his own judgement in this regard.

The 1K X 16 memory card used was configured per the diagram in Figure 36. Notice that the card is completely self contained for standby/power down operation with the battery included on the card. With this configuration the card can be unplugged, transported to another location (with data being maintained by batteries) and operation resumed.

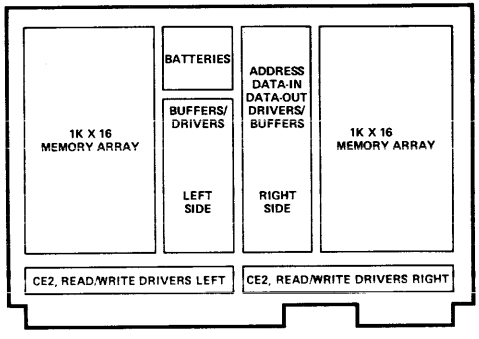

Figure 36. Dual 1K X 16 5101 Memory Card

5101 ORGANIZATION ADVANTAGES

The organization of the 5101 as 256 words X 4 bits has distinct advantages over memory devices organized as 1024 words X 1 bit in many systems applications. These applications include terminals, CRT displays, microprocessors and others which have most (or at least a portion) of their memory expandable in 256 or 512 word increments. For these cases, the number of devices required for a 256 X 4 memory device is much smaller than for a 1024 X 1 memory device.

SUMMARY

There are many selections of 5101 256 word X 4 bit devices available. Table VIII is the product selection guide for this family of devices. As shown, the designer has a wide range of choices in selecting the device most suited to his particular requirements.

Table VIII. 5101 Product Selection Guide

PART NUMBER	STANDBY CURRENT NA/BIT	+2V POWER DOWN OPTION	ACCESS TIME (NS)
5101-1	15	No	450
5101L-1	15	Yes	450
5101-2	200	No	450
5101L-2	200	Yes	450
5101	15	No	650
5101L	15	Yes	650
5101-3	200	No	650
5101L-3	200	Yes	650
5101-8	500	No	800
*M5101-4	200	No	800
*M5101L-4	200	Yes	800
*M5101-5	1000	No	800
*M5101L-5	1000	Yes	800

*Temp Range −55 to +125°C

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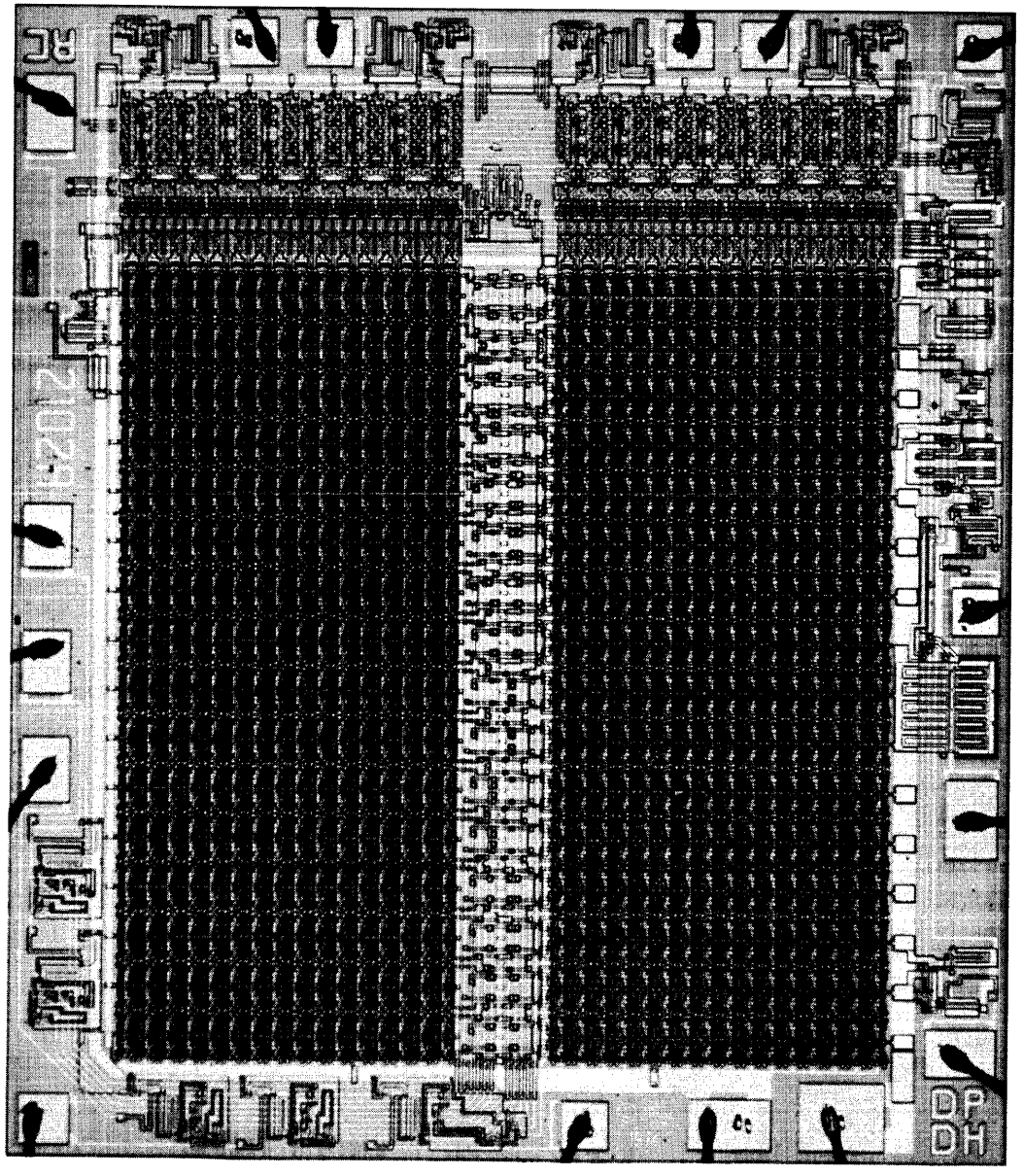
Designing with Intel's Static MOS RAMs

Jim Oliphant
Application Engineering

Contents



Photomicrograph of 1024 Word x 1Bit 2102A Static MOS RAM

INTRODUCTION

Intel's introduction of reliable, low cost, static, high-density MOS RAMs has done much to stimulate the use of semiconductor memory in new and unique applications. These RAMs, which do not require special refresh or timing circuitry, are used with as much ease as the standard TTL gates.

The Intel family of static high-density MOS RAMs, shown in Table I, offers the system designer flexibility in memory configuration, speed and ease of use. The devices in this family are directly TTL compatible in all respects: inputs, output(s) and power supply. Internal circuits are designed for full DC stability requiring no clocks or refreshing to operate. These static RAMs are manufactured with Intel's reliability proven N-channel silicon gate and CMOS silicon gate process.

The purpose of this application note is to outline the internal operation of these static RAMs, how they are used, and to present system design considerations in their use. In addition, suggested layout configurations for larger memory systems and techniques for reducing power dissipation during standby will be discussed.

DEVICE DESCRIPTIONS

As shown in Table I, there are two data organizations in the Intel static RAM family—1024 words x 1 bit and 256 words x 4 bits. The memory devices organized as 256 words x 4 bits are available with separate data input and output pins with an output disable pin (22 pin DIP), combined input/output pins with an output disable pin (18 pin DIP), and combined input/output with no output disable pin (16 pin DIP).

The sections on Device Operation detailed below describe the internal circuits which are common to both the 1024 word x 1 bit devices and the 256 word x 4 bit devices. The operational differences between the devices in the static RAM family are limited to the logic state and timing of chip enable(s) and data I/O lines and are discussed separately under the heading for each device type.

General Device Operation

Each of the Intel N-channel static RAMs utilize a DC stable six transistor cell configuration for the storage medium. The storage cells are arranged in a 32 x 32 matrix as shown in Figure 1. Data selection on the 1024 x 1 devices is accomplished by the coincidence of a row select (A_0–A_4, 1 of 32) and column select (A_5–A_9, 1 of 32). For the four bit wide configured RAMs, the selection is made by a row select (A_0–A_4, 1 of 32) and four column selects (A_5–A_7, 4 of 32). The data contained in the selected cell(s) is sensed, buffered, and presented to the data out pin D_0. In all devices the polarity of data read from memory is the same polarity as the data written into memory.

Storage Cell Operation

The two types of storage cells used in the Intel static RAM family are shown in Figure 2A and 2B. Static RAMs suffixed by "A" (e.g., 2102A) utilize

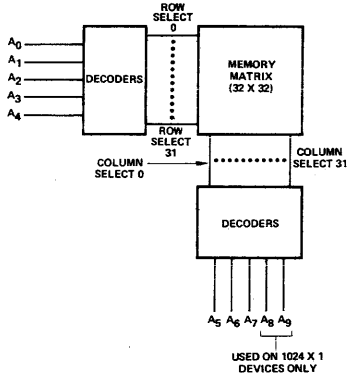


Figure 1. Simplified Memory Block Diagram

Table I. Intel Static MOS RAM Family

INTEL PART NUMBER	CONFIGURATION (WORDS X BITS)	DATA INPUT/OUTPUT	OUTPUT DISABLE	NUMBER CHIP ENABLES	POWER DOWN CAPABILITY	NUMBER PACKAGE PINS
2101A	1024 X 1	SEPARATE	N/A	1	NO	16
2102AL	1024 X 1	SEPARATE	N/A	1	YES	16
2101A	256 X 4	SEPARATE	YES	2	NO	22
2111A	256 X 4	COMMON	YES	2	NO	18
2112A	256 X 4	COMMON	NO	1	NO	16
5101(1)	256 X 4	SEPARATE	YES	2	YES*	22

*Extremely low standby current at 15.4 ua total.
(1) (CMOS)

depletion mode load devices, which are normally "on" (Fig. 2B). (Earlier product designated without the "A" suffix (e.g., 2102, 2101, etc.) utilize enhancement mode load devices which are normally "off" [Fig. 2A].) The basic operation of these two types of cells is similar in the manner in which data is written, stored, and retrieved. The differences between these cells will be discussed later.

Consider the storage cell shown in Figure 2A. Data is stored as a charge on the gate of either Q_3 or Q_4 (which determines the logic state of the cell). The voltage on the charged node is approximately $V_{CC} - V_{TH}$ (where V_{TH} is the effective threshold of the load devices) and turns Q_3 or Q_4 on. By definition a logic "0" is stored in the cell if Q_3 is on and a logic "1" is stored if Q_4 is on. If it is assumed that Q_3 is on (logic "0" stored) then current will flow from the load on Q_3 (device Q_2) through Q_3 to ground (V_{SS}). This current will cause the voltage at node (1) to assume a value near V_{SS} (the voltage is proportional to the effective on resistance of Q_2 and Q_3). The resultant low voltage on node (1) turns device Q_4 off. Device Q_5 maintains the charge on the gate of Q_3 by replacing charge leaked off through the high impedance parasitic leakage resistor $R_{LEAKAGE}$. (This leakage is typically in the picoampere range.) The storage cell will remain in this logic state until an external forcing function is applied (write cycle).

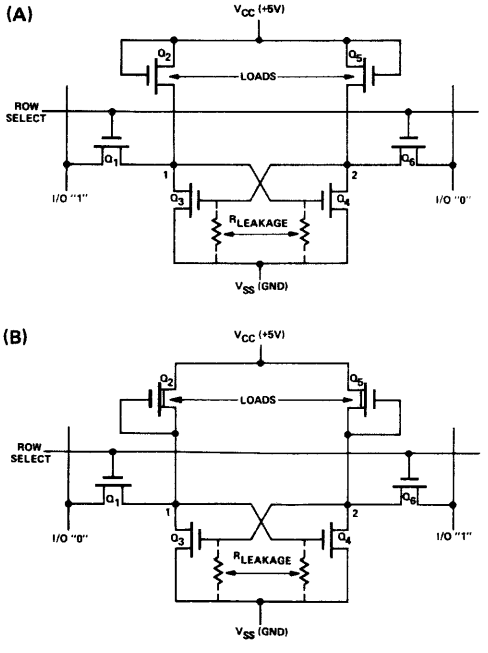


Figure 2. Storage Cell

Operation of the storage cell shown in Figure 2B is similar to that described above except for the implementation of the load device. A brief discussion of differences between enhancement and depletion type devices will aid the understanding of the storage cell operation.

A depletion type MOS device has a channel implanted between the source and drain (see Fig. 3). The effect of this conducting channel is to shift the threshold of a standard enhancement device such that it is on at lower gate voltages. The basic operation of these two types of devices can be summarized as follows for N-channel technology: An enhancement mode device requires a positive gate voltage (relative to the source) to turn the device on. A depletion mode device requires a negative gate voltage (relative to source) to turn it off. These two conditions are shown in Figure 3.

(The actual threshold of the depletion mode device can be controlled by the degree of channel doping used in the fabrication process.)

Operation of the storage cell is as follows: assume the gate of Q_3 is high turning Q_3 on causing current to flow in Q_3 and Q_2. Since devices Q_2 and Q_3 are ratioed (that is, Q_2 has a higher impedance than Q_3) the voltage at node 1 will drop close to V_{SS}. Note that the gate of Q_2 is tied to node 1; therefore as node 1 decreases in voltage, the voltage drive on Q_2 is reduced, making the effective impedance of Q_2 higher. This allows the voltage at node 1 to move even closer to V_{SS}.

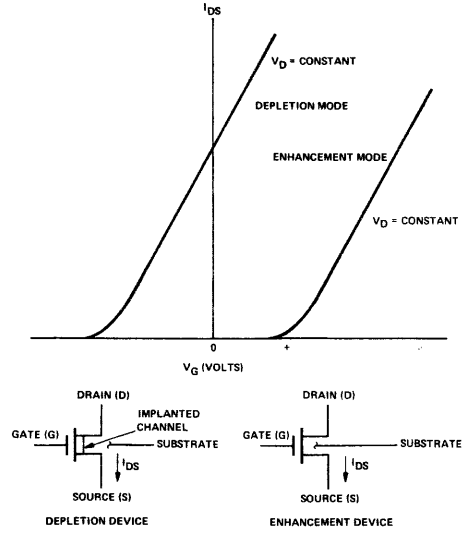


Figure 3. Enhancement/Depletion Characteristics

Since node 1 is low and is tied to the gate of Q_4, device Q_4 is off. The charge on Q_3 is maintained by the load device Q_5. Note that only leakage currents flow through device Q_5 which has a minimal effect on the voltage at node 2. Since increased positive voltage at node 2 increases the voltage drive on Q_5, device Q_5 turns on hard. The voltage at node 2 is therefore equal to V_{CC} (note that there is no threshold drop across device Q_5 since it is a depletion mode device).

Accessing the Storage Cell

The storage cell is interrogated for a read or write operation by activating the proper row select line which turns devices Q_1 and Q_6 on (Fig. 2A, 2B). For a read operation, a sense amplifier (see Fig. 4) connected to both the I/O "0" and I/O "1" outputs of each column detects the state of the selected storage cell in that column. If Q_3 is on (logic "0") then current will flow in the I/O "0" line. If Q_4 is on (logic "1"), current will flow in the I/O "1" line. A write buffer (Fig. 4) places a high level ($\sim V_{CC}$) on the I/O "0" line to write a logic "0", and a high level on the I/O "1" to write a logic "1". For both write conditions, the opposite line is held low (V_{SS}).

As is shown in Figure 4, there are internal data-in/data-out buses. Data is gated to/from the appropriate columns by column select. Note that chip enable(s) gate the output data to a three state buffer and then to the output pin. Therefore, if a chip is not selected, the output pin goes to a high impedance state (allowing the output pins to be OR tied).

Address Buffers/Decoders

Typical address buffers and decoders, for the static RAM family are shown in Figures 5 and 6 respectively. As is shown in these figures, the address buffers and decoders are static requiring no precharging for operation. The buffers/decoders respond to changes on the address lines and do not latch the input addresses. Therefore, in those systems where the address lines are not stable throughout the cycle, it may be necessary to buffer them with external latches. An example of such a system is discussed later.

It should be noted however that in many systems requiring memory the addition of external address latches is not required. This is particularly true of microprocessor systems.

2102A OPERATION

As discussed before, the 2102A device is organized as 1024 words x 1 bit having separate data-in/data-out pins. The memory is organized internally in a 32 row by 32 column matrix as shown in Figure 7. The pin configuration and logic symbol are shown in Figure 8.

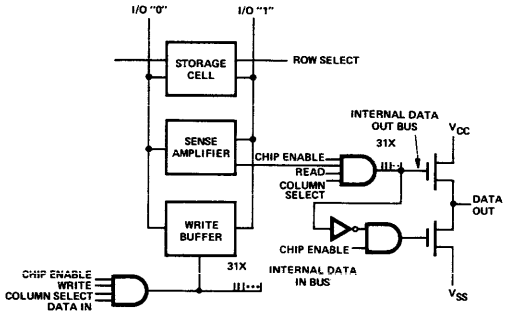


Figure 4. Internal Data Path

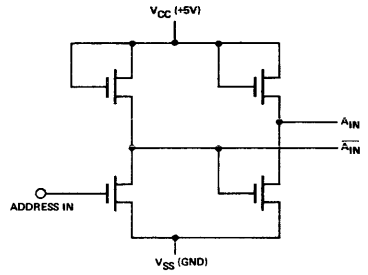


Figure 5. Address Input Buffer

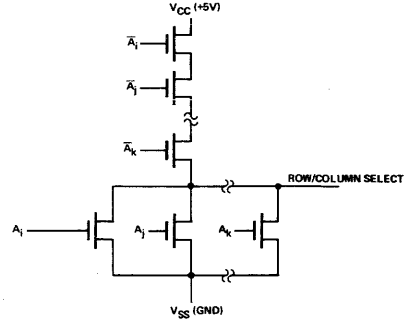


Figure 6. Address Decoder

There are only two control inputs to the 2102A: Read/write and chip enable. For unselected devices (chip enable high), the data-in input is electrically disconnected from the input data bus internal to the 2102A and the data-out buffer goes to a high impedance state. The addresses, however, are buffered and decoded (generating an internal row/column select) independent of chip enable.

BLOCK DIAGRAM

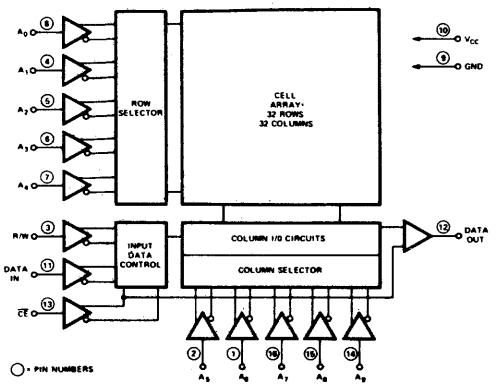
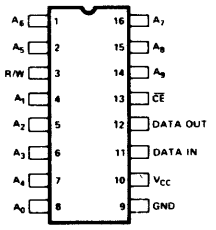


Figure 7. 2102A Block Diagram

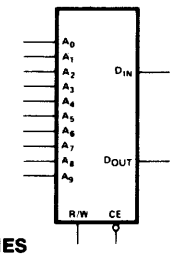
PIN CONFIGURATION

2102A



LOGIC SYMBOL

2102A



PIN NAMES

D_{IN}	DATA INPUT	$\overline{CE}$	CHIP ENABLE
$A_0 - A_9$	ADDRESS INPUTS	D_{OUT}	DATA OUTPUT
R/W	READ/WRITE INPUT	V_{CC}	POWER (+5V)

Figure 8. 2102A Pin Configuration, Logic Symbol

Read Cycle

Basic read cycle timing is shown in Figure 9. Note that although chip enable is shown as a pulse occurring after the address changes, there is no specified time at which it must occur (either before or after address change). It is therefore permissible to tie the chip enable input low if the data-out pin is not OR tied with other outputs and operate the memory device with only the read/write line and address inputs.

For example, if a series of read cycles are to be performed (such as for CRT displays), and the data-out pin is not OR-tied with another output, chip enable may be held low and the addresses may be cycled in any order to access data. During this time, however, the read/write input must always be in the high state. For this case, output data will be valid at T_A as shown in Figure 9 and specified in Table II.

A second method may be used to read data from the memory. If the addresses are set up before a read decision can be made, then chip enable may be brought low at the read decision time. Output data will be valid at t_{CO} (Table II) for this condition.

Write Cycle

Basic timing for a write cycle is shown in Figure 10. In the write cycle it is *not* permissible to perform a series of write cycles by holding chip enable and read/write low and cycling through the desired addresses. However, chip enable can be held low for continuous writes if the read/write input is timed per Figure 10. For the 2102A, a minimum write to address set up time, t_{AW}, must be observed per Table III. The minimum data hold time, t_{DH}, beyond read/write is 0 ns.

READ CYCLE

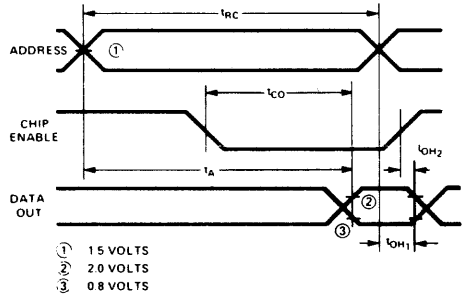


Figure 9. 2102A Read Cycle

WRITE CYCLE

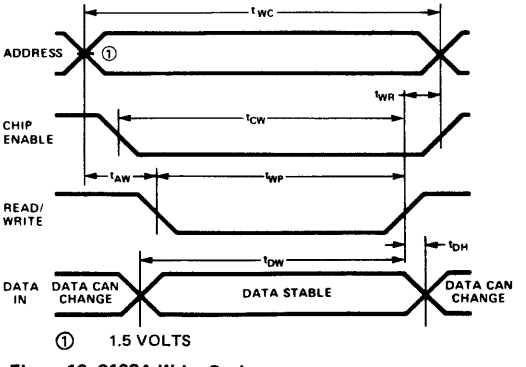


Figure 10. 2102A Write Cycle

Table II. 2102A Read Timing

READ CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit
t_{RC}	Read Cycle	350			ns
t_A	Access Time			350	ns
t_{CO}	Chip Enable to Output Time			180	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40			ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0			ns

Table III. 2102A Write Timing

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit
t_{WC}	Write Cycle	350			ns
t_{AW}	Address to Write Setup Time	20			ns
t_{WP}	Write Pulse Width	250			ns
t_{WR}	Write Recovery Time	0			ns
t_{DW}	Data Setup Time	250			ns
t_{DH}	Data Hold Time	0			ns
t_{CW}	Chip Enable to Write Setup Time	250			ns

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

Note that the minimum write cycle may be obtained by using the minimum times associated with t_{AW}, t_{WP} and t_{WR} (Fig. 10), that is:

$$t_{WC}\,(MIN) = t_{AW} + t_{WP} + t_{WR}$$

Read-Modify-Write

A read-modify-write cycle is merely a combination of a read cycle and a read/write pulse, t_{WP}. The minimum read-modify-write cycle time is therefore $t_{RC} + t_{WP}$. The timing associated with the 2102A read-modify-write cycle is shown in Figure 11.

D.C. and Operating Characteristics

The D.C. and operating characteristics for the 2102A is given in Table IV. Power supply current versus V_{CC} supply voltage is shown in Figure 12 for the 2102A. Power supply current as a function of temperature is shown in Figure 13 for the 2102A.

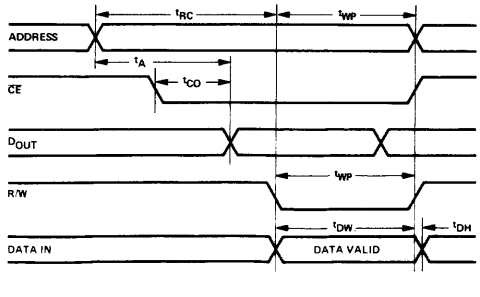


Figure 11. 2102A Read-Modify-Write Cycle

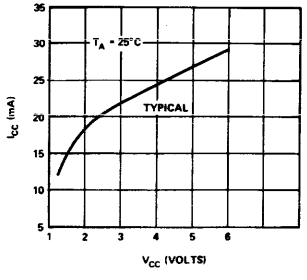


Figure 12. 2102A Power Supply vs. Supply Voltage

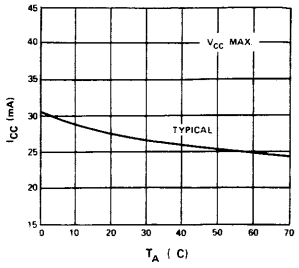


Figure 13. Power Supply Current vs. Ambient Temperature.

For reference, typical A.C. and D.C characteristics for the 2102A are shown in the graphs of Figure 14. In particular, note the relative insensitivity of access time as a function of load capacitance.

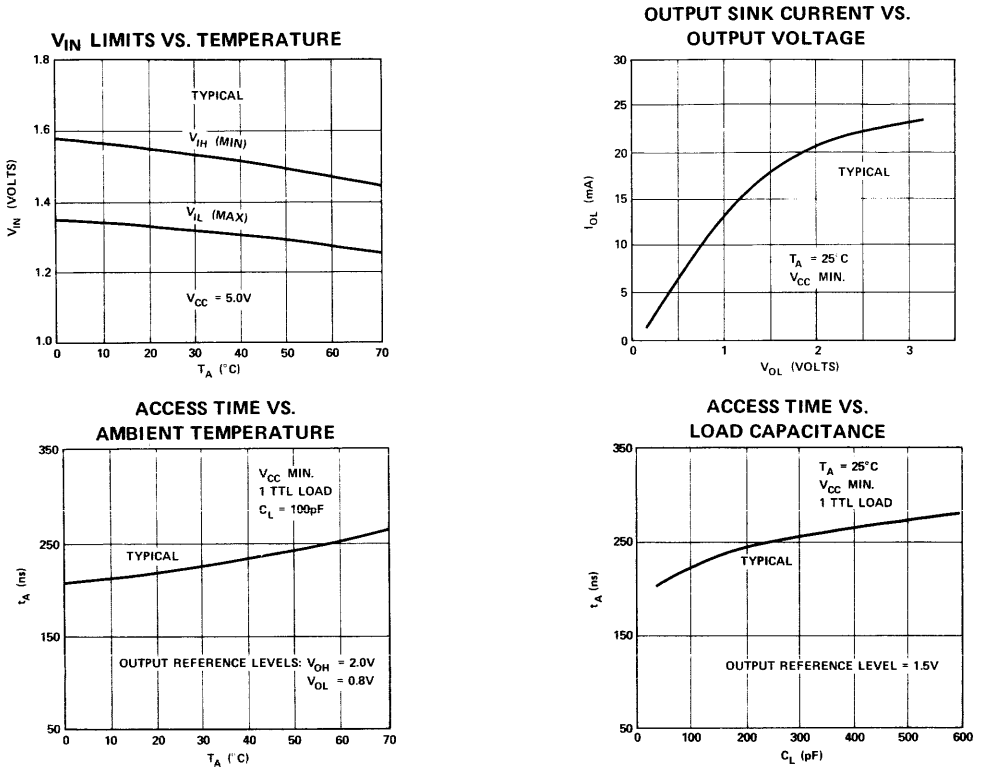


Figure 14. 2102A Typical D.C. and A.C. Characteristics

Table IV. 2102A D.C. and Operating Characteristics.
T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	2102A, 2102A-4 2102AL, 2102AL-4 Limits Min.	Typ.[1]	Max.	2102A-2, 2102AL-2 Limits Min.	Typ.[1]	Max.	2102A-6 Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10		1	10		1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Output Leakage Current		1	5		1	5		1	5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = V_{OH}
I_{LOL}	Output Leakage Current		-1	-10		-1	-10		-1	-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
I_{CC}	Power Supply Current		33	Note 2		45	65		33	55	mA	All Inputs = 5.25V, Data Out Open, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	-0.5		0.65	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4			0.4			0.45	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4			2.4			2.2			V	I_{OH} = -100μA

Notes: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. The maximum I_{CC} value is 55mA for the 2102A and 2102A-4, and 33mA for the 2102AL and 2102AL-4.

Power Down Standby Operation

The 2102AL may be placed in a power down mode where data is maintained with greatly reduced power dissipation (maximum of 42 mW vs. 368 mW). Data is maintained at a reduced power setting because the load devices in the storage cell (Q_2 and Q_5) shown in Figure 2B are implemented with depletion load devices. As mentioned previously, a depletion mode device is normally "on" and requires a negative voltage (below ground) to reach cut-off in operation (see Fig. 3). The only requirement, therefore, to assure data retention is to guarantee that the minimum V_{CC} voltage allowed in standby operation is sufficient to bias the gate of the appropriate storage node (Q_3 or Q_4 Fig. 2B) on. (Recall that there is no threshold drop across the depletion load device supplying the on drive to the storage device.)

A summary of the power down requirements and characteristics for the 2102AL family are shown in Figure 15 and Table V. As is shown in this figure, there is a requirement that chip enable be brought to a level of 2.0V, or higher, a T_{CP} time (minimum 0 nsec) before V_{CC} drops below its minimum value (4.75V).

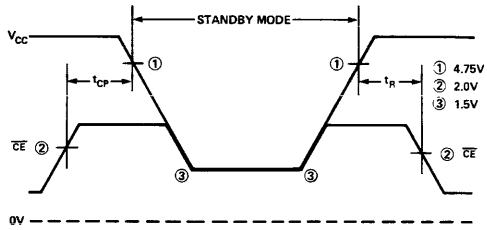


Figure 15. 2102AL Family Standby Characteristics.

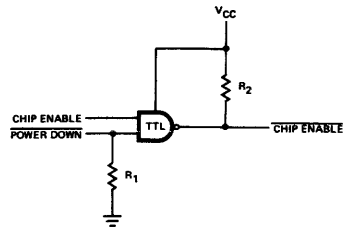


Figure 16. Chip Enable Generator for Power Down Mode

To assure that stored data is not over-written, the chip enable input must either be held at a level of 1.5V, or higher, or allowed to track with V_{CC} at the same or higher voltage level and same or slower discharge rate as V_{CC}.

A circuit that implements the tracking of chip enable with V_{CC} is shown in Figure 16. In this figure, the chip enable NAND circuit is powered by the same supply, V_{CC}, that is discharging. A power down signal ($\overline{\text{power down}}$) is generated to set the chip enable signal high at the appropriate time (discussed later). As V_{CC} begins to discharge beyond the limit of TTL operation, resistors R_1 and R_2 are used to assure that the $\overline{\text{chip enable}}$ output stays high and tracks the discharging V_{CC} independent of the chip enable input.

The power down signal can occur at any time if the memory is in a read cycle or is inactive. However, if a write cycle is being executed and power loss is detected, then the power down signal must be delayed until the write cycle is complete. In most

Table V. 2101AL Family D.C. Standby Characteristics.

T_A = 0°C to 70°C

Symbol	Parameter	2102AL, 2102AL-4 Limits Min.	Typ.[1]	Max.	2102AL-2 Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
V_{PD}	V_{CC} in Standby	1.5			1.5			V	
V_{CES}[2]	$\overline{CE}$ Bias in Standby	2.0			2.0			V	$2.0V \leqslant V_{PD} \leqslant V_{CC}$ Max.
		V_{PD}			V_{PD}			V	$1.5V \leqslant V_{PD} < 2.0V$
I_{PD1}	Standby Current		15	23		20	28	mA	All Inputs = V_{PD1} = 1.5V
I_{PD2}	Standby Current		20	30		25	38	mA	All Inputs = V_{PD2} = 2.0V
t_{CP}	Chip Deselect to Standby Time	0			0			ns	
t_R[3]	Standby Recovery Time	t_{RC}			t_{RC}			ns	

NOTES:

1. Typical values are for T_A = 25°C and nominal supply voltage.
2. Consider the test conditions as shown: If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max.) and 2.0V, then CE must be held at 2.0V Min. (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD}Min.), then CE and standby voltage must be at least the same value or, if they are different, CE must be the more positive of the two.
3. $t_R = t_{RC}$ (READ CYCLE TIME).

systems this is entirely feasible since the decoupling capacitors will hold V_{CC} power long enough to finish a complete write cycle at full power.

A schematic representation of a sudden loss of normal V_{CC} power is shown in Figure 17. If at t = 0 the V_{CC} supply is removed, power will be supplied to the load (L) from the capacitor (C) until the load voltage (V_L) is a diode drop below the battery voltage (V_B), after which power to the load is supplied by the battery. There is no requirement to control the rate at which V_{CC} discharges.

Similarly, when the supply voltage is restored, the voltage at the load (V_L) will begin to rise when the supply voltage becomes greater than the battery voltage.

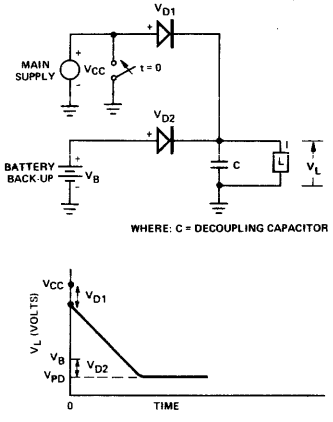


Figure 17. Battery Backup Characteristics

Note that the 2102A is capable of retaining data in a power down mode over a V_{CC} voltage range of 1.5 to 4.75 *if the chip enable input is always a high level equal to or higher than V_{PD}* during standby. This allows maximum flexibility in the selection of batteries for standby. Remember that chip enable tracking requirements to V_{CC} are required *only* if the state of the chip enable input can not be guaranteed to be a high level during the entire standby period.

256 WORD x 4-BIT STATIC RAMs

The introduction of static, high density MOS RAMs organized as 256 words x 4 bits has significantly reduced the complexity, size and component count of systems not requiring large storage capacity.

With the Intel family of 256 word x 4 bit RAMs it is now possible to realize more benefits of "distributed" memory using MOS devices with their attendant low power and simple interface.

designated as 2101A, 2111A, and 2112A. In summary the 2101A is packaged in a 22 pin DIP, has four data-in and four data-out lines, two chip enables and an output disable. The 2111A is packaged in an 18 pin DIP, has four common data-in/data-out lines, two chip enables, and an output disable. The 2112A is packaged in a 16 pin DIP, has four common data-in/data-out lines, one chip enable and does *not* have an output disable. These selections allow the system designer almost any configuration he might desire.

2101A Operation

Internal operation of the 2101A is similar to that outlined for the 2102A. The storage cell is shown in Figure 2A; the address input buffers and internal decoders are shown in Figures 5 and 6 respectively.

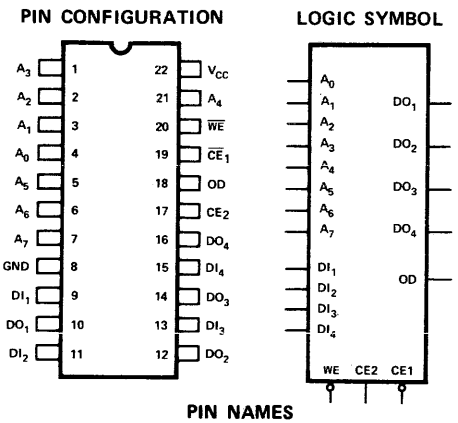
Maximum system design flexibility is achieved with the 2101A for those applications requiring 256 word x 4 bit memory devices. Since the input/output lines are separated, it is not necessary to multiplex these lines unless required by the system. The two chip enables of opposite logic polarity simplify system interface design (especially with the 8080 microprocessor as discussed in the *Systems* section).

The pin configuration and logic symbol for the 2101A are shown in Figure 18. The block diagram is shown in Figure 19.

The 2101A may be operated in the same operating modes as the 2102A. For example, a series of reads may be performed on a given device with the chip enables at the proper selected state and the output disable line held low. The write and read-modify-write cycles may be performed per the 2102A description. For reference, the read and write waveforms are shown in Figure 20 with A.C. characteristics given in Table VI. D.C. and operating characteristics are shown in Table VII.

As discussed previously, the 2101A has separate input and output pins for data. When operating the device with the output OR-tied, it is permissible to tie the output disable pin low for all operations. If the data output pins are OR-tied with other devices, the chip enable inputs are used to electrically disconnect the unselected devices from the output data buses. In this unselected state ($\overline{CE1}$ high or CE2 low) the output devices are placed in the high impedance state.

The 2101A may also be operated with the corresponding input and output lines tied together. In this mode of operation output disable must be used to place the output devices in the high impedance state during a write cycle or the write portion of a read-modify-write cycle.



PIN NAMES

DI_1-DI_4	DATA INPUT	CE_2	CHIP ENABLE 2
A_0-A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
$\overline{WE}$	WRITE ENABLE	DO_1-DO_4	DATA OUTPUT
$\overline{CE_1}$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

Figure 18. 2101A Pin Configuration/Logic Symbol.

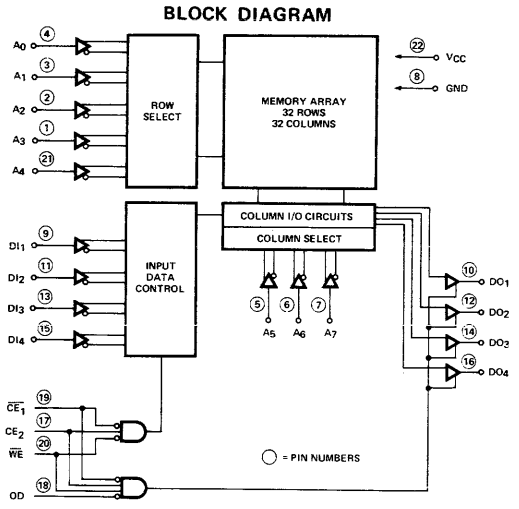
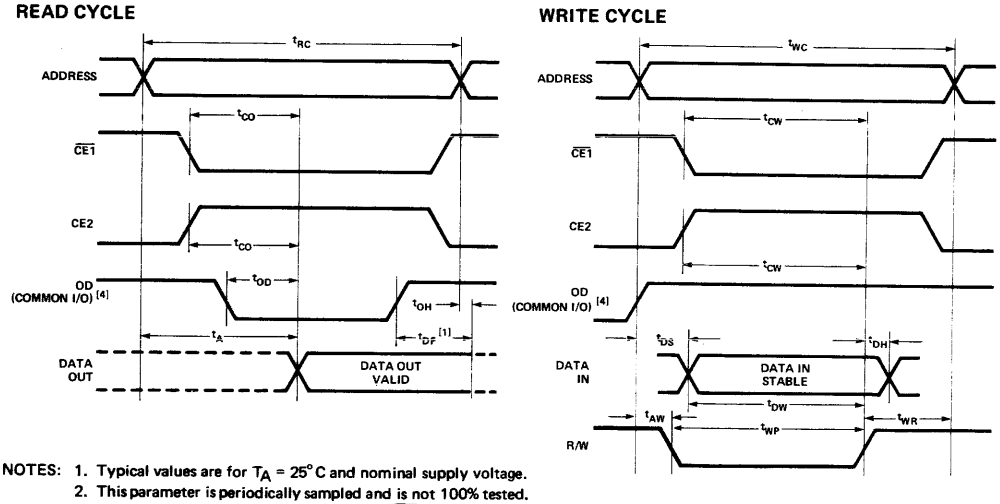


Figure 19. 2101A Block Diagram.



NOTES:
1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, CE_2, or OD, whichever occurs first.
4. OD should be tied low for separate I/O operation.

Figure 20. 2101A Read/Write Waveforms.

Table VI. 2101A A.C. Characteristics.

READ CYCLE $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	
t_A	Access Time			250	ns	t_r, t_f = 20ns
t_{CO}	Chip Enable To Output			180	ns	Input Levels = 0.8V or 2.0V
t_{OD}	Output Disable To Output			130	ns	Timing Reference = 1.5V
t_{DF}[3]	Data Output to High Z State	0		180	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid after change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	170			ns	
t_{AW}	Write Delay	20			ns	t_r, t_f = 20ns
t_{CW}	Chip Enable To Write	150			ns	Input Levels = 0.8V or 2.0V
t_{DW}	Data Setup	150			ns	Timing Reference = 1.5V
t_{DH}	Data Hold	0			ns	Load = 1 TTL Gate
t_{WP}	Write Pulse	150			ns	and C_L = 100pF.
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

Table VII. 2101A D.C. and Operating Characteristics

$T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ unless otherwise specified.

Symbol	Parameter		Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			1	10	μA	V_{IN} = 0 to 5.25V
I_{LOH}	Data Output Leakage Current			1	10	μA	Output Disabled, V_{OUT}=4.0V
I_{LOL}	Data Output Leakage Current			-1	-10	μA	Output Disabled, V_{OUT}=0.45V
I_{CC1}	Power Supply Current	2101A, 2101A-4		35	55	mA	V_{IN} = 5.25V, I_O = 0mA
		2101A-2		45	65		$T_A = 25°C$
I_{CC2}	Power Supply Current	2101A, 2101A-4			60	mA	V_{IN} = 5.25V, I_O = 0mA
		2101A-2			70		$T_A = 0°C$
V_{IL}	Input "Low" Voltage		-0.5		+0.8	V	
V_{IH}	Input "High" Voltage		2.0		V_{CC}	V	
V_{OL}	Output "Low" Voltage				+0.45	V	I_{OL} = 2.0mA
V_{OH}	Output "High" Voltage	2101A, 2101A-2	2.4			V	I_{OH} = -200μA
		2101A-4	2.4			V	I_{OH} = -150μA

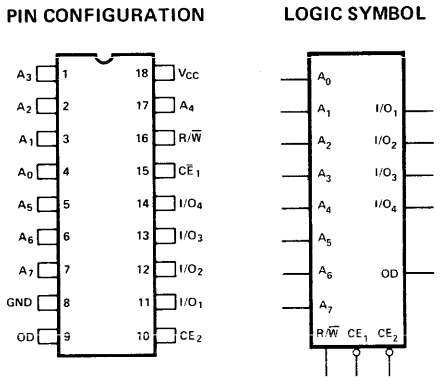
2111A Operation

The 2111A has common input/output data buses and operates in a manner similar to that described for the 2101A with the data bus made common. The only logical difference between the two devices is the logic level of the two chip enables. For the 2111A both chip enables are true in the low state.

If either or both of the chip enables are high the internal input output data buffers are electrically disconnected from the external data bus.

The pin configuration and logic symbol for the 2111A are shown in Figure 21. The block diagram is shown in Figure 22.

As indicated previously, the read/write, address, and data in timing requirements for the 2111A are the same as for the 2101A operating in the



PIN NAMES

A_0-A_7	ADDRESS INPUTS
OD	OUTPUT DISABLE
$\overline{R/W}$	READ/WRITE INPUT
$\overline{CE}_1$	CHIP ENABLE 1
CE_2	CHIP ENABLE 2
I/O_1-I/O_4	DATA INPUT/OUTPUT

Figure 21. 2111A Pin Configuration/Logic Symbol

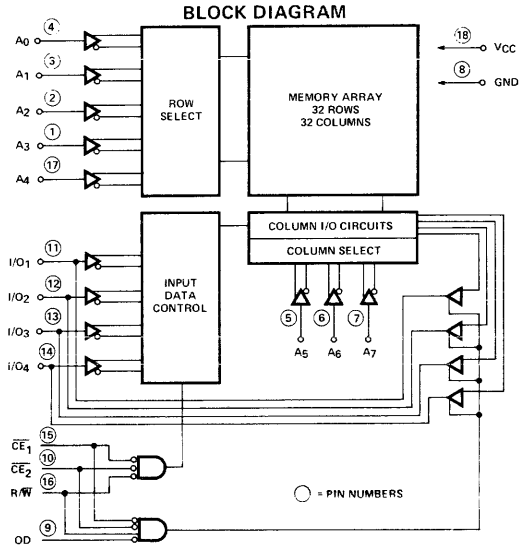
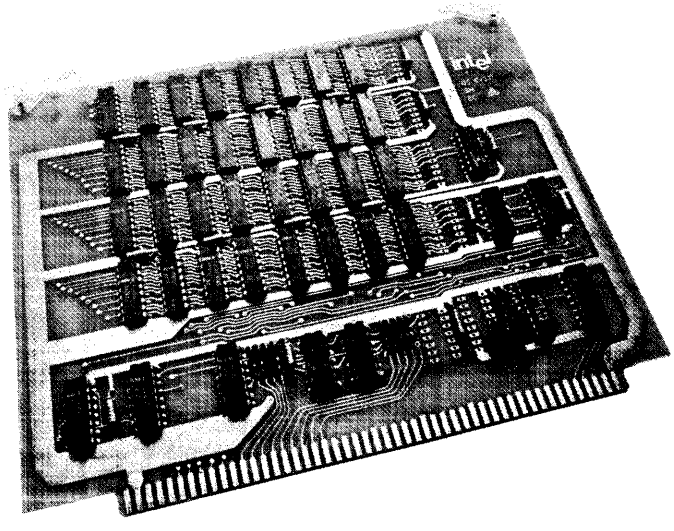


Figure 22. 2111A Block Diagram



Intel Memory Systems Division 4K x 8 Memory Card

common data bus mode. For reference, however, the read/write waveforms for the 2111A are shown in Figure 23 with the A.C. characteristics shown in Table VIII. D.C. characteristics are given in Table IX.

2112A Operation

The 2112A operates in a manner very similar to the 2111A. The major difference is that no output disable pin is available and one (instead of two) chip enables is used. Pin configuration and logic symbol for the 2112A are shown in Figure 24. The block diagram is shown in Figure 25.

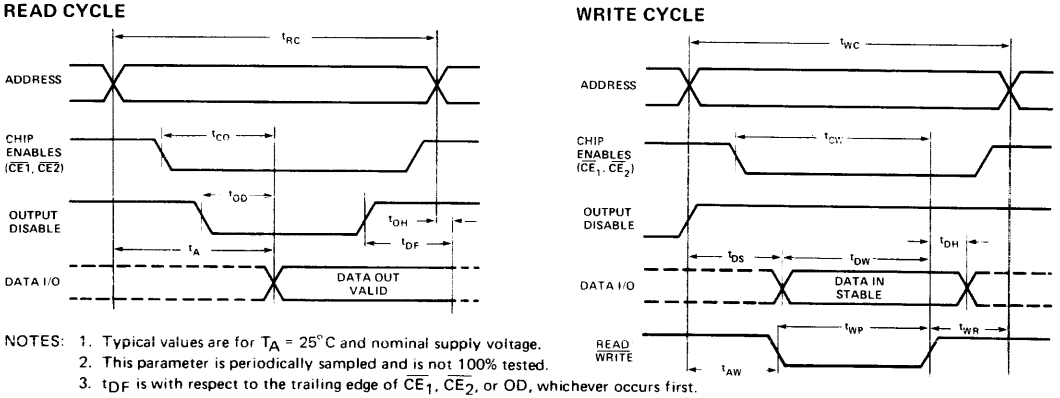
Since no output disable pin is available for the 2112A, care should be exercised to assure that the data in bus is not activated any time the read/write line is high (read cycle). When operating the memory in a write, read-modify-write, or write-verify-read cycle, the read/write input is used to perform the function of an output disable. The output is disabled on the chip according to the following logical equation:

$$OD = \overline{R/W} + \overline{CE}$$

where:

OD = OUTPUT DISABLE

The basic read/write timing waveforms are shown in Figure 26 with the A.C. characteristics given in Table X.



NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltage.
2. This parameter is periodically sampled and is not 100% tested.
3. t_{DF} is with respect to the trailing edge of $\overline{CE_1}$, $\overline{CE_2}$, or OD, whichever occurs first.

Figure 23. 2111A Read/Write Waveforms.

Table VIII. 2111A A.C. Characteristics

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	250			ns	
t_A	Access Time			250	ns	t_r, t_f = 20ns
t_{CO}	Chip Enable To Output			180	ns	Input Levels = 0.8V or 2.0V
t_{OD}	Output Disable To Output			130	ns	Timing Reference = 1.5V
t_{DF}[3]	Data Output to High Z State	0		180	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid after change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE

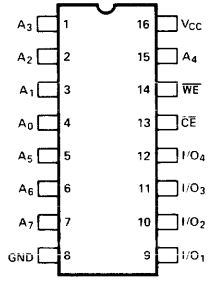
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC}	Write Cycle	170			ns	
t_{AW}	Write Delay	20			ns	t_r, t_f = 20ns
t_{CW}	Chip Enable To Write	150			ns	Input Levels = 0.8V or 2.0V
t_{DW}	Data Setup	150			ns	Timing Reference = 1.5V
t_{DH}	Data Hold	0			ns	Load = 1 TTL Gate
t_{WP}	Write Pulse	150			ns	and C_L = 100pF.
t_{WR}	Write Recovery	0			ns	
t_{DS}	Output Disable Setup	20			ns	

Table IX. 2111A D.C. Characteristics.

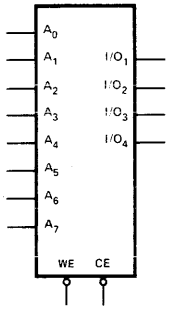
T_A = 0°C to 70°C, V_{CC} = 5V ±5% , unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current		1	10	µA	V_{IN} = 0 to 5.25V
I_{LOH}	I/O Leakage Current		1	10	µA	Output Disabled, $V_{I/O}$ = 4.0V
I_{LOL}	I/O Leakage Current		-1	-10	µA	Output Disabled, $V_{I/O}$=0.45V
I_{CC1}	Power Supply Current 2111A, 2111A-4		35	55	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
	Power Supply Current 2111A-2		45	65	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 25°C
I_{CC2}	Power Supply Current 2111A, 2111A-4			60	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
	Power Supply Current 2111A-2			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage 2111A, 2111A-2	2.4			V	I_{OH} = -200µA
	Output High Voltage 2111A-4	2.4			V	I_{OH} = -150µA

PIN CONFIGURATION



LOGIC SYMBOL



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
$\overline{CE}$	CHIP ENABLE INPUT
I/O_1-I/O_4	DATA INPUT/OUTPUT
V_{CC}	POWER (+5V)

Figure 24. 2112A Pin Configuration/Logic Symbol.

BLOCK DIAGRAM

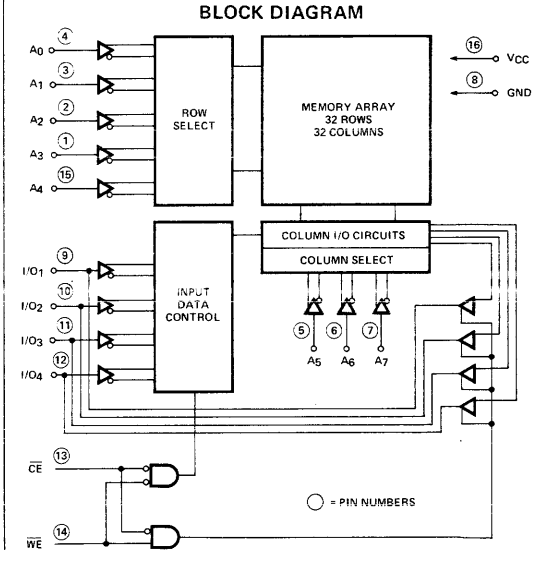
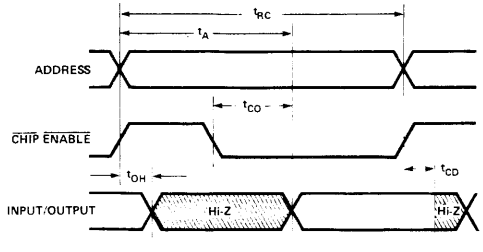


Figure 25. 2112A Block Diagram.

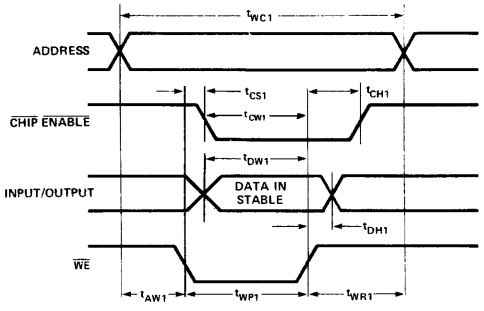
READ CYCLE WAVEFORMS



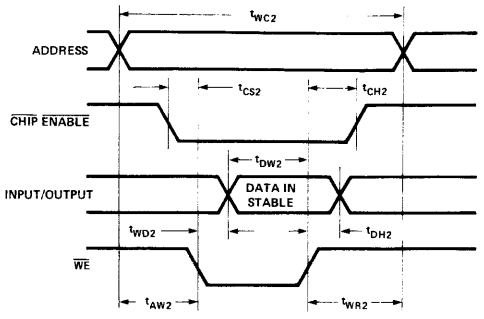
NOTE 1: Data Hold Time (T_{OH}) is referenced to the trailing edge of CHIP ENABLE (CE) or READ/WRITE (R/W) whichever comes first.

Figure 26. 2112A Read/Write Waveforms.

WRITE CYCLE #1



WRITE CYCLE #2



NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

Figure 26. (cont'd)

RAMs

Table X. 2112A A.C. Characteristics.

READ CYCLE T_A = 0°C to 70°C, V_{CC} = 5V ±5% unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{RC}	Read Cycle	350			ns	t_r, t_f = 20ns
t_A	Access Time			350	ns	Input Levels = 0.8V or 2.0V
t_{CO}	Chip Enable To Output Time			240	ns	Timing Reference = 1.5V
t_{CD}	Chip Enable To Output Disable Time	0		200	ns	Load = 1 TTL Gate
t_{OH}	Previous Read Data Valid After Change of Address	40			ns	and C_L = 100pF.

WRITE CYCLE #1 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC1}	Write Cycle	270			ns	t_r, t_f = 20ns
t_{AW1}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW1}	Write Setup Time	250			ns	Timing Reference = 1.5V
t_{WP1}	Write Pulse Width	250			ns	Load = 1 TTL Gate
t_{CS1}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH1}	Chip Enable Hold Time	0			ns	
t_{WR1}	Write Recovery Time	0			ns	
t_{DH1}	Data Hold Time	0			ns	
t_{CW1}	Chip Enable to Write Setup Time	250			ns	

WRITE CYCLE #2 T_A = 0°C to 70°C, V_{CC} = 5V ±5%

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
t_{WC2}	Write Cycle	470			ns	t_r, t_f = 20ns
t_{AW2}	Address To Write Setup Time	20			ns	Input Levels = 0.8V or 2.0V
t_{DW2}	Write Setup Time	250			ns	Timing Reference = 1.5V
t_{WD2}	Write To Output Disable Time	200			ns	Load = 1 TTL Gate
t_{CS2}	Chip Enable Setup Time	0			ns	and C_L = 100pF.
t_{CH2}	Chip Enable Hold Time	0			ns	
t_{WR2}	Write Recovery Time	0			ns	
t_{DH2}	Data Hold Time	0			ns	

NOTE: 1. Typical values are for T_A = 25°C and nominal supply voltage.

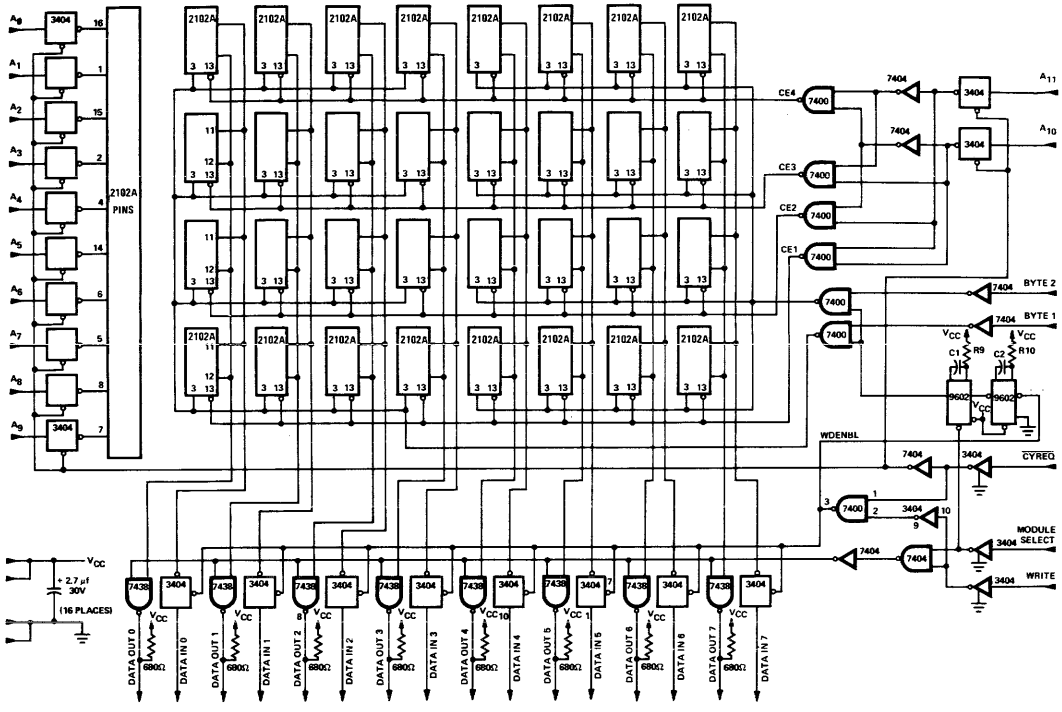


Figure 27. 4K x 8 Memory System.

SYSTEM DESIGN/OPERATION

The design of timing and interface circuits for memory systems utilizing Intel static RAMs is simple and straightforward. In this section, details of system designs using these static RAMs will be discussed.

Consider first the 4K x 8 system shown in Figure 27. This system, Intel's in-26 self-contained memory card, is expandable in both the number of words and number of bits/word directions. (Expanding the number of words per system is accomplished with the module select input.) Note that there are only three input control lines: write, module select and cycle request (CYREQ) (with byte control provided). Operation of the 4K x 8 memory system is explained with the aid of the timing diagram is shown in Figure 28.

At time T_0 the 100 nsec $\overline{\text{CYREQ}}$ pulse is applied, the addresses made valid, the write input, and data is made valid (for write mode only). The module select input is set low no later than 80 nsec after T_0. (If only one board is used, the module select line may be permanently tied to ground.) Output data is available at time defined by timing diagram (650 nsec) with cycle completed for both read and write at 650 nsec after start of cycle. (Note

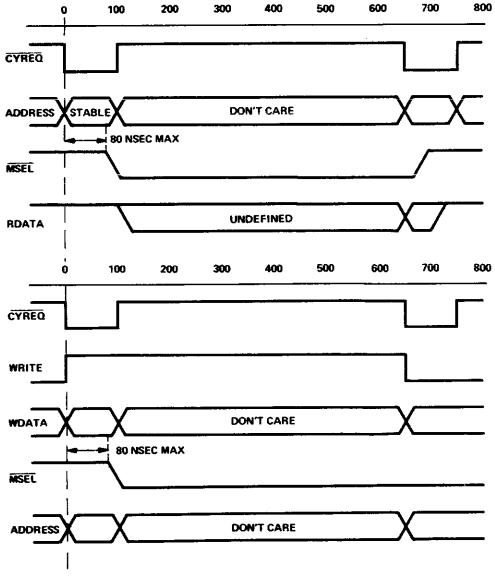


Figure 28. Timing Diagram, 4K x 8/9 System.

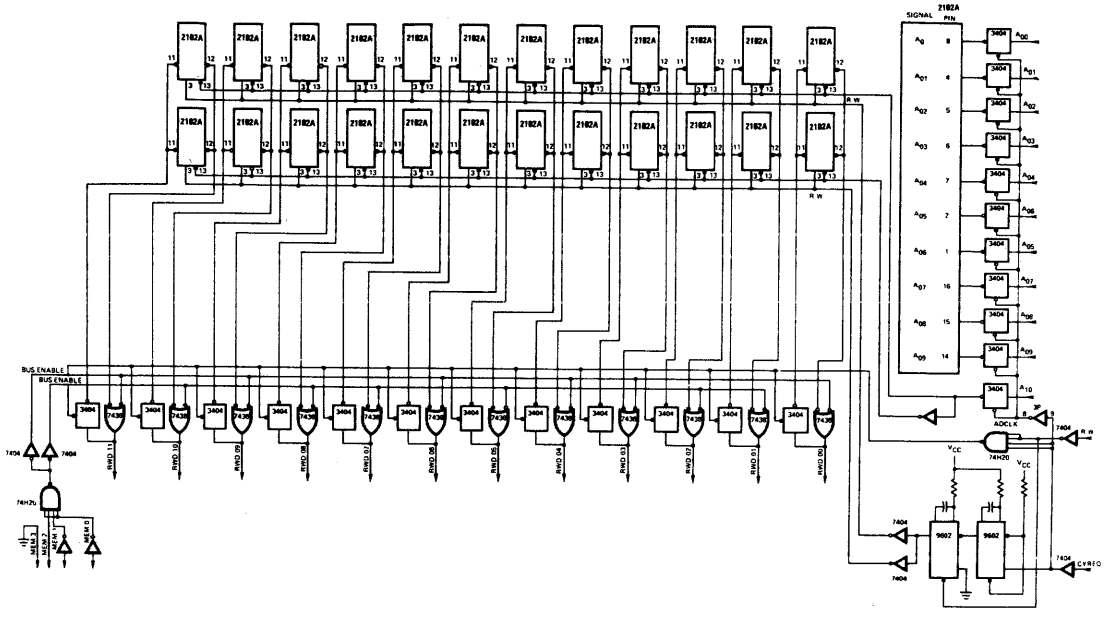


Figure 29. 2K x 12 Memory System.

that the in-26 is designed for use with standard 2102-1 devices. Faster system access/cycle times can be obtained by using 2102A devices and 74H or 74S series instead of 74 series gates in the $\overline{\text{CYREQ}}$ and module select data paths.)

Note that the input data is latched at the end of cycle request ($\overline{\text{CYREQ}}$). It is possible to remove the two monostable multivibrators from the system and control the memory device read/write line externally further simplifying the memory system.

An example of a 2K x 12 single card memory system (IN-24) with full control and interfacing is shown in Figure 29. In this system, the input/output data is on a single bus. Note that data output enable is provided by an address selection for this system. Operation of the in-24 is similar to the in-26.

STATIC RAM MEMORY ARRAY

A layout of the memory array for the 2102A static RAM is shown in Figure 30. Note that there are no layout constraints as a result of noise considerations caused by high level clocks. Power busing is greatly simplified over other MOS RAMs because only one supply plus ground is required for the memory.

Memory array layout for the 2101A, 2111A, and 2112A is entirely similar to the layout shown above. The exception, of course, is the number of data input/output lines in the array. Decoupling is handled in a manner identical to that shown in Figure 31.

INTERFACING WITH MICROPROCESSORS

The Intel static RAM family is ideal for use in microprocessor applications. Control and timing functions are all performed by the microprocessor itself so that additional timing is not required by the memory.

An example of a microprocessor system utilizing both read only (ROM) and random access memory is shown in Figure 32. Although it is not the purpose of this application note to explain microprocessor systems, several comments on the operation of the system are in order.

The buffered 16 bit address bus is tapped (as shown) to provide both chip select and memory address to the static RAMs. (In this case the 2101A equivalent for microprocessors, the 8101 is used.) A control circuit used with the 8080 generates a memory read signal which enables the output on the 8101. Since both chip enables and output disable are used to gate data out of the 8101, the data out bus from these sources is in a high impedance state whenever the ROM is being addressed. This allows OR tying of the data out lines to the data bus. Note that in this case the data in/data out pins of the 8101 are tied together (see discussion of 2101A operation).

Care should be taken when connecting P-channel

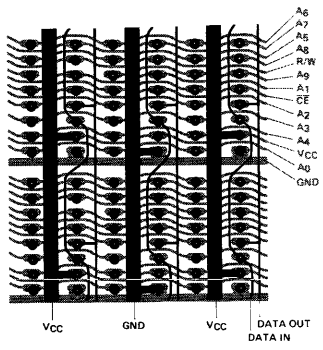


Figure 30. 2102A Memory Array Layout.

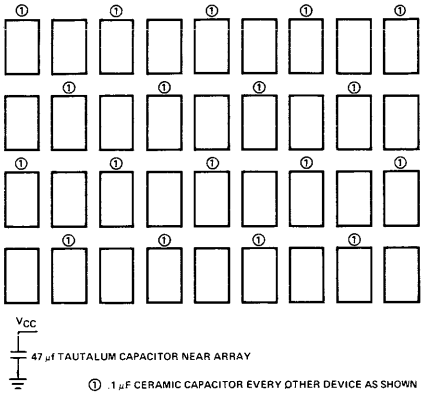


Figure 31. Memory System Decoupling.

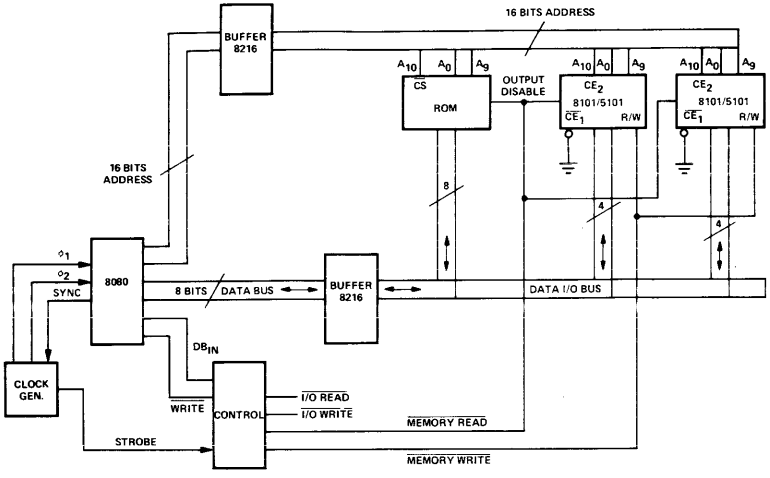


Figure 32. Microprocessor System.

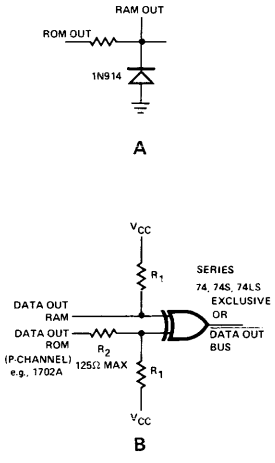


Figure 33. Output Data Bus.

ROMs such as the 1602A and 1702A to the data bus as shown in Figure 32 to assure that the minimum output low level is compatible with the N-channel RAMs being used. It is necessary to protect the data line of the static RAMs if the output level of the ROMs attached to the line can drop below V_{SS} -0.8V. This protection can be done by using a diode to ground and current limiting resistor on those data lines effected (see Fig. 33). It is also permissible to use an exclusive OR which has an internal clamping diode on its input configured per Figure 34B. Note that series 74L86 cannot be used in this application because it does not have a terminating diode.

In the figure shown in Figure 33B, resistors R_1 are pull up resistors to the unselected data out line. R_2 is a current limiting resistor connected to the output of the P-channel ROM. The maximum value permissible for this resistor is determined by the maximum sink current drawn by the ROM device and the maximum acceptable (most positive) down level required for the input of the exclusive OR.

SUMMARY

The Intel static RAM family is a broad and expanding line of simple to use high density MOS RAMs. This application note has detailed those portions of the internal MOS circuits of these RAMs which are of primary concern to the system designer. Through a better understanding of the internal workings of the device, the designer is able to take full advantage of the capability of these RAMs.

A summary of some of the more important technical specifications for each device and device spec type is given in the Product Selection Guide at the end of this section.

RANDOM ACCESS MEMORIES

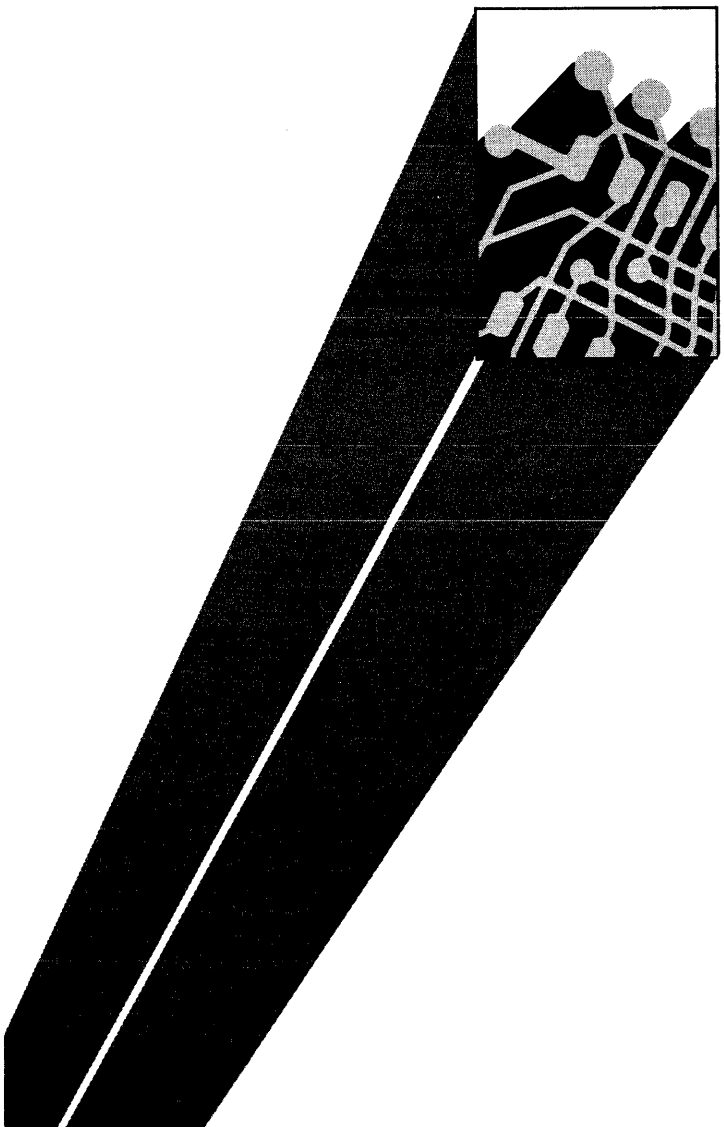
SILICON GATE MOS

Type	No. of Bits	Description	Organi-zation	No. of Pins	Electrical Characteristics Over Temperature			
					Access Time Max.	Cycle Time Max.	Power Dissipation Max.[1] Operating/Standby	Supplies[V]
1101A	256	Static Fully Decoded	256x1	16	1500ns	1500ns	685mW/340mW	+5, -9
1101A1	256	Hi-Speed Static Fully Decoded	256x1	16	1000ns	1000ns	685mW/340mW	+5, -9
1103	1024	Dynamic Fully Decoded	1024x1	18	300ns	580ns	400mW/64mW	+16, +19
1103-1	1024	Dynamic Fully Decoded	1024x1	18	150ns	340ns	437mW/76mW	+19, +22
1103A	1024	Dynamic Fully Decoded	1024x1	18	205ns	580ns	400mW/64mW	+16, +19
1103A-1	1024	Dynamic Fully Decoded	1024x1	18	145ns	340ns	627mW/10mW	+19, +22
1103A-2	1024	Dynamic Fully Decoded	1024x1	18	145ns	400ns	570mW/10mW	+19, +22
2101A	1024	Static, Separate I/O	256x4	22	350ns	350ns	300mW	+5
2101A-2	1024	Static, Separate I/O	256x4	22	250ns	250ns	350mW	+5
2101A-4	1024	Static, Separate I/O	256x4	22	450ns	450ns	300mW	+5
2102A	1024	High Speed Static	1024x1	16	350ns	350ns	275mW	+5
2102A-2	1024	High Speed Static	1024x1	16	250ns	250ns	325mW	+5
2102A-4	1024	High Speed Static	1024x1	16	450ns	450ns	275mW	+5
2102A-6	1024	High Speed Static	1024x1	16	650ns	650ns	275mW	+5
2102AL	1024	Low Standby Power Static	1024x1	16	350ns	350ns	165mW/35mW	+5
2102AL-2	1024	Low Standby Power Static	1024x1	16	250ns	250ns	325mW/42mW	+5
2102AL-4	1024	Low Standby Power Static	1024x1	16	450ns	450ns	165mW/35mW	+5
M2102A-4	1024	Static, T_A = -55°C to +125°C	1024x1	16	450ns	450ns	350mW	+5
2104A-1	4096	16 Pin Dynamic	4096x1	16	150ns	320ns	420mW/18mW	+12, +5 -5
2104A-2	4096	16 Pin Dynamic	4096x1	16	200ns	320ns	384mW/18mW	+12, +5, -5
2104A-3	4096	16 Pin Dynamic	4096x1	16	250ns	375ns	360mW/18mW	+12, +5, -5
2104A-4	4096	16 Pin Dynamic	4096x1	16	300ns	425ns	360mW/18mW	+12, +5, -5
2107A	4096	22 Pin Dynamic	4096x1	22	300ns	700ns	458mW/2mW	+12, +5, -5
2107A-1	4096	22 Pin Dynamic	4096x1	22	280ns	550ns	516mW/2mW	+12, +5, -5
2107A-4	4096	22 Pin Dynamic	4096x1	22	350ns	840ns	450mW/2mW	+12, +5, -5
2107A-5	4096	22 Pin Dynamic	4096x1	22	420ns	970ns	376mW/2mW	+12, +5, -5
2107B	4096	22 Pin Dynamic	4096x1	22	200ns	400ns	648mW/4mW	+12, +5, -5
2107B-4	4096	22 Pin Dynamic	4096x1	22	270ns	470ns	648mW/4mW	+12, +5, -5
2107B-5	4096	22 Pin Dynamic	4096x1	22	300ns	590ns	648mW/5mW	+12, +5, -5
2108-2	8192	16 Pin Dynamic	8192x1	16	200ns	350ns	828mW/24mW	+12, +5, -5
2108-4	8192	16 Pin Dynamic	8192x1	16	300ns	425ns	780mW/24mW	+12, +5, -5
2111A	1024	Static, Common I/O with Output Deselect	256x4	18	350ns	350ns	300mW	+5
2111A-2	1024	Static, Common I/O with Output Deselect	256x4	18	250ns	250ns	350mW	+5
2111A-4	1024	Static, Common I/O with Output Deselect	256x4	18	450ns	450ns	300mW	+5
2112A	1024	Static, Common I/O without Output Deselect	256x4	16	350ns	350ns	300mW	+5
2112A-2	1024	Static, Common I/O without Output Deselect	256x4	16	250ns	250ns	350mW	+5
2112A-4	1024	Static, Common I/O without Output Deselect	256x4	16	450ns	450ns	300mW	+5

RANDOM ACCESS MEMORIES (Continued)

	Type	No. of Bits	Description	Organi-zation	No. of Pins	Electrical Characteristics Over Temperature			
						Access Time Max.	Cycle Time Max.	Power Dissipation Max.[1] Operating/Standby	Supplies[V]
SILICON GATE MOS	**2114**	4096	Static, Common I/O	1024x4	18	450ns	450ns	710mW	+5
	2114-2	4096	Static, Common I/O	1024x4	18	200ns	200ns	710mW	+5
	2114-3	4096	Static, Common I/O	1024x4	18	300ns	300ns	710mW	+5
	2114L	4096	Static, Common I/O	1024x4	18	450ns	450ns	370mW	+5
	2114L-3	4096	Static, Common I/O	1024x4	18	300ns	300ns	370mW	+5
	2115A	1024	Static, Open Collector	1024x1	16	45ns	45ns	660mW	+5
	2115A-2	1024	Static, Open Collector	1024x1	16	70ns	70ns	660mW	+5
	2115AL	1024	Static, Open Collector	1024x1	16	45ns	45ns	395mW	+5
	2115AL-2	1024	Static, Open Collector	1024x1	16	70ns	70ns	395mW	+5
	M2115A	1024	Static, Open Collector	1024x1	16	55ns	55ns	690mW	+5
	M2115AL	1024	Static, Open Collector	1024x1	16	75ns	75ns	415mW	+5
	2115	1024	Static, Open Collector	1024x1	16	95ns	95ns	525mW	+5
	2115-2	1024	Static, Open Collector	1024x1	16	70ns	70ns	660mW	+5
	2115L	1024	Static, Open Collector	1024x1	16	95ns	95ns	345mW	+5
	2125A	1024	Static, Three-State	1024x1	16	45ns	45ns	660mW	+5
	2125A-2	1024	Static, Three-State	1024x1	16	70ns	70ns	660mW	+5
	2125AL	1024	Static, Three-State	1024x1	16	45ns	45ns	395mW	+5
	2125AL-2	1024	Static, Three-State	1024x1	16	70ns	70ns	395mW	+5
	M2125A	1024	Static, Three-State	1024x1	16	55ns	55ns	690mW	+5
	M2125AL	1024	Static, Three-State	1024x1	16	75ns	75ns	415mW	+5
	2125	1024	Static, Three-State	1024x1	16	95ns	95ns	525mW	+5
	2125-2	1024	Static, Three-State	1024x1	16	70ns	70ns	660mW	+5
	2125L	1024	Static, Three-State	1024x1	16	95ns	95ns	345mW	+5
	2116-2	16384	16 Pin Dynamic	16384x1	16	200ns	350ns	828mW/24mW	+12, +5, -5
	2116-3	16384	16 Pin Dynamic	16384x1	16	250ns	375ns	816mW/24mW	+12, +5, -5
	2116-4	16384	16 Pin Dynamic	16384x1	16	300ns	425ns	780mW/24mW	+12, +5, -5
	2147	4096	High Speed Static	4096x1	18	60-90ns	60-90ns	500mW/50mW (Typical)	+5
SCHOTTKY BIPOLAR	**3101**	64	Fully Decoded	16x4	16	60ns	60ns	525mW	+5
	3101A	64	High Speed Fully Decoded	16x4	16	35ns	35ns	525mW	+5
	3104	16	Content Addressable Memory	4x4	24	30ns	40ns	625mW	+5
SILICON GATE CMOS	**5101-8**	1024	Static CMOS RAM	256x4	22	800ns	800ns	150mW/2.5mW	+5
	5101L	1024	Static CMOS RAM	256x4	22	650ns	650ns	135mW/20µW	+5
	5101L-1	1024	Static CMOS RAM	256x4	22	450ns	450ns	135mW/20µW	+5
	5101L-3	1024	Static CMOS RAM	256x4	22	650ns	650ns	135mW/1mW	+5
	M5101-4	1024	Static CMOS RAM (-55°C to 125°C)	256x4	22	800ns	800ns	168mW/1mW	+5
	M5101L-4	1024	Static CMOS RAM (-55°C to 125°C)	256x4	22	800ns	800ns	168mW/400µW	+5

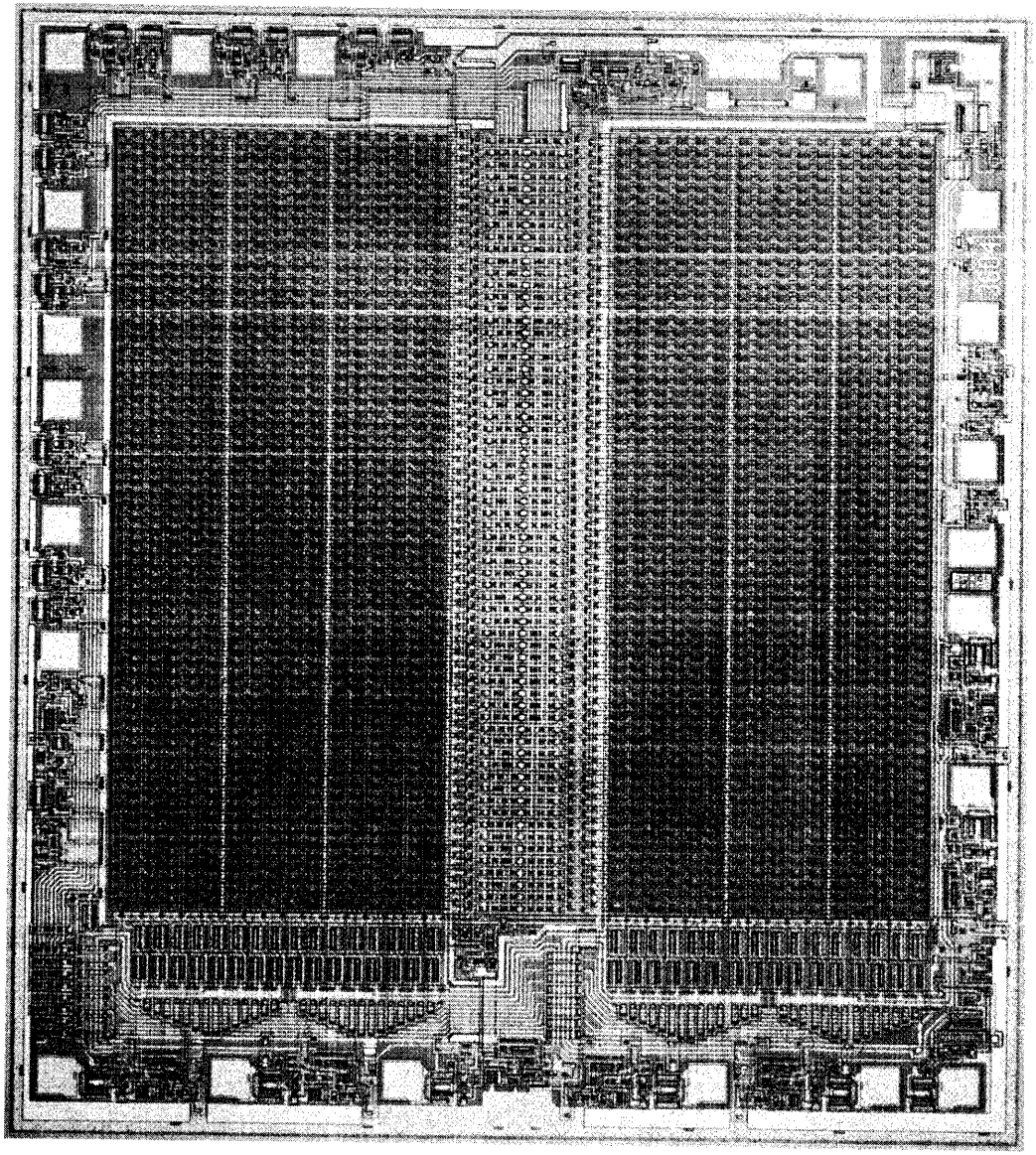
Read Only Memories



Designing with Intel® PROMs & ROMs

Bob Greene and
Dave House
Application Engineering

Contents



Photomicrograph of the Intel® 3604 4K (512 x 8) Bipolar PROM

INTRODUCTION

The combination of low cost, high speed, system design flexibility and data non-volatility has made read only memories an important part of many digital systems in production today. The rapid development of semiconductor read only memories has produced a succession of faster, larger, and more flexible devices.

Today, Intel combines the best of Schottky bipolar and P- and N-channel MOS semiconductor processing technologies to manufacture the fastest and largest line of read only memory products available anywhere in the world.

This chapter is divided into three sections. In the first section, *Understanding the Technology*, the various technologies used to produce read only memories and programmable read only memories are discussed in order to achieve a good understanding of how these devices operate and how one technology differs from another.

The second section describes the device from an operational and programming point of view, and presents Intel's extensive line of read only memories. In the third section, *System Applications*, the system aspects of address driving, output ORing, array configuration, printed circuit board layout, and power supply decoupling are presented.

Read Only Memories

A read only memory is an array of selectively open and closed unidirectional contacts. In the 16-bit array example shown in Figure 1, half of the address lines are decoded and used to energize one of the four row lines. This, in turn, activates those column lines which have a closed contact to the one selected row line. The remaining address lines are decoded and enable one of the column sense amplifiers. If chip select is true, the data is gated to the output pin by the output driver.

The primary differences in read only memories is in the forming of the open or closed contact; that is, in the design of the cell. In mask programmable read only memories (ROMs) the contact is made to selectively including or excluding a small conducting jumper during the final phase of semiconductor manufacture. In bipolar programmable read only memories (PROMs) the contact is made with a fusible material such that the contact can later be opened, allowing the data pattern to be configured by the user after the device has been manufactured.

Once programmed, Erasable Programmable Read Only Memories (EPROMs) allow the programmed contacts to be restored to their initial state, such that they can be re-programmed as often as desired.

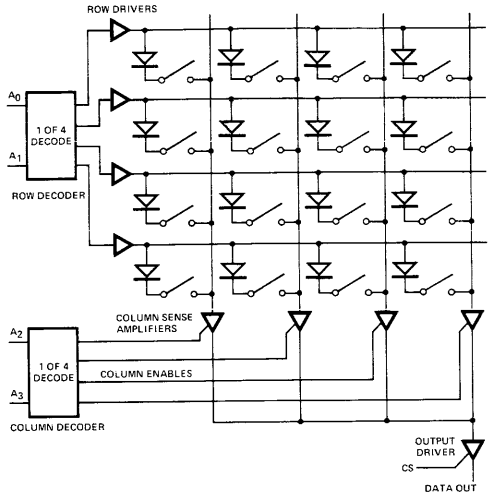


Figure 1. 16-Bit Simplified Array.

UNDERSTANDING THE TECHNOLOGY

As shown in Figure 2, there are two basic PROM/ROM technologies – bipolar and MOS. Their primary difference is in access time; bipolar access times are approximately 50–90 nS, and MOS access times are about an order of magnitude higher. Bipolar read only memories are available in 1K, 2K, and 4K bit sizes, while MOS read only memories are available in 2K through 16K bit sizes. Although PROMs and ROMs are available from both technologies, EPROMs are available only with MOS technology.

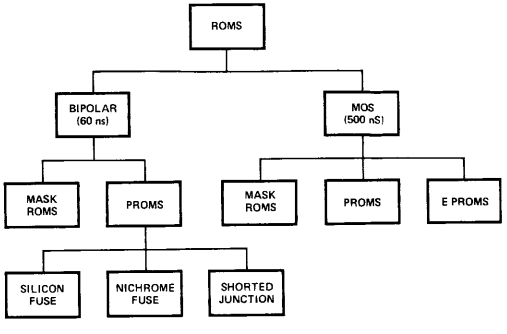


Figure 2. PROM/ROM Technology Family Tree.

Bipolar Technologies

As previously mentioned, bipolar devices offer higher speeds than MOS devices. For very high volume usage with those devices whose data pattern never change, mask programmable read only memories, commonly called ROMs, provide the lowest cost.

Electrically programmable read only memories, or PROMs, allow the data pattern to be defined when the device is used rather than when the device is manufactured.

MASK PROGRAMMABLE READ ONLY MEMORIES

Integrated circuit devices are fabricated from a wafer of silicon through a number of processing steps, including photo masking, etching, and diffusing in order to create a pattern of junctions and interconnections across the surface of the wafer. One of the final steps in the manufacturing process is to coat the entire surface of the silicon wafer with a layer of aluminum, and then to selectively etch away portions of the aluminum, leaving the desired interconnecting pattern. In the manufacture of mask programmed read only memories, the row-to-column contacts are selectively made by the inclusion or exclusion of aluminum connections in the final aluminum etch process.

The normal lead time required for fabrication of a new integrated circuit can be foreshortened from 9 to 10 weeks to about 4 to 6 weeks because the wafers can be manufactured through the point of metalization and held in storage until the data pattern is defined. By this method, the lead time required for delivery of a particular ROM pattern is only the time required to produce the mask and etch the final metal pattern on the wafer.

ELECTRICALLY PROGRAMMABLE READ ONLY MEMORIES

Electrically programmable read only memories allow the data pattern to be defined after final packaging rather than when the device is manufactured.

Three types of electrically programmable read only memories, commonly called PROMs, will be discussed here.

The Nichrome Fuse

The first PROMs were made with a nichrome fuse technology. Nichrome, an alloy of nickel and chrome, is deposited as a very thin film link to the column lines of the PROM. Heavy currents cause this film to "blow", opening the connection between the row and column lines. The cell is actually constructed of a transistor switch and the nichrome fuse, as shown in Figure 3. When the row is selected, the transistor, Q_{XY}, is turned on, and, if the fuse is intact, the column bus is pulled towards V_{CC} (+5V). If the fuse is "blown" or open, the column bus is left floating.

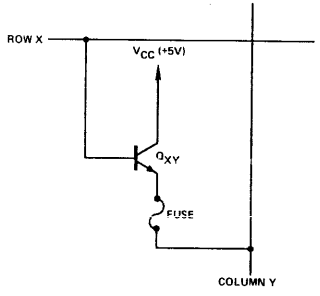


Figure 3. Typical Fuse Cell.

Nichrome Problems

Problems with nichrome fuses are all related to the technology. The selection of aluminum as the conductive material in integrated circuits and transistors did involve some serious metallurgical considerations. Of major importance is the fact that aluminum readily adheres to silicon dioxide, but does not rapidly diffuse through it. In addition, aluminum forms non-rectifying (ohmic) contacts with silicon.[1] Still, the formation of good silicon-to-aluminum contacts has always been a problem; the formation of good, reliable nichrome contact is a greater problem.

In addition, nichrome is not the easiest material to work with, especially considering the extremely thin layer (about 200 Angstroms) that must be deposited in order to achieve the desired resistance in the fuse. This deposition is very hard to control and the nichrome is additionally subject to corrosion.[2]

[1] Parker, G. H., J. C. Cornet, and W. S. Pinter. "Reliability Considerations in the Design and Fabrication of Polysilicon Fusible Link PROMs." A lecture to the IEEE 12th Annual Proceedings on Reliability Physics, 1974.

[2] Bauer, Joseph B. "Military Microcircuit Packaging," *The Electronic Engineer*, July 1972.

The most serious problem associated with nichrome fuse technology is probably the phenomenon commonly referred to as "growback",[3] the reversal of the programming process such that a single bit will, after some time, go from the programmed state back to the unprogrammed state.[4] Considerable analysis has been done to investigate this growback phenomenon[2-7] in nichrome fuse PROMs to understand how the nichrome fuse blows,[3,5,6] to determine the location and movement of the metals before and after fusion.[5,6] and to determine why a small number of these fuses (once blown) appear to reconnect.[2,5,6]

Fusion occurs under a layer of glass which has been added to the entire wafer to provide scratch protection and to minimize electron migration in the metal. Since fusion takes place without oxygen, or any other atmosphere, oxidation cannot play an important part in the fusing. It appears, rather, that the nichrome heats up under heavy current and becomes molten, forming a very narrow gap. Figure 4 is a picture taken with a scanning electron microscope of a blown nichrome fuse. Notice the fingers, or dendrites, of nichrome. Studies indicate that it is dendritic relinking that causes the fuse to begin to reconduct after some period of time.[5]

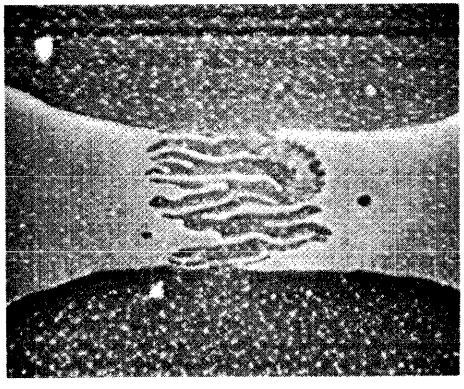


Photo courtesy of HI-REL Laboratories
San Marina, California

Figure 4. Blown Nichrome Fuse.

Electron microscope investigations reveal that random concentrations of nickel appear around the fused links,[6] and that the nickel reacts with the underlying SiO_2 in the gap,[5] forming a nickel-glass structure that resists chemical etching.[3] Also, chromium was found present in the gap.[5]

A CASE STUDY OF NICHROME GROWBACK

In one particular study of nichrome fuse failures performed by Litton,[5] the PROMs "were random samples from PROMs supplied by four manufacturers representing a buy of about twenty thousand 1024 PROMs over a three-year period. These PROMs were purchased to a high reliability full-temperature range specification reflecting a Mil Std-883 Class B screening requirement."

From this same study . . .

"It was found that there appeared to be a glass nichrome reaction which resulted in the formation of a glass structure which resisted the etch. These resistors had exhibited the reappearing bit phenomena after being in the computer in service in the field for some length of time. Further analysis of these resistors by the electron beam microprobe provided information needed to achieve a conceptual understanding of this growback reaction."

"Hard to program bits were associated with process control and PROM design. It was concluded that better than state of the art process controls were required. Therefore, additional screens were needed to insure reliability. The limitation of the number of program pulses and the energy to program was of extreme importance."

The reliability problems with nichrome fuse PROMs all relate to nichrome fuse processing technology; "growback" is inherent in the use of this technology. Some efforts have been made to find tests that will isolate PROM fuses that have a higher probability of relinking. These testing techniques include temperature stressing, temperature cycling, high temperature burn-in, and testing at reduced voltages. No test has been devised which will eliminate the relinking problem.

[3]Barnes, D. E. and J. E. Thomas. "Reliability Assessment of a Semiconductor Memory by Design Analysis." A lecture to the IEEE 12th Annual Proceedings on Reliability Physics, 1974.

[4]Devaney, John R. and A. M. Sheble, III. "Plasma Etching PROMs and Other Problems." A lecture to the IEEE 12th Annual Proceedings on Reliability Physics, 1974.

[5]Eisenberg, P. H. and R. Nosler. "Nichrome Resistors in Programmable Read Only Memory Integrated Circuits." A lecture to the IEEE 12th Annual Proceedings on Reliability Physics, 1974.

[6]Franklin, Paul and David Burgess. "Reliability Aspects of Nichrome Fusible Link PROMs (Programmable Read Only Memories)." A lecture to the IEEE 12th Annual Proceedings on Reliability Physics, 1974.

[7]Baitinger, W. E., N. Winograd, J. W. Amy, and J. A. Munarin. "Nichrome Resistor Failures as Studied by X-Ray Photoelectron Spectroscopy (XPS or ESCA)." A lecture to the IEEE 12th Annual Proceedings on Reliability Physics, 1974.

The Silicon Fuse

Intel bipolar PROMs, a typical cell of which is shown in Figure 3, work in the same manner as do the nichrome fuses, with the exception that the fuse material is polycrystalline silicon, which is deposited in a thick layer at the appropriate stage in the manufacturing process. This is the same standard, reliable technique that has been used by Intel in producing millions of MOS LSI circuits every week using polycrystalline silicon.

All of the Intel bipolar PROMs have included on the die a test row and column which are blown at wafer sort. The extra row and column are incorporated primarily to improve the programming yield of the final end product. By addressing this test row, the functionality of the decoders and the programmability of the fuses can be verified. The test fuse circuitry is designed such that arrays with unusual fuses that could cause programming yield problems can be screened at electrical test.

The fuse, shown in Figure 5, is a notched strip of polycrystalline silicon. Figure 6 shows an array of 12 cells. Each cell consists of a single transistor in an emitter-follower configuration with the silicon fuse connecting to the column line as shown in Figure 3. A cross section of the cell is shown in Figure 7.

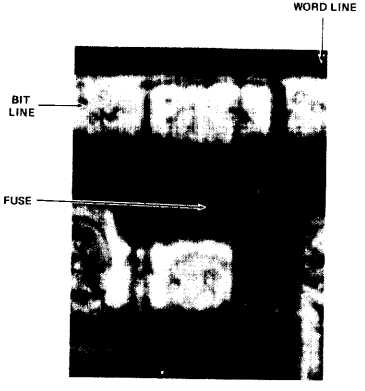


Figure 5. Unblown Polysilicon Fuse.

The thickness of the silicon fuse is nominally 3000 Angstroms, 15 times the thickness of the nichrome fuse. Resistivity of the fuse is controlled by doping, as in standard integrated circuits.

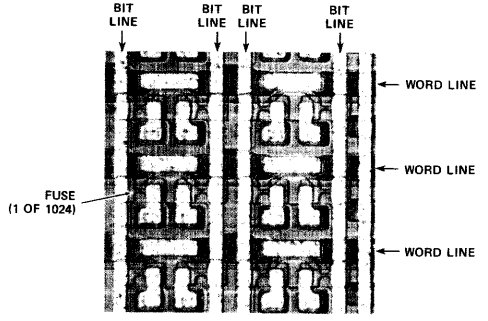


Figure 6. Polysilicon Cell Array.

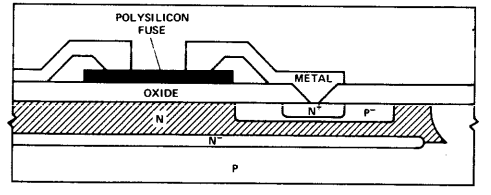


Figure 7. Polysilicon Fuse Cross Section.

The fuse is blown with a pulse train of successively wider pulses, with a current of 20–30 mA typically needed to blow the fuse. During this "blowing" operation, temperatures estimated at 1400°C are reached in the notch of the polysilicon fuse. At these temperatures, the silicon oxidizes and forms an insulating material. Figure 8 shows a blown and unblown fuse. *The use of silicon eliminates conductive dendrites and the existence of conductive materials in the fused gap.*

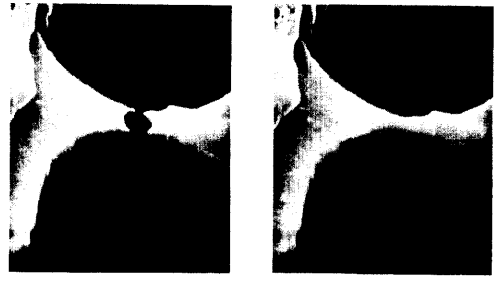


Figure 8. Blown and Unblown Polysilicon Fuse.

Since silicon is a standard integrated circuit material, no new contact problems or problems with dissimilar materials are encountered. Growback does not exist with the silicon fuse. *After 3 billion fuse hours of system life testing at 85°C, zero failures have been found.*

The Shorted Junction

A third type of bipolar PROM implementation is the shorted junction. The shorted junction cell is shown in Figures 9 and 10. In this cell, diode Q_1 is reverse-biased and the heavy flow of electrons in the reverse direction causes aluminum atoms from the emitter contact to migrate through the emitter to the base, causing an emitter-to-base short. Extreme care must be taken such that sufficient contact is made to the base without actually puncturing and shorting through the base.

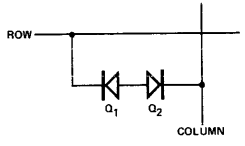


Figure 9. Schematic of Shorted Junction Cells.

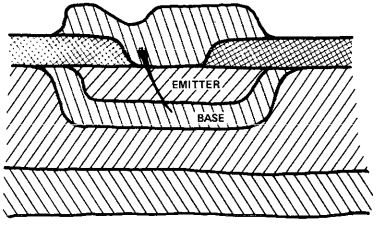


Figure 10. Cross Section of Shorted Junction Cell.

Although the shorted junction PROM does not have the reliability problems associated with the nichrome fuse, programming is greatly complicated by the fact that underprogramming results in insufficient or intermittent contact with the base and overprogramming results in possible internal shorts. The problem of distributing heavy currents around the chip requires the use of multiple-layer metalization, and, as a result, most major semiconductor companies have not committed to the shorted junction technology.

MOS Technology

FAMOS IMPLEMENTATION

As mentioned earlier, it is possible to produce PROMs and ROMs using MOS technology. In 1971 Intel introduced a unique erasable PROM that allows the programmed information to be erased by exposure to ultraviolet light of the correct wavelength and intensity.

The storage element is the Floating gate Avalanche-injection MOS (FAMOS) charge storage device, a cross section of which is shown in Figure 11. The

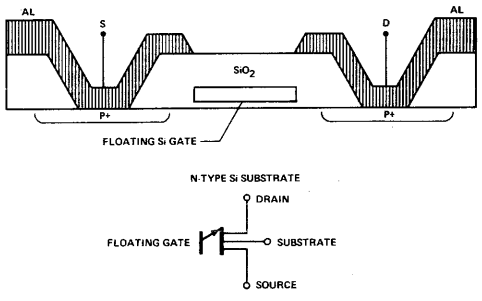


Figure 11. FAMOS Storage Cell.

operation of the cell depends on charge transport to the floating gate by avalanche injection of electrons. The device is essentially a silicon gate MOS field effect transistor in which no connection is made to the silicon gate. Operation of the FAMOS memory structure depends on charge transport to the floating gate by avalanche injection of electrons from either the source or drain. A junction voltage in excess of –30V applied to a p-channel FAMOS device will result in the injection of high-energy electrons from the p–n junction surface avalanche region to the floating silicon gate. The amount of charge transferred to the floating gate is a function of amplitude and duration of the applied junction voltage, as shown in Figure 12. The presence or absence of charge can be sensed by measuring the conductance between the source and drain.

Once the applied junction voltage is removed, no discharge path is available for the accumulated electrons since the gate is surrounded by thermal oxide, which is a very low conductivity dielectric. The electric field in the structure after the removal of junction voltage is due only to the accumulated

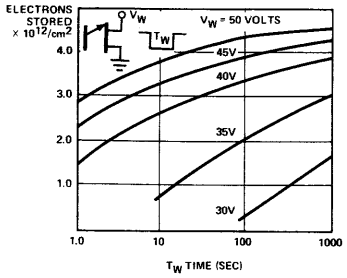


Figure 12. Charge Transfer vs. Programming Pulse Width.

electron charge and is not sufficient to cause charge transport across the polysilicon-thermal-oxide energy barrier.

Charge decay plots as a function of time at 125°C and 300°C are shown in Figure 13. An extrapolation of the 300°C charge decay results indicates that 70% of the initial induced charge will be retained for as long as 10 years at 125°C.

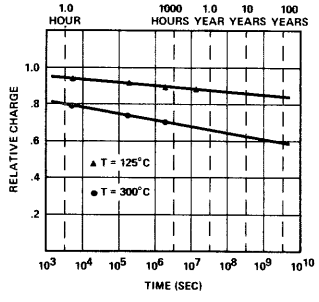


Figure 13. Charge Decay vs. Time.

Since the gate electrode is not electrically accessible, the charge cannot be removed by an electrical pulse. However, the initial condition of no electronic charge on the gate can be restored by illuminating the FAMOS device with ultraviolet light, which results in the flow of a photocurrent from the floating gate back to the silicon substrate, thereby discharging the gate to its initial condition. This erase method allows complete testing of a complex programmable read only memory array.

SPECIFIC DEVICE DESCRIPTIONS

Bipolar Devices

Intel manufacturers a complete line of bipolar PROMs and ROMs as shown in Table I, and in the Product Selection Guide, page PSG-2.

Table I. The Intel PROM/ROM Family.

	1K (256 x 4) 16-Pin		2K (512 x 4) 16-Pin		4K (512 x 8) 24-Pin	
	OC[1]	TS[2]	OC[1]	TS[2]	OC[1]	TS[2]
PROMs	3601	3621	3602	3622	3604	3624
ROMs	3301A	--	3302	3322	3304A	3324A

NOTES: 1. Open-collector output
2. Three-state output.

Each PROM is pin-for-pin compatible with its mask ROM counterpart. Programming is accomplished by "blowing" a polysilicon fuse in the emitter leg of the bipolar transistor that serves as a data storage cell. Because of the internal circuitry, the initial (unprogrammed) state of the output of the 3601 PROM is low, while the 3602/3622 and 3604/3624 devices have an initial state that produces a high output.

In the 2K and 4K sizes, the part can be ordered with either an open-collector or three-state output.

3601/3621 AND 3301A

The 3601/3621 and 3301A 1K PROM and ROM pin configuration and logic symbol are shown in

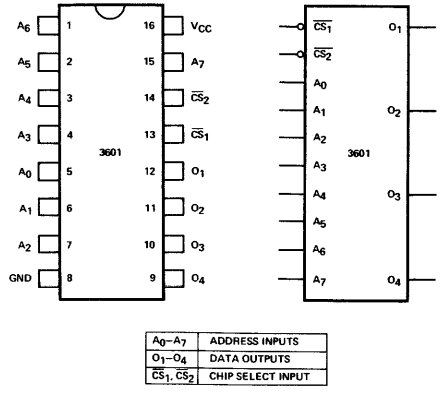


Figure 14. 3601/3621 and 3301A Pin Configuration and Logic Symbol.

Figure 14, and the address and data waveforms are shown in Figure 15. The device is organized as 256 4-bit words. The AC characteristics are summarized in Table II, and the DC characteristics in Table III. Capacitance is shown in Table IV.

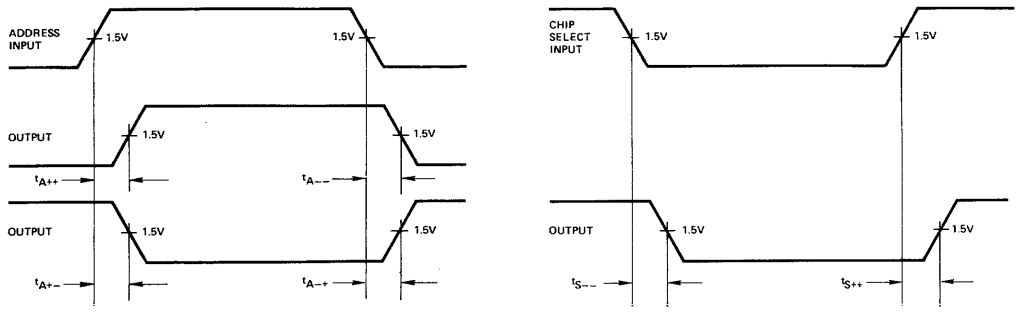


Figure 15. 3601/3301A Address and Data Waveforms.

Table II. 3601/3301A A.C. Characteristics.

SYMBOL	PARAMETER	DEVICE TYPE	LIMITS 0°C	LIMITS 25°C	LIMITS 75°C	UNIT	TEST CONDITIONS
t_{A++}, t_{A--}	Address to Output Delay	3301A	45	45	45	nS	$\overline{CS}_1$ and $\overline{CS}_2$ must be at V_{IL} to activate the PROM.
t_{A++}, t_{A-+}		3601	70	60	70	nS	
		3601-1	50	50	50	nS	
t_{S++}, t_{S--}	Chip Select to Output Delay	3301A	20	20	20	nS	
		3601	25	25	25	nS	
		3601-1	25	25	25	nS	

A simplified block diagram is shown in Figure 16, with a typical 1-bit schematic shown in Figure 17.

Addresses A_3–A_7 select 1 of 32 rows by activating 1 of 32 decoders. Each row consists of 32 cells. Addresses A_0–A_2 enable the 1 of 8 decoders, multiplexing 1 of 8 bits to the appropriate sense amplifier as shown in Figure 17. The logical AND of $\overline{CS}_2 \cdot \overline{CS}_1$ energizes all the columns in the array and provides a programming path as will be described later. $\overline{CS}_1$, which is also active low, enables each of the four output buffers.

The transistors are Schottky barrier diode clamped to allow faster switching speeds than devices fabricated with a conventional gold diffusion process.

Each of the address lines has a low voltage diode input clamp to minimize line reflections.

The outputs are open-collector, which allows them to be OR-connected for memory expansion. The capacitance of the data out pins is typically 7 pF, as shown in Table IV, or 56 pF for eight devices OR-tied together.

Programming the 3601 is accomplished by pulsing V_{CC} and $\overline{CS}_2$ with waveforms as described in the programming section. The initial (unprogrammed) state of the device is with all outputs low; that is, a bit is considered programmed when the output is high.

3602/3622 AND 3302/3322

The 3602/3622 and 3302/3322 pin configuration and logic symbol are shown in Figure 18.

The 3602/3302 has an open-collector output, while the 3622/3322 is a three-state output. A simplified block diagram of the part is shown in Figure 16. The schematic is shown in Figure 17. As indicated in Figure 16, the organization is 512 X 4 bits. Operation is analogous to the 1K PROM described earlier.

Table III. 3601/3301A D.C. Characteristics.

All limits apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	TEST CONDITIONS
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 4.0V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} 5.25V, V_S = 4.0V
V_{CA}	Address Input Clamp Voltage		-0.7	-1.0	V	V_{CC} = 4.75V, I_A = -5.0 mA
V_{CS}	Chip Select Input Clamp Voltage		-0.7	-1.0	V	V_{CC} = 4.75V, I_S = -5.0 mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15 mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC}	Power Supply Current 3601		90	130	mA	V_{CC} = 5.25V, $V_{A0} \rightarrow V_{A7}$ = 0V $V_{S0} = V_{S1}$ = 0V
	3301A		90	125	mA	
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

NOTE: 1. Typical values are at 25°C and at nominal voltage.

Table IV. 3601/3301A Capacitance[1].

SYMBOL	PARAMETER	TYP	MAX	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE: 1. This parameter is only periodically samples and is not 100% tested.

Referring to Figure 17, addresses A_3–A_8 select 1 of 64 rows, each row consisting of 32 cells. Addresses A_0–A_2 enable the 1 of 8 decoders, multiplexing 1 of 8 bits to the appropriate sense amplifier.

Chip select, $\overline{CS}$, enables the output buffer, and provides the programming path.

The 3302 and 3322 provide ROM capability for applications that have matured sufficiently to allow use of a fixed data pattern.

The 3602L-6 and 3622L-6 have the additional capability of reducing power whenever the chip is deselected; i.e., $\overline{CS}$ high. The standby power is 236mW, compared to 685mW for the 3602 and 3622.

3604/3624 AND 3304A/3324A

The 3604/3304A pin configuration and logic symbol are shown in Figure 19, and typical waveforms

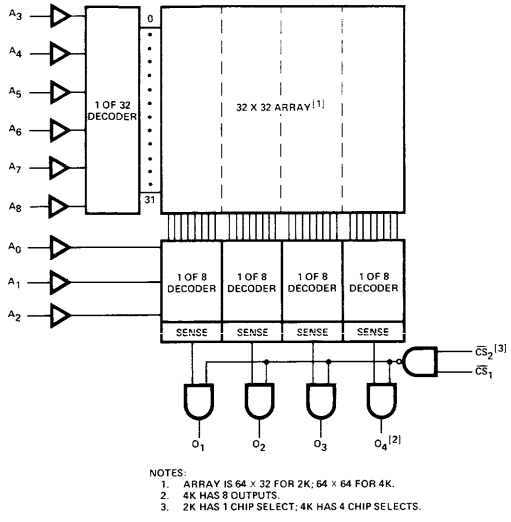
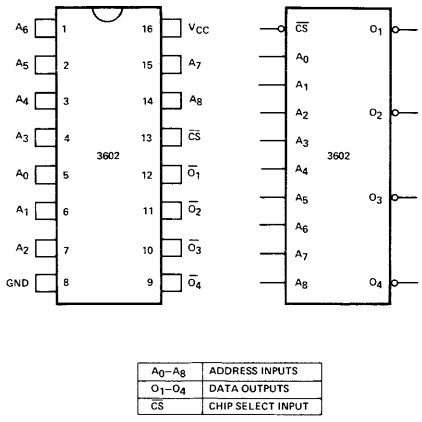


Figure 16. Simplified Bipolar PROM Block Diagram.



A_0–A_8	ADDRESS INPUTS
O_1–O_4	DATA OUTPUTS
$\overline{CS}$	CHIP SELECT INPUT

Figure 18. 3602/3622 and 3302/3322 Pin Configuration and Logic Symbol.

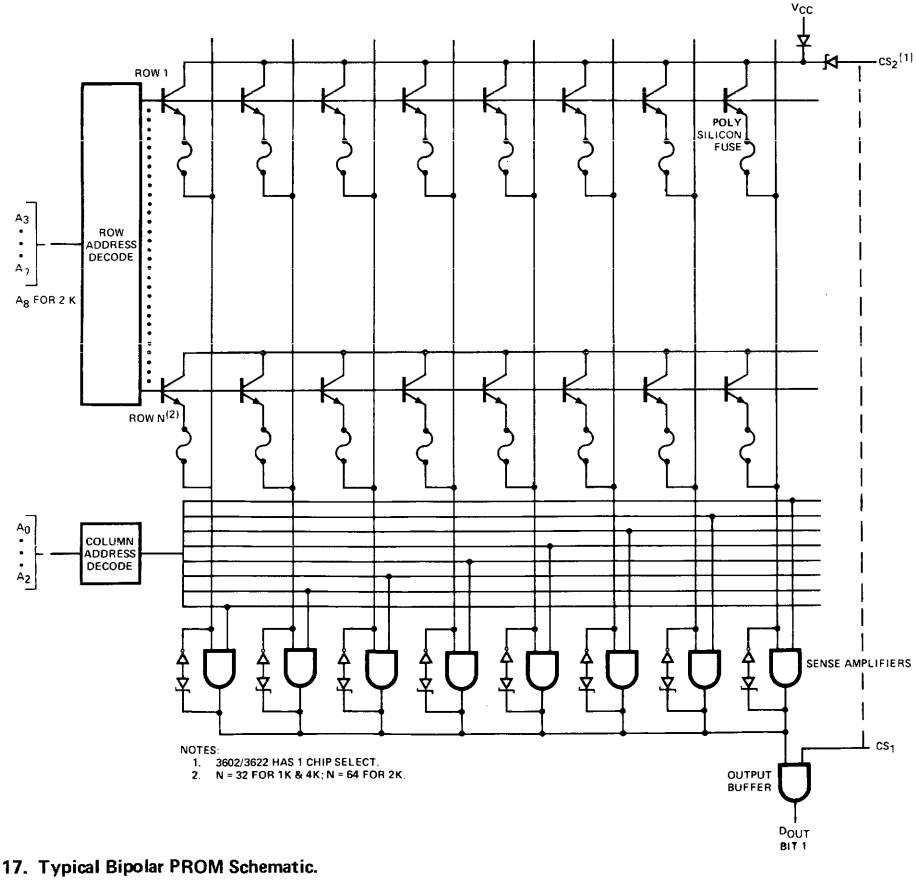


Figure 17. Typical Bipolar PROM Schematic.

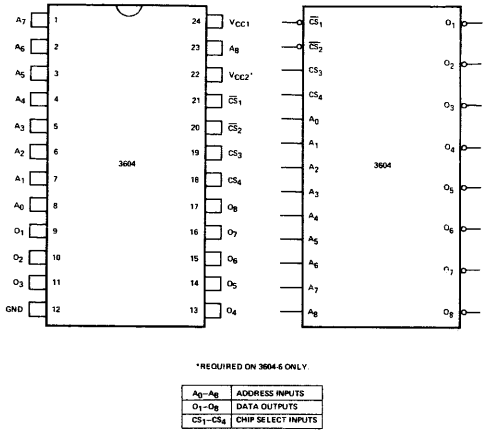


Figure 19. 3604/3304A Pin Configuration and Logic Symbol.

are shown in Figure 20. Table V summarizes the AC characteristics, with capacitance and DC characteristics summarized in Tables VI and VII, respectively.

The organization of the device is 512 X 8 bits. The basic operation of the 4K device is directly analogous to the 1K PROM as shown in Figure 17. Addresses A_3–A_8 select 1 of 64 rows, each row consisting of 64 cells. Addresses A_0–A_2 enable the decoders, multiplexing 1 of 8 bits to the appropriate sense amplifier. CS_1 provides the programming path, while $\overline{CS}_1 \cdot \overline{CS}_2 \cdot CS_3 \cdot CS_4$ provide an enable to the output. The 4-chip select terms may facilitate decoding when working with large arrays.

The 3604L-6 has the additional feature that when the chip is selected (i.e., $\overline{CS}_1$ or $\overline{CS}_2$ high), the power is reduced by approximately 70%. To utilize this feature, pins 22 and 24 must be connected as shown in Table VIII, which compares the 3604 and 3604L-6 V_{CC} connections.

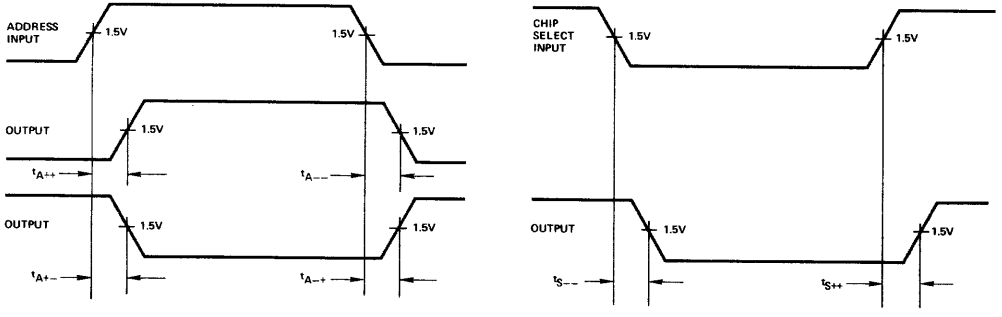


Figure 20. 3304A/3604 Address and Data Waveforms.

Table V. 3304A/3604 A.C. Characteristics.

V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER		MAX	UNIT	TEST CONDITIONS
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	3304A	70	nS	$\overline{CS}_1 = \overline{CS}_2 = V_{IL}$ and $CS_3 = CS_4 = V_{IH}$ to select the PROM.
		3604	70	nS	
		3604L-6	90	nS	
t_{S++}	Chip Select to Output Delay	3304A	30	nS	
		3604	30	nS	
		3604L-6	30	nS	
t_{S--}	Chip Select to Output Delay	3304A	30	nS	
		3604	30	nS	
		3604L-6	120	nS	

Table VI. 3304A/3604 Capacitance[1].

SYMBOL	PARAMETER	TYP	MAX	UNIT	TEST CONDITIONS
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{INS}	Chip Select Input Capacitance	6	10	pF	V_{CC} = 5V V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V V_{OUT} = 2.5V

NOTE: 1. This parameter is only periodically samples and is not 100% tested.

Table VII. 3304A/3604 D.C. Characteristics.

All limits apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	TEST CONDITIONS
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.50	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 4.0V
V_{CA}	Address Input Clamp Voltage		-0.7	-1.0	V	V_{CC} = 4.75V, I_A = -5.0 mA
V_{CS}	Chip Select Input Clamp Voltage		-0.7	-1.0	V	V_{CC} = 4.75V, I_S = -5.0 mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15 mA
I_{CEX}	Output Leakage Current			100	μA	V_{CC}= 5.25V, V_{CE} = 5.25V
I_{CC1}	Power Supply Current 3304A and 3604			190	mA	V_{CC1} = 5.25V, V_{A0}→V_{A7} = 0V CS_1 = CS_2 = 0V CS_3 = CS_4 = 5.25V
I_{CC2}	Power Supply Current (3604L-6) Active			140	mA	V_{CC2} = 5.25V, V_{CC1} = Open Chip Selected
	Standby			45	mA	Chip Deselected
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

NOTE: 1. Typical values are at 25°C and at nominal voltage.

Table VIII. 3604/3604L-6 Connections and Power Consumption.

DEVICE TYPE	CONNECTION	READ	PROGRAM	POWER
3604	Pin 22	+5V or No Connect	Pulsed 12.5V	998 mW maximum
	Pin 24	+5V	Pulsed 12.5V	
3604L-6	Pin 22	+5V	Pulsed 12.5V	735 mW maximum with chip selected
	Pin 24	No Connect[1]	Pulsed 12.5V	236 mW maximum with chip deselected

NOTE: 1. Do not connect pin 24 of the 3604L-6 to any other pin

The 3304AL6 mask ROM is available for ROM users who wish to take advantage of the power reduction feature of the reduced standby power.

MOS Devices

The Intel family of MOS PROMs and ROMs can also be divided into two groups. The 1602A/1702A, and its mask programmable counterpart, the 1302, are 2048 bit MOS devices, organized as 256 x 8 bits. The 2704 and 2708 are, respectively, 4K (512 x 8) and 8K (1024 x 8). The 2308 is the mask counterpart of the 2708. The 1702A, the 2704 and the 2708 EPROMs are all implemented with the Intel FAMOS technology.

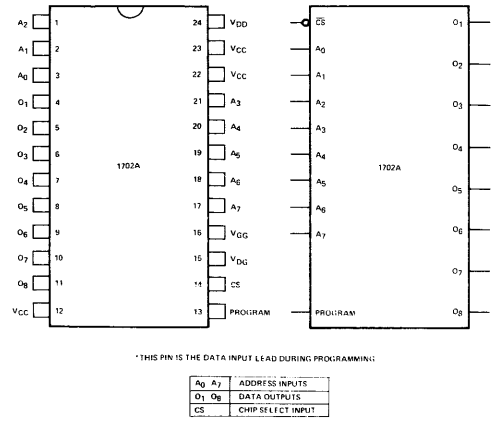


Figure 21. 1302/1602A/1702A Pin Configuration and Logic Symbol.

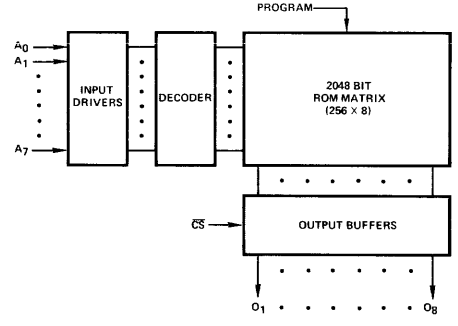


Figure 22. 1602A/1702A Block Diagram.

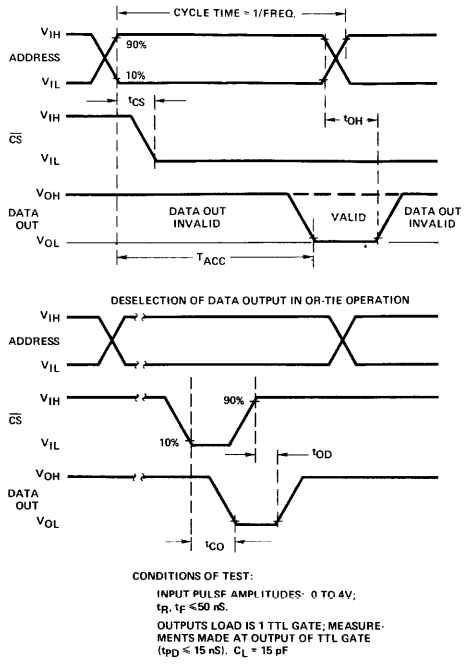


Figure 23. 1302/1602A/1702A Waveforms.

1602A/1702A/1302

The logic symbol and pin configuration for these devices is shown in Figure 21, and the block diagram is shown in Figure 22. The 1302 mask programmable device is pin for pin compatible with the electrically programmable devices.

The FAMOS data storage cell used in the 1602A/1702A is described in the technology section.

The operation and electrical characteristics of the 1602A and the 1702A are identical; the 1702A is packaged with a quartz lid to allow erasure by high intensity ultraviolet light as described in the technology chapter. The 1602A/1702A switching characteristics are shown in Figure 23, and AC and DC characteristics are summarized in Tables IX and X, respectively. Capacitance is shown in Table XI.

The operation of the 1602A/1702A is similar to the bipolar PROMs described earlier. The higher order address bits A_5–A_7 perform the row decode function, while the low order address bits provide the column decode. Chip select, $\overline{CS}$, is active low and enables the eight output buffers.

For low power applications, with the 1602AL/1702AL it is possible to clock the V_{GG} (-9V) supply, resulting in a decrease of power proportional to the V_{GG} duty cycle.

As with the bipolar PROMs, care should be taken with the number of devices that are OR-tied together such that access time is not compromised.

The initial (unprogrammed) state of the 1602A/1702A is all "0's" (output low). Programming is accomplished by writing "1's" (output high) in the proper bit locations.

Figure 24 presents various parametric curves that will assist the designer in determining worst case conditions when using the device.

Table IX. 1302/1602A/1702A A.C. Characteristics.

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG} = −9V ±5%, unless otherwise specified.

SYMBOL	PARAMETER		MIN	TYP[1]	MAX	UNIT
Frequency	Repetition Rate				1	MHz
t_{OH}	Previous Read Data Valid				100	nS
t_{ACC}	Address to Output Delay			0.7	1	µS
t_{DVGG}	Clocked V_{GG} Set Up	1602AL/1702AL 1302	1 1			µS µS
t_{CS}	Chip Select Delay	1602A/1702A 1302			100 200	nS nS
t_{CO}	Output Delay from CS	1602A/1702A 1302			900 500	nS nS
t_{OD}	Output Deselect				300	nS
t_{OHC}	Data Out Hold In Clocked V_{GG} Mode[2]				5	µS

NOTES: 1. Typical values are at 25°C and at nominal voltage.

2. The outputs will remain valid for t_{OHC} as long as clocked V_{GG} is at V_{CC}. An address change may occur as soon as the output is sensed (clocked V_{GG} may still be at V_{CC}). Data becomes invalid for the old address when clocked V_{GG} is returned to V_{GG}.

Table X. 1302/1602A/1702A D.C. and Operating Characteristics[1].

T_A = 0°C to +70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5%, V_{GG}[2] = −9V ±5%, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP[3]	MAX	UNIT	TEST CONDITIONS
I_{LI}	Address and Chip Select Input Load Current			1	µA	V_{IN} = 0V
I_{LO}	Output Leakage Current			1	µA	V_{OUT} = 0.0V, $\overline{CS}$ = V_{CC}−2
I_{DDO}	Power Supply Current		5	10	mA	V_{GG} = V_{CC}, $\overline{CS}$ = V_{CC}−2, I_{OL} = 0.0 mA, T_A = 25°C
I_{DD1}	Power Supply Current		35	50	mA	$\overline{CS}$ = V_{CC}−2, I_{OL} = 0.0 mA, T_A = 25°C
I_{DD2}	Power Supply Current		32	46	mA	$\overline{CS}$ = 0.0, I_{OL} = 0.0 mA, T_A = 25°C
I_{DD3}	Power Supply Current		38.5	60	mA	$\overline{CS}$ = V_{CC}−2, I_{OL} = 0.0 mA, T_A = 0°C
I_{CF1}	Output Clamp Current		8	14	mA	V_{OUT} = −1.0V, T_A = 0°C
I_{CF2}	Output Clamp Current			13	mA	V_{OUT} = −1.0V, T_A = 25°C
						Continuous Operation
I_{GG}	Gate Supply Current			1	µA	
V_{IL1}	Input Low Voltage for TTL Interface	−1.0		0.65	V	
V_{IL2}	Input Low Voltage for MOS Interface	V_{DD}		V_{CC}−6	V	
V_{IH}	Address and Chip Select Input High Voltage	V_{CC}−2		V_{CC}+0.3	V	
I_{OL}	Output Sink Current	1.6	4		mA	V_{OUT} = 0.45V
I_{OH}	Output Source Current	−2.0			mA	V_{OUT} = 0.0V
V_{OL}	Output Low Voltage		−0.7	0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	3.5	4.5		V	I_{OH} = −100 µA

NOTES: 1. In the programming mode, data inputs 1–8 are pins 4–11, respectively; $\overline{CS}$ = GND.

2. V_{GG} may be clocked to reduce power dissipation. In this mode average I_{DD} decreases in proportion to V_{GG} duty cycle.

3. Typical values are at 25°C and at nominal voltage.

Table XI. 1302/1602A Capacitance.

$T_A = 25°C$

SYMBOL	PARAMETER		TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance	1302	5	10	pF	$V_{IN} = V_{CC}$ $\overline{CS} = V_{CC}$ $V_{OUT} = V_{CC}$ $V_{GG} = V_{CC}$ All unused pins are at AC ground.
		1602A/1702A	8	15	pF	
C_{OUT}	Output Capacitance	1302	5	10	pF	
		1602A/1702A	10	15	pF	
C_{VGG}	V_{GG} Capacitance (Clocked V_{GG} Mode)			30	pF	

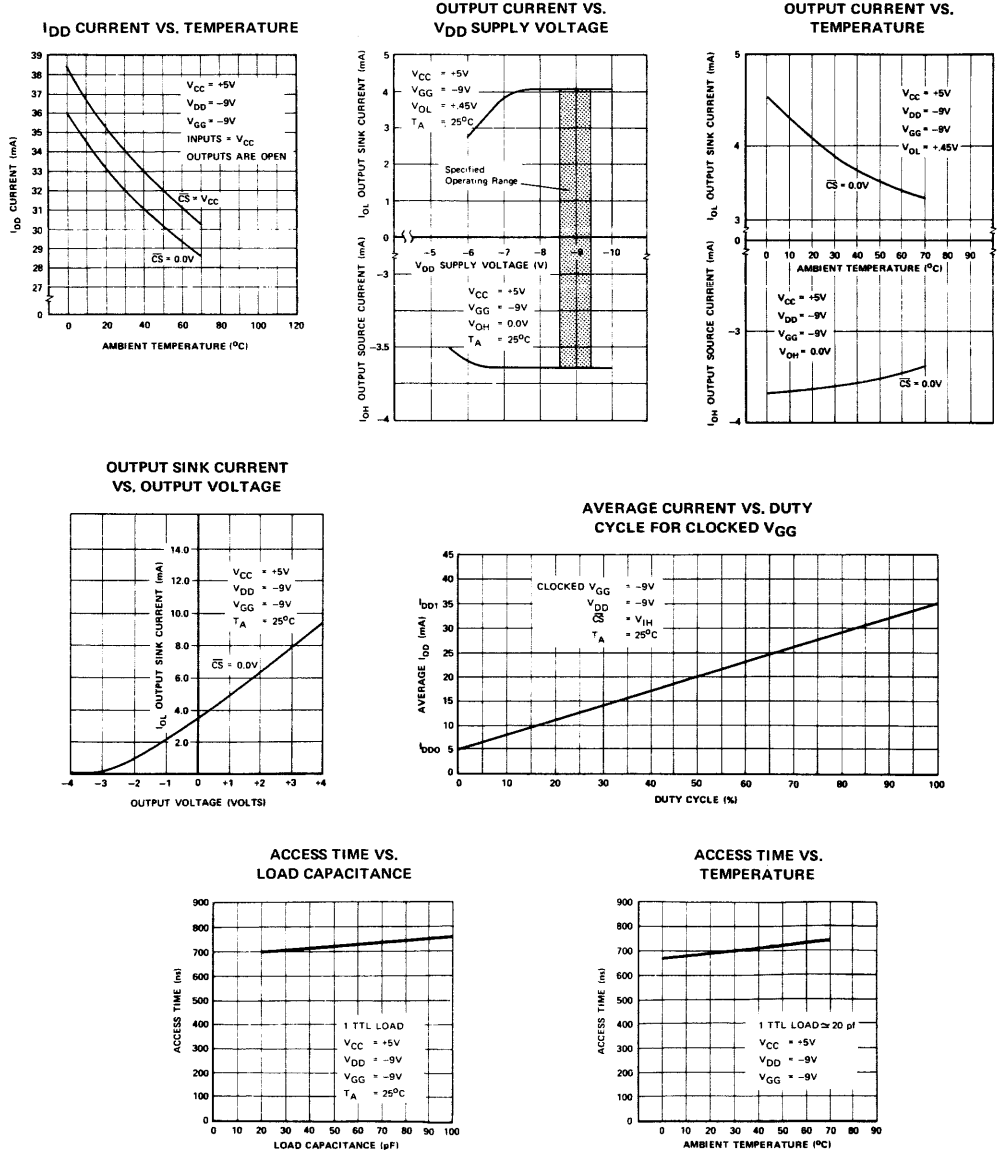


Figure 24. 1602A/1702A Parametric Curves.

PROGRAMMING

All of the PROMs described earlier require that data be entered by a technique different from that required to read. There are two ways of programming a PROM; one is to satisfy the control requirements for a particular address, apply some sort of pulsed voltage to the appropriate connection, and proceed to the next location. The other is to put the information on a mark/sense card or paper tape and give it to somebody. Both methods are presented here.

PROGRAMMING THE 1K BIPOLAR PROM (3601)

The 3601 may be programmed using the basic circuit of Figure 25. Address inputs are at standard TTL levels. Only one output may be programmed at a time. The output to be programmed must be connected to V_{CC} through a 300Ω resistor. This will force the proper programming current (3-6mA) into the output when the V_{CC} supply is later raised to 10V. All other outputs must be held at a TTL low level (0.4V maximum).

The programming pulse generator produces a series of pulses to the 3601 V_{CC} and $\overline{CS}_2$ leads as shown in Figure 26 V_{CC} is pulsed from a low of 4.5V ±0.25V to a high of 10V ±0.25V, while $\overline{CS}_2$ is pulsed from a low of ground (TTL logic 0) to a high of 15V ±0.25V. It is important to accurately maintain these voltage levels; otherwise, improper programming may result.

The pulses applied must maintain a duty cycle of 50% ±10%, and start with an initial width of 1 μS ±10%, *and increase linearly over a period of approximately 100 mS* to a maximum width of 8 μS ±10%. Typical devices have their fuse blown within 1 mS, but occasionally a fuse may take up to 400 mS to blow.

During the application of the program pulse, current to $\overline{CS}_2$ must be limited to 100 mA. The output of the 3601 is sensed when $\overline{CS}_2$ is at a TTL low level output. A programmed bit will have a TTL high output. After a fuse is blown, the V_{CC} and $\overline{CS}_2$ pulse trains must be applied for another 500 μS

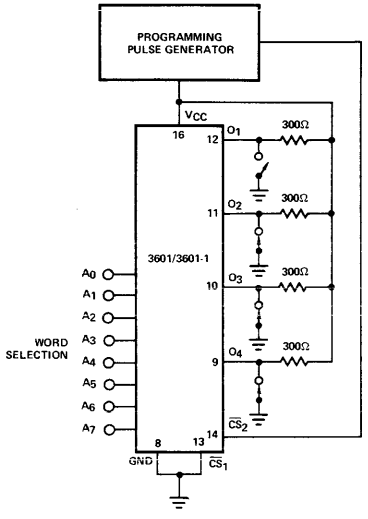


Figure 25. 3601 Programming Connections.

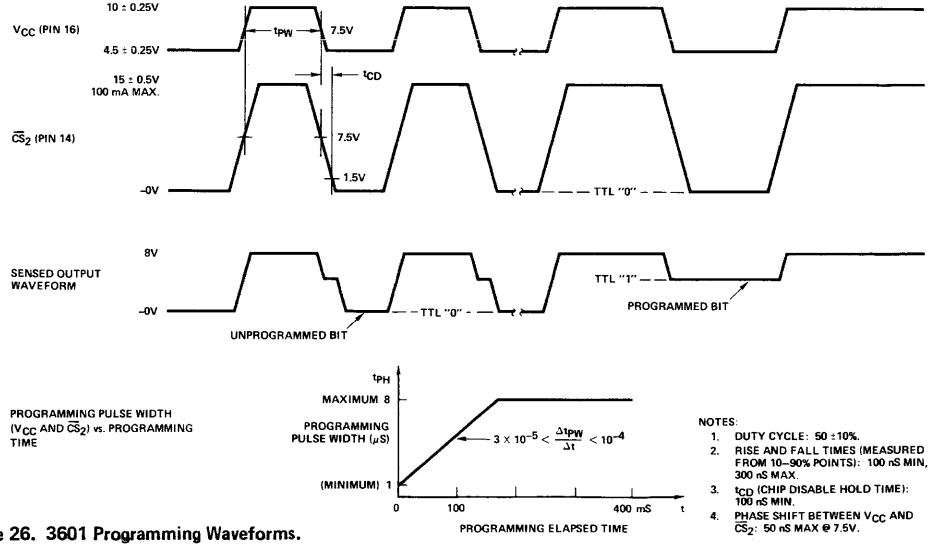


Figure 26. 3601 Programming Waveforms.

PROGRAMMING THE 2K AND 4K BIPOLAR PROMs (3602/3622 AND 3604/3624) [1]

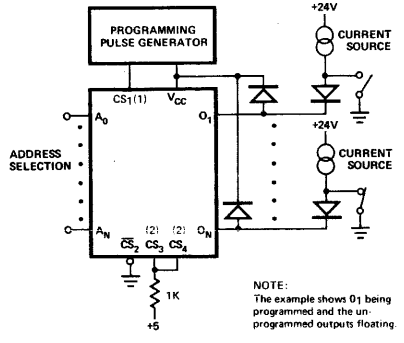
The 3602/3622 and 3604/3624 parts are also programmed by forcing current into the output, but with the 3622 and 3624, the three-state outputs that are not being programmed must be allowed to float. Figure 27 shows the basic circuit for programming the 2K and 4K family of PROMs.

The programming current that must be provided to each output is 5 mA ±10% for the 3602/3622 and 3604/3624.

The low standby power devices can be programmed in the same way, the only differences being that V_{CC1}, V_{CC2}, and $\overline{CS}_1$ must be connected and pulsed in accordance with Table XII and Figure 28. Note that pin 24 of the 3604L-6 must not be connected to any other pin, or the power down circuit will not operate.

Note that the V_{CC1} and V_{CC2} programming levels are 12.5V ±0.5V for the 3602, 3604, 3622, and 3624.

1. The 3621 is also programmed by this technique.



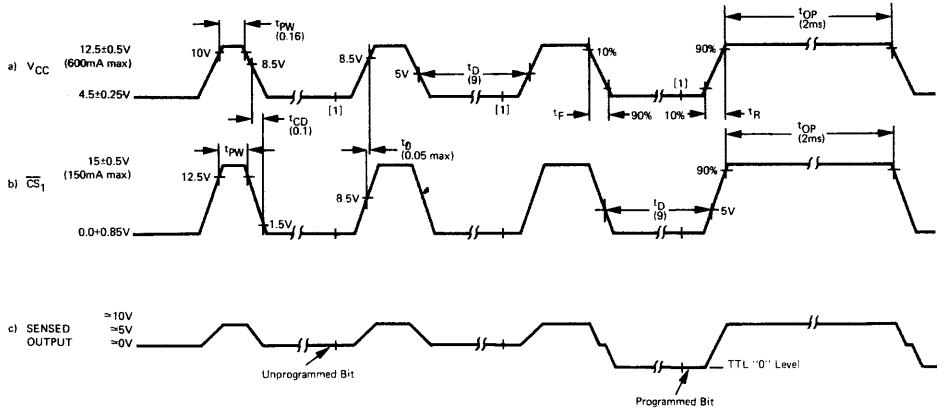
NOTES:
1. For the 3621 and 3605/3625 family only the program pulse may be applied to either CS_1 or CS_2.
2. CS_3, CS_4 are only for the 3604/3624 PROM family.

Figure 27. 3621, 2K and 4K Bipolar PROM Programming Connections.

Table XII. 3604/3604AL6 Programming Connections.

MODE \ PIN		22 V_{CC2}	24 V_{CC1}
READ	3604	No Connect or +5V	+5V
	3604L-6	+5V	No Connect [1]
PROGRAM	3604	Pulsed 12.5V	Pulsed 12.5V
	3604L-6	Pulsed 12.5V	Pulsed 12.5V
STANDBY POWER	3604L-6	Power dissipation is automatically reduced whenever the 3604L-6 is deselected.	

NOTE: 1. Do not connect pin 24 of the 3604L-6 to any other pin



[1] Data Sense Time should be at 90% (or greater) of t_D. A bit is considered programmed after 128 successful verifications. The program pulses should continue to increase in accordance with the ramp shown above. After 128 successful verifications, the DC over program time can start.

NOTE: All times in parenthesis are in microseconds and are in minimum times unless otherwise specified.

Figure 28. 3602/3622 and 3604/3624 Programming Waveforms.

Programming the 1602A/1702A

In its initial state the 1602A/1702A array will have all outputs low. Programming is accomplished by writing highs in the proper bit locations. The peak I_{DD} current that must be provided for programming the 1602A/1702A is approximately 200 mA, and the entire device can be programmed in about 2 minutes. Figure 29 shows the waveforms required for programming, while Table XIII shows the connections used. Table XIV and XV show the A.C. and D.C. characteristics for programming.

During programming, V_{CC} should be held at ground and V_{BB} should be held at +12V. Address levels are approximately –40V for a logic "0" (output low), and approximately 0V for a logic "1" (output high). Note that these levels are larger in magnitude but in the same polarity sense as those used for reading from the memory:

logic "0": -1V≤ logic "0" ≤.65V,

logic "1": ≥ V_{CC} -2

where V_{CC} = 5V ±5%.

When programming, the negative-going power supplies (V_{DD}) must be pulsed. V_{DD} is pulsed to –47V ±1V. V_{GG} is brought to -35 to -40V, and the complement of the address to be programmed is applied. After the power has been applied for at least 25μS, the address must be returned to its true form 10μS or more after the address has reached its true state, and at least 100 μS after turning on power, the 3 mS program pulse (pin 13) at –47V ±1V may be applied. During the interval when V_{DD} is applied, data signals must be applied to the data output lines. A data level of approximately 0V will result in the location remaining unchanged, while a level of –47V ±1V will program a logic "1" (output high in read mode). After the program pulse is turned off, the V_{DD} and V_{GG} voltages should be turned off. This turn-off should occur from 10–100μS after removal of the program pulse.

For best results, the 1602A/1702A should be programmed by scanning through the addresses in binary sequence 32 times. Each pass repeats the same series of programming pulses. The duty cycle for applied power must not exceed 20%. As a re-

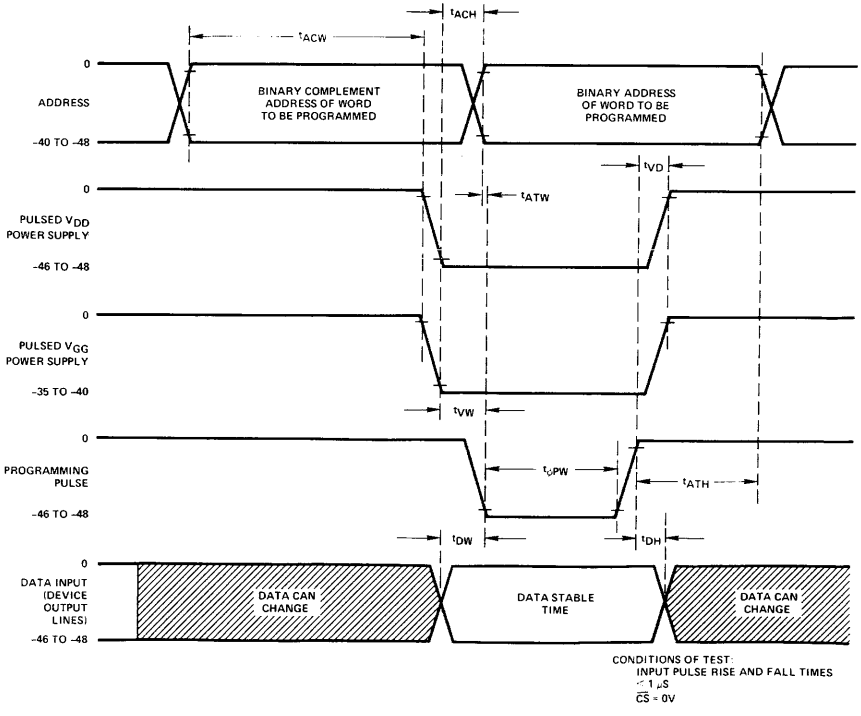


Figure 29. 1602A/1702A Programming Waveforms.

sult, each pass takes about 4 seconds, with the 32 passes taking just over 2 minutes.

ERASING THE 1702A

The 1702A EPROM may be erased by exposure to high intensity, short-wave ultraviolet light at a wavelength of 2537 Angstroms. The recommended integrated dose (i.e., UV intensity X intensity time) is 6W-sec/cm^2. The devices are made with a transparent quartz lid covering the silicon die. Conventional room light, fluorescent light, or sunlight has no measurable effect on stored data, even after years of exposure. However, after 10–20 minutes under a suitable source, the device is erased to a state of all "0's" (outputs low). To prevent damage to the device, it is recommended that no more ultraviolet light exposure be used than that necessary to erase the 1702A.

CAUTION

When using an ultraviolet source of this type, care should be taken not to expose the eyes or skin to the ultraviolet rays, as damage to vision or burns may occur. Also, these short-wave rays may generate considerable amounts of ozone which is potentially hazardous.

Table XIII. 1602A/1702A Programming Connections.

MODE \ PIN	12 (V_{CC})	13 (Program)	14 (CS)	15 (V_{BB})	16 (V_{GG})	22 (V_{CC})	23 (V_{CC})
Read	V_{CC}	V_{CC}	GND	V_{CC}	V_{GG}	V_{CC}	V_{CC}
Programming	GND	Program Pulse	GND	V_{BB}	Pulsed V_{GG} (V_{IL4P})	GND	GND

Table XIV. 1602A/1702A D.C. and Operating Characteristics for Programming Operation.

T_A = 25°C, V_{CC} = 0V, V_{BB} = +12V ± 10%, $\overline{CS}$ = 0V unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{LI1P}	Address and Data Input Load Current			10	mA	V_{IN} = −48V
I_{LI2P}	Program and V_{GG} Load Current			10	mA	V_{IN} = −48V
I_{BB}	V_{BB} Supply Load Current		10		mA	
I_{DDP}(1)	Peak I_{DD} Supply Load Current		200		mA	V_{DD} = V_{prog} = −48V V_{GG} = −35V
V_{IHP}	Input High Voltage			0.3	V	
V_{IL1P}	Pulsed Data Input Low Voltage	−46		−48	V	
V_{IL2P}	Address Input Low Voltage	−40		−48	V	
V_{IL3P}	Pulsed Input Low V_{DD} and Program Voltage	−46		−48	V	
V_{IL4P}	Pulsed Input Low V_{GG} Voltage	−35		−40	V	

Note 1: I_{DDP} flows only during V_{DD}, V_{GG} on time. I_{DDP} should not be allowed to exceed 300mA for greater than 100μsec. Average power supply current I_{DDP} is typically 40mA at 20% duty cycle.

2. The V_{BB} supply must be limited to 100mA max current to prevent damage to the device.

Table XV. 1602A/1702A A.C. Characteristics for Programming Operation.

T_A = 25°C, V_{CC} = 0V, V_{BB} = + 12V ± 10%, $\overline{CS}$ = 0V unless otherwise noted

SYMBOL	TEST	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Duty Cycle			20	%	
$t_{\phi PW}$	Program Pulse Width			3	ms	V_{GG} = −35V, V_{DD} = V_{prog} = −48V
t_{DW}	Data Set Up Time	25			μs	
t_{DH}	Data Hold Time	10			μs	
t_{VW}	V_{DD} , V_{GG} Set Up	100			μs	
t_{VD}	V_{DD} , V_{GG} Hold	10		100	μs	
t_{ACW} [3]	Address Complement Set Up	25			μs	
t_{ACH} [3]	Address Complement Hold	25			μs	
t_{ATW}	Address True Set Up	10			μs	
t_{ATH}	Address True Hold	10			μs	

Note 3. All 8 address bits must be in the complement state when pulsed V_{DD} and V_{GG} move to their negative levels. The addresses (0 through 255) must be programmed as shown in the timing diagram for a minimum of 32 times.

Programmers

Table XVI summarized some of the available programmers that support Intel PROMs. Specific questions regarding prices, availability, and options should be directed to the particular manufacturer.

Programmed Parts

All of the electrically programmable parts manufactured by Intel can be programmed by the end user with Intel approved equipment, or can be ordered from local distributors who are equipped with programmers compatible with each device type. In general, orders for less than 1000 pieces of programmed PROMs should be handled by local distributors, while orders for greater than that quantity should be referred to the factory. In either case, the data must be prepared in accordance with the following paragraphs.

Programming information should be sent in the form of computer punched cards or punched paper tape. In all cases, the order should be accompanied by a printout of the truth table.

The following general format is applicable to the programming information sent to Intel:

1. A data field should start with the most significant bit (O_8) and end with the least significant bit (O_1).
2. The data field should consist of P's and N's. P indicates a high level output (most positive), and N a low level output (most negative). If the programming information is sent on a punched paper tape, a start character (B) and an end character (F) must be used in the data field.

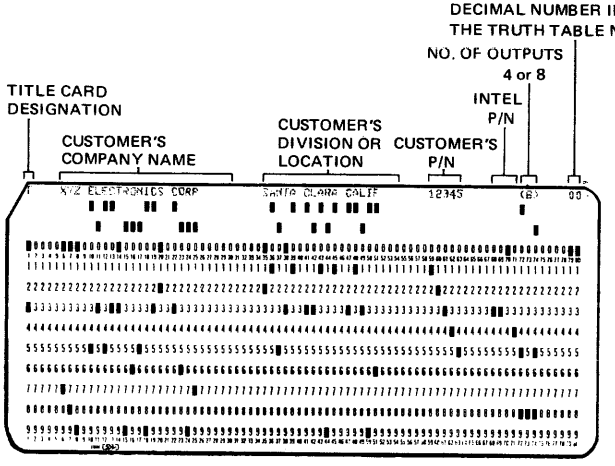
Table XVI. Approved Programmers.

	1602A/1702A Family	2704 Family	2708 Family	3601 Family	3602/3622 Family	3604/3624 Family
Intel MDS-UPP-100 Santa Clara, Calif.	X	X	X	X	X	X
Data I/O Model V Issaquah, Wash.	X	X	X	X	X	X
Prolog Series 90 Monterey, Calif.	X	Note 1	Note 1	X	X	X
Spectrum Dynamics Series 550 Burlington, Mass.	X	Note 1	Note 1	Note 1	Note 1	Note 1

Note 1. This programming card is pending Intel approval.

PUNCHED CARD FORMAT

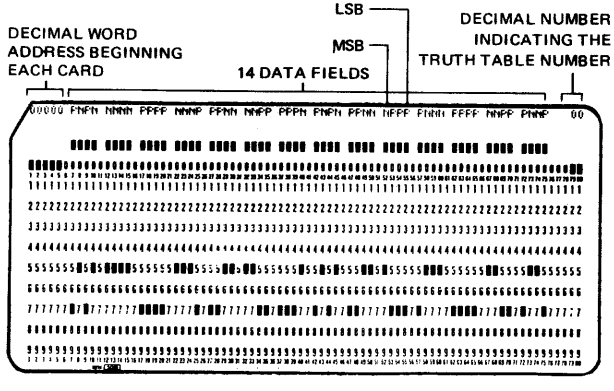
1. An 80-column Hollerith card (preferably interpreted at time of punching) punched by an IBM 026 or 029 keypunch should be submitted. The first card will be a title card, formatted as shown in Figure 30.
2. For a N words X 4-bit organization only, card 2 and the following cards should be punched as shown in Figure 31. Each card specified the 4-bit output of 14 words.
3. For a N words X 8-bit organization only, card 2 and the following cards should be punched as shown in Figure 32. Each card specifies the 8-bit output of eight words.



Column	Data
1	Punch a T
2-5	Blank
6-30	Customer Company Name
31-34	Blank
35-54	Customer's Company Division or location
55-58	Blank
59-63	Customer Part Number
64-67	Blank
68-74	Punch the Intel® 4-digit basic part number and in ( ) the number of output bits; e.g., 1702 (8), 3304 (8), 3301 (4), or 3601 (4).
75-78	Blank
79-80	Punch a 2 digit decimal number to identify the truth table number. The first truth table will be ØØ, second Ø1, third Ø3, etc.

Figure 30. Title Card Format.

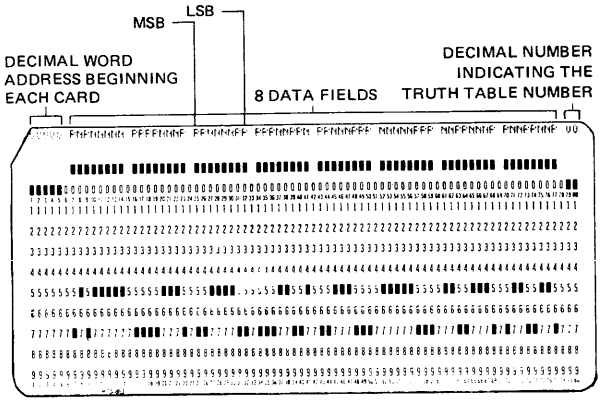
For a N words X 4-bit organization only, cards 2 and those following should be punched as shown. Each card specifies the 4-bit output of 14 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., ØØØØØ, ØØØ14, ØØØ28, etc.
6	Blank
7-10	Data Field
11	Blank
12-15	Data Field
16	Blank
17-20	Data Field
21	Blank
22-25	Data Field
26	Blank
27-30	Data Field
31	Blank
32-35	Data Field
36	Blank
37-40	Data Field
41	Blank
42-45	Data Field
46	Blank
47-50	Data Field
51	Blank
52-55	Data Field
56	Blank
57-60	Data Field
61	Blank
62-65	Data Field
66	Blank
67-70	Data Field
71	Blank
72-75	Data Field
76-78	Blank
79-80	Punch same 2 digit decimal number as in title card.

Figure 31. 4-Bit Data Card Format.

For a N words X 8-bit organization only, cards 2 and those following should be punched as shown. Each card specifies the 8-bit output of 8 words.



Column	Data
1-5	Punch the 5 digit decimal equivalent of the binary coded location which begins each card. The address is right justified, i.e., ØØØØØ, ØØØØ8, ØØØ16, etc.
6	Blank
7-14	Data Field
15	Blank
16-23	Data Field
24	Blank
25-32	Data Field
33	Blank
34-41	Data Field
42	Blank
43-50	Data Field
51	Blank
52-59	Data Field
60	Blank
61-68	Data Field
69	Blank
70-77	Data Field
78	Blank
79-80	Punch same 2 digit decimal number as in title card.

Figure 32. 8-Bit Data Card Format.

PAPER TAPE FORMAT (Figure 33)

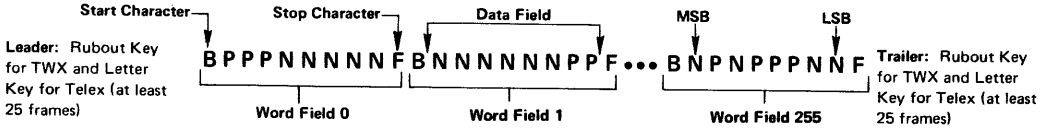
1. 1 inch-wide paper tape using 7- or 8-bit ASCII code, such as a model 33 ASR Teletype produces or
2. 11/16-inch-wide paper tape using a 5-bit Baudot code, such as a Telex produces.

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the N X 8 or N X 4 ROM organization.
2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 or 4 data characters between the B and F for the N X 8 or N X 4 organization, respectively.

   No other characters, such as rubouts, are allowed anywhere in a word field. If in preparing the tape an error is made, the entire word field, including the B and F must be rubbed out. Within the word field, a P results in a high level output, and an N results in a low level output.
3. Preceding the first word field and following the last word field, there must be a leader/trailer length of at least 25 characters. This should consist of rubout punches (letter key for Telex tapes).
4. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc., are inserted, the tape may be easily listed on the Teletype for purposes of error checking. The customer may also find it helpful to insert the word number (as a comment) at least every four word fields.
5. Included in the tape before the leader should be the customer's complete Telex or TWX number, and, if more than one pattern is being transmitted, the ROM pattern number.
6. MSB and LSB are the most and least significant bits of the device outputs. Refer to the data sheet for the pin numbers.

Example of 256 X 8 format (N = 256):



Example of 512 X 4 format (N = 2048):

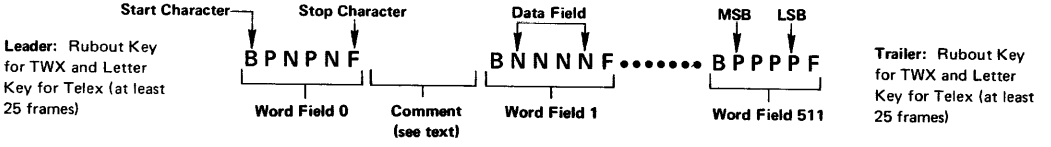


Figure 33. Paper Tape Format.

SYSTEM APPLICATIONS

System Organization

Most PROM/ROM devices contain 1K, 2K, or 4K bits and are organized as 256 or 512 locations with 4 or 8 bits per word, as shown in Figure 34. The implementation of most PROM/ROM systems requires that one or more of these devices be interconnected to provide the required number of locations and the number of bits per location.

NUMBER OF LOCATIONS	BITS PER LOCATION	
	4	8
256	3301 3601/21	1302 1602A 1702A
512	3302/22 3602/22	3304A/24 3604/24

Figure 34. PROM/ROM Device Organizations.

WORD EXPANSION

The simplest type of expansion involves the paralleling of devices to increase the number of bits per word, otherwise known as word expansion.

This type of expansion is illustrated in Figure 35, where two 3601's are paralleled to produce a 256 X 8-bit memory. The number of parallel devices can easily be calculated from the following formula:

$$\text{No. of Devices} = \frac{\text{No. of Bits per Word of the System}}{\text{No. of Bits per Word of the Device}}$$

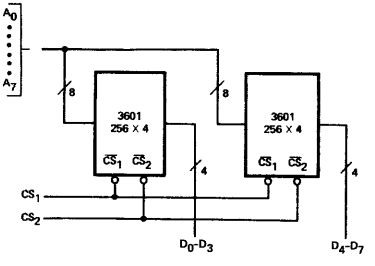


Figure 35. Word Expansion.

Therefore, a system employing a 32-bit word would require the paralleling of eight 3601's or 3602's, or four 3604's.

Word expansion requires nothing more than the parallel connection (i.e., tying together) of each individual address and chip select input; outputs remain separate.

ADDRESS EXPANSION

Just as inputs are OR-tied to obtain more bits per word, outputs can be OR-tied to obtain more words of memory (see Figure 36). When OR-tying outputs, it is necessary to select only one chip at a time to insure that the correct data is accessed. This requires the addition of logic to decode addresses and to activate the chip select for a single memory address.

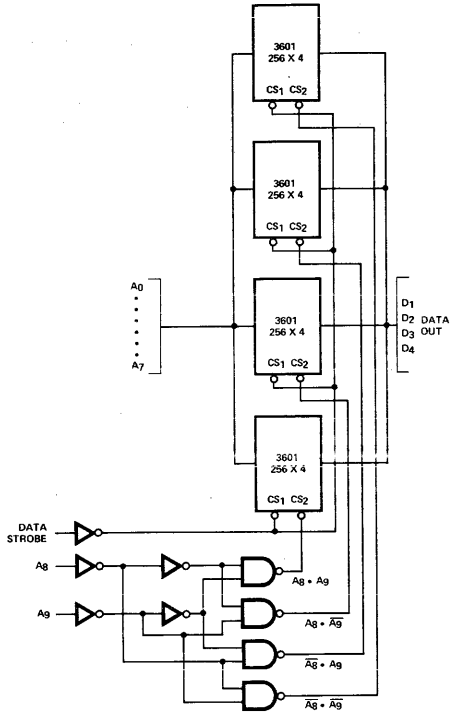


Figure 36. Address Expansion.

The number of devices required to obtain a given number of words of memory can be calculated from the following formula:

$$\text{No. of Devices} = \frac{\text{No. of Words Required in the System}}{\text{No. of Words in the Device}}$$

A system requiring 1024 words would require four 3601's, or two 3602's or 3604's.

ARRAY CONFIGURATIONS

Word expansion and address expansion can obviously be combined to produce a memory array of any size, provided the array size is an integral multiple of the device size.

Figure 37 shows a memory array configured by OR-tying inputs to obtain word expansion and OR-tying outputs to expand the number of words.

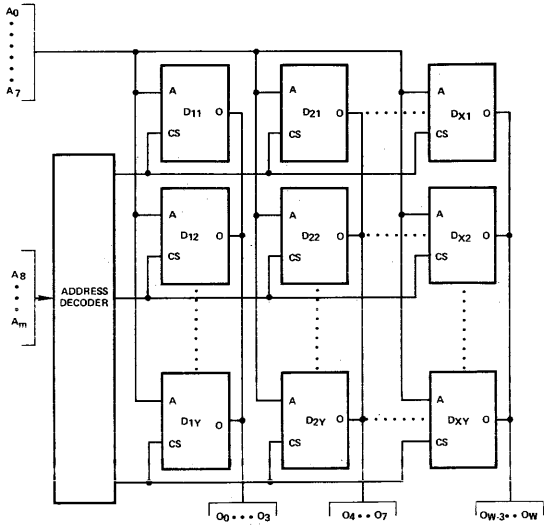


Figure 37. Combined Word and Address Expansion.

System Performance

The paralleling of inputs and outputs in memory array configurations affects capacitive loading and, therefore, system performance. Analysis of these loading effects requires consideration of buffers for driving the PROM/ROM inputs, as well as the output drive characteristics of the memory devices themselves.

BUFFERS

Buffers for driving address and chip select inputs are generally TTL devices. The effect of capacitive loading on standard, high speed, and Schottky TTL devices is shown in Figure 38.

The degradation in buffer propagation delay is directly due to increased transition time under increased capacitive loads. Figure 39 consists of

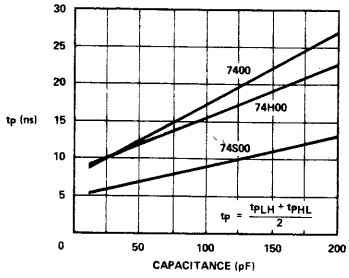


Figure 38. Capacitance vs. Propagation Time (tp).

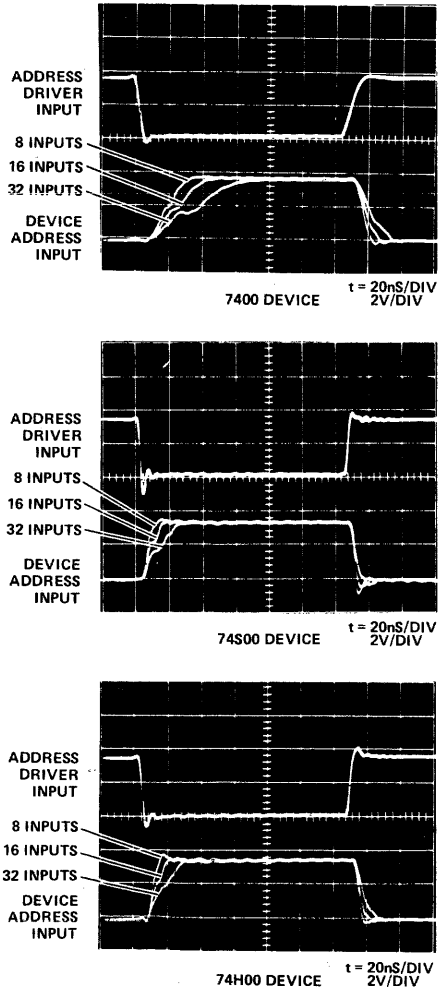


Figure 39. Various Standard TTL Devices Driving 8, 16 and 32 3601 Address Inputs.

multiple exposed photographs showing the effects of increased capacitive loads on different families of TTL gates. Figure 40 shows the same results for an increased number of chip select loads.

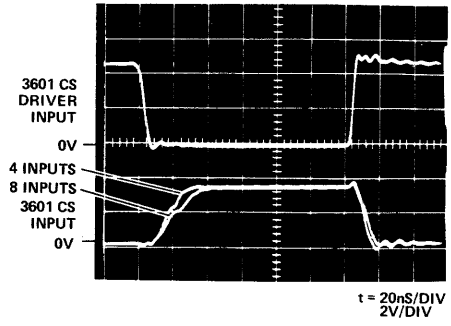


Figure 40. Input and Output of 7400 Driving 4 and 8 3601 $\overline{CS}$ Inputs.

OUTPUT LOADING

Address expansion by PROM/ROM output OR-tying increases the capacitive load on each PROM/ROM output, and results in some reduction in device access time. Figure 41 shows that going from two outputs to four outputs OR-tied increases access typically by 4 nS. The access times of the Intel bipolar PROM/ROMs are specified with a capacitive load of 30 pF, which is equivalent to the typical capacitive of output OR-tying four devices. The OR-connection of any fewer devices can reduce access time.

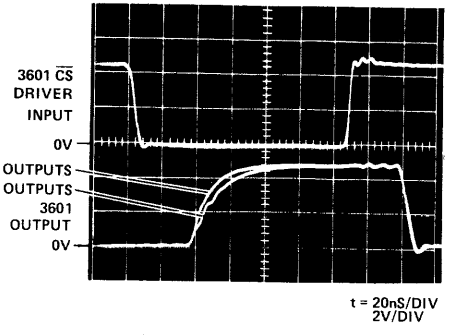


Figure 41. 2 and 4 3601 Outputs OR-Tied.

Another consideration when OR-tying outputs of PROMs and ROMs is the case where n-channel and p-channel devices must be tied together. Consider the microprocessor system shown in Figure 55. If the ROM were a p-channel 1702A and the RAM an Intel n-channel 2102A, a problem could occur. The 1702A has negative supply of -9V, and if its output pulls the 2102A output below V_{SS}-0.8V, the output circuit of the 2102A can be destroyed because of forward biasing the drain–substrate junction. A method of providing protection is to use an exclusive OR gate as shown in Figure 42. In this case, the value of R_1, the current limiting resistor, is determined by the maximum sink current drawn by the ROM and the maximum acceptable (most positive) low level required for the input of the exclusive OR gate.

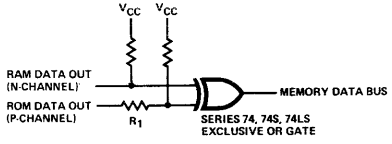
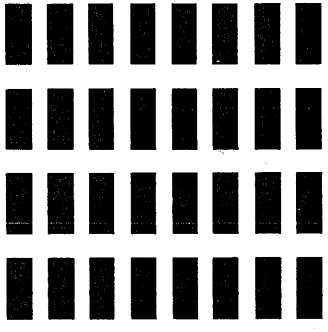


Figure 42. OR-Connecting P-Channel and N-Channel Devices.

Referring to the product selection guide, the required speed of 100 nS dictates the use of a bipolar device, eliminating the MOS devices. The 3601, 3602/3622, and 3604/3624 are all possible candidates for use in this system implementation. The system design resulting from the use of these three product types will be compared.

The system must be implemented using combinations of word expansion and address expansion as shown in Figure 37. Array layouts for these three parts are compared in Figures 43, 44, and 45. Each layout was done using the same rules: 0.200-inch adjacent spacing and 0.300-inch end-to-end spacing.



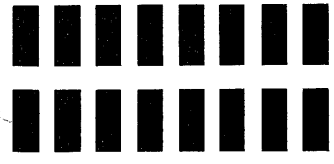
32 DEVICE ARRAY = 3.7 X 3.8 = 14.06 SQUARE INCHES
OR 2276 BITS/SQUARE INCH

Figure 43. 1K x 32-Bit System with 1K PROM (16-Pin Package).

Case Study

The selection of a memory device for a system implementation can be illustrated by the consideration of a hypothetical 1K X 32 PROM system, such as would be used for a computer microprogram control memory. Access time requirements for this system are assumed to be less than 100 nS.

The number of words required is specified as 1K, which allows the use of any device that is organized such that its number of words in the device divided into the required number of words for the system is an integer. For this application, 256 or 512 word organization would be possible devices. In a similar manner, a 4-bit or 8-bit device will allow an integral number of devices to be used to form the required 32-bit word.



16 DEVICE ARRAY = 1.7 X 3.8 = 6.46 SQUARE INCHES
OR 4953 BITS/SQUARE INCH

Figure 44. 1K x 32-Bit System with 2K PROM (16-Pin Package).

8 DEVICE ARRAY = 5.9 X 1.4 = 8.26 SQUARE INCHES

OR 3874 BITS/SQUARE INCH

Figure 45. 1K x 32-Bit System with 4K PROM (22-Pin Package).

Performance comparisons require the investigation of capacitive loading effects and device access times. Table XVII compares the number of address lines tied together, the resulting capacitance, and the resulting TTL delays for the three devices under consideration. Table XIX makes the same comparison for the chip select inputs, and Table XIX compares output loading effects. Total array power dissipation is summarized in Table XX and the complete results of the three different designs are summarized in Table XXI.

As can be seen in Table XXI, fastest system access time is achieved with the 3601, smallest printed circuit board layout area is realized with the 3602/3622, and the 3604 provides lowest system power dissipation. Selection of the optimum device is therefore left to other system development or cost considerations since all three parts are more than adequate for the stated system requirements.

Table XVII. Address Input Loading.

DEVICE SIZE	NO. OF DEVICES REQUIRED	NO. OF ADDRESS INPUTS DRIVEN	TYPICAL INPUT CAPACITANCE/ DEVICE	TOTAL CAPACITANCE	MEASURED ADDRESS DRIVER DELAY
1K	32	32	4 pF	128 pF	22 nS
2K	16	16	4 pF	64 pF	16 nS
4K	8	8	4 pF	32 pF	12 nS

Table XVIII. Chip Select Input Loading.

DEVICE SIZE	NO. OF DEVICES REQUIRED	NO. OF CHIP SELECT LINES OR-TIED	TYPICAL INPUT CAPACITANCE/ DEVICE	TOTAL CAPACITANCE	MEASURED CHIP SELECT DRIVER DELAY
1K	32	8	6 pF	48 pF	16 nS
2K	16	8	6 pF	48 pF	16 nS
4K	8	4	6 pF	24 pF	12 nS

Table XIX. Output Loading.

DEVICE SIZE	NO. OF DEVICES REQUIRED	NO. OF OUTPUTS OR-TIED	TYPICAL OUTPUT CAPACITANCE/ DEVICE	TOTAL CAPACITANCE	MEASURED OUTPUT DELAY	OUTPUT OR-ING DELAY
1K	32	4	7 pF	28 pF	32 nS	4 nS
2K	16	2	7 pF	14 pF	28 nS	0 nS
4K	8	2	7 pF	14 pF	28 nS	0 nS

Table XX. Power Dissipation.

DEVICE SIZE	NO. OF DEVICES REQUIRED	POWER DISSIPATION (TYPICAL)		REDUCED POWER MODE (MAXIMUM)	
		mW PER DEVICE	mW PER BIT (SYSTEM)	mW ACTIVE/STANDBY PER DEVICE	mW PER BIT (SYSTEM)
1K	32	450	0.45	[1]	[1]
2K	16	700	0.35	550/225	0.19
4K	8	950	0.24	700/225	0.11

NOTE: 1. Power reduction not offered.

Table XXI. Device Comparison for 1K x 32 Memory System.

DEVICE SIZE	NO. OF DEVICES	ARRAY SIZE	MEASURED ADDRESS DRIVER TIME[1]	OUTPUT OR-ING DELAY[1]	MAXIMUM DEVICE ACCESS TIME[1]	SYSTEM ACCESS TIME[1,2]
1K	32	14.06 sq in.	22 nS	0 nS	50 nS	72 nS
2K	16	6.46 sq in.	16 nS	-4 nS	70 nS	82 nS
4K	8	8.26 sq in.	12 nS	-4 nS	70 nS	78 nS

NOTES: 1. All times taken at 1.5V points.
2. This time is the sum of device maximum and measured buffer delays.

Printed Circuit Layout Considerations

PROMs and ROMs can easily be used in much the same manner as other types of TTL design elements. The usual attention should be paid to ground distribution and decoupling.

Ideally, the circuit board ground system should consist of a ground plane on one side of the board and all signal and power distribution on the other. In reality, this is very difficult to achieve because of component densities, but the concept should be carried out as far as possible. The ground distribution should be as wide as possible everywhere, even if it means large variations in the width of the conductor.

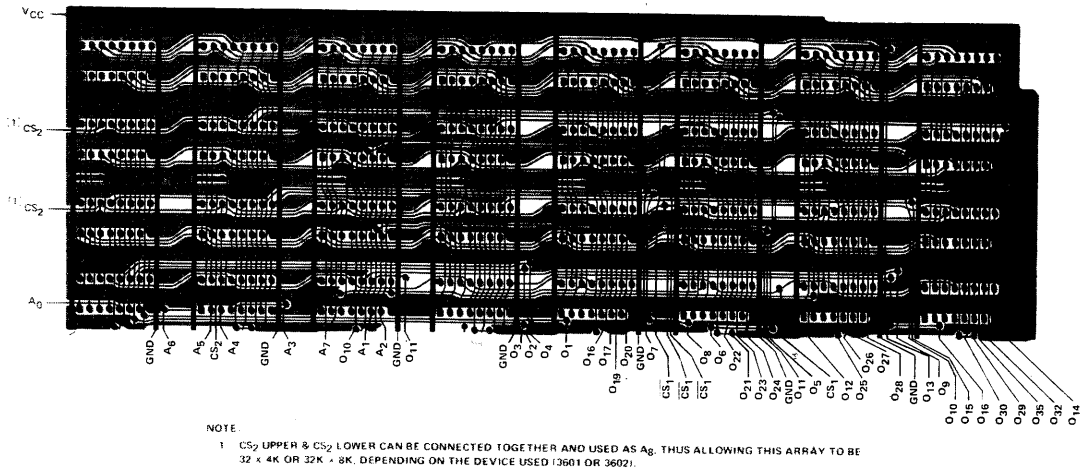
To further approach a ground plane or mesh, horizontal and vertical power and ground traces on opposite sides of the board should be tied together at each DIP site, or as often as possible. The tying of the horizontal and vertical traces is important because long "floating" distribution lines can easily act as an antenna or a noise distribution system, allowing noise to propagate and exceed device thresholds.

In addition to reducing ground noise, an effective ground grid can serve to reduce cross-talk between address and data lines.

As can be seen in Figure 41 (previous section) the high to low transition can be very rapid, and if proper attention is not paid to the ground and power distribution, the noise resulting from these transitions can couple throughout the board and into the system. The memory devices should be decoupled at approximately every other DIP site with high frequency disc ceramic capacitors. There also should be bulk decoupling at the point where the V_{CC} line enters the board, usually one or more tantalum capacitors in the 10–50 μF range.

The layouts shown in Figure 46 and 47 are a good example of proper ground distribution. Notice that the ground plane forms a complete loop around the array (board) on both sides and that the two sides are connected periodically by horizontal and vertical traces.

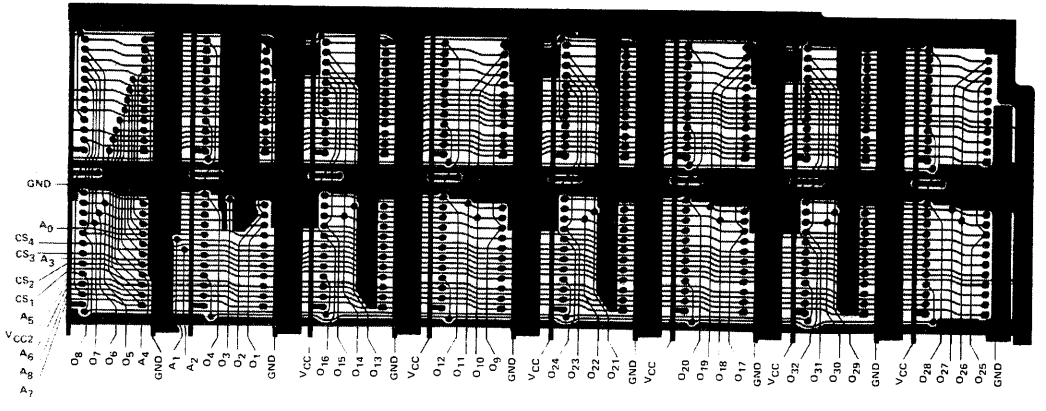
The decoupling for the 1K/2K array consists of eight 0.1 μF high frequency capacitors, or one capacitor for each four devices, distributed through the array. This decoupling is adequate, but a better arrangement would be 0.1 μF located at every other device site, similar to the scheme used on the 4K layout.



This array illustrates the layout for a 1K X 32-bit PROM memory. Power has been distributed with a grid system, and decoupling is located in the center of the array. By routing all the $\overline{CS_2}$ lines to a common point, the memory can be expanded to use 2K parts simply by supplying an additional address, A8, and connecting it to all the former $\overline{CS_2}$ inputs.

Array layout courtesy of
MICRODATA INC.,
Irvine, California

Figure 46. 1K/2K PROM Array.



This array illustrates the use of a 24-pin 4K PROM to implement a 1K X 32-bit control store memory. As with the 1K/2K array, gridded power distribution has been used, with decoupling capacitors located in the center of the array.

Array layout courtesy of
MICRODATA INC.,
Irvine, California

Figure 47. 4K PROM Array.

Uses of PROM/ROMs

CODE CONVERSION

Read only memories lend themselves readily to converting from one binary code to another (such as from binary to Gray). This conversion is particularly useful in electromechanical systems controlled by a computer.

For example, consider a computer-controlled electromechanical encoder system. The computer performs data operation in binary form and outputs the x–y coordinates in the same form. If the stepping motor has a binary data input, erratic movement of the motor will be observed as the motor moves sequentially from one set of coordinates to another, because, as many data bits change and their exact switching relationship is not fixed, the motor will receive multiple codes until the data stabilizes. Consider the case of changing from decimal 7 to decimal 8 as shown in the truth table (Figure 48a), where 4 binary bits will change state. This transition will generate several random binary codes (up to 8) until the data stabilizes causing the stepping motor to move erratically.

It would be highly desirable to have a code where sequential motor stepping could be accomplished by changing only one bit per word between adjacent steps. The Gray code is such a code. By using the Gray code for the above example in moving from decimal 7 to 8 requires the change of only one bit (0100 to 1100). The stepping motor now moves smoothly without jitter or ambiguity as one Gray code bit changes after another. (Note that since the bit positions are not numerically weighted in Gray code, it is not possible to perform conventional binary arithmetic on the word. Therefore, the computer does not operate with such a code internally).

The code conversion from binary to Gray code for communication between the computer and the system motor becomes a simple matter if a read only memory is used. To use the truth table to convert from binary to Gray code it is merely necessary to use the binary data as the address to a ROM and read the corresponding Gray code at the output of the ROM. The example presented here is a 4-bit code but can be expanded to provide the desired resolution.

The conversion from binary to Gray code is only one of many code conversions possible. PROM/ROMs can be used to encode data for secured data transmission systems. These types of codes can be as simple or as complex as desired. A terminal attached to a central computer can "talk" to the computer over a secured line if both the terminal and computer have the proper encoding/decoding PROM/ROMs. Multiple terminals, each with its separate code, can likewise be connected to the computer. Of course for multiple terminals the computer must have the proper encoding/decoding PROM/ROM circuitry.

An example of such an encoding/decoding scheme is shown in the truth table (Figure 48b). To encode for data transmission, a standard binary code is presented to the address inputs of a ROM. The output of the ROM contains the code for the particular character to be sent. At the receiving end the order is reversed with the encoded data presented to another ROM address input whose output corresponds to the original character or data sent by the terminal. Data transmission in the reverse direction is handled in an identical manner.

DECIMAL	BINARY	GRAY
0	0 0 0 0	0 0 0 0
1	0 0 0 1	0 0 0 1
2	0 0 1 0	0 0 1 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 1 1 0
5	0 1 0 1	0 1 1 1
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 0 0
8	1 0 0 0	1 1 0 0
9	1 0 0 1	1 1 0 1
10	1 0 1 0	1 1 1 1
11	1 0 1 1	1 1 1 0
12	1 1 0 0	1 0 1 0
13	1 1 0 1	1 0 1 1
14	1 1 1 0	1 0 0 1
15	1 1 1 1	1 0 0 0

(a)

TRANSMISSION SCRAMBLER	
ADDRESS	DATA
BINARY CODE	SCRAMBLER CODE
0 0 0 0	0 0 0 1
0 0 0 1	1 1 0 1
0 0 1 0	1 1 1 1
0 0 1 1	1 0 1 0
0 1 0 0	0 1 1 0
0 1 0 1	0 0 1 1
0 1 1 0	0 0 1 0
0 1 1 1	0 0 0 0
1 0 0 0	1 0 0 0
1 0 0 1	1 0 1 1
1 0 1 0	1 1 1 0
1 0 1 1	1 0 0 1
1 1 0 0	1 1 0 0
1 1 0 1	0 1 1 1
1 1 1 0	0 1 1 0
1 1 1 1	0 1 0 0

RECEIVING SCRAMBLER	
ADDRESS	DATA
SCRAMBLER CODE	BINARY CODE
0 0 0 1	0 0 0 0
1 1 0 1	0 0 0 1
1 1 1 1	0 0 1 0
1 0 1 0	0 0 1 1
0 1 1 0	0 1 0 0
0 0 1 1	0 1 0 1
0 0 1 0	0 1 1 0
0 0 0 0	0 1 1 1
1 0 0 0	1 0 0 0
1 0 1 1	1 0 0 1
1 1 1 0	1 0 1 0
1 0 0 1	1 0 1 1
1 1 0 0	1 1 0 0
0 1 1 1	1 1 0 1
0 1 1 0	1 1 1 0
0 1 0 0	1 1 1 1

(b)

Figure 48. Code Conversion Truth Tables.

COMBINATORIAL CIRCUITS

Digital circuits are often divided into two categories: combinatorial and sequential. Combinatorial circuits have no internal storage elements. As a result, the output signals are functions only of the inputs supplied at the time the output is measured (neglecting propagation delays). A ROM may be used to generate combinatorial functions when the number of input signals is not excessive. For example, a 256 word by 4 bit ROM has 8 input leads (addresses) and 4 output leads and so can be used to generate any 4 combinatorial functions of 8 variables. Additional functions may be generated by adding more ROMs – doubling the number of ROMs doubles the number of functions which can be generated.

Expanding the number of input variables is much more costly, however, Additional input variable may be decoded to operate chip selects just as additional addresses inputs are decoded in a memory array. However, each additional input variable doubles the amount of ROM required.

Various authors have expressed the option that 8 to 16 bits of ROM are equivalent to one logic gate. However, this ratio does not apply to all designs. For example, to make a quad full adder (5 outputs, 9 inputs) would require 5×2^9 or 2560 bits of ROM, but can be realized with less than 40 gates – for ratio greater than 64 bits/gate.

When using ROM to replace wired logic gates, the designer should remember that the ROM is not guaranteed to give a single output transition for a single input transition. Figure 49 illustrates the way the designer should view the ROMs behavior. In Figure 49, after a short hold time, the outputs are undefined until a period equal to the ROMs access time has elapsed. During this undefined interval, the ROM outputs may show noise or extra transitions. Not all ROMs specify a hold time. Even when a hold time is specified, it is valid only when access to a location has been made, and is measured from the first address transition.

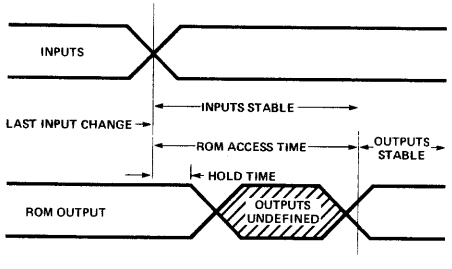


Figure 49. ROM Behavior for Combinatorial Logic.

SEQUENTIAL CIRCUITS

Sequential circuits are logic circuits with internal storage. As a result, outputs are a function of past as well as present inputs. Seqeuntial circuits are often realized by a collection of storage elements (flip-flops) together with combinatorial logic. Outputs of the sequential network are combinatorial functions of the inputs to the network and the flip-flop outputs. The inputs to the flip-flops are combinatorial functions of network inputs and flip-flop outputs.

When a sequential digital system is described in the above manner, the state of the circuit is determined by the contents of the flip-flops. Therefore, a machine with n flip-flops can have at most 2^n internal states. To describe the circuit behavior, two sets of information must be known:

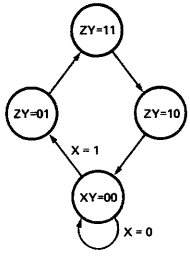
1. The outputs as function of inputs and internal states; and
2. The next states as functions of inputs and internal states.

This information may be presented via tables or graphically in the form of a state sequence diagram, such as that shown in Figure 50a. The state sequence diagram is usually drawn as a collection of circles, each labelled to correspond to one state of the machine. The circles (states) are connected by directed lines (arrows) indicating which state transitions may take place. Each such transition line is labelled with the values of the input variables for which the transition takes place, unless the input variables have no effect. In that case, the state transition always takes place and the arrow is unlabelled.

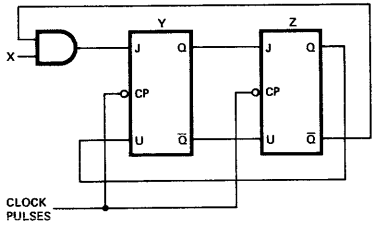
Some digital circuits are clocked, i.e., state transitions take place only upon occurrence of a clock pulse. If for some input conditions no state transition takes place at a clock time, it is indicated on the diagram as an arrow which leaves and re-enters the same circle. This arrow is labelled, like any other, with the corresponding input conditions. Clocked sequential circuits are readily designed using clocked flip-flops of the JK or D variety such as those shown in Figures 50b and 50c.

State Assignment

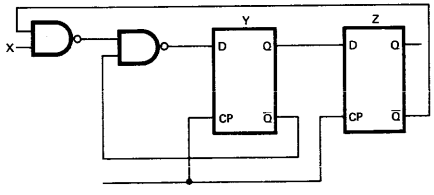
The state-sequence diagram describes the digital circuit behavior independent of the assignment of states to the circles of the diagram. Each circle in the diagram must be assigned a unique set of values for the state variables. Each state variable can take on the value of 1 or 0, so that n state variables can provide values for up to 2^n circles in the diagram. However, the way the values are assigned to the circles can make a significant difference in the ease of realization when JK or D flip-flops are used. At present, no known technique, other than repeated trails, exists for determining the minimum cost state assignment. The designer's insight and experience contribute significantly to the design efficiency. However, when ROMs are used, state assignments are less critical than for realization with wired logic gates.



a. State Diagram



b. Corresponding Sequential Circuit – JK Realization



c. Corresponding Sequential Circuit – D Realization

Figure 50. Sequential Circuit State Diagram Realizations.

Asynchronous Input to Clocked System

When a clocked system has asynchronous input variables, i.e., variables which can change at other than clock times, proper behavior may depend upon the state assignment used. For example, if the values of a given asynchronous input variable can affect the values of two state variables in a given state transition, differential delays in the logic may allow 4 rather than 2 possible state changes to take place: neither, either, or both of the variables may change. To avoid this situation, state assignments should be such that only one state variable is a function of each asynchronous input variable or the asynchronous input variable should be made synchronous by clocking it into a flip-flop. Of course, the latter procedure increases the response time of the system to the input signal.

These considerations also apply to the asynchronous flip-flop forcing inputs. In general, these inputs can force the network into one or more of a subset of the states where it will remain until the forcing input is removed. If the network clocked transitions attempt to change more than one forced state variable, asynchronous removal of the forcing signal may result in any of several state transitions: any or all of the variables attempting to change may do so, depending upon differential delays in flip-flop responses, clock distribution, and distribution of the forcing signal.

Realizations with D Flip-Flops

Having assigned state variable values for each state, realization with D flip-flops is very straightforward.* First, a truth table or set of Karanaugh maps is prepared. The source variables include all state variables and all input variables. The functions to be generated involve all state variables (next state value) and all output functions. Those functions representing the next state values are used as the data inputs to the corresponding D flip-flops.

Figure 51 shows a symbolic diagram of such a network. The "clocked register" is an array of n D-type flip-flops.

A read only memory array with p address inputs and q outputs (2^p x q bits) can generate a total of q output functions of p inputs. Thus for Figure 51, if n state variables are required, p-n input variables may be used and q-n output signals may be generated.

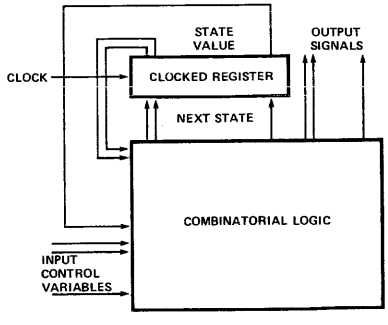


Figure 51. Realization of Digital Machine.

*For sequential networks wired with logic gates, JK flip-flops may reduce the gate count as in Figure 50b and 50c. However, ROM realizations are more economical when D flip-flops are used, because fewer functions need be generated.

Because a ROMs internal realization is quite different than that of a conventional combinatorial logic network, different considerations apply to ROM designs than for conventional designs. For example:

1. State variable assignment has little or no effect on circuit complexity when ROM realization is used. Therefore, the designer may use state variables to form output functions directly with greater ease than for conventional designs. If, however, additional logic circuits are added to reduce total ROM requirements or allow asynchronous input variables (see next paragraph), some of this design freedom may be removed.
2. All outputs of a ROM must be considered functions of all inputs. Therefore, asynchronous inputs to the ROM should not be permitted to change within an access time prior to clocking the output register, or the contents of the output register may be completely unpredictable. Additional latches or separate logic between the ROM output and D flip-flop inputs should be used so that the conditions described above (under Asynchronous Inputs to Clocked Systems) can be met. Additional ROM outputs may be used to enable or disable this logic.

Methods of Reducing ROM Size

If the number of input or output variables is large, a straightforward realization with ROM may not be practical. However, it may be possible in certain areas to reduce the amount of ROMs by adding a small amount of additional logic. Several methods for reducing the size of a ROM needed to perform a given function are described below. The use of these techniques when appropriate may permit a ROM approach to be used in a situation where it would normally be impractical to do so. Most of these techniques are illustrated in Figure 52.

Multiplexing Input Variable

Instead of using all input control variables at all times, many digital machines have only a few states where the next state decision is affected by the input variables. Therefore, a multiplexer may be used to select the input variables which are active for each given state of the machine. The effective number of input control variables at the ROM may be reduced to a number equivalent to the largest number active at any one time.

The control signals for the multiplexer may be generated by logic circuits which decode the state information or by extra output variables from the ROM. In general, these extra ROM output variables are far less expensive than the extra ROM inputs that would otherwise be necessary.

Bypassing the ROM for Input Control Variables

If the state assignments are made so that the next state is a simple function of the input variables, a small amount of logic may be placed between the ROM output and the clocked register. Some of the input control variables are then brought into the system via this logic rather than through the ROM. As in the case with input multiplexing, additional output signals may be used to enable this logic.

One simple form of this method uses a multiplexer between the ROM output and the clocked register. Certain of the

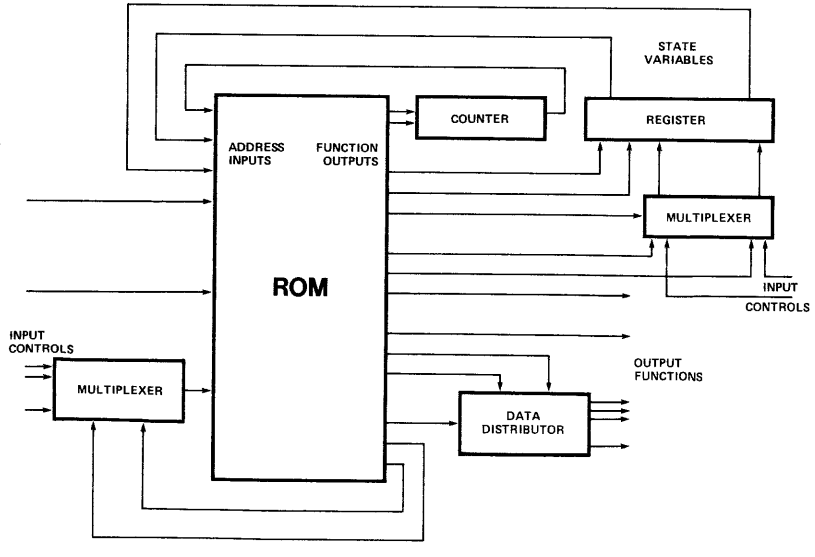


Figure 52. ROM Realization of Sequential Machine.

state variables take on the values of the input variables whenever the multiplexer is set to accept these inputs. This method places restrictions on state assignment.

A similar technique is usually necessary for use with input control variables which are asynchronous.

Output Function Distribution

When a large number of control functions must be generated, but only one or two are active at one time, data distributors may be used to generate a large number of control functions from a few ROM outputs. As an example of the type of coding which might be used, 8 non-simultaneous control functions might be generated using one data bit and 3 selection bits. The Intel® 3205 decoder may also find use in ROM output expansion. Eight selection signals can be generated from three ROM function outputs.

External State Generators/Partitioning/Factoring

When a large number of states of a state diagram fall in an easy to generate sequence, the number of state variables generated by the ROM may in some cases be reduced by generating the additional states with external circuits such as counters or shift registers. Functions of these separately realized state variables may be used as equivalent state variable inputs to the ROM.

As an example of this technique, consider a binary counter connected to a ROM such that the ROM can generate a preset or count enable variable and accept a carry output as equivalent to a state input variable. The ROM may be programmed so that for some states of the conventional state variables, the counter counts from its preset values until it overflows with the ROM staying the same state throughout the counting sequence. In this example, one input (equivalent state) variable replaces all of the state variables in the counter.

The example above is a special case of a more general technique which may be called partitioning. Instead of using an external counter with the ROM system, another ROM/register sequential machine might have been connected. The net result is a ROM/register realization of a sequential digital machine in which not all state variables are used as inputs to all of the ROM. In effect, the machine is partitioned into a number of smaller, but interactive, machines.

To partition a circuit, the state variables must be isolated into two or more groups. A new state diagram can be generated for each group. In these partitioned state diagrams, the state variables for one state diagram are treated as if they were input control variables in the other. In general, for partitioning to be effective, the state variables must be such that they can be divided into relatively independent groups.

These examples are but a few of those available to the designer wishing to take advantage of ROM. As the design complexity progresses, the structure approaches the complexity of a microprogrammed processor – one application where ROM is extensively applied.

ROM, even in complicated networks like that of Figure 52 or a microprogrammed processor, offers much easier modification of machine structure than wired logic. With the availability of programmable ROMs, ROM approaches to sequential circuit design merit serious consideration.

Even when a prototype system has been developed using the 3601 or 1702A, once ROM patterns have been fixed, the prototypes can be easily converted to use the 3301A or 1302 for production for these mask programmed devices are pin and signal compatible with their field programmable counterparts.

WAVEFORM GENERATOR

To show one simple application of ROM, consider the signal generator shown in Figure 53. An 8-bit counter driven by an oscillator drives a 2048-bit ROM (256 words of 8 bits). The ROM outputs are converted to an analog voltage by a digital to analog converter (DAC). By properly coding the ROM, a wide variety of waveforms may be generated.

For the system shown in Figure 53, each step of the 8-bit counter represents $\frac{360}{256}$ degrees of phase angle. The value at each address in ROM is the digital number representing the signal output for that phase angle. Multiple ROM/DAC combinations might be used to generate several simultaneous waveforms, or multiple phases of a signal, for example. The output of the DACs will change in small discrete steps, each less than 1% of full scale. Where this might be a problem, filtering might be used. However, undesired harmonic content of the signal will be limited to the upper harmonics.

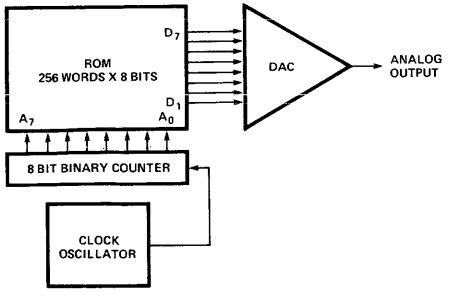
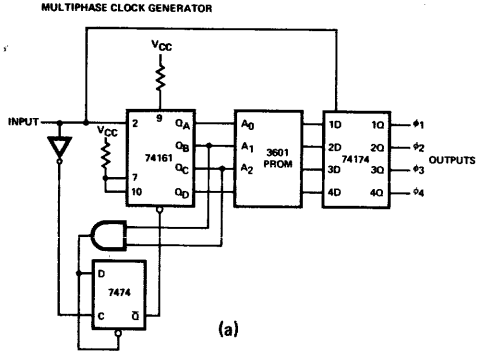


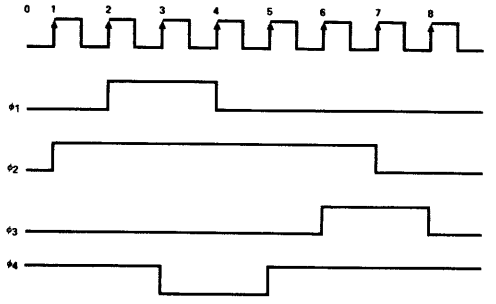
Figure 53. Digitally Controlled Waveform Generator.

CLOCK GENERATION

ROMs can be used to generate clock phases for use in multi-clock systems (such as driving a 16K CCD, Intel's 2416). An example of the generation of a general clock generator is shown in (a). The desired timing is shown in (b).

Basic operation is as follows: A clock input is applied to the input of a 74161 TTL counter as shown in (a). The counter sequentially counts six cycles of the input as shown in (b). The counter output is presented to the PROM as an address. The output of the PROM as a function of the address is shown in truth table (c). The outputs of the PROM are latched in the 74174 by the input clock. This prevents unwanted transients from occurring on the four-phase clock lines.





ADDRESS	O_1	O_2	O_3	O_4
0	0	0	0	1
1	0	1	0	1
2	1	1	0	1
3	1	1	0	0
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	0	1	0

(c)

Figure 54. Clock Generation.

MICROPROCESSOR SYSTEM

Illustrated here is a typical microprocessor system, based on the Intel® 8080. The 2708 provides 8K (1024 X 8) of PROM storage, while the combination of two 8101/5101's provides 2K (256 X 4) of RAM storage. A_{10} is used to select the desired type of storage access; A_{10} high selects RAM and A_{10} low selects the PROM storage. The other address bits, A_{11}–A_{16}, are generated by the 8080 and can be used for system expansion. The ROM storage can be modified to use a 1702A for 2K (256 X 8) of EPROM storage, or a 2316 for 16K (2K X 8) of ROM storage. In the case of the 2316, 11 of the 8080 address lines would be used.

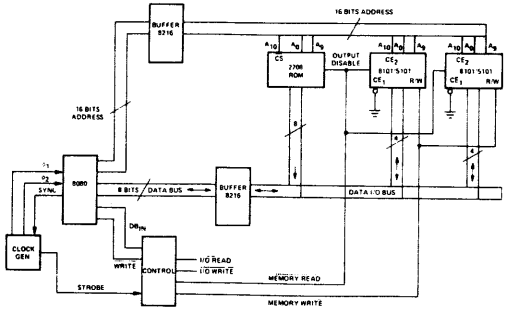


Figure 55. Microprocessor System.

4K BYTE SYSTEM

A 32 kilo-bit PROM memory organized as 4K X 8 utilizing the 1702A is shown in Figures 55 and 56. Each of the 1702A's is accessed individually by means of a 3-to-8 encoder (Intel® 3205) with decoder enables connected as shown. The three low-order addresses (A_0–A_2) are decoded simultaneously by two 3205's and the proper 1702A selected by address A_{11} activating either the right or left 3205. Since all unselected 1702A's have high impedance outputs, the selected module controls the internal data bus with its output gated through the three-state output buffers shown in the schematic.

The 4K X 8 board shown is expandable with a given PROM board identified by the PROM Board Resident Select Switches.

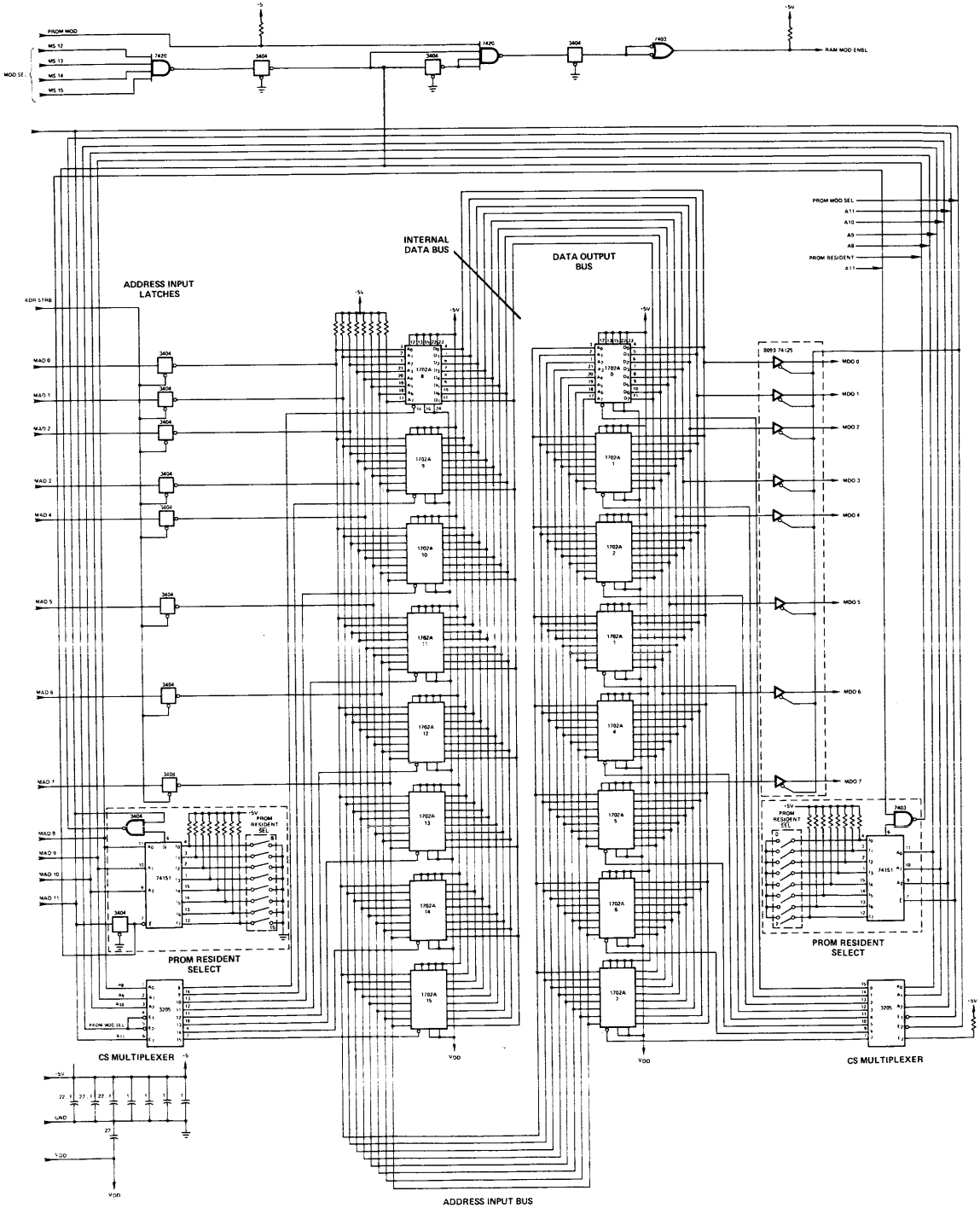


Figure 56. 4K Byte PROM System.

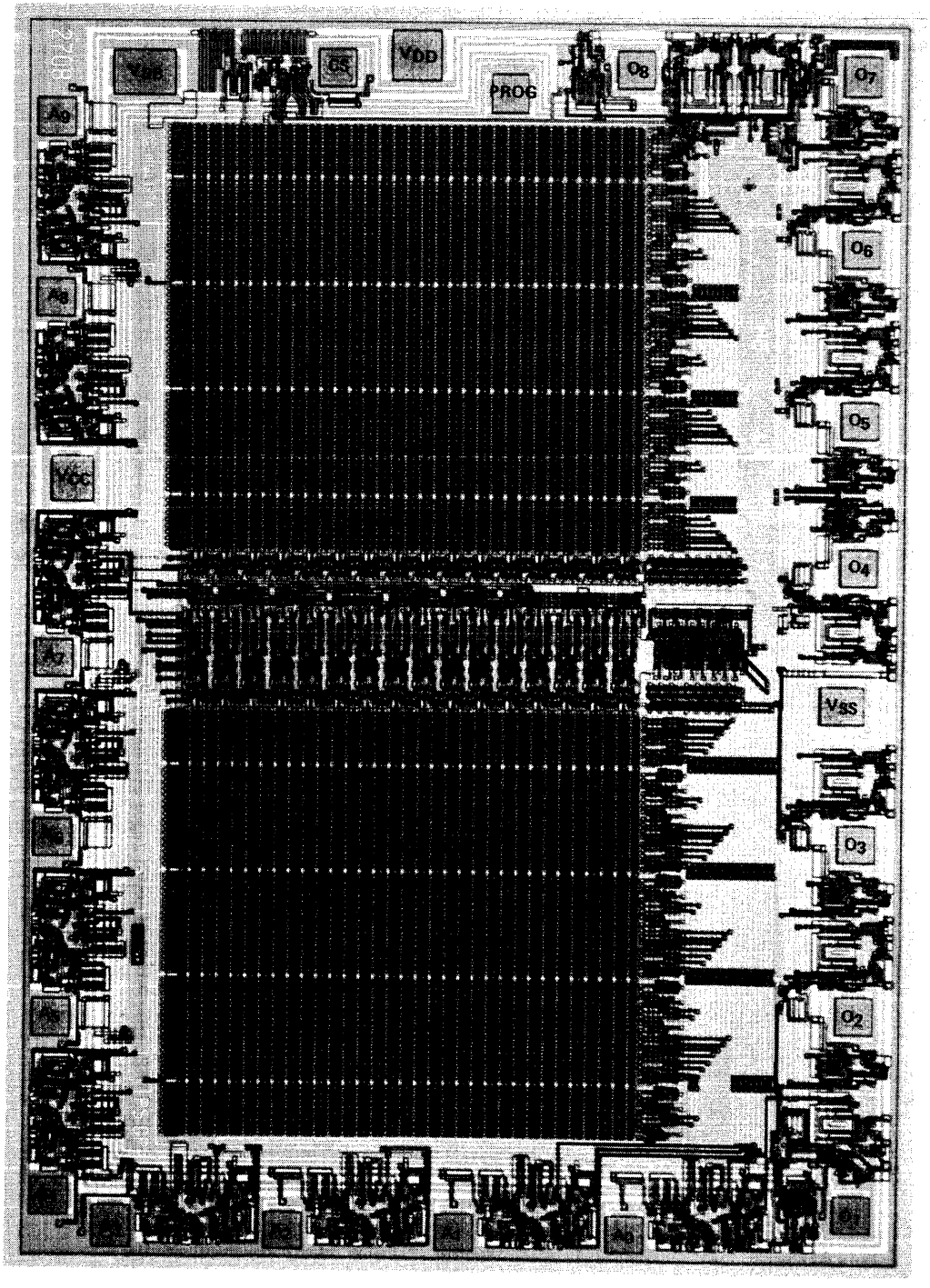
Application of the Intel® 2708 8K Erasable PROM

Bob Greene

Application Engineering

Contents

2708 8K UV EPROM



INTRODUCTION

The Intel® 2708 is a static 8192-bit (1024 X 8) Erasable Programmable Read Only Memory, or EPROM. The device is packaged in a standard 24-pin package, which has a transparent lid to allow erasure in a manner similar to the Intel® 1702A. Maximum access time is 450 ns. The device requires three power supplies, ±5V and +12V, for normal read cycles; while for programming a 26V pulse is required on the Program pin.

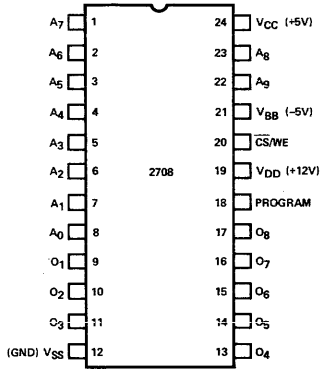
The address inputs and data I/Os are TTL compatible during read and programming. The data outputs are three state to facilitate memory expansion by OR-tying. Initially, and after each erasure, the device contains all "1's". Programming, or introducing "0's", is accomplished by: applying TTL level addresses and TTL level data; a +12V Write Enable signal; then sequencing through all addresses consecutively a minimum of 100 times, applying a 26V program pulse at each address. ALL ADDRESSES MUST BE PROGRAMMED DURING EACH PROGRAMMING SESSION; PROGRAMMING OF SINGLE WORDS OR SMALL BLOCKS OF WORDS IS NOT ALLOWED. As discussed in detail in the PROGRAMMING section, approximately 100 seconds are required to program the entire device.

DEVICE DESCRIPTION

The device is packaged in an industry standard 24-pin package as shown in Figure 1. The Program pin (18) receives 26V pulses during programming; during read operations it must be connected to V_{SS} (GND) or held at V_{IL}.

Pin 20, the $\overline{CS}$/WE connection, serves three functions. When at V_{IL} (0V) the device is selected for normal read operation; when at V_{IH} (3.0V min) the device is deselected and the outputs are placed in the high impedance state; and when at V_{IHW} (11.4V min) the device is Write Enabled and ready to receive program pulses.

A block diagram of the 2708 is shown in Figure 2. The low order address bits (A_0–A_3) perform column (or Y) selection, while the high order address



PIN NAMES

A_1-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

Figure 1. 2708 Pin Configuration

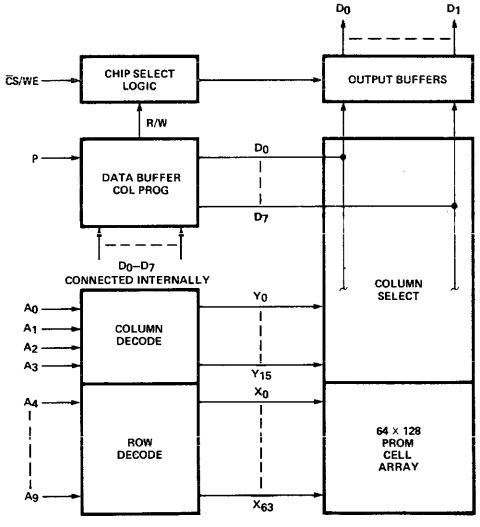


Figure 2. Detailed Block Diagram

Table I. 2708 Pin Connections and Functions

Function / Pin Number / Mode	Data I/O 9–11, 13–17	Address Inputs 1–7, 23, 22	V_{SS} (GND) 12	Program 18	V_{DD} Supply 19	$\overline{CS}$/WE 20	V_{BB} Supply 21	V_{CC} Supply 24
Read	D_{OUT}	A_{IN}	GND	GND	+12V	V_{IL}	-5V	+5V
Deselect	High Impedance	Don't Care	GND	GND	+12V	V_{IH}	-5V	+5V
Program	D_{IN}	A_{IN}	GND	Pulsed +26V	+12V	V_{IHW}	-5V	+5V

bits (A_4–A_9) perform the row (or X) selection. Table I assists in determining the proper voltage connections for the three modes of operation; Read, Deselect and Program.

Cell Description

The heart of the 2708 is the single transistor stacked gate cell, implemented with two layer polysilicon. The cell consists of a bottom floating gate and a top select gate, as shown in Figure 3. The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by injection of high energy electrons through the oxide and onto the floating gate. Once there the charge is trapped, as there are no electrical connections to this floating gate. The presence of charge on the floating gate causes a shift to the cell threshold, as shown in Figure 4. In the initial state the cell has a very low threshold and selection of the cell, by way of the top select gate, will cause the transistor to turn on. Programming shifts the threshold to a higher level and selection of the cell will not allow it to turn on. The status of the cell is determined by examining its state at the sense threshold, also indicated in Figure 4. If a "1" is programmed into the cell, selection will allow a higher current to flow between the source and drain than if a "0" is programmed into the cell.

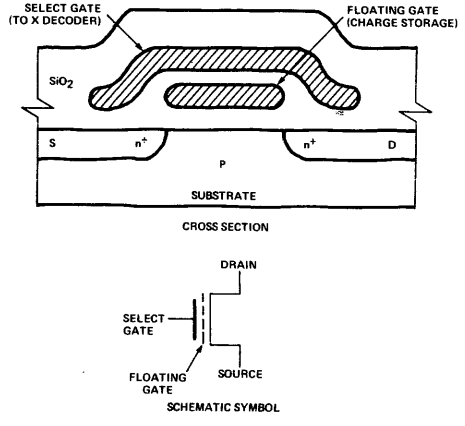


Figure 3. 2708 Storage Cell

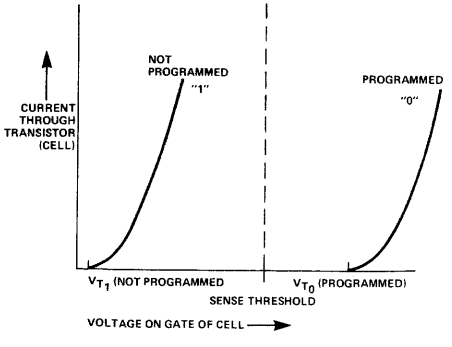


Figure 4. Storage Cell Threshold Shift

As there are no electrical connections to the floating gate, erasure must be accomplished by non-electrical means. Illumination of the cell with ultraviolet light of the correct frequency (2537Å) and duration will impart sufficient photon energy to the trapped electrons to allow them to overcome the inherent energy barrier and be transported through the oxide to the substrate.

Memory Array Operation

The cells described in the previous paragraph are interconnected to form a 64 X 128 matrix, or array, as shown in Figure 5. Access to a particular cell is described as follows: When the Row Address is stable, one row is selected, turning on the row line to all 128 cells in the row. The Column Address connects 8 of the 128 column lines to their respective sense amplifiers. The row line provides bias to all the top gates in a particular selected row, and, depending on the state of the cells, the column lines will be left at the precharged level (for a programmed "0") or will be discharged, pulling the column lines down to a low level (for a programmed "1"). To provide the very fast Chip Select to Output Delay time (t_{CO}) of 120 ns, all of the sense amplifiers are turned on when the device is deselected, and, when $\overline{CS}/WE$ reaches V_{IL}, those which are not selected are turned off, and the remaining eight amplifiers convert the charge on the column lines to TTL output levels by way of the output buffers.

During programming the selected row and column lines are pulsed to approximately 26 volts and the floating gate is charged as was described in the previous section. It is the presence of these 26V pulses on the interconnected top gates that lead to the requirement that ALL ADDRESSES MUST BE PROGRAMMED SEQUENTIALLY; PROGRAMMING OF SINGLE WORDS OR SMALL BLOCKS OF WORDS IS NOT ALLOWED, as transients may be generated that could partially alter the charge state of the cell.

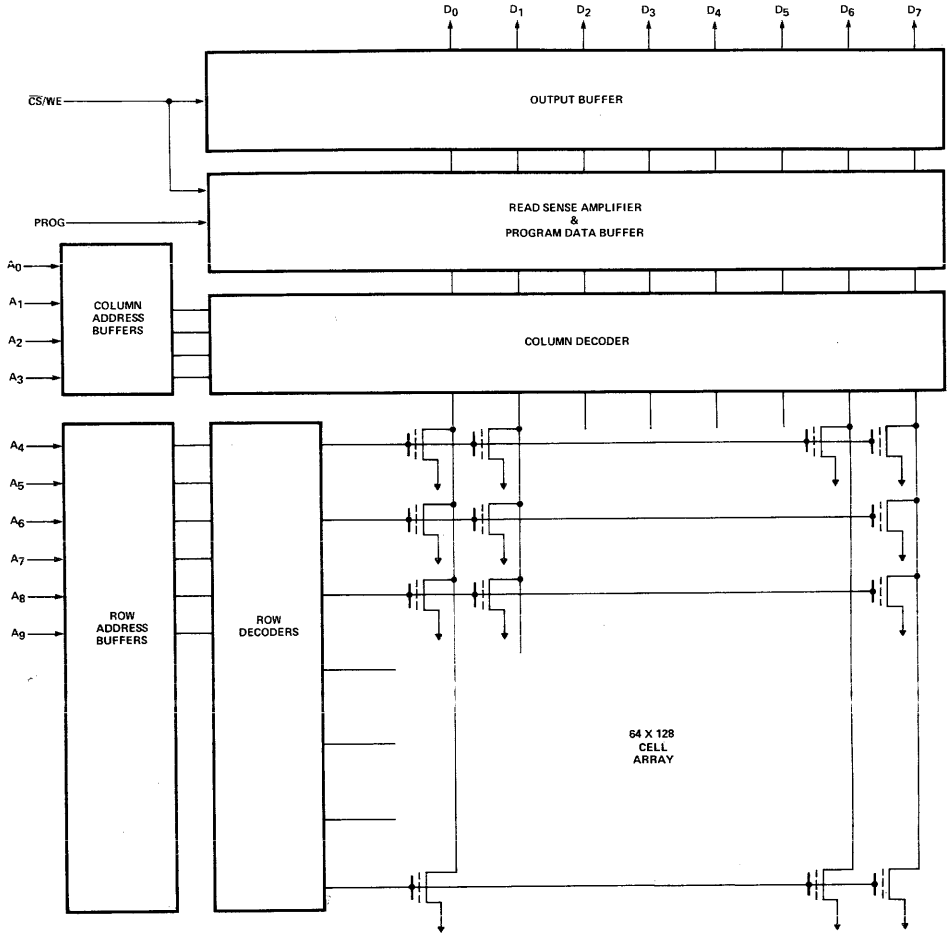


Figure 5. Expanded Block Diagram

Output Buffer

The equivalent schematic of the Output Buffer is shown in Figure 6. As is shown, the output buffer consists of a pair of MOS transistors, connected in a push-pull configuration. $\overline{CS}$ enables both transistors when true, while when $\overline{CS}$ is false both output devices are turned off, providing three state output operation. The output buffer will provide a V_{OL} of 0.45V at an I_{OL} of 1.6 mA, and a V_{OH} of 2.4V at −1.0 mA.

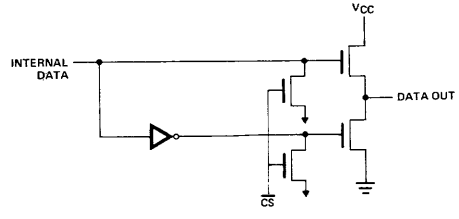


Figure 6. 2708 Output Buffer

Table II. D.C. Read Mode Characteristics

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Sink Current		1	10	μA	V_{IN} = 5.25 V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10	μA	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V
I_{DD}[2]	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}[2]	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}[2]	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = -1mA
P_D	Power Dissipation			800	mW	T_A = 70°C

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. The total power dissipation of the 2708 is specified at 800 mW. It is not calculable by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

D.C. DEVICE CHARACTERISTICS

Only those D.C. Characteristics that require special attention by the user are presented in this section. The reader is referred to the 2708 device data sheet for further details. The pertinent D.C. device specifications are tabulated in Table II.

The 2708 requires three power supplies, +12V and ±5V. The device is rated to meet all applicable specifications with these supplies held within ±5% of their normal value. The Absolute Maximum Ratings in the data sheet are the maximum that the various device parameters can withstand and should not be exceeded during any phase of device operation, including programming.

Read Mode

The range of values of currents from the three power supplies, V_{DD} (+12V), V_{CC} (+5V) and V_{BB} (−5V) are shown in Table II, presented for the worst case conditions; i.e., $\overline{CS}$/WE = 5V and T_A = 0°C. The I_{DD}, I_{CC} and I_{BB} data presented indicates the maximum current drawn by the respective power input. These inputs cannot simultaneously draw maximum current. Refer to the APPLICATIONS SECTION for measured laboratory data of the interactive effects of switching the various supplies off to conserve power.

The addresses are TTL compatible, requiring V_{IL} between V_{SS} and 0.65V and V_{IH} between 3V and V_{CC} + 1. Care should be exercised in selecting address buffers to insure the minimum V_{IH} level is met by use of appropriate TTL circuit elements or pull-up resistors to V_{CC}.

During the Read mode, the $\overline{CS}$/WE input (pin 20) is also TTL compatible; however, the V_{IL} and V_{IH} requirements for the address inputs are still applicable.

The outputs are also TTL compatible, producing a V_{OL} of 0.45V maximum @ 1.6 mA and a V_{OH} of 3.7V with −100 μA capability, or 2.4V with −1 mA capability. Typical output sink current is plotted in Figure 7 as a function of the output voltage and temperature for applications requiring higher than normal I_{OL} currents.

Figure 8 illustrates several points regarding the 2708 power supply currents. First of all, as with all MOS devices, the power supply currents will decrease as a function of increasing temperature. The second point is that the current requirements of the device increase when it is deselected, i.e., when $\overline{CS}$/WE is at V_{IH}. The reason for this is that in order to meet the very fast t_{CO} time of 120 ns, all of the decoders and output stages are turned on when $\overline{CS}$/WE is at V_{IH}, and the decoders deselect those that are not required for the given data cycle. The graph also illustrates that the V_{DD} power supply is the most logical supply to be selected for switching to reduce power. Of course, if the system configuration permits, $\overline{CS}$/WE can be tied to V_{SS} to reduce power.

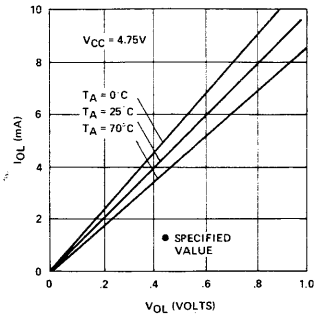


Figure 7. 2708 Typical Output Sink Current vs. Output Voltage

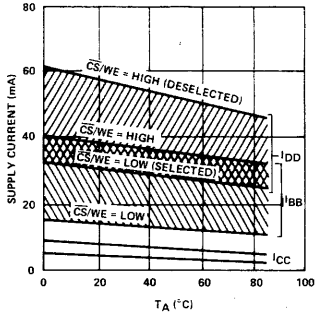


Figure 8. 2708 Power Supply Currents

Table III. D.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Address and $\overline{CS}$/WE Input Sink Current			10	μA	V_{IN} = 5.25V
I_{IPL}	Program Pulse Source Current			3	mA	
I_{IPH}	Program Pulse Sink Current			20	mA	
I_{DD}	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Level (except Program)	V_{SS}		0.65	V	
V_{IH}	Input High Level for all Addresses and Data	3.0		V_{CC}+1	V	
V_{IHW}	$\overline{CS}$/WE Input High Level	11.4		12.6	V	Referenced to V_{SS}
V_{IHP}	Program Pulse High Level	25		27	V	Referenced to V_{SS}
V_{ILP}	Program Pulse Low Level	V_{SS}		1	V	V_{IHP} - V_{ILP} = 25V min.

Program Mode

The address and data inputs are low level compatible during programming, with the same requirements of V_{IL} and V_{IH} as for the Read mode. The D.C. characteristics for programming are shown in Table III. To enable the device for programming, the $\overline{CS}$/WE pin is raised to V_{IHW}, (11.4V). If the system requirements dictate that the device stay in the same socket or location for both reading and programming, it should be recalled that this pin will require three input levels: V_{IL} of V_{SS} to 0.65V to select the device for a read operation, a V_{IH} of 3V to V_{CC} +1 to deselct the device and place the output in the high impedance state, and a V_{IHW} of 11.4 to 12.6V to Write Enable, or allow programming of the device. Several circuits for generating these three active levels (V_{IL}, V_{IH} and V_{IHW})are shown in the PROGRAMMING section (page 7).

During program operation, the outputs become the data inputs and should be treated as a three state bus. The same V_{IL} and V_{IH} levels apply to the data I/O pins as apply to the address pins.

The program pulse, which is applied to pin 18 during programming, must meet a V_{ILP} requirement (V_{SS} to 1V) and a V_{IHP} requirement (26V ± 1V).

The program pulse source must be capable of supplying a maximum of 20 mA per device when high (V_{IHP}), and be able to withstand the Program Pulse Sink current of 3 mA (I_{IPL}). This sink current should be considered when designing the program pulse driver, as, if a resistive pull-down is used, the voltage drop across the resistor can violate the V_{ILP} max requirement of 1V. It also should be noted that the program pulse will not meet specification if V_{IHP} is taken at its minimum value (25V) and V_{ILP} is taken at its maximum value (1V), as V_{IHP}–V_{ILP} must equal 25 volts minimum. Several circuits are presented in the PROGRAMMING section to provide program pulses which easily meet the 25V minimum requirement for V_{IHP}–V_{ILP}.

A.C. DEVICE CHARACTERISTICS

Read Mode

Figure 9, the Read mode timing, indicates the maximum or minimum timing for the various timing parameters. Particular attention should be paid to t_{DF}, chip deselect to output float time. This indicates that the output buffers of the 2708 are not guaranteed to reach the high impedance state until 120 ns after $\overline{CS}$/WE reaches the 2.8V point. If another device attempts to take control of the output node during this time, very high I_{CC} current will be drawn, generating noise on the supply lines and possibly reducing the V_{CC} level such that other devices may become inoperative. t_{DF} is also a factor to consider when switched V_{DD} is used. See the APPLICATIONS section for further discussion.

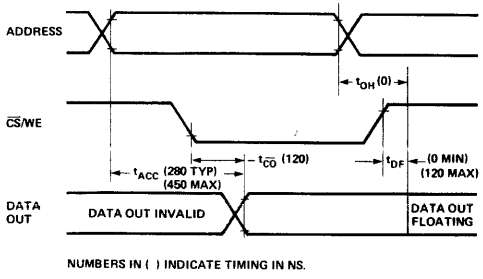


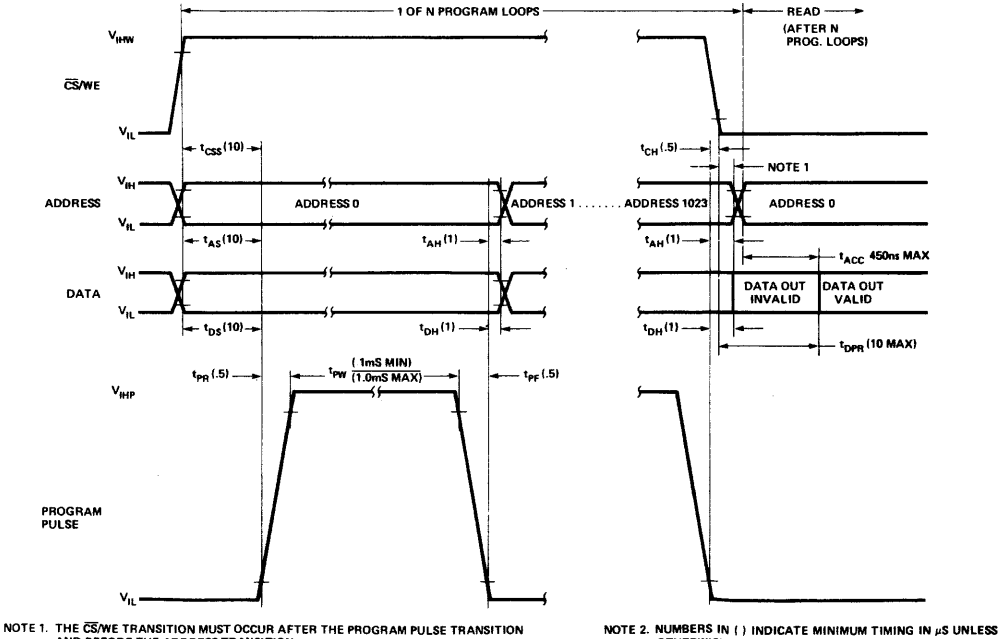
Figure 9. 2708 Read Cycle Waveforms

Program Mode

Figure 10 indicates the Program mode timing, while Table IV tabulates the various programming A.C. parameters.

Several options are available to the user when programming the 2708, as shown in the data sheet. The waveforms shown in Figure 10 represent the most efficient method. The various parameters are self-explanatory; two will be discussed here. The program pulse rise and fall times, t_{PR} and t_{PF}, must be held within the range of 0.5 and 2 μs to minimize the transient coupling effects discussed in the memory array section. This usually requires a series RC network on the output of the program pulse driver to slow down the rise time. Exotic waveform generators are not required. Refer to the PROGRAMMING section for circuit recommendations.

The other parameter of concern to the user is the transition from Program mode to Read mode. If the $\overline{CS}$/WE transition does not occur after the final program pulse transition and before the address transition, as shown in Figure 10, nodes internal to the device will not discharge, causing the output buffers to indicate false data for several milliseconds.



NOTE 1. THE $\overline{CS}$/WE TRANSITION MUST OCCUR AFTER THE PROGRAM PULSE TRANSITION AND BEFORE THE ADDRESS TRANSITION.

NOTE 2. NUMBERS IN ( ) INDICATE MINIMUM TIMING IN μS UNLESS OTHERWISE SPECIFIED.

Figure 10. 2708 Programming Waveforms

Table IV. A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	10			μs
t_{CSS}	$\overline{CS}$/WE Setup Time	10			μs
t_{DS}	Data Setup Time	10			μs
t_{AH}	Address Hold Time	1			μs
t_{CH}	$\overline{CS}$/WE Hold Time	.5			μs
t_{DH}	Data Hold Time	1			μs
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns
t_{DPR}	Program To Read Delay			10	μs
t_{PW}	Program Pulse Width	.1		1.0	ms
t_{PR}	Program Pulse Rise Time	.5		2.0	μs
t_{PF}	Program Pulse Fall Time	.5		2.0	μs

NOTE: Intel's standard product warranty applies only to devices programmed to specifications described herein.

This will appear as an excessively long t_{DPR}, Program to Read Delay. If the $\overline{CS}$/WE timing is difficult to adjust, providing the binary complement of the first address to be verified before actually verifying will also discharge the internal nodes.

PROGRAMMING

A number of programmers are commercially available that will properly program the 2708. Intel maintains a service whereby commercial programmer manufacturers obtain design approval prior to marketing their device, in order to assure compatibility with Intel specifications. This approval should be verified with the particular programmer manufacturer prior to purchase.

It is also possible to build a programmer as part of the user's system, by adhering to the following description: The device is set up for programming operation by raising the $\overline{CS}$/WE input (pin 20) to V_{IHW} (+12V). The word address is then selected in the same manner as in the Read mode. Data to be programmed are presented, 8 bits in parallel, to the data output pins (O_1–O_8). Logic levels for address and data lines and the supply voltages are the same as for the Read mode. After address and data set up times (t_{AS} and t_{DS}, Fig. 10), one program pulse of width t_{PW} is applied to the program pin (pin 18). This sequence is then repeated for the next address. One pass through all 1024 addresses is defined as a program loop. The number of program loops (N) required is a function of the program pulse width (t_{PW}) according to the formula:

$$N \times t_{PW} \geqslant 100 \text{ ms}$$

where

N is the number of program loops

t_{PW} is the program pulse width.

The width of the program pulse can vary from 0.1 to 1.0 ms. The number of loops (N) can vary from a minimum of 100 (t_{PW} = 1.0 ms) to greater than 1000 (t_{PW} = 0.1 ms), depending on the value chosen for t_{PW}. IT IS NOT PERMITTED TO APPLY N PROGRAM PULSES TO AN ADDRESS AND THEN CHANGE TO THE NEXT ADDRESS AND APPLY N PROGRAM PULSES. THERE MUST BE N SUCCESSIVE LOOPS THROUGH ALL 1024 ADDRESSES.

Referring to the timing diagram, Figure 10, optimum or most efficient programming is achieved when:

$$t_{CSS} = t_{AS} = t_{DS} = 10\ \mu s$$
$$t_{PW} = 1.0 \text{ ms}$$
$$t_{AH} = t_{DH} = 1.0\ \mu s$$
$$t_{PR} = t_{PF} = 0.5\ \mu s$$

and the time for 1 address becomes:

$$t_{AS} + t_{PR} + t_{PW} + t_{PF} + t_{AH} = 1.012 \text{ ms}$$

or, for 100 loops and 1024 addresses, the total time to program an entire device will be 1.012 ms/address × 100 loops × 1024 addresses, or 103.6 sec. Note that the program pulse duty cycle is approximately 99%. Whatever the length of the program pulse, the requirement for making successive passes through all addresses cannot be eliminated.

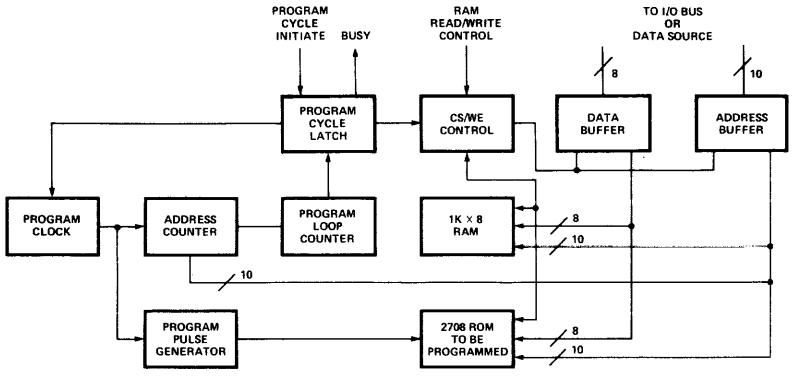


Figure 11. Typical Programming Block Diagram

Typical Programmer

Figure 11 illustrates a block diagram of a typical programmer that meets all the requirements for programming the 2708, as well as facilitating interface to a microcomputer I/O bus if it is desired to use the microprocessor system as a data source. Keyboard entry is also possible, although it does become tedious to manually enter data for 1024 PROM locations.

Operation of the programmer is as follows: While the data is being generated, the RAM Read/Write Control line allows information to pass through the Data Buffer and Address Buffer as in normal microcomputer memory operation. When the data is finalized in the 1K by 8 RAM, a Program Cycle Initiate command is generated, which responds, via the Program Cycle Latch, by generating a Busy signal back to the processor, and disenables the Data and Address Buffers, inhibiting further communication with the I/O bus until the program cycle is complete. The Program Cycle Latch also starts the Program Clock, enables the RAM, and Write Enables the PROM. It also initializes the Address and Program Loop Counters. The Program Clock activates the Program Pulse Generator, causing the information from RAM address A_0 to be programmed into the PROM. The next clock pulse increments the address counter and when the RAM data corresponding to that address is presented to the PROM inputs (outputs during read), it again increments the address counter and continues until the Address Counter overflows on the 1024th pulse, at which time the Program Loop Counter is incremented. The entire process is then repeated until the required number of program pulses has been received by each PROM location, and the Program Loop Counter overflows, resetting the Program Cycle Latch. The PROM can now be read or verified by way of the PROM cycle request.

To modify data in a partially programmed PROM it is only necessary to read the PROM into the RAM, enter the new data pattern, and check to be sure that no bits will be attempting to program 0's to 1's, and reprogram the PROM as described above. The only method of programming a "1" where there is a "0" is to erase the entire device and reprogram. This process is illustrated graphically in Figure 12.

STATUS	PROM OUTPUTS							
	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8
INITIAL STATE	1	1	1	1	1	1	1	1
FIRST PROGRAMMING	1	1	0	0	1	0	1	0
FIRST REPROGRAMMING	0	1	0	0	0	0	1	0
SECOND REPROGRAMMING	0	0	0	0	0	0	1	0
FINAL REPROGRAMMING	0	0	0	0	0	0	0	0
ERASURE	1	1	1	1	1	1	1	1

Figure 12. Reprogramming 2708 Outputs

Program Pulse Driver Circuits

Figure 13 presents several circuits which have been successfully used to generate the required 26V pulse for programming, and one circuit which should not be used.

The circuit shown in Figure 13a should not be used, as the resistive pull-down will not meet the V_{ILP} requirement of 1V max, thus not allowing $V_{IHP}-V_{ILP}$ to be equal to or greater than 25V. As was mentioned earlier, the reason for this is that the Program pin, Pin 18, sources I_{ILP} of about 2 mA when the program pulse is low and $\overline{CS}$/WE is at +12V. The other circuits, b and c, do meet all the A.C. and D.C. specifications associated with the program pulse.

$\overline{CS}$/WE Driver Circuits

Figure 14 presents several circuits for generating the $\overline{CS}$/WE signal. Circuit a is very simple, providing the three necessary levels for on board programming. Circuit b has increased driving capability and isolation over circuit a, and will allow more noise margin. In addition, the inclusion of the two 100Ω resistors provide short circuit protection in case of socketing or soldering errors. A truth table is included with circuits a and b to indicate the various input/output conditions. Circuit c provides only two levels, V_{IL} (0V) and V_{IHW} (+12V), for use in "program and verify only" circuits; the PROM cannot be deselected using this circuit. Another way of generating the 0 and +12V signals would be to use a TTL to MOS driver, such as the Intel® 3245.

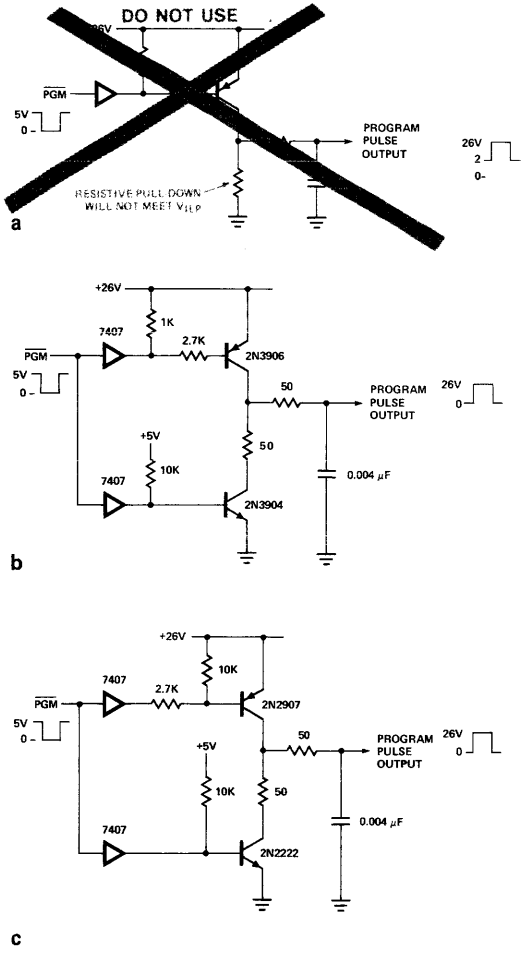


Figure 13. Program Pulse Driver Circuits

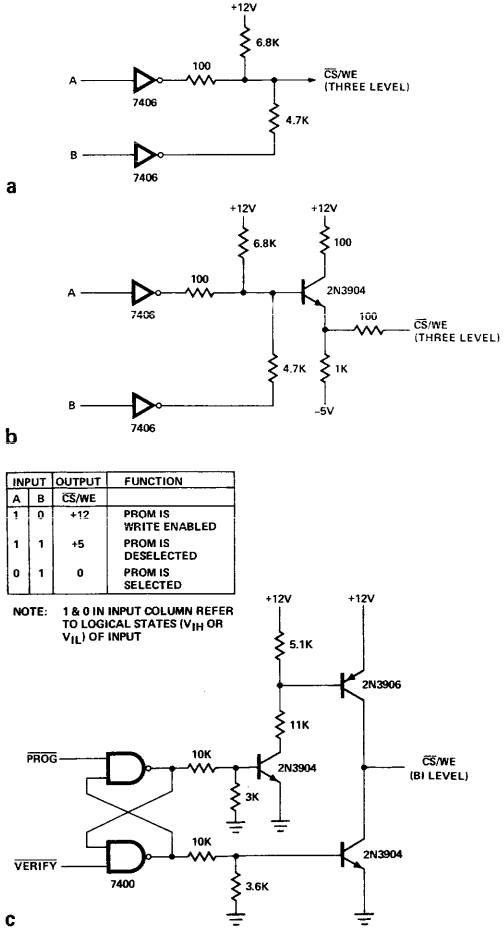


Figure 14. $\overline{CS}$/WE Driver Circuits

On Board Programming

Unlike many other erasable and programmable Read Only Memories, the 2708 can be soldered directly into a printed circuit board and programmed while "in circuit", as the inputs and outputs stay low level compatible during both read and program modes of operation. When erasure is required, the circuit board is unplugged and placed under a UV lamp for the required period of time.

In many microprocessor systems, it is quite easy to implement the RAM storage required for a data base when programming by using available RAM storage. Be sure to observe all the required setup times if the address and data bus will be performing non-programming related functions while the PROM is being programmed.

Figure 15 illustrates a possible scheme for implementing a data output/input buffer.

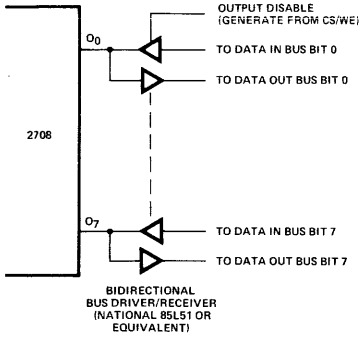


Figure 15. Data Output/Input Buffer

To take advantage of this feature, which is not tested or included as part of the device specifications, the program pulse should be applied to all devices as shown in Figure 16. Program decode is then accomplished by way of the $\overline{CS}$/WE pin. PROM's to be programmed have this pin raised to the V_{IHW} level (+12V), while it is left at V_{IH} ($\overline{CS}$=3V) for those parts which are not to be programmed. Reserve should be built into the program pulse power supply when operation in this mode is planned, but in no case will it exceed the maximum of 20 mA per 2708 as specified in Table III.

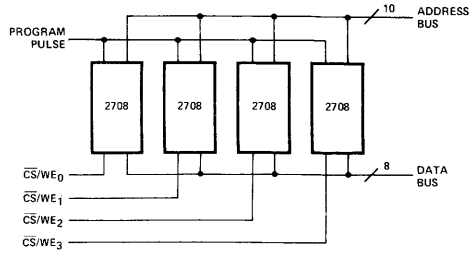


Figure 16. Circuit Implementation for On-Board Programming

ERASING

The 2708 is erased by exposure to ultra-violet light at a wavelength of 2537Å. The recommended integrated dosage (i.e. UV intensity X exposure time) is 15 W-sec/cm^2. In order to insure that all bits are erased, this dosage includes a guard band and is not equal to the dosage required to see the last bits return to the initial state. A guard band of 3 to 4 times the initial period (that time which appears to erase all bits) is suggested so that the device will appear erased at extremes of temperature and voltage.

Table V. UV Sources for Erasing the 2708

Model	Power Rating	Typical Time to Erase a 2708 Device
S-68	12000 uW/cm^2	15 minutes
S-52	12000 uW/cm^2	15 minutes
UVS-54	5700 uW/cm^2	45 minutes
R-52	13000 uW/cm^2	15 minutes
UVS-11	5500 uW/cm^2	45 minutes

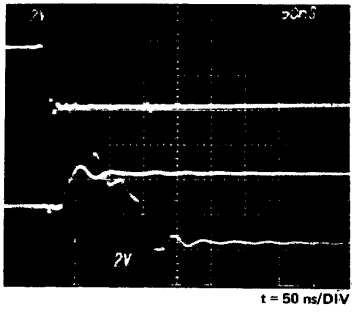
Table V lists several UV sources for erasing the 2708. The model numbers referred to are manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, CA).

The times indicated are for the lamps placed about 1 inch away from the parts to be erased and without shortwave filters installed. For lamps other than those listed, the required times can be determined empirically or by means of an ultra-violet intensity meter, such as the UV Products Model J-225. When a meter is used, the intensity should be determined at the same location (distance from UV tube) as the PROM will be placed; this will require careful measurement to insure that the sensor is receiving exactly the same amount of UV light that the PROMs will receive.

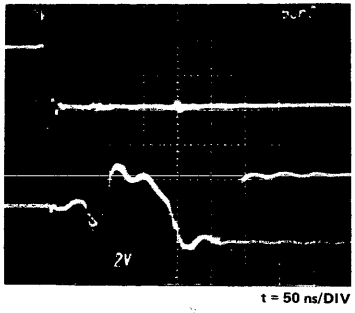
APPLICATIONS

Switched Power Supplies

Although not specified in the D.C. and A.C. DEVICE SPECIFICATIONS sections, the 2708 can be operated in a power down mode by switching off the V_{DD} power supply. This is advantageous in many applications where power dissipation is a critical factor, such as battery operated or battery backed-up systems. Referring to Table II, the maximum I_{DD} power that can be saved by switching the V_{DD} power supply is 780 mW. Two factors should be noted, however. First of all, the access time will increase somewhat, as shown in Figure 17.



a. WITHOUT SWITCHED V_{DD}



b. WITH SWITCHED V_{DD}

Figure 17. 2708 Access Time

The photos were taken using the circuit of Figure 18, at room temperature and with a small sample of parts. Based on this information, the PROM data strobe should be moved out approximately 150 ns to allow a guard band for the system. The second point related to the switching of V_{DD} is the reduction of V_{BB} current (I_{BB}). Figure 19 indicates that I_{BB} decreases to an average of approximately 8 mA when V_{DD} is off.

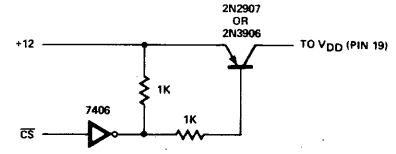
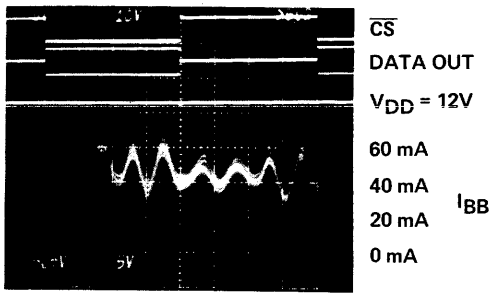
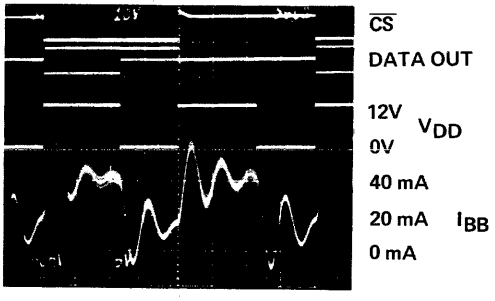


Figure 18. Circuit for Switching V_{DD}



a. WITHOUT SWITCHED V_{DD}



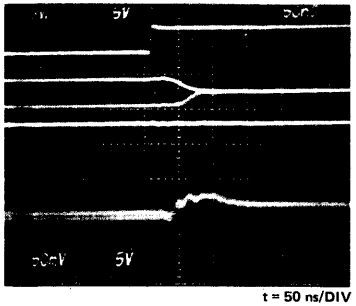
b. WITH SWITCHED V_{DD}

Figure 19. 2708 I_{BB} Current

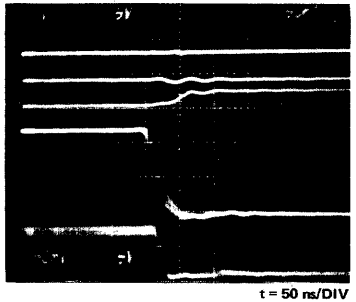
As shown in Figure 20, output deselection occurs within t_{DF} (Chip Select to Output Float Delay) when $\overline{CS}$ is held low and V_{DD} is switched.

Switching off V_{CC} will save some power, but the maximum value is so low (10 mA) that the extra components required for switching are probably not justified. Typical values of I_{CC} decrease about 50% when the V_{DD} supply is switched off.

The V_{BB} supply could also be switched, but, considering the reduction when the V_{DD} supply is switched off, the additional components required to switch this supply would probably not be justified, either. In addition, unless an extra power supply of −10 to −15 volts is available for a driver circuit, access time would be significantly degraded (laboratory data indicates about 50 μs).



a. WITHOUT SWITCHED V_{DD}



b. WITH SWITCHED V_{DD}

Figure 20. 2708 Output Deselection and I_{DD} Current

Another way of reducing power is to leave the device continuously selected and control the output by way of an enable signal on a latch or gate. Referring to Figure 8, this method would reduce power dissipation nearly 50%, as the device does dissipate less power when $\overline{CS}$/WE is low.

OR Tie Considerations

When two or more 2708's are wire ORed together, care should be exercised to see that valid data will be obtained. Referring back to Figure 7 and Figure 21, if two devices are selected at the same time, a current path can exist from Q_1 to Q_4 is shown in Figure 21. This current can be destructive to the output stage of one of the devices, or, the transistor with greater current sourcing or sinking capability can cause false data to be read from the output bus. In addition, the very high V_{CC} current drawn while both Q_1 and Q_4 are on will generate noise on the V_{CC} power supply lines, and possibly reduce the V_{CC} that is connected to other TTL control circuits, causing momentary false indications. If the maximum chip deselect to output float delay (t_{DF}) is observed, there will be no problem. The same type of situation can occur when the 2708 is used in conjunction with other memory devices, such as the RAM portion of the programmer shown in Figure 11. Careful analysis of the system timing requirements and maximum delay paths can eliminate these problems before they occur at the final checkout of a system.

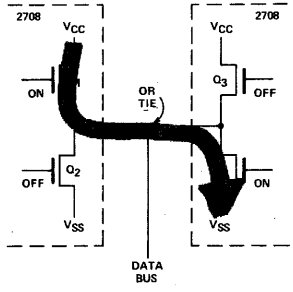


Figure 21. Results of Improper Timing when OR Tying 2708's

High Voltage CMOS Interface

Because the 2708 is erased by the same technique as the Intel® 1702A, some users have assumed that the various techniques for interfacing to high voltage CMOS circuits are similar. In fact, they are not. The 1702A is a p-channel device, requiring two power supplies (+5V and –9V), while the 2708 is a n-channel device and requires three power supplies (+12V, +5V and –5V). It is permissible to assign the ground (0V) to the most negative supply and reference all the other supplies to it; however, suitable level shifters must be used to provide the 2708 with suitable input level signals, and to convert the output signals back to the system reference levels. Figure 22 shows a possible voltage translation.

SUPPLY	2708 VOLTAGE	SYSTEM VOLTAGE
V_{DD}	+12V	+17V
V_{CC}	+ 5V	+10V
V_{SS}	0V	+ 5V
V_{BB}	- 5V	0V
V_{IL}	0 to +0.65	+5.0 to +5.65
V_{IH}	+3.0 to +6.0	+8.0 to +11.0
V_{OL}	+0.45	+5.45
V_{OH}	+2.4 @ –1 mA	+7.4

Figure 22. 2708 Voltage Translation

Some suitable translator circuits are: RCA CD4009/4010 or National F/4104/34104. The use of these circuits also allows some high voltage CMOS logic to be implemented, such as address and data clocks, at the CMOS levels, rather than convert them to TTL levels for operation of the 2708.

Another incorrect method of attempting to interface directly to CMOS circuits is to change the V_{CC} supply to the new interface voltage. In devices such as the Intel® 2107B this is permissible, as the V_{CC} supply is connected to the output buffer stage, but in the 2708, the +5V is used in the sense amplifier and other internal circuitry, so this should not be done.

Under Programming and Under Erasing

It is possible to "under program" the 2708, such that the cell characteristic crosses the sense threshold. The result of this is that the cell apparently drops or picks up bits. As can be seen in Figure 23, the threshold characteristic has been shifted such that small changes in voltage or temperature will cause a "1" or a "0" to be sensed. This is always the result of insufficient erasing or programming. For erasure to cause this problem, the device has only been partially programmed, and the characteristic curve has only been shifted to the sense threshold point and the device will again seem to either pick up or drop bits. The cure, in either case, is to 1) adequately erase by providing the required 10 W-sec/cm^2 of UV light at a frequency of 2537Å, or 2) program in accordance with the specifications.

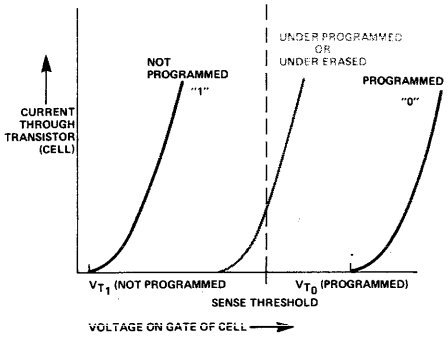


Figure 23. Effect of Under Programming or Under Erasure

ACKNOWLEDGEMENT

I would like to extend my thanks and appreciation to the Technology Development Group for their assistance in preparing the background material for this Application Note.

Application of the Intel® 2716 16K 5V Erasable PROM

Bob Greene
Application Engineering

Contents

INTRODUCTION

The INTEL® 2716 is a fully static 16,384-bit (2048 x 8) Eraseable Programmable Read Only Memory, or EPROM. The device is packaged in a standard 24-pin DIP, which has a transparent lid to allow erasure in a manner similar to that of the INTEL® 1702A and 2708. Maximum access time is 450ns. The device requires a single power supply (V_{CC} = 5V ±5%) for normal read cycles; during programming the program power supply (V_{PP}) must be raised to +25V to program each location, a single TTL level pulse is required; one 50ms pulse per address programs 8 bits in parallel. The addresses can be randomly programmed.

All input signals are fully TTL compatible during both the read and program modes. The data outputs are three state to facilitate memory expansion by OR tying. Initially and after each erasure the 2716 contains all TTL highs ("1"s); programming or introducing TTL lows ("0"s) is accomplished by: 1) raising the V_{PP} pin from +5V to +25V, 2) applying TTL level addresses and TTL level data, 3) raising the $\overline{CS}$ pin to a TTL high, and 4) applying a single 50ms TTL level pulse to the PD/PGM input.

The V_{PP} supply may be left at the +25V level for program verification, but should be returned to +5V level during normal read cycles to reduce power dissipation.

DEVICE DESCRIPTION

The 2716 is packaged in an industry standard 24 pin DIP as shown in Figure 1. The functions of the various control pins are shown in Table I.

During read operation $\overline{CS}$ is used to select and deselect the 2716. The PD/PGM pin is maintained at V_{IL}, while V_{PP}, the program power supply, is maintained at +5V. As shown in the D.C. Device Characteristics Section, I_{PP1} (the current required by pin 21) is 5mA maximum during read mode, so pin 20 should be kept at V_{CC} except when programming. As a convenience to users, it is allowable to keep the V_{PP} pin at +25 volts for program verification, but it must be returned to +5V upon completing program verification. This is easily accomplished by connecting a diode from pin 24 to pin 21 as shown in Figure 2. The tolerance on V_{PP} allows for a diode drop as discussed in the D.C. Operating Characteristics section. For read only applications, the V_{PP} pin may be tied directly to the V_{CC} pin.

Table I. 2716 Pin Connections and Functions.

MODE \ PINS	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

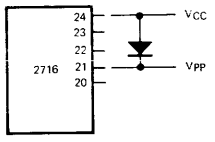
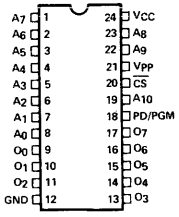


Figure 2. 2716 Power Supply Connections.



PIN NAMES

A_0–A_{10}	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O_0–O_7	OUTPUTS

Figure 1. 2716 Pin Configuration.

The PD/PGM input serves several functions. When low this signal enables the address, data and $\overline{CS}$ input buffers, whether V_{PP} is at +25V or +5V. When high with V_{PP} at +5V, the 2716 is powered down and the outputs are deselected without regard for the state of $\overline{CS}$. In this mode the maximum I_{CC} current is reduced from 100mA to 25mA. When $\overline{CS}$ is high and V_{PP} is at 25V, the data present on the output will be programmed into the selected address when PD/PGM is pulsed high (from V_{IL} to V_{IH}) for 50ms.

A block diagram for the 2716 is shown in Figure 3. The array of stacked gate cells is arranged as two 64 x 128 matrices, each of which is split into four 16 x 128 segments. The high order address bits (A_4-A_{10}) determine which of the 128 rows is to be accessed by way of the top select gate, while the low order address bits (A_0-A_3) perform the column decode function by activating the 1 of 16 decoders which are associated with each output bit.

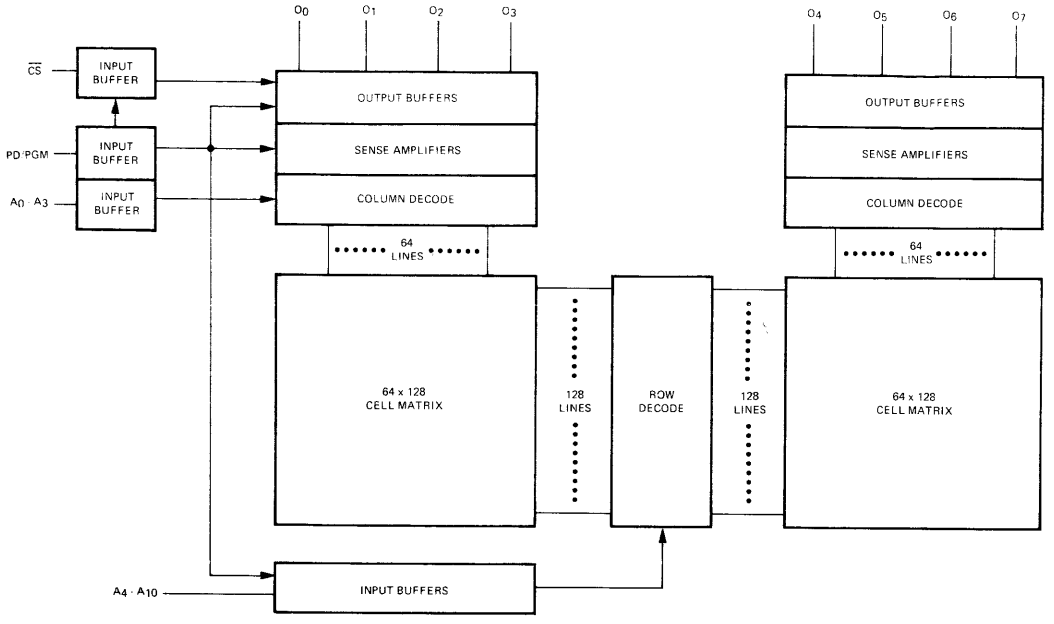


Figure 3. Detailed Block Diagram.

Cell Description

The heart of the 2716 is the single transistor stacked gate cell, which is similar to the cell used in the INTEL® 2708. The cell consists of a floating gate, used to store charge, and a top select gate which is connected to the output of the row decoder. The cell is programmed by injection of high energy electrons through the isolating oxide and onto the floating gate. Once there, the charge is trapped, as there are no electrical connections to the floating gate. The presence of electrons on the floating gate causes a shift in cell threshold, as shown in Figure 4. In the initial or erased state the threshold of the cell is low, selection via the top gate will cause the column line to discharge, which is sensed as a "HIGH" by the sense amplifier. Programming shifts the threshold to a higher level, and selection of the cell will not turn it on, the column line will not discharge, and a low will be sensed by the sense amplifier. The status of the cell is determined by examining its state at the sense threshold; if the cell is erased (HIGH data) selection will cause a higher current to flow between the source and drain than if the cell is programmed (LOW data).

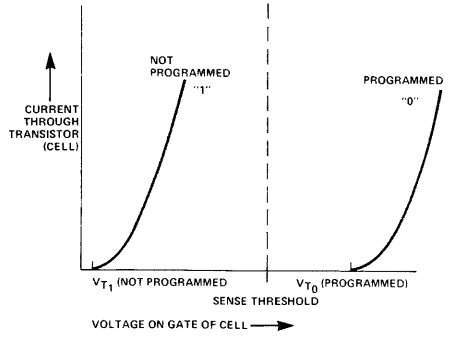


Figure 4. Storage Cell Threshold Shift

Memory Array Operation

The cells described in the previous paragraph are interconnected to form a split 128 x 128 cell matrix, as shown in Figure 3. This array is divided into 8 sections organized as 16 x 128 cells. Each of these sections is connected to a column decoder, which selects one of 16 columns, connecting it to the sense amplifier which is associated with the particular bit. The sense amplifier is directly connected to the output buffer associated with the same bit. This data flow is illustrated graphically in Figure 5.

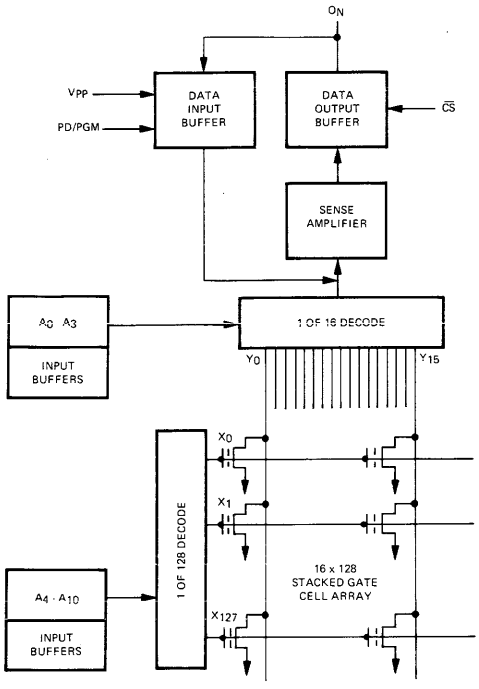


Figure 5. 2716 Single Bit Data Flow.

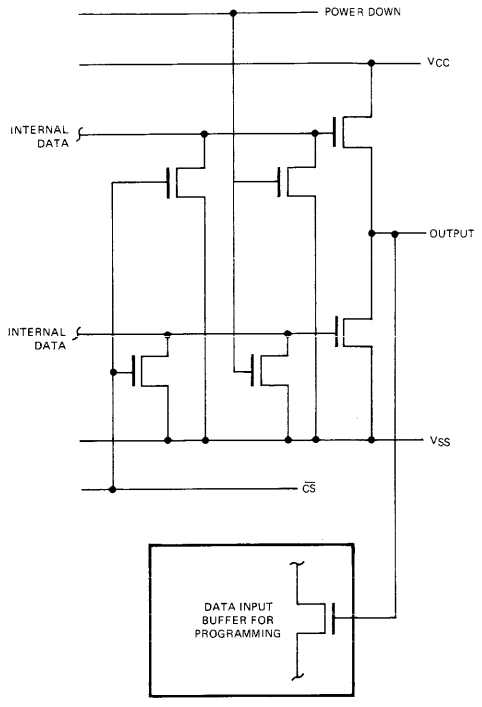


Figure 6. 2716 Output Buffer.

Output Buffer

An equivalent schematic of the output buffer is shown in Figure 6. As is shown, the output buffer consists of a pair of MOS transistors, connected in a push-pull configuration. $\overline{CS}$ enables both transistors when true; when $\overline{CS}$ is false both output devices are turned off. The PD/PGM input also is related to the output buffer and does place the output buffer in the high impedence state when the internal signal Power Down is high. This signal is normally low for regular read operations, and functions as an output deselect when high. Remember that if V_{PP} is at +25V and $\overline{CS}$ is high, raising PD/PGM high will cause a program cycle on the selected address.

READ MODE

The 2716 requires only one power supply, +5V. The device is rated to meet all applicable specifications with this supply held within ±5% of its nominal value. The Absolute Maximum Ratings in the data sheet are the maximum that the various device parameters can withstand and should not be exceeded during any phase of device operation, including programming.

D.C. Characteristics

Only those D.C. Characteristics that require special attention by the user are presented in this section. The reader is referred to the 2716 device data sheet for further details. The pertinent D.C. device specifications are tabulated in Table II.

The range of the leakage currents shown in Table II apply for all inputs and outputs, including the outputs (O_0-O_7) when they are serving as data inputs for programming.

I_{PP1} is the current required by the V_{PP} pin (pin 21) when the V_{PP} supply is set to 5V, as it would be for normal read operations. The device specification requires a ±5% tolerance on the V_{CC} supply. In anticipation that users will couple pin 21 to pin 24 by way of a diode, the tolerance on V_{PP} has been relaxed to ±0.6V to allow for the forward drop of the diode.

I_{PP} is only applicable to the current drawn by pin 21 when the PD/PGM pulse is low; when it is high (as in the case of the program pulse) the current drawn by this pin will be 30mA.

I_{CC1} is the power supply current when PD/PGM is high and V_{PP} is at a nominal 5V, and represents 25% of the total maximum I_{CC} current. As was discussed previously, the outputs are automatically placed in the high impedance state when the PD/PGM pin is raised to V_{IH}. I_{CC2} is the maximum power supply current required by a 2716 in read mode, and reaches this maximum of 500mW (30μW/bit) at maximum temperature.

Table II. 2716 D.C. and Operating Characteristics.

$T_A = 0°C$ to $70°C$, V_{CC}[1,2] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[4]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.85V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	PD/PGM = V_{IH}, $\overline{CS}$ = V_{IL}
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{CS}$ = PD/PGM = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.2		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.
4. Typical values are for T_A = 25°C and nominal supply voltages.
5. This parameter is only sampled and is not 100% tested.
6. t_{ACC2} is referenced to PD/PGM or the addresses, whichever occurs last.

ROMS

All inputs are TTL compatible, requiring a VIL between -.01 and 0.8V and a V_{IH} of 2.2V minimum. Care should be exercised in selecting address buffers to ensure that the minimum V_{IH} level is met by use of appropriate TTL circuit elements or pull-up resistors to V_{CC}.

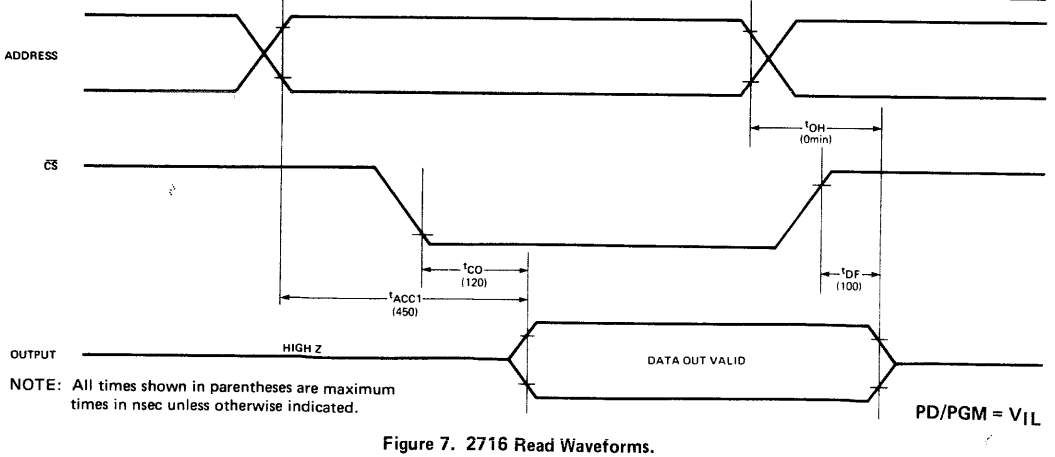
The outputs are also TTL compatible, producing a V_{OL} of 0.45V maximum at 2.1mA and a V_{OH} of 2.4V with -400mA capability.

A.C. Characteristics

Figure 7, the read mode timing indicates the maximum or minimum timing for the various timing parameters. Particular attention should be paid to t_{DF}, chip deselect to output float time. This parameter indicates that the output buffers of the 2716 are not guaranteed to reach the high impedence state until 100ns after $\overline{CS}$ reaches V_{IH}. If another device takes control of the output node before the first device output is in the high impedence state, excessive I_{CC} current will be drawn. See the Applications Section for further discussion.

Power Down Mode

The 2716 is the first MOS EPROM to have a completely static power down mode. This mode is activated by raising the PD/PGM input to a TTL high level, with V_{PP} = 5V.

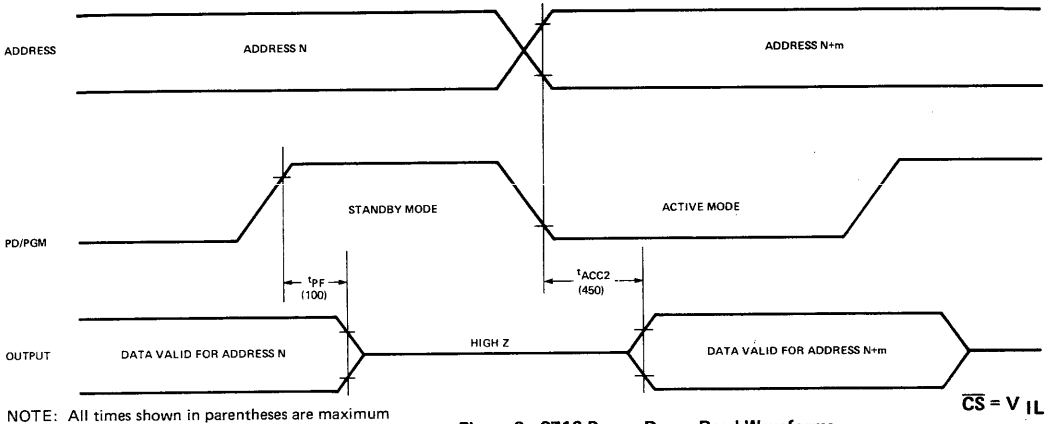


NOTE: All times shown in parentheses are maximum times in nsec unless otherwise indicated.

Figure 7. 2716 Read Waveforms.

The power is reduced by 75% (from 500mW to 125mW) during the time PD/PGM is high.

When the PD/PGM pin is lowered to a TTL low level, the access time (t_{ACC2}) of 450ns is met as shown in Figure 8. Of course, t_{ACC2} is referenced to either the addresses becoming stable or to the rising edge of PD/PGM, whichever occurs last. Table III summarizes the A.C. Characterstics for both normal and power down read cycles.



NOTE: All times shown in parentheses are maximum times in nsec unless otherwise indicated.

Figure 8. 2716 Power Down Read Waveforms.

Table III. 2716 A.C. Characteristics.

$T_A = 0°C$ to $70°C$, V_{CC}[1] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[4]	Max.		
t_{ACC1}	Address to Output Delay		250	450	ns	PD/PGM = $\overline{CS}$ = V_{IL}
t_{ACC2}	PD/PGM to Output Delay		280	450	ns	$\overline{CS}$ = V_{IL}
t_{CO}	Chip Select to Output Delay			120	ns	PD/PGM = V_{IL}
t_{PF}	PD/PGM to Output Float	0		100	ns	$\overline{CS}$ = V_{IL}
t_{DF}	Chip Deselect to Output Float	0		100	ns	PD/PGM = V_{IL}
t_{OH}	Address to Output Hold	0			ns	PD/PGM = $\overline{CS}$ = V_{IL}

PROGRAM MODE

D.C. Characteristics

The 2716 requires a single TTL level pulse to program each address with the V_{PP} supply set to 25V. Addresses can be programmed in any sequence. The V_{PP} supply can be left at +25V continuously while programming; it can also be left at +25V for program verify cycles, but must be returned to the +5 volt level for normal read cycles to reduce power dissipation. A maximum of 30mA will be drawn from the V_{PP} supply when the PD/PGM pulse is high and $\overline{CS}$ is high; during read operations the I_{PP1} specification of 5mA applies.

The address and data inputs are TTL compatible during programming, with the same requirements of V_{IL} and V_{IH} as for the Read Mode. The D.C. Characteristics for programming are shown in Table IV. To enable the device for programming, the $\overline{CS}$ pin is taken to V_{IH} and the correct address and data inputs provided. After the appropriate set up times, (see Figure 9) a single pulse from V_{IL} to V_{IH} on the PD/PGM input for 50ms programs the desired address.

During program operation, the outputs become the data inputs and should be treated as a three state bus. The same leakage, as well as V_{IL} and V_{IH} specifications apply to the outputs as for the inputs during normal read operations.

The program pulse, which is a TTL pulse of 50ms duration, is applied to the PD/PGM input. During the time that this pulse is high, a maximum of 30mA (I_{CC2}) will be required from the V_{PP} power supply. V_{PP} can be left high (at +25V) to verify the programmed data, however, it must be returned to the 5V level to reduce power dissipation. Also, in order to reduce power dissipation, the PD/PGM pulse must not be left high longer than 55ms when

Table IV. 2716 D.C. Programming Characteristics.

$T_A = 25°C \pm 5°C$, V_{CC}[2] = 5V ±5%, V_{PP}[2,3] = 25V ±1V

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Input Current (for Any Input)			10	μA	V_{IN} = 5.25V/0.45
I_{PP1}	V_{PP} Supply Current			5	mA	PD/PGM = V_{IL}
I_{PP2}	V_{PP} Supply Current During Programming Pulse			30	mA	PD/PGM = V_{IH}
I_{CC}	V_{CC} Supply Current			100	mA	
V_{IL}	Input Low Level	-0.1		0.8	V	
V_{IH}	Input High Level	2.2		V_{CC}+1	V	

NOTES: 1. Intel's standard product warranty applies only to devices programmed to specifications described herein.

2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The 2716 must not be inserted into or removed from a board with V_{PP} at 25 ±1V to prevent damage to the device.

3. The maximum allowable voltage which may be applied to the V_{PP} pin during programming is +26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification.

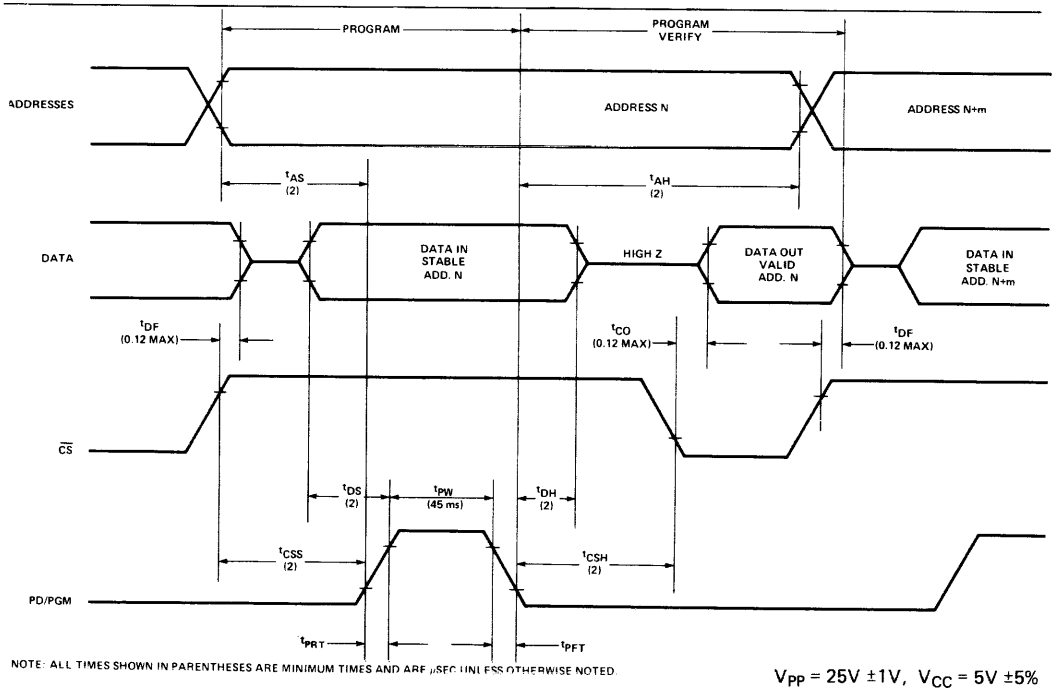


Figure 9. 2716 Programming Waveforms.

the V_{PP} supply is at +25V; it can be left high only with V_{PP} at +5V, which deselects the output and places the device in the low power standby mode.

The tolerance on the V_{PP} supply is 25V ±1V. When switching the V_{PP} supply from +5V to +25V, particular care should be taken to ensure that there is no overshoot above 26V; exceeding this can be destructive to the programming circuits on the device. It is also not permitted to "hot socket" the device in a programmer (with respect to the V_{PP} supply) as the resulting transients could cause the V_{PP} supply to exceed the maximum of 26V.

A.C. Characteristics

Figure 9 indicates the program mode timing, while Table V tabulates the various programming A.C. parameters.

To program a 2716, the address, data and $\overline{CS}$ signals must all be stable 2μs before the PD/PGM pin is pulsed high for 50ms ±5ms. This is shown in

Figure 9 as t_{AS}, t_{DS} and t_{CS}. After the falling edge of the program pulse, these same signals must be held stable for 2μs (t_{AH}, t_{DH} and t_{CSH}); then the next address and data can be presented, sequentially or not according to the ease of system implementation, and the next address programmed. In this manner it is possible to program an entire 2716 in approximately 100 seconds, while a single address requires only 50ms to program.

PROGRAMMING

A number of programmers are commercially available that will properly program the 2716. (see Table VI) Intel maintains a service whereby commercial programmer manufacturers obtain design approval prior to marketing their device, in order to assure compatibility with Intel specifications. This approval should be verified with the particular manufacturer prior to purchase.

For those users who want to build their own programmer, a design is included at the end of this section.

Figure 10 illustrates a typical 2716 programmer block diagram. The address & data inputs can come from a system bus, or from toggle or thumbwheel switches. If system inputs are used, the Address Input Buffer should be a latch to allow the system bus to be free during the 50ms program time per address. The Data Input/Output Buffer should be of the bi-directional type to allow both programming and data verification.

The start control activates the timing chain to generate the required address and data setup and hold times, as well as the program pulse.

The program timer latches the address and data inputs stable and raises CS to V_{IH}, while the address and data setup timer delays the start of the program pulse for at least 2μs, which is the minimum re-

Table V. 2716 A.C. Programming Characteristics.

$T_A = 25°C \pm 5°C$, V_{CC}[2] = 5V ±5%, V_{PP}[2,3] = 25V ±1V

Symbol	Parameter	Min.	Typ.	Max.	Units	
t_{AS}	Address Setup Time	2			μs	
t_{CSS}	$\overline{CS}$ Setup Time	2			μs	
t_{DS}	Data Setup Time	2			μs	
t_{AH}	Address Hold Time	2			μs	
t_{CSH}	$\overline{CS}$ Hold Time	2			μs	
t_{DH}	Data Hold Time	2			μs	
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns	PD/PGM = V_{IL}
t_{CO}	Chip Select to Output Delay			120	ns	PD/PGM = V_{IL}
t_{PW}	Program Pulse Width	45	50	55	ms	
t_{PRT}	Program Pulse Rise Time	5			ns	
t_{PFT}	Program Pulse Fall Time	5			ns	

NOTES: 1. Intel's standard product warranty applies only to devices programmed to specifications described herein.

2. V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp. The 2716 must not be inserted into or removed from a board with Vpp at 25 ±1V to prevent damage to the device.

3. The maximum allowable voltage which may be applied to the Vpp pin during programming is +26V. Care must be taken when switching the Vpp supply to prevent overshoot exceeding this 26V maximum specification.

Table VI. Approved Programmers.

	1602A/1702A Family	2708 Family	2716 Family	3601 Family	3602/3622 Family	3604/3624 Family
Intel MDS-UPP-100 Santa Clara, Calif.	X	X	X	X	X	X
Data I/O Model V Issaquah, Wash.	X	X	X	X	X	X
Prolog Series 90 Monterey, Calif.	X	Note 1	Note 1	X	X	X
Spectrum Dynamics Series 350 Burlington, Mass.	X	Note 1	Note 1	Note 1	Note 1	Note 1

Note 1. This programming card is pending Intel approval.

quired address and data setup time (t_{AS} and t_{DS}). The program pulse timer is activated by the falling edge of the address and data setup timer, and generates the required 50ms program pulse. The falling edge of the program pulse activates the address and data hold timer, (2μs minimum) and the falling edge of the data hold timer resets the program times, releasing the latch on the address and data in buffers, freeing the system for either a verify cycle or a program cycle on another address.

On board programming is also very easily implemented with the 2716, as the PD/PGM pin functions as a program inhibit, i.e., if a given device has $\overline{CS}$ high, V_{PP} = 25V, and PD/PGM low, it will not be programmed. A system showing how on-board programming could be implemented is shown in Figure 11. In the figure, device #4 will have address IFF_H programmed with $F4_H$, while the contents of address IFF in devices #1, #2 and #3 will be unaffected.

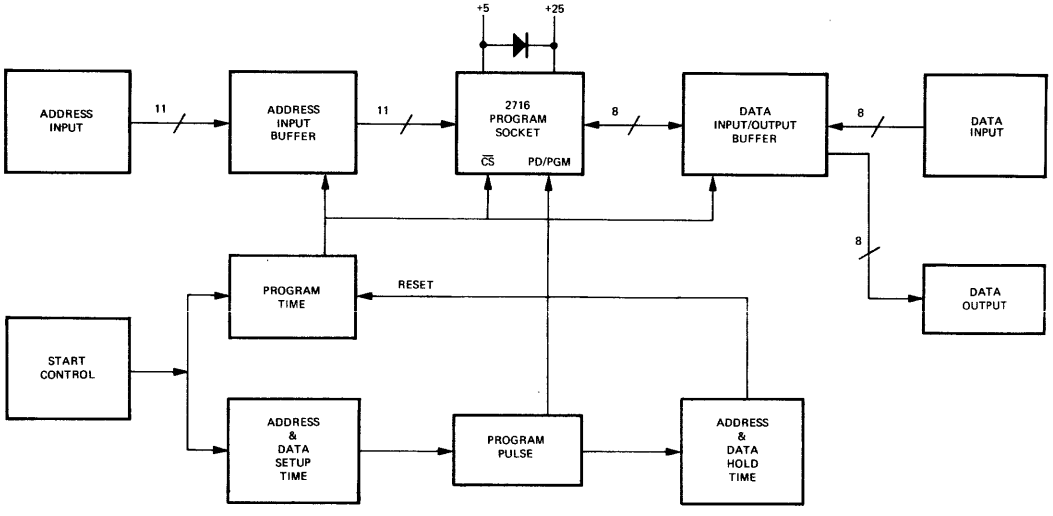


Figure 10. 2716 Programmer Block Diagram.

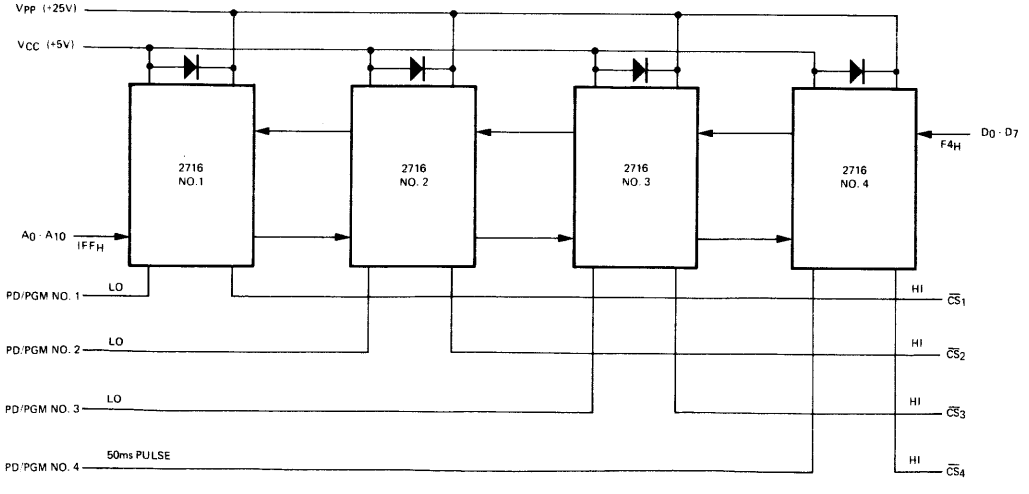


Figure 11. 2716 On Board Programming.

2716 Mini Programmer

Figure 12 presents the schematic for a 2716 programmer which is based on the block diagram shown in the previous section. This programmer has been design approved by Intel, by the same procedure used for commercial programmer manufacturers. The programmer has several features that make it useful for small development labs.

Manual Programming

Selecting any Hex address with the 3 address input thumb wheel switches and entering it by depressing the load button will cause the selected address to be displayed in Hex. The data is then entered by way of the 2 Hex thumb wheel data switches. When programming the data, the PROGRAM button is depressed, the location indicated by the address display is programmed and the address incremented to the next sequential location. For verification a verify mode is included that will automatically slowly step through all addresses, allowing for manual, visual verification of the programmed data. The rate at which it sequences through the addresses is adjustable, and can be started at any location by way of the ADDRESS INPUT and LOAD ADDRESS switches.

Duplicate Mode

By selecting the duplicate mode, a 2716 placed in the READ ONLY socket will be duplicate and automatically compared with a 2716 placed in the PROGRAM socket. After verification a green "PASS" or a red "FAIL" LED will indicate the completion of the program cycle. A blank check is not performed.

The design described here does not include a power supply design—the user must provide appropriate +5 volt and +25 volt power supplies. Current requirements, as measured on the prototype board, are about 1 A at +5 V and 60 mA at 25 V.

The design also includes a transistor switch to prevent hot socketing of the 2716. As was mentioned in the programming section, it is not permitted to install a 2716 in a socket with the +25 volts present: it must be switched on after the 2716 is in the socket and +5 volts is applied.

ERASING

Erasure begins to appear when the 2716 is exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3.5 years while it would take approximately 1 month to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2716 should be placed within one inch from the lamp tubes during exposure. Some lamps have a filter on their tubes and this filter should be removed before erasure.

The 2716 should not be under bias during erasure as current paths exist that will effectively cancel the energy being provided by the UV light.

UV Sources

There are several models of UV lamps that can be used to erase 2716's (see Table VII). The model numbers in the table refer to lamps manufactured by Ultra Violet Products of San Gabriel, Calif. In addition there are several other manufacturers, including Data I/O, PRO-LOG, Prometrics, and Turner Designs. The individual manufacturers should be consulted for detailed product descriptions.

Table VII. 2716 Erase Time.

MODEL	POWER RATING	REQUIRED TIME FOR INDICATED DOSAGE
		15 W-sec 2716
R-52	13000μW/cm^2	19.2 min
S-52	12000μW/cm^2	20.7 min
S-68	12000μW/cm^2	20.7 min
UVS-54	5700μW/cm^2	43.8 min
UVS-11	5500μW/cm^2	45.6 min

According to the manufacturers, the output of the UV lamp bulb decreases with age. The output of the lamp should be verified periodically to ensure that adequate intensities are maintained. If this is not done, bits may be partially erased which will interfere with later programming and/or operation at high temperature.

For lamps other than those listed, the erase time can be determined by using a UV intensity meter, such as the Ultra Violet Products model J-225. When a meter is used, the intensity should be measured at the same position (distance from the lamp) as the EPROMs to be erased. This will require careful positioning to insure that the sensor will receive the same amount of UV light that the window of the EPROM will receive.

The sensors used with most UV intensity meters showed reduced output with constant exposure to UV light. Therefore they should not be permanently placed inside the erasure enclosure; they should only be used for periodic measurements.

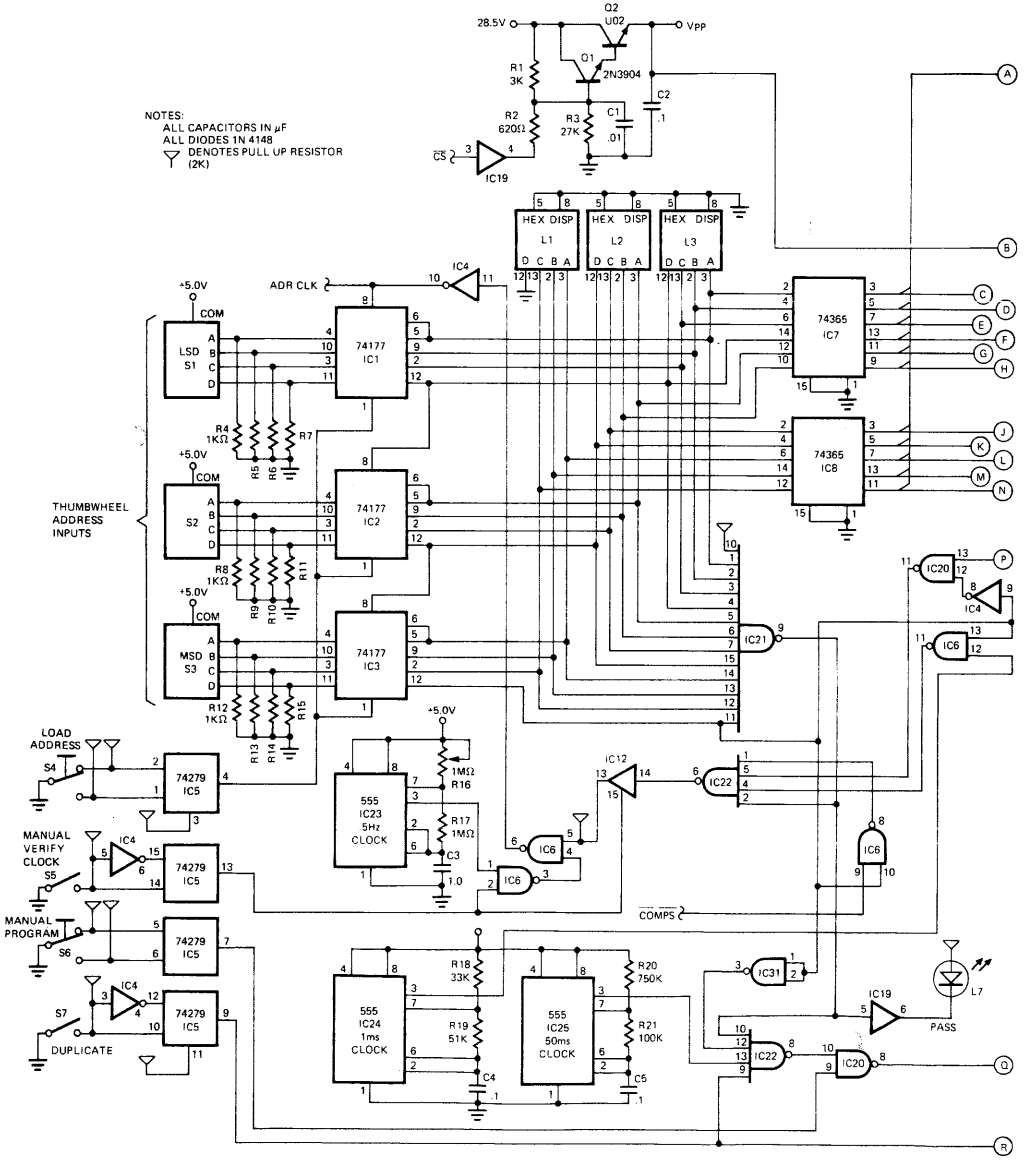
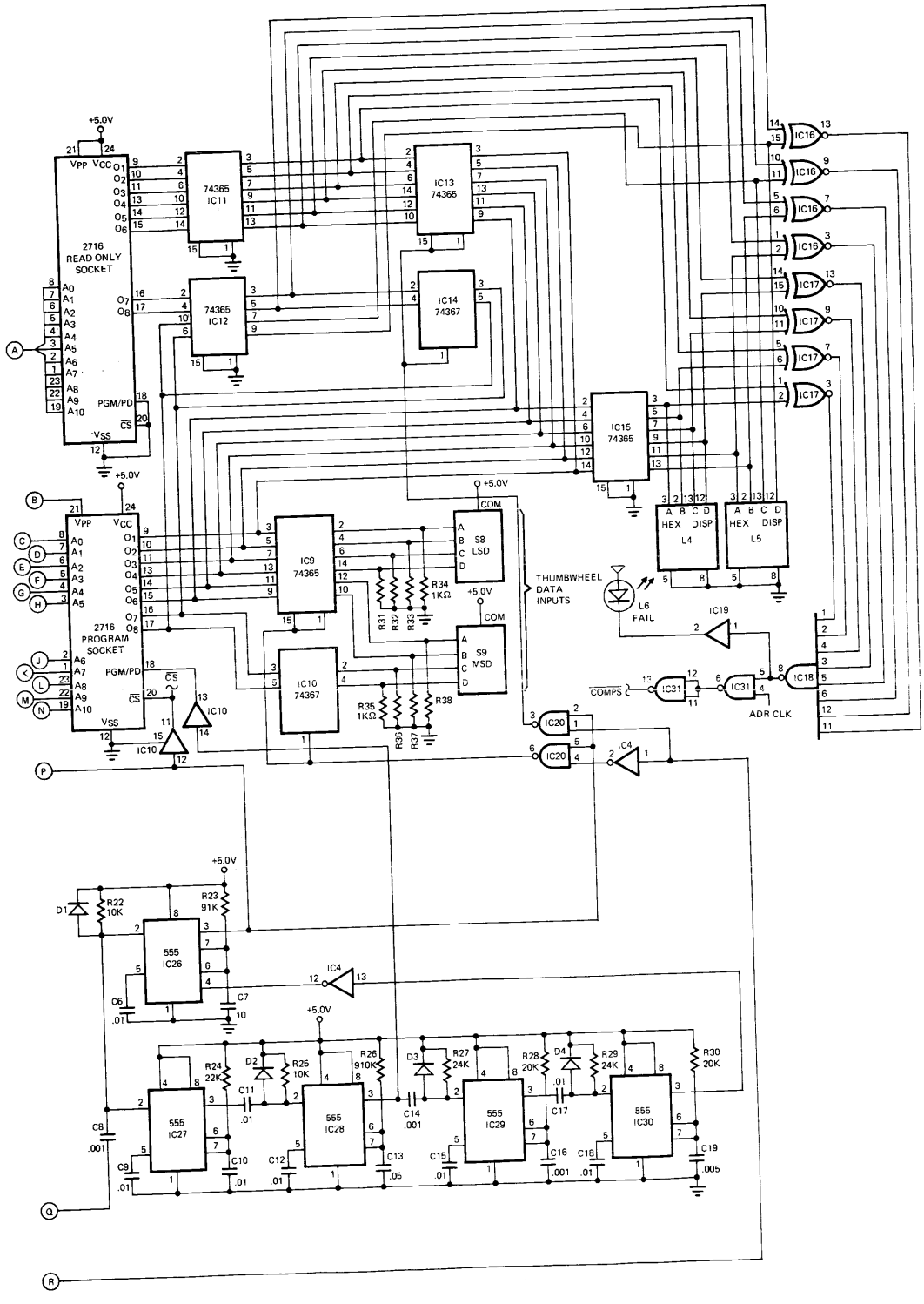


Figure 12. 2716 Mini Programmer Schematic.


+5.0V
2716
READ ONLY
SOCKET
74365
IC11
74365
IC12
IC13
74365
IC14
74367
IC15
74365
IC16
IC17
2716
PROGRAM
SOCKET
IC9
74365
IC10
74367
S8
LSD
S9
MSD
COM
R31
R32
R33
R34
1KΩ
R35
1KΩ
R36
R37
R38
THUMBWHEEL
DATA
INPUTS
HEX DISP
L4
HEX DISP
L5
L6
FAIL
IC19
COMPS
IC31
IC18
ADR CLK
IC20
IC4
IC10
555
IC26
555
IC27
555
IC28
555
IC29
555
IC30
R22
10K
R23
91K
R24
22K
R25
10K
R26
910K
R27
24K
R28
20K
R29
24K
R30
20K
D1
D2
D3
D4
C6
.01
C7
C8
.001
C9
.01
C10
.01
C11
.01
C12
.01
C13
.05
C14
.001
C15
.01
C16
.001
C17
.01
C18
.01
C19
.005

Under Programming And Under Erasing

It is possible to "under program" the 2716 the same as it is with the 2708, such that the cell characteristic crosses the sense threshold. The result is that the cell apparently drops or picks up bits. As can be seen in Figure 13, the threshold characteristic has been shifted such that small changes in voltage or temperature will cause a "1" or a "0" to be sensed. This is always the result of insufficient erasing or programming. For programming to cause this problem, the device has only been partially programmed, and the characteristic curve has been shifted to the sense threshold point and the device will again seem to either pick up or drop bits. For erasure to cause the problem, the device has only been partially erased, such that the characteristic curve has only been shifted (right to left in the figure) to the threshold.

The cure in either case is to: 1) adequately erase by providing the required 15 W-sec/cm^2 of UV light at a frequency of 2537Å or; 2) program in accordance with the specifications.

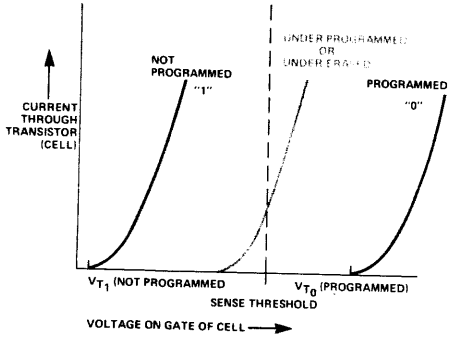


Figure 13. Effect of Under Programming or Under Erasure

2716 Mini Programmer

The Mini Programmer shown on the previous pages has been design approved by Intel and can be built as shown, or portions of the circuit can be modified to fit a specific user circuit application.

Circuit Description

The Mini Programmer has several modes of operation which are described below.

Manual Program – Controlled by pushbutton switch S6, this mode allows the user to program the address displayed by the address input displays (L1-L3) with the data that is entered in the data input thumbwheels (S8 & S9). The desired address to be programmed is entered by way of the LOAD ADDRESS switch, S4. This transfers the contents of the address input thumbwheel switches (S1-S3) to the address input buffers and the address display LEDs, L1-L3.

The desired data is entered in the form of two hexadecimal characters by way of the data input thumbwheel switches, S8 & S9. Prior to programming, the data output display will read FF_H, indicating that the addressed location contains all highs, i.e., is erased.

After the displayed address is programmed, the output display will momentarily display the contents of the programmed address, and then increment the address by 1 count, thus preparing the next sequential address to be programmed. Should other than the next sequential be desired, it is only necessary to dial in the new address and depress the LOAD ADDRESS pushbutton.

Manual Verify – In order to assure the user that the correct data pattern has been entered in an entire program, a manual verify function has been included. In this mode, the address counter will slowly cycle through addresses starting with the address that was loaded by the LOAD ADDRESS switch. The rate at which the counter will cycle is controlled by R16, and should be set for convenient visual recognition of the programmed data.

Duplicate Mode – Duplicate mode allows the contents of another 2716 to be programmed into an erased device that is inserted in the program socket. Each location is programmed and verified, and the next sequential location is programmed. Upon completion, PASS-FAIL indication is provided by way of LEDs L6 and L7.

Transistors Q1 and Q2 provide for switching V_{PP} between 26V and 5V, while assuring that proper sequence and overshoot control is maintained.

Table VIII. 2716 Mini Programmer Parts List.

IC1-3	74177	4-Bit Counter
IC4	7404	Hex Driver
IC5	74279	Quad Set/Reset Latch
IC6, 20, 31	7400	Quad NAND
IC7-15	74367	Hex Tristate Driver
IC16, 17	74135	Quad Exclusive OR/NOR Gates
IC18	7430	8-Input NAND
IC19	7407	Open Collector, High Voltage Driver
IC21	74133	13-Input NAND
IC22	7420	Dual 4-Input NAND
IC23-30	NE555	Timer
Q1	MPS UO2	Transistor
Q2	2N3904	Transistor
R1	3KΩ	¼W Resistor
R2	820Ω	¼W Resistor
R3	27KΩ	¼W Resistor
R4-15, 31-38	1KΩ	¼W Resistor
R16	1MΩ	Potentiometer (VERIFY Clock Rate)
R4-15	1KΩ	¼W Resistor
R31-38	1KΩ	¼W Resistor
R16	1MΩ	Potentiometer
R17	1MΩ	¼W Resistor
R18	33KΩ	¼W Resistor
R19	51KΩ	¼W Resistor
R20	750KΩ	¼W Resistor
R21	100KΩ	¼W Resistor
R22	10KΩ	¼W Resistor
R23	91KΩ	¼W Resistor
R24	22KΩ	¼W Resistor
R25	10KΩ	¼W Resistor
R26	910KΩ	¼W Resistor
R27, 29	24KΩ	¼W Resistor
R28, 30	20KΩ	¼W Resistor
C1, 6, 9-12, 15, 17, 18	0.01μF	Capacitor 20 wvdc (min)
C2, 4, 5	0.1μF	Capacitor 20 wvdc (min)
C3	1.0μF	Capacitor 20 wvdc (min)
C7	10μF	Capacitor 20 wvdc (min)
C8, 14, 16	0.001μF	Capacitor 20 wvdc (min)
C13	0.05μF	Capacitor 20 wvdc (min)
C19	0.005μF	Capacitor 20 wvdc (min)
S1-S3		(LSD-MSD): Address Input Switches (Cherry T-10 Thumbwheel)
S4		Address Load (Pushbutton)
S5		1Hz Verify Clock SPST Switch
S6		Program Button (Pushbutton)
S7		Duplicate Mode SPST Switch
S8, S9		(LSD-MSD): Data Input (Cherry T-10 Thumbwheel)
PROM Sockets		Textool 24-Pin ZIP DIP
L1-L5		TIL311 Hexadecimal Display
L6		MV5025 (Red LED)
L7		MV5253 (Green LED)

MOS ROM AND PROM FAMILY

	Type	No. of Bits	Organization	No. of Pins	Output[1]	Maximum Access (ns)	Maximum Power Dissipation (mW)	Operating Temperature Range (°C)	Power Supply (V)
SILICON GATE MOS ROM	**2308**	8192	1024x8	24	T.S.	450	840	0 to 70	5V ± 5% 12V ± 5% -5V ± 5%
	2316A	16384	2048x8	24	T.S.	850	515	0 to 70	5V ± 5%
	2316E	16384	2048x8	24	T.S.	450	630	0 to 70	5V ± 10%
SILICON GATE MOS PROM	**1702A**	2048	256x8	24	T.S.	1μs	885	0 to 70	5V ± 5% -9V ± 5%
	1702A-2	2048	256x8	24	T.S.	650	959	0 to 70	5V ± 5% -9V ± 5%
	1702A-6	2048	256x8	24	T.S.	1.5 μs	885	0 to 70	5V ± 5% -9V ± 5%
	M1702A	2048	256x8	24	T.S.	850	960	-55 to 100	5V ± 10% -9V ± 10%
	1702AL	2048	256x8	24	T.S.	1 μs	221	0 to 70	5V ± 5% -9V ± 5%
	1702AL-2	2048	256x8	24	T.S.	650	221	0 to 70	5V ± 5% -9V ± 5%
	2704	4096	512x8	24	T.S.	450	800	0 to 70	5V ± 5% 12V ± 5% -5V ± 5%
	2708	8192	1024x8	24	T.S.	450	800	0 to 70	5V ± 5% 12V ± 5% -5V ± 5%
	2708-1	8192	1024x8	24	T.S.	350	800	0 to 70	5V ± 5% 12V ± 5% -5V ± 5%
	M2708	8192	1024x8	24	T.S.	450	750	-55 to 100	5V ± 10% 12V ± 10% -5V ± 10%
	2716	16384	2048x8	24	T.S.	450	525/132[2]	0 to 70	5V ± 5%

Notes: 1. O.C. and TS are open collector and three-state output respectively.
2. The 2716 has a standby power down feature.

BIPOLAR PROM FAMILY

Type	No. of Bits	Organization	No. of Pins	Output[1]	Maximum Access (ns)	Maximum Power Dissipation (mW)	Operating Temperature Range (°C)	Power Supply (V)
3601	1024	256x4	16	O.C.	70	685	0 to 75	5V ±5%
3601-1	1024	256x4	16	O.C.	50	685	0 to 75	5V ± 5%
3621	1024	256x4	16	T.S.	70	685	0 to 75	5V ± 5%
3621-1	1024	256x4	16	T.S.	50	685	0 to 75	5V ± 5%
M3601	1024	256x4	16	O.C.	90	685	-55 to 125	5V ± 5%
3602A	2048	512x4	16	O.C.	70	735	0 to 75	5V ± 5%
3602A-2	2048	512x4	16	O.C.	60	735	0 to 75	5V ± 5%
3602	2048	512x4	16	O.C.	70	735	0 to 75	5V ± 5%
3622A	2048	512x4	16	T.S.	70	1735	0 to 75	5V ± 5%
3622A-2	2048	512x4	16	T.S.	60	735	0 to 75	5V ± 5%
3622	2048	512x4	16	T.S.	70	735	0 to 75	5V ± 5%
3604A	4096	512x8	24	O.C.	70	998	0 to 75	5V ± 5%
3604A-2	4096	512x8	24	O.C.	60	998	0 to 75	5V ± 5%
3604AL	4096	512x8	24	O.C.	90	630/105[2]	0 to 75	5V ± 5%
3604	4096	512x8	24	O.C.	70	998	0 to 75	5V ± 5%
3604-4	4096	512x8	24	O.C.	90	998	0 to 75	5V ± 5%
3604L-6	4096	512x8	24	O.C.	90	735/240[2]	0 to 75	5V ± 5%
3624A	4096	512x8	24	T.S.	70	998	0 to 75	5V ± 5%
3624A-2	4096	512x8	24	T.S.	60	998	0 to 75	5V ± 5%
3624	4096	512x8	24	T.S.	70	998	0 to 75	5V ± 5%
3624-4	4096	512x8	24	T.S.	90	998	0 to 75	5V ± 5%
M3604	4096	512x8	24	O.C.	90	1045	-55 to 125	5V ± 10%
M3624	4096	512x8	24	T.S.	90	1045	-55 to 125	5V ± 10%
3605	4096	1024x4	18	O.C.	70	787	0 to 75	5V ± 5%
3605-2	4096	1024x4	18	O.C.	60	787	0 to 75	5V ± 5%
3625	4096	1024x4	18	T.S.	70	787	0 to 75	5V ± 5%
3625-2	4096	1024x4	18	T.S.	60	787	0 to 75	5V ± 5%
3608	8192	1024x8	24	O.C.	80	998	0 to 75	5V ± 5%
3608-4	8192	1024x8	24	O.C.	100	998	0 to 75	5V ± 5%
3628	8192	1024x8	24	O.C.	80	998	0 to 75	5V ± 5%
3628-4	8192	1024x8	24	O.C.	100	998	0 to 75	5V ± 5%

Notes: 1. O.C. and T.S. are open collector and three-state output respectively.
2. The 3604AL and 3604L-6 have a low power dissipation feature.

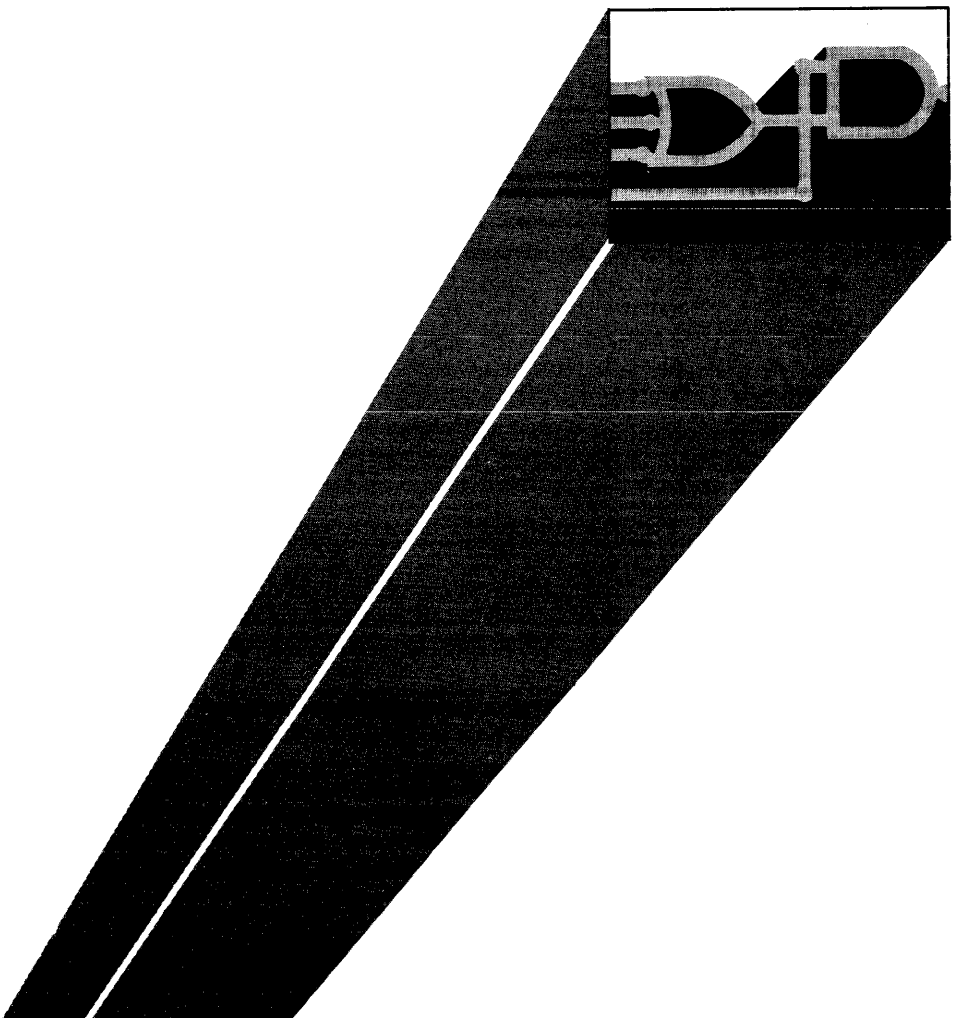
BIPOLAR PROM CROSS REFERENCE

Part Number	Prefix and Manufacturer	Organization	Intel Part Number	
			Direct Replacement	For New Designs[1]
1024-4	HPROM—Harris	256 x 4	3621	
1024A-2	HPROM—Harris	256 x 4	M3601	
1024A-5	HRPOM—Harris	256 x 4	3601	
27S10C	AMD	256 x 4	3601	
27S10M	AMD	256 x 4	M3601	
27S11C	AMD	256 x 4	3621	
27S11M	AMD	256 x 4	M3621	
5300-1	MMI	256 x 4	M3601	
5340-1	MMI	512 x 8	M3604	
5341-1	MMI	512 x 8	M3624	
54S387	SN—TI	256 x 4	M3601	
54S387	DM—National	256 x 4	M3601	
5603AC	IM—Intersil	256 x 4	3601	
5603AM	IM—Intersil	256 x 4	M3601	
5604C	IM—Intersil	512 x 4	3602A	
5605C	IM—Intersil	512 x 8	3604A	
5623C	IM—Intersil	256 x 4	3621	
5624C	IM—Intersil	512 x 4	3622A	
5625C	IM—Intersil	512 x 8	3624A	
6300-1	MMI	256 x 4	3601-1	
6301-1	MMI	256 x 4	3621-1	
6305-1	MMI	512 x 4	3602A-2	
6306-1	MMI	512 x 4	3622A-2	
6340-1	MMI	512 x 8	3604A	
6341-1	MMI	512 x 8	3624A	
6352-1	MMI	1024 x 4	3605-2	
6353-1	MMI	1024 x 4	3625-2	
6380-1	MMI	1024 x 8	3608	
6381-1	MMI	1024 x 8	3628	
74S287	SN—TI	256 x 4	3621-1	
74S287	DM—National	256 x 4	3621-1	
74S387	SN—TI	256 x 4	3601-1	
74S387	DM—National	256 x 4	3601-1	
74S472	TI	512 x 8		3624
74S473	TI	512 x 8		3604
74S474	TI	512 x 8	3624A	
74S475	TI	512 x 8	3604A	
74S570	National	512 x 4	3602A	
74S571	National	512 x 4	3622A	
7573	DM—National	256 x 4	M3601	
7610-2	HM—Harris	256 x 4		M3601
7610-5	HM—Harris	256 x 4	3601-1	
7611-5	HM—Harris	256 x 4	3621-1	
7620-5	HM—Harris	512 x 4	3602A	
7621-5	HM—Harris	512 x 4	3622A	
7640-2	HM—Harris	512 x 8		M3604
7640-5	HM—Harris	512 x 8	3604A	
7641-2	HM—Harris	512 x 8		M3624
7641-5	HM—Harris	512 x 8	3624A	
7642-5	HM—Harris	1024 x 4	3605	
7643-5	HM—Harris	1024 x 4	3625	
7644-5	HM—Harris	1024 x 4		3625

Part Number	Prefix and Manufacturer	Organization	Intel Part Number	
			Direct Replacement	For New Designs[1]
82S115	N—Signetics	512 x 8		3624
82S115	S—Signetics	512 x 8		M3624
82S126	N—Signetics	256 x 4	3601-1	
82S126	S—Signetics	256 x 4		M3601
82S129	N—Signetics	256 x 4	3621-1	
82S130	N—Signetics	512 x 4		3602
82S131	N—Signetics	512 x 4		3622
82S140	N—Signetics	512 x 8	3604A	
82S141	N—Signetics	512 x 8	3624A	
82S136	N—Signetics	1024 x 4	3605-2	
82S137	N—Signetics	1024 x 4	3625-2	
82S180	N—Signetics	1024 x 8		3608
82S181	N—Signetics	1024 x 8		3628
82S184	N—Signetics	2048 x 4		3608
82S185	N—Signetics	2048 x 4		3628
8573	DM—National	256 x 4	3601	
8574	DM—National	256 x 4	3621	
87S295	National	512 x 8	3604A	
87S296	National	512 x 8	3624A	
93416C	Fairchild	256 x 4	3601	
93416M	Fairchild	256 x 4		M3601
93426C	Fairchild	256 x 4	3621	
93436C	Fairchild	512 x 4		3602
93438C	Fairchild	512 x 8		3604
93438M	Fairchild	512 x 8		M3604
93446C	Fairchild	512 x 4		3622
93448C	Fairchild	512 x 8		3624
93448M	Fairchild	512 x 8		M3624
93452C	Fairchild	1024 x 4	3605-2	
93453C	Fairchild	1024 x 4	3625-2	

NOTE: 1. The Intel® PROMs have the same pin configuration and differ only in access time from the PROMs in the first column. The exceptions are the 6350, 6351, 82S115, and 82S184/85 which have different pin configurations.

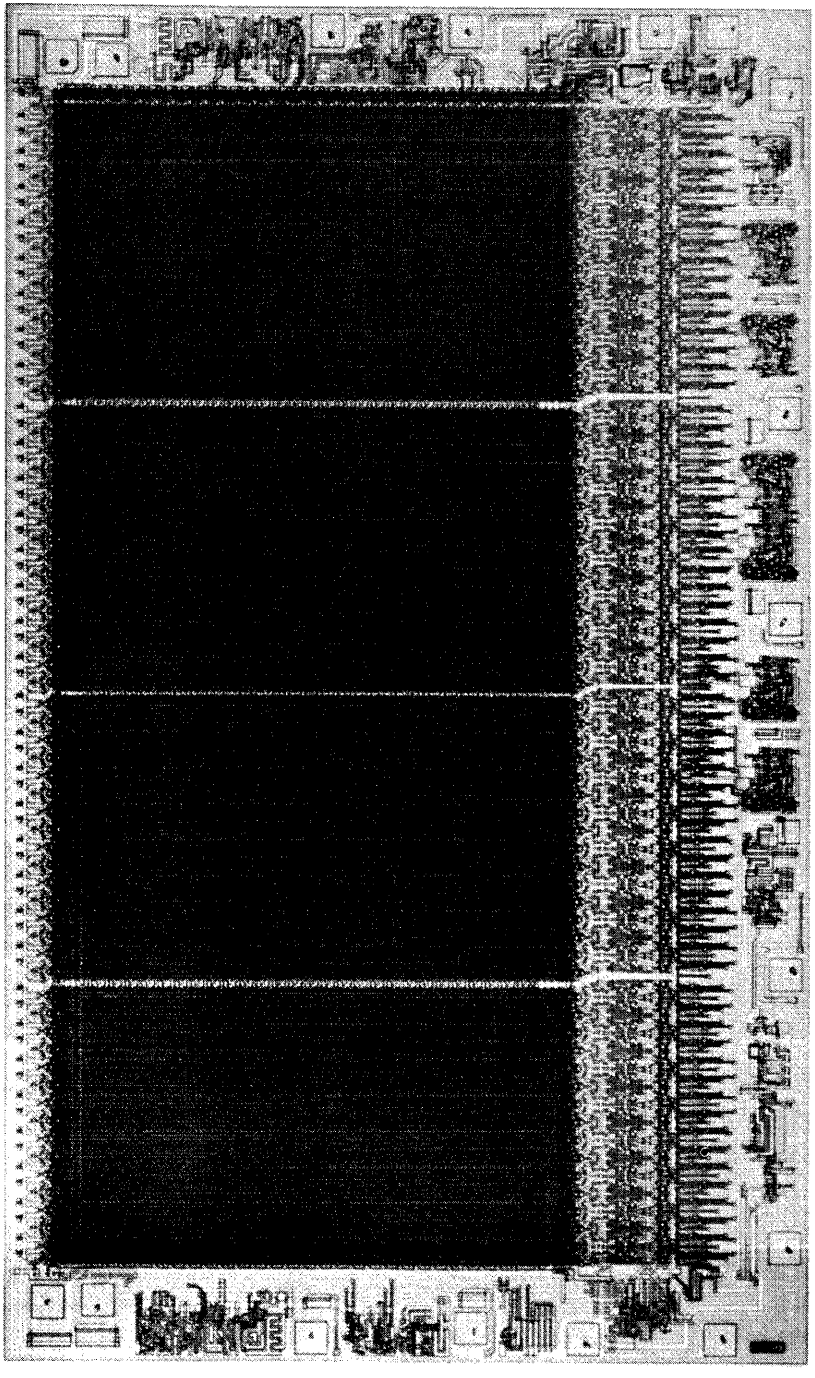
Serial Memories



Design and Applications of Intel's 2416 16K Charge Coupled Device

Bob Papenberg
Application Engineering

Contents



Photomicrograph of 2416 16,384 Word x 1 Bit CCD

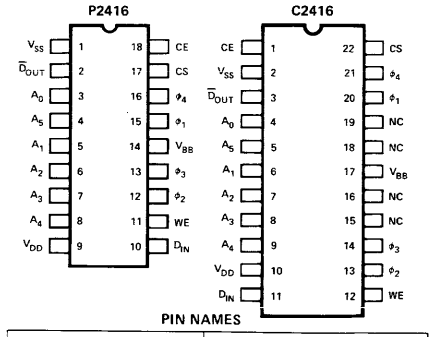
INTRODUCTION

The Intel® 2416 is a 16,384 word X 1-bit CCD serial memory designed for very low-cost memory applications. The memory is configured as 64 independent recirculating shift registers of 256 bits each. Access to any one of the 64 internal shift registers is done by applying the appropriate code to the 6 address inputs. The 2416 is fabricated using Intel's advanced high voltage n-channel silicon gate MOS process.

The 2416 memory device utilizes the simple surface channel structure and inherent very high density of a charge coupled device. This, in addition to a unique memory organization, provides an extremely versatile, dense and reliable memory unit. The purpose of this application note is to provide the system design engineer with an insight into the organization, structure, technology and operation of the 2416 device.

This application note is divided into three major sections: 1). Internal device organization, operation and specifications; 2). Device operation in a system; and 3). System organization examples. It is particularly important to users unfamiliar with the 2416 to carefully review the first section on organization and operation. A thorough understanding of the device will increase the versatility of the device to the user.

Information is also presented on interfacing clock and control signals to the 2416 in a system environment. Several specific applications are shown to illustrate the versatility of the 2416.



PIN NAMES

A_0-A_5	ADDRESS INPUTS	CE	CHIP ENABLE INPUT
D_{IN}	DATA INPUT	ϕ_1-ϕ_4	CCD CLOCK INPUTS
WE	WRITE ENABLE INPUT	V_{DD}, V_{SS}, V_{BB}	POWER SUPPLIES
CS	CHIP SELECT INPUT	$\overline{D}_{OUT}$	DATA OUTPUT

Figure 1. 2416 Pin Configuration.

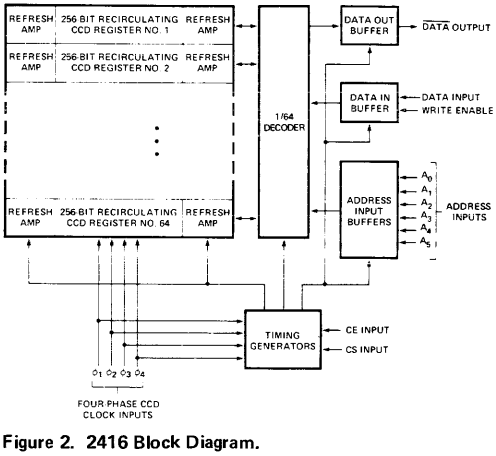


Figure 2. 2416 Block Diagram.

2416 INTERNAL ORGANIZATION AND OPERATION

The 2416 operates with the industry standard power supplies for memory components: V_{DD} = 12.0V and V_{BB} = -5.0V. The output is implemented with an open drain device which allows OR tieing of the outputs. For TTL operation the output pin is usually tied to a resistor which is returned to V_{CC} (+5V). The pin configuration for the 18 and 22 pin versions of the 2416 are shown in Figure 1.

The 2416 internal memory organization combines both serial and random address memory functions. As shown in Figure 2, the 2416 is arranged as 64-256 bit charge coupled device (CCD) shift registers. The data in these registers is simultaneously shifted by exercising the four-phase clock signals ϕ_1 through ϕ_4. After a shift cycle, each of the 64 CCD registers can be selected for an input/output (I/O) function by applying the appropriate 6-bit address code and applying cenable, chip select and write-enable signals in the required manner.

The flexibility of the 2416 internal memory organization in memory systems applications cannot be overemphasized. It is necessary for the designer to have a clear understanding of this organization to be able to take maximum advantage of the capability of the 2416.

The organization of the 2416 is most easily seen by referring to the diagram in Figure 3. In this diagram, the CCD is visualized as a cylinder comprised of 64 "tracks" (representing the 64 CCD recirculating shift registers) with each track divided into 256 "sectors" (representing the 256 CCD data storage cells). The "rate of rotation" of the cylinder is controlled by the four-phase clocks and is in the direction indicated by the "shift direction" arrow shown in Figure 3. (Note that the four-phase clocks *always* shift the cylinder in the same direction. The clocks cannot be manipulated to reverse the shift direction).

Read/Write capability in the CCD is performed by 64 bi-directional data buffers (one data-buffer per track). These buffers are located in position A shown in Figure 3 as the shaded column. The cylinder is considered to rotate *through* the buffers so that each shift of the cylinder (controlled by the four-phase clocks) places the next sequential sector of each track "in" the buffer. The buffers shown in column A also provide a refresh function to each cell in addition to performing read/write functions. (Note that an additional refresh-only buffer is shown in column B of Figure 3. These buffers are located half way around the cylinder as shown.)

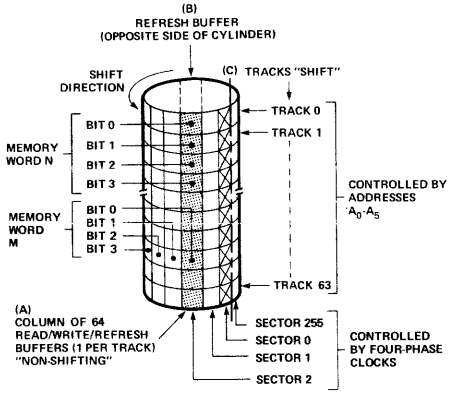


Figure 3. Symbolic 2416 Organization.

Two basic addressing methods may be used to store data words in the 2416:

1. In a given sector.
2. Around a given track.

In the first method, the desired word is accessed by shifting the cylinder (using the four-phase clocks) until the sector (0-255) containing the word is coincident with the read/write buffers (shown as column A). The word is then accessed one bit at a time by addressing the appropriate track with addresses A_0-A_5. An example of this addressing technique is shown as the four bit memory word N shown in Figure 3. The second addressing method places a word sequentially around the cylinder in a given track. Access to a particular word requires both a four-phase clock shift followed by a data access cycle for each bit of the word. (Note that for this case, A_0-A_5 do not change once the desired track is accessed.) An example of this addressing technique is shown as four bit memory word M in Figure 3.

Because of system addressing problems it is not generally desirable to combine the two addressing methods at once (although it is certainly possible). As is shown in the Systems Considerations section, addressing method 1 (sector addressing) is usually the more preferable technique. A major advantage of this data organization is the low four-phase clock driver power required to achieve the maximum serial data transfer rate of 2 megabits/sec from a single 2416. In most serial applications, the four-phase clock signals are only required to operate at less than 55 kHz rate to obtain a 2 MHz I/O data rate. *This is because the four-phase clocks are used solely to shift/refresh data and are not used to perform input/output functions.* For each shift of the clock, 64 "new" data bits are available in the 64 internal data registers for access through the address, chip enable and read/write control signals. These data control signals have a low input capacitance which makes them very easy to drive.

An alternate method of visualizing the organization of the 2416 is shown in Figure 4. This diagram is derived from the cylinder shown in Figure 3 by imagining that the cylinder is cut along the line marked C (between sector 0 and 255) and laying the cylinder out flat as shown in Figure 4.

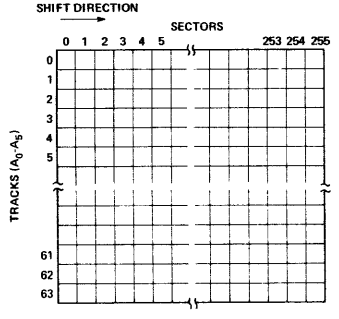


Figure 4. Planar View Symbolic 2416 Organization.

CCD Structure

There are two common CCD types referred to as surface channel and buried channel. The surface channel is characterized by the storing and transferring of charge (data) along the surface of the substrate. The buried channel type, because of additional substrate doping, stores and transfers the charge (data) further into the bulk of the substrate.

The primary differences in characteristics between the surface channel and buried channel is that the surface channel has: (1) higher total charge carrying capability, (2) lower charge transfer efficiency at extremely high charge transfer rates. (However, it is noted that the loss of charge transfer efficiency occurs at a frequency much higher than the maximum shift frequency of the 2416.) (3) simpler fabrication process. Charge transfer efficiency, number

2 above, is defined as the percentage of the total charge packet (data) which is actually shifted or transferred per shift (the efficiency is typically greater than 99.9% per shift).

The 2416 internal memory array is comprised of four-phase surface channel charge-coupled structures. The CCD structure is formed by a series of MOS thinfield gate oxide devices placed as shown in Figure 5. Note that these MOS devices do not have the source/drain diffusions usually associated with other MOS structures. Figure 5(a) is the top view of the storage array and illustrates that the clock phases are laid out perpendicular to the shift register channels. Electrical isolation between shift register channels is obtained by channel stop diffusions and thick film oxide methods. Data input/output connections to the registers are obtained from n+ diffusions at the ends of the registers.

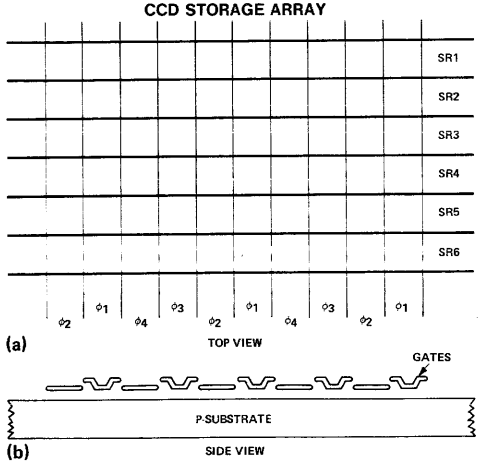


Figure 5. CCD Storage Array Layout.

Data Storage

The CCD stores data in the form of charge, as do all dynamic MOS memory devices. Indeed, in many respects the storage mechanism of the 2416 is very similar to the 4096 bit random access memories implemented with single transistor cells (such as Intel's 2107B). The storage element is most easily understood if it is considered to resemble a "potential well." This potential well is formed when a positive voltage potential is applied on the clock gates. The positive voltage repels the majority substrate carriers (holes) from the vicinity of the gate and forms a charge depletion area under it. This depleted region has the capability of accepting and storing a negative charge packet as long as the gate forming the well remains sufficiently positive with respect to the substrate.

The CCD structure is inherently dynamic and therefore must be refreshed periodically to maintain data. The dynamic nature of a CCD device is the result of thermally generated carriers (traditionally called "dark current effect") which acts to fill an uncharged potential well with charge thereby changing that particular cell's logic state.

Data Transfer

Figure 6 shows the relationship between the 2416 four-phase clock sequence and the CCD data storage and transfer mechanism.

The position of potential wells relative to the four-phase clock levels is shown in Figure 6(a). When the clocks are sequenced in the manner outlined in Figure 6(b), the potential wells generated provide a "low impedance" path for the charge packets to follow.

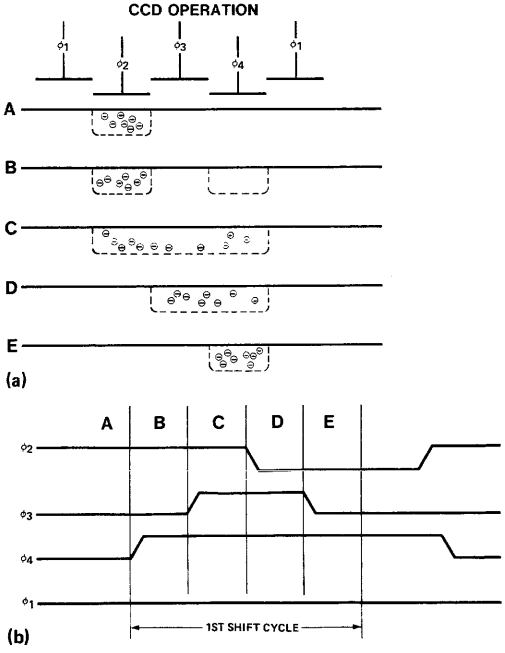


Figure 6. 2416 Charge Transfer Mechanism.

At time A, only the ϕ_2 gates are at a high level forming a storage well under the ϕ_2 gates. The storage well is assumed to contain an externally injected charge packet. The origin of the charge packet will be discussed later. At time B, both ϕ_2 and ϕ_4 gates are high and an additional storage well is formed in the substrate under the ϕ_4 gates. Note that the storage wells under the ϕ_4 gates do not now contain charge packets. At time C, ϕ_2, ϕ_3 and ϕ_4

gates are all high which forms ϕ_3 storage wells overlapping both the ϕ_2 and ϕ_4 storage wells. Thus a continuous storage well is formed from the ϕ_2 gates to the ϕ_4 gates which allows charge packets under ϕ_2 gates to disperse throughout the charge wells of all three gates. At time D, the ϕ_2 gate goes to a low level eliminating the storage well under it. This forces the charge packet into the remaining storage wells under the ϕ_3 and ϕ_4 gates. At time E, the charge transfer is complete when the ϕ_3 gate voltage goes low which forces the charge packet into the remaining storage well under the ϕ_4 gate. The charge packet (data) has now been shifted by one bit position. Note that the shift execution time shown in Figure 6 is the time that data is being shifted as defined by periods B, C, and D.

Applying clocks in the above manner (ϕ_3 shift) results in a parallel shift of all data. Another shift cycle can then begin by utilizing ϕ_1 and ϕ_4 (ϕ_1 shift) thus completing a full cycle on the four-phase clocks. The shifting mechanism using the ϕ_1 and ϕ_4 clocks is identical to that described for the ϕ_3 and ϕ_2 clocks.

CCD Internal Data Interface

Each of the 256-bit CCD shift registers is comprised of two 128-bit registers. Each of the two 128-bit registers is further multiplexed into dual 64-bit registers (making the 256-bit register a quad 64-bit register). This allows data operation on either ϕ_1 or ϕ_3 shift. A simplified diagram of an internal 256-bit register is shown in Figure 7.

Data is written into the internal CCD register by the Write Data Amplifier which either injects or removes charge from the N+ regions as shown in Figure 7. The data will then be multiplexed through register 1 or register 2 (in each 128-bit half) depending on the state of ϕ_1 and ϕ_3. A read of the data is performed in a similar manner except the N+ region is either charged or discharged by the state of the CCD cell adjacent to the buffer. Data is read from either register 3 or register 4 depending on the state of ϕ_1 and ϕ_3. A sense amplifier, connected as shown, senses the state of the data after it passes through the refresh amplifier.

Data Refresh

As shown in Figure 7, each of sixty-four 256-bit shift registers is arranged as four 64-bit shift registers (as far as refresh is concerned) connected by an inverting refresh amplifier at each end to form a continuous data loop. Therefore, it requires 128 shift cycles (clock phases 1 through 4) to completely refresh the memory. The refresh amplifiers serve to restore the integrity of the data charge which is reduced through the dark current effect and shift transfer losses inherent in the CCD structure. The refresh amplifiers shown on the right side of the array in Figure 7 include an input/output gating function controlled by the address decoders and write enable lines. These refresh amplifiers serve as read/write amplifiers to the associated 256-bit channel.

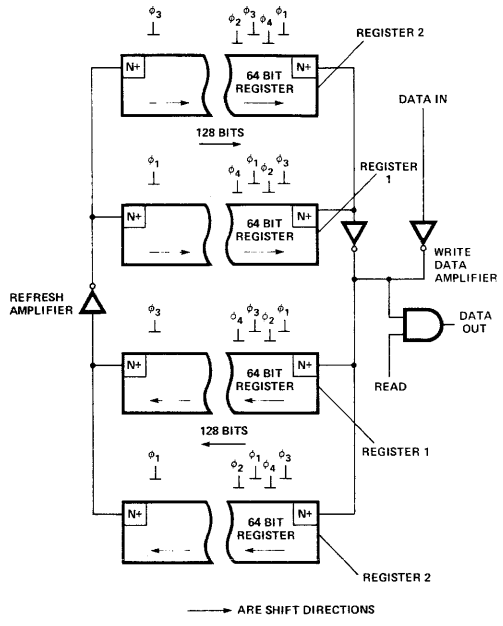


Figure 7. Simplified Diagram 2416 256-Bit Register.

2416 DEVICE SPECIFICATIONS

D.C. Characteristics

The D.C. and Operating characteristics of the 2416 are shown in Table I. Although the table is self explanatory, several items (marked as (3) in Table I) deserve special attention. First, note that the maximum average V_{DD} supply current (I_{DDAV}) is very low (25mA max.) at minimum cycle timing. This results in very low device power during operation at maximum data rate or shift rate. I_{DDAV} is inversely proportional to the cycle time of shift or data access cycles.

The input levels for the four-phase clocks (V_{ILC}, V_{IHC1}, V_{IHC2}) show the margin available for clock drivers and for the control inputs (addresses, read/write, chip enable, etc). Each of these limits will be discussed in detail in the Systems Considerations section along with driver designs which meet the 2416 input requirements.

Table I. 2416 D.C. and Operating Characteristics: T_A=0°C to 70°C, V_{DD}=+12V ±5%, V_{BB}[1] =-5V ±5%, V_{SS}=0V, unless otherwise specified.

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{LI}	Input Leakage		10	μA	V_{IN} = 0V
I_{LO}	Output Leakage Current		10	μA	CE=0V, V_{OUT} = 0V
I_{DD1}	Standby V_{DD} Supply Current		2	mA	CE=0V, ϕ_2= V_{DD}, ϕ_4 = 0V (or ϕ_2 = 0V, ϕ_4 = V_{DD}), ϕ_1 = ϕ_3 = 0V.
I_{DDAV}[3]	Average V_{DD} Supply Current [4]		25	mA	Minimum Cycle Timing
I_{BB}	Average V_{BB} Supply Current		200	μA	
V_{IL1}	Input Low Voltage, all Inputs except D_{IN} and $\phi_1 \ldots \phi_4$	-1.0	0.8	V	
V_{IH1}[3]	Input High Voltage, all Inputs except D_{IN} and $\phi_1 \ldots \phi_4$	V_{DD}-1	V_{DD}+1	V	
V_{ILC}[3]	$\phi_1 \ldots \phi_4$ Input Low Voltage	-2.0	0.6	V	Note 2
V_{IHC1}[3]	ϕ_1 and ϕ_3 Input High Voltage	V_{DD}-1.0	V_{DD}+2	V	
V_{IHC2}[3]	ϕ_2 and ϕ_4 Input High Voltage	V_{DD} -.6	V_{DD}+2	V	
V_{ILD}	D_{IN} Input Low Voltage	-1.0	0.8	V	
V_{IHD}	D_{IN} Input High Voltage	3.5	V_{DD}+1	V	
I_{OL}	Output Low Current	3		mA	V_{OL} = .45V
I_{OH}	Output High Current		10	μA	V_{OH} = +5V

NOTES:
1. The only requirement for the sequence of applying voltage to the device is that V_{DD} and V_{SS} should never be 0.3V more negative than V_{BB}.
2. The difference in the low level reference voltages between all four clock phases must not exceed 0.5 volts.
3. See Text.
4. Combined shift and Data I/O. For shift only mode I_{DD} = 2.0 +15/t_ϕ/2 (t_ϕ/2 is in μsec).

Data Cycles

The 2416 has two basic modes of operation: (1) data and (2) shift. In normal operation, the 2416 will use both of these modes. For clarity, however, the data mode will be treated separately from the shift mode. In the following sections, the discussion will describe writes, reads, and read-modify-writes to the 2416, *before or after a shift operation has been performed.* Figure 8 shows a detailed block diagram of the 2416 as it relates to data I/O cycles.

WRITE CYCLE

The write cycle of the 2416 is explained with the aid of the diagram of Figure 9 and term definitions shown in Table II.

As shown in Figure 9, write cycles may only be performed after a delay time (t_{TC}) from the trailing edge of ϕ_1 or ϕ_3 and continue until a time t_{CP} prior to the leading edges of ϕ_4 or ϕ_2. During the intervals between, ϕ_1 and ϕ_4 or ϕ_3 and ϕ_2, the data is not shifted and remains stationary in the 256 discrete locations of each of the 64 shift registers. Any of the 64 register input/output buffers can be accessed during this time through addresses A_0-A_5 and chip enable.

After the address lines are stable and chip select (CS) signal is high, a write cycle can start with the leading edge of the chip enable (CE) pulse. The CE and CS signals trigger an internal timing generator which generates internal enable and precharge signals to the address decoders and data-in buffers. The addresses are then decoded to activate one of the 64 decode lines which in turn enables the write amplifier for the selected channel. The write enable signal (WE) is then set to a high state after the data-in signal is stable (t_{DW}) and the CE to WE set up time (T_{cw}) has lapsed. The write enable signal enables the data-in buffer which in turn gates the input data to the selected write amplifier (WRT) via the data-in bus line. The selected write amp stores the data in the form of a charge "packet" at the input bit location of the selected buffer register (see CCD Internal Data Interface section). By selecting new address combinations and maintaining the chip enable off time requirement (t_{CC}), additional data bits can be stored in the other registers before a new shift execution cycle (t_ϕ/2) is required.

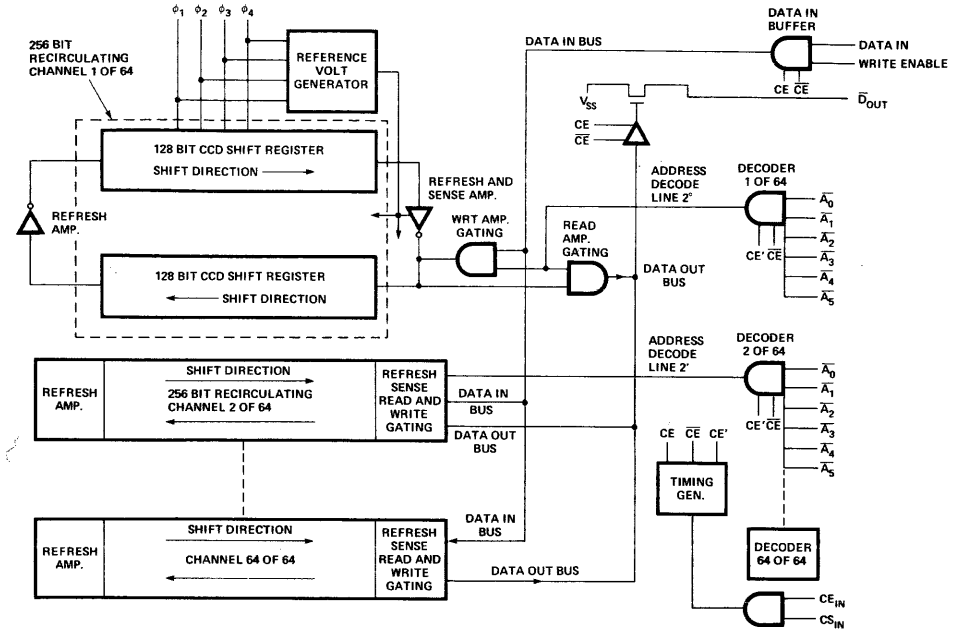
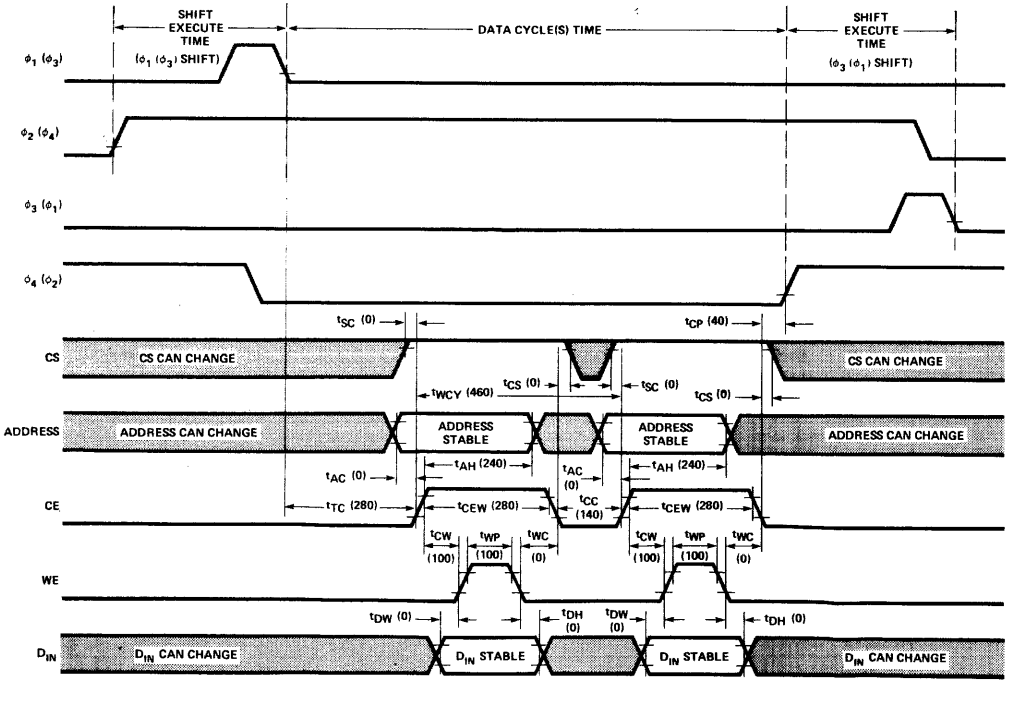


Figure 8. 2416 Internal Detailed Block Diagram.



(Numbers in parentheses are for minimum cycle timing in ns.)

Figure 9. 2416 Write Cycle Timing.

Table II. Definition of Terms.

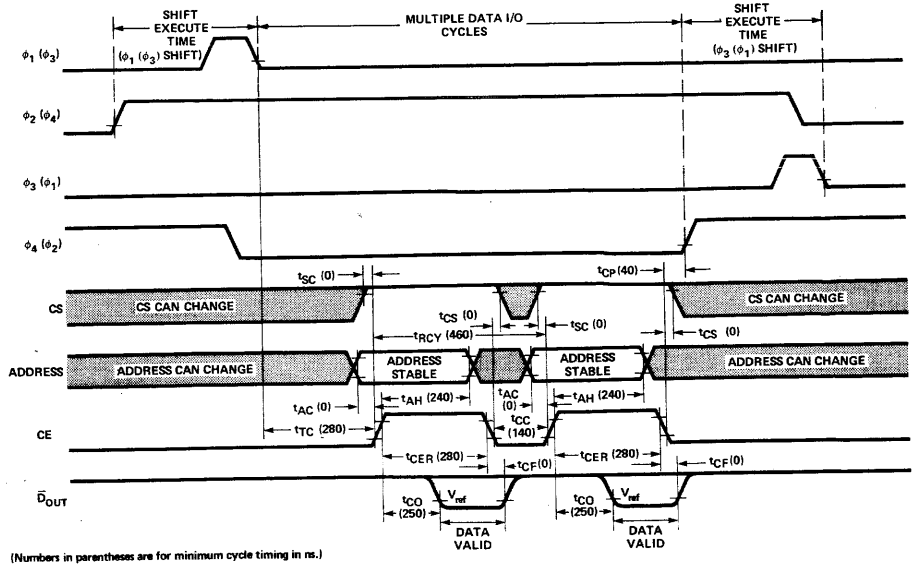
Symbol	Parameter
t_{WCY}	WRITE Cycle Time
t_{PT}	ϕ_2 On to ϕ_1 On Time, ϕ_4 On to ϕ_3 On Time
t_{TD}	ϕ_1 to ϕ_4 Overlap, ϕ_3 to ϕ_2 Overlap
t_{DT}	ϕ_4 to ϕ_1 Hold Time, ϕ_2 to ϕ_3 Hold Time
$t_{\phi/2}$	Half Clock Period for $\phi_1 \ldots \phi_4$
t_{T1}	Transition Times for $\phi_1 \ldots \phi_4$
t_{T2}	Transition Times for Inputs Other than $\phi_1 \ldots \phi_4$
t_{TC}	ϕ_1 or ϕ_3 Off to CE On
t_{SC}	CS to CE Setup Time
t_{AC}	Address to CE Setup Time
t_{AH}	Address Hold Time
t_{CS}	CE to CS Hold Time
t_{CC}	CE Off Time
t_{CP}	CE Off to ϕ_2 or ϕ_4 On
t_{CEW}	CE On Time
t_{CW}	CE to WE Setup Time
t_{DW}	D_{IN} to WE Set Up
t_{WP}	WE Pulse Width
t_{WC}	WE Off to CE Off
t_{DH}	D_{IN} Hold Time
t_{RCY}	READ Cycle Time
t_{CER}	CE On Time
t_{CF}	CE Off to Output High Impedance State
t_{CO}	CE to $\overline{D}_{OUT}$ Valid
t_{RWC}	READ–MODIFY–WRITE Cycle Time
t_{WD}	CE On to WE On
t_{WF}	WE to $\overline{D}_{OUT}$ Undefined

READ CYCLE

The read cycle timing (shown in Figure 10 and Table II) is identical to the write cycle for the CE, address and four-phase clock inputs. The only difference in operation between the read and write cycle is that the write enable (WE) signal must remain at a low state. In a read cycle the data-in line is electrically disconnected from the internal circuitry by a low level on the write enable input. Data is presented at the output pin at or before t_{CO} time.

The detailed block diagram shown in Figure 8 shows that a low level write enable signal inhibits the write amplifier gates. This allows valid register data to be present at the read amplifier inputs. The data from the read amplifier selected by the address decoder is gated to the data-out buffer via the data-out bus line. The data-out buffer amplifies the stored data voltage level and provides an open drain output signal from the memory device. The organization and CCD shift structure of the 2416 inherently contribute to a high internal signal-to-noise ratio at the data-out buffer as the result of the following:

1. Relatively small number of shift cycles (128) required between refresh. (This compensates for transfer losses and provides a high input signal level to the sense amplifier.)
2. The CCD shift structure minimizes the interconnection length from the data cell to the read amplifiers.



(Numbers in parentheses are for minimum cycle timing in ns.)

Figure 10. 2416 Read Cycle Timing.

Reducing the line lengths reduces the RC time constant effect on the signals to the read amplifier. This allows the signal to switch through the threshold point of the amplifier at a very fast rate, thus providing a very definite and easily sensed data-out signal.

READ-MODIFY-WRITE CYCLE

The read-modify-write cycle (RMW) shown in Figure 11 (see Table II for symbol explanation) combines both a read cycle and a write cycle, but requires less than the sum of the two cycle times to execute. The cycle time reduction is attributed to the condition that one, not two, CE off time intervals (T_{CC}) is required for a RMW cycle. Another advantage of the RMW cycle is that only one address hold time (t_{AH}) is required. Control of the RMW cycle is up to the user in that on an individual cycle a RMW cycle may be initiated by a separate command from the control logic (which extends the CE on time and delays the WE signal from the normal write time) or it can be performed on all data cycles.

SHIFT ONLY CYCLE

The previous section on Data Cycles outlined the timing requirements on the address, data, read-write and chip enable inputs necessary to perform a read or write operation. This section on shift-only cycles outlines the timing conditions on the four clock lines ϕ_1, ϕ_2, ϕ_3 and ϕ_4 required to simultaneously shift the 64-256 bit CCD registers.

The shift only mode performs two basic functions: (1) "Searches" for data or blocks of data in the CCD registers (see Systems Considerations section) and (2) Sequentially shifts data through refresh amplifiers (see 2416 Internal Organization and Operation) to perform data refresh.

The timing diagram for shift only mode operation of the 2416 is shown in Figure 12 with symbol definition shown in Table II. (Note that the timing diagram shown in Figure 12 is an extension of the description on charge transfer mechanism Figure 6.) As shown in Figure 12, *a complete clock* cycle (all four phases sequentially exercised) is given by:

$$t_{cyc} = 2\ t_{\phi}/2 = t_{\phi} \qquad (1)$$

(See Table II for definition of terms.)

Note that a complete clock cycle actually shifts data two locations.

A half clock cycle ($t_{\phi}/2$) shifts the CCD register one location. The half clock cycle is composed of two parts:

1. Shift execution time (t_{SX}). (See Figure 12.)
2. Clock "low" (t_{TP}). (See Table II.)

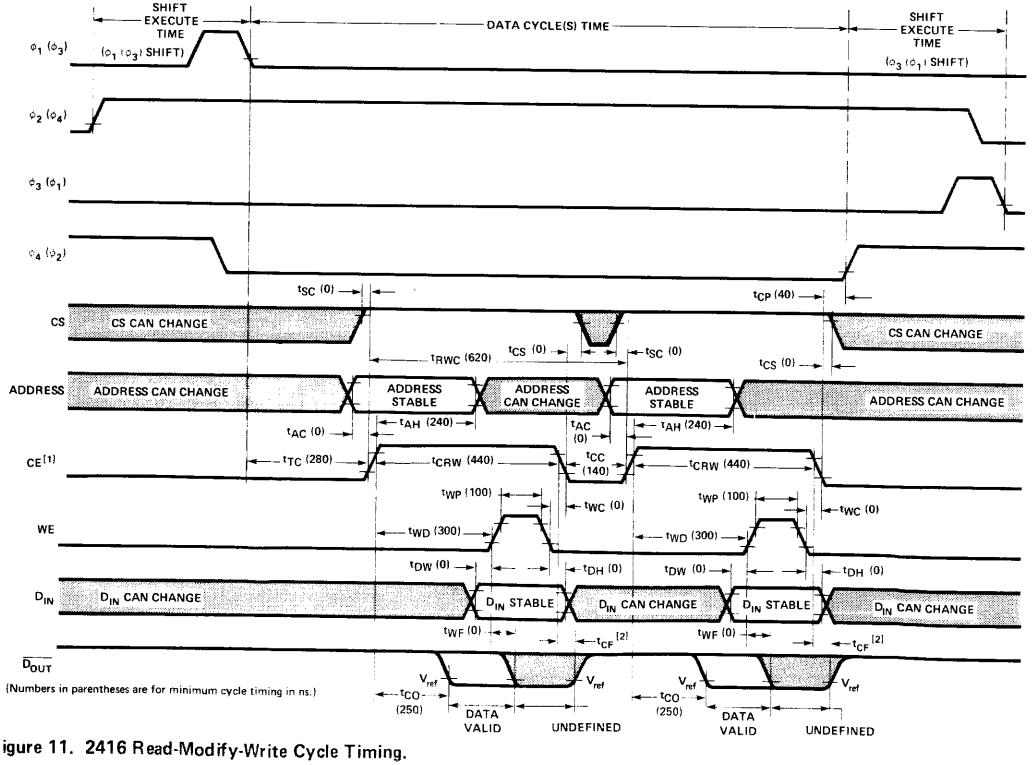


Figure 11. 2416 Read-Modify-Write Cycle Timing.

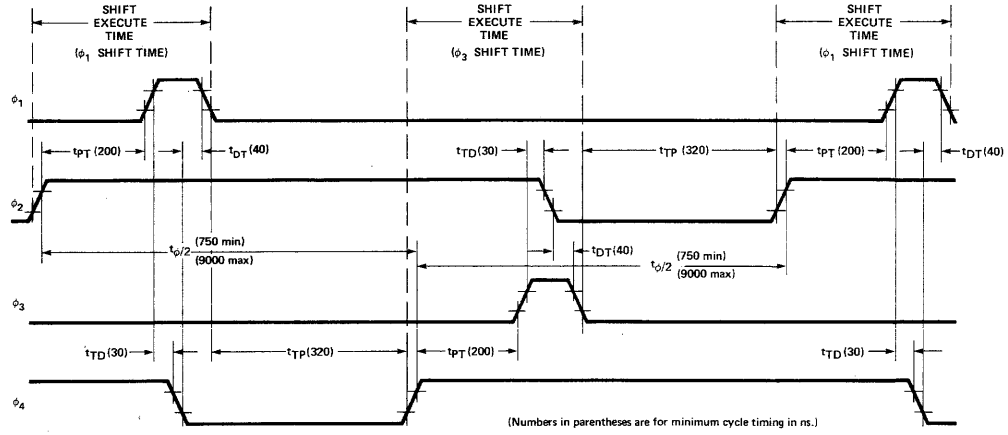


Figure 12. Shift Only Cycle Timing.

Note that the two shift execution times shown in Figure 12 *can be* identical but are relative to different portions of the four-phase clocks. For example, the first shift execution time is timing associated with ϕ_1, ϕ_2, ϕ_4 while the second shift execution time is associated with ϕ_3, ϕ_4 and ϕ_2.

The time required to shift data (shift execution time t_{SX}) is given by:

$$t_{SX} = t_{PT} + t_{TD} + t_{DT} + 4t_T \quad (2)$$

(See Table II and Figure 12 for definition of terms.)

The shift period, t_{SP}, is given by:

$$t_{SP} = t_{SX} + t_{TP} = t_{\phi}/2 \quad (3)$$

Where:

t_{SX} = shift execution time (equation 2).

t_{TP} = clock off to on time (Table II).

(Note that the term t_{SP} has been substituted for $t_{\phi}/2$ in equation 3. The reasons for this will be evident in the Systems Considerations section.) The minimum search cycle time is obtained by operating the four-phase clocks at the maximum repetition rate (for this case t_{SP} is 750 nsec). The maximum half cycle time between clocks (for a single shift cycle) is 9000 nsec. The maximum cycle time is most often used for refresh and for obtaining maximum data rates.

SHIFT/MULTIPLE DATA/SHIFT CYCLE

The previous sections discussed the data and shift cycles of the 2416 as separate functions. *This section discusses the combined operation of the shift and data cycles.* Data cycles may be initiated after a minimum of t_{TC} nsec from the completion of a shift execution (end of ϕ_1, see Figure 10). After a shift, the 64 internal data buffers may be accessed in any order by addresses A_0-A_5. The number of data cycles, N, which may be performed between shift execution times is dependent on two criteria:

1. System addressing technique.
2. Refresh rate.

The number of data cycles which can be performed between shift periods is simply the time available between shift cycles divided by the data cycle time. A simple expression for the number of data cycles allowable between shift cycles is determined by inspection from Figures 9, 10, or 11 and is expressed as:

$$N = \frac{t_{SP} - t_{SX} - t_{TC} + (t_{CC} - t_{CP})}{t_{DC}} \quad (4)$$

Where:

N — number of cycles between shifts

t_{SX} — shift execution time (see equation 2 or Figures 9, 10, or 11)

t_{TC}, t_{CC}, t_{CP} — (see Table II or Figures 9, 10, or 11)

t_{DC} — data cycle time (e.g. $t_{DC} = t_{RCY}$ for a read cycle).

For those systems where the time relationship of the last data cycle relative to a shift cycle cannot be predicted, the term $(t_{CC} - t_{CP})$ in equation (4) equals zero. (For this case, the maximum number of cycles is decreased slightly.) A practical maximum (due to system address considerations) of data cycles between shift periods is sixteen for a shift period of 9000 nsec.

DATA RATE

Consider now the data rate for the following conditions:

A. Maximum number of cycles between shifts.

B. One data cycle per shift.

1. The maximum data rate of 2 megabits/sec is obtained when the time between clock cycles is maximized and the maximum number of data cycles possible are inserted between these shift executions. As shown in Figure 10, this rate is actually a maximum *average* data rate because of the shift execution intervals. (Recall that during shift execution, no data cycles are permitted. Therefore, the maximum data rate is the average of the data rate during data cycles and a data rate of zero during shift cycles.)

   Clearly the maximum data rate is proportional to the shift period and approaches $1/t_{DC}$ as the shift period t_{SP} is increased. Also, as the shift period is increased the clock frequency is decreased resulting in lower clock driver power and higher data rates. (The significance of this will be evident in the four-phase driver section.)

2. The data rate is the same as the shift execution rate when there is only one data cycle (N) between shift cycles (see Figure 13). In this special case, clock driver power will increase as the data rate increases. (Remember that minimum driver power and maximum data rate occur when a maximum number of data cycles are performed between shift periods, t_{SP}.)

SYSTEM CONSIDERATIONS

Typical Applications

The combined high density and high speed characteristics of the 2416 make this part ideal for use in many types of systems. Of particular interest to many designers are four general system categories where the 2416 is especially ideal from a cost/performance viewpoint.

These categories are:

1. Drum replacement.
2. Small "rotating" memory applications.
3. Hi-reliability (ruggedized) "rotating" memory.
4. Conventional shift register replacement.

It is useful to briefly review each of the above categories to illustrate the versatility of the 2416.

DRUM REPLACEMENT

The 2416 has several significant system advantages over conventional mechanical drum assemblies. For example, the 2416 is an order of magnitude faster than a high speed drum (average latency time of a 2416 system is 100μsec); the 2416 system is more reliable since there are no mechanical assemblies rotating at high speed; and the 2416 drum type system is cost competitive and more compact than standard drum type systems. In addition, the extremely high data rate of a 2416 system can handle virtually any computer data rate requirement.

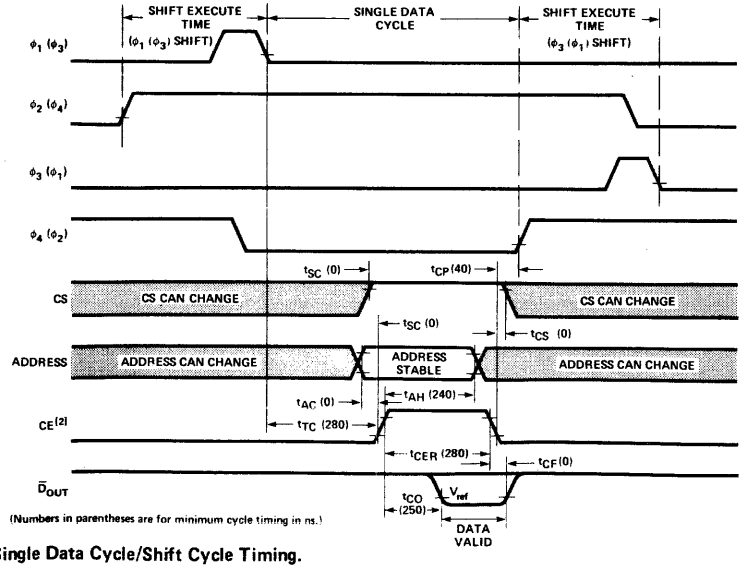


Figure 13. Shift/Single Data Cycle/Shift Cycle Timing.

SMALL "ROTATING" MEMORY APPLICATIONS

The 2416 is very competitive in applications previously favoring various types of rotating memory. The real strength of this CCD device is readily apparent in those types of applications requiring a relatively small amount of rotating memory. In these rotating systems the overhead cost of drive motors, sense heads and other peripherals significantly impact the overall cost per bit at the system level. For these systems the 2416 offers a significant cost advantage over conventional rotating memory devices. As in the case of drum replacement type memories, the 2416 is significantly faster than the small rotating memories it is designed to replace.

HI-RELIABILITY (RUGGEDIZED) "ROTATING" MEMORY

Many applications for mass storage requiring a "ruggedized" rotating memory need significant attention paid to the mechanical mechanisms to assure reliable operation in a hostile mechanical environment. A clear advantage of the 2416 is its lack of any mechanical rotating mechanism which needs to be ruggedized. This CCD device offers high density and speed for most Hi-reliability applications requiring a mechanically rugged support.

SHIFT REGISTER REPLACEMENT

The 2416 can easily be used (as is shown later in this section) as one very long shift register (16,384 stages) or as 64 256-bit shift registers. In either case the density advantage of this CCD device over conventional shift registers is readily apparent. These types of shift register applications include CRT display refresh and communications buffers. In these applications the advantages of speed and density are particularly evident.

The previous sections detailed specific timing requirements and associated data rates of the 2416. In this section, examples of timing, control, and driver interface implementation for a memory system are discussed.

Addressing Considerations and Control

In the previous sections describing the internal organization and operation of the 2416, it was pointed out that this CCD device has both a "sector" type address controlled by the four phase clocks and a "track" type address defined by addresses A_0-A_5. The location of specific "track" addresses is very straight forward with track zero defined by A_0 through A_5 equaling logic zero and track 63 defined by A_0 through A_5 equaling logic one, etc. However, the starting and ending "sector" addresses are not uniquely defined in the same manner as the "track" addresses. Throughout this section on Addressing Considerations it should be remembered that control circuitry for the four-phase clocks must contain logic capable of "recalling" where the previously defined starting location of the sector addresses is positioned and determining how many shifts to perform to reach a desired sector. It is shown later in this section just how simple such interface requirements are. In the following discussion, two basic types of control circuitry will be analyzed:

1. Serial memory applications (shift/single data cycle/shift).
2. "Random" memory applications (shift/multiple data/shift).

(The "random" memory application is actually an extension of the serial mode to include search type operations.)

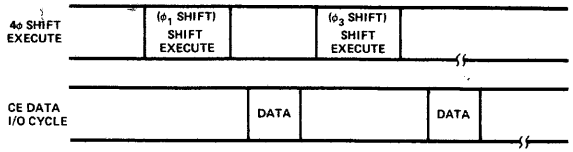
SHIFT/SINGLE DATA CYCLE/SHIFT CONTROL

A simple shift/single data cycle/shift control circuit which has one data cycle per shift is shown in Figure 14(a) and (b). Basic timing of the control circuit is shown in Figure 14(a). The four-phase clocks (performing the shift) are shown in block form (labeled as shift execution time) with the corresponding data cycle shown below.

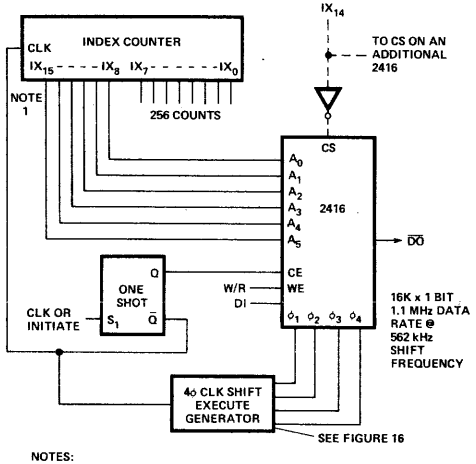
Operation is most easily understood with the aid of the diagram shown in Figure 14(c). This figure illustrates the addressing and shifting sequence applied to a 2416 operating in a shift/single data cycle/shift mode as a 16K bit shift register. First a particular CCD register (1 of 64) is accessed by addresses A_0-A_5 and a read or write cycle performed. Then a shift is executed and the next CCD cell accessed (data is moving from IA_0 to IA_1 as shown in Figure 14(c) (refer to Figure 4 for explanation of data sequencing addressing). This sequence is repeated 255 times to access all of the cells in one of the 64 256-bit CCD registers. (Note that during this entire operation addresses A_0-A_5 have not changed.) After the entire 256-bit register has been accessed, the 2416 addresses are incremented (A+1) and the next internal register is sequenced in the same manner. The entire operation is summarized as follows:

1. Access memory.
2. Shift (four-phase clocks) once.
3. Repeat 1 and 2 255 times then:
4. Increment 2416 addresses by 1 (A_0-A_5).
5. Repeat 1 through 4 sixty-four times.

As shown in Figure 14(b), a data cycle is begun with an initial pulse triggering a single-shot S_1. The leading edge of the single-shot output (Q) initiates a read or write to the 2416 at the address defined by A_0-A_5. When the single-shot times out, the trailing edge ($\overline{Q}$) triggers a four-phase clock generator and increments the index counter controlling addresses A_0-A_5 as shown. (Details of the four-phase clock generator are shown in Figure 16.)

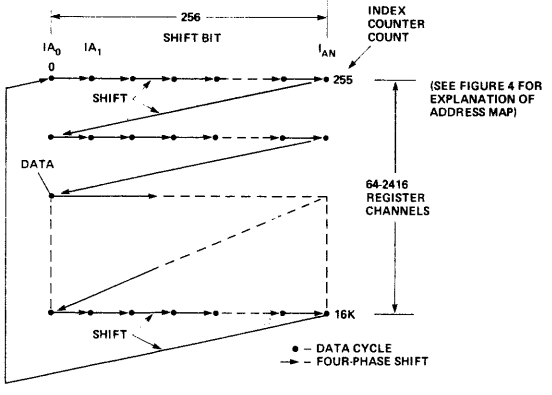


(a) Timing



NOTES:
1. NUMBER BITS PER WORD EXPANSION IS ACCOMPLISHED WITH ALL LINES PARALLEL EXCEPT THE DI AND DO LINES.
2. WORD DEPTH EXPANSION ACCOMPLISHED WITH ALL LINES PARALLEL EXCEPT FOR DECODED CE AND/OR CS LINES.

(b) Control Block Diagram



(c) Address Sequence

Figure 14. Control and Address Sequence Shift/Single Data Cycle/Shift.

Address Expansion

The control circuit shown in Figure 15(b) is easily expanded in the bit direction (e.g., 16K x 8) by adding more 2416s and paralleling the addresses (A_0-A_5), four-phase clock, and control input (R/W, CE, CS) lines. Further expansion to 32K words is most easily done by using the next high order bit of the index counter and generating a select and $\overline{\text{select}}$ signal which go to respective CS inputs. Figure 15 shows a 64K x 1-bit configuration. (Other lines are paralleled as described.)

SHIFT/MULTIPLE DATA/SHIFT CONTROL

An expansion of the shift/single data cycle/shift mode is the shift/multiple data/shift mode. It is this mode that is most often used in general system applications because of its ability to handle a wide variety of applications. This mode also includes the "search" mode requirement.

A shift/multiple data/shift control interface is given in Figure 17. (The addressing sequence is given in Figure 18.) Note that in this implementation *16* data cycles are performed between shift cycles. The relationship of data cycles to shift cycles is shown in Figure 17(b).

Implementing control for the multiple data mode differs from the implementation used for the single cycle data mode (Figure 14) by simply changing the 2416 address and shift initiate address connections to the index counter as shown. The multiple data mode control requires that, during a shift operation, the data cycle request line must be inhibited. (A method to "hide" the four-phase shift clocks so that the data cycles are not interrupted will be dis-

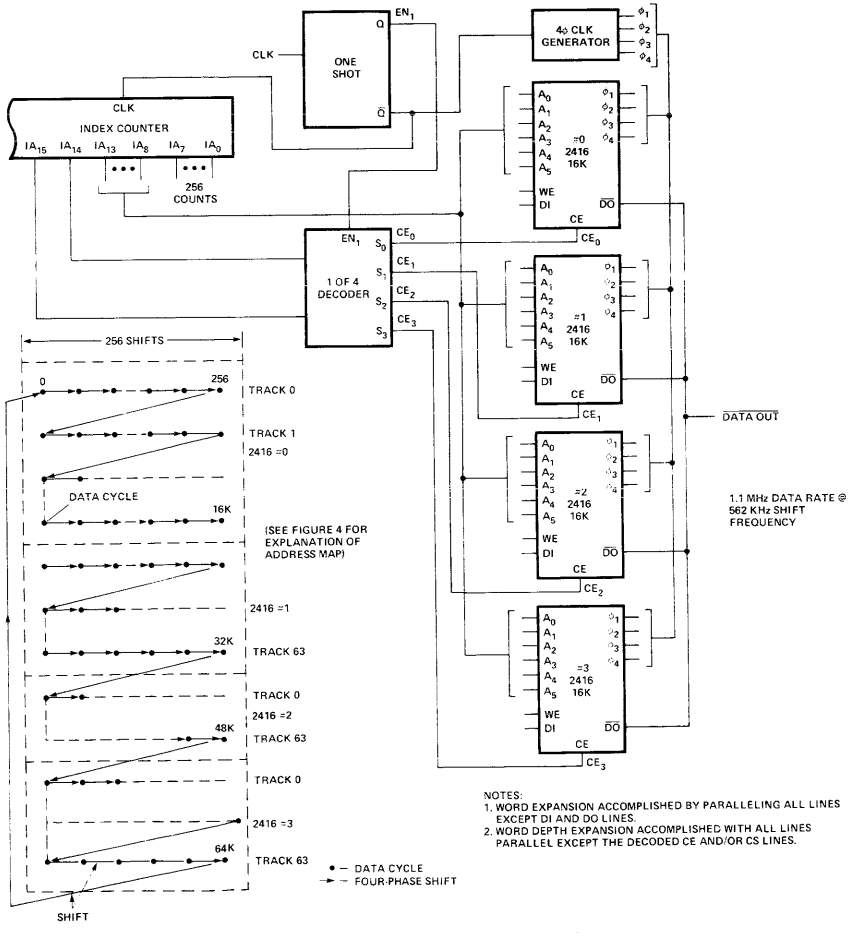


Figure 15. Shift/Single Data Cycle/Shift Address Expansion.

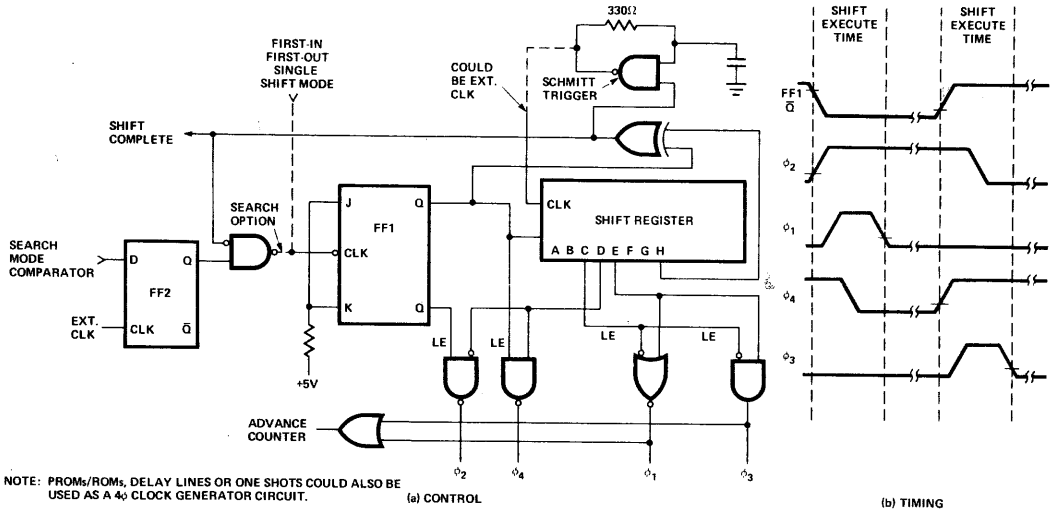


Figure 16. Four-Phase Clock Generator Circuit.

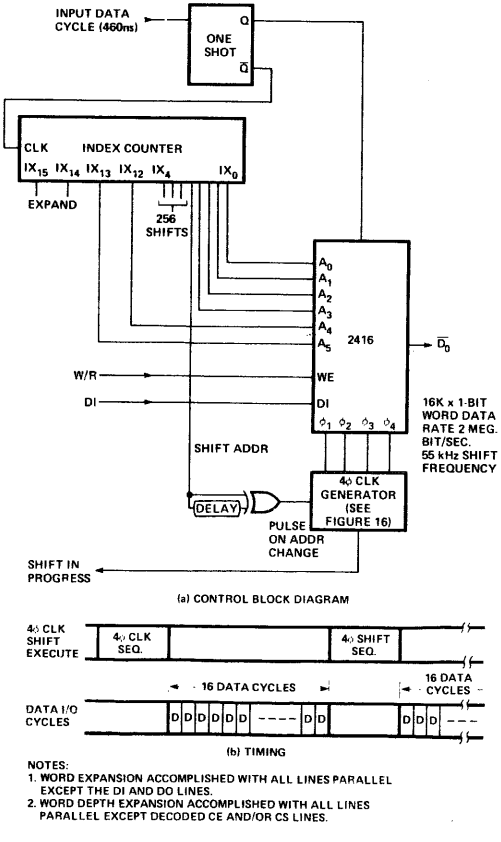


Figure 17. Shift/Multiple Data Cycle/Shift Control.

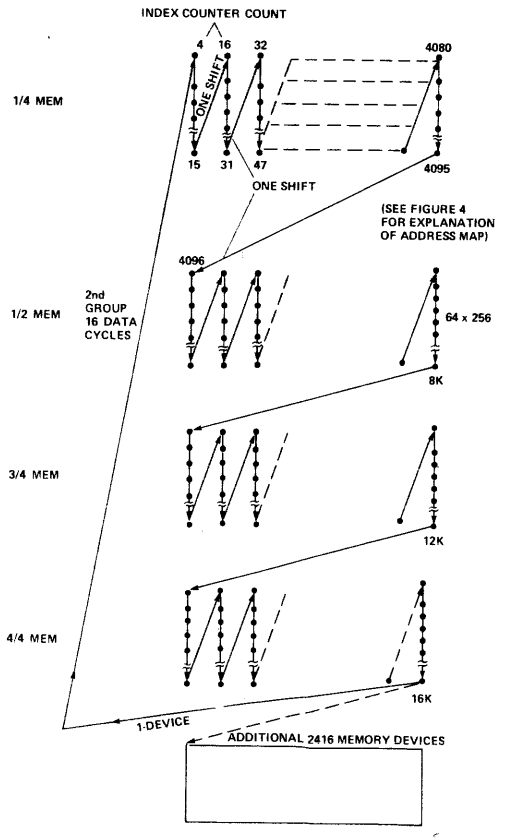


Figure 18. Shift/Multiple Data Cycle/Shift Address Sequence.

cussed later.) The data cycle inhibit time gap is shown in Figure 17(b) by the absences of data cycles during the shift cycles. Relating the control schematic (Figure 17b) to the data address sequence chart (Figure 18) shows that 16 (out of 64) of the internal 2416 registers are selected before a shift cycle is initiated by index address 4 (IX_4). The selection of this first group of internal registers is repeated 255 times before a new group of 16 is selected by the change in index counter address 12 (IX_{12}). This sequence is repeated three more times, before the index counter either selects a new 2416 or returns to the original address location.

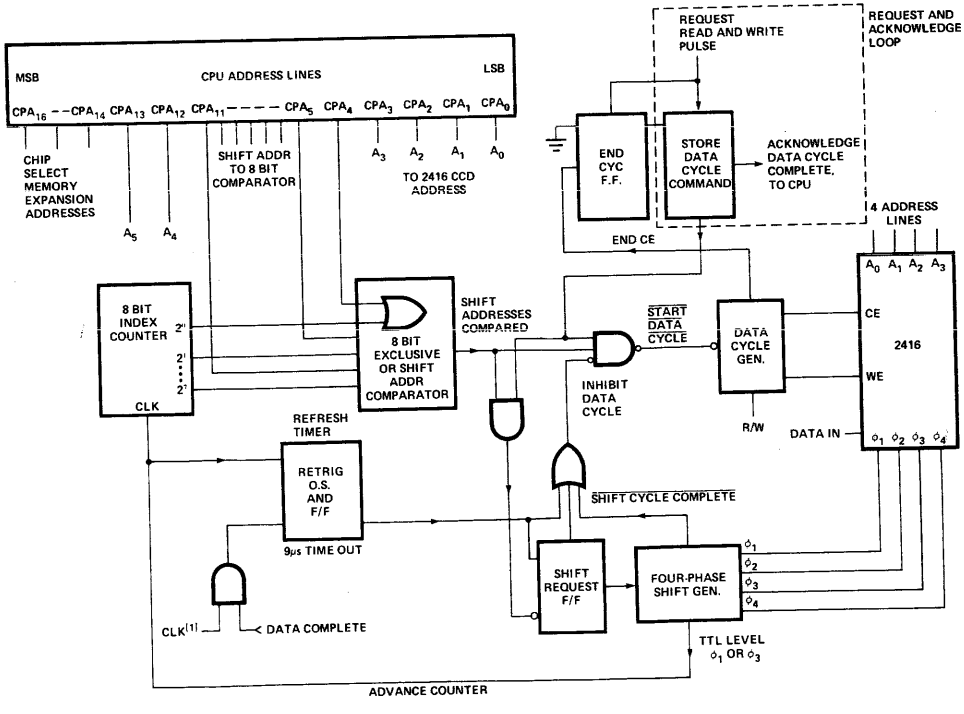
COMBINED SEARCH AND DATA CYCLE CONTROL

The control circuitry described in Figure 14 and 17 applied primarily to sequential applications which do not require a "search" to find a block of data. A more general control circuit is one that is capable of performing a "search" (or shift at high speeds to locate a block of data) and then accessing data at the maximum data transfer rate and the minimum shift cycle time.

Figure 19 is a block diagram of the control for operation of the 2416 in a random access or search cycle mode. The previously discussed principles of the sequential control modes are applied with the addition of a shift address comparator circuit and a request and acknowledge loop (which provides data synchronization). The search cycle mode occurs when one or more of the 8 shift address lines do not compare to the corresponding 8-bit index counter lines. (This means that the starting address location of a block of data is not in the data out buffer.) A "not compared" condition inhibits a data start cycle signal and enables the four-phase shift generator. The four-phase shift generator shifts the 2416 at the maximum four-phase clock shift rate and increments the 8-bit index counter until a "compare" is obtained. The compare enables a data start cycle which allows data access to the 2416 in the same manner as described in the sequential mode of Figure 17.

"HIDDEN" SHIFT CYCLE CONTROL

Time gaps in input/output data transfers in the previously described control circuit are the result



NOTES:
1. CLK MUST LEAD READ WRITE PULSE ≥30ns.
2. SHIFT ADDRESS SET UP TIME > COMPARATOR DELAY.

Figure 19. Block Diagram Control Random Access Mode.

of a shift cycle taking place. (Remember that no data I/O operations may be performed during a shift cycle.) In most systems applications, this time gap in the data I/O rate can be ignored or an external one word data buffer added to "hide" the gap. However, for those systems in which neither of the above alternatives is acceptable, the time gap can be hidden by the system controller shown in Figure 20. (The particular example is for a serial access design but can be extended to the search/multiple data mode described previously.)

The circuit in Figure 20 emphasizes the concept of obtaining high data rates with minimum four-phase clock shift rates and expands this concept by interleaving the shift times between two 2416 devices. As shown in the timing diagram included in Figure 20, interleaving the shift times and multiplexing the data out signals from both 2416 devices to a common data out line "hides" the shift time of the device being shifted from the *system* input/output data stream. Note that only one 2416 at a time is being shifted.

Operation of the 2416 in the system shown in Figure 20 is described as follows (see Figure 21). The first input data cycle inhibits the refresh oscillator and generates a chip enable signal from the I/O data cycle generator. The chip enable signal is steered to either device A or B by the state of the 2^3 bit on the index counter. (Read or write is determined by the state of the R/W.) The end of chip enable increments the index counter which establishes a new data location by changing the 2416 address lines. As the index counter is incremented it will select one shift location in one CCD and sequentially access 8 of the 64 CCD internal shift registers. At the end of the 8th cycle, the 2^3 index bit initiates a shift in the device being accessed and enables the data I/O in the other device. In summary, when one device is being shifted the other device is being accessed. Note that the same 8 registers (defined by addresses A_0-A_5) will alternately be selected between devices until 256 shift cycles have occurred, (i.e., the 2^{12} index counter bit changes state). After every 256 shift cycles a new group of 8 internal CCD registers per device (defined by addresses A_0-

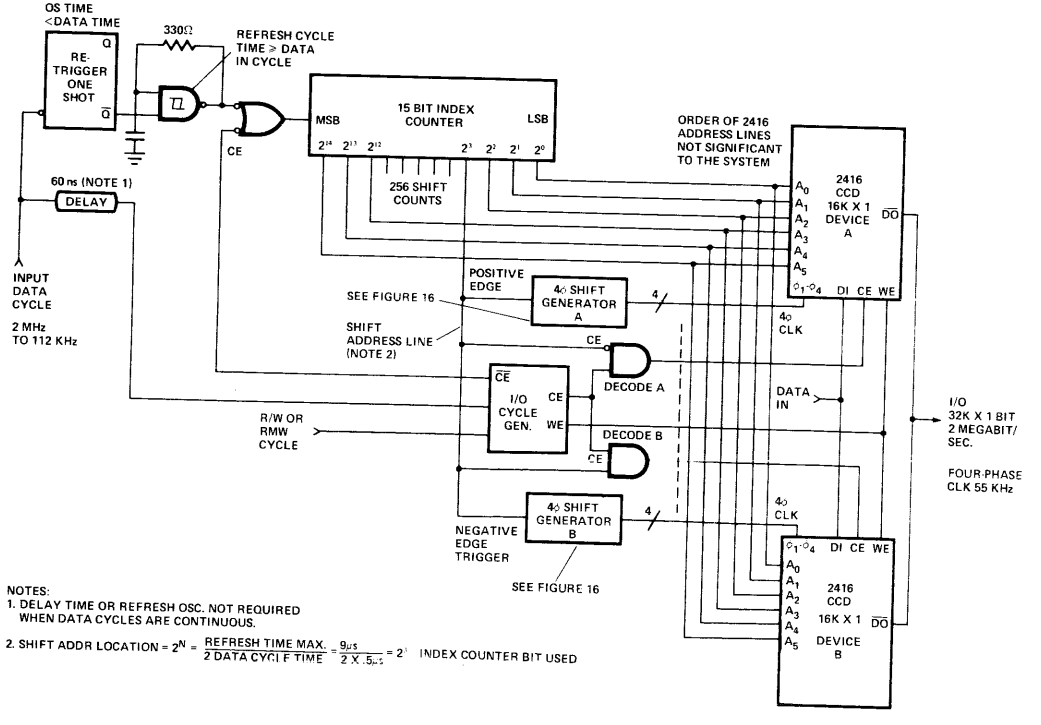
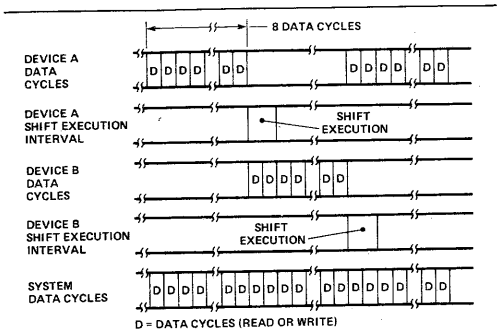
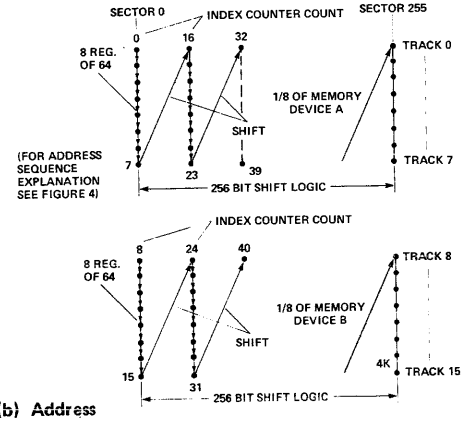


Figure 20. Hidden Shift Cycle Control.



(a) Data



(b) Address

Figure 21. Hidden Shift Cycles Data and Address Sequence.

A_5) will be alternately selected between the two devices for 256 shift locations. This cycle continues until 8 groups of 8 registers (i.e., all 64 CCD internal data registers) are selected. The system described in Figure 19 can be expanded to 128K x 1 as shown in Figure 22.

Driving Considerations

This section discusses the 2416 input signal characteristics, driver requirements and data-out sensing considerations. All 2416 input lines operate from a nominal 12 volt logic swing driving signals. However, there are basic differences in input capacitance and voltage margins between some input signals. We will first consider the driver requirements for the four-phase clock inputs.

FOUR-PHASE CLOCK INPUTS

The four-phase clock inputs are connected internally to thin oxide gates (which overlap other clock lines) and as a result have relatively long lines (Figure 5). These clock lines cover the 64 shift register channels. The long lines and the close proximity of the gates to the substrate result in a high capacitance to substrate on the four-phase clock inputs. In addition, the overlapping on the gate electrode (to adjacent clock lines) produces added coupling capacitance between adjacent four-phase clock inputs.

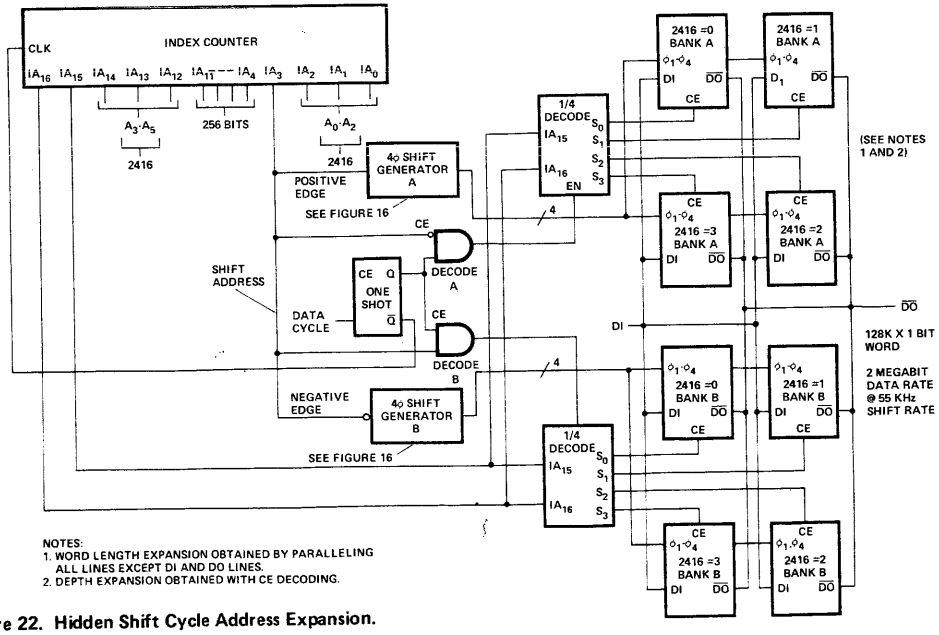
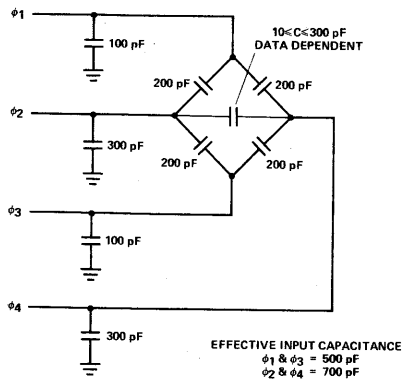


Figure 22. Hidden Shift Cycle Address Expansion.

2416 CLOCK CAPACITANCE



(a) Equivalent Circuit

		Max. pF
$C_{\phi1}$[1],$C_{\phi3}$[1]	ϕ_1,ϕ_3 Input Capacitance	500
$C_{\phi2}$[1],$C_{\phi4}$[1]	ϕ_2,ϕ_4 Input Capacitance	700
$C_{\phi1\text{-}\phi2}$	Clock ϕ_1 To Clock ϕ_2 Capacitance	200
$C_{\phi1\text{-}\phi4}$	Clock ϕ_1 To Clock ϕ_4 Capacitance	200
$C_{\phi3\text{-}\phi2}$	Clock ϕ_3 To Clock ϕ_2 Capacitance	200
$C_{\phi3\text{-}\phi4}$	Clock ϕ_3 To Clock ϕ_4 Capacitance	200

Note 1: The $C_{\phi1}$. . . . $C_{\phi4}$ input clock capacitance includes the clock to clock capacitance.

(b) Capacitance Values

Figure 23. Four-Phase Clock Input Equivalent Circuit.

Figure 23 shows the four-phase clock input equivalent circuit with the maximum capacitance values.

The equivalent circuit of Figure 23 suggests two clock driver requirements which must be considered in most clock driver designs for a particular system. These two requirements are:

1. Ability to drive high capacitance loads.
2. Ability to suppress cross-coupling current transients.

Of the two design requirements, number two is the most difficult to control. The cross-coupled current affects the ability of an adjacent clock driver to maintain the required high or low voltage margins while the adjacent phase driver is switching. The cross-coupled current that the quiescent driver must sink is proportional to the coupling capacitance and the slope of the active driver transitions (expressed as nsec per volt). The cross-coupled current is expressed by the equation for a linear charge of a capacitor:

$$I = C\frac{dv}{dt} \qquad (5)$$

Where:

I is the current for the duration of the signal transition.

C is the cross-coupling capacitance.

$\frac{dv}{dt}$ is the slope of the voltage transition across the capacitor.

The coupling capacitor between clock phases two and four shown in Figure 23(a) has a capacitance value that is a function of the data stored in the 2416. Its minimum value occurs when all data results in no charge stored in the potential wells under the phase 2 and phase 4 devices. Its maximum value occurs when the data under phase 2 and phase 4 devices has stored charge in the potential wells. (Remember that the refresh and buffer amplifiers in the 2416 are inverting, see Figure 7, so that all potential wells contain stored charge *only if* the original input data is a low level for 128 shifts and then a high level for 128 shifts. Complete absence of charge is the opposite logic condition.) This capacitance generally has a negligible effect on the overall design of the clock driver and is included only for completeness of the discussion on drivers.

Examining the clock input equivalent circuit and the above equation indicates a contradictory driver output impedance requirement. For the quiescent driver to hold the coupling voltage to a minimum requires that the driver have a very low output impedance. However, when that driver becomes active this low output impedance increases the slope of the transitions which in turn increases coupling currents to the other drivers. The above conditions suggest that a driver have a controlled output transition time and a low output impedance characteristic in the quiescent state (high or low level). Doubling the clock transition time (t_T) results in halving the cross-coupled currents (a very desirable effect). The clock transitions ($4t_T$) in the shift execution time expression, t_{SX}, (equation 2) have a minimal effect on data rate. Therefore, a large change in clock transition time will not appreciably effect the shift cycle, data rates, and latency time of the 2416. The effect of doubling the clock transition time decreases the maximum data I/O rate by less than 1% and increases the latency time by less than 20%.

FOUR-PHASE VOLTAGE MARGINS

The clock voltage margins and optimum "low" levels are also driver considerations. All four-phase clock low levels, V_{ILC}, are specified at V_{SS} +0.6/-2.0V for the 2416, including cross-coupling and over shoot transients. Another clock margin requirement is that the difference in the low level average reference

voltage between all four-phase clocks must not exceed 0.5 volts. This means that all four-phase clock drivers should use the same DC power supply voltages. (Although MOS drivers usually take power from the same power supplies, it is emphasized here because of the 0.5 volt restriction.)

The high level margin (V_{IHC1}) for the transfer gates, ϕ_1 and ϕ_3 is V_{DD} ±2.0V, and the high level margin (V_{IHC2}) for the storage gates ϕ_2 to ϕ_4, is V_{DD} +2.0/-0.6V.

The power dissipated by a clock driver when driving a capacitive load is given by:

$$P = P_{dc} + P_{ac}, \quad (6)$$

where:

P_{dc} — is the average dc power dissipated by the driver when in quiescent state (high or low).

P_{ac} — is the power associated with driving capacitive loads.

and:

$$P_{ac} = CV^2f \quad (7)$$

where:

C is load capacitance

f is clock frequency.

V is clock voltage swing.

The term P_{dc} can be considered a constant for a given clock driver design (to a first order approximation) and attention focused on P_{ac}. As shown in the equation for P_{ac} for a given capacitive load and drive voltage, the transient power is a function solely of the clock frequency. Therefore, to minimize driver power, the clock frequency must be minimized. As a result, maximum input/output data rates are achieved with minimum clock driver power. (Remember that the maximum data rate is obtained at minimum clock frequency.)

CLOCK DRIVER POWER VS. 2416 OPERATING MODE

A.C. clock driver power is calculated for several 2416 operating modes. In these calculations the d.c. component of the driver power is neglected as a first order approximation.

The four basic operating modes of the 2416 which effect the clock shift frequency and hence the clock driver power are:

1. Continuous search (maximum shift rate).
2. Refresh mode (minimum shift rate).
3. Shift/multiple data/shift mode.
4. Search data block transfer mode (combination of maximum and minimum shift rates).

Continuous Search Driver Power

This mode results in the maximum driver power dissipation with minimum (zero) input/output data rate. The clock driver power for the continuous search mode is expressed by the following equation:

$$P_S = C_T V^2 f_s \quad (8)$$

Where:

P_S — driver power in search mode.
C_T — total driver load capacitance.
f_s — clock frequency in search mode = $\frac{1}{t_{CYC}}$ (equation 1).

V — clock voltage swing.

For maximum loading conditions and search frequencies, equation (8) is solved as follows:

$$P_S = 2400\,(10^{-12})(12)^2\,\frac{1}{(2)(750)(10^{-9})} \quad (9)$$

or

P_S = .23 watts dissipated in clock driver per 2416 device. (10)

The search-after-every-data-cycle mode of operation (similar to the search only mode) results in a driver power dissipation of approximately that derived in equation 10 for maximum shift rates.

Refresh Cycle Driver Power

Derivation of the driver power for system operating in the refresh only mode is similar to the power derived for a continuous search mode. The power is calculated as follows:

$$P_{REF} = 2400\,(10^{-12})(12)^2\,\frac{1}{2(9000)(10^{-9})} \quad (11)$$

or

P_{REF} = .019 watts per 2416 device. (12)

Equations 11 and 12 clearly show that clock driver power is a reciprocal of the clock cycle time. Remember, to minimize clock driver power and simultaneously maximize data input/output rate, the four-phase clock cycle time should be maximized.

Shift/Multiple Data/Shift Driver Power

The continuous shift / multiple data / shift mode driver power depends on how many multiple data cycles occur between shift intervals. In this mode, the driver power can range from approximately 73% of the continuous search power (when only one data cycle between a shift interval is implemented) to as low as the refresh power (when 16 data cycles are implemented between shift intervals).

SERIAL

The calculation of four-phase driver power for a general system operating in a shift/multiple data/shift mode is a combination of the Search cycle and Refresh cycle power previously calculated. Since the actual power dissipated is a function of a particular system, the user is left to make the calculation for his particular system.

Search/Data Block Transfer Driver Power

The clock driver power in the search/data block transfer mode is the time averaged power between the high driver power during a search mode and the low power of the shift/multiple data/shift mode during a data block I/O transfer. The following example will better illustrate the power and time magnitudes involved in this mode of operation.

In this example, the data block length is assumed to be 4K data cycles and the maximum search latency time is assumed to be 200 μsec. The maximum 2416 shift/multiple data/shift rate is 2 megabits/sec. The average driver power including the search latency time and total data I/O time is expressed by the following equation:

$$P_{SDB}=P_{REF}\ \frac{(D_{bt})}{D_{bt}+L_{at}}\ +P_S\ \frac{(L_{at})}{D_{bt}+L_{at}} \qquad (13)$$

Where:

P_{SDB} – the driver power in a search/data block transfer mode.

P_S – is the search mode driver power.

P_{REF} – is the previously determined refresh power.

D_{bt} – the time required to transfer a block of data, and is expressed by:

D_{bt} = number of Data Cycles/Data Block
or Average Data Rate

$$D_{bt}=\frac{4K}{2meg.\ bit}=2ms$$

L_{at} – maximum latency time (255 x tϕ/2 – see equation 1).

$$P_{SDB}=.019w\ (\frac{2ms}{2.2ms})+.23w\ (\frac{2ms}{2.2ms})=.038w/2416\ device. \qquad (14)$$

The above example indicates that even at the highest search rates, a search/data block retrieval time ratio as low as 1 to 10 results in very low clock driver power dissipation.

Table III gives a summary comparison between the driver power requirements, data rates and mode of operation as calculated in the previous sections.

DRIVING THE 2416

The 4ϕ clock driving requirements of the 2416 determine the type of drivers that must be used. This driver must have the ability to drive a large capacitance as well as be able to maintain voltage levels during other clock transitions. (The four phase clock equivalent circuit is shown in Figure 23.) Two basic types of drivers which can be used to drive the clock inputs are those made with discrete components and integrated drivers. The complexity of discrete drivers virtually eliminate them from consideration. The problem now reduces to the selection of a suitable integrated circuit driver.

There are many integrated circuit drivers capable of driving a high capacitive load. However, the additional requirement of being able to suppress clock coupling transients make these drivers unsatisfactory for use in large 2416 systems. A driver designed especially for CCD devices is the Intel® 5244. The 5244 is a quad CCD clock driver capable of driving high capacitance loads *and* suppressing clock coupling transients.

THE 5244 QUAD CCD CLOCK DRIVER

The 5244 is a CMOS driver capable of driving four 2416's. This driver requires a single +12V supply and has fully TTL compatible inputs. The 5244 is designed specifically to drive CCD devices and as

Table III. Four-Phase Clock Driver Power Summary.

Mode of Operation	Symbol	Data Rates Bits/Sec.	4-ϕ Driver Power (mW)	Comments
Continuous Search	P_S	0 to 5000[1]	230	Maximum Driver Power
Refresh Only Mode	P_{REF}	0	19	–
Shift/Multiple Data/Shift (MIN)	P_{SMS} (MIN)	2 Megabit	19	Maximum Data Rate (16 Data Cycles between Shifts)
Shift/Multiple Data/Shift (MAX)	P_{SMS} (MAX)	970 Kilo Bit[2]	167	Shift after each Data Cycle
Search with Block Transfer	P_{SDB}	2 Megabit[3]	38	Data Block 4K Words

Notes:
1. Worst case decrement pattern on shift locations.
2. Input data rate is actual data rate and not average data rate.
3. Does not include search time.

such has internal circuitry designed to minimize the cross-coupling transients during clock transitions. The pin configuration and block diagram are shown in Figure 24 and 25 respectively. As shown in Figure 25, the output signal is fed back to an output transition control to assure that the clock transition times do not fall below the minimum required by CCD devices.

In most memory systems, and certainly in large CCD memory systems the power dissipation of any drivers is very important. Because the 5244 is implemented by CMOS devices, the quiescent power dissipation is very low. The DC characteristics of the 5244 are shown in Table IV. I_{DD0} and I_{DD1} (standby and operating currents respectively) are defined for zero frequency ($t\phi/2$) and for a frequency of f = 0.67MHZ respectively. The readers attention is directed to the equation for operating current shown in note 1, Table IV. This equation gives the expected operating current as a function of shift time ($t\phi/2$) and can be used accordingly.

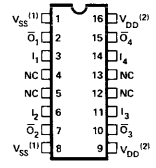
Driver Characteristics

The 5244 is specified to drive four 2416's and have the characteristics required by the 2416. These requirements are placed in two categories:

1.) Transition time
2.) Cross coupled voltage suppression

The transition time of the 5244 is specified between a minimum of 30nsec and a maximum of 75nsec for phases 1 and 3 and a minimum of 30nsec and maximum of 90nsec for phases 2 and 4 when driving four 2416's. When using the driver in this configuration, no additional components (such as resistors) are necessary to be added in the output. However, if fewer than 4 2416's are driven by the

PIN CONFIGURATION



NOTES: 1. BOTH PIN 1 AND 8 MUST BE CONNECTED TO V_{SS}.
2. BOTH PIN 9 AND 16 MUST BE CONNECTED TO V_{DD}.

PIN NAMES

$I_1 \cdot I_4$	TTL INPUT
$\bar{O}_1 \cdot \bar{O}_4$	DRIVER OUTPUT
V_{DD}	+12V POWER SUPPLY
NC	NOT CONNECTED
V_{SS}	GROUND

Figure 24. 5244 Pin Configuration.

BLOCK DIAGRAM

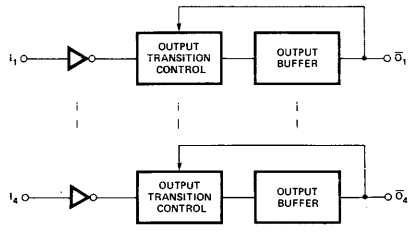


Figure 25. 5244 Block Diagram.

Table IV. 5244 D.C. and Operating Characteristics.

T_A = 0°C to 70°C, V_{DD} = +12V ±5%, V_{SS} = 0V

Symbol	Parameter	Limits Min.	Typ.	Max.	Unit	Test Conditions
I_{IL}	Low Level Input Current	-10	±0.1	10	μA	$V_{IN} \leq V_{IL}$
I_{IH}	High Level Input Current	-10	±0.1	10	μA	$V_{IN} \geq V_{IH}$
V_{IL}	Input Low Voltage		+1.2	+0.85	V	
V_{IH}	Input High Voltage	+2.0	+1.5	V_{DD}+1.0	V	
V_{OL}	Output Low Voltage	0	0.03	+0.1	V	I_{OL} = 5mA
V_{OH}	Output High Voltage	V_{DD}-0.1	V_{DD}-.03	V_{DD}	V	I_{OH} = -5mA
I_{DD0}	Standby Current		2.0	4.0	mA	$V_{IN} \geq V_{IH}$, $V_{IN} \leq V_{IL}$, f = 0 MHz
I_{DD1}	Operating Current		75	105[1]	mA	$V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f=0.67MHz [2]

[1] $I_{DD1} = 4.0mA + \frac{75.4mA}{t0/2\ (in\ \mu s)}$

[2] Output load = four 2416 clock inputs or equivalents per Figure 23.

SERIAL

5244, an external capacitor must be added to each phase driver as shown in Figure 26. These capacitors must be added to assure that the driver transition time is not less than the minimum specified by the 2416.

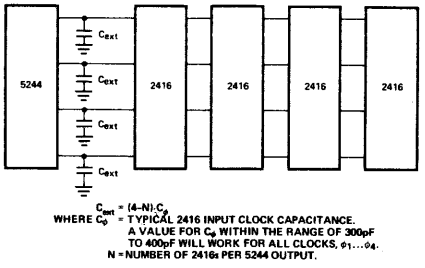


Figure 26. External Loading Requirements When Driving Fewer Than Four 2416's.

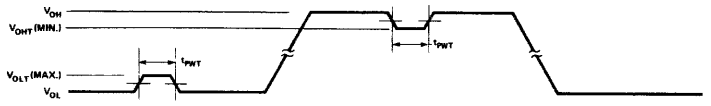
A more difficult parameter to specify is the cross-coupled voltage transient resulting from driving four 2416's. Figure 27 shows the cross-coupling to be expected (vertical scale is exaggerated). The cross coupled noise suppression is specified both in level above and below quiescent and in time. The designer is reminded that the coupling transients shown assume a reasonable signal distribution the printed circuit board of the clock inputs. A typical distribution technique acceptable for CCD devices is shown in the Memory Array Layout section.

The relationship between the 5244 driver output specification, and the 2416 input requirements are shown in Figure 28. As shown in these diagrams, the specifications associated with the 5244 allow an adequate noise margin when operating with the 2416's

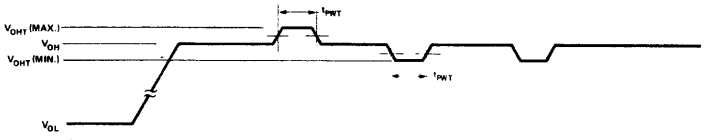
Typical Waveforms of the 5244

Typical waveforms of the 5244 driving 4 2416's are shown in Figure 29. The driver placement shown in this figure is that described in Figure 36.

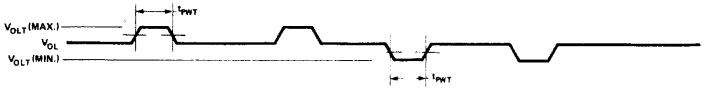
5244 OUTPUT DRIVING 2416 ϕ_1



5244 OUTPUT DRIVING 2416 ϕ_2



5244 OUTPUT DRIVING 2416 ϕ_3



5244 OUTPUT DRIVING 2416 ϕ_4

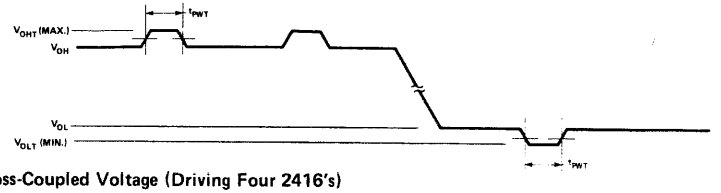


Figure 27. 5244 Output Cross-Coupled Voltage (Driving Four 2416's)

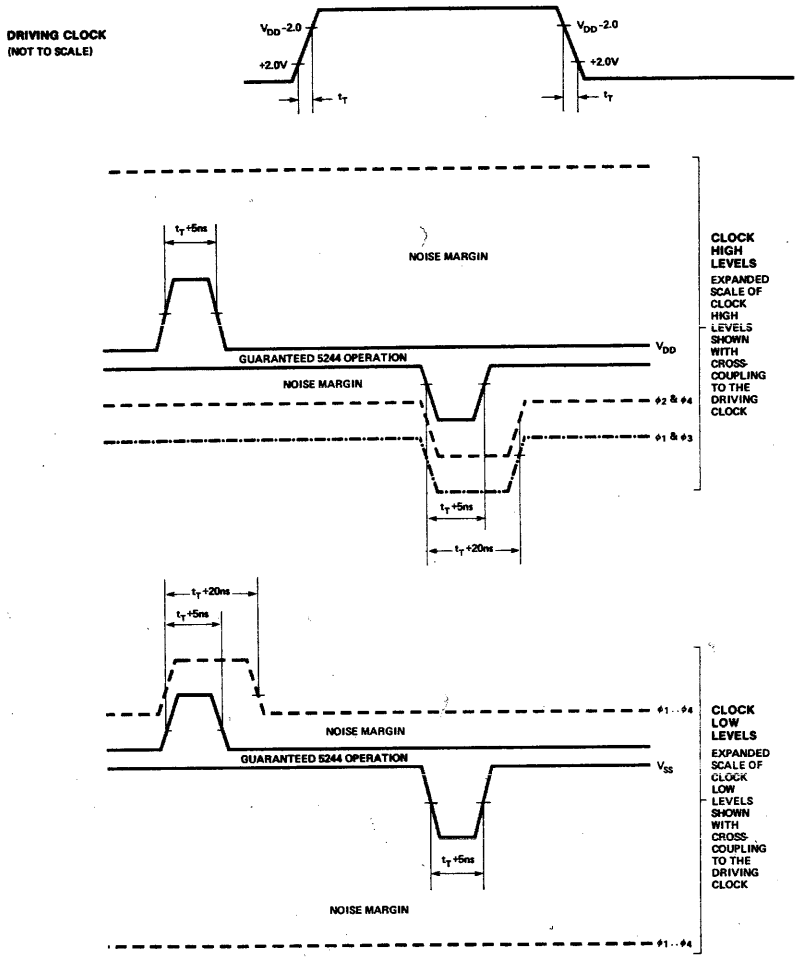


Figure 28. Noise Margins Between 5244 Output Specs and 2416 $\phi_1 \ldots \phi_4$ Input Requirements.

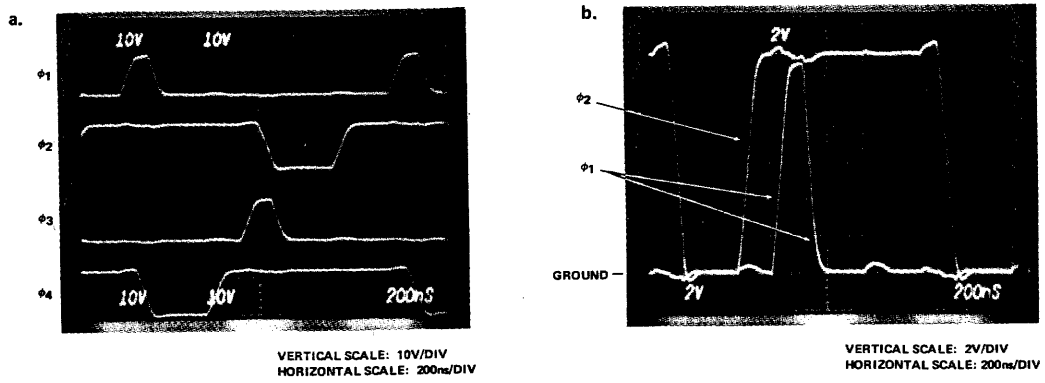


Figure 29. 5244 Typical Waveforms Driving Four 2416's.

DRIVING CS, CE, ADDRESS AND DATA-IN LINES

The remaining 2416 input lines, i.e. chip enable, chip select, address and data-in, exhibit a capacitive input of 4pF each. The low level margin (V_{IL1}) for these inputs is V_{SS} +.8V/-1.0V. The high level margin (V_{IH1}) for these signals is V_{DD} ±1.0 volts, except for data-in which has a V_{IHD} from 3.5 volts to V_{DD}+1 volt. The wide voltage margin on the data-in line allows it to be driven by a CMOS circuit or a TTL with a 470Ω pull-up resistor or the same type of driver used for the CE, CS, and address lines.

Maintaining Voltage Levels

The internal line to line coupling capacitance between the low capacitance inputs is less than 1pF. In addition, coupling can exist between signals at the card level. To suppress this total cross coupling effect, and thus maintain the required voltage margins, a driver with a low output impedance to V_{SS} and/or V_{DD} is required. Generally, drivers utilizing CMOS, complementary collector, and the totem pole type configurations, with an over-driven emitter follower, will suppress or recover from the coupling transients with sufficient margin. A driver employing a passive pull-up resistor or an emitter follower without over-drive voltage produces marginal results.

In addition to coupling, the over-shoot tendencies associated with the fast signal transition times also affect the voltage margins. It is important to locate the driver as close as possible to the memory array, usually split or branched from the center. Inserting a 10Ω (for multilayer board) or a 20Ω (for a two-sided printed circuit board) series damping resistor suppresses these over-shoot tendencies. The number of memory devices connected to the driver increases the coupling between inputs in addition to increasing the driver delay. These effects are shown in Figure 30 for an Intel® 3245 and 5235 quad drivers driving 4, 8, 32 and 64 2416 devices on a two sided printed circuit board array.

Sensing and Data-Out Characteristics

The 2416 data-out line is driven from an open drain MOS circuit which allows "OR" tying of the outputs. The access time of the 2416 is specified with a 5K pull-up resistor on the data-out pin to a 5 volt supply and a capacitive load of 50pF. The 50pF represents eight 2416 data-out lines OR tied. (i.e., 5pF per device and approximately .5pF/device stray capacitance.)

The waveforms in Figure 31 show the results of connecting 4, 8 and 16 2416 data out lines to the input of a series 74 type TTL gate. The recovery time of the data-out line is determined from the RC time constant of the data out line pull up resistor (including the sensing device input resistance) and the total data-out line load capacitance. This time constant should be less than 60% of the data cycle time to allow the bus to recharge from the previous cycle. The minimum value of the pull-up resistor is determined from the 2416 (I_{OL}) data out 3mA low sink current capability while maintaining less than +.45 volts above V_{SS} (GND). Limiting the data out sink current to 3mA results in an effective minimum pullup resistance of 1.7K ohms when connected to 5 volts and 4K ohms when connected to 12 volts.

The output of the 2416 goes low *only* when a logic "0" is read out. The output is held at a high level at all other times by the pull-up resistor. The advantage of this arrangement is that the time constant of the load capacitance and pull-up resistance has a minor effect on the access time.

Care should be taken when using a large value of pull-up resistance to assure that noise coupled into the output during sense time is not excessive.

In summary, the 2416 data out sensing characteristics are suitable to both high and low level CMOS

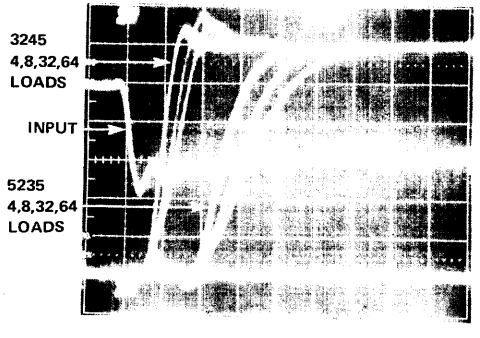


Figure 30. Driver Waveforms as a Function of Loading.

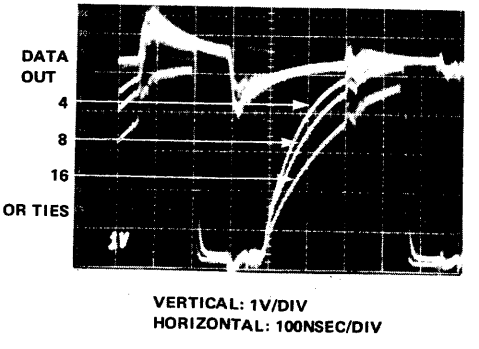


Figure 31. 2416 Data Out Waveforms OR Tied.

inputs and TTL inputs. The Intel® 3212 high input impedance 8-bit latch with three state output or the 3404 6-bit latch also provides system advantages when used as a 2416 sensing device.

CARD AND SYSTEM ORGANIZATION

The optimum organization of a CCD memory card is determined by the memory application, card expansion capability and memory word size requirements of the system. When a simple parity check or single error correction is used, it is desirable to organize the memory card to minimize multiple bit errors by avoiding common drivers and sensing circuits to more than one bit in a word. This is easy to accomplish where large memory systems are required. If the card is organized in a one or two bit configuration, the number of bits per word is obtained by adding additional cards. For example, such a card might be organized as 512K words by 1 bit. For this case, 8 cards would be required to obtain a word size of 8 bits. This system is capable of a data rate of 2 megabytes/sec.

Additional memory depth expansion is accomplished by additional basic storage units which also become very adaptable to four-phase clock bank switching techniques. Figure 32 shows the basic card organization for the 512K x 1-bit card.

Megabit Storage Card

In many previous systems, a requirement for a large amount of memory usually meant the necessity of having several printed circuit cards to achieve the storage requirements. With the introduction of a 16K CCD device, very high memory densities can be achieved on a single printed circuit card. As an example, the high density storage card shown in Figure 33 stores one million bits of information. This card is self contained in that all clock drivers, sense amplifiers, and data bus drivers are included on the card.

This card is organized as 128K words x 8 bits (and can be modified to 64K x 16) as shown in Figure 35. The data rate of this memory is two megabytes per second (i.e. sixteen megabits per second) as configured. (This high data rate is achieved with the four-phase clocks cycling at minimum frequency of 55 KHz.) The combination of high density and high data rates make this type of card ideal for use in many types of applications. The 128K x 8 CCD storage card operates in parallel on the eight bits of a given word to achieve a data rate of sixteen megabits per second. If the data stream is to enter the memory system at a *serial* data rate of sixteen megabits per second then the memory interface can be

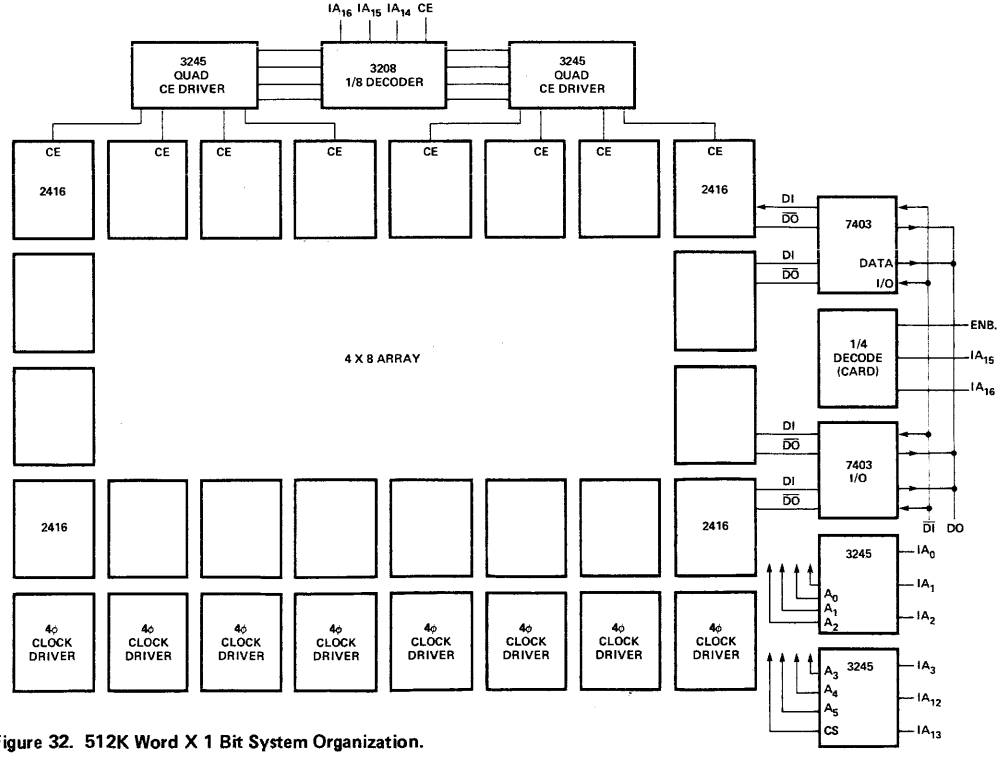


Figure 32. 512K Word X 1 Bit System Organization.

slightly modified to eliminate undesirable interruptions to the input and output data streams. Such a modification is shown in Figure 34 (for an eight megabit data rate).

Memory Array Layout

A well grided power distribution in the memory array is a very important layout consideration. Both

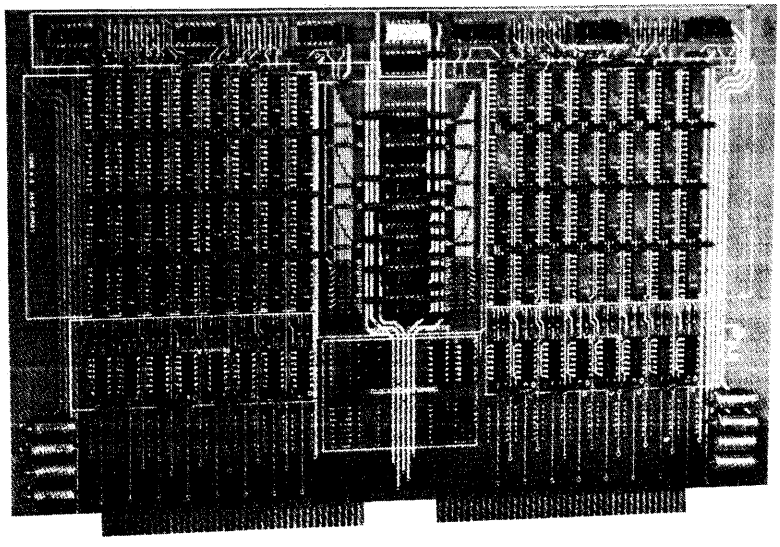


Figure 33. 128K Word X 8 Bit CCD Memory System (Megabit Card).

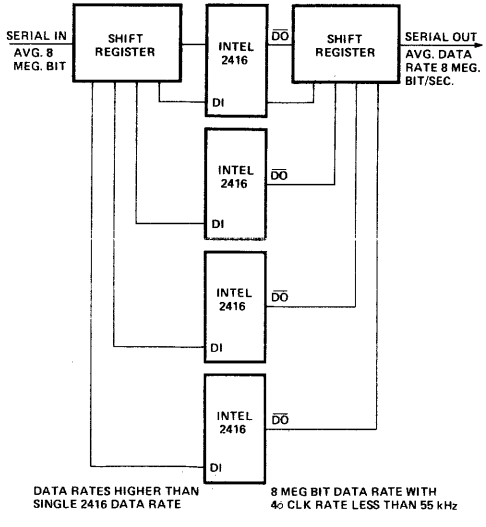


Figure 34. Paralleling 2416 to Handle Very High Data Rates.

voltage and ground buses should be bused in the horizontal and vertical directions through every memory component. Generally, the width of the bus traces is not as critical as the separation between the grid construction. *Even in multilayer construction, an internally grided or continuous structure is important to minimize the charge and discharge paths from the array to the drivers.*

All memory array signal traces are usually 15 mils wide, which allows them to fit between the device pins with sufficient margin. However, at least 50 mil clock traces are recommended because of the peak currents involved with 2416 four-phase clock lines when several 2416s are driven with minimum transition times. It is recommended that these clock lines be run next to a GND line back to the driver as shown in Figure 36. These wider traces and the GND separation between them lowers the series inductance and coupling properties of these clock lines. However, the ground trace between the clock lines is not required when an internal ground plane or voltage plane is incorporated into the card.

The memory array layout of the 64K x 16 memory described previously is shown in Figure 37.

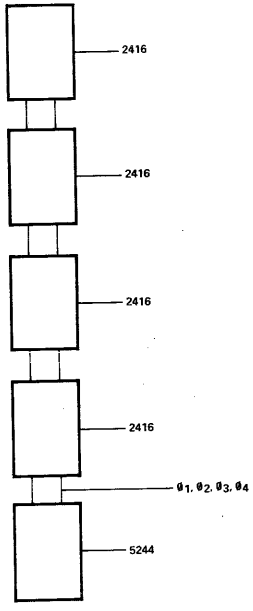


Figure 36. Four-Phase Clock Layout.

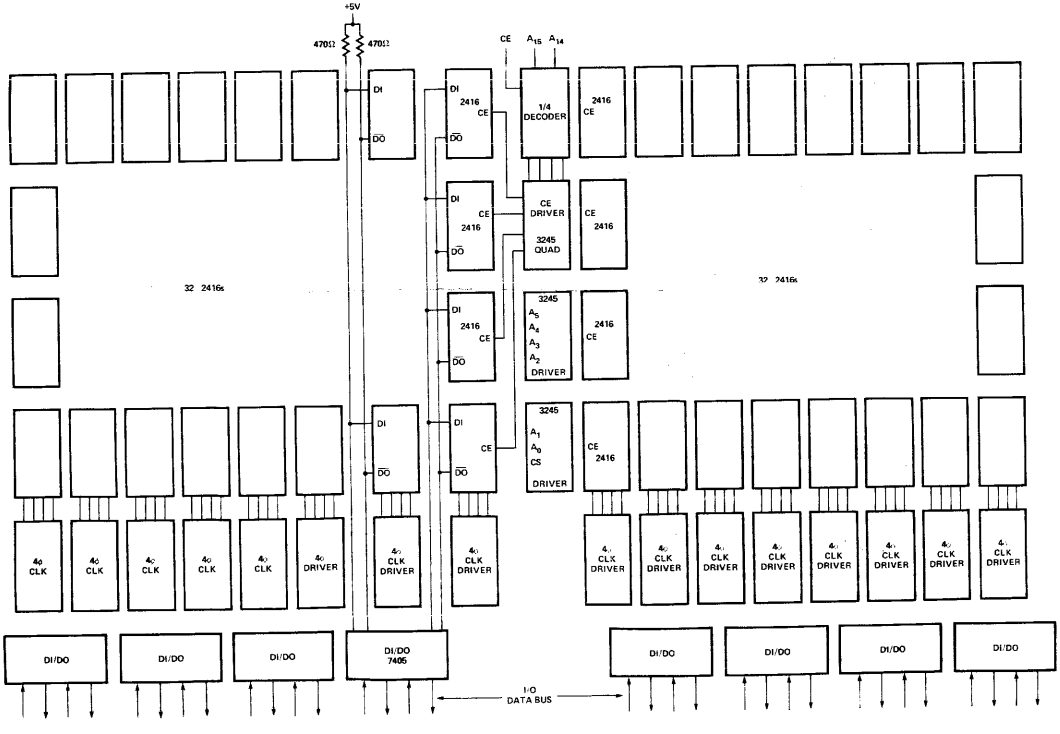


Figure 35. 128K Word x 8 Bit Card Organization.

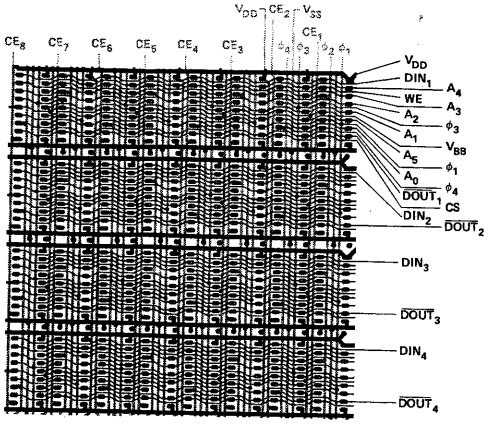


Figure 37. 2416 Memory Array Layout.

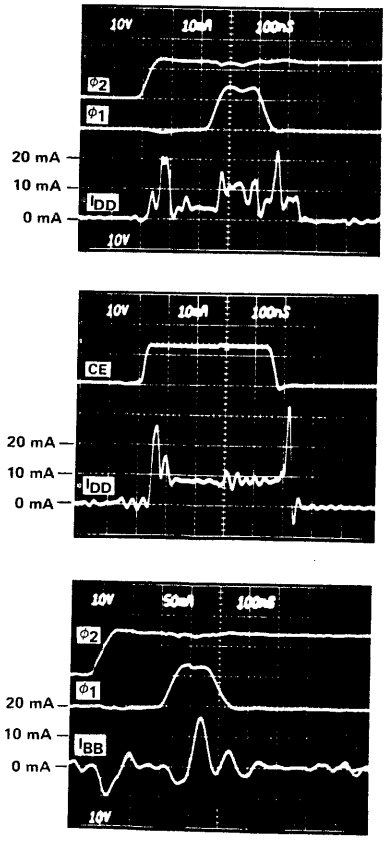


Figure 38. Transient Currents

Memory Array Decoupling

The 2416 decoupling requirements, as shown by the transient current waveforms in Figure 38, are very moderate. Tests show, from a 64 device 1 million bit board, that placing .1μF decoupling capacitors from V_{DD} to V_{SS} at every other device location in the array and a .1μF from V_{BB} to V_{SS} at the other devices will suppress the transient voltage spikes to less than 200mV.

However, on the four-phase clock drivers, a 1μF from V_{DD} to V_{SS} and 1μF from V_{BB} to V_{SS} is recommended for every two four-phase drivers.

Tantalum capacitors (~100μF) should also be added for low frequency decoupling.

SUMMARY

The 2416 has been shown to be a versatile and flexible memory device. This flexibility is maximized when a thorough understanding of the internal storage organization is achieved. Interface drivers and control circuits have been discussed for several of the more typical applications to demonstrate the ease with which the 2416 can be used.

ACKNOWLEDGMENT

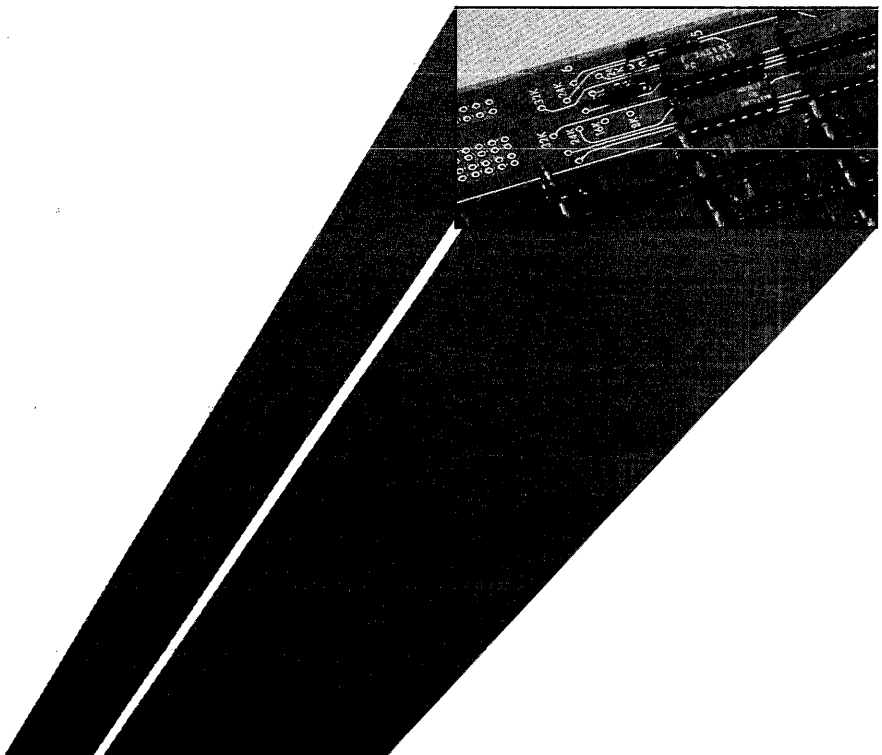
Appreciation is extended to Jim Oliphant of the Application Engineering Department for his review and comments on this chapter.

SERIAL MEMORIES

	Type	No. of Bits	Description	No. of Pins	Electrical Characteristics Over Temperature					
					Data Rep. Rate		Power Dissipation	Input Output	Clock	
					Min.	Max.	Max.[1]	Levels	Levels	Supplies[V]
SILICON GATE MOS	**1402A**	1024	Quad 256-Bit Dynamic	16	10kHz	5MHz	500mW	TTL	MOS/TTL	5, -5 or 5, -9
	1403A	1024	Dual 512-Bit Dynamic	8	10kHz	5MHz	500mW	TTL	MOS/TTL	5, -5 or 5, -9
	1404A	1024	1024-Bit Dynamic	8	10kHz	5MHz	500mW	TTL	MOS/TTL	5, -5 or 5, -9
	1405A	512	Dynamic Recirculating	10	10kHz	2MHz	400mW	TTL	MOS/TTL	5, -5 or 5, -9
	2401	2048	Dual 1024-Bit Dynamic Recirculating	16	25kHz	1MHz	350mW	TTL	TTL	+5
	2405	1024	1024-Bit Dynamic Recirculating	16	25kHz	1MHz	350mW	TTL	TTL	+5
	2416	16,384	CCD Serial Memory	18	125kHz	2MHz	300mW	TTL	MOS	+12, -5

Note: Power Dissipation calculated with maximum power supply current and nominal supply voltages.

Support Circuits



Using Support Circuits for Dynamic RAMs

Jim Oliphant
Application Engineering

Contents

INTRODUCTION

The evolution of semiconductor dynamic Random Access Memories has resulted in devices which are very easy to use in system applications. These devices have evolved to the point that, today, some are fully TTL compatible including clocks, while others have all but the clock input TTL compatible. Most random access memory devices are treated as "just another component" by system designers – a very desirable situation.

Although there are many ways to design a solid and reliable memory system, care must be exercised in the implementation of the support circuits which "surround" the memory devices. In many cases, marginal memory system operation can be traced directly to marginal or inadequate peripheral components. This is especially true in those memory systems which exhibit "soft" failures. ("Soft" failures are usually not repeatable and are almost completely random.) These "soft" failures can result from timing glitches causes by refresh interference, inadequate high or low input levels to the memory device, or very tight timing constraints in the system. Using the reasonably conservative design techniques discussed in this Application Brief allows the memory system designer to obtain maximum system speed with minimum peripheral power. This, in turn, allows the system into which the memory goes to treat its memory as just another "black box."

Common characteristics of dynamic RAMs are the requirements for:

1. Refresh
2. Signal drive (TTL or MOS level)

The first requirement allows high density, high speed, and low power RAMs to be designed in the first place. The second requirement is the result of the large number of memory devices (and therefore high capacitance) usually contained on a printed circuit board.

The pupose of this Application Brief is to describe support circuits which are used to perform refresh control and multiplexing functions and drivers used to drive the memory array. The devices described are used primarily with 16 and 22-pin 4K and 16-pin 16K RAMs. For reference, those devices to be described in this Brief are shown in Table I.

This Application Brief is divided into two major sections. The first section describes Refresh Controllers and Address Multiplexers and the second section describes TTL and MOS level drivers (for clocks, address lines, etc.).

REFRESH SUPPORT CIRCUITS

Two relatively new types of memory support circuits have been made available recently, Refresh Controllers and Address Multiplexers. The devices in this category which will be discussed are Refresh Controller/Address Multiplexer – Intel® 3222, and Address Multiplexers – Intel® 3232 and 3242. As shown in Table I, the 3222 is used primarily with 22-pin 4K RAMs, while the 3232 and 3242 are used with the 16-pin 4K and 16K RAMs, respectively.

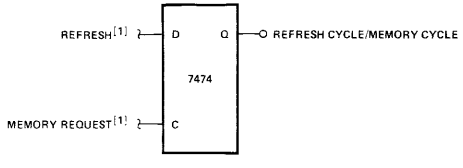
Refresh Controllers/Address Multiplexers

In any memory system utilizing dynamic RAMs, some method must be provided to periodically refresh the contents of memory. Although the design of a refresh controller using standard TTL logic gates is not difficult, care is required to avoid refresh interference (especially in asynchronous systems).

Refresh interference is usually caused by the inability of system logic to distinguish between a simultaneous memory cycle and refresh cycle request. The cause is most likely the result of using a latch improperly in trying to distinguish between the two types of cycles. An example of the improper use of a latch is shown in Figure 1. In this figure, the D input is asynchronous from the clock input C. If both should occur simultaneously, the set-up time required between the clock and data inputs is violated and the latch state is indeterminate for an undefined period of time. This indeterminate state can cause *both* a refresh and memory cycle to be started almost simultaneously, causing errors to occur.

Table I. Support Circuit Characteristics

FUNCTIONS PERFORMED	DEVICE		
	3222	3232	3242
Refresh Controller	X		
Refresh Counter	X	X	X
12 Two-Way Multiplexers (used with 22-pin 4K RAM)	X		
6 Three-Way Multiplexers (used with 16-pin 4K RAM)		X	
7 Three-Way Multiplexers (used with 16-pin 16K RAM)			X
Driver Capability		X	X
Zero Refresh Address Detect		X	X



NOTE:
[1] REFRESH AND MEMORY REQUEST ARE ASYNCHRONOUS

Figure 1. Improper Use of Latch

In addition to logic controller functions, the system refresh controller is required to have a sequential counter for the refresh addresses and an address multiplexer to multiplex between refresh and system addresses. Most controller designs able to handle all of the above requirements require a minimum of 12 IC packages in addition to a moderate amount of design and debug time.

The Intel® 3222 is designed to perform the functions associated with a system refresh controller. The 3222 is designed especially for systems using 22-pin 4K RAMs such as the Intel® 2107B.

The 3222 performs the following functions:

1. Selection between a Refresh and Read/Write cycle (system control)
2. 64 refresh address counter
3. 6-bit refresh and system address multiplexer
4. Refresh timing control generator

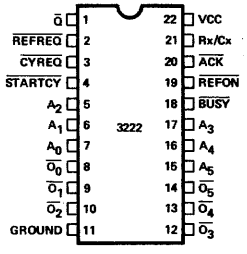


Figure 2. 3222 Pin Configuration

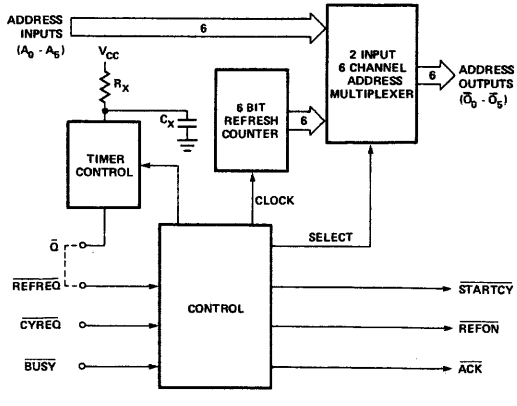


Figure 3. 3222 Block Diagram

The pin configuration for the 3222 is shown in Figure 2. An internal block diagram of this device is shown in Figure 3, outlining the four functions described previously. The use of the 3222 is made easier if the designer understands the internal logic circuits of the device. The internal logic diagram of the 3222 is shown in Figure 4. Each of the four device functions is described using the internal logic diagram.

System Control

The system control logic internal to the 3222 performs two functions:

1. Selects either a Refresh or Read/Write Cycle (depending on input).
2. Provides external control signals back to the system.

The first function – selection between a refresh and read/write cycle – is most important to the designer because it eliminates the chance of refresh interference associated with many new system designs. This function is performed by the priority latch shown in Figure 4. This latch has been designed so that the simultaneous occurrence of a cycle request ($\overline{CYREQ}$) and refresh request ($\overline{REFREQ}$) does not cause the latch to enter a long period of indecisiveness. (This problem may occur when such a latch is implemented with standard TTL logic gates.)

The second function – providing external control signals to the system – is implemented by the generation of the three control signals. These signals and their functions are:

1. Start Cycle ($\overline{STARTCY}$): Occurs shortly after a Refresh *or* Read/Write cycle is initiated. This signal is used by external control logic to start memory system timing.
2. Refresh On ($\overline{REFON}$): This signal is a logic low *only* when refresh cycle is beginning or is in progress.
3. Acknowledge ($\overline{ACK}$): $\overline{ACK}$ is a logic low *only* when the system is in a read or write cycle.

6-Bit Refresh Address Counter

An internal 6-bit refresh address counter provides for the refresh of the first 64 low-order addresses required for 4K RAMs. The address counter is automatically incremented by one at the end of every Refresh cycle. In addition, the counter is wrapped around so that after the 64th count the counter automatically resets to the first refresh address.

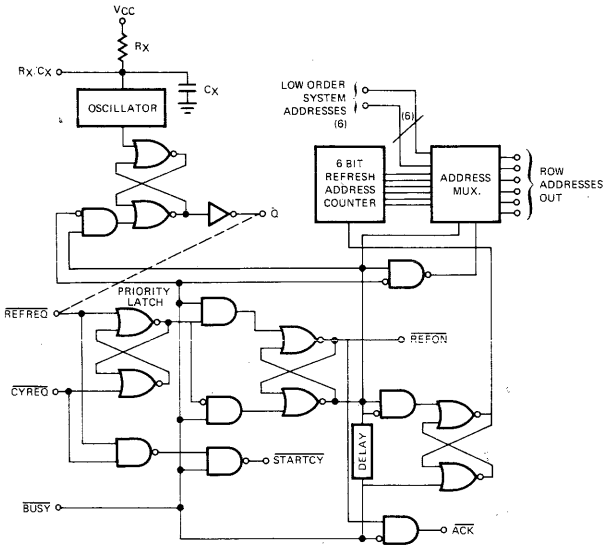


Figure 4. 3222 Internal Logic Diagram Support Circuits

Address Multiplexing

An internal 2-input-, 6-channel address multiplexer selects either the 6-bit refresh address or the 6 low-order system addresses. To allow minimum access time systems to be designed using the 3222, the 6 low-order system addresses are selected (i.e., available at the output pins) at all times except for refresh.

Refresh Timing Control

To round out the capability of the 3222, a refresh timing one-shot is incorporated in the device. This one-shot allows a distributed refresh mode to be used with no external circuits added. (If burst refresh is desired, an external one-shot is added, as will be explained later.)

The timing of the refresh interval is controlled by a simple RC network connected as shown in Figure 5. The relationship between the RC time constant and the time between refresh is given by:

1. $\frac{t_{REF}}{r} = 0.63 R_X C_X$

where:

t_{REF} = Total time between refreshes in msec (e.g., 2 msec).

r = number of device addresses to be refreshed

R_X = external timing resistor in kΩ

C_X = external timing capacitor in μF

The range of values associated with R_X and C_X are:

2. $3\ k\Omega \leqslant R_X \leqslant 10\ k\Omega$

and

3. $0.005\ \mu F \leqslant C_X \leqslant 0.02\ \mu F$

These conditions on R_X and C_X result in a range of refresh intervals (assuming r = 64) of:

4. $0.6\ msec \leqslant t_{REF} \leqslant 8.1\ msec$

This refresh range includes virtually all system refresh requirements for 64 refresh address RAMs.

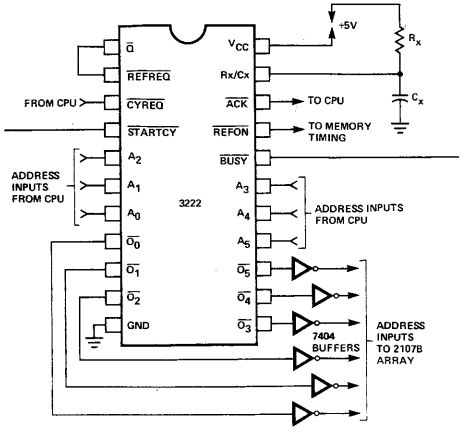
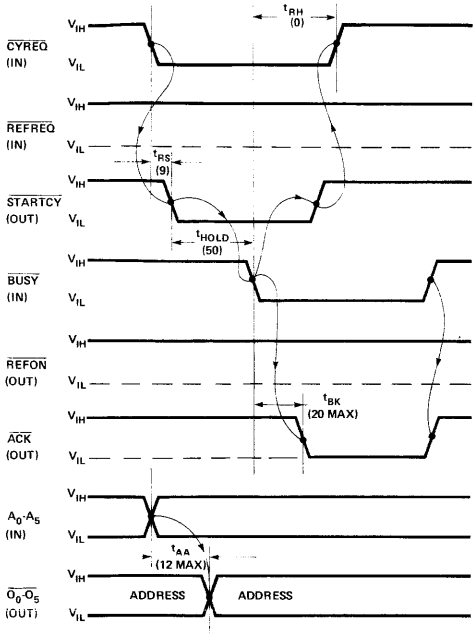
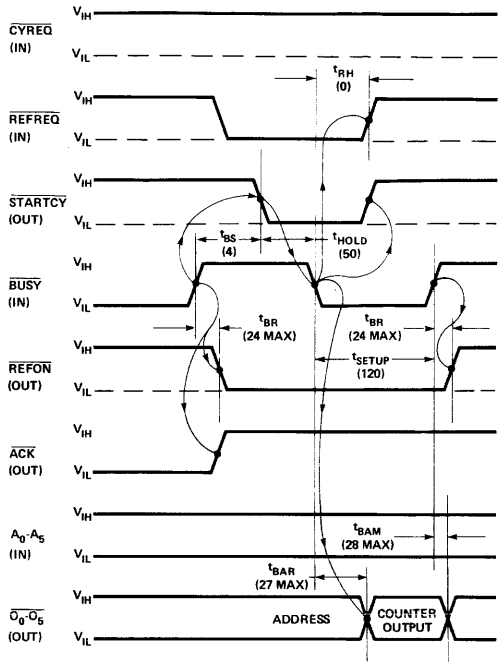


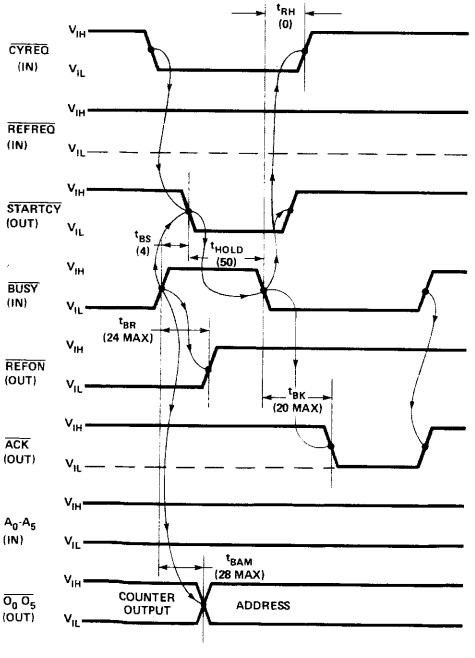
Figure 5. Refresh Timing Control



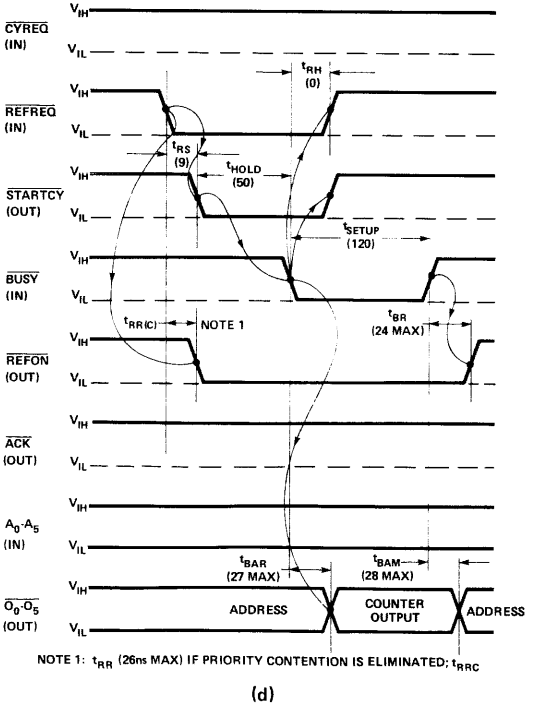
(a)



(b)



(c)



NOTE 1: t_{RR} (26ns MAX) IF PRIORITY CONTENTION IS ELIMINATED; t_{RRC}

(d)

Figure 6. 3222 Timing States

3222 System Operation

The 3222 Refresh Controller/Address Multiplexer is designed for memory systems using 22-pin RAMs such as the 2107B. The following discussion concentrates on the use of the 3222 in a system using just such a RAM. Because of the plethora of RAM timing specifications available, the discussion will be limited to the operation of the device with only those timing parameters critical to the 3222 being mentioned.

The two timing diagrams showing the combinations of system memory cycles/refresh cycles for the two Busy states are shown in Figure 6. A schematic of the logic required to implement timing/control for the 3222 is shown in Figure 7. In order to simplify the explanation of circuit operation, the discussion is limited to the following examples:

1. System Memory Cycle with Memory Not Busy
2. Refresh Cycle with Memory Busy (following System Cycle)
3. System Memory Cycle with Memory Busy (following Refresh Cycle)
4. Refresh Cycle with Memory Not Busy

The above four conditions are shown in Figure 8. using Cycle Request ($\overline{CYREQ}$) and Refresh Request ($\overline{REFREQ}$). In all system memory cycle examples, it is assumed that the system addresses are valid at the 3222 inputs (A_0–A_5) coincident with cycle request.

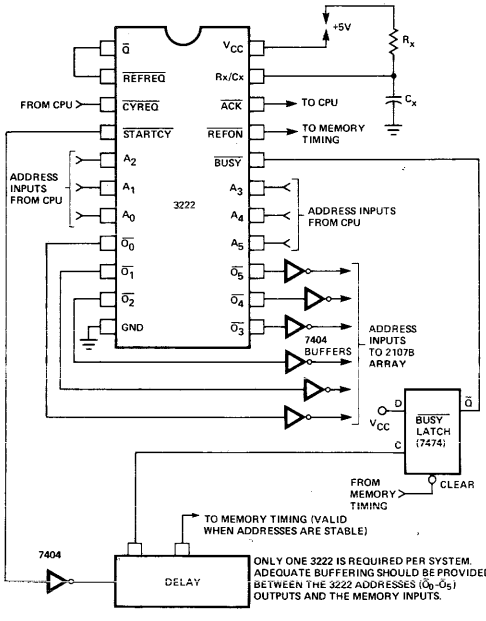


Figure 7. Timing/Control Logic for 3222

System Memory Cycle with Memory Not Busy

The first example is for a system memory cycle with memory not busy (refer to Figure 6a). The control function is followed by the arrows labeled 1–4. When $\overline{CYREQ}$ goes low, start cycle ($\overline{STARTCY}$) goes low at or before t_{RS} time (arrow 1). The $\overline{STARTCY}$ output is used to trigger a Busy latch at or after t_{HOLD} time. When the externally generated Busy signal goes low, it automatically sends $\overline{STARTCY}$ high and issues an acknowledge ($\overline{ACK}$) command from the 3222. The $\overline{ACK}$ output of the 3222 is used to signal the system controller that a memory cycle has been initiated and accepted by the processor. It is important to note that the system controller cannot issue a memory cycle request and not monitor the acknowledge output in an asynchronous system, since there is no other way to assure that the command has been accepted by the 3222. In a asynchronous system, however, the acknowledge out need not be monitored if refresh is designed *not* to occur during a data cycle.

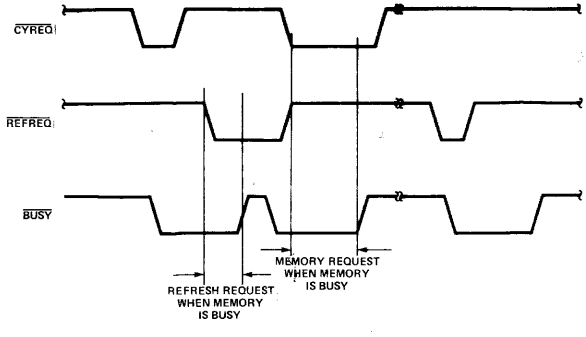


Figure 8. Four 3222 "Wait" States

Refresh Cycle with Memory Busy

The second example (for a refresh cycle with the memory busy) shows the timing expected to/from the 3222 for a refresh cycle requirement during a system access cycle. In this case, refresh has been requested while $\overline{BUSY}$ is low; i.e., the system is busy. After $\overline{BUSY}$ is set high (the $\overline{REFREQ}$ is still low) the $\overline{STARTCY}$ out goes low a maximum of t_{RS} later. After $\overline{BUSY}$ goes high, the refresh on output ($\overline{REFON}$) goes low, indicating the 3222 has accepted the refresh request. The $\overline{STARTCY}$ output going low is again used to set the external $\overline{BUSY}$ input low. Shortly after $\overline{BUSY}$ goes low, $\overline{STARTCY}$ and $\overline{REFREQ}$ are reset (i.e., go high) after the time indicated in Figure 6b, and the refresh addresses are valid at or after t_{BAR} time.

System Memory Cycle with Memory Busy

The third example assumes that the memory system is busy with a refresh cycle when a system access is requested. The major difference between this example and example 1 is that the system addresses at the output of the 3222 are not valid until after t_{BAM} time. It is noted that t_{BAM} is much greater than t_{AA} (see Figure 6c). Care should be exercised to assure that addresses are valid at the memory device at or before the clock (chip enable for the 2107B) goes high. More will be discussed about these requirements in the 3222 systems considerations section.

Refresh Memory Cycle with Memory Not Busy

The last example gives the timing for a lonesome refresh out in the middle of nowhere. The major difference between this example and example 2 is the occurrence of $\overline{REFON}$. When the memory is not busy, refresh is delayed by t_{RRC} relative to the refresh request input. All other timing conditions are as described in example 2.

3222 System Considerations

There are many ways to interface a 3222 to a memory system as there are creative designers. Therefore, it is useless to describe in detail the cleverness of a particular design. However, several hints regarding what to watch out for (or-how-not-to-foul-things-up-before-you-even-get-started) in the interface are useful. These hints are the requirements of the memory component used and not because of the 3222. The following hints should be observed:

1. Do not allow start cycle to begin a memory cycle before the addresses are valid at the memory component (see Figure 9). In an asynchronous system (where a system cycle or refresh cycle can be requested while the memory is busy) this means using the start cycle to address output delay maximum of t_{BAM} and not t_{AA}.
2. If delay lines are used as the timing element in the $\overline{STARTCY}$ path, care should be exercised to assure that the $\overline{STARTCY}$ output is long enough to propagate through the delay line with minimum distortion. The $\overline{STARTCY}$ output can be very short if a fixed pulse width is used for $\overline{CYREQ}$ and $\overline{REFREQ}$ (see Figure 10). This condition may result in the delay line not transmitting the signal properly (see Figure 11). For this reason, externally generated

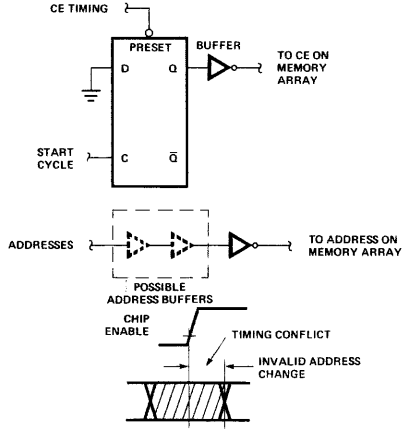


Figure 9. Possible Timing Conflict in Chip Enable Address Path

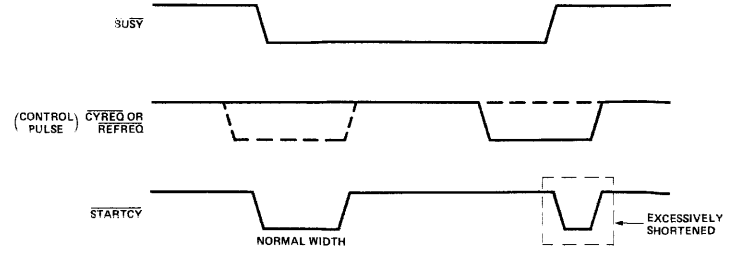


Figure 10. $\overline{STARTCY}$ Pulse Width

$\overline{CYREQ}$ and $\overline{REFREQ}$ inputs should be generated as shown in Figure 12. As shown in Figure 12, a latch is used to form the cycle and refresh requests $\overline{CYREQ}$ and $\overline{REFREQ}$, respectively. When a cycle is requested (either for an access or refresh), the request remains valid until it is serviced. An Acknowledge ($\overline{ACK}$) for a memory request or a refresh on ($\overline{REFON}$) are required to remove the request from the line.

3. If a delay line is used on $\overline{STARTCY}$, the line should not be driven directly from the 3222 because of insufficient output drive for this application.

4. Note that the address outputs (O_0–O_5) are buffered before driving a memory array. The 3222 output drive is not normally sufficient to drive the memory array directly.

5. A power-on reset must be provided to the 3222 to assure proper start-up operation. This reset should be a negative-going pulse on the BUSY line and is best provided by momentarily clamping the $\overline{BUSY}$ input to ground. The time constant selected should assure that the $\overline{BUSY}$ input is held at or below $V_{IL(MAX)}$ until the V_{CC} (+5V) supply has stabilized.

Burst Refresh Timing Generation

The 3222 is capable of generating both sequential and burst refresh cycles. Sequential refresh has been previously discussed. Consider the requirements for burst refresh generation.

Burst refresh is used primarily in systems which cannot be interrupted for refresh during data operation. These systems must have a time period when no memory accesses are required so that the entire memory can be refreshed. A circuit which allows for burst refresh cycles is shown in Figure 13.

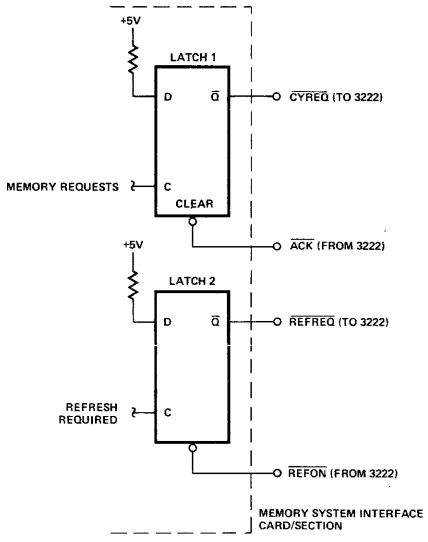


Figure 12. External Generation of $\overline{CYREQ}$ and $\overline{REFREQ}$

Operation of the circuit shown in Figure 13 is as follows. The refresh timing interval (usually 2 ms) is generated by timing circuits internal to the 3222 by using appropriate values of R_X and C_X. When the 3222 timer signals for refresh ($\overline{Q}$ output on the 3222 goes low), single-shot S_1 is triggered. The timing interval of S_1 is 64 times the refresh cycle time of the memory devices (for memory devices requiring 64-cycle refresh). S_1 allows astable multivibrator A_1 to cycle through all 64 refresh addresses at the desired cycle time (e.g., 500 ns). Refresh addresses are counted automatically at the completion of each refresh cycle. Note that S_1 is required because the $\overline{Q}$ output of the 3222 goes high after the first refresh cycle.

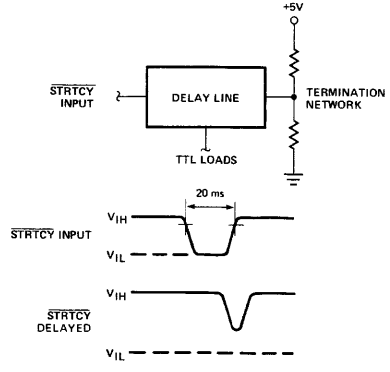


Figure 11. Delay Line Effects

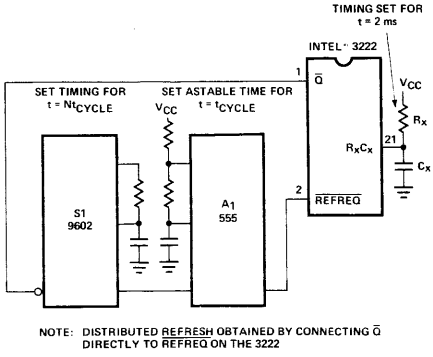


Figure 13. Burst Refresh Connections

16-Pin RAM Support Circuits

The support circuits required for 16-pin dynamic RAMs differ from those required for 22-pin devices. The primary difference for 16-pin RAMs (both 4K and 16K) is the requirement for three-way multiplexing on the address lines. (Recall that a single address line performs the functions of row, column, and refresh address.) The class of devices available for supporting 16-pin RAM memories are called Refresh Counter/Address Multiplexers. The two devices of this type to be discussed in this Application Brief are the Intel® 3232 and 3242. These devices are designed primarily for interface to the memory array when using 16-pin 4K and 16K RAMs, respectively.

The high packaging density realized by using 16-pin 4K RAMs is made possible by multiplexing the 12 (14 for 16K) system addresses on 6 (7 for 16K) pins. Because the addresses are multiplexed, it is necessary to provide two strobe clocks. These clocks are called Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$).

The relationship of addresses to $\overline{RAS}$ and $\overline{CAS}$ is shown in Figure 14. Operation of these 16-pin RAMs requires a three-way multiplexer to provide for the following functions:

1. low-order system addresses for the Row Address Strobe.
2. high-order system addresses during $\overline{CAS}$.
3. refresh addresses during refresh cycle.

3232/3242 Operation

Operation of the Intel® 3242 is identical to the 3232, with one exception. This difference is that a 7-bit, three-way multiplexer is provided on the 3242 (allowing 14 system addresses to be multiplexed by the device). Otherwise, description of operation of the 3232 applies equally to the 3242.

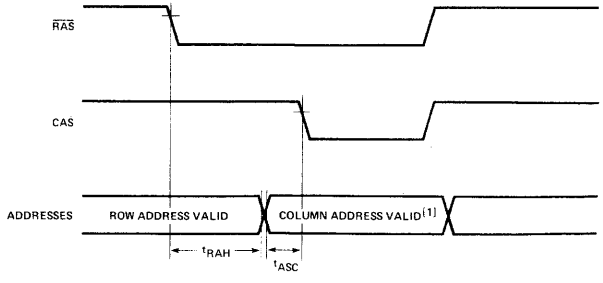
The pin configuration and logic diagram of the 3232 is shown in Figure 15. For completeness the pin configuration and logic diagram for the 3242 is shown in Figure 16.

The 3232/3242 provides four basic functions:

1. Address multiplexing
2. Refresh address counting
3. Refresh address zero detect output
4. Memory array address drive capability.

Timing considerations for a system memory cycle and refresh cycle are shown in Figures 17 and 18, respectively. The logic operation is evident from Figures 15 and 16.

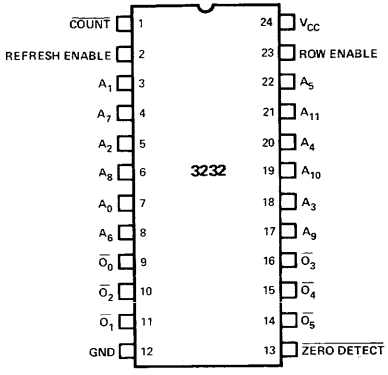
The zero detect function provides a means of keeping track of refresh addresses during burst mode refresh cycles. When using the 3232/3242 it is important to remember that momentary indications of zero detect are likely when incrementing the refresh address counter.



NOTE: [1] HOLDING COLUMN ADDRESSES STABLE THROUGHOUT CAS IS NOT REQUIRED BY DEVICE, BUT IS DESIRABLE FROM SYSTEM STANDPOINT.

Figure 14. Pin Dynamic RAM Clock Timing

PIN CONFIGURATION



NOTE: A_0 THROUGH A_5 ARE ROW ADDRESSES.
A_6 THROUGH A_{11} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_5)
L	L	COLUMN ADDRESS (A_6 THROUGH A_{11})

$\overline{\text{COUNT}}$ – ADVANCES INTERNAL REFRESH COUNTER.
$\overline{\text{ZERO DETECT}}$ – INDICATES A ZERO IN THE REFRESH ADDRESS (USED IN BURST REFRESH MODE).

LOGIC DIAGRAM

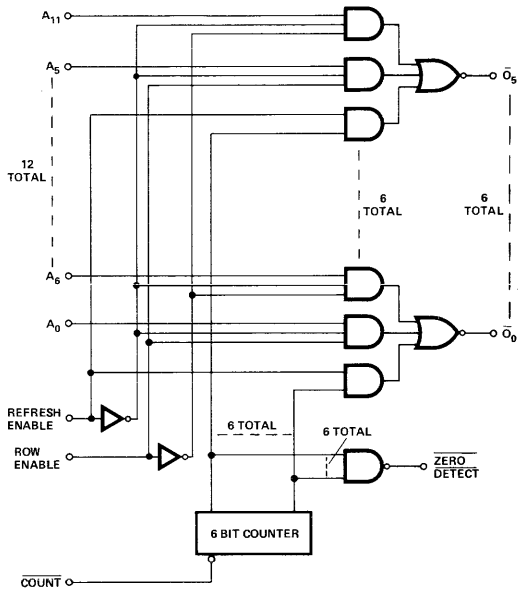
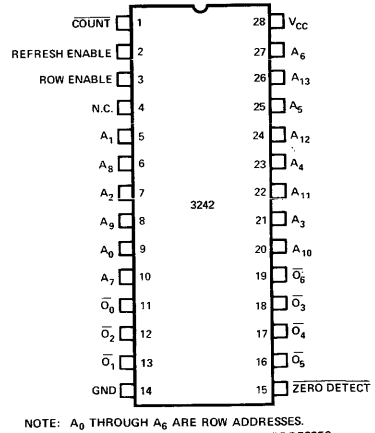


Figure 15. Pin Configuration and Logic Diagram

PIN CONFIGURATION



NOTE: A_0 THROUGH A_6 ARE ROW ADDRESSES.
A_7 THROUGH A_{13} ARE COLUMN ADDRESSES.

TRUTH TABLE AND DEFINITIONS:

REFRESH ENABLE	ROW ENABLE	OUTPUT
H	X	REFRESH ADDRESS (FROM INTERNAL COUNTER)
L	H	ROW ADDRESS (A_0 THROUGH A_6)
L	L	COLUMN ADDRESS (A_7 THROUGH A_{13})

$\overline{\text{COUNT}}$ – ADVANCES INTERNAL REFRESH COUNTER.
$\overline{\text{ZERO DETECT}}$ – INDICATES ZERO IN THE FIRST 6 SIGNIFICANT REFRESH COUNTER BITS (USED IN BURST REFRESH MODE)

LOGIC DIAGRAM

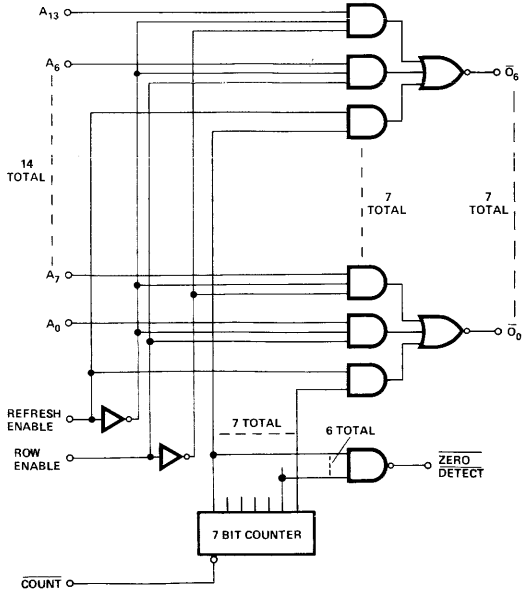


Figure 16. 3242 Pin Configuration and Logic Diagram

3232/3242 System Considerations

Interfacing the 3232/3242 to memory systems is very simple. An example of such an interface is shown in Figure 19. The 3232/3234 is specified for driving a capacitance load of 250 pF. Since the 4K/16K address inputs are implemented with MOS devices, there is only low input leakage current in both the high and low logic states. The address input capacitance is a maximum of 7 pF on the Intel® 2104A (16-pin 4K RAM). This indicates that, if worst case address capacitance is assumed, the 3232/3242 can drive 32 RAM devices, taking into account stray line capacitance. A more detailed description of the 3232/3242 as a driver is found in the Driver Circuits for Memory Arrays Section, along with various other types of drivers.

DRIVER CIRCUITS FOR MEMORY ARRAYS

Drivers for semiconductor memory arrays fall into two general categories:

1. Low level (TTL, ECL) to MOS level converter/drivers (for MOS level clocks, etc.)

2. TTL-TTL buffer drivers (for data lines, addresses, etc.).

These categories are treated separately in this Application Brief.

TTL to MOS Level Converter/Drivers

The continual improvement in TTL to MOS level drivers have kept pace with dynamic RAMs in ease of use. Gone are the days when drivers required external components (such as transistors or capacitors) or an extra power supply (usually 3V above the supply required for the memory). Today, there are several types of TTL-MOS drivers which require no external components nor additional power supplies for proper operation.

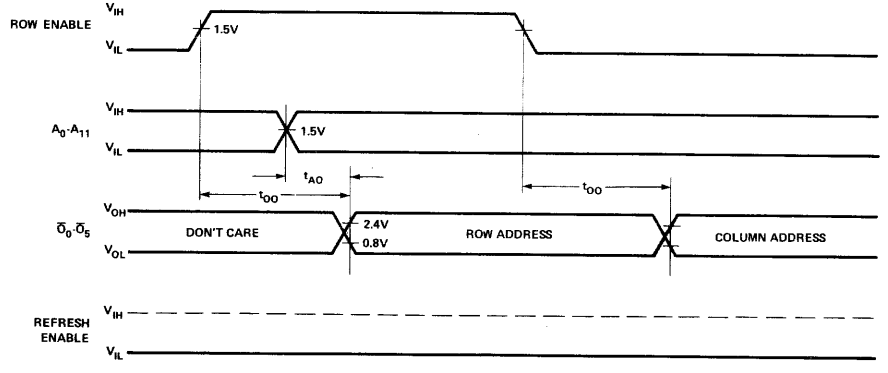


Figure 17. System Cycle Timing Relationships

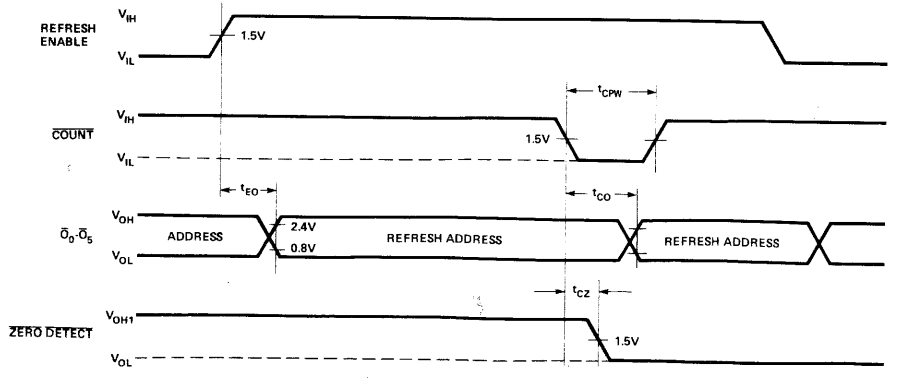


Figure 18. Refresh Cycle Timing Relationships

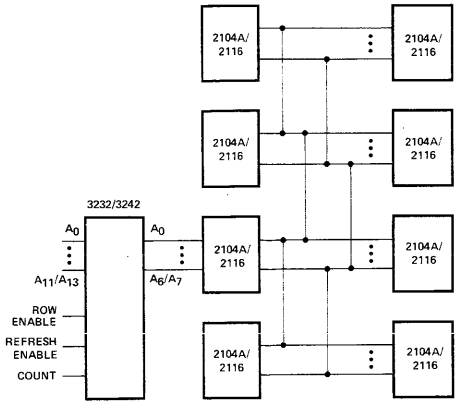


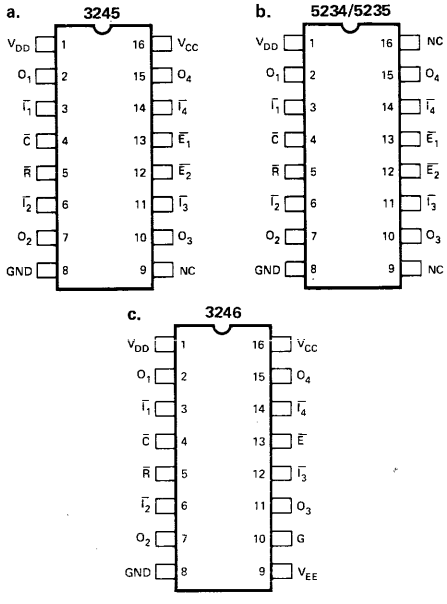
Figure 19. 3232/3242 Memory Array Interface

Intel has produced a complete family of Quad High Voltage Clock Drivers as shown in Figure 20. Figure 20 also shows the pin configuration for each of the members of the driver family.

The device speed, listed in Table II, is the maximum worst case value from the data sheet. For consistency, each driver is specified with minimum, typical, and maximum delays which correspond to load values of 150, 200 and 250pF, respectively, which also correspond to the minimum, typical and maximum capacitance, respectively, of nine 2107B chip enable inputs plus associated stray capacitance.

The two level gating structure, shown in the logic diagram, Figure 21, is common to all but the 3246. The gating structure for the 3246 is shown in Figure 28.

The 3245 is designed specifically to support the Intel® 2107B, although its input and output levels make it compatible with many other N-channel MOS RAMs. A specific application of the 3245 can be seen in the 2107B section of this handbook, where the Row Enable selection is accomplished by using this device.



PIN NAMES

$\bar{I}_1$–$\bar{I}_4$	DATA INPUTS	O_1-O_4	DRIVER OUTPUTS
$\bar{E}_1$, $\bar{E}_2$	ENABLE INPUTS	V_{CC}	+5V POWER SUPPLY
$\bar{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
$\bar{C}$	CLOCK CONTROL INPUT	V_{EE}	-5.2V POWER SUPPLY
NC	NO CONNECTION	G	ECL GROUND REFERENCE

Figure 20. Quad Clock Driver Pin Configuration

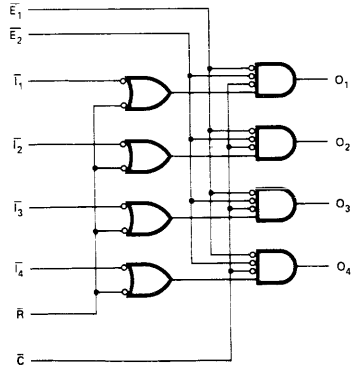


Figure 21. 3245, 5234, 5235 Quad Family Logic Diagram

Table II. Quad Clock Drivers

Device Type	Input Level		Output Level		Speed (1)	Power Dissipation	Power Supplies
	V_{IL}	V_{IH}	V_{OL}	V_{OH}			
3245	0.8	2.0	0.45	V_{DD}-0.5	32nS	485mW	+5,+12
3246	-1.500	-1.025	0.45	V_{DD}-0.5	30nS	725mW	+5,+12,-5.2
5234	2.0	V_{DD}-2.0	0.4	V_{DD}-0.4	100nS	1.4μW	+12
5235/-1	0.8	2.0	0.4	V_{DD}-0.4	90/120nS	27mW	+12

Note: 1. Maximum Delay and Transition Time Driving 1 TTL Gate and 250pF.

Table III. 3245 D.C. Characteristics

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%.

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FD}	Input Load Current, $\bar{I}_1, \bar{I}_2, \bar{I}_3, \bar{I}_4$		-0.25	mA	V_F = 0.45V
I_{FE}	Input Load Current, $\bar{R}, \bar{C}, \bar{E}_1, \bar{E}_2$		-1.0	mA	V_F = 0.45V
I_{RD}	Data Input Leakage Current		10	μA	V_R = 5.0V
I_{RE}	Enable Input Leakage Current		40	μA	V_R = 5.0V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5mA, V_{IH} = 2V
		-1.0		V	I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.50		V	I_{OH} = -1mA, V_{IL} = 0.8V
			V_{DD}+1.0	V	I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs		0.8	V	
V_{IH}	Input High Voltage, All Inputs	2		V	

Table IV. 3245 Power Supply Current Drain and Power Dissipation

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions – Input states to ensure the following output states:	Additional Test Conditions
I_{CC}	Current from V_{CC}	23	30	mA	High	V_{CC} = 5.25V V_{DD} = 12.6V
I_{DD}	Current from V_{DD}	19	26	mA		
P_{D1}	Power Dissipation	365	485	mW		
	Power Per Channel	91	121	mW		
I_{CC}	Current from V_{CC}	29	39	mA	Low	
I_{DD}	Current from V_{DD}	12	15	mA		
P_{D2}	Power Dissipation	300	388	mW		
	Power Per Channel	75	97	mW		

Table V. 3245 A.C. Characteristics. T_A = 0° to 75° C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%

Symbol	Parameter	Min.[1]	Typ.[2,4]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	5	11		ns	R_{SERIES} = 0
t_{DR}	Delay Plus Rise Time		20	32	ns	R_{SERIES} = 0
t_{+-}	Input to Output Delay	3	7		ns	R_{SERIES} = 0
t_{DF}	Delay Plus Fall Time		18	32	ns	R_{SERIES} = 0
t_T	Output Transition Time	10	17	25	ns	R_{SERIES} = 20Ω
t_{DR}	Delay Plus Rise Time		27	38	ns	R_{SERIES} = 20Ω

Notes: 1. C_L = 150pF (minimum C_L for 9 4K RAMs)
2. C_L = 200pF (typical C_L for 9 4K RAMs). Typical values measured at T_A = 25°C.
3. C_L = 250pF (maximum C_L for 9 4K RAMs).
4. Refer to Figure 22 for waveforms used.

The 3245, whose pin configuration is shown in Figure 20a has DTL and TTL compatible inputs as shown in Table III. The D.C. characteristics and power dissipation for various outputs states is shown in Table IV.

Table VI. 3245 Input Capacitance

Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance, $\overline{I_1},\overline{I_2},\overline{I_3},\overline{I_4}$	5	8	pF
C_{IN}	Input Capacitance, $\overline{R},\overline{C},\overline{E_1},\overline{E_2}$	8	12	pF

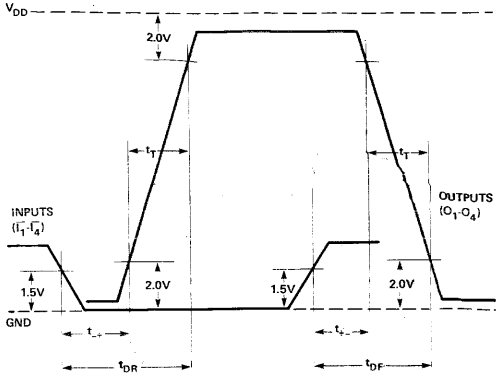


Figure 22. 3245 Waveforms

The A.C. characteristics are shown in Table V and the capacitance of the input pins is shown in Table VI. Figure 22 shows the threshold levels used in determining the delays specified in Table V.

Graphs showing the effect of capacitance loads on delay and rise times are shown in Figures 23a and b.

Waveforms of the 3245 driver in a 2107B system are shown in Figure 24a-d. The driver configuration used is shown in Figure 25.

Figure 24 shows the leading and trailing edge of chip enable at both the beginning and ending of the printed line for an added series resistance R of 10Ω. Note the transition time and overshoot for each of these edges. The overshoot is worst case at the leading edge at the driver end and on the trailing edge at the end of the line. The trailing edge overshoot is 2.2V while the leading edge overshoot is 1.5V. Both values are very marginal for system operation.

The effect of increasing the series resistance to 20Ω for the above driver is shown in Figure 24. Note that the transition time has increased but is still within entirely acceptable limits and the overshoots have been cut in half. the driver is now operating in an acceptable mode with minimal overshoot.

The effect of high temperatures (70°C) on the 3245 is shown in Figure 26. A 20Ω series resistor is used with the driver.

The power dissipation values shown in Table II are based on worst case conditions; power supplies at maximum voltage levels and outputs continuously enabled. In reality, the drivers operate on some duty cycle, as determined by the memory system cycle specifications. To realistically determine the power dissipated by the driver at a system level, calculations should be performed as shown below.

Referring to the 2107B chapter of this handbook, the minimum timing for a 2107B is with CE high for 230nS and low for 130nS for a 400nS minimum cycle. The total power dissipated in the driver for each cycle will be the sum of the power as shown by equation (1). For each memory cycle, 1 of the 4 driver elements will execute a cycle, while the other 3 outputs will remain low.

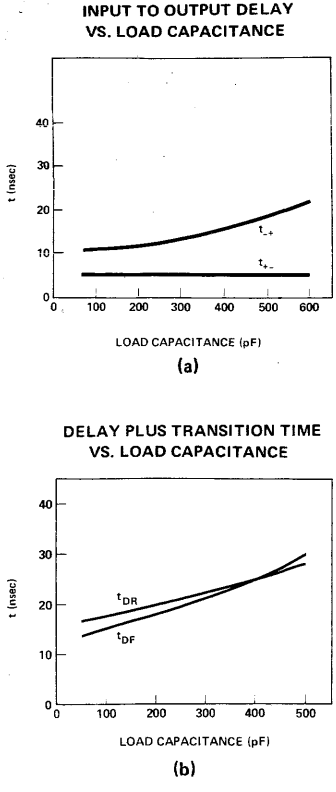


Figure 23. 3245 Delay and Transition Times as a Function of Load Capacitance

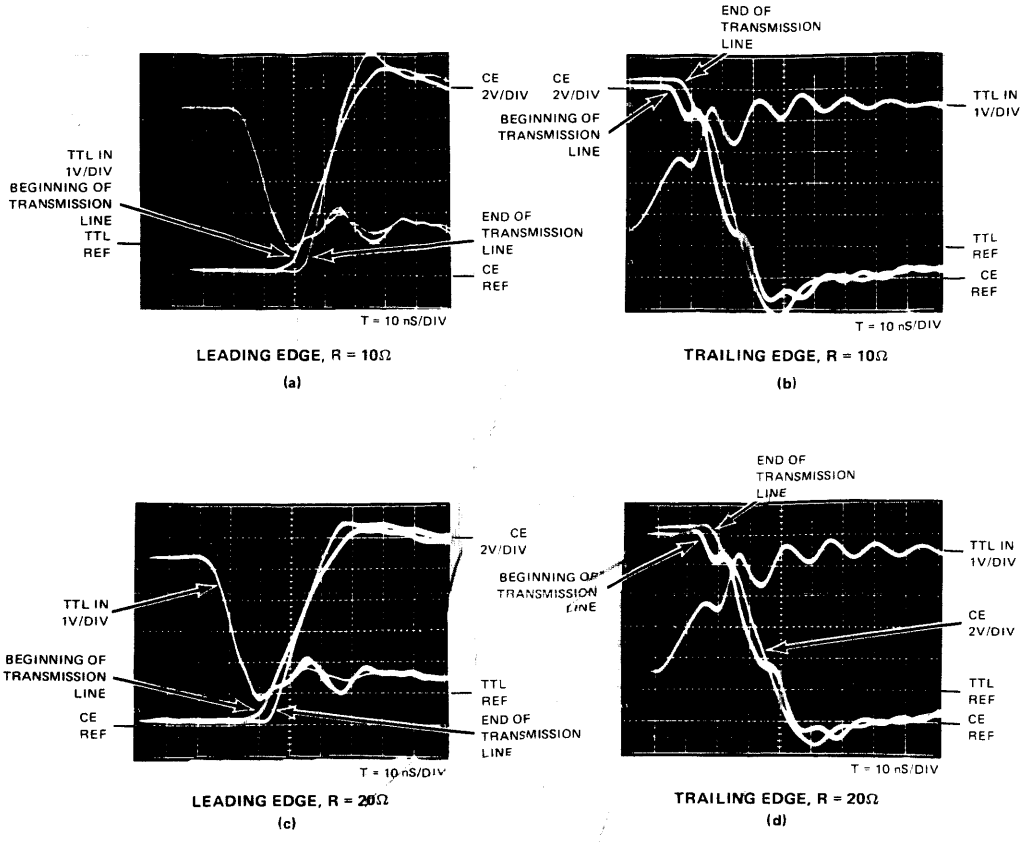


Figure 24. 3245 Typical Driver Waveforms

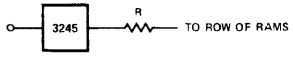


Figure 25. 3245 Driver Configuration

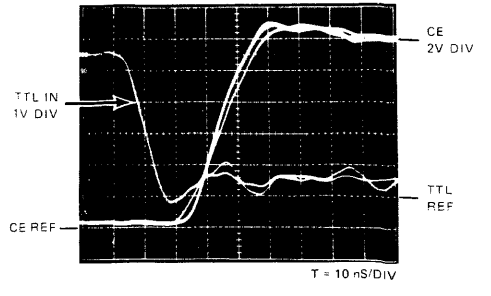
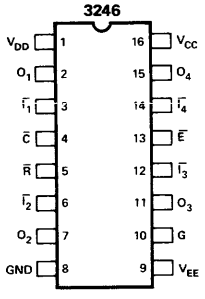


Figure 26. 3245 Driver Waveform with Temperature = 70°C

OTHER MOS LEVEL DRIVERS

3246 Operation

The Intel® 3246 is a QUAD ECL to MOS Driver designed for driving 4K N-channel MOS RAMs. The pin configuration and logic diagrams are shown in Figures 27 and 28. The device requires three power supplies, V_{DD} = 12V, V_{CC} = +5V and the ECL reference voltage V_{EE} of -5.25V.



PIN NAMES

$\overline{I}_1$-$\overline{I}_4$	DATA INPUTS	O_1-O_4	DRIVER OUTPUTS
$\overline{E}$	ENABLE INPUT	V_{CC}	+5V POWER SUPPLY
$\overline{R}$	REFRESH SELECT INPUT	V_{DD}	+12V POWER SUPPLY
$\overline{C}$	CLOCK CONTROL INPUT	V_{EE}	-5.2V POWER SUPPLY
		G	ECL GROUND REF.

Figure 27. 3246 Pin Configuration

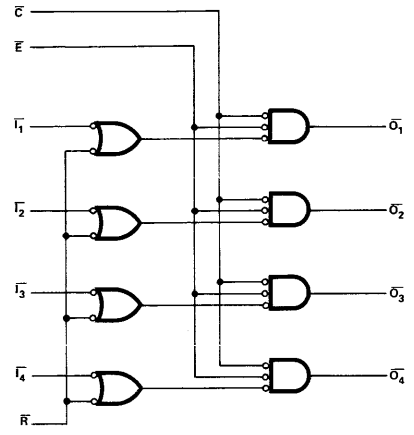


Figure 28. 3246 Logic Diagram

Tables VIII and IX presents the DC characteristics, including the power supply drain and input and output levels. To aid overall system planning, the supply currents are shown for outputs both high and low, so that power dissipation can be calculated as was done in the 2107B chapter.

Table VIII. 3246 D.C. Characteristics

T_A = 0°C to 75°C, V_{CC} = 5.0V ±5%, V_{DD} = 12V ±5%, V_{EE} = -5.2V ±5%.

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
I_{FD}	Input Load Current, $\overline{I}_1$, $\overline{I}_2$, $\overline{I}_3$, $\overline{I}_4$		0.5	mA	V_F = -0.8V
I_{FE}	Input Load Current, $\overline{R}$, $\overline{C}$, $\overline{E}_1$, $\overline{E}_2$		3.0	mA	V_F = -0.8V
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 10mA, V_{IH} = -1.025V
V_{OH}	Output High Voltage	V_{DD}-0.5		V	I_{OH} = -1mA, V_{IL} = -1.500V
V_{IL}	Input Low Voltage, All Inputs		-1.500	V	
V_{IH}	Input High Voltage, All Inputs	-1.025		V	

Table IX. 3246 Power Supply Current Drain and Power Dissipation

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions – Input states to ensure the following output states:	Additional Test Conditions
I_{CC}	Current from V_{CC}	20	26	mA		
I_{DD}	Current from V_{DD}	22	30	mA		
I_{EE}	Current from V_{EE}	-31	-39	mA	High	
P_{D1}	Power Dissipation	550	725	mW		
	Power Per Channel	137	181	mW		V_{CC} = 5.25V
I_{CC}	Current from V_{CC}	20	26	mA		V_{DD} = 12.6V
I_{DD}	Current from V_{DD}	14	20	mA		V_{EE} = -5.46V
I_{EE}	Current from V_{EE}	-29	-36	mA	Low	
P_{D2}	Power Dissipation	440	585	mW		
	Power Per Channel	110	146	mW		

SUPPORT

Table X. 3246 A.C. Characteristics

$T_A = 0°$ to $75°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$, $V_{EE} = -5.2V \pm 5\%$.

Symbol	Parameter	Min.[1]	Typ.[2]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	8	12		ns	$R_{SERIES} = 0$
t_{DR}	Delay Plus Rise Time		18	30	ns	$R_{SERIES} = 0$
t_{+-}	Input to Output Delay	8	14		ns	$R_{SERIES} = 0$
t_{DF}	Delay Plus Fall Time		25	35	ns	$R_{SERIES} = 0$
t_R	Rise Time	10	17	25	ns	$R_{SERIES} = 20\Omega$
$t_{\overline{DR}}$	Delay Plus Rise Time			40		$R_{SERIES} = 20\Omega$

Notes: 1. $C_L = 150pF$ (minimum C_L for 9-4K RAMs).
2. $C_L = 200pF$ (typical C_L for 9-4K RAMs). Typical values measured at $T_A = 25°C$.
3. $C_L = 250pF$ (maximum C_L for 9-4K RAMs).
4. Refer to Figure 29 for waveforms.

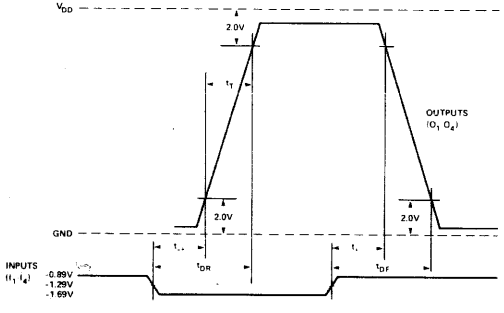


Figure 29. 3246 Waveform

The AC characteristics are shown in Table X, as specified with the waveforms shown in Figure 29.

The capacitive load attached to the output of the driver will affect the effective device speed. For this reason, the AC characteristics are specified with capacitive load values corresponding to typical system configurations. Figures 30a and b show the speed variations as a function of other capacitive loads.

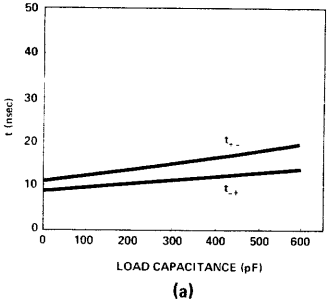
The input capacitance of the various input pins are shown in Table XI.

Table XI. 3246 A.C. Characteristics

$T_A = 25°C$

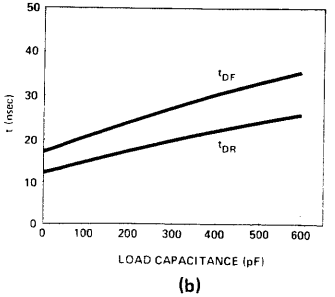
Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance, $\overline{I_1}, \overline{I_2}, \overline{I_3}, \overline{I_4}, \overline{R}$	4	7	pF
C_{IN}	Input Capacitance, $\overline{C}, \overline{E}$	8	12	pF

DELAY PLUS TRANSITION TIME
VS. LOAD CAPACITANCE



(a)

INPUT TO OUTPUT DELAY
VS. LOAD CAPACITANCE



(b)

Figure 30. 3246 Delays vs. Load Capacity

5234 and 5235 Operation

The Intel® 5234 and 5235 are respectively CMOS to MOS and TTL to MOS drivers implemented with Silicon Gate CMOS technology. Because of the very low power drain each device is suitable for systems where battery backup is used. The pin configuration is shown in Figure 20b, and the logic configuration is shown in Figure 21. The DC characteristics are shown in Tables XII and XIII for both devices.

The AC characteristics for the 5234 are shown in Table XIV, with waveforms shown in Figure 31a. In a similar manner Table XV and Figure 31b present the AC characteristics and waveforms for the 5235.

Pertinent input capacitance information is presented in Table XVI.

Table XII. 5234 D.C. Characteristics

T_A = 0°C to 70°C, V_{DD} = 12V ±5%.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_{LI}\|$	Input Load Current, $\bar{I}_1, \bar{I}_2, \bar{I}_3, \bar{I}_4$			0.1	μA	V_{IN} = 0 to V_{DD}
V_{OL}	Output Low Voltage		0.15	0.4	V	I_{OL} = 5mA
		-1.0	-0.15			I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.4	V_{DD}-0.15		V	I_{OH} = -5mA
			V_{DD}+.15	V_{DD}+0.5		I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs			2.0	V	
V_{IH}	Input High Voltage, All Inputs	V_{DD}-2.0			V	
I_{DD}	Supply Current		0.1	100	μA	V_{DD} = 13.2V, f = 0
I_{DD1}	Supply Current		13	20	mA	V_{DD} = 13.2V, f = 1MHz, C_L = 0, (See Figure 15a)

Note 1: Typical values are at 25°C and nominal voltage.

Table XIII. 5235 D.C. Characteristics

T_A = 0°C to 70°C, V_{DD} = 12V ±10%.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_{LI}\|$	Input Load Current		0.1	10	μA	$V_{IN} \leq 0.4V$ or $\geq 2.4V$
V_{OL}	Output Low Voltage		0.15	0.4	V	I_{OL} = 5mA
		-1.0	-0.15		V	I_{OL} = -5mA
V_{OH}	Output High Voltage	V_{DD}-0.4	V_{DD}-0.15		V	I_{OH} = -5mA
			V_{DD}+0.15	V_{DD}+0.5		I_{OH} = 5mA
V_{IL}	Input Low Voltage, All Inputs			0.8	V	
V_{IH}	Input High Voltage, All Inputs	2.0			V	
I_{DD}	Supply Current		1.0	2.0	mA	f = 0MHz; V_{DD}=13.2V, $V_{IN} \leq 0.4V$ or $V_{IN} \geq 2.4V$, C_L = 0.
I_{DD1}	Supply Current		12	20	mA	f = 1MHz (See Figure 15b); V_{DD}=13.2V, $V_{IN} \leq 0.4V$ or $V_{IN} \geq 2.4V$, C_L = 0.

Note 1: Typical values are at 25°C and nominal voltage.

Table XIV. 5234 A.C. Characteristics

T_A = 0°C to 70°C, V_{DD} = ±5%.

Symbol	Parameter	Min.[1]	Typ.[2,4]	Max.[3]	Unit	Test Conditions
t_{-+}	Input to Output Delay	20	45		ns	R_{SERIES} = 0
t_{DR}	Delay Plus Rise Time		70	100	ns	R_{SERIES} = 0
t_{+-}	Input to Output Delay	20	45		ns	R_{SERIES} = 0
t_{DF}	Delay Plus Fall Time		70	100	ns	R_{SERIES} = 0
t_T	Output Transition Time	10	25	40	ns	R_{SERIES} = 0

NOTES: 1. C_L = 150pF
2. C_L = 200pF
3. C_L = 250pF
These values represent a range of total stray plus clock capacitance for nine 4K RAMs.
4. Typical values are measured at 25 C.

Table XV. 5235 A.C. Characteristics

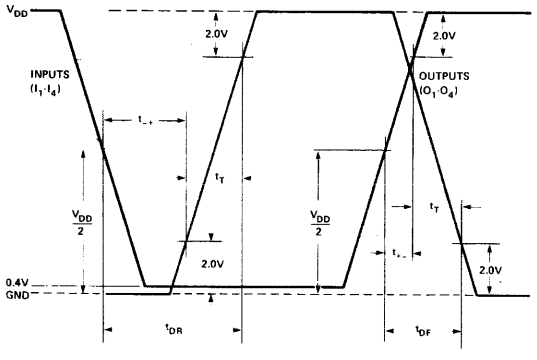
T_A = 0°C to 70°C, V_{DD} = 12V ±5%.

Symbol	Parameter	5235-1			5235			Unit	Test Conditions
		Min.[1]	Typ.[2,4]	Max.[3]	Min.[1]	Typ.[2,4]	Max.[3]		
t_{-+}	Input to Output Delay	20	55		20	70		ns	R_{SERIES} = 0
t_{DR}	Delay Plus Rise Time		75	90		95	120	ns	R_{SERIES} = 0
t_{+-}	Input to Output Delay	20	55		20	70		ns	R_{SERIES} = 0
t_{DF}	Delay Plus Fall Time		75	90		95	120	ns	R_{SERIES} = 0
t_T	Transition Time	10	20	40	10	25	40	ns	R_{SERIES} = 0

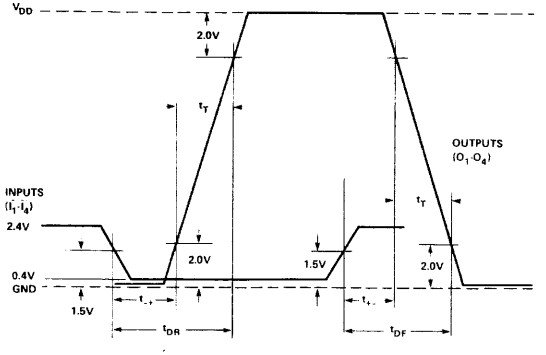
NOTES: 1. C_L = 150pF
2. C_L = 200pF
3. C_L = 250pF

These values represent a range of total stray plus clock capacitance for nine 4K RAMs.

4. Typical values are measured at 25° C, and nominal voltage.



a. 5234 Waveforms



b. 5235 Waveforms

Figure 31. CMOS Driver Waveforms

Table XVI. 5234/35 Capacitance

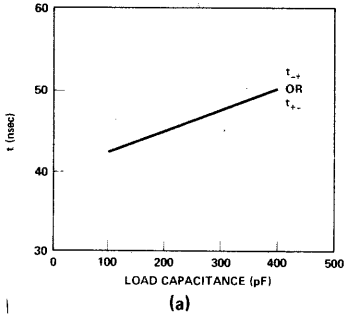
Symbol	Test	Typ.	Max.	Unit
C_{IN}	Input Capacitance	8	14	pF

As has been pointed out before, the effective device speed will vary as a function of the capacitive load which the device is driving. For determining driver speed with capacitive loads different from those mentioned in Table XIV or XV, Figure 32 or 33 can be used to find typical delays.

Because the 5234 and 5235 are implemented with CMOS technology, the power supply current will vary as a function of frequency. Figure 34 will aid in the calculation of power supply requirements, as it correlates the input frequency to I_{DD}.

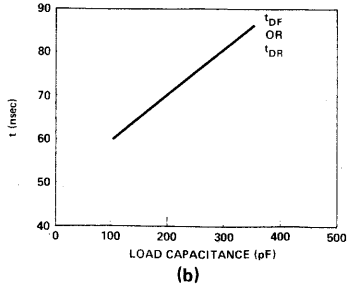
Figure 35 shows the variation in V_{IL} and V_{IH} as a function of t_{DR} and t_{DF}.

5234 INPUT TO OUTPUT DELAY VS. LOAD CAPACITANCE



(a)

5234 DELAY PLUS TRANSITION TIME VS. LOAD CAPACITANCE

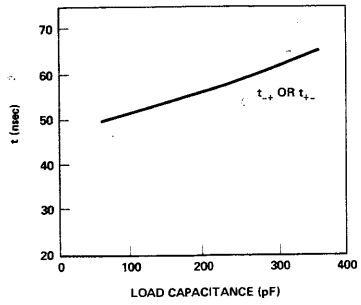


(b)

Figure 32. Output Characteristics

a.

5235 INPUT TO OUTPUT DELAY
VS. LOAD CAPACITANCE



b.

5235 DELAY PLUS TRANSITION TIME
VS. LOAD CAPACITANCE

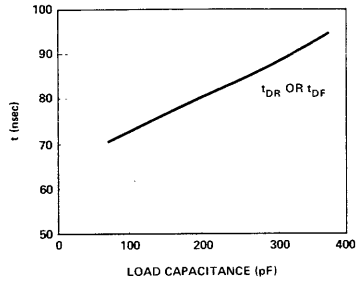
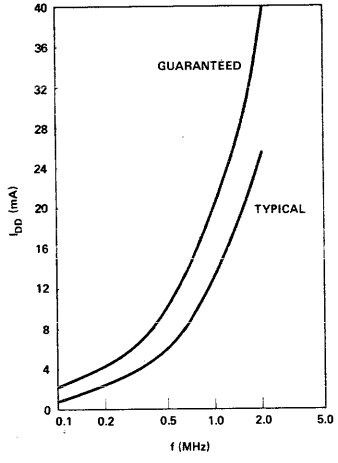


Figure 33. 5235 Delay vs. Capacitance

a.

5234 POWER SUPPLY CURRENT VS. FREQUENCY



b.

5235 POWER SUPPLY CURRENT VS. FREQUENCY

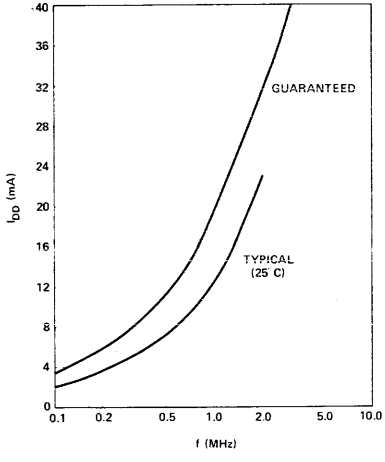
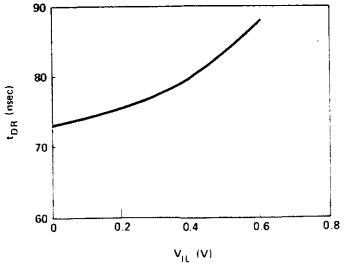


Figure 34. 5234/5235 Switching Frequency vs. I_{DD} Current

DELAY PLUS TRANSITION TIME
VS. INPUT VOLTAGE



DELAY PLUS TRANSITION TIME
VS. INPUT VOLTAGE

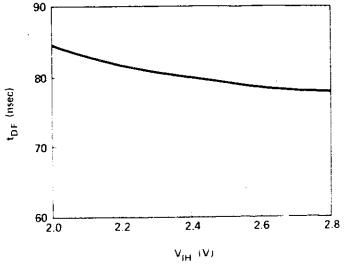


Figure 35. 5235 Delay Plus Transition Time vs. V_{IL} and V_{IH}.

SYSTEMS CONSIDERATIONS

Because MOS level drivers are used primarily to drive the timing clock on 4K RAMs, the clock drivers are subjected to more stringent requirements than TTL level drivers. These requirements are usually on driver transition time and high and low output levels. In addition, drivers for MOS level clocks should have minimum power dissipation when their output is in the low or inactive state to minimize system standby power.

A typical system configuration using the 3245 in a 2107B memory system is shown in Figure 36. Note that each driver output drives 9 devices with the drivers placed in the middle of the array. It is important to place the drivers as close as possible to the clock inputs. This minimizes adverse transmission line effects.

When several memory cards are used in a system, the drivers can be used as logic gates inhibiting those memory devices not in use. The necessary logic to perform this function is shown in Figure 36. Using this method of decoding, up to four memory cards can be accommodated in the system.

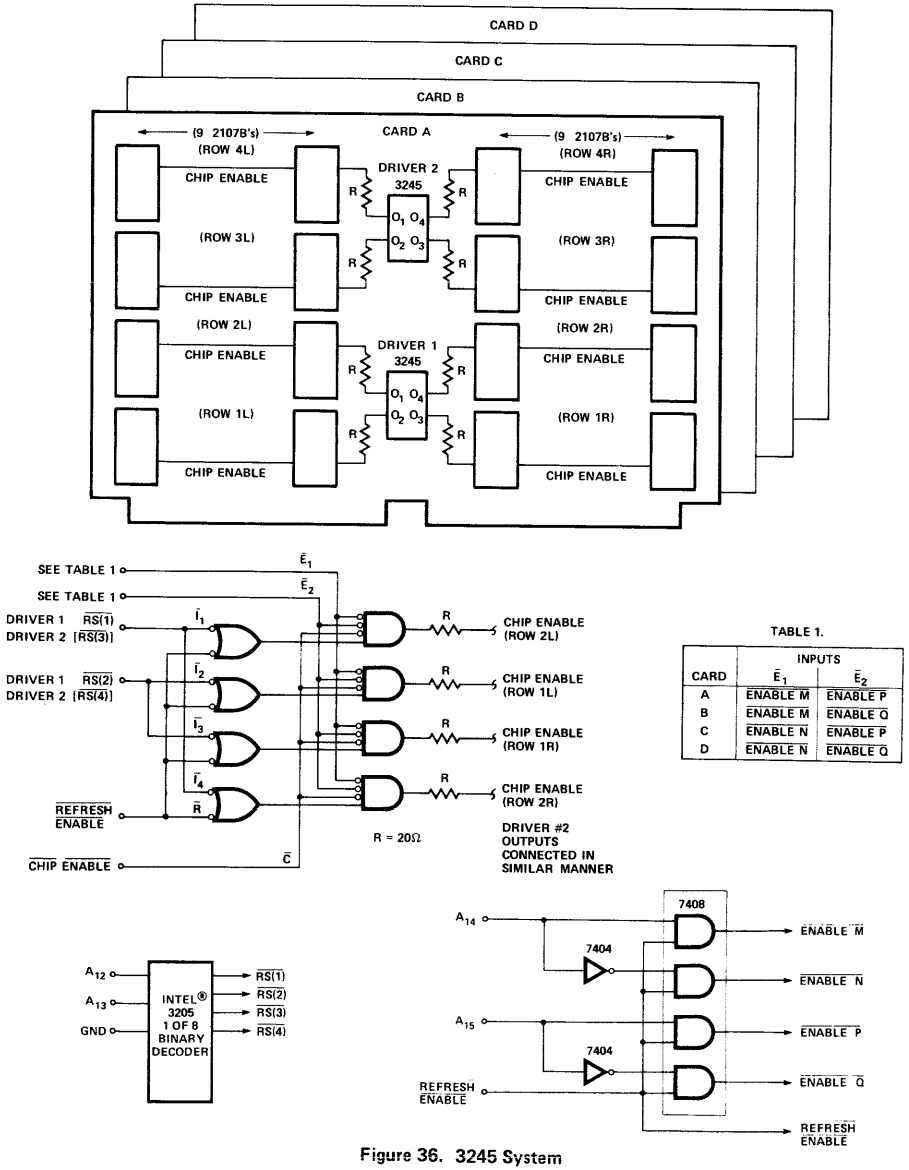


Figure 36. 3245 System

The characteristics of the MOS level waveform generated by the 3245 depends on several factors: load capacitance, transmission line characteristics, driver placement relative to memory array, etc. In most systems, it is necessary to add a series terminating resistor on the output of the driver (see Figure 36) to more closely match the characteristics of the transmission line. The effect of adding a series terminating resistor is shown in Figure 37. The two extremes of resistance (R_S = 0Ω and R_S = 51Ω) is clearly evident for a load of 250 pF. With R_S = 0Ω, the overshoot on the clock driver is excessive and will lead to marginal system operation. The over/undershoots shown will not damage MOS devices. If the series resistence is too high, the R_S = 51Ω, the effect is to significantly slow the clock transition times. Since 4K dynamic devices use the chip enable clock to initiate internal timing, the rising transistion of this external clock has a maximum limit. On the other hand, too fast a transition can introduce noise or cause marginal device operation. It is therefore necessary to control the transition time so that it is neither too fast nor too slow.

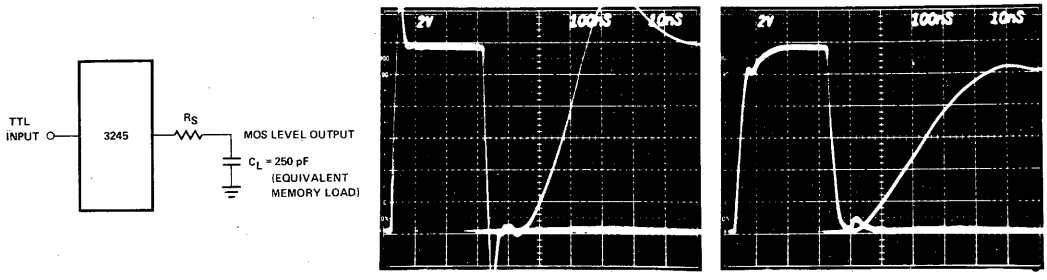


Figure 37. Effect of Series Terminating Resistor on MOS Level Driver

Table XVII. Summary of 3245 Driver Board Delay Measurements

NUMBER 2107B LOADS AND CIRCUIT CONFIGURATION		MEASURED CONDITIONS INPUT TO OUTPUT DELAY				MEASURED DELAY[3] PLUS RISE		MEASURED DELAY[4] PLUS FALL	
		t_{-+}[1]		t_{+-}[2]					
		TYP.	WORST[5] CASE	TYP.	WORST[5] CASE	TYP.	WORST[5] CASE	TYP.	WORST[5] CASE
3245 18 LOADS[6]	R = 20Ω	12	12	10	10	34	37	33	35
3245 9 LOADS	R = 20Ω	11		10		30	33[7]	25	27[7]

NOTES:

1. TTL 1.5 to V_{SS} +1 volt
2. TTL 1.5 to V_{DD} −1 volt
3. TTL 1.5 to V_{DD} −1 volt
4. TTL 1.5 to V_{SS} +1 volt
5. Worst case driver on board at 70°C and 5% power supply variation.
6. 18 loads 20Ω split resistor (see Figure 25).
7. Projected from 18 load delay.

(1)

$$P_{Total} = \frac{CV^2}{t_r} + \frac{t_{ce}}{t_{cyc}} \times P_{OH} + \frac{t_{\overline{ce}}}{t_{cyc}} \times P_{OL} + 3 \times P_{OL}$$

$$= \frac{(153)(8)^2}{20} + \frac{250}{400} \times 121 + \frac{150}{400} \times 97 +$$

3 x 97 = 892.6 MW/Cycle for 36 2107B's; 1 row of 9 Enabled

Where:

P_{TOTAL} = Total power per cycle dissipated per 3245 driver.

C = input capacitance for 9 2107B CE inputs = 17pF x 9 = 153pF.

V = $(V_{DD}-2) - (V_{SS}+2)$ = 8V.

t_r = CE transition time = 20nS.

t_{ce} = CE high time = 230nS + transition time.

$t_{\overline{ce}}$ = CE low time = 130ns + transition time.

t_{cyc} = memory cycle time = 400nS.

P_{OH} = 3245 power per driver for output high = 121mW.

P_{OL} = 3245 power per driver for output low = 97mW.

All values used are based on the 2107B system described in Section II. Nominal supply voltages and typical values were used where applicable.

The Motorola MC3460 and the National DS3644/3674 are alternate sources to the 3245.

The results of tests made on the board shown in Figure 36, of a typical 3245 driver driving 18 loads and 9 loads is shown in Table XVII. Note that the delay does not change appreciably with temperature but the transition time increased approximately 2-3 nsec from 25°C to 70°C. Calculation of driver power is shown in Equation 1.

Transmission Line Effect

The physical placement of the clock driver in close proximity to the memory array is an important design requirement. An equivalent circuit of the transmission line from the driver through the memory array is shown in Figure 38. The first section of transmission line, L, consists solely of the printed trace etch. At the memory array, the transmission line characteristics are significantly modified by the load of the chip enable inputs. While this load effects both the delay and impedance characteristics of the line, the primary effect observed by the system designer is the effect of the line impedance variation. The mismatch between the two sections of transmission lines is approximated by:

$$Z_1 = \sqrt{\frac{L}{C_1}}$$

and

$$Z_2 = \sqrt{\frac{L}{C_2}}$$

where:

Z_1, Z_2 = impedance of sections L_1 and L_2, respectively

L = per unit length inductance of line (assume constant for entire length of line)

C_1 = per unit length capacitance of L_1

C_2 = per unit length capacitance of L_2

Since the per unit length inductance is assumed constant for the transmissions line, the impedance mismatch is approximated by:

$$\frac{Z_1}{Z_2} = \sqrt{\frac{C_2}{C_1}}$$

Assuming the memory devices are on 0.5-in. centers in the array with each chip enable input typically 17 pF, C_2 is equivalent to:

$$C_2 = C_1 + 2\,(17\text{ pF}) = C_1 + 34\text{ pF/in.}$$

Therefore, the impedance ratio is:

$$\frac{Z_1}{Z_2} = \sqrt{34} = 5.8 \qquad \text{Since } C_1 \ll 34\text{ pF/in.}$$

There is, therefore, almost a 6:1 impedance difference between the two lines.

It is evident that if the clock driver is far removed from the memory array (L_1 is large) the effect of the mismatch is greatly magnified. Figure 39 shows a typical clock driver waveform. The "step" shown in the middle of the rising transition is the result of line mismatch. The severity of the "step" is a direct function of the length of segment L_1.

The placement of the MOS level clock driver close to the memory array is important to minimize ground (V_{SS}) and power supply (V_{DD}) noise. It is important to have ground traces between the memory array and MOS level drivers as short as possible. An example of an acceptable and marginal power distribution is shown in Figure 40.

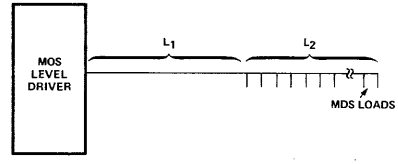


Figure 38. Typical Transmission Line on MOS Level Driver

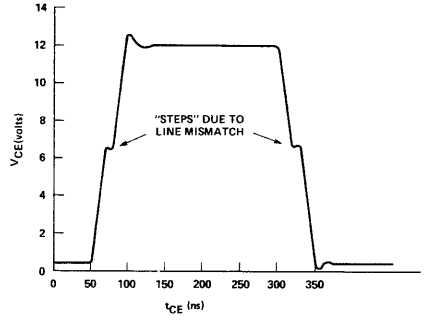


Figure 39. Effect of Transmission Line Mismatch

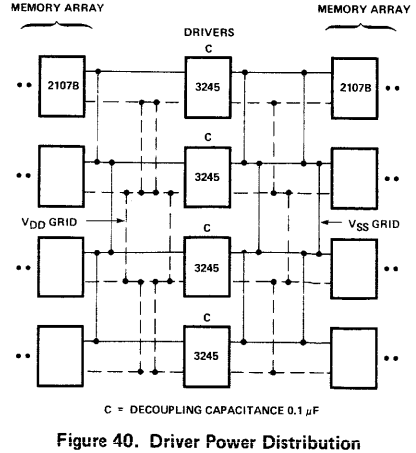


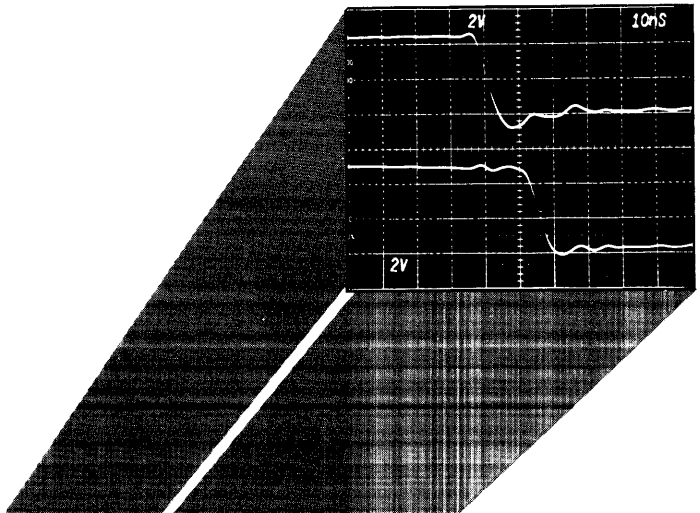
Figure 40. Driver Power Distribution

MEMORY SUPPORT CIRCUITS

	Type	Description	No. of Pins	Electrical Characteristics Over Temperature		Supplies[V]
				Input to Output Delay Max.	Power Dissipation[1] Maximum	
SCHOTTKY BIPOLAR	**3205**	1 of 8 Binary Decoder	16	18ns	350mW	+5
	3207A	Quad Bipolar to MOS Level Shifter and Driver	16	25ns	900mW	+5, +16, +19
	3207A-1	Quad Bipolar to MOS Level Shifter and Driver	16	25ns	1040mW	+5, +19, +22
	3208A	Hex Sense Amp for MOS Memories	18	20ns	600mW	+5
	3222	4K Dynamic RAM Refresh Controller	22	—	600mW	+5
	3232	4K Dynamic RAM Address Multiplexer and Refresh Counter	24	20ns	750mW	+5
	3242	16K Dynamic RAM Address Multiplexer and Refresh Counter	28	20ns	825mW	+5
	3245	Quad TTL to MOS Driver for 4K RAMs	16	32ns	388mW	+12, +5
	3404	High Speed 6-Bit Latch	16	12ns	375mW	+5
	3408A	Hex Sense Amp and Latch for MOS Memories	18	25ns	625mW	+5
CMOS	**5235**	Quad Low Power TTL to MOS Driver for 4K RAMs	16	125ns	240mW	12
	5235-1	High Speed Quad Low Power TTL to MOS Driver for 4K RAMs	16	95ns	240mW	12
	5244	Quad CCD Driver	16	90ns	1260mW	12

Note 1. Power Dissipation calculated with maximum power supply current and nominal supply voltages.

Appendix



Bipolar/MOS Static Ram Compatability

Dennis Galloway
Application Engineering

Contents

INTRODUCTION

High speed memory systems (system access in the 50 - 100nsec range) have in the past only been implemented with bipolar devices. Bipolar RAMs are generally characterized as very high speed, relatively high powered, and high bit cost devices. The speed characteristic of the bipolar device, necessary for system operation, usually outweighed the power penalty that was paid to obtain the system speed.

MOS technology is characterized as having very high bit densities, very low operating and standby power, with relatively slow access time and low bit cost, However, recent advances have now allowed bipolar speeds to be achieved and at the same time retaining MOS power dissipation with low cost.

Now, the best of both worlds, in the design of the memory system with Bipolar speeds and MOS power dissipation combined, is possible.

In new designs of memory systems, the user is able to take advantage of low power characteristic of MOS with minimum power supplies, thereby reducing overall system cost. In addition, the lower bit cost of MOS can help to reduce system costs further.

The advantage of replacing Bipolar devices with memory devices in existing designs is to reduce device costs in addition to savings on lower power requirements.

When upgrading existing systems to benefit from MOS characteristics, the user begins to realize possible potential problems in interfacing Bipolar and MOS devices simultaneously. For MOS and Bipolar to be truly compatible, not only must access and cycle timings be equal, but all intermediate timing considerations for MOS must be at least equal or better to those of the Bipolar.

In this article we will describe the operation of a static RAM memory board using both Bipolar and MOS memory devices together.

Intel's 2115A/2125A is designed to be pin for pin and timing compatible with Fairchild's 93415A/25A. We begin with a summary of the device characteristics (similarities and differences), compatibilities operating together at the board level, and summarize the various present and future possibilities of high speed MOS memory systems.

BIPOLAR/MOS SPECIFICATION SUMMARY

The specifications for Intel's 2125A and Fairchild's 93425A are similar and shown below. (Fairchild's 93425A data sheet dated 8/74.)

The Similarities:

t_{AA}	(Address Access Time)	45ns
t_{ACS}	(Chip Select Time)	30ns
t_{RCS}	(Chip Select Recovery Time)	30ns
t_{WSCS}	(Chip Select Set-Up Time)	5ns
t_{WHCS}	(Chip Select Hold Time)	5ns
t_{WSA}	(Address Set-Up Time)	5ns
t_{WHA}	(Address Hold Time)	5ns

	Differences	93425A	2125A
t_{WS}	(Write Enable Time)	30ns	25ns
t_{WSD}	(Data Set-Up Prior to Write)	0ns	-10ns
t_W	(Write Pulse Width)	35ns	30ns
I_{IL}	(Input Low Current)	-400μA	-40μA
I_{CC}	(Power Supply Current)	130mA	80mA
Power Dissipation		0.5 mW/bit	0.3mW/bit

MOS/BIPOLAR SYSTEM COMPATIBILITY

In evaluating the compatibility between MOS and Bipolar devices, it is necessary to examine the characteristics of a memory system which uses both devices on the same board, in the evaluation primary emphasis is placed on analyzing those characteristics found in the data sheet specifications which may have a negative impact on system level compatibility.

The memory system used to perform this MOS/Bipolar system compatibility is shown in Figure 1.

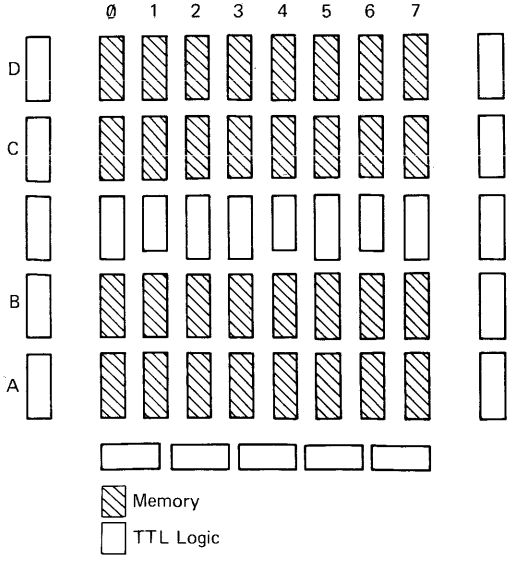


Figure 1. MOS/Bipolar Evaluation Board.

APPENDIX

The system analysis performed considers the following system related characteristics:

1) Device placement
2) Timing requirements
3) Power characteristics

Each of the above characteristics is explained as to their effect on a system in the following sections.

DEVICE PLACEMENT

The ultimate test of system level compatibility between devices is whether or not these devices can be treated as "black boxes". For MOS high speed devices to be universally accepted in new and existing systems, they must be able to replace existing bipolar at any location on the memory card. The configurations of interest are shown in Figure 2 and Figure 3.

The configurations in Figure 2 are as follows (label numbers refer to configuration shown in Figure 2):

label Number	Comments
(1)	Determines compatibility along the Dout OR tie between devices, e.g., if bipolar device turns off (or vice versa) excessive transient current will be drawn in power supply and data out line.
(2) (3)	Established to provide a "standard" for a row of MOS and bipolar during testing. Determine loading change (if any) on inputs – Particularly $\overline{CS}$.
(4)	Examines capacitive and leakage loading effects on data out line. Effects, if any, on access time are evaluated.
(5)	Determines address line capacitive and leakage loading effect. Provides information on possible system level sensitivities to either "too" fast or "too" slow address transition time effecting address valid time (for t_{AA} measurements).

Figure 3 is a configuration likely to be encountered when a MOS device is used to replace a defective bipolar device in an existing storage card. (Of course it is always possible that a MOS device will fail and have to be replaced by a bipolar device ... even that possibility is considered.)

The condition shown by label (1) Figure 2 is best analyzed by considering the circuit configuration shown in Figure 4.

Opposite data is loaded into devices (1) and (2) in Figure 4. A read operation is performed by toggling chip select as shown in Figure 4b. If the device being deselected goes to the high impedence state too slowly while the device being selected accesses data too rapidly, a large transient current spike in the data-out output will occur during the time both devices are ON. Time t_0 represents the case where a slow bipolar device may cause a transient spike while time t_1 represents the case where a slow MOS device may cause a similar spike. Photos showing these conditions as a function of $\overline{CS}$, $\overline{CS}_2$ overlap are shown in Figure 5.

The width and height of the current spike are a function of the amount of overlap of the respective $\overline{CS}$. Normal system timing requirements should be such that neither device is turned ON (or OFF) while the neighbor device, on the data-out line is still active.

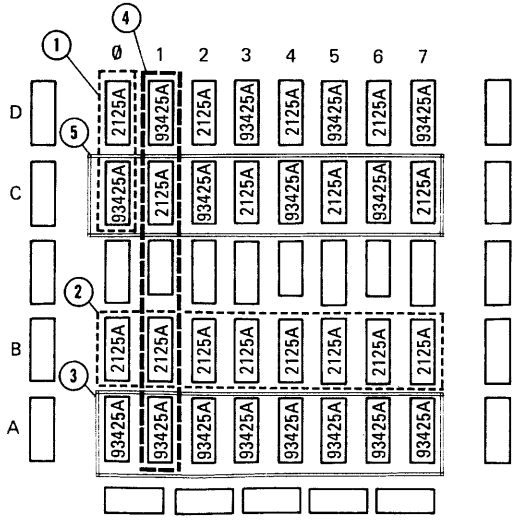


Figure 2. MOS/Bipolar Evaluation Board Population.

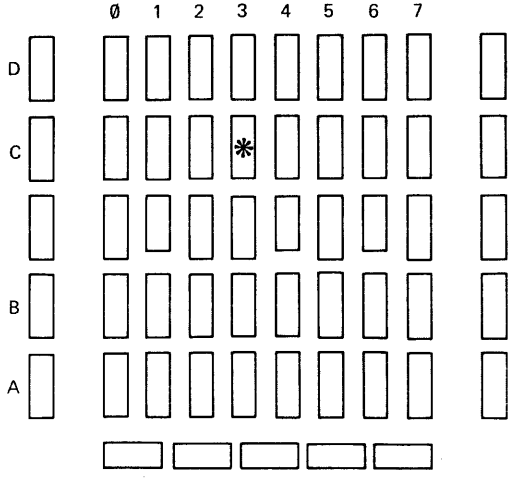
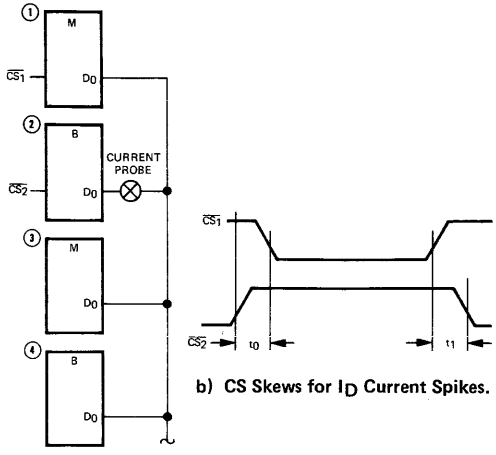


Figure 3. Isolated MOS Device On Bipolar Storage Card.

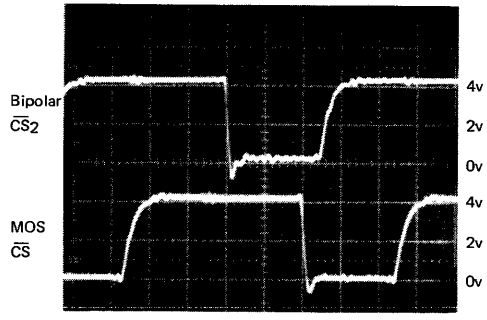
APPENDIX



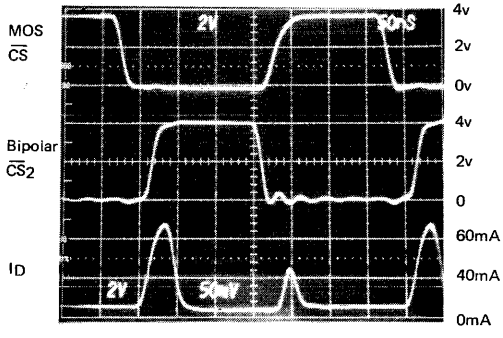
a) Current Probe Location for I_D Spike.

b) CS Skews for I_D Current Spikes.

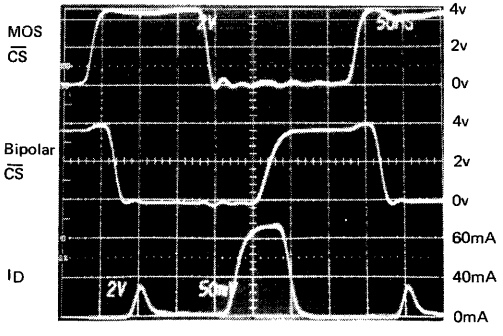
Figure 4. I_D Circuit Configuration for Measurement.



a) Bipolar /MOS $\overline{CS}$ With Bipolar Turning Off Late.



b) Bipolar /MOS Data Out Current Spike.



c) Bipolar /MOS Data Out Current Spike.

Figure 5. Bipolar OFF/MOS ON Current Transients.

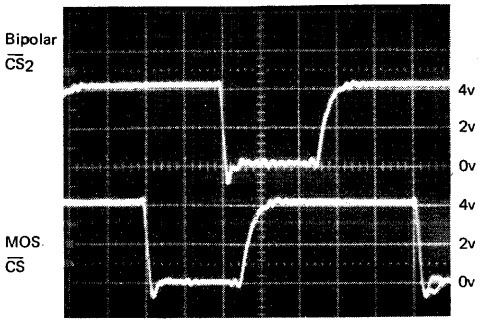
However, when the system timing is designed such that a row is deselected at the same time another row is selected, the designer must assure himself that the current spike generated is not excessive. The photos shown in Figures 5 and 6 illustrate these conditions. Figure 5a, b, c, show the condition for a bipolar device turning OFF while a MOS device is turning ON. The transient current through the data out buffers is shown in Figures 5b and c for different deselection times. It is important to note that for deselection times shown it makes no difference whether or not the devices used are all bipolar, all MOS, or a mixture of the two. The transient spike shown is similar for all three conditions.

Figures 6a, b, and c show the condition for a MOS device turning OFF while a bipolar device is turning ON. The transient spikes shown are again independent of the use of bipolar, MOS, or a combination of devices.

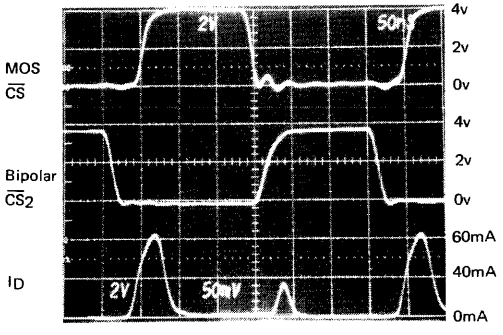
The analysis and photos showing the effect on the data-out line between MOS and bipolar devices has demonstrated their compatibility in a data out OR tie condition. Subsequent analysis of timing parameters will show that, as far as system timing is concerned, there is no difference between MOS and bipolar (both are equally fast).

LOADING EFFECTS

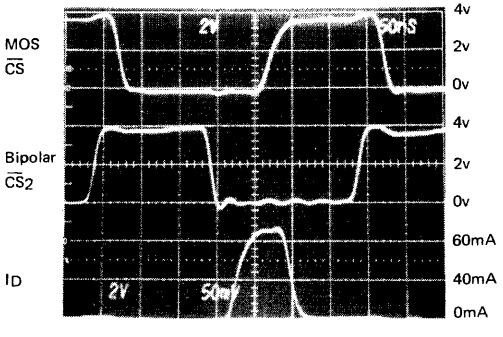
There are two basic loading effects to be considered: "horizontal" and "vertical". A horizontal loading effect refers to a typical printed circuit board layout where the address $\overline{CS}$ and write enable lines are distributed horizontally. The "vertical loading effect is along the data in and data out directions; usually laid out vertically.



a) Bipolar /MOS $\overline{CS}$ With MOS Turning Off Late.



b) Bipolar /MOS Data Out Current Spike.



c) Bipolar /MOS Data Out Current Spike.

Figure 6. MOS OFF/Bipolar ON Current Transients.

The horizontal loading effects and changes (if any) between MOS and bipolar are demonstrated by configurations 2 and 3 in Figure 2. $\overline{CS}$ is chosen to show this effect. If the capacitance loading of $\overline{CS}$ is significantly different between MOS and bipolar, than a difference in the $\overline{CS}$ waveform would be expected to occur. Figure 7 shows the $\overline{CS}$ waveform for a row of all MOS and a row of all bipolar devices. From this figure, it is evident that the capacitive loading effect of MOS and bipolar are comparable. However, due to the higher loading currents, the low level input can be expected to be typically higher for bipolar than for MOS on the inputs. The noise margin for a bipolar system is therefore, somewhat reduced from that of a MOS system. Configuration 4 in Figure 2 considers the differences (if any) in the loading effects of OR tieing data out lines. The primary difference due to capacitance loading would be a change in access time due to this loading. Specifications for both bipolar and MOS devices indicate comparable capacitive loads. The effect of these two devices on each other in a system environment, does not impair the system.

TIMING REQUIREMENTS

When considering device specifications for a memory board, one of the most critical aspects is timing. If changes to the timing were required, when changing to MOS from bipolar (even with the same access time) device compatibility could not be claimed.

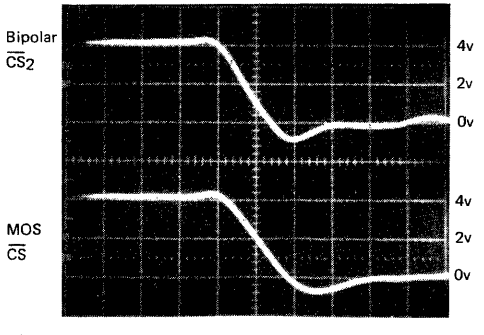


Figure 7. Bipolar /MOS $\overline{CS}$ Accessing Two Rows Simultaneously.

Selected plots showing critical timing parameter tested for different device configurations on a board is shown in Figure 8. As is shown in these figures, both MOS and bipolar are well within worst case device specifications over temperature and voltage.

POWER CHARACTERISTICS

The use of the 2115A/2125A in a high speed memory system replacing bipolar devices causes no change in system characteristics .... except one. That of course is power dissipated in the system. The 2115A/2125A devices are much lower in power than their bipolar counterparts. Table 1 summarizes the system level power when using all bipolar and all MOS devices. Reducing power, of course, reduces system operating temperature. This reduction in operating temperature improves semiconductor reliability. Equally important to lowering temperature is that lower power results in lower power supply costs.

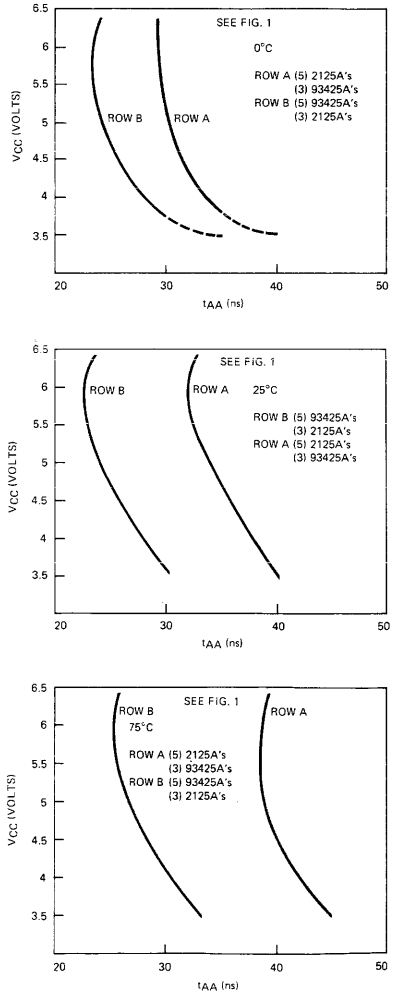


Figure 8. V_{CC} vs t_{AA} for Various Temperatures.

Table I. MOS/Bipolar Power Dissipation.

Device	Pwr/bit	Total bits	Total/Pwr
93425A	0.5mW	32,768	16.384watts
2125A	0.3mW	32,758	9.830watts

SUMMARY

The compatibility between the 2115A/2125A and the 93425A family has been demonstrated. The designer now has the opportunity to achieve very high speed operation and simultaneously achieve low memory system power dissipation.

Enter the 16,384-bit RAM

The densest-yet random-access-memory chip has a two-level cell structure, plus a 16-pin package that can slip straight into a 4-k socket

by Jim E. Coe and William G. Oldham, *Intel Corp., Santa Clara, Calif.*

☐ A triumph of semiconductor device technology, the 16,384-bit random-access memory has arrived. Its bit density is unprecedented and springs from an enhanced n-channel silicon-gate technique, in which a double level of polysilicon conductors shrinks the memory cell to 450 micrometers square. That's less than half the cell size in the densest 4,096-bit RAM.

The achievement is the latest in a long line of achievements that have doubled memory-chip bit density virtually every year since 1969 (Fig. 1). That year witnessed the arrival of Intel's 1101 256-bit p-channel RAM. Then came the three-transistor cell of the p-channel 1103, adopted by industry as its 1,024-bit standard, and most recently the silicon-gate process produced the one-transistor-cell n-channel 4-k RAM.

As for memory costs, the 16-k RAM promises to cut them dramatically. Compared to present 4-k designs, the 16-k device offers the designer four times as much memory at no increase in equivalent system costs. An example of a 1-million-bit memory system built around 16-k RAMs is shown below: 64 packages, plus all the required peripheral circuitry, fit on a board of the size that today accommodates only a quarter of a million bits of 4-k RAM. And to judge by previous experience, which indicates at least a two-to-one cost savings as each new device generation matures, the 16-k system will become even more attractive.

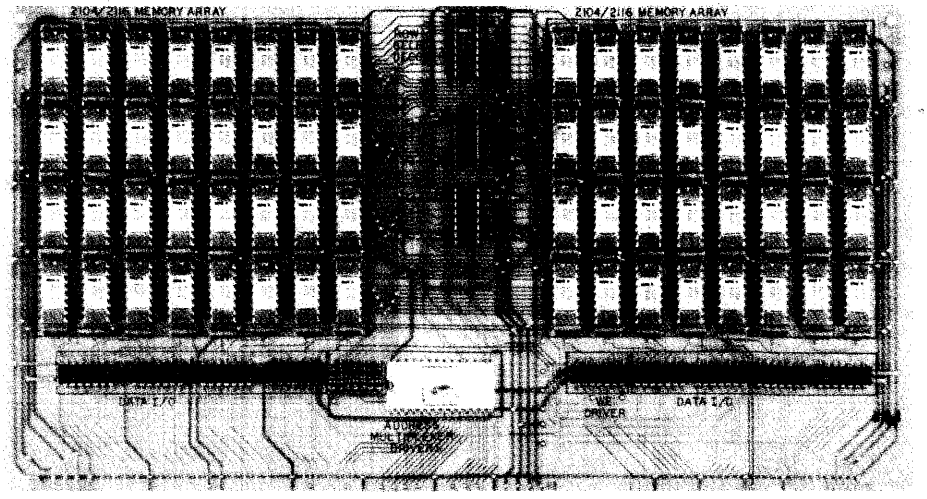
Moreover, system specialists can expect the 16-k technology to mature much faster than did the 4-k RAM technology. The new chip is an extension of, rather than a radical departure from, the n-channel process used in today's standard 4-k devices. Even its most innovative feature—the double polysilicon level—is borrowed from charge-coupled block-memory designs that are already in production. So a high degree of 16-k reliability should build up quickly.

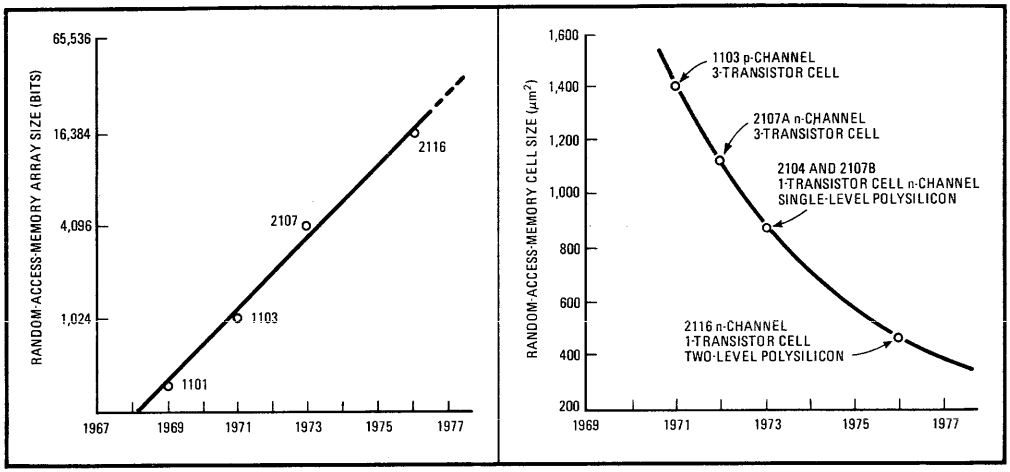
Why the cell shrinks

Basically, there are two elements in a one-transistor cell: the storage capacitor, which holds the charge quantity appropriate to a logic 1 or 0, and the transistor itself, which acts as a switch, dumping the capacitor's charge onto the bit sense line for sensing. In the cell of a 4-k RAM (Fig. 2a), transistor and capacitor sit side by side in the same plane, and a single level of polysilicon is used both as an interconnection and as one capacitor element. Clearly, space could be saved if the capacitor sat under the transistor and a second level of polysilicon made the interconnection.

That's what's done in the cell of the 16-k RAM (Fig.

Four times the memory. Intel's new 16,384-bit random-access-memory chip, the 2116, packs 1 million bits onto a memory board of the size that now holds 250,000 bits of 4,096-bit RAM. The two 16-pin RAM chips are pin-compatible. Board is organized as 64,000 16-bit words.





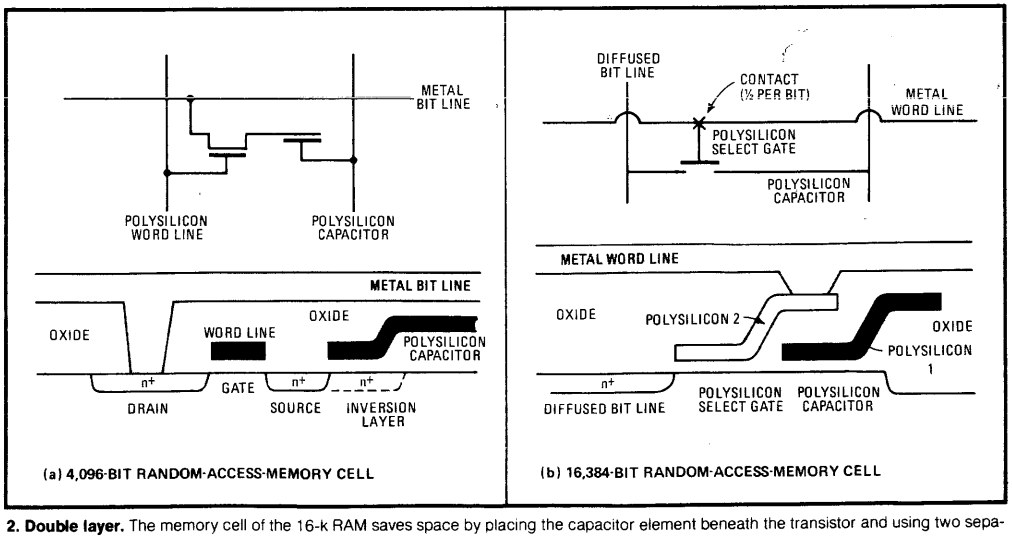
1. Onward and upward. Borne along by an evolutionary MOS technology, RAMs have increased their bit density by almost five orders of magnitude since 1969. The first p-channel three-transistor cell has developed into today's double-polysilicon one-transistor n-MOS cell.

2b). The first polysilicon layer serves as one capacitor element, while the second serves as the gate contact and interconnection. Since a diffused region (transistor source) is no longer needed between gate and capacitor, still more space is saved. What's more, the cell even operates more efficiently because a diffused bit-sense line can be used rather than a deposited metal one, which has higher parasitic capacitance. The entire cell squeezes into an area that is only about 450 micrometers square, or about half the area occupied by the 4-k RAM's cell (Fig. 3).

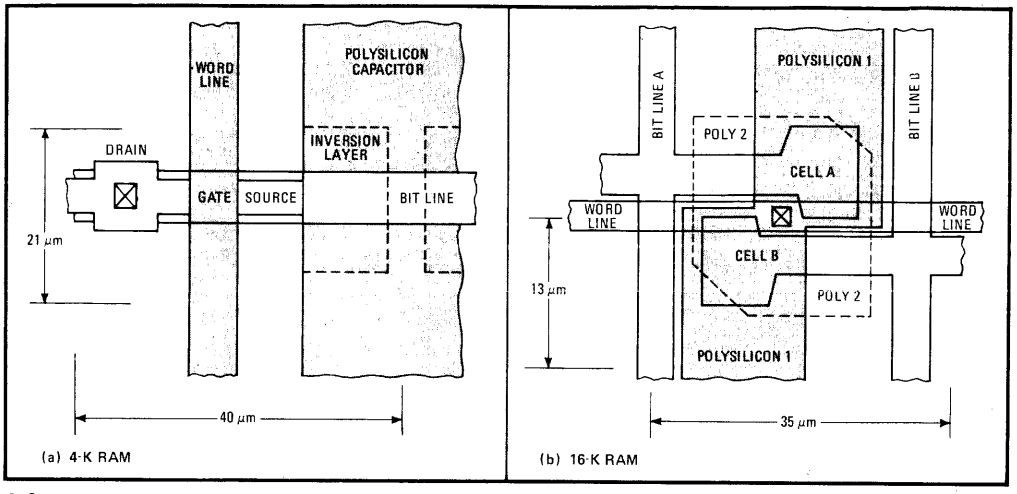
A side result of the smaller cell is that the storage capacitor in the 16-k cell has about half the capacitance of the 4-k cell. Actual figures are 0.03 picofarad as against 0.07 pF. This could result in smaller bit-sense-line signals to the sense amplifier if it weren't for the fact that the 16-k cells are both smaller and closer together than in the 4-k RAM. This tightened geometry reduces the per-cell parasitic capacitance of the bit line still further and compensates for the lower cell capacitance. The 16-k RAM therefore presents its sense amplifiers with differential signals of about 200 millivolts—no smaller than those found in the 4-k RAM.

Designing the 16-k chip

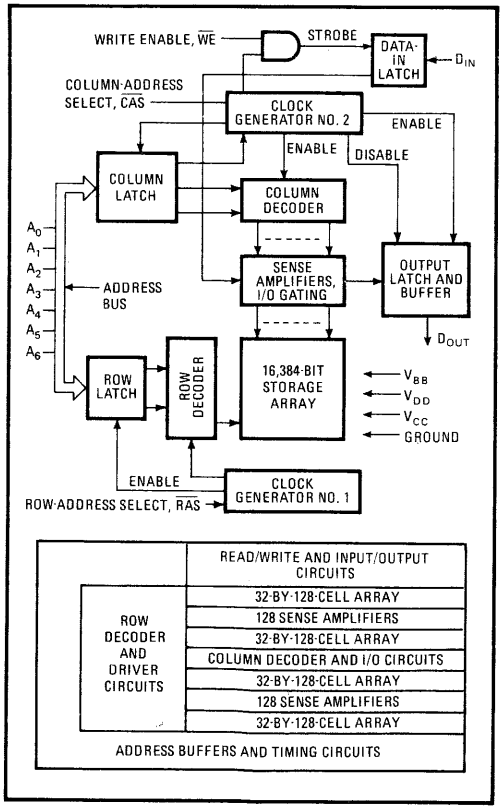
The Intel 2116 RAM uses the kind of double-level polysilicon cell just described. Although a 16,384-word-by-1-bit RAM could have fitted in a 20- or 22-pin pack-



2. Double layer. The memory cell of the 16-k RAM saves space by placing the capacitor element beneath the transistor and using two separate polysilicon interconnections. In 4-k RAMs, a single polysilicon layer serves both transistor and capacitor, which are on the same plane.



3. Compact layout. Thanks to its two levels of polysilicon, the 16-k cell occupies half the area of a 4-k cell with its single level. The 16-k cell needs only 450 square micrometers and has about 0.03 pF of capacitance, but still presents a 200-mV data signal to the sense amplifier.



4. Organization. The 2116 chip is laid out as two 8,192-bit RAMs sharing a column decoder. Each 8-k RAM consists of two balanced 32-by-128-bit arrays sharing 128 sense amplifiers. Address A_6 selects the top or bottom 8-k half, leaving the other half inactive.

age, the 2116 was chosen to be compatible with existing 16-pin 4-k RAMs. This configuration affords greatest memory density and lowest package cost. For instance, like the 16-pin 4-k, the 16-k's address lines are multiplexed. But that is now standard practice for users of 4-k 16-pin devices, such as Intel's 2104. Fourteen addresses are multiplexed on seven of the 2116's pins, with the seventh address pin obtained by eliminating the chip-select input used on the 2104.

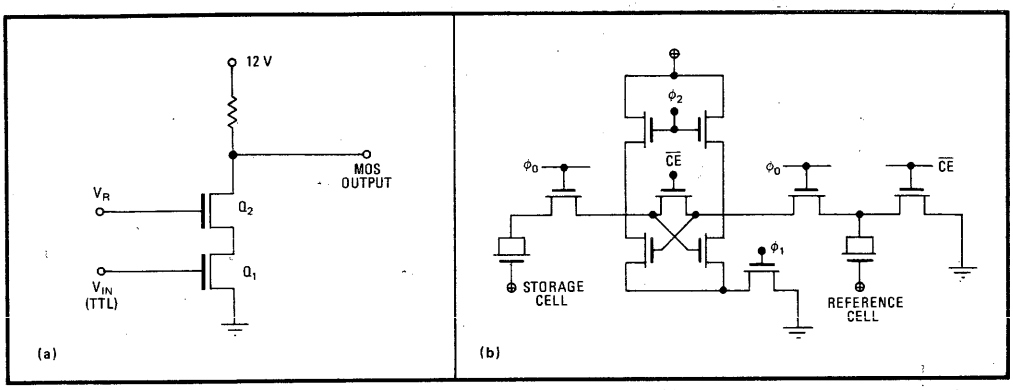
The block diagram and chart of Fig. 4 explain the organization of the 2116. The chip is arranged as two 8-k RAMs sharing a column decoder. Each 8-k RAM is organized as two balanced 32-by-128-bit arrays, sharing 128 sense amplifiers. In normal operation, address A_6 selects the top or bottom 8-k half, and the other 8-k half is kept inactive to conserve power.

Like the 4-k RAM, the 2116 generates all clock signals internally. A static input buffer converts the TTL level of the row address select, $\overline{RAS}$ to MOS levels (Fig. 5a). To reduce the effect of the large capacitance associated with the drain of the input device Q_1, a transistor operating in a common-gate configuration (Q_2) is inserted between the MOS output and the drain of Q_1. This scheme permits fairly high buffer speed with minimal standby power consumption—typically, 40 ns delay with 1-milliampere standby.

Sensing the small signal

Shown in Fig. 5 is a schematic of the data sense amplifier. Its design is key to the proper operation of a 16-k device. It must detect the small, 200-mV signals read out from the cell, and it must also keep power consumption low—after all, there are 256 such amplifiers on the chip and large unit power dissipation would be disastrous.

In order to pick up the small signals, the otherwise straightforward flip-flop sense amplifier incorporates a reference cell. In order to reduce the power consumption, the load devices of the sense amplifier switch off after information has been written into or restored to

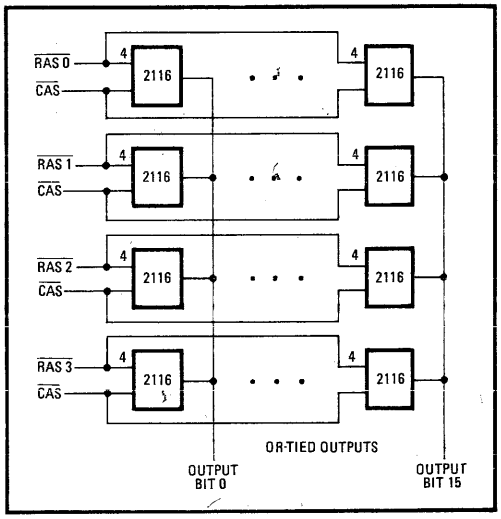


5. The periphery. The static buffer (a) converts TTL column select signals to higher MOS levels. To sense low-level data, a reference cell teams up with a flip-flop sense amplifier (b). To save power, load devices switch off when sense amplifier is idle.

the cell. The load devices also serve to precharge the bit line, to minimize device count and input capacitance.

The 16,384 memory cells of the 2116 could increase the overhead time needed to refresh the memory. To minimize this overhead, the 2116 organization is modified in the refresh mode. The refresh signal is multiplexed on the column-address-select signal $\overline{CAS}$ (Fig. 4). That is, if $\overline{CAS}$ is valid at the leading edge of the row-address-select signal $\overline{RAS}$, it's recognized as a refresh operation. The output then goes to the high-impedance state, A_6 is ignored, and all cells on the word line selected by A_0 to A_5 are refreshed in both 8-k halves of the RAM. Only 64 refresh cycles are therefore required to refresh the entire memory. (The various refresh modes available with the 2116 are discussed in detail later.)

As for device characteristics and performance, the 2116 operates from standard dynamic-RAM power-supplies (+12 volt, +5 V, and -5 V) over an ambient temperature range of 0°C to 70°C. All its input and output signals, including its two clocks, are TTL-compatible. Its three speed ranges are identical with those of 4-k RAMs like the 2104: maximum access times are 250, 300, or 350 ns, and read/write cycle times are 375, 425, or 500 ns. Typical operating power is less than 700 milliwatts, and typical standby power is less than 12 mW.



6. Power cut. This 64-k-by-16 word system has OR-tied outputs—a good way to save power in 16-pin random-access-memory designs that use more than 4,096 words. Row-address-select pin is used instead of chip-select pin to select devices.

The upwardly mobile system design

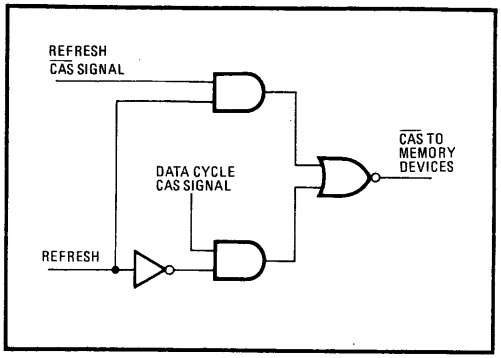
Because the 2116 fits the same socket as the 2104 and other 16-pin 4-k RAMs, an engineer can design a system around the 4-k device for later, easy upgrading into one based on the 16-k device. His reward then will be a quadrupled bit density.

The compatibility between the two memory chips depends on making the 2104's chip-select input the equivalent of the seventh multiplexed address input (A_6) of the 2116 device (Fig. 4). Since in the 16-k part each address input pin is used twice in the multiplexed address mode, the single new address input yields the additional two bits required to address 16,384 bits rather than 4,096 bits.

However, the fact that the chip-select pin on the 4-k RAM will later be used for address A_6 on the 16-k RAM changes the system design rules. For device selection, it's now preferable to use the row-address select ($\overline{RAS}$) instead of chip select ($\overline{CS}$). It's done by applying $\overline{RAS}$ only to selected 2104/2116 devices while the column-address signal is applied to all devices.

Figure 6 illustrates this arrangement in a 64-k-by-16-bit system with OR-tied outputs. The same design is used in the photograph of the 1-megabit board on page 116. In fact, the configuration is already in most 16-pin 4-k RAM system designs of greater than 4,096 words. Its advantage is substantial power savings over system designs that employ the chip-select pin for the job of device selection.

However, if a designer wants to use $\overline{CS}$ for device selection in his 4-k/16-k design, then the chip-select line should be distributed to all devices and terminated so



7. Keeping in time. An OR function in the column-address logic prevents refresh cycle timing from conflicting with data cycle timing. It guarantees that the column-address signals will always occur before the row-address signals for refresh and after them for data.

that it can serve as an address line when needed. He can do that in the 4-k design by connecting the chip-select line to a signal driver. That forces $\overline{CS}$ to a high level (V_{IH}) during column-address hold time (t_{AH}) during refresh cycles, and to a low level (V_{IL}) during data cycles. Later, when he substitutes the 2116 for the 2104 in his upgraded design, the chip-select line becomes the A_6 line and is properly jumpered to an address driver.

A refreshing difference

In refreshing a 4-k/16-k system, a designer has even more leeway than in refreshing a straight 4-k system. Two refresh modes are available with the 2116: 128-cycle and 64-cycle refresh, each taking 2 milliseconds. Any 2104/2116 designs which employ 128-cycle refresh should provide for a 7-bit refresh address counter and a three-wide, 7-bit address multiplexer. Both are needed for the 16-k system, although only 6 bits are used with the 4-k system.

The designer can choose from two timing conditions for the 128-cycle refresh: a read-cycle and a row-address-select-only timing condition. Read-cycle timing is recommended when only one row of the 2116 devices is used—16-k words by n bits. But if two or more rows of RAMs are used with OR-tied outputs, as on the 1-megabit board, read-cycle timing is not recommended unless each row of RAMs can be refreshed separately. Refreshing all rows simultaneously could turn on all the OR-tied outputs at the same time, causing the output buffers to conflict. For instance one output might be high while three are low, and so on.

This condition will not degrade the device outputs. Data out is not normally expected to be valid during refresh cycles. The problem is that it increases the current drawn from the V_{CC} supply and may result in supply noise that can affect the TTL in the system.

For an OR-tied output system it's better to use the second 128-cycle refresh timing condition, the row-address-select-only timing. $\overline{RAS}$-only timing is when the 2116 receives $\overline{RAS}$ but no $\overline{CAS}$ during a cycle. In this mode, the data stored in the addressed row of 128 cells will be refreshed, but the data output will not change.

Suppose two or more RAMs were OR-tied at the outputs. Then the RAM that had last performed a data cycle (i.e. received both a $\overline{RAS}$ and $\overline{CAS}$ input) would remain with its output buffer turned on (high or low), while the remaining RAMs would have their outputs in a high impedance state. This obviates data output buffer conflicts and their associated power-supply noise for systems above the 16-kiloword level. In addition, output data from RAMs accessed prior to refresh is valid during and after the refresh cycle.

Maximizing memory availability

The second refresh mode of the 2116 requires only 64 refresh cycles every 2 milliseconds instead of 128 cycles. This mode simultaneously refreshes corresponding rows in each half of the 2116. To the system designer, it increases memory availability, making it equal to that of a 4-k RAM's. For instance, for a 500-ns refresh/data cycle time (t_{cyc}) and a 2-ms refresh period (t_{ref}), 64-cycle refresh yields a percent availability of (t_{ref} - 64 t_{cyc})/t_{ref}, or 98.4%. In contrast, 16-k RAMs refreshed in 128 cycles have only 96.8% availability, which could be a reason for avoiding this mode in a high-throughput memory.

The timing requirements for 64-cycle refresh are hardly more complex than for 128-cycle refresh. The important thing is to assure that the column-address-select signal is valid (low) at the leading edge of the row-address-select signal and remains valid during address hold time, just like refresh addresses. Under these conditions, the A_6 address input pin on the 2116 is ignored, and the data output buffer is set to the high-impedance state. Consequently, no conflict can occur in this mode between data outputs since they are at high impedance during and following the 64-cycle refresh operation.

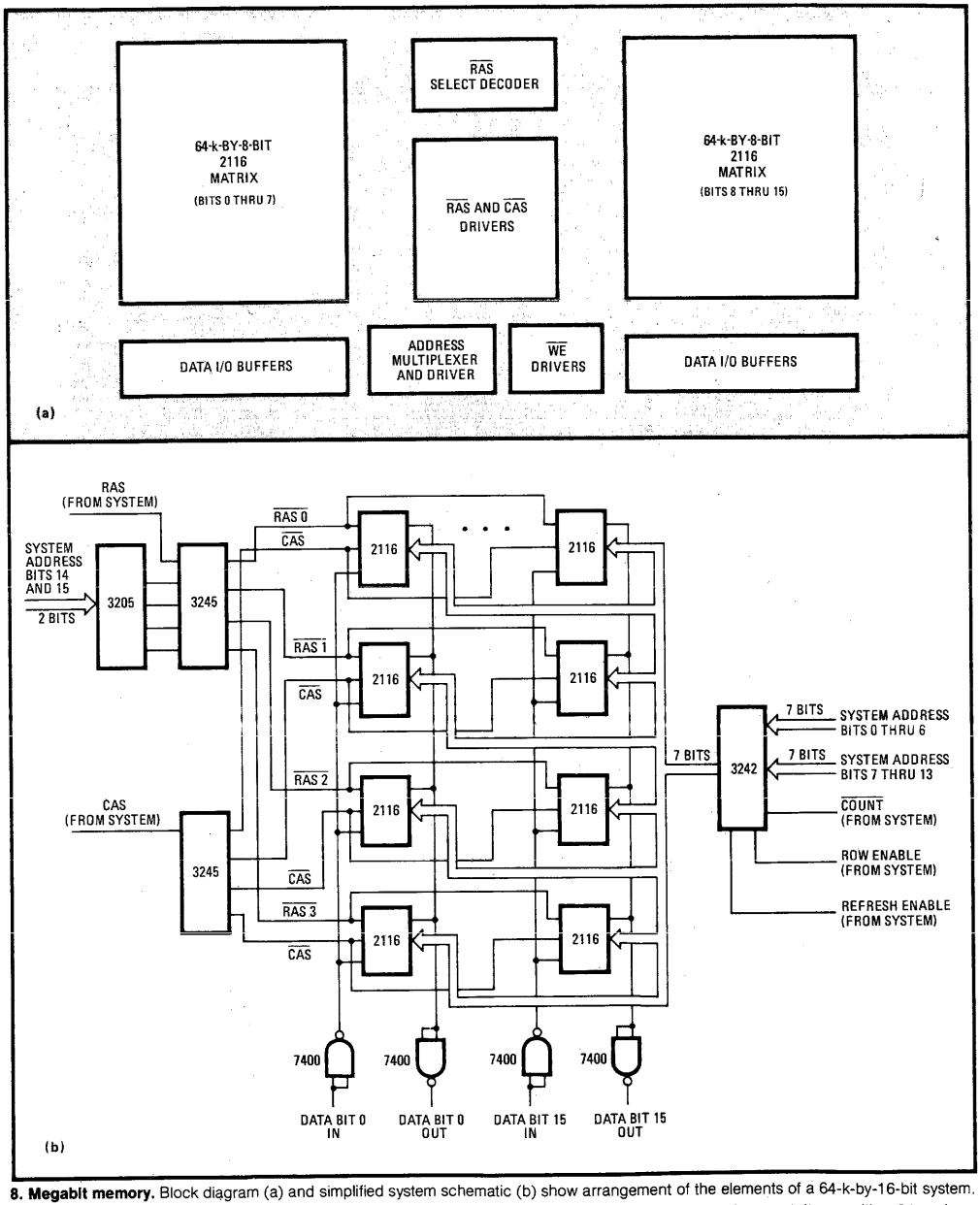
The high-impedance output state in the refresh mode also benefits standby power consumption, always a major concern of the system designer. As in 4-k RAMs, the 2116's standby current is 2 mA maximum, and as in system designs based on 4-k RAMs, this low level is obtained only when the device is deselected (that is, when its data output is in the high-impedance state). If data output is active (high or low), then the standby current is typically 3 mA.

Once the timing is worked out, the 2104/2116 system designer should consider incorporating an OR function (Fig. 7) in his column-address-select logic, such that $\overline{CAS}$ can be made to occur prior to row-address select for refresh or after $\overline{RAS}$ (delayed by the refresh cycle time, t_{cyc}) for data cycles. By so doing, he will guarantee that the refresh cycle timing will not clash with the data cycle timing.

At last, the 1-megabit memory system

To evaluate the 2116 in a system environment, Intel's applications group built the 1-megabit unit pictured on page 116. Figure 8 shows its block program (a) and a schematic (b). The system, which has been undergoing testing since June 1975, is arranged as 64-k 16-bit words and uses either 64- or 128-cycle refresh modes.

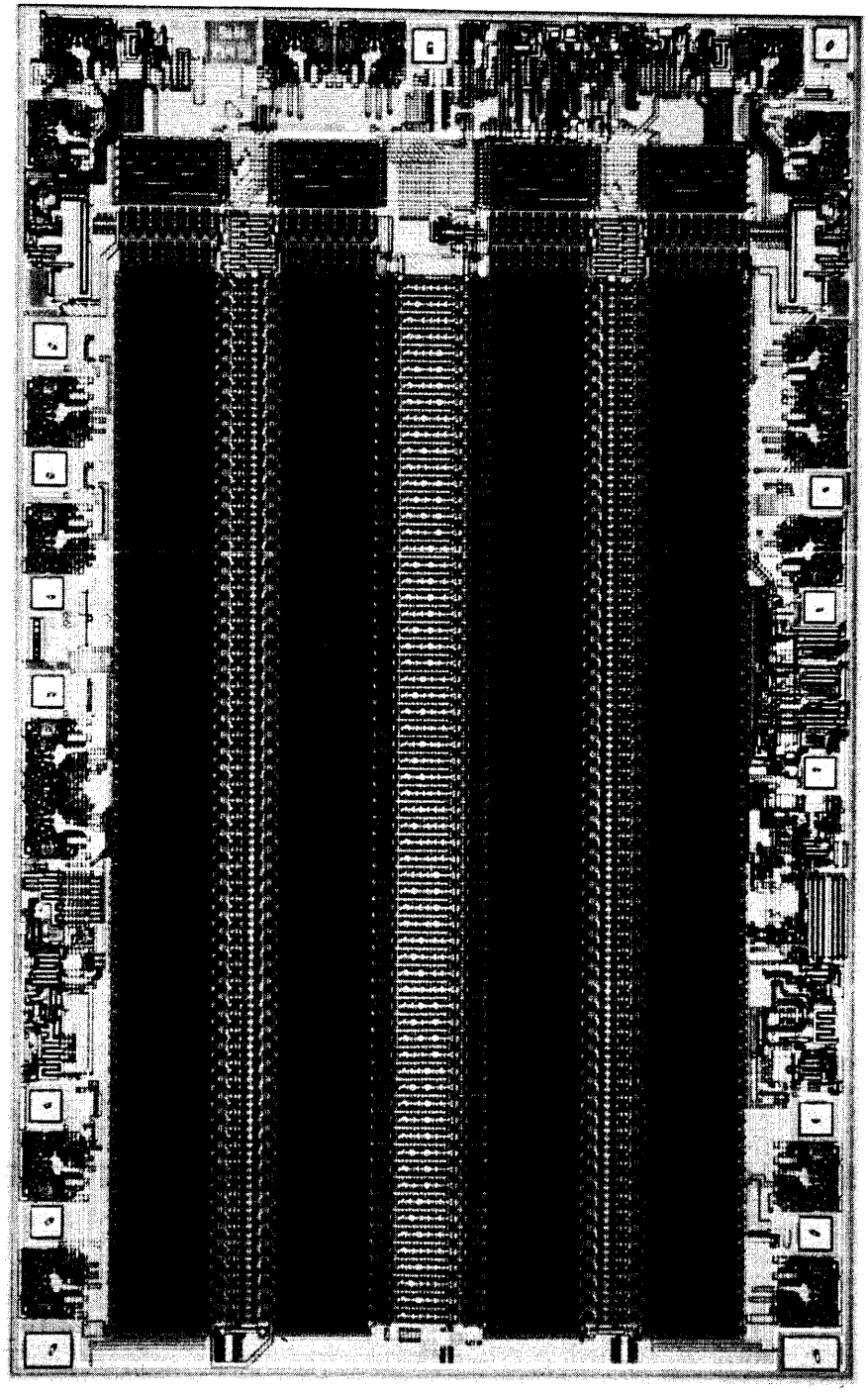
A key peripheral chip in the setup has been especially designed for 16-k RAM systems. The Intel 3242 serves as the address multiplexer and refresh address counter



8. Megabit memory. Block diagram (a) and simplified system schematic (b) show arrangement of the elements of a 64-k-by-16-bit system. This setup, which contains over 1 million bits of memory, has been operated successfully in a system environment. It uses either 64-cycle or 128-cycle refresh modes. The 64-cycle option maximizes memory availability in systems that need high throughput.

and is a TTL, single-supply (+5-V) device that comes in a 28-pin package. It multiplexes 14 bits of externally supplied system address plus the 7-bit refresh address from the internal-refresh address counter to the seven-output address pins.

The 3242 also includes an internal zero-detection circuit to indicate when the refresh address is all zeroes. This saves logic and board space by allowing users of "burst mode" refresh to determine when the burst is complete without having to count the refresh cycles. □



WHICH WAY FOR 16K?

The engineers who struggled through the pin-out confusion (16, 18 or 22 pin) on the 4K Random Access Memories (RAMs) and very adamantly protested the lack of pinout standardization among manufacturers have gotten their wish with the 16K RAMs, almost.

The 16K RAMs are all in 16-pin packages, have the same pinout, are TTL compatible, with multiplexed addresses, two clocks, and basic operation like the 16-pin 4K RAMs. There are differences with respect to refresh modes and data output operation but these variations do not preclude a system design which will accept all of the devices.

A FRESH APPROACH TO REFRESH

One of the most requested features Intel encountered during the market research efforts that led to the 2116 definition was the ability to refresh the data cell matrix with only 64 cycles. With this in mind, Intel implemented the 2116 in such a manner that both 64 cycle and 128 cycle refresh modes are available and the user has the option as to which mode best suits his system needs. Figure 1 shows that the 2116 is really two 8K x 1-bit RAMs sharing some common circuits. In normal data operations (Read, Write, etc.) the seventh address bit, A_6, is decoded and selects only one 8K half to be powered up during any given cycle.

64-Cycle Mode

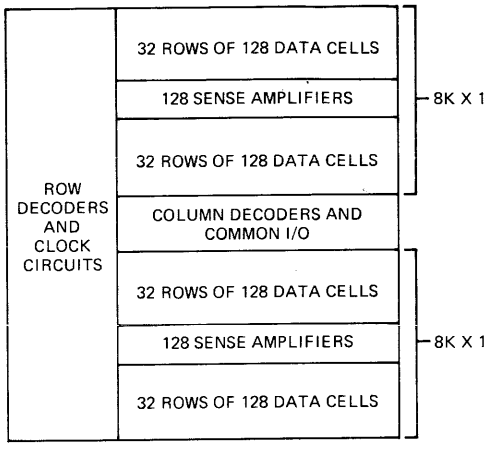
The $\overline{CAS}$-before-$\overline{RAS}$ 64 cycle refresh mode operates by disabling the common I/O circuitry shown in Figure 1a and refreshing one row in both 8K x 1-bit halves of the 2116. Since there are 64 rows in each 8K half and one row in each half is refreshed each cycle, only 64 refresh cycles are required.

128-Cycle Modes

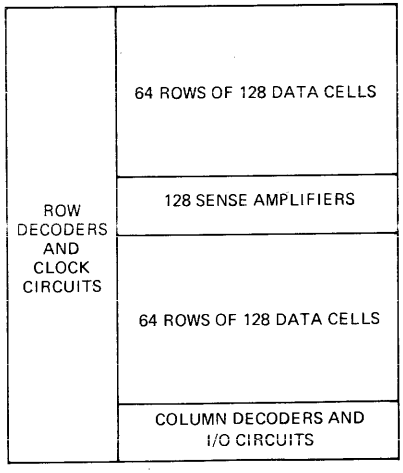
During Read/Refresh and $\overline{RAS}$-only refresh cycles, only one 8K x 1-bit half of the 2116 is activated and one of the 64 rows in the active section is refreshed. Thus 128 cycles are required to refresh the 128 rows of cells (64 rows in each half of the RAM).

EFFECTS OF REFRESH

The requirement for refreshing the data stored in the cells of a 16K dynamic RAM such as the 2116 impacts system characteristics in three areas; memory available time or throughput, system standby power, and the maximum usable page size during page mode operation. The 64 cycle refresh mode of the 2116 offers improved performance in all these areas over the 128 cycle refresh mode.



a. Intel® 2116 Layout



b. Alternate Device Layout

Figure 1. 16K RAM Device Configurations

Memory Availability

Assuming a minimum cycle time of 375 nsec, 128 refresh cycles in 2 msec requires 48 μsec or 2.4% of the available memory time. But that's a minimum. Typical computer memory cycle times run closer to 700-900 nsec, so 128 cycle refresh typically requires 102 μsec or 5.1% of the available memory time. 64 cycle refresh requires only 51 μsec or 2.5% of the available memory time under the same conditions of 700-900 nsec cycle time. (See Table I). That's higher throughput capability and less chance of having to wait for completion of a refresh cycle to start a data access.

Table I. Time Impact Of Refresh

Refresh Mode	System Cycle Time	Requirements of Refresh: Time Spent On Refresh During Each 2 msec	Requirements of Refresh: Percent Of Available Memory Time
64 cycle	375 nsec	24 μsec	1.2%
	800 nsec	51 μsec	2.6%
128 cycle	375 nsec	48 μsec	2.4%
	800 nsec	102 μsec	5.1%

System Standby Power

Remember, the 2116 can be refreshed each 2 milliseconds in one of three ways; 128 Read cycles, 128 $\overline{RAS}$-only cycles, or 64 $\overline{CAS}$-before-$\overline{RAS}$ cycles. The standby power (refresh only) for the three types of 2116 refresh cycles is given in Table II.

Table II. Power Considerations For Refresh

Parameter \ Cycle	Read/ Refresh	$\overline{RAS}$-Only Refresh	$\overline{CAS}$-Before-$\overline{RAS}$ Refresh
Refresh Cycles	128	128	64
Power Per 500 nsec Cycle	444 mW	346 mW	426 mW
Average Refresh Power	31 mW	28 mW	24 mW

"Wait a minute," you say! "If you turn on both 8K x 1-bit halves of the 2116 during 64 cycle refresh, why is the power per cycle less than during a Read/Refresh cycle and why is the average power less than with either Read/Refresh or $\overline{RAS}$-only cycles?" Let's take these questions one at a time!

The *per cycle* power with $\overline{CAS}$-before-$\overline{RAS}$ is lower than for the Read/Refresh cycles because the $\overline{CAS}$ clock generator circuits and column decoders do not operate during 64 cycle refresh and the common I/O circuits are off. The power reduction due to these circuits being off more than offsets the increase in power dissipation due to both halves of the RAM being on.

The *average power* is lower with $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles because there are only 64 cycles each 2 milliseconds rather than 128. The 2116 is, therefore, in standby a larger percentage of time during the 2 millisecond refresh period. Although the $\overline{CAS}$-before-$\overline{RAS}$ *per cycle* power is 23% higher than the $\overline{RAS}$-only per cycle power, the *average* power is 14% lower!

There is one other power related characteristic of $\overline{CAS}$-before-$\overline{RAS}$ refresh which must be considered. The peak value of the transient currents during a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle is approximately 20% higher than during the other two refresh modes. This is caused by the capacitive charging/discharge currents associated with 128 additional sense amplifiers. Care must be taken in the system design to decouple the slightly higher transient peaks. Work in the Intel Applications Lab has shown that the decoupling and board layout suggestions included in the 2116 data sheet yield acceptable power distribution noise levels with any of the allowable refresh modes.

Refresh-Page Mode Interaction

Page mode operation with 16K RAMs allows faster successive memory data operations at the 128 *column* locations in a single addressed *row*. Receipt of a $\overline{RAS}$ and a 7-bit row address byte causes the RAM to access the 128 data cells on the addressed row.

At access time all 128 data bits are available at the sense amplifier outputs as long as $\overline{RAS}$ is held active. By cycling the $\overline{CAS}$ clock and addressing the desired data bit with the 7-bit column address byte all 128 data bits may be brought to the data output of the device. Data access and cycle time in this mode, called page mode, is faster than normal data cycles. Page mode is an excellent way to transfer blocks of data to and from memory at high speed, but it is impacted by refreshing. The refresh requirements of the devices limit the number of consecutive page mode cycles to less than the 128 available from each row of devices. As an example, recall that the 2 millisecond distributed refresh mode requires a refresh cycle every 15.5 microseconds, (for 128 cycle refresh mode) and every 31 microseconds (for the 2116 in its 64 cycle refresh mode). This means that the devices may remain in the page mode for a period no longer than the time required between refresh cycles.

For example, for systems using 128 cycle refresh, the maximum time in the page mode is 15.5 μsec. For systems using 64 cycle refresh the time in page mode is doubled to 31 μsec. In practice, this limits the number of consecutive page mode cycles to 55 or less for the designs which use 128 refresh cycles and to 110 or less for the 2116 in its 64 cycle refresh mode. The 2116 with its 64 cycle refresh mode clearly permits more useful page mode operation than would a 16K RAM which requires 128 refresh cycles. Table III summarizes the impact of refresh upon page mode operation.

Table III. Refresh Impact Upon Page Mode Operation

Refresh Mode	Time Period Between Refresh Cycles	Number of Page Mode Cycles Possible Between Refresh Cycles
128 Cycle/2msec Read, or $\overline{RAS}$ - Only	15.5 μsec	55
64 Cycle/2msec 2116 $\overline{CAS}$/$\overline{RAS}$ mode	31.0 μsec	110

IMPLEMENTATION OF 64/128 CYCLE REFRESH MODES

Provision for 64 cycle refresh was a major factor in the selection of the device architecture shown in Figure 1a for the 2116. There are, however, several other performance and yield related advantages to the 2116 architecture.

Implementing 64 cycle refresh requires limiting the number of data cells per sense amplifier to 64. That means 256 sense amplifiers are required (16,384 cells ÷ 64 cells/sense amp = 256 sense amps). 128 cycle refresh would force 128 cells per sense amplifier and only 128 sense amplifiers. So the question boils down to a 256 x 64-bit organization versus a 128 x 128-bit organization. (See Figure 1).

256 Sense Amps Means Twice As Much Chip Area For Sense Amps

True, when you double the number of sense amps, you double the chip area required for sense amps. However, the sense amp area on the 2116 amounts to only 12% of the total chip area so reducing the number of sense amps to 128 would only reduce the chip area by 6% which isn't very significant.

128 Cells Per Sense Amplifier Means Larger Cells

Putting 128 storage cells on each sense amplifier would require the bit sense lines to be twice as long as with 64 cells per sense amp. This means the bit sense line capacitance would nearly double. To keep the sensed signal level the same, the cell-capacitance-to-bit-line-capacitance ratio must remain the same.

With double the bit sense line capacitance, the cell capacitance must be doubled and this would increase the chip area devoted to the storage cell by approximately 25%.

The cell capacitor could be made larger by less than a factor of two, but the signal-to-noise ratio of the sensing function would be degraded. It also would adversely affect the access time and device operating margins and is not a good alternative.

Complete Capatibility

The 128 cycle refresh mode offered with the 2116 is 100% compatible with other 16K RAMs that offer *only* 128 cycle refresh. That means that the 2116 fits into sockets designed for 64 cycle refresh *and* into sockets designed for 128 cycle refresh. Other RAMs only fit into sockets designed for 128 cycle refresh.

TO LATCH OR NOT TO LATCH

One area of non-compatibility between the announced 16K RAMs is the inclusion of an output latch on the device. This has given rise to a LATCHED/NON-LATCHED device debate. Let's examine the issue to understand the system effects of the output latch.

4K Compatibility

The 16-pin 4K RAM, available from a multitude of suppliers, established the standard for latched output, multiplexed address RAMs. All available 16-pin 4K RAMs have compatible latched outputs.

Since the 16-pin 16K is virtually identical to the 16-pin 4K in terms of pin-out and timing, it seems reasonable to make the interface between the two devices as close as possible. The 2116 is *fully* output compatible with *all* 16-pin 4K RAMs. This allows the unprecedented "luxury" to system designers of upgrading their system densities by a factor of four with only an address strapping change on their memory boards.

Also, no new learning curve is required for the system designers since the parts would operate the same. Chip select, $\overline{CS}$ (pin 13), on the 4K was actually latched and implemented as an address bit just like the 6 column address bits. Pin 13 on the 16K is address bit A_7.

A number of Intel's 16-pin 4K customers are using their 4K RAM boards to evaluate the 2116 with pin 13 jumpered to an address driver rather than the old $\overline{CS}$ driver. Even the test procedures can be the same.

Common I/O Operation

When designing with microprocessors that employ bi-directional I/O buses, the ability to connect memory devices directly to the bus can be an asset. A memory device without an output data latch can have it's Data-In and Data-Out pins connected together and directly to the I/O bus if the operation of the RAM is restricted to simple read and write cycles. Let's look at what this means in two separate classes of microprocessor systems.

Single Board Systems

Small microprocessor systems typically use a limited number of LSI circuits designed as a CPU-I/O combination and sold together as a chip set. Because of the limited number of devices connected to the microprocessor I/O bus, memory devices can often be directly connected to the data ports without any buffering or isolation devices. Since the bus is generally local to the chip set, and does not leave the printed circuit board, it is not subject to the risks of backplane voltage shorts and potential device destruction. These systems can benefit from direct RAM connection to the I/O bus. Single board microprocessor systems that employ bidirectional I/O buses can benefit from non-latched output RAMs because the Data-In and Data-Out pins can be tied together. These small systems use small amounts of memory, however, and it is often contained on the CPU chip or integrated into an I/O device. The amount of external RAM memory, when used, seldom exceeds 1K to 2K words and the 16K RAM will not find much usage in these small systems.

Multiple Board Systems

Larger microprocessor systems place the main RAM storage, or an expansion to the RAM storage, on separate printed circuit boards. All signals to and from the memory must then be buffered to prevent overloading of the microprocessor I/O bus and to protect the outputs (and inputs) of both the microprocessor and memory devices from accidental shorting to a supply voltage or to ground during troubleshooting and normal system maintenance/repair. The effect of these buffers (see Figure 2) is to eliminate any need or advantage to tying the RAM data input and output together.

It is in these larger systems that the 4K and 16K RAMs are most useful due to the size of the memory required. These systems normally use 12K to 64K bytes of memory and the density of the 16-pin RAMs is an asset. Common I/O RAM operation is not a factor in these systems. Besides, if common I/O is so important for RAMs in microprocessor systems, why does the RAM that is the most widely used in microprocessor systems today (the 2102) have separate I/O?

ADVANTAGES OF THE LATCH

There are a number of system advantages to the data-out latch on board the RAM. Some of the more important of these advantages are:

1) Many small, non-microprocessor systems, especially those which run with long system cycle times (1 μsec or more) need the data read from memory to be latched in order to minimize the clock or active time and minimize power dissipation. In these systems, the on-chip data latch is an asset because off-chip data latches increase the system power dissipation. Power dissipation for TTL data latches runs about 70 mW per bit. For 16K by 8-bit memory that is 70 mW per 16K and is a constant DC power drain during active or standby cycles. The on-chip latch adds only 24mW to the device power dissipation and only while the data output is active, not during standby.

2) Off chip latches require more packages on the memory board. A 16-bit system will require four 16 pin packages or two 24 pin packages. These latches take up board space and add part, assembly, and maintenance costs to the system.

3) Off chip latches also add to access time. The delay of an on chip latch is included in the access time for the device. Using an unlatched output device and adding external

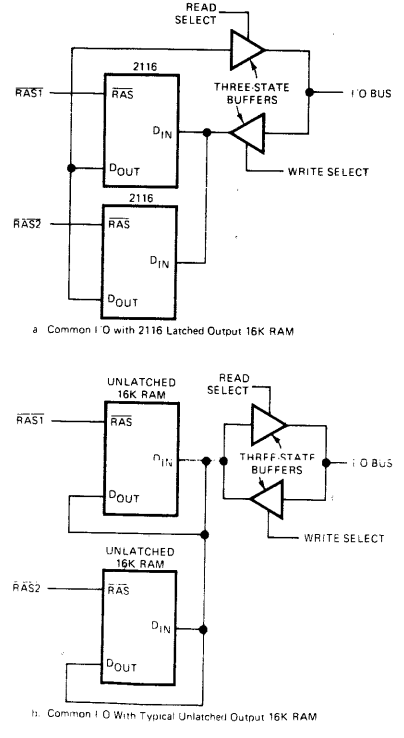
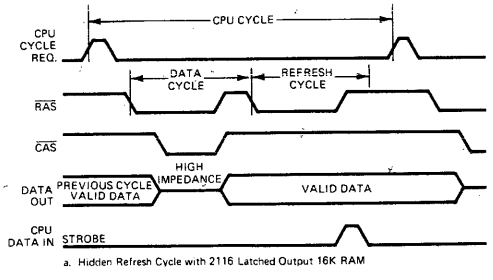


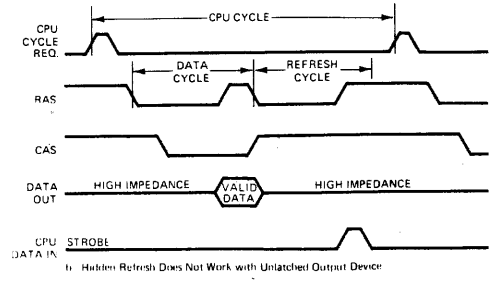
Figure 2. Common I/O Configurations

latches adds typically about 20 nsec to system access time due to timing skew in the latch clock plus the latch propagation delay.

4) An operational feature that is offered in latched output RAMs and is not available on unlatched output RAMs is the ability to perform a refresh cycle immediately following a data cycle without impacting the availability of output data. This "hidden" refresh cycle is possible with the latched output device because a $\overline{RAS}$-only refresh cycle does not affect the data contained in the output latch. A typical timing diagram for the hidden refresh mode is shown in Figure 3. This mode of operation is not possible with the unlatched output devices unless external latches are added because the data output of the unlatched devices goes to the high impedance state at the beginning of the $\overline{RAS}$-only refresh cycle and is not available to the processor when required. This hidden refresh cycle feature of the 2116 and the latched output 4K RAMs can be used to advantage in many systems.



a. Hidden Refresh Cycle with 2116 Latched Output 16K RAM



b. Hidden Refresh Does Not Work with Unlatched Output Device

Figure 3. Hidden Refresh Cycle Operation

DISADVANTAGES OF THE LATCH

There are also a number of potential system disadvantages to the data out latch. These disadvantages are generally not practical limitations on system design due to other overriding considerations as discussed below:

1) Systems designed with latched 16K's whose outputs are OR-tied must provide $\overline{CAS}$ to every device during every cycle in order to deselect devices selected on the previous cycle. Although non-latched devices can and do operate in this mode, this $\overline{CAS}$ deselect cycle is not required and $\overline{CAS}$ can be decoded and sent to the selected devices only.

   Since $\overline{CAS}$ occurs after $\overline{RAS}$ in a cycle, a cycle could be started with $\overline{RAS}$ to every device and $\overline{CAS}$ decoded during t_{RCL} and applied only to the desired devices. Thus $\overline{CAS}$ is now like $\overline{CS}$ on the 16-pin 4K RAMs. This operation reduces access times by 10ns when using a 74S138 decoder since the chip select decode time is not required prior to $\overline{RAS}$ as it is with the latched output 16K RAMs. The practical usefulness of this operational mode is limited since using $\overline{CAS}$ as a chip select means that the unselected devices in a system dissipate power at a level only slightly less than the selected devices (See Table II $\overline{RAS}$-only cycle power). This mode dissipates almost as much power as that dissipated when using $\overline{CS}$ in 4K RAMs for deselection. (Which explains why nobody used $\overline{CS}$ for device selection with the 4K).

2) The Data-In and Data-Out pins may not be directly tied together and to a common I/O bus. This is a disadvantage only in single-board microprocessor systems and not in larger systems (refer to Figure 2).

WHICH NON-LATCHED 16K?

All non-latched 16K's are not alike! In fact, none of them are alike. The three currently released designs all react differently during either read or write cycles.

Data Output Control

The data output is controlled by $\overline{CAS}$ in both the latched and non-latched devices and becomes valid at column access time (t_{CAC}) after $\overline{CAS}$ goes low (active). The difference lies at the point in time at which the data out goes to the off (high-impedance) state. In the latched output case, data out goes to the off state after $\overline{CAS}$ goes low in the *next cycle*. In the non-latched output case, data out goes to the off state after $\overline{CAS}$ goes high in the *current* cycle.

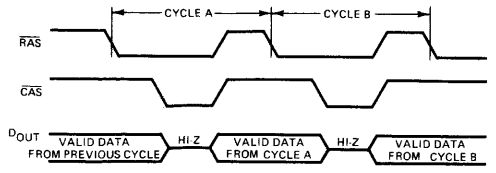


Figure 4. 2116 Data Output Operation

Unlatched Device Output Characteristics

Differences in characteristics of the outputs of non-latched devices are shown in Figure 5 for a read cycle.

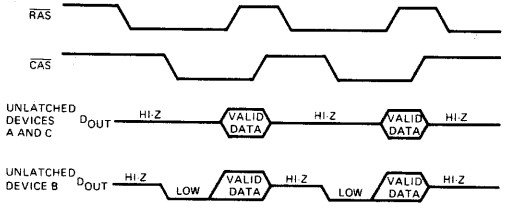


Figure 5. Unlatched Device Output Operation During Read Cycles

When it comes to a write cycle the data-out characteristics of the 3 suppliers are different from each other (see Figure 6). So why would anyone care what the *output* is doing during a write cycle? Incoming test programs and device qualification testing must account for these differences. Also, since the device outputs are connected to an I/O bus of some sort, the designer must consider the output operational characteristics to assure compatibility with the bus.

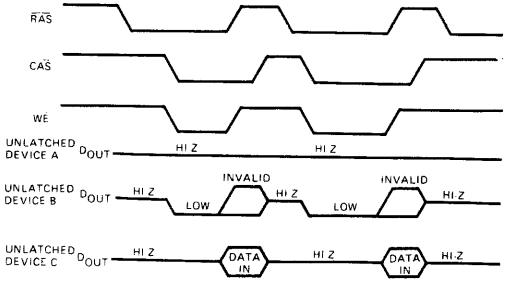


Figure 6. Unlatched Device Output Operation is Different During Write Cycles

None of the above differences by itself is hard to handle but it can be troublesome to have to account for all conditions especially in testing and qualifying the devices.

$\overline{CAS}$ AS A CHIP SELECT

During the discussion of the disadvantages of a data out latch, the use of $\overline{CAS}$ as a chip select signal was mentioned briefly. The system parameters affected by this use of $\overline{CAS}$ are access speed, power dissipation, and page mode.

Access Speed

Decoding the chip select address bits and gating $\overline{CAS}$ only to the selected devices reduces access times by about 10 nanoseconds compared to gating $\overline{RAS}$ as the chip select signal.

Power Dissipation

Using $\overline{CAS}$ as the chip select signal means that the unselected devices in a system dissipate $\overline{RAS}$-only power levels while the selected devices dissipate full power levels.

What does that mean in a 128K x 8-bit system? Decoding only $\overline{CAS}$ and supplying $\overline{RAS}$ to all 64 devices means one row of devices would dissipate normal power while seven rows would dissipate $\overline{RAS}$-only power levels during each cycle. The 128K by 8-bit system (8 rows of 16 devices) will dissipate 23.0 Watts in this mode.

Decoding only $\overline{RAS}$ as chip select and supplying $\overline{CAS}$ to every device does add slightly to access time (about 10 nsec) but it also means only 8 devices of the 64 in our example system would be active in any given cycle while the other 56 devices would remain in refresh/standby. The same 128K x 8-bit system will dissipate 5.2 Watts in this mode. (See Table IV).

Table IV. Power Considerations for 128K x 8-bit System

Operational Mode / System Parameter	Decoded $\overline{RAS}$	Decoded $\overline{CAS}$
I_{DD} Current	0.43 Amps	1.92 Amps
Power Dissipation	5.2 Watts	23.0 Watts

Page Mode

In the non-latched RAM, $\overline{CAS}$ used as a chip select signal allows extension of the page mode boundary beyond 128 data cells. This is accomplished by supplying $\overline{RAS}$ to all the devices in a system and $\overline{CAS}$ to the selected devices extending the boundary to include the selected row in all of the RAMs in the system. This operation is valid but there are some practical restrictions on its usefulness.

Extension of the page mode boundary again requires activating all the devices in the system rather than just one row of devices. The increase in power dissipation incurred makes this mode of operation rather undesirable as previously discussed. In addition, the refresh requirements of the devices limits the number of consecutive page mode cycles to less than the 128 available from *one* row of *one* device. Remember that refresh requires $\overline{RAS}$ to be cycled to refresh a row of cells every 15.5 microseconds with the 128 refresh cycle mode and 31 microseconds with the 2116 in its $\overline{CAS}$-before-$\overline{RAS}$ 64 cycle refresh mode. Why activate *all* of the RAMs in the system when you can't even cycle through all the locations in *one* row of *one* RAM in a single page mode cycle?

SUMMARY

The goals for the 2116 16K RAM, increased bit density while maintaining performance and functional compatibility with the 16-pin 4K RAMs, have been achieved. This compatibility is a boon to the users since no new learning curve is needed when upgrading to the 16K RAM.

While there are differences in the announced 16K RAMs, these differences are slight when compared to the differences between the proliferation of 4K RAMs. By including TTL data out latches in the board design and using 128 cycle refresh, the designer can accommodate any of the 16-pin 16K devices.

For those users who wish to maintain the throughput rate of the 4K devices, the 64 cycle refresh mode of the Intel 2116 is ideal. The on board data out latch of the 2116 is a definite asset to those users with restrictive board space limitations. In extremely cost sensitive applications, the 2116's data out latch not only eliminates the need for external TTL latches but also reduces system power dissipation thereby reducing power supply and cooling costs.

The biggest erasable PROM yet puts 16,384 bits on a chip

Using just one 5-V supply, the ultraviolet-erasable device is interchangeable with 16-k read-only memories—a boon to designers of microprocessor systems

by Robert Greene, George Perlegos, Phillip J. Salsbury, and William L. Morgan, *Intel Corp., Santa Clara, Calif.*

☐ In just two or three years, from being barely on the edge of visibility, a field-erasable read-only memory has blazed its way to prominence in the system designer's world. Because its contents can be erased with ultraviolet light, its user can program and reprogram it at will—an unaccustomed liberty.

Known as EPROMs (for erasable programmable ROMs), the devices in heavy use today are the 2,048-bit 1702A and the 8,192-bit 2708, both of which have been designed into a wide variety of equipment over the past few years. But the new 16,384-bit model, which is also faster and easier to use than its predecessors, is bound to attract old and new users alike.

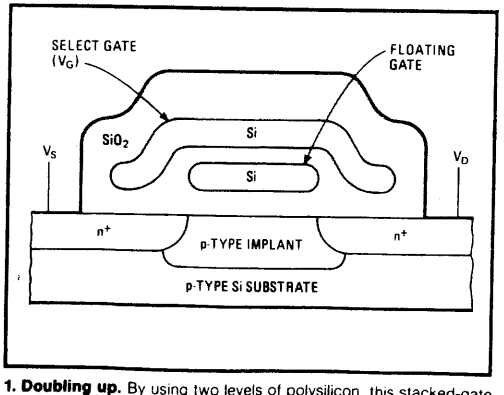
The attraction, of course, is the devices' extreme usefulness for prototyping software code in microprocessor-based designs. It typically takes tens of passes through a system before a program's code can be optimized, and each pass requires a new ROM program. But a ROM that can be erased and reprogrammed quickly from standard address signals makes it much easier to optimize a program.

Indeed, individual words can be rewritten in today's UV-erasable PROMs, so that programmers can fine-tune their software well into the development cycle or change a portion of the program to accommodate new system features. Then, once satisfied with the program, the user can switch into production with factory-programmable ROMs that have identical pin assignments and use similar power supplies.

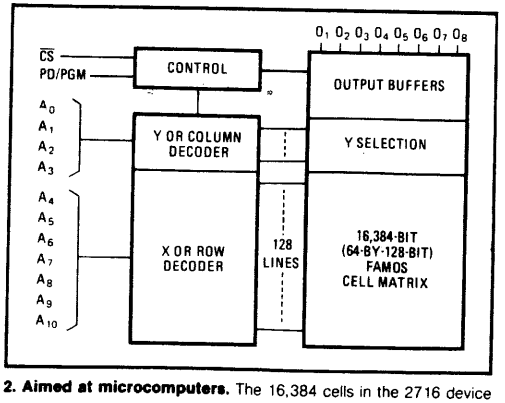
Alternatively, as the availability of erasable PROMs increases, system designers are beginning to use them in place of standard ROMs in the production equipment itself, especially in the early sample stage and also in small-volume designs. It is an all-too-familiar problem, getting small numbers of mask-programmed ROMs from the factory in anything like a reasonable time and at less than an exorbitant per-piece cost. Here the erasable PROM is the perfect answer, for it goes straight into the equipment once its program is fixed.

A good deal in all respects

The new Intel Corp. 2716 16-k device has all this versatility, and then some (see table). It offers twice the memory capacity on a chip only 20% larger than the 8-k version—and the smaller the die, the lower its production costs eventually fall. Its performance is better. Though its maximum access time stays at a short 450 nanoseconds, its active power dissipation per bit has been reduced to 40% of the 8-k device level, so that the chip's total power dissipation is 20% lower for 16,384 bits than



1. Doubling up. By using two levels of polysilicon, this stacked-gate version of the floating-gate avalanche-injection MOS cell occupies half the area of earlier Famos cells. As a result, the 16,384-bit 2716 chip is only 20% larger than the 8,192-bit 2708 devices.



2. Aimed at microcomputers. The 16,384 cells in the 2716 device are organized into two 64-by-128-cell arrays or 2,048 8-bit words, an arrangement that makes the device useful for byte-oriented microcomputer designs and also compatible with 16-k ROMs.

ULTRAVIOLET-LIGHT-ERASABLE PROGRAMMABLE ROMs			
Year	1972	1975	1977
Model	1702A	2708	2716
Basic features			
Technology	p MOS	n MOS	n MOS
Organization	256 X 8	1,024 X 8	2,048 X 8
Chip area (mil^2 equiv.)	134	160	175
Package pins	24	24	24
Read performance			
Access time (max) (ns)	650	450	450
Power dissipation (mW)	700	730	500
" " per bit (mW)	0.4	0.1	0.04
Standby power (mW)	·	·	125
" " per bit (mW)	·	·	0.006
Power supplies (V)	+5, −9	+5, +12, −5	+5
TTL compatibility	yes	yes	yes
Programming requirements			
Supply voltages (V)	+12, −35, −48	+26, +5, +12, −5	+25, +5
" " pulsed, V_P	yes	yes	no
Program control levels (V)	0/−48	0/+12	TTL
Address and data inputs (V)	0/−48	TTL	TTL
Duty cycle (%)	20	80 − 100	80 − 100
Programming performance			
Programming time of all words (s)	120	100	100
" " per word (s)	0.4	100	0.05
Single-pulse programming	no	no	yes
Single-location programming	yes	no	yes
Erase time of all words (minutes)	10 − 20	10 − 30	10 − 30

*Power dissipation can be reduced by clocking power supply or turning off during deselect

it was for 8,192 bits. In fact, the 2716's speed-power product, at 450 ns and 500 milliwatts, puts it on a par with standard high-density ROMs. Moreover, the chip's low standby power mode, in which it dissipates only 125 mW, affords further power savings at the system level.

Equally important, the 2716 works off a single 5-volt power supply, in contrast to the earlier multiple-supply 1702A and 2708 devices. This change is vital for today's designs, since it allows the device to be used with the new, more powerful 5-V microcomputers. In fact, another device using the same basic cell concept, the 8755, has been designed with special input/output ports and control lines to work directly with the 5-V Intel 8085 microcomputer, as well as with other types of 5-V microprocessor systems.

In applying the new 16-k 2716 in microprocessor-based systems, the system designer not only replaces two 2708 packages with one 2716, but he or she can also eliminate the 1-of-4 decoder chip that is needed with the two earlier devices. Indeed, when hooking up the 2716 to single-chip microcomputers such as Intel's 8048, only a standard, commercially available 8212 latch is used, as with the 2708 configuration, and nothing else. All other control signals and address signals are supplied by the processor.

Finally, the new devices are easier to program than the earlier ones. They need only two programming supply voltages (+25 and +5 V) instead of three and four different voltage levels (some as high as 48 V) typical of UV-erasable PROMs. Moreover, the program voltage V_P need not be a low-duty-cycle pulse, so that program time is greatly reduced—from 100 seconds to 0.05 s per bit—even while control levels and address and data inputs are kept at straight 5-V transistor-transistor-logic levels.

All these improvements flow from a new n-channel stacked-gate cell that uses just one transistor. This cell is fabricated with a dual-layer silicon-gate process that closely resembles the one used in today's 16-k dynamic random-access memories. As the cross section in Fig. 1

The Famos principle

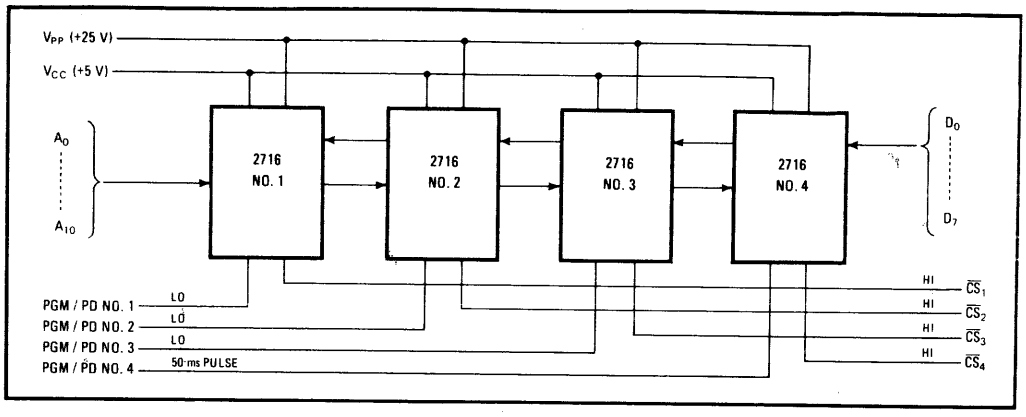
Famos describes the floating-gate avalanche-injection metal-oxide-semiconductor transistor that Dov Frohman-Bentchkowsky developed at Intel Corp. in 1971.

The Famos device is essentially a silicon-gate MOS field-effect transistor in which no connection is made to the floating silicon gate. Instead, charge is injected into the gate by avalanches of high-energy electrons from either the source or the drain. A voltage of -28 volts applied to the pn junction releases the electrons.

Data is stored in a Famos memory by charging the floating-gate insulator above the channel region. The threshold voltage then changes, and the presence or absence of conduction is the basis for readout.

The Famos cell has generally been considered more reliable than nitride storage mechanism used in reprogrammable metal-nitride-oxide-semiconductor memories. In MNOS memories, carriers tunnel through a thin oxide layer into traps at the oxide-nitride interface. But a partial loss of stored charge during readout limits the number of readout cycles to approximately 10^{11}.

In Famos memories, on the other hand, there is no loss of charge due to reading. Moreover, over time, the loss of stored electrons is negligible, less than one per cell per year, and information retention is excellent.



3. Picking and choosing. The 2716 erasable PROM has a program inhibit mode, to allow the designer of a multipackage system to program some of the devices and not others. Only those devices that receive a TTL-level pulse on the PGM/PD pin will be programmed.

shows, a lower floating gate stores the cell's charge, and an upper control or select gate operates the cell. Being stacked one over the other, the gates create an extremely compact structure—the smallest cell of any UV-erasable PROM in production. Including decode, address, drive, and sense circuitry, the entire memory fits on a chip well under 40,000 mil^2 in area.

As for the cell's operation, the fact that it has a fairly complicated stacked-gate configuration is completely transparent to the user. Unlike the 1702A erasable-PROM floating-gate cells (see "The Famos principle," p. 109), the stacked-gate cell is programmed by means of hot electrons injected from the channel through the oxide to the floating gate. This injected charge raises the threshold voltages at the top or select gate, so that a charged cell has a higher select voltage than an uncharged cell. The overall charge pattern, then, as seen from the select gates, duplicates the pattern of a standard mask-ROM.

Once programmed, the charge retention of the new 16-k UV-erasable PROM is as good as in the original Famos devices. Reliability studies of standard production runs indicate that 95% of the devices can be expected to retain their memory for 100 years at 70°C. Charge removal from the stacked-gate cell occurs with its exposure to ultraviolet light, just as in both the earlier UV-erasable devices.

Using the 2716

The array of 16,384 Famos cells, which are formed into two 64-by-128-cell matrixes (Fig. 2), is organized as 2,048 8-bit words, giving the 2716 a byte orientation that is useful in microcomputer applications. Because of this arrangement, the device operates almost exactly like the 2708 8-k erasable-PROM. The only differences are that on the 2708 device the power-supply voltages V_{DD} and V_{BB} are on pin 19 and pin 21 respectively, whereas on the 2716 device the address A_{10} is on pin 19 and the program voltages (+25 V for programming, 5 V for reading) are on pin 21.

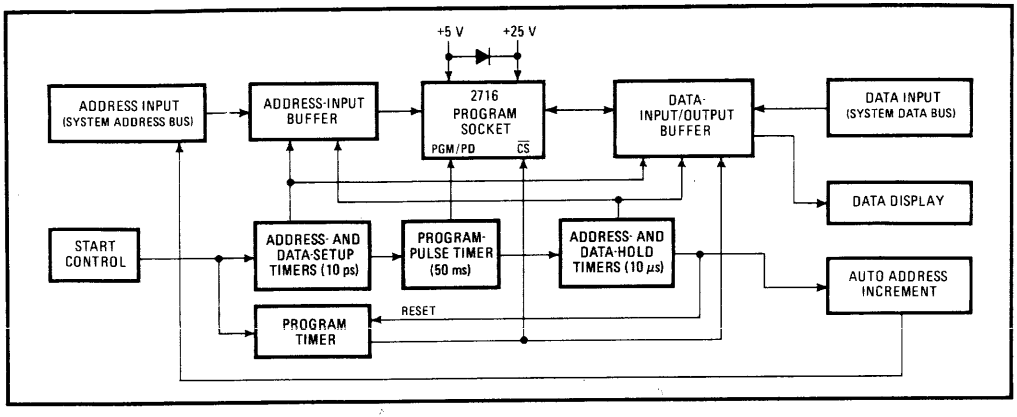
Otherwise, complete data and power-supply compatibility exists between the familiar 2708 and the new 2716: they plug into exactly the same sockets, having exactly the same standard 24-pin package and the same pin assignments (except for those mentioned above). The one change in designing a board with a 2716 is that programming it requires a +25 V power supply and reading it takes a 5-V supply instead of the 26-V pulses needed for programming and the ±12 V, +5 V, and −5 V supplies needed for reading the 2708.

As for ease of use, the 2716 compares well with ordinary ROMs. The seven highest-order address bits, A_4 to A_{10}, select the rows, while address bits A_0 to A_3 select the columns and operate on eight 1-of-16 decoders, such that one of 16 column lines is gated to each of the eight output buffers.

Sensing is the same as in the 2708 devices. The charge on the selected column line is monitored. Unprogrammed cells will have a low threshold and will discharge the column line when selected, while the threshold of programmed cells will have been raised to an impedance level that is high enough to keep the column line charged.

To read the 2716, the chip-select input is the only control input required. Lower this input to a transistor-transistor-logic 0 and the device reads; raise it to a TTL 1 again and the device stops reading—is deselected. When deselected, this chip-select input causes the outputs to go into the high impedance state within about 120 ns, a time short enough to allow a designer to OR-tie several 2716s in parallel yet still retain the maximum 450-ns access times of individual devices. On the other hand, since chip select is really an enabling signal, if only one or two 2716s are being used in a system, they may be left low during all cycles, allowing a designer to exploit the typically faster access times of any individually selected devices.

Writing and erasing are no big chores, either. Initially, and after each erasure, all bits of the 2716 are in the logic 1 state (output high). Data is written by selectively programming 0s (output low) into the desired bit locations. To set up the 2716 for programming, the program power supply, V_{PP}, is raised to 25 V, and the chip-select is raised to the input high-voltage state (V_{IH}) or 2.2 V



4. Programming made easy. In this setup, the user need only observe the appropriate setup times for the programming operation to succeed. The start control signal gets the timing chain moving, and from then on things are practically automatic.

minimum. The data is then presented, 8 bits in parallel, on the data output lines (O_1 to O_8 in Fig. 2), while the corresponding address is presented to the address inputs.

After the address and data setup times have elapsed, a program pulse is applied to the programming PGM/PD pin. This pulse is a TTL-level signal that serves to gate the program power supply, V_{PP}, into the array. It must be present for at least 50 milliseconds to ensure long-term retention of the programmed data. When this program is completed, the V_{PP} pin should be returned to +5 V.

Finally, erasing the 2716 is the same as for all UV-erasable PROMs. The user places it under an UV lamp and exposes it to the equivalent of 15 watt-seconds/cm^2. Although there is no evidence that extended exposure harms the device, the lamp should be placed on a timer and shut off after 30 minutes to prevent unduly long (overnight and over-weekend) accidental exposure.

A useful feature of the 2716's program design is its program-inhibit mode. In multipackage systems, this mode lets the designer ignore some of the devices on a given board and only program or reprogram the rest. The setup is shown in Fig. 3. All inputs and outputs are tied together except for PGM/PD. Only those devices that receive a TTL-level pulse on the PGM/PD pin will be programmed. In the setup shown, device No. 4 is being programmed with a 50-millisecond pulse on this pin, while the address contents of the other three devices are unaffected.

The programming schemes devised for the 2716 are easier than for previous UV-erasible PROMs, as may be seen from the example diagrammed in Fig. 4. In this scheme, the addresses and data may be derived from a microcomputer system bus. Alternatively, the user can generate both manually, employing toggle switches for control and a counter for address input. However, when manual operation is performed, a provision must be made for automatic incrementing of the address pulses.

In either case, a start control signal enables the timing chain shown in Fig. 4, assuring that the appropriate setup times are observed. This signal also enables the program timer, which controls the 2716 chip-select signal, and places the data input/output buffer in the input mode. The program timer must be reset after the address and data hold times have passed.

Once started, the address and data-setup timers enable the program pulse timer, which applies the required TTL pulse to the 2716 PGM/PD pin. This pulse, in turn, on its falling edge, enables the address- and data-hold timers. After they have finished, the auto-address-increment timer does one of two things. Either it advances the address-input counter on a manual programmer, or it resets a not-busy flag on a microprocessor. The program timer is then reset, placing the data I/O buffer in the output mode for data verification. Note that the V_{PP} (+25-V) supply does not have to be turned off or switched during program/read transitions. However, it should be lowered to V_{CC} for nonprogramming operation to reduce power dissipation. □

From PROM to final ROM—fast

Since the UV-erasable 16,384-bit 2716 user-programmable ROM is pin-compatible with the 2316E mask-programmed 16-k ROM, designers can debug systems with the 2716 and, as soon as the data pattern is firm, order read-only memories to plug directly into the 2716/2316E socket. In fact, the initial system can be shipped with erasable PROMs and fitted with ROMs in the field when they become available. Also, the 2716 can be used as the master for transmitting the desired data pattern back to the factory without all the hassle of tape formats.

This direct interchangeability between the 2716 and the 2316E can also speed up implementing code changes. In the past, even when systems were successfully prototyped with UV-erasable PROMs and released to production using mask ROMs, the slightest code change forced the end user to wait while the new code was implemented on the prototype system, then translated into a ROM pattern, and only then placed in the production system. But when the 2316E is used in production systems, any change in code can be performed in a matter of a few hours by programming a 2716 with the custom pattern and plugging it in.

Using charge coupled devices can reduce bulk memory costs

CCD's offer adequate performance in these applications and provide truly significant cost savings when compared to RAM configurations.

Dave House and **Kirk MacKenzie,** Intel Corp.

Over the course of the past several years, semiconductor memories have become a dominant form of main memory. And today they are being applied in secondary or bulk storage applications as well. Assuming that you've already made the decision to go semiconductor for your bulk storage, the first and most important choice facing you is this—should you go the MOS RAM (Random Access Memory) or CCD memory component route?

In areas where their performance is adequate, CCD memories can provide a significant reduction in cost for bulk memory applications. At both the component and system level, costs will be reduced by 65 to 75% by using CCD's instead of RAM's.

Quite naturally, such significant savings have not gone unnoticed and many systems have been configured to take advantage of the favorable CCD cost picture. We contend that these savings will always be possible. By their very nature, CCD's require simpler design techniques and offer both higher densities and higher yields than RAM's. The result is lower manufacturing costs both today and in the future because any advances in manufacturing or photolithography techniques will equally benefit both CCD and RAM technologies.

You can find all the answers inside

Understanding actual device costs requires some understanding of device construction and

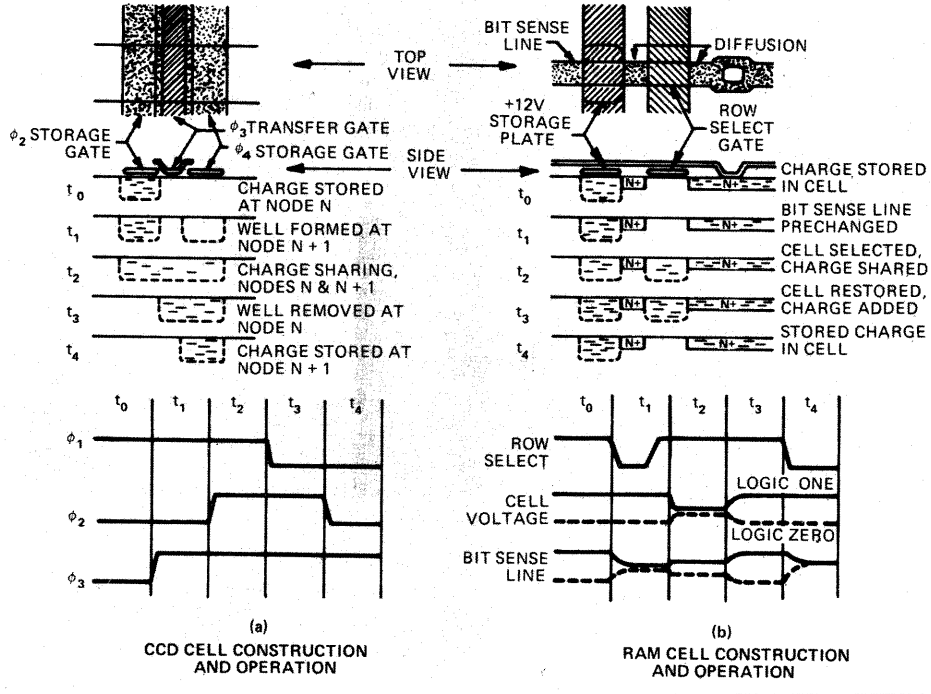


Fig. 1—Identical storage methods are employed in both the CCD and RAM cells. The positive electrode under which charge is stored is clocked in a CCD, rather than tied to a positive voltage as in the RAM.

operation. **Fig. 1** shows the basic construction of a storage cell from a 4-phase surface-channel CCD and a single transistor cell dynamic RAM. Note that in both cases the storage method is the same—charge storage in a depletion region under a positively charged electrode. Disposition of this electrode varies, however, being tied to +12V in a RAM, and clocked in CCD's. Charge transfer performs storage cell access, accomplished by turning on a MOS device to connect the storage node to either the next storage cell (CCD) or a bit sense line (RAM).

Dynamic RAM charge transfer, a generally well understood function, occurs as follows: An X or row decoder gates one transfer device per bit sense line, passing information from that cell onto the precharged bit sense line. A small positive shift occurs on the bit sense line if charge was stored in the cell; a small negative shift, if no charge was stored. In order to rewrite the data in the cell, this small shift in bit sense line voltage must be amplified by the sense amplifier.

The information transfer method in a CCD is generally not as well known, even though the mechanism is very similar and quite simple. Appropriate sequencing of a series of shift clocks common to each cell within a loop controls charge transfer. For example, the 2416, a 16k CCD available on the market today, uses four clocks, each tied to all loops. Other configurations are possible, however.

Right-left or left-right—how goes the flow?

Because the CCD is itself symmetrical to charge flow, charge can be moved either left-to-right or right-to-left, depending on the sequencing of the clocks. Most designs, however, restrict the flow of charge to one direction to simplify the design of the refresh amplifier within a loop.

Fig. 1a shows a charge packet—representing a logic ONE—moving one location to the right as the clocks are sequenced. A well first forms at node n+1 when phase 4 goes HIGH. But it contains no charge until transfer phase 3 connects the charge at node n to the well at node n+1, causing redistribution of the charge over the larger storage well. Transfer completes as phase 2 and then phase 3 go LOW, causing the well to shorten and the charge to flow to the n+1 node. A logic ZERO transfers in the same fashion, except the charge packet contains significantly less charge.

Let's get organized

The primary organizational difference between a RAM and a CCD is that the RAM—because of its direct access capability—requires a very long and highly capacitive bit sense line to conduct the stored charge to the sense amplifier. In contrast, a CCD moves the charge serially to a sense amplifier at the end of a register. This charge dumps onto a low capacitance region, resulting in significantly larger voltage transitions than experienced with RAM's. For this reason, CCD sense amplifiers can be greatly simplified. In turn, since sense amplifiers represent a major portion of RAM power dissipation, RAM's use considerably more power than CCD's.

Fig. 2 shows the layout of a 16k dynamic RAM and a 16k CCD. Because of the additional decoders required, the more complex sense amplifiers, and the increased timing and control, the RAM-cell periphery represents 66% of the total chip area. This compares to 45% for the CCD.

Although these organizational factors tend to lower CCD manufacturing costs somewhat, the primary cost differences tend to relate to the simpler construction techniques for the CCD storage array. In **Fig. 1,** note that unlike the RAM design, the CCD cell has no metal-to-silicon contacts, requires no diffusions and contains no metal. The CCD array is an undisturbed area of silicon with overlaying gate structures.

Device costs reflect device complexity

These fabrication advantages combine to produce a price per bit ratio between RAM's and CCD's of approximately 4:1; i.e., a 16k CCD costs about the same at the device level as the 4k RAM. But while this price ratio exists today for comparable quantities and deliveries, will it continue in the future? The fact that both RAM's and CCD's

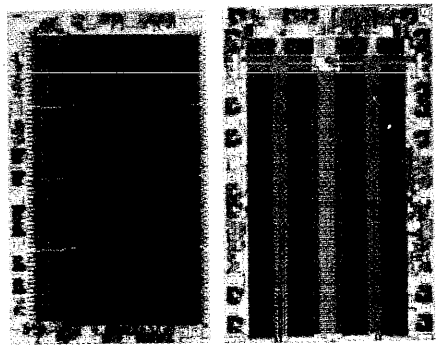


Fig. 2—Lower manufacturing costs are the direct result of CCD chip organizational factors. As the comparison shows, almost half again as much of the RAM chip area is dedicated to peripheral circuit requirements (decoders, amplifiers, etc.).

TABLE 1
BOARD COST–CCD vs. RAM

	16k CCD				4k RAM				16k RAM			
	QTY.	ITEM	COST	TOTAL	QTY.	ITEM	COST	TOTAL	QTY.	ITEM	COST	TOTAL
STORAGE DEVICES	64	2416	$8	$512	64	2104	$8	$512	64	2116	$32	$2048
CLOCK DRIVERS	16	5244	$3	$ 48	2	TTL	$0.5	$ 1	2	TTL	$0.5	$ 1
OTHER MEMORY DRIVERS	6	3245	$3	$ 18	6	TTL	$0.5	$ 3	6	TTL	$0.5	$ 3
LOGIC	10	TTL	$0.5	$ 5	10	TTL	$0.5	$ 5	10	TTL	$0.5	$ 5
P.C. BOARDS	1	PCB	$35	$ 35	1	PCB	$35	$ 35	1	PCB	$35	$ 35
MISC. COMPONENTS			$10	$ 10			$10	$ 10			$10	$ 10
ASSEMBLY & TEST			$60	$ 60			$60	$ 60			$60	$ 60
TOTAL				$688				$626				$2162

are currently available in 16k densities prompts some concern that the ratio has already collapsed, even though 16k CCD's have been in production for two years and 16k RAM's are just entering early production. To understand why this is not the case, let's study historical MOS trends.

Using the past to predict the future

From the introduction of the integrated flip-flop to the 16k dynamic RAM, the trend has been that RAM densities increase by a factor of four every two years. Dynamic RAM's have led the way, with static RAM's following one generation (two years) behind. Fabrication similarities for dynamic RAM's and CCD's, coupled with the more simplified CCD cell and array structure, suggest that a given density can be achieved at an earlier point in time with a CCD organization than with a RAM organization. Actually, CCD devices appear to be one year (one half a generation) ahead of RAM devices in level of integration.

A corollary of the previously mentioned postulate (i.e., a factor of four increase in density every two years) states that a factor of two reduction in price/bit is achieved with every new level of density. That is, two years gives a factor of four in density and a factor of one half in price/bit. These trends have been maintained through many successive generations of devices. At each generation, the new device is initially manufactured and sold at a cost/bit premium over the previous generation. Early in the product life, cost falls rapidly as the new device moves into full production. Typically, within a year the cost drops below the level established by the previous device, eventually tending towards a level of approximately one half the previous bit cost.

Technology transfers back and forth

One factor supporting the continuation of a constant price ratio between CCD's and RAM's relates to the close similarities in their fabrication. The relationship between CCD development and dynamic RAM development is more causal than it appears. In fact, it was the development of the 4k RAM that led to the development of the 16k CCD, that in turn led to the development of the 16k RAM.

Next generation devices build on current generation technology, and in this way shipments of either CCD's or RAM's provide a learning experience for the process, and both device types benefit. Any improvements in masking technology made for RAM's or CCD's can be applied to the other. Similarly, any reduction in defect densities made for one reduces the defect density for the other. Thus, the RAM and CCD share a joint learning curve.

The numbers tell the story

Now for a specific example—a hypothetical 10M-byte bulk storage system. To compare currently available 16k CCD's and 4k RAM's would somewhat distort the analysis due to the half generation difference between CCD and RAM developments. Therefore, we have also included 16k RAM's in the analysis, although 16k RAM availability lags 16k CCD availability by about one year.

A 8-in. × 12-in. board can hold 64 storage devices with their associated drivers. **Table 1** compares the cost of such a memory board incorporating CCD or RAM devices, with the assumed device costs based on medium volume

TABLE 2
STRUCTURAL, ASSEMBLY AND TEST COSTS

	16k CCD/RAM			4k RAM		
	QTY.	COST	TOTAL	QTY.	COST	TOTAL
CHASSIS & BACKPLANE	3	400	1200	10	400	4000
MAINTENANCE PANEL	1	500	500	1	500	500
CABLING			500			1000
CABINET			500			1000
SYSTEM ASSEMBLY			1000			2000
SYSTEM TEST			1000			1500
TOTAL			$4700			$10,000

TABLE 3
SYSTEM COST-CCD vs. RAM

	16k CCD			4k RAM			16k RAM		
	QTY.	COST	TOTAL	QTY.	COST	TOTAL	QTY.	COST	TOTAL
STORAGE BOARDS	80	668	55,040	320	626	200,320	80	2162	172,960
CONTROL UNIT	1	700	700	1	700	700	1	500	500
POWER SUPPLY	1kW	$1/W	1,000	2kW	$1/W	2,000	0.7kW	$1/W	700
STRUCTURAL, ASS'Y & TEST			4,700			10,000			4,700
TOTAL			$61,440			$213,020			$178,860

TABLE 4
BIT COST COMPARISON—CCD vs. RAM

	16k CCD		4k RAM		16k RAM	
	COST (m¢/BIT)	%	COST (m¢/BIT)	%	COST (m¢/BIT)	%
STORAGE DEVICES	48.8	66.7	195.3	76.9	195.3	91.6
CLOCK DRIVERS	4.6	6.3	0.4	0.1	0.1	–
OTHER BOARD COSTS	12.2	16.7	43.1	17.0	10.8	5.1
CONTROL UNIT	0.8	1.1	0.8	0.3	0.6	0.3
POWER	1.2	1.6	2.4	1.0	0.8	0.4
STRUCTURAL, ASS'Y & TEST	5.6	7.6	11.9	4.7	5.6	2.6
TOTAL	73.2		253.9		213.2	

purchases of standard products. Higher volumes would produce lower prices, but would not disturb the price ratios and would not materially affect the results of the comparison.

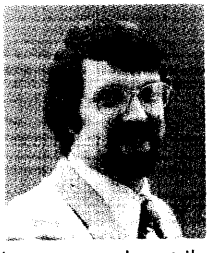
The CCD board requires 16 MOS-level drivers for the CCD shift clock inputs, compared to two TTL-level clock drivers for the RAM's. It also needs MOS-level address and control drivers instead of TTL-level drivers. The remaining board costs are the same.

A chassis 22-in. W×9-in. H×13-in. D holds 32 memory boards spaced 5/8 in. apart. Three chassis hold the 80 16k CCD or 16k RAM boards required for the complete system with room to spare. By contrast, you need ten chassis to hold the 320 4k RAM boards for this size system.

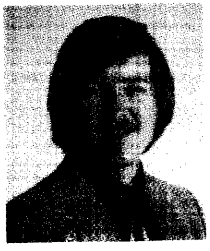
Table 2 breaks out structural, assembly and test costs. Although these are identical for the 16k CCD and 16k RAM systems, they are considerably higher for the 4k RAM system due to the larger number of boards and components. **Table 3** summarizes all system costs. The hypothetical 10M byte system costs $61,440 when built with CCD's, or $117,420 less than the least expensive (16k) RAM system.

Observe that the 4:1 RAM/CCD device cost ratio reduces to a 3:1 system cost ratio because of the allocation of the other system costs to the memory as shown in **Table 4.** Notice also that only 67% of the total CCD system cost is in the storage devices, compared to 92% for the 16k RAM system. □

Authors' biographies



Dave House is manager of Product Marketing and Applications at the Components Div. of Intel Corp. in Santa Clara, CA. In addition to running these two departments, Dave also gets involved in product planning, pricing and advertising. He has authored company application notes and contributed inputs to the Intel Memory Design Handbook. When he can find some spare time, Dave enjoys skiing, racketball and cycling.



Kirk MacKenzie is a CCD Product Marketing engineer at the Intel's Components Div. His present duties involve both product management and planning for CCD's as well as static RAM's. He has a BSEE from the Univ. of California and is presently working on his MBA. Kirk's hobbies include photography, kayaking and backpacking.

NON-VOLATILE MEMORY USING THE INTEL® MCS-40™ WITH THE 5101 RAM

Chon Hock Leow, Application Engineering

INTRODUCTION

The unpredictability of power failure in a volatile memory based system can result in a loss of irreplaceable information. Terminals, portable equipment and data collection instruments are but a few devices that require low cost non-volatile storage. Most read/write semiconductor memories are volatile i.e., information is lost when power is removed. Intel's 5101, 1K (256 x 4) CMOS static RAM with its extremely low standby power dissipation, typically 25μW, makes it feasible to retain information for weeks (444 days) using ordinary pen-light batteries on a "battery standby" mode. The use of a simple battery subsystem to maintain information can be a significant system cost reduction.

This note describes a technique for utilizing the 5101 RAM in a MCS-40 microcomputer based system. The MCS-40 is a four bit microcomputer system consisting of an array of CPUs, ROMs, RAMs, I/O devices and Peripherals. The specific MCS-40 configuration discussed here, offers a means of maintaining processor data via batteries in a power standby mode.

4289 AND 5101 INTERFACE

The MCS-40 utilizes a 4289 standard memory interface chip to accommodate the 5101 RAM. The RAM being CMOS and the 4289 being PMOS necessitates family interface considerations.

The Data Input lines (DI_0-DI_3) of the 5101 have a minimum input 'low' voltage (V_{IL}) of -0.3V, while the bi-directional I/O data lines (I/O_0-I/O_3) of the 4289 have a typical output 'low' voltage (V_{OL}) of -5V (with V_{SS} tied to +5V). With this incompatibility in voltages, buffers or clamped diodes (Germanium) are needed between the bi-directional I/O data lines (I/O_0-I/O_3) of the 4289 and the Data Input lines (DI_0-DI_3) of the 5101. This also applies to the PM line of the 4289 and the R/W line of the 5101.

The Data Output lines (DO_0-DO_3) of 5101 have a minimum output 'high' voltage of 2.4V, while the OPA_0-OPA_3 and OPR_0-OPR_3 need a minimum input 'high' voltage of 3.5V (with V_{SS} tied to 5V). Pull-up resistors are required on the OPR_0-OPR_3 of the 4289 to meet the required voltage. The DB_0-DB_3 lines of 3216 have a minimum output 'high' voltage of 3.5V, eliminating the need for any pull-up resistors.

With V_{DD1} of the 4289 tied to ground, the address and chip select lines are TTL compatible, eliminating the need for any buffering.

As can be seen in the schematic, Germanium diodes are used on the DI_0-DI_3 bus and R/W line (5101) and 3.3K pull-up resistors are used on the DO_0-DO_3 bus (5101).

The user has the option of not using the 3216 to channel data from 5101 onto the OPA_0-OPA_3 of 4289 by using an additional RPM instruction to flip the F/L flip-flop of the 4289.

INTERFACE CONSIDERATIONS

Only 1 standard CMOS NAND chip is needed to ensure CE2 of the 5101 is low during and after the process of power failure. When power is going down, one has to ensure that no random data is written into the 5101. This is accomplished by an output port and controlled by the program. In this case, a RAM output port, 4002, is used to control a simple RS flip-flop, implemented with 2 NAND gates, CD4011AE. This CMOS NAND device has to be backed up by the battery also.

The output lines (O_0-O_3) of 4002 have a minimum output low voltage of -7V (with V_{SS} tied to 5V). A clamped diode is advised although a gate-oxide protection circuit is already incorporated into CMOS integrated circuits. In this case, a silicon diode is used.

Further Details

(1) A pull-up resistor is needed per CS input of 4702A.
(2) A pull-up resistor is needed on the output of TTL driving the CMOS.
(3) Buffering is required between the outputs of 4702A and 5101. Intel's 3212 Input/Output Bipolar device meets this requirement adequately, with the added feature that more than four 4702As can be OR-tied without degrading the access time tremendously.

Battery Supply

The battery standby system used is a simple, low cost parallel diode switch. In order to drive this sys-

tem, the battery voltage and dc supply voltage should relate as follows:

V_D = 0.7V (diode drop)

$V_{max} + V_D \geq V_{battery}\ (V_{BB}) \geq V_{min} + V_D$

$V_{max} + V_D \geq V$ supply $(V_S) \geq V_{min} + V_D$

Note: V_{max} and V_{min} refer to the 5101 and CD 4011AE.

In the event the supply drops below V_{min}., the battery will forward bias diode D1 (refer to schematic) to form a closed-circuit and the 5101 and CD4011AE will continue to function properly through the battery. If a rechargeable battery is used, the battery can be trickle charged through a resistor.

Theory of Operation

Hardware Aspect

On detecting power up, the 4201 generates a reset pulse required by MCS-40 components. This reset pulse is also translated to TTL level by transistor Q_1 to enable operation of the 5101. The CPU has to be enabled for interrupt in order to recognize any interrupt. On detection of a power failure, the CPU is interrupted and 4040 begins program execution at memory location 3. Either a Power Down Routine (PDR) starts at location 3 or it contains a jump vector to the PDR. With one 5101, more than three 4002 memories can be saved in it. The F/L line of 4289 is not used in both writing into and reading from 5101. After the PDR, the RS flip-flop has to be toggled by the 4002 to disable the CE2 line so as to ensure that no random data is written into the 5101 during the power transitions. This is done by bringing the CECTL low (refer to schematic). All the above operations have to be done before the power supply drops below the minimum required voltage for the system. The time depends on how much memory one needs to save and what other I/O procedures need to be accomplished. This implies that the DC power supply must maintain power for a limited time after a line drop occurs.

Software Considerations

As the operation of the system depends entirely on the program, careful consideration must be given to the construction of the program given the limited time that the CPU has before the voltage drops below the minimum requirement. The following program is written only to save the majority of the 4002 (specifically, 4 registers of the 16 main memory characters — 64 characters). The test line is used to distinguish whether a power failure has occurred. Test line is false (0) when no power failure has occurred and true otherwise.

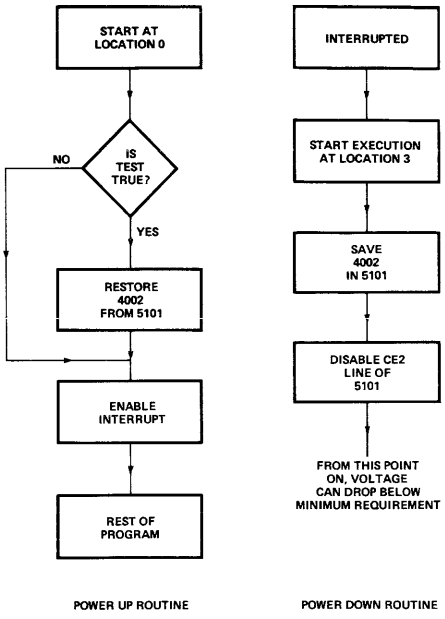


Figure 1. Program Flow Chart

The mnemonics used in the following program are those of the 4004/4040 Macro Assembler (MAC 4).

INDEX REGISTERS MAP

		14	15		
		12	13		
		10	11		
		8	9		
5101 RAM ADR	MSB	6	7	LSB	
RAM PORT ADR		4	5		
		2	3		
4002 CHIP/REG ADR		0	1	4002 CHAR ADR	

MAIN PROGRAM

```
        NOP                     ;No Operation
START:  JUN   CKTEST            :Jump to check test
                                ;line
PDR:    FIM   6,0               ;A7-A0 = 00H for
                                ;CMOS RAM
        LDM   0                 ;Select CM-RAM0
                                ;line
        DCL                     ;These two instruc-
                                ;tions are required if
                                ;CM-RAM line is not
                                ;0 during interrupt
        FIM   0,0               ;Save 4002s Reg. 0
                                ;in CMOS RAM
```

```
        JMS   SAVE
        INC   0        ;Save 4002s Reg. 1
        JMS   SAVE
        INC   0        ;Save 4002s Reg. 2
        JMS   SAVE
        INC   0        ;Save 4002s Reg. 3
        JMS   SAVE
        FIM   4,PORT 0 ;PORT 0=00000000B
        SRC   4        ;Set-up RAM port 0
        LDM   CECTL    ;CECTL=0001B cor-
                       ;responds to O0 line
        WMP            ;Disable CE2 line
HERE:   JUN   HERE     ;Wait for power to
                       ;go down.
CKTEST: JNT   INIT
PUR:    FIM   6,0      ;A7-A0 = 00H
                       ;CM-RAM0 is auto-
                       ;matically selected
                       ;after reset so that
                       ;no LDM 0, DCL
                       ;needed
        FIM   0,0      ;Restore 4002s Reg.
                       ;0 from
        JMS   RESTORE  ;CMOS RAM
        INC   0        ;Restore 4002s
                       ;Reg. 1
        JMS   RESTORE
        INC   0        ;Restore 4002s
                       ;Reg 2
        JMS   RESTORE
        INC   0        ;Restore 4002s
                       ;Reg. 3
        JMS   RESTORE
INIT:   EIN            ;Enable interrupt
```

From this point on, normal processing can proceed.

SUBROUTINES

```
SAVE:   SRC   0        ;Set-up 4002 RAM
                       ;character
        RDM            ;Fetch RAM charac-
                       ;ter
        SRC   6        ;Set-up 5101s
                       ;address
        WPM            ;Write into CMOS
                       ;RAM. Note that
                       ;only one WPM is re-
                       ;quired as the hard-
                       ;ware does not uti-
                       ;lize F/L flip-flop
        INC   7        ;Increment 5101s
                       ;address A3-A0
        ISZ   1,SAVE   ;Point to next 4002s
                       ;RAM character and
                       ;continue until all 16
                       ;main characters are
                       ;saved
        INC   6        ;Increment 5101s ad-
                       ;dress A7-A4
        BBL   0        ;Return
RESTORE: SRC  6        ;Set-up 5101s
                       ;address
        RPM            ;Fetch data from
                       ;5101
        SRC   0        ;Set-up 4002s RAM
                       ;character
        WRM            ;Restores it
        INC   7        ;Increment 5101s
                       ;address A3-A0
        ISZ   1,RESTORE ;Point to next 4002s
                       ;RAM character and
                       ;continue until all 16
                       ;main characters are
                       ;restored
        INC   6        ;Increment 5101s
                       ;address A7-A4
        BBL   0        ;Return
```

Subroutine called SAVE is to save 4002s RAM characters into 5101. The data is saved sequentially starting at address 00. The above power down routine requires 478 memory cycles. With a 10.8 μs per memory cycle, the power supply has to maintain the minimum required voltage for at least 5.16 ms (478 x 10.8 μs = 5160.4 μs).

Subroutine called RESTORE is to restore 4002s RAM characters from 5101.

Note that CPU was not enabled for interrupt until after all the restoring was finished.

System Performance

The 2 CMOS chips, CD4011AE and 5101, draw a maximum of (15 + 15) μA = 30 μA, and Q1, R1, R2, R3 draw a maximum of 7.5 μA (with V_{CCB} = 4V). With a total of 37.5 μA on a standby mode, data retention can be maintained for 444 days using a 0.4 ampere-hour battery system. The 256 x 4 organization of the 5101 makes it suitable as a substitute for 4002 on standby mode.

The schematic shown can address up to 2K of ROM i.e., 8 of 4702As. R1, R2 and R3 can be optimized to draw less current depending on the transistor used.

Alternate System Configuration

The Power Down Protect Logic (PDPL) which comprises of 4002, CD4011AE and 7404 can be left out if the user does not require the power down protect capability. If PDPL were left out, the following connections have to be modified:

(1) Tie CE2 of 5101 high
(2) Connect PM of 4289 to $\overline{CE1}$ of 5101.

The 3216 can be left out if the user chooses to use an extra RPM instruction to keep track of the F/L flip-flop of 4289. If the 3216 were left out, the RESTORE subroutine would then be the following.

```
RESTORE:  SRC   6
          RPM                 ;This is the dummy
                              ;instruction in
                              ;place of the 3216.
                              ;After reset, the first
                              ;RPM will read
                              ;OPA0-OPA3. Be-
                              ;cause the DO0-DO3
                              ;of 5101 are tied to
                              ;OPR0-OPR3, this
                              ;first RPM does not
                              ;pick up any useful
                              ;information. It
                              ;only serves to flip
                              ;the F/L flip-flop so
                              ;as to enable the
                              ;next RPM to ac-
                              ;cess the useful in-
                              ;formation.
          RPM                 ;Fetch data from
                              ;5101
          SRC   0
          WRM
          INC   7
          ISZ   1,RESTORE
          INC   6
          BBL   0
```

Conclusion

The 5101 as an MCS-40 Data Memory element can reduce the power consumption during the power down or standby mode. The use of low cost batteries to maintain important system data during a standby mode dramatically reduces user system cost over alternative methods. This is particularly true when small quantities of memory are involved.

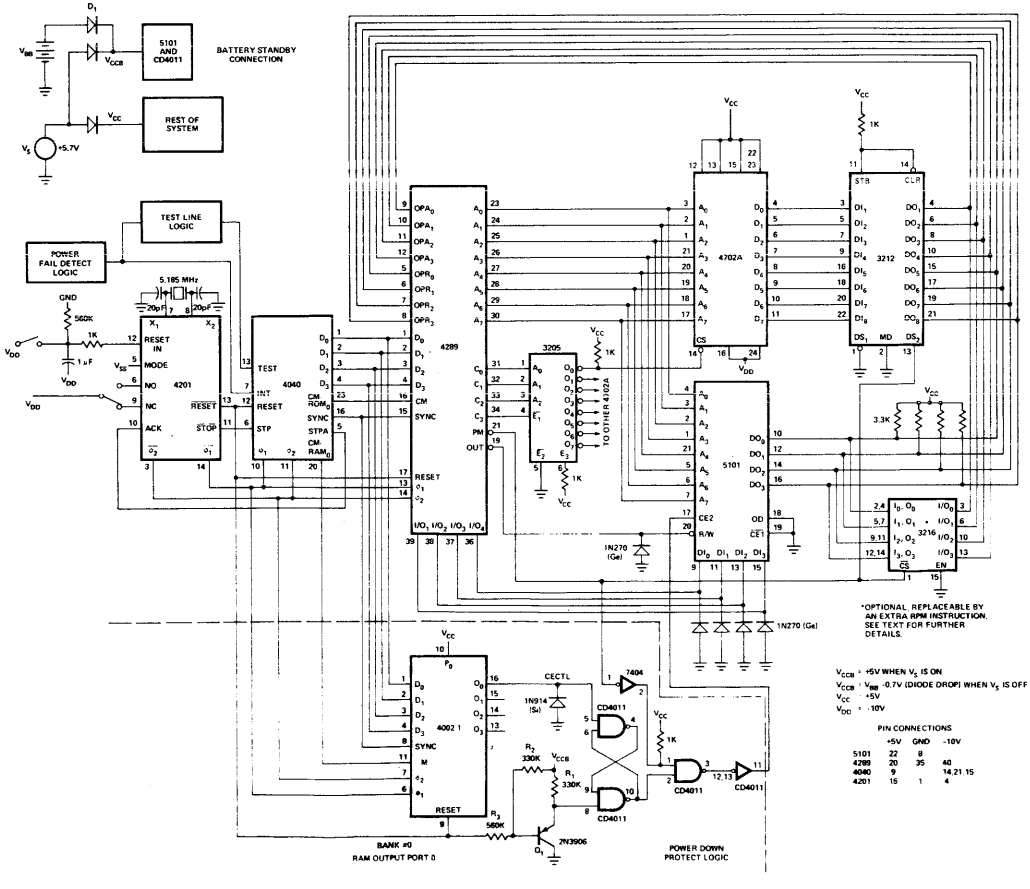


Figure 2. 4040 and 5101 Block Diagram

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