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AP-615

APPLICATION NOTE

Accommodating Industry Trends in Boot Code Flash Memory

COLLIN K. ONG
TECHNICAL MARKETING ENGINEER
DEBORAH SEE
FLASH SOFTWARE ENGINEER

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1.0 INTRODUCTION

The boot code for microprocessor-based systems have traditionally been stored in a ROM or PROM device. Because of the increasing need to update system boot code during the development process and after a product is in end-user hands, flash memory has become the ideal solution for storing system boot code. First generation flash memory products (also called bulk-erase or bulk-array flash) modeled after ROMs contain a single unsegmented address space which can only be erased all at once. Next generation flash components introduced segmented address spaces so that individual blocks could be erased independently of the others. This development facilitates flash memories with block sizes optimized for a particular application.

For the boot code application, Intel introduced their high-integration boot block flash architecture, with block sizes selected to reduce memory component redundancy within a system and to provide security for system boot code. Products in this architecture are 28F200/400 for 2-Mbit/4-Mbit parts that are x8/x16 bus width switchable and 28F002/004 for parts with only a x8 bus width.

Several other manufacturers now offer flash components with similar architectures, but some minor variations. Accommodating these differences in a single socket requires a design to address several issues, including intelligent identifiers, packages and pinouts, command sequences and some feature differences in blocking and block locking. These differences and some possible resolutions will be discussed in this paper, which will focus mainly on the Intel 28F200/400 and the AMD 29F200/400 and 29F040, though most of the concepts discussed can be applied to the rest of Intel's boot block products and corresponding devices from other manufacturers.

2.0 INTELLIGENT IDENTIFIERS

Intelligent ID codes allow a design to determine a flash component's manufacturer and the model of the component, which allows the software to decide which erase and program command sequences and algorithms to use. These codes can be read using both hardware and software methods. Intel and AMD components use the same hardware method for reading identifier information: taking A_9 to a high voltage (about 12V). Both manufacturers also provide software command sequences for reading identifier information. While these sequences are different, they are easily accommodated with a modified software routine.

Figure 1 shows an algorithm that can distinguish between Intel and AMD components, providing interface commands applicable to most AMD and Intel components. Validate these commands using the datasheets for the specific components in use. Command sequences for other flash vendors can also be substituted as appropriate.

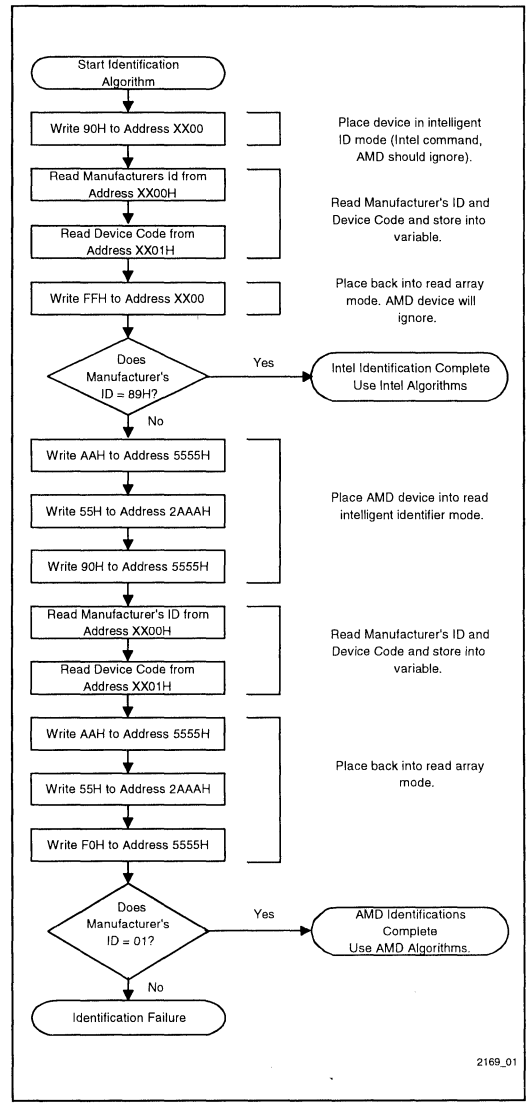

Figure 1. Example ID Algorithm

3.0 PACKAGES AND PINOUTS

Intel 28F200/400 and AMD 29F200/400 flash components have two packages in common: 44-lead PSOP and 48-lead TSOP. In these common packages, the Intel and AMD pinouts have only minor differences. Intel does not offer any of the packages of AMD 29F040, but Section 3.1 discusses dual site layouts for this situation.

3.1 44-Lead PSOP

In this package, the primary differences between the AMD and Intel pinouts are the additional V_{PP} and WP# pins on the Intel component, and the RY/BY# pin on the AMD component. Figure 2 shows the two pinouts and Table 1 summarizes the differences between the components:

Table 1. 44-Lead PSOP Pinout Differences

Pin	Intel Pin	AMD Pin	Description
1	V_{PP}	NC	Program/Erase Power
2	WP#	RY/BY#	Write Protect Input (Intel) / Ready/Busy Signal (AMD)

To accommodate Intel 28F200/400 and AMD 29F200/400 parts in a single 44-lead PSOP socket, at least one jumper is necessary. Jumper Pin 2 to switch between the write protect function for Intel and the ready/busy output for AMD. When using Intel 28F200/400 parts, this jumper must connect pin 2 to a control signal, ground, or V_{CC} (not floated), to control the boot block lock status. (See Section 6.1) When using AMD 29F200/400 parts, the jumper should connect the flash chip's RY/BY# output to the system. Note that since the Intel 28F200/400 devices do not have the ready/busy function, the status register should be used to check device status, or AMD's ready/busy function not used.

The other pinout difference is pin 1, V_{PP} for Intel and NC (No Connection) for AMD. This pin should be connected to a 5V or 12V supply (for Intel SmartVoltage 28F200/400BV components) or 12V (for Intel 28F200/400BX/BL parts). Another jumper can be used to prevent power from reaching the AMD device's NC pin, if additional safety is desired.

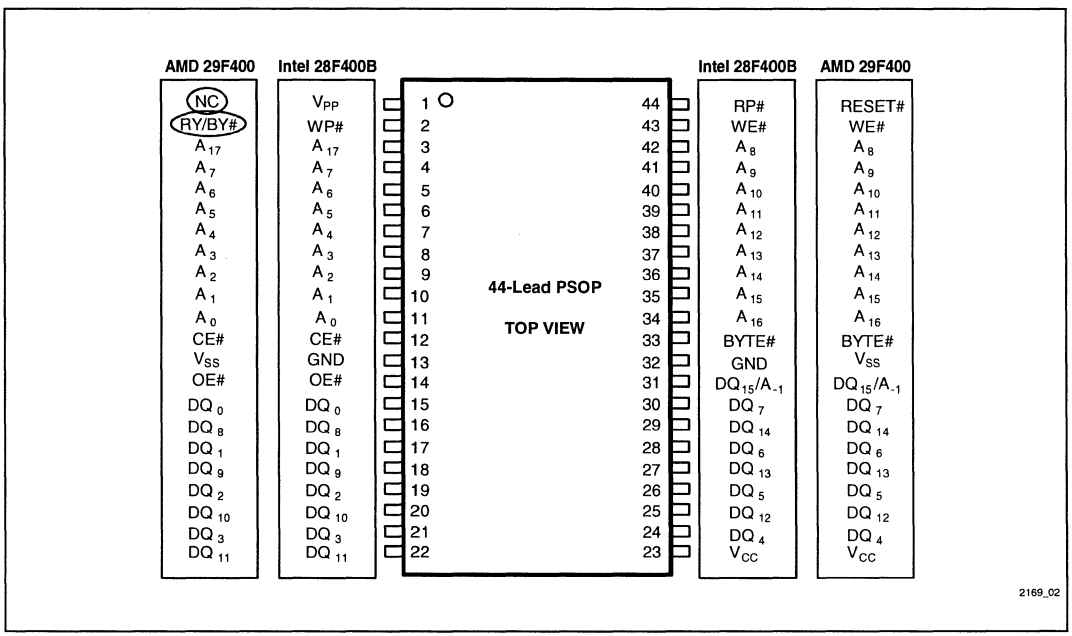

Figure 2. Pinout Comparison between AMD 29F400T/B and Intel 28F400-T/B 44-Lead PSOP

3.2 48-Lead TSOP

In this package, the AMD pinout can be considered a subset of the Intel pinout. The primary differences between the AMD and Intel pinouts are the additional V_{PP} and WP# pins on the Intel component, and the RY/BY# pin on the AMD component. Figure 3 shows the two pinouts.

All pins that differ between the components are not connected on the other device. The following table summarizes the pinout differences between the two components:

Table 2. 48-Lead TSOP Pinout Differences

Pin	Intel Pin	AMD Pin	Description
13	V_{PP}	NC	Program/Erase Power
14	WP#	NC	Write Protect Pin
15	NC	RY/BY#	Ready/Busy Output

To accommodate Intel 28F200/400 and AMD 29F200/400 parts in a common 48-lead TSOP socket, no jumpers are necessary. Pin 14, WP# on the Intel device, should connect to a control signal, ground, or V_{CC} (not floated), in order to control the locking status of the boot block (See Section 6.1). Since Pin 14 is NC on the AMD device, these signals should have no effect on it.

Pin 15 should connect the flash chip's RY/BY# output to the system. Note that since the Intel 28F200/400 devices do not have the ready/busy function the status register should be used to check status, or AMD ready/busy function not used.

The other pinout difference is pin 13: V_{PP} for Intel and NC (No Connection) for AMD. This pin should be connected to a 5V or 12V supply (for Intel SmartVoltage 28F200/400BV components) or 12V (for Intel 28F200/400BX/BL parts). Another jumper can be used to prevent power from reaching the AMD device's NC pin, if additional safety is desired.

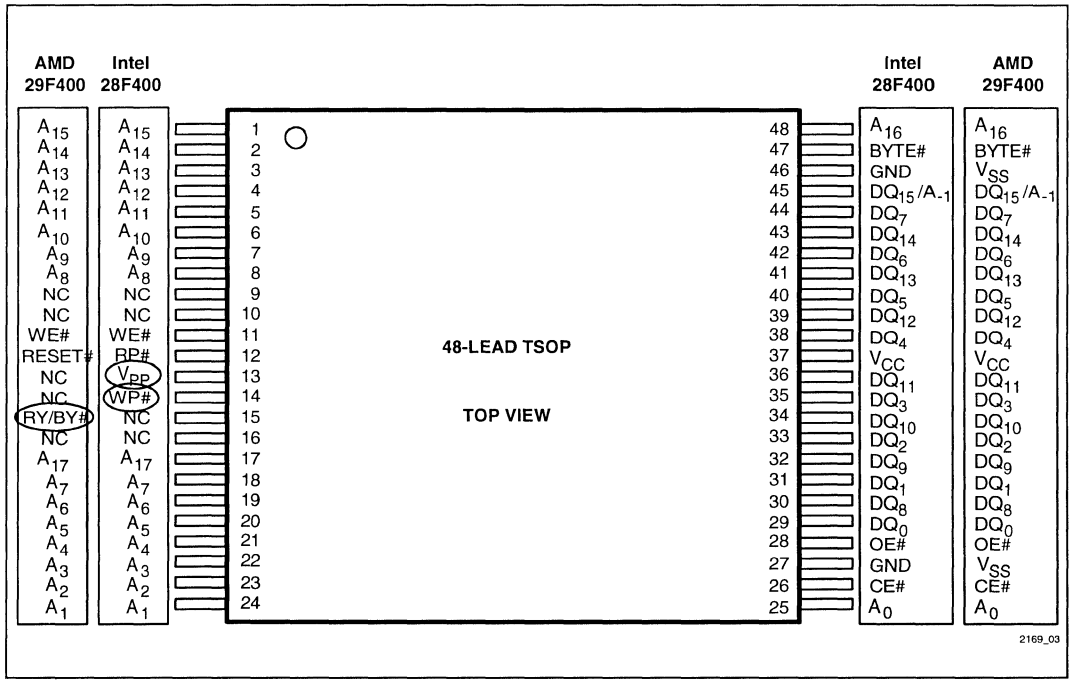

Figure 3. Pinout Comparison between AMD29F400 and Intel 28F400B 48-Lead TSOP

3.3 Dual Site Layouts

In some cases, a design may wish to accommodate both Intel 28F004/400B along with AMD 29F040 in a dual site layout. This poses several problems, since these components do not share any packages or pinouts in common. In addition, the 29F040 has a symmetrically-blocked address space, while the Intel 28F004/400B has an asymmetrically-blocked architecture. Solving these blocking differences are discussed in Section 4.2, and the software differences in Section 2.0.

The following space-efficient, dual site layouts accommodate Intel's 40-lead TSOP and 44-lead PSOP along with AMD's 32-lead PLCC and 32-lead TSOP. Only layer 1 (of 2) is shown in these illustrations. Gerber files for these layouts are available on the Intel BBS for easy insertion in your design (filenames given in parentheses; locator info and files not shown listed at end of document).

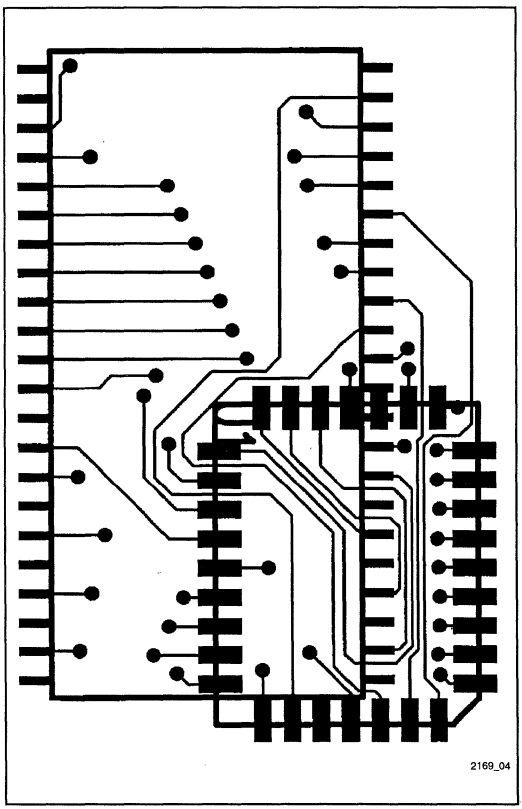

Figure 4. Intel 44-Ld PSOP and AMD 32-Ld PLCC (AMN32P44)

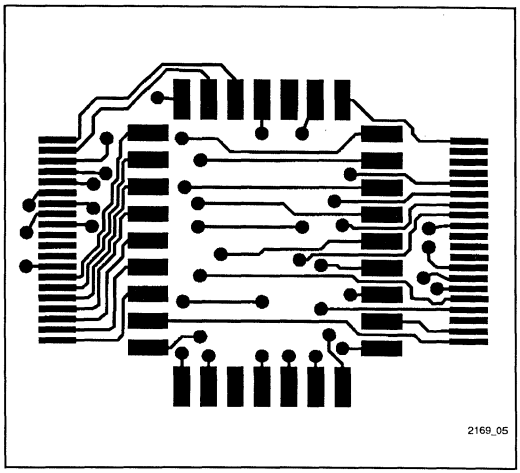

Figure 5. Intel 40-Ld TSOP and AMD 32-Ld PLCC (AMN32E40)

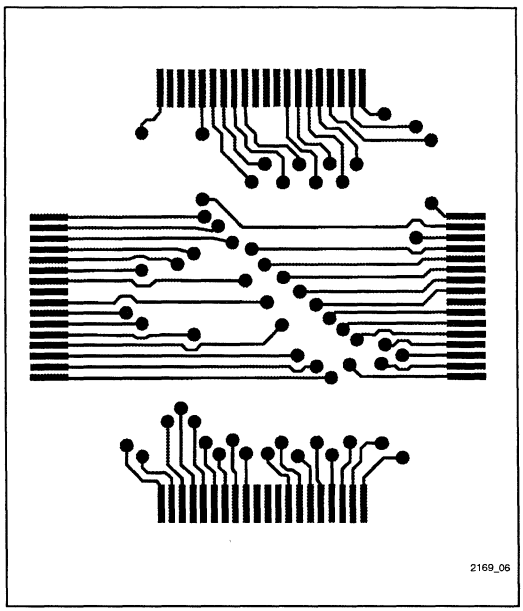

Figure 6. Intel 40-Ld TSOP and AMD 32-Ld TSOP (AME32E40)

4.0 BLOCK ARCHITECTURES

Intel currently offers asymmetrically blocked flash components in the mid-density range (about 2- to 4-Mbits) with its high-integration boot block line (the 28Fx00/00xB model numbers). AMD offers similarly asymmetrically block components (29Fx00) as well as symmetrically blocked components (29F0x0) in this density range.

4.1 Asymmetrical Blocking

The high-integration boot block flash architecture incorporates three types of blocks with different purposes:

1. The 16-Kbyte boot block is intended to replace a dedicated boot PROM in a microprocessor-based system and features hardware controllable write-protection for the crucial boot code.
2. Two 8-Kbyte parameter blocks facilitate storage of frequently updated small parameters normally stored in an EEPROM. (See AP-604)
3. Main blocks which divide the remaining space into 128-Kbyte segments for data or code storage.

The erase blocking architectures for Intel and AMD's respective asymmetrically blocked devices are slightly different. Intel's blocking scheme can be thought of as the memory space divided into 128-Kbyte blocks, with one block (at the top or bottom) further subdivided into a 16-Kbyte lockable boot block, two 8-Kbyte parameter blocks and one 96-Kbyte block. AMD's blocking scheme can be thought of as the memory space divided into 64-Kbyte blocks, with one block (at the top or bottom) further subdivided into a 16-Kbyte boot block, two 8-Kbyte parameter blocks and one 32-Kbyte block. These memory maps are compared in Figure 7.

The differences in blocking will impact the amount of code that can be erased at one time. The software designer should ensure that the code modules can be erased according to the Intel erase blocking, since the AMD block sizes can be grouped together to make up Intel block sizes. Programming of the devices are not affected by the block sizes, because data can be programmed across block boundaries.

Firmware for the AMD device to emulate the Intel blocking style should map the smaller AMD blocks to each Intel block, and erase two AMD blocks for each Intel block. For example, if the firmware is requested to erase the 96-Kbyte main block of an Intel device, it should erase the 32-Kbyte and neighboring 64-Kbyte block when using the AMD device.

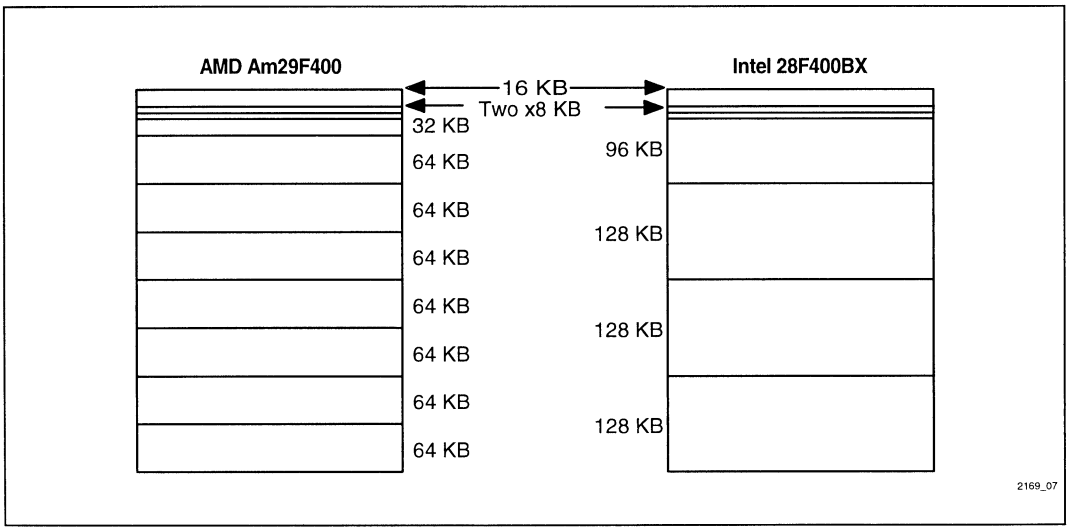

Figure 7. Erase Blocking Differences

4.2 Symmetrical Blocking

Another set of differences arise when switching from symmetrically-blocked flash such as the AMD 29F040 to asymmetrically-blocked flash, such as the Intel 28F400/004. These differences lie in the way block erases are handled, block sizes, and hardware control of the boot block.

The asymmetrically-blocked boot block architecture includes a hardware-lockable boot block for secure storage and two parameter blocks for parameter storage. If these features are not desired, these blocks can be combined with the first main block to provide an effective 128-Kbyte "Special" block, making the device architecture appear symmetrically blocked in 128-Kbyte segments. Implementing this requires modification of the following tasks: block erase handling, block size handling, and the hardware interface.

The virtual combination of the boot block, parameter block, and small main block into a single 128-Kbyte block is carried out in the erase algorithm. Figure 8 illustrates how the "Special" block is treated in the erase algorithm. This algorithm erases all four blocks in the "Special" block if any block within receives an erase command, effectively making those four blocks function as a single 128-Kbyte block.

Another issue to resolve is the locking feature on the 16-Kbyte block of the Intel boot block component, which prevents the boot block from being written or erased unless unlocked by a signal on the WP# or RP# pins. For this component to be treated as a symmetrically blocked component, the boot block must be either permanently unlocked or the controlling software must unlock that block with a hardware signal whenever an erase to the "Special" block occurs. Intel –BX/BL suffix parts require 12V on the RP# pin to unlock the boot block. SmartVoltage –BV/CV suffix products, include a WP# pin for unlocking the boot block with a logic-level signal. (See Section 6.1)

5.0 COMMAND SEQUENCES

The command sequences for different manufacturers have several basic differences which make development of a common algorithm difficult. However, because these are generally controlled by software, multiple command sequences can be incorporated without difficulty and switched between using the identification procedures discussed in Section 2.0. Refer to each manufacturer's datasheets for the specific program and erase commands and procedures.

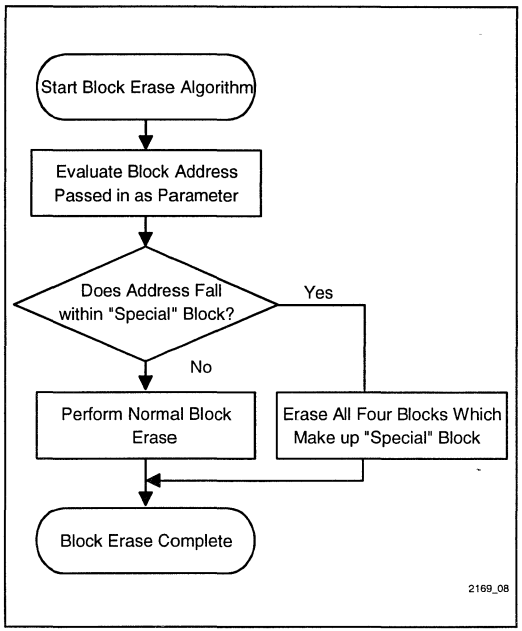

Figure 8. Erase Algorithm for Making Boot Block Symmetrical

6.0 BLOCK LOCKING

Block locking protects certain blocks from being altered by any command sequence, although the proper sequences could alter other blocks that are not locked. Block locking protects the data integrity of locked blocks from commands that make it through any implemented write protection methods.

Intel's boot block locking and AMD's block locking are implemented in different manners, which will impact the way "hardware" data protection is implemented.

6.1 Intel Flash Block Locking

Intel boot block devices support hardware-controlled locking of the boot block, but do not provide locking control for any of the other blocks. However, an address decoding scheme can be implemented such that addresses in "locked" sectors would turn V_{PP} on/off, providing locking for those blocks.

Tables 3 and 4 summarize the locking controls for the BX/BL and SmartVoltage BV/CV components, respectively. For the BX/BL products, locking is controlled using the V_{PP} and RP# pins. The BV/CV products provide an additional WP# pin to allow logic-level control of boot block locking.

Table 3. Locking Summary for BX/BL Parts

V_{PP}	RP#	Block Locking Provided
V_{IL}	X	All Blocks Locked
$\geq V_{PPLK}$	V_{IL}	All Blocks Locked (Reset)
$\geq V_{PPLK}$	V_{HH}	All Blocks Unlocked
$\geq V_{PPLK}$	V_{IH}	Boot Block Locked

Table 4. Locking Summary for BV/CV Parts

V_{PP}	RP#	WP#	Block Locking Provided
V_{IL}	X	X	All Blocks Locked
$\geq V_{PPLK}$	V_{IL}	X	All Blocks Locked (Reset)
$\geq V_{PPLK}$	V_{HH}	X	All Blocks Unlocked
$\geq V_{PPLK}$	V_{IH}	V_{IL}	Boot Block Locked
$\geq V_{PPLK}$	V_{IH}	V_{IH}	All Blocks Unlocked

6.2 AMD Block Locking

AMD's 29F040/400 devices support locking of any combination of the erase blocks in the device, but the locking procedure requires 12V. The locking and unlocking algorithms (see AMD datasheets for specific algorithms) are similar to the manual algorithms used by first-generation bulk-array flash products, and require a 12V supply to be multiplexed onto address and control lines. AMD's datasheet states: "However, multiplexing high voltage onto the address lines is not generally desired system practice." System overhead such as pulse counts and timings need to be tracked by the system when using these algorithms.

The blocks marked for locking can be temporarily unlocked by raising the RESET# pin to 12V, similar to one of the unlocking procedures using RP# on Intel boot block flash devices.

7.0 AC/DC SPECIFICATIONS

While the major architectural differences between Intel and AMD flash devices have been discussed in this document, these devices differ in many other specification differences which system designers should account for in a dual design. A few key issues will be noted here, however.

7.1 DC Characteristics

The power (current) requirements are comparable between the Intel and AMD devices; however, when comparing current specifications, take note of the test conditions, especially the read frequency. Current specs should be compared at the actual read frequency for the system. This can be calculated by inverting the read access time of the system. To equalize read frequencies between components, use the approximate rule for Intel components that I_{CC} read current is related to frequency by 4 mA/MHz, so for every increase of 1 MHz of read frequency, read current increases 4 mA. Correspondingly, a decrease of 1 MHz in read frequency reduces read current by 4 mA.

7.2 AC Characteristics

Designers should compare timing specifications and accommodate any differences for a dual site layout. In particular, Intel boot block devices latch both addresses and data on the rising edge of the controlling WE# or CE# signal, while AMD latches addresses on the falling edge and data on the rising edge.

8.0 SUMMARY

This document discusses many of the issues which will need attention when using Intel and AMD flash in the same design. The following summary table indicates which of the measures (with section numbers referenced) are necessary for each Intel and AMD product/package combinations. The first row of the table shows those measures that are necessary for all of the Intel/AMD combinations, and the following rows indicate the additional measures necessary for each specific combination.

Table 5. Cross-Reference of Required Compatibility Measures by Component Combination

Component Combination	Required Measures
All Intel and AMD Combinations	Intelligent Identifiers (2.0)
	Command Sequences (5.0)
	Block Locking (6.0)
	AC/DC Specifications (7.0)
Intel 28F200, 28F400, 28F800 (44-PSOP or 48-TSOP) and	44-Lead PSOP (3.1) or 48-Lead TSOP (3.2)
AMD 29F100, 29F200, 29F400 (44-PSOP or 48-TSOP)	Asymmetrical Blocking (4.1)
Intel 28F200, 28F400 (44-PSOP) and	Dual Site Layouts (3.3, Figure 4)
AMD 29F010, 29F040 (32-PLCC)	Symmetrical Blocking (4.2)
Intel 28F002B, 28F004B, 28F008B (40-TSOP) and	Dual Site Layouts (3.3, Figure 5)
AMD 29F010, 29F040 (32-PLCC)	Symmetrical Blocking (4.2)
Intel 28F002B, 28F004B, 28F008B (40-TSOP) and	Dual Site Layouts (3.3, Figure 6)
AMD 29F010, 29F040 (32-TSOP)	Symmetrical Blocking (4.2)

9.0 ADDITIONAL INFORMATION

9.1 Documentation

Order Number	Title
290531	2-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet
290530	4-Mbit SmartVoltage Boot Block Flash Memory Family Datasheet
292148	AP-604, "Using Intel's Boot Block Flash Memory Parameter Blocks to Replace EEPROM"
292159	AP- 607, "Multi-Site Layout Planning with Intel's FlashFile™ Components, Including ROM Compatibility"

9.2 Electronic Files

Title/Description (self-extracting)	**Location**
AMN32E40.EXE: AMD 29F0x0 32-PLCC to Intel 28F00xB 40-TSOP Layout file	**BBS:** (916) 356-3600 / Flash Boot Block Layout Area
AME32E40.EXE: AMD 29F0x0 32-TSOP to Intel 28F00xB 40-TSOP Layout file	**BBS:** (916) 356-3600 / Flash Boot Block Layout Area
AMN32P44.EXE: AMD 29F0x0 32-PLCC to Intel 28Fx00B 44-PSOP Layout file	**BBS:** (916) 356-3600 / Flash Boot Block Layout Area
BKN32E40.EXE: Bulk 28F0x0 32-PLCC to Intel 28F00xB 40-TSOP Layout file	**BBS:** (916) 356-3600 / Flash Boot Block Layout Area
BKN32P44.EXE: Bulk 28F0x0 32-PLCC to Intel 28Fx00B 44-PSOP Layout file	**BBS:** (916) 356-3600 / Flash Boot Block Layout Area

9.3 Revision History

Number	**Description**
001	Original Version

UNITED STATES, Intel Corporation
2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052-8119
Tel: (408) 765-8080

JAPAN, Intel Japan K.K.
5-6 Tokodai, Tsukuba-shi, Ibaraki-ken 300-26
Tel: 0298-47-8511

FRANCE, Intel Corporation S.A.R.L.
1, Rue Edison, BP 303, 78054 Saint-Quentin-en-Yvelines Cedex
Tel: (33) (1) 30 57 70 00

UNITED KINGDOM, Intel Corporation (U.K.) Ltd.
Pipers Way, Swindon, Wiltshire, England SN3 1RJ
Tel: (44) (0793) 696000

GERMANY, Intel GmbH
Dornacher Strasse 1
8016 Feldkirchen bei Muenchen
Tel: (49) 089/90992-0

HONG KONG, Intel Semiconductor Ltd.
32/F Two Pacific Place, 88 Queensway, Central
Tel: (852) 844-4555

CANADA, Intel Semiconductor of Canada, Ltd.
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Rexdale, Ontario M9W 6H8
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