82546GB/EB and 82545GM/EM Gigabit Ethernet Controller EEPROM Map and Programming Information

Revision 1.7
March 2009

Contents

Revision History

Revision	Revision Date	Description
1.7	Mar 2009	• Updated Table 12.
1.6	Sept 2008	• Change device ID from FF63h to 7863h.
1.5	June 2005	• Added the 82545GM and 82545EM EEPROM mapping, word, and bit descriptions. • Removed all references to the EEEdit utility.
1.2	Jan 2005	• Updated Word 13h/23h (Table 7, Bits 15:13, Bits 9:8, and Bit 2) to reflect current Initial Management Control Register settings.
1.1	Dec 2004	• Updated to match the 8254x Family of Gigabit Ethernet Controllers Software Developer's Manual.
1.0	Sept 2004	• Released as White Cover Confidential (WCC). • Updated Table 12, "LED Configuration Defaults". Added/updated bit assignments for LED0_MODE, LED1_MODE, LED2_MODE, and LED3_MODE. • Added Table 13, "MODE Encodings for Selecting an LED Signal Source for an LED Output".
.9	August 2004	Initial release (Intel Secret)

1.0 Introduction and Scope

The 82546GB/EB and 82545GM/EM Gigabit Ethernet controllers use an EEPROM device for storing product configuration information. The EEPROM is divided into four general regions:

- **Hardware accessed** – loaded by the Ethernet controller after power-up, PCI Reset deassertion, D3->D0 transition, or software commanded EEPROM reset (CTRL_EXT.EE_RST).
- **ASF accessed** – loaded by the Ethernet controller in ASF mode after power-up, ASF Soft Reset (ASF FRC_RST), or software commanded ASF EEPROM read (ASF FRC_EELD).
- **Software accessed** – used by software only. The meaning of these registers as listed here is a convention for the software only and is ignored by the Ethernet controller.
- **External BMC (TCO) accessed** – loaded by external BMC (TCO) from SMBus in pass-through mode after power up.

Several words of the EEPROM are accessed automatically by the Ethernet controller after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the stored information is available to software for storing the MAC address, serial numbers, and additional configuration information.

Intel has a software utility called EEUPDATE that can be used to program EEPROM images in development or production line environments. To obtain a copy of this program, contact your Intel representative.

Note: Since the **82546GB/EB** are dual port devices, there are portions of the EEPROM and Flash that control one or both ports. Special considerations due to this feature are noted in this section.

Unless otherwise specified, all numbers in this document use the following numbering convention:

- Numbers with a suffix of “b” are binary (base 2).
- Numbers that do not have a suffix are decimal (base 10).
- Numbers with a suffix of “h” are hexadecimal (base 16).

1.1 Component Identification Via Programming Interface

Ethernet controller stepping is identified by the following register contents.

Table 1. Component Identification

Stepping	Vendor ID	Device ID	Description
82546GB	8086h	1079h	Copper; Dual Port
82546GB	8086h	107Ah	Fiber; Dual Port
82546GB	8086h	107Bh	SerDes; Dual Port
82546EB	8086h	1010h	Copper; Dual Port
82546EB	8086h	1012h	Fiber; Dual Port

Table 1. Component Identification

Stepping	Vendor ID	Device ID	Description
82545GM-B	8086h	1026h	Copper; MAC Default
82545GM-B	8086h	1027h	Fiber
82545GM-B	8086h	1028h	SerDes
82545EM-A	8086h	100Fh	Copper
82545EM-A	8086h	1011h	Fiber

Note: These Ethernet controllers also provide identification data through the Test Access Port (TAP).

1.2 EEPROM Device and Interface

The EEPROM access algorithm, programmed into the Ethernet controller, is compatible with most, but not all, commerically available 3.3 V dc Microwire* interfaces and serial EEPROM devices with a 1 MHz speed rating. The Ethernet controller is compatible with two sizes of 4-wire serial EEPROM devices. If ASF mode functionality is desired, a 4096-bit serial NM93C66 compatible EEPROM can be used. Otherwise, a 1024-bit serial NM93C46 compatible EEPROM can be used. Both EEPROMs are accessed in 16-bit words; the larger has 256 words while the smaller has 64 words.

The Ethernet controller automatically determines which EEPROM it is connected to and sets the EEPROM SIZE field of the EEPROM/FLASH Control and Data Register (EEC.EE_SIZE) field appropriately. Software can use this field to determine how to access the EEPROM using direct access. Note that different EEPROM sizes have different numbers of address bits and therefore must be accessed with a slightly different serial protocol. Software must be aware of this if it accesses the EEPROM using direct access.

The EEPROM interface trace routing is not critical because the interface runs at a very slow speed.

1.3 Software Access

The Ethernet controller provides two different methods for software access to the EEPROM. Software can either use the built-in controller to read the EEPROM, or access the EEPROM directly using the EEPROM's 4-wire interface.

Software can use the EEPROM Read register (EERD) to cause the Ethernet controller to read a word from the EEPROM that the software can then use. To do this, software writes the address to read the Read Address (EERD.ADDR) field and then simultaneously writes a 1b to the Start Read bit (EERD.START). The Ethernet controller then reads the word from the EEPROM, sets the Read Done bit (EERD.DONE), and puts the data in the Read Data field (EERD.DATA). Software can poll the EEPROM Read register until it sees the Read Done bit set, then use the data from the Read Data field. Any words read this way are not written to hardware's internal registers.

Software can also directly access the EEPROM's 4-wire interface through the EEPROM/FLASH Control Register (EEC). It can use this for reads, writes, or other EEPROM operations.

To directly access the EEPROM, software should follow these steps:

1. Write a 1b to the EEPROM Request bit (EEC.EE_REQ).
2. Read the EEPROM Grant bit (EEC.EE_GNT) until it becomes 1b. It remains 0b as long as the hardware is accessing the EEPROM.
3. Write or read the EEPROM using the direct access to the 4-wire interface as defined in the EEPROM/FLASH Control & Data Register (EEC). The exact protocol used depends on the EEPROM placed on the board and can be found in the appropriate data sheet.
4. Write a 0b to the EEPROM Request bit (EEC.EE_REQ).

Software can cause the Ethernet controller to re-read the hardware accessed fields of the EEPROM (setting hardware's internal registers appropriately) by writing a 1b to the EEPROM Reset bit of the Extended Device Control Register (CTRL_EXT.EE_RST).

1.4 Signature and CRC Fields

The Ethernet controller uses the Signature and CRC fields to determine if an EEPROM is present by attempting to read the EEPROM. The Ethernet controller first reads the Initialization Control Word 1 at address 0Ah and then checks the received value for bits 15 and 14. If bit 15 is 0b and bit 14 is 1b, the Ethernet controller considers the EEPROM to be present and valid. It then reads the additional EEPROM words and programs its internal registers based on the values read. Otherwise, it ignores the values it read from the Initialization Control Word 1 and does not read any other words.

In ASF Mode, the Ethernet controller's ASF function reads the ASF CRC word to determine if the EEPROM is valid. If the CRC is not valid, the ASF Configuration registers retain their default value. This CRC does not affect any of the remaining Ethernet controller's configuration, including the Management Control Register.

1.5 EEUPDATE Utility

Intel has created a utility that meets the two basic requirements for an in-circuit programming utility. First, the utility can be used to update EEPROM images as part of an end-of-line production tool. Secondly, it can be used as a standalone development tool. The tool uses the two basic data files outlined in the following section (static data file and IA address file). To obtain a copy of this program, contact your Intel representative.

The EEUPDATE utility is flexible and can be used to update the entire EEPROM image or update only the IA address of the Ethernet controller.

1.5.1 Command Line Parameters

The DOS command format is a follows:

```
EEUPDATE Parameter_1 Parameter_2
```

where:

```
Parameter_1 = filename or /D

Parameter_2 = filename or /A
```

`Parameter 1`, in this example case, is `file1.eep`, which contains the complete EEPROM image in a specific format that is used to update the complete EEPROM. All comments in the `.eep` file must be preceded by a semicolon (;).

`Parameter 1` can also be a switch /D. the switch /D implies: do not update the complete EEPROM image.

`Parameter 2`, in this example case, is `file2.dat`, which contains a list of IA addresses. the EEUPDATE utility picks up the first unused address from this file and uses it to update the EEPROM. An address is marked as used by following the address with a date stamp. When the utility uses a specific address, it updates that address as used in a log file called eelog.dat. This file should then be used as the `.dat` file for the next update.

`Parameter 2` can also be a switch: /A. The switch /A implies, do not update the IA address.

Note: See Appendix A for an example of the raw EEPROM images.

2.0 EEPROM Address Map

The following table lists the EEPROM address map for the Gigabit Ethernet controllers. Each word listed is described in the sections that follow.

The “LAN A/B” column in Table 2 is only applicable to the 82546GB/EB.

Table 2. Ethernet Controller Address Map

Word	Used By	Bit 15 - 8	Bit 7 - 0	Image Value	LAN A/B
00h 01h 02h	HW HW HW	Ethernet Address Byte 2 Ethernet Address Byte 4 Ethernet Address Byte 6[a]	Ethernet Address Byte 1 Ethernet Address Byte 3 Ethernet Address Byte 5	IA(2,1) IA(4,3) IA(6,5)	LAN A/B (both)
03h		Compatibility High	Compatibility Low	0000h	both
04h	SW	SERDES Configuration		FFFFh	both
05h 06h 07h		Compatibility High	Compatibility Low	0000h 0000h 0000h	both
08h 09h		PBA, byte 1 PBA, byte 3	PBA, byte 2 PBA, byte 4		
0Ah	HW	Init Control 1		4408h	both
0Bh	HW	Subsystem ID (Vendor)		See Table 1 for specific image values	both
0Ch	HW	Subsystem Vendor ID		8086h	both
0Dh	HW	Device ID		See Table 1 for specific image values	LAN A
0Eh	HW	Vendor ID		8086h	both
0Fh	HW	Init Control 2		3040h	both
10h	HW	Software Defined Pins Control (**82546GB**/**EB** only) **Note:** Words 10h, 11h, and 13h through 1Fh are reserved for the **82545G**/**EM**)		XXXXh	LAN B
11h	HW	Device ID			LAN B
12h	HW		Common Power		both
13h	HW	Management Control			LAN B
14h	HW	Init Control 3	SMBus Address[b]	XXXXh	LAN B
15h 16h	HW	IPv4 Address Byte 2 IPv4 Address Byte 4	IPv4 Address Byte 1 IPv4 Address Byte 3	IP(2,1) IP(4,3)	LAN B

Table 2. Ethernet Controller Address Map

Word	Used By	Bit 15 - 8	Bit 7 - 0	Image Value	LAN A/B
17h 18h 19h 1Ah 1Bh 1Ch 1Dh 1Eh	HW	IPv6 Address Byte 2 IPv6 Address Byte 4 IPv6 Address Byte 6 IPv6 Address Byte 8 IPv6 Address Byte 10 IPv6 Address Byte 12 IPv6 Address Byte 14 IPv6 Address Byte 16	IPv6 Address Byte 1 IPv6 Address Byte 3 IPv6 Address Byte 5 IPv6 Address Byte 7 IPv6 Address Byte 9 IPv6 Address Byte 11 IPv6 Address Byte 13 IPv6 Address Byte 15	IP(2,1) IP(4,3) IP(6,5) IP(8,7) IP(10,9) IP(12,11) IP(14,13) IP(16,15)	LAN B
1Fh		Reserved			
20h	HW	Software Defined Pins Control		XXXXh	LAN A
21h	HW	Circuit Control		7863h	both
22h	HW	D0 Power	D3 Power	280Ch	both
23h	HW	Management Control		XXC8h	LAN A
24h	HW	Init Control 3	SMBus Address[b]	XXXXh XXC8h (**82545GM/EM**)	LAN A
25h 26h	HW	IPv4 Address Byte 2 IPv4 Address Byte 4	IPv4 Address Byte 1 IPv4 Address Byte 3	IP(2,1) IP(4,3)	LAN A
27h 28h 29h 2Ah 2Bh 2Ch 2Dh 2Eh	HW	IPv6 Address Byte 2 IPv6 Address Byte 4 IPv6 Address Byte 6 IPv6 Address Byte 8 IPv6 Address Byte 10 IPv6 Address Byte 12 IPv6 Address Byte 14 IPv6 Address Byte 16	IPv6 Address Byte 1 IPv6 Address Byte 3 IPv6 Address Byte 5 IPv6 Address Byte 7 IPv6 Address Byte 9 IPv6 Address Byte 11 IPv6 Address Byte 13 IPv6 Address Byte 15	IP(2,1) IP(4,3) IP(6,5) IP(8,7) IP(10,9) IP(12,11) IP(14,13) IP(16,15)	LAN A
2Fh	HW	LEDCTL Default		0602h	both

Table 2. Ethernet Controller Address Map

Word	Used By	Bit 15 - 8	Bit 7 - 0	Image Value	LAN A/B
30h 31h 32h 33h 34h ... 3Eh	PXE	Intel Boot Agent Configuration **Note:** Words 34h and 35h are not applicable to the **82545GM/EM**			
3Fh		Software Checksum, words 00h through 3Fh			
40h ... F7h	ASF	Controlled by the ASF Agent			
F8h ... FFh		Free for Software			

a. The lower bit of the last byte is complemented for LAN B.
b. The SMBus Address is a 7-bit value that is found in bits 7 through 1 of this byte. Bit 0 should be 0b.

2.1 Ethernet Data Word Descriptions

The following sections detail each word listed in the EEPROM address map.

2.1.1 Ethernet Address (Words 00h-02h

The Ethernet Individual Address (IA) is a six-byte field that must be unique for each Ethernet port (and unique for each copy of the EEPROM image). The first three bytes are vendor specific. The value from this field is loaded into the Receive Address Register 0 (RAL0/RAH0). For a MAC address of 12-34-56-78-90-AB, words 2:0 load as follows (note that these words are byte-swapped):

Word 0 = 3412

Word 1 = 7856

Word 2 = AB90

Note: Since the **82546GB/EB** is a dual-port device, the Ethernet Address in these words are assigned to LAN A. The Ethernet Address for LAN B is the Ethernet Address for LAN A with its least significant bit inverted.

2.1.2 Software Compatibility Word (Word 03h)

This is the third word read by the Ethernet controller and contains additional initialization values that:

- Sets defaults for some internal registers
- Enables/disables specific features

Table 3. Software Compatibility Word (Word 03h)

Bit	Name	Description
15:12	Reserved	Reserved for future use.
11	LOM	LAN on Motherboard (LOM#). Set this bit to 1b (default) to enable LOM#; set to 0b to disable LOM#.
10	SRV	Server card. Set this bit to 1b (default) to enable server card; set to 0b to disable server card.
9	CLI	Client card. Set this bit to 0b (default) to disable client card; set to 1b to enable client card.
8	OEM	OEM card. Set this bit to 1b (default) to enable OEM card; set to 0b to disable OEM card.
7:6	Reserved	Reserved for future use.
5	Reserved	Set this bit to 1b.
4	SMB	SMBus. Set this bit to 1b (default) to enable SMBus; set to 0b to disable SMBus.
3	Reserved	Reserved for future use.
2	BOB	PCI bridge. Set this bit to 0b (default) to disable PCI bridge; set to 1b to enable PCI bridge.
1:0	Reserved	Reserved for future use.

2.1.3 SerDes Configuration (Word 04h)

If this word has a value of other than FFFFh, software programs its value into the Extended PHY Specific Control Register 2, located at address 26d in the PHY register space.

2.1.4 Compatibility Fields (Word 05h - 07h)

These areas are reserved for compatibility information and are used by software drivers.

2.1.5 PBA Number (Word 08h - 09h)

A nine-digit Printed Board Assembly (PBA) number, used for Intel manufactured adapter cards, are stored in a four-byte field. Other hardware manufacturers can use these fields as they wish. Network driver software should not rely on this field to identify the product or its capabilities.

2.1.6 Initialization Control Word 1 (Word 0Ah)

The first word read by the Ethernet controller contains initialization values that:

- Sets defaults for some internal registers
- Enables/disables specific features
- Determines which PCI configuration space values are loaded from the EEPROM

Table 4. Initialization Control Word 1 (Word 0Ah)

Bit	Name	Description
15:14	Signature	The Signature field represents a signature of 01b (default), indicating to the device that there is a valid EEPROM present. If the Signature field is not 01b, the other bits in this word are ignored, no further EEPROM read is performed, and default values are used for the configuration space IDs.
13	64/32 BAR	When set to 0b (default), enables 64-bit memory mapping. When set to 1b, disables 64-bit memory mapping.
12	IPS0	When set to 0b (default), does not invert the Power State Output bit 0 (CTRL_EXT[14]). When set to 1b, inverts the Power State Output invert bit 0 (CTRL_EXT[14]).
11	FRCSPD	Force Speed bit in the Device Control register (CTRL[11]). When set to 0b (default), does not force speed. When set to 1b, forces speed. For 10/100/1000 Mb/s systems using internal SerDes mode, set this bit to 0b.
10	FD	Full Duplex (mapped to CTRL[0] and TXCW[5]). When set to 1b (default), enables full duplex (internal SerDes mode only). When set to 0b, disables full duplex (internal SerDes mode only).
9	LRST	Link Reset (mapped to CTRL[3]). When set to 0b, enables Auto-Negotiation at power up or when asserting RST# without driver intervention. When set to 1b, disables Auto-Negotiation at power up or when asserting RST# without driver intervention.
8	IPS1	When set to 0b (default), does not invert the Power State Output bit 1 (CTRL_EXT[16]). When set to 1b, inverts the Power State Output invert bit 1 (CTRL_EXT[16]).
7:5	Reserved	Reserved for future use. Set these bits to 0b.
4	Reserved	Reserved for copper PHY. Set this bit to 0b.
3	Power Management	When set to 1b (default), enables full support for power management. When set to 0b, the Power Management Registers set is read only. The Ethernet controller does not execute a hardware transition to D3.

Table 4. Initialization Control Word 1 (Word 0Ah)

Bit	Name	Description
2	PME Clock	When set to 0b (default), indicates that the PCICLK is not required for PME# output. When set to 1b, indicates that the PCICLK is required for PME# output.
1	Load Subsystem IDs	When set to 1b (default), indicates that the Ethernet controller is to load its PCI Subsystem ID and Subsystem Vendor ID from the EEPROM (words 0Bh, 0Ch). When set to 0b, indicates that the Ethernet controller is to load the default PCI Subsystem ID and Subsystem Vendor ID.
0	Load Vendor/Device IDS	When set to 0b (default), indicates that the Ethernet controller is to load the default values for PCI Vendor and Device IDs. When set to 1b, indicates that the Ethernet controller is to load its PCI Vendor and Device IDs from the EEPROM (words 0Dh, 0Eh).

2.1.7 Subsystem ID (Word 0Bh)

If the signature bits (15:14) and bit 1 (Load Subsystem IDs) of word 0Ah are valid, this word is read in to initialize the Subsystem ID.

2.1.8 Subsystem Vendor ID (Word 0Ch)

If the signature bits (15:14) and bit 1 (Load Subsystem IDs) of word 0Ah are valid, this word is read in to initialize the Subsystem Vendor ID.

2.1.9 Device ID (Word 0Dh - 11h[1])

If the signature bits (15:14) and bit 1 (Load Subsystem IDs) of word 0Ah are valid, this word is read in to initialize the Subsystem ID.

For the **82546GB**, the Device ID must be forced to 107Bh for SerDes-SerDes interface operation. For the **82545GM**, the Device ID should be 1028h. This ensures proper functionality with Intel drivers and boot agent.

Note: Since the **82546GB/EB** are dual-port devices, the Device ID in 0Dh corresponds to LAN A and the Device ID in 11h corresponds to LAN B.

2.1.10 Vendor ID (Word 0Eh)

If the signature bits (15:14) and bit 1 (Load Subsystem IDs) of word 0Ah are valid, this word is read in to initialize the Subsystem ID.

1. Word 11h only applicable to the **82546GB/EB**.

2.1.11 Initialization Control Word 2 (Word 0Fh)

This is the second word read by the Ethernet controller and contains additional initialization values that:

- Sets defaults for some internal registers
- Enables/disables specific features

Table 5. Initialization Control Word 2 (Word 0Fh)

Bit	Name	Description
15	APM PME# Enable	Initial value of the Assert PME On APM Wakeup bit in the Wakeup Control Register (WUC.APMPME). When set to 0b (default), deasserts PME# on wakeup. Set this bit to 1b for Intel LAN controller cards.
14	ASDE	When set to 0b (default), indicates the initial value of the Auto-Speed Detection Enable (ASDE) bit of the Device Control Register (CTRL). When set to 1b, enables 10/100/1000 Mb/s systems.
13:12	PAUSE Capability	Pause Capability - Mapped to TXCW[8:7]. When set to 1b (default), enables desired PAUSE capability for an advertised configuration base page. When set to 0b, disables desired PAUSE capability for an advertised configuration base page.
11	ANE	Auto-Negotiation Enable. Mapped to TXCW[31]. Set this bit to 1b to automatically enable Auto-Negotiation. Set this bit to 0b (default) to automatically disable Auto-Negotiation. **Note:** Fiber implementations do not support this function.
10:9	FLASH Size Indication	Indicates FLASH size. 00b = 64 KB (default); 01b = 128 KB; 10b = 256 KB; 11b = 512 KB. These bits also impact the requested memory space for the FLASH and Expansion ROM BARs in PCI configuration space.
8	Reserved	Reserved for future use (set to 0b). Formerly FLASH Disable, now located in Initialization Control Word 3, bit 3.
7	MSI Disable	When set to 1b, disables Message Signalled Interrupts (MSI) in standard PCI mode. When set to 0b (default), enables Message Signalled Interrupts (MSI) in standard PCI mode.
6	133 MHz Capable	When set to 1b (default), maps the 133 MHz Capable bit of the PCI-X Status Register (PCIXS). When set to 0b, does not map the 133 MHz Capable bit of the PCI-X Status Register (PCIXS).
5	DMCR_Map	Indicates how the Designed Maximum Cumulative Read size bits in the PCI-X Status register are mapped. When set to 1b (default), the DMCR value reflects the hard-coded design capability as indicated by the Max_Read bit (bit 4). When set to 0b, the DMCR is mapped directly to the Maximum Memory Read Byte Count indicated in the PCI-X Command register.

Table 5. Initialization Control Word 2 (Word 0Fh)

Bit	Name	Description
4	Max_Read	Indicates the maximum read value as advertised in the Designed Maximum Memory Read Byte Count field in the PCI-X Status Register. When set to 0b (default), or if there is no EEPROM, the advertised maximum read is 2 KB. When set to 1b, the advertised maximum read is 4 KB. Note that it is not recommended to set Max_Read to 1b because transmit FIFO overruns are possible under specific operating conditions.
3	64-bit	When set to 1b (default), loads the 64-bit Device field of the PCI-X Status Register. When set to 0b, does not load the 64-bit Device field of the PCI-X Status Register.
2	Reserved	Reserved for future use. Formerly APM Enable, now located in Initialization Control Word 3, bit 2.
1	Force CSR Read Split	When set to 1b, forces all Ethernet controller control/status register-reads to be split when operating in a PCI-X environment. When set to 0b (default), certain critical registers are decoded for non-split access.
0	Reserved	Reserved for future use.

2.1.12 Common Power (Word 12h)

If the signature bits are valid and Power Management is not disabled, the value in this field is used in the PCI Power Management Data Register when the *Data_Select* field of the Power Management Control/Status Register (PMCSR) is set to 8. This setting indicates the power usage and heat dissipation of the common logic that is shared by both functions in tenths of a watt.

2.1.13 Software Defined Pins Control (Word 10h[1], 20h)

This field contains initial settings for the Software Defined Pins (SPD).

Table 6. Software Defined Pins Control (Word 10h, 20h)

Bit	Name	Description
15	SDPDIR[7]	SDP7 Pin - Initial Direction. Set this bit to 0b (default) to configure the initial hardware value of the SDP7_IODIR bit in the Extended Device Control Register (CTRL_EXT) following power up. Set this bit to 1b if not connected on a board or if used as an output.
14	SDPDIR[6]	SDP6 Pin - Initial Direction. Set this bit to 0b (default) to configure the initial hardware value of the SDP6_IODIR bit in the Extended Device Control Register (CTRL_EXT) following power up. Set this bit to 1b if not connected on a board or if used as an output.
13:10	Reserved	Set these bits to 0b.
9	SDPDIR[1]	SDP1 Pin - Initial Direction. Set this bit to 0b (default) to configure the initial hardware value of the SDP1_IODIR bit in the Extended Device Control Register (CTRL_EXT) following power up. Set this bit to 1b if not connected on a board or if used as an output.
8	SDPDIR[0]	SDP0 Pin - Initial Direction. Set this bit to 0b (default) to configure the initial hardware value of the SDP0_IODIR bit in the Extended Device Control Register (CTRL_EXT) following power up. Set this bit to 1b if not connected on a board or if used as an output.
7	SDPVAL[7]	SDP7 Pin - Initial Output Value. Set this bit to 0b (default) to configure the initial power-on value output on SDP7 (when configured as an output) by configuring the initial hardware value of the SDP7_DATA bit in the Extended Device Control Register (CTRL_EXT) after power up. Set this bit to 1b if used as an output.
6	SDPVAL[6]	SDP6 Pin - Initial Output Value. Set this bit to 0b (default) to configure the initial power-on value output on SDP6 (when configured as an output) by configuring the initial hardware value of the SDP6_DATA bit in the Extended Device Control Register (CTRL_EXT) after power up. Set this bit to 1b if used as an output.
5:4	Reserved	Set these bits to 0b.
3	EN_PHY_PWR_MGMT	Set this bit to 1b (default) to configure the initial hardware default value of this bit in the Device Control Register (CTRL) following power up. Set this bit to 0b to not configure the initial hardware default value of this bit in the Device Control Register (CTRL) following power up.

1. Applicable to the **82546GB/EB** only.

Table 6. Software Defined Pins Control (Word 10h, 20h)

Bit	Name	Description
2	D3COLD_WAKEUP_ADV_EN	Set this bit to 1b (default) to configure the initial hardware default value of the ADVD3WUC bit in the Device Control Register (CTRL) following power up. Set this bit to 0b to not configure the initial hardware default value of the ADVD3WUC bit in the Device Control Register (CTRL) following power up.
1	SDPVAL[1]	SDP1 Pin - Initial Output Value. Set this bit to 0b (default) to configure the initial power-on value output on SDP1 (when configured as an output) by configuring the initial hardware value of the SDP1_DATA bit in the Extended Device Control Register (CTRL_EXT) after power up. Set this bit to 1b if used as an output.
0	SDPVAL[0]	SDP0 Pin - Initial Output Value. Set this bit to 0b (default) to configure the initial power-on value output on SDP0 (when configured as an output) by configuring the initial hardware value of the SDP0_DATA bit in the Extended Device Control Register (CTRL_EXT) after power up. Set this bit to 1b if used as an output.

Note: Since the **82546GB/EB** are dual-port devices, the SDP control in 10h corresponds to LAN B, and the SDP control in 20h corresponds to LAN A.

2.1.14 Circuit Control (Word 21h)

This word is loaded into the Circuit Control Register for setting PCI-X driver strength. It should have a value of 7863h.

2.1.15 D0 Power (Word 22h high byte)

If the signature bits are valid and Power Management is not disabled, the value in this field is used in the PCI Power Management Data Register when the Data_Select field of the Power Management Control/Status Register (PMCSR) is set to 0 or 4. This indicates the power usage and heat dissipation of the networking function (including the Ethernet controller and any other devices managed by the Ethernet controller) in tenths of a watt. For example:

```
If word 22h = 290E, POWER CONSUMPTION (in 1/10 W, hex), then:

    Bits 15:8 = 29h Power in D0a, 29h = 4.1 W

    Bits 7:0 = 0Eh Power in D3h, 0Eh = 1.4 W
```

2.1.16 D3 Power (Word 22h low byte)

If the signature bits are valid and Power Management is not disabled, the value in this field is used in the PCI Power Management Data Register when the Data_Select field of the Power Management Control/Status Register (PMCSR) is set to 3 or 7. This indicates the power usage and heat dissipation of the networking function (including the Ethernet controller and any other devices managed by the Ethernet controller) in tenths of a watt as described in Section 2.1.15.

2.1.17 Management Control (Word 13h[1], 23h)

The following table lists the initial settings for the Management Control Register as well as valid bits for the IPv4 Address and the IPv6 Address.

Table 7. Initial Management Control Register Settings

Bit	Name	Description
15	Enable ARP Response Filtering	This bit controls the initial value of the *MANC.RSP_EN* bit. 0b: ARP response packets are delivered to host memory. 1b: ARP response packets are delivered to the Ethernet controller for automatic ARP reply or forwarded to the BMC.
14	Reserved	Reserved. Set this bit to 0b.
13	Enable ARP Request Filtering	This bit controls the initial value of the *MANC.ARP_EN* bit. 0b: ARP request packets are delivered to host memory. 1b: ARP request packets are delivered to the Ethernet controller for automatic ARP reply or forwarded to the BMC.
12:10	Reserved	Set these bits to 0b.
9	Enable RMCP 0298h Filtering	This bit is controlled by the ASF agent. Manually set this bit for TCO mode. Set this bit to 0b (default) to control the initial value of the *MANC.0298_EN* bit, which enables classifying UDP packets of port 0298h as Management Packets for delivery to the SMBus or ASF controller. Set this bit to 0b if the SMBus is disabled.
8	Enable RMCP 026F Filtering	This bit is controlled by the ASF agent. Manually set this bit for TCO mode. Set this bit to 1b (default) to control the initial value of the *MANC.0298_EN* bit, which enables classifying UDP packets of port 026Fh as Management Packets for delivery to the SMBus or ASF controller. Set this bit to 0b if the SMBus is disabled.
7	IPv6 Address Valid	IPv6 Address in the IP Address EEPROM register is valid. This is written to bit 16 of the IP Address Valid (IPAV[16]) register.
6	IPv4 Address Valid	IPv4 Address in the IP Address EEPROM register is valid. This is written to bit 0b of the IP Address Valid (IPAV[0]) register.
5:3	Reserved	Set these bits to 0b.

1. Applicable to the **82546GB/EB** only.

Table 7. Initial Management Control Register Settings

Bit	Name	Description
2	Reset on Force TCO	This bit is controlled by the ASF agent. Manually set this bit for TCO mode. Reset the Ethernet controller on a ForceTCO SMBus Command with the “Force” bit set to 1b (default) in TCO mode, or on various conditions in ASF mode. Set this bit to 0b if the SMBus is disabled.
1	ASF Mode	This bit is controlled by the ASF agent. Set this bit to 1b to enable ASF mode. Set this bit to 0b (default) for TCO mode and Intel’s ASF Agent implementation.
0	SMBus Enable	This bit is controlled by the ASF agent. Manually set this bit for TCO mode. Set this bit to 1b (default) to enable SMBus functionality. Set this bit to 0b to enable ASF mode if its being routed by LAN A and if LAN A is the active interface for ASF to the BIOS.

Note: Since the **82546GB/EB** are dual-port devices, the Management Control in 13h corresponds to LAN B, and the Management Control in 23h corresponds to LAN A.

2.1.18 SMBus Slave Address (Word 14h[1] low byte, 24h low byte)

The following table lists the SMBus slave address for TCO mode.

Table 8. SMBus Slave Address

Bit	Name	Description
7:1	SMBus Slave Address	These bits are controlled by the ASF agent. Manually set these bits for TCO mode. Contains the SMBus slave address for TCO mode. This address must be 1100b 100b for ASF mode.
0	Reserved	Set this bit to 0b.

Note: This byte must be C8h for ASF mode. For example, to program an address of 0011b 001b, the byte should be set to 0011b 0010b. When this address is used on the SMBus, the address byte is 0011b 0010b for writes and 0011b 0011b for reads.

Note: Since the **82546GB/EB** are dual-port devices, the SMBus Slave Address in 14h corresponds to LAN B, and the SMBus Slave Address in 24h corresponds to LAN A.

1. Applicable to the **82546GB/EB** only.

2.1.19 Initialization Control 3 (Word 14h[1] high byte, 24h high byte)

This word controls the general initialization values.

Table 9. Initialization Control 3

Bit	Name	Description
7:5	Reserved	Reserved. Set these bits to 0b.
4	Interrupt Pin	Controls the value advertised in the Interrupt Pin field of the PCI Configuration header for this device/function. A value of 0b (default), reflected in the Interrupt Pin field, indicates that the **82546GB/EB** uses INTA#; a value of 1b indicates that the **82546GB/EB** uses INTB#. If only a single device/function of the Ethernet controller is enabled, this value is ignored and the Interrupt Pin field of the enabled device reports INTA# usage.
3	FLASH Disable	Set this bit to 1b to disable the FLASH logic. Note that the Expansion ROM & secondary FLASH access BARs in PCI configuration space are also disabled. Set this bit to 0b (default) to enable the FLASH logic.
2	APM Enable	Initial value of Advanced Power Management Wakeup Enable in the Wakeup Control Register (WUC.APME). The default for this bit is 0b.
1:0	Link Mode	Initial value of Link Mode bits of the Extended Device Control Register (CTRL_EXT.LINK_MODE), specifying which link interface and protocol is used by the MAC. **For Address 24h (High Byte) / LAN A** 00b = MAC operates in GMII/MII mode with internal copper PHY 01b = External GMII/MII mode 10b = Internal SerDes mode 11b = MAC operates in TBI mode using external TBI interface **For Address 14h (High Byte) / LAN B** 00b = MAC operates in GMII/MII mode with internal copper PHY 01b = Reserved 10b = Internal SerDes mode 11b = MAC operates in TBI mode using external TBI interface

Note: Since the **82546GB/EB** are dual-port devices, the Initialization Control Word 3 bit assignments are port specific.

1. Applicable to the **82546GB/EB** only.

2.1.20 IPv4 Address (Words 15h-16h[1] and 25h-26h)

The following table lists the initial values for the IPv4 addresses.

Table 10. IPv4 Addresses

Bit	Name	Description
31:0	IPv4 Address	The initial value of IPv4 Address Table entry 0. (IP4AT[0]). Refer to the EEPROM Address Map listed in Table 2 for an indication of how the bytes are stored.

Note: Since the **82546GB/EB** are dual-port devices, the IPv4 Address in 15h-16h corresponds to LAN B, and the IPv4 Address in 25h-26h corresponds to LAN A.

2.1.21 IPv6 Address (Words 17h-1Eh[1] and 27h-2Eh)

The following table lists the initial values for the IPv6 addresses.

Table 11. IPv6 Addresses

Bit	Name	Description
127:0	IPv6 Address	The initial value of IPv6 Address Table entry 0. (IP6AT[0]) Refer to the EEPROM Address Map listed in Table 2 for an indication of how the bytes are stored.

Note: Since the **82546GB/EB** are dual-port devices, the IPv6 Address in 17h-1Eh corresponds to LAN B, and the IPv6 Address in 27h-2Eh corresponds to LAN A.

2.1.22 LED Configuration Defaults (Word 2Fh)

This EEPROM word specifies the hardware defaults for the LEDCTL register fields controlling the LED0/(LINK_UP#) and LED2/LINK100 output behaviors. Refer to Table 12 for the LED Control bit descriptions and Table 13 for the Mode Encodings.

Note: A value of 0602h is used to configure default hardware LED behavior equivalent to 82544-based Copper adapters (LED0/LINK_UP#, LED1/ACTIVITY# (blinking), LED2/LINK100#, and LED3/LINK1000#).

1. Applicable to the **82546GB/EB** only.

Table 12. LED Configuration Defaults

Bit	Name	Description
3:0	LED0 Mode	Initial value of the LED0_MODE field specifying what event/state/ pattern will be displayed on LED0 (LINK_UP) output. A value of 0010 (0x2) causes this to indicate LINK_UP state.
5:4	Reserved	Reserved. Set as 0b.
6	LED0 Invert	Initial value of LED0_IVRT field. 0b = Active-low output.
7	LED0 Blink	Initial value of LED0_BLINK field. 0b = Non-blinking.
11:8	LED2 Mode	Initial value of the LED2_MODE field specifying what event/state/ pattern will be displayed on LED2 (LINK_100) output. A value of 0110b (0x6) causes this to indicate 100 Mb/s operation.
13:12	Reserved	Reserved. Set as 0b.
14	LED2 Invert	Initial value of LED2_IVRT field. 0b = Active-low output.
15	LED2 Blink	Initial value of.LED2_BLINK field. 0b = Non-blinking

Table 13 lists the MODE encodings used to select the desired LED signal source for each LED output.

Note: All 16 modes listed are functional.

Table 13. Mode Encodings for LED Outputs

Mode	Pneumonic	State / Event Indicated
0000b	LINK_10/1000	Asserted when either 10 or 1000 Mbps link is established and maintained.
0001b	LINK_100/1000	Asserted when either 100 or 1000 Mbps link is established and maintained.
0010b	LINK_UP	Asserted when any speed link is established and maintained.
0011b	ACTIVITY	Asserted when link is established and packets are being transmitted along with any receive activity that passes filtering.
0100b	LINK/ACTIVITY	Asserted when link is established and when there is no transmit or receive activity.
0101b	LINK_10	Asserted when a 10 Mbps link is established and maintained.
0110b	LINK_100	Asserted when a 100 Mbps link is established and maintained.
0111b	LINK_1000	Asserted when a 1000 Mbps link is established and maintained.
1000b	PCIX_MODE	Asserted when Ethernet controller is in PCI-X mode (deasserted in PCI mode).
1001b	FULL_DUPLEX	Asserted when the link is configured for full duplex operation (deasserted in half-duplex).
1010b	COLLISION	Asserted when a collision is observed.
1011b	BUS_SPEED	Asserted when the Ethernet controller is operating in a PCI 66 MHz or a PCI-X 133 MHz configuration (high-speed PCI operation), deasserted for 33 MHz PCI and 66 MHz PCI-X (as determined by pins sampled at PCI reset).
1100b	BUS_SIZE	Asserted when the Ethernet controller is operating as a 64-bit PCI or PCI-X device, deasserted for 32-bit configuration.
1101b	PAUSED	Asserted when the Ethernet controller's transmitter is flow controlled.
1110b	VCC/LED_ON	Always high. Assuming no optional inversion selected, causes output pin high / LED ON for typical LED circuit.
1111b	GND/LED_OFF	Always low. Assuming no optional inversion selected, causes output pin low / LED OFF for typical LED circuit.

2.1.23 Boot Agent Main Setup Options (Word 30h)

The boot agent software configuration is controlled by the EEPROM with the main setup options stored in word 30h. These options are those that can be changed by using the Control-S setup menu or by using the IBA Intel Agent utility.

Table 14. Boot Agent Main Setup Options

Bit	Name	Description
15	PPB	PXE Presence. Setting this bit to 0b Indicates that the image in the FLASH contains a PXE image. Setting this bit to 1b indicates that no PXE image is contained. The default for this bit is 0b in order to be backwards compatible with existing systems already in the field. If this bit is set to 0b, EEPROM word 32h (PXE Version) is valid. When EPB is set to 1b and this bit is set to 0b, indicates that both images are present in the FLASH.
14	EPB	EFI Presence. Setting this bit to 1b Indicates that the image in the FLASH contains an EFI image. Setting this bit to 0b indicates that no EFI image is contained. The default for this bit is 0b in order to be backwards compatible with existing systems already in the field. If this bit is set to 1b, EEPROM word 33h (EFI Version) is valid. When PPB is set to 0b and this bit is set to 1b, indicates that both images (PXE and EFI) are present in the FLASH.
13	Reserved	Reserved for future use. Set this bit to 0b.
12	FDP	Force Full Duplex. Set this bit to 0b for half duplex; set to 1b for full duplex. Note that this bit is a don't care unless bits 10 and 11 are set.
11:10	FSP	These bits determine speed. 01b = 10 Mbs, 10b = 100 Mbs, 11b = Not allowed. All zeros indicate Auto-negotiate (the current bit state). Note that bit 12 is a don't care unless these bits are set.
9	Reserved	Reserved for future use. Set this bit to 0b.
8	DSM	Display Setup Message. If this bit is set to 1b, the "Press Control-S" message appears after the title message. The default for this bit is 1b.
7:6	PT	Prompt Time. These bits control how long the "Press Control-S" setup prompt message appears, if enabled by DIM. 00b = 2 seconds (default) 01b = 3 seconds 10b = 5 seconds 11b = 0 seconds Note that the Ctrl-S message does not appear if 0 seconds prompt time is selected.

Table 14. Boot Agent Main Setup Options

Bit	Name	Description
5	LBS	Local Boot Selection (OBSOLETE). In previous versions of the agent, this bit enables or disables local boot, if the DBS bit selects it. The default for this bit is 1b; enable local booting. The boot agent, at runtime, no longer uses this bit.
4:3	DBS	Default Boot Selection. These bits select which device is the default boot device. These bits are only used if the agent detects that the BIOS does not support boot order selection or if the MODE field of word 31h is set to MODE_LEGACY. 00b = Network boot, then local boot 01b = Local boot, then network boot 10b = Network boot only 11b = Local boot only
2	BBS	BIOS Boot Specification (OBSOLETE). In previous versions of the agent, this bit enables or disables use of the BBS to determine boot order. If set to 1b, the BIOS boot order is used, and the DBS bits are ignored. The boot agent at runtime no longer uses this bit. The runtime checks for BBS/PnP and the setting in the MODE field of word 31h are used instead.
1:0	PS	Protocol Select. These bits select the boot protocol. 00b = PXE (default value) 01b = RPL protocol Other values are undefined.

2.1.24 Boot Agent Configuration Customization Options (Word 31h)

Word 31h contains settings that can be programmed by an OEM or network administrator to customize the operation of the software. These settings cannot be changed from within the Control-S setup menu or the IBA Intel Boot Agent utility. The lower byte contains settings that would typically be configured by a network administrator using the Intel Boot Agent utility; these settings generally control which setup menu options are changeable. The upper byte are generally settings that would be used by an OEM to control the operation of the agent in a LOM environment, although there is nothing in the agent to prevent their use on a NIC implementation

.

Table 15. Boot Agent Configuration Customization Options (Word 31h)

Bit	Name	Description
15:14	SIG	Signature. These bits must be set to 1b to indicate that this word has been programmed by the agent or other configuration software.
13:11	Reserved	Reserved for future use. Set these bits to 0b.
10:8	MODE	Selects the agent's boot order setup mode. This field changes the agent's default behavior in order to make it compatible with systems that do not completely support the BBS and PnP Expansion ROM standards. Valid values and their meanings are: 000b - Normal behavior. The agent attempts to detect BBS and PnP Expansion ROM support as it normally does. 001b - Force Legacy mode. The agent does not attempt to detect BBS or PnP Expansion ROM supports in the BIOS and assumes the BIOS is not compliant. The BIOS boot order can be changed in the Setup Menu. 010b - Force BBS mode. The agent assumes the BIOS is BBS-compliant, even though it may not be detected as such by the agent's detection code. The BIOS boot order CANNOT be changed in the Setup Menu. 011b - Force PnP Int18 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 18h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order CANNOT be changed in the Setup Menu. 100b - Force PnP Int19 mode. The agent assumes the BIOS allows boot order setup for PnP Expansion ROMs and hooks interrupt 19h (to inform the BIOS that the agent is a bootable device) in addition to registering as a BBS IPL device. The BIOS boot order CANNOT be changed in the Setup Menu. 101b - Reserved for future use. If specified, treated as value 000b. 110b - Reserved for future use. If specified, treated as value 000b. 111b - Reserved for future use. If specified, treated as value 000b.
7:6	Reserved	Reserved for future use. Set these bits to 0b.
5	DFU	Disable FLASH Update. If set to 1b, no updates to the FLASH image using PROSet is allowed. The default for this bit is 0b; allow FLASH image updates using PROSet.
4	DLWS	Disable Legacy Wakeup Support. If set to 1b, no changes to the Legacy OS Wakeup Support menu option is allowed. The default for this bit is 0b; allow Legacy OS Wakeup Support menu option changes.
3	DBS	Disable Boot Selection. If set to 1b, no changes to the boot order menu option is allowed. The default for this bit 0b; allow boot order menu option changes.

Table 15. Boot Agent Configuration Customization Options (Word 31h)

Bit	Name	Description
2	DPS	Disable Protocol Select. If set to 1b, no changes to the boot protocol is allowed. The default for this bit is 0b; allow changes to the boot protocol.
1	DTM	Disable Title Message. If set to 1b, the title message displaying the version of the boot agent is suppressed; the Control-S message is also suppressed. This is for OEMs who do not wish the boot agent to display any messages at system boot. The default for this bit is 0b; allow the title message that displays the version of the boot agent and the Control-S message.
0	DSM	Disable Setup Menu. If set to 1b, no invoking the setup menu by pressing Control-S is allowed. In this case, the EEPROM can only be changed via an external program. The default for this bit is 0b; allow invoking the setup menu by pressing Control-S.

2.1.25 Boot Agent Configuration Customization Options (Word 32h)

Word 32h is used to store the version of the boot agent that is stored in the FLASH image. When the Boot Agent loads, it can check this value to determine if any first-time configuration needs to be performed. The agent then updates this word with its version. Some diagnostic tools to report the version of the Boot Agent in the FLASH also read this word. This word is only valid if the PPB is set to 0b. Otherwise the contents might be undefined.

Table 16. Boot Agent Configuration Customization Options (Word 32h)

Bit	Name	Description
15:12	MAJOR	PXE boot agent major version. The default for these bits is 0b.
11:8	MINOR	PXE boot agent minor version. The default for these bits is 0b.
7:0	BUILD	PXE boot agent build number. The default for these bits is 0b.

2.1.26 IBA Capabilities (Word 33h)

Word 33h is used to enumerate the boot technologies that have been programmed into the FLASH. It is updated by IBA configuration tools and is not updated or read by IBA.

Table 17. IBA Capabilities

Bit	Name	Description
15:14	SIG	Signature. These bits must be set to 1b to indicate that this word has been programmed by the agent or other configuration software.
13:5	Reserved	Reserved for future use. Set these bits to 0b.
4	SAN	SAN capability is present in FLASH. 0b = The SAN capability is not present (default). 1b = The SAN capability is present.
3	EFI	EFI UNDI capability is present in FLASH. 0b = The RPL code is not present (default). 1b = The RPL code is present.
2	RPL	RPL capability is present in FLASH. 1b = The RPL code is present (default). 0b = The RPL code is not present.
1	UNDI	PXE/UNDI capability is present in FLASH. 1b = The PXE base code is present (default). 0b = The PXE base code is not present.
0	BC	PXE base code is present in FLASH. 0b = The PXE base code is present (default). 1b = The PXE base code is not present.

2.1.27 IBA Secondary Port Configuration (Words 34h-35h)

These words provide a unique configuration for the second port of the **82546GB/EB**. The format is the same as that used in words 30h and 31h for LAN A.

2.1.28 Checksum Word Calculation (Word 3Fh)

The Checksum word (3Fh) should be calculated such that after adding all the words (00h-3Fh), including the Checksum word itself, the sum should be BABAh. The initial value in the 16-bit summing register should be 0000h and the carry bit should be ignored after each addition. This checksum is not accessed by the Ethernet controller. If CRC checking is required, it must be performed by software.

Note: Hardware does not calculate checksum word 3Fh during EEPROM write; it must be calculated by software independently and included in the EEPROM write data. Hardware does not compute a checksum over words 00h-0Fh during EEPROM reads in order to determine the validity of the EEPROM image; this field is provided strictly for software verification of EEPROM validity. All hardware configuration based on word 00h-0Fh content is based on the validity of the Signature field of EEPROM Initialization Control Word 1. Signature must be 01b.

2.1.29 Dual-Channel Fiber Wake on LAN (WOL) Mode and Functionality (Word 0Ah, 20h)

Four bits and two words determine dual-channel fiber WOL mode and functionality. In addition to the power management bits, one of the SDP's must be set in order for the "A" laser to remain on when the system goes into D3. Three states are defined for the EEPROM image:

- Never - The Ethernet controller has WOL disabled and cannot be put into WOL mode.
- Possible - The Ethernet controller can be WOL enabled, but currently has the feature turned off. This is the normal shipping configuration for WOL-capable server adapter cards.
- On - The Ethernet controller is set with WOL functionality enabled.

Table 18. WOL Mode and Functionality (Word 0Ah)

State	Bit 2	Bit 7	Resulting Word
Never	0	0	4C03
Possible	1	0	4C0B
On	1	1	4C2B

Table 19. WOL Mode and Functionality (Word 20h)

State	Bit 2	Bit 7	Resulting Word
Never	0	0	C109
Possible	1	0	C10D
On	1	1	C18D

2.2 Parallel FLASH Memory

The Ethernet controller provides an external parallel interface to an optional FLASH or boot EEPROM device. Accesses to the FLASH memory are controlled by the Ethernet controller, but are accessible to host software as normal PCI reads or writes to the FLASH memory mapping range. Software developers can also map FLASH memory to I/O space. The Ethernet controller supports 8-bit wide parallel FLASH memory up to 4 Mb (512 KB); an appropriate size for typical applications would be 1 Mb (128 KB). The size of the FLASH implemented in the design can be encoded into bits in the EEPROM. FLASH and expansion ROM base address registers are reconfigured based on these EEPROM settings.

Representative FLASH memory devices that have been found to work satisfactorily with the Ethernet controller are listed in the following table (two different sizes):

Table 20. FLASH Memory Manufacturers

Manufacturer	Manufacturer's Part Number
Atmel	AT49LV010 AT49BV002AN-70J1
Silicon Storage Technology	SST39V512 39VF020-90-4I-NH 39VF020-70-4C-NH

The FLASH memory interface trace routing is not critical because the interface runs at a very slow speed. In a tightly space-constrained design, the FLASH memory device is a good choice for placement in relative isolation from the Ethernet controller.

Appendix A: Ethernet Controller EEPROM Contents

This appendix contains a sample of raw EEPROM contents for the Ethernet controller. All values for this image are in hexadecimal.

Note: This silicon has not been developed using the EEPROM process.

These images are for base reference only. They are tested production images designed for a generic NIC using the silicon specified. They do not necessarily have every possible feature enabled or configured. The comments have been scrubbed for feature confidentiality.

Please carefully review any setting for applicability to your particular design needs.

A.1 82546GB/EB EEPROM Image

Note: "XXXX" denotes the Individual Address.

```
0400 0023 XXXX 0530 FFFF FFFF FFFF FFFF
XXXX XXXX 460B XXXX XXXX 1079 8086 34E8
000C 1079 0000 2102 10C8 FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
C30C 7863 5004 2102 00C8 FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF 0602
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF XXXX
```

A.2 82545GM/EM EEPROM Image

Note: "XXXX" denotes the Individual Address.

```
0400 0023 FFFF 0530 FFFF FFFF FFFF FFFF
FFFF FFFF 460B FFFF FFFF 1026 8086 34E8
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
C30C 7863 280C 2102 00C8 FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF 0602
FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
FFFF FFFF FFFF FFFF FFFF FFFF FFFF XXXX
```