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1.5-Micron Compacted Array Technology Databook

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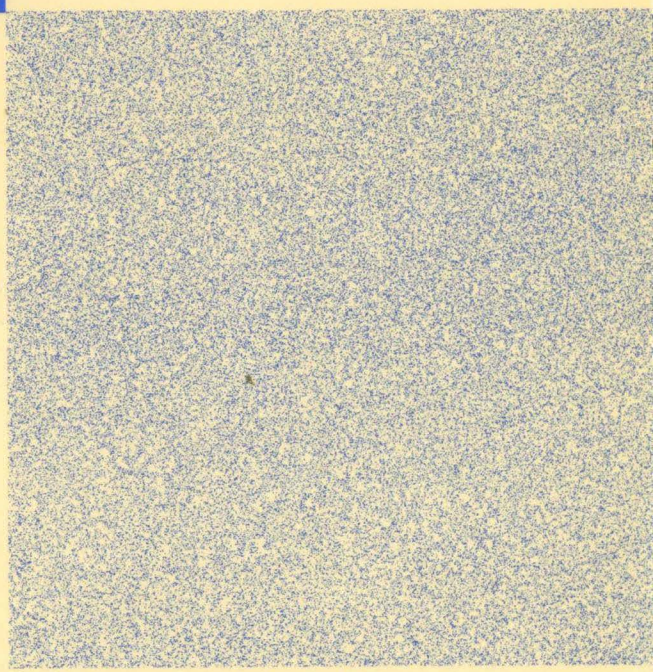

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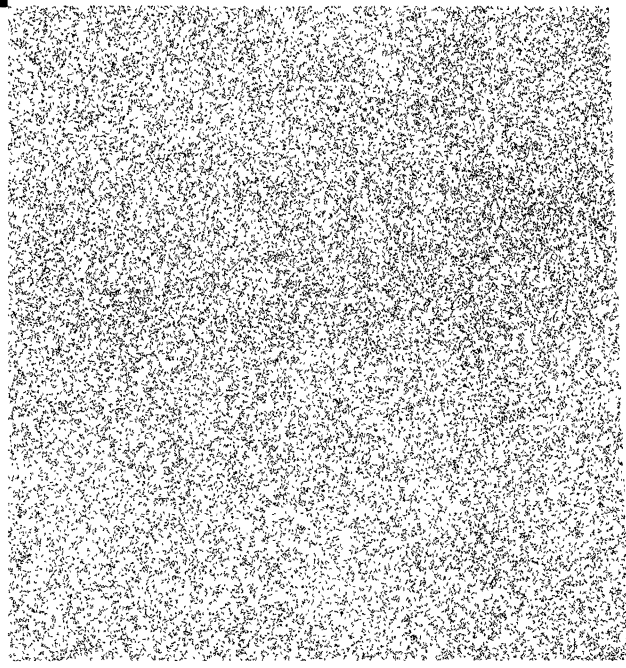

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Preface

The HCMOS Compacted Array products databook is written for logic and system designers who wish to use LSI Logic's Compacted Array™ products to create a system-scale design. It is assumed that the user of this manual will be familiar with LSI Logic's LDS® design sequence from having attended an LDS Gate Array design class and an LDS Compacted Array design class at one of LSI Logic's Design Centers.

The following information is provided:

- An overview introducing LSI Logic's LCA1000 Compacted Array technology.
- A discussion of the LCA10000 propagation delay which is caused by interconnect routing, input loading, temperature, and voltage.
- A description of the array family
- A description of available packaging
- An explanation of power and ground rules.
- A catalogue of Compacted Array products macrocells
- A catalogue of Compacted Array products macrofunctions
- A list of megafunctions available in LSI Logic's libraries.
- A list of available RAMs and ROMs

Publications are stocked at the address given below.
Requests should be addressed to:

LSI Logic Corporation
1551 McCarthy Boulevard
Milpitas, CA 95035
Telex 172153

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Chapter 1: Introduction to the LCA10000 Compacted Array™ Series

1.1 THE PLACE OF THIS MANUAL IN THE DESIGN PROCESS

This LCA10000 Compacted Array™ databook provides logic and system designers with an overview of LCA10000 Compacted Array technology and serves as a catalogue for macrocells (including data), macrofunctions, RAMS, ROMS, and metal megacells (including memories) used in compacted array designs. Data about megafunctions and metal megacells are available elsewhere.

LCA10000 LIBRARIES

The macrocell library for the LCA10000 series is functionally equivalent to the logic elements available for LSI Logic's 2-micron LL7000 series gate arrays, with minor I/O naming modification (exceptions: FD3 and FD3S, on which Q and QN are Ø when both CD and SD are at logic Ø). This equivalence provides design compatibility so that existing gate array designs can be more easily integrated into a single LCA10000 device.

1.2 A GENERAL DESCRIPTION OF THE LCA10000 COMPACTED ARRAY SERIES

The LCA10000 Compacted Array Series is a family of devices capable of allowing system-scale integration. With 1.5 micron drawn transistor geometries and dual-layer metal HCMOS process, the family offers high levels of semi-custom integration, together with maximum circuit performance. The Compacted Array family consists of six devices, with features listed in Table 1.1 below.

Device Number	Gate Complexity	Estimated(1) Usable Gates	Maximum pads (2)	Minimum Power Pads (2)		Maximum I/O Pads (2,3)
				V_{DD}	V_{SS}	
LCA10026	25,740	10,000	168	4	6	158
LCA10038	37,932	15,000	204	8	12	184
LCA10051	50,904	20,000	234	8	12	214
LCA10075	74,970	30,000	282	8	12	256
LCA10100	100,182	40,000	326	8	12	256
LCA10129	129,042	50,000	368	8	12	256

Table 1.1
The LCA10000 Compacted Array Series

The LCA10000 family exhibits internal gate speeds equivalent to 10K ECL technology. This comparison is based on a 2-input NAND gate with a fanout of two at nominal conditions (25°C, 5.0V). The average of rise and fall delays is about 570 psec. Even though I/O paths generally are not as fast as those of ECL products, the Compacted Array's density reduces the number of ICs and thus eliminates performance degradation caused by interchip connections-- a problem apparent in ECL designs which use off-the-shelf components.

The LCA10000 series has a high pad count--up to 256 signal I/Os in the largest sizes--a number limited only by the capabilities of present semiconductor test equipment. Three-state, bidirectional, and unidirectional buffers are offered with designer-specific options: pull-up or pull-down resistors, variable drive strengths, and slew rate controls.

1.3 OUTPUT SLEW RATE SELECTION

In LCA10000 Compacted Array series, the user can slow down the output edge rate by selecting the slew rate control option. Outputs can thus be configured with slew rate control.

Slew rate control helps decrease the system noise and output signal overshoot and undershoot caused by the fast rise and fall times of CMOS output buffers, even with relatively short interconnections in transmission lines.

The impedance of signal lines on most PC boards is in the range of 50 to 140 ohms. In general, CMOS output buffers are not strong enough to drive a properly terminated line. When a buffer is driving an unterminated line, the maximum allowable length of the line can be determined from the rise or fall time of the output buffer and the round-trip delay of the line. As a rule of thumb, the round-trip delay of the line should not exceed the rise or fall time of the driving signal. In other words, the longer the transmission line, the more the system performance will be degraded due to reflections and ringing.

Two slew rates are provided for each type of output buffer (except B1 and B2) to slow down the edge rate. The lower drive strength (higher slew rate) is designated by the suffix R; the higher drive strength (moderate slew rate) by the suffix RP. The choice of slew rate depends on design requirements.

A B4 output buffer (4mA drive) has a typical edge rate of 1.4 ns when loaded with 15pf. A B4R (4 mA with the lower of the two drive strengths (R) for slew rate control) has an edge rate of 3.7 ns. For a typical line delay of 0.055 ns/cm, the maximum allowable length of the signal trace is 13 cm for the B4 and 34 cm for the B4R. Outputs with slew rate control thus make the PC board design less stringent.

Table 1.2 below shows the maximum allowable interconnection length for various types of output buffers. Longer interconnections will degrade system performance.

OUTPUT BUFFERS	MAXIMUM INTERCONNECTION LENGTH (cm)
B1	46
B2	24
B4	13
B4RP	25
B4R	34
B6	10
B6RP	17
B6R	24
B8	10
B8RP	13
B8R	17
B12	7
B12RP	10
B12R	13

Table 1.2
The Effect of Output Buffer Choice
on Maximum Interconnection Lengths (cm)

1.4 PROPAGATION DELAYS

Propagation delays for the LCA10000 series macrocells are a function of input transition time, input-signal polarity, fanout loading, interconnect routing, junction temperature, supply voltage, and processing tolerance. This section presents details about how the following affect propagation delays:

- interconnect routing
- input loading
- temperature and voltage

Note: In this databook, performance information for a Compacted Array macrocell is provided for nominal conditions (Ta = 25° C, V_{DD} = 5.0V, and typical process). Scaling factors allow a simple determination of perfomance under other conditions.

Table 1.3 below explains the factors influencing the percent of gate utilization/available gates per block.

ATTRIBUTE	UTILIZATION		
	LOWER	↔	HIGHER
CELL TYPES USED	SMALL, BASIC	SMALL AND LARGE MIX	MEMORY, METAL MEGACELL
HIERARCHY INCORPORATED	FEW OR NO LEVELS	SEVERAL LEVELS	MANY LEVELS
DESIGN ARCHITECTURE	RANDOM LOGIC	BUS-ORIENTED PIPELINED	STRUCTURED REPEATED
CELL INTER-CONNECTIONS	MANY	MODERATE	FEW

Table 1.3
Factors Influencing the
Percent of Gate Utilization

NOTE: Actual utilization will vary, depending on design

THE EFFECT OF INTERCONNECT ROUTING

Figure 1.1 shows the relative capacitive loading that estimates wire length for different sized block areas.

The following explanations are keyed to the numbers circled on the data sheet of Figure 1.1:

1. These dimensions define the physical size of the block.
2. F.O. means the number of pins on that net minus 1.
3. W.L. (WIRE LOAD) represents the standard load equivalents of the wire length used within the block.
4. SLOPE is the linear ratio of the equivalent standard wire loading over the number of F.O. (as shown in Figure 1.2).
5. INCPT equals the y-axis intercept of the equivalent standard load.

0.5x0.5 mmxmm											
F.O.	1	2	3	4	5	6	7	8	16	32	64
W.L.	.39	.57	.76	.94	1.13	1.32	1.50	1.69	3.18	6.16	12.13
SLOPE = 0.186 (std. loading/F.O.) INCPT = 0.198 (std. loading)											
1.0X1.0 mmxmm											
F.O.	1	2	3	4	5	6	7	8	16	32	64
W.L.	.53	.84	1.16	1.47	1.78	2.09	2.40	2.71	5.19	10.2	20.1
SLOPE = 0.311 (std. loading/F.O.) INCPT = 0.225 (std. loading)											
2.0X2.0 mmxmm											
F.O.	1	2	3	4	5	6	7	8	16	32	64
W.L.	.86	1.4	2.0	2.5	3.0	3.6	4.1	4.7	9.1	17.8	35.3
SLOPE = 0.547 (std. loading/F.O.) INCPT = 0.314 (std. loading)											
3.0X3.0 mmxmm											
F.O.	1	2	3	4	5	6	7	8	16	32	64
W.L.	1.4	2.2	3.0	3.8	4.5	5.3	6.1	6.9	13.1	25.7	50.7
SLOPE = 0.782 (std. loading/F.O.) INCPT = 0.627 (std. loading)											
4.0X4.0 mmxmm											
F.O.	1	2	3	4	5	6	7	8	16	32	64
W.L.	1.9	2.9	3.9	4.9	5.9	6.9	7.9	8.9	17.0	33.1	65.3
SLOPE = 1.007 (std. loading/F.O.) INCPT = 0.873 (std. loading)											
5.0X5.0 mmxmm											
F.O.	1	2	3	4	5	6	7	8	16	32	64
W.L.	1.8	3.0	4.2	5.4	6.6	7.9	9.1	10.3	20.0	39.5	78.5
SLOPE = 1.218 (std. loading/F.O.) INCPT = 0.533 (std. loading)											
6.0X6.0 mmxmm											
F.O.	1	2	3	4	5	6	7	8	16	32	64
W.L.	1.7	3.1	4.5	5.9	7.3	8.7	10.1	11.4	22.6	44.8	89.4
SLOPE = 1.391 (std. loading/F.O.) INCPT = 0.324 (std. loading)											
7.0X7.0 mmxmm											
F.O.	1	2	3	4	5	6	7	8	16	32	64
W.L.	1.8	3.3	4.8	6.3	7.8	9.3	10.8	12.4	24.5	48.5	97.3
SLOPE = 1.517 (std. loading/F.O.) INCPT = 0.240 (std. loading)											
8.0X8.0 mmxmm											
F.O.	1	2	3	4	5	6	7	8	16	32	64
W.L.	1.8	3.4	5.0	6.6	8.2	9.8	11.4	13.0	25.7	51.1	102
SLOPE = 1.590 (std. loading/F.O.) INCPT = 0.245 (std. loading)											
9.0X9.0 mmxmm											
F.O.	1	2	3	4	5	6	7	8	16	32	64
W.L.	1.9	3.5	5.1	6.8	8.4	10.1	11 7	13.3	26.5	52.7	105.2
SLOPE = 1.640 (std. loading/F.O.) INCPT = 0.260 (std. loading)											

Figure 1.1
Estimated Capacitive Loading for
Fanout relative to mm^2 Area

Use the following formula to interpolate for load conditions other than those provided:

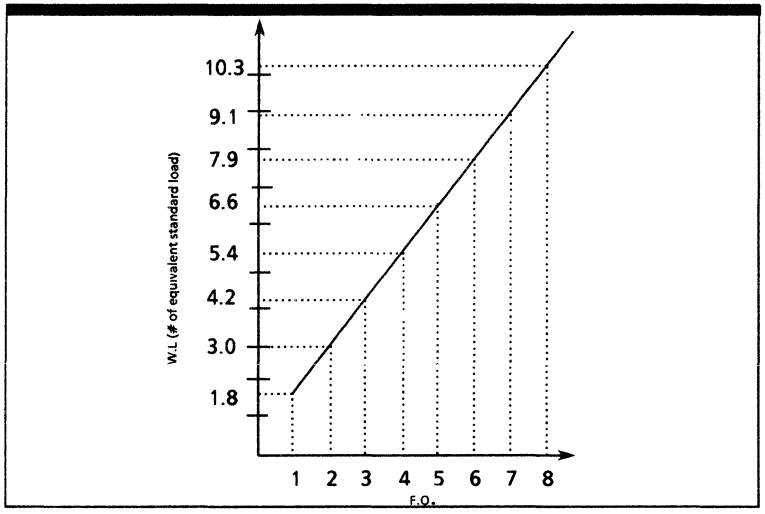


Figure 1.2
Graph of Fanout/Wire Load

W.L. (equivalent standard load) = # of fanouts * Slope + Incpt.

THE EFFECT OF INPUT LOADING

In the macrocell models, propagation delays are listed for specific input loadings of the next stages. Table 1.4 is an example, the model for AN2. Explanations for how to read these data are keyed to circled numbers.

AN2 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.7	0.8	1.0	1.2	1.8	3.2
t_{PHL}	0.9	1.0	1.0	1.1	1.3	1.8

Slope1 = 0.1678 Incpt = 0.50
Slope0 = 0.0589 Incpt = 0.85

Gate Count: 2
Coding Syntax: Z = AN2 (A,B);
Input Loading: (1,1)

Table 1.4
Propagation Delay Table
from Model for AN2

1. "Std. Load" indicates one pair of P and N transistors being driven.
2. "t_{PLH}" is the propagation delay from low to high.
3. "t_{PHL}" is the propagation delay from high to low.
4. "Slope 1:" is the delta of t_{PLH} divided by the delta of Standard Load equivalent.
5. "Slope 0" is the delta of t_{PHL} divided by the delta of Standard Load equivalent.
6. "Incpt" is the intrinsic delay of the cell.

EXAMPLE OF COMPUTING t_{PLH} AND t_{PHL}

The following example shows the method for calculating delays for specific paths within individual functional blocks located in LCA10000 Compacted Array devices.

The floorplan for this example design appears in Figure 1.3.

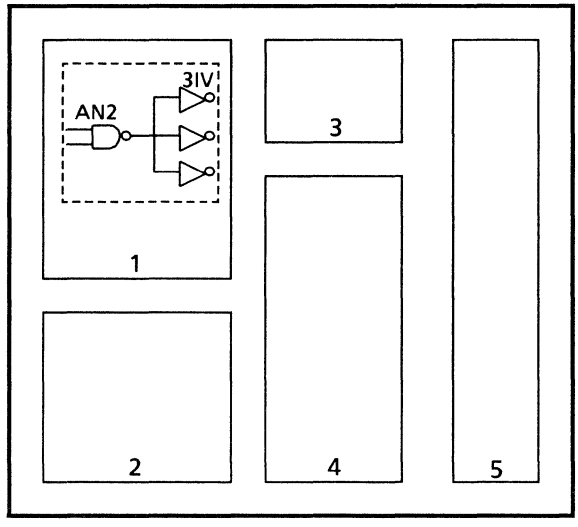


Figure 1.3
Floorplan for Delay Calculation Example

Assume (1) that we are trying to calculate the delay through a 2-input AND gate driving three IV inverters located inside Block #1, (2) that Block #1 contains 8,000 used gates, and (3) that because of the design factors listed in Table 1.3, Block #1 has an estimated 40% gate utilization.

Using this information, we take the following steps:

(1) Determine the number of gates Block #1 would occupy on the die.

In the example, the estimated gate utilization is 40%, so we divide 8000 gates by 0.4--which equals 20,000 gates.

(2) Determine the size of the physical area that the 20,000 gates would occupy.

We divide 20,000 by the known constant of 708 gates/mm^2--which equals 28.2mm^2.

(3) Refer to the wire length loading index (Figure 1.1) and find the nearest region-size bracket.

In this example, we find that 5.0mm x 5.0mm (25mm^2) is nearest to the 28.2mm^2.

(4) Find the total loading in the index, which lists the number of standard loads being driven and the additional loading contributed by the estimated wire length.

In the example of the AND gate driving 3 IV inverters, the standard load is 3. Referring to the index, we find a 4.2 equivalent standard load contributed by the estimated wire length. Adding that to the 3 inverters loading we get a total loading of 7.2 standard loads.

(5) Find the delay on a total loading of 7.2 loads.

We refer to the cell delay tables (the AN2 delay table on Table 1.3), and use the formula previously shown:

$$T_{PD} = \#\text{ of Std. Loads} * \text{Slope} + \text{Intercept}$$

Using the data for the total loading (7.2) and for the slopes and intercepts for the AN2 delay curve, we compute the t_{PLH} and t_{PHL} thus:

$$t_{PLH} = 7.2 \times 0.1678 + 0.50 = 1.7 \text{ ns}$$

$$t_{PHL} = 7.2 \times 0.0589 + 0.85 = 1.3 \text{ ns}$$

The above procedure will provide you with an approximation of delay values with which to calculate critical path delay.

THE EFFECT OF TEMPERATURE AND VOLTAGE

The effects of temperature and voltage on LCA10000 series macrocell performance agree closely with those in LSI Logic's previous gate array technologies. Figure 1.4 shows the propagation delay as a function of temperature (KT), and as a function of supply voltage (KV). LSI Logic allows for a +50% and -40% variance attributed to all other factors, including the processing factor (Kp_{min} = 0.6, Kp_{max} = 1.5).

The worst-case propagation delay can be calculated as follows:

$$t_{max} = K_{pmax} * K_T * K_V * t_{nom} = K_{wc} * t_{nom}$$

For the three standard environmental conditions, K_{wc} is:

WC commercial (70° C, 4.75V)	1.862
WC industrial (85° C, 4.75V)	1.958
WC military (125° C, 4.50V)	2.381

The best-case delay, similarly, is:

$$t_{min} = K_{pmin} * K_T * K_V * t_{nom} = K_{bc} * t_{nom}$$

For the three standard environmental conditions, K_{bc} is:

BC commercial (0° C, 5.25V)	0.508
BC industrial (-40° C, 5.25V)	0.429
BC military (-55° C, 5.50V)	0.374

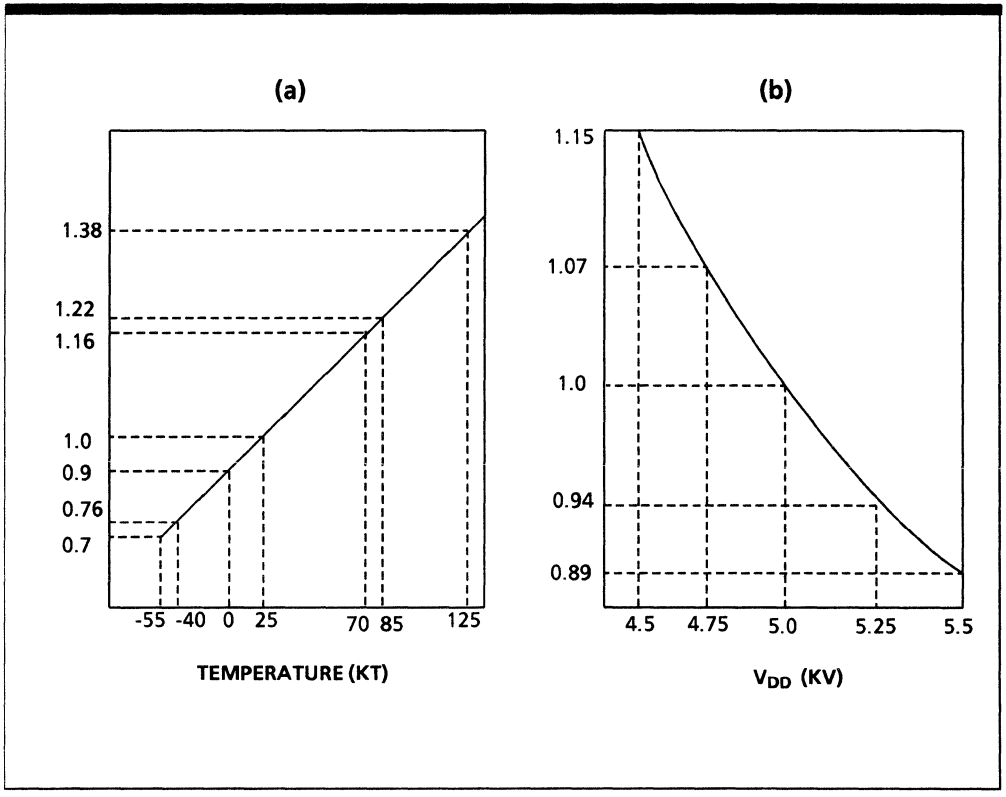


Figure 1.4
Propagation Delays as a function
of Temperature and Supply Voltage

1.5 PACKAGES

LSI Logic offers a variety ceramic pin grid array packages for the LCA10000 Compacted Array series.

Figures 1.5, 1.6 and 1.7 show the master slices of the six LCA10000 chips with preassigned power pads indicated on each footprint.

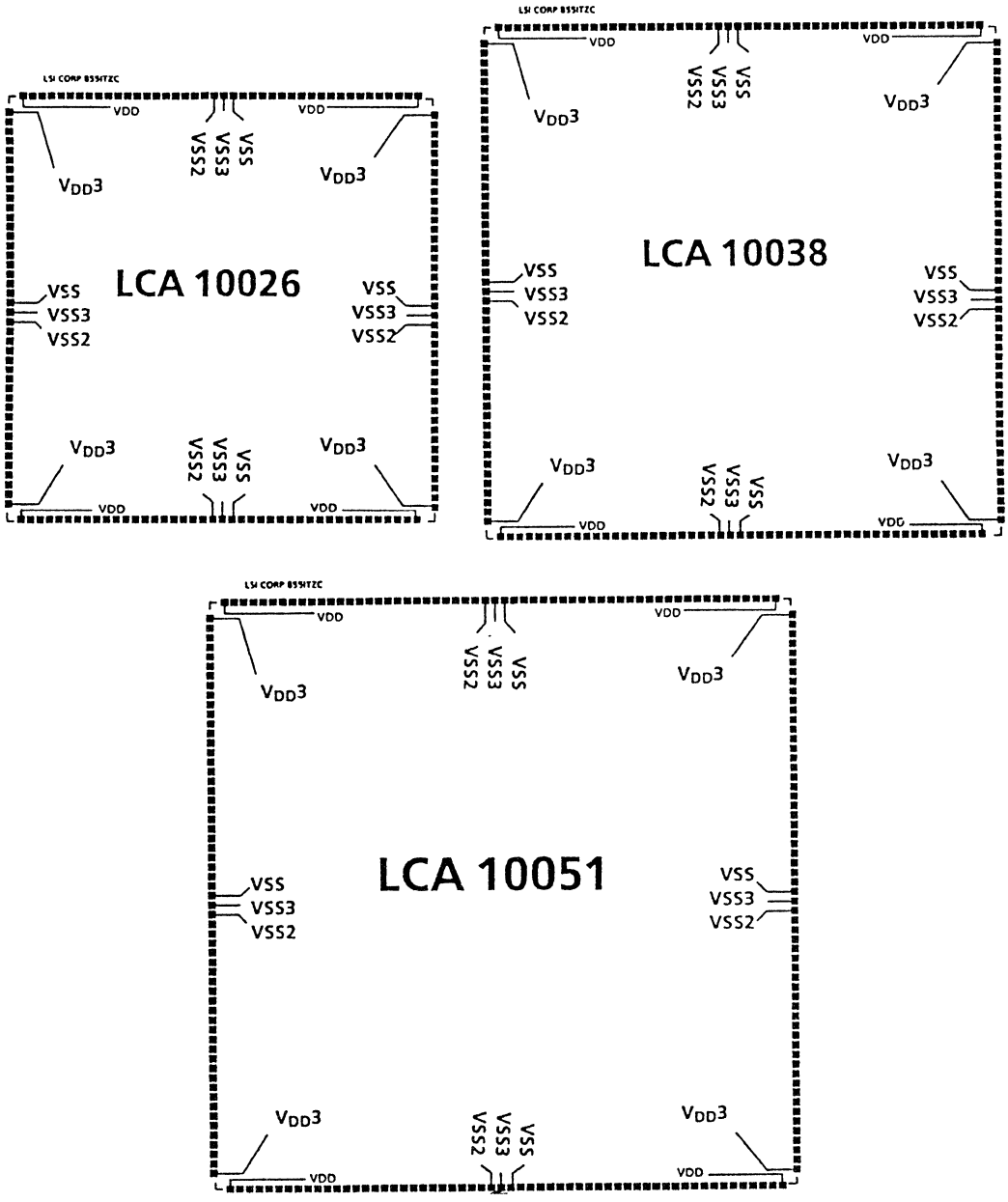
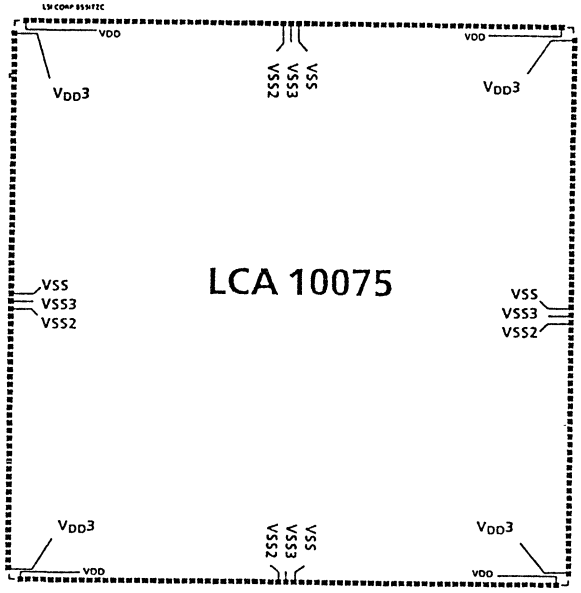
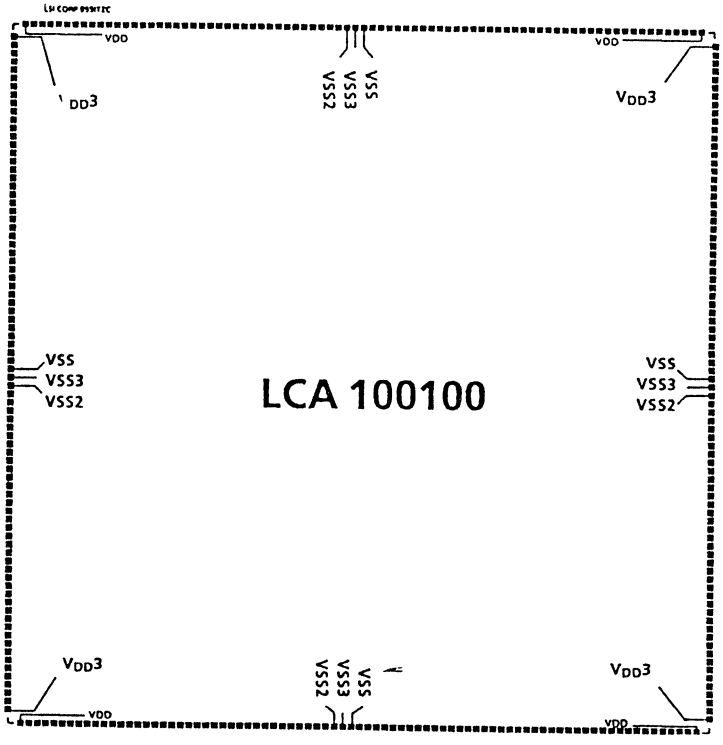
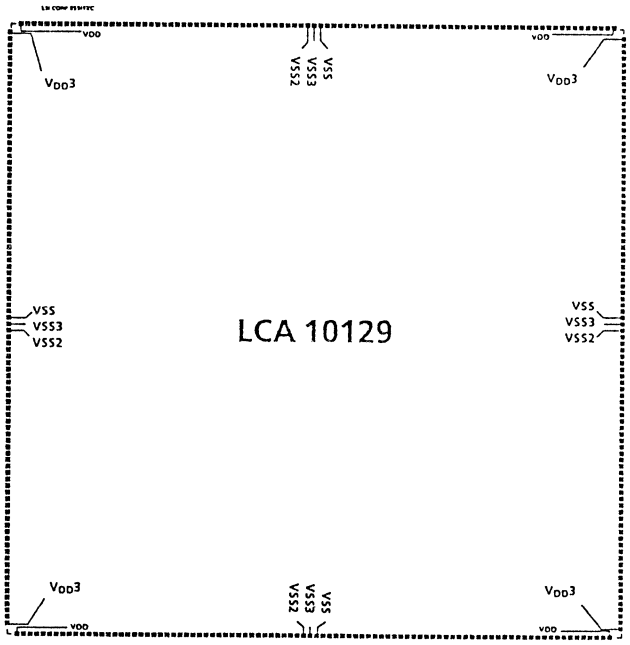


Figure 1.5
Master Slices Showing
Preassigned Power Pads







STANDARD PACKAGES

With the exception of the LCA10075, LCA10100, and LCA10129 devices, standard LSI Logic package types are available for the smaller Compacted Array die sizes, as shown in Table 1.5 below. Package compatibility will be determined on an individual basis.

Figure 1.7
Master Slices Showing
Preassigned Power Pads

Package Name	# Pins	Package Type	LCA 10026	10038	10051	10075	10100	10129
GA38	24	C DIP	X					
GB39	28	C DIP	X	X				
LB34	28	C DIP	X					
GC40	40	C DIP	X	X				
LC35	40	P DIP	X					
MF35	44	P LDCJ	X	X				
GJ40	48	C DIP	X					
LJ34	48	P DIP	X					
CA40	64	C LDC	X	X				
FA40	64	C PGA	X	X				
GD31	64	C DIP	X					
GD48	64	C DIP		X	X			
AB35	68	C LLC	X					
AC40	68	C LLC	X	X				
AK40	68	C LLC	X					
AK45	68	C LLC	X	X	X			
CB45	68	C LDCJ	X	X	X			
CC40	68	C LDC	X	X				
FB44	68	C PGA	X	X	X			
MC41	68	P LDCJ	X	X	X			
NB45	68	P PGA	X	X	X			
AD39	84	C LLC	X					
AD47	84	C LLC		X	X			
AL45	84	C LLC	X	X	X			
AM39	84	C LLC	X	X				
AM50	84	C LLC			X			
CD45	84	C LDCJ	X	X	X			
CE38	84	C LDC	X					
CE47	84	C LDC		X	X			
FC40	84	C PGA	X					
FC44	84	C PGA		X	X			
MD35	84	PLCC	X					
MD42	84	P LDCJ		X	X			
NC45	84	P PGA	X	X	X			
FJ40	88	C PGA	X	X				
DG45	100	C LDC	X	X	X			
FG43	100	C PGA	X	X	X			
NG45	100	P PGA	X	X	X			
FD43	120	C, PGA	X	X	X			
ND37	120	P PGA	X					
ND45	120	P PGA		X	X			
FP38	124	C PGA	X					
BA40	132	C LLC	X	X				
BA54	132	C LLC		X	X			
DE45	132	C LDC	X	X	X			
FH45	132	C PGA	X	X	X			
FK43	132	C PGA	X	X	X			
FE40	144	C PGA	X	X				
FE47	144	C PGA		X	X			
NE45	144	P PGA		X	X			
BB40	148	C LLC	X					
BB45	148	C LLC		X	X			
FF40	148	C PGA	X	X				
FF47	180	C PGA		X	X			
FM48	224	C PGA	X					

Table 1.5
LCA Standard Packages
Mechanical die-Package compatibility chart/Electrical perfomance is design dependent

MULTIPLANE PIN GRID ARRAYS

Table 1.6 below indicates which of the four styles of advanced pin grids are available for each of the six Compacted Array sizes.

Package Name	#Pins	Pin for I/O's	Package Type	LCA 10026	10038	10051	10075	10100	10129
FQ47	95	84	LD CPGA		X	X			
FQ55	95	84	LD CPGA				X		
FR47	155	136	LD CPGA		X	X			
FR55	155	136	LD CPGA				X		
FR64	155	136	LD CPGA					X	X
FS47	223	196	LD CPGA		X	X			
FS55	223	196	LD CPGA				X		
FS64	223	196	LD CPGA					X	X
FT64	299	257	LD CPGA					X	X

Table 1.6
LCA10000 Multiplane C PGA Packages
Mechanical and Electrical performance Die - Package compatibility chart

The Compacted Array multiplane pin grid packages have been designed for high-performance applications. They differ from LSI Logic's standard pin grid packages in the following ways:

- Advanced pin grid packages are designed cavity-down to improve convective cooling. If necessary, the user may attach a heat spreader to the package to increase thermal dissipation. The use of heat spreaders is dependent upon 1) the expected power dissipation, 2) die, cavity, and package sizes, and 3) the external environment of the package; these will be reviewed during design simulation.

- Multiple power (V_{DD}) and ground (V_{SS}) planes have been designed into the package to reduce signal I/O path inductance, signal capacitance, and V_{DD}/V_{SS} path inductance and resistance; and to enhance internal decoupling capacitance. Refer to Table 1.7 for electrical characteristics of the advanced PGAs. Note that specific pins have been dedicated to V_{DD} and V_{SS} to maximize and ensure uniform current flow and effective use of the V_{DD} and V_{SS} planes within the package. No additional package pins need be assigned to V_{DD} or V_{SS}.

PACKAGE LEADCOUNT	POWER (V_{DD})/GROUND (V_{SS})		
	INDUCTANCE,(2) NANOHENRYS	CAPACITANCE,(3) PICOFARADS	RESISTANCE MILLIOHMS
95	0.90	300	40
155	0.50	1000	50(6)
223	0 35	1300	60
299	0 25	1600	60

PACKAGE LEADCOUNT	Signal I/O		
	INDUCTANCE,(4) NANOHENRYS	CAPACITANCE,(5) PICOFARADS	RESISTANCE MILLIOHMS
95	9	<0.75 4.0	250
155	10	<0.75 4.0	300(6)
223	11.5	<1.0 5.0	350
299	11.5	<1.0 5.0	350

NOTES:

1. The above values are estimates based on design calculations.
2. Inductance values are for V_{DD} or V_{SS}. Taken into account are wires (double bonds), planes, vias and pins acting in parallel.
3. Capacitance is between V_{DD} and V_{SS}. Actual measurements for 155 PGA [.640" (16 26mm) cavity] show C = 1050pF.
4. The values shown are for single wire, via and pin inductance.
5. The first value given is measured from signal I/O to signal I/O The second value is measured from signal I/O to ground (V_{SS})
6. Actual measurements for 155 PGA. [640" (16 26mm) cavity] show R (V_{DD} or V_{SS}) = 30 milliohms and R (signal I/O) = 200 millohms

Table 1.7
Electrical Characteristics

- Chip capacitor attachment pads are available for each package to provide additional decoupling capability. The use of chip capacitors is optional at device operational frequencies less than 35 MHz. Above 35 MHz, their use should be reviewed by LSI Logic application engineering. The attachment pads are sized for standard 0.1 microfarad capacitors (.125 x .095 x .065) and strategically placed to decouple V_{DD}/V_{SS} pin inductance while allowing attachment of a heat spreader.
- Multi-level cavity construction permits great flexibility in V_{DD}/V_{SS} bond-out requirements. Virtually any pad on the die can be bonded to power or ground.

THERMAL IMPEDANCE

The thermal impedance requirement for a particular device can be calculated as follows:

$$(Tj - Ta) / Pd = \Theta_{ja}$$

where:

Tj = maximum junction temperature in degrees C.
Ta = maximum ambient temperature in degrees C.
Pd = power dissipation in watts.

The maximum junction temperature specified by LSI Logic for the LCA10000 Compacted Array series is 175 degrees C. Some degradation in device performances may occur as the operating junction temperature of the device reaches 175° C.

This information will enable an engineer to compare calculated ja measurements in both still and flowing air, with or without a heat spreader. Table 1.8 provides the proper conditions that correspond to calculated ja values

.

PACKAGE LEADCOUNT	STILL AIR		FLOWING AIR, 300LFPM	
	Θ_{JA}	Θ_{JA}(HEATSPREADER)(3)	Θ_{JA}	Θ_{JA}(HEATSPREADER)(3)
95	23	N/E	14	11
155	18(2)	N/E	11	9
223	14	N/E	9	8
299	12	N/E	8	7

NOTES:

1. The above values are estimates based on small die [.344" (8.74mm) sq.], medium cavity [.470" (11.94mm) sq.}, glass die attach and power $\approx$ 1W. Heat spreader is assumed to be of omnidirectional format.

2. Initial measurements show Θ_{JA} = 14°C/W in still air for large die [.573" (14.55mm) sq.] and large cavity [.640" (16.26mm) sq.], power = 7.0W.

3. No estimate available.

Table 1.8
Thermal Characteristics

1.6 THE POWER AND GROUND RULES

The LCA10000 family has three types of V_{SS} buses and two types of V_{DD} buses, as follows:

V_{SS} = a ground bus for external output drivers
V_{SS}^3 = a ground bus for external input receivers
V_{SS}^2 = a ground bus for internal arrays
V_{DD} = a power bus for external output drivers and internal arrays
V_{DD}^3 = a power bus for external input receivers

The number of ground and power pins required by each LCA10000 series array is determined by:

- the array size, which effects V_{SS}, V_{SS}^2, and V_{DD}
- the number of output or bidirectional drivers, which effects V_{SS} and V_{DD}
- The location of output and bidirectional drivers, which effects V_{SS} and V_{DD}
- Simultaneous output switching, which effects V_{DD} and V_{SS}
- the array usage, which effects V_{SS}^2
- The operational frequency, which effects V_{SS}^2

Each array of the Compacted Array family has a minimum requirement for power and ground pads--namely, the primary power and ground pads, which have a fixed location and must be connected to package pins. For the LCA10100 die size, for example, the minimum power pad requirement is eight and the minimum ground pad requirement is twelve.

Depending on the number of output drivers, their locations, the array usage, and the operational frequency, additional power and ground pads may be required and will be determined by LDS.

The following rules apply to the assignment of additional power and ground pins:

THE V_{DD}/V_{SS} RULES

1. All primary V_{DD}/V_{SS} pads must be used and bonded out to the package V_{DD}/V_{SS} bond finger.

   If the number of power and ground pads required exceeds the number of primary power and ground pads in the array selected, additional power and ground pads must be used.

2. Every V_{DD}/V_{SS} pad can support up to 16 standard output buffers. Table 1.9 shows the standard drives for output buffers to be used in this calculation.

output buffer w/slew rate cntl	B4R/B4RP	B6R/B6RP	B8R/B8RP	B12R/B12RP
standard drive	0.4/0.5	0.5/0.8	0.8/1.0	1.0/1.5

output buffer	B1	B2	B4	B6	B8	B12
standard drive	.25	.5	1.0	1.5	2.0	3.0

Table 1.9
Standard Drive per Output Buffer

The number for V_{DD}/V_{SS} pads should be counted individually for each side of the array using the following formula:

n = (the total # of standard output buffers for the side) /16

When n is not an integer and the fractional part is = or > 0.1, the number should be rounded off one integer higher (e.g., if n = 3.2, use 4 V_{DD}/V_{SS} pads on that side).

3. For the case of simultaneous switching, if the number of simultaneous switching outputs per package side is greater than 32 std. output drive, then each pair of V_{SS} and V_{DD} bond wires can support only 10 B4 (4mA)-type outputs.

   For better system performance, LSI Logic recommends the following guidelines:

   a. For chips with heavy bus-oriented design, where signals are expected to be received or sent simultaneously, reflections are likely to come back to the I/Os, probably at the same time. In this case, one V_{SS} bond wire and one V_{DD} bond wire should not support more than 10 I/Os.

   b. Two V_{SS} (or two V_{DD}) pads can be bonded out to the same V_{SS} (or V_{DD}) bond finger to satisfy the above rule.

   c. If more V_{SS} and V_{DD} can be bonded, bond them out to further increase the system performance.

THE $V_{SS}2$ RULES

1. The number of V_{SS}^2 pads required in any design is determined by the following formula:

   # of V_{SS}^2 pads = G_u * $\%G_s$ * Sp * (2.5E-6) / (150E-3)

   where:

   G_u = the number of used gates.
   $\%G_s$ = the percent of gates switched.
   Sp = the operating frequency in MHz.

2. All primary V_{SS}^2 pads must be used, even if the number given by the formula above is less than the number of primary V_{SS}^2 pads.

3. If the formula gives a number which is not an integer and which is greater than the number of primary V_{SS}^2 pads, then

   (a) if the calculated fraction = or < 0.1, use the integer portion of the calculation as the number of V_{SS}^2 pads.

   (b) if the calculated fraction > 0.1, add one to the integer portion of the calculation.

THE $V_{DD}3$ RULE

V_{DD}^3 pads, located in each corner of the array, are dedicated. All V_{DD}^3 pads must be used and bonded out to the package V_{DD} bond finger. Extra V_{DD}^3 pads are not necessary.

THE $V_{SS}3$ RULE

All V_{SS}^3 pads must be used be and bonded out to the package V_{SS} bond finger. Extra V_{SS}^3 pads are not necessary.

Chapter 2: The LCA10000 Macrocells

2.1 INTRODUCTION

This chapter provides a comprehensive catalogue of the following types of LCA10000 macrocells:

- input buffers
- unidirectional and three-state output buffers
- bidirectional buffers
- internal cells
- internal drivers
- flip-flops and latches

Each of the following subsections contains a list of available features for each type of macrocell. In addition, naming conventions for input and output buffers are explained, and tables with possible configurations are given.

INPUT BUFFERS

Features

Input buffers have the following features:

- an input-protection circuit
- a built-in parametric gate (except for DDRV, a direct input clock driver)
- three voltage-level options:

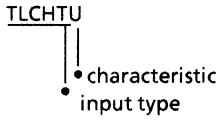
  CMOS
  TTL
  Schmitt Trigger

- optional pull-up and pull-down resistors
- protection against latch-up and electrostatic discharge to a specification of 200 mA and 2000V

Naming Conventions

The form for an input buffer name varies (1) for voltage level options (CMOS, TTL, SCHMITT, CMOS) and (2) for input clock drivers:

- The following example show the form for the name of an input buffer with different voltage level options:



where:

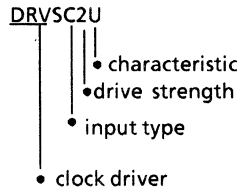
The characteristic may be:

U (pull-up resistor)
D (pull-down resistor)

The input type may be:

TLCHT (input pad with buffer for TTL)
TLCHTN (input pad with buffer for inverted TTL)
IBUF (input pad with buffer for CMOS)
IBUFN (input pad with buffer for inverted CMOS)
SCHMITC (input pad with Schmitt Trigger for CMOS)
SCHMITCN (input pad with inverted Schmitt Trigger for CMOS)

- The following example shows the form for the name of an input clock driver:



where:

The characteristic may be:

<no letter> (no special characteristic)
U (pull-up resistor)
D (pull-down resistor)

The drive strength may be:

2 (maximum recommended loading)
4 (maximum recommended loading)
8 (maximum recommended loading)

The input type may be:

D (as prefix to DRV) for direct
T (TTL)
C (CMOS)
SC (Schmitt Trigger for CMOS)

Possible Input Buffer Configurations

Table 2.1 shows the names for input buffers with the range of possible configurations

w/o resistor	w/pull-up	w/pull-down	slots*
TLCHT	TLCHTU	TLCHTD	1
TLCHN	TLCHNU	TLCHTD	1
IBUF	IBUFU	IBUFD	1
IBUFN	IBUFNU	IBUFND	1
SCHMITC	SCHMITCU	SCHMITCD	1
SCHMITCN	SCHMITCNU	SCHMITCND	1
DRVT2	DRVT2U	DRVT2D	2
DRVT4	DRVT4U	DRVT4D	2
DRVT8	DRVT8U	DRVT8D	2
DRVC2	DRVC2U	DRVC2D	2
DRVC4	DRVC4U	DRVC4D	2
DRVC8	DRVC8U	DRVC8D	2
DRVSC2	DRVSC2U	DRVSC2D	2
DRVSC4	DRVSC4U	DRVSC4D	2
DRVSC8	DRVSC8U	DRVSC8D	2
DDRV	DDRVU	DDRVD	1

*Slot-one pad and one I/O device occupying a position on the periphery of the device

Table 2.1
Possible Input Buffer Configurations

UNIDIRECTIONAL AND THREE-STATE OUTPUT BUFFERS

Features

Unidirectional and three-state output buffers have the following features:

- protection against latch-up: 200 mA
- slew rate control through the choice of different edge-rate characteristics
- options for characteristics: open drain, open source
- output drive tailored to 1.0 mA, 2.0 mA, 4.0 mA, 6.0 mA, 8.0 mA, and 12.0 mA

To convert the delay from a CMOS level to a TTL level, use the following formulas:

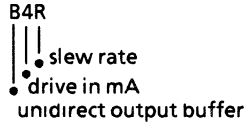
t_{PLH} = slope 1 * Cload * 0.55 + incpt 1

t_{PHL} = slope 0 * Cload * 1.50 + incpt 0

Naming Conventions

The form for buffer names varies for unidirectional and three-state output buffers:

- The following example shows the form for the name of a unidirectional output buffer



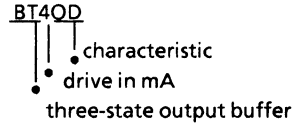
where:

The slew rate contol may be designated as:

<no letter> (without slew rate control)
R (with slew rate control)
RP (with moderate slew rate control)

The drive strength may be: 1, 2, 4, 6, 8, or 12 mA

- The following example shows the form for the name of a three-state output buffer:



where:

The characteristic may be:

<no letter> (no special characteristic)
OD (open drain)
OS (open source)
R (with slew rate control)
RP (with moderate slew rate control)

The drive may be : 1, 2, 4, 6, 8, or 12 mA

Possible Configurations for Unidirectional and Three-state Output Buffers

Tables 2.2 and 2.3 show the possible configurations for unidirectional and three-state output buffers, with the number of I/O slots and output drive in milliamps for each

Name	I/O Slot (s)	Output Drive (ma)
B1	1	1
B2	1	2
B4	1	4
B4R/B4RP	1	4
B6	1	6
B6R/B6RP	1	6
B8	1	8
B8R/B8RP	1	8
B12	2	12
B12R/B12RP	2	12

Table 2.2
Possible Configurations for
Unidirectional Output Buffers

Type and drive	Open drain	Open source	Slew rate	I/O Slot (s)	Output drive (mA)
BT1	BT1OD	BT1OS		1	1
BT2	BT2OD	BT2OS		1	2
BT4	BT4OD	BT4OS	BT4R/BT4RP	1	4
BT6	BT6OD	BT6OS	BT6R/BT6RP	1	6
BT8	BT8OD	BT8OS	BT8R/BT8RP	1	8
BT12	BT12OD	BT12OS	BT12R/BT12RP	2	12

Table 2.3
Possible Configurations for
Three-state Output Buffers

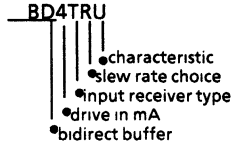
BIDIRECTIONAL OUTPUT BUFFERS

Features

Bidirectional output buffers contain the features of both input and output buffers

Naming Conventions

The following example shows the form for bidirectional output names:



where:

The characteristic may be:

OD (open drain)
OS (open source)
U (pull-up resistor)
D (pull-down resistor)

The slew rate may be designated as:

<no letter> (without control)
R (with slew rate control)
RP (with moderate slew rate control)

Note: Slew rate control is not available for buffers with drive strengths of 1 or 2 mA

The input receiver type may be:

T (TTL)
TN (inverted TTL)
C (CMOS)
CN (inverted CMOS)
SC (CMOS Schmitt Trigger)
SCN (inverted CMOS Schmitt Trigger)

The drive may be : 1, 2, 4, 6, 8, or 12 mA

Possible Configurations for Bidirectional Output Buffers

Table 2.4a-f shows the possible configurations for bidirectional output buffers. Each table shows the possible configurations for one type of input buffer on the bidirectional signals. For each buffer, the number of slots and the output drive are also shown.

Type and drive	w/PU	w/PD	w/OD	w/OS	w/SR	w/PU &SR	w/PD &SR	Slot (s)	Output drive (mA)
BDT1	X	X	X	X				1	0.25
BDT2	X	X	X	X				1	0.5
BDT4	X	X	X	X	X	X	X	1	1.0
BDT6	X	X	X	X	X	X	X	1	1.5
BDT8	X	X	X	X	X	X	X	1	2.0
BDT12	X	X	X	X	X	X	X	2	3.0

Table 2.4a
Possible Configurations for
Bidirectional Output Buffers
with TTL Input

Type and drive	w/PU	w/PD	w/OD	w/OS	w/SR	w/PU &SR	w/PD &SR	Slot (s)	Output drive (mA)
BD1TN	X	X	X	X				1	0.25
BD2TN	X	X	X	X				1	0.5
BD4TN	X	X	X	X	X	X	X	1	1.0
BD6TN	X	X	X	X	X	X	X	1	1.5
BD8TN	X	X	X	X	X	X	X	1	2.0
BD12TN	X	X	X	X	X	X	X	2	3.0

Table 2.4b
Possible Configurations for
Bidirectional Output Buffers
with inverted TTL Input

Type and drive	w/PU	w/PD	w/OD	w/OS	w/SR	w/PU &SR	w/PD &SR	Slot (s)	Output drive (mA)
BD1C	X	X	X	X				1	0.25
BD2C	X	X	X	X				1	0.5
BD4C	X	X	X	X	X	X	X	1	1.0
BD6C	X	X	X	X	X	X	X	1	1.5
BD8C	X	X	X	X	X	X	X	1	2.0
BD12C	X	X	X	X	X	X	X	2	3.0

Table 2.4c
Possible Configurations for
Bidirectional Output Buffers
with CMOS Input

Type and drive	w/PU	w/PD	w/OD	w/OS	w/SR	w/PU &SR	w/PD &SR	Slot (s)	Output drive (mA)
BD1CN	X	X	X	X				1	0.25
BD2CN	X	X	X	X				1	0.5
BD4CN	X	X	X	X	X	X	X	1	1.0
BD6CN	X	X	X	X	X	X	X	1	1.5
BD8CN	X	X	X	X	X	X	X	1	2.0
BD12CN	X	X	X	X	X	X	X	2	3.0

Table 2.4d
Possible Configurations for
Bidirectional Output Buffers
with inverted CMOS Input

Type and drive	w/PU	w/PD	w/OD	w/OS	w/SR	w/PU &SR	w/PD &SR	Slot (s)	Output drive (mA)
BD1SC	X	X	X	X				1	0.25
BD2SC	X	X	X	X				1	0.5
BD4SC	X	X	X	X	X	X	X	1	1.0
BD6SC	X	X	X	X	X	X	X	1	1.5
BD8SC	X	X	X	X	X	X	X	1	2.0
BD12SC	X	X	X	X	X	X	X	2	3.0

Table 2.4e
Possible Configurations for
Bidirectional Output Buffers
with SCHMITT Trigger for CMOS Input

Type and drive	w/PU	w/PD	w/OD	w/OS	w/SR	w/PU &SR	w/PD &SR	Slot (s)	Output drive (mA)
BD1SCN	X	X	X	X				1	0.25
BD2SCN	X	X	X	X				1	0.5
BD4SCN	X	X	X	X	X	X	X	1	1.0
BD6SCN	X	X	X	X	X	X	X	1	1.5
BD8SCN	X	X	X	X	X	X	X	1	2.0
BD12SCN	X	X	X	X	X	X	X	2	3.0

Table 2.4f
Possible Configurations for
Bidirectional Output Buffers
with inverted SCHMITT Trigger for CMOS Input

INTERNAL CELLS, INTERNAL DRIVERS, FLIP-FLOPS, AND LATCHES

Features

All of these cells have standard-drive and high drive configurations. Flip-flops and latches also have buffered input and buffered outputs.

2.2 DATA PAGES FOR MACROCELLS

Following in alphabetical order are data pages for the macrocells.

HOW TO READ A DATA PAGE

Figure 2.1 shows a sample data page (TLCHT, TLCHTU, and TLCHTD). Circled numerals are keyed to the explanations below:

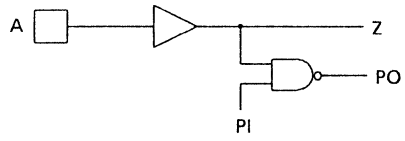
1. The macrocell name appears in the upper-left, upper-middle, and upper-right of the page.
2. The macrocell function appears below the name.
3. The logic diagram is shown.
4. The electrical schematic is shown.
5. A table of typical propagation delays for various standard loads is provided.
6. The syntax coding order of the inputs is given, along with their respective load factors.
7. Input loading is shown for every input pin to the macrocell. The order of the values follows that in the coding syntax equation shown just above.

TTL INPUT BUFFER

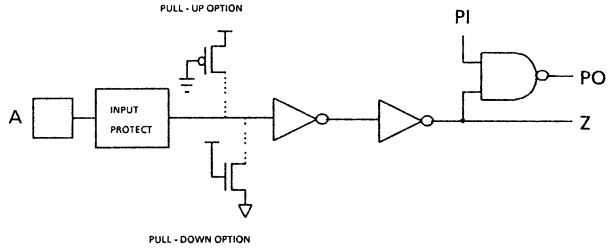
① **TLCHT**
TTL INPUT ②

TLCHTU
TTL INPUT
WITH PULL-UP

TLCHTD
TTL INPUT
WITH PULL-DOWN



③ LOGIC SYMBOL



④ ELECTRICAL SCHEMATIC

⑤ TLCHT / TLCHTU / TLCHTD (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

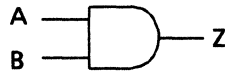
STD LOAD	1	2	3	4	8	16
t_{PLH}(Z) t_{PHL}(Z)	0.8 0.7	0 8 0 7	0.9 0.7	0.9 0.8	1.1 0.8	1.4 1.0

Z Output Slope 1 = 0.0411 Incpt = 0 75
Slope 0 = 0 0201 Incpt = 0.67

⑥ Coding Syntax: (Z,PO) = &TLCHT (A, PI);
Coding Syntax: (Z,PO) = &TLCHTU (A, PI);
Coding Syntax: (Z,PO) = &TLCHTD (A, PI);

⑦ Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

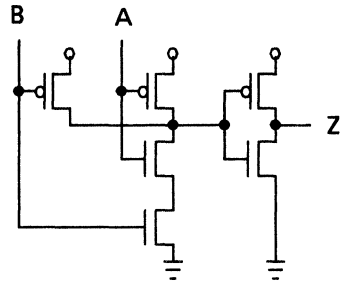
Figure 2.1
Sample Model Sheet for Input Buffers
(TLCHT, TLCHTU, TLCHTD)



LOGIC SYMBOL

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

AN2 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.6	0.8	0.9	1.1	1.6	2.8
t_{PHL}	0.8	0.9	0.9	1.0	1.2	1.6

Slope1 = 0.1443 Incpt = 0.48
Slope0 = 0.0523 Incpt = 0.77

Gate Count: 2
Coding Syntax: Z = AN2 (A,B);
Input loading: (1,1)

AN2P (HIGH DRIVE)

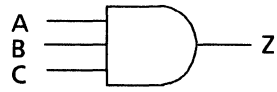
STD LOAD	1	2	3	4	8	16
t_{PLH}	0.6	0.7	0.8	0.8	1.1	1.7
t_{PHL}	0.9	0.9	0.9	1.0	1.1	1.4

Slope1 = 0.0718 Incpt = 0.54
Slope0 = 0.0347 Incpt = 0.84

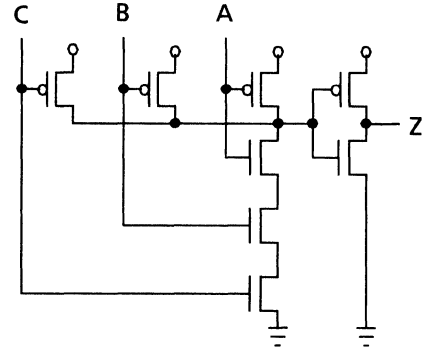
Gate Count: 2
Coding Syntax: Z = AN2P (A,B);
Input loading: (1,1)

A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

TRUTH TABLE



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

AN3 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.8	1.0	1.1	1.3	1.9	3.0
t_{PHL}	0.9	1.0	1.0	1.1	1.3	1.8

Slope1 = 0.1458 Incpt = 0.69
Slope0 = 0.0589 Incpt = 0.85

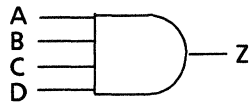
Gate Count: 2
Coding Syntax: Z = AN3 (A,B,C);
Input loading: (1,1,1)

AN3P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.9	1.0	1.1	1.1	1.4	2.0
t_{PHL}	1.0	1.0	1.0	1.1	1.2	1.5

Slope1 = 0.0718 Incpt = 0.84
Slope0 = 0.0347 Incpt = 0.94

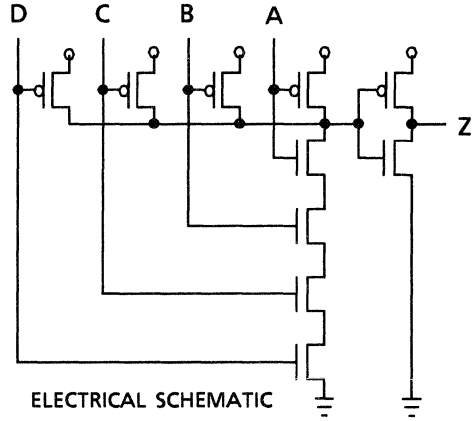
Gate Count: 3
Coding Syntax: Z = AN3P (A,B,C);
Input loading: (1,1,1)



LOGIC SYMBOL

A	B	C	D	Z
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

AN4 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
Tplh	1.1	1.3	1.4	1.6	2.2	3.4
Tphl	1.0	1.1	1.1	1.2	1.4	1.9

Slope1 = 0.1523 Incpt = 0.97
Slope0 = 0.0589 Incpt = 0.95

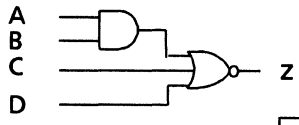
Gate Count: 3
Coding Syntax: Z = AN4 (A,B,C,D);
Input loading: (1,1,1,1)

AN4P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
Tplh	1.2	1.3	1.4	1.5	1.8	2.4
Tphl	1.0	1.0	1.1	1.1	1.2	1.5

Slope1 = 0.0788 Incpt = 1.15
Slope0 = 0.0331 Incpt = 0.96

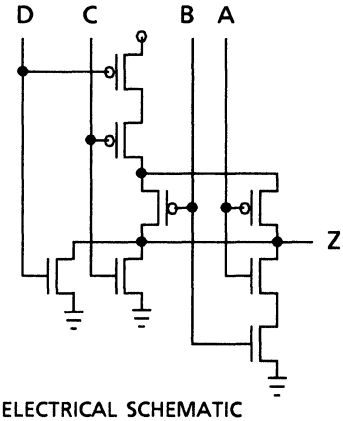
Gate Count: 3
Coding Syntax: Z = AN4P (A,B,C,D);
Input loading: (1,1,1,1)



LOGIC SYMBOL

A	B	C	D	Z
1	1	x	x	0
x	x	1	x	0
x	x	x	1	0
x	0	0	0	1
0	x	0	0	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

AO1 (STANDARD DRIVE)

STD LOAD	1	2	3	4
t_{PLH}	1.5	1.9	2.3	2.6
t_{PHL}	0.4	0.4	0.5	0.6

Slope1 = 0.3864 Incpt = 1.11
Slope0 = 0.0824 Incpt = 0.27

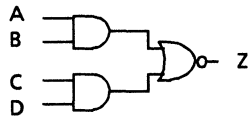
Gate Count: 2
Coding Syntax: Z = AO1 (A,B,C,D);
Input loading: (1,1, 1,1)

AO1P (HIGH DRIVE)

STD LOAD	1	2	3	4	8
t_{PLH}	1.3	1.5	1.7	1.9	2.7
t_{PHL}	0.3	0.4	0.4	0.5	0.6

Slope1 = 0.1934 Incpt = 1.12
Slope0 = 0.0443 Incpt = 0.28

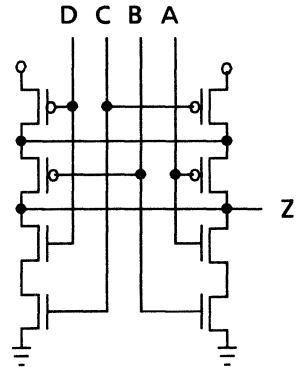
Gate Count: 4
Coding Syntax: Z = AO1P (A,B,C,D);
Input loading: (2,2, 2,2)



LOGIC SYMBOL

A	B	C	D	Z
1	1	x	x	0
x	x	1	1	0
0	x	0	x	1
0	x	x	0	1
x	0	x	0	1
x	0	0	x	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

AO2 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8
t_{PLH}	1.1	1.3	1.6	1.9	2.9
t_{PHL}	0.6	0.6	0.7	0.8	1.1

Slope1 = 0.2612 Incpt = 0.82
Slope0 = 0.0824 Incpt = 0.47

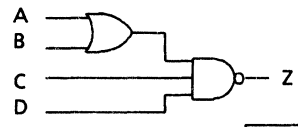
Gate Count: 2
Coding Syntax: Z = AO2 (A,B,C,D);
Input loading: (1,1, 1,1)

AO2P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.9	1.1	1.2	1.3	1.9	2.9
t_{PHL}	0.4	0.5	0.5	0.6	0.7	1.1

Slope1 = 0.1322 Incpt = 0.80
Slope0 = 0.0443 Incpt = 0.38

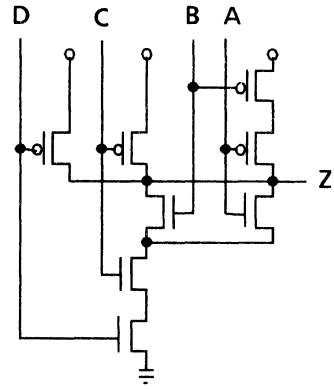
Gate Count: 4
Coding Syntax: Z = AO2P (A,B,C,D);
Input loading: (2,2, 2,2)



LOGIC SYMBOL

A	B	C	D	Z
1	x	1	1	0
x	1	1	1	0
0	0	x	x	1
x	x	0	x	1
x	x	x	0	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal[25 deg c, 5v performance (ns)] wirelength not included

AO3 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8
t_{PLH}	0.8	1.0	1.3	1.6	2.6
t_{PHL}	0.5	0.6	0.7	0.9	1.3

Slope1 = 0.2612 Incpt = 0.52
Slope0 = 0.1136 Incpt = 0.39

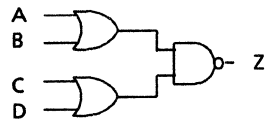
Gate Count: 2
Coding Syntax: Z = AO3 (A,B,C,D);
Input loading: (1,1, 1,1)

AO3P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.6	0.8	0.9	1.0	1.6	2.6
t_{PHL}	0.5	0.5	0.6	0.6	0.9	1.3

Slope1 = 0.1322 Incpt = 0.50
Slope0 = 0.0557 Incpt = 0.42

Gate Count: 4
Coding Syntax: Z = AO3P (A,B,C,D);
Input loading: (2,2, 2,2)

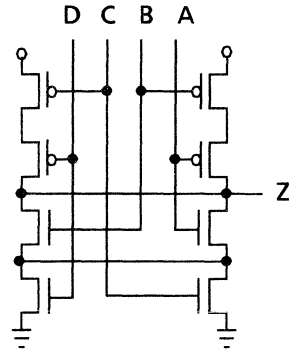


LOGIC SYMBOL

A	B	C	D	Z
0	0	x	x	1
x	x	0	0	1
1	x	1	x	0
x	1	1	x	0
1	x	x	1	0
x	1	x	1	0

TRUTH TABLE

ELECTRICAL SCHEMATIC



Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

AO4 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8
t_{PLH}	1.2	1.4	1.7	2.0	3. 0
t_{PHL}	0.5	0.5	0.6	0.7	1.0

Slope1 = 0.2612 Incpt = 0.92
Slope0 = 0.0824 Incpt = 0.37

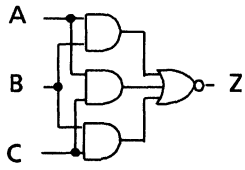
Gate Count: 2
Coding Syntax: Z = AO4 (A,B,C,D);
Input loading: (1,1, 1,1)

AO4P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.0	1.2	1.3	1.4	2.0	3.0
t_{PHL}	0.4	0.5	0.5	0.6	0.7	1.1

Slope1 = 0.1322 Incpt = 0.90
Slope0 = 0.0443 Incpt = 0.38

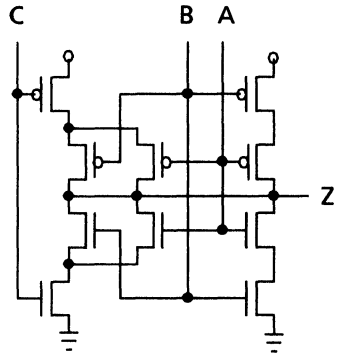
Gate Count: 4
Coding Syntax: Z = AO4P (A,B,C,D);
Input loading: (2,2, 2,2)



LOGIC SYMBOL

A	B	C	Z
1	1	x	0
1	x	1	0
x	1	1	0
0	0	x	1
0	x	0	1
x	0	0	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

AO5 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8
t_{PLH}	1.4	1.6	1.9	2.2	3.2
t_{PHL}	0.5	0.6	0.7	0.8	1.1

Slope1 = 0.2612 Incpt = 1.12
Slope0 = 0.0788 Incpt = 0.45

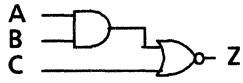
Gate Count: 3
Coding Syntax: Z = AO5 (A,B,C);
Input loading: (2, 2,1)

AO5P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.2	1.3	1.4	1.6	2.1	3.1
t_{PHL}	0.5	0.5	0.5	0.6	0.8	1.1

Slope1 = 0.1282 Incpt = 1.06
Slope0 = 0.0428 Incpt = 0.42

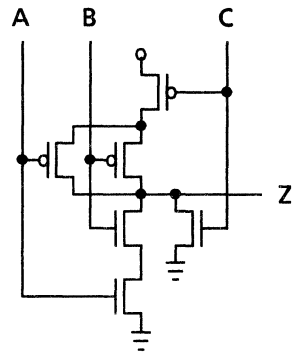
Gate Count: 5
Coding Syntax: Z = AO5P (A,B,C);
Input loading: (4, 4,2)



LOGIC SYMBOL

A	B	C	Z
x	x	1	0
0	x	0	1
x	0	0	1
1	1	0	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

AO6 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8
t_{PLH}	1.1	1.3	1.6	1.9	2.9
t_{PHL}	0.4	0.4	0.5	0.6	0.9

Slope1 = 0.2612 Incpt = 0.82
Slope0 = 0.0824 Incpt = 0.27

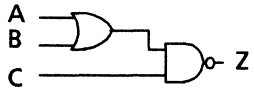
Gate Count: 2
Coding Syntax: Z = AO6 (A,B,C);
Input loading: (1, 1,1)

AO6P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.9	1.1	1.2	1.3	1.9	2.9
t_{PHL}	0.2	0.3	0.3	0.4	0.5	0.9

Slope1 = 0.1322 Incpt = 0.80
Slope0 = 0.0443 Incpt = 0.18

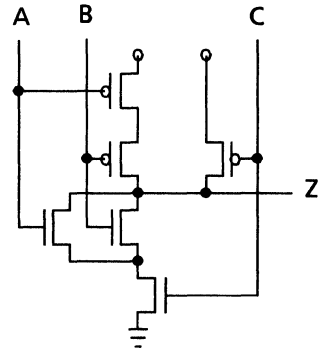
Gate Count: 3
Coding Syntax: Z = AO6P (A,B,C);
Input loading: (2, 2,2)



LOGIC SYMBOL

A	B	C	Z
x	x	0	1
1	x	1	0
x	1	1	0
0	0	1	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

AO7 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8
t_{PLH}	0.8	1.0	1.3	1.6	2.6
t_{PHL}	0.5	0.5	0.6	0.7	1.0

Slope1 = 0.2612 Incpt = 0.52
Slope0 = 0.0824 Incpt = 0.37

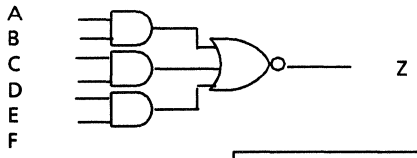
Gate Count: 2
Coding Syntax:Z = AO7 (A,B,C);
Input loading: (1, 1,1)

AO7P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.6	0.8	0.9	1.0	1.6	2.6
t_{PHL}	0.3	0.4	0.4	0.5	0.6	1.0

Slope1 = 0.1322 Incpt = 0.50
Slope0 = 0.0443 Incpt = 0.28

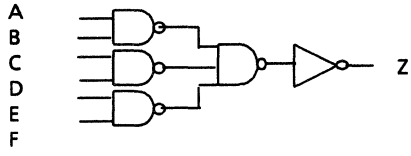
Gate Count: 3
Coding Syntax:Z = AO7P (A,B,C);
Input loading: (2, 2,2)



LOGIC SYMBOL

A	B	C	D	E	F	Z
1	1	x	x	x	x	0
x	x	1	1	x	x	0
x	x	x	x	1	1	0
otherstates						1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

AO11 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.3	1.5	1.6	1.8	2.4	3.6
t_{PHL}	1.0	1.1	1.1	1.2	1.4	1.9

Slope1 = 0.1523 Incpt = 1.17
Slope0 = 0.0589 Incpt = 0.95

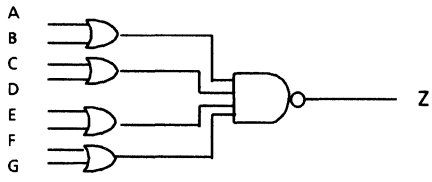
Gate Count: 5
Coding Syntax: Z = AO11 (A,B,C,D,E,F);
Input loading: (1,1, 1,1,1,1)

AO11P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.4	1.5	1.6	1.6	1.9	2.5
t_{PHL}	1.1	1.1	1.1	1.2	1.3	1.6

Slope1 = 0.0718 Incpt = 1.34
Slope0 = 0.0347 Incpt = 1.04

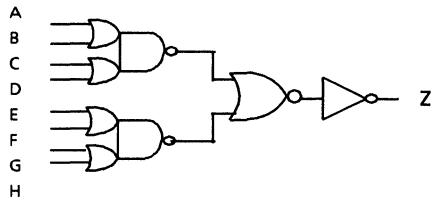
Gate Count: 6
Coding Syntax: Z = AO4P (A,B,C,D,E,F);
Input loading: (1,1,1,1,1,1)



LOGIC SYMBOL

A	B	C	D	E	F	G	H	Z
0	0	x	x	x	x	x	x	1
x	x	0	0	x	x	x	x	1
x	x	x	x	0	0	x	x	1
x	x	x	x	x	x	0	0	1
other states								0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

AO12 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.5	1.7	1.8	2.0	2.5	3.7
t_{PHL}	1.2	1.3	1.3	1.4	1.6	2.1

Slope1 = 0.1443 Incpt = 1.38
Slope0 = 0.0589 Incpt = 1.15

Gate Count: 6
Coding Syntax: Z = AO11 (A,B,C,D,E,F,G,H);
Input loading: (1,1, 1,1,1,1,1,1)

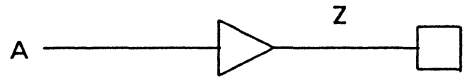
AO12P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.6	1.7	1.8	1.8	2.1	2.6
t_{PHL}	1.3	1.3	1.4	1.4	1.5	1.8

Slope1 = 0.0653 Incpt = 1.56
Slope0 = 0.0331 Incpt = 1.26

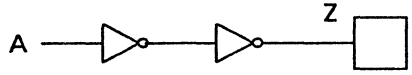
Gate Count: 6
Coding Syntax: Z = AO4P (A,B,C,D,E,F,G,H);
Input loading: (1,1,1,1,1,1,1,1)

UNIDIRECT OUTPUT BUFFERS

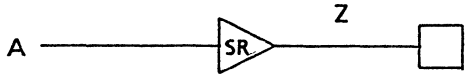


a. LOGIC SYMBOL

ELECTRICAL SCHEMATICS



b. UNIDIRECT OUTPUT BUFFER



c. UNIDIRECT OUTPUT BUFFER WITH SLEW RATE CONTROL

Figure 2.2

B1/B2 UNIDIRECT OUTPUT BUFFERS

B1
1mA OUTPUT BUFFER

B2
2mA OUTPUT BUFFER

B1 (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH} (Z)	4.1	11.7	19.3	22.5
t_{PHL} (Z)	3.6	9.3	15.0	17.4

IO Output Slope 1 (ns/pf) = 0.2166 Incpt (ns) = 0.86
Slope 0 (ns/pf) = 0.1625 Incpt (ns) = 1.17

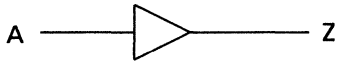
Coding Syntax: Z = &B1 (A);
Input Loading: (2)

B2 (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

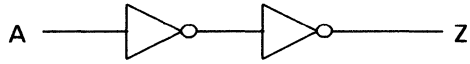
CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH} (Z)	2.7	7.3	11.8	13.8
t_{PHL} (Z)	2.3	5.2	8.1	9.3

IO Output Slope 1 (ns/pf) = 0.1303 Incpt (ns) = 0.76
Slope 0 (ns/pf) = 0.0825 Incpt (ns) = 1.07

Coding Syntax: Z = &B2 (A);
Input Loading: (2)



LOGIC SYMBOLC



SCHEMATIC

A	Z
0	0
1	1

TRUTH TABLE

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

B1I (A - Z)

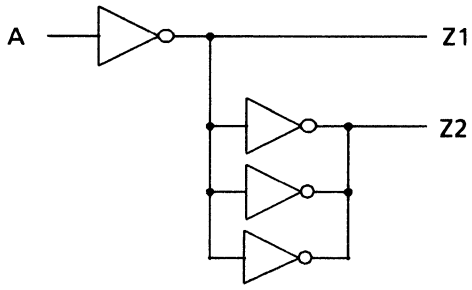
STD LOAD	50	100	200	300	400	500
t_{PLH}	0.9	1.1	1.7	2.3	2.9	3.5
t_{PHL}	1.3	1.5	1.9	2.3	2.7	3.1

Z Output Slope 1 = 0.0059 Incpt = 0.55
Slope 0 = 0.0040 Incpt = 1.10

Coding Syntax: Z = B1I (A);
Input Loading: (4)

INVERTER INTO 3 PARALLEL INVERTERS

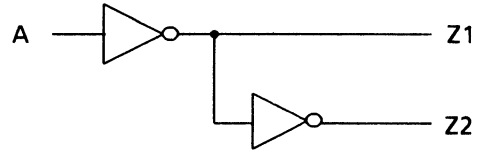
B2I / B2IP



ELECTRICAL SCHEMATIC

A	Z1	Z2
1	0	1
0	1	0

TRUTH TABLE



LOGIC DIAGRAM

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

B2I (A-Z1 / Z2) (STANDARD DRIVE)

STD LOAD	2	4	8	16
t_{PLH}(Z1) t_{PHL}(Z1)	1.0 0.5	1.3 0.6	1.8 0.8	3.0 1.2
t_{PLH}(Z2) t_{PHL}(Z2)	0.7 0.9	0.8 0.9	0.9 1.0	1.3 1.2

Z1 Output	Slope 1	= 0.1403	Incpt	=	0.72
	Slope 0	= 0.0500	Incpt	=	0.40
Z2 Output	Slope 1	= 0.0475	Incpt	=	0.56
	Slope 0	= 0.0198	Incpt	=	0.85

Gate Count: 2
Coding Syntax: X (Z1,Z2) = B2I (A);
Input Loading: (1)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

B2IP (A-Z1 / Z2) (HIGH DRIVE)

STD LOAD	4	8	16	32
t_{PLH}(Z1) t_{PHL}(Z1)	1.0 0.5	1.3 0.6	1.8 0.8	3.0 1.2
t_{PLH}(Z2) t_{PHL}(Z2)	0.7 0.9	0.8 0.9	1.0 1.0	1.3 1.2

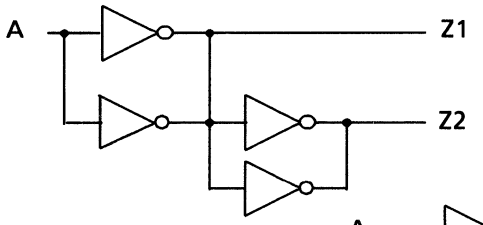
Z1 Output	Slope 1 = 0.0718	Incpt	= 0.70	
	Slope 0 = 0.0266	Incpt	= 0.38	
Z2 Output	Slope 1 = 0.0214	Incpt	= 0.63	
	Slope0 = 0.0121	Incpt	= 0.82	

Gate Count: 4
Coding Syntax: X (Z1,Z2) = B2IP (A);
Input Loading: (2)

B3I / B3IP

2 PARALLEL INVERTERS INTO 2 PARALLEL INVERTERS

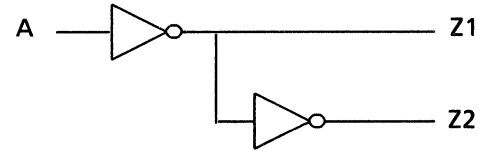
B3I / B3IP



ELECTRICAL SCHEMATIC

A	Z1	Z2
1	0	1
0	1	0

TRUTH TABLE



LOGIC DIAGRAM

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

B3I (A-Z1 / Z2) (STANDARD DRIVE)

STD LOAD	2	4	8	16	32
t_{PLH}(Z1) t_{PHL}(Z1)	0.6 0.2	0.8 0.3	1.1 0.4	1.6 0.7	2.8 1.1
t_{PLH}(Z1) t_{PHL}(Z2)	0.5 0.7	0.6 0.7	0.9 0.8	1.5 1.0	2.6 1.5

Z1 Output	Slope 1	= 0.0720	Incpt	= 0.49
	Slope 0	= 0.0298	Incpt	= 0.17
Z2 Output	Slope 1	= 0.0708	Incpt	= 0.34
	Slope 0	= 0.0274	Incpt	= 0.60

Gate Count: 2
Coding Syntax: X(Z1,Z2) = B2I (A);
Input Loading: (2)

B3IP (A-Z1 / Z2) (HIGH DRIVE)

STD LOAD	2	4	8	16	32
t_{PLH}(Z1) t_{PHL}(Z1)	0.5 0.2	0.5 0.3	0.7 0.3	0.9 0.5	1.5 0.8
t_{PLH}(Z1) t_{PHL}(Z2)	0.4 0.6	0.5 0.6	0.6 0.6	0.9 0.8	1.4 1.0

Z1 Output	Slope 1	= 0.0339	Incpt	= 0.40
	Slope 0	= 0.0194	Incpt	= 0.18
Z2 Output	Slope 1	= 0.0331	Incpt	= 0.35
	Slope 0	= 0.0144	Incpt	= 0.54

Gate Count: 4
Coding Syntax: X(Z1,Z2) = B2IP (A);
Input Loading: (4)

B4 UNIDIRECT OUTPUT BUFFERS

B4
4mA OUTPUT BUFFER

B4R
4mA OUTPUT BUFFER WITH SLEW RATE

B4RP
4mA OUTPUT BUFFER WITH MODERATE SLEW RATE

B4 (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	1.6	3.8	6.1	7.0
t_{PHL}	1.6	3.1	4.5	5.1

IO Output
Slope 1 (ns/pf) = 0.0639 Incpt (ns) = 0.63
Slope 0 (ns/pf) = 0.0411 Incpt (ns) = 1.00

Coding Syntax: Z = &B4 (A);
Input Loading: (4)

B4R (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	3.2	6.8	10.5	12.1
t_{PHL}	2.8	6.0	9.2	10.6

IO Output
Slope 1 (ns/pf) = 0.1047 Incpt (ns) = 1.60
Slope 0 (ns/pf) = 0.0917 Incpt (ns) = 1.42

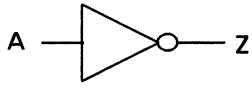
Coding Syntax: Z = &B4R (A);
Input Loading: (4.5)

B4RP (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	2.4	5.4	8.5	9.8
t_{PHL}	2.4	5.0	7.6	8.8

IO Output
Slope 1 (ns/pf) = 0.0872 Incpt (ns) = 1.07
Slope 0 (ns/pf) = 0.0750 Incpt (ns) = 1.26

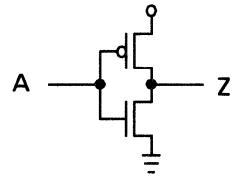
Coding Syntax: Z = &B4RP (A);
Input Loading: (4.5)



LOGIC DIAGRAM

A	Z
1	0
0	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

B4I (STANDARD DRIVE)

STD LOAD	4	8	16	32	64
t_{PLH}	0.5	0.6	0.9	1.4	2.5
t_{PHL}	0.2	0.3	0.4	0.7	1.4

Slope1 = 0.0335 Incpt = 0.35
Slope0 = 0.0198 Incpt = 0.11

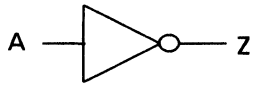
Gate Count: 2
Coding Syntax:Z = B4I (A);
Input loading: (4)

B4IP (HIGH DRIVE)

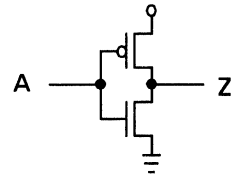
STD LOAD	4	8	16	32	64
t_{PLH}	0.4	0.5	0.6	0.9	1.4
t_{PHL}	0.1	0.1	0.2	0.4	0.8

Slope1 = 0.0165 Incpt = 0.35
Slope0 = 0.0121 Incpt = 0.02

Gate Count: 4
Coding Syntax:Z = B4IP (A);
Input loading: (8)



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

A	Z
1	0
0	1

TRUTH TABLE

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

B5I (STANDARD DRIVE)

STD LOAD	4	8	16	32
t_{PLH}	0.6	0.7	1.1	1.9
t_{PHL}	0.2	0.3	0.5	0.9

Slope1 = 0.0475 Incpt = 0.36
Slope0 = 0.0234 Incpt = 0.12

Gate Count: 2
Coding Syntax: Z = B5I (A);
Input loading: (3)

B5IP (HIGH DRIVE)

STD LOAD	4	8	16	32	64
t_{PLH}	0.4	0.5	0.7	1.0	1.7
t_{PHL}	0.2	0.3	0.4	0.6	1.1

Slope1 = 0.0214 Incpt = 0.33
Slope0 = 0.0146 Incpt = 0.16

Gate Count: 3
Coding Syntax: Z = B5IP (A);
Input loading: (6)

B6 UNIDIRECT OUTPUT BUFFERS

B6
6mA OUTPUT BUFFER

B6R
6mA OUTPUT BUFFER WITH SLEW RATE

B6RP
6mA OUTPUT BUFFER WITH MODERATE SLEW RATE

B6 (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	1.4	3.0	4.6	5.3
t_{PHL}	1.5	2.5	3.6	4.0

IO Output
Slope 1 (ns/pf) = 0.0458 Incpt (ns) = 0.71
Slope 0 (ns/pf) = 0.0297 Incpt (ns) = 1.04

Coding Syntax: Z = &B6 (A);
Input Loading: (4)

B6R (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	2.4	5.6	8.7	10.0
t_{PHL}	2.3	5.0	7.8	9.0

IO Output
Slope 1 (ns/pf) = 0.0894 Incpt (ns) = 1.09
Slope 0 (ns/pf) = 0.0789 Incpt (ns) = 1.09

Coding Syntax: Z = &B6R (A);
Input Loading: (6.5)

B6RP (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	1.9	4.4	6.9	8.0
t_{PHL}	1.8	3.7	5.6	6.5

IO Output
Slope 1 (ns/pf) = 0.0717 Incpt = 0.82
Slope 0 (ns/pf) = 0.0550 Incpt = 0.96

Coding Syntax: Z = &B6RP (A);
Input Loading: (6.5)

B8 UNIDIRECT OUTPUT BUFFERS

B8	B8R	B8RP
8mA OUTPUT BUFFER	8mA OUTPUT BUFFER WITH SLEW RATE	8mA OUTPUT BUFFER WITH MODERATE SLEW RATE

B8 (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	1.3	2.6	3.8	4.4
t_{PHL}	1.5	2.3	3.1	3.4

IO Output
Slope 1 (ns/pf) = 0.0361 Incpt (ns) = 0.77
Slope 0 (ns/pf) = 0.0225 Incpt (ns) = 1.17

Coding Syntax: Z = &B8 (A);
Input Loading: (4)

B8R (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	2.0	4.6	7.1	8.3
t_{PHL}	1.8	3.7	5.6	6.5

IO Output
Slope 1 (ns/pf) = 0.0736 Incpt (ns) = 0.90
Slope 0 (ns/pf) = 0.0550 Incpt(ns) = 0.96

Coding Syntax: Z = &B8R (A);
Input Loading: (6.5)

B8RP (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	1.7	3.8	5.9	6.9
t_{PHL}	1.6	3.1	4.5	5.1

IO Output
Slope 1 (ns/pf) = 0.0609 Incpt (ns) = 0.77
Slope 0 (ns/pf) = 0.0411 Incpt (ns) = 1.01

Coding Syntax: Z = &B8RP (A);
Input Loading: (6.5)

B12 UNIDIRECT OUTPUT BUFFERS

B12	B12R	B12RP
12mA OUTPUT BUFFER	12mA OUTPUT BUFFER WITH SLEW RATE	12mA OUTPUT BUFFER WITH MODERATE SLEW RATE

B12 (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	1.0	1.8	2.6	3.0
t_{PHL}	1.3	1.8	2.4	2.6

IO Output

Slope 1 (ns/pf) = 0.0234 Incpt (ns) = 0.64
Slope 0 (ns/pf) = 0.0155 Incpt (ns) = 1.05

Coding Syntax: Z = &B12 (A);
Input Loading: (8)

B12R (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	1.5	3.3	5.1	5.9
t_{PHL}	1.5	2.9	4.4	5.0

IO Output

Slope 1 (ns/pf) = 0.0517 Incpt (ns) = 0.72
Slope 0 (ns/pf) = = 0.0414 Incpt (ns) = 0.86

Coding Syntax: Z = &B12R (A);
Input Loading: (13)

B12RP (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

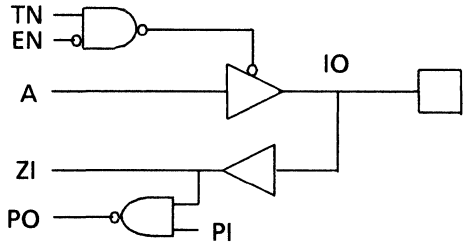
CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	1.2	2.5	3.9	4.5
t_{PHL}	1.3	2.3	3.2	3.6

IO Output

Slope 1 (ns/pf) = 0.0389 Incpt (ns) = 0.59
Slope 0 (ns/pf) = 0.0269 Incpt (ns) = 0.92

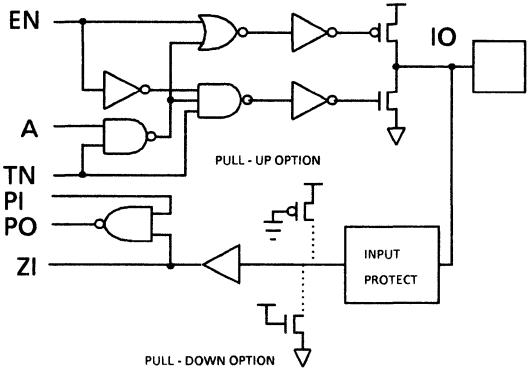
Coding Syntax: Z = &B12RP (A);
Input Loading: (13)

BIDIRECT OUTPUT BUFFERS

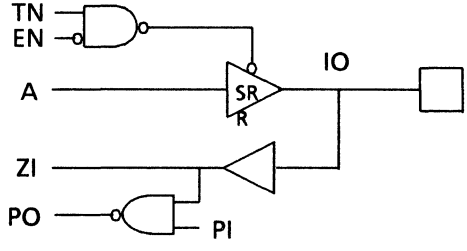


a. LOGIC SYMBOL

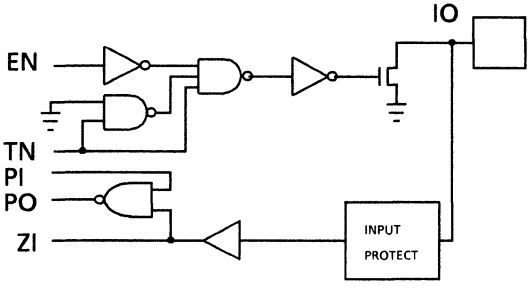
ELECTRICAL SCHEMATICS



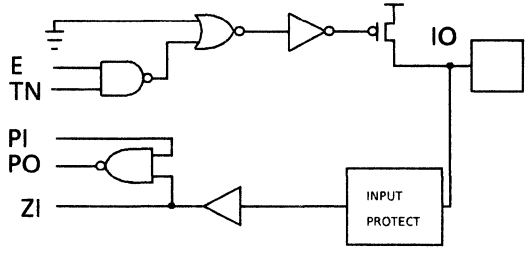
b. BIDIRECT BUFFER WITH OPTIONAL PULL-UP / PULL-DOWN



c. BIDIRECT BUFFER WITH SLEW RATE CONTROL AND OPTIONAL PULL-UP / PULL-DOWN



d. BIDIRECT BUFFER WITH OPEN DRAIN



e. BIDIRECT BUFFER WITH OPEN SOURCE

Figure 2.4

BD1 BIDIRECT BUFFERS

BD1T-TTL INPUT	/ **BD1TU**-PULL-UP	/ **BD1TD**-PULL-DOWN
BD1TN-INVERTED TTL INPUT	/ **BD1TNU**-PULL-UP	/ **BD1TND**-PULL-DOWN
BD1C-CMOS INPUT	/ **BD1CU**-PULL-UP	/ **BD1CD**-PULL-DOWN
BD1CN-INVERTED CMOS INPUT	/ **BD1CNU**-PULL-UP	/ **BD1CND**-PULL-DOWN
BD1SC-SCHMITT INPUT	/ **BD1SCU**-PULL-UP	/ **BD1SCD**-PULL-DOWN
BD1SCN-INVERTED SCHMITT INPUT	/ **BD1SCNU**-PULL-UP	/ **BD1SCND**-PULL-DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not include

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH} t_{PHL}	5.5 4.8	13.1 10.5	20.7 16.2	23.9 18.6
t_{PLZ}	(INTRINSIC DELAY = 2.3)			
t_{PZL}	4.6	10.3	16.0	18.4
t_{PHZ}	(INTRINSIC DELAY = 1.8)			
t_{PZH}	5.5	13.1	20.7	23.9

IO Output Slope 1 (ns/pf) = 0.2166 Incpt (ns) = 2.26
Slope 0 (ns/pf) = 0.1625 Incpt (ns) = 2.37

Coding Syntax: (IO, ZI, PO) = &BD1% (IO, A,EN,TN,PI);
Input Loading: (-, 1, 2, 2, 1)
Input capacitance:device(1.5pf) + pad(1pf) = 2.5pf

(IO-ZI) delays for all the cells with { TLCHTD, TLCHTN, IBUF, IBUFN, SCHMITC, SCHMITCN } input please refer to { TTL, INVERTED TTL, CMOS, INVERTED CMOS, SCHMITT TRIGGER, INVERTED SCHMITT TRIGGER } delay time

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD1 BIDIRECT BUFFERS

BD1TOD-OPEN DRAIN

BD1TNOD-OPEN DRAIN

BD1COD-OPEN DRAIN

BD1CNOD-OPEN DRAIN

BD1SCOD-OPEN DRAIN

BD1SCNOD-OPEN DRAIN

BD1TOS-OPEN SOURCE

BD1TNOS-OPEN SOURCE

BD1COS-OPEN SOURCE

BD1CNOS-OPEN SOURCE

BD1SCOS-OPEN SOURCE

BD1SCNOS-OPEN SOURCE

BD1TOD / BD1TNOD / BD1COD / BD1CNOD / BD1SCOD / BD1SCNOD(EN-IO)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLZ}	(INTRINSIC DELAY = 2.3)			
t_{PZL}	4.6	10.3	16.0	18.4

IO Output Slope 0 $_{(ns/pf)}$ = 0.1625 Incpt $_{(ns)}$ = 2.17

Coding Syntax: (IO, ZI, PO) = &BD1% (IO, EN,TN,PI);
Input Loading: (-, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

BD1TOS / BD1TNOS / BD1COS / BD1CNOS / BD1SCOS / BD1SCNOS(E-IO)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PHZ}	(INTRINSIC DELAY = 1.8)			
t_{PZH}	5.5	13.1	20.7	23.9

Z Output Slope 1 $_{(ns/pf)}$ = 0.2166 Incpt $_{(ns)}$ = 2.26

Coding Syntax: (IO, ZI, PO) = &BD1% (IO, EN,TN,PI);
Input Loading: (-, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD2 BIDIRECT BUFFERS

BD2T-TTL INPUT	/ **BD2TU**-PULL-UP	/ **BD2TD**-PULL-DOWN
BD2TN-INVERTED TTL INPUT	/ **BD2TNU**-PULL-UP	/ **BD2TND**-PULL-DOWN
BD2C-CMOS INPUT	/ **BD2CU**-PULL-UP	/ **BD2CD**-PULL-DOWN
BD2CN-INVERTED CMOS INPUT	/ **BD2CNU**-PULL-UP	/ **BD2CND**-PULL-DOWN
BD2SC-SCHMITT INPUT	/ **BD2SCU**-PULL-UP	/ **BD2SCD**-PULL-DOWN
BD2SCN-INVERTED SCHMITT INPUT	/ **BD2SCNU**-PULL-UP	/ **BD2SCND**-PULL-DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not include

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	4.0	8.5	13.1	15.0
t_{PHL}	3.3	6.2	9.0	10.3
t_{PLZ}	(INTRINSIC DELAY = 1.7)			
t_{PZL}	3.1	6.0	8.8	10.1
t_{PHZ}	(INTRINSIC DELAY = 1.8)			
t_{PZH}	4.0	8.5	13.1	15.0

IO Output Slope 1 (ns/pf) = 0.1297 Incpt (ns) = 2.04
Slope 0 (ns/pf) = 0.0820 Incpt (ns) = 2.08

Coding Syntax: (IO, ZI, PO) = &BD2% (IO, A,EN,TN,PI);
Input Loading: (-, 1, 2, 2, 1)
Input capacitance:device(1.5pf) + pad(1pf) = 2.5p

(IO-ZI) delays for all the cells with { TLCHTD, TLCHTN, IBUF, IBUFN, SCHMITC, SCHMITCN } input please refer to { TTL, INVERTED TTL, CMOS, INVERTED CMOS, SCHMITT TRIGGER, INVERTED SCHMITT TRIGGER } delay time

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD2 BIDIRECT BUFFERS

BD2TOD-OPEN DRAIN

BD2TNOD-OPEN DRAIN

BD2COD-OPEN DRAIN

BD2CNOD-OPEN DRAIN

BD2SCOD-OPEN DRAIN

BD2SCNOD-OPEN DRAIN

BD2TOS-OPEN SOURCE

BD2TNOS-OPEN SOURCE

BD2COS-OPEN SOURCE

BD2CNOS-OPEN SOURCE

BD2SCOS-OPEN SOURCE

BD2SCNOS-OPEN SOURCE

BD2TOD / BD2TNOD / BD2COD / BD2CNOD / BD2SCOD / BD2SCNOD(EN-IO)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLZ}	(INTRINSIC DELAY = 1.7)			
t_{PZL}	3.1	6.0	8.8	10.1

IO Output Slope 0 $_{(ns/pf)}$ = 0.0820 Incpt $_{(ns)}$ = 1.88

Coding Syntax: (IO, ZI, PO) = &BD2% (IO, EN,TN,PI);
Input Loading: (-, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

BD2TOS / BD2TNOS / BD2COS / BD2CNOS / BD2SCOS / BD2SCNOS(E-IO)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PHZ}	(INTRINSIC DELAY = 1.8)			
t_{PZH}	4.0	8.5	13.1	15.0

IO Output Slope 1 $_{(ns/pf)}$ = 0.1297 Incpt $_{(ns)}$ = 2.04

Coding Syntax: (IO, ZI, PO) = &BD2% (IO, EN,TN,PI);
Input Loading: (-, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD4 BIDIRECT BUFFERS

BD4T-TTL INPUT	/ **BD4TU**-PULL-UP	/ **BD4TD**-PULL-DOWN
BD4TN-INVERTED TTL INPUT	/ **BD4TNU**-PULL-UP	/ **BD4TND**-PULL-DOWN
BD4C-CMOS INPUT	/ **BD4CU**-PULL-UP	/ **BD4CD**-PULL-DOWN
BD4CN-INVERTED CMOS INPUT	/ **BD4CNU**-PULL-UP	/ **BD4CND**-PULL-DOWN
BD4SC-SCHMITT INPUT	/ **BD4SCU**-PULL-UP	/ **BD4SCD**-PULL-DOWN
BD4SCN-INVERTED SCHMITT INPUT	/ **BD4SCNU**-PULL-UP	/ **BD4SCND**-PULL-DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not include

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH} t_{PHL}	2.9 2.8	5.2 4.2	7.5 5.7	8.5 6.4
t_{PLZ}	(INTRINSIC DELAY = 1.7)			
t_{PZL}	2.6	4.0	5.5	6.2
t_{PHZ}	(INTRINSIC DELAY = 1.8)			
t_{PZH}	2.9	5.2	7.5	8.5

IO Output Slope 1 (ns/pf) = 0.0658 Incpt (ns) = 1.91
Slope 0 (ns/pf) = 0.0423 Incpt (ns) = 2.13

Coding Syntax: (IO, ZI, PO) = &BD4% (IO, A,EN,TN,PI);
Input Loading: (-, 1, 2, 2, 1)
Input capacitance:device(1.5pf) + pad(1pf) = 2.5pf

(IO-ZI) delays for all the cells with { TLCHTD, TLCHTN, IBUF, IBUFN, SCHMITC, SCHMITCN } input please refer to { TTL, INVERTED TTL, CMOS, INVERTED CMOS, SCHMITT TRIGGER, INVERTED SCHMITT TRIGGER } delay time

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD4 BIDIRECT BUFFERS

BD4TOD-OPEN DRAIN

BD4TNOD-OPEN DRAIN

BD4COD-OPEN DRAIN

BD4CNOD-OPEN DRAIN

BD4SCOD-OPEN DRAIN

BD4SCNOD-OPEN DRAIN

BD4TOS-OPEN SOURCE

BD4TNOS-OPEN SOURCE

BD4COS-OPEN SOURCE

BD4CNOS-OPEN SOURCE

BD4SCOS-OPEN SOURCE

BD4SCNOS-OPEN SOURCE

BD4TOD / BD4TNOD / BD4COD / BD4CNOD / BD4SCOD / BD4SCNOD(EN-IO)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLZ}	(INTRINSIC DELAY = 1.7)			
t_{PZL}	2.6	4.0	5.5	6.2

IO Output Slope 0 (ns/pf) = 0.0423 Incpt (ns) = 1.93

Coding Syntax: (IO, ZI, PO) = &BD4% (IO, EN,TN,PI);
Input Loading: (-, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

BD4TOS / BD4TNOS / BD4COS / BD4CNOS / BD4SCOS / BD4SCNOS(E-IO)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PHZ}	(INTRINSIC DELAY = 1.8)			
t_{PZH}	2.9	5.2	7.5	8.5

IO Output Slope 1 (ns/pf) = 0.0658 Incpt (ns) = 1.91

Coding Syntax: (IO, ZI, PO) = &BD4% (IO, EN,TN,PI);
Input Loading: (-, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD4 BIDIRECT BUFFERS

BD4TR-SLEW RATE CONTROL
BD4TNR-SLEW RATE CONTROL
BD4CR-SLEW RATE CONTROL
BD4CNR-SLEW RATE CONTROL
BD4SCR-SLEW RATE CONTROL
BD4SCNR-SLEW RATE CONTROL

BD4TRU-PULL UP
BD4TNRU-PULL UP
BD4CRU-PULL UP
BD4CNRU-PULL UP
BD4SCRU-PULL UP
BD4SCNRU-PULL UP

BD4TRD-PULL DOWN
BD4TNRD-PULL DOWN
BD4CRD-PULL DOWN
BD4CNRD-PULL DOWN
BD4SCRD-PULL DOWN
BD4SCNRD-PULL DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	4.6	8.5	12.3	13.9
t_{PHL}	4.0	7.3	10.6	12.0

IO Output
Slope 1 (ns/pf) = 0.1094 Incpt (ns) = 2.99
Slope 0 (ns/pf) = 0.0942 Incpt (ns) = 2.59

Coding Syntax: (IO, ZI, PO) = &BD4% (IO, A,EN,TN,PI);
Input Loading: (-, 1, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

BD4TRP-MODERATE SLEW RATE
BD4TNRP-MODERATE SLEW RATE
BD4CRP-MODERATE SLEW RATE
BD4CNRP-MODERATE SLEW RATE
BD4SCRP-MODERATE SLEW RATE
BD4SCNRP-MODERATE SLEW RATE

BD4TRPU-PULL UP
BD4TNRPU-PULL UP
BD4CRPU-PULL UP
BD4CNRPU-PULL UP
BD4SCRPU-PULL UP
BD4SCNRPU-PULL UP

BD4TRPD-PULL DOWN
BD4TNRPD-PULL DOWN
BD4CRPD-PULL DOWN
BD4CNRPD-PULL DOWN
BD4SCRPD-PULL DOWN
BD4SCNRPD-PULL DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	3.8	6.9	10.0	11.4
t_{PHL}	3.5	6.2	8.9	10.0

IO Output
Slope 1 (ns/pf) = 0.0892 Incpt (ns) = 2.45
Slope 0 (ns/pf) = 0.0766 Incpt (ns) = 2.36

Coding Syntax: (IO, ZI, PO) = &BD4% (IO, A,EN,TN,PI);
Input Loading: (-, 1, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD6 BIDIRECT BUFFERS

BD6T-TTL INPUT	/ **BD6TU**-PULL-UP	/ **BD6TD**-PULL-DOWN
BD6TN-INVERTED TTL INPUT	/ **BD6TNU**-PULL-UP	/ **BD6TND**-PULL-DOWN
BD6C-CMOS INPUT	/ **BD6CU**-PULL-UP	/ **BD6CD**-PULL-DOWN
BD6CN-INVERTED CMOS INPUT	/ **BD6CNU**-PULL-UP	/ **BD6CND**-PULL-DOWN
BD6SC-SCHMITT INPUT	/ **BD6SCU**-PULL-UP	/ **BD6SCD**-PULL-DOWN
BD6SCN-INVERTED SCHMITT INPUT	/ **BD6SCNU**-PULL-UP	/ **BD6SCND**-PULL-DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not include

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH} t_{PHL}	2.7 2.6	4.3 3.7	5.9 4.7	6.6 5.1
t_{PLZ}	(INTRINSIC DELAY = 1.7)			
t_{PZL}	2.4	3.5	4.5	4.9
t_{PHZ}	(INTRINSIC DELAY = 2.0)			
t_{PZH}	2.7	4.3	5.9	6.6

IO Output	Slope 1 (ns/pf) =	0.0458	Incpt	=	2.01
	Slope 0 (ns/pf) =	0.0294	Incpt	=	2.19

Coding Syntax: (IO, ZI, PO) = &BD6% (IO, A,EN,TN,PI);
Input Loading: (- , 1, 2, 2, 1)
Input capacitance:device(1.5pf) + pad(1pf) = 2.5pf

(IO-ZI) delays for all the cells with { TLCHTD, TLCHTN, IBUF, IBUFN, SCHMITC, SCHMITCN } input please refer to { TTL, INVERTED TTL, CMOS, INVERTED CMOS, SCHMITT TRIGGER, INVERTED SCHMITT TRIGGER } delay time

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD6 BIDIRECT BUFFERS

BD6TOD-OPEN DRAIN

BD6TNOD-OPEN DRAIN

BD6COD-OPEN DRAIN

BD6CNOD-OPEN DRAIN

BD6SCOD-OPEN DRAIN

BD6SCNOD-OPEN DRAIN

BD6TOS-OPEN SOURCE

BD6TNOS-OPEN SOURCE

BD6COS-OPEN SOURCE

BD6CNOS-OPEN SOURCE

BD6SCOS-OPEN SOURCE

BD6SCNOS-OPEN SOURCE

BD6TOD / BD6TNOD / BD6COD / BD6CNOD / BD6SCOD / BD6SCNOD(EN-IO)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLZ}	(INTRINSIC DELAY = 1.7)			
t_{PZL}	2.4	3.5	4.5	4.9

IO Output Slope 0 $_{(ns/pf)}$ = 0.0294 Incpt $_{(ns)}$ = 1.99

Coding Syntax: (IO, ZI, PO) = &BD6% (IO, EN,TN,PI);
Input Loading: (-, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

BD6TOS / BD6TNOS / BD6COS / BD6CNOS / BD6SCOS / BD6SCNOS(E-IO)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PHZ}	(INTRINSIC DELAY = 2.0)			
t_{PZH}	2.7	4.3	5.9	6.6

IO Output Slope 1 $_{(ns/pf)}$ = 0.0458 Incpt $_{(ns)}$ = 2.01

Coding Syntax: (IO, ZI, PO) = &BD6% (IO, EN,TN,PI);
Input Loading: (-, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD6 BIDIRECT BUFFERS

BD6TR-SLEW RATE CONTROL
BD6TNR-SLEW RATE CONTROL
BD6CR-SLEW RATE CONTROL
BD6CNR-SLEW RATE CONTROL
BD6SCR-SLEW RATE CONTROL
BD6SCNR-SLEW RATE CONTROL

BD6TRU-PULL UP
BD6TNRU-PULL UP
BD6CRU-PULL UP
BD6CNRU-PULL UP
BD6SCRU-PULL UP
BD6SCNRU-PULL UP

BD6TRD-PULL DOWN
BD6TNRD-PULL DOWN
BD6CRD-PULL DOWN
BD6CNRD-PULL DOWN
BD6SCRD-PULL DOWN
BD6SCNRD-PULL DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	3.9	7.1	10.3	11.7
t_{PHL}	3.5	6.3	9.1	10.4

IO Output
Slope 1 $_{(ns/pf)}$ = 0.0917
Slope 0 $_{(ns/pf)}$ = 0.0809
Incpt $_{(ns)}$ = 2.52
Incpt $_{(ns)}$ = 2.27

Coding Syntax: (IO, ZI, PO) = &BD6% (IO, A,EN,TN,PI);
Input Loading: (- , 1, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

BD6TRP-MODERATE SLEW RATE
BD6TNRP-MODERATE SLEW RATE
BD6CRP-MODERATE SLEW RATE
BD6CNRP-MODERATE SLEW RATE
BD6SCRP-MODERATE SLEW RATE
BD6SCNRP-MODERATE SLEW RATE

BD6TRPU-PULL UP
BD6TNRPU-PULL UP
BD6CRPU-PULL UP
BD6CNRPU-PULL UP
BD6SCRPU-PULL UP
BD6SCNRPU-PULL UP

BD6TRPD-PULL DOWN
BD6TNRPD-PULL DOWN
BD6CRPD-PULL DOWN
BD6CNRPD-PULL DOWN
BD6SCRPD-PULL DOWN
BD6SCNRPD-PULL DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	3.4	6.0	8.6	9.7
t_{PHL}	3.1	5.0	7.0	7.8

IO Output
Slope 1 $_{(ns/pf)}$ = 0.0742
Slope 0 $_{(ns/pf)}$ = 0.0555
Incpt $_{(ns)}$ = 2.29
Incpt $_{(ns)}$ = 2.25

Coding Syntax: (IO, ZI, PO) = &BD6% (IO, A,EN,TN,PI);
Input Loading: (- , 1, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD8 BIDIRECT BUFFERS

BD8T-TTL INPUT	/ **BD8TU**-PULL-UP	/ **BD8TD**-PULL-DOWN
BD8TN-INVERTED TTL INPUT	/ **BD8TNU**-PULL-UP	/ **BD8TND**-PULL-DOWN
BD8C-CMOS INPUT	/ **BD8CU**-PULL-UP	/ **BD8CD**-PULL-DOWN
BD8CN-INVERTED CMOS INPUT	/ **BD8CNU**-PULL-UP	/ **BD8CND**-PULL-DOWN
BD8SC-SCHMITT INPUT	/ **BD8SCU**-PULL-UP	/ **BD8SCD**-PULL-DOWN
BD8SCN-INVERTED SCHMITT INPUT	/ **BD8SCNU**-PULL-UP	/ **BD8SCND**-PULL-DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not include

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	2.6	3.9	5.1	5.7
t_{PHL}	2.7	3.6	4.4	4.8
t_{PLZ}	(INTRINSIC DELAY = 1.8)			
t_{PZL}	2.5	3.4	4.2	4.6
t_{PHZ}	(INTRINSIC DELAY = 2.2)			
t_{PZH}	2.6	3.9	5.1	5.7

IO Output Slope 1 (ns/pf) = 0.0361 Incpt (ns) = 2.07
Slope 0 (ns/pf) = 0.0245 Incpt (ns) = 2.35

Coding Syntax: (IO, ZI, PO) = &BD8% (IO, A,EN,TN,PI);
Input Loading: (-, 1, 2, 2, 1)
Input capacitance:device(1.5pf) + pad(1pf) = 2.5pf

(IO-ZI) delays for all the cells with { TLCHTD, TLCHTN, IBUF, IBUFN, SCHMITC, SCHMITCN } input please refer to { TTL, INVERTED TTL, CMOS, INVERTED CMOS, SCHMITT TRIGGER, INVERTED SCHMITT TRIGGER } delay time

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD8 BIDIRECT BUFFERS

BD8TOD-OPEN DRAIN

BD8TNOD-OPEN DRAIN

BD8COD-OPEN DRAIN

BD8CNOD-OPEN DRAIN

BD8SCOD-OPEN DRAIN

BD8SCNOD-OPEN DRAIN

BD8TOS-OPEN SOURCE

BD8TNOS-OPEN SOURCE

BD8COS-OPEN SOURCE

BD8CNOS-OPEN SOURCE

BD8SCOS-OPEN SOURCE

BD8SCNOS-OPEN SOURCE

BD8TOD / BD8TNOD / BD48OD / BD8CNOD / BD8SCOD / BD48CNOD(EN-IO)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLZ}	(INTRINSIC DELAY = 1.8)			
t_{PZL}	2.5	3.4	4.2	4.6

IO Output Slope 0 $_{(ns/pf)}$ = 0.0245 Incpt $_{(ns)}$ = 2.15

Coding Syntax: (IO, ZI, PO) = &BD8% (IO, EN,TN,PI);
Input Loading: (-, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

BD8TOS / BD8TNOS / BD8COS / BD8CNOS / BD8SCOS / BD8SCNOS(E-IO)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PHZ}	(INTRINSIC DELAY = 2.2)			
t_{PZH}	2.6	3.9	5.1	5.7

IO Output Slope 1$_{(ns/pf)}$ = 0.0361 Incpt $_{(ns)}$ = 2.07

Coding Syntax: (IO, ZI, PO) = &BD8% (IO, EN,TN,PI);
Input Loading: (-, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD8 BIDIRECT BUFFERS

BD8TR-SLEW RATE CONTROL
BD8TNR-SLEW RATE CONTROL
BD8CR-SLEW RATE CONTROL
BD8CNR-SLEW RATE CONTROL
BD8SCR-SLEW RATE CONTROL
BD8SCNR-SLEW RATE CONTROL

BD8TRU-PULL UP
BD8TNRU-PULL UP
BD8CRU-PULL UP
BD8CNRU-PULL UP
BD8SCRU-PULL UP
BD8SCNRU-PULL UP

BD8TRD-PULL DOWN
BD8TNRD-PULL DOWN
BD8CRD-PULL DOWN
BD8CNRD-PULL DOWN
BD8SCRD-PULL DOWN
BD8SCNRD-PULL DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	3.5	6.1	8.8	10.0
t_{PHL}	3.3	5.2	7.2	8.0

IO Output Slope 1 (ns/pf) = 0.0764 Incpt(ns) = 2.32
Slope 0 (ns/pf) = 0.0555 Incpt(ns) = 2.45

Coding Syntax: (IO, ZI, PO) = &BD8% (IO, A,EN,TN,PI);
Input Loading: (-, 1, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

BD8TRP-MODERATE SLEW RATE
BD8TNRP-MODERATE SLEW RATE
BD8CRP-MODERATE SLEW RATE
BD8CNRP-MODERATE SLEW RATE
BD8SCRP-MODERATE SLEW RATE
BD8SCNRP-MODERATE SLEW RATE

BD8TRPU-PULL UP
BD8TNRPU-PULL UP
BD8CRPU-PULL UP
BD8CNRPU-PULL UP
BD8SCRPU-PULL UP
BD8SCNRPU-PULL UP

BD8TRPD-PULL DOWN
BD8TNRPD-PULL DOWN
BD8CRPD-PULL DOWN
BD8CNRPD-PULL DOWN
BD8SCRPD-PULL DOWN
BD8SCNRPD-PULL DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	3.1	5.4	7.6	8.5
t_{PHL}	3.1	4.5	6.0	6.7

IO Output Slope 1 (ns/pf) = 0.0636 Incpt (ns) = 2.18
Slope 0 (ns/pf) = 0.0423 Incpt (ns) = 2.43

Coding Syntax: (IO, ZI, PO) = &BD8% (IO, A,EN,TN,PI);
Input Loading: (-, 1, 2, 2, 1)
Input capacitance: device(1.5pf) + pad(1pf) = 2.5pf

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD12 BIDIRECT BUFFERS

BD12T-TTL INPUT	/ **BD12TU**-PULL-UP	/ **BD12TD**-PULL-DOWN
BD12TN-INVERTED TTL INPUT	/ **BD12TNU**-PULL-UP	/ **BD12TND**-PULL-DOWN
BD12C-CMOS INPUT	/ **BD12CU**-PULL-UP	/ **BD12CD**-PULL-DOWN
BD12CN-INVERTED CMOS INPUT	/ **BD12CNU**-PULL-UP	/ **BD12CND**-PULL-DOWN
BD12SC-SCHMITT INPUT	/ **BD12SCU**-PULL-UP	/ **BD12SCD**-PULL-DOWN
BD12SCN-INVERTED SCHMITT INPUT	/ **BD12SCNU**-PULL-UP	/ **BD12SCND**-PULL-DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not include

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH} t_{PHL}	2.4 2.4	3.2 3.0	4.0 3.6	4.3 3.8
t_{PLZ}	(INTRINSIC DELAY = 1.6)			
t_{PZL}	2.2	2.8	3.4	3.6
t_{PHZ}	(INTRINSIC DELAY = 2.0)			
t_{PZH}	2.4	3.2	4.0	4.3

IO Output Slope 1 (ns/pf) = 0.0225 Incpt = 2.07
Slope 0 (ns/pf) = 0.0166 Incpt = 2.16

Coding Syntax: (IO, ZI, PO) = &BD12% (IO, A,EN,TN,PI);
Input Loading: (-, 2, 4, 4, 1)
Input capacitance: device(2.5pf) + pad(1pf) = 3.5pf

(IO-ZI) delays for all the cells with { TLCHTD, TLCHTN, IBUF, IBUFN, SCHMITC, SCHMITCN } input please refer to { TTL, INVERTED TTL, CMOS, INVERTED CMOS, SCHMITT TRIGGER, INVERTED SCHMITT TRIGGER } delay time

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD12 BIDIRECT BUFFERS

BD12TOD-OPEN DRAIN

BD12TNOD-OPEN DRAIN

BD12COD-OPEN DRAIN

BD12CNOD-OPEN DRAIN

BD12SCOD-OPEN DRAIN

BD12SCNOD-OPEN DRAIN

BD12TOS-OPEN SOURCE

BD12TNOS-OPEN SOURCE

BD12COS-OPEN SOURCE

BD12CNOS-OPEN SOURCE

BD12SCOS-OPEN SOURCE

BD12SCNOS-OPEN SOURCE

BD12TOD / BD12TNOD / BD12COD / BD12CNOD / BD12SCOD / BD12SCNOD(EN-IO)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLZ}	(INTRINSIC DELAY = 1.6)			
t_{PZL}	2.2	2.8	3.4	3.6

IO Output Slope 0(ns/pf) = 0.0166 Incpt = 1.96

Coding Syntax: (IO, ZI, PO) = &BD12% (IO, EN,TN,PI);
Input Loading: (- , 4, 4, 1)
Input capacitance: device(2.5pf) + pad(1pf) = 3.5pf

BD12TOS / BD12TNOS / BD12COS / BD12CNOS / BD12SCOS / BD12SCNOS(E-IO)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PHZ}	(INTRINSIC DELAY = 2.0)			
t_{PZH}	2.4	3.2	4.0	4.3

IO Output Slope 1(ns/pf) = 0.0225 Incpt = 2.07

Coding Syntax: (IO, ZI, PO) = &BD12% (IO, EN,TN,PI);
Input Loading: (- , 4, 4, 1)
Input capacitance: device(2.5pf) + pad(1pf) = 3.5pf

NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

BD12 BIDIRECT BUFFERS

BD12TR-SLEW RATE CONTROL
BD12TNR-SLEW RATE CONTROL
BD12CR-SLEW RATE CONTROL
BD12CNR-SLEW RATE CONTROL
BD12SCR-SLEW RATE CONTROL
BD12SCNR-SLEW RATE CONTROL

BD12TRU-PULL UP
BD12TNRU-PULL UP
BD12CRU-PULL UP
BD12CNRU-PULL UP
BD12SCRU-PULL UP
BD12SCNRU-PULL UP

BD12TRD-PULL DOWN
BD12TNRD-PULL DOWN
BD12CRD-PULL DOWN
BD12CNRD-PULL DOWN
BD12SCRD-PULL DOWN
BD12SCNRD-PULL DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	2.9	4.8	6.7	7.5
t_{PHL}	2.9	4.3	5.8	6.4

IO Output
Slope 1 (ns/pf) = 0.0542 Incpt (ns) = 2.09
Slope 0 (ns/pf) = 0.0414 Incpt (ns) = 2.26

Coding Syntax: (IO, ZI, PO) = &BD12% (IO, A,EN,TN,PI);
Input Loading: (- , 2, 4, 4, 1)
Input capacitance: device(2.5pf) + pad(1pf) = 3.5pf

BD12TRP-MODERATE SLEW RATE
BD12TNRP-MODERATE SLEW RATE
BD12CRP-MODERATE SLEW RATE
BD12CNRP-MODERATE SLEW RATE
BD12SCRP-MODERATE SLEW RATE
BD12SCNRP-MODERATE SLEW RATE

BD12TRPU-PULL UP
BD12TNRPU-PULL UP
BD12CRPU-PULL UP
BD12CNRPU-PULL UP
BD12SCRPU-PULL UP
BD12SCNRPU-PULL UP

BD12TRPD-PULL DOWN
BD12TNRPD-PULL DOWN
BD12CRPD-PULL DOWN
BD12CNRPD-PULL DOWN
BD12SCRPD-PULL DOWN
BD12SCNRPD-PULL DOWN

(A-IO) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

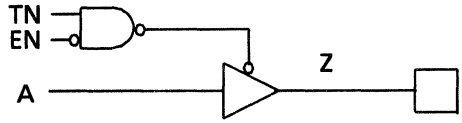
CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	2.7	4.1	5.5	6.2
t_{PHL}	2.7	3.6	4.6	5.1

IO Output
Slope 1 (ns/pf) = 0.0409 Incpt (ns) = 2.07
Slope 0 (ns/pf) = 0.0281 Incpt (ns) = 2.24

Coding Syntax: (IO, ZI, PO) = &BD12% (IO, A,EN,TN,PI);
Input Loading: (- , 2, 4, 4, 1)
Input capacitance: device(2.5pf) + pad(1pf) = 3.5pf

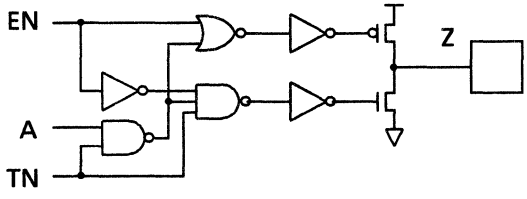
NOTE : % is a wildcard that represents ANY STRING OF CONFIGURED CHARACTERISTIC

THREE-STATE OUTPUT BUFFERS

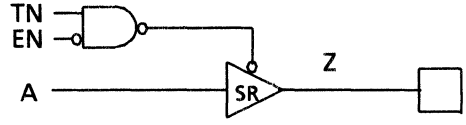


a. LOGIC SYMBOL

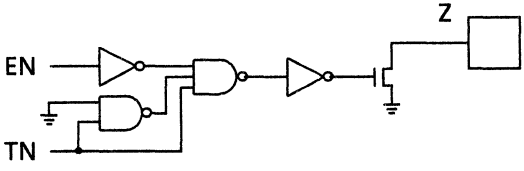
ELECTRICAL SCHEMATICS



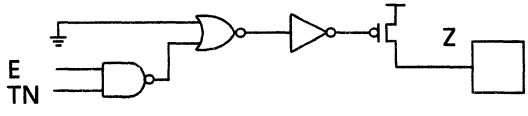
b. THREE-STATE BUFFER



c. THREE-STATE BUFFER WITH SLEW RATE CONTROL



d. THREE-STATE BUFFER WITH OPEN DRAIN



e. THREE-STATE BUFFER WITH OPEN SOURCE

Figure 2.3

BT1 THREE-STATE OUTPUT BUFFERS

BT1
1mA THREE-STATE BUFFER

BT1OD
1mA THREE-STATE BUFFER WITH OPEN DRAIN

BT1OS
1mA THREE-STATE BUFFER WITH OPEN SOURCE

BT1 (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH} t_{PHL}	5.4 4.7	13.0 10.4	20.6 16.1	23.8 18.5
t_{PLZ}	(INTRINSIC DELAY = 2.1)			
t_{PZL}	4.5	10.2	15.9	18.3
t_{PHZ}	(INTRINSIC DELAY = 1.8)			
t_{PZH}	5.4	13.0	20.6	23.8

IO Output Slope 1 (ns/pf) = 0.2166 Incpt (ns) = 2.16
Slope 0 (ns/pf) = 0.1625 Incpt (ns) = 2.27

Coding Syntax: Z = &BT1 (A,EN,TN);
Input Loading: (1, 2, 2)

BT1OD (EN-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLZ}	(INTRINSIC DELAY = 2.1)			
t_{PZL}	4.5	10.2	15.9	18.3

IO Output Slope 0 (ns/pf) = 0.1625 Incpt (ns) = 2.07

Coding Syntax: Z = &BT1OD (EN,TN);
Input Loading: (2, 2)

BT1OS (E-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PHZ}	(INTRINSIC DELAY = 1.8)			
t_{PZH}	5.4	13.0	20.6	23.8

IO Output Slope 1 (ns/pf) = 0.2166 Incpt (ns) = 2.16

Coding Syntax: Z = &BT1OS (E,TN);
Input Loading: (1, 2)

BT2 THREE-STATE OUTPUT BUFFERS

BT2
2mA THREE-STATE BUFFER

BT2OD
2mA THREE-STATE BUFFER WITH OPEN DRAIN

BT2OS
2mA THREE-STATE BUFFER WITH OPEN SOURCE

BT2 (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	3.9	8.5	13.0	15.0
t_{PHL}	3.2	6.1	9.0	10.2
t_{PLZ}	(INTRINSIC DELAY = 6.1)			
t_{PZL}	3.0	5.9	8.8	10.0
t_{PHZ}	(INTRINSIC DELAY = 1.8)			
t_{PZH}	5.4	13.0	20.6	23.8

IO Output Slope 1 (ns/pf) = 0.1303 Incpt (ns) = 1.96
Slope 0 (ns/pf) = 0.0825 Incpt (ns) = 1.97

Coding Syntax: Z = &BT2 (A,EN,TN);
Input Loading: (1, 2, 2)

BT2OD (EN-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLZ}	(INTRINSIC DELAY = 1.6)			
t_{PZL}	3.0	5.9	8.8	10.0

IO Output Slope 0 (ns/pf) = 0.0825 Incpt (ns) = 1.77

Coding Syntax: Z = &BT2OD (EN,TN);
Input Loading: (2, 2)

BT2OS (E-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PHZ}	(INTRINSIC DELAY = 1.8)			
t_{PZH}	3.9	8.5	13.0	15.0

IO Output Slope 1 (ns/pf) = 0.1303 Incpt (ns) = 1.96

Coding Syntax: Z = &BT2OS (E,TN);
Input Loading: (1, 2)

BT4 THREE-STATE OUTPUT BUFFERS

BT4
4mA THREE-STATE BUFFER

BT4OD
4mA THREE-STATE BUFFER WITH OPEN DRAIN

BT4OS
4mA THREE-STATE BUFFER WITH OPEN SOURCE

BT4 (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH} t_{PHL}	2.8 2.7	5.2 4.2	7.5 5.7	8.5 6.3
t_{PLZ}	(INTRINSIC DELAY = 1.6)			
t_{PZL}	2.5	4.0	5.5	6.1
t_{PHZ}	(INTRINSIC DELAY = 1.8)			
t_{PZH}	2.8	5.2	7.5	8.5

IO Output Slope 1 (ns/pf) = 0.0669 Incpt (ns) = 1.82
Slope 0 (ns/pf) = 0.0425 Incpt (ns) = 2.07

Coding Syntax: Z = &BT4 (A,EN,TN);
Input Loading: (1, 2, 2)

BT4OD (EN-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLZ}	(INTRINSIC DELAY = 1.6)			
t_{PZL}	2.5	4.0	5.5	6.1

IO Output Slope 0 (ns/pf) = 0.0425 Incpt (ns) = 1.87

Coding Syntax: Z = &BT4OD (EN,TN);
Input Loading: (2, 2)

BT4OS (E-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PHZ}	(INTRINSIC DELAY = 1.8)			
t_{PZH}	2.8	5.2	7.5	8.5

IO Output Slope 1 (ns/pf) = 0.0669 Incpt (ns) = 1.82

Coding Syntax: Z = &BT4OS (E,TN);
Input Loading: (1, 2)

BT4 THREE STATE OUTPUT BUFFERS

BT4R

4mA THREE-STATE BUFFER
WITH SLEW RATE

BT4RP

4mA THREE-STATE BUFFER
WITH MODERATE SLEW RATE

BT4R (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	4.6	8.4	12.2	13.9
t_{PHL}	3.9	7.2	10.5	12.0

IO Output

Slope 1 (ns/pf) = 0.1092 Incpt (ns) = 2.95
Slope 0 (ns/pf) = 0.0950 Incpt (ns) = 2.46

Coding Syntax: Z = &BT4R (A,EN,TN);
Input Loading: (1, 2, 2)

BT4RP (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	3.7	6.9	10.0	11.3
t_{PHL}	3.5	6.2	8.8	10.0

IO Output

Slope 1 (ns/pf) = 0.0894 Incpt (ns) = 2.39
Slope 0 (ns/pf) = 0.0761 Incpt (ns) = 2.37

Coding Syntax: Z = &BT4RP (A,EN,TN);
Input Loading: (1, 2, 2)

BT6 THREE-STATE OUTPUT BUFFERS

BT6
6mA THREE-STATE BUFFER

BT6OD
6mA THREE-STATE BUFFER WITH OPEN DRAIN

BT6OS
6mA THREE-STATE BUFFER WITH OPEN SOURCE

BT6 (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH} t_{PHL}	2.7 2.6	4.3 3.6	5.9 4.7	6.6 5.1
t_{PLZ}	(INTRINSIC DELAY = 1.7)			
t_{PZL}	2.4	3.4	4.5	4.9
t_{PHZ}	(INTRINSIC DELAY = 2.0)			
t_{PZH}	2.7	4.3	5.9	6.6

IO Output Slope 1 (ns/pf) = 0.0458 Incpt (ns) = 2.01
Slope 0 (ns/pf) = 0.0297 Incpt (ns) = 2.14

Coding Syntax: Z = &BT6 (A,EN,TN);
Input Loading: (1, 2, 2)

BT6OD (EN-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLZ}	(INTRINSIC DELAY = 1.7)			
t_{PZL}	2.4	3.4	4.5	4.9

IO Output Slope 0 (ns/pf) = 0.0297 Incpt (ns) = 1.94

Coding Syntax: Z = &BT6OD (EN,TN);
Input Loading: (2, 2)

BT6OS (E-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PHZ}	(INTRINSIC DELAY = 2.0)			
t_{PZH}	2.7	4.3	5.9	6.6

IO Output Slope 1 (ns/pf) = 0.0458 Incpt (ns) = 2.01

Coding Syntax: Z = &BT6OS (E,TN);
Input Loading: (1, 2)

BT6 THREE-STATE OUTPUT BUFFERS

BT6R

6mA THREE-STATE BUFFER
WITH SLEW RATE

BT6RP

6mA THREE-STATE BUFFER
WITH MODERATE SLEW RATE

BT6R (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	3.9	7.1	10.3	11.7
t_{PHL}	3.5	6.3	9.1	10.3

IO Output

Slope 1 (ns/pf) = 0.0917 Incpt (ns) = 2.52
Slope 0 (ns/pf) = 0.0800 Incpt (ns) = 2.30

Coding Syntax: Z = &BT6R (A,EN,TN);
Input Loading: (1, 2, 2)

BT6RP (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}(Z)	3.4	6.0	8.5	9.7
t_{PHL}(Z)	3.1	5.0	6.9	7.8

IO Output

Slope 1 (ns/pf) = 0.0736 Incpt (ns) = 2.30
Slope 0 (ns/pf) = 0.0550 Incpt (ns) = 2.26

Coding Syntax: Z = &BT6RP (A,EN,TN);
Input Loading: (1, 2, 2)

BT8 THREE-STATE OUTPUT BUFFERS

BT8
8mA THREE-STATE BUFFER

BT8OD
8mA THREE-STATE BUFFER WITH OPEN DRAIN

BT8OS
8mA THREE-STATE BUFFER WITH OPEN SOURCE

BT8 (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH} t_{PHL}	2.6 2.7	3.9 3.6	5.1 4.4	5.7 4.8
t_{PLZ}	(INTRINSIC DELAY = 1.8)			
	t_{PZL}	2.5	3.4	4.2 4.6
t_{PHZ}	(INTRINSIC DELAY = 2.2)			
t_{PZH}	2.6	3.9	5.1	5.7

IO Output Slope 1 (ns/pf) = 0.0361 Incpt (ns) = 2.07
Slope 0 (ns/pf) = 0.0245 Incpt (ns) = 2.35

Coding Syntax: Z = &BT8 (A,EN,TN);
Input Loading: (1, 2, 2)

BT8OD (EN-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLZ}	(INTRINSIC DELAY = 1.8)			
t_{PZL}	2.5	3.4	4.2	4.6

IO Output Slope 0 (ns/pf) = 0.0245 Incpt (ns) = 2.15

Coding Syntax: Z = &BT8OD (EN,TN);
Input Loading: (2, 2)

BT8OS (E-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PHZ}	(INTRINSIC DELAY = 2.2)			
t_{PZH}	2.6	3.9	5.1	5.7

IO Output Slope 1 (ns/pf) = 0.0361 Incpt (ns) = 2.07

Coding Syntax: Z = &BT8OS (E,TN);
Input Loading: (1, 2)

BT8 THREE-STATE OUTPUT BUFFERS

BT8R

8mA THREE-STATE BUFFER
WITH SLEW RATE

BT8RP

8mA THREE-STATE BUFFER
WITH MODERATE SLEW RATE

BT8R (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	3.4	6.1	8.8	9.9
t_{PHL}	3.3	5.2	7.1	8.0

IO Output Slope $1_{(ns/pf)}$ = 0.0766 $Incpt_{(ns)}$ = 2.26
Slope $0_{(ns/pf)}$ = 0.0550 $Incpt_{(ns)}$ = 2.46

Coding Syntax: Z = &BT8R (A,EN,TN);
Input Loading: (1, 2, 2)

BT8RP (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	3.1	5.3	7.6	8.5
t_{PHL}	3.0	4.5	6.0	6.6

IO Output Slope $1_{(ns/pf)}$ = 0.0639 $Incpt_{(ns)}$ = 2.13
Slope $0_{(ns/pf)}$ = 0.0425 $Incpt_{(ns)}$ = 2.37

Coding Syntax: Z = &BT8RP (A,EN,TN);
Input Loading: (1, 2, 2)

BT12 THREE-STATE OUTPUT BUFFERS

BT12
12mA THREE-STATE BUFFER

BT12OD
12mA THREE-STATE BUFFER WITH OPEN DRAIN

BT12OS
12mA THREE-STATE BUFFER WITH OPEN SOURCE

BT12 (A-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH} t_{PHL}	2.3 2.4	3.1 3.0	3.9 3.6	4.3 3.8
t_{PLZ}	(INTRINSIC DELAY = 1.6)			
t_{PZL}	2.2	2.8	3.4	3.6
t_{PHZ}	(INTRINSIC DELAY = 1.9)			
t_{PZH}	3	3.1	3.9	4.3

IO Output Slope 1 (ns/pf) = 0.0234 Incpt (ns) = 1.94
Slope 0 (ns/pf) = 0.0166 Incpt (ns) = 2.16

Coding Syntax: Z = &BT12 (A,EN,TN);
Input Loading: (2, 4, 4)

BT12OD (EN-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLZ}	(INTRINSIC DELAY = 1.6)			
t_{PZL}	2.2	2.8	3.4	3.6

IO Output Slope 0 (ns/pf) = 0.0166 Incpt (ns) = 1.96

Coding Syntax: Z = &BT12OD (EN,TN);
Input Loading: (4, 4)

BT12OS (E-Z)
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PHZ}	(INTRINSIC DELAY = 1.9)			
t_{PZH}	3	3.1	3.9	4.3

IO Output Slope 1 (ns/pf) = 0.0234 Incpt (ns) = 1.94

Coding Syntax: Z = &BT12OS (E,TN);
Input Loading: (2, 4)

BT12 THREE-STATE OUTPUT BUFFERS

BT12R

12mA THREE-STATE BUFFER
WITH SLEW RATE

BT12RP

12mA THREE-STATE BUFFER
WITH MODERATE SLEW RATE

BT12R (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	2.9	4.8	6.6	7.4
t_{PHL}	2.9	4.3	5.7	6.4

IO Output
Slope 1 (ns/pf) = 0.0528 Incpt (ns) = 2.13
Slope 0 (ns/pf) = 0.0409 Incpt (ns) = 2.27

Coding Syntax: Z = &BT12R (A,EN,TN);
Input Loading: (2, 4, 4)

BT12RP (A-Z)

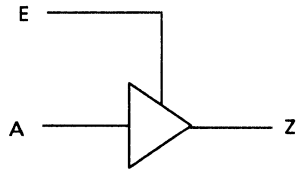
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

CLOAD	C = 15PF	C = 50PF	C = 85PF	C = 100PF
t_{PLH}	2.7	4.1	5.5	6.1
t_{PHL}	2.6	3.6	4.6	5.0

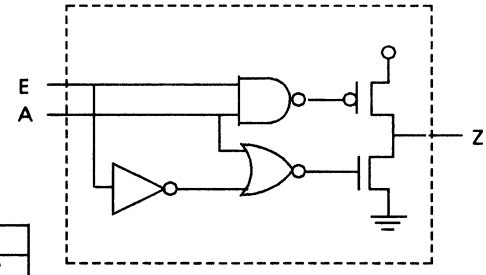
IO Output
Slope 1 (ns/pf) = 0.0400 Incpt (ns) = 2.10
Slope 0 (ns/pf) = 0.0283 Incpt (ns) = 2.18

Coding Syntax: Z = &BT12RP (A,EN,TN);
Input Loading: (2, 4, 4)

BTS4 / BTS4P THREE-STATE INTERNAL BUS DRIVER BTS4 / BTS4P



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

A	E	Z
x	0	Hi-Z
1	1	1
0	1	0

TRUTH TABLE

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

BTS4 (A/E TO Z) (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.5	0.7	0.8	1.0	1.6	2.7
t_{PHL}	0.8	0.9	0.9	1.0	1.2	1.7

Slope1 = 0.1458 Incpt = 0.39
Slope0 = 0.0589 Incpt = 0.75

Gate Count: 3
Coding Syntax: Z = BTS4 (A,E);
Input loading: (2,2)

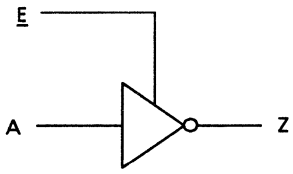
BTS4P (AE/ TO Z) (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.4	0.5	0.6	0.6	0.9	1.5
t_{PHL}	0.8	0.8	0.8	0.9	1.0	1.3

Slope1 = 0.0718 Incpt = 0.34
Slope0 = 0.0347 Incpt = 0.74

Gate Count: 4
Coding Syntax: Z = BTS4P (A,E);
Input loading: (2,2)

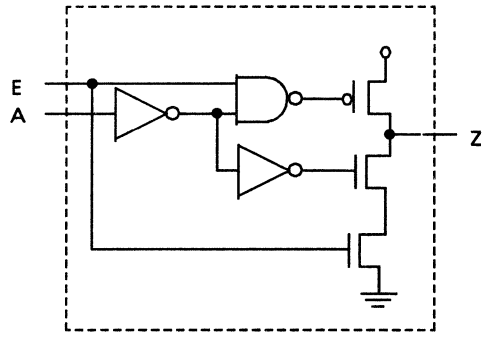
BTS5 / BTS5P INVERTING THREE-STATE INTERNAL BUS DRIVER BTS5 / BTS5P



LOGIC SYMBOL

A	E	Z
x	0	Hi-Z
1	1	0
0	1	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

BTS5 (A/E TO Z) (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.0	1.2	1.3	1.5	2.1	3.2
t_{PHL}	0.7	0.8	0.9	1.0	1.3	1.9

Slope1 = 0.1458 Incpt = 0.89
Slope0 = 0.0788 Incpt = 0.65

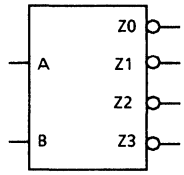
Gate Count: 3
Coding Syntax: Z = BTS5 (A, E);
Input loading: (1,1.5)

BTS5P (A/E TO Z) (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.1	1.1	1.2	1.3	1.5	2.1
t_{PHL}	0.8	0.8	0.9	0.9	1.1	1.4

Slope1 = 0.0678 Incpt = 1.00
Slope0 = 0.0411 Incpt = 0.75

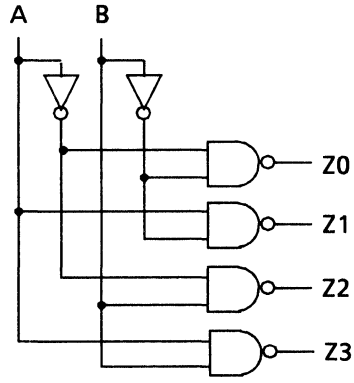
Gate Count: 4
Coding Syntax: Z = BTS5P (A, E);
Input loading: (1,1.5)



LOGIC SYMBOL

A	B	Z0	Z1	Z2	Z3
0	0	0	1	1	1
1	0	1	0	1	1
0	1	1	1	0	1
1	1	1	1	1	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

D24L (A OR B TO Z2 / Z3) (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}(Z2) t_{PHL}(Z2)	0.6 0.8	0.8 0.9	0.9 1.0	1.1 1.1	1.6 1.4	2.8 2.1
t_{PLH}(Z3) t_{PHL}(Z3)	0.6 0.2	0.8 0.3	0.9 0.4	1.1 0.5	1.6 0.8	2.7 1.5

Z2 Output Slope 1 = 0.1443 Incpt = 0.48
Slope 0 = 0.0854 Incpt = 0.73

Z3 Output Slope 1 = 0.1377 Incpt = 0.50
Slope 0 = 0.0854 Incpt = 0.13

Gate Count: 5
Coding Syntax: Z (Z0,Z1,Z2,Z3) = D24L (A,B);
Input Loading: (3,3)

D24LP (A OR B TO Z2 / Z3) (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}(Z2) t_{PHL}(Z2)	0.7 1.0	0.7 1.1	0.8 1.1	0.9 1.1	1.1 1.3	1.7 1.7
t_{PLH} (Z3) t_{PHL}(Z3)	0.6 0.2	0.6 0.3	0.7 0.3	0.7 0.3	1.0 0.5	1.5 0.9

Z2 Output Slope 1 = 0.0678 Incpt = 0.60
Slope 0 = 0.0453 Incpt = 0.96

Z3 Output Slope 1 = 0.0623 Incpt = 0.50
Slope 0 = 0.0453 Incpt = 0.16

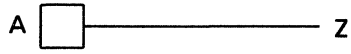
Gate Count: 9
Coding Syntax: Z (Z0,Z1,Z2,Z3) = D24LP (A,B);
Input Loading: (5,5)

DIRECT INPUT CLOCK DRIVER

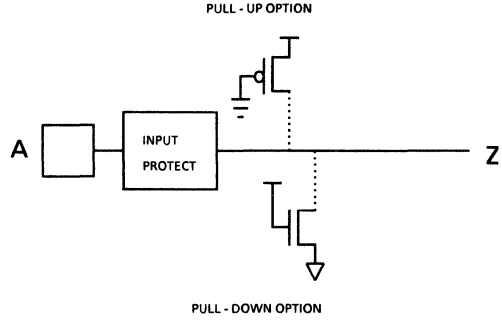
DDRV
DIRECT INPUT CLOCK DRIVER

DDRVU
DIRECT INPUT CLOCK DRIVER
WITH PULL-UP

DDRVD
DIRECT INPUT CLOCK DRIVER
WITH PULL-DOWN



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

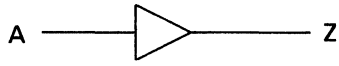
DDRV / DDRVU / DDRVD (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

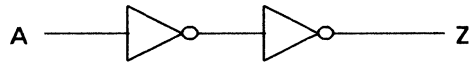
STD LOAD	50	100	200	300	400	500
t_{PLH}	0.0	0.0	0.0	0.0	0.0	0.0
t_{PHL}	0.0	0.0	0.0	0.0	0.0	0.0

Z Output Slope 1 = 0.0000 Incpt = 0.00
Slope 0 = 0.0000 Incpt = 0.00

Coding Syntax: Z = & DDRV (A);
Coding Syntax: Z = & DDRVU (A);
Coding Syntax: Z = & DDRV D (A);
Input Loading: (-)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf



LOGIC SYMBOL



SCHEMATIC

A	Z
0	0
1	1

TRUTH TABLE

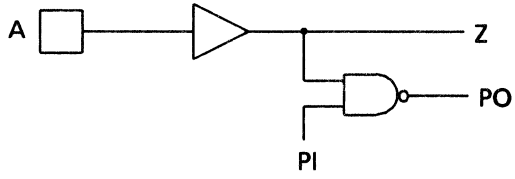
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

DRV8I (A - Z)

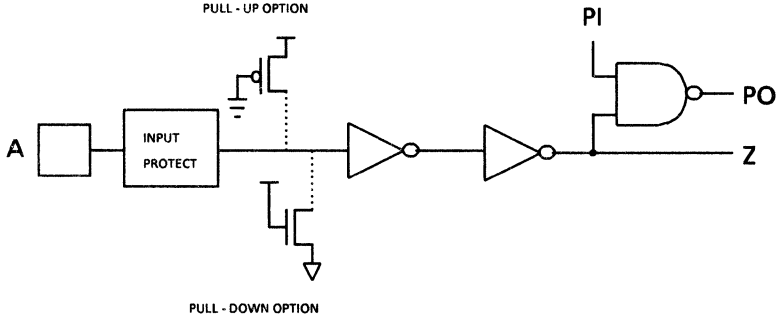
STD LOAD	100	200	400	600	800
t_{PLH} (Z)	1.0	1.2	1.6	2.0	2.5
t_{PHL} (Z)	1.0	1.2	1.5	1.9	2.2

Z Output	Slope 1	=	0.0021	Incpt	=	0.77
	Slope 0	=	0.0017	Incpt	=	0.85

Coding Syntax: Z = & DRV8I (A);
Input Loading: (8.3)



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

INPUT CLOCK DRIVER FOR CMOS

(2) DRVC(4) (8)	(2) DRVC(4)U (8)	(2) DRVC(4)D (8)
CLOCK DRIVER WITH CMOS INPUT	CLOCK DRIVER WITH CMOS INPUT AND PULL-UP	CLOCK DRIVER WITH CMOS INPUT AND PULL-DOWN

DRVC2 / DRVC2U / DRVC2D (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	25	50	75	100	200
t_{PLH}	1.0	1.3	1.7	2.0	3.3
t_{PHL}	1.0	1.4	1.6	2.1	3.4

Z Output Slope 1 = 0.0131 Incpt = 0.67
Slope 0 = 0.0128 Incpt = 0.80

Coding Syntax: (Z, PO) = &DRVC2 (A, PI);
Coding Syntax: (Z, PO) = &DRVC2U (A, PI);
Coding Syntax: (Z, PO) = &DRVC2D (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

DRVC4 / DRVC4U / DRVC4D (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	50	100	200	300	400
t_{PLH}	1.0	1.3	2.0	2.7	3.4
t_{PHL}	1.1	1.4	2.1	2.8	3.5

Z Output Slope 1 = 0.0068 Incpt = 0.65
Slope 0 = 0.0069 Incpt = 0.73

Coding Syntax: (Z, PO) = &DRVC4 (A, PI);
Coding Syntax: (Z, PO) = &DRVC4U (A, PI);
Coding Syntax: (Z, PO) = &DRVC4D (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

DRVC8 / DRVC8U / DRVC8D (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	100	200	300	400	600
t_{PLH}	1.2	1.6	2.0	2.4	3.2
t_{PHL}	1.3	1.7	2.1	2.5	3.3

Z Output Slope 1 = 0.0039 Incpt = 0.83
Slope 0 = 0.0040 Incpt = 0.90

Coding Syntax: (Z, PO) = &DRVC8 (A, PI);
Coding Syntax: (Z, PO) = &DRVC8U (A, PI);
Coding Syntax: (Z, PO) = &DRVC8D (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

INPUT CLOCK DRIVER FOR CMOS

DRVC16

CLOCK DRIVER WITH CMOS INPUT

DRVC16U

CLOCK DRIVER WITH CMOS INPUT AND PULL-UP

DRVC16D

CLOCK DRIVER WITH CMOS INPUT AND PULL-DOWN

DRVC16 / DRVC16U / DRVC16D (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	200	400	800	1200
t_{PLH}	1.4	1.8	2.6	3.4
t_{PHL}	1.5	1.9	2.7	3.5

Z Output Slope 1 = 0.0019 Incpt = 1.03
Slope 0 = 0.0020 Incpt = 1.10

Coding Syntax: (Z, PO) = &DRVC16 (A, PI);
Coding Syntax: (Z, PO) = &DRVC16U (A, PI);
Coding Syntax: (Z, PO) = &DRVC16D (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

INPUT CLOCK DRIVER FOR SCHMITT

(2) DRVSC (4) (8)	(2) DRVSC (4)U (8)	(2) DRVSC (4)D (8)
CLOCK DRIVER WITH SCHMITT CMOS INPUT	CLOCK DRIVER WITH SCHMITT CMOS INPUT AND PULL-UP	CLOCK DRIVER WITH SCHMITT CMOS INPUT AND PULL-DOWN

DRVSC2 / DRVSC2U / DRVSC2D (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	25	50	75	100	200
t_{PLH}	1.9	2.2	2.6	2.9	4.2
t_{PHL}	2.3	2.6	3.0	3.3	4.6

IO Output
Slope 1 (ns/pf) = 0.0131 Incpt (ns) = 1.57
Slope 0 (ns/pf) = 0.0131 Incpt (ns) = 1.97

Coding Syntax: (Z, PO) = &DRVSC2 (A, PI);
Coding Syntax: (Z,PO) = &DRVSC2U (A, PI);
Coding Syntax: (Z,PO) = &DRVSC2D (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

DRVSC4 / DRVSC4U / DRVSC4D (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	50	100	200	300	400
t_{PLH} (Z)	2.0	2.3	3.0	3.7	4.4
t_{PHL} (Z)	2.3	2.6	3.3	4.0	4.7

IO Output
Slope 1 (ns/pf) = 0.0068 Incpt (ns) = 1.65
Slope 0 (ns/pf) = 0.0069 Incpt (ns) = 1.93

Coding Syntax: (Z,PO) = &DRVSC4 (A, PI);
Coding Syntax: (Z,PO) = &DRVSC4U (A, PI);
Coding Syntax: (Z,PO) = &DRVSC4D (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

DRVSC8 / DRVSC8U / DRVSC8D (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	100	200	300	400	600
t_{PLH} (Z)	2.2	2.6	3.0	3.4	4.2
t_{PHL} (Z)	2.5	2.9	3.3	3.7	4.5

IO Output
Slope 1 (ns/pf) = 0.0039 Incpt (ns) = 1.83
Slope 0 (ns/pf) = 0.0040 Incpt (ns) = 2.10

Coding Syntax: (Z,PO) = &DRVSC8 (A, PI);
Coding Syntax: (Z,PO) = &DRVSC8U (A, PI);
Coding Syntax: (Z,PO) = &DRVSC8D (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

INPUT CLOCK DRIVER FOR SCHMITT

DRVSC16

CLOCK DRIVER WITH CMOS INPUT

DRVSC16U

CLOCK DRIVER WITH CMOS INPUT AND PULL-UP

DRVSC16D

CLOCK DRIVER WITH CMOS INPUT AND PULL-DOWN

DRVSC16 / DRVSC16U / DRVSC16D (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	200	400	800
t_{PLH}	2.5	2.9	3.7
t_{PHL}	2.7	3.1	3.9

Z Output Slope 1 = 0.0019 Incpt = 2.13
Slope 0 = 0.0020 Incpt = 2.30

Coding Syntax: (Z, PO) = &DRVSC16 (A, PI);
Coding Syntax: (Z, PO) = &DRVSC16U (A, PI);
Coding Syntax: (Z, PO) = &DRVSC16D (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

INPUT CLOCK DRIVER FOR TTL

(2) DRVT(4) (8)
CLOCK DRIVER WITH TTL INPUT

(2) DRVT(4)U (8)
CLOCK DRIVER WITH TTL INPUT AND PULL-UP

(2) DRVT(4)D (8)
CLOCK DRIVER WITH TTL INPUT AND PULL-DOWN

DRVT2 / DRVT2U / DRVT2D (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	25	50	75	100	200
t_{PLH}(Z)	1.5	1.8	2.2	2.5	3.8
t_{PHL}(Z)	1.5	1.8	2.2	2.5	3.8

Z Output Slope 1 = 0.0131 Incpt = 1.17
Slope 0 = 0.0131 Incpt = 1.17

Coding Syntax: (Z,PO) = &DRVT2 (A, PI);
Coding Syntax: (Z,PO) = &DRVT2U (A, PI);
Coding Syntax: (Z,PO) = &DRVT2D (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

DRVT4 / DRVT4U / DRVT4D (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	50	100	200	300	400
t_{PLH}(Z)	1.6	1.9	2.6	3.3	4.0
t_{PHL}(Z)	1.5	1.8	2.5	3.2	3.9

Z Output Slope 1 = 0.0068 Incpt = 1.25
Slope 0 = 0.0069 Incpt = 1.13

Coding Syntax: (Z,PO) = &DRVT4 (A, PI);
Coding Syntax: (Z,PO) = &DRVT4U (A, PI);
Coding Syntax: (Z,PO) = &DRVT4D (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

DRVT8 / DRVT8U / DRVT8D (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	100	200	300	400	600
t_{PLH}(Z)	1.8	2.2	2.6	3.0	3.8
t_{PHL}(Z)	1.7	2.1	2.5	2.9	3.7

Z Output Slope 1 = 0.0039 Incpt = 1.43
Slope 0 = 0.0040 Incpt = 1.30

Coding Syntax: (Z,PO) = &DRVT8 (A, PI);
Coding Syntax: (Z,PO) = &DRVT8U (A, PI);
Coding Syntax: (Z,PO) = &DRVT8D (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

INPUT CLOCK DRIVER FOR TTL

DRVT16

CLOCK DRIVER WITH CMOS INPUT

DRVT16U

CLOCK DRIVER WITH CMOS INPUT AND PULL-UP

DRVT16D

CLOCK DRIVER WITH CMOS INPUT AND PULL-DOWN

DRVT16 / DRVT16U / DRVT16D (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	200	400	800	1200
t_{PLH}	2.0	2.4	3.2	4.0
t_{PHL}	1.9	2.3	3.1	3.9

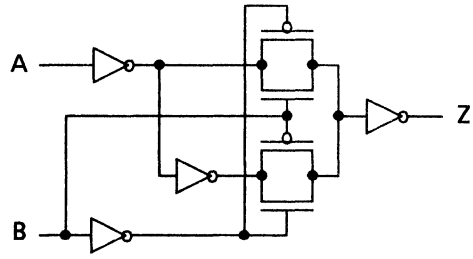
Z Output Slope 1 = 0.0019 Incpt = 1.63
Slope 0 = 0.0020 Incpt = 1.50

Coding Syntax: (Z, PO) = &DRVT16 (A, PI);
Coding Syntax: (Z, PO) = &DRVT16U (A, PI);
Coding Syntax: (Z, PO) = &DRVT16D (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

LOGIC SYMBOL

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

EN (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.9	1.1	1.2	1.4	2.0	3.1
t_{PHL}	1.1	1.2	1.3	1.3	1.6	2.1

Slope1 = 0.1458 Incpt = 0.79
Slope0 = 0.0653 Incpt = 1.06

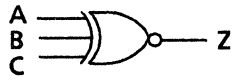
Gate Count: 3
Coding Syntax: Z = EN (A,B);
Input loading: (1,2)

ENP (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.9	1.0	1.1	1.1	1.4	2.0
t_{PHL}	1.1	1.1	1.2	1.2	1.4	1.7

Slope1 = 0.0718 Incpt = 0.84
Slope0 = 0.0411 Incpt = 1.05

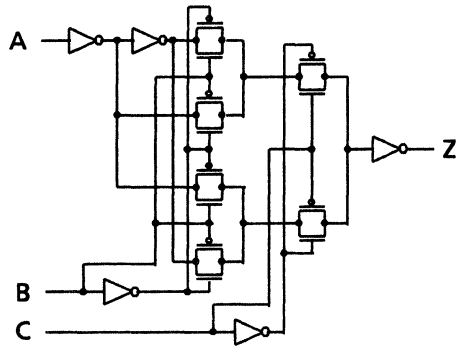
Gate Count: 4
Coding Syntax: Z = ENP (A,B);
Input loading: (1,2)



LOGIC SYMBOL

A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

TRUTH TABLE



ELECTICAL SCHEMATIC

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

EN3 (A-Z) (STANDARD DRIVE)

STD LOAD	1	2	4	8	16
t_{PLH}(Z)	1.8	2.0	2.3	2.9	4.10
t_{PHL}(Z)	1.9	2.0	2.2	2.5	3.10

Z Output Slope 1 = 0.1517 Incpt = 1.68
Slope 0 = 0.0790 Incpt = 1.85

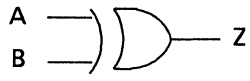
Gate Count: 7
Coding Syntax: Z = EN3 (A,B,C);
Input Loading: (1, 3,2)

EN3P (A-Z) (HIGH DRIVE)

STD LOAD	1	2	4	8	16
t_{PLH}(Z)	1.7	1.8	2.0	2.3	2.9
t_{PHL}(Z)	2.0	2.0	2.2	2.4	2.8

Z Output Slope 1 = 0.0790 Incpt = 1.65
Slope 0 = 0.0546 Incpt = 1.94

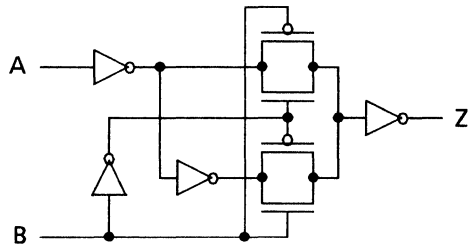
Gate Count: 7
Coding Syntax: Z = EN3P (A,B,C);
Input Loading: (1, 3,2)



LOGIC SYMBOL

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

EO (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.9	1.1	1.2	1.4	2.0	3.1
t_{PHL}	1.1	1.2	1.3	1.3	1.6	2.1

Slope1 = 0.1458 Incpt = 0.79
Slope0 = 0.0653 Incpt = 1.06

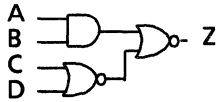
Gate Count: 3
Coding Syntax: Z = EO (A,B);
Input loading: (1,2)

EOP (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.9	1.0	1.1	1.1	1.4	2.0
t_{PHL}	1.1	1.1	1.2	1.2	1.4	1.7

Slope1 = 0.0718 Incpt = 0.84
Slope0 = 0.0411 Incpt = 1.05

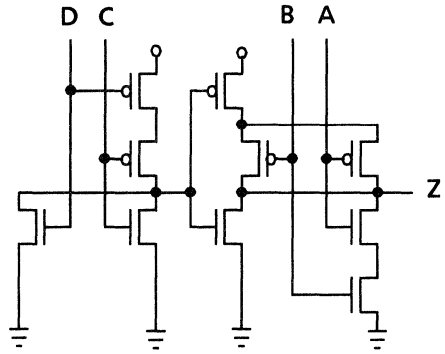
Gate Count: 4
Coding Syntax: Z = EOP (A,B);
Input loading: (1,2)



LOGIC SYMBOL

A	B	C	D	Z
1	1	x	x	0
0	x	1	x	1
0	x	x	1	1
x	0	1	x	1
x	0	x	1	1
x	x	0	0	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

EO1 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8
t_{PLH}	1.1	1.3	1.6	1.9	2.9
t_{PHL}	1.1	1.1	1.2	1.3	1.7

Slope1 = 0.2612 Incpt = 0.82
Slope0 = 0.0839 Incpt = 0.97

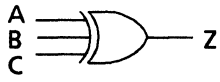
Gate Count : 3
Coding Syntax: Z = EO1 (A,B,C,D);
Input loading: (1,1, 1,1)

EO1P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.1	1.3	1.4	1.5	2.1	3.1
t_{PHL}	0.9	1.0	1.0	1.1	1.2	1.6

Slope1 = 0.1322 Incpt = 1.00
Slope0 = 0.0443 Incpt = 0.88

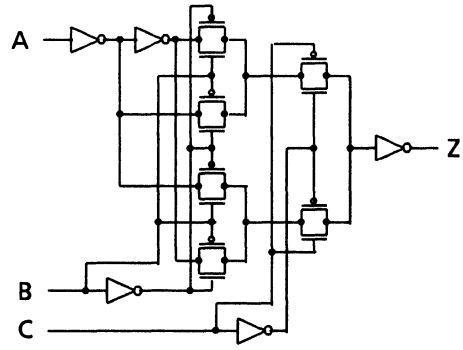
Gate Count: 4
Coding Syntax: Z = EO1P (A,B,C,D);
Input loading: (2,2, 1,1)



LOGIC SYMBOL

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

TRUTH TABLE



ELECTICAL SCHEMATIC

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

EO3 (A TO Z) (STANDARD DRIVE)

STD LOAD	1	2	4	8	16
t_{PLH} (Z)	1.8	2.0	2.3	2.9	4.1
t_{PHL} (Z)	1.9	2.0	2.2	2.5	3.1

Z Output Slope 1 = 0.1517 Incpt = 1.68
Slope 0 = 0.0790 Incpt = 1.85

Gate Count: 7
Coding Syntax: Z = EO3 (A,B,C);
Input Loading: (1,3,2)

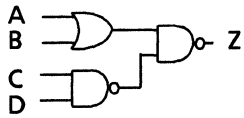
EO3P (A TO Z) (HIGH DRIVE)

STD LOAD	1	2	4	8	16
t_{PLH} (Z)	1.7	1.8	2.0	2.3	2.9
t_{PHL} (Z)	2.0	2.0	2.2	2.4	2.8

Z Output Slope 1 = 0.0790 Incpt = 1.65
Slope 0 = 0.0546 Incpt = 1.94

Gate Count: 7
Coding Syntax: Z = EO3P (A,B,C);
Input Loading: (1,3,2)

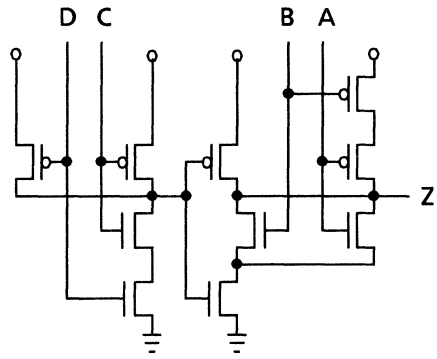
EON1 / EON1P 2OR,2NAND INTO 2NAND EON1 / EON1P



LOGIC SYMBOL

A	B	C	D	Z
x	x	1	1	1
1	x	0	x	0
x	1	0	x	0
1	x	x	0	0
x	1	x	0	0
0	0	x	x	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

EON1 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8
t_{PLH}	1.1	1.3	1.6	1.9	2.9
t_{PHL}	1.0	1.0	1.1	1.2	1.6

Slope1 = 0.2612 Incpt = 0.82
Slope0 = 0.0839 Incpt = 0.87

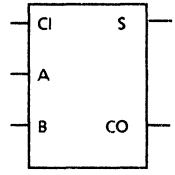
Gate Count: 3
Coding Syntax: Z = EON1 (A,B,C,D);
Input loading: (1,1, 1,1)

EON1P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.1	1.3	1.4	1.5	2.1	3.1
t_{PHL}	0.9	1.0	1.0	1.1	1.2	1.6

Slope1 = 0.1322 Incpt = 1.00
Slope0 = 0.0443 Incpt = 0.88

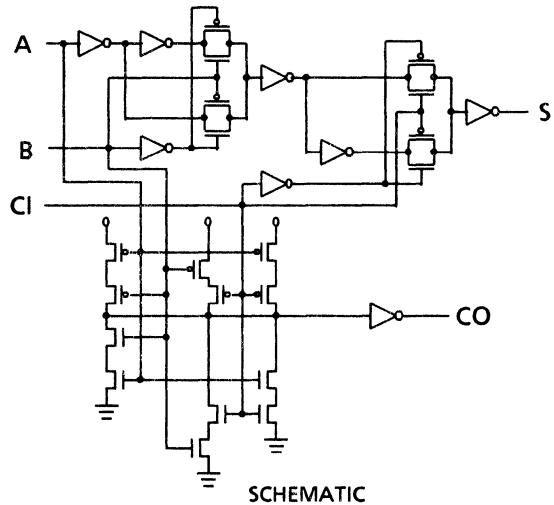
Gate Count: 4
Coding Syntax: Z = EON1P (A,B,C,D);
Input loading: (2,2, 1,1)



LOGIC SYMBOL

CI	A	B	S	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

TRUTH TABLE



SCHEMATIC

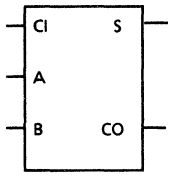
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

FA1 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}(CI-S) t_{PHL}(CI-S)	0.9 0.7	1.1 0.8	1.2 0.8	1.4 0.9	1.9 1.2	3.1 1.7
t_{PLH}(CI-CO) t_{PHL}(CI-CO)	0.9 1.4	1.1 1.5	1.2 1.6	1.4 1.6	2.0 1.9	3.1 2.5
t_{PLH}(A-S) t_{PHL}(A-S)	2.0 2.0	2.2 2.1	2.3 2.1	2.5 2.2	3.0 2.5	4.2 3.0
t_{PLH}(A-CO) t_{PHL}(A-CO)	0.9 1.4	1.1 1.5	1.2 1.6	1.4 1.6	2.0 1.9	3.1 2.5

CI-S Output	Slope 1 = 0.1443	Incpt = 0.78
	Slope 0 = 0.0669	Incpt = 0.64
CI-CO Output	Slope 1 = 0.1458	Incpt = 0.79
	Slope 0 = 0.0718	Incpt = 1.34
A-S Output	Slope 1 = 0.1443	Incpt = 1.88
	Slope 0 = 0.0669	Incpt = 1.94
A-CO Output	Slope 1 = 0.1458	Incpt = 0.79
	Slope 0 = 0.0718	Incpt = 1.34

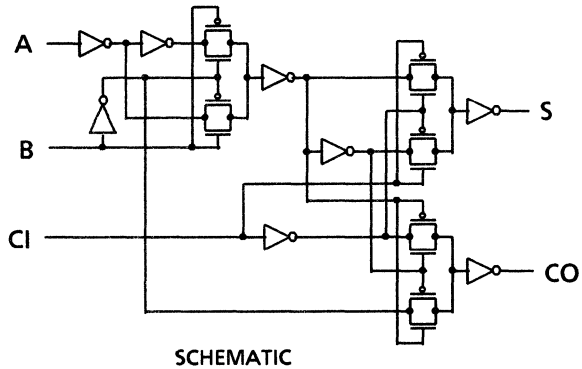
Gate Count: 10
Coding Syntax: Z (S, CO) = FA1 (CI,A,B);
Input Loading: (4, 3, 4)



LOGIC SYMBOL

CI	A	B	S	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

TRUTH TABLE



SCHEMATIC

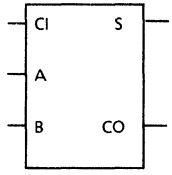
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

FA1A (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH} (CI-S)	1.0	1.2	1.3	1.5	2.1	3.2
t_{PHL} (CI-S)	0.8	0.9	1.0	1.0	1.3	1.8
t_{PLH} (CI-CO)	0.9	1.1	1.2	1.4	2.0	3.1
t_{PHL} (CI-CO)	1.1	1.2	1.2	1.3	1.6	2.1
t_{PLH} (A-S)	2.1	2.3	2.4	2.6	3.2	4.3
t_{PHL} (A-S)	1.9	2.0	2.1	2.1	2.4	2.9
t_{PLH} (A-CO)	2.0	2.2	2.3	2.5	3.1	4.2
t_{PHL} (A-CO)	2.2	2.3	2.3	2.4	2.7	3.2

CI-S Output	Slope 1	= 0.1458	Incpt	=	0.89
	Slope 0	= 0.0653	Incpt	=	0.76
CI-CO Output	Slope 1	= 0.1458	Incpt	=	0.79
	Slope 0	= 0.0669	Incpt	=	1.04
A-S Output	Slope 1	= 0.1458	Incpt	=	1.99
	Slope 0	= 0.0653	Incpt	=	1.86
A-CO Output	Slope 1	= 0.1458	Incpt	=	1.89
	Slope 0	= 0.0669	Incpt	=	2.14

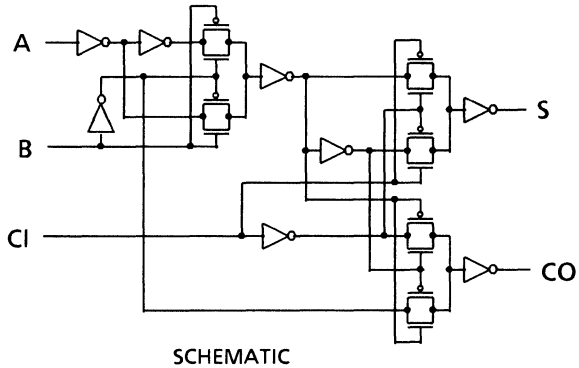
Gate Count: 8
Coding Syntax: Z (S, CO) = FA1A (CI,A,B);
Input Loading: (2, 1, 2)



LOGIC SYMBOL

CI	A	B	S	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

TRUTH TABLE



SCHEMATIC

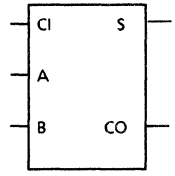
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

FA1AP (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH} (CI-S) t_{PHL} (CI-S)	1.0 0.9	1.1 0.9	1.2 1.0	1.2 1.0	1.5 1.2	2.1 1.5
t_{PLH} (CI-CO) t_{PHL} (CI-CO)	1.0 1.2	1.1 1.2	1.2 1.3	1.2 1.3	1.5 1.5	2.1 1.8
t_{PLH} (A-S) t_{PHL} (A-S)	2.1 2.0	2.2 2.0	2.3 2.1	2.3 2.1	2.6 2.3	3.2 2.6
t_{PLH} (A-CO) t_{PHL} (A-CO)	2.1 2.3	2.2 2.3	2.3 2.4	2.3 2.4	2.6 2.6	3.2 2.9

CI-S Output	Slope 1	= 0.0718	Incpt	=	0.94
	Slope 0	= 0.0411	Incpt	=	0.85
CI-CO Output	Slope 1	= 0.0718	Incpt	=	0.94
	Slope 0	= 0.0411	Incpt	=	1.15
A-S Output	Slope 1	= 0.0718	Incpt	=	2.04
	Slope 0	= 0.0411	Incpt	=	1.95
A-CO Output	Slope 1	= 0.0718	Incpt	=	2.04
	Slope 0	= 0.0411	Incpt	=	2.25

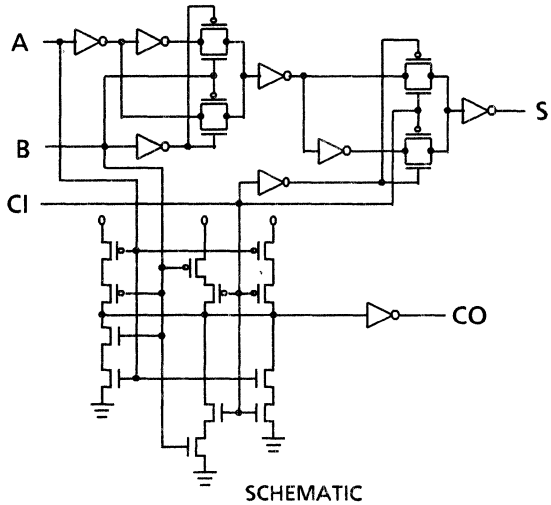
Gate Count: 9
Coding Syntax: Z (S, CO) = FA1AP (CI,A,B);
Input Loading: (2, 1, 2)



LOGIC SYMBOL

CI	A	B	S	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

TRUTH TABLE



SCHEMATIC

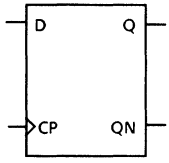
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

FA1P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH} (CI-S) t_{PHL} (CI-S)	0.9 0.7	1.0 0.7	1.1 0.8	1.1 0.8	1.4 1.0	2.0 1.3
t_{PLH} (CI-CO) t_{PHL} (CI-CO)	0.9 1.5	1.0 1.5	1.1 1.6	1.1 1.6	1.4 1.8	2.0 2.2
t_{PLH} (A-S) t_{PHL} (A-S)	2.1 2.0	2.2 2.0	2.3 2.1	2.3 2.1	2.6 2.3	3.2 2.6
t_{PLH} (A-CO) t_{PHL} (A-CO)	0.9 1.5	1.0 1.5	1.1 1.6	1.1 1.6	1.4 1.8	2.0 2.2

CI-S Output	Slope 1 = 0.0718	Incpt = 0.84
	Slope 0 = 0.0411	Incpt = 0.65
CI-CO Output	Slope 1 = 0.0718	Incpt = 0.84
	Slope 0 = 0.0477	Incpt = 1.43
A-S Output	Slope 1 = 0.0718	Incpt = 2.04
	Slope 0 = 0.0411	Incpt = 1.95
A-CO Output	Slope 1 = 0.0718	Incpt = 0.84
	Slope 0 = 0.0477	Incpt = 1.43

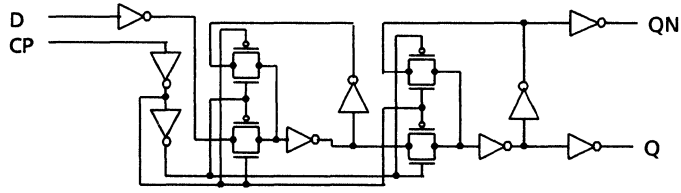
Gate Count: 10
Coding Syntax: Z (S, CO) = FA1P (CI,A,B);
Input Loading: (4, 3, 4)



LOGIC SYMBOL

D	CP	Q	QN
0	↑	0	1
1	↑	1	0

TRUTH TABLE



SCHEMATIC

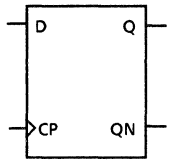
CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH} (Q)	1.2	1.4	1.5	1.7	2.3	3.4
t_{PHL} (Q)	1.4	1.5	1.5	1.6	1.8	2.2
t_{PLH} (QN)	1.7	1.9	2.0	2.2	2.8	3.9
t_{PHL} (QN)	1.6	1.7	1.7	1.8	2.0	2.4

Q Output	Slope 1	=	0.1458	Incpt	=	1.09
	Slope 0	=	0.0523	Incpt	=	1.37
QN Output	Slope 1	=	0.1458	Incpt	=	1.59
	Slope 0	=	0.0523	Incpt	=	1.57

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.8
t_{HOLD} (Input Hold Time)	0.4
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

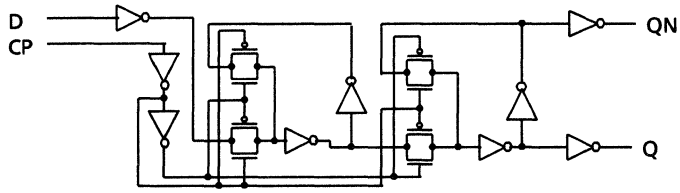
Gate Count : 7
Coding Syntax: Z (Q, QN) = FD1 (D,CP);
Input Loading: (1, 1)



LOGIC SYMBOL

D	CP	Q	QN
0	↑	0	1
1	↑	1	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

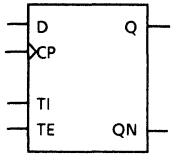
STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.3	1.4	1.4	1.7	2.2
t_{PHL}(Q)	1.5	1.5	1.5	1.6	1.7	2.0
t_{PLH}(QN)	1.9	2.0	2.0	2.1	2.4	2.9
t_{PHL}(QN)	1.8	1.8	1.8	1.9	2.0	2.3

Q Output	Slope 1	=	0.0653	Incpt	=	1.16
	Slope 0	=	0.0347	Incpt	=	1.44
QN Output	Slope 1	=	0.0669	Incpt	=	1.84
	Slope 0	=	0.0347	Incpt	=	1.74

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.8
t_{HOLD} (Input Hold Time)	0.4
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

Gate Count: 8
Coding Syntax: Z (Q, QN) = FD1P (D,CP);
Input Loading: (1, 1)

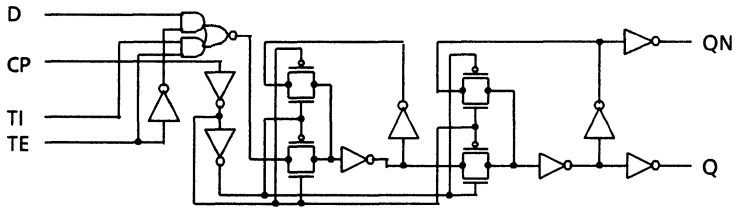
FD1S D FLIP FLOP WITH SCAN / STANDARD DRIVE FD1S



LOGIC SYMBOL

D	TI	TE	CP	Q	QN
0	x	0	↑	0	1
1	x	0	↑	1	0
x	0	1	↑	0	1
x	1	1	↑	1	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

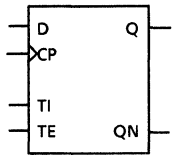
STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.4	1.5	1.7	2.3	3.4
t_{PHL}(Q)	1.4	1.5	1.5	1.6	1.8	2.2
t_{PLH}(QN)	1.7	1.9	2.0	2.2	2.8	3.9
t_{PHL}(QN)	1.6	1.7	1.7	1.8	2.0	2.4

Q Output	Slope 1	=	0.1458	Incpt	=	1.09
	Slope 0	=	0.0523	Incpt	=	1.37
QN Output	Slope 1	=	0.1458	Incpt	=	1.59
	Slope 0	=	0.0523	Incpt	=	1.57

PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.3
t_{HOLD}(Input Hold Time)	0.3
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

Gate Count: 9
Coding Syntax: Z (Q, QN) = FD1S (D,CP,TI,TE);
Input Loading: (1, 1 , 1, 2)

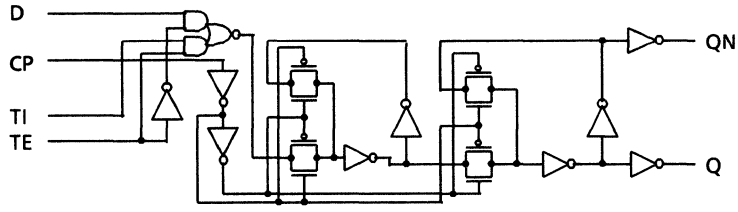
FD1SP D FLIP FLOP WITH SCAN / HIGH DRIVE FD1SP



LOGIC SYMBOL

D	TI	TE	CP	Q	QN
0	x	0	↑	0	1
1	x	0	↑	1	0
x	0	1	↑	0	1
x	1	1	↑	1	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

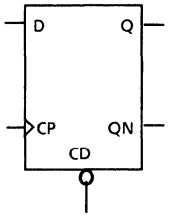
STD LOAD	1	2	3	4	8	16
t_{PLH} (Q)	1.2	1.3	1.4	1.4	1.7	2.2
t_{PHL} (Q)	1.5	1.5	1.5	1.6	1.7	2.0
t_{PLH} (QN)	1.9	2.0	2.0	2.1	2.4	2.9
t_{PHL} (QN)	1.8	1.8	1.8	1.9	2.0	2.3

Q Output	Slope 1	=	0.0653	Incpt	=	1.16
	Slope 0	=	0.0347	Incpt	=	1.44
QN Output	Slope 1	=	0.0669	Incpt	=	1.84
	Slope 0	=	0.0347	Incpt	=	1.74

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.3
t_{HOLD} (Input Hold Time)	0.3
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.6

Gate Count : 10
Coding Syntax: Z (Q, QN) = FD1SP (D,CP,TI,TE);
Input Loading: (1, 1 , 1, 2)

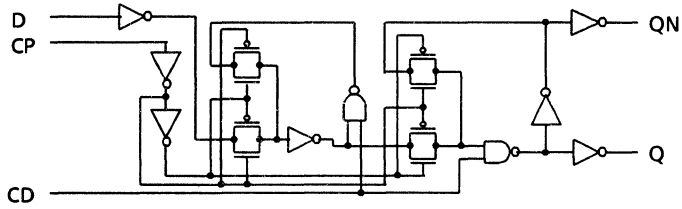
FD2 D FLIP FLOP WITH CLEAR / STANDARD DRIVE FD2



LOGIC SYMBOL

D	CP	CD	Q	QN
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

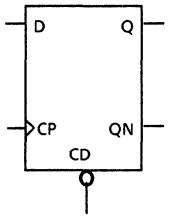
STD LOAD	1	2	3	4	8	16
t_{PLH} (Q)	1.3	1.5	1.6	1.8	2.4	3.5
t_{PHL} (Q)	1.4	1.5	1.5	1.6	1.8	2.2
t_{PLH} (QN)	1.6	1.8	1.9	2.1	2.7	3.9
t_{PHL} (QN)	1.7	1.8	1.8	1.9	2.1	2.5

Q Output	Slope 1	=	0.1458	Incpt	=	1.19
	Slope 0	=	0.0523	Incpt	=	1.37
QN Output	Slope 1	=	0.1523	Incpt	=	1.47
	Slope 0	=	0.0523	Incpt	=	1.67

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.85
t_{HOLD} (Input Hold Time)	0.4
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL} (Q) - 0.6
CD ↓ to QN ↑	t_{PLH} (QN) - 0.6

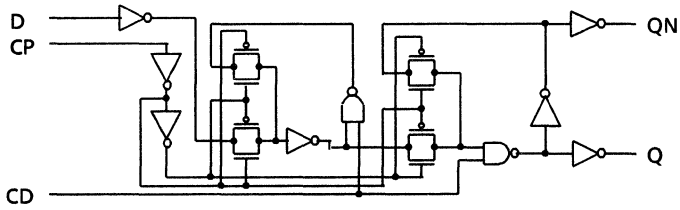
Gate Count : 9
Coding Syntax: Z (Q, QN) = FD2 (D,CP,CD);
Input Loading: (1, 1, 2)



LOGIC SYMBOL

D	CP	CD	Q	QN
0	↑	1	0	1
1	↑	1	1	0
x	x	0	0	1

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.4	1.5	1.6	1.6	1.9	2.5
t_{PHL}(Q)	1.4	1.4	1.4	1.5	1.6	1.9
t_{PLH}(QN)	1.8	1.9	2.0	2.0	2.3	2.8
t_{PHL}(QN)	2.0	2.0	2.0	2.1	2.2	2.4

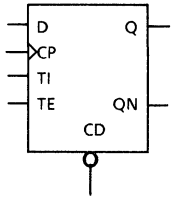
Q Output	Slope 1	=	0.0718	Incpt	=	1.34
	Slope 0	=	0.0347	Incpt	=	1.34
QN Output	Slope 1	=	0.0653	Incpt	=	1.76
	Slope 0	=	0.0282	Incpt	=	1.96

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.85
t_{HOLD} (Input Hold Time)	0.4
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL}(Q) - 0.6
CD ↓ to QN ↑	t_{PLH}(QN) - 0.6

Gate Count : 10
Coding Syntax: Z (Q, QN) = FD2P (D,CP,CD);
Input Loading: (1, 1, 2)

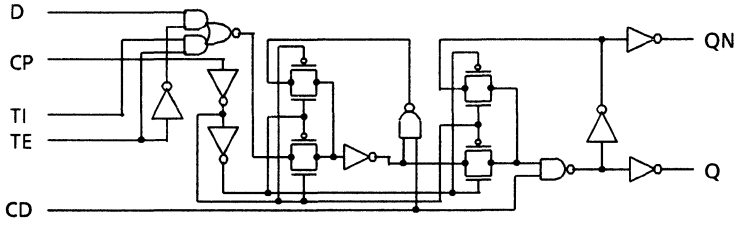
FD2S D FLIP FLOP WITH CLEAR / SCAN / STANDARD DRIVE FD2S



LOGIC SYMBOL

D	TI	TE	CP	CD	Q	QN
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	0	1

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH} (Q) t_{PHL} (Q)	1.3 1.4	1.5 1.5	1.6 1.5	1.8 1.6	2.4 1.8	3.5 2.2
t_{PLH} (QN) t_{PHL} (QN)	1.6 1.7	1.8 1.8	1.9 1.8	2.1 1.9	2.7 2.1	3.9 2.5

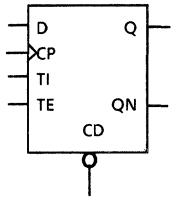
Q Output	Slope 1	= 0.1458	Incpt	=	1.19
	Slope 0	= 0.0523	Incpt	=	1.37
QN Output	Slope 1	= 0.1523	Incpt	=	1.47
	Slope 0	= 0.0523	Incpt	=	1.67

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.25
t_{HOLD} (Input Hold Time)	0.3
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.55
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL} (Q) -0.6
CD ↓ to QN ↑	t_{PLH} (QN) -0.6

Gate Count : 10
Coding Syntax: Z (Q, QN) = FD2S (D,CP,CD,TI,TE);
Input Loading: (1, 1 , 2 , 1, 2)

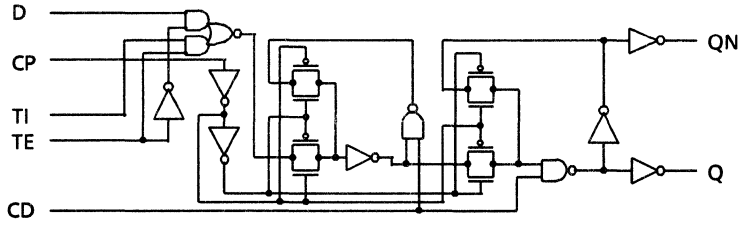
FD2SP D FLIP FLOP WITH CLEAR / SCAN / HIGH DRIVE FD2SP



LOGIC SYMBOL

D	TI	TE	CP	CD	Q	QN
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	0	1

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.4	1.5	1.6	1.6	1.9	2.5
t_{PHL}(Q)	1.4	1.4	1.4	1.5	1.6	1.9
t_{PLH}(QN)	1.8	1.9	2.0	2.0	2.3	2.8
t_{PHL}(QN)	2.0	2.0	2.0	2.1	2.2	2.4

Q Output	Slope 1	=	0.0718	Incpt	=	1.34
	Slope 0	=	0.0347	Incpt	=	1.34
QN Output	Slope 1	=	0.0653	Incpt	=	1.76
	Slope 0	=	0.0282	Incpt	=	1.96

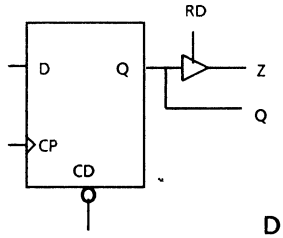
PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.25
t_{HOLD}(Input Hold Time)	0.3
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.55
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL}(Q) -0.6
CD ↓ to QN ↑	t_{PLH}(QN) -0.6

Gate Count: 11
Coding Syntax: Z (Q, QN) = FD2SP (D,CP,CD,TI,TE);
Input Loading: (1, 1 , 2 , 1, 2)

FD2TS D FLIP FLOP WITH CLEAR AND ADDED THREE-STATE OUTPUT FD2TS

STANDARD DRIVE

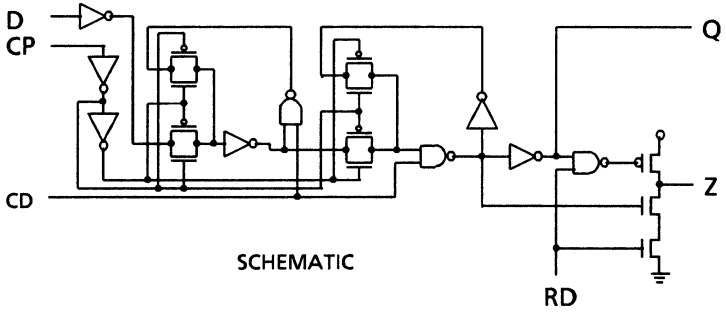


LOGIC SYMBOL

D	CP	CD	Q
0	↑	1	0
1	↑	1	1
x	x	0	0

RD	Q	Z
0	x	Hi-Z
1	0	0
1	1	1

TRUTH TABLE



SCHEMATIC

RD TO Z

CP TO Q

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(CP-Q)	1.6	1.7	1.9	2.0	2.6	3.8
t_{PHL} (CP-Q)	1.5	1.5	1.6	1.6	1.9	2.3
t_{PLH} (RD-Z)	0.3	0.4	0.5	0.6	0.9	1.5
t_{PHL} (RD-Z)	0.6	0.8	0.9	1.1	1.6	2.7

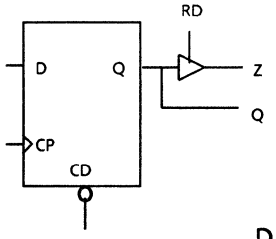
Q Output	Slope 1	=	0.1477	Incpt =	1.43
	Slope 0	=	0.0557	Incpt =	1.42
Z Output	Slope 1	=	0.1377	Incpt =	0.50
	Slope 0	=	0.0788	Incpt =	0.25

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.85
t_{HOLD} (Input Hold Time)	0.4
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL} (Q) -0.6

Gate Count : 9
Coding Syntax: Z (Z, Q) = FD2TS (D,CP,CD,RD);
Input Loading: (1, 1, 2, 1.5)

FD2TSP D FLIP FLOP WITH CLEAR AND ADDED THREE-STATE OUTPUT HIGH DRIVE FD2TSP

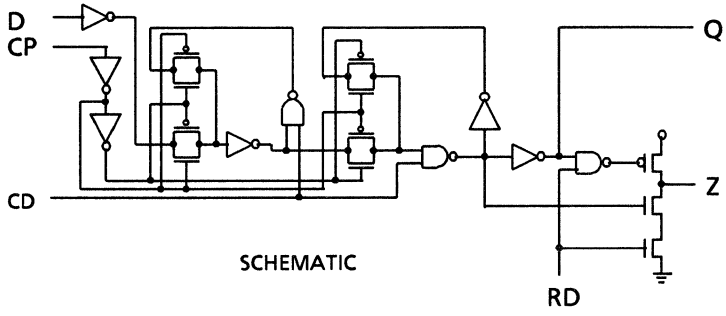


LOGIC SYMBOL

D	CP	CD	Q
0	↑	1	0
1	↑	1	1
x	x	0	0

RD	Q	Z
0	x	Hi-Z
1	0	0
1	1	1

TRUTH TABLE



SCHEMATIC

RD TO Z

CP TO Q

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH} (CP-Q)	1.5	1.6	1.7	1.7	2.0	2.6
t_{PHL} (CP-Q)	1.5	1.5	1.6	1.6	1.8	2.0
t_{PLH} (RD-Z)	0.4	0.4	0.5	0.5	0.7	1.0
t_{PHL} (RD-Z)	0.5	0.5	0.6	0.7	1.0	1.5

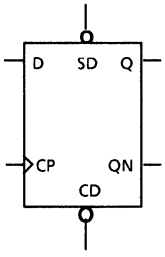
Q Output	Slope 1	=	0.0718	Incpt =	1.44
	Slope 0	=	0.0345	Incpt =	1.47
Z Output	Slope 1	=	0.0693	Incpt =	0.41
	Slope 0	=	0.0411	Incpt =	0.35

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.85
t_{HOLD} (Input Hold Time)	0.4
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL} (Q) -0.6

Gate Count : 11
Coding Syntax: Z (Z, Q) = FD2TSP (D,CP,CD,RD);
Input Loading: (1, 1, 2, 1.5)

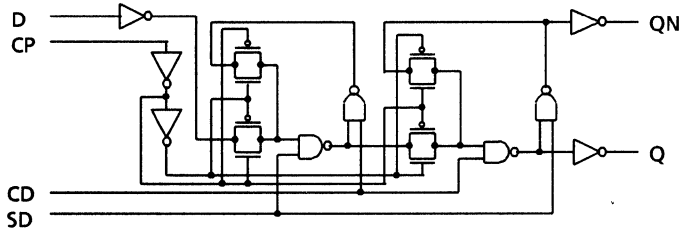
FD3 D FLIP FLOP WITH CLEAR / SET / STANDARD DRIVE FD3



LOGIC SYMBOL

D	CP	CD	SD	Q	QN
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	0	1	0	1
x	x	1	0	1	0
x	x	0	0	0	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH} (Q) t_{PHL} (Q)	1.3 1.4	1.5 1.5	1.6 1.5	1.8 1.6	2.4 1.8	3.6 2.3
t_{PLH} (QN) t_{PHL} (QN)	1.8 1.7	2.0 1.8	2.1 1.8	2.3 1.9	2.9 2.1	4.0 2.5

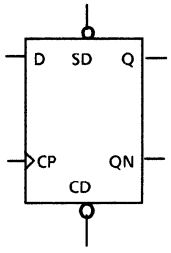
Q Output	Slope 1	=	0.1523	Incpt	=	1.17
	Slope 0	=	0.0589	Incpt	=	1.35
QN Output	Slope 1	=	0.1458	Incpt	=	1.69
	Slope 0	=	0.0523	Incpt	=	1.67

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.9
t_{HOLD} (Input Hold Time)	0.4
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5
Trel SD Release time SD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL} (Q) - 0.6
CD ↓ to QN ↑	t_{PLH} (QN) - 0.6
SD ↓ to Q ↑	t_{PLH} (Q) - 0.2
SD ↓ to QN ↓	t_{PHL} (QN) - 0.9

Gate Count : 9
Coding Syntax: Z (Q, QN) = FD3 (D,CP,CD,SD);
Input Loading: (1, 1, 2 , 2)

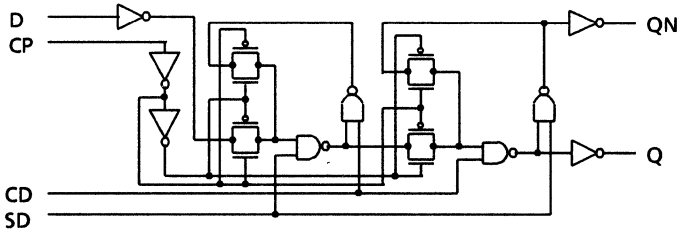
FD3P D FLIP FLOP WITH CLEAR / SET / HIGH DRIVE FD3P



LOGIC SYMBOL

D	CP	CD	SD	Q	QN
0	↑	1	1	0	1
1	↑	1	1	1	0
x	x	0	1	0	1
x	x	1	0	1	0
x	x	0	0	0	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.4	1.5	1.6	1.6	1.9	2.5
t_{PHL}(Q)	1.6	1.6	1.6	1.7	1.8	2.1
t_{PLH}(QN)	2.1	2.2	2.3	2.3	2.6	3.2
t_{PHL}(QN)	2.0	2.0	2.0	2.1	2.2	2.5

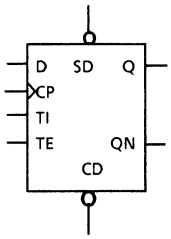
Q Output	Slope 1	=	0.0718	Incpt	=	1.34
	Slope 0	=	0.0347	Incpt	=	1.54
QN Output	Slope 1	=	0.0718	Incpt	=	2.04
	Slope 0	=	0.0347	Incpt	=	1.94

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.9
t_{HOLD} (Input Hold Time)	0.4
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5
Trel SD Release time SD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL} (Q) - 0.6
CD ↓ to QN ↑	t_{PLH} (QN) - 0.6
SD ↓ to Q ↑	t_{PLH} (Q) -0 .15
SD ↓ to QN ↓	t_{PHL} (QN) - 1.05

Gate Count : 10
Coding Syntax: Z (Q, QN) = FD3P (D,CP,CD,SD);
Input Loading: (1, 1, 2 , 2)

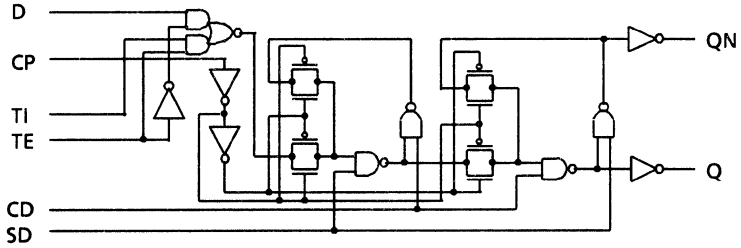
FD3S D FLIP FLOP WITH CLEAR / SET / SCAN / STANDARD DRIVE FD3S



LOGIC SYMBOL

D	TI	TE	CP	CD	SD	Q	QN
0	x	0	↑	1	1	0	1
1	x	0	↑	1	1	1	0
x	0	1	↑	1	1	0	1
x	1	1	↑	1	1	1	0
x	x	x	x	0	1	0	1
x	x	x	x	1	0	1	0
x	x	x	x	0	0	0	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q) t_{PHL}(Q)	1.3 1.4	1.5 1.5	1.6 1.5	1.8 1.6	2.4 1.8	3.6 2.3
t_{PLH}(QN) t_{PHL}(QN)	1.8 1.7	2.0 1.8	2.1 1.8	2.3 1.9	2.9 2.1	4.0 2.5

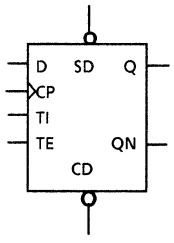
Q Output	Slope 1	=	0.1523	Incpt	=	1.17
	Slope 0	=	0.0589	Incpt	=	1.35
QN Output	Slope 1	=	0.1458	Incpt	=	1.69
	Slope 0	=	0.0523	Incpt	=	1.67

PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.4
t_{HOLD}(Input Hold Time)	0.3
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.7
Trel CD Release time CD to CLK	0.5
Trel SD Release time SD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL}(Q) -0.6
CD ↓ to QN ↑	t_{PLH}(QN) -0.6
SD ↓ to Q ↑	t_{PLH}(Q) -0.2
SD ↓ to QN ↓	t_{PHL}(QN) -0.9

Gate Count: 11
Coding Syntax: Z(Q, QN) = FD3S (D,CP,CD,SD,TI,TE);
Input Loading: (1, 1 , 2 , 2 , 1, 2)

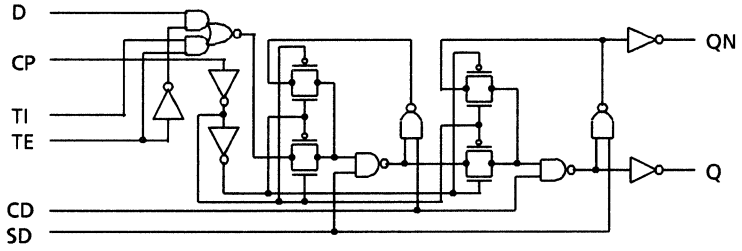
FD3SP D FLIP FLOP WITH CLEAR / SET / SCAN / HIGH DRIVE FD3SP



LOGIC SYMBOL

D	TI	TE	CP	CD	SD	Q	QN
0	x	0	↑	1	1	0	1
1	x	0	↑	1	1	1	0
x	0	1	↑	1	1	0	1
x	1	1	↑	1	1	1	0
x	x	x	x	0	1	0	1
x	x	x	x	1	0	1	0
x	x	x	x	0	0	0	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q) t_{PHL}(Q)	1.4 1.6	1.5 1.6	1.6 1.6	1.6 1.7	1.9 1.8	2.5 2.1
t_{PLH}(QN) t_{PHL}(QN)	2.1 2.0	2.2 2.0	2.3 2.0	2.3 2.1	2.6 2.2	3.2 2.5

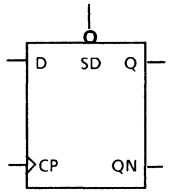
Q Output	Slope 1	=	0.0718	Incpt	=	1.34
	Slope 0	=	0.0347	Incpt	=	1.54
QN Output	Slope 1	=	0.0718	Incpt	=	2.04
	Slope 0	=	0.0347	Incpt	=	1.94

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.4
t_{HOLD} (Input Hold Time)	0.3
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.7
Trel CD Release time CD to CLK	0.5
Trel SD Release time SD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL} (Q) -0.6
CD ↓ to QN ↑	t_{PHL} (QN) -0.6
SD ↓ to Q ↑	t_{PHL} (Q) -0.15
SD ↓ to QN ↓	t_{PHL} (QN) -1.05

Gate Count: 12
Coding Syntax: Z (Q, QN) = FD3SP (D,CP,CD,SD,TI,TE);
Input Loading: (1, 1 , 2 , 2 , 1, 2)

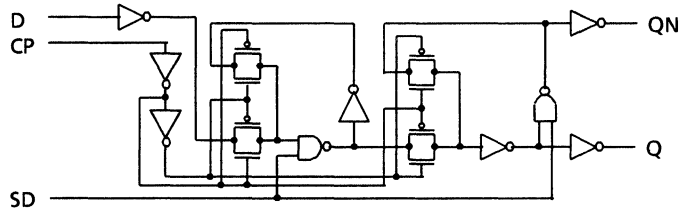
FD4 D FLIP FLOP WITH SET / STANDARD DRIVE FD4



LOGIC SYMBOL

D	CP	SD	Q	QN
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.4	1.5	1.7	2.3	3.4
t_{PHL}(Q)	1.5	1.6	1.6	1.7	1.9	2.4
t_{PLH}(QN)	1.9	2.1	2.2	2.4	3.0	4.1
t_{PHL}(QN)	1.6	1.7	1.7	1.8	2.0	2.4

Q Output	Slope 1	=	0.1458	Incpt	=	1.09
	Slope 0	=	0.0589	Incpt	=	1.45
QN Output	Slope 1	=	0.1458	Incpt	=	1.79
	Slope 0	=	0.0523	Incpt	=	1.57

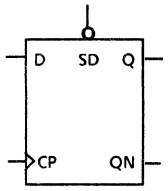
PARAMETER	NS
t_{SETUP}(Input Setup Time)	0.9
t_{HOLD}(Input Hold Time)	0.4
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel SD Release time SD to CLK	0.5

PROPAGATION	DELAY
SD ↓ to Q ↑	t_{PHL}(Q) -0.2
SD ↓ to QN ↓	t_{PLH}(QN) -0.85

↓

Gate Count: 8
Coding Syntax: Z(Q, QN) = FD4 (D,CP,SD);
Input Loading: (1, 1, 2)

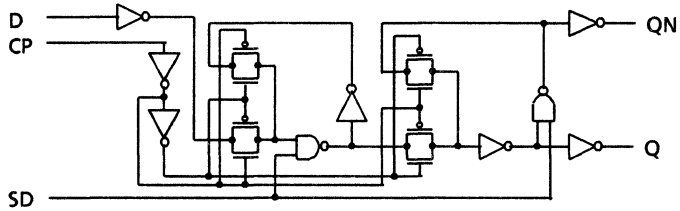
FD4P D FLIP FLOP WITH SET / HIGH DRIVE FD4P



LOGIC SYMBOL

D	CP	SD	Q	QN
0	↑	1	0	1
1	↑	1	1	0
x	x	0	1	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.3	1.4	1.4	1.7	2.2
t_{PHL}(Q)	1.5	1.5	1.5	1.6	1.7	2.0
t_{PLH}(QN)	2.1	2.2	2.3	2.3	2.6	3.2
t_{PHL}(QN)	1.8	1.8	1.8	1.9	2.0	2.3

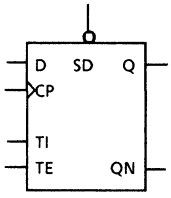
Q Output	Slope 1	=	0.0653	Incpt	=	1.16
	Slope 0	=	0.0347	Incpt	=	1.44
QN Output	Slope 1	=	0.0718	Incpt	=	2.04
	Slope 0	=	0.0347	Incpt	=	1.74

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.9
t_{HOLD} (Input Hold Time)	0.4
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel SD Release time SD to CLK	0.5

PROPAGATION	DELAY
SD ↓ to Q ↑	t_{PHL}(Q) -0.15
SD ↓ to QN ↓	t_{PLH}(QN) -1.00

Gate Count : 9
Coding Syntax: Z (Q, QN) = FD4P (D,CP,SD);
Input Loading: (1, 1, 2)

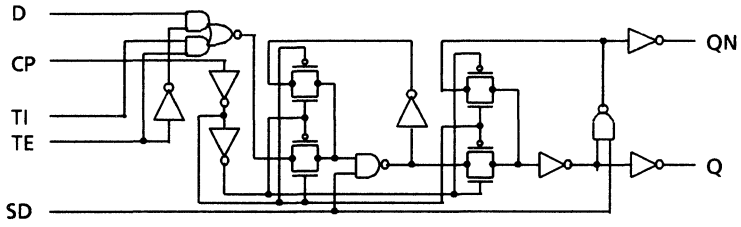
FD4S D FLIP FLOP WITH SET / SCAN / STANDARD DRIVE FD4S



LOGIC SYMBOL

D	TI	TE	CP	SD	Q	QN
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	1	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q) t_{PHL}(Q)	1.2 1.5	1.4 1.6	1.5 1.6	1.7 1.7	2.3 1.9	3.4 2.4
t_{PLH}(QN) t_{PHL}(QN)	1.9 1.6	2.1 1.7	2.2 1.7	2.4 1.8	3.0 2.0	4.1 2.4

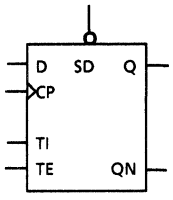
Q Output	Slope 1	=	0.1458	Incpt	=	1.09
	Slope 0	=	0.0589	Incpt	=	1.45
QN Output	Slope 1	=	0.1458	Incpt	=	1.79
	Slope 0	=	0.0523	Incpt	=	1.57

PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.4
t_{HOLD}(Input Hold Time)	0.3
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.7
Trel SD Release time CD to CLK	0.5

PROPAGATION	DELAY
SD ↓ to Q ↑	t_{PLH}(Q) -0.2
SD ↓ to QN ↓	t_{PHL}(QN) -0.85

Gate Count : 10
Coding Syntax: Z (Q, QN) = FD4S (D,CP,SD,TI,TE);
Input Loading: (1, 1 , 2 , 1, 2)

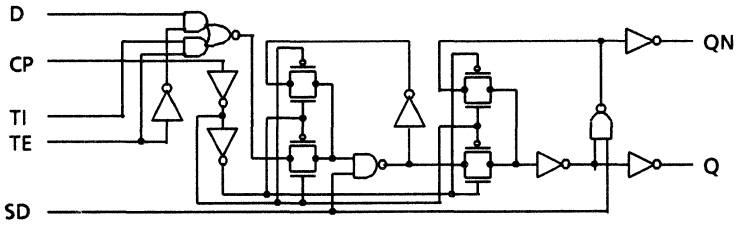
FD4SP — D FLIP FLOP WITH SET / SCAN / HIGH DRIVE — FD4SP



LOGIC SYMBOL

D	TI	TE	CP	SD	Q	QN
0	x	0	↑	1	0	1
1	x	0	↑	1	1	0
x	0	1	↑	1	0	1
x	1	1	↑	1	1	0
x	x	x	x	0	1	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.3	1.4	1.4	1.7	2.2
t_{PHL}(Q)	1.5	1.5	1.5	1.6	1.7	2.0
t_{PLH}(QN)	2.1	2.2	2.3	2.3	2.6	3.2
t_{PHL}(QN)	1.8	1.8	1.8	1.9	2.0	2.3

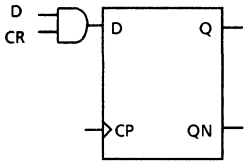
Q Output	Slope 1	=	0.0653	Incpt	=	1.16
	Slope 0	=	0.0347	Incpt	=	1.44
QN Output	Slope 1	=	0.0718	Incpt	=	2.04
	Slope 0	=	0.0347	Incpt	=	1.74

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.4
t_{HOLD} (Input Hold Time)	0.3
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.7
Trel SD Release time CD to CLK	0.5

PROPAGATION	DELAY
SD ↓ to Q ↑	t_{PLH}(Q) -0.15
SD ↓ to QN ↓	t_{PHL} (QN) -1.00

Gate Count : 11
Coding Syntax: Z (Q, QN) = FD4SP (D,CP,SD,TI,TE);
Input Loading: (1, 1 , 2 , 1, 2)

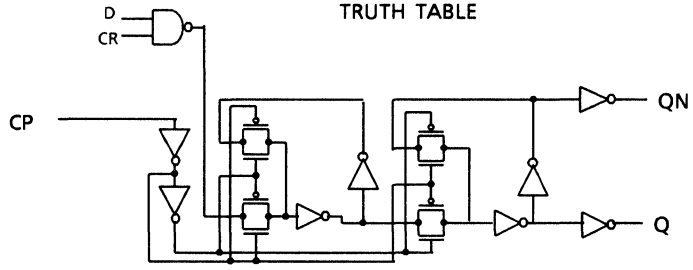
FDS2 D FLIP FLOP WITH SYNCHRONOUS CLEAR / STANDARD DRIVE FDS2



LOGIC SYMBOL

D	CR	CP	Q	QN
X	0	↑	0	1
0	X	↑	0	1
1	1	↑	1	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

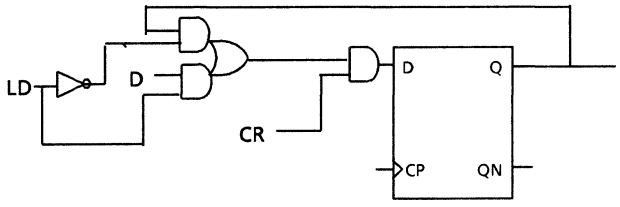
STD LOAD	1	2	3	4	8	16
t_{PLH} (Q) t_{PHL} (Q)	1.2 1.3	1.4 1.4	1.5 1.4	1.7 1.5	2.3 1.7	3.4 2.1
t_{PLH} (QN) t_{PHL} (QN)	1.6 1.6	1.8 1.7	1.9 1.7	2.1 1.8	2.7 2.0	3.8 2.4

Q Output	Slope 1	=	0.1458	Incpt	=	1.09
	Slope 0	=	0.0523	Incpt	=	1.27
QN Output	Slope 1	=	0.1458	Incpt	=	1.49
	Slope 0	=	0.0523	Incpt	=	1.57

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.9
t_{HOLD} (Input Hold Time)	0.4
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

Gate Count : 7
Coding Syntax: Z (Q, QN) = FDS2 (D,CP,CR);
Input Loading: (1, 1, 1)

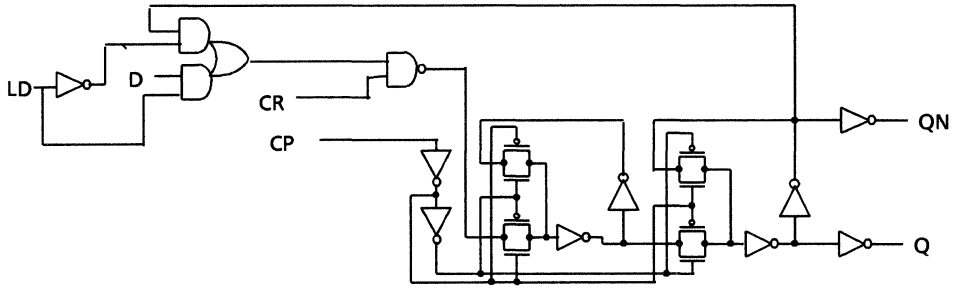
FDS2L D FLIP FLOP WITH SYNCHRONOUS CLEAR AND LOAD / STANDARD DRIVE FDS2L



LOGIC SYMBOL

D	LD	CR	CP	Qn	QNn + 1
0	1	1	↑	0	1
1	1	1	↑	1	0
X	0	1	↑	Q	QN
X	X	0	↑	0	1

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

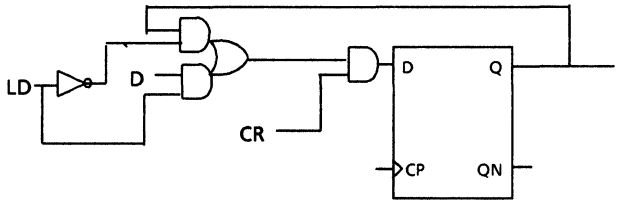
STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.4	1.5	1.7	2.3	3.4
t_{PHL}(Q)	1.3	1.4	1.4	1.5	1.7	2.2
t_{PLH}(QN)	1.6	1.8	1.9	2.1	2.7	3.9
t_{PHL}(QN)	1.6	1.7	1.7	1.8	2.0	2.5

Q Output	Slope 1	=	0.1458	Incpt	=	1.09
	Slope 0	=	0.0589	Incpt	=	1.25
QN Output	Slope 1	=	0.1523	Incpt	=	1.47
	Slope 0	=	0.0589	Incpt	=	1.55

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.6
t_{HOLD} (Input Hold Time)	0.2
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.8

Gate Count : 10
Coding Syntax: Z (Q, QN) = FDS2L (D,CP,CR,LD);
Input Loading: (1, 1, 1 , 1)

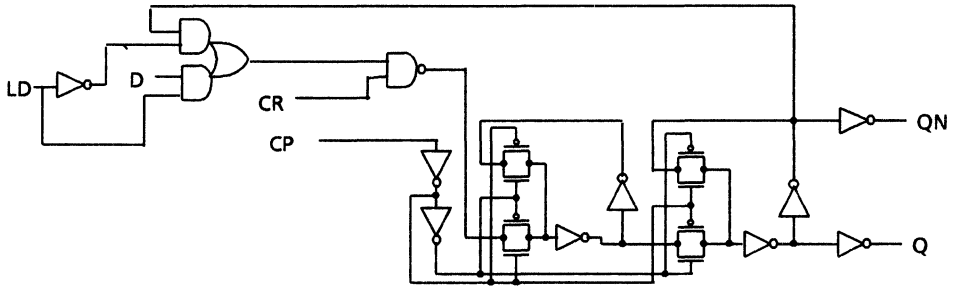
FDS2LP D FLIP FLOP WITH SYNCHRONOUS CLEAR AND LOAD / HIGH DRIVE FDS2LP



LOGIC SYMBOL

D	LD	CR	CP	Qn	QNn + 1
0	1	x	↑	0	1
1	1	1	↑	1	0
X	0	1	↑	Q	QN
X	X	0	↑	0	1

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

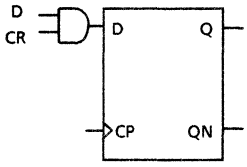
STD LOAD	1	2	3	4	8	16
t_{PLH}(Q) t_{PHL}(Q)	1.3 1.4	1.4 1.4	1.5 1.4	1.5 1.5	1.8 1.6	2.3 1.9
t_{PLH}(QN) t_{PHL}(QN)	1.8 1.8	1.9 1.8	2.0 1.8	2.0 1.9	2.3 2.0	2.9 2.3

Q Output	Slope 1	=	0.0653	Incpt	=	1.26
	Slope 0	=	0.0347	Incpt	=	1.34
QN Output	Slope 1	=	0.0718	Incpt	=	1.74
	Slope 0	=	0.0347	Incpt	=	1.74

PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.6
t_{HOLD}(Input Hold Time)	0.2
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.8

Gate Count: 11
Coding Syntax: Z (Q, QN) = FDS2LP (D,CP,CR,LD);
Input Loading: (1, 1, 1 , 1)

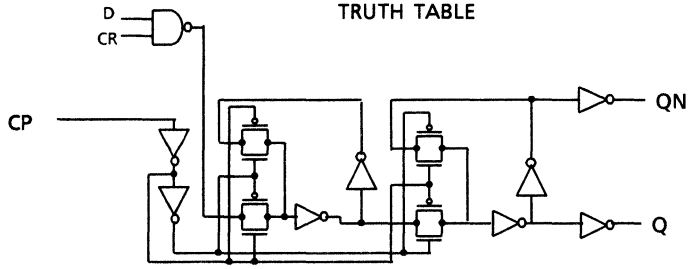
FDS2P D FLIP FLOP WITH SYNCHRONOUS CLEAR / HIGH DRIVE FDS2P



LOGIC SYMBOL

D	CR	CP	Q	QN
X	0	↑	0	1
0	x	↑	0	1
1	1	↑	1	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

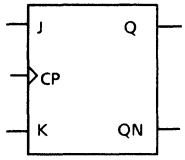
STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.3	1.4	1.4	1.7	2.2
t_{PHL}(Q)	1.5	1.5	1.5	1.6	1.7	2.0
t_{PLH}(QN)	1.9	2.0	2.0	2.1	2.4	2.9
t_{PHL}(QN)	1.8	1.8	1.8	1.9	2.0	2.3

Q Output	Slope 1	=	0.0653	Incpt	=	1.16
	Slope 0	=	0.0347	Incpt	=	1.44
QN Output	Slope 1	=	0.0669	Incpt	=	1.84
	Slope 0	=	0.0347	Incpt	=	1.74

PARAMETER	NS
t_{SETUP}(Input Setup Time)	0.9
t_{HOLD}(Input Hold Time)	0.4
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

Gate Count: 8
Coding Syntax: Z (Q, QN) = FDS2P (D,CP,CR);
Input Loading: (1, 1, 1)

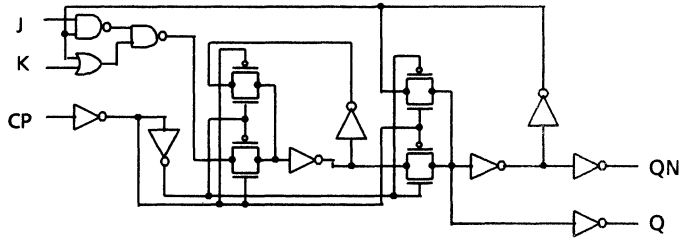
FJK1 JK FLIP FLOP STANDARD DRIVE FJK1



LOGIC SYMBOL

J	K	CP	Q	QN
0	0	↑	Q	QN
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	QN	Q

TRUTH TABLE



SCHEMATIC

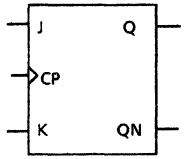
CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.4	1.5	1.7	2.3	3.4
t_{PHL}(Q)	1.0	1.1	1.2	1.2	1.5	2.1
t_{PLH}(QN)	1.5	1.7	1.8	2.0	2.5	3.7
t_{PHL}(QN)	1.5	1.6	1.6	1.7	1.9	2.4

Q Output	Slope 1	=	0.1458	Incpt	=	1.09
	Slope 0	=	0.0718	Incpt	=	0.94
QN Output	Slope 1	=	0.1443	Incpt	=	1.38
	Slope 0	=	0.0589	Incpt	=	1.45

PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.4
t_{HOLD}(Input Hold Time)	0.0
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

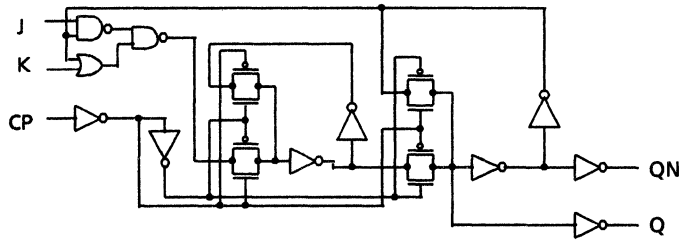
Gate Count : 9
Coding Syntax: Z (Q, QN) = FJK1 (J,K,CP);
Input Loading: (1,1, 1)



LOGIC SYMBOL

J	K	CP	Q	QN
0	0	↑	Q	QN
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	QN	Q

TRUTH TABLE



SCHEMATIC

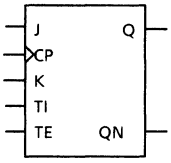
CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.3	1.4	1.4	1.7	2.3
t_{PHL}(Q)	1.1	1.1	1.2	1.2	1.4	1.8
t_{PLH}(QN)	1.6	1.7	1.8	1.8	2.1	2.6
t_{PHL}(QN)	1.6	1.6	1.6	1.7	1.8	2.1

Q Output	Slope 1	=	0.0718	Incpt	=	1.14
	Slope 0	=	0.0477	Incpt	=	1.03
QN Output	Slope 1	=	0.0653	Incpt	=	1.56
	Slope 0	=	0.0347	Incpt	=	1.54

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.4
t_{HOLD} (Input Hold Time)	0.0
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

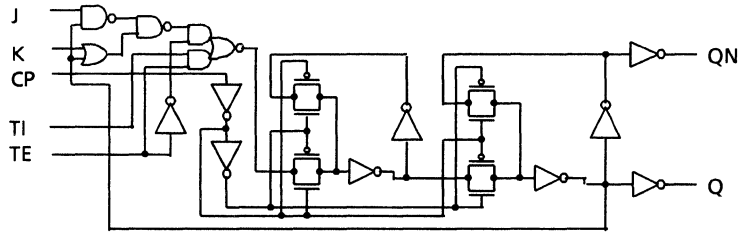
Gate Count: 10
Coding Syntax: Z (Q, QN) = FJK1P (J,K,CP);
Input Loading: (1,1, 1)



LOGIC SYMBOL

J	K	TI	TE	CP	Q	QN
0	0	x	0	↑	Q	QN
0	1	x	0	↑	0	1
1	0	x	0	↑	1	0
1	1	x	0	↑	QN	Q
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0

TRUTH TABLE



SCHEMATIC

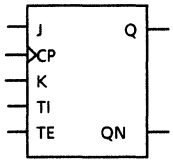
CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.4	1.6	1.7	1.9	2.5	3.6
t_{PHL}(Q)	1.6	1.7	1.7	1.8	2.0	2.5
t_{PLH}(QN)	1.9	2.1	2.2	2.4	2.9	4.1
t_{PHL}(QN)	1.8	1.9	1.9	2.0	2.2	2.6

Q Output	Slope 1	=	0.1458	Incpt	=	1.29
	Slope 0	=	0.0589	Incpt	=	1.55
QN Output	Slope 1	=	0.1443	Incpt	=	1.78
	Slope 0	=	0.0523	Incpt	=	1.77

PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.7
t_{HOLD}(Input Hold Time)	0.0
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

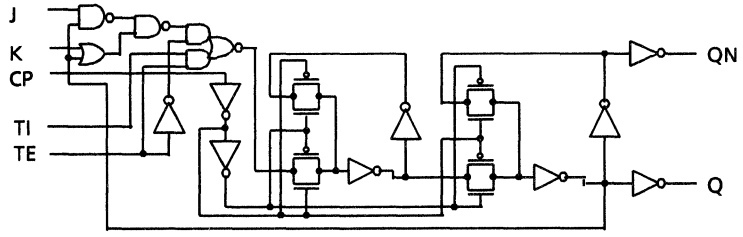
Gate Count : 11
Coding Syntax: Z (Q, QN) = FJK1S (J,K,CP,TI,TE);
Input Loading: (1,1,1 , 1, 2)



LOGIC SYMBOL

J	K	TI	TE	CP	Q	QN
0	0	x	0	↑	Q	QN
0	1	x	0	↑	0	1
1	0	x	0	↑	1	0
1	1	x	0	↑	QN	Q
x	x	0	1	↑	0	1
x	x	1	1	↑	1	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

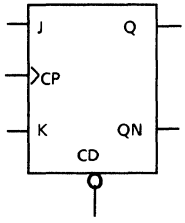
STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.4	1.5	1.6	1.6	1.9	2.5
t_{PHL}(Q)	1.6	1.6	1.7	1.7	1.8	2.1
t_{PLH}(QN)	2.0	2.1	2.2	2.2	2.5	3.0
t_{PHL}(QN)	1.8	1.8	1.8	1.9	2.0	2.3

Q Output	Slope 1	=	0.0718	Incpt	=	1.34
	Slope 0	=	0.0331	Incpt	=	1.56
QN Output	Slope 1	=	0.0653	Incpt	=	1.96
	Slope 0	=	0.0347	Incpt	=	1.74

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.7
t_{HOLD} (Input Hold Time)	0.0
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

Gate Count : 12
Coding Syntax: Z (Q, QN) = FJK1SP (J,K,CP,TI,TE);
Input Loading: (1,1,1 , 1, 2)

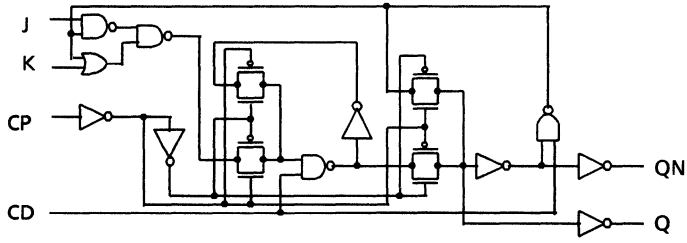
FJK2 JK FLIP FLOP WITH CLEAR / STANDARD DRIVE FJK2



LOGIC SYMBOL

J	K	CP	CD	Q	QN
0	0	↑	1	Q	QN
0	1	↑	1	0	1
1	0	↑	1	1	0
1	1	↑	1	QN	Q
x	x	x	0	0	1

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

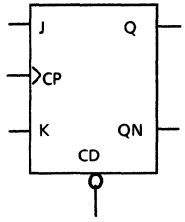
STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.3	1.5	1.6	1.8	2.4	3.6
t_{PHL}(Q)	1.0	1.1	1.2	1.2	1.5	2.1
t_{PLH}(QN)	1.5	1.6	1.8	2.0	2.6	3.9
t_{PHL}(QN)	1.6	1.7	1.7	1.8	2.0	2.5

Q Output	Slope 1	=	0.1523	Incpt	=	1.17
	Slope 0	=	0.0718	Incpt	=	0.94
QN Output	Slope 1	=	0.1612	Incpt	=	1.32
	Slope 0	=	0.0589	Incpt	=	1.55

PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.4
t_{HOLD}(Input Hold Time)	0.0
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL}(Q) -0.25
CD ↓ to QN ↑	t_{PLH}(QN) -0.25

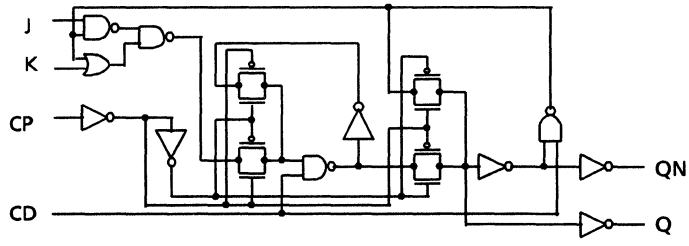
Gate Count : 11
Coding Syntax: Z (Q, QN) = FJK2 (J,K,CP,CD);
Input Loading: (1,1, 1, 2)



LOGIC SYMBOL

J	K	CP	CD	Q	QN
0	0	↑	1	Q	QN
0	1	↑	1	0	1
1	0	↑	1	1	0
1	1	↑	1	QN	Q
x	x	x	0	0	1

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.3	1.4	1.5	1.6	1.9	2.5
t_{PHL}(Q)	1.1	1.1	1.2	1.2	1.4	1.7
t_{PLH}(QN)	1.6	1.7	1.8	1.8	2.1	2.6
t_{PHL}(QN)	1.8	1.8	1.8	1.9	2.0	2.3

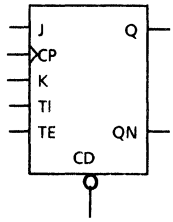
Q Output	Slope 1	=	0.0788	Incpt	=	1.25
	Slope 0	=	0.0411	Incpt	=	1.05
QN Output	Slope 1	=	0.0653	Incpt	=	1.56
	Slope 0	=	0.0347	Incpt	=	1.74

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.4
t_{HOLD} (Input Hold Time)	0.0
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL}(Q) -0.2
CD ↓ to QN ↑	t_{PLH}(QN) -0.2

Gate Count : 12
Coding Syntax: Z (Q, QN) = FJK2P (J,K,CP,CD);
Input Loading: (1,1, 1, 2)

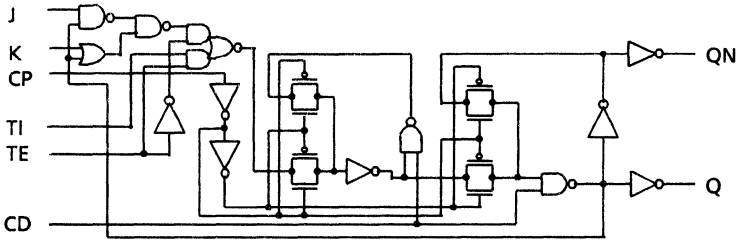
FJK2S JK FLIP FLOP WITH CLEAR / SCAN / STANDARD DRIVE FJK2S



LOGIC SYMBOL

J	K	TI	TE	CP	CD	Q	QN
0	0	x	0	↑	1	Q	QN
0	1	x	0	↑	1	0	1
1	0	x	0	↑	1	1	0
1	1	x	0	↑	1	QN	Q
x	x	0	1	↑	1	0	1
x	x	1	1	↑	1	1	0
x	x	x	x	x	0	0	1

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

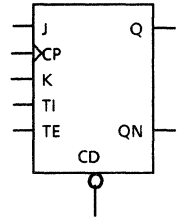
STD LOAD	1	2	3	4	8	16
t_{PLH} (Q)	1.6	1.8	1.9	2.1	2.7	3.9
t_{PHL} (Q)	1.5	1.6	1.6	1.7	1.9	2.4
t_{PLH} (QN)	1.9	2.1	2.2	2.4	2.9	4.1
t_{PHL} (QN)	2.0	2.1	2.1	2.2	2.4	2.8

Q Output	Slope 1	=	0.1523	Incpt	=	1.47
	Slope 0	=	0.0589	Incpt	=	1.45
QN Output	Slope 1	=	0.1443	Incpt	=	1.78
	Slope 0	=	0.0523	Incpt	=	1.97

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.8
t_{HOLD} (Input Hold Time)	0.0
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PLH} (Q) -0.7
CD ↓ to QN ↑	t_{PLH} (QN) -0.7

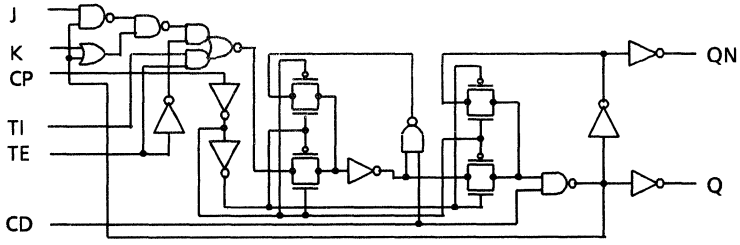
Gate Count : 13
Coding Syntax: Z (Q, QN) = FJK2S (J,K,CP,CD,TI,TE);
Input Loading: (1,1,1 , 2 , 1, 2)



LOGIC SYMBOL

J	K	TI	TE	CP	CD	Q	QN
0	0	x	0	↑	1	Q	QN
0	1	x	0	↑	1	0	1
1	0	x	0	↑	1	1	0
1	1	x	0	↑	1	QN	Q
x	x	0	1	↑	1	0	1
x	x	1	1	↑	1	1	0
x	x	x	x	x	0	0	1

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.6	1.7	1.8	1.9	2.1	2.7
t_{PHL}(Q)	1.6	1.6	1.7	1.7	1.8	2.2
t_{PLH}(QN)	2.0	2.1	2.2	2.2	2.5	3.0
t_{PHL}(QN)	2.1	2.1	2.1	2.2	2.3	2.6

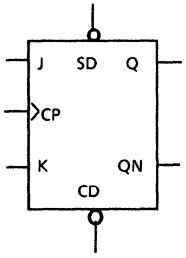
Q Output	Slope 1	=	0.0708	Incpt	=	1.57
	Slope 0	=	0.0396	Incpt	=	1.54
QN Output	Slope 1	=	0.0653	Incpt	=	1.96
	Slope 0	=	0.0347	Incpt	=	2.04

PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.8
t_{HOLD}(Input Hold Time)	0.0
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL}(Q) -0.7
CD ↓ to QN ↑	t_{PLH}(QN) -0.7

Gate Count : 14
Coding Syntax: Z(Q, QN) = FJK2SP (J,K,CP,CD,TI,TE);
Input Loading: (1,1,1 , 2 , 1, 2)

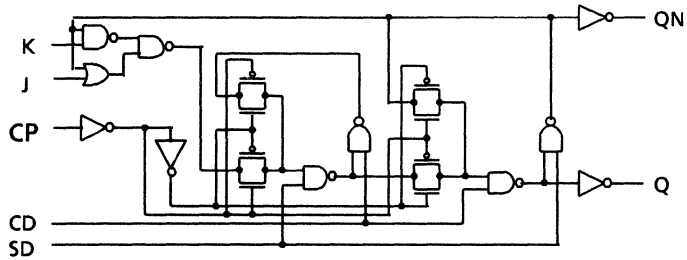
FJK3 JK FLIP FLOP WITH CLEAR / SET / STANDARD DRIVE FJK3



LOGIC SYMBOL

J	K	CP	CD	SD	Q	QN
0	0	↑	1	1	Q	QN
0	1	↑	1	1	0	1
1	0	↑	1	1	1	0
1	1	↑	1	1	QN	Q
x	x	x	0	1	0	1
x	x	x	1	0	1	0
x	x	x	0	0	0	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

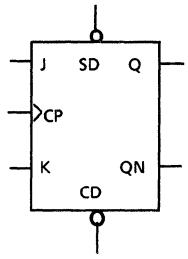
STD LOAD	1	2	3	4	8	16
t_{PLH} (Q) t_{PHL} (Q)	1.4 1.5	1.6 1.6	1.7 1.6	1.9 1.7	2.5 1.9	3.6 2.4
t_{PLH} (QN) t_{PHL} (QN)	2.2 2.0	2.4 2.1	2.5 2.1	2.7 2.2	3.3 2.4	4.4 2.9

Q Output	Slope 1	=	0.1458	Incpt	=	1.29
	Slope 0	=	0.0589	Incpt	=	1.45
QN Output	Slope 1	=	0.1458	Incpt	=	2.09
	Slope 0	=	0.0589	Incpt	=	1.95

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.4
t_{HOLD} (Input Hold Time)	0.0
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5
Trel SD Release time SD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL} (Q) -0.7
CD ↓ to QN ↑	t_{PLH} (QN) -0.7
SD ↓ to Q ↑	t_{PLH} (Q) -0.15
SD ↓ to QN ↓	t_{PHL} (QN) -O.15

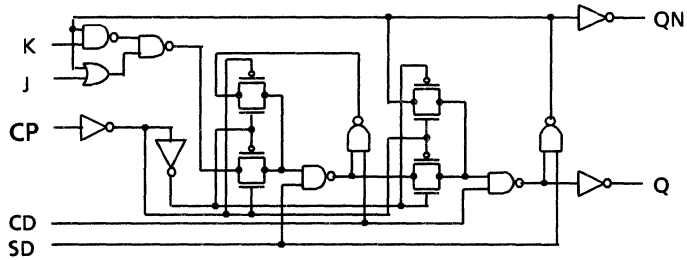
Gate Count : 12
Coding Syntax: Z (Q, QN) = FJK3 (J,K,CP,CD,SD);
Input Loading: (1,1,1, 2, 2)



LOGIC SYMBOL

J	K	CP	CD	SD	Q	QN
0	0	↑	1	1	Q	QN
0	1	↑	1	1	0	1
1	0	↑	1	1	1	0
1	1	↑	1	1	QN	Q
x	x	x	0	1	0	1
x	x	x	1	0	1	0
x	x	x	0	0	0	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH} (Q) t_{PHL} (Q)	1.4 1.5	1.5 1.5	1.6 1.5	1.6 1.6	1.9 1.7	2.5 2.0
t_{PLH} (QN) t_{PHL} (QN)	2.3 2.1	2.4 2.1	2.5 2.2	2.5 2.2	2.8 2.3	3.4 2.6

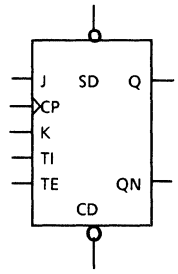
Q Output	Slope 1	=	0.0718	Incpt	=	1.34
	Slope 0	=	0.0347	Incpt	=	1.44
QN Output	Slope 1	=	0.0718	Incpt	=	2.24
	Slope 0	=	0.0331	Incpt	=	2.06

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.4
t_{HOLD} (Input Hold Time)	0.0
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5
Trel SD Release time SD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL} (Q) -0.7
CD ↓ to QN ↑	t_{PLH} (QN) -0.7
SD ↓ to Q ↑	t_{PLH} (Q) -0.1
SD ↓ to QN ↓	t_{PHL} (QN) -1.2

Gate Count: 12
Coding Syntax: Z (Q, QN) = FJK3P (J,K,CP,CD,SD);
Input Loading: (1,1,1 , 2 , 2)

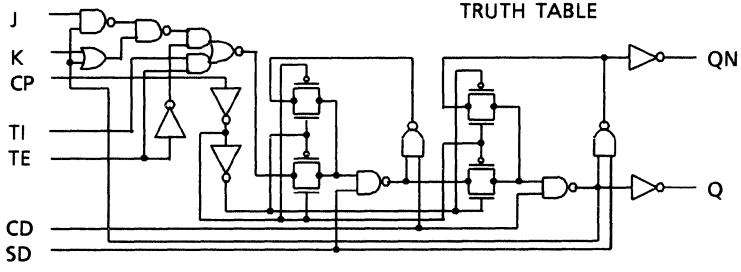
FJK3S JK FLIP FLOP WITH CLEAR / SET / SCAN / STANDARD DRIVE FJK3S



LOGIC SYMBOL

J	K	TI	TE	CP	CD	SD	Q	QN
0	0	x	0	↑	1	1	Q	QN
0	1	x	0	↑	1	1	0	1
1	0	x	0	↑	1	1	1	0
1	1	x	0	↑	1	1	QN	Q
x	x	0	1	↑	1	1	0	1
x	x	1	1	↑	1	1	1	0
x	x	x	x	x	0	1	0	1
x	x	x	x	x	1	0	1	0
x	x	x	x	x	0	0	0	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.7	1.9	2.0	2.2	2.8	4.0
t_{PHL}(Q)	1.7	1.8	1.8	1.9	2.2	2.7
t_{PLH}(QN)	2.3	2.5	2.6	2.8	3.4	4.5
t_{PHL}(QN)	2.0	2.1	2.1	2.2	2.4	2.8

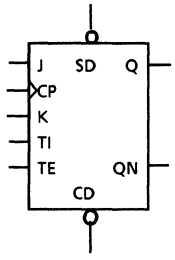
Q Output	Slope 1	=	0.1523	Incpt	=	1.57
	Slope 0	=	0.0669	Incpt	=	1.64
QN Output	Slope 1	=	0.1458	Incpt	=	2.19
	Slope 0	=	0.0523	Incpt	=	1.97

PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.7
t_{HOLD}(Input Hold Time)	0.0
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5
Trel SD Release time SD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL}(Q) -0.7
CD ↓ to QN ↑	t_{PLH}(QN) -0.7
SD ↓ to Q ↑	t_{PLH}(Q) -0.15
SD ↓ to QN ↓	t_{PHL}(QN) -1.15

Gate Count : 14
Coding Syntax: Z (Q, QN) = FJK3S (J,K,CP,CD,SD,TI,TE);
Input Loading: (1,1,1, 2, 2, 1, 2)

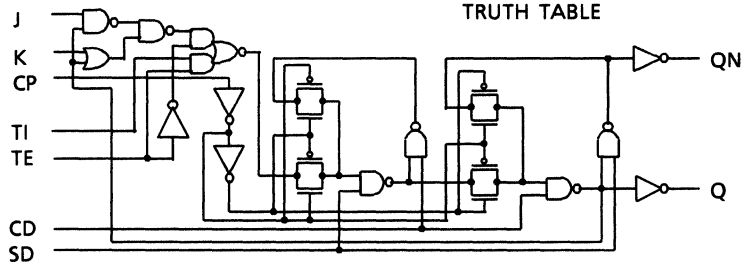
FJK3SP JK FLIP FLOP WITH CLEAR / SET / SCAN / HIGH DRIVE FJK3SP



LOGIC SYMBOL

J	K	TI	TE	CP	CD	SD	Q	QN
0	0	x	0	↑	1	1	Q	QN
0	1	x	0	↑	1	1	0	1
1	0	x	0	↑	1	1	1	0
1	1	x	0	↑	1	1	QN	Q
x	x	0	1	↑	1	1	0	1
x	x	1	1	↑	1	1	1	0
x	x	x	x	x	0	1	0	1
x	x	x	x	x	1	0	1	0
x	x	x	x	x	0	0	0	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH} (Q)	1.7	1.8	1.9	2.0	2.2	2.8
t_{PHL} (Q)	1.7	1.7	1.8	1.8	1.9	2.3
t_{PLH} (QN)	2.5	2.6	2.7	2.7	3.0	3.6
t_{PHL} (QN)	2.2	2.2	2.2	2.3	2.4	2.7

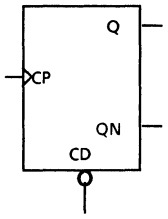
Q Output	Slope 1	=	0.0708	Incpt	=	1.67
	Slope 0	=	0.0396	Incpt	=	1.64
QN Output	Slope 1	=	0.0718	Incpt	=	2.44
	Slope 0	=	0.0347	Incpt	=	2.14

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.7
t_{HOLD} (Input Hold Time)	0.0
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5
Trel SD Release time SD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL} (Q) -0.7
CD ↓ to QN ↑	t_{PLH} (QN) -0.7
SD ↓ to Q ↑	t_{PLH} (Q) -0.05
SD ↓ to QN ↓	t_{PHL} (QN) -1.25

Gate Count : 14
Coding Syntax: Z (Q, QN) = FJK3SP (J,K,CP,CD,SD,TI,TE);
Input Loading: (1,1, 1, 2, 2, 1, 2)

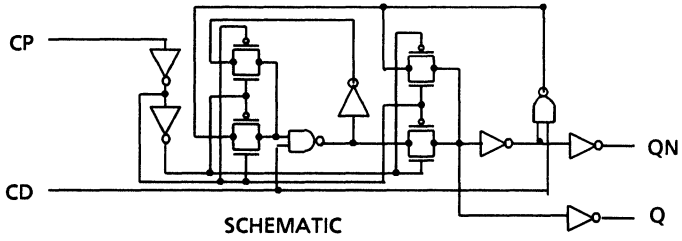
FT2 TOGGLE FLIP FLOP WITH CLEAR / STANDARD DRIVE FT2



LOGIC SYMBOL

CP	CD	Q	QN
↑	1	QN	Q
x	0	0	1

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.4	1.5	1.7	2.3	3.5
t_{PHL}(Q)	1.1	1.2	1.3	1.3	1.6	2.2
t_{PLH}(QN)	1.4	1.6	1.7	1.9	2.5	3.6
t_{PHL}(QN)	1.6	1.7	1.7	1.8	2.0	2.5

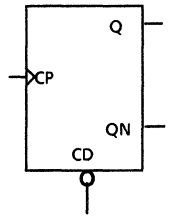
Q Output	Slope 1	=	0.1523	Incpt =	1.07
	Slope 0	=	0.0718	Incpt =	1.04
QN Output	Slope 1	=	0.1458	Incpt =	1.29
	Slope 0	=	0.0589	Incpt =	1.55

PARAMETER	NS
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL}(Q) - 0.15
CD ↓ to QN ↑	t_{PLH}(QN) - 0.15

Gate Count: 8
Coding Syntax: Z (Q, QN) = FT2 (CP,CD);
Input Loading: (1, 2)

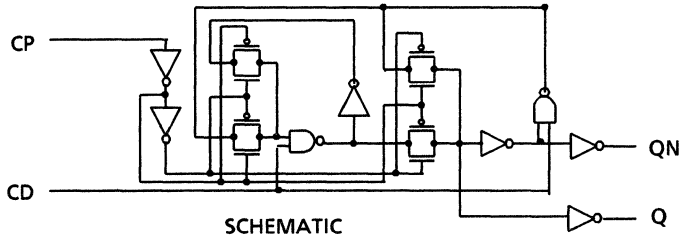
FT2P TOGGLE FLIP FLOP WITH CLEAR / HIGH DRIVE FT2P



LOGIC SYMBOL

CP	CD	Q	QN
↑	1	QN	Q
x	0	0	1

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.3	1.4	1.5	1.8	2.4
t_{PHL}(Q)	1.1	1.1	1.2	1.2	1.4	1.8
t_{PLH}(QN)	1.5	1.6	1.7	1.7	2.0	2.5
t_{PHL}(QN)	1.8	1.8	1.8	1.9	2.0	2.3

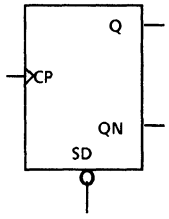
Q Output	Slope 1	=	0.0788	Incpt =	1.15
	Slope 0	=	0.0477	Incpt =	1.03
QN Output	Slope 1	=	0.0653	Incpt =	1.46
	Slope 0	=	0.0347	Incpt =	1.74

PARAMETER	NS
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL}(Q) - 0.15
CD ↓ to QN ↑	t_{PLH}(QN) - 0.15

Gate Count: 9
Coding Syntax: Z (Q, QN) = FT2P (CP,CD);
Input Loading: (1, 2)

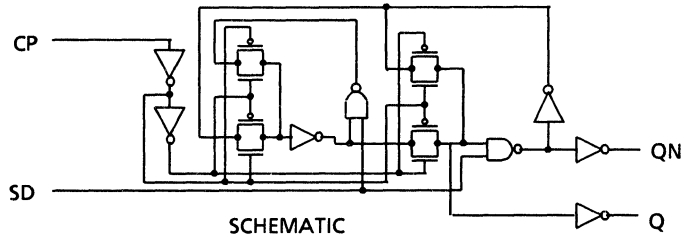
FT4 TOGGLE FLIP FLOP WITH SET / STANDARD DRIVE FT4



LOGIC SYMBOL

CP	SD	Q	QN
↑	1	QN	Q
x	0	1	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.1	1.3	1.4	1.6	2.2	3.3
t_{PHL}(Q)	1.1	1.2	1.3	1.3	1.6	2.2
t_{PLH}(QN)	1.6	1.8	1.9	2.1	2.7	3.8
t_{PHL}(QN)	1.6	1.7	1.7	1.8	2.0	2.5

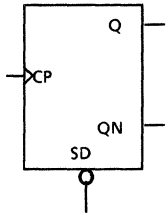
Q Output	Slope 1	=	0.1458	Incpt =	0.99
	Slope 0	=	0.0718	Incpt =	1.04
QN Output	Slope 1	=	0.1458	Incpt =	1.49
	Slope 0	=	0.0589	Incpt =	1.55

PARAMETER	NS
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel SD Release time SD to CLK	0.5

PROPAGATION	DELAY
SD ↓ to Q ↑	t_{PLH}(Q) + 0.15
SD ↓ to QN ↓	t_{PHL} (QN) - 0.6

Gate Count : 8
Coding Syntax: Z (Q, QN) = FT4 (CP,SD);
Input Loading: (1, 2)

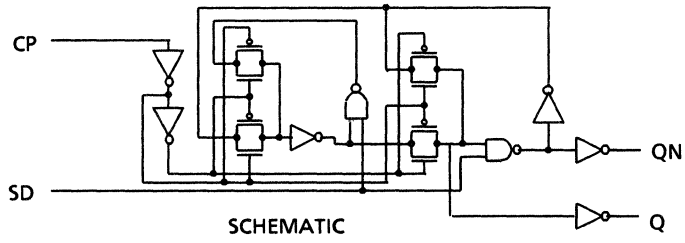
FT4P TOGGLE FLIP FLOP WITH SET / HIGH DRIVE FT4P



LOGIC SYMBOL

CP	SD	Q	QN
↑	1	QN	Q
x	0	1	0

TRUTH TABLE



SCHEMATIC

CP TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.1	1.2	1.3	1.3	1.6	2.2
t_{PHL}(Q)	1.1	1.1	1.2	1.2	1.4	1.8
t_{PLH}(QN)	1.7	1.8	1.9	1.9	2.2	2.8
t_{PHL}(QN)	1.7	1.7	1.7	1.8	1.9	2.2

Q Output	Slope 1	=	0.0718	Incpt =	1.04
	Slope 0	=	0.0477	Incpt =	1.03
QN Output	Slope 1	=	0.0718	Incpt =	1.64
	Slope 0	=	0.0347	Incpt =	1.64

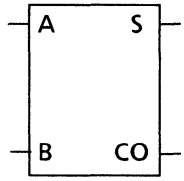
PARAMETER	NS
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel SD Release time SD to CLK	0.5

PROPAGATION	DELAY
SD ↓ to Q ↑	t_{PLH}(Q) + 0.25
SD ↓ to QN ↓	t_{PHL}(QN) + 0.6

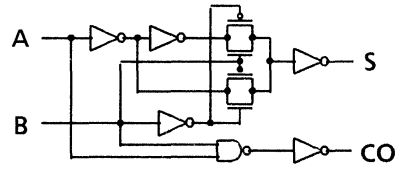
Gate Count: 9
Coding Syntax: Z (Q, QN) = FT4P (CP,SD);
Input Loading: (1, 2)

A	B	S	CO
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

TRUTH TABLE



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

HA1 (A TO S,CO) (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH} (A-S)	1.2	1.4	1.5	1.7	2.2	3.4
t_{PHL} (A-S)	1.0	1.1	1.1	1.2	1.5	2.0
t_{PLH} (A-CO)	0.6	0.8	0.9	1.1	1.6	2.8
t_{PHL} (A-CO)	0.8	0.9	0.9	1.0	1.2	1.6

S Output	Slope 1	=	0.1443	Incpt	=	1.08
	Slope 0	=	0.0669	Incpt	=	0.94
CO Output	Slope 1	=	0.1443	Incpt	=	0.48
	Slope 0	=	0.0523	Incpt	=	0.77

Gate Count: 5
Coding Syntax: X (S,CO) = HA1 (A,B);
Input Loading: (2,3)

HA1P (A TO S,CO) (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
T*plh* (A-S)	1.2	1.3	1.4	1.4	1.7	2.3
T*phl* (A-S)	1.1	1.1	1.2	1.2	1.4	1.7
T*plh* (A-CO)	0.6	0.7	0.8	0.8	1.1	1.7
T*phl* (A-CO)	0.9	0.9	0.9	1.0	1.1	1.4

S Output	Slope 1	=	0.0718	Incpt	=	1.14
	Slope 0	=	0.0411	Incpt	=	1.05
CO Output	Slope 1	=	0.0718	Incpt	=	0.54
	Slope 0	=	0.0347	Incpt	=	0.84

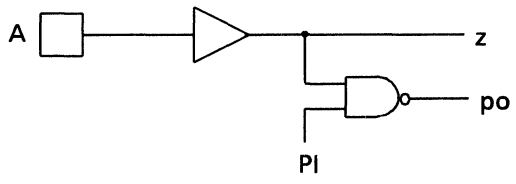
Gate Count: 6
Coding Syntax: X (S,CO) = HA1P (A,B);
Input Loading: (2,3)

CMOS INPUT BUFFER

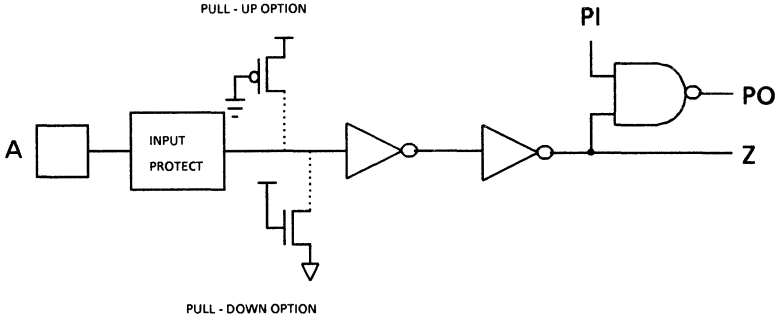
IBUF
CMOS INPUT

IBUFU
CMOS INPUT
WITH PULL-UP

IBUFD
CMOS INPUT
WITH PULL-DOWN



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

IBUF / IBUFU / IBUFD (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Z)	0.7	0.7	0.7	0.8	0.8	1.0
t_{PHL}(Z)	0.8	0.8	0.8	0.8	0.9	1.0

Z Output Slope 1 = 0.0201 Incpt = 0.67
Slope 0 = 0.0146 Incpt = 0.77

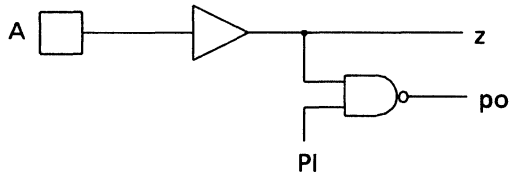
Coding Syntax: (Z,PO) = &IBUF (A, PI);
Coding Syntax: (Z,PO) = &IBUFU (A, PI);
Coding Syntax: (Z,PO) = &IBUFD (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

INVERTED CMOS INPUT BUFFER

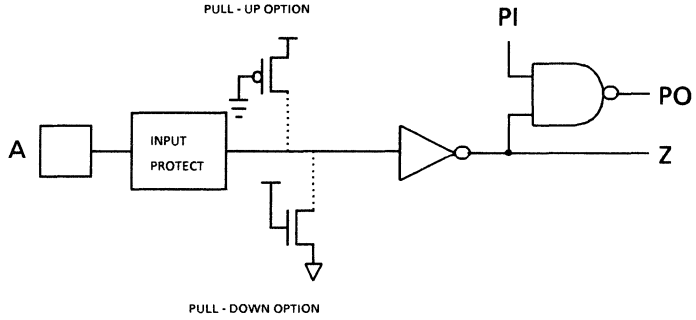
IBUFN
INVERTED CMOS INPUT

IBUFNU
INVERTED CMOS INPUT
WITH PULL-UP

IBUFND
INVERTED CMOS INPUT
WITH PULL-DOWN



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

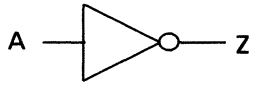
IBUFN / IBUFNU / IBUFND (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

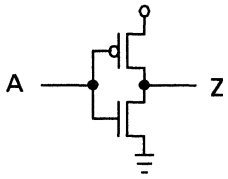
STD LOAD	1	2	3	4	8	16
t_{PLH}(Z)	0.5	0.6	0.6	0.6	0.7	0.8
t_{PHL}(Z)	0.4	0.4	0.5	0.5	0.6	0.7

Z Output Slope 1 = 0.0176 Incpt = 0.53
Slope 0 = 0.0199 Incpt = 0.40

Coding Syntax: (Z,PO) = &IBUFN (A, PI);
Coding Syntax: (Z,PO) = &IBUFNU (A, PI);
Coding Syntax: (Z,PO) = &IBUFND (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

A	Z
0	1
1	0

TRUTH TABLE

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

IV (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.5	0.7	0.8	1.0	1.5	2.7
t_{PHL}	0.2	0.3	0.3	0.4	0.6	1.1

Slope1 = 0.1443 Incpt = 0.38
Slope0 = 0.0589 Incpt = 0.15

Gate Count: 1
Coding Syntax: Z = IV (A);
Input loading: (1)

IVP (HIGH DRIVE)

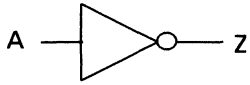
STD LOAD	1	2	3	4	8	16
t_{PLH}	0.4	0.5	0.6	0.6	0.9	1.4
t_{PHL}	0.2	0.2	0.3	0.3	0.4	0.7

Slope1 = 0.0653 Incpt = 0.36
Slope0 = 0.0331 Incpt = 0.16

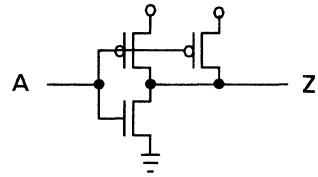
Gate Count : 1
Coding Syntax: Z = IVP (A);
Input loading: (2)

INVERTER WITH PARALLEL P TRANSISTORS

IVA / IVAP



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

A	Z
0	1
1	0

TRUTH TABLE

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

IVA (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.3	0.4	0.5	0.5	0.8	1.4
t_{PHL}	0.3	0.4	0.4	0.5	0.7	1.2

Slope1 = 0.0718 Incpt = 0.24
Slope0 = 0.0589 Incpt = 0.25

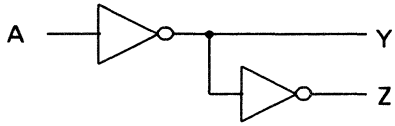
Gate Count: 1
Coding Syntax: Z = IVA (A);
Input loading: (1.5)

IVAP (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.3	0.3	0.4	0.4	0.5	0.8
t_{PHL}	0.2	0.2	0.2	0.3	0.4	0.7

Slope1 = 0.0331 Incpt = 0.26
Slope0 = 0.0347 Incpt = 0.14

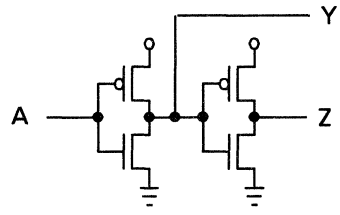
Gate Count: 2
Coding Syntax: Z = IVAP (A);
Input loading: (3)



LOGIC SYMBOL

A	Y	Z
1	0	1
0	1	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

IVDA (A TO Y / Z) (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH} (Y)	0.7	0.8	1.0	1.1	1.7	2.8
t_{PHL} (Y)	0.4	0.4	0.5	0.5	0.8	1.2
t_{PLH} (Z)	0.6	0.8	0.9	1.1	1.6	2.8
t_{PHL} (Z)	0.7	0.8	0.8	0.9	1.1	1.5

Y Output	Slope 1	=	0.1411	Incpt	=	0.55
	Slope 0	=	0.0557	Incpt	=	0.32
Z Output	Slope 1	=	0.1443	Incpt	=	0.48
	Slope 0	=	0.0523	Incpt	=	0.67

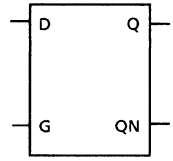
Gate Count: 1
Coding Syntax: X (Y,Z) = IVDA (A);
Input Loading: (1)

IVDAP (A TO Y / Z) (HIGH DRIVE)

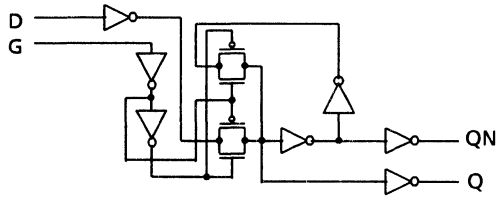
STD LOAD	1	2	3	4	8	16
t_{PLH} (Y)	0.5	0.5	0.6	0.7	0.9	1.5
t_{PHL} (Y)	0.2	0.3	0.3	0.3	0.5	0.8
t_{PLH} (Z)	0.4	0.5	0.6	0.6	0.9	1.4
t_{PHL} (Z)	0.6	0.6	0.6	0.6	0.8	1.0

Y Output	Slope 1	=	0.0678	Incpt	=	0.40
	Slope 0	=	0.0388	Incpt	=	0.18
Z Output	Slope 1	=	0.0653	Incpt	=	0.36
	Slope 0	=	0.0292	Incpt	=	0.53

Gate Count: 2
Coding Syntax: X (Y,Z) = IVDAP (A);
Input Loading: (2)



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

D	G	Q	QN
0	1	0	1
1	1	1	0
x	0	Q	QN

TRUTH TABLE

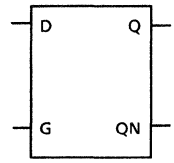
G TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.0	1.2	1.3	1.5	2.1	3.2
t_{PHL}(Q)	0.9	1.0	1.1	1.1	1.4	1.9
t_{PLH}(QN)	1.3	1.5	1.6	1.8	2.3	3.5
t_{PHL}(QN)	1.4	1.5	1.5	1.6	1.8	2.2

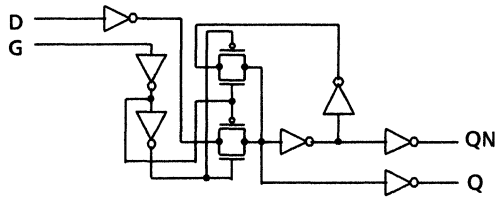
Q Output	Slope 1	=	0.1458	Incpt	=	0.89
	Slope 0	=	0.0653	Incpt	=	0.86
QN Output	Slope 1	=	0.1443	Incpt	=	1.18
	Slope 0	=	0.0523	Incpt	=	1.37

PARAMETER	NS
t_{SETUP}(Input Setup Time)	0.4
t_{HOLD}(Input Hold Time)	0.4
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

Gate Count: 5
Coding Syntax: Z (Q, QN) = LD1 (D,G);
Input Loading: (1, 1)



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

D	G	Q	QN
0	1	0	1
1	1	1	0
x	0	Q	QN

TRUTH TABLE

G TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
(Q)	1.0	1.1	1.2	1.2	1.5	2.1
(Q)	1.0	1.0	1.1	1.1	1.3	1.6
(QN)	1.5	1.6	1.7	1.7	2.0	2.5
(QN)	1.6	1.6	1.6	1.7	1.8	2.1

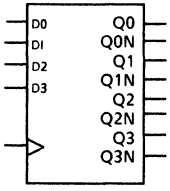
Q Output	Slope 1	= 0.0718	Incpt	=	0.94
	Slope 0	= 0.0411	Incpt	=	0.95
QN Output	Slope 1	= 0.0653	Incpt	=	1.46
	Slope 0	= 0.0347	Incpt	=	1.54

PARAMETER	NS
Tsetup (Input Setup Time)	0.6
Thold (Input Hold Time)	0.4
Tw (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

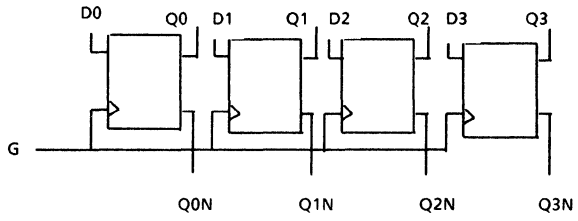
Gate Count: 6
Coding Syntax: Z (Q, QN) = LD1P (D,G);
Input Loading: (1, 1)

4 LD1 IN PARALLEL WITH COMMON GATES

LD1X4



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

G	D0	Q0	Q0N
↑	0	0	1
↑	1	1	0
0	x	Q0	Q0N

TRUTH TABLE

G TO (Q0, Q0N) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q0)	1.1	1.3	1.4	1.6	2.2	3.3
t_{PHL}(Q0)	1.0	1.1	1.2	1.2	1.5	2.0
t_{PLH}(Q0N)	1.4	1.6	1.7	1.9	2.4	3.6
t_{PHL}(Q0N)	1.5	1.6	1.6	1.7	1.9	2.4

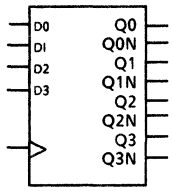
Q Output	Slope 1	=	0.1458	Incpt	=	0.99
	Slope 0	=	0.0653	Incpt	=	0.96
QN Output	Slope 1	=	0.1443	Incpt	=	1.28
	Slope 0	=	0.0589	Incpt	=	1.45

PARAMETER	NS
t_{SETUP}(Input Setup Time)	0.40
t_{HOLD}(Input Hold Time)	0.40
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	0.80
CLOCK Low Min	0.80

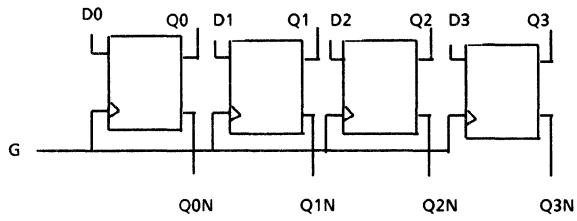
Gate Count : 16
Coding Syntax: Z (Q0,Q0N,Q1,Q1N,Q2,Q2N,Q3,Q3N) = LD1X4 (D0,D1,D2,D3,G);
Input Loading: (1 , 1 , 1 , 1 , 2)

4 LD1P IN PARALLEL WITH COMMON GATES

LD1X4P



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

G	D0	Q0	Q0N
↑	0	0	1
↑	1	1	0
0	x	Q0	Q0N

TRUTH TABLE

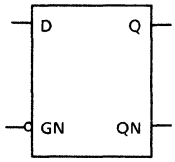
G TO (Q0, Q0N) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q0)	1.1	1.2	1.3	1.3	1.6	2.2
t_{PHL}(Q0)	1.0	1.0	1.1	1.1	1.3	1.6
t_{PLH}(Q0N)	1.5	1.6	1.7	1.7	2.0	2.5
t_{PHL}(Q0N)	1.6	1.6	1.6	1.7	1.8	2.1

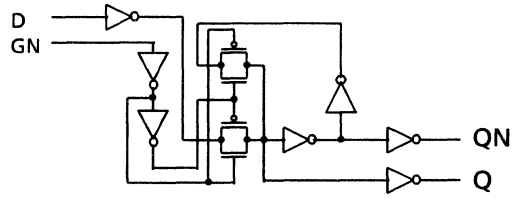
Q Output	Slope 1	=	0.0718	Incpt	=	1.04
	Slope 0	=	0.0411	Incpt	=	0.95
QN Output	Slope 1	=	0.0653	Incpt	=	1.46
	Slope 0	=	0.0347	Incpt	=	1.54

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.50
t_{HOLD} (Input Hold Time)	0.40
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	0.90
CLOCK Low Min	0.90

Gate Count: 20
Coding Syntax: Z (Q0,Q0N,Q1,Q1N,Q2,Q2N,Q3,Q3N) = LD1X4P (D0,D1,D2,D3,G);
Input Loading: (1 , 1 , 1 , 1 , 2)



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

D	GN	Q	QN
0	0	0	1
1	0	1	0
x	1	Q	QN

TRUTH TABLE

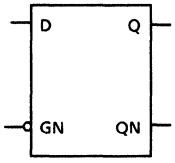
GN TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.4	1.5	1.7	2.3	3.4
t_{PHL}(Q)	1.3	1.4	1.5	1.5	1.8	2.4
t_{PLH}(QN)	1.7	1.9	2.0	2.2	2.7	3.9
t_{PHL}(QN)	1.6	1.7	1.7	1.8	2.0	2.4

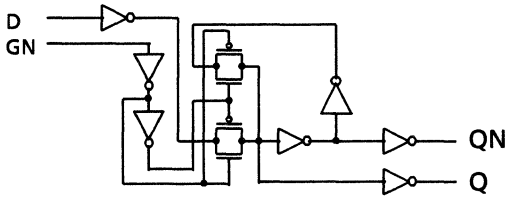
Q Output	Slope 1	=	0.1458	Incpt	=	1.09
	Slope 0	=	0.0718	Incpt	=	1.24
QN Output	Slope 1	=	0.1443	Incpt	=	1.58
	Slope 0	=	0.0523	Incpt	=	1.57

PARAMETER	NS
t_{SETUP}(Input Setup Time)	0.4
t_{HOLD}(Input Hold Time)	0.4
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

Gate Count : 5
Coding Syntax: Z (Q, QN) = LD2 (D,GN);
Input Loading: (1, 1)



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

D	GN	Q	QN
0	0	0	1
1	0	1	0
x	1	Q	QN

TRUTH TABLE

GN TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH} (Q)	1.2	1.3	1.4	1.4	1.7	2.3
t_{PHL}(Q)	1.3	1.3	1.4	1.4	1.6	2.0
t_{PLH} (QN)	1.8	1.9	2.0	2.0	2.3	2.8
t_{PHL} (QN)	1.8	1.8	1.8	1.9	2.0	2.3

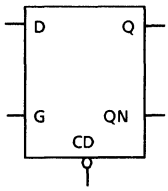
Q Output	Slope 1	=	0.0718	Incpt	=	1.14
	Slope 0	=	0.0477	Incpt	=	1.23
QN Output	Slope 1	=	0.0653	Incpt	=	1.76
	Slope 0	=	0.0347	Incpt	=	1.74

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.6
t_{HOLD} (Input Hold Time)	0.4
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

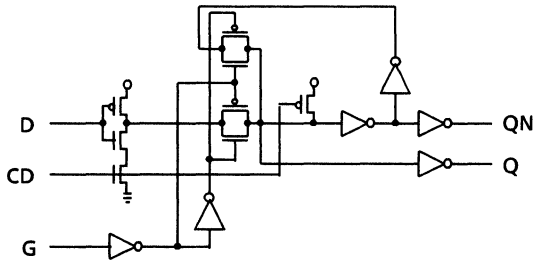
Gate Count: 6
Coding Syntax: Z (Q, QN) = LD2P (D,GN);
Input Loading: (1, 1)

LD3 DLATCH, GATED CLEAR DIRECT / GATE ACTIVE HIGH LD3

STANDARD DRIVE



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

D	G	CD	Q	QN
0	1	1	0	1
1	1	1	1	0
x	0	1	Q	QN
x	x	0	0	1

TRUTH TABLE

G TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH} (Q)	1.2	1.4	1.5	1.7	2.3	3.5
t_{PHL} (Q)	1.0	1.1	1.2	1.2	1.5	2.1
t_{PLH} (QN)	1.3	1.5	1.6	1.8	2.3	3.5
t_{PHL} (QN)	1.5	1.6	1.6	1.7	1.9	2.3

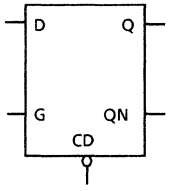
Q Output	Slope 1	=	0.1523	Incpt	=	1.07
	Slope 0	=	0.0718	Incpt	=	0.94
QN Output	Slope 1	=	0.1443	Incpt	=	1.18
	Slope 0	=	0.0523	Incpt	=	1.47

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.5
t_{HOLD} (Input Hold Time)	0.4
t (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

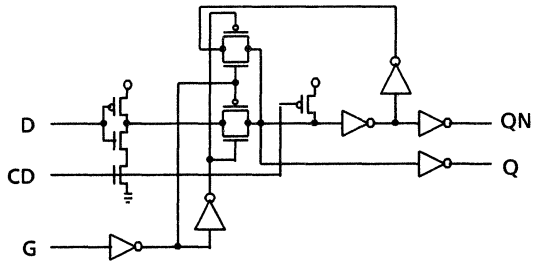
PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL} (Q) + 0.4
CD ↓ to QN ↑	t_{PHL} (QN) + 0.4

Gate Count: 5
Coding Syntax: Z (Q, QN) = LD3 (D,G,CD);
Input Loading: (1, 1, 1)

LD3P DLATCH, GATED CLEAR DIRECT / GATE ACTIVE HIGH HIGH DRIVE LD3P



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

D	G	CD	Q	QN
0	1	1	0	1
1	1	1	1	0
x	0	1	Q	QN
x	x	0	0	1

TRUTH TABLE

G TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.2	1.3	1.4	1.5	1.8	2.4
t_{PHL}(Q)	1.0	1.0	1.1	1.1	1.3	1.7
t_{PLH}(QN)	1.5	1.6	1.7	1.7	2.0	2.5
t_{PHL}(QN)	1.7	1.7	1.7	1.8	1.9	2.2

Q Output	Slope 1	=	0.0788	Incpt	=	1.15
	Slope 0	=	0.0477	Incpt	=	1.93
QN Output	Slope 1	=	0.0653	Incpt	=	1.46
	Slope 0	=	0.0347	Incpt	=	1.64

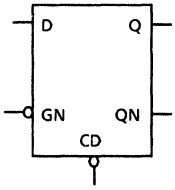
PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.7
t_{HOLD} (Input Hold Time)	0.4
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL}(Q) + 0.4
CD ↓ to QN ↑	t_{PHL}(QN) + 0.4

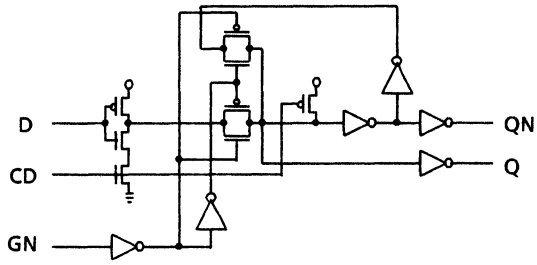
Gate Count: 6
Coding Syntax: Z (Q, QN) = LD3P (D,G,CD);
Input Loading: (1, 1, 1)

LD4 DLATCH, GATED, CLEAR DIRECT, GATE ACTIVE LOW LD4

STANDARD DRIVE



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

D	GN	CD	Q	QN
0	0	1	0	1
1	0	1	1	0
x	1	1	Q	QN
x	x	0	0	1

TRUTH TABLE

GN TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.4	1.6	1.7	1.9	2.5	3.7
t_{PHL}(Q)	1.3	1.4	1.5	1.5	1.8	2.4
t_{PLH}(QN)	1.6	1.8	1.9	2.1	2.6	3.8
t_{PHL}(QN)	1.7	1.8	1.8	1.9	2.1	2.6

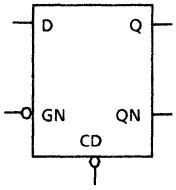
Q Output	Slope 1	=	0.1523	Incpt	=	1.27
	Slope 0	=	0.0718	Incpt	=	1.24
QN Output	Slope 1	=	0.1443	Incpt	=	1.48
	Slope 0	=	0.0589	Incpt	=	1.65

PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.5
t_{HOLD} (Input Hold Time)	0.4
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

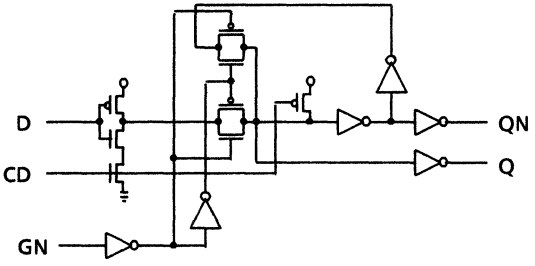
PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL}(Q) + 0.4
CD ↓ to QN ↑	t_{PHL}(QN) + 0.4

Gate Count: 5
Coding Syntax: Z (Q, QN) = LD4 (D,GN,CD);
Input Loading: (1, 1, 1)

LD4P DLATCH, GATED CLEAR DIRECT / GATE ACTIVE LOW HIGH DRIVE LD4P



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

D	GN	CD	Q	QN
0	0	1	0	1
1	0	1	1	0
x	1	1	Q	QN
x	x	0	0	1

TRUTH TABLE

GN TO (Q, QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH} (Q)	1.4	1.5	1.6	1.7	2.0	2.6
t_{PHL} (Q)	1.3	1.3	1.4	1.4	1.6	2.0
t_{PLH} (QN)	1.8	1.9	2.0	2.0	2.3	2.8
t_{PHL} (QN)	2.0	2.0	2.0	2.1	2.2	2.5

Q Output	Slope 1	= 0.0788	Incpt	=	1.35
	Slope 0	= 0.0477	Incpt	=	1.23
QN Output	Slope 1	= 0.0653	Incpt	=	1.76
	Slope 0	= 0.0347	Incpt	=	1.94

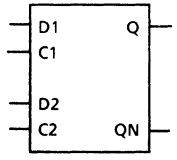
PARAMETER	NS
t_{SETUP} (Input Setup Time)	0.7
t_{HOLD} (Input Hold Time)	0.4
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel CD Release time CD to CLK	0.5

PROPAGATION	DELAY
CD ↓ to Q ↓	t_{PHL} (Q) + 0.4
CD ↓ to QN ↑	t_{PHL} (QN) + 0.4

Gate Count : 6
Coding Syntax: Z (Q, QN) = LD4P (D,GN,CD);
Input Loading: (1, 1, 1)

DLATCH WITH SCAN TEST INPUTS

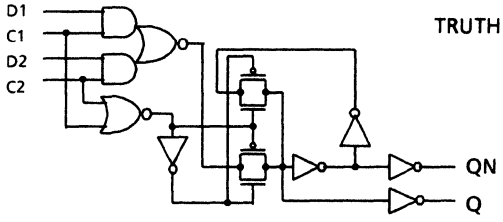
STANDARD DRIVE



LOGIC SYMBOL

D1	C1	D2	C2	Q	QN
x	0	x	0	Q	QN
x	0	1	1	1	0
x	0	0	1	0	1
1	1	x	0	1	0
0	1	x	0	0	1
1	1	x	1	1	0
x	1	1	0	1	0

TRUTH TABLE



SCHEMATIC

C1/C2 TO (Q,QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.4	1.6	1.8	1.9	2.5	3.7
t_{PHL}(Q)	1.0	1.1	1.2	1.3	1.6	2.3
t_{PLH}(QN)	1.5	1.7	1.8	2.0	2.5	3.7
t_{PHL}(QN)	1.6	1.7	1.7	1.8	2.0	2.5

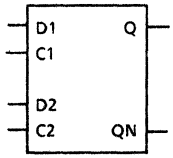
Q Output	Slope 1	= 0.1506	Incpt =	1.30
	Slope 0	= 0.0854	Incpt =	0.93
QN Output	Slope 1	= 0.1443	Incpt =	1.38
	Slope 0	= 0.0589	Incpt =	1.55

PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.1
t_{HOLD}(Input Hold Time)	0.0
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

Gate Count: 7
Coding Syntax: Z (Q, QN) = LS1 (D1,C1,D2,C2);
Input Loading: (1, 2, 1, 2)

LS1P DLATCH WITH SCAN TEST INPUTS LS1P

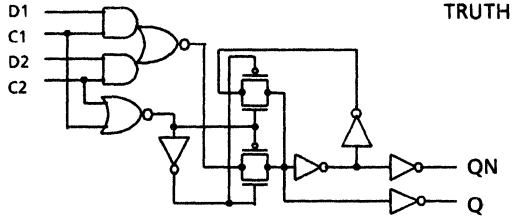
HIGH DRIVE



LOGIC SYMBOL

D1	C1	D2	C2	Q	QN
x	0	x	0	Q	QN
x	0	1	1	1	0
x	0	0	1	0	1
1	1	x	0	1	0
0	1	x	0	0	1
1	1	x	1	1	0
x	1	1	0	1	0

TRUTH TABLE



SCHEMATIC

C1/C2 TO (Q,QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q)	1.3	1.4	1.5	1.6	1.9	2.5
t_{PHL}(Q)	1.0	1.1	1.1	1.2	1.4	1.8
t_{PLH}(QN)	1.6	1.7	1.8	1.8	2.1	2.7
t_{PHL}(QN)	2.0	2.0	2.0	2.1	2.2	2.5

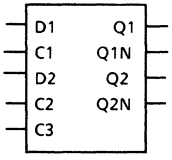
Q Output	Slope 1	= 0.0788	Incpt =	1.25
	Slope 0	= 0.0523	Incpt =	0.97
QN Output	Slope 1	= 0.0718	Incpt =	1.54
	Slope 0	= 0.0347	Incpt =	1.94

PARAMETER	NS
t_{SETUP} (Input Setup Time)	1.3
t_{HOLD} (Input Hold Time)	0.0
t_W (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

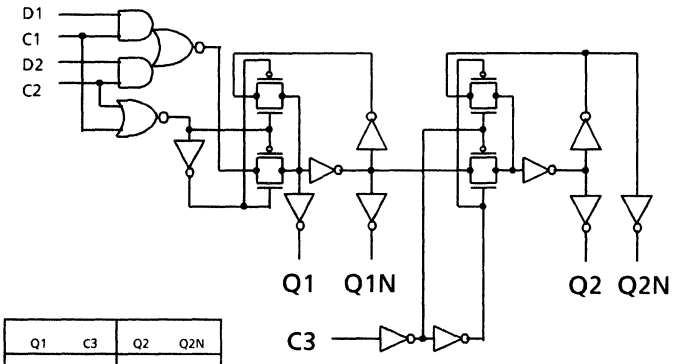
Gate Count: 8
Coding Syntax: Z (Q, QN) = LS1P (D1,C1,D2,C2);
Input Loading: (1, 2 , 1, 2)

LS2 DLATCH INTO DLATCH WITH SCAN TEST INPUTS LS2

STANDARD DRIVE



LOGIC SYMBOL



SCHEMATIC

D1	C1	D2	C2	Q	QN
x	0	x	0	Q	QN
x	0	1	1	1	0
x	0	0	1	0	1
1	1	x	0	1	0
0	1	x	0	0	1
*1	1	x	1	1	0
*x	1	1	0	1	0

Q1	C3	Q2	Q2N
x	0	Q2	Q2N
0	1	0	1
1	1	1	0

TRUTH TABLE

C1/C2 TO (Q1,Q1N) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

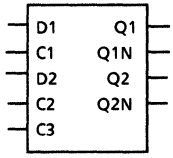
STD LOAD	1	2	3	4	8	16
t_{PLH}(Q1) t_{PHL}(Q1)	1.4 1.0	1.6 1.1	1.8 1.2	1.9 1.3	2.5 1.6	3.7 2.3
t_{PLH}(Q1N) t_{PHL}(Q1N)	1.6 1.7	1.8 1.8	1.9 1.8	2.1 1.9	2.6 2.1	3.8 2.6

Q1 Output	Slope 1	=	0.1506	Incpt =	1.30
	Slope 0	=	0.0854	Incpt =	0.93
Q1N Output	Slope 1	=	0.1443	Incpt =	1.48
	Slope 0	=	0.0589	Incpt =	1.65

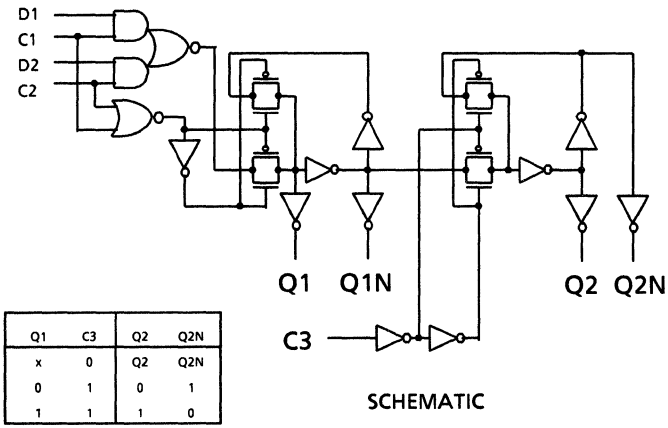
PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.3
t_{HOLD}(Input Hold Time)	0.0
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

Gate Count: 11
Coding Syntax: Z(Q1, Q1N,Q2,Q2N) = LS2 (D1,C1,D2,C2,C3);
Input Loading: (1, 2, 1, 2, 1)

LS2P DLATCH INTO DLATCH WITH SCAN TEST INPUTS LS2P
HIGH DRIVE



LOGIC SYMBOL



SCHEMATIC

D1	C1	D2	C2	Q	QN
x	0	x	0	Q	QN
x	0	1	1	1	0
x	0	0	1	0	1
0	1	x	0	1	0
1	1	x	0	1	0
*1	1	x	1	1	0
*x	1	1	0	1	0

*UNCONVENTIONAL

Q1	C3	Q2	Q2N
x	0	Q2	Q2N
0	1	0	1
1	1	1	0

TRUTH TABLE

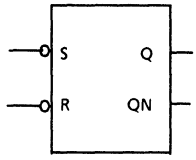
CP TO (Q1,Q1N) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Q1)	1.3	1.4	1.5	1.6	1.9	2.5
t_{PHL}(Q1)	1.0	1.1	1.1	1.2	1.4	1.8
t_{PLH}(Q1N)	1.7	1.8	1.9	1.9	2.2	2.8
t_{PHL}(Q1N)	2.1	2.1	2.1	2.2	2.3	2.6

Q1 Output	Slope 1	= 0.0788	Incpt =	1.25
	Slope 0	= 0.0523	Incpt =	0.97
Q1N Output	Slope 1	= 0.0718	Incpt =	1.64
	Slope 0	= 0.0347	Incpt =	2.04

PARAMETER	NS
t_{SETUP}(Input Setup Time)	1.5
t_{HOLD}(Input Hold Time)	0.0
t_W(CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5

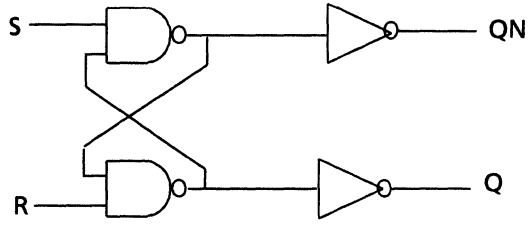
Gate Count: 13
Coding Syntax: Z(Q1, Q1N,Q2,Q2N) = LS2P (D1,C1,D2,C2,C3);
Input Loading: (1, 2, 1, 2, 1)



LOGIC SYMBOL

S	R	Q	QN
0	0	0	0
0	1	1	0
1	0	0	1
1	1	Q	QN

TRUTH TABLE



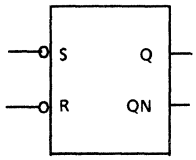
ELECTRICAL SCHEMATIC

S TO (Q,QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8
t_{PLH}(Q) t_{PHL}(Q)	1.7 1.0	1.8 1.0	2.0 1.1	2.1 1.1	2.7 1.4
t_{PLH}(QN) t_{PHL}(QN)	1.7 1.0	1.8 1.0	2.0 1.1	2.1 1.1	2.7 1.4

Q Output	Slope 1 = 0.1477	Incpt = 1.53
	Slope 0 = 0.0557	Incpt = 0.92
QN Output	Slope 1 = 0.1477	Incpt = 1.53
	Slope 0 = 0.0557	Incpt = 0.92

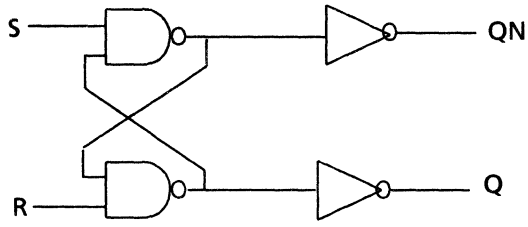
Gate Count: 3
Coding Syntax: Z (Q, QN) = LSR0 (S, R);
Input Loading: (1, 1)



LOGIC SYMBOL

S	R	Q	QN
0	0	0	0
0	1	1	0
1	0	0	1
1	1	Q	QN

TRUTH TABLE



ELECTRICAL SCHEMATIC

S TO (Q,QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

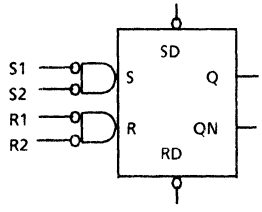
STD LOAD	1	2	3	4	8
t_{PLH}(Q)	1.8	1.9	1.9	2.0	2.3
t_{PHL}(Q)	1.0	1.0	1.1	1.1	1.3
t_{PLH}(QN)	1.8	1.9	1.9	2.0	2.3
t_{PHL}(QN)	1.0	1.0	1.1	1.1	1.3

Q Output	Slope 1 = 0.0735	Incpt = 1.72
	Slope 0 = 0.0345	Incpt = 0.97
QN Output	Slope 1 = 0.0735	Incpt = 1.72
	Slope 0 = 0.0345	Incpt = 0.97

Gate Count: 4
Coding Syntax: Z (Q, QN) = LSR0P (S, R);
Input Loading: (1,1)

LSR1 SR LATCH WITH SEPARATE GATE INPUTS, SD, RD LSR1

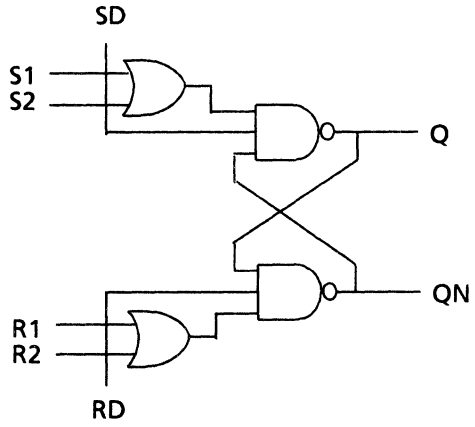
STANDARD DRIVE



LOGIC SYMBOL

S1,S2	R1,R2	SD	RD	Q	QN
x	x	0	1	1	0
x	x	1	0	0	1
x	x	0	0	1	1
1	1	1	1	Q	QN
1	0	1	1	0	1
0	1	1	1	1	0
0	0	1	1	1	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

S/R TO (Q,QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

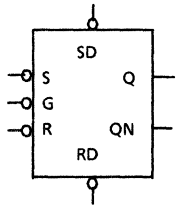
STD LOAD	1	2	3	4	8
t_{PLH}(Q)	1.0	1.3	1.6	1.8	2.9
t_{PHL}(Q)	1.3	1.4	1.6	1.7	2.1
t_{PLH}(QN)	1.0	1.3	1.6	1.8	2.9
t_{PHL}(QN)	1.3	1.4	1.6	1.7	2.1

Q Output	Slope 1	=	0.2653	Incpt =	0.76
	Slope 0	=	0.1119	Incpt =	1.22
QN Output	Slope 1	=	0.2653	Incpt =	0.76
	Slope 0	=	0.1119	Incpt =	1.22

Gate Count: 4
Coding Syntax: Z(Q, QN) = LSR1 (S1,S2,SD,R1,R2,RD);
Input Loading: (1, 1, 1, 1, 1, 1)

LSR2 SR LATCH WITH COMMON GATED INPUTS, SD, RD LSR2

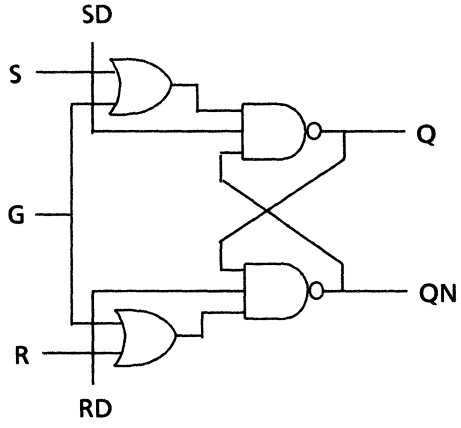
STANDARD DRIVE



LOGIC SYMBOL

S	R	G	SD	RD	Q	QN
x	x	x	0	1	1	0
x	x	x	1	0	0	1
x	x	x	0	0	1	1
x	x	1	1	1	Q	QN
1	1	0	1	1	Q	QN
1	0	0	1	1	0	1
0	1	0	1	1	1	0
0	0	0	1	1	1	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

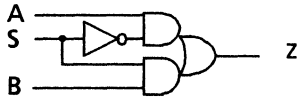
S/R TO (Q,QN) Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8
t_{PLH}(Q)	1.0	1.3	1.6	1.8	2.9
t_{PHL}(Q)	1.3	1.4	1.6	1.7	2.1
t_{PLH}(QN)	1.0	1.3	1.6	1.8	2.9
t_{PHL}(QN)	1.3	1.4	1.6	1.7	2.1

Q Output	Slope 1	=	0.2653	Incpt =	0.76
	Slope 0	=	0.1119	Incpt =	1.22
QN Output	Slope 1	=	0.2653	Incpt =	0.76
	Slope 0	=	0.1119	Incpt =	1.22

Gate Count: 4
Coding Syntax: Z (Q, QN) = LSR2 (S,R,G,SD,RD);
Input Loading: (1,1,2, 1, 1)

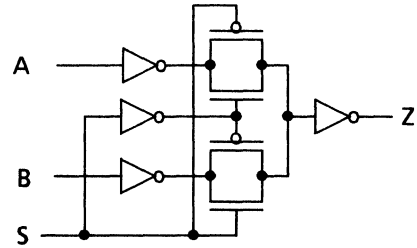
NON-INVERTING GATE MULTIPLEXER



LOGIC SYMBOL

S	A	B	Z
0	0	x	0
0	1	x	1
1	x	0	0
1	x	1	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

MUX21H (A/S TO Z) (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH} (A-Z)	0.7	0.8	0.9	0.9	1.2	1.8
t_{PHL} (A-Z)	1.2	1.3	1.3	1.4	1.6	2.1
t_{PLH} (S-Z)	0.9	1.0	1.1	1.1	1.4	2.0
t_{PHL} (S-Z)	0.9	1.0	1.0	1.1	1.3	1.8

A-Z Output	Slope 1	= 0.0718	Incpt	=	0.64
	Slope 0	= 0.0589	Incpt	=	1.15
S-Z Output	Slope 1	= 0.0718	Incpt	=	0.84
	Slope 0	= 0.0589	Incpt	=	0.85

Gate Count: 4
Coding Syntax: Z = MUX21H (A,B,S);
Input Loading: (1,1,2)

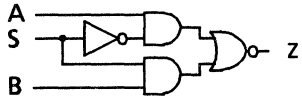
MUX21HP (A/S TO Z) (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH} (A-Z)	0.8	0.8	0.9	0.9	1.0	1.3
t_{PHL} (A-Z)	1.3	1.3	1.4	1.4	1.6	1.9
t_{PLH} (S-Z)	1.0	1.0	1.1	1.1	1.2	1.5
t_{PHL} (S-Z)	1.0	1.0	1.1	1.1	1.3	1.6

A-Z Output	Slope 1	= 0.0331	Incpt	=	0.76
	Slope 0	= 0.0411	Incpt	=	1.25
S-Z Output	Slope 1	= 0.0331	Incpt	=	0.96
	Slope 0	= 0.0411	Incpt	=	0.95

Gate Count: 5
Coding Syntax: Z = MUX21HP (A,B,S);
Input Loading: (1,1,2)

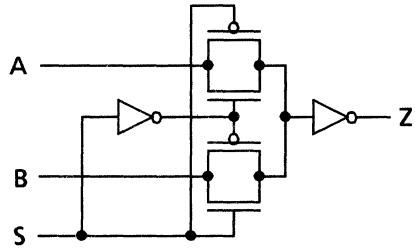
INVERTING GATE MULTIPLEXER



LOGIC SYMBOL

S	A	B	Z
0	0	x	1
0	1	x	0
1	x	0	1
1	x	1	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

MUX21L (A/S TO Z) (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH} (A-Z)	0.4	0.5	0.6	0.6	0.9	1.4
t_{PHL} (A-Z)	0.4	0.5	0.5	0.6	0.8	1.2
t_{PLH} (S-Z)	0.8	0.9	1.0	1.0	1.3	1.8
t_{PHL} (S-Z)	0.6	0.7	0.7	0.8	1.0	1.4

A-Z Output	Slope 1	=	0.0653	Incpt	=	0.36
	Slope 0	=	0.0523	Incpt	=	0.37
S-Z Output	Slope 1	=	0.0653	Incpt	=	0.76
	Slope 0	=	0.0523	Incpt	=	0.57

Gate Count: 3
Coding Syntax: Z = MUX21L (A,B,S);
Input Loading: (2,2,2)

MUX21LP (A/S TO Z) (HIGH DRIVE)

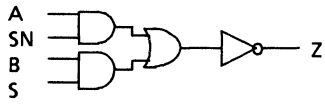
STD LOAD	1	2	3	4	8	16
t_{PLH} (A-Z)	0.5	0.5	0.6	0.6	0.7	1.0
t_{PHL} (A-Z)	0.4	0.4	0.5	0.5	0.6	0.9
t_{PLH} (S-Z)	0.9	0.9	1.0	1.0	1.1	1.4
t_{PHL} (S-Z)	0.7	0.7	0.8	0.8	0.9	1.2

A-Z Output	Slope 1	=	0.0331	Incpt	=	0.46
	Slope 0	=	0.0331	Incpt	=	0.36
S-Z Output	Slope 1	=	0.0331	Incpt	=	0.86
	Slope 0	=	0.0331	Incpt	=	0.66

Gate Count: 4
Coding Syntax: Z = MUX21LP (A,B,S);
Input Loading: (2,2,2)

MUX21LA / MUX21LAP MUX21LA / MUX21LAP

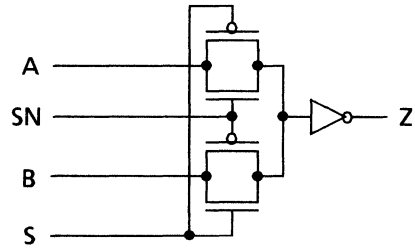
TWO TO ONE MUX, INVERTING OUTPUT



LOGIC SYMBOL

S	SN	A	B	Z
1	0	x	0	1
1	0	x	1	0
0	1	0	x	1
0	1	1	x	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

MUX21LA (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.4	0.6	0.7	0.9	1.4	2.6
t_{PHL}	0.6	0.7	0.7	0.8	1.0	1.4

Slope1 = 0.1443 Incpt = 0.28
Slope0 = 0.0523 Incpt = 0.57

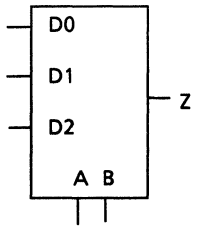
Gate Count: 2
Coding Syntax: Z = MUX21LA (SN,A,S,B);
Input loading: (1, 2,1,2)

MUX21LAP (HIGH DRIVE)

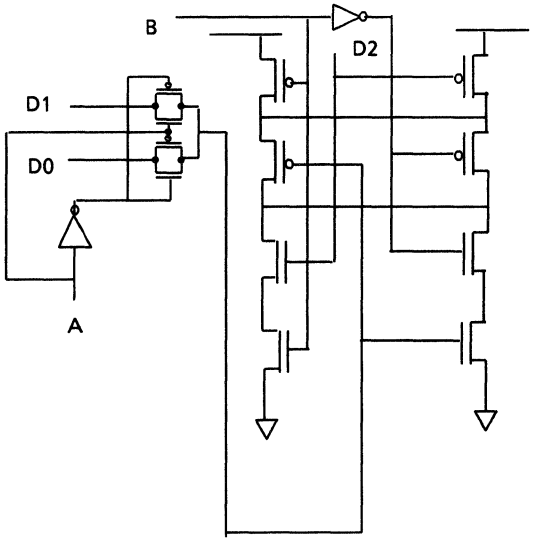
STD LOAD	1	2	3	4	8	16
t_{PLH}	0.5	0.6	0.7	0.7	1.0	1.5
t_{PHL}	0.6	0.6	0.6	0.7	0.8	1.1

Slope1 = 0.0653 Incpt = 0.46
Slope0 = 0.0347 Incpt = 0.54

Gate Count: 2
Coding Syntax: Z = MUX21LAP (SN,A, S, B);
Input loading: (1,2.3,1,2.3)



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

A	B	Z
0	0	D0
1	0	D1
X	1	D2

TRUTH TABLE

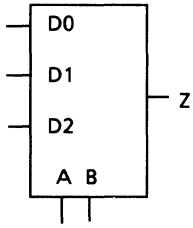
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

MUX31L (STANDARD DRIVE)

STD LOAD	1	2	4	8
t_{PLH}(D0-Z) t_{PHL} (D0-Z)	1.5 0.7	1.7 0.7	2.3 0.9	3.3 1.2
t_{PLH} (D2-Z) t_{PHL} (D2-Z)	1.0 0.6	1.2 0.6	1.8 0.8	2.8 1.1
t_{PLH} (A-Z) t_{PHL} (A-Z)	1.8 0.9	2.0 0.9	2.6 1.1	3.6 1.4
t_{PLH} (B-Z) t_{PHL} (B-Z)	1.0 0.6	1.2 0.6	1.8 0.8	2.8 1.1

D0-Z Output	Slope 1	= 0.2612	Incpt	=	1.22
	Slope 0	= 0.0824	Incpt	=	0.57
D2-Z Output	Slope 1	= 0.2612	Incpt	=	0.72
	Slope 0	= 0.0824	Incpt	=	0.47
A-Z Output	Slope 1	= 0.2612	Incpt	=	1.52
	Slope 0	= 0.0824	Incpt	=	0.77
B-Z Output	Slope 1	= 0.2612	Incpt	=	0.72
	Slope 0	= 0.0824	Incpt	=	0.47

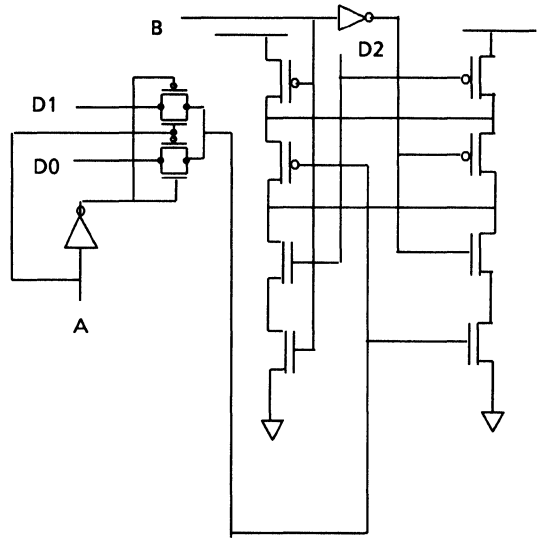
Gate Count: 4
Coding Syntax: Z = MUX31L (D0 ,D1 ,D2,A,B);
Input Loading: (2.25,2.25,2 ,2 ,3)



LOGIC SYMBOL

A	B	Z
0	0	D0
1	0	D1
X	1	D2

TRUTH TABLE



ELECTRICAL SCHEMATIC

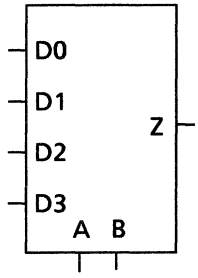
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

MUX31LP (HIGH DRIVE)

STD LOAD	1	2	4	8	16
t_{PLH}(D0-Z)	1.2	1.3	1.6	2.1	3.2
t_{PHL}(D0-Z)	0.5	0.5	0.6	0.8	1.1
t_{PLH}(D2-Z)	0.7	0.8	1.1	1.6	2.7
t_{PHL}(D2-Z)	0.4	0.4	0.5	0.7	1.0
t_{PLH}(A-Z)	1.3	1.4	1.7	2.2	3.3
t_{PHL}(A-Z)	0.9	0.9	1.0	1.2	1.5
t_{PLH}(B-Z)	0.7	0.8	1.1	1.6	2.7
t_{PHL}(B-Z)	0.4	0.4	0.5	0.7	1.0

D0-Z Output	Slope 1	= 0.1331	Incpt	=	1.06
	Slope 0	= 0.0411	Incpt	=	0.45
D2-Z Output	Slope 1	= 0.1331	Incpt	=	0.56
	Slope 0	= 0.0411	Incpt	=	0.35
A-Z Output	Slope 1	= 0.1331	Incpt	=	1.16
	Slope 0	= 0.0411	Incpt	=	0.85
B-Z Output	Slope 1	= 0.1331	Incpt	=	0.56
	Slope 0	= 0.0411	Incpt	=	0.35

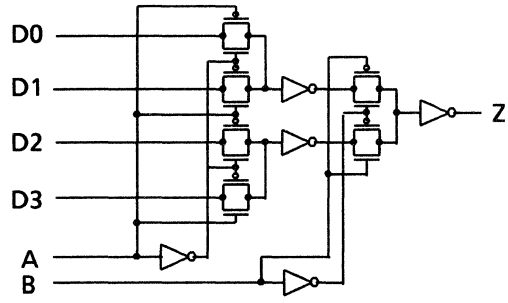
Gate Count: 6
Coding Syntax: Z = MUX31L (D0 ,D1 ,D2,A,B);
Input Loading: (2.25,2.25,2 ,2 ,3)



LOGIC SYMBOL

A	B	Z
0	0	D0
1	0	D1
0	1	D2
1	1	D3

TRUTH TABLE



ELECTRICAL SCHEMATIC

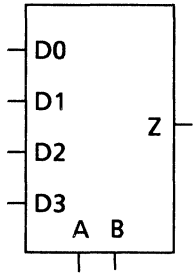
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

MUX41 (STANDARD DRIVE)

STD LOAD	1	2	4	8	16
t_{PLH}(D0-Z) t_{PHL}(D0-Z)	0.8 1.0	1.0 1.1	1.3 1.2	1.8 1.5	3.0 1.9
t_{PLH}(A-Z) t_{PHL}(A-Z)	0.9 1.4	1.1 1.5	1.4 1.6	1.9 1.9	3.1 2.3
t_{PLH}(B-Z) t_{PHL}(B-Z)	0.9 0.7	1.1 0.8	1.4 0.9	1.9 1.2	3.1 1.6

D0-Z Output	Slope 1	= 0.1440	Incpt	=	0.69
	Slope 0	= 0.0595	Incpt	=	0.97
A-Z Output	Slope 1	= 0.1440	Incpt	=	0.79
	Slope 0	= 0.0595	Incpt	=	1.37
B-Z Output	Slope 1	= 0.1440	Incpt	=	0.79
	Slope 0	= 0.0595	Incpt	=	0.67

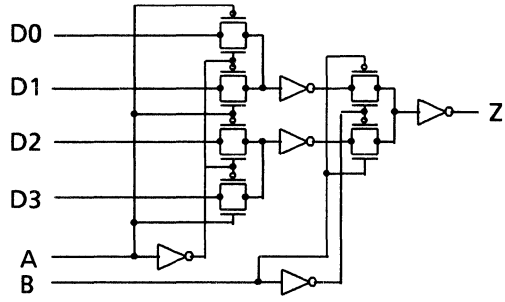
Gate Count: 6
Coding Syntax: Z = MUX41 (D0,D1,D2,D3,A,B);
Input Loading: (2, 2, 2, 2, 3,2)



LOGIC SYMBOL

A	B	Z
0	0	D0
1	0	D1
0	1	D2
1	1	D3

TRUTH TABLE



ELECTRICAL SCHEMATIC

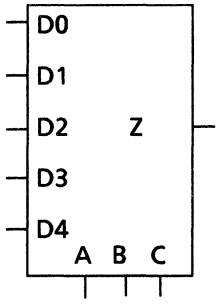
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

MUX41P (HIGH DRIVE)

STD LOAD	1	2	4	8	16
t_{PLH} (D0-Z)	0.8	0.9	1.0	1.3	1.9
t_{PHL} (D0-Z)	1.0	1.0	1.1	1.3	1.6
t_{PLH} (A-Z)	0.9	1.0	1.1	1.4	2.0
t_{PHL} (A-Z)	1.3	1.3	1.4	1.6	1.9
t_{PLH} (B-Z)	0.9	1.0	1.1	1.4	2.0
t_{PHL} (B-Z)	0.7	0.7	0.8	1.0	1.3

D0-Z Output	Slope 1	= 0.0727	Incpt	=	0.73
	Slope 0	= 0.0417	Incpt	=	0.94
A-Z Output	Slope 1	= 0.0727	Incpt	=	0.83
	Slope 0	= 0.0417	Incpt	=	1.24
B-Z Output	Slope 1	= 0.0727	Incpt	=	0.83
	Slope 0	= 0.0417	Incpt	=	0.64

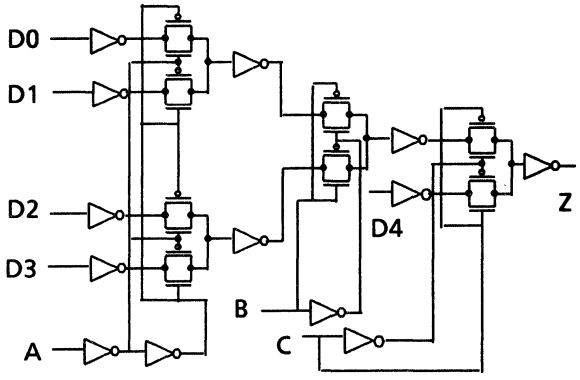
Gate Count: 7
Coding Syntax: Z = MUX41P (D0,D1,D2,D3,A,B);
Input Loading: (2, 2, 2, 2, 3,2)



LOGIC SYMBOL

A	B	C	Z
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
X	X	1	D4

TRUTH TABLE



ELECTRICAL SCHEMATIC

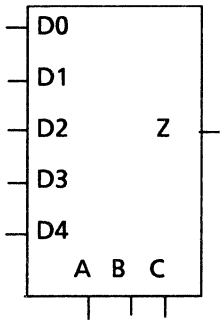
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

MUX51H (STANDARD DRIVE)

STD LOAD	1	2	4	8	16
t_{PLH}(D0-Z)	1.9	2.1	2.4	3.0	4.1
t_{PHL}(D0-Z)	2.0	2.1	2.2	2.5	3.0
t_{PLH}(D4-Z)	0.8	1.0	1.3	1.9	3.0
t_{PHL}(D4-Z)	1.0	1.1	1.2	1.5	2.0
t_{PLH}(A-Z)	2.3	2.5	2.8	3.4	4.5
t_{PHL}(A-Z)	1.9	2.0	2.1	2.4	2.9
t_{PLH}(B-Z)	1.4	1.6	1.9	2.5	3.6
t_{PHL}(B-Z)	1.0	1.1	1.2	1.5	2.0
t_{PLH}(C-Z)	1.0	1.2	1.5	2.1	3.2
t_{PHL}(C-Z)	0.7	0.8	0.9	1.2	1.7

D0-Z Output	Slope 1	= 0.1458	Incpt	=	1.79
	Slope 0	= 0.0669	Incpt	=	1.94
D4-Z Output	Slope 1	= 0.1458	Incpt	=	0.69
	Slope 0	= 0.0669	Incpt	=	0.94
A-Z Output	Slope 1	= 0.1458	Incpt	=	2.19
	Slope 0	= 0.0669	Incpt	=	1.84
B-Z Output	Slope 1	= 0.1458	Incpt	=	1.29
	Slope 0	= 0.0669	Incpt	=	0.94
C-Z Output	Slope 1	= 0.1458	Incpt	=	0.89
	Slope 0	= 0.0669	Incpt	=	0.64

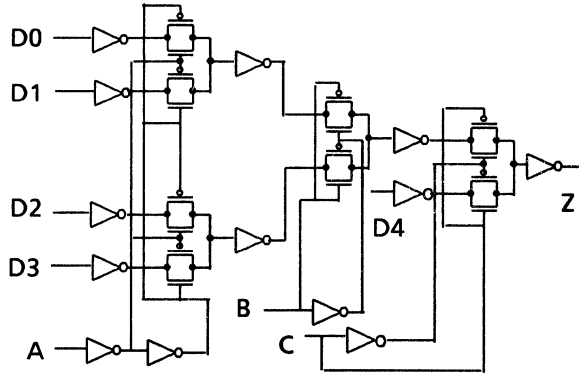
Gate Count: 11
Coding Syntax: Z = MUX51H (D0,D1,D2,D3,D4,A,B,C);
Input Loading: (1 ,1 ,1 ,1 , 1 ,1 ,2,2)



LOGIC SYMBOL

A	B	C	Z
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
X	X	1	D4

TRUTH TABLE



ELECTRICAL SCHEMATIC

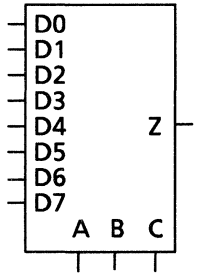
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

MUX51HP (HIGH DRIVE)

STD LOAD	1	2	4	8	16
t_{PLH} (D0-Z)	1.9	2.0	2.1	2.4	3.0
t_{PHL} (D0-Z)	2.1	2.1	2.2	2.4	2.7
t_{PLH} (D4-Z)	0.8	0.9	1.0	1.3	1.9
t_{PHL} (D4-Z)	1.1	1.1	1.2	1.4	1.7
t_{PLH} (A-Z)	2.3	2.4	2.5	2.8	3.4
t_{PHL} (A-Z)	2.0	2.0	2.1	2.3	2.6
t_{PLH} (B-Z)	1.4	1.5	1.6	1.9	2.5
t_{PHL} (B-Z)	1.1	1.1	1.2	1.4	1.7
t_{PLH} (C-Z)	1.0	1.1	1.2	1.5	2.1
t_{PHL} (C-Z)	0.8	0.8	0.9	1.1	1.4

D0-Z Output	Slope 1	= 0.0718	Incpt	=	1.84
	Slope 0	= 0.0411	Incpt	=	2.05
D4-Z Output	Slope 1	= 0.0718	Incpt	=	0.74
	Slope 0	= 0.0411	Incpt	=	1.05
A-Z Output	Slope 1	= 0.0718	Incpt	=	2.24
	Slope 0	= 0.0411	Incpt	=	1.95
B-Z Output	Slope 1	= 0.0718	Incpt	=	1.34
	Slope 0	= 0.0411	Incpt	=	1.05
C-Z Output	Slope 1	= 0.0718	Incpt	=	0.94
	Slope 0	= 0.0411	Incpt	=	0.75

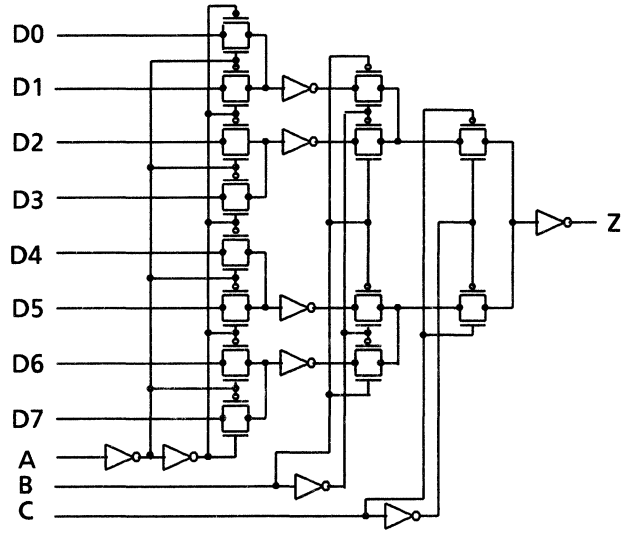
Gate Count: 11
Coding Syntax: Z = MUX51HP (D0,D1,D2,D3,D4,A,B,C);
Input Loading: (1 ,1 ,1 ,1 ,1 ,1 ,2,2)



LOGIC SYMBOL

A	B	C	Z
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D7

TRUTH TABLE



ELECTRICAL SCHEMATIC

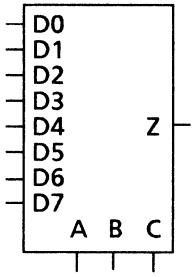
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

MUX81 (STANDARD DRIVE)

STD LOAD	1	2	4	8	16
t_{PLH} (D0-Z)	1.2	1.4	1.7	2.2	3.4
t_{PHL} (D0-Z)	1.3	1.4	1.6	1.9	2.5
t_{PLH} (A-Z)	1.9	2.1	2.4	2.9	4.1
t_{PHL} (A-Z)	2.4	2.5	2.7	3.0	3.6
t_{PLH} (B-Z)	1.2	1.4	1.7	2.2	3.4
t_{PHL} (B-Z)	0.9	1.0	1.2	1.5	2.1
t_{PLH} (C-Z)	1.0	1.2	1.5	2.0	3.2
t_{PHL} (C-Z)	0.7	0.8	1.0	1.3	1.9

D0-Z Output	Slope 1	=	0.1440	Incpt	= 1.09
	Slope 0	=	0.0790	Incpt	= 1.25
A-Z Output	Slope 1	=	0.1440	Incpt	= 1.79
	Slope 0	=	0.0790	Incpt	= 2.35
B-Z Output	Slope 1	=	0.1440	Incpt	= 1.09
	Slope 0	=	0.0790	Incpt	= 0.85
C-Z Output	Slope 1	=	0.1440	Incpt	= 0.89
	Slope 0	=	0.0790	Incpt	= 0.65

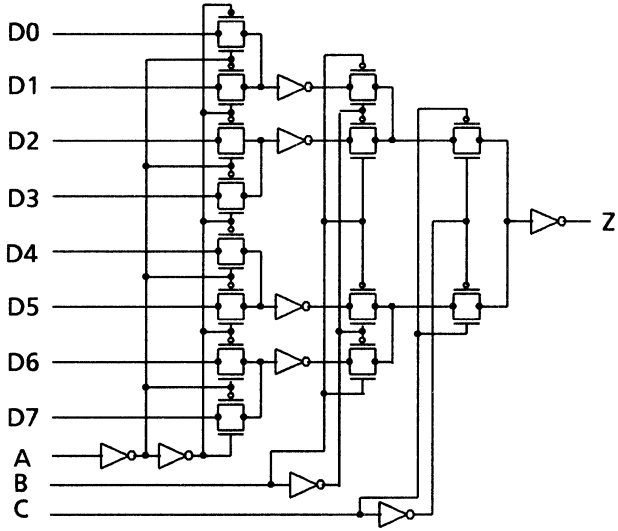
Gate Count: 15
Coding Syntax: Z = MUX81 (D0,D1,D2,D3,D4,D5,D6,D7,A,B,C);
Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 1,3,2)



LOGIC SYMBOL

A	B	C	Z
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D7

TRUTH TABLE



ELECTRICAL SCHEMATIC

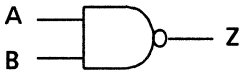
Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

MUX81P (HIGH DRIVE)

STD LOAD	1	2	4	8	16
t_{PLH} (D0-Z)	1.4	1.5	1.6	1.9	2.5
t_{PHL} (D0-Z)	1.2	1.2	1.3	1.5	1.9
t_{PLH} (A-Z)	2.2	2.3	2.4	2.7	3.3
t_{PHL} (A-Z)	2.1	2.1	2.2	2.4	2.8
t_{PLH} (B-Z)	1.2	1.3	1.4	1.7	2.3
t_{PHL} (B-Z)	1.0	1.0	1.1	1.3	1.7
t_{PLH} (C-Z)	0.9	1.0	1.1	1.4	2.0
t_{PHL} (C-Z)	0.7	0.7	0.8	1.0	1.4

D0-Z Output	Slope 1	= 0.0727	Incpt	=	1.33
	Slope 0	= 0.0483	Incpt	=	1.12
A-Z Output	Slope 1	= 0.0727	Incpt	=	2.13
	Slope 0	= 0.0483	Incpt	=	2.02
B-Z Output	Slope 1	= 0.0727	Incpt	=	1.13
	Slope 0	= 0.0483	Incpt	=	0.92
C-Z Output	Slope 1	= 0.0727	Incpt	=	0.83
	Slope 0	= 0.0483	Incpt	=	0.62

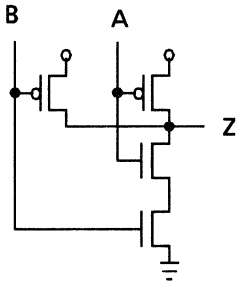
Gate Count: 15
Coding Syntax: Z = MUX81P (D0,D1,D2,D3,D4,D5,D6,D7,A,B,C);
Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 1,3,2)



LOGIC SYMBOL

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

ND2 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.6	0.8	0.9	1.1	1.6	2.7
t_{PHL}	0.2	0.3	0.4	0.5	0.8	1.5

Slope1 = 0.1377 Incpt = 0.50
Slope0 = 0.0854 Incpt = 0.13

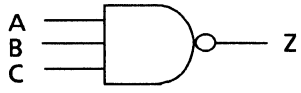
Gate Count: 1
Coding Syntax: Z = ND2 (A,B);
Input loading: (1,1)

ND2P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.6	0.6	0.7	0.7	1.0	1.5
t_{PHL}	0.2	0.3	0.3	0.3	0.5	0.9

Slope1 = 0.0623 Incpt = 0.50
Slope0 = 0.0453 Incpt = 0.16

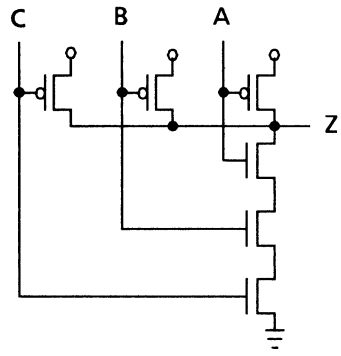
Gate Count: 2
Coding Syntax: Z = ND2P (A,B);
Input loading: (2,2)



LOGIC SYMBOL

A	B	C	Z
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

ND3 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.8	0.9	1.1	1.2	1.8	2.9
t_{PHL}	0.5	0.6	0.7	0.8	1.3	2.2

Slope1 = 0.1411 Incpt = 0.65
Slope0 = 0.1146 Incpt = 0.37

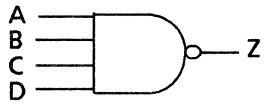
Gate Count: 2
Coding Syntax: Z = ND3 (A,B,C);
Input loading: (1,1,1)

ND3P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.7	0.8	0.8	0.9	1.2	1.7
t_{PHL}	0.5	0.5	0.6	0.6	0.8	1.3

Slope1 = 0.0669 Incpt = 0.64
Slope0 = 0.0542 Incpt = 0.41

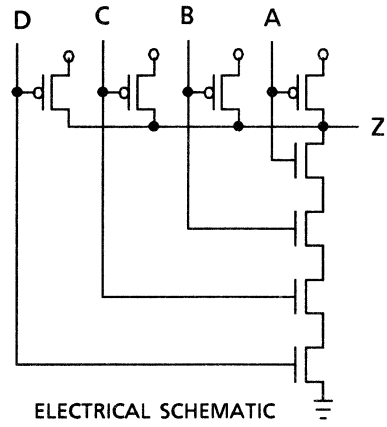
Gate Count: 3
Coding Syntax: Z = ND3P (A,B,C);
Input loading: (2,2,2)



LOGIC SYMBOL

A	B	C	D	Z
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

ND4 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.8	0.9	1.1	1.2	1.8	2.9
t_{PHL}	0.6	0.7	0.9	1.0	1.6	2.7

Slope1 = 0.1411 Incpt = 0.65
Slope0 = 0.1411 Incpt = 0.45

Gate Count: 2
Coding Syntax: Z = ND4 (A,B,C,D);
Input loading: (1,1, 1,1)

ND4P (HIGH DRIVE)

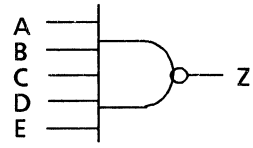
STD LOAD	1	2	3	4	8	16
t_{PLH}	0.7	0.8	0.8	0.9	1.2	1.8
t_{PHL}	0.5	0.6	0.6	0.7	1.0	1.6

Slope1 = 0.0735 Incpt = 0.62
Slope0 = 0.0735 Incpt = 0.42

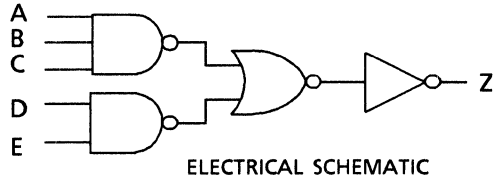
Gate Count: 4
Coding Syntax: Z = ND4P (A,B,C,D);
Input loading: (2,2, 2,2)

A	B	C	D	E	Z
0	x	x	x	x	1
x	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
1	1	1	1	1	0

TRUTH TABLE



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

ND5 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.2	1.4	1.5	1.7	2.2	3.4
t_{PHL}	1.2	1.3	1.3	1.4	1.6	2.1

Slope1 = 0.1443 Incpt = 1.08
Slope0 = 0.0589 Incpt = 1.15

Gate Count: 4
Coding Syntax: Z = ND5 (A,B,C,D,E);
Input loading: (1,1, 1,1.1)

ND5P (HIGH DRIVE)

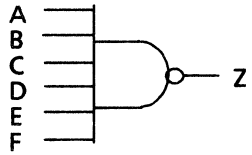
STD LOAD	1	2	3	4	8	16
t_{PLH}	1.2	1.3	1.4	1.4	1.7	2.2
t_{PHL}	1.3	1.3	1.4	1.4	1.5	1.8

Slope1 = 0.0653 Incpt = 1.16
Slope0 = 0.0331 Incpt = 1.26

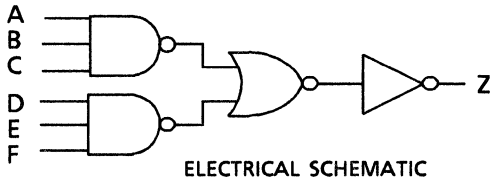
Gate Count: 5
Coding Syntax: Z = ND5P (A,B,C,D,E);
Input loading: (1,1, 1,1,1)

A	B	C	D	E	F	Z
0	x	x	x	x	x	1
x	0	x	x	x	x	1
x	x	0	x	x	x	1
x	x	x	0	x	x	1
x	x	x	x	0	x	1
x	x	x	x	x	0	1
1	1	1	1	1	1	0

TRUTH TABLE



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

ND6 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.1	1.3	1.4	1.6	2.1	3.3
t_{PHL}	1.2	1.3	1.3	1.4	1.6	2.1

Slope1 = 0.1443 Incpt = 0.98
Slope0 = 0.0589 Incpt = 1.15

Gate Count: 5
Coding Syntax: Z = ND6 (A,B,C,D,E,F);
Input loading: (1,1,1,1.1,1)

ND6P (HIGH DRIVE)

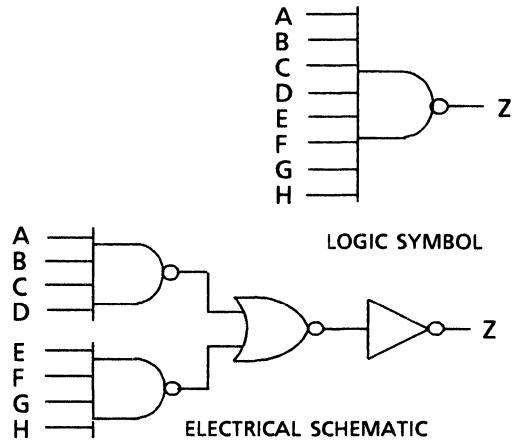
STD LOAD	1	2	3	4	8	16
t_{PLH}	1.1	1.2	1.3	1.3	1.6	2.1
t_{PHL}	1.3	1.3	1.4	1.4	1.5	1.8

Slope1 = 0.0653 Incpt = 1.06
Slope0 = 0.0331 Incpt = 1.26

Gate Count: 5
Coding Syntax: Z = ND6P (A,B,C,D,E,F);
Input loading: (1,1,1,1,1,1)

A	B	C	D	E	F	G	H	Z
0	x	x	x	x	x	x	x	1
x	0	x	x	x	x	x	x	1
x	x	0	x	x	x	x	x	1
x	x	x	0	x	x	x	x	1
x	x	x	x	0	x	x	x	1
x	x	x	x	x	0	x	x	1
x	x	x	x	x	x	0	x	1
x	x	x	x	x	x	x	0	1
1	1	1	1	1	1	1	1	0

TRUTH TABLE



Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

ND8 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.2	1.4	1.5	1.7	2.2	3.4
t_{PHL}	1.5	1.6	1.6	1.7	1.9	2.4

Slope1 = 0.1443 Incpt = 1.08
Slope0 = 0.0589 Incpt = 1.45

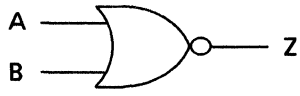
Gate Count: 6
Coding Syntax: Z = ND8 (A,B,C,D,E,F,G,H);
Input loading: (1,1,1,1. 1,1,1,1)

ND8P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.2	1.3	1.4	1.4	1.7	2.2
t_{PHL}	1.6	1.6	1.7	1.7	1.8	2.1

Slope1 = 0.0653 Incpt = 1.16
Slope0 = 0.0331 Incpt = 1.56

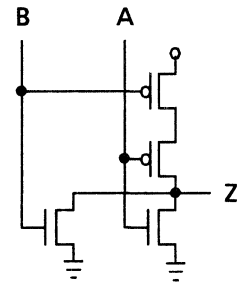
Gate Count: 6
Coding Syntax: Z = ND8P (A,B,C,D,E,F,G,H);
Input loading: (1,1,1, 1,1,1,1,1)



LOGIC SYMBOL

A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

NR2 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8
t_{PLH}	0.8	1.1	1.3	1.6	2.6
t_{PHL}	0.3	0.4	0.4	0.5	0.7

Slope1 = 0.2589 Incpt = 0.55
Slope0 = 0.0589 Incpt = 0.25

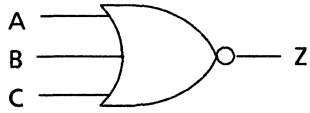
Gate Count: 1
Coding Syntax: Z = NR2 (A,B);
Input loading: (1,1)

NR2P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.7	0.8	0.9	1.1	1.6	2.6
t_{PHL}	0.2	0.2	0.3	0.3	0.4	0.7

Slope1 = 0.1282 Incpt = 0.56
Slope0 = 0.0331 Incpt = 0.16

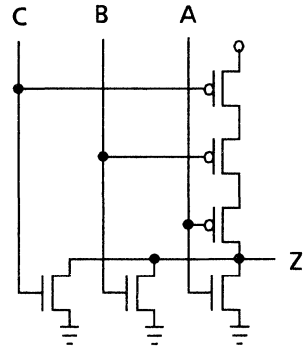
Gate Count: 2
Coding Syntax: Z = NR2P (A,B);
Input loading: (2,2)



LOGIC SYMBOL

A	B	C	Z
0	0	0	1
1	x	x	0
x	1	x	0
x	x	1	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

NR3 (STANDARD DRIVE)

STD LOAD	1	2	3	4
t_{PLH}	1.2	1.6	2.0	2.3
t_{PHL}	0.3	0.4	0.4	0.5

Slope1 = 0.3864 Incpt = 0.81
Slope0 = 0.0589 Incpt = 0.25

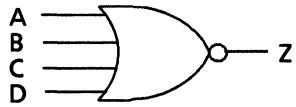
Gate Count: 2
Coding Syntax: Z = NR3 (A,B,C);
Input loading: (1,1,1)

NR3P (HIGH DRIVE)

STD LOAD	1	2	3	4	8
t_{PLH}	1.0	1.2	1.4	1.6	2.4
t_{PHL}	0.3	0.3	0.4	0.4	0.6

Slope1 = 0.1934 Incpt = 0.82
Slope0 = 0.0345 Incpt = 0.27

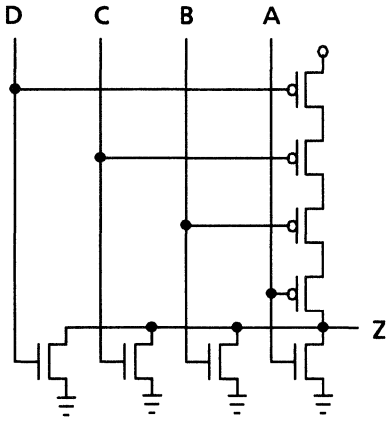
Gate Count: 3
Coding Syntax: Z = NR3P (A,B,C);
Input loading: (2,2,2)



LOGIC SYMBOL

A	B	C	D	Z
0	0	0	0	1
1	x	x	x	0
x	1	x	x	0
x	x	1	x	0
x	x	x	1	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

NR4 (STANDARD DRIVE)

STD LOAD	1	2	3	4
t_{PLH}	1.6	2.1	2.6	3.1
t_{PHL}	0.3	0.4	0.4	0.5

Slope1 = 0.5146 Incpt = 1.07
Slope0 = 0.0589 Incpt = 0.25

Gate Count: 2
Coding Syntax: Z = NR4 (A,B,C,D);
Input loading: (1,1, 1,1)

NR4P (HIGH DRIVE)

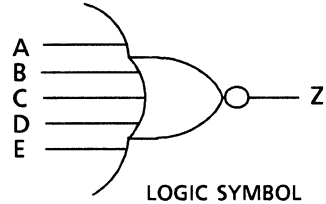
STD LOAD	1	2	3	4	8
t_{PLH}	1.4	1.6	1.9	2.1	3.2
t_{PHL}	0.3	0.3	0.4	0.4	0.6

Slope1 = 0.2557 Incpt = 1.12
Slope0 = 0.0345 Incpt = 0.27

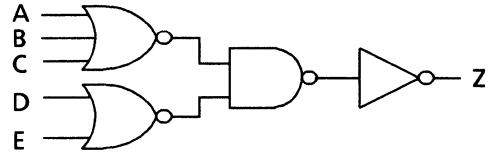
Gate Count: 4
Coding Syntax: Z = NR4P (A,B,C,D);
Input loading: (2,2, 2,2)

A	B	C	D	E	Z
0	0	0	0	0	1
1	x	x	x	x	0
x	1	x	x	x	0
x	x	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0

TRUTH TABLE



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

NR5 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.6	1.8	1.9	2.1	2.7	3.8
t_{PHL}	0.9	1.0	1.0	1.1	1.3	1.7

Slope1 = 0.1458 Incpt = 1.49
Slope0 = 0.0523 Incpt = 0.87

Gate Count: 4
Coding Syntax: Z = NR5 (A,B,C,D,E);
Input loading: (1,1, 1,1.1)

NR5P (HIGH DRIVE)

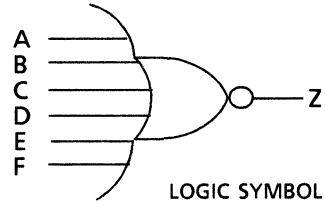
STD LOAD	1	2	3	4	8	16
t_{PLH}	1.7	1.8	1.9	1.9	2.2	2.8
t_{PHL}	0.9	0.9	0.9	1.0	1.1	1.3

Slope1 = 0.0718 Incpt = 1.64
Slope0 = 0.0282 Incpt = 0.86

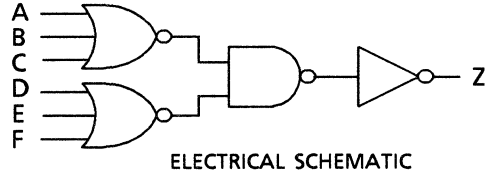
Gate Count: 5
Coding Syntax: Z = NR5P (A,B,C,D,E);
Input loading: (1,1, 1,1,1)

A	B	C	D	E	F	Z
0	0	0	0	0	0	1
1	x	x	x	x	x	0
x	1	x	x	x	x	0
x	x	1	x	x	x	0
x	x	x	1	x	x	0
x	x	x	x	1	x	0
x	x	x	x	x	1	0

TRUTH TABLE



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

NR6 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.7	1.9	2.0	2.2	2.8	3.9
t_{PHL}	0.9	1.0	1.0	1.1	1.3	1.7

Slope1 = 0.1458 Incpt = 1.59
Slope0 = 0.0523 Incpt = 0.87

Gate Count: 5
Coding Syntax: Z = NR6 (A,B,C,D,E,F);
Input loading: (1,1,1,1,1,1)

NR6P (HIGH DRIVE)

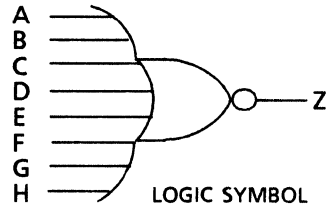
STD LOAD	1	2	3	4	8	16
t_{PLH}	1.8	1.9	2.0	2.0	2.3	2.9
t_{PHL}	1.0	1.0	1.0	1.1	1.2	1.5

Slope1 = 0.0718 Incpt = 1.74
Slope0 = 0.0347 Incpt = 0.94

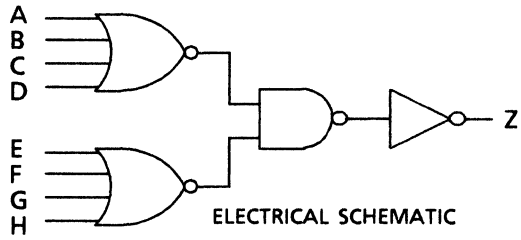
Gate Count: 5
Coding Syntax: Z = NR6P (A,B,C,D,E,F);
Input loading: (1,1,1,1,1,1)

A	B	C	D	E	F	G	H	Z
0	0	0	0	0	0	0	0	1
1	x	x	x	x	x	x	x	0
x	1	x	x	x	x	x	x	0
x	x	1	x	x	x	x	x	0
x	x	x	1	x	x	x	x	0
x	x	x	x	1	x	x	x	0
x	x	x	x	x	1	x	x	0
x	x	x	x	x	x	1	x	0
x	x	x	x	x	x	x	1	0

TRUTH TABLE



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

NR8 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	2.0	2.2	2.3	2.5	3.1	4.2
t_{PHL}	0.9	1.0	1.0	1.1	1.3	1.7

Slope1 = 0.1458 Incpt = 1.89
Slope0 = 0.0523 Incpt = 0.87

Gate Count: 6
Coding Syntax: Z = NR8 (A,B,C,D,E,F,G,H);
Input loading: (1,1,1, 1,1,1,1,1)

NR8P (HIGH DRIVE)

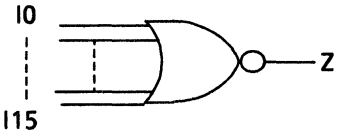
STD LOAD	1	2	3	4	8	16
t_{PLH}	2.1	2.2	2.3	2.3	2.6	3.2
t_{PHL}	0.9	0.9	0.9	1.0	1.1	1.4

Slope1 = 0.0718 Incpt = 2.04
Slope0 = 0.0347 Incpt = 0.84

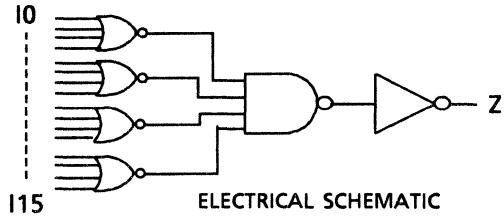
Gate Count: 6
Coding Syntax: Z = NR8P (A,B,C,D,E,F,G,H);
Input loading: (1,1,1, 1,1,1,1,1)

I0	I1	I2	I3	I4	I5	I6	I7	I8	I9	I10	I11	I12	I13	I14	I15	Z
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

TRUTH TABLE



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

NR16 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	2.4	2.6	2.7	2.9	3.5	4.7
t_{PHL}	1.0	1.1	1.1	1.2	1.4	1.9

Slope1 = 0.1523 Incpt = 2.27
Slope0 = 0.0589 Incpt = 0.95

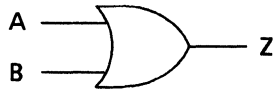
Gate Count: 11
Coding Syntax: Z = NR16 (I0,I1,I2,I3,I4,I5,I6,I7,I8,I9,I10,I11,I12,I13,I14,I15);
Input loading: (1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1)

NR16P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	2.5	2.6	2.7	2.8	3.1	3.7
t_{PHL}	1.1	1.1	1.2	1.2	1.3	1.7

Slope1 = 0.0788 Incpt = 2.45
Slope0 = 0.0396 Incpt = 1.04

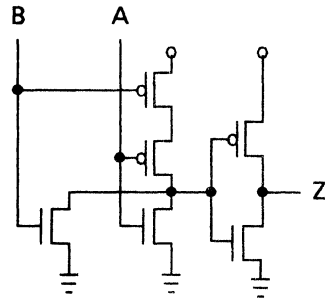
Gate Count: 11
Coding Syntax: Z = NR16P (I0,I1,I2,I3,I4,I5,I6,I7,I8,I9,I10,I11,I12,I13,I14,I15);
Input loading: (1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1)



LOGIC SYMBOL

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

OR2 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.5	0.7	0.8	1.0	1.5	2.7
t_{PHL}	0.9	1.0	1.0	1.1	1.3	1.8

Slope1 = 0.1443 Incpt = 0.38
Slope0 = 0.0589 Incpt = 0.85

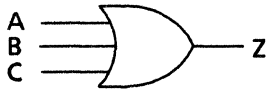
Gate Count: 2
Coding Syntax: Z = OR2 (A,B);
Input loading: (1,1)

OR2P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.5	0.6	0.7	0.7	1.0	1.5
t_{PHL}	1.0	1.0	1.0	1.1	1.2	1.5

Slope1 = 0.0653 Incpt = 0.46
Slope0 = 0.0347 Incpt = 0.94

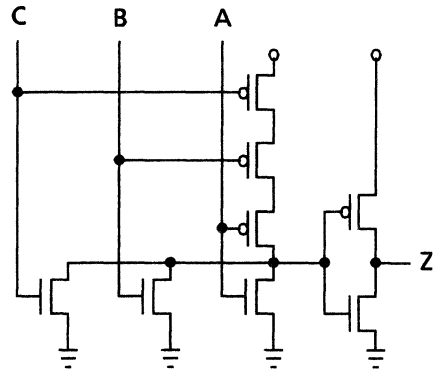
Gate Count: 2
Coding Syntax: Z = OR2P (A,B);
Input loading: (1,1)



LOGIC SYMBOL

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

OR3 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.6	0.8	0.9	1.1	1.6	2.8
t_{PHL}	1.3	1.4	1.5	1.5	1.8	2.4

Slope1 = 0.1443 Incpt = 0.48
Slope0 = 0.0718 Incpt = 1.24

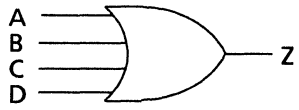
Gate Count: 2
Coding Syntax: Z = OR3 (A,B,C);
Input loading: (1,1,1)

OR3P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.6	0.7	0.8	0.8	1.1	1.6
t_{PHL}	1.4	1.4	1.5	1.5	1.7	2.1

Slope1 = 0.0653 Incpt = 0.56
Slope0 = 0.0477 Incpt = 1.33

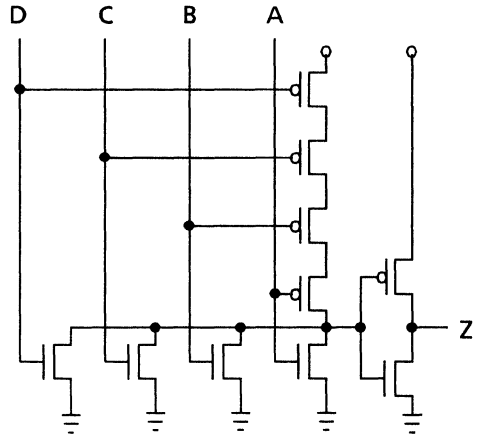
Gate Count: 3
Coding Syntax: Z = OR3P (A,B,C);
Input loading: (1,1,1)



LOGIC SYMBOL

A	B	C	D	Z
0	0	0	0	1
1	x	x	x	0
x	1	x	x	0
x	x	1	x	0
x	x	x	1	0

TRUTH TABLE



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

OR4 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	0.5	0.7	0.8	1.0	1.5	2.7
t_{PHL}	1.4	1.5	1.6	1.7	2.0	2.6

Slope1 = 0.1443 Incpt = 0.38
Slope0 = 0.0788 Incpt = 1.35

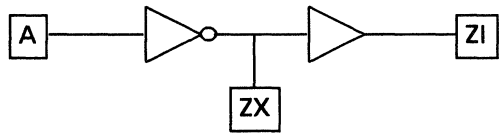
Gate Count: 3
Coding Syntax: Z = OR4 (A,B,C,D);
Input loading: (1,1, 1,1)

OR4P (HIGH DRIVE)

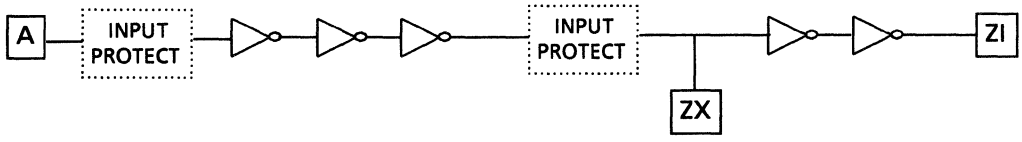
STD LOAD	1	2	3	4	8	16
t_{PLH}	0.6	0.7	0.8	0.8	1.1	1.6
t_{PHL}	1.9	2.0	2.0	2.1	2.3	2.7

Slope1 = 0.0653 Incpt = 0.56
Slope0 = 0.0523 Incpt = 1.87

Gate Count: 3
Coding Syntax: Z = OR4P (A,B,C,D);
Input loading: (1,1, 1,1)



LOGIC SYMBOLC



SCHEMATIC

A	ZX	ZI
0	1	1
1	0	0

TRUTH TABLE

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

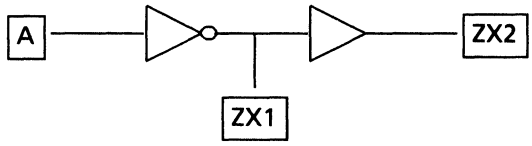
OSCI (A - ZX/ZI)

STD LOAD	15	50	85	100
T*plh* (A - ZX)	4.0	9.1	14.3	16.5
T*phl* (A - ZX)	3.6	8.2	12.7	14.6

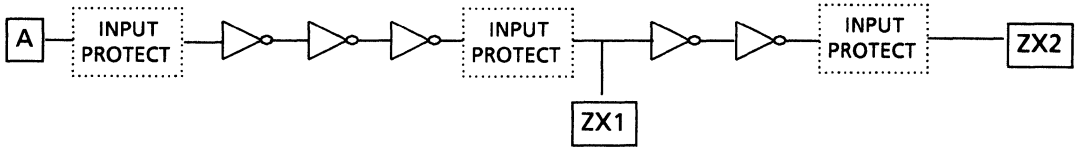
STD LOAD	50	100	200	400	500
T*plh* (A - ZI)	1.8	2.1	2.9	4.4	5.2
T*phl* (A - ZI)	1.9	2.1	2.5	3.3	3.7

ZX Output	Slope 1(ns/pf) =	0.1472	Incpt	=	1.77
	Slope 0(ns/pf) =	0.1294	Incpt	=	1.69
ZI Output	Slope 1(ns/pf) =	0.0076	Incpt	=	1.38
	Slope 0(ns/pf) =	0.0040	Incpt	=	1.70

Coding Syntax: Z = OSCI (A);
Input Loading: (12.5)



LOGIC SYMBOLC



SCHEMATIC

A	ZX1	ZX2
0	1	1
1	0	0

TRUTH TABLE

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

OSCO (A - ZX1/ZX2)

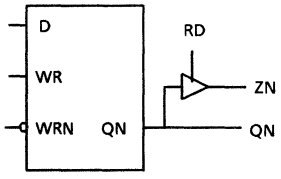
CLOAD	15	50	85	100
T*plh* (A - ZX1) T*phl* (A - ZX1)	3.3 2.9	8.4 7.5	13.6 12.0	15.8 13.9
T*plh* (A - ZX2) T*phl* (A - ZX2)	2.3 2.2	4.5 3.4	6.8 4.6	7.7 5.2

ZX1 Output	Slope 1(ns/pf) =	0.1472	Incpt	=	1.07
	Slope 0(ns/pf) =	0.1294	Incpt	=	0.99
ZX2 Output	Slope 1(ns/pf) =	0.0639	Incpt	=	1.33
	Slope 0(ns/pf) =	0.0350	Incpt	=	1.66

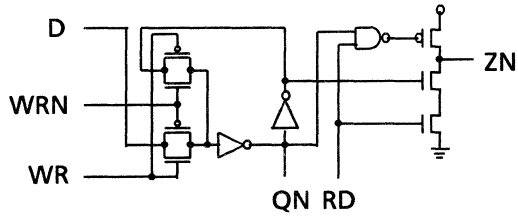
Coding Syntax: Z = OSCO (A);
Input Loading: (12.5)

RAM1 DLATCH, GATED WITH ADDED THREE-STATE OUTPUT RAM1

STANDARD DRIVE



LOGIC SYMBOL



SCHEMATIC

D	WR	WRN	QN
x	0	1	QN
0	1	0	1
1	1	0	0

RD	QN	ZN
0	x	Hi-Z
1	0	0
1	1	1

TRUTH TABLE

RAM1

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(WR-QN)	0.7	0.7	0.8	0.8	1.0	1.5
t_{PHL}(WR-QN)	0.6	0.8	0.9	1.0	1.6	2.8
t_{PLH}(RD-ZN)	0.3	0.4	0.5	0.6	0.9	1.6
t_{PHL}(RD-ZN)	0.5	0.7	0.8	1.0	1.6	2.7

WR-QN Output	Slope 1	=	0.1453	Incpt =	0.46
	Slope 0	=	0.0542	Incpt =	0.61
RD-ZN Output	Slope 1	=	0.1458	Incpt =	0.39
	Slope 0	=	0.0854	Incpt =	0.23

PARAMETER	NS
Tsetup (Input Setup Time)	1.0*
Thold (Input Hold Time)	0.0
Tw (CLOCK) (Width of CLK Pulse)	
CLOCK High Min	1.5
CLOCK Low Min	1.5
Trel RD Release time RD to CLK	0.5

* with zero loading at QN

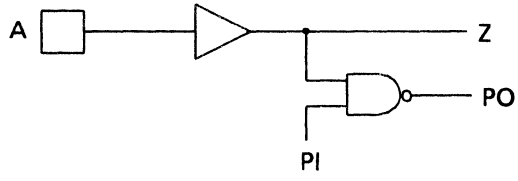
Gate Count: 4
Coding Syntax: Z (ZN, QN) = RAM1 (D,WR,WRN,RD);
Input Loading: (2, 1, 1, 1.5)

SCHMITT CMOS INPUT BUFFER

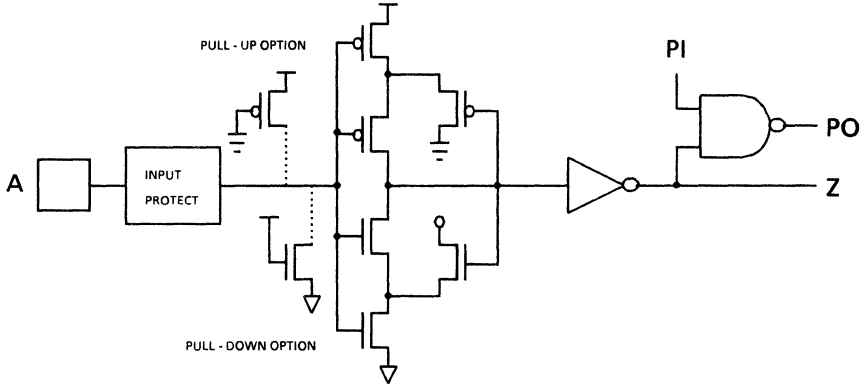
SCHMITC
SCHMITT CMOS INPUT

SCHMITCU
SCHMITT CMOS INPUT
WITH PULL-UP

SCHMITCD
SCHMITT CMOS INPUT
WITH PULL-DOWN



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

SCHMITC / SCHMITCU / SCHMITCD (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH} (Z)	1.4	1.4	1.5	1.5	1.7	2.0
t_{PHL} (Z)	1.7	1.7	1.8	1.8	1.9	2.1

Z Output	Slope 1	=	0.0411	Incpt	=	1.35
	Slope 0	=	0.0265	Incpt	=	1.68

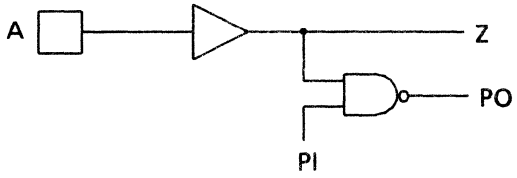
Coding Syntax: (Z,PO) = &SCHMITC (A, PI);
Coding Syntax: (Z,PO) = &SCHMITCU(A, PI);
Coding Syntax: (Z,PO) = &SCHMITCD(A, PI);
Input Loading: (- , 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

INVERTED SCHMITT CMOS INPUT BUFFER

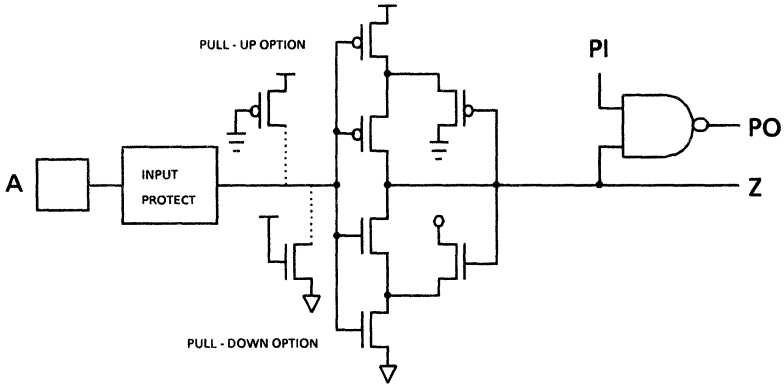
SCHMITCN
INVERTED SCHMITT CMOS INPUT

SCHMITCNU
INVERTED SCHMITT CMOS INPUT WITH PULL-UP

SCHMITCND
INVERTED SCHMITT CMOS INPUT WITH PULL-DOWN



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

SCHMITCN / SCHMITCNU / SCHMITCND (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

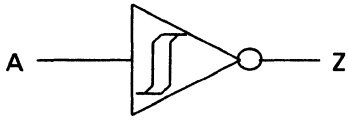
STD LOAD	1	2	3	4	8
t_{PLH} (Z)	1.6	1.8	2.1	2.3	3.2
t_{PHL} (Z)	1.0	1.2	1.2	1.3	1.6

Z Output Slope 1 = 0.2199 Incpt = 1.40
Slope 0 = 0.0669 Incpt = 1.04

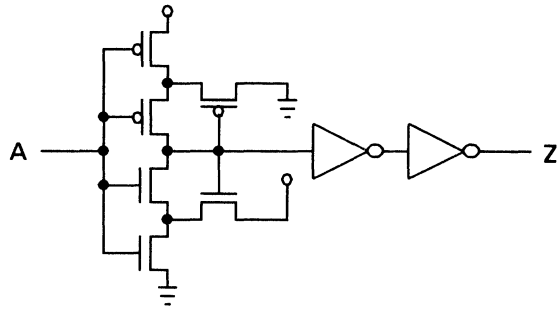
Coding Syntax: (Z,PO) = &SCHMITCN (A, PI);
Coding Syntax: (Z,PO) = &SCHMITCNU (A, PI);
Coding Syntax: (Z,PO) = &SCHMITCND (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

INVERTING SCHMITT TRIGGER IN FOR INTRACHIP WAVE SHAPING

ST / STP



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

ST (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.5	1.7	1.8	2.0	2.5	3.7
t_{PHL}	1.2	1.2	1.3	1.4	1.6	2.0

Slope1 = 0.1443 Incpt = 1.38
Slope0 = 0.0547 Incpt = 1.14

Gate Count: 3
Coding Syntax: Z = ST (A);
Input loading: (2)

STP (HIGH DRIVE)

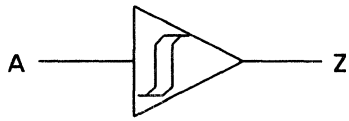
STD LOAD	1	2	3	4	8	16
t_{PLH}	1.5	1.6	1.7	1.7	2.0	2.5
t_{PHL}	1.3	1.3	1.3	1.4	1.5	1.7

Slope1 = 0.0653 Incpt = 1.46
Slope0 = 0.0282 Incpt = 1.26

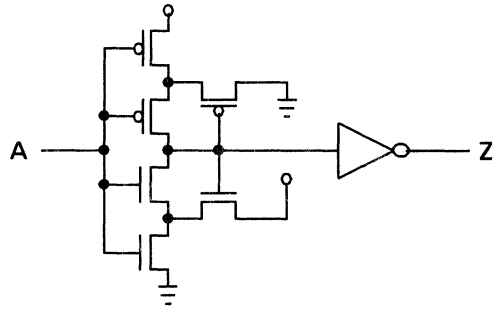
Gate Count: 4
Coding Syntax: Z = STP (A);
Input loading: (2)

NON INVERTING SCHMITT TRIGGER IN FOR INTRACHIP WAVE SHAPING

ST1 / ST1P



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

Delays are nominal [25 deg c, 5v performance (ns)] wirelength not included

ST1 (STANDARD DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.0	1.2	1.3	1.5	2.0	3.2
t_{PHL}	1.3	1.4	1.4	1.5	1.7	2.2

Slope1 = 0.1443 Incpt = 0.88
Slope0 = 0.0589 Incpt = 1.25

Gate Count: 3
Coding Syntax: Z = ST1 (A);
Input loading: (2)

ST1P (HIGH DRIVE)

STD LOAD	1	2	3	4	8	16
t_{PLH}	1.1	1.2	1.3	1.3	1.6	2.1
t_{PHL}	1.5	1.5	1.6	1.6	1.7	2.1

Slope1 = 0.0653 Incpt = 1.06
Slope0 = 0.0396 Incpt = 1.44

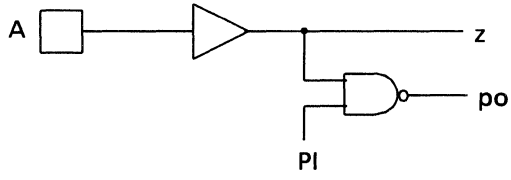
Gate Count: 3
Coding Syntax: Z = ST1P (A);
Input loading: (2)

INVERTED TTL INPUT BUFFER

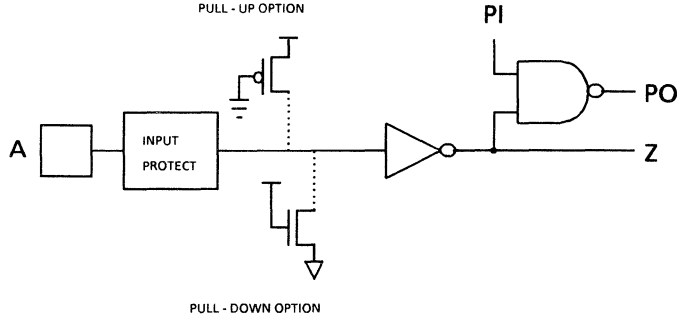
TLCHN
INVERTING TTL INPUT

TLCHNU
INVERTING TTL INPUT
WITH PULL-UP

TLCHND
INVERTING TTL INPUT
WITH PULL-DOWN



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

TLCHN / TLCHNU / TLCHND (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Z)	0.6	0.7	0.7	0.8	1.2	1.9
t_{PHL}(Z)	0.4	0.5	0.5	0.5	0.6	0.9

Z Output Slope 1 = 0.0881 Incpt = 0.48
Slope 0 = 0.0307 Incpt = 0.39

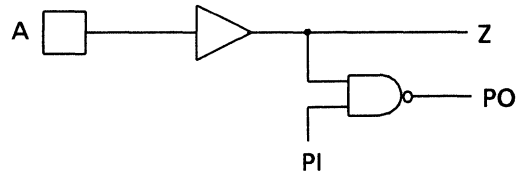
Coding Syntax: (Z,PO) = &TLCHN (A, PI);
Coding Syntax: (Z,PO) = &TLCHNU (A, PI);
Coding Syntax: (Z,PO) = &TLCHND (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 p

TTL INPUT BUFFER

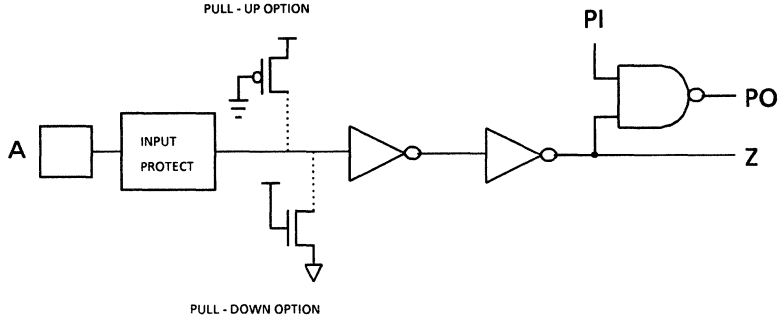
TLCHT
TTL INPUT

TLCHTU
TTL INPUT
WITH PULL-UP

TLCHTD
TTL INPUT
WITH PULL-DOWN



LOGIC SYMBOL



ELECTRICAL SCHEMATIC

TLCHT / TLCHTU / TLCHTD (A-Z)

Delays are Nominal [25 deg c, 5v Performance (ns)] wirelength not included

STD LOAD	1	2	3	4	8	16
t_{PLH}(Z)	0.8	0.8	0.9	0.9	1.1	1.4
t_{PHL}(Z)	0.7	0.7	0.7	0.8	0.8	1.0

Z Output Slope 1 = 0.0411 Incpt = 0.75
Slope 0 = 0.0201 Incpt = 0.67

Coding Syntax: (Z,PO) = &TLCHT (A, PI);
Coding Syntax: (Z,PO) = &TLCHTU (A, PI);
Coding Syntax: (Z,PO) = &TLCHTD (A, PI);
Input Loading: (-, 1)
Input Capacitance: Device(1.5 pf) + pad(1 pf) = 2.5 pf

CHAPTER 3: Macrofunction Catalogue

This chapter contains, in alphabetical and numerical order, model and data sheet for all the macrofunctions available for the LCA10000 Series. Macrofunctions are available to all mainframe users.

3.1 HOW TO READ A MACROFUNCTION MODEL

This section explains how to read a macrofunction model by annotating the CB4C macrofunctin model in Figure 3.1.

1. The **Macrofunciton Name** appears in the upper-left and upper-right corner of the page.

2. The **Macrofunction Function** is given on the same line as the macrofunction's name.

3. The macrofunction **Logic Symbol** is shown on the left hand box, under the header.

4. **Truth Table** is shown in the right hand box, at the top, under the header.

5. The macrofunction network schematic, or **Logic Diagram** illustrating interconnected macrocells, is shown.

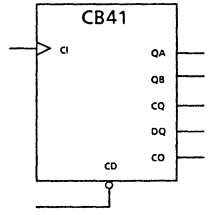
6. The number of **Gates Used** by the macrofunction is shown in the lower left corner.

7. The **Coding Syntax** in TDL format is shown. This particular syntax is used by the LDS System Logic Simulator, not the workstation simulator.

8. **Input Loading** is shown on the last line of the model.

CB41 ① **10 BIT BINARY UP COUNTER FAST, SYNC CLEAR** ② **CB41**

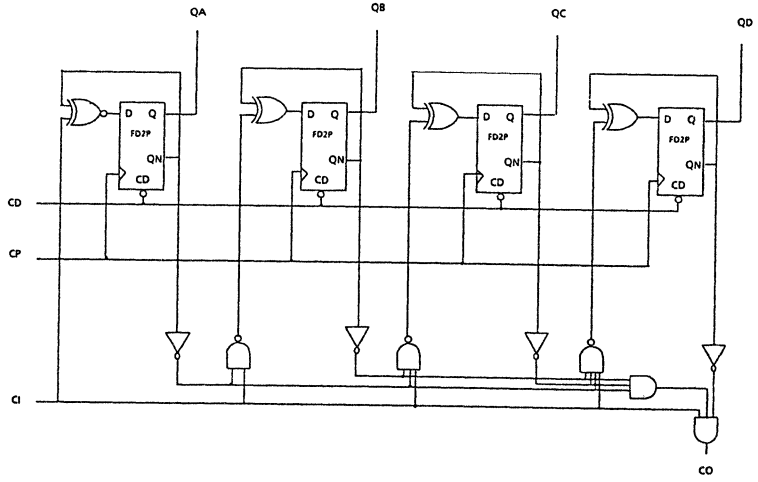
LOGIC SYMBOL ③



OUTPUT ④

	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

LOGIC DIAGRAM ⑤



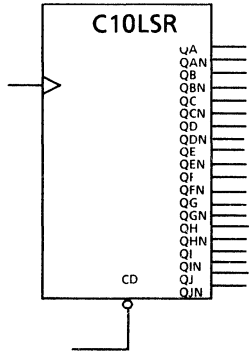
⑥ Gates Used: 62 February, 1987

⑦ Coding syntax: Z (QA, QB QC, QD, CO) = CB41 (CP, CI, CD) $

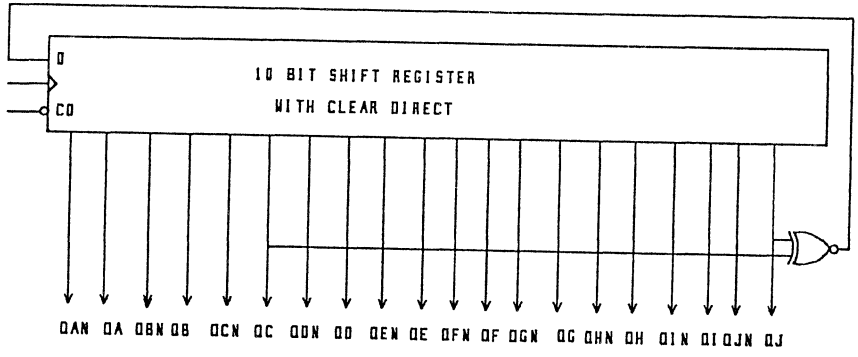
⑧ Input Loading: (4, 5, 4)

C10LSR	10 BIT MODULO 1023 LINEAR FEEDBACK SHIFT REGISTER	C10LSR

LOGIC SYMBOL



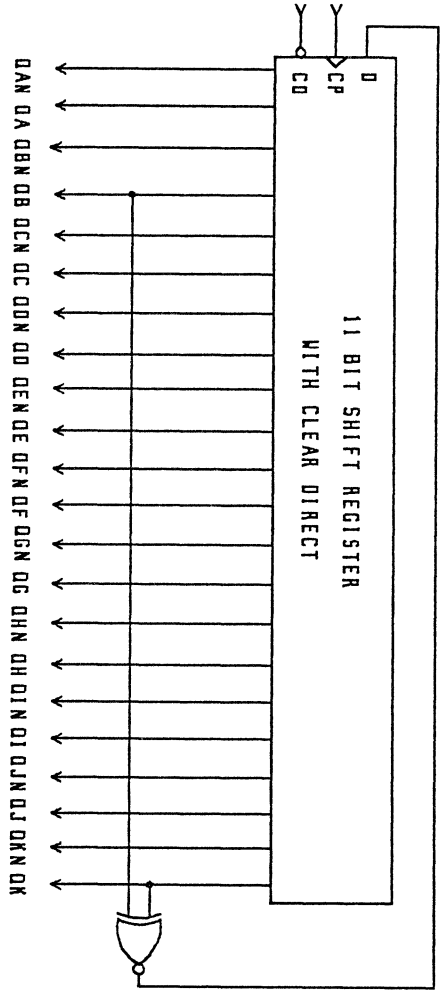
LOGIC DIAGRAM



Gates Used: 23	February, 1987
Loading Syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN,	
QI, QIN, QJ, QJN) C10LSR (CP, CD) $	
Input Loading:	(10 , 20)

C11LSR	11 BIT MODULO 2047 LINEAR FEEDBACK SHIFT REGISTER	C11LSR

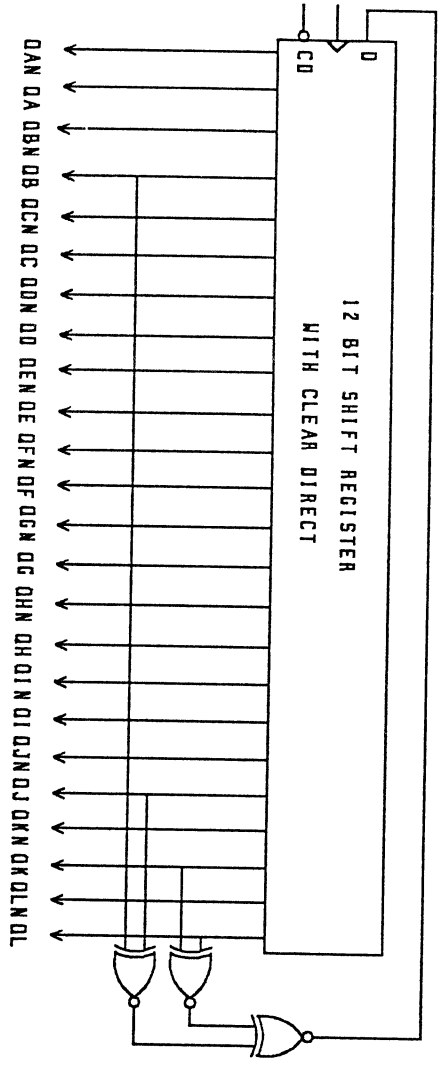
LOGIC DIAGRAM



Gates Used: 102	February, 1987
Loading Syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN,	
QI, QIN, QJ, QJN, QK, QKN) C11LSR (CP, CD) $	
Input Loading: (11 , 22)	

C12LSR	12 BIT MODULO 4095 LINEAR FEEDBACK SHIFT REGISTER	C12LSR

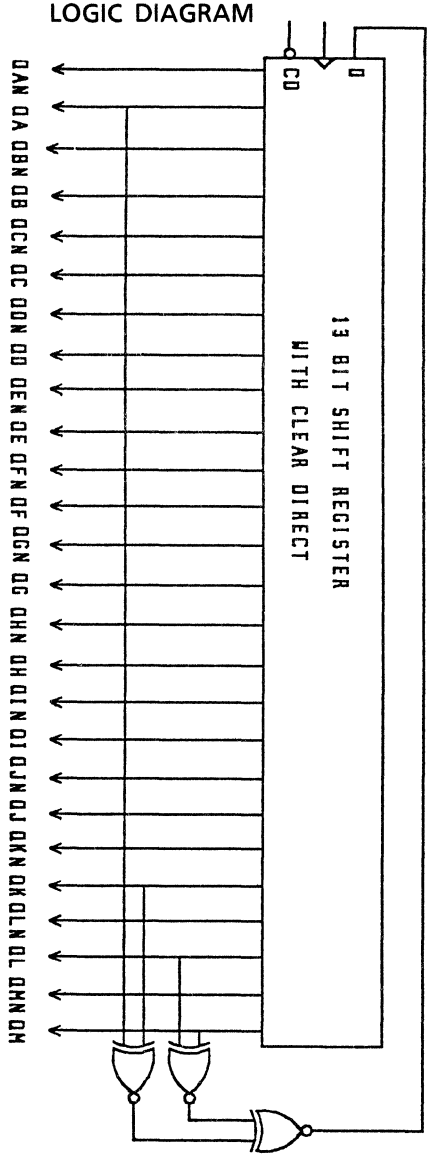
LOGIC DIAGRAM



Gates Used: 117	February, 1987
Loading Syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN, QI, QIN, QJ, QJN, QK, QKN, QL, QLN) C12LSR (CP, CD) $	
Input Loading:	(12 , 24)

C13LSR	13 BIT MODULO 8191 LINEAR FEEDBACK SHIFT REGISTER	C13LSR

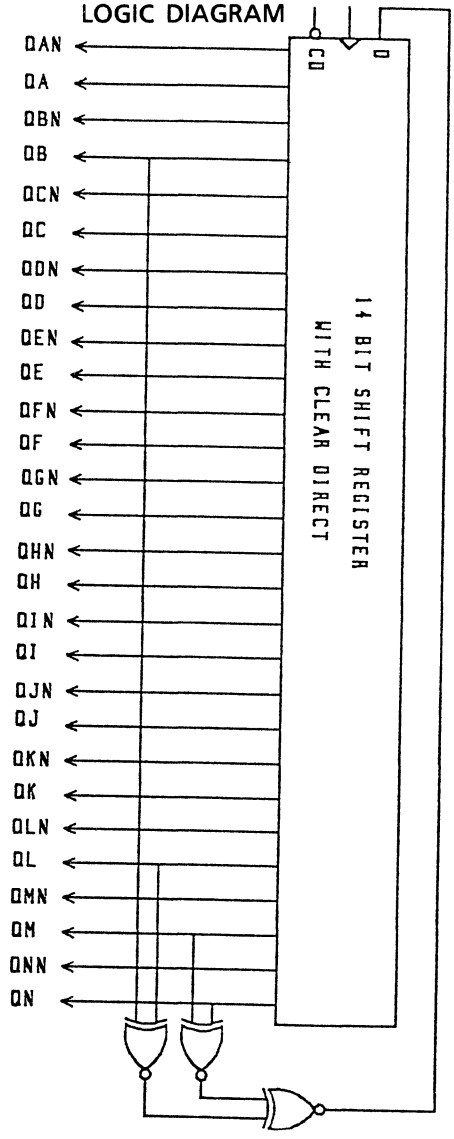
LOGIC DIAGRAM



Gates Used: 126	February, 1987
Loading Syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN,	
QI, QIN, QJ, QJN, QK, QKN, QL, QLN, QM, QMN,) C13LSR (CP, CD) $	
Input Loading:	(13 , 26)

C14LSR	14 BIT MODULO 16383 LINEAR FEEDBACK SHIFT REGISTER	C14LSR

LOGIC DIAGRAM



Gates Used: 135 February, 1987

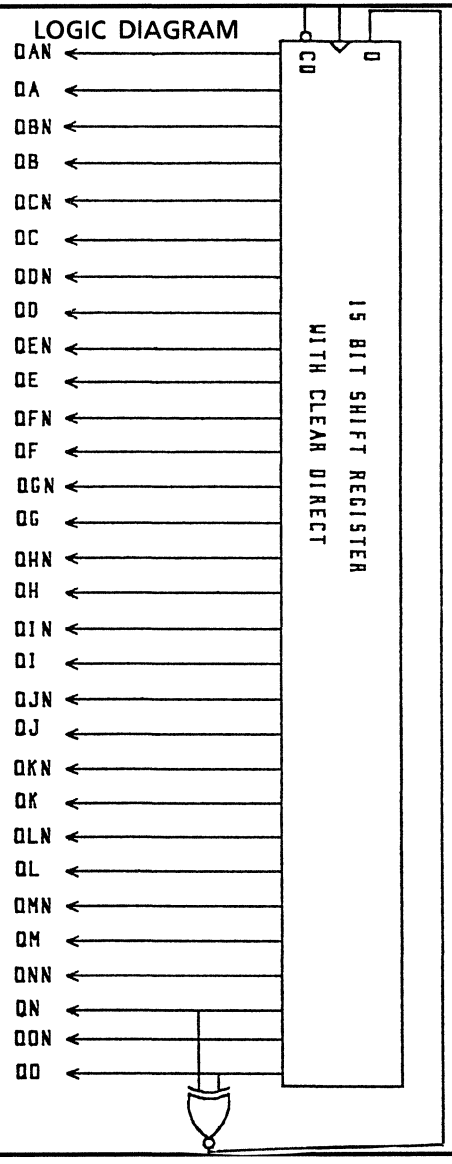
Coding Syntax: Z (QA, QAN, QB, QBN, QC, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN, QI, QIN, QJ, QJN, QL, QLN, QN, QNN)

= C14LSR (CP, CD) $

Input Loading: (14, 28)

C15LSR	15 BIT MODULO 32767 LINEAR FEEDBACK SHIFT REGISTER	C15LSR

LOGIC DIAGRAM



Gates Used: 138 February, 1987

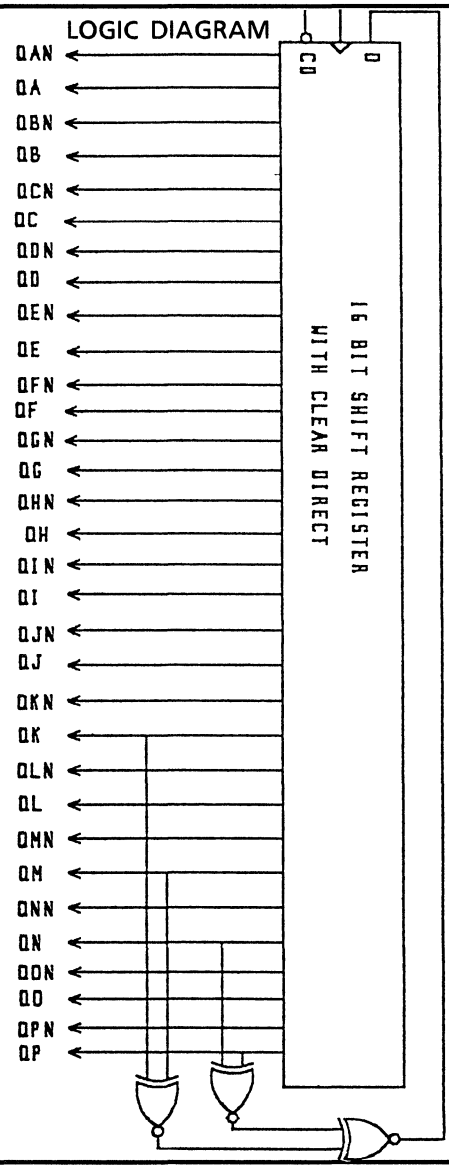
Coding Syntax: Z (QA, QAN, QB, QBN, QC, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN, QI, QIN, QJ, QJN, QL, QLN, QN, QNN, QO, QON)

= C15LSR (CP, CD) $

Input Loading: (15, 30)

C16LSR	16 BIT MODULO 65535 LINEAR FEEDBACK SHIFT REGISTER	C16LSR

LOGIC DIAGRAM



Gates Used: 153 February, 1987

Coding Syntax: Z (QA, QAN, QB, QBN, QC, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN, QI, QIN,

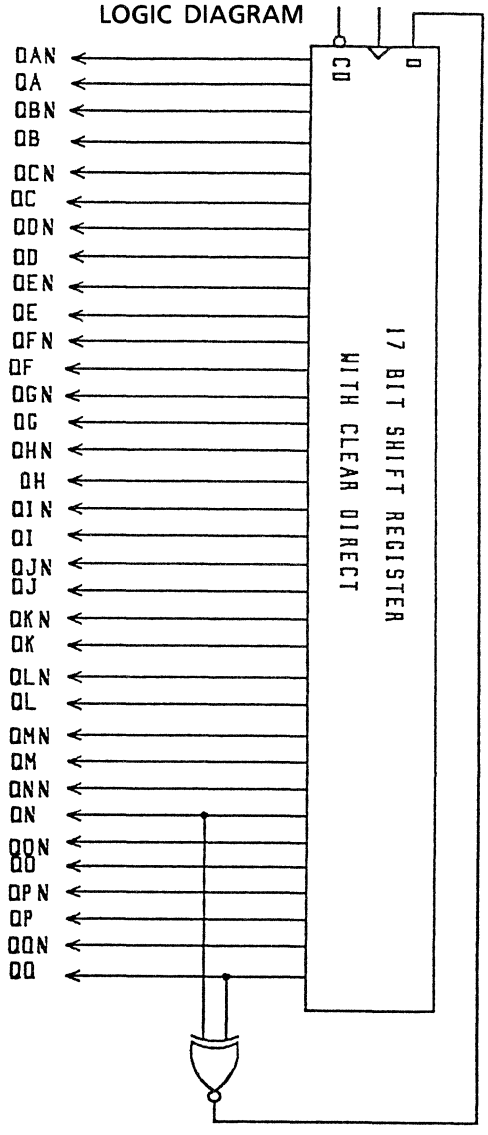
QJ, QJN, QL, QLN, QN, QNN, QO, QON, QPM, QPN)

= C16LSR (CP, CD) $

Input Loading: (16, 32)

C17LSR	17 BIT MODULO 131071 LINEAR FEEDBACK SHIFT REGISTER	C17LSR

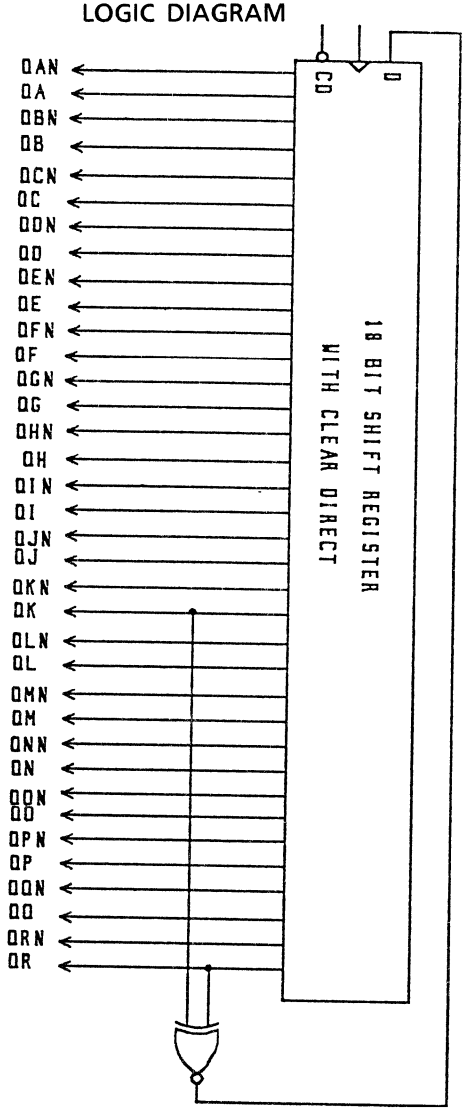
LOGIC DIAGRAM



Gates Used: 156	February, 1987
Coding Syntax: Z (QA, QAN, QB, QBN, QC, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN, QI, QIN,	
QJ, QJN, QL, QLN, QN, QNN, QO, QON, QPM,QPN, QQ, QQN)	
= C17LSR (CP, CD) $	
Input Loading: (17, 34)	

C18LSR	18 BIT MODULO 262143 LINEAR FEEDBACK SHIFT REGISTER	C18LSR

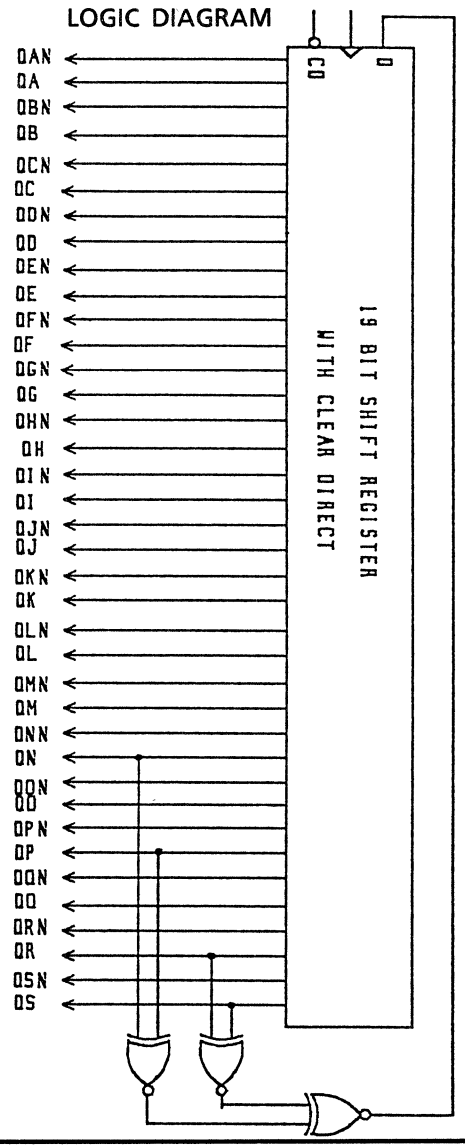
LOGIC DIAGRAM



Gates Used: 165 February, 1987
Coding Syntax: Z (QA, QAN, QB, QBN, QC, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN, QI, QIN,
QJ, QJN, QL, QLN, QN, QNN, QQ,QQN, QPM,QPN, QQ, QQN,QR, QRN)
= C18LSR (CP, CD) $
Input Loading: (18, 36)

C19LSR	19 BIT MODULO 524287 LINEAR FEEDBACK SHIFT REGISTER	C19LSR

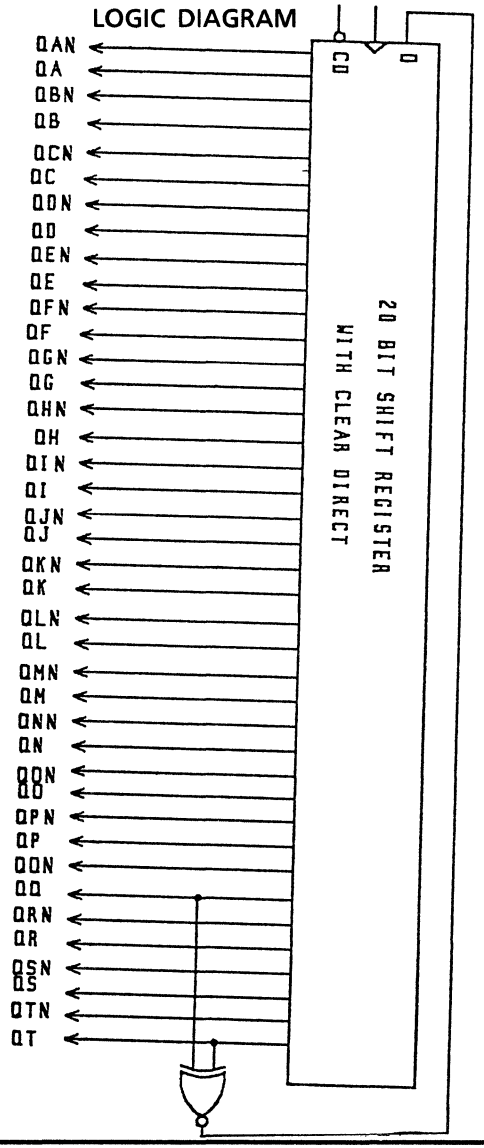
LOGIC DIAGRAM



Gates Used: 180	February, 1987
Coding Syntax: Z (QA, QAN, QB, QBN, QC, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN, QI, QIN,	
QJ, QJN, QL, QLN, QN, QNN, QO,QON, QPM,QPN, QQ, QQN,QR, QRN, QS, QSN)	
= C19LSR (CP, CD) $	
Input Loading: (19, 38)	

C20LSR	20 BIT MODULO 1048575 LINEAR FEEDBACK SHIFT REGISTER	C20LSR

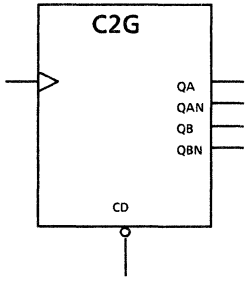
LOGIC DIAGRAM



Gates Used: 183	February, 1987
Coding Syntax: Z (QA, QAN, QB, QBN, QC, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN, QI, QIN,	
QJ, QJN, QL, QLN, QN, QNN, QO, QON, QPM, QPN, QQ, QQN, QR, QRN, QS, QSN, QT, QTN)	
= C20LSR (CP, CD) $	
Input Loading: (20, 40)	

C2G — MODULO 4 GRAY COUNTER CLEAR DIRECT, PRESCALED — C2G

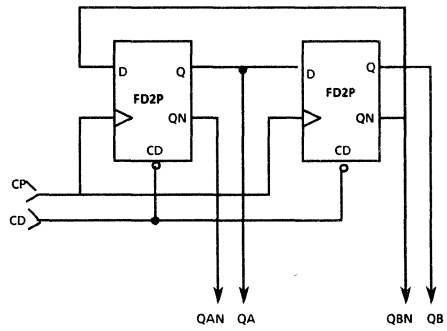
LOGIC SYMBOL



TRUTH TABLE

OUTPUT	
QA	QB
0	0
1	0
1	1
0	1

LOGIC DIAGRAM



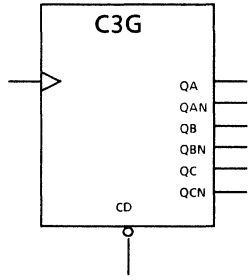
Gates Used: 20 — February, 1987

Coding syntax: Z (QA, QB) = C2G (CP, CD) $

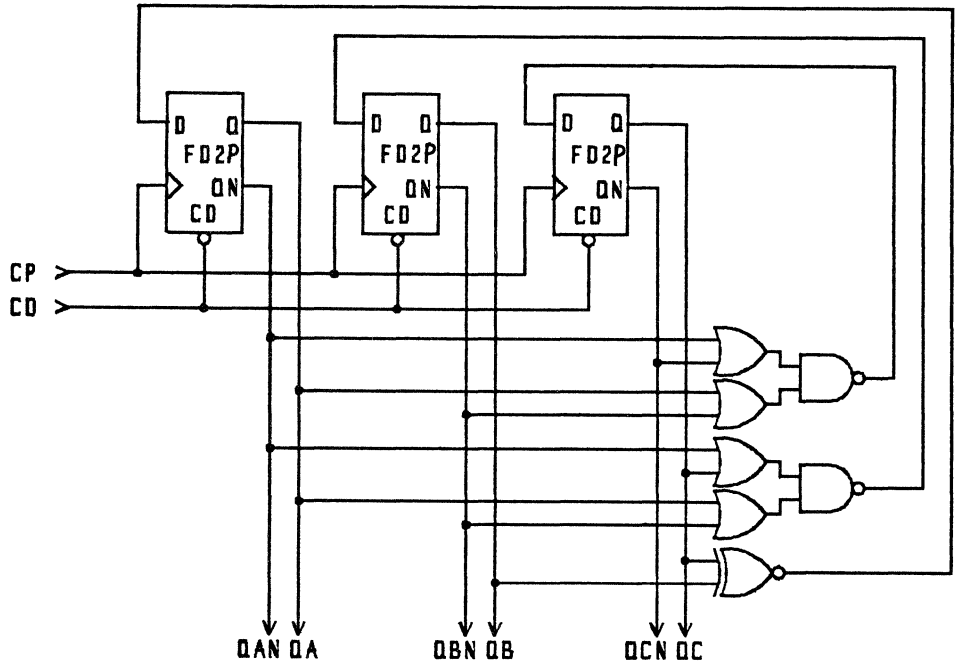
Input Loading: (2, 4)

C3G	MODULO 8 GRAY COUNTER CLEAR DIRECT, PRESCALED	C3G

LOGIC SYMBOL



LOGIC DIAGRAM



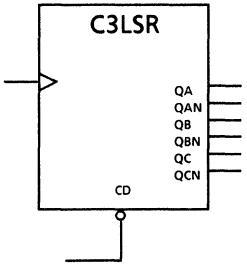
Gates Used: 34 February, 1987

Coding syntax: Z (QA, QB, QC, QD) = C3G (CP, CD) $

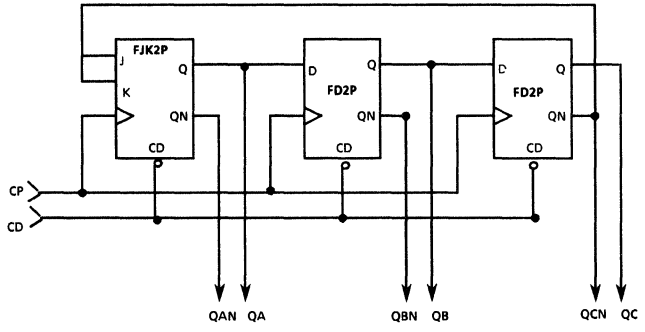
Input Loading: (3, 6)

C3LSR	3 BIT MODULO 7 LINEAR FEEDBACK SHIFT REGISTER	C3LSR

LOGIC SYMBOL



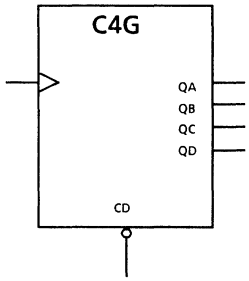
LOGIC DIAGRAM



Gates Used: 29	February, 1987
Loading Syntax: Z (QA, QAN, QB, QBN, QC, QCN)	
C3LSR (CP, CD) $	
Input Loading: (3 , 6)	

C4G — MODULO 16 GRAY COUNTER CLEAR DIRECT, PRESCALED — C4G

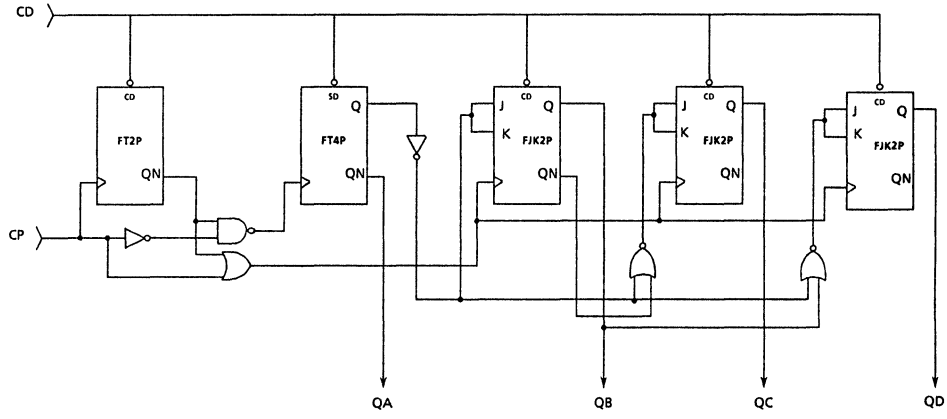
LOGIC SYMBOL



TRUTH TABLE

QA	QB	QC	QD
0	0	0	0
1	0	0	0
1	1	0	0
0	1	0	0
0	1	1	0
1	1	1	0
1	0	1	0
0	0	1	0
0	0	1	1
1	0	1	1
1	1	1	1
0	1	1	1
0	1	0	1
1	1	0	1
1	0	0	1
0	0	0	1

LOGIC DIAGRAM



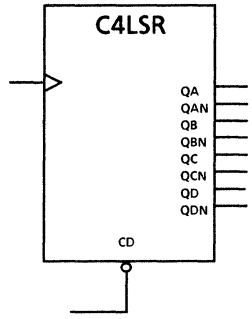
Gates Used: 56 — February, 1987

Coding syntax: Z (QA, QB, QC, QD) = C4G (CP, CD) $

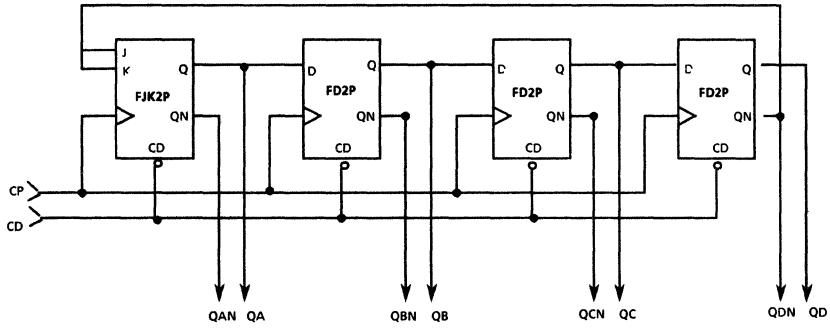
Input Loading: (4.5, 12)

C4LSR	4 BIT MODULO 15 LINEAR FEEDBACK SHIFT REGISTER	C4LSR

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 38 February, 1987

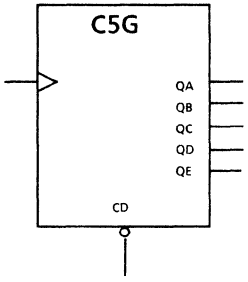
Loading Syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN)

C4LSR (CP, CD) $

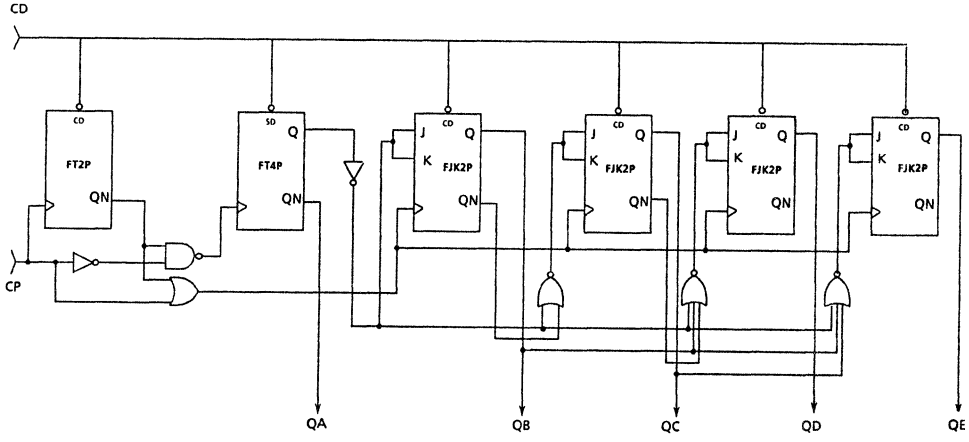
Input Loading: (4 , 8)

C5G	MODULO 32 GRAY COUNTER CLEAR DIRECT, PRESCALED	C5G

LOGIC SYMBOL



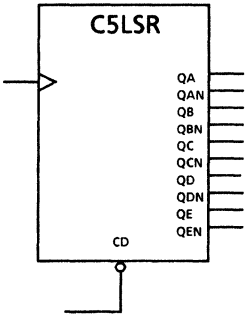
LOGIC DIAGRAM



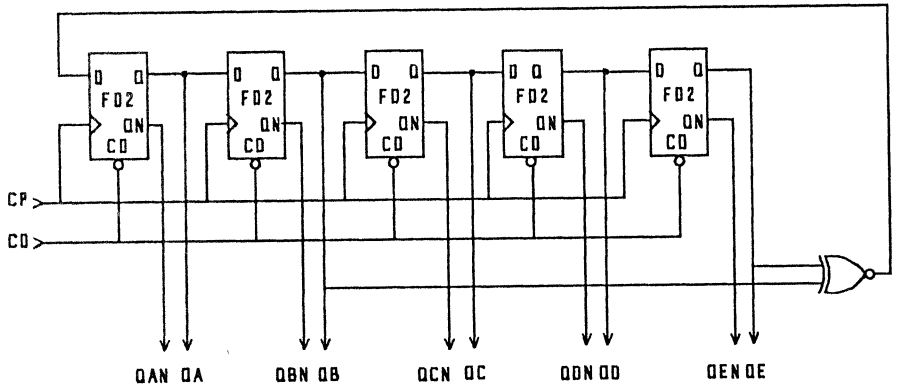
Gates Used: 70	February, 1987
Coding syntax: Z (QA, QB, QC, QD, QE) = C5G (CP, CD) $	
Input Loading: (4.5, 12)	

C5LSR	5 BIT MODULO 31 LINEAR FEEDBACK SHIFT REGISTER	C5LSR

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 48 February, 1987

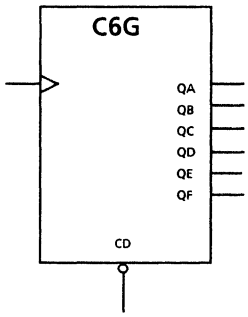
Loading Syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN)

C5LSR (CP, CD) $

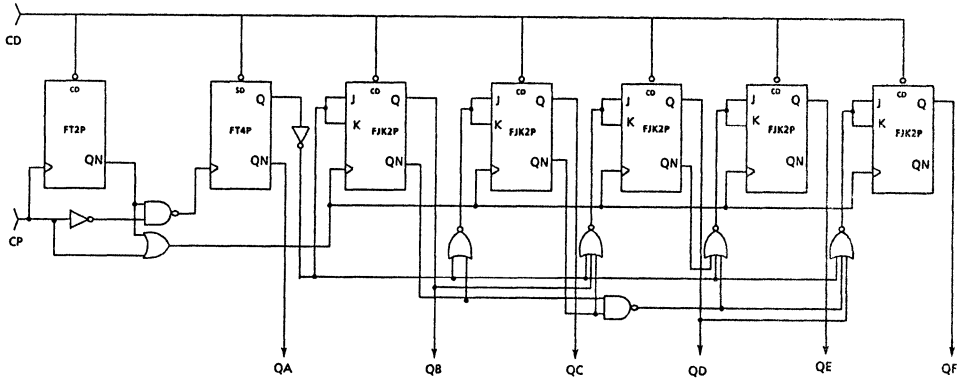
Input Loading: (5 , 10)

C6G	MODULO 64 GRAY COUNTER CLEAR DIRECT, PRESCALED	C6G

LOGIC SYMBOL



LOGIC DIAGRAM



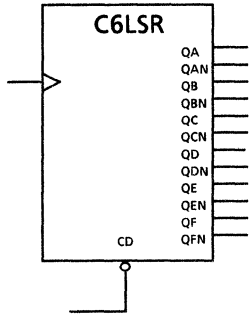
Gates Used: 84 February, 1987

Coding syntax: Z (QA, QB, QC, QD, QE, QF) = C6G (CP, CD) $

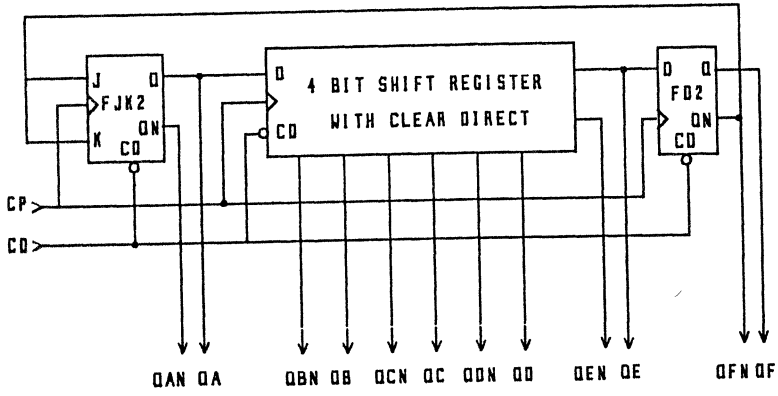
Input Loading: (4.5, 14)

C6LSR	6 BIT MODULO 63 LINEAR FEEDBACK SHIFT REGISTER	C6LSR

LOGIC SYMBOL



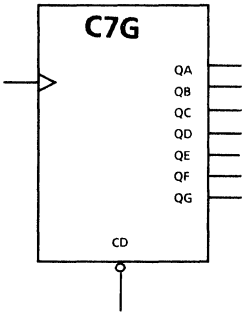
LOGIC DIAGRAM



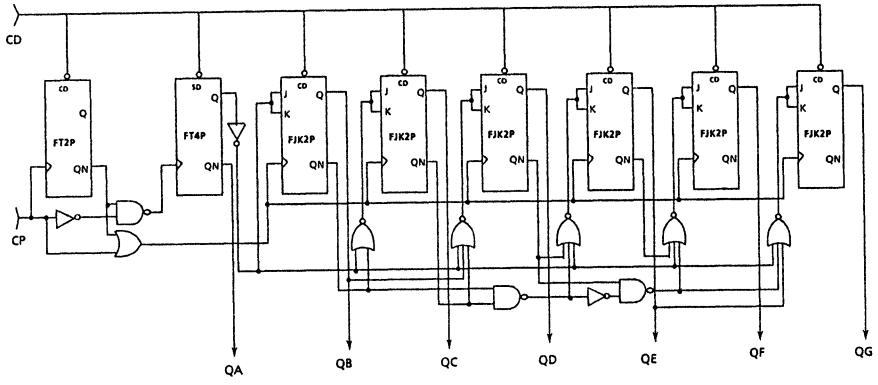
Gates Used: 56	February, 1987
Loading Syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF QFN)	
C6LSR (CP, CD) $	
Input Loading: (6 , 12)	

C7G	MODULO 128 GRAY COUNTER CLEAR DIRECT, PRESCALED	C7G

LOGIC SYMBOL



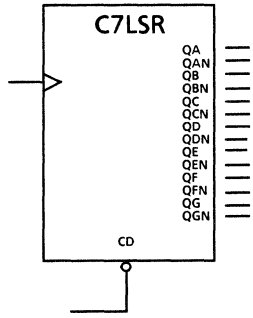
LOGIC DIAGRAM



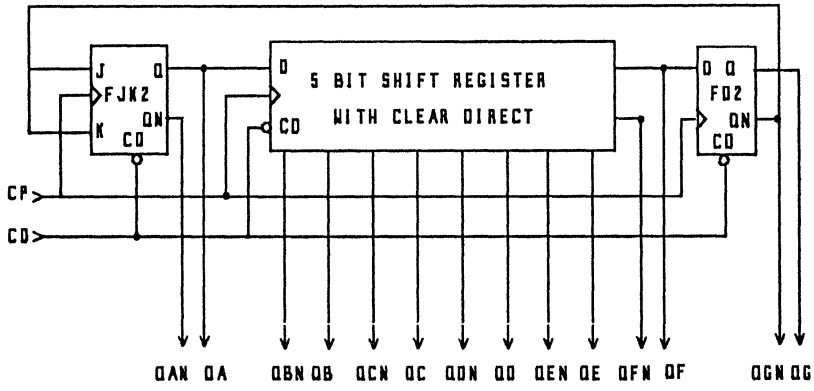
Gates Used: 100	February, 1987
Coding syntax: Z (QA, QB, QC, QD, QE, QF, QG) = C7G (CP, CD) $	
Input Loading:	(4.5, 18)

C7LSR	7 BIT MODULO 127 LINEAR FEEDBACK SHIFT REGISTER	C7LSR

LOGIC SYMBOL



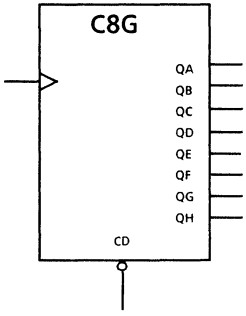
LOGIC DIAGRAM



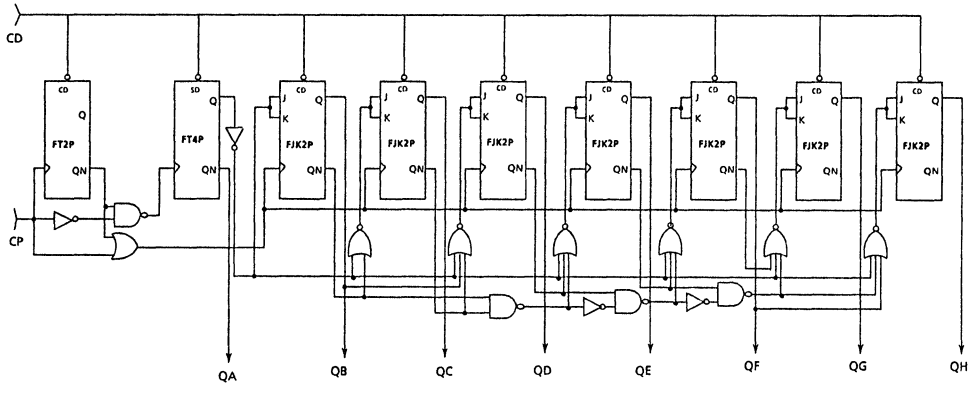
Gates Used: 65	February, 1987
Loading Syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN)	
C7LSR (CP, CD) $	
Input Loading: (7 , 14)	

C8G — MODULO 256 GRAY COUNTER CLEAR DIRECT, PRESCALED — C8G

LOGIC SYMBOL



LOGIC DIAGRAM



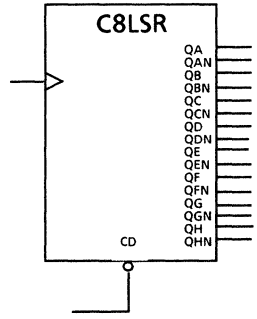
Gates Used: 115 — February, 1987

Coding syntax: Z (QA, QB, QC, QD, QE, QF, QG, QH) = C8G (CP, CD) $

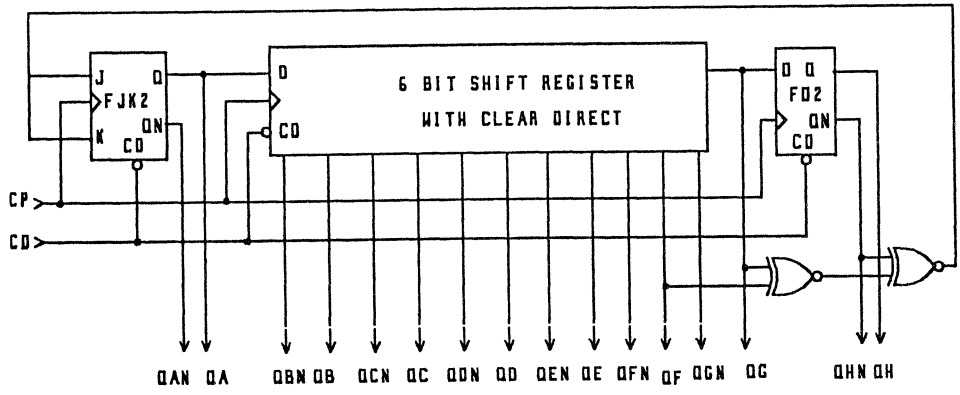
Input Loading: (4.5, 18)

C8LSR	8 BIT MODULO 255 LINEAR FEEDBACK SHIFT REGISTER	C8LSR

LOGIC SYMBOL



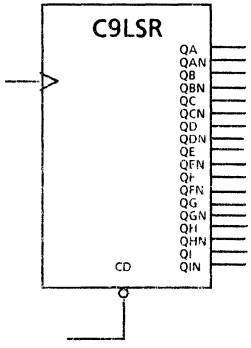
LOGIC DIAGRAM



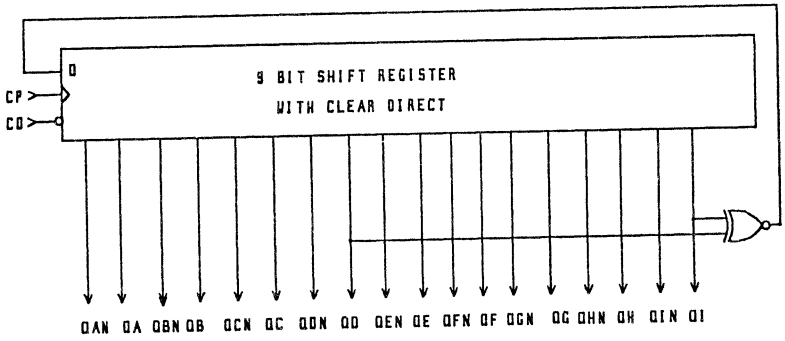
Gates Used: 80	February, 1987
Loading Syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN,	
C8LSR (CP, CD) $	
Input Loading: (8 , 16)	

C9LSR	9 BIT MODULO 511 LINEAR FEEDBACK SHIFT REGISTER	C9LSR

LOGIC SYMBOL



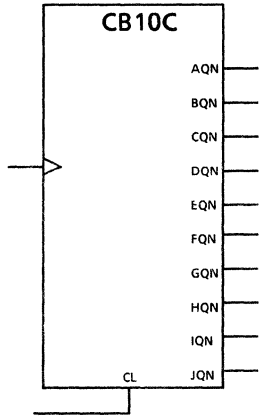
LOGIC DIAGRAM



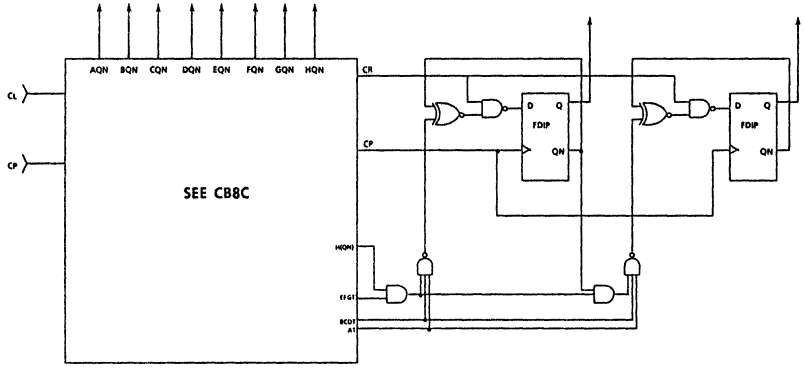
Gates Used: 84	February, 1987
Loading Syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN,	
QI, QIN) C9LSR (CP, CD) $	
Input Loading: (9 , 18)	

CB10C	10 BIT BINARY UP COUNTER FAST, SYNC CLEAR	CB10C

LOGIC SYMBOL



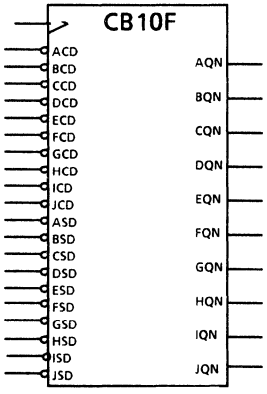
LOGIC DIAGRAM



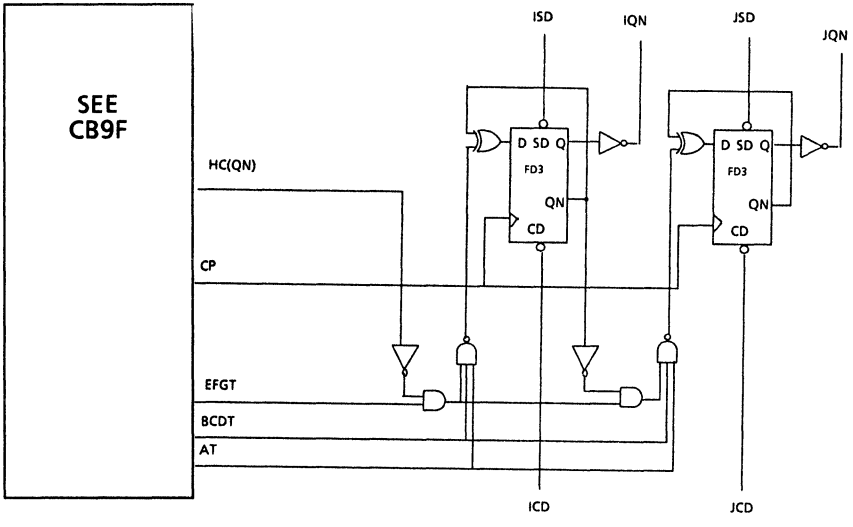
Gates Used: 147	February, 1987
Coding syntax: Z (AQN, BQN, CQN, DQN, EQN, FQN, GQN, HQN, IQN, JQN) = CB10C (CL, CP) $	
Input Loading:	(3, 10)

CB10F	10 BIT BINARY UP COUNTER FAST, INDIVIDUAL CD SD	CB10F

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 163 February, 1987

Coding syntax: Z (AQN, BQN, CQN, DQN, EQN, FQN, GQN, HQN, IQN, JQN) =

CB10F (CP, ACD, BCD, CCD, DCD, ECD, FCD, GCD, HCD, ICD, JCD, ASD, BSD, CSD, DSD, ESD,

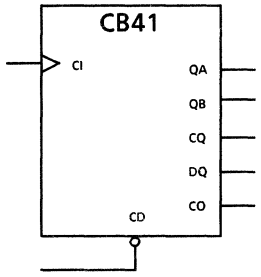
Input Loading: (8, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2,

FSD, GSD, HSD, ISD, JSD) $

2, 2, 2, 2, 2)

CB41 — 10 BIT BINARY UP COUNTER FAST, SYNC CLEAR — CB41

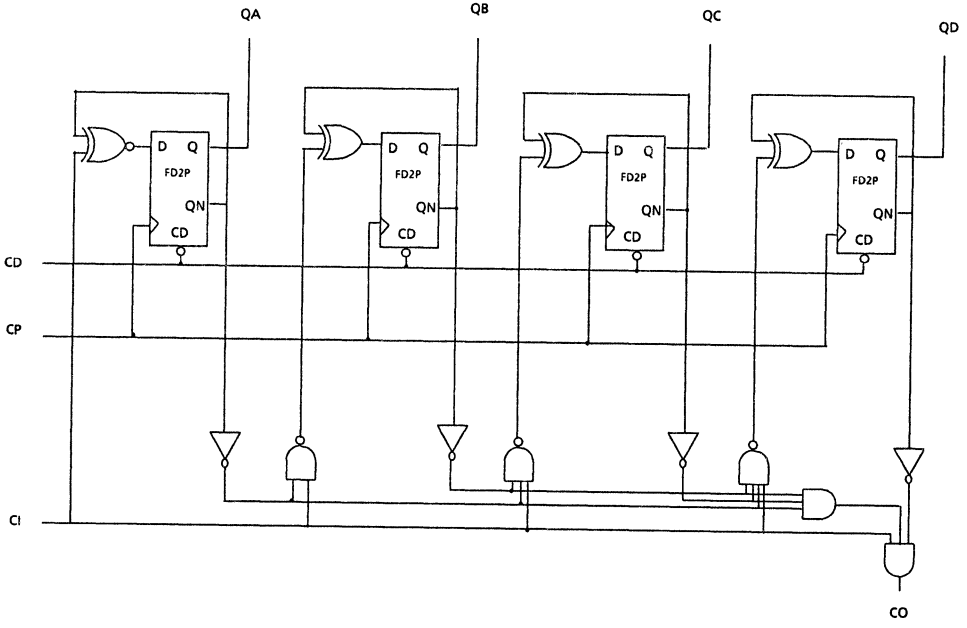
LOGIC SYMBOL



OUTPUT

	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

LOGIC DIAGRAM



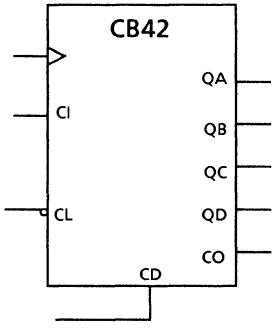
Gates Used: 62 — February, 1987

Coding syntax: Z (QA, QB QC, QD, CO) = CB41 (CP, CI, CD) $

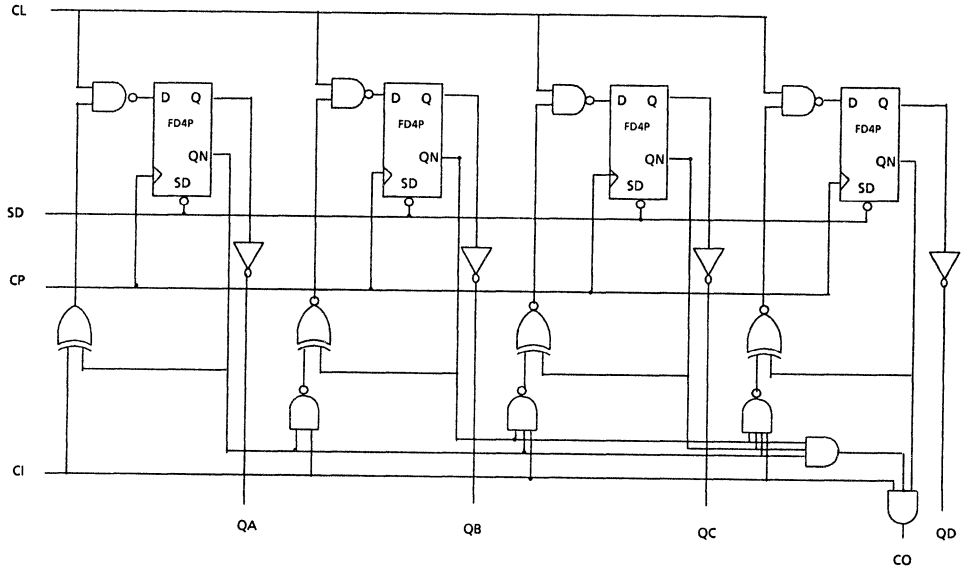
Input Loading: (4, 5, 4)

CB42	4 BIT BINARY UP COUNTER EXPANDABLE ENABLE SYNC CLEAR, CD	CB42

LOGIC SYMBOL



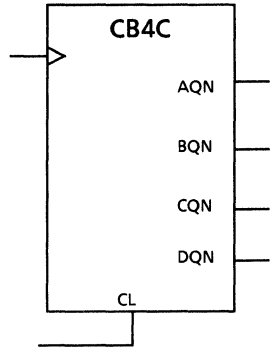
LOGIC DIAGRAM



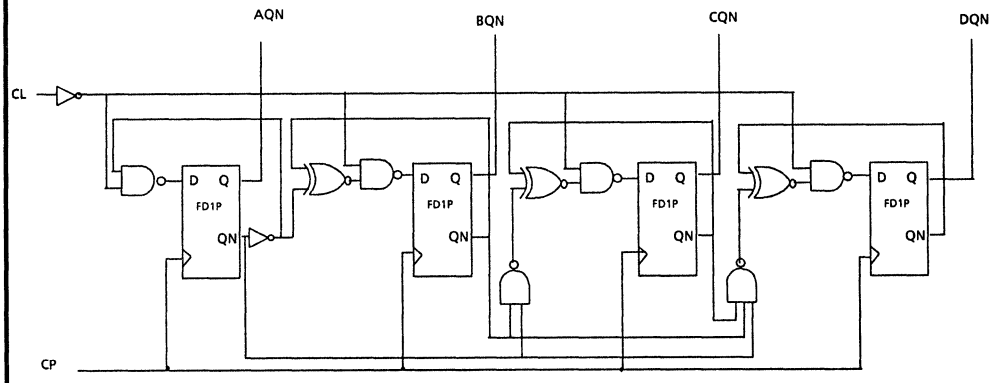
Gates Used: 62	February, 1987
Coding syntax: Z (QA, QB, QC, QD, CO) = CB42	(CP,CI, CL, CD) $
Input Loading:	(4, 6, 4, 8)

CB4C	4 BIT BINARY UP COUNTER FAST, SYNC CLEAR	CB4C

LOGIC SYMBOL



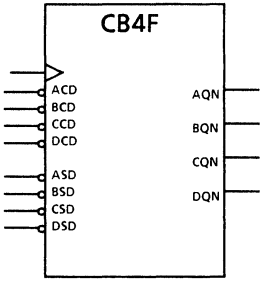
LOGIC DIAGRAM



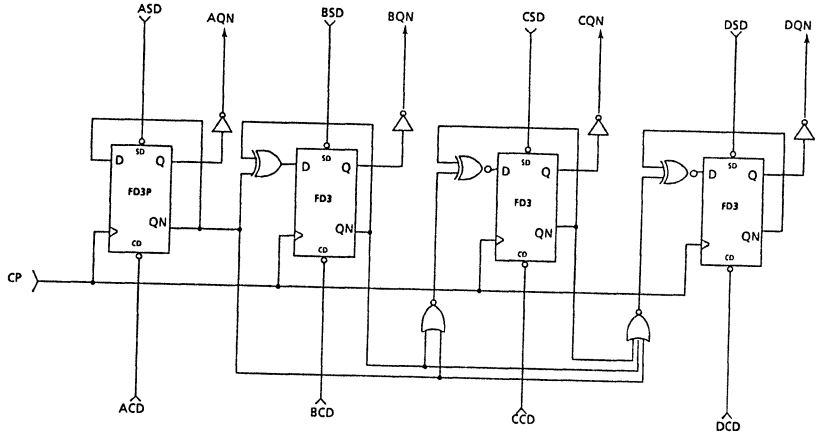
Gates Used: 50	February, 1987
Coding syntax: Z (AQN, BQN, CQN, DQN) = CB4C	(CL, CP) $
Input Loading:	(2, 4)

CB4F	4 BIT BINARY UP COUNTER FAST, INDIVIDUAL CD SD	CB4F

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 53 February, 1987

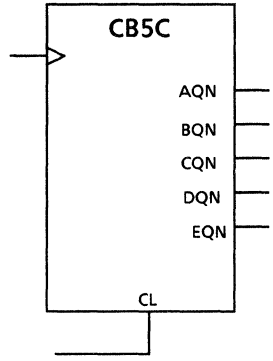
Coding syntax: Z (AQN, BQN, CQN, DQN) =

CB4F (CP, ACD, BCD, CCD, DCD, ASD, BSD, CSD, DSD) $

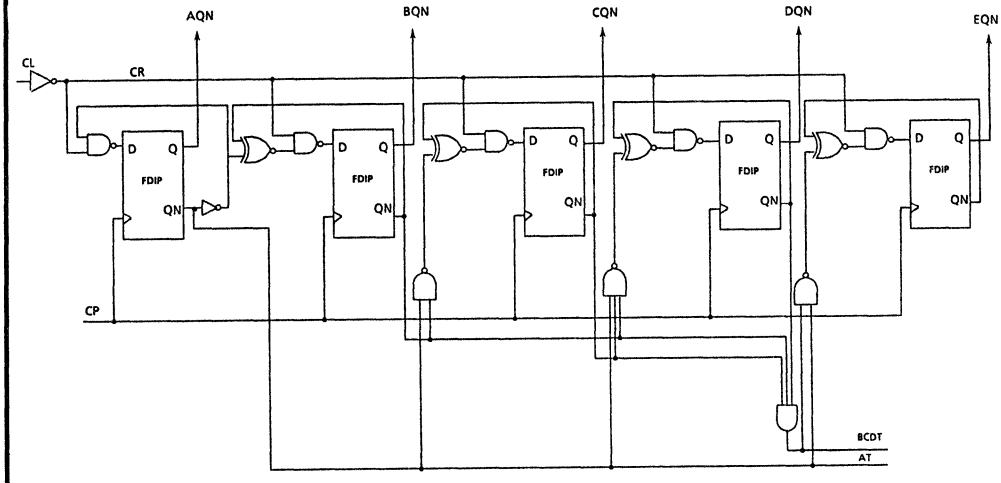
Input Loading: (4, 2, 2, 2, 2, 2, 2, 2, 2)

CB5C	5 BIT BINARY UP COUNTER FAST, SYNC CLEAR	CB5C

LOGIC SYMBOL



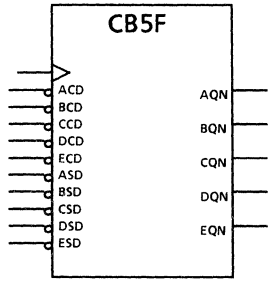
LOGIC DIAGRAM



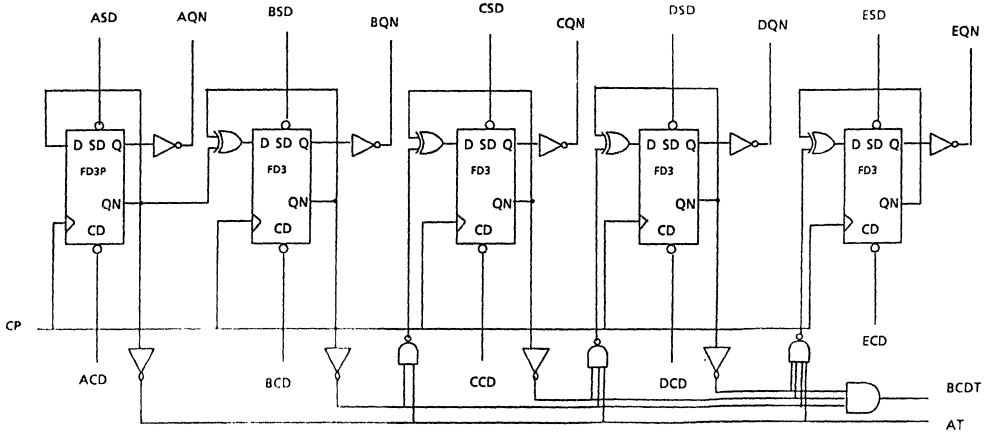
Gates Used: 64	February, 1987
Coding syntax: Z (AQN, BQN, CQN, DQN, EQN) = CB5C	(CL, CP) $
Input Loading:	(2, 5)

CB5F	5 BIT BINARY UP COUNTER FAST, INDIVIDUAL CD SD	CB5F

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 72 February, 1987

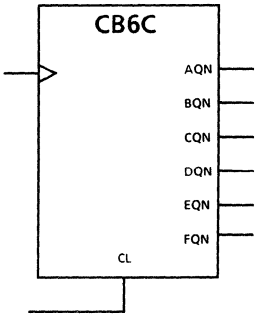
Coding syntax: Z (AQN, BQN, CQN, DQN, EQN) =

CB5F (CP, ACD, BCD, CCD, DCD, ECD, ASD, BSD, CSD, DSD, ESD) $

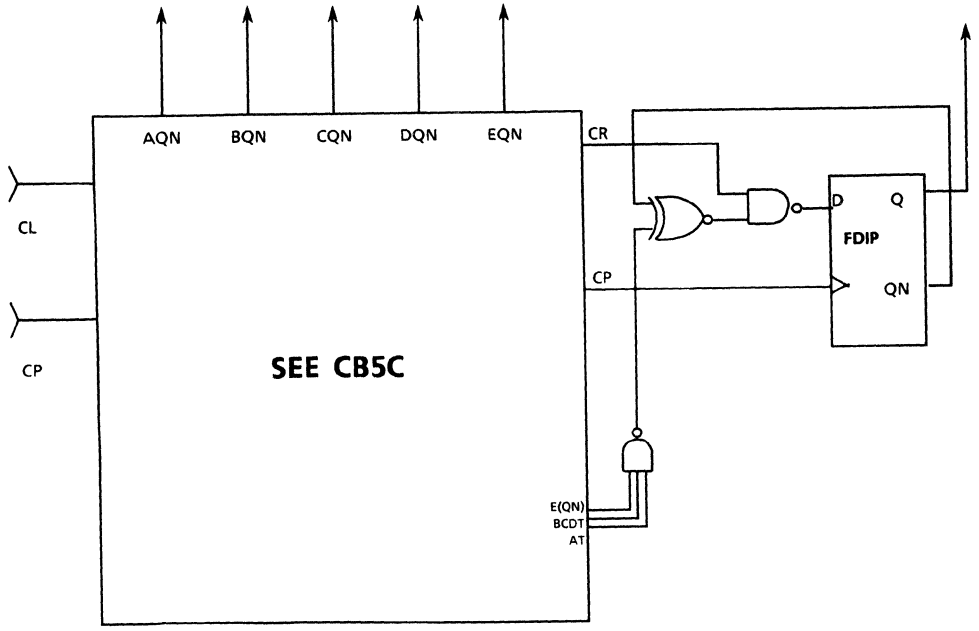
Input Loading: (5, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2)

CB6C	6 BIT BINARY UP COUNTER FAST, SYNC CLEAR	CB6C

LOGIC SYMBOL



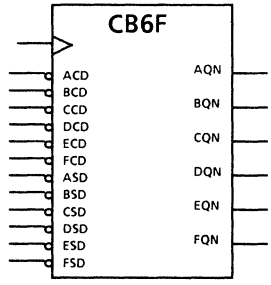
LOGIC DIAGRAM



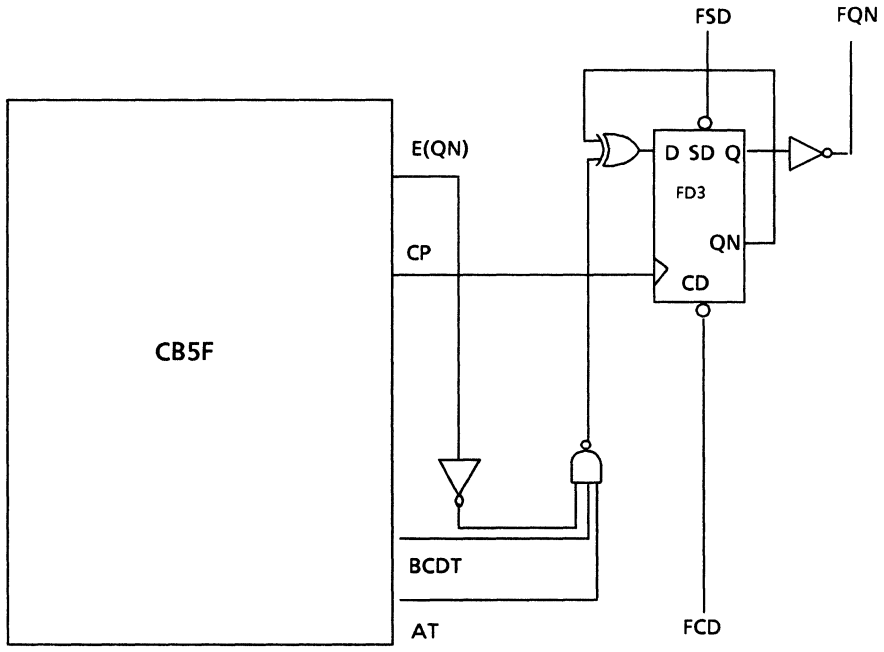
Gates Used: 78		February, 1987
Coding syntax: Z (AQN, BQN, CQN, DQN, EQN, FQN) =	CB6C	(CL, CP) $
Input Loading:		(3, 6)

CB6F	6 BIT BINARY UP COUNTER FAST, INDIVIDUAL CD SD	CB6F

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 90 February, 1987

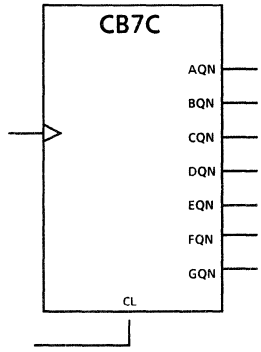
Coding syntax: Z (AQN, BQN, CQN, DQN, EQN, FQN) =

CB6F(CP, ACD, BCD, CCD, DCD, ECD, FCD, ASD, BSD, CSD, DSD, ESD, FSD) $

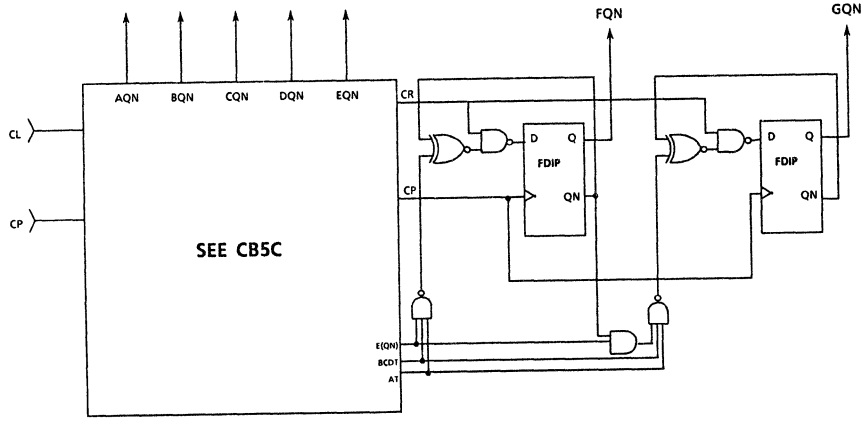
Input Loading: (6, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2)

CB7C	7 BIT BINARY UP COUNTER FAST, SYNC CLEAR	CB7C

LOGIC SYMBOL



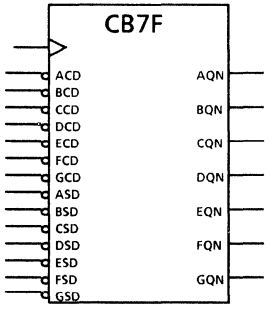
LOGIC DIAGRAM



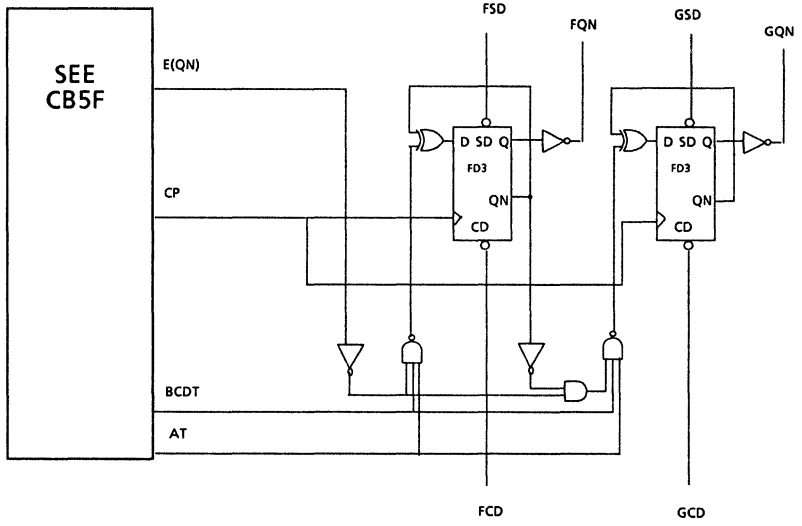
Gates Used: 96	February, 1987
Coding syntax: Z (AQN, BQN, CQN, DQN, EQN, FQN, GQN) = CB7C	(CL, CP) $
Input Loading:	(3, 7)

CB7F	7 BIT BINARY UP COUNTER FAST, INDIVIDUAL CD SD	CB7F

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 108 February, 1987

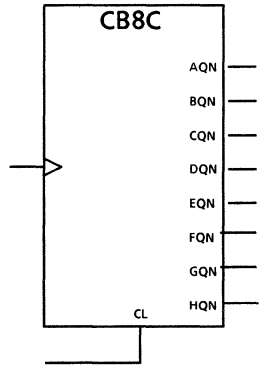
Coding syntax: Z (AQN, BQN, CQN, DQN, EQN, FQN, GQN) =

CB7F(CP, ACD, BCD, CCD, DCD, ECD, FCD, GCD, ASD, BSD, CSD, DSD, ESD, FSD, GSD) $

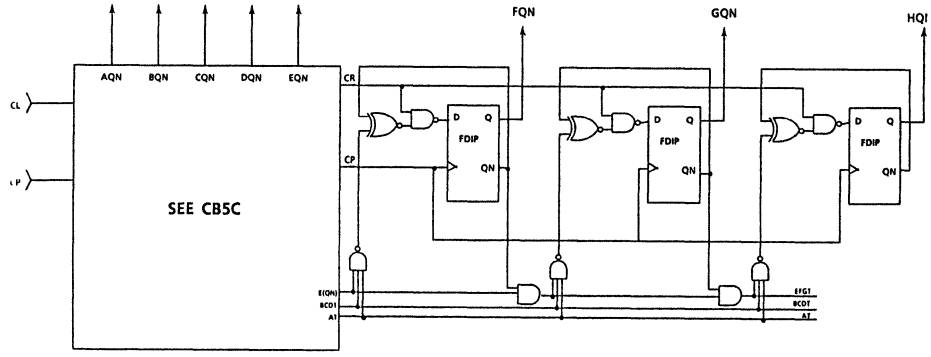
Input Loading: (7, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2)

CB8C	8 BIT BINARY UP COUNTER FAST, SYNC CLEAR	CB8C

LOGIC SYMBOL



LOGIC DIAGRAM



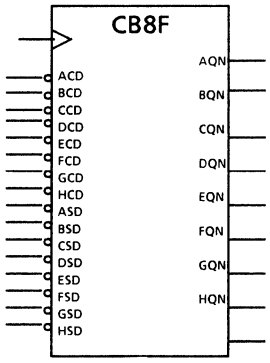
Gates Used: 113 February, 1987

Coding syntax: Z (AQN, BQN, CQN, DQN, EQN, FQN, GQN, HQN) = CB8C (CL, CP) $

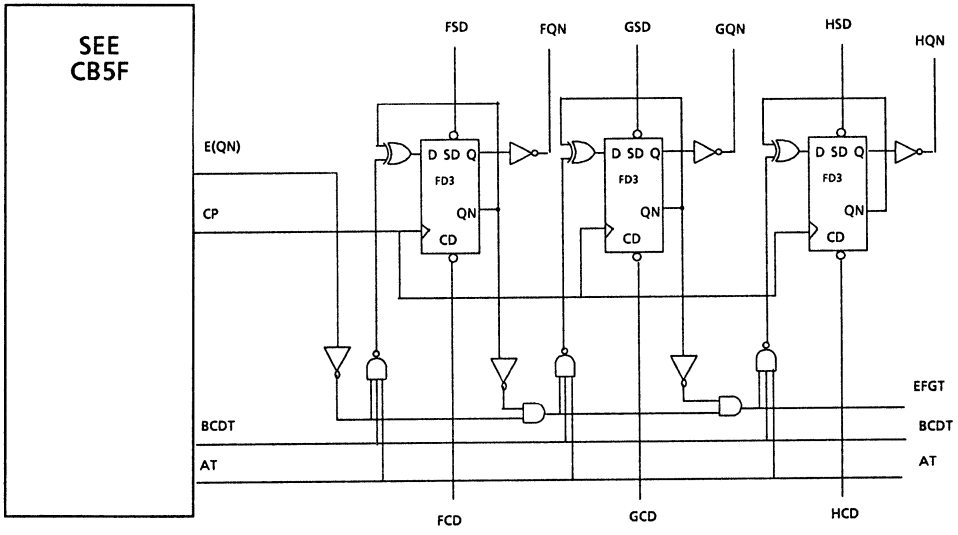
Input Loading: (3, 8)

CB8F	8 BIT BINARY UP COUNTER FAST, INDIVIDUAL CD SD	CB8F

LOGIC SYMBOL



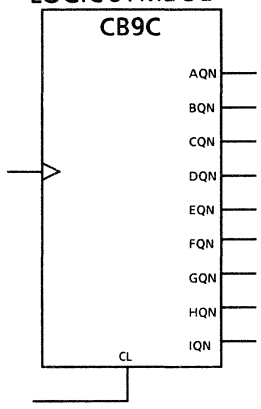
LOGIC DIAGRAM



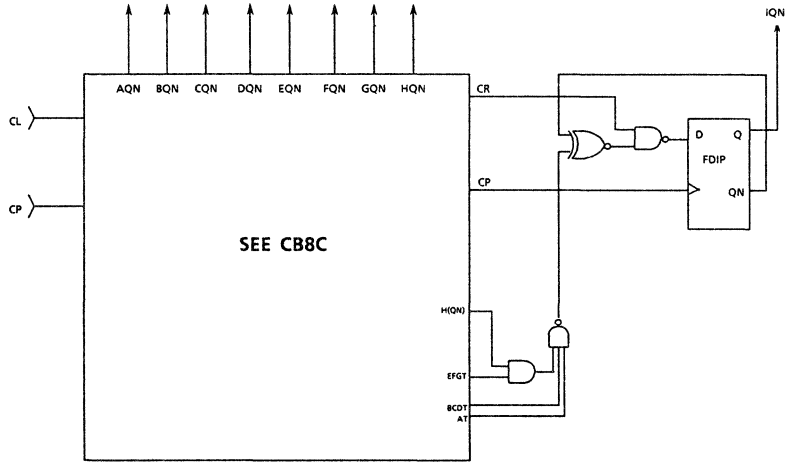
Gates Used: 127	February, 1987
Coding syntax: Z (AQN, BQN, CQN, DQN, EQN, FQN, GQN, HQN) =	
CB8F (CP, ACD, BCD, CCD, DCD, ECD, FCD, GCD, HCD, ASD, BSD, CSD, DSD, ESD,	
HSD GSD, HSD) $	
Input Loading: (8, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2,	
2, 2, 2)	

CB9C	9 BIT BINARY UP COUNTER FAST, SYNC CLEAR	CB9C

LOGIC SYMBOL



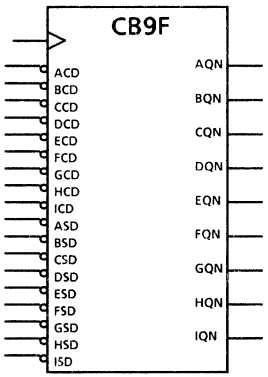
LOGIC DIAGRAM



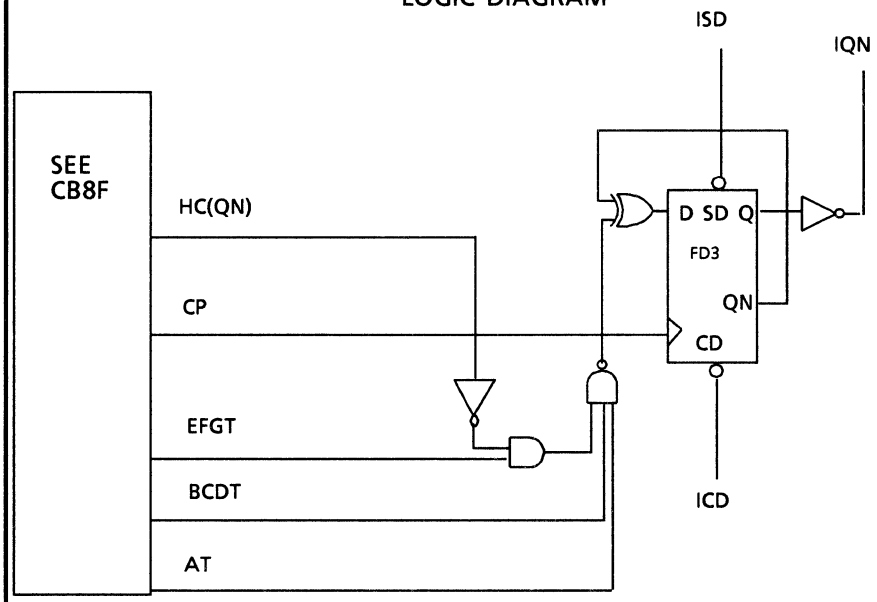
ates Used: 131	February, 1987
ding syntax: Z (AQN, BQN, CQN, DQN, EQN, FQN, GQN, HQN, IQN) = CB9C	(CL, CP) $
ut Loading:	(3, 9)

CB9F — 9 BIT BINARY UP COUNTER FAST, INDIVIDUAL CD SD — CB9F

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 145 — February, 1987

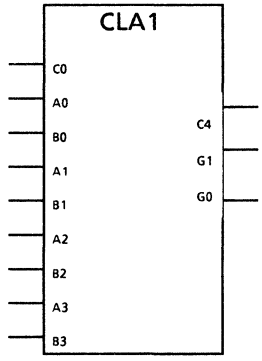
Coding syntax: Z (AQN, BQN, CQN, DQN, EQN, FQN, GQN, HQN, IQN)

= CB9F (CP, ACD, BCD, CCD, DCD, ECD,FCD, GCD, HCD, ICD, ASD, BSD, CSD, DSD, ESD, FSD, GSD, HSD, ISD) $

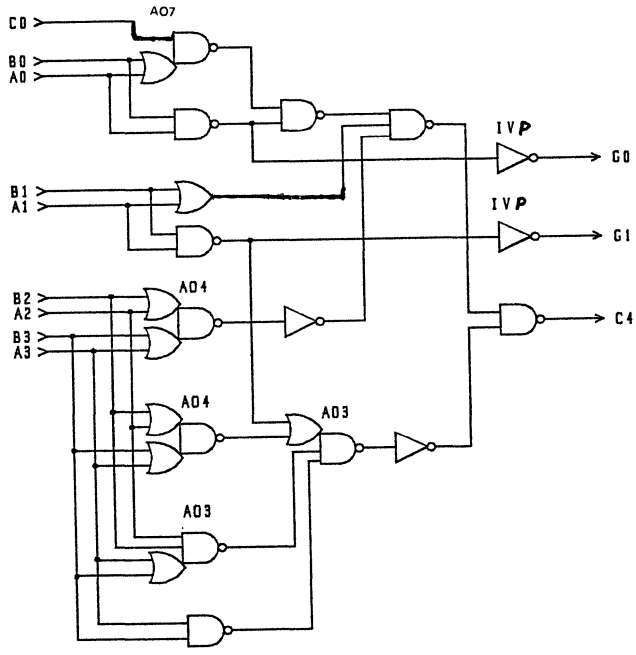
Input Loading: (9, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2)

CLA1	CARRY LOOK AHEAD FOR 4 BIT ADDER (LEAST SIGNIFICANT NIBBLE)	CLA1

LOGIC SYMBOL



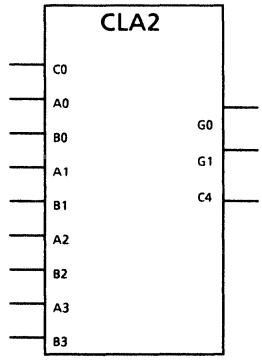
LOGIC DIAGRAM



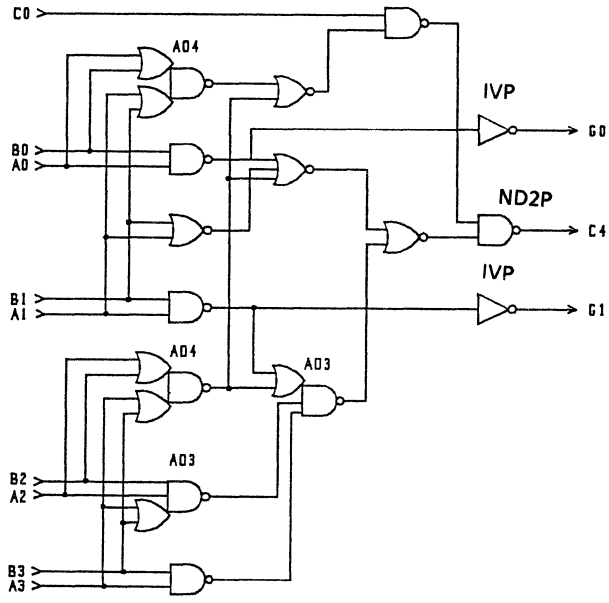
Gates Used: 24	February, 1987
Coding syntax: Z (C4, G0, G1) = CLA1 (C0, A0, B0, A1, B1, A2, A2, A3, A3) $	
Input Loading: (1, 2, 2, 2, 2, 3, 3, 4, 4)	

CLA2 — CARRY LOOK AHEAD FOR 4 BIT ADDER — CLA2

LOGIC SYMBOL



LOGIC DIAGRAM



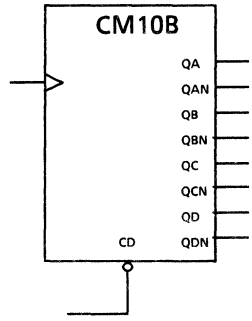
Gates Used: 21 — February, 1987

Coding syntax: Z (G0, G1, C4) = CLA2 (C0, A0, B0, A1, B1, A2, B2, A3, B3) $

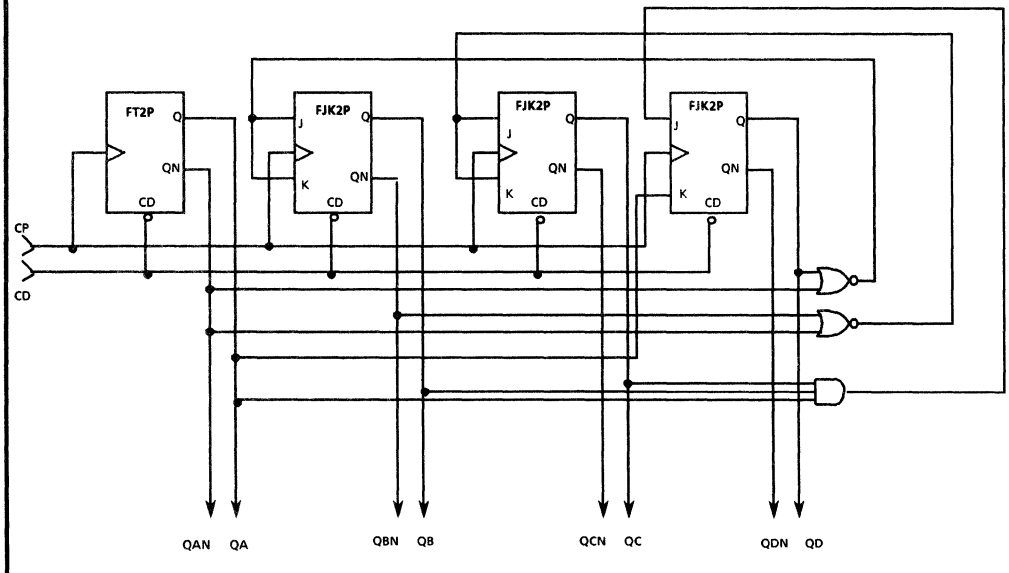
Input Loading: (1, 2, 2, 3, 3, 2, 2, 3, 3)

CM10B	MODULO 10 BINARY COUNTER CLEAR DIRECT	CM10B

LOGIC SYMBOL



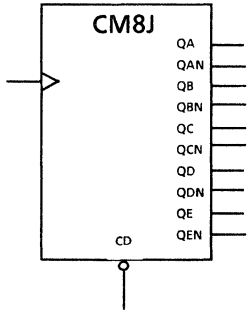
LOGIC DIAGRAM



Gates Used: 45	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = CM10B (CP, CD) $	
Input Loading:	(4, 8)

CM10J MODULO 10 JOHNSON COUNTER CLEAR DIRECT CM10J

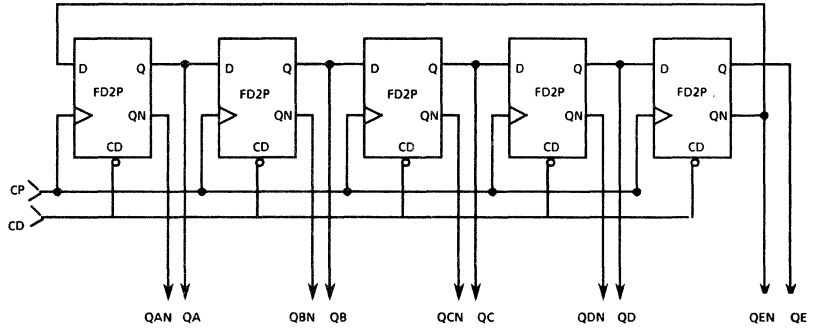
LOGIC SYMBOL



TRUTH TABLE

OUTPUT				
QA	QB	QC	QD	QE
0	0	0	0	0
1	0	0	0	0
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0
1	1	1	1	1
0	1	1	1	1
0	0	1	1	1
0	0	0	1	1
0	0	0	0	1

LOGIC DIAGRAM



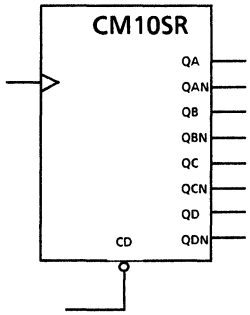
Gates Used: 45 February, 1987

Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE QEN,) = CM10J (CP, CD) $

Input Loading: (5, 10)

CM10SR — MODULO 10 SHIFT COUNTER CLEAR DIRECT — CM10SR

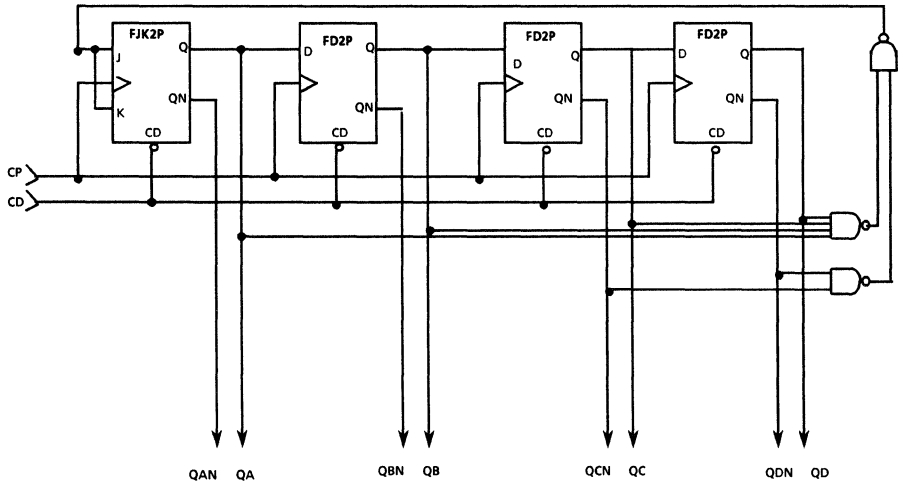
LOGIC SYMBOL



TRUTH TABLE

OUTPUT			
QA	QB	QC	QD
0	0	0	0
1	0	0	0
0	1	0	0
1	0	1	0
1	1	0	1
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1

LOGIC DIAGRAM



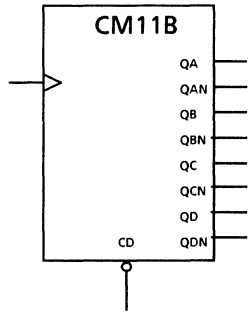
Gates Used: 42 — February, 1987

Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = CM10SR (CP, CD) $

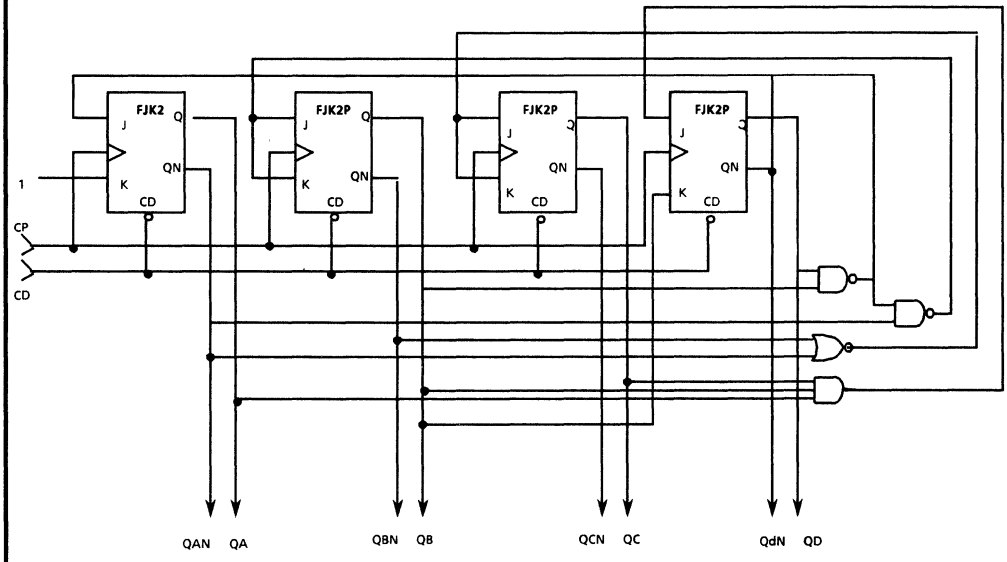
Input Loading: (4, 8)

CM11B	MODULO 11 BINARY COUNTER CLEAR DIRECT	CM11B

LOGIC SYMBOL



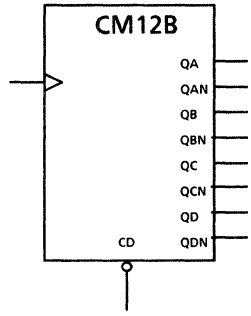
LOGIC DIAGRAM



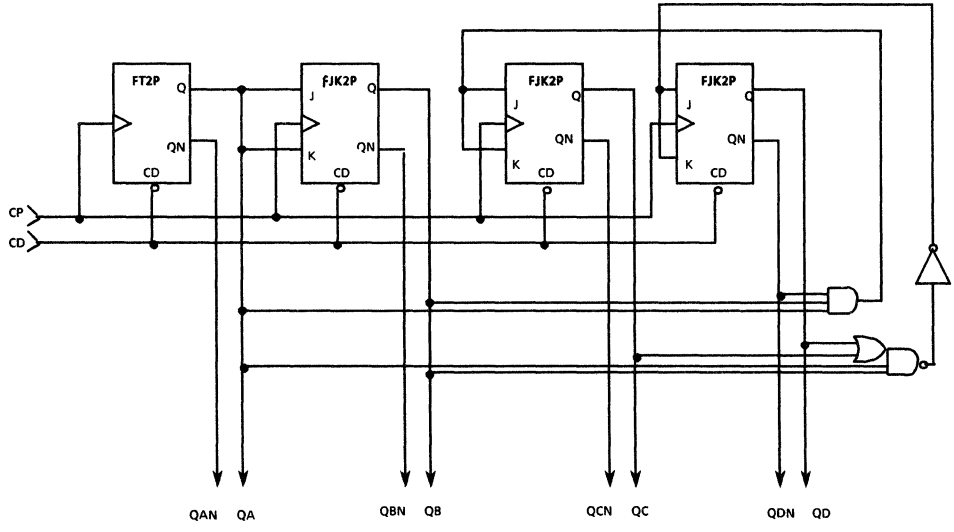
Gates Used: 49	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = CM11B (CP, CD) $	
Input Loading:	(4, 8)

CM12B	MODULO 12 BINARY COUNTER CLEAR DIRECT	CM12B

LOGIC SYMBOL



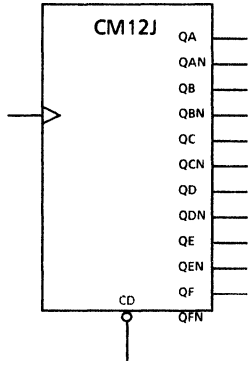
LOGIC DIAGRAM



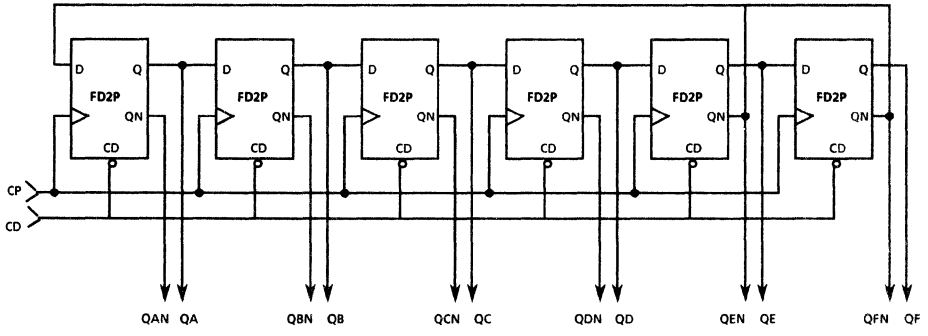
Gates Used: 46	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = CM12B (CP, CD) $	
Input Loading:	(4, 8)

CM12J	MODULO 12 JOHNSON COUNTER CLEAR DIRECT	CM12J

LOGIC SYMBOL



LOGIC DIAGRAM



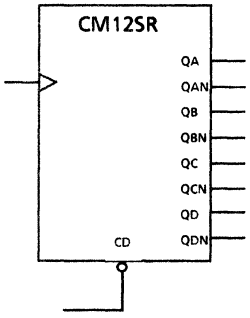
Gates Used: 54 February, 1987

Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN) = CM12J (CP, CD) $

Input Loading: (6, 12)

CM12SR — MODULO 10 SHIFT COUNTER CLEAR DIRECT — CM12SR

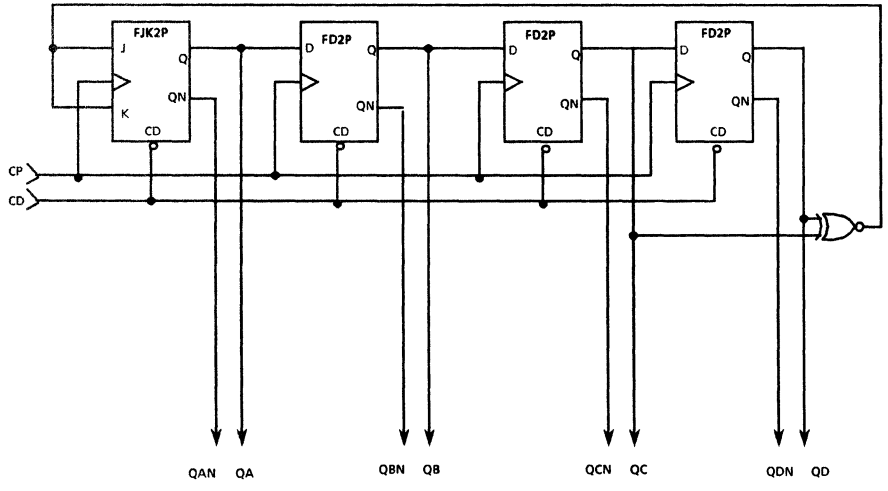
LOGIC SYMBOL



TRUTH TABLE

OUTPUT			
QA	QB	QC	QD
0	0	0	0
1	0	0	0
0	1	0	0
1	0	1	0
1	1	0	1
1	1	1	0
1	1	1	1
0	1	1	1
1	0	1	1
0	1	0	1
0	0	1	1
0	0	0	1

LOGIC DIAGRAM



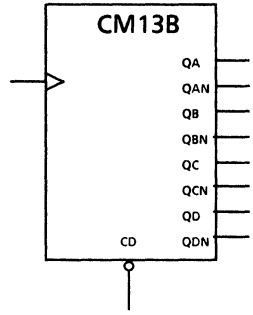
Gates Used: 41 — February, 1987

Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = CM12SR (CP, CD) $

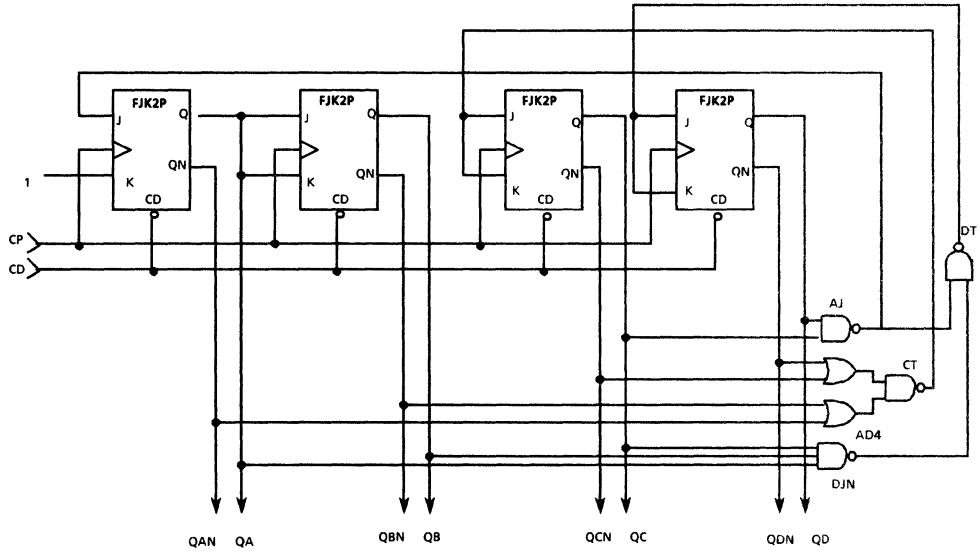
Input Loading: (4, 8)

CM13B	MODULO 13 BINARY COUNTER CLEAR DIRECT	CM13B

LOGIC SYMBOL



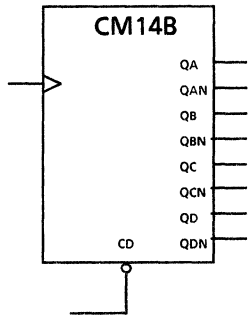
LOGIC DIAGRAM



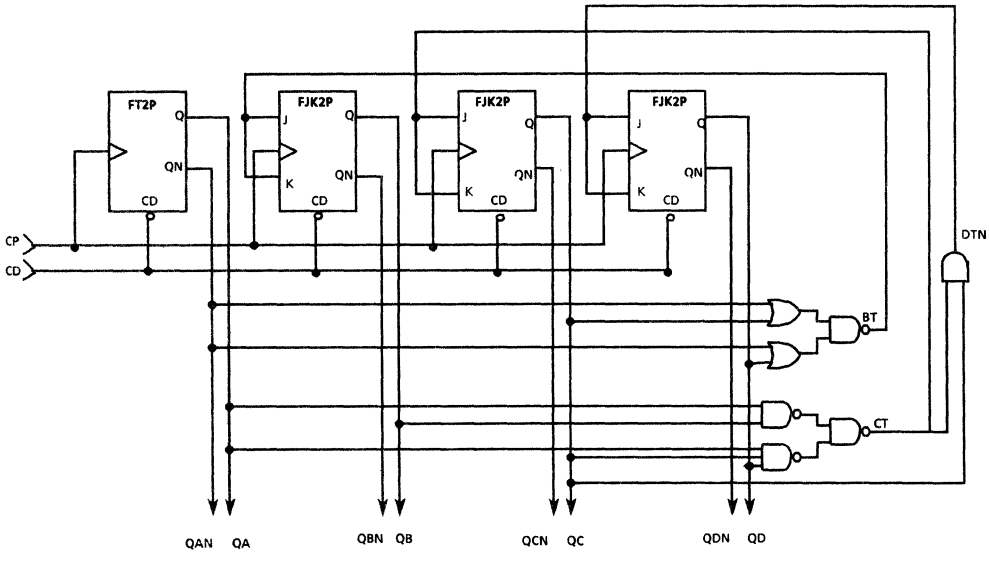
Gates Used: 50	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = CM13B (CP, CD) $	
Input Loading:	(4, 8)

CM14B	MODULO 14 BINARY COUNTER CLEAR DIRECT	CM14B

LOGIC SYMBOL



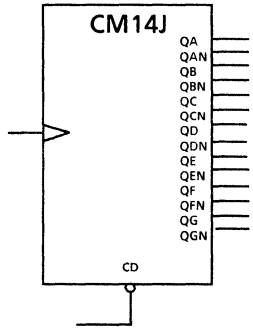
LOGIC DIAGRAM



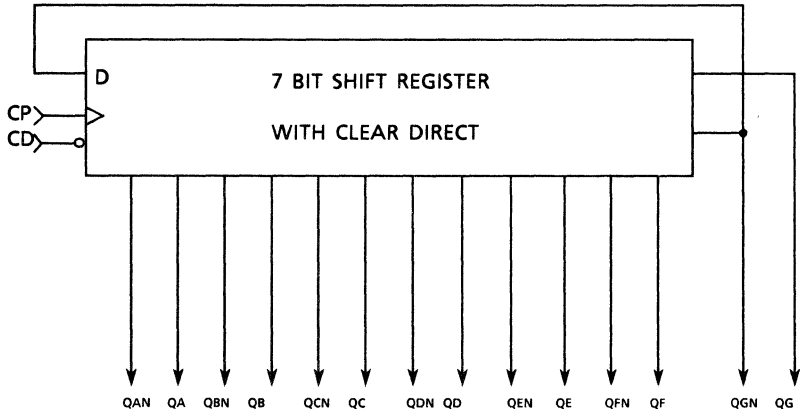
Gates Used: 49	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = CM14B (CP, CD) $	
Input Loading:	(4, 8)

CM14J	MODULD 14 JOHNSON COUNTER, CLEAR DIRECT	CM14J

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 63 February, 1987

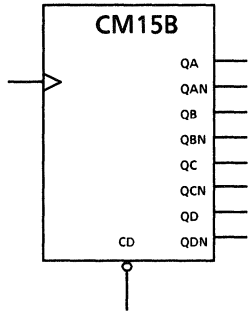
Coding syntax: Z ((QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN) =

CM14J (CP, CD) $

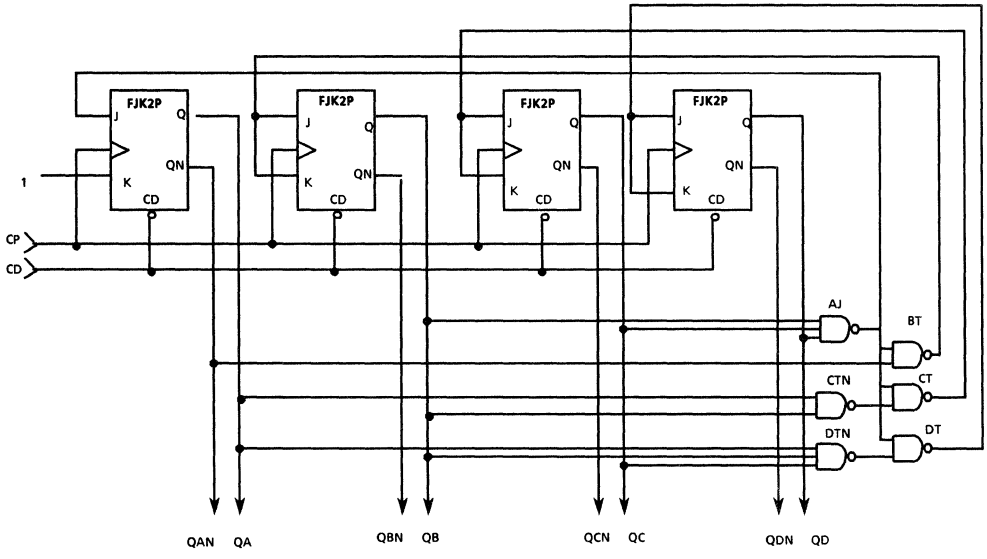
Input Loading: (7, 14)

CM15B	MODULO 15 BINARY COUNTER CLEAR DIRECT	CM15B

LOGIC SYMBOL



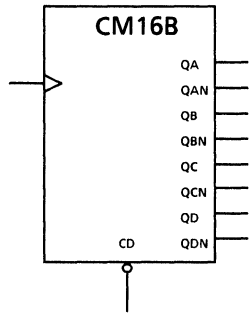
LOGIC DIAGRAM



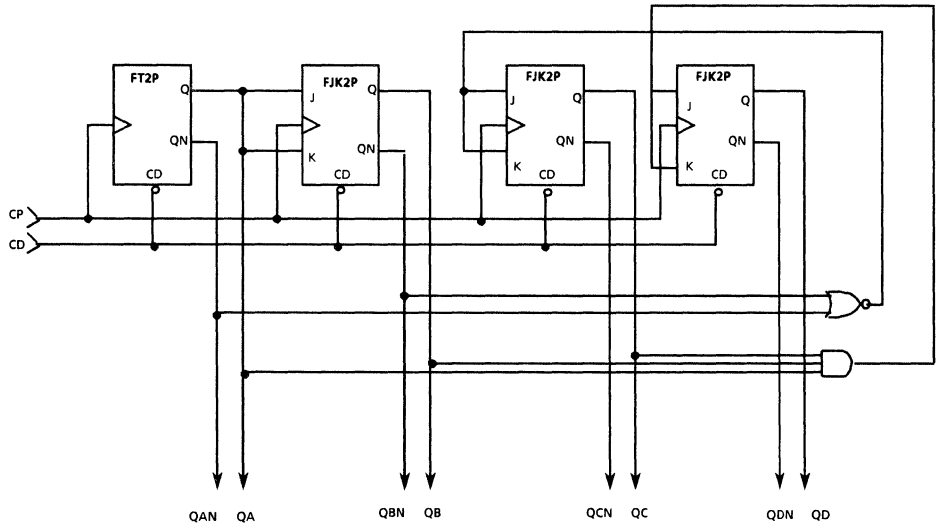
Gates Used: 52	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = CM15B (CP, CD) $	
Input Loading:	(4, 8)

CM16B	MODULO 16 BINARY COUNTER CLEAR DIRECT	CM16B

LOGIC SYMBOL



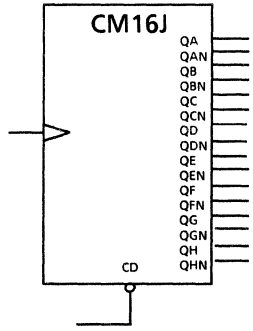
LOGIC DIAGRAM



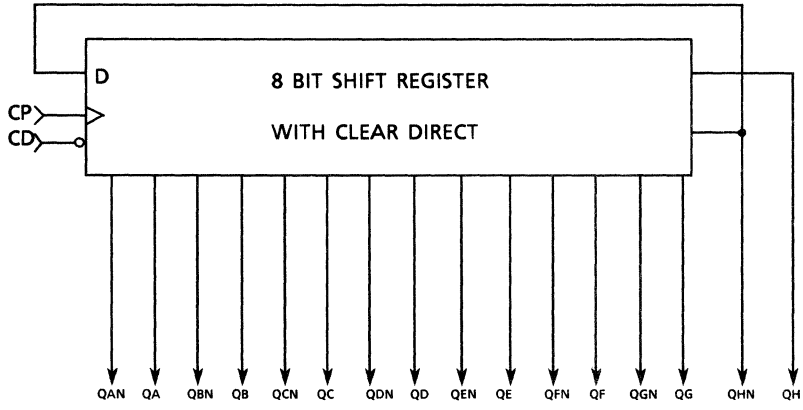
Gates Used: 44	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = CM16B (CP, CD) $	
Input Loading:	(4, 8)

CM16J	MODULD 16 JOHNSON COUNTER, CLEAR DIRECT	CM16J

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 72 February, 1987

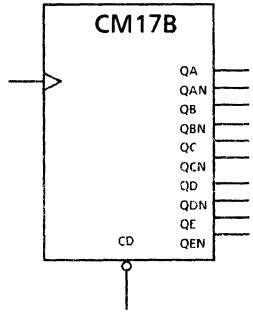
Coding syntax: Z ((QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN) =

CM16J (CP, CD) $

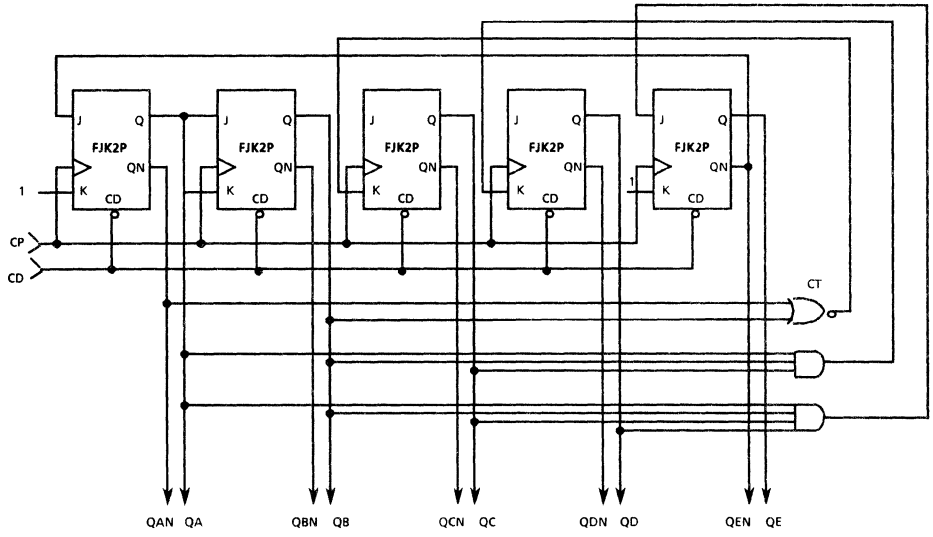
Input Loading: (8, 16)

CM17B	MODULO 17 BINARY COUNTER CLEAR DIRECT	CM17B

LOGIC SYMBOL



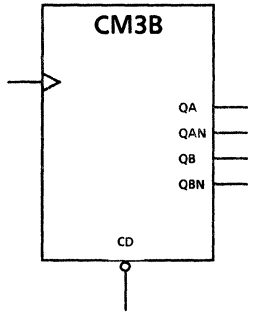
LOGIC DIAGRAM



Gates Used: 61	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE QEN) = CM17B (CP, CD) $	
Input Loading:	(5, 10)

CM3B — MODULO 3 BINARY COUNTER CLEAR DIRECT — CM3B

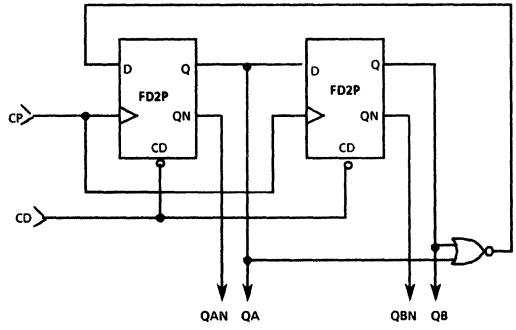
LOGIC SYMBOL



TRUTH TABLE

OUTPUT	
QA	QB
0	0
1	0
0	1

LOGIC DIAGRAM



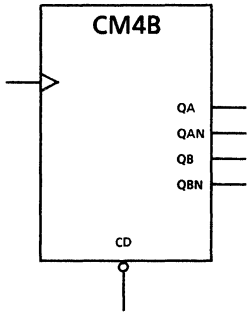
Gates Used: 19 — February, 1987

Coding syntax: Z (QA, QAN, QB, QBN) = CM3B (CP, CD) $

Input Loading: (2, 4)

CM4B — MODULO 4 BINARY COUNTER CLEAR DIRECT — CM4B

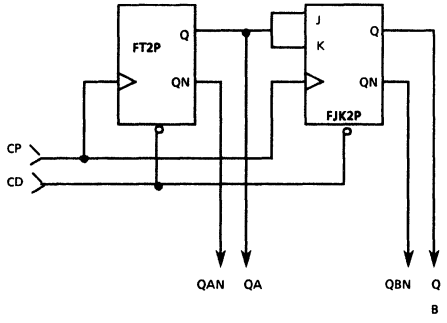
LOGIC SYMBOL



TRUTH TABLE

OUTPUT	
QA	QB
0	0
1	0
0	1
1	1

LOGIC DIAGRAM



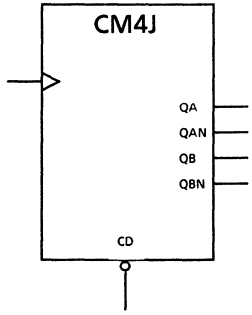
Gates Used: 19 — February, 1987

Coding syntax: Z (QA, QAN, QB, QBN) = CM4B (CP, CD) $

Input Loading: (2, 4)

CM4J MODULO 4 JOHNSON COUNTER CLEAR DIRECT CM4J

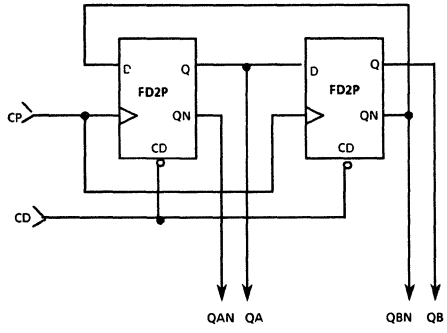
LOGIC SYMBOL



TRUTH TABLE

OUTPUT	
QA	QB
0	0
1	0
1	1
0	1

LOGIC DIAGRAM



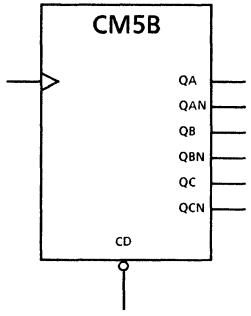
Gates Used: 18 February, 1987

Coding syntax: Z (QA, QAN, QB, QBN) = CM4J (CP, CD) $

Input Loading: (2, 4)

CM5B — MODULO 5 BINARY COUNTER CLEAR DIRECT — CM5B

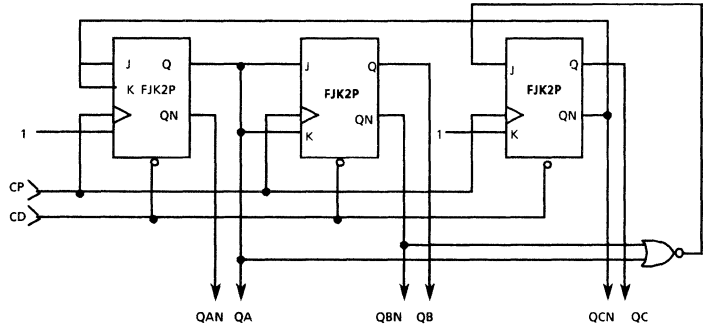
LOGIC SYMBOL



TRUTH TABLE

OUTPUT		
QA	QB	QC
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1

LOGIC DIAGRAM



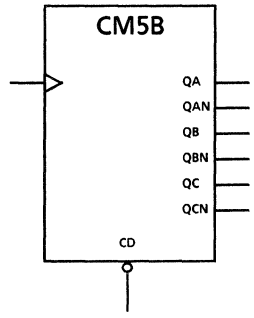
Gates Used: 34 — February, 1987

Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN) = CM5B (CP, CD) $

Input Loading: (3, 6)

CM5SR	MODULO 5 SHIFT COUNTER CLEAR DIRECT	CM5SR

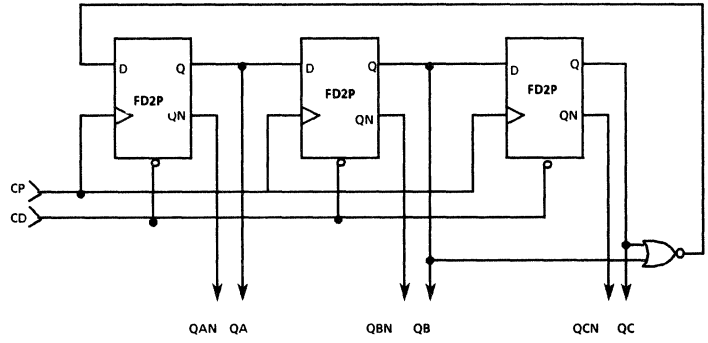
LOGIC SYMBOL



TRUTH TABLE

OUTPUT		
QA	QB	QC
0	0	0
1	0	0
1	1	0
0	1	1
0	0	1

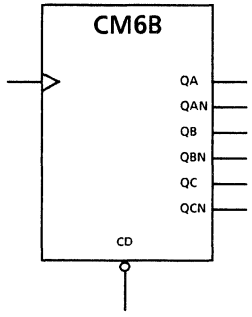
LOGIC DIAGRAM



Gates Used: 28	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN) = CM5SR (CP, CD) $	
Input Loading:	(3, 6)

CM6B — MODULO 6 BINARY COUNTER CLEAR DIRECT — CM6B

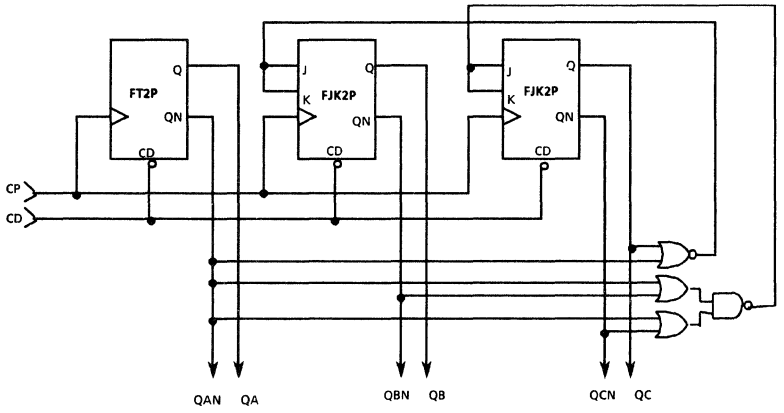
LOGIC SYMBOL



TRUTH TABLE

OUTPUT		
QA	QB	QC
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1
1	0	1

LOGIC DIAGRAM



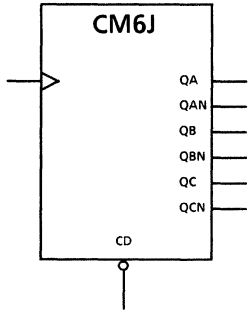
Gates Used: 33 — February, 1987

Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN) = CM6B (CP, CD) $

Input Loading: (3, 6)

CM6J — MODULO 6 JOHNSON COUNTER CLEAR DIRECT — CM6J

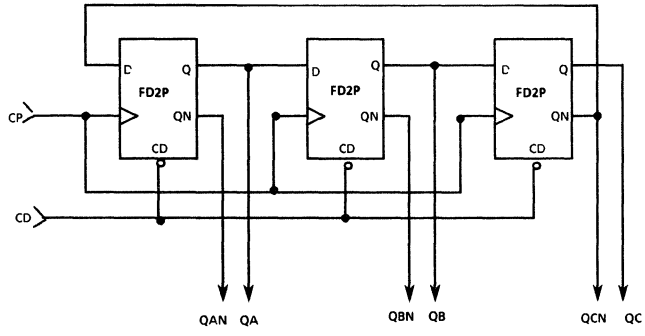
LOGIC SYMBOL



TRUTH TABLE

OUTPUT		
QA	QB	QC
0	0	0
1	0	0
1	1	0
1	1	1
0	1	1
0	0	1

LOGIC DIAGRAM



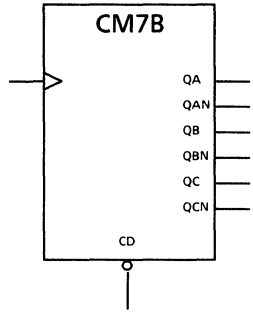
Gates Used: 27 — February, 1987

Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN) = CM6J (CP, CD) $

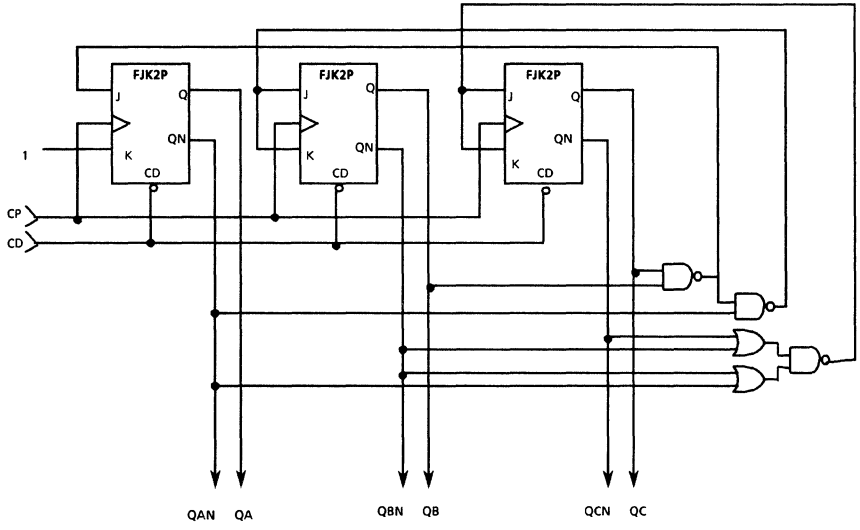
Input Loading: (3, 6)

CM7B	MODULO 7 BINARY COUNTER CLEAR DIRECT	CM7B

LOGIC SYMBOL



LOGIC DIAGRAM



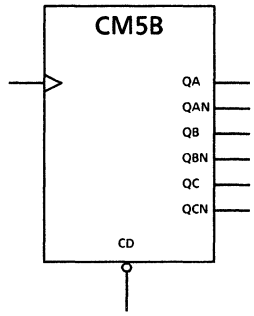
Gates Used: 37 February, 1987

Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN) = CM7B (CP, CD) $

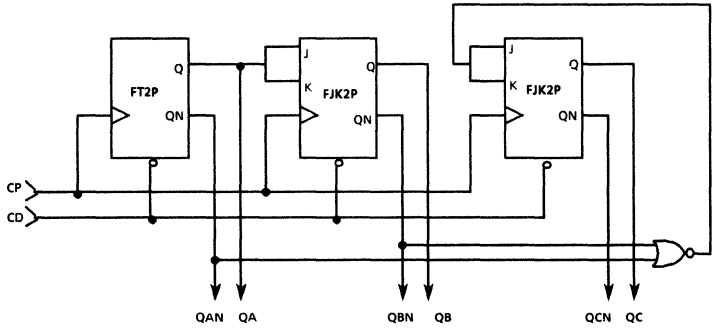
Input Loading: (3, 6)

CM8B	MODULO 8 BINARY COUNTER CLEAR DIRECT	CM8B

LOGIC SYMBOL



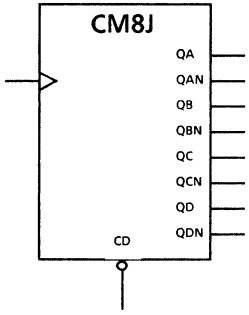
LOGIC DIAGRAM



Gates Used: 29	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN) = CM8B (CP, CD) $	
Input Loading:	(3, 6)

CM8J — MODULO 8 BINARY COUNTER CLEAR DIRECT — CM8J

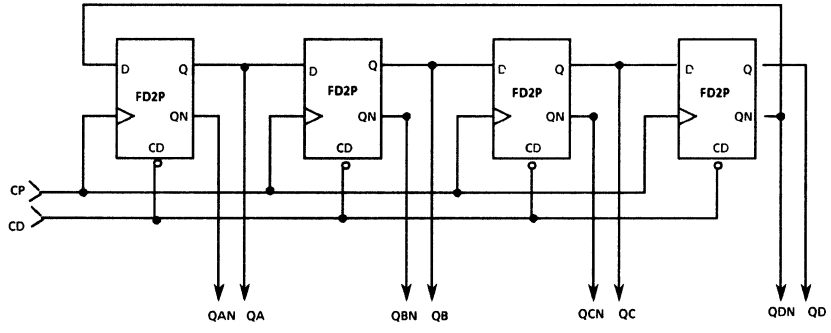
LOGIC SYMBOL



TRUTH TABLE

OUTPUT			
QA	QB	QC	QD
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1

LOGIC DIAGRAM



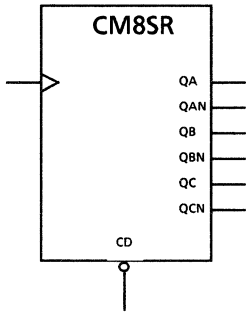
Gates Used: 36 — February, 1987

Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN,) = CM8J (CP, CD) $

Input Loading: (4, 8)

CM8SR — MODULO 8 SHIFT COUNTER CLEAR DIRECT — CM8SR

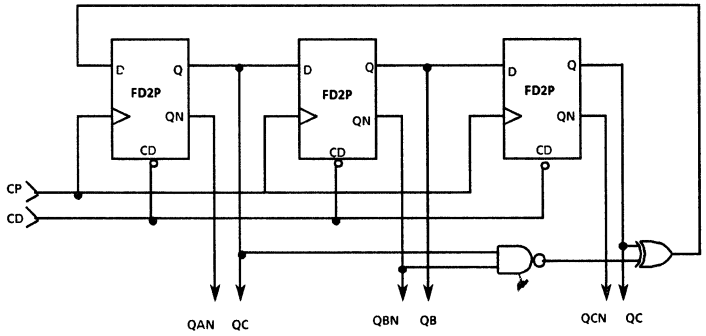
LOGIC SYMBOL



TRUTH TABLE

OUTPUT		
QA	QB	QC
0	0	0
1	0	0
0	1	0
1	0	1
1	1	0
1	1	1
0	1	1
0	0	1

LOGIC DIAGRAM



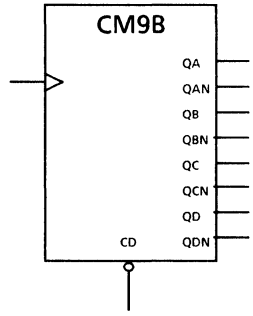
Gates Used: 31 — February, 1987

Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN) = CM8SR (CP, CD) $

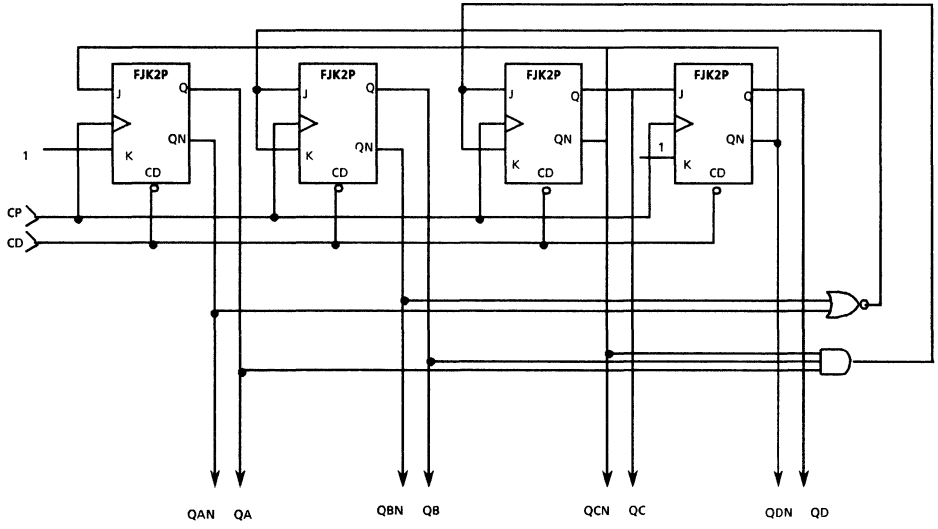
(3, 6)

CM9B	MODULO 9 BINARY COUNTER CLEAR DIRECT	CM9B

LOGIC SYMBOL



LOGIC DIAGRAM



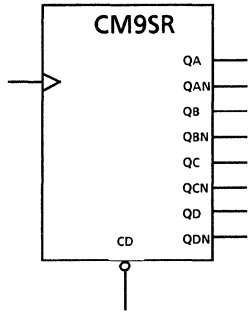
Gates Used: 47 February, 1987

Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = CM9B (CP, CD) $

Input Loading: (4, 8)

CM9SR — MODULO 9 SHIFT COUNTER CLEAR DIRECT — CM9SR

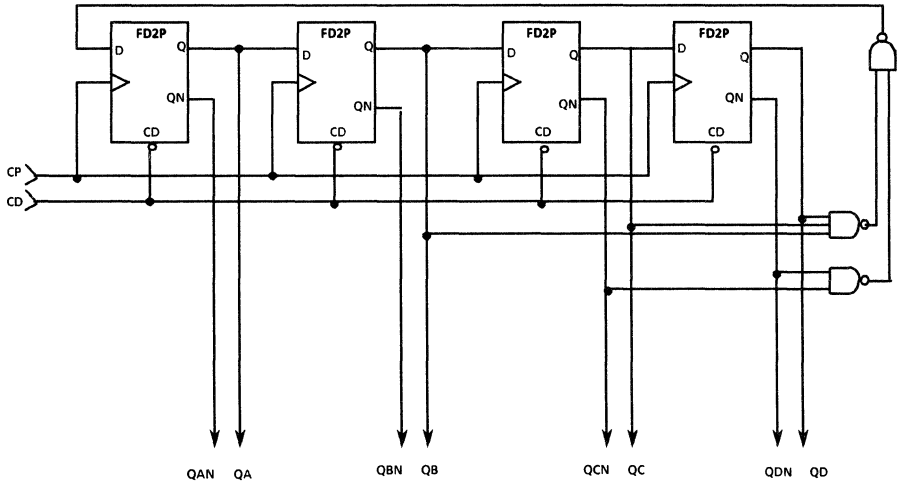
LOGIC SYMBOL



TRUTH TABLE

OUTPUT			
QA	QB	QC	QD
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
0	1	1	1
1	0	1	1
0	1	0	1
0	0	1	0
0	0	0	1

LOGIC DIAGRAM



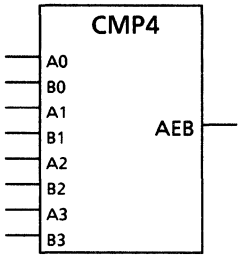
Gates Used: 40 — February, 1987

Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = CM9SR (CP, CD) $

Input Loading: (4, 8)

CMP4 — 4 BIT EQUALITY COMPARATOR — CMP4

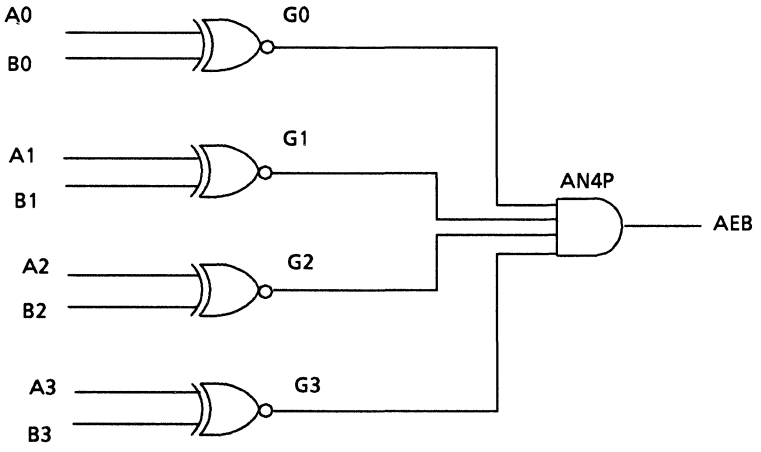
LOGIC SYMBOL



TRUTH TABLE

0=0	1=1	2=2	3=3	AEB
1	1	1	1	1
(	ANY	0	)	0

LOGIC DIAGRAM



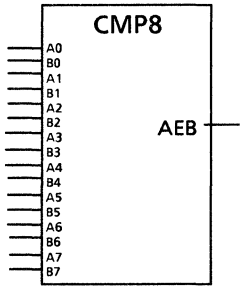
Gates Used: 15 — February, 1987

Coding syntax: Z (AEB) = CMP4 (A0, B0, A1, B1, A2, B2, A3, B3) $

Input Loading: (1, 2, 1, 2, 1, 2, 1, 2)

CMP8 — 8 BIT EQUALITY COMPARATOR — CMP8

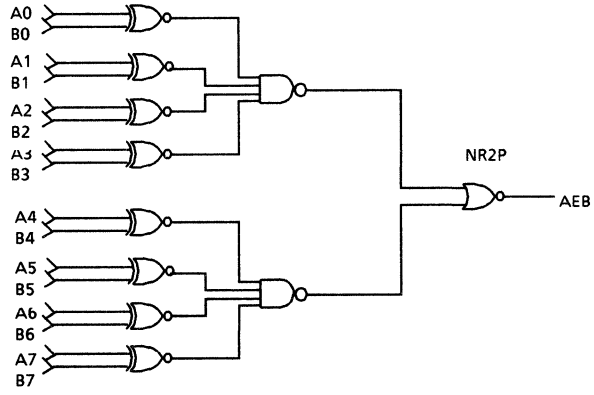
LOGIC SYMBOL



TRUTH TABLE

0=0	1=1	2=2	3=3	4=4	5=5	6=6	7=7	AEB
1	1	1	1	1	1	1	1	1
(		ANY		0		)		0

LOGIC DIAGRAM



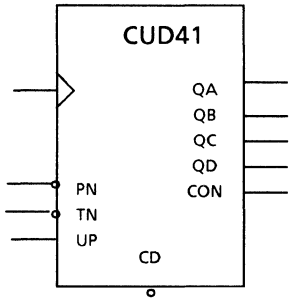
Gates Used: 30 — February, 1987

Coding syntax: Z (AEB) = CMP8 (A0, B0, A1, B1, A2, B2, A3, B3, A4, B4, A5, B5, A6, B6, A7, B7) $

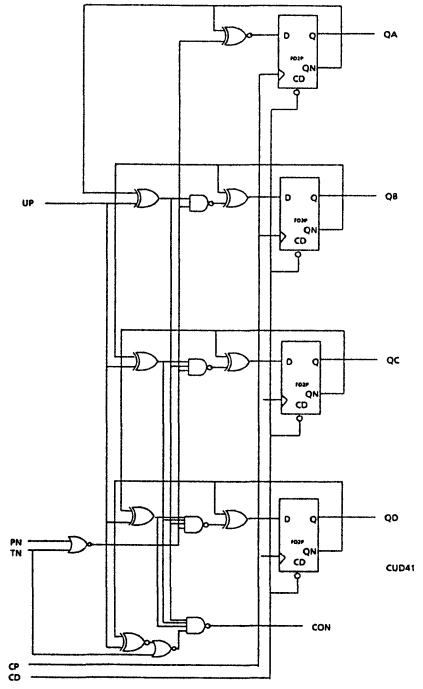
Input Loading: (1, 2, 1, 2, 1, 2, 1, 2, 1, 2, 1, 2, 1, 2, 1, 2)

CUD41	4 BIT UP/DOWN COUNTER, EXPANDABLE WITH ASYNCHRONOUS CLEAR	CUD41

LOGIC SYMBOL



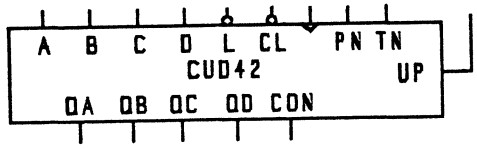
LOGIC DIAGRAM



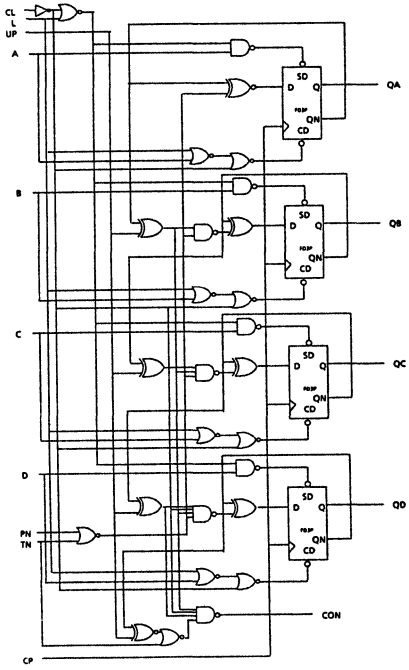
Gates Used: 72	February, 1987
Coding syntax: Z (QA, QB, QC, QD, CON) = CUD41 (CP, PN, TN, UP, CD) $	
Input Loading:	(4, 2, 3, 4, 8)

CUD42	4 BIT UP/DOWN COUNTER, EXPANDABLE WITH ASYNCHRONOUS LOAD AND CLEAR	CUD42

LOGIC SYMBOL



LOGIC DIAGRAM



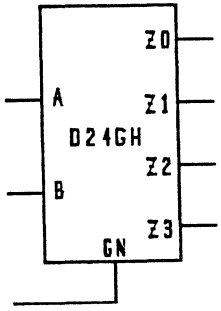
Gates Used: 92 February, 1987

Coding syntax: Z (QA, QB, QC, QD, CON) = CUD42 (A, B, C, D, L, CL, CP, PN, TN, UP) $

Input Loading: (2, 2, 2, 2, 6, 3, 4, 2, 3, 4,)

D24GH	2 TO 4 DECODER, GATED OUTPUTS ACTIVE HI	D24GH

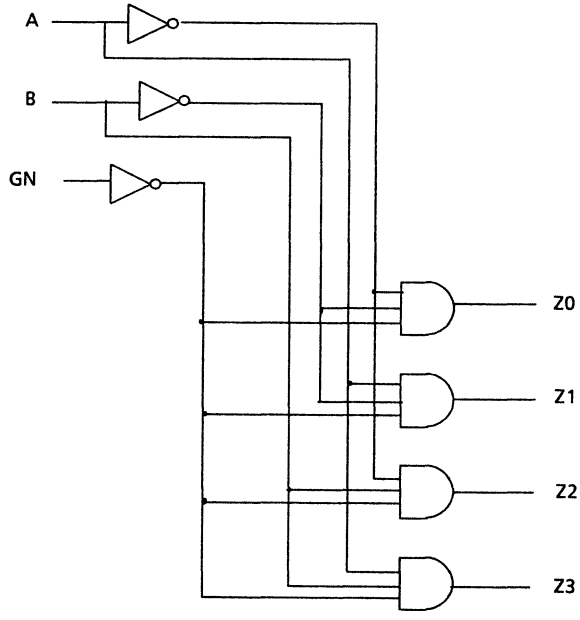
LOGIC SYMBOL



TRUTH TABLE

A	B	GN	Z0	Z1	Z2	Z3
0	0	0	1	0	0	0
1	0	0	0	1	0	0
0	1	0	0	0	1	0
1	1	0	0	0	0	1
X	X	1	0	0	0	0

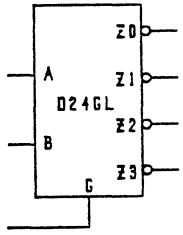
LOGIC DIAGRAM



Gates Used: 15	February, 1987
Coding syntax: Z (Z0, Z1, Z2, Z3) = D24GH (A, B, GN) $	
Input Loading: (3.5, 3.5, 2)	

D24GL	2 TO 4 DECODER, GATES OUTPUTS ACTIVE LO	D24GL

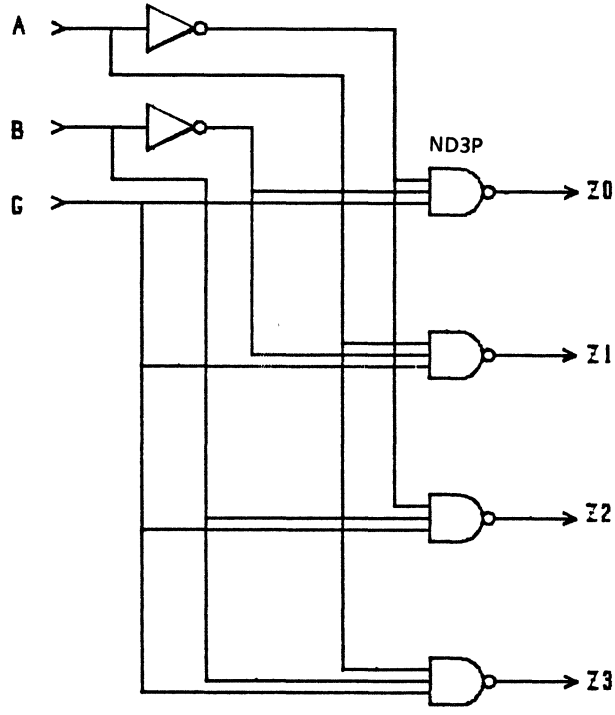
LOGIC SYMBOL



TRUTH TABLE

A	B	G	Z0	Z1	Z2	Z3
0	0	1	0	1	1	1
1	0	1	1	0	1	1
0	1	1	1	1	0	1
1	1	1	1	1	1	0
X	X	0	1	1	1	1

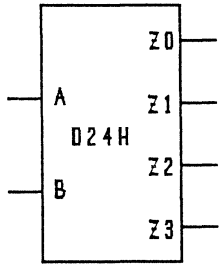
LOGIC DIAGRAM



Gates Used: 16	February, 1987
Coding syntax: Z (Z0, Z1, Z2, Z3) = D24GL (A, B, G) $	
Input Loading: (6, 6, 8)	

D24H	2 TO 4 DECODER, OUTPUTS ACTIVE HI	D24H

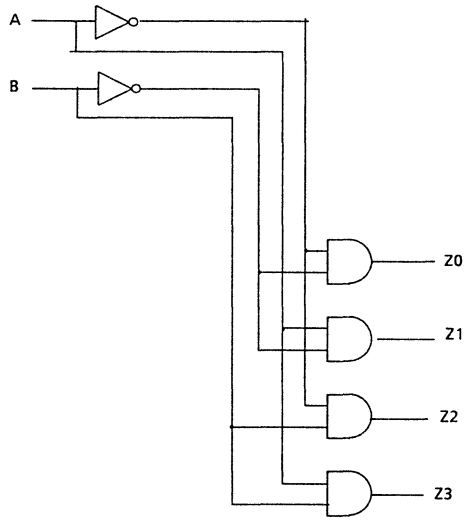
LOGIC SYMBOL



TRUTH TABLE

A	B	Z0	Z1	Z2	Z3
0	0	1	0	0	0
1	0	0	1	0	0
0	1	0	0	1	0
1	1	0	0	0	1

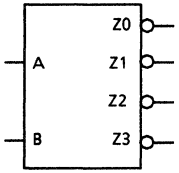
LOGIC DIAGRAM



Gates Used: 10	February, 1987
Coding syntax: Z (Z0, Z1, Z2, Z3) = D24H (A, B,) $	
Input Loading: (3.5, 3.5)	

D24L	2 TO 4 DECODER, OUTPUTS ACTIVE LO	D24L

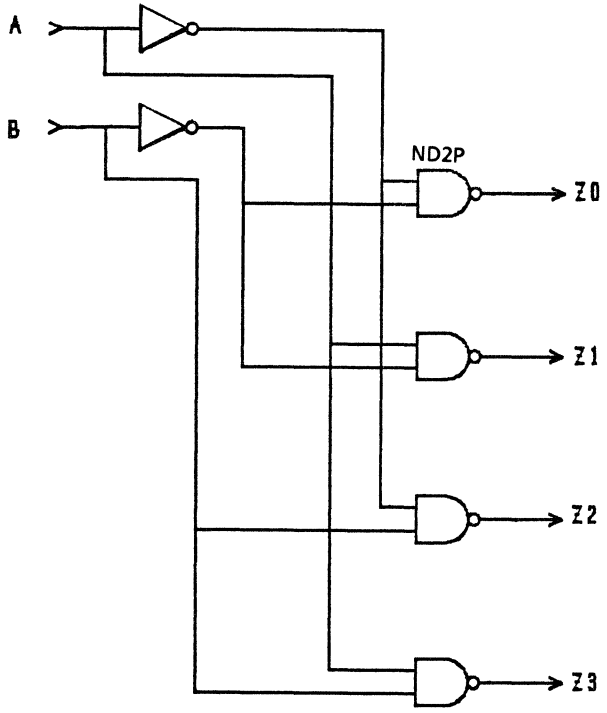
LOGIC SYMBOL



TRUTH TABLE

A	B	Z0	Z1	Z2	Z3
0	0	0	1	1	1
1	0	1	0	1	1
0	1	1	1	0	1
1	1	1	1	1	0

LOGIC DIAGRAM



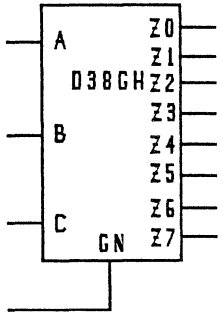
Gates Used: 10 February, 1987

Coding syntax: Z (Z0, Z1, Z2, Z3) = D24L (A, B,) $

Input Loading: (6, 6)

D38GH	3 TO 8 DECODER, GATED OUTPUTS ACTIVE HI	D38GH

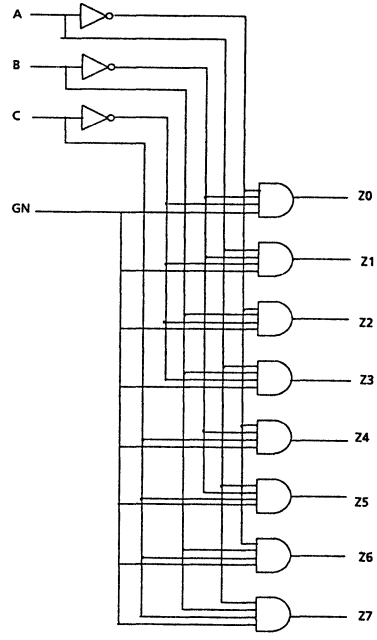
LOGIC SYMBOL



TRUTH TABLE

A	B	C	GN	0	1	2	3	4	5	6	7
0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	0	1
X	X	X	1	0	0	0	0	0	0	0	0

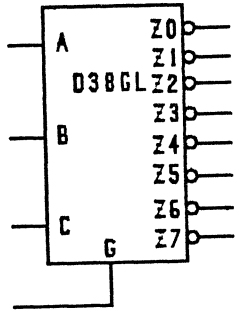
LOGIC DIAGRAM



Gates Used: 32	February, 1987
Coding syntax: Z (Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7) = D38GH	(A, B, C, GN) $
Input Loading:	(7, 7, 7, 8)

D38GL	3 TO 8 DECODER, GATED OUTPUTS ACTIVE LO	D38GL

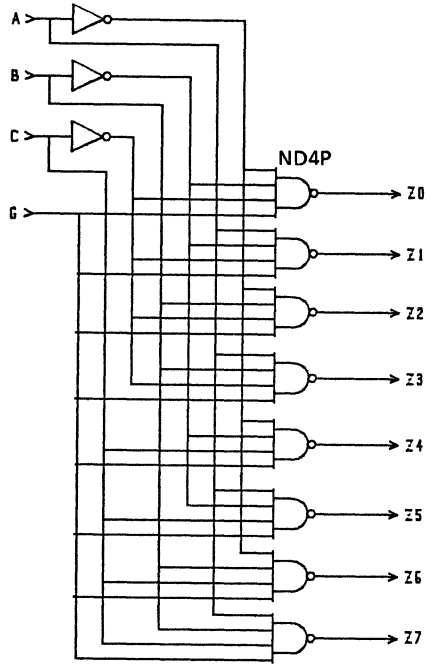
LOGIC SYMBOL



TRUTH TABLE

A	B	C	G	0	1	2	3	4	5	6	7
0	0	0	1	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	1	1	1	0	1	1	1	1
0	0	1	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0
X	X	X	0	1	1	1	1	1	1	1	1

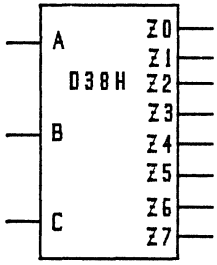
LOGIC DIAGRAM



Gates Used: 38	February, 1987
Coding syntax: Z (Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7) = D38GL	(A, B, C, G) $
Input Loading:	(11, 11, 11,16)

D38H — 3 TO 4 DECODER, OUTPUTS ACTIVE HI — D38H

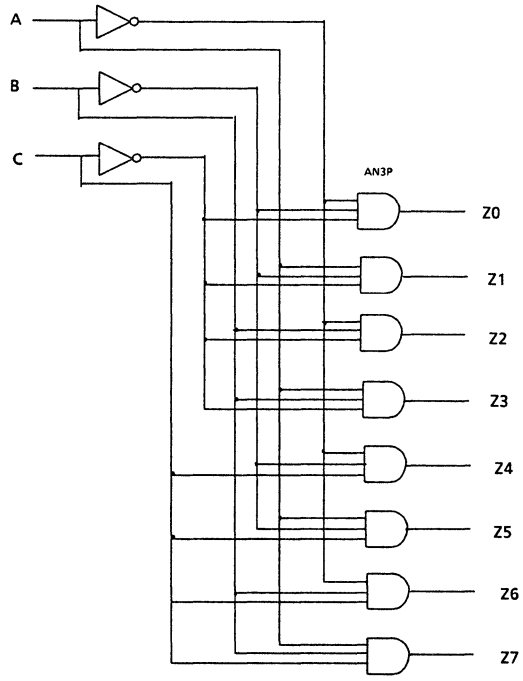
LOGIC SYMBOL



TRUTH TABLE

A	B	C	0	1	2	3	4	5	6	7
0	0	0	1	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
1	1	0	0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

LOGIC DIAGRAM



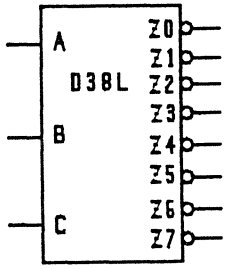
Gates Used: 27 — February, 1987

Coding syntax: Z (Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7) = D38H (A, B, C)$

Input Loading: (10, 10, 10)

D38L	3 TO 8 DECODER, OUTPUTS ACTIVE LO	D38L

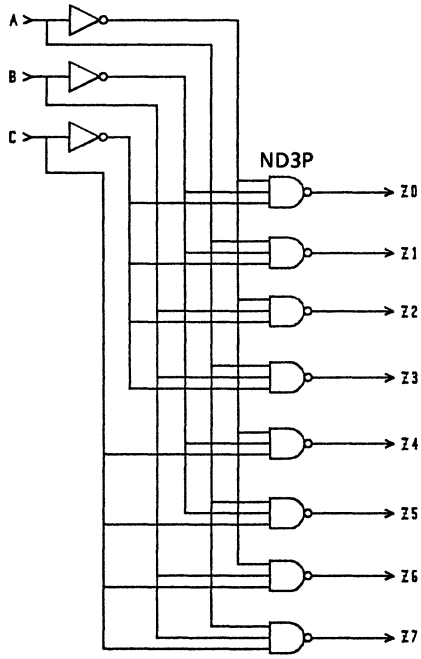
LOGIC SYMBOL



TRUTH TABLE

A	B	C	0	1	2	3	4	5	6	7
0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
1	1	0	1	1	1	0	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

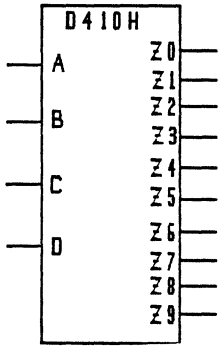
LOGIC DIAGRAM



Gates Used: 30	February, 1987
Coding syntax: Z (Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7) = D38L	(A, B, C) $
Input Loading:	(11, 11, 11)

D410H — 4 TO 10 DECODER, OUTPUTS ACTIVE HI — D410H

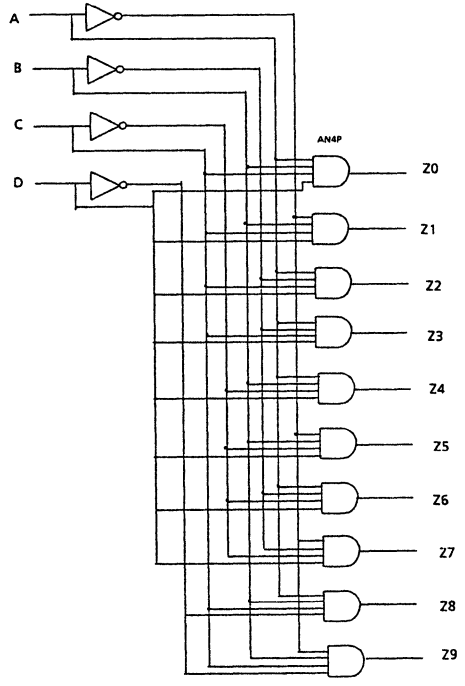
LOGIC SYMBOL



TRUTH TABLE

A	B	C	D	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	0	0	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
1	1	1	0	0	0	0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
X	1	X	1	0	0	0	0	0	0	0	0	0	0
X	X	1	1	0	0	0	0	0	0	0	0	0	0

LOGIC DIAGRAM



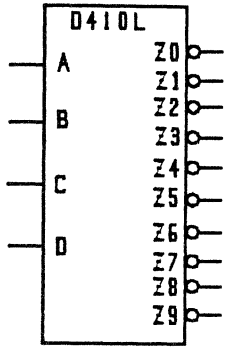
Gates Used: 38 — February, 1987

Coding syntax: Z (Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7, Z8, Z9) = D410H (A, B, C, D) $

Input Loading: (8, 7, 7, 5)

D410L	4 TO 10 DECODER, OUTPUTS ACTIVE LO	D410L

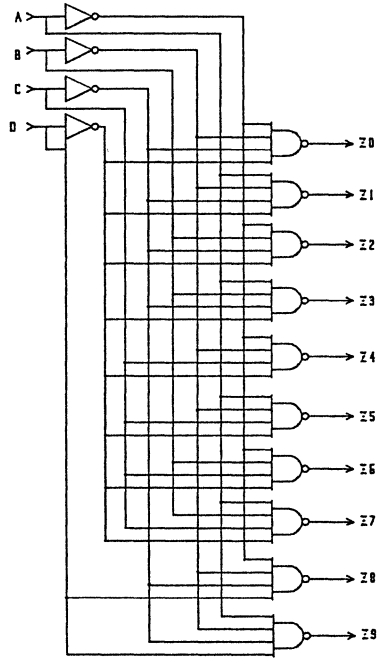
LOGIC SYMBOL



TRUTH TABLE

A	B	C	D	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
X	1	X	1	1	1	1	1	1	1	1	1	1	1
X	X	1	1	1	1	1	1	1	1	1	1	1	1

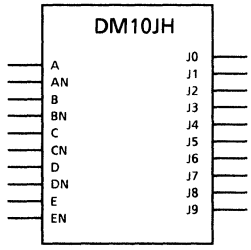
LOGIC DIAGRAM



Gates Used: 49	February, 1987
Coding syntax: Z (Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7, Z8, Z9) = D410L (A, B, C, D) $	
Input Loading:	(13, 11, 11, 7)

DM10JH SPIKE FREE DECODER FOR MOD 10 JOHNSON COUNTER, ACTIVE HI, SEE CM10J DM10JH

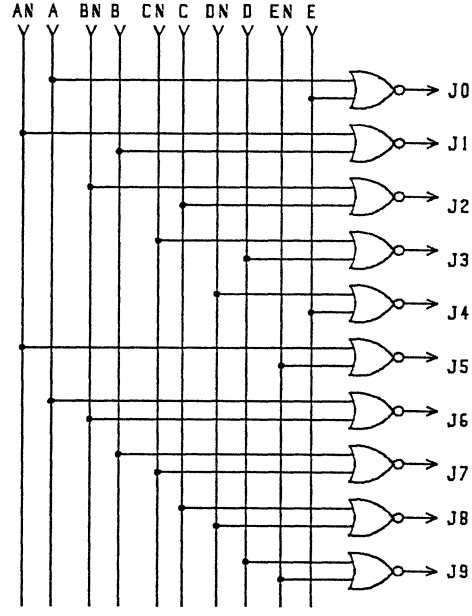
LOGIC SYMBOL



TRUTH TABLE

QA	QB	QC	QD	QE	
0	0	0	0	0	J0
1	0	0	0	0	J1
1	1	0	0	0	J2
1	1	1	0	0	J3
1	1	1	1	0	J4
0	1	1	1	1	J5
0	0	1	1	1	J6
0	0	0	1	1	J7
0	0	0	0	1	J8
0	0	0	0	1	J9

LOGIC DIAGRAM



Gates Used: 20 February, 1987

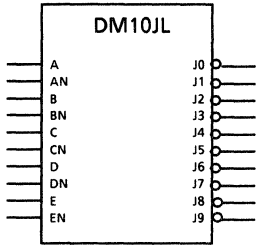
Loading Syntax: Z (J0, J1, J2, J3, J4, J5, J6, J7, J8, J9)

DM10JH (A, AN, B, BN, C, CN, D, DN, E, EN) $

Input Loading: (4, 4, 4, 4, 4, 4, 4, 4, 4, 4)

DM10JL SPIKE FREE DECODER FOR MOD 10 JOHNSON COUNTER, ACTIVE LO, SEE CM10J DM10JL

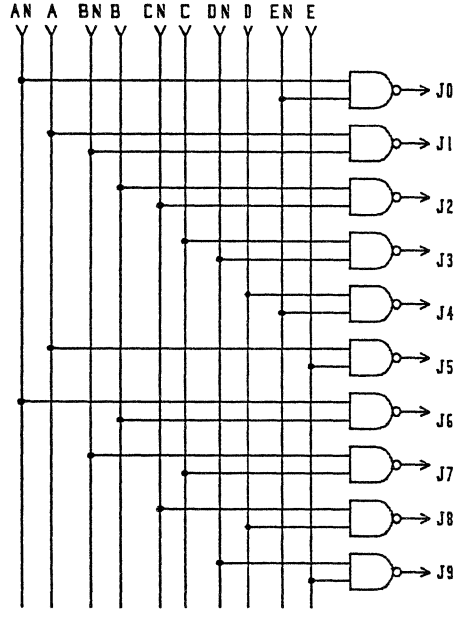
LOGIC SYMBOL



TRUTH TABLE

QA	QB	QC	QD	QE	
0	0	0	0	0	J0
1	0	0	0	0	J1
1	1	0	0	0	J2
1	1	1	0	0	J3
1	1	1	1	0	J4
0	1	1	1	1	J5
0	0	1	1	1	J6
0	0	0	1	1	J7
0	0	0	0	1	J8
0	0	0	0	1	J9

LOGIC DIAGRAM



Gates Used: 20 February, 1987

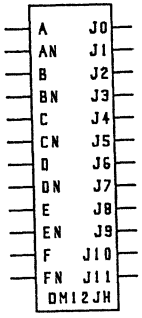
Loading Syntax: Z (J0, J1, J2, J3, J4, J5, J6, J7, J8, J9)

DM10JL (A, AN, B, BN, C, CN, D, DN, E, EN) $

Input Loading: (4, 4, 4, 4, 4, 4, 4, 4, 4, 4)

DM12JH SPIKE FREE DECODER FOR MOD 12 JOHNSON COUNTER, ACTIVE HI, SEE CM12J DM12JH

LOGIC SYMBOL

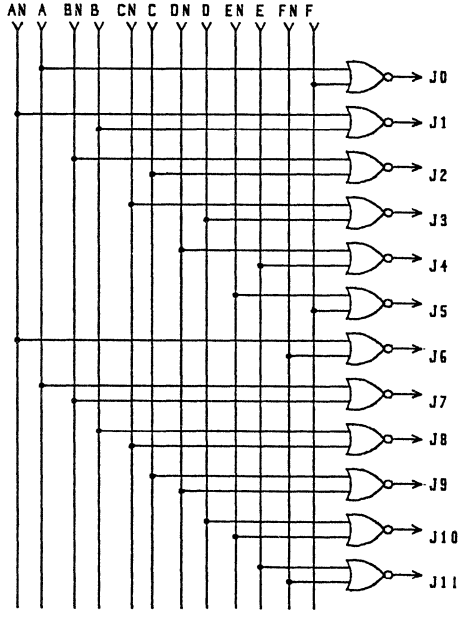


TRUTH TABLE

Q OUTPUT OF THE JOHNSON COUNTER

QA	QB	QC	QD	QE	QF	
0	0	0	0	0	0	J0
1	0	0	0	0	0	J1
1	1	0	0	0	0	J2
1	1	1	0	0	0	J3
1	1	1	1	0	0	J4
1	1	1	1	1	0	J5
1	1	1	1	1	1	J6
0	1	1	1	1	1	J7
0	0	1	1	1	1	J8
0	0	0	1	1	1	J9
0	0	0	0	1	1	J10
0	0	0	0	0	1	J11

LOGIC DIAGRAM



Gates Used: 24 February, 1987

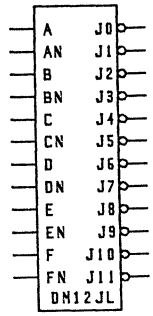
Loading Syntax: Z (J0, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11)

DM12JH (A, AN, B, BN, C, CN, D, DN, E, EN F, FN) $

Input Loading: (4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4)

DM12JL — SPIKE FREE DECODER FOR MOD 12 JOHNSON COUNTER, ACTIVE LO, SEE CM12J — DM12JL

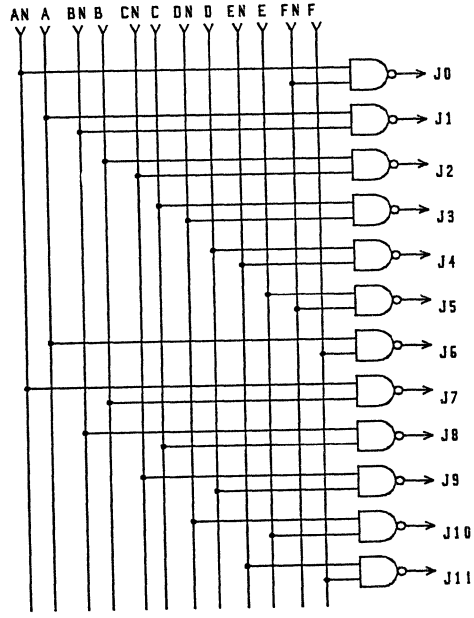
LOGIC SYMBOL



TRUTH TABLE

QA	QB	QC	QD	QE	QF	
0	0	0	0	0	0	J0
1	0	0	0	0	0	J1
1	1	0	0	0	0	J2
1	1	1	0	0	0	J3
1	1	1	1	0	0	J4
1	1	1	1	1	0	J5
1	1	1	1	1	1	J6
0	1	1	1	1	1	J7
0	0	1	1	1	1	J8
0	0	0	1	1	1	J9
0	0	0	0	1	1	J10
0	0	0	0	0	1	J11

LOGIC DIAGRAM



Gates Used: 24 — February, 1987

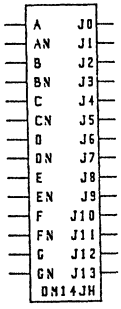
Loading Syntax: Z (J0, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11)

DM12JL (A, AN, B, BN, C, CN, D, DN, E, EN, F, FN) $

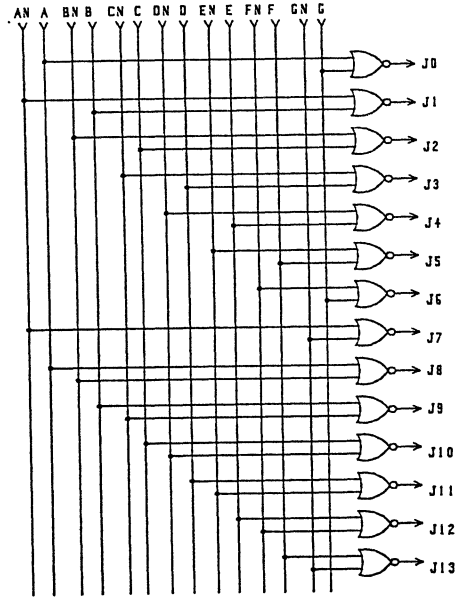
Input Loading: (4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4)

DM14JH	SPIKE FREE DECODER FOR MOD 14 JOHNSON COUNTER, ACTIVE HI, SEE CM14J	DM14JH

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 28 February, 1987

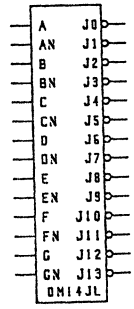
Loading Syntax: Z (J0, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J13)

DM14JH (A, AN, B, BN, C, CN, D, DN, E, EN, F, FN, G, GN) $

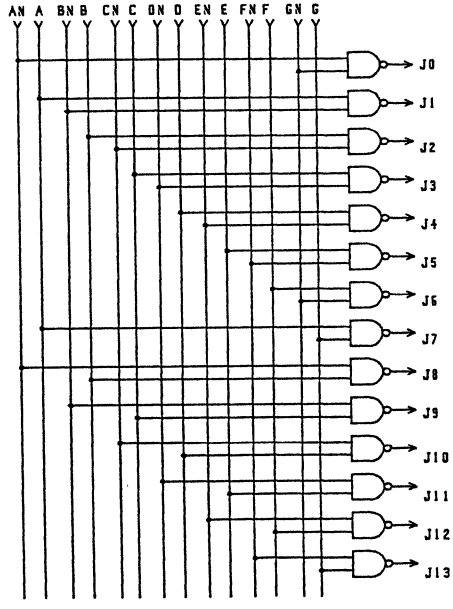
Input Loading: (4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4)

DM14JL	SPIKE FREE DECODER FOR MOD 14 JOHNSON COUNTER, ACTIVE LO, SEE CM14J	DM14JL

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 28 February, 1987

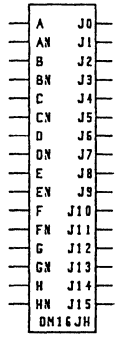
Loading Syntax: Z (J0, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13)

DM14JL (A, AN, B, BN, C, CN, D, DN, E, EN, F, FN, G, GN) $

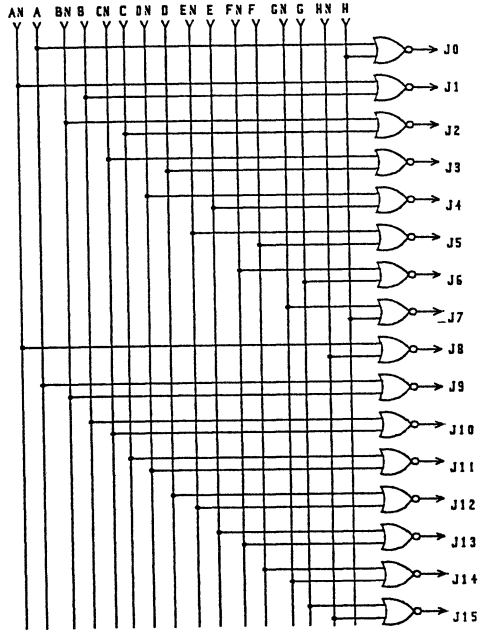
Input Loading: (4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4)

DM16JH	SPIKE FREE DECODER FOR MOD 16 JOHNSON COUNTER, ACTIVE HI, SEE CM16J	DM16JH

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 32 February, 1987

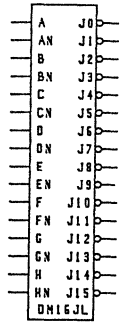
Loading Syntax: Z (J0, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15)

DM16JH (A, AN, B, BN, C, CN, D, DN, E, EN, F, FN, G, GN, H, HN) $

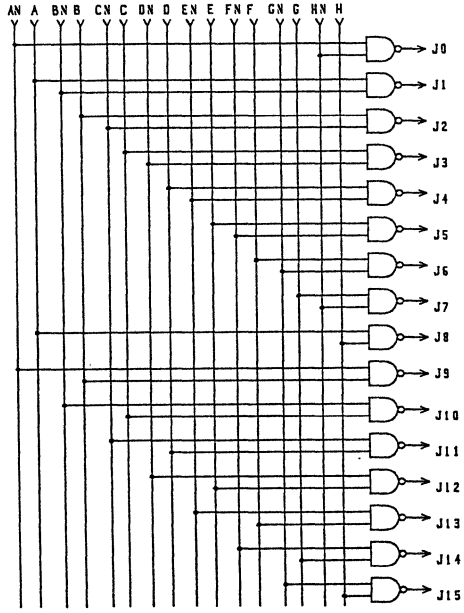
Input Loading: (4, 4,4, 4,4, 4,4, 4,4, 4,4, 4,4, 4,4, 4,4, 4)

DM16JL SPIKE FREE DECODER FOR MOD 16 JOHNSON COUNTER, ACTIVE LO, SEE CM16J DM16JL

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 32 February, 1987

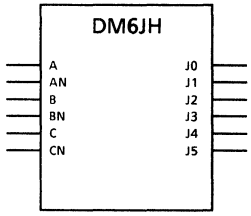
Loading Syntax: Z (J0, J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15)

DM16JL (A, AN, B, BN, C, CN, D, DN, E, EN, F, FN, G, GN, H, HN) $

Input Loading: (4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4, 4)

DM6JH — SPIKE FREE DECODER FOR MOD 6 JOHNSON COUNTER, ACTIVE HI, SEE CM6J — DM6JH

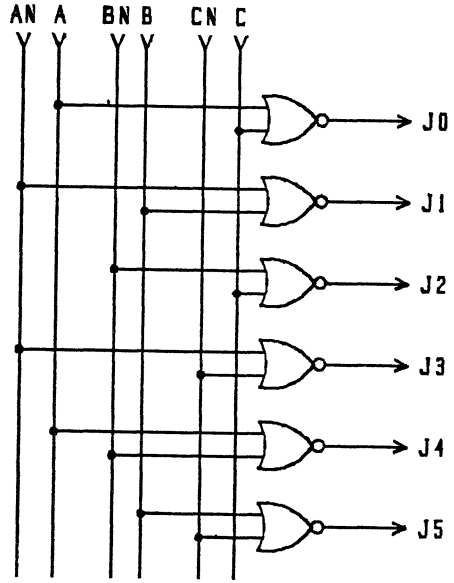
LOGIC SYMBOL



TRUTH TABLE

QA	QB	QC	
0	0	0	J0
1	0	0	J1
1	1	0	J2
1	1	1	J3
0	1	1	J4
0	0	1	J5

LOGIC DIAGRAM



Gates Used: 12 — February, 1987

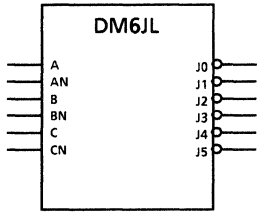
Loading Syntax: Z (J0, J1, J2, J3, J4, J5)

DM6JH (A, AN, B, BN, C, CN) $

Input Loading: (4, 4, 4, 4, 4, 4)

DM6JL — SPIKE FREE DECODER FOR MOD 6 JOHNSON COUNTER, ACTIVE LO, SEE CM6J — DM6JL

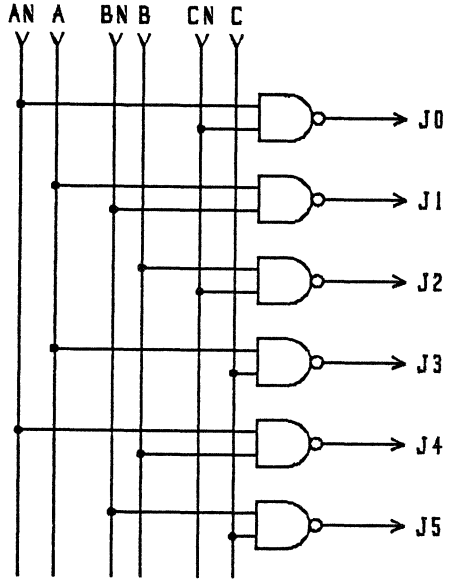
LOGIC SYMBOL



TRUTH TABLE

QA	QB	QC	
0	0	0	J0
1	0	0	J1
1	1	0	J2
1	1	1	J3
0	1	1	J4
0	0	1	J5

LOGIC DIAGRAM



Gates Used: 12 — February, 1987

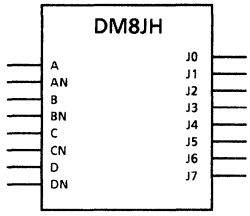
Loading Syntax: Z (J0, J1, J2, J3, J4, J5)

DM6JL (A, AN, B, BN, C, CN) $

Input Loading: (4, 4, 4, 4, 4, 4)

DM8JH — SPIKE FREE DECODER FOR MOD 8 JOHNSON COUNTER, ACTIVE HI, SEE CM8J — DM8JH

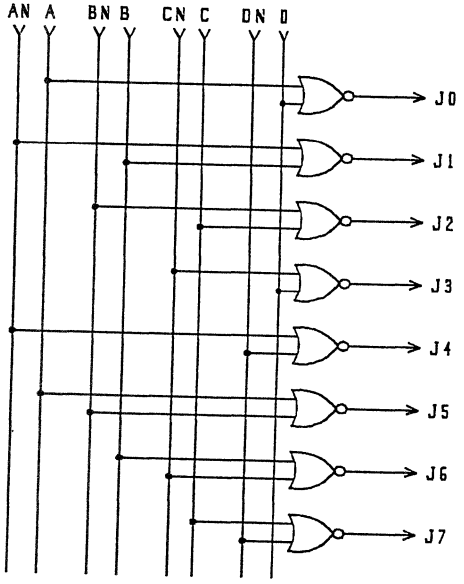
LOGIC SYMBOL



TRUTH TABLE

QA	QB	QC	QD	
0	0	0	0	J0
1	0	0	0	J1
1	1	0	0	J2
1	1	1	0	J3
1	1	1	1	J4
0	1	1	1	J5
0	0	1	1	J6
0	0	0	1	J7

LOGIC DIAGRAM



Gates Used: 16 — February, 1987

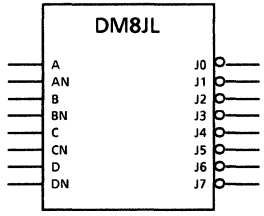
Loading Syntax: Z (J0, J1, J2, J3, J4, J5, J6, J7)

DM8JH (A, AN, B, BN, C, CN, D, DN) $

Input Loading: (4, 4, 4, 4, 4, 4, 4, 4)

DM8JL — SPIKE FREE DECODER FOR MOD 8 JOHNSON COUNTER, ACTIVE LO, SEE CM8J — DM8JL

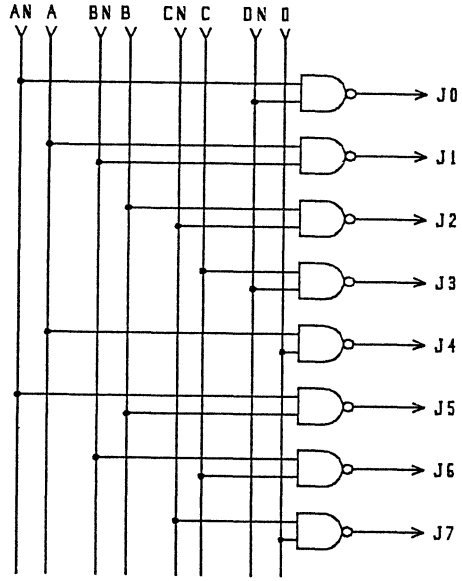
LOGIC SYMBOL



TRUTH TABLE

QA	QB	QC	QD	
0	0	0	0	J0
1	0	0	0	J1
1	1	0	0	J2
1	1	1	0	J3
1	1	1	1	J4
0	1	1	1	J5
0	0	1	1	J6
0	0	0	1	J7

LOGIC DIAGRAM



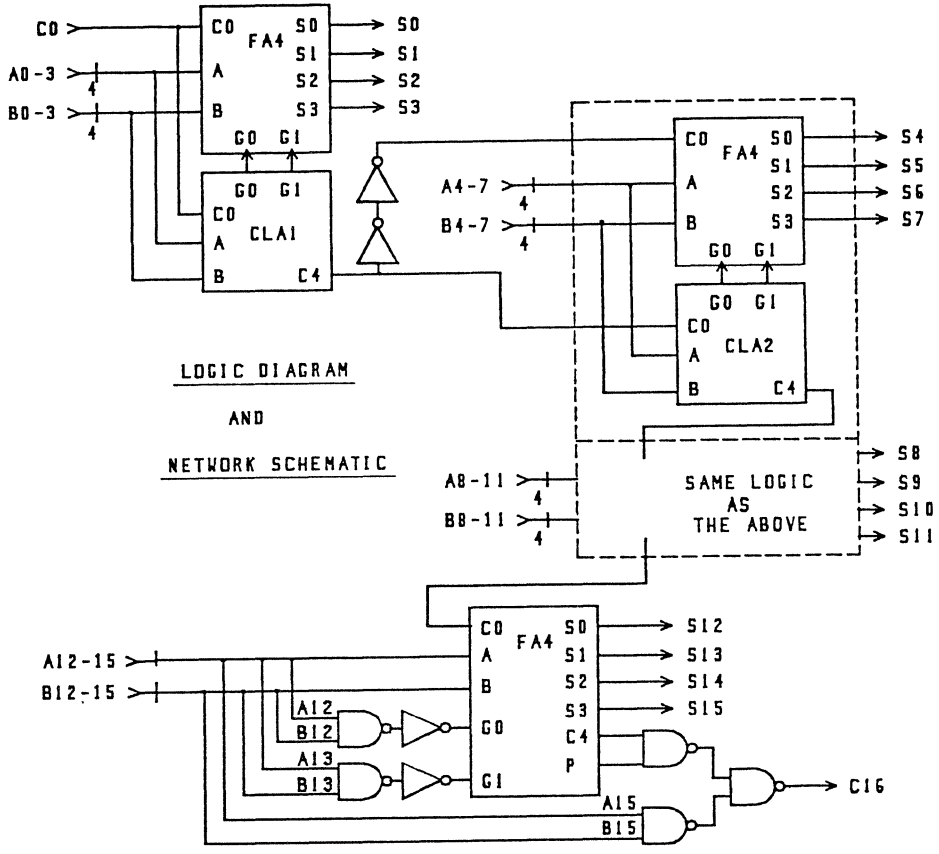
Gates Used: 16 — February, 1987

Loading Syntax: Z (J0, J1, J2, J3, J4, J5, J6, J7)

DM8JL (A, AN, B, BN, C, CN, D, DN) $

Input Loading: (4, 4, 4, 4, 4, 4, 4, 4)

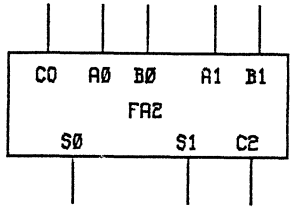
LOGIC DIAGRAM



Gates Used: 277	February, 1987
Coding syntax: Z (S0, S1, S2, S3 S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15, C16)	
= FA16	(C0, A0, B0, A1, B1, A2, B2, A3, B3, A4, B4, A5, B5, A6, B6, A7, B7,
	A8, B8, A9, B9, A10, B10, A11, B11, A12, B12, A13, B13, A14, B14, A15, B15) $
Input loading:	(5, 3, 4, 3, 4, 6, 5, 5, 6, 3, 4, 4, 5, 5, 4, 4, 5,
Input loading:	3, 4, 4, 5, 5, 4, 4, 5, 4, 5, 5, 6, 5, 4, 5, 6)

FA2	2 BIT BINARY FULL ADDER (SAME AS M82C)	FA2

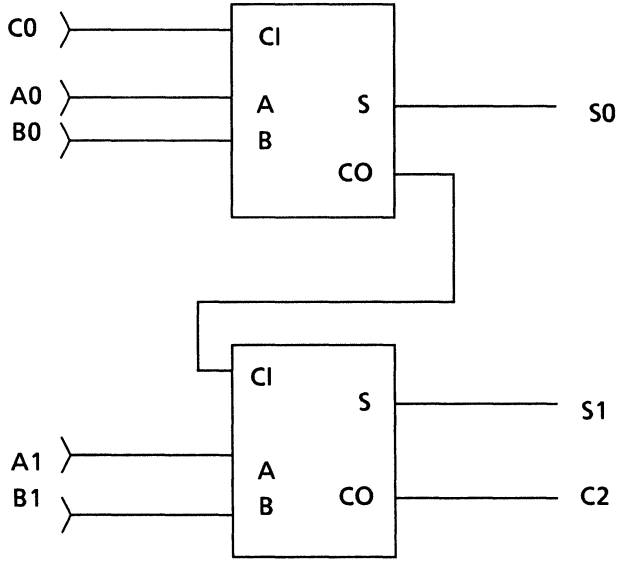
LOGIC SYMBOL



TRUTH TABLE

C0	A0	B0	A1	B1	S0	S1	C2
0 OF 3			0 OF 2	0	0	0	
1 OF 3			0 OF 2	1	0	0	
2 OF 3			0 OF 2	0	1	0	
3 OF 3			0 OF 2	1	1	0	
0 OF 3			1 OF 2	0	1	0	
1 OF 3			1 OF 2	1	1	0	
2 OF 3			1 OF 2	0	0	1	
3 OF 3			1 OF 2	1	0	1	
0 OF 3			2 OF 2	0	0	1	
1 OF 3			2 OF 2	1	0	1	
2 OF 3			2 OF 2	0	1	1	
3 OF 3			2 OF 2	1	1	1	

LOGIC DIAGRAM



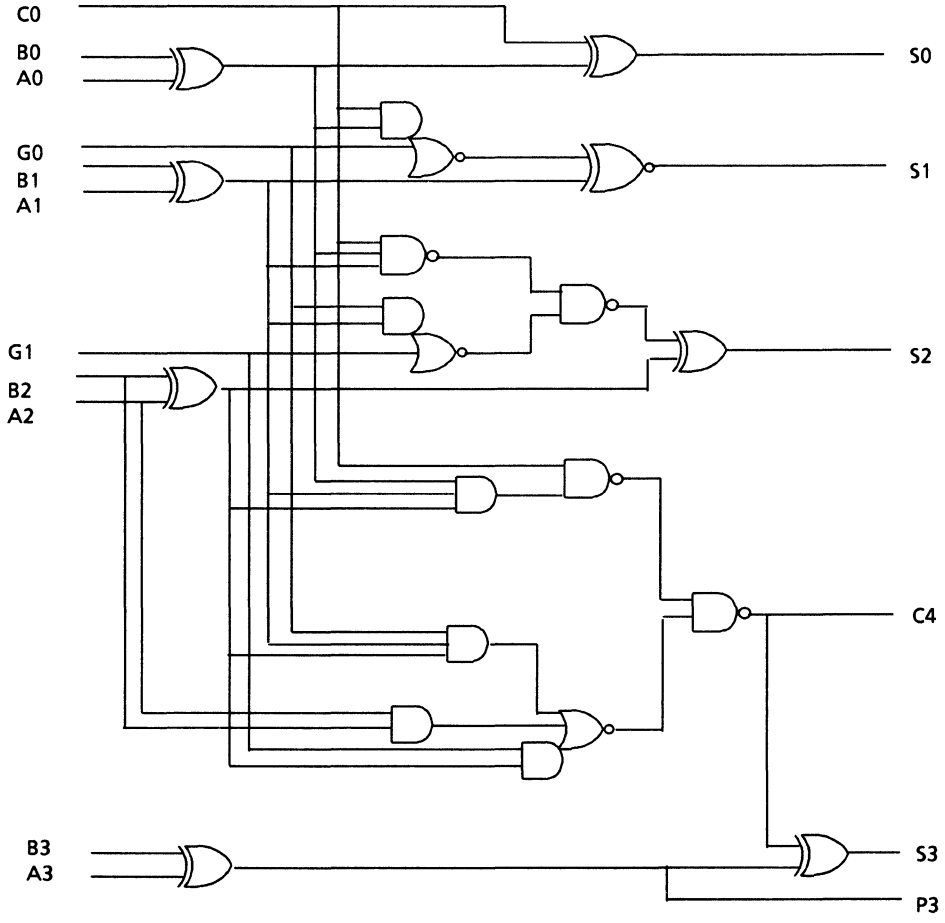
Gates Used: 20 February, 1987

Coding syntax: Z(S0, S1, C2) = FA2 (C0, A0, B0, A1, B1)$

Input Loading: (4, 3, 4, 3, 4)

FA4	4 BIT BINARY FULL ADDER	FA4

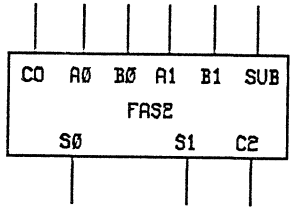
LOGIC DIAGRAM



Gates Used: 50	February, 1987
Coding syntax: Z (S0, S1, S2, S3 C4, P3) = FA4 (C0, A0, B0, G0, A1, B1, G1, B2, A2, A3, B3) $	
Input Loading:	(4, 1, 2, 3, 1, 2, 2, 2, 3, 1, 2)

FAS2 — 2 BIT BINARY FULL ADDER (SAME AS M82C) — FAS2

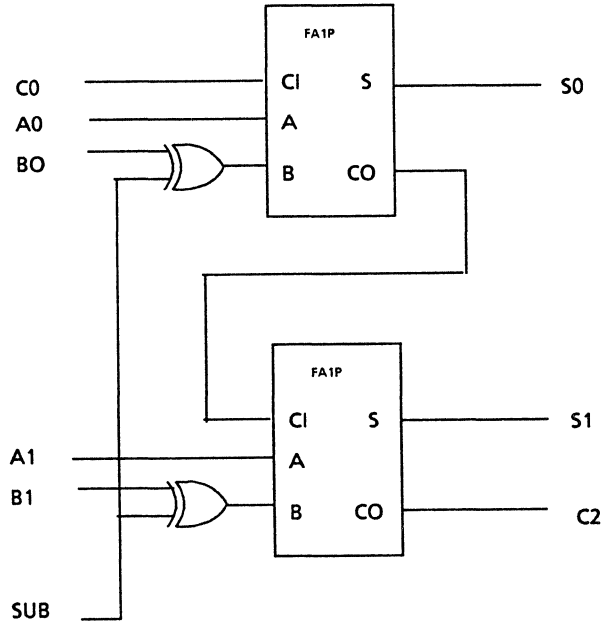
LOGIC SYMBOL



TRUTH TABLE

C0 A0 B0	A1 B1	SUB	S0 S1 C2
		0	SEE FA2
C0 A0 B0	A1 B1	SUB	S0 S1 C2
		1	SEE FA2

LOGIC DIAGRAM



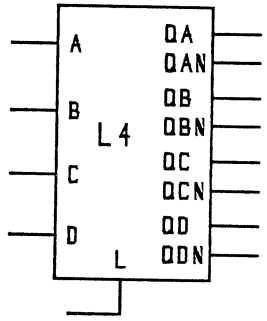
Gates Used: 26 — February, 1987

Coding syntax: Z (S0, S1, C2) = FAS2 (C0, A0, B0, A1, B1, SUB) $

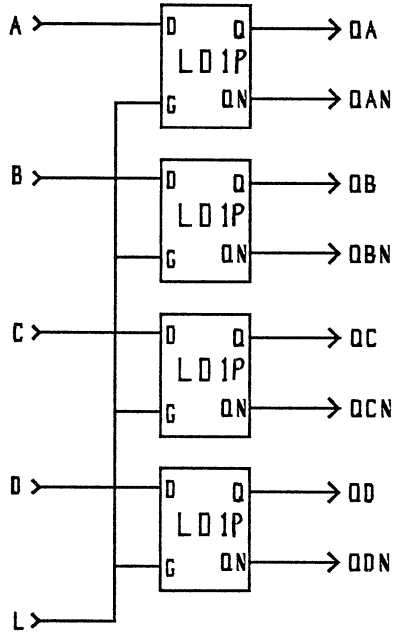
Input Loading: (4, 3, 1, 3, 1, 4)

L4	4 BIT DATA LATCH	L4

LOGIC SYMBOL



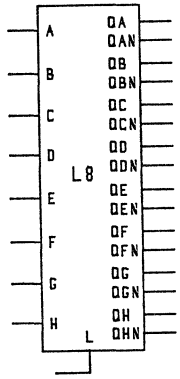
LOGIC DIAGRAM



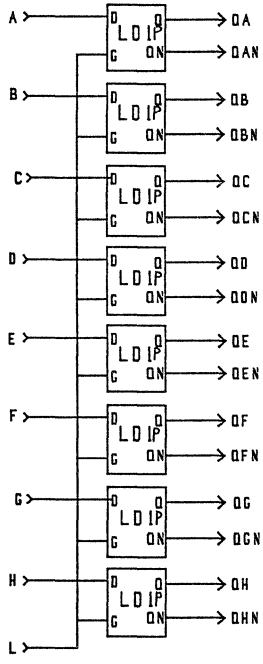
Gates Used: 24	February, 1987
Coding syntax: Z (S0, S1, C2) = L4 (A, B, C, D, L) $	
Input Loading: (1, 1, 1, 1, 4)	

L8 — 8 BIT DATA LATCH — L8

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 48 — February, 1987

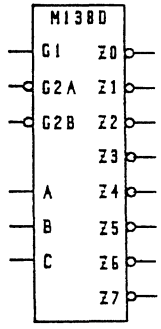
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN) $

= L8 (A, B, C, D, E, F, G, H, L)

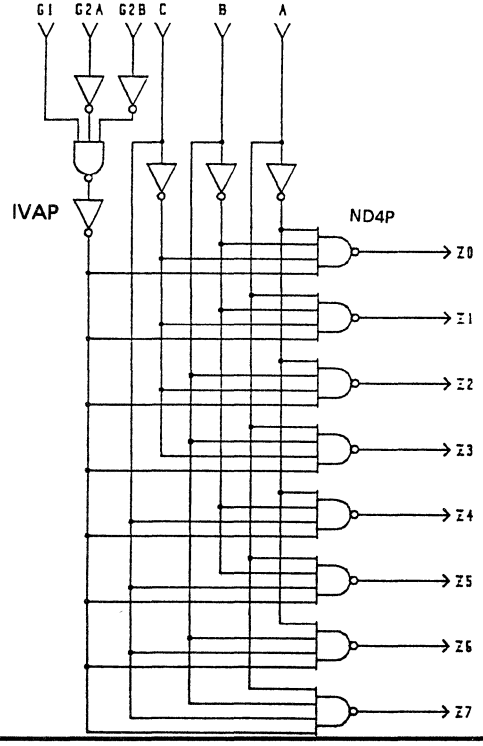
Input Loading: (1, 1, 1, 1, 1, 1, 1, 1, 8)

M138D	GATED 3 TO 8 DECODER OUTPUTS ACTIVE LO (74138)	M138D

LOGIC SYMBOL



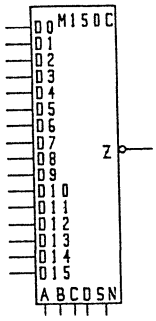
LOGIC DIAGRAM



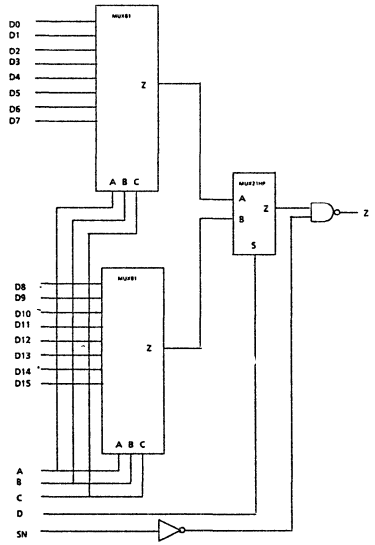
Gates Used: 42	February, 1987
Coding syntax: Z (Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7) = M138D (G1, G2A, G2B, A, B, C)	
Input Loading: (2, 1 .5, 1.5, 2, 2, 2)	

M150C	16 INPUT GATED INVERTING MUX	M150C

LOGIC SYMBOL



LOGIC DIAGRAM



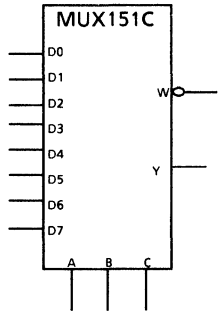
Gates Used: 31 February, 1987

Coding syntax: Z M150C (D0, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, A, B, C, D, SN) $

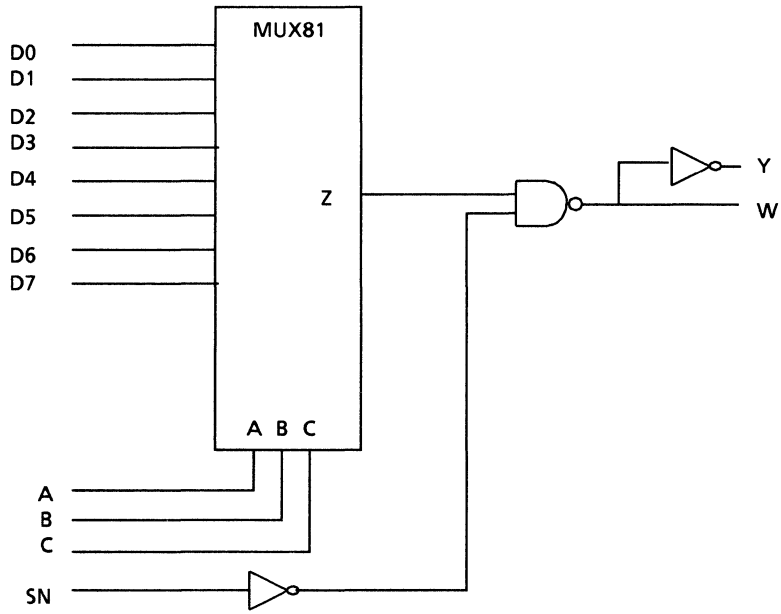
Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 6, 4, 2, 1.5)

M151C	8 INPUT GATED MUX	M151C

LOGIC SYMBOL



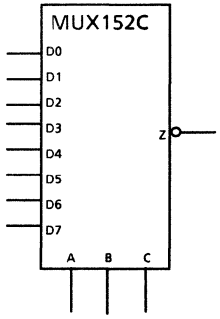
LOGIC DIAGRAM



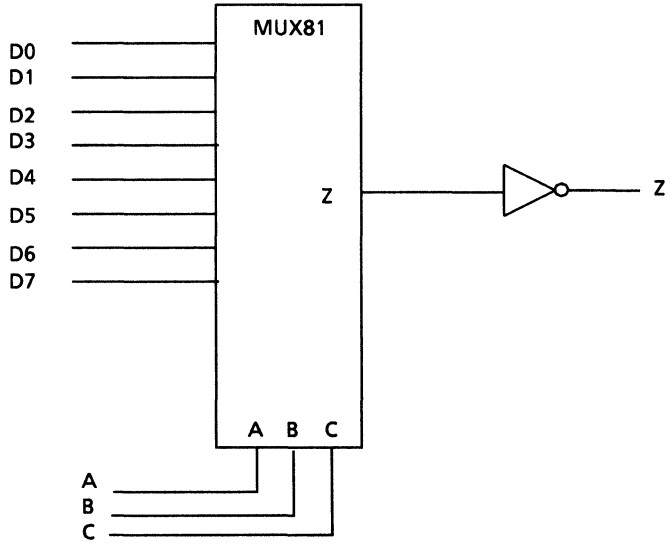
Gates Used: 16	February, 1987
Coding syntax: Z (W,Y) = M151C (D0, D1, D2, D3, D4, D5, D6, D7, A, B, C, SN) $	
Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 1, 3, 2, 1.5)	

M152C	8 INPUT INVERTING MUX	M152C

LOGIC SYMBOL



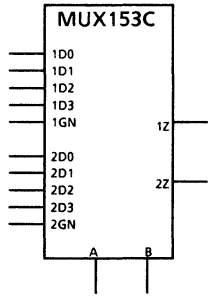
LOGIC DIAGRAM



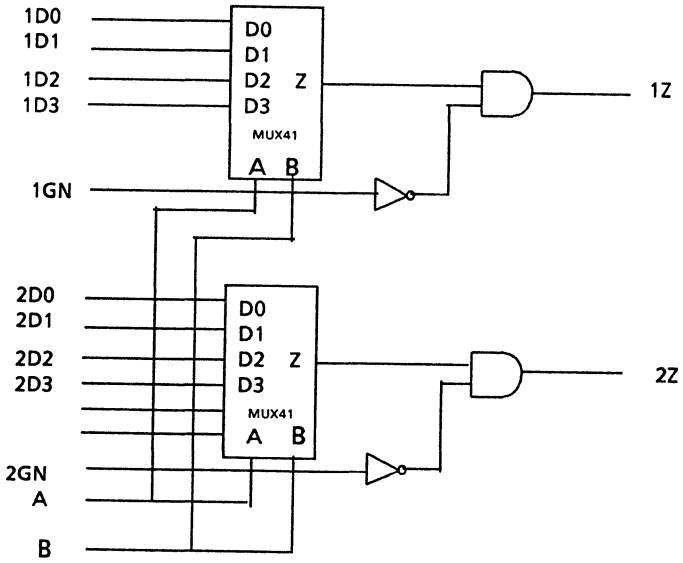
Gates used: 13	February 1987
Coding syntax:	Z = M152C (D0, D1, D2, D3, D4, D5, D6, D7, A, B, C) $
Input Loading:	(2, 2, 2, 2, 2, 2, 2, 2, 1, 3, 2)

M153C DUAL 4 INPUT MUX M153C

LOGIC SYMBOL



LOGIC DIAGRAM



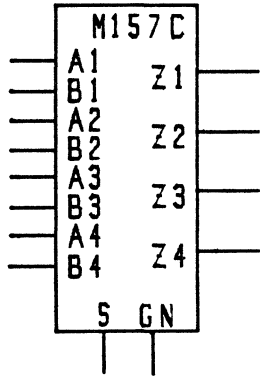
Gates used: 18 February 1987

Coding syntax: X(1Z, 2Z) = M153C (1D0, 1D1, 1D2, 1D3, 2D0, 2D1, 2D2, 2D3, A, B, 1GN, 2GN) $

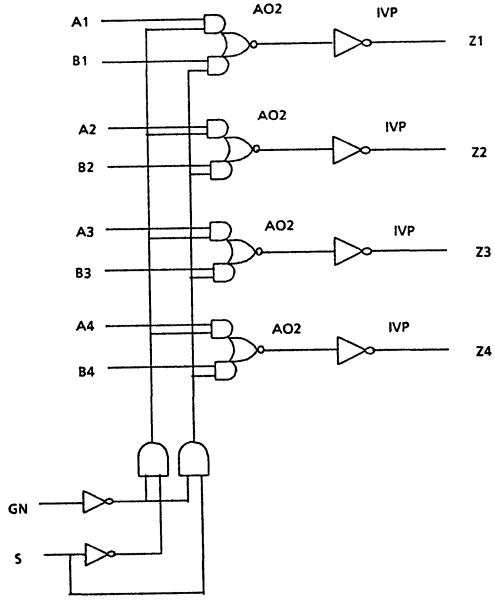
Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 6, 4, 1.5, 1.5)

M157C	QUAD 2 INPUT GATED NON INVERTING MUX	M157C

LOGIC SYMBOL



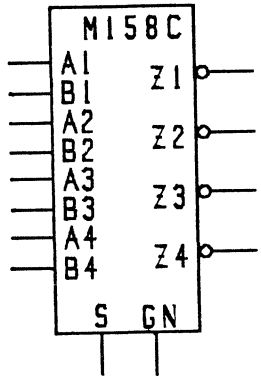
LOGIC DIAGRAM



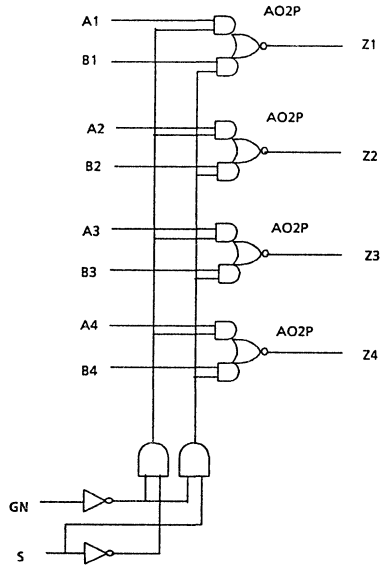
Gates Used: 18	February, 1987
Coding syntax: Y (Z1, Z2, Z3, Z4) = M157C (A1, B1, A2, B2, A3, B3, A4, B4, S, GN) $	
Input Loading:	(1, 1, 1, 1, 1, 1, 1, 1, 2.5, 1.5)

M158C	QUAD 2 INPUT GATED INVERTING MUX	M158C

LOGIC SYMBOL



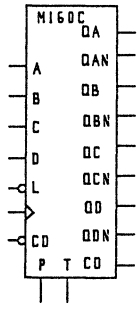
LOGIC DIAGRAM



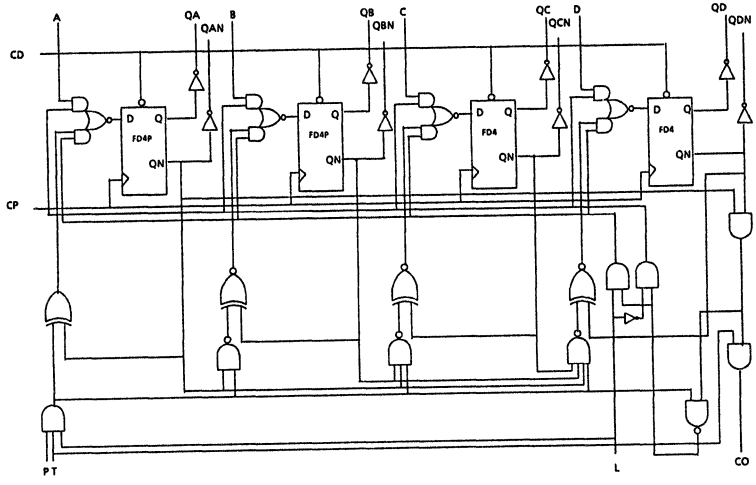
Gates Used: 22	February, 1987
Coding syntax: Y (Z1, Z2, Z3, Z4) = M158C (A1, B1, A2, B2, A3, B3, A4, B4, S, GN) $	
Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 1.5, 1.5)	

M160C	SYNC 4 BIT BCD COUNTER (74LS160)	M160C

LOGIC SYMBOL



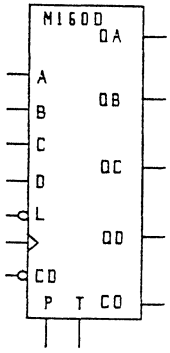
LOGIC DIAGRAM



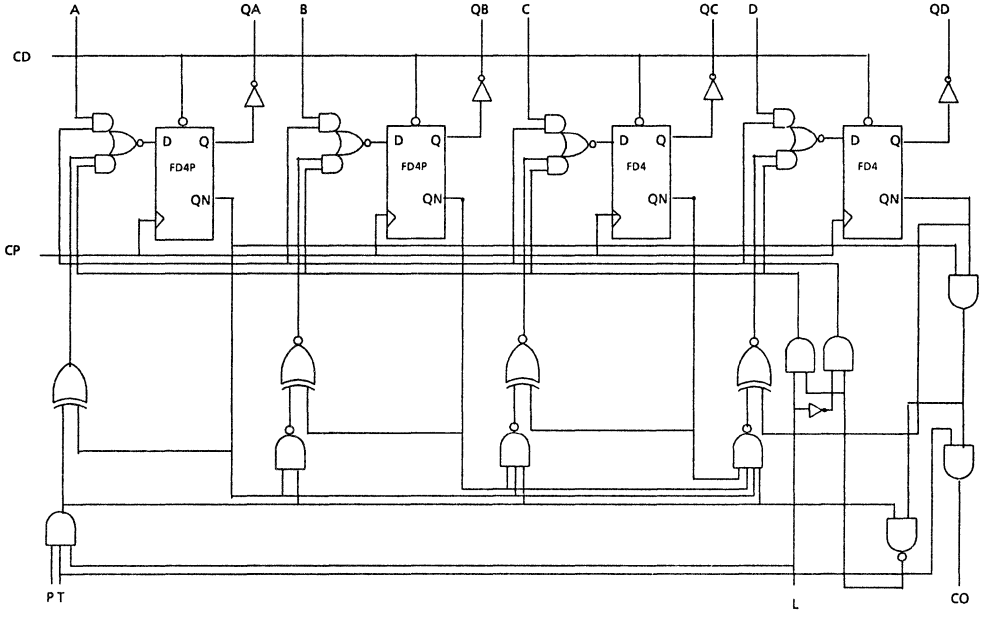
Gates Used: 80	February, 1987
Coding syntax: Z (QA, QB, QC, QD, CD, QAN, QBN, QBN, QCN,QDN)	
= M160C (A, B, C, D, L, CP, CD, P, T) $	
Input Loading: (1, 1, 1, 1, 3.5, 4, 8, 1, 2)	

M160D	SYNC 4 BIT BCD COUNTER (74LS160)	160D

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 76 February, 1987

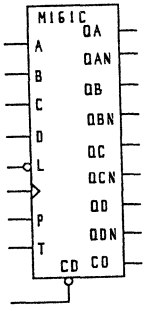
Coding syntax: Z (QA, QB, QC, QD, CO)

= M160D (A, B, C, D, L, CP, CD, P, T) $

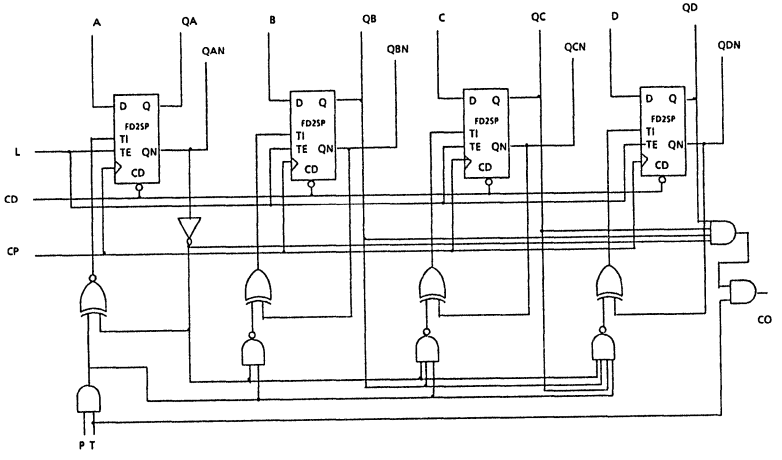
Input Loading: (1, 1, 1, 1, 3.5, 4, 8, 1, 2)

M161C	SYNC 4 BIT COUNTER (74LS161)	M161C

LOGIC SYMBOL



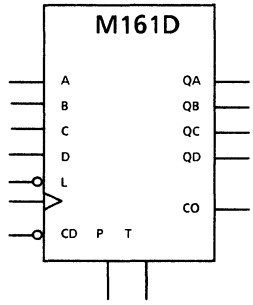
LOGIC DIAGRAM



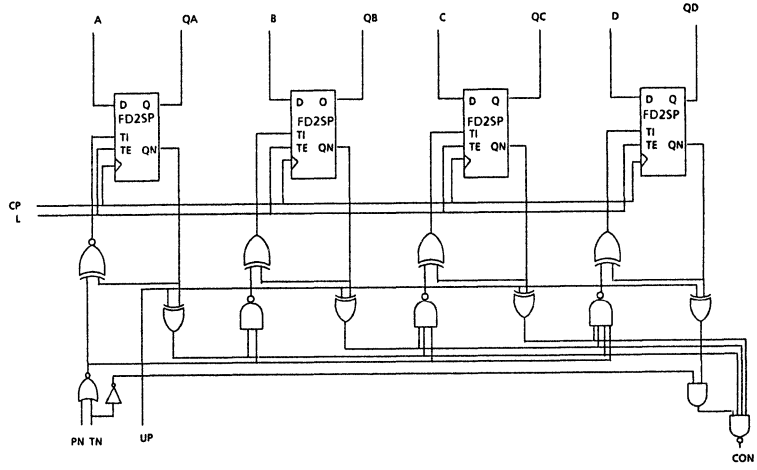
Gates Used: 70	February, 1987
Coding syntax: Z (QA, QB, QC, QD, CO, QAN, QBN, QCN, QDN)	
= M161C (A, B, C, D, L, CP, P, T, CD) $	
Input Loading: (1, 1, 1, 1, 8, 4, 1, 2, 8)	

M161D	SYNC 4 BIT BCD COUNTER (74LS161)	M161D

LOGIC SYMBOL



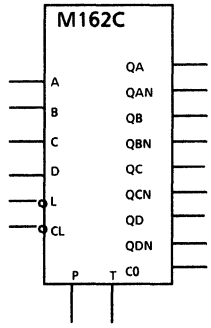
LOGIC DIAGRAM



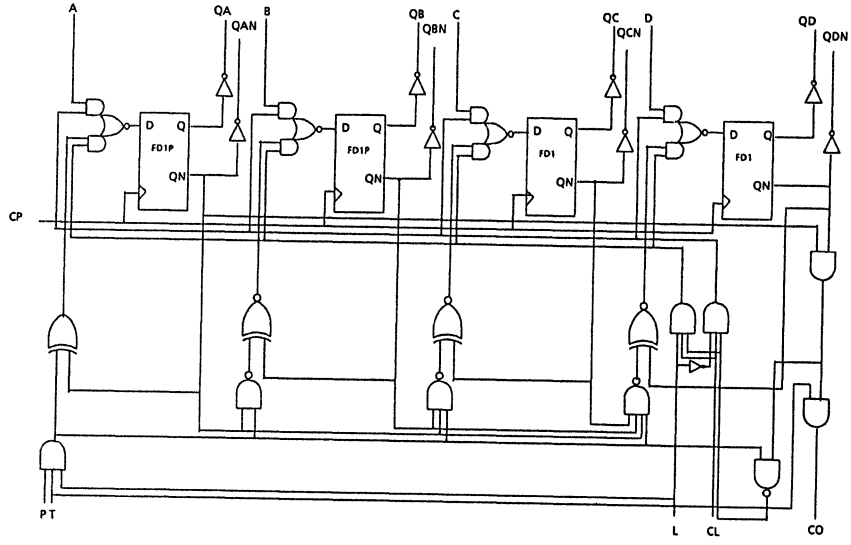
Gates Used: 70	February, 1987
Coding syntax: Z (QA, QB, QC, QD, CO)	
= M161D (A, B, C, D, L, CP, P, T, CD) $	
Input Loading: (1, 1, 1, 1, 8, 4, 1, 2, 8)	

M162C	SYNC 4 BIT BCD COUNTER (74LS162)	M162C

LOGIC SYMBOL



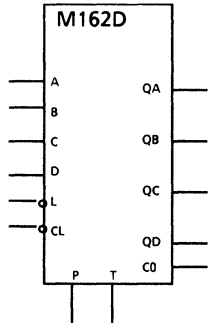
LOGIC DIAGRAM



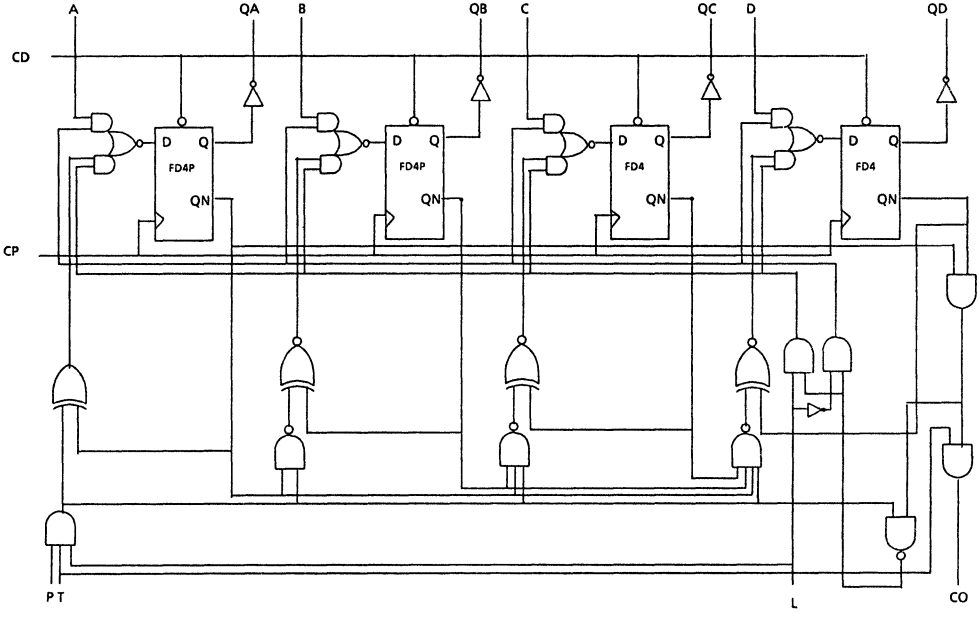
Gates Used: 78	February, 1987
Coding syntax: Z (QA, QB, QC, QD, CO)	
= M162D (A, B, C, D, L, CL, CP, P, T) $	
Input Loading: (1, 1, 1, 1, 3.5, 2, 4, 1, 2)	

M162D	SYNC 4 BIT BCD COUNTER (74LS162)	M162D

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 74 February, 1987

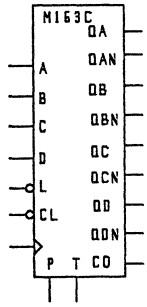
Coding syntax: Z (QA, QB, QC, QD, CO)

= M162D (A, B, C, D, L, CL, CP, P, T) $

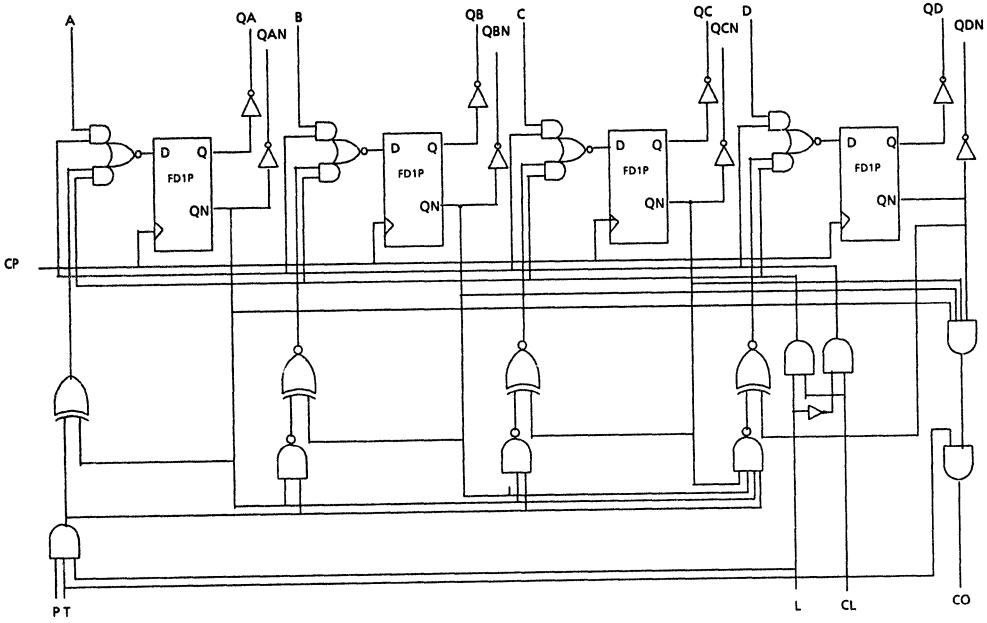
Input Loading: (1, 1, 1, 1, 3.5, 2, 4, 1, 2)

M163C	SYNC 4 BIT BCD COUNTER (74LS163)	M163C

LOGIC SYMBOL



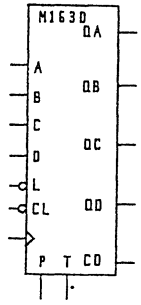
LOGIC DIAGRAM



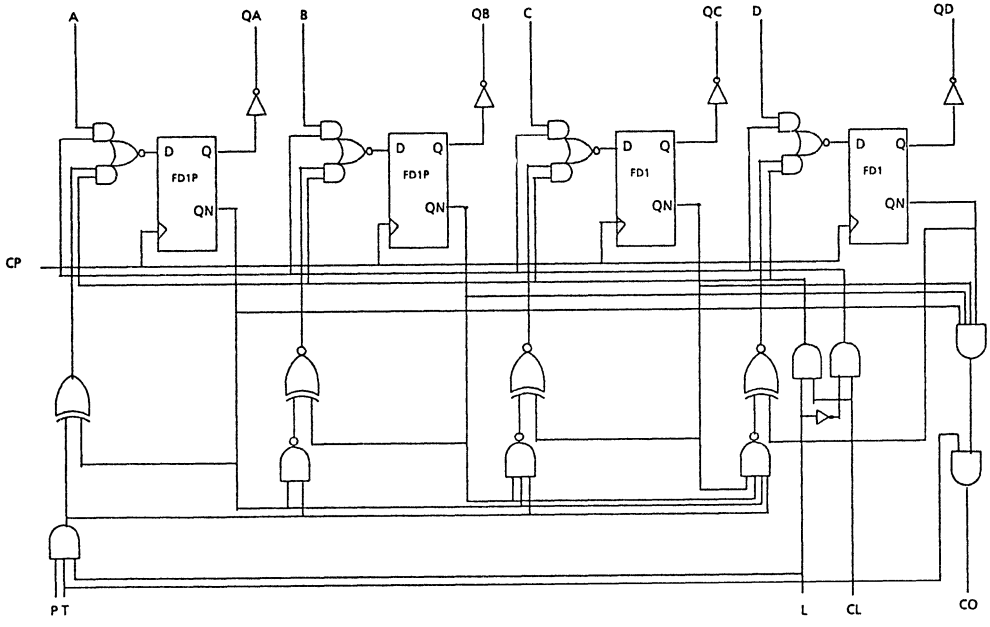
Gates Used: 78	February, 1987
Coding syntax: Z (QA, QB, QC, QD, CO, QAN, QBN, QCN, QDN)	
= M163C (A, B, C, D, L, CL, CP, P, T) $	
Input Loading: (1, 1, 1, 1, 3.5, 2, 4, 1, 2)	

M163D	SYNC 4 BIT COUNTER (74LS163)	M163D

LOGIC SYMBOL



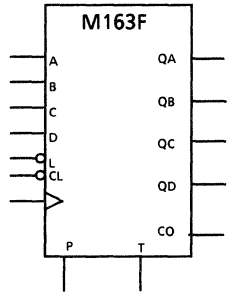
LOGIC DIAGRAM



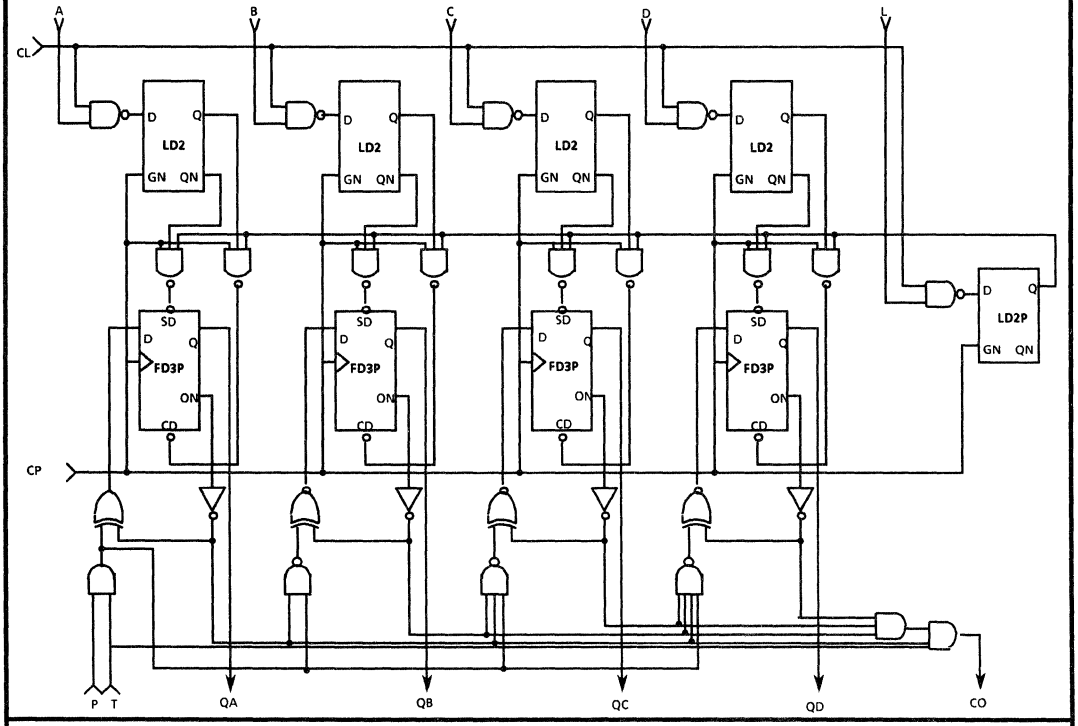
Gates Used: 72	February, 1987
Coding syntax: Z (QA, QB, QC, QD, CO)	
= M163D (A, B, C, D, L, CL, CP, P, T) $	
Input Loading: (1, 1, 1, 1, 3.5, 2, 4, 1, 2)	

M163F	SYNC 4 BIT COUNTER	M163F
	(74LS163) OPTIMIZED FOR MAX CLOCK FREQ	

LOGIC SYMBOL



LOGIC DIAGRAM



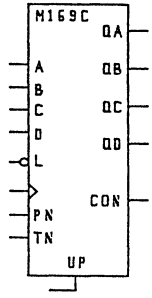
Gates Used: 115 February, 1987

Coding syntax: Z (QA, QB, QC, QD, CO) = M163 (A, B, C, D, L, CL, CP, P, T) $

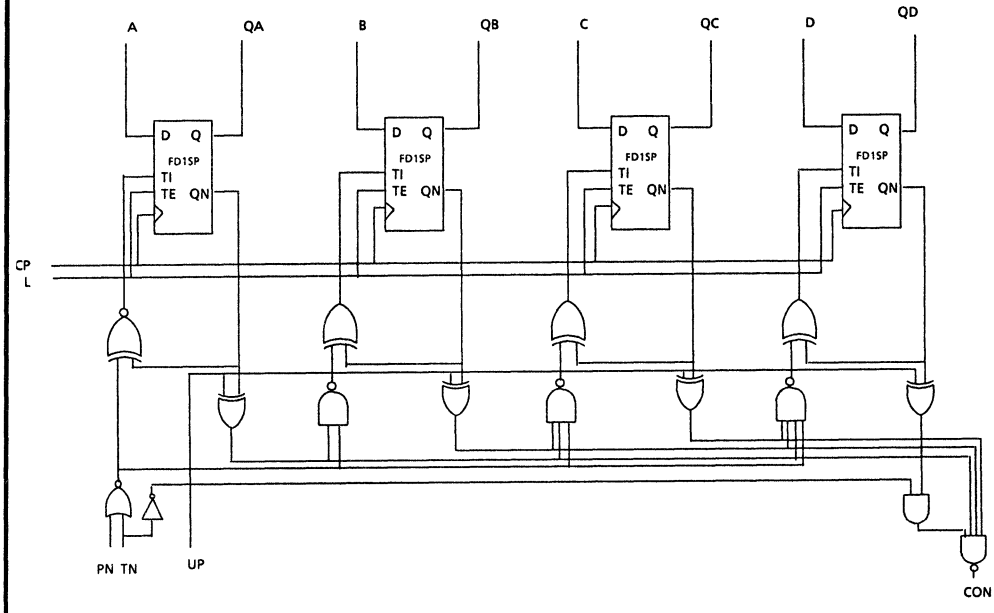
Input Loading: (1, 1, 1, 1, 1, 5, 16, 1, 2)

M169C	4 BIT U/D COUNTER (74LS169)	M169C

LOGIC SYMBOL



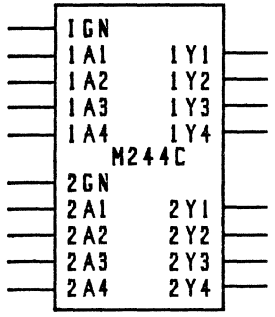
LOGIC DIAGRAM



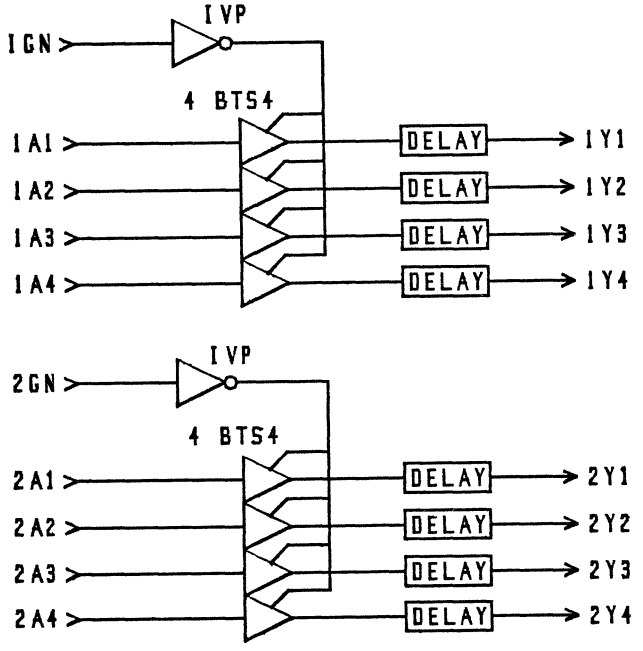
Gates Used: 77	February, 1987
Coding syntax: Z (QA, QB, QC, QD, CON) = M169C (A, B, C, D, L, CP, PN, TN, UP) $	
Input Loading:	(1, 1, 1, 1, 8, 4, 2, 3.5, 4)

M244C	DUAL 4 BIT THREE-STATE BUFFER ON CHIP	M244C

LOGIC SYMBOL



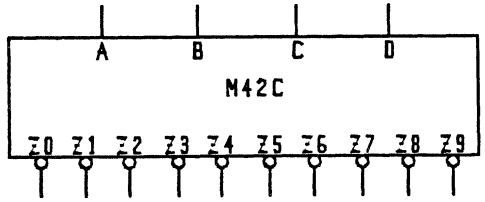
LOGIC DIAGRAM



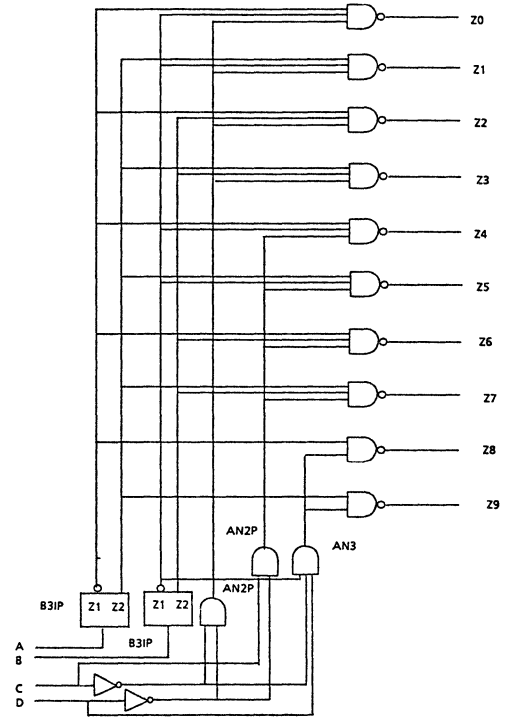
Gates Used: 36	February, 1987
Coding syntax: Z (1Y1, 1Y2, 1Y3, 1Y4, 2Y1, 2Y2, 2Y3, 2Y4)	
= M244C (1A1, 1A2, 1A3, 1A4, 2A1, 2A2, 2A3, 2A4, 1GN, 2GN) $	
Input Loading: (2, 2, 2 , 2, 2, 2, 2, 2, 3, 3)	

M42C	4 TO 10 DECODER	M42C

LOGIC SYMBOL



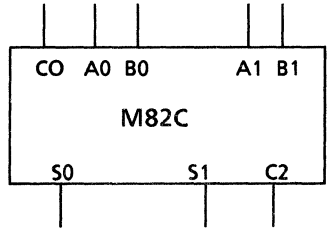
LOGIC DIAGRAM



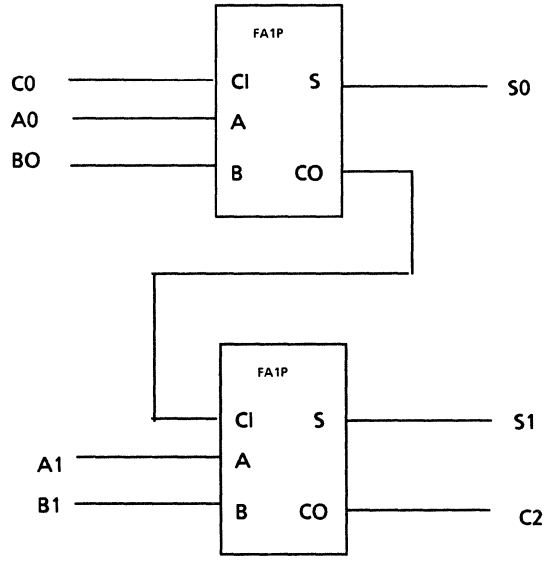
Gates Used: 44	February, 1987
Coding syntax: Y (Z0, Z1, Z2, Z3, Z4, Z5, Z6, Z7, Z8, Z9) = M42C (A, B, C, D)	
Input Loading:	(4, 4, 2.5, 2.5)

M82C	2 BIT BINARY FULL ADDER (SAME AS FA2)	M82C

LOGIC SYMBOL



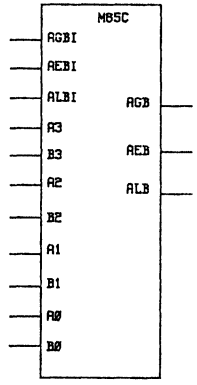
LOGIC DIAGRAM



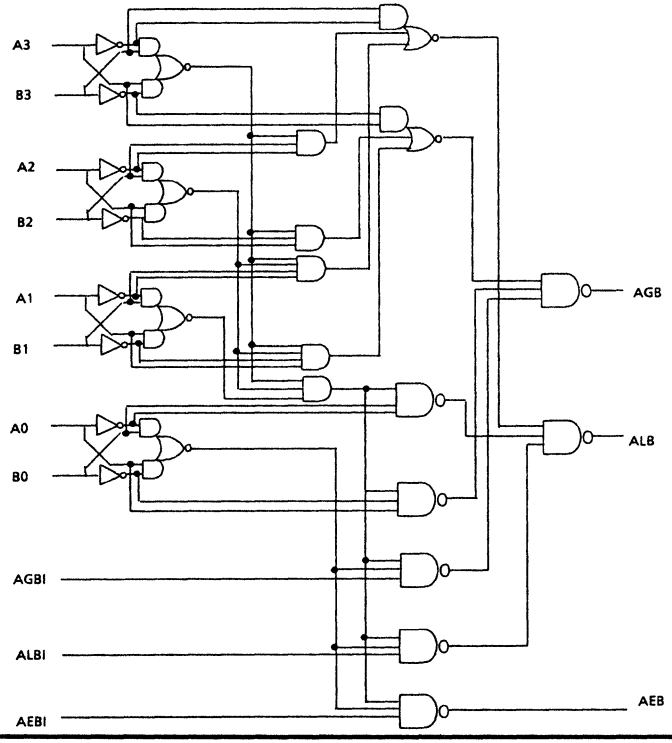
Gates Used: 20	February, 1987
Coding syntax: Z (S0, S1, C2) = M82C (C0, A0, B0, A1, B1) $	
Input Loading: (4, 3, 4, 3, 4)	

M85C — 4 BIT MAGNITUDE COMPARATOR EXPANDABLE (SIMILIAR TO MAG4) — M85C

LOGIC SYMBOL



LOGIC DIAGRAM



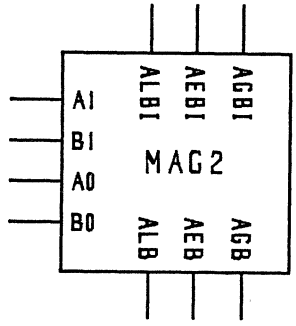
Gates Used: 50 — February, 1987

Coding syntax: Z (AGB, AEB, ALB) = M85C (AGBI, AEBI, ALBI, A3, B3, A2, B2, A1, B1, A0, B0)

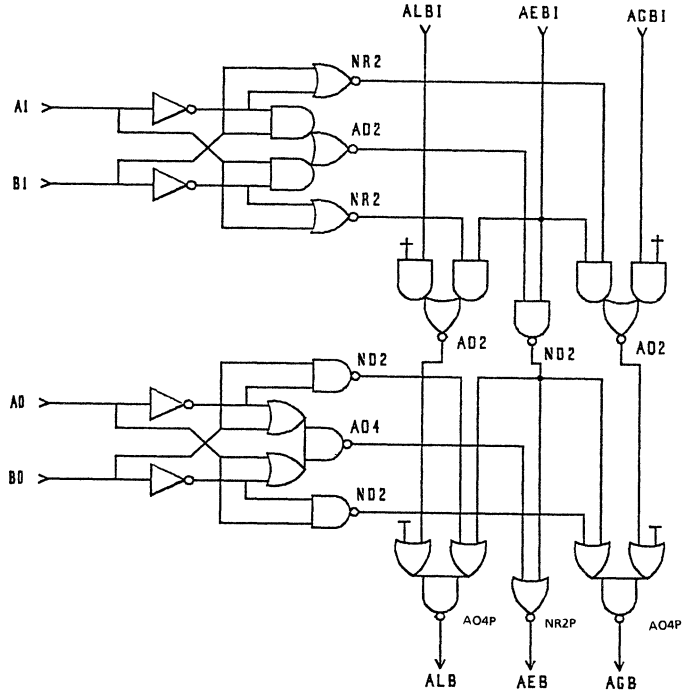
Input Loading: (1, 1, 1, 4.8, 3.5, 4.5, 3.5, 4.5, 3.5, 4.5, 3.5)

MAG2	2 BIT EXTENDABLE MAGNITUDE COMPARATOR	MAG2

LOGIC SYMBOL



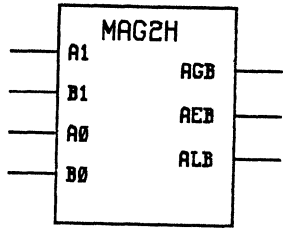
LOGIC DIAGRAM



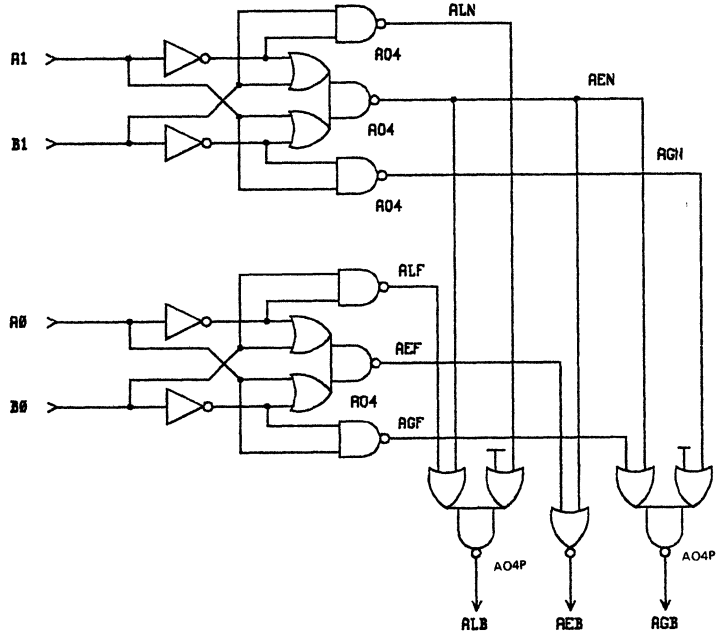
Gates Used: 27	February, 1987
Coding syntax: Z (AGB, AEB, ALB) MAG2 (AGBI, AEBI, ALBI, A1, B1, A0, B0) $	
Input Loading:	(1, 1, 1, 3.5, 3.5, 3.5, 3.5)

MAG2H	2 BIT MAGNITUDE COMPARATOR	MAG2H

LOGIC SYMBOL



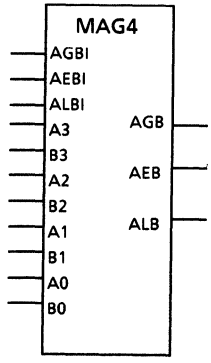
LOGIC DIAGRAM



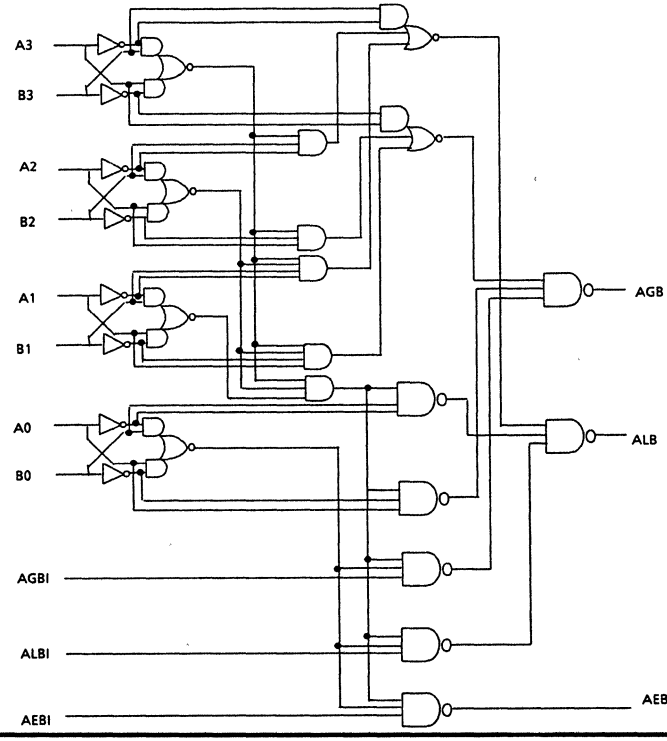
Gates Used: 22	February, 1987
Coding syntax: Z (AGB, AEB, ALB) MAG2H (A1, B1, A0, B0) $	
Input Loading:	(3.5, 3.5, 3.5, 3.5)

MAG4	4 BIT MAGNITUDE COMPARATOR EXPANDABLE (SAME AS M85C)	MAG4

LOGIC SYMBOL



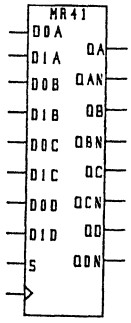
LOGIC DIAGRAM



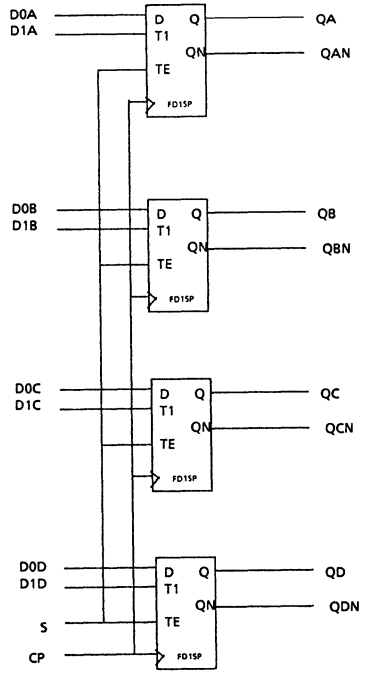
Gates Used: 50	February, 1987
Coding syntax: Z (AGB, AEB, ALB) MAG4 (AGBI, AEBI, ALBI, A3, B3, A2, B2, A1, B1, A0, B0)$	
Input Loading: (1, 1, 1, 4.8, 3.5, 4.5, 3.5, 4.5, 3.5,4.5, 3.5)	

MR41 — 4 BIT REGISTER WITH 2 BIT MULTIPLEXED INPUTS — MR41

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 40 — February, 1987

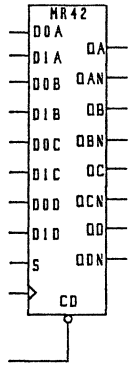
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN QD, QDN)

MR41 (D0A, D1A, D0B, D1B, D0C, D1C, D0D, D1D, S, CP) $

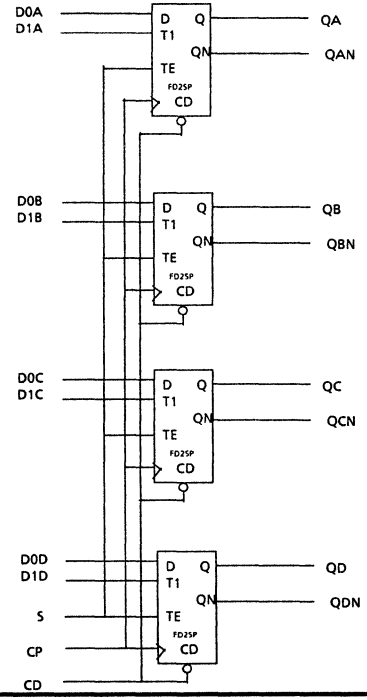
Input Loading: (1, 1, 1, 1, 1, 1, 1, 1, 8, 4)

MR42	4 BIT REGISTER WITH 2 BIT MULTIPLEXED INPUTS, CLEAR DIRECT	MR42

LOGIC SYMBOL



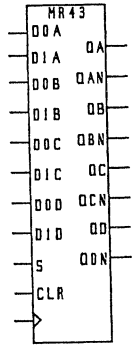
LOGIC DIAGRAM



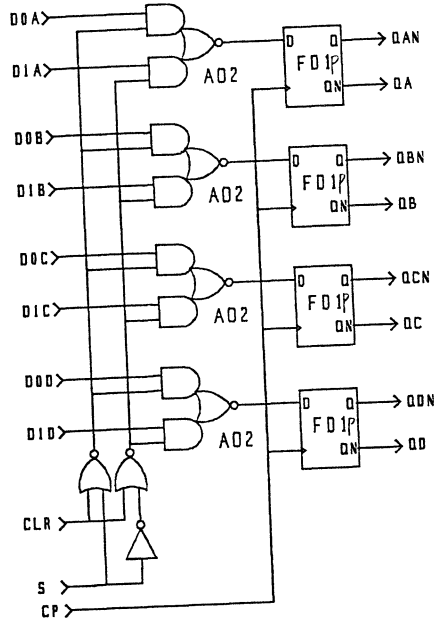
Gates Used: 44	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN QD, QDN)	
MR42 (D0A, D1A, D0B, D1B, D0C, D1C, D0D, D1D, S, CP, CD) $	
Input Loading:	(1, 1, 1, 1, 1, 1, 1, 1, 8, 4, 8)

MR43	4 BIT REGISTER WITH 2 BIT MULTIPLEXED INPUTS, SYNC CLEAR	MR43

LOGIC SYMBOL



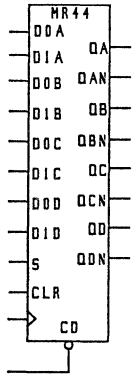
LOGIC DIAGRAM



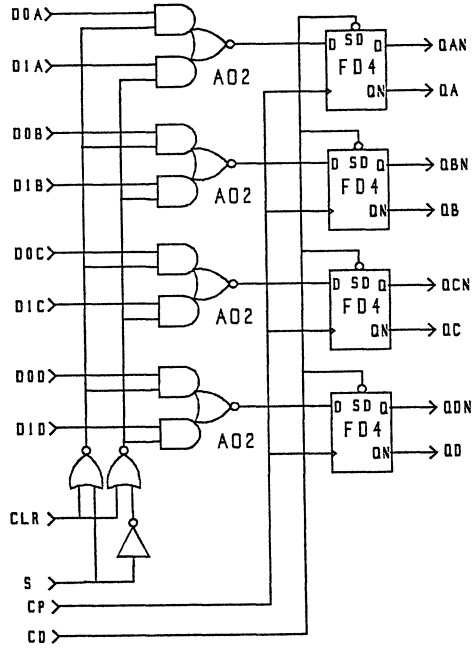
Gates Used: 45	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN QD, QDN)	
MR43 (D0A, D1A, D0B, D1B, D0C, D1C, D0D, D1D, S, CLR, CD) $	
Input Loading: (1, 1, 1, 1, 1, 1, 1, 1, 3.5, 4, 4)	

MR44 — 4 BIT REGISTER WITH 2 BIT MULTIPLEXED INPUTS, SYNC CLEAR CD — MR44

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 49 — February, 1987

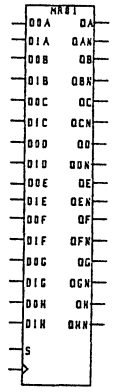
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN QD, QDN)

MR44 (D0A, D1A, D0B, D1B, D0C, D1C, D0D, D1D, S, CLR, CP, CD) $

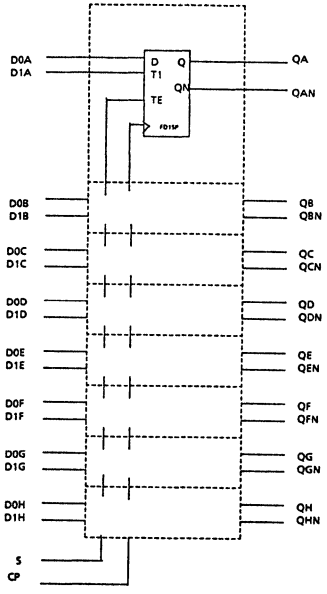
Input Loading:	(1, 1, 1, 1, 1, 1, 1, 1, 3.5, 4, 4, 8)

MR81	8 BIT REGISTER WITH 2 BIT MULTIPLEXED INPUTS	MR81

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 80 February, 1987

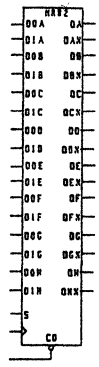
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN)

MR81 (D0A, D1A, D0B, D1B, D0C, D1C, D0D, D1D, D0E, D1E, D0F, D1F, D0G, D1G, D0H, D1H, S, CP) $

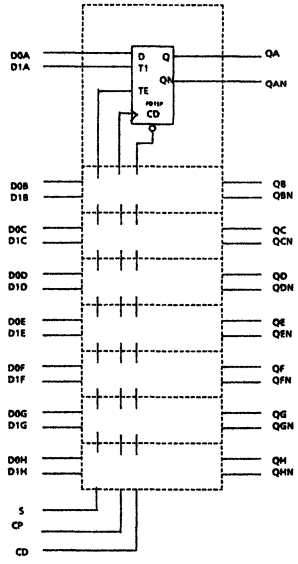
Input Loading: (1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 16, 8)

MR82	8 BIT REGISTER WITH 2 BIT MULTIPLEXED INPUTS CLEAR DIRECT	MR82

LOGIC SYMBOL



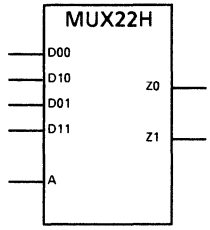
LOGIC DIAGRAM



Gates Used: 88	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN)	
MR82 (D0A, D1A, D0B, D1B, D0C, D1C, D0D, D1D, D0E, D1E, D0F, D1F, D0G, D1G,	
D0H, D1H, S, CP, CD) $	
Input Loading: (1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1,	
1, 1, 16, 8)	

MUX22H	DUAL 2 BIT NON INVERTING MUX	MUX22H

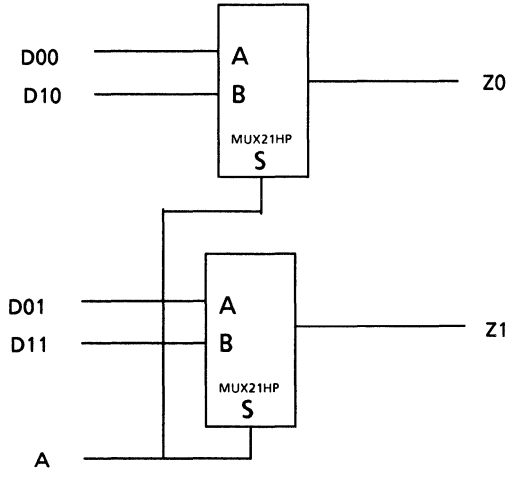
LOGIC SYMBOL



TRUTH TABLE

A	Z (I)
0	D0 (I)
1	D1 (I)

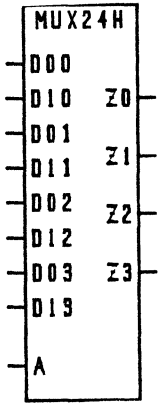
LOGIC DIAGRAM



Gates Used: 8	February, 1987
Coding syntax: Y(Z0, Z1) = MUX22H (D00, D10, D01, D11, A) $	
Input Loading: (1, 1, 1, 1, 4)	

MUX24H	QUAD 2 BIT NON INVERTING MUX	MUX24H

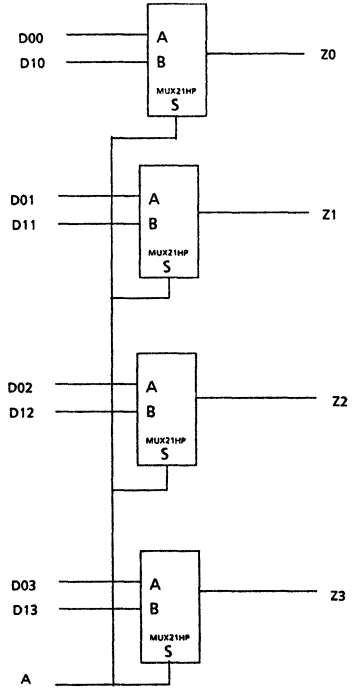
LOGIC SYMBOL



TRUTH TABLE

A	Z(I)
0	D0(I)
1	D1(I)

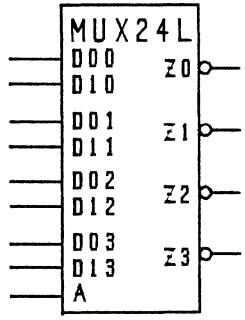
LOGIC DIAGRAM



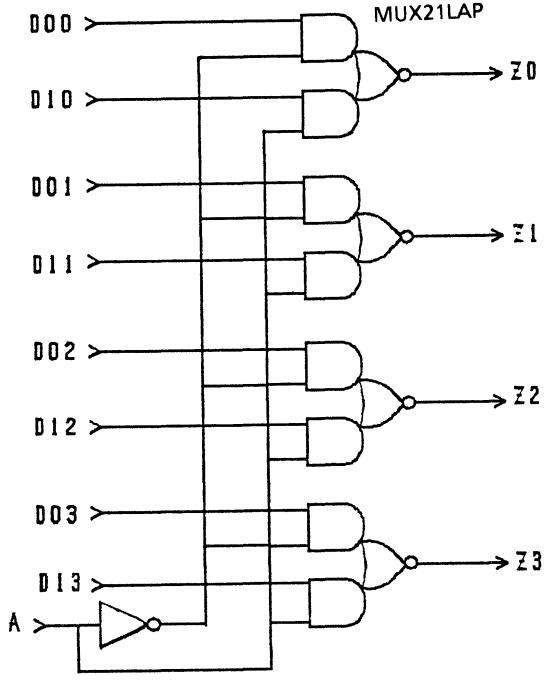
Gates Used: 16	February, 1987
Coding syntax: Y(Z0, Z1, Z2, Z3) =	MUX24H (D00, D10, D01, D11, D02, D12, D03, D13, A) $
Input Loading:	(1, 1, 1, 1, 1, 1, 1, 1, 8)

MUX24L	QUAD 2 BIT INVERTING MUX	MUX24L

LOGIC SYMBOL



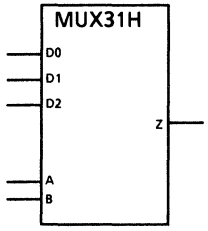
LOGIC DIAGRAM



Gates Used: 9	February, 1987
Coding syntax: Z(Z0, Z1, Z2, Z3) =	MUX24L (D00, D10, D01, D11, D02, D12, D03, D13, A) $
Input Loading:	(1, 1, 1, 1, 1, 1, 1, 1, 6)

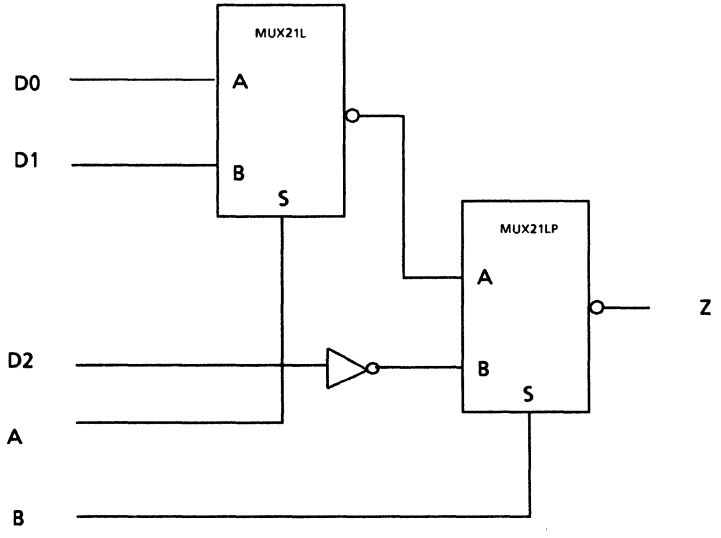
MUX31H	QUAD 2 BIT NON INVERTING MUX	MUX31H

LOGIC SYMBOL



A	B	Z
0	0	D0
1	0	D1
0	1	D2
1	1	D2

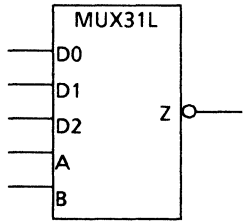
LOGIC DIAGRAM



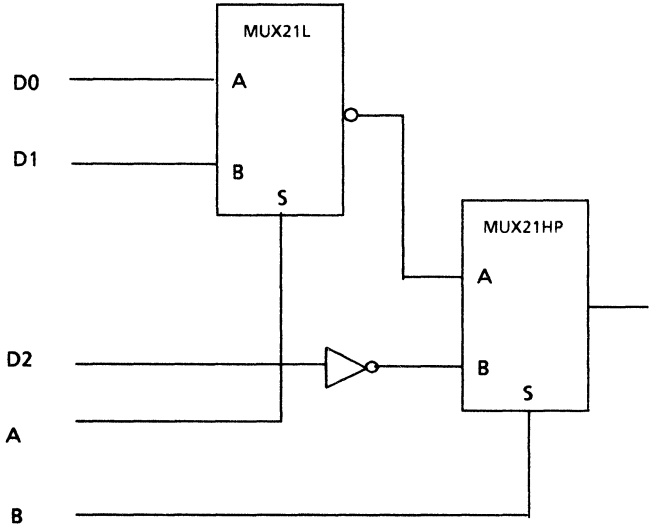
Gates Used: 8	February, 1987
Coding syntax:	Z = MUX31H (D0, D1, D2, A, B) $
Input Loading:	(2, 2, 1.5, 2, 2)

MUX31L	3 BIT INVERTING MUX	MUX31L

LOGIC SYMBOL



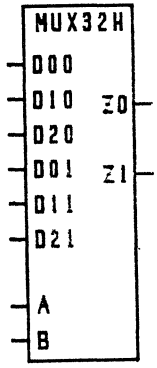
LOGIC DIAGRAM



Gates Used: 8		February, 1987
Coding syntax:	Z = MUX31H (D0, D1, D2, A, B) $	
Input Loading:	(2, 2, 1.5, 2, 2)	

MUX32H	DUAL 3 BIT NON INVERTING MUX	MUX32H

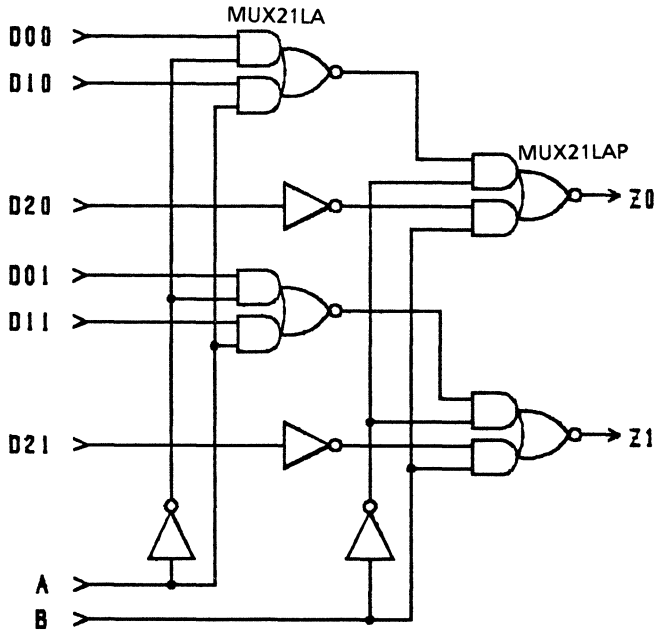
LOGIC SYMBOL



TRUTH TABLE

A	B	Z(I)
0	0	D0(I)
1	0	D1(I)
0	1	D2(I)
1	1	D2(I)

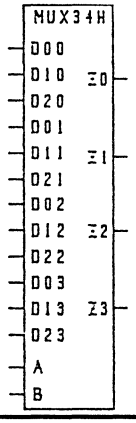
LOGIC DIAGRAM



Gates Used: 12		February, 1987
Coding syntax:	Y(Z0, Z1) = MUX32H (D00, D01, D20, D01, D11, D21, A, B) $	
Input Loading:	(2, 2, 1.5, 2, 2, 1.5, 3.5, 3.5)	

MUX34H	QUAD 3 BIT NON INVERTING MUX	MUX34H

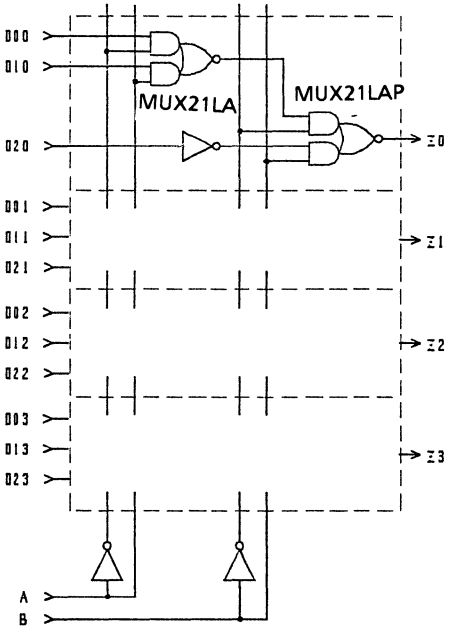
LOGIC SYMBOL



TRUTH TABLE

A	B	Z(I)
0	0	D0(I)
1	0	D1(I)
0	1	D2(I)
1	1	D2(I)

LOGIC DIAGRAM



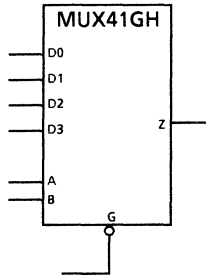
Gates Used: 22 February, 1987

Coding syntax: Y(Z0, Z1, Z2, Z3) = MUX34H (D00, D10, D20, D01, D11, D21, D02, D12, D22) $
D03, D13, D23, A, B) $

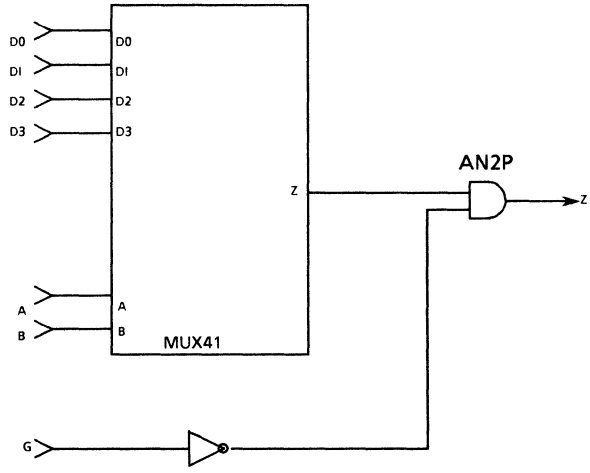
Input Loading: (2, 2, 1.5, 2, 2, 1.5, 2, 2, 1.5,
2, 2, 1.5)

MUX41GH	4 BIT NON INVERTING MUX, GATED	MUX41GH

LOGIC SYMBOL



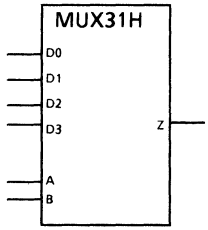
LOGIC DIAGRAM



Gates Used: 9	February, 1987
Coding syntax: Z(Z) = MUX41GH (D0, D1, D2, D3, A, B, G) $	
Input Loading: (2, 2, 2, 2, 3, 2, 1.5)	

MUX41H	4 BIT NON INVERTING MUX	MUX41H

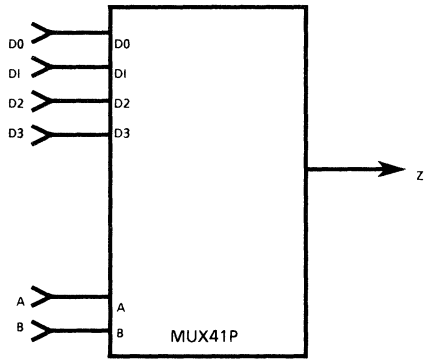
LOGIC SYMBOL



TRUTH TABLE

A	B	Z
0	0	D0
1	0	D1
0	1	D2
1	1	D3

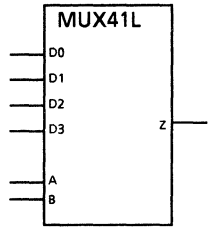
LOGIC DIAGRAM



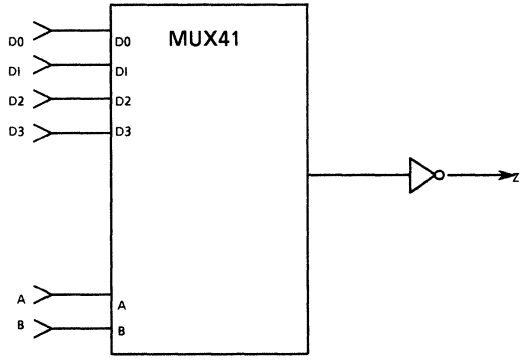
Gates Used: 7	February, 1987
Coding syntax: Z(Z) = MUX41H (D0, D1, D2, D3, A, B) $	
Input Loading: (2, 2, 2, 2, 3, 2)	

MUX41L	4 BIT INVERTING MUX	MUX41L

LOGIC SYMBOL



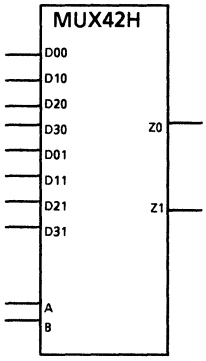
LOGIC DIAGRAM



Gates Used: 7	February, 1987
Coding syntax: Z(Z) = MUX41L (D0, D1, D2, D3, A, B) $	
Input Loading: (2, 2, 2, 2, 3, 2)	

MUX42H	DUAL 4 BIT NON INVERTING MUX	MUX42H

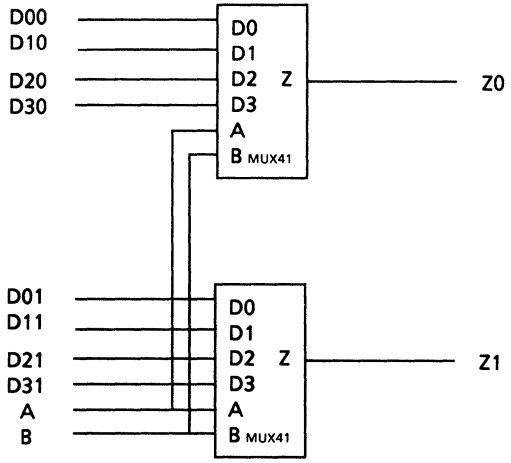
LOGIC SYMBOL



TRUTH TABLE

A	B	Z (I)
0	0	D0 (I)
1	0	D1 (I)
0	1	D2 (I)
1	1	D2 (I)

LOGIC DIAGRAM



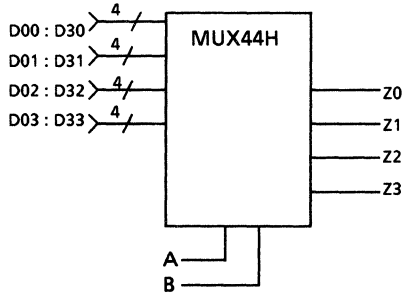
Gates Used: 14 February, 1987

Coding syntax: Z(Z0, Z1) = MUX42H (D00, D10, D20, D30, D01, D11, D21, D31, A, B) $

Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 6, 4)

MUX44H	QUAD 4 BIT NON INVERTING MUX	MUX44H

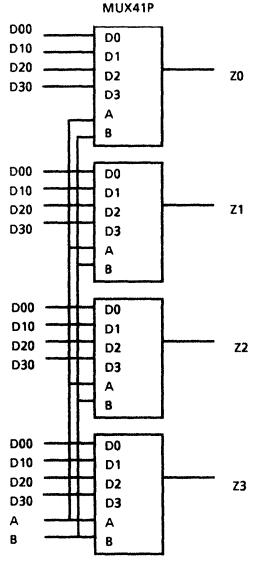
LOGIC SYMBOL



TRUTH TABLE

A	B	Z (I)
0	0	D0 (I)
1	0	D1 (I)
0	1	D2 (I)
1	1	D3 (I)

LOGIC DIAGRAM



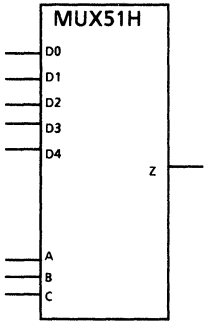
Gates Used: 24 February, 1987

Coding syntax: Y(Z0, Z1, Z2, Z3) = MUX44H (D00, D10, D20, D30, D01, D11, D21, D31, D02, D12, D22, D32, D03, D13, D23, D33, A, B) $

Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 12, 8)

MUX51H — 5 BIT NON INVERTING MUX — MUX51H

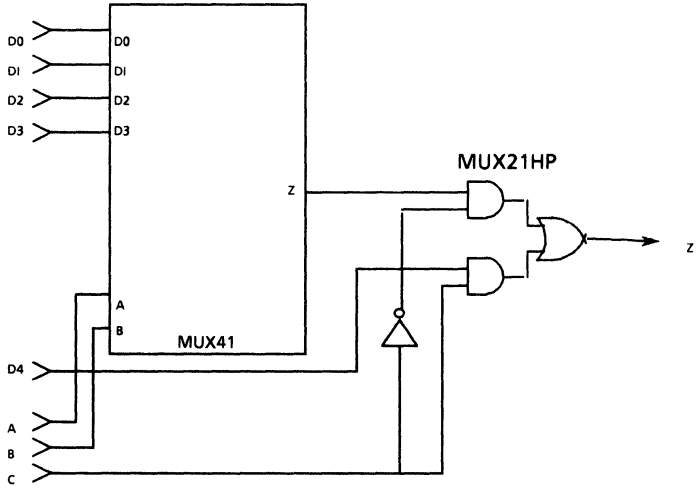
LOGIC SYMBOL



TRUTH TABLE

A	B	C	Z
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D4
0	1	1	D4
1	1	1	D4

LOGIC DIAGRAM



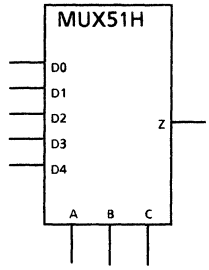
Gates Used: 10 — February, 1987

Coding syntax: Y(Z0, Z1, Z2, Z3) = MUX51H (D0,D1, D2, D3, D4, A, B, C)

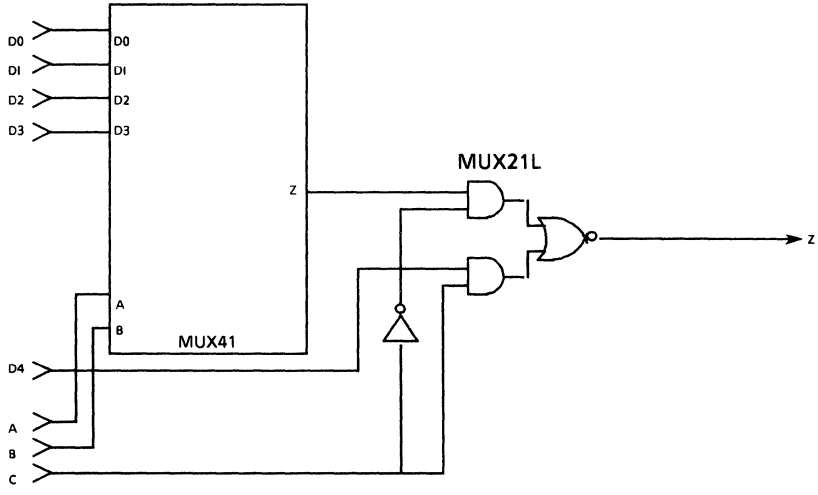
Input Loading: (2, 2, 2, 2, 1, 3, 2, 2)

MUX51L	5 BIT INVERTING MUX	MUX51L

LOGIC SYMBOL



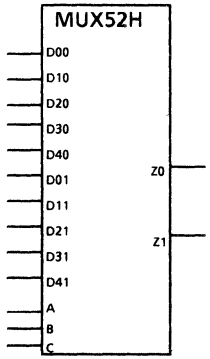
LOGIC DIAGRAM



Gates Used: 10	February, 1987
Coding syntax: Y(Z0, Z1, Z2, Z3) = MUX51L (D0, D1, D2, D3, D4, A, B, C)	
Input Loading:	(2, 2, 2, 2, 1, 3, 2, 2)

MUX52H — DUAL 5 BIT NON INVERTING MUX — MUX52H

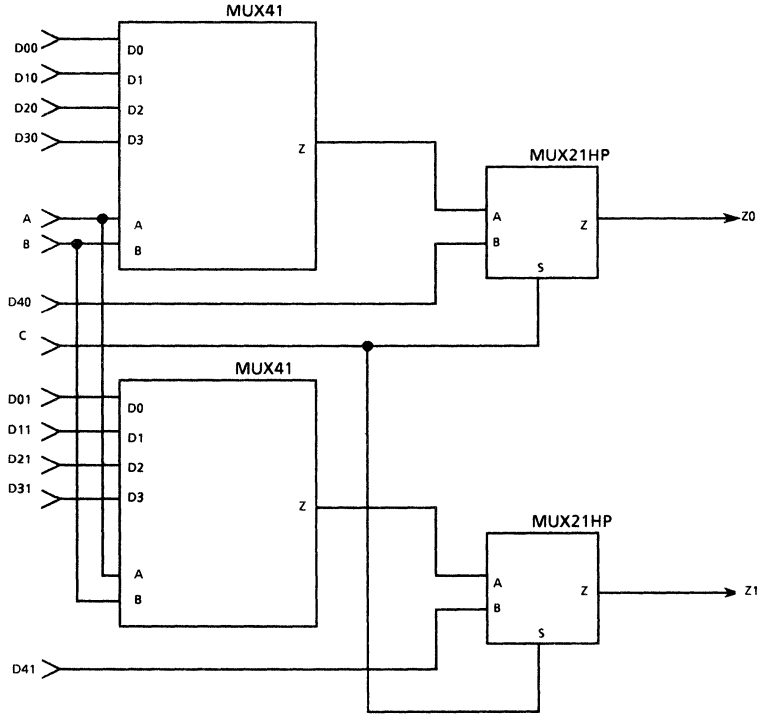
LOGIC SYMBOL



TRUTH TABLE

A	B	C	Z (I)
0	0	0	D0 (I)
1	0	0	D1 (I)
0	1	0	D2 (I)
1	1	0	D3 (I)
0	0	1	D4 (I)
1	0	1	D4 (I)
0	1	1	D4 (I)
1	1	1	D4 (I)

LOGIC DIAGRAM



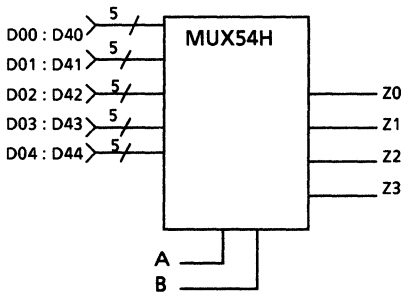
Gates Used: 20 — February, 1987

Coding syntax: Y (Z0, Z1) = MUX52H (D00, D10, D20, D30, D40, DO1, D11, D21, D31, D41, A, B, C) $

Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 4, 6, 4)

MUX54H	QUAD 5 BIT NON INVERTING MUX	MUX54H

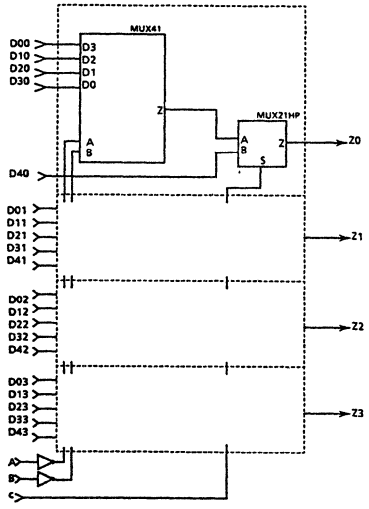
LOGIC SYMBOL



TRUTH TABLE

A	B	C	Z (I)
0	0	0	D0 (I)
1	0	0	D1 (I)
0	1	0	D2 (I)
1	1	0	D3 (I)
0	0	1	D4 (I)
1	0	1	D4 (I)
0	1	1	D4 (I)
1	1	1	D4 (I)

LOGIC DIAGRAM



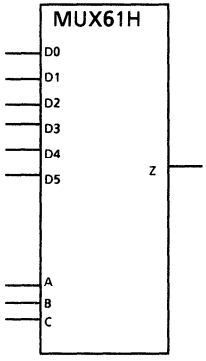
Gates Used: 44 February, 1987

Coding syntax: Y (Z0, Z1, Z2, Z3) = MUX54H (D00, D10, D20, D30, D40, DO1, D11, D21, D31, D41,
D02, D12, D22, D32, D42, D03, D13, D23, D33, D43,
A, B, C) $

Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 2, 2,
2, 2, 2, 2, 2, 2, 2, 2, 2, 2,
3, 3, 8)

MUX61H — 6 BIT NON INVERTING MUX — MUX61H

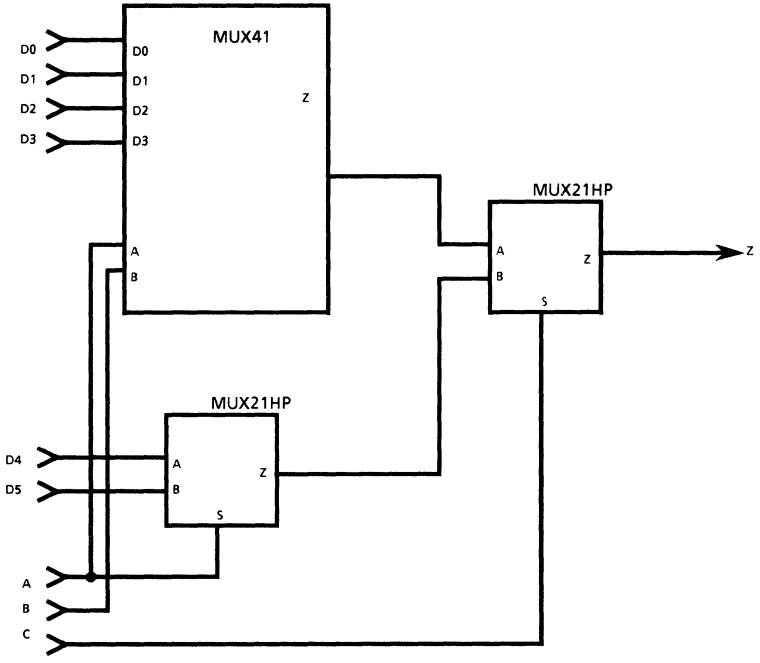
LOGIC SYMBOL



TRUTH TABLE

A	B	C	Z
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D4
1	1	1	D5

LOGIC DIAGRAM



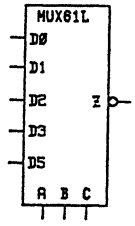
Gates Used: 14 — February, 1987

Coding syntax: Y(Z0, Z2, Z1, Z3) = MUX61H (D0, D1, D2, D3, D4, D5, A, B, C) $

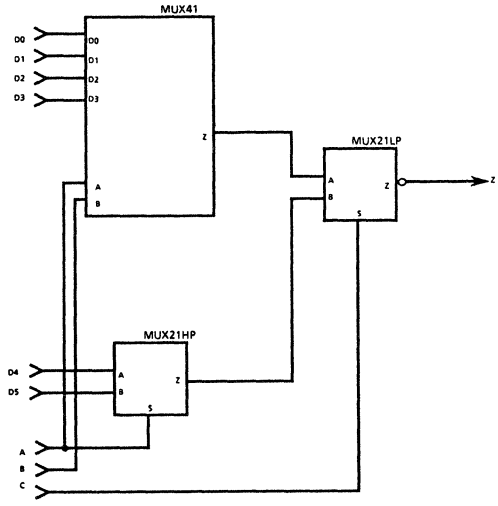
Input Loading: (2, 2, 2, 2, 1, 1, 5, 2, 2)

MUX61L	6 BIT INVERTING MUX	MUX61L

LOGIC SYMBOL



LOGIC DIAGRAM



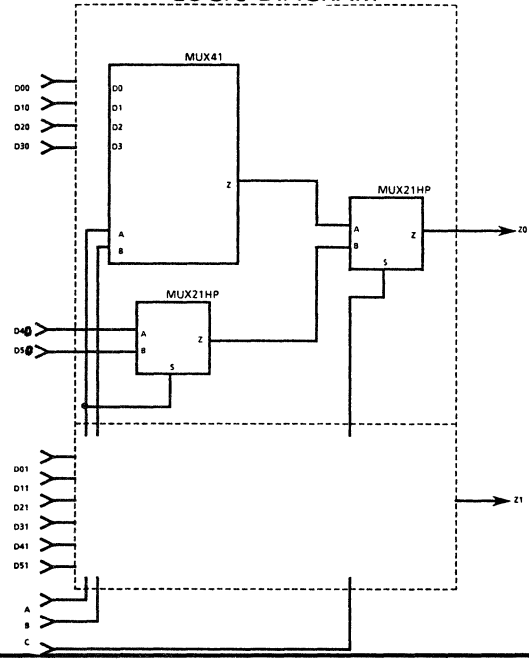
Gates Used: 14		February, 1987
Coding syntax:	Z = MUX61L (D0, D1, D2, D3, D4, D5, A, B, C) $	
Input Loading:	(2, 2, 2, 2, 1, 1, 5, 2, 2)	

MUX62H	DUAL 6 BIT NON INVERTING MUX	MUX62H

LOGIC SYMBOL

A	B	C	Z(I)
0	0	0	D0(I)
1	0	0	D1(I)
0	1	0	D2(I)
1	1	0	D3(I)
0	0	1	D4(I)
1	0	1	D5(I)
0	1	1	D4(I)
1	1	1	D5(I)

LOGIC DIAGRAM



Gates Used: 28 February, 1987

Coding syntax: Y (Z0, Z1) = MUX62H (D00, D10, D20, D30, D40, D50, DO1, D11, D21, D31, D41, D51

A, B, C) $

Input Loading: (2, 2, 2, 2, 1, 1, 2, 2, 2, 2, 1,

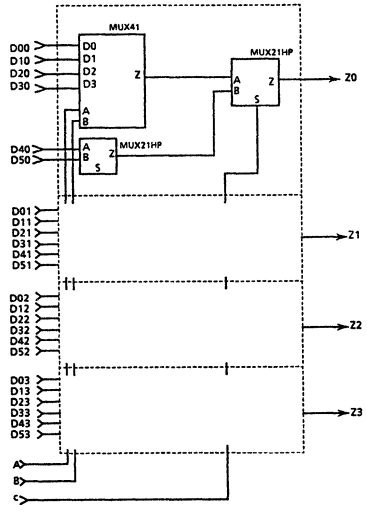
Input Loading: 10, 4, 4)

MUX64H	QUAD 6 BIT NON INVERTING MUX	MUX64H

TRUTH TABLE

A	B	C	Z (I)
0	0	0	D0 (I)
1	0	0	D1 (I)
0	1	0	D2 (I)
1	1	0	D3 (I)
0	0	1	D4 (I)
1	0	1	D5 (I)
0	1	1	D4 (I)
1	1	1	D5 (I)

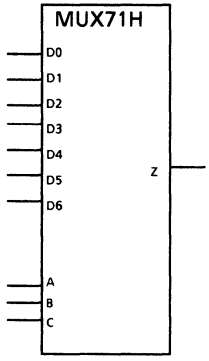
LOGIC DIAGRAM



Gates Used: 56	February, 1987
Coding syntax: Y (Z0, Z1, Z2, Z3) = MUX64H (D00, D10, D20, D30, D40, D50, DO1, D11, D21, D31,	
D41, D51, D02, D12, D22, D32, D42, D52, D03, D13,	
D23, D33, D43, D53, A, B, C) $	
Input Loading:	(2, 2, 2, 2, 1, 1, 2, 2, 2, 1,
2, 1, 2, 2, 2, 2, 1, 1, 2, 2,	
2, 2, 1, 1, 20, 8, 8)	

MUX71H — DUAL 7 BIT NON INVERTING MUX — MUX71H

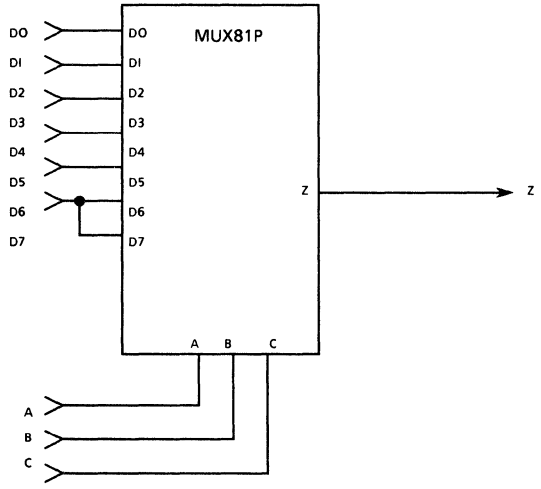
LOGIC SYMBOL



TRUTH TABLE

A	B	C	Z
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D6

LOGIC DIAGRAM



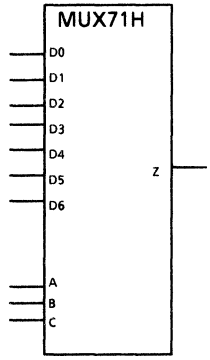
Gates Used: 15 — February, 1987

Coding syntax: Z = MUX71H (D0, D1, D2, D3, D4, D5, D6, A, B, C) $

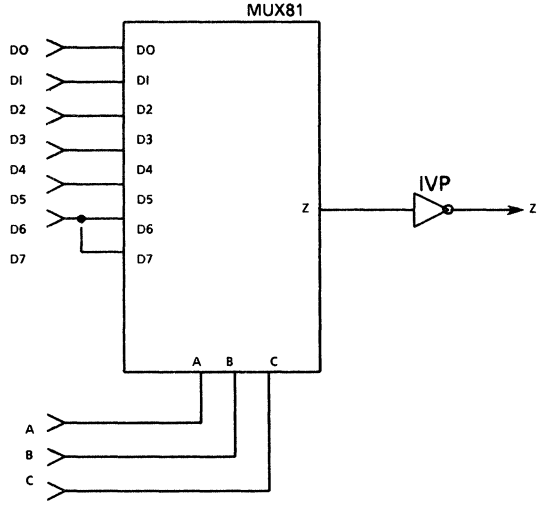
Input Loading: (2, 2, 2, 2, 2, 2, 2, 1, 3, 2)

MUX71L	7 BIT NON INVERTING MUX	MUX71L

LOGIC SYMBOL



LOGIC DIAGRAM



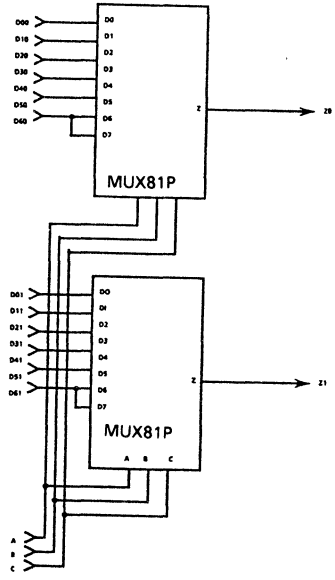
Gates Used: 16	February, 1987
Coding syntax: Z = MUX71L (D0, D1, D2, D3, D4, D5, D6, A, B, C) $	
Input Loading: (2, 2, 2, 2, 2, 2, 2, 1, 3, 2)	

MUX72H	QUAD 7 BIT NON INVERTING MUX	MUX72H

TRUTH TABLE

A	B	C	Z(I)
0	0	0	D0(I)
1	0	0	D1(I)
0	1	0	D2(I)
1	1	0	D3(I)
0	0	1	D4(I)
1	0	1	D5(I)
0	1	1	D6(I)
1	1	1	D6(I)

LOGIC DIAGRAM



Gates Used: 30 February, 1987

Coding syntax: Y (Z0, Z1) = MUX72H (D00, D10, D20, D30, D40, D50, D60, DO1, D11, D21, D31, D41, D51, D61, A, B, C) $

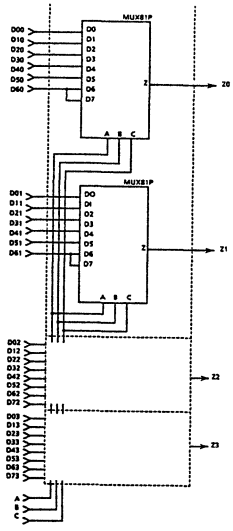
Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 2, 6, 4)

MUX74H	QUAD 7 BIT NON INVERTING MUX	MUX74H

TRUTH TABLE

A	B	C	Z(I)
0	0	0	D0(I)
1	0	0	D1(I)
0	1	0	D2(I)
1	1	0	D3(I)
0	0	1	D4(I)
1	0	1	D5(I)
0	1	1	D6(I)
1	1	1	D6(I)

LOGIC DIAGRAM



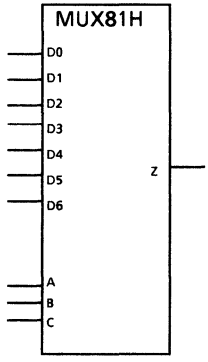
Gates Used: 48 February, 1987

Coding syntax: Y (Z0, Z1, Z2, Z3) = MUX74H (D00, D10, D20, D30, D40, DO1, D11, D21, D31, D41,
D51, D61, D02, D12, D22, D32, D42, D52, D62, D03,
D13, D23, D33, D43, D53, D63, A, B, C) $

Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 2, 2,
2, 2, 2, 2, 2, 2, 2, 2, 2, 2,
2, 2, 2, 2, 2, 2, 4, 12, 8)

MUX81H — 8 BIT NON INVERTING MUX — MUX81H

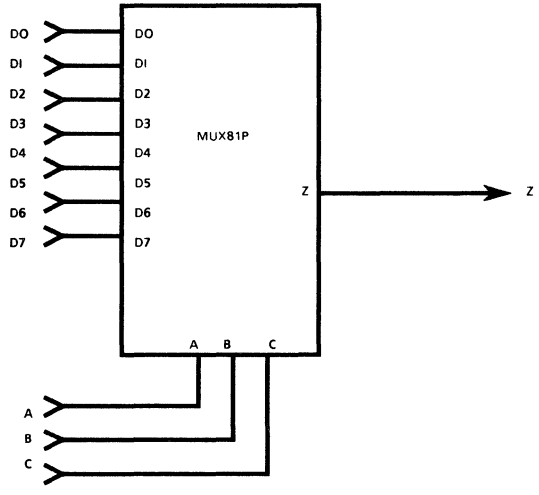
LOGIC SYMBOL



TRUTH TABLE

A	B	C	Z
0	0	0	D0
1	0	0	D1
0	1	0	D2
1	1	0	D3
0	0	1	D4
1	0	1	D5
0	1	1	D6
1	1	1	D7

LOGIC DIAGRAM



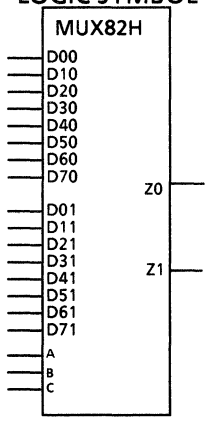
Gates Used: 15 — February, 1987

Coding syntax: Z = MUX81H (D0, D1, D2, D3, D4, D5, D6, D7, A, B, C) $

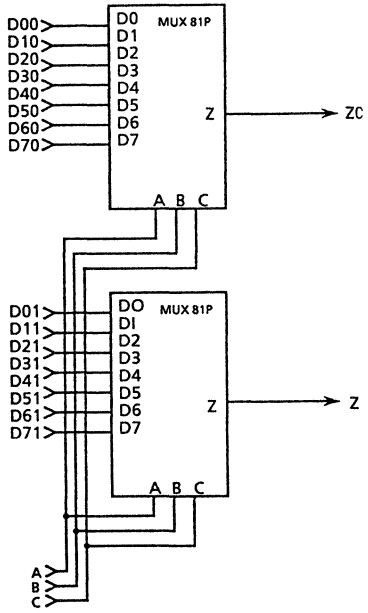
Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 1, 3, 2)

MUX82H	DUAL 8 BIT NON INVERTING MUX	MUX82H

LOGIC SYMBOL



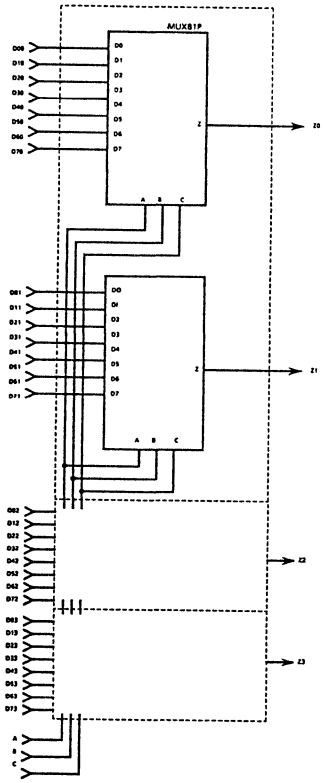
LOGIC DIAGRAM



Gates Used: 30	February, 1987
Coding syntax: Y (Z0, Z1) = MUX82H (D00, D10, D20, D30, D40, D50, D60, D70, DO1, D11, D21,	
D31, D41, D51, D61, D71, A, B, C) $	
Input Loading: (2, 2, 2, 2, 2, 2, 2, 2, 2, 2,	
2, 2, 2, 2, 2, 2, 2, 3, 3, 8)	

MUX84H	QUAD 8 BIT NON INVERTING MUX	MUX84H

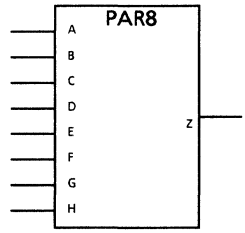
LOGIC DIAGRAM



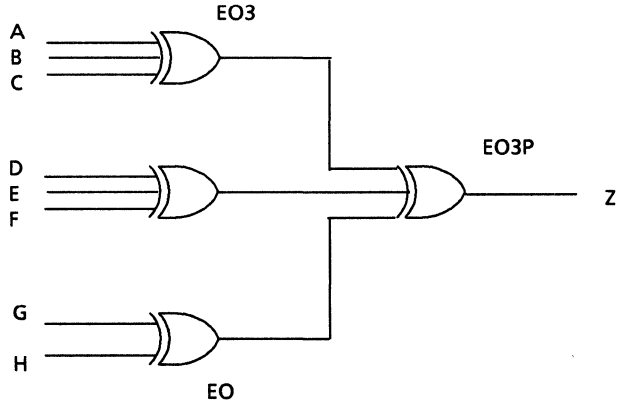
Gates Used: 60	February, 1987
Coding syntax: Y (Z0, Z1, Z2, Z3) = MUX84H (D00, D10, D20, D30, D40, D50, D60, D70, D01, D11,	
D21, D31, D41, D51, D61, D71, D02, D12, D22, D32,	
D42, D52, D62, D72, D03, D13, D23, D33, D43, D53,	
D63, D73, A, B, C) $	
Input Loading:	(2, 2, 2, 2, 2, 2, 2, 2, 2, 2,
	2, 2, 2, 2, 2, 2, 2, 2, 2, 2,
	2, 2, 2, 2, 2, 2, 2, 2, 2, 2,
	2, 2, 4, 12, 8)

PAR8	8 BIT ODD PARITY DETECTOR	PAR8

LOGIC SYMBOL



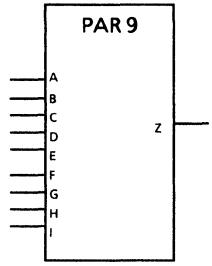
LOGIC DIAGRAM



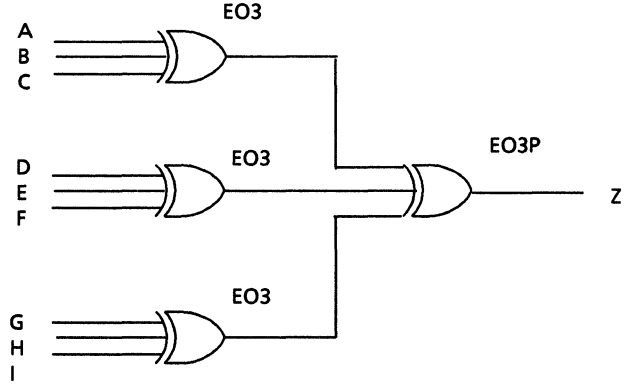
Gates Used: 24	February, 1987
Coding syntax: Y (Z) = PAR8 (A, B, C, D, E, F, G, H) $	
Input Loading: (1, 3, 2, 1, 3, 2, 1, 2)	

PAR9	9 BIT ODD PARITY DETECTOR	PAR9

LOGIC SYMBOL



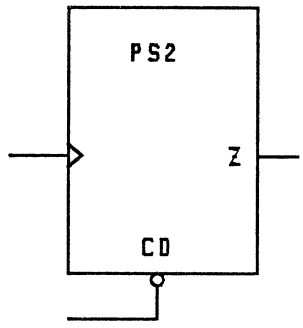
LOGIC DIAGRAM



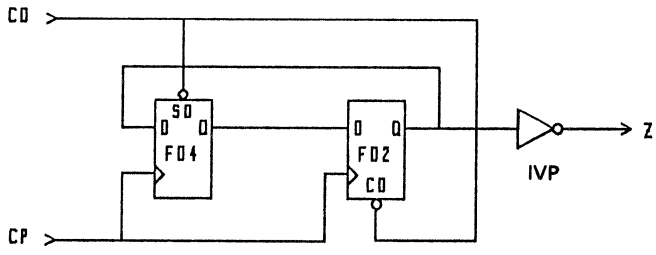
Gates Used: 28	February, 1987
Coding syntax: Y (Z) = PAR9 (A, B, C, D, E, F, G, H, I) $	
Input Loading: (1, 3, 2, 1, 3, 2, 1, 3, 2)	

PS2	DIVIDE BY 2 EXETERNAL CLOCK PRESCALER WITH NO INPUT PROTECTION	PS2

LOGIC SYMBOL



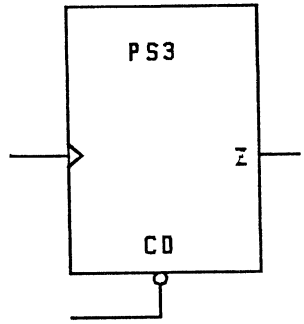
LOGIC DIAGRAM



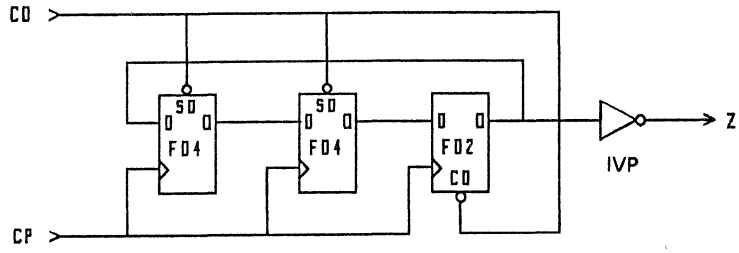
Gates Used: 17	February, 1987
Coding syntax: Z = PS2 (CP, CD) $	
Input Loading: (2, 4)	

PS3	DIVIDE BY 3 EXETERNAL CLOCK PRESCALER WITH NO INPUT PROTECTION	PS3

LOGIC SYMBOL



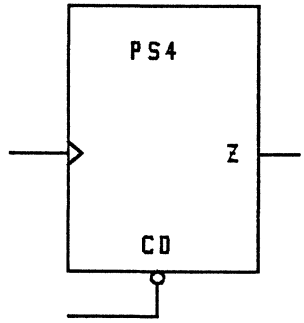
LOGIC DIAGRAM



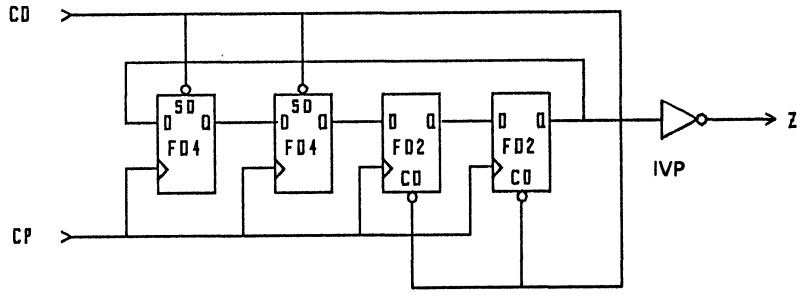
Gates Used: 25	February, 1987
Coding syntax: Z = PS3 (CP, CD) $	
Input Loading: (3, 6)	

PS4	DIVIDE BY 4 EXETERNAL CLOCK PRESCALER WITH NO INPUT PROTECTION	PS4

LOGIC SYMBOL



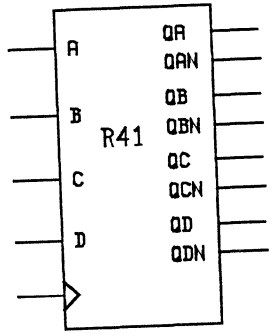
LOGIC DIAGRAM



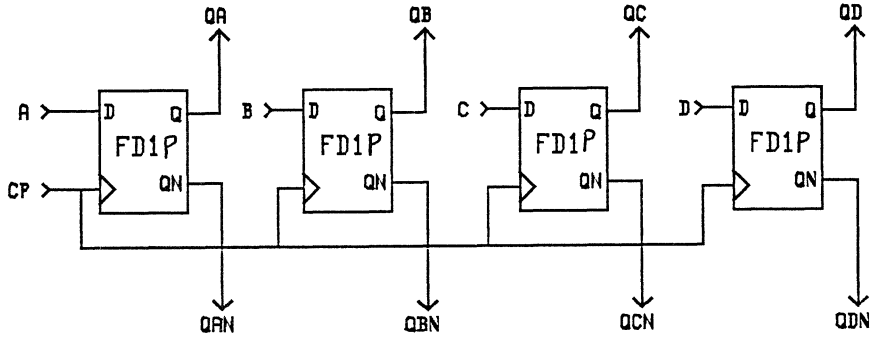
Gates Used: 33	February, 1987
Coding syntax: Z = PS4 (CP, CD) $	
Input Loading: (4, 8)	

R41	4 BIT DATA REGISTER	R41

LOGIC SYMBOL



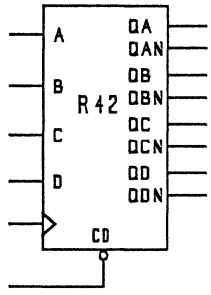
LOGIC DIAGRAM



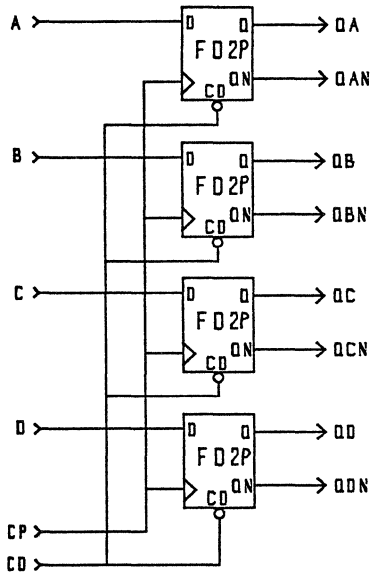
Gates Used: 32	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = R41 (A, B, C, D, CP) $	
Input Loading:	(1, 1, 1, 1, 4)

R42	4 BIT DATA REGISTER CLEAR DIRECT	R42

LOGIC SYMBOL



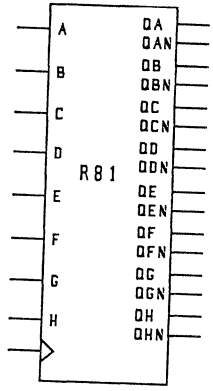
LOGIC DIAGRAM



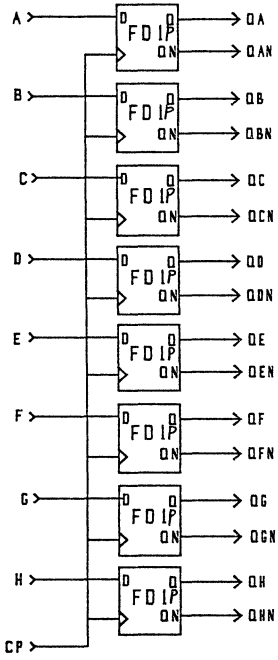
Gates Used: 36	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN) = R42 (A, B, C, D, CP, CD) $	
Input Loading:	(1, 1, 1, 1, 4, 8)

R81	8 BIT DATA REGISTER	R81

LOGIC SYMBOL



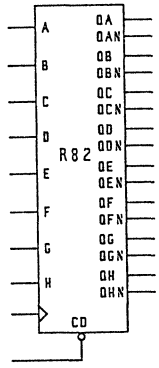
LOGIC DIAGRAM



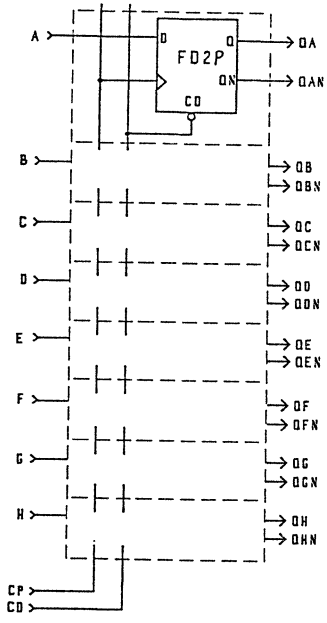
Gates Used: 64	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN)	
Coding syntax: = R81 (A, B, C, D, E, F, G, H, CP) $	
Input Loading: (1, 1, 1, 1, 1, 1, 1, 1, 8)	

R82	8 BIT DATA REGISTER CLEAR DIRECT	R82

LOGIC SYMBOL



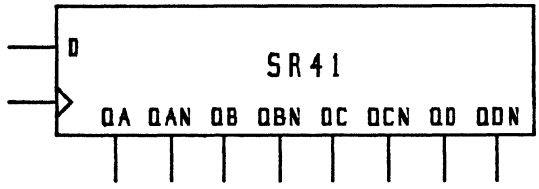
LOGIC DIAGRAM



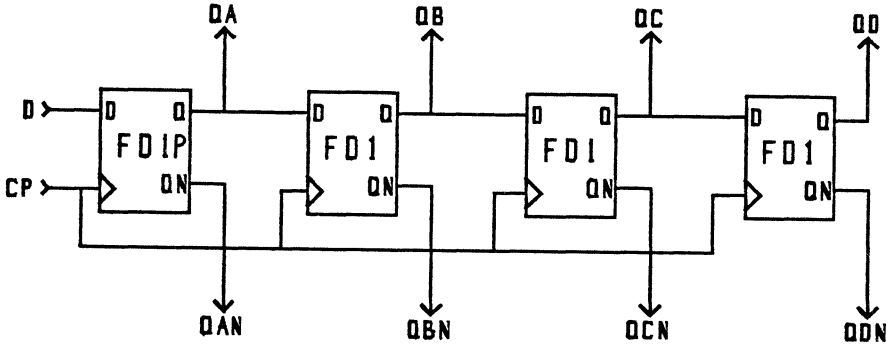
Gates Used: 80	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN, QE, QEN, QF, QFN, QG, QGN, QH, QHN)	
Coding syntax: = R82 (A, B, C, D, E, F, G, H, CP, CD) $	
Input Loading: (1, 1, 1, 1, 1, 1, 1, 1, 8, 16)	

SR41	4 BIT SHIFT REGISTER	SR41

LOGIC SYMBOL



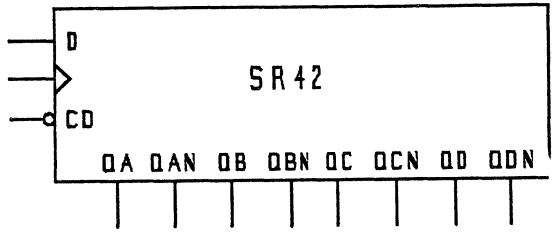
LOGIC DIAGRAM



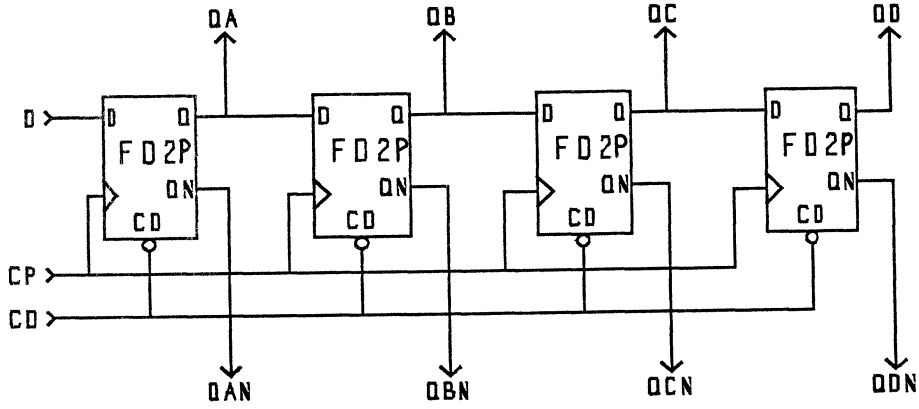
Gates Used: 32	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN)	
Coding syntax: = SR41 (D, CP) $	
Input Loading: (1, 4)	

SR42	4 BIT SHIFT REGISTER, CLEAR DIRECT	SR42

LOGIC SYMBOL



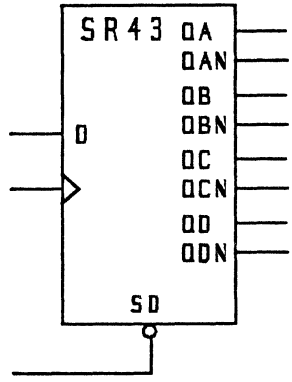
LOGIC DIAGRAM



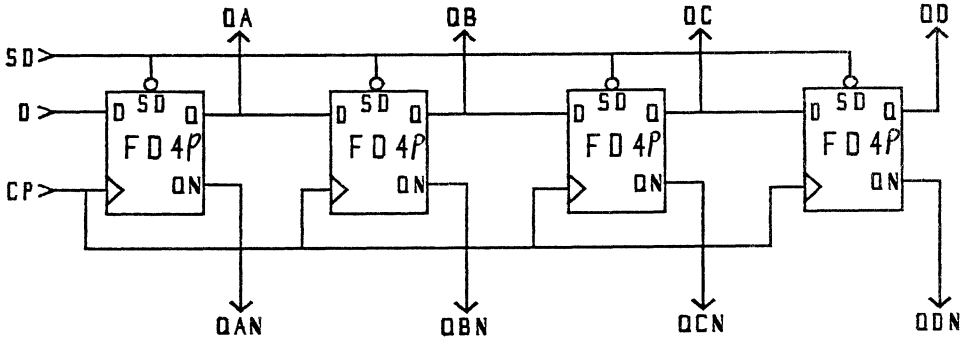
Gates Used: 40	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN)	
Coding syntax: = SR42 (D, CP, CD) $	
Input Loading: (1, 4, 8)	

SR43	4 BIT SHIFT REGISTER, SET DIRECT	SR43

LOGIC SYMBOL



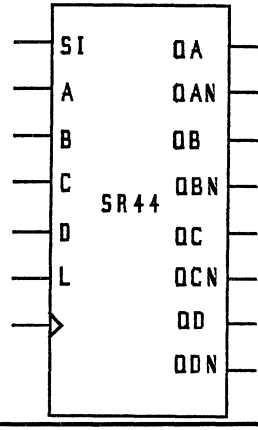
LOGIC DIAGRAM



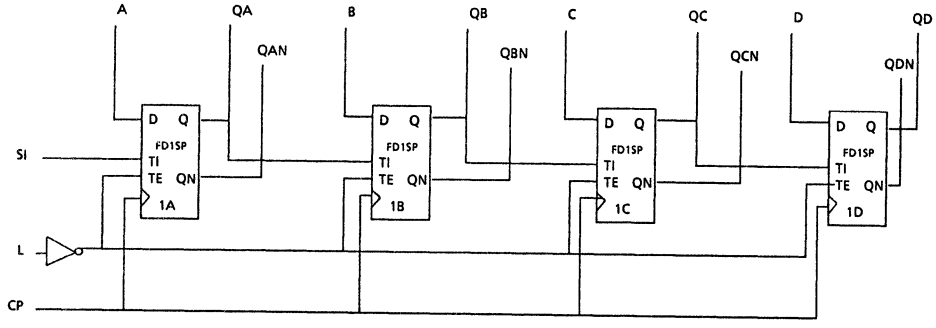
Gates Used: 36	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN)	
Coding syntax: = SR43 (D, CP, SD) $	
Input Loading: (1, 4, 8)	

SR44	4 BIT SHIFT REGISTER, SYNCHRONOUS PARALLEL LOAD	SR44

LOGIC SYMBOL



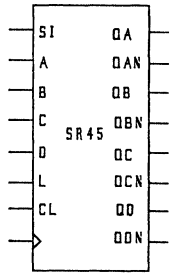
LOGIC DIAGRAM



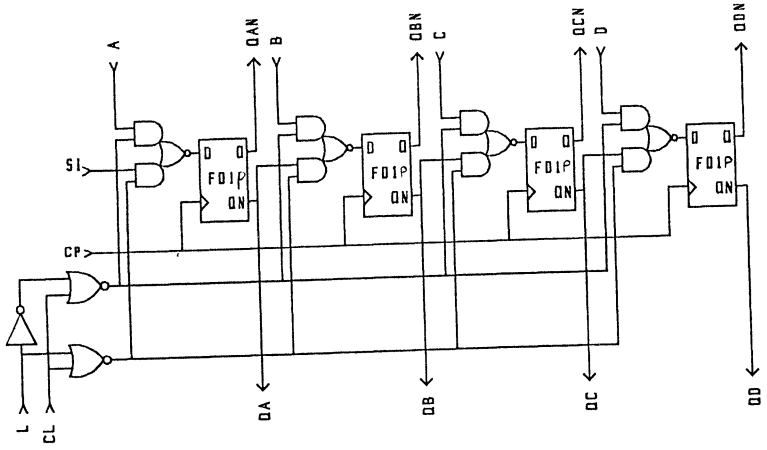
Gates Used: 42	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN)	
Coding syntax: = SR44 (SI, A, B, C, D, L, CP) $	
Input Loading: (1, 1, 1, 1, 1, 3, 4)	

SR45	4 BIT SHIFT REGISTER, SYNCHRONOUS PARALLEL LOAD AND CLEAR	SR45

LOGIC SYMBOL



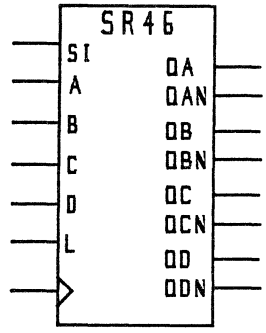
LOGIC DIAGRAM



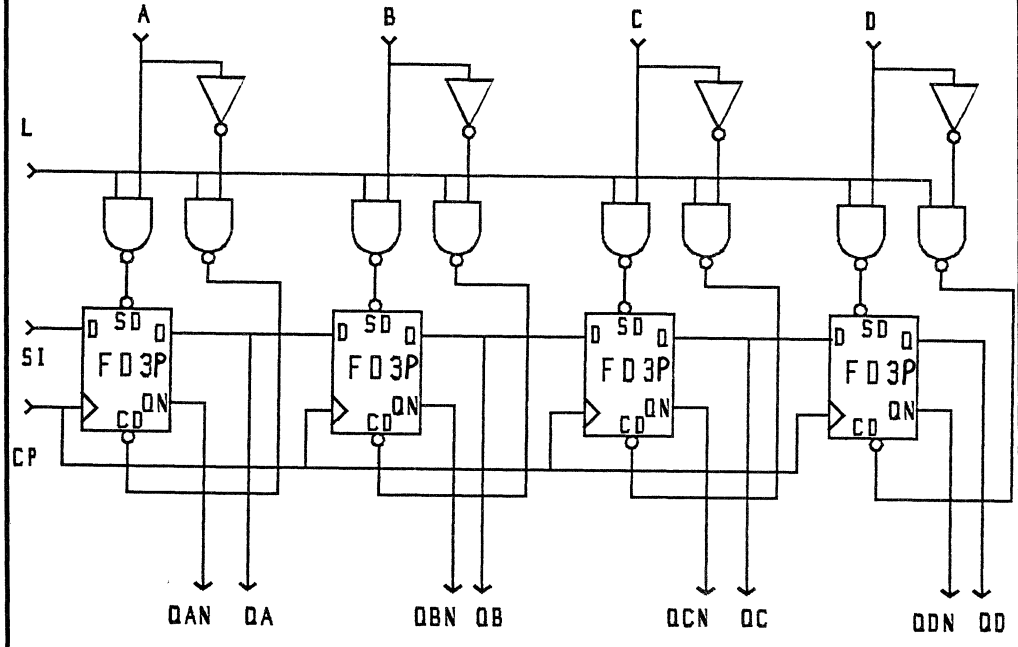
Gates Used: 45	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN)	
Coding syntax: = SR45 (SI, A, B, C, D, L, CL, CP) $	
Input Loading: (1, 1, 1, 1, 1, 3.5, 4, 4)	

SR46	4 BIT SHIFT REGISTER, ASYNCHRONOUS PARALLEL LOAD AND CLEAR	SR46

LOGIC SYMBOL



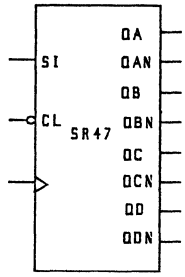
LOGIC DIAGRAM



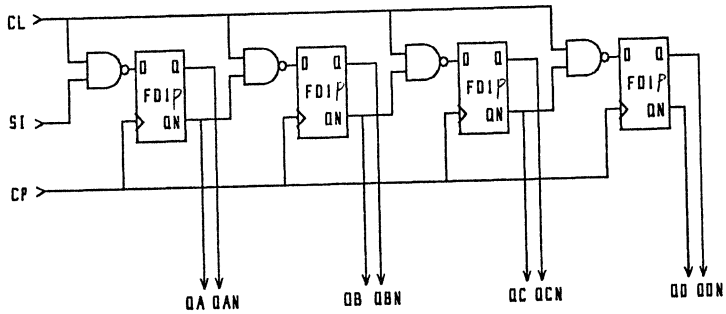
Gates Used: 52	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN)	
Coding syntax: = SR46 (SI, A, B, C, D, L, CP) $	
Input Loading: (1, 2.5, 2.5, 2.5, 2.5, 8, 4)	

SR47	4 BIT SHIFT REGISTER, SYNC CLEAR	SR47

LOGIC SYMBOL



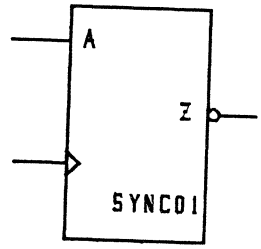
LOGIC DIAGRAM



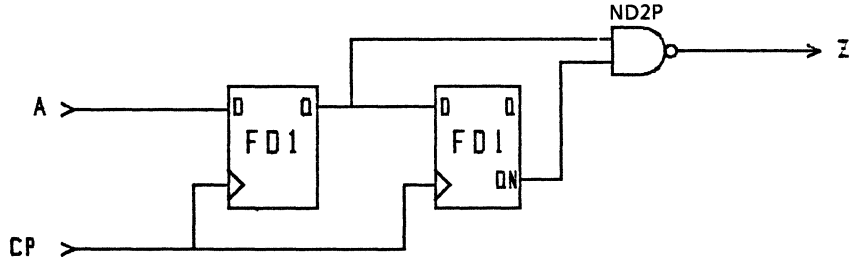
Gates Used: 36	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN)	
Coding syntax: = SR47 (SI, CL, CP) $	
Input Loading: (1, 4, 4)	

SYNC01	SYNCHRONIZER FOR ASYNCHRONOUS 0 TO 1 EVENT	SYNC01

LOGIC SYMBOL



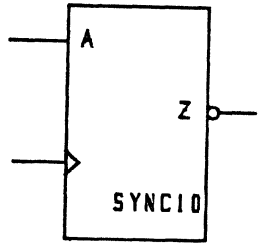
LOGIC DIAGRAM



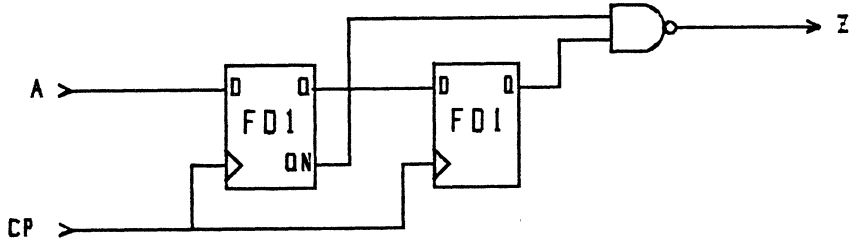
Gates Used: 16	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN)	
Coding syntax: = SYNC01 (A, CP) $	
Input Loading: (1, 2)	

SYNC10	SYNCHRONIZER FOR ASYNCHRONOUS 1 TO 0 EVENT	SYNC10

LOGIC SYMBOL



LOGIC DIAGRAM



Gates Used: 16	February, 1987
Coding syntax: Z (QA, QAN, QB, QBN, QC, QCN, QD, QDN)	
Coding syntax: = SYNC10 (A, CP) $	
Input Loading: (1, 2)	

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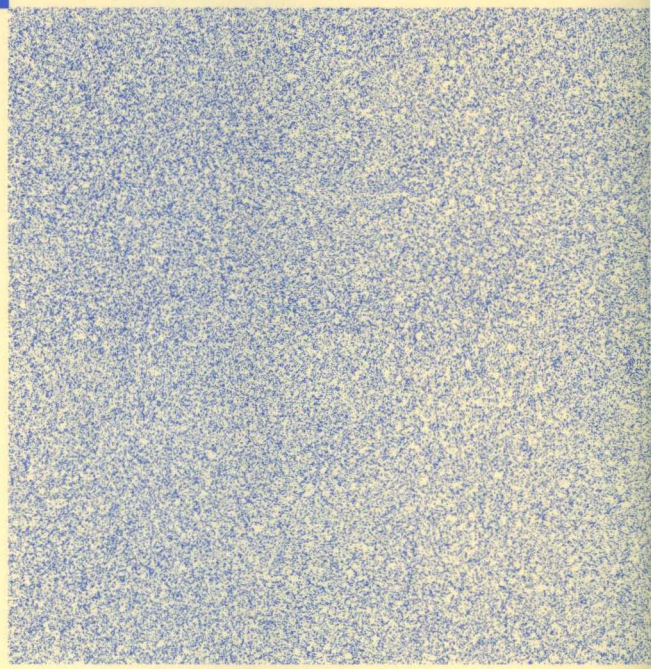

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