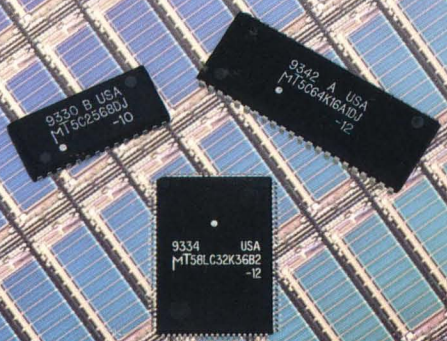
1994 SRAM DATA BOOK



MICRON
SEMICONDUCTOR, INC.

MICRON SEMICONDUCTOR, INC.

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SEMICONDUCTOR, INC.

SRAM DATA BOOK

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ABOUT THE COVER:

Front — A variety of features highlight Micron's SRAM product line. Shown at left, a circuitry backdrop rendered from a scanning electron microscope. Bottom right, the intricate memory of a 256K SRAM wafer, etched in silicon, which reflects the many hues of the natural color spectrum.

Back — Micron's Boise, Idaho, headquarters.

IMPORTANT NOTICE

Micron Semiconductor, Inc. (Micron), reserves the right to change products or specifications without notice. Customers are advised to obtain the latest versions of product specifications, which should be considered in evaluating a product's appropriateness for a particular use. There is no assurance that Micron's semiconductor products are appropriate for any application by a customer.

MICRON MAKES NO WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OTHER THAN COMPLIANCE WITH MICRON'S SPECIFICATION SHEET FOR THE PRODUCT AT THE TIME OF DELIVERY. IN NO EVENT SHALL MICRON BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES AS A RESULT OF THE PERFORMANCE, OR FAILURE TO PERFORM, OF ANY MICRON PRODUCT.

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MICRON DOES NOT WARRANT PRODUCT TO BE FREE OF CLAIMS OF PATENT INFRINGEMENT BY ANY THIRD PARTY AND DISCLAIMS ANY SUCH WARRANTY OR INDEMNIFICATION AGAINST PATENT INFRINGEMENT.

Dear Customer:

Micron Semiconductor, Inc., is dedicated to the design, manufacture and marketing of high-quality, highly reliable memory components. Our corporate mission is:

"To be a world-class team developing advantages for our customers."

At Micron, we are investing time, talent and resources to bring you the finest DRAMs, SRAMs and other specialty memory products. We have developed a unique intelligent burn-in system, AMBYX®, which evaluates and reports the quality level of each and every component we produce.

We are dedicated to continuous improvement of all our products and services. This means continual reduction of electrical and mechanical defect levels. It also means the addition of new services such as "just-in-time" delivery and electronic data interchange programs. And when you have a design or application question, you can get the answers you need from one of Micron's applications engineers.

We're proud of our products, our progress and our performance. And we're pleased that you're choosing Micron as your memory supplier.

The Micron Team

ADVANTAGES

Micron Semiconductor brings quality, productivity and innovation together to provide advantages for our customers. Our products feature some of the industry's fastest speeds. And we establish delivery standards based on customer expectations, including JIT programs, made possible by ever-increasing product reliability.

COMPONENT INTEGRATED CIRCUITS

Micron entered the memory market in 1978, first designing, then manufacturing dynamic random access memory (DRAM). From there, we developed high-performance fast static RAM (SRAM), multiport DRAM (including triple-port DRAM), and a variety of other memory products.

As we bring innovative memory solutions to our customers, we enjoy recognition for our achievements. Micron's Triple-Port DRAM was the first IC ever to incorporate a second, independent serial access port, allowing unparalleled flexibility in data manipulation. Micron's Triple-Port received the 1990 "Product of the Year" award from *Electronic Products* magazine.

SPECIALTY MEMORY PRODUCTS

Beyond our standard component memory, Micron is introducing many revolutionary products that we expect will follow the Triple-Port tradition. Micron continues to forge ahead into new and exciting frontiers.

We are pleased to be first to market with our compact, easy-to-install 88-pin DRAM card. Ideal for laptop, notebook and other portable systems, Micron's DRAM Card offers both high density and low power within JEDEC and JEIDA specifications.*

DIE SALES

In addition to our durable packaging, Micron also provides memory devices in bare die form. These are increasingly in demand for use in highly specialized applications. Micron's bare die products are available both in 6" wafers and wafflepacks.

CUSTOM MANUFACTURING SERVICES

For total project management, Micron offers value-added services. These include both standard contract manufacturing services for system-level products including design, assembly, customer kitted assembly, comprehensive quality testing or shipping as well as complete turnkey services covering all phases of production. Our component and system-level manufacturing facilities are centrally located in Boise, Idaho, so the component products you need are readily available.

MICRON DATAFAX

When you can't afford to wait for critical product information or specifications, Micron offers a convenient solution available 24 hours a day, every day. Micron DataFax enables you to make automated requests for data sheets, product literature, and other information from your fax machine. Just dial 208-368-5800 from your fax machine and Micron DataFax will give you instructions on how to order documents, including an index of documents. Once your order is placed, Micron DataFax will process your order, faxing up to two documents per call to your fax machine.

QUALITY

Without a doubt, quality is the most important thing we provide to every Micron customer with each Micron shipment. That's because we believe that quality must be internalized consistently at each level of our company. We provide every Micron team member with the training and motivation needed to make Micron's quality philosophy a reality.

One way we have measurably improved both productivity and product quality is through our own quality improvement program formed by individuals throughout the company. Micron quality teams get together to address a wide range of issues within their areas. We consistently and regularly perform a company-wide self-assessment based on the Malcolm Baldrige National Quality Award criteria. We've also implemented statistical process controls to evaluate every facet of the memory design, fabrication, assembly and shipping process. And our AMBYX intelligent burn-in and test system** gives Micron a unique edge in product reliability.

These quality programs recently resulted in Micron becoming one of the first U.S. semiconductor manufacturers to receive ISO 9001 certification. ISO 9001 is the most comprehensive level of certification in the internationally recognized ISO family of specifications. The certification implies that Micron's systems for accepting orders, reviewing customers' specifications, manufacturing and testing products, and delivering those products to its customers are quality controlled and produce consistent results.

*See NOTE, page v.
**For more information on AMBYX, see Section 6.

ABOUT THIS BOOK

CONTENT

The 1995 *SRAM Data Book* from Micron Semiconductor provides complete specifications on Micron's standard SRAMs, Synchronous SRAMs and SRAM Modules.

The *SRAM Data Book* is one of three product data books Micron currently publishes. Its two companion volumes include our *DRAM Data Book* and *Flash Data Book*. As product lines continue to diversify, more data books will be released.

SECTION ORGANIZATION

Micron's 1995 *SRAM Data Book* contains a detailed Table of Contents with sequential and numerical indexes of products as well as a complete product selection guide. The *Data Book* is organized into nine sections:

- **Sections 1–4:** Individual product families. Each contains a product selection guide followed by data sheets.
- **Section 5:** Technical/application notes.
- **Section 6:** Summary of Micron's unique quality and reliability programs and testing operation, including our AMBYX intelligent burn-in and test system.*
- **Section 7:** Packaging information.
- **Section 8:** Sales information, including a list of sales representatives and distributors worldwide.

DATA SHEET SEQUENCE

Data sheets in this book are ordered first by width and second by depth. For example, the SRAM section begins with the 256K x 1 followed by 1 Meg x 1, the 64K x 4 and all other x4 configurations in order of ascending depth. Next come the x8 products, etc., as applicable to the specific product family.

DATA SHEET DESIGNATIONS

As detailed in the table below, each Micron product data sheet is classified as either Advance, Preliminary or Final. In addition, new product data sheets that are new additions are designated with a "New" indicator in the tab area of each page.

SURVEY

We have included a removable, postage-paid survey form in the front of this book. Your time in completing and returning this survey will enhance our efforts to continually improve our product literature.

For more information on Micron product literature, or to order additional copies of this publication, contact:

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Fax 208-368-3342

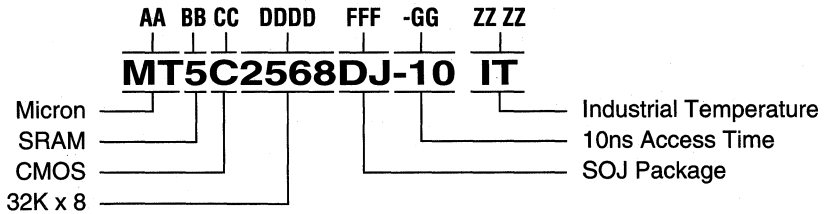
DATA SHEET DESIGNATIONS

DATA SHEET MARKING	DEFINITION
Advance	This data sheet contains initial descriptions of products still under development.
Preliminary	This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.
No Marking	This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.
New	This data sheet (which may be either Advance, Preliminary or Final) is a new addition to the data book.

NOTE: Micron uses acronyms to refer to certain industry-standard-setting bodies. These are defined below:
EIA/JEDEC—Electronics Industry Association/Joint Electron Device Engineering Council
JEIDA—Japanese Electronics Industry Development Association
PCMCIA—Personal Computer Memory Card International Association

*Micron's *Quality/Reliability Handbook* is available by calling 208-368-3900.

EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product	MT

BB – PRODUCT FAMILY

Flash	28
DRAM	4
SGRAM	41
SRAM	5
Synchronous SRAM	58

CC – PROCESS TECHNOLOGY

CMOS	C
Low Voltage CMOS	LC
Flash CMOS	F
Low Voltage Flash CMOS	LF

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

Flash	Density, Configuration
DRAM	Width, Density
TPDRAM	Width, Density
SRAM	Total Bits, Width
Synchronous SRAM	Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required.)

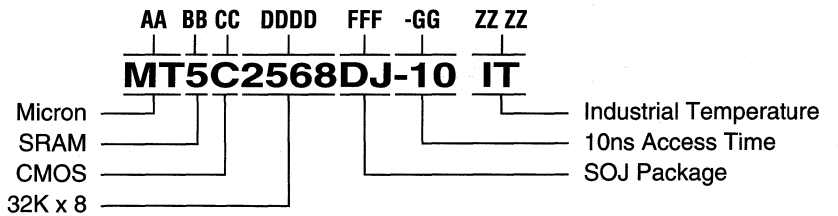
JEDEC Test Mode (4 Meg DRAM)	J
Errata on Base Part	Q

FFF – PACKAGE CODES

PLASTIC

DIP	Blank
DIP (Wide Body)	W
ZIP	Z
LCC	EJ
SOP/SOIC	SG
QFP	LG
TSOP (Type I)	VG
TSOP (Type I, Reversed)	XG
TSOP (Type II)	TG
TSOP (Reversed)	RG
TSOP (Longer)	TL
SOJ	DJ
SOJ (Reversed)	DR
SOJ (Longer)	DL

EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

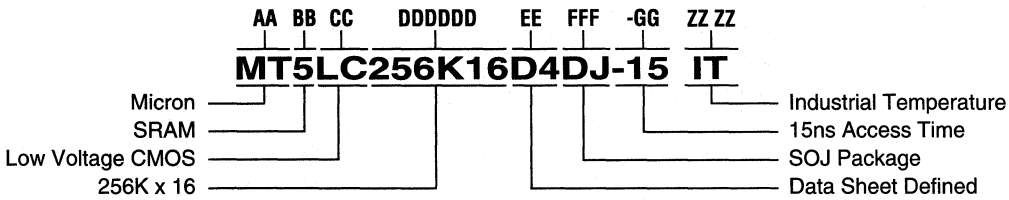
Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh/Extended Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
Flash	
Bottom Boot	B
Top Boot	T
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
SGRAM 41
TPDRAM 43
Synchronous DRAM 48
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC
BiCMOS ..... B
Low Voltage BiCMOS ..... LB

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter ..... Bits
K ..... Kilobits
M ..... Megabits
G ..... Gigabits

EE – DEVICE VERSIONS

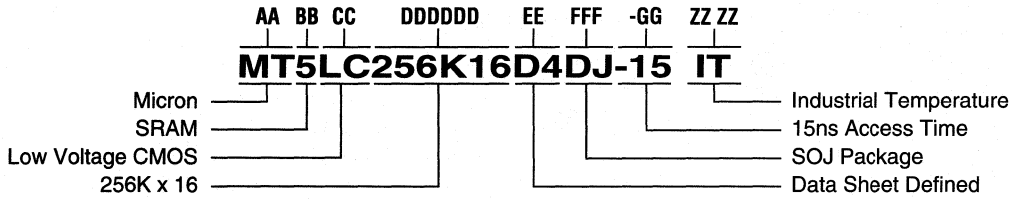
(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet.

FFF – PACKAGE CODES

Plastic

DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG
QFP ..... LG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Wide) ..... DW
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-9	9ns or 90ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

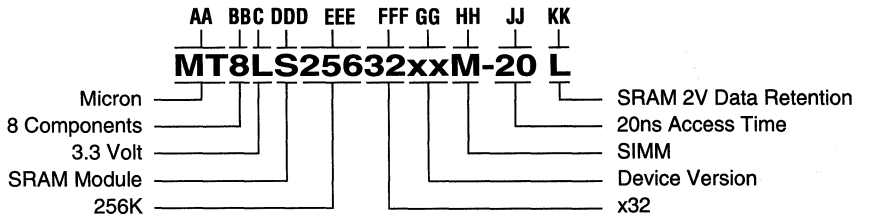
Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh/Extended Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Volt Data Retention, Low Power	LP
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
- Micron Semiconductor Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

C – PROCESS TECHNOLOGY
- LOW VOLTAGE (3.3V) L

DDD – RAM FAMILY
- DRAM ..... D
- DRAM TSOP ..... DT
- SRAM ..... S
- SRAM TSOP ..... ST
- SYNCHRONOUS SRAM ..... SY
- SYNCHRONOUS SRAM TQFP ..... SYT

EEE – DEPTH

FFF – WIDTH

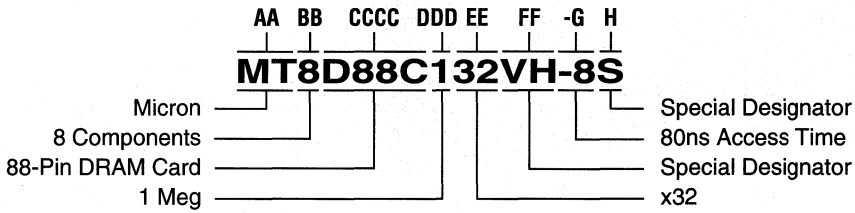
GG – DEVICE VERSIONS
- Specified by individual data sheet (Synchronous SRAM only)

HH – PACKAGE CODE
- Gold Plated SIMM/DIMM ..... G
- ZIP ..... Z
- SIP ..... N
- SIMM/DIMM ..... M
- Small Outline DIMM ..... H
- Small Outline Gold DIMM ..... HG
- Double-Sided SIMM (1 or 4 Meg x 36 Only) ..... DM
- Double-Sided SIMM (Gold 1 or 4 Meg x 36 Only) ..... DG

JJ – ACCESS TIME
- -10 ..... 10ns
- -12 ..... 12ns
- -15 ..... 15ns
- -17 ..... 17ns
- -20 ..... 20ns
- -25 ..... 25ns
- -35 ..... 35ns
- -6 ..... 60ns
- -7 ..... 70ns
- -8 ..... 80ns

KK – MODULE SPECIAL DESIGNATOR
- SRAM
  - 2V data retention L
  - Low Power ..... P
  - Low Power, 2V data retention ..... LP
- DRAM
  - Low Power (Extended Refresh) L
  - ECC C
  - Extended Data Out X
  - Self Refresh ..... S
  - 16 Meg DRAM 4,096 Refresh ..... B

DRAM CARD NUMBERING SYSTEM



AA – Product Line Identifier
Micron Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

CCCC – DRAM CARD DESIGNATOR AND PIN COUNT
88-Pin DRAM Card D88C

DDD – DEPTH

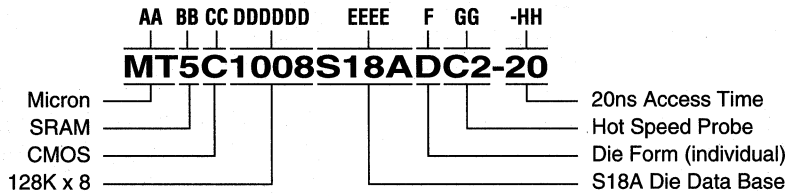
EE – WIDTH

FF – SPECIAL DESIGNATOR
3.3 Volts V
Reduced length (2") ..... H

G – ACCESS TIME
-5 ..... 50ns
-6 ..... 60ns
-7 ..... 70ns
-8 ..... 80ns

H– SPECIAL DESIGNATOR
Self Refresh ..... S

DIE PRODUCT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
Component Product ..... MT

BB – PRODUCT FAMILY
SRAM 5
DRAM 4
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY
CMOS C
Low Voltage CMOS LC

DDDDDD – DEVICE NUMBER
When *no* alpha character appears as part of this section, the section is defined as:
DRAM ..... Width, Density
SRAM ..... Total Bits, Width
Synchronous SRAM ..... Depth, Width

When an alpha character occurs as part of this section, the section is defined as:
Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter ..... Bits
K ..... Kilobits
M ..... Megabits
G ..... Gigabits

EEEE – DIE DATA BASE REVISION

F – FORM
Die Form ..... D
Wafer Form (6" Wafer) ..... W

GG – TESTING LEVELS
Standard Probe (0° to 70°C) C1
Hot Speed Probe (0° to 70°C) C2
Known Good Die (0° to 70°C) C3

HH – ACCESS TIME
(Applicable for C2 and C3 only)
-5 ..... 5ns or 50ns
-6 ..... 6ns or 60ns
-7 ..... 7ns or 70ns
-8 ..... 8ns or 80ns
-9 ..... 9ns or 90ns
-10 ..... 10ns or 100ns
-12 ..... 12ns or 120ns
-15 ..... 15ns or 150ns
-17 ..... 17ns
-20 ..... 20ns
-25 ..... 25ns
-35 ..... 35ns
-45 ..... 45ns
-50 (SRAM only) 50ns
-SS (C2 only) ..... speed sorted

5V ASYNCHRONOUS SRAMs

CE ..... CHIP ENABLE
BE ..... BYTE ENABLE
OE ..... OUTPUT ENABLE
REVOLUTIONARY PINOUT ..... CENTER PIN POWER AND GROUND

3V ASYNCHRONOUS SRAMs

CE ..... CHIP ENABLE
BE ..... BYTE ENABLE
OE ..... OUTPUT ENABLE
REVOLUTIONARY PINOUT ..... CENTER PIN POWER AND GROUND

SYNCHRONOUS SRAMs

SRAM MODULES

CE ..... CHIP ENABLE

OE ..... OUTPUT ENABLE

TECHNICAL NOTES

PRODUCT RELIABILITY

PACKAGE INFORMATION

SALES INFORMATION

NUMERICAL INDEX

NUMERICAL INDEX (continued)

5V ASYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package/No. of Pins		Page
				PDIP	SOJ	
256K x 1	$\overline{CE}$ only	MT5C2561	10, 12, 15, 20, 25	24	24	1-1
1 Meg x 1	$\overline{CE}$ only	MT5C1001	12, 15, 20, 25	28	28	1-11
64K x 4	$\overline{CE}$ only	MT5C2564	10, 12, 15, 20, 25	24	24	1-21
64K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C2565	10, 12, 15, 20, 25	28	28	1-31
256K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C1005	12, 15, 20, 25	28	28	1-41
256K x 4	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5C256K4A1	12, 15, 20, 25	-	32	1-51
32K x 8	$\overline{CE}$ and $\overline{OE}$	MT5C2568	10, 12, 15, 20, 25	28	28	1-61
128K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5C1008	12, 15, 20, 25	32	32	1-71
128K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5C128K8A1	12, 15, 20, 25	-	32	1-81
64K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and Revolutionary Pinout	MT5C64K16A1	12, 15, 20, 25	-	44	1-91

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

3.3V ASYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package/No. of Pins		Page
				PDIP	SOJ	
256K x 1	$\overline{CE}$ only with separate I/O	MT5LC2561	12, 15, 20, 25	24	24	2-1
1 Meg x 1	$\overline{CE}$ only with separate I/O	MT5LC1001	15, 17, 20, 25	28	28	2-9
64K x 4	$\overline{CE}$ only	MT5LC2564	12, 15, 20, 25	24	24	2-17
64K x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC2565	12, 15, 20, 25	28	28	2-25
256K x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC1005	15, 17, 20, 25	28	28	2-33
256K x 4	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC256K4D4	12, 15, 20, 25	-	32	2-41
1 Meg x 4	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC1M4D4	12, 15, 20, 25, 35	-	32	2-51
32K x 8	$\overline{CE}$ and $\overline{OE}$	MT5LC2568	12, 15, 20, 25	28	28	2-59
128K x 8	$\overline{CE}$1, CE2 and $\overline{OE}$	MT5LC1008	15, 17, 20, 25	32	32	2-67
128K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC128K8D4	12, 15, 20, 25	-	32	2-75
512K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC512K8D4	12, 15, 20, 25, 35	-	36	2-85
64K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and Revolutionary Pinout	MT5LC64K16D4	12, 15, 20, 25	-	44	2-93
256K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable	MT5LC256K16D4	12, 15, 20, 25, 35	-	54	2-103

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

SYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Supply Voltage	Control Functions	Part Number	Access Time (ns)	Cycle Time (ns)	Package and Number of Pins			Page
						PLCC	TQFP	DIE	
64K x 18	3.3V	SyncBurst™, Interleaved, Linear	MT58LC64K18B2	9,10,11,12,14	15,15,15,20,20	52	100	CD1/CD2	3-1
64K x 18	3.3V	SyncBurst, Linear	MT58LC64K18M1	9,10,11,12,14	15,15,15,20,20	52	100	CD1/CD2	3-1
64K x 18	3.3V	SyncBurst, Interleaved, Linear	MT58LC64K18C4	4.5,5,6,7,8	8,10,12,15,20	52	100	CD1/CD2	3-17
64K x 18	3.3V	SyncBurst, Linear	MT58LC64K18A6	4.5,5,6,7,8	8,10,12,15,20	52	100	CD1/CD2	3-17
32K x 32	3.3V	SyncBurst	MT58LC32K32B2	9,10,11,12,14	15,15,15,20,20	-	100	CD1/CD2	3-33
32K x 32	3.3V	SyncBurst, Interleaved Burst, Pipelined	MT58LC32K32C4	4.5,5,6,7,8	8,10,12,15,20	-	100	CD1/CD2	3-49
32K x 36	3.3V	SyncBurst, Interleaved Burst	MT58LC32K36B2	9,10,11,12,14	15,15,15,20,20	-	100	CD1/CD2	3-65
32K x 36	3.3V	SyncBurst, Interleaved Burst, Pipelined	MT58LC32K36C4	4.5,5,6,7,8	8,10,12,15,20	-	100	CD1/CD2	3-81

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

SRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and No. of Pins			Page
				ZIP	SIMM	DIMM	
64K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S6432	12, 15, 20, 25	64	64	-	4-1
64K x 32	$\overline{CE}$ and $\overline{OE}$	MT8LS6432	15, 20, 25	64	64	-	4-9
128K x 32	$\overline{CE}$ and $\overline{OE}$	MT4S12832	15, 20, 25	64	64	-	4-17
128K x 32	$\overline{CE}$ and $\overline{OE}$	MT4LS12832	17, 20, 25	64	64	-	4-25
256K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S25632	15, 20, 25	64	64	-	4-33
256K x 32	$\overline{CE}$ and $\overline{OE}$	MT8LS25632	17, 20, 25	64	64	-	4-41
1 Meg x 32	$\overline{CE}$ and $\overline{OE}$	MT8LS132	15, 20, 25, 35	72	72	-	4-49
32K x 64	SyncBurst™, Linear Burst	MT2LSYT3264T1	9, 10, 11, 12	-	-	160	4-57
32K x 64	SyncBurst, Interleaved Burst	MT2LSYT3264T2	9, 10, 11, 12	-	-	160	4-57
32K x 64	SyncBurst, Interleaved Burst, Pipelined	MT2LSYT3264T4	5, 6, 7, 8	-	-	160	4-69
32K x 64	SyncBurst, Linear Burst, Pipelined	MT2LSYT3264T6	5, 6, 7, 8	-	-	160	4-69
32K x 64	SyncBurst, Linear/Interleaved Burst	MT2LSYT3264B2	9, 10, 11, 12	-	-	160	4-81
32K x 64	SyncBurst, Linear/ Interleaved Burst, Pipelined	MT2LSYT3264C4	5, 6, 7, 8	-	-	160	4-87
32K x 72	SyncBurst, Linear Burst	MT2LSYT3272T1	9, 10, 11, 12	-	-	160	4-93
32K x 72	SyncBurst, Interleaved Burst	MT2LSYT3272T2	9, 10, 11, 12	-	-	160	4-93
32K x 72	SyncBurst, Interleaved Burst, Pipelined	MT2LSYT3272T4	5, 6, 7, 8	-	-	160	4-107
32K x 72	SyncBurst, Linear Burst, Pipelined	MT2LSYT3272T6	5, 6, 7, 8	-	-	160	4-107
32K x 72	SyncBurst, Linear/ Interleaved Burst	MT2LSYT3272B2	9, 10, 11, 12	-	-	160	4-121
32K x 72	SyncBurst, Linear/ Interleaved Burst, Pipelined	MT2LSYT3272C4	5, 6, 7, 8	-	-	160	4-129
64K x 72	SyncBurst, Linear Burst	MT4LSY6472T1	9, 10, 11, 12	-	-	160	4-93
64K x 72	SyncBurst, Interleaved Burst	MT4LSY6472T2	9, 10, 11, 12	-	-	160	4-93
64K x 72	SyncBurst, Interleaved Burst, Pipelined	MT4LSY6472T4	5, 6, 7, 8	-	-	160	4-107
64K x 72	SyncBurst, Linear Burst, Pipelined	MT4LSY6472T6	5, 6, 7, 8	-	-	160	4-107
64K x 72	SyncBurst, Linear/ Interleaved Burst	MT4LSYT6472B2	9, 10, 11, 12	-	-	160	4-121
64K x 72	SyncBurst, Linear/ Interleaved Burst, Pipelined	MT4LSYT6472C4	5, 6, 7, 8	-	-	160	4-129

TECHNICAL NOTE SELECTION GUIDE

MICRON SEMICONDUCTOR, INC.

5V ASYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package/No. of Pins		Page
				PDIP	SOJ	
256K x 1	$\overline{CE}$ only	MT5C2561	10, 12, 15, 20, 25	24	24	1-1
1 Meg x 1	$\overline{CE}$ only	MT5C1001	12, 15, 20, 25	28	28	1-11
64K x 4	$\overline{CE}$ only	MT5C2564	10, 12, 15, 20, 25	24	24	1-21
64K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C2565	10, 12, 15, 20, 25	28	28	1-31
256K x 4	$\overline{CE}$ and $\overline{OE}$	MT5C1005	12, 15, 20, 25	28	28	1-41
256K x 4	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5C256K4A1	12, 15, 20, 25	-	32	1-51
32K x 8	$\overline{CE}$ and $\overline{OE}$	MT5C2568	10, 12, 15, 20, 25	28	28	1-61
128K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5C1008	12, 15, 20, 25	32	32	1-71
128K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5C128K8A1	12, 15, 20, 25	-	32	1-81
64K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and Revolutionary Pinout	MT5C64K16A1	12, 15, 20, 25	-	44	1-91

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

SRAM

256K x 1 SRAM

FEATURES

- High speed: 10, 12, 15, 20 and 25
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible

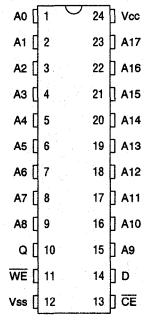
OPTIONS MARKING

- Timing
  - 10ns access -10
  - 12ns access -12
  - 15ns access -15
  - 20ns access -20
  - 25ns access -25
- Packages
  - Plastic DIP (300 mil) None
  - Plastic SOJ (300 mil) DJ
- 2V data retention (optional) L
- Low power (optional) P
- Temperature
  - Commercial (0°C to +70°C) None
  - Industrial (-40°C to +85°C) IT
  - Automotive (-40°C to +125°C) AT
  - Extended (-55°C to +125°C) XT
- Part Number Example: MT5C2561DJ-15 P

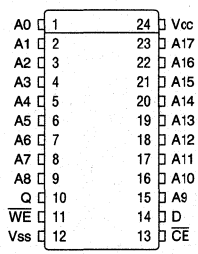
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

24-Pin DIP (SA-3)



24-Pin SOJ (SD-1)



GENERAL DESCRIPTION

The MT5C2561 is organized as a 262,144 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

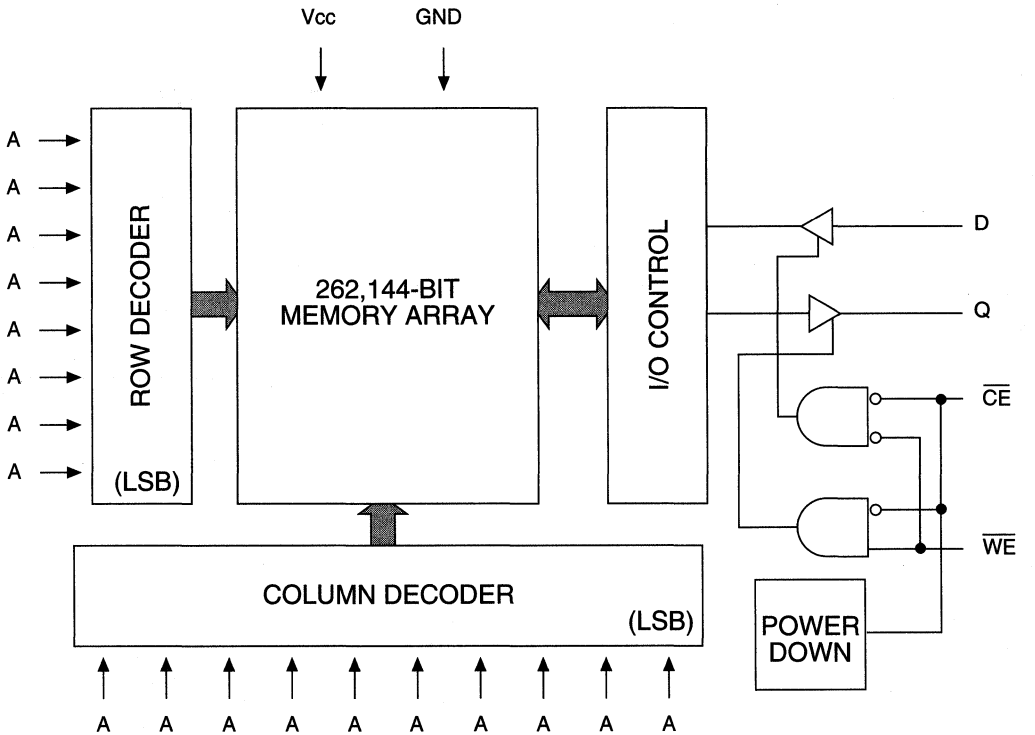
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'T CARE	HIGH-Z	STANDBY
READ	L	H	DON'T CARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10†	-12†	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	130	200	180	165	150	140	mA	3, 13
	P version	I_{CC}	100	-	-	140	125	120	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	24	55	50	45	40	35	mA	13
	P version	I_{SB1}	1.4	-	-	4	4	4	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	5	mA	13
	P version	I_{SB2}	0.4	-	-	3	3	3	mA	13

†P version not available with this speed.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	SYM	-10		-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle													
READ cycle time	^tRC	10		12		15		20		25		ns	
Address access time	^tAA		10		12		15		20		25	ns	
Chip Enable access time	^tACE		10		12		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		3		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		8		9		9	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	4
Chip disable to power-down time	^tPD		10		12		15		20		25	ns	4
WRITE Cycle													
WRITE cycle time	^tWC	10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		ns	
Chip Enable to end of write (P and LP version)	^tCW	-		-		12		12		15		ns	
Address valid to end of write	^tAW	7		8		10		12		15		ns	
Address valid to end of write (P and LP version)	^tAW	-		-		12		12		15		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		ns	
WRITE pulse width	^tWP	7		8		10		12		15		ns	
Data setup time	^tDS	6		7		7		10		10		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C2561 SRAMs.
(-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-10**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	210	190	170	160	150	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	65	60	50	45	40	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	6	6	6	6	6	mA	

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 125°C - AT; -55°C ≤ T_A ≤ 125°C - XT; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	7
WRITE Cycle											
Address hold from end of write	^tAH	2		2		2		2		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage		V_{IH}	2.3	V_{CC} +1	V	1

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C2561 SRAMs.
(-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	195	175	165	155	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	7	7	7	7	mA	

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ± 10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	7
WRITE Cycle											
Address hold from end of write	^tAH	2		2		2		2		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 85°C)

DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage		V_{IH}	2.3	V_{CC} +1	V	1

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

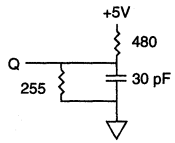


Fig. 1 OUTPUT LOAD EQUIVALENT

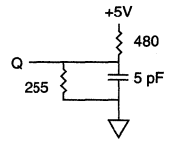


Fig. 2 OUTPUT LOAD EQUIVALENT

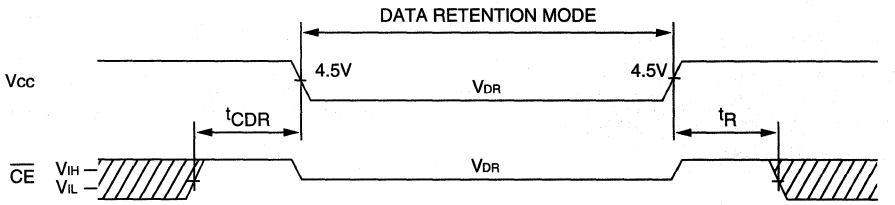
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

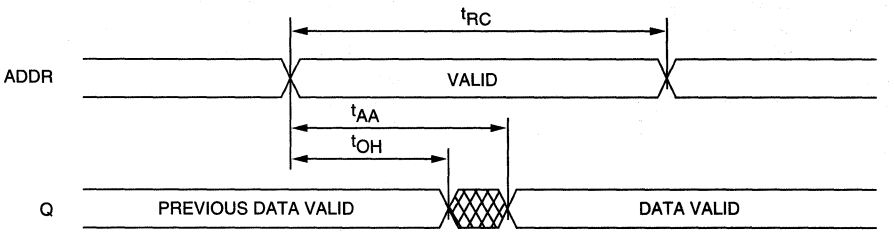
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		125	300	µA	14
		Vcc = 3V	ICCDR		175	500	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		100	300	µA	14
		Vcc = 3V	ICCDR		150	500	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

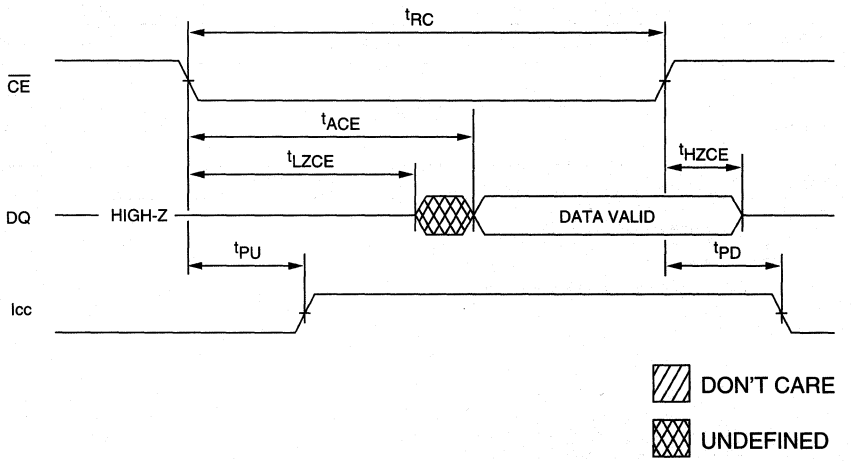
LOW Vcc DATA RETENTION WAVEFORM



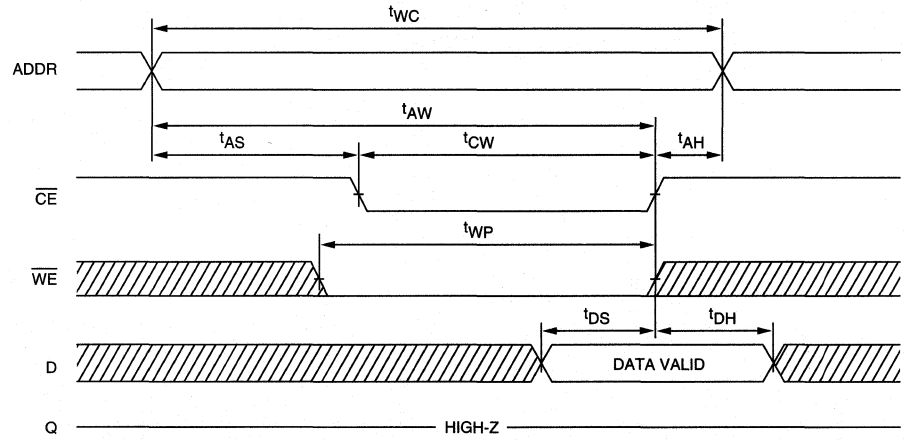
READ CYCLE NO. 1 [8, 9]



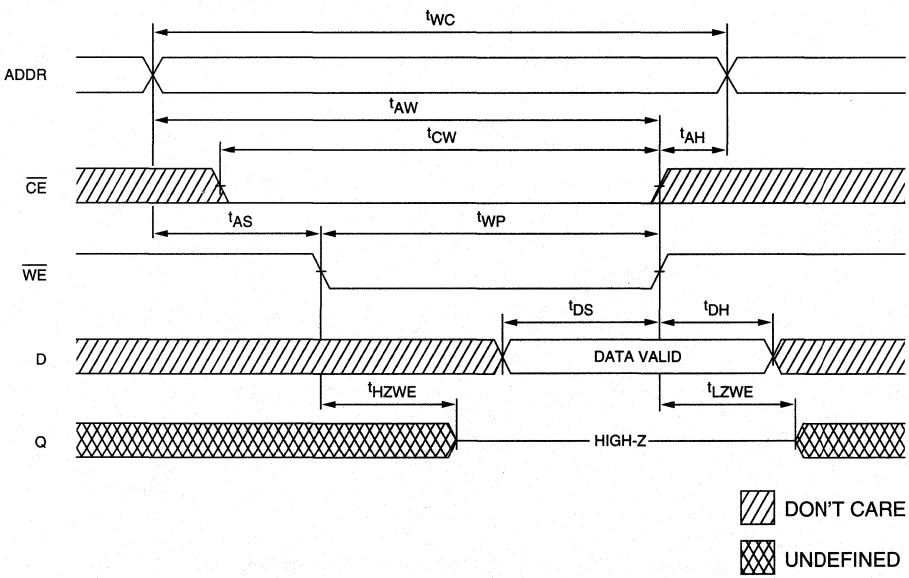
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

1 MEG x 1 SRAM

FEATURES

- High speed: 12, 15, 20 and 25
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible

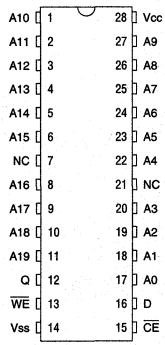
OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic DIP (400 mil) — None
  - Plastic SOJ (400 mil) — DJ
- 2V data retention (optional) — L
- 2V data retention, low power (optional) — LP
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5C1001DJ-20 L

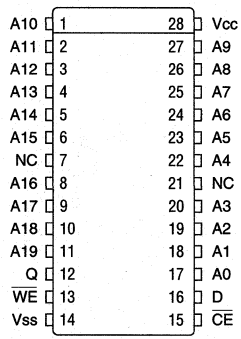
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-5)



28-Pin SOJ
(SD-3)



GENERAL DESCRIPTION

The MT5C1001 is organized as a 1,048,576 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

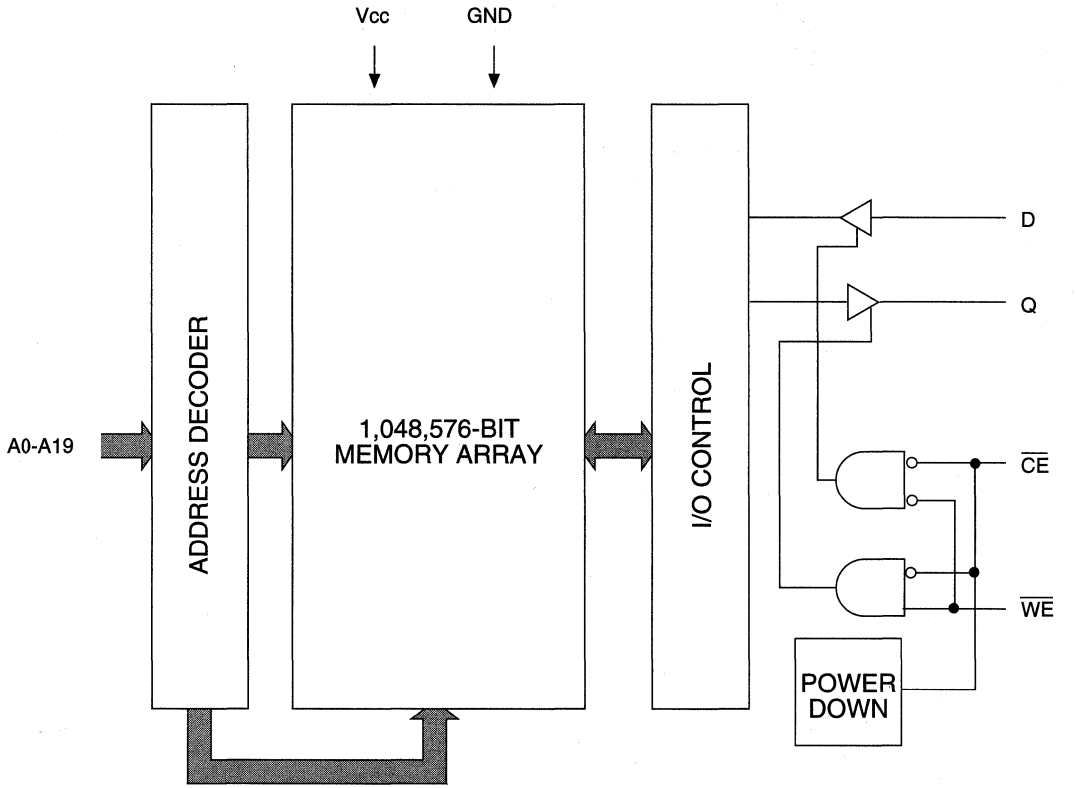
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "L" and "LP" versions each provide a 70 percent reduction in CMOS standby current (I_{SB2}) over the standard version. The LP version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'T CARE	HIGH-Z	STANDBY
READ	L	H	DON'T CARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	107	195	170	145	130	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	37	75	65	50	45	mA	13
	LP version only	I_{SB1}	1.3	3	3	3	3	mA	13
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	13
	L and LP versions only	I_{SB2}	0.3	1.5	1.5	1.5	1.5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	3		3				5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		10	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	8		10		12		15		ns	
Address valid to end of write	^tAW	8		10		12		15		ns	
Address setup time	^tAS	0		0		0		0			
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	^tWP	8		9		12		15		ns	
Data setup time	^tDS	6		7		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		10	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1001 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	107	155	140	130	125	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	37	50	45	40	40	mA	13
LP version only	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	1.3	6	6	6	6	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	13
L version and LP version	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	2	2	2	2	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1}$ ≥ (V_{CC} -0.2V) or CE2 ≤ (V_{SS} +0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	170	µA	14
		V_{CC} = 3V	I_{CCDR}		60	325	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 85°C; V_{CC} = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
WRITE Cycle											
Address hold from end of write	^tAH	1		1		1		1		ns	

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1001 SRAMs.
(-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	107	155	140	130	125	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	37	60	55	50	47	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	7	7	7	7	mA	13
L version only	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1}$ ≥ (V_{CC} -0.2V) or CE2 ≤ (V_{SS} +0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	1,000	µA	14
		V_{CC} = 3V	I_{CCDR}		60	1,500	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C - AT; -55°C ≤ T_A ≤ 125°C - XT; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	7
WRITE Cycle											
Address hold from end of write	^tAH	1		1		1		1		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

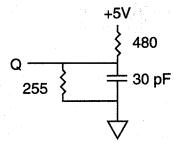


Fig. 1 OUTPUT LOAD EQUIVALENT

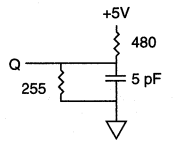


Fig. 2 OUTPUT LOAD EQUIVALENT

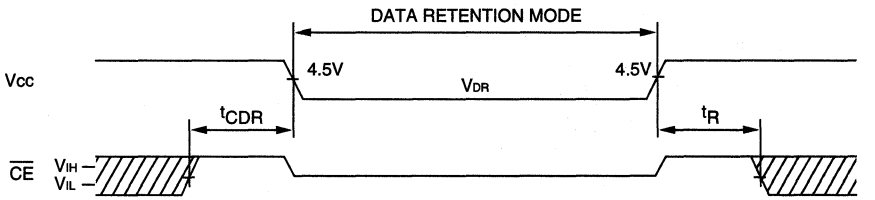
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.
14. Typical currents are measured at 25°C.

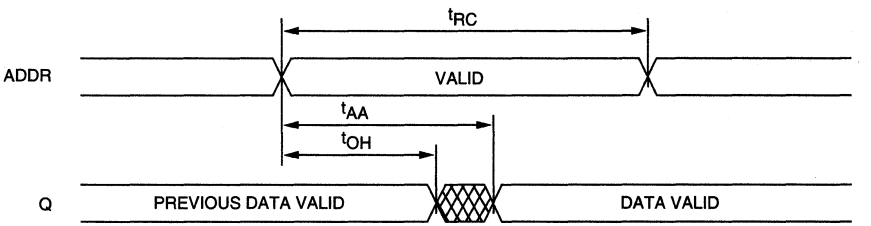
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		35	150	µA	14
		Vcc = 3V	ICCDR		60	250	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		35	150	µA	14
		Vcc = 3V	ICCDR		60	250	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

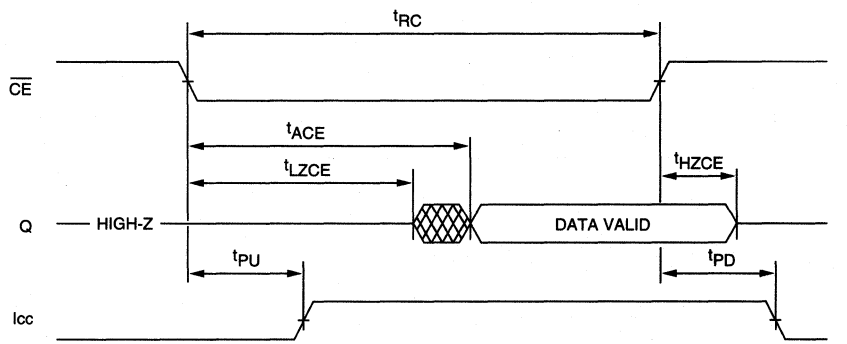
LOW Vcc DATA RETENTION WAVEFORM



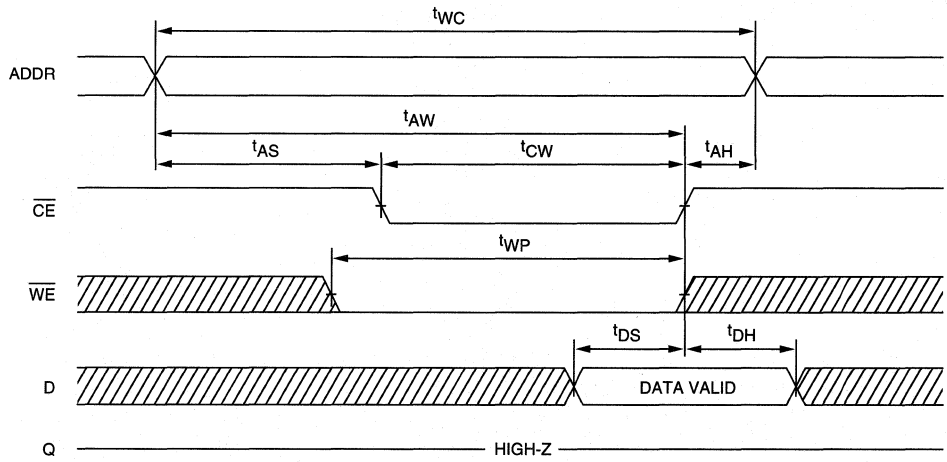
READ CYCLE NO. 1 [8, 9]



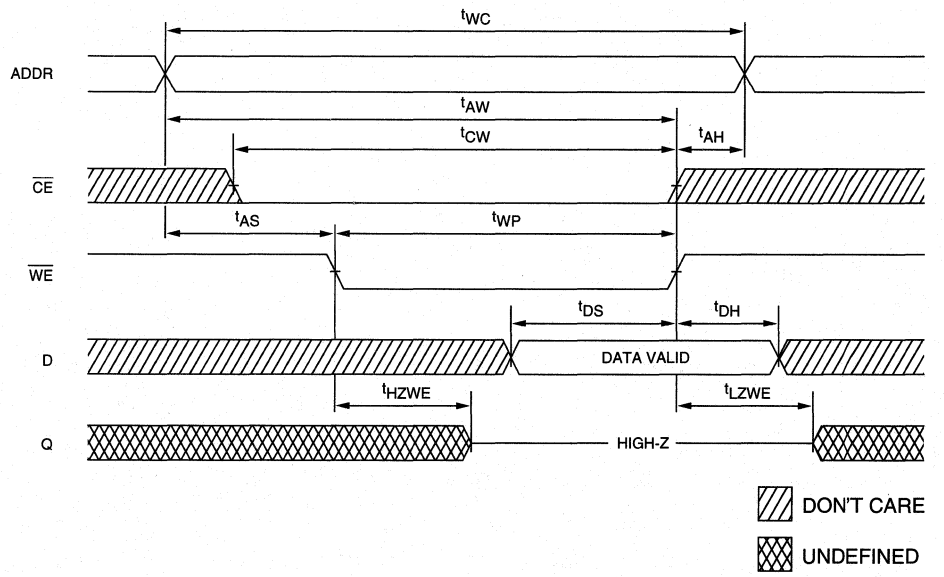
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

64K x 4 SRAM

FEATURES

- High speed: 10, 12, 15, 20 and 25
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible

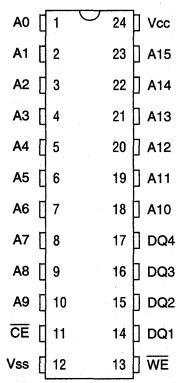
OPTIONS MARKING

- Timing
  - 10ns access -10
  - 12ns access -12
  - 15ns access -15
  - 20ns access -20
  - 25ns access -25
- Packages
  - Plastic DIP (300 mil) None
  - Plastic SOJ (300 mil) DJ
- 2V data retention (optional) L
- Low power (optional) P
- Temperature
  - Commercial (0°C to +70°C) None
  - Industrial (-40°C to +85°C) IT
  - Automotive (-40°C to +125°C) AT
  - Extended (-55°C to +125°C) XT
- Part Number Example: MT5C2564DJ-15 L

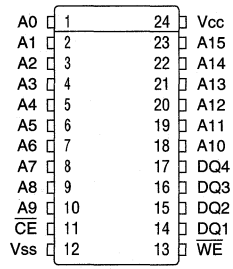
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

24-Pin DIP (SA-3)



24-Pin SOJ (SD-1)



GENERAL DESCRIPTION

The MT5C2564 is organized as a 65,536 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

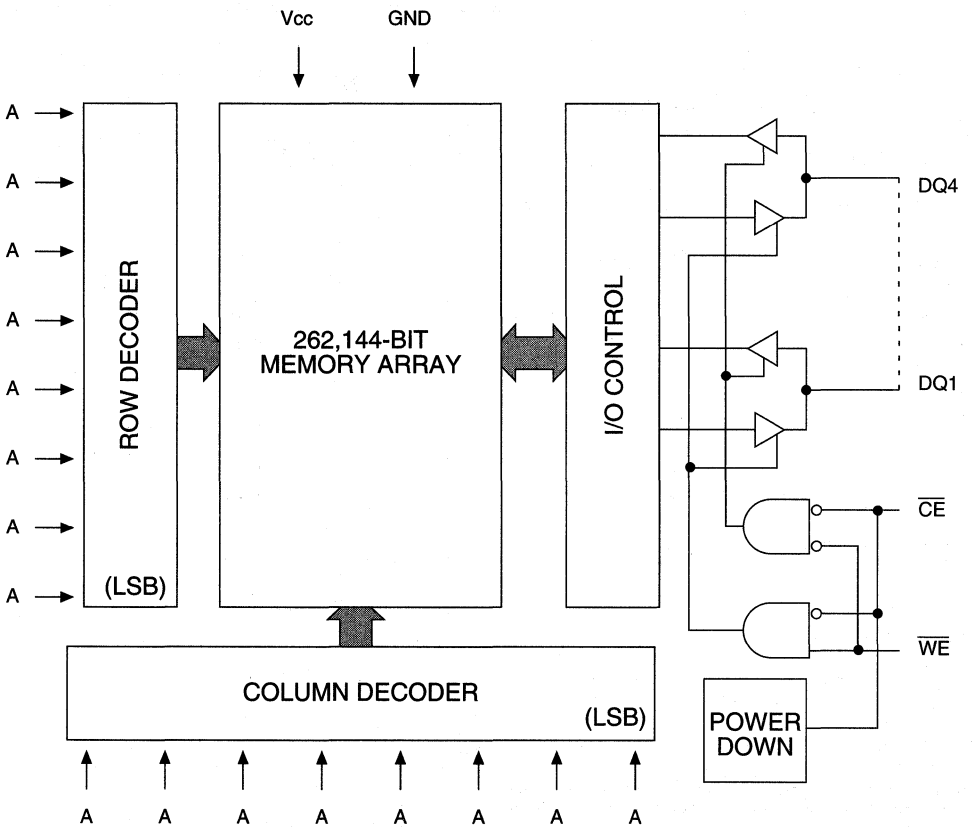
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10†	-12†	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	130	200	180	165	150	140	mA	3, 13
	P version	I_{CC}	100	-	-	140	125	120	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	24	55	50	45	40	35	mA	13
	P version	I_{SB1}	1.4	-	-	4	4	4	mA	13
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	7	mA	13
	P version	I_{SB2}	0.4	-	-	3	3	3	mA	13

†P version not available with this speed.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	Vcc = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYM	-10		-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle													
READ cycle time	^tRC	10		12		15		20		25		ns	
Address access time	^tAA		10		12		15		20		25	ns	
Chip Enable access time	^tACE		10		12		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		3		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		8		9		9	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	4
Chip disable to power-down time	^tPD		10		12		15		20		25	ns	4
WRITE Cycle													
WRITE cycle time	^tWC	10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		ns	
Chip Enable to end of write (P and LP version)	^tCW	-		-		12		12		15		ns	
Address valid to end of write	^tAW	7		8		10		12		15		ns	
Address valid to end of write (P and LP version)	^tAW	-		-		12		12		15		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		ns	
WRITE pulse width	$^tWP1$	7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	10		12		12		15		15		ns	
Data setup time	^tDS	6		7		7		10		10		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C2564 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-10**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	210	190	170	160	150	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	65	60	50	45	40	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	6	6	6	6	6	mA	

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	7
WRITE Cycle											
Address hold from end of write	^tAH	2		2		2		2		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 85°C)

DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage		V_{IH}	2.3	V_{CC} +1	V	1

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C2564 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	195	175	165	155	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	7	7	7	7	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 125°C - AT; -55°C ≤ T_A ≤ 125°C - XT; V_{CC} = 5V ±10%)

DESCRIPTION		**-12**		**-15**		**-20**		**-25**			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	7
WRITE Cycle											
Address hold from end of write	^tAH	2		2		2		2		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage		V_{IH}	2.3	V_{CC} +1	V	1

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

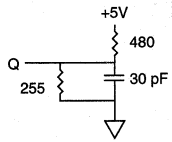


Fig. 1 OUTPUT LOAD EQUIVALENT

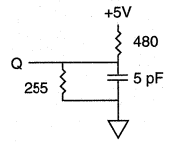


Fig. 2 OUTPUT LOAD EQUIVALENT

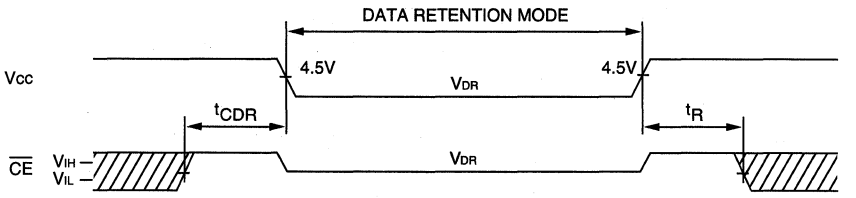
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE and ^{t}HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

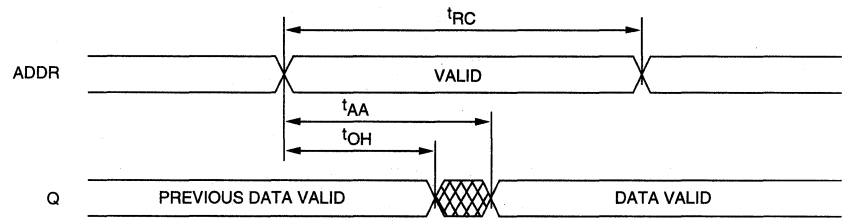
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		125	300	µA	14
		Vcc = 3V	ICCDR		175	500	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		100	300	µA	14
		Vcc = 3V	ICCDR		150	500	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 10

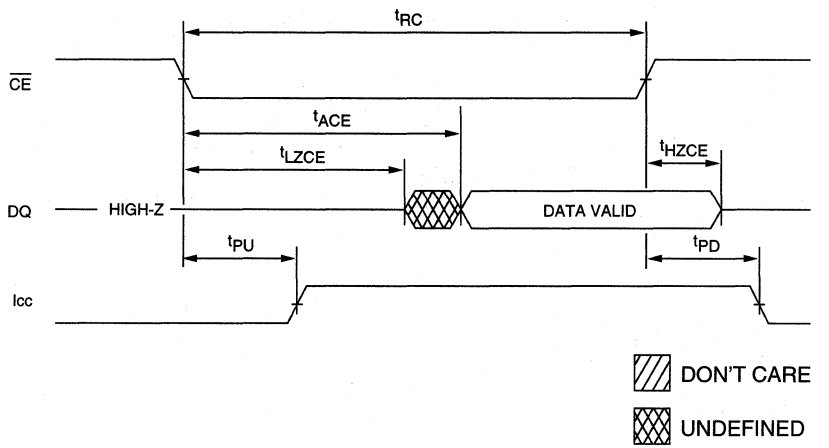
LOW Vcc DATA RETENTION WAVEFORM



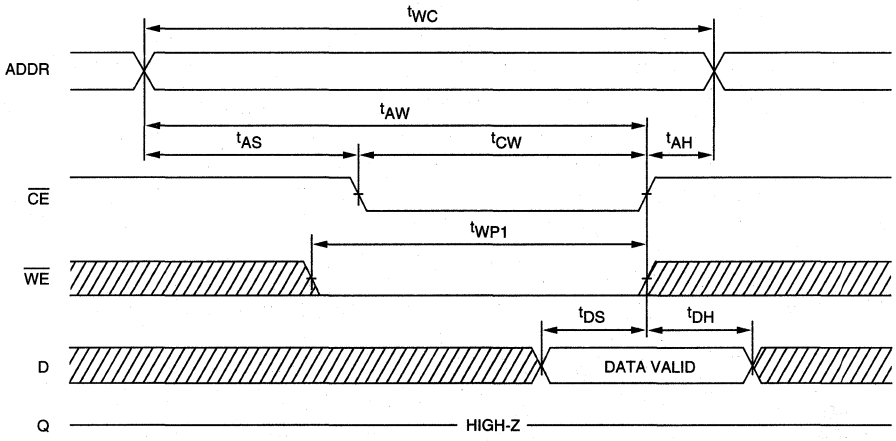
READ CYCLE NO. 1 [8, 9]



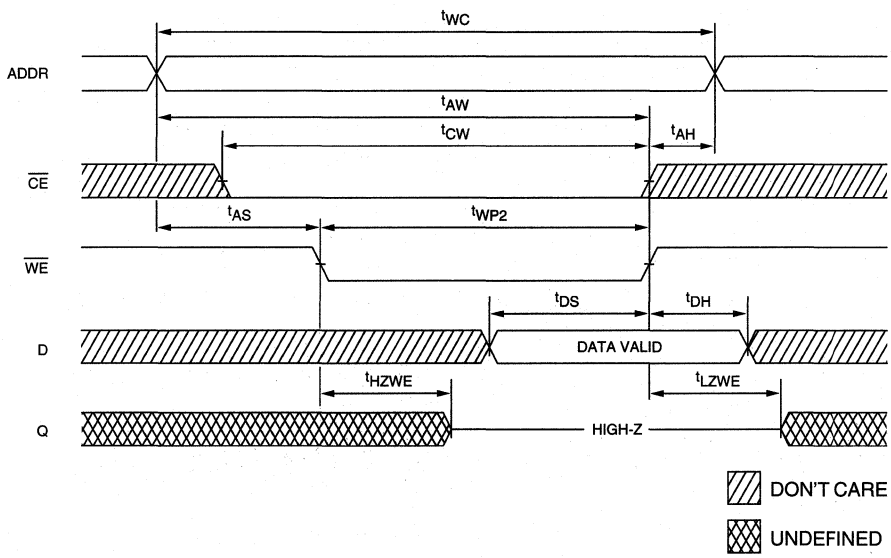
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

64K x 4 SRAM
WITH OUTPUT ENABLE

FEATURES
- High speed: 10, 12, 15, 20 and 25
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible

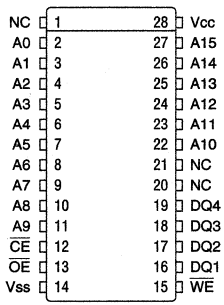
OPTIONS — MARKING

- Timing
  - 10ns access — -10
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
- 2V data retention (optional) — L
- Low power (optional) — P
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5C2565DJ-15 L

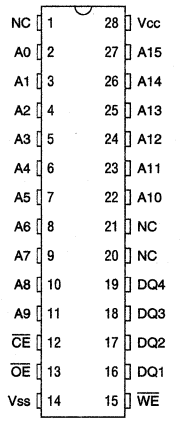
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin SOJ (SD-2)



28-Pin DIP (SA-4)



GENERAL DESCRIPTION

The MT5C2565 is organized as a 65,536 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

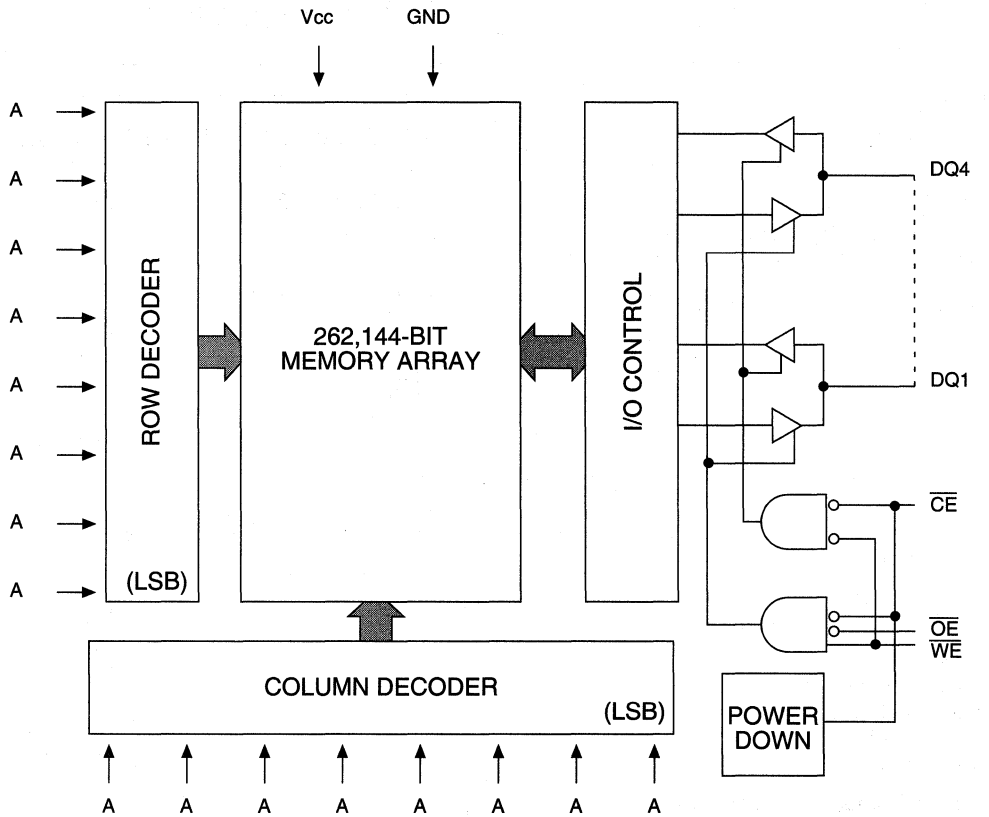
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10†	-12†	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	130	200	180	165	150	140	mA	3, 13
	P version	I_{CC}	100	-	-	140	125	120	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	24	55	50	45	40	35	mA	13
	P version	I_{SB1}	1.4	-	-	4	4	4	mA	13
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	7	mA	13
	P version	I_{SB2}	0.4	-	-	3	3	3	mA	13

†P version not available with this speed.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	Vcc = 5V	Co	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	10		12		15		20		25		ns	
Address access time	^tAA		10		12		15		20		25	ns	
Chip Enable access time	^tACE		10		12		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		3		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		8		9		9	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	4
Chip disable to power-down time	^tPD		10		12		15		20		25	ns	4
Output Enable access time	^tAOE		5		6		8		8		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to out put in High-Z	^tHZOE		5		6		6		7		7	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		ns	
Chip Enable to end of write (P and LP version)	^tCW	-		-		12		12		15		ns	
Address valid to end of write	^tAW	7		8		10		12		15		ns	
Address valid to end of write (P and LP version)	^tAW	-		-		12		12		15		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		ns	
WRITE pulse width	$^tWP1$	7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	10		12		12		15		15		ns	
Data setup time	^tDS	6		7		7		10		10		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C2565 SRAMs.
(-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-10**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	210	190	170	160	150	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	65	60	50	45	40	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	6	6	6	6	6	mA	

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current L version	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	
Data Retention Current LP version	$\overline{CE}$ ≥ (V_{CC} -0.2V)	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 125°C - AT; -55°C ≤ T_A ≤ 125°C - XT; V_{CC} = 5V ±10%)

DESCRIPTION		**-12**		**-15**		**-20**		**-25**			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	7
WRITE Cycle											
Address hold from end of write	^tAH	2		2		2		2		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage		V_{IH}	2.3	V_{CC} +1	V	1

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C2565 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	195	175	165	155	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	7	7	7	7	mA	

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current L version	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	
Data Retention Current LP version	$\overline{CE}$ ≥ (V_{CC} -0.2V)	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 125°C; -55°C ≤ T_A ≤ 125°C; V_{CC} = 5V ±10%)

DESCRIPTION		**-12**		**-15**		**-20**		**-25**			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	7
WRITE Cycle											
Address hold from end of write	^tAH	2		2		2		2		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 85°C)

DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage		V_{IH}	2.3	V_{CC} +1	V	1

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

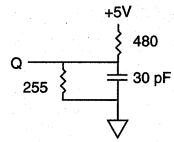


Fig. 1 OUTPUT LOAD EQUIVALENT

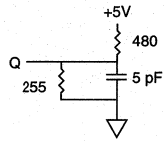


Fig. 2 OUTPUT LOAD EQUIVALENT

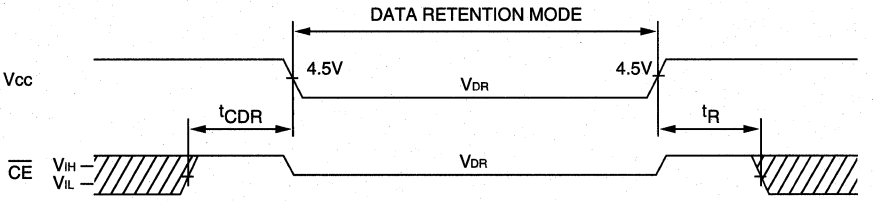
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

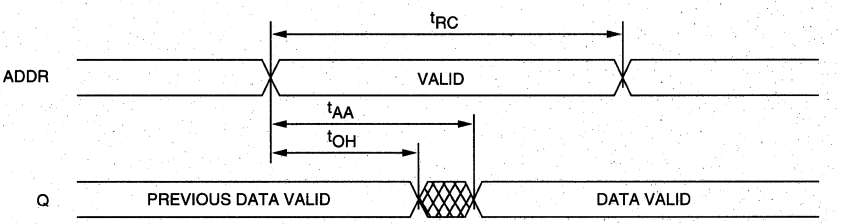
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		125	300	µA	14
		Vcc = 3V	ICCDR		175	500	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		100	300	µA	14
		Vcc = 3V	ICCDR		150	500	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

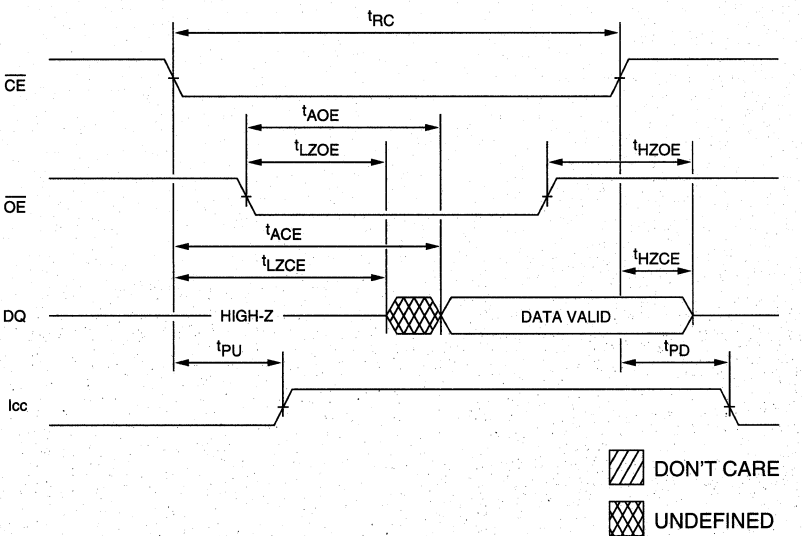
LOW Vcc DATA RETENTION WAVEFORM



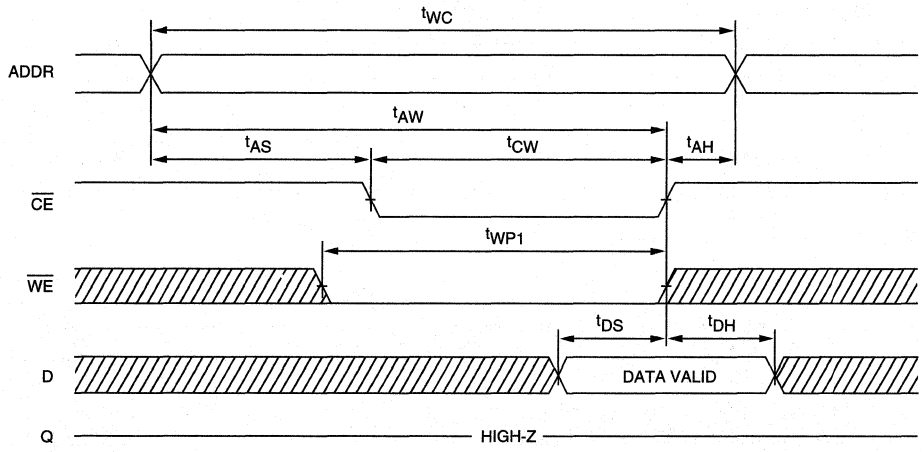
READ CYCLE NO. 1 [8, 9]



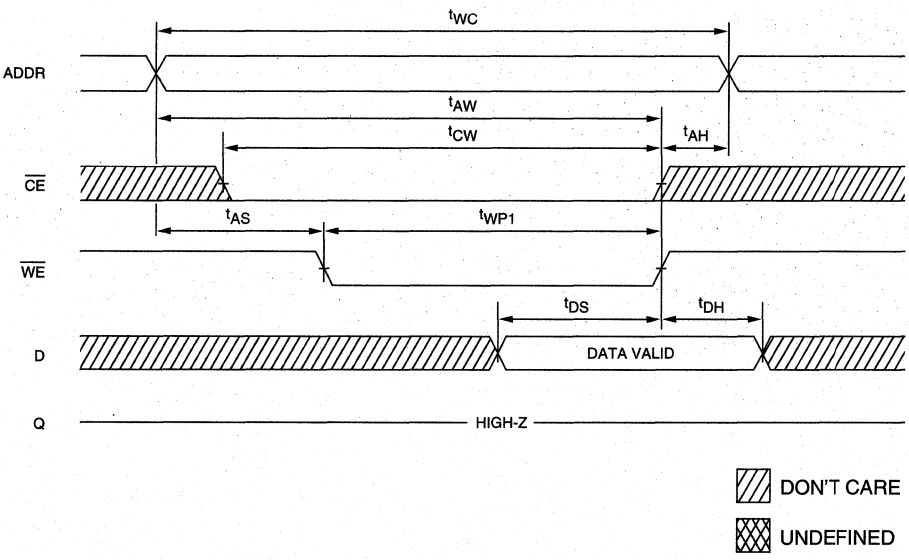
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

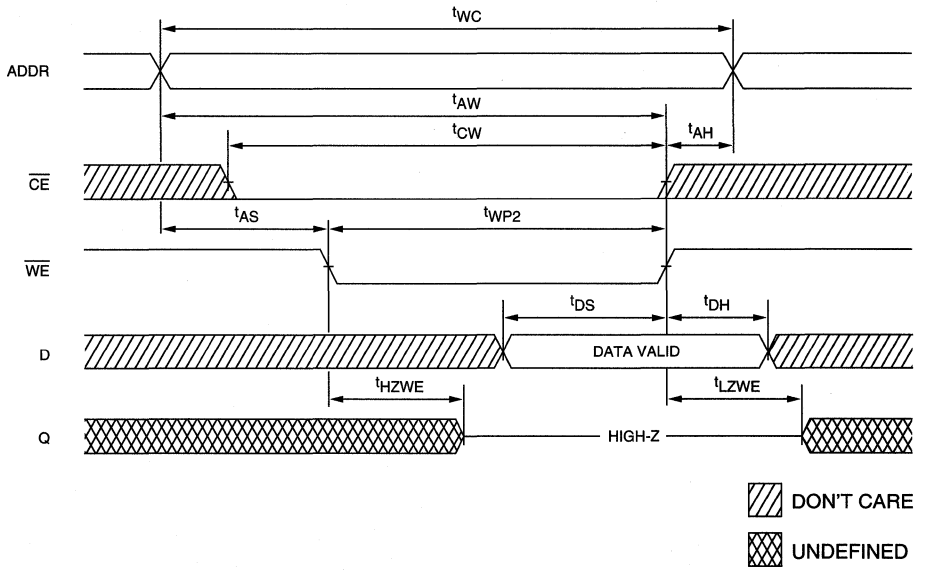


WRITE CYCLE NO. 2 [7, 12, 15]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

256K x 4 SRAM

WITH OUTPUT ENABLE

FEATURES

- High speed: 12, 15, 20 and 25
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6ns

OPTIONS

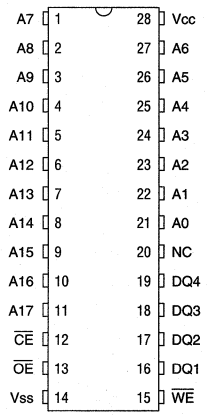
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
• Packages	
Plastic DIP (400 mil)	None
Plastic SOJ (400 mil)	DJ
• 2V data retention (optional)	L
• 2V data retention, low power (optional)	LP
• Temperature	
Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

- Part Number Example: MT5C1005DJ-20 L

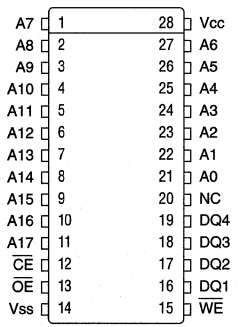
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-5)



28-Pin SOJ
(SD-3)



GENERAL DESCRIPTION

The MT5C1005 is organized as a 262,144 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

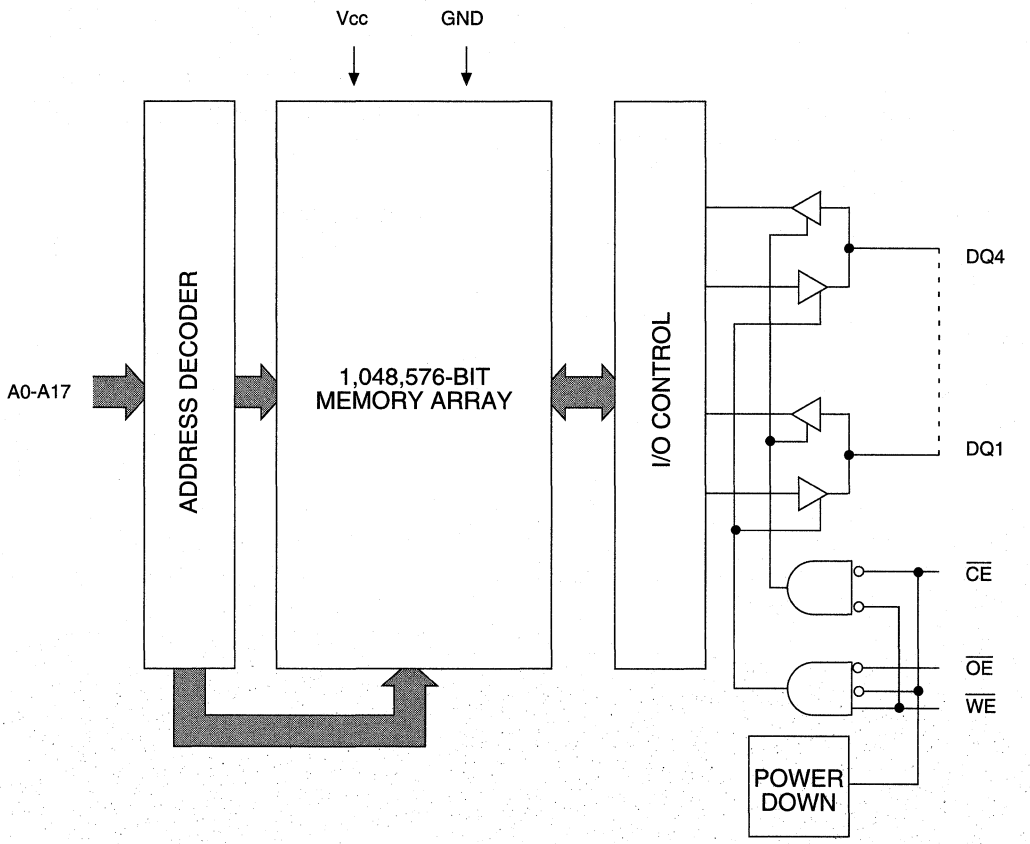
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "L" and "LP" versions each provide a 70 percent reduction in CMOS standby current (I_{SB2}) over the standard version. The LP version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	107	195	170	145	130	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	37	75	65	50	45	mA	13
	LP version only	I_{SB1}	1.3	3	3	3	3	mA	13
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	13
	L and LP versions only	I_{SB2}	0.3	1.5	1.5	1.5	1.5	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYM	-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		10	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		5		6		6		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4		5		6		10	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	8		10		12		15		ns	
Address valid to end of write	^tAW	8		10		12		15		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		12		15		ns	
WRITE pulse width	$^tWP2$	10		12		15		15		ns	
Data setup time	^tDS	6		7		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		10	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1005 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

					MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	107	155	140	130	125	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	37	50	45	40	40	mA	13
LP only	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	1.3	6	6	6	6	mA	13
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	13
L version and LP version	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	2	2	2	2	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1}$ ≥ (V_{CC} -0.2V) or CE2 ≤ (V_{SS} +0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	170	µA	14
		V_{CC} = 3V	I_{CCDR}		60	325	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 85°C; V_{CC} = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
WRITE Cycle											
Address hold from end of write	^tAH	1		1		1		1		ns	

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1005 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE2} \geq V_{IH}$; $\overline{CE1} \leq V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	107	155	140	130	125	mA	3, 13
Power Supply Current: Standby	$\overline{CE2} \leq V_{IH}$ or $\overline{CE1} \geq V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	37	60	55	50	47	mA	13
	$\overline{CE2} \leq V_{SS}$ +0.2V; $\overline{CE1} \geq V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \leq V_{SS}$ +0.2V or $V_{IN} \geq V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	7	7	7	7	mA	13
L version only	$\overline{CE2} \leq V_{SS}$ +0.2V; $\overline{CE1} \geq V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \leq V_{SS}$ +0.2V or $V_{IN} \geq V_{CC}$ -0.2V; f = 0	I_{SB2}	0.3	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1} \geq (V_{CC}$ -0.2V) or $\overline{CE2} \leq (V_{SS}$ +0.2V) $V_{IN} \geq (V_{CC}$ -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	1,000	µA	14
		V_{CC} = 3V	I_{CCDR}		60	1,500	µA	14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C - AT; -55°C ≤ T_A ≤ 125°C - XT; V_{CC} = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	7
WRITE Cycle											
Address hold from end of write	^tAH	1		1		1		1		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

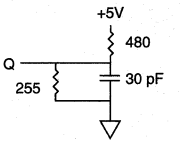


Fig. 1 OUTPUT LOAD EQUIVALENT

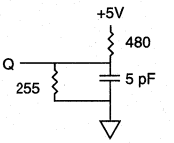


Fig. 2 OUTPUT LOAD EQUIVALENT

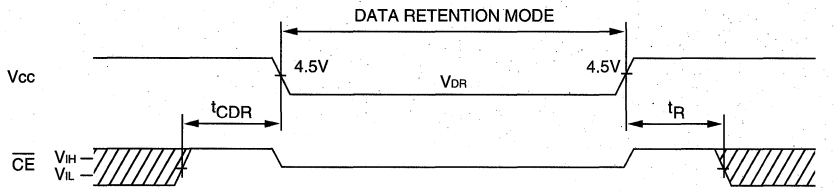
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.
14. Typical currents are measured at 25°C.

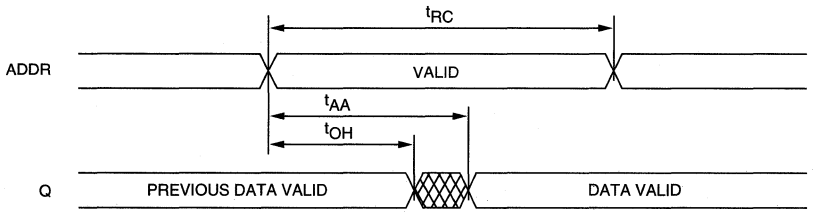
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		35	150	µA	14
		Vcc = 3V	ICCDR		60	250	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		35	150	µA	14
		Vcc = 3V	ICCDR		60	250	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

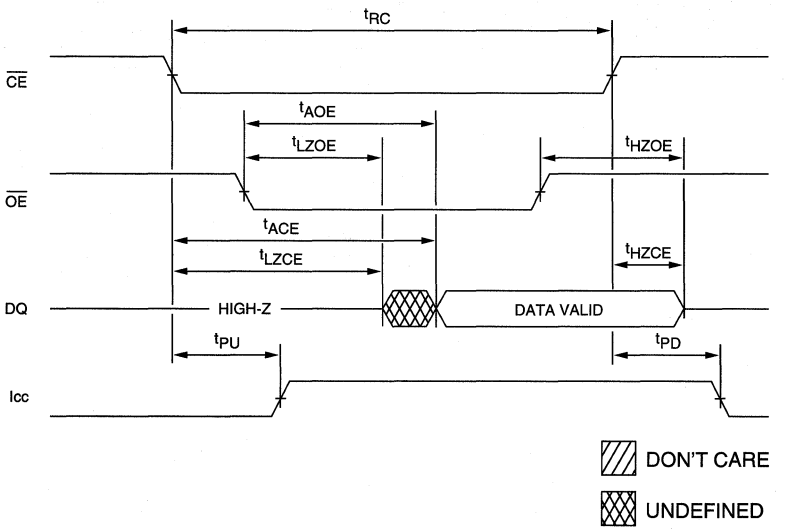
LOW Vcc DATA RETENTION WAVEFORM



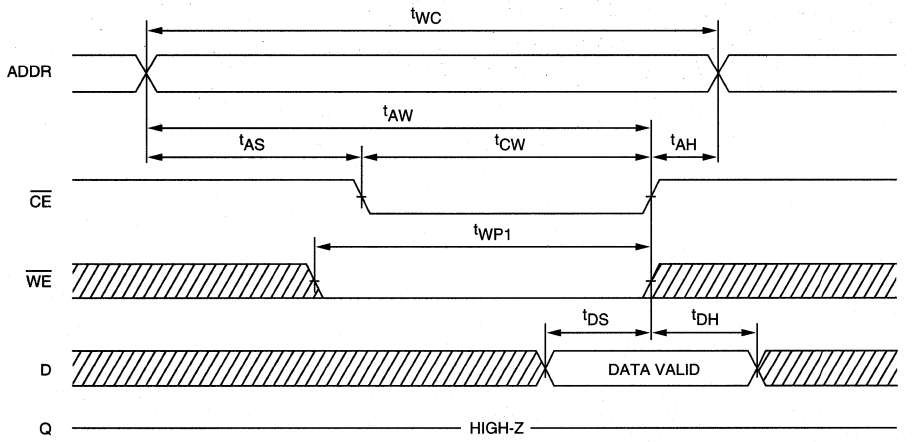
READ CYCLE NO. 1 [8, 9]



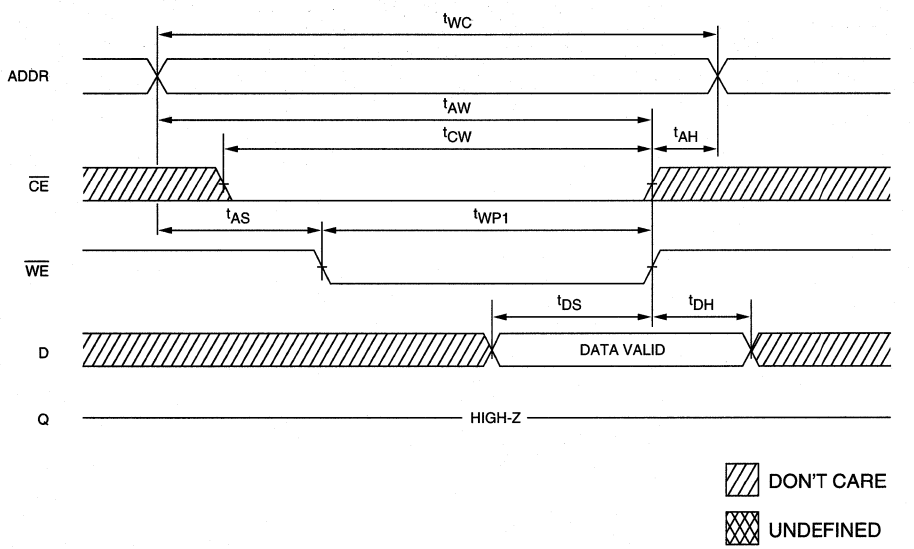
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

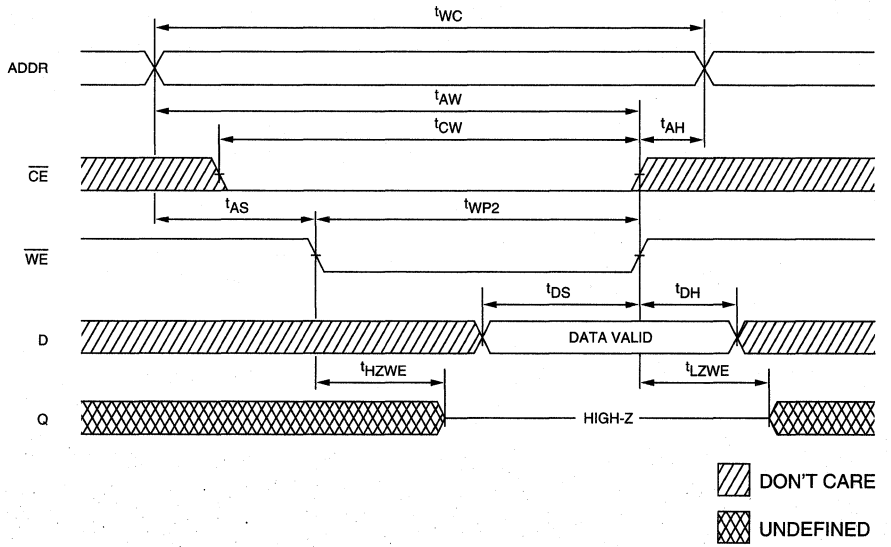


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

256K x 4 SRAM

REVOLUTIONARY PINOUT WITH SINGLE CHIP ENABLE

FEATURES

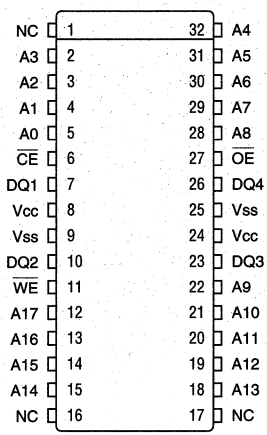
- High speed: 12, 15, 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL-compatible
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Fast $\overline{OE}$ access times: 6, 8, 10 and 12ns

OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 32-pin SOJ (400 mil) — DJ
- 2V data retention (optional) — L
- Temperature
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT5C256K4A1DJ-15 L

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

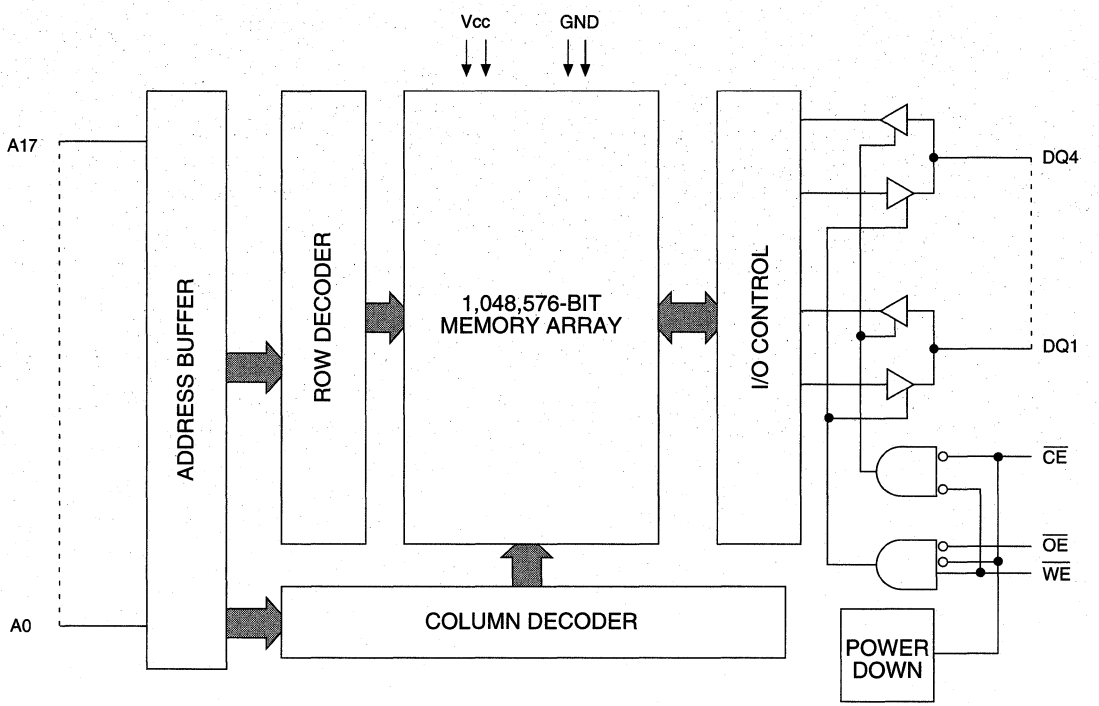
The MT5C256K4A1 is organized as a 262,144 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{OE}$ and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 32, 31, 30, 29, 28, 22, 21, 20, 19, 18, 15, 14, 13, 12	A0-A17	Input	Address Inputs: These inputs determine which cell is addressed.
11	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
6	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
27	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
7, 10, 23, 26	DQ1-DQ4	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	Vcc	Supply	Power Supply: 5V ±10%
9, 25	Vss	Supply	Ground: GND
1, 16, 17	NC	-	No Connect: These signals are not internally connected.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply relative to Vss ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to Vss ..... -1V to Vcc +1V
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	200	330	280	230	200	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	45	80	70	60	50	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.75	5	5	5	7	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 15) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	9		10		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	9		10		12		14		ns	
WRITE pulse width	$^tWP2$	9		10		12		14		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

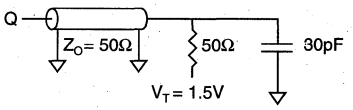


Fig. 1 OUTPUT LOAD EQUIVALENT

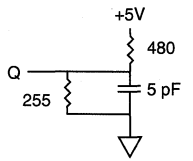


Fig. 2 OUTPUT LOAD EQUIVALENT

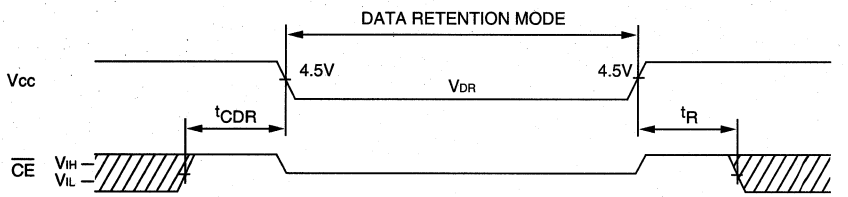
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded and $f = \frac{1}{^{t}RC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical currents are measured at 25°C.
14. Typical values are measured at 25°C, 5V and 15ns cycle time.
15. Contact Micron for extended temperature (IT/AT/XT) timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.

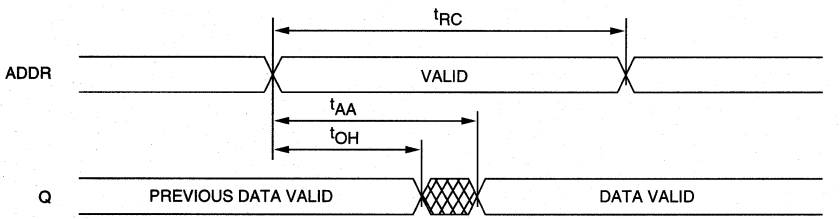
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		70	300	µA	13
		Vcc = 3V	ICCDR		175	500	µA	13
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

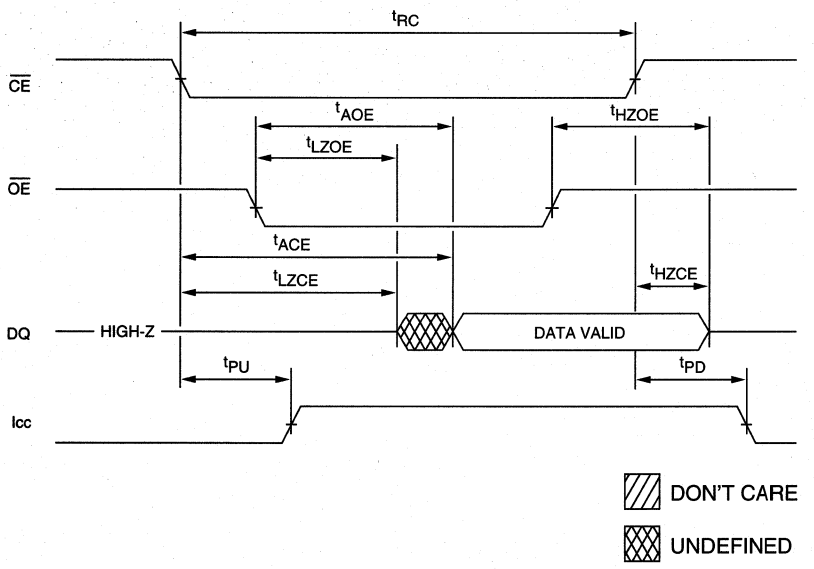
LOW Vcc DATA RETENTION WAVEFORM



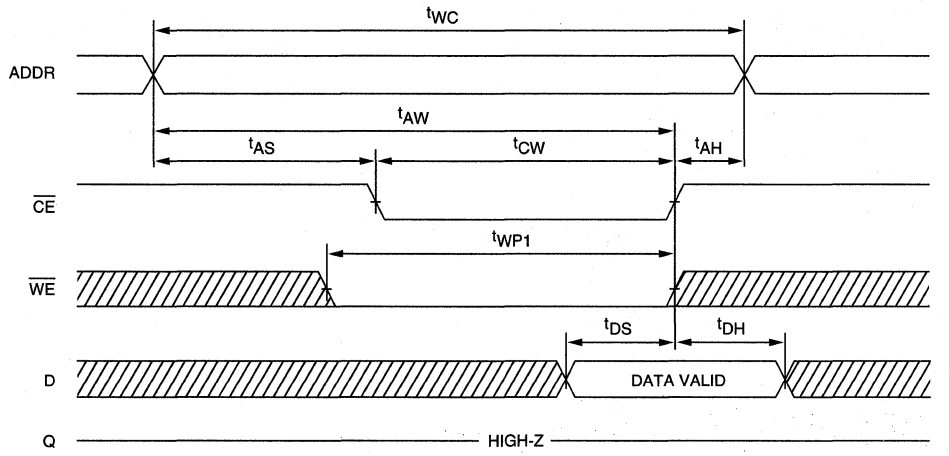
READ CYCLE NO. 1 [8, 9]



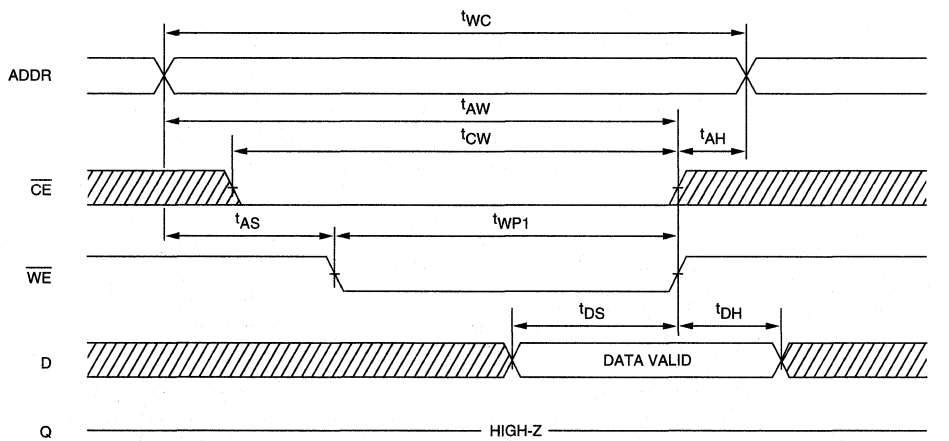
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

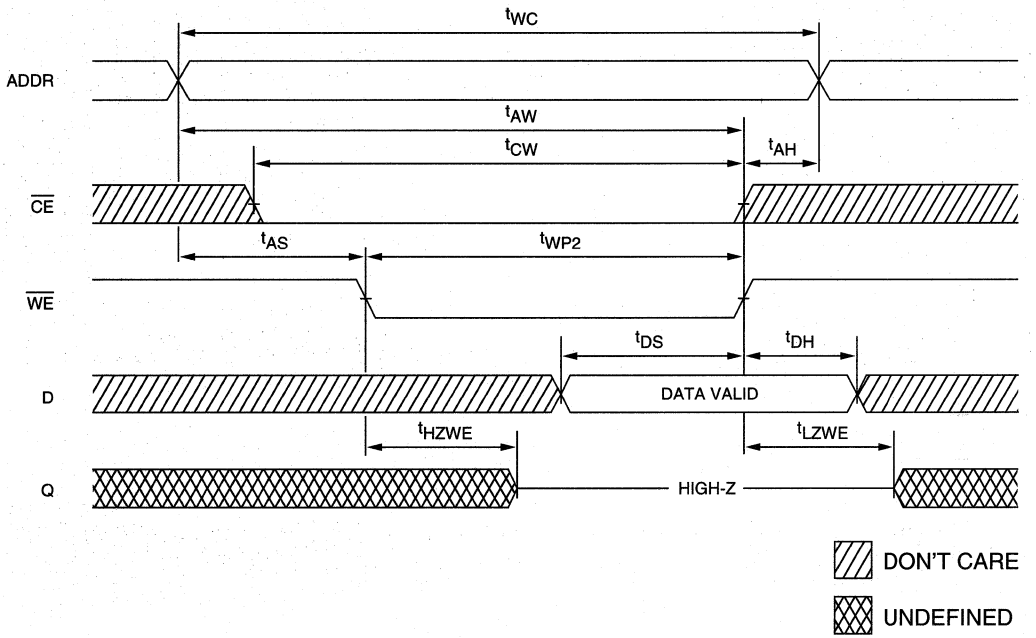


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

32K x 8 SRAM

FEATURES

- High speed: 10, 12, 15, 20 and 25
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible

OPTIONS MARKING

- Timing

10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25

- Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

- 2V data retention (optional) L
- Low power (optional) P
- Temperature

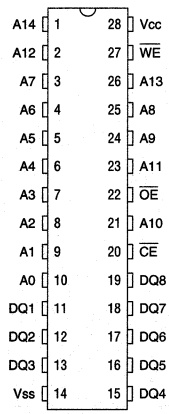
Commercial	(0°C to +70°C)	None
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

- Part Number Example: MT5C2568DJ-20 L

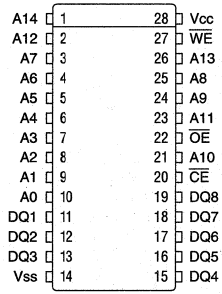
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-4)



28-Pin SOJ (SD-2)



GENERAL DESCRIPTION

The MT5C2568 is organized as a 32,768 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

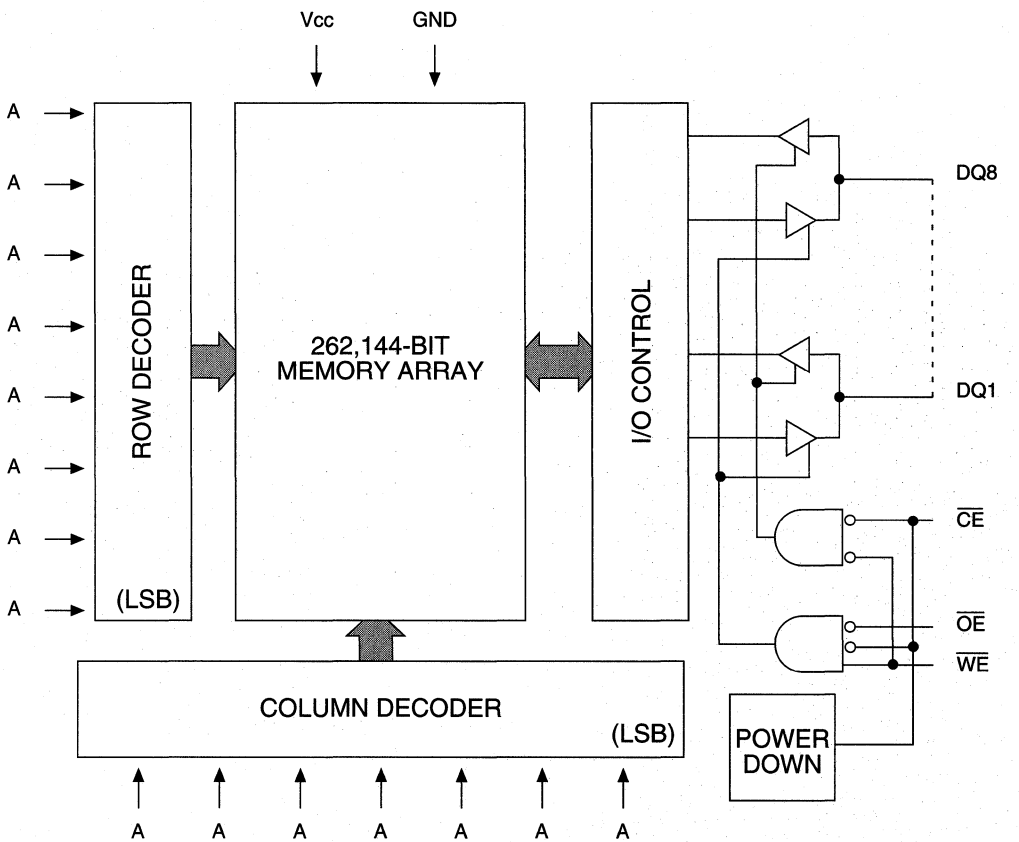
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-10†	-12†	-15†	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	130	200	180	165	150	140	mA	3, 13
	P version	I_{CC}	100	-	-	140	125	120	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	24	55	50	45	40	35	mA	13
	P version	I_{SB1}	1.4	-	-	4	4	4	mA	13
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	5	mA	13
	P version	I_{SB2}	0.4	-	-	3	3	3	mA	13

†P version not available with this speed.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	Vcc = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-10		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	10		12		15		20		25		ns	
Address access time	^tAA		10		12		15		20		25	ns	
Chip Enable access time	^tACE		10		12		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		3		ns	7
Chip disable to output in High-Z	^tHZCE		5		6		8		9		9	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	4
Chip disable to power-down time	^tPD		10		12		15		20		25	ns	4
Output Enable access time	^tAOE		5		6		8		8		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to out put in High-Z	^tHZOE		5		6		6		7		7	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	10		12		15		20		25		ns	
Chip Enable to end of write	^tCW	7		8		10		12		15		ns	
Chip Enable to end of write (P and LP version)	^tCW	-		-		12		12		15		ns	
Address valid to end of write	^tAW	7		8		10		12		15		ns	
Address valid to end of write (P and LP version)	^tAW	-		-		12		12		15		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		1		ns	
WRITE pulse width	$^tWP1$	7		8		10		12		15		ns	
WRITE pulse width	$^tWP2$	10		12		12		15		15		ns	
Data setup time	^tDS	6		7		7		10		10		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		2		2		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		7		8		10	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C2568 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

			MAX						
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-10**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	210	190	170	160	150	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	65	60	50	45	40	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	6	6	6	6	6	mA	

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	400	µA	
		V_{CC} = 3V	I_{CCDR}	600	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 85°C)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	7
WRITE Cycle											
Address hold from end of write	^tAH	2		2		2		2		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 85°C)

DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage		V_{IH}	2.3	V_{CC} +1	V	1

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C2568 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

			MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**-12**	**-15**	**-20**	**-25**	**UNITS**	**NOTES**
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	195	175	165	155	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	60	50	45	40	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	7	7	7	7	mA	

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 125°C - AT; -55°C ≤ T_A ≤ 125°C - XT; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
Output hold from address change	^tOH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	7
WRITE Cycle											
Address hold from end of write	^tAH	2		2		2		2		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

DESCRIPTION	**CONDITIONS**	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Input High (Logic 1) Voltage		V_{IH}	2.3	V_{CC} +1	V	1

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

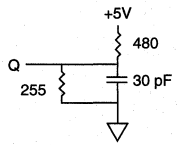


Fig. 1 OUTPUT LOAD EQUIVALENT

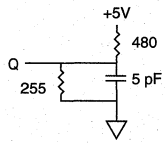


Fig. 2 OUTPUT LOAD EQUIVALENT

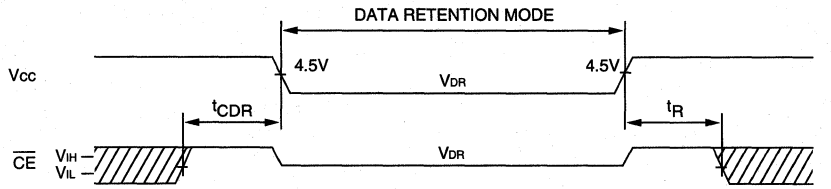
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

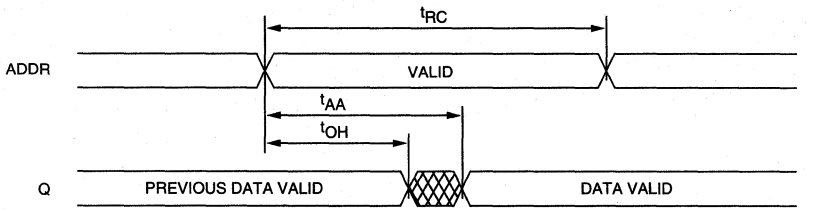
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current L version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		125	300	µA	14
		Vcc = 3V	I_{CCDR}		175	500	µA	14
Data Retention Current LP version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	I_{CCDR}		100	300	µA	14
		Vcc = 3V	I_{CCDR}		150	500	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

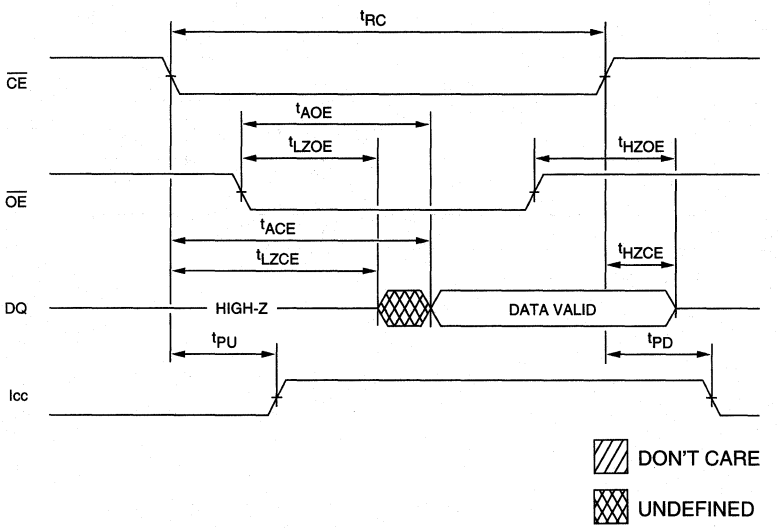
LOW Vcc DATA RETENTION WAVEFORM



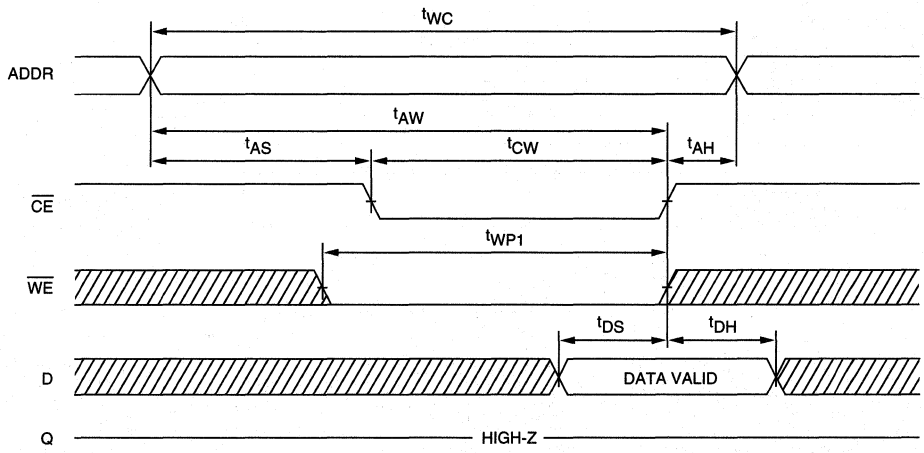
READ CYCLE NO. 1 [8, 9]



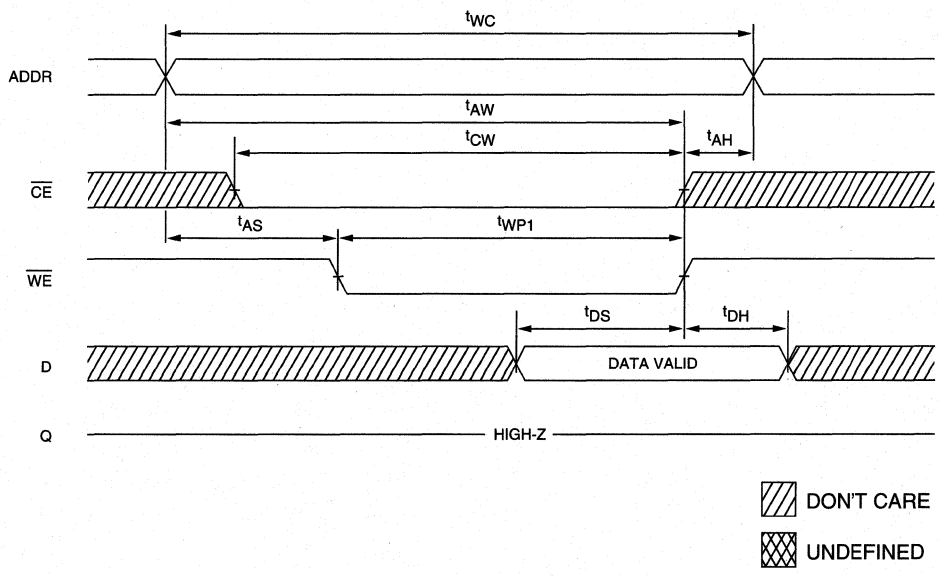
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

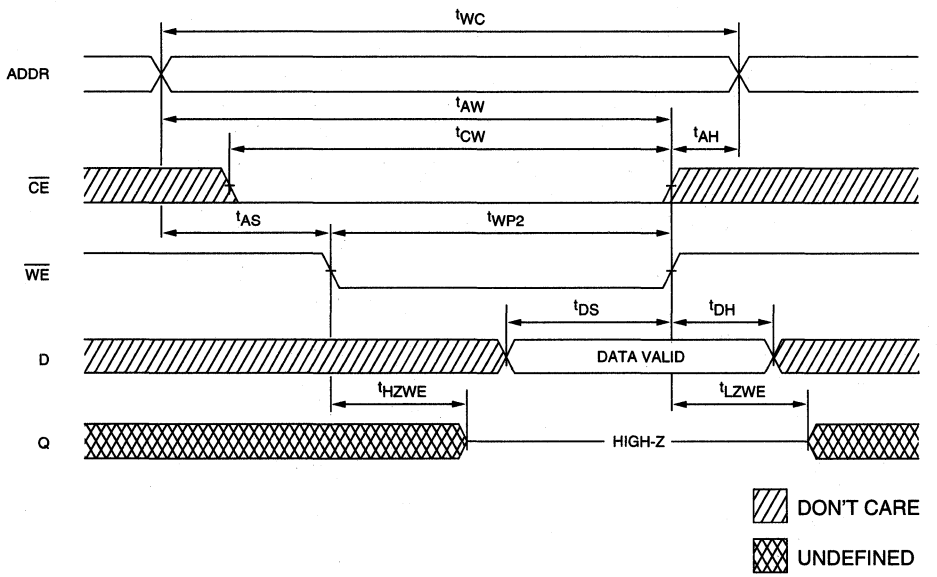


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

128K x 8 SRAM
WITH OUTPUT ENABLE

FEATURES
- High speed: 12, 15, 20 and 25
- Available in 300 mil- and 400 mil-wide SOJ packages
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6ns

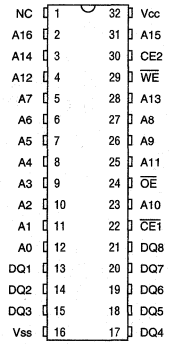
OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic DIP (400 mil) — None
  - Plastic SOJ (400 mil) — DJ
  - Plastic SOJ (300 mil) — SJ
- 2V data retention (optional) — L
- 2V data retention, low power (optional) — LP
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5C1008DJ-20 L

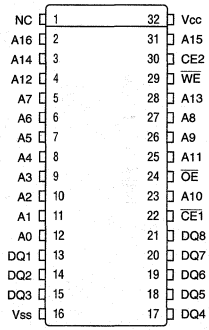
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin DIP (SA-6)



32-Pin SOJ (SD-4, SD-5)



GENERAL DESCRIPTION

The MT5C1008 is organized as a 131,072 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

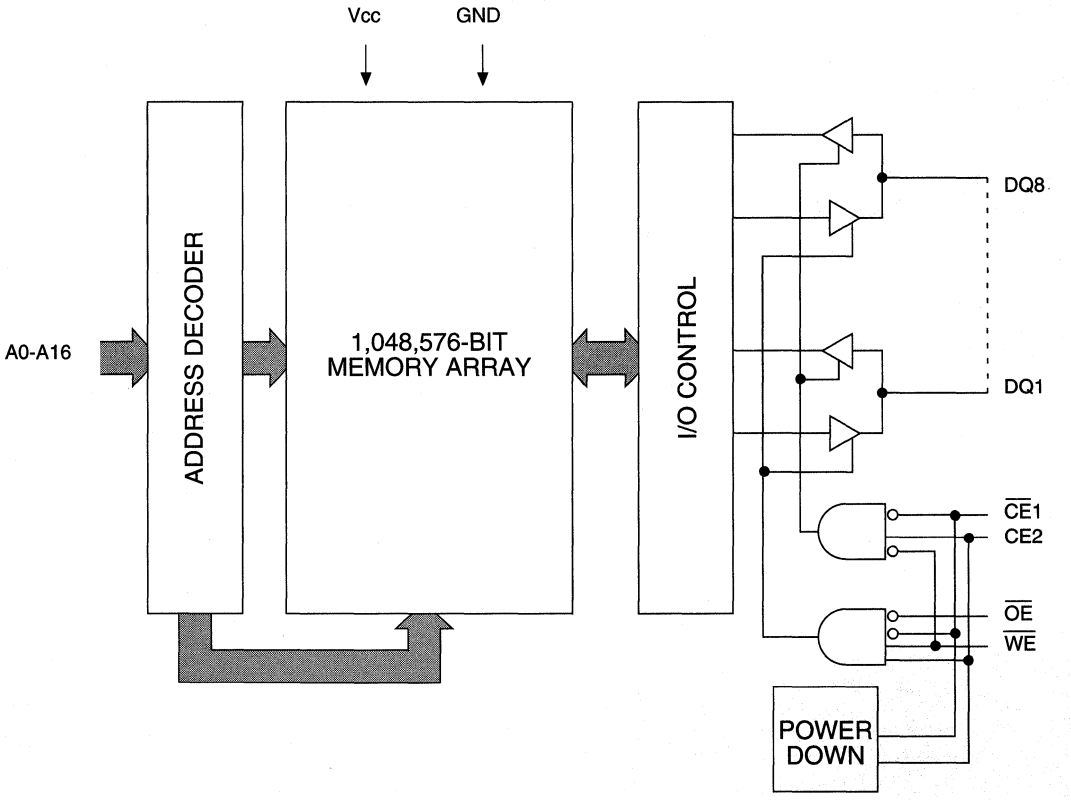
For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2) and an output enable ($\overline{OE}$). This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ and $\overline{OE}$ go LOW. The device offers reduced power standby modes when disabled. This allows system designers to meet low standby power requirements.

The "L" and "LP" versions each provide a 70% reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90% reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$CE2 \ge V_{IH}$; $\overline{CE1} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	107	195	170	145	130	mA	3, 14
Power Supply Current: Standby	$CE2 \le V_{IH}$ or $\overline{CE1} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	37	75	65	50	45	mA	14
	LP version only	I_{SB1}	1.3	3	3	3	3	mA	14
	$CE2 \le V_{SS}$ +0.2V; $\overline{CE1} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	14
	L and LP versions only	I_{SB2}	0.3	1.5	1.5	1.5	1.5	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 5V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYM	-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		10	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		5		6		6		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4		5		6		10	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	8		10		12		15		ns	
Address valid to end of write	^tAW	8		10		12		15		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		9		12		15		ns	
WRITE pulse width	$^tWP2$	10		12		15		15		ns	
Data setup time	^tDS	6		7		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		10	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C1008 SRAMs.
(-40°C ≤ T_A ≤ 85°C)

				MAX					
DESCRIPTION	**CONDITIONS**	**SYMBOL**	**TYP**	**-20**	**-25**	**-35**	**-45**	**UNITS**	**NOTES**
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	107	155	140	130	125	mA	3, 14
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	37	50	45	40	40	mA	14
LP version only	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	1.3	6	6	6	6	mA	14
	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.4	5	5	5	5	mA	14
L version and LP version	CE2 ≤ V_{SS} +0.2V; $\overline{CE1}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.3	2	2	2	2	mA	14

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	**CONDITIONS**		**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**NOTES**
Data Retention Current	$\overline{CE1}$ ≥ (V_{CC} -0.2V) or CE2 ≤ (V_{SS} +0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		35	170	µA	15
		V_{CC} = 3V	I_{CCDR}		60	325	µA	15

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 85°C; V_{CC} = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
WRITE Cycle											
Address hold from end of write	^tAH	1		1		1		1		ns	

AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C1008 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	CE2 ≥ V_{IH}; $\overline{CE1}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	Icc	107	155	140	130	125	mA	3, 13
Power Supply Current: Standby	CE2 ≤ V_{IH} or $\overline{CE1}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	37	60	55	50	47	mA	13
	CE2 ≤ Vss +0.2V; $\overline{CE1}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	0.4	7	7	7	7	mA	13
L version only	CE2 ≤ Vss +0.2V; $\overline{CE1}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	0.3	5	5	5	5	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Data Retention Current	$\overline{CE1}$ ≥ (Vcc -0.2V) or CE2 ≤ (Vss +0.2V) V_{IN} ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		35	1,000	µA	15
		Vcc = 3V	I_{CCDR}		60	1,500	µA	15

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ T_A ≤ 125°C - AT; -55°C ≤ T_A ≤ 125°C - XT; Vcc = 5V ±10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	7
WRITE Cycle											
Address hold from end of write	^tAH	1		1		1		1		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

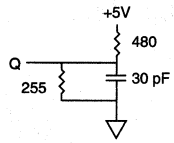


Fig. 1 OUTPUT LOAD EQUIVALENT

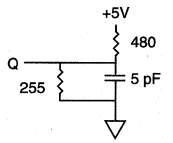


Fig. 2 OUTPUT LOAD EQUIVALENT

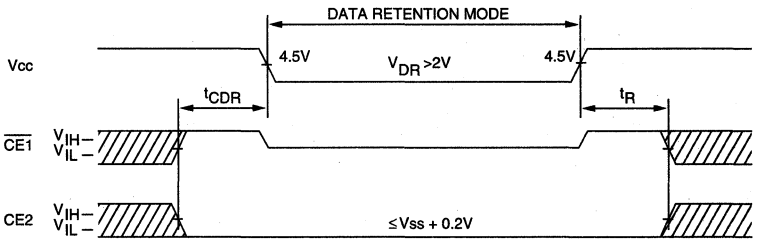
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 timing is the same as $\overline{CE1}$ timing. The waveform is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.
15. Typical currents are measured at 25°C.

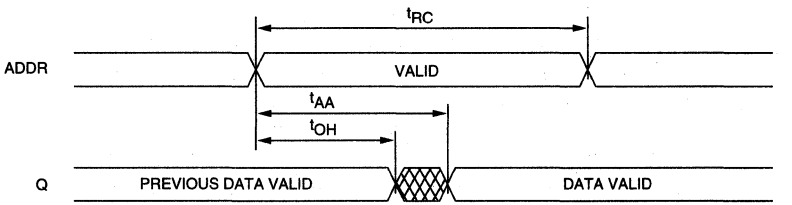
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE1}$ ≥ (Vcc -0.2V) or CE2 ≤ (Vss +0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		35	150	µA	15
		Vcc = 3V	ICCDR		60	250	µA	15
Data Retention Current LP version	$\overline{CE1}$ ≥ (Vcc -0.2V) or CE2 ≤ (Vss +0.2V)	Vcc = 2V	ICCDR		35	150	µA	15
		Vcc = 3V	ICCDR		60	250	µA	15
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4, 11

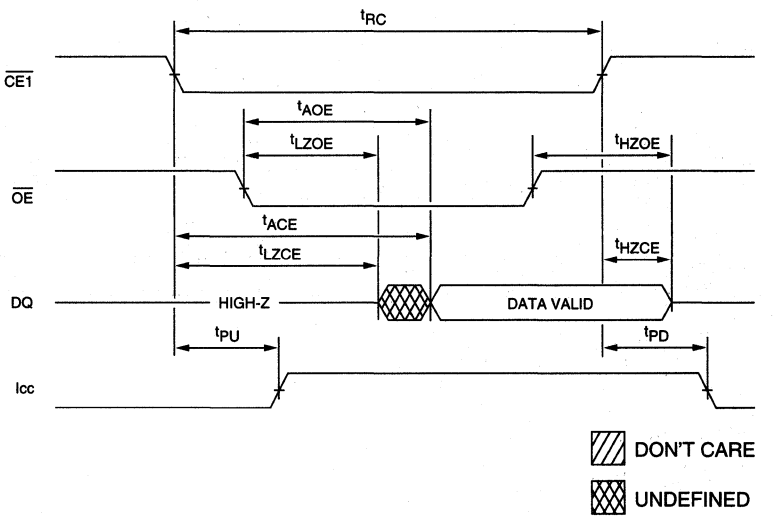
LOW Vcc DATA RETENTION WAVEFORM



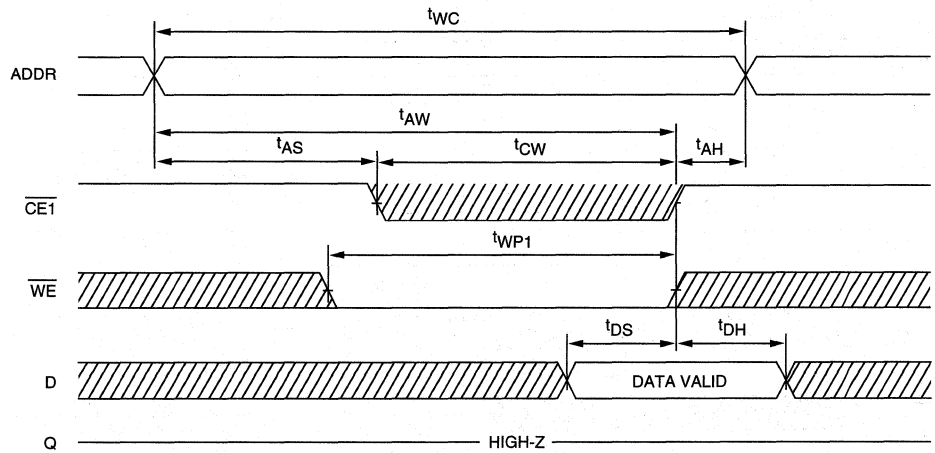
READ CYCLE NO. 1 [8, 9]



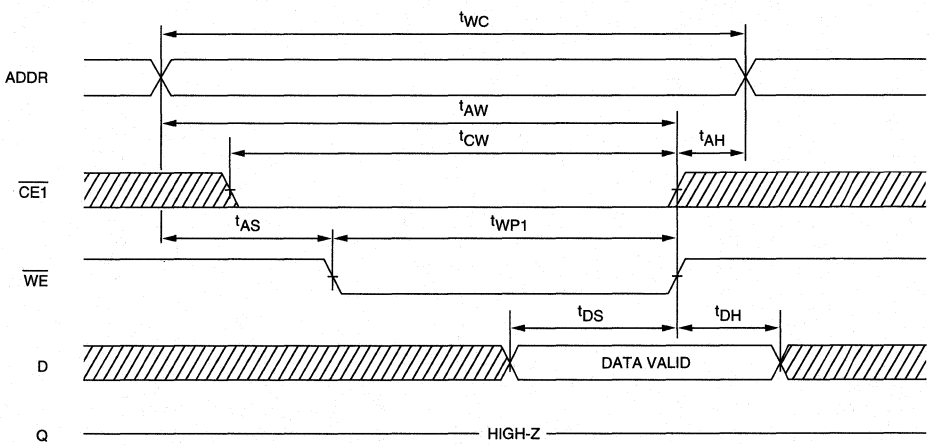
READ CYCLE NO. 2 [7, 8, 10, 12]

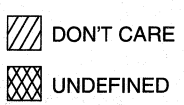


WRITE CYCLE NO. 1 [12, 13]
(Chip Enable Controlled)



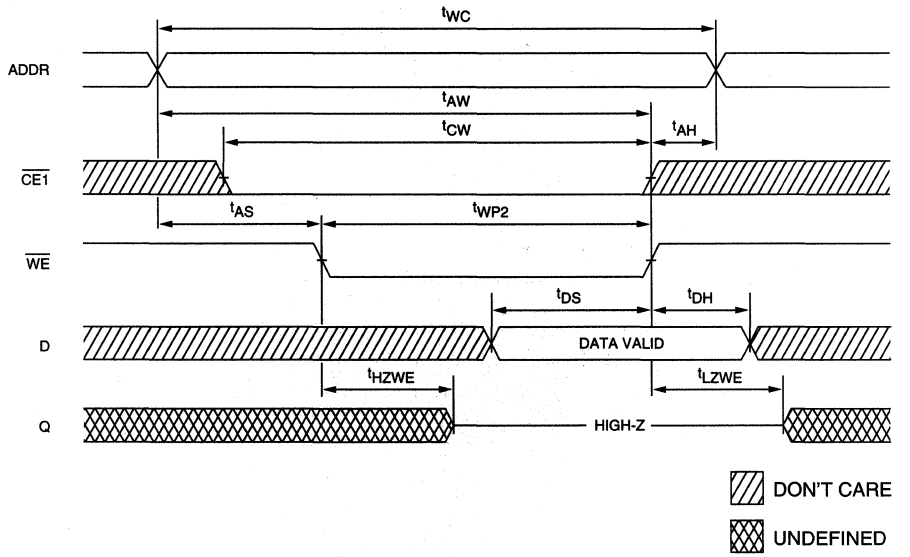
WRITE CYCLE NO. 2 [12, 13]
(Write Enable Controlled)





NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

128K x 8 SRAM

WITH SINGLE CHIP ENABLE, REVOLUTIONARY PINOUT

FEATURES

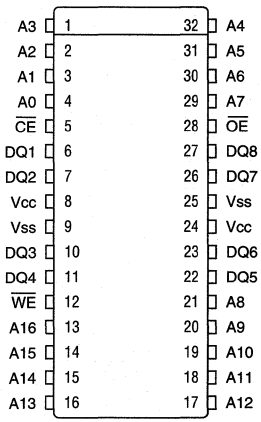
- High speed: 12, 15, 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL-compatible
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Fast $\overline{OE}$ access times: 6, 8, 10 and 12ns

OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- 2V data retention (optional) — L
- Temperature
  - Commercial (0°C to +70°C) — None
- Packages
  - 32-pin SOJ (400 mil) — DJ
- Part Number Example: MT5C128K8A1DJ-25 L

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

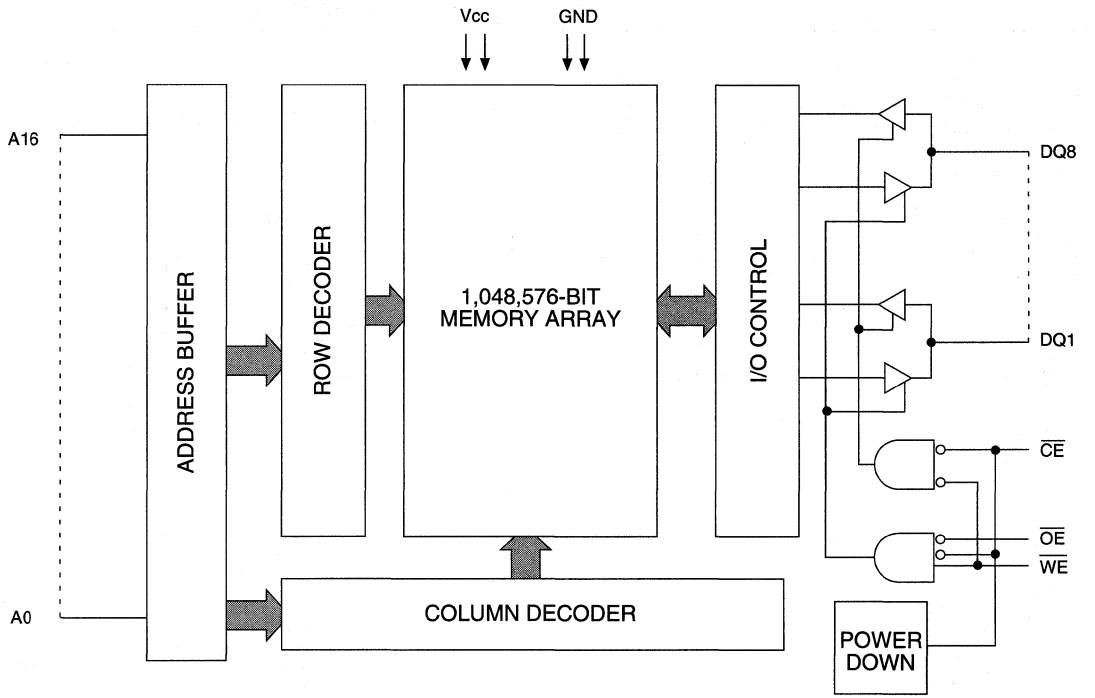
The MT5C128K8A1 is organized as a 131,072 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
4, 3, 2, 1, 32, 31, 30, 29, 21, 20, 19, 18, 17, 16, 15, 14, 13	A0-A16	Input	Address Inputs: These inputs determine which cell is addressed.
12	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
5	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
28	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
6, 7, 10, 11, 22, 23, 26, 27	DQ1-DQ8	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	Vcc	Supply	Power Supply: 5V ±10%
9, 25	Vss	Supply	Ground: GND

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to Vcc +1V
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	200	330	280	230	200	mA	3, 14
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	45	80	70	60	50	mA	14
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.75	5	5	5	7	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 5V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 15) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	9		10		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	9		10		12		14		ns	
WRITE pulse width	$^tWP2$	9		10		12		14		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

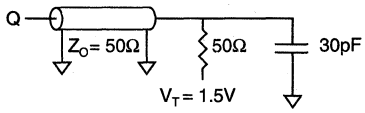


Fig. 1 OUTPUT LOAD EQUIVALENT

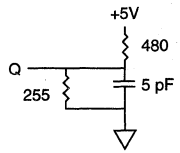


Fig. 2 OUTPUT LOAD EQUIVALENT

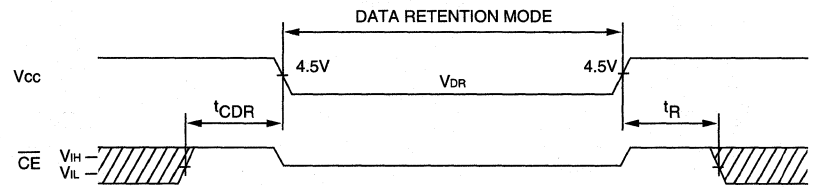
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^tRC/2$.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded and $f = \frac{1}{^tRC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tHZCE, ^tHZOE and ^tHZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE, and ^tHZWE is less than ^tLZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^tRC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical currents are measured at 25°C.
14. Typical values are measured at 25°C, 5V and 15ns cycle time.
15. Contact Micron for extended temperature (IT/AT/XT) timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.

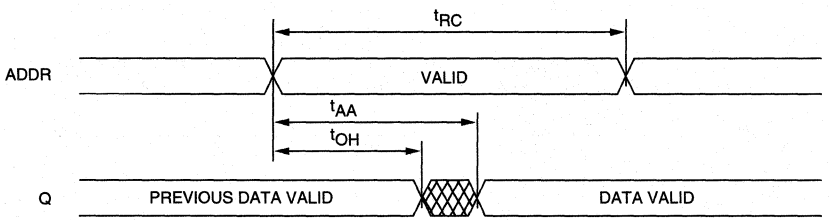
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq$ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		70	300	µA	13
		Vcc = 3V	I_{CCDR}		175	500	µA	13
Chip Deselect to Data Retention Time			^tCDR	0			ns	4
Operation Recovery Time			^tR	^tRC			ns	4, 11

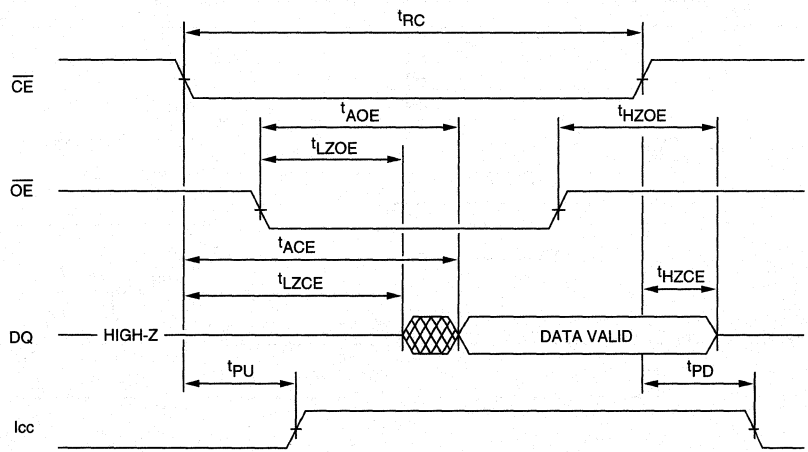
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



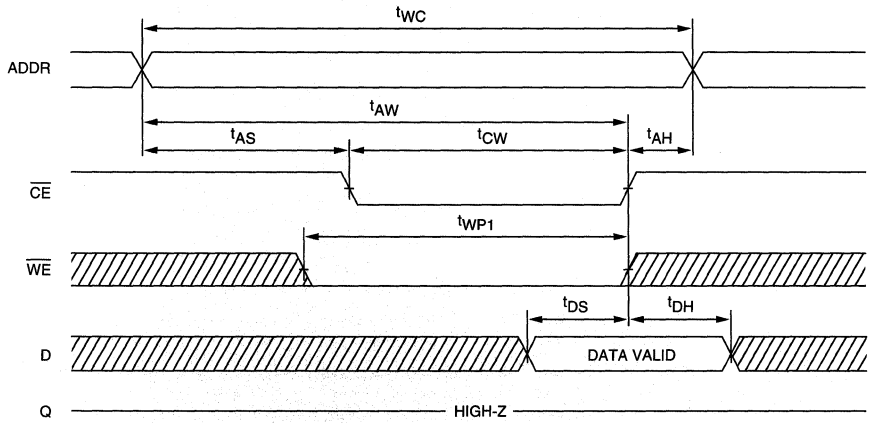
READ CYCLE NO. 2 [7, 8, 10]



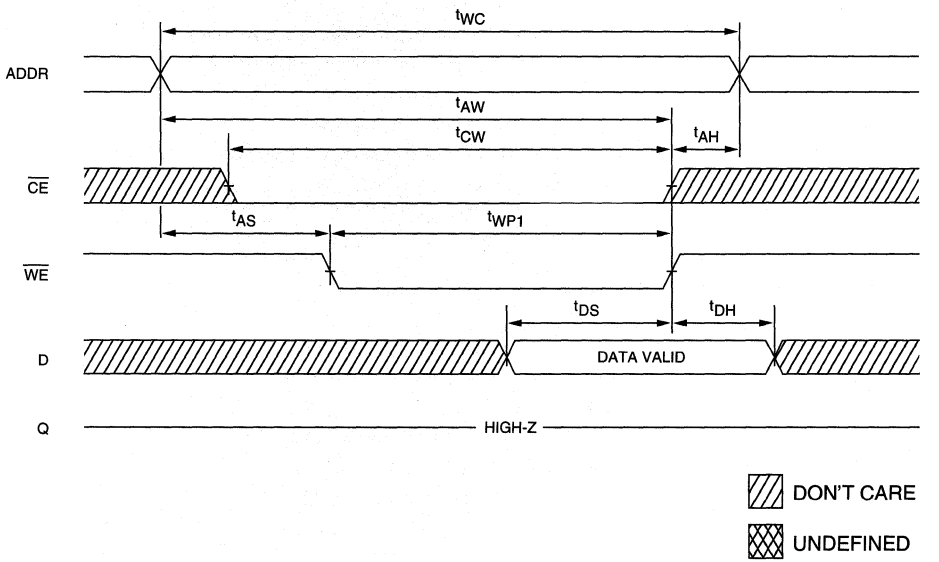
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

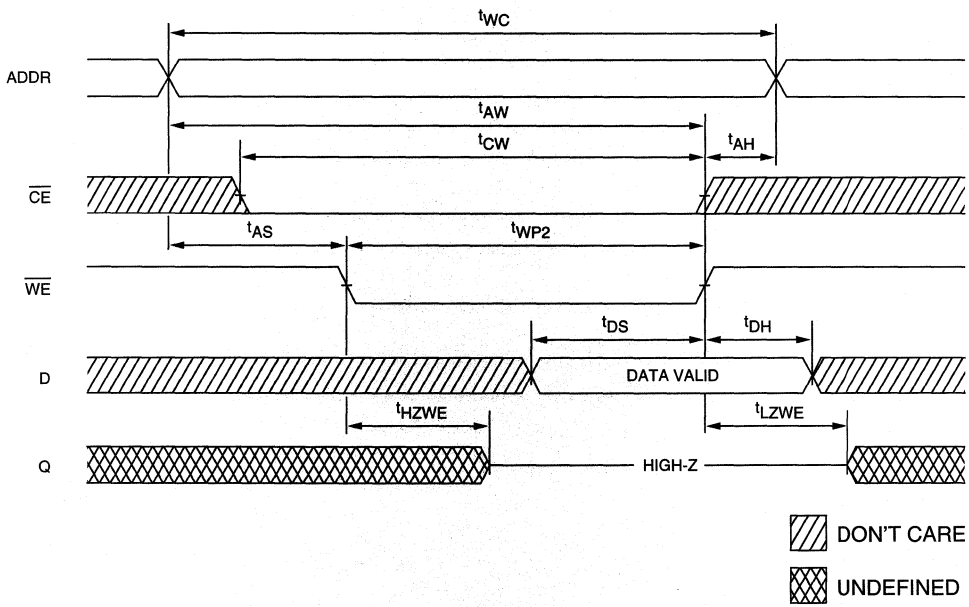


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

64K x 16 SRAM

REVOLUTIONARY PINOUT WITH OUTPUT ENABLE AND BYTE WRITES

FEATURES

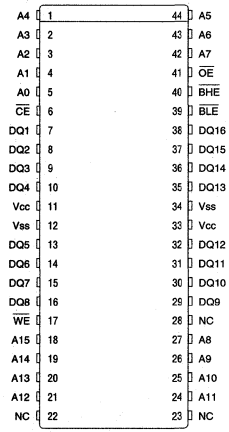
- Fast access times: 12, 15, 20 and 25ns
- Fast output enable access time: 6, 8, 10 and 12ns
- Multiple center power and ground pins for improved noise immunity
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Individual byte controls for both READ and WRITE cycles
- All inputs and outputs are TTL-compatible

OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 44-pin SOJ (400 mil) — DJ
- 2V data retention (optional) — L
- Temperature
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT5C64K16A1DJ-15 L

PIN ASSIGNMENT (Top View)

44-Pin SOJ
(SD-7)



GENERAL DESCRIPTION

The MT5C64K16A1 is organized as a 65,536 x 16 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

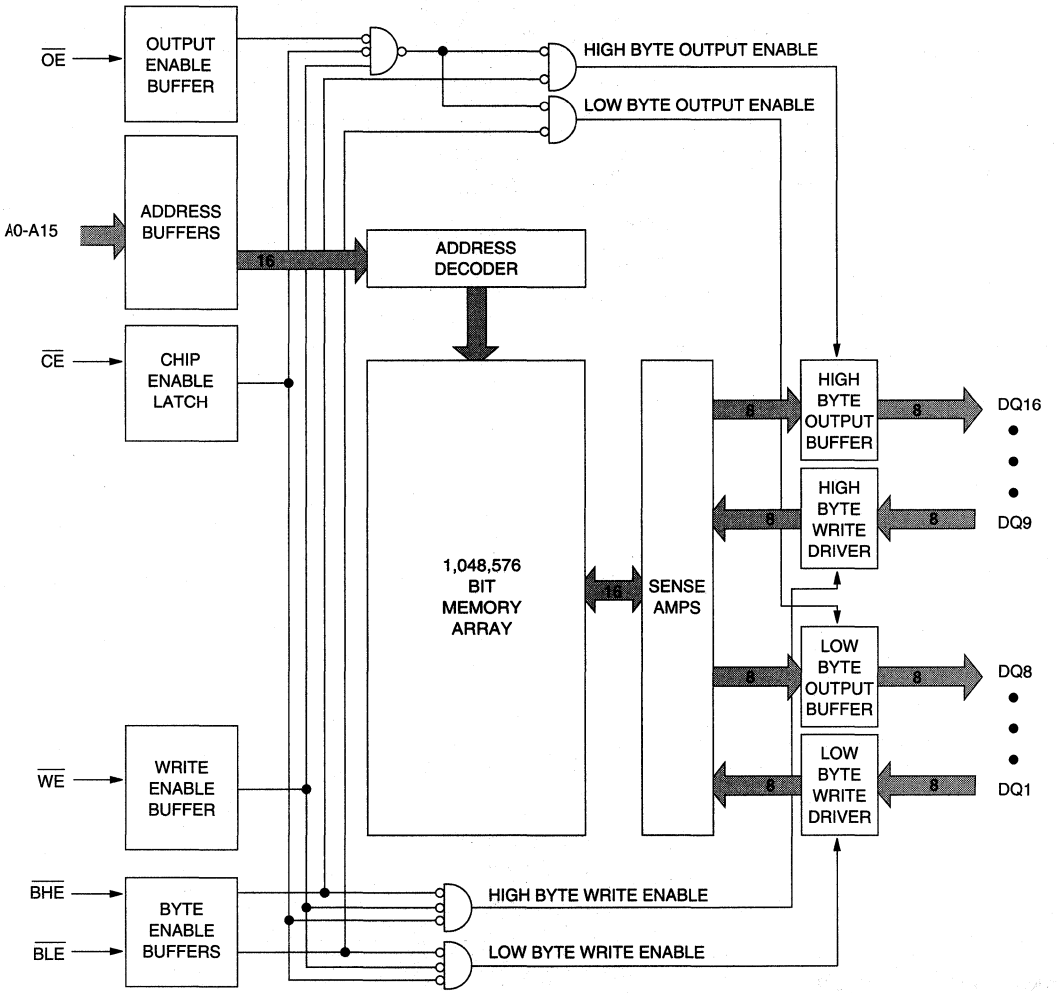
This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capabilities. This enhancement can place the output pin in High-Z for additional flexibility in system design.

The MT5C64K16A1 SRAM integrates a 64K x 16 SRAM core with peripheral circuitry consisting of active LOW chip enable, separate upper and lower byte enables and a fast output enable.

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be written and read. $\overline{BLE}$ controls DQ1-DQ8, the lower bits. $\overline{BHE}$ controls DQ9-DQ16, the upper bits.

The MT5C64K16A1 operates from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ and TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 1, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19, 18	A0-A15	Input	Address Inputs: These inputs determine which cell is accessed.
17	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or a WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
39, 40	$\overline{BLE}$, $\overline{BHE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written or read to the lower byte, DQ1-DQ8. When $\overline{BHE}$ is LOW, data is written or read to the upper byte, DQ9-DQ16.
6	$\overline{CE}$	Input	Chip Enable: This signal is used to enable the device. When $\overline{CE}$ is HIGH, the chip automatically goes into standby power mode.
41	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
22, 23, 28	NC	-	No Connect: These signals are not internally connected.
7, 8, 9, 10, 13, 14, 15, 16, 29, 30, 31, 32, 35, 36, 37, 38	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16.
11, 33	Vcc	Supply	Power Supply: +5V ±10%
12, 34	Vss	Supply	Ground: GND

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	DQ1-DQ8	DQ9-DQ16	POWER
STANDBY	H	X	X	X	X	HIGH-Z	HIGH-Z	STANDBY
LOW BYTE READ (DQ1-DQ8)	L	L	H	L	H	D	HIGH-Z	ACTIVE
HIGH BYTE READ (DQ9-DQ16)	L	L	H	H	L	HIGH-Z	D	ACTIVE
WORD READ (DQ1-DQ16)	L	L	H	L	L	D	D	ACTIVE
WORD WRITE (DQ1-DQ16)	L	X	L	L	L	Q	Q	ACTIVE
LOW BYTE WRITE (DQ1-DQ8)	L	X	L	L	H	Q	HIGH-Z	ACTIVE
HIGH BYTE WRITE (DQ9-DQ16)	L	X	L	H	L	HIGH-Z	Q	ACTIVE
OUTPUT DISABLE	L	H	H	X	X	HIGH-Z	HIGH-Z	ACTIVE
	L	X	X	H	H	HIGH-Z	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1V to 7V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Voltage at Any Pin Relative toV_{SS} ..... -1V to V_{CC}+1V
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX outputs open f = MAX = 1/ ^tRC	I_{CC}	200	330	280	230	200	mA	3, 15
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX outputs open f = MAX = 1/ ^tRC	I_{SB1}	45	70	60	50	40	mA	15
	$\overline{CE} \ge V_{CC}$ - 0.2V V_{CC} = MAX; $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.75	5	5	5	7	mA	15

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I		5	pF	4
Input/Output Capacitance (D/Q)	Vcc = 5V	$C_{I/O}$		5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 16) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	4		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	6, 7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6, 7
Byte Enable access time	^tABE		6		8		10		12	ns	
Byte Enable to output in Low-Z	^tLZBE	0		0		0		0		ns	6, 7
Byte disable to output in High-Z	^tHZBE		6		6		8		8	ns	6, 7
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	9		10		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
Write pulse width	^tWP	9		10		12		14		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	6, 7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7
Byte Enable to end of write	^tBW	9		10		12		14		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

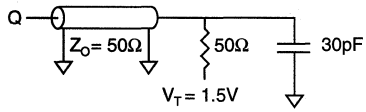


Fig. 1 OUTPUT LOAD EQUIVALENT

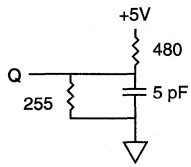


Fig. 2 OUTPUT LOAD EQUIVALENT

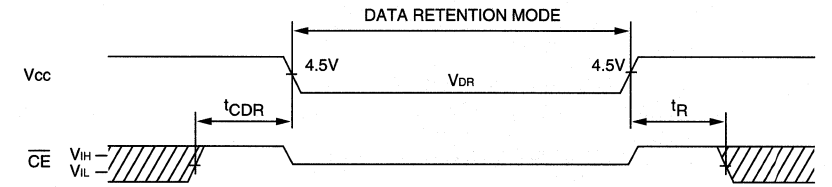
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^tRC/2$.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded and $f = \frac{1}{^tRC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE, ^tHZOE is less than ^tLZOE, and ^tHZBE is less than ^tLZBE.
8. Any combination of write enable, chip enable and byte enable can initiate and terminate a WRITE cycle.
9. $\overline{WE}$ is HIGH for READ cycle.
10. Device is continuously selected. Chip enable is held in its active state.
11. Address valid prior to, or coincident with, the latest occurring chip enable.
12. $\overline{BHE}$ and $\overline{BLE}$ are held in their active state (LOW).
13. The output will be in the High-Z state if output enable is HIGH.
14. Typical currents are measured at 25°C.
15. Typical values are measured at 25°C, 5V and 15ns cycle time.
16. Contact Micron for extended temperature (IT/AT/XT) timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.

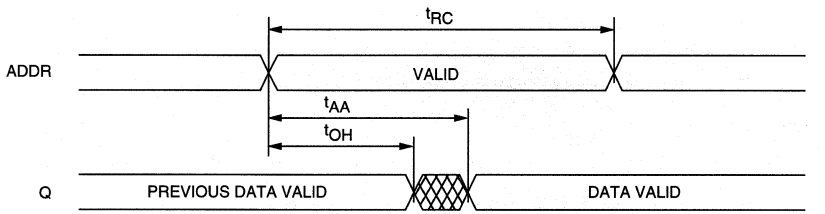
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		70	300	µA	14
		Vcc = 3V	I_{CCDR}		175	500	µA	14
Chip Deselect to Data Retention Time			^tCDR	0			ns	4
Operation Recovery Time			^tR	^tRC			ns	4, 11

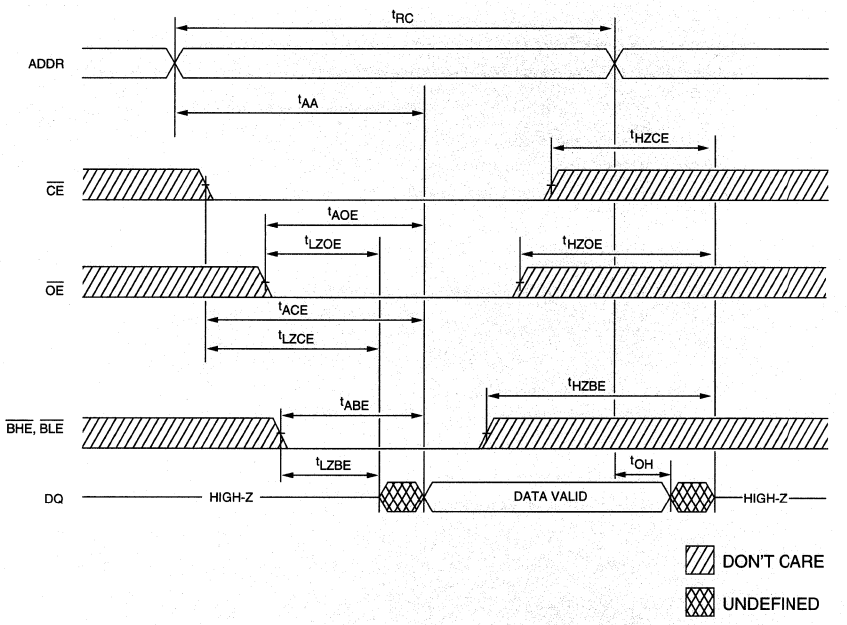
LOW Vcc DATA RETENTION WAVEFORM



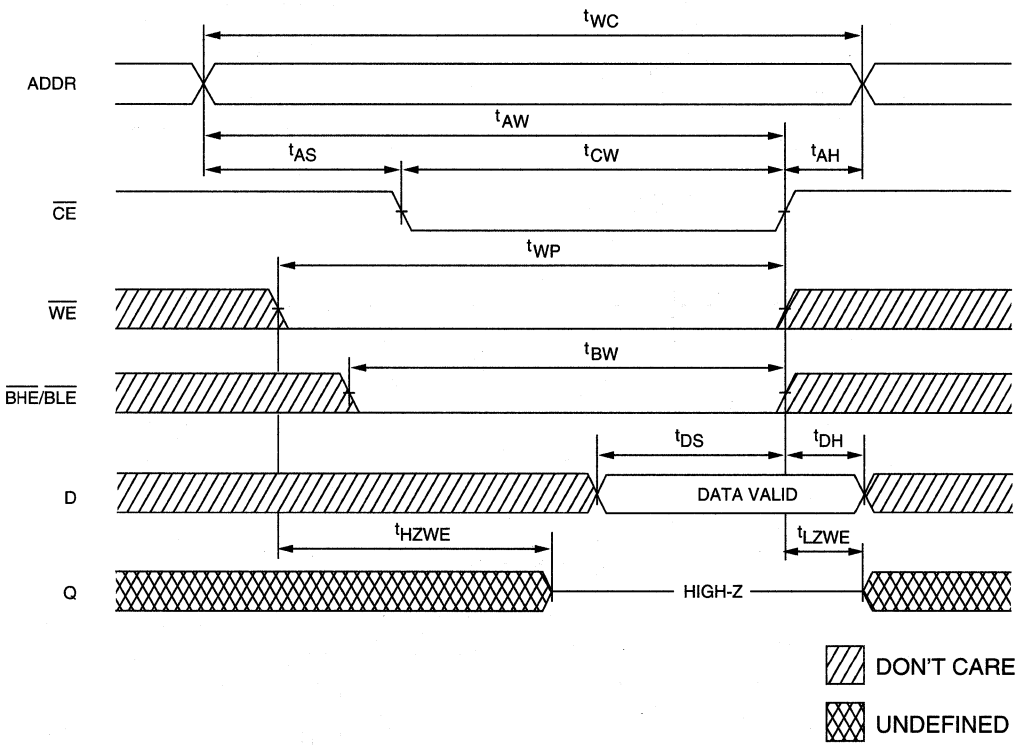
READ CYCLE NO. 1 [9, 10, 12]



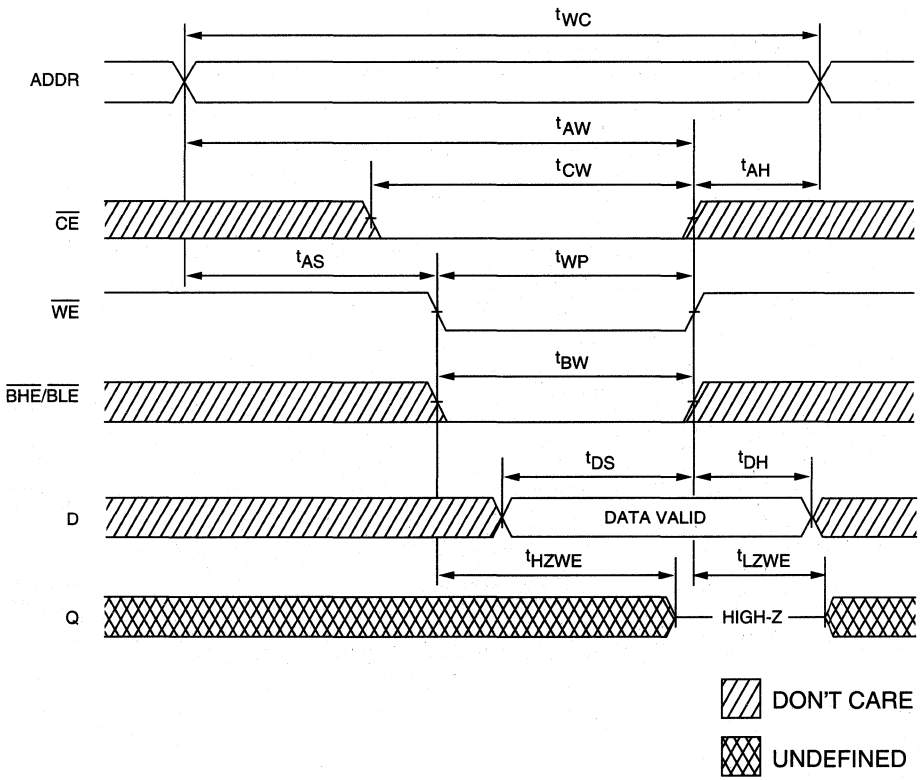
READ CYCLE NO. 2 [7, 9]



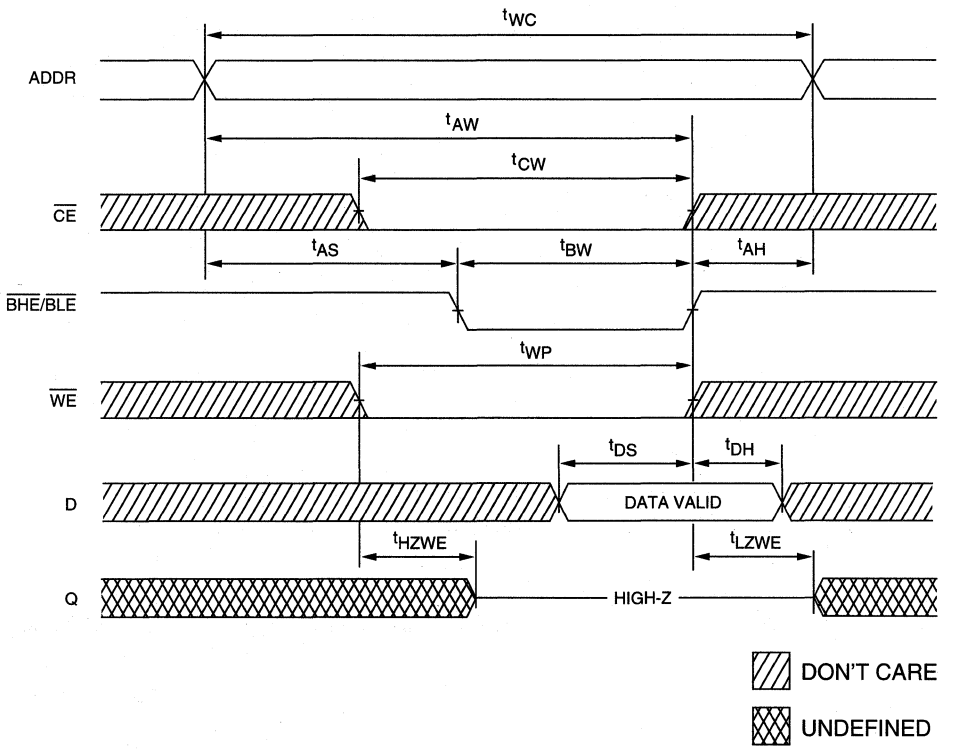
WRITE CYCLE NO. 1 [8, 13]
Chip Enable Controlled



WRITE CYCLE NO. 2 [8, 13]
Write Enable Controlled



WRITE CYCLE NO. 3 [8, 13]
Byte Enable Controlled



MICRON
SEMICONDUCTOR, INC.

3.3V ASYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package/No. of Pins		Page
				PDIP	SOJ	
256K x 1	$\overline{CE}$ only with separate I/O	MT5LC2561	12, 15, 20, 25	24	24	2-1
1 Meg x 1	$\overline{CE}$ only with separate I/O	MT5LC1001	15, 17, 20, 25	28	28	2-9
64K x 4	$\overline{CE}$ only	MT5LC2564	12, 15, 20, 25	24	24	2-17
64K x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC2565	12, 15, 20, 25	28	28	2-25
256K x 4	$\overline{CE}$ and $\overline{OE}$	MT5LC1005	15, 17, 20, 25	28	28	2-33
256K x 4	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC256K4D4	12, 15, 20, 25	-	32	2-41
1 Meg x 4	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC1M4D4	12, 15, 20, 25, 35	-	32	2-51
32K x 8	$\overline{CE}$ and $\overline{OE}$	MT5LC2568	12, 15, 20, 25	28	28	2-59
128K x 8	$\overline{CE1}$, CE2 and $\overline{OE}$	MT5LC1008	15, 17, 20, 25	32	32	2-67
128K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC128K8D4	12, 15, 20, 25	-	32	2-75
512K x 8	$\overline{CE}$, $\overline{OE}$ and Revolutionary Pinout	MT5LC512K8D4	12, 15, 20, 25, 35	-	36	2-85
64K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable and Revolutionary Pinout	MT5LC64K16D4	12, 15, 20, 25	-	44	2-93
256K x 16	$\overline{CE}$, $\overline{OE}$, Byte Enable	MT5LC256K16D4	12, 15, 20, 25, 35	-	54	2-103

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

SRAM

256K x 1 SRAM

LOW VOLTAGE

FEATURES

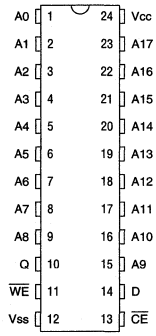
- All I/O pins are 5V tolerant
- High speed: 12, 15, 20 and 25
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible
- Complies to JEDEC low-voltage TTL voltage standards

OPTIONS / MARKING

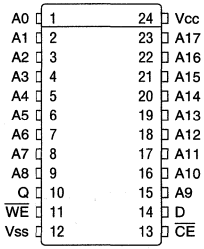
- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
- 2V data retention (optional) — L
- Temperature
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT5LC2561DJ-15 L

PIN ASSIGNMENT (Top View)

24-Pin DIP (SA-3)



24-Pin SOJ (SD-1)



GENERAL DESCRIPTION

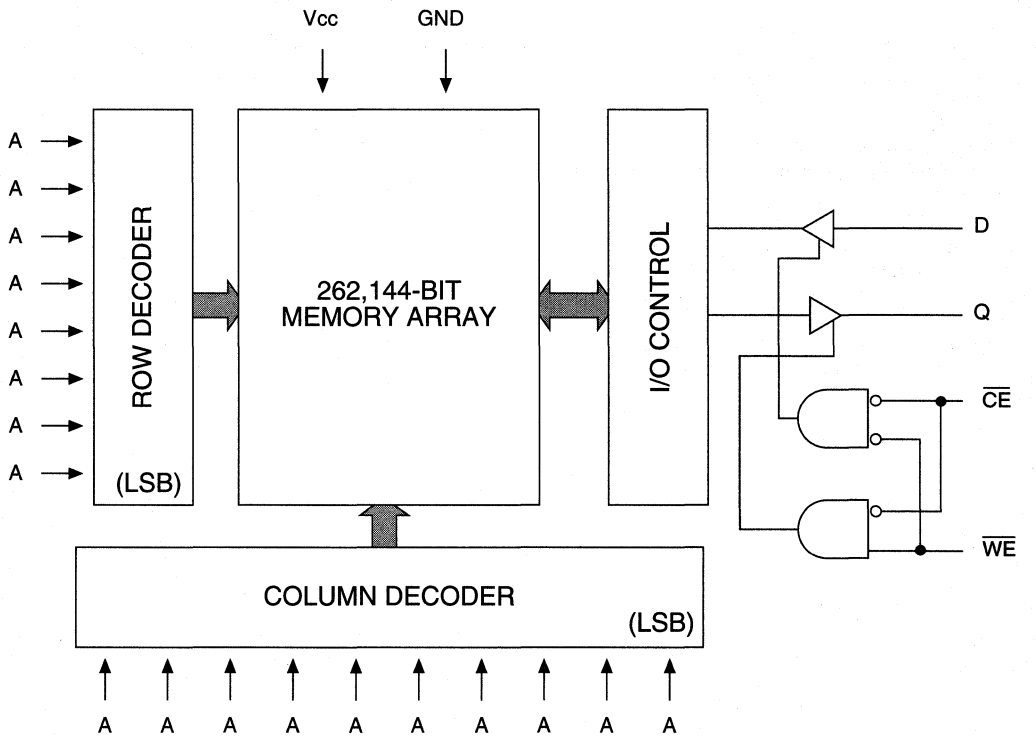
The MT5LC2561 is organized as a 262,144 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'T CARE	HIGH-Z	STANDBY
READ	L	H	DON'T CARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage	15, 20 and 25ns	V_{CC}	3.0	3.6	V	1
Supply Voltage	12ns	V_{CC}	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYM	TYP	-12**	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX outputs open f = MAX = 1/^tRC	I_{CC}	75	125	110	95	90	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX outputs open f = MAX = 1/^tRC	I_{SB1}	17	35	30	25	25	mA	13
	$\overline{CE}$ ≥ V_{CC} - 0.2V; V_{CC} = MAX V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	1.0	3	3	3	3	mA	13

**The P version of this part is not available at 12ns.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13, 15) ($0°C \leq T_A \leq 70°C$)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	7
Chip disable to output in High-Z	^tHZCE		6		8		9		9	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	4
Chip disable to power-down time	^tPD		12		15		20		25	ns	4
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	8		10		12		15		ns	
Address valid to end of write	^tAW	8		10		12		15		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		ns	
WRITE pulse width	^tWP	8		10		12		15		ns	
Data setup time	^tDS	7		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

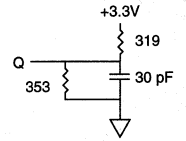


Fig. 1 OUTPUT LOAD EQUIVALENT

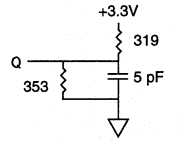


Fig. 2 OUTPUT LOAD EQUIVALENT

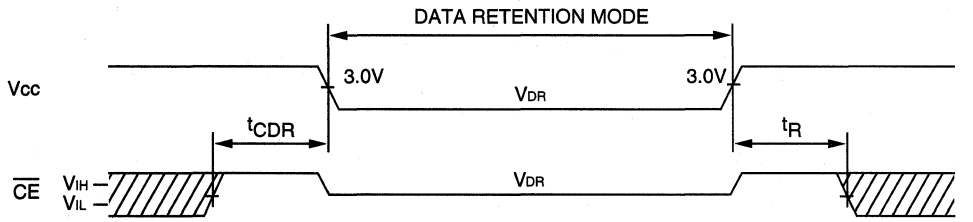
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.
15. V_{CC} is 3.3V ±0.3V for the 15, 20 and 25ns speed grades and 3.3V ±0.2V for the 12ns speed grade.

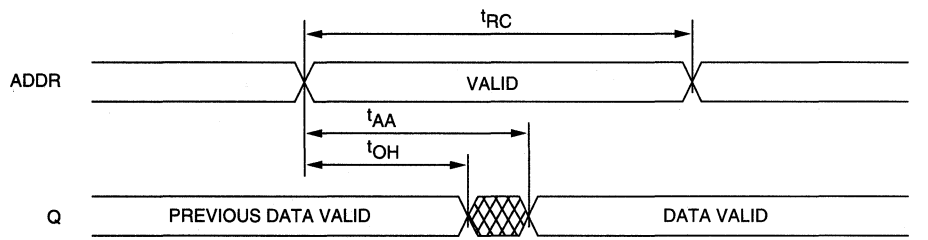
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq V_{CC}$ -0.2V Other Inputs: $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq V_{SS}$+0.2V V_{CC} = 2V	I_{CCDR}		310	500	µA	14
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

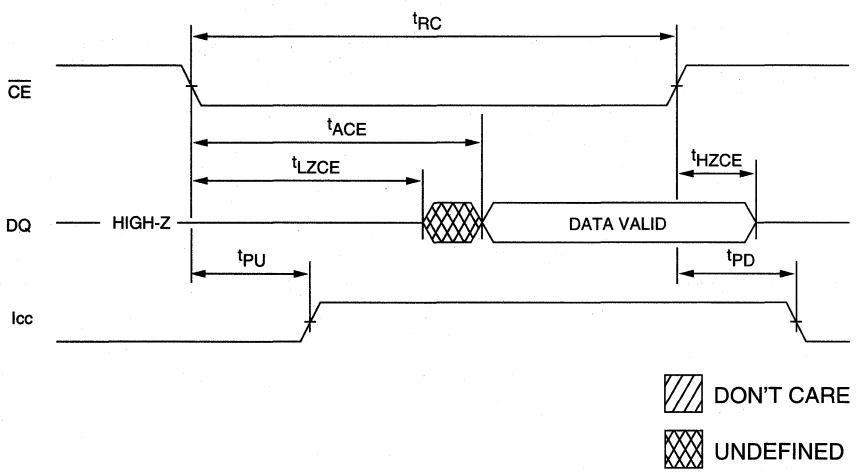
LOW Vcc DATA RETENTION WAVEFORM



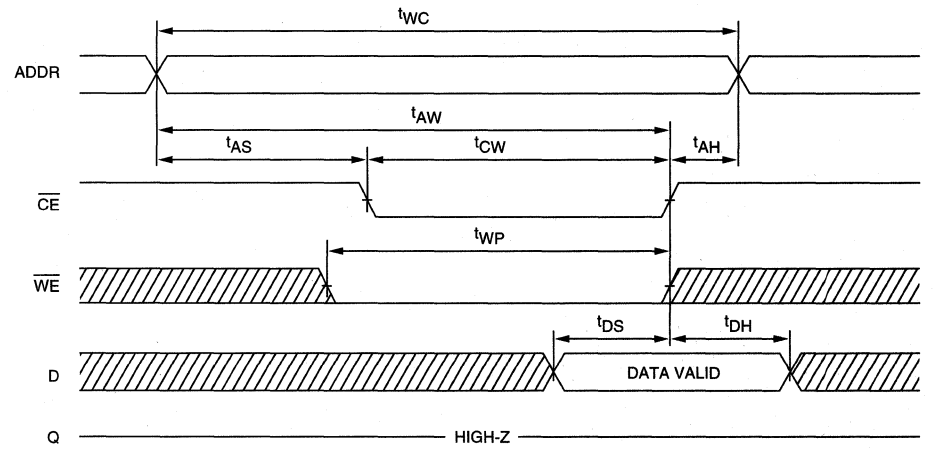
READ CYCLE NO. 1 [8, 9]



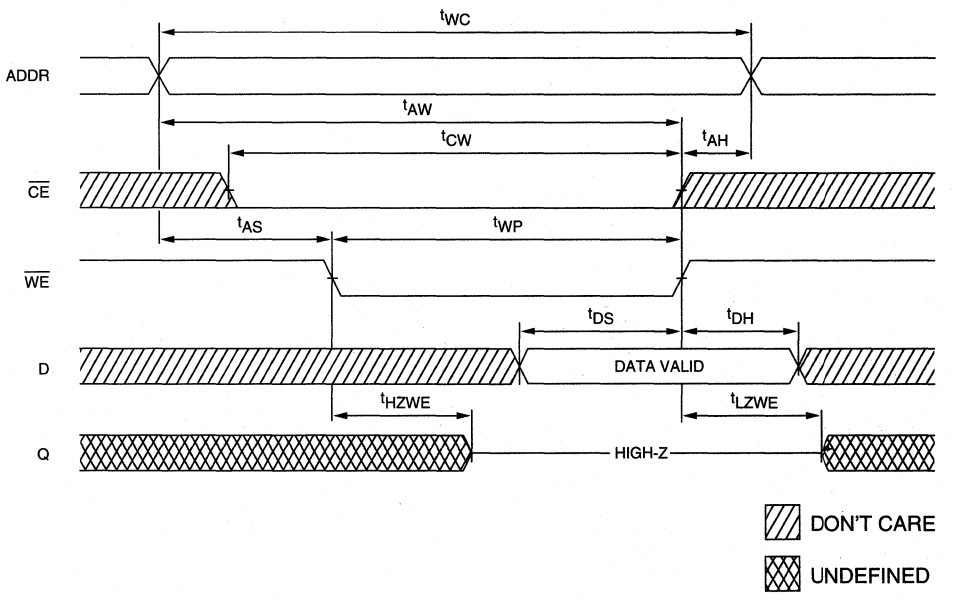
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

1 MEG x 1 SRAM

LOW VOLTAGE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 15, 17, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3 power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible
- Complies to JEDEC low-voltage TTL standards

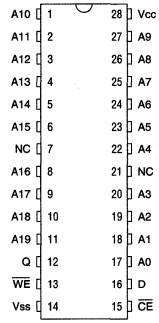
OPTIONS — MARKING

- Timing
  - 15ns access — -15
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic DIP (400 mil) — None
  - Plastic SOJ (400 mil) — DJ
- 2V data retention (optional) — L
- 2V data retention, low power (optional) — LP
- Temperature
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT5LC1001DJ-20 L

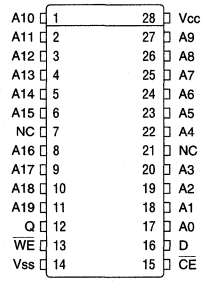
NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-5)



28-Pin SOJ (SD-3)



GENERAL DESCRIPTION

The MT5LC1001 is organized as a 1,048,576 x 1 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

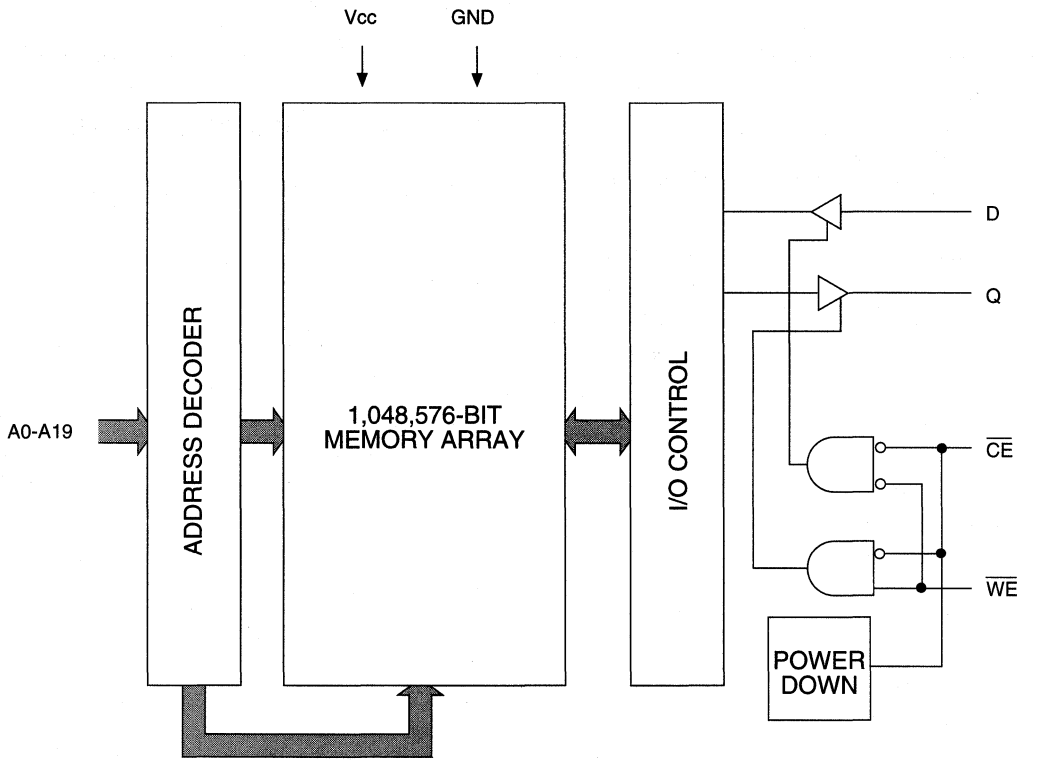
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both CMOS standby current (I_{SB2}) and TTL standby current (I_{SB1}) over the standard part. This is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	INPUT	OUTPUT	POWER
STANDBY	H	X	DON'T CARE	HIGH-Z	STANDBY
READ	L	H	DON'T CARE	Q	ACTIVE
WRITE	L	L	DATA-IN	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

					MAX					
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-15	-17	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX outputs open f = MAX = 1/t_{RC}	I_{CC}	ALL	70	155	145	135	125	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX outputs open f = MAX = 1/t_{RC}	I_{SB1}	STD, L	20	45	40	35	30	mA	13
			LP	1.5	3	3	3	3	mA	
	$\overline{CE}$ ≥ Vcc - 0.2V; Vcc = MAX V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD, L	1.0	3	3	3	3	mA	13
			LP	0.7	1.5	1.5	1.5	1.5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz Vcc = 3.3V	C_I	6	pF	4
Output Capacitance		C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13, 15) ($0°C \le T_A \le 70°C$)

DESCRIPTION	SYM	-15		-17		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	tRC	15		17		20		25		ns	
Address access time	tAA		15		17		20		25	ns	
Chip Enable access time	tACE		15		17		20		25	ns	
Output hold from address change	tOH	3		3		3		5		ns	
Chip Enable to output in Low-Z	tLZCE	5		5		5		5		ns	7
Chip disable to output in High-Z	tHZCE		6		7		8		10	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		ns	
Chip disable to power-down time	tPD		15		17		20		25	ns	
WRITE Cycle											
WRITE cycle time	tWC	15		17		20		25		ns	
Chip Enable to end of write	tCW	10		12		12		15		ns	
Address valid to end of write	tAW	10		12		12		15		ns	
Address setup time	tAS	0		0		0		0		ns	
Address hold from end of write	tAH	0		0		0		0		ns	
WRITE pulse width	tWP	9		12		12		15		ns	
Data setup time	tDS	7		8		8		10		ns	
Data hold time	tDH	0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		3		3		5		ns	7
Write Enable to output in High-Z	tHZWE		6		7		8		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

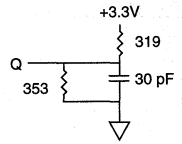


Fig. 1 OUTPUT LOAD EQUIVALENT

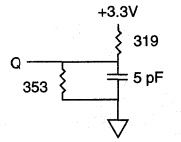


Fig. 2 OUTPUT LOAD EQUIVALENT

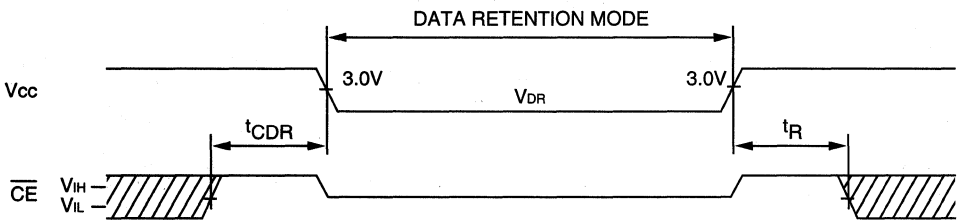
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$ and ${}^tHZWE$ are specified with $C_L = 5pF$ as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Typical currents are measured at 25°C.
15. Contact the factory for IT/AT/XT specifications.

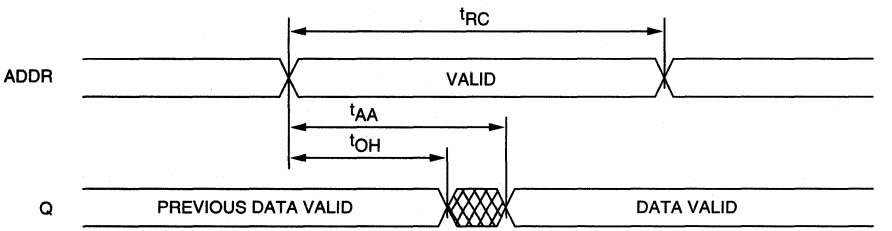
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq$ Vcc -0.2V Other inputs: $V_{IN} \geq$ Vcc -0.2V or $V_{IN} \leq$ Vss+0.2V Vcc = 2V	I_{CCDR}		145	260	µA	14
Data Retention Current LP version	$\overline{CE} \geq$ Vcc -0.2V Vcc = 2V	I_{CCDR}		145	260	µA	14
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

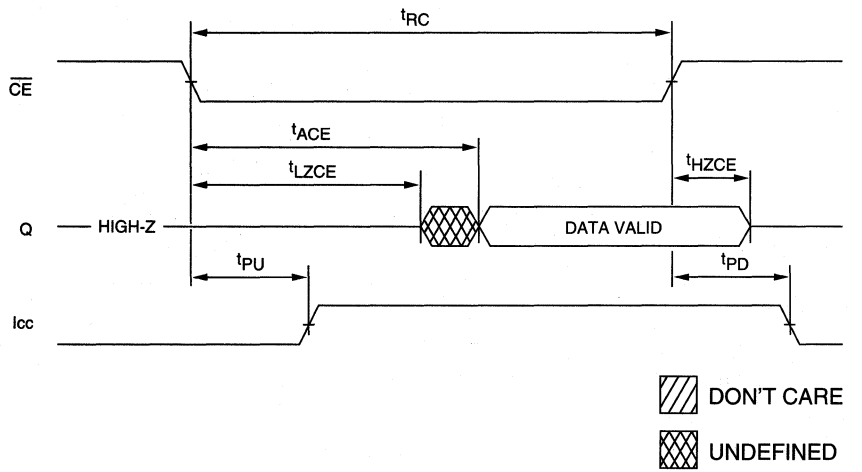
LOW Vcc DATA RETENTION WAVEFORM



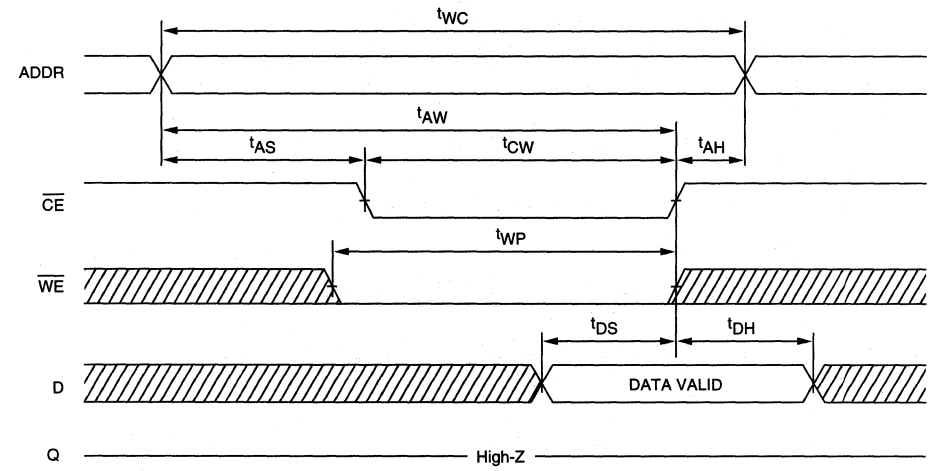
READ CYCLE NO. 1 [8, 9]



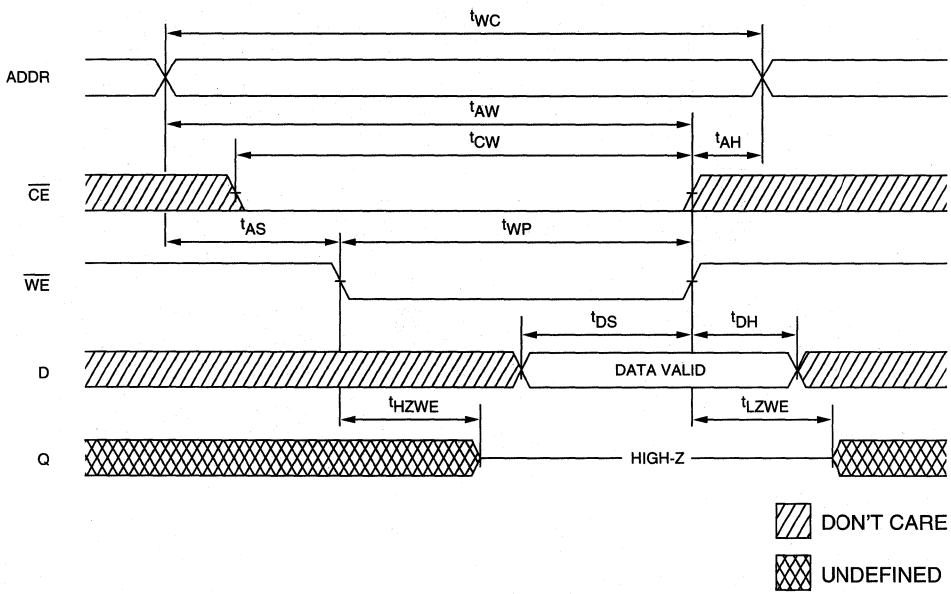
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

64K x 4 SRAM

LOW VOLTAGE

FEATURES

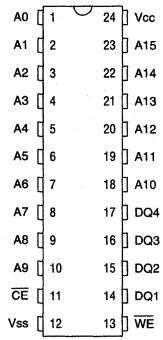
- All I/O pins are 5V tolerant
- High speed: 12, 15, 20 and 25
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible
- Complies to JEDEC low-voltage TTL standards

OPTIONS — MARKING

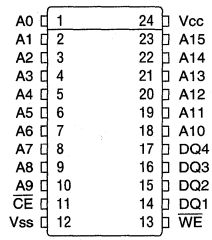
- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
- 2V data retention (optional) — L
- Temperature
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT5LC2564DJ-15 L

PIN ASSIGNMENT (Top View)

24-Pin DIP (SA-3)



24-Pin SOJ (SD-1)



GENERAL DESCRIPTION

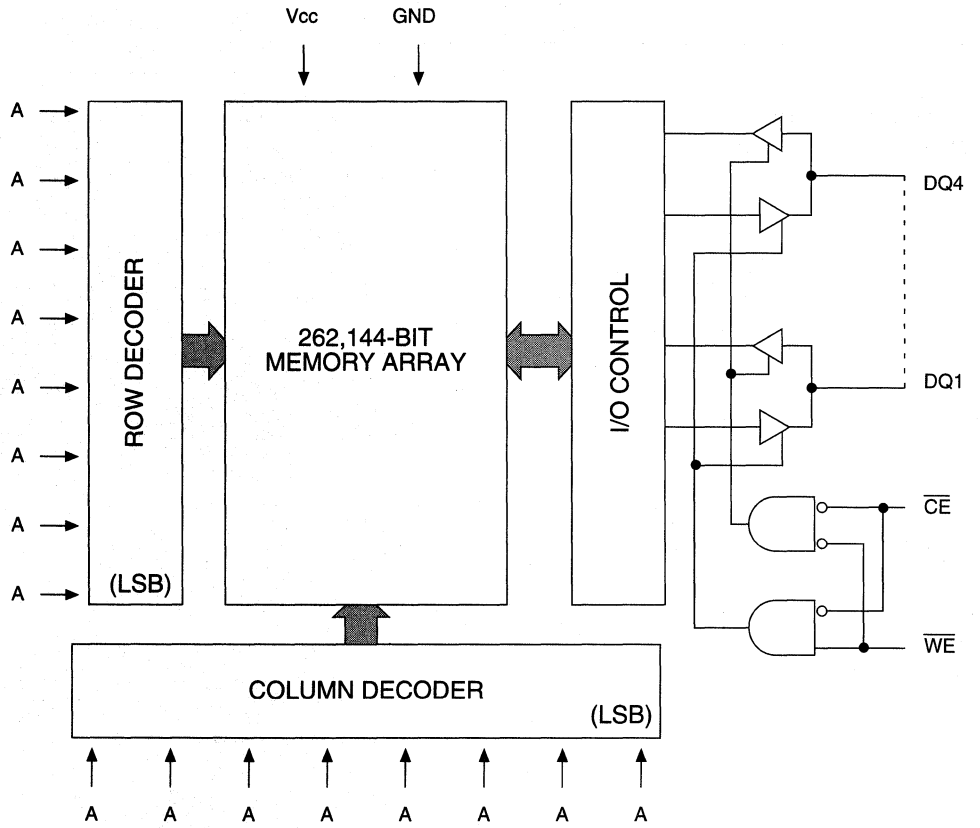
The MT5LC2564 is organized as a 65,536 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage	15, 20 and 25ns	Vcc	3.0	3.6	V	1
Supply Voltage	12ns	Vcc	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYM	TYP	-12**	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX outputs open f = MAX = 1/t_{RC}	Icc	75	125	110	95	90	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX outputs open f = MAX = 1/t_{RC}	I_{SB1}	17	35	30	25	25	mA	13
	$\overline{CE}$ ≥ Vcc - 0.2V; Vcc = MAX V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	1.0	3	3	3	3	mA	13

**The P version of this part is not available at 12ns.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	Vcc = 3.3V	Co	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13, 15) ($0°C \le T_A \le 70°C$)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	4		3		3		3		ns	7
Chip disable to output in High-Z	^tHZCE		6		8		9		9	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	4
Chip disable to power-down time	^tPD		12		15		20		25	ns	4
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	8		10		12		15		ns	
Address valid to end of write	^tAW	8		10		12		15		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		ns	
WRITE pulse width	$^tWP1$	8		10		12		15		ns	
WRITE pulse width	$^tWP2$	12		12		15		15		ns	
Data setup time	^tDS	7		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

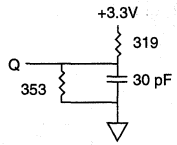


Fig. 1 OUTPUT LOAD EQUIVALENT

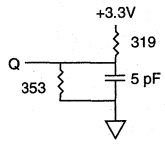


Fig. 2 OUTPUT LOAD EQUIVALENT

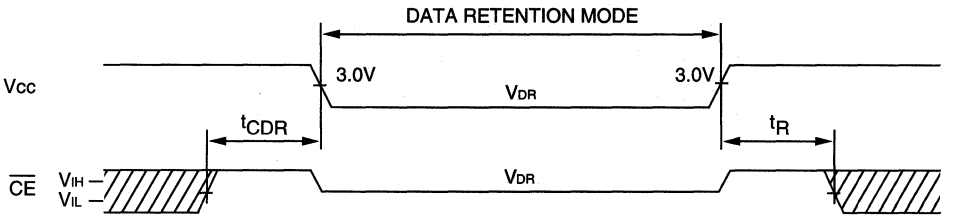
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \le +6.0V$ for $t \le {}^tRC/2$
   Undershoot: $V_{IL} \ge -2.0V$ for $t \le {}^tRC/2$
   Power-up: $V_{IH} \le +6.0V$ and $V_{CC} \le 3.1V$ for $t \le 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$ and ${}^tHZWE$ are specified with $C_L = 5pF$ as in Fig. 2. Transition is measured ± 200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Typical currents are measured at 25°C.
15. Vcc is 3.3V ±0.3V for the 15, 20 and 25ns speed grades and 3.3V ±0.2V for the 12ns speed grade.

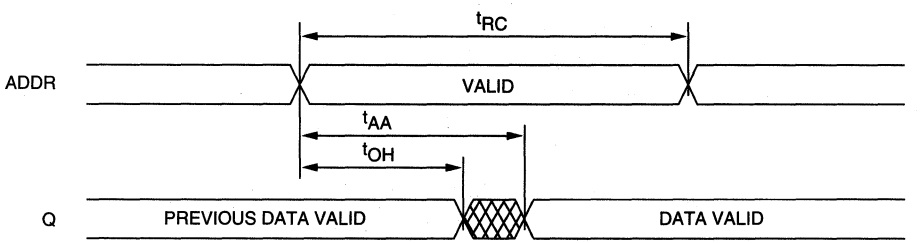
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current	$\overline{CE} \ge Vcc$ -0.2V Other inputs: $V_{IN} \ge Vcc$ -0.2V or $V_{IN} \le Vss$+0.2V Vcc = 2V	I_{CCDR}		310	500	µA	14
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

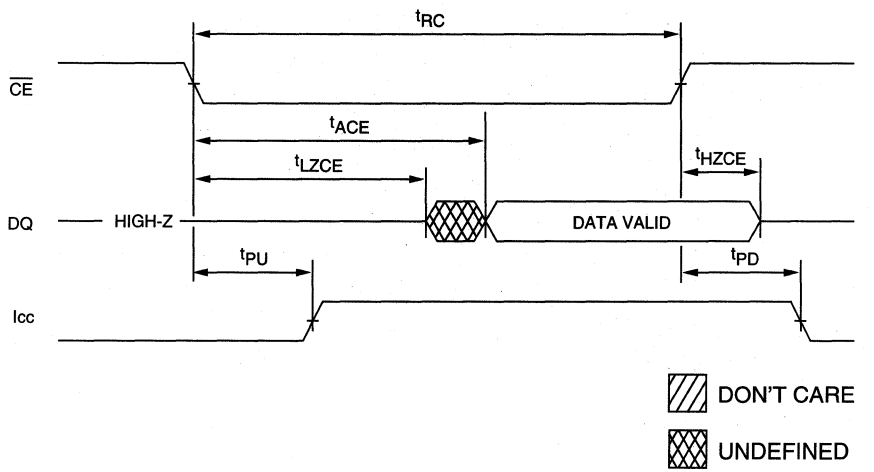
LOW Vcc DATA RETENTION WAVEFORM



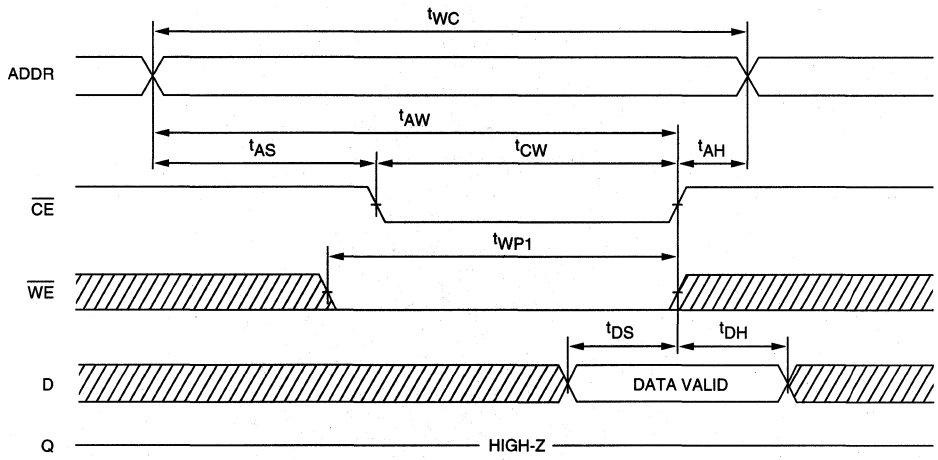
READ CYCLE NO. 1 [8, 9]



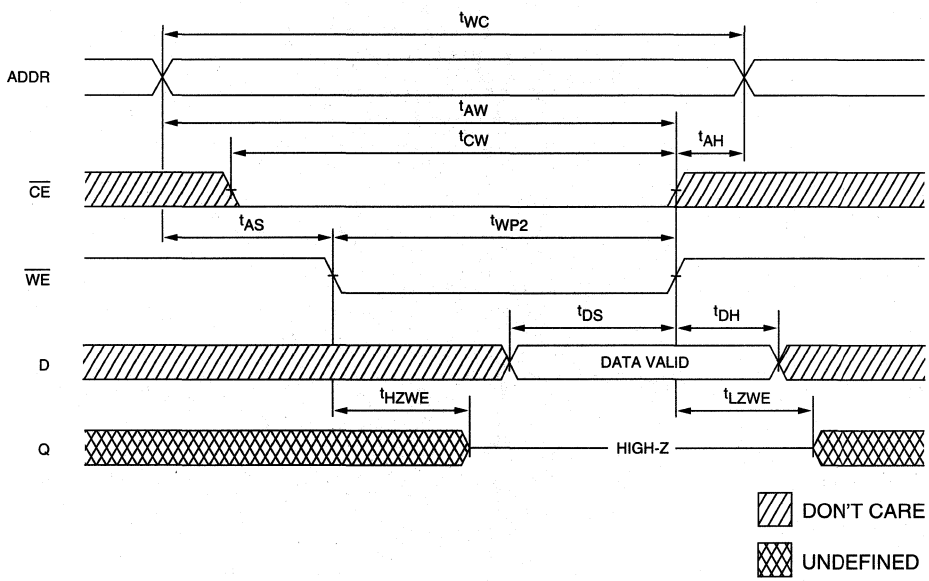
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



SRAM

64K x 4 SRAM

LOW VOLTAGE WITH OUTPUT ENABLE

FEATURES

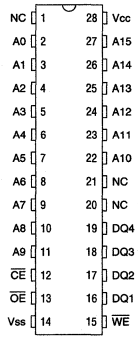
- All I/O pins are 5V tolerant
- High speed: 12, 15, 20 and 25
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Complies to JEDEC low-voltage TTL standards

OPTIONS — MARKING

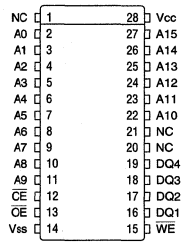
- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
- 2V data retention (optional) — L
- Temperature
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT5LC2565DJ-15 L

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-4)



28-Pin SOJ (SD-2)



GENERAL DESCRIPTION

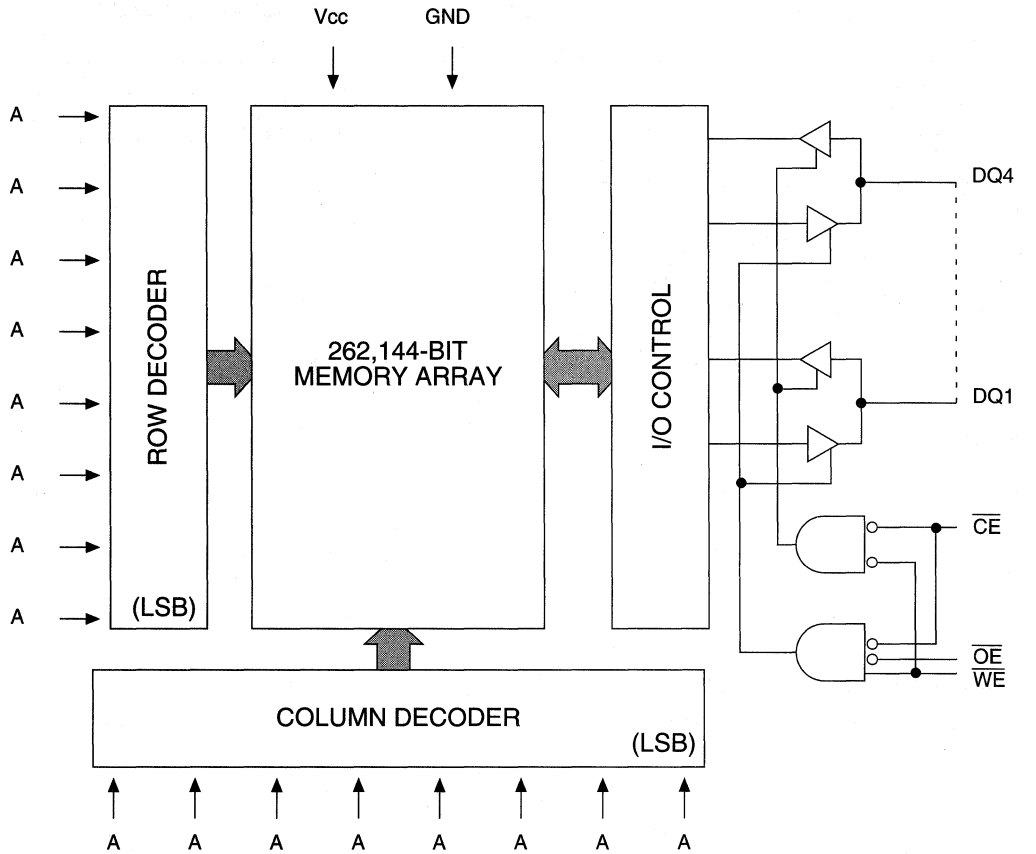
The MT5LC2565 is organized as a 65,536 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage	15, 20 and 25ns	V_{CC}	3.0	3.6	V	1
Supply Voltage	12ns	V_{CC}	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYM	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX outputs open f = MAX = $1/t_{RC}$	I_{CC}	75	125	110	95	90	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX outputs open f = MAX = $1/t_{RC}$	I_{SB1}	17	35	30	25	25	mA	13
	$\overline{CE} \ge V_{CC}$ - 0.2V; V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le V_{SS}$ + 0.2V	I_{SB2}	1.0	3	3	3	3	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13, 15) ($0°C \le T_A \le 70°C$)

DESCRIPTION	SYM	-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	7
Chip disable to output in High-Z	^tHZCE		6		8		9		9	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	4
Chip disable to power-down time	^tPD		12		15		20		25	ns	4
Output Enable access time	^tAOE		6		7		8		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		7		7	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	8		10		12		15		ns	
Address valid to end of write	^tAW	8		10		12		15		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		ns	
WRITE pulse width	$^tWP1$	8		10		12		15		ns	
WRITE pulse width	$^tWP2$	12		12		15		15		ns	
Data setup time	^tDS	7		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

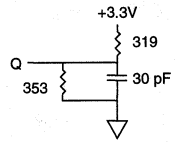


Fig. 1 OUTPUT LOAD EQUIVALENT

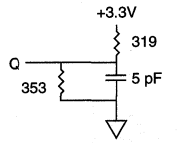


Fig. 2 OUTPUT LOAD EQUIVALENT

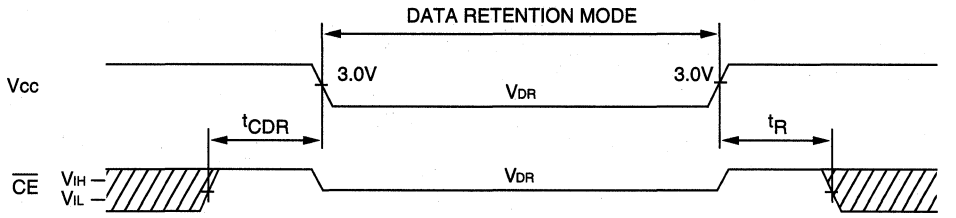
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with C_L = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Typical currents are measured at 25°C.
15. V_{CC} is 3.3V ±0.3V for the 15, 20 and 25ns speed grades and 3.3V ±0.2V for the 12ns speed grade.

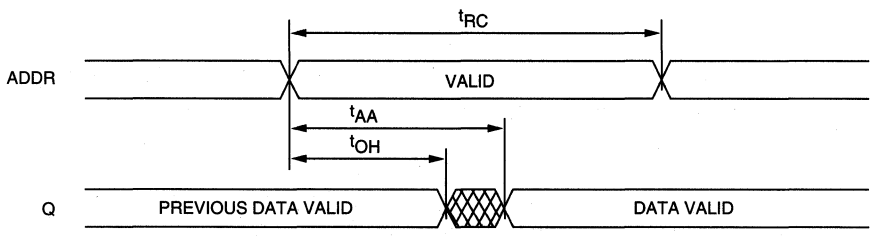
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq V_{CC}$ -0.2V Other inputs: $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq V_{SS}$+0.2V V_{CC} = 2V	I_{CCDR}		310	500	µA	14
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

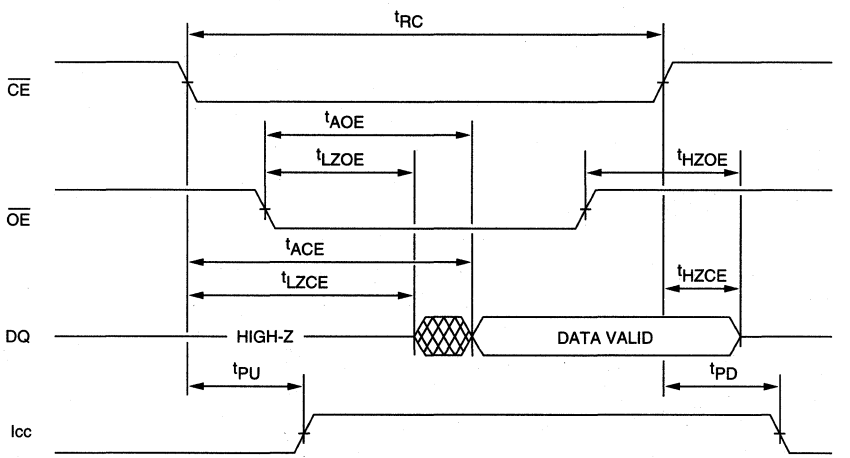
LOW Vcc DATA RETENTION WAVEFORM



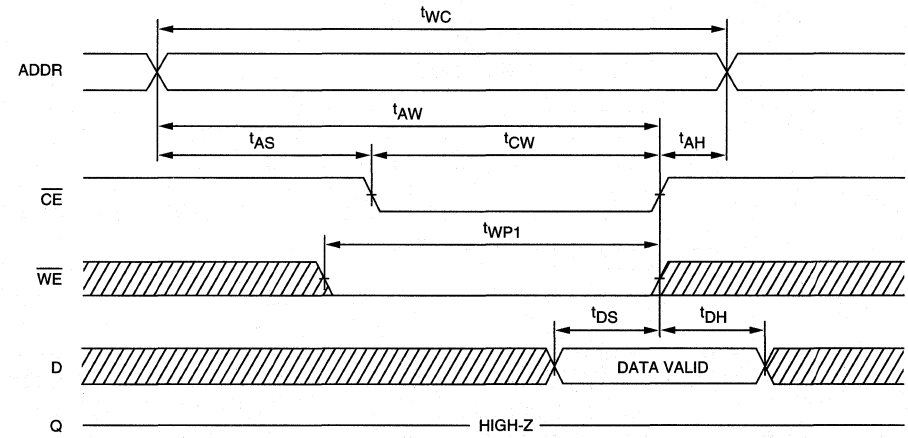
READ CYCLE NO. 1 [8, 9]



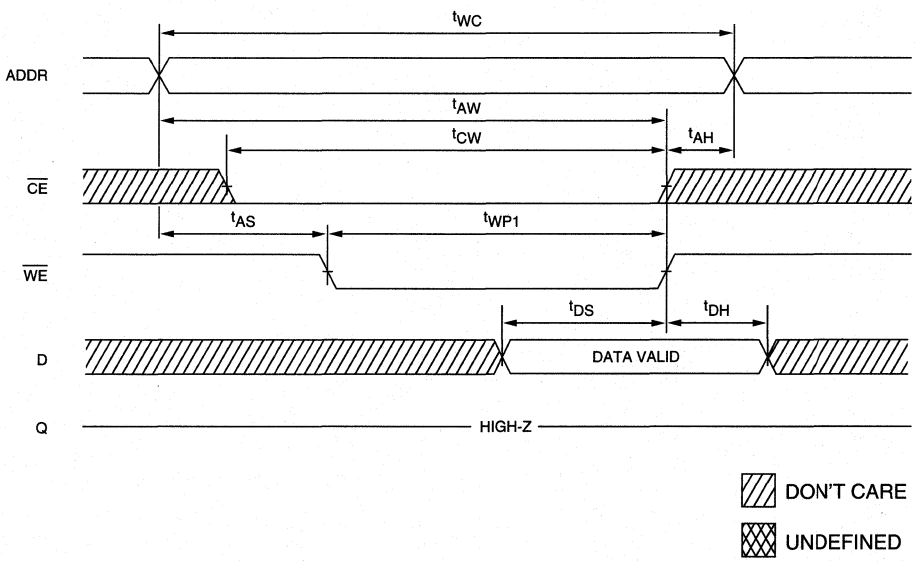
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

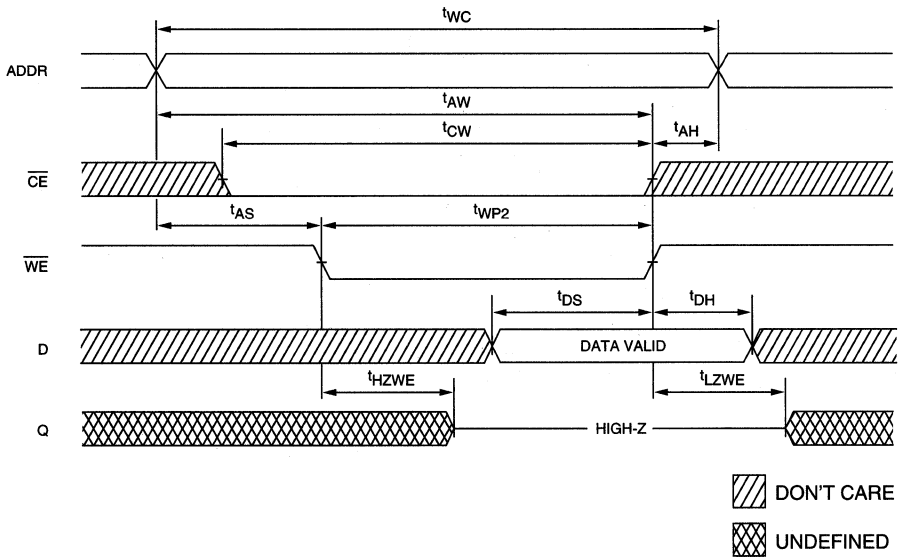


WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

256K x 4 SRAM

LOW VOLTAGE WITH OUTPUT ENABLE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 15, 17, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 7 and 8ns
- Complies to JEDEC low-voltage TTL standards

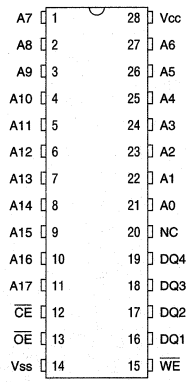
OPTIONS — MARKING

- Timing
  - 15ns access — -15
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic DIP (400 mil) — None
  - Plastic SOJ (400 mil) — DJ
- 2V data retention (optional) — L
- 2V data retention, low power (optional) — LP
- Temperature
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT5LC1005DJ-15 LP

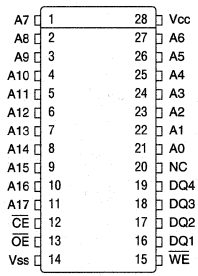
NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

28-Pin DIP
(SA-5)



28-Pin SOJ
(SD-3)



GENERAL DESCRIPTION

The MT5LC1005 is organized as a 262,144 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

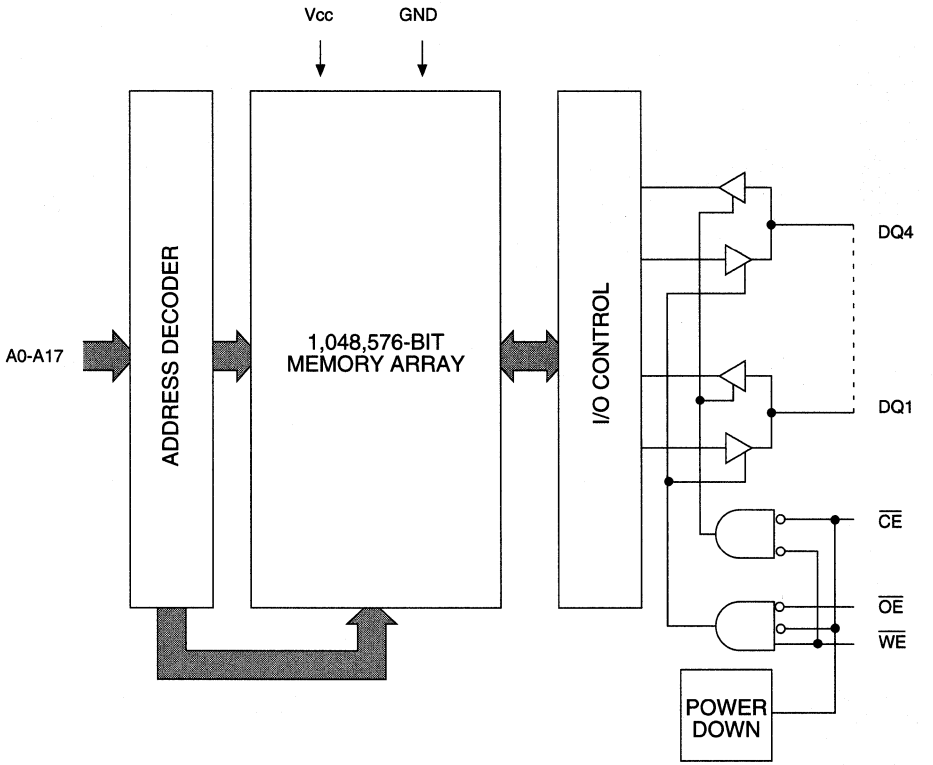
For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ are LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both CMOS standby current (I_{SB2}) and TTL standby current (I_{SB1}) over the standard part. This is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

					MAX					
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-15	-17	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX outputs open f = MAX = 1/t_{RC}	I_{CC}	ALL	70	155	145	135	125	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX outputs open f = MAX = 1/t_{RC}	I_{SB1}	STD, L	20	45	40	35	30	mA	13
			LP	1.5	3	3	3	3	mA	
	$\overline{CE}$ ≥ Vcc - 0.2V; Vcc = MAX V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD, L	1.0	3	3	3	3	mA	13
			LP	0.7	1.5	1.5	1.5	1.5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	Vcc = 3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13, 15) ($0°C \le T_A \le 70°C$)

DESCRIPTION		-15		-17		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	15		17		20		25		ns	
Address access time	^tAA		15		17		20		25	ns	
Chip Enable access time	^tACE		15		17		20		25	ns	
Output hold from address change	^tOH	3		3		3		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		17		20		25	ns	
Output Enable access time	^tAOE		6		6		7		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		7		8	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	15		17		20		25		ns	
Chip Enable to end of write	^tCW	10		12		12		15		ns	
Address valid to end of write	^tAW	10		12		12		15		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	9		12		12		15		ns	
WRITE pulse width	$^tWP2$	12		8		15		15		ns	
Data setup time	^tDS	7		7		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		5		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

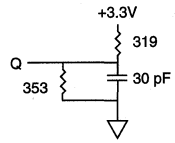


Fig. 1 OUTPUT LOAD EQUIVALENT

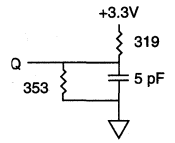


Fig. 2 OUTPUT LOAD EQUIVALENT

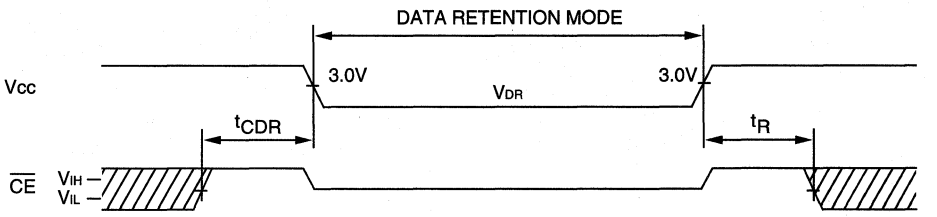
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with $C_L = 5pF$ as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
14. Typical currents are measured at 25°C.

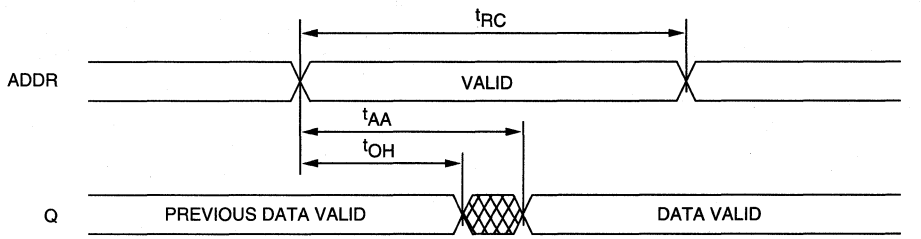
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq Vcc -0.2V$ Other inputs: $V_{IN} \geq Vcc -0.2V$ or $V_{IN} \leq Vss+0.2V$ $Vcc = 2V$	I_{CCDR}		145	260	µA	14
Data Retention Current LP version	$\overline{CE} \geq Vcc -0.2V$ $Vcc = 2V$	I_{CCDR}		145	260	µA	14
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

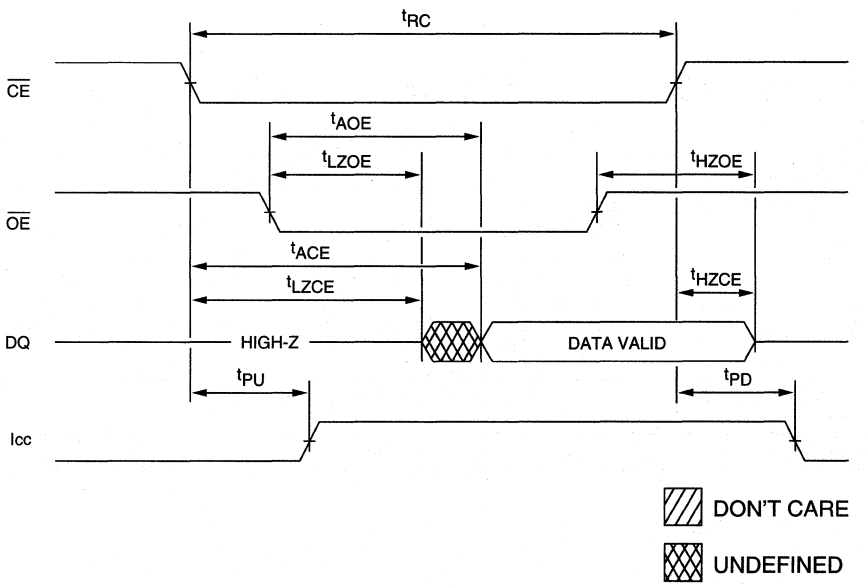
LOW Vcc DATA RETENTION WAVEFORM



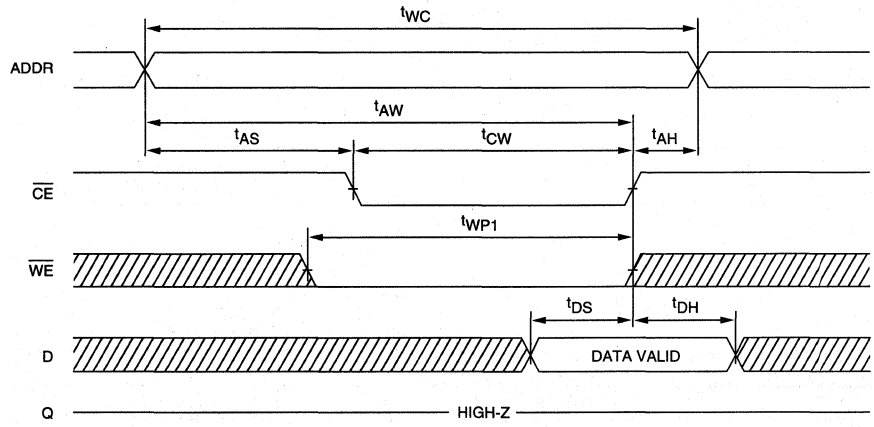
READ CYCLE NO. 1 [8, 9]



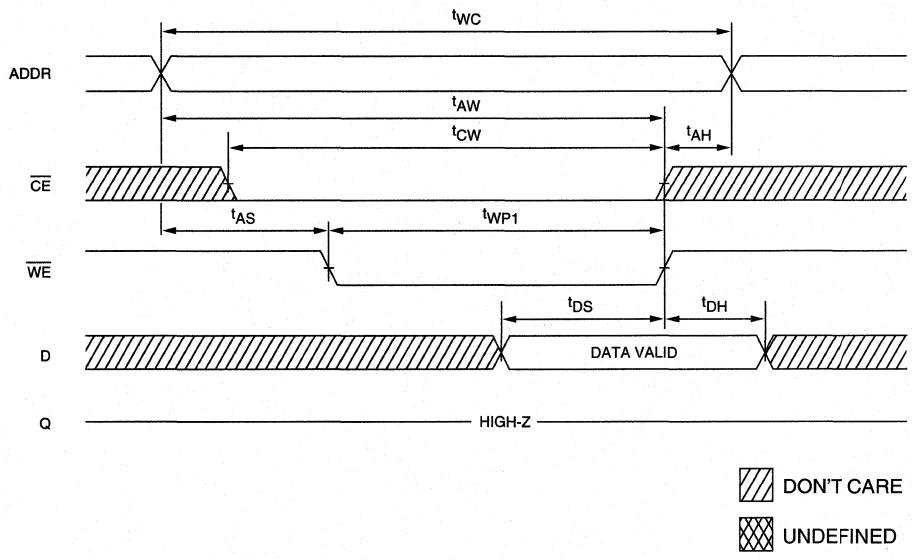
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

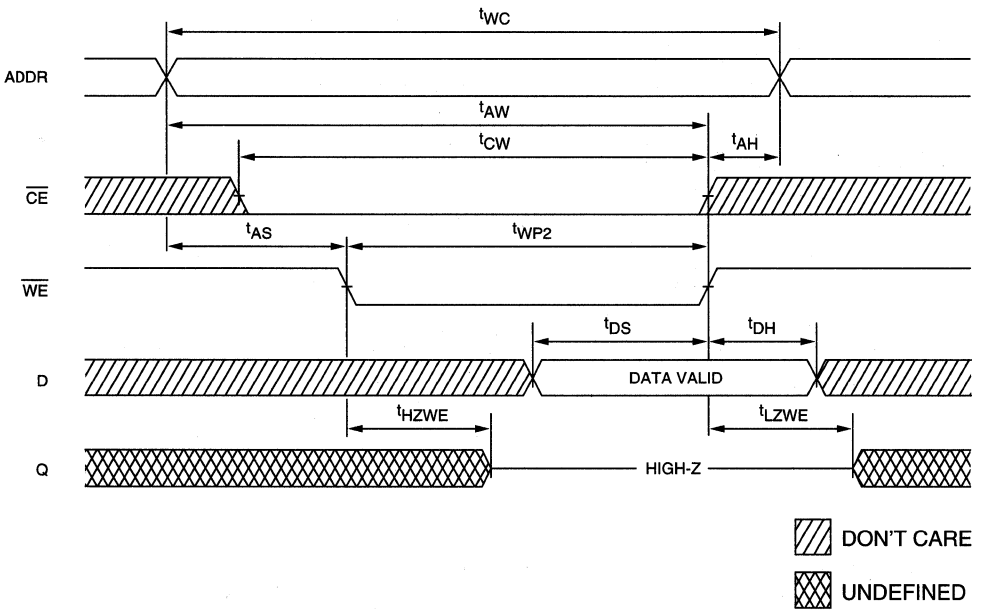


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

256K x 4 SRAM

REVOLUTIONARY PINOUT, 3.3V
OPERATION WITH SINGLE CHIP ENABLE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12*, 15, 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL-compatible
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Fast $\overline{OE}$ access times: 8, 10 and 12ns
- Complies to JEDEC low-voltage TTL standards

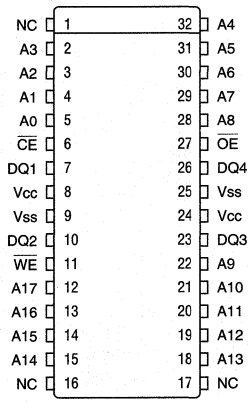
OPTIONS — MARKING

- Timing
  - 12ns access — -12*
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 32-pin SOJ (400 mil) — DJ
- 2V data retention (optional) — L
- Temperature
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT5LC256K4D4DJ-20 L

*Consult the factory for availability.

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

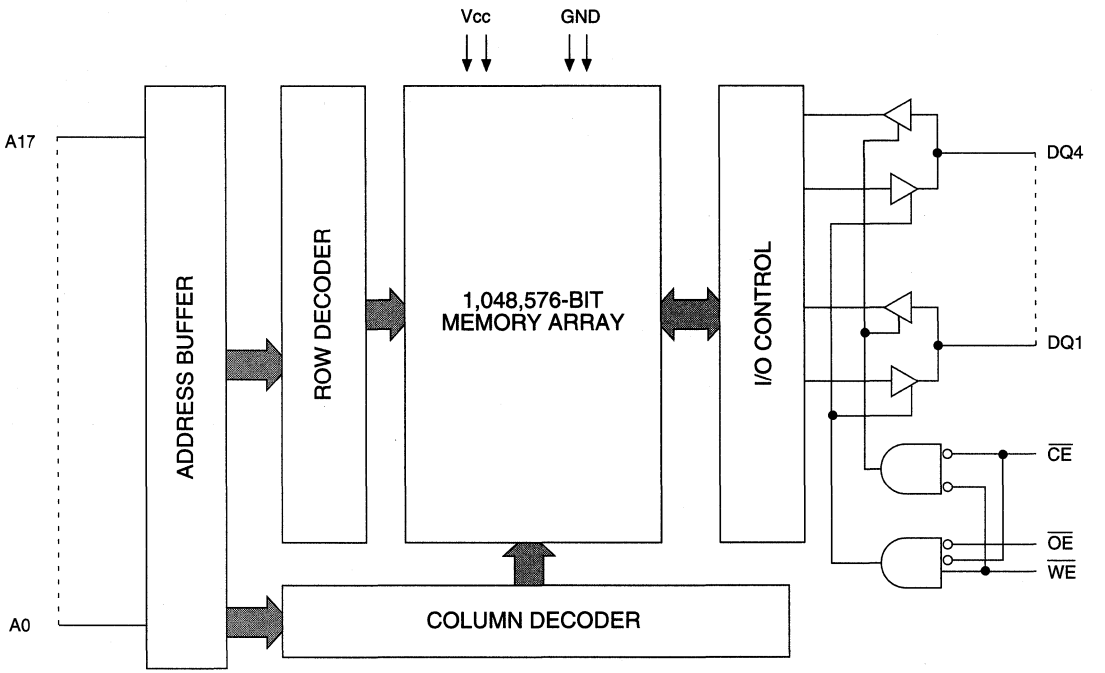
The MT5LC256K4D4 is organized as a 262,144 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ are LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ AND TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 32, 31, 30, 29, 28, 22, 21, 20, 19, 18, 15, 14, 13, 12	A0-A17	Input	Address Inputs: These inputs determine which cell is addressed.
11	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
6	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
27	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
7, 10, 23, 26	DQ1-DQ4	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	Vcc	Supply	Power Supply: 3.3V ±0.3V
9, 25	Vss	Supply	Ground: GND
1, 16, 17	NC	-	No Connect: These signals are not internally connected.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 3.3V \pm 0.3V$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	165	280	230	180	160	mA	3, 15
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	35	60	50	40	35	mA	15
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.5	5	5	5	5	mA	15

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} =3.3V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13, 15) ($0°C \le T_A \le 70°C$)

DESCRIPTION	SYM	-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	3		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	9		10		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	9		10		12		14		ns	
WRITE pulse width	$^tWP2$	10		10		12		14		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

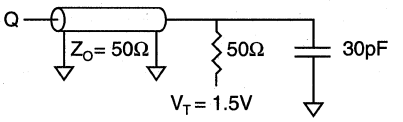


Fig. 1 OUTPUT LOAD EQUIVALENT

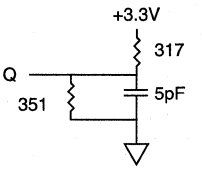


Fig. 2 OUTPUT LOAD EQUIVALENT

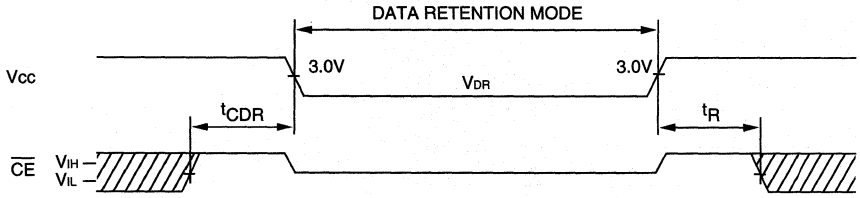
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded and $f = \frac{1}{{}^tRC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with C_L = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. The output will be in the High-Z state if output enable is high.
14. Typical currents are measured at 25°C.
15. Typical values are measured at 3.3V, 25°C and 15ns cycle time.

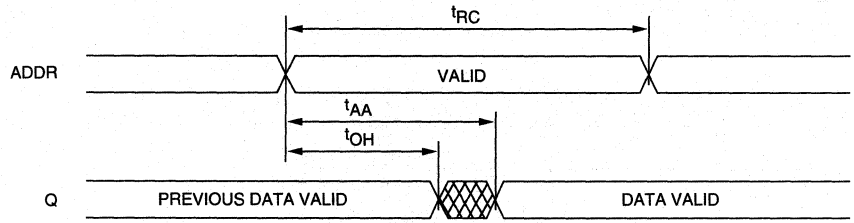
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	V_{CC} = 2V	I_{CCDR}		70	300	µA	14
Chip Deselect to Data Retention Time			${}^tCDR$	0			ns	4
Operation Recovery Time			${}^tR$	${}^tRC$			ns	4, 11

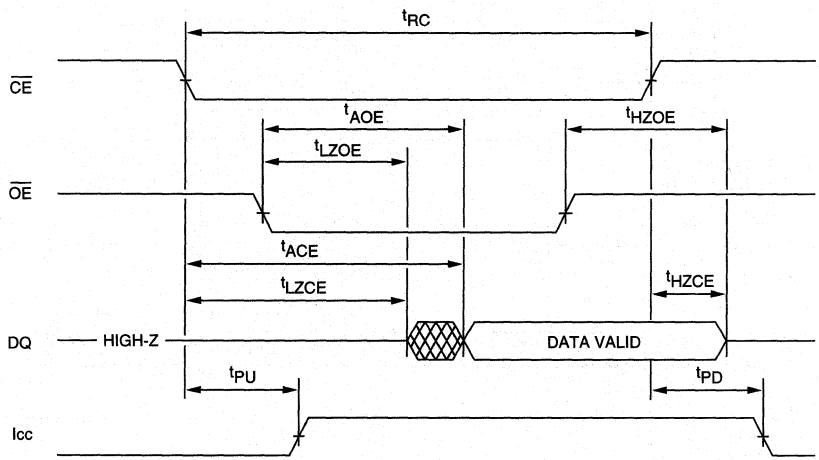
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



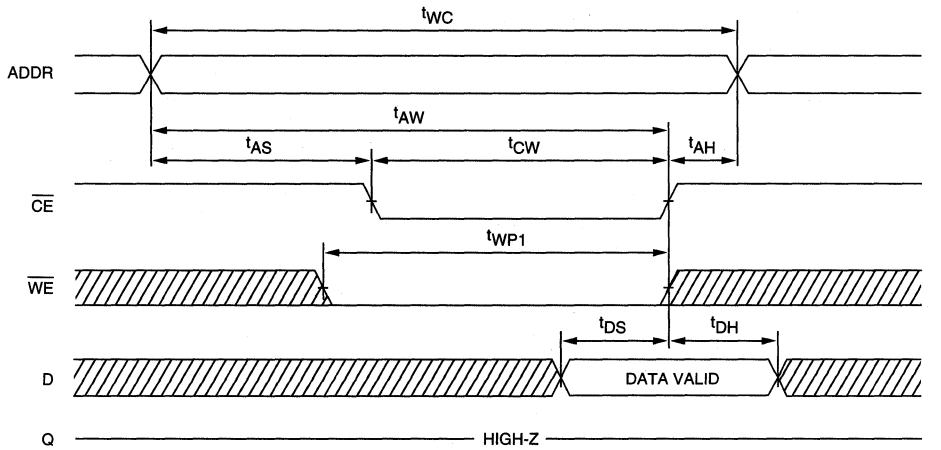
READ CYCLE NO. 2 [7, 8, 10]



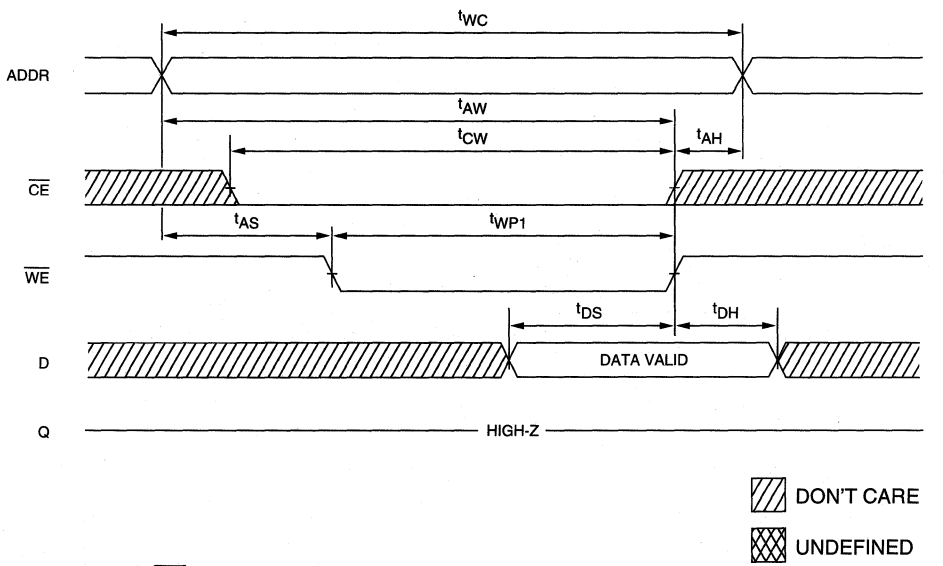
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

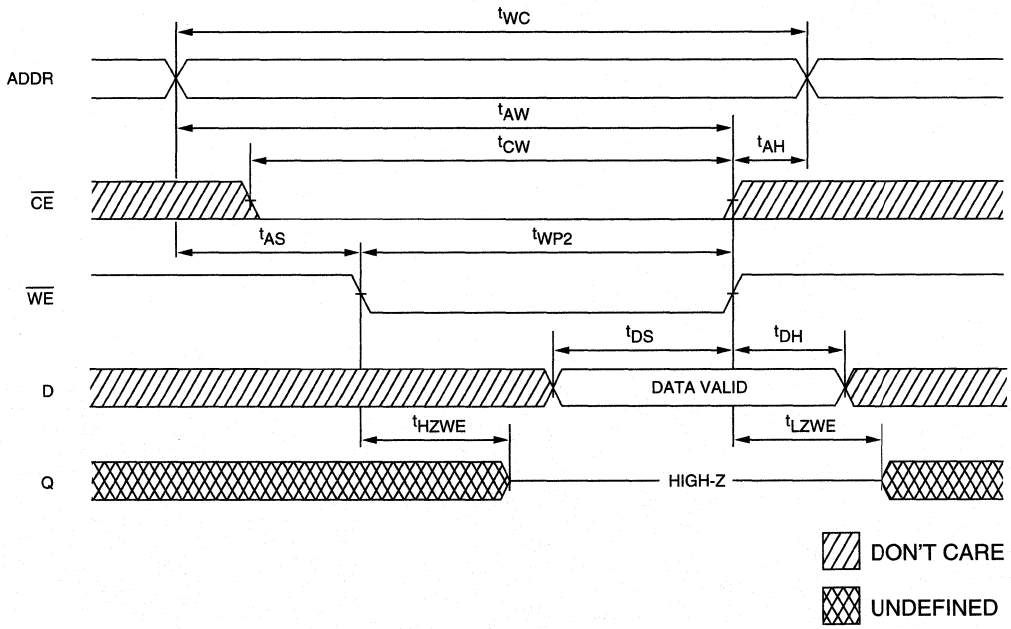


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

MICRON SEMICONDUCTOR, INC.

MT5LC256K4D4
REVOLUTIONARY PINOUT 256K x 4 SRAM

SRAM

1 MEG x 4 SRAM

3.3V OPERATION WITH OUTPUT ENABLE, REVOLUTIONARY PINOUT

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 8, 10, 12 and 15ns
- Complies to JEDEC low-voltage TTL standards

OPTIONS / MARKING

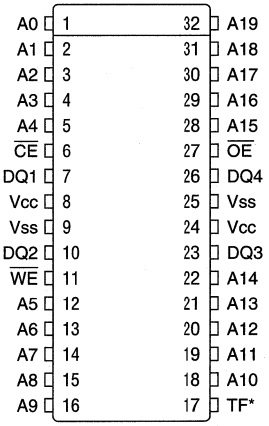
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic SOJ (400 mil)	DJ
• 2V data retention (optional)	L
• Temperature	
Commercial (0°C to +70°C)	None

- Part Number Example: MT5LC1M4D4DJ-20

NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



* TF = Test Function. See note 14.

GENERAL DESCRIPTION

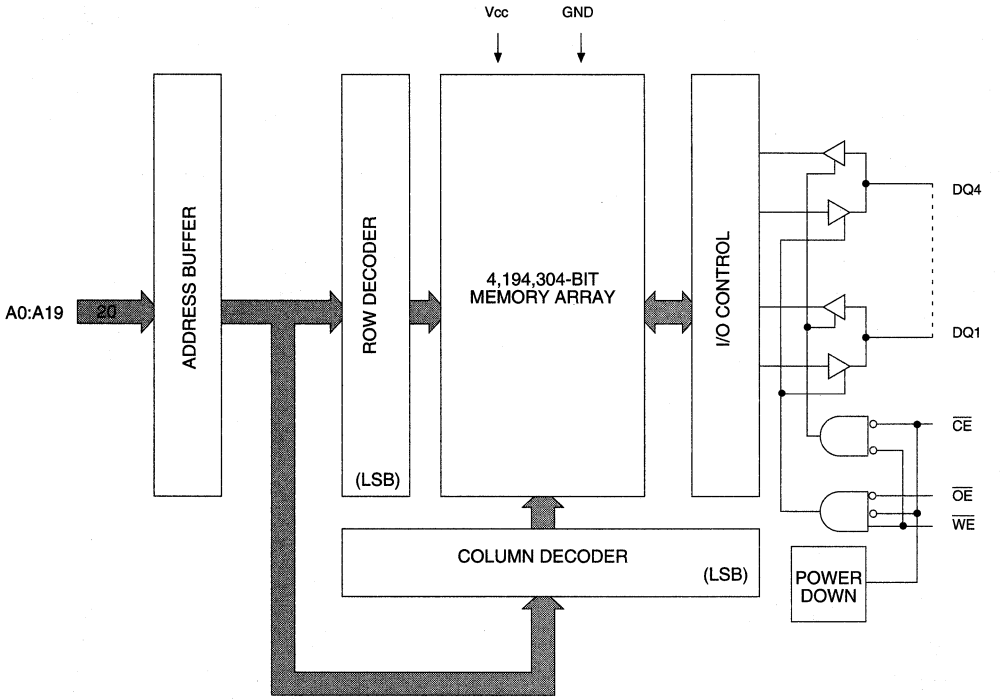
The MT5LC1M4D4 is organized as a 1,048,576 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to this device is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while output enable ($\overline{OE}$) and $\overline{CE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

THERMAL IMPEDANCE (estimated)

PACKAGE	NUMBER OF PINS	θ_{JC} (°C/W)	θ_{JA} (°C/W)	NOTES
SOJ	32	15	60	13, 15
TSOP	32	5	70	13, 15

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC; outputs open	I_{CC}	185	165	160	155	145	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	80	75	70	70	65	mA	
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX; f = 0 VIN ≥ Vcc -0.2V or VIN ≤ VSS +0.2	I_{SB2}	1.0	1.0	1.0	1.0	1.0	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	Vcc = 3.3V	Co	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	4
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	4
Output Enable access time	^tAOE		6		8		10		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		7		10		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		10		12		15		20		ns	
WRITE pulse width	$^tWP2$	11		12		15		15		20		ns	
Data setup time	^tDS	6		7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

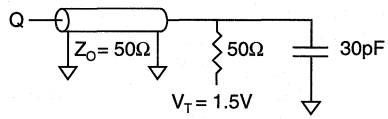


Fig. 1 OUTPUT LOAD EQUIVALENT

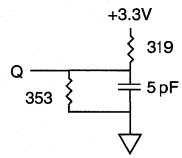


Fig. 2 OUTPUT LOAD EQUIVALENT

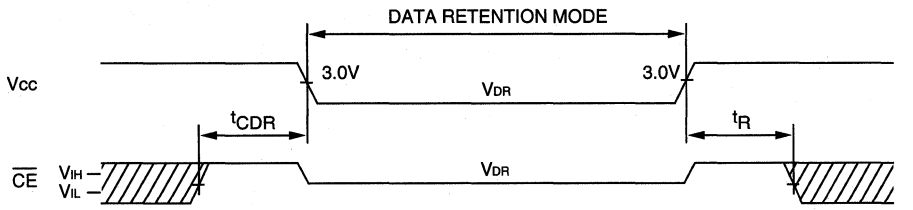
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.
14. The test function pin (TF) can be treated as a no connect pin. However, it is recommended that the pin be grounded.
15. The thermal impedance numbers assume the device is socketed on a PC board and air flow is zero.

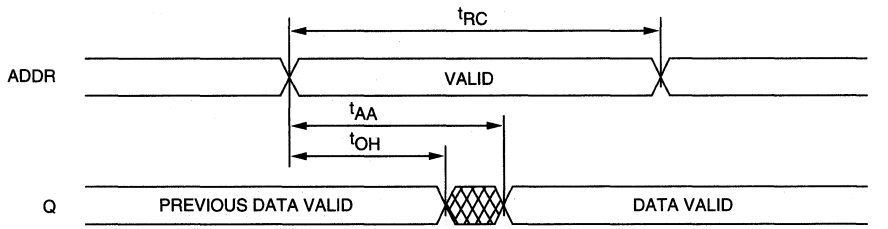
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2		V	
Data Retention Current	$\overline{CE} \geq (Vcc -0.2V)$ $V_{IN} \geq (Vcc -0.2V)$ or $\leq 0.2V$ Vcc = 2.0V	I_{CCDR}		700	µA	
Chip Deselect to Data Retention Time		${}^tCDR$	0		ns	4
Operation Recovery Time		${}^tR$	${}^tRC$		ns	4, 11

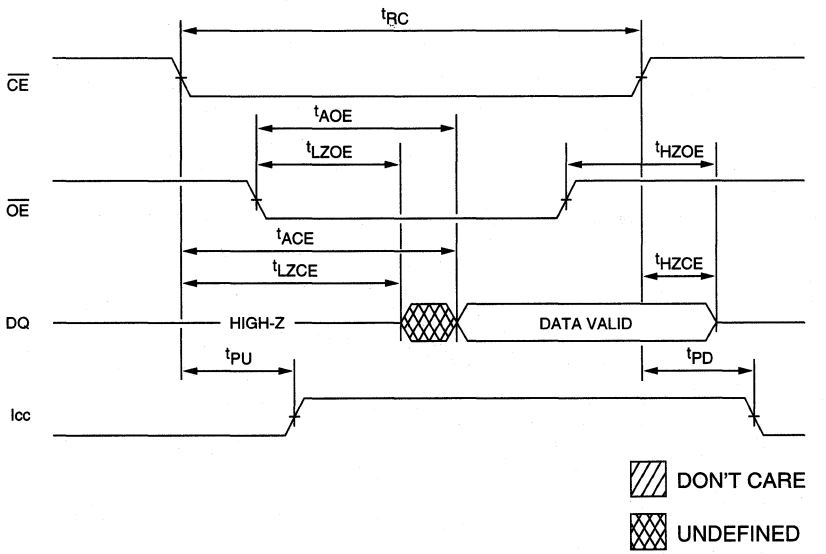
LOW Vcc DATA RETENTION WAVEFORM



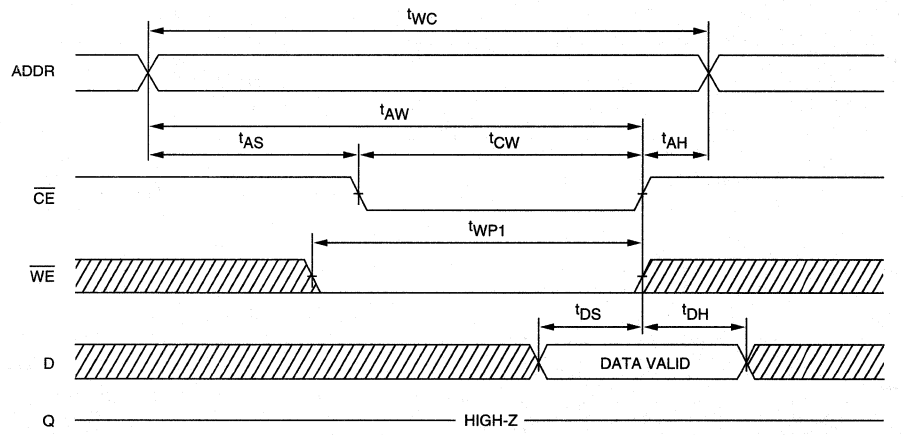
READ CYCLE NO. 1 [8, 9]



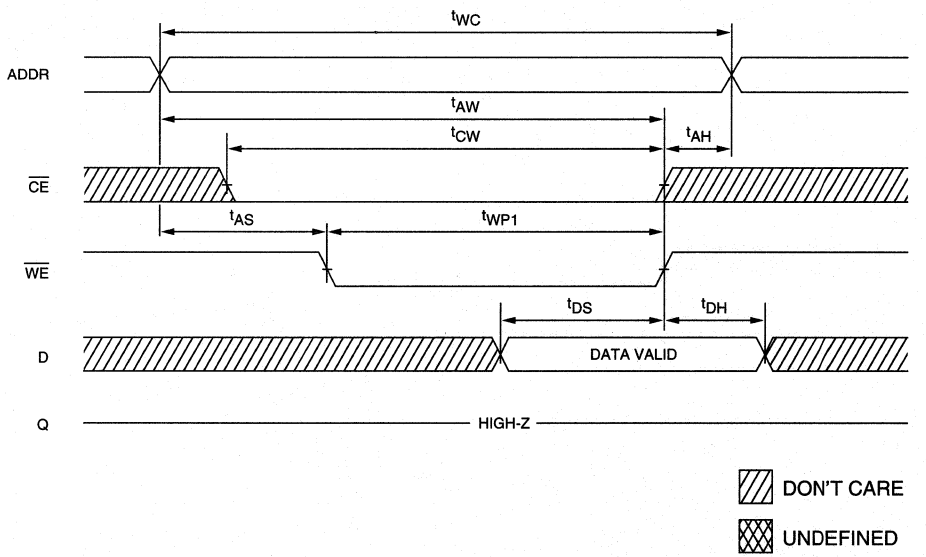
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

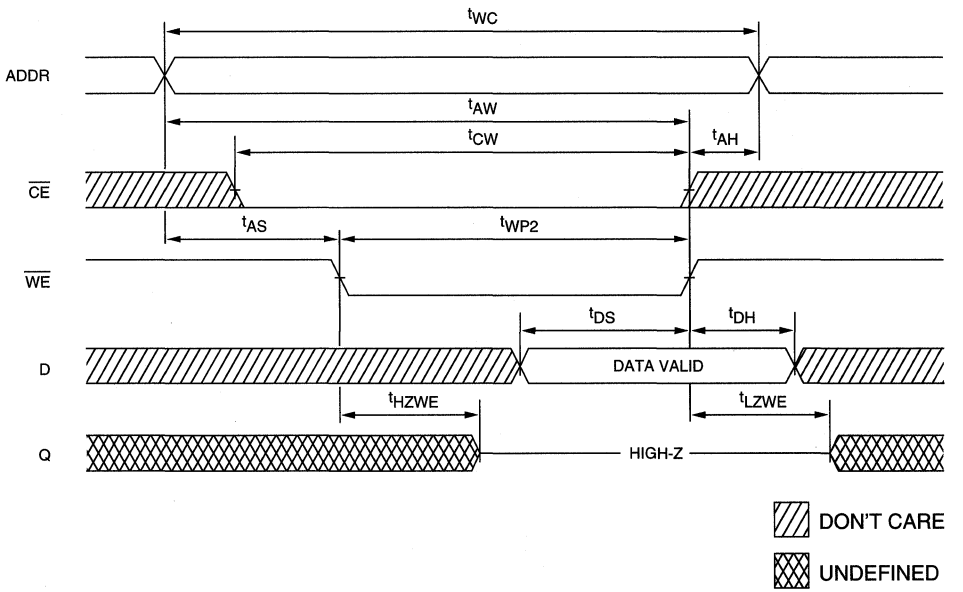


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

32K x 8 SRAM

LOW VOLTAGE

FEATURES

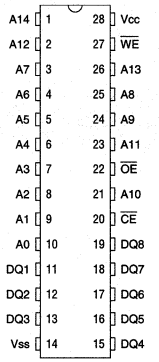
- All I/O pins are 5V tolerant
- High speed: 12, 15, 20 and 25
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Complies to JEDEC low-voltage TTL standards

OPTIONS — MARKING

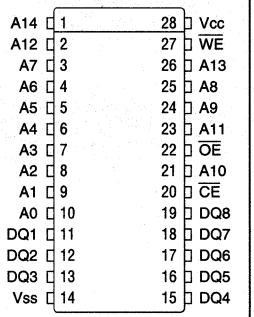
- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
- 2V data retention (optional) — L
- Temperature
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT5LC2568DJ-15 L

PIN ASSIGNMENT (Top View)

28-Pin DIP (SA-4)



28-Pin SOJ (SD-2)



GENERAL DESCRIPTION

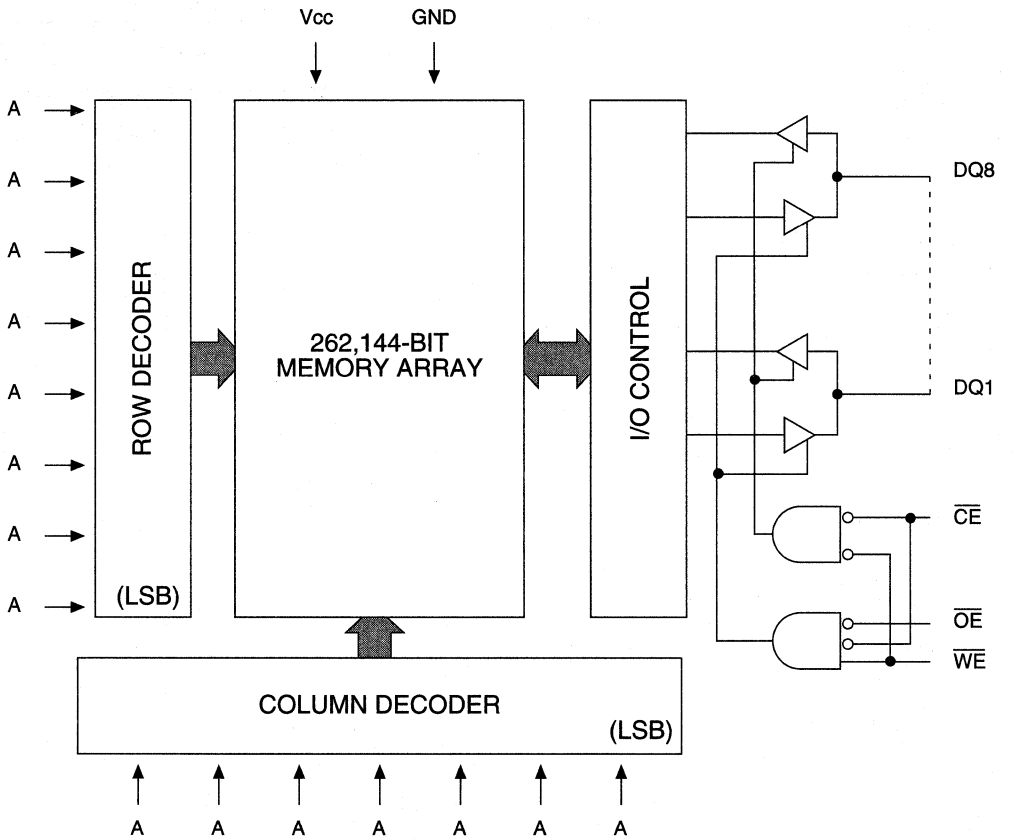
The MT5LC2568 is organized as a 32,768 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage	15, 20 and 25ns	V_{CC}	3.0	3.6	V	1
Supply Voltage	12ns	V_{CC}	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYM	TYP	-12**	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX outputs open f = MAX = 1/t_{RC}	I_{CC}	75	125	110	95	90	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX outputs open f = MAX = 1/t_{RC}	I_{SB1}	17	35	30	25	25	mA	13
	$\overline{CE} \ge V_{CC}$ - 0.2V; V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le V_{SS}$ + 0.2V	I_{SB2}	1.0	3	3	3	3	mA	13

**The P version of this part is not available at 12ns.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13, 15) ($0°C \le T_A \le 70°C$)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	7
Chip disable to output in High-Z	^tHZCE		6		8		9		9	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	4
Chip disable to power-down time	^tPD		12		15		20		25	ns	4
Output Enable access time	^tAOE		6		7		8		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		7		7	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	8		10		12		15		ns	
Address valid to end of write	^tAW	8		10		12		15		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		ns	
WRITE pulse width	$^tWP1$	8		10		12		15		ns	
WRITE pulse width	$^tWP2$	12		12		15		15		ns	
Data setup time	^tDS	7		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10	ns	6,7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

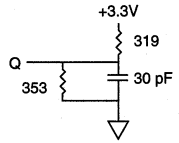


Fig. 1 OUTPUT LOAD EQUIVALENT

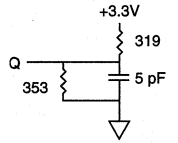


Fig. 2 OUTPUT LOAD EQUIVALENT

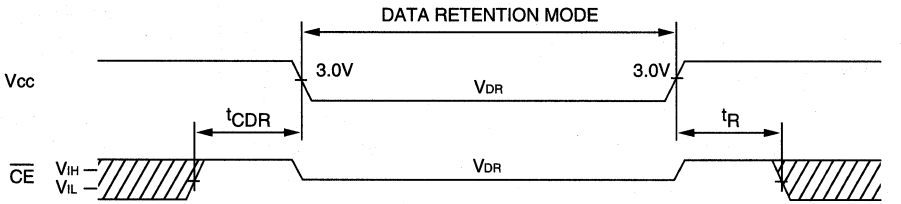
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with C_L = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Typical currents are measured at 25°C.
15. Vcc is 3.3V ±0.3V for the 15, 20 and 25ns speed grades and 3.3V ±0.2V for the 12ns speed grade.

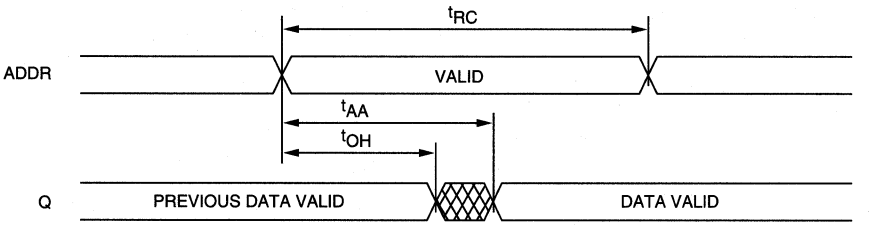
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq V_{CC}$ -0.2V Other inputs: $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq V_{SS}$+0.2V V_{CC} = 2V	I_{CCDR}		310	500	µA	14
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

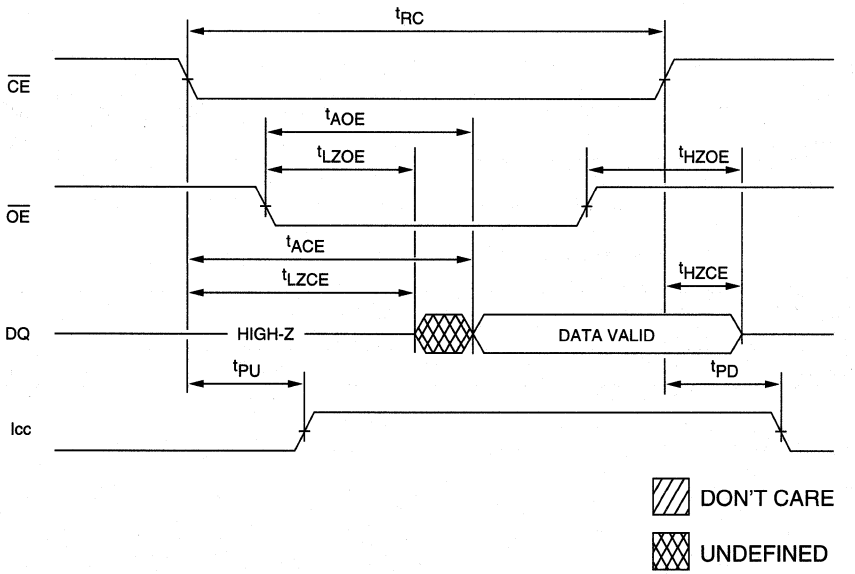
LOW Vcc DATA RETENTION WAVEFORM



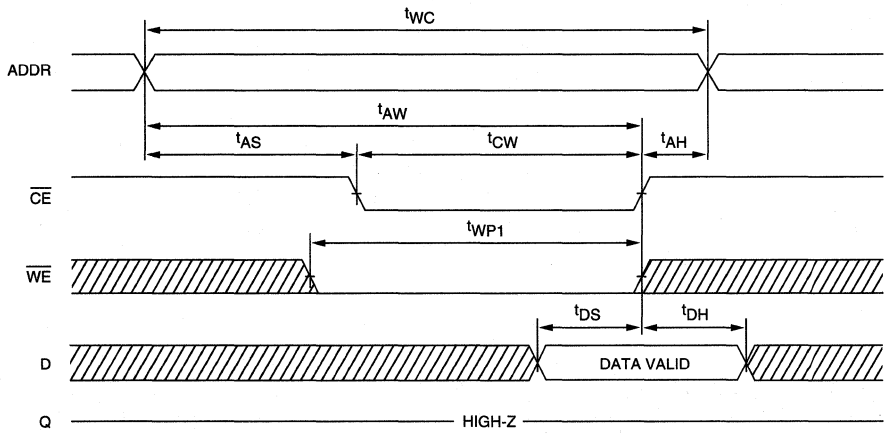
READ CYCLE NO. 1 [8, 9]



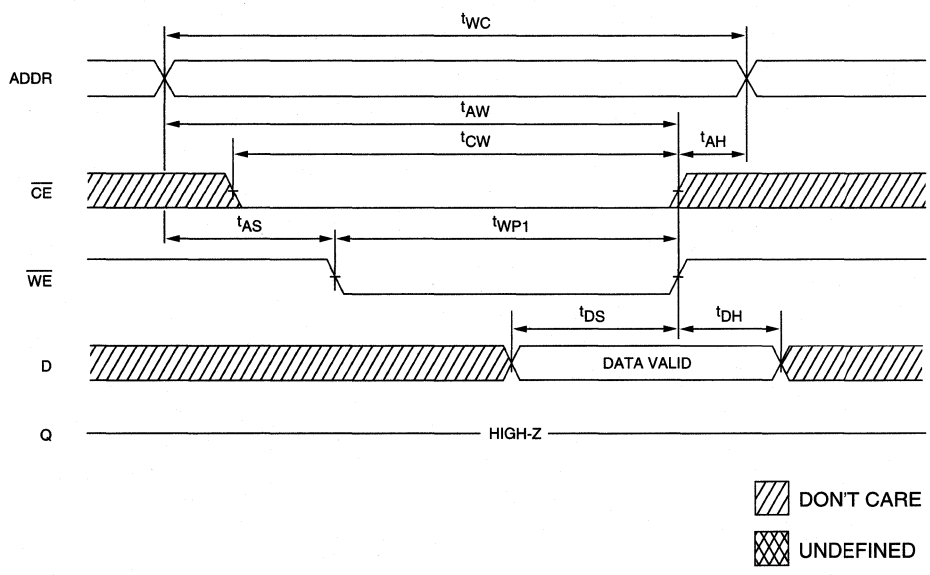
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

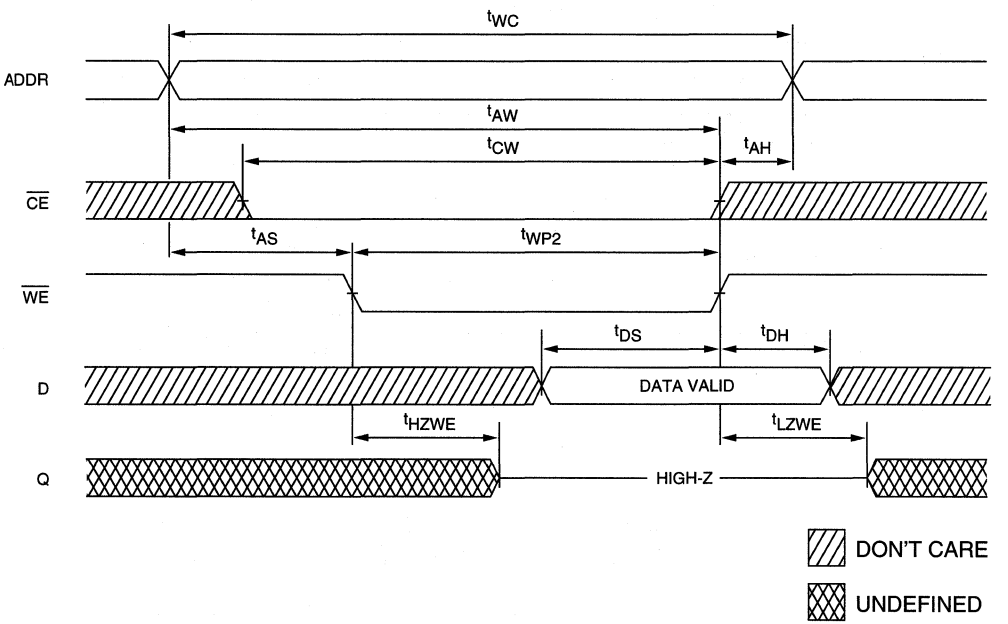


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

128K x 8 SRAM

LOW VOLTAGE WITH OUTPUT ENABLE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 15, 17, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 7 and 8ns
- Complies to JEDEC low-voltage TTL standards

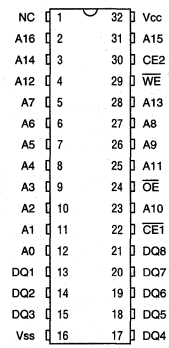
OPTIONS — MARKING

- Timing
  - 15ns access — -15
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic DIP (400 mil) — None
  - Plastic SOJ (400 mil) — DJ
  - Plastic SOJ (300 mil) — SJ
- 2V data retention (optional) — L
- 2V data retention, low power (optional) — LP
- Temperature
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT5LC1008DJ-15 LP

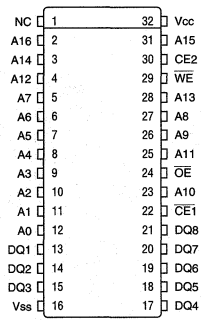
NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin DIP
(SA-6)



32-Pin SOJ
(SD-4)
(SD-5)



GENERAL DESCRIPTION

The MT5LC1008 is organized as a 131,072 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

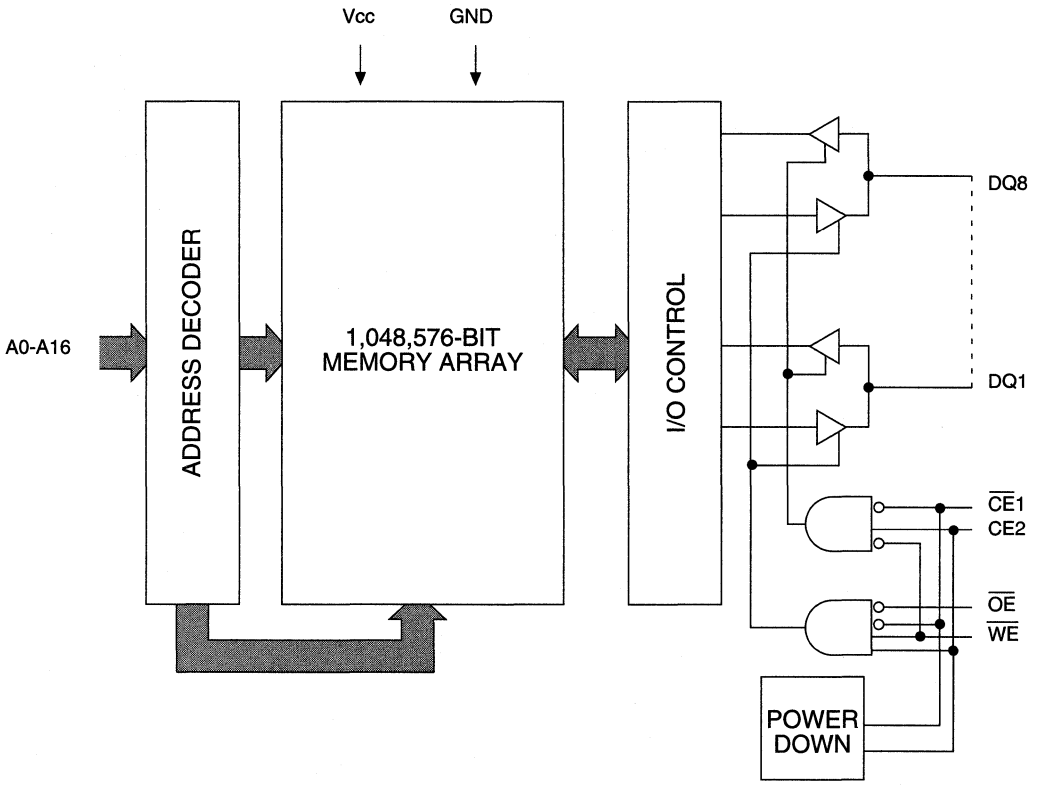
For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2). This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ goes LOW. The device offers reduced power standby modes when disabled. These modes allow system designers to meet low standby power requirements.

The "LP" version provides a reduction in both CMOS standby current (I_{SB2}) and TTL standby current (I_{SB1}) over the standard part. This is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery-backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
NOT SELECTED	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

					MAX					
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-15	-17	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE1} \le V_{IL}$ and CE2 ≥ V_{IH}; V_{CC} = MAX; outputs open f = MAX = $1/t_{RC}$	I_{CC}	ALL	70	155	145	135	125	mA	3, 14
Power Supply Current: Standby	$\overline{CE1} \le V_{IH}$ and CE2 ≥ V_{IL}; V_{CC} = MAX; outputs open f = MAX = $1/t_{RC}$	I_{SB1}	STD, L	20	45	40	35	30	mA	14, 15
			LP	1.5	3	3	3	3	mA	
	$\overline{CE1} \ge V_{CC}$ - 0.2V or CE2 ≤ Vss + o.2V V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le$ Vss + 0.2V	I_{SB2}	STD, L	1.0	3	3	3	3	mA	14, 16
			LP	0.7	1.5	1.5	1.5	1.5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13, 15) (0°C ≤ T_A ≤ 70°C)

DESCRIPTION	SYM	-15		-17		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	^tRC	15		17		20		25		ns	
Address access time	^tAA		15		17		20		25	ns	
Chip Enable access time	^tACE		15		17		20		25	ns	
Output hold from address change	^tOH	3		3		3		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		15		17		20		25	ns	
Output Enable access time	^tAOE		6		6		7		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		7		8	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	15		17		20		25		ns	
Chip Enable to end of write	^tCW	10		12		12		15		ns	
Address valid to end of write	^tAW	10		12		12		15		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	9		12		12		15		ns	
WRITE pulse width	$^tWP2$	12		13		15		15		ns	
Data setup time	^tDS	7		8		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		5		ns	7
Write Enable to output in High-Z	^tHZWE		6		7		8		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

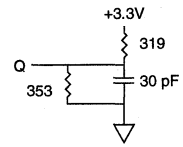


Fig. 1 OUTPUT LOAD EQUIVALENT

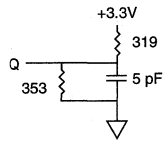


Fig. 2 OUTPUT LOAD EQUIVALENT

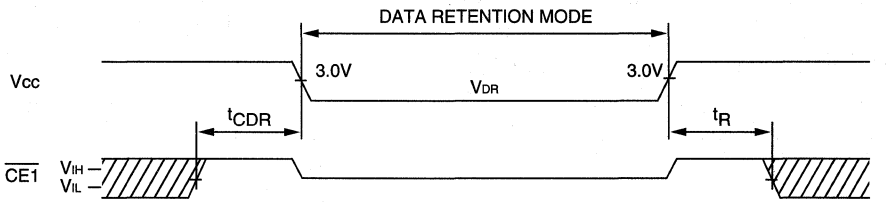
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \le +6.0V$ for $t \le {}^tRC/2$
   Undershoot: $V_{IL} \ge -2.0V$ for $t \le {}^tRC/2$
   Power-up: $V_{IH} \le +6.0V$ and $V_{CC} \le 3.1V$ for $t \le 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with $C_L = 5pF$ as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. CE2 timing is the same as $\overline{CE1}$ timing. The wave form is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
15. One chip enable must be inactive; the other may be $\ge V_{IH}$ or $\le V_{IL}$.
16. One chip enable must be inactive; the other may be $\le V_{SS} +0.2$ or $\ge V_{CC} -0.2$.
17. Typical currents are measured at 25°C.

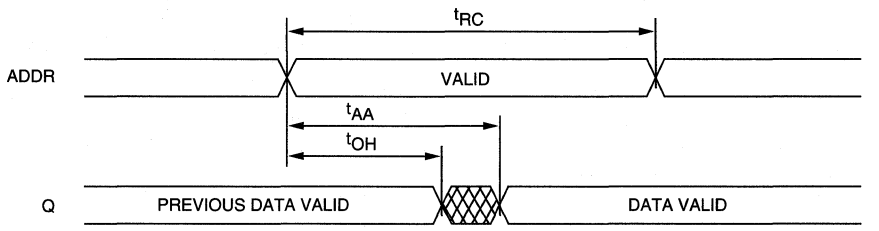
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE1} \ge V_{CC} -0.2V$ or $CE2 \le V_{SS} +0.2V$ Other inputs: $V_{IN} \ge V_{CC} -0.2V$ or $V_{IN} \le V_{SS} +0.2V$ $V_{CC} = 2V$	I_{CCDR}		145	260	µA	16, 17
Data Retention Current LP version	$\overline{CE1} \ge V_{CC} -0.2V$ or $CE2 \le V_{SS} +0.2V$ $V_{CC} = 2V$	I_{CCDR}		145	260	µA	16, 17
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

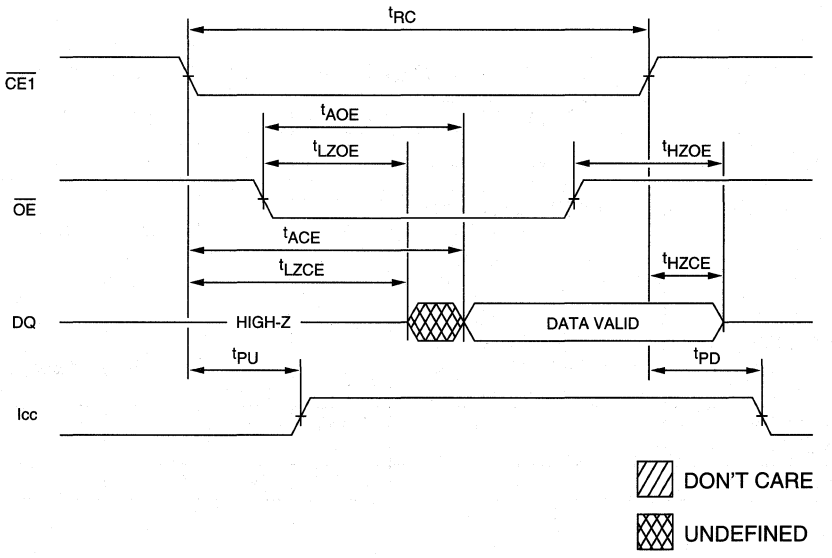
LOW Vcc DATA RETENTION WAVEFORM [12]



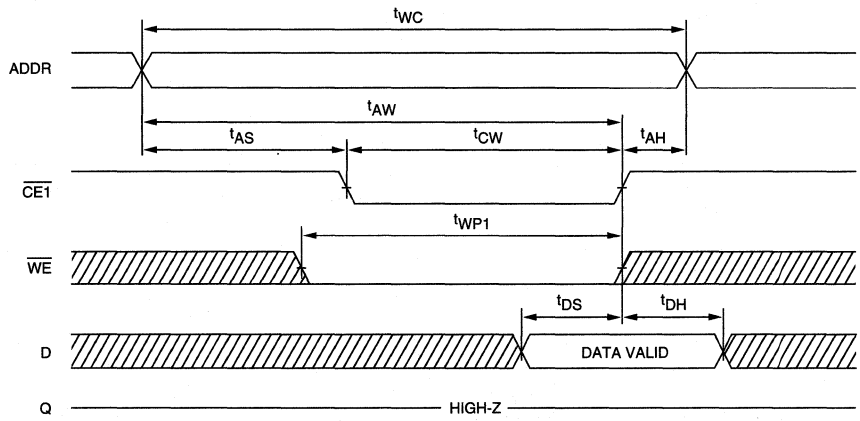
READ CYCLE NO. 1 [8, 9]



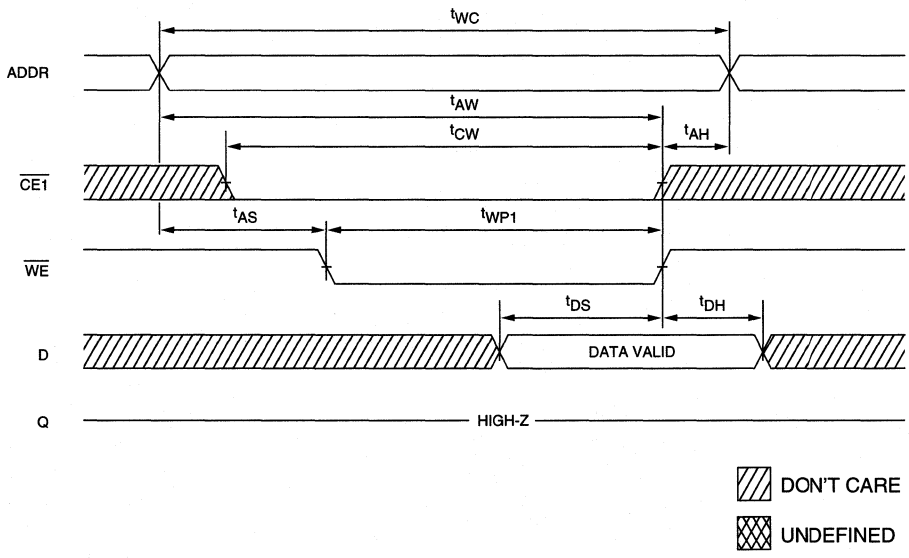
READ CYCLE NO. 2 [7, 8, 10, 12]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

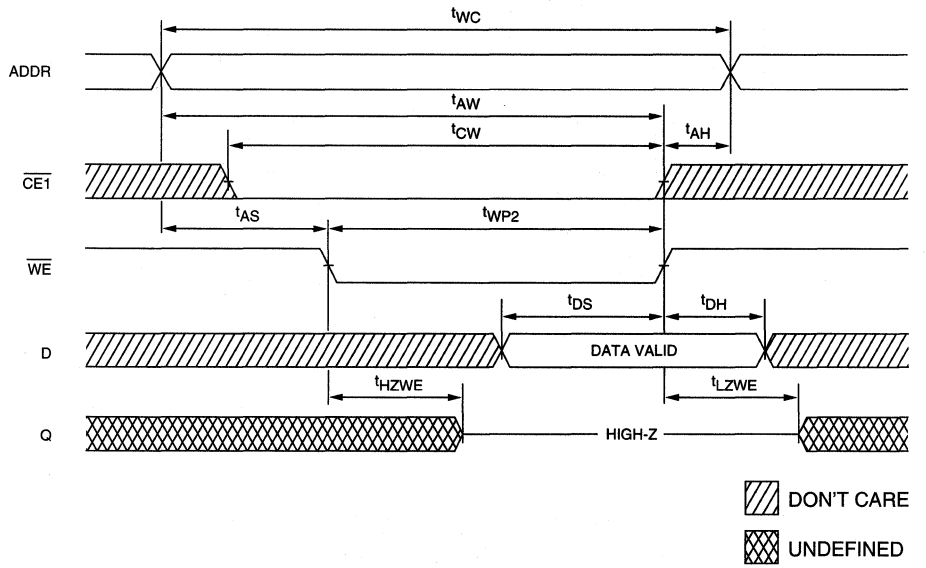


WRITE CYCLE NO. 2 [12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

128K x 8 SRAM

REVOLUTIONARY PINOUT, 3.3V
OPERATION WITH SINGLE CHIP ENABLE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12*, 15, 20 and 25ns
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Automatic $\overline{CE}$ power down
- All inputs and outputs are TTL-compatible
- High-performance, low-power, CMOS double-metal process
- Single 3.3V ±0.3V power supply
- Fast $\overline{OE}$ access times: 8, 10 and 12ns
- Complies to JEDEC low-voltage TTL-standards

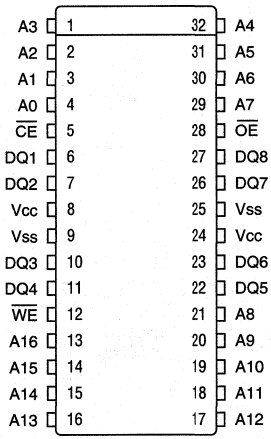
OPTIONS — MARKING

- Timing
  - 12ns access — -12*
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 32-pin SOJ (400 mil) — DJ
- 2V data retention (optional) — L
- Temperature
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT5LC128K8D4DJ-20 L

*Consult the factory for availability.

PIN ASSIGNMENT (Top View)

32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

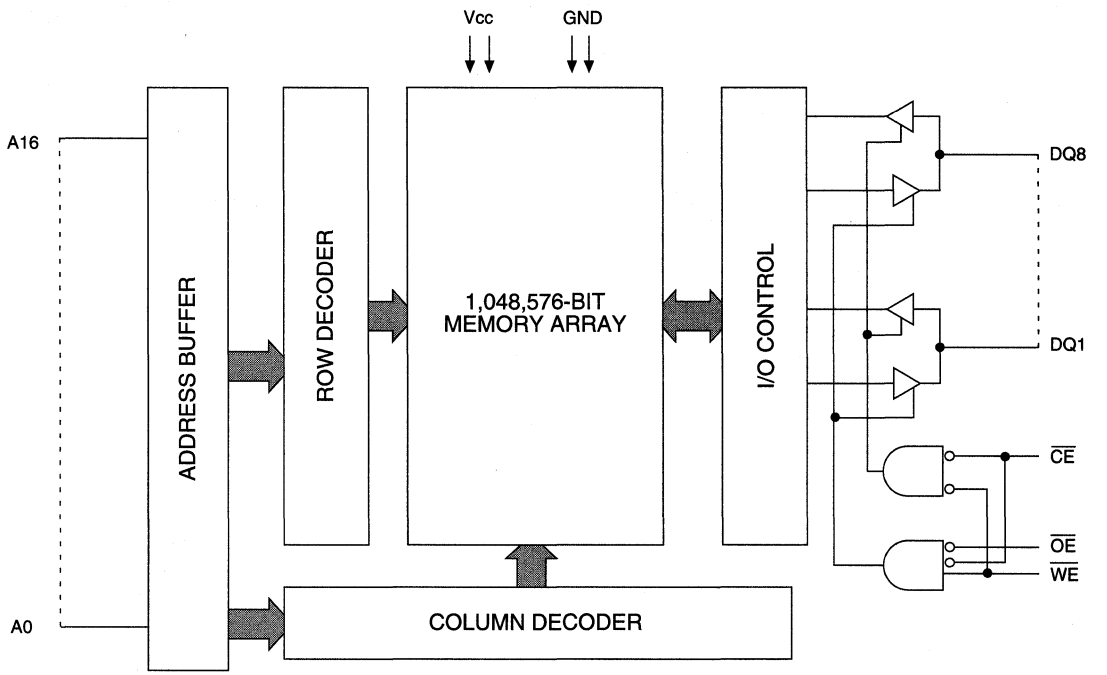
The MT5LC128K8D4 is organized as a 131,072 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. This enhancement can place the output in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and chip enable inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

PIN DESCRIPTIONS

SOJ AND TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
4, 3, 2, 1, 32, 31, 30, 29, 21, 20, 19, 18, 17, 16, 15, 14, 13	A0-A16	Input	Address Inputs: These inputs determine which cell is addressed.
12	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle.
5	$\overline{CE}$	Input	Chip Enable: This active LOW input is used to enable the device. When $\overline{CE}$ is HIGH, the chip is disabled and automatically goes into standby power mode.
28	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
6, 7, 10, 11, 22, 23, 26, 27	DQ1-DQ8	Input/ Output	SRAM Data I/O: Data inputs and tristate data outputs.
8, 24	V_{CC}	Supply	Power Supply: 3.3V ±0.3V
9, 25	V_{SS}	Supply	Ground: GND

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc =3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	165	280	230	180	160	mA	3, 15
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	35	60	50	40	35	mA	15
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	0.5	5	5	5	5	mA	15

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz V_{CC} =3.3V	C_I	5	pF	4
Output Capacitance		C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13, 15) (0°C ≤ T_A ≤ 70°C)

DESCRIPTION	SYM	-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	3		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	9		10		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	9		10		12		14		ns	
WRITE pulse width	$^tWP2$	10		10		12		14		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

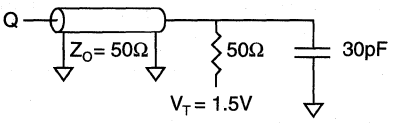


Fig. 1 OUTPUT LOAD EQUIVALENT

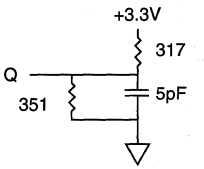


Fig. 2 OUTPUT LOAD EQUIVALENT

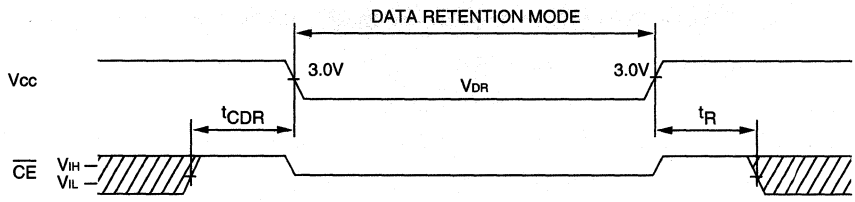
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded and $f = \frac{1}{{}^tRC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with C_L = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = read cycle time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. The output will be in the High-Z state if output enable is high.
14. Typical currents are measured at 25°C.
15. Typical values are measured at 3.3V, 25°C and 15ns cycle time.

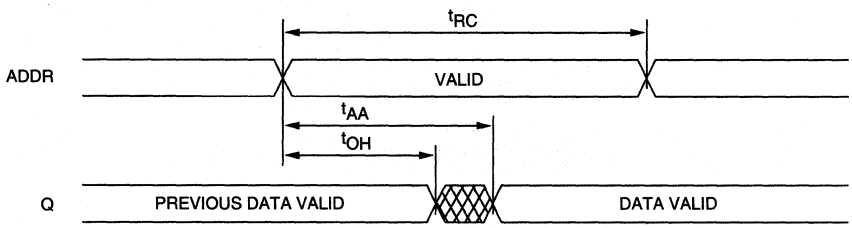
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq$ (Vcc -0.2V) $V_{IN} \geq$ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		70	300	µA	14
Chip Deselect to Data Retention Time			${}^tCDR$	0			ns	4
Operation Recovery Time			${}^tR$	${}^tRC$			ns	4, 11

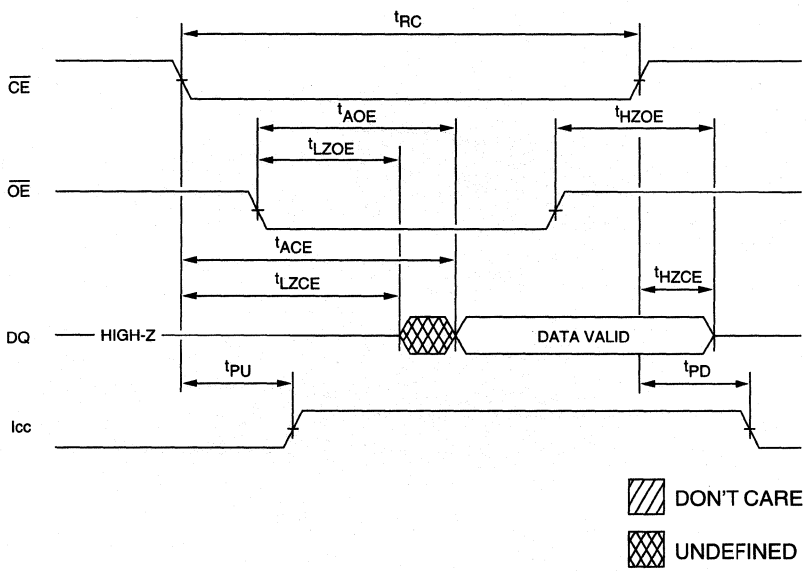
LOW Vcc DATA RETENTION WAVEFORM



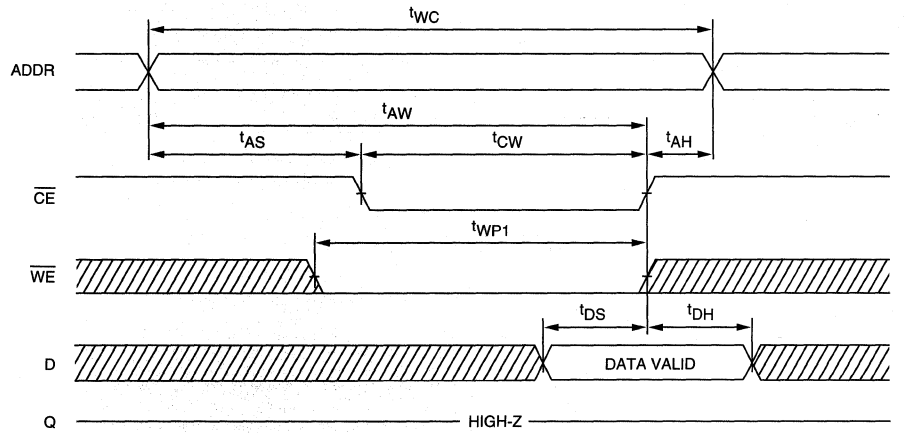
READ CYCLE NO. 1 [8, 9]



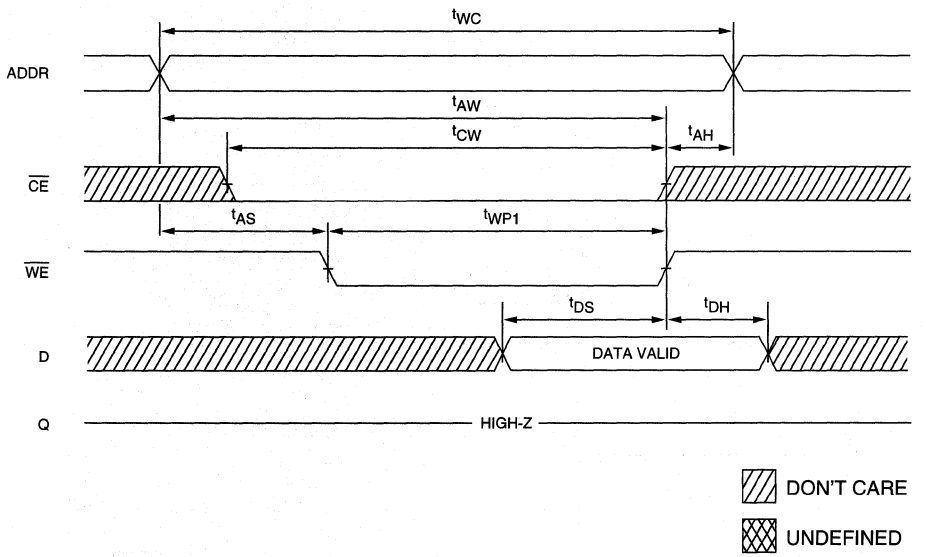
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

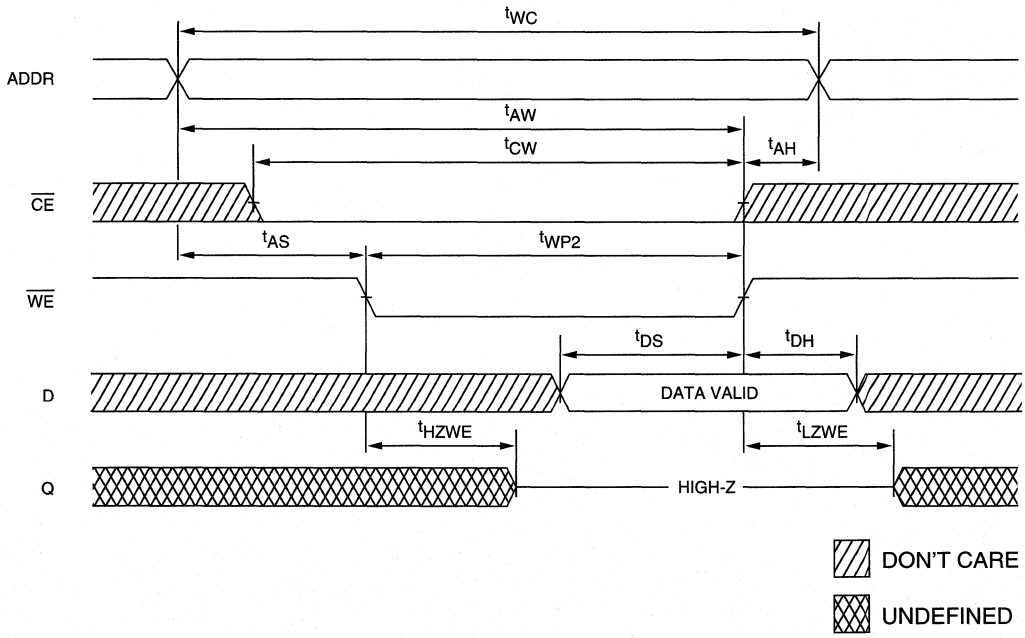


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

MICRON SEMICONDUCTOR INC

MT5LC128K8D4
REVOLUTIONARY PINOUT 128K x 8 SRAM

SRAM

512K x 8 SRAM

3.3V OPERATION WITH OUTPUT ENABLE, REVOLUTIONARY PINOUT

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 8, 10, 12 and 15ns
- Complies to JEDEC low-voltage TTL standards

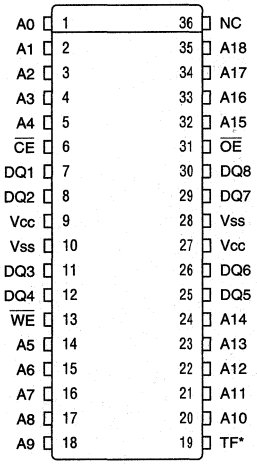
OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic SOJ (400 mil) — DJ
- 2V data retention (optional) — L
- Temperature
  - Commercial (0°C to +70°C) — None
- Part number example: MT5LC512K8D4DJ-20 L

NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

36-Pin SOJ
(SD-6)



* TF = Test Function. See note 14.

GENERAL DESCRIPTION

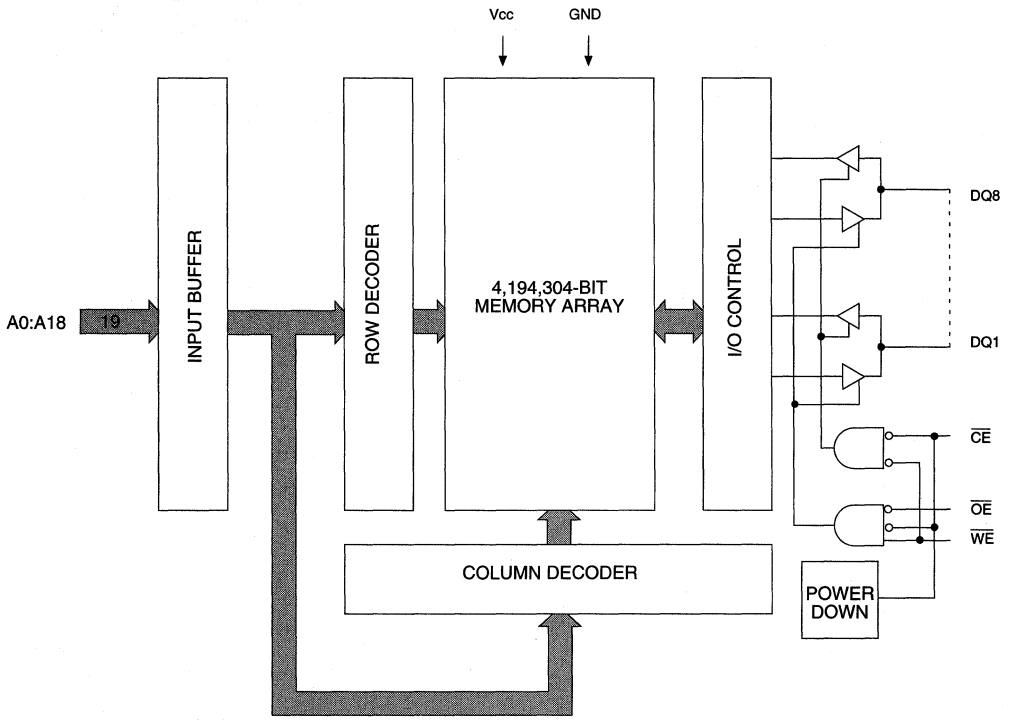
The MT5LC512K8D4 is organized as a 524,288 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using double-layer metal, triple-layer poly-silicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

THERMAL IMPEDANCE (estimated)

PACKAGE	NUMBER OF PINS	θ_{JC} (°C/W)	θ_{JA} (°C/W)	NOTES
SOJ	36	15	55	13, 15
TSOP	36	5	65	13, 15

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5 to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX outputs open f = MAX = $1/t_{RC}$	I_{CC}	185	165	160	155	145	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX outputs open f = MAX = $1/t_{RC}$	I_{SB1}	80	75	70	70	65	mA	
	$\overline{CE} \ge V_{CC}$ - 0.2V; V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le V_{SS}$ + 0.2V; f = 0	I_{SB2}	1.0	1.0	1.0	1.0	1.0	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	4
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	4
Output Enable access time	^tAOE		6		8		10		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		7		10		12	ns	6
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of write	^tCW	8		10		12		15		20		ns	
Address valid to end of write	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		10		12		15		20		ns	
WRITE pulse width	$^tWP2$	11		12		15		15		20		ns	
Data setup time	^tDS	6		7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

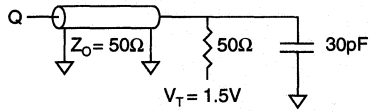


Fig. 1 OUTPUT LOAD EQUIVALENT

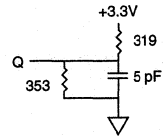


Fig. 2 OUTPUT LOAD EQUIVALENT

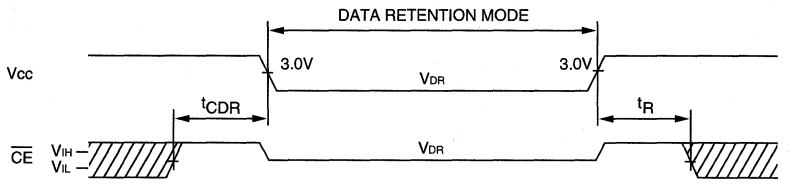
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.
14. The test function pin (TF) can be treated as a no connect pin. However, it is recommended that the pin be grounded.
15. The thermal impedance numbers assume the device is socketed on a PC board and air flow is zero.

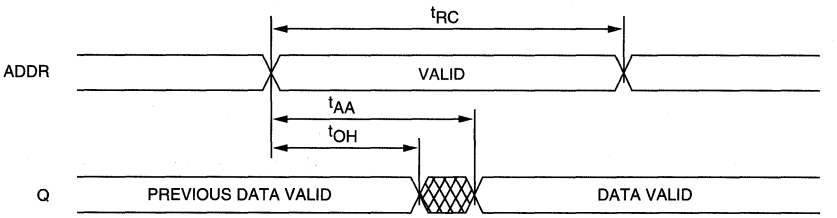
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2		V	
Data Retention Current	$\overline{CE} \geq (Vcc -0.2V)$ $V_{IN} \geq (Vcc -0.2V)$ or ≤ 0.2V Vcc = 2V	I_{CCDR}		700	µA	
Chip Deselect to Data Retention Time		${}^tCDR$	0		ns	4
Operation Recovery Time		${}^tR$	${}^tRC$		ns	4, 11

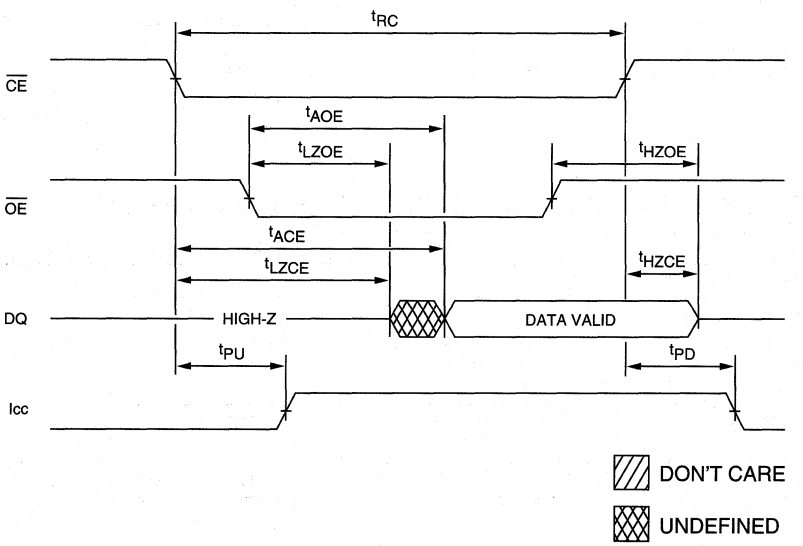
LOW Vcc DATA RETENTION WAVEFORM



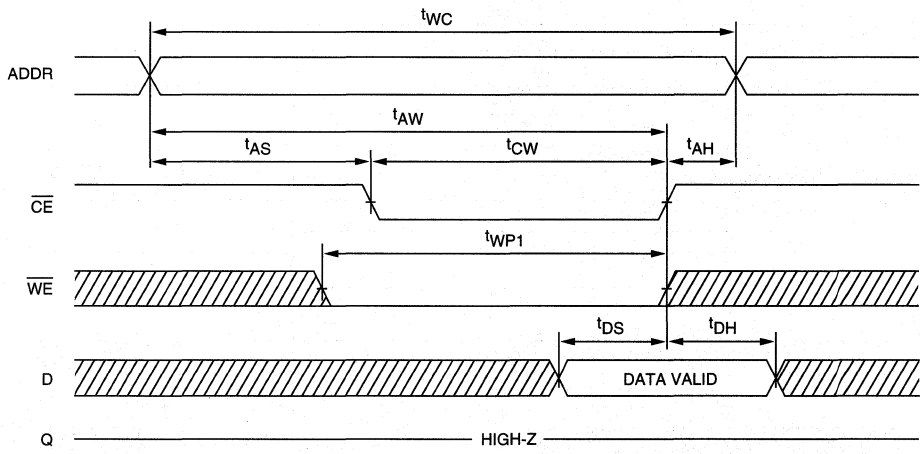
READ CYCLE NO. 1 [8, 9]



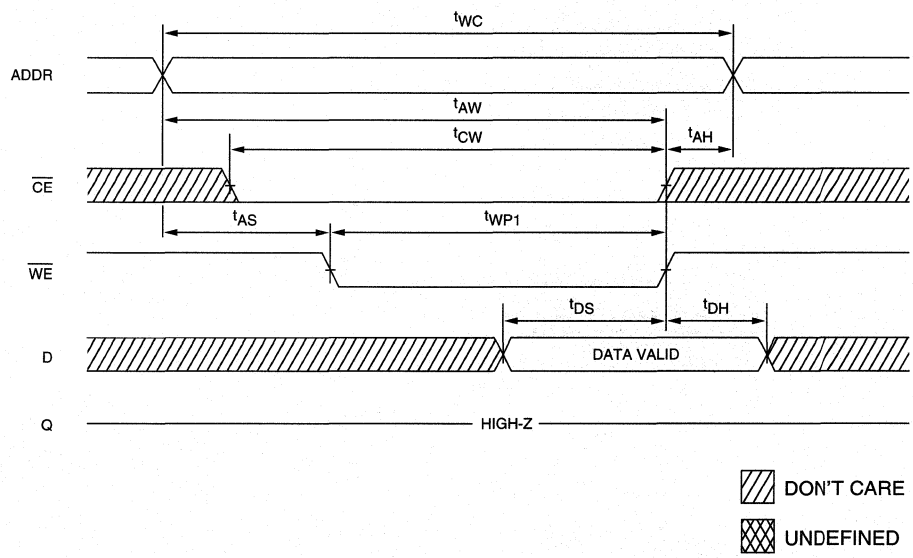
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

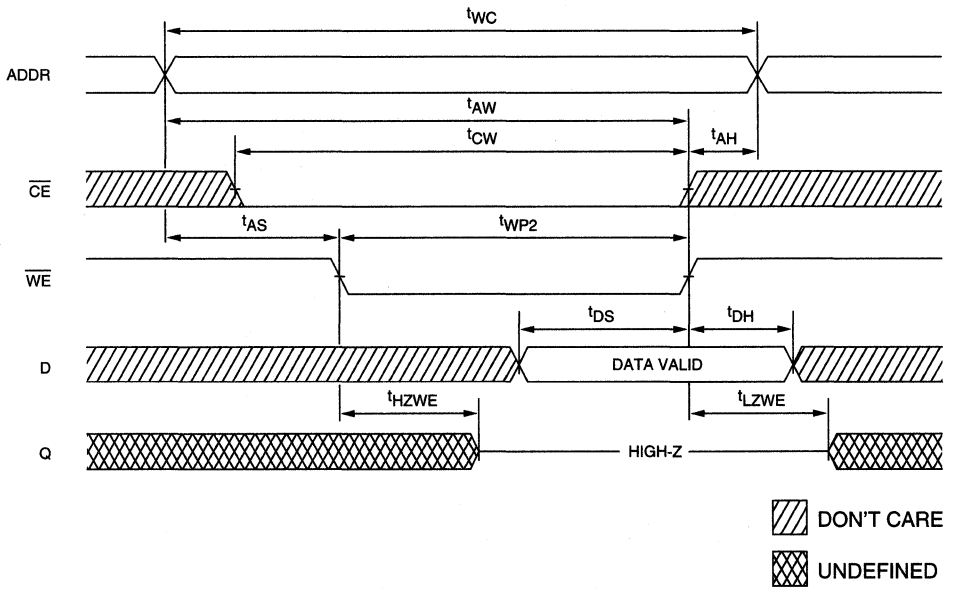


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM

64K x 16 SRAM

REVOLUTIONARY PINOUT 3.3V OPERATION WITH OUTPUT ENABLE

FEATURES

- All I/O pins are 5V tolerant
- Fast access times: 12*, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3Vpower supply
- Individual byte controls for both READ and WRITE cycles
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 8, 10 and 12ns
- Complies to JEDEC low-voltage TTL standards

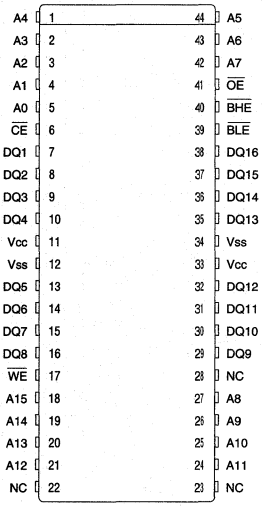
OPTIONS — MARKING

- Timing
  - 12ns access — -12*
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 44-pin SOJ (400 mil) — DJ
- 2V data retention (optional) — L
- Temperature
  - Commercial (0°C to +70°C) — None
- Part Number Example: MT5LC64K16D4DJ-20 L

*Consult the factory for availability.

PIN ASSIGNMENT (Top View)

44-Pin SOJ
(SD-7)



GENERAL DESCRIPTION

The MT5LC64K16D4 is organized as a 65,536 x 16 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

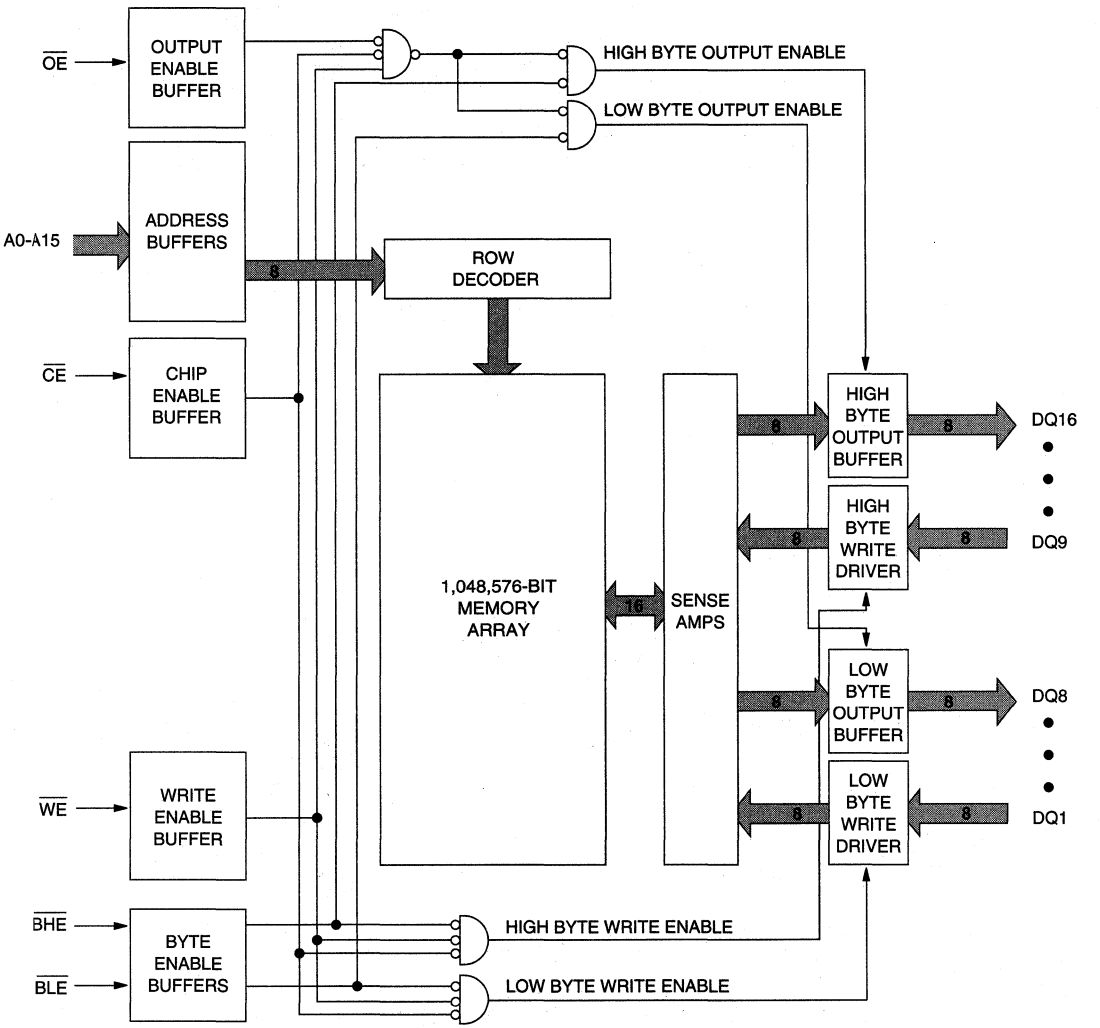
The MT5LC64K16D4 SRAM integrates a 64K x 16 SRAM core with peripheral circuitry consisting of active LOW chip enable, separate upper and lower byte enables and a fast output enable.

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be written and read. $\overline{BLE}$ controls DQ1-DQ8, the lower bits. $\overline{BHE}$ controls DQ9-DQ16, the upper bits.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

3.3V ASYNCHRONOUS SRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ and TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 1, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19, 18	A0-A15	Input	Address Inputs: These inputs determine which cell is accessed.
17	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
39, 40	$\overline{BLE}$, $\overline{BHE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written or read to the lower byte, DQ1-DQ8. When $\overline{BHE}$ is LOW, data is written or read to the upper byte, DQ9-DQ16.
6	$\overline{CE}$	Input	Chip Enable: This signal is used to enable the device. When $\overline{CE}$ is HIGH, the chip automatically goes into standby power mode.
41	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
22, 23, 28	NC	-	No Connect: These signals are not internally connected.
7, 8, 9, 10, 13, 14, 15, 16, 29, 30, 31, 32, 35, 36, 37, 38	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16.
11, 33	Vcc	Supply	Power Supply: +3.3V ±0.3V
12, 34	Vss	Supply	Ground: GND

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	DQ1-DQ8	DQ9-DQ16	POWER
STANDBY	H	X	X	X	X	HIGH-Z	HIGH-Z	STANDBY
LOW BYTE READ (DQ1-DQ8)	L	L	H	L	H	D	HIGH-Z	ACTIVE
HIGH BYTE READ (DQ9-DQ16)	L	L	H	H	L	HIGH-Z	D	ACTIVE
WORD READ (DQ1-DQ16)	L	L	H	L	L	D	D	ACTIVE
WORD WRITE (DQ1-DQ16)	L	X	L	L	L	Q	Q	ACTIVE
LOW BYTE WRITE (DQ1-DQ8)	L	X	L	L	H	Q	HIGH-Z	ACTIVE
HIGH BYTE WRITE (DQ9-DQ16)	L	X	L	H	L	HIGH-Z	Q	ACTIVE
OUTPUT DISABLE	L	H	H	X	X	HIGH-Z	HIGH-Z	ACTIVE
	L	X	X	H	H	HIGH-Z	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to 4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 3.3V \pm 0.3V$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	v	

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	165	280	230	180	160	mA	3, 15
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	32	60	50	40	35	mA	15
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.5	5	5	5	5	mA	15

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 3.3V	$C_{I/O}$	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13, 15) ($0°C \le T_A \le 70°C$)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	3		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	4		5		5		5		ns	6, 7
Chip disable to output in High-Z	^tHZCE		6		6		8		8	ns	6, 7
Output Enable access time	^tAOE		6		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE		6		6		8		8	ns	6, 7
Byte Enable access time	^tABE		6		8		10		12	ns	
Byte Enable to output in Low-Z	^tLZBE	0		0		0		0		ns	6, 7
Byte disable to output in High-Z	^tHZBE		6		6		8		8	ns	6, 7
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		13		15		ns	
Address valid to end of write	^tAW	9		10		12		14		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
Write pulse width	^tWP	9		10		12		14		ns	
Data setup time	^tDS	6		8		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		3		ns	6, 7
Write Enable to output in High-Z	^tHZWE		6		6		8		8	ns	6, 7
Byte Enable to end of write	^tBW	9		10		12		14		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

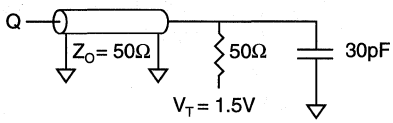


Fig. 1 OUTPUT LOAD EQUIVALENT

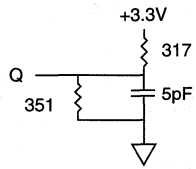


Fig. 2 OUTPUT LOAD EQUIVALENT

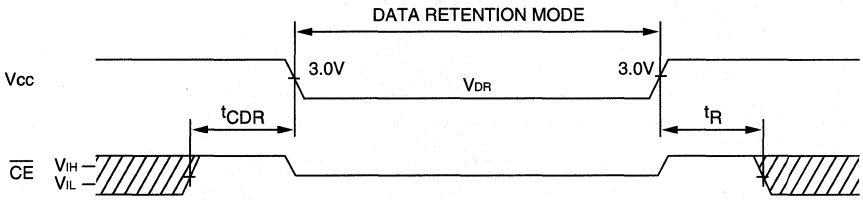
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded and $f = \frac{1}{{}^tRC\ (MIN)}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. Any combination of write enable, chip enable and byte enable can initiate and terminate a WRITE cycle.
9. $\overline{WE}$ is HIGH for READ cycle.
10. Device is continuously selected. Chip enable is held in its active state.
11. Address valid prior to, or coincident with, the latest occurring chip enable.
12. $\overline{BHE}$ and $\overline{BLE}$ are held in their active state (LOW).
13. The output will be in the High-Z state if output enable is HIGH.
14. Typical currents are measured at 25°C.
15. Typical values are measured at 3.3V, 25°C and 15ns cycle time.

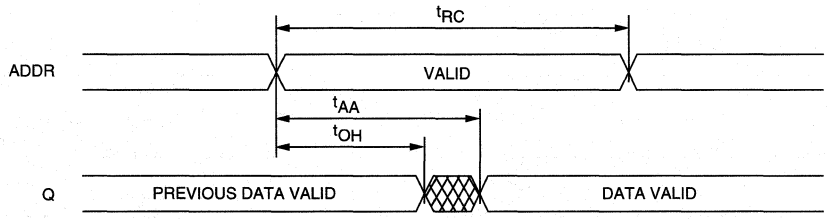
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq$ (Vcc -0.2V) $V_{IN} \geq$ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}		70	300	µA	14
Chip Deselect to Data Retention Time			${}^tCDR$	0			ns	4
Operation Recovery Time			${}^tR$	${}^tRC$			ns	4, 11

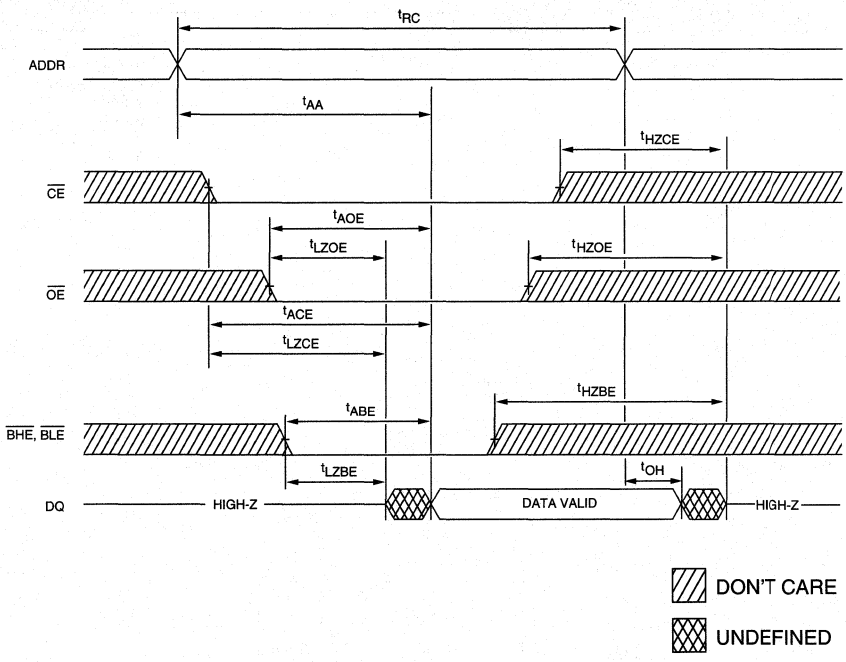
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [9, 10, 12]

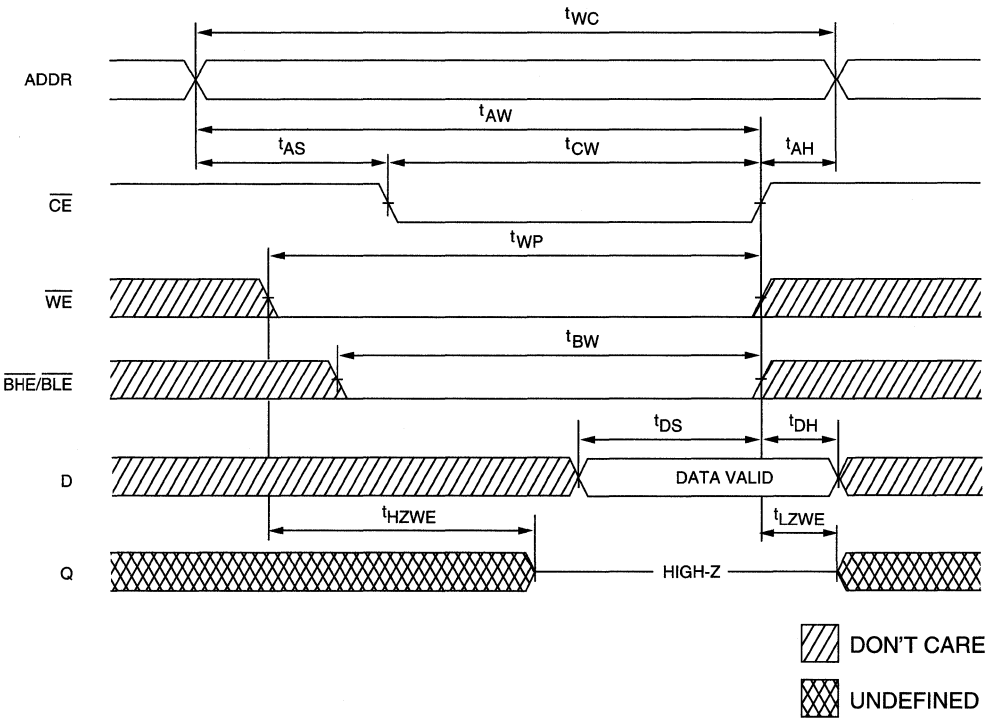


READ CYCLE NO. 2 [7, 9]



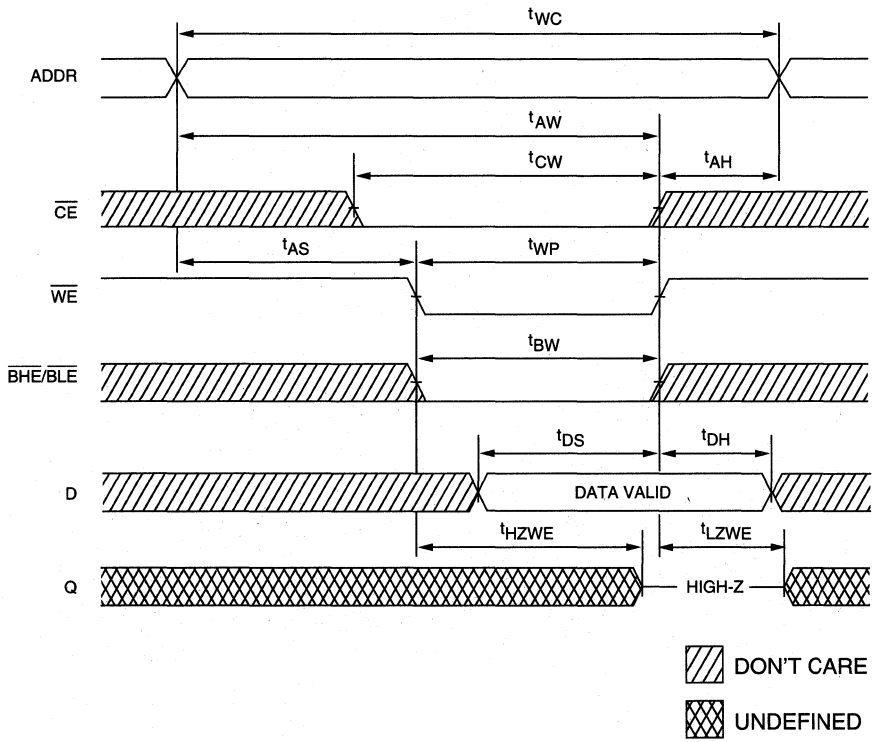
WRITE CYCLE NO. 1 [8, 13]

Chip Enable Controlled

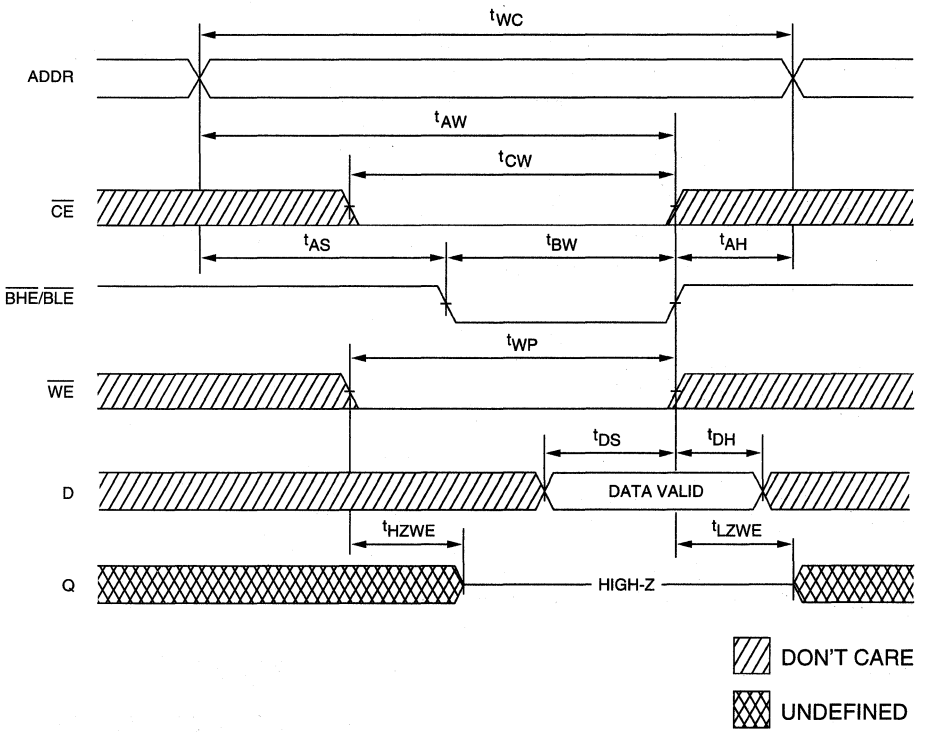


WRITE CYCLE NO. 2 [8, 13]

Write Enable Controlled



WRITE CYCLE NO. 3 [8, 13]
Byte Enable Controlled



SRAM

256K x 16 SRAM

3.3V OPERATION WITH OUTPUT ENABLE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3V power supply
- Easy memory expansion with chip enable($\overline{CE}$) and output enable ($\overline{OE}$) options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 8, 10, 12 and 15ns
- High-performance, low-power, CMOS double-metal process
- Complies to JEDEC low-voltage TTL standards

OPTIONS

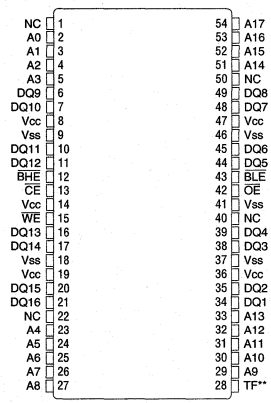
	MARKING
• Timing	
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25
35ns access	-35
• Packages	
Plastic SOJ (400 mil)	DJ
• 2V data retention (optional)	L
• Temperature	
Commercial (0°C to +70°C)	None

- Part number example: MT5LC256K16D4DJ-20 L

NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

54-Pin SOJ* (SD-8)



* JEDEC-proposed pinout (0.8mm pitch)
** TF = Test Function. See note 16.

GENERAL DESCRIPTION

The MT5LC256K16D4 is organized as a 262,144 x 16 using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using a double-layer metal, triple-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers $\overline{CE}$ and $\overline{OE}$ capabilities. These enhancements can place the outputs in High-Z for additional flexibility in system design.

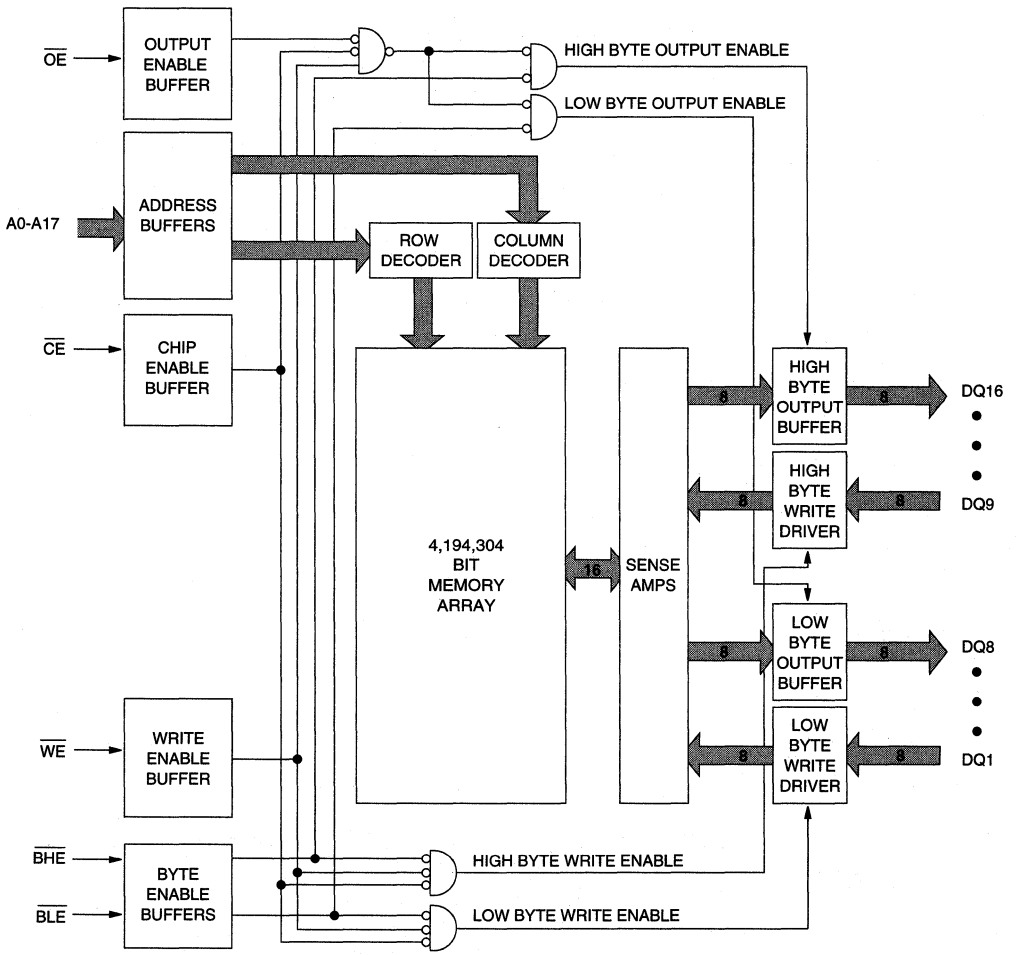
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW and the appropriate byte enables ($\overline{BHE}$ and $\overline{BLE}$) are in their proper states. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW and the appropriate byte enables ($\overline{BHE}$ and $\overline{BLE}$) are in their proper states. The device offers a reduced-power standby mode when disabled. This allows system designers to meet low standby power requirements.

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be written and read. $\overline{BLE}$ controls the lower bits (DQ1-DQ8). $\overline{BHE}$ controls the upper bits (DQ9-DQ16).

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible. These 3.3V devices are ideal for 3.3V-only and mixed 3.3V and 5V systems. All input pins and bidirectional pins are 5V-tolerant, meaning that 5V devices can directly drive these devices without increased current or any damaging effects. Refer to Technical Note TN-05-16 for further information.

3.3V ASYNCHRONOUS SRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ and TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2-5, 23-27, 29-33, 51-54	A0-A17	Input	Address Inputs: These inputs determine which cell is accessed.
15	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
12, 43	$\overline{BHE}$, $\overline{BLE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written to or read from the lower byte, D1-D8. When $\overline{BHE}$ is LOW, data is written to or read from the upper byte, D9-D16.
13	$\overline{CE}$	Input	Chip Enable: This signal is used to enable the device. When $\overline{CE}$ is HIGH, the chip goes into standby power mode.
42	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
28	TF	Test Pin	Test Function: This pin can be treated as a No Connect. However, it is recommended that this pin be connected to GND.
1, 22, 40, 50	NC	-	No Connect: These signals are not internally connected.
6, 7, 10, 11, 16, 17, 20, 21, 34, 35, 38, 39, 44, 45, 48, 49	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
8, 14, 19, 36, 47	Vcc	Supply	Power Supply: +3.3V ±0.3V
9, 18, 37, 41, 46	Vss	Supply	Ground: GND

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	DQ1-DQ8	DQ9-DQ16	POWER
STANDBY	H	X	X	X	X	HIGH-Z	HIGH-Z	STANDBY
LOW BYTE READ (DQ1-DQ8)	L	L	H	L	H	D	HIGH-Z	ACTIVE
HIGH BYTE READ (DQ9-DQ16)	L	L	H	H	L	HIGH-Z	D	ACTIVE
WORD READ (DQ1-DQ16)	L	L	H	L	L	D	D	ACTIVE
WORD WRITE (DQ1-DQ16)	L	X	L	L	L	Q	Q	ACTIVE
LOW BYTE WRITE (DQ1-DQ8)	L	X	L	L	H	Q	HIGH-Z	ACTIVE
HIGH BYTE WRITE (DQ9-DQ16)	L	X	L	H	L	HIGH-Z	Q	ACTIVE
OUTPUT DISABLE	L	H	H	X	X	HIGH-Z	HIGH-Z	ACTIVE
	L	X	X	H	H	HIGH -Z	HIGH-Z	ACTIVE

THERMAL IMPEDANCE (estimated)

PACKAGE	NUMBER OF PINS	θ_{JC} (°C/W)	θ_{JA} (°C/W)	NOTES
SOJ	54	15	55	15, 17
TSOP	54	5	65	15, 17

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... 0.5V to +4.6V
V_{IN} ..... -0.5 to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Short Circuit Output Current 50mA
Junction Temperature** ..... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this data sheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

			MAX						
DESCRIPTION	CONDITIONS	SYMBOL	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	200	180	170	160	150	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	80	75	70	70	65	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	1.0	1.0	1.0	1.0	1.0	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 15) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	SYM	-12		-15		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle													
READ cycle time	^tRC	12		15		20		25		35		ns	
Address access time	^tAA		12		15		20		25		35	ns	
Chip Enable access time	^tACE		12		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		0		ns	4
Chip disable to power-down time	^tPD		12		15		20		25		35	ns	4
Output Enable access time	^tAOE		6		8		10		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		7		10		12	ns	6
Byte Enable access time	^tABE		7		8		10		12		15	ns	
Byte Enable to output in Low-Z	^tLZBE	0		0		0		0		0		ns	
Byte Enable to output in High-Z	^tHZBE		7		8		8		8		10	ns	
WRITE Cycle													
WRITE cycle time	^tWC	12		15		20		25		35		ns	
Chip Enable to end of WRITE	^tCW	8		10		12		15		20		ns	
Address valid to end of WRITE	^tAW	8		10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		0		ns	
Address hold from end of WRITE	^tAH	0		0		0		0		0		ns	
WRITE pulse width	$^tWP1$	8		10		12		15		20		ns	
WRITE pulse width	$^tWP2$	11		12		15		15		20		ns	
Data setup time	^tDS	6		7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		5		6		8		10		15	ns	6, 7
Byte Enable to end of WRITE	^tBW	8		9		12		14		18		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

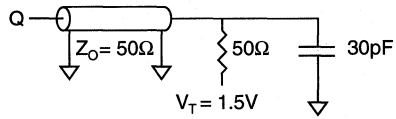


Fig. 1 OUTPUT LOAD EQUIVALENT

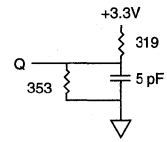


Fig. 2 OUTPUT LOAD EQUIVALENT

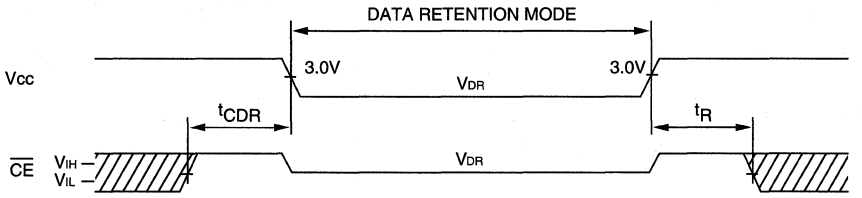
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \le +6.0V$ for $t \le {}^tRC/2$
   Undershoot: $V_{IL} \ge -2.0V$ for $t \le {}^tRC/2$
   Power-up: $V_{IH} \le +6.0V$ and $V_{CC} \le 3.1V$ for $t \le 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$, ${}^tHZBE$ and ${}^tHZWE$ are specified with C_L = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = READ cycle time.
12. Chip enable, write enable and byte enables can initiate and terminate a WRITE cycle.
13. $\overline{BLE}$ and $\overline{BLH}$ determine what outputs are active during the READ cycle.
14. The output will be in a High-Z state if $\overline{OE}$ is HIGH.
15. Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.
16. The test function pin (TF) can be treated as a no connect pin. However, it is recommended that the pin be grounded.
17. The thermal impedance numbers assume the device is socketed on a PC board and air flow is zero.

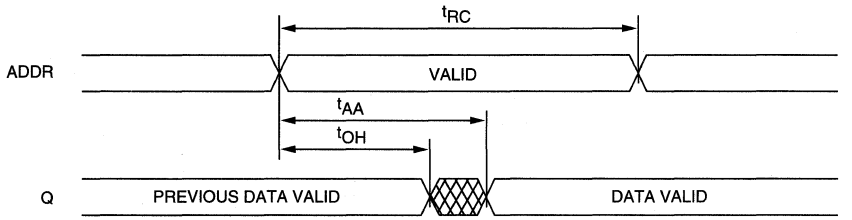
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2		V	
Data Retention Current	$\overline{CE} \ge$ (Vcc -0.2V) $V_{IN} \ge$ (Vcc -0.2V) or ≤ 0.2V Vcc = 2V	I_{CCDR}		700	µA	
Chip Deselect to Data Retention Time		${}^tCDR$	0		ns	4
Operation Recovery Time		${}^tR$	${}^tRC$		ns	4, 11

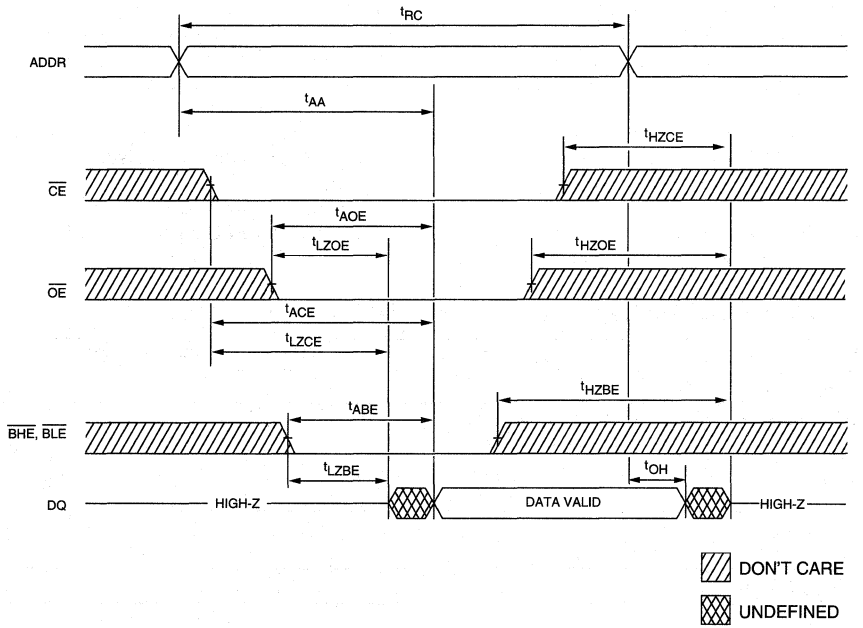
LOW Vcc DATA RETENTION WAVEFORM



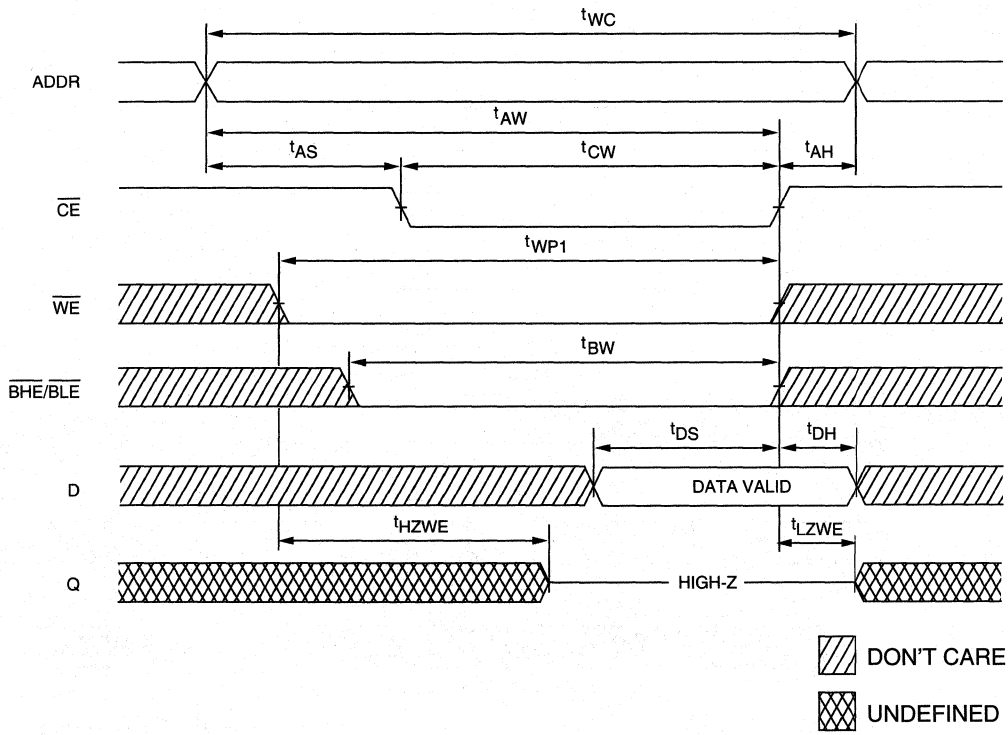
READ CYCLE NO. 1 [8, 9, 13]



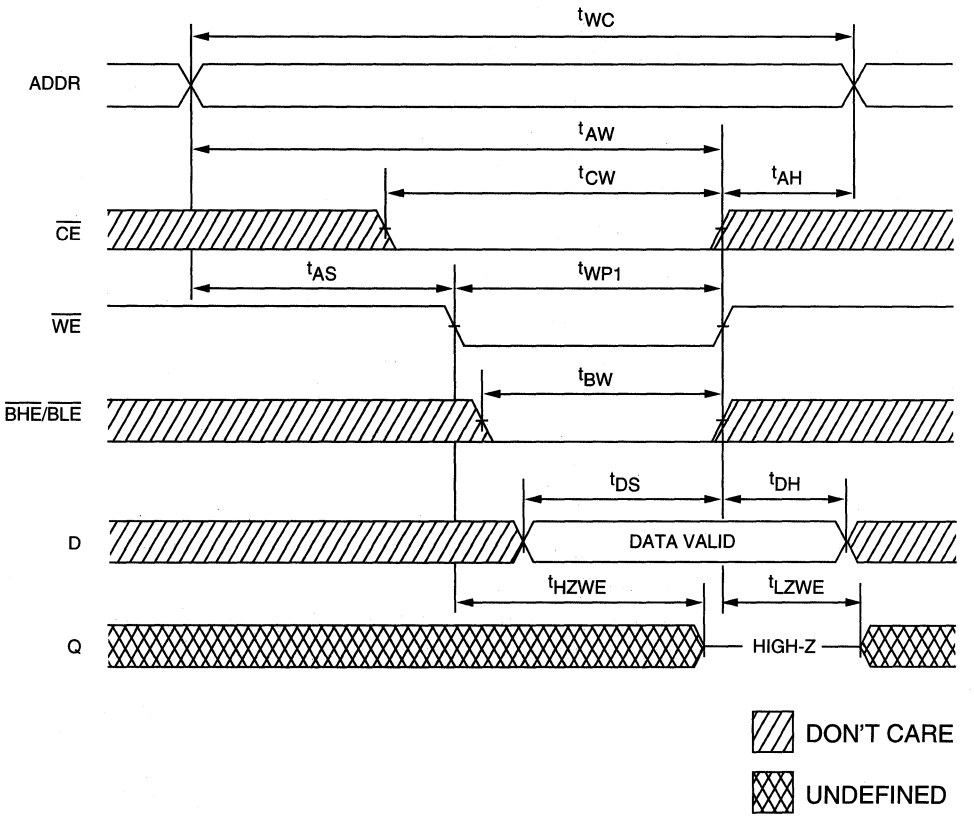
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12,14]
(Chip Enable Controlled)

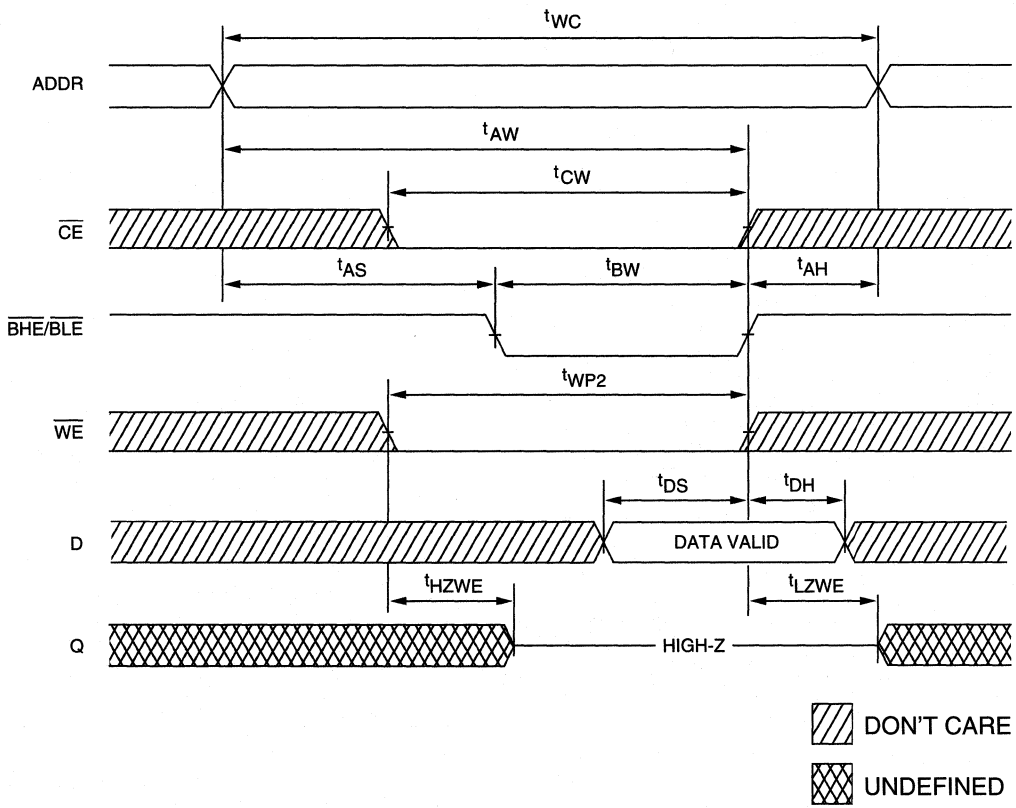


WRITE CYCLE NO. 2 [7, 12, 14]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 14]
(Byte Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

APPLICATION INFORMATION

THERMAL CONSIDERATIONS

This section describes how to determine the junction temperature during operating conditions. It is essential that the maximum junction temperature of the 4 Meg SRAM is not exceeded. If this temperature is exceeded it is necessary to add external cooling such as forced airflow or change the operating conditions. The maximum junction temperature for Micron SRAMs is 150°C. The limiting temperature factor is not the SRAM but the mold compound which prevents reliable operating temperatures significantly about 150°C. However, it is advisable to run the part as cool as possible since reliability (FIT rates) are exponentially dependent upon junction temperature.

The calculation of the actual junction temperature begins with a power calculation followed by a junction temperature calculation. Equations 1 and 2 below show how T_j is determined using the ambient temperature, thermal resistance and operating power. If an airflow is introduced into a system then Equation 2 should be used with an airflow thermal multiplier. Specific thermal resistances are given in Micron technical note "SRAM Thermal Design Considerations" (TN-05-14) and in individual data sheets.

$$T_j = T_A + P * \theta_{JA} \quad (1)$$

$$T_j = T_A + P * \theta_{JA} * \theta_M \quad (2)$$

T_j = Junction temperature of the active portion of the silicon die (°C)
T_A = Ambient air temperature (°C) at which the device is operated
P = Average power dissipation of the device (W)
θ_{JA} = Junction to ambient thermal resistance (°C/W)
θ_M = Airflow multiplier. This value changes for different values of airflow over the part (fpm).

To solve the above equations the average operating power must be calculated. Total power has three separate components (P_1, P_2 and P_3). P_1 is the operating power dissipated by the chip, P_2 is the AC output power due to the capacitive load and P_3 is the DC output power due to TTL DC load current (P_3 is usually negligible). For this example we have chosen P_2 such that outputs are switching from a logic LOW state to a logic HIGH state which gives the worst case output AC current. A complete description of these equations and their derivation is given in Micron technical note (TN-58-02) "Design Tips: 32K x 36 Synchronous SRAM."

$$P_1 = Vcc\ Icc$$

$$P_2 = \frac{C_L}{T} (Vcc [V_{OH} - V_{OL}] - 0.5 [V_{OH}^2 - V_{OL}^2]) N_S$$

$$P_3 = (Vcc - V_{OH})\ I_O\ N_H + V_{OL}\ I_I\ N_L.$$

Vcc = Supply voltage
Icc = Supply current
C_L = Capacitive output loading
T = Clock period
V_{OH} = Output high voltage
V_{OL} = Output low voltage
I_O = Output current on DQ lines which are high
I_I = Input current on DQ lines which are low
N_H = Number of DQ lines which are high
N_L = Number of DQ lines which are low.

Table 1
EFFECTS OF AIRFLOW ON 4 MEG SRAM SOJ PACKAGES

Package	Air Flow	θ_M Multiplier
PSOJ	200 fpm	0.7 - 0.75
PSOJ	500 fpm	0.55 - 0.65

ADDITIONAL INFORMATION

For more information on thermal considerations see Micron's technical notes, "SRAM Thermal Design Considerations" and "Design Tips: 32K x 36 Synchronous SRAM." These notes explain how to calculate thermal resistance and how to improve thermal performance in much greater detail. Also available is Micron's *Quality and Reliability Handbook*, which gives an explanation of how thermal impedances are calculated.

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SYNCHRONOUS SRAM PRODUCT SELECTION GUIDE

Memory Configuration	Supply Voltage	Control Functions	Part Number	Access Time (ns)	Cycle Time (ns)	Package and Number of Pins			Page
						PLCC	TQFP	DIE	
64K x 18	3.3V	SyncBurst™, Interleaved, Linear	MT58LC64K18B2	9,10,11,12,14	15,15,15,20,20	52	100	CD1/CD2	3-1
64K x 18	3.3V	SyncBurst, Linear	MT58LC64K18M1	9,10,11,12,14	15,15,15,20,20	52	100	CD1/CD2	3-1
64K x 18	3.3V	SyncBurst, Interleaved, Linear	MT58LC64K18C4	4.5,5,6,7,8	8,10,12,15,20	52	100	CD1/CD2	3-17
64K x 18	3.3V	SyncBurst, Linear	MT58LC64K18A6	4.5,5,6,7,8	8,10,12,15,20	52	100	CD1/CD2	3-17
32K x 32	3.3V	SyncBurst	MT58LC32K32B2	9,10,11,12,14	15,15,15,20,20	-	100	CD1/CD2	3-33
32K x 32	3.3V	SyncBurst, Interleaved Burst, Pipelined	MT58LC32K32C4	4.5,5,6,7,8	8,10,12,15,20	-	100	CD1/CD2	3-49
32K x 36	3.3V	SyncBurst, Interleaved Burst	MT58LC32K36B2	9,10,11,12,14	15,15,15,20,20	-	100	CD1/CD2	3-65
32K x 36	3.3V	SyncBurst, Interleaved Burst, Pipelined	MT58LC32K36C4	4.5,5,6,7,8	8,10,12,15,20	-	100	CD1/CD2	3-81

NOTE: 1. Many Micron components are available in bare die form. Contact Micron Semiconductor, Inc., for more information.

SYNCHRONOUS SRAM

64K x 18 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS, BURST COUNTER

FEATURES

- Fast access times: 9, 10, 11, 12 and 14ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Burst control pins (interleaved or linear burst sequence)
- Automatic power-down for portable applications
- High density, high speed packages
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- DIMMs also available

OPTIONS — MARKING

- Timing
  - 9ns access/15ns cycle — -9
  - 10ns access/15ns cycle — -10
  - 11ns access/15ns cycle — -11
  - 12ns access/20ns cycle — -12
  - 14ns access/20ns cycle — -14
- Packages
  - 52-pin PLCC — EJ
  - 100-pin TQFP — LG
- Low power — P
- 2V data retention, low power — L

Part Number Examples

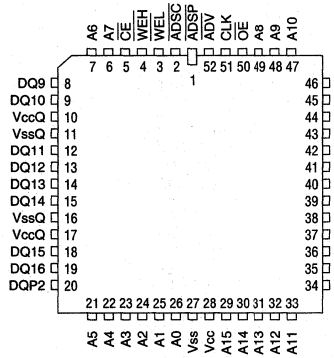
BASE PART NO.	VERSION SUFFIX	PACKAGE	BURST SEQUENCE
MT58LC64K18	M1	EJ	Linear
MT58LC64K18	B2	EJ	Interleaved
MT58LC64K18	B2	LG	Interleaved (Mode = NC) Linear (Mode = GND)

GENERAL DESCRIPTION

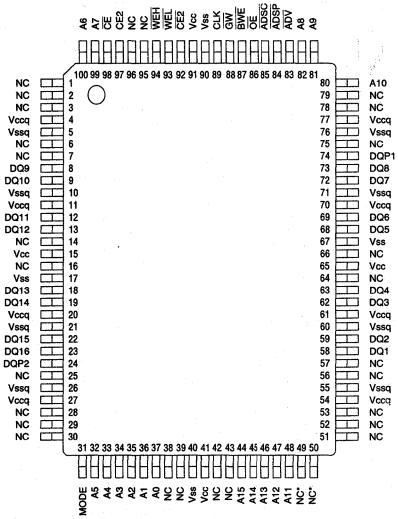
The Micron SyncBurst™ SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

PIN ASSIGNMENT (Top View)

52-Pin PLCC (SB-1)



100-Pin TQFP (SC-1)



*Pin 49 is reserved for A16, pin 50 for A17

SYNCHRONOUS SRAM

GENERAL DESCRIPTION (continued)

The MT58LC64K18B2/M1 SRAM integrates a 64K x 18 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion ($\overline{CE2}$, CE2), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$), byte write enables ($\overline{WEH}$, $\overline{WEL}$, $\overline{BWE}$), and global write ($\overline{GW}$).

Asynchronous inputs include the output enable ($\overline{OE}$), clock (CLK) and burst mode (MODE). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to two bytes wide as controlled by the write control inputs.

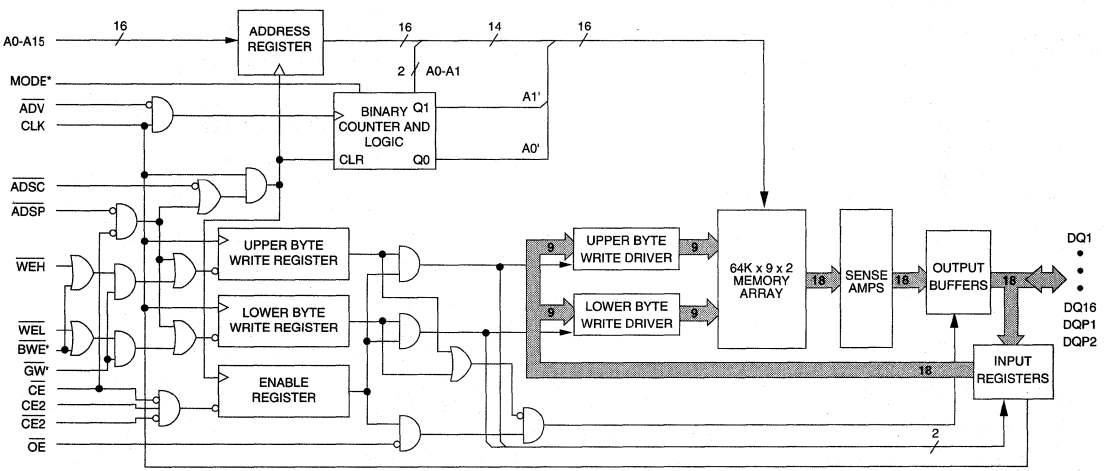
Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{WEL}$ controls DQ1-DQ8 and DQP1. $\overline{WEH}$ controls DQ9-DQ16 and DQP2, conditioned by $\overline{BWE}$ being LOW. $\overline{GW}$ LOW causes all bytes to be written.

The "L" version of this device has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below V_{CC} MIN (3.1V), it will retain data with a minimum of power dissipation.

The MT58LC64K18B2/M1 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V-tolerant. The device is ideally suited for 486, Pentium™, 680x0 and PowerPC™ systems and those systems which benefit from a wide synchronous data bus.

FUNCTIONAL BLOCK DIAGRAM



*LG package only

NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

BURST ADDRESS TABLE (MODE = NC or MT58LC64K18B2 EJ device)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

BURST ADDRESS TABLE (MODE = GND or MT58LC64K18M1 EJ device)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PIN DESCRIPTIONS

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
26, 25, 24, 23, 22, 21, 7, 6, 49, 48, 47, 33, 32, 31, 30, 29	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 80, 48, 47, 46, 45, 44	A0-A15	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
4, 3	94, 93	$\overline{WEH}$, $\overline{WEL}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{WEL}$ controls DQ1-DQ8 and DQP1. $\overline{WEH}$ controls DQ9-DQ16 and DQP2. Data I/O are tristated if either of these inputs are LOW.
n/a	87	$\overline{BWE}$	Input	Byte Write Enable: This active LOW input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
n/a	88	$\overline{GW}$	Input	Global Write: This active LOW input allows a full 18-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{WEn}$ lines and must meet the setup and hold times around the rising edge of CLK.
51	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
5	98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
n/a	92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded.

PIN DESCRIPTIONS (continued)

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
n/a	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded.
50	86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
52	83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
1	84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon $\overline{CE}$ being LOW.
2	85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if $\overline{CE}$ is LOW. $\overline{ADSC}$ is also used to place the chip into power-down state when $\overline{CE}$ is HIGH.
n/a	31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1-DQ16	Input/ Output	SRAM Data I/O: Low Byte is DQ1-DQ8. High Byte is DQ9-DQ16. Input data must meet setup and hold times around the rising edge of CLK.
46, 20	74, 24	DQP1, DQP2	Input/ Output	Parity Data I/O: Low Byte Parity is DQP1. High Byte Parity is DQP2.
28	15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
27	17, 40, 67, 90	Vss	Supply	Ground: GND
10, 17, 36, 43	4, 11, 20, 28, 54, 77, 61, 70	Vccq	Supply	Isolated Output Buffer Supply: +3.3V ±5%
11, 16, 37, 42	6, 10, 21, 26, 60, 55, 71, 76	Vssq	Supply	Isolated Output Buffer Ground: GND
	1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 43,49, 50, 51, 52, 53, 56, 57, 64, 66, 75, 78, 79, 95, 96	NC	-	No Connect: These signals are not internally connected. These signals may be connected to ground to improve package heat dissipation.

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{WEH}$, $\overline{WEL}$, and $\overline{BWE}$) are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$=H means all byte write enable signals and $\overline{GW}$ are HIGH.
2. $\overline{WEL}$ enables writes to DQ1-DQ8 and DQP1. $\overline{WEH}$ enables writes to DQ9-DQ16 and DQP2.
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signal and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE FOR WRITEs

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{WEL}$	$\overline{WEH}$
READ	H	H	X	X
READ	H	L	H	H
WRITE LOW Byte	H	L	L	H
WRITE HIGH Byte	H	L	H	L
WRITE all bytes	H	L	L	L
WRITE all bytes	L	X	X	X

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +150°C
Junction Temperature** ..... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	14
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1, 11
Supply Voltage		V_{CC}	3.1	3.5	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYM	TYP	VER	-9	-10	-11	-12	-14	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; Vcc = MAX; outputs open	I_{CC}	175	ALL	250	250	225	200	200	mA	3, 12 13
Power Supply Current: Idle	Device selected; Vcc = MAX; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, $\overline{GW}$, $\overline{BW}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; cycle time ≥ ^tKC MIN; outputs open	I_{CC1}	28	ALL	45	45	45	40	40	mA	12, 13
CMOS Standby	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.5	STD	5	5	5	5	5	mA	12, 13
			0.2	P	2	2	2	2	2	mA	
TTL Standby	Device deselected; Vcc = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB3}	15	STD	25	25	25	25	25	mA	12, 13
			10	P	18	18	18	18	18	mA	
Clock Running	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB4}	30	ALL	50	50	50	45	45	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	V_{CC} = 3.3V	C_O	6	7	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	PLCC TYP	TQFP TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still air, soldered on 4.25 x 1.125 inch 4-layer PCB	θ_{JA}	45	20	°C/W	
Thermal resistance - Junction to Case		θ_{JC}	15	1	°C/W	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±5%)

DESCRIPTION		-9		-10		-11		-12		-14			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock													
Clock cycle time	tKC	15		15		15		20		20		ns	
Clock HIGH time	tKH	4		5		5		6		6		ns	
Clock LOW time	tKL	4		5		5		6		6		ns	
Output Times													
Clock to output valid	tKQ		9		10		11		12		14	ns	
Clock to output invalid	tKQX	3		3		3		3		3		ns	
Clock to output in Low-Z	tKQLZ	5		5		5		5		5		ns	6, 7
Clock to output in High-Z	tKQHZ		5		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	tOEQ		5		5		5		6		6	ns	9
$\overline{OE}$ to output in Low-Z	tOELZ	0		0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	tOEHZ		5		5		5		6		6	ns	6, 7
Setup Times													
Address	tAS	2.5		2.5		2.5		3		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	tADSS	2.5		3		3		3		3		ns	8, 10
Address Advance ($\overline{ADV}$)	tAAS	2.5		3		3		3		3		ns	8, 10
Byte Write Enables ($\overline{WEH}$, $\overline{WEL}$, $\overline{GW}$, $\overline{BWE}$)	tWS	2.5		3		3		3		3		ns	8, 10
Data-in	tDS	2.5		3		3		3		3		ns	8, 10
Chip Enable ($\overline{CE}$)	tCES	2.5		3		3		3		3		ns	8, 10
Hold Times													
Address	tAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	tADSH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	tAAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{WEH}$, $\overline{WEL}$, $\overline{GW}$, $\overline{BWE}$)	tWH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Data-in	tDH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Chip Enable ($\overline{CE}$)	tCEH	0.5		0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

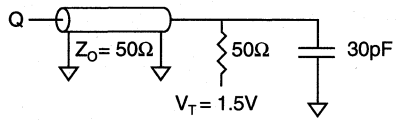


Fig. 1 OUTPUT LOAD EQUIVALENT

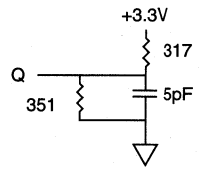


Fig. 2 OUTPUT LOAD EQUIVALENT

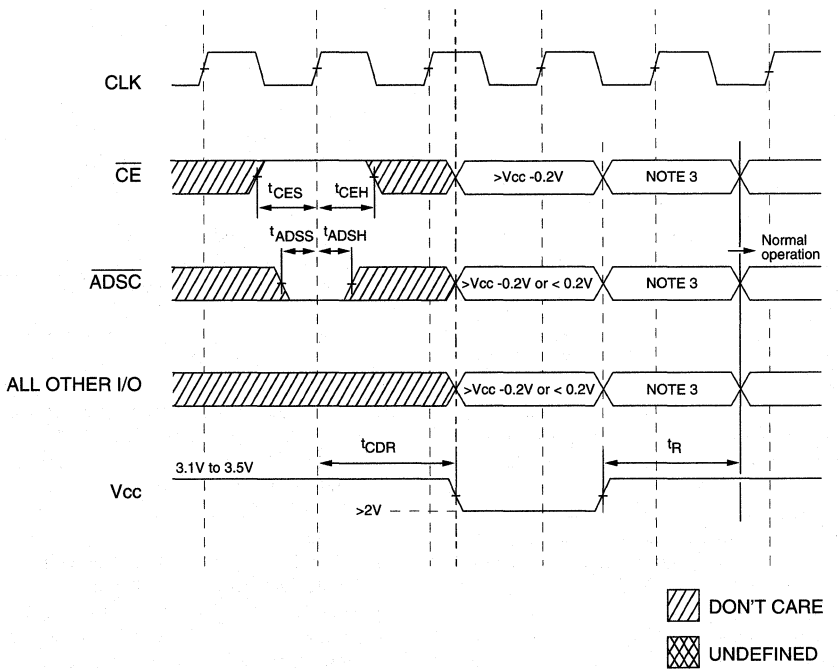
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte Write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the stated DC values. AC I/O curves are available upon request.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
15. Typical values are measured at 25°C.
16. The device must have a deselect cycle applied at least one clock cycle before data retention mode is entered.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

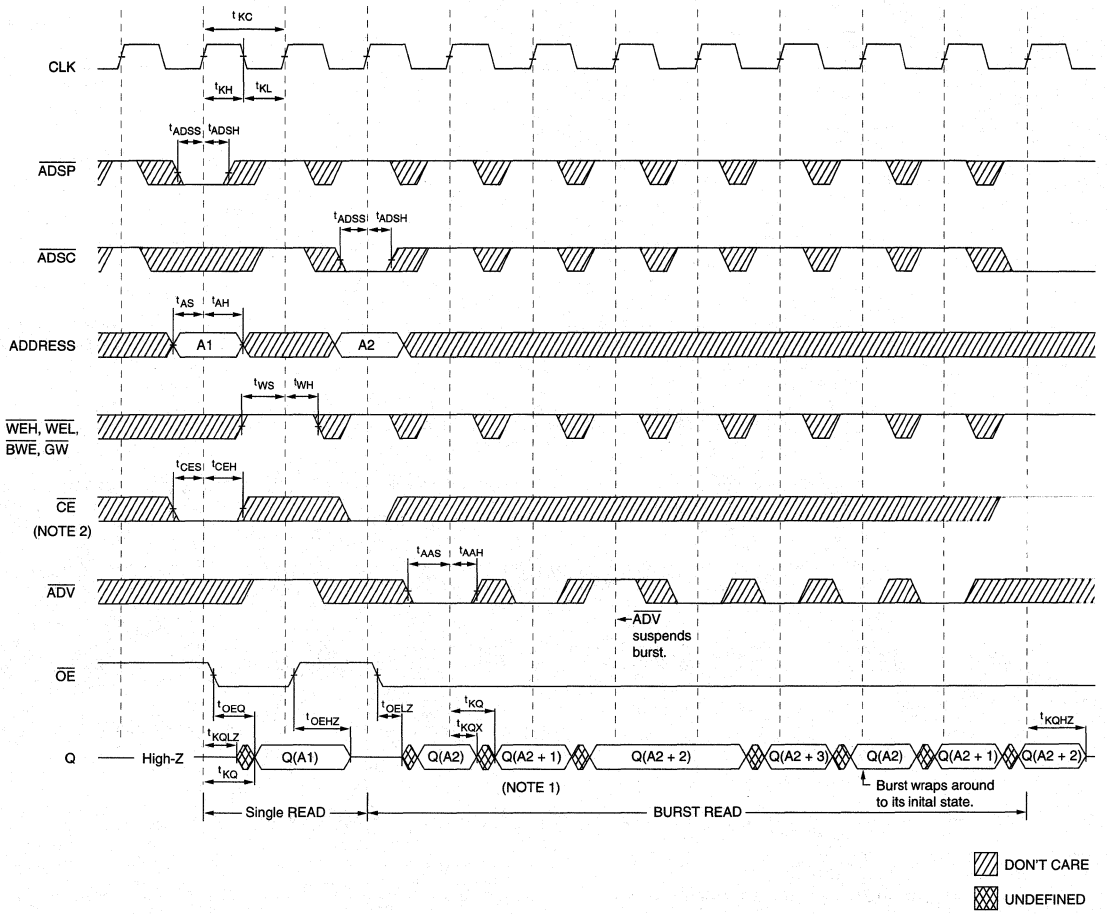
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2} \geq (V_{CC} - 0.2V)$, $CE2 \leq 0.2V$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$ $V_{CC} = 2V$	I_{CCDR}		TBD	µA	15
Chip Deselect to Data Retention Time		^tCDR	^tKC		ns	4, 16
Operation Recovery Time		^tR	^tKC		ns	4

LOW V_{CC} DATA RETENTION WAVEFORM



NOTE:
1. All inputs must be ≥ Vcc - 0.2V or ≤ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded.
2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.
3. The device control signals should be in a deselect state between the rising edge of Vcc and until ^tR is met.

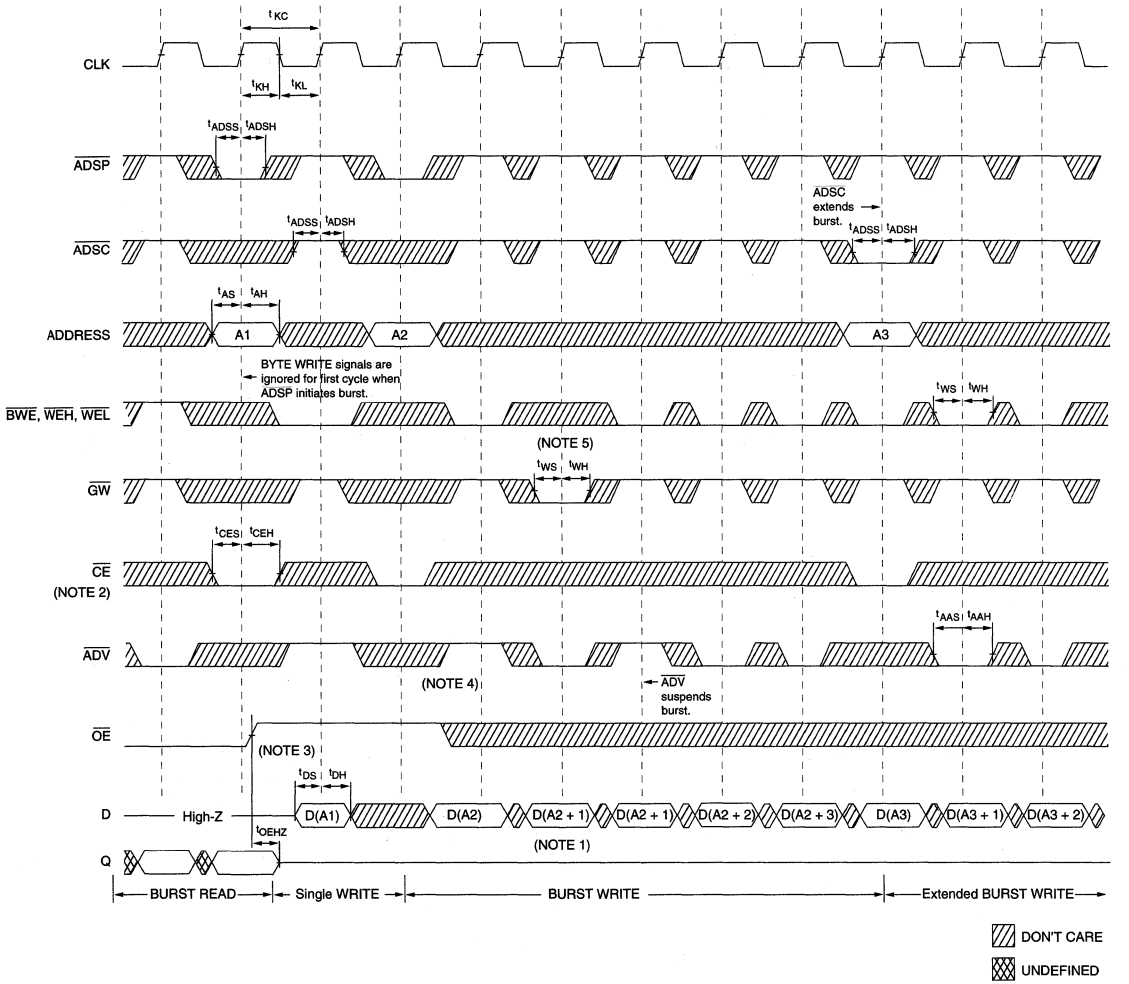
READ TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

SYNCHRONOUS SRAM

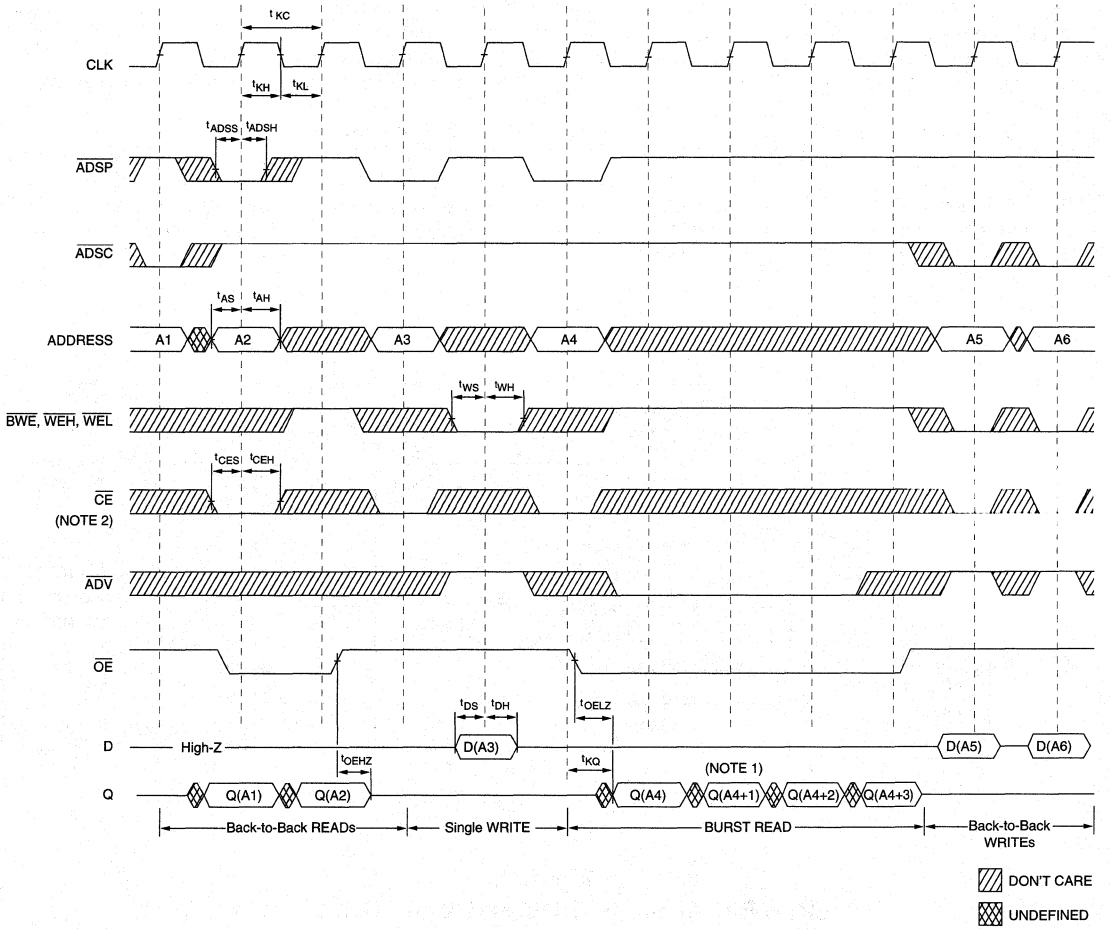
WRITE TIMING



NOTE:

1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.
5. Full width WRITE can be initiated by $\overline{GW}$ LOW or $\overline{GW}$ HIGH and $\overline{BWE}$, $\overline{WEH}$, and $\overline{WEL}$ LOW.

READ/WRITE TIMING



NOTE:
1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{ADSP}$, $\overline{ADSC}$ or $\overline{ADV}$ cycle is performed.
4. $\overline{GW}$ is HIGH.
5. Back-to-back READs may be controlled by either $\overline{ADSP}$ or $\overline{ADSC}$.

APPLICATION INFORMATION

LOAD DERATING CURVES

The Micron 64K x 18 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

$\Delta^tKQ = 0.016$ ns/pF x ΔC_L pF.
(Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8pF (8pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device is a 12ns part, the worst case ^tKQ becomes 11.87ns (approximately).

Consult the factory for copies of I/O current versus voltage curves and capacitive loading derating curves.

DEPTH EXPANSION

The Micron 64K x 18 Synchronous SRAM incorporates two additional chip enables to facilitate simple depth expansion. As shown in Figure 3, this permits easy cache upgrades from 64K depth to 128K depth with no extra logic.

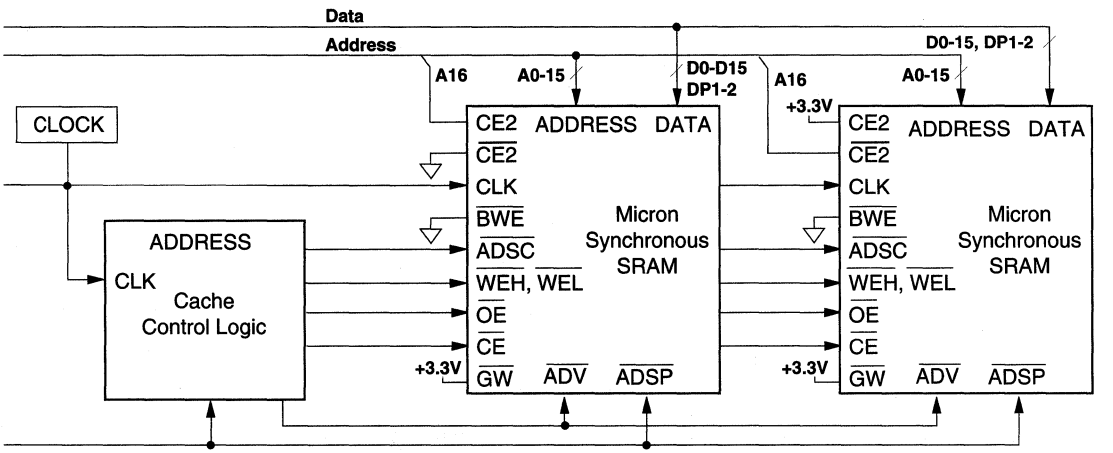


Figure 3
DEPTH EXPANSION FROM 64K x 36 TO 128K x 36

APPLICATION EXAMPLE

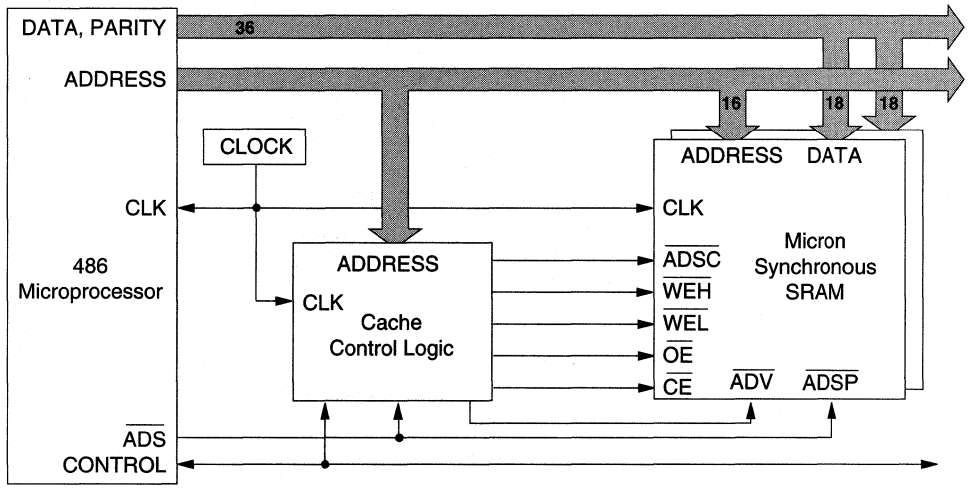


Figure 4
256K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz 80486 USING TWO MT58LC64K18B2EJ-12 SYNCHRONOUS SRAMs

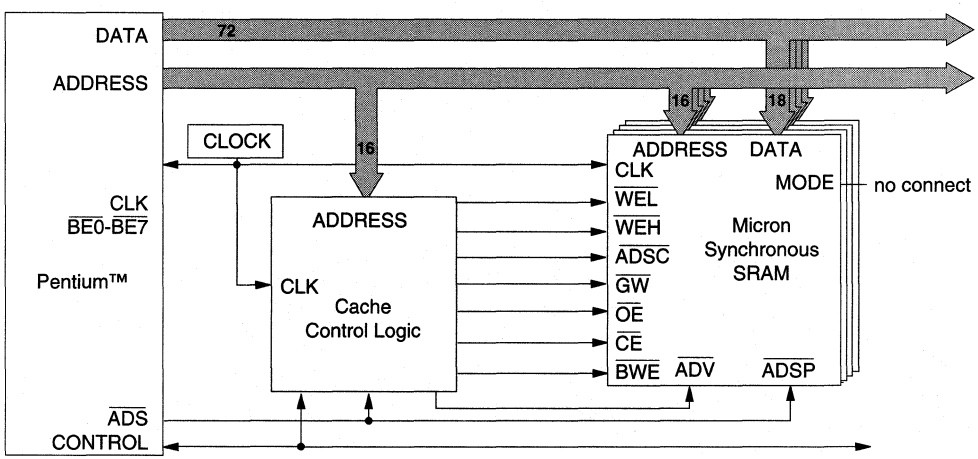


Figure 5
512K BYTE SECONDARY CACHE WITH INTERLEAVED BURST AND DIRECT CONNECTION OF BE# LINES TO SYNCBURST SRAM

SYNCHRONOUS SRAM

64K x 18 SRAM

+3.3V SUPPLY, FULLY REGISTERED INPUTS AND OUTPUTS AND BURST COUNTER

FEATURES

- Fast access times: 4.5, 5, 6, 7 and 8ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- WRITE pass-through capability
- Burst control pins (interleaved or linear burst)
- Automatic power-down for portable applications
- High density, high speed packages
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- DIMMs also available

OPTIONS — MARKING

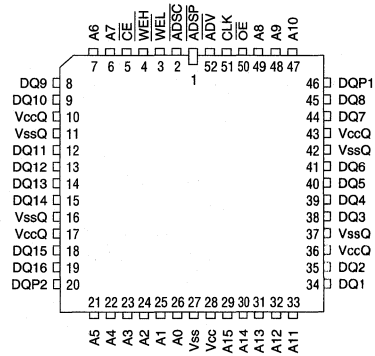
- Timing
  - 4.5ns access/8ns cycle — -4.5
  - 5ns access/10ns cycle — -5
  - 6ns access/12ns cycle — -6
  - 7ns access/15ns cycle — -7
  - 8ns access/20ns cycle — -8
- Packages
  - 52-pin PLCC — EJ
  - 100-pin TQFP — LG
- Low power — P
- 2V data retention, low power — L
- Part Number Example: MT58LC64K18C4LG-7 P

Part Number Examples

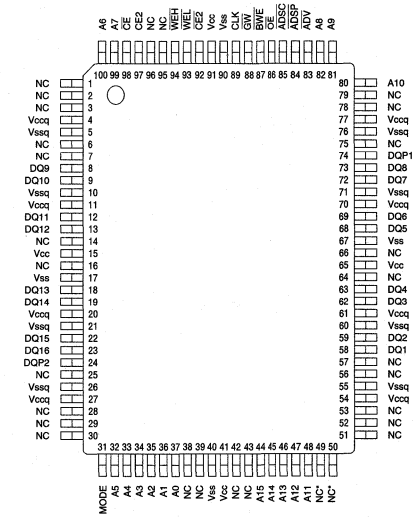
BASE PART NO.	VERSION SUFFIX	PACKAGE	BURST SEQUENCE
MT58LC64K18	A6	EJ	Linear
MT58LC64K18	C4	EJ	Interleaved
MT58LC64K18	C4	LG	Interleaved (Mode = NC) Linear (Mode = GND)

PIN ASSIGNMENT (Top View)

52-Pin PLCC
(SB-1)



100-Pin TQFP
(SC-1)



*Pin 49 is reserved for A16, pin 50 for A17

GENERAL DESCRIPTION

The Micron SyncBurst™ SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC64K18 SRAM integrates a 64K x 18 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) byte write enables ($\overline{WEH}$, $\overline{WEL}$, $\overline{BWE}$) and global write ($\overline{GW}$).

Asynchronous inputs include the output enable ($\overline{OE}$), clock (CLK) and burst mode (MODE). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to two bytes wide as controlled by the write control inputs.

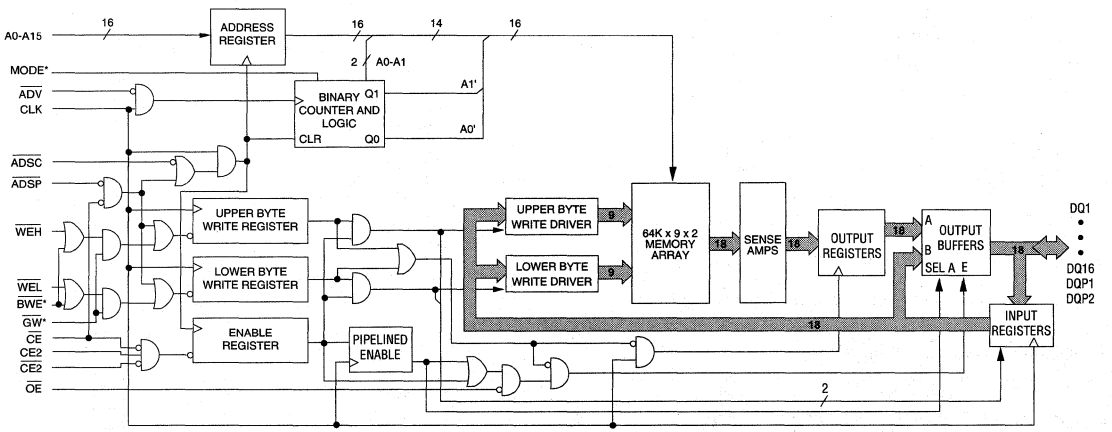
Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{WEL}$ controls DQ1-DQ8 and DQP1. $\overline{WEH}$ controls DQ9-DQ16 and DQP2, conditioned by $\overline{BWE}$ being LOW. $\overline{GW}$ LOW causes all bytes to be written. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE as controlled solely by $\overline{OE}$ to improve cache system response. The device incorporates an additional pipelined enable register to allow depth expansion without penalizing system performance.

The "L" version of this device has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The MT58LC64K18 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V-tolerant. The device is ideally suited for Pentium™ and PowerPC™ pipelined systems and systems that benefit from a very wide high-speed data bus.

FUNCTIONAL BLOCK DIAGRAM



*LG package only

NOTE: 1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

BURST ADDRESS TABLE (MODE = NC or MT58LC64K18C4 EJ device)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

BURST ADDRESS TABLE (MODE = GND or MT58LC64K18A4 EJ device)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PIN DESCRIPTIONS

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
26, 25, 24, 23, 22, 21, 7, 6, 49, 48, 47, 33, 32, 31, 30, 29	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 80, 48, 47, 46, 45, 44	A0-A15	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
4, 3	94, 93	$\overline{WEH}$, $\overline{WEL}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{WEL}$ controls DQ1-DQ8 and DQP1. $\overline{WEH}$ controls DQ9-DQ16 and DQP2. Data I/O are tristated if either of these inputs are LOW.
n/a	87	$\overline{BWE}$	Input	Byte Write Enable: This active LOW input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
n/a	88	$\overline{GW}$	Input	Global Write: This active LOW input allows a full 18-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{WEn}$ lines and must meet the setup and hold times around the rising edge of CLK.
51	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
5	98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
n/a	92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded.

PIN DESCRIPTIONS (continued)

PLCC PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
n/a	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded.
50	86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
52	83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
1	84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon $\overline{CE}$ being LOW.
2	85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if $\overline{CE}$ is LOW. $\overline{ADSC}$ is also used to place the chip into power-down state when $\overline{CE}$ is HIGH.
n/a	31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12, 13, 14, 15, 18, 19	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1-DQ16	Input/ Output	SRAM Data I/O: Low Byte is DQ1-DQ8. High Byte is DQ9-DQ16. Input data must meet setup and hold times around the rising edge of CLK.
46, 20	74, 24	DQP1, DQP2	Input/ Output	Parity Data I/O: Low Byte Parity is DQP1. High Byte Parity is DQP2.
28	15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
27	17, 40, 67, 90	Vss	Supply	Ground: GND
10, 17, 36, 43	4, 11, 20, 28, 54, 61, 70, 77	Vccq	Supply	Isolated Output Buffer Supply: +3.3V ±5%
11, 16, 37, 42	6, 10, 21, 26, 55, 60, 71, 76	Vssq	Supply	Isolated Output Buffer Ground: GND
	1, 2, 3, 6, 7, 14, 16, 25, 28, 29, 30, 38, 39, 42, 43, 49, 50, 51, 52, 53, 56, 57, 64, 66, 75, 78, 79, 95, 96	NC	-	No Connect: These signals are not internally connected. These signals may be connected to ground to improve package heat dissipation.

PARTIAL TRUTH TABLE FOR WRITEs

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{WEL}$	$\overline{WEH}$
READ	H	H	X	X
READ	H	L	H	H
WRITE Low Byte	H	L	L	H
WRITE High Byte	H	L	H	L
WRITE all bytes	H	L	L	L
WRITE all bytes	L	X	X	X

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{WEs}$	OPERATION	$\overline{CE}$	$\overline{WEs}$	$\overline{OE}$	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L[2,3]	Initiate READ cycle Register A(n), Q = D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L[2,3]	No new cycle Q = D(n-1)	H	H	L	No carry-over from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L[2,3]	No new cycle Q = HIGH-Z	H	H	H	No carry-over from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1), data = D(n-1)	One L[2]	No new cycle Q = D(n-1) for one byte	H	H	L	No carry-over from previous cycle

NOTE: 1. Previous cycle may be either BURST or NONBURST cycle.
2. $\overline{BWE}$ is LOW when one or two $\overline{WEn}$ is LOW.
3. $\overline{GW}$ LOW will yield identical results.

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{WEL}$ or $\overline{WEH}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{WEL}$ enables WRITEs to DQ1-DQ8, DQP1. $\overline{WEH}$ enables WRITEs to DQ9-DQ16, DQP2.
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +150°C
Junction Temperature** ..... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	14
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1, 11
Supply Voltage		V_{CC}	3.1	3.5	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-4.5	-5	-6	-7	-8	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; V_{CC} = MAX; outputs open	I_{CC}	ALL	180	400	335	300	250	210	mA	3, 12, 13
Power Supply Current: Idle	Device selected; V_{CC} = MAX; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{GW}$, $\overline{BWs}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; cycle time ≥ ^tKC MIN	I_{CC1}	ALL	30	65	60	55	50	45	mA	12, 13
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB2}	STD	0.5	5	5	5	5	5	mA	12, 13
			P	0.2	2	2	2	2	2	mA	
TTL Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB3}	STD	15	25	25	25	25	25	mA	12, 13
			P	8	18	18	18	18	18	mA	
Clock Running	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB4}	ALL	30	65	60	55	50	45	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	V_{CC} = 3.3V	C_O	6	7	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	PLCC TYP	TQFP TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still air, soldered on 4.25 x	θ_{JA}	45	20	°C/W	
Thermal resistance - Junction to Case	1.125 inch 4-layer PCB	θ_{JC}	15	1	°C/W	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±5%)

DESCRIPTION		-4.5		-5		-6		-7		-8			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock													
Clock cycle time	^tKC	8		10		12		15		20		ns	
Clock HIGH time	^tKH	3		4		4.5		5		6		ns	
Clock LOW time	^tKL	3		4		4.5		5		6		ns	
Output Times													
Clock to output valid	^tKQ		4.5		5		6		7		8	ns	
Clock to output invalid	^tKQX	2		2		2		2		2		ns	
Clock to output in Low-Z	^tKQLZ	4		4		5		5		5		ns	6, 7
Clock to output in High-Z	^tKQHZ		4.5		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		4.5		5		5		5		6	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		3		4		5		6		6	ns	6, 7
Setup Times													
Address	^tAS	2.5		2.5		2.5		2.5		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSS	2.5		2.5		2.5		2.5		3		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAS	2.5		2.5		2.5		2.5		3		ns	8, 10
Write Signals ($\overline{WE1}$, $\overline{WE2}$, $\overline{BWE}$, $\overline{GW}$)	^tWS	2.5		2.5		2.5		2.5		3		ns	8, 10
Data-in	^tDS	2.5		2.5		2.5		2.5		3		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCES	2.5		2.5		2.5		2.5		3		ns	8, 10
Hold Times													
Address	^tAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Write Signals ($\overline{WE1}$, $\overline{WE2}$, $\overline{BWE}$, $\overline{GW}$)	^tWH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCEH	0.5		0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

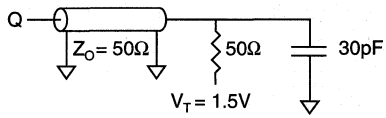


Fig. 1 OUTPUT LOAD EQUIVALENT

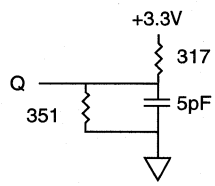


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

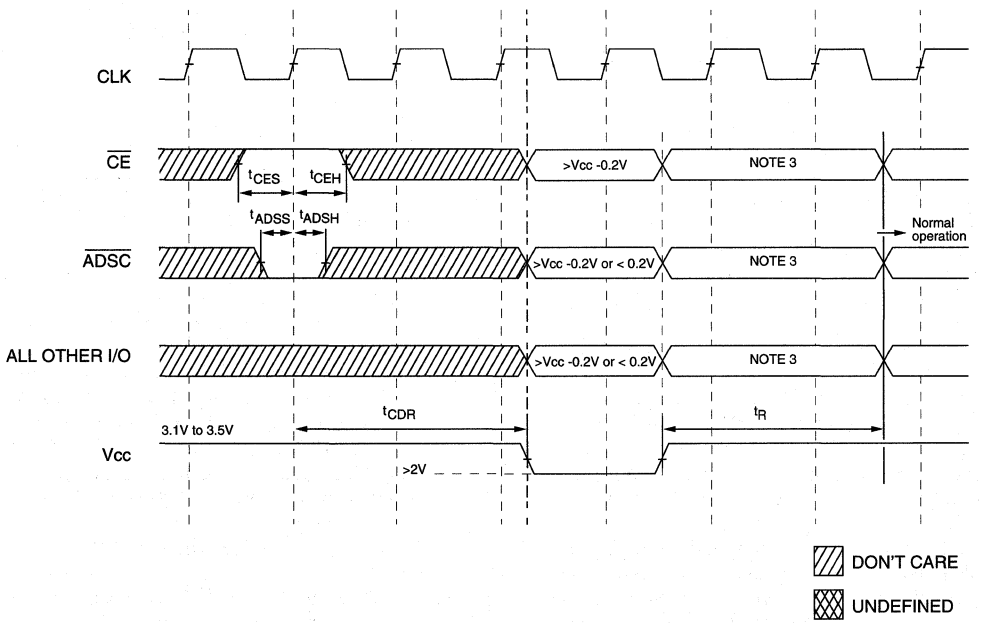
1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200ms$
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ($\overline{ADSC}$ or $\overline{ADV}$ LOW) or $\overline{ADSP}$ LOW for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
15. Typical values are measured at 25°C.
16. The device must have a deselect cycle applied at least two clock cycles before data retention mode is entered.

SYNCHRONOUS SRAM

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

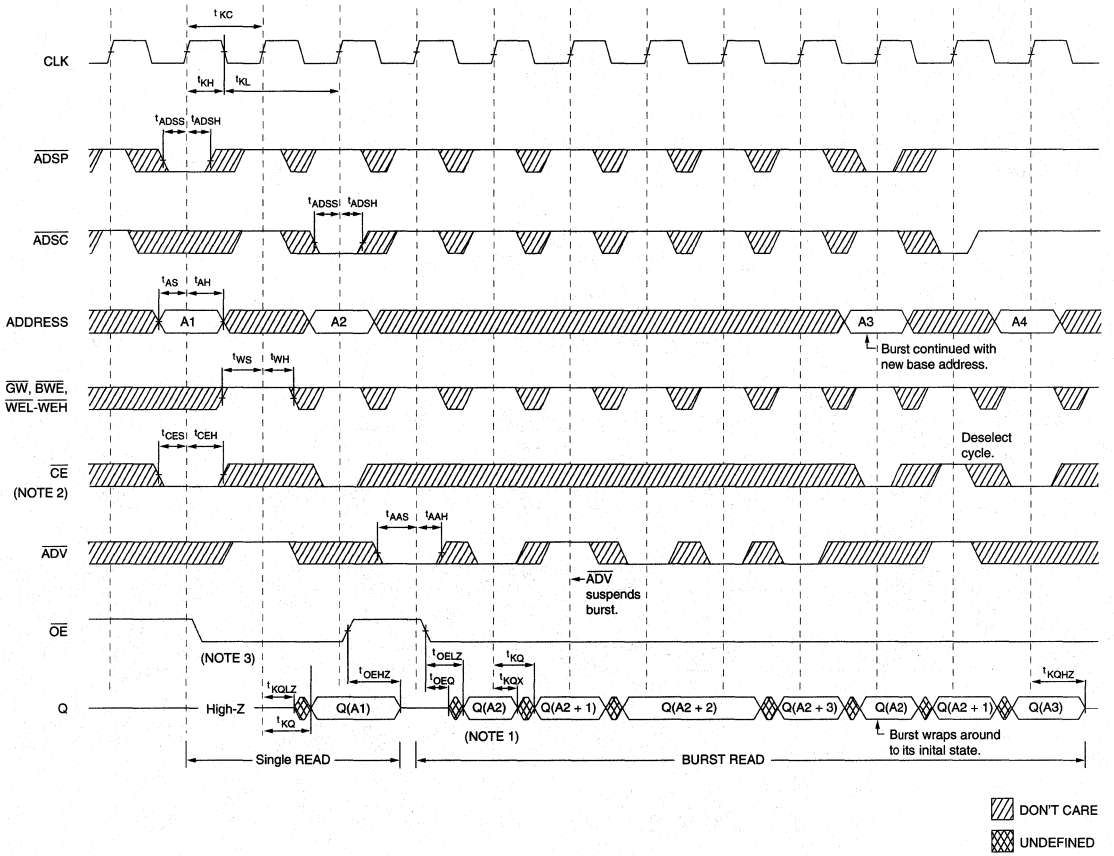
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2} \geq (V_{CC} - 0.2V)$, $CE2 \leq 0.2V$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$ $V_{CC} = 2V$	I_{CCDR}		TBD	µA	15
Chip Deselect to Data Retention Time		^tCDR	2 ^tKC		ns	4, 16
Operation Recovery Time		^tR	2 ^tKC		ns	4

LOW V_{CC} DATA RETENTION WAVEFORM



NOTE:
1. All inputs must be ≥ V_{CC} - 0.2V or ≤ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded.
2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.
3. The device control signals should be in a deselect state between the rising edge of V_{CC} and until ^tR is met.

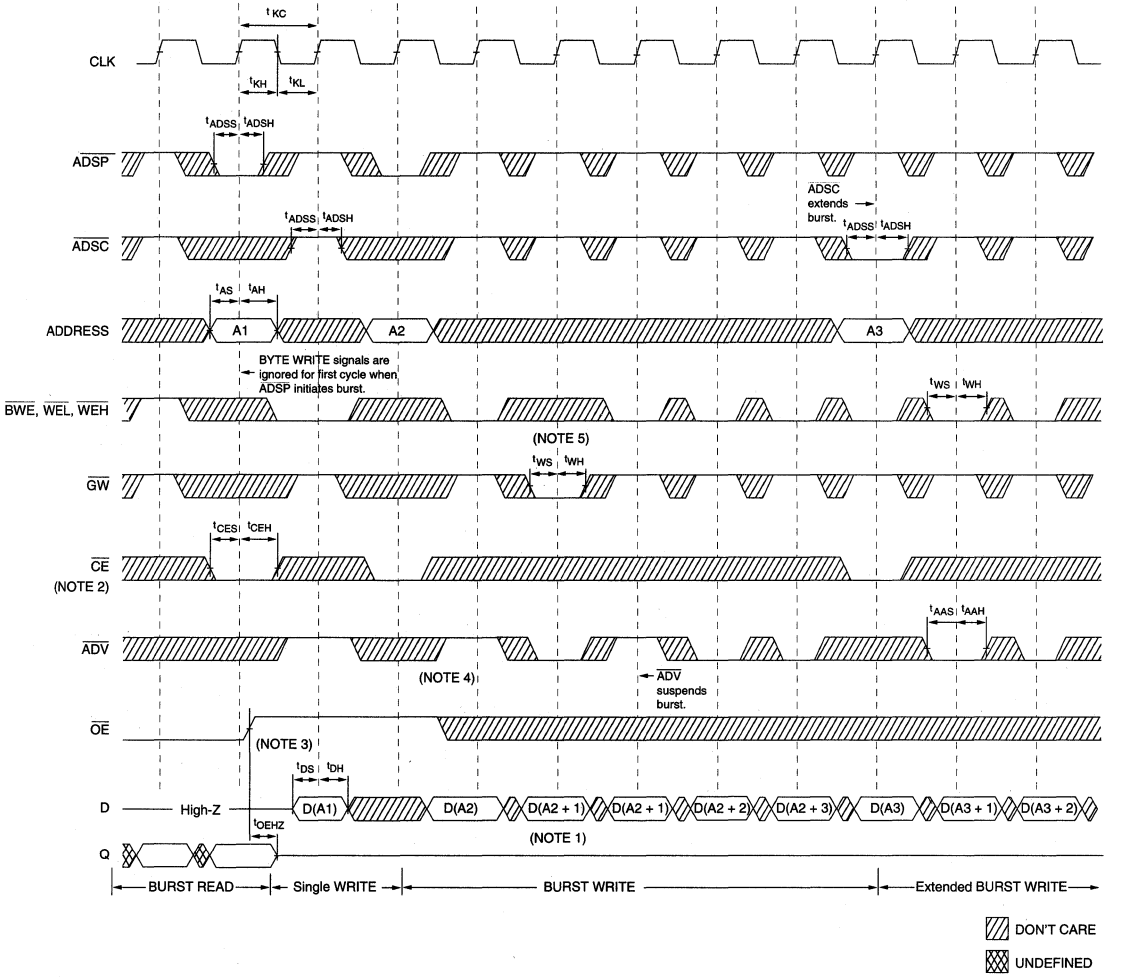
READ TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

SYNCHRONOUS SRAM

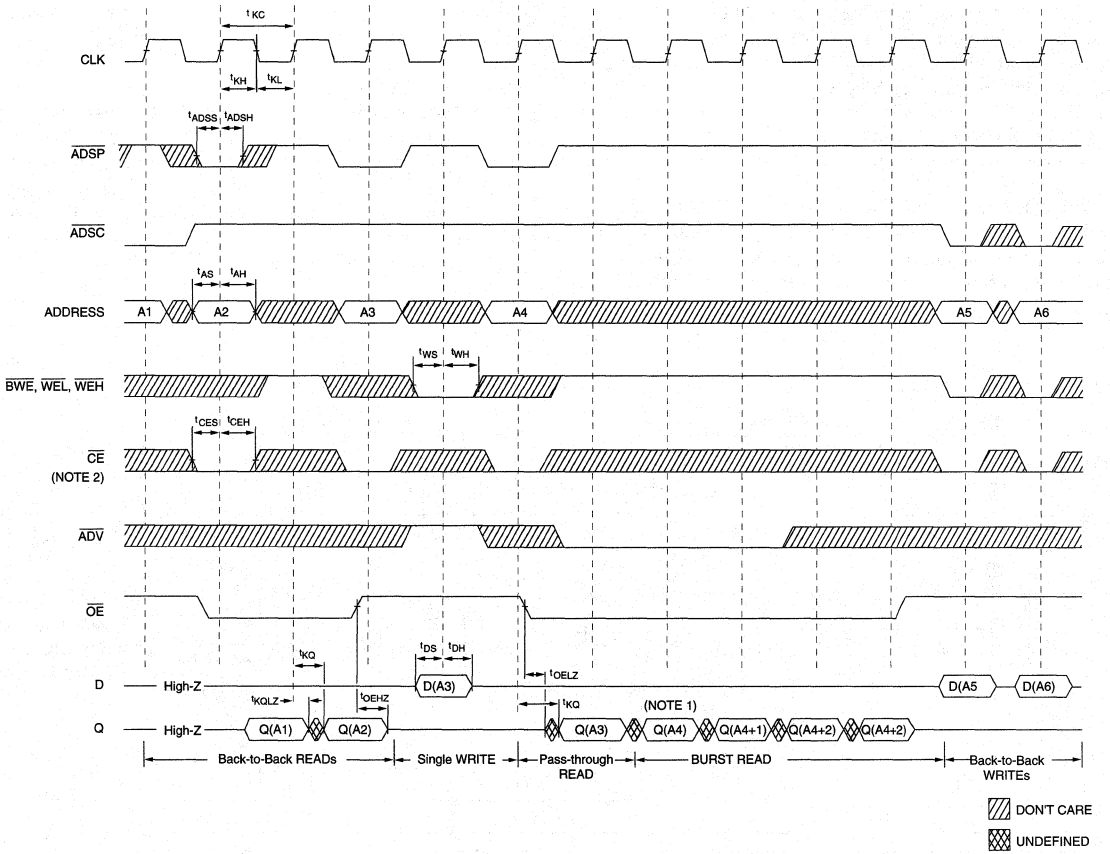
WRITE TIMING



NOTE:

1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.
5. Full width WRITE can be initiated by $\overline{GW}$ LOW or $\overline{GW}$ HIGH and $\overline{BWE}$, $\overline{WEL}$ and $\overline{WEH}$ LOW.

READ/WRITE TIMING



NOTE:
1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{ADSP}$, $\overline{ADSC}$ or $\overline{ADV}$ cycle is performed.
4. $\overline{GW}$ is HIGH.
5. Back-to-back READs may be controlled by either $\overline{ADSP}$ or $\overline{ADSC}$.

APPLICATION INFORMATION

LOAD DERATING CURVES

The Micron 64K x 18 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

$\Delta^{t}KQ = 0.016$ ns/pF x ΔC_L pF.
(Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8pF (8pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device is an 8ns part, the worst case ^{t}KQ becomes 7.87ns (approximately).

Consult the factory for copies of I/O current versus voltage curves and capacitive loading derating curves.

DEPTH EXPANSION

The Micron 64K x 18 Synchronous SRAM incorporates two additional chip enables to facilitate simple depth expansion. As shown in Figure 3, this permits easy cache upgrades from 64K depth to 128K depth with no extra logic. The chip enables are pipelined to allow contention-free transition between Micron devices which are physically and electrically close together.

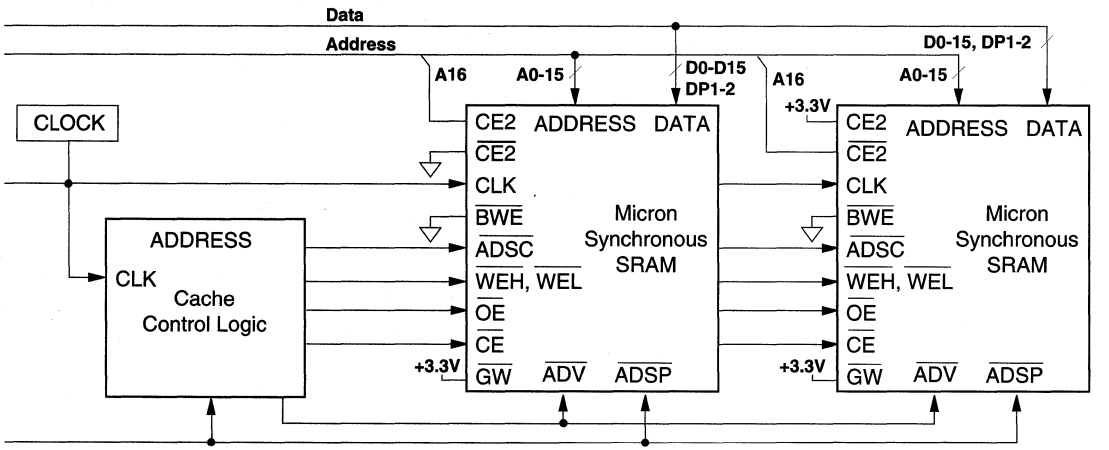


Figure 3
DEPTH EXPANSION FROM 64K x 18 TO 128K x 18 USING TQFP PACKAGES

APPLICATION EXAMPLES

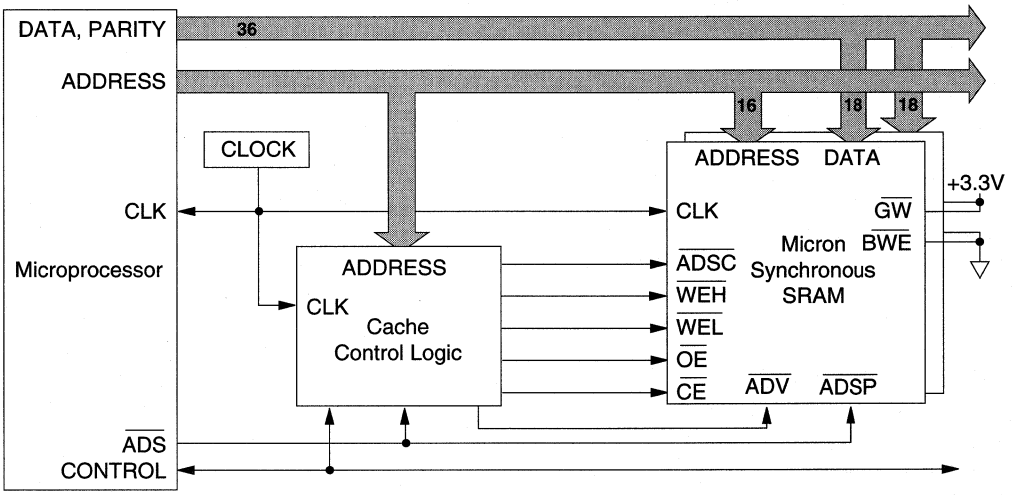


Figure 4
256K BYTE 50 MHz SECONDARY CACHE WITH PARITY AND BURST USING TWO MT58LC64K18C4LG-8 SYNCBURST SRAMs

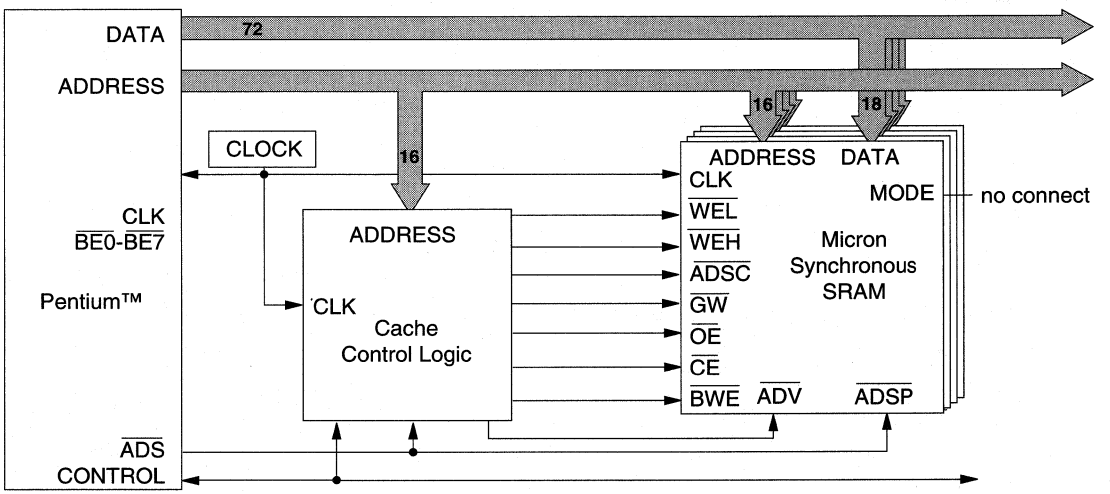


Figure 5
256K BYTE SECONDARY CACHE WITH PARITY, INTERLEAVED BURST AND DIRECT CONNECTION OF BE# LINES TO SYNCBURST SRAM

SYNCHRONOUS SRAM

32K x 32 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS, BURST COUNTER

NEW SYNCHRONOUS SRAM

FEATURES

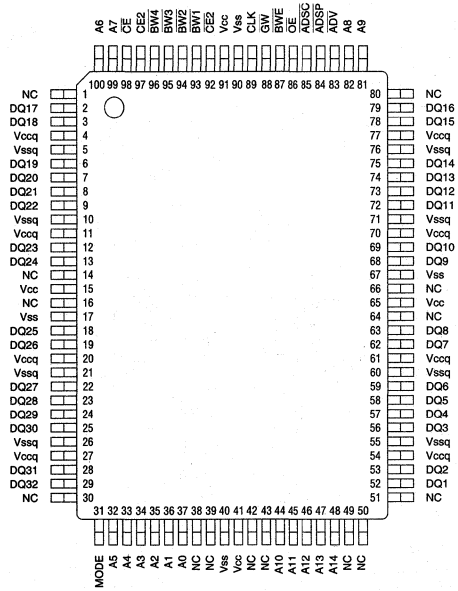
- Fast access times: 9, 10, 11, 12 and 14ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Burst control pins (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- DIMMs also available

OPTIONS — MARKING

- Timing
  - 9ns access/15ns cycle — -9
  - 10ns access/15ns cycle — -10
  - 11ns access/15ns cycle — -11
  - 12ns access/20ns cycle — -12
  - 14ns access/20ns cycle — -14
- Packages
  - 100-pin TQFP — LG
- Low power — P
- 2V data retention, low power — L
- Part Number Example: MT58LC32K32B2LG-12 P

PIN ASSIGNMENT (Top View)

100-Pin TQFP
(SC-1)



GENERAL DESCRIPTION

The Micron SyncBurst™ SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC32K32B2 SRAM integrates a 32K x 32 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$) and global write ($\overline{GW}$).

Asynchronous inputs include the output enable ($\overline{OE}$), clock (CLK) and burst mode (MODE). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQ1-DQ8, $\overline{BW2}$ controls DQ9-DQ16, $\overline{BW3}$

NEW ■ SYNCHRONOUS SRAM

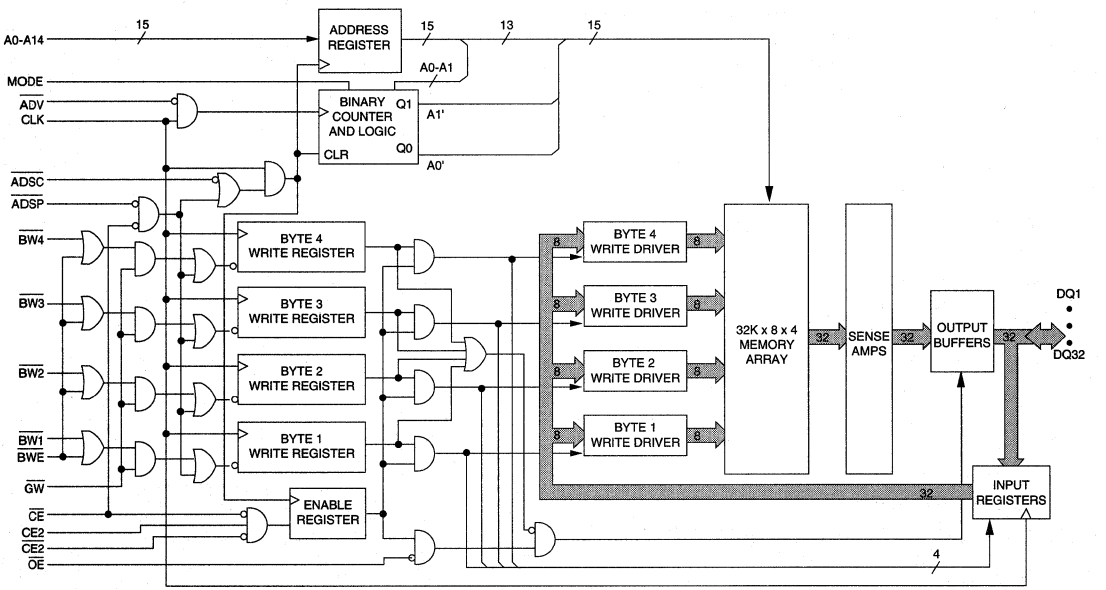
GENERAL DESCRIPTION (continued)

controls DQ17-DQ24, and $\overline{BW4}$ controls DQ25-DQ32, conditioned by $\overline{BWE}$ being LOW. $\overline{GW}$ LOW causes all bytes to be written.

The "L" version of this device has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The MT58LC32K32B2 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V-tolerant. The device is ideally suited for 486, Pentium™, 680X0 and PowerPC™ systems and systems that benefit from a very wide data bus. The device is also ideal in generic 32- and 64-bit-wide applications.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
37, 32, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0-A14	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when $\overline{BWE}$ is LOW and must meet the setup and hold times around the rising edge of CLK. A Byte Write Enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW1}$ controls DQ1-DQ8. $\overline{BW2}$ controls DQ9-DQ16. $\overline{BW3}$ controls DQ17-DQ24 and $\overline{BW4}$ controls DQ25-DQ32. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

NEW ■ SYNCHRONOUS SRAM

PIN DESCRIPTIONS (continued)

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
87	$\overline{BWE}$	Input	Byte Write Enable: This active low input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
88	$\overline{GW}$	Input	Global Write: This active low input allows a full 32-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BWn}$ lines and must meet the setup and hold times around the rising edge of CLK.
1, 14, 16, 30, 38, 39, 42, 43, 49, 50, 51, 64, 66, 80	NC	-	No Connect: These signals are not internally connected.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 64, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ1-DQ32	Input/ Output	SRAM Data I/O: Byte 1 is DQ1-DQ8; Byte 2 is DQ9-DQ16; Byte 3 is DQ17-DQ24; Byte 4 is DQ25-DQ32. Input data must meet setup and hold times around the rising edge of CLK.
31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
17, 40, 67, 90	Vss	Supply	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%
5, 10, 21, 26, 55, 60, 71, 76	VssQ	Supply	Isolated Output Buffer Ground: GND

INTERLEAVED BURST ADDRESS TABLE (MODE = NC)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = GND)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW1}$ enables WRITEs to Byte 1 (DQ1-DQ8). $\overline{BW2}$ enables WRITEs to Byte 2 (DQ9-DQ16). $\overline{BW3}$ enables WRITEs to Byte 3 (DQ17-DQ24). $\overline{BW4}$ enables WRITEs to Byte 4 (DQ25-DQ32).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE FOR WRITEs

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte 1	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

NOTE: Using $\overline{BWE}$ and $\overline{BW1}$ through $\overline{BW4}$, any one or more bytes may be written.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +150°C
Junction Temperature** ..... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	14
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1, 11
Supply Voltage		V_{CC}	3.1	3.5	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-9	-10	-11	-12	-14	UNITS	NOTES
Power Supply Current: Operating	Device selected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; outputs open	I_{CC}	ALL	180	270	270	250	225	225	mA	3, 12, 13
Power Supply Current: Idle	Device selected; V_{CC} = MAX; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{GW}$, $\overline{BWs}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; cycle time ≥ ^tKC MIN	I_{CC1}	ALL	28	45	45	45	40	40	mA	12, 13
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB2}	STD	0.5	5	5	5	5	5	mA	12, 13
			P	0.2	2	2	2	2	2	mA	
TTL Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB3}	STD	15	25	25	25	25	25	mA	12, 13
			P	8	18	18	18	18	18	mA	
Clock Running	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB4}	ALL	30	50	50	50	45	45	mA	12, 13

NEW SYNCHRONOUS SRAM

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	V_{CC} = 3.3V	C_O	6	7	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air, Soldered on 4.25 x	θ_{JA}	20	°C/W	
Thermal resistance - Junction to Case	1.125 inch 4-layer circuit board	θ_{JC}	1	°C/W	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±5%)

DESCRIPTION		-9		-10		-11		-12		-14			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock													
Clock cycle time	^tKC	15		15		15		20		20		ns	
Clock HIGH time	^tKH	4		5		5		6		6		ns	
Clock LOW time	^tKL	4		5		5		6		6		ns	
Output Times													
Clock to output valid	^tKQ		9		10		11		12		14	ns	
Clock to output invalid	^tKQX	3		3		3		3		3		ns	
Clock to output in Low-Z	^tKQLZ	5		5		5		5		5		ns	6, 7
Clock to output in High-Z	^tKQHZ		5		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		5		5		5		6		6	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		5		5		5		6		6	ns	6, 7
Setup Times													
Address	^tAS	2.5		2.5		2.5		3		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSS	2.5		3		3		3		3		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAS	2.5		3		3		3		3		ns	8, 10
Write Signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	^tWS	2.5		3		3		3		3		ns	8, 10
Data-in	^tDS	2.5		3		3		3		3		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCES	2.5		3		3		3		3		ns	8, 10
Hold Times													
Address	^tAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Write Signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	^tWH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCEH	0.5		0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

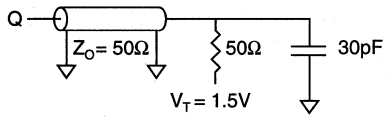


Fig. 1 OUTPUT LOAD EQUIVALENT

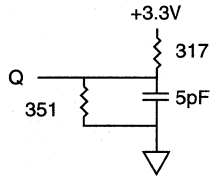


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

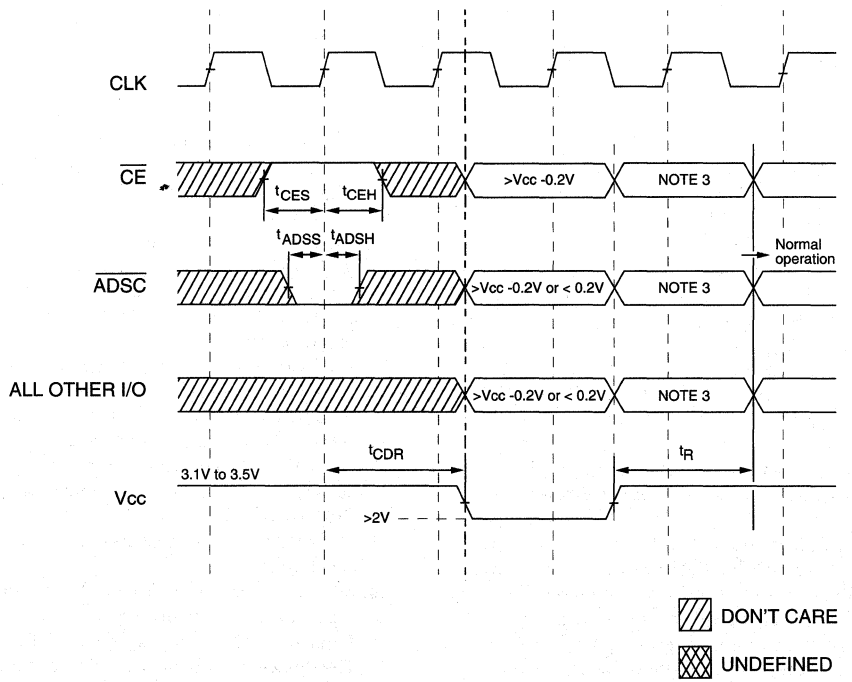
1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200ms$
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ($\overline{ADSC}$ or $\overline{ADV}$ LOW) or $\overline{ADSP}$ LOW for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
15. Typical values are measured at 25°C.
16. The device must have a deselect cycle applied at least one clock cycle before data retention mode is entered.

NEW SYNCHRONOUS SRAM

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

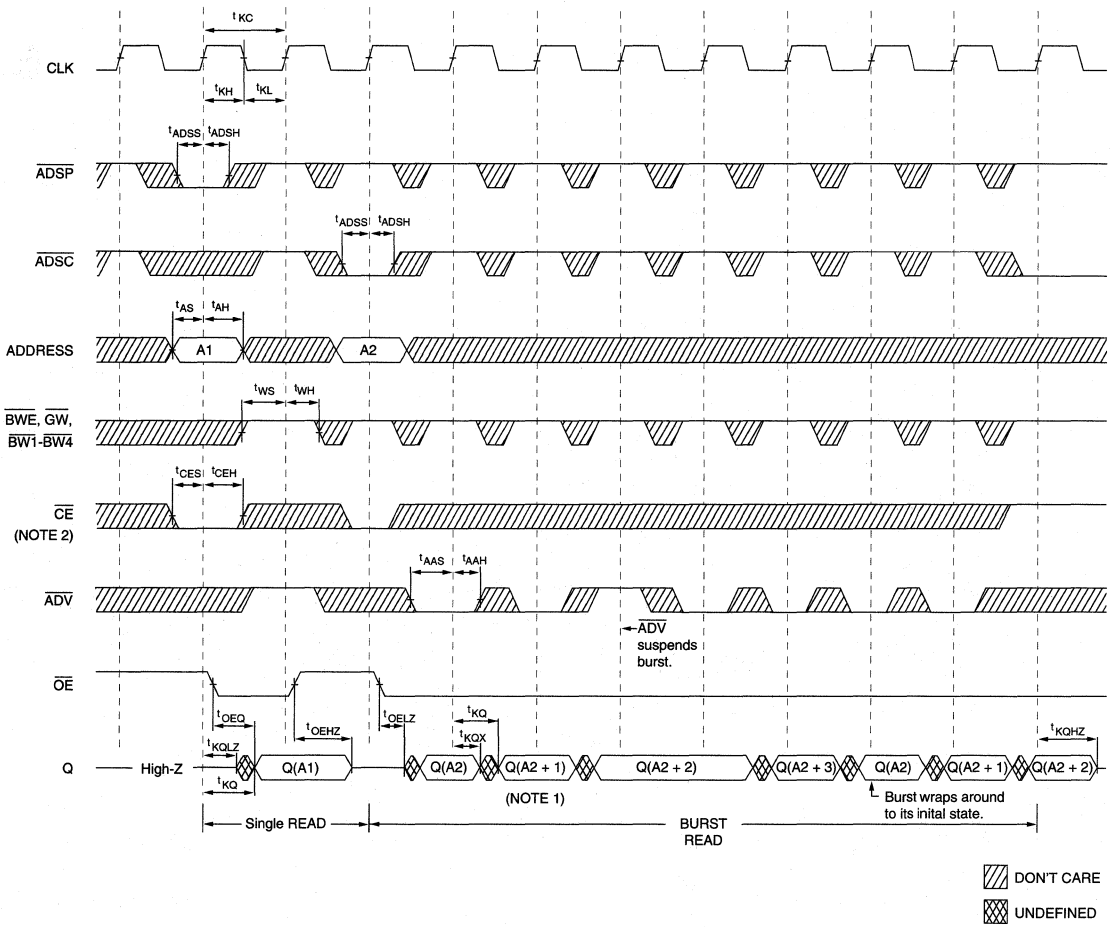
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2} \geq (V_{CC} - 0.2V)$, $CE2 \leq 0.2V$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$ $V_{CC} = 2V$	I_{CCDR}		TBD	µA	15
Chip Deselect to Data Retention Time		^tCDR	^tKC		ns	4, 16
Operation Recovery Time		^tR	^tKC		ns	4

LOW V_{CC} DATA RETENTION WAVEFORM



NOTE:
1. All inputs must be ≥ V_{CC} - 0.2V or ≤ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded.
2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.
3. The device control signals should be in a deselect state between the rising edge of V_{CC} and until ^tR is met.

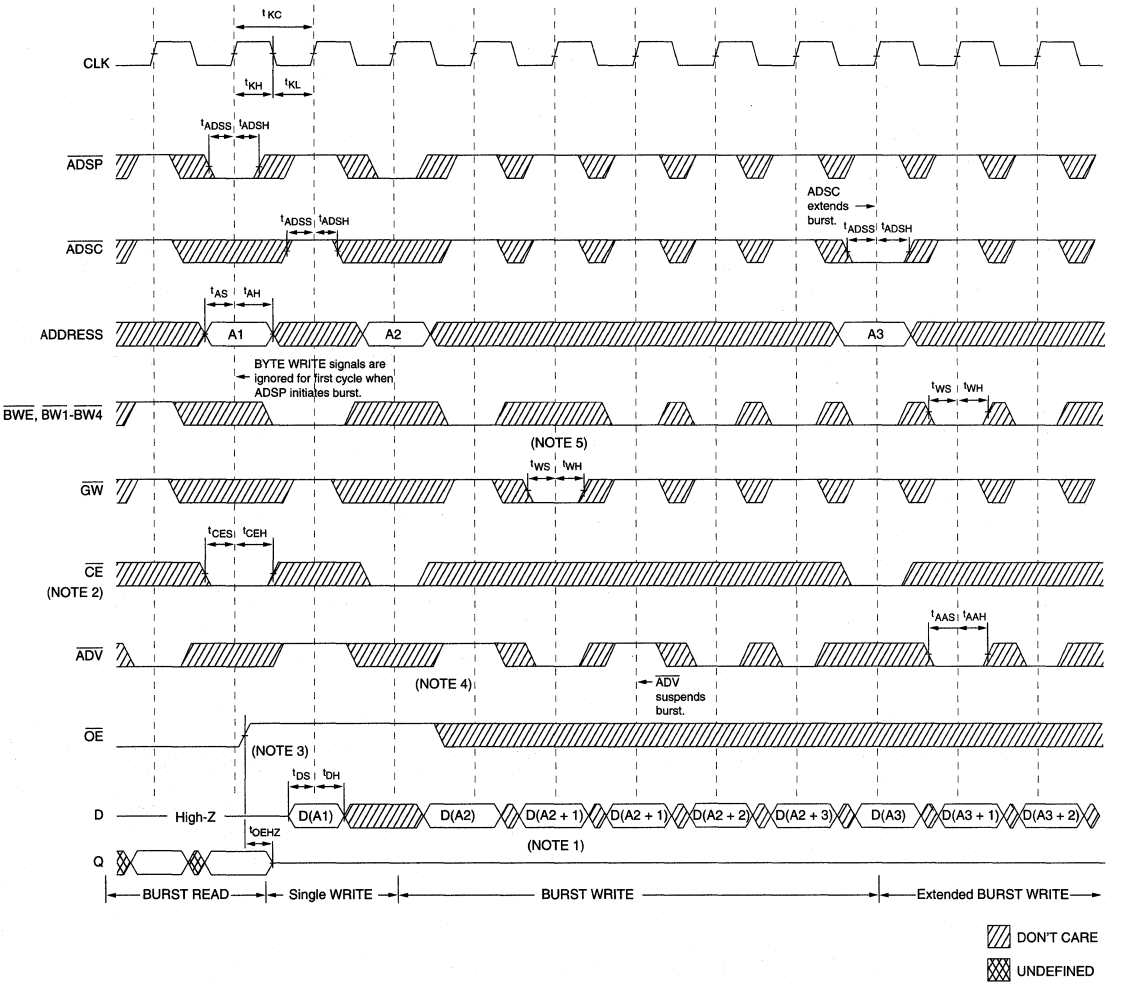
READ TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

NEW ■ SYNCHRONOUS SRAM

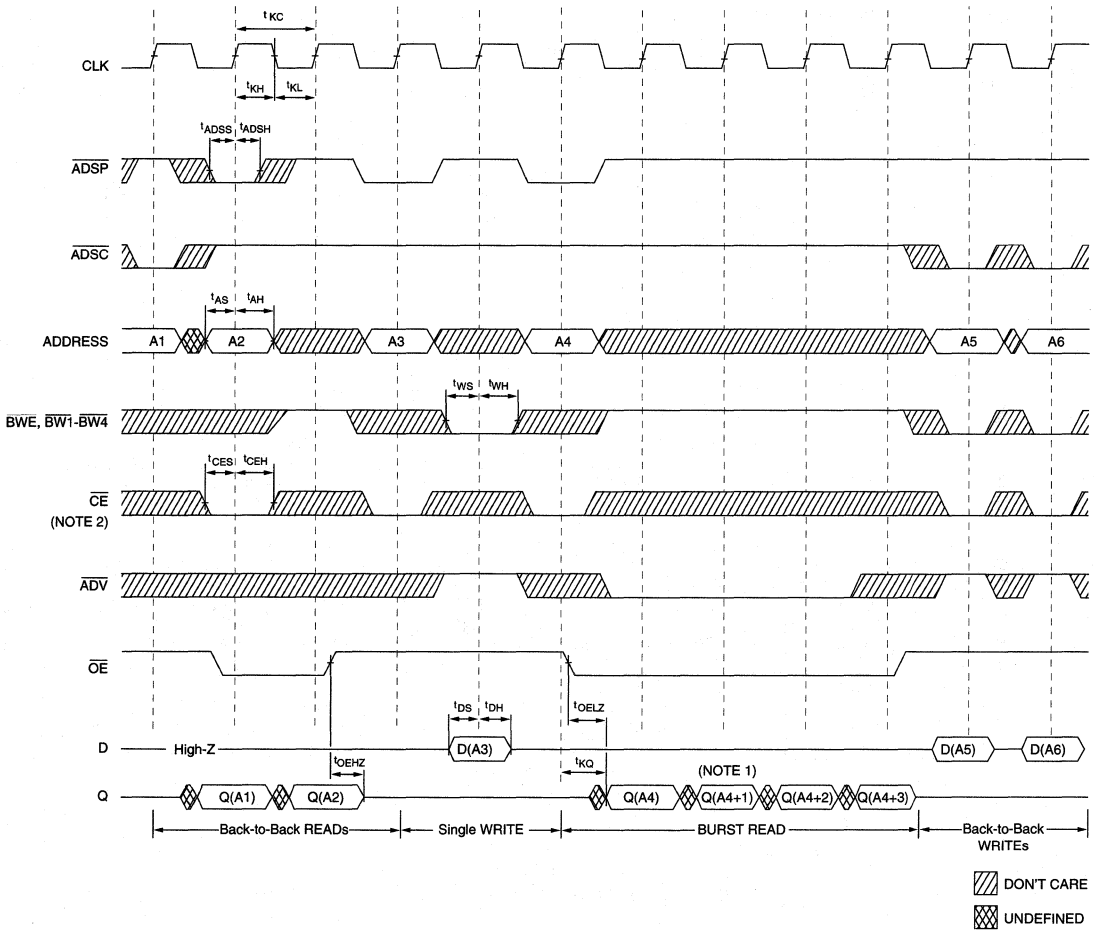
WRITE TIMING



NOTE:

1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.
5. Full width WRITE can be initiated by $\overline{GW}$ LOW or $\overline{GW}$ HIGH and $\overline{BWE}$, $\overline{BW1}$- $\overline{BW4}$ LOW.

READ/WRITE TIMING



NOTE:
1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{ADSP}$, $\overline{ADSC}$ or $\overline{ADV}$ cycle is performed.
4. $\overline{GW}$ is HIGH.

NEW SYNCHRONOUS SRAM

APPLICATION INFORMATION

LOAD DERATING CURVES

The Micron 32K x 32 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

$\Delta^{t}KQ = 0.016$ ns/pF x ΔC_L pF.
(Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8pF (8pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device is a 12ns part, the worst case ^{t}KQ becomes 11.87ns (approximately).

Consult the factory for copies of I/O current versus voltage curves and capacitive loading derating curves.

DEPTH EXPANSION

The Micron 32K x 32 Synchronous SRAM incorporates two additional chip enables to facilitate simple depth expansion. As shown in Figure 3, this permits easy cache upgrades from 32K depth to 64K depth with no extra logic.

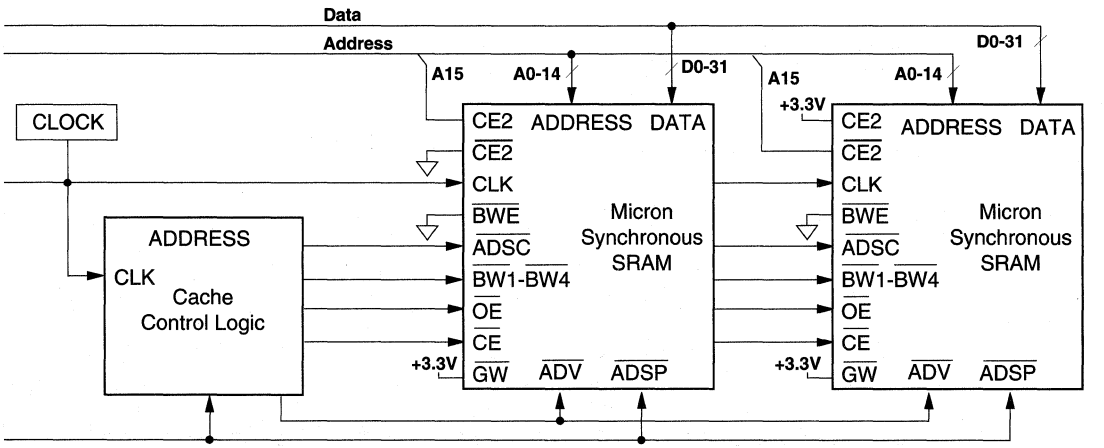


Figure 3
DEPTH EXPANSION FROM 32K x 32 TO 64K x 32

APPLICATION EXAMPLES

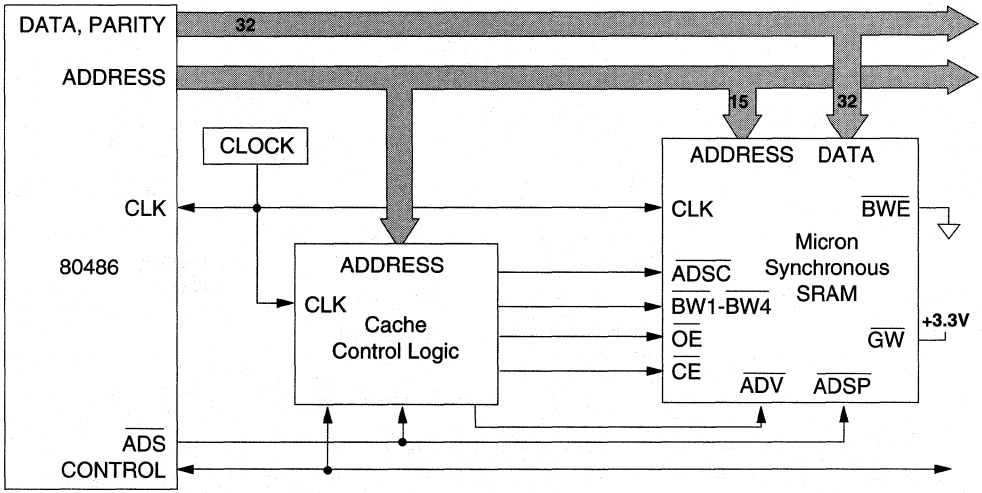


Figure 4
128K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz 80486 USING ONE MT58LC32K32B2LG-12 SYNCHRONOUS SRAM

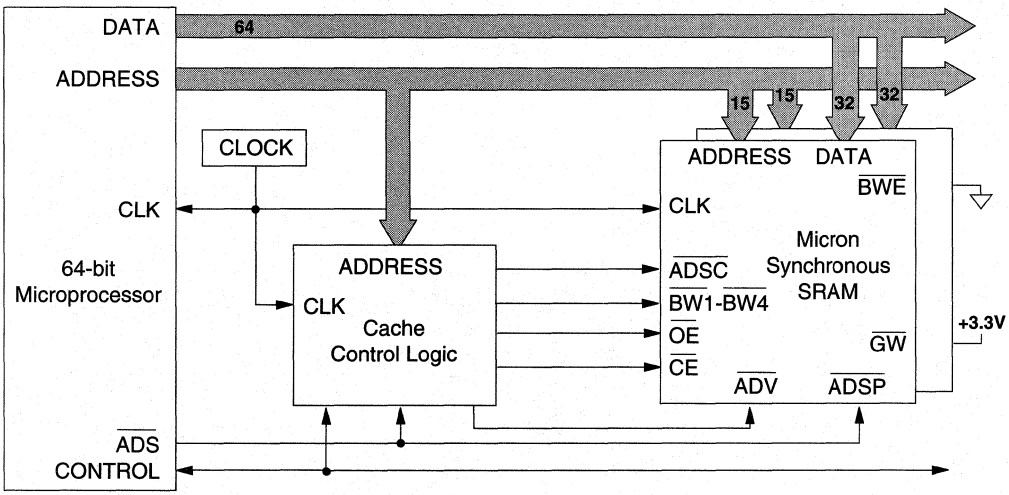


Figure 5
256K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 66 MHz PENTIUM USING TWO MT58LC32K32B2LG-9 SYNCHRONOUS SRAMs

APPLICATION EXAMPLES

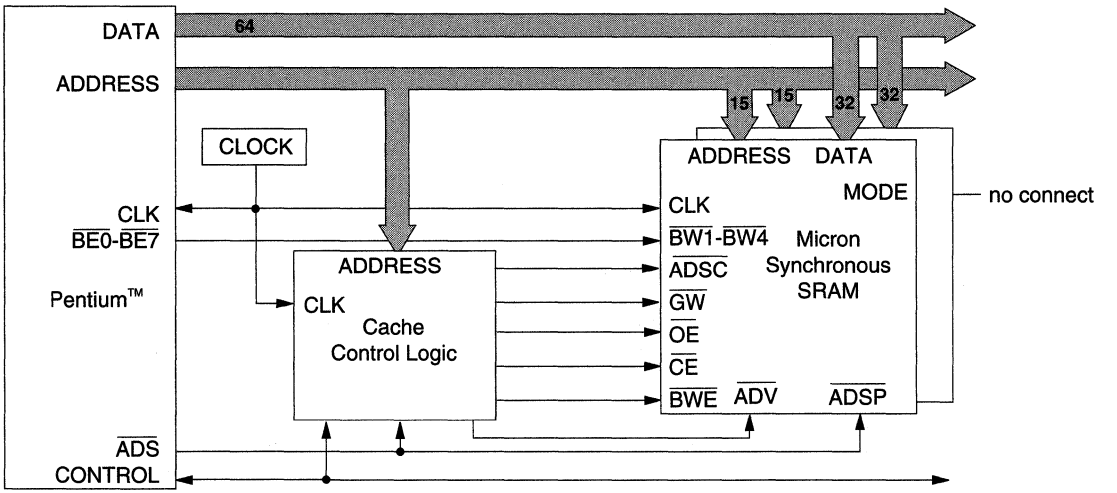


Figure 6
256K BYTE SECONDARY CACHE WITH PARITY, INTERLEAVED BURST AND DIRECT CONNECTION OF BE# LINES TO SYNCBURST SRAM

SYNCHRONOUS SRAM

32K x 32 SRAM

+3.3V SUPPLY, FULLY REGISTERED INPUTS AND OUTPUTS AND BURST COUNTER

NEW SYNCHRONOUS SRAM

FEATURES

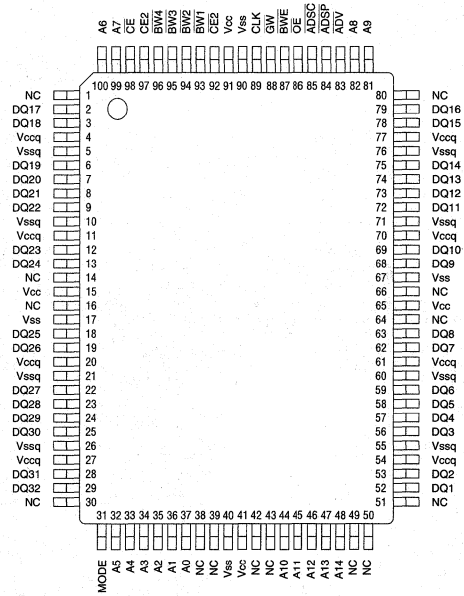
- Fast access times: 4.5, 5, 6, 7 and 8ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- WRITE pass-through capability
- Burst control pins (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- DIMMs also available

OPTIONS — MARKING

- Timing
  - 4.5ns access/8ns cycle — -4.5
  - 5ns access/10ns cycle — -5
  - 6ns access/12ns cycle — -6
  - 7ns access/15ns cycle — -7
  - 8ns access/20ns cycle — -8
- Packages
  - 100-pin TQFP — LG
- Low power — P
- 2V data retention, low power — L
- Part Number Example: MT58LC32K32C4LG-7 P

PIN ASSIGNMENT (Top View)

100-Pin TQFP
(SC-1)



GENERAL DESCRIPTION

The Micron SyncBurst™ SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC32K32C4 SRAM integrates a 32K x 32 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$) and global write ($\overline{GW}$).

Asynchronous inputs include the output enable ($\overline{OE}$), clock (CLK) and burst mode (MODE). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

NEW ■ SYNCHRONOUS SRAM

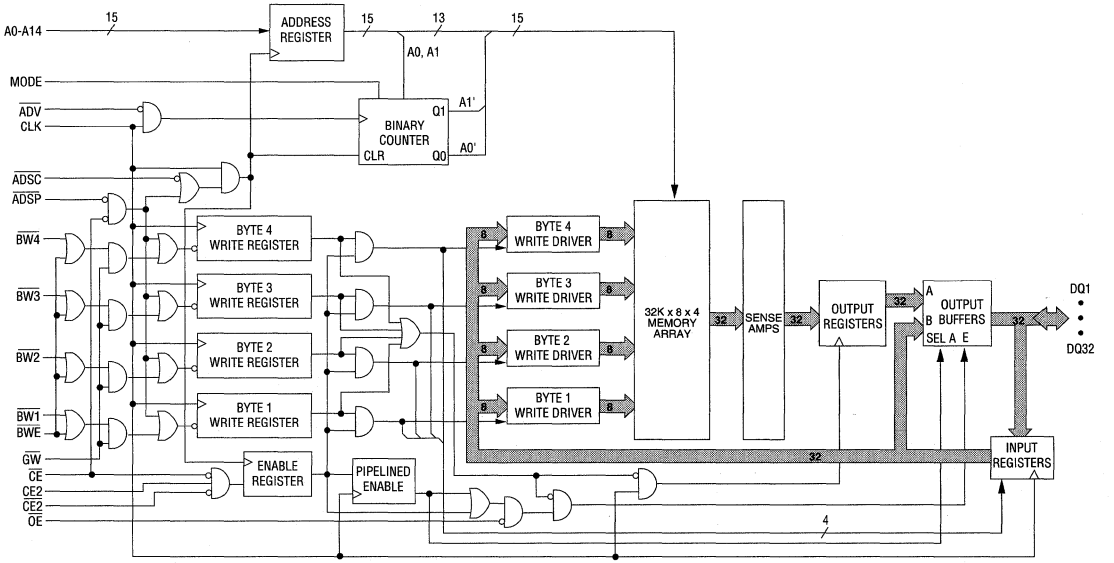
GENERAL DESCRIPTION (continued)

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQ1-DQ8, $\overline{BW2}$ controls DQ9-DQ16, $\overline{BW3}$ controls DQ17-DQ24, and $\overline{BW4}$ controls DQ25-DQ32, conditioned by $\overline{BWE}$ being LOW. $\overline{GW}$ LOW causes all bytes to be written. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE as controlled solely by $\overline{OE}$ to improve cache system response. The device incorporates an additional pipelined enable register to allow depth expansion without penalizing system performance.

The "L" version of this device has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below VCC MIN (3.1V), it will retain data with a minimum of power dissipation.

The MT58LC32K32C4 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V-tolerant. The device is ideally suited for Pentium™ and PowerPC™ pipelined systems and systems that benefit from a very wide high-speed data bus.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0-A14	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when $\overline{BWE}$ is LOW and must meet the setup and hold times around the rising edge of CLK. A Byte Write Enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW1}$ controls DQ1-DQ8. $\overline{BW2}$ controls DQ9-DQ16. $\overline{BW3}$ controls DQ17-DQ24 . $\overline{BW4}$ controls DQ25-DQ32. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

NEW ■ SYNCHRONOUS SRAM

PIN DESCRIPTIONS (continued)

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
87	$\overline{BWE}$	Input	Byte Write Enable: This active low input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
88	$\overline{GW}$	Input	Global Write: This active low input allows a full 32-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BWn}$ lines and must meet the setup and hold times around the rising edge of CLK.
1, 14, 16, 30, 38, 39, 42, 43, 49, 50, 51, 64, 66, 80	NC	-	No Connect: These signals are not internally connected.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ1-DQ32	Input/ Output	SRAM Data I/O: Byte 1 is DQ1-DQ8; Byte 2 is DQ9-DQ16; Byte 3 is DQ17-DQ24; Byte 4 is DQ25-DQ32. Input data must meet setup and hold times around the rising edge of CLK.
31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
17, 40, 67, 90	Vss	Supply	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%
5, 10, 21, 26, 55, 60, 71, 76	VssQ	Supply	Isolated Output Buffer Ground: GND

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{BWs}$	OPERATION	$\overline{CE}$	$\overline{BWs}$	$\overline{OE}$	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L[2,3]	Initiate READ cycle Register A(n), Q = D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L[2,3]	No new cycle Q = D(n-1)	H	H	L	No carry-over from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L[2,3]	No new cycle Q = HIGH-Z	H	H	H	No carry-over from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1), data = D(n-1)	One L[2]	No new cycle Q = D(n-1) for one byte	H	H	L	No carry-over from previous cycle

NOTE: 1. Previous cycle may be either BURST or NONBURST cycle.
2. $\overline{BWE}$ is LOW when one or more $\overline{BWn}$ is LOW.
3. $\overline{GW}$ LOW will yield identical results.

INTERLEAVED BURST ADDRESS TABLE (MODE = NC)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = GND)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR WRITEs

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte 1	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

NOTE: Using $\overline{BWE}$ and $\overline{BW1}$ through $\overline{BW4}$, any one or more bytes may be written.

NEW ■ SYNCHRONOUS SRAM

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW1}$ enables WRITEs to Byte 1 (DQ1-DQ8). $\overline{BW2}$ enables WRITEs to Byte 2 (DQ9-DQ16). $\overline{BW3}$ enables WRITEs to Byte 3 (DQ17-DQ24). $\overline{BW4}$ enables WRITEs to Byte 4 (DQ25-DQ32).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +150°C
Junction Temperature** ..... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	14
Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1, 11
Supply Voltage		V_{CC}	3.1	3.5	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-4.5	-5	-6	-7	-8	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; Vcc = MAX; outputs open	I_{CC}	ALL	180	425	360	315	270	225	mA	3, 12, 13
Power Supply Current: Idle	Device selected; Vcc = MAX; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{GW}$, $\overline{BWs}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; cycle time ≥ ^tKC MIN	I_{CC1}	ALL	30	65	60	55	50	45	mA	12, 13
CMOS Standby	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0	I_{SB2}	STD	0.5	5	5	5	5	5	mA	12, 13
			P	0.2	2	2	2	2	2	mA	
TTL Standby	Device deselected; Vcc = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB3}	STD	15	25	25	25	25	25	mA	12, 13
			P	8	18	18	18	18	18	mA	
Clock Running	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB4}	ALL	30	65	60	55	50	45	mA	12, 13

NEW ■ SYNCHRONOUS SRAM

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	Vcc = 3.3V	C_O	6	7	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air, Soldered on 4.25 x	θ_{JA}	20	°C/W	
Thermal resistance - Junction to Case	1.125 inch 4-layer circuit board	θ_{JC}	1	°C/W	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±5%)

DESCRIPTION		-4.5		-5		-6		-7		-8			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock													
Clock cycle time	^tKC	8		10		12		15		20		ns	
Clock HIGH time	^tKH	3		4		4.5		5		6		ns	
Clock LOW time	^tKL	3		4		4.5		5		6		ns	
Output Times													
Clock to output valid	^tKQ		4.5		5		6		7		8	ns	
Clock to output invalid	^tKQX	2		2		2		2		2		ns	
Clock to output in Low-Z	^tKQLZ	4		4		5		5		5		ns	6, 7
Clock to output in High-Z	^tKQHZ		4.5		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		4.5		5		5		5		6	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		3		4		5		6		6	ns	6, 7
Setup Times													
Address	^tAS	2.5		2.5		2.5		2.5		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSS	2.5		2.5		2.5		2.5		3		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAS	2.5		2.5		2.5		2.5		3		ns	8, 10
Write Signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	^tWS	2.5		2.5		2.5		2.5		3		ns	8, 10
Data-in	^tDS	2.5		2.5		2.5		2.5		3		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCES	2.5		2.5		2.5		2.5		3		ns	8, 10
Hold Times													
Address	^tAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Write Signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	^tWH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCEH	0.5		0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

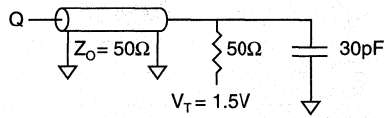


Fig. 1 OUTPUT LOAD EQUIVALENT

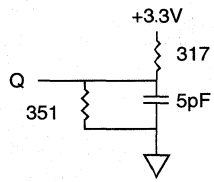


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

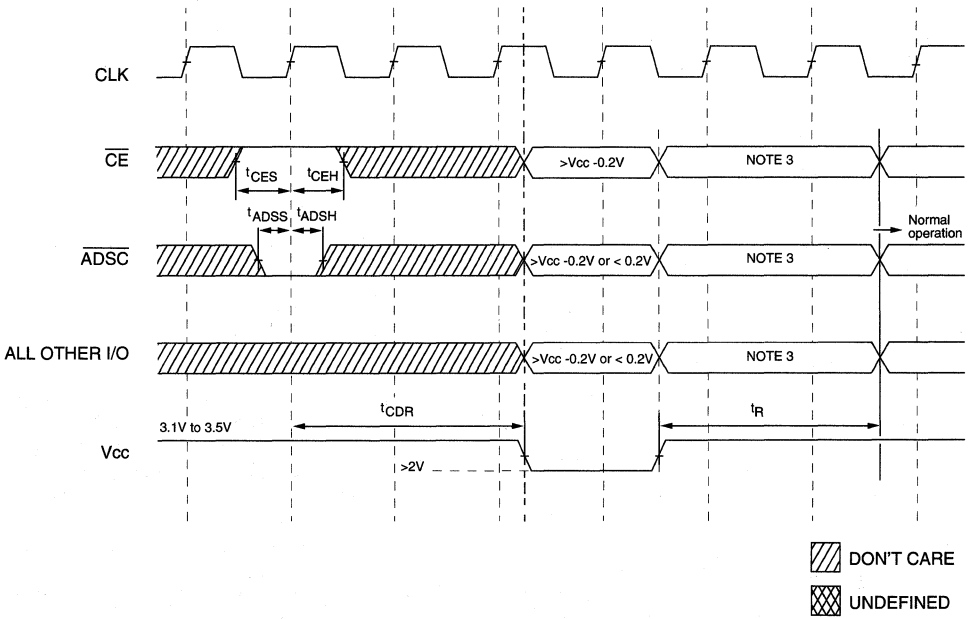
1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200ms$
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ($\overline{ADSC}$ or $\overline{ADV}$ LOW) or $\overline{ADSP}$ LOW for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
15. Typical values are measured at 25°C.
16. The device must have a deselect cycle applied at least two clock cycles before data retention mode is entered.

NEW ■ SYNCHRONOUS SRAM

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

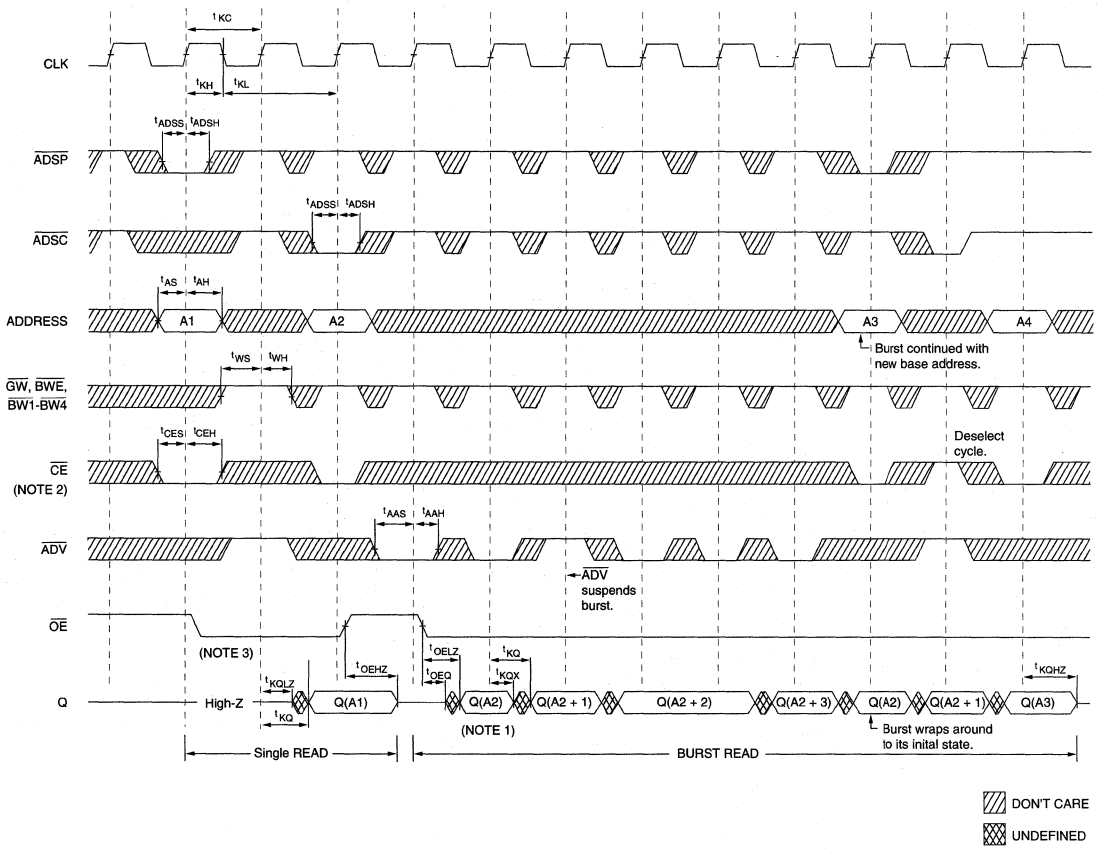
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2} \geq (V_{CC} - 0.2V)$, $CE2 \leq 0.2V$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$ $V_{CC} = 2V$	I_{CCDR}		TBD	µA	15
Chip Deselect to Data Retention Time		^tCDR	2 ^tKC		ns	4, 16
Operation Recovery Time		^tR	2 ^tKC		ns	4

LOW V_{CC} DATA RETENTION WAVEFORM



NOTE:
1. All inputs must be ≥ V_{CC} - 0.2V or ≤ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded.
2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.
3. The device control signals should be in a deselect state between the rising edge of V_{CC} and until ^tR is met.

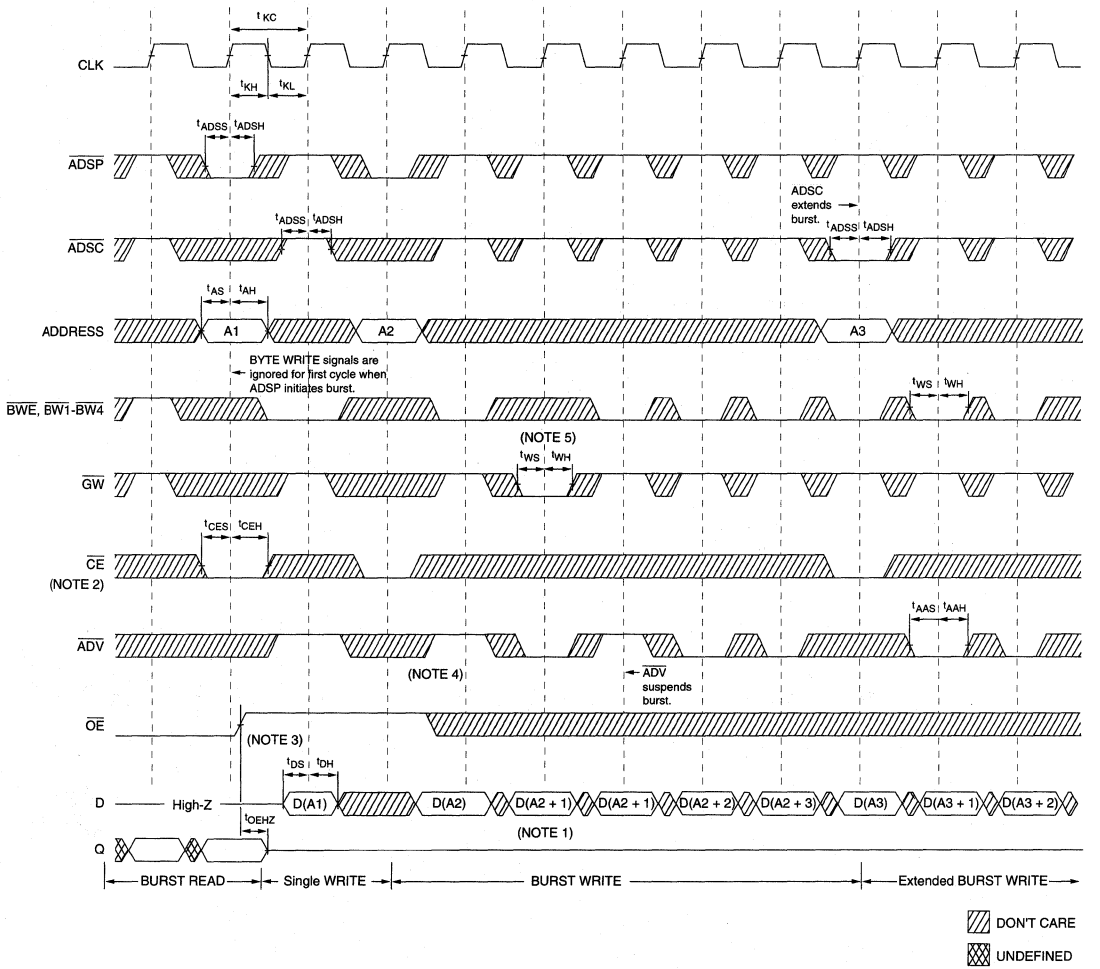
READ TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

NEW SYNCHRONOUS SRAM

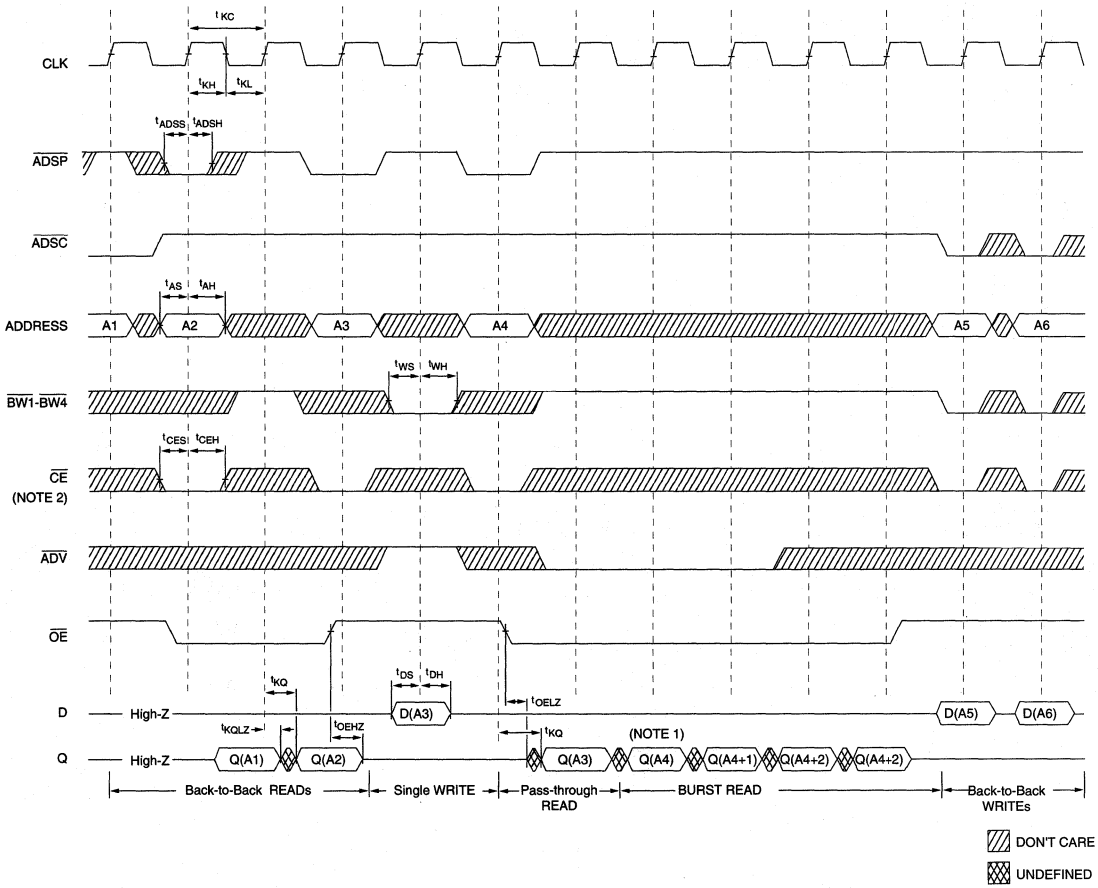
WRITE TIMING



NOTE:

1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.
5. Full width WRITE can be initiated by $\overline{GW}$ LOW or $\overline{GW}$ HIGH and $\overline{BWE}$, $\overline{BW1}$- $\overline{BW4}$ LOW.

READ/WRITE TIMING



NOTE:
1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{ADSP}$, $\overline{ADSC}$ or $\overline{ADV}$ cycle is performed.
4. $\overline{GW}$ is HIGH.
5. Back-to-back READs may be controlled by either $\overline{ADSP}$ or $\overline{ADSC}$.

APPLICATION INFORMATION

LOAD DERATING CURVES

The Micron 32K x 32SyncBurst SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

$\Delta^tKQ = 0.016$ ns/pF x ΔC_L pF.
(Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8pF (8pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device is a 12ns part, the worst case ^tKQ becomes 11.87ns (approximately).

Consult the factory for copies of I/O current versus voltage curves and capacitive loading derating curves.

DEPTH EXPANSION

The Micron 32K x 32 SyncBurst SRAM incorporates two additional chip enables to facilitate simple depth expansion. As shown in Figure 3, this permits easy cache upgrades from 32K depth to 64K depth with no extra logic. The chip enables are pipelined to allow contention-free transition between Micron devices which are physically and electrically close together.

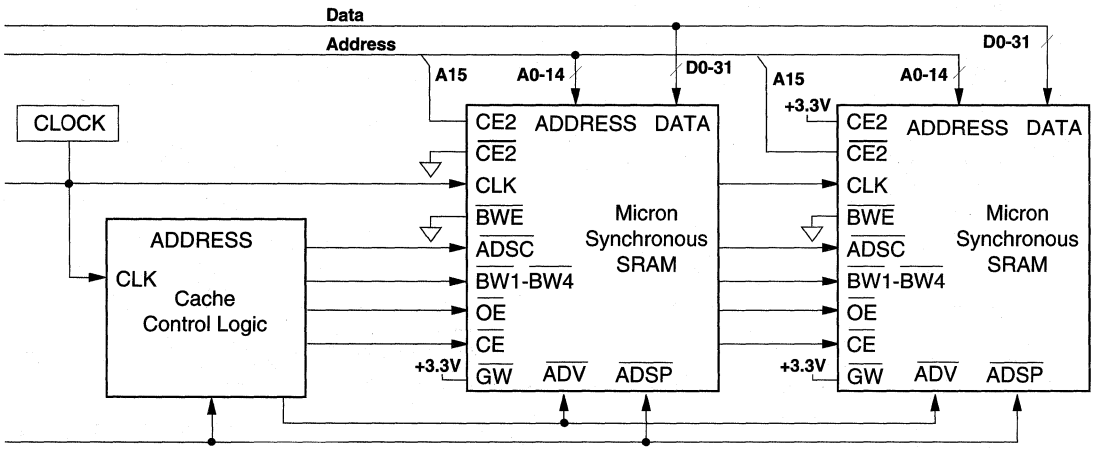


Figure 3
DEPTH EXPANSION FROM 32K x 32 TO 64K x 32

APPLICATION EXAMPLES

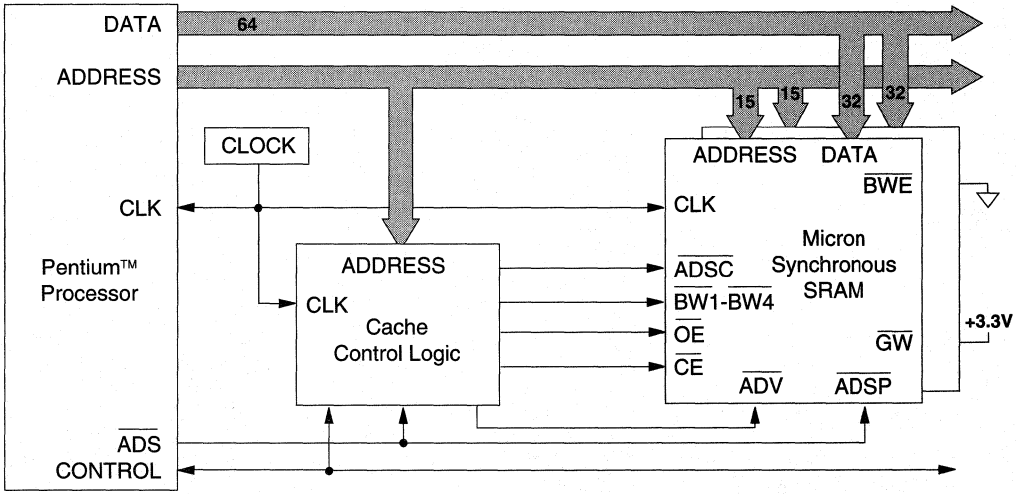


Figure 4
256K BYTE SECONDARY CACHE WITH INTERLEAVED BURST FOR 66 MHz PENTIUM™ USING TWO MT58LC32K32B2LG-9 SYNCBURST SRAMs

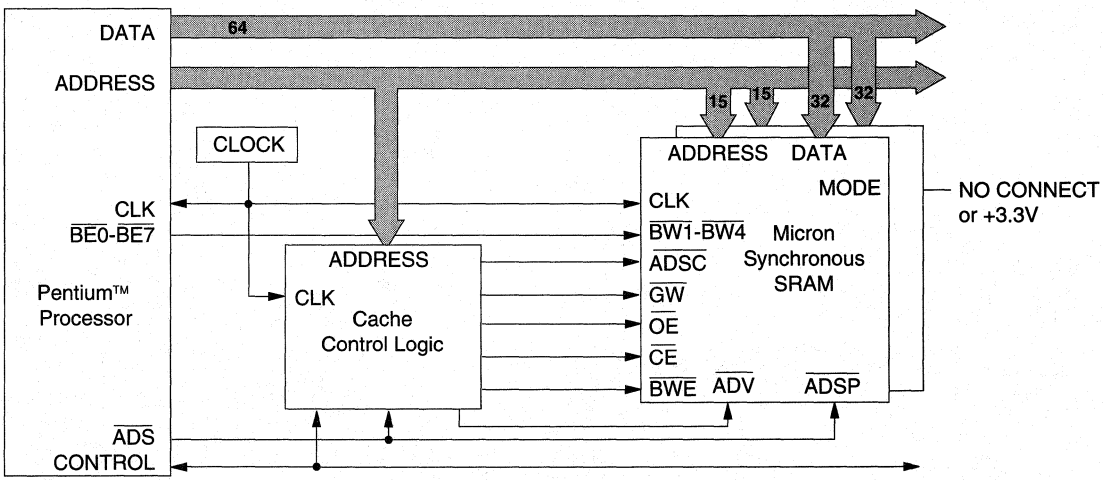


Figure 5
256K BYTE SECONDARY CACHE WITH INTERLEAVED BURST AND DIRECT CONNECTION OF BE# LINES TO SYNCBURST SRAM

SYNCHRONOUS SRAM

32K x 36 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS, BURST COUNTER

FEATURES

- Fast access times: 9, 10, 11, 12 and 14ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Burst control pins (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- DIMMs also available

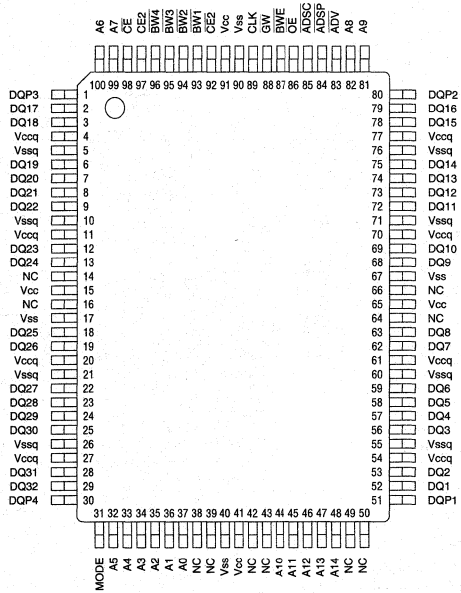
OPTIONS

	MARKING
• Timing	
9ns access/15ns cycle	- 9
10ns access/15ns cycle	-10
11ns access/15ns cycle	-11
12ns access/20ns cycle	-12
14ns access/20ns cycle	-14
• Packages	
100-pin TQFP	LG
• Low power	P
• 2V data retention, low power	L

• Part Number Example: MT58LC32K36B2LG-12 P

PIN ASSIGNMENT (Top View)

100-Pin TQFP
(SC-1)



GENERAL DESCRIPTION

The Micron SyncBurst™ SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC32K36B2 SRAM integrates a 32K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$) and global write ($\overline{GW}$).

Asynchronous inputs include the output enable ($\overline{OE}$), clock (CLK) and burst mode (MODE). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written.

SYNCHRONOUS SRAM

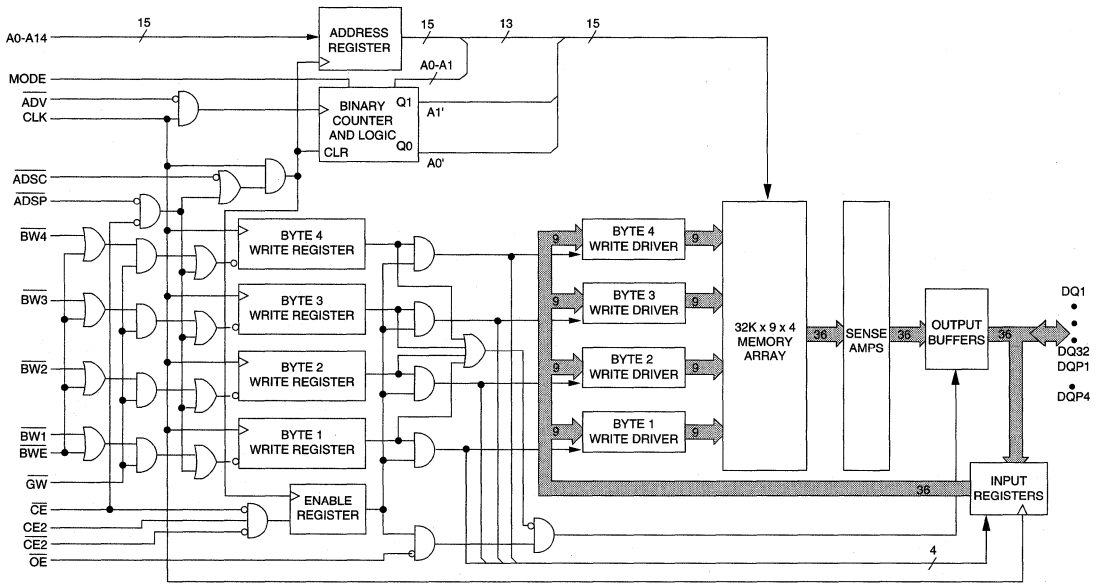
GENERAL DESCRIPTION (continued)

$\overline{BW1}$ controls DQ1-DQ8 and DQP1, $\overline{BW2}$ controls DQ9-DQ16 and DQP2, $\overline{BW3}$ controls DQ17-DQ24 and DQP3, and $\overline{BW4}$ controls DQ25-DQ32 and DQP4, conditioned by $\overline{BWE}$ being LOW. $\overline{GW}$ LOW causes all bytes to be written.

The "L" version of this device has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The MT58LC32K36B2 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V-tolerant. The device is ideally suited for 486, Pentium™, 680X0 and PowerPC™ systems and systems that benefit from a very wide data bus. The device is also ideal in generic 36- and 72-bit-wide applications.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0-A14	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when $\overline{BWE}$ is LOW and must meet the setup and hold times around the rising edge of CLK. A Byte Write Enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW1}$ controls DQ1-DQ8 and DQP1. $\overline{BW2}$ controls DQ9-DQ16 and DQP2. $\overline{BW3}$ controls DQ17-DQ24 and DQP3. $\overline{BW4}$ controls DQ25-DQ32 and DQP4. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

PIN DESCRIPTIONS (continued)

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
87	$\overline{BWE}$	Input	Byte Write Enable: This active low input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
88	$\overline{GW}$	Input	Global Write: This active low input allows a full 36-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BWn}$ lines and must meet the setup and hold times around the rising edge of CLK.
14, 16, 38, 39, 42, 43, 49, 50, 64, 66	NC	-	No Connect: These signals are not internally connected.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ1-DQ32	Input/ Output	SRAM Data I/O: Byte 1 is DQ1-DQ8; Byte 2 is DQ9-DQ16; Byte 3 is DQ17-DQ24; Byte 4 is DQ25-DQ32. Input data must meet setup and hold times around the rising edge of CLK.
51, 80, 1, 30	DQP1-DQP4	Input/ Output	Parity Data I/O: Byte 1 Parity is DQP1; Byte 2 Parity is DQP2; Byte 3 Parity is DQP3; Byte 4 Parity is DQP4.
31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
17, 40, 67, 90	Vss	Supply	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%
5, 10, 21, 26, 55, 60, 71, 76	VssQ	Supply	Isolated Output Buffer Ground: GND

INTERLEAVED BURST ADDRESS TABLE (MODE = NC)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = GND)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	ADV	WRITE	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW1}$ enables WRITEs to Byte 1 (DQ1-DQ8, DQP1). $\overline{BW2}$ enables WRITEs to Byte 2 (DQ9-DQ16, DQP2). $\overline{BW3}$ enables WRITEs to Byte 3 (DQ17-DQ24, DQP3). $\overline{BW4}$ enables WRITEs to Byte 4 (DQ25-DQ32, DQP4).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE FOR WRITEs

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte 1	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

NOTE: Using $\overline{BWE}$ and $\overline{BW1}$ through $\overline{BW4}$, any one or more bytes may be written.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +150°C
Junction Temperature** ..... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	14
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1, 11
Supply Voltage		V_{CC}	3.1	3.5	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-9	-10	-11	-12	-14	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; V_{CC} = MAX; outputs open	I_{CC}	ALL	200	300	300	275	250	250	mA	3, 12 13
Power Supply Current: Idle	Device selected; V_{CC} = MAX; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, $\overline{GW}$, $\overline{BW}$ ≥ V_{IH}; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; cycle time ≥ ^tKC MIN	I_{CC1}	ALL	28	45	45	45	40	40	mA	12, 13
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB2}	STD	0.5	5	5	5	5	5	mA	12, 13
			P	0.2	2	2	2	2	2	mA	
TTL Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB3}	STD	15	25	25	25	25	25	mA	12, 13
			P	8	18	18	18	18	18	mA	
Clock Running	Device deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB4}	ALL	30	50	50	50	45	45	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	V_{CC} = 3.3V	C_O	6	7	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air, Soldered on 4.25 x	θ_{JA}	20	°C/W	
Thermal resistance - Junction to Case	1.125 inch 4-layer circuit board	θ_{JC}	1	°C/W	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±5%)

DESCRIPTION		-9		-10		-11		-12		-14			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock													
Clock cycle time	^tKC	15		15		15		20		20		ns	
Clock HIGH time	^tKH	4		5		5		6		6		ns	
Clock LOW time	^tKL	4		5		5		6		6		ns	
Output Times													
Clock to output valid	^tKQ		9		10		11		12		14	ns	
Clock to output invalid	^tKQX	3		3		3		3		3		ns	
Clock to output in Low-Z	^tKQLZ	5		5		5		5		5		ns	6, 7
Clock to output in High-Z	^tKQHZ		5		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		5		5		5		6		6	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		5		5		5		6		6	ns	6, 7
Setup Times													
Address	^tAS	2.5		2.5		2.5		3		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSS	2.5		3		3		3		3		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAS	2.5		3		3		3		3		ns	8, 10
Write Signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	^tWS	2.5		3		3		3		3		ns	8, 10
Data-in	^tDS	2.5		3		3		3		3		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCES	2.5		3		3		3		3		ns	8, 10
Hold Times													
Address	^tAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Write Signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	^tWH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCEH	0.5		0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

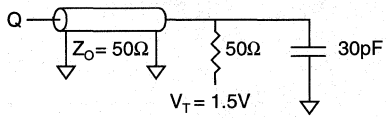


Fig. 1 OUTPUT LOAD EQUIVALENT

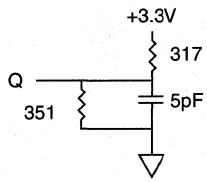


Fig. 2 OUTPUT LOAD EQUIVALENT

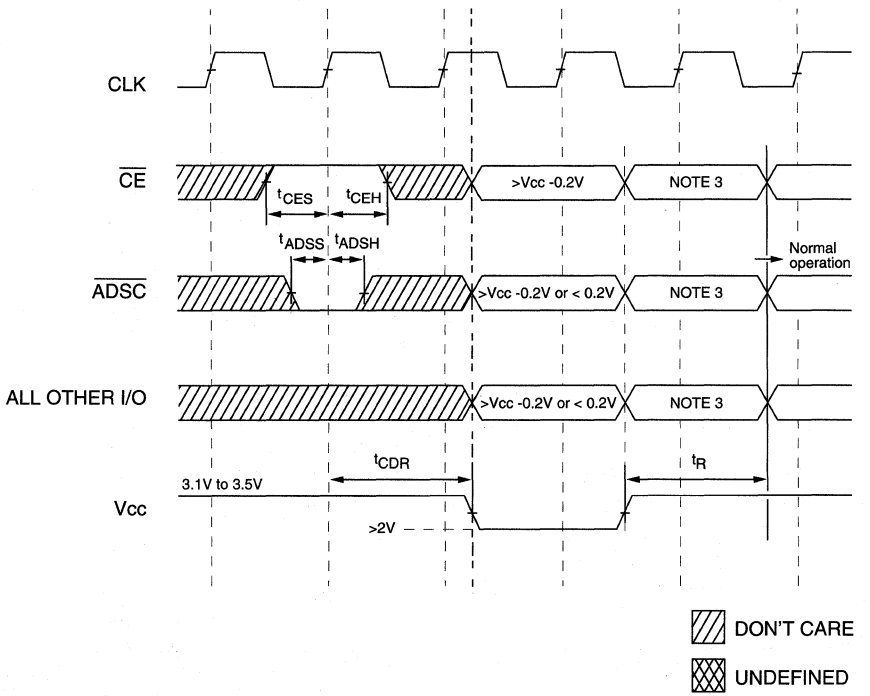
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200ms$
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ($\overline{ADSC}$ or $\overline{ADV}$ LOW) or $\overline{ADSP}$ LOW for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
15. Typical values are measured at 25°C.
16. The device must have a deselect cycle applied at least one clock cycle before data retention mode is entered.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

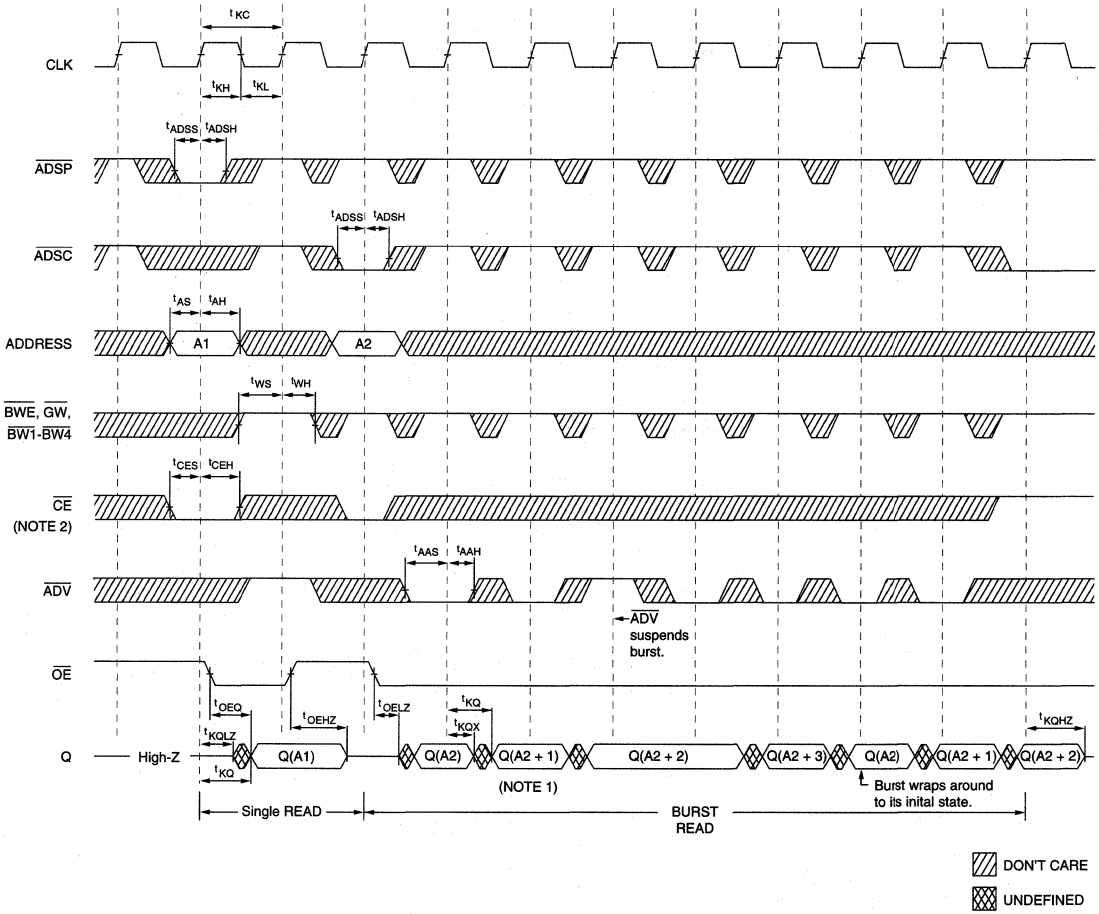
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2} \geq (V_{CC} - 0.2V)$, $CE2 \leq 0.2V$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$ $V_{CC} = 2V$	I_{CCDR}		TBD	µA	15
Chip Deselect to Data Retention Time		^tCDR	^tKC		ns	4, 16
Operation Recovery Time		^tR	^tKC		ns	4

LOW V_{CC} DATA RETENTION WAVEFORM



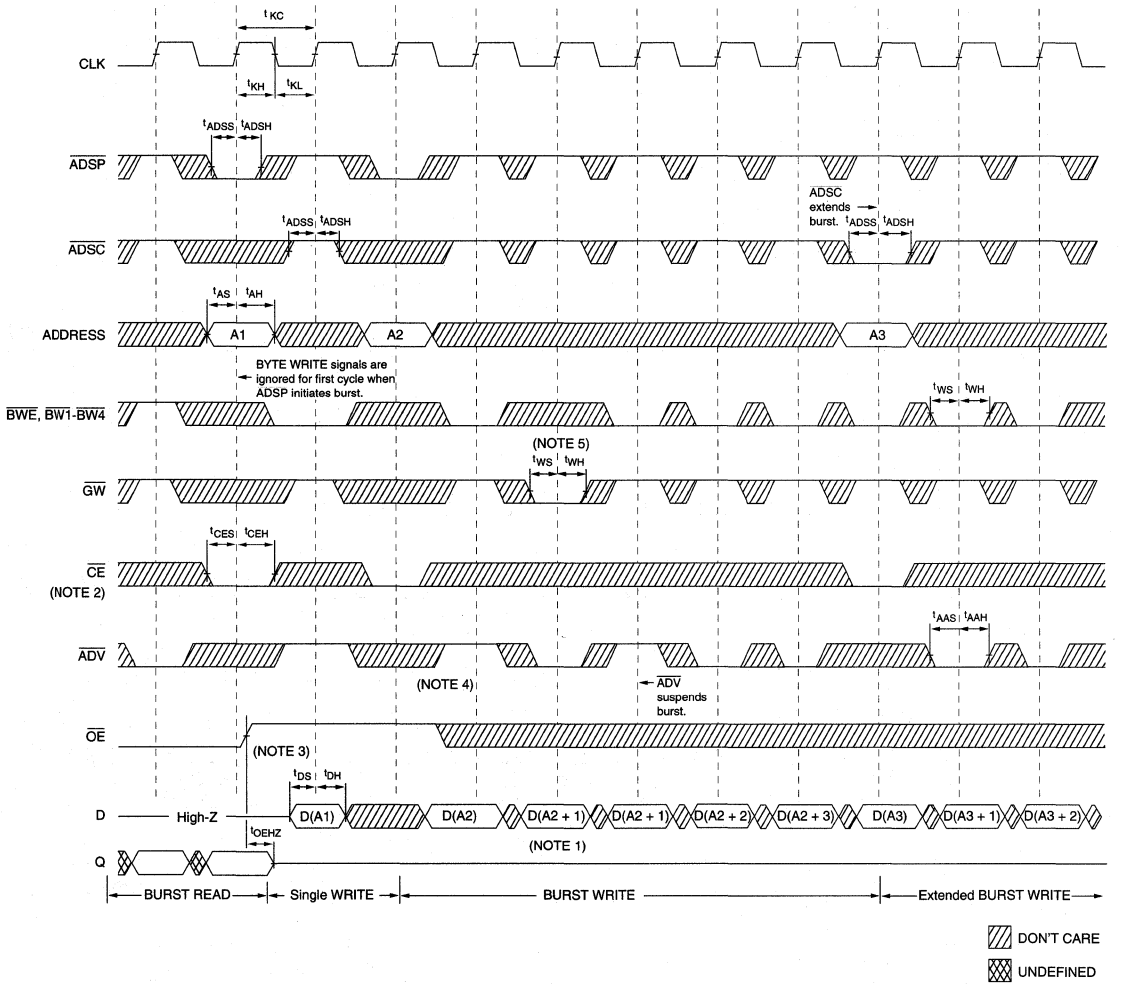
NOTE:
1. All inputs must be ≥ V_{CC} - 0.2V or ≤ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded.
2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.
3. The device control signals should be in a deselect state between the rising edge of V_{CC} and until ^tR is met.

READ TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

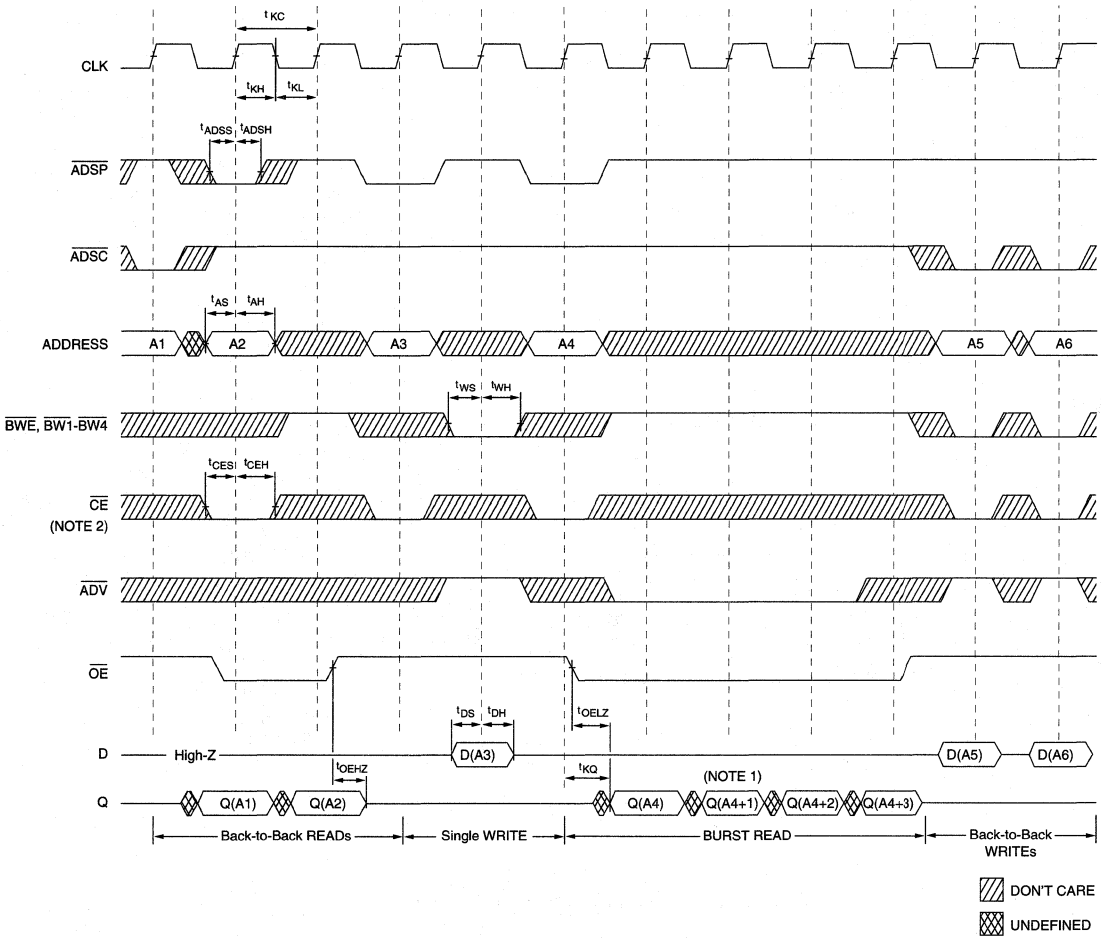
WRITE TIMING



NOTE:

1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.
5. Full width WRITE can be initiated by $\overline{GW}$ LOW or $\overline{GW}$ HIGH and $\overline{BWE}$, $\overline{BW1}$- $\overline{BW4}$ LOW.

READ/WRITE TIMING



NOTE:
1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{ADSP}$, $\overline{ADSC}$ or $\overline{ADV}$ cycle is performed.
4. $\overline{GW}$ is HIGH.

APPLICATION INFORMATION

LOAD DERATING CURVES

The Micron 32K x 36 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

$\Delta^{t}KQ = 0.016$ ns/pF x ΔC_L pF.
(Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8pF (8pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device is a 12ns part, the worst case ^{t}KQ becomes 11.87ns (approximately).

Consult the factory for copies of I/O current versus voltage curves and capacitive loading derating curves.

DEPTH EXPANSION

The Micron 32K x 36 Synchronous SRAM incorporates two additional chip enables to facilitate simple depth expansion. As shown in Figure 3, this permits easy cache upgrades from 32K depth to 64K depth with no extra logic.

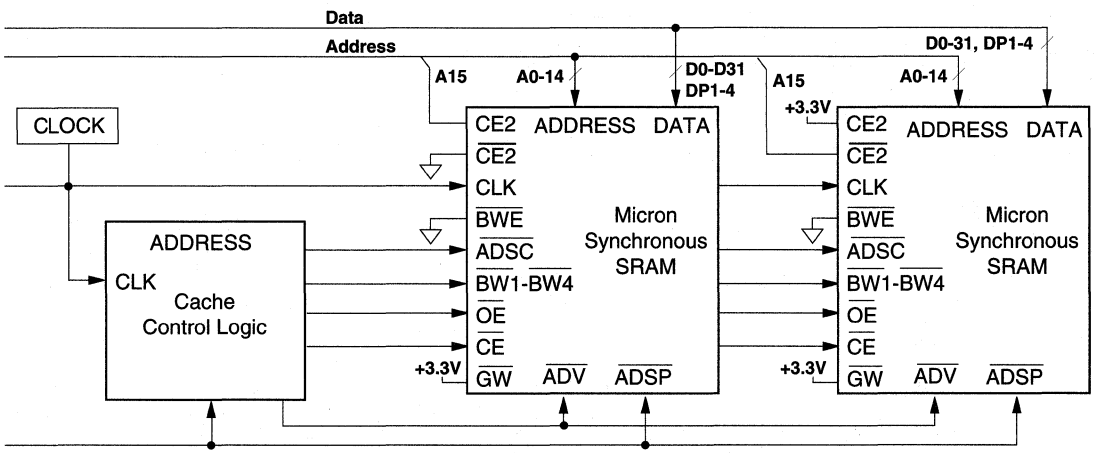


Figure 3
DEPTH EXPANSION FROM 32K x 36 TO 64K x 36

APPLICATION EXAMPLES

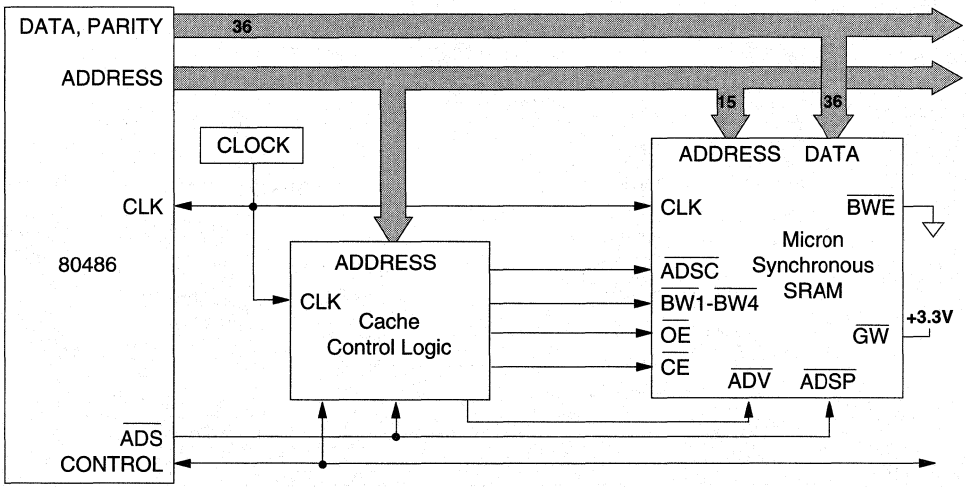


Figure 4
128K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz 80486 USING ONE MT58LC32K36B2LG-12 SYNCHRONOUS SRAM

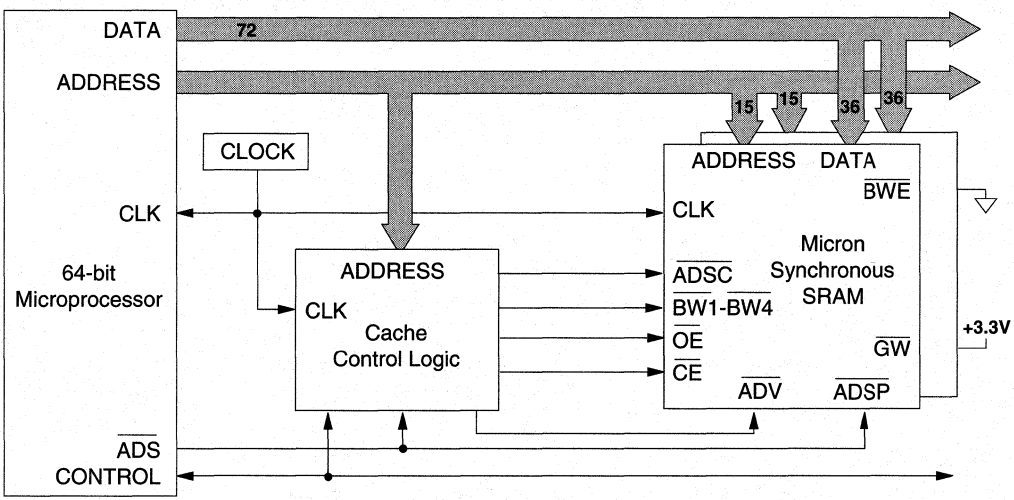


Figure 5
256K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 66 MHz PENTIUM USING TWO MT58LC32K36B2LG-9 SYNCHRONOUS SRAMs

APPLICATION EXAMPLES

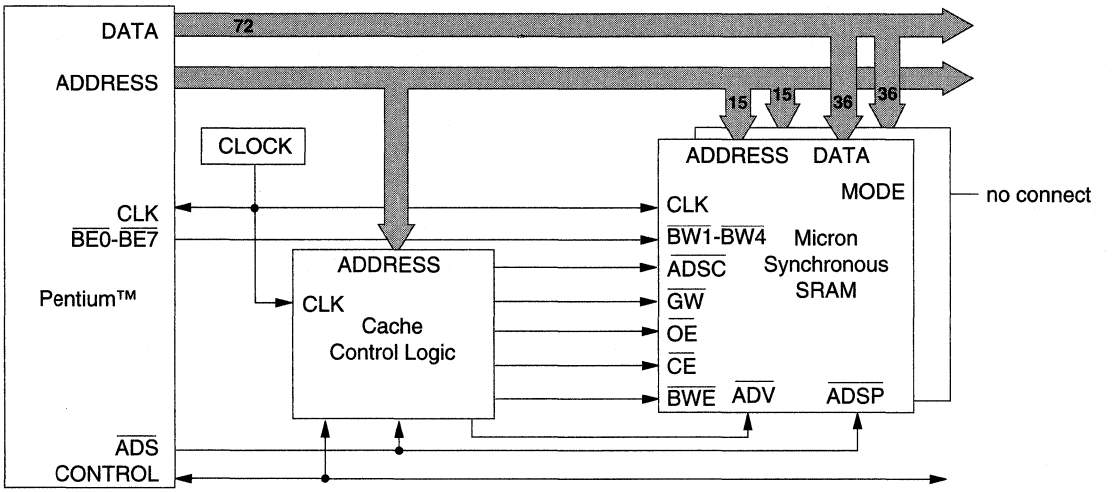


Figure 6
256K BYTE SECONDARY CACHE WITH PARITY, INTERLEAVED BURST AND DIRECT CONNECTION OF BE# LINES TO SYNCBURST SRAM

SYNCHRONOUS SRAM

32K x 36 SRAM

+3.3V SUPPLY, FULLY REGISTERED INPUTS AND OUTPUTS AND BURST COUNTER

FEATURES

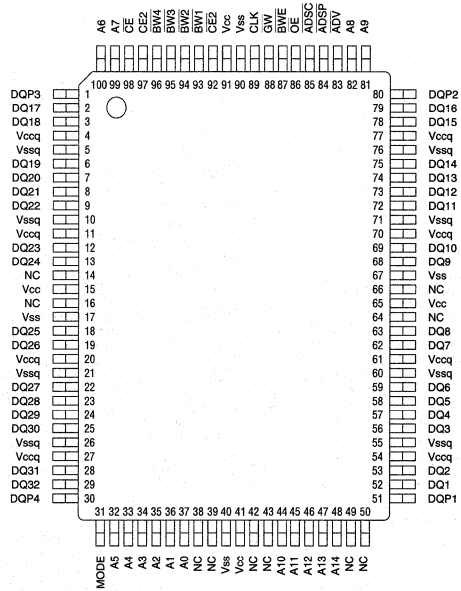
- Fast access times: 4.5, 5, 6, 7 and 8ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- WRITE pass-through capability
- Burst control pins (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- DIMMs also available

OPTIONS — MARKING

- Timing
  - 4.5ns access/8ns cycle — -4.5
  - 5ns access/10ns cycle — -5
  - 6ns access/12ns cycle — -6
  - 7ns access/15ns cycle — -7
  - 8ns access/20ns cycle — -8
- Packages
  - 100-pin TQFP — LG
- Low power — P
- 2V data retention, low power — L
- Part Number Example: MT58LC32K36C4LG-7 P

PIN ASSIGNMENT (Top View)

100-Pin TQFP
(SC-1)



GENERAL DESCRIPTION

The Micron SyncBurst™ SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC32K36C4 SRAM integrates a 32K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$) and global write ($\overline{GW}$).

Asynchronous inputs include the output enable ($\overline{OE}$), clock (CLK) and burst mode (MODE). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to four bytes wide as controlled by the write control inputs.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

SYNCHRONOUS SRAM

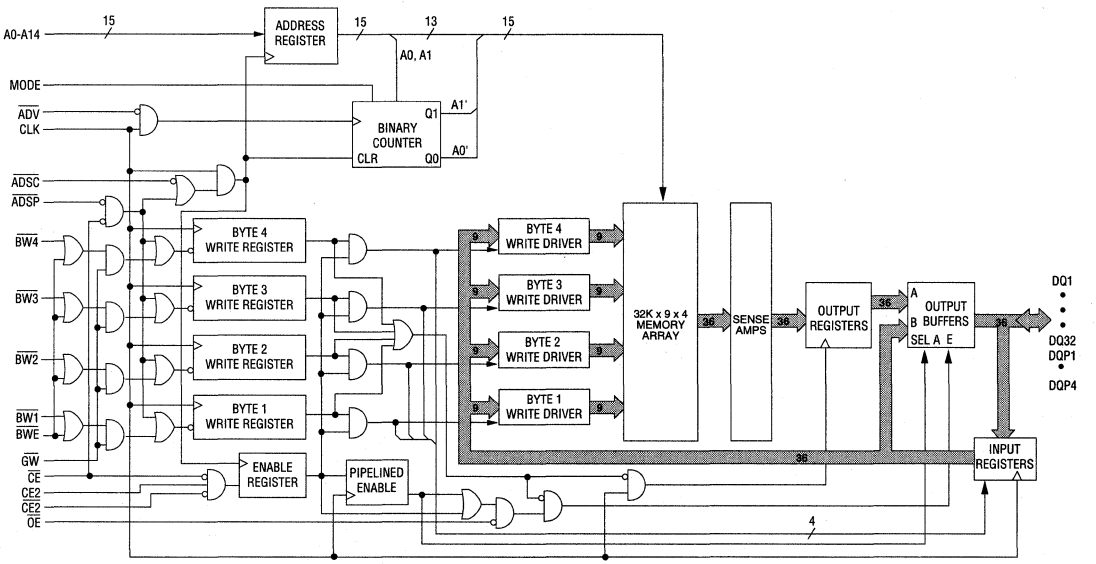
GENERAL DESCRIPTION (continued)

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQ1-DQ8 and DQP1, $\overline{BW2}$ controls DQ9-DQ16 and DQP2, $\overline{BW3}$ controls DQ17-DQ24 and DQP3, and $\overline{BW4}$ controls DQ25-DQ32 and DQP4, conditioned by $\overline{BWE}$ being LOW. $\overline{GW}$ LOW causes all bytes to be written. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE as controlled solely by $\overline{OE}$ to improve cache system response. The device incorporates an additional pipelined enable register to allow depth expansion without penalizing system performance.

The "L" version of this device has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The MT58LC32K36C4 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V-tolerant. The device is ideally suited for Pentium™ and PowerPC™ pipelined systems and systems that benefit from a very wide high-speed data bus.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0-A14	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when $\overline{WE}$ is LOW and must meet the setup and hold times around the rising edge of CLK. A Byte Write Enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW1}$ controls DQ1-DQ8 and DQP1. $\overline{BW2}$ controls DQ9-DQ16 and DQP2. $\overline{BW3}$ controls DQ17-DQ24 and DQP3. $\overline{BW4}$ controls DQ25-DQ32 and DQP4. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

PIN DESCRIPTIONS (continued)

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
87	$\overline{BWE}$	Input	Byte Write Enable: This active low input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
88	$\overline{GW}$	Input	Global Write: This active low input allows a full 36-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BWn}$ lines and must meet the setup and hold times around the rising edge of CLK.
14, 16, 38, 39, 42, 43, 49, 50, 64, 66	NC	-	No Connect: These signals are not internally connected.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ1-DQ32	Input/ Output	SRAM Data I/O: Byte 1 is DQ1-DQ8; Byte 2 is DQ9-DQ16; Byte 3 is DQ17-DQ24; Byte 4 is DQ25-DQ32. Input data must meet setup and hold times around the rising edge of CLK.
51, 80, 1, 30	DQP1-DQP4	Input/ Output	Parity Data I/O: Byte 1 Parity is DQP1; Byte 2 Parity is DQP2; Byte 3 Parity is DQP3; Byte 4 Parity is DQP4.
31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
17, 40, 67, 90	Vss	Supply	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%
5, 10, 21, 26, 55, 60, 71, 76	VssQ	Supply	Isolated Output Buffer Ground: GND

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{BWs}$	OPERATION	$\overline{CE}$	$\overline{BWs}$	$\overline{OE}$	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L[2,3]	Initiate READ cycle Register A(n), Q = D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L[2,3]	No new cycle Q = D(n-1)	H	H	L	No carry-over from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L[2,3]	No new cycle Q = HIGH-Z	H	H	H	No carry-over from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1), data = D(n-1)	One L[2]	No new cycle Q = D(n-1) for one byte	H	H	L	No carry-over from previous cycle

NOTE: 1. Previous cycle may be either BURST or NONBURST cycle.
2. $\overline{BWE}$ is LOW when one or more $\overline{BWn}$ is LOW.
3. $\overline{GW}$ LOW will yield identical results.

INTERLEAVED BURST ADDRESS TABLE (MODE = NC)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = GND)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR WRITEs

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte 1	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

NOTE: Using $\overline{BWE}$ and $\overline{BW1}$ through $\overline{BW4}$, any one or more bytes may be written.

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$) and $\overline{BWE}$ are LOW or $\overline{GW}$ is LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW1}$ enables WRITEs to Byte 1 (DQ1-DQ8, DQP1). $\overline{BW2}$ enables WRITEs to Byte 2 (DQ9-DQ16, DQP2). $\overline{BW3}$ enables WRITEs to Byte 3 (DQ17-DQ24, DQP3). $\overline{BW4}$ enables WRITEs to Byte 4 (DQ25-DQ32, DQP4).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a WRITE operation following a READ operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and $\overline{BWE}$ LOW or $\overline{GW}$ LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +150°C
Junction Temperature** ..... +150°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	14
Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1, 11
Supply Voltage		V_{CC}	3.1	3.5	V	1

					MAX						
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-4.5	-5	-6	-7	-8	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; Vcc = MAX; outputs open	I_{CC}	ALL	200	475	400	350	300	250	mA	3, 12, 13
Power Supply Current: Idle	Device selected; Vcc = MAX; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{GW}$, $\overline{BW}$s, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; cycle time ≥ ^tKC MIN	I_{CC1}	ALL	30	65	60	55	50	45	mA	12, 13
CMOS Standby	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0	I_{SB2}	STD	0.5	5	5	5	5	5	mA	12, 13
			P	0.2	2	2	2	2	2	mA	
TTL Standby	Device deselected; Vcc = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB3}	STD	15	25	25	25	25	25	mA	12, 13
			P	8	18	18	18	18	18	mA	
Clock Running	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB4}	ALL	30	65	60	55	50	45	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	Vcc = 3.3V	C_O	6	7	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air, Soldered on 4.25 x	θ_{JA}	20	°C/W	
Thermal resistance - Junction to Case	1.125 inch 4-layer circuit board	θ_{JC}	1	°C/W	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±5%)

DESCRIPTION		-4.5		-5		-6		-7		-8			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock													
Clock cycle time	tKC	8		10		12		15		20		ns	
Clock HIGH time	tKH	3		4		4.5		5		6		ns	
Clock LOW time	tKL	3		4		4.5		5		6		ns	
Output Times													
Clock to output valid	tKQ		4.5		5		6		7		8	ns	
Clock to output invalid	tKQX	2		2		2		2		2		ns	
Clock to output in Low-Z	tKQLZ	4		4		5		5		5		ns	6, 7
Clock to output in High-Z	tKQHZ		4.5		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	tOEQ		4.5		5		5		5		6	ns	9
$\overline{OE}$ to output in Low-Z	tOELZ	0		0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	tOEHZ		3		4		5		6		6	ns	6, 7
Setup Times													
Address	tAS	2.5		2.5		2.5		2.5		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	tADSS	2.5		2.5		2.5		2.5		3		ns	8, 10
Address Advance ($\overline{ADV}$)	tAAS	2.5		2.5		2.5		2.5		3		ns	8, 10
Write Signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	tWS	2.5		2.5		2.5		2.5		3		ns	8, 10
Data-in	tDS	2.5		2.5		2.5		2.5		3		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	tCES	2.5		2.5		2.5		2.5		3		ns	8, 10
Hold Times													
Address	tAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	tADSH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	tAAH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Write Signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$, $\overline{BWE}$, $\overline{GW}$)	tWH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Data-in	tDH	0.5		0.5		0.5		0.5		0.5		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	tCEH	0.5		0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

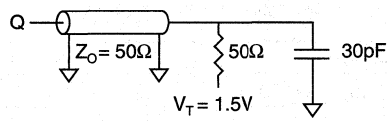


Fig. 1 OUTPUT LOAD EQUIVALENT

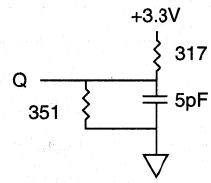


Fig. 2 OUTPUT LOAD EQUIVALENT

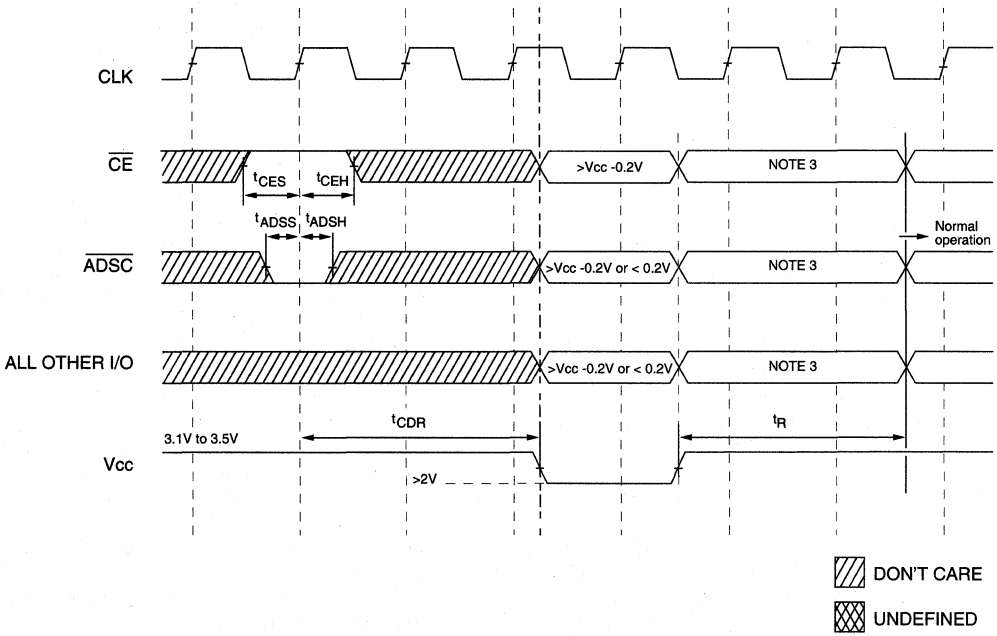
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200ms$
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ($\overline{ADSC}$ or $\overline{ADV}$ LOW) or $\overline{ADSP}$ LOW for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
15. Typical values are measured at 25°C.
16. The device must have a deselect cycle applied at least two clock cycles before data retention mode is entered.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

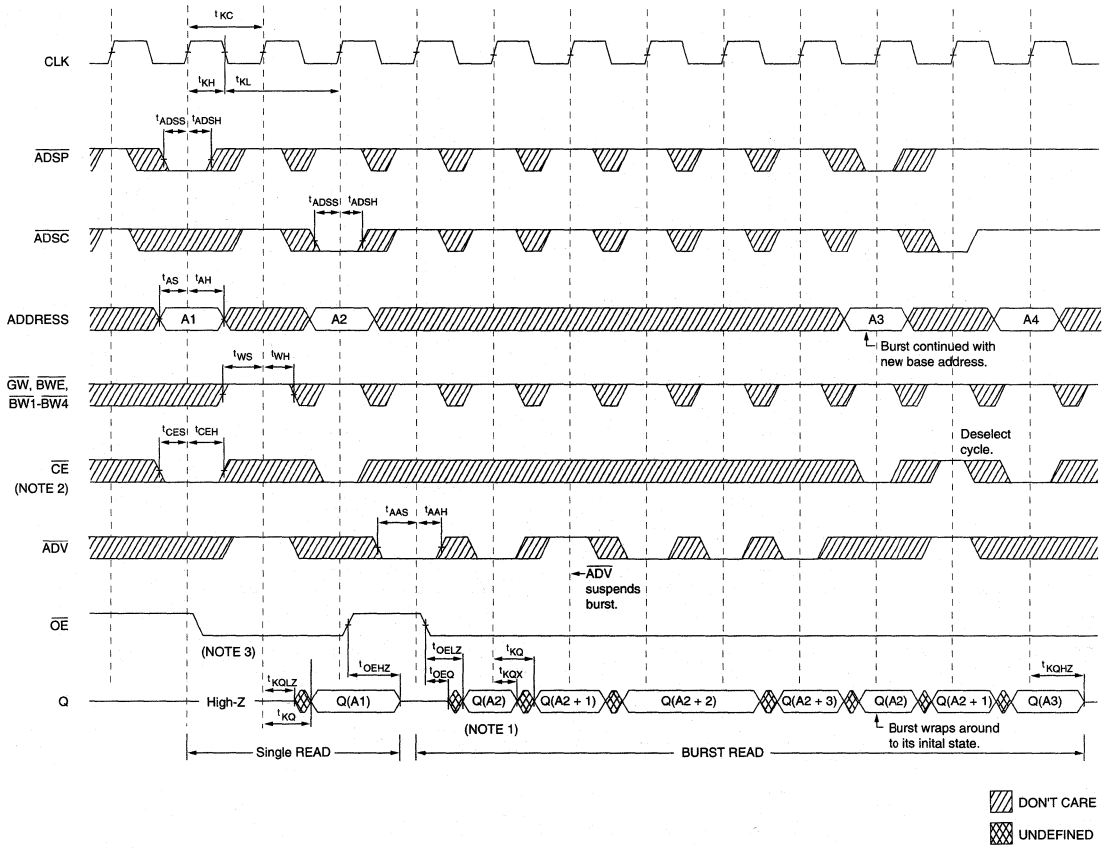
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2}$ ≥ (Vcc -0.2V), CE2 ≤ 0.2V VIN ≥ (Vcc -0.2V) or ≤ 0.2V Vcc = 2V	I_{CCDR}		TBD	µA	15
Chip Deselect to Data Retention Time		^tCDR	2 ^tKC		ns	4, 16
Operation Recovery Time		^tR	2 ^tKC		ns	4

LOW Vcc DATA RETENTION WAVEFORM



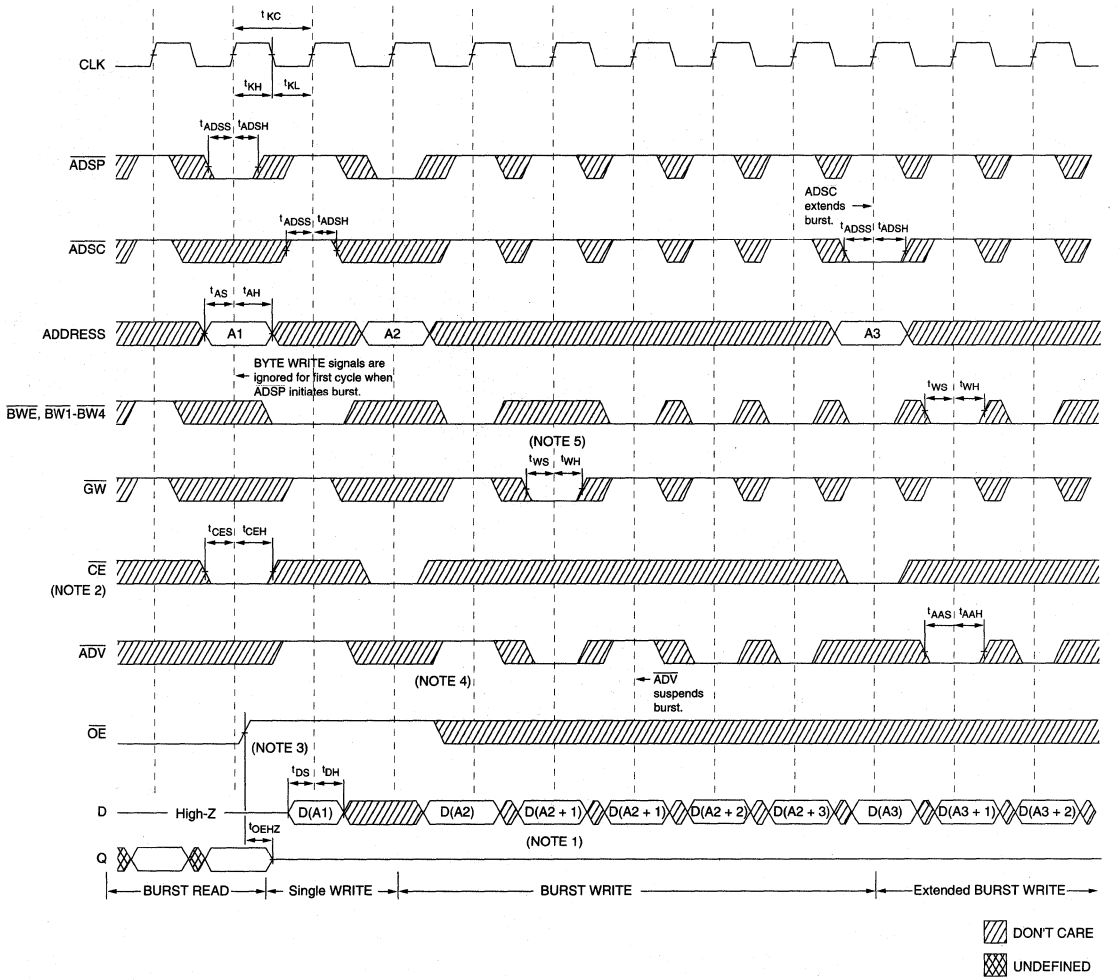
NOTE:
1. All inputs must be ≥ Vcc - 0.2V or ≤ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded.
2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.
3. The device control signals should be in a deselect state between the rising edge of Vcc and until ^tR is met.

READ TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

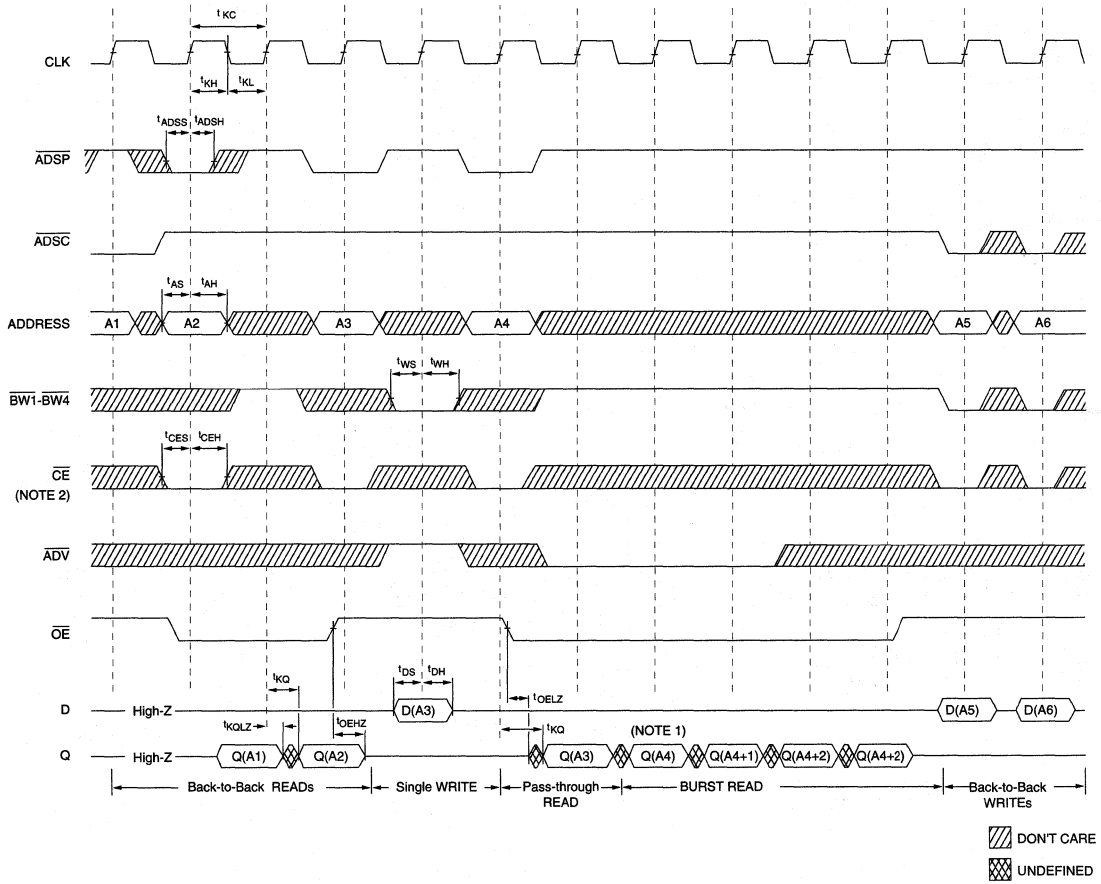
WRITE TIMING



NOTE:

1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.
5. Full width WRITE can be initiated by $\overline{GW}$ LOW or $\overline{GW}$ HIGH and $\overline{BWE}$, $\overline{BW1}$- $\overline{BW4}$ LOW.

READ/WRITE TIMING



NOTE:
1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{ADSP}$, $\overline{ADSC}$ or $\overline{ADV}$ cycle is performed.
4. $\overline{GW}$ is HIGH.
5. Back-to-back READs may be controlled by either $\overline{ADSP}$ or $\overline{ADSC}$.

APPLICATION INFORMATION

LOAD DERATING CURVES

The Micron 32K x 36 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

$\Delta^{t}KQ = 0.016$ ns/pF x ΔC_L pF.
(Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8pF (8pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device is a 12ns part, the worst case ^{t}KQ becomes 11.87ns (approximately).

Consult the factory for copies of I/O current versus voltage curves and capacitive loading derating curves.

DEPTH EXPANSION

The Micron 32K x 36 Synchronous SRAM incorporates two additional chip enables to facilitate simple depth expansion. As shown in Figure 3, this permits easy cache upgrades from 32K depth to 64K depth with no extra logic. The chip enables are pipelined to allow contention-free transition between Micron devices which are physically and electrically close together.

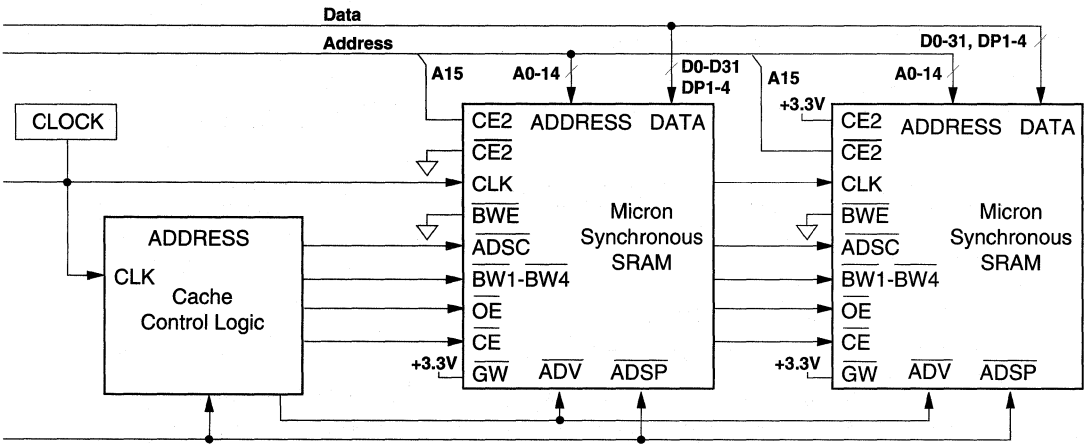


Figure 3
DEPTH EXPANSION FROM 32K x 36 TO 64K x 36

APPLICATION EXAMPLES

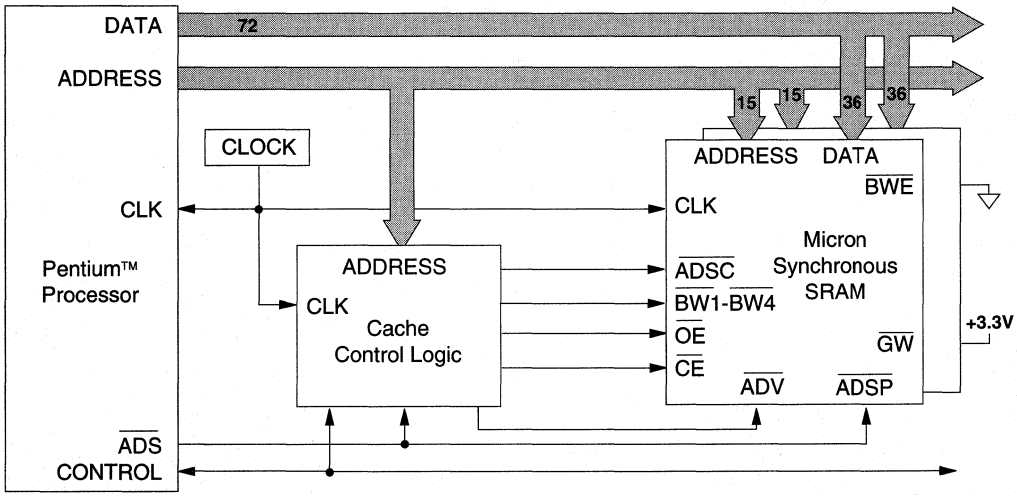


Figure 4
256K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 66 MHz PENTIUM USING TWO MT58LC32K36B2LG-9 SYNCHRONOUS SRAMs

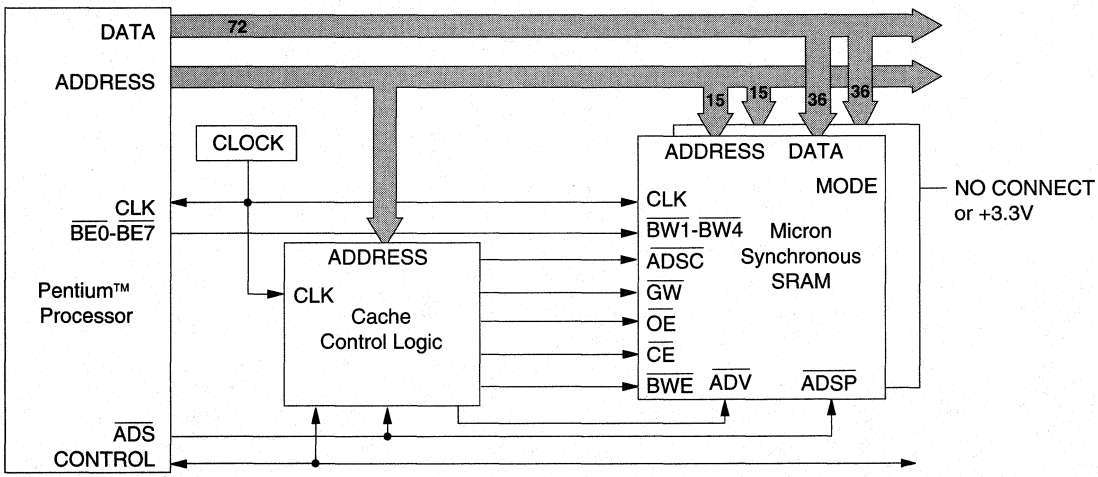


Figure 5
256K BYTE SECONDARY CACHE WITH PARITY, INTERLEAVED BURST AND DIRECT CONNECTION OF BE# LINES TO SYNCBURST SRAM

MICRON
SEMICONDUCTOR, INC.

SRAM MODULE PRODUCT SELECTION GUIDE

Memory Configuration	Control Functions	Part Number	Access Time (ns)	Package and No. of Pins			Page
				ZIP	SIMM	DIMM	
64K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S6432	12, 15, 20, 25	64	64	-	4-1
64K x 32	$\overline{CE}$ and $\overline{OE}$	MT8LS6432	15, 20, 25	64	64	-	4-9
128K x 32	$\overline{CE}$ and $\overline{OE}$	MT4S12832	15, 20, 25	64	64	-	4-17
128K x 32	$\overline{CE}$ and $\overline{OE}$	MT4LS12832	17, 20, 25	64	64	-	4-25
256K x 32	$\overline{CE}$ and $\overline{OE}$	MT8S25632	15, 20, 25	64	64	-	4-33
256K x 32	$\overline{CE}$ and $\overline{OE}$	MT8LS25632	17, 20, 25	64	64	-	4-41
1 Meg x 32	$\overline{CE}$ and $\overline{OE}$	MT8LS132	15, 20, 25, 35	72	72	-	4-49
32K x 64	SyncBurst™, Linear Burst	MT2LSYT3264T1	9, 10, 11, 12	-	-	160	4-57
32K x 64	SyncBurst, Interleaved Burst	MT2LSYT3264T2	9, 10, 11, 12	-	-	160	4-57
32K x 64	SyncBurst, Interleaved Burst, Pipelined	MT2LSYT3264T4	5, 6, 7, 8	-	-	160	4-69
32K x 64	SyncBurst, Linear Burst, Pipelined	MT2LSYT3264T6	5, 6, 7, 8	-	-	160	4-69
32K x 64	SyncBurst, Linear/Interleaved Burst	MT2LSYT3264B2	9, 10, 11, 12	-	-	160	4-81
32K x 64	SyncBurst, Linear/ Interleaved Burst, Pipelined	MT2LSYT3264C4	5, 6, 7, 8	-	-	160	4-87
32K x 72	SyncBurst, Linear Burst	MT2LSYT3272T1	9, 10, 11, 12	-	-	160	4-93
32K x 72	SyncBurst, Interleaved Burst	MT2LSYT3272T2	9, 10, 11, 12	-	-	160	4-93
32K x 72	SyncBurst, Interleaved Burst, Pipelined	MT2LSYT3272T4	5, 6, 7, 8	-	-	160	4-107
32K x 72	SyncBurst, Linear Burst, Pipelined	MT2LSYT3272T6	5, 6, 7, 8	-	-	160	4-107
32K x 72	SyncBurst, Linear/ Interleaved Burst	MT2LSYT3272B2	9, 10, 11, 12	-	-	160	4-121
32K x 72	SyncBurst, Linear/ Interleaved Burst, Pipelined	MT2LSYT3272C4	5, 6, 7, 8	-	-	160	4-129
64K x 72	SyncBurst, Linear Burst	MT4LSY6472T1	9, 10, 11, 12	-	-	160	4-93
64K x 72	SyncBurst, Interleaved Burst	MT4LSY6472T2	9, 10, 11, 12	-	-	160	4-93
64K x 72	SyncBurst, Interleaved Burst, Pipelined	MT4LSY6472T4	5, 6, 7, 8	-	-	160	4-107
64K x 72	SyncBurst, Linear Burst, Pipelined	MT4LSY6472T6	5, 6, 7, 8	-	-	160	4-107
64K x 72	SyncBurst, Linear/ Interleaved Burst	MT4LSYT6472B2	9, 10, 11, 12	-	-	160	4-121
64K x 72	SyncBurst, Linear/ Interleaved Burst, Pipelined	MT4LSYT6472C4	5, 6, 7, 8	-	-	160	4-129

SRAM MODULE

64K x 32 SRAM

FEATURES

- High speed: 12, 15, 20 and 25ns
- High-performance, low-power CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Low profile
- Industry-standard pinout
- All inputs and outputs are TTL-compatible
- Upgradable with 128K x 32 and 256K x 32 modules

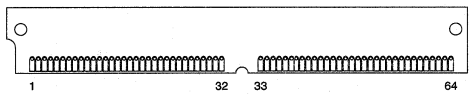
OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 64-pin SIMM — M
  - 64-pin ZIP — Z
- 2V data retention (optional) — L
- Low power (optional) — P
- Part Number Example: MT8S6432Z-15 P

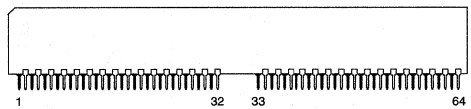
NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SE-1)



64-Pin ZIP
(SG-2)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT8S6432 is a high-speed SRAM memory module containing 65,536 words organized in a x32-bit configuration. The module consists of eight 64K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4 printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

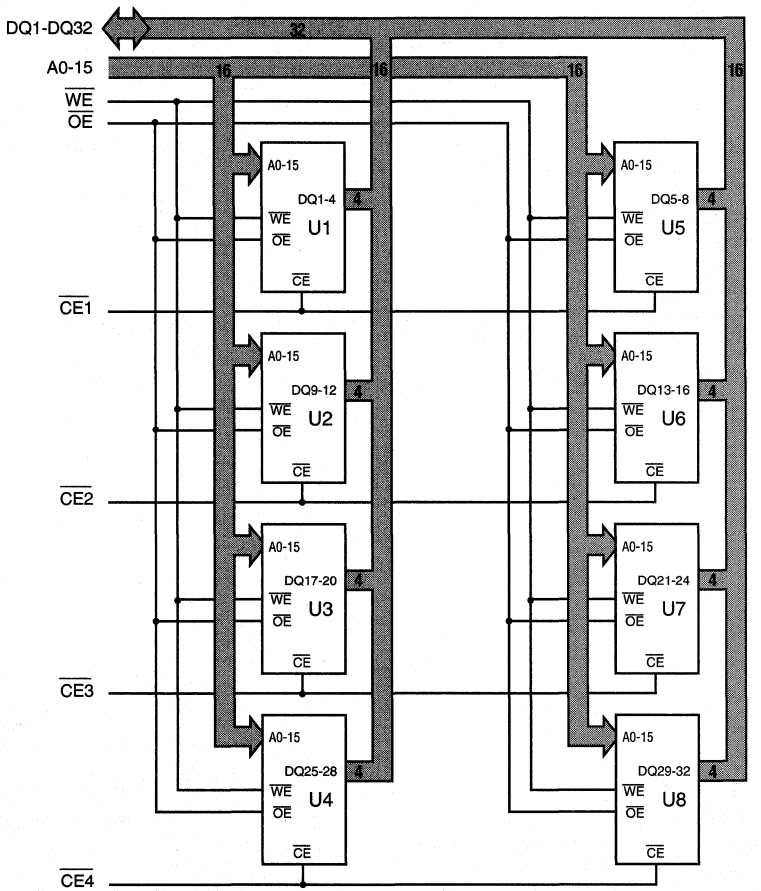
PD0 and PD1 identify the module's density, allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology.

All module components may be powered from a single +5V DC supply and all inputs and outputs are fully TTL-compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE-DETECT
PD0 = No Connect
PD1 = Vss

U1-U8 = MT5C2565DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage			V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	A0-A15, $\overline{WE}$, $\overline{OE}$	I_{LI1}	-40	40	µA	
		$\overline{CE1}$-$\overline{CE4}$	I_{LI2}	-10	10	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	DQ1-DQ32	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			V_{CC}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX -12†	MAX -15†	MAX -20	MAX -25	UNITS	NOTES
Operating Current TTL Input Levels	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	824	1,520	1,360	1,200	1,040	mA	3, 13
	P Version	I_{CC}	768	-	-	1,080	1,000	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	192	440	400	360	320	mA	13
	P Version	I_{SB1}	11.2	-	-	32	32	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	4.8	40	40	40	40	mA	13
	P Version	I_{SB2}	3.2	-	-	3	3	mA	13

† P version not available with this speed.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A15, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz V_{CC} = 5V	C_I	60	pF	4
Input Capacitance: $\overline{CE1}$- $\overline{CE4}$		C12	15	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-12		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	12		15		20		25		ns	
Address access time	^tAA		12		15		20		25	ns	
Chip Enable access time	^tACE		12		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable LOW to output in Low-Z	^tLZCE	3		3		3		3		ns	7
Chip Enable to output in High-Z	^tHZCE		6		8		9		9	ns	6, 7
Chip Enable LOW to power-up time	^tPU	0		0		0		0		ns	
Chip Enable HIGH to power-down time	^tPD		12		15		20		25	ns	
Output Enable access time	^tAOE		6		8		8		8	ns	
Output Enable LOW to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output Enable HIGH to output in High-Z	^tHZOE		6		6		7		7	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	12		15		20		25		ns	
Chip Enable to end of write	^tCW	8		10		12		15		ns	
Chip Enable to end of write (P-version)	^tCW	-		-		12		15		ns	
Address valid to end of write	^tAW	8		10		12		15		ns	
Address valid to end of write (P-version)	^tAW	-		-		12		15		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		ns	
WRITE pulse width	$^tWP1$	8		10		12		15		ns	
WRITE pulse width	$^tWP2$	12		12		15		15		ns	
Data setup time	^tDS	7		7		10		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write Enable LOW to output in Low-Z	^tLZWE	2		2		2		2		ns	7
Write Enable HIGH to output in High-Z	^tHZWE		6	0	7	0	8	0	10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

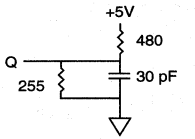


Fig. 1 OUTPUT LOAD EQUIVALENT

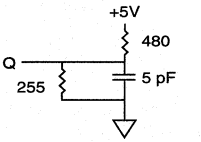


Fig. 2 OUTPUT LOAD EQUIVALENT

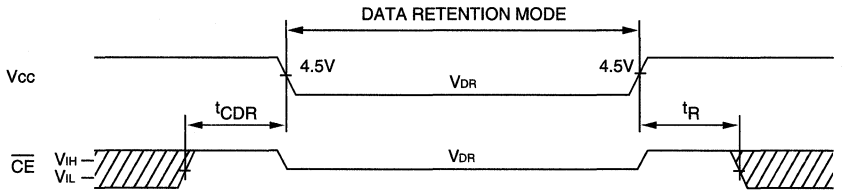
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 20ns cycle time.
14. Typical values are measured at 25°C.

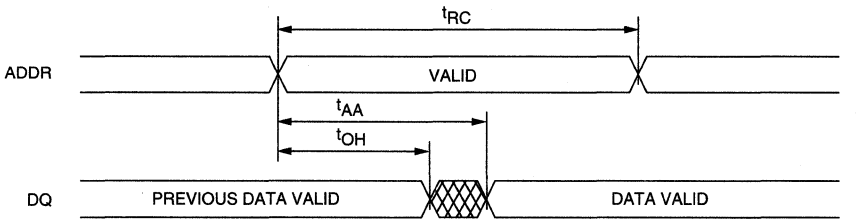
DATA RETENTION ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L Version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		1.0	2.4	mA	14
		Vcc = 3V	ICCDR		1.4	4	mA	14
Data Retention Current LP Version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		1.0	2.4	mA	14
		Vcc = 3V	ICCDR		1.4	4	mA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

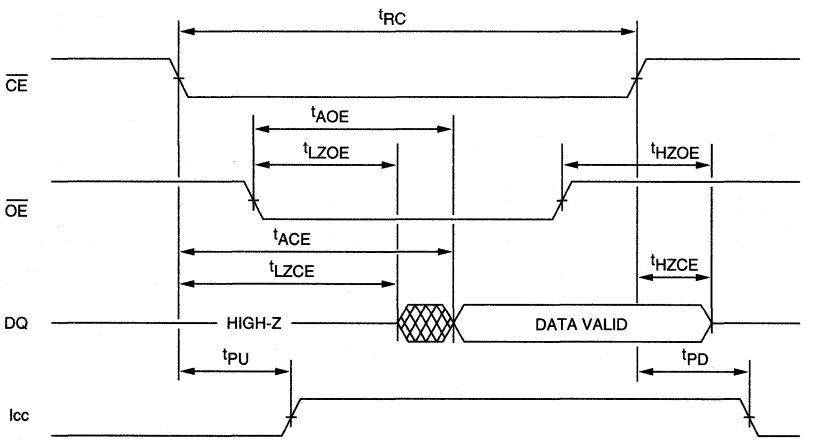
LOW Vcc DATA-RETENTION WAVEFORM



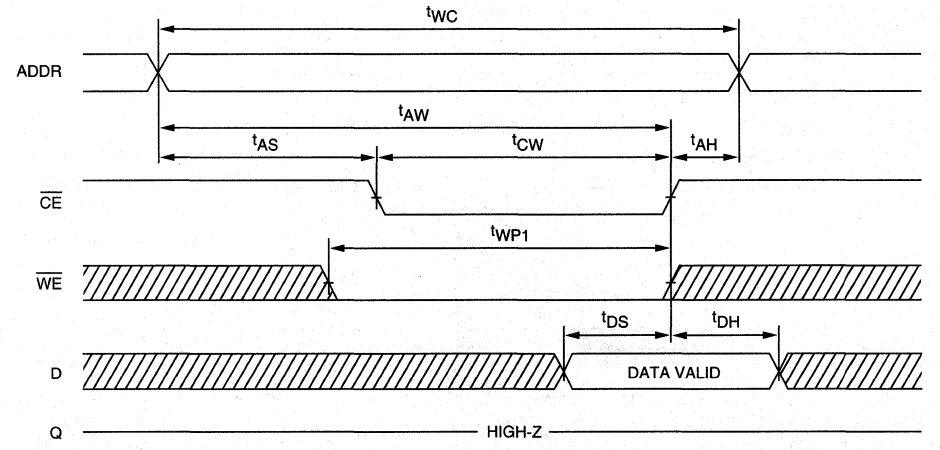
READ CYCLE NO. 1 [8, 9]



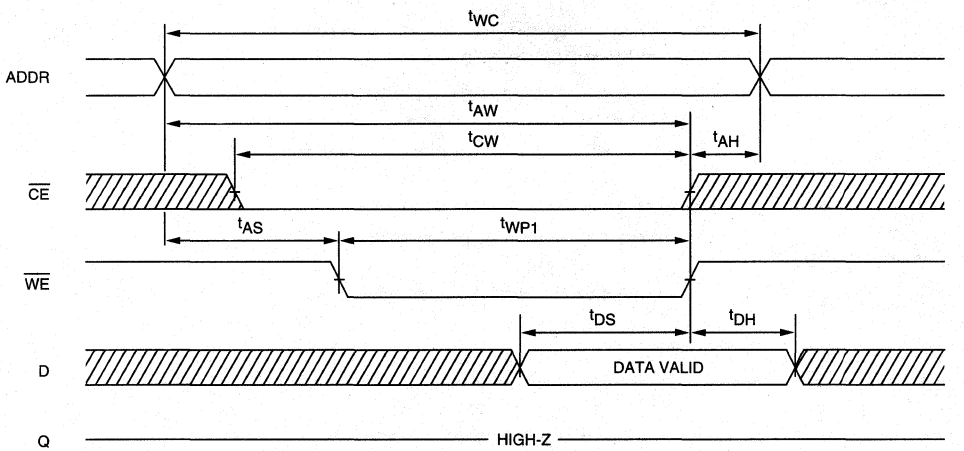
READ CYCLE NO. 2 [7, 8, 10]

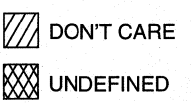


WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



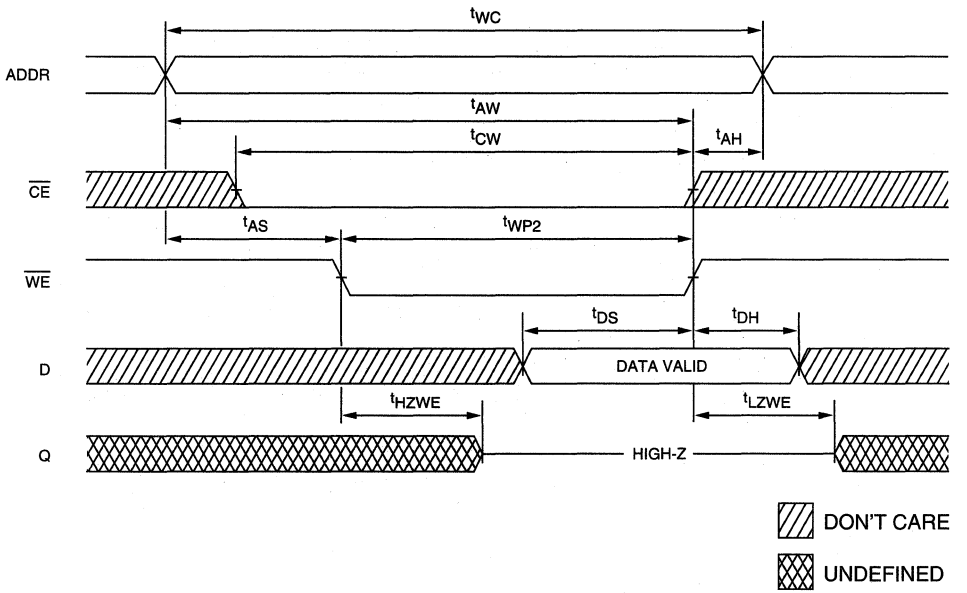
WRITE CYCLE NO. 2 [7, 12, 15]
(Write Enable Controlled)





NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12, 16]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

64K x 32 SRAM

LOW VOLTAGE

FEATURES

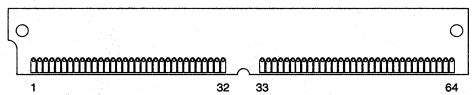
- High speed: 15, 20 and 25ns
- High-performance, low-power CMOS process
- Single +3.3V ± 0.3V power supply
- 5V-tolerant I/O
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Low profile
- Industry-standard pinout
- All inputs and outputs are TTL-compatible
- Upgradable with 128K x 32 and 256K x 32 modules

OPTIONS MARKING

- Timing
  - 15ns access -15
  - 20ns access -20
  - 25ns access -25
- Packages
  - 64-pin SIMM M
  - 64-pin ZIP Z
- 2V data retention (optional) L
- Part Number Example: MT8LS6432Z-20 L

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SE-1)



64-Pin ZIP
(SG-2)

PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

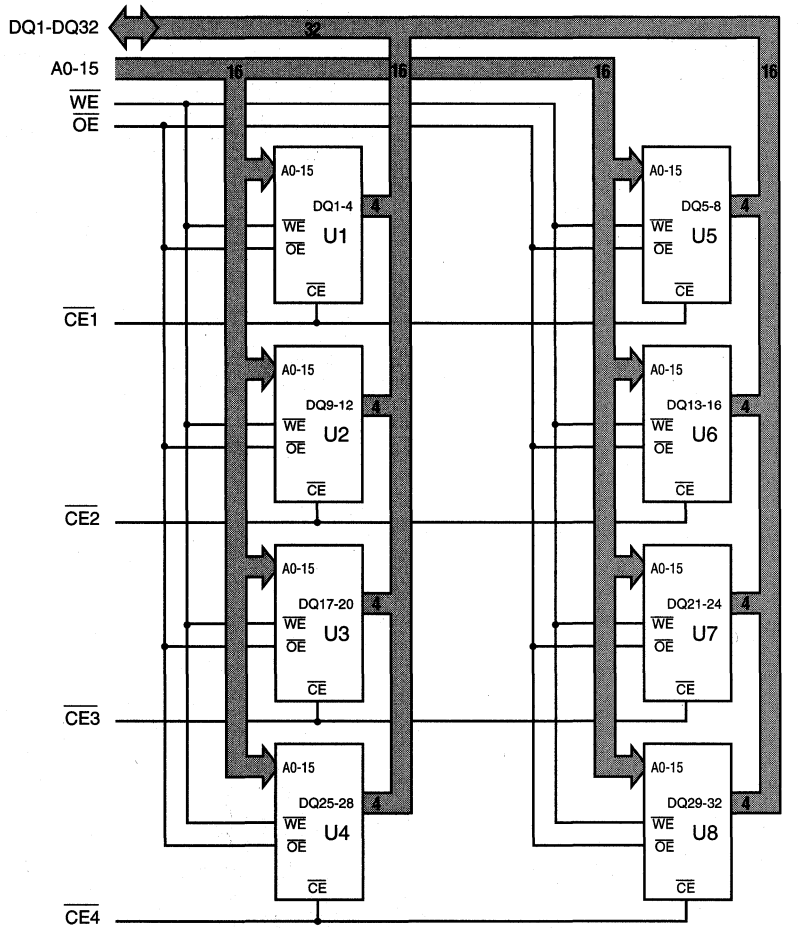
The MT8LS6432 is a high-speed SRAM memory module containing 65,536 words organized in a x32-bit configuration. The module consists of eight low voltage 64K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4 printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density, allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +3.3V DC supply and all inputs and outputs are fully TTL-compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE-DETECT
PD0 = No Connect
PD1 = Vss

U1-U8 = MT5LC2565DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage temperature ..... -55°C to +125°C
Power dissipation 8W
Short circuit output current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5V	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	A0-A15, $\overline{WE}$, $\overline{OE}$	I_{LI1}	-8	8	µA	
		$\overline{CE1}$-$\overline{CE4}$	I_{L2}	-2	2	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	DQ1-DQ32	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			V_{CC}	3.0	3.6	V	1

					MAX				
DESCRIPTION	CONDITIONS	SYMBOL	VER	TYP	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{CC}	STD, L	584	1,000	880	760	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{SB1}	STD, L	136	280	240	200	mA	13
	$\overline{CE} \ge V_{CC}$ - 0.2V; V_{CC} = MAX $V_{IN} \ge V_{CC}$ - 0.2V or $V_{IN} \le V_{SS}$ + 0.2V	I_{SB2}	STD, L	8	24	24	24	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A15, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz V_{CC} = 3.3V	C_{I1}	56	pF	4
Input Capacitance: $\overline{CE1}$-$\overline{CE4}$		C_{I2}	15	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	15		20		25		ns	
Address access time	^tAA		15		20		25	ns	
Chip Enable access time	^tACE		15		20		25	ns	
Output hold from address change	^tOH	3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		ns	
Chip disable to output in High-Z	^tHZCE		8		9		9	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	4
Chip disable to power-down time	^tPD		15		20		25	ns	4
Output Enable access time	^tAOE		7		8		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		7		7	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		15		ns	
Address valid to end of write	^tAW	10		12		15		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		ns	
WRITE pulse width	$^tWP1$	10		12		15		ns	
WRITE pulse width	$^tWP2$	12		15		15		ns	
Data setup time	^tDS	8		10		10		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		7		8		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

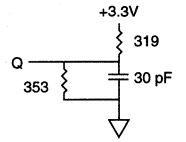


Fig. 1 OUTPUT LOAD EQUIVALENT

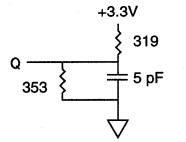


Fig. 2 OUTPUT LOAD EQUIVALENT

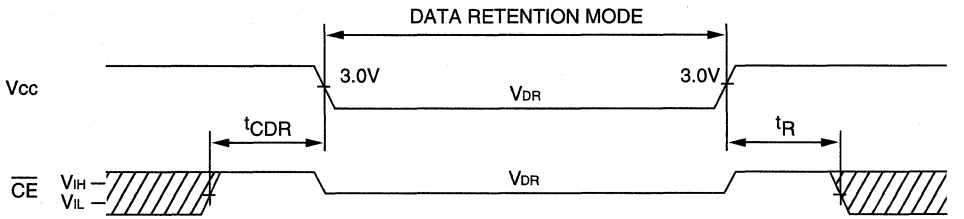
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0$ for $t \leq {}^tKC/2$
   Undershoot: $V_{IL} \geq -2.0$ for $t \leq {}^tKC/2$
   Power-up: $V_{IH} \leq +6.0$ for and $V_{CC} \leq 3.1V$ for $t \leq 200$msec.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = READ cycle time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
14. Typical currents are measured at 25°C. MAX is over operating temperature range.

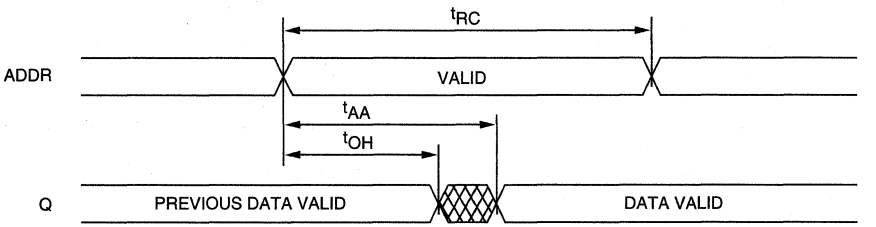
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq V_{CC}$ -0.2V Other inputs: $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq V_{SS}$+0.2V V_{CC} = 2V	I_{CCDR}		2.48	4	mA	14
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

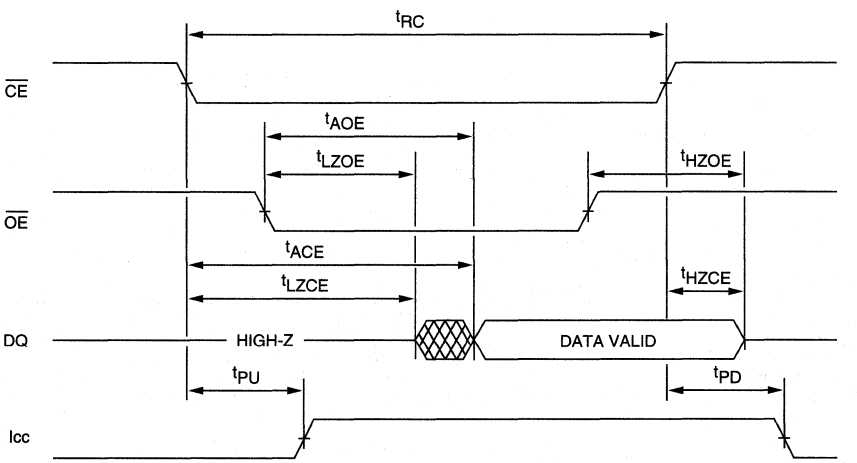
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



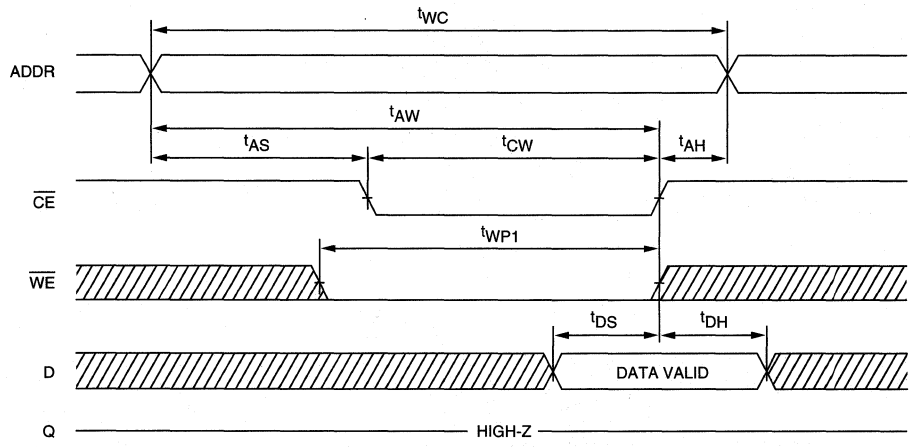
READ CYCLE NO. 2 [7, 8, 10]



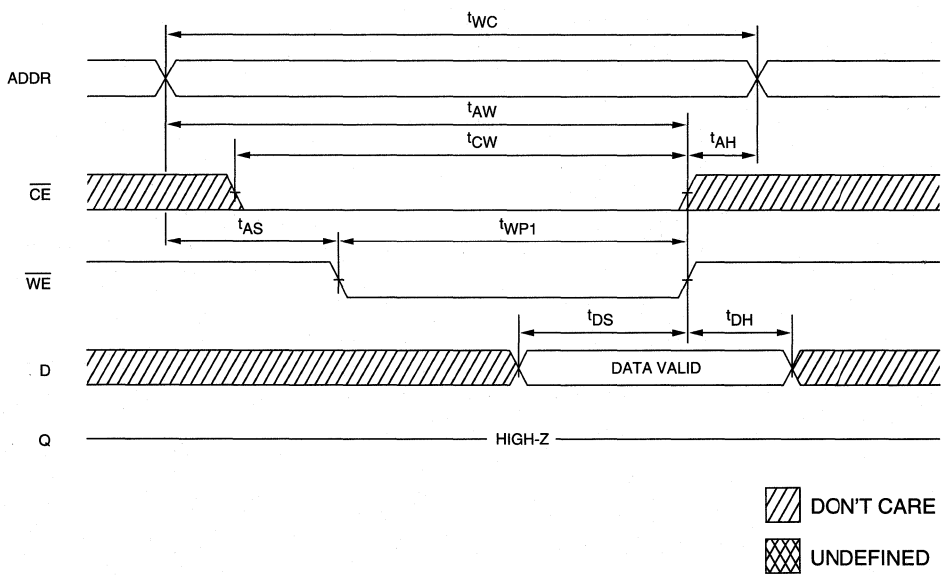
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

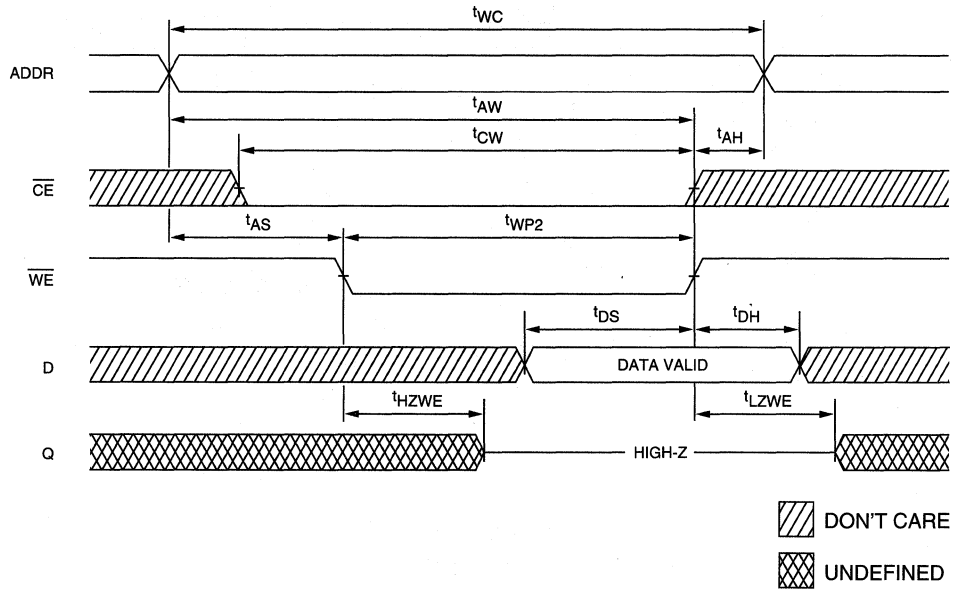


WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

128K x 32 SRAM

FEATURES

- High speed: 15, 20 and 25ns
- High-density 512KB design
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- All inputs and outputs are TTL-compatible
- Industry standard pinout
- Low profile
- Upgradable to a 256K x 32 module

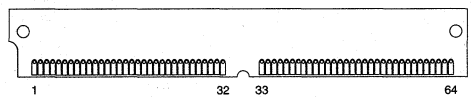
OPTIONS — MARKING

- Timing
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 64-pin SIMM — M
  - 64-pin ZIP — Z
- 2V data retention (optional) — L
- 2V data retention, low power (optional) — LP
- Part Number Example: MT4S12832M-15 LP

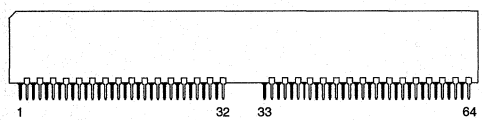
NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SE-2)



64-Pin ZIP
(SG-3)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT4S12832 is a high-speed SRAM memory module containing 131,072 words organized in a x32-bit configuration. The module consists of four 128K x 8 fast SRAMs mounted on a 64-pin, single-sided, FR4-printed circuit board.

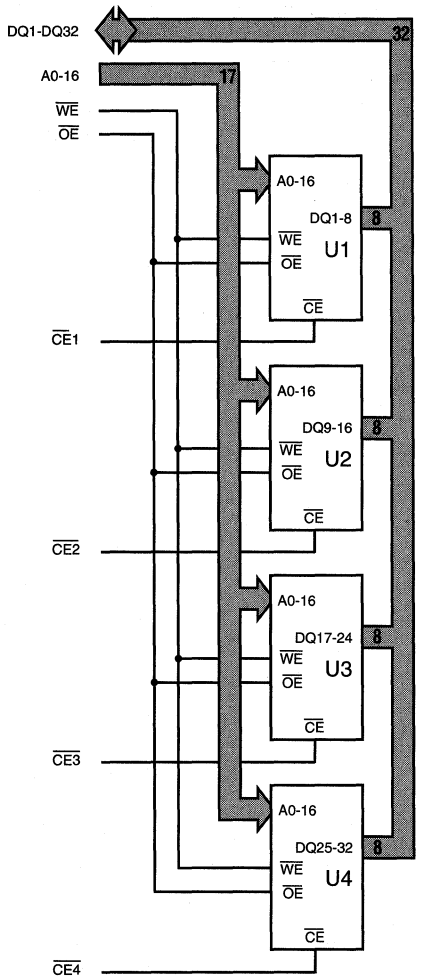
Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL-compatible.

The "L" and "LP" versions each provide a 70 percent reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90 percent reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5C1008DJ

PRESENCE-DETECT
PD0 = No Connect
PD1 = No Connect

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage			V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	A0-A16, $\overline{WE}$, $\overline{OE}$	I_{LI1}	-20	20	µA	
		$\overline{CE1}$-$\overline{CE4}$	I_{LI2}	-5	5	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	DQ1-DQ32	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			V_{CC}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX -15	MAX -20	MAX -25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	428	780	640	580	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	148	300	260	220	mA	13
	LP version only	I_{SB1}	5.2	12	12	12	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IL} ≤ V_{SS} +0.2V V_{IH} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	1.6	20	20	20	mA	13
	L and LP versions only	I_{SB2}	1.2	6	6	6	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A16, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz V_{CC} = 5V	C_I	35	pF	4
Input Capacitance: $\overline{CE1}$- $\overline{CE4}$		C_{I2}	10	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	15		20		25		ns	
Address access time	^tAA		15		20		25	ns	
Chip Enable access time	^tACE		15		20		25	ns	
Output hold from address change	^tOH	3		3		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		8		10	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip disable to power-down time	^tPD		15		20		25	ns	
Output Enable access time	^tAOE		6		6		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		10	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		15		ns	
Address valid to end of write	^tAW	10		12		15		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	9		12		15		ns	
WRITE pulse width	$^tWP2$	12		15		15		ns	
Data setup time	^tDS	7		8		10		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		8		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

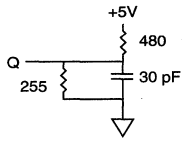


Fig. 1 OUTPUT LOAD EQUIVALENT

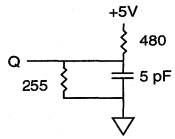


Fig. 2 OUTPUT LOAD EQUIVALENT

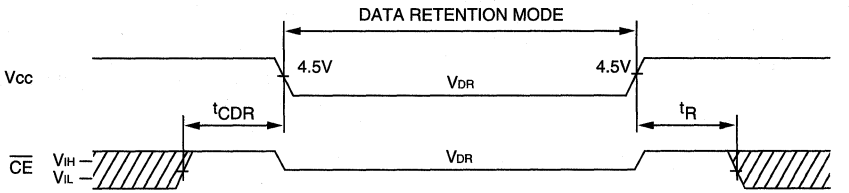
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1, unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 25ns cycle time.
14. Typical currents are measured at 25°C.

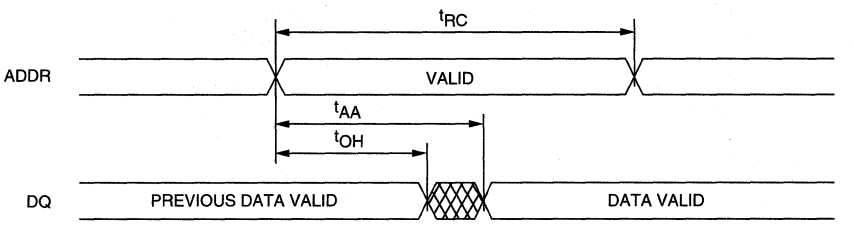
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L Version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		140	600	µA	14
	VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 3V	ICCDR		240	1,000	µA	14
Data Retention Current LP Version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		140	600	µA	14
		Vcc = 3V	ICCDR		240	1,000	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

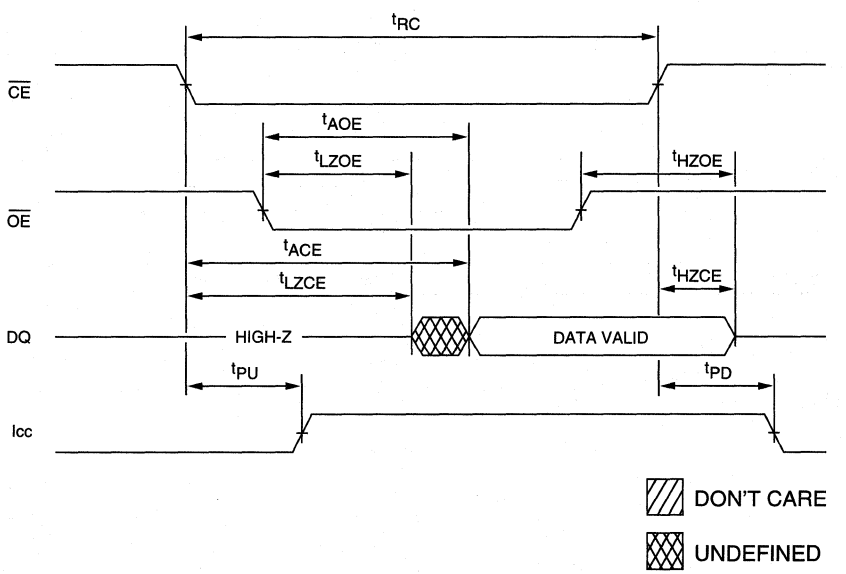
LOW Vcc DATA-RETENTION WAVEFORM



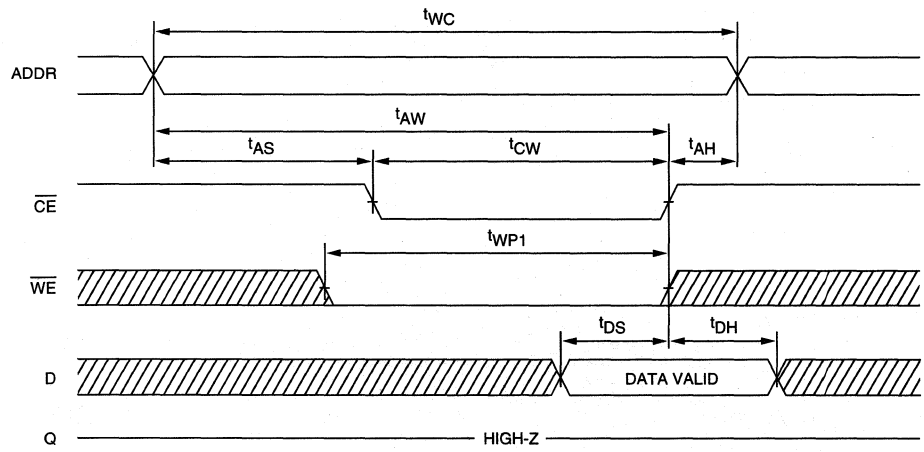
READ CYCLE NO. 1 [8, 9]



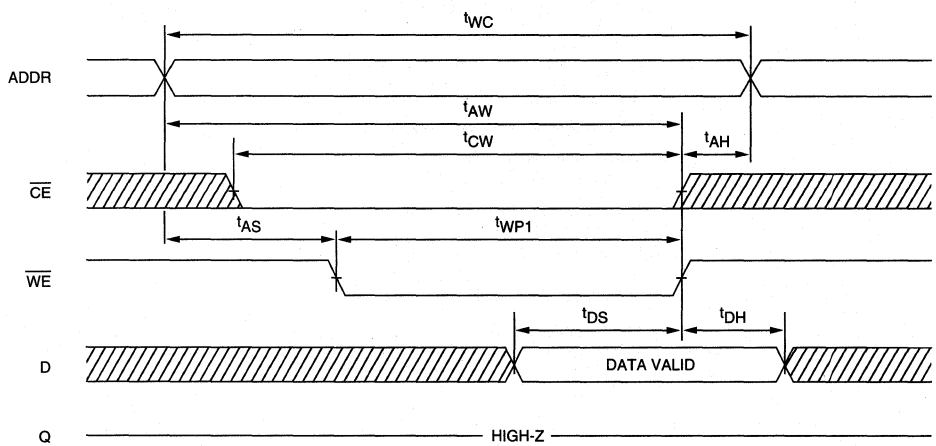
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)

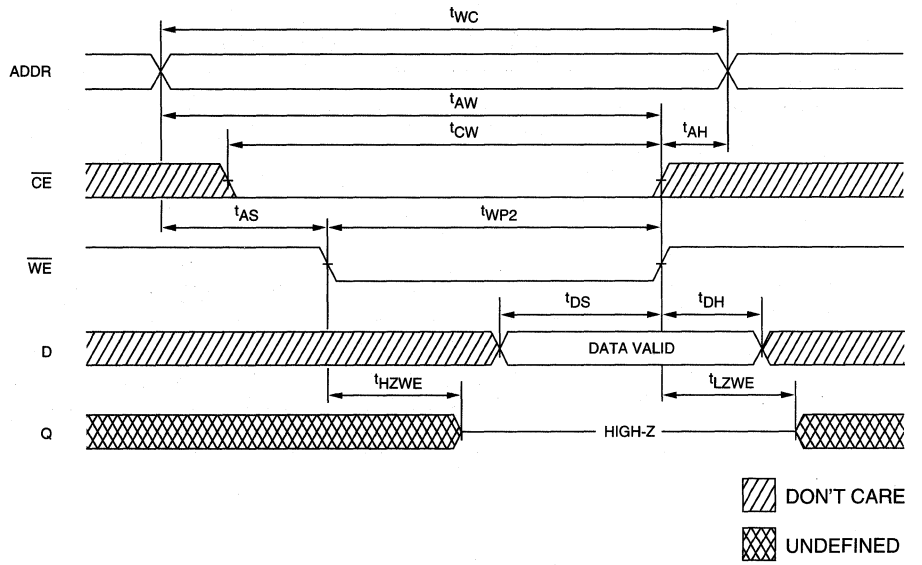


DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

128K x 32 SRAM
LOW VOLTAGE

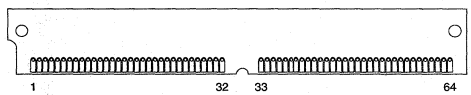
FEATURES
- High speed: 17, 20 and 25ns
- High-density 512KB design
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- 5V-tolerant I/O
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- All inputs and outputs are TTL-compatible
- Industry-standard pinout
- Low profile
- Upgradable to a 256K x 32 module

OPTIONS — MARKING
- Timing
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - 64-pin SIMM — M
  - 64-pin ZIP — Z
- 2V data retention (optional) — L
- 2V data retention, low power (optional) — LP
- Part Number Example: MT4LS12832M-20 LP

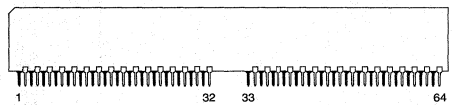
NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SE-2)



64-Pin ZIP
(SG-3)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT4LS12832 is a high-speed SRAM memory module containing 131,072 words organized in a x32-bit configuration. The module consists of four low voltage128K x 8 fast SRAMs mounted on a 64-pin, single-sided, FR4-printed circuit board.

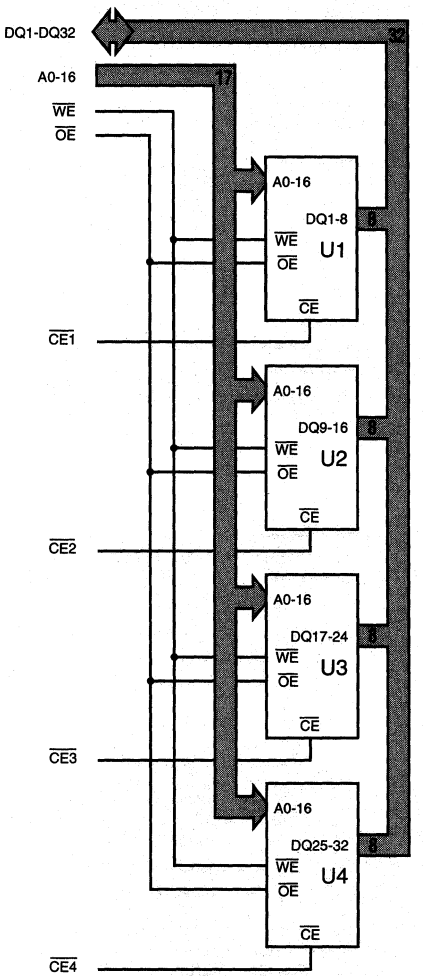
Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry-standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +3.3V DC supply and all inputs and outputs are fully TTL-compatible.

The "L" and "LP" versions each provide a significant reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a significant reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

FUNCTIONAL BLOCK DIAGRAM



U1-U4 = MT5LC1008DJ

PRESENCE-DETECT
PD0 = No Connect
PD1 = No Connect

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage temperature ..... -55°C to +125°C
Power dissipation 4W
Short circuit output current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5V	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	A0-A16, $\overline{WE}$, $\overline{OE}$	I_{LI1}	-4	4	µA	
		$\overline{CE1}$-$\overline{CE4}$	I_{LI2}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	DQ1-DQ32	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			V_{CC}	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYMBOL	VER	TYP	MAX -17	MAX -20	MAX -25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	ALL	280	620	580	540	mA	3, 13
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	STD,L	80	180	160	140	mA	13
			LP	6	12	12	12	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	STD,L	4	12	12	12	mA	13
			LP	2.8	6	6	6	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A16, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz V_{CC} = 3.3V	C_{I1}	30	pF	4
Input Capacitance: $\overline{CE1}$-$\overline{CE4}$		C_{I2}	8	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-17		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	17		20		25		ns	
Address access time	^tAA		17		20		25	ns	
Chip Enable access time	^tACE		17		20		25	ns	
Output hold from address change	^tOH	3		3		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		7		8		10	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip disable to power-down time	^tPD		17		20		25	ns	
Output Enable access time	^tAOE		6		7		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		7		8	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	17		20		25		ns	
Chip Enable to end of write	^tCW	12		12		15		ns	
Address valid to end of write	^tAW	12		12		15		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	12		12		15		ns	
WRITE pulse width	$^tWP2$	13		15		15		ns	
Data setup time	^tDS	8		8		10		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		5		ns	7
Write Enable to output in High-Z	^tHZWE		7		8		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

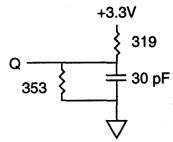


Fig. 1 OUTPUT LOAD EQUIVALENT

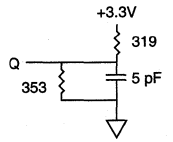


Fig. 2 OUTPUT LOAD EQUIVALENT

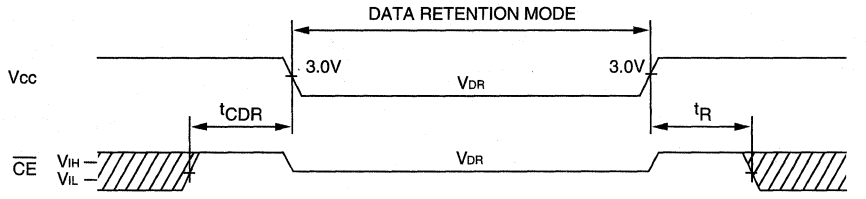
NOTES

1. All voltages referenced to V_{SS} (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$
   Power-up: $V_{IH} \geq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200$ msec.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1, unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$=READ cycle time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Typical currents are measured at 25°C.

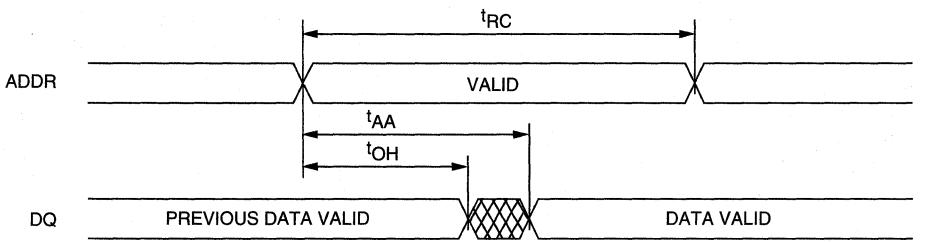
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V	
Data Retention Current L version	$\overline{CE} \geq V_{CC}$ -0.2V Other inputs: $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq V_{SS}$+0.2V V_{CC} = 2V	I_{CCDR}		580	1,040	µA	14
Data Retention Current LP version	$\overline{CE} \geq V_{CC}$ -0.2V V_{CC} = 2V	I_{CCDR}		580	1,040	µA	14
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

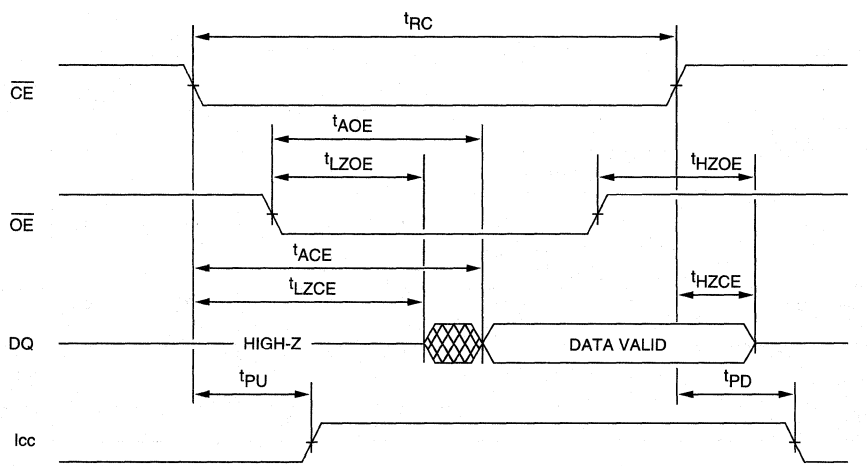
LOW Vcc DATA RETENTION WAVEFORM

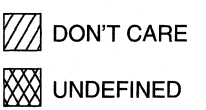


READ CYCLE NO. 1 [8, 9]

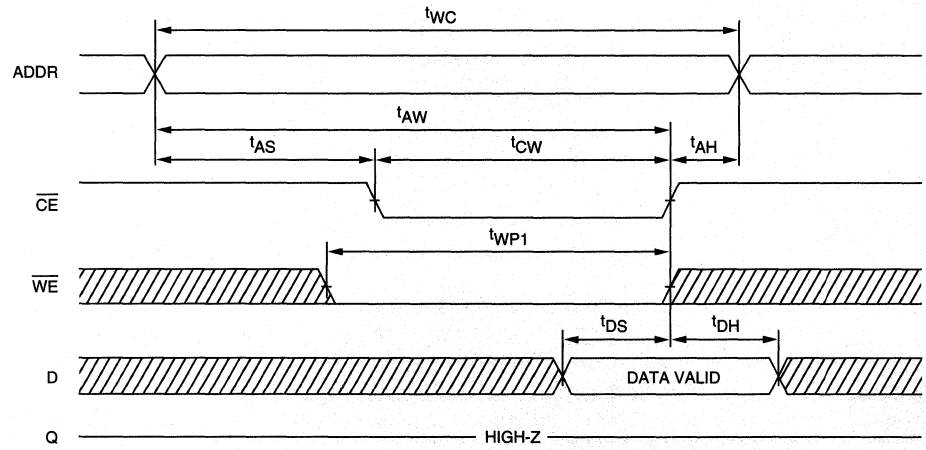


READ CYCLE NO. 2 [7, 8, 10]

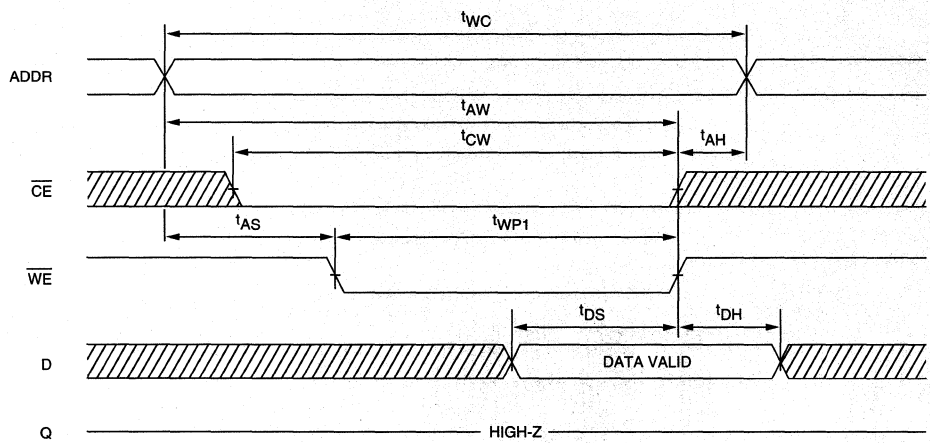


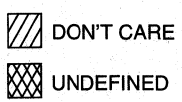


WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



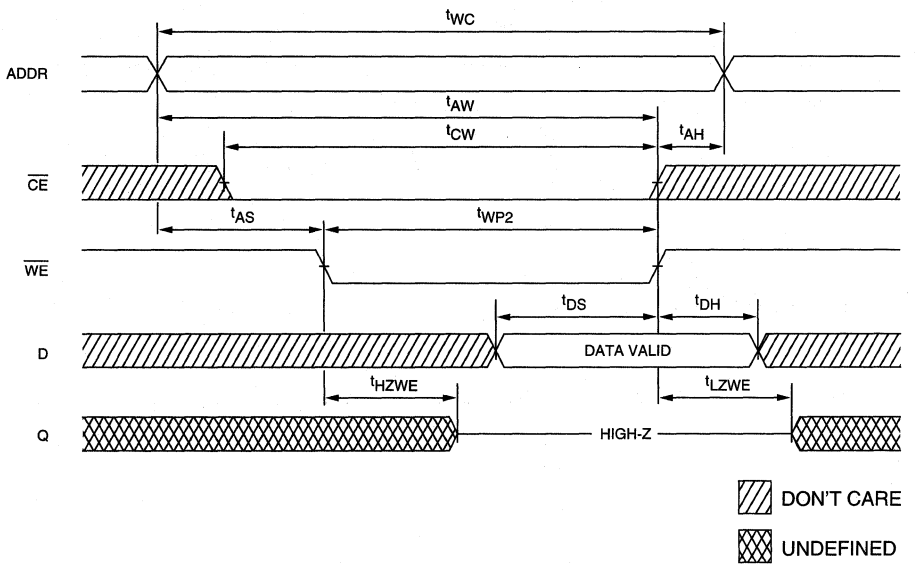
WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)





NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

256K x 32 SRAM

FEATURES

- High speed: 15, 20 and 25ns
- High-density 1MB design
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Industry-standard pinout
- All inputs and outputs are TTL-compatible
- Low profile

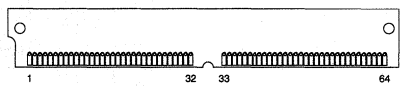
OPTIONS MARKING

- Timing
  - 15ns access -15
  - 20ns access -20
  - 25ns access -25
- Packages
  - 64-pin SIMM M
  - 64-pin ZIP Z
- 2V data retention (optional) L
- 2V data retention, low power (optional) LP
- Part Number Example: MT8S25632Z-15 L

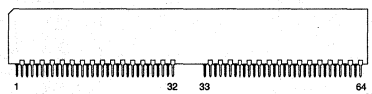
NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM (SE3)



64-Pin ZIP (SG-1)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	A17	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT8S25632 is a high-speed SRAM memory module containing 262,144 words organized in a x32-bit configuration. The module consists of eight 256K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in High-Z for additional flexibility in system design and memory expansion.

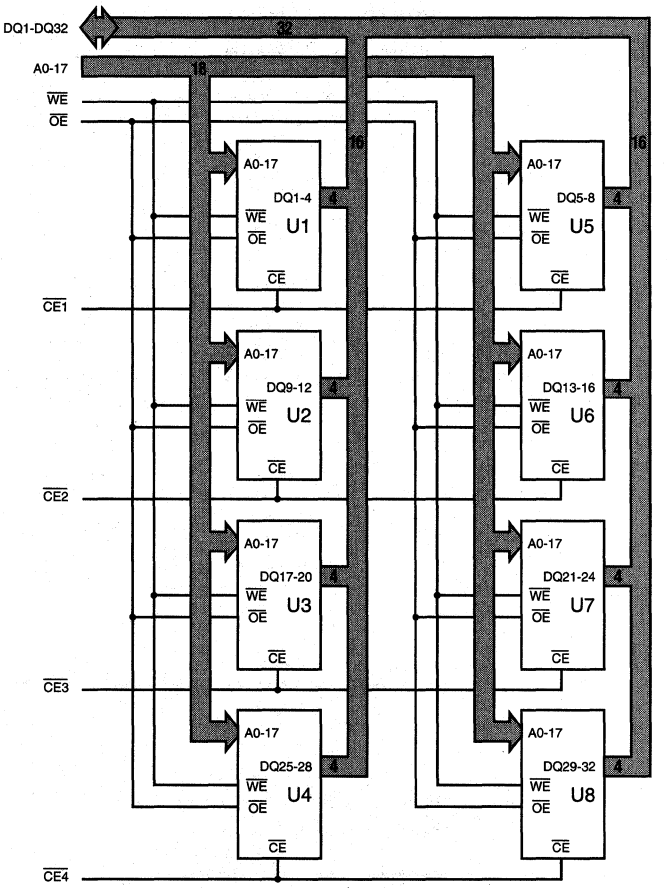
PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology.

All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL-compatible.

The "L" and "LP" versions each provide a 70 percent reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE-DETECT U1-U8 = MT5C1005DJ
PD0 = Vss
PD1 = Vss

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage			V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	A0-A17, $\overline{WE}$, $\overline{OE}$	I_{LI1}	-40	40	µA	
		$\overline{CE1}$-$\overline{CE4}$	I_{LI2}	-10	10	µA	
Input/Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	DQ1-DQ32	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			Vcc	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX -15	MAX -20	MAX -25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	856	1,560	1,280	1,160	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	296	600	440	400	mA	13
	LP version only	I_{SB1}	10.4	24	24	24	mA	13
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	3.2	40	40	40	mA	13
	L and LP versions only	I_{SB2}	2.4	12	12	12	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance; A0-A17, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 5V	C_{I1}	60	pF	4
Input Capacitance; $\overline{CE1}$-$\overline{CE4}$		C_{I2}	15	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	15		20		25		ns	
Address access time	^tAA		15		20		25	ns	
Chip Enable access time	^tACE		15		20		25	ns	
Output hold from address change	^tOH	3		3		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		6		8		10	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip disable to power-down time	^tPD		15		20		25	ns	
Output Enable access time	^tAOE		6		6		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output disable to output in High-Z	^tHZOE		5		6		10	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	15		20		25		ns	
Chip Enable to end of write	^tCW	10		12		15		ns	
Address valid to end of write	^tAW	10		12		15		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	9		12		15		ns	
WRITE pulse width	$^tWP2$	12		15		15		ns	
Data setup time	^tDS	7		8		10		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		ns	7
Write Enable to output in High-Z	^tHZWE		6		8		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

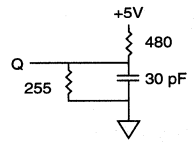


Fig. 1 OUTPUT LOAD EQUIVALENT

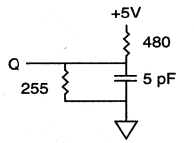


Fig. 2 OUTPUT LOAD EQUIVALENT

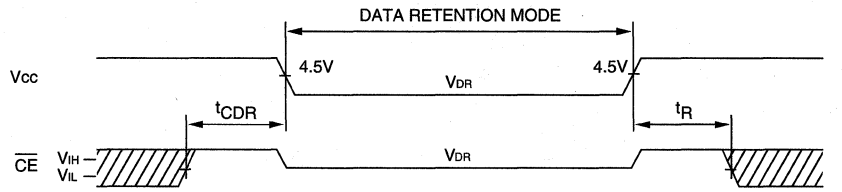
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC=Read Cycle Time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 25ns cycle time.
14. Typical values are measured at 25°C.

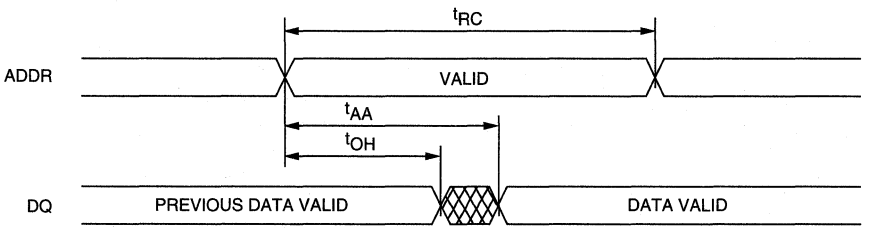
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L Version	$\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V	Vcc = 2V	ICCDR		280	1,200	µA	14
		Vcc = 3V			480	2,000	µA	14
Data Retention Current LP Version	$\overline{CE}$ ≥ (Vcc -0.2V)	Vcc = 2V	ICCDR		280	1,200	µA	14
		Vcc = 3V	ICCDR		240	2,000	µA	14
Chip Deselect to Data Retention Time			^{t}CDR	0			ns	4
Operation Recovery Time			^{t}R	^{t}RC			ns	4,11

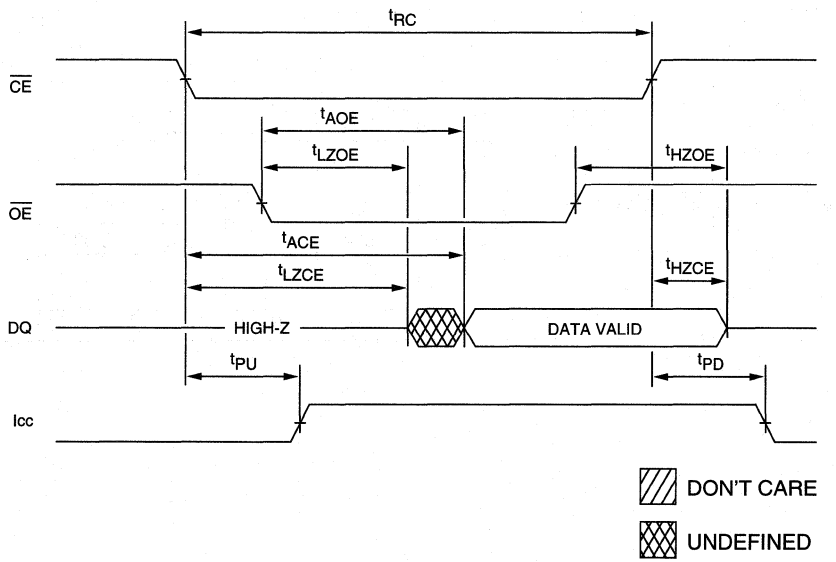
LOW Vcc DATA-RETENTION WAVEFORM



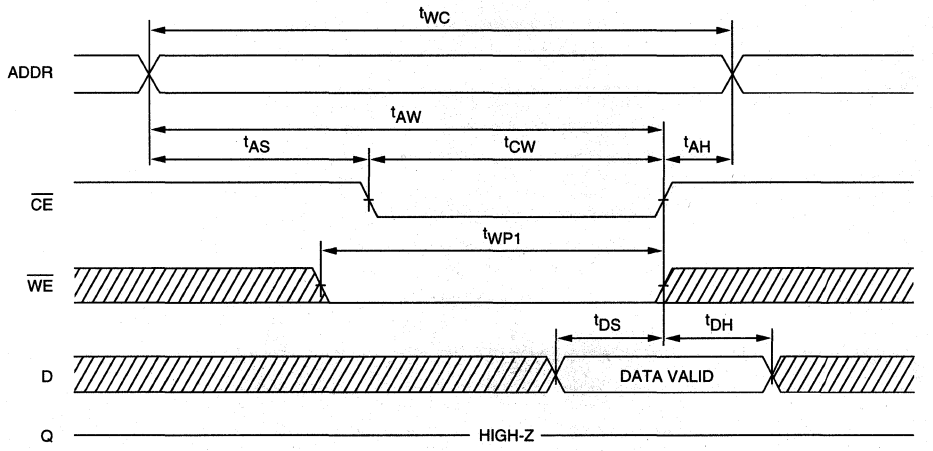
READ CYCLE NO. 1 [8, 9]



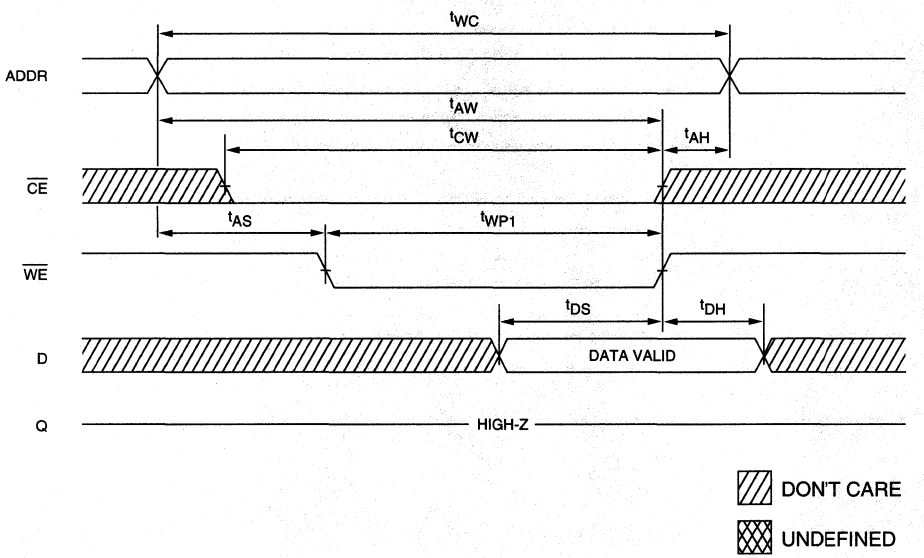
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

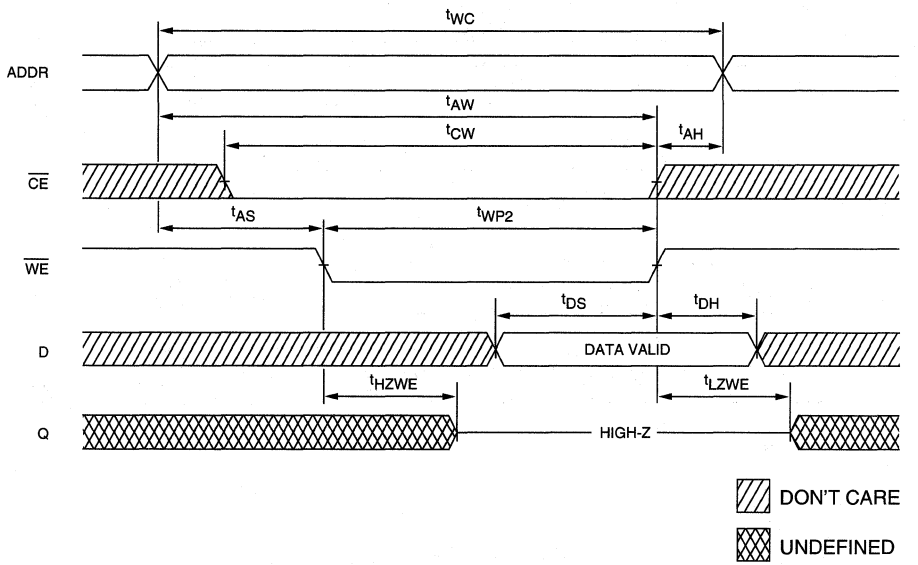


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

256K x 32 SRAM
LOW VOLTAGE

FEATURES
- High speed: 17, 20 and 25ns
- High-density 1MB design
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ± 0.3V power supply
- 5V-tolerant I/O
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ functions
- Industry-standard pinout
- All inputs and outputs are TTL-compatible
- Low profile

OPTIONS / MARKING

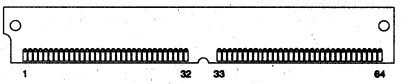
• Timing	
17ns access	-17
20ns access	-20
25ns access	-25
• Packages	
64-pin SIMM	M
64-pin ZIP	Z
• 2V data retention (optional)	L
• 2V data retention, low power (optional)	LP

- Part Number Example: MT8LS25632Z-20 LP

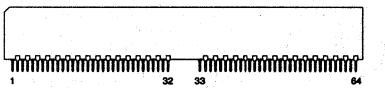
NOTE: Not all combinations of speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SE-3)



64-Pin ZIP
(SG-1)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	A17	51	A5
4	DQ1	20	DQ5	36	A16	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT8LS25632 is a high-speed SRAM memory module containing 262,144 words organized in a x32-bit configuration. The module consists of eight low voltage 256K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in High-Z for additional flexibility in system design and memory expansion.

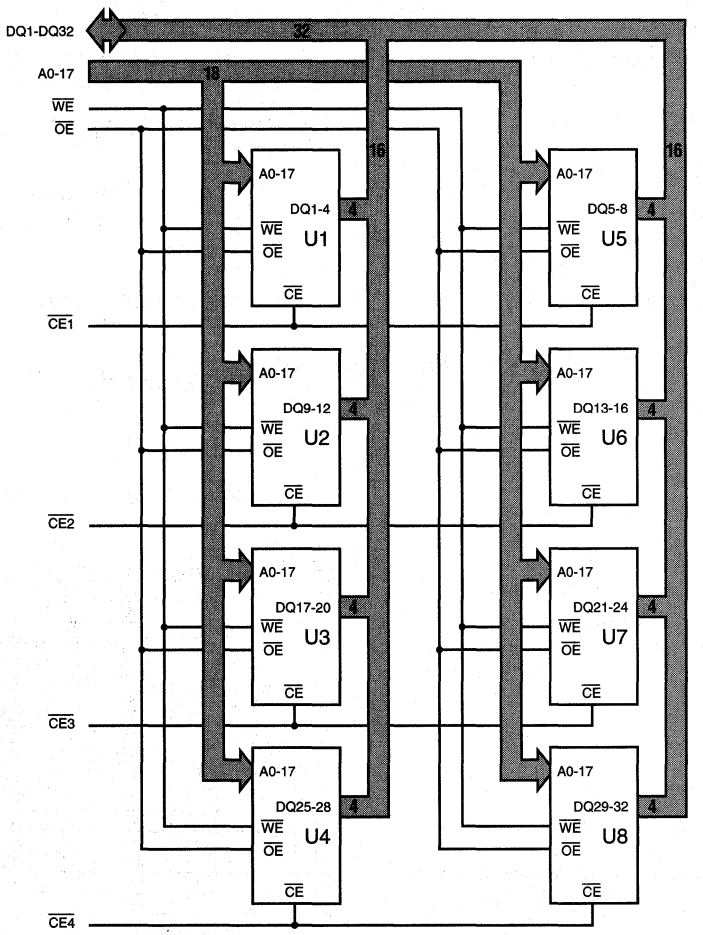
PD0 and PD1 identify the module's density allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology.

All module components may be powered from a single +3.3V DC supply and all inputs and outputs are fully TTL-compatible.

The "L" and "LP" versions each provide a significant reduction in CMOS standby current (I_{SB2}) over the standard version. The "LP" version also provides a significant reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

FUNCTIONAL BLOCK DIAGRAM



PRESENCE-DETECT U1-U8 = MT5LC1005DJ
PD0 = Vss
PD1 = Vss

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage temperature ..... -55°C to +125°C
Power dissipation 8W
Short circuit output current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5V	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	A0-A17, $\overline{WE}$, $\overline{OE}$	I_{LI1}	-8	8	µA	
		$\overline{CE1}$-$\overline{CE4}$	I_{LI2}	-2	2	µA	
Input/Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	DQ1-DQ32	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			Vcc	3.0	3.6	V	1

					MAX				
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-17	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	Icc	ALL	560	1,240	1,160	1,080	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	STD,L	160	360	320	280	mA	13
			LP	12	24	24	24	mA	
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	STD,L	8	24	24	24	mA	13
			LP	5.6	12	12	12	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A17, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz Vcc = 3.3V	C_{I1}	50	pF	4
Input Capacitance: $\overline{CE1}$-$\overline{CE4}$		C_{I2}	15	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-17		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	17		20		25		ns	
Address access time	^tAA		17		20		25	ns	
Chip Enable access time	^tACE		17		20		25	ns	
Output hold from address change	^tOH	3		3		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		7		8		10	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		ns	
Chip disable to power-down time	^tPD		17		20		25	ns	
Output Enable access time	^tAOE		6		7		8	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		7		8	ns	6
WRITE Cycle									
WRITE cycle time	^tWC	17		20		25		ns	
Chip Enable to end of write	^tCW	12		12		15		ns	
Address valid to end of write	^tAW	12		12		15		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP1$	12		12		15		ns	
WRITE pulse width	$^tWP2$	13		15		15		ns	
Data setup time	^tDS	8		8		10		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		5		ns	7
Write Enable to output in High-Z	^tHZWE		7		8		10	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

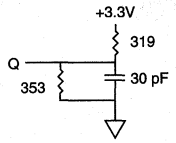


Fig. 1 OUTPUT LOAD EQUIVALENT

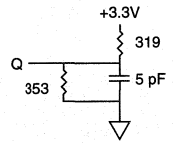


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

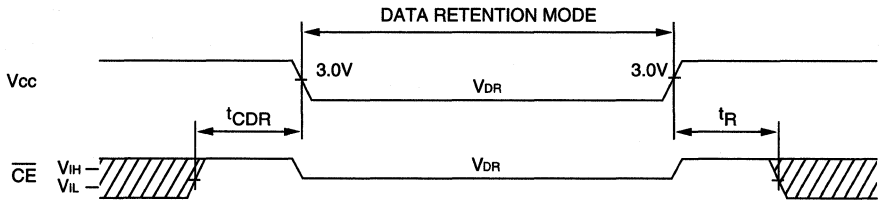
1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$
   Power-up: $V_{IH} \geq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200$ msec.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1, unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$=READ cycle time
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Typical currents are measured at 25°C. MAX is over operating temperature range.

SRAM MODULE

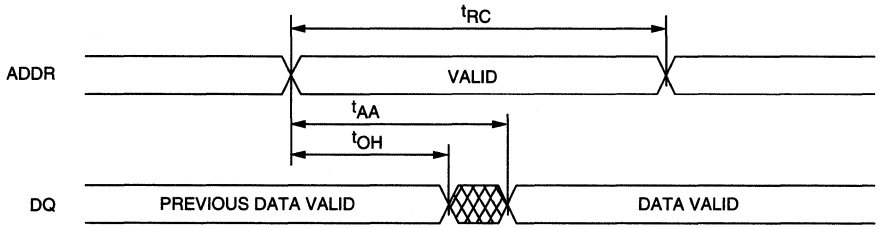
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current L Version	$\overline{CE} \geq$ Vcc -0.2V Other inputs: $V_{IN} \geq$ Vcc -0.2V or $V_{IN} \leq$ Vss+0.2V Vcc = 2V	I_{CCDR}		1.16	2.08	mA	14
Data Retention Current LP Version	$\overline{CE} \geq$ Vcc -0.2V Vcc = 2V	I_{CCDR}		1.16	2.08	mA	14
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

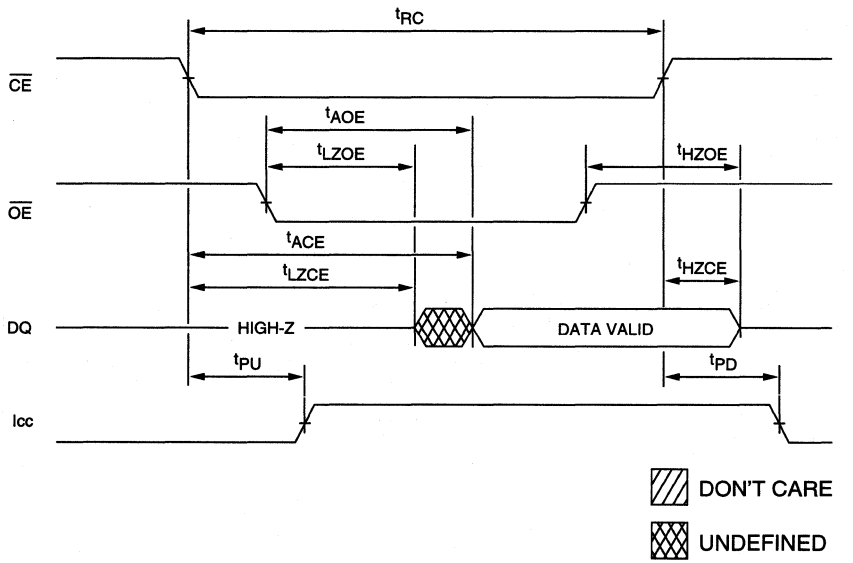
LOW Vcc DATA RETENTION WAVEFORM



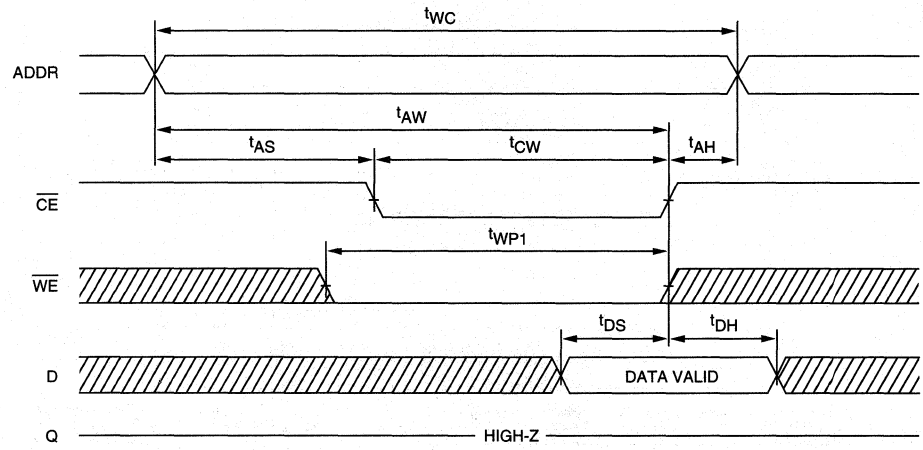
READ CYCLE NO. 1 [8, 9]



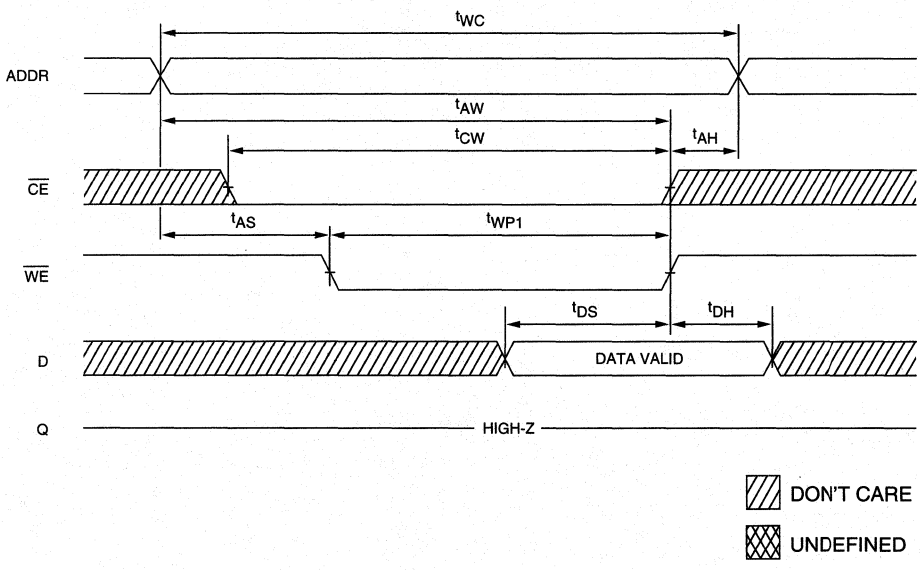
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

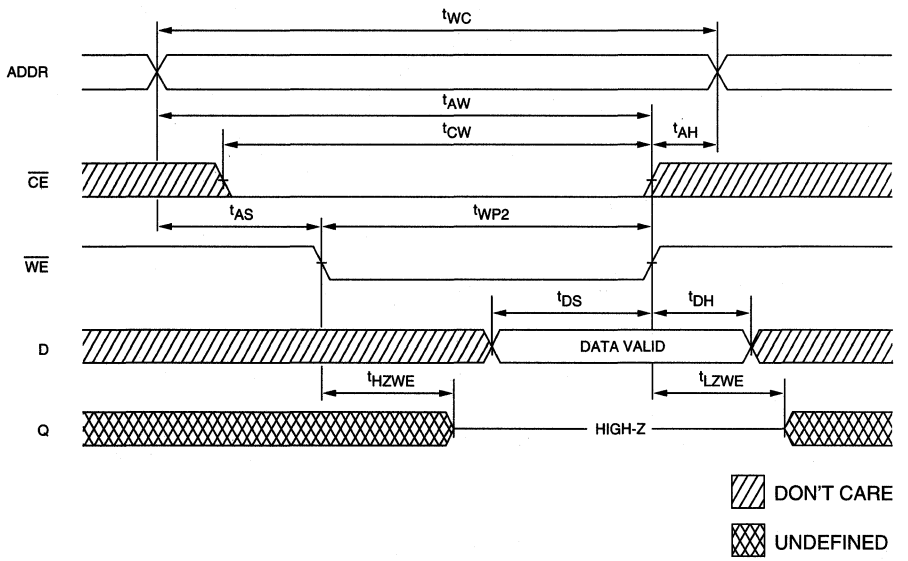


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SRAM MODULE

1 MEG x 32 SRAM

3.3V WITH OUTPUT ENABLE

NEW SRAM MODULE

FEATURES

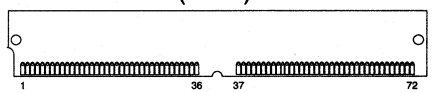
- All I/O pins are 5V tolerant
- Complies with JEDEC low-voltage TTL standards
- Industry-compatible pinout
- High speed: 15, 20, 25 and 35ns
- High-density 4MB design
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ function
- All inputs and outputs are TTL-compatible
- Low profile (.610 inches maximum height)

OPTIONS — MARKING

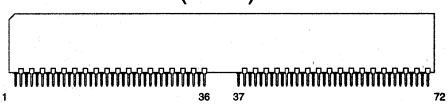
- Timing
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - 72-pin SIMM — M
  - 72-pin ZIP — Z
- 2V data retention (optional) — L
- Part Number Example: MT8LS132M-20 L

PIN ASSIGNMENT (Top View)

72-Pin SIMM
(SE-4)



72-Pin ZIP
(SG-4)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	NC	19	A1	37	$\overline{CE4}$	55	A5
2	NC	20	A8	38	$\overline{CE3}$	56	A12
3	PD2	21	A2	39	A17	57	Vcc
4	PD3	22	A9	40	A16	58	A13
5	Vss	23	DQ13	41	$\overline{OE}$	59	A6
6	PD0	24	DQ5	42	Vss	60	DQ21
7	PD1	25	DQ14	43	DQ25	61	DQ29
8	DQ1	26	DQ6	44	DQ17	62	DQ22
9	DQ9	27	DQ15	45	DQ26	63	DQ30
10	DQ2	28	DQ7	46	DQ18	64	DQ23
11	DQ10	29	DQ16	47	DQ27	65	DQ31
12	DQ3	30	DQ8	48	DQ19	66	DQ24
13	DQ11	31	Vss	49	DQ28	67	DQ32
14	DQ4	32	$\overline{WE}$	50	DQ20	68	Vss
15	DQ12	33	A15	51	A3	69	A18
16	Vcc	34	A14	52	A10	70	A19
17	A0	35	$\overline{CE2}$	53	A4	71	NC
18	A7	36	$\overline{CE1}$	54	A11	72	NC

GENERAL DESCRIPTION

The MT8L S132 is a high-speed SRAM memory module containing 1,048,576 words organized in a x32-bit configuration. The module consists of eight 3.3V 1Meg x 4 fast SRAMs mounted on a 72-pin, double-sided, FR4-printed circuit board. They are specially processed to operate from 3.0V to 3.6V for low-voltage memory systems.

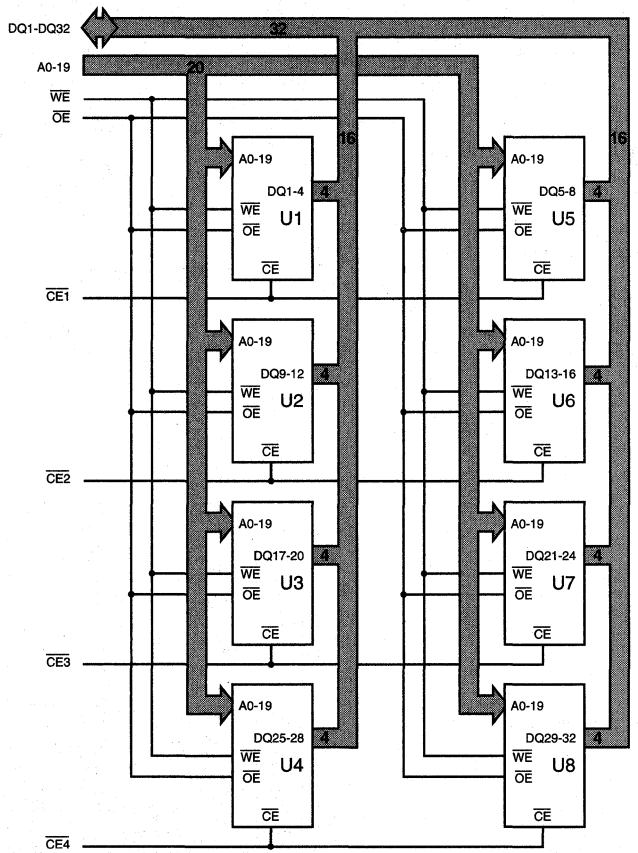
Data is written into the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in High-Z for additional flexibility in system design and memory expansion.

PD0 - PD3 identify the module's density allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage modules are ideal for mixed 3.3V and 5V systems.

NEW SRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



PRESENCE-DETECT
PD0 = Vss
PD1 = NC
PD2 = Vss
PD3 = NC

U1-U8 = MT5LC1M4D4DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	A0-A19, $\overline{WE}$, $\overline{OE}$	I_{LI1}	-8	8	µA	
		$\overline{CE1}$-$\overline{CE4}$	I_{LI2}	-2	2	µA	
Input/Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	DQ1-DQ32	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			V_{CC}	3.0	3.6	V	1

			MAX					
DESCRIPTION	CONDITIONS	SYMBOL	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	1,480	1,320	1,280	1,240	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	640	600	560	560	mA	
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	8	8	8	8	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance; A0-A19, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz V_{CC} = 3.3V	C_{I1}	48	pF	4
Input Capacitance; $\overline{CE1}$-$\overline{CE4}$		C_{I2}	12	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	8	pF	4

NEW SRAM MODULE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($0°C \le T_A \le 70°C$; Vcc = 3.3V ±0.3V)

DESCRIPTION		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MAX	MIN	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	15		20		25		35		ns	
Address access time	^tAA		15		20		25		35	ns	
Chip Enable access time	^tACE		15		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		7		8		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	4
Chip disable to power-down time	^tPD		15		20		25		35	ns	4
Output Enable access time	^tAOE		8		10		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		6		7		10		12	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	15		20		25		35		ns	
Chip Enable to end of write	^tCW	10		12		15		20		ns	
Address valid to end of write	^tAW	10		12		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	10		12		15		20		ns	
WRITE pulse width	$^tWP2$	12		15		15		20		ns	
Data setup time	^tDS	7		8		10		15		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		6		8		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

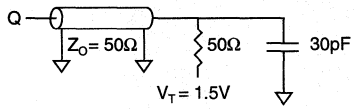


Fig. 1 OUTPUT LOAD EQUIVALENT

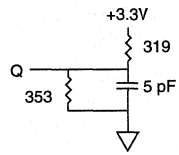


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

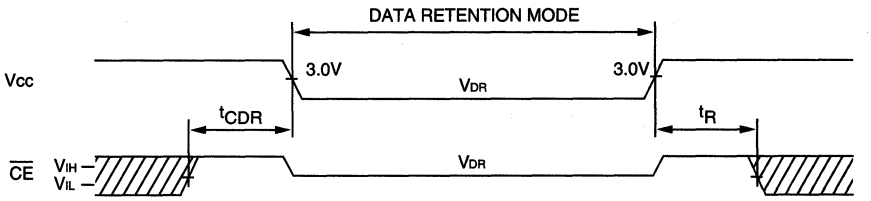
1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$. Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$. Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with C_L = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ${}^tRC$ = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 25°C.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

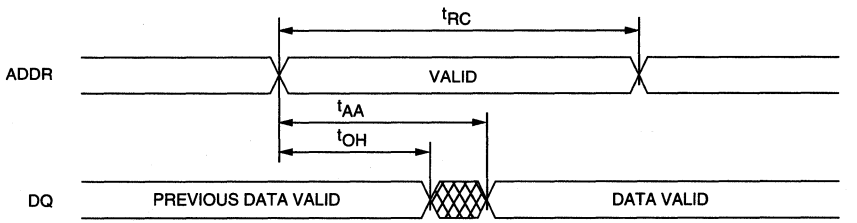
DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2			V	
Data Retention Current	$\overline{CE} \geq (V_{CC} -0.2V)$ $V_{IN} \geq (V_{CC} -0.2V)$ or $\leq 0.2V$	V_{CC} = 2V	I_{CCDR}			5.6	mA	
Chip Deselect to Data Retention Time		${}^tCDR$	0		—	ns	4	
Operation Recovery Time			${}^tR$	${}^tRC$			ns	4,11

NEW SRAM MODULE

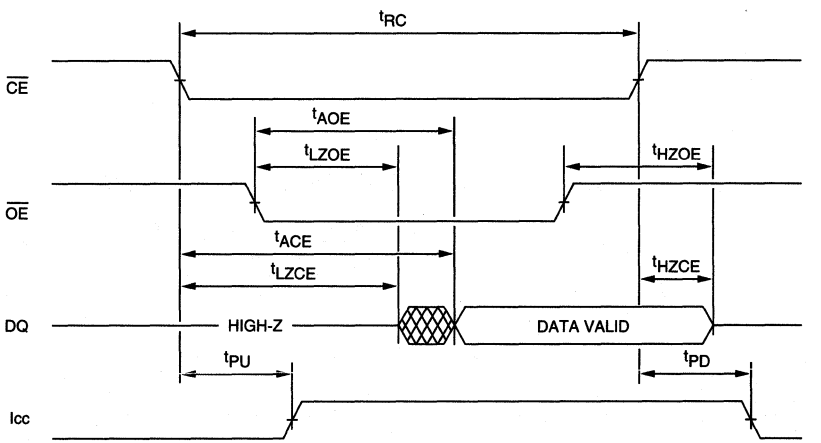
LOW Vcc DATA RETENTION WAVEFORM



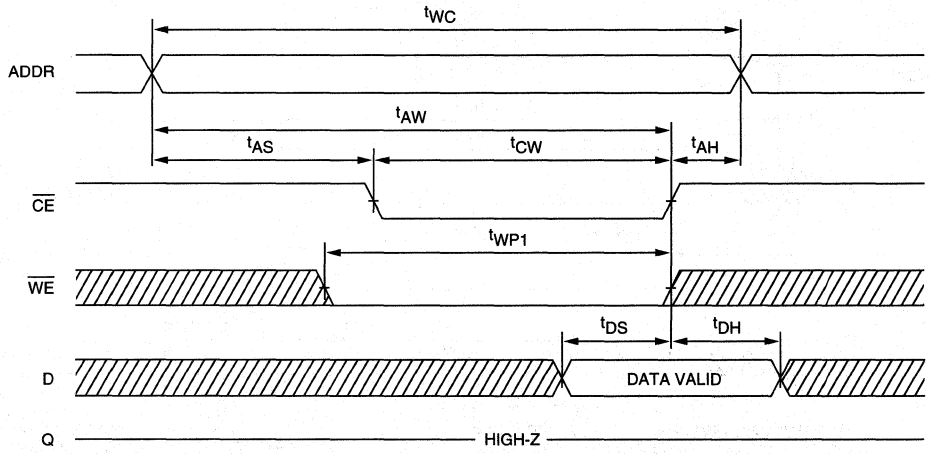
READ CYCLE NO. 1 [8, 9]



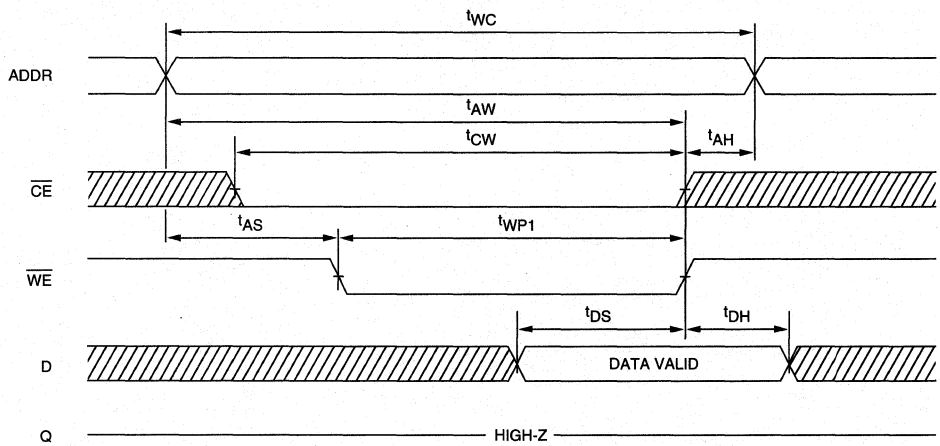
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)

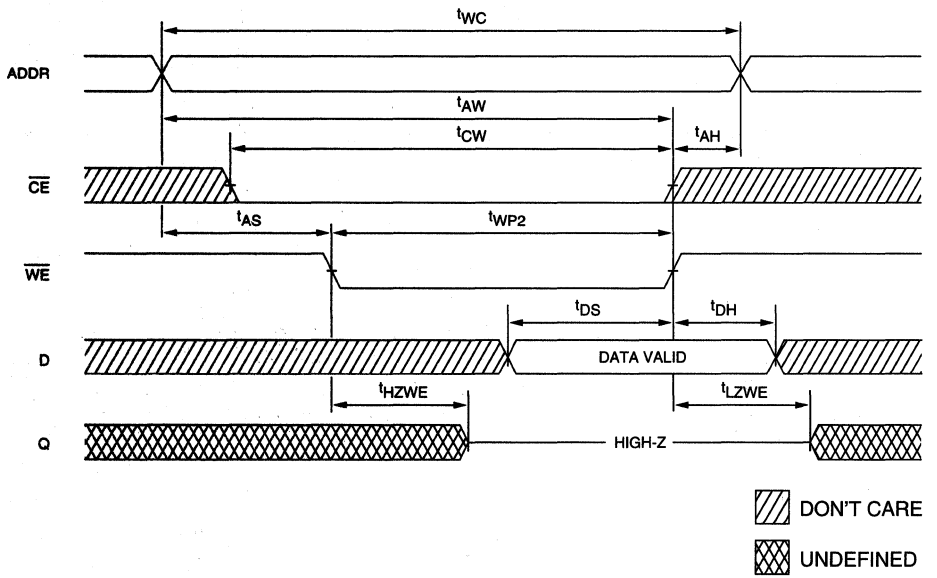


WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).

SYNCHRONOUS SRAM MODULE

32K x 64 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS AND BURST COUNTER

FEATURES

- 80 position dual read-out dual in-line memory module (DIMM) with 160 leads
- Fast access times: 9, 10, 11 and 12ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant common data I/O
- Individual BYTE WRITE control
- Clock controlled and registered inputs
- Internally self-timed WRITE cycle
- Burst control pins (interleaved T2 or linear burst T1)
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS — MARKING

- Timing
  - 9ns access/15ns cycle — -9
  - 10ns access/15ns cycle — -10
  - 11ns access/15ns cycle — -11
  - 12ns access/20ns cycle — -12
- Burst sequence
  - Linear Burst — T1
  - 486/Pentium™ Burst — T2
- Packages
  - 160-lead DIMM (gold) — G
- Low power (optional) — P
- 2V data retention, low power (optional) — L
- Part Number Example: MT2LSYT3264T2G-10 L

GENERAL DESCRIPTION

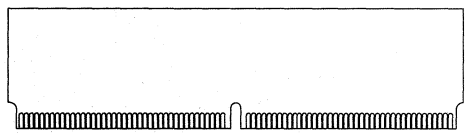
The Micron SyncBurst™ SRAM module family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT2LSYT3264T1/T2 module integrates two 32K x 32 synchronous SRAMs. All synchronous inputs pass through registers controlled by positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, data inputs, active LOW chip enables ($\overline{CE0}$-1), burst control inputs ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1, $\overline{ADV0}$-1) and byte write enables ($\overline{BW0}$-7).

Asynchronous inputs include the output enables ($\overline{OE0}$-1) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to eight bytes wide as controlled by the byte write enables.

PIN ASSIGNMENT (Top View)

160-Lead, Dual Read-out DIMM
(SF-1)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	41	Vss	81	Vss	121	Vss
2	DQ62	42	DQ10	82	DQ63	122	DQ11
3	Vcc	43	Vcc	83	RSVD	123	RSVD
4	DQ60	44	DQ8	84	DQ61	124	DQ9
5	Vcc	45	NC	85	RSVD	125	NC
6	DQ58	46	Vcc	86	DQ59	126	RSVD
7	DQ56	47	DQ6	87	DQ57	127	DQ7
8	Vss	48	DQ4	88	Vss	128	DQ5
9	NC	49	DQ2	89	NC	129	DQ3
10	DQ54	50	DQ0	90	DQ55	130	DQ1
11	DQ52	51	Vss	91	DQ53	131	Vss
12	DQ50	52	A0A	92	DQ51	132	A0B
13	Vss	53	A1A	93	Vss	133	A1B
14	DQ48	54	A2A	94	DQ49	134	A2B
15	DQ46	55	A3A	95	DQ47	135	A3B
16	DQ44	56	A5	96	DQ45	136	A4
17	DQ42	57	Vss	97	DQ43	137	Vss
18	Vss	58	A7	98	Vss	138	A6
19	DQ40	59	A9	99	DQ41	139	A8
20	NC	60	A11	100	NC	140	A10
21	DQ38	61	A13	101	DQ39	141	A12
22	DQ36	62	NC	102	DQ37	142	A14
23	DQ34	63	Vss	103	DQ35	143	Vss
24	Vss	64	PD0	104	Vss	144	NC
25	DQ32	65	Vss	105	DQ33	145	Vss
26	DQ30	66	RSVD	106	DQ31	146	CLK
27	DQ28	67	RSVD	107	DQ29	147	RSVD
28	DQ26	68	Vss	108	DQ27	148	Vss
29	DQ24	69	$\overline{BW6}$	109	DQ25	149	$\overline{BW7}$
30	Vss	70	$\overline{BW4}$	110	Vss	150	$\overline{BW5}$
31	NC	71	$\overline{BW2}$	111	NC	151	$\overline{BW3}$
32	DQ22	72	$\overline{BW0}$	112	DQ23	152	$\overline{BW1}$
33	DQ20	73	Vss	113	DQ21	153	Vss
34	Vcc	74	$\overline{ADSC0}$	114	RSVD	154	$\overline{ADSC1}$
35	DQ18	75	$\overline{CE0}$	115	DQ19	155	$\overline{CE1}$
36	Vss	76	$\overline{ADV0}$	116	Vss	156	$\overline{ADV1}$
37	DQ16	77	$\overline{OE0}$	117	DQ17	157	$\overline{OE1}$
38	Vcc	78	Vcc	118	RSVD	158	RSVD
39	DQ14	79	$\overline{ADSP0}$	119	DQ15	159	$\overline{ADSP1}$
40	DQ12	80	Vss	120	DQ13	160	Vss

GENERAL DESCRIPTION (continued)

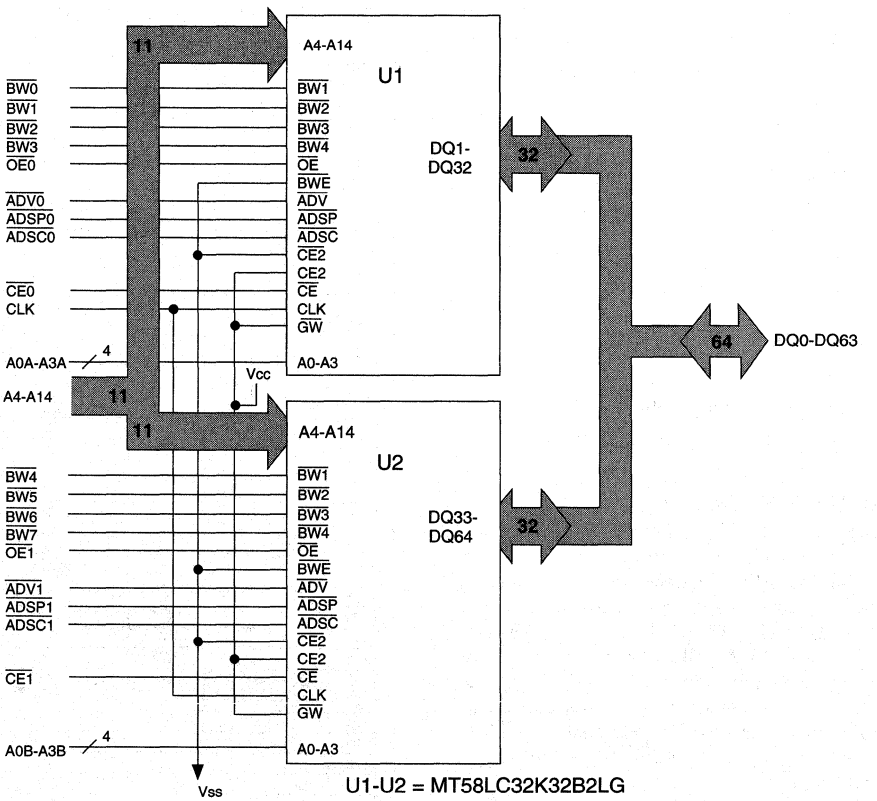
Burst operation can be initiated with either address status processor ($\overline{ADSP0}$-1) or address status controller ($\overline{ADSC0}$-1) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pins ($\overline{ADV0}$-1).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW0}$ controls DQ0-DQ7, $\overline{BW1}$ controls DQ8-DQ15, $\overline{BW2}$ controls DQ16-DQ23, $\overline{BW3}$ controls DQ24-DQ31 and so forth.

The "L" version of this module has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The module operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. This module is ideally suited to Pentium™ systems and those systems which benefit from a very wide data bus.

FUNCTIONAL BLOCK DIAGRAM
256KB
(32K x 64)



NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
56, 58-61, 136, 138-142	A4-A14	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
69-72, 149-152	$\overline{BW0}$-7	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW0}$ controls DQ0-DQ7. $\overline{BW1}$ controls DQ8-DQ15. $\overline{BW2}$ controls DQ16-DQ23. $\overline{BW3}$ controls DQ24-DQ31, and so forth. Data I/O are tristated if any of these eight inputs are LOW.
146	CLK	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
75, 155	$\overline{CE0}$-$\overline{CE1}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
52-55, 132-135	A0A-A3A, A0B-A3B	Input	Synchronous Address Input: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. These lower order address signals are provided for the two data banks to simplify the interface to many cache controllers.
77, 157	$\overline{OE0}$-$\overline{OE1}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
76, 156	$\overline{ADV0}$-$\overline{ADV1}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
79, 159	$\overline{ADSP0}$-$\overline{ADSP1}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH.
74, 154	$\overline{ADSC0}$-$\overline{ADSC1}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
66, 83, 85, 114, 118, 123, 126, 147, 158	RSVD	-	No Connect: These pins are reserved.

PIN DESCRIPTIONS (continued)

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
2, 4, 6-7, 10-12, 14, 16-17, 19, 21-23, 25-29, 32-33, 35, 37, 39-40, 42, 44, 47-50, 82, 84, 86-87, 90-92, 94-97, 99, 101-103, 105-109, 112-113, 115, 117, 119-120, 122, 124, 127-130	DQ0-DQ63	Input/ Output	SRAM Data I/O: Byte 1 is DQ0-DQ7; Byte 2 is DQ8-DQ15; Byte 3 is DQ16-DQ23; Byte 4 is DQ24-DQ31 and so forth. Input data must meet setup and hold times around the rising edge of CLK.
3, 5, 34, 38, 43, 46, 78	Vcc	Supply	Power Supply: +3.3V ±5%
1, 8, 13, 18, 24, 30, 36, 41, 51, 57, 63, 68, 73, 80, 81, 88, 93, 98, 104, 110, 116, 121, 131, 137, 143, 148, 153, 160	Vss	Supply	Ground: GND

INTERLEAVED BURST ADDRESS TABLE (MODE = NC) MT2LSYT3264T2

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = GND) MT2LSYT3264T1

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PRESENCE-DETECT TABLE

DENSITY	PD0
• 256KB	NC
512KB	Vss

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ0-63
Deselected Cycle, Power-down	None	H	X	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW0}$, $\overline{BW1}$, $\overline{BW2}$, etc.) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW0}$ enables writes to Byte 1 (DQ0-DQ7). $\overline{BW1}$ enables writes to Byte 2 (DQ8-DQ15). $\overline{BW2}$ enables writes to Byte 3 (DQ16-DQ23). $\overline{BW3}$ enables writes to Byte 4 (DQ24-DQ31) and so forth.
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +125°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	$\overline{BW0}$-7	I_{LI1}	-1	1	µA	
		A4-A15	I_{LI2}	-4	4	µA	
		All other inputs	I_{LI3}	-2	2	µA	
Output Leakage Current	Output(s) Disabled, 0V ≤ V_{OUT} ≤ V_{CC}		I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1, 11
Supply Voltage			V_{CC}	3.1	3.5	V	1

DESCRIPTION	CONDITIONS	SYM	VER	TYP	MAX -9	MAX -10	MAX -11	MAX -12	UNITS	NOTES
Power Supply Current: Operating	Device selected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; outputs open	I_{CC1}	ALL	360	540	540	500	450	mA	3, 12, 13
Power Supply Current: Idle	Device selected; V_{CC} = MAX; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; cycle time ≥ ^tKC MIN	I_{CC2}	ALL	56	90	90	90	80	mA	12, 13
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB1}	STD	1.0	10	10	10	10	mA	12, 13
			P	0.4	4	4	4	4	mA	
TTL Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB2}	STD	30	50	50	50	50	mA	12, 13
			P	16	36	36	36	36	mA	
Clock Running	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB3}	ALL	60	100	100	100	90	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A4-A14, CLK	T_A = 25°C; f = 1 MHz	C_{I1}		10	pF	4
Input Capacitance: $\overline{ADSP0}$-1 or $\overline{ADV0}$-1, $\overline{ADSC0}$-1	V_{CC} = 3.3V	C_{I2}		5	pF	4
Input Capacitance: $\overline{BW0}$-7, $\overline{OE0}$-1, $\overline{CE0}$-1, A0A-A3A, A0B-A3B		C_{I3}		5	pF	4
Input/Output Capacitance: DQ0-63		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (V_{CC} = 3.3V ±5%)

DESCRIPTION		-9		-10		-11		-12			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock											
Clock cycle time	^tKC	15		15		15		20		ns	
Clock HIGH time	^tKH	4		5		5		6		ns	
Clock LOW time	^tKL	4		5		5		6		ns	
Output Times											
Clock to output valid	^tKQ		9		10		11		12	ns	
Clock to output invalid	^tKQX	3		3		3		3		ns	
Clock to output in Low-Z	^tKQLZ	5		5		5		5		ns	6, 7
Clock to output in High-Z	^tKQHZ		5		5		5		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		5		5		5		6	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		5		5		5		6	ns	6, 7
Setup Times											
Address	^tAS	2.5		2.5		2.5		3		ns	8, 10
Address Status ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1)	^tADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{ADV0}$-1)	^tAAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{BW0}$-7)	^tWS	2.5		3		3		3		ns	8, 10
Data-in	^tDS	2.5		3		3		3		ns	8, 10
Chip Enable ($\overline{CE0}$-1)	^tCES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	^tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1)	^tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV0}$-1)	^tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{BW0}$-7)	^tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enable ($\overline{CE0}$-1)	^tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

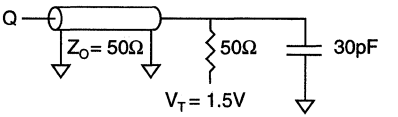


Fig. 1 OUTPUT LOAD EQUIVALENT

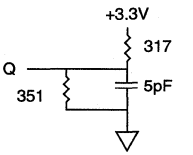


Fig. 2 OUTPUT LOAD EQUIVALENT

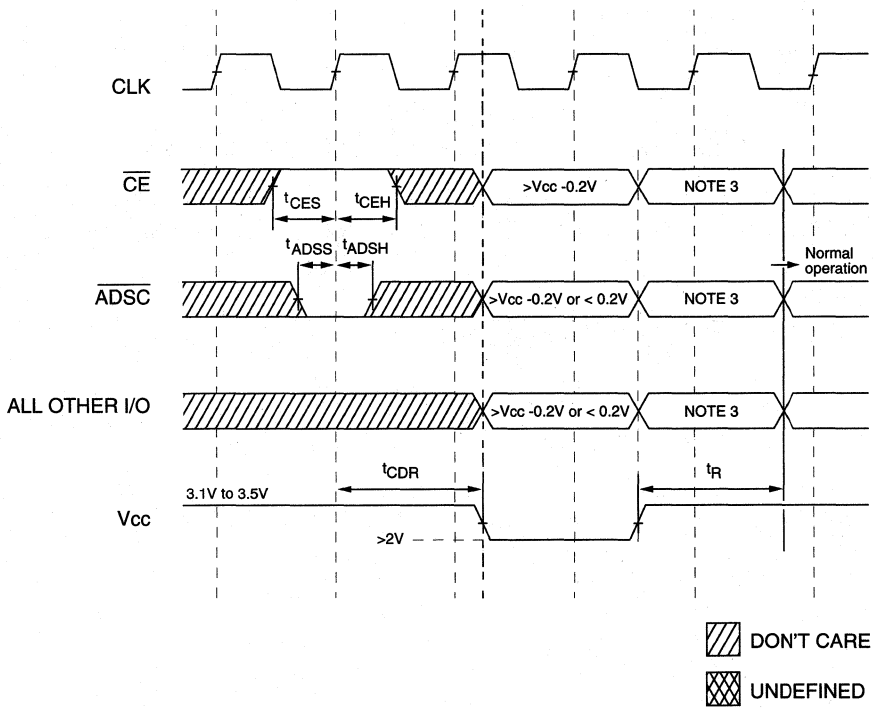
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the shown DC values.
12. "Device deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Typical values are measured at 25°C.
15. The device must have a deselect cycle applied at least one clock cycle before data retention mode is entered.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

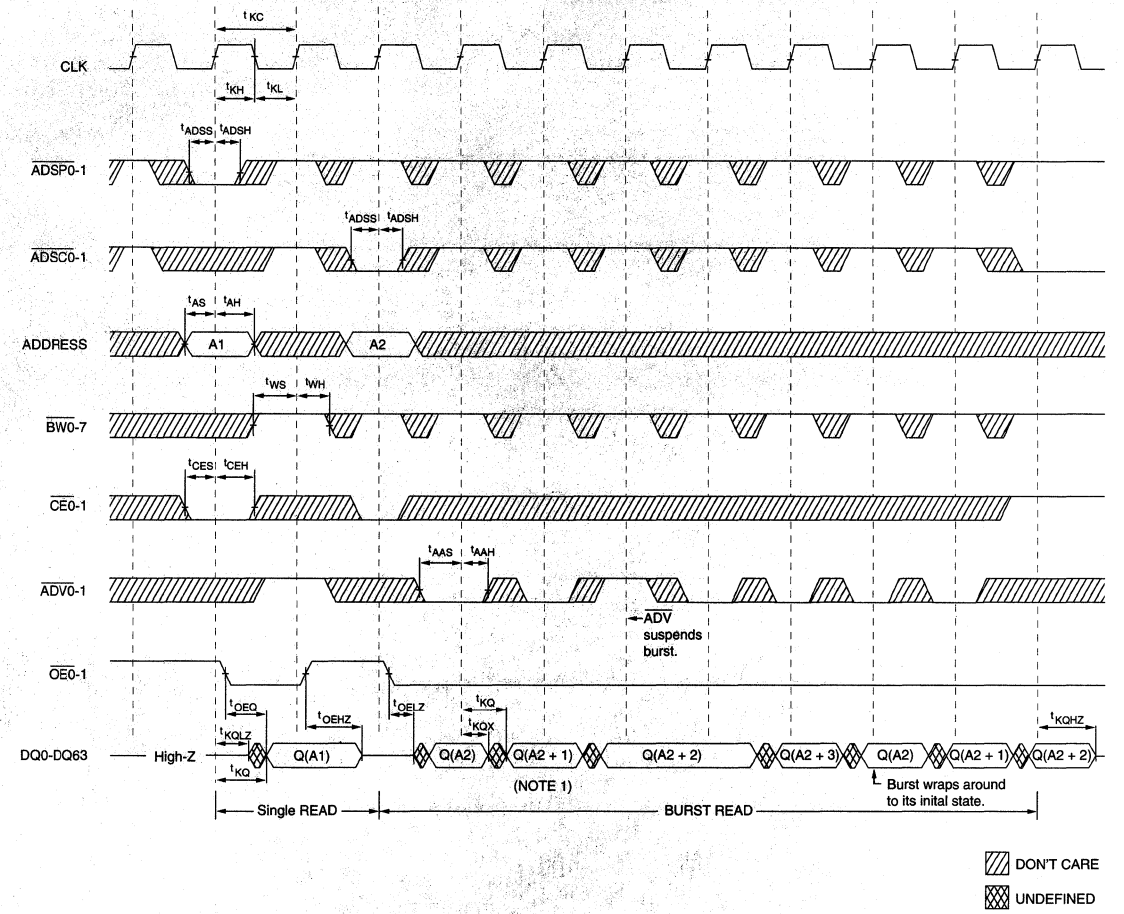
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2} \geq (V_{CC} - 0.2V)$, $CE2 \leq 0.2V$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$ $V_{CC} = 2V$	I_{CCDR}		TBD	µA	14
Chip Deselect to Data Retention Time		^tCDR	^tKC		ns	4, 15
Operation Recovery Time		^tR	^tKC		ns	4

LOW V_{CC} DATA RETENTION WAVEFORM



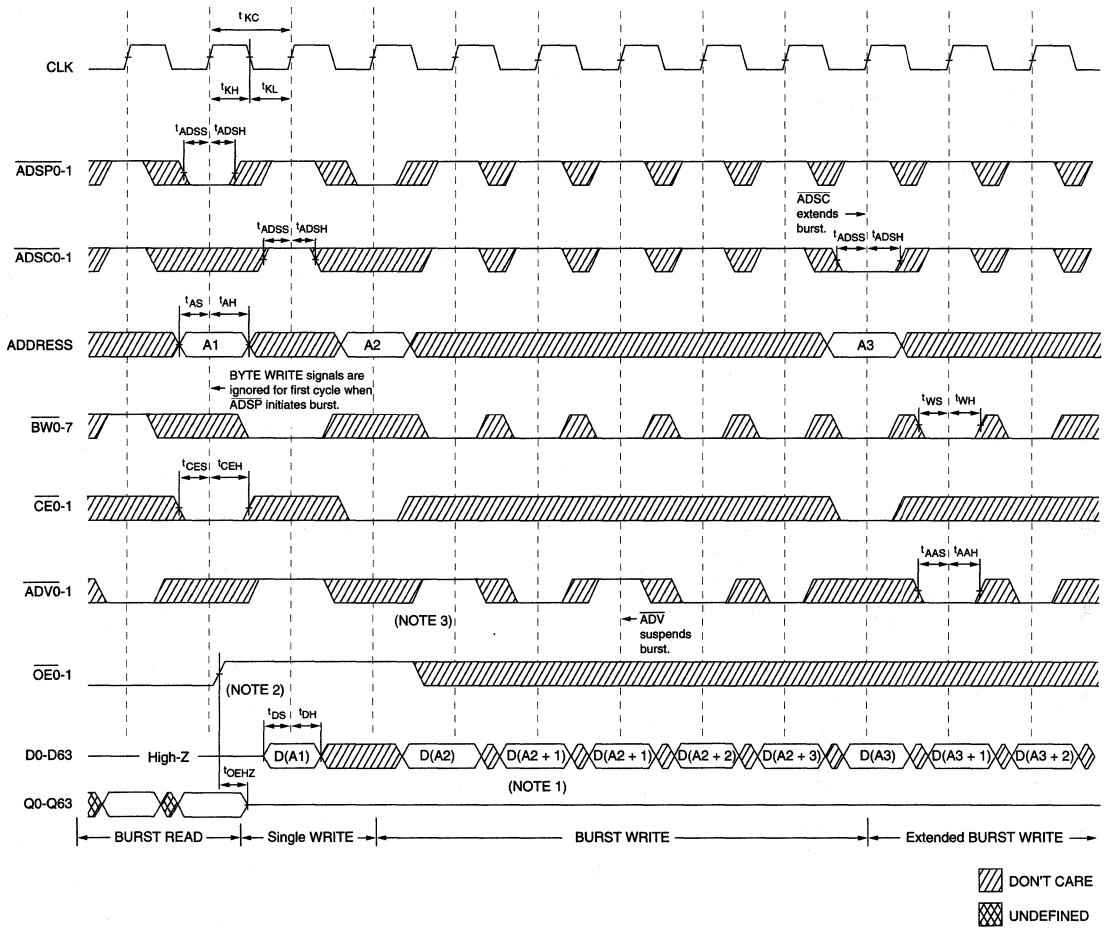
NOTE:
1. All inputs must be $\geq V_{CC}$ - 0.2V or $\leq$ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded.
2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.
3. The device control signals should be in a deselect state between the rising edge of V_{CC} and until ^tR is met.

READ TIMING



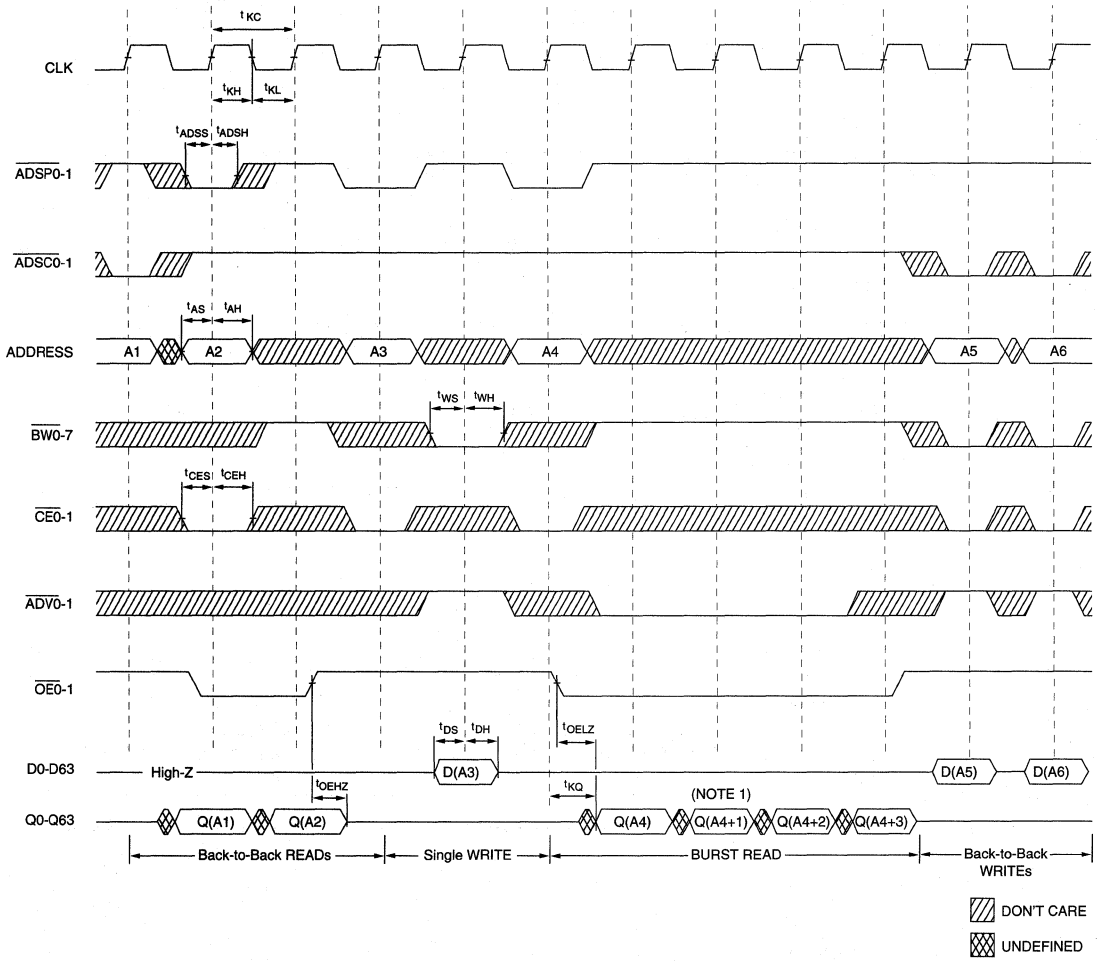
NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

WRITE TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING



NOTE:
1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.
2. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$ or $\overline{\text{ADV}}$ cycle is performed.

SYNCHRONOUS SRAM MODULE

32K x 64 SRAM

+3.3V SUPPLY, FULLY REGISTERED INPUTS, OUTPUTS AND BURST COUNTER

FEATURES

- 80 position dual read-out dual in-line memory module (DIMM) with 160 leads
- Fast access times: 5, 6, 7 and 8ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant common data I/O
- Individual BYTE WRITE control
- WRITE pass-through capability
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- Burst control pins (interleaved T4 or linear burst T6)
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS — MARKING

- Timing
  - 5ns access/10ns cycle — -5
  - 6ns access/12ns cycle — -6
  - 7ns access/15ns cycle — -7
  - 8ns access/20ns cycle — -8
- Burst sequence
  - Interleaved Burst — T4
  - Linear Burst — T6
- Packages
  - 160-lead DIMM (gold) — G
- Low power (optional) — P
- 2V data retention, low power (optional) — L
- Part Number Example: MT2LSYT3264T4G-6 L

GENERAL DESCRIPTION

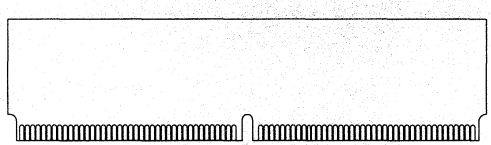
The Micron SyncBurst™ SRAM module family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT2LSYT3264T4/T6 module integrates two 32K x 32 synchronous SRAMs. All synchronous inputs pass through registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, data inputs, active LOW chip enables ($\overline{CE0}$-1), burst control inputs ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1, $\overline{ADV0}$-1) and byte write enables ($\overline{BW0}$-7).

Asynchronous inputs include the output enables ($\overline{OE0}$-1) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is

PIN ASSIGNMENT (Top View)

160-Lead, Dual Read-out DIMM
(SF-1)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	41	Vss	81	Vss	121	Vss
2	DQ62	42	DQ10	82	DQ63	122	DQ11
3	Vcc	43	Vcc	83	RSVD	123	RSVD
4	DQ60	44	DQ8	84	DQ61	124	DQ9
5	Vcc	45	NC	85	RSVD	125	NC
6	DQ58	46	Vcc	86	DQ59	126	RSVD
7	DQ56	47	DQ6	87	DQ57	127	DQ7
8	Vss	48	DQ4	88	Vss	128	DQ5
9	NC	49	DQ2	89	NC	129	DQ3
10	DQ54	50	DQ0	90	DQ55	130	DQ1
11	DQ52	51	Vss	91	DQ53	131	Vss
12	DQ50	52	A0A	92	DQ51	132	A0B
13	Vss	53	A1A	93	Vss	133	A1B
14	DQ48	54	A2A	94	DQ49	134	A2B
15	DQ46	55	A3A	95	DQ47	135	A3B
16	DQ44	56	A5	96	DQ45	136	A4
17	DQ42	57	Vss	97	DQ43	137	Vss
18	Vss	58	A7	98	Vss	138	A6
19	DQ40	59	A9	99	DQ41	139	A8
20	NC	60	A11	100	NC	140	A10
21	DQ38	61	A13	101	DQ39	141	A12
22	DQ36	62	NC	102	DQ37	142	A14
23	DQ34	63	Vss	103	DQ35	143	Vss
24	Vss	64	PD0	104	Vss	144	NC
25	DQ32	65	Vss	105	DQ33	145	Vss
26	DQ30	66	RSVD	106	DQ31	146	CLK
27	DQ28	67	RSVD	107	DQ29	147	RSVD
28	DQ26	68	Vss	108	DQ27	148	Vss
29	DQ24	69	$\overline{BW6}$	109	DQ25	149	$\overline{BW7}$
30	Vss	70	$\overline{BW4}$	110	Vss	150	$\overline{BW5}$
31	NC	71	$\overline{BW2}$	111	NC	151	$\overline{BW3}$
32	DQ22	72	$\overline{BW0}$	112	DQ23	152	$\overline{BW1}$
33	DQ20	73	Vss	113	DQ21	153	Vss
34	Vcc	74	$\overline{ADSC0}$	114	RSVD	154	$\overline{ADSC1}$
35	DQ18	75	$\overline{CE0}$	115	DQ19	155	$\overline{CE1}$
36	Vss	76	$\overline{ADV0}$	116	Vss	156	$\overline{ADV1}$
37	DQ16	77	$\overline{OE0}$	117	DQ17	157	$\overline{OE1}$
38	Vcc	78	Vcc	118	RSVD	158	RSVD
39	DQ14	79	$\overline{ADSP0}$	119	DQ15	159	$\overline{ADSP1}$
40	DQ12	80	Vss	120	DQ13	160	Vss

GENERAL DESCRIPTION (continued)

also asynchronous. WRITE cycles can be from one to eight bytes wide as controlled by the byte write enables.

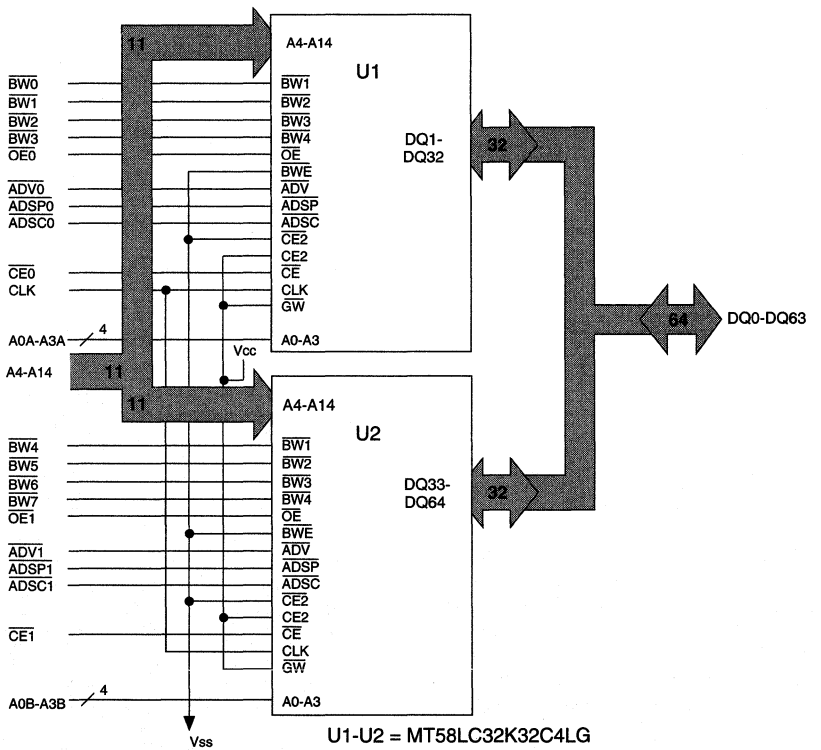
Burst operation can be initiated with either address status processor ($\overline{ADSP0}$-1) or address status controller ($\overline{ADSC0}$-1) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pins ($\overline{ADV0}$-1).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW0}$ controls DQ0-DQ7, $\overline{BW1}$ controls DQ8-DQ15, $\overline{BW2}$ controls DQ16-DQ23, $\overline{BW3}$ controls DQ24-DQ31 and so forth.

The "L" version of this module has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The module operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. This module is ideally suited to Pentium™ and PowerPC™ pipelined systems and systems that benefit from a very wide high-speed data bus.

FUNCTIONAL BLOCK DIAGRAM
256KB
(32K x 64)



NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
56, 58-61, 136, 138-142	A4-A14	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
69-72, 149-152	$\overline{BW0}$-7	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW0}$ controls DQ0-DQ7. $\overline{BW1}$ controls DQ8-DQ15. $\overline{BW2}$ controls DQ16-DQ23. $\overline{BW3}$ controls DQ24-DQ31, and so forth. Data I/O are tristated if any of these eight inputs are LOW.
146	CLK	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
75, 155	$\overline{CE0}$-$\overline{CE1}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
52-55, 132-135	A0A-A3A, A0B-A3B	Input	Synchronous Address Input: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. These lower order address signals are provided for the two data banks to simplify the interface to many cache controllers.
77, 157	$\overline{OE0}$-$\overline{OE1}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
76, 156	$\overline{ADV0}$-$\overline{ADV1}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
79, 159	$\overline{ADSP0}$-$\overline{ADSP1}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH.
74, 154	$\overline{ADSC0}$-$\overline{ADSC1}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
66, 83, 85, 114, 118, 123, 126, 147, 158	RSVD	-	No Connect: These pins are reserved.

PIN DESCRIPTIONS (continued)

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
2, 4, 6-7, 10-12, 14, 16-17, 19, 21-23, 25-29, 32-33, 35, 37, 39-40, 42, 44, 47-50, 82, 84, 86-87, 90-92, 94-97, 99, 101-103, 105-109, 112-113, 115, 117, 119-120, 122, 124, 127-130	DQ0-DQ63	Input/ Output	SRAM Data I/O: Byte 1 is DQ0-DQ7; Byte 2 is DQ8-DQ15; Byte 3 is DQ16-DQ23; Byte 4 is DQ24-DQ31 and so forth. Input data must meet setup and hold times around the rising edge of CLK.
3, 5, 34, 38, 43, 46, 78	Vcc	Supply	Power Supply: +3.3V ±5%
1, 8, 13, 18, 24, 30, 36, 41, 51, 57, 63, 68, 73, 80, 81, 88, 93, 98, 104, 110, 116, 121, 131, 137, 143, 148, 153, 160	Vss	Supply	Ground: GND

INTERLEAVED BURST ADDRESS TABLE (MODE = NC) MT2LSYT3264T4

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = GND) MT2LSYT3264T6

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{BWs}$	OPERATION	$\overline{CE}$	$\overline{BWs}$	$\overline{OE}$	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L	Initiate READ cycle Register A(n), Q = D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L	No new cycle Q = D(n-1)	H	H	L	No carry-over from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L	No new cycle Q = HIGH-Z	H	H	H	No carry-over from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1), data = D(n-1)	One L	No new cycle Q = D(n-1) for one byte	H	H	L	No carry-over from previous cycle

NOTE: Previous cycle may be either BURST or NONBURST cycle.

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ0-63
Deselected Cycle, Power-down	None	H	X	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW0}$, $\overline{BW1}$, $\overline{BW2}$, etc.) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW0}$ enables writes to Byte 1 (DQ0-DQ7). $\overline{BW1}$ enables writes to Byte 2 (DQ8-DQ15). $\overline{BW2}$ enables writes to Byte 3 (DQ16-DQ23). $\overline{BW3}$ enables writes to Byte 4 (DQ24-DQ31) and so forth.
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

PRESENCE-DETECT TABLE

DENSITY	PD0
• 256KB	NC
512KB	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss .. .... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +125°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	$\overline{BW0}$-7	I_{LI1}	-1	1	µA	
		A4-A15	I_{LI2}	-4	4	µA	
		All other inputs	I_{LI3}	-2	2	µA	
Output Leakage Current	Output(s) Disabled, 0V ≤ V_{OUT} ≤ V_{CC}		I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			V_{CC}	3.1	3.5	V	1

					MAX					
DESCRIPTION	CONDITIONS	SYM	VER	TYP	-5	-6	-7	-8	UNITS	NOTES
Power Supply Current: Operating	Device selected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; outputs open	I_{CC1}	ALL	360	720	630	540	450	mA	3, 12
Power Supply Current: Idle	Device selected; V_{CC} = MAX; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; cycle time ≥ ^tKC MIN	I_{CC2}	ALL	60	120	110	100	90	mA	12, 13
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB1}	STD	1.0	10	10	10	10	mA	12, 13
			P	0.4	4	4	4	4	mA	
TTL Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB2}	STD	30	50	50	50	50	mA	12, 13
			P	16	36	36	36	36	mA	
Clock Running	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB3}	ALL	60	120	110	100	90	mA	12, 13

SYNCHRONOUS SRAM MODULE

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A4-A14, CLK	T_A = 25°C; f = 1 MHz	C_{I1}		10	pF	4
Input Capacitance: $\overline{ADSP0}$-1, $\overline{ADV0}$-1, $\overline{OE0}$-1, $\overline{CE0}$-1	Vcc = 3.3V	C_{I2}		5	pF	4
Input Capacitance: $\overline{BW0}$-7, $\overline{ADSC0}$-1, A0A-A3A, A0B-A3B		C_{I3}		5	pF	4
Input/Output Capacitance: DQ0-63		C_O		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (Vcc = 3.3V ±5%)

DESCRIPTION		-5		-6		-7		-8			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock											
Clock cycle time	^tKC	10		12		15		20		ns	
Clock HIGH time	^tKH	4		4.5		5		6		ns	
Clock LOW time	^tKL	4		4.5		5		6		ns	
Output Times											
Clock to output valid	^tKQ		5		6		7		8	ns	
Clock to output invalid	^tKQX	2		2		2		2		ns	
Clock to output in Low-Z	^tKQLZ	4		5		5		5		ns	6, 7
Clock to output in High-Z	^tKQHZ		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		5		5		5		6	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		4		5		6		6	ns	6, 7
Setup Times											
Address	^tAS	2.5		2.5		2.5		3		ns	8, 10
Address Status ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1)	^tADSS	2.5		2.5		2.5		3		ns	8, 10
Address Advance ($\overline{ADV0}$-1)	^tAAS	2.5		2.5		2.5		3		ns	8, 10
Byte Write Enables ($\overline{BW0}$-7)	^tWS	2.5		2.5		2.5		3		ns	8, 10
Data-in	^tDS	2.5		2.5		2.5		3		ns	8, 10
Chip Enable ($\overline{CE0}$-1)	^tCES	2.5		2.5		2.5		3		ns	8, 10
Hold Times											
Address	^tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1)	^tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV0}$-1)	^tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{BW0}$-7)	^tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enable ($\overline{CE0}$-1)	^tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

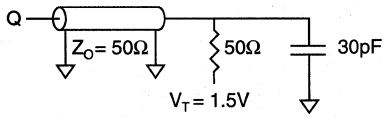


Fig. 1 OUTPUT LOAD EQUIVALENT

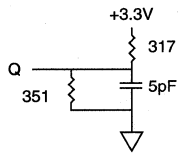


Fig. 2 OUTPUT LOAD EQUIVALENT

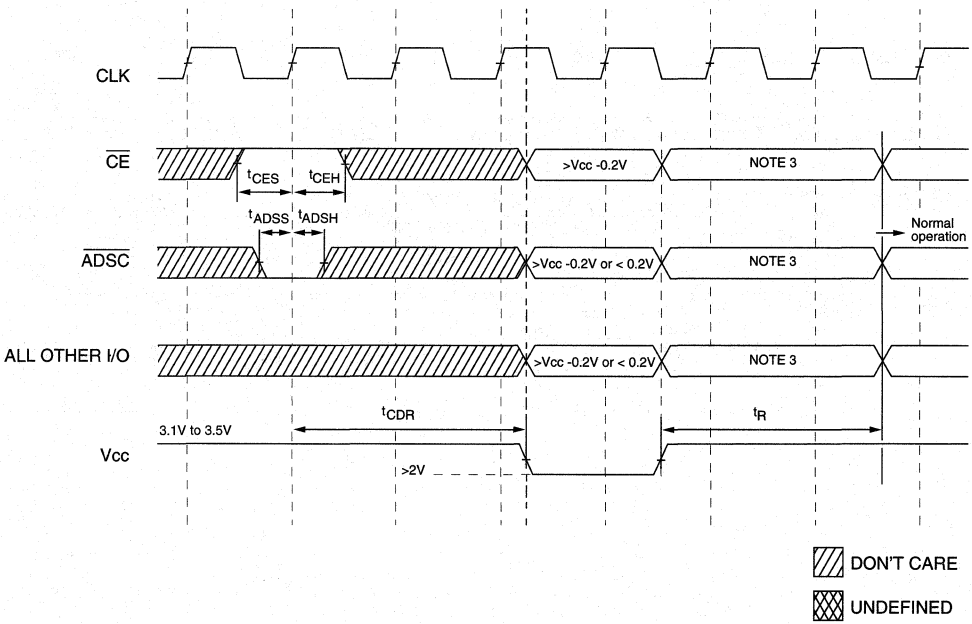
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the shown DC values.
12. "Device deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Typical values are measured at 25°C.
15. The device must have a deselect cycle applied at least two clock cycles before data retention mode is entered.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

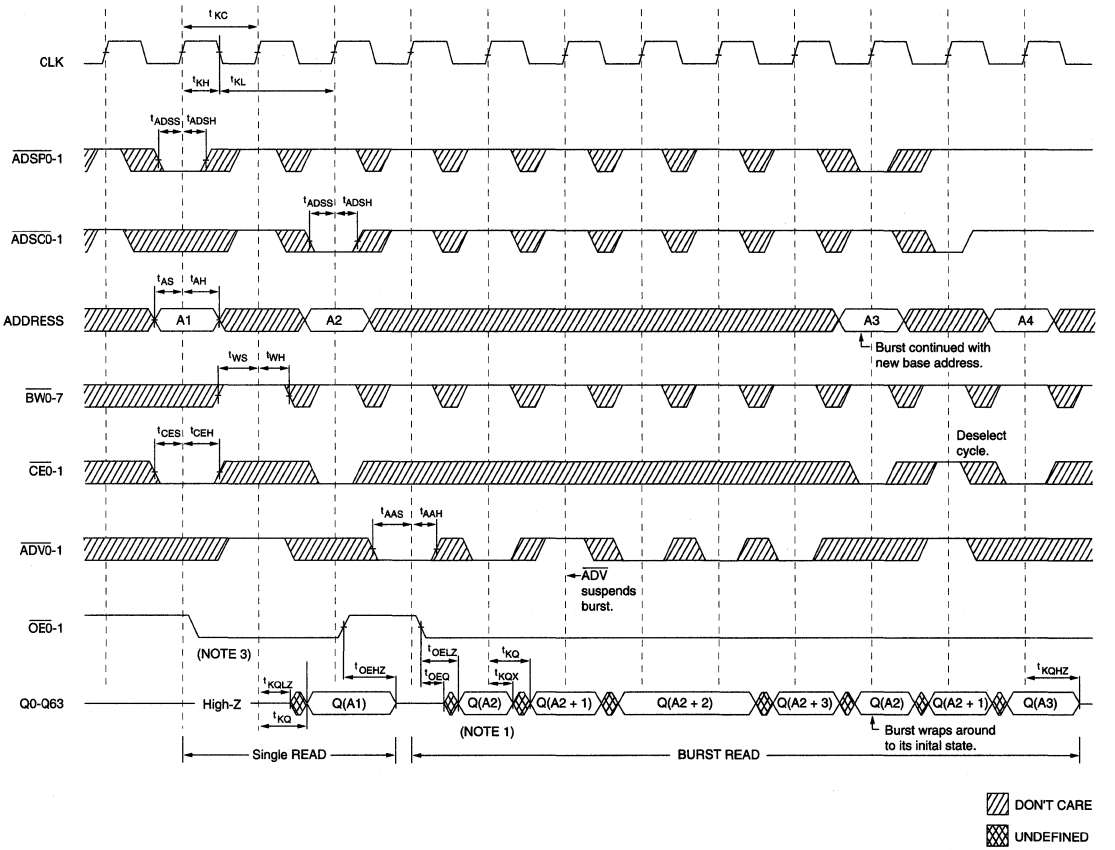
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2} \geq (V_{CC} - 0.2V)$, $CE2 \leq 0.2V$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$ $V_{CC} = 2V$	I_{CCDR}		TBD	µA	14
Chip Deselect to Data Retention Time		^tCDR	2 ^tKC		ns	4, 15
Operation Recovery Time		^tR	2 ^tKC		ns	4

LOW V_{CC} DATA RETENTION WAVEFORM



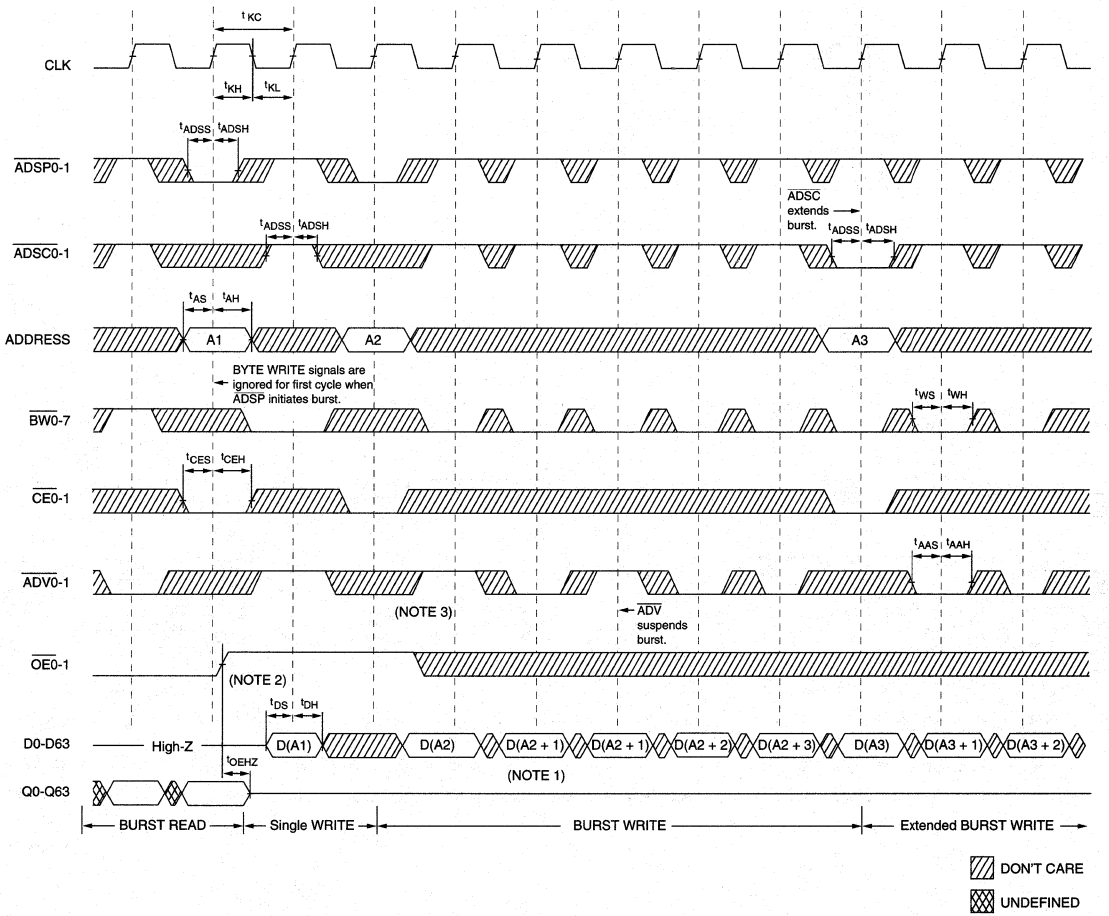
NOTE:
1. All inputs must be ≥ V_{CC} - 0.2V or ≤ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded.
2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.
3. The device control signals should be in a deselect state between the rising edge of V_{CC} and until ^tR is met.

READ TIMING



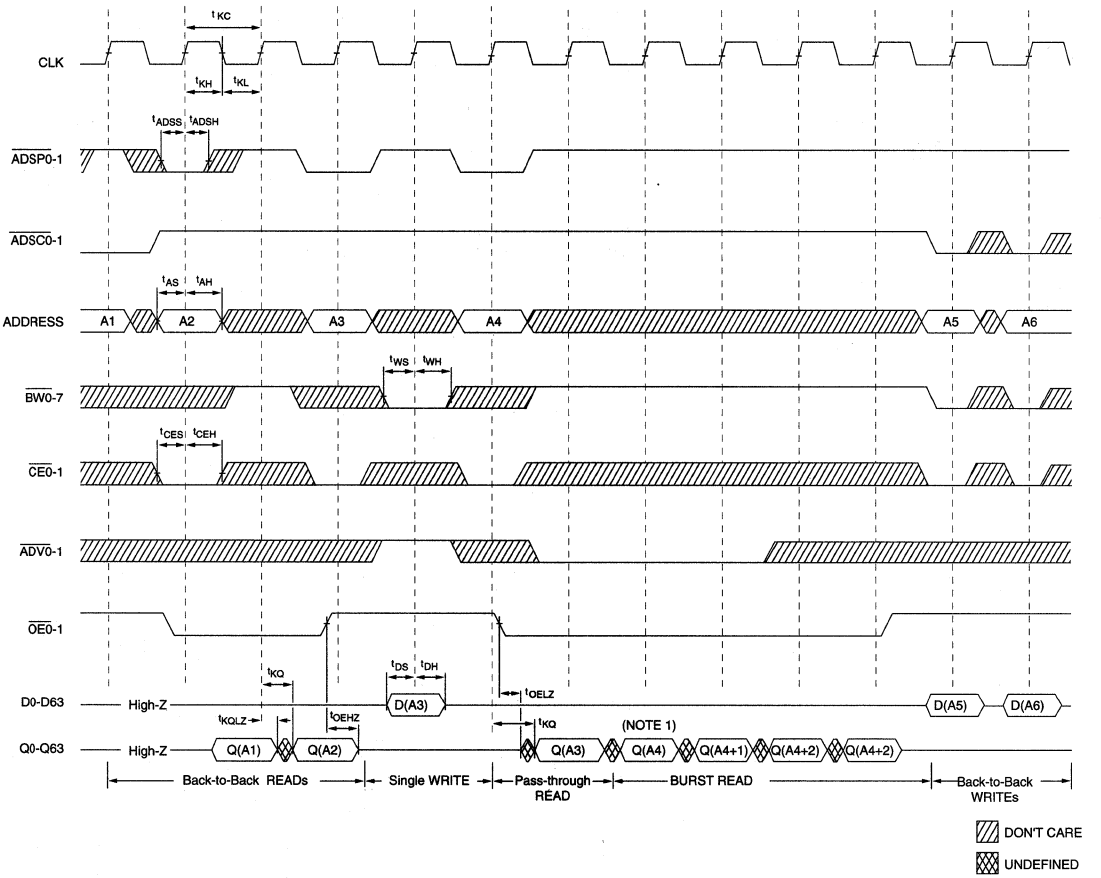
NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

WRITE TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING



NOTE:
1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.
2. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$ or $\overline{\text{ADV}}$ cycle is performed.
3. Back-to-back READs may be controlled by either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$.

SYNCHRONOUS SRAM MODULE

32K x 64 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS AND BURST COUNTER

FEATURES

- 80 position dual-read-out dual in-line memory module (DIMM) with 160 leads
- Fast access times: 9, 10, 11 and 12ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant common data I/O
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Burst control pins (interleaved or linear burst)
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS — MARKING

- Timing
  - 9ns access/15ns cycle — -9
  - 10ns access/15ns cycle — -10
  - 11ns access/15ns cycle — -11
  - 12ns access/20ns cycle — -12
- Packages
  - 160-lead DIMM (gold) — G
- Low power (optional) — P
- 2V data retention, low power (optional) — L
- Part Number Example: MT2LSYT3264B2G-9 L

GENERAL DESCRIPTION

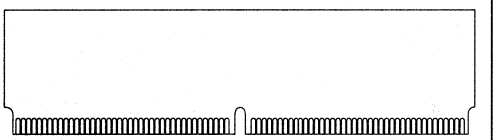
The Micron Synchronous SRAM module family employs high- speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double- layer metal, double-layer polysilicon technology.

The MT2LSYT3264B2 module integrates two 32K x 32 synchronous SRAMs. All synchronous inputs pass through registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and byte write enables ($\overline{BW0}$ - $\overline{BW7}$, $\overline{BWE}$) and global write ($\overline{GW}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK) and burst mode (MODE). The Data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to eight bytes wide as controlled by the byte write enables.

PIN ASSIGNMENT (Top View)

160-Lead, Dual Read-out DIMM
(SF-1)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	41	$\overline{GW}$	81	Vss	121	CE2
2	DQ0	42	Vcc2	82	DQ1	122	RSVD
3	Vcc2	43	RSVD	83	RSVD	123	RSVD
4	DQ2	44	A13	84	DQ3	124	A14
5	DQ4	45	MODE	85	DQ5	125	$\overline{ADV}$
6	DQ6	46	A15	86	DQ7	126	A16
7	RSVD	47	A17	87	DQ8	127	NC
8	Vss	48	NC	88	Vss	128	NC
9	DQ9	49	DQ32	89	DQ10	129	DQ33
10	DQ11	50	NC	90	DQ12	130	NC
11	DQ13	51	Vss	91	DQ14	131	Vss
12	Vcc2	52	DQ34	92	RSVD	132	DQ35
13	DQ15	53	DQ36	93	RSVD	133	DQ37
14	DQ16	54	DQ38	94	Vss	134	DQ39
15	Vss	55	DQ40	95	DQ17	135	RSVD
16	DQ18	56	$\overline{BW4}$	96	DQ19	136	$\overline{BW5}$
17	DQ20	57	Vss	97	DQ21	137	Vss
18	$\overline{OE}$	58	$\overline{BW6}$	98	DQ22	138	$\overline{BW7}$
19	Vss	59	DQ41	99	Vss	139	DQ42
20	$\overline{BW0}$	60	DQ43	100	$\overline{BW1}$	140	DQ44
21	DQ23	61	DQ45	101	RSVD	141	DQ46
22	DQ24	62	Vcc2	102	DQ25	142	RSVD
23	Vcc2	63	DQ47	103	RSVD	143	DQ48
24	DQ26	64	RSVD	104	DQ27	144	DQ49
25	DQ28	65	DQ50	105	DQ29	145	DQ51
26	DQ30	66	DQ52	106	DQ31	146	DQ53
27	RSVD	67	DQ54	107	A6	147	DQ55
28	A5	68	Vss	108	A8	148	Vss
29	A7	69	PRD0	109	A10	149	PRD1
30	A9	70	Vcc2	110	A12	150	RSVD
31	$\overline{BW2}$	71	DQ56	111	$\overline{BW3}$	151	RSVD
32	Vss	72	DQ57	112	Vss	152	DQ58
33	$\overline{BWE}$	73	Vss	113	CLK	153	Vss
34	A11	74	DQ59	114	A3	154	DQ60
35	A4	75	DQ61	115	$\overline{CE2}$	155	DQ62
36	RSVD	76	DQ63	116	RSVD	156	RSVD
37	$\overline{ADSC}$	77	PRD2	117	$\overline{ADSP}$	157	PRD3
38	RSVD	78	Vcc2	118	RSVD	158	RSVD
39	$\overline{CE}$	79	NC	119	RSVD	15	NC
40	Vss	80	Vss	120	Vss	160	Vss

GENERAL DESCRIPTION (continued)

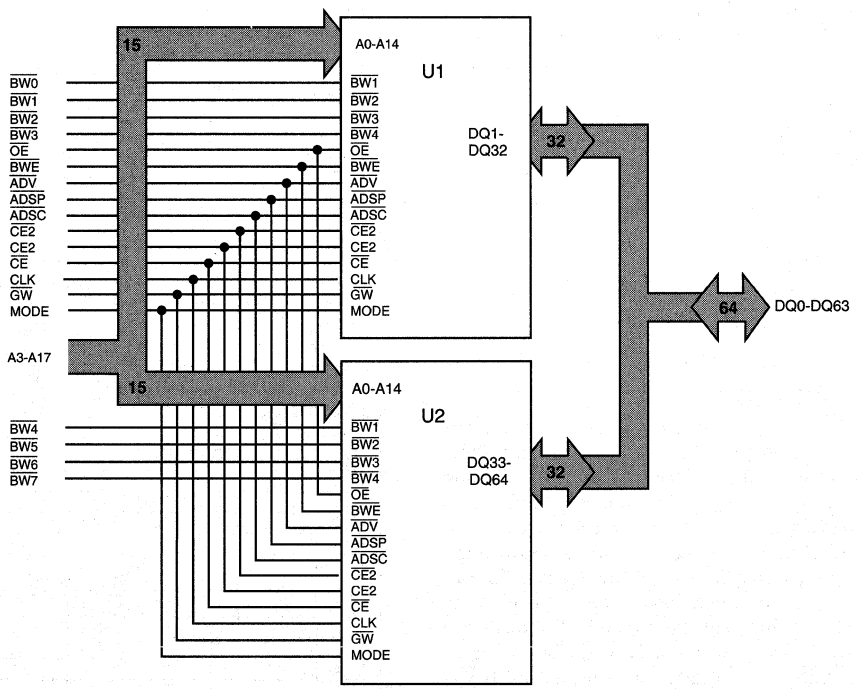
Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW0}$ controls DQ0-DQ7, $\overline{BW1}$ controls DQ8-DQ15, $\overline{BW2}$ controls DQ16-DQ23, $\overline{BW3}$ controls DQ24-DQ31 and so forth, conditioned by $\overline{BWE}$ being LOW. $\overline{GW}$ LOW causes all bytes to be written.

The "L" version of this module has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The module operates from a +3.3V power supply and all inputs and outputs are TTL compatible and 5V tolerant. This module is ideally suited to Pentium™ and Power PC™ systems and systems that benefit from a very wide data bus. The module is also ideal in generic 32- and 64-bit-wide applications. For additional functional and timing information consult the MT58LC32K32B2 synchronous SRAM data sheet.

FUNCTIONAL BLOCK DIAGRAM
256KB
(32K x 64)



U1-U2 = MT58LC32K32B2LG

NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See MT58LC32K32B2 synchronous SRAM data sheet for more detailed functional information.

PIN DESCRIPTIONS

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
28-30, 34-35, 44, 46-47, 107-110, 114, 124, 126	A3-A17	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
20, 31, 56, 58, 100, 111, 136, 138	$\overline{BW0}$-7	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when $\overline{BWE}$ is LOW and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW0}$ controls DQ0-DQ7. $\overline{BW1}$ controls DQ8-DQ15. $\overline{BW2}$ controls DQ16-DQ23. $\overline{BW3}$ controls DQ24-DQ31, and so forth. Data I/O are tristated if any of these eight inputs are LOW.
113	CLK	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
39	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
121	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to nable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
115	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
18	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
125	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
117	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$, but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.

PIN DESCRIPTIONS (continued)

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
37	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
7, 27, 36, 38, 43, 64, 83, 92, 93, 101, 103, 116, 118, 119, 122, 123, 135, 142, 150, 151, 156, 158	RSVD	-	No Connect: These pins are reserved.
33	$\overline{BWE}$	Input	Byte Write Enable: This active low input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
41	$\overline{GW}$	Input	Global Write: This active low input allows a full 32-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BW}$n lines and must meet the setup and hold times around the rising edge of CLK.
45	MODE	Input	Mode: This input selects the burst sequence. A low on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST. Do not alter input state while device is operating.
2, 4-6, 9-11, 13-14, 16-17, 21-22, 24-26, 49, 52-55, 59-61, 63, 65-67, 71-72, 74-76, 82, 84-87, 89-91, 95-98, 102, 104-106, 129, 132-134, 139-141, 143-147, 152, 154-155	DQ0-DQ63	Input/ Output	SRAM Data I/O: Byte 1 is DQ0-DQ7; Byte 2 is DQ8-DQ15; Byte 3 is DQ16-DQ23; Byte 4 is DQ24-DQ31 and so forth. Input data must meet setup and hold times around the rising edge of CLK.
3, 12, 23, 42, 62, 70, 78	Vcc2	Supply	Power Supply: +3.3V ±5%
1, 8, 15, 19, 32, 40, 51, 57, 68, 73, 80, 81, 88, 94, 99, 112, 120, 131, 137, 148, 153, 160	Vss	Supply	Ground: GND

PRESENCE-DETECT TABLE

Description	Size	PRD3	PRD2	PRD1	PRD0
None		NC	NC	NC	NC
Synchronous Pipelined	256KB	NC	Vss	NC	NC
Synchronous Pipelined	512KB	NC	Vss	NC	Vss
Synchronous	256KB	NC	Vss	Vss	NC
Synchronous	512KB	NC	Vss	Vss	Vss
Asynchronous	256KB	NC	NC	NC	Vss
Asynchronous	512KB	NC	NC	Vss	NC
Reserved		NC	NC	Vss	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +125°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	$\overline{BW}$0-7	I_{LI1}	-1	1	µA	7
		A3-A17	I_{LI2}	-4	4	µA	7
		All other inputs	I_{LI3}	-2	2	µA	7
Output Leakage Current	Output(s) Disabled, 0V ≤ V_{OUT} ≤ V_{CC}		I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			V_{CC}	3.1	3.5	V	1

DESCRIPTION	CONDITIONS	SYM	VER	TYP	MAX -9	MAX -10	MAX -11	MAX -12	UNITS	NOTES
Power Supply Current: Operating	Device selected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; outputs open	I_{CC1}	ALL	360	540	540	500	450	mA	3, 5, 6
Power Supply Current: Idle	Device selected; V_{CC} = MAX; $\overline{GW}$, $\overline{BW}$, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; cycle time ≥ ^tKC MIN	I_{CC2}	ALL	56	90	90	90	80	mA	5, 6
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB1}	STD	1.0	10	10	10	10	mA	5, 6
			P	0.4	4	4	4	4	mA	
TTL Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB2}	STD	30	50	50	50	50	mA	5, 6
			P	16	36	36	36	36	mA	
Clock Running	Device deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB3}	ALL	60	100	100	100	90	mA	5, 6

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A3-A17, $\overline{ADSC}$, $\overline{GW}$, MODE	T_A = 25°C; f = 1 MHz	C_{I1}		10	pF	4
Input Capacitance: $\overline{ADSP}$, $\overline{ADV}$, CLK, $\overline{OE}$, $\overline{CE}$, $\overline{BWE}$	V_{CC} = 3.3V	C_{I2}		10	pF	4
Input Capacitance: $\overline{BW0}$-7		C_{I3}		5	pF	4
Input/Output Capacitance: DQ0-63		C_O		8	pF	4

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2}$ ≥ (V_{CC} -0.2V), CE2 ≤ 0.2V V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V V_{CC} = 2V	I_{CCDR}		TBD	µA	8
Chip Deselect to Data Retention Time		^tCDR	^tKC		ns	4, 9
Operation Reccvery Time		^tR	^tKC		ns	4

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: V_{IH} ≤ +6.0V for t ≤ ^tKC /2.
   Undershoot: V_{IL} ≥ -2.0V for t ≤ ^tKC /2.
   Power-up: V_{IH} ≤ +6.0V and V_{CC} ≤ 3.1V for t ≤ 200ms
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. "Device deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device selected" means device is active (not in POWER-DOWN mode).
6. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
7. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
8. Typical values are measured at 25°C.
9. The device must have a deselect cycle applied at least one clock cycle before data retention mode is entered.

SYNCHRONOUS SRAM MODULE

32K x 64 SRAM

+3.3V SUPPLY, FULLY REGISTERED INPUTS, OUTPUTS AND BURST COUNTER

FEATURES

- 80 position dual-read-out dual in-line memory module (DIMM) with 160 leads
- Fast access times: 5, 6, 7 and 8ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant common data I/O
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- WRITE pass-through capability
- Burst control pins (interleaved or linear burst)
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS — MARKING

- Timing
  - 5ns access/10ns cycle — -5
  - 6ns access/12ns cycle — -6
  - 7ns access/15ns cycle — -7
  - 8ns access/20ns cycle — -8
- Packages
  - 160-lead DIMM (gold) — G
- Low power (optional) — P
- 2V data retention, low power (optional) — L
- Part Number Example: MT2LSYT3264C4G-5 P

GENERAL DESCRIPTION

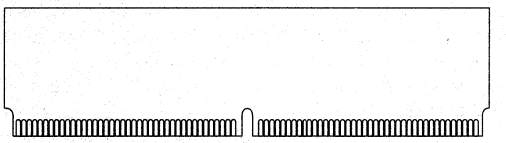
The Micron Synchronous SRAM module family employs high- speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double- layer metal, double-layer polysilicon technology.

The MT2LSYT3264C4 module integrates two 32K x 32 synchronous SRAMs. All synchronous inputs pass through registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2,$\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and byte write enables ($\overline{BW0}$ - $\overline{BW7}$, $\overline{BWE}$) and global write ($\overline{GW}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK) and burst mode (MODE). The Data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be

PIN ASSIGNMENT (Top View)

160-Lead, Dual Read-out DIMM
(SF-1)



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	41	$\overline{GW}$	81	Vss	121	CE2
2	DQ0	42	Vcc2	82	DQ1	122	RSVD
3	Vcc2	43	RSVD	83	RSVD	123	RSVD
4	DQ2	44	A13	84	DQ3	124	A14
5	DQ4	45	MODE	85	DQ5	125	$\overline{ADV}$
6	DQ6	46	A15	86	DQ7	126	A16
7	RSVD	47	A17	87	DQ8	127	NC
8	Vss	48	NC	88	Vss	128	NC
9	DQ9	49	DQ32	89	DQ10	129	DQ33
10	DQ11	50	NC	90	DQ12	130	NC
11	DQ13	51	Vss	91	DQ14	131	Vss
12	Vcc2	52	DQ34	92	RSVD	132	DQ35
13	DQ15	53	DQ36	93	RSVD	133	DQ37
14	DQ16	54	DQ38	94	Vss	134	DQ39
15	Vss	55	DQ40	95	DQ17	135	RSVD
16	DQ18	56	$\overline{BW4}$	96	DQ19	136	$\overline{BW5}$
17	DQ20	57	Vss	97	DQ21	137	Vss
18	$\overline{OE}$	58	$\overline{BW6}$	98	DQ22	138	$\overline{BW7}$
19	Vss	59	DQ41	99	Vss	139	DQ42
20	$\overline{BW0}$	60	DQ43	100	$\overline{BW1}$	140	DQ44
21	DQ23	61	DQ45	101	RSVD	141	DQ46
22	DQ24	62	Vcc2	102	DQ25	142	RSVD
23	Vcc2	63	DQ47	103	RSVD	143	DQ48
24	DQ26	64	RSVD	104	DQ27	144	DQ49
25	DQ28	65	DQ50	105	DQ29	145	DQ51
26	DQ30	66	DQ52	106	DQ31	146	DQ53
27	RSVD	67	DQ54	107	A6	147	DQ55
28	A5	68	Vss	108	A8	148	Vss
29	A7	69	PRD0	109	A10	149	PRD1
30	A9	70	Vcc2	110	A12	150	RSVD
31	$\overline{BW2}$	71	DQ56	111	$\overline{BW3}$	151	RSVD
32	Vss	72	DQ57	112	Vss	152	DQ58
33	$\overline{BWE}$	73	Vss	113	CLK	153	Vss
34	A11	74	DQ59	114	A3	154	DQ60
35	A4	75	DQ61	115	$\overline{CE2}$	155	DQ62
36	RSVD	76	DQ63	116	RSVD	156	RSVD
37	$\overline{ADSC}$	77	PRD2	117	$\overline{ADSP}$	157	PRD3
38	RSVD	78	Vcc2	118	RSVD	158	RSVD
39	$\overline{CE}$	79	NC	119	RSVD	15	NC
40	Vss	80	Vss	120	Vss	160	Vss

GENERAL DESCRIPTION (continued)

from one to eight bytes wide as controlled by the byte write enables.

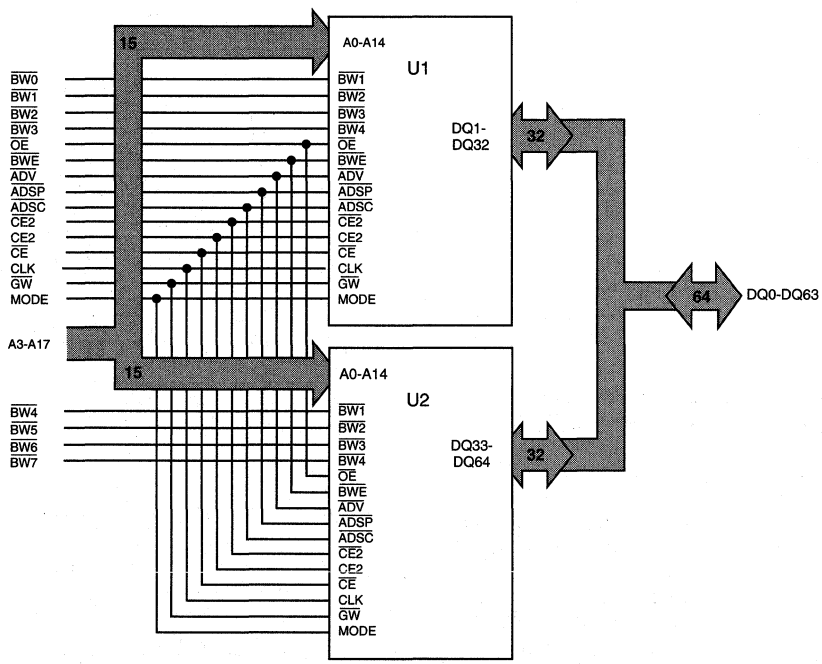
Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW0}$ controls DQ0-DQ7, $\overline{BW1}$ controls DQ8-DQ15, $\overline{BW2}$ controls DQ16-DQ23, $\overline{BW3}$ controls DQ24-DQ31 and so forth, conditioned by $\overline{BWE}$ being LOW. $\overline{GW}$ LOW causes all bytes to be written. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE as controlled solely by $\overline{OE}$ to improve cache system response. The module incorporates an additional pipelined enable register to allow depth expansion without penalizing system performance.

The "L" version of this module has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The module operates from a +3.3V power supply and all inputs and outputs are TTL compatible and 5V tolerant. This module is ideally suited to Pentium™ and Power PC™ systems and systems that benefit from a very wide data bus. The module is also ideal in generic 32- and 64-bit-wide applications. For additional functional and timing information consult the MT58LC32K32C4 synchronous SRAM data sheet.

FUNCTIONAL BLOCK DIAGRAM
256KB
(32K x 64)



U1-U2 = MT58LC32K32C4LG

NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See MT58LC32K32C4 synchronous SRAM data sheet for more detailed functional information.

PIN DESCRIPTIONS

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
28-30, 34-35, 44, 46-47, 107-110, 114, 124, 126	A3-A17	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
20, 31, 56, 58, 100, 111, 136, 138	$\overline{BW0}$-7	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when $\overline{BWE}$ is LOW and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle.$\overline{BW0}$ controls DQ0-DQ7. $\overline{BW1}$ controls DQ8-DQ15. $\overline{BW2}$ controls DQ16-DQ23. $\overline{BW3}$ controls DQ24-DQ31, and so forth. Data I/O are tristated if any of these eight inputs are LOW.
113	CLK	Input	Clock: This signal latches the address, data, chip enables, bytewrite enables and burst control inputs on its rising edge. Allsynchronous inputs must meet setup and hold times around the clock's rising edge.
39	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
121	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
115	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
18	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
125	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
117	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW inputinterrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$, but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.
37	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external addressto be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

PIN DESCRIPTIONS (continued)

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
7, 27, 36, 38, 43, 64, 83, 92, 93, 101, 103, 116, 118, 119, 122, 123, 135, 142, 150, 151, 156, 158	RSVD	-	No Connect: These pins are reserved.
33	$\overline{BWE}$	Input	Byte Write Enable: This active low input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
41	$\overline{GW}$	Input	Global Write: This active low input allows a full 32-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BW}$n lines and must meet the setup and hold times around the rising edge of CLK.
45	MODE	Input	Mode: This input selects the burst sequence. A low on this pin selects LINEAR BURST. A NC on this pin selects INTER-LEAVED BURST. Do not alter input state while device is operating.
2, 4-6, 9-11, 13-14, 16-17, 21-22, 24-26, 49, 52-55, 59-61, 63, 65-67, 71-72, 74-76, 82, 84-87, 89-91, 95-98, 102, 104-106, 129, 132-134, 139-141, 143-147, 152, 154-155	DQ0-DQ63	Input/ Output	SRAM Data I/O: Byte 1 is DQ0-DQ7; Byte 2 is DQ8-DQ15; Byte 3 is DQ16-DQ23; Byte 4 is DQ24-DQ31 and so forth. Input data must meet setup and hold times around the rising edge of CLK.
3, 12, 23, 42, 62, 70, 78	Vcc2	Supply	Power Supply: +3.3V ±5%
1, 8, 15, 19, 32, 40, 51, 57, 68, 73, 80, 81, 88, 94, 99, 112, 120, 131, 137, 148, 153, 160	Vss	Supply	Ground: GND

PRESENCE-DETECT TABLE

Description	Size	PRD3	PRD2	PRD1	PRD0
None		NC	NC	NC	NC
Synchronous Pipelined	256KB	NC	Vss	NC	NC
Synchronous Pipelined	512KB	NC	Vss	NC	Vss
Synchronous	256KB	NC	Vss	Vss	NC
Synchronous	512KB	NC	Vss	Vss	Vss
Asynchronous	256KB	NC	NC	NC	Vss
Asynchronous	512KB	NC	NC	Vss	NC
Reserved		NC	NC	Vss	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +125°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	$\overline{BW0}$-7	I_{LI1}	-1	1	µA	7
		A3-A17	I_{LI2}	-4	4	µA	7
		All other inputs	I_{LI3}	-2	2	µA	7
Output Leakage Current	Output(s) Disabled, 0V ≤ V_{OUT} ≤ V_{CC}		I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			V_{CC}	3.1	3.5	V	1

DESCRIPTION	CONDITIONS	SYM	VER	TYP	MAX -5	MAX -6	MAX -7	MAX -8	UNITS	NOTES
Power Supply Current: Operating	Device selected; Vcc = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; outputs open	I_{CC1}	ALL	360	720	630	540	450	mA	3, 5, 6
Power Supply Current: Idle	Device selected; Vcc = MAX; $\overline{GW}$, $\overline{BW}$, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; cycle time ≥ ^tKC MIN	I_{CC2}	ALL	60	120	110	100	90	mA	5, 6
CMOS Standby	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; all inputs static; CLK frequency = 0	I_{SB1}	STD	1.0	10	10	10	10	mA	5, 6
			P	0.4	4	4	4	4	mA	
TTL Standby	Device deselected; Vcc = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB2}	STD	30	50	50	50	50	mA	5, 6
			P	16	36	36	36	36	mA	
Clock Running	Device deselected; Vcc = MAX; all inputs ≤ Vss +0.2 or ≥ Vcc -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB3}	ALL	60	120	110	100	90	mA	5, 6

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A3-A17, $\overline{ADSC}$, $\overline{GW}$, MODE	T_A = 25°C; f = 1 MHz	C_{I1}		10	pF	4
Input Capacitance: $\overline{ADSP}$, $\overline{ADV}$, CLK,$\overline{OE}$, $\overline{CE}$, $\overline{BWE}$	V_{CC} = 3.3V	C_{I2}		10	pF	4
Input Capacitance: $\overline{BW0}$-7		C_{I3}		5	pF	4
Input/Output Capacitance: DQ0-63		C_O		8	pF	4

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2}$ ≥ (V_{CC} -0.2V), CE2 ≤ 0.2V V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V V_{CC} = 2V	I_{CCDR}		TBD	µA	8
Chip Deselect to Data Retention Time		^tCDR	^tKC		ns	4, 9
Operation Recovery Time		^tR	^tKC		ns	4

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: V_{IH} ≤ +6.0V for t ≤ ^tKC /2.
   Undershoot: V_{IL} ≥ -2.0V for t ≤ ^tKC /2.
   Power-up: V_{IH} ≤ +6.0V and V_{CC} ≤ 3.1V for t ≤ 200ms
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. "Device deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device selected" means device is active (not in POWER-DOWN mode).
6. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
7. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
8. Typical values are measured at 25°C.
9. The device must have a deselect cycle applied at least one clock cycle before data retention mode is entered.

MICRON SEMICONDUCTOR, INC.

MT2LSYT3272T1/T2, MT4LSY6472T1/T2
32K, 64K x 72 SYNCHRONOUS SRAM MODULE

SYNCHRONOUS SRAM MODULE

32K, 64K x 72 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS AND BURST COUNTER

FEATURES

- 80 position dual read-out dual in-line memory module (DIMM) with 160 leads
- Fast access times: 9, 10, 11 and 12ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant common data I/O
- Individual BYTE WRITE control
- Clock controlled, registered address, data and control
- Internally self-timed WRITE cycle
- Burst control pins (interleaved T2 or linear burst T1)
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS — MARKING

- Timing
  - 9ns access/15ns cycle — -9
  - 10ns access/15ns cycle — -10
  - 11ns access/15ns cycle — -11
  - 12ns access/20ns cycle — -12
- Burst sequence
  - Linear Burst — T1
  - 486/Pentium™ Burst — T2
- Packages
  - 160-lead DIMM (gold) — G
- Low power (optional) — P
- 2V data retention, low power (optional) — L
- Part Number Examples: MT2LSYT3272T2G-10 L
  MT4LSY6472T2G-10 L

GENERAL DESCRIPTION

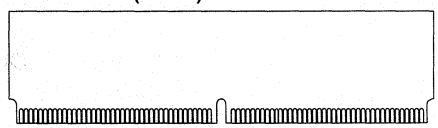
The Micron SyncBurst™ SRAM module family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT2LSYT3272T1/T2 module integrates two 32K x 36 synchronous SRAMs and the MT4LSY6472T1/T2 integrates four 64K x 18 synchronous SRAMs. All synchronous inputs pass through registers controlled by positive-edge-triggered clock inputs (CLK0 and CLK1*). The synchronous inputs include all addresses, data inputs, active LOW chip enables ($\overline{CE0}$-1), burst control inputs ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1, $\overline{ADV0}$-1) and byte write enables ($\overline{BW0}$-7).

PIN ASSIGNMENT (Top View)

160-Lead, Dual Read-out DIMM

(SF-1) 32K x 72
(SF-3) 64K x 72



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	41	Vss	81	Vss	121	Vss
2	DQ62	42	DQ10	82	DQ63	122	DQ11
3	Vcc	43	Vcc	83	RSVD	123	RSVD
4	DQ60	44	DQ8	84	DQ61	124	DQ9
5	Vcc	45	DQP0	85	RSVD	125	DQP1
6	DQ58	46	Vcc	86	DQ59	126	RSVD
7	DQ56	47	DQ6	87	DQ57	127	DQ7
8	Vss	48	DQ4	88	Vss	128	DQ5
9	DQP6	49	DQ2	89	DQP7	129	DQ3
10	DQ54	50	DQ0	90	DQ55	130	DQ1
11	DQ52	51	Vss	91	DQ53	131	Vss
12	DQ50	52	A0A	92	DQ51	132	A0B
13	Vss	53	A1A	93	Vss	133	A1B
14	DQ48	54	A2A	94	DQ49	134	A2B
15	DQ46	55	A3A	95	DQ47	135	A3B
16	DQ44	56	A5	96	DQ45	136	A4
17	DQ42	57	Vss	97	DQ43	137	Vss
18	Vss	58	A7	98	Vss	138	A6
19	DQ40	59	A9	99	DQ41	139	A8
20	DQP4	60	A11	100	DQP5	140	A10
21	DQ38	61	A13	101	DQ39	141	A12
22	DQ36	62	A15*	102	DQ37	142	A14
23	DQ34	63	Vss	103	DQ35	143	Vss
24	Vss	64	PD0	104	Vss	144	NC
25	DQ32	65	Vss	105	DQ33	145	Vss
26	DQ30	66	NC/CLK1*	106	DQ31	146	CLK0
27	DQ28	67	RSVD	107	DQ29	147	RSVD
28	DQ26	68	Vss	108	DQ27	148	Vss
29	DQ24	69	$\overline{BW6}$	109	DQ25	149	$\overline{BW7}$
30	Vss	70	$\overline{BW4}$	110	Vss	150	$\overline{BW5}$
31	DQP2	71	$\overline{BW2}$	111	DQP3	151	$\overline{BW3}$
32	DQ22	72	$\overline{BW0}$	112	DQ23	152	$\overline{BW1}$
33	DQ20	73	Vss	113	DQ21	153	Vss
34	Vcc	74	$\overline{ADSC0}$	114	RSVD	154	$\overline{ADSC1}$
35	DQ18	75	$\overline{CE0}$	115	DQ19	155	$\overline{CE1}$
36	Vss	76	$\overline{ADV0}$	116	Vss	156	$\overline{ADV1}$
37	DQ16	77	$\overline{OE0}$	117	DQ17	157	$\overline{OE1}$
38	Vcc	78	Vcc	118	RSVD	158	RSVD
39	DQ14	79	$\overline{ADSP0}$	119	DQ15	159	$\overline{ADSP1}$
40	DQ12	80	Vss	120	DQ13	160	Vss

*64K x 72 version only

GENERAL DESCRIPTION (continued)

Asynchronous inputs include the output enable ($\overline{OE}$) and the clocks (CLK0 and CLK1*). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to eight bytes wide as controlled by the byte write enables.

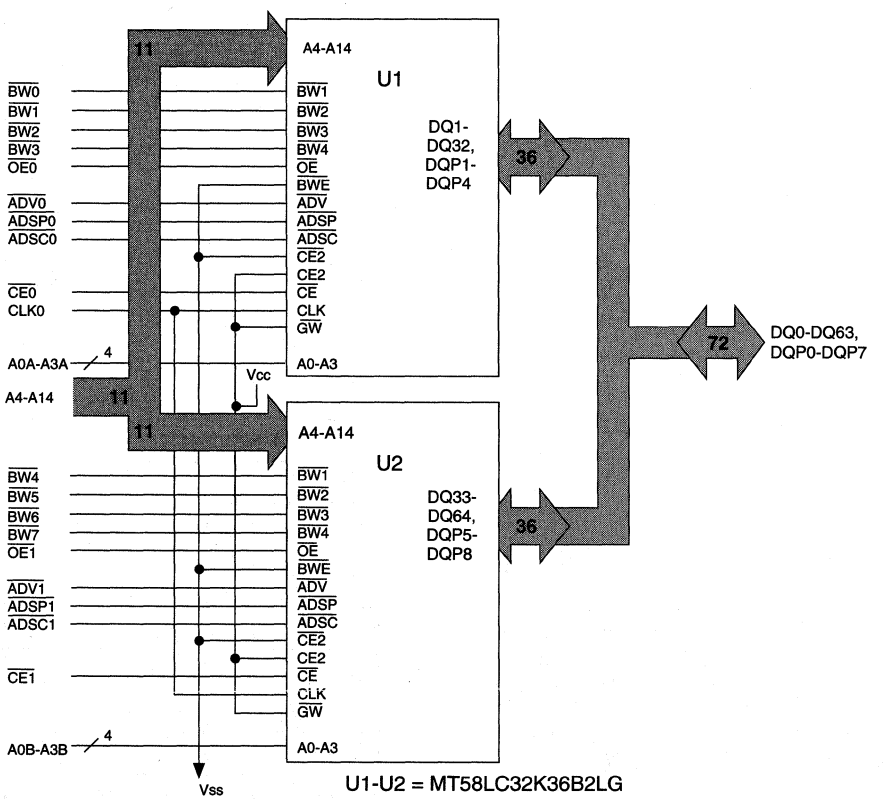
Burst operation can be initiated with either address status processor ($\overline{ADSP0}$-1) or address status controller ($\overline{ADSC0}$-1) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pins ($\overline{ADV0}$-1).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW0}$ controls DQ0-DQ7 and DQP0, $\overline{BW1}$ controls DQ8-DQ15 and DQP1, $\overline{BW2}$ controls DQ16-DQ23 and DQP2, $\overline{BW3}$ controls DQ24-DQ31 and DQP4 and so forth.

The "L" version of this module has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

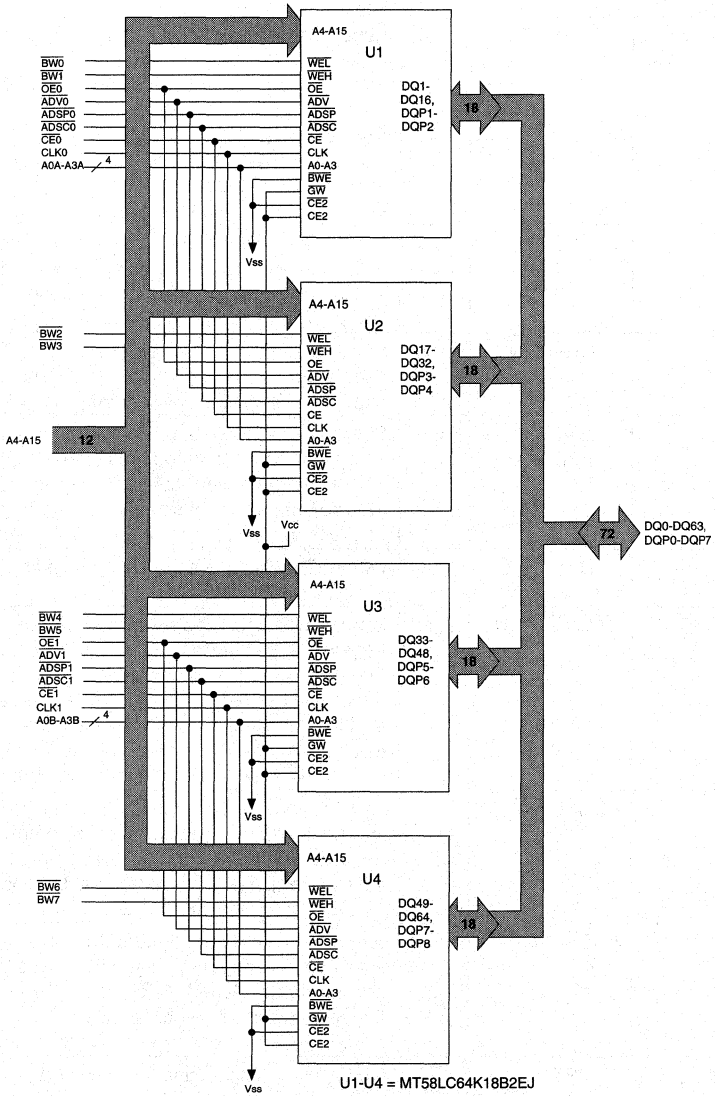
The module operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V-tolerant. This module is ideally suited to Pentium™ systems and those systems which benefit from a very wide data bus.

FUNCTIONAL BLOCK DIAGRAM
256KB
(32K x 72)



NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

FUNCTIONAL BLOCK DIAGRAM
512KB
(64K x 72)



NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
56, 58-62, 136, 138-142	A4-A15	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
69-72, 149-152	$\overline{BW0}$-7	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW0}$ controls DQ0-DQ7 and DQP0. $\overline{BW1}$ controls DQ8-DQ15 and DQP1. $\overline{BW2}$ controls DQ16-DQ23 and DQP2. $\overline{BW3}$ controls DQ24-DQ31 and DQP3, and so forth. Data I/O are tristated if any of these eight inputs are LOW.
66, 146	CLK0-CLK1	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge. (CLK1 used on 64K x 72 only).
75, 155	$\overline{CE0}$-$\overline{CE1}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
52-55, 132-135	A0A-A3A, A0B-A3B	Input	Synchronous Address Input: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. These lower order address signals are provided for the two data banks to simplify the interface to many cache controllers.
77, 157	$\overline{OE0}$-$\overline{OE1}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
76, 156	$\overline{ADV0}$-$\overline{ADV1}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
79, 159	$\overline{ADSP0}$-$\overline{ADSP1}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH.
74, 154	$\overline{ADSC0}$-$\overline{ADSC1}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
83, 85, 114, 118, 123, 126, 147, 158	RSVD	-	No Connect: These pins are reserved.

PIN DESCRIPTIONS (continued)

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
2, 4, 6-7, 10-12, 14, 16-17, 19, 21-23, 25-29, 32-33, 35, 37, 39-40, 42, 44, 47-50, 82, 84, 86-87, 90-92, 94-97, 99, 101-103, 105-109, 112-113, 115, 117, 119-120, 122, 124, 127-130	DQ0-DQ63	Input/ Output	SRAM Data I/O: Byte 1 is DQ0-DQ7; Byte 2 is DQ8-DQ15; Byte 3 is DQ16-DQ23; Byte 4 is DQ24-DQ31 and so forth. Input data must meet setup and hold times around the rising edge of CLK.
9, 20, 31, 45, 89, 100, 111, 125	DQP0-DQP7	Input/ Output	Parity Data I/O: Byte 1 Parity is DQP0; Byte 2 Parity is DQP1 and so forth.
3, 5, 34, 38, 43, 46, 78	Vcc	Supply	Power Supply: +3.3V ±5%
1, 8, 13, 18, 24, 30, 36, 41, 51, 57, 63, 68, 73, 80, 81, 88, 93, 98, 104, 110, 116, 121, 131, 137, 143, 148, 153, 160	Vss	Supply	Ground: GND

INTERLEAVED BURST ADDRESS TABLE (MODE = NC) MT2LSYT3272T2, MT4LSY6472T2

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = GND) MT2LSYT3272T1, MT4LSY6472T1

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PRESENCE-DETECT TABLE

DENSITY	PD0
256KB	NC
512KB	Vss

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ0-63, DQP0-7
Deselected Cycle, Power-down	None	H	X	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW0}$, $\overline{BW1}$, $\overline{BW2}$, etc.) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW0}$ enables writes to Byte 1 (DQ0-DQ7, DQP0). $\overline{BW1}$ enables writes to Byte 2 (DQ8-DQ15, DQP1). $\overline{BW2}$ enables writes to Byte 3 (DQ16-DQ23, DQP2). $\overline{BW3}$ enables writes to Byte 4 (DQ24-DQ31, DQP3) and so forth.
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +125°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	$\overline{BW0}$-$\overline{BW7}$	I_{LI1}	-1	1	µA	
		A4-A15	I_{LI2}	-4	4	µA	
		All other inputs	I_{LI3}	-2	2	µA	
Output Leakage Current	Output(s) Disabled, 0V ≤ V_{OUT} ≤ V_{CC}		I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			V_{CC}	3.1	3.5	V	1

DESCRIPTION	CONDITIONS	SYM	VER	SIZE	TYP	MAX -9	MAX -10	MAX -11	MAX -12	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; V_{CC} = MAX; outputs open	I_{CC1}	ALL	256KB	400	600	600	550	500	mA	3, 12,
				512KB	700	1,000	1,000	900	800	mA	13
Power Supply Current: Idle	Device selected; V_{CC} = MAX; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; cycle time ≥ ^tKC MIN	I_{CC2}	ALL	256KB	56	90	90	90	80	mA	12, 13
				512KB	112	180	180	180	160	mA	
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB1}	STD	256KB	1.0	10	10	10	10	mA	12, 13
				512KB	2.0	20	20	20	20	mA	
			P	256KB	0.4	4	4	4	4	mA	
				512KB	0.8	8	8	8	8	mA	
TTL Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB2}	STD	256KB	30	50	50	50	50	mA	12, 13
				512KB	60	100	100	100	100	mA	
			P	256KB	16	36	36	36	36	mA	
				512KB	40	72	72	72	72	mA	
Clock Running	Device deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB3}	ALL	256KB	60	100	100	100	90	mA	12, 13
				512KB	120	200	200	200	180	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX 32K	MAX 64K	UNITS	NOTES
Input Capacitance: A4-A15	T_A = 25°C; f = 1 MHz	C_{I1}	10	18	pF	4
Input Capacitance: $\overline{ADSP0}$-1, $\overline{ADV0}$-1, CLK0-1, $\overline{OE0}$-1, $\overline{CE0}$-1, $\overline{ADSC0}$-1, A0A-A3A, A0B-A3B	Vcc = 3.3V	C_{I2}	5	10	pF	4
Input Capacitance: $\overline{BW0}$-7		C_{I3}	5	5	pF	4
Input/Output Capacitance: DQ0-63, PDQ0-7		C_O	8	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (Vcc = 3.3V ±5%)

DESCRIPTION	SYM	-9 MIN	-9 MAX	-10 MIN	-10 MAX	-11 MIN	-11 MAX	-12 MIN	-12 MAX	UNITS	NOTES
Clock											
Clock cycle time	^tKC	15		15		15		20		ns	
Clock HIGH time	^tKH	4		5		5		6		ns	
Clock LOW time	^tKL	4		5		5		6		ns	
Output Times											
Clock to output valid	^tKQ		9		10		11		12	ns	
Clock to output invalid	^tKQX	3		3		3		3		ns	
Clock to output in Low-Z	^tKQLZ	5		5		5		5		ns	6, 7
Clock to output in High-Z	^tKQHZ		5		5		5		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		5		5		5		6	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		5		5		5		6	ns	6, 7
Setup Times											
Address	^tAS	2.5		2.5		2.5		3		ns	8, 10
Address Status ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1)	^tADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{ADV0}$-1)	^tAAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{BW0}$-7)	^tWS	2.5		3		3		3		ns	8, 10
Data-in	^tDS	2.5		3		3		3		ns	8, 10
Chip Enable ($\overline{CE0}$-1)	^tCES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	^tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1)	^tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV0}$-1)	^tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{BW0}$-7)	^tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enable ($\overline{CE0}$-1)	^tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

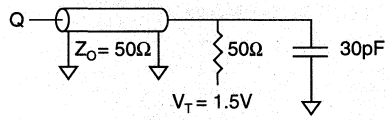


Fig. 1 OUTPUT LOAD EQUIVALENT

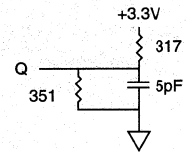


Fig. 2 OUTPUT LOAD EQUIVALENT

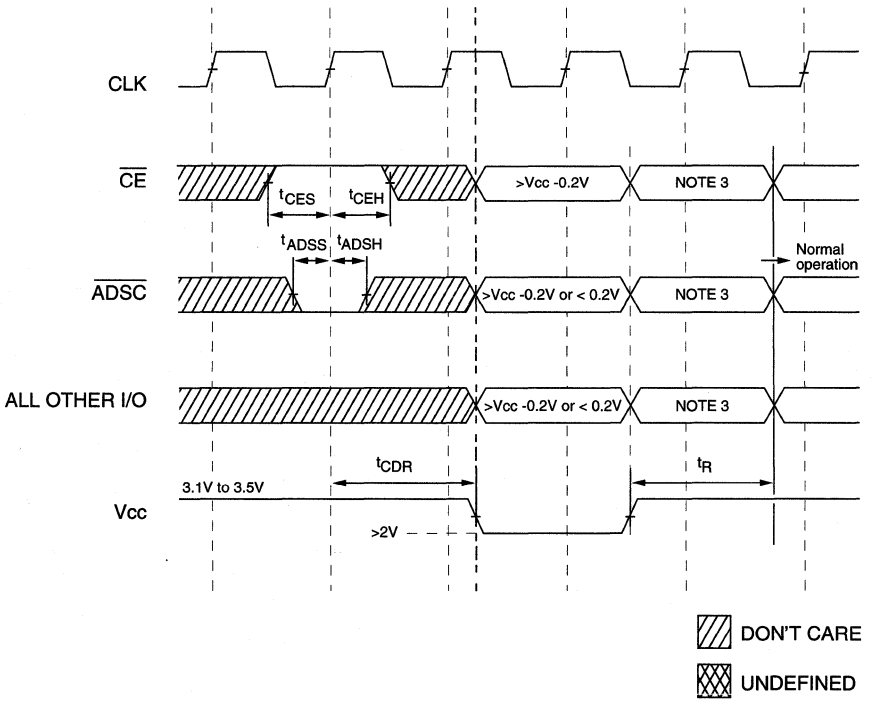
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the shown DC values.
12. "Device deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Typical values are measured at 25°C.
15. The device must have a deselect cycle applied at least one clock cycle before data retention mode is entered.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

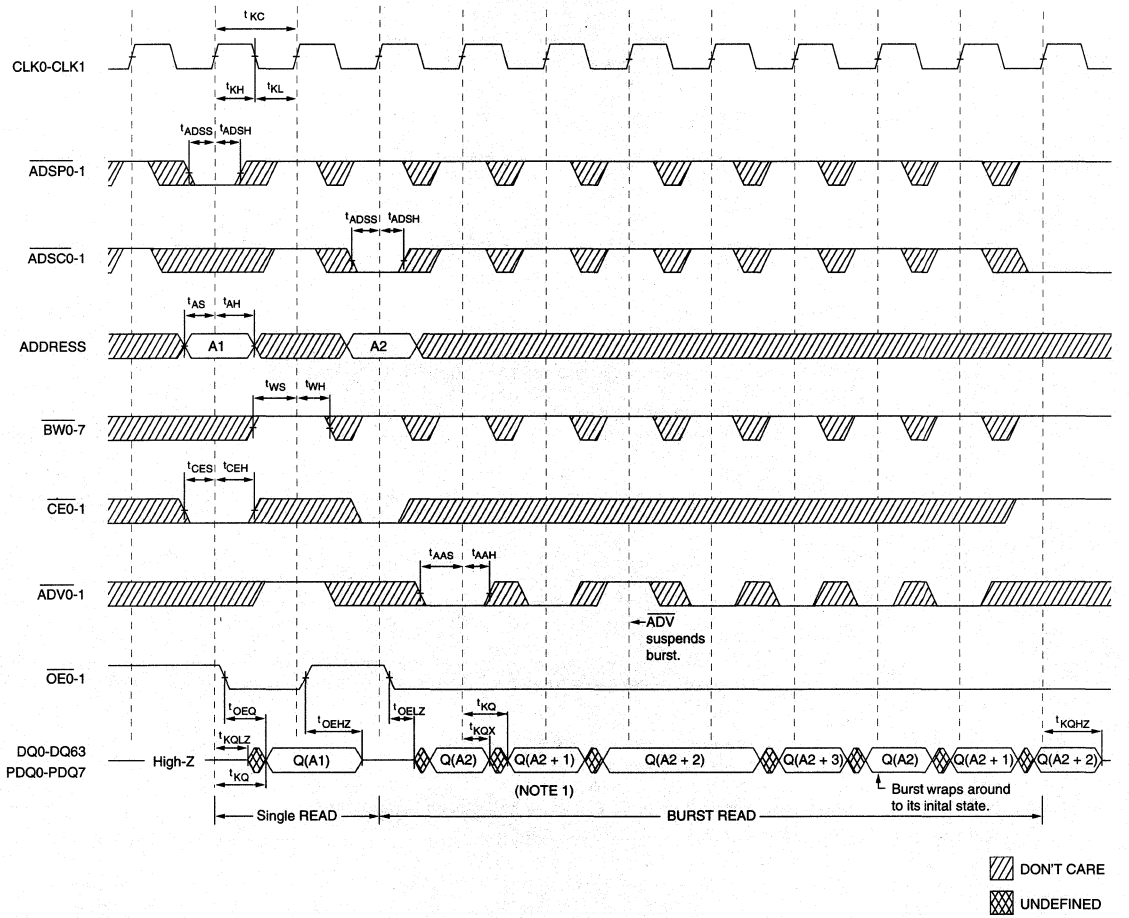
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2} \geq (V_{CC} - 0.2V)$, $CE2 \leq 0.2V$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$ $V_{CC} = 2V$	I_{CCDR}		TBD	µA	14
Chip Deselect to Data Retention Time		^tCDR	^tKC		ns	4, 15
Operation Recovery Time		^tR	^tKC		ns	4

LOW V_{CC} DATA RETENTION WAVEFORM



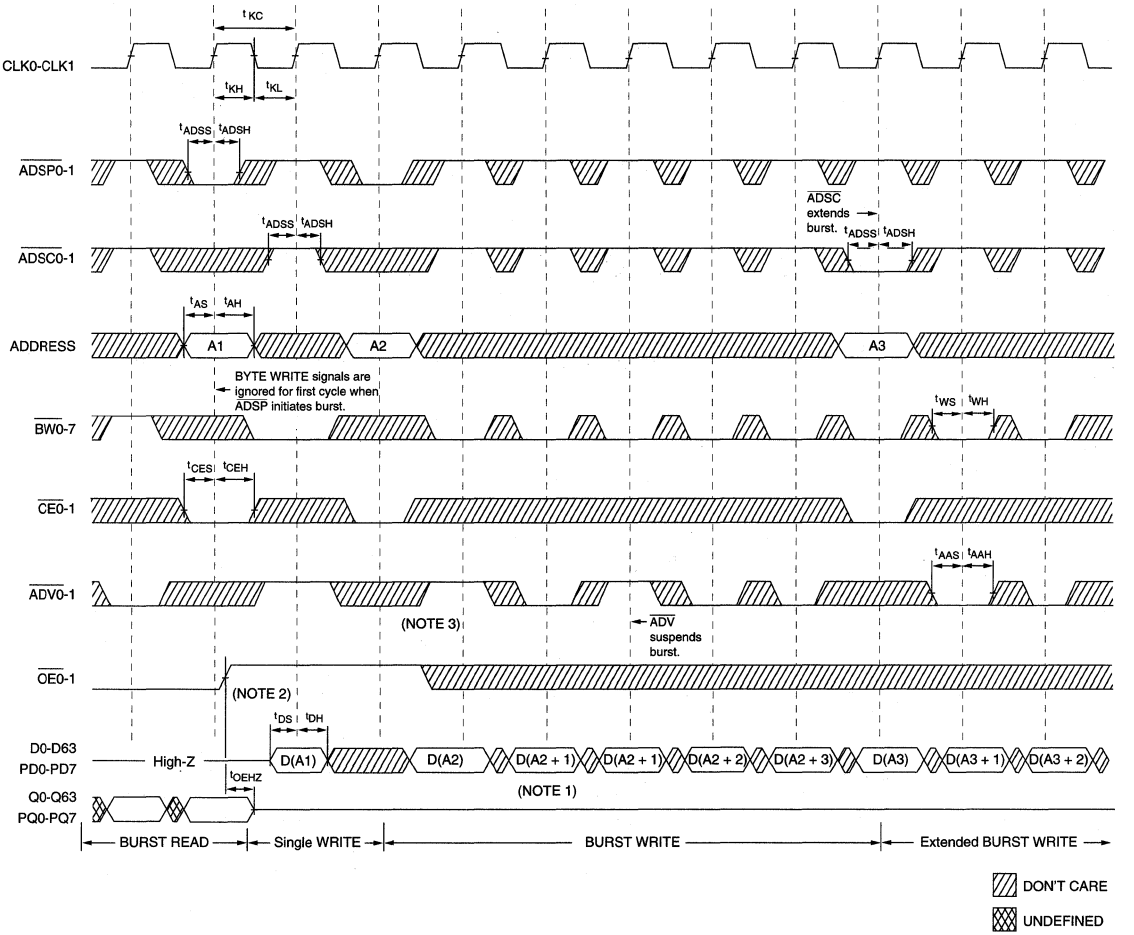
NOTE:
1. All inputs must be $\geq V_{CC}$ - 0.2V or $\leq$ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded.
2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.
3. The device control signals should be in a deselect state between the rising edge of Vcc and until ^tR is met.

READ TIMING



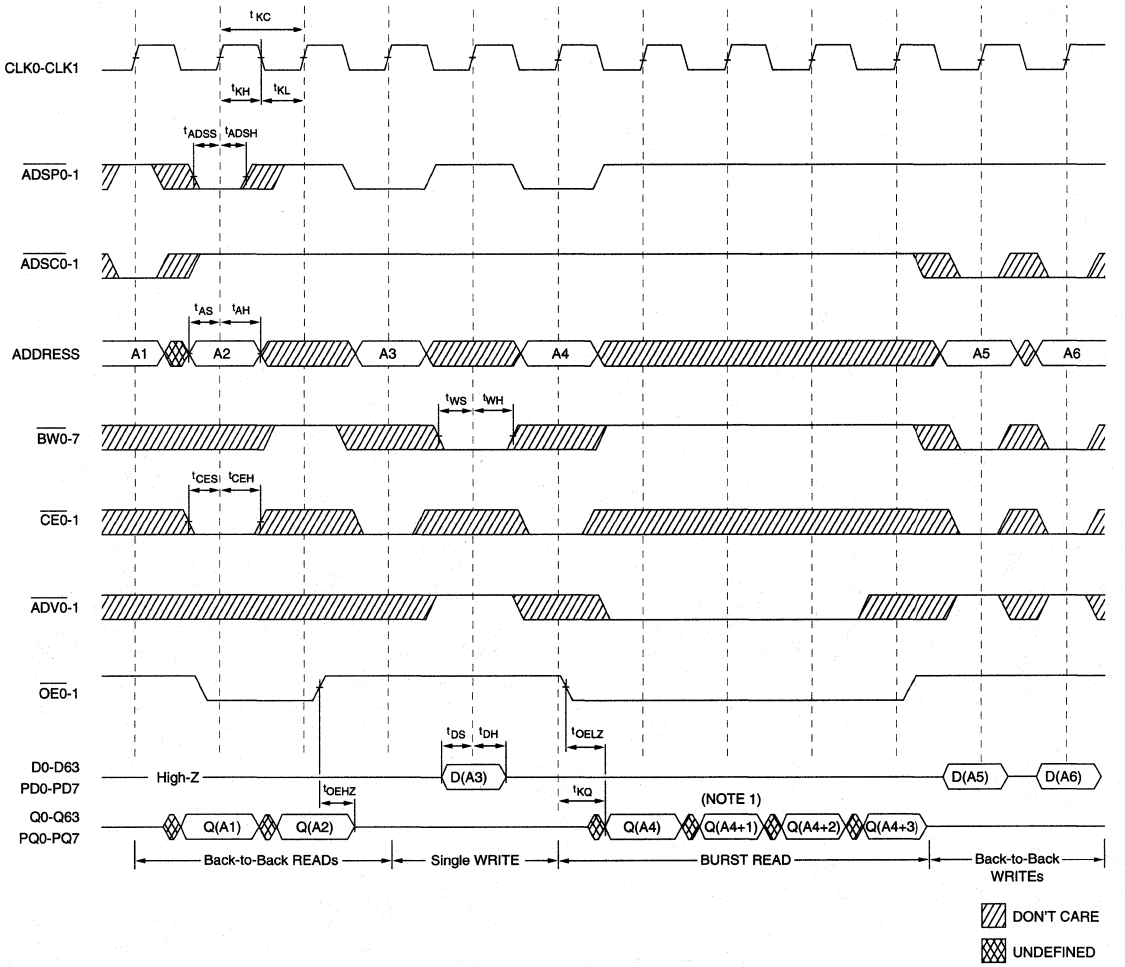
NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. Timing is shown assuming that the device was not enabled before entering this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

WRITE TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING



NOTE:
1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.
2. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$ or $\overline{\text{ADV}}$ cycle is performed.
3. Back-to-back READs may be controlled by either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$.

MICRON SEMICONDUCTOR, INC.

MT2LSYT3272T1/T2, MT4LSY6472T1/T2
32K, 64K x 72 SYNCHRONOUS SRAM MODULE

MICRON SEMICONDUCTOR, INC.

MT2LSYT3272T4/T6, MT4LSY6472T4/T6
32K, 64K x 72 SYNCHRONOUS SRAM MODULE

SYNCHRONOUS SRAM MODULE

32K, 64K x 72 SRAM

+3.3V SUPPLY, FULLY REGISTERED INPUTS, OUTPUTS AND BURST COUNTER

FEATURES

- 80 position dual read-out dual in-line memory module (DIMM) with 160 leads
- Fast access times: 5, 6, 7 and 8ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant common data I/O
- Individual BYTE WRITE control
- WRITE pass-through capability
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- Burst control pins (interleaved T4 or linear burst T6)
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS — MARKING

- Timing
  - 5ns access/10ns cycle — -5
  - 6ns access/12ns cycle — -6
  - 7ns access/15ns cycle — -7
  - 8ns access/20ns cycle — -8
- Burst sequence
  - Interleaved Burst — T4
  - Linear Burst — T6
- Packages
  - 160-lead DIMM (gold) — G
- Low power (optional) — P
- 2V data retention, low power (optional) — L
- Part Number Examples: MT2LSYT3272T4G-6 L
  MT4LSY6472T4G-6 L

GENERAL DESCRIPTION

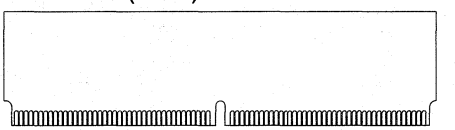
The Micron SyncBurst™ SRAM module family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT2LSYT3272T4/T6 module integrates two 32K x 36 synchronous SRAMs and the MT4LSY6472T4/T6 integrates four 64K x 18 synchronous SRAMs. All synchronous inputs pass through registers controlled by positive-edge-triggered clock inputs (CLK0 and CLK1*). The synchronous inputs include all addresses, data inputs, active LOW chip enables ($\overline{CE0}$-1), burst control inputs ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1, $\overline{ADV0}$-1) and byte write enables ($\overline{BW0}$-7).

PIN ASSIGNMENT (Top View)

160-Lead, Dual Read-out DIMM

(SF-1) 32K x 72
(SF-3) 64K x 72



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	41	Vss	81	Vss	121	Vss
2	DQ62	42	DQ10	82	DQ63	122	DQ11
3	Vcc	43	Vcc	83	RSVD	123	RSVD
4	DQ60	44	DQ8	84	DQ61	124	DQ9
5	Vcc	45	DQP0	85	RSVD	125	DQP1
6	DQ58	46	Vcc	86	DQ59	126	RSVD
7	DQ56	47	DQ6	87	DQ57	127	DQ7
8	Vss	48	DQ4	88	Vss	128	DQ5
9	DQP6	49	DQ2	89	DQP7	129	DQ3
10	DQ54	50	DQ0	90	DQ55	130	DQ1
11	DQ52	51	Vss	91	DQ53	131	Vss
12	DQ50	52	A0A	92	DQ51	132	A0B
13	Vss	53	A1A	93	Vss	133	A1B
14	DQ48	54	A2A	94	DQ49	134	A2B
15	DQ46	55	A3A	95	DQ47	135	A3B
16	DQ44	56	A5	96	DQ45	136	A4
17	DQ42	57	Vss	97	DQ43	137	Vss
18	Vss	58	A7	98	Vss	138	A6
19	DQ40	59	A9	99	DQ41	139	A8
20	DQP4	60	A11	100	DQP5	140	A10
21	DQ38	61	A13	101	DQ39	141	A12
22	DQ36	62	A15*	102	DQ37	142	A14
23	DQ34	63	Vss	103	DQ35	143	Vss
24	Vss	64	PD0	104	Vss	144	NC
25	DQ32	65	Vss	105	DQ33	145	Vss
26	DQ30	66	NC/CLK1*	106	DQ31	146	CLK0
27	DQ28	67	RSVD	107	DQ29	147	RSVD
28	DQ26	68	Vss	108	DQ27	148	Vss
29	DQ24	69	$\overline{BW6}$	109	DQ25	149	$\overline{BW7}$
30	Vss	70	$\overline{BW4}$	110	Vss	150	$\overline{BW5}$
31	DQP2	71	$\overline{BW2}$	111	DQP3	151	$\overline{BW3}$
32	DQ22	72	$\overline{BW0}$	112	DQ23	152	$\overline{BW1}$
33	DQ20	73	Vss	113	DQ21	153	Vss
34	Vcc	74	$\overline{ADSC0}$	114	RSVD	154	$\overline{ADSC1}$
35	DQ18	75	$\overline{CE0}$	115	DQ19	155	$\overline{CE1}$
36	Vss	76	$\overline{ADV0}$	116	Vss	156	$\overline{ADV1}$
37	DQ16	77	$\overline{OE0}$	117	DQ17	157	$\overline{OE1}$
38	Vcc	78	Vcc	118	RSVD	158	RSVD
39	DQ14	79	$\overline{ADSP0}$	119	DQ15	159	$\overline{ADSP1}$
40	DQ12	80	Vss	120	DQ13	160	Vss

*64K x 72 version only

GENERAL DESCRIPTION (continued)

Asynchronous inputs include the output enables ($\overline{OE0}$-1) and the clocks (CLK0 and CLK1*). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to eight bytes wide as controlled by the byte write enables.

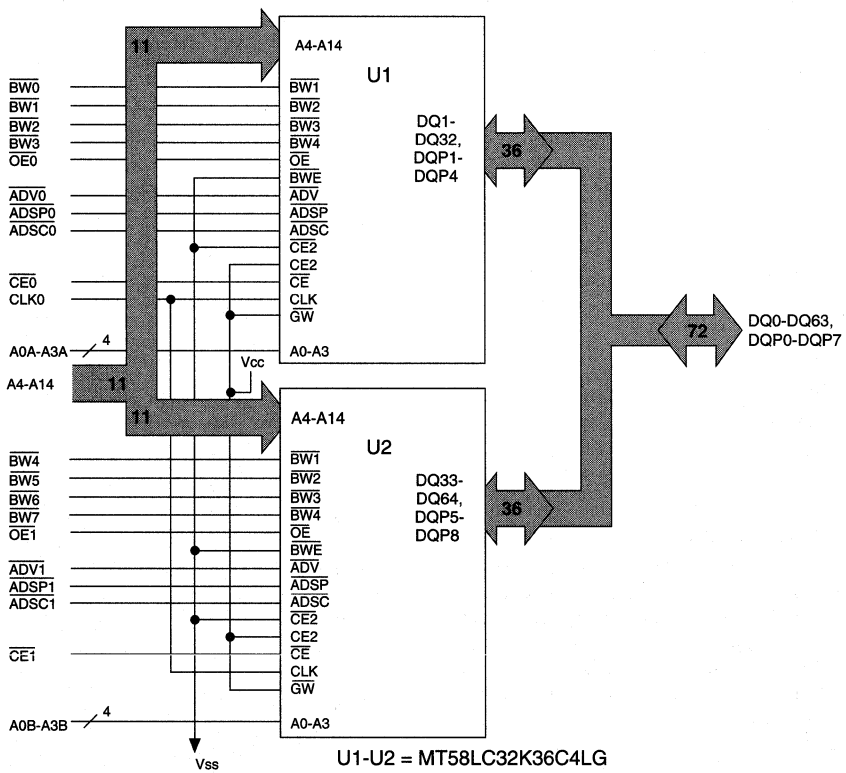
Burst operation can be initiated with either address status processor ($\overline{ADSP0}$-1) or address status controller ($\overline{ADSC0}$-1) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pins ($\overline{ADV0}$-1).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW0}$ controls DQ0-DQ7 and DQP0, $\overline{BW1}$ controls DQ8-DQ15 and DQP1, $\overline{BW2}$ controls DQ16-DQ23 and DQP2, $\overline{BW3}$ controls DQ24-DQ31 and DQP4 and so forth.

The "L" version of this module has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

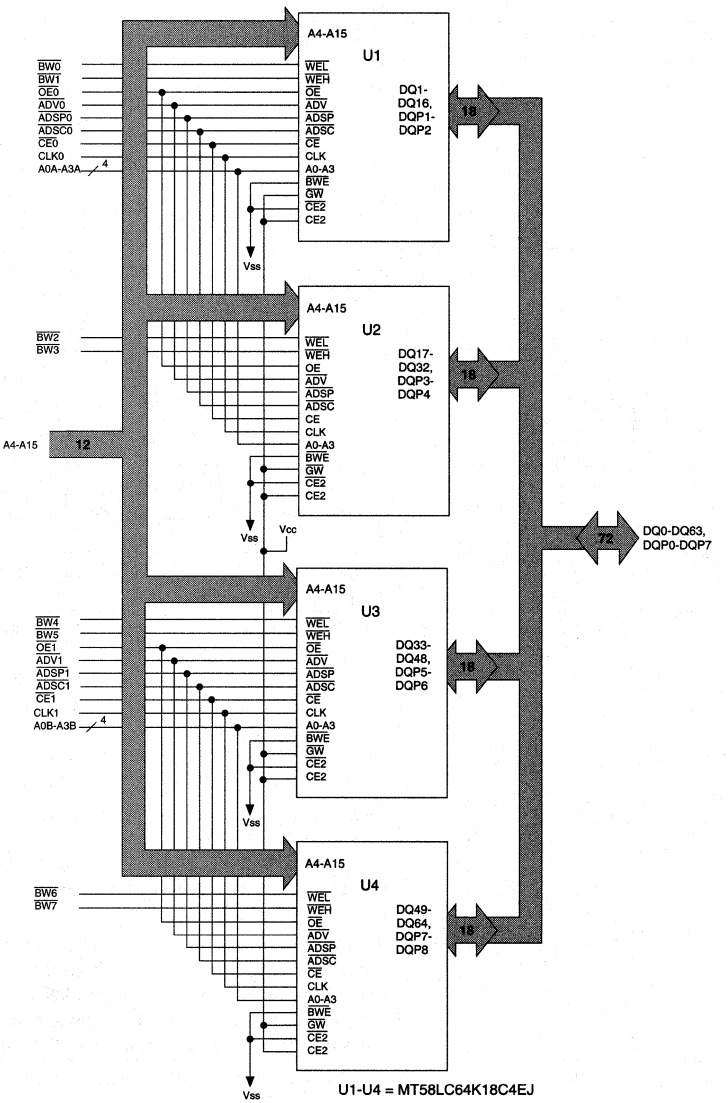
The module operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. This module is ideally suited to Pentium™ and PowerPC™ pipelined systems and systems that benefit from a very wide high-speed data bus.

FUNCTIONAL BLOCK DIAGRAM
256KB
(32K x 72)



NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

FUNCTIONAL BLOCK DIAGRAM
512KB
(64K x 72)



NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
56, 58-62, 136, 138-142	A4-A15	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
69-72, 149-152	$\overline{BW0}$-7	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW0}$ controls DQ0-DQ7 and DQP0. $\overline{BW1}$ controls DQ8-DQ15 and DQP1. $\overline{BW2}$ controls DQ16-DQ23 and DQP2. $\overline{BW3}$ controls DQ24-DQ31 and DQP3, and so forth. Data I/O are tristated if any of these eight inputs are LOW.
66, 146	CLK0-CLK1	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge. (CLK1 used on 64K x 72 only).
75, 155	$\overline{CE0}$-$\overline{CE1}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
52-55, 132-135	A0A-A3A, A0B-A3B	Input	Synchronous Address Input: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. These lower order address signals are provided for the two data banks to simplify the interface to many cache controllers.
77, 157	$\overline{OE0}$-$\overline{OE1}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
76, 156	$\overline{ADV0}$-$\overline{ADV1}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
79, 159	$\overline{ADSP0}$-$\overline{ADSP1}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH.
74, 154	$\overline{ADSC0}$-$\overline{ADSC1}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
83, 85, 114, 118, 123, 126, 147, 158	RSVD	-	No Connect: These pins are reserved.

PIN DESCRIPTIONS (continued)

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
2, 4, 6-7, 10-12, 14, 16-17, 19, 21-23, 25-29, 32-33, 35, 37, 39-40, 42, 44, 47-50, 82, 84, 86-87, 90-92, 94-97, 99, 101-103, 105-109, 112-113, 115, 117, 119-120, 122, 124, 127-130	DQ0-DQ63	Input/ Output	SRAM Data I/O: Byte 1 is DQ0-DQ7; Byte 2 is DQ8-DQ15; Byte 3 is DQ16-DQ23; Byte 4 is DQ24-DQ31 and so forth. Input data must meet setup and hold times around the rising edge of CLK.
9, 20, 31, 45, 89, 100, 111, 125	DQP0-DQP7	Input/ Output	Parity Data I/O: Byte 1 Parity is DQP0; Byte 2 Parity is DQP1 and so forth.
3, 5, 34, 38, 43, 46, 78	Vcc	Supply	Power Supply: +3.3V ±5%
1, 8, 13, 18, 24, 30, 36, 41, 51, 57, 63, 68, 73, 80, 81, 88, 93, 98, 104, 110, 116, 121, 131, 137, 143, 148, 153, 160	Vss	Supply	Ground: GND

INTERLEAVED BURST ADDRESS TABLE (MODE = NC) MT2LSYT3272T4, MT4LSY6472T4

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = GND) MT2LSYT3272T6, MT4LSY6472T6

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{BWs}$	OPERATION	$\overline{CE}$	$\overline{BWs}$	$\overline{OE}$	OPERATION
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L	Initiate READ cycle Register A(n), Q = D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L	No new cycle Q = D(n-1)	H	H	L	No carry-over from previous cycle
Initiate WRITE cycle, all bytes Address = A(n-1), data = D(n-1)	All L	No new cycle Q = HIGH-Z	H	H	H	No carry-over from previous cycle
Initiate WRITE cycle, one byte Address = A(n-1), data = D(n-1)	One L	No new cycle Q = D(n-1) for one byte	H	H	L	No carry-over from previous cycle

NOTE: Previous cycle may be either BURST or NONBURST cycle.

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ0-63, DQP0-7
Deselected Cycle, Power-down	None	H	X	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW0}$, $\overline{BW1}$, $\overline{BW2}$, etc.) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW0}$ enables writes to Byte 1 (DQ0-DQ7, DQP0). $\overline{BW1}$ enables writes to Byte 2 (DQ8-DQ15, DQP1). $\overline{BW2}$ enables writes to Byte 3 (DQ16-DQ23, DQP2). $\overline{BW3}$ enables writes to Byte 4 (DQ24-DQ31, DQP3) and so forth.
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

PRESENCE-DETECT TABLE

DENSITY	PD0
256KB	NC
512KB	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +125°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	$\overline{BW0}$-7	I_{LI1}	-1	1	µA	
		A4-A15	I_{LI2}	-4	4	µA	
		All other inputs	I_{LI3}	-2	2	µA	
Output Leakage Current	Output(s) Disabled, 0V ≤ V_{OUT} ≤ V_{CC}		I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1, 11
Supply Voltage			V_{CC}	3.1	3.5	V	1

DESCRIPTION	CONDITIONS	SYM	VER	SIZE	TYP	MAX -5	MAX -6	MAX -7	MAX -8	UNITS	NOTES
Power Supply Current: Operating	Device selected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; outputs open	I_{CC1}	ALL	256KB	400	800	700	600	500	mA	3, 12, 13
				512KB	720	1,340	1,200	1,000	840	mA	
Power Supply Current: Idle	Device selected; V_{CC} = MAX; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; cycle time ≥ ^tKC MIN	I_{CC2}	ALL	256KB	60	120	110	100	90	mA	12, 13
				512KB	120	240	220	200	180	mA	
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB1}	STD	256KB	1.0	10	10	10	10	mA	12, 13
				512KB	2.0	20	20	20	20		
			P	256KB	0.4	4	4	4	4	mA	
				512KB	0.8	8	8	8	8		
TTL Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB2}	STD	256KB	30	50	50	50	50	mA	12, 13
				512KB	60	100	100	100	100		
			P	256KB	16	36	36	36	36	mA	
				512KB	32	72	72	72	72		
Clock Running	Device deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB3}	ALL	256KB	60	120	110	100	90	mA	12, 13
				512KB	120	240	220	200	180	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX 256KB	MAX 512KB	UNITS	NOTES
Input Capacitance: A4-A15	T_A = 25°C; f = 1 MHz	C_{I1}	10	18	pF	4
Input Capacitance: $\overline{ADSP0}$-1, $\overline{ADV0}$-1, CLK0-1, $\overline{OE0}$-1, $\overline{CE0}$-1, $\overline{ADSC0}$-1, A0A-A3A, A0B-A3B	V_{CC} = 3.3V	C_{I2}	5	10	pF	4
Input Capacitance: $\overline{BW0}$-7		C_{I3}	5	5	pF	4
Input/Output Capacitance: DQ0-63, PDQ0-7		C_O	8	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (V_{CC} = 3.3V ±5%)

DESCRIPTION	SYM	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	-8 MIN	-8 MAX	UNITS	NOTES
Clock											
Clock cycle time	^tKC	10		12		15		20		ns	
Clock HIGH time	^tKH	4		4.5		5		6		ns	
Clock LOW time	^tKL	4		4.5		5		6		ns	
Output Times											
Clock to output valid	^tKQ		5		6		7		8	ns	
Clock to output invalid	^tKQX	2		2		2		2		ns	
Clock to output in Low-Z	^tKQLZ	4		5		5		5		ns	6, 7
Clock to output in High-Z	^tKQHZ		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		5		5		5		6	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		4		5		6		6	ns	6, 7
Setup Times											
Address	^tAS	2.5		2.5		2.5		3		ns	8, 10
Address Status ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1)	^tADSS	2.5		2.5		2.5		3		ns	8, 10
Address Advance ($\overline{ADV0}$-1)	^tAAS	2.5		2.5		2.5		3		ns	8, 10
Byte Write Enables ($\overline{BW0}$-7)	^tWS	2.5		2.5		2.5		3		ns	8, 10
Data-in	^tDS	2.5		2.5		2.5		3		ns	8, 10
Chip Enable ($\overline{CE0}$-1)	^tCES	2.5		2.5		2.5		3		ns	8, 10
Hold Times											
Address	^tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC0}$-1, $\overline{ADSP0}$-1)	^tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV0}$-1)	^tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{BW0}$-7)	^tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enable ($\overline{CE0}$-1)	^tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

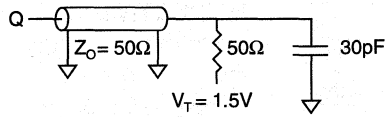


Fig. 1 OUTPUT LOAD EQUIVALENT

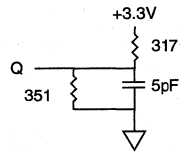


Fig. 2 OUTPUT LOAD EQUIVALENT

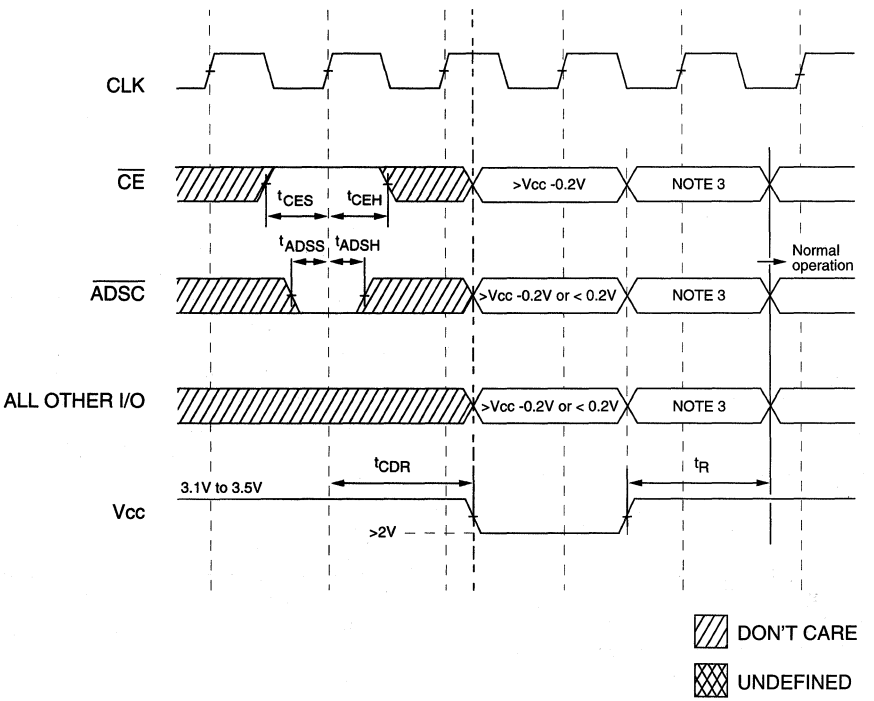
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. The load used for V_{OH}, V_{OL} testing is shown in Fig. 2. AC load current is higher than the shown DC values.
12. "Device deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Typical values are measured at 25°C.
15. The device must have a deselect cycle applied at least two clock cycles before data retention mode is entered.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

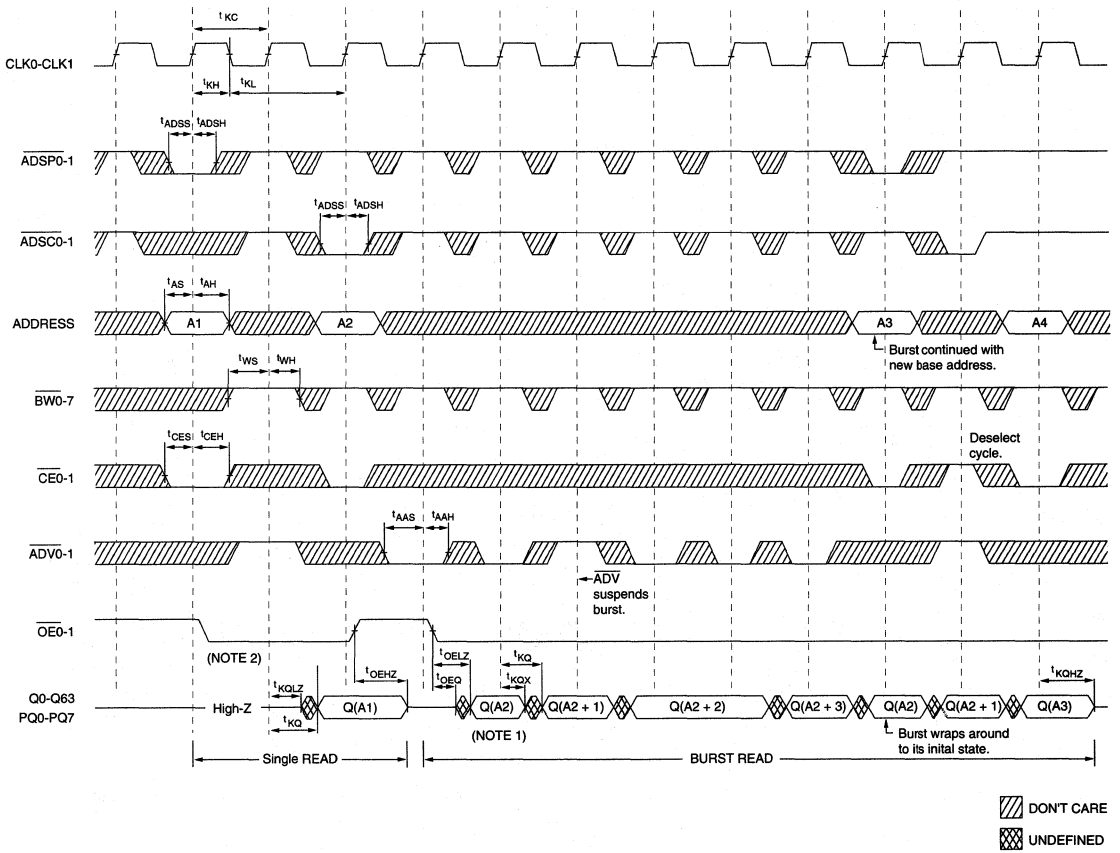
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2} \geq (V_{CC} - 0.2V)$, $CE2 \leq 0.2V$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$ $V_{CC} = 2V$	I_{CCDR}		TBD	µA	14
Chip Deselect to Data Retention Time		^tCDR	^tKC		ns	4, 15
Operation Recovery Time		^tR	^tKC		ns	4

LOW V_{CC} DATA RETENTION WAVEFORM



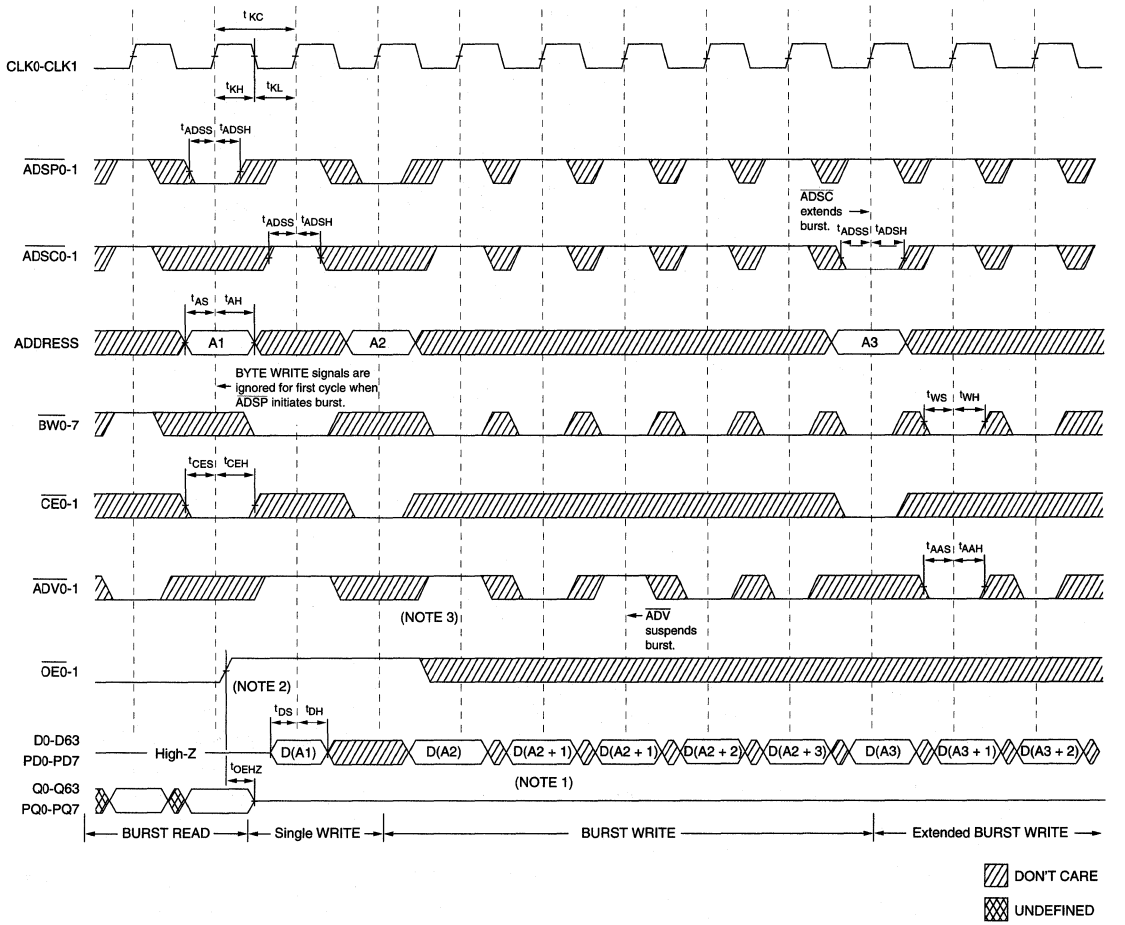
NOTE:
1. All inputs must be ≥ V_{CC} - 0.2V or ≤ 0.2V to guarantee I_{CCDR} in data retention mode. If inputs are between these levels or left floating, I_{CCDR} may be exceeded.
2. Only one of the available deselect cycle sequences is shown above ($\overline{CE}$ = HIGH, $\overline{ADSC}$ = LOW). Any of the other deselect cycle sequences may also be used.
3. The device control signals should be in a deselect state between the rising edge of V_{CC} and until ^tR is met.

READ TIMING



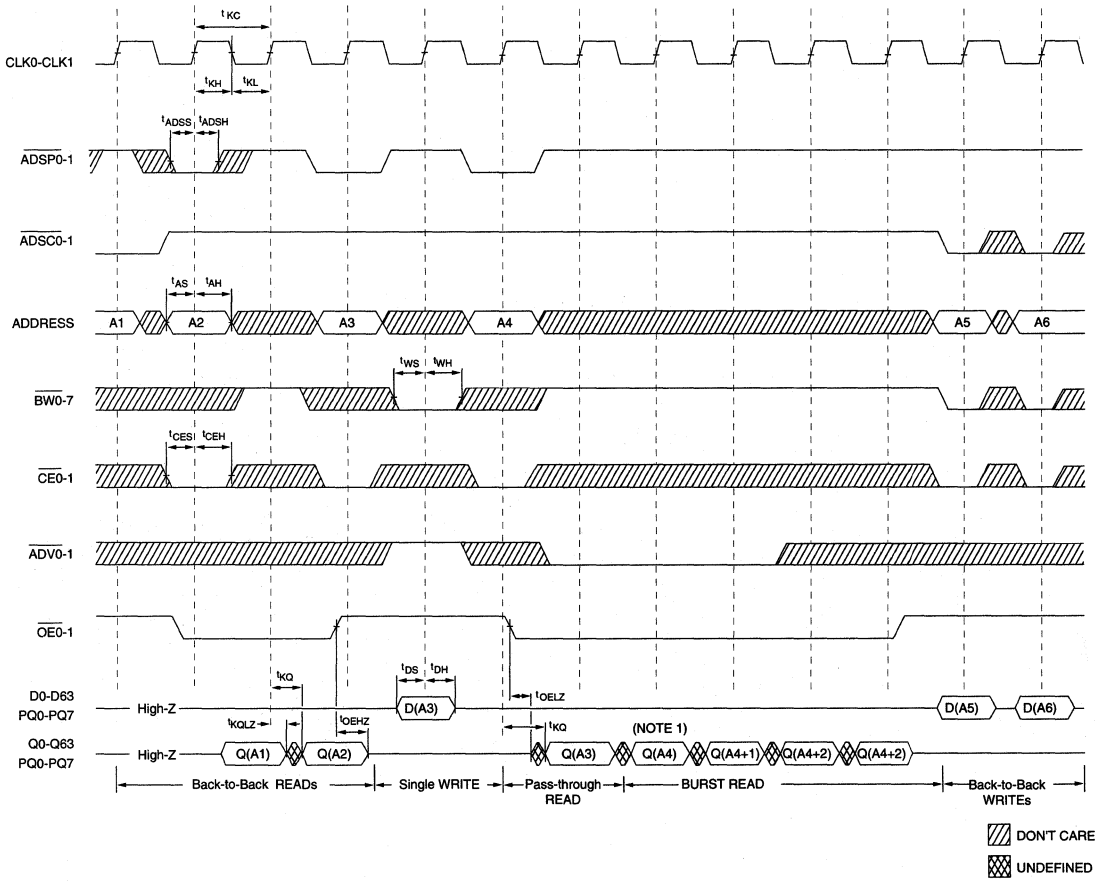
NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. Timing is shown assuming that the device was not enabled before entering into this sequence. $\overline{OE}$ does not cause Q to be driven until after the following clock rising edge.

WRITE TIMING



NOTE:
1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
3. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

READ/WRITE TIMING



NOTE:
1. Q(A4) refers to output from address A4. Q(A4+1) refers to output from the next internal burst address following A4.
2. The data bus (Q) remains in High-Z following a WRITE cycle unless an $\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$ or $\overline{\text{ADV}}$ cycle is performed.
3. Back-to-back READs may be controlled by either $\overline{\text{ADSP}}$ or $\overline{\text{ADSC}}$.

MICRON SEMICONDUCTOR, INC.

MT2LSYT3272T4/T6, MT4LSY6472T4/T6
32K, 64K x 72 SYNCHRONOUS SRAM MODULE

SYNCHRONOUS SRAM MODULE

32K, 64K x 72 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS AND BURST COUNTER

FEATURES

- 80 position dual-read-out dual in-line memory module (DIMM) with 160 leads
- Fast access times: 9, 10, 11 and 12ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant common data I/O
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address data and control
- Internally self-timed WRITE cycle
- Burst control pins (interleaved or linear burst)
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS — MARKING

- Timing
  - 9ns access/15ns cycle — -9
  - 10ns access/15ns cycle — -10
  - 11ns access/15ns cycle — -11
  - 12ns access/20ns cycle — -12
- Packages
  - 160-lead DIMM (gold) — G
- Low power (optional) — P
- 2V data retention, low power (optional) — L
- Part Number Examples: MT2LSYT3272B2G-10 L
  MT4LSYT6472B2G-10 L

GENERAL DESCRIPTION

The Micron Synchronous SRAM module family employs high- speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double- layer metal, double-layer polysilicon technology.

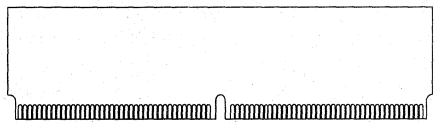
The MT2LSYT3272B2 module integrates two 32K x 36 synchronous SRAMs and the MT4LSYT6472B2 integrates four 64K x 18 synchronous SRAMs. All synchronous inputs pass through registers controlled by positive-edge-triggered clock inputs (CLK0 and CLK1). The synchronous inputs include all addresses, data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and byte write enables ($\overline{BW0}$ - $\overline{BW7}$, $\overline{BWE}$) and global write ($\overline{GW}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and the clocks (CLK0 and CLK1) and burst mode (MODE). The

PIN ASSIGNMENT (Top View)

160-Lead, Dual Read-out DIMM

(SF-1) 32K x 72
(SF-2) 64K x 72



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	41	$\overline{GW}$	81	Vss	121	CE2
2	DQ0	42	Vcc2	82	DQ1	122	RSVD
3	Vcc2	43	RSVD	83	RSVD	123	RSVD
4	DQ2	44	A13	84	DQ3	124	A14
5	DQ4	45	MODE	85	DQ5	125	$\overline{ADV}$
6	DQ6	46	A15	86	DQ7	126	A16
7	DQP0	47	A17	87	DQ8	127	A18*
8	Vss	48	NC	88	Vss	128	NC
9	DQ9	49	DQ32	89	DQ10	129	DQ33
10	DQ11	50	NC	90	DQ12	130	NC
11	DQ13	51	Vss	91	DQ14	131	Vss
12	Vcc2	52	DQ34	92	RSVD	132	DQ35
13	DQ15	53	DQ36	93	DQP1	133	DQ37
14	DQ16	54	DQ38	94	Vss	134	DQ39
15	Vss	55	DQ40	95	DQ17	135	DQP4
16	DQ18	56	$\overline{BW4}$	96	DQ19	136	$\overline{BW5}$
17	DQ20	57	Vss	97	DQ21	137	Vss
18	$\overline{OE}$	58	$\overline{BW6}$	98	DQ22	138	$\overline{BW7}$
19	Vss	59	DQ41	99	Vss	139	DQ42
20	$\overline{BW0}$	60	DQ43	100	$\overline{BW1}$	140	DQ44
21	DQ23	61	DQ45	101	DQP2	141	DQ46
22	DQ24	62	Vcc2	102	DQ25	142	RSVD
23	Vcc2	63	DQ47	103	RSVD	143	DQ48
24	DQ26	64	DQP5	104	DQ27	144	DQ49
25	DQ28	65	DQ50	105	DQ29	145	DQ51
26	DQ30	66	DQ52	106	DQ31	146	DQ53
27	DQP3	67	DQ54	107	A6	147	DQ55
28	A5	68	Vss	108	A8	148	Vss
29	A7	69	PRD0	109	A10	149	PRD1
30	A9	70	Vcc2	110	A12	150	RSVD
31	$\overline{BW2}$	71	DQ56	111	$\overline{BW3}$	151	DQP6
32	Vss	72	DQ57	112	Vss	152	DQ58
33	$\overline{BWE}$	73	Vss	113	CLK0	153	Vss
34	A11	74	DQ59	114	A3	154	DQ60
35	A4	75	DQ61	115	$\overline{CE2}$	155	DQ62
36	RSVD	76	DQ63	116	RSVD	156	DQP7
37	$\overline{ADSC}$	77	PRD2	117	$\overline{ADSP}$	157	PRD3
38	RSVD	78	Vcc2	118	RSVD	158	RSVD
39	$\overline{CE}$	79	NC	119	CLK1*	15	NC
40	Vss	80	Vss	120	Vss	160	Vss

*64K x 72 version only

GENERAL DESCRIPTION (continued)

Data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to eight bytes wide as controlled by the byte write enables.

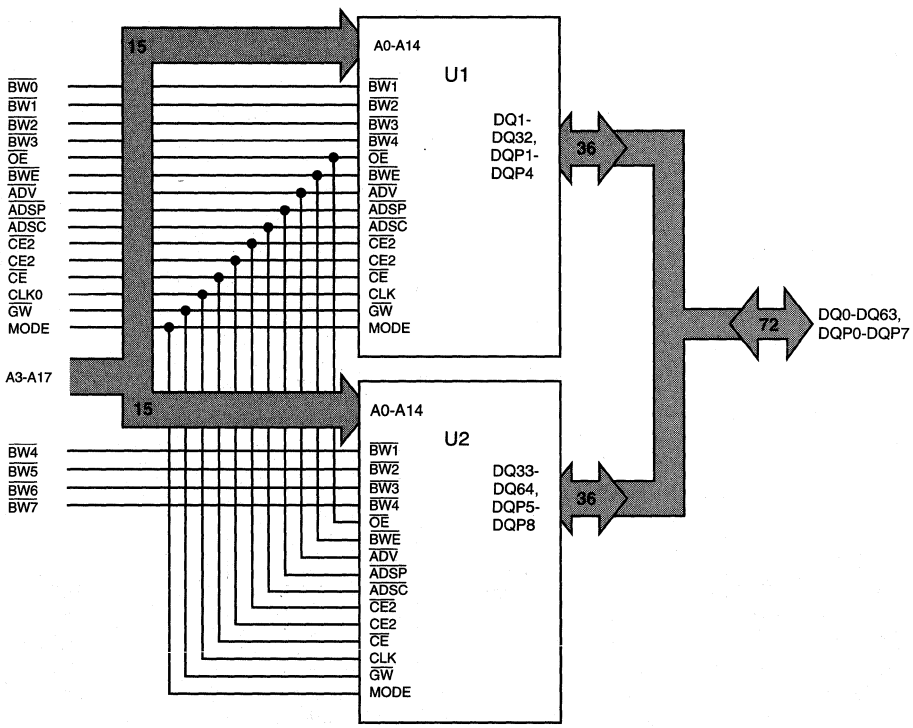
Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW0}$ controls DQ0-DQ7 and DQP0, $\overline{BW1}$ controls DQ8-DQ15 and DQP1, $\overline{BW2}$ controls DQ16-DQ23 and DQP2, $\overline{BW3}$ controls DQ24-DQ31 and DQP4 and so forth.

The "L" version of this module has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The module operates from a +3.3V power supply and all inputs and outputs are TTL compatible and 5V tolerant. This module is ideally suited to Pentium™, 680X0 and Power PC™ systems and systems that benefit from a very wide data bus. The module is also ideal in generic 32- and 64-bit-wide applications. For additional functional and timing information consult the MT58LC32K36B2 and MT58LC64K18B2 synchronous SRAM data sheets.

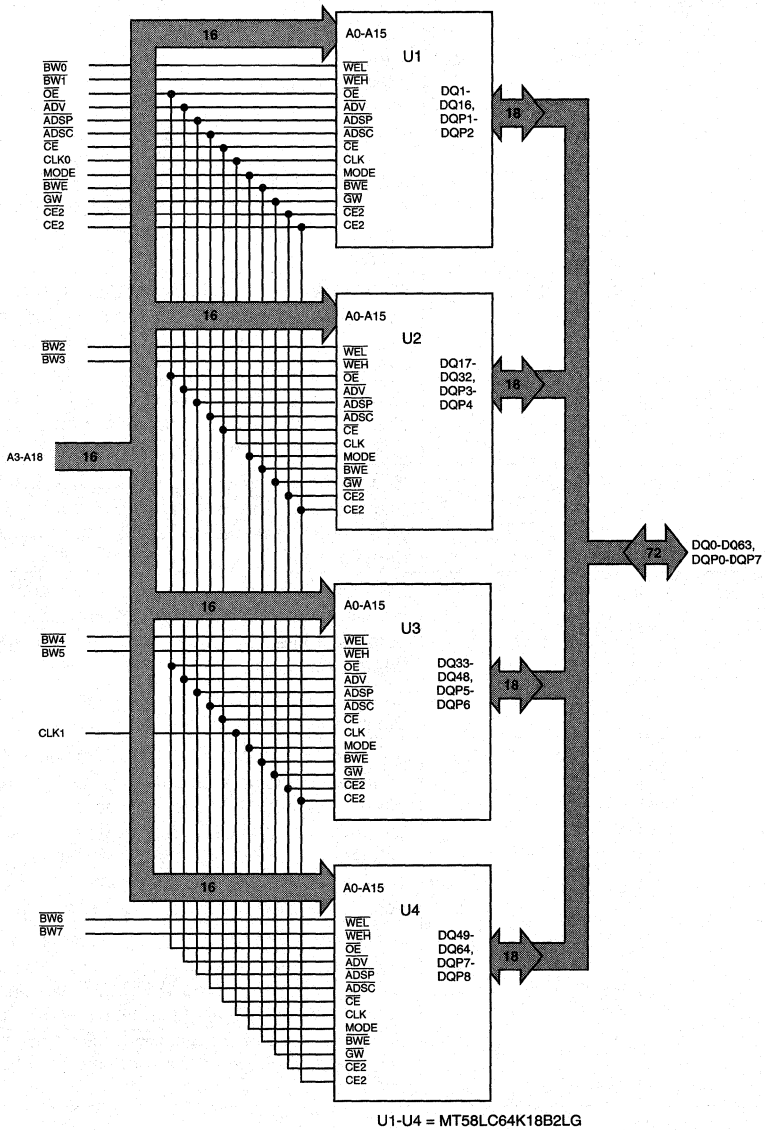
FUNCTIONAL BLOCK DIAGRAM
256KB
(32K x 72)



U1-U2 = MT58LC32K36B2LG

NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See MT58LC32K36B2 synchronous SRAM data sheet for more detailed functional information.

FUNCTIONAL BLOCK DIAGRAM
512KB
(64K x 72)



U1-U4 = MT58LC64K18B2LG

NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See MT58LC64K18B2 synchronous SRAM data sheet for more detailed functional information.

PIN DESCRIPTIONS

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
28-30, 34-35, 44, 46-47, 107-110, 114, 124, 126-127	A3-A18	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
20, 31, 56, 58, 100, 111, 136, 138	$\overline{BW0}$-7	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when $\overline{BWE}$ is LOW and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW0}$ controls DQ0-DQ7 and DQP0. $\overline{BW1}$ controls DQ8-DQ15 and DQP1. $\overline{BW2}$ controls DQ16-DQ23 and DQP2. $\overline{BW3}$ controls DQ24-DQ31 and DQP3, and so forth. Data I/O are tristated if any of these eight inputs are LOW.
113, 119	CLK0-CLK1	Input	Clock: This signal latches the address, data, chip enables, bytewrite enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge. (CLK1 used on 64K x 72 only).
39	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
121	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
115	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
18	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
125	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
117	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.

PIN DESCRIPTIONS (continued)

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
37	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external addressto be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
36, 38, 43, 83, 92, 103, 116, 118, 122, 123, 142, 150, 158	RSVD	-	No Connect: These pins are reserved.
33	$\overline{BWE}$	Input	Byte Write Enable: This active low input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
41	$\overline{GW}$	Input	Global Write: This active low input allows a full 36-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BW}$n lines and must meet the setup and hold times around the rising edge of CLK.
45	MODE	Input	Mode: This input selects the burst sequence. A low on this pin selects LINEAR BURST. A NC on this pin selects INTER-LEAVED BURST. Do not alter input state while device is operating.
2, 4-6, 9-11, 13-14, 16-17, 21-22, 24- 26, 49, 52-55, 59-61, 63, 65-67, 71-72, 74-76, 82, 84-87, 89-91, 95-98, 102, 104-106, 129, 132-134, 139-141, 143-147, 152, 154-155	DQ0-DQ63	Input/ Output	SRAM Data I/O: Byte 1 is DQ0-DQ7; Byte 2 is DQ8-DQ15; Byte 3 is DQ16-DQ23; Byte 4 is DQ24-DQ31 and so forth. Input data must meet setup and hold times around the rising edge of CLK
7, 27, 64, 93, 101, 135, 151, 156	DQP0-DQP7	Input/ Output	Parity Data I/O: Byte 1 Parity is DQP0; Byte 2 Parity is DQP1 and so forth.
3, 12, 23, 42, 62, 70, 78	Vcc2	Supply	Power Supply: +3.3V ±5%
1, 8, 15, 19, 32, 40, 51, 57, 68, 73, 80, 81, 88, 94, 99, 112, 120, 131, 137, 148, 153, 160	Vss	Supply	Ground: GND

PRESENCE-DETECT TABLE

Description	Size	PRD3	PRD2	PRD1	PRD0
None		NC	NC	NC	NC
Synchronous Pipelined	256KB	NC	Vss	NC	NC
Synchronous Pipelined	512KB	NC	Vss	NC	Vss
Synchronous	256KB	NC	Vss	Vss	NC
Synchronous	512KB	NC	Vss	Vss	Vss
Asynchronous	256KB	NC	NC	NC	Vss
Asynchronous	512KB	NC	NC	Vss	NC
Reserved		NC	NC	Vss	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +125°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	V_{IH}		2.0	5.5	V		1, 2
Input Low (Logic 0) Voltage	V_{IL}		-0.3	0.8	V		1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	$\overline{BW0}$-7	I_{LI1}	-1	1	µA	7
		A3-A18	I_{LI2}	-4	4	µA	7
		All other inputs	I_{LI3}	-2	2	µA	7
Output Leakage Current	Output(s) Disabled, 0V ≤ V_{OUT} ≤ V_{CC}		I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			V_{CC}	3.1	3.5	V	1

DESCRIPTION	CONDITIONS	SYM	VER	SIZE	TYP	MAX -9	MAX -10	MAX -11	MAX -12	UNITS	NOTES
Power Supply Current: Operating	Device selected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; outputs open	I_{CC1}	ALL	256KB	400	600	600	550	500	mA	3, 5, 6
				512KB	700	1,000	1,000	900	800	mA	
Power Supply Current: Idle	Device selected; V_{CC} = MAX; $\overline{GW}$, $\overline{BW}$, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; cycle time ≥ ^tKC MIN; outputs open	I_{CC2}	ALL	256KB	56	90	90	90	80	mA	5, 6
				512KB	112	180	180	180	160	mA	
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB1}	STD	256KB	1.0	10	10	10	10	mA	5, 6
				512KB	2.0	20	20	20	20		
			P	256KB	0.4	4	4	4	4	mA	
				512KB	0.8	8	8	8	8		
TTL Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB2}	STD	256KB	30	50	50	50	50	mA	5, 6
				512KB	60	100	100	100	100		
			P	256KB	16	36	36	36	36	mA	
				512KB	40	72	72	72	72		
Clock Running	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB3}	ALL	256KB	60	100	100	100	90	mA	5, 6
				512KB	120	200	200	200	180	mA	

SYNCHRONOUS SRAM MODULE

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX 256KB	MAX 512KB	UNITS	NOTES
Input Capacitance: A3-A18,$\overline{ADSC}$, $\overline{GW}$, MODE	T_A = 25°C; f = 1 MHz	C_{I1}	10	20	pF	4
Input Capacitance: $\overline{ADSP}$, $\overline{ADV}$,CLK,$\overline{OE}$,$\overline{CE}$, $\overline{BWE}$	V_{CC} = 3.3V	C_{I2}	10	20	pF	4
Input Capacitance: $\overline{BW}$0-7		C_{I3}	5	5	pF	4
Input/Output Capacitance: DQ0-63,PDQ0-7		C_O	8	8	pF	4

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2}$ ≥ (V_{CC} -0.2V), CE2 ≤ 0.2V V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V V_{CC} = 2V	I_{CCDR}		TBD	µA	8
Chip Deselect to Data Retention Time		^tCDR	^tKC		ns	4, 9
Operation Recovery Time		^tR	^tKC		ns	4

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: V_{IH} ≤ +6.0V for t ≤ ^tKC /2.
   Undershoot: V_{IL} ≥ -2.0V for t ≤ ^tKC /2.
   Power-up: V_{IH} ≤ +6.0V and V_{CC} ≤ 3.1V for t ≤ 200ms
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. "Device deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device selected" means device is active (not in POWER-DOWN mode).
6. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
7. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
8. Typical values are measured at 25°C.
9. The device must have a deselect cycle applied at least one clock cycle before data retention mode is entered.

MICRON SEMICONDUCTOR, INC.

MT2LSYT3272B2, MT4LSYT6472B2
32K, 64K x 72 SYNCHRONOUS SRAM MODULE

SYNCHRONOUS SRAM MODULE

32K, 64K x 72 SRAM

+3.3V SUPPLY, FULLY REGISTERED INPUTS, OUTPUTS AND BURST COUNTER

FEATURES

- 80 position dual read-out dual in-line memory module (DIMM) with 160 leads
- Fast access times: 5, 6, 7 and 8ns
- Fast $\overline{OE}$: 5 and 6ns
- Single +3.3V ±5% power supply
- 5V-tolerant common data I/O
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock controlled, registered, address, data I/O and control for fully pipelined applications
- Internally self-timed WRITE cycle
- WRITE pass-through capability
- Burst control pins (interleaved or linear burst)
- Low capacitive bus loading
- High 30pF output drive capability at rated access time

OPTIONS — MARKING

- Timing
  - 5ns access/10ns cycle — -5
  - 6ns access/12ns cycle — -6
  - 7ns access/15ns cycle — -7
  - 8ns access/20ns cycle — -8
- Packages
  - 160-lead DIMM (gold) — G
- Low power (optional) — P
- 2V data retention, low power (optional) — L
- Part Number Examples: MT2LSYT3272C4G-5 L
  MT4LSYT6472C4G-5 L

GENERAL DESCRIPTION

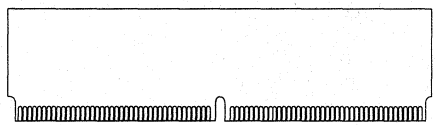
The Micron Synchronous SRAM module family employs high- speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double- layer metal, double-layer polysilicon technology.

The MT2LSYT3272C4 module integrates two 32K x 36 synchronous SRAMs and the MT4LSYT6472C4 integrates four 64K x 18 synchronous SRAMs. All synchronous inputs pass through registers controlled by positive-edge-triggered clock inputs (CLK0 and CLK1). The synchronous inputs include all addresses, data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and byte write enables ($\overline{BW0}$ - $\overline{BW7}$, $\overline{BWE}$) and global write ($\overline{GW}$).

PIN ASSIGNMENT (Top View)

160-Lead, Dual Read-out DIMM

(SF-1) 32K x 72
(SF-2) 64K x 72



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	41	$\overline{GW}$	81	Vss	121	CE2
2	DQ0	42	Vcc2	82	DQ1	122	RSVD
3	Vcc2	43	RSVD	83	RSVD	123	RSVD
4	DQ2	44	A13	84	DQ3	124	A14
5	DQ4	45	MODE	85	DQ5	125	$\overline{ADV}$
6	DQ6	46	A15	86	DQ7	126	A16
7	DQP0	47	A17	87	DQ8	127	A18*
8	Vss	48	NC	88	Vss	128	NC
9	DQ9	49	DQ32	89	DQ10	129	DQ33
10	DQ11	50	NC	90	DQ12	130	NC
11	DQ13	51	Vss	91	DQ14	131	Vss
12	Vcc2	52	DQ34	92	RSVD	132	DQ35
13	DQ15	53	DQ36	93	DQP1	133	DQ37
14	DQ16	54	DQ38	94	Vss	134	DQ39
15	Vss	55	DQ40	95	DQ17	135	DQP4
16	DQ18	56	$\overline{BW4}$	96	DQ19	136	$\overline{BW5}$
17	DQ20	57	Vss	97	DQ21	137	Vss
18	$\overline{OE}$	58	$\overline{BW6}$	98	DQ22	138	$\overline{BW7}$
19	Vss	59	DQ41	99	Vss	139	DQ42
20	$\overline{BW0}$	60	DQ43	100	$\overline{BW1}$	140	DQ44
21	DQ23	61	DQ45	101	DQP2	141	DQ46
22	DQ24	62	Vcc2	102	DQ25	142	RSVD
23	Vcc2	63	DQ47	103	RSVD	143	DQ48
24	DQ26	64	DQP5	104	DQ27	144	DQ49
25	DQ28	65	DQ50	105	DQ29	145	DQ51
26	DQ30	66	DQ52	106	DQ31	146	DQ53
27	DQP3	67	DQ54	107	A6	147	DQ55
28	A5	68	Vss	108	A8	148	Vss
29	A7	69	PRD0	109	A10	149	PRD1
30	A9	70	Vcc2	110	A12	150	RSVD
31	$\overline{BW2}$	71	DQ56	111	$\overline{BW3}$	151	DQP6
32	Vss	72	DQ57	112	Vss	152	DQ58
33	$\overline{BWE}$	73	Vss	113	CLK0	153	Vss
34	A11	74	DQ59	114	A3	154	DQ60
35	A4	75	DQ61	115	$\overline{CE2}$	155	DQ62
36	RSVD	76	DQ63	116	RSVD	156	DQP7
37	$\overline{ADSC}$	77	PRD2	117	$\overline{ADSP}$	157	PRD3
38	RSVD	78	Vcc2	118	RSVD	158	RSVD
39	$\overline{CE}$	79	NC	119	CLK1*	15	NC
40	Vss	80	Vss	120	Vss	160	Vss

*64K x 72 version only

GENERAL DESCRIPTION (continued)

Asynchronous inputs include the output enable ($\overline{OE}$) and the clocks (CLK0 and CLK1) and burst mode (MODE). The Data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to eight bytes wide as controlled by the byte write enables.

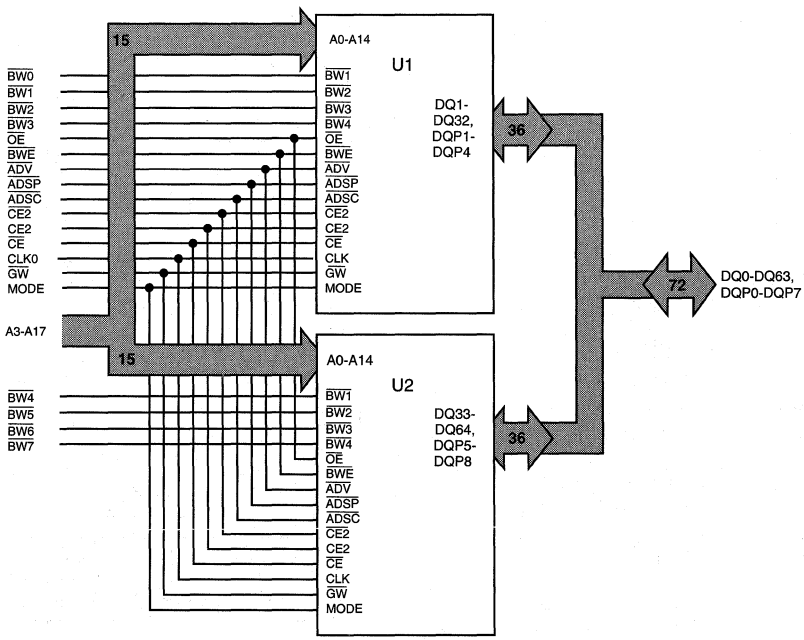
Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW0}$ controls DQ0-DQ7 and DQP0, $\overline{BW1}$ controls DQ8-DQ15 and DQP1, $\overline{BW2}$ controls DQ16-DQ23 and DQP2, $\overline{BW3}$ controls DQ24-DQ31 and DQP4 and so forth, conditioned by $\overline{BWE}$ being LOW. $\overline{GW}$ LOW causes all bytes to be written. WRITE pass-through makes written data immediately available at the output register during the READ cycle following a WRITE as controlled solely by $\overline{OE}$ to improve cache system response. The module incorporates an additional pipelined enable register to allow depth expansion without penalizing system performance.

The "L" version of this module has a data retention option which is useful for battery backup mode of operation. Although the part is not guaranteed to operate functionally below Vcc MIN (3.1V), it will retain data with a minimum of power dissipation.

The module operates from a +3.3V power supply and all inputs and outputs are TTL compatible and 5V tolerant. This module is ideally suited to Pentium™, and Power PC™ systems and systems that benefit from a very wide data bus. The module is also ideal in generic 32- and 64-bit-wide applications. For additional functional and timing information consult the MT58LC32K36C4 and MT58LC64K18C4 synchronous SRAM data sheets.

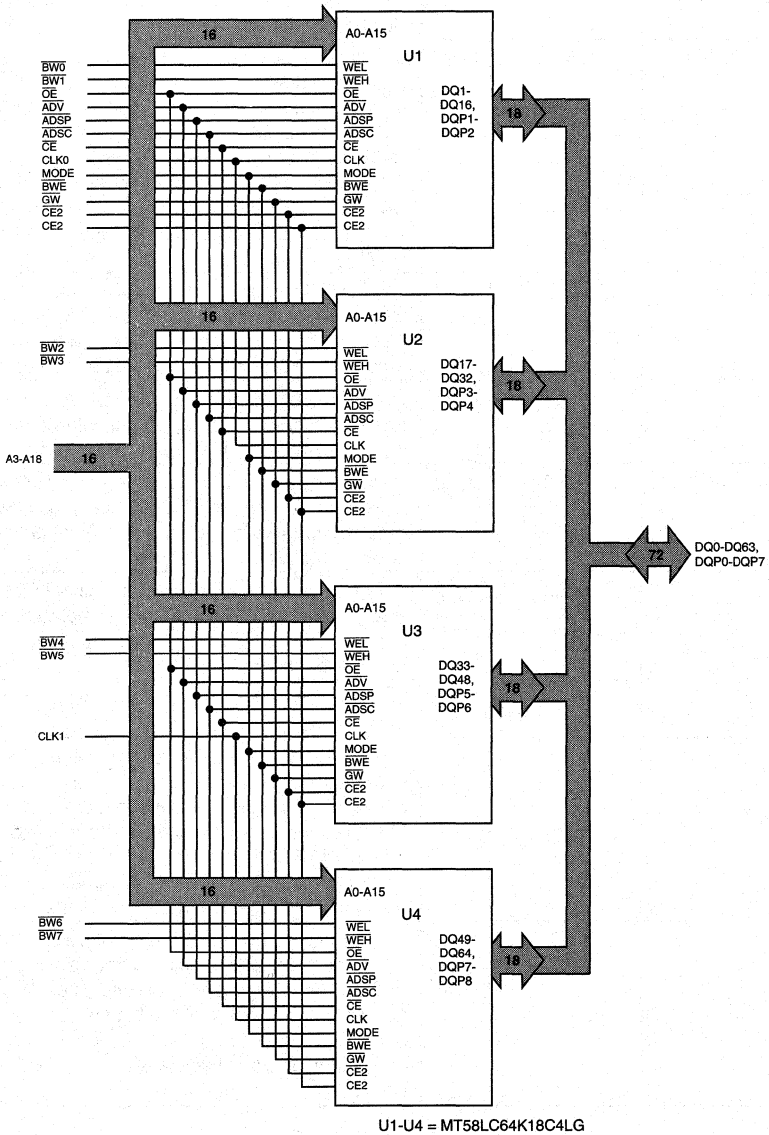
FUNCTIONAL BLOCK DIAGRAM
256KB
(32K x 72)



U1-U2 = MT58LC32K36C4LG

NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See MT58LC32K36C4 synchronous SRAM data sheet for more detailed functional information.

FUNCTIONAL BLOCK DIAGRAM
512KB
(64K x 72)



U1-U4 = MT58LC64K18C4LG

NOTE: 1. The Functional Block Diagram illustrates simplified module operation. See MT58LC64K18C4 synchronous SRAM data sheet for more detailed functional information.

PIN DESCRIPTIONS

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
28-30, 34-35, 44, 46-47, 107-110, 114, 124, 126-127	A3-A18	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
20, 31, 56, 58, 100, 111, 136, 138	$\overline{BW0}$-7	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written when $\overline{BWE}$ is LOW and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW0}$ controls DQ0-DQ7 and DQP0. $\overline{BW1}$ controls DQ8-DQ15 and DQP1. $\overline{BW2}$ controls DQ16-DQ23 and DQP2 $\overline{BW3}$ controls DQ24-DQ31 and DQP3, and so forth. Data I/O are tristated if any of these eight inputs are LOW.
113, 119	CLK0-CLK1	Input	Clock: This signal latches the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge. (CLK1 used on 64K x 72 only).
39	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
121	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
115	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
18	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
125	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
117	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$, but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.

PIN DESCRIPTIONS (continued)

MODULE PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
37	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
36, 38, 43, 83, 92, 103, 116, 118, 122, 123, 142, 150, 158	RSVD	-	No Connect: These pins are reserved.
33	$\overline{BWE}$	Input	Byte Write Enable: This active low input permits byte write operations and must meet the setup and hold times around the rising edge of CLK.
41	$\overline{GW}$	Input	Global Write: This active low input allows a full 36-bit WRITE to occur independent of the $\overline{BWE}$ and $\overline{BW}$n lines and must meet the setup and hold times around the rising edge of CLK.
45	MODE	Input	Mode: This input selects the burst sequence. A low on this pin selects LINEAR BURST. A NC on this pin selects INTER-LEAVED BURST. Do not alter input state while device is operating.
2, 4-6, 9-11, 13-14, 16-17, 21-22, 24-26, 49, 52-55, 59-61, 63, 65-67, 71-72, 74-76, 82, 84-87, 89-91, 95-98, 102, 104-106, 129, 132-134, 139-141, 143-147, 152, 154-155	DQ0-DQ63	Input/ Output	SRAM Data I/O: Byte 1 is DQ0-DQ7; Byte 2 is DQ8-DQ15; Byte 3 is DQ16-DQ23; Byte 4 is DQ24-DQ31 and so forth. Input data must meet setup and hold times around the rising edge of CLK
7, 27, 64, 93, 101, 135, 151, 156	DQP0-DQP7	Input/ Output	Parity Data I/O: Byte 1 Parity is DQP0; Byte 2 Parity is DQP1 and so forth.
3, 12, 23, 42, 62, 70, 78	V_{CC2}	Supply	Power Supply: +3.3V ±5%
1, 8, 15, 19, 32, 40, 51, 57, 68, 73, 80, 81, 88, 94, 99, 112, 120, 131, 137, 148, 153, 160	Vss	Supply	Ground: GND

PRESENCE-DETECT TABLE

Description	Size	PRD3	PRD2	PRD1	PRD0
None		NC	NC	NC	NC
Synchronous Pipelined	256KB	NC	Vss	NC	NC
Synchronous Pipelined	512KB	NC	Vss	NC	Vss
Synchronous	256KB	NC	Vss	Vss	NC
Synchronous	512KB	NC	Vss	Vss	Vss
Asynchronous	256KB	NC	NC	NC	Vss
Asynchronous	512KB	NC	NC	Vss	NC
Reserved		NC	NC	Vss	Vss

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6V
Storage Temperature (plastic) ..... -55°C to +125°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage			V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage			V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	$\overline{BW0}$-7	I_{LI1}	-1	1	µA	7
		A3-A18	I_{LI2}	-4	4	µA	7
		All other inputs	I_{LI3}	-2	2	µA	7
Output Leakage Current	Output(s) Disabled, 0V ≤ V_{OUT} ≤ V_{CC}		I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA		V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA		V_{OL}		0.4	V	1
Supply Voltage			V_{CC}	3.1	3.5	V	1

DESCRIPTION	CONDITIONS	SYM	VER	SIZE	TYP	MAX -5	MAX -6	MAX -7	MAX -8	UNITS	NOTES
Power Supply Current: Operating	Device selected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; outputs open	I_{CC1}	ALL	256KB	400	800	700	600	500	mA	3, 5, 6
				512KB	720	1,340	1,200	1,000	840	mA	
Power Supply Current: Idle	Device selected; V_{CC} = MAX; $\overline{GW}$, $\overline{BW}$, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; cycle time ≥ ^tKC MIN	I_{CC2}	ALL	256KB	60	120	110	100	90	mA	5, 6
				512KB	120	240	220	200	180	mA	
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB1}	STD	256KB	1.0	10	10	10	10	mA	5, 6
				512KB	2.0	20	20	20	20		
			P	256KB	0.4	4	4	4	4	mA	
				512KB	0.8	8	8	8	8		
TTL Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; CLK frequency = 0	I_{SB2}	STD	256KB	30	50	50	50	50	mA	5, 6
				512KB	60	100	100	100	100		
			P	256KB	16	36	36	36	36	mA	
				512KB	32	72	72	72	72		
Clock Running	Device deselected; V_{CC} = MAX; all inputs ≤ Vss +0.2 or ≥ V_{CC} -0.2; CLK cycle time ≥ ^tKC MIN	I_{SB3}	ALL	256KB	60	120	110	100	90	mA	5, 6
				512KB	120	240	220	200	180	mA	

SYNCHRONOUS SRAM MODULE

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX 256KB	MAX 512KB	UNITS	NOTES
Input Capacitance: A3-A18, $\overline{ADSC}$, $\overline{GW}$, MODE	T_A = 25°C; f = 1 MHz	C_{I1}	10	20	pF	4
Input Capacitance: $\overline{ADSP}$, $\overline{ADV}$, CLK, $\overline{OE}$, $\overline{CE}$, $\overline{BWE}$	V_{CC} = 3.3V	C_{I2}	10	20	pF	4
Input Capacitance: $\overline{BW}$0-7		C_{I3}	5	5	pF	4
Input/Output Capacitance: DQ0-63, PDQ0-7		C_O	8	8	pF	4

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2			V
Data Retention Current	$\overline{CE}$, $\overline{CE2}$ ≥ (V_{CC} -0.2V), CE2 ≤ 0.2V V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V V_{CC} = 2V	I_{CCDR}		TBD	µA	8
Chip Deselect to Data Retention Time		^tCDR	^tKC		ns	4, 9
Operation Recovery Time		^tR	^tKC		ns	4

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: V_{IH} ≤ +6.0V for t ≤ ^tKC /2.
   Undershoot: V_{IL} ≥ -2.0V for t ≤ ^tKC /2.
   Power-up: V_{IH} ≤ +6.0V and Vcc ≤ 3.1V for t ≤ 200ms
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. "Device deselected" means device is in POWER-DOWN mode as defined in the Truth Table. "Device selected" means device is active (not in POWER-DOWN mode).
6. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
7. MODE pin has an internal pull-up and exhibits an input leakage current of ±10µA.
8. Typical values are measured at 25°C.
9. The device must have a deselect cycle applied at least one clock cycle before data retention mode is entered.

MICRON SEMICONDUCTOR, INC.

MT2LSYT3272C4, MT4LSYT6472C4
32K, 64K x 72 SYNCHRONOUS SRAM MODULE

MICRON
SEMICONDUCTOR, INC.

TECHNICAL NOTE SELECTION GUIDE

TECHNICAL NOTE

MOISTURE ABSORPTION IN PLASTIC PACKAGES

INTRODUCTION

All plastic integrated-circuit packages have a tendency to absorb moisture. During surface-mount assembly, this moisture can vaporize when subjected to the heat associated with solder reflow operations. Vaporization creates internal stresses that can cause the plastic molding compound to crack. Cracks in the package allow contamination to penetrate to the die and potentially reduce the reliability of the semiconductor device. The cracking process associated with surface-mountable devices is commonly referred to as the "popcorn effect."

Cracks in the plastic pose several reliability concerns. The moisture path to the die is shortened, allowing ion migration or corrosion to occur more readily. Minor cracks which might not be harmful initially could propagate with time, resulting in a longer-term functional failure.

Since plastic packages absorb moisture, care must be taken to prevent exposure for any long period prior to surface-mounting the devices on the printed circuit board. If exposed to excessive moisture, the devices should be baked to remove moisture prior to solder reflow operations.

This technical note describes the shipping procedures that ensure Micron's customers will receive memory devices that do not exhibit the popcorn effect. It also discusses Micron's recommendations for baking the devices if they are exposed to excessive moisture.

ABSORPTION CHARACTERISTICS

Micron's extensive testing empirically characterizes the moisture absorption characteristics of plastic packages. As the plastic takes on moisture, the weight of the device increases. Micron employs a standard procedure for weighing the device before and after it is exposed to moisture. We calculate the percentage of weight gain to determine the relative efficiency of different packaging techniques used for shipping devices.

MICRON PROCEDURES

Micron has eliminated any chance of having popcorn failures with surface-mount packages by shipping all surface-mount devices in sealed bags containing a desiccant. Devices stored in these bags show no measurable weight gain when subjected to a high-humidity environment for long time periods.

DEVICE STORAGE

To prevent device failure due to the popcorn effect, store plastic surface-mount packages carefully before PCB assembly. Micron has run tests on devices that have been exposed to 50 percent humidity outside of their shipping containers for time intervals from six months to one year, and no failures have been recorded.

Any concerns about the moisture absorption can be eliminated by storing the devices in Micron's shipping bags. We designed these containers to prevent the passage of water vapor for long periods of time.

DEVICE BAKING

If devices have been removed from their shipping containers and exposed to high levels of moisture, Micron recommends a device bake-out procedure before surface mounting. This bake-out may be accomplished by placing the parts in a tray and baking them in an oven for 160 hours at 40° C. Any moisture is driven out of the devices during the exposure to the heat.

Moisture may be removed faster by baking at 100° C for 24 hours.

SUMMARY

1. All plastic packages absorb moisture when exposed to high levels of humidity for long time intervals.
2. Micron devices have not exhibited any popcorn effect when exposed to 50 percent humidity for long time periods.
3. Micron ships all surface-mount packages in containers that prevent absorption of moisture.
4. If devices have been removed from their shipping containers and exposed to excessive moisture, they should be baked before being surface-mounted.

REFERENCES

"Moisture Absorption and Mechanical Performance of Surface Mountable Plastic Packages": Bhattacharyya, B. K., et al. : 1988 Proceedings of the 38th Electronics Components Conference.

"Analysis of Package Cracking During Reflow Soldering Process": Kitano, M., et al. : 26th Annual Proceeding, Reliability Physics, 1988.

"Moisture Induced Package Cracking in Plastic Encapsulated Surface Mounted Components During Solder Reflow Process": Lin, R., et al.: 26th Annual Proceeding, Reliability Physics, 1988.

TECHNICAL NOTE

TAPE-AND-REEL PROCEDURES

GENERAL DESCRIPTION

Tape-and-reel is becoming the packaging and shipment method of choice for Micron's surface-mounted memory devices. Tape-and-reel minimizes the handling of components by directly interfacing with automatic pick-and-place machines.

Micron supports the Electronic Industries Association's (EIA) standardization of tape-and-reel specifications number 481A. The intent of this technical note is to describe Micron's status in support of the EIA standard.

Table 1*
MICRON TAPE SIZES AND DEVICES PER REEL

COMPONENT	TAPE WIDTH (W) mm	PITCH (P) mm	DEVICES PER 13-INCH REEL
PLCC			
18 Pin	24	12	1,000
32 Pin	24	16	500
52 Pin	32	24	500
SOJ (300 mil)			
20/26 Pin	24	12	1,000
24 Pin	24	12	1,000
28 Pin	24	12	1,000
32 Pin	32	12	1,000
SOJ (400 mil)			
28 Pin	32	16	500
32 Pin	44	16	500
40 Pin	44	16	500
TSOP (300 mil)			
20/26 Pin	24	12	1,000
TSOP (400 mil)			
40/44 Pin	32	16	1,000

*These are examples of tape-and-reel sizes available. Please contact Micron for all available options.

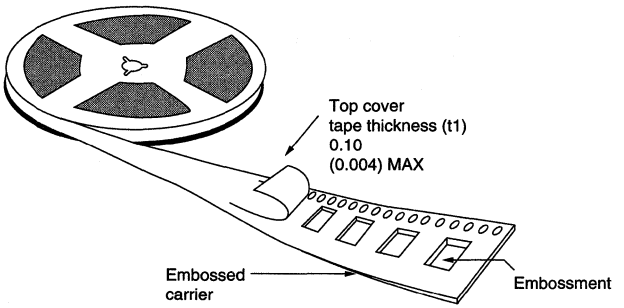


Figure 1
REEL

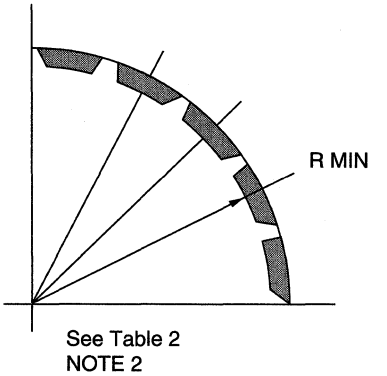
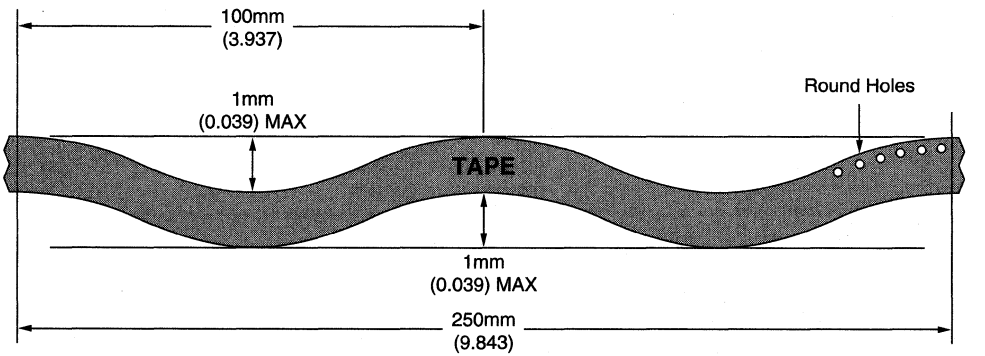


Figure 2
BENDING RADIUS



Allowable camber to be 1mm/100mm nonaccumulative over 250mm.

Figure 3
CAMBER
(top view)

TECHNICAL NOTE

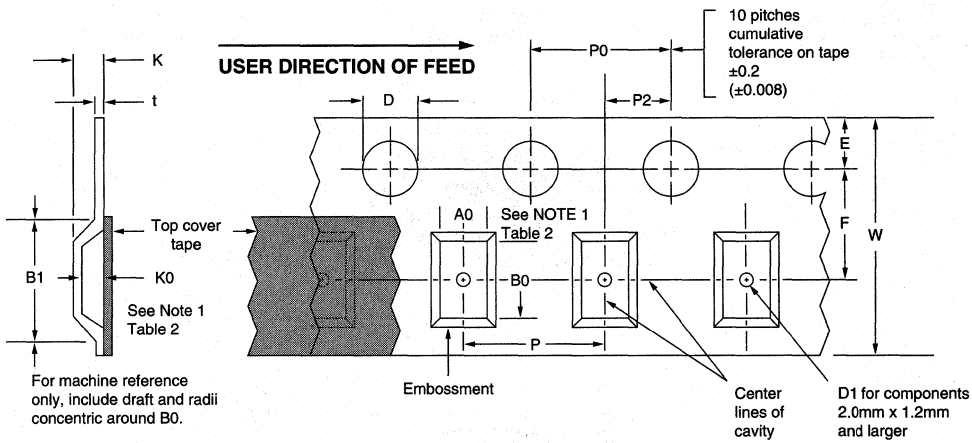


Figure 4
EMBOSSED CARRIER DIMENSIONS
(24mm tape only)

Table 2
24mm EMBOSSED TAPE DIMENSIONS [3]

TAPE SIZE	D	E	P0	t (MAX)	A0, B0, K0
24mm	1.5 $^{+0.10}_{-0.00}$ (0.59) $^{+0.004}_{-0.000}$	1.75 (0.069 ±0.004)	4 (0.157 ±0.004)	0.400 (0.16)	Note 1

TAPE SIZE	B1 (MAX)	D1 (MIN)	F	K (MAX)	P2	R (MIN)	W
24mm	20.1 (0.791)	1.5 (0.059)	11.5 ±0.10 (0.453 ±0.004)	6.5 (0.256)	2 ±0.10 (0.079 ±0.004)	50 (1.969)	24 ±0.30 (0.945 ±0.012)

TAPE SIZE	P					
	4 ±0.10 (0.157 ±0.004)	8 ±0.10 (0.315 ±0.004)	12 ±0.10 (0.472 ±0.004)	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)
24mm			x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters, (inches).

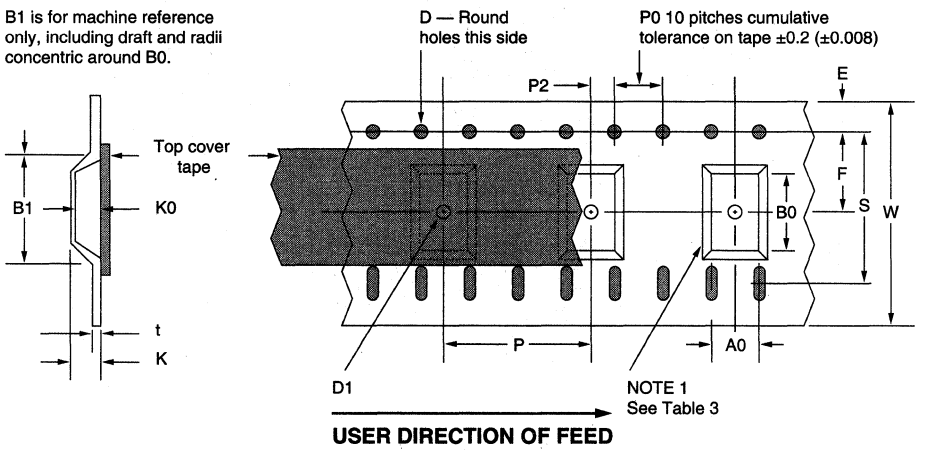


Figure 5
EMBOSSED CARRIER DIMENSIONS
(32 and 44mm tape only)

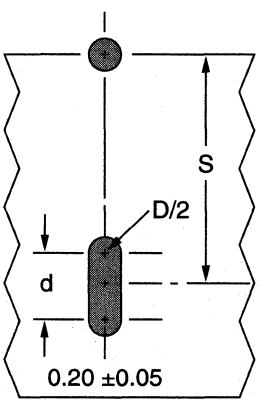


Figure 6
DETAIL ELONGATED HOLE

Table 3
32 AND 44mm EMBOSSED TAPE [3]

TAPE SIZE	D	D1 (MIN)	E	K (MAX)	P0	t (MAX)	A0, B0, K0
32 and 44mm	$1.5^{+0.10}_{+0.00}$ $(0.059)^{+0.004}_{+0.000}$	2 (0.079)	1.75 ±0.10 (0.069 ±0.004)	10 (0.394)	4 ±0.10 (0.156 ±0.004)	0.500 (0.20)	NOTE 1

TAPE SIZE	B1 (MAX)	F	P2	S	W	R (MIN)
32mm	23 (0.906)	14.2 ±0.10 (0.559 ±0.004)	2 ±0.10 (0.079 ±0.004)	28.4 ±0.10 (1.118 ±0.004)	32 ±0.30 (1.26 ±0.012)	50 (1.973)
44mm	35 (1.378)	20.2 ±0.15 (0.795 ±0.006)	2 ±0.15 (0.079 ±0.006)	40.4 ±0.10 (1.591 ±0.004)	44.8 ±0.30 (1.732 ±0.12)	50 (1.973)

TAPE SIZE	P							
	16 ±0.10 (0.630 ±0.004)	20 ±0.10 (0.787 ±0.004)	24 ±0.10 (0.945 ±0.004)	28 ±0.10 (1.102 ±0.004)	32 ±0.10 (1.26 ±0.004)	36 ±0.10 (1.417 ±0.004)	40 ±0.10 (1.575 ±0.004)	44 ±0.10 (1.732 ±0.004)
32mm	x	x	x	x	x			
44mm			x	x	x	x	x	x

NOTE:
1. A0, B0 and K0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) MIN to 1.00 (0.039) MAX for 24mm tape. The component cannot rotate more than 20° within the determined cavity.
2. Tape and components shall pass around radius "R" without damage.
3. All dimensions in millimeters (inches).

TECHNICAL NOTE

TECHNICAL NOTE

SRAM BUS CONTENTION DESIGN CONSIDERATIONS

INTRODUCTION

High-speed SRAM memory systems normally share a common data bus with other memory devices, processors and memory management or caching devices. All of these devices are required to control the data bus at one time or another. Turning off a device that is driving the bus before a new device takes control of the bus can be a difficult design problem when these systems are operating at minimum cycle times.

When two or more devices are driving the bus at the same time, a conflict known as "bus contention" occurs. This technical note discusses bus contention design issues and points out design features of Micron's fast SRAMs that help minimize bus contention problems.

BUS CONTENTION EFFECTS

System-design problems caused by bus contention are difficult to analyze. The effects are transient, normally not longer than 5ns. The most visible result of bus contention is observed as noise on power-supply lines and data lines connecting the contending devices. While these conflicts are not destructive, they potentially reduce long-term system reliability. However, in most cases, they do not affect system performance when all the active components are MOS.

MOS devices are inherently self-current limiting. As the current through a MOS transistor increases, the transistor heats up and its gain decreases. Bipolar transistors have the opposite behavior. When a bipolar transistor's temperature

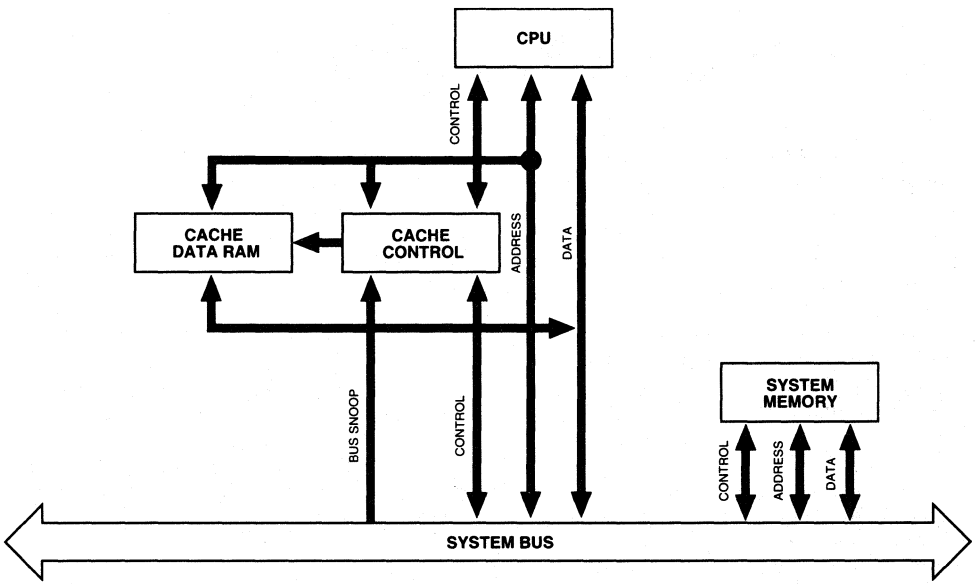


Figure 1
BLOCK DIAGRAM OF A CACHE MEMORY SYSTEM

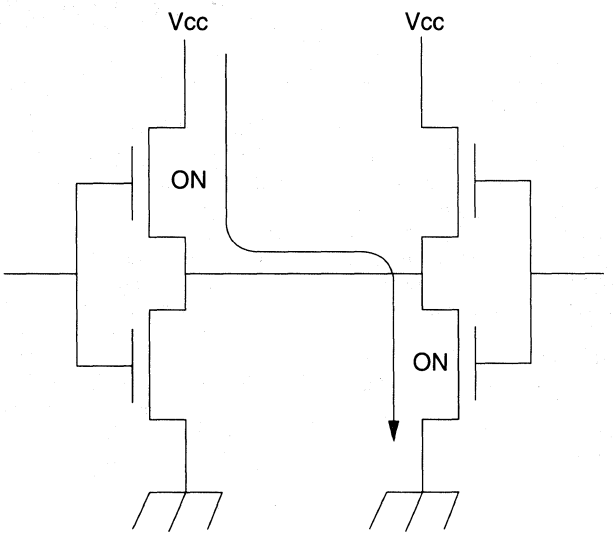


Figure 2
BUS CONTENTION CURRENT PATH

is elevated, the gain of the device increases, making it possible for the current through the transistor to increase to a destructive level. This phenomenon is known as "thermal runaway." If CMOS SRAMs share any data lines with bipolar or BiCMOS output devices, the system should be designed to eliminate any possibility of bus contention.

Figure 2 is a schematic diagram of two contending SRAM output buffers. A high current path has been created by two SRAM output buffers. The current is flowing between the "on" transistor connected to Vcc in the buffer on the left and the transistor connected to ground in the buffer on the right.

SRAM SPECIFICATIONS

The critical parameter for calculating the amount of bus contention for a high-speed SRAM system design is the time it takes for a device to go to low impedance (logic 1 or 0) on its output versus the time required for a contending output to go to high impedance. A typical SRAM has three control signals: chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$). ^tLZCE, ^tLZWE and ^tLZOE are the times it takes for the outputs to become active or low impedance upon the assertion of $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$. ^tHZCE, ^tHZWE and ^tHZOE are the times required for the outputs to become inactive or high impedance after $\overline{CE}$, $\overline{WE}$ and $\overline{OE}$ are removed. These times are shown in the READ and WRITE cycle timing diagram (Figure 3). A preliminary review of a fast SRAM data sheet would imply that the worst case for bus contention could be calculated from the equation:

$$^tC = {}^tHZ\ (MAX) - {}^tLZ\ (MIN)$$

where ^tC is equal to the bus-contention overlap time. For an output enable change in an SRAM rated at 20ns access time, ^tHZWE = 7ns and ^tLZWE = 2ns; therefore ^tC = 5ns. If this calculation is correct, there would be a serious bus contention problem. Thus, for a system running with a 20ns cycle, almost 25 percent of the total cycle would be lost to bus contention and there would be a large increase in power dissipation in the output buffers.

Fortunately, the previous analysis is not valid because ^tHZWE is a MAX parameter and ^tLZWE is a MIN parameter. ^tHZWE maximum occurs under completely different test conditions than ^tLZWE minimum. ^tHZWE maximum is worst-case at the highest operating temperature and the lowest power-supply voltage. On a commercial data sheet,

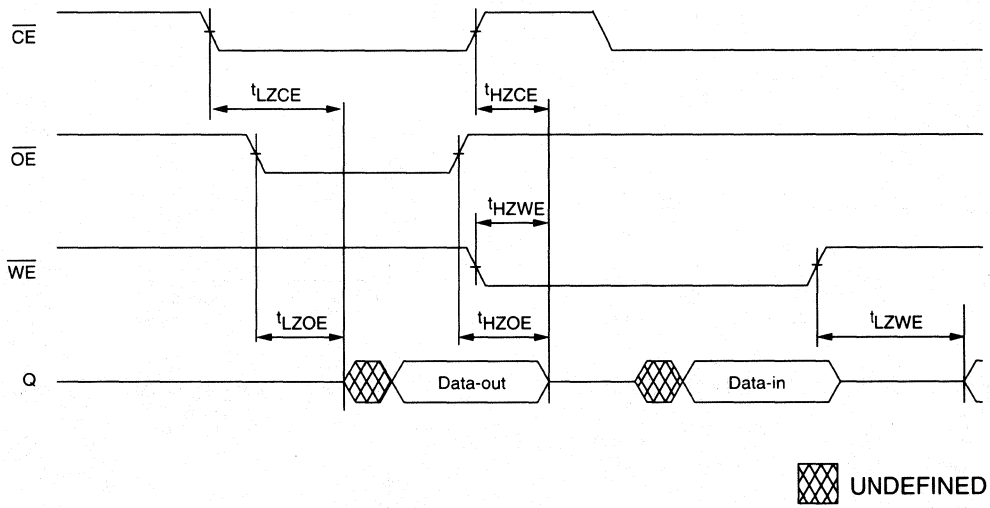


Figure 3
READ AND WRITE CYCLE TIMING

this would be at 70°C and 4.5V. ^{t}LZWE minimum is specified at the lowest operating temperature and the highest voltage. Again, on the commercial data sheet, this would be 0° C and 5.5V. It is not possible for two SRAMs on the same board to be at such diverse temperatures and voltages. Micron devices are designed to turn-off faster than they turn-on under the same voltage/temperature conditions.

This means Micron fast SRAMs have been designed so that at any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE. Since the devices will normally be mounted on the same board, the bus contention associated with the SRAM control signals has been eliminated.

Care must be taken when multiple vendors' SRAMs share the bus. An analysis of the output turn-off time must be done under the same operating and temperature conditions to insure that bus contention between the devices is minimized.

EXAMPLE DATA

As an example, Figures 4 to 9 shows actual ^{t}HZCE and ^{t}LZCE data taken from an 8ns and 10ns 64K SRAM. Note that the SRAM always turns off much faster than it turns on.

Figure 4 - 8ns 64K SRAM (0°C)

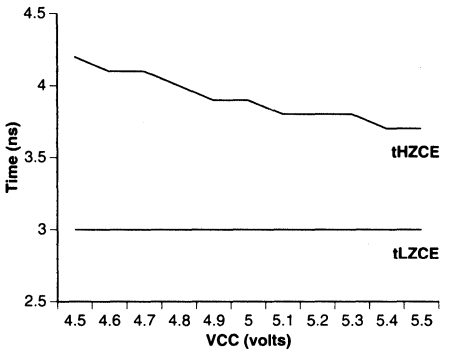


Figure 5 - 8ns 64K SRAM (25°C)

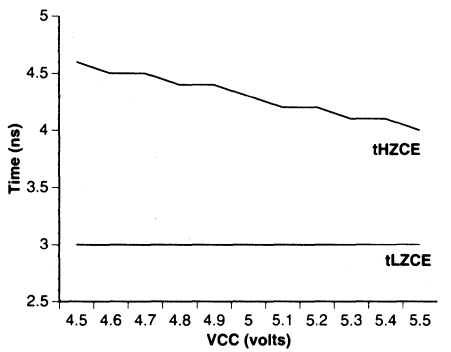


Figure 6 - 8ns 64K SRAM (70°C)

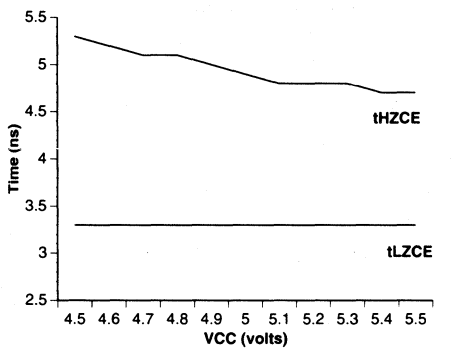


Figure 7 - 10ns 64K SRAM (0°C)

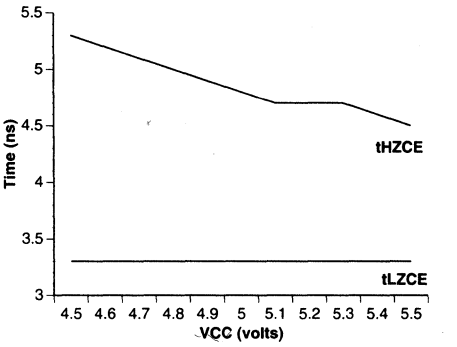


Figure 8 - 10ns 64K SRAM (25°C)

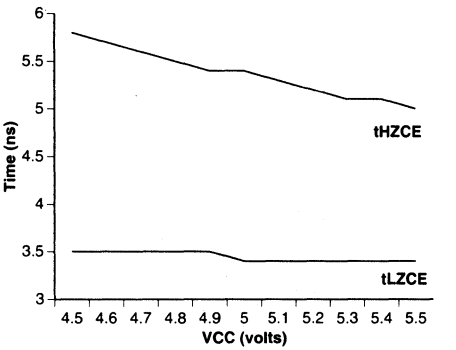
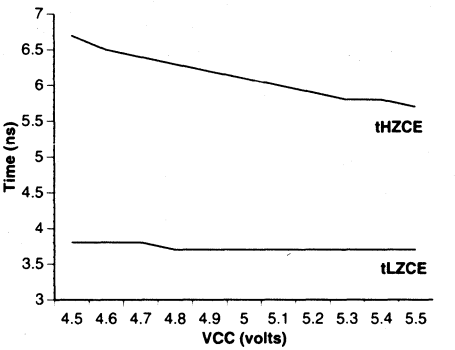


Figure 9 - 10ns 64K SRAM (70°C)



TECHNICAL NOTE

5V SRAM CAPACITIVE LOADING

INTRODUCTION

Many high-speed 16-bit and 32-bit microprocessor systems require fast SRAMs. SRAMs are used either in main memory or caching subsystems. In either case, the SRAMs are typically required to interface with a system bus that is shared by one or more microprocessors, several I/O devices and other types of memory (ROM, EPROM, etc.).

Even though transceivers and/or buffers interface with the actual bus, SRAMs are typically required to drive loads larger than what is specified in the data sheet timing parameters. Hence, the access time must be derated to reflect the actual performance of the SRAM under these circumstances.

SIMILARITY BETWEEN SRAM FAMILIES

Micron's 16K, 64K, 256K and 1 Meg 5.0V SRAM families all have the same size output transistors and output architecture. Hence, all devices will have the same drive characteristics. The actual data presented in this technical note are derived from the 256K SRAM family.

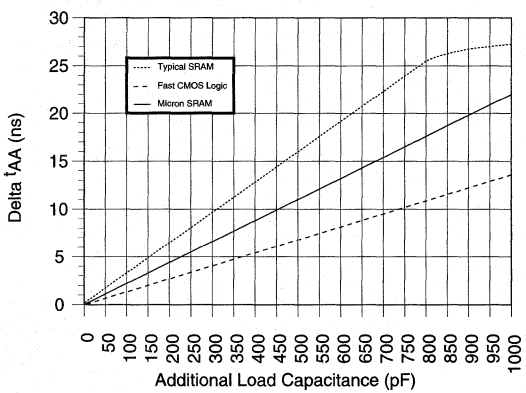


Figure 1
INCREASED ACCESS TIME vs. ADDITIONAL OUTPUT LOADING

COMPARISON OF DEVICES

Figure 1 compares the effects of capacitive loading on the Micron SRAM family with SRAMs from a typical memory supplier and discrete CMOS logic, designed to drive heavy loads. The graph illustrates the additional access time required to drive various capacitive loads.

As expected, the Micron SRAM family does not drive heavy loads as well as the discrete CMOS logic, but does drive faster than the typical SRAM from other suppliers.

The graph line representing the Micron SRAM family is based on data gathered on the Micron 256K SRAM. Access time measurements were taken with the SRAM subjected to various capacitive loads. In the range covered, the change in access time was seen to be a linear function of the capacitive load. The following equation may be used to determine the access time required for a specific load.

$$T_{AA}(\text{actual}) = T_{AA}(\text{data sheet}) + T_{AA}(\text{additional})$$

$$T_{AA}(\text{additional})\ (\text{ns}) = .022\ (\text{ns/pF})\ C_a$$

This applies where C_a is the additional capacitive load expressed in picofarads (pF). For example, the access time needed for a 100pF total capacitive load is:

T_{AA}(actual) = 20ns + T_{AA}(additional) =
20ns + .022 * (total load - rated load) =
20ns + .022ns/pF * (100pF - 30pF) =
20ns + 1.5ns = 21.5ns

SUMMARY

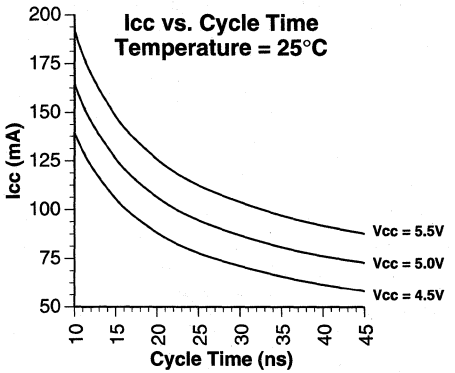
The SRAM timing specifications of all major vendors are based upon an industry standard capacitive load of 30pF. In many applications, the SRAMs are required to drive much larger capacitive loads. In addition, today's designs are implemented around higher frequencies. This requires the system timing to be more precise; hence, loading becomes a more important issue. Understanding how the SRAM will perform under specific loading conditions may result in a more reliable design.

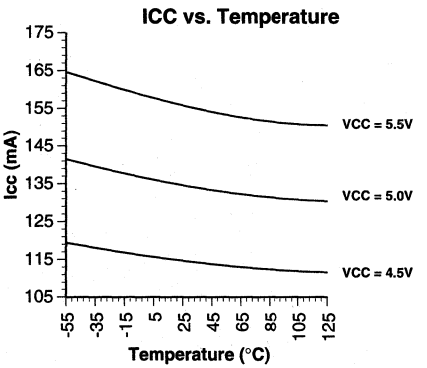
TECHNICAL NOTE

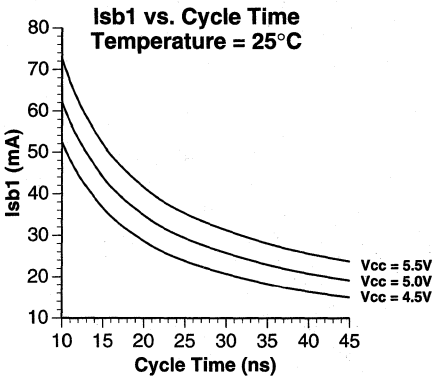
1 MEG EVOLUTIONARY PINOUT SRAM TYPICAL (5V) OPERATING CURVES

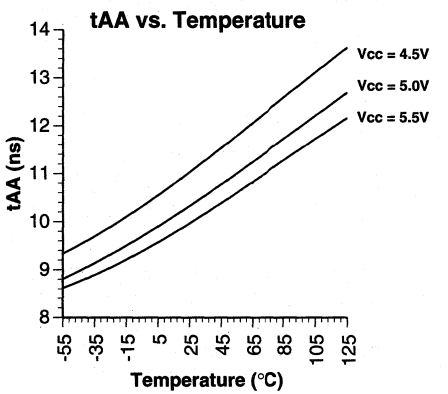
INTRODUCTION

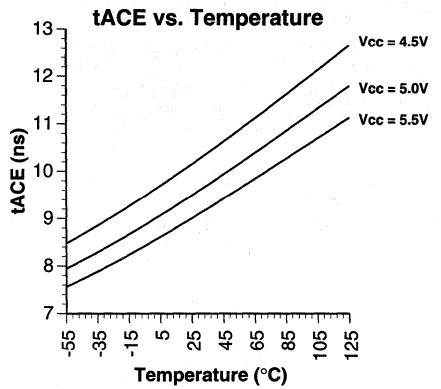
These curves represent the typical operating characteristics of Micron's 1 Meg, 15ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.

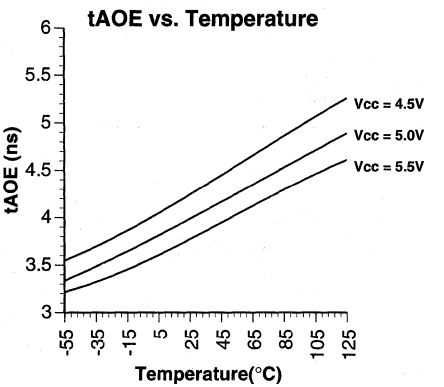


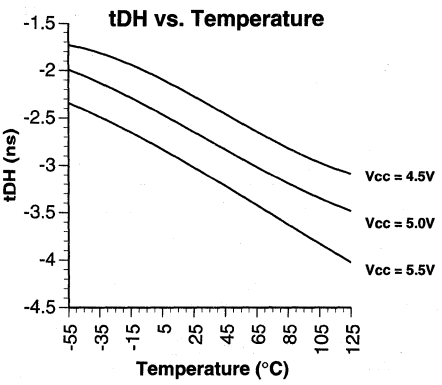


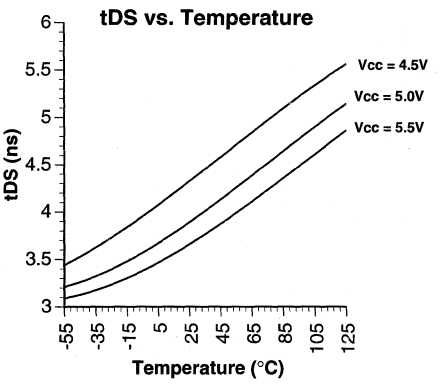


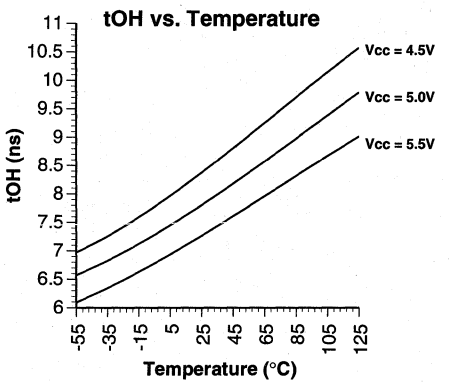


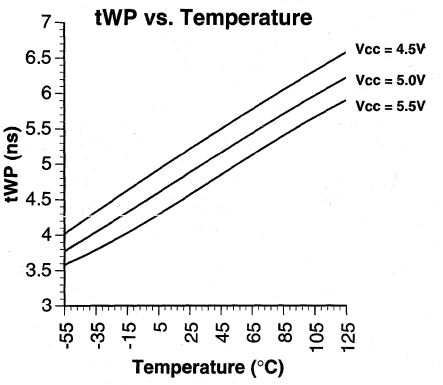










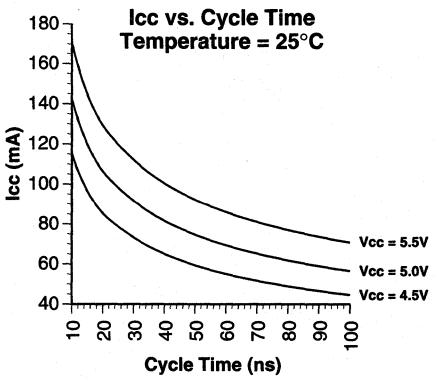


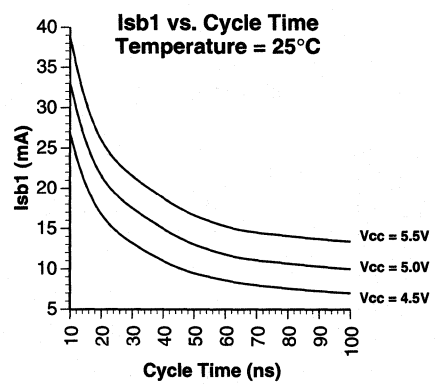
TECHNICAL NOTE

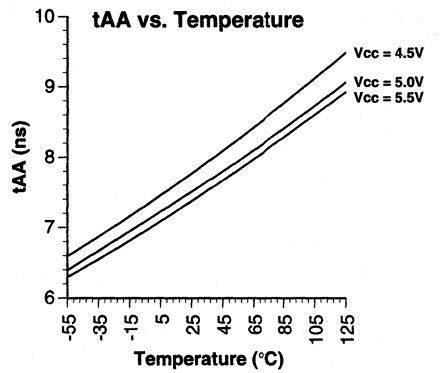
256K SRAM TYPICAL (5V) OPERATING CURVES

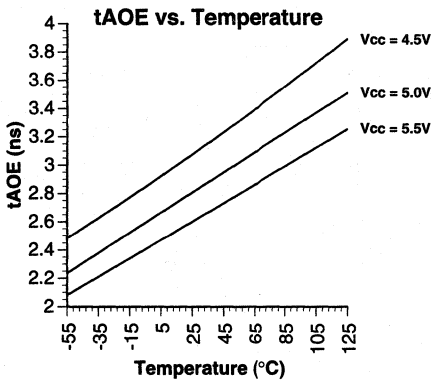
INTRODUCTION

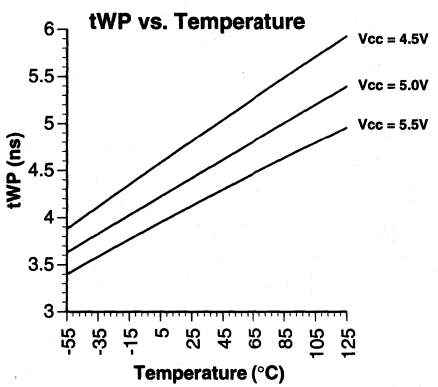
These curves represent the typical operating characteristics of Micron's 256K, 12ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.



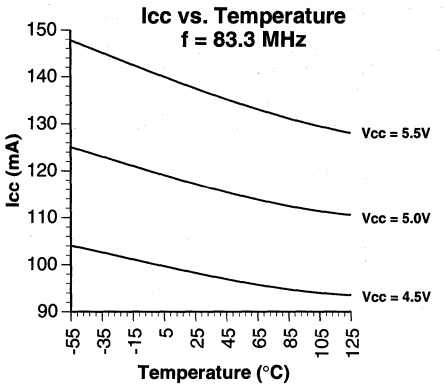


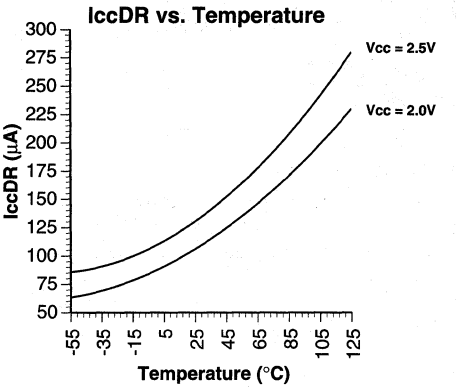


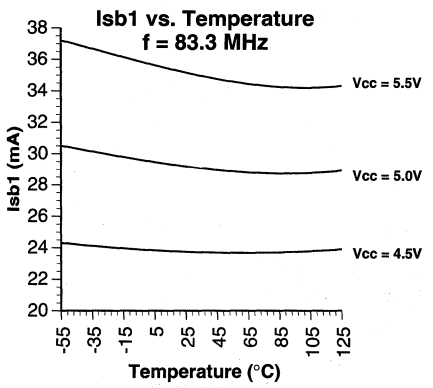


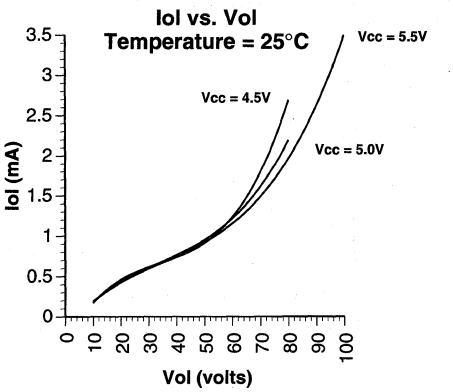


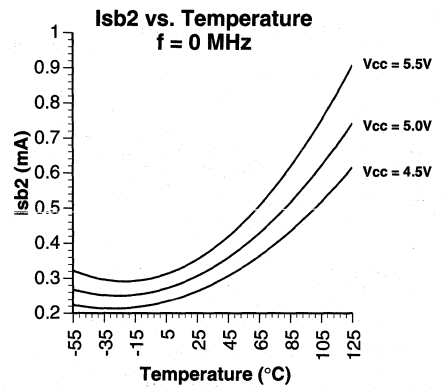
TECHNICAL NOTE

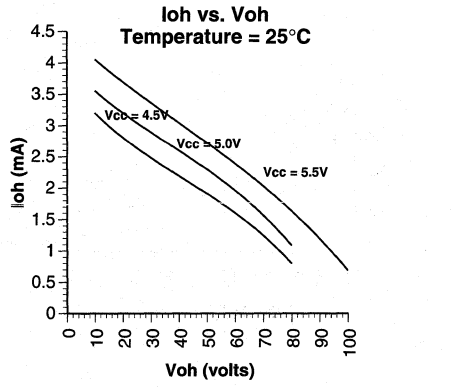












TECHNICAL NOTE

1 MEG LOW-POWER SRAMs

INTRODUCTION

By using the low-power versions of the Micron 1 Meg SRAM family (MT5C100X LP), designers can reduce both operating power consumption and battery back-up power consumption in their systems. This technical note describes the physical differences between the low-power versions and the standard versions of the 1 Meg SRAM and how these differences affect the various current consumption specifications for the devices. The note then discusses the system-level benefits of low-power parts.

LOW-POWER vs. STANDARD VERSIONS

The primary difference between the low-power versions and the standard versions of the 1 Meg SRAM is that the low-power versions contain gated inputs on the write enable ($\overline{WE}$), output enable ($\overline{OE}$) and address inputs. The difference between gated and non-gated inputs is shown in Figure 1. In the non-gated input buffer, current will flow from V_{CC} to V_{SS} when both transistors are conducting (i.e. when the input is switching or is sitting at a level between V_{CC} and V_{SS}). Current flow is at a minimum when the input is held at either the V_{CC} or V_{SS} level. In the gated input buffer, $\overline{CE}$ is an internal chip enable signal derived from the chip enable pin(s) of the device. When the chip is selected, $\overline{CE}$ is LOW, P2 is ON and N2 is OFF. Operation in this mode is similar to the non-gated input buffer. When the chip is deselected, $\overline{CE}$ is HIGH, N2 is ON and P2 is OFF. In this case, both the logical operation of the buffer and the flow-through current are independent of the voltage level at the

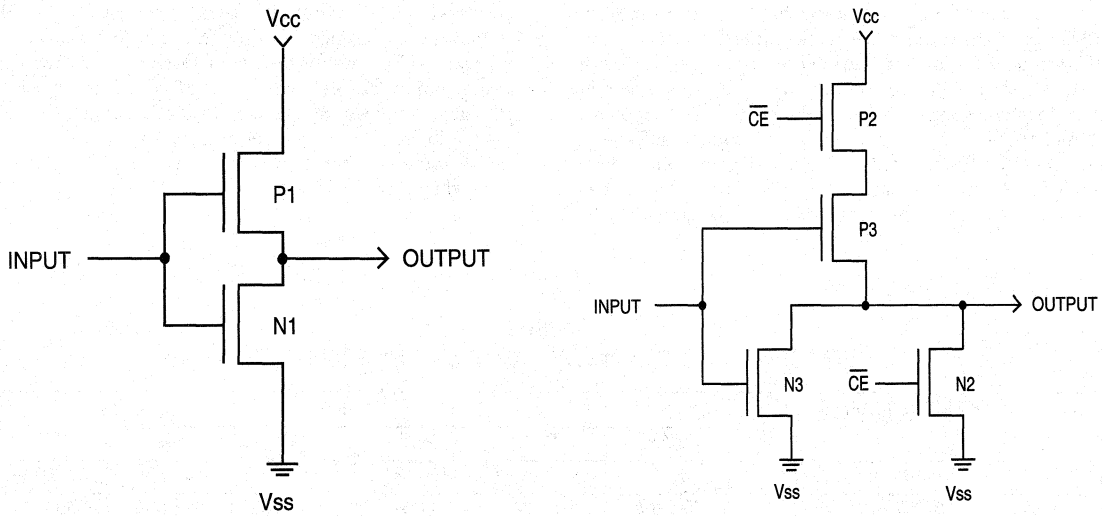


Figure 1
NON-GATED vs. GATED INPUT BUFFERS

Table 1
OPERATING AND STANDBY CURRENT DEFINITIONS

PARAMETER	MODE	CHIP ENABLE CONDITIONS	INPUT CONDITIONS
I_{CC}	Chip Selected	$\overline{CE} \le V_{IL}$	switching at MAX frequency
I_{SB1} (Standard)	Chip Deselected	$\overline{CE} \ge V_{IH}$	switching at MAX frequency
I_{SB1} (Low-Power)	Chip Deselected	$\overline{CE} \ge V_{IH}$	static or switching
I_{SB2} (Standard)	Chip Deselected	$\overline{CE} \ge (V_{CC} - 0.2V)$	static
I_{SB2} (Low-Power)	Chip Deselected	$\overline{CE} \ge (V_{CC} - 0.2V)$	static or switching

input node. The output of the buffer is LOW because N2 is ON, and virtually no current flows from V_{CC} to V_{SS}, because the gate of P2 is held at the V_{CC} level.

Another difference from the standard versions found in the low-power versions is a process enhancement designed to reduce the current consumed by the memory cells under quiescent conditions. This means that the standby current attributed to the memory array is reduced.

Specifications are summarized in Table 1 to help illustrate the effects of these differences on the various current consumption specifications of the parts. The values for these parameters are shown in Table 2. Note that I_{SB1} and I_{SB2} are substantially reduced in the low-power version while I_{CC} remains the same. The I_{SB1} (MAX) limit is reduced by 90 percent, primarily through the use of gated inputs, and the I_{SB2} (MAX) limit is reduced by 70 percent due to the process enhancements. I_{CC} is not affected by these changes because it is measured when the chip is selected and the memory array is being accessed.

Another way of looking at the effects of these changes on I_{SB1} and I_{SB2} for the low-power version is to note that the specified values for I_{SB1} approach the values for I_{SB2}. The remaining difference between the I_{SB1} and I_{SB2} values represents the amount of current consumed by the chip enable input buffers themselves. By definition, I_{SB1} is measured with the chip enable inputs at V_{IH} (MIN) or V_{IL} (MAX) levels. This causes more current to flow than if the inputs were within 0.2 volts of V_{CC} or V_{SS} levels, as is the case when measuring I_{SB2}.

Table 2
OPERATING AND STANDBY CURRENT SPECIFICATIONS

DEVICE VERSION	I_{CC}*		I_{SB1}		I_{SB2}	
	MAX	TYP	MAX	TYP	MAX	TYP
Standard	130 mA	107 mA	45 mA*	37 mA	5 mA	400 uA
Low-Power	130 mA	107 mA	3 mA	1.3 mA	1.5 mA	300 uA

* Specified at 40 MHz
Typical values are measured at V_{CC} = 5.0V and T_A = 25°C

SYSTEM-LEVEL BENEFITS

The system-level benefits can be seen by examining two different modes of system operation. First, consider a system containing several banks of SRAMs where, in an effort to minimize operating current, only one bank will be selected at any given time during normal operation. While the active bank is being accessed, the address and control signals being switched appear on the inputs of SRAMs in all banks. This causes current consumption by input buffers in standard parts. When using low-power parts, the power consumption in the deselected banks will be reduced to one-tenth of the value for standard parts. This reduces the overall operating power consumption of the system. Next, consider a system with a battery back-up mode requiring data retention in the SRAMs while the devices that interface with the SRAMs are completely powered down. In addition to a 70 percent reduction in battery back-up power consumption, the low-power SRAMs facilitate the system design. When using standard devices, designers must take precautions to ensure that all the address and control inputs are taken to within 0.2 volts of V_{CC} or V_{SS}, while taking care to avoid powering-up other devices in the system. With the low-power devices, only the chip enable inputs need to be taken to these levels—the $\overline{WE}$, $\overline{OE}$ and address inputs may then be driven to, or allowed to assume, any value between V_{CC} and V_{SS}.

SUMMARY

The low-power versions of the Micron 1 Meg SRAMs offer a 90 percent reduction in TTL standby current and a 70 percent reduction in CMOS standby current. These reductions in component standby current lead to reductions in both operating power and battery back-up power consumption at the system level, while at the same time facilitating system design.

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SRAM THERMAL DESIGN CONSIDERATIONS

INTRODUCTION

As operating frequencies increase, memory components must dissipate more power to satisfy the needed reduction in permissible access time. SRAM thermal design considerations become increasingly important as power consumption approaches the package power dissipation limit. This technical note separately addresses thermal performance of Micron packaged SRAMs and SRAM die. Contact the factory for thermal information on any package not listed in this note.

DEFINITIONS

T_A = ambient air temperature (°C) at which the device is operated. The ambient temperature range of a device is listed under the "Electrical Characteristics and Recommended DC Operating Conditions" section of each SRAM data sheet. Commercial temperature range is 0°C to 70°C, industrial temperature range is -40°C to 85°C, automotive temperature range is -40°C to 125°C and extended and military temperature range is -55°C to 125°C.

T_C = case temperature of the device (°C). In a packaged part this is the surface temperature at a point on the device package.

T_J = junction temperature of the active portion of the silicon die (°C). The maximum recommended junction temperature of Micron SRAMs is 150°C to achieve good long-term reliability. All Micron SRAMs are tested for high temperature operating life (HTOL) at 125°C ambient and 6V. Under HTOL conditions, the failure rate of a 1 Meg SRAM is 484 FITs compared with 5 FITs at 50°C ambient and 5V. The device will operate with junction temperatures in excess of 150°C but much higher failure rates should be expected. Since the limiting factor in plastic components is the plastic mold compound, 155°C should never be exceeded anywhere in the plastic body.

P = average device power dissipation. Device power is dependent upon the operating conditions. SRAM data sheets indicate maximum Icc values that incorporate significant guardband (margin to guard against process changes, tester skew, etc.). Device power should be calculated to reflect the actual junction temperature, supply voltage, operating frequency and output loading conditions.

θ_{JC} = junction to case thermal resistance (°C/W). In a die-level product, the case is considered to be the surface of the die which is bonded to the hybrid substrate. θ_{JC} is a function of the die thickness, area, and number of bonds. In a packaged component, θ_{JC} is larger due to the extra thermal resistance of the package material thickness.

θ_{CA} = case to ambient thermal resistance (°C/W). In a die-level product, this is comprised of the θ_{CA} of the hybrid substrate plus packaging around the substrate if applicable. In a packaged component, this is a function of the surface area of the component (for convection and radiation) and the amount of heat conduction through the device leads. In applications where a heat sink is attached to the device, θ_{CA} is expressed as $\theta_{CS} + \theta_{SA}$ where θ_{CS} is the case to heat sink thermal resistance and θ_{SA} is the heat sink to ambient thermal resistance. θ_{CS} is normally very small, typically 0.3° C/W. θ_{SA} is mostly dependent upon the surface area of the heat sink. Under most circumstances, Micron SRAMs do not require heat sinks for reliable long-term operation.

θ_{JA} = junction to ambient thermal resistance. This is the sum of $\theta_{JC} + \theta_{CA}$.

Given the above parameters, T_J may be calculated using the following equation:

$$T_J = T_A + P(\theta_{JC} + \theta_{CA})$$
$$= T_A + P\theta_{JA}.$$

DETERMINING THERMAL RESISTANCES

The reliability monitors published for each component family details the procedure used to determine thermal impedances. The procedure is summarized as follows: θ_{JC} is determined by inserting the IC package into a socket assembly with a thermocouple glued to the top side of the package to measure the case temperature. The contact area is minimized so that the thermocouple does not act as a significant additional heat sink. θ_{JA} is measured with the IC package inserted into the same socket assembly but suspended inside a one-cubic-foot closed container that provides a still-air environment. The junction temperature

is measured by characterizing the IC's input pin to substrate diode at various temperatures. θ_{JA} and θ_{JC} are determined using linear regression analysis on the data gathered. Characterization data generally indicates a 99.0% correlation to a linear curve fit.

The above discussion accounts for the determination of packaged component thermal properties. In actual applications, θ_{JA} is lower because printed circuit board traces conduct heat away from the package more efficiently than the test socket. θ_{JC} is essentially a constant, therefore the user may determine the actual θ_{JA} by calculating θ_{CA}. This can be done by measuring the average device power, ambient air temperature and package surface temperature of the SRAM soldered in circuit and calculating as follows:

$$\theta_{CA} = (T_C - T_A)/P.$$

θ_{JA} is simply the sum of the calculated θ_{CA} and the supplied θ_{JC}.

Table 1 summarizes the thermal resistances of Micron plastic package SRAMs rounded to two significant figures.

Table 1
PLASTIC SRAM THERMAL RESISTANCE

Device	Package Pins	Width (mils)	Type	θ_{JC} °C/W	θ_{CA} °C/W	θ_{JA} °C/W
256K x 1	24	300	PDIP	18	55	73
64K x 4	24	300	PDIP	18	53	71
32K x 8	28	300	PDIP	10	56	66
256K x 1	24	300	PSOJ	19	71	90
64K x 4	24	300	PSOJ	14	72	86
32K x 8	28	300	PSOJ	11	71	82
1 Meg x 1	28	400	PDIP	5.9	50	56
128K x 8	32	400	PDIP	5.3	50	56
1 Meg x 1	28	400	PSOJ	4.4	62	66
128K x 8	32	400	PSOJ	3.0	55	58
128K x 9	32	400	PSOJ	3.5	56	59
128K x 8 Revolutionary	32	400	PSOJ	2	48	50
64K x 16 Revolutionary	44	400	PSOJ	2	48	50
64K x 18 Synchronous	52	—	PLCC	15	30	45
32K x 36 Synchronous	100	—	TQFP	6	59	65

TRUE SRAM POWER

SRAM power is determined by accounting for three components: power dissipation of internal operations, power dissipation due to transient output current (AC load current) and power dissipation due to steady state output current (DC load current). Data sheets generally contain worst-case numbers which, for I_{CC}, occur at the fastest cycle time, coldest ambient temperature and highest voltage. Device data for specific operating voltages, temperatures and frequencies can be obtained from Micron, generally in the Reliability Monitors.

The following is a derivation from first principles, hopefully putting the issue to rest concerning how to calculate the extra power due to AC output load current:

$$P_L = \frac{1}{T}\int_0^T v\,i\,dt.$$

$$P_L = \frac{1}{T}\int_0^T (Vcc - V_L)\,I_L\,dt \text{ for LOW to HIGH case.}$$

$$P_L = \frac{1}{T}\int_0^T (V_L)\,I_L\,dt \text{ for HIGH to LOW case.}$$

Solving for the LOW to HIGH case (substituting $I_L = C\frac{dV_L}{dt}$):

$$P_L = \frac{1}{T}\int_{VOL}^{VOH} (Vcc - V_L)\,C_L\,dV_L$$

$$= \frac{C_L}{T}\left(Vcc\,V_L - 0.5\,V_L^2\right)\Big|_{VOL}^{VOH}$$

$$= \frac{C_L}{T}\left(Vcc\,[VOH - VOL] - 0.5\,[VOH^2 - VOL^2]\right).$$

Solving for the HIGH to LOW case:

$$P_L = \frac{1}{T}\int_{VOL}^{VOH} V_L\,C_L\,dV_L$$

$$= \frac{C_L}{T}\left(0.5\,V_L^2\right)\Big|_{VOL}^{VOH}$$

$$= \frac{C_L}{T}\left(0.5\,[VOH^2 - VOL^2]\right)$$

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where: C_L is the load capacitance.
V_{OH} is the highest load voltage during the cycle.
V_{OL} is the lowest load voltage during the cycle.
I_L is the load current resulting from C_L.
T is the device cycle time.
P_L is the power dissipation in the SRAM due to the output current on one DQ line.

These solutions make one important assumption: the output voltage waveform has no overshoot/undershoot. The presence of either overshoot or undershoot increases the SRAM power dissipation. True SRAM power for Micron synchronous devices is therefore:

$$P = Vcc\ I_{CC} + \Sigma\ P_{L\ (\text{for all output changes})}.$$

The marginal power due to steady-state current flow into or out of the DQ pins (due to I/O leakage of connected devices) is ignored in the above equation because it is insignificant in most new design work. That extra power would be:

$$(Vcc - V_{OH})\ I_O\ N_H + V_{OL}\ I_I\ N_L,$$

where V_{OH} is the logic HIGH output voltage, I_O is output current on those DQ lines and N_H is the number of DQ lines that are HIGH; V_{OL} is the actual logic LOW voltage, I_I is the resulting input current into the DQ line and N_L is the number of DQ lines that are LOW. Almost all CMOS devices have I_I or I_O less than 10uA (often 1 or 2uA), hence this calculation is inconsequential. If devices with high input currents are connected to the DQ lines, do not ignore this additional power component. For example, take the case where eight outputs are connected to loads having 10uA of leakage. The contribution to device power is (given that V_{OH} is 3.8V during the average cycle):

$$(5V - 3.8V)\ 10uA\ (8) = 96uW,$$

which can indeed be ignored. With higher leakage, V_{OH} drops and power increases as a result of both increased current and greater voltage drop in the SRAM output driver.

DESIGN EXAMPLE

Use of thermal resistance information can be seen in the following example: An MT5C128K8A1-20 SRAM operates at an ambient temperature of 70°C with a 5.5V supply, READ and WRITE cycle times of 25ns (40 MHz), continuous operation in still-air and an output loading of 50pF. The following discussion demonstrates how this thermal resistance information is utilized.

In the 1 Meg Evolutionary Pinout SRAM *Internal Qualification* document, the typical device current at 25ns cycle time, 5.5V and 100°C is 145mA. The power is calculated as follows (assuming the worst case, all outputs switch from LOW to HIGH):

$$P = I_{CC}\ Vcc + \frac{C_L}{T}(Vcc\ [V_{OH} - V_{OL}] - 0.5\ [V_{OH}^2 - V_{OL}^2])\ x\ 8$$

$$= 0.145(5.5) + \frac{50E\text{-}12}{25E\text{-}9}(5.5[4.3\text{-}0.1] - 0.5\ [4.3^2 - 0.1^2])\ 8$$

$$= 0.798 + 0.222$$

$$= 1.02 \text{ watts.}$$

The V_{OH} used (4.3V) is typical for operation at 5.5V. At 5V and full speed operation, V_{OH} is approximately 3.8V. V_{OL} is typically between 0.1 and 0V.

Given the true operating power of 0.803W, the case and junction temperatures can be predicted as follows:

$$T_C = T_A + P\theta_{CA}$$
$$= 70 + 1.02 \times 34$$
$$= 104.7°C.$$
$$T_J = T_A + P\theta_{JA}$$
$$= 70 + 1.02 \times 40$$
$$= 110.8°C.$$

The calculated junction temperature is below the 150°C recommended limit demonstrating that the operating conditions are acceptable. As previously mentioned, the actual θ_{CA} is lower when the SRAM is soldered in circuit. One can therefore expect lower case temperatures than calculated in this example.

To illustrate this point, the MT58LC32K36LG synchronous SRAM was characterized in both still air and circuit. In still air, θ_{JA} was determined to be 39°C/W maximum. θ_{JC} was determined to be 5°C/W maximum. In circuit (4.340 x 1.150 in^2 circuit board with 1 power and 1 ground plane), θ_{JA} was found to drop to 20°C/W and θ_{JC} to1°C/W. This implies that θ_{CA} dropped from 34 to 19°C/W (since $\theta_{CA} = \theta_{JA} - \theta_{JC}$) as a result of the additional conduction through the device leads and the circuit board traces.

IMPROVING THERMAL PERFORMANCE

The motivation for achieving the lowest possible junction temperatures is twofold: most AC timing parameters change adversely as junction temperature increases. This can be seen in any of the SRAM reliability monitors where AC timing specifications versus temperature are plotted. Another consideration is that component life decreases

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exponentially as temperature increases. Component life shows a strong correlation to the following equation:

$$t_O = t_N \exp([Ea/k][1/T_O - 1/T_N]),$$

where: t_O is the mean time to failure under the stress operating condition.
t_N is the mean time to failure under normal operating conditions.
Ea is the activation energy of failure modes, the most common one being dielectric defects, 0.3eV.
k is Boltzmann's constant, 8.617×10^{-5} eV/K.
T_N is the normal operating temperature (Kelvin).
T_O is the stress operating temperature (Kelvin).

Several considerations can improve thermal performance. Ground and power planes on a PCB can have a significant effect on conduction and therefore on power dissipation and safe operating temperatures. More power and ground leads on the device package produce greater relief. The addition of a thermal pad under the device with appropriate thermal bonding will also help conduct heat away from the device.

Air flow has a significant effect in reducing component temperatures. Table 3 shows test results for industry standard packages, demonstrating the effective reduction in θ_{CA} as airflow increases (these results have *not* been verified by Micron). For example, a 1 Meg SRAM in plastic SOJ having θ_{CA} of 48°C/W in still air would have a θ_{CA} of approximately 48°C/W x 0.75 or 36°C/W at 200fpm of air flow. The new θ_{JA} is approximately 36 + 2.0 = 38°C/W.

DIE THERMAL CONSIDERATIONS

Die level thermal considerations are more complex for the user to handle because more factors are involved than with factory packaged components. Figure 1 illustrates the thermal interfaces involved in a die application with ceramic substrate. Typical thermal resistances which need to be quantified are: die to adhesive, adhesive to substrate, substrate to lid, lid and/or substrate to ambient. The path is highly dependent upon the multichip module (MCM) construction. Heat radiation from die to lid could be an applicable factor. Thermal vias below the die would significantly reduce the total package thermal resistance and should be modeled appropriately.

An application which uses a ceramic substrate can use the

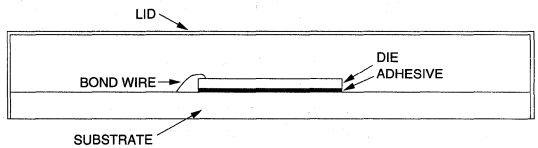

Figure 1
DIE APPLICATION

θ_{JC} values provided for ceramic SRAMs as a conservative value. This accounts for thermal resistances from die to adhesive (assuming gold eutectic in ceramic packaged parts), adhesive to substrate, and also accounts for the effects of the bond wires. The value is conservative because the thermal resistance through the substrate material of Figure 1 is included, whereas this portion is actually unique to the substrate of each user. Without adjustment, this would be double-counting a portion of the thermal resistance.

Figure 2 illustrates the thermal resistances in a typical die application on silicon substrate. The following discussion uses a silicon substrate die application with four Micron 1 Meg SRAM die mounted on the substrate. The die areas for various Micron SRAM die products are listed in Table 4. Thermal resistance from junction to die backside for the 1 Meg SRAM (S18A) is calculated as follows:

θ = (0.0185 inch die thickness)/(2.23W/°C/inch)
/ (0.107 sq. inches die area)
= 0.08°C/W.

The remaining thermal resistance values are user-dependent and also dependent upon contact area. Some typical values are: 0.06°C cm^2/W for the die to silicon substrate interface, 0.2°C cm^2/W through the silicon substrate, 0.7°C cm^2/W silicon substrate to module carrier, 0.6°C cm^2/W through the aluminum module carrier, 0.7°C cm^2/W from module carrier to heat sink and 30°C cm^2/W

Table 3
EFFECTS OF AIRFLOW ON θ_{CA}

Package	Air Flow	θ_{CA} Multiplier
PDIP	200 fpm	0.7 - 0.75
PSOJ	200 fpm	0.7 - 0.75
PDIP	500 fpm	0.55 - 0.65
PSOJ	500 fpm	0.55 - 0.65

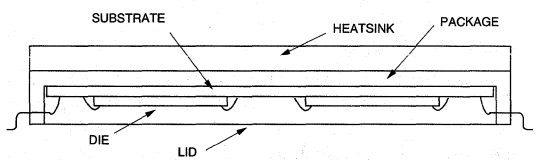

Figure 2
SILICON SUBSTRATE DIE APPLICATION

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from heat sink to ambient. For an MCM with 4 SRAMs dissipating the 1.02W of the previous example with 3cm x 3cm dimensions, the calculations would be as follows (assuming 70°C ambient is in still air):

$T_{heat\ sink}$ = 70°C + (30°C/W/9cm^2) x 1.02W x 4
= 83.6°C.

$T_{module\ carrier}$ = 83.6°C + (0.6 + 0.7°C cm^2/W)/9cm^2 x 1.02W x 4
= 84.19°C.

$T_{silicon\ substrate}$ = 84.19°C + (0.2+0.7°C cm^2/W)/9cm^2 x 1.02W x 4
= 84.60°C.

$T_{junction}$ = 84.60°C + (0.06°C cm^2/W/0.691cm^2 + 0.08°C/W) x 1.02W
= 84.77°C.

This MCM type, as seen from the example, is very well suited for much higher power dissipation devices than the four SRAMs used in this example. Eliminating the heat sink would alter the analysis (using 170°C cm^2/W for the module carrier package to air thermal resistance):

$T_{module\ carrier}$ = 70°C + (0.6 + 170°C cm^2/W)/9cm^2 x 1.02W x 4
= 147.34°C.

$T_{junction}$ = 147.51°C.

The junction temperature is calculated using the same methodology as before. This indicates that a heat sink would not be necessary using the stated assumptions.

Table 4
MICRON DIE INFORMATION

Configuration	Data Base	Dimensions (mils)	Area cm^2	θ^1 °C/W
32K x 8	S06	167 x 346	0.373	0.144
128K x 8	S01	241 x 544	0.846	0.063
128K x 8	S18A	210 x 510	0.691	0.078

NOTE: 1. This is the thermal resistance from junction to die backside (calculated value).

SUMMARY

Thermal analysis and design have become an important consideration in SRAM applications. The benefit to the end user when these considerations are properly accounted for is higher system reliability due to longer component life. For the designer, thermal design techniques result in knowledge of device junction temperatures over the operating temperature range, which directly leads to an understanding of device characteristics under the varying operating conditions. In die applications, thermal considerations are an essential part of the design task. Analysis tools based on finite element and finite difference techniques are frequently used to predict temperatures throughout MCM assemblies. Tables included in this note provide thermal resistance values which are useful in analyzing both die and packaged component applications.

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A DESIGNER'S GUIDE TO 3.3V SRAMs

INTRODUCTION

The challenge of reducing power consumption is critical in laptop, notebook and palmtop computers, and is a growing factor in desktop and workstation applications. A key solution to reducing power is the use of 3.3 volt components in system designs. Although battery life is the dominant issue in most portable designs, other issues such as the migration of high-performance microprocessors to 3.3V and technology requirements to produce memory components, especially in DRAMs, are forcing the transition to 3.3V. Even the Environmental Protection Agency (EPA) is getting into the act by mandating power reduction for all computers purchased by the federal government.

This paper discusses the main reasons propelling system designers to use 3.3V logic, how Micron SRAMs are constructed for 3.3V operation, and issues specific to designing mixed 3.3V and 5V systems. Because not all components are currently available at 3.3V, it is especially important for designers to understand how to incorporate these lower voltage parts in robust, reliable system designs.

REASONS FOR 3.3V LOGIC

Several issues are accelerating the use of 3.3V components in computer systems. Although reduction of system power is the primary reason, other considerations form a powerful argument for converting new designs to 3.3V. This section details the main reasons and advantages.

REDUCING SYSTEM POWER AND EXTENDING BATTERY LIFE

Extending battery life and reducing the size and weight of the battery pack are two key design concerns. Many current laptop and notebook designs run out of power in one to two hours, forcing the user to recharge batteries frequently or carry spare battery packs. The long-term goal of portable computers is to provide desktop-equivalent performance, extended battery life (8 to 10 hours or more) and drastically reduced battery weight (perhaps as few as two AA cells).

Current techniques to reduce power rely on enhanced power-management modes implemented in memory controllers, or in the processor itself. Other savings in power have come about through the use of low-power components such as Extended Refresh or SELF REFRESH DRAMs. These methods have decreased power, but fail to achieve desired performance and battery life levels. These goals

Table 1
A COMPARISON OF 3.3V AND 5V MEMORY POWER DISSIPATION

Manufacturer	Part Type	Power Mode	5V Power (MAX mW)	3.3V Power (MAX mW)	% Savings 3.3V vs. 5V
SRAMs					
Micron	256K, x8, 20ns	Operating	715	324	54
		CMOS Standby	28	10	64
IDT	256K, x8, 20ns	Operating	798	378	52
		CMOS Standby	83	1.8	97
DRAMs					
Micron	4 Meg, x4, 80ns	Operating	495	180	44
		BBU*	1.65	.324	80
NEC	4 Meg, x4, 80ns	Operating	495	216	56
		SELF REFRESH	0.72	0.36	50
MICROPROCESSORS					
TI	DSP TMS320C5x	Typical Operating	13.8mW per MIPS	5.4mW per MIPS	61
Motorola	DSP56L002	Operating 40 MHz	500	165	67

* BATTERY BACKUP current. This represents the DRAM operating at a $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ refresh at the slowest possible cycle time.

can be realized only through the use of lower voltage components.

To show the benefits of 3.3V over 5V components, Table 1 gives a comparison of power for several products available at both voltages. Memory components (DRAMs and SRAMs) and DSP microprocessors are shown. As shown, the amount of power saved in converting to 3.3V is significant. Power savings average 63 percent, allowing the system battery life to more than double.

SUPPORTING 3.3V PROCESSORS

A number of 3.3V microprocessors and microcontrollers have appeared in the marketplace and are leading the industry into low-voltage system design. For optimal performance, minimized power and chipcount, and simplified design, these chips require lower voltage support chips and peripherals.

High-speed and high-performance designs are adopting 3.3V products as demonstrated by Intel's Pentium™, IBM and Motorola's PowerPC™, Digital's Alpha AXP chip and Silicon Graphics' MIPS R4400. One of the main reasons these products have moved to 3.3V is to reduce the power dissipated by the high-frequency processor chips. At 5V, Intel's Pentium chip draws some 17 watts at 66 MHz. The problems of dissipating this power should force Intel to move quickly to a reduced-voltage part. Even though Digital's 21064 Alpha chip already operates at 3.3V, it still dissipates a whopping 23 watts at 150 MHz. Digital recently announced new versions running up to 200 MHz with plans to move to 300 MHz in the next several years. These processors must move to 3.3V (or lower) due to high transistor count and high-frequency operation. The lower voltage helps reduce or eliminate external cooling components such as heatsinks or fans.

At the lower end of the scale, portable applications are using 3.3V microprocessors to reduce system power and extend battery life. A number of 3.3V microprocessors have appeared for use in portable applications such as personal digital assistants (PDAs) and notebook computers. Digital signal processors such as TI's TMS320C5x and Motorola's DSP56L002 have appeared with options to run at either 3.3V or 5V. As shown in Table 1, the TMS320C5x runs with a 62 percent reduction in power at 3.3V, while the DSP56L002 saves 67 percent.

EPA ENERGY STAR PROGRAM

According to the EPA, computer systems account for five percent of commercial electricity consumption in the United States. Left unchecked, this could grow to 10 percent by the year 2000. A large percentage of this power is consumed by unused computers left on after hours or through the weekend. During these time periods, as many as 30 to 40 percent of all computers are left on and inactive.

The goal of the Energy Star Program is to reverse the trend of increased power usage of computers, thus reducing the need to build more power plants. The primary strategy is to reduce power requirements of desktop computers that can use as much as 300 watts of power in active mode to below 150W with a standby mode power of less than 30W (not including the monitor). PCs meeting these specifications are commonly referred to as "green machines" or "green PCs."

Another incentive has been given to the computer industry by the federal government through its purchase of computer products. All computers purchased after October 1993 by the federal government must meet these new Energy Star standards. This motivator has led to development of a number of "green PCs," with an increasing number running at 3.3V.

RELIABILITY

Because 3.3V logic reduces power consumption, devices run cooler than their higher voltage counterparts, and junction temperatures are reduced. Reliability is exponentially related to junction temperature, and a reduction in junction temperature increases the long-term reliability of the component. Reduced voltage levels mean less stress is placed on the dielectrics. Because Micron's SRAM inputs are tolerant to 5V inputs (+6V MAX), potential problems with damaging input voltage levels in mixed-voltage systems are considerably reduced.

Reliability improvements also extend to the system level since 3.3V components generate less noise due to their reduced power levels. This reduced power leads to a minimization in the number of components for cooling, thus reducing system size.

TECHNOLOGY ISSUES

As DRAM technology moves to 0.55µm and smaller, the voltage level has to be reduced. Current 16 Meg DRAMs are manufactured with 5V periphery logic and I/O using an internally generated 3.3V power supply for the memory array. These parts interface with the external world using industry-standard 5V I/O levels while maintaining the benefits of lower voltage for the internal array. Next generation 16 Meg DRAMs will have versions operating externally at 3.3V, while all 64 Meg DRAMs will operate exclusively at the 3.3V level.

The main motivation for DRAM conversion to 3.3V has been to reduce power in the DRAM device. However, at the transistor level, several technical factors are also making 3.3V a desired standard. As DRAM technology moves

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toward thinner oxides, and 0.55µm (and finer) design rules are used to shrink transistor dimensions, applying 5V across the transistor degrades both performance and reliability. The move to 3.3V allows reliable transistor performance down to channel lengths of 0.4µm before requiring further voltage reduction.

3.3V SRAM MEMORIES

In the past year, several 3.3V SRAM memory components have been introduced. Initially these 3.3V SRAMs were recharacterized 5V products that usually suffered a significant speed loss and sometimes reduced noise margins when operating at 3.3V. Some estimates have shown that recharacterization slows parts by at least 50 percent. Users are unwilling to pay a performance penalty in order to extend battery life, and desire the same type of performance in a portable machine as in a desktop. This is attainable only if the lower power components can also operate at high-performance levels.

The second generation of 3.3V SRAMs takes advantage of new design techniques that optimize speed at the reduced voltage level. These speed improvements are made possible by the lower voltage, which, due to lower breakdown levels, reduces critical transistor dimensions. As lithographic techniques improve and dimensions get smaller, only lower-voltage parts can take advantage of smaller transistor dimensions. For this reason, they will eventually exceed the speed of 5V parts. The other advantage new 3.3V designs have over screened parts is that they optimize transistor threshold voltages, increasing noise margin on inputs and outputs.

The input protection circuits on Micron's 3.3V SRAMs have been designed to provide excellent immunity to electrostatic discharge (ESD). Micron's new 3.3V 256K SRAM exhibited greater than 2000V of ESD tolerance on all pins with the average pin typically having more than 6000V of tolerance. These tests were performed using the Human Body Model ESD test. Even though Micron SRAMs have excellent tolerance to ESD, it is still recommended that while handling, shipping or storing devices, appropriate ESD measures be used.

Micron 3.3V SRAMs have been designed to work in cache memory applications for high-performance systems ranging from workstations to notebooks. Micron's 3.3V SRAM product line features a wide variety of SRAMs including 256K, 1 Meg (evolutionary and revolutionary pinout) and 4 Meg versions (Table 2). These SRAMs have been designed using Micron's advanced 3.3V process technology and optimized 3.3V circuits.

One of the major advantages of these SRAMs is their ability to work in high-performance systems. Micron's 3.3V 256K SRAMs presently run as fast as 12ns and are excellent choices for cached memory systems in 3.3V desktop green machine or notebook design. While these 3.3V SRAMs provide the power savings that portable applications require, they do not have the speed penalty associated with screened 5V SRAMs.

3.3V JEDEC STANDARDS

In order to ensure conformity of 3.3V interfaces among manufacturers, the computer industry has adopted JEDEC protocol 8-1, "Interface Standard for 3.3V ±0.3V Supply Digital Integrated Circuits." The voltage requirements for this specification are shown in Table 3. All Micron 3.3V SRAMs meet or exceed this standard.

Some confusion may exist because a number of ICs operate with a wide voltage supply range of 2.7 to 5.5V. This voltage range has been used in some battery-powered applications where speed is not as important as battery life. These systems pay a significant penalty in speed and will

Table 2
MICRON'S 3.3V ASYNCHRONOUS FAMILY

Part Number	Configuration	Access Time	Packages
MT5LC2561	256K x 1	12, 15, 20, 25	DIP, SOJ
MT5LC1001	1 Meg x 1	20, 25, 35, 45	DIP, SOJ
MT5LC2564	64K x 4	12, 15, 20, 25	DIP, SOJ
MT5LC2565	64K x 4 $\overline{OE}$	12, 15, 20, 25	DIP, SOJ
MT5LC1005	256K x 4	20, 25, 35, 45	DIP, SOJ
MT5LC256K4D4	256K x 4	20, 25	SOJ
MT5LC1M4D4	1 Meg x 4	20, 25, 35	SOJ
MT5LC2568	32K x 8	12, 15, 20, 25	DIP, SOJ
MT5LC1008	128K x 8	20, 25, 35, 45	DIP, SOJ
MT5LC128K8D4	128K x 8	20, 25	SOJ
MT5LC512K8D4	512K x 8	20, 25, 35	SOJ
MT5LC64K16D4	64K x 16	20, 25	SOJ
MT5LC256K16D4	256K x 16	20, 25, 35	SOJ

Table 3
JEDEC STANDARD 8-1 FOR 3.3V LOGIC

DC Operating Conditions			
Parameter	**Condition**	**MIN**	**MAX**
V_{CC}	-	3.0V	3.6V
V_{OH}	-2mA	2.4V	-
V_{OL}	2mA	-	0.4V
V_{IH}	-	2.0V	Vcc + 0.3V
V_{IL}	-	-0.3V	0.8V
Absolute Maximum Conditions			
V_{CC}	-	0.5V	4.6V
V_{IN}	-	0.5V	Vcc + 0.5V (4.6V MAX)

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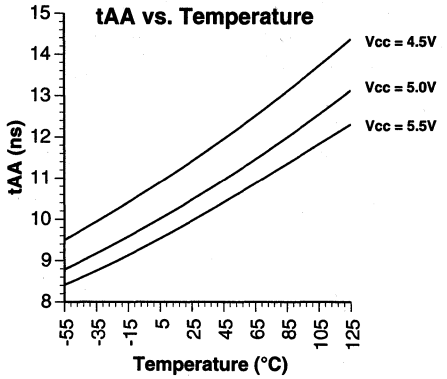

Figure 1
ACCESS TIME vs. TEMPERATURE AND VOLTAGE

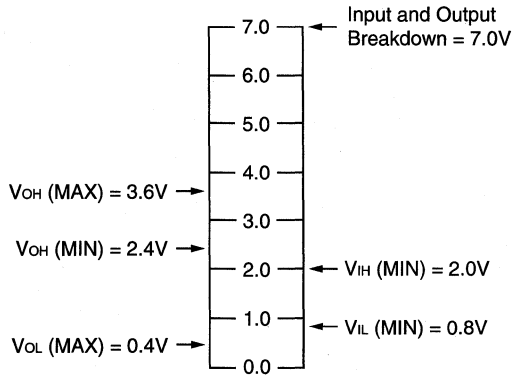

Figure 2
3.3V DEVICES DRIVING 5V LOGIC

not be used when performance is an issue. Designers refer to these systems as unregulated because the wide voltage range means they can be designed without voltage regulators.

High-speed systems use microprocessors running with a much tighter tolerance with Vcc of 5V ±5% or 3.3V ±0.15V to provide higher performance. The voltage supply of the microprocessor is usually shared with the cache memory and hence the SRAM speed can also benefit from the increased timing margins due to only a five percent variance.

Figure 1 shows how access time varies versus temperature and voltages for the 5V 256K SRAM. A 3.3V part will exhibit similar performance characteristics. At 5V, a 10 percent tolerance on Vcc means a low Vcc of 4.5V and a five percent tolerance means a low Vcc of 4.75V. For the parts shown here, the increase in low end Vcc increases the speed of the part. This gain becomes even more important as clock speeds approach or exceed 60 MHz.

3.3V SRAMS DRIVING 5V COMPONENTS

Figure 2 shows how 3.3V output logic levels can be used to drive 5V TTL levels. These logic levels guarantee a minimum noise margin to 400mV when driving HIGH or LOW output levels and typical values provide even more margin. 5V device inputs require a minimum V_{IL} of 0.8V and 3.3V devices supply less than 0.4V. Similarly, inputs require a minimum V_{IH} of 2.0V and are supplied with 2.4V or greater.

There has been some concern that 3.3V parts driving 5V inputs will cause a slightly higher power dissipation because the inputs are not driven to a full voltage rail. But because not all 5V TTL memories drive to CMOS rails, they will have similar power dissipation on inputs.

There are no difficulties using 3.3V outputs to drive 5V TTL circuits, but they should not be used to directly drive 5V CMOS level inputs on true CMOS devices. To reach V_{IH} (MIN), 5V CMOS devices with CMOS thresholds require a greater logic-HIGH input voltage than can be supplied by 3.3V devices. Designs requiring 5V CMOS levels need a voltage translation or buffer circuit. This restriction is also present on 5V TTL outputs, but can be more easily alleviated by means of a pull-up device.

Some manufacturers specify that logic HIGH on their 3.3V High-Z outputs or bi-directional buses not exceed Vcc+0.5V. This limitation is especially critical when the outputs are connected to a bus with 5V drivers. Even a 3.3V notebook might be connected to a 5V printer or peripheral. Although the 3.3V devices can drive 5V inputs, the 5V bus may overdrive the maximum allowable voltage during High-Z. Devices with restrictive maximum voltages require some type of buffering to prevent damage to the I/O pins. This buffering may be the addition of a current limiting resistor for 3.3V components that would have excessive current through a clamping diode or a register latch buffer for those devices that suffer from latchup problem when overdriven.

An advantage of Micron 3.3V SRAMs is that these extra circuits are not required when connecting to a 5V bus. Micron SRAMs are designed to tolerate 5V signals driven directly into bi-directional or High-Z outputs. This also means our 3.3V circuits can be connected to buses using

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pull-up resistors to 5V or drivers using 5V TTL or CMOS levels. If a pull-up transistor is required on a bus, we recommend a pull-up connected to 3.3V instead of 5V. While saving power, this pull-up to 3.3V will still allow a logic HIGH on the bus when driving TTL components. This SRAM tolerance to 5V signals saves space by eliminating buffer circuits, saves power by reducing components, and prevents headaches. Figure 3 shows the various bus options that must be considered by a designer. In the figure, 3.3V circuit A requires a current limiting register to prevent destructive currents when being driven by a 5V output. 3.3V circuit B requires a buffer to prevent latchup, and Micron's 3.3V SRAM, interfaces directly to the bus.

5V COMPONENTS DRIVING 3.3V SRAMS

The JEDEC 8-1 standard specifies that 3.3V input voltages can range from -0.5V to Vcc+0.5V (4.6V [MAX]). This range was reduced by JEDEC from their original 1984 standard, which specified a maximum input voltage of 5.5V, therefore allowing 5V devices to directly drive 3.3V inputs. JEDEC modified the older standard because the transition period to 3.3V is turning out to be much shorter than originally envisioned.

Micron SRAMs are designed to surpass the 8-1 JEDEC standard by allowing an absolute maximum voltage of +6.0V on the inputs, with 5.5V as the recommended maximum DC operating condition. This allows any 5V device with either a TTL or CMOS output to directly drive the 3.3V inputs. These 5V-tolerant inputs supplant buffer logic between components with different supply voltages, thus saving power and board space and reducing complexity.

Designers need to be careful when considering 3.3V components because some do not exceed the JEDEC +4.6V MAX (V_{IN}) specification. Directly driving these 3.3V components with 5V parts will exceed this value and could cause a latchup failure. Mismatched impedances worsen the problem since ringing will occur and drive the voltages higher than their steady-state values. A number of companies including IDT, National Semiconductor, Texas Instruments and Toshiba offer buffering components specifically designed to address the buffering issues encountered in mixed-voltage systems. As 3.3V components proliferate, designers may be forced to use these buffer circuits if the 3.3V component does not offer direct 5V compatibility. Figures 4 and 5 show how to connect circuits and how the voltage levels interact when 5V components drive 3.3V circuits.

Although the minimum JEDEC standard for V_{OH} and V_{OL} specifies a current of +2mA and -2mA, Micron exceeds these standards and offers output currents identical to the

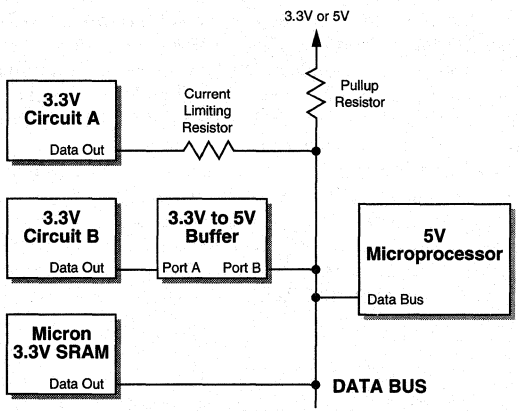

Figure 3
CONNECTING 3.3V OUTPUTS TO 5V CIRCUITS

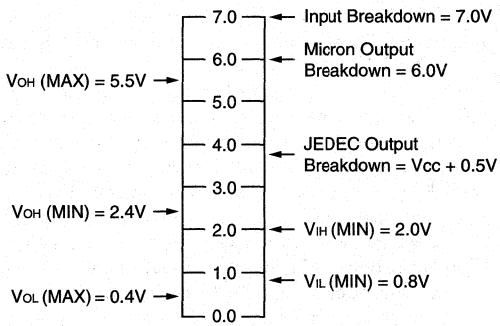

Figure 4
5V DEVICES DRIVING 3.3V LOGIC

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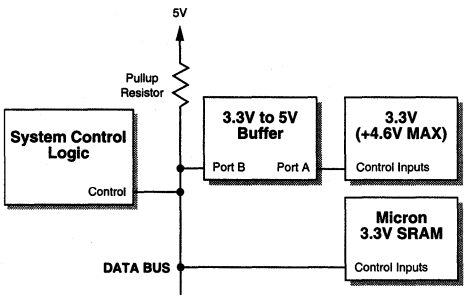


Figure 5
5V DEVICES DRIVING 3V LOGIC

5V TTL standards of +8 and -4mA. These high currents allow Micron SRAMs to attain high-speed operation.

POWER-UP DESIGN CONSIDERATIONS

Mixed-voltage designers need to be especially careful during the power-up and power-down sequence to ensure that 5V parts do not violate the input specifications of 3.3V parts. For instance, even though the 3.3V Alpha microprocessor can tolerate direct 5V inputs, according to the Hardware Reference Manual no input or bi-directional pin can rise above 4V until the 3.3V supply is stable. Failure to meet this rule can cause damage to the Alpha. This is because a 5V part could drive an input to a 3.3V part with a Vcc of 0V, exceeding breakdown voltages and permanently damaging the device.

Three solutions are available to minimize problems during power-up and power-down in mixed voltage systems. The first is to use power supply sequencing to ensure that the 3.3V power supply is stable before any 5V signals are applied. The second is to use tristate outputs to drive 3.3V logic, and ensure that all inputs remain in tristate until the 3.3V supply is stable. Power supply designs that sample the 3.3V power supply and generate a tristate signal based on it offer the safest design approach because the tristate will be removed only when power is stable.

The third solution is to use a 3.3V product without a power-up problem. Micron SRAMs have been constructed to completely eliminate such problems. They are designed so that a 5V signal can be applied to the inputs even if the 3.3V Vcc pin is between 0 and 3V. These SRAMs provide ample time for both power supplies to reach a stable state regardless of which is turned on first. A typical power supply voltage ramp-up time is between 10ms and 20ms. For long term reliability, we recommend that the input voltage does not exceed 3.3V for greater than 200ms while Vcc < 3.0V. To support a wide variety of 3.3V parts, power supplies of mixed-voltage systems should ensure a minimum delay between power-up of the 5V supply and the 3.3V supply.

POWER SUPPLY CONSIDERATIONS

Power supply manufacturers are developing a wide array of products simplifying mixed-voltage designs and power-up considerations. Power supply chips that supply multiple output voltages are now available, such as Maxim's MAX782 supply. These chips can be used to generate the voltage supplies of mixed voltage systems, and support power supply sequencing per the designer's specifications.

Some designers have not considered using a lower voltage part because a 3.3V supply is unavailable. Many expansion slots in computers only have a 5V supply available and 3.3V has to be generated on the card. A 3.3V supply can easily be generated with a voltage regulator as shown in Figure 6. Regulators are inexpensive and take up minimal area (typically < 0.4 in2). The additional power drawn by the regulator is insignificant given the power savings of the 3.3V components. Micron SRAMs require only a 3.3V supply and no additional buffer circuitry when interfacing to other 5V components.

CONCLUSION

Although the transition to 3.3V was envisioned to take a number of years, 3.3V microprocessors and low-power portable designs may force a majority of systems to transition in the next 18 months. This transition will be marked by a number of mixed-voltage systems until all computer components are available in 3.3V versions. Designers of the mixed-voltage systems must look carefully at manufacturers' specifications to determine if external buffering is required, and how to gain maximum power savings from the devices. Micron 3.3V SRAMs are an excellent choice for 3.3V systems because they have been designed to minimize design headaches and eliminate buffers when interfacing with 5V TTL components. As Micron is continually improving and expanding our 3.3V line, designers should consult the factory for the latest information on new products.

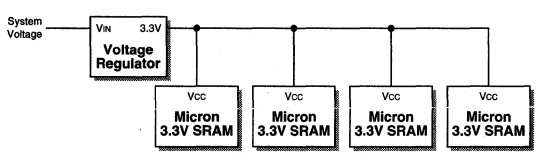


Figure 6
GENERATING 3.3V IN A 5V SYSTEM OR PERIPHERAL

TECHNICAL NOTE

TECHNICAL NOTE

LOW-POWER MEMORY DESIGN USING DATA RETENTION

INTRODUCTION

Increasingly, designers are looking for ways to minimize power consumption. Although battery-powered portable systems have always been optimized for low power, it is becoming increasingly important to minimize power and heat in other nonportable applications. Many users are replacing their desktop computers with portables or notebooks and do not want to sacrifice performance. To support these users, high-speed, low-power SRAM cache memory will increasingly be used, but with the addition of power management circuitry optimized for low-power operation.

Data retention mode is a standby mode of SRAM operation, which helps engineers to improve battery lifetime. Many applications are already designed to take advantage of this data retention capability to reduce power. This technical note describes this mode of operation and shows how to take advantage of this feature.

DATA RETENTION APPLICATIONS

Applications which require the low power of data retention have typically been portable designs using SRAM memory either as a secondary cache for a computer or as primary memory for a DSP or embedded processor. These applications require the lowest power possible and can take advantage of data retention mode when in standby operation. To demonstrate the power savings of data retention over other operational modes, Tables 1 and 2 show power consumption for several versions of Micron SRAMs. The power savings of data retention can be quite dramatic, with over a 90 percent savings attained by using 2V data retention over normal 5V CMOS standby mode and over 75 percent for 3.3V SRAMs. Although not as dramatic, data retention for 3.3V SRAMs still offers significant power savings. Any convienient voltage down to 2V may be chosen for the data retention mode.

NEW TECHNICAL NOTE

Table 1
POWER DISSIPATION FOR 5 VOLT SRAMs (mW)

POWER MODE	256K SRAM	1 MEG SRAM
Operating (50 MHz)	715	800
Standby (TTL)	248	250
Standby (CMOS)	27	27
3V Data Retention	1.8	0.98
2V Data Retention	0.8	0.35

Table 2
POWER DISSIPATION FOR 3.3 VOLT SRAMs (mW)

POWER MODE	256K SRAM	1 MEG SRAM
Operating	198	198
Standby (TTL)	54	43
Standby (CMOS)	2.7	1
2V Data Retention	0.7	0.3

Data retention can be incorporated into a design in a myriad of ways. One specific implementation has been chosen to demonstrate how this mode can easily be incorporated. Figure 1 shows a schematic of an SRAM memory array consisting of two 32K x 8 SRAMs connected to a DSP processor and powered by a voltage regulator circuit. Voltage regulators and/or power management circuitry is already included in designs, and frequently only minor modifications are required to add the data retention capability.

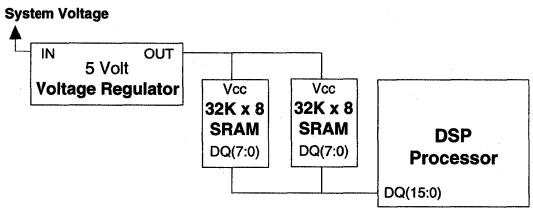


Figure 1
A DATA RETENTION DESIGN

The voltage regulator used in the circuit has an adjustable output voltage. The output voltage of many off-the-shelf regulators are controlled by a voltage divider circuit. Typically, these divider circuits are set to generate a single output voltage of 5 or 3.3 Volts. By including a switch into the network (Figure 2), it is possible to have two different programmable voltages to the SRAM array. During normal operation, resistor R1 generates a compensation voltage which gives an output of 5 volts. When the system goes into standby mode, switch S1 closes, pulling resistor R2 into the circuit and changing the compensation voltage to provide an output of 3 volts.

Several companies such as Maxim, National Semiconductor and Silicon General offer voltage regulators with an adjustable output as described above. These circuits make the incorporation of data retention mode straightforward. SRAM power dissipation for the memory array shown in Figure 1 decreases to 2mW in 3V data retention mode from the 54mW when in 5V standby. Future power controller products have been announced with circuitry to automatically switch to a battery voltage when Vcc drops below a threshold voltage, eliminating the external resistors.

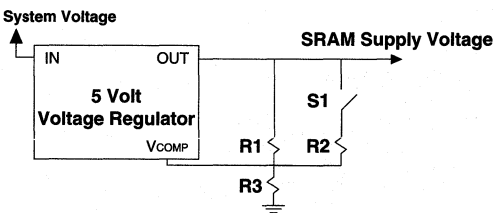


Figure 2
GENERATING DATA RETENTION STANDBY VOLTAGE

DATA RETENTION MODE

In order to ensure that the memory array operates with the lowest possible power, the conditions in Table 3 must be met. Vcc for data retention must not fall below 2 Volts to ensure that the the memory cell retains stored data.

If the input voltage restrictions are violated, such as setting the control lines in a High-Z state, the CMOS input buffer transistors can enter a linear or saturation region of operation with an increase in standby current. To prevent this, the input voltage specification must be observed. TTL input levels can be applied to the device inputs without loss of functionality or data, but with an increase in power dissipation. Devices with gated inputs do not have this restriction for input voltages. These versions of Micron's SRAMs have gated inputs which are controlled by the $\overline{CE}$ inputs. $\overline{CE}$ on the gated input parts ensure that the input buffers remain fully turned off. Consult data sheets for information on specific versions.

The time to enter data retention mode is nearly instantaneous. Chip deselect to data retention occurs as soon as the power supply is reduced. Exiting data retention and entering operational mode takes a maximum of one SRAM cycle time (^tR), between 8ns and 35ns, depending upon the SRAM used.

Table 3
DATA RETENTION OPERATING CONDITIONS

Parameter	Symbol	Conditions
Data Retention Vcc	V_{DR}	≥ 2 Volts
Input Voltage*	V_{IN}	V_{IN} ≥ (Vcc-0.2V) or ≤ 0.2V
Chip Enable	$\overline{CE}$	$\overline{CE}$ ≥ (Vcc-0.2V)
Chip Deselect to Data Retention Time	^tCDR	0ns
Operation Recovery Time	^tR	^tRC (MIN)

*Not required for gated input parts

TEMPERATURE CHARACTERISTICS

Applications that run cooler than the maximum operating temperature of the SRAM will benefit by having reduced power in data retention mode. Figure 4 shows how data retention current (IccDR) varies over temperature and voltage for a 256K SRAM. Typically, current is reduced as temperature decreases and a "cooler" application can extend battery life further.

As an example, a 256K SRAM circuit used in an ambient temperature not exceeding 30°C will typically see a power reduction of 50 percent over parts exposed to 70°C. The curve in Figure 4 can be used to estimate the increase in battery lifetime. IccDR curves are available for specific SRAM families.

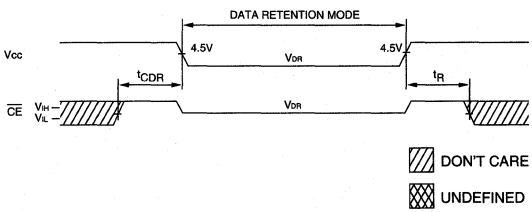


Figure 3
LOW Vcc DATA RETENTION WAVEFORM

CONCLUSION

Data retention mode offers a method to drastically decrease the power of SRAMs. As described in this technical note, this feature is a method to reduce current during standby mode, especially for portable and notebook applications where battery power is used and standby mode is entered often. The ease and negligible cost of adding this feature makes data retention a preferred method of extending battery life.

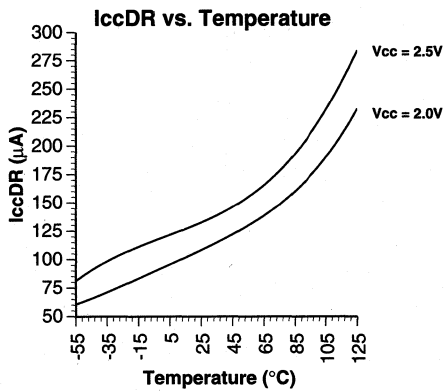


Figure 4
IccDR vs. TEMPERATURE FOR A 256K SRAM

NEW TECHNICAL NOTE

NEW TECHNICAL NOTE

TECHNICAL NOTE

SRAMs AND LOW-VOLTAGE DATA RETENTION

INTRODUCTION

Data retention is a mode of operation on Micron SRAMs that allows data to be maintained while Vcc is allowed to be as low as 2.0V. Because of the desire for low-power in portable and handheld systems, this mode is a popular option for extending battery lifetime. This technical note describes how low-voltage, data retention is used in systems to save power and why Micron SRAMs can store data in this mode. It also describes what tests Micron performs on SRAMs to assure this mode of operation.

DATA RETENTION - HOW IS IT USED?

Many battery-powered microprocessor and DSP applications use SRAM. These applications typically access the SRAM memory infrequently. This makes the dominant component of power dissipation the standby mode of operation. One standby mode consists of disabling the device by setting $\overline{CE}$ inactive (HIGH), but keeping Vcc between 4.5V and 5.5V. This places the SRAM in standby mode and reduces power dissipation from operating levels. However, this does not reduce power to the lowest possible level. The other standby mode, low-voltage data retention, is entered by deselecting the device (setting $\overline{CE}$ to a logic HIGH) and reducing the supply voltage to a value greater than 2V but less than the Vcc operating voltage. The device can be accessed again by returning Vcc to normal operating levels without loss of data.

As an example, consider a 1 Meg SRAM organized as a 128K x 8 (part number MT5C1008). Power dissipation in standby mode will be 27.5mW, but can be reduced to 0.85mW in data retention mode at 2V which gives a power savings of 97 percent.

HOW DOES DATA RETENTION WORK?

Micron manufactures data retention SRAMs that are guaranteed to retain data under low-voltage data retention conditions. These SRAMs are designed with a four-transistor SRAM cell that is inherently designed to prevent data loss in the low-voltage mode. Figure 1 shows a schematic of this cell structure. Unlike a DRAM that uses a capacitor to store information, the SRAM cell uses two cross-coupled inverters to retain data which is shown logically in Figure 2.

To ensure that the cell retains data when Vcc is reduced, the current supplied to nodes A and B from the pull-up resistors must exceed any leakage current present on the node. The pull-up transistor is designed to exceed leakage under all conditions.

If the leakage current at nodes A or B were greater than the pull-up resistor current, the voltage on the node would

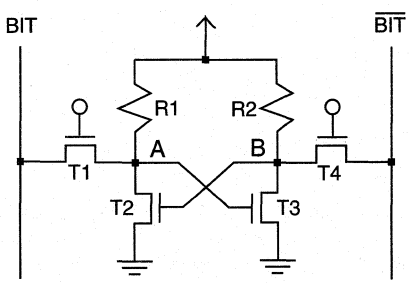


Figure 1
THE SRAM CELL

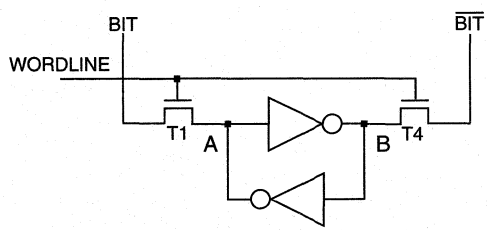


Figure 2
THE SRAM CELL

decay during data retention mode. After returning to a normal operating condition, this could cause the bistable cell to power-up with invalid data. Because Micron SRAMs are designed to prevent this condition, the cell will not "flip" logic levels when returning to an operating mode from data retention mode.

ENSURING DATA INTEGRITY

In addition to the cell design for data retention operations, Micron tests all data retention parts to guarantee data retention operation. All SRAM parts tested for data retention are marked with an "L" in the part number (i.e. MT5C1008 L).

Leakage currents are quite small and the time to fail can be fairly long. Because of these long test times, automated test equipment (ATE) cannot effectively screen these parts. To effectively guarantee memory retention, the test procedure must be conducted in the data retention mode at temperature extremes for a prolonged period of time. These parts are tested using the Micron AMBYX® burn-in system which dynamically tests memory devices at various temperatures.

Micron has established a test sequence for low V_{CC} data retention. Every device is tested in our AMBYX burn-in system using the following sequence:

1. Ambient (25°C) preretention test confirms device contact continuity.
2. Ramp temperature up to 125°C and write a checkerboard pattern with V_{CC} = 4.5V.
3. Reduce V_{CC} to 1.9V and hold data for one hour.
4. Raise V_{CC} to 4.5V and read pattern.
5. Write a checkerboard complement pattern at V_{CC} = 4.5V.
6. Lower V_{CC} to 1.9V for one hour.
7. Raise voltage to 4.5V and read the pattern.
8. Ramp temperature down to -45° and write a checkerboard pattern at V_{CC} = 4.5V.
9. Reduce V_{CC} to 1.6V and hold data for one hour.
10. Raise V_{CC} to 4.5V and read the pattern.
11. Write a checkerboard complement pattern with V_{CC} = 4.5V.
12. Lower V_{CC} to 1.6V for one hour.
13. Raise voltage to 4.5V and read the pattern.

CONCLUSION

Micron is able to reduce system power in critical applications such as portable and handheld equipment through the use of low voltage, data retention. By proper design and testing, Micron parts with the "L" designator are guaranteed to operate down to a 2V V_{CC} which can reduce power dramatically.

TECHNICAL NOTE

3.3V SRAM CAPACITIVE LOADING

INTRODUCTION

High-speed SRAMs are used in many applications which require external memory. Microprocessors such as Pentium™, PowerPC™ and 680X0 use caching subsystems to minimize external data access times and reduce or eliminate wait states. DSP designs for telecommunications, disk drives and video compression also use SRAMs, but as main memory. All these applications place the SRAMs on a system bus that is shared by one or more microprocessors, several I/O devices and other types of memory (ROM, EPROM, etc.).

Even though transceivers and/or buffers interface with the actual bus, SRAMs are typically required to drive loads larger than the maximum loading specification given in data sheets. Hence, the access time must be derated to reflect the actual performance of the SRAM under these circumstances.

SIMILARITY BETWEEN SRAM FAMILIES

Micron's 256K and 1 Meg SRAM families all have similar size output transistors and identical architectures. Hence, all devices will have the same drive characteristics. The actual data presented in this technical note are derived from the 256K SRAM family.

DERATING THE OUTPUT DELAY

Figure 1 shows the typical output load as specified in Micron SRAM data sheets. This load tests the capability of the output to drive a capacitive load. It also ensures that the output drive current is met (I_{OH} = -4mA and I_{OL} = +8mA). Products such as Micron's 32K x 36 and 64K x 18 SyncBurst™ SRAMs use an output load as given in Figure 2 to more accurately reflect the transmission line characteristics that the device will encounter. In both cases 30pF is the maximum output capacitance tested.

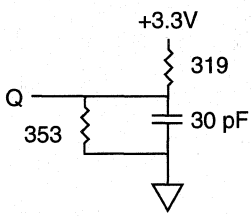


Figure 1
Typical Output Load

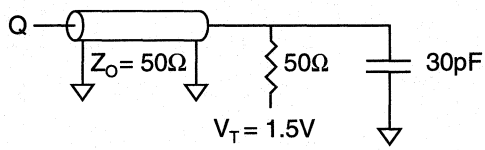


Figure 2
A Transmission Line Load

NEW TECHNICAL NOTE

High bus frequencies (>50 MHz) cannot tolerate the delay associated with high capacitive loads and typically remain under 30pF. Other applications occur that have heavily loaded outputs and require proper derating of the output delay. This derating is shown in Figure 3.

The graph representing access time (^tAA) delay is based on data gathered on Micron's 256K SRAM. Access time measurements were taken with the SRAM subjected to various capacitive loads. In the range covered, the change in access time was seen to be a third order polynomial function of the capacitive load. Figure 3 can be used to properly derate the output timing.

For example, imagine an output load of 330pF. This load is 300pF above the 30pF maximum. Using the chart we can translate this additional 300pF into approximately 4.2ns of additional delay. If the part used was a 20ns SRAM (^tAA = 20ns), the derated ^tAA is 24.2ns.

A more detailed description of output delay using transmission line analysis is given in the technical note, "High-Speed Memory Design Techniques," TN-05-21.

SUMMARY

The SRAM timing specifications of all major vendors are based upon an industry standard capacitive load of 30pF. In some applications, the SRAMs are required to drive much larger capacitive loads. In addition, today's designs are implemented around higher frequencies. This requires the system timing to be more precise; hence, loading becomes a more important issue. Understanding how the SRAM will perform under specific loading conditions may result in a more reliable design.

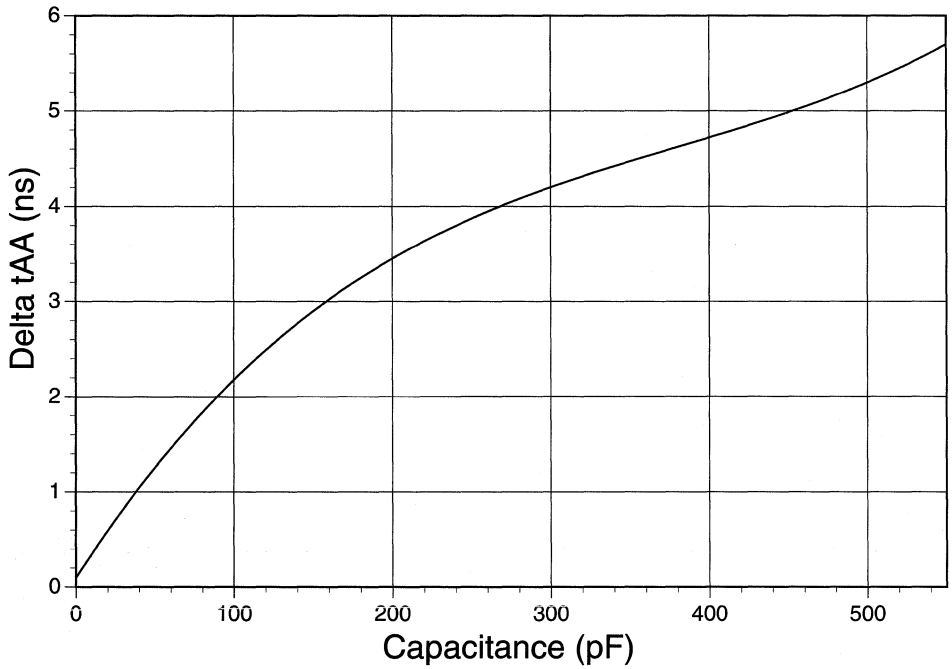


Figure 3
INCREASED ACCESS TIME vs. ADDITIONAL OUTPUT LOADING

TECHNICAL NOTE

HIGH-SPEED MEMORY DESIGN TECHNIQUES

INTRODUCTION

Over the last 20 years microprocessor clock speeds have increased at an exponential rate. As we can see from Figure 1 below, clock speeds have migrated from 1 MHz with the Intel 4004 to 200 MHz with the latest version of the Alpha processor. A parallel increase in bus speeds has occurred with current systems having cycle rates of 50 MHz and 60 MHz and moving toward 75 MHz and 100 MHz.

Design techniques which were used at slower frequencies (20 MHz and lower) are no longer appropriate for these higher bus frequencies. Much more attention must be paid to board layout, bus loading and termination to ensure that short clock cycle times can be met without noise, ringing, crosstalk or ground bounce. This article discusses these issues and the choices a designer faces in high-speed memory system design.

THE MEMORY HIERARCHY

Figure 2 shows the memory hierarchy conventionally used in a computer system. High-speed cache memory integrated with the microprocessor is used to store frequently accessed instructions and data and to avoid the time penalties associated with off-chip accesses. However, only a limited amount of cache can be included directly on the chip in the level one (L1) cache (sizes vary from 8KB to 32KB). Secondary or level two (L2) cache is included in systems to increase system performance when the processor requires information that is not stored in the L1 cache. Sizes for the L2 cache vary greatly depending on system requirements. The largest portion of data, stored in the DRAM bulk memory array, is significantly slower and has a large access time penalty. If a cache miss occurs, retrieving data from the DRAM array could take up to six or more processor clock cycles, drastically reducing system performance. DRAM sizes in PCs vary from 4MB to 512MB.

High-speed techniques must be used in evaluating data transfers between the cache SRAM and microprocessor. Timing between the cache and the microprocessor is especially critical because of the short cycle and access time required. Bus frequencies are already at 50 and 60 MHz and require careful design to attain zero wait-state performance. At these frequencies designers are increasingly using synchronous SRAMs to help alleviate timing problems, but even synchronous SRAMs require a thorough timing analysis.

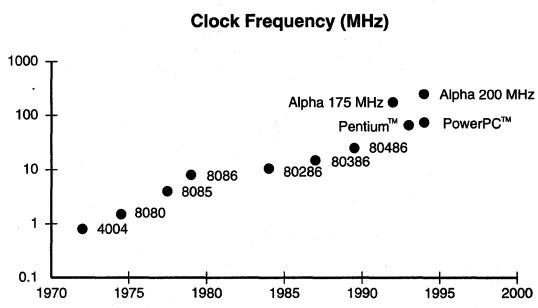


Figure 1
MICROPROCESSOR CLOCK SPEEDS

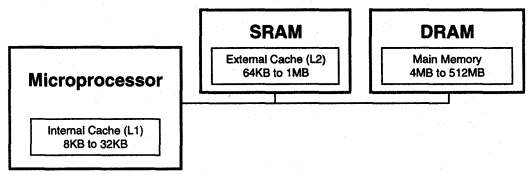


Figure 2
TYPICAL PC MICROPROCESSOR MEMORY CONFIGURATION

A CACHE TIMING EXAMPLE

The following example demonstrates how little timing margin is available for bus speeds exceeding 50 MHz and why it is important to carefully analyze bus timing when designing memory subsystems at these frequencies. For this example, we assume that the microprocessor operates at 60 MHz and is using a synchronous cache array organized as 32K x 72, with two 32K x 36 SyncBurst™ SRAMs (MT58LC32K36B2) as shown in Figure 3.

The timing of a READ cycle for this system is shown in Figure 4. The equation below shows how to calculate the amount of timing margin available in any design. The variable $^tCLK represents the clock cycle time of the external bus. For a 60 MHz system this represents a 16.7ns cycle time.

$$\begin{aligned} t_{margin} &= t_{clk} - t_{flight} - t_{setup} - t_{access} \\ &= 16.7 - 1.4 - 4 - 10 \\ &= 1.3ns \end{aligned}$$

In this example a READ cycle is being performed which sends data from the SRAM cache memory to the microprocessor. This example assumes that the address and control signals are valid during the positive edge of the clock pulse and exceed the setup time of the SRAM. In a synchronous system the memory clock cycle begins with the rising edge of the clock which signals the SRAM to use the address on the bus, find the data stored at this address and send it to the outputs. The data appears at the output t_{access}ns later (10ns for this example). Once data appears at the output it must travel from the SRAM to the microprocessor through signal traces on the circuit board. This transfer time is called t_{flight} and can vary greatly. t_{flight} will be discussed in more detail in the next section. Lastly, the microprocessor must latch the data and it must be available to meet the processor setup time (t_{setup}). The hold time must also be met, but it occurs as part of the next clock cycle and does not have to be subtracted as part of the timing calculation.

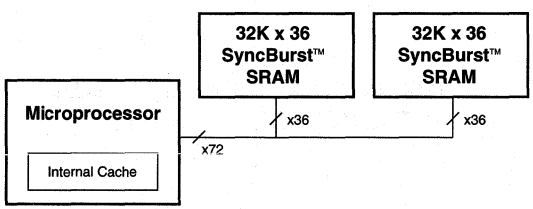


Figure 3
SYNCHRONOUS CACHE MEMORY DESIGN USING TWO MICRON 32K x 36 SRAMs

Altogether the total time is 15.4ns and the requirement for 60 MHz operation is anything less than 16.7ns. The margin for error is 1.3ns and board layout or other factors can easily cause the cycle time to be exceeded. In the next section we will discuss how t_{flight} can vary. Even with careful design, a t_{flight} of less than 2ns may be very difficult to obtain. Typical times in some designs could be 5ns or more. It is no longer sufficient just to connect components without considering the timing impact to the system.

CALCULATING t_{flight}

t_{flight} consists of the components shown in the equation below:

$$t_{flight} = t_{clock\ skew} + t_{propagation\ delay} + t_{rise\ time}$$

The first component, $t_{clock\ skew}$, can be defined as the skew between rising and falling edges of the clock signal for different components on the board. If a clock rises at time t = 0 on the microprocessor clock input, the clock input to the first SRAM might rise at time t = 0.25ns and t = 0.45ns on the second. This skew in timing can be due to uneven line lengths or varying load capacitances on the different lines. If a series of buffers are used to distribute the clock signal,

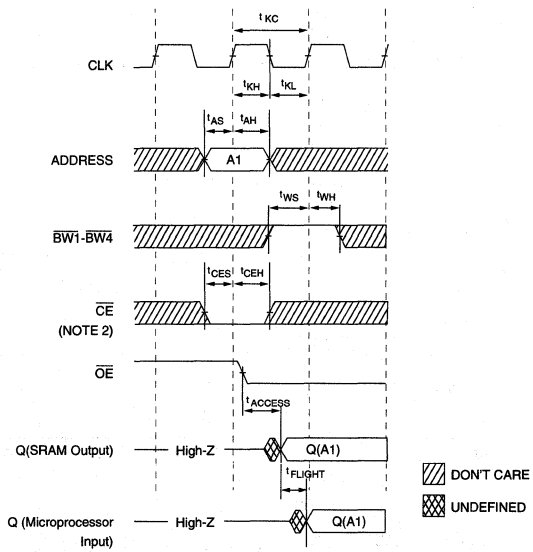


Figure 4
READ CYCLE TO CACHE MEMORY TIMING DIAGRAM

delay times through these buffers will also vary and add to the skew. These types of skew are frequently ignored for slower systems but must be accounted for in high-performance ones.

The second component, $t_{propagation\ delay}$, is determined through the characteristics of the transmission line and line load. The propagation delay now consumes a considerable portion of the cycle time of a high-speed system and can no longer be ignored. Designers cannot assume that outputs drive purely capacitive loads and must determine if interconnects should be treated as transmission lines. A purely capacitive load assumes an RC time constant delay consisting of trace resistance, output driver resistance and total lumped capacitance. Transmission line analysis, although more difficult, more accurately reflects actual conditions. Determining propagation delay is discussed in more detail in the next section.

The next component, $t_{rise\ time}$, is determined by the speed of the component driving the line. A faster rise time can help speed the cycle time of a system but may require a huge output driver with a large current dissipation. Rise times can also vary from component to component and worst-case times should be used for design analysis.

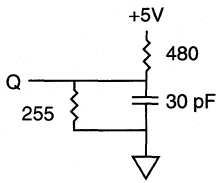


Figure 5
OUTPUT LOAD EQUIVALENT

A component that should not be ignored is circuit loading. The external capacitive loading is usually accounted for in the access time of the device (t_{access}). A device will have an access time rating that is valid up to a given loading. For example, high-speed asynchronous SRAMs are usually rated with an AC loading as shown in Figure 5 with a capacitive rating of 30pF. Designers can modify their timing margin if the capacitive loading is less than or greater than the specified rating. The equation below shows how timing varies with capacitive loading above or below the rated specification for Micron's SyncBurst family of SRAMs. The difference between the rated capacitive load and the actual capacitive load is represented by the variable DC_L ($DC_L = C_{actual} - C_{rated}$).

$$\Delta T_{KQ} = 0.016 \frac{ns}{pF} X \Delta C_L\ pF$$

CIRCUIT TERMINATION

Unterminated Lines

Because electrical signals travel at a finite velocity through a circuit board, it is necessary to determine how long they take to propagate from driver to receiver. This length of time determines if the output circuit requires termination. As an example, assume that a circuit board uses a polyimide dielectric with a relative dielectric constant (ε_r) of 3.5. Common dielectric constants are shown in Table 1. If the circuit board has a strip conductor and a ground plane separated by a dielectric medium as shown in Figure 6a (microstrip line), we could use the following equation to calculate the signal speed:

$$T_d = 0.004 \sqrt{0.45\varepsilon_r + 0.67}\ ns\ per\ mm$$

For this circuit board the equation gives us a signal velocity of 6 ps/mm. If the signal conductor were instead sandwiched between two power planes (Figure 6b) we can use a stripline equation to calculate the signal velocity.

$$T_d = 0.004 \sqrt{\varepsilon_r}\ ns\ per\ mm$$

For the same circuit board we now have a signal velocity of 7.5 ps/mm. The equations above give valid results for reasonable values of trace widths, dielectric constants and dielectric thicknesses. Books are available on transmission line theory for a detailed analysis of propagation delay for various structures.

The purpose of calculating a delay time for signals is to determine if the circuit delay can be treated as an RC time constant. This can be done if the maximum trace length meets the following inequality:

$$L_{max} < \frac{t_r}{2T_d}$$

t_r = Rise time or fall time of the output driver

Table 1
VARIOUS DIELECTRIC CONSTANTS

Material	Relative Dielectric Constant (ε_r)
Ceramic - Alumina	9.4
FR-4	4.7
Glass epoxy	4.0
Polyimide	3.5
Silicon	11.8

NEW TECHNICAL NOTE

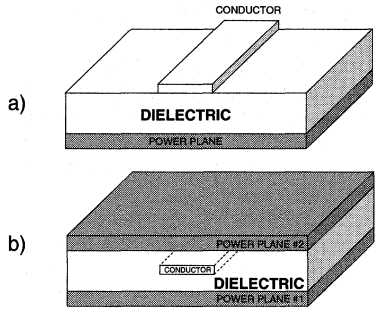


Figure 6
a) MICROSTRIP LINE, b) STRIPLINE

For our example we assume a rise or fall time of 2ns. This means that as long as the maximum line length is less than 133mm or 5.2 inches (for stripline), the circuit delay can be treated as an RC time constant. For a given capacitive load we can calculate the actual signal propagation time using the equation:

$$T_{ld} = T_d \sqrt{1 + \frac{C_L}{C_o}} \text{ ns per mm}$$

C_L = Load Capacitance
C_O= Transmission Line Capacitance
where:

$$C_o < \frac{T_d}{Z_o}$$

Z_O = Characteristic impedance of the signal trace

For our stripline example, C_O = 1.5 pf/cm and the load is C_L = 50pf with a 5cm transmission trace length. The actual signal velocity is 22 ps/mm or 1.1ns for 5cm of line length. For this example we assumed a value of Z_O of 50Ω. This value can be calculated using the equations below, or supplied from a board vendor. It is recommended that a designer use computer software to determine Z_O instead of these equations which are only approximate.

For stripline:

$$Z_o = \frac{30\pi(1-t/b)}{\sqrt{\varepsilon_r}\,(W_e / b + C_f/\pi)}$$

where:

$$C_f = 2\ln\left(\frac{1}{1-t/b}+1\right) - \frac{t}{b}\ln\left\{\frac{1}{(1-t/b)^2}-1\right\}$$

$$W_e = b\left[\frac{W}{b} - \left\{\frac{(0.35 - W/b)^2}{1+12t/b}\right\}\right]$$

W = width of strip conductor
t = thickness of strip conductor
b = dielectric thickness

These stripline equations are relatively accurate if the following limitations are met:

$$0.05 \le W/(b-t) \le 0.35$$
$$t/b \le 25$$

Terminated Lines

If line lengths are greater than L_{max}, the above equations can no longer be used and terminations should be considered. For these situations the user should use simulation tools to accurately define and analyze their distributed element circuit. Several considerations for terminated lines are discussed in this section.

When transmission line analysis is used, the designer must determine if the design will use incidence-wave or reflected-wave switching. Incidence-wave switching is potentially the quickest way to drive external devices because it does not depend upon the reflected signal to exceed V_{IH} or V_{IL}.

Incidence-wave switching has the drawback that large amounts of power can be generated in the output driver of a chip. Let's calculate what the power of one I/O signal can be using this method. First, the effective characteristic impedance must be calculated using the equation below:

$$Z_L = \frac{Z_O}{\sqrt{1 + \frac{C_L}{C_O}}}$$

For our example in the previous section, using a value of Z_O of 50Ω and a transmission line of 10cm, Z_L is equal to 24Ω. We can use this number and the output impedance of the driver to determine the instantaneous switching current of the outputs. If the output driver is 25Ω, we will see an instantaneous current of 100mA. A circuit implementation using wide devices could generate a large noise spike that would be very difficult to decouple. The reflection at the end of the line must also be accounted for.

Reflected-wave switching can cut power and noise dramatically because the driving circuit needs to generate only half the output voltage upon switching as the incidence-wave solution. The signal initially propagates at half the required voltage level until it hits the end of the transmission line. Then the reflection causes the voltage level to double. Because the reflected-wave is used, time must be allotted for the reflected-wave propagation. This method was

adopted for use in the Peripheral Component Interconnect (PCI) bus.

TYPES OF TERMINATION

Several types of termination are commonly used in designs. The first (shown in Figure 7a) is series-resistance termination. A resistor is connected between the output of a driver and the driven elements. A reflected wave from the load which reaches the output can again be reflected generating noise in the output signal. The series-termination is used to prevent this type of reflection. This is done by making the output resistance (R_{device}) of the driver plus the series resistor (R_s) equal to the line impedance or:
$R_s = Z_o - R_{device}$

There is a potential disadvantage to the series termination resistor because of the associated voltage drop. This voltage drop could cause problems with noise margin to V_{OH} and V_{OL} and in a bi-directional signal with V_{IH} and V_{IL}. CMOS device inputs have a high-impedance and only initial AC power is needed to charge/discharge capacitance. Once the output reaches the final level, current dissipation (and voltage drop) across R_s is minimal in CMOS circuits.

In addition to preventing reflection problems, series termination is commonly used in mixed-voltage systems to prevent high currents. In Figure 8, a 5V device is driving a 3.3V input. Many 3.3V devices contain a protection diode

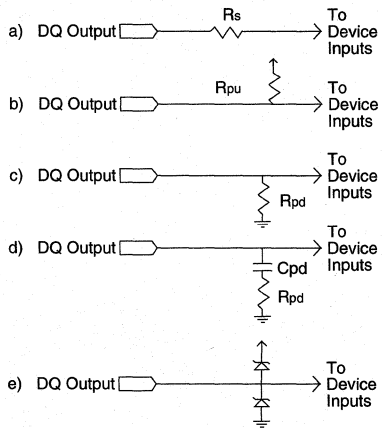


Figure 7
a) SERIES RESISTANCE TERMINATION,
b) PULL-UP TERMINATION,
c) PULL-DOWN TERMINATION,
d) RC TERMINATION,
e) SCHOTTKY DIODE TERMINATION

which is connected to 3.3V. If the input was driven to 5V, the diode would become forward-biased and would generate a low resistance path to V_{CC} which could result in potentially damaging currents. In this case, the series termination resistor has the added advantage of limiting the current in these mixed-voltage systems.

Figures 7b and 7c show pull-up and pull-down termination. A pull-up and pull-down resistor could be also used simultaneously. The main disadvantage of this type of design is that there is a DC power dissipation associated with the devices. For instance, for the pull-up case, there is a DC current path when the output driver is low. This extra current is unacceptable in portable or notebook applications. Mixed 5V and 3.3V designs are recommended to use a pull-up to a 3.3V supply versus a 5V one wherever possible to reduce power consumption.

Another advantage of pull-ups are in connecting TTL-level outputs to CMOS-level inputs. TTL outputs have a V_{OH} specification of 2.4V versus a CMOS V_{IH} of 3.15V. CMOS input levels occur in low-power microprocessors and microcontrollers used in portable and hand-held applications. The pull-up to 5V will allow fast SRAMs with TTL-I/O to drive these CMOS circuits.

RC termination (Figure 7d) allows for proper termination without an associated DC current component. The disadvantage of this approach is that it requires an extra component, the capacitor. An advantage is that this circuit acts as a low-pass filter and can absorb unwanted glitches. Care must be taken in the choice of a capacitor since it must be large enough to absorb glitches that may occur in the system but small enough so it does not slow down the system.

Lastly, Schottky diode termination (Figure 7e) can be used to save power over resistance termination techniques. The advantage of this method is that it prevents overshoot and undershoot problems. The diode turns on if the voltage goes above $V_{CC} + V_{diode}$ or below $V_{SS} - V_{diode}$. The main advantage of this technique is in prototypes constructed with wire wrap or breadboards where line impedance may not be constant. These diodes provide termination without requiring detailed impedance matching calculations.

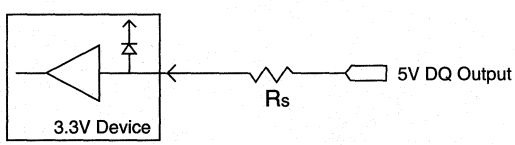


Figure 8
DIODE PROTECTION IN 3.3V CIRCUITS CAN CAUSE PROBLEMS IN MIXED 5V-3.3V SYSTEMS

NEW TECHNICAL NOTE

FUTURE TRENDS

The computer industry always moves toward faster architectures. To meet the bus speeds of the future with 10ns bus cycle times (or faster), new output structures such as Gunning Transmission Logic (GTL) developed by Xerox or HSTL (High-Speed Transmission Logic) under discussion by JEDEC need to be incorporated into designs to minimize output voltage swings and drive transmission lines. Until these new standards are finalized and adopted, designers need to thoroughly analyze their circuit to ensure that cycle times are met.

CONCLUSION

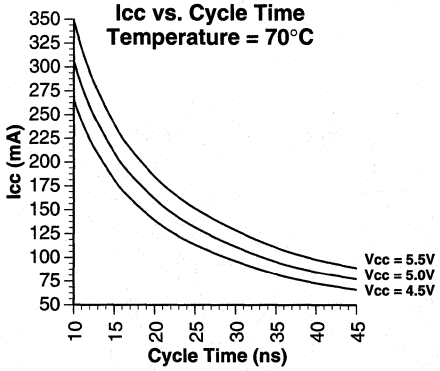
As we have seen in this article, high-speed bus design requires detailed analysis to ensure that the system will work properly. A proper analysis of clock skew and propagation delay is essential to ensure that the system will work properly and with the required performance. This detailed analysis is essential for bus speeds over 50 MHz.

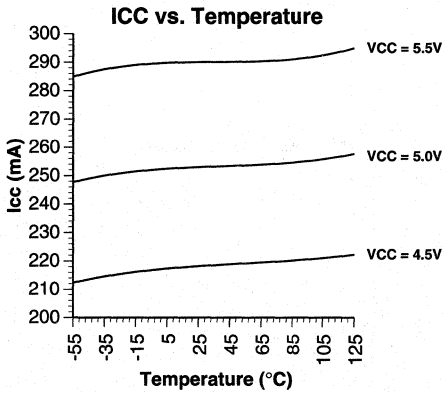
TECHNICAL NOTE

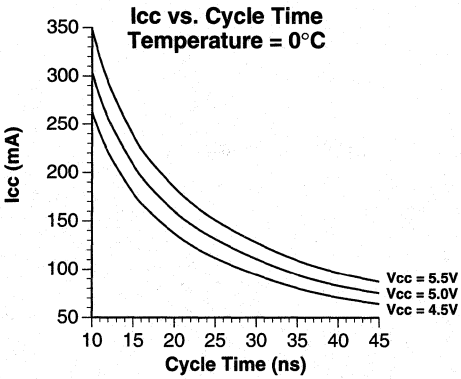
1 MEG REVOLUTIONARY PINOUT SRAM TYPICAL (5V) OPERATING CURVES

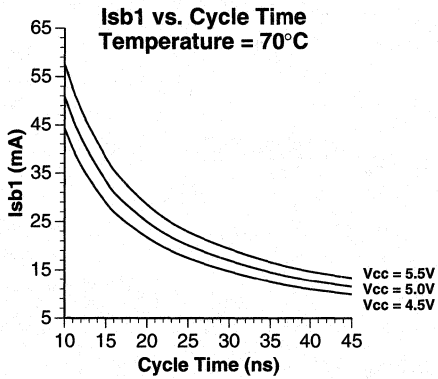
INTRODUCTION

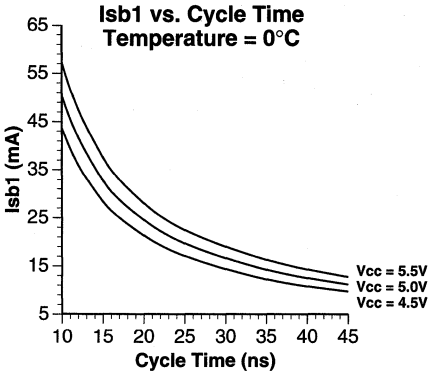
These curves represent the typical operating characteristics of Micron's 1 Meg, 12ns SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.

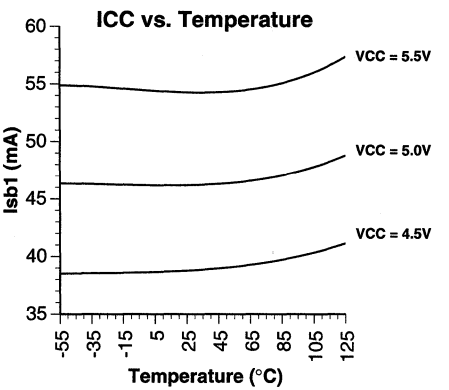


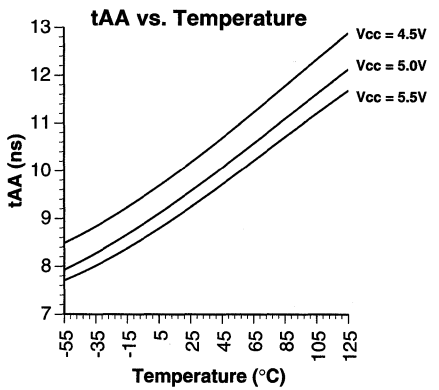


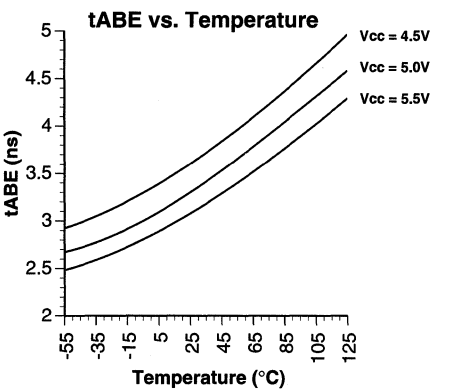


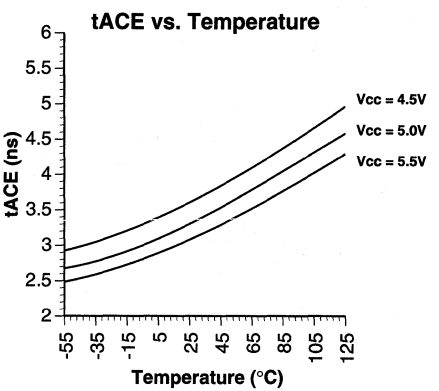


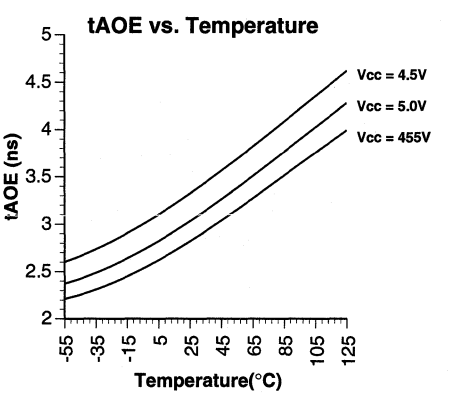


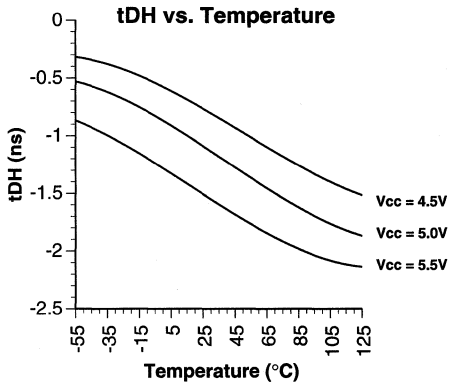


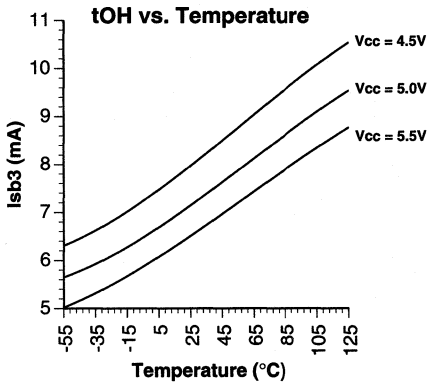


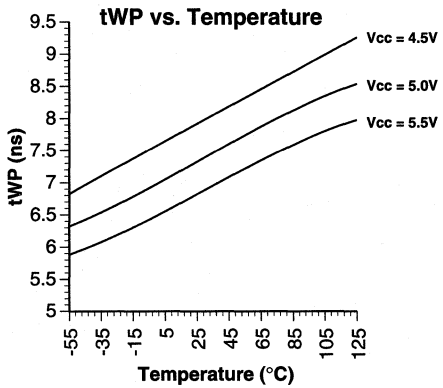












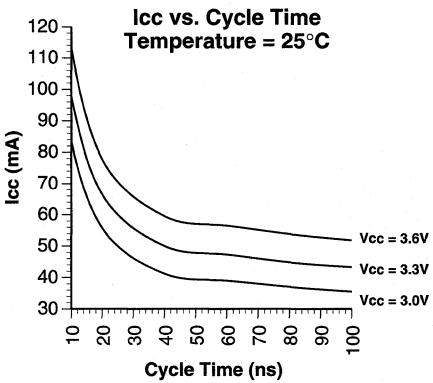
TECHNICAL NOTE

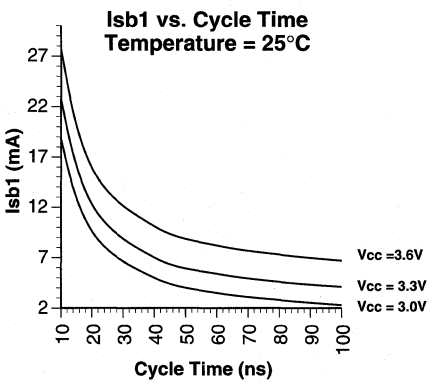
TECHNICAL NOTE

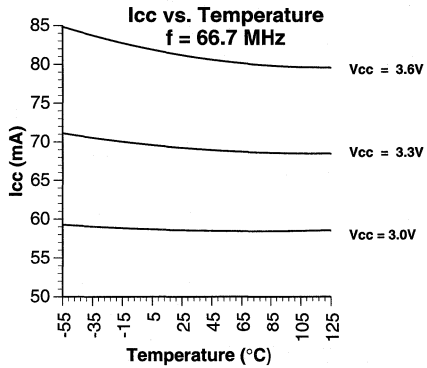
256K SRAM TYPICAL (3.3V) OPERATING CURVES

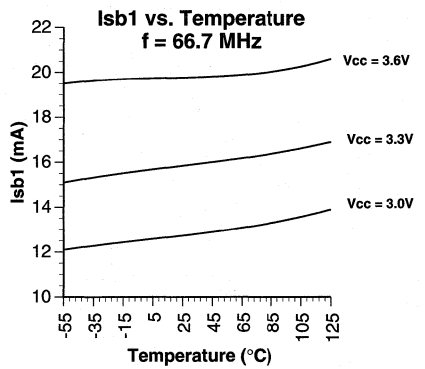
INTRODUCTION

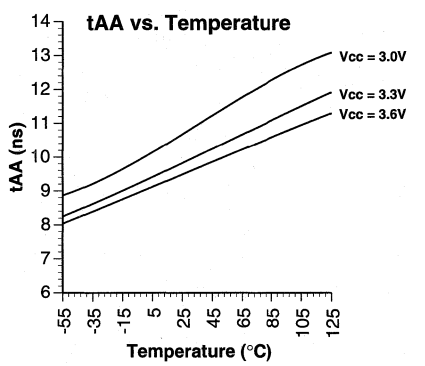
These curves represent the typical operating characteristics of Micron's 256K, 15ns low power (LP) SRAM. They may be used to calculate the typical operating parameters of a memory system. For worst-case design limits, the system designer should refer to the individual data sheets in the SRAM section of this data book.



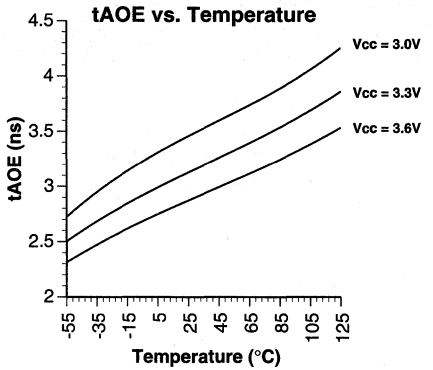


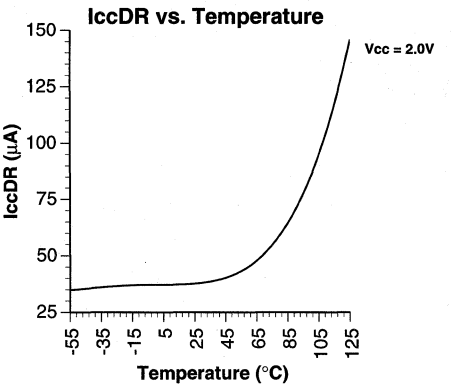


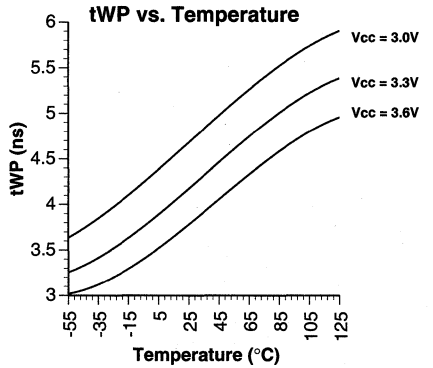


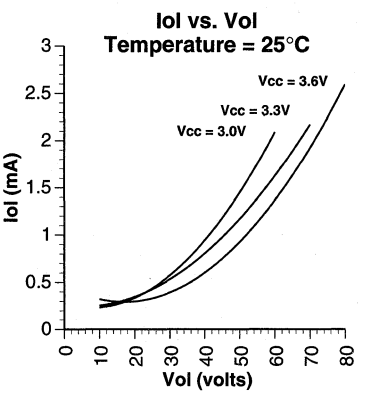


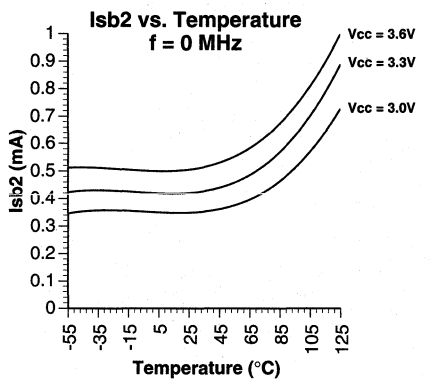
TECHNICAL NOTE

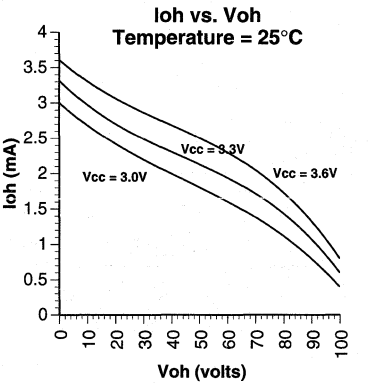












TECHNICAL NOTE

SYNCBURST SRAM DESIGN FOR COMPATIBILITY

INTRODUCTION

Since introducing the industry's first four-byte-wide synchronous burst SRAM, Micron has worked with its customers to maximize the performance of the SyncBurst™ architecture. Micron has facilitated standardization of the new features and attempted to maintain compatibility in the SRAM industry. This article discusses the new features, how they can be used to improve system performance and design convenience, and how compatibility can be maintained throughout the introduction of these and future enhancements. It should be noted that as of this writing, we believe that virtually all synchronous burst SRAM vendors support or plan to support the enhanced functionality discussed herein. However, we suggest that you contact each potential supplier for verification.

PARITY ISSUES

One extra bit per byte has long been used as an easy method of detecting memory/data transmission errors. The main drawback to this method is a lack of choices in error response. If the error occurred in the L2 cache SRAM and the cache line has not been modified, a possible response is to flush the cache line and refill from main memory. Most systems do not bother and just shut down instead. More sophisticated systems use error correction circuitry to detect and correct all single-bit errors and some double-bit errors. This sounds obviously better than just using parity but causes extra delays in data delivery because of the error checking logic. This compromise is essential in systems with high data-integrity requirements such as file servers, transaction processors, some data communications equipment and workstations.

Many systems have been and are being designed without parity or error correcting requirements. The rationale is fourfold. Error rates are low if the circuit design and printed circuit board layout is done expertly (i.e. low transmission error rate, however, transmission errors can be significant and will be left for future discussion). With cache systems, DRAM runs for a small percentage of the time, reducing its average cycle time and hence decreasing the DRAM soft error rate (SER, see Micron Design Line Vol. 3, Issue 1 for a detailed discussion of DRAM SER). SRAM soft error rate is very low (less than one failure per 50 years of continuous operation for a 256KB cache composed of two 3.3V 1 Meg synchronous SRAMs). Ignoring transmission errors and adding the SRAM and 16 Meg DRAM failure rates (using 4 Meg x 4 DRAMs) results in a combined system memory error rate of one per 25 years of continuous full-speed operation. The fourth rationale is cost. It is difficult for a system with parity and no innovative error handling to compete against one without parity.

In response to the low system error rates and customer demand for cost-effective solutions, Micron has added a separate 32K x 32 organization to the SyncBurst SRAM family. The 32K x 32 is pin- and function-compatible with the 32K x 36 SyncBurst SRAM devices. The four DQPn lines (data parity bits) are no-connects on the 32K x 32 device. As a result of the introduction of the non-parity devices, the PDIS pin (parity disable) is no longer needed. The signal was located on pin 87 on the original device. That pin has been freed for a new function which is described in Table 1.

TABLE 1
NEW FUNCTIONS

NEW FUNCTION	TQFP PIN	DESCRIPTION
MODE	31	Burst Mode Input. This pin is also known as LBO# among some vendors. When this input is LOW, linear burst sequence is selected. When this input is HIGH or left UNCONNECTED, interleaved burst sequence is selected. This signal is not intended to be altered dynamically. Adding this pin allows suppliers to reduce the number of device versions and provide optimum lead times for customers. (Competitors' devices may not implement the internal pull-up resistor therefore it is recommended that a HIGH or LOW state be assigned to this input. Micron has added the pull-up resistor to ease design compatibility with the original SyncBurst SRAM release.)
GW#	88	Global Write Input. This input allows a full bus-width device write. This function is valuable to cache controllers which, during cache fill operations, must modify the SRAM contents independent of the state of the BWn# or WEn# signals. This pin, in concert with BWE#, permits direct connection of the BWn# lines to the microprocessor BEn# signals. Two system benefits result: one clock cycle can be eliminated from write cycles because BEn# lines do not have to be conditioned in the ASIC and rebroadcast as BWn# signals, and the pin count of the controller ASIC can be reduced. If this function is not required, this pin should be tied HIGH (to 3.3V). See Figures 1 and 2 for connection examples.
BWE#	87	Byte Write Enable Input. Formerly, PDIS occupied this pin position but was made obsolete by the addition of 32K x 32 devices. This input, when LOW, allows the byte write signals to control write operations (BW1# through BW4# or WEH# and WEL# on 64K x 18 in TQFP). This permits partial bus write operations to the SyncBurst SRAM. If this function and the GW# function is not required, this pin should be tied LOW (to GND). This will permit writes to be controlled solely by the BWn# signals as is the case with original 32K x 36 and 64K x 18 devices. See Figures 1 and 2 for connection examples.

TABLE 2
FUTURE FUNCTIONS

FUNCTION	TQFP PIN	DESCRIPTION
FT#	14	Flow-Through Input. Some vendors will implement this input to allow user selection of pipelined (FT# = HIGH) or non-pipelined, i.e. flow-through operation (FT# = LOW). This function is not implemented in Micron devices. It is recommended that the user select the appropriate input level, neither of which will interfere with reliable operation in the Micron device.
ZZ	64	Snooze Input. This input may be implemented in future Micron devices. When HIGH, this input will cause the device to enter into the lowest-power standby mode within two clock cycles in the non-pipelined device and three clock cycles in the pipelined device (the industry standard will require this to occur within four clock cycles). The device will take an equal number of clock cycles to return to active operation when ZZ is LOW. Prior to implementation, lowest power standby current can be achieved if the clock is blocked from the SRAM and all control and data inputs are static and held near a rail voltage. The ZZ function is most useful to designers of mobile computer systems but it does require that the cache controller create this extra signal. Where pin-count is limited and does not permit, external clock blocking is an alternative and equally effective choice to reduce power consumption. It is recommended that this input be tied LOW for future compatibility.

NEW SIGNALS ADDED TO THE SYNCBURST SRAM ARCHITECTURE

Three new signals have been added to the SyncBurst SRAMs in the Thin Quad Flat Pack (TQFP) package. New signal additions are not possible with the pin-limited 52-PLCC therefore it is not affected by this discussion. Provisions for two future functions have been made which will also be described. Table 1 describes the signal additions and outlines their benefits. Table 2 describes possible future additions to the architecture.

BENEFITS OF THE NEW WRITE INPUTS: PENTIUM EXAMPLE

The descriptions in Tables 1 and 2 outline some benefits obtained by supporting the new functions. More detail regarding WRITE functionality is necessary. Figure 1 shows the connection of two Micron 32K x 32 SyncBurst SRAMs with a Pentium processor without taking advantage of the GW# and BWE# signals. In this case, chipset logic must input the processor's eight Byte Enable (BE#) inputs and separately output eight Byte Write (BW#) signals, four to

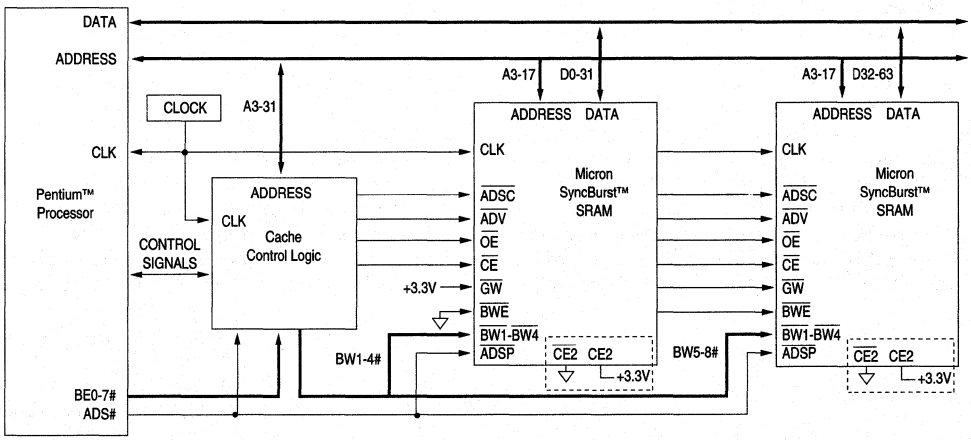


Figure 1
PENTIUM CONNECTION WITHOUT GW# AND BWE#

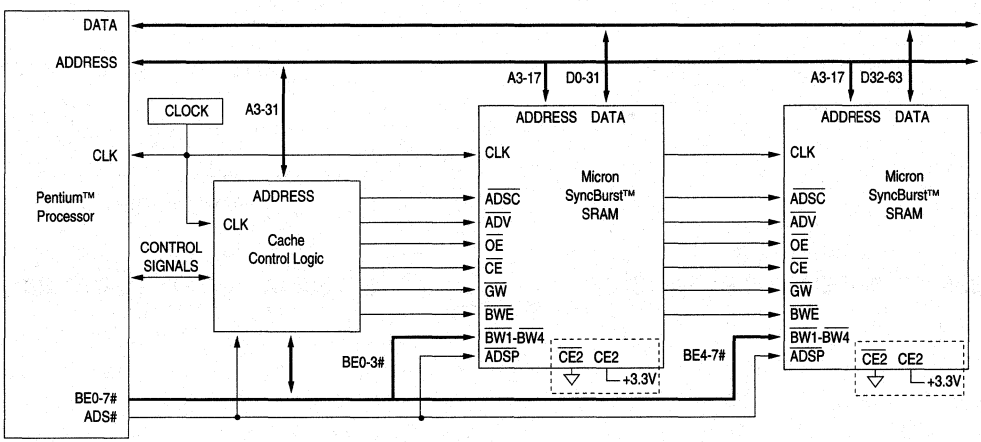


Figure 2
PENTIUM CONNECTION WITH GW# AND BWE#

each SRAM. It is necessary in this case to separate the BEn# lines from BWn# lines because the byte enables from the processor will not be in the correct state during some operations such as external cache snoop cycles. The BEn# lines are not tri-stated when the Pentium AHOLD input is asserted, hence the cache controller cannot simply re-drive those signals to the desired states to cover those cases where the BEn# lines are in unacceptable states. The only way to overcome these constraints is for the cache controller to use eight inputs and eight outputs as described above.

Figure 2 shows the connection of two Micron 32K x 32 SyncBurst SRAMs with a Pentium processor while taking advantage of the GW# and BWE# signals. The cache controller pin count has been reduced from 16 in the previous example to only 10 pins in Figure 2. GW# forces all bytes to be written into the SRAM independent of the state of the BWn# inputs. This is the normal mode of operation during cache line fills. The BWE# signal permits the direct connection of the processor's BEn# signals to the SRAMs for individual processor-derived byte write operations. Regardless of pipelined or non-pipelined (flow-through) operation, all BWn#, BWE# and GW# signals are required to be valid at the same clock rising edge that the data is valid.

Another important benefit of the direct-connection of the processor's BEn# signals to SRAM BWn# signals is the ability to reduce wait states during write operations. The extra time for a BEn# to travel from the processor into the ASIC, propagate through the ASIC logic, drive through the output buffers and to the SRAM as in Figure 1 can induce an extra wait state during write cycles if the tag SRAM is no longer the most speed critical element. Figure 2 shows the direct path. Now, only the BWE# signal is on that critical timing path. Any ASIC designer will testify that a single critical signal can be speed optimized far more easily than 16 signals.

Figure 3 illustrates how depth expansion from 32K x 64 to 64K x 64 is accomplished by adding two more 32K x 32 devices. This method has not been altered by the addition of any new signals. Figure 4 shows how this may be done using two devices on a motherboard and adding a DIMM (dual in-line memory module) to expand memory size. Note that no jumpers are required because the DIMM provides the additional necessary connection of A18 to the chip enables of the "HIGH SRAMs." The HIGH SRAMs normally function during all cache cycles but serve as the upper half of the cache when cache is depth-expanded.

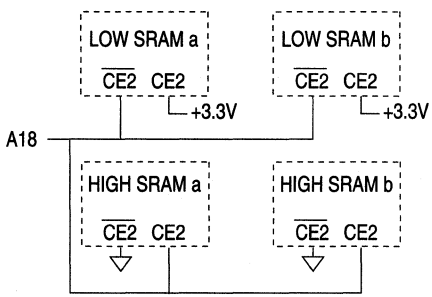


Figure 3
32K TO 64K DEPTH EXPANSION

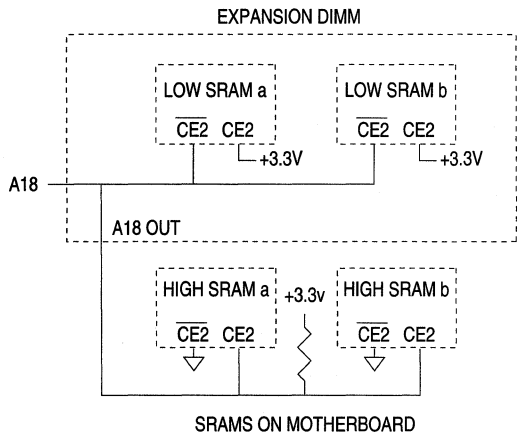
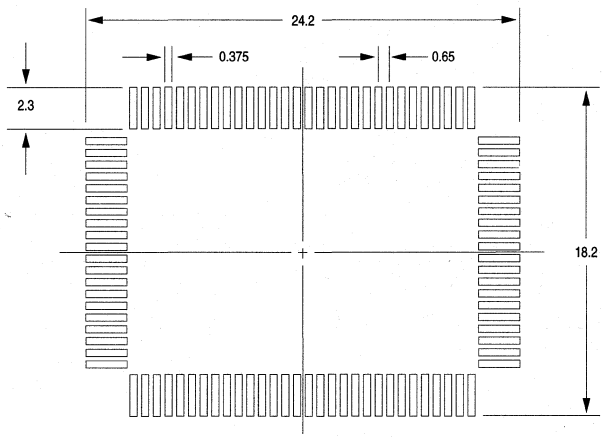


Figure 4
DEPTH EXPANSION USING DIMM

PACKAGE AND PIN COMPATIBILITY

While most vendors are joining in the use of the industry-standard Thin Quad Flat Pack (100-Pin TQFP), some have elected to use the thicker Plastic Quad Flat Pack. Either may be accommodated in a single design by making the pads long enough to accept either package. The thicker PQFP has a slightly broader footprint. This is due to the device lead vertical runs not being shaped perpendicularly to the package underside, hence the taller the package, the wider the lead excursion . It is not desirable to use 90° lead bends due to reduced reliability. See Figure 5 for a recommended PCB land pattern which will accommodate either package thickness. The TQFP offers several advantages over the PQFP. The TQFP can be mounted in systems where height is restricted (JEDEC specification MO-136 lists TQFP overall height as 1.60 mm maximum whereas the PQFP is 2.2 or 3.0 mm depending upon package option). The TQFP is also more speed capable because the thermal resistance is smaller for the thinner package.

Tables 3 and 4 summarize the signals designers need to be aware of when designing for multiple vendors. Figures 6 through 8 provide pictorial pin assignments for the 1 Meg and 1.125 Meg SyncBurst SRAMs in PLCC and TQFP packages accounting for industry compatibility requirements.



NOTE: ALL DIMENSIONS ARE NOMINAL AND IN MM

Figure 5
PCB LAND PATTERN FOR 100-TQFP AND 100-PQFP DEVICES

TABLE 3
CONNECTION FOR COMPATIBILITY: 32K x 36 AND 32K x 32

TQFP PIN	CONNECTION	PURPOSE
1	NC or DQP3	Accommodates parity version if desired
14	LOW HIGH	Flow-through or non-pipelined operation Pipelined operation Note that Micron devices "do not care"
16	NC	Reserved for a reference voltage input in future devices
30	NC or DQP4	Accommodates parity version if desired
31	LOW HIGH	MODE (LBO#) input. LOW sets linear burst sequence. Interleaved burst sequence for generic devices. Micron devices also allow NC for interleaved burst.
38, 39, 42, 43	NC	These pins are currently reserved for JTAG or future functions. Leaving these pins unconnected allows for compatibility with future device enhancements.
49	NC or A15	Reserved for A15 on future devices
50	NC or A16	Reserved for A16 on future devices
51	NC or DQP1	Accommodates parity version if desired
64	LOW HIGH	Future location for ZZ pin. LOW allows future generic devices to operate. Micron devices also allow NC. HIGH will cause future devices to enter low-power mode.
66	NC	Reserved for a reference voltage input in future devices
80	NC or DQP2	Accommodates parity version if desired
87	LOW or BWE#	BWE# input. If this function is not required, tie LOW.
88	HIGH or GW#	GW# input. If this function is not required, tie HIGH.

TABLE 4
CONNECTION FOR COMPATIBILITY: 64K x 18 AND FUTURE 64K x 16

TQFP PIN	CONNECTION	PURPOSE
1-7, 25-30, 51-57, 75-80	NC or Vss	Not reserved for any established functions May be tied LOW to assist in thermal conduction
14	LOW HIGH	Flow-through or non-pipelined operation Pipelined operation Note that Micron devices do not care
16	NC	Reserved for a reference voltage input in future devices
24	NC or DQP2	Accommodates parity version if desired
31	LOW HIGH	MODE (LBO#) input. LOW sets linear burst sequence. Interleaved burst sequence for generic devices. Micron devices also allow NC for interleaved burst.
38, 39, 42, 43	NC	These pins are currently reserved for JTAG or future functions. Leaving these pins unconnected allows for compatibility with future device enhancements.
49	NC or A16	Reserved for A16 on future devices
50	NC or A17	Reserved for A17 on future devices
64	LOW HIGH	Future location for ZZ pin. LOW allows future generic devices to operate. Micron devices also allow NC. HIGH will cause future devices to enter low-power mode.
66	NC	Reserved for a reference voltage input in future devices
74	NC or DQP1	Accommodates parity version if desired
87	LOW or BWE#	BWE# input. If this function is not required, tie LOW.
88	HIGH or GW#	GW# input. If this function is not required, tie HIGH.
92	NC	This pin is reserved for currently undefined future use.

EXISTING DESIGNS

Existing designs which use the original SyncBurst SRAM and do not need the new functionality must make a few modifications to accommodate the enhanced devices. Pin 88 must be tied HIGH (formerly NC), pin 87 must be tied LOW (formerly PDIS) and mode tied LOW if linear burst is desired or tied HIGH or left unconnected for interleaved burst. In this configuration (x32 operation) the parity bits will not be disabled when using the original device functionality, therefore the parity lines (DQP1-4) should be left unconnected or supplied with weak pull-up or pull-down termination in non-parity designs.

SUMMARY

This article provides information which enables engineers to design with the synchronous burst SRAM architecture and avoid compatibility problems in the future. Recommended PCB pad dimensions are supplied to ensure package compatibility. Parity issues are discussed as are the benefits of some new signals. The greatest performance and ease-of-use benefits are derived from the addition of global write and byte write enable inputs to the SRAM family and are described in detail.

NEW TECHNICAL NOTE

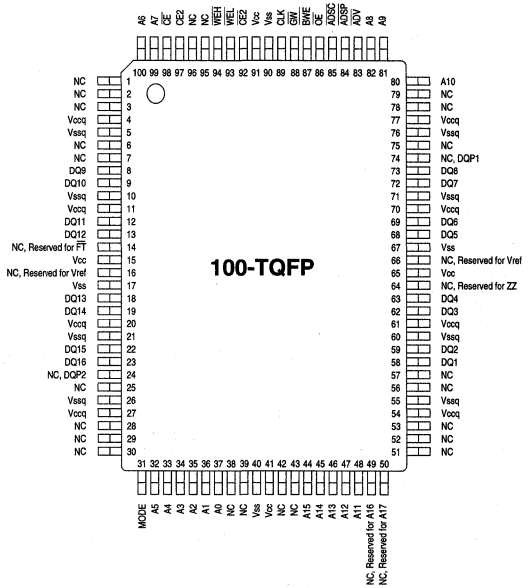


Figure 6
64K x 16/18 COMPATIBLE
PIN ASSIGNMENT

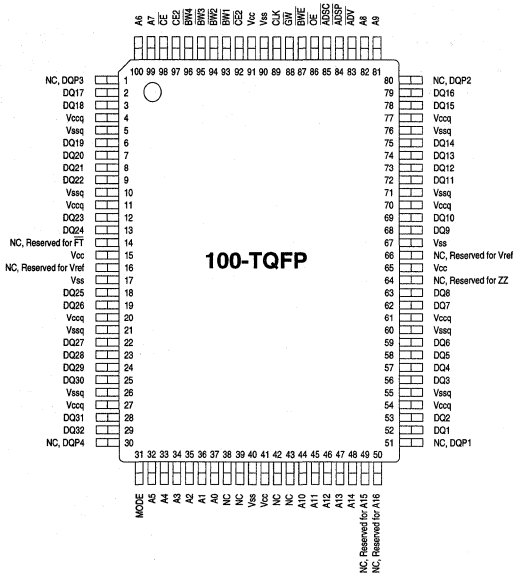


Figure 8
32K x 32/36 COMPATIBLE
PIN ASSIGNMENT

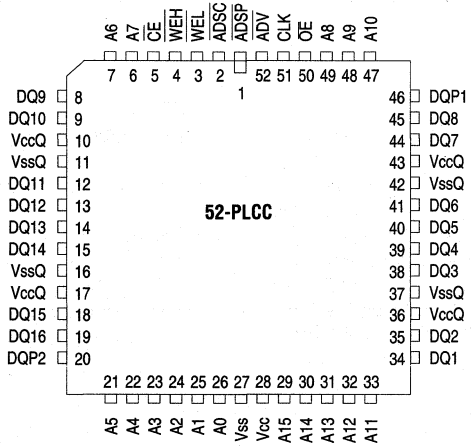


Figure 7
64K x 18 52-PLCC
PIN ASSIGNMENT

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DESIGN TIPS: 32K x 36 SYNCHRONOUS SRAM

INTRODUCTION

New medium- and high-end personal computers all need cache to reach a reasonable point on the price-performance curve. The most desirable cache is one that eliminates the most wait states. In workstation design, cache is compulsory. In personal computer design, cache is becoming essential, even in portable computer designs. The new Micron family of synchronous SRAMs provides the means to achieve the desired price-performance target. This technical note discusses the benefits of these new parts and compares them to alternatives currently available. The discussion will focus primarily on the 32K x 36 SyncBurst™ family members. Since this technical note was written, new functionality has been added along with the 32K x 32 organization. See technical note TN-58-01.

NEW MICRON SYNCHRONOUS SRAMs

The new Micron synchronous SRAMs comprise two configurations, each having four versions. The configurations are 32K x 36 and 64K x 18. The versions are summarized in Table 1. Interleaved burst sequence parts (B2 and C4 versions) are ideal for 486 and Pentium™ non-pipelined and pipelined applications. Linear burst sequence parts (M1 and A6 versions) are ideal for PowerPC™ and 680X0 non-pipelined and pipelined applications. These four versions all use BYTE WRITE inputs rather than byte enable inputs. This enables them to functionally replace 32K x 9 synchronous burst SRAMs. Hence, any cache controllers or chipsets that can use the 32K x 9 devices will function with these four 32K x 36 devices from Micron.

32K DEEP CACHE SYSTEMS WITH BURST

Zero wait state performance can be achieved in fast systems (bus speeds of 50 MHz and above) only by using synchronous burst SRAMs or multiple banks of fast SRAMs with extremely fast control logic. The latter solution will at least double the minimum cache size because a minimum of two banks is required. Also, buffers are generally added in the dual bank solution because bus loading is doubled, hence more timing pressure falls upon the SRAMs and control logic which inevitably makes both more costly.

Synchronous burst SRAMs available at a 32K depth provide the easiest solution to the zero wait state dilemma. If a larger cache size is needed, they provide the option of depth expansion or using the additional parts as a second set of associativity. Studies have shown that many new software applications benefit as much or more from partitioning the cache into the two-way set associative architecture as compared to doubling the direct-mapped cache size. In other words, a 64K x 72 two-way set associative cache will perform as well or better than a 128K x 72 direct-mapped cache. Although the two-way cache is more complex to control, only half the memory is needed for a given performance target. The multiple bank SRAM solution for a two-way set design results in too much bus loading and is therefore not a practical option. In contrast, two 32K x 72 sets of synchronous burst SRAMs with each set comprised of two 32K x 36 devices can be implemented with minimal bus loading and board space.

The available 32K deep synchronous burst SRAM solutions in the industry are (or will be) 32K x 9, 32K x 18 and 32K x 36. Table 2 compares several key considerations. Since no 3.3V x9 and x18 devices have been announced, the 5V versions are used for comparison. The 32K x 36 3.3V SRAM is the clear winner in every category. The power dissipation in a 5V system using 32K x 36 devices includes the power dissipated by the 5V to 3.3V linear regulator which is needed if 3.3V is not available anywhere. The regulator adds less than 0.4 square inches more board area than listed in Table 2. This still results in the least area used. None of the cases include I/O power.

Table 1
MICRON SYNCHRONOUS SRAM VERSIONS

Part Number	Features
MT58LC32K36B2 MT58LC64K18B2	Byte Writes, Interleaved Burst
MT58LC32K36C4 MT58LC64K18C4	Byte Writes, Interleaved Burst Output Registers, Write-Through
MT58LC32K36M1 MT58LC64K18M1	Byte Writes, Linear Burst
MT58LC32K36A6 MT58LC64K18A6	Byte Writes, Linear Burst Output Registers, Write-Through

Table 2
32K x 72 DIRECT-MAPPED CACHE COMPARISON

	32K x 9	32K x 18	32K x 36
Quantity for 32K x 72	8	4	2
SRAM Voltage (V)	5	5	3.3
Board area (sq. in.)	3.86	2.53	1.10
Address loading (pF)	24	16	8
Data loading (pF)	8	6	6
Power in 5V System 66 MHz (W)	7.0	5.3	2.5
Power in 3.3V System 66 MHz (W)	n/a	n/a	1.65
Power in 5V System 50 MHz (W)	5.8 (est)	4.3	2.2
Maximum height (mils)	180	180	63

FUNCTIONAL DIFFERENCES

There are almost no differences in functionality between the various 32K deep devices listed in Table 2. The 32K x 18 and 32K x 36 devices both use BYTE WRITE signals. This means that four 32K x 9 devices may be replaced by two 32K x 18 devices or one 32K x 36 device. Any of these alternatives appear the same to cache control logic. The only functional difference lies within the $\overline{ADSP}$ /$\overline{CE}$ logic within the device. The 32K x 18 and 32K x 36, because they are newer devices, benefit from lessons learned in systems employing 32K x 9 parts. The $\overline{ADSP}$ signal (which is typically fed directly from the microprocessor address/data strobe) is gated by $\overline{CE}$ in the new wider devices. This permits address pipelining to function correctly, whereas in systems built using 32K x 9 devices, this becomes awkward.

For example, assume that the cache controller discovers an L2 cache READ miss. The controller initiates a cache line fill from main memory. $\overline{ADSC}$ is used to latch in the address to the SRAM. While this fill is in progress, there is no reason to tie up the address bus since the main memory controller knows where data is needed from and the SRAM knows where it is going. The cache controller can issue a "next address" command to the microprocessor and begin the tag hit/miss comparison of the new address while the fill is still in progress. This potentially eliminates wait states when the system is ready to proceed with the next bus operation. A problem can arise using 32K x 9 SRAMs when the next address is requested because the microprocessor will issue a new $\overline{ADSP}$ and address simultaneously. Since there is no way to block this command from that SRAM, the cache fill in progress would be terminated by the new $\overline{ADSP}$ command.

The newer SRAMs (32K x 18 and 32K x 36) address this problem by the extra gate shown in Figure 1. This extra gate intercepts $\overline{ADSP}$ before propagating inside the chip and conditions it with $\overline{CE}$. Figure 1 actually shows the 32K x 36 although the logic is independent of the device width. Also shown in Figure 1 are the additional chip enables in the 32K x 36, which will be addressed later. The cache controller can simply take $\overline{CE}$ HIGH during the fill, which will block $\overline{ADSP}$ from terminating the fill in progress. In systems not utilizing this extra functionality, the extra gate does no harm and introduces no functional incompatibilities with existing designs.

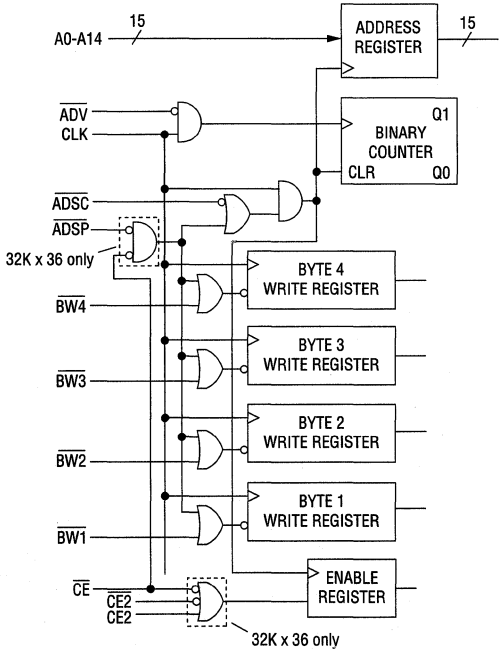

Figure 1
DIFFERENCE BETWEEN 32K x 9 AND 32K x 36

VOLTAGE CONSIDERATIONS

The electronics industry is well into the transition from 5V to 3.3V devices. High-speed (hence, high-power) requirements in microprocessors have made them very difficult to design at 5V. This is the main reason for the new 3.3V microprocessors such as Pentium, Alpha, PowerPC, 680X0, 486, etc. With the steady increase in system speed, there has also been a steady increase in SRAM power dissipation. The transition to 3.3V provides welcome relief—power dissipation is less than half in 3.3V devices compared to 5V devices with identical speed. This enables devices such as the 32K x 36 to be placed into the space-efficient TQFP without requiring expensive thermal management.

The new Micron devices obviously function in systems which are 3.3V only. However, they also function correctly in mixed voltage systems (5V and 3.3V both present). A single 3.3V supply is needed for all V_{CC} and $V_{CC}Q$ pins. All other I/O pins are 5V tolerant. Hence, 5V CMOS logic may drive inputs to the 32K x 36 and 5V devices may reside on the same data bus with these devices. The data sheets guarantee that no special precautions are required during power-up. For example, if the main power supply is 5V and a secondary 3.3V linear regulator operates from the 5V supply to provide 3.3V to the SRAMs and elsewhere, the 5V logic could present signals to the SRAM before 3.3V is present at its supply pins. Since the 32K x 36 will not be damaged in this condition, costly power supply sequencing is not required in mixed voltage systems.

Another consideration is systems that do not have any 3.3V supplies available. Although at first glance it may seem that only 5V SRAMs should be considered, this may be a hasty judgment. Referring to Table 2, to implement a 32K x 72 cache, two 32K x 36 devices using 1.10 sq. in. of board area are required. If a 3.3V regulator is added, less than 0.4 additional square inches is needed resulting in 1.50 square inches of board area. This is still less board area than four 32K x 18 devices (2.53 sq. in.) and results in less power dissipation than the 32K x 18 devices even with the inherent inefficiency of linear regulation. Since 3.3V regulators are inexpensive, this solution is very cost competitive as well. Once again, the argument about mixed voltage systems apply—the Micron device will accept the 5V I/O levels of the rest of the system. All outputs are 5V TTL-compatible; therefore, two-way data transfer occurs with no translation circuitry required.

The Micron parts can be used in 3.6V systems as well. It is best to set the power supply voltage on the low side of 3.6V. With a reasonable tolerance, both microprocessor and SRAM will operate nominally. For example, at 3.5±0.1V both SRAM and microprocessor will operate within design specifications. In fact, the SRAM will operate slightly faster than data sheet specifications (which are listed for the low voltage and high temperature case).

POWER CONSIDERATIONS

There is a great deal of confusion in the industry about how to accurately predict power and we have all fallen victim to misconceptions at one time or another. The SRAM data sheets from any vendor excludes the current needed to switch the load capacitance from one state to another. The I_{CC} given in the data sheet accounts for everything else. The I_{CC} used in the calculation should be appropriate for the operating conditions; e.g., I_{CC} max is specified for the lowest operating temperature, the highest recommended V_{CC} and has guardband added to it. For actual power, I_{CC} should be looked up from published current versus voltage, temperature and cycle times. See the Micron Technical Note "SRAM Thermal Design Considerations" (TN-05-14) for a derivation of true SRAM power. True SRAM power for Micron synchronous devices is:

$$P = V_{CC}\, I_{CC} + \sum P_{LAC\ (\text{for all outputs that toggle})} + P_{LDC}.$$

The incremental power due to steady-state current flow into or out of the DQ pins (P_{LDC} due to I/O leakage of connected devices) is generally ignored because it is small in systems employing CMOS devices. That extra power would be:

$$P_{LDC} = (V_{CC} - V_{OH})\, I_O\, N_H + V_{OL}\, I_I\, N_L,$$

where V_{OH} is the actual logic HIGH output voltage, I_O is output current on those DQ lines and N_H is the number of DQ lines that are HIGH; V_{OL} is the actual logic LOW voltage, I_I is the resulting input current into the DQ line and N_L is the number of DQ lines that are LOW. Since almost all CMOS devices have I_I or I_O less than 10uA (often 1 or 2uA), this calculation is inconsequential. For example, take the case where 36 outputs are connected to loads having 10uA of leakage. The contribution to device power is :

$$(3.3V - 3.0V)\ 10uA\ (36) = 108uW.$$

With higher leakage, V_{OH} drops and power increases as a result of both increased current and greater voltage drop in the SRAM output driver.

The AC load component is a different matter. For outputs which swing from logic LOW to logic HIGH, each output contributes the following to device power:

$$P_{LAC} = \frac{C_L}{T}\left(V_{CC}\,[V_{OH} - V_{OL}] - 0.5\,[V_{OH}^2 - V_{OL}^2]\right).$$

Assuming a load capacitance (C_L) of 30pF, V_{CC} = +3.3V, clock period (T) of 20ns, dynamic V_{OH} of 3.0V, dynamic V_{OL} of 0.1V, the incremental power for each output that swings

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from LOW to HIGH is 7.6mW. If 36 outputs did this, the output power component of the SRAM would be 274mW. The total power would be:

$$210mA \times 3.3V + 274mW = 0.967W.$$

The HIGH to LOW transition case is less severe:

$$P_{LAC} = \frac{C_L}{T}(0.5\,[V_{OH}^2 - V_{OL}^2]).$$

Using the same load conditions as the logic LOW to logic HIGH example, the resulting AC power for each output that changes from logic HIGH to logic LOW is 6.7mW.

Using the logic LOW to logic HIGH calculated power, the device case temperature is:

$$\begin{aligned} T_C &= T_A + P \times \theta_{CA} \\ &= 70°C + 0.967W \times 19°C/W \\ &= 88°C. \end{aligned}$$

Extra thermal conduction through the 100 leads of the device lowers the θ_{CA} to approximately 19°C/W (this is dependent upon each circuit board design) assuming a small PCB with a ground plane. θ_{CA} is greater when the device is tested in still air with minimal conduction through the device leads but this is not a practical operating mode.

$$\begin{aligned} T_J &= T_A + P \times \theta_{JA} \\ &= 70°C + 0.967W \times 20°C/W \\ &= 89°C \text{ junction temperature} \end{aligned}$$

is less than the 150°C specification limit.

At 66 MHz, the device power with all outputs switching from LOW to HIGH is 1.19W (0.365W I/O power) resulting in a T_C for a device soldered in circuit of 93°C and a T_J of 94°C, assuming 70°C ambient temperature. No specified limits are violated.

DEPTH EXPANSION

Another major advantage of the 32K x 36 synchronous burst SRAMs is the two extra chip enables. The extra active LOW and HIGH chip enables ($\overline{CE2}$, CE2) facilitate expansion from 32K to 64K memory depth without any additional logic. This is illustrated in Figure 2. None of the other 32K deep devices offer this flexibility.

This expandability translates into greater flexibility in PC designs. For example, a 72-bit system which requires either a 256KB or a 512KB cache can be laid out for four 32K x 36 devices and then populated with either two or four devices, depending on the desired cache size—with no board changes and no sockets. The only other upgrade which is that simple is the change from 32K x 18 to 64K x 18. This has several disadvantages by comparison: four devices are needed in either case, the total board area needed is greater than the

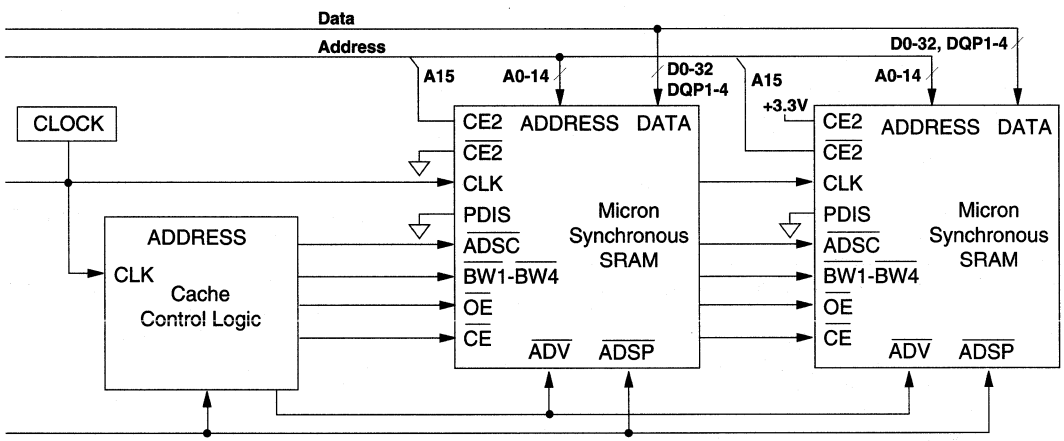


Figure 2
DEPTH EXPANSION FROM 32K x 36 TO 64K x 72

TECHNICAL NOTE

Table 3
64K x 72 DIRECT-MAPPED CACHE COMPARISON

	64K x 18	TQFP Micron 32K x 36	PLCC Micron 64K x 18**
Quantity for 64K x 72	4	4	4
SRAM Voltage (V)	5	3.3	3.3
Board area (sq. in.)	5.06	4.40	5.06
Address loading (pF)	20	16	16
Data loading (pF)	8	12	6
Power in 5V System 66 MHz (W)	7.2	3.4*	4.1*
Power in 3.3V System 66 MHz (W)	n/a	2.2	2.6
Power in 3.3V System 50 MHz (W)	n/a	1.8	2.2
Maximum height (mils)	180	63	180

* Micron device power at 5V includes power dissipated by 3.3V regulator
** Also available in a 100-pin TQFP

32K x 36 devices (and greater still if sockets are required), power dissipation is higher and two separate part types must be stocked by the manufacturer instead of just one. Table 2 compares the 32K x 18 solution to the 32K x 36 assuming that sockets are not required. Table 3 compares the 64K x 72 cache configuration using four 32K x 36 devices versus four 64K x 18 devices. The Micron 64K x 18 solution is also shown for completeness. The one advantage that the 64K x 18 solution does offer is lower data bus loading, although the difference is small. In all other criteria, the 32K x 36 is a superior solution. Although it is clear why the 3.3V 32K x 36 results in lower power than the 5V 64K x 18, it may not be clear why the 32K x 36 system has lower power than the 3.3V 64K x 18. The reason is that only two of the four 32K x 36 devices are active at one time. At 66 MHz, the active current is 250mA but the standby current is only 85mA with clock running and all inputs toggling. By contrast, the four 64K x 18 devices from Micron would each require 200mA. The 5V competing parts require 360mA at the higher voltage.

SUMMARY

The new family of Micron Synchronous SRAMs provides the optimal solution for high-performance cache systems. 3.3V operation with 5V-tolerant I/O affords these devices flexibility to operate in any system with either 3.3V or 5V (or function with both types of devices) while dissipating less power than other alternatives. Caches of 32K depth can be created using the 32K x 36 devices and result in the lowest board space, loading and power requirements of any alternative. Systems requiring the flexibility of cache depth doubling can also be satisfied with the 32K x 36 devices using the extra available chip enables incorporated into the device. The resulting 64K deep cache is still more efficient than designs using the 5V 64K x 18 devices.

TECHNICAL NOTE

SYNCBURST SRAMs IN ASYNCHRONOUS DESIGNS

INTRODUCTION

The 32K x 36 SyncBurst SRAM is taking the world by storm. It is emerging as the synchronous SRAM of choice in secondary cache designs, offering a small footprint, low-loading, high-performance cache data SRAM solution. A number of questions have recently been asked by individuals who need the wide architecture yet use the device more like a conventional asynchronous SRAM in noncache applications. This article addresses the latter desire, with a discussion of basic device operation in synchronous systems provided as background information.

SYNCHRONOUS BURST SRAM SYSTEM OPERATION

Although designed specifically for use in microprocessor secondary cache, the Micron SyncBurst SRAM is by no means restricted to that function. Microprocessors such as the Pentium™ and PowerPC™ have two distinct modes of external bus operation: normal and burst. Normal bus operation consists of a two-clock-cycle external bus access. In the first cycle (labeled as T1), address and control signals are set up. By the end of the next cycle (T2), the bus operation completes and a new external bus cycle may begin (Figure 1). The microprocessor bus is synchronous. During a READ cycle (at the end of T2), data is registered into the microprocessor at the rising edge of the system clock. During a WRITE cycle, data is made available to the memory device such that it can be registered at the end of T2. One of the many synchronous SRAM advantages is that WRITE pulses need not be generated. This advantage increases as bus frequency increases. Control signals are supplied at one clock's rising edge; data is supplied at the next rising edge.

Burst bus operation takes a shortcut by executing four consecutive external bus cycles. The first cycle requires the same setup and completion (T1 and T2). The next three cycles operate without the setup cycle (Figure 2). This is done by defining the sequence of addresses that follow the first issued address. PowerPC and Pentium differ in address sequence (PowerPC uses a linear burst sequence whereas Pentium uses an interleaved sequence) but do not differ in the total burst length of four bus accesses. The Micron SyncBurst SRAM supports both linear and interleaved burst sequences by incorporating a two-bit burst counter that tracks the internal-address generation of the target microprocessor. Note in Figure 2 that some microprocessors, such as Intel's 486, attempt to alter the address to reflect the burst sequence (only the two least significant external address lines change) but they don't do this fast enough to be useful. An SRAM without the burst counter

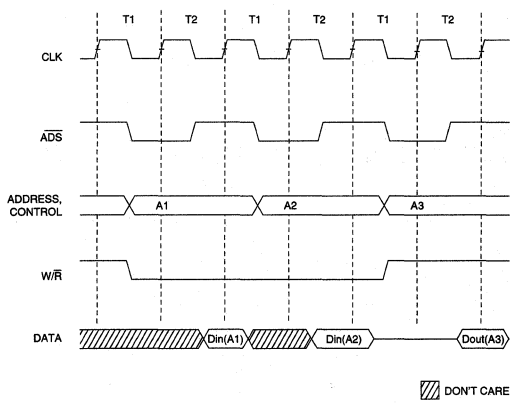


Figure 1
TWO CYCLE MICROPROCESSOR BUS OPERATION

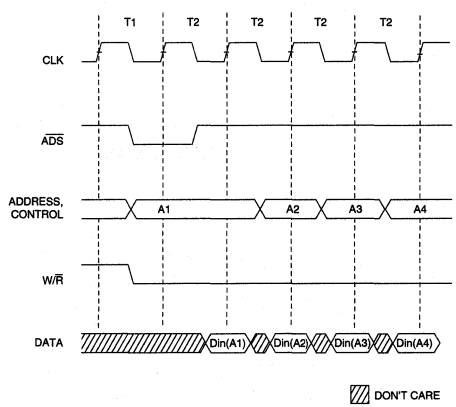


Figure 2
BURST CYCLE OPERATION

must receive the lower two address bits long before the microprocessor can supply them. This requires logic external to the microprocessor and SRAM, resulting in additional system delays. The SyncBurst SRAM adds no such delay.

The foregoing described just one of several SyncBurst SRAM advantages. Cache controller ASICs (application-specific integrated circuits) do not operate efficiently if they use the bus during WRITE cycles in the same manner as microprocessors. If address and data are both known, sending them simultaneously to the SRAM (this is called an EARLY WRITE) is better than having data follow the address by one clock cycle as the microprocessor does (this is called a LATE WRITE). The SyncBurst SRAM supports both EARLY WRITE (using $\overline{ADSC}$ as the address control signal) and LATE WRITE (using $\overline{ADSP}$ as the address control signal) so that both microprocessor and cache controller cycles are optimized. Figure 3 shows the difference between LATE WRITE ($\overline{ADSP}$-controlled) and EARLY WRITE ($\overline{ADSC}$-controlled). Note that EARLY WRITE cycles permit a new address to be used once every clock whereas LATE WRITE cycles only permit WRITEs to new addresses every second clock. READ cycles can actually be performed at the rate of one new access per clock regardless of being $\overline{ADSP}$ or $\overline{ADSC}$ initiated, although when using microprocessors such as PowerPC and Pentium the microprocessor is the limiting factor (recall the two-cycle normal bus operation).

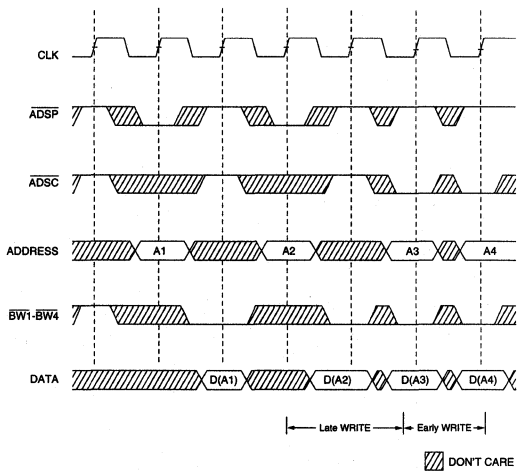


Figure 3
LATE WRITE AND EARLY WRITE IN THE SYNCBURST SRAM

SYSTEMS WITHOUT MICROPROCESSORS

ASICs "want" to run synchronously. If their internal design is very small, synchronicity is less critical. But if the ASIC design is large enough to need an external SRAM, synchronicity becomes important to the system design. The first step in the design process is to "synchronize" the ASIC to the "outside world." This involves the use of registers or latches to make the interface signals appear to be synchronous whether or not they are. If the SRAM that interfaces with the ASIC is synchronous, then the task is already done. The $\overline{OE}$ signal is the only one in Micron's 32K x 36/64K x 18 family that is asynchronous, but it can easily be treated as synchronous. Figure 4 illustrates a low-pin-count circuit while Figure 5 shows the timing relationships between the ASIC and SyncBurst SRAM during READ and WRITE cycles. Minimal control signals are used in this application. $\overline{OE}$ is toggled on CLK rising edges whereas the synchronous signals are toggled on CLK falling edges. The latter ensures that very generous setup and hold times are provided to the SyncBurst SRAM. In this example, the transition from READ cycles to WRITE cycles requires a dummy READ with $\overline{OE}$ HIGH to allow the bus to make room for input data. The gap is apparent on the data bus at the transition from WRITE cycles to READ cycles.

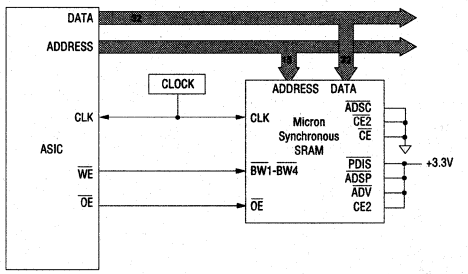


Figure 4
MINIMUM ASIC SYNCHRONOUS INTERFACE, $\overline{OE}$-CONTROLLED

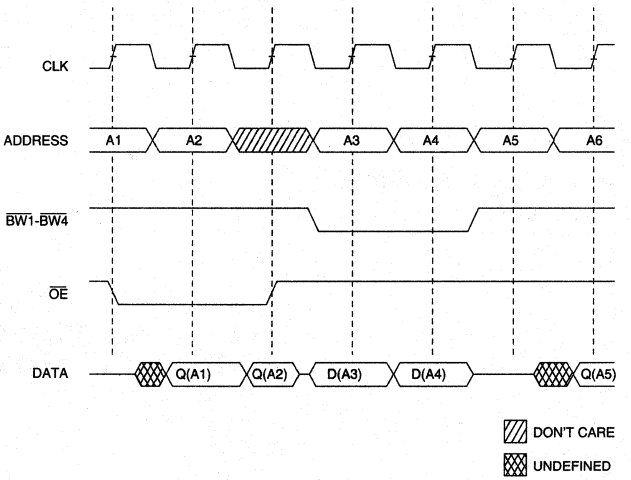


Figure 5
SYNCBURST SRAM TIMING IN ASIC APPLICATION

NEW TECHNICAL NOTE

USING SYNCBURST SRAMS IN PLACE OF ASYNCHRONOUS SRAMS

Whenever a clock signal is available, SyncBurst SRAMs can be used in place of asynchronous SRAMs through two distinct approaches. The first involves a design similar to the one illustrated in Figure 4. In this case, synchronous SRAMs are desired but without additional ASIC control pins that aren't needed for an asynchronous SRAM solution. Often, solutions are I/O-bound and not gate-bound; therefore, extra pins can add cost to a product. The second approach involves the creation of a signal internal to the ASIC that helps speed up the bus frequency when READ and WRITE cycles are intermixed frequently.

The only requirement for this first method to work is that a clock signal (CLK) must be available. The logic connections of control signals that are static are shown in Figure 6. PDIS (parity disable) is shown HIGH for a 32-bit design but could have been LOW for a 36-bit design. Addresses are generated by the ASIC at the falling edges of CLK. The only signals that must be controlled are: $\overline{BW1}$ through $\overline{BW4}$ and $\overline{CE}$. $\overline{OE}$ can always be LOW if bus contention with other devices is not a concern. The $\overline{BW}$ signals can all be driven from a single ASIC pin if only full bus width operations will be performed. A minor performance reduction will be experienced using this control structure. One idle cycle will appear on the data bus (Figure 7) every time a transition from WRITE to READ (and not vice-versa) occurs. If many WRITE cycles occur consecutively followed by many consecutive READ cycles, the performance change will be barely noticeable. If the system constantly changes between READ and WRITE cycles, the bus speed will appear to be two thirds of the clock frequency. The actual number of control signals from the ASIC is the same as in the Figure 4 design solution. The difference lies only in which signals are selected. The Figure 6 solution is easier to implement because all ASIC outputs are produced at the falling edge of CLOCK whereas the Figure 4 solution mixes edges (due to $\overline{OE}$ control).

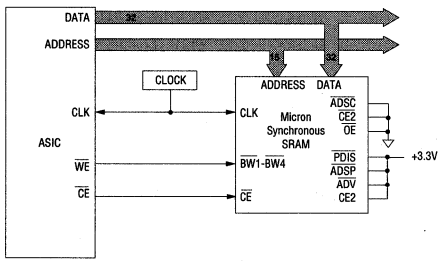


Figure 6
MINIMUM ASIC SYNCHRONOUS INTERFACE, $\overline{CE}$-CONTROLLED

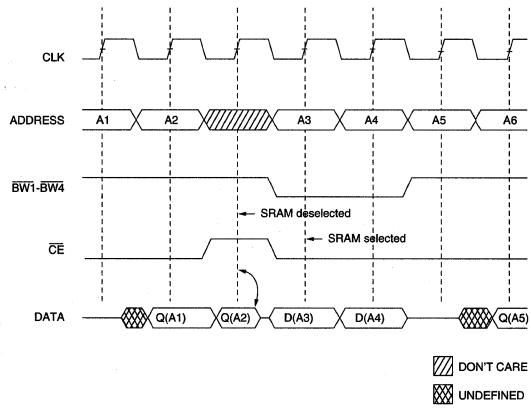


Figure 7
SYNCBURST SRAM TIMING, $\overline{CE}$-CONTROLLED ASIC APPLICATION

TREATING SYNCBURST SRAMS LIKE ASYNCHRONOUS SRAMS

Some designs can't tolerate any idle cycles on the bus. This can still be accommodated using the SyncBurst SRAM. There are two keys to making this work. The first is to ensure that the SyncBurst SRAM access time is sufficient. It will not have a full clock cycle to output data to the ASIC. The second is to design the ASIC such that it can register the input data before the rising edge of CLK. The bus must be clear before the next CLK rising edge so that either a READ or a WRITE may occur once per clock. This can be done by using extraneous gate delays with inversion from the falling edge of CLK in order to create an internal reference for registering input data inside the ASIC (see ICLK, Figure 8). $\overline{OE}$ transitions must occur such that the SRAM tristates its data outputs before the ASIC drives the data bus to allow contention-free read-write transitions.

Figure 8 shows the relationship between signals. The critical path is the transition from READ to WRITE cycles: data must be registered into the ASIC before it can output data; $\overline{OE}$ must be timed to tristate the data bus in time but not so soon that the data has insufficient time to be registered. This is clearly a more difficult internal ASIC design because the timing for the ASIC output signals is much more critical than in the previous examples. Care must be taken to account for maximum and minimum propagation delays inside the ASIC and also in the SRAM, particularly in the High-Z and Low-Z parameters. However, if idle cycles are to be avoided in the system, this does provide a means for accomplishing that goal with no more control pins than required by asynchronous SRAMs.

SUMMARY

The robustness of control inputs in the SyncBurst SRAM make it versatile enough for use in almost any application. This article demonstrates how it may be applied in pin-count sensitive applications and applications which are pin-count sensitive but cannot tolerate data-bus idle cycles. The ASIC design using SyncBurst SRAMs is simplified by having a primarily synchronous external interface and a self-timed write: no timing-critical write pulses need to be generated.

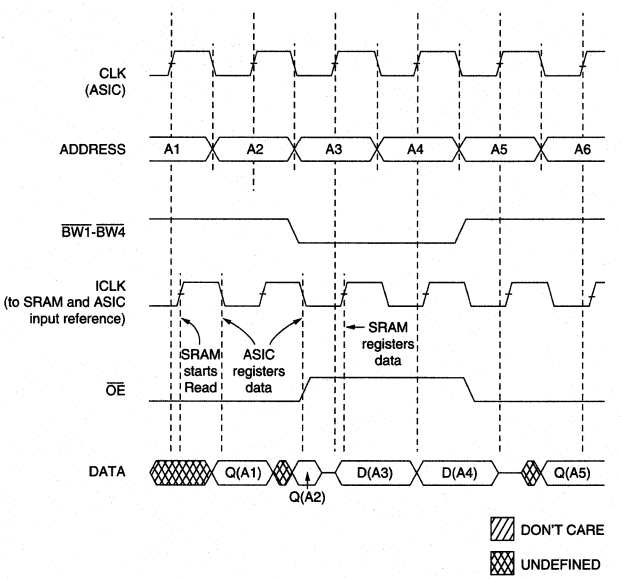


Figure 8
SYNCBURST SRAM TIMING, $\overline{CE}$-CONTROLLED ASIC APPLICATION

NEW TECHNICAL NOTE

MICRON
SEMICONDUCTOR, INC.

OVERVIEW

Product reliability is a product's ability to function within given performance limits, under specified operating conditions over time. This section contains a brief overview of some of the issues that affect the reliability of IC devices and briefly describes Micron's reliability program.

For a more in-depth discussion of reliability, please refer to Micron's Quality/Reliability literature.

RELIABILITY GOALS

When we discuss reliability goals of semiconductor ICs, we typically refer to the traditional reliability curve of component life. The reliability curve, or "bathtub curve," appears below, where h(t) is the hazard rate or the probability of a component failing at t_0+1 in time if it has survived at time t_0.

The reliability curve in Figure 1 is divided into three segments: infant mortality, random failures and wearout. The term "infant mortality" refers to those ICs that would fail early in their lives due to manufacturing defects. To screen out such failures, Micron evaluates all our products using intelligent burn-in. This unique AMBYX® intelligent burn-in/test system developed by Micron is described in the following section.

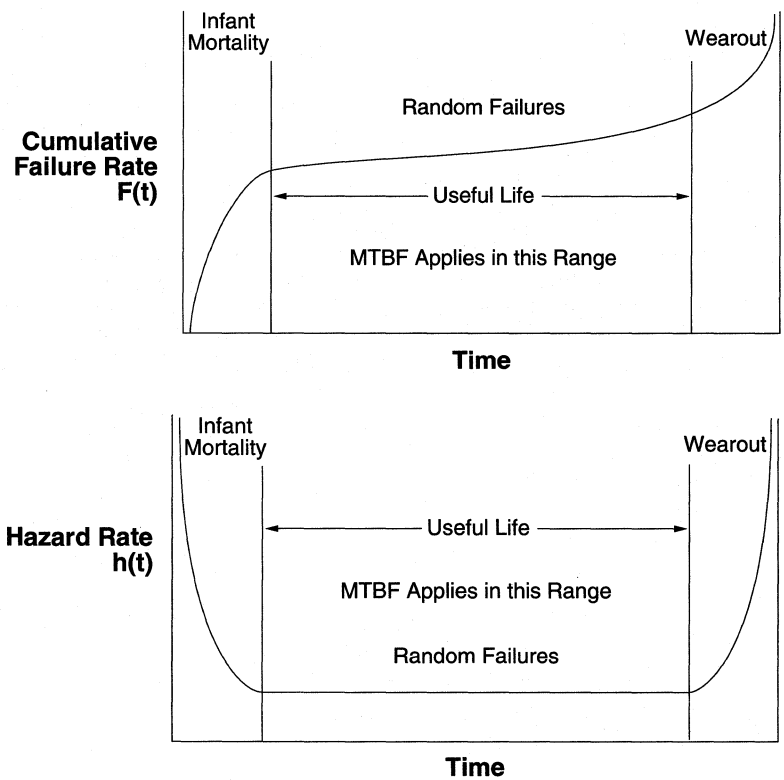


Figure 1
RELIABILITY CURVE

MICRON'S AMBYX® INTELLIGENT BURN-IN AND TEST SYSTEM

Burn-in refers to the process of accelerating failures that occur during the infant mortality phase of component life to remove the inherently weaker devices. The process has been regarded as critical for ensuring product reliability since the beginning of the semiconductor industry. To effectively screen out infant mortalities, Micron believes it is critical to functionally test devices several times during the burn-in cycle without removing them from the burn-in oven. In 1986, when we were unable to find a system that met our requirements, we introduced the concept of "intelligent" burn-in and developed the AMBYX® intelligent burn-in and test system. Today, we use AMBYX to test every component product we make.

With AMBYX, we can determine if the failure rate curves of individual product lots reach the random failure region of the bathtub curve by the end of the burn-in cycle. We subject product lots that do not exhibit a stable failure rate to additional burn-in. This burn-in flow also brings to our attention the slightest variation in a product's failure rate.

Since AMBYX allows us to test devices for functionality without removing them from the burn-in oven, we effectively eliminate failures resulting from handling, thereby minimizing "noise" from the test results. During the test phase, output produced by the devices under test is compared to the pattern expected. If a discrepancy occurs, AMBYX records the failure and provides the bit address, device address, board address, temperature, V_{CC} voltage, test pattern and time set.

During the burn-in cycle itself, devices are functionally tested in four intervals. The first test begins at room temperature. Then we ramp up the oven to 85°C for more functional testing. This enables us to detect thermal intermittent failures, another unique feature of intelligent burn-in. We conduct the next test at 125°C — any device that does not pass this sequence is eliminated. As the burn-in process continues, the devices are dynamically stressed at high temperature and voltage for a given number of hours. At the end of this period, we functionally test all devices again, followed by another burn-in cycle and further tests. This sequence is repeated four times on every device in every production lot.

These test results allow us to identify individual failures after each burn-in cycle. Figure 2 illustrates how the four burn-in and test cycles flow. The typical test results shown make up the first portion of the bathtub curve of component reliability.

There are two important reasons why Micron conducts the last two burn-in and test periods (or "quarters") at lower V_{CC} than the first two portions. First, we want the several million device hours that we accumulate weekly on production lots to be conducted at stress conditions identical to the conditions for the extended high-temperature-operating-life (HTOL) test used by IC manufacturers to compute random field failure rates. Second, we want to be sure we are not introducing new failure modes unrelated to normal wearout, such as VOS, by testing them at extremely elevated conditions.

Control charts, such as the one shown in Figure 3, alert us to trends in lot failure rates. When we detect an upward trend in a failure rate, we correlate the lots that need additional burn-in with all the variables that might be influencing the increased rate.

The overall benefits of intelligent burn-in are wide ranging. Intelligent burn-in allows us to identify early-life failures and failure mechanisms as they would actually occur in customer applications. It also allows us to identify problem lots that, if undetected, could contribute substantially to infant mortalities.

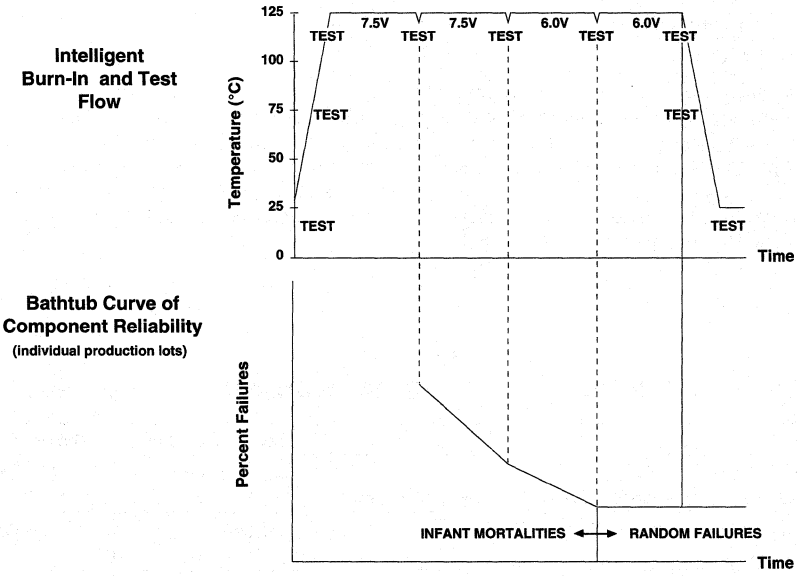


Figure 2
AMBYX BURN-IN/TEST FLOW AND TEST RESULTS

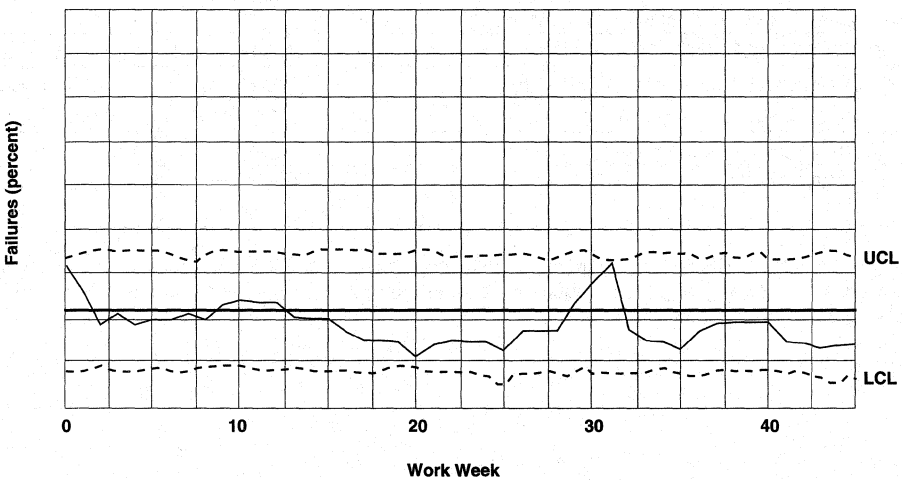


Figure 3
AMBYX FOURTH QUARTER FAILURES

RELIABILITY

ENVIRONMENTAL PROCESS MONITOR PROGRAM

Micron's environmental process monitor (EPM) program is designed to ensure the reliability of our standard products. Under this program, we subject weekly samples of our various product and package types to a battery of stress tests.

During these tests, we stress the devices for many hours under conditions designed to simulate years of normal field use. We then apply equations derived from intricate engineering models to the data collected from the accelerated tests. From these calculations, we are able to predict failure rates under normal use. Table 1 shows the conditions for these tests, known as environmental stress tests. The EPM program described in Table 1 is for Micron's 1 Meg SRAM.

Table 1
SAMPLE ENVIRONMENTAL PROCESS MONITOR – 1 MEG SRAM

TEST NAME AND DESCRIPTION	TEST DURATION	BIWEEKLY SAMPLE SIZE
HIGH TEMPERATURE OPERATING LIFE (125°C, 6V, Checkerboard and Checkerboard-Complement Pattern)	1,008 Hours	100 Devices
LOW TEMPERATURE LIFE (-25°C, 7V, Dynamic Bias)	1,008 Hours	5 Devices
TEMPERATURE AND HUMIDITY (85°C, 85% RH, 5.5V, Alternating Bias)	1,008 Hours	50 Devices
AUTOCLAVE (121°C, 100% RH, 15 PSI, No Bias)	288 Hours	25 Devices
TEMPERATURE CYCLE (-40°C for 15 minutes, +85°C for 15 min, air to air)	1,000 Cycles	50 Devices
THERMAL SHOCK (-55°C for 5 minutes, +125°C for 5 minutes, liquid to liquid)	700 Cycles	10 Devices
HIGH TEMPERATURE STORAGE (150°C, No Bias)	1,008 Hours	50 Devices
HIGH TEMPERATURE STEADY STATE (150°C, 6.5V)	1,008 Hours	5 Devices
ELECTROSTATIC DISCHARGE (+ and -)	MIL-STD-3015	40 Devices
V_{CC} LATCH-UP (Minimum Voltage, 25°C)	—	10 Devices
SYSTEM SOFT ERROR (5V, 30ns)	168 Hours	190 Devices

NOTE: Samples used in the EPM program are taken from five different lots at finished goods. Before being subjected to environmental testing, all surface-mount products are run twice through an infrared (IR) reflow furnace, reaching a peak temperature of 240°C.

FAILURE RATE CALCULATION

The failure rate during the useful life of a device is expressed as either the percentage of failures per thousand device hours or as failures in time, per billion device hours (FITs), and is calculated as follows:

$$\text{Failure Rate} = \frac{Pn}{\text{Device hours at accelerated environments} \times \text{AF relative to typical operating environment}}$$

where: Pn = Poisson Statistic (at a given confidence level). For the data above, one device failure, Pn at at 60 percent confidence level = 2.022.

Device hours = sample size multiplied by test time (in hours) From Table 2, device hours = (2,294 x 168) + (2,294 x 168) + (2,292 x 168) + (2,292 x 168) + (2,292 x 168) + (2,290 x 168) = 2,310,672 or 2.311×10^6.

AF = acceleration factor between the stress environment and typical operating conditions. For the 1 Meg SRAM, the acceleration factor between 125°C, 6V (HTOL stress conditions) and 50°C, 5V (typical operating conditions) equals 93. (Calculation of this acceleration factor is described in the following section.)

Thus, the failure rate of the Micron 1 Meg SRAM family is computed as follows:

$$\text{Failure Rate} = \frac{2.022}{(2.311 \times 10^6)\,93} = 9.408 \times 10^{-9}$$

where: total device hours at test conditions = 2.311×10^6. Equivalent device hours at typical use conditions (50°C, 5V Vcc) using an acceleration factor of 93 equals 93 (2.311×10^6) = 215×10^6.

To translate this failure rate for the 1 Meg SRAM family into percentage failures per thousand device hours, we multiply the failure rate obtained from the equation above by 10^5:

$$\text{Failure Rate} = (9.408 \times 10^{-9}) \times 10^5 = 0.0009408\% \text{ or } 0.0009\% \text{ per 1K device hours}$$

To state the failure rate in FITs, we multiply the failure rate obtained from the equation above by 10^9:

$$\text{Failure Rate} = (9.408 \times 10^{-9}) \times 10^9 = 9.408 \text{ or } 9 \text{ FITs.}$$

Table 2
HIGH TEMPERATURE OPERATING LIFE (HTOL)

Sample No.	168 Hours	336 Hours	504 Hours	672 Hours	840 Hours	1,008 Hours
1	0/0200	0/0200	0/0200	0/0200	0/0200	0/0200
2	0/0200	0/0200	0/0200	0/0200	0/0200	0/0200
3	0/0200	0/0200	0/0200	0/0200	0/0200	0/0200
4	0/0200	0/0200	0/0200	0/0200	0/0200	0/0199
5	0/0200	0/0200	0/0200	0/0200	0/0200	0/0200
6	0/0195	0/0195	0/0195	0/0195	0/0195	0/0195
7	0/0200	1/0200	0/0198	0/0198	0/0198	0/0198
8	0/0200	0/0200	0/0200	0/0200	0/0200	0/0200
9	0/0300	0/0300	0/0300	0/0300	0/0300	0/0299
10	0/0200	0/0200	0/0200	0/0200	0/0200	0/0200
11	0/0199	0/0199	0/0199	0/0199	0/0199	0/0199
Total	0/2294	1/2294	0/2292	0/2292	0/2292	0/2290

Note:
1. Preconditioning: All surface-mount packages are run twice through an infrared (IR) reflow oven, reaching a peak temperature of 240°C.
2. Test conditions: 125°C, 6V Vcc, checkerboards and checkerboard complement pattern for up to 1,008 hours in 168-hour intervals. Devices are tested for functionality after each interval.
3. Failure rate at 60 percent confidence level: Typical operating conditions (5V, 50°C) = 0.0009% per 1K device hours or 9 FITs (failures in time per billion device hours).

ACCELERATION FACTOR CALCULATION

Again, using the 1 Meg SRAM as our example, the acceleration factor between high temperature operating life stress conditions (125°C, 6V) and typical operating conditions (50°C, 5V) is computed using the following models:

ACCELERATION FACTOR DUE TO TEMPERATURE STRESS

The acceleration factor due to temperature stress is computed using the Arrhenius equation, which is stated as follows:

$$AF_T = e^{\frac{E_a}{k}\left[\frac{1}{T_O} - \frac{1}{T_S}\right]}$$

where: k = Boltzmann's constant, which is equal to 8.617×10^{-5} eV/K.

T_O and T_S = typical operating and stress temperatures, respectively, in kelvins.

E_a = activation energy in eV. (For oxide defects, which is the most common failure mechanism for the 1 Meg SRAM used in our example. The activation energy is determined to be 0.3eV.)

Using these values, the temperature acceleration factor between 125°C and 50°C is computed to be 7.622.

ACCELERATION FACTOR DUE TO VOLTAGE STRESS

The acceleration factor due to voltage stress is computed using the following model:

$$AF_V = e^{\beta (V_S - V_O)}$$

where:

v_S and v_O = stress voltage and typical operating voltage, respectively, in volts

β = constant, the value of which was derived experimentally by running several sessions of Micron's intelligent burn-in test sequence at different voltages on large numbers of the device. (For the 1 Meg SRAM used in our example, β equals 2.5).

Thus, the voltage acceleration factor for the 1 Meg SRAM between 6V (stress condition) and 5V (typical operating condition) is computed to be 12.182.

Finally, the overall acceleration factor due to temperature and voltage stress is calculated as the product of the two respective acceleration factors or:

$$\begin{aligned} AF_{overall} &= AF_{temperature} \times AF_{voltage} \\ &= 7.622 \times 12.182 \\ &= 93 \end{aligned}$$

OUTGOING PRODUCT QUALITY

Before being sent to our finished goods area, where products are prepared for shipping, a special unit within the quality assurance department takes a sample from each production lot. These samples are subjected to visual and electrical testing to measure the acceptable quality level (AQL) of all outgoing product. Test flows for new products that have not met required production volume and ppm levels are more comprehensive than for mature products. Over a period of time, as a product matures, the objective is to eliminate those tests which devices never fail. AQL testing, although it is performed on only a small percentage of each product, is much more exhaustive. Conducted at spec conditions without guardband for every known timing, pattern and background, it is a sanity check on the production test flow. Its purpose is to detect subtle shifts in defect mechanisms which the production test flow may not catch.

Visual testing for mechanical defects consists of visual inspection of the sample devices for any physical irregularities that could negatively affect device performance. If a sample device is found to have, for example, a bent lead, a package irregularity or excess solder, the entire lot is returned to our test area for a 100 percent visual inspection.

Electrical testing of the sample devices is performed using automatic test equipment (ATE) systems. Testing is conducted at 0°C, or room temperature (~25°C) and at 70°C. Should an electrical failure occur, a quality assurance engineer further evaluates the failing device. After completing this analysis, the quality assurance engineer determines which production monitor/test should have caught the failure, and the devices are retested beginning at that point in the test flow. These are important steps to preserve the integrity of our test process.

AUTOMATED DATA CAPTURE AND ANALYSIS

Micron has developed a sophisticated data capture and analysis system with a computer network tailored to the needs of quality IC manufacturing. Figure 4 shows the various functional areas that provide the input to our VAX data bases.

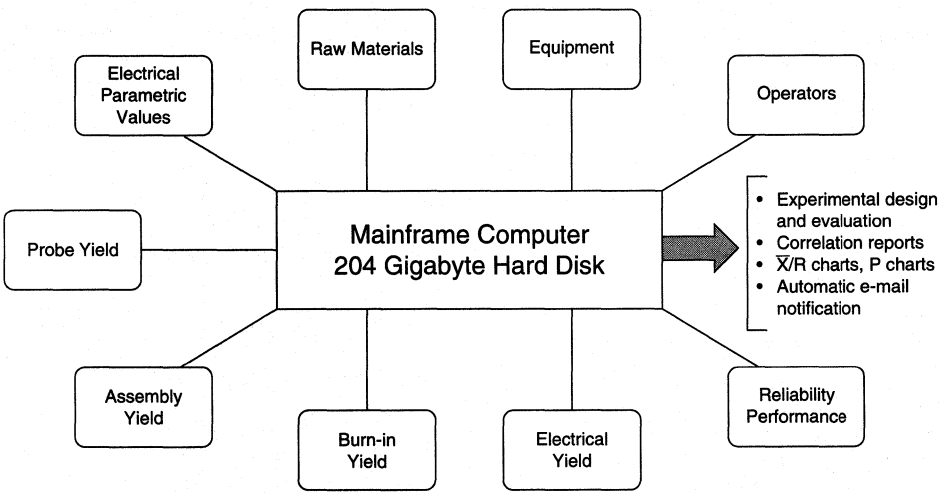


Figure 4
STATISTICAL CORRELATION

DATA CAPTURE

Automated, real-time data capture makes real-time charting ($\overline{X}$ and R charts, etc.) of all critical operations and processes possible and ensures that appropriate personnel know of any unexpected variation on a timely basis. As production lots move through each manufacturing step, detailed information (including step number, lot number, machine number, date/time, and operator number) is entered into the production data base. Automated, highly-programmable measurement systems capture a host of parameters associated with equipment, on-line process material and environmental variables.

STATISTICAL TECHNIQUES AND TOOLS

By using highly flexible, on-line data extraction programs, system users can tap this vast data base and design their own correlation and trend analyses. Because we can correlate process variables to product performance, we can make on-line projections of the quality of our finished product for a given lot or process run. In addition, we can estimate the impact of process improvements on quality well in advance and can make the impact of process deviations more visible to our engineers. This approach allows us to model yield and quality parameters based on on-line parameters. We then use this model to predict the final product results through the following means:

GROUP SUMMARIES

Summaries, which provide the means and standard deviations of user-defined parametrics, enable system users to compare the parametric values of production lots as well as special engineering lots.

TREND ANALYSIS

Trend charts are routinely generated for critical parameters. System users can plot the means and ranges of any probe or parametric data captured throughout the manufacturing process.

CORRELATION ANALYSIS

Correlation analysis can be performed on any combination of factors, such as equipment, masks or electrical parameters. One report, regularly produced and disseminated to key personnel, takes two groups of lots (one with a high failure rate, the other with a low failure rate) and identifies all the pieces of equipment that are common to one or the other group. The report quickly alerts us to any correlation between a lot with a high failure rate and particular piece(s) of equipment in the wafer fabrication or assembly areas.

Another regularly produced report analyzes a user-selected set of database parametrics against an index, such as manufacturing yield. Lots are divided into three subgroups (upper yielding, middle yielding and lower yielding). The report then correlates the yields with all electrical parametric values taken on individual lots at wafer sort. It helps us determine which processing step may have caused the yields to vary among the three subgroups.

STATISTICAL PROCESS CONTROL (SPC) CHARTS

Micron employs SPC control charts throughout the company to monitor and evaluate critical process parameters, such as critical dimensions (CDs), oxide thickness, chemical vapor depositions (CVDs), particle counts, temperature and humidity, and many other critical process and product quality parameters.

OVERLAYS OR WAFER MAPS

Maps, which are produced for all wafers during probe, show various parameters as a function of position on the wafer and are very useful for problem isolation. Maps may be analyzed individually or in groups. For example, wafers from an entire lot may be analyzed in relation to one particular parameter.

RS/1 DISCOVER/EXPLORE/MULREG

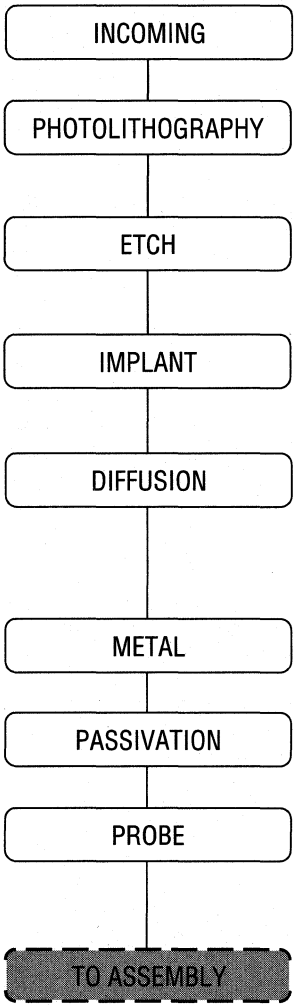
This analysis software is used for experimental design and evaluation of results. The statistical approach supported by this software (t tests, ANOVA tables, multiregression analysis, etc.) has proven invaluable in reducing time expended for product development and trouble-shooting. It is also used to determine the relationships between process output, probe and parametric data. Using multiregression analysis, for example, we are able to determine the relationship between L effective and CD dimensions to the speed of a device.

The use of automation in data capture, analysis and feedback greatly enhances the flexibility and speed with which we can view all aspects of the manufacturing process. This effective data analysis and feedback system helps to reduce parametric deviations, improve margin to specifications, increase manufacturing yields and provide more accurate fabrication output planning.

GAUGE CAPABILITY STUDIES

These studies are performed on both new and existing equipment. Gauge studies help us understand the cause of variation in a measurement process and determine the amount of variation in the system.

FABRICATION*



Incoming
Verification that the starting material is clean, uniform and compliant with all requirements. Each wafer receives an individual laser scribe for total product traceability.

Photolithography
Wafers are coated with a layer of light-sensitive photoresist. Specified sections of the wafer are exposed by projecting ultraviolet light onto the wafer through a mask. The exposed photoresist hardens and becomes impervious to etchants.

Etch
The areas of the wafer not protected by the exposed photoresist are removed by either plasma (dry etch) or acid (wet etch). The photoresist is then cleaned ("stripped") off of the wafer, leaving a pattern in the exact design of the mask.

Implant
Wafers are bombarded with positively or negatively charged dopant ions, which are implanted into the silicon. This process changes electrical characteristics in selective areas of the silicon. This is called "doping" and forms conductive regions on the wafer.

Diffusion
Silicon dioxide, nitrite and polysilicon layers are formed on the wafer during a number of high-temperature furnace processes. The wafers are exposed to various gases which either react with the silicon, causing it to oxidize and form an SiO_2 layer or react with each other, forming poly and nitrite deposits. These layers are patterned using photolithography and form the layers of the diodes, transistors and capacitors of the circuit. High temperature furnaces are also used to introduce and diffuse dopants into the wafers.

Metal
A thin layer of aluminum or other metal is deposited and patterned, forming interconnections between various regions of the die.

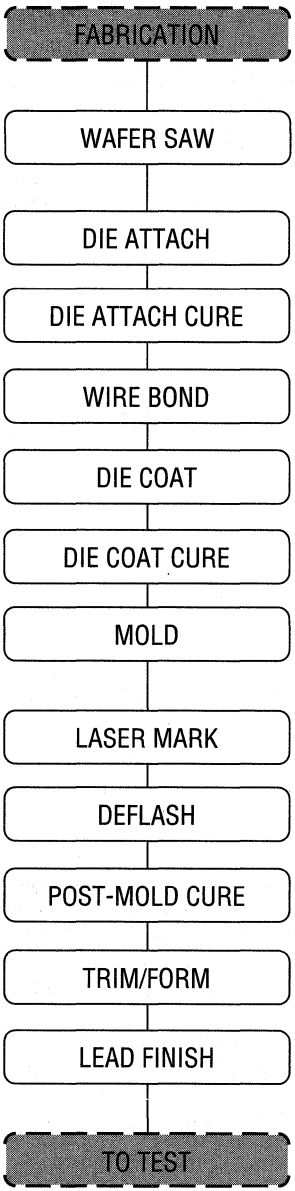
Passivation
The fabrication process is completed by forming a final glass layer on the wafer. This layer protects the circuits from contamination or damage through the testing and packaging process flows.

Probe
When the fabrication process is complete, each wafer consists of many die. Each individual die on the wafer is taken through a series of tests. A computer attached to a probe card tests the die and produces a "wafer map," storing data on each functioning (good) die. All data is collected and stored for each die. Wafer maps are used in assembly to ensure that only good die are packaged.

Assembly (see next page)

*This flow is general and relates to all Micron products.

ASSEMBLY*



Fabrication
Before assembly, incoming raw silicon wafers are processed through a myriad of fabrication steps. This fabrication process yields fully-fabricated wafers containing complete, functioning circuitry in die form. These wafers go to assembly so each individual die may be separated and packaged prior to final testing.

Wafer Saw
Wafers that have finished fab processing and probe are automatically mounted on a carrying film. The wafer is then sawed using an automated, high-speed diamond blade and high-pressure water. This separates each individual die from the others on the wafer without disturbing the carrying film.

Die Attach
With automated pick-and-place equipment, the good die as specified by the probe "wafer map" are removed from the carrier film. Each die is attached to a leadframe with a layer of adhesive.

Die Attach Cure
The die-attached leadframes are cured in an oven for two and one-half hours to fully polymerize the die attach adhesive.

Wire Bond
With high-speed automated equipment, interconnections are made with gold wire the diameter of a human hair. These interconnections are between the aluminum circuit on the die and the lead fingers of the leadframe.

Die Coat
Polyimide die coat is drop-dispensed onto the wirebonded die. The die coat protects the surface of the die during the subsequent encapsulation step.

Die Coat Cure
To fully polymerize the die coat, the die-coated leadframes are cured for six hours in an oven that reaches 265°C.

Mold
A heated mold with a hydraulic press is used to transfer hot thermosetting plastic into mold cavities where the leadframe is placed. This encapsulation protects the die and the interconnections throughout the useful life of the product.

Laser Mark
A laser mark is scribed on the bottom side of the package. This mark is a code used to identify the assembly manufacturing lot.

Deflash
Prior to lead-finish processing, the leadframes are run through chemical baths to remove contaminants. This process is known as deflash.

Post-Mold Cure
Molded leadframes are placed in an oven for four and one-half hours at 175°C to complete the polymerization of the epoxy encapsulant.

Trim/Form
A press with a tool set is used to cut the leadframes, separating the encapsulated die into discrete devices and forming the leads into specified shapes for surface-mount or through-hole applications.

Lead Finish
The leads of each device receive a lead finish of tin/lead solder or tin/lead electroplating to ensure reliable application by the customer. If the leads receive an electroplated rather than solder finish, the lead-finish step is performed prior to trim and form.

Test (see next page)

*This flow is general and relates to all Micron products.

TEST*

ASSEMBLY

PREBURN

BURN-IN

SPEED SORT

MARKING

AMBIENT POSTBURN

SCANNER

VISUAL INSPECTION

AQL

PACKAGING

FINISHED GOODS

Assembly
Fully fabricated silicon wafers reach assembly after each die has been probed to screen out failures. Passing chips are then carried through a number of steps to become individual units in leaded packages.

Preburn
All testing is conducted at 125°C. Parametric tests are performed to detect opens, shorts, and input/output leakage, and to determine whether standby/operating currents are within specified limits. Functional tests include low/high Vcc margin and Vcc bump.

Burn-in*
Micron uses its exclusive AMBYX® intelligent burn-in and test system to screen out infant mortalities. Devices are dynamically burned-in, using checkerboard/checkerboard complement patterns in four intervals under the following conditions: 125°C, 6.5V Vcc for the first three intervals and 125°C, 6V Vcc for the final interval. During temperature ramping from 25° to 85°C and from 85° to 25°C, AMBYX tests for thermal intermittent opens. Devices are also functionally tested at burn-in conditions (125°C, 6.5V) at the beginning of the burn-in cycle to verify that the devices under test are being properly exercised.

Speed Sort
Parametric and functional testing is conducted at 86°C. Parametric tests are performed to detect opens, shorts, and input/output leakage and to determine whether voltage input/output high and low levels and standby/operating currents are within specified limits. Functional tests include low/high Vcc margin, Vcc bump and access tests. Patterns performed include march, scan and address complement. A wide range of test algorithms and data backgrounds are used to verify AC parameters.

Marking
Devices are marked with ink with the following information: year, special process designator, part type, package type and speed grade.

Ambient Postburn
Parametric and functional tests are conducted at 25°C. Parametric tests are performed to detect opens, shorts, and input/output leakage, and to determine whether voltage input/output high and low levels and standby and operating currents are within specified limits. Functional tests include low/high Vcc margin and Vcc bump. A wide range of test algorithms and data backgrounds are used to verify AC parameters.

Scanner
Devices are optically scanned by an automated scanning machine for bent leads, incorrect splay and coplanarity failures. Passing and failing parts are then sorted into appropriate bins.

Visual Inspection
All devices determined functional are visually inspected for cosmetic defects such as bent leads, poor marks, broken packages and poor solder. Defective products are removed and if possible, repaired. Data on the type of defects found is recorded and used for improving the manufacturing processes in both assembly and test.

AQL
A quality assurance monitoring program oversees the electrical and environmental performance of all production lots. New products that have not met required production volume and ppm levels are held at this stage until it is confirmed that electrical and environmental test results meet Micron's requirements.

Packaging
In preparation for shipping, devices may remain in tubes or they may be mechanically placed in tape-and-reel packages for use in automated pick-and-place machines. Moisture-sensitive products (including all tape-and-reel) are dry-packaged in vacuum-sealed bags with a desiccant. Through-hole devices are placed in static-shielded bags.

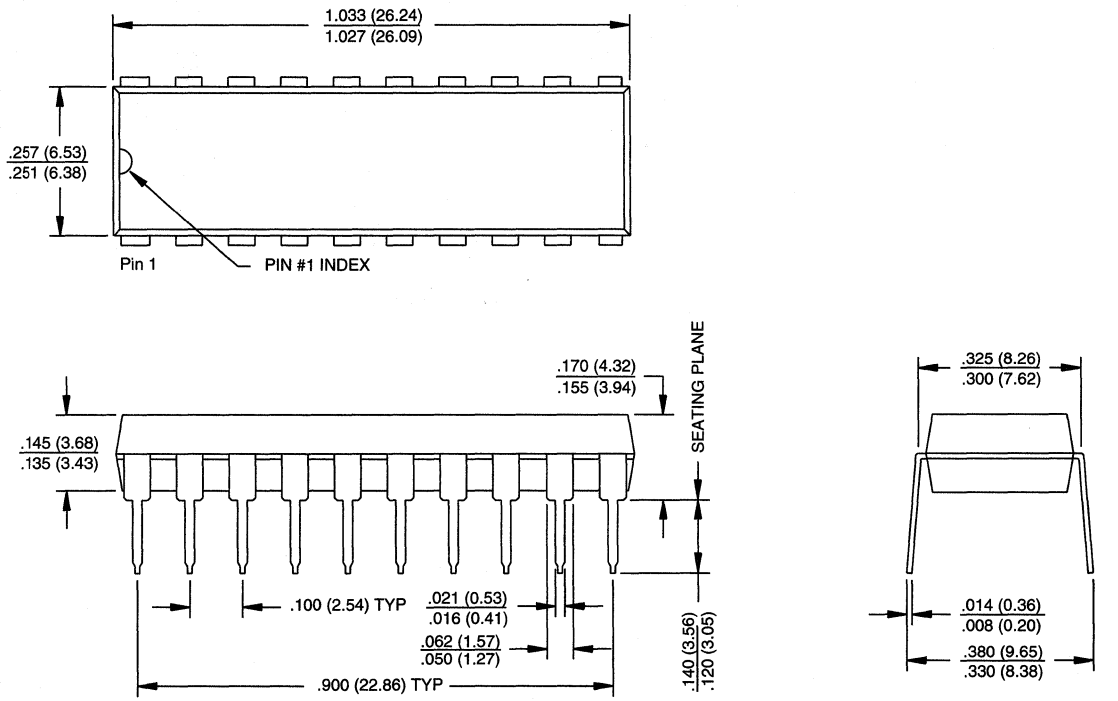
Finished Goods
Devices are shipped through a system that maintains lot identity.

*This flow is general and is based on the 1 Meg SRAM.

MICRON
SEMICONDUCTOR, INC.

20-PIN PLASTIC DIP

SA-1

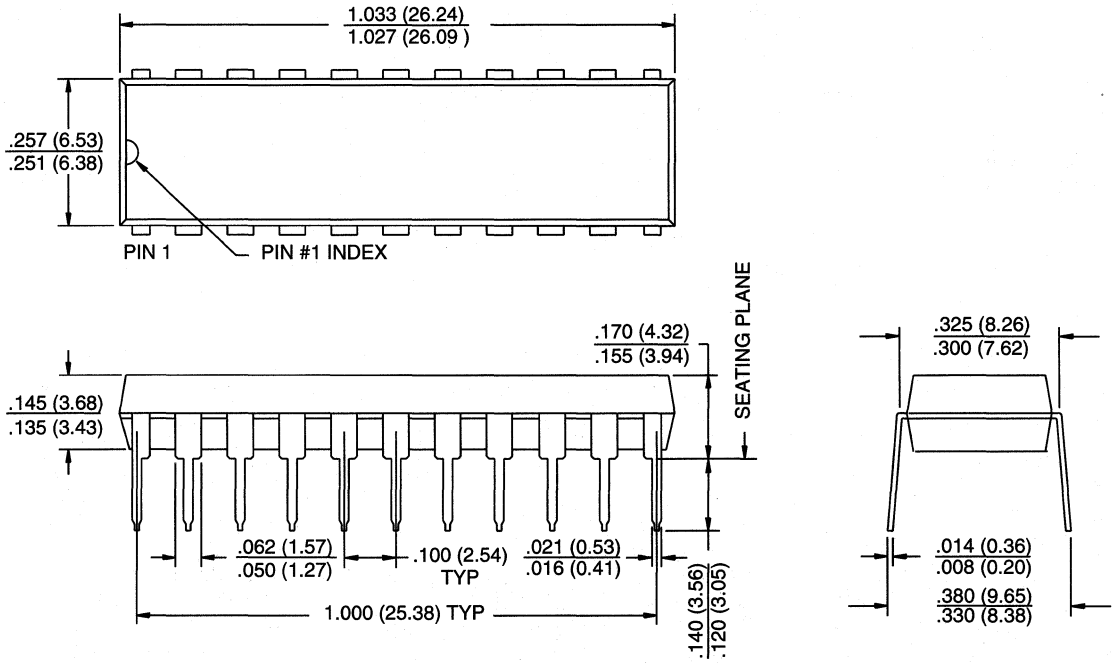


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

22-PIN PLASTIC DIP

SA-2

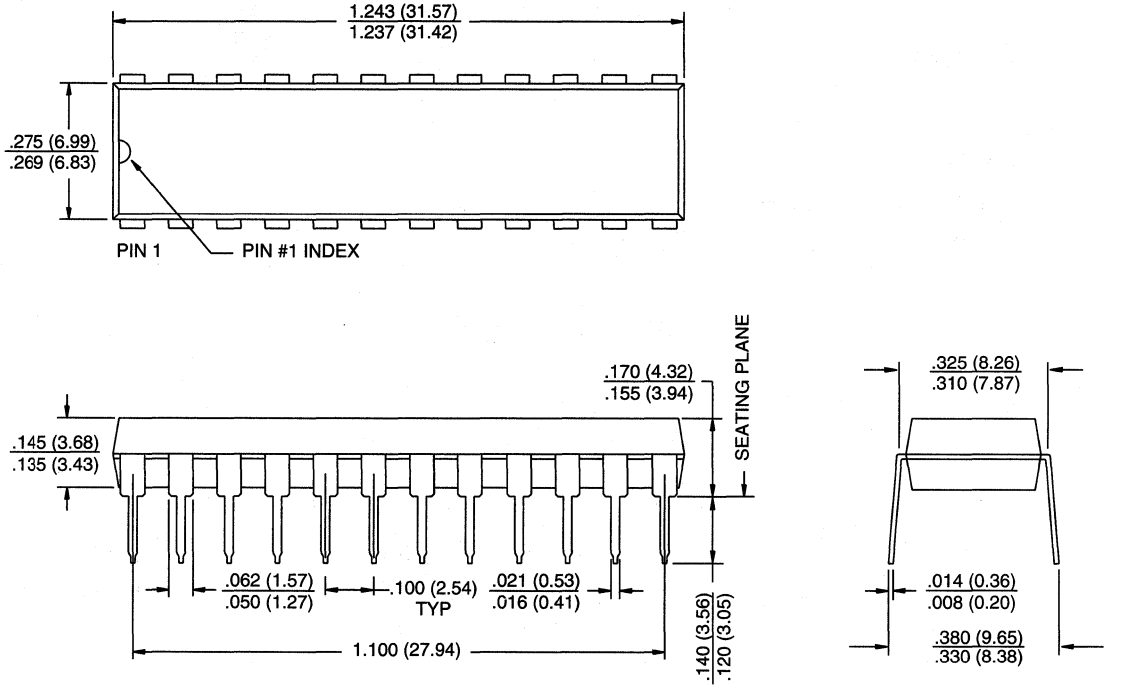


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

24-PIN PLASTIC DIP

SA-3

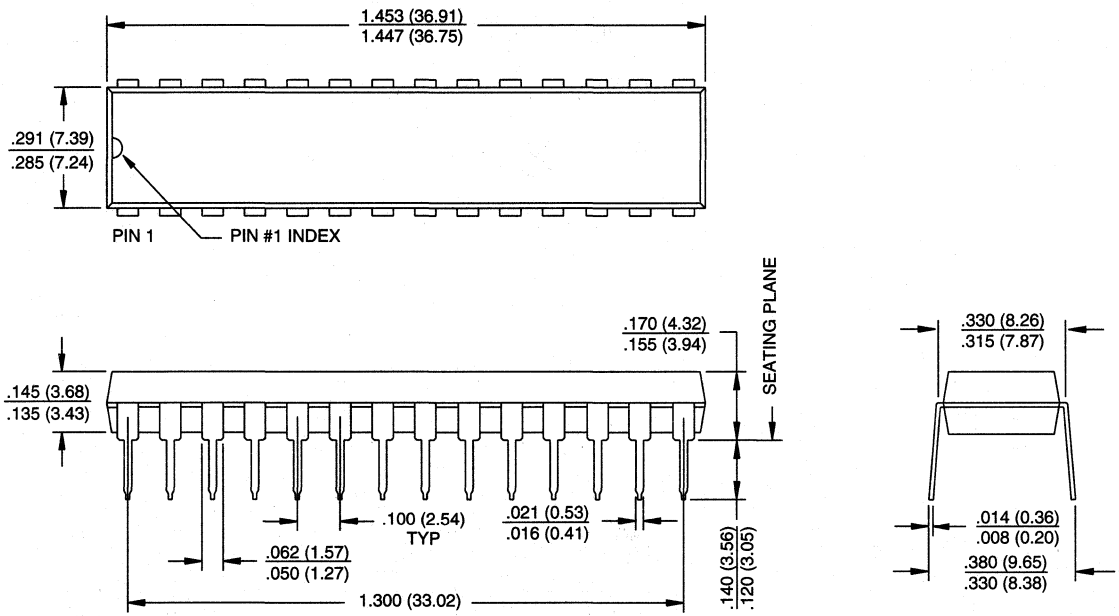


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC DIP

SA-4

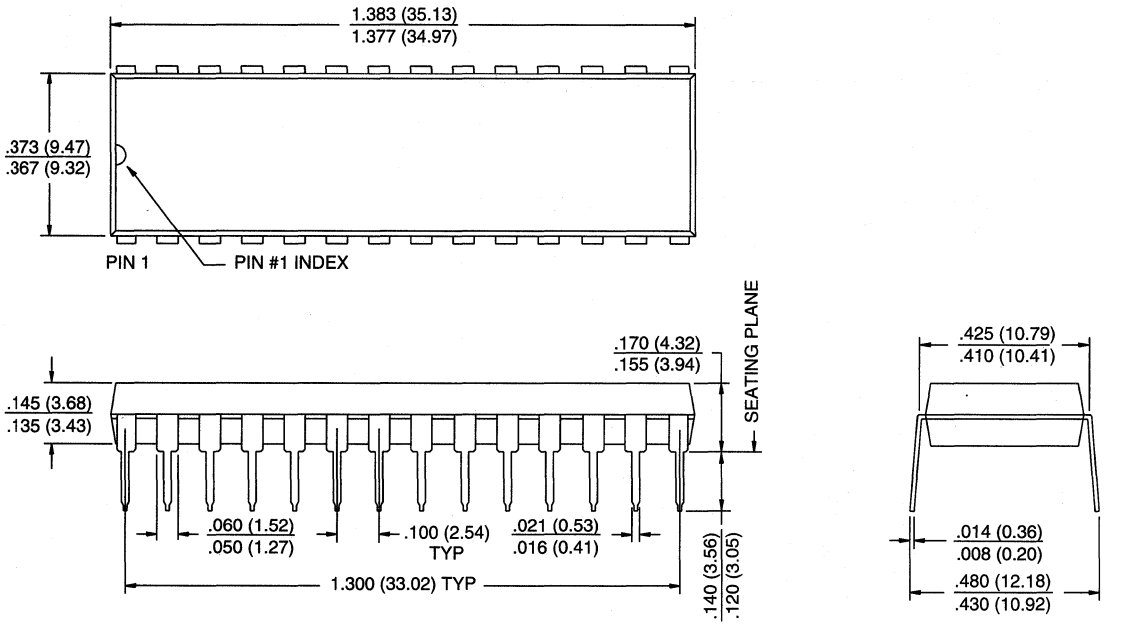


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC DIP

SA-5

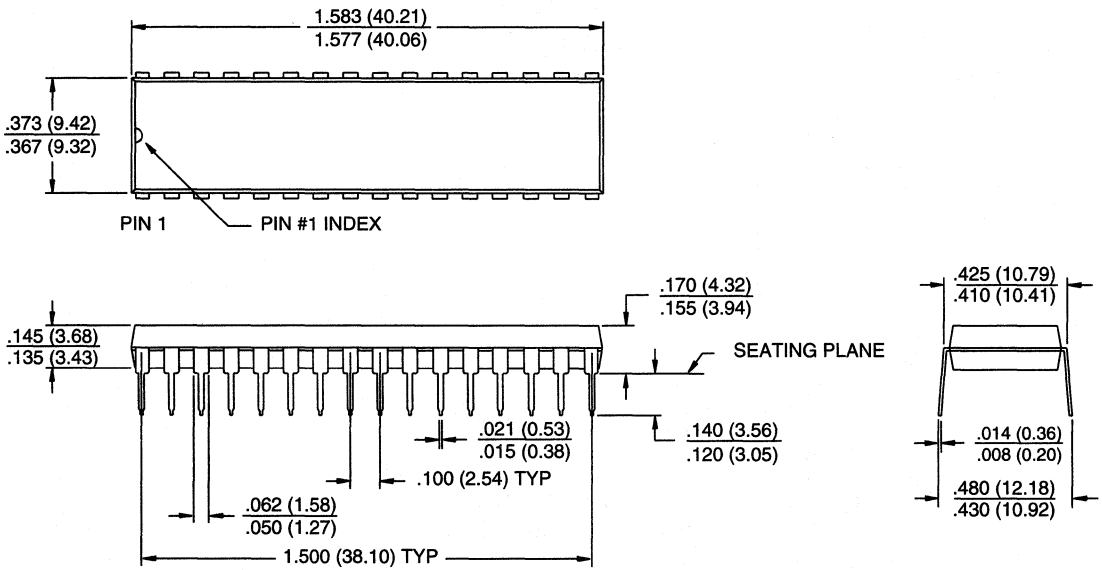


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC DIP

SA-6

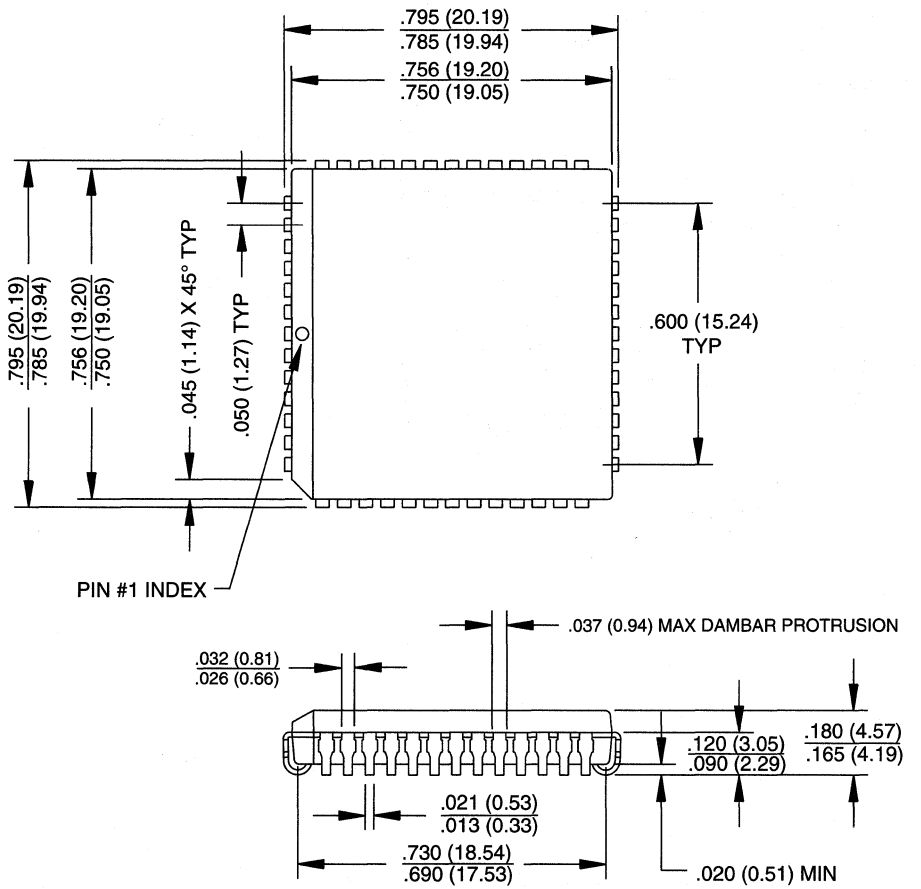


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

52-PIN PLCC

SB-1

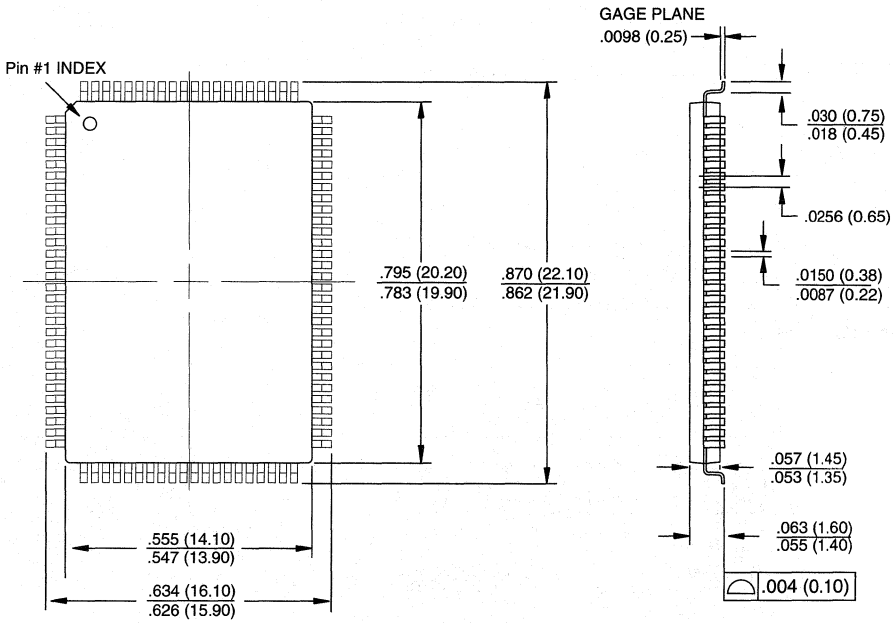


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

100-PIN TQFP

SC-1

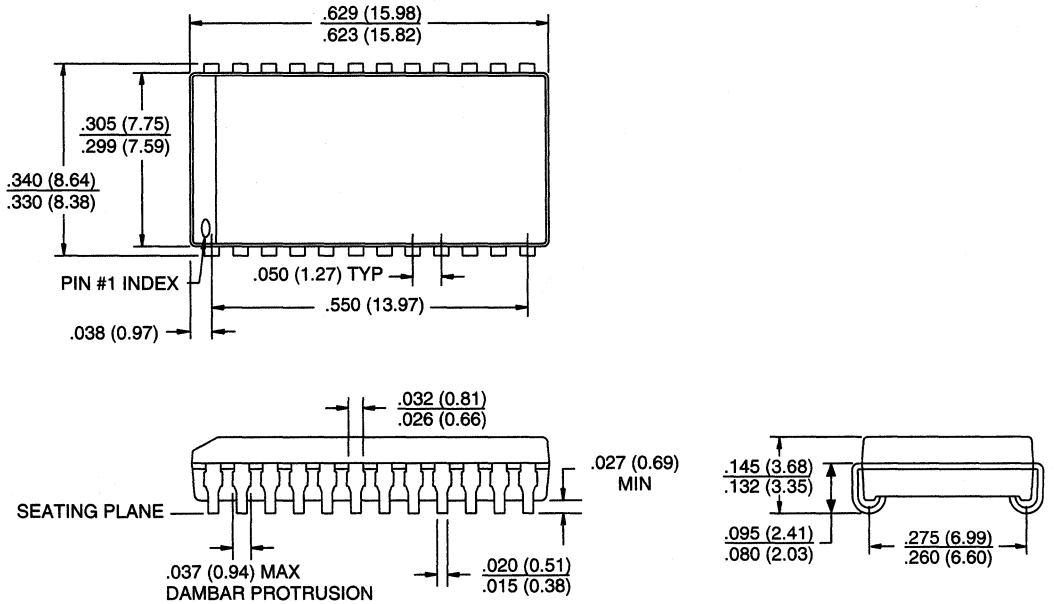


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

24-PIN PLASTIC SOJ

SD-1

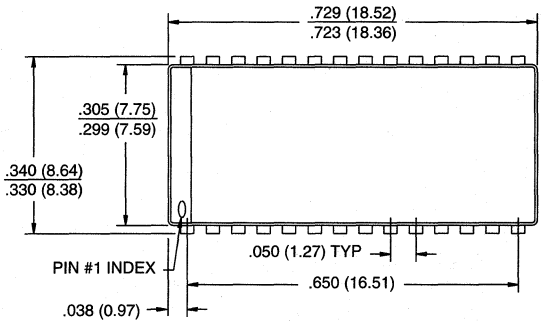


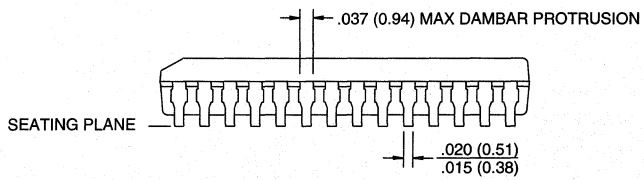
NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

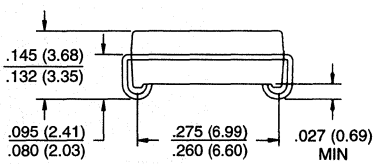
2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC SOJ

SD-2





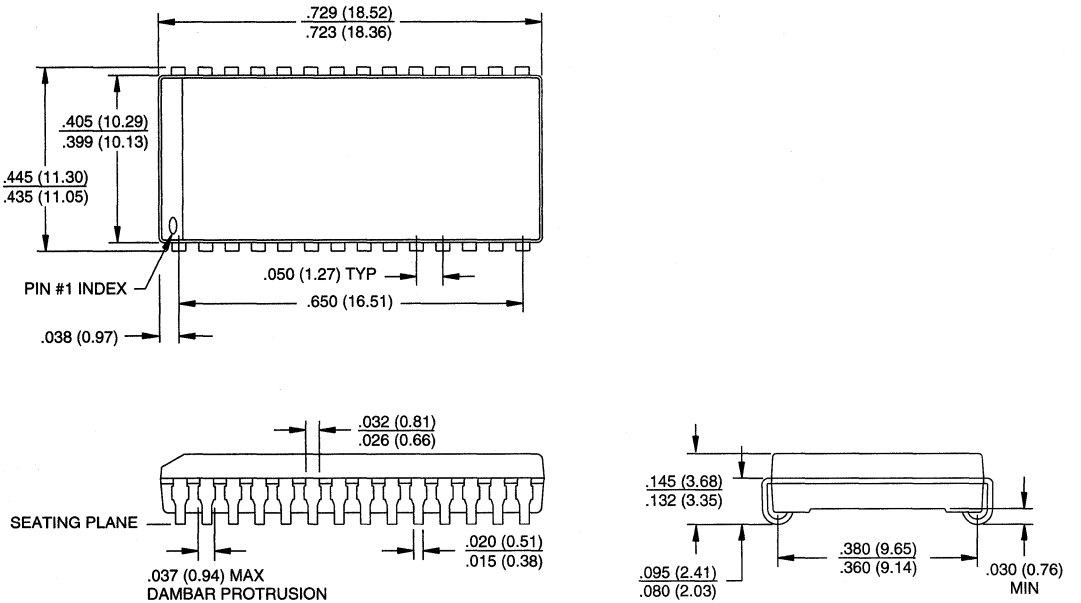


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC SOJ

SD-3



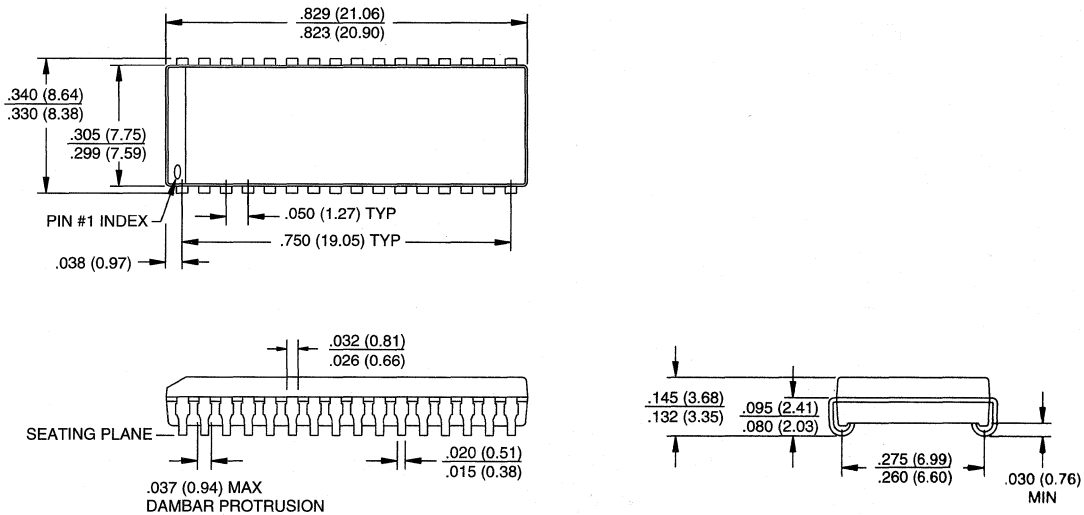
PACKAGE INFORMATION

NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC SOJ

SD-4

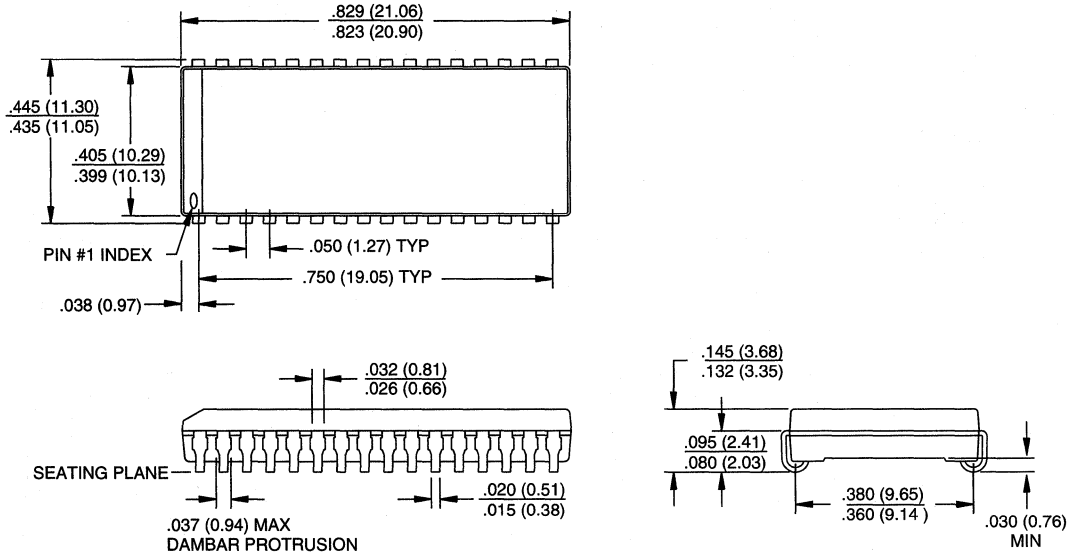


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC SOJ

SD-5

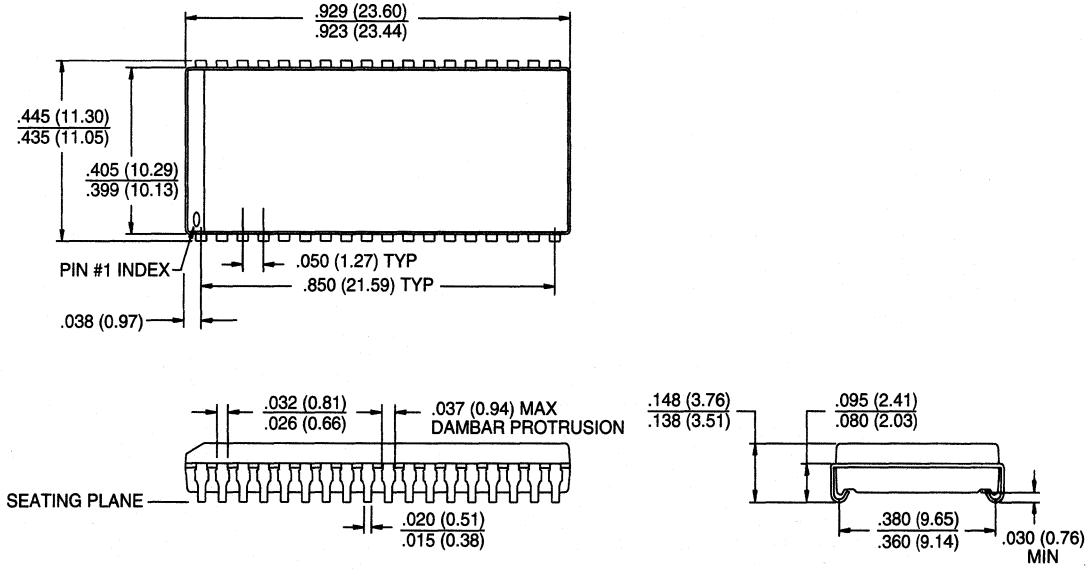


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

36-PIN PLASTIC SOJ

SD-6

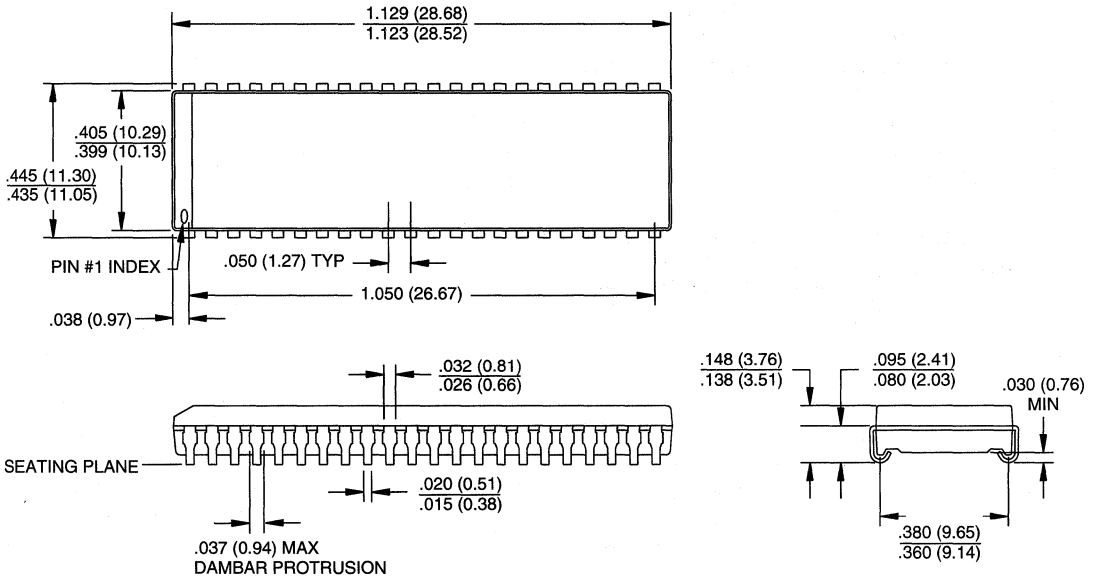


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

44-PIN PLASTIC SOJ

SD-7

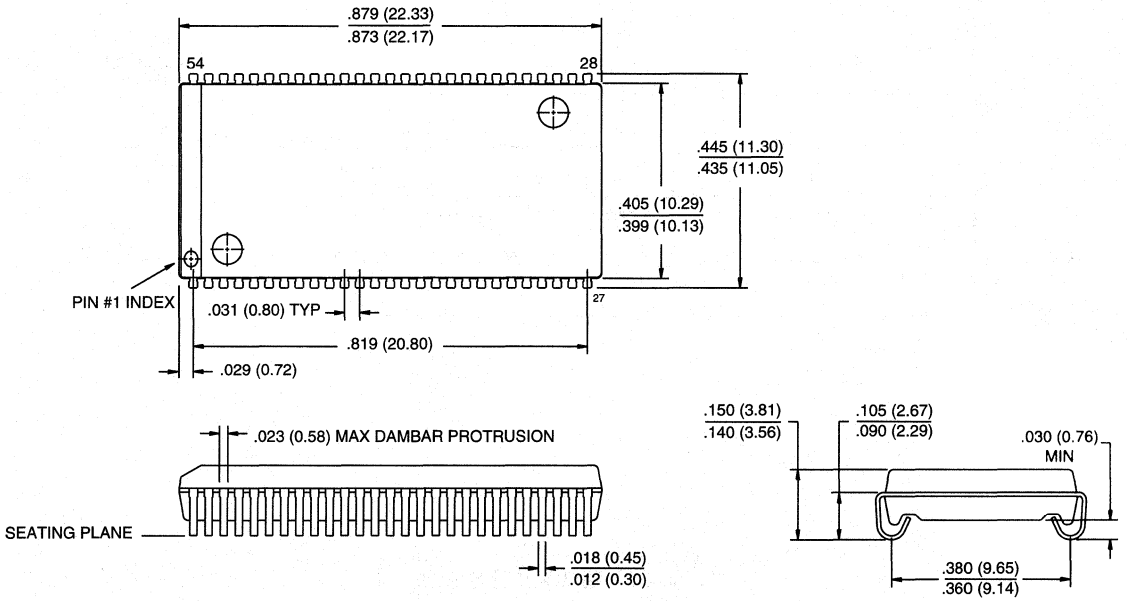


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

54-PIN PLASTIC SOJ

SD-8

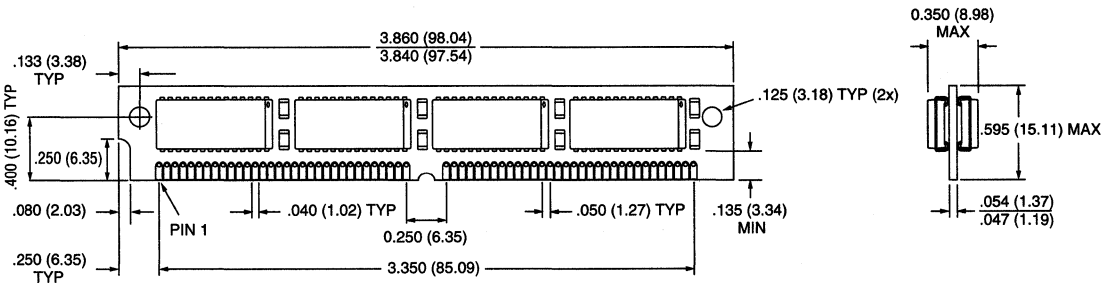


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

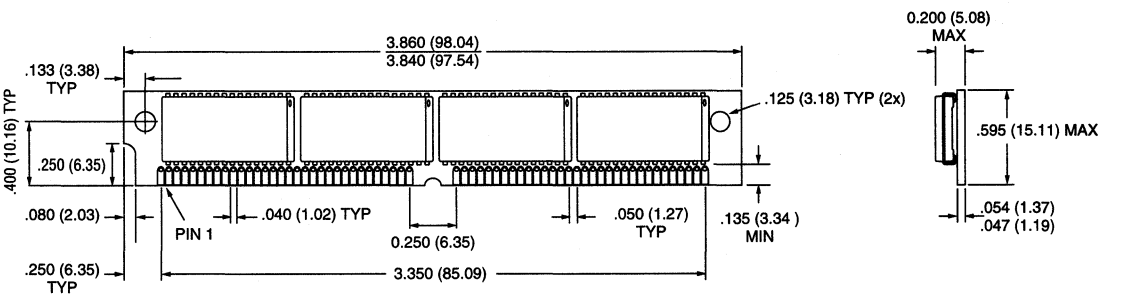
64-PIN MODULE SIMM

SE-1



64-PIN MODULE SIMM

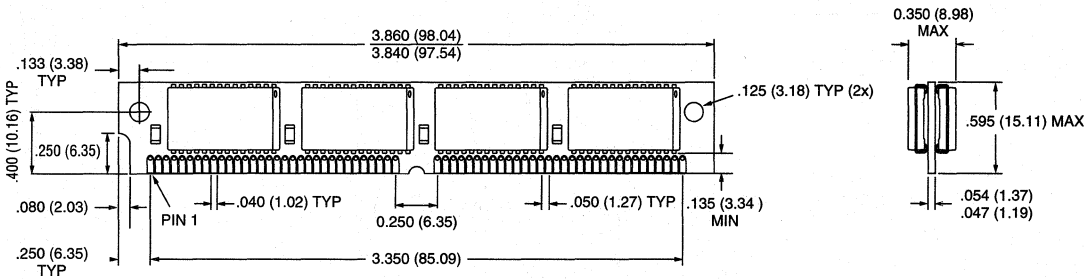
SE-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

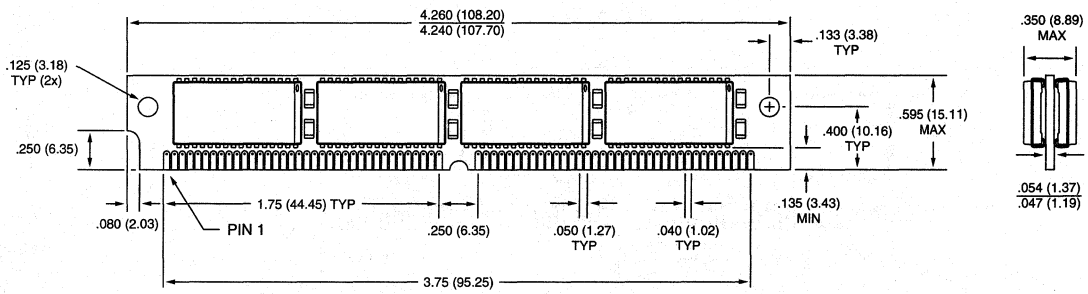
64-PIN MODULE SIMM

SE-3



72-PIN MODULE SIMM

SE-4

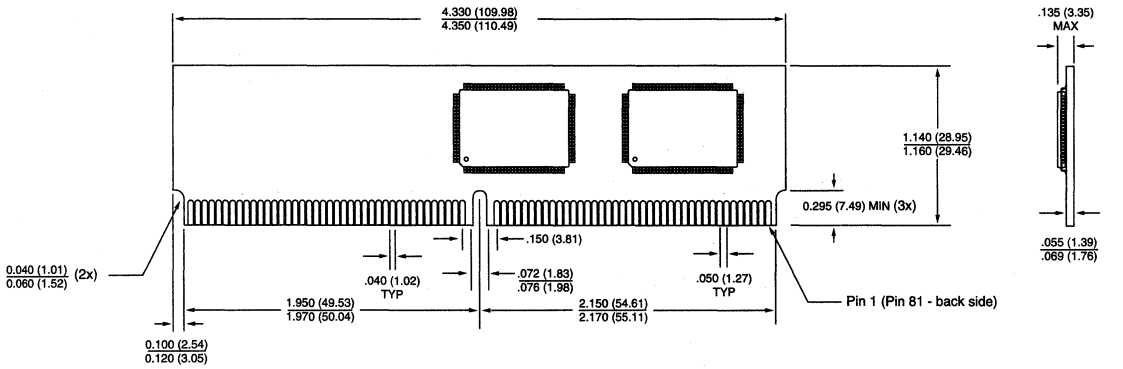


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

PACKAGE INFORMATION

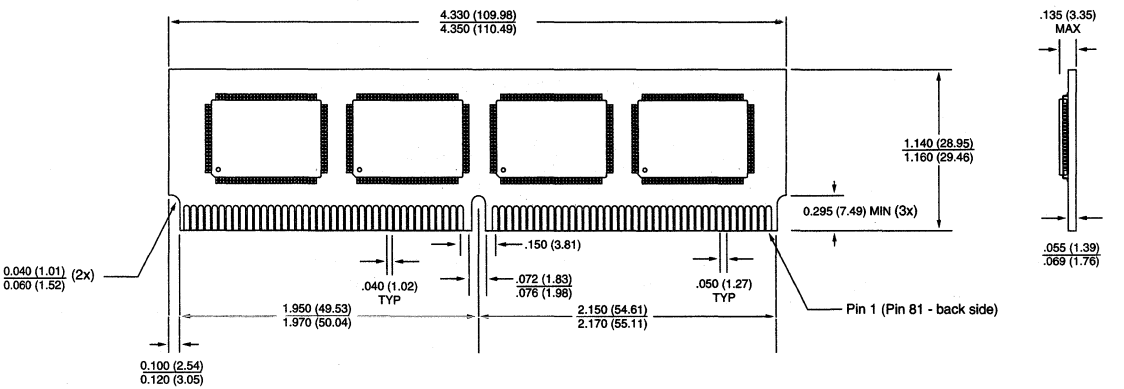
160-PIN MODULE DIMM

SF-1



160-PIN MODULE DIMM

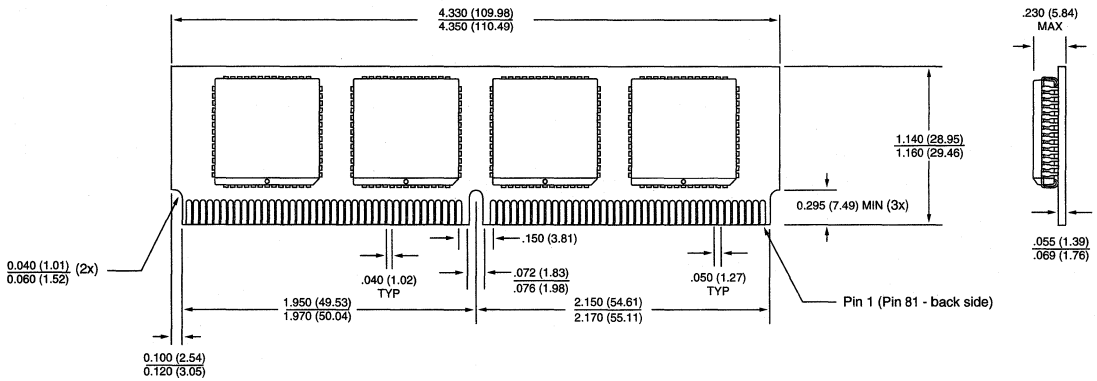
SF-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

160-PIN MODULE DIMM

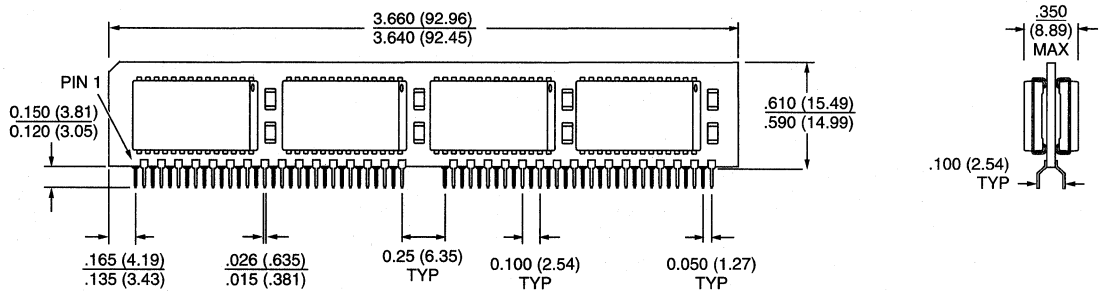
SF-3



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

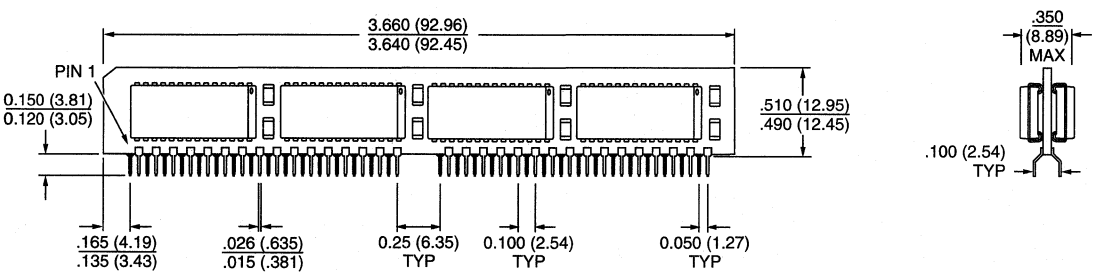
64-PIN MODULE ZIP

SG-1



64-PIN MODULE ZIP

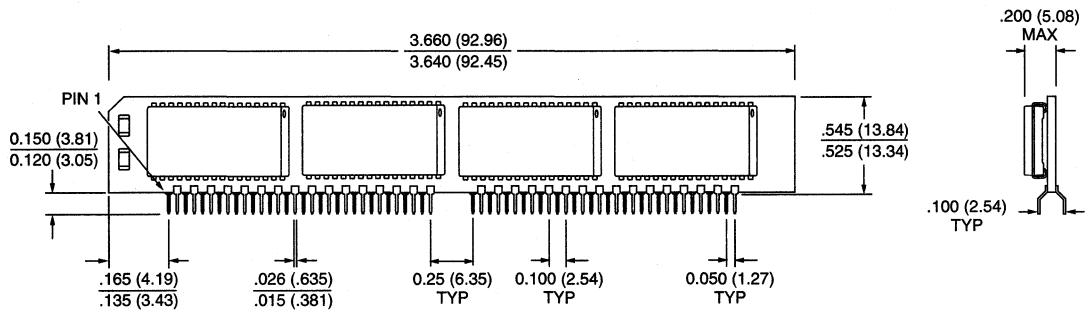
SG-2



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

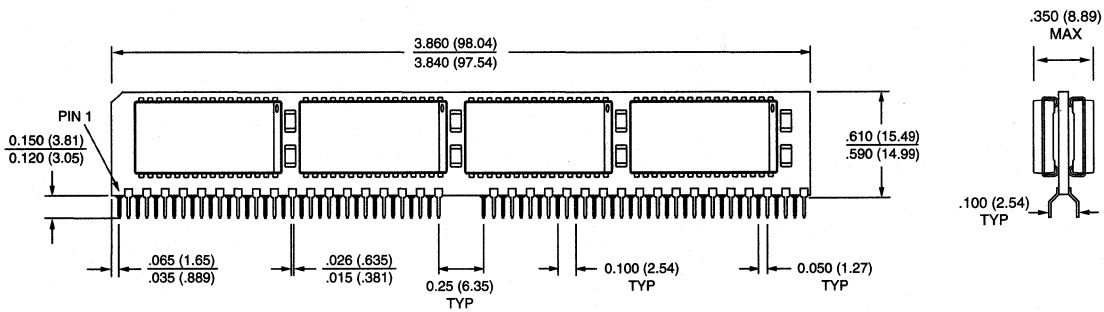
64-PIN MODULE ZIP

SG-3



72-PIN MODULE ZIP

SG-4



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

MICRON
SEMICONDUCTOR, INC.

CUSTOMER SERVICE NOTE

STANDARD SHIPPING BAR CODE LABELS

INTRODUCTION

Micron Semiconductor, Inc., has implemented standard bar code labels which accompany all shipments. These labels conform to EIA Standard 556.

The bar code labels allow customers to scan individual Micron containers for quick order verification. Figure 1 shows an example of the standard bar code label for master containers. Each individual box and/or container also has its own individual bar code label (see CSN-02).

BAR CODE INFORMATION

The information provided on the label is:

(4S) — Invoice/Packing Slip Number
(Q) — Quantity in master container
(Z) — Special: Reserved for individual customer requirements
(K) — Trans ID: Customer purchase order number
(P) — Customer Product ID: Customer part number. If a customer part number is not designated, the Micron part number will be printed.

ADDITIONAL SALES INFORMATION

Ship-to-Name: Customer's name and ship-to address
Ship-From-Name: Micron name and address
Master container package count
Package weight

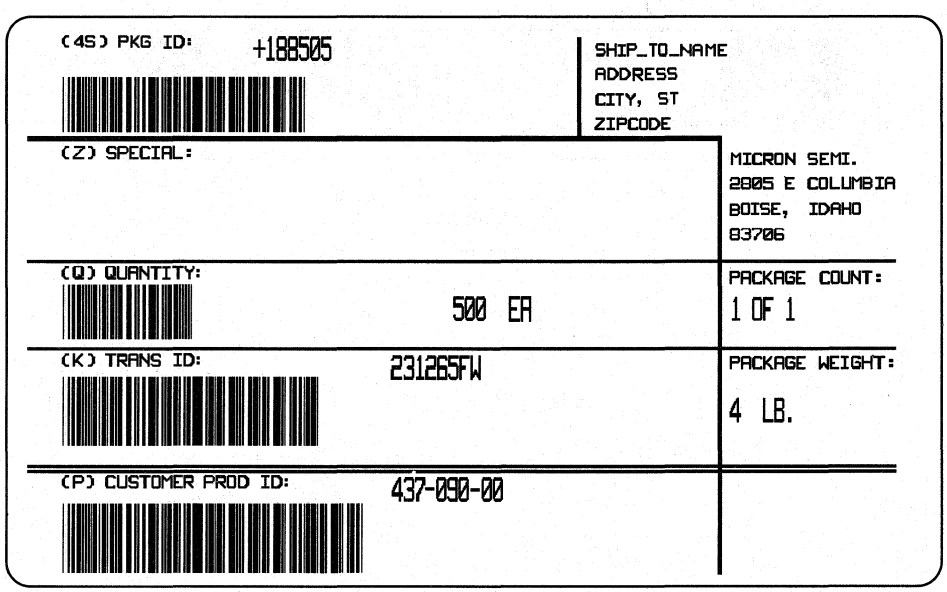


Figure 1
STANDARD BAR-CODE LABEL

CUSTOMER SERVICE NOTE

INDIVIDUAL BOX AND CONTAINER BAR CODE LABELS

INTRODUCTION

Micron Semiconductor, Inc., provides a standard bar code label on each individual box or container. The standard bar code label allows scanning of Micron shipping containers at a receiving dock for quick order verification.

Figure 1 shows an example of the standard bar code label used on individual boxes.

BAR CODE INFORMATION

The information provided on the label is:

Label 1: Individual box number (in a multibox shipment)
Actual box number printed
Micron part number/speed/customer code
Part type/rev/quantity/date code of oldest lot*

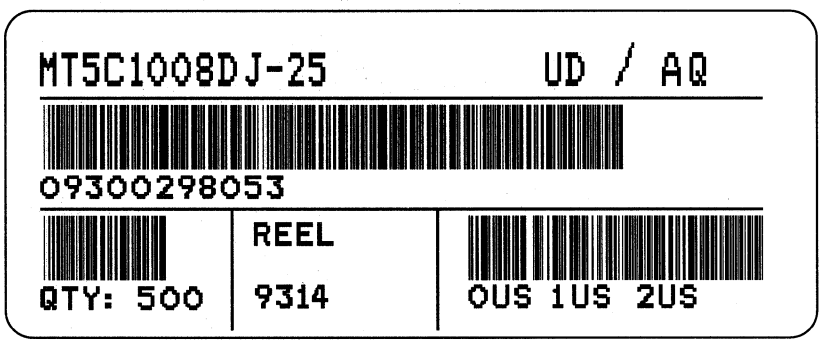


Figure 1
LABEL 1

*Indicates that more than one date code is contained on the reel.

CUSTOMER SERVICE NOTE

SURFACE-MOUNT PRODUCT LABELING

INTRODUCTION

Micron Semiconductor, Inc., provides a Humidity Indicator Card (HIC) with all surface-mount products.

Figure 1 shows an example of the standard HIC. Figure 2 shows approximate labeling of tape-and-reel packaged products.

HUMIDITY INDICATOR CARD (HIC)

The Humidity Indicator Card is hermetically sealed in drypack and provides an indication of the RH level of the contents.

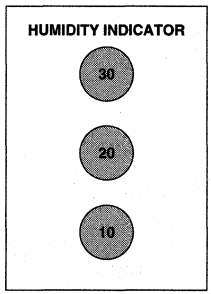


Figure 1
SURFACE-MOUNT PRODUCT HUMIDITY INDICATOR CARD

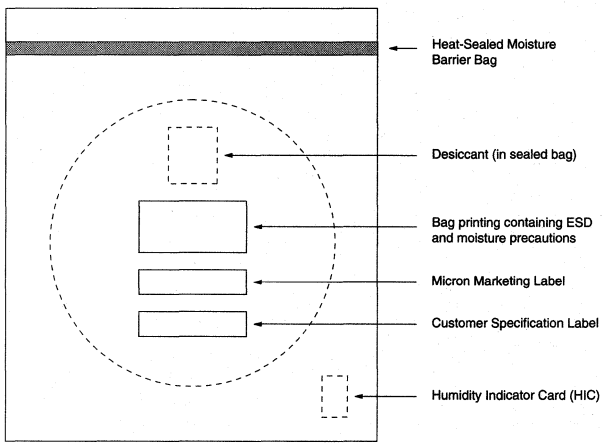


Figure 2
TAPE-AND-REEL PACKAGED PRODUCT LABEL

CUSTOMER SERVICE NOTE

BOX AND TAPE-AND-REEL QUANTITY AND WEIGHT CHART

INTRODUCTION

Micron encourages customers to place orders in increments of standard box, tray and reel quantities whenever possible. The chart below will help determine order quantities.

ADDITIONAL SALES INFORMATION

Benefits to Micron's customers by ordering in standard quantities:

1. Cost Savings—it is less expensive to send a shipment containing full boxes.
2. Process Control—Micron's production tracking system automatically checks speeds, revs, customer codes and quantities. When standard box quantities are ordered, manual errors are eliminated, thus ensuring error-free shipments.
3. Lot Integrity—lot integrity is kept in tact when box quantities are not broken up.
4. Fewer returns—fewer errors equal fewer complaints and returns.

SRAM STANDARD BOX AND TAPE-AND-REEL CHART

PART TYPE	QUANTITY PER TRAY	QUANTITY PER BOX	LBS PER BOX	QUANTITY PER TUBE	TAPE-AND-REEL QUANTITY	LBS PER REEL	TAPE SIZE
SRAM 256K							
MT5(L)C2561-2564	—	1500	9.9	15	—	—	—
MT5(L)C2565-2568	—	1000	9.9	10	—	—	—
MT5(L)C2561DJ-2568DJ	—	4000	12.5	25	1000	3.9	24mm x 12mm
SRAM 1 MEG							
MT5(L)C1001-1005	—	500	6.5	10	—	—	—
MT5(L)C1008	—	500	7.8	10	—	—	—
MT5(L)C1001DJ-1005DJ	—	2000	11.5	25	500	3.5	32mm x 16mm
MT5(L)C1008DJ	—	2000	11.5	20	500	3.5	44mm x 16mm
MT5(L)C128K8A1DJ	—	2000	11.5	20	500	3.5	44mm x 16mm
MT5(L)C256K4A1DJ	—	2000	11.5	20	500	3.5	44mm x 16mm
MT5(L)C64K16A1DJ	—	1500	19.9	15	500	3.5	—
SYNCHRONOUS SRAMs							
MT58LC64K18B2EJ	—	1500	15.7	25	500	5.6	32mm x 24mm
MT58LC64K18C4EJ	—	1500	15.7	25	500	5.6	32mm x 24mm
MT58LC64K18M1EJ	—	1500	15.7	25	500	5.6	32mm x 24mm
MT58LC64K18A6EJ	—	1500	15.7	25	500	5.6	32mm x 24mm
MT58LC64K18B2LG	72	1000	—	—	—	—	—
MT58LC64K18C4LG	72	1000	—	—	—	—	—
MT58LC32K32B2LG	72	1000	—	—	—	—	—
MT58LC32K32C4LG	72	1000	—	—	—	—	—
MT58LC32K36B2LG	72	1000	—	—	—	—	—
MT58LC32K36C4LG	72	1000	—	—	—	—	—

CUSTOMER SERVICE NOTE

ENVIRONMENTAL PROGRAMS

INTRODUCTION

Micron Semiconductor, Inc., takes a proactive approach to environmental protection and worker safety. We believe that this is not only environmentally responsible, but gives the company a long-term competitive advantage. Environmental protection programs include educating the workforce about chemical hazards, reduction in toxic chemical usage and air pollutants, recycling, and treating waste water.

CHEMICAL AWARENESS AND MONITORING

Micron educates and involves its workforce in eliminating hazardous and polluting chemicals and conditions. Micron currently has several programs in place which enable the company to minimize hazardous chemical use while maintaining flexibility in processes and operations. Examples of these programs include:

ENVIRONMENTAL TASK FORCE

This internal task force meets weekly to review the effects of process changes, new construction, and new equipment on the environment and on worker safety. The group also reviews regulations and compliance issues, and anticipates possible impacts of potential regulation changes from legislation.

CHEMICAL APPROVAL SYSTEM

This approval and monitoring system insures that Micron remains in compliance with OSHA and EPA reporting requirements and tracks chemicals in use. Acting as a guidance and training resource, the Chemical Approval Team gives direction and alternatives, rather than policing, chemical use. This cooperative method of identifying hazardous chemicals, waste treatment needs and costs, and safety procedures has proven very effective.

TOXIC CHEMICAL REDUCTION PROGRAM

This is an active program for continuous reduction of EPA toxic chemicals and other chemicals determined to be of some risk to employees or the environment. Through this program, in 1992 Micron eliminated the use of hazardous ethylene-based glycol ethers in manufacturing and replaced anhydrous ammonia in storage tanks with a process that uses aqueous calcium hydroxide. Micron also eliminated ozone-depleting chemicals from the manufacturing process in 1992.

REDUCTION OF AIR POLLUTANTS

Micron has an ongoing program to reduce toxic air pollutant emissions and is evaluating several different types of pollution abatement methods for air emissions. Micron has successfully reduced toxic air pollutant emissions and fugitive volatile organic compound (VOC) emmisions by 90 percent. Reductions were made in the use of acetone, toluene, methanol, and isopropyl alcohol. Use of methyl ethyl ketone was completely eliminated.

The company successfully replaced its solvent-based cleanroom cleaner with a water-based solution. Because cleaning procedures were changed and existing wipes were replaced with more absorbent ones, the water-based cleaner proved to be more effective than the solvent-based cleaner and has greatly reduced fugitive VOC emissions.

In converting from "puddle primers" to vapor primer ovens in our photo process, Micron has reduced HMDS usage by 90 percent. Micron has also installed high-efficiency purge pumps which exceed EPA specifications on refrigeration units in order to eliminate the discharge of refrigerants into the atmosphere. In addition, portable refrigerant reclaim units are used to recover and recycle refrigerants during maintenance or when equipment is retired.

WASTE WATER TREATMENT

Micron has completed the first phase of a three-phase industrial waste water treatment facility. The system was designed to remove fluoride from used process water and allow the water to be reclaimed. By 1997 Micron will reclaim all of its waste water and reduce ground water use by 80 percent. Micron recently won a Water Conservation Award from the Pacific Northwest Section of the American Water Works Association for this project.

RECYCLING AND ENERGY CONSERVATION

Several Micron teams have developed systems to recycle items for sale to outside customers or reuse within the manufacturing process. These items include sulfuric acid, gold, various solvents and alcohols, scrap metal, wire, aluminum and steel cans, buckets and barrels, pallets, plastic, and cardboard and paper products.

In 1987 Micron engineers developed an alternate cooling system, the Wet Side Economizer, which saves the company approximately $150,000 annually. The Wet Side Economizer uses cold air rather than refrigeration to cool the manufacturing complex. The system reduces kwh consumption by 15.1 million, which translates into a 11,174-ton reduction in CO_2 emissions, a 121-ton reduction in SO_2 emissions, and a 53-ton cut in NOx emissions. The system earned Micron a Certificate of Recognition for Energy Consciousness from the state of Idaho and an award for Energy Innovation from the U. S. Department of Energy in 1991.

Micron is continually working toward reducing emissions through recycling of solvents. We work with suppliers and internally to incorporate chemical recycling systems into processes. Micron is currently redistilling acetone and isopropyl alcohol on-site to repurify for reuse in the fab. We are also reviewing methods to recycle resist edge remover and organic strip.

COMMUNITY ASSISTANCE

Micron volunteers lab resources and provides consultation to local companies and community organizations, such as the Peregrine Fund, to help resolve industrial hygiene and environmental issues. Micron team members are active in local environmental and safety organizations and in the Community Emergency Planning Committee. Team members periodically host training classes (such as Hazardous Gas Bottle Handling and Disposal) for local professional organizations. Micron is also a member of the Idaho Association of Commerce and Industry (IACI) and is very active in the environmental committee.

CUSTOMER SERVICE NOTE

ELECTRONIC DATA INTERCHANGE

INTRODUCTION

Electronic Data Interchange (EDI) has become an important data transmission element in today's marketplace. Micron is ready to serve your EDI needs and encourages customer participation.

STANDARDS SUPPORTED

X.12

Micron supports versions 002000 through 003040 for all implemented transaction sets. The addition of new versions is an automated process which drives off of the standard diskettes available through Data Interchange Standards Association.

EDIFACT

Micron supports EDIFACT under the 90.1 EDIFICE guidelines for the Purchase Order (PO), PO Acknowledgment, PO Change and PO Change Acknowledgment messages.

TRANSACTION SETS

Inbound	Outbound
850 - PO	855 - PO Acknowledgment
860 - PO Change	865 - PO Change Acknowledgment
840 - Request For Quote (RFQ)	843 - Response to RFQ
830 - Forecast	856 - Advanced Ship Notice
846 - Inventory Inquiry/ Advice	810 - Invoice
867 - Product Transfer & Resale	
844 - Product Transfer Account Adjustment (PTAA)	849 - Response to PTAA
997 - Functional Acknowledgment	

VALUE ADDED NETWORKS

A T & T

A T & T allows our partners to transmit EDI documents via standard protocol or X.400 (e-mail protocol).

Advantis

Advantis is the result of a merger between the Sears and IBM networks.

TRANSMISSION TIMES

Transmission times are 2 a.m., 10 a.m., 1 p.m., 3 p.m. and 8 p.m. MST weekdays and 1 p.m. MST on weekends. Additional transmission times can be added easily as circumstances warrant.

MICRON EDI CONTACTS

EDI Project Leader	EDI Software Development
Becka Shirrod	Tony Holden
208-368-3338	208-368-3855

STEPS TO IMPLEMENTATION

The following are typical steps taken as Micron begins exchanging EDI data with a new trading partner:

- Micron receives an implementation guide from a trading partner
- Micron's EDI team contacts the trading partner's EDI coordinator to set up a trading partnership and coordinate the transmission and receipt of test documents
- Micron receives a test EDI document from the partner's VAN and responds with the necessary acknowledgments
- Once both parties agree everything is working properly, parallel testing with EDI and paper documents begins
- Micron insures an EDI agreement has been signed and returned to the trading partner
- Paper documents are replaced with EDI documents (full production).

CUSTOMER SERVICE NOTE

RETURN MATERIAL AUTHORIZATION (RMA) PROCEDURES

HOW TO RETURN PRODUCT TO MICRON

- Obtain an RMA number (see "How to Obtain an RMA" below).
- Package product taking all antistatic precautions.
- Write RMA number on outside of box for proper routing.
- Ship package prepaid to:
  Micron Semiconductor, Inc.
  Attn.: RMA Area
  2805 East Columbia Road
  Boise, ID 83706
- If RMA is being shipped from outside of the United States, please note that Boise, Idaho, is a customs port city; reference Port City Code 2907.

HOW TO OBTAIN AN RMA

NONFAILURE-RELATED RETURNS:

- If you buy direct, contact your Micron sales rep at 1-208-368-3900.
- If you buy through a Micron rep, contact that rep.
- If you buy through Distribution, contact the distributor.

Provide the Following Information:

- Micron part number, including speed and package
- Reason for return
- One of the following: PO number, invoice number, or sales order number
- One of the following: replacement parts, credit only, or refund

FAILURE-RELATED RETURNS AND/OR APPLICATION PROBLEMS:

- Contact Micron Application Engineering Department at 1-208-368-3900

Provide the Following Information:

- Micron part number, including speed and package
- Type of failure
- Name of engineer who witnessed failure or requested failure analysis report
- One of the following: PO number, invoice number, or sales order number
- One of the following: replacement parts, credit only, or refund

FAILURE ANALYSIS STANDARDS FOR RETURN MATERIAL AUTHORIZATIONS:

- Upon receipt of an RMA for failure analysis, Micron's Quality Assurance Department will provide an initial response within 48 hours.
- Micron's Quality Assurance Department will issue a completed failure analysis report within three weeks of receiving an RMA.

MICRON ACCOUNTING PROCEDURES FOR RETURN MATERIAL AUTHORIZATIONS

- Replacements: Replacement parts are shipped after receipt of the RMA parts. The credit memo will be applied directly to the replacement invoice. A new invoice will be sent when the replacement amount is greater than the returned amount. If this is not compatible with your accounts payable procedures, please advise your sales rep upon RMA request.
- Credit: A credit memo is sent out for the amount of the return upon arrival of the RMA parts. This credit memo number should be referenced when sending in payment information if intended to be used.
- Refund: A check request is submitted to Micron Accounts Payable upon receipt of RMA parts. A refund check is sent upon completion of the check request approval process.

CUSTOMER SERVICE NOTE

ISO 9001 CERTIFICATION

INTRODUCTION

Micron Semiconductor, Inc., was certified to ISO 9001 in the United States and Europe on February 1, 1994, by KEMA Registered Quality, Inc. The certification is also recognized by EQNET, the European Network for Quality System Assessment and Certification. Through this network, our KEMA certification is recognized by: AENOR Spain, AFAQ France, AIB-Vincotte Belgium, BSI QA United Kingdom, CISQ Italy, DS Denmark, ELOT Greece, IPQ Portugal, NCS Norway, NSAI Ireland, OQS Austria, SFS Finland, SIS Sweden and SQS Switzerland.

ISO 9001 CERTIFICATION DEFINED

ISO 9001 is one of a series of three international standards dealing with quality systems that can be used for external quality assurance purposes. It is a model for quality assurance in design/development, manufacturing, testing, installation and servicing. It is the most comprehensive level of certification in the internationally recognized ISO 9000 family for quality assurance management systems.

ISO 9000 gives customers and suppliers a single set of guidelines that are accepted worldwide and that can be followed to achieve a definable level of quality. The certification implies that a company's systems for accepting orders, reviewing customers' specifications, manufacturing and testing products, and delivering those products to its customers are quality controlled and should produce consistent results. A company seeking ISO certification must be certified as ISO 9001 if it has complete control over the design of its product with that control being a major factor in ensuring delivered quality.

A supplier's ability to conform to the ISO 9001 standard is assessed via the standard's Quality System Requirements—a set of twenty paragraphs each designed to address a specific portion of a quality system: management responsibility; quality system; contract review; design control; document control; purchasing; purchaser supplied product; product identification and traceability; process control; inspection and testing; inspection measuring and test equipment; inspection and test status; control of nonconforming product; corrective action; handling, storage, packaging and delivery; quality records; internal quality audits; training; servicing; and statistical techniques.

Micron's ISO 9001 certificate, number 93119, is valid until February 1, 1997, at which time Micron must again complete the audit cycle.

KEMA

cimei

MEMBER OF THE EUROPEAN NETWORK FOR QUALITY SYSTEM ASSESSMENT AND CERTIFICATION "EQNET"

CERTIFICATE

Number: 93119

The quality system of:

MICRON SEMICONDUCTOR, INC.
BOISE, IDAHO

including the implementation meets the requirements of the standard:

ISO 9001

Scope:
Micron's semiconductor business, including the design, manufacturing, electrical and environmental testing and the marketing of semiconductor memory components.

Reports that form the basis of this certificate:
93119-KRQ-1 up to and including 93119-KRQ-3.

This certificate is valid until: February 1, 1997

Issued for the first time: February 1, 1994

dr.ir. J.H. Blom
managing director

The method of operation for quality certification is defined in the KEMA Regulations for Quality System Certification. Integral publication of this certificate and adjoining reports is allowed.

N.V. KEMA
Utrechtseweg 310, Arnhem, Postbus 9035, 6800 ET ARNHEM
Telephone +31 85 56 34 98 Telefax +31 85 45 88 25

ACCEPTED BY THE
DUTCH COUNCIL FOR
CERTIFICATION

SALES INFORMATION

CUSTOMER SERVICE NOTE

MICRON DATAFAX

INTRODUCTION

Micron Semiconductor, Inc., gives customers and potential customers instant access to technical and sales information via Micron DataFax[SM], a user-friendly, fax-on-demand system.

Micron DataFax allows callers to make automated requests for data sheets, product literature and other product information during and after regular business hours. Micron DataFax improves customer support by offering product information 24-hours-a-day, and shortens the sales and design-in cycle by offering engineers the most up-to-date product information.

HOW IT WORKS

Micron DataFax makes ordering product information quick and easy using the touchtone keypad on your fax machine. Here's how it works:

1. From your fax machine, call 208-368-5800.
2. Press 1 to order. When requested, enter document number(s).*
3. The documents you ordered will be sent to the fax machine you called from.

*When you call, Micron DataFax will offer you a document index, which lists all documents currently in the system. Order the index to use as a reference for your subsequent document orders.

MICRON DataFax[SM]

CUSTOMER SERVICE NOTE

CUSTOMER COMMENT LINE

INTRODUCTION

Micron Semiconductor, Inc., is committed to achieving the highest standard in customer satisfaction, and we believe that giving our customers the opportunity to voice comments and complaints will help us discover ways to better serve them. To achieve continuous improvement, we need ongoing constructive customer feedback so we know exactly what our customers expect and need.

COMMENT LINE INFORMATION

Micron's Comment Line is answered by Customer Service personnel from 8:00 a.m. to 5:00 p.m. MST weekdays and is transferred to voice mail during off hours, weekends, and holidays. You may also fax your comments to us at any time. Whether you have experienced a recent transaction with Micron that requires immediate assistance, you want to provide feedback, or need information on local representatives in your area, please call or fax. Direct your inquiry to a customer satisfaction representative. We value your input!

STANDARDS

At Micron, we are dedicated to serving our customers and have set a 24-hour standard of returning all calls received on the Customer Comment Line. If we can't solve the matter at the time of your call, we will respond with an update to your question or concern within 24 hours.

Customer Comment Line:
U.S.A. 800-932-4992
Intl. 01-208-368-3410
Fax 01-208-368-3342

CUSTOMER SERVICE NOTE

PART MARKING

INTRODUCTION

Micron Semiconductor, Inc., utilizes a standard part marking on each product as shown in Figure 1 below. The only exceptions to this marking are for 32-lead and 52-lead EJ products on which the pin one designator is assigned a different location (see Figure 2).

PART MARKING INFORMATION

The part marking is right and left justified, and the character size is a minimum of .035/maximum of .045 inches high. Each part marking contains the following information: date code, revision letter (if relevant), country of origin (assembly), Micron logo, product family, process technology, device number, package type, pin one designator, speed and special test option (if relevant).

LASER SCRIBE IDENTIFICATION

Each part is also laser-scribed with a unique identification number. This identification number was previously located on the bottom side of the part only. We are currently adding the laser inscription to the top side as well.* The top-side inscription will allow for complete traceability of a component even after soldered onto a printed circuit board.

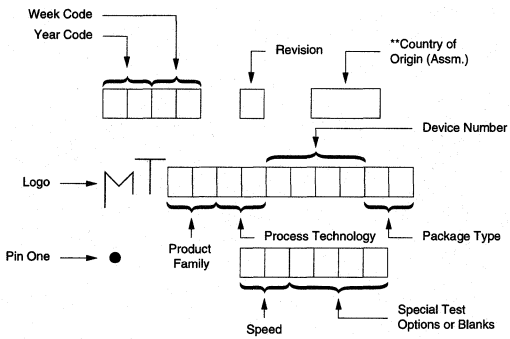


Figure 1
STANDARD PART MARKING

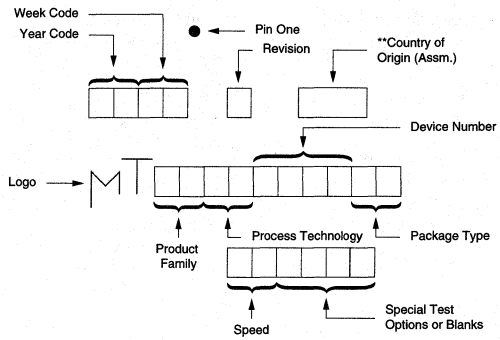


Figure 2
32-LEAD AND 52-LEAD EJ PRODUCTS PART MARKING

* Exceptions: A top-side laser inscription will not be added to the ZIP package. Off-shore assembled products will not be laser-scribed on the top side.

** May be blank if country of origin is printed on bottom of device.

CUSTOMER SERVICE NOTE

PRODUCT CHANGE NOTIFICATION (PCN) SYSTEM

MICRON'S PCN SYSTEM

Micron's automated Product Change Notification (PCN) System provides notification to customers, per mutually agreed upon requirements, of Micron product or production changes affecting form, fit or function.

CHANGES REQUIRING NOTIFICATION

Product and production changes requiring customer notification include:

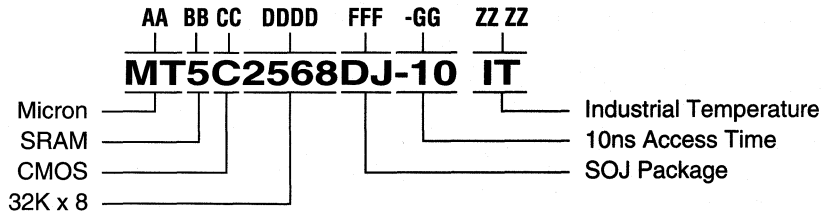
- bonding wire
- data sheet
- die coat
- die redesign
- die shrink
- geographic location
- internal connections
- lead frame
- mark change
- mark ink
- metalization
- mold compound
- package dimensions
- packaging
- passivation
- plating material
- plating process
- product obsolescence
- shipping tube
- wafer material

PCN LETTER DOCUMENTATION

PCN letters include the following information:

- PCN number
- a detailed description of the change
- a statement of the reason for the change
- supporting qualification data if appropriate
- a description of Micron product(s) affected by the change
- a list of each Micron part number (along with the corresponding customer number if available) purchased during the past 12 months or for which there is current backlog.

EXPANDED COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product ..... MT

BB – PRODUCT FAMILY

Flash 28
DRAM 4
SGRAM 41
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC
Flash CMOS ..... F
Low Voltage Flash CMOS ..... LF

DDDD – DEVICE NUMBER

(Can be modified to indicate variations)

Flash ..... Density, Configuration
DRAM ..... Width, Density
TPDRAM ..... Width, Density
SRAM ..... Total Bits, Width
Synchronous SRAM ..... Density, Width

E – DEVICE VERSIONS

(Alphabetic characters only; located between D and F when required.)

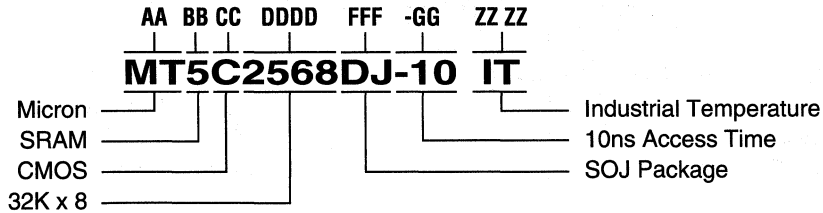
JEDEC Test Mode (4 Meg DRAM) ..... J
Errata on Base Part ..... Q

FFF – PACKAGE CODES

PLASTIC

DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG
QFP ..... LG
TSOP (Type I) ..... VG
TSOP (Type I, Reversed) ..... XG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

EXPANDED COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

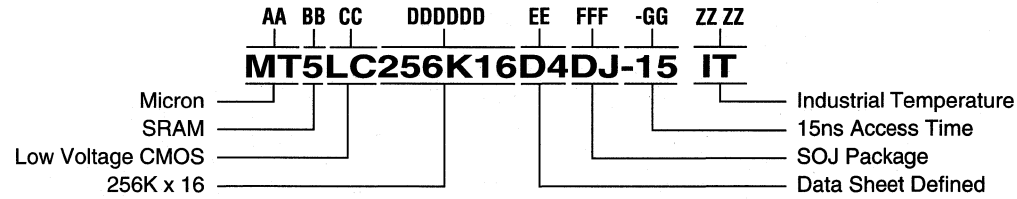
Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh/Extended Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Power, Low Volt Data Retention	LP
Flash	
Bottom Boot	B
Top Boot	T
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

NEW COMPONENT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER

Micron Product ..... MT

BB – PRODUCT FAMILY

DRAM 4
SGRAM 41
TPDRAM 43
Synchronous DRAM 48
SRAM 5
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY

CMOS C
Low Voltage CMOS LC
BiCMOS ..... B
Low Voltage BiCMOS ..... LB

DDDDDD – DEVICE NUMBER

Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter ..... Bits
K ..... Kilobits
M ..... Megabits
G ..... Gigabits

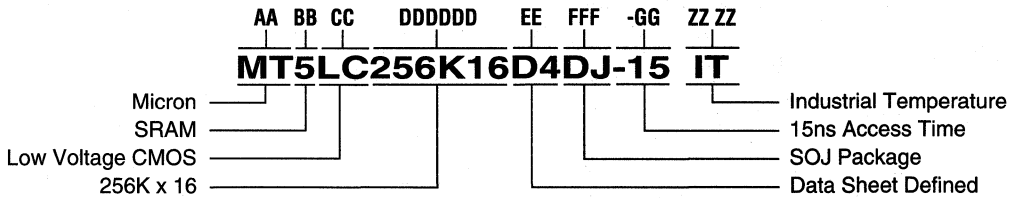
EE – DEVICE VERSIONS

(The first character is an alphabetic character only; the second character is a numeric character only.)
Specified by individual data sheet.

FFF – PACKAGE CODES

Plastic
DIP ..... Blank
DIP (Wide Body) ..... W
ZIP ..... Z
LCC ..... EJ
SOP/SOIC ..... SG
QFP ..... LG
TSOP (Type II) ..... TG
TSOP (Reversed) ..... RG
TSOP (Longer) ..... TL
SOJ ..... DJ
SOJ (Wide) ..... DW
SOJ (Reversed) ..... DR
SOJ (Longer) ..... DL

NEW COMPONENT NUMBERING SYSTEM (continued)



GG – ACCESS TIME

-5	5ns or 50ns
-6	6ns or 60ns
-7	7ns or 70ns
-8	8ns or 80ns
-9	9ns or 90ns
-10	10ns or 100ns
-12	12ns or 120ns
-15	15ns or 150ns
-17	17ns
-20	20ns
-25	25ns
-35	35ns
-45	45ns
-53	53ns
-55	55ns

ZZ ZZ – PROCESSING CODES

(Multiple processing codes are separated by a space and are listed in hierarchical order.)

Example:
A DRAM supporting low power, extended refresh (L); low voltage (V) and the industrial temperature range (IT) would be indicated as V L IT.

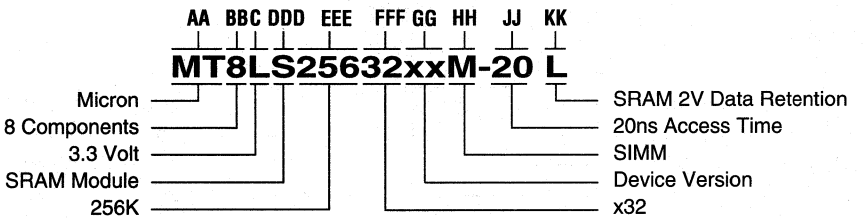
Interim	I
Low Voltage	V

ZZ ZZ – PROCESSING CODES (continued)

DRAMs	
Low Power (Extended Refresh)	L
Low Power (Self Refresh/Extended Refresh)	S
SRAMs	
Low Volt Data Retention	L
Low Power	P
Low Volt Data Retention, Low Power	LP
EPI Wafer	E
Commercial Testing	
0°C to +70°C	Blank
-40°C to +85°C	IT
-40°C to +125°C	AT
-55°C to +125°C	XT
Special Processing	
Engineering Sample	ES
Mechanical Sample	MS
Sample Kit*	SK
Tape-and-Reel*	TR
Bar Code*	BC

* Used in device order codes; this code is not marked on device.

MODULE NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
- Micron Semiconductor Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

C – PROCESS TECHNOLOGY
- LOW VOLTAGE (3.3V) L

DDD – RAM FAMILY
- DRAM ..... D
- DRAM TSOP ..... DT
- SRAM ..... S
- SRAM TSOP ..... ST
- SYNCHRONOUS SRAM ..... SY
- SYNCHRONOUS SRAM TQFP ..... SYT

EEE – DEPTH

FFF – WIDTH

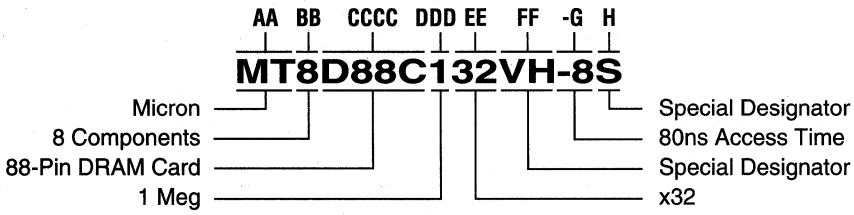
GG – DEVICE VERSIONS
- Specified by individual data sheet (Synchronous SRAM only)

HH – PACKAGE CODE
- Gold Plated SIMM/DIMM ..... G
- ZIP ..... Z
- SIP ..... N
- SIMM/DIMM ..... M
- Small Outline DIMM ..... H
- Small Outline Gold DIMM ..... HG
- Double-Sided SIMM (1 or 4 Meg x 36 Only) ..... DM
- Double-Sided SIMM (Gold 1 or 4 Meg x 36 Only) ..... DG

JJ – ACCESS TIME
- -10 ..... 10ns
- -12 ..... 12ns
- -15 ..... 15ns
- -17 ..... 17ns
- -20 ..... 20ns
- -25 ..... 25ns
- -35 ..... 35ns
- -6 ..... 60ns
- -7 ..... 70ns
- -8 ..... 80ns

KK – MODULE SPECIAL DESIGNATOR
- SRAM
  - 2V data retention L
  - Low Power ..... P
  - Low Power, 2V data retention ..... LP
- DRAM
  - Low Power (Extended Refresh) L
  - ECC C
  - Extended Data Out X
  - Self Refresh ..... S
  - 16 Meg DRAM 4,096 Refresh ..... B

DRAM CARD NUMBERING SYSTEM



AA – Product Line Identifier
Micron Product ..... MT

BB – NUMBER OF MEMORY COMPONENTS

CCCC – DRAM CARD DESIGNATOR AND PIN COUNT
88-Pin DRAM Card D88C

DDD – DEPTH

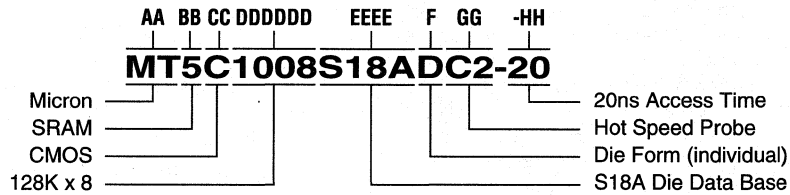
EE – WIDTH

FF – SPECIAL DESIGNATOR
3.3 Volts V
Reduced length (2") ..... H

G – ACCESS TIME
-5 ..... 50ns
-6 ..... 60ns
-7 ..... 70ns
-8 ..... 80ns

H– SPECIAL DESIGNATOR
Self Refresh ..... S

DIE PRODUCT NUMBERING SYSTEM



AA – PRODUCT LINE IDENTIFIER
Component Product ..... MT

BB – PRODUCT FAMILY
SRAM 5
DRAM 4
Synchronous SRAM 58

CC – PROCESS TECHNOLOGY
CMOS C
Low Voltage CMOS LC

DDDDDD – DEVICE NUMBER
When *no* alpha character appears as part of this section, the section is defined as:
DRAM ..... Width, Density
SRAM ..... Total Bits, Width
Synchronous SRAM ..... Depth, Width

When an alpha character occurs as part of this section, the section is defined as:
Depth, Width

Example:
1M16 = 1 megabit deep by 16 bits wide = 16 megabits of total memory.

No Letter ..... Bits
K ..... Kilobits
M ..... Megabits
G ..... Gigabits

EEEE – DIE DATA BASE REVISION

F – FORM
Die Form ..... D
Wafer Form (6" Wafer) ..... W

GG – TESTING LEVELS
Standard Probe (0° to 70°C) C1
Hot Speed Probe (0° to 70°C) C2
Known Good Die (0° to 70°C) C3

HH – ACCESS TIME
(Applicable for C2 and C3 only)
-5 ..... 5ns or 50ns
-6 ..... 6ns or 60ns
-7 ..... 7ns or 70ns
-8 ..... 8ns or 80ns
-9 ..... 9ns or 90ns
-10 ..... 10ns or 100ns
-12 ..... 12ns or 120ns
-15 ..... 15ns or 150ns
-17 ..... 17ns
-20 ..... 20ns
-25 ..... 25ns
-35 ..... 35ns
-45 ..... 45ns
-50 (SRAM only) 50ns
-SS (C2 only) ..... speed sorted

ORDER INFORMATION*

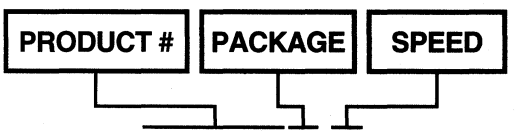
Each Micron component family is manufactured and quality controlled in the U.S.A. at our modern Boise, Idaho, facility employing Micron's low-power, high-performance CMOS silicon-gate process. Micron products are functionally equivalent to other manufacturers' products that meet JEDEC standards. Device functionality is consistently assured over a wider power supply, temperature range and refresh range than specified. Each unit receives continuous system-level testing during many hours of accelerated burn-in prior to final test and shipment. This testing is performed with Micron's exclusive AMBYX intelligent burn-in and test system.

Please contact the factory for technical, test and application assistance. Micron can also furnish the sales representative and distributor nearest you. Micron's policy is to offer prompt, accurate and courteous service while assuring reliability and quality.

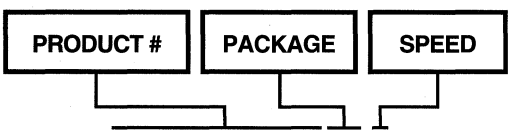
Telephone: 208-368-3900
Fax: 208-368-4431
Micron DataFax: 208-368-5800
Customer Comment Line:
800-932-4992 (U.S.A.)
01-208-368-3410 (Intl.)
Customer Comment Fax Line:
208-368-3342

ORDER EXAMPLES

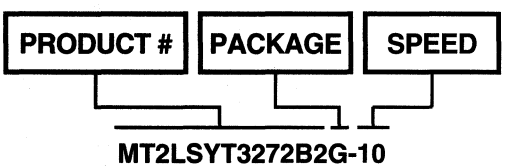
SRAM
128K x 8, 3.3V, 15ns in Plastic SOJ



SYNCHRONOUS SRAM
32K x 32, 9ns in Plastic TQFP



SRAM MODULE
32K x 72, 10ns in Gold Plated SIMM



SALES INFORMATION

*For more detailed information, refer to the product numbering charts on pages 8-15 through 8-21.

ALABAMA

Representative

Southeast Technical Group
101 Washington, Suite 6
Huntsville, AL 35801
Phone - 205-534-2376
Fax - 205-534-2384

Distributors

Anthem Electronics Incorporated
4920 H, Corporate Drive
Huntsville, AL 35805
Phone - 205-890-0302
Phone - 800-359-3531
Fax - 205-890-0130

Hamilton Hallmark
4890 University Square, Suite 1
Huntsville, AL 35816
Phone - 205-837-8700
Phone - 800-572-7236
Fax - 205-830-2565

Wyle Laboratories
Tower Building, 2nd Floor
7800 Governers Drive West
Huntsville, AL 35807
Phone - 205-830-1119
Fax - 205-830-1520

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ARIZONA

Representative

Quatra Associates
4645 South Lakeshore Drive, Suite 1
Tempe, AZ 85282
Phone - 602-820-7050
Fax - 602-820-7054

Distributors

Anthem Electronics Incorporated
1555 10th Place, Suite 101
Tempe, AZ 85281
Phone - 602-966-6600
Fax - 602-966-4826

Hamilton Hallmark
4637 South 36th Place
Phoenix, AZ 85040
Phone - 602-437-1200
Phone - 800-352-8489
Fax - 602-437-2348

Wyle Laboratories
4141 E. Raymond Street, Suite 1
Phoenix, AZ 85040
Phone - 602-437-2088
Fax - 602-437-2124

Die Distributor

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7725 N. Orange Blossom Trail
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Fax - 407-290-0164

ARKANSAS

Representative

Nova Marketing Incorporated
8350 Meadow Road, Suite 174
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Phone - 214-265-4600
Fax - 214-265-4668

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651 N. Plano Road, Suite 401
Richardson, TX 75081
Phone - 214-238-7100
Fax - 214-238-0237

Hamilton Hallmark
7079 University Blvd.
Winter Park, FL 32792
Phone - 407-657-3300
Fax - 407-678-4414

Wyle Laboratories
1810 N. Greenville Avenue
Richardson, TX 75081
Phone - 214- 235-9953
Fax - 214-644-5064

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

CALIFORNIA

Representatives (Northern California)

Bay Area Electronic Sales, Inc.
2001 Gateway Place, Suite 315 W
San Jose, CA 95110
Phone - 408-452-8133
Fax - 408-452-8139

Bay Area Electronic Sales, Inc.
9119 Eden Oak Circle
Loomis, CA 95650
Phone - 916-652-6777
Fax - 916-652-5678

Representatives (Southern California)

Micron Sales Southwest, Inc.
5060 Shoreham Place, Suite 200
San Diego, CA 92122
Phone - 619-458-5859
Fax - 619-453-0034

Micron Sales Southwest, Inc.
5100 Campus Drive, Suite 200
Newport Beach, CA 92660
Phone - 714-724-8085
Fax - 714-724-0560

Distributors

Anthem Electronics Incorporated
1160 Ridder Park Drive
San Jose, CA 95131
Phone - 408-453-1200
Fax - 408-441-4500

Anthem Electronics Incorporated
9131 Oakdale Avenue
Chatsworth, CA 91311
Phone - 818-700-1000
Fax - 818-775-1302

Anthem Electronics Incorporated
1 Old Field Drive
East Irvine, CA 92718-2809
Phone - 714-768-4444
Fax - 714-768-6456

Anthem Electronics Incorporated
580 Menlo Drive, Suite 8
Rocklin, CA 95677
Phone - 916-624-9744
Fax - 916-624-9750

Anthem Electronics Incorporated
9369 Carroll Park Drive
San Diego, CA 92121
Phone - 619-453-9005
Fax - 619-546-7893

Hamilton Hallmark
3170 Pullman Street
Costa Mesa, CA 92626
Phone - 714-641-4100
Fax - 714-641-4122

Hamilton Hallmark
580 Menlo Drive, Suite 2
Rocklin, CA 95765
Phone - 916-624-9781
Fax - 916-961-0922

Hamilton Hallmark
4545 Viewridge Avenue
San Diego, CA 92123
Phone - 619-571-7540
Fax - 619-277-6136

Hamilton Hallmark
2105 Lundy Avenue
San Jose, CA 95131-1849
Phone - 408-435-3500
Fax - 408-435-3535

Hamilton Hallmark
21150 Califa Street
Woodland Hills, CA 91367
Phone - 818-594-0404
Fax - 818-594-8234

Wyle Laboratories
3000 Bowers Avenue
Santa Clara, CA 95051
Phone - 408-727-2500
Fax - 408-988-3479

Wyle Laboratories
17872 Cowan Avenue
Irvine, CA 92714
Phone - 714-863-9953
Fax - 714-863-0473

Wyle Laboratories
2951 Sunrise Blvd., Suite 175
Rancho Cordova, CA 95742
Phone - 916-638-5282
Fax - 916-638-1491

Wyle Laboratories
9525 Chesapeake Drive
San Diego, CA 92123
Phone - 619-565-9171
Fax - 619-565-0512

Wyle Laboratories
26010 Mureau Road, Suite 150
Calabasas, CA 91302
Phone - 818-880-9000
Fax - 818-880-5510

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

CANADA

Representatives

Clark-Hurman Associates
20 Regan Road, Unit 14
Brampton, Ontario L7A 1C3
Phone - 905-840-6066
Fax - 905-840-6091

Clark-Hurman Associates
308 Palladium Drive, Suite 200
Kanata, Ontario K2B 1A1
Phone - 613-599-5626
Fax - 613-599-5707

Clark-Hurman Associates
78 Donegani, Suite 200
Pointe Claire, Quebec H9R 2V4
Phone - 514-426-0453
Fax - 514-426-0455

Distributors

Hamilton Hallmark
8610 Commerce Court
Burnaby, BC V5A 4N6
Phone - 604-420-4101
Fax - 604-420-5376

Hamilton Hallmark
151 Superior Blvd., Unit 1-6
Mississauga, Ontario L5T 2L1
Phone - 905-564-6060
Fax - 905-564-6033

Hamilton Hallmark
190 Colonnade Road
Nepean, Ontario K2E 7J5
Phone - 613-226-1700
Fax - 613-226-1184

Hamilton Hallmark
Suite 600 7575 Transcanada Hwy.
Ville St. Laurent, Quebec H4T 1V6
Phone - 514-335-1000
Fax - 514-335-2481

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

COLORADO

Representative

Wescom Marketing
4860 Ward Road
Wheatridge, CO 80033
Phone - 303-422-8957
Fax - 303-422-9892

Distributors

Anthem Electronics Incorporated
373 Inverness Drive
Englewood, CO 80112
Phone - 303-790-4500
Fax - 303-790-4532

Hamilton Hallmark
12503 E. Euclid Drive, Suite 20
Englewood, CO 80111
Phone - 303-790-1662
Fax - 303-790-4991

Wyle Laboratories
451 E. 124th Street
Thornton, CO 80241
Phone - 303-457-9953
Fax - 303-457-4831

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

CONNECTICUT

Representative

Advanced Tech Sales Incorporated
Westview Office Park
Building 2, Suite 1C
850 N. Main Street Extension
Wallingford, CT 06492
Phone - 508-664-0888
Fax - 508-664-5503

Distributors

Anthem Electronics Incorporated
61 Mattatuck Heights
Waterbury, CT 06705
Phone - 203-575-1575
Fax - 203-596-3232

Hamilton Hallmark
125 Commerce Court, Unit 6
Cheshire, CT 06410
Phone - 203-271-2844
Fax - 203-272-1704

Wyle Laboratories
20 Chapin Road, Bldg. 1013
Pinebrook, NJ 07058
Phone - 201-882-8358
Phone - 800-862-9953
Fax - 201-882-9109

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

DELAWARE

Representative
Omega Electronic Sales Inc.
Four Neshaminy Interplex, Suite 101
Trevose, PA 19053
Phone - 215-244-4000
Fax - 215-244-4104

Distributor
Wyle Laboratories
815 Eastgate Drive
Mt. Laurel, NJ 08054
Phone - 609-439-9110
Fax - 609-439-9020

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

DISTRICT OF COLUMBIA

Representative
Electronic Engineering & Sales, Inc.
305 Kramer Road
Pasadena, MD 21122
Phone - 410-255-9686
Fax - 410-255-9688

Distributors
Anthem Electronics Incorporated
7168 A Columbia Gateway Drive
Columbia, MD 21046-2101
Phone - 301-995-6640
Fax - 301-381-4379

Hamilton Hallmark
10240 Old Columbia Road
Columbia, MD 21046
Phone - 410-988-9800
Fax - 410-381-2036

Wyle Laboratories
9101 Guilford Road, Suite 120
Columbia, MD 21046
Phone - 301-490-2170
Fax - 301-490-2190

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

FLORIDA

Representatives
Photon Sales, Inc.
1600 Sarno Road, Suite 21
Melbourne, FL 32935
Phone - 407-259-8999
Fax - 407-259-1323

Photon Sales, Inc.
715 Florida Street
Orlando, FL 32806
Phone - 407-841-7423
Fax - 407-896-6197

Distributors
Anthem Electronics Incorporated
598 S. Northlake Blvd., Suite 1024
Altamonte Springs, FL 32701
Phone - 407-831-0007
Fax - 407-831-6990

Anthem Electronics Incorporated
5200 N.W. 33rd Avenue, Suite 206
Ft. Lauderdale, FL 33309
Phone - 305-484-0990
Fax - 305-484-0951

Hamilton Hallmark
3350 NW 53rd Street, Suite 105-107
Ft. Lauderdale, FL 33309
Phone - 305-484-5482
Fax - 305-484-2995

Hamilton Hallmark
10491 72nd Street North
Largo, FL 34647
Phone - 813-541-7440
Phone - 800-282-9350
Fax - 813-544-4394

Hamilton Hallmark
7079 University Blvd.
Winter Park, FL 32792
Phone - 407-657-3300
Fax - 407-678-4414

Wyle Laboratories
1000 112th Circle North, Suite 800
St. Petersburg, FL 33716
Phone - 813-576-3004
Fax - 813-579-1518

Wyle Laboratories
600 W. Hillsboro Blvd., Suite 300
Deerfield Beach. FL 33441
Phone - 305-420-0500
Fax - 305-428-2134

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

GEORGIA

Representative
Southeast Technical Group
3500 Parkway Lane, Suite 420
Norcross, GA 30092
Phone - 404-416-6336
Fax - 404-416-6433

Distributors
Anthem Electronics Incorporated
3305 Breckenridge, Suite 108
Duluth, GA 30136
Phone - 404-931-3900
Fax - 404-931-3902

Hamilton Hallmark
3425 Corporate Way, Suite A and G
Duluth, GA 30136-2552
Phone - 404-623-4400
Fax - 404-476-8806

Wyle Laboratories
6025 The Corners Pkwy, Suite 111
Norcross, GA 30092
Phone - 404-441-9045
Fax - 404-441-9086

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

HAWAII

Representatives
Bay Area Electronics Sales, Inc.
2001 Gateway Place, Suite 315
San Jose, CA 95110
Phone - 408-452-8133
Fax - 408-452-8139

Bay Area Electronics Sales, Inc.
5711 Reinhold Street
Fair Oaks, CA 95628
Phone - 916-863-0563
Fax - 916-863-0615

Distributors

Anthem Electronics Incorporated
1160 Ridder Park Drive
San Jose, CA 95131
Phone - 408-453-1200
Fax - 408-441-4500

Hamilton Hallmark
2105 Lundy Avenue
San Jose, CA 95131-1849
Phone - 408-435-3500
Fax - 408-435-3535

Wyle Laboratories
3000 Bowers Avenue
Santa Clara, CA 95051
Phone - 408-727-2500
Fax - 408-988-3479

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

IDAHO

Representative

Contact Micron Semiconductor, Inc.
Component Sales
Phone - 208-368-3900
Fax - 208-368-3488
Micron DataFax - 208-368-5800

Distributors

Anthem Electronics Incorporated
1279 West 2200 South
Salt Lake City, UT 84119
Phone - 801-973-8555
Fax - 801-973-8909

Hamilton Hallmark
2105 Lundy Avenue
San Jose, CA 95131-1849
Phone - 408-435-3500
Fax - 408-435-3535

Wyle Laboratories
1325 West 2200 South, Suite E
Salt Lake City, UT 84119
Phone - 801-974-9953
Fax - 801-972-2524

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ILLINOIS

Representatives

Advanced Technical Sales (S. IL)
13755 St. Charles Rock Road
Bridgeton, MO 63044
Phone - 314-291-5003
Fax - 314-291-7958

Industrial Representatives, Inc. (N. IL)
8430 Gross Point Road
Skokie, IL 60077
Phone - 708-967-8430
Fax - 708-967-5903

Distributors

Anthem Electronics Incorporated
1300 Remington, Suite A
Schaumburg, IL 60173
Phone - 708-884-0200
Fax - 708-884-0480

Hamilton Hallmark
1130 Thorndale Avenue
Bensenville, IL 60106
Phone - 708-860-7780
Fax - 708-860-8530

Wyle Laboratories
2055 Army Trail Road, Suite 140
Addison, IL 60101
Phone - 708-620-0969
Fax - 708-620-1610

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

INDIANA

Representatives

Scott Electronics, Inc. (S. IN)
7321 Shadeland Station, Suite 256
Indianapolis, IN 46256
Phone - 317-841-0010
Fax - 317-841-0107

Scott Electronics, Inc. (N. IN)
Lima Valley Office Village
8109 Lima Road
Fort Wayne, IN 46818
Phone - 219-489-5690
Fax - 219-489-1842

Distributor

Hamilton Hallmark
4275 W. 96th Street
Indianapolis, IN 46268
Phone - 317-872-8875
Phone - 800-829-0146
Fax - 317-876-7165

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

IOWA

Representative

Advanced Technical Sales
375 Collins Road N.E.
Cedar Rapids, IA 52402
Phone - 319-393-8280
Fax - 319-393-7258

Distributors

Anthem Electronics Incorporated
7690 Golden Triangle Drive
Eden Prairie, MN 55344
Phone - 612-944-5454
Fax - 612-944-3045

Hamilton Hallmark
1130 Thorndale Avenue
Bensonville, IL 60106
Phone - 708-860-7780
Fax - 708-860-8530

Hamilton Hallmark
9401 James Avenue South, Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
Fax - 612-881-9461

Wyle Laboratories
1821 Walden Office Square, Suite 332
Schaumburg, IL 60173
Phone - 708-303-1040
Fax - 708-303-1055

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

KANSAS

Representative

Advanced Technical Sales
601 N. Mur-Len, Suite 8
Olathe, KS 66062
Phone - 913-782-8702
Fax - 913-782-8641

Distributors

Anthem Electronics Incorporated
8780 Mastin
Overland Park, KS 66212
Phone - 913-599-1528
Fax - 913-599-1326

Hamilton Hallmark
10809 Lakeview Avenue
Lenexa, KS 66215
Phone - 913-888-4747
Phone - 800-332-4375
Fax - 913-888-0523
Fax - 800-255-6946

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

KENTUCKY

Representative

Scott Electronics, Inc.
10901 Reed-Hartman Hwy., Suite 301
Cincinnati, OH 45242-2821
Phone - 513-791-2513
Fax - 513-791-8059

Distributor

Hamilton Hallmark
1847 Mercer Road, Suite G
Lexington, KY 40511
Phone - 800-327-4426 (IBM)
Phone - 800-525-0068 (DEC)

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

LOUISIANA

Representative

Nova Marketing Incorporated
8350 Meadow Road, Suite 174
Dallas, TX 75231
Phone - 214-265-4600
Fax - 214-265-4668

Distributors

Anthem Electronics
651 N. Plano Road, Suite 401
Richardson, TX 75081
Phone - 214-238-7100
Fax - 214-238-0237

Hamilton Hallmark
11420 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
Fax - 214-553-4395

Wyle Laboratories
1810 N. Greenville Avenue
Richardson, TX 75081
Phone - 214-235-9953
Fax - 214-644-5064

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MAINE

Representative

Advanced Tech Sales Inc.
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
Fax - 508-664-5503

Distributors

Anthem Electronics Incorporated
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
Fax - 508-657-6008

Hamilton Hallmark
10P Centennial Drive
Peabody, MA 01960
Phone - 508-532-9808
Fax - 508-532-9713

Wyle Laboratories
15 3rd Avenue
Burlington, MA 01803
Phone - 617-272-7300
Fax - 617-272-6809

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MARYLAND

Representative

Electronic Engineering & Sales, Inc.
305 Kramer Road
Pasadena, MD 21122
Phone - 410-255-9686
Fax - 410-255-9688

Distributors

Anthem Electronics Incorporated
7168 A Columbia Gateway Drive
Columbia, MD 21046-2101
Phone - 410-995-6640
Fax - 410-290-9862

Hamilton Hallmark
10240 Old Columbia Road
Columbia, MD 21046
Phone - 410-988-9800
Fax - 410-381-2036

Wyle Laboratories
7180 Columbia Gateway Drive, Suite 100
Columbia, MD 21046
Phone - 410-312-4844
Fax - 410-312-4953

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MASSACHUSETTS

Representative

Advanced Tech Sales, Inc.
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
Fax - 508-664-5503

Distributors

Anthem Electronics Incorporated
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
Fax - 508-657-6008

Hamilton Hallmark
10P Centennial Drive
Peabody, MA 01960
Phone - 508-532-9808
Fax - 508-532-9713

Wyle Laboratories
5 Oak Park Drive
Bedford, MA 01730
Phone - 617-271-9953
Fax - 617-275-3687

Wyle Laboratories
15 3rd Avenue
Burlington, MA 01803
Phone - 617-272-7300
Fax - 617-272-6809

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MICHIGAN

Representative

Rathsburg Associates Incorporated
41100 Bridge Street
Novi, MI 48375
Phone - 810-615-4000
Fax - 810-615-4001

Distributors

Hamilton Hallmark
41650 Gardenbrook Road, Suite 100
Novi, MI 49418
Phone - 313-347-4271
Fax - 313-347-4021

Hamilton Hallmark
44191 Plymouth Oaks Blvd. #1300
Plymouth, MI 48170
Phone - 313-416-5800
Phone - 800-767-9654
Fax - 313-416-5811

Wyle Laboratories
150 N. Patrick Blvd., Suite 150
Brookfield, WI 53045
Phone - 414-879-0434
Phone - 800-867-9953
Fax - 414-879-0474

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MINNESOTA

Representative

High Technology Sales Associates
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
Fax - 612-844-9930

Distributors

Anthem Electronics Incorporated
7646 Golden Triangle Drive, Suite 160
Eden Prairie, MN 55344
Phone - 612-944-5454
Fax - 612-944-3045

Hamilton Hallmark
9401 James Avenue South, Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
Fax - 612-881-9461

Wyle Laboratories
1325 East 79th Street, Suite 1
Bloomington, MN 55425
Phone - 612-853-2280
Fax - 612-853-2298

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MISSISSIPPI

Representative

Southeast Technical Group
4315 Hwy., 39 North
Northwood Place, Suite 3L
Meridian, MS 39305
Phone - 601-485-7055
Fax - 601-485-7063

Distributors

Anthem Electronics
4920-H Corporate Drive
Huntsville, AL 35805
Phone - 205-890-0302
Fax - 205-890-0130

Hamilton Hallmark
7079 University Blvd.
Winter Park, FL 32792
Phone - 407-657-3300
Fax - 407-678-4414

Wyle Laboratories
Tower Building, 2nd Floor
7800 Governers Drive West
Huntsville, AL 35807
Phone - 205-830-1119
Fax - 205-830-1520

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MISSOURI

Representative

Advanced Technical Sales
13755 St. Charles Rock Road
Bridgeton, MO 63044
Phone - 314-291-5003
Fax - 314-291-7958

Distributors

Hamilton Hallmark
3783 Rider Trail South
Earth City, MO 63045
Phone - 314-291-5350
Fax - 314-291-0362

Wyle Laboratories
1821 Walden Office Square, Suite 332
Schaumburg, IL 60173
Phone - 708-303-1040
Fax - 708-303-1055

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MONTANA

Representative

Contact Micron Semiconductor, Inc.
Component Sales
Phone - 208-368-3900
Fax - 208-368-3488
Micron DataFax - 208-368-5800

Distributor
Hamilton Hallmark
2105 Lundy Avenue
San Jose, CA 95131-1849
Phone - 408-435-3500
Fax - 408-435-3535

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEBRASKA

Representative
Advanced Technical Sales
601 North Mur-Len, Suite 8
Olathe, KS 66062
Phone - 913-782-8702
Fax - 913-782-8641

Distributors
Hamilton Hallmark
1130 Thorndale Avenue
Bensenville, IL 60106
Phone - 708-860-7780
Fax - 708-860-8530

Wyle Laboratories
451 E. 124th Street
Thornton, CO 80241
Phone - 303-457-9953
Fax - 303-457-4831

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEVADA

Representatives
Bay Area Electronics Sales, Inc.
2001 Gateway Place, Suite 315 W.
San Jose, CA 95110
Phone - 408-452-8133
Fax - 408-452-8139

Quatra Associates (Clark County)
4645 S. Lakeshore Drive, Suite 1
Tempe, AZ 85282
Phone - 602-820-7050
Fax - 602-820-7054

Distributors
Anthem Electronics Incorporated
580 Menlo Drive, Suite 8
Rocklin, CA 95677
Phone - 916-624-9744
Fax - 916-624-9750

Hamilton Hallmark
2105 Lundy Avenue
San Jose, CA 95131-1849
Phone - 408-435-3500
Fax - 408-435-3535

Wyle Laboratories
2951 Sunrise Blvd., Suite 175
Rancho Cordova, CA 95742
Phone - 916-638-5282
Fax - 916-638-1491

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEW HAMPSHIRE

Representative
Advanced Tech Sales Inc.
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
Fax - 508-664-5503

Distributors
Anthem Electronics Incorporated
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
Fax - 508-657-6008

Hamilton Hallmark
10P Centennial Drive
Peabody, MA 01960
Phone - 508-532-9808
Fax - 508-532-9713

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEW JERSEY

Representatives
Omega Electronic Sales Inc.
Four Neshaminy Interplex, Suite 101
Trevose, PA 19053
Phone - 215-244-4000
Fax - 215-244-4104

Parallax, Inc. (N. NJ)
734 Walt Whitman Road
Melville, NY 11747
Phone - 516-351-1000
Fax - 516-351-1606

Distributors
Anthem Electronics Incorporated
355 Business Center Drive
Horsham, PA 19044
Phone - 215-443-5150
Fax - 215-675-9875

Anthem Electronics Incorporated
26 Chapin Road, Unit K
Pine Brook, NJ 07058
Phone - 201-227-7960
Fax - 201-227-9246

Hamilton Hallmark
1 Keystone Avenue, Bldg. #36
Cherry Hill, NJ 08003
Phone - 609-424-0110
Fax - 609-751-2552

Hamilton Hallmark
10 Lanidex Plaza West
Parsippany, NJ 07054
Phone - 201-515-5300
Fax - 201-515-1601

Wyle Laboratories
20 Chapin Road, Bldg. 1013
Pinebrook, NJ 07058
Phone - 201-882-8358
Phone - 800-862-9953
Fax - 201-882-9109

Wyle Laboratories
815 Eastgate Drive
Mt. Laurel, NJ 08054
Phone - 609-439-9110
Fax - 609-439-9020

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEW MEXICO

Representative

Quatra Associates Incorporated
600 Autumnwood Place, S.E.
Albuquerque, NM 87123
Phone - 505-296-6781
Fax - 505-292-2092

Distributors

Anthem Electronics Incorporated
1555 W. 10th Place, Suite 101
Tempe, AZ 85281
Phone - 602-966-6600
Fax - 602-966-4826

Hamilton Hallmark
4637 South 36th Place
Phoenix, AZ 85040
Phone - 602-437-1200
Phone - 800-528-8471
Fax - 602-437-2348

Wyle Laboratories
4141 E. Raymond Street, Suite 1
Phoenix, AZ 85040
Phone - 602-437-2088
Fax - 602-437-2124

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEW YORK

Representatives

Electra Sales Corporation
333 Metro Park, Suite M103
Rochester, NY 14623
Phone - 716-427-7860
Fax - 716-427-0614

Electra Sales Corporation
6700 Old Collamer Road
East Syracuse, NY 13057
Phone - 315-463-1248
Fax - 315-463-1717

Parallax, Inc.
734 Walt Whitman Road
Melville, NY 11747
Phone - 516-351-1000
Fax - 516-351-1606

Distributors

Anthem Electronics-Military
47 Mall Drive
Commack, NY 11725-5703
Phone - 516-864-6600
Fax - 516-493-2244

Anthem Electronics Incorporated
26 Chapin Road, Unit K
Pinebrook, NJ 07058
Phone - 201-227-7960
Fax - 201-227-9246

Hamilton Hallmark
3075 Veterans Memorial Hwy.
Ronkonkoma, NY 11779
Phone - 516-737-0600
Fax - 516-737-0838

Hamilton Hallmark
933A Motor Parkway
Hauppauge, NY 11788
Phone - 516-434-7470
Fax - 516-434-7491

Hamilton Hallmark
1057 East Henrietta Road
Rochester, NY 14623
Phone - 716-475-9130
Phone - 800-462-6440
Fax - 716-475-9119

Wyle Laboratories
20 Chapin Road, Bldg. 1013
Pinebrook, NJ 07058
Phone - 201-882-8358
Phone - 800-862-9953
Fax - 201-882-9109

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NORTH CAROLINA

Representatives

Southeast Technical Group
4408 Ennismore Circle
Raliegh, NC 27613
Phone - 919-781-9857
Fax - 919-420-0274

Southeast Technical Group
1401 N. Arendell Avenue
Zebulon, NC 27597
Phone - 919-269-5589
Fax - 919-269-5670

Distributor

Hamilton Hallmark
5234 Green's Dairy Road
Raleigh, NC 27604
Phone - 919-872-0712
Fax - 919-878-8729

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NORTH DAKOTA

Representative

High Technology Sales Associates
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
Fax - 612-844-9930

Distributors

Anthem Electronics Incorporated
7646 Golden Triangle Drive, Suite 160
Eden Prairie, MN 55344
Phone - 612-944-5454
Fax - 612-944-3045

Hamilton Hallmark
9401 James Avenue South, Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
Fax - 612-881-9461

Wyle Laboratories
1325 E 79th Street, Suite 1
Bloomington, MN 55425
Phone - 612-853-2280
Fax - 612-853-2298

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

OHIO

Representatives

Scott Electronics, Inc.
30 Alpha Park
Cleveland, OH 44143-2240
Phone - 216-473-5050
Fax - 216-473-5055

Scott Electronics, Inc.
6728 Loop Road, Suite 202
Centerville, OH 45459
Phone - 513-291-9910
Fax - 513-291-9022

Scott Electronics, Inc.
916 Eastwind Drive
Westerville, OH 43081-3379
Phone - 614-882-6100
Fax - 614-882-0900

Scott Electronics, Inc.
10901 Reed-Hartman Hwy., Suite 301
Cincinnati, OH 45242-2821
Phone - 513-791-2513
Fax - 513-791-8059

Distributors

Anthem Electronics Incorporated
110 North High Street
Gahanna, OH 43230
Phone - 800-359-3517
Fax - 614-471-2879

Hamilton Hallmark
5821 Harper Road
Solon, OH 44139
Phone - 216-498-1100
Fax - 216-248-4803

Hamilton Hallmark
777 Dearborn Park Lane, Suite L
Worthington, OH 43085
Phone - 614-888-3313
Fax - 614-888-0767

Hamilton Hallmark
7760 Washington Village Drive
Dayton, OH 45459
Phone - 513-439-6735
Phone - 800-423-4688
Fax - 513-439-6711

Wyle Laboratories
1821 Walden Office Square, Suite 332
Schaumburg, IL 60173
Phone - 708-303-1040
Fax - 708-303-1055

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

OKLAHOMA

Representative

Nova Marketing Incorporated
8125D E. 51st Street, Suite 1339
Tulsa, OK 74145
Phone - 918-660-5105
Fax - 918-357-3450

Distributor

Hamilton Hallmark
12206 E. 51st Street, Suite 103
Tulsa, OK 74146
Phone - 918-254-6110
Fax - 918-254-6207

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

OREGON

Representative

Micron Sales Northwest, Inc.
AmberGlen Business Center
1600 N.W. Compton Drive, Suite 206
Beaverton, OR 97006
Phone - 503-531-2010
Fax - 503-531-2011

Distributors

Anthem Electronics Incorporated
9090 S.W. Gemini Drive
Beaverton, OR 97005
Phone - 503-643-1114
Fax - 503-626-7928

Hamilton Hallmark
9750 S.W. Nimbus Avenue
Beaverton, OR 97005
Phone - 503-526-6200
Fax - 503-641-5939

Wyle Laboratories
9640 Sunshine Court, Suite 200, Bldg. G
Beaverton, OR 97005
Phone - 503-643-7900
Fax - 503-646-5466

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

PENNSYLVANIA

Representatives

Omega Electronic Sales Incorporated (E. PA)
Four Neshaminy Interplex, Suite 101
Trevose, PA 19053
Phone - 215-244-4000
Fax - 215-244-4104

Scott Electronics, Inc. (W. PA)
916 Eastwind Drive
Westerville, OH 43081-3379
Phone - 614-882-6100
Fax - 614-882-0900

Distributors

Anthem Electronics Incorporated
355 Business Center Drive
Horsham, PA 19044
Phone - 215-443-5150
Fax - 215-675-9875

Hamilton Hallmark (W. PA)
5821 Harper Road
Solon, OH 44139
Phone - 216-498-1100
Fax - 216-248-4803

Wyle Laboratories
815 Eastgate Drive
Mt. Laurel, NJ 08054
Phone - 609-439-9110
Fax - 609-439-9020

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

PUERTO RICO

Representative

Photon Sales, Inc.
1600 Sarno Road, Suite 21
Melbourne, FL 32935
Phone - 407-259-8999
Fax - 407-259-1323

Distributors

Anthem Electronics
5200 N.W. 33rd Avenue, Suite 206
Ft. Lauderdale, FL 33309
Phone - 305-484-0900
Fax - 305-484-0951

Wyle Laboratories
600 West Hillsboro, Suite 300
Deerfield Beach, FL 33441
Phone - 305-420-0500
Fax - 305-428-2134

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

RHODE ISLAND

Representative

Advanced Tech Sales Inc.
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
Fax - 508-664-5503

Distributors

Anthem Electronics Incorporated
61 Mattatuck Heights
Waterbury, CT 06705
Phone - 203-575-1575
Fax - 203-596-3232

Hamilton Hallmark
125 Commerce Court, Unit 6
Cheshire, CT 06410
Phone - 203-271-2844
Fax - 203-272-1704

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SOUTH CAROLINA

Representative

Southeast Technical Group
1401 N. Arendell Avenue
Zebulon, NC 27597
Phone - 919-269-5589
Fax - 919-269-5670

Distributor

Hamilton Hallmark
5234 Green's Dairy Road
Raleigh, NC 27604
Phone - 919-872-0712
Fax - 919-878-8729

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SOUTH DAKOTA

Representative

High Technology Sales Associates
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
Fax - 612-844-9930

Distributors

Anthem Electronics Incorporated
7646 Golden Triangle Drive, Suite 160
Eden Prairie, MN 55344
Phone - 612-944-5454
Fax - 612-944-3045

Hamilton Hallmark
9401 James Avenue South, Suite 140
Bloomington, MN 55431
Phone - 612-881-2600
Fax - 612-881-9461

Wyle Laboratories
1325 East 79th Street, Suite 1
Bloomington, MN 55425
Phone - 612-853-2280
Fax - 612-853-2298

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

TENNESSEE

Representative

Southeast Technical Group
101 Washington, Suite 6
Huntsville, AL 35801
Phone - 205-534-2376
Fax - 205-534-2384

Distributors

Hamilton Hallmark
3425 Corporate Way, Suite A and G
Duluth, GA 30136-2552
Phone - 404-623-4400
Fax - 404-476-8806

Wyle Laboratories
Tower Building, 2nd Floor
7800 Governers Drive West
Huntsville, AL 35807
Phone - 205-830-1119
Fax - 205-830-1520

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

TEXAS

Representatives

Nova Marketing Incorporated
8350 Meadow Road, Suite 174
Dallas, TX 75231
Phone - 214-265-4600
Fax - 214-265-4668

Nova Marketing Incorporated
10701 Corporate Drive, Suite 140
Stafford, TX 77477
Phone - 713-240-6082
Fax - 713-240-6094

Nova Marketing Incorporated
8310 Capitol of Texas Hwy. North, Suite 180
Austin, TX 78731
Phone - 512-343-2321
Fax - 512-343-2487

Quatra Associates, Inc. (El Paso, TX)
600 Autumnwood Place, S.E.
Albuquerque, NM 87123
Phone - 505-296-6781
Fax - 505-292-2092

Distributors

Anthem Electronics Incorporated
651 N. Plano Road, Suite 401
Richardson, TX 75081
Phone - 214-238-7100
Fax - 214-238-0237

Anthem Electronics Incorporated
14050 Summit Drive, Suite 119
Austin, TX 78728
Phone - 512-388-0049
Fax - 512-388-0271

Hamilton Hallmark
12211 Technology Blvd.
Austin, TX 78727
Phone - 512-258-8848
Fax - 512-258-3777

Hamilton Hallmark
11420 Pagemill Road
Dallas, TX 75243
Phone - 214-553-4300
Fax - 214-553-4395

Hamilton Hallmark
8000 Westglen
Houston, TX 77063
Phone - 713-781-6100
Fax - 713-953-8420

Wyle Laboratories
4030 W. Braker Lane, Suite 420
Austin, TX 78759
Phone - 512-345-8853
Fax - 512-834-0981

Wyle Laboratories
1810 N. Greenville Avenue
Richardson, TX 75081
Phone - 214-235-9953
Fax - 214-644-5064

Wyle Laboratories
11001 S. Wilcrest, Suite 100
Houston, TX 77099
Phone - 713-879-9953
Fax - 713-879-6540

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

UTAH

Representative

Wescom Marketing
3500 S. Main, Suite 100
Salt Lake City, UT 84115
Phone - 801-269-0419
Fax - 801-269-0665

Distributors

Anthem Electronics Incorporated
1279 West 2200 South
Salt Lake City, UT 84119
Phone - 801-973-8555
Fax - 801-973-8909

Hamilton Hallmark
1100 East 6600 South, Suite 120
Salt Lake City, UT 84121
Phone - 801-266-2022
Fax - 801-263-0104

Wyle Laboratories
1325 West 2200 South, Suite E
Salt Lake City, UT 84119
Phone - 801-974-9953
Fax - 801-972-2524

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

VERMONT

Representative

Advanced Tech Sales Inc.
348 Park Street, Suite 102
North Reading, MA 01864
Phone - 508-664-0888
Fax - 508-664-5503

Distributors

Anthem Electronics Incorporated
36 Jonspin Road
Wilmington, MA 01887
Phone - 508-657-5170
Fax - 508-657-6008

Hamilton Hallmark
10P Centennial Drive
Peabody, MA 01960
Phone - 508-532-9808
Fax - 508-532-9713

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

VIRGINIA

Representative

Electronic Engineering & Sales, Inc.
305 Kramer Road
Pasadena, MD 21122
Phone - 410-255-9686
Fax - 410-255-9688

Distributors

Anthem Electronics Incorporated
7168 A Columbia Gateway Drive
Columbia, MD 21046-2101
Phone - 301-995-6640
Fax - 301-381-4379

Hamilton Hallmark
10240 Old Columbia Road
Columbia, MD 21046
Phone - 410-988-9800
Fax - 410-381-2036

Wyle Laboratories
7180 Columbia Gateway Drive, Suite 100
Columbia, MD 21046
Phone - 410-312-4844
Fax - 410-312-4953

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

WASHINGTON

Representative

Micron Sales Northwest, Inc.
14901 N.E. 147th Place
Woodinville, WA 98072
Phone - 206-486-2775
Fax - 206-486-3960

Distributors

Anthem Electronics Incorporated
19017-120th Avenue N.E., Suite 102
Bothell, WA 98011
Phone - 206-483-1700
Fax - 206-486-0571

Hamilton Hallmark
8216 154th Avenue N.E.
Redmond, WA 98052
Phone - 206-882-7000
Fax - 206-882-7070

Wyle Laboratories
15385 N.E. 90th Street
Redmond, WA 98052-3522
Phone - 206-881-1150
Phone - 800-248-9953
Fax - 206-881-1567

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

WEST VIRGINIA

Representative

Scott Electronics, Inc.
916 Eastwind Drive
Westerville, OH 43081-3379
Phone - 614-882-6100
Fax - 614-882-0900

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

WISCONSIN

Representatives

High Technology Sales Associates (W. WI)
4801 W. 81st Street, Suite 115
Bloomington, MN 55437
Phone - 612-844-9933
Fax - 612-844-9930

Industrial Representatives, Inc. (E. WI)
2831 N. Grandview, Suite 215
Pewaukee, WI 53072
Phone - 414-574-9393
Fax - 414-574-9394

Distributors

Anthem Electronics Incorporated
1300 Remington, Suite A
Schaumburg, IL 60173
Phone - 708-884-0200
Fax - 708-884-0480

Hamilton Hallmark
2440 S. 179th Street
New Berlin, WI 53146-2152
Phone - 414-797-7844
Fax - 414-797-9259

Wyle Laboratories
150 N. Patrick Blvd., Suite 150
Brookfield, WI 53045
Phone - 414-879-0434
Phone - 800-867-9953
Fax - 414-879-0474

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

WYOMING

Representative

Contact Micron Semiconductor, Inc.
Component Sales
Phone - 208-368-3900
Fax - 208-368-3488
Micron DataFax - 208-368-5800

Distributors

Anthem Electronics Incorporated
373 Inverness Drive
Englewood, CO 80112
Phone - 303-790-4500
Fax - 303-790-4532

Wyle Laboratories
1325 West 2200 South, Suite E
Salt Lake City, UT 84119
Phone - 801-974-9953
Fax - 801-972-2524

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

AUSTRALIA

Representative

Reptechnic Pty. Ltd.
3/36 Bydown Street
Neutral Bay, NSW 2089
Phone - 612-953-9844
Fax - 612-953-9683

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

AUSTRIA

Distributor

EBV Elektronik GmbH
Diefenbachgasse 35/6
A-1150 Wien
Phone - 43-222-8-94-17-74
Fax - 43-222-8-94-17-75

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

BELGIUM

Representative

Microtron
Generaal De Wittelaan 7
B-2800 Mechelen
Phone - 32-15-212223
Fax - 32-15-210069

Distributor

EBV Elektronik GmbH
Excelsiorlaan 35
B-1930 Zaventem
Phone - 32-2 7209936
Fax - 32-2-7208152

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

DENMARK

Representative & Distributor

E.V. Johanssen Elektronik A/S
Titangade 15
DK-2200 Copenhagen N
Phone - 45-31-83-90-22
Fax - 45-31-83-92-22

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

FINLAND

Representative & Distributor

Integrated Electronics Oy Ab
Turkhaudantie 1
P.O. Box 160
SF-00700 Helsinki
Phone - 358-0-351-3133
Fax - 358-0-351-3134

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

FRANCE

Representative

Rep'Tronic S.A.
1 bis, rue Marcel Paul
Bâtiment A,
Z.I. de la Bonde
F-91300 Massy
Phone - 33-1-60-13-93-00
Fax - 33-1-60-13-91-98

Distributors

Avnet EMG SA
79, rue Pierre Semard
B.P. 90
F-92322 Chatillon, Cedex
Phone - 33-1-49-65-2600
Fax - 33-1-49-65-2769

EBV Elektronik
Parc Club de la Haute Maison
16, rue Galilée, Cité Descartes
77420 Champs-sur-Marne
Phone - 33-1-64-68-8609
Fax - 33-1-64-68-2767

Société Paris Sud Electronique
12, rue René-Cassin
Z.I. de la Bonde
F-91300 Massy
Phone - 33-1-69-20-6699
Fax - 33-1-69-20-7532

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

GERMANY

Sales & Customer Service Office

Micron Semiconductor (Deutschland) GmbH
Sternstrasse 20
D-85609 Aschheim
Phone - 49-89-9030021
Fax - 49-89-9043114

Distributors

EBV Elektronik GmbH
Hans-Pinsel-Str. 4
D-85540 Haar b. München
Phone - 49-89-45610-0
Fax - 49-89-464488

MSC-Vertriebs GmbH
Industriestraße 16
D-76297 Stutensee
Phone - 49-72-49910-0
Fax - 49-72-497993

Metronik GmbH
Leonhardsweg 2
D-82008 Unterhaching b. München
Phone - 49-89-61108-0
Fax - 49-89-6116468

Neumüller-Fenner Elektronik GmbH
Mehlbeerenstr. 2
D-82024 Taufkirchen
Phone - 49-89-6144990
Fax - 49-89-61449980

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

HONG KONG

Sales & Customer Service Office

Micron Semiconductor Asia Pacific Pte Ltd
629 Aljunied Road #07-21
Cititech Industrial Bldg.
Singapore 1438
Phone - 65-841-4066
Fax - 65-841-4166

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

INDIA

Distributor

Pandori Electronics Pvt Ltd
306, Guru Ram Das Bhawan
Ranjit Nagar,
Commercial Complex
New Delhi 110008
Phone - 91-11-5703615
Fax - 91-11-5700478

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

INDONESIA

Representative

Desner Electronics (FE) Pte. Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
Fax - 65-284-9466

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

IRELAND

Representative

New England Technical Sales
The Diamond,
Malahide,
Co. Dublin
Phone - 353-18-450635
Fax - 353-18-453625

Distributor

Macro Group
Merrion Business Corp.
20 Upper Merrion Street
Dublin 2
Phone - 1-67-66-904
Fax - 1-76-0-713

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ISRAEL

Representative & Distributor

C.R.G. Electronics Ltd.
Industrial Park
P.O.B. 590
Carmiel 20101
Phone - 972-4-887-877
Fax - 972-4-887-588

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

ITALY

Representative

Acsis srl
via Alberto Mario, 26
Milano 20149
Phone - 39-2-4802-2522
Fax - 39-2-4801-2289

Distributors

Claitron SPA
Via le Fulvio Testi 280/B
20126 Milano
Phone - 39-2-66-14-91
Fax - 39-2-66-10-56-66

EBV Elektronik
Sede di Milano
Via C. Frova, 34
I-20092 Cinisello Balsamo (MI)
Phone - 39-2-66-01-71-11
Fax - 39-2-66-01-7020

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

JAPAN

Distributors

Internix Inc.
Shinjuku Hamada Bldg. 7-4-7
Nishi-Shinjuku, Shinjuku-ku
Tokyo 160
Phone - 81-3-3369-1105
Fax - 81-3-3363-8486

Macnica, Inc.
Hakusan High-Tech Park
1-22-2 Hakusan
Midori-ku, Yokohama City 226
Phone - 81-45-939-6140
Fax - 81-45-939-6141

Sanyo Electric Co. Ltd.
Import Promotion Division
1-1-10 Ueno
Taito-ku, Tokyo 110
Phone - 81-3-3837-6345
Fax - 81-3-3837-6379

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

KOREA

Representative

I & C Microsystems Co. Ltd.
3rd Floor, Jung-Nam Bldg.
191-3 Poi-Dong
Kangnam-Ku
Seoul
Phone - 822-577-9131
Fax - 822-577-9130

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

LUXEMBOURG

Representative
Microtron
Beneluxweg 37
Postbus 4336
NL-4904 SJ Oosterhout
Phone - 31-162-060-308
Fax - 31-162-060-633

Distributor
EBV Elektronik GmbH
Excelsiorlaan 35
B-1930 Zaventem
Belgium
Phone - 32-2 7209936
Fax - 32-2-7208152

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

MALAYSIA

Representatives
Desner (Malaysia) Sdn. Bhd.
23 Jalan Sarikei
53000 Kuala Lumpur
Phone - 60-3-4211123
Fax - 60-3-4219923

Desner (Malaysia) Sdn. Bhd.
39 Persiaran Bukit Kecil 5
Taman Sri Nibong
11900 Bayan Lepas
Penang
Phone - 60-4-838352
Fax - 60-4-849370

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

THE NETHERLANDS

Representative
Microtron
Beneluxweg 37
Postbus 4336
NL-4904 SJ Oosterhout
Phone - 31-162-060-308
Fax - 31-162-060-633

Distributor
EBV Elektronik GmbH
Planetenbaan 2
NL-3606 AK Maarssenbroek
Phone - 31 34 65-62353
Fax - 31 34 65-64277

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NEW ZEALAND

Representative
Reptechnic Pty. Ltd.
3/36 Bydown Street
Neutral Bay, NSW 2089
Australia
Phone - 612-953-9844
Fax - 612-953-9683

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

NORWAY

Representative & Distributor
BIT Elektronikk A/S
Smedsvingen 4
Postboks 194
1360 Nesbru
Phone - 47-66-981370
Fax - 47-66-981371

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

PHILLIPINES

Representative
Desner Electronics (FE) Pte. Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
Fax - 65-284-9466

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

PORTUGAL

Distributor
EBV Elektronik
Calle Maria Tubau, 5
28050 Madrid
Phone - 34-1-358-8608
Fax - 34-1-358-8560

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SINGAPORE

Sales & Customer Service Office
Micron Semiconductor Asia Pacific Pte Ltd
629 Aljunied Road #07-21
Cititech Industrial Bldg.
Singapore 1438
Phone - 65-841-4066
Fax - 65-841-4166

Representative
Desner Electronics (FE) Pte. Ltd.
42 Mactaggart Road
#04-01 Mactaggart Bldg.
Singapore 1336
Phone - 65-285-1566
Fax - 65-284-9466

Die Distributor
Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SOUTH AFRICA

Distributor

Computer Parts cc
CNR Athol and Louis Botha Avenue
Highlands North
Johannesburg 2192
Phone - 27-11-887-2438
Fax - 27-11-887-2514

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SPAIN

Distributor

EBV Elektronik
Calle Maria Tubau, 5
28050 Madrid
Phone - 34-1-358-8608
Fax - 34-1-358-8560

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SWEDEN

Representative & Distributor

IE Komponenter AB
Ulvsundavägen 106 C
Box 11 113
S-161 11 Bromma
Phone - 46-8-804685
Fax - 46-8-262286

Die Distributor

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 32810-2696
Phone - 407-298-7100
Fax - 407-290-0164

SWITZERLAND

Distributors

EBV Elektronik GmbH
Vorstadtstrasse 37
CH-8953 Dietikon
Phone - 41 1-7 40 10 90
Fax - 41 1-7 41 51 10

Fenner Elektronik AG
Gewerbestraße 10
CH-4450 Sissach
Phone - 41 6-1 97 50 00 0
Fax - 41 6-1 97 17 42 1

Die Distributor

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NOTES

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