MITSUBISHI SEMICONDUCTORS 1989

SINGLE-CHIP 8-BIT MICROCOMPUTERS

DATA BOOK

MITSUBISHI ELECTRIC

MITSUBISHI SEMICONDUCTORS 1989

SINGLE-CHIP 8-BIT MICROCOMPUTERS

DATA BOOK

MITSUBISHI ELECTRIC

All values shown in this catalogue are subject to change for product improvement.

The information, diagrams and all other data included herein are believed to be correct and reliable. However, no responsibility is assumed by Mitsubishi Electric Corporation for their use, nor for any infringements of patents or other rights belonging to third parties which may result from their use.

CONTENTS

1 GUIDANCE

2 SERIES MELPS 740 SINGLE-CHIP 8-BIT MICROCOMPUTERS

CONTENTS

3 EXTENDED OPERATING TEMPERATURE VERSION OF MICROCOMPUTERS

4 PIGGYBACK TYPE MICROCOMPUTERS

5 BUILT-IN EPROM TYPE MICROCOMPUTERS

6 APPENDICES

Contact Addresses for Further Information

GUIDANCE 1

INDEX BY FUNCTION

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics: Typ. pwr dissipation (mW)	Electrical characteristics: Min. cycle time (μs)	Electrical characteristics: Max. frequency (MHz)	Package	Page
■Series MELPS 740 single-chip microcomputers								
M50708-XXXSP/FP	6K-Byte Mask-Prog. ROM, 128-Byte RAM, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	2—28
M50740A-XXXSP/FP	3K-Byte Mask-Prog. ROM, 96-Byte RAM	C, Si	5±10%	15	2	4	52P4B/50P6	2—3
M50740ASP	External ROM type, 96-Byte RAM	C, Si	5±10%	15	2	4	52P4B	2—3
M50741-XXXSP/FP	4K-Byte Mask-Prog. ROM, 96-Byte RAM	C, Si	5±10%	15	2	4	52P4B/50P6	2—3
M50742-XXXSP/FP	4K-Byte Mask-Prog. ROM, 128-Byte RAM, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	2—28
M50743-XXXSP/FP	4K-Byte Mask-Prog. ROM, 128-Byte RAM	C, Si	5±10%	30	1	8	64P4B/72P6	2—54
M50744-XXXSP/FP	4K-Byte Mask-Prog. ROM, 144-Byte RAM	C, Si	5±10%	15	2	4	64P4B/72P6	2—80
M50745-XXXSP/FP	6K-Byte Mask-Prog. ROM, 192-Byte RAM	C, Si	5±10%	15	2	4	64P4B/60P6	2—108
M50746-XXXSP/FP	6K-Byte Mask-Prog. ROM, 144-Byte RAM	C, Si	5±10%	15	2	4	64P4B/72P6	2—80
M50747-XXXSP/FP	8K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	5±10%	30	1	8	64P4B/72P6	2—134
M50747H-XXXSP/FP	8K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	5±5%	45	0.67	12	64P4B/72P6	2—164
M50752-XXXSP	4K-Byte Mask-Prog. ROM, 128-Byte RAM, High voltage port, CR oscillation type	C, Si	5±10%	15	2	4	52P4B	2—175
M50753-XXXSP/FP	6K-Byte Mask-Prog. ROM, 96-Byte RAM, 8-bit A-D converter	C, Si	5±10%	15	2	4	64P4B/60P6	2—199
M50754-XXXSP/FP/GP	6K-Byte Mask-Prog. ROM, 160-Byte RAM, PWM, High voltage port, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6/ 64P6W	2—228
M50757-XXXSP	3K-Byte Mask-Prog. ROM, 96-Byte RAM, High voltage port, CR oscillation type	C, Si	5±10%	15	2	4	52P4B	2—175
M50758-XXXSP	3K-Byte Mask-Prog. ROM, 96-Byte RAM, High voltage port, Ceramic oscillation type	C, Si	5±10%	15	2	4	52P4B	2—175
M50930-XXXFP	4K-Byte Mask-Prog. ROM, 128-Byte RAM, LCD controller/driver, Serial I/O	C, Si	5±10%	20	1.86	4.3	80P6	2—265
M50931-XXXFP	4K-Byte Mask-Prog. ROM, 512-Byte RAM, LCD controller/driver, Serial I/O	C, Si	5±10%	20	1.86	4.3	80P6	2—265
M50932-XXXFP	8K-Byte Mask-Prog. ROM, 512-Byte RAM, LCD controller/driver, Serial I/O	C, Si	5±10%	20	1.86	4.3	80P6	2—265
M50940-XXXSP/FP	4K-Byte Mask-Prog. ROM, 128-Byte RAM, 8-bit A-D converter, High voltage port, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	2—300
M50941-XXXSP/FP	8K-Byte Mask-Prog. ROM, 192-Byte RAM, 8-bit A-D converter, High voltage port, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	2—300
M50943-XXXSP/FP	8K-Byte Mask-Prog. ROM, 192-Byte RAM, 8-bit A-D converter, Serial I/O	C, Si	5±10%	30	1	8	64P4B/60P6	2—334
M50944-XXXSP/FP ★★	12K-Byte Mask-Prog. ROM, 192-Byte RAM, 8-bit A-D converter, Two serial I/Os	C, Si	5±10%	15	1.91	4.19	64P4B/64P6S	2—364
M50950-XXXSP	6K-Byte Mask-Prog. ROM, 144-Byte RAM, High voltage port, Two serial I/Os	C, Si	5±10%	20	1.6	5	52P4B	2—400
M50951-XXXSP	4K-Byte Mask-Prog. ROM, 144-Byte RAM, High voltage port, Two serial I/Os	C, Si	5±10%	20	1.6	5	52P4B	2—400
M50954-XXXSP/FP/GP	8K-Byte Mask-Prog. ROM, 192-Byte RAM, PWM, High voltage port, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6/ 64P6W	2—228
M50955-XXXSP/FP/GP	10K-Byte Mask-Prog. ROM, 192-Byte RAM, PWM, High voltage port, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6/ 64P6W	2—228
M50957-XXXSP/FP	10K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, High voltage port, 4-bit comparator, Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6	2—433
M50959-XXXSP/FP	16K-Byte Mask-Prog. ROM, 256-Byte RAM, PWM, High voltage port, 4-bit comparator Serial I/O	C, Si	4~5.5	20	1.90	4.2	64P4B/72P6	2—433
M50963-XXXSP/FP	10K-Byte Mask-Prog. ROM, 160-Byte RAM, 8-bit A-D converter, 5-bit D-A converter PWM, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	2—472
M50964-XXXSP/FP	6K-Byte Mask-Prog. ROM, 160-Byte RAM, 8-bit A-D converter, 5-bit D-A converter PWM, Serial I/O	C, Si	5±10%	15	2	4	64P4B/72P6	2—472

★★ : Under development

INDEX BY FUNCTION

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics: Typ. pwr dissipation (mW)	Electrical characteristics: Min. cycle time (μs)	Electrical characteristics: Max. frequency (MHz)	Package	Page
M37410M3-XXXFP ★★	6K-Byte Mask-Prog. ROM, 192-Byte RAM, Serial I/O, A-D converter, LCD controller/driver	C, Si	5±10%	30	1	8	80P6S	2—503
M37410M4-XXXFP ★★	8K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	5±10%	30	1	8	80P6S	2—503
M37415M4-XXXFP ★★	8K-Byte Mask-Prog. ROM, 512-Byte RAM, LCD controller/driver, Serial I/O, DTMF generator	C, Si	4.5~5.5	20	2.5	3.2	80P6	2—534
M37450M2-XXXSP/FP ★	4K-Byte Mask-Prog. ROM, 128-Byte RAM, 8-bit A-D converter, 8-bit D-A converter, UART, DBB, 3-Timer, PWM	C, Si	5±10%	30	0.8	10	64P4B/80P6	2—565
M37450M4-XXXSP/FP ★	8K-Byte Mask-Prog. ROM, 256-Byte RAM	C, Si	5±10%	30	0.8	10	64P4B/80P6	2—565
M37450M8-XXXSP/FP ★	16K-Byte Mask-Prog. ROM, 384-Byte RAM	C, Si	5±10%	30	0.8	10	64P4B/80P6	2—565
M50734SP/FP	External ROM and RAM type, 5-Timer, 8-bit A-D converter, Serial I/O	C, Si	5±10%	30	1	8	64P4B/72P6	2—625
M50734SP-10	External ROM and RAM type, 5-Timer, 8-bit A-D converter, Serial I/O	C, Si	5±10%	35	0.8	10	64P4B	2—663
M37450S1SP/FP ★	External ROM type 128-Byte RAM	C, Si	5±10%	30	0.8	10	64P4B/80P6	2—608
M37450S2SP/FP ★	External ROM type 256-Byte RAM	C, Si	5±10%	30	0.8	10	64P4B/80P6	2—608
M37450S4SP/FP ★	External ROM type 384-Byte RAM	C, Si	5±10%	30	0.8	10	64P4B/80P6	2—608

★ : New product ★★ : Under development

INDEX BY FUNCTION

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics: Typ. pwr dissipation (mW)	Electrical characteristics: Min. cycle time (μs)	Electrical characteristics: Max. frequency (MHz)	Package	Page
■Extended operating temperature version of microcomputers								
M50744T-XXXSP ★	4K-Byte Mask-Prog. ROM,144-Byte RAM Extended operating temperature version of M50744-XXXSP	C, Si	5±10%	15	2	4	64P4B	3—3
M50747T-XXXSP ★	8K-Byte Mask-Prog. ROM,256-Byte RAM Extended operating temperature version of M50747-XXXSP	C, Si	5±10%	30	1	8	64P4B	3—7
M50753T-XXXSP ★	6K-Byte Mask-Prog. ROM,96-Byte RAM Extended operating temperature version of M50753-XXXSP	C, Si	5±10%	15	2	4	64P4B	3—11
M50930T-XXXFP ★	4K-Byte Mask-Prog. ROM,128-Byte RAM Extended operating temperature version of M50930-XXXFP	C, Si	5±10%	20	1.86	4.3	80P6	3—18
■Piggyback type microcomputers (EPROM mounted type)								
M50740-PGYS	Piggyback for M50740/M50741	C, Si	5±5%	—	2	4	52S1M	4—3
M50742-PGYS	Piggyback for M50742/M50708	C, Si	5±5%	—	2	4	64S1M	4—8
M50743-PGYS	Piggyback for M50743	C, Si	5±5%	—	1	8	64S1M	4—13
M50745-PGYS	Piggyback for M50745	C, Si	5±5%	—	2	4	64S1M	4—18
M50752-PGYS	Piggyback for M50757/M50752	C, Si	5±5%	—	2	4	52S1M	4—23
M50753-PGYS	Piggyback for M50753	C, Si	5±5%	—	2	4	64S1M	4—28
M50931-PGYS	Piggyback for M50930/M50931/M50932	C, Si	5±5%	—	2	4	80S6M	4—34
M50941-PGYS	Piggyback for M50940/M50941	C, Si	5±5%	—	2	4	64S1M	4—41
M50950-PGYS	Piggyback for M50950/M50951	C, Si	5±5%	—	1.6	5	52S1M	4—48
M50955-PGYS	Piggyback for M50754/M50954/M50955	C, Si	5±5%	—	1.9	4.2	64S1M	4—54
M50964-PGYS	Piggyback for M50964/M50963	C, Si	5±5%	—	2	4	64S1M	4—60
M37450PSS ★	Piggyback for M37450M2/M4/M8-XXXSP	C, Si	5±5%	—	0.8	10	64S1M	4—66
M37450PFS ★	Piggyback for M37450M2/M4/M8-XXXFP	C, Si	5±5%	—	0.8	10	80S6M	4—72
■Built-in EPROM type microcomputers								
M50746E-XXXSP/FP	One time programmable version of M50746-XXXSP/FP	C, Si	5±5%	15	2	4	64P4B/72P6	5—3
M50746ES/EFS	EPROM version of M50746-XXXSP/FP	C, Si	5±5%	15	2	4	64S1B/72S6	5—3
M50747E-XXXSP/FP	One time programmable version of M50747-XXXSP/FP	C, Si	5±5%	30	1	8	64P4B/72P6	5—18
M50747ES/EFS	EPROM version of M50747-XXXSP/FP	C, Si	5±5%	30	1	8	64S1B/72S6	5—18
M50944E-XXXSP/FP ★★	One time programmable version of M50944-XXXSP/FP	C, Si	5±5%	15	2	4	64P4B/64P6S	5—32
M50944ES ★★	EPROM version of M50944-XXXSP	C, Si	5±5%	15	2	4	64S1B	5—32
M50957E-XXXSP ★★	One time programmable version of M50957-XXXSP	C, Si	5±5%	20	1.9	4.2	64P4B	5—47
M50957ES ★★	EPROM version of M50957-XXXSP	C, Si	5±5%	20	1.9	4.2	64S1B	5—47
M50963E-XXXSP/FP	One time programmable version of M50963-XXXSP	C, Si	5±5%	15	2	4	64P4B/72P6	5—57
M50963ES/EFS	EPROM version of M50963-XXXSP/FP	C, Si	5±5%	15	2	4	64S1B/72P6	5—57
M37410E6-XXXFP ★★	One time programmable version of M37410M4-XXXFP	C, Si	5±5%	30	1	8	80P6S	5—72
M37450E4-XXXSP/FP ★	One time programmable version of M37450M4-XXXSP/FP	C, Si	5±5%	30	0.8	10	64P4B/80P6	5—81
M37450E4SS/FS ★	EPROM version of M37450M4-XXXSP/FP	C, Si	5±5%	30	0.8	10	64S1B/80S6	5—81

★ : New product ★★ : Under development

INDEX BY FUNCTION

Type	Circuit function and organization	Structure	Supply voltage (V)	Electrical characteristics: Typ. pwr dissipation (mW)	Electrical characteristics: Min. cycle time (μs)	Electrical characteristics: Max. frequency (MHz)	Package	Remarks
■Series MELPS 8-48 8-bit microcomputer								
M5L8048-XXXP	1K-Byte Mask-Prog. ROM, 64-Byte RAM	N,Si,ED	5±10%	325	2.5	6	40P4	Note 2
M5L8035LP	External ROM type, 64-Byte RAM	N,Si,ED	5±10%	325	2.5	6	40P4	Note 2
M5L8049-XXXP M5L8049-XXXP-6	2K-Byte Mask-Prog. ROM, 128-Byte RAM	N,Si,ED	5±10%	500 500	1.36 2.5	11 6	40P4	Note 2
M5L8039P-11 M5L8039P-6	External ROM type, 128-Byte RAM	N,Si,ED	5±10%	500 500	1.36 2.5	11 6	40P4	Note 2
M5L8049H1-XXXP	2K-Byte Mask-Prog. ROM, 128-Byte RAM	N,Si,ED	5±10%	350	1.07	14	40P4	Note 2
M5L8039HLP-14	External ROM type, 128-Byte RAM	N,Si,ED	5±10%	350	1.07	14	40P4	Note 2
M5M80C49A-XXXP M5M80C49H-XXXP	2K-Byte Mask-Prog. ROM, 128-Byte RAM	C,Si	5±10%	25	1.36	11	40P4	Note 2
M5M80C39AP M5M80C39HP	External ROM type, 128-Byte RAM	C,Si	5±10%	25	1.36	11	40P4	Note 2
M5MC49A-XXXFP M5MC49H-XXXFP	2K-Byte Mask-Prog. ROM, 128-Byte RAM	C,Si	5±10%	25	1.36	11	42P6	Note 2
M5M8050H-XXXP	4K-Byte Mask-Prog. ROM, 256-Byte RAM	N,Si,ED	5±10%	350	1.36	11	40P4	Note 2
M5M8040HP	External ROM type, 256-Byte RAM	N,Si,ED	5±10%	350	1.36	11	40P4	Note 2
M5M8050L-XXXP	4K-Byte Mask-Prog. ROM, 256-Byte RAM	N,Si,ED	5±10%	250	2.5	6	40P4	Note 2
M5M8040LP	External ROM type, 256-Byte RAM	N,Si,ED	5±10%	250	2.5	6	40P4	Note 2
■Series MELPS 8-41 8-bit microcomputer								
M5L8041A-XXXP	Universal peripheral interface 1K-Byte Mask-Prog. ROM, 64-Byte RAM	N,Si,ED	5±10%	300	2.5	6	40P4	Note 2
M5L8041AH-XXXP	Universal peripheral interface 1K-Byte Mask-Prog. ROM, 64-Byte RAM	N,Si,ED	5±10%	450	1.25	12	40P4	Note 2
M5L8042-XXXP	Universal peripheral interface 2K-Byte Mask-Prog. ROM, 128-Byte RAM	N,Si,ED	5±10%	450	1.25	12	40P4	Note 2
■LSIs for pheripheral circuit								
M50790SP	I/O Expander(CE = low active)	C,Al	4~14	—	—	—	52P4B	Note 3
M50791SP	I/O Expander(CE = low active)	C,Al	4~11	—	—	—	52P4B	Note 3
M5L8243P	I/O Expander	N,Si,ED	5±10%	—	—	—	24P4	Note 2
M5M82C43P	I/O Expander	C,Si	5±10%	—	—	—	24P4	Note 2
M5M82C43FP	I/O Expander	C,Si	5±10%	—	—	—	24P2W	Note 2

Note 1. Al=Aluminum gate. C=CMOS. ED=Enhancement depletion mode. N=N-channel. Si=Silicon gate
Note 2. Refor to 1987 MITSUBISHI SEMICONDUCTORS SINGLE-CHIP 8-BIT MICROCOMPUTERS Vol. 2.
Note 3. Refor to 1986 MITSUBISHI SEMICONDUCTORS SINGLE-CHIP 8-BIT MICROCOMPUTERS.

Development support systems

Type	Development support systems	Host machine	Assembler	Debugging machine			Evaluation board or piggyback
				Main unit	Option board	Software	
CMOS 8-bit Series MELPS 740	M50740A-XXXSP/FP M50741-XXXSP/FP M50740ASP	16-bit personal computer (MS-DOS) (Note 2)	ASM745 RASM745 SAMS745★	PC4000E	PCA4040	SDT745	M50740-PGYS
	M50742-XXXSP/FP M50708-XXXSP/FP				PCA4042		M50742-PGYS
	M50743-XXXSP/FP				PCA4043		M50743-PGYS
					PAC4043R	RTT745	
	M50744-XXXSP/FP M50744T-XXXSP M50746-XXXSP/FP M50746E-XXXSP/FP M50746ES/EFS				PCA4044G02	SDT745	M50746E-XXXSP/FP (Note 1) M50746ES/EFS
					PCA4044RG02	RTT745	
	M50745-XXXSP/FP				PCA4045	SDT745	M50745-PGYS
					PCA4045R	RTT745	
	M50747-XXXSP/FP M50747H-XXXSP/FP M50747T-XXXSP M50747E-XXXSP/FP M50747ES/EFS				PCA4047G02 PCA4047XG02★	SDT745	M50747E-XXXSP/FP (Note 1) M50747ES/EFS
					PCA4047RG02★ PCA4047XRG02★	RTT745	
	M50752-XXXSP M50757-XXXSP M50758-XXXSP				PCA4057	SDT745	M50752-PGYS
	M50753-XXXSP/FP M50753T-XXXSP				PCA4053		M50753-PGYS (Note 1)
	M50754-XXXSP/FP/GP M50954-XXXSP/FP/GP M50955-XXXSP/FP/GP				PCA4054G02		M50955-PGYS
					PCA4054RG02	RTT745	
	M50957-XXXSP/FP M50957E-XXXSP M50957ES M50959-XXXSP/FP				PCA4054RG02 (Reconstruct by order)	SDT745	M50957E-XXXSP/FP M50957ES
					PCA4054RG02 (Reconstruct by order)	RTT745	
	M50930-XXXFP M50930T-XXXFP M50931-XXXFP M50932-XXXFP				PCA4093	SDT745	M50931-PGYS (Note 1)
					PCA4093R	RTT745	
	M50940-XXXSP/FP M50941-XXXSP/FP				PCA4094	SDT745	M50941-PGYS
					PCA4094R	RTT745	
	M50943-XXXSP/FP				PCA4033	SDT745	PCA4333G02*
	M50944-XXXSP/FP M50944E-XXXSP/FP				PCA7044★★		M50944E-XXXSP/FP★★ M50944ES★★
	M50950-XXXSP M50951-XXXSP				PCA4095		M50950-PGYS
	M50964-XXXSP/FP M50963-XXXSP/FP M50963E-XXXSP/FP M50963ES/EFS				PCA4064★		M50963E-XXXSP/FP M50963ES/EFS M50964PGYS
					PCA4064R★	RTT745	
	M37410M3-XXXFP M37410M4-XXXFP M37410E6-XXXFP				M37410T-OPT★★	SDT745	M37410E6-XXXFP★★
	M37415M4-XXXFP				M37415T-OPT★★		—
	M37450M2-XXXSP/FP M37450M4-XXXSP/FP M37450M8-XXXSP/FP M37450S1SP/FP M37450S2SP/FP M37450S4SP/FP M37450E4-XXXSP/FP M37450E4SS/FS				M37450T-OPT★ M37450TX-OPT★		M37450PSS/FS M37450E4-XXXSP/FP
					M37450T-RTT★ M37450TX-RTT★	RTT745	M37450E4SS/FS
	M50734SP/FP M50734SP-10				PCA4034G02★	SDT745	—
					PCA4034RG02★	RTT745	

∗ : Evaluation board ★New product ★★Under development
(Note 1) Notes on the operation temperature range when used for extended operating temperature version.
(Note 2) MS-DOS® is a registered trade-mark of Microsoft® Inc.

Program writing adapter for EPROM version

MELPS 740 EPROM version microcomputers	Program writing adapter for EPROM version
M50746E-XXXSP	PCA4700G02
M50746ES	
M50747E-XXXSP	
M50747ES	
M50963E-XXXSP	
M50963ES	
M50746E-XXXFP	PCA4701G02
M50746EFS	
M50747E-XXXFP	
M50747EFS	
M50963E-XXXFP	
M50963EFS	
M50944E-XXXFP	PCA4714★
M50957E-XXXSP	PCA4703
M50957ES	
M37450E4-XXXSP	PCA4710
M37450E4SS	
M37450E4-XXXFP	PCA4711
M37450E4FS	
M37410E6-XXXFP	PCA4705★

★ : New product

FUNCTION CODE

Mitsubisi integrated circuits may be ordered using the following simplified alphanumeric type-codes which define the function of the IC/LSIs and the package style.

1. Mitsubishi Original Producs

Example 1. **M 5 07 40 - 001 SP -2**

M : Mitsubishi integrated prefix

Temperature range
- **5** : Standard industrial/commercial (0 to 70/75℃ or −20 to 85℃)
- **9** : High reliability

Series designation using 1 or 2 alphanumeric chracters.
- **01～09** : CMOS
- **1** : Linear circuit
- **3** : TTL
- **10～19** : Linear circuit
- **32～33** : TTL
- **41～47** : TTL (the others)
- **81** : P-channel aluminum-gate MOS
- **84** : CMOS
- **85** : P-channel silicon-gate MOS
- **86** : P-channel aluminum-gate MOS
- **87** : N-channel silicon-gate MOS
- **88** : P-channel aluminum-gate ED-MOS
- **89** : CMOS
- **9** : DTL
- **S0～S2** : Schottky TTL

Circuit function identification code using 2 digits.
A character next to 2-digit alphanumeric characters, "T", is represented using for automobile/industrial

Mask ROM number.

Package style
- **K** : Glass-sealed ceramic flat package
- **P** : Molded plastic
- **FP** : Molded plastic flat package
- **GP** : Molded plastic flat package
- **SP** : Molded plastic shrink package
- **S** : Metal-sealed ceramic

Electrical characteristic identification code using 1 or 2 digits.

ORDERING INFORMATION

Example 2. **M 3 74 50 E 4 - 001 SP**

M : Mitsubishi integrated prefix

3 : Represent an original single-chip microcomputer

Series designation using 2 alphanumeric chracters

Circuit function identification code using 2 digits

Memory identification code using a digit
- **E** : EPROM
- **M** : Mask ROM
- **N** : Mask ROM+EEPROM
- **P** : Piggyback
- **S** : External ROM

Memory size identification code using a digit

Normally, using hyphen.
When electrical characteristic, or division of quality identification code using alphanumeric character.
- **T** : For automobile/industrial

Mask ROM number

Package style
- **J** : PLCC, or SOJ package
- **K** : Glass-sealed ceramic flat package
- **P** : Molded plastic DIP
- **FP** : Molded plastic flat package
- **FS** : Ceramic flat package
- **GP** : Molded plastic flat package
- **SP** : Molded plastic shrink package
- **S** : Ceramic (layered type) package
- **SS** : Ceramic shrink package

2. PACKAGE CODE

Package style may be specified by using the following simplified alphanumeric code.

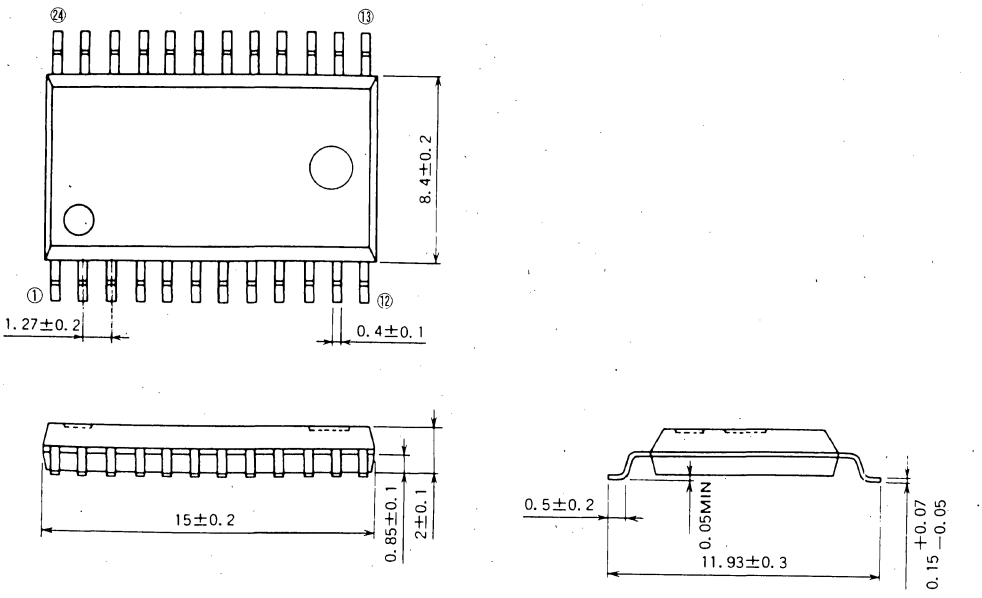
Example : **42 P 4 B**

- **42** — Number of pins
- **P** — Package structure
  - **K** : Glass-sealed ceramic
  - **P** : Molded plastic
  - **S** : Metal-sealed ceramic
- **4** — Package outline
  - **1** : DIP
  - **2** : SOP
  - **4** : DIP
  - **6** : QFP
- **B** — Secondary outline code

Special-purpose secondary codes describing outline are included as necessary. For details, contact your sales representative.

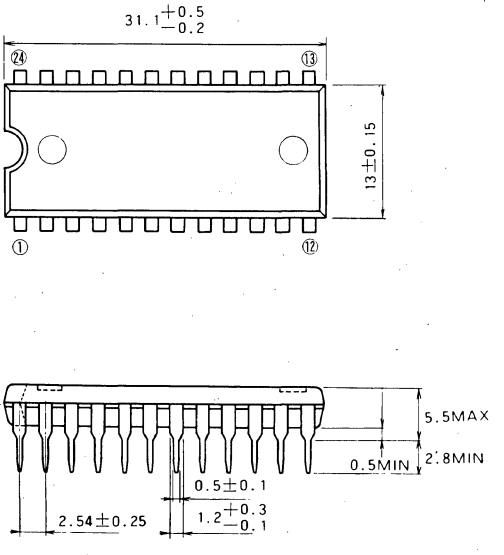
TYPE 24P2W 24-PIN MOLDED PLASTIC SOP

Dimension in mm



TYPE 24P4 24-PIN MOLDED PLASTIC DIP

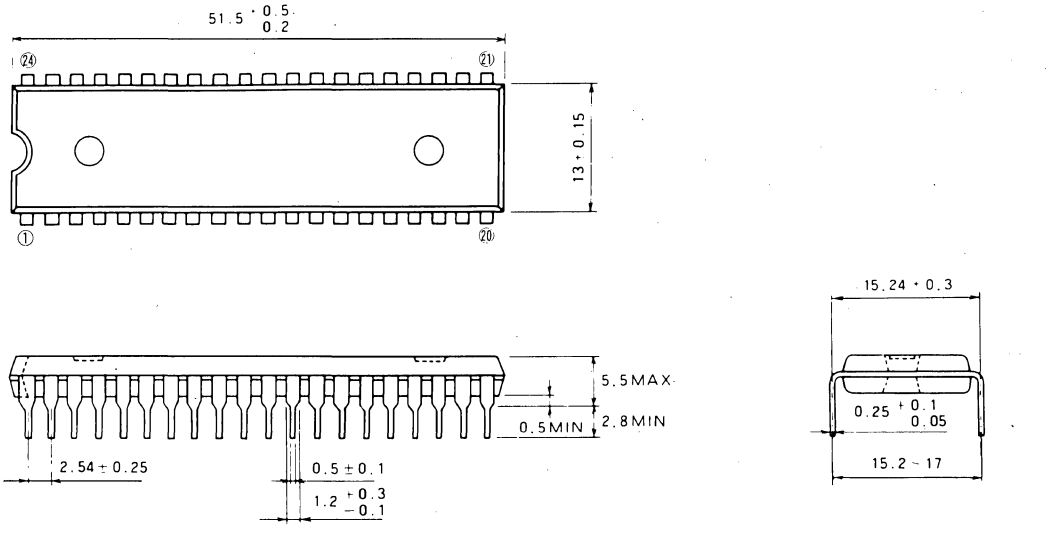
Dimension in mm



MITSUBISHI ELECTRIC

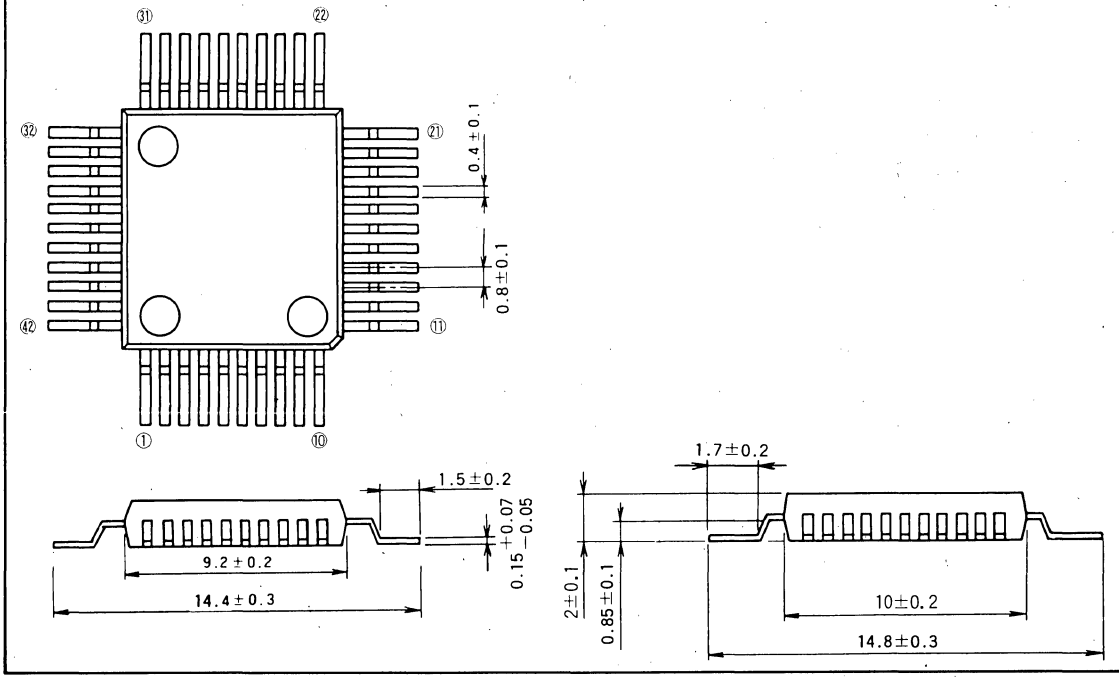
TYPE 40P4 40-PIN MOLDED PLASTIC DIP

Dimension in mm



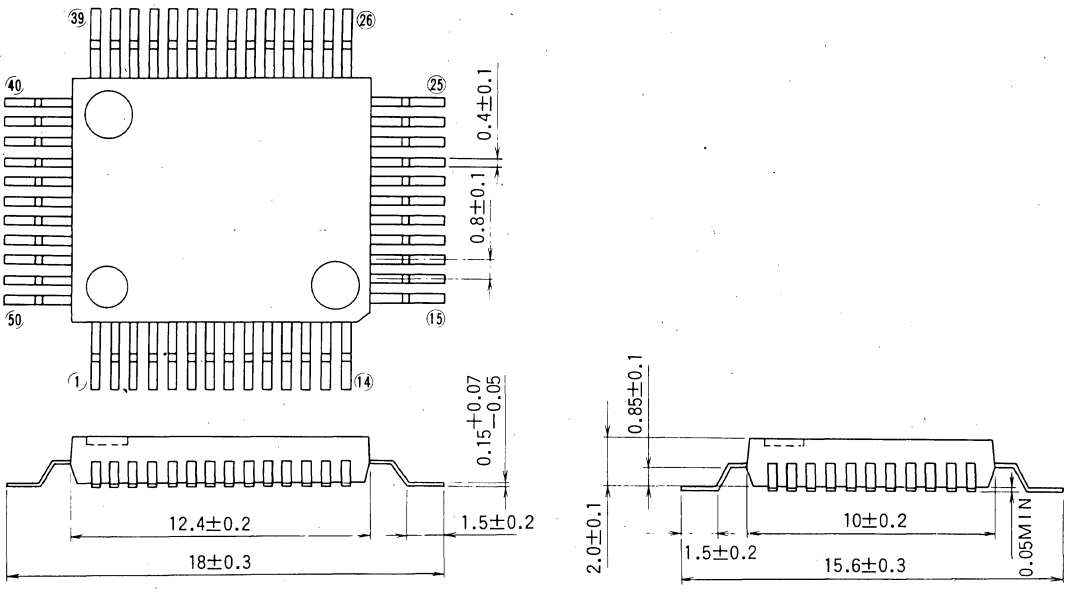
TYPE 42P6 42-PIN MOLDED PLASTIC QFP

Dimension in mm



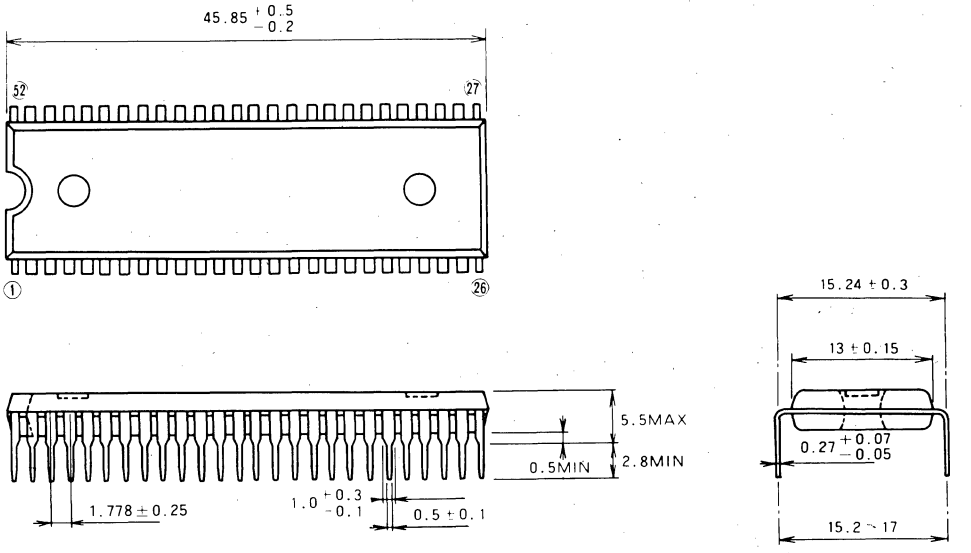
TYPE 50P6 50-PIN MOLDED PLASTIC FLAT

Dimension in mm



TYPE 52P4B 52-PIN MOLDED PLASTIC DIP(LEAD PITCH 1.778mm)

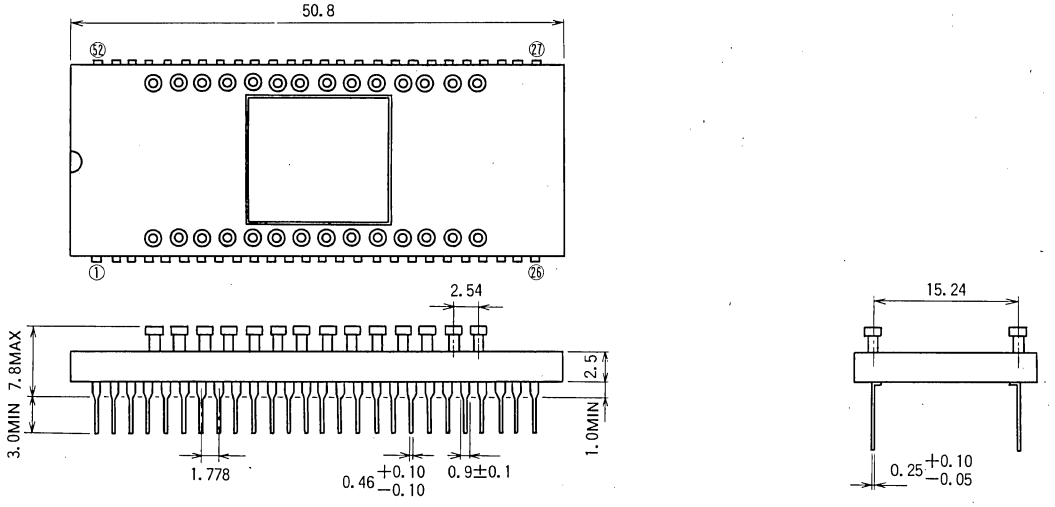
Dimension in mm



MITSUBISHI ELECTRIC

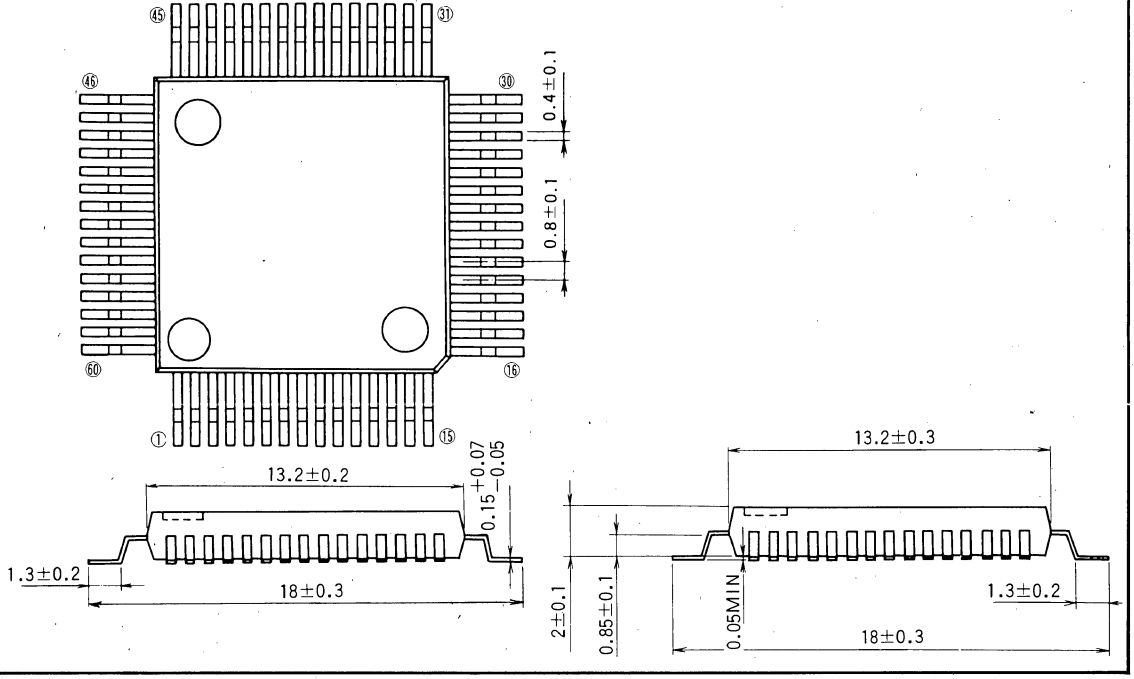
TYPE 52S1M 52-PIN PIGGYBACK DIP

Dimension in mm



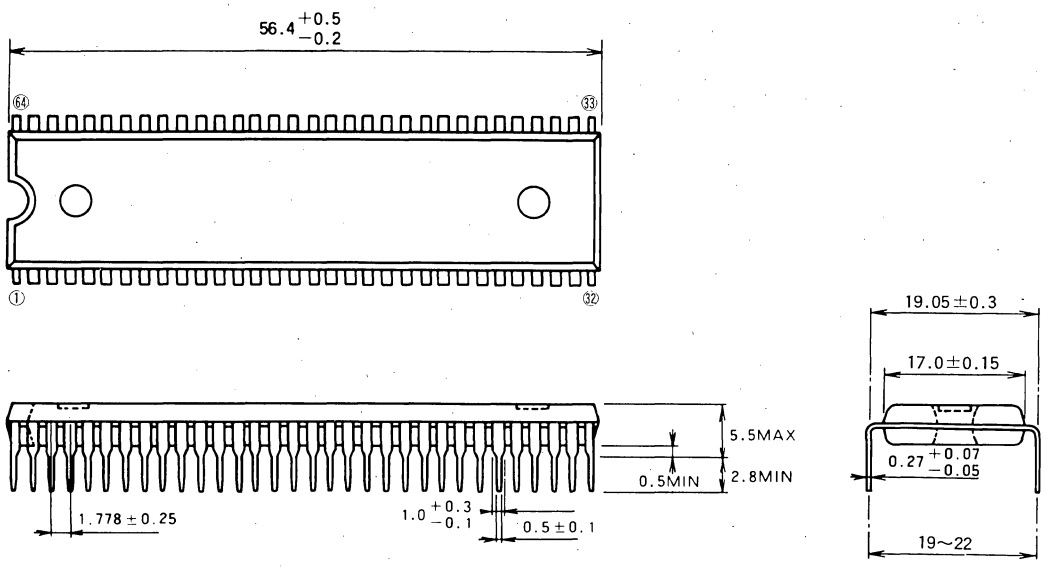
TYPE 60P6 60-PIN MOLDED PLASTIC QFP

Dimension in mm



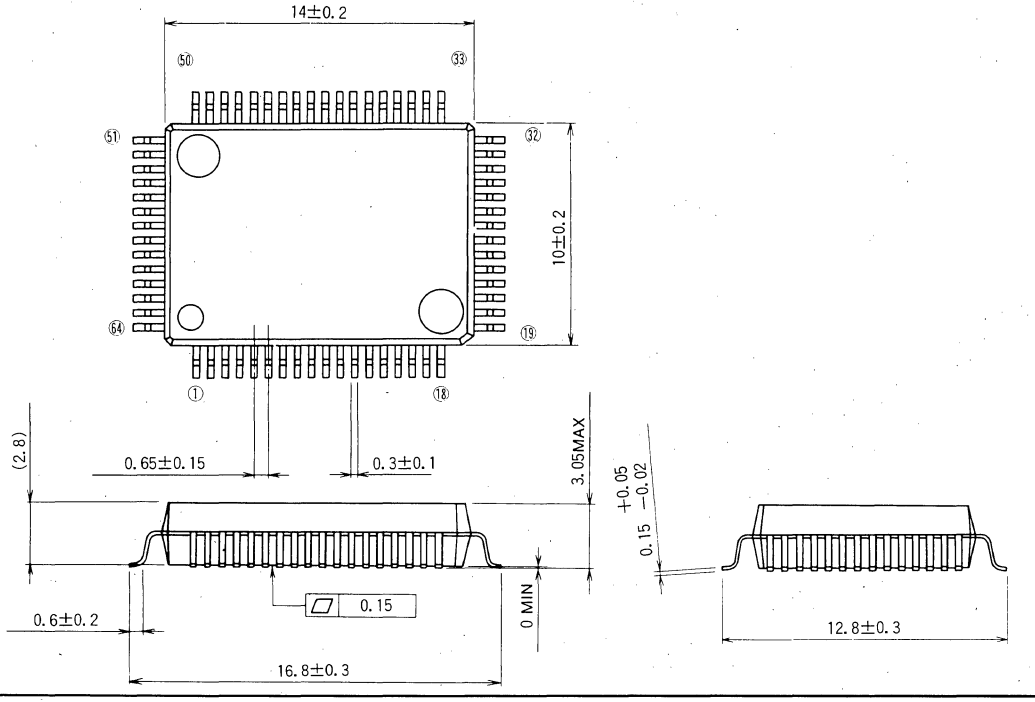
TYPE 64P4B 64-PIN MOLDED PLASTIC DIP(LEAD PITCH 1.778mm)

Dimension in mm



TYPE 64P6S 64-PIN MOLDED PLASTIC QFP

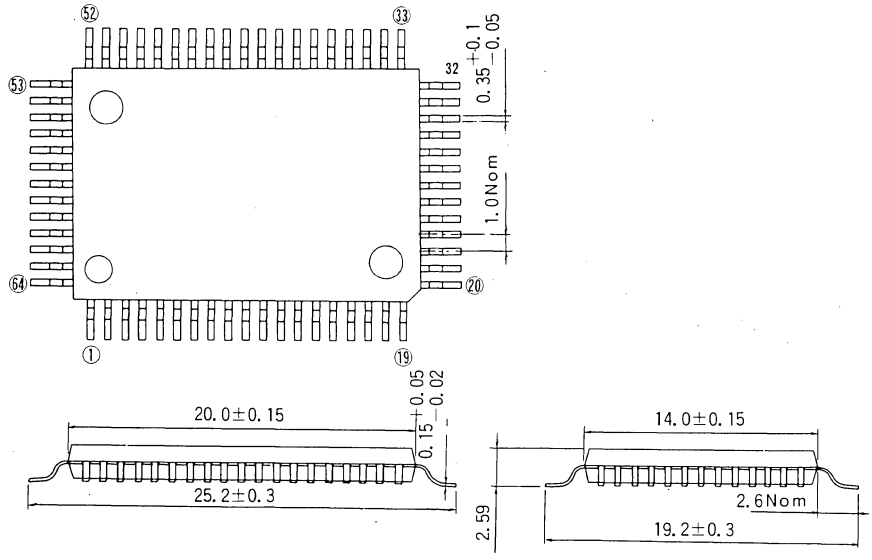
Dimension in mm



MITSUBISHI ELECTRIC

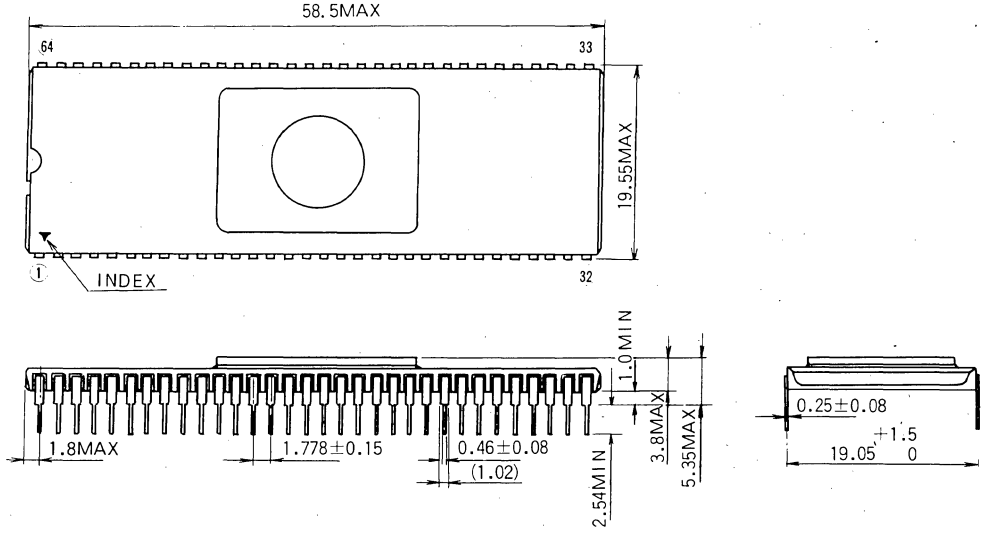
TYPE 64P6W 64-PIN MOLDED PLASTIC QFP

Dimension in mm



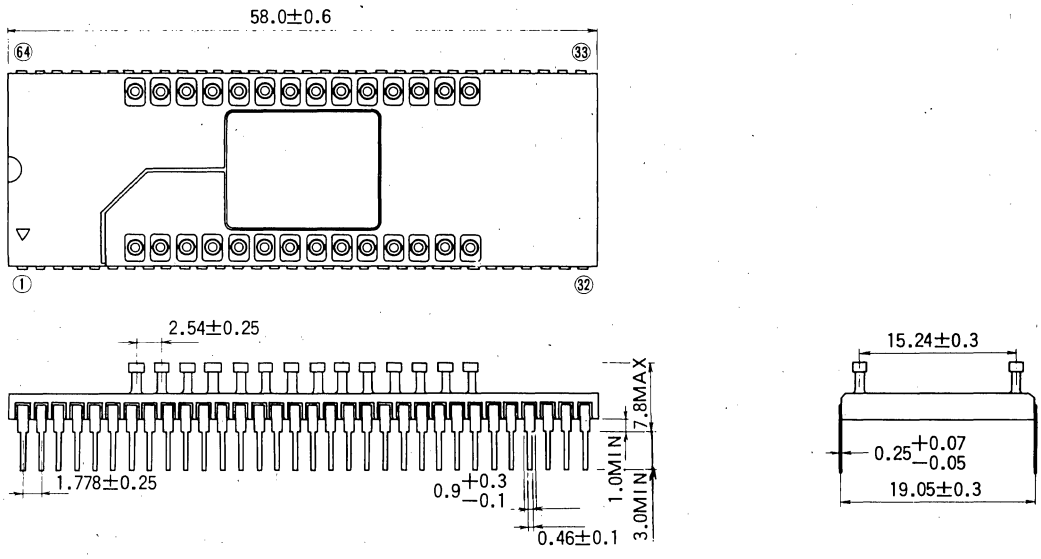
TYPE 64S1B 64-PIN CERAMIC DIP

Dimension in mm



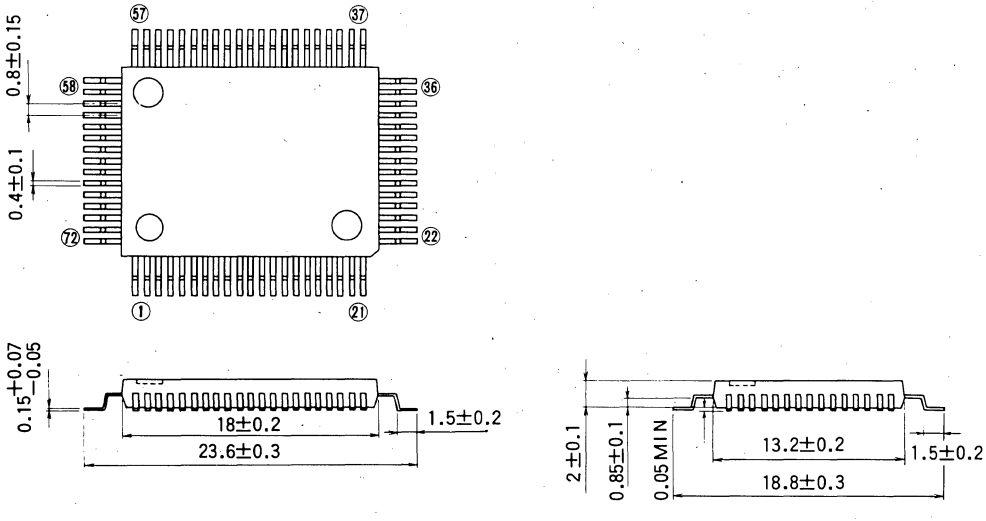
TYPE 64S1M 64-PIN PIGGYBACK DIP

Dimension in mm



TYPE 72P6 72-PIN MOLDED PLASTIC QFP

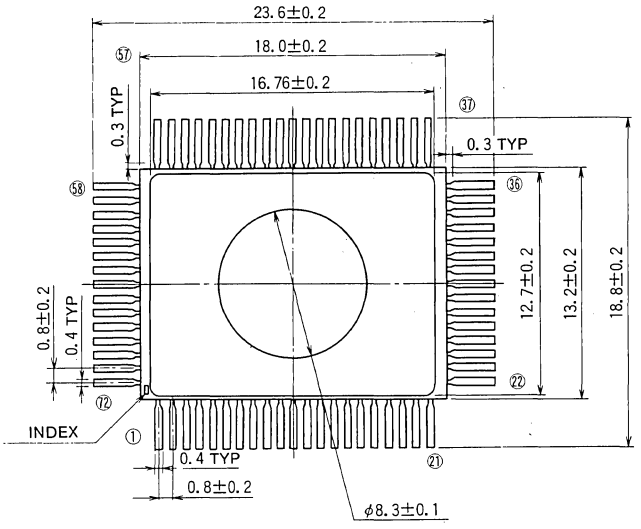
Dimension in mm

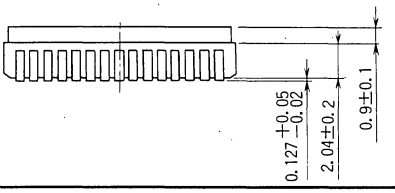


MITSUBISHI ELECTRIC

TYPE 72S6 72-PIN MOLDED CERAMIC QFP

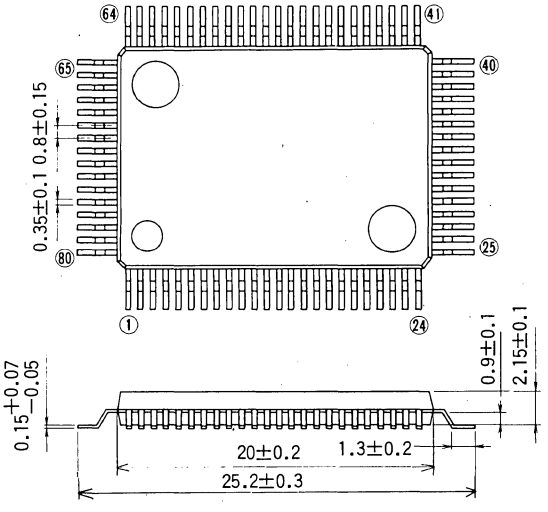
Dimension in mm

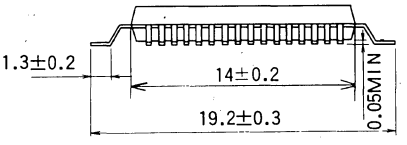




TYPE 80P6 80-PIN MOLDED PLASTIC QFP

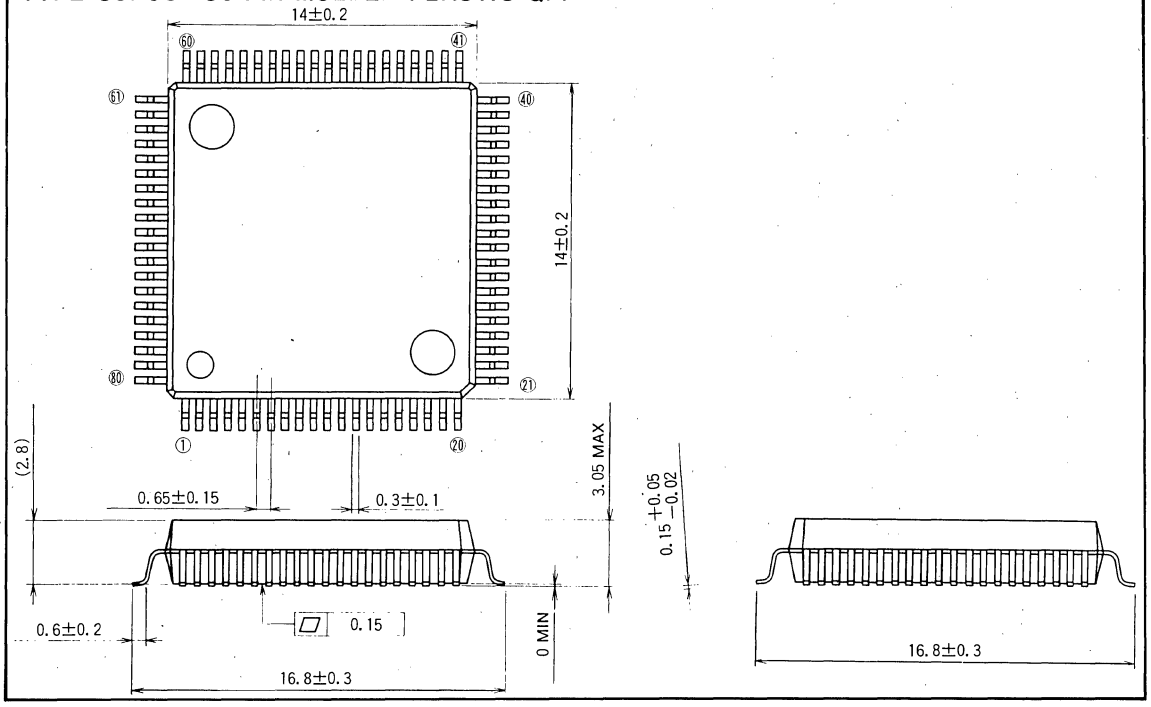
Dimension in mm





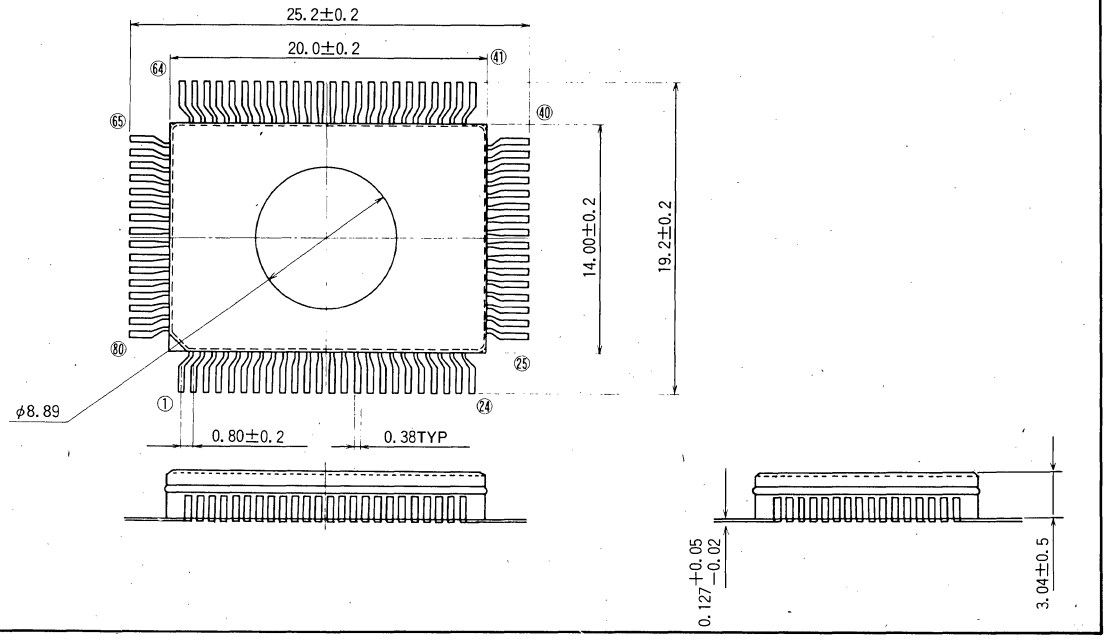
TYPE 80P6S 80-PIN MOLDED PLASTIC QFP

Dimension in mm



TYPE 80S6 80-PIN MOLDED CERAMIC QFP

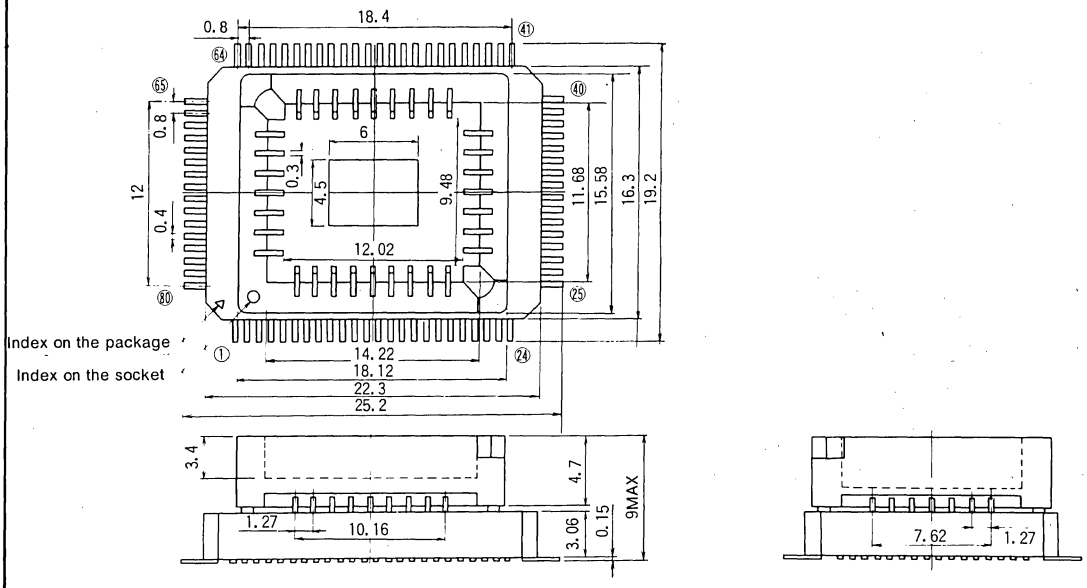
Dimension in mm



MITSUBISHI ELECTRIC

TYPE 80S6M 80-PIN PIGGYBACK QFP

Dimension in mm



LETTER SYMBOLS FOR THE DYNAMIC PARAMETERS

1. INTRODUCTION

A system of letter symbols to be used to represent the dynamic parameters of intergrated circuit memories and other sequential circuits especially for single-chip microcomputers, microprocessors and LSIs for peripheral circuits has been discussed internationally in the TC47 of the International Electrotechnical Committee (IEC). Finally the IEC has decided on the meeting of TC47 in February 1980 that this system of letter symbols will be a Central Office document and circulated to all countries to vote which means this system of letter symbols will be a international standard.

The system is applied in this LSI data book for the new products only. Future editions of this data book will be applied this system. The IEC document which describes "Letter symbols for dynamic parameters of sequential integrated circuits, including memories" is introduced below. In this data book, the dynamic parameters in the IEC document are applied to timing requirements and switching characteristics.

2. LETTER SYMBOLS

The system of letter symbols outlined in this document enables symbols to be generated for the dynamic parameters of complex sequential circuits, including memories, and also allows these symbols to be abbreviated to simple mnemonic symbols when no ambiguity is likely to arise.

2.1. General Form

The dynamic parameters are represented by the general symbol of the form:-

$t_{A(BC-DC)F}$ ..... (1)

where :

Subscript A indicates the type of dynamic parameter being represented, for example; cycle time, setup time, enable time, etc.

Subscript B indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur first, that is, at the beginning of the time interval. If this event actually occurs last, that is, at the end of the time interval, the value of the time interval is negative.

Subscript C indicates the direction of the transition and/or the final state or level of the signal represented by B. When two letters are used, the initial state or level is also indicated.

Subscript D indicates the name of the signal or terminal for which a change of state or level (or establishment of a state or level) constitutes a signal event assumed to occur last, that is, at the end of the time interval. If this event actually occurs first, that is, at the beginning of the time interval, the value of the time interval is negative.

Subscript E indicates the direction of the transition and/or the final state or level of the signal represented by D. When two letters are used, the initial state or level is also indicated.

Subscript F indicates additional information such as mode of operation, test conditions, etc.

Note 1: Subscripts A to F may each consists of one or more letters.
2: Subscripts D and E are not used for transition times.
3: The "–" in the symbol (1) above is used to indicate "to", hence the symbol represents the time interval from signal event B occuring to signal event D occuring, and it is important to note that this convention is used for all dynamic parameters including hold times. Where no misunderstanding can occur the hyphen may be omitted.

2.2. Abbreviated Form

The general symbol given above may be abbreviated when no misunderstanding is likely to arise. For example to :

$t_{A(B-D)}$

or $t_{A(B)}$

or $t_{A(D)}$ – often used for hold times

or t_{AF} – no brackets are used in this case

or t_{A}

or t_{BC-DE} – often used for unclassified time intervals

2.3. Allocation of Subscripts

In allocating letter symbols for the subscripts, the most commonly used subscripts are given single letters where practicable and those less commonly used are designated by up to three letters. As far as possible, some form of mnemonic representation is used. Longer letter symbols may be used for specialised signals or terminals if this aids understanding.

3. SUBSCRIPT A (For Type of Dynamic Parameter

The subscript A represents the type of dynamic parameter to be designated by the symbol and, for memories, the parameters may be divided into two classes :

a) those that are timing requirements for the memory and

b) those that are characteristics of the memory.
The letter symbols so far proposed for memory circuits are listed in sub-clauses 3.1 and 3.2 below.
All subscripts A should be in lower-case.

3.1. Timing Requirements

The letter symbols for the timing requirements of semiconductor memories are as follows :

Term	Subscript
Cycle time	c
Time interval between two signal events	d
Fall time	f
Hold time	h
Precharging time	pc
Rise time	r
Recovery time	rec
Refresh time interval	rf
Setup time	su
Transition time	t
Pulse duration (width)	w

3.2. Characteristics

The letter symbols for the dynamic characteristics of semiconductor memories are as follows :

Characteristic	Subscript
Access time	a
Disable time	dis
Enable time	en
Propagation time	P
Recovery time	rec
Transition time	T
Valid time	v

Note: Recovery time for use as a characteristic is limited to sense recovery time.

4. SUBSCRIPTS B AND D (For Signal Name or Terminal Name)

The letter symbols for the signal name or the name of the terminal are as given below.
All subscripts B and D should be in upper-case.

Signal or terminal	Subscript
Address	A
Clock	C
Column address	CA
Column address strobe	CAS
Data input	D
Data input/output	DQ
Chip enable	E
Erasure	ER
Output enable	G
Program	PR
Data output	Q
Read	R
Row address	RA
Row address strobe	RAS
Refresh	RF
Read/Write	RW
Chip select	S
Write (write enable)	W

Note 1: In the letter symbols for time intervals, bars over the subscripts, for example CAS, should not be used.
2: It should be noted, when further letter symbols are chosen, that the subscript should not end with H, K, V, X, or Z. (See clause 5)
3: If the same terminal, or signal, can be used for two functions (for example Data input/output, Read/Write) the waveform should be labelled with the dual function, if appropriate, but the symbols for the dynamic parameters should include only that part of the subscript relevant to the parameter.

5. SUBSCRIPTS C AND E (For Transition of Signal)

The following symbols are used to represent the level or state of a signal :

Transition of signal	Subscript
High logic level	H
Low logic level	L
Valid steady-state level (either low or high)	V
Unknown, changing, or 'don't care' level	X
High-impedance state of three-state output	Z

The direction of transition is expressed by two letters, the direction being from the state represented by the first letter to that represented by the second letter, with the letters being as given above.
When no misunderstanding can occur, the first letter may be omitted to give an abbreviated symbol for subscripts C and E as indicated below.
All subscripts C and E should be in upper-case.

Examples	Subscript	
	Full	Abbreviated
Transition from high level to low level	HL	L
Transition from low level to high level	LH	H
Transition from unknown or changing state to valid state	XV	V
Transition from valid state to unknown or changing state	VX	X
Transition from high-impedance state to valid state	ZV	V

Note: Since subscripts C and E may be abbreviated, and since subscripts B and D may contain an indeterminate number of letters, it is necessary to put the restriction on the subscripts B and D that they should not end with H, L, V, X, or Z, so as to avoid possible confusion.

6. SUBSCRIPT F (For Additional Information)

If necessary, subscript F is used to represent any additional qualification of the parameter such as mode of operation, test conditions, etc. The letter symbols for subscript F are given below.
Subscript F should be in upper-case.

Modes of operation	Subscript
Power-down	PD
Page-mode read	PGR
Page-mode write	PGW
Read	R
Refresh	RF
Read-modify-write	RMW
Read-write	RW
Write	W

FOR DIGITAL INTEGRATED CIRCUITS

New symbol	Former symbol	Parameter–definition
C_i		Input capacitance
C_o		Output capacitance
$C_{i/o}$		Input/output terminal capacitance
$C_{I(\phi)}$		Input capacitance of clock input
f		Frequency
$f_{(\phi)}$		Clock frequency
I		Current–the current into an integrated circuit terminal is defined as a positive value and the current out of a terminal is defined as a negative value
I_{BB}		Supply current from V_{BB}
$I_{BB(AV)}$		Average supply current from V_{BB}
I_{CC}		Supply current from Vcc
$I_{CC(AV)}$		Avarage supply current from Vcc
$I_{CC(PD)}$		Power-down supply current from Vcc
I_{DD}		Supply current from V_{DD}
$I_{DD(AV)}$		Average supply current from V_{DD}
I_{GG}		Supply current from V_{GG}
$I_{GG(AV)}$		Average supply current from V_{GG}
I_I		Input current
I_{IH}		High-level input current–the value of the input current when V_{OH} is applied to the input considered
I_{IL}		Low-level input current–the value of the input current when V_{OL} is applied to the input considered
I_{LOAD}		Built-in resistor current
I_{PEAK}		Peak current
I_{OH}		High-level output current–the value of the output current when V_{OH} is applied to the output considered
I_{OL}		Low-level output current–the value of the output current when V_{OL} is applied to the output considered
I_{OZ}		Off-state (high-impedance state) output current–the current into an output having a three-state capability with input condition so applied that it will establish according to the product specification, the off (high-impedance) state at the output
I_{OZH}		Off-state (high-impedance state) output current, with high-level voltage applied to the output
I_{OZL}		Off-state (high-impedance state) output current, with low-level voltage applied to the output
I_{OS}		Short-circuit output current
I_{SS}		Supply current from V_{SS}
Pd		Power dissipation
N_{EW}		Number of erase/write cycles
N_{RA}		Number of read access unrefreshed
R_i		Input resistance
R_L		External load resistance
R_{OFF}		Off-state output resistance
R_{ON}		On-state output resistance
t_a		Access time–the time interval between the application of a specified input pulse during a read cycle and the availability of valid data signal at an output
$t_{a(A)}$	$t_{a(AD)}$	Address access time–the time interval between the application of an address input pulse and the availability of valid data signals at an output
$t_{a(CAS)}$		Column address strobe access time
$t_{a(E)}$	$t_{a(CE)}$	Chip enable access time
$t_{a(G)}$	$t_{a(OE)}$	Output enable access time
$t_{a(PR)}$		Data access time after program
$t_{a(RAS)}$		Row address strobe access time
$t_{a(S)}$	$t_{a(CS)}$	Chip select access time
t_C		Cycle time
t_{CR}	$t_{C(RD)}$	Read cycle time–the time interval between the start of a read cylce and the start of the next cycle
t_{CRF}	$t_{C(REF)}$	Refresh cycle time–the time interval between successive signals that are intended to restore the level in a dynamic memory cell to its original level
t_{CPG}	$t_{C(PG)}$	Page-mode cycle time

New symbol	Former symbol	Parameter—definition
t_{CRMW}	$t_{C(RMR)}$	Read-modify-write cycle time—the time interval between the start of a cycle in which the memory is read and new data is entered, and the start of the next cycle
t_{CW}	$t_{C(WR)}$	Write cycle time—the time interval between the start of a write cycle and the start of the next cycle
t_d		Delay time—the time between the specified reference points on two pulses
$t_{d(\phi)}$		Delay time between clock pulses—e.g., symbology, delay time, clock 1 to clock 2 or clock 2 to clock 1
$t_{d(CAS\text{-}RAS)}$		Delay time, column address strobe to row address strobe
$t_{d(CAS\text{-}W)}$	$t_{d(CAS\ WR)}$	Delay time, column address strobe to write
$t_{d(RAS\text{-}CAS)}$		Delay time, row address strobe to column address strobe
$t_{d(RAS\text{-}W)}$	$t_{d(RAS\text{-}WR)}$	Delay time, row address strobe to write
$t_{dis(R\text{-}Q)}$	$t_{dis(R\text{-}DA)}$	Output disable time after read
$t_{dis(S)}$	$t_{PXZ(CS)}$	Output disable time after chip select
$t_{dis(W)}$	$t_{PXZ(WR)}$	Output disable time after write
t_{DHL}		High-level to low-level delay time } the time interval between specified reference points on the input and on the output pulses, when the output is going to the low (high) level and when the device is driven with a specified loading networks.
t_{DLH}		Low-level to high-level delay time }
$t_{en(A\text{-}Q)}$	$t_{PZV(A\text{-}DQ)}$	Output enable time after address
$t_{en(R\text{-}Q)}$	$t_{PZV(R\text{-}DQ)}$	Output enable time after read
$t_{en(S\text{-}Q)}$	$t_{PZX(CS\text{-}DQ)}$	Output enable time after chip select
t_f		Fall time
t_h		Hold time—the interval of time during which a signal at a specified input terminal appears after an active transition occurs at another specified input terminal
$t_{h(A)}$	$t_{h(AD)}$	Address hold time
$t_{h(A\text{-}E)}$	$t_{h(AD\text{-}CE)}$	Chip enable hold time after address
$t_{h(A\text{-}PR)}$	$t_{h(AD\text{-}PRO)}$	Program hold time after address
$t_{h(CAS\text{-}CA)}$		Column address hold time after column address strobe
$t_{h(CAS\text{-}D)}$	$t_{h(CAS\text{-}DA)}$	Data-in hold time after column address strobe
$t_{h(CAS\text{-}Q)}$	$t_{h(CAS\text{-}OUT)}$	Data-out hold time after column address strobe
$t_{h(CAS\text{-}RAS)}$		Row address strobe hold time after column address strobe
$t_{h(CAS\text{-}W)}$	$t_{h(CAS\text{-}WR)}$	Write hold time after column address strobe
$t_{h(D)}$	$t_{h(DA)}$	Data-in hold time
$t_{h(D\text{-}PR)}$	$t_{h(DA\text{-}PRO)}$	Program hold time after data-in
$t_{h(E)}$	$t_{h(CE)}$	Chip enable hold time
$t_{h(E\text{-}D)}$	$t_{h(CE\text{-}DA)}$	Data-in hold time after chip enable
$t_{h(E\text{-}G)}$	$t_{h(CE\text{-}OE)}$	Output enable hold time after chip enable
$t_{h(R)}$	$t_{h(RD)}$	Read hold time
$t_{h(RAS\text{-}CA)}$		Column address hold time after row address strobe
$t_{h(RAS\text{-}CAS)}$		Column address strobe hold time after row address strobe
$t_{h(RAS\text{-}D)}$	$t_{h(RAS\text{-}DA)}$	Data-in hold time after row address strobe
$t_{h(RAS\text{-}W)}$	$t_{h(RAS\text{-}WR)}$	Write hold time after row address strobe
$t_{h(S)}$	$t_{h(CS)}$	Chip select hold time
$t_{h(W)}$	$t_{h(WR)}$	Write hold time
$t_{h(W\text{-}CAS)}$	$t_{h(WR\text{-}CAS)}$	Column address strobe hold time after write
$t_{h(W\text{-}D)}$	$t_{h(WR\text{-}DA)}$	Data-in hold time after write
$t_{h(W\text{-}RAS)}$	$t_{h(WR\text{-}RAS)}$	Row address hold time after write
t_{PHL}		High-level to low-level propagation time } the time interval between specified reference points on the input and on the output pulses when the output is going to the low (high) level and when the device is driven and loaded by typical devices of stated type
t_{PLH}		Low-level to high-level propagation time }
t_r		Rise time
$t_{rec(W)}$	t_{wr}	Write recovery time—the time interval between the termination of a write pulse and the initiation of a new cycle
$t_{rec(PD)}$	$t_{R(PD)}$	Power-down recovery time
t_{su}		Setup time—the time interval between the application of a signal which is maintained at a speciifed input terminal and a consecutive active tarnsition at another specified input terminal
$t_{su(A)}$	$t_{su(AD)}$	Address setup time

New symbol	Former symbol	Parameter—definition
$t_{su(A-E)}$	$t_{su(AD-CE)}$	Chip enable setup time before address
$t_{su(A-W)}$	$t_{su(AD-WR)}$	Write setup time before address
$t_{su(CA-RAS)}$		Row address strobe setup time before column address
$t_{su(D)}$	$t_{su(DA)}$	Data-in setup time
$t_{su(D-E)}$	$t_{su(DA-CE)}$	Chip enable setup time before data-in
$t_{su(D-W)}$	$t_{su(DA-WR)}$	Write setup time before data-in
$t_{su(E)}$	$t_{su(CE)}$	Chip enable setup time
$t_{su(E-P)}$	$t_{su(CE-P)}$	Precharge setup time before chip enable
$t_{su(G-E)}$	$t_{su(OE-CE)}$	Chip enable setup time before output enable
$t_{su(P-E)}$	$t_{su(P-CE)}$	Chip enable setup time before precharge
$t_{su(PD)}$		Power-down setup time
$t_{su(R)}$	$t_{su(RD)}$	Read setup time
$t_{su(R-CAS)}$	$t_{su(RA-CAS)}$	Column address strobe setup time before read
$t_{su(RA-CAS)}$		Column address strobe setup time before row address
$t_{su(S)}$	$t_{su(CS)}$	Chip select setup time
$t_{su(S-W)}$	$t_{su(CS-WR)}$	Write setup time before chip select
$t_{su(W)}$	$t_{su(WR)}$	Write setup time
t_{THL}		High-level to low-level transition time } the time interval between specified reference points on the edge of the output pulse when the output is going to the low (high) level and when a specified input signal is applied through a specified network and the output is loaded by another specified network
t_{TLH}		Low-level- to high-level transition time }
$t_{v(A)}$	$t_{dv(AD)}$	Data valid time after address
$t_{v(E)}$	$t_{dv(CE)}$	Data valid time after chip enable
$t_{v(E)PR}$	$t_{v(CE)PR}$	Data valid time after chip enable in program mode
$t_{v(G)}$	$t_{v(OE)}$	Data valid time after output enable
$t_{v(PR)}$		Data valid time after program
$t_{v(S)}$	$t_{v(CS)}$	Data valid time after chip select
t_w		Pulse width (pulse duration) the time interval between specified reference points on the leading and training edges of the waveforms
$t_{w(E)}$	$t_{w(CE)}$	Chip enable pulse width
$t_{w(EH)}$	$t_{w(CEH)}$	Chip enable high pulse width
$t_{w(EL)}$	$t_{w(EL)}$	Chip enable low pulse width
$t_{w(PR)}$		Program pulse width
$t_{w(R)}$	$t_{w(RD)}$	Read pulse width
$t_{w(S)}$	$t_{w(CS)}$	Chip select pulse width
$t_{w(W)}$	$t_{w(WR)}$	Wrtie pulse width
$t_{w(\phi)}$		Clock pulse width
Ta		Ambient temperature
Topr		Operating temperature
Tstg		Storage temperature
V_{BB}		V_{BB} supply voltage
V_{CC}		V_{CC} supply voltage
V_{DD}		V_{DD} supply voltage
V_{GG}		V_{GG} supply voltage
V_I		Input voltage
V_{IH}		High-level input voltage—the value of the permitted high-state voltage at the input
V_{IL}		Low-level input voltage—the value of the permitted low-state voltage at the input
V_O		Output voltage
V_{OH}		High-level output voltage—the value of the guaranteed high-state voltage range at the output
V_{OL}		Low-level output voltage—the value of the guaranteed low-state voltage range at the output
V_{SS}		V_{SS} supply voltage

Note 1. These letter symbols are based on the IEC publication 148 except a part of them.

QUALITY ASSURANCE AND RELIABILITY TESTING

1 INTRODUCTION

IC & LSI have made rapid technical progress in electrical performances of high integration, high speed, and sophisticated functionality. And now they have got boundless wider applications in electronic systems and electrical appliances.

To meet the above trend of expanding utilization of IC & LSI, Mitsubishi considers that it is extremely important to supply stable quality and high reliable products to customers.

Mitsubishi Electric places great emphasis on quality as a basic policy "Quality First", and has striven always to improve quality and reliability.

Mitsubishi has already developed the Quality Assurance System covering design, manufacturing, inventory and delivery for IC & LSI, and has supplied highly reliable products to customers for many years. The following articles describe the Quality Assurance System and examples of reliability control for Mitsubishi Single-chip 8-bit Microcomputer.

2. QUALITY ASSURANCE SYSTEM

The Quality Assurance System places emphasis on built-in reliability in designing and built-in quality in manufacturing. The System from development to delivery is summarized in Fig. 1.

2.1 Quality Assurance in Designing

The following steps are applied in the designing stage for a new product.

(1) Setting of perfomance, quality and reliability target for new product.
(2) Discussion of performance and quality for circuit design, device structure, process, material and package.
(3) Verification of design by CAD system to meet standardized design rule.
(4) Functional evaluation for bread-board device to confirm electrical performance.
(5) Reliability evaluation for TEG (Test Element Group) chip to detect basic failure mode and investigate failure mechanism.
(6) Reliability test (In-house qualification) for new product to confirm quality and reliability target.
(7) Decision of pre-production from the standpoint of performance, reliability, production flow/conditions, production capability, delivery and etc.

2.2 Quality Assurance in Manufacturing

Quality assurance in manufacturing is performed as follows.

(1) Environment control such as temperature, humidity and dust as well as deionized water and utility gases.
(2) Maintenance and calibration control for automatized manufacturing equipments, automatic testing equipments, and measuring instruments.
(3) Material control such as silicon wafer, lead frame, packaging material, mask and chemicals.
(4) In-process inspections in wafer-fabrication, assembly and testing.
(5) 100% final inspection of electrical characteristics, visual inspection and burn-in, if necessary.
(6) Quality assurance test
-Electrical characteristics and visual inspection, lot by lot sampling
-Environment and endurance test, periodical sampling.
(7) Inventory and shipping control, such as storage environment, date code identification, handling and ESD (Electro Static Discharge) preventive procedure.

2.3 Reliability Test

To verify the reliability of a product as described in the Mitsubishi Quality Assurance System, reliability tests are performed at three different stages in new product development, pre-production and mass-production.

At the development of a new product the reliability test plan is fixed corresponding to the quality and reliability target of each product, respectively. The test plan includes in-house qualification test and TEG evaluation, if necessary. TEG chips are designed and prepared for new device structure, new process and new material.

After the proto-type product has passed the in-house qualification test, the product advances to the pre-production. In the pre-production stage, the specific reliability tests are programmed and performed again to verify the quality of pre-production product.

In the mass production, the reliability tests are performed periodically to confirm the quality of the mass production product according to the quality assurance test program.

Table 1 shows an example of reliability test program for plastic encapsulated IC & LSI.

Table 1 TYPICAL RELIABILITY TEST PROGRAM FOR PLASTIC ENCAPSULATED IC & LSI

Group	Test	Test condition
1	Solderability	230℃, 5sec. Rosin flux
2	Soldering heat	260℃, 10sec.
	Thermal shock	−55℃, 125℃, 15cycles
	Temperature cycling	−65℃, 150℃, 100cycles
3	Lead fatigue	250gr, 90°, 2arcs
4	Shock	1500G, 0.5msec.
	Vibration	20G, 100~2000Hz X, Y, Z direction 4min./cycle, 4cycles/direction
	Constant acceleration	20000G, Y direction, 1min.
5	Operation life	T_a=125℃, Vccmax 1000hours
6	High temperature storage life	T_a=150℃, 1000hours
7	High temperature and high humidity	85℃, 85%, 1000hours
	Pressure cooker	121℃, 100%, 100hours

QUALITY ASSURANCE AND RELIABILITY TESTING

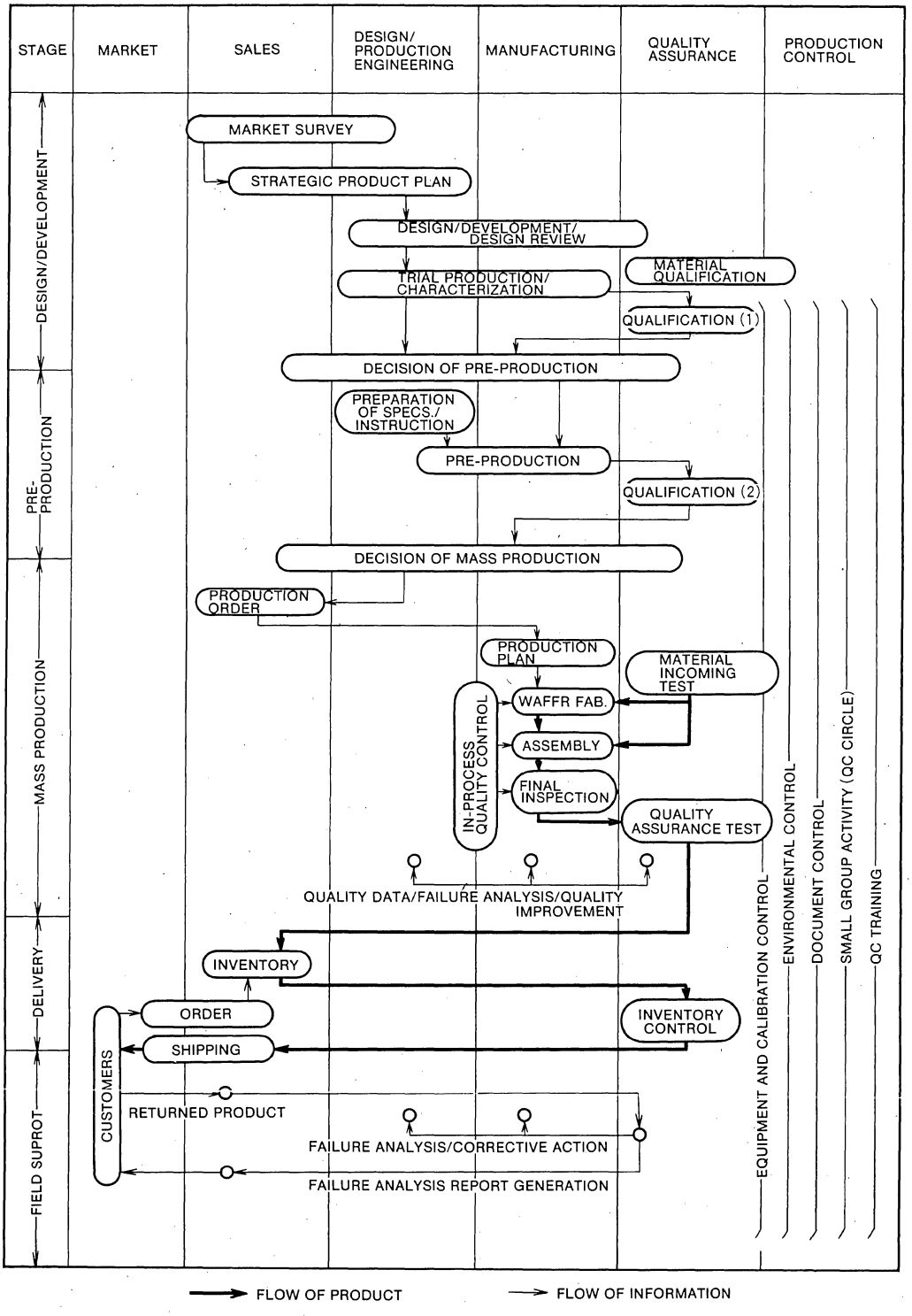


Fig.1 FLOW CHART OF QUALITY ASSURANCE SYSTEM

2.4 Returned Product Control

When failure analysis is requested by a customer, the failed devices are returned to Mitsubishi Electric via the sales office of Mitsubishi using the form of "Analysis Request of Returned Product"

Mitsubishi provides various failure analysis equipments to analyze the returned product. A failure analysis report is generated to the customer upon completion of the analysis. The failure analysis result enforces taking corrective action for the design, fabrication, assembly or testing of the product to improve reliability and realize lower failure rate.

Fig. 2 shows the procedure of returned product control from customer.

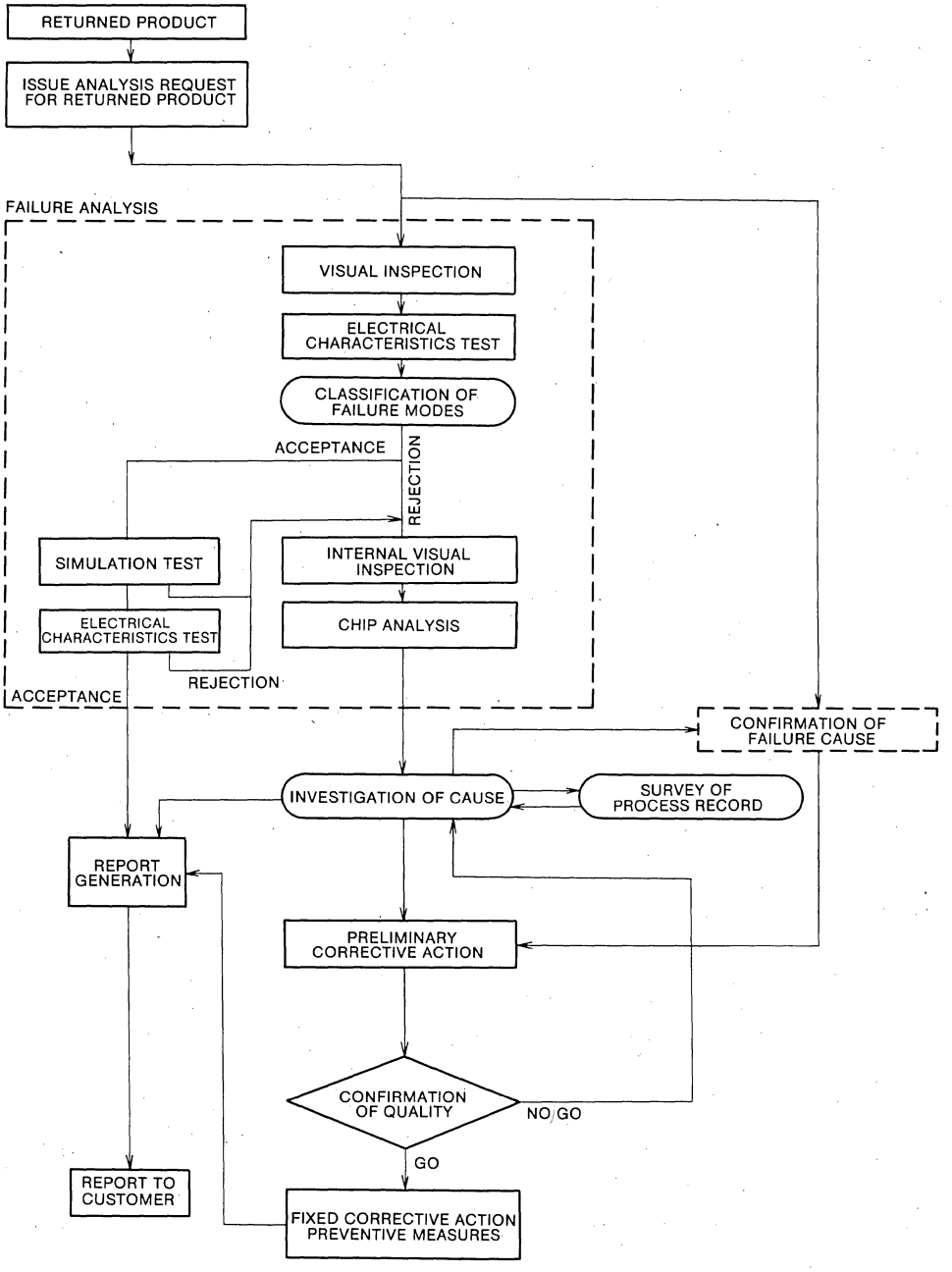


Fig.2 PROCEDURE OF RETURNED PRODUCT CONTROL

3 RELIABILITY TEST RESULTS

The reliability test results for Mitsubishi Single-chip 8-bit Microcomputers are shown in Table 2, Table 3 and Table 4. Table 2 shows the result of endurance tests of high temparature operation life and high temperature storage life test for representative types of Single-chip 8-bit Microcomputers, MELPS 740, MELPS 8-48, MELPS 8-41, and Peripheral LSIs.

From Table 2, the combined failure rate of Mitsubishi Single-chip 8-bit Microcomputers is calculated 0.16%/1000hours at 125℃ ambient temperature operation.

Table 2 ENDURANCE TEST RESULTS

Test	Series	Type Number	Test Condition		Number of	Device Hours	Number of
			T_a(℃)	V_{CC}(volt)	Samples	(Hours)	Failures
High Temperature Operation Life	MELPS 740	M50740A-XXXSP	125	7	1084	1,816,000	4
		M50743-XXXSP		7	36	36,000	0
		M50744-XXXSP		7	132	180,000	0
		M50745-XXXFP		7	48	96,000	0
		M50747-XXXSP		7	480	732,000	2
		M50753-XXXFP		7	48	48,000	0
		M50754-XXXSP		7	120	186,000	0
		M50757-XXXSP		7	48	48,000	0
		M50931-XXXFP		7	48	72,000	0
		M50943-XXXFP		7	36	36,000	0
		M50950-XXXSP		7	36	72,000	0
		M50734SP		7	84	132,000	0
		M37450M2-XXXSP		7	38	38,000	0
		M37450S4SP		7	38	76,000	0
		M50747ES	125	7	38	38,000	0
		M50747E-XXXSP		7	140	280,000	1
	MELPS 8-48	M5L8049-XXXP	125	5.5	66	66,000	0
		M5L8050H-XXXP		5.5	72	72,000	0
		M5M80C49-XXXP		5.5	170	170,000	0
	MELPS 8-41	M5L8041A-XXXP	125	5.5	44	44,000	0
		M5L8042-XXXP		5.5	88	88,000	0
	Peripheral	M5L8243P	125	5.5	44	44,000	0
		M5M82C43P		5.5	66	66,000	0
High Temperature Storage Life	MELPS 740	M50740A-XXXSP	150	—	448	448,000	0
		M50744-XXXSP			120	120,000	0
		M50747-XXXSP			360	720,000	0
		M50753-XXXFP			32	32,000	0
		M50754-XXXSP			60	60,000	0
		M50931-XXXFP			32	32,000	0
		M50943-XXXFP			22	22,000	0
		M50734SP			48	48,000	0
		M37450M2-XXXSP			44	44,000	0
		M37450S4SP			44	44,000	0
		M50747ES	250	—	44	44,000	0
		M50747E-XXXSP	175		66	66,000	0
	MELPS 8-48	M5L8049-XXXP	150	—	66	66,000	0
		M5L8050H-XXXP			66	66,000	0
		M5M80C49-XXXP			88	88,000	0
	MELPS 8-41	M5L8041A-XXXP	150	—	44	44,000	0
		M5L8042-XXXP			88	88,000	0
	Peripheral	M5L8243P	150	—	44	44,000	0
		M5M82C43P			66	66,000	0
Low Temperature Storage Life	MELPS 740	M50740A-XXXSP	−55	5.5	48	44,000	0
		M50744-XXXSP		5.5	36	36,000	0
		M50747-XXXSP		5.5	36	36,000	0
				—	22	22,000	0
		M50753-XXXSP		5.5	36	36,000	0
		M50757-XXXSP		5.5	48	48,000	0
		M50950-XXXSP		5.5	24	24,000	0
		M50734SP		—	22	44,000	0
		M37450S4SP		5.5	22	22,000	0
		M50747E-XXXSP	−55	5.5	44	44,000	0
	MELPS 8-48	M5L8049-XXXP	−55	—	22	22,000	0
		M5M80C49-XXXP			22	22,000	0
	MELPS 8-41	M5L8042-XXXP	−55	—	22	22,000	0

QUALITY ASSURANCE AND RELIABILITY TESTING

Table 3 shows the results of the environment tests of thermal stress high temperature/high humidity and pressure cooker test for the same type of products in regards to endurance tests.

Table 4 shows the results of mechanical tests for representative products of various package types.

Table 3 ENVIRONMENTAL TEST RESULTS

Test	Series	Type Number	Test Condition			Number of Samples	Device Hours (Hours)	Number of Failures
			T_a(℃)	RH(%)	V_{CC}(volt)			
High Temperature High Humidity Life	MELPS 740	M50740A-XXXSP	85	85	5.5	144	288,000	1
		M50744-XXXSP			5.5	72	144,000	0
		M50744-XXXFP			—	88	88,000	0
		M50745-XXXFP			5.5	24	48,000	0
		M50747-XXXSP			5.5	108	216,000	0
		M50747-XXXFP			—	128	128,000	0
		M50753-XXXFP			5.5	32	32,000	0
		M50754-XXXSP			5.5	48	48,000	0
		M50754-XXXFP			—	44	44,000	0
		M50931-XXXFP			—	66	66,000	0
		M50734SP			5.5	48	96,000	0
		M37450M2-XXXSP			5.5	38	38,000	0
		M50747E-XXXSP	85	85	5.5	44	44,000	0
	MELPS 8-48	M5L8049-XXXP	85	85	5.5	66	66,000	0
		M5L8050H-XXXP			5.5	66	66,000	0
		M5M80C49-XXXP			5.5	88	88,000	0
		M5MC49A-XXXFP			5.5	44	44,000	0
	MELPS 8-41	M5L8041A-XXXP	85	85	5.5	32	32,000	0
		M5L8042-XXXP			5.5	88	88,000	0
		M5L8042-XXXP			—	44	44,000	0
	Peripheral	M5L8243P	85	85	5.5	66	66,000	0
		M5M82C43P			5.5	44	44,000	0
		M5M82C43FP			5.5	22	22,000	0

Test	Series	Type Number	Test Condition	Number of Samples	Number of Failures		
					96Hours	240Hours	500Hours
Pressure Cooker	MELPS 740	M50740A-XXXSP	121℃, 100%	666	0	2	4
		M50744-XXXSP		102	0	0	1
		M50747-XXXSP		388	0	1	2
		M50753-XXXFP		44	0	0	1
		M50754-XXXSP		96	0	0	0
		M50754-XXXFP		44	0	0	1
		M50931-XXXFP		44	0	1	2
		M50734SP		66	0	0	0
		M37450M2-XXXSP		38	0	0	0
		M37450S4SP		52	0	0	0
		M50747E-XXXSP	121℃, 100%	220	0	1	—
	MELPS 8-48	M5L8049-XXXP	121℃, 100%	66	0	0	0
		M5L8050H-XXXP		44	0	0	1
		M5M80C49-XXXP		154	0	0	2
	MELPS 8-41	M5L8041A-XXXP	121℃, 100%	44	0	0	0
		M5L8042-XXXP		110	0	0	1
	Peripheral	M5L8243P	121℃, 100%	22	0	0	0
		M5M82C43P		22	0	0	0

QUALITY ASSURANCE AND RELIABILITY TESTING

Test	Series	Type Number	Test Condition	Number of Samples	Number of Failures		
					10Cycles	100Cycles	500Cycles
Temperature Cycling	MELPS 740	M50740A-XXXSP	−65℃, 30min	220	0	0	1
		M50743-XXXSP	150℃, 30min	38	0	0	0
		M50744-XXXSP		120	0	0	0
		M50745-XXXFP		38	0	0	0
		M50747-XXXSP		400	0	0	0
		M50747-XXXFP		38	0	0	0
		M50753-XXXFP		38	0	0	0
		M50754-XXXSP		88	0	0	0
		M50754-XXXFP		96	0	0	0
		M50931-XXXFP		38	0	0	0
		M50734SP		72	0	0	0
		M37450M2-XXXSP		72	0	0	0
		M37450S4SP		52	0	0	0
		M50747ES	−65℃, 30min	38	0	0	0
		M50747E-XXXSP	150℃, 30min	38	0	0	0
	MELPS 8-48	M5L8049-XXXP	−65℃, 30min	88	0	0	0
		M5L8050H-XXXP	150℃, 30min	76	0	0	0
		M5M80C49-XXXP		220	0	0	0
		M5MC49-XXXFP		50	0	0	0
	MELPS 8-41	M5L8041A-XXXP	−65℃, 30min	82	0	0	0
		M5L8042-XXXP	150℃, 30min	50	0	0	0
	Peripheral	M5L8243P	−65℃, 30min	38	0	0	0
		M5M82C43P	150℃, 30min	38	0	0	0

Table 4 MECHANICAL TEST RESULTS

Test	Test Condition	Package Pin Count	40P4		52P4B		64P4B		42P6		72P6, 80P6	
		Series	MELPS 8-48		MELPS 740		MELPS 740		MELPS 8-48		MELPS 740	
			Number of Samples	Number of Failures	Number of Samples	Number of Failures	Number of Samples	Number of Failures	Number of Samples	Number of Failures	Number of Samples	Number of Failures
Soldering Heat	260℃, 10s		44	0	250	0	600	0	44	0	230	0
Thermal shack	−40℃, 125℃, 15cycles		44	0	250	0	600	0	44	0	280	0
Solderebility	230℃, 10s		110	0	110	0	110	0	110	0	110	0
Shock	1500G, 0.5ms		40	0	44	0	52	0	44	0	44	0
Vibration	20G, 100~2000Hz, 4m/cycle, 4cycles/direction		40	0	44	0	52	0	44	0	44	0
Constant Acceleration	20000G, 1m		40	0	44	0	52	0	44	0	44	0
Lead Integrity	250gr/125gr, 90°Berding 2times		100	0	100	0	100	0	100	0	100	0
	500gr/250gr, Tension 30s		50	0	50	0	50	0	50	0	50	0

4 FAILURE ANALYSIS

Accelerated reliability tests are applied to observe failures casued by temperature, voltage, humidity, current, mechanical stress and those combined stresses on chips and packages.

Examples of typical failure modes are shown below.

(1) Wire Bonding Failure by Thermal Stress

Fig. 3, Fig. 4 and Fig. 5 are example of a failure occurred by temperature storage test of 225℃, 1000hours.

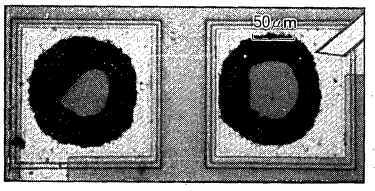


Fig.3 Micrograph of lifted Au ball trace on Al bonding pad

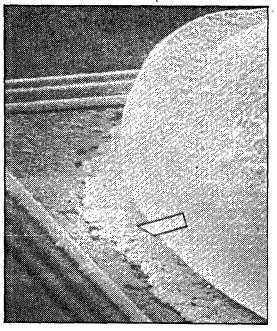


Fig.4 Au-Al plague formation on bonding pad

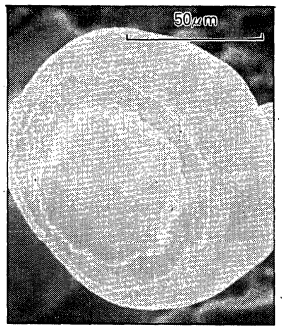


Fig.5 Lifted Au wire ball base

Au-Al intermetallic formation so-called "Purple plague" by thermal overstress makes Au wire lift off from aluminum metallization. The activation energy of this failure mode is estimated approximately 1.0eV and no failure has been observed so far in practical uses.

(2) Aluminum Corrosion Failure by Temperature/Humidity Stress.

Fig. 6, Fig. 7 and Fig. 8 are an example of corroded failure of aluminum metallization in plastic encapsulated IC after accelerated temperature/humidity storage test (pressure cooker test) of 121℃, 100% RH, 1000hours duration.

Aluminum bonding pad is dissolved by penetrated water from plastic package, and chlorine concentration is observed on corroded aluminum bonding pad as shown in Fig. 8.

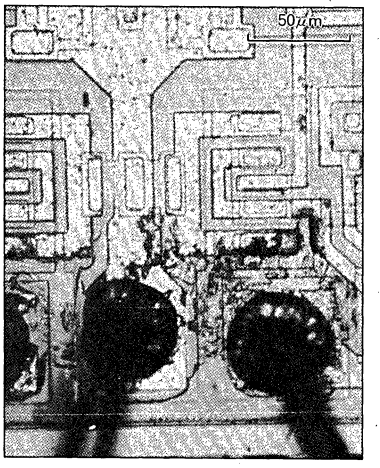


Fig.6 Micrograph of corroded Aluminum metallization

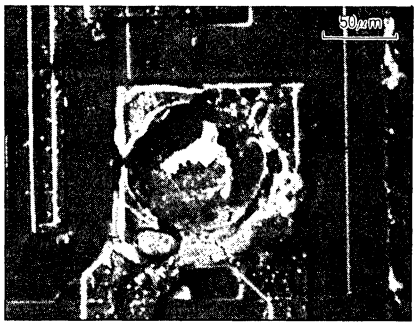


Fig.7 Enlarged micrograph of corroded Aluminum bonding pad

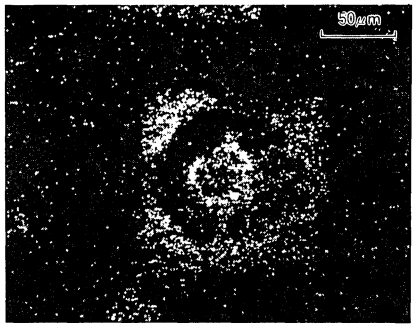


Fig.8 CI distribution on corroded Aluminum bonding pad

(3) Destructive Failure by Electrical Overstress
ESD have been performed to reproduce the electrical overstress failure in field uses.
Fig. 9 and Fig. 10 are an example of failure observed by surge voltage test. The trace of destruction is verified as the aluminum bridge by X-ray micro analysis.

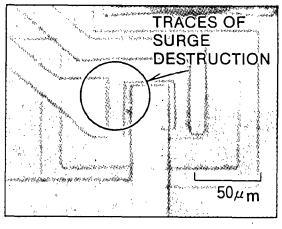


Fig.9 Micrograph of surge voltage destruction

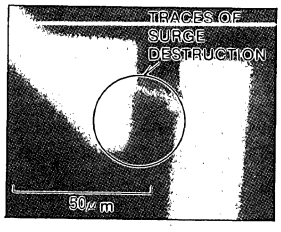


Fig.10 Aluminum trace of destructive spot

(4) Aluminum Electromigration
Fig. 11 shows an open circuit of aluminum metallization in high current density region caused by accelerated operating life test. This failure is caused by the aluminum electromigration. Voids and hillock have been formed in aluminum metallization by high current density.

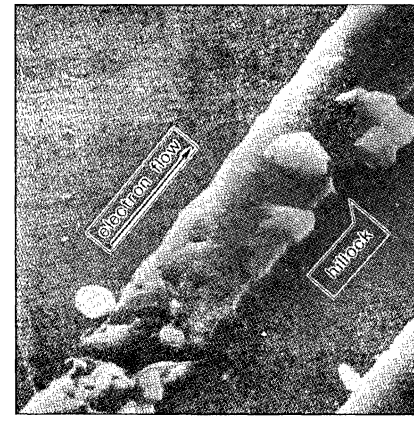


Fig.11 Voids and hillocks formation by Aluminum electromigration

5 SUMMARY

The Mitsubishi quality assurance system and examples of reliability control have been discussed. Customer's interest and requirement for high reliable IC & LSI are increasing significantly. To satisfy customer's expectancy. Mitsubishi as an IC vendor, would like to make perpetual efforts in the following areas.

(1) Emphasis on built-in reliability at design stage and reliability evaluation to investigate latent failure modes and acceleration factors.
(2) Execution of periodical endurance, environment and mechanical test to verify reliability target and realize higher reliability.
(3) Focus on development of advanced failure analysis techniques. Detail failure analysis, intensive corrective action and quick response to customer's analysis request.
(4) Collection of customer's quality data in qualification, incoming inspection, production and field use to improve PPM, fraction defective and FIT, failure rate.

Mitsubishi would highly appreciate if the customer would provide quality and reliability data of incoming inspection or field failure rate essential to verify and improve the quality/reliability of IC & LSI.

QUALITY ASSURANCE AND RELIABILITY TESTING

A MOS transistor has a very thin oxide insulator under the gate electrode on the silicon substrate. It is operated by altering the conductance (g_m) between source and drain to control mobile charges in the channel formed by the applied gate voltage.

If a high voltage were applied to a gate terminal, the insulator-film under the gate electrode could be destroyed, and all Mitsubishi MOS IC/LSIs contain internal protection circuits at each input terminal to prevent this. It is inherently necessary to apply reverse bias to the P-N junctions of a MOS IC/LSI.

Under certain conditions, however, it may be impossible to completely avoid destruction of the thin insulator-film due to the application of unexpectedly high voltage or thermal destruction due to excessive current from a forward biased P-N junction. Therefore the following recommendations should be followed in handling MOS devices.

1. KEEPING VOLTAGE AND CURRENT TO EACH TERMINAL BELOW MAXIMUM RATINGS

1. The recommended ranges of operating conditions provide adequate safety margins. Operating within these limits will assure maximum equipment performance and quality.
2. Forward bias should not be applied to any terminal since excessive current may cause thermal destruction.
3. Output terminals should not be connected directly to the power supply. Short-circuiting of a terminal to a power supply having low impedance may cause burn-out of the internal leads or thermal destruction due to excessive current.

2. KEEPING ALL TERMINALS AT THE SAME POTENTIAL DURING TRANSPORT AND STORAGE

When MOS IC/LSIs are not in use, both input and output terminals can be in a very high impedance state so that they are easily subjected to electrostatic induction from AC fields of the surrounding space or from charged objects in their vicinity. For this reason, MOS IC/LSIs should be protected from electrostatic charges while being transported and stored by conductive rubber foam, aluminum foil, shielded boxes or other protective precautions.

3. KEEPING ELECTRICAL EQUIPMENT, WORK TABLES AND OPERATING PERSONNEL AT THE SAME POTENTIAL

1. All electric equipment, work table surfaces and operating personnel should be grounded. Work tables should be covered with copper or aluminum plates of good conductivity, and grounded. One method of grounding personnel, after making sure that there is no potential difference with electrical equipment, is by the use of a wristwatch metallic ring, etc. attached around the wrist and grounded in series with a 1mΩ resistor. Be sure that the grounding meets national regulations on personnel safety.
2. Current leakage from electric equipment must be prevented not only for personnel safety, but also to avert the destruction of MOS IC/LSIs, as described above. Items such as testers, curve-tracers and synchroscopes must be checked for current leakage before being grounded.

4. PRECAUTIONS FOR MOUNTING OF MOS IC/LSIs

1. The printed wiring lines between input and output terminals of MOS IC/LSIs should not be close to or parallel to high-voltage or high-power signal lines. Turning power on while the device is short-circuited, either by a solder bridge made during assembly or by a probe during adjusting and testing, may cause maximum ratings to be exceeded, which can result in the destruction of the device.
2. When input/output, or input and/or output, terminals of MOS IC/LSIs (now open-circuits) are connected, we must consider the possibility of current leakage and take precautions similar to §2 above. To reduce such undesirable trouble, it is recommended that an interface circuit be inserted at the input or output terminal, or a resistor with a resistance that does not exceed the output driving capability of the MOS IC/LSI be inserted between the power supply and the ground.
3. A filter circuit should be inserted in the AC power supply line to absorb surges which can frequently be strong enough to destroy a MOS IC/LSI.
4. Terminal connections should be made as described in the catalog while being careful to meet specifications.
5. Ungrounded metal plates should not be placed near input or output terminals of any MOS IC/LSIs, since destruction of the insulation may result if they become electrostatically charged.
6. Equipment cases should provide shielding from electrostatic charges for more reliable operation. When a plastic case is used, it is desirable to coat the inside of the case with conductive paint and to ground it. This is considered necessary even for battery-operated equipment.

SERIES MELPS 740 SINGLE-CHIP 8-BIT MICROCOMPUTERS

2

M50740A-XXXSP/FP, M50741-XXXSP/FP
M50740ASP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50740A-XXXSP, M50741-XXXSP and the M50740ASP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 52-pin shrink plastic molded DIP (flat package type also available). These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences among the M50740A-XXXSP, M50741-XXXSP and the M50740ASP are noted below. The following explanations apply to the M50740A-XXXSP. Specification variations for other chips are noted accordingly.

M50740A-XXXSP	ROM 3072bytes Port P0, P1, P2·····Pull-up transistor option Port P3·····Pull-down transistor option Port R·····Input exclusive option
M50741-XXXSP	ROM 4096bytes
M50740ASP	External ROM type of M50740A-XXXSP

The differences among the M50740A-XXXSP and the M50740A-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

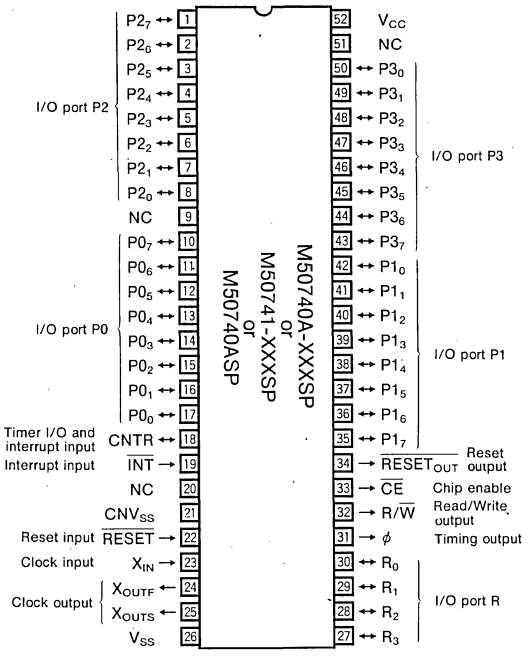
DISTINCTIVE FEATURES

- Number of basic instructions····· 70
- Memory size ROM ·····3072bytes (M50740A-XXXSP)
  4096bytes (M50741-XXXSP)
  RAM·····96bytes
- Instruction executing time
  ····· 2μs (minimum instructions at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz·····5V±10%
- Power dissipation
  normal operation mode (at 4MHz frequency)
  ····· 15mW (V_{CC}=5V, Typ.)
- Subroutine nesting ·····48 levels (Max.)
- Interrupt·····6types, 5 vecters
- 8-bit timer·····3
- Programmable I/O (Ports P0, P1, P2, P3)·····32

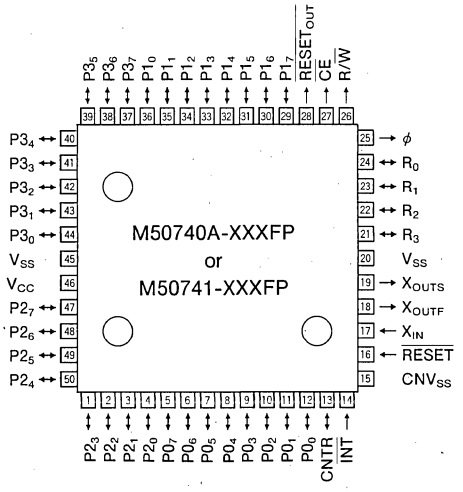
APPLICATION

VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 52P4B

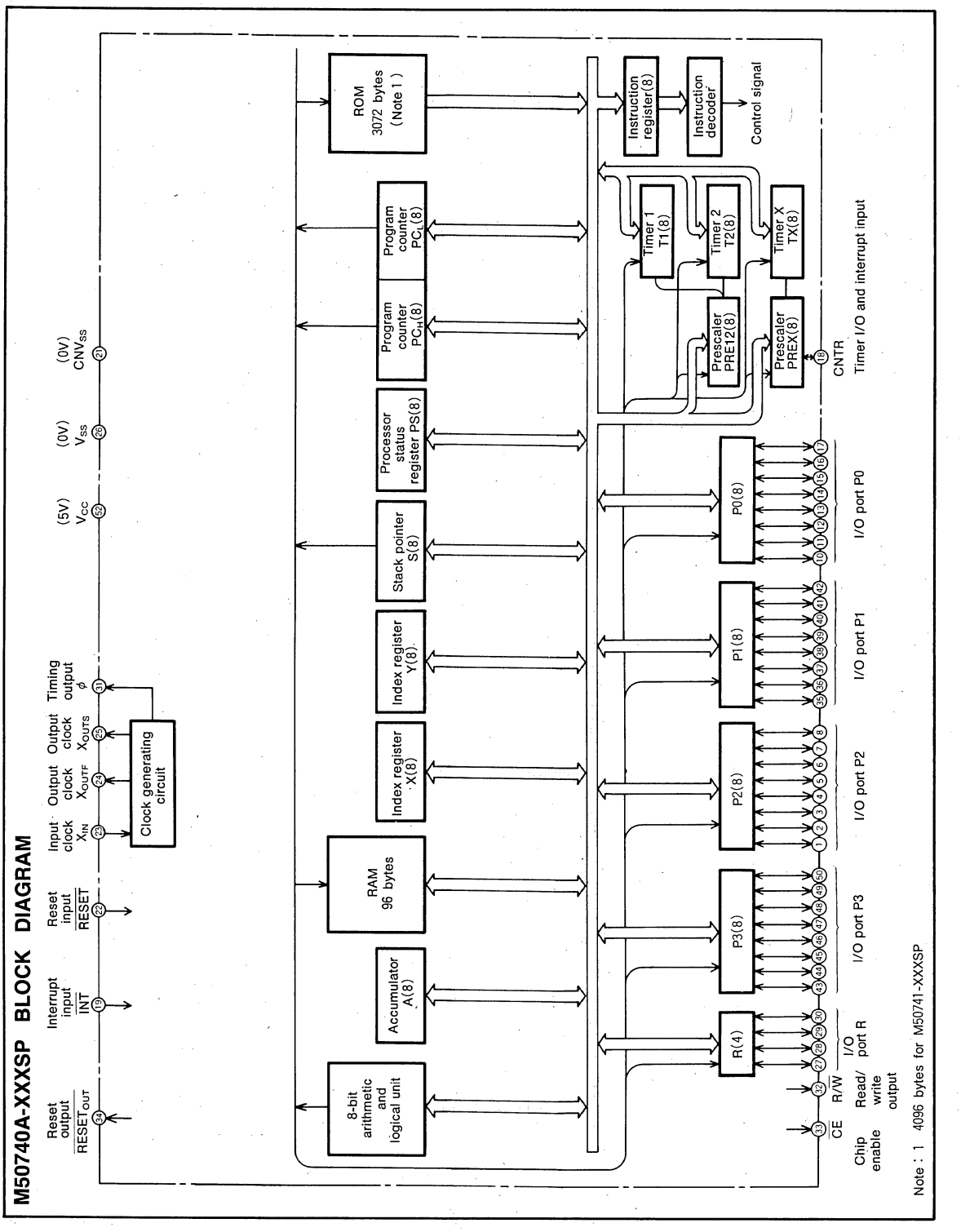


Outline 50P6

For M50740ASP, CNV_{SS} should be connected to V_{CC}

NC : No Connection

M50740A-XXXSP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONS OF M50740A-XXXSP

Parameter			Functions
Number of basic instruction			70
Instruction execution time			2μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory size	ROM		3072bytes (4096bytes for M50741-XXXSP)
	RAM		96bytes
I/O port	$\overline{INT}$	Input	1-bit×1
	P0, P1, P2, P3	I/O	8-bit×4
	R	I/O	4-bit×1
	CNTR	I/O	1-bit×1
Timers			8-bit prescaler×2+8-bit timer×3
Subroutine nesting			48 level (max.)
Interrupts			External interrupt 2, Timer interrupt 3
Clock generating circuit			Built-in (RC, ceramic or quartz crystal oscillator)
Supply voltage	at operating		5V±10%
Power dissipation	at high speed		15mW (at 4MHz frequency)
I/O characteristics	I/O voltage		12V (ports P0, P1, P2, $\overline{INT}$, CNTR)
	Output current		10mA (ports P0, P1, P2, P3)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M50740A-XXXSP, M50741-XXXSP, M50740ASP		52-pin shrink plastic molded DIP
	M50740A-XXXFP, M50741-XXXFP		50-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS} (for M50740ASP, connected to V_{CC}).
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external RC circuit is connected between the X_{IN} and X_{OUTS} or the X_{OUTF} pins, and an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUTS} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin, and the X_{OUTS} and X_{OUTF} pins should be left open.
X_{OUTS}	Clock output	Output	This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a RC circuit, a ceramic or a quartz crystal oscillator between this pin and X_{IN} pin.
X_{OUTF}	Clock output	Output	This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a RC circuit between this pin and X_{IN} pin.
ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O or interrupt input	I/O	This is in common with an I/O for the timer X and an interrupt input pin.
$\overline{INT}$	Interrupt input	Input	This is the lowest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is P-channel open drain.
R_0~R_3	I/O port R	I/O	Port R is a 4-bit I/O port, and is used to connect with an I/O expander. For M50740A-XXXSP, it can be only for input.
R/$\overline{W}$	Read/Write output	Output	This pin outputs read/write signal for I/O expander.
$\overline{CE}$	Chip enable output	Output	This pin outputs the chip enable signal for I/O expander.
$\overline{RESET_{OUT}}$	Reset output	Output	This pin outputs the reset signal for I/O expander.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50740A-XXXSP is shown in Figure 1. Addresses 1400_{16} to $1FFF_{16}$ are assigned to the built-in ROM area which consists of 3072 bytes.

Addresses 1000_{16} to $1FFF_{16}$ are the ROM address area assigned to the M50741-XXXSP.

Addresses $1F00_{16}$ to $1FFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $1FF4_{16}$ to $1FFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $005F_{16}$ are assigned to the built-in RAM and consist of 96 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

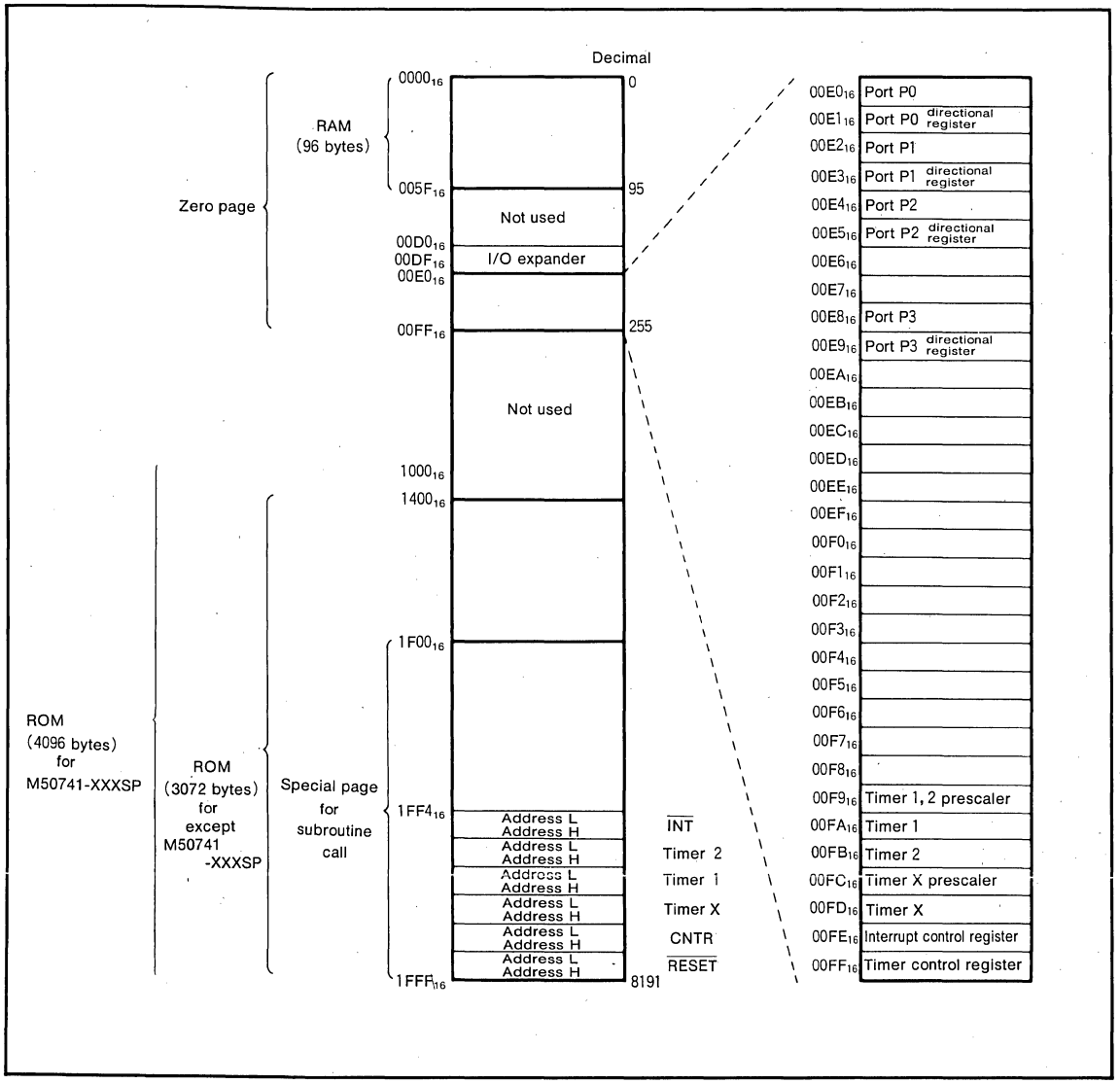


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.
The contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When using this microcomputer in the single-chip mode, the stack pointer should be set at the bottom address of the internal RAM.
When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.
The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.
The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed. PC_H is only 5 bits long.

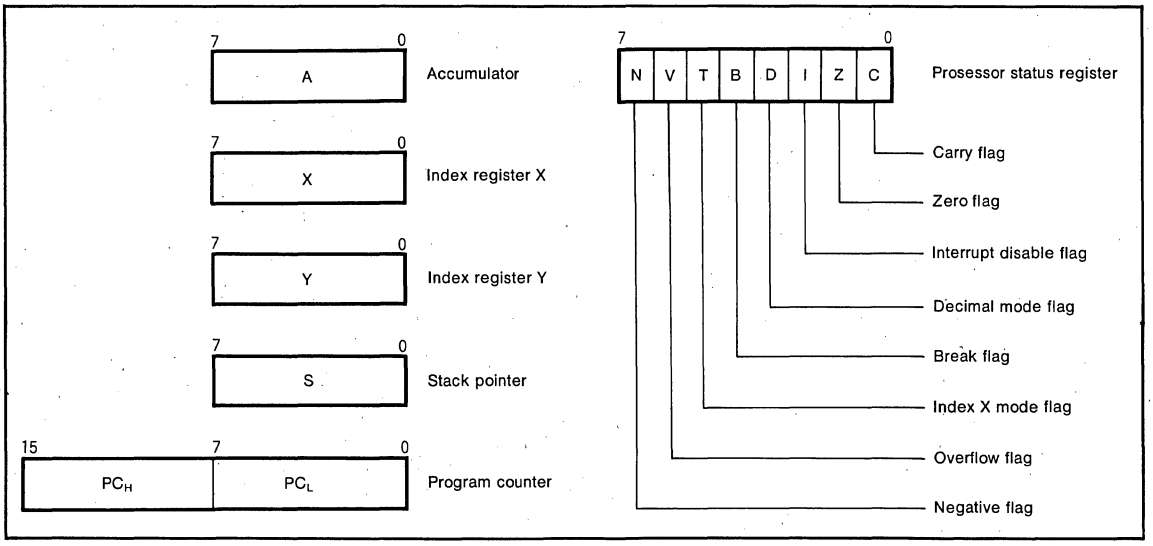


Fig.2 Register structure

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The oveflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

INTERRUPT

The M50740A-XXXSP can be interrupted from seven souces; CNTR, timer X, timer 1, timer 2, or $\overline{INT}$/BRK instruction.

These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the CNTR or $\overline{INT}$ pins go from "H" to "L"

(2) When the contents of timer X, timer 1, timer 2 go to "0"

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the $\overline{INT}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT}$ generated the interrupt.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$1FFF_{16}$, $1FFE_{16}$
CNTR	2	$1FFD_{16}$, $1FFC_{16}$
Timer X	3	$1FFB_{16}$, $1FFA_{16}$
Timer 1	4	$1FF9_{16}$, $1FF8_{16}$
Timer 2	5	$1FF7_{16}$, $1FF6_{16}$
$\overline{INT}$(BRK)	6	$1FF5_{16}$, $1FF4_{16}$

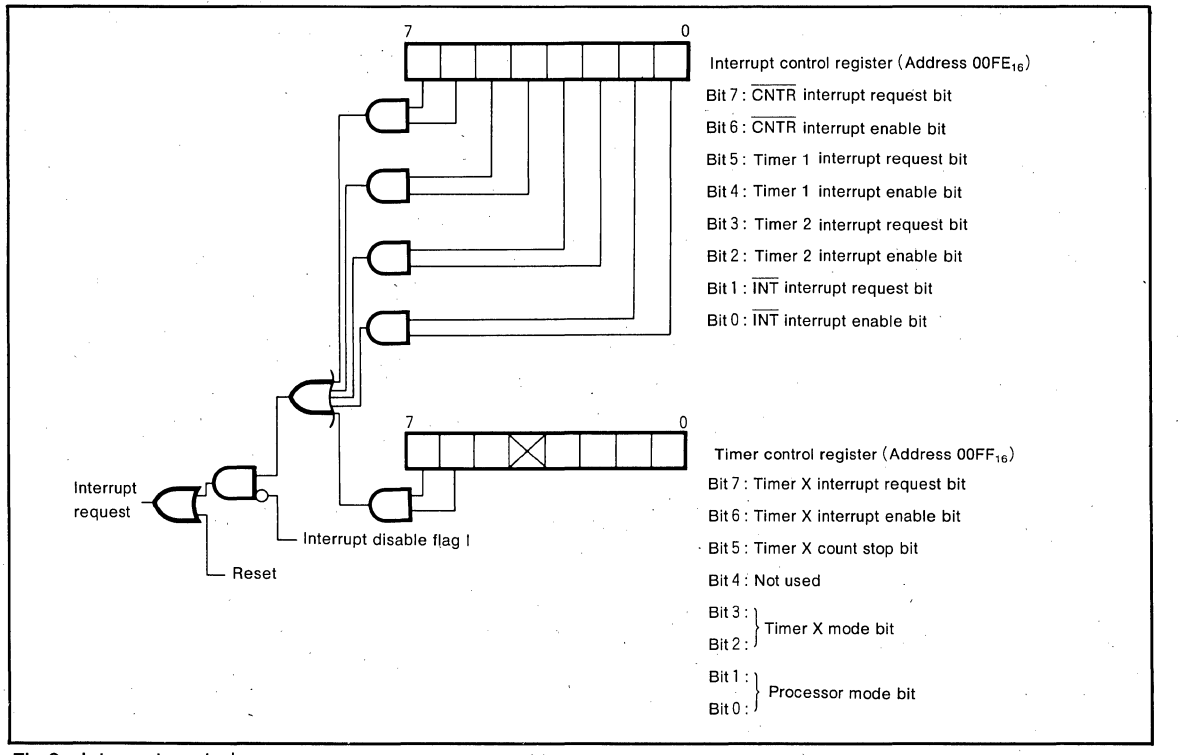


Fig.3 Interrupt control

TIMER

The M50740A-XXXSP has three timers; timer X, timer 1, and timer 2. Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1 and timer 2 is shown in Figure 4.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+2)$, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section). The prescaler latch and timer latch can be loaded with any number except zero.

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock sourse.

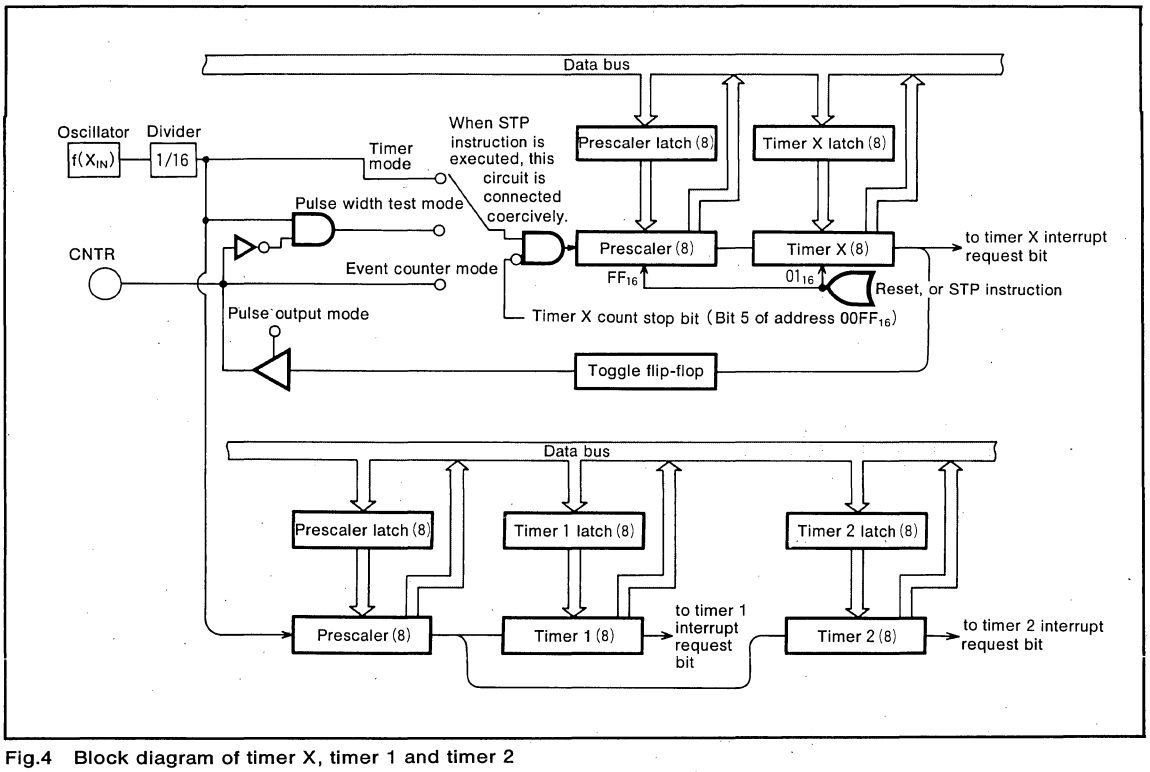


Fig.4 Block diagram of timer X, timer 1 and timer 2

(4) Pulse width measurement mode [11]

This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

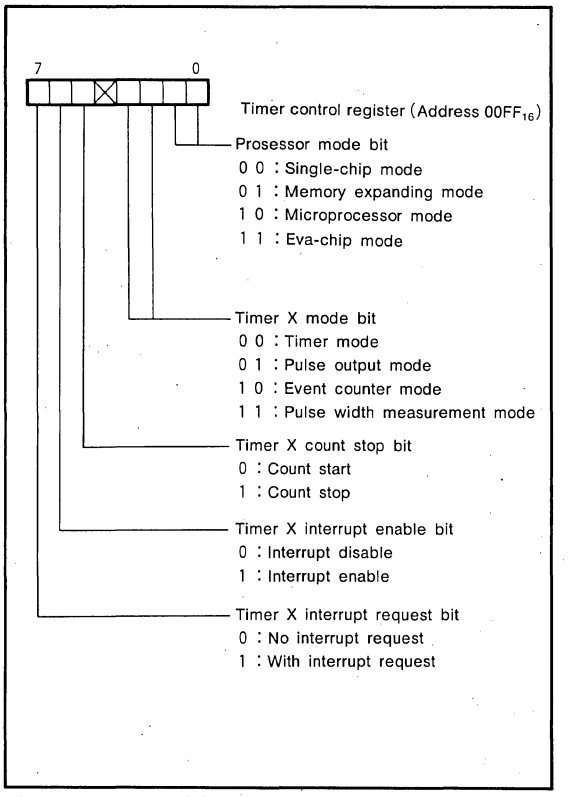


Fig.5 Structure of timer control register

		Address	
(1)	Port P0 directional register	($E1_{16}$) ···	00_{16}
(2)	Port P1 directional register	($E3_{16}$) ···	00_{16}
(3)	Port P2 directional register	($E5_{16}$) ···	00_{16}
(4)	Port P3 directional register	($E9_{16}$) ···	00_{16}
(5)	Prescaler X	(FC_{16}) ···	FF_{16}
(6)	Timer X	(FD_{16}) ···	01_{16}
(7)	Interrupt control register	(FE_{16}) ···	00_{16}
(8)	Timer control register	(FF_{16}) ···	00_{16}
(9)	Interrupt disable flag on processor status register	(PS) ···	1
(10)	Program counter	(PC_H) ···	Contents of address $1FFF_{16}$
		(PC_L) ···	Contents of address $1FFE_{16}$

(11) The output of oscillator is in the same state as the one after "FST" instruction execution, and is connected to X_{OUTF} pin.

Fig.7 Internal state of microcomputer at reset

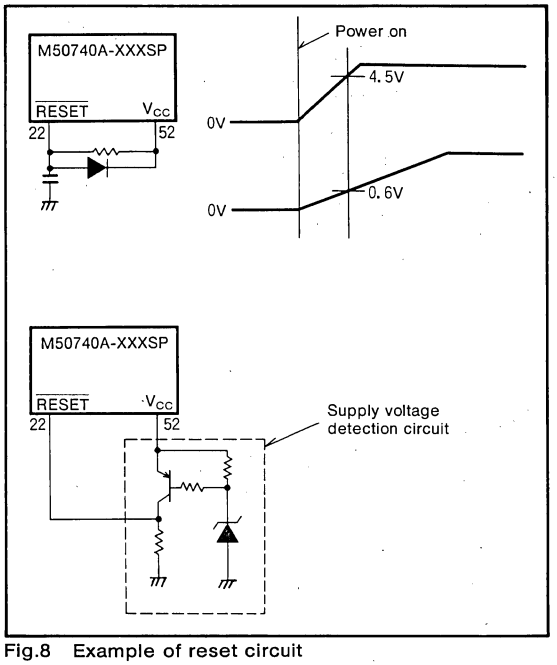


Fig.8 Example of reset circuit

RESET CIRCUIT

The M50740A-XXXSP is reset according to the sequence shown in Figure 6. It starts the program from the address formed by the content of address $1FFF_{16}$ as the high order address and the content of the address $1FFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable, and then returned to "H" level. The internal initializations following reset are shown in Figure 7.

An example of the reset circuit is shown in Figure 8.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

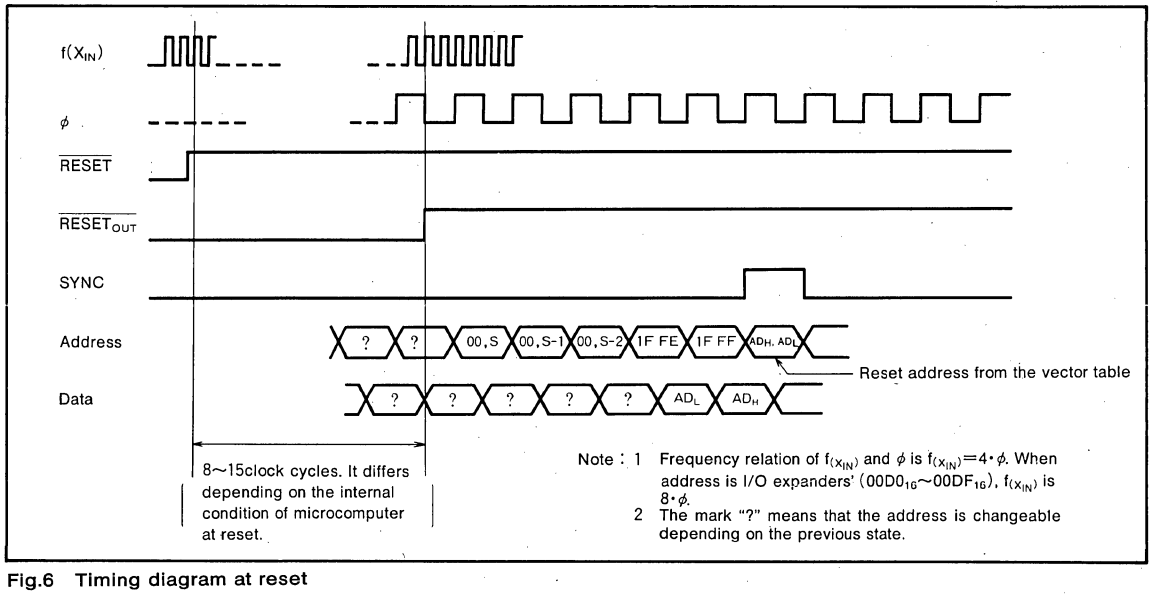


Fig.6 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

Pull-up transistor can be specified as an option for M50740A-XXXSP. As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

Port P3 is an 8-bit I/O port with P-channel open drain outputs. This port also has the pull-down transistor option for M50740A-XXXSP.

(5) Port R

Port R communicates with an I/O expander. When ϕ goes to level "H", port R outputs the port address to that of the I/O expander. When ϕ goes to "L", it outputs/inputs data to from the I/O expander. The above data is effective only when $\overline{CE}$ pin goes to "L". For the M50740A-XXXSP, this port can be an input port as an option. The timing diagram is shown in Figure 9.

(6) $\overline{CE}$ pin

The $\overline{CE}$ pin goes to "L" when addresses are moved to the I/O expander addresses ($00D0_{16} \sim 00DF_{10}$). This port is used to determine whether the address or data of port R is effective.

(7) R/$\overline{W}$ pin

The R/$\overline{W}$ pin goes to "L" when the operation is executed. The R/$\overline{W}$ signal tells an external device that the CPU wants to write or read.

(8) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ. When $\overline{CE}$ pin goes to "L", the oscillator frequency divided by eight is output as ϕ. This is to synchronize with I/O expander.

(9) $\overline{RESET_{OUT}}$ pin

Wne the $\overline{RESET}$ pin goes to level "L", the $\overline{RESET_{OUT}}$ pin also goes to "L". On the other hand, when the $\overline{RESET}$ pin goes to "H" the $\overline{RESET_{OUT}}$ pin also goes to "H" after 8~15 clock cycles. This output is used to reset the external devices.

(10) $\overline{INT}$ pin

The INT pin is an interrupt input pin. The $\overline{INT}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

(11) CNTR pin

The CNTR pin is an I/O pin of timer X and also an interrupt input pin. The CNTR interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

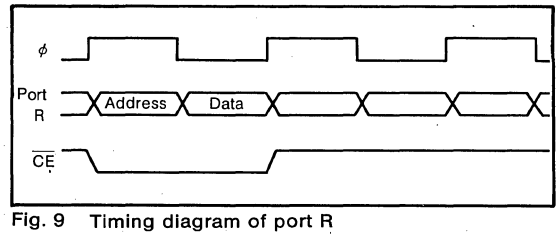


Fig. 9 Timing diagram of port R

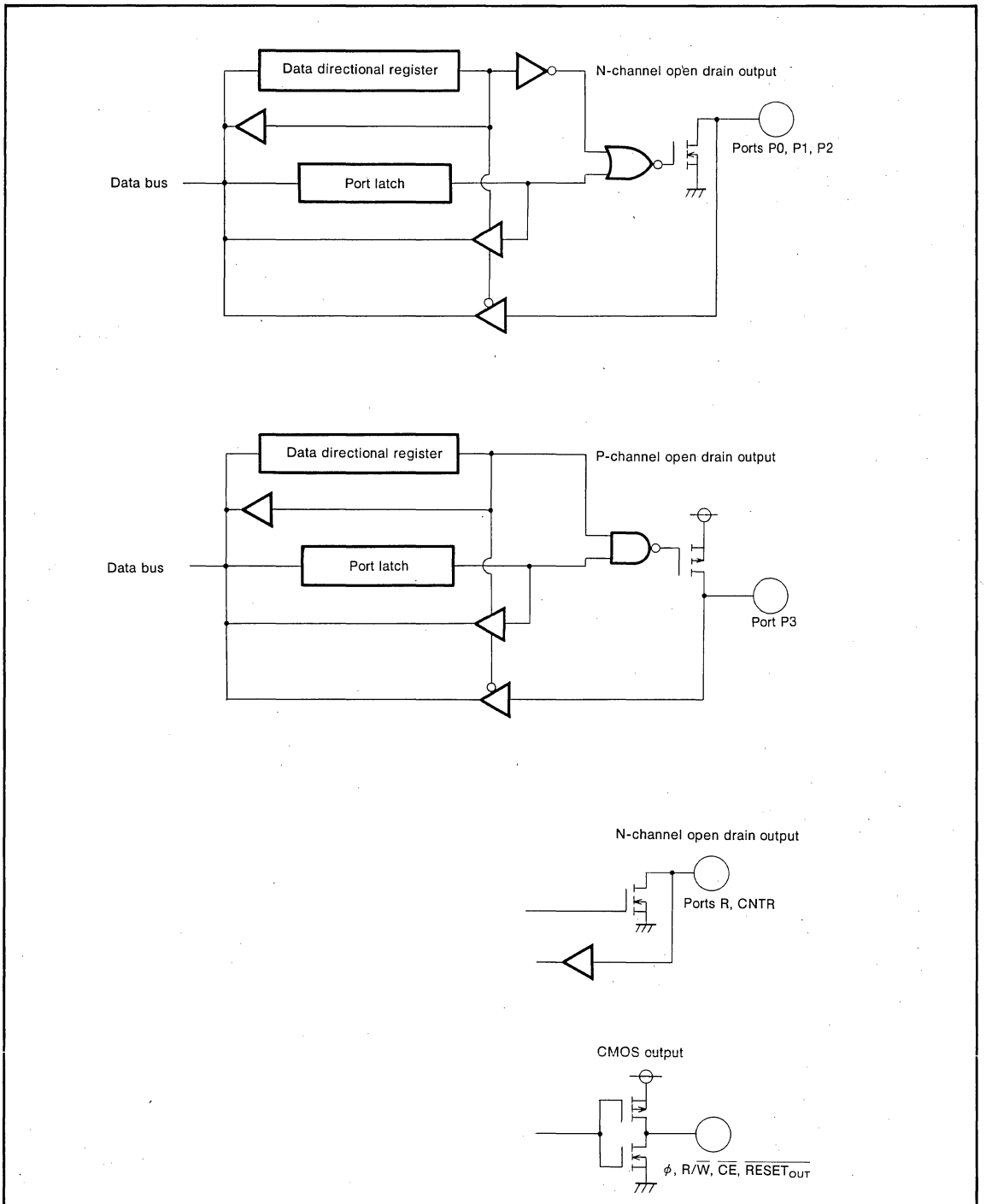


Fig.10 Block diagram of port P0~P3 (singl-chip mode) and output formats of port R, CNTR, ϕ, R/$\overline{W}$, $\overline{CE}$, $\overline{RESET_{OUT}}$

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0 ~ P2 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 11 shows the functions of ports P0~P2.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 12.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits.

Supplying "H" level to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0 ~ P2 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 5 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions.

Pins $P1_6$ and $P1_5$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. $\overline{RDY}$ signal is input from $P1_7$. When in the "L" state, $P1_5$, $P1_6$, and $P1_7$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The $\overline{RDY}$ is a ready signal input and, when it goes to "L", internal clock stops and the CPU waits the data. However, the oscillation does not stop.

Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of $D_7 \sim D_0$ (including instruction code) while at the "L" state.

(3) Microprocessor mode [10]

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port $P1_5$, $P1_6$ and $P1_7$ become the R/$\overline{W}$, SYNC and $\overline{RDY}$ pins, respectively and the normal I/O functions are lost. Port P2 becomes the data bus ($D_7 \sim D_0$) and loses its normal I/O functions. Internal memory ($00E1_{16}$ to $00E0_{16}$) cannot be used, and an external memory is needed if the address where normal I/O function have lost.

(4) Eva-chip mode [11]

When "H" level is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

With the exceptions that the internal ROM is disabled and that external memory must be attached, this mode is the same as the memory expanding mode.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	M50741-XXXSP		M50740A-XXXSP		M50740ASP	
V_{SS}	• Single-chip • Memory expanding • Eva-chip • Microprocessor	After reset, processor mode is single chip mode. All modes can be selected by changing the processor mode bit in the program.	Same as left		—	
V_{CC}	• Eva-chip	Eva-chip mode only	• Microprocessor • Eva-chip	After reset, processor mode is microprocessor mode. Eva chip mode also can be selected by changing the processor mode bit in the program.	• Microprocessor	Microprocessor mode only. (Do not change the processor mode bit in the program).
+10V	—		• Eva-chip	Eva-chip mode only	—	

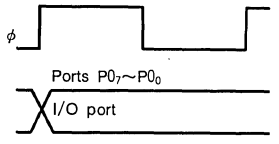
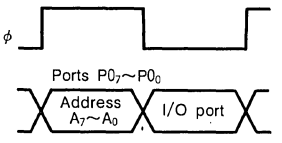
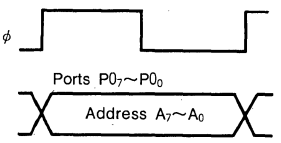
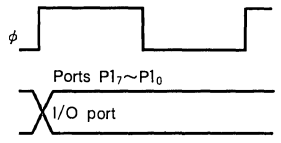
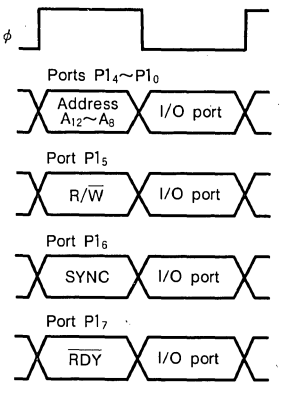
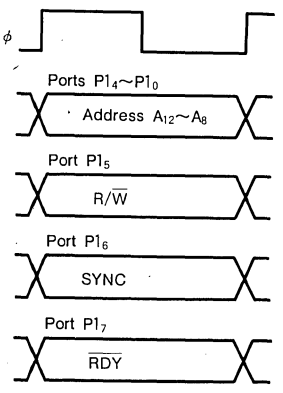
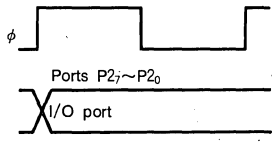
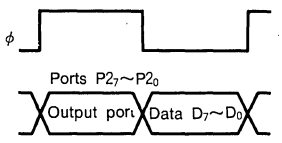
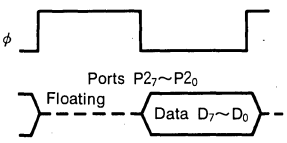
Port \ Mode	CM_1 = 0, CM_0 = 0 Single-chip mode	CM_1 = 0, CM_0 = 1 Memory expanding mode	CM_1 = 1, CM_0 = 1 Eva-chip mode	CM_1 = 1, CM_0 = 0 Microprocessor mode
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	

Fig.11 Processor mode and functions of ports P0~P2

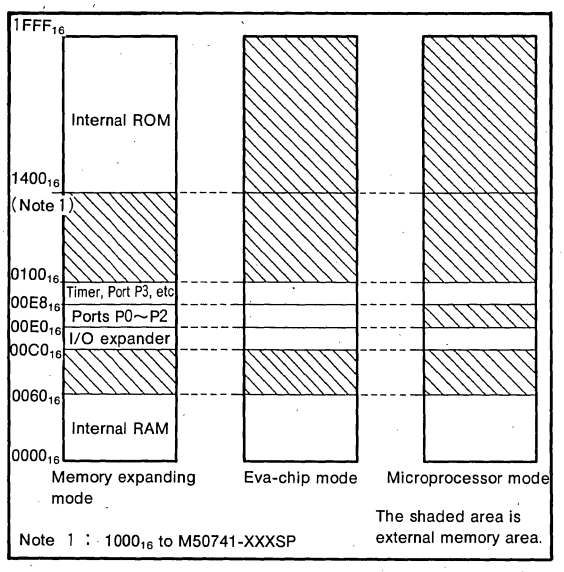


Fig.12 External memory area in processor mode

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 13.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleared when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

To return from the stop status, the interrupt enable bit must be set to "1" before executing STP instruction. To return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

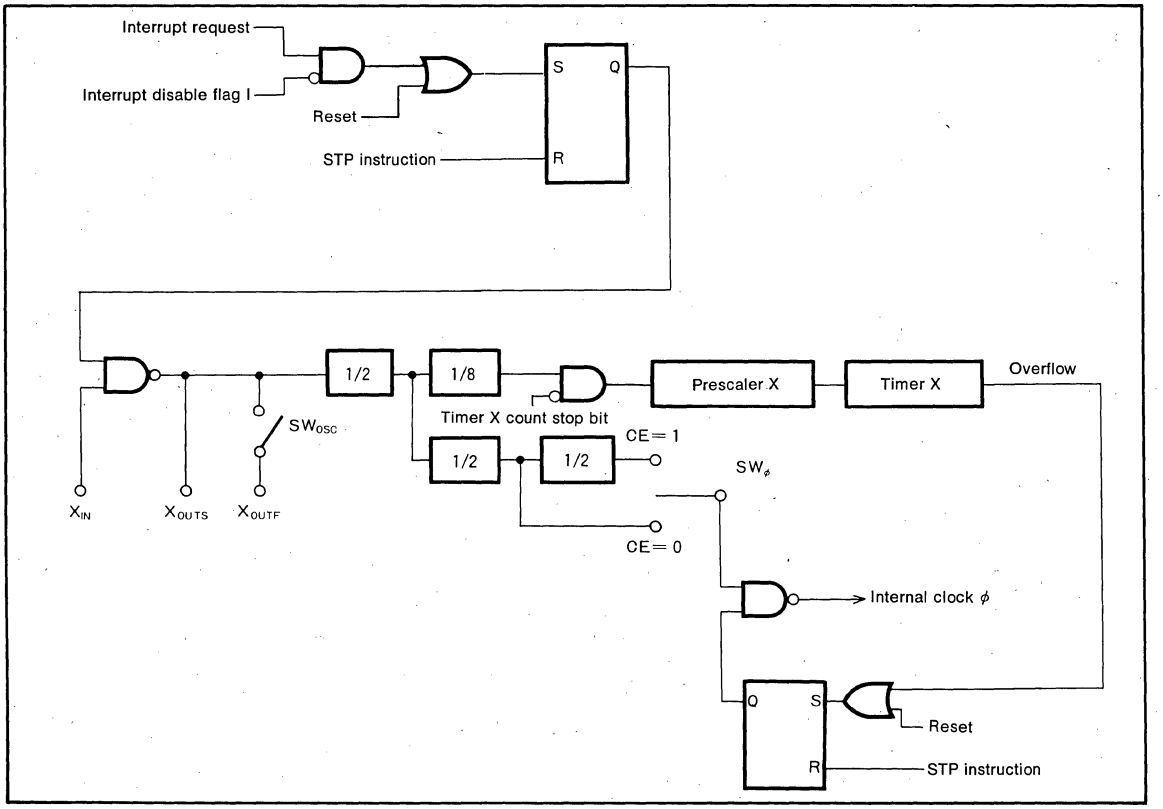


Fig.13 Block diagram of clock generating circuit

MITSUBISHI ELECTRIC

When FST instructions are executed, SW_{OSC} closes and when SLW instructions are executed, it opens. These instructions are used for CR oscillation and changes oscillation fequency. The SW_{OSC} closes at reset.

The SW_{ϕ} is connected to the output of oscillation frequency divided by 8 (CE=1) when addresses are I/O expanders ($00D0_{16}$~$00DF_{16}$), otherwise it is connected to the output devided by 4 (CE=0). Therefore the frequency of the internal clock ϕ differs depending on addresses.

This is to retain enough time for communication between I/O expander and signals.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 14.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufacturs suggested value.

The example of external clock usage is shown in Figure 15. X_{IN} is the input, and X_{OUT} is open.

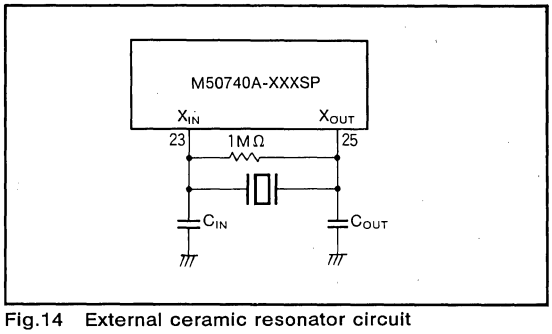


Fig.14 External ceramic resonator circuit

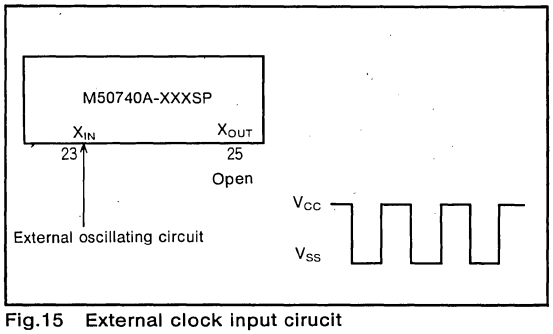


Fig.15 External clock input cirucit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+2).
(2) Set a value other than "0" for the timer and the prescaler.
(3) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(4) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
(5) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(6) A NOP instruction must be used after the execution of a PLP instruction.
(7) The timer X and prescaler X must be set "FF_{16}" immediately before the execution of a STP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) Mask ROM confirmation form
(2) Mark specification form
(3) ROM data ····· EPROM 3sets

Write the following option on the mask ROM confirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port R I/O mode

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off.	−0.3∼7	V
V_I	Input voltage R_0∼R_3, CNV_{SS}(Note 1), $\overline{RESET}$, X_{IN}		−0.3∼7	V
V_I	Input voltage $P3_0$∼$P3_7$		−3.0∼V_{CC}+0.3	V
V_I	Input voltage $\overline{INT}$, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, CNTR		−0.3∼13	V
V_O	Output voltage R_0∼R_3		−0.3∼7	V
V_O	Output voltage $P3_0$∼$P3_7$, X_{OUTF}, X_{OUTS}, ϕ, R/$\overline{W}$, $\overline{CE}$, $\overline{RESET_{OUT}}$		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, CNTR		−0.3∼13	V
P_d	Power dissipation	T_a=25℃	1000(Note 2)	mW
T_{opr}	Operating temperature		−10∼70	℃
T_{stg}	Storage temperature		−40∼125	℃

Note 1 : −0.3∼13V for M50740A-XXXSP.
2 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (T_a=−10∼70℃, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Nom.	Max.	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, R_0∼R_3, CNV_{SS}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, CNTR, $\overline{INT}$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, $\overline{RESET}$	M50740A-XXXSP M50740ASP	0.8V_{CC}		V_{CC}	V
		M50741-XXXSP	0.48V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, X_{IN}		0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, R_0∼R_3, CNV_{SS}		0		0.2V_{CC}	V
V_{IL}	"L" input voltage, CNTR, $\overline{INT}$		0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}		0		0.12V_{CC}	V
$I_{OL(peak)}$	"L" peak output current, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$				10	mA
$I_{OL(avg)}$	"L" average output current, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$				5	mA
$I_{OH(peak)}$	"H" peak output current, $P3_0$∼$P3_7$				−10	mA
$I_{OH(avg)}$	"H" average output current, $P3_0$∼$P3_7$				−5	mA
$f_{(X_{IN})}$	Internal clock oscillating freqency				4	MHz

Note 3 : High-level input voltage of up to +12V may be applied to permissible for ports P0, P1, P2, CNTR, and $\overline{INT}$
4 : The total of low-level peak output current should be 60mA max. for ports P0 and P2
The total of low-level peak output current should be 30mA max. for port P1
The total of low-level peak output current should be 80mA max. for port P3

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage, $P3_0 \sim P3_7$	T_a=25℃ I_{OH}=−10mA		3			V
V_{OH}	"H" output voltage, ϕ, R/$\overline{W}$, $\overline{CE}$, $\overline{RESET_{OUT}}$	T_a=25℃ I_{OH}=−2.5mA		3			V
V_{OL}	"L" output voltage, $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$ $R_0 \sim R_3$, CNTR	T_a=25℃ I_{OL}=10mA				2	V
V_{OL}	"L" output voltage, ϕ, R/$\overline{W}$, $\overline{CE}$, $\overline{RESET_{OUT}}$	T_a=25℃ I_{OL}=5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis, CNTR, $\overline{INT}$	T_a=25℃		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{RESET}$	T_a=25℃			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis, X_{IN}	T_a=25℃		0.1		0.5	V
I_I	Input leak current, $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$ $\overline{INT}$, CNTR	T_a=25℃ 0 ≦ V_I ≦ 12V, without port option		−12		12	μA
I_I	Input leak current, $P3_0 \sim P3_7$, $R_0 \sim R_3$, CNV_{SS}, $\overline{RESET}$, X_{IN}	T_a=25℃ 0 ≦ V_I ≦ 5V, without port option		−5		5	μA
I_{IL}	"L" input current, $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$	T_a=25℃ V_I = 0V, with port option		−60		−200	μA
I_{IH}	"H" input current, $P3_0 \sim P3_7$	T_a=25℃ V_I = 5V, with port option		60		200	μA
V_{RAM}	RAM retention voltage	Stop mode		2			V
I_{CC}	Supply current	P-channel open drain input/output to V_{CC}, output terminals are opened, others to V_{SS}	$f_{(X_{IN})}$=4MHz Square wave		3	6	mA
			Stop mode T_a=25℃			1	μA
			Stop mode T_a=70℃			10	μA

TIMING REQUIREMENTS
Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{SU(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{SU(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{SU(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{SU(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{SU(RD-\phi)}$	Port R input setup time	330			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	0			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	0			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	0			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	0			ns
$t_{h(\phi-RD)}$	Port R input hold time	0			ns
t_C	External clock input cycle time	250			ns
t_W	External clock input pulse width	75			ns
t_r	External clock rising edge time			25	ns
t_f	External clock falling edge time			25	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, Vss=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(RDY-\phi)}$	$\overline{RDY}$ input setup time	150			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	0			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	0			ns
$t_{h(\phi-RDY)}$	$\overline{RDY}$ input hold time	500			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	0			ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(\phi-RDY)}$	$\overline{RDY}$ input setup time	150			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-RDY)}$	$\overline{RDY}$ input hold time	500			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	0			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.17			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig.18			200	ns
$t_{d(\phi-RA)}$	Port R address output delay time	Fig.17			200	ns
$t_{d(\phi-RAF)}$	Port R address output delay time		0		200	ns
$t_{d(\phi-RQ)}$	Port R data output delay time				200	ns
$t_{d(\phi-RQF)}$	Port R data output delay time				200	ns
$t_{d(\phi-CE)}$	$\overline{CE}$ output delay time	Fig.19			200	ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ output delay time				100	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.17			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address and control signal delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address and control signal delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				200	ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25°C, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.17			250	ns
$t_{d(\phi-P1A)}$	Port P1 address and control signal delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				200	ns

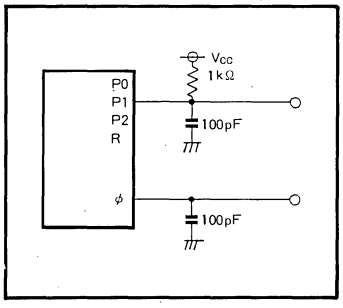


Fig.17 Ports P0~P2, R test circuit

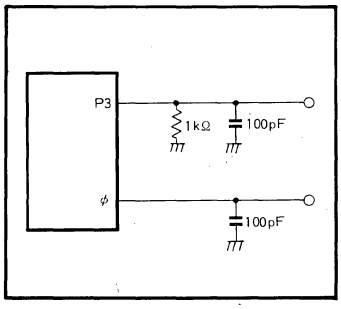


Fig.18 Port P3 test circuit

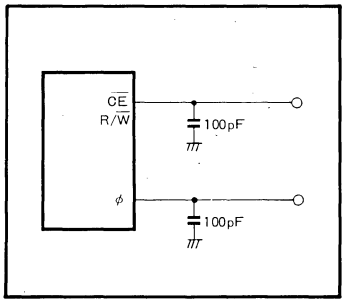
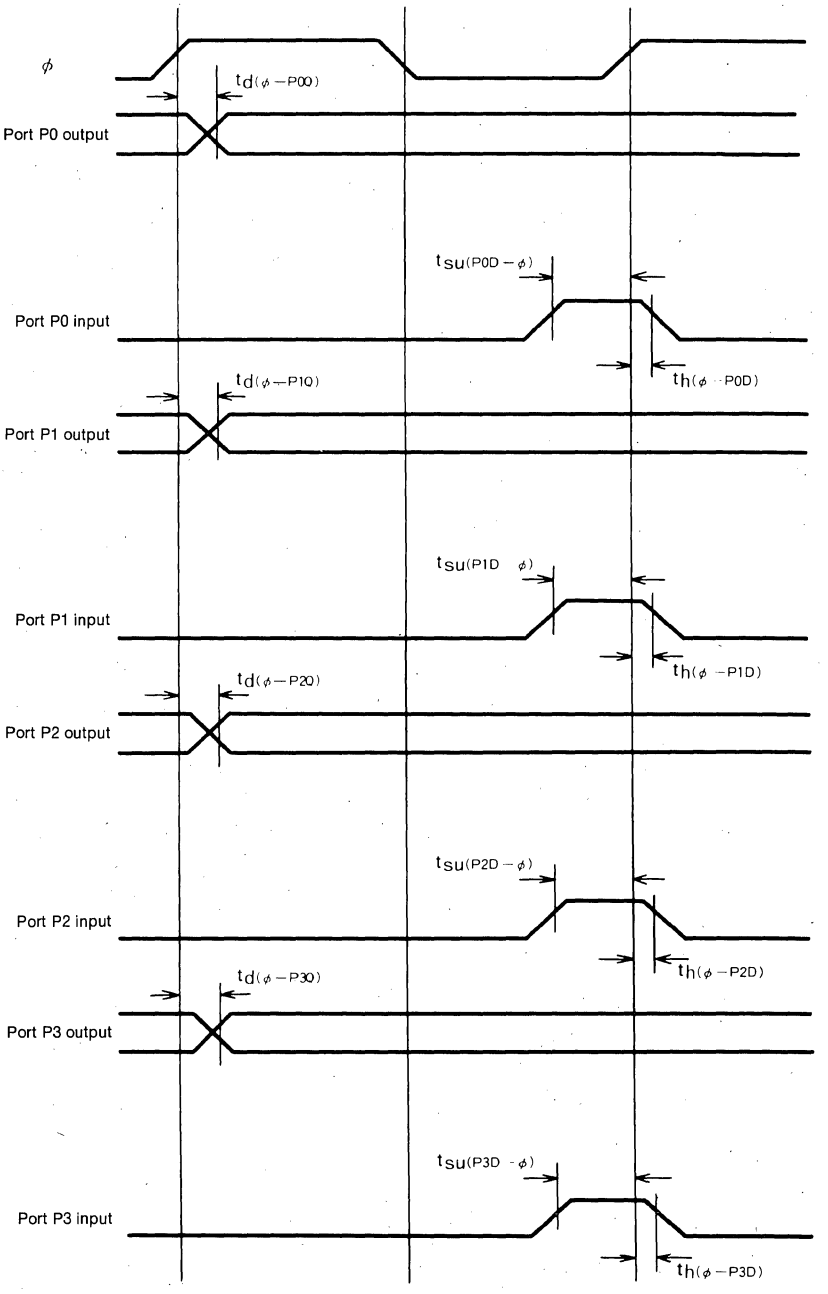


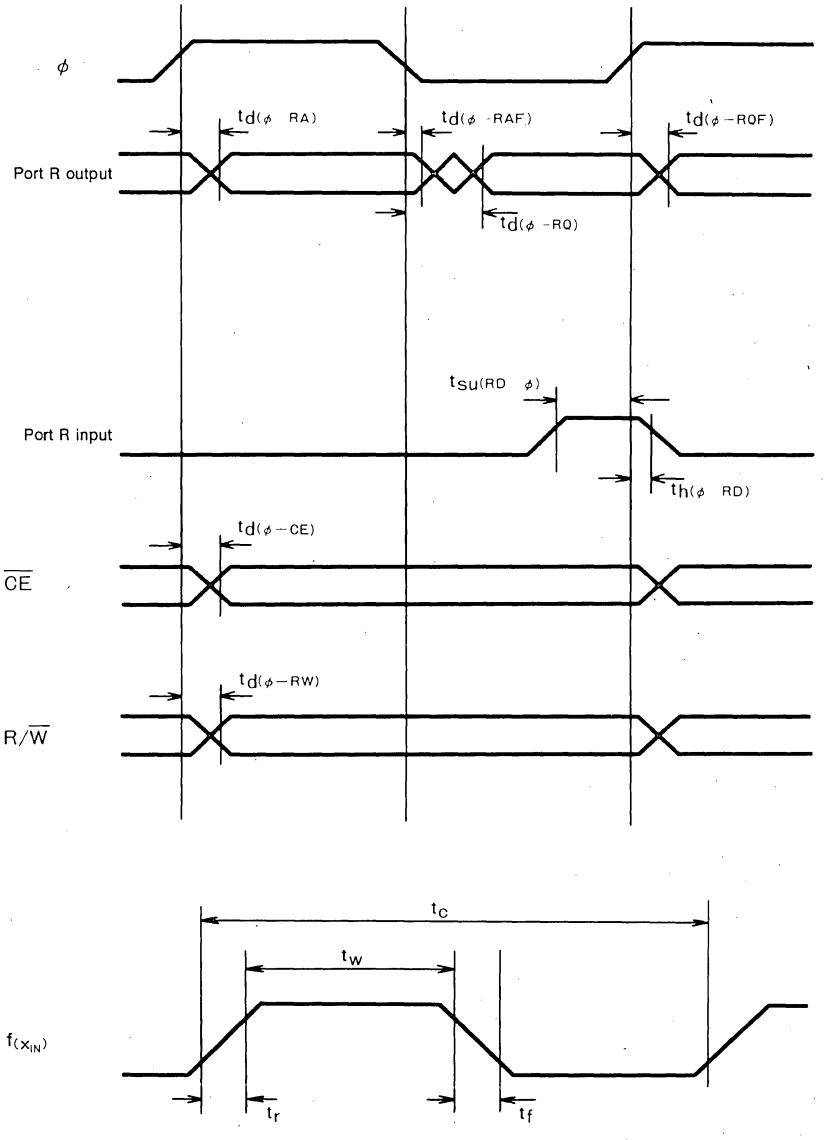
Fig.19 $\overline{CE}$ and R/$\overline{W}$ test circuit

TIMING DIAGRAMS

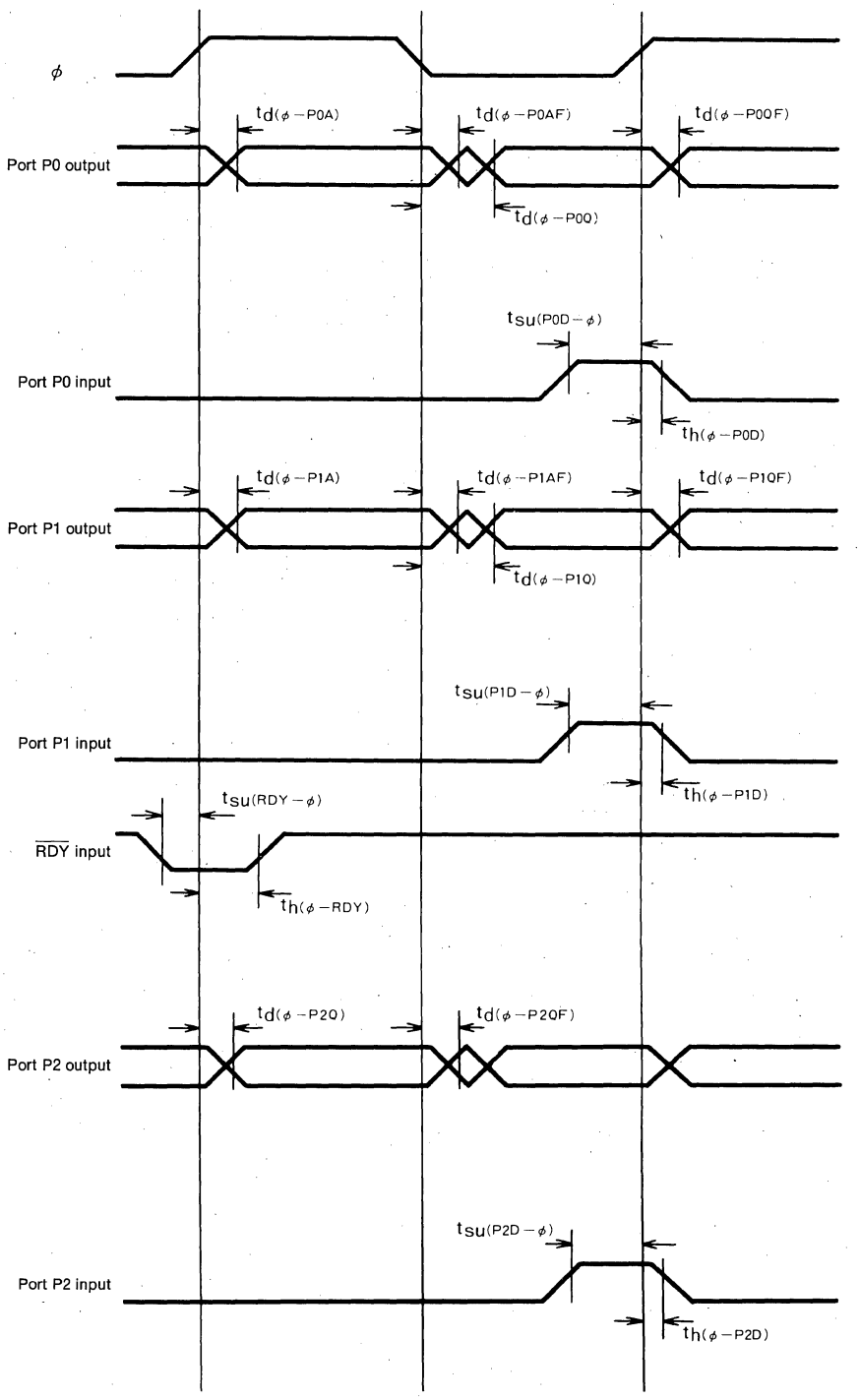
In single-chip mode



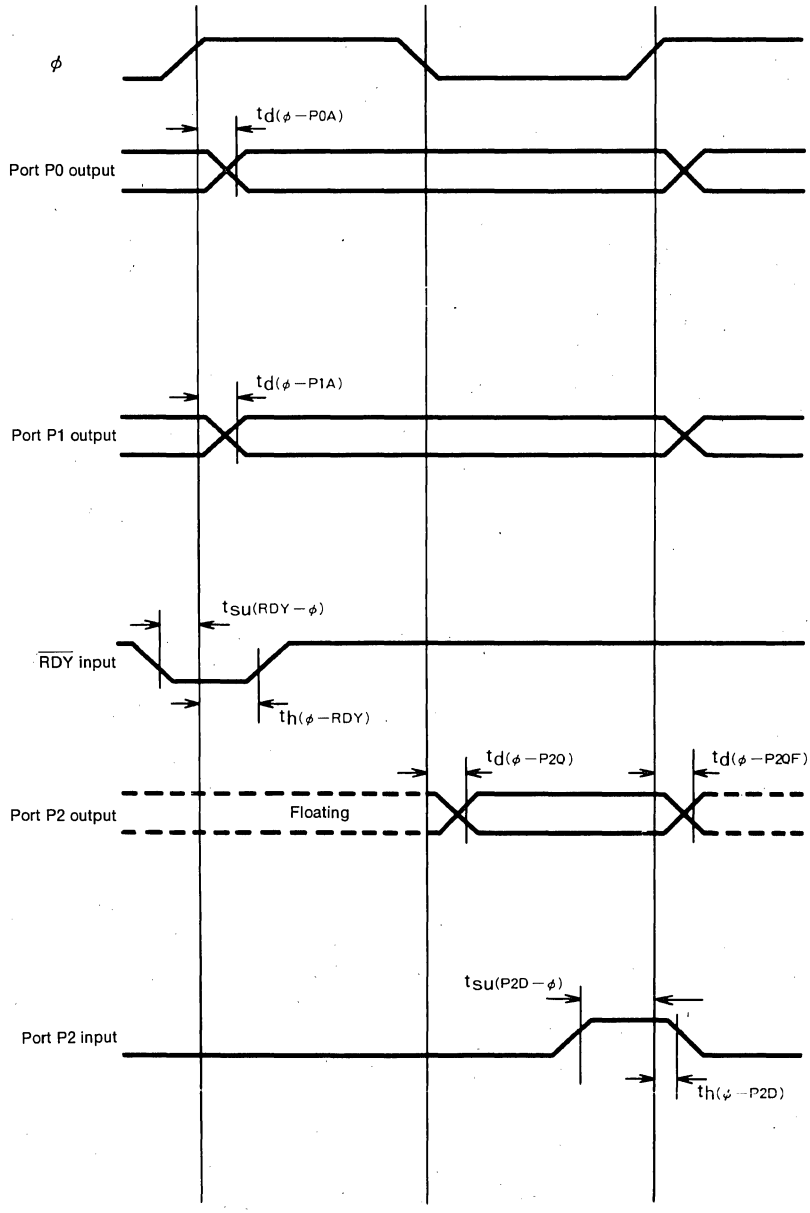
In single-chip mode (continued from the preceding page)



In memory expanding mode and eva-chip mode



In microprocessor mode



M50742-XXXSP/FP
M50708-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50742-XXXSP and the M50708-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. Both are housed in a 64-pin shrink plastic molded DIP (flat package type also available). These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50742-XXXSP and the M50708-XXXSP are noted below. The following explanations apply to the M50742-XXXSP. Specification variations for other chips are noted accordingly.

Type name	ROM size
M50742-XXXSP	4096bytes
M50708-XXXSP	6144bytes

The differences between the M50742-XXXSP and the M50742-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

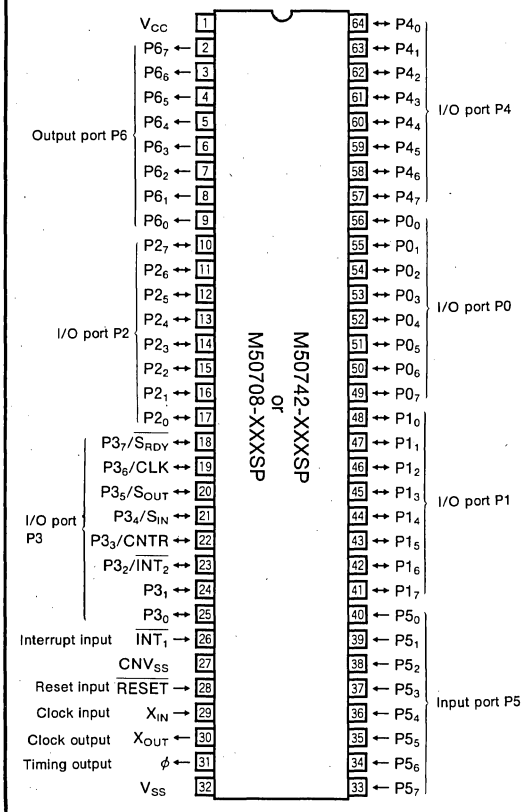
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM 4096bytes (M50742-XXXSP)
  6144bytes (M50708-XXXSP)
  RAM 128bytes
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz ..... 5V$\pm$10%
- Power dissipation
  normal operation mode (at 4MHz frequency)
  ..... 15mW (V_{CC}=5V, Typ.)
- Subroutine nesting ..... 64 levels (Max.)
- Interrupt ..... 7 types, 5 vecters
- 8-bit timer ..... 3 (2 when used as serial I/O)
- Programmable I/O (Ports P0, P1, P2, P3, P4) 40
- Input port (Port P5) 8
- Output port (Port P6) 8
- Serial I/O(8-bit) 1

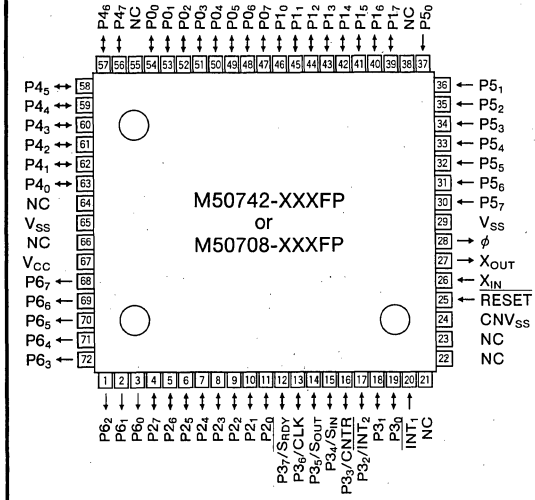
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

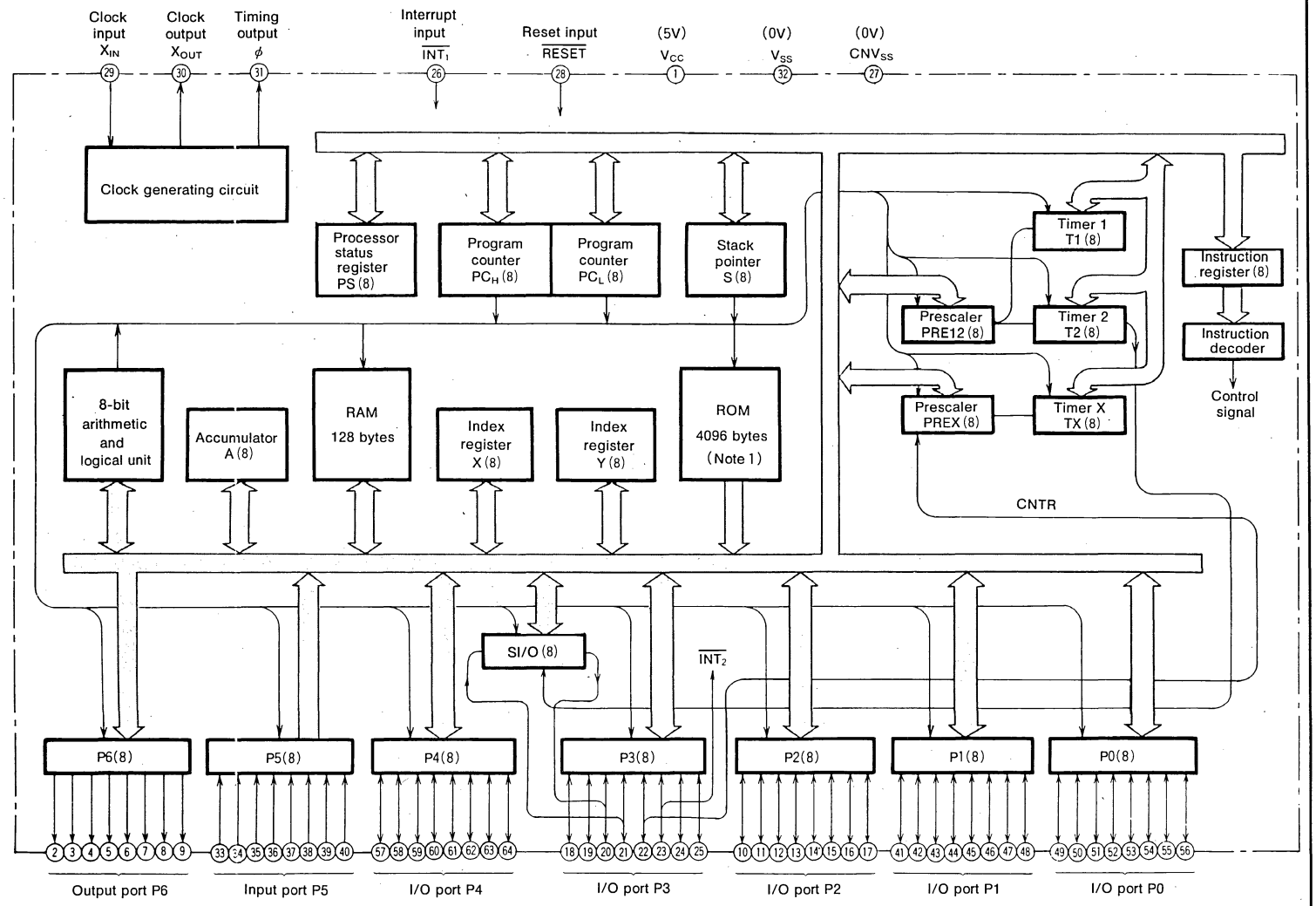


Outline 72P6

NC : No connection

MITSUBISHI ELECTRIC

M50742-XXXSP BLOCK DIAGRAM



Note 1 : 6144 bytes for M50708-XXXSP

FUNCTIONS OF M50742-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency)
Memory size	ROM		4096bytes (6144bytes for M50708-XXXSP)
	RAM		128bytes
Input/output port	$\overline{INT_1}$	Input	1-bit×1
	P0, P1, P2, P3, P4	I/O	8-bit×5 (part of P3 are in common with serial I/O)
	P5	Input	8-bit×1
	P6	Output	8-bit×1
Serial I/O			8-bit×1
Timers			8-bit prescaler×2+8-bit timer×3 (8-bit timer×2 when serial I/O is used)
Subroutine nesting			64 levels (max.)
Interrupts			Two external interrupts (1 of external interrupt is in common with port $P3_2$) Three timer interrupts (or timer×2, serial I/O×1)
Clock generating circuit			Built-in (ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	At high-speed mode		15mW (at 4MHz frequency)
Input/output characteristics	Input/output voltage		9V (Ports P0, P1, P2, P3, P4, P5, P6, $\overline{INT_1}$)
	Output current		5mA (Ports P0, P1, P2, P3, P4, P6)
Memory expansion			Possible
Operating temperature range			−10∼70℃
Device structure			CMOS silicon gate process
Package	M50742-XXXSP, M50708-XXXSP		64-pin shrink plastic molded DIP
	M50742-XXXFP, M50708-XXXFP		72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an I/O pin for the timer X.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest order interrupt input pin ($\overline{INT_2}$), respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is P-channel open drain.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
$P6_0$~$P6_7$	Output port P6	Output	Port P6 is an 8-bit output port. The output structure is N-channel open drain.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50742-XXXSP is shown in Figure 1. Addresses $F000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 4096 bytes.

Addresses $E800_{16}$ to $FFFF_{16}$ are the ROM address area assigned to the M50708-XXXSP.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $007F_{16}$ are assigned to the built-in RAM and consist of 128 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

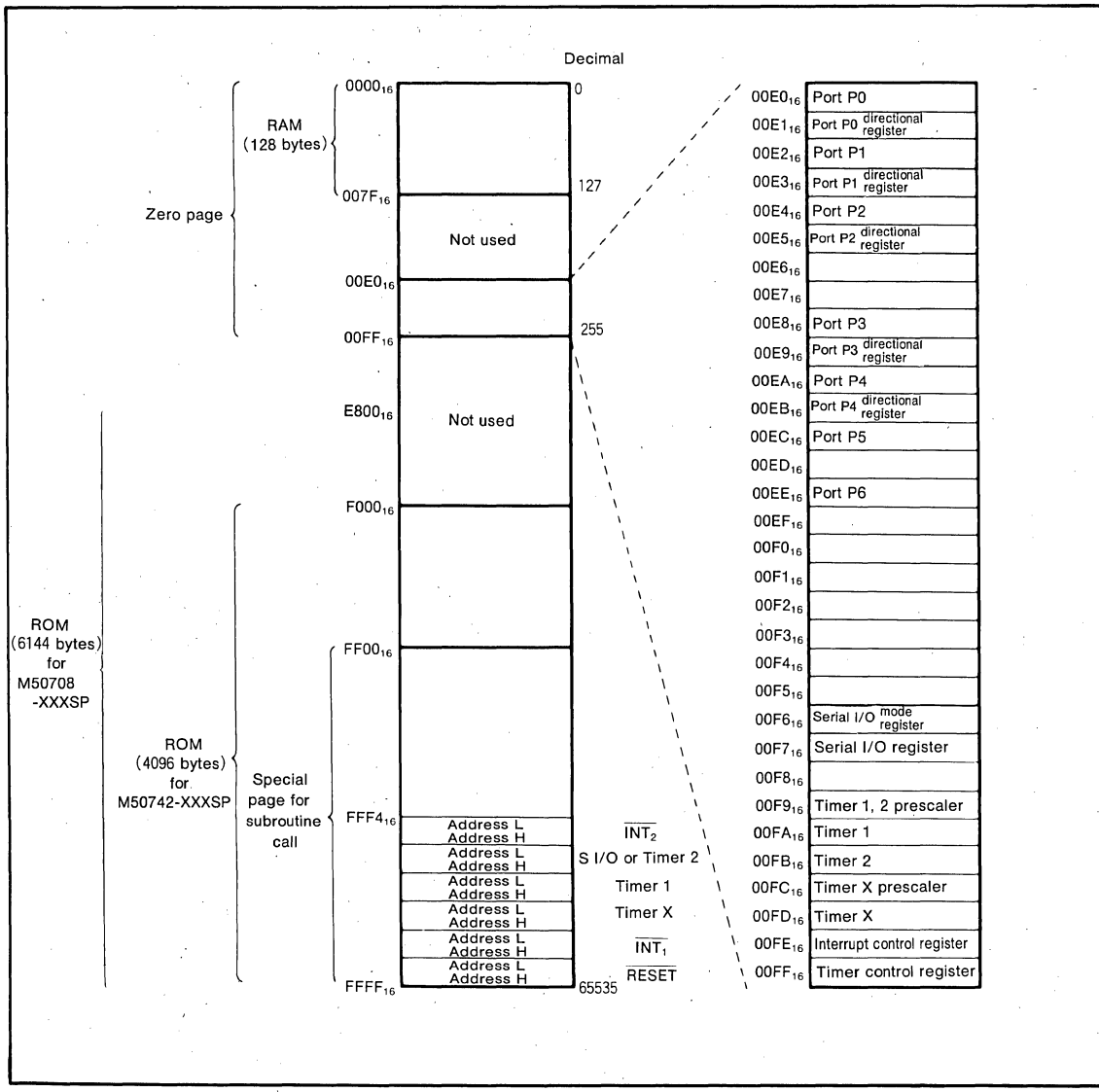


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

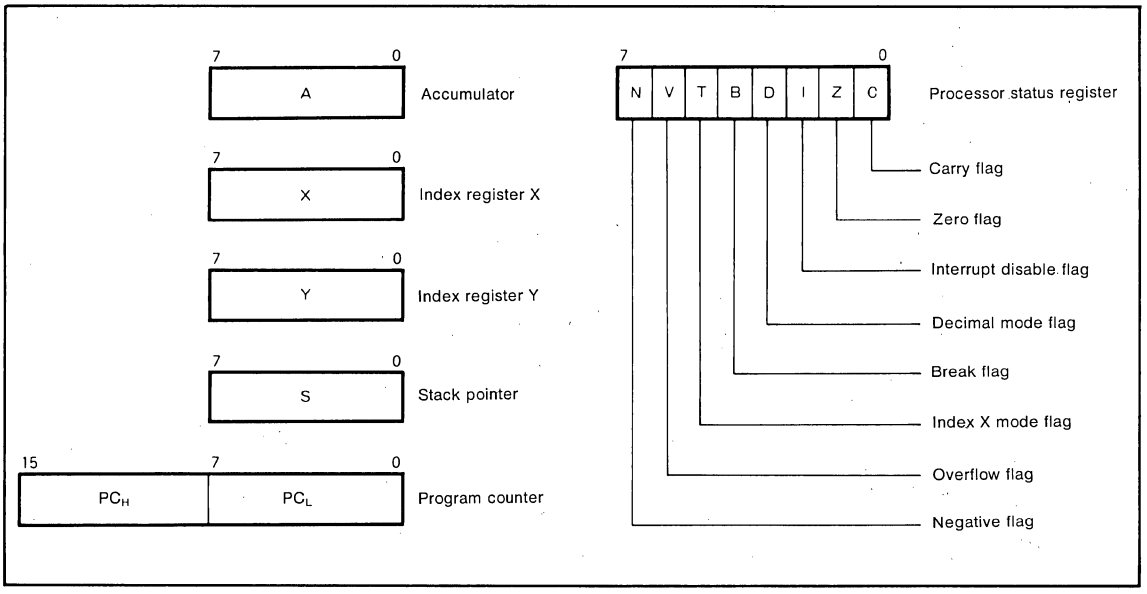


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The location of the stack can be determined by the stack page bit (bit 4 at address $00FF_{16}$). When bit 4 is "0" and the contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When bit 4 is "1", the stack address is set to $01XX_{16}$. When using this microcomputer in the single-chip mode, the stack page bit must be "0" and the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{\text{INT}_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1	4	$FFF9_{16}$, $FFF8_{16}$
Timer 2 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{\text{INT}_2}$ (BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50742-XXXSP can be interrupted from seven souces; $\overline{\text{INT}_1}$, timer X, timer 1, timer 2/serial I/O, or $\overline{\text{INT}_2}$/BRK instruction.

However, the $\overline{\text{INT}_2}$ pin is used with port $P3_2$ and the corresponding directional register bit should be set to "0" when $P3_2$ is used as an interrupt input pin.

The value of bit 2 of the serial I/O mode register (address $00F6_{16}$) determine whether the interrupt is from timer 2 or from serial I/O. When bit 2 is "0" the interrupt is from timer 3, and when bit 2 is "1" the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and

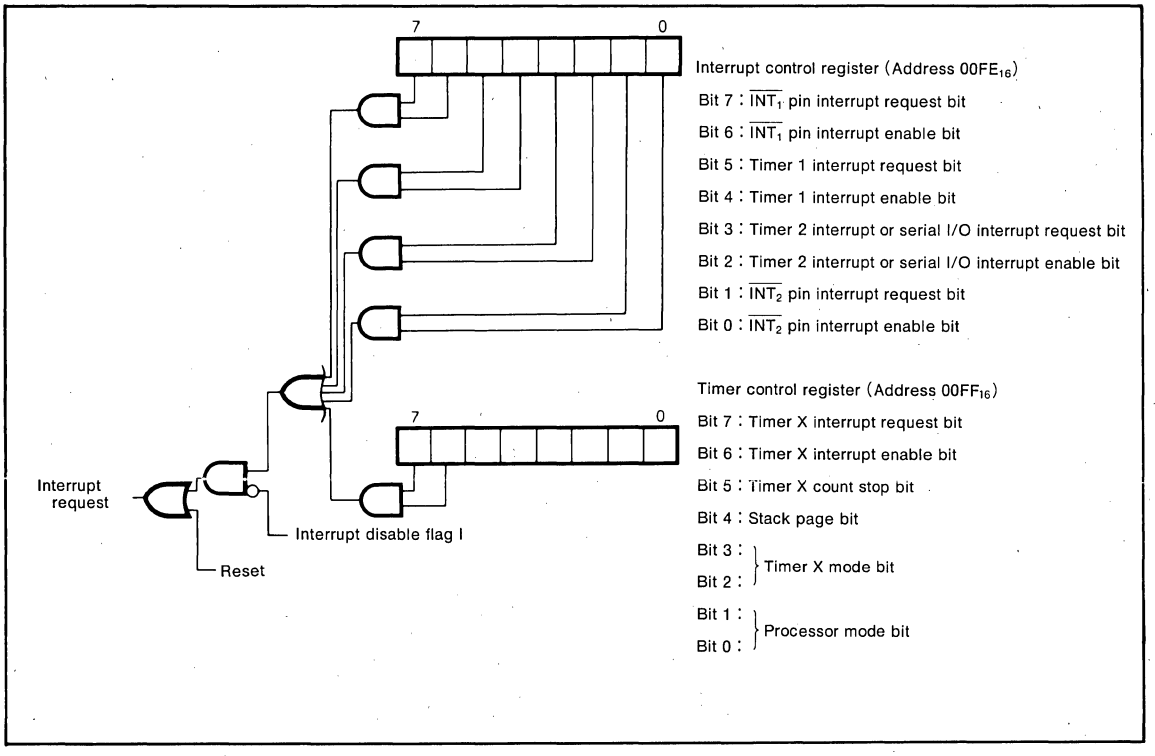


Fig.3 Interrupt control

the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"

(2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

TIMER

The M50742-XXXSP has three timers; timer X, timer 1, and timer 2. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section). Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1 and timer 2 is shown in Figure 4.

The $P3_3$/CNTR pin cannot be used as CNTR when $P3_3$ is being used in the normal I/O mode.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency di-

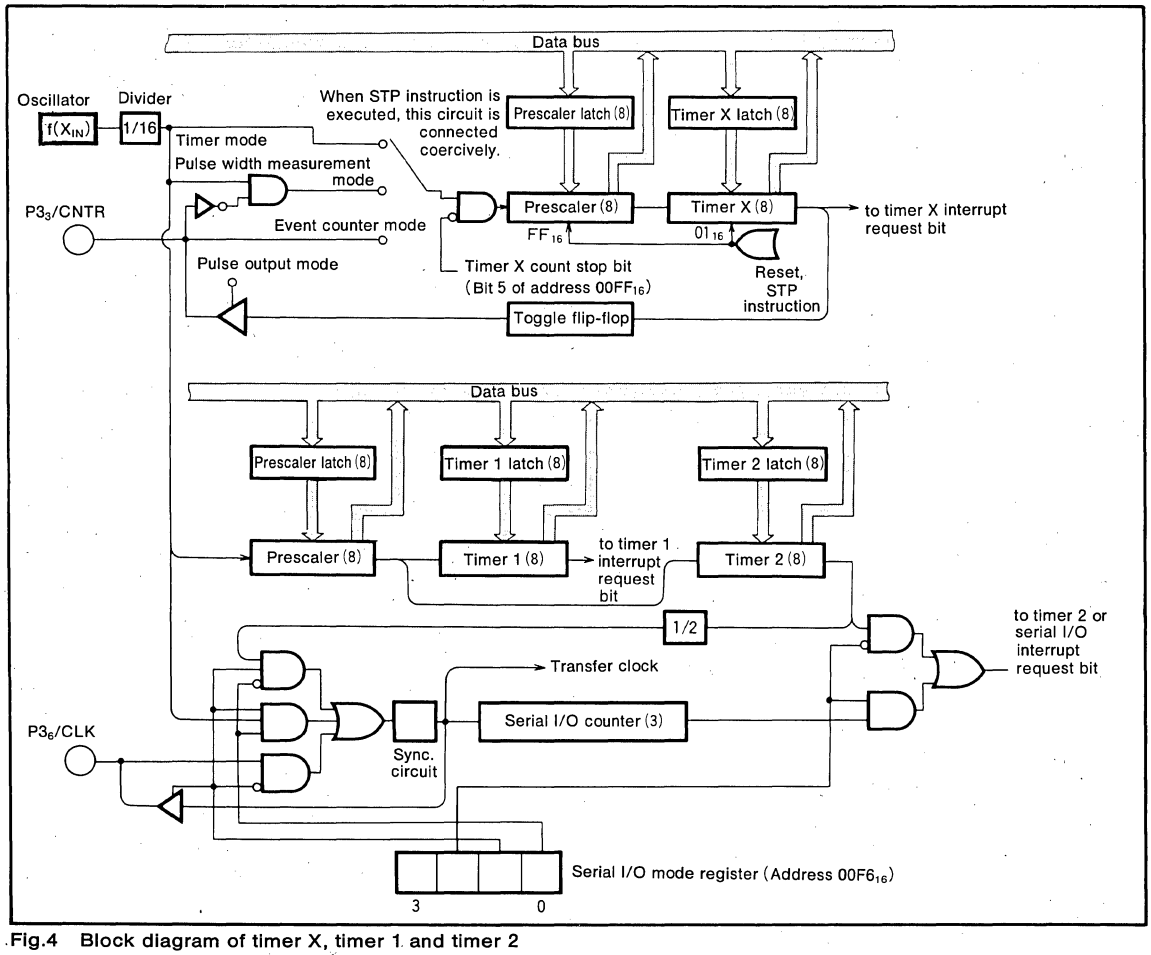


Fig.4 Block diagram of timer X, timer 1 and timer 2

vider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section). The prescaler latch and timer latch can be loaded with any number except zero.

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock sourse.

(4) Pulse width measurement mode [11]
This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

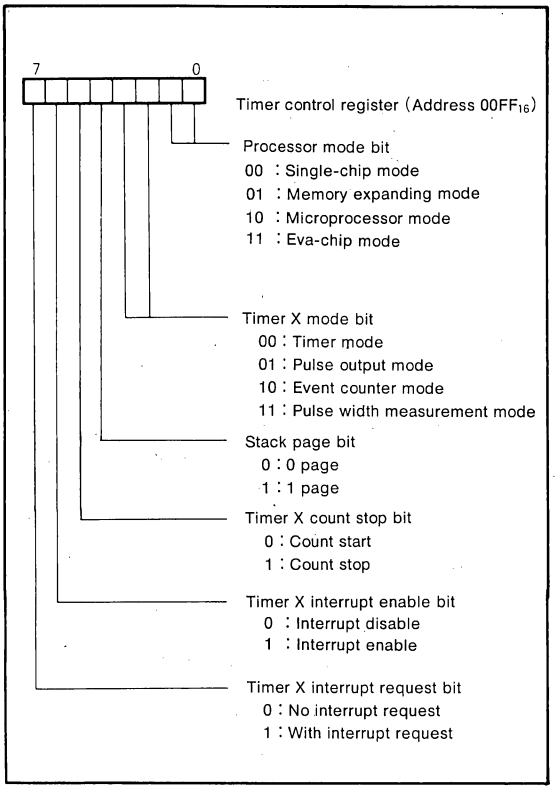


Fig.5 Structure of timer control register

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 6.

In the serial I/O mode the receive raady signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O pins (S_{OUT}, S_{IN}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F6_{16}$) is 4-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 2, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], oscillator frequency divided by 16, becomes the clock.

Bit 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is a "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 2. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (Bit 3=1, $\overline{S_{RDY}}$) or used as normal I/O pin (Bit 3=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

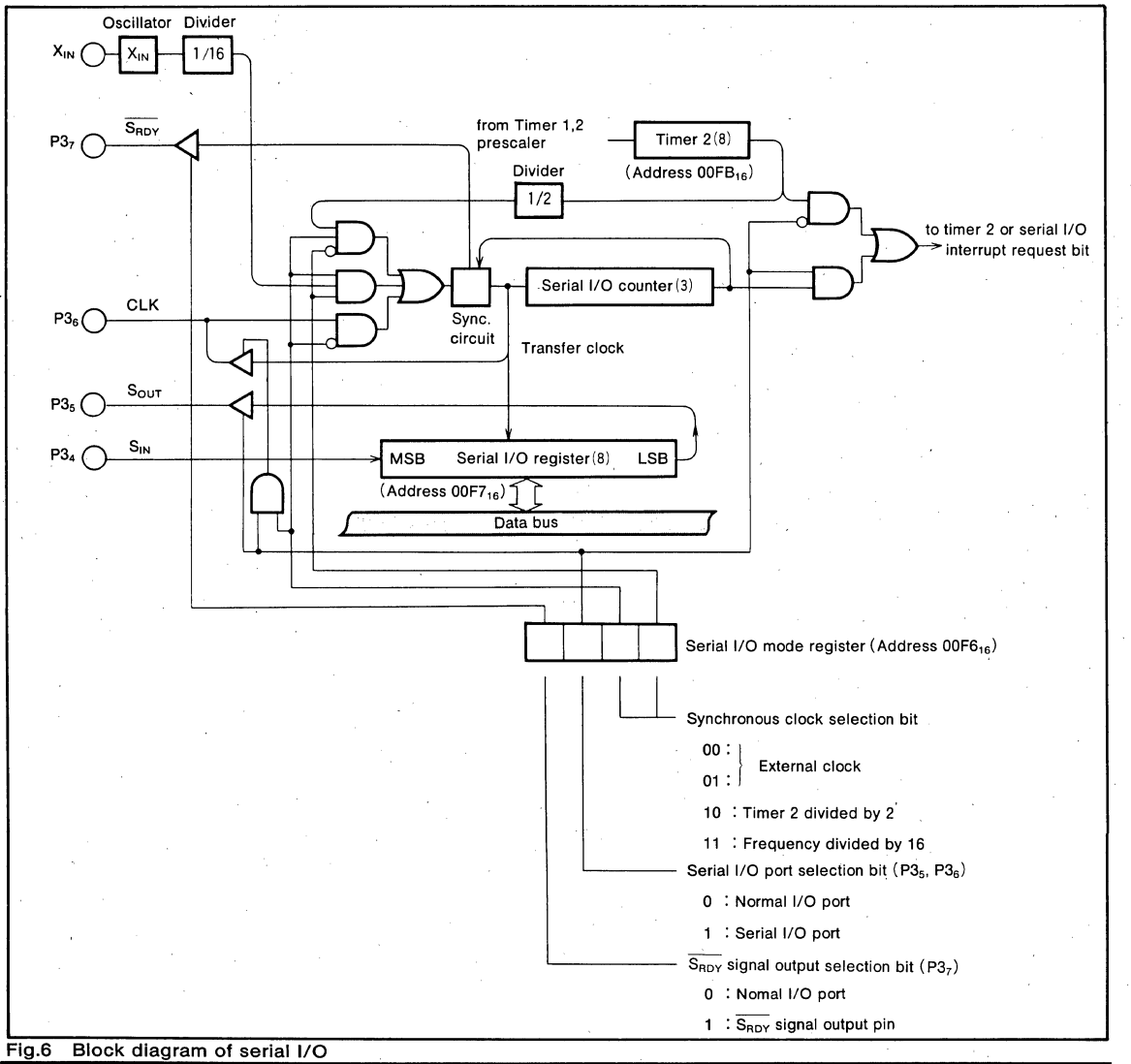


Fig.6 Block diagram of serial I/O

Internal Clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address $00F7_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50742-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit.
Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrpt request bit will be set.

External Clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.
Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 7. An example of communication between two M50742-XXXSPs is shown in Figur 8.

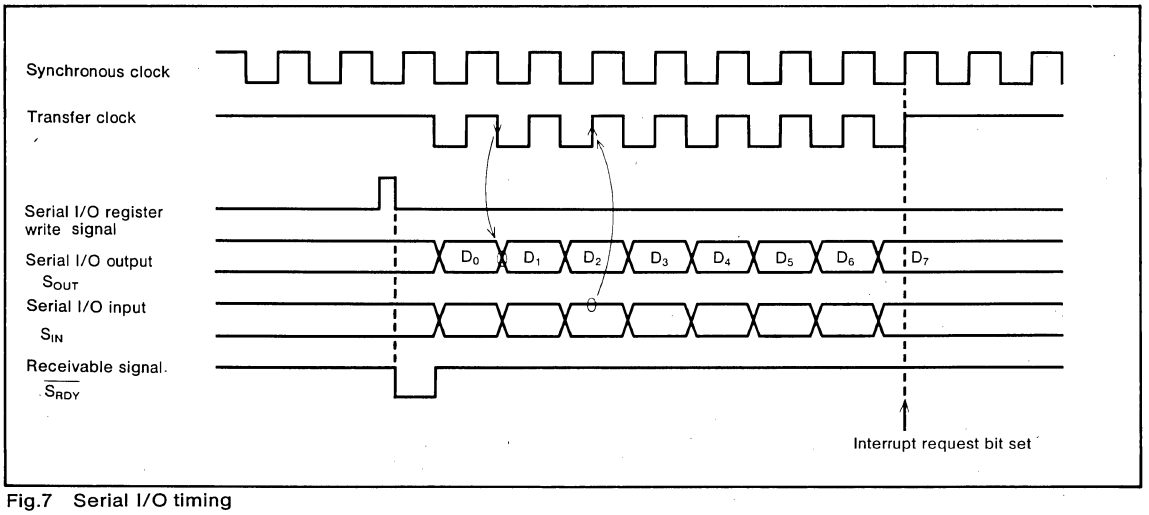


Fig.7 Serial I/O timing

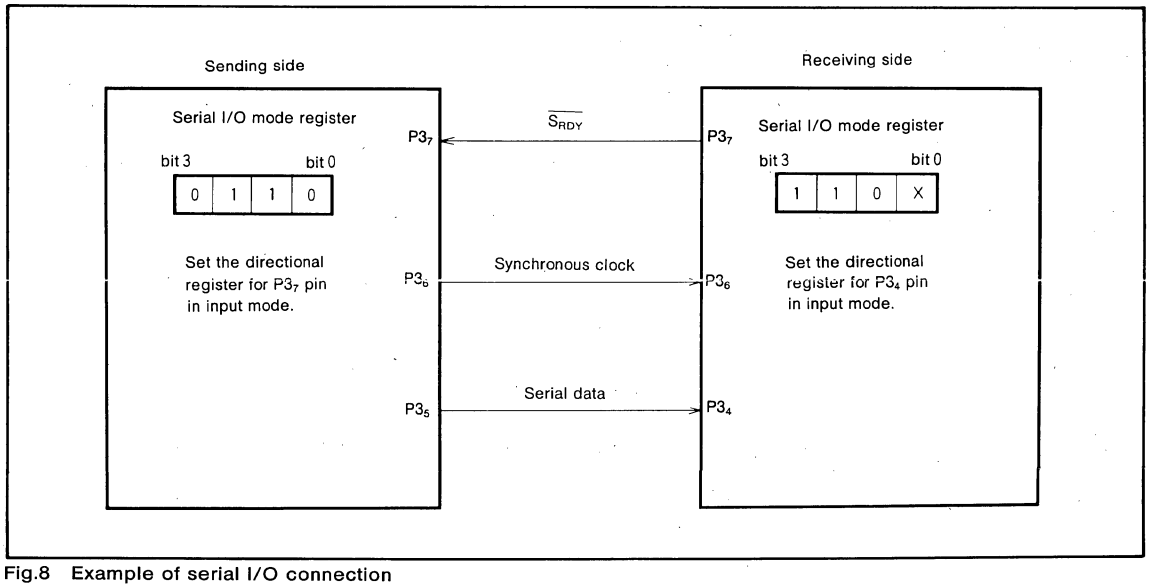


Fig.8 Example of serial I/O connection

RESET CIRCUIT

The M50742-XXXSP is reset according to the sequence shown in Figure 9. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 10.

An example of the reset circuit is shown in Figure 11.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

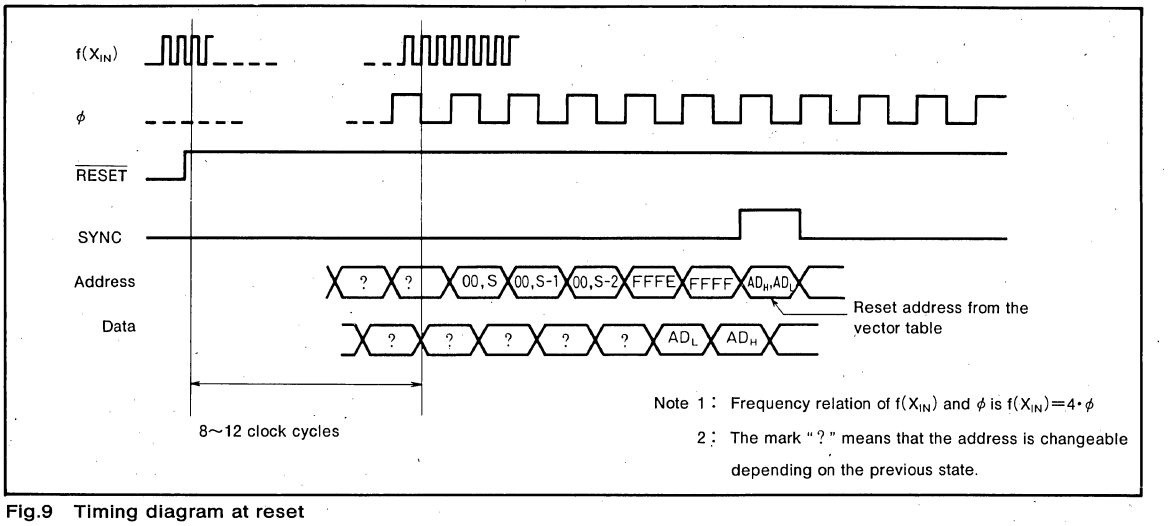


Fig.9 Timing diagram at reset

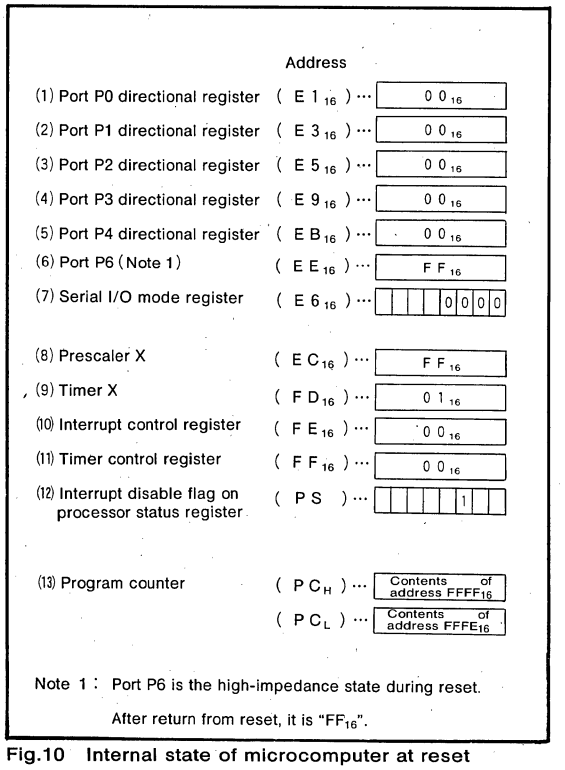


Fig.10 Internal state of microcomputer at reset

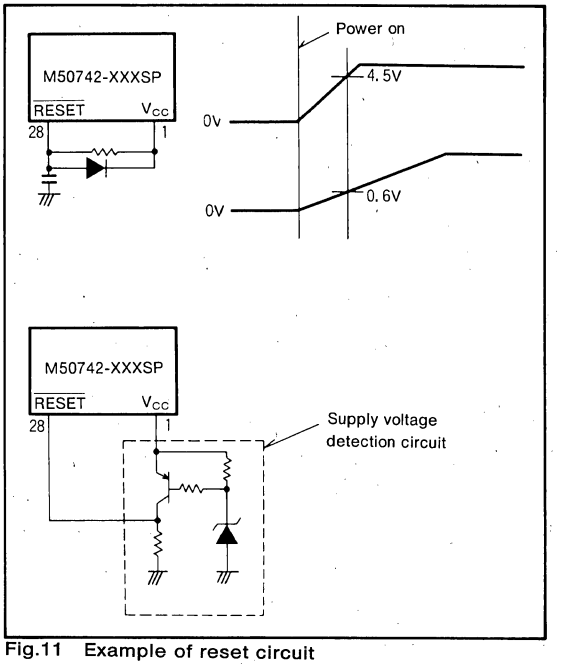


Fig.11 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

Pull-up transistor can be specified as an option. As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as serial I/O, $\overline{INT_2}$ and I/O pins for timer X. For more details, see the processor mode information.

(5) Port P4

Port P4 is an 8-bit I/O port with P-channel open drain outputs. This port also has the pull-down transistor option.

(6) Port P5

Port P5 is and input port with pull-up transistor option.

(7) Port P6

Port P6 is an output port. It has N-channel open drain output with pull-up transistor option. See Figure 12 for more details.

(8) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ.

(9) $\overline{INT_1}$ pin

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

(10) $\overline{INT_2}$ pin ($P3_2/\overline{INT_2}$ pin)

The $\overline{INT_2}$ pin is an interrupt input pin used with $P3_2$. To use this pin as an interrupt pin, set the corresponding bit in the directional register to input ("0"). When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1".

(11) CNTR pin ($P3_3$/CNTR pin)

The $P3_3$/CNTR pin is an I/O pin of timer X. To use this pin as the timer X input pin, set the corresponding directional register bit to input ("0"). In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

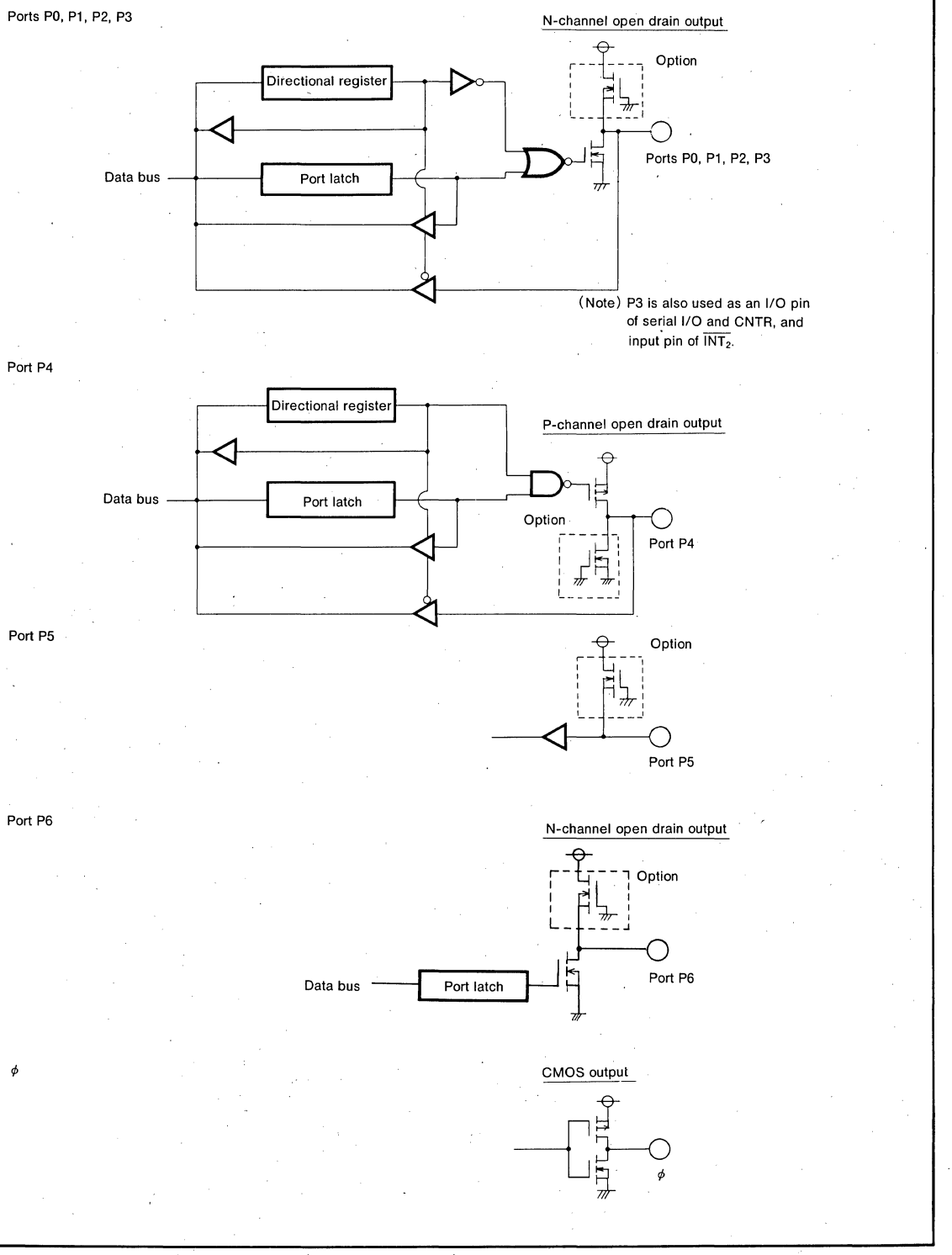


Fig.12 Block diagram of ports P0~P6 (single-chip mode) and output format of φ

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 14 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 13.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

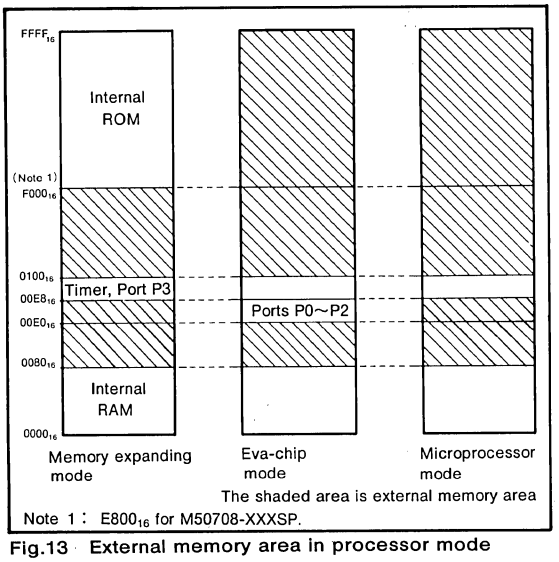


Fig.13 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost. Port P2 becomes the data bus of D_7～D_0 (including instruction code) and loses its nomal I/O functions. $P3_2$ of port P3 becomes the input port. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively when ϕ enters into the "H" state. Port $P3_2$ functions as an input port during this same transition.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode.

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the databus (D_7～D_0) and loses its normal I/O functions. Port $P3_1$ and $P3_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is requierd.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_2$, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

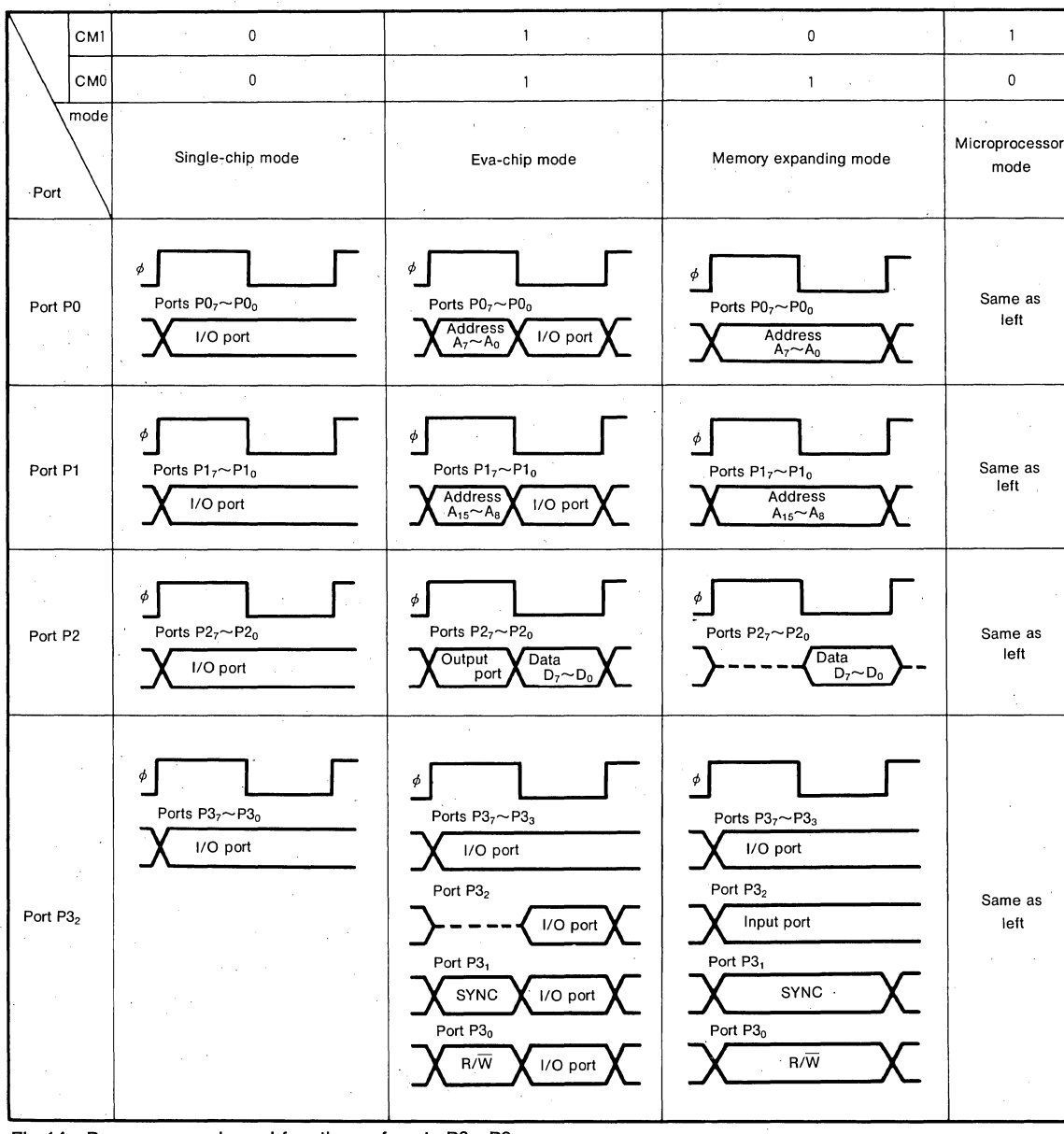


Fig.14 Processor mode and functions of ports P0~P3

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 17.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleard when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 15.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

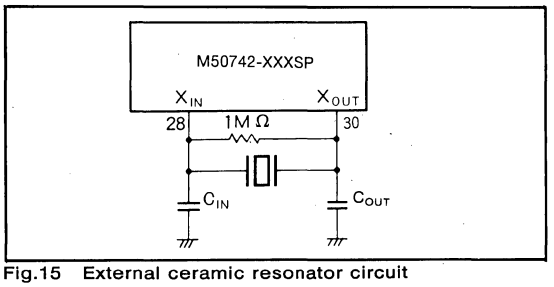


Fig.15 External ceramic resonator circuit

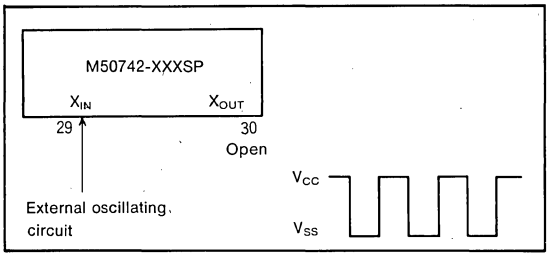


Fig.16 External clock input circuit

The example of external clock uasge is shown in Figure 16. X_{IN} is the input, and X_{OUT} is open.

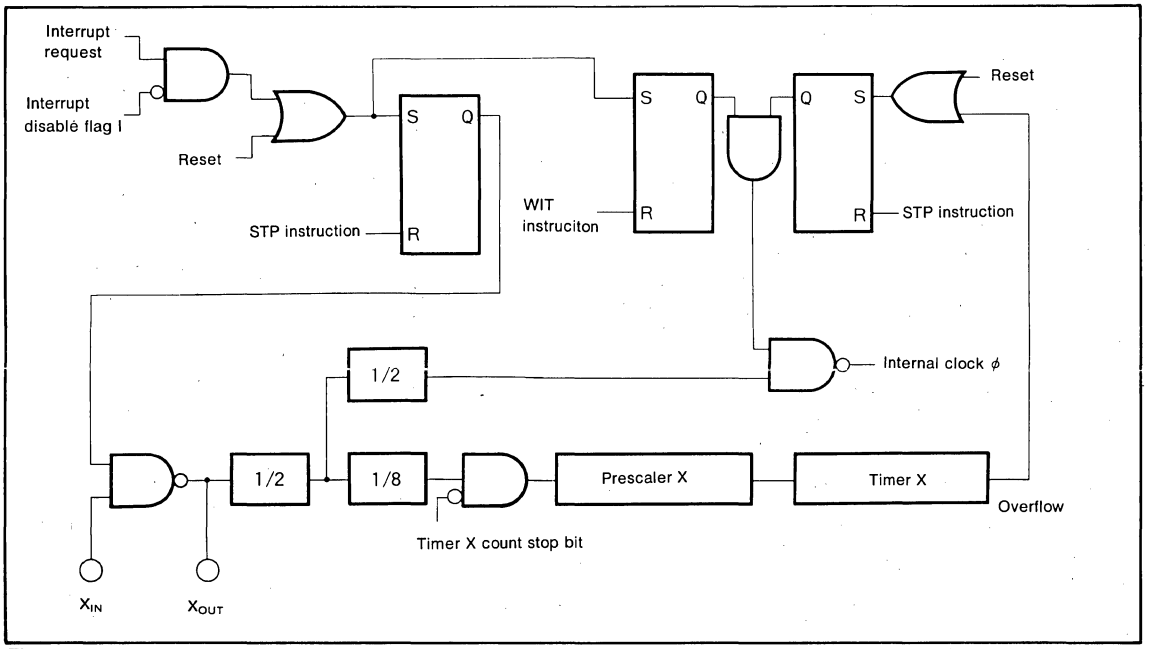


Fig.17 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(5) A NOP instruction must be used after the execution of a PLP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) Mask ROM confirmation form
(2) Mark specification form
(3) ROM data ..... EPROM 3sets

Write the following option on the mask ROM confirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port P4 pull-down transistor bit
- Port P5 pull-up transistor bit
- Port P6 pull-up transistor bit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors are at "off" state.	−0.3∼7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}		−0.3∼7	V
V_I	Input voltage, $P4_0$∼$P4_7$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, CNTR, $\overline{INT_1}$		−0.3∼11	V
V_I	Input voltage, CNV_{SS}		−0.3∼13	V
V_O	Output voltage, $P4_0$∼$P4_7$, X_{OUT}, ϕ		−0.3∼V_{CC}+0.3	V
V_O	Output voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P6_0$∼$P6_7$		−0.3∼11	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
T_{opr}	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5V±10%, T_a = −10∼70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P6_0$∼$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P6_0$∼$P6_7$ (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current, $P4_0$∼$P4_7$			−10	mA
$I_{OH(avg)}$	"H" average output current, $P4_0$∼$P4_7$ (Note 2)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

Note 2 : $I_{OL(avg)}$, $I_{OH(avg)}$ is the average current in 100ms.
3 : The total of $I_{OL(peak)}$ of P0, P1, P2, P3, P6 should be 80mA max, and the total of $I_{OH(peak)}$ of P4 should be 80mA max.
4 : "H" input voltage of ports P0, P1, P2, P3, P5 and $\overline{INT_1}$ is available up to + 9 V. (For ports, it is only when pull-up transistor is omitted.)

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage, $P4_0$~$P4_7$	I_{OH} = −10mA		3			V
V_{OH}	"H" output voltage, ϕ	I_{OH} = −2.5mA		3			V
V_{OL}	"L" output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P6_0$~$P6_7$	I_{OL} = 10mA				2	V
V_{OL}	"L" output voltage, ϕ	I_{OL} = 5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_6$	When used as CLK input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{INT_1}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_2$	When used as $\overline{INT_2}$ input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_3$	When used as CNTR input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis, X_{IN}			0.1		0.5	V
I_{IL}	"L" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	V_I = 0V without pull-up transistor				−5	μA
I_{IL}	"L" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	V_I = 0V with pull-up transistor		−40	−70	−125	μA
I_{IL}	"L" input current, $P4_0$~$P4_7$	V_I = 0V				−5	μA
I_{IL}	"L" input current, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 0V				−5	μA
I_{IH}	"H" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	V_I = 9V without pull-up transistor				9	μA
I_{IH}	"H" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	V_I = 5V with pull-up transistor				5	μA
I_{IH}	"H" input current, $P4_0$~$P4_7$	V_I = 5V without pull-down transistor				5	μA
I_{IH}	"H" input current, $P4_0$~$P4_7$	V_I = 5V with pull-down transistor		40	70	125	μA
I_{IH}	"H" input current, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 5V				5	μA
V_{RAM}	RAM retention voltage	At clock stop		2			V
I_{CC}	Supply current	P-channel open-drain output pins are to V_{CC}, output pins are open, other I/O pins are connected to V_{SS}.	$f_{(X_{IN})}$ = 4MHz square wave		3	6	mA
			T_a = 25℃ At clock stop			1	μA
			T_a = 70℃ At clock stop			10	μA

TIMING REQUIREMENTS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	270			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time	20			ns
t_c	External clock input cycle time	250			ns
t_w	External clock input pulse width	75			ns
t_r	External clock rising edge			25	ns
t_f	External clock falling edge			25	ns

Eva-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Memory expanding mode and microprocessor mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.18			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time	Fig.19			230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time	Fig.18			230	ns

Eva-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.18			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_2Q)}$	Port $P3_2$ data output delay time				200	ns
$t_{d(\phi-P3_2QF)}$	Port $P3_2$ data output delay time				200	ns

Memory expanding mode and microprocessor mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.18			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

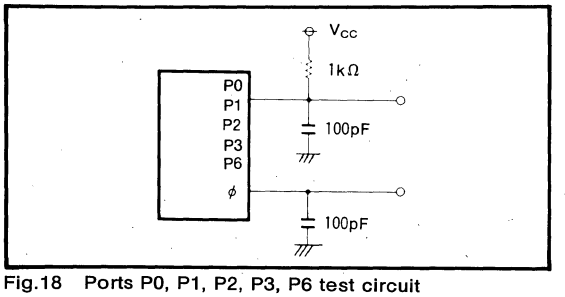


Fig.18 Ports P0, P1, P2, P3, P6 test circuit

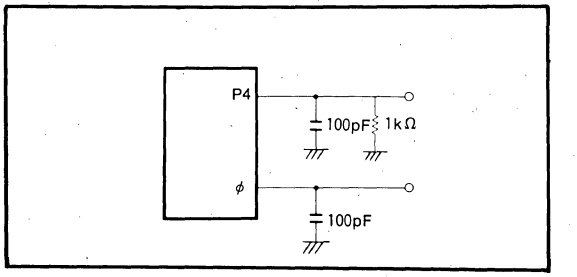
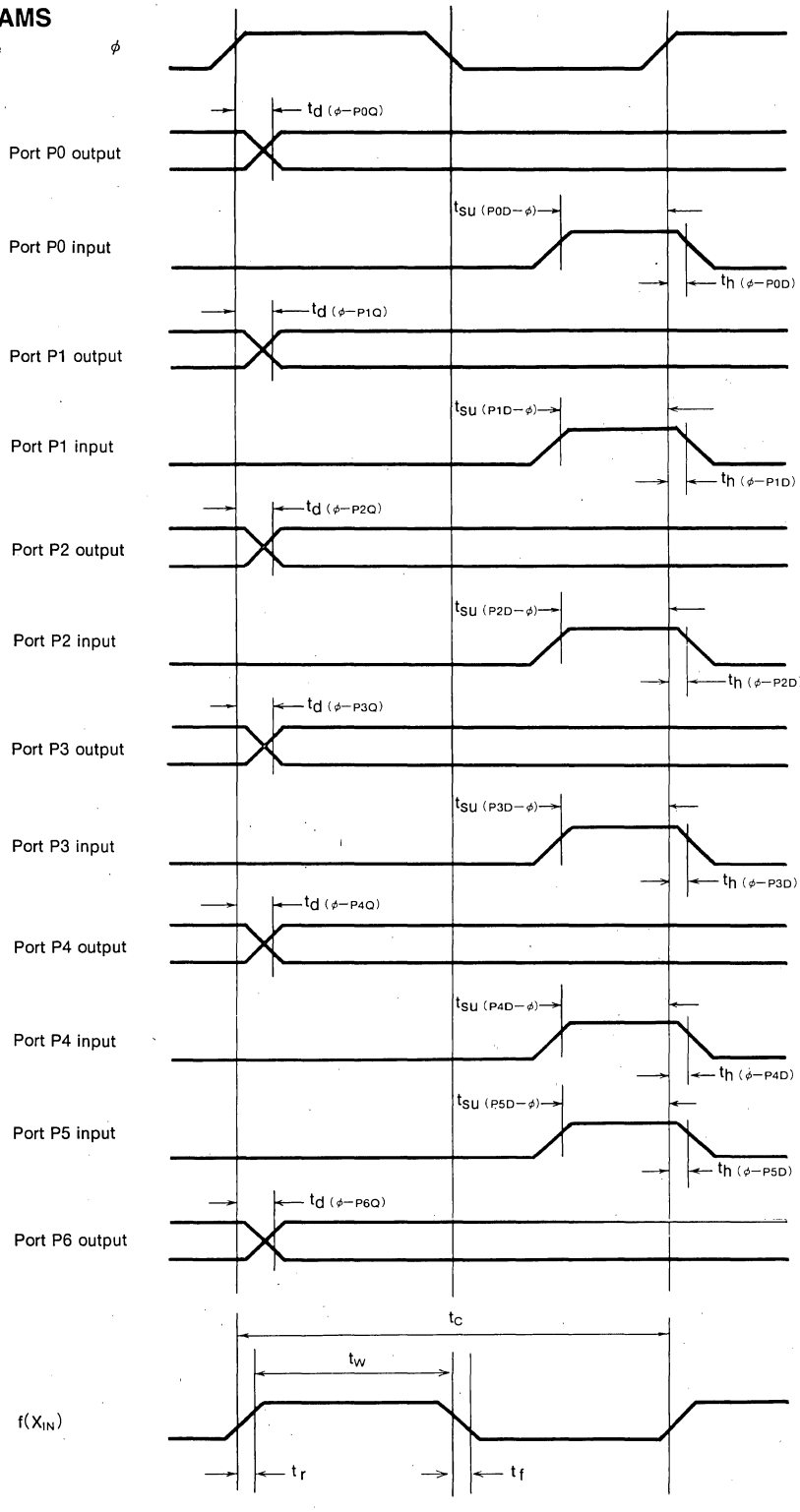


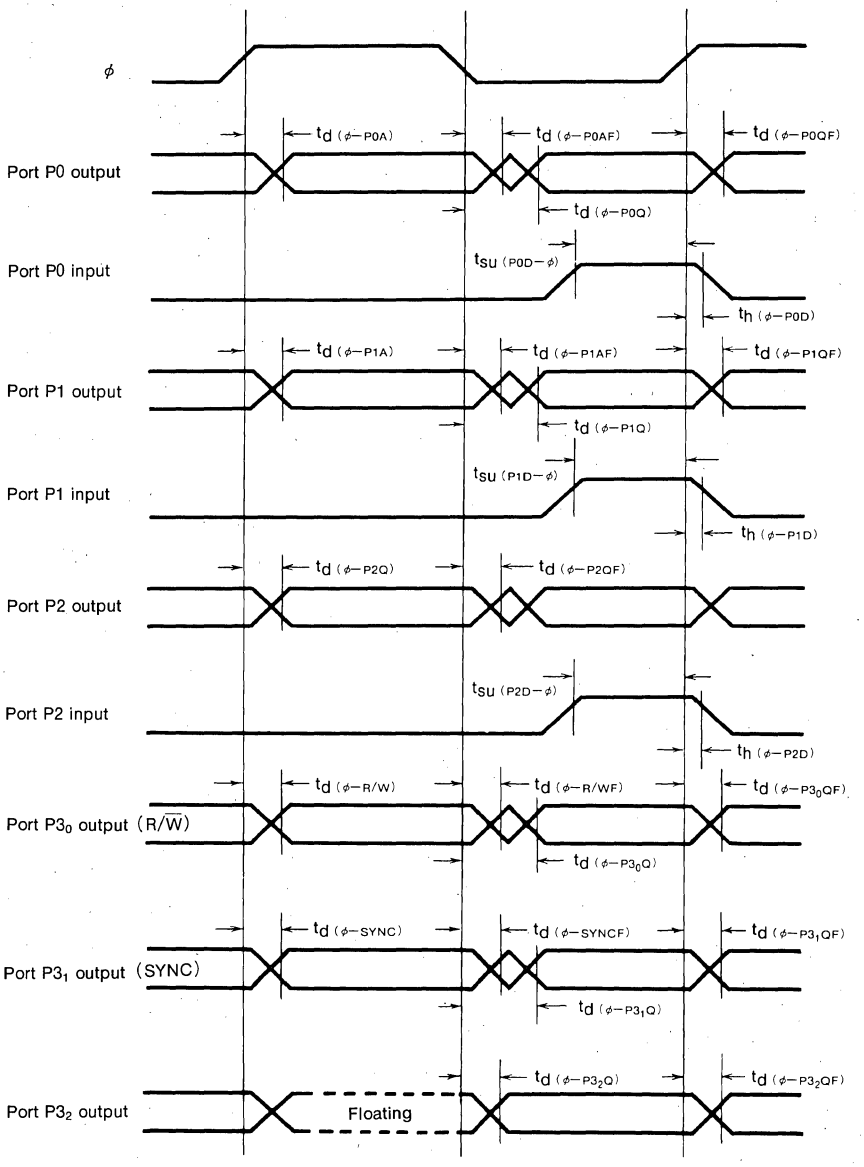
Fig.19 Port P4 test circuit

TIMING DIAGRAMS

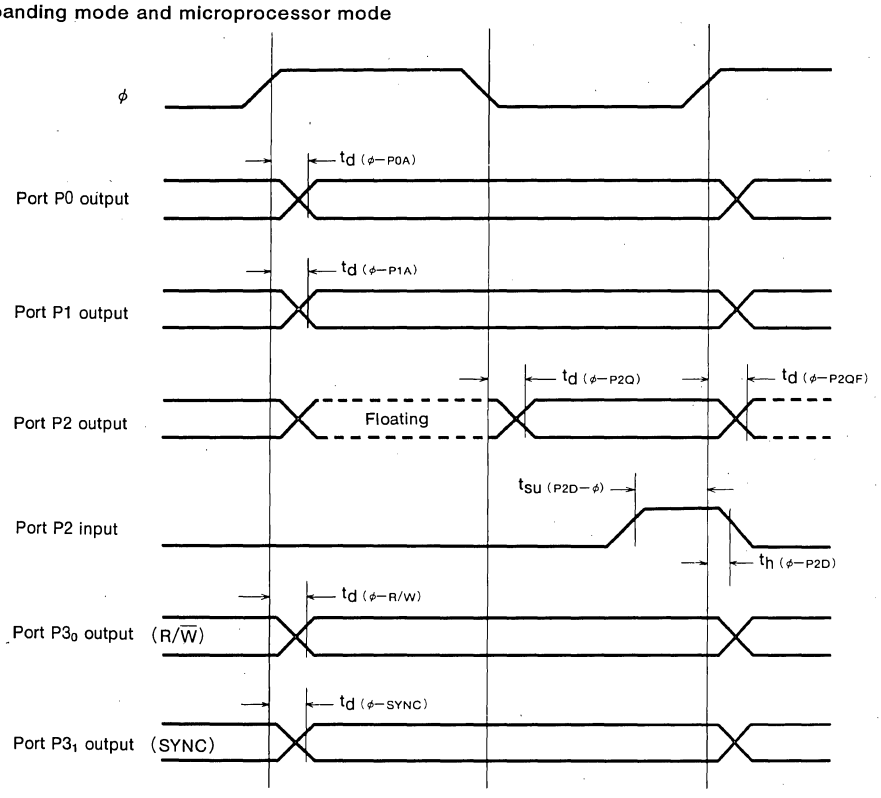
In single-chip mode



In eva-chip mode



In memory expanding mode and microprocessor mode



M50743-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50743-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP (flat package type also available). This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50743-XXXSP and the M50743-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

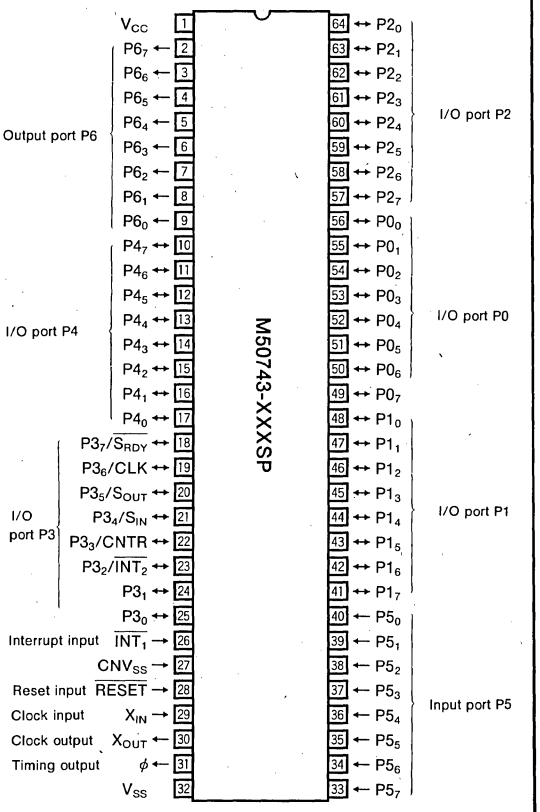
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM 4096bytes
  RAM 128bytes
- Instruction execution time
  ..... 1μs (minimum instructions at 8MHz frequency)
- Single power supply f(X_{IN})=8MHz ..... 5V±10%
- Power dissipation
  normal operation mode (at 8MHz frequency) 30mW
- Subroutine nesting ..... 64 levels (Max.)
- Interrupt ..... 7 types, 5 vecters
- 8-bit timer ..... 3 (2 when used as serial I/O)
- Programmable I/O (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Output ports (Port P6) 8
- Serial I/O (8-bit) 1

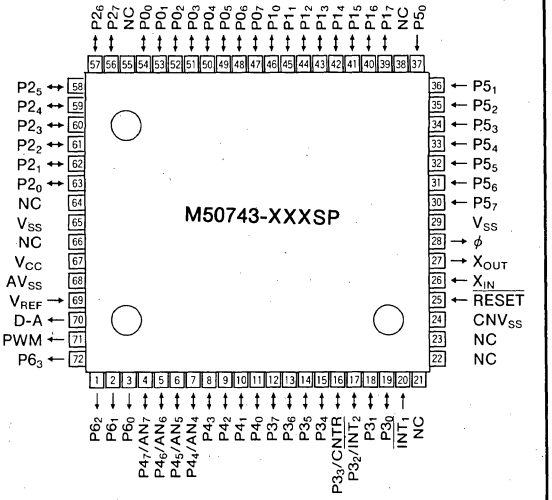
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



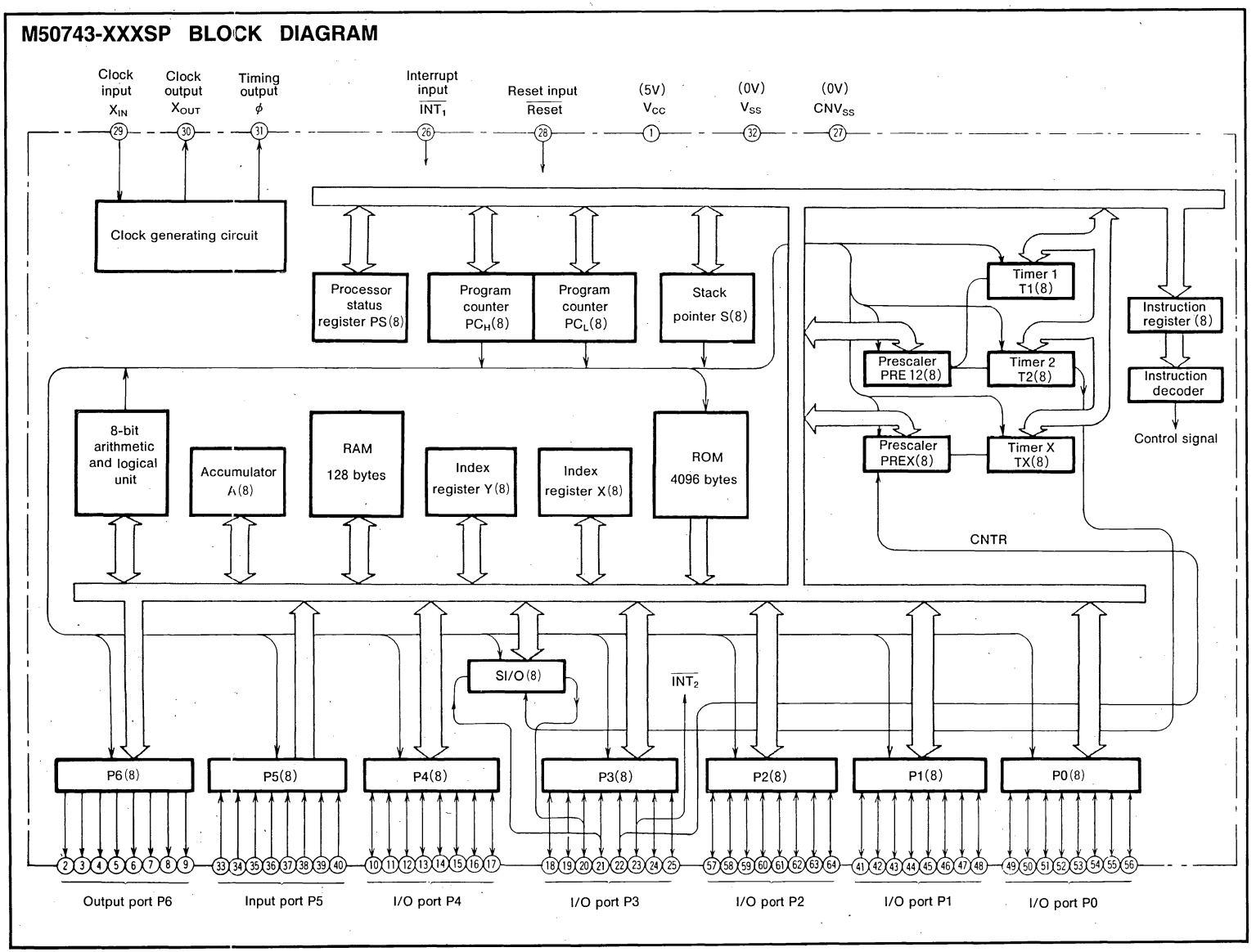
Outline 64P4B



Outline 72P6 NC : No connection

MITSUBISHI ELECTRIC

M50743-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M50743-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1 μs (minimum instructions, at 8MHz frequency)
Memory size	ROM		4096bytes
	RAM		128bytes
Input/output ports	$\overline{INT_1}$, $\overline{INT_2}$	Input	1-bit×1
	P0, P1, P2, P3, P4	I/O	8-bit×5 (part of P3 is used for serial I/O, timer I/O and interrupt input)
	P5	Input	8-bit×1
	P6	Output	8-bit×1
Serial I/O			8-bit×1
Timers			8-bit prescalers×2+8-bit timer×3 (2 when serial I/O is used)
Subroutine nesting			64 levels (max.)
Interrupts			Two external interrupts, three internal timer interrupts (or timer×2, serial I/O×1)
Clock generating circuit			Built-in (externally connected ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	At high-speed operation		30mW (at 8MHz frequency)
Input/Output characteristics	Input/Output voltage		5V
	Output current		5mA (ports P0, P1, P2, P3, P4, P6)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M50743-XXXSP		64-pin shrink plastic molded DIP
	M50743-XXXFP		72-pin plastic molded QFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions).If more time is needed for the crystal oscillator to stabilize, this "L" condition should be mained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an output pin for the timer X.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest order order interrupt input pin ($\overline{INT_2}$) , respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
$P6_0$~$P6_7$	Output port P6	Output	Port P6 is an 8-bit output port. The output structure is CMOS output.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50743-XXXSP is shown in Figure 1. Addresses $F000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 4096 bytes.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $007F_{16}$ are assigned to the built-in RAM and consist of 128 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

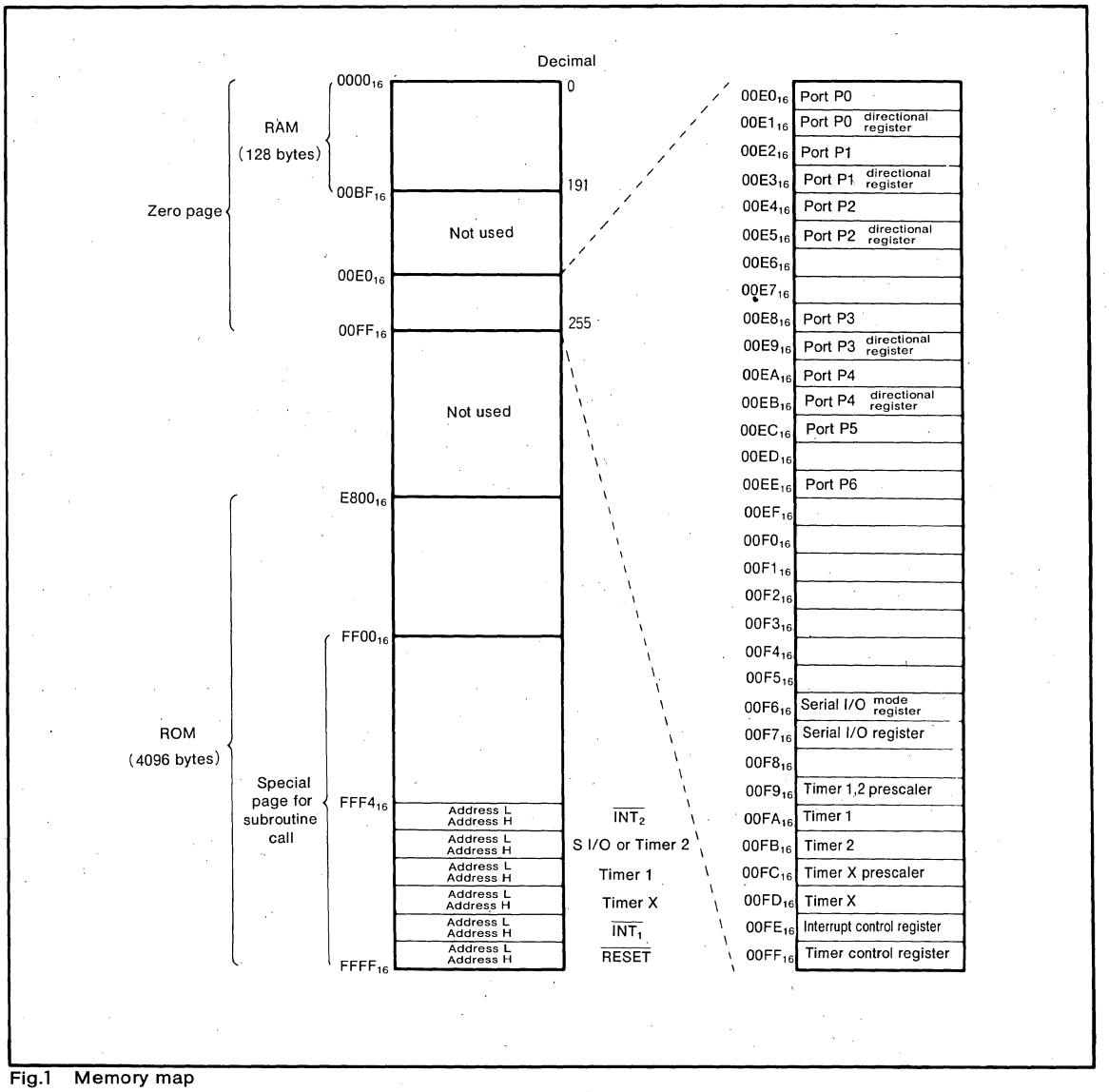


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

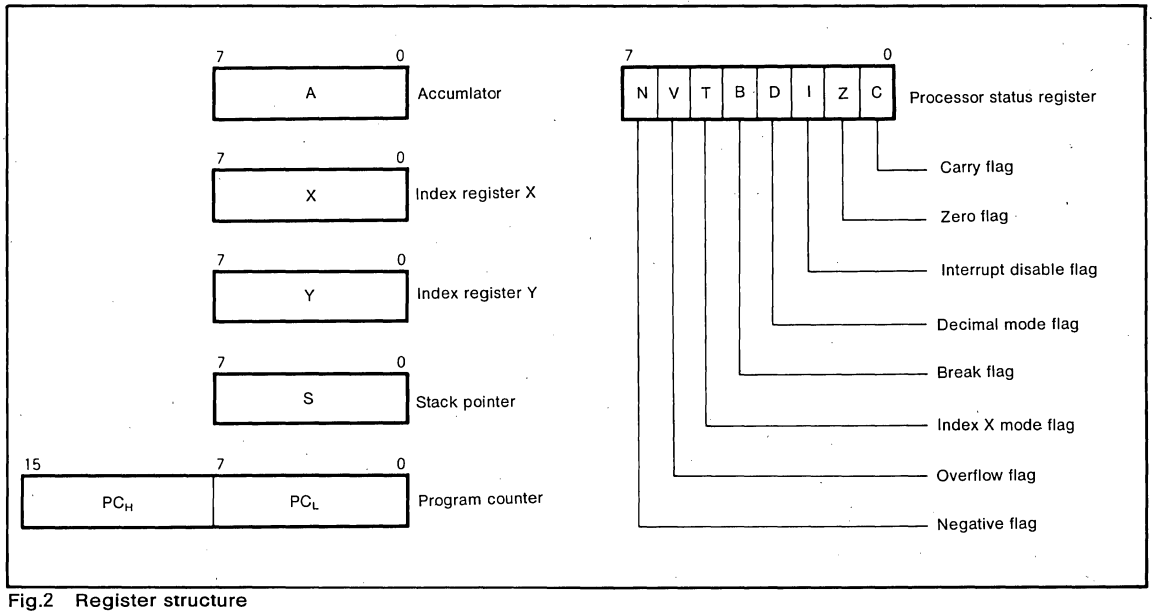


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The location of the stack can be determined by the stack page bit (bit 4 at address $00FF_{16}$). When bit 4 is "0" and the contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When bit 4 is "1", the stack address is set to $01XX_{16}$. When using this microcomputer in the single-chip mode, the stack page bit must be "0" and the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{\text{INT}_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1	4	$FFF9_{16}$, $FFF8_{16}$
Timer 2 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{\text{INT}_2}$ (BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50743-XXXSP can be interrupted from seven souces; $\overline{\text{INT}_1}$, timer X, timer 1, timer 2/serial I/O, or $\overline{\text{INT}_2}$/BRK instruction.

However, the $\overline{\text{INT}_2}$ pin is used with port $P3_2$ and the corresponding directional register bit should be set to "0" when $P3_2$ is used as an interrupt input pin.

The value of bit 2 of the serial I/O mode register (address $00F6_{16}$) determine whether the interrupt is from timer 2 or from serial I/O. When bit 2 is "0" the interrupt is from timer 2, and when bit 2 is "1" the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and

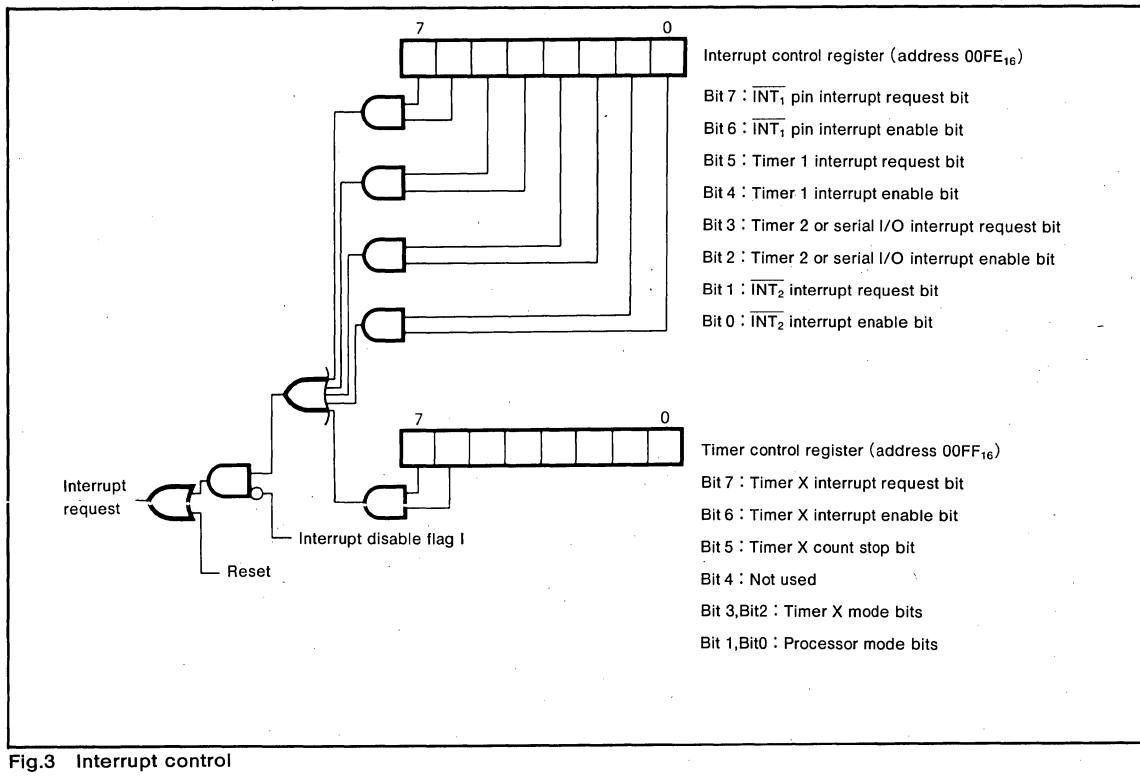


Fig.3 Interrupt control

the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"

(2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

TIMER

The M50743-XXXSP has three timers; timer X, timer 1, and timer 2. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section). Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1 and timer 2 is shown in Figure 4.

The $P3_3$/CNTR pin cannot be used as CNTR when $P3_3$ is being used in the normal I/O mode.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

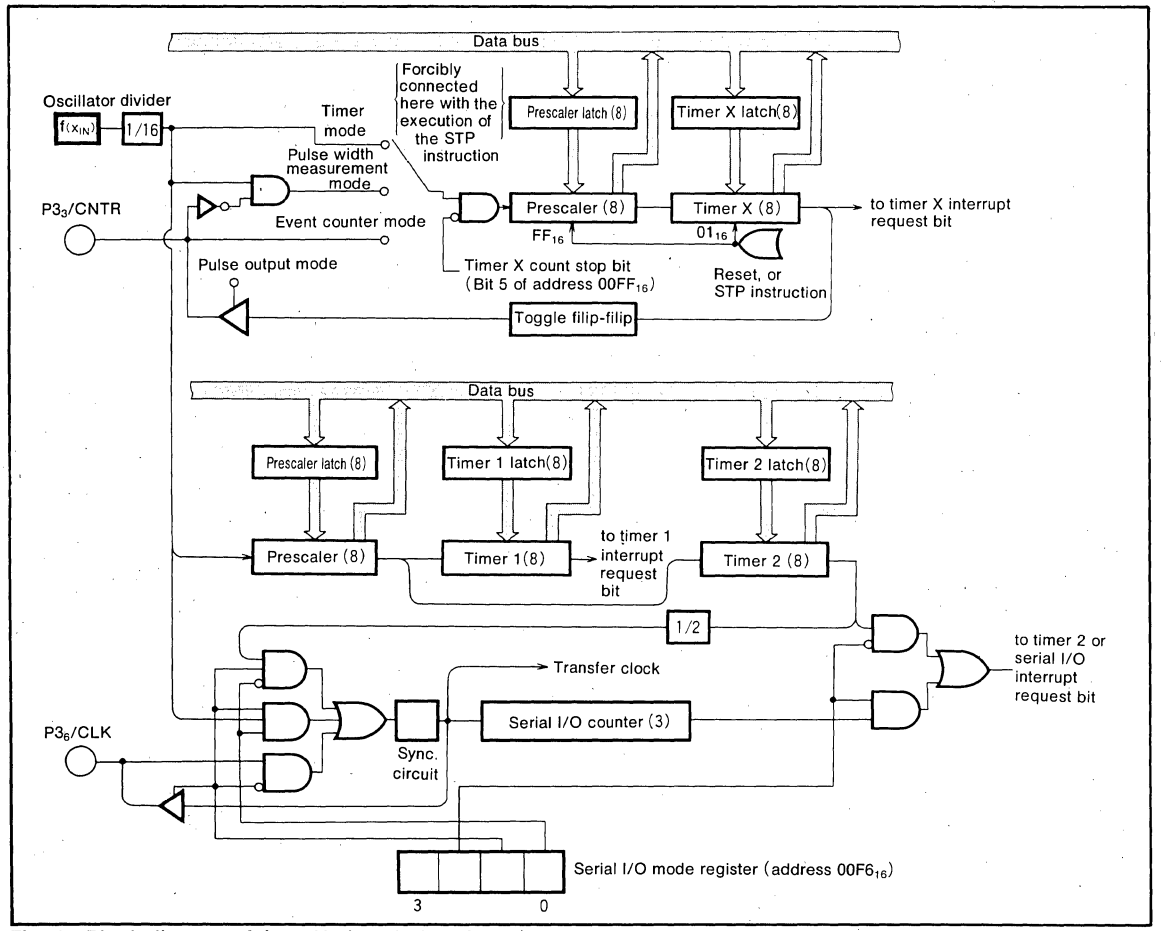


Fig. 4 Block diagram of timer X, timer1, timer2

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see Interrupt section). The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock sourse.

(4) Pulse width measurement mode [11]
This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

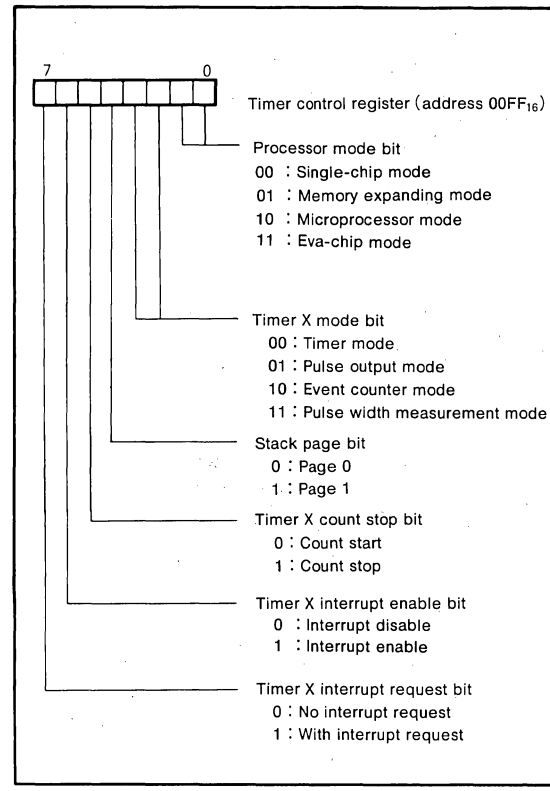


Fig.5 Structure of timer control register

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 6.

In the serial I/O mode the receive raady signal ($\overline{S_{RDY}}$), synchronous input /output clock (CLK), and the serial I/O pins (S_{OUT}, S_{IN}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F6_{16}$) is 4-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 2, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], oscillator frequency divided by 16, becomes the clock.

Bit 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is a "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0"

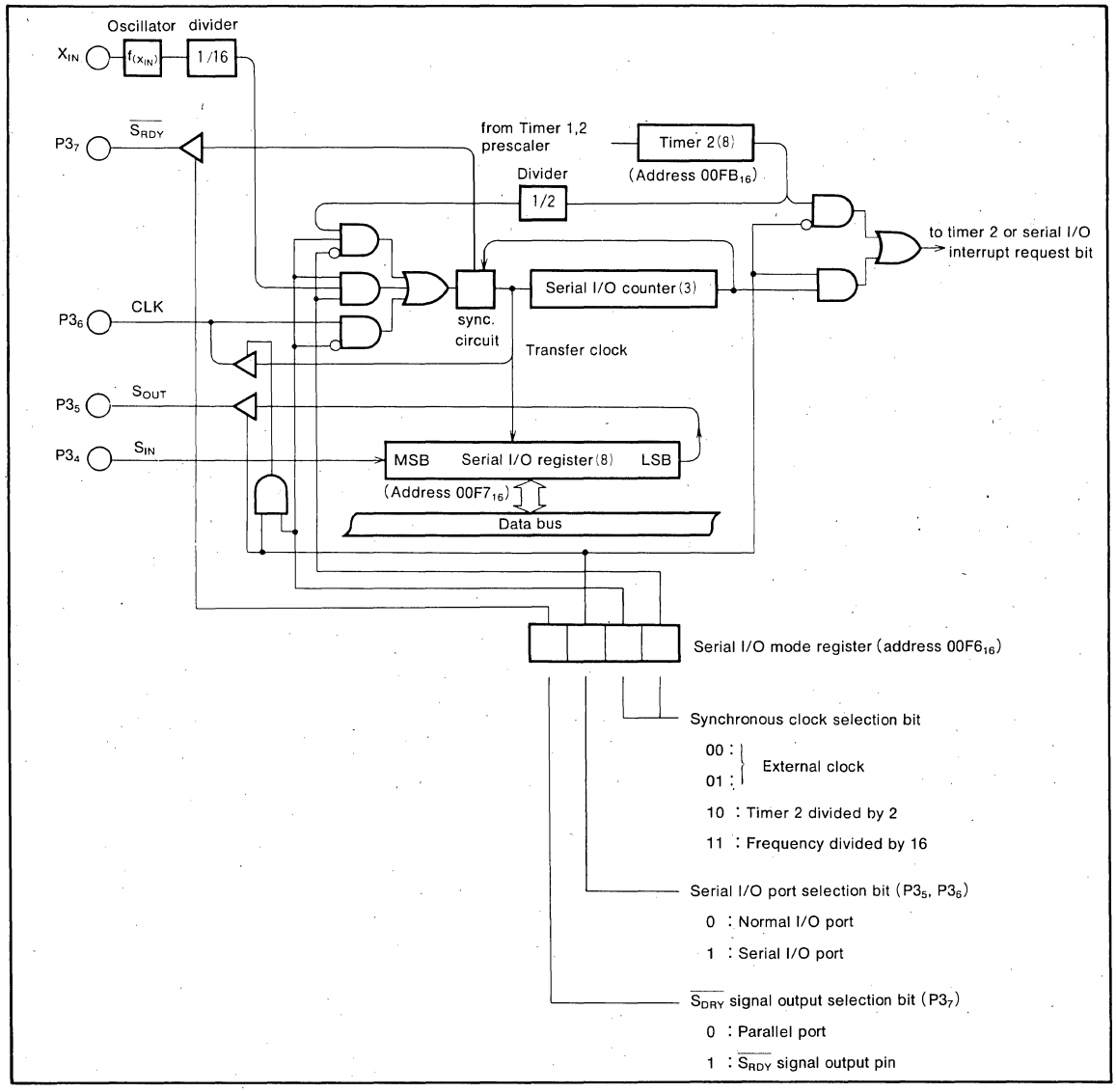


Fig.6 Block diagram of serial I/O

$P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 2. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3=1, $\overline{S_{RDY}}$) or used as normal I/O pin (bit 3=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address $00F7_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50743-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrpt request bit will be set.

External Clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 7. An example of communication between two M50743-XXXSPs is shown in Figure 8.

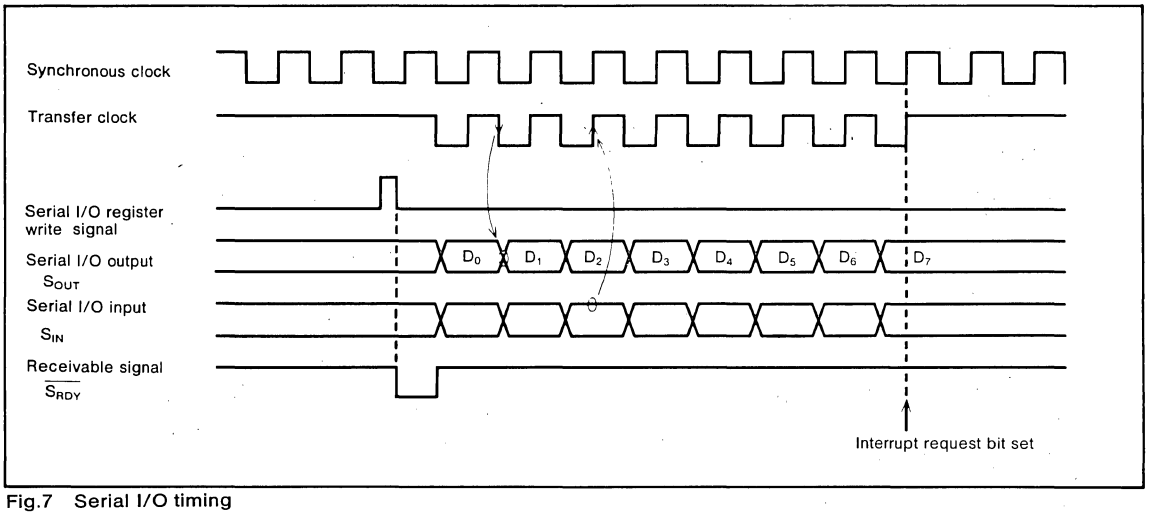


Fig.7 Serial I/O timing

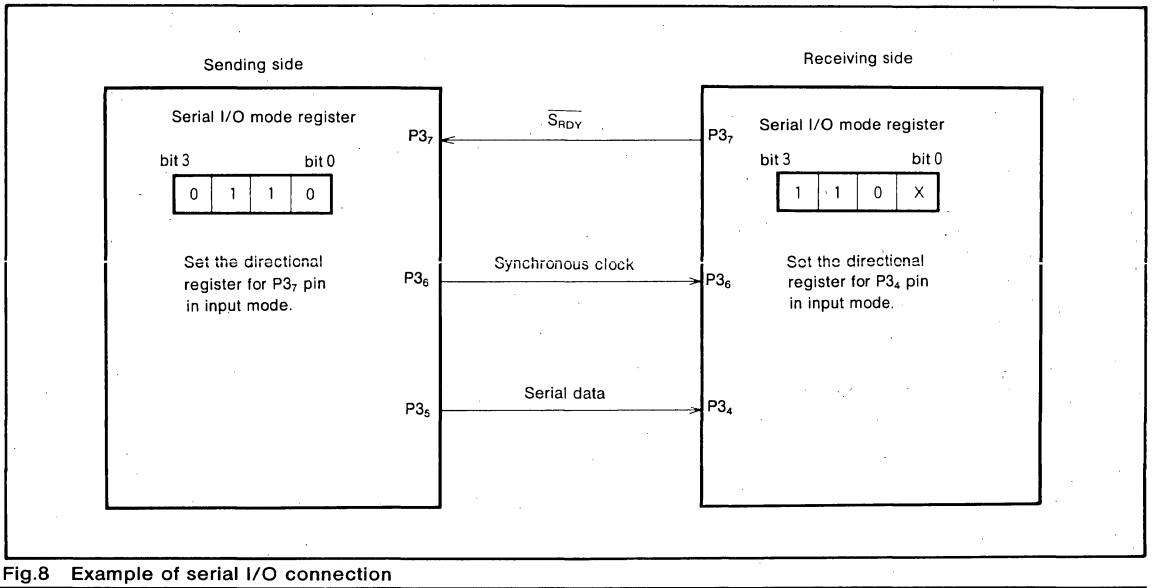
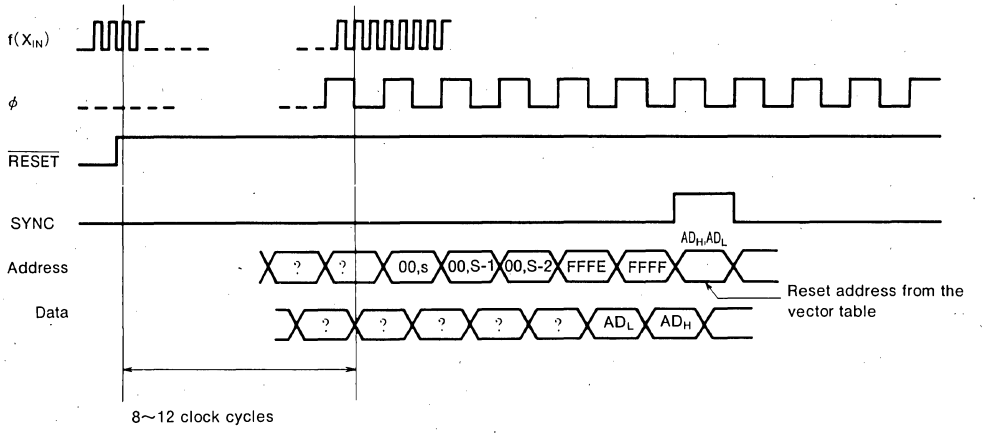


Fig.8 Example of serial I/O connection

RESET CIRCUIT

The M50743-XXXSP is reset according to the sequence shown in Figure 9. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 10. An example of the reset circuit is shown in Figure 11. When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.



Note 1 : The relationship between ϕ and $f_{(X_{IN})}$ is normally $f_{(X_{IN})}=4\cdot\phi$

2 : The mark "?" means that the address is changeable depending on the previous state.

Fig.9 Timing diagram at reset

	Address	
(1) Port P0 directional register	(E 1 $_{16}$) ···	0 0 $_{16}$
(2) Port P1 directional register	(E 3 $_{16}$) ···	0 0 $_{16}$
(3) Port P2 directional register	(E 5 $_{16}$) ···	0 0 $_{16}$
(4) Port P3 directional register	(E 9 $_{16}$) ···	0 0 $_{16}$
(5) Port P4 directional register	(E B $_{16}$) ···	0 0 $_{16}$
(6) Port P6 (Note 1)	(E E $_{16}$) ···	F F $_{16}$
(7) Serial I/O mode register	(E 6 $_{16}$) ···	0 0 0 0
(8) Prescaler X	(E C $_{16}$) ···	F F $_{16}$
(9) Timer X	(F D $_{16}$) ···	0 1 $_{16}$
(10) Interrupt control register	(F E $_{16}$) ···	0 0 $_{16}$
(11) Timer control register	(F F $_{16}$) ···	0 0 $_{16}$
(12) Interrupt disable flag on processor status register	(P S) ···	1
(13) Program counter	(P C $_H$) ···	Contents of address $FFFF_{16}$
	(P C $_L$) ···	Contents of address $FFFE_{16}$

Note 1 : Port P6 is the high-impedance state during reset.
After return from reset, it is "FF_{16}".

Fig.10 Internal state of microcomputer at reset

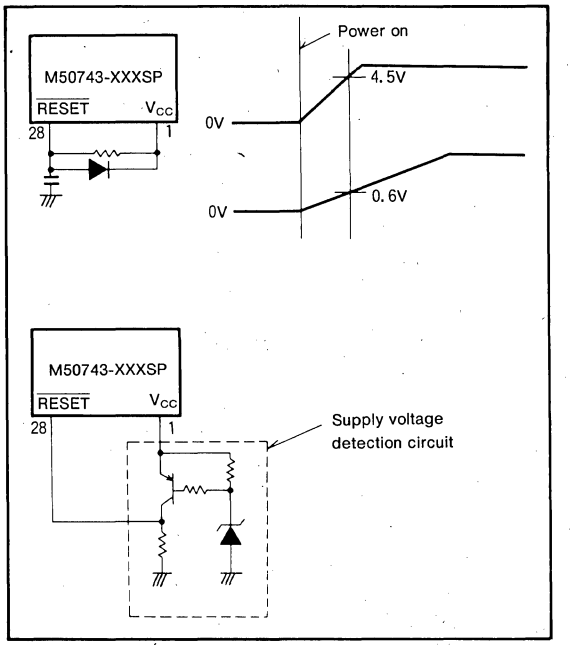


Fig.11 Example of reset circuit

MITSUBISHI ELECTRIC

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as serial I/O, $\overline{INT_2}$ and I/O pins for timer X. For more details, see the processor mode information.

(5) Port P4

Port P4 has the same function as port P0 in the single-chip mode. This function does not change even though the processor mode changes.

(6) Port P5

Port P5 is an input port.

(7) Port P6

Port P6 is a CMOS output port. See Figure 12 for more details.

(8) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ.

(9) $\overline{INT_1}$ pin

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

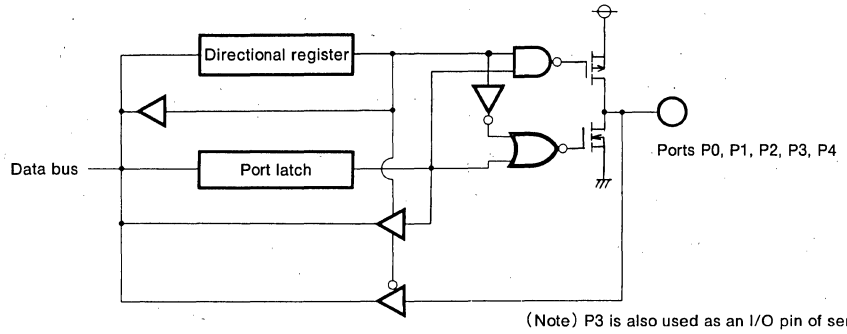
(10) $\overline{INT_2}$ pin ($P3_2/\overline{INT_2}$ pin)

The $\overline{INT_2}$ pin is an interrupt input pin used with $P3_2$. To use this pin as an interrupt pin, set the corresponding bit in the directional register to input ("0"). When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1".

(11) CNTR pin ($P3_3$/CNTR pin)

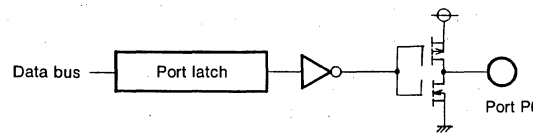
The $P3_3$/CNTR pin is an I/O pin of timer X. To use this pin as the timer X input pin, set the corresponding directional register bit to input ("0"). In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

Ports P0, P1, P2, P3, P4

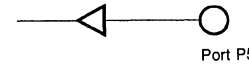


(Note) P3 is also used as an I/O pin of serial I/O and CNTR, and input pin of $\overline{INT_2}$.

Port P6



Port P5



ϕ

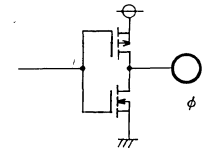


Fig.12 Block diagram of port P0~P6 (single-chip mode) and output format of ϕ

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 14 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 13.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

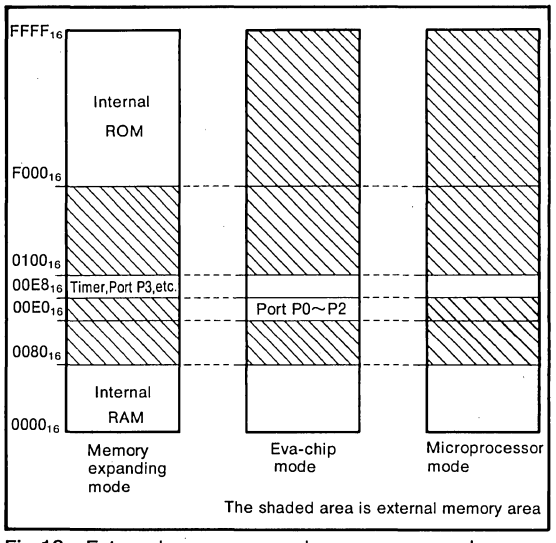


Fig.13 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost. Port P2 becomes the data bus of D_7～D_0 (including instruction code) and loses its normal I/O functions. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively when ϕ enters into the "H" state. Port $P3_2$ functions as an input port during this same transition.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode.

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the databus (D_7～D_0) and loses its normal I/O functions. Port $P3_1$ and $P3_1$ and $P3_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is requierd.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

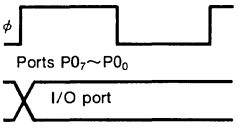
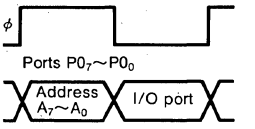
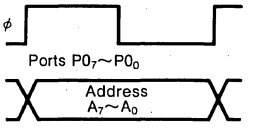
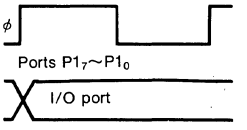
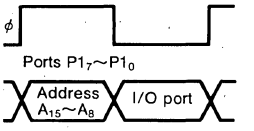
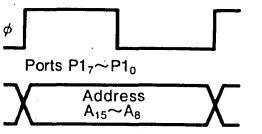
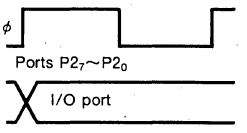
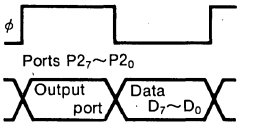
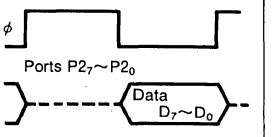
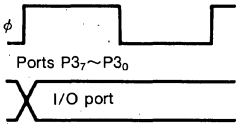
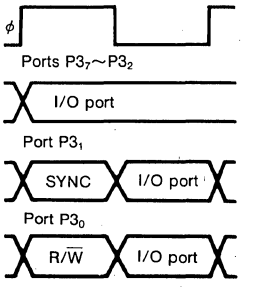
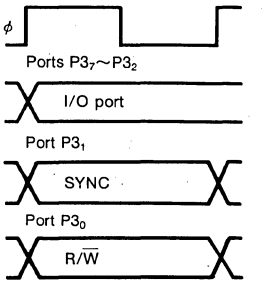
Port \ Mode	CM_1 0, CM_0 0 Single-chip mode	CM_1 1, CM_0 1 Eva-chip mode	CM_1 0, CM_0 1 Memory expanding mode	CM_1 1, CM_0 0 Microprocessor mode
Port P0				Same as left
Port P1				Same as left
Port P2				Same as left
Port P3				Same as left

Fig.14 Processor mode and functions of port P0~P3

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 17.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleard when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 15.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock uasge is shown in Figure 16. X_{IN} is the input, and X_{OUT} is open.

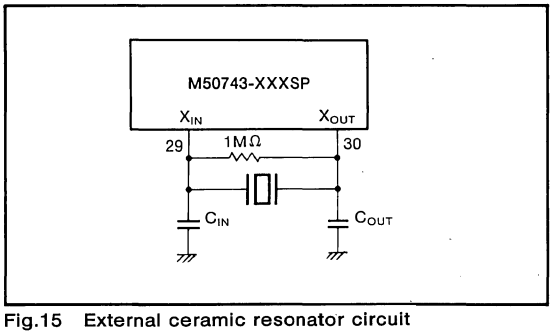


Fig.15 External ceramic resonator circuit

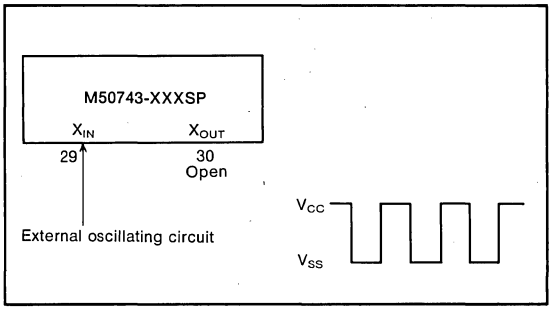


Fig.16 External clock input circuit

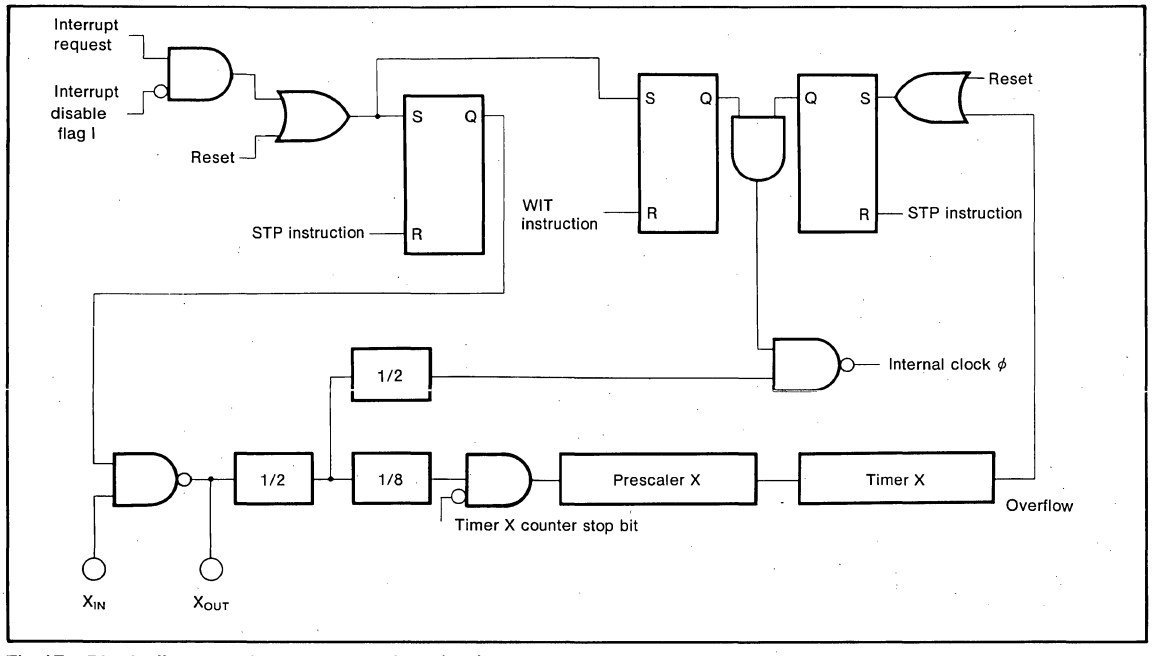


Fig.17 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(5) A NOP instruction must be used after the execution of a PLP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ..... EPROM 3sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off.	−0.3∼7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, $\overline{INT_1}$, $P5_0$∼$P5_7$		−0.3∼7	V
V_I	Input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage, CNV_{SS}		−0.3∼13	V
V_O	Output voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P6_0$∼$P6_7$, X_{OUT}, ϕ		−0.3∼V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
T_{opr}	Operating temperature		−10∼70	℃
T_{stg}	Storage temperature		−40∼125	℃

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (T_a = −10∼70℃, V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P6_0$∼$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P6_0$∼$P6_7$ (Note 3)			5	mA
$I_{OH(peak)}$	"H" peak output current, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P6_0$∼$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P6_0$∼$P6_7$ (Note 3)			−5	mA
$f(X_{IN})$	Internal clock oscillating frequency			8	MHz

Note 2 : $I_{OL(avg)}$, $I_{OH(avg)}$ is the average current in 100ms.
3 : The total of $I_{OL(peak)}$ of P0, P1, P2, P3, P4 and P6 should be 80mA max.
The total of $I_{OH(peak)}$ of P0 and P1 should be 30mA max.
The total of $I_{OH(peak)}$ of P2 should be 50mA max.
The total of $I_{OH(peak)}$ of P3, P4 and P6 should be 30mA max.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OH} = −10mA		3			V
V_{OH}	"H" output voltage, ϕ	I_{OH} = −2.5mA		3			V
V_{OL}	"L" output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OL} = 10mA				2	V
V_{OL}	"L" output voltage, ϕ	I_{OL} = 5mA				2	V
V_{T+}−V_{T-}	Hysteresis, $P3_6$	When used as CLK input		0.3		1	V
V_{T+}−V_{T-}	Hysteresis, $\overline{INT_1}$			0.3		1	V
V_{T+}−V_{T-}	Hysteresis, $P3_2$	When used as $\overline{INT_2}$		0.3		1	V
V_{T+}−V_{T-}	Hysteresis, $P3_3$	When used as CNTR		0.3		1	V
V_{T+}−V_{T-}	Hysteresis, $\overline{RESET}$				0.5	0.7	V
V_{T+}−V_{T-}	Hysteresis, X_{IN}			0.1		0.5	V
I_{IL}	"L" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 0V				−5	μA
I_{IH}	"H" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 5V				5	μA
V_{RAM}	RAM holding voltage	When clock stops		2			V
I_{CC}	Supply current	Output port open; other ports are connected to V_{SS}.	$f_{(X_{IN})}$ = 8MHz Square wave		6	12	mA
			T_a=25℃ At clock stops			1	μA
			T_a=70℃ At clock stops			10	μA

TIMING REQUIREMENTS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time	200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time	20			ns
t_C	External clock input cycle time	125			ns
t_W	External clock input pulse width	62			ns
t_r	External clock rising edge			20	ns
t_f	External clock falling edge			20	ns

Eva-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Memory expanding mode and microprocessor mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	150			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.18			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns

Eva-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.18			150	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				150	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				150	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				150	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				150	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				150	ns
$t_{d(\phi-R/\overline{W})}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-R/\overline{W}F)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				150	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				150	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				150	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				150	ns

Memory expanding mode and microprocessor mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.18			150	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time		40		150	ns
$t_{d(\phi-R/\overline{W})}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				150	ns

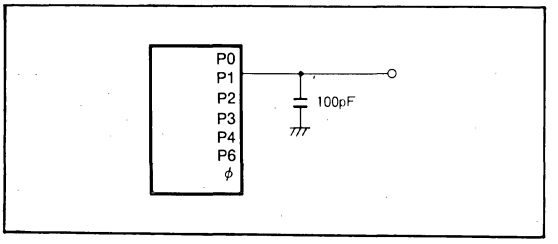
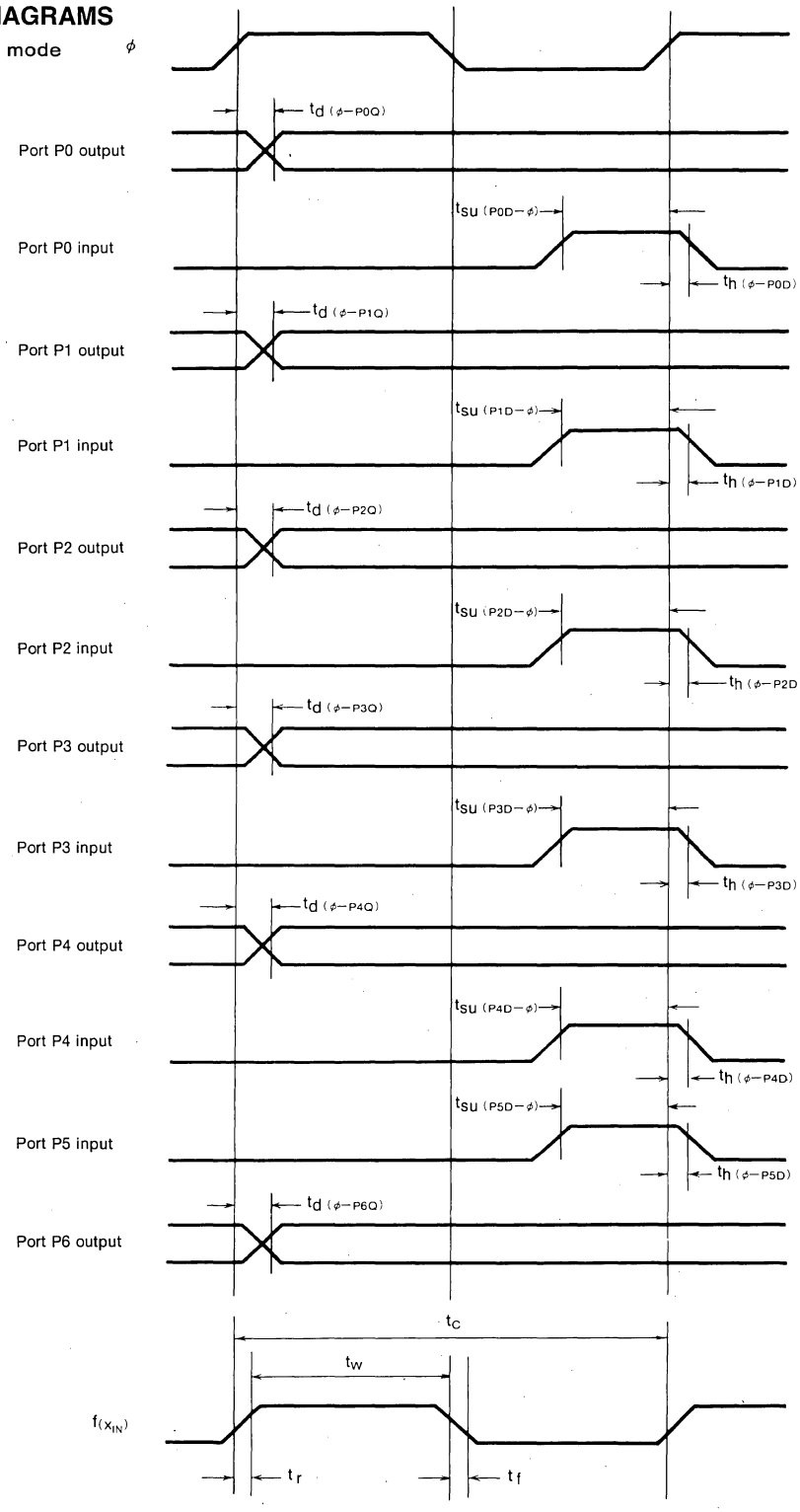


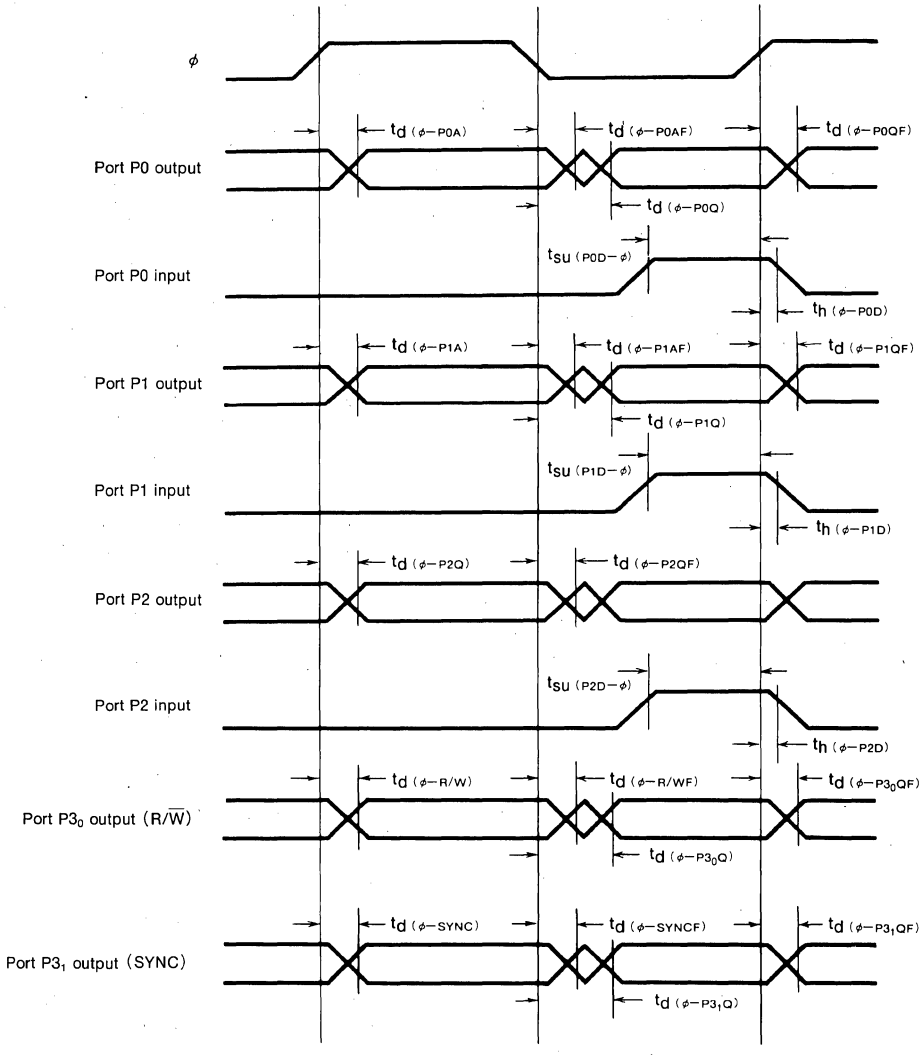
Fig.18 Port P0~P4 and port P6 test circuit

TIMING DIAGRAMS

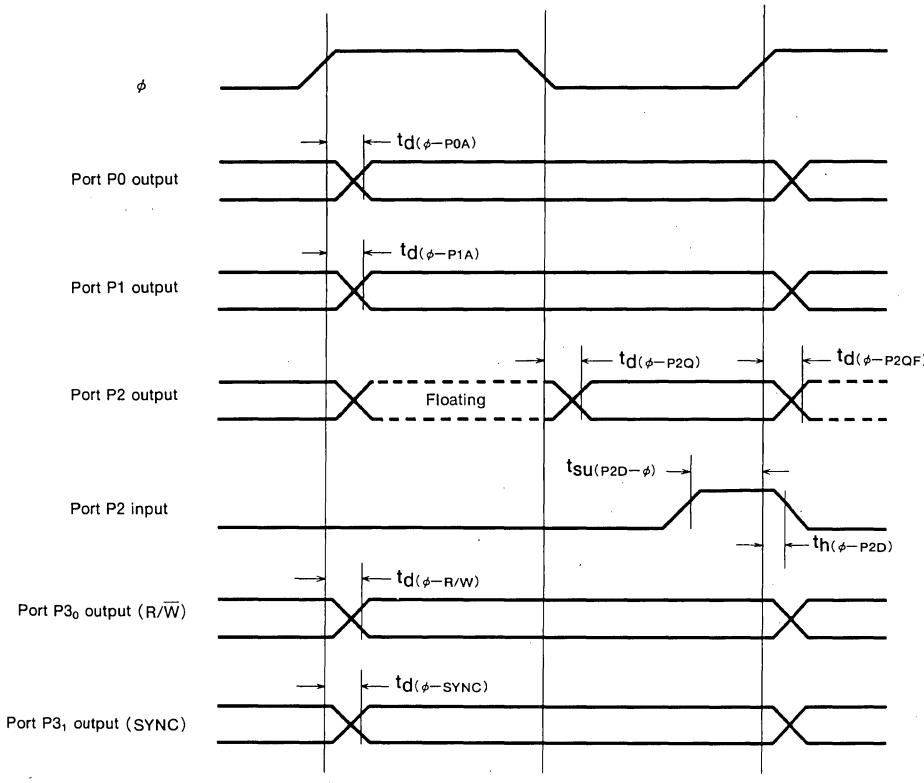
In single-chip mode



In eva-chip mode



In memory expanding mode and microprocessor mode



M50744-XXXSP/FP
M50746-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50744-XXXSP and the M50746-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. Both are housed in a 64-pin shrink plastic molded DIP (flat package type also available). These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50744-XXXSP and the M50746-XXXSP are noted below. The following explanations apply to the M50744-XXXSP. Specification variations for other chips are noted accordingly.

Type name	ROM size
M50744-XXXSP	4096bytes
M50746-XXXSP	6144bytes

The differences between the M50744-XXXSP and the M50744-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

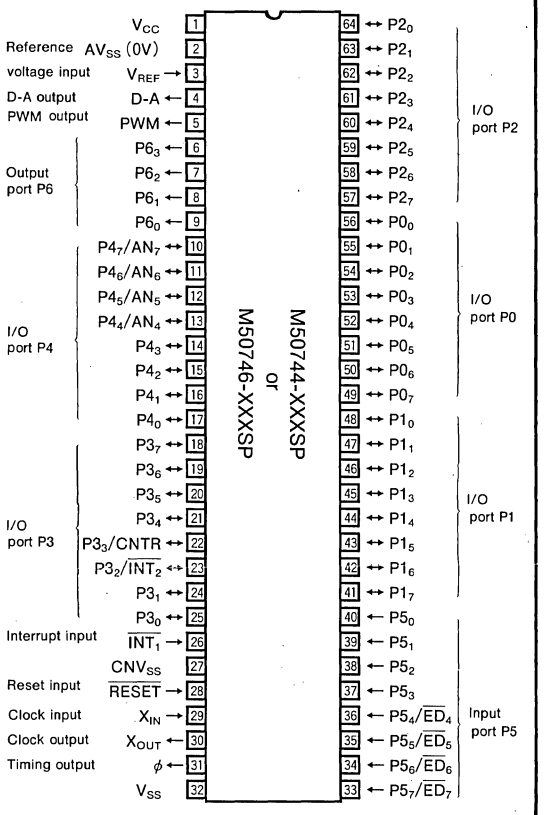
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM .....4096 bytes (M50744-XXXSP)
  6144 bytes (M50746-XXXSP)
  RAM 144bytes
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz .....5V±10%
- Power dissipation
  normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting .....72 levels (Max.)
- Interrupt .....6 types, 5 vecters
- 8-bit timer 3
- Programmable I/O (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Output ports (Port P6) 4
- A-D converter ..... 8-bit successive approximation
- D-A converter
- 8-bit PWM function
- Watchdog timer

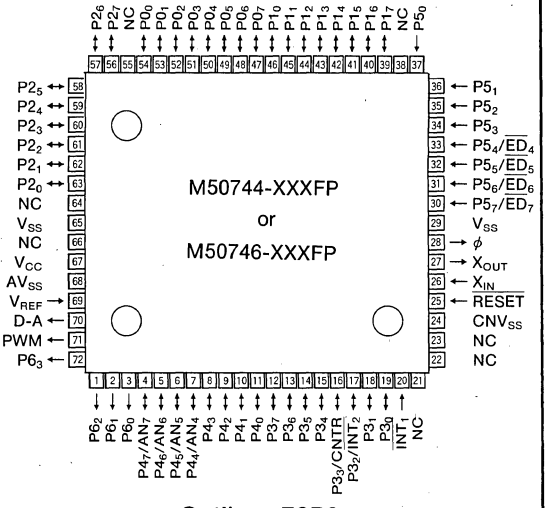
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

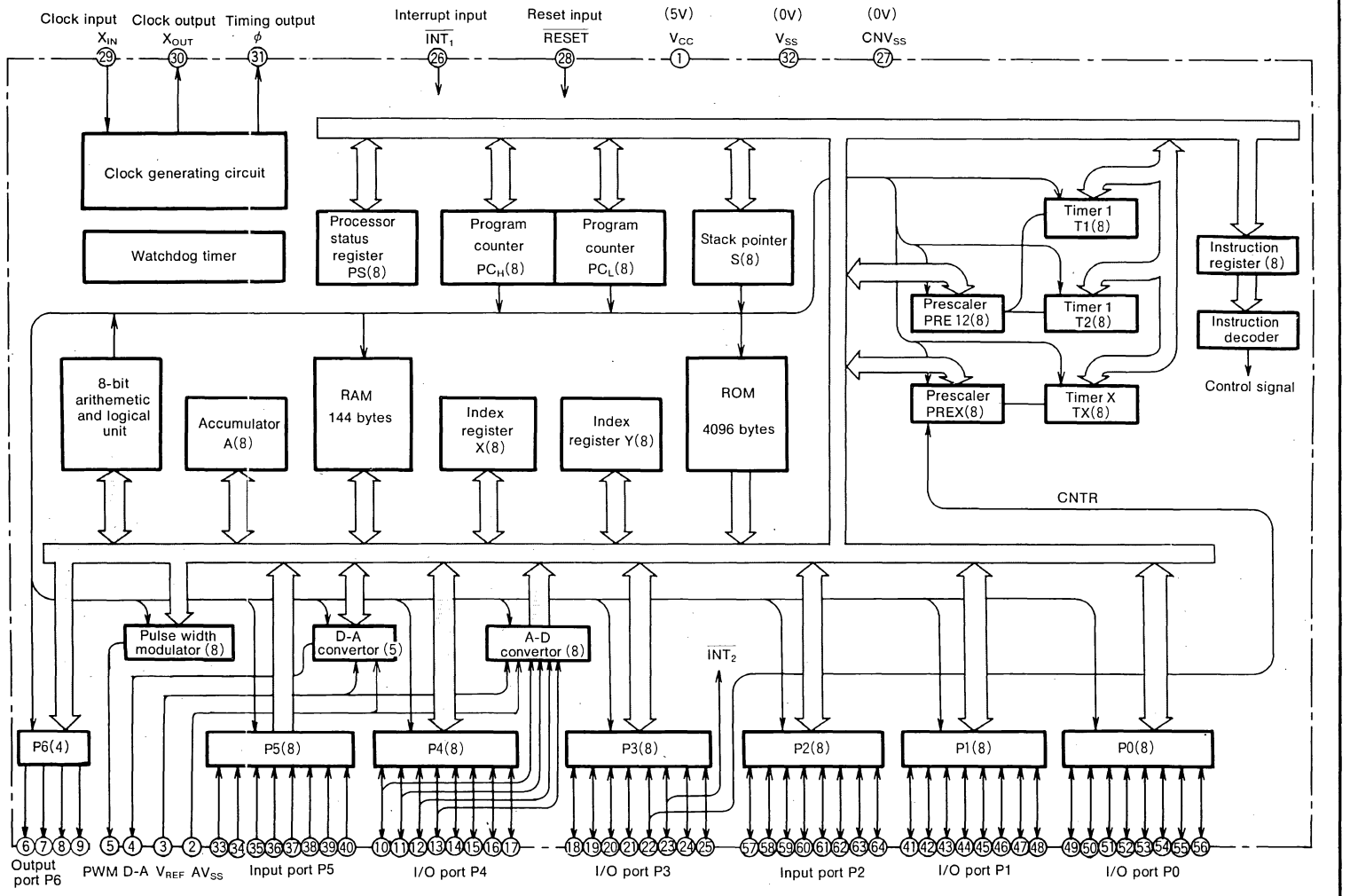


Outline 72P6

NC : No connection

MITSUBISHI ELECTRIC

M50744-XXXSP BLOCK DIAGRAM



Note 1 : 6144 byts for M50746-XXXSP

FUNCTIONS OF M50744-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction excution time			2μs (minimum instructions at 4MHz frequency)
Memory size	ROM		4096bytes (6144bytes for M50746-XXXSP)
	RAM		144bytes
I/O ports	$\overline{INT_1}$	Input	1-bit×1
	P0, P1, P2, P3, P4	I/O	8-bit×5(Part of P3 used with timer I/O and interrupt input)
	P5	Input	8-bit×1
	P6	Output	4-bit×1
Timers			8-bit prescaler×2+8-bit timer×3
A-D converter			8-bit× 1 (4 channels)
D-A converter			5-bit×1
Pulse width modulator			8-bit×1
Watchdog timer			15-bit×1
Subroutine nesting			72 levels (max.)
Interrupt			2 external interrupts, 3 internal timer interrupts
Clock generating circuit			Built-in (externally connected ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	High-speed operation		15mW (at 4MHz frequency)
I/O characteristics	I/O voltage		12V (Ports P0, P1, P3, P4, P5, P6, $\overline{INT_1}$)
	Output current		5mA (Ports P0, P1, P2, P3, P4)
Memory expansion			Possibe
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M50744-XXXSP, M50746-XXXSP		64-pin shrink plastic molded DIP
	M50744-XXXFP, M50746-XXXFP		72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
AV_{SS}	Voltage input for A-D and D-A		This is GND input pin for the A-D and D-A converters.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D and D-A converters.
D-A	D-A output	Output	This is output pin from the D-A converter.
PWM	PWM output	Output	This is output pin from the pulse width modulator. The output structure is N-channel open drain.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. $P3_3$ and $P3_2$ work as CNTR pin and the lowest interrupt input pin ($\overline{INT_2}$), respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. $P4_4$~$P4_7$ work as analog input port AN_4~AN_7.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port. $P5_4$~$P5_7$ can be used as the edge sense inputs.
$P6_0$~$P6_3$	Output port P6	Output	Port P6 is a 4-bit output port. The output structure is N-channel open drain.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50744-XXXSP is shown in Figure 1. Addresses $F000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 4096 bytes.

Addresses $E800_{16}$ to $FFFF_{16}$ are the ROM address area assigned to the M50746-XXXSP.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $008F_{16}$ are assigned to the built-in RAM and consist of 144 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

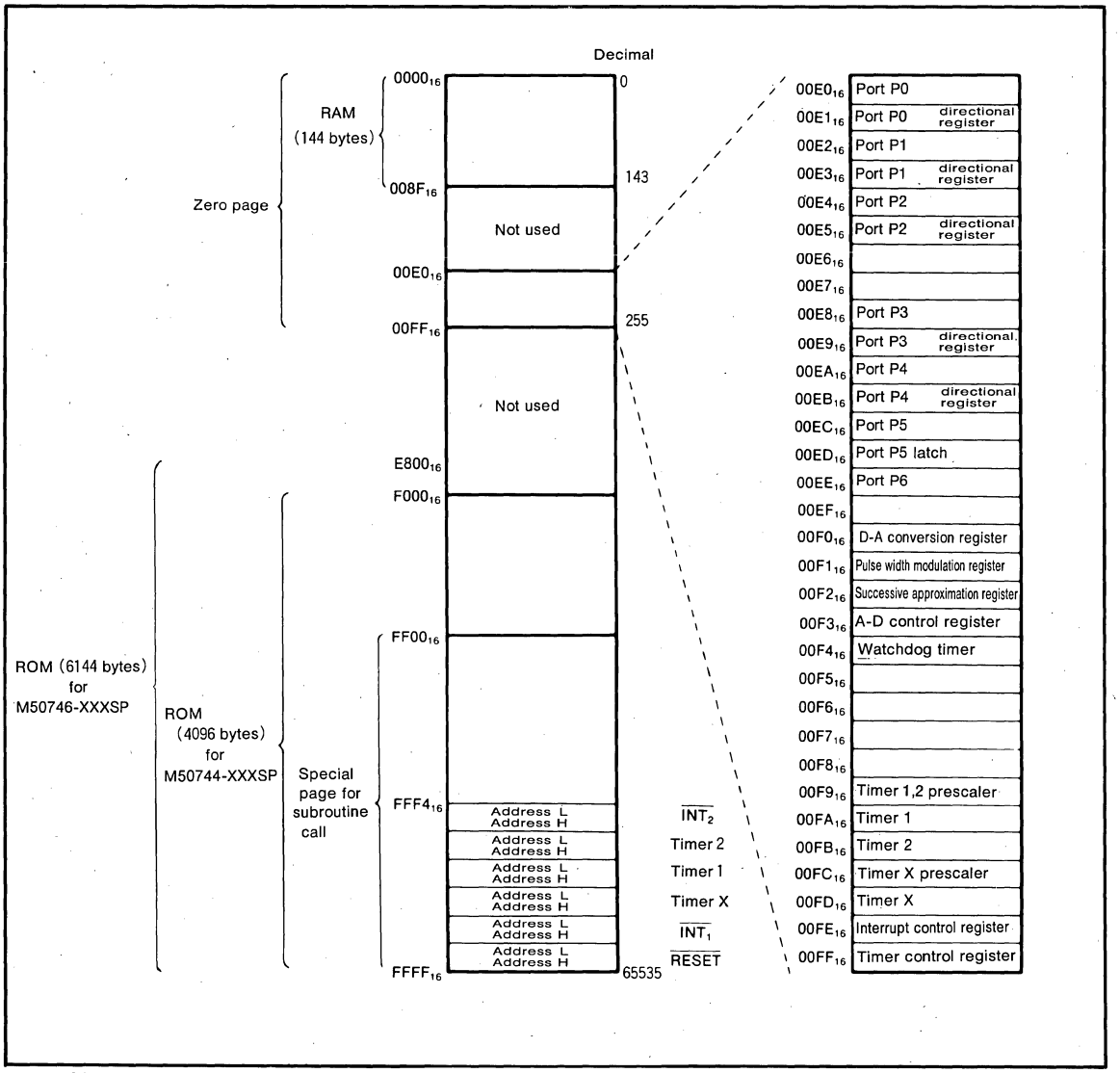


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

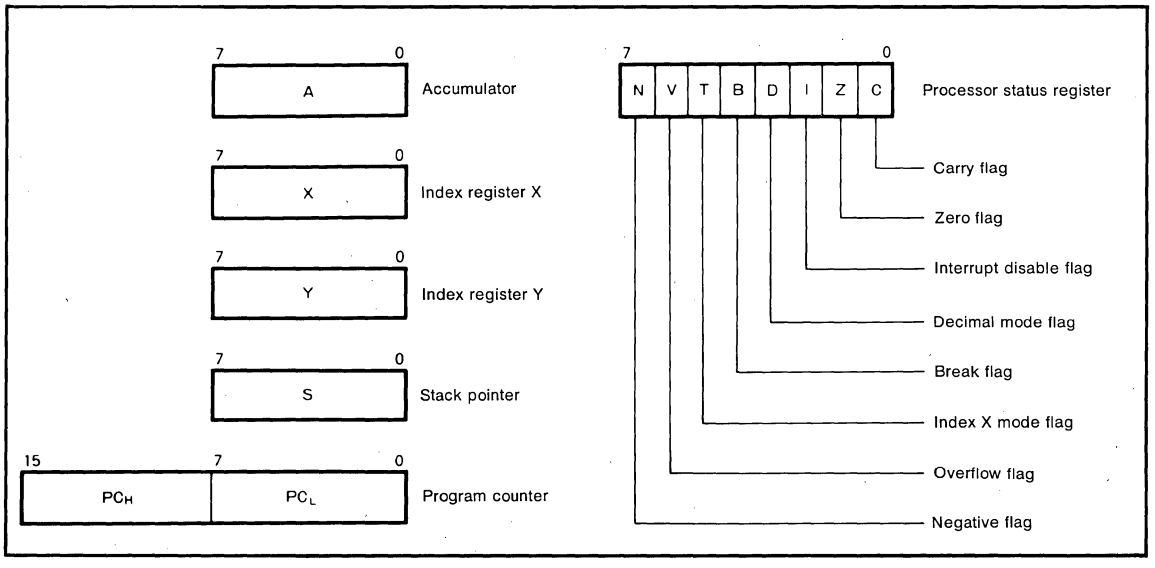


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The location of the stack can be determined by the stack page bit (bit 4 at address $00FF_{16}$). When bit 4 is "0" and the contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When bit 4 is "1", the stack address is set to $01XX_{16}$. When using this microcomputer in the single-chip mode, the stack page bit must be "0" and the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{\text{INT}_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1	4	$FFF9_{16}$, $FFF8_{16}$
Timer 2	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{\text{INT}_2}$(BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50744-XXXSP can be interrupted from seven souces; $\overline{\text{INT}_1}$, timer X, timer 1, timer 2, or $\overline{\text{INT}_2}$/BRK instruction.

However, the $\overline{\text{INT}_2}$ pin is used with port $P3_2$ and the corresponding directional register bit should be set to "0" when $P3_2$ is used as an interrupt input pin.

These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{\text{INT}_1}$ or $\overline{\text{INT}_2}$ pins go from "H" to "L"

(2) When the contents of timer X, timer 1, timer 2 go to "0"

These request bits can be reset by the program but can not

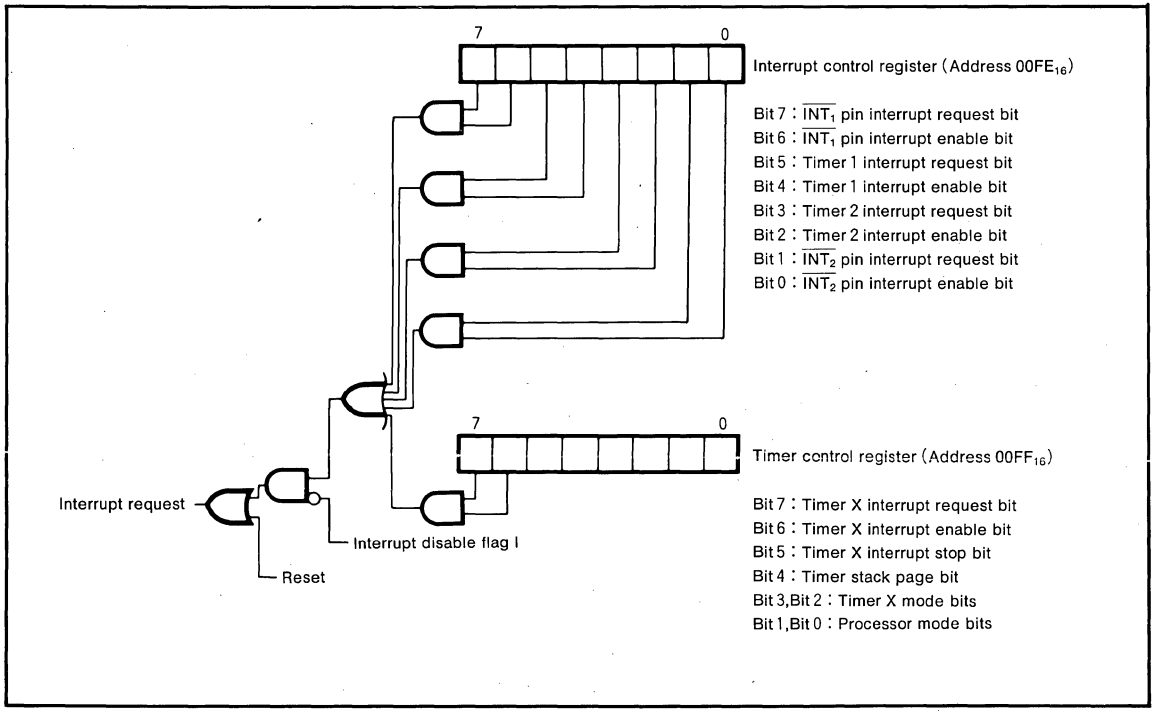


Fig. 3 Interrupt control

be set by the program. However, the interrupt enable bit can be set and reset by the program.
Since the BRK instruction and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

TIMER

The M50744-XXXSP has three timers; timer X, timer 1, and timer 2. Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1 and timer 2 is shown in Figure 4.
The $P3_3$/CNTR pin cannot be used as CNTR when $P3_3$ is being used in the normal I/O mode.
Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).
The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section).
The four modes of timer X as follows:

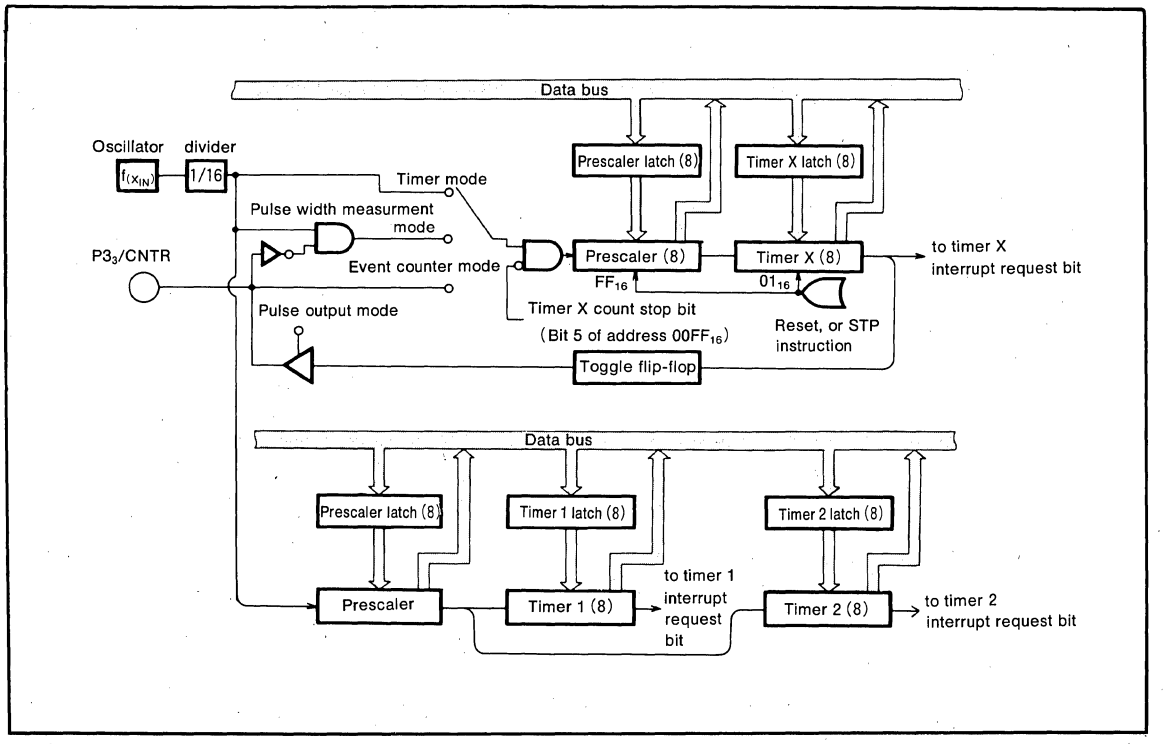


Fig.4 Block diagram of timer X, timer 1, timer 2

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock sourse.

(4) Pulse width measurement mode [11]
This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

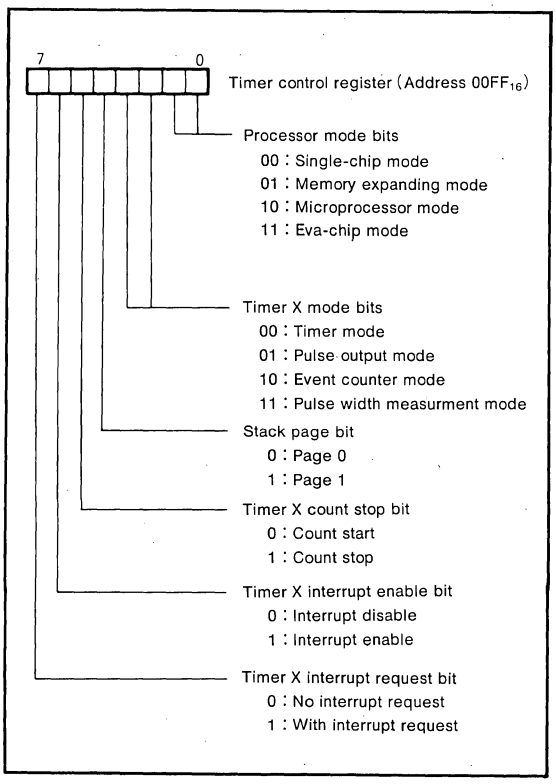


Fig.5 Structure of timer control registe

A-D CONVERTER

An 8-bit successive approximation method of A-D conversion is employed providing a precision of ±3LSB. A block diagram of the A-D convertor is shown in Figure 6. Conversion is automatic once it is started with the program.

The four analog inputs are used in common with pins $P4_7$, $P4_6$, $P4_5$, and $P4_4$ of port 4. Bits 1 and 0 of the A-D control regsiter (address $00F3_{16}$) are used to select which pins are used for A-D conversion. The input condition is accomplished by setting to "0" the bit in the directional register that corresponds to the pin where A-D conversion is to take place. Bit 4 of the A-D control regsiter is the A-D conversion end bit. During A-D conversion, this bit is "0", and upon completion becomes "1". Thus, it can be ascertained whether or not A-D conversion has been completed or not by inspecting this bit. The relation between the contents of the A-D control register and the selection of input pins are shown in Figure 7.

The results of the conversion can be found be reading the contents of the successive approximation register (address $00F2_{16}$) which stores the results of the conversion. The procedure for executing A-D conversion is next explained. Firstly, the pin that is to be used for the A-D conversion is selected by setting bit 1 and bit 0 of the A-D control register. Next, the successive approximation is written to upon which the A-D conversion starts. Since actual data is not written to the successive approximation, any type of may be written. Simultaneous with its being written, the A-D conversion end bit (bit 4 of address $00F3_{16}$) is cleared to "0" signifying that A-D conversion operations are being conducted. A-D conversion completes after 198 clock cycles upon which the A-D conversion end bit is set to "1" and the results of the conversion can be found in the successive approximation. Since the comparator consists of the capacitive coupled configuration, f (X_{IN}) is needed larger than 1MHz during A-D conversion.

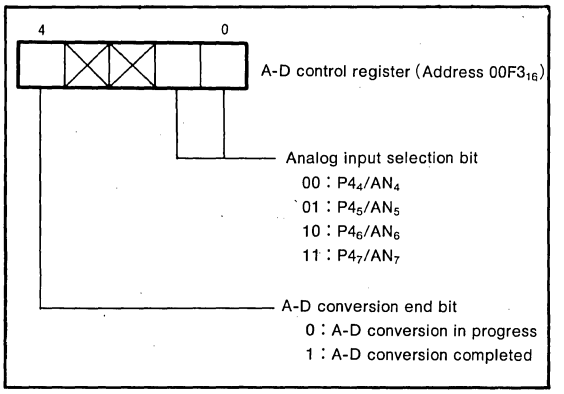


Fig.7 Structure of A-D control register

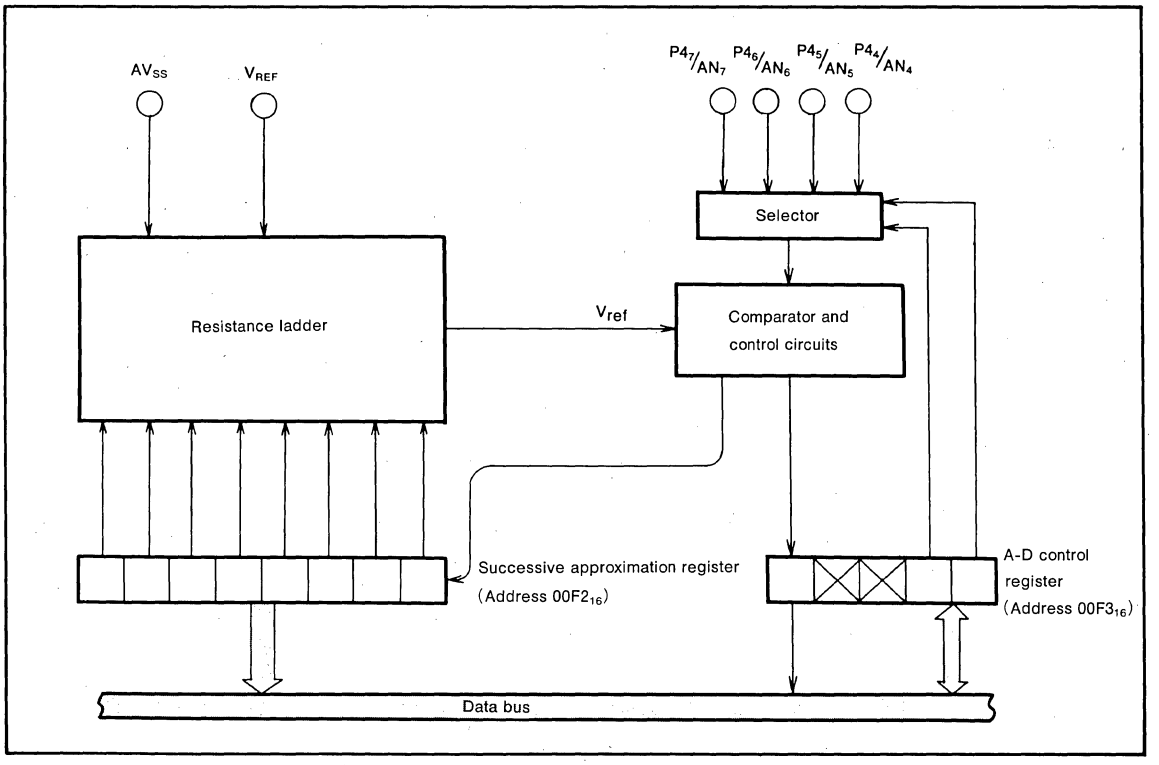


Fig.6 Block diagram of A-D converter

D-A CONVERTER

The R-2R method is used for D-A conversion. The block diagram is shown in Figure 8. An analog voltage is output that corresponds to the contents of the D-A conversion register (address $00F0_{16}$). Ideally, the relation of the analog output voltage V and the content n of the D-A conversion register is $V=V_{REF} \times n/32 (n=0 \sim 31)$.

Reset operation clears the contents (n) of the D-A conversion register to 0_{16}.

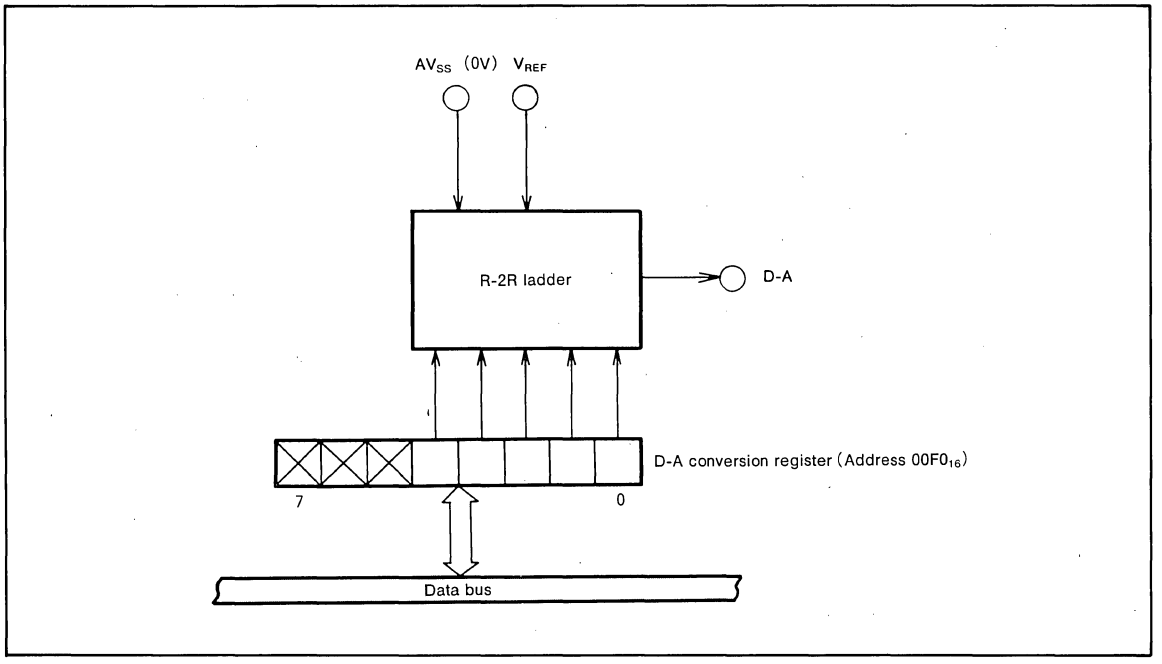


Fig.8 Block diagram of the D-A converter

PULSE WIDTH MODULATOR

The pulse width modulation register (address $00F1_{16}$) is configured of an 8-bit counter. The period of repetition is 4080 clock cycles. With the content of the pulse width modulation register m, the PWM pin becomes high-level for the period of 4080 × m/255 (m=0～255). Figure 9 shows that relationship. An N-channel open drain output is used for the PWM pin.

Reset sets the content m of the pulse width modulation register to 00_{16}.

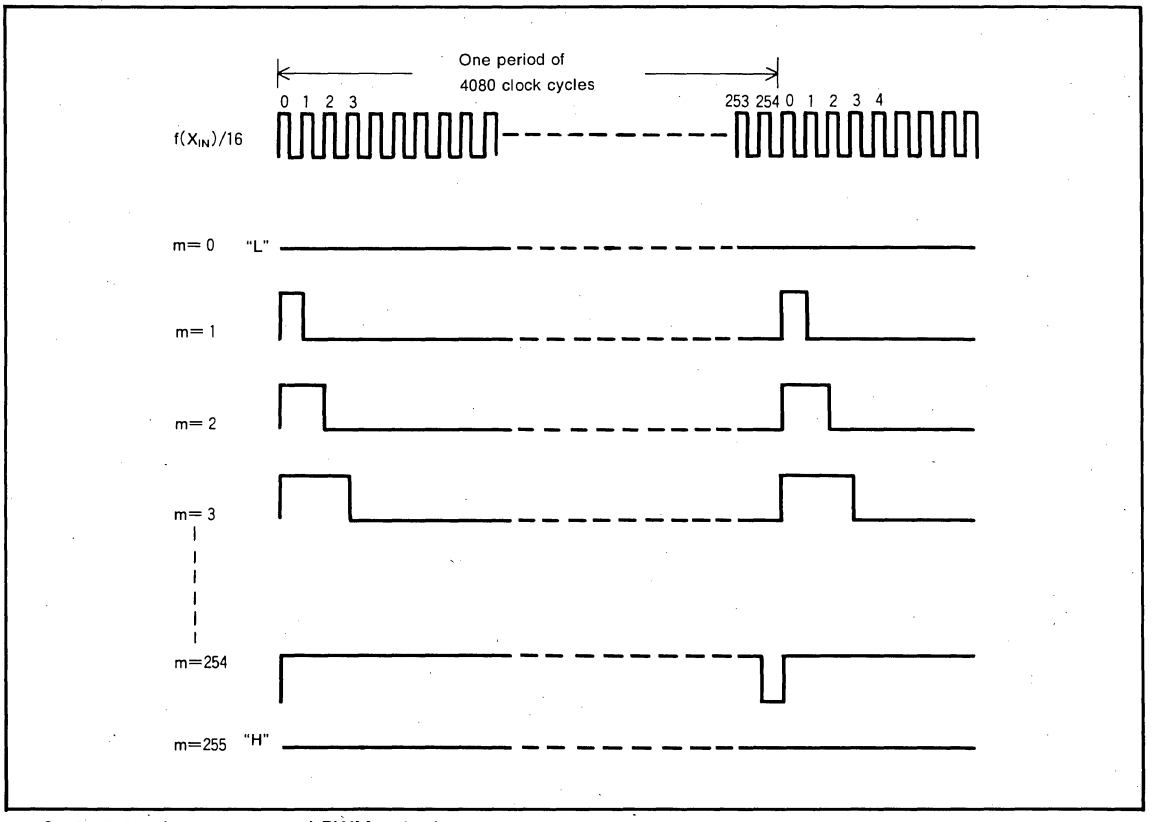


Fig.9 Relation between m and PWM output

WATCHDOG TIMER

The watchdog timer provides the means to return to a reset condition when a program runs wild and the program will not run the normal loops.

The watchdog timer (address $00F4_{16}$) is a 15-bit counter. The watchdog timer counts 1/16th the output frequency of the oscillator. The watchdog timer is set to $7FFF_{16}$ when a reset is accomplished or a write operation has been made to it. As well as any of the instructions that generate a write signal, such as STA, LDM, and CLB, can be used to write data to the watchdog timer. An output of the most significant bits of the watchdog timer is input to the reset circuit. When 262144 clock cycles have been counted, the most significant bit becomes "0" and reset is carried out. When reset is carried out, the watchdog timer is set to $7FFF_{16}$ and reset is released. The program then begins again from reset vector address. Normally, the program is written so that a writing operation is made to the watchdog timer prior to the most significant bit's becoming "0". Application of a + 10V to the $\overline{RESET}$ pin will disable the watchdog timer function.

Since execution of the STP instruction causes both the clock and the watchdog timer to stop, an option is offered where the STP instruciotn can be disabled.

RESET CIRCUIT

The M50744-XXXSP is reset according to the sequence shown in Figure 10. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 11.

An example of the reset circuit is shown in Figure 12.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

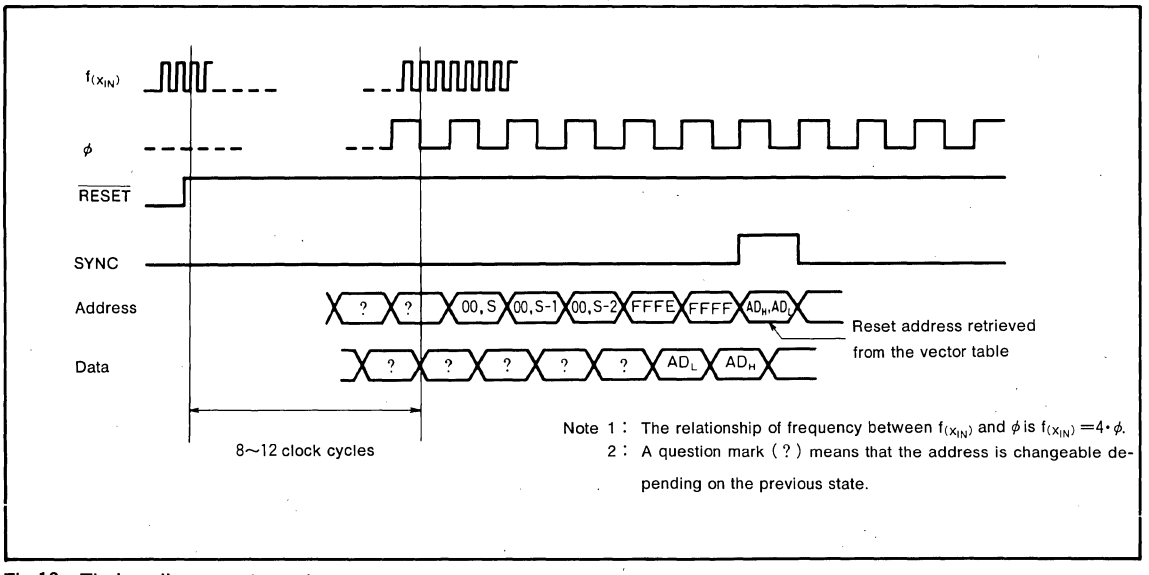


Fig.10 Timing diagram at reset

	Address	
(1) Port P0 directional register	($E1_{16}$) ···	00_{16}
(2) Port P1 directional register	($E3_{16}$) ···	00_{16}
(3) Port P2 directional register	($E5_{16}$) ···	00_{16}
(4) Port P3 directional register	($E9_{16}$) ···	00_{16}
(5) Port P4 directional register	(EB_{16}) ···	00_{16}
(6) Port 6 (Note 1)	(EE_{16}) ···	FF_{16}
(7) D-A conversion register	($F0_{16}$) ···	0 0 0 0 0
(8) Pulse width modulation register	($F1_{16}$) ···	00_{16}
(9) Watchdog timer	($F4_{16}$) ···	$7FFF_{16}$
(10) Prescaler	(FC_{16}) ···	FF_{16}
(11) Timer X	(FD_{16}) ···	01_{16}
(12) Interrupt control register	(FE_{16}) ···	00_{16}
(13) Timer control register	(FF_{16}) ···	00_{16}
(14) Processor status register (only the interrupt disable flag is set.)	(PS) ···	1
(15) Program counter	(PC_H) ···	Contents of address $FFFF_{16}$
	(PC_L) ···	Contents of address $FFFF_{16}$

Note 1 : Port P6 is the high-impedance state during reset.
After return from reset, it is "FF_{16}".

Fig.11 Internal state of microcomputer at reset

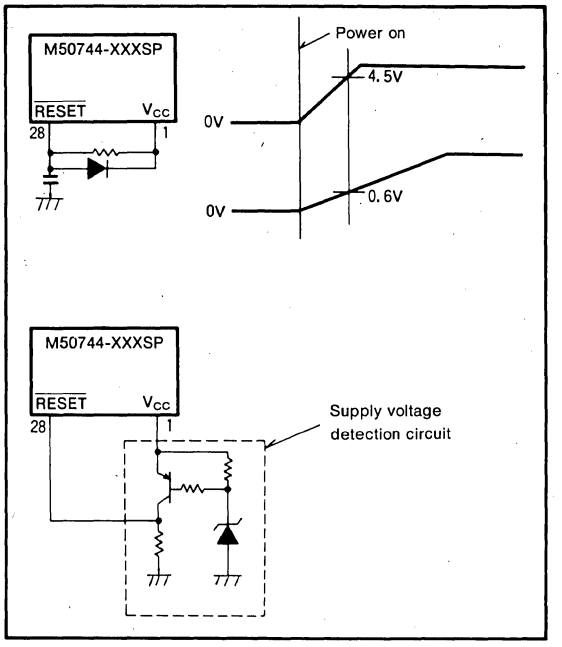


Fig.12 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slighlty different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0, but it has CMOS output. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as $\overline{INT_2}$ and I/O pins for timer X. For more details, see the processor mode information.

(5) Port P4

Port P4 has the same function as port P0 in the single-chip mode. But $P4_7$ through $P4_4$ can also be used as analog input pins AN_7 through AN_4.

(6) Port P5

Port P5 is an input port. $P5_4$ through $P5_7$ can also be used as edge sence inputs. In such a case, reading is begun from $00ED_{16}$. $00ED_{16}$ is provided with a latch which is set to "1" when the input changes from high-level to low-level. The input pulse width must be at least 7 clock cycle wide. The latch is reset by using such instructions as LDM and CLB to write a "0" to the latch. When $00ED_{16}$ is read, the lower order 4 bits are always zero.

When port P5 is used as level sence input, read the contents of the address $00EC_{16}$.

(7) Port P6

Port P6 is a 4-bit output port. It has N-channel open drain output. See Figure 13 for more details.

(8) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ.

(9) $\overline{INT_1}$ pin

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

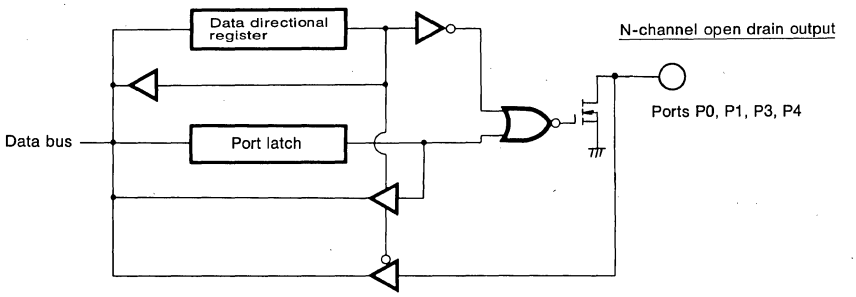
(10) $\overline{INT_2}$ pin ($P3_2/\overline{INT_2}$ pin)

The $\overline{INT_2}$ pin is an interrupt input pin used with $P3_2$. To use this pin as an interrupt pin, set the corresponding bit in the directional register to input ("0"). When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1".

(11) CNTR pin ($P3_3$/CNTR pin)

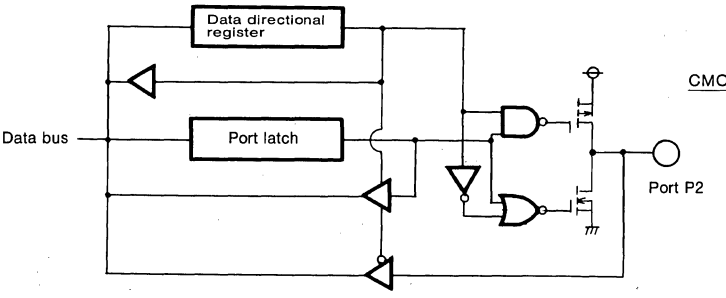
The $P3_3$/CNTR pin is an I/O pin of timer X. To use this pin as the timer X input pin, set the corresponding directional register bit to input ("0"). In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

Ports P0, P1, P3, P4

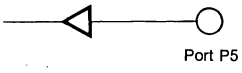


Note : P3 is used both as a timer input/output pin and an interrupt input pin.
P4 is used as an analog input pin.

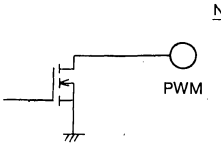
Port P2



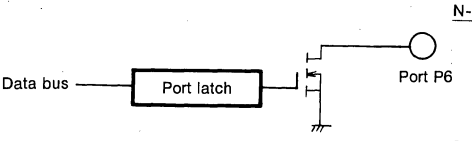
Port P5



PWM



Port P6



ϕ

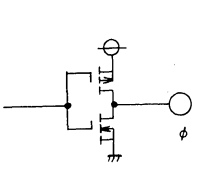


Fig.13 Block diagram of port P0~P6 (single-chip mode) and ϕ output format

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 15 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 14.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

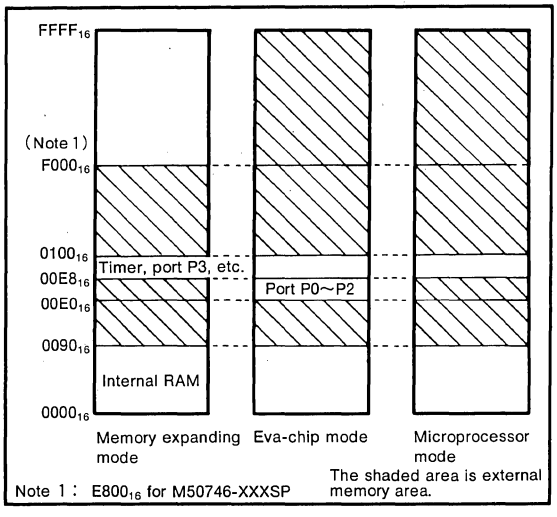


Fig.14 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost. Port P2 becomes the data bus of D_7～D_0 (including instruction code) and loses its normal I/O functions. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively when ϕ enters into the "H" state. Port $P3_2$ functions as an input port during this same transition.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode.

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the databus (D_7～D_0) and loses its normal I/O functions. Port $P3_1$ and $P3_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is requierd.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original I/O functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

Port \ Mode	Single-chip mode	Eva-chip mode	Memory expanding mode	Microprocessing mode
	CM_1 = 0, CM_0 = 0	CM_1 = 1, CM_0 = 1	CM_1 = 0, CM_0 = 1	CM_1 = 1, CM_0 = 0
Port P0	Ports $P0_7$~$P0_0$: I/O port	Ports $P0_7$~$P0_0$: Address A_7~A_0 / I/O port	Ports $P0_7$~$P0_0$: Address A_7~A_0	Same as left
Port P1	Ports $P1_7$~$P1_0$: I/O port	Ports $P1_7$~$P1_0$: Address A_{15}~A_8 / I/O port	Ports $P1_7$~$P1_0$: Address A_{15}~A_8	Same as left
Port P2	Ports $P2_7$~$P2_0$: I/O port	Ports $P2_7$~$P2_0$: Output port / Data D_7~D_0	Ports $P2_7$~$P2_0$: Data D_7~D_0	Same as left
Port P3	Ports $P3_7$~$P3_0$: I/O port	Ports $P3_7$~$P3_2$: I/O port; Port $P3_1$: SYNC / I/O port; Port $P3_0$: R/$\overline{W}$ / I/O port	Ports $P3_7$~$P3_2$: I/O port; Port $P3_1$: SYNC; Port $P3_0$: R/$\overline{W}$	Same as left

Fig.15 Processor mode and functions of Ports P0~P3

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 18.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleard when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 16.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

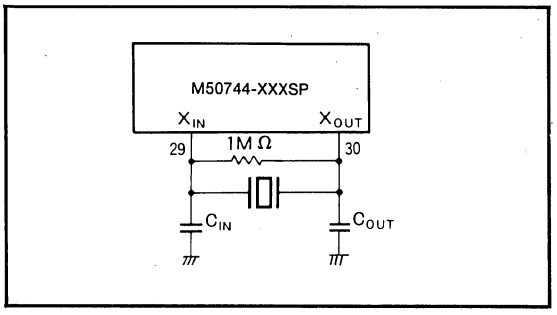


Fig.16 External ceramic resonator circuit

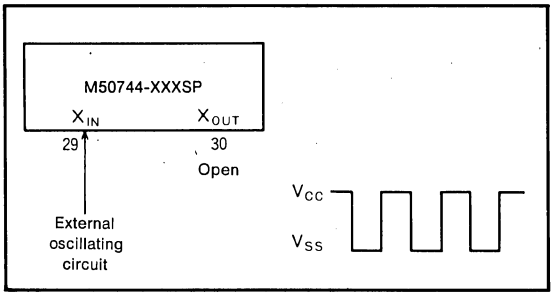


Fig.17 External clock input circuit

The example of external clock uasge is shown in Figure 17. X_{IN} is the input, and X_{OUT} is open.

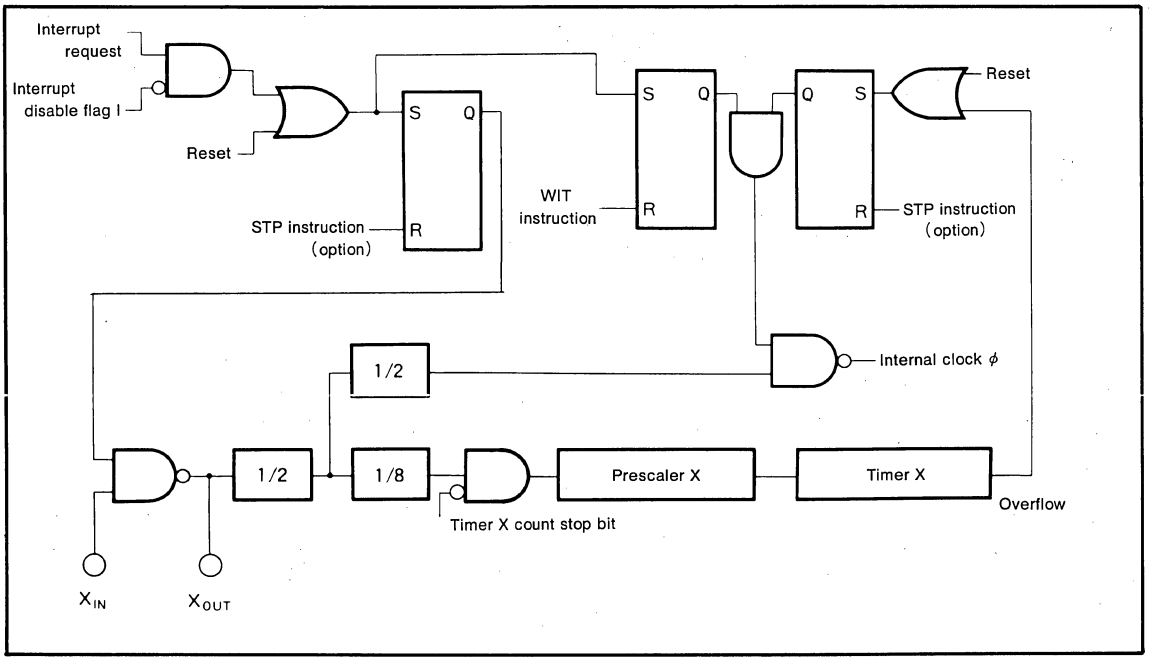


Fig.18 Block diagram of the clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(5) A NOP instruction must be used after the execution of a PLP instruction.
(6) Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed lager than 1MHz during A-D conversion. And during A-D conversion, don't use STP or WIT instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ..... EPROM 3sets
Write the following option on the mask ROM confirmation form
• STP instruction option

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} With the output transistor cut-off	−0.3∼7	V
V_I	Input voltage X_{IN}		−0.3∼7	V
V_I	Input voltage $P2_0$∼$P2_7$, $P4_4$∼$P4_7$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, $P5_0$∼$P5_7$, $\overline{INT_1}$		−0.3∼13	V
V_I	Input voltage CNV_{SS}, $\overline{RESET}$		−0.3∼13	V
V_O	Output voltage $P2_0$∼$P2_7$, $P4_4$∼$P4_7$, X_{OUT}, ϕ, D-A		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, $P6_0$∼$P6_3$, PWM		−0.3∼13	V
P_d	Power dissipation	T_a=25℃	1000(Note 1)	mW
T_{opr}	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : 300mW for QFP types

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, PWM (Note 3)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$∼$P6_3$ (Note 3)			15	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, PWM (Note 2)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0$∼$P6_3$ (Note 2)			7	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$∼$P2_7$ (Note 3)			−10	mA
$I_{OH(avg)}$	"H" average output current $P2_0$∼$P2_7$ (Note 2)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillator frequency			4	MHz

Note 2 : The average output currents $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
3 : Do not allow the combined low- level output current of ports P0, P1, P2, P3, P4, P6, and PWM to exceed 80mA.
Do not allow the combined high- level output current of port P2 to exceed 50mA.
4 : "H" input voltage of ports' P0, P1, P3, $P4_0$∼$P4_3$, P5 and $\overline{INT_1}$ is available up to +12V.

ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=5V, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P2_0$~$P2_7$	I_{OH}=−10mA		3			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA		3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_3$, PWM	I_{OL}=10mA				2	V
V_{OL}	"L" output voltage ϕ	I_{OL}=5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$	When used as $\overline{INT_2}$ input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_3$	When used as CNTR input		0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}			0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=0V				−5	μA
I_{IL}	"L" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I=0V				−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=12V				12	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, $P2_0$~$P2_7$, $P4_4$~$P4_7$	V_I=5V				5	μA
V_{RAM}	RAM retention voltage	When clock disabled		2			V
I_{CC}	Supply current	ϕ, X_{OUT}, and D-A pins opened, other pins at V_{SS}, and A-D converter in the finished condition.	$f_{(X_{IN})}$=4MHz Square wave		3	6	mA
			at clock stop T_a=25°C			1	μA
			at clock stop T_a=75°C			10	μA

A-D CONVERTER CHARACTERISTICS (T_a=25°C, V_{CC}=5V, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute precision	V_{REF}=V_{CC}, with the output transistor cut-off			±3	LSB
R_{LADDER}	Ladder resistance	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS (T_a=25°C, V_{CC}=5V, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			5	Bits
—	Error in full scale range	V_{REF}=V_{CC}, with the output transistor cut-off			±1	%
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
R_O	Output resistance	V_{REF}=V_{CC}			3	kΩ
V_{REF}	Reference voltage		4		V_{CC}	V

TIMING REQUIREMENTS

Single-chip mode (T_a=25℃, V_{CC}=5V±10%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	270			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time	20			ns
t_c	External clock input cycle time	250			ns
t_w	External clock input pulse width	75			ns
t_r	External clock rise-time			25	ns
t_f	External clock fall-time			25	ns

Eva-chip mode (T_a=25℃, V_{CC}=5V±10%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Memory expanding and microprocessor modes

(T_a=25℃, V_{CC}=5V±10%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	30			ns

SWITCHING CHARACTERISTICS

Single-chip mode (T_a=25℃, V_{CC}=5V±10%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 19			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 20			230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig. 19			230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				230	ns

Eva-chip mode (T_a=25℃, V_{CC}=5V±10%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 19			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 20			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig. 19			250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns

Memory expanding and microprocessor modes

(T_a=25℃, V_{CC}=5V±10%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 19			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 20			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig. 19			250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

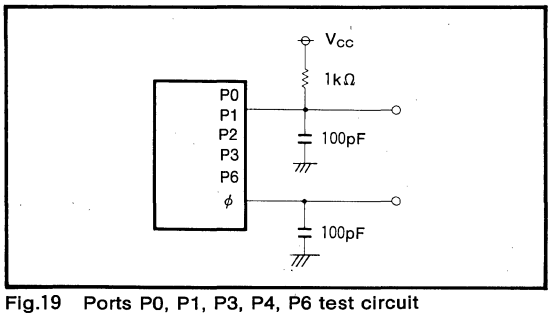


Fig.19 Ports P0, P1, P3, P4, P6 test circuit

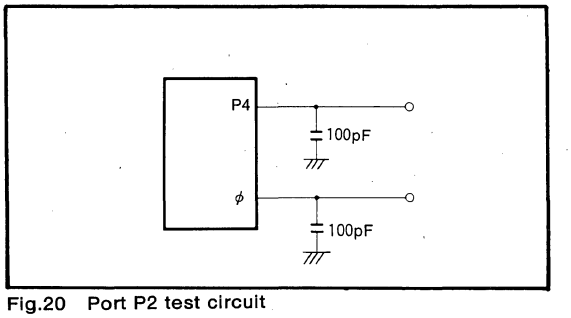
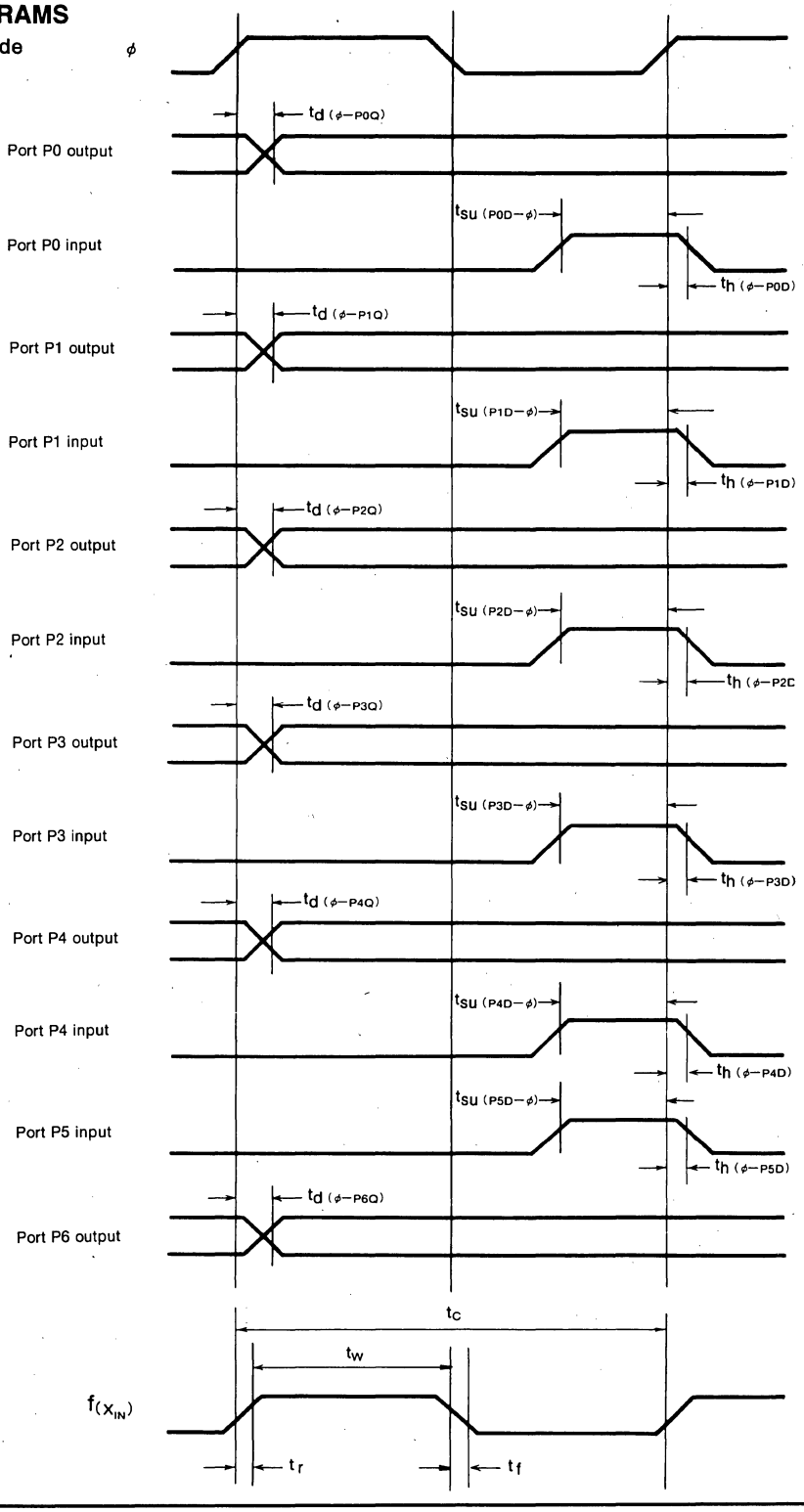


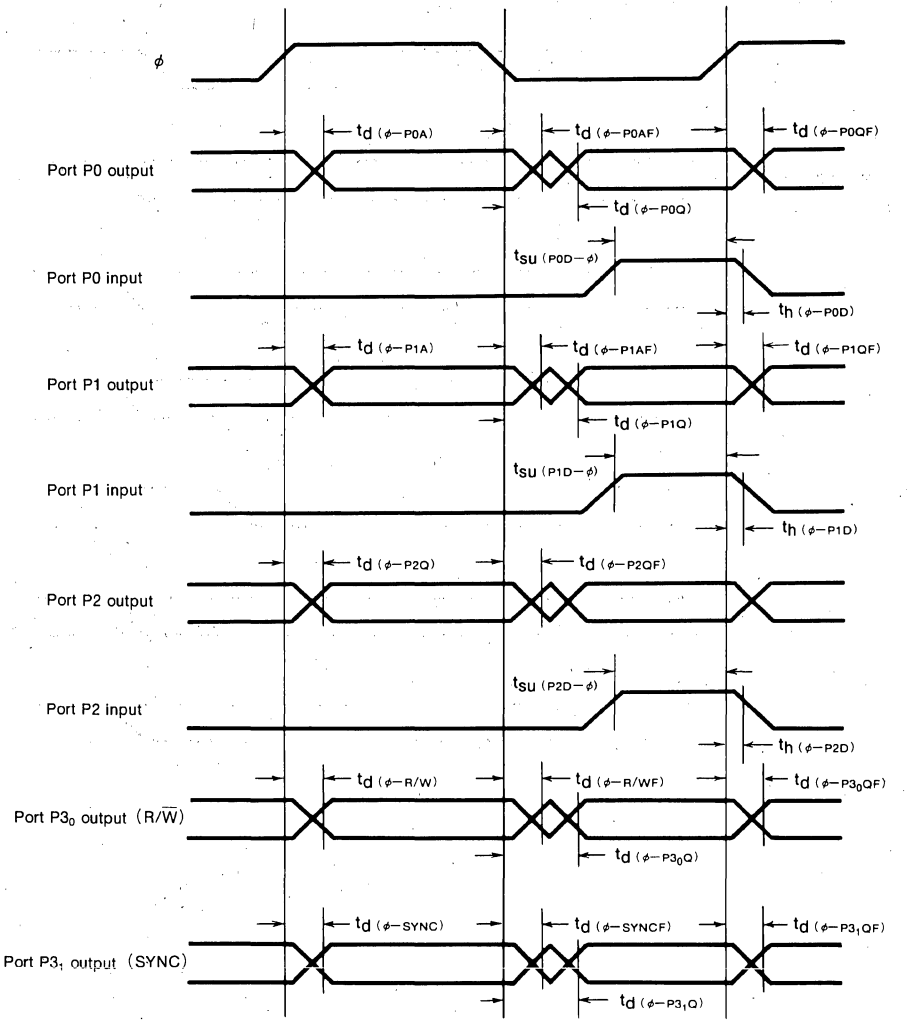
Fig.20 Port P2 test circuit

TIMING DIAGRAMS

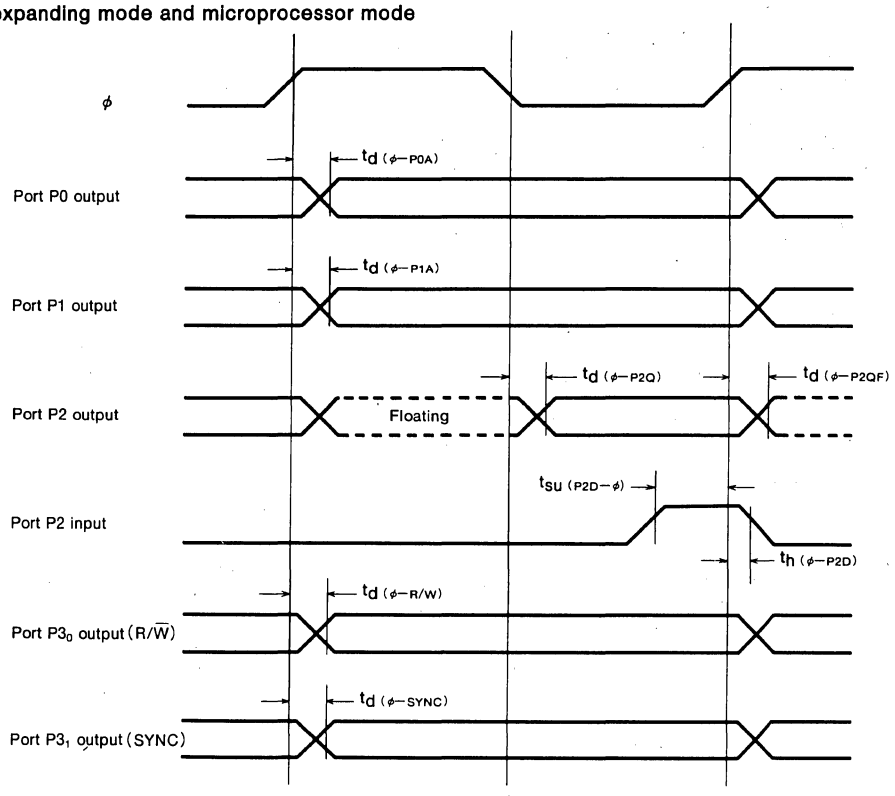
In single-chip mode



In eva-chip mode



In memory expanding mode and microprocessor mode



M50745-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50745-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP (flat package type also available). This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50745-XXXSP and the M50745-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

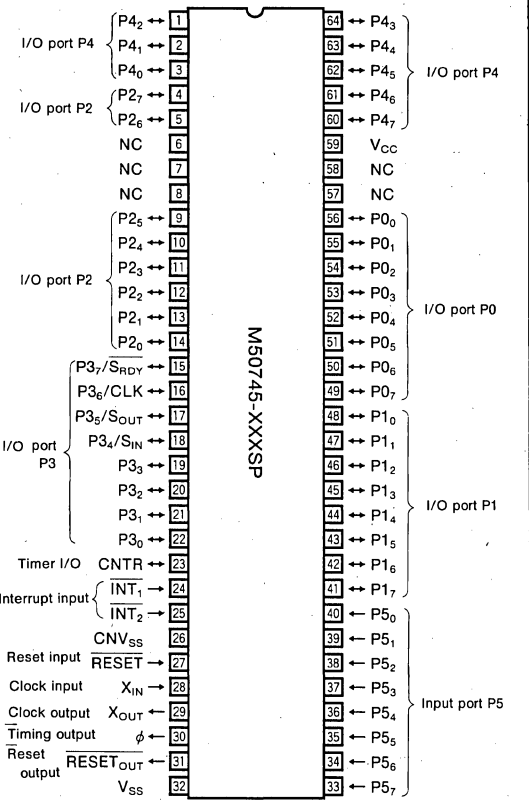
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 6144 bytes
  RAM ..... 192 bytes
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz ..... 5V±10%
- Power dissipation
  normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 7 types, 5 vecters
- 8-bit timer ..... 3 (2 when used as serial I/O)
- Programmable I/O (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Serial I/O (8-bit) 1

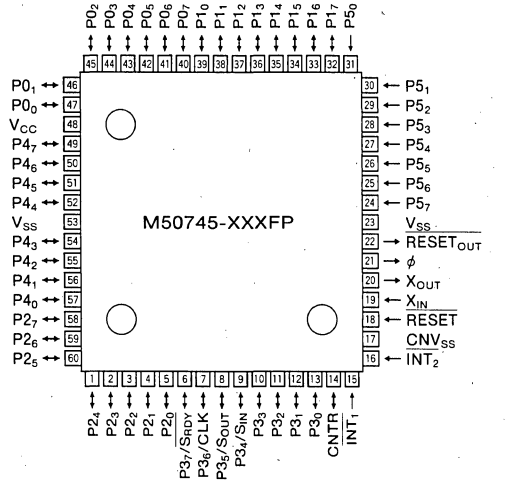
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

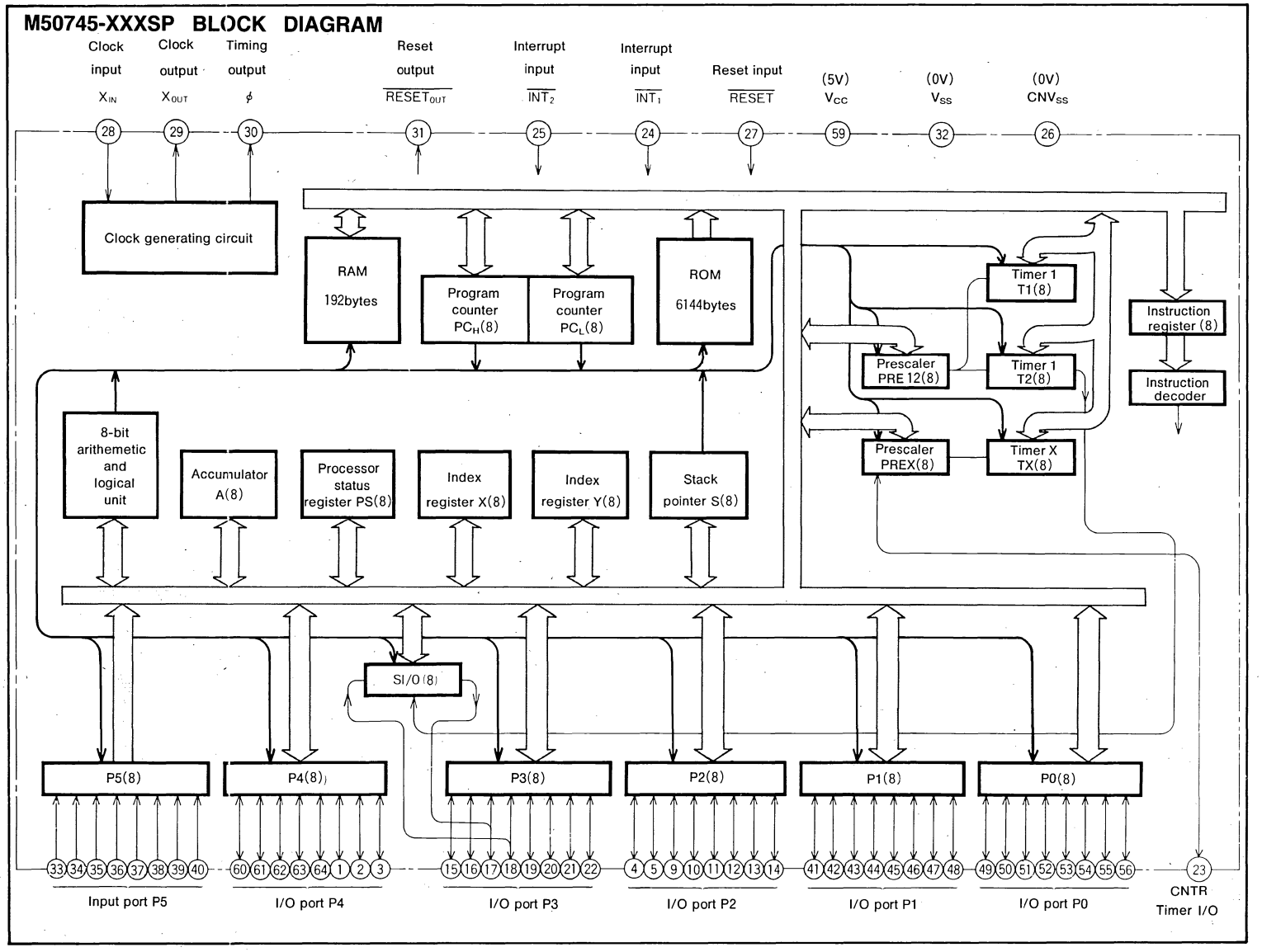


Outline 60P6

NC : No connection

MITSUBISHI ELECTRIC

M50745-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M50745-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (Minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory size	ROM		6144bytes
	RAM		192bytes
Input/Output port	$\overline{INT_1}$, $\overline{INT_2}$	Input	1-bit×2
	P0, P1, P2, P3, P4	I/O	8-bit×5 (Part of P3 are in common with serial I/O)
	P5	Input	8-bit×1
	CNTR	I/O	1-bit×1
Serial I/O			8-bit×1
Timers			8-bit prescaler×2+8-bit timer×3 (2 when serial I/O is used)
Subroutine nesting			96 levels (max.)
Interrupts			two external interrupts, three timer interrupts (or timer×2, serial I/O×1)
Clock generating circuit			Built-in (ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	At high-speed operation		15mW (at 4MHz frequency)
Input/Output characteristics	Input/Output voltage		12V (Ports P0, P1, P2, P3, P4, P5, $\overline{INT_1}$, $\overline{INT_2}$, CNTR)
	Output current		5mA (Ports P0, P1, P2, P3, P4)
Memory expansion			Possible
Operating temperature range			−10∼70℃
Device structure			CMOS silicon gate process
Package	M50745-XXXSP		64-pin shrink plastic molded DIP
	M50745-XXXFP		60-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an output pin for the timer X.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$\overline{INT_2}$	Interrupt input	Input	This is the lowest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is P-channel open drain.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
$\overline{RESET_{OUT}}$	Reset output	Output	This pin outputs the reset signal for peripheral devices.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50745-XXXSP is shown in Figure 1. Addresses $E800_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 6144 bytes.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $00BF_{16}$ are assigned to the built-in RAM and consist of 192 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

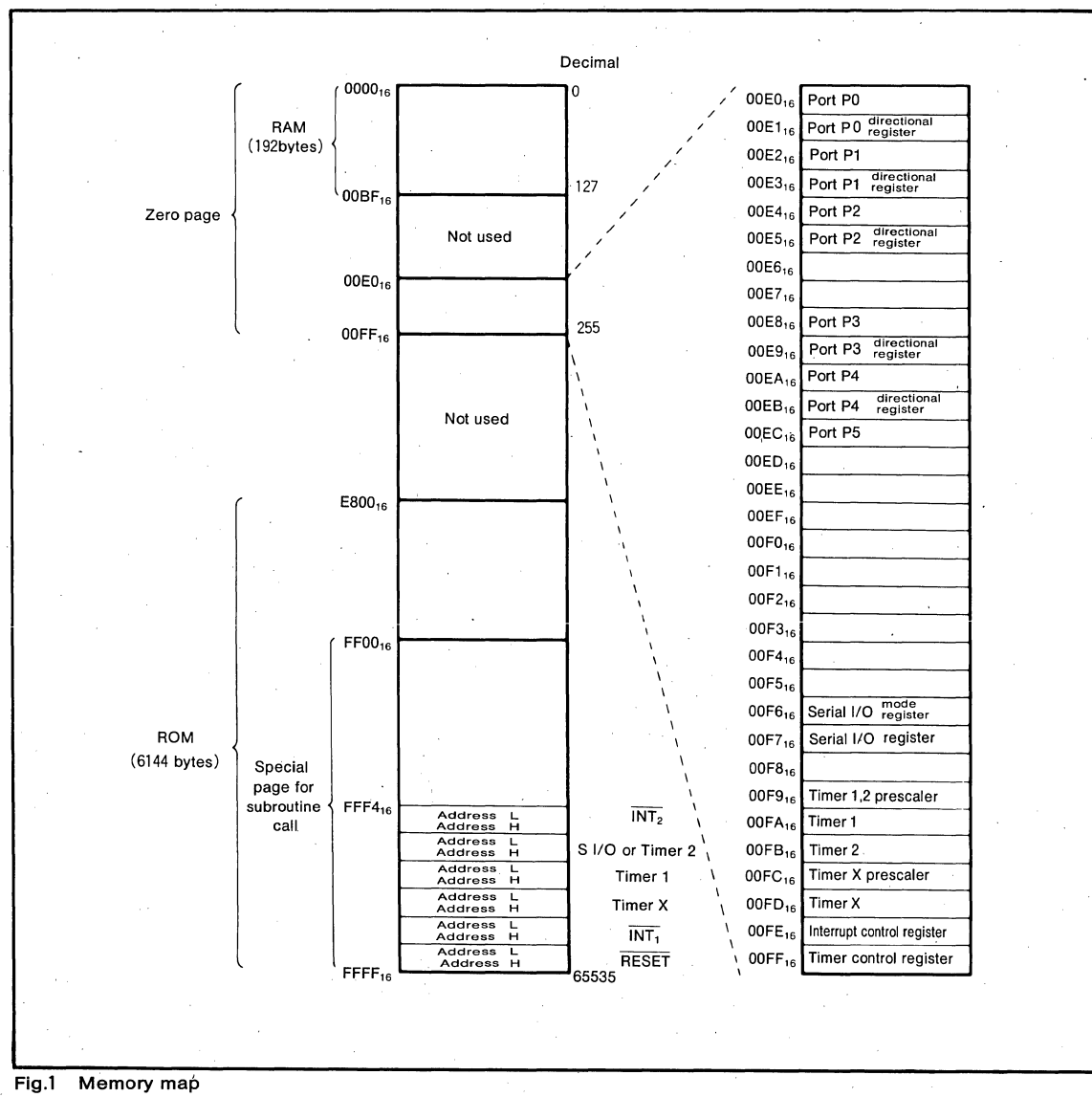


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

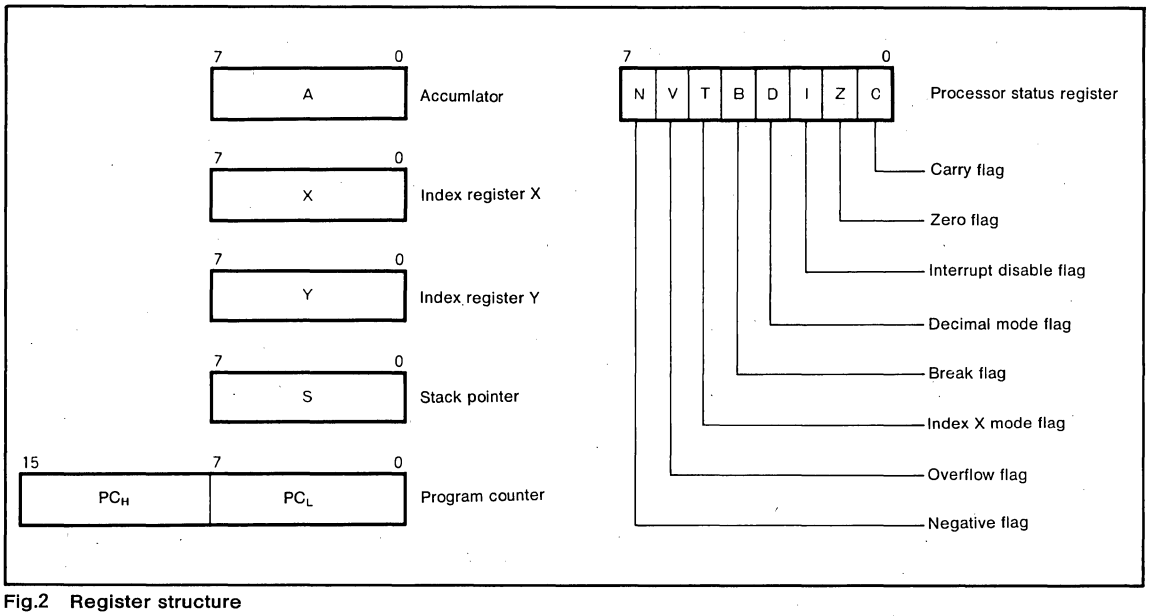


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The location of the stack can be determined by the stack page bit (bit 4 at address $00FF_{16}$). When bit 4 is "0" and the contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When bit 4 is "1", the stack address is set to $01XX_{16}$. When using this microcomputer in the single-chip mode, the stack page bit must be "0" and the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{\text{INT}_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1	4	$FFF9_{16}$, $FFF8_{16}$
Timer 2 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{\text{INT}_2}$ (BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50745-XXXSP can be interrupted from seven souces; $\overline{\text{INT}_1}$, timer X, timer 1, timer 2/serial I/O, or $\overline{\text{INT}_2}$/BRK instruction.

The value of bit 2 of the serial I/O mode register (address $00F6_{16}$) determine whether the interrupt is from timer 2 or from serial I/O. When bit 2 is "0" the interrupt is from timer 2, and when bit 2 is "1" the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3.

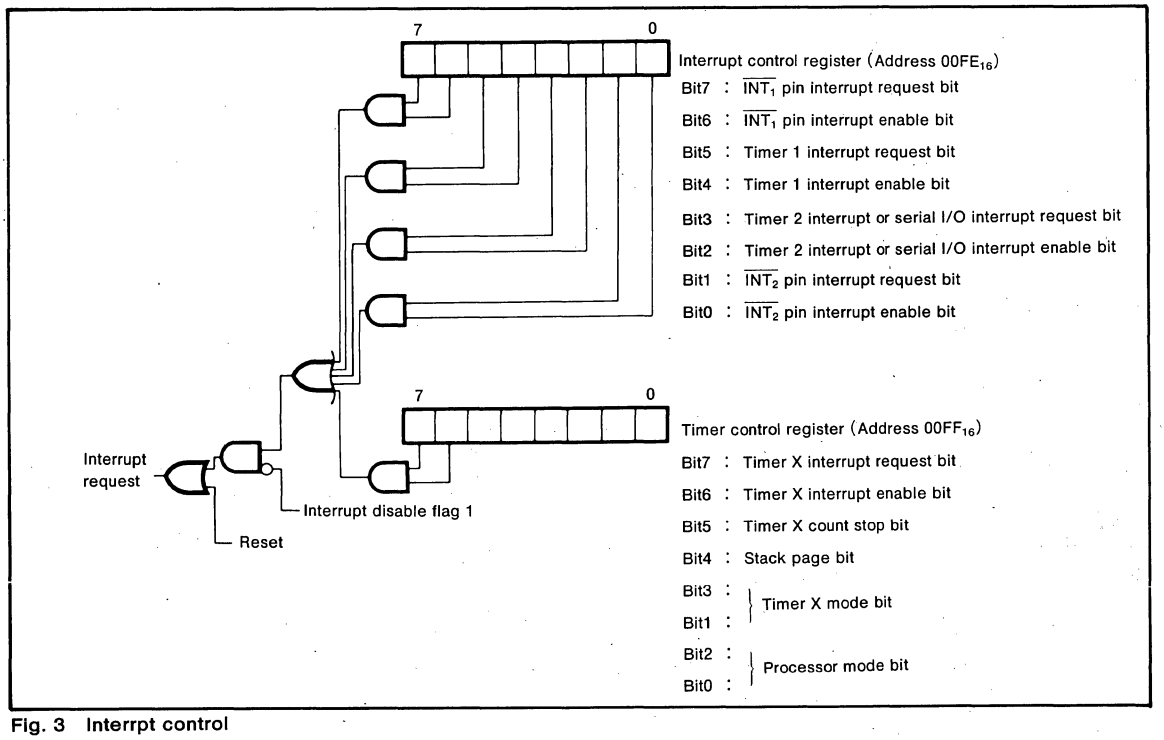


Fig. 3 Interrpt control

An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"

(2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

TIMER

The M50745-XXXSP has three timers; timer X, timer 1, and timer 2. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section). Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1 and timer 2 is shown in Figure 4.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+2)$, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

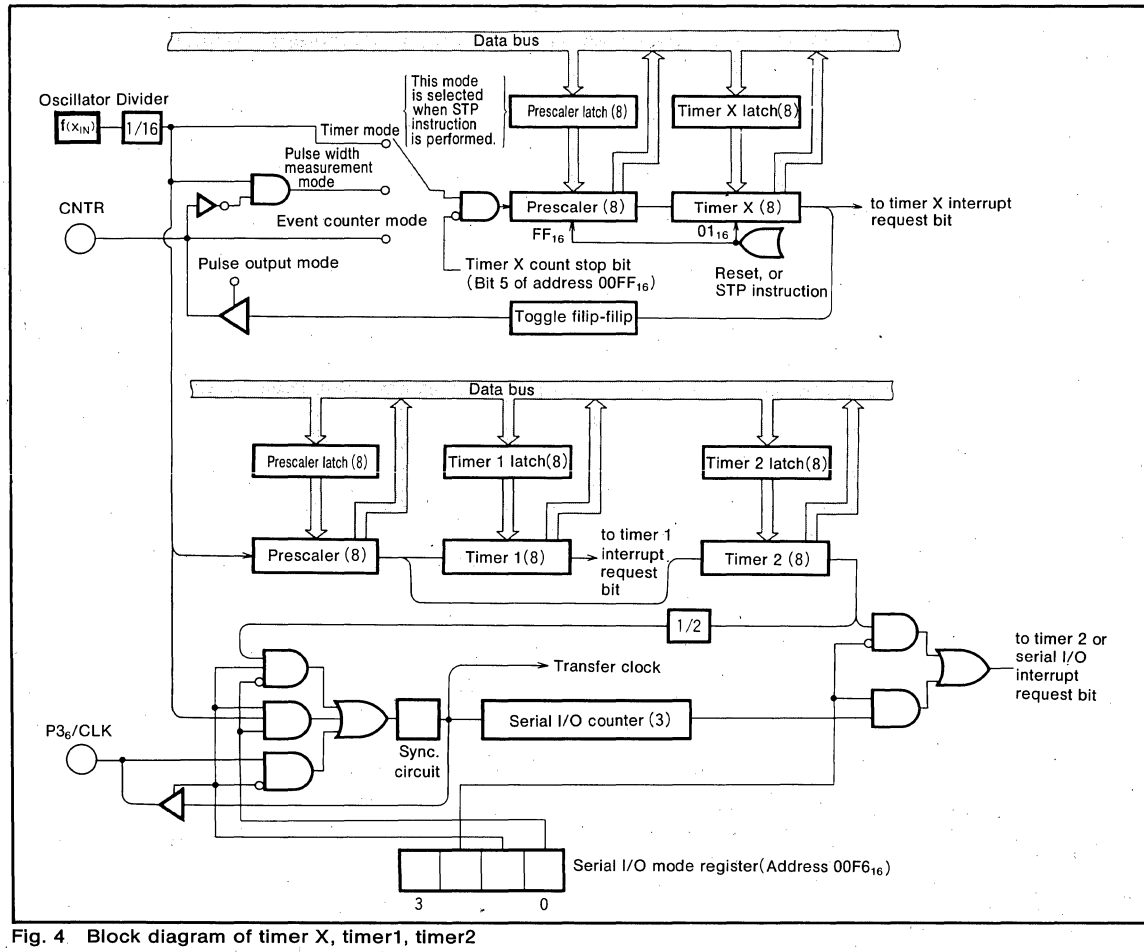


Fig. 4 Block diagram of timer X, timer1, timer2

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section). The prescaler latch and timer latch can be loaded with any number except zero.

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

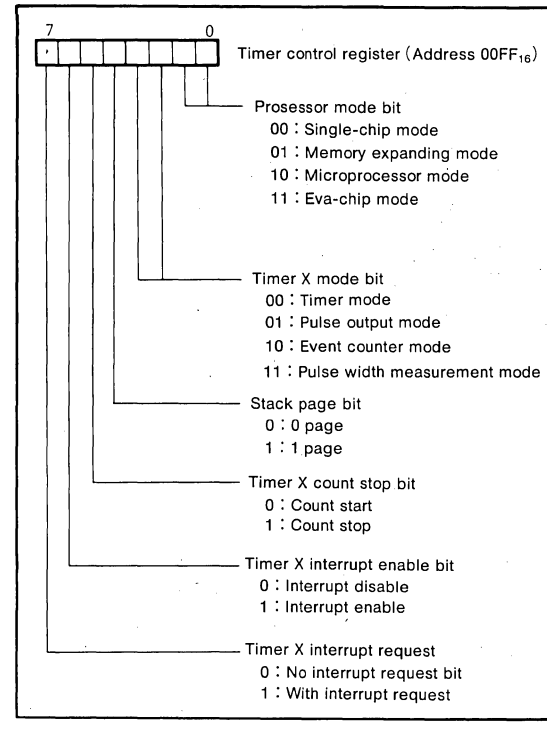
(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock sourse.

(4) Pulse width measurement mode [11]
This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.



SERIAL I/O

A block diagram of the serial I/O is shown in Figure 6.

In the serial I/O mode the receive raady signal ($\overline{S_{RDY}}$), synchronous input /output clock (CLK), and the serial I/O pins (S_{OUT}, S_{IN}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F6_{16}$) is 4-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 2, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], oscillator frequency divided by 16, becomes the clock.

Bit 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is a "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on

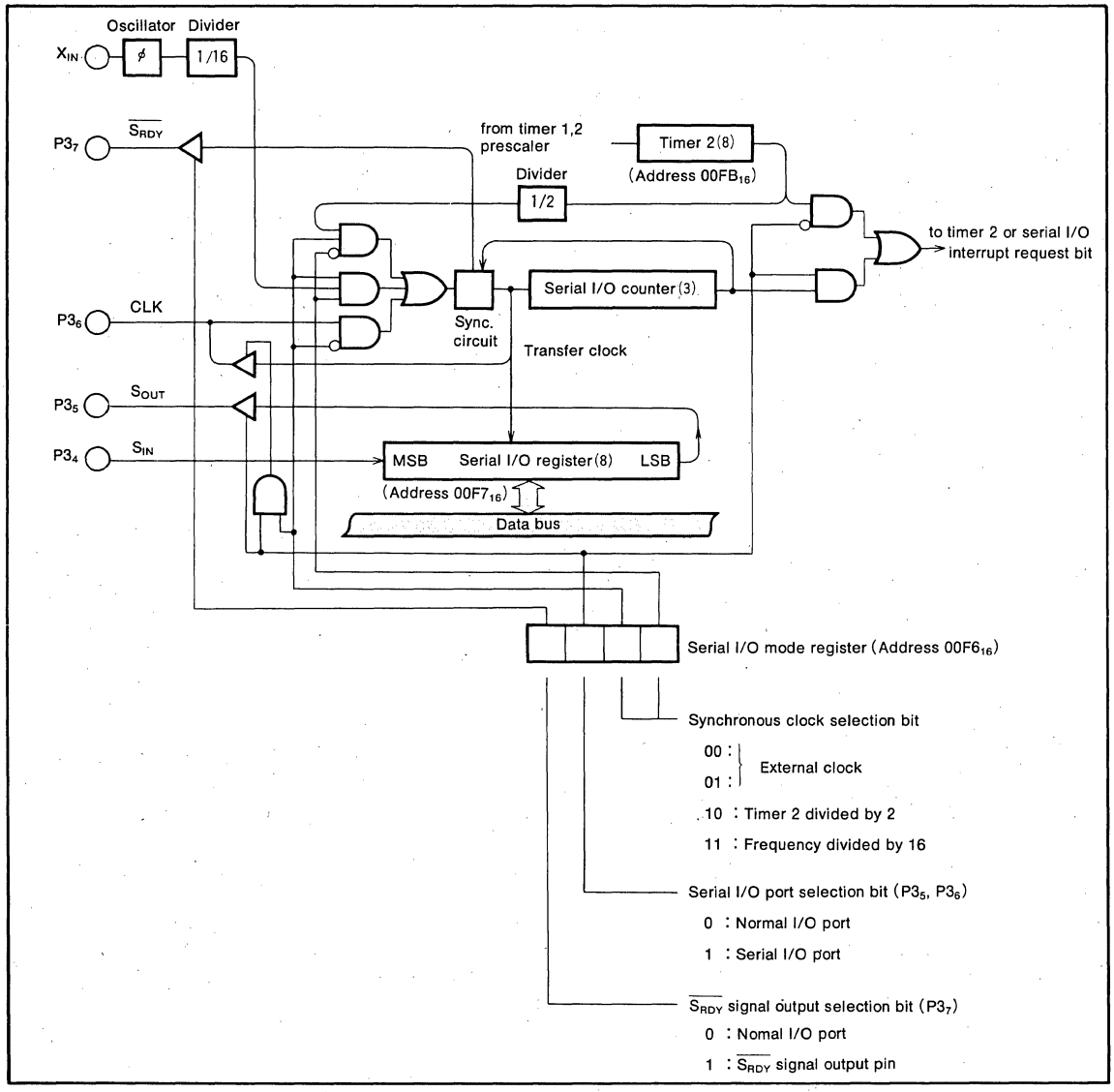


Fig.6 Block diagram of serial I/O

the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 2. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3=1, $\overline{S_{RDY}}$) or used as normal I/O pin (bit 3=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address $00F7_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50745-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes to "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrpt request bit will be set.

External Clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 7. An example of communication between two M50745-XXXSPs is shown in Figure 8.

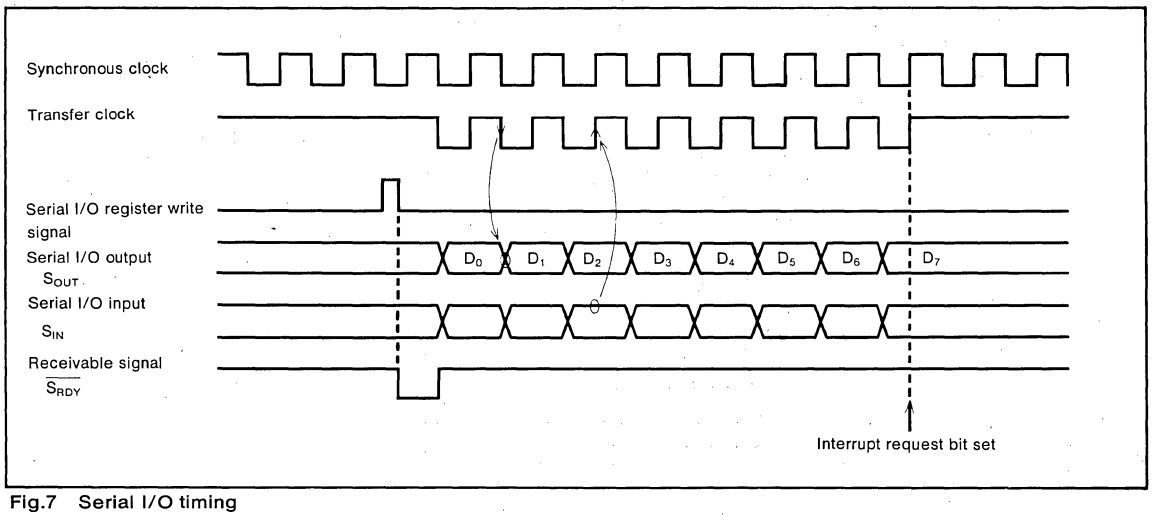


Fig.7 Serial I/O timing

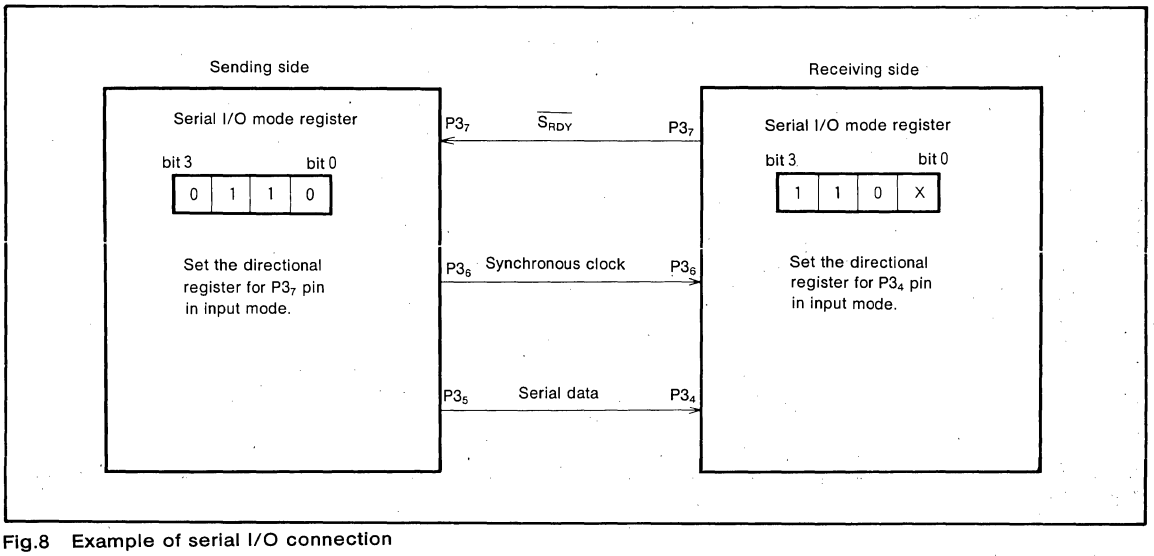


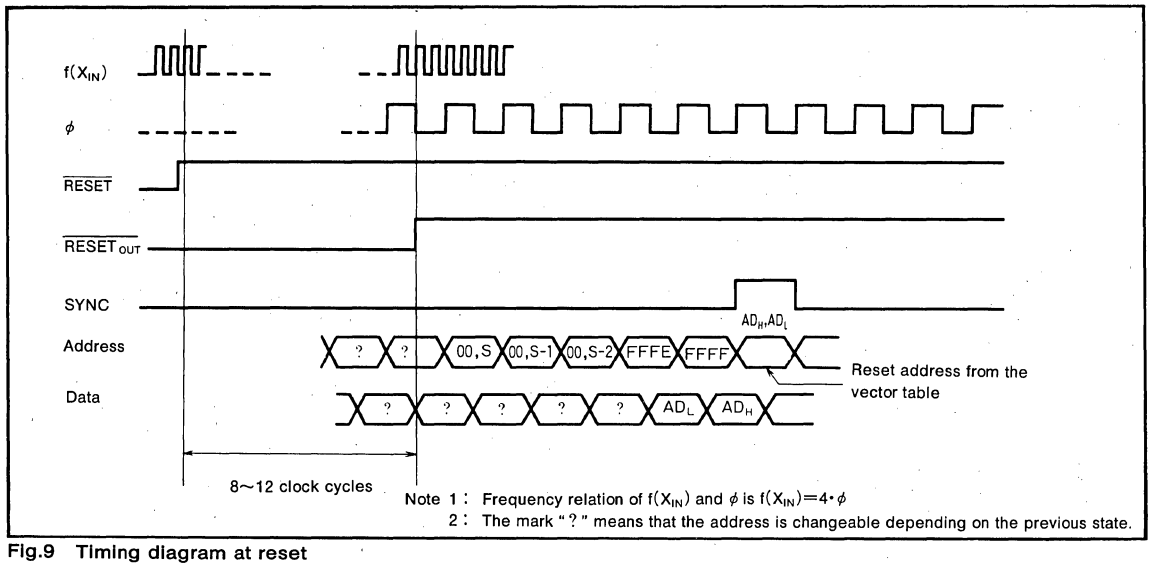
Fig.8 Example of serial I/O connection

RESET CIRCUIT

The M50745-XXXSP is reset according to the sequence shown in Figure 9. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 10.

An example of the reset circuit is shown in Figure 11.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.



Note 1 : Frequency relation of $f(X_{IN})$ and ϕ is $f(X_{IN})=4\cdot\phi$
2 : The mark "?" means that the address is changeable depending on the previous state.

Fig.9 Timing diagram at reset

	Address	
(1) Port P0 directional register	($E1_{16}$) ···	00_{16}
(2) Port P1 directional register	($E3_{16}$) ···	00_{16}
(3) Port P2 directional register	($E5_{16}$) ···	00_{16}
(4) Port P3 directional register	($E9_{16}$) ···	00_{16}
(5) Port P4 directional register	(EB_{16}) ···	00_{16}
(6) Serial I/O mode register	($F6_{16}$) ···	0 0 0 0
(7) Prescaler X	(FC_{16}) ···	FF_{16}
(8) Timer X	(FD_{16}) ···	01_{16}
(9) Interrupt control register	(FE_{16}) ···	00_{16}
(10) Timer control register	(FF_{16}) ···	00_{16}
(11) Interrupt disable flag on processor status register	(PS) ···	1
(12) Program counter	(PC_H) ···	Contents of address $FFFF_{16}$
	(PC_L) ···	Contents of address $FFFE_{16}$

Fig.10 Internal state of microcomputer at reset

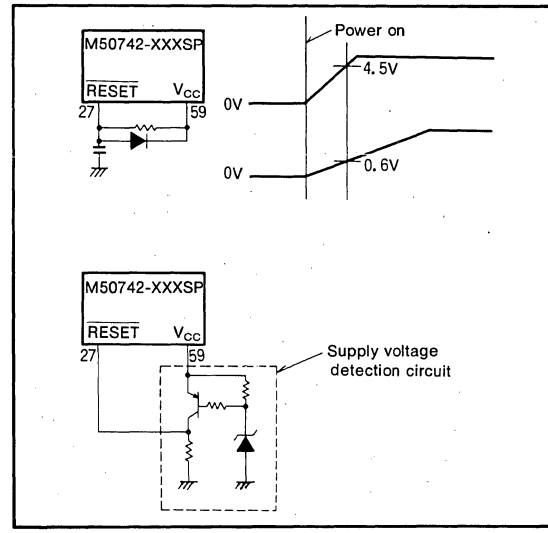


Fig.11 Example of reset circuit

MITSUBISHI ELECTRIC

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

Pull-up transistor can be specified as an option. As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as serial I/O pins. For more details, see the processor mode information.

(5) Port P4

Port P4 is an 8-bit I/O port with P-channel open drain outputs. This port also has the pull-down transistor option.

(6) Port P5

Port P5 is and input port with pull-up transistor option. See Figure 12 for more details.

(7) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ.

(8) $\overline{RESET_{OUT}}$ pin

When the $\overline{RESET}$ pin goes to level "L", the $\overline{RESET_{OUT}}$ pin also goes to "L". On the other hand, when the $\overline{RESET}$ pin goes to level "H", the $\overline{RESET_{OUT}}$ pin also goes to "H" after 8 clock cycles. This output is used to reset the external circuits.

(9) $\overline{INT_1}$ pin

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

(10) $\overline{INT_2}$ pin

The $\overline{INT_2}$ pin is an interrupt input pin. When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1".

(11) CNTR pin

The CNTR pin is an I/O pin of timer X. In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

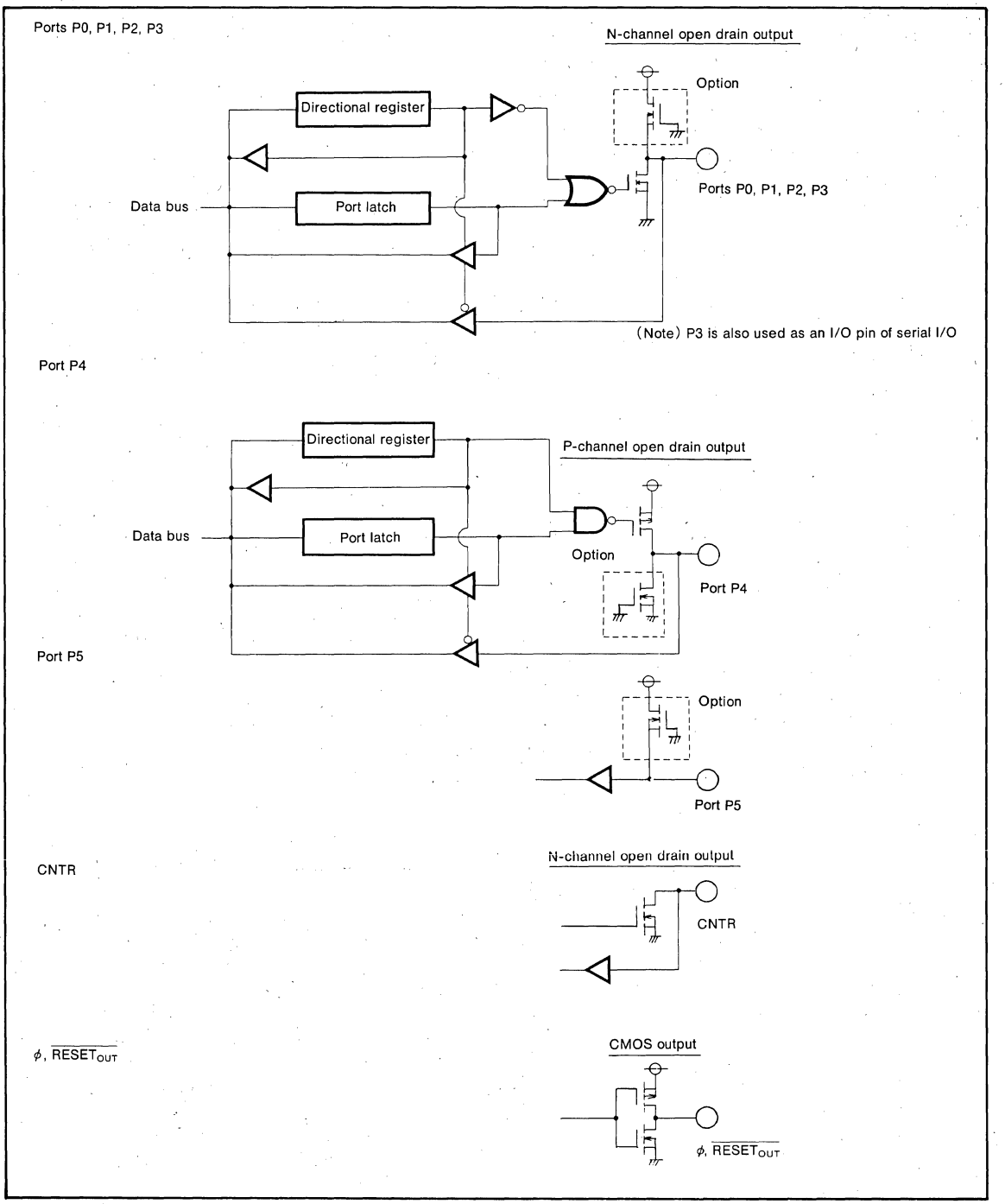


Fig.12 Block diagram of port P0~P6 (single-chip mode) and output format of ϕ

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 14 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 13.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

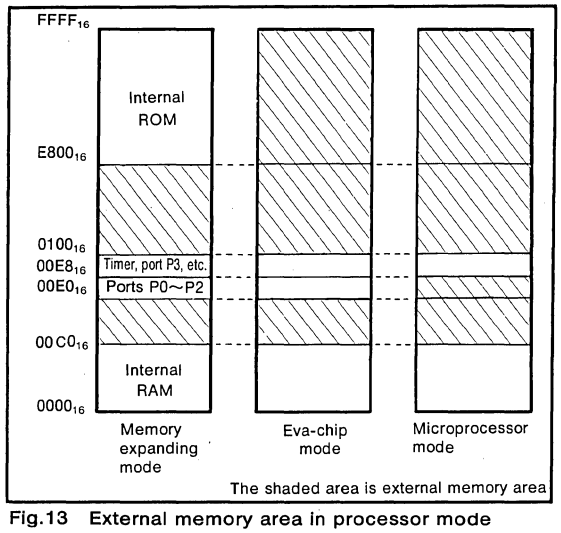


Fig.13 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state, and $\overline{RDY}$ signal is input from $P3_2$ pin. When in the "L" state, $P3_2$, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The $\overline{RDY}$ is ready signal input and, when it goes to "L", internal clock stops and the CPU waits the data. However, the oscillation does not stop.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode.

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the data bus (D_7～D_0) and loses its normal I/O functions. Port $P3_2$, $P3_1$ and $P3_0$ become the $\overline{RDY}$, SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is requierd.

This mode has almost the same function as the memory expanding mode except that it needs to attach all program memories to the outside.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

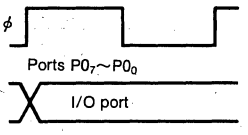
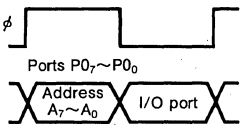
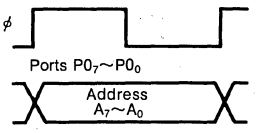
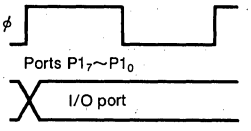
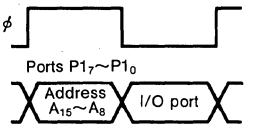
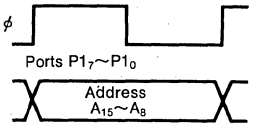
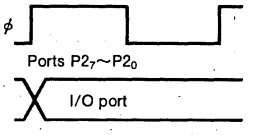
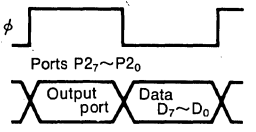
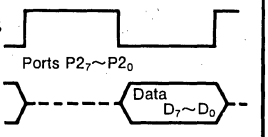
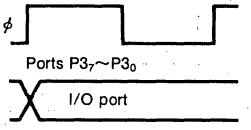
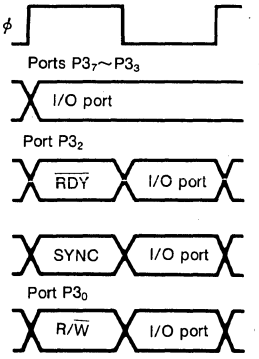
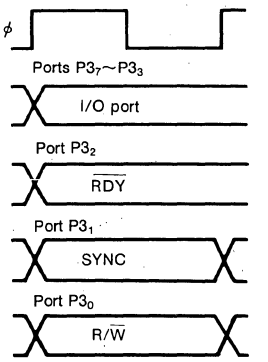
Port \ Mode	Single-chip mode	Memory expanding mode	Eva-chip mode	Microprocessor mode
CM_1	0	0	1	1
CM_0	0	1	1	0
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	
Port $P3_2$			Same as left	

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 17.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleard when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 15.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock uasge is shown in Figure 16. X_{IN} is the input, and X_{OUT} is open.

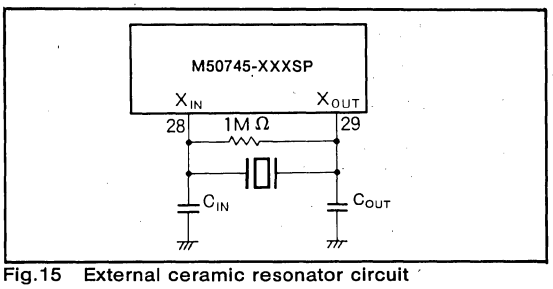


Fig.15 External ceramic resonator circuit

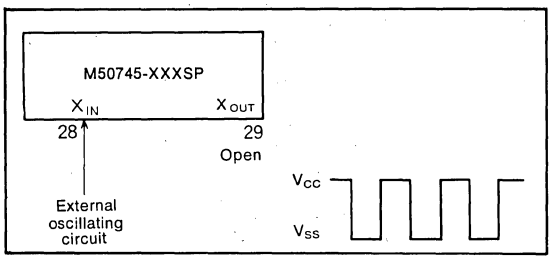


Fig.16 External clock input circuit

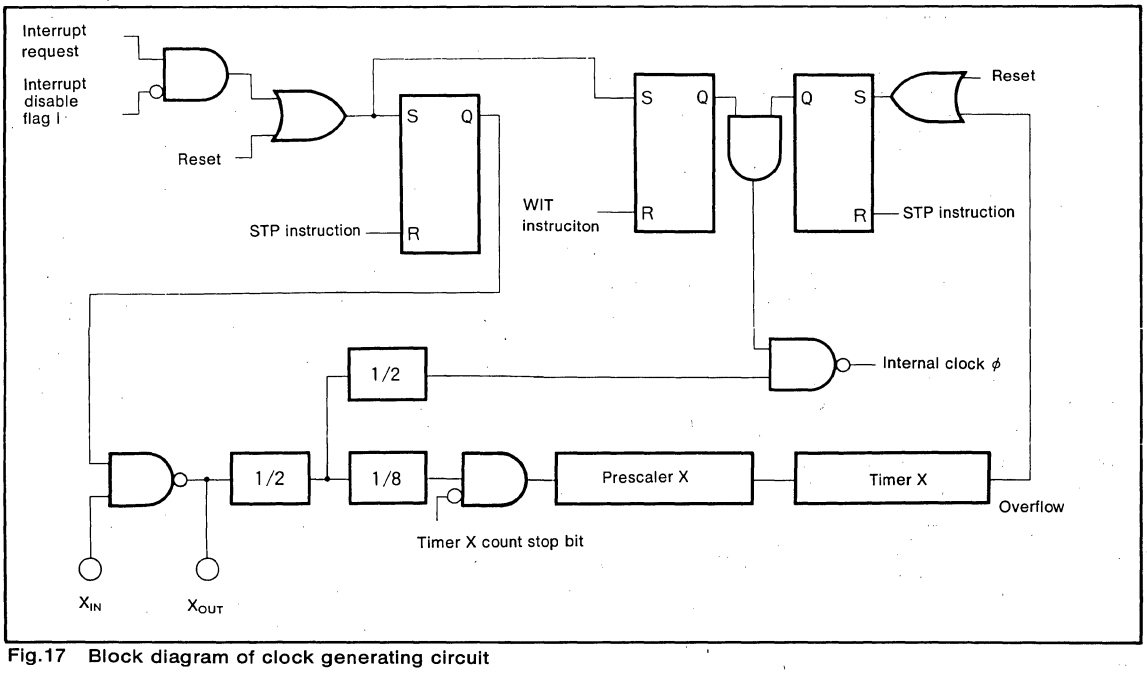


Fig.17 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+2).
(2) Set a value other than "0" for the timer and the prescaler.
(3) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(4) Reading the timer and prescaler must be abvoided while the input to the prescaler is changing.
(5) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(6) A NOP instruction must be used after the execution of a PLP instruction.
(7) Notes on serial I/O
① Set "0" in the serial I/O interrupt enable bit (bit 2 of address $00FE_{16}$) before setting the serial I/O mode.
② Insert at least one instruction and set "0" in the serial I/O interrupt request bit (bit 3 of address $00FE_{16}$) after setting the serial I/O mode.
③ Set "1" in the serial I/O interrupt enable bit after the operation described in ②.
(8) The timer X and prescaler X must be set "FF_{16}" immediately before the execution of a STP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ····· EPROM 3sets

Write the following option on the mask ROM confirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port P4 pull-down transistor bit
- Port P5 pull-up transistor bit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors are in "off" state.	−0.3~7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}		−0.3~7	V
V_I	Input voltage, $P4_0$~$P4_7$		−0.3~V_{CC}+0.3	V
V_I	Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}		−0.3~13	V
V_O	Output voltage, $P4_0$~$P4_7$, X_{OUT}, ϕ, $\overline{RESET_{OUT}}$		−0.3~V_{CC}+0.3	V
V_O	Output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR		−0.3~13	V
P_d	Power dissipation	T_a = 25℃	1000 (Note 1)	mW
T_{opr}	Operating temperature		−10~70	℃
Tstg	Storage temperature		−40~125	℃

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (T_a = −10~70℃, V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current, $P0_0$ ~ $P0_7$, $P1_0$ ~ $P1_7$, $P2_0$ ~ $P2_7$, $P3_0$ ~ $P3_7$, CNTR			10	mA
$I_{OL(avg)}$	"L" averaged output current, $P0_0$ ~ $P0_7$, $P1_0$ ~ $P1_7$, $P2_0$ ~ $P2_7$, $P3_0$ ~ $P3_7$, CNTR, (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current, $P4_0$ ~ $P4_7$			−10	mA
$I_{OH(avg)}$	"H" averaged output current, $P4_0$ ~ $P4_7$ (Note 2)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

Note 2 : $I_{OL(avg)}$, $I_{OH(avg)}$ is the average current in 100ms.
3 : "H" input voltage of ports P0, P1, P2, P3, and P5, CNTR, $\overline{INT_1}$ and $\overline{INT_2}$ is available up to +12V. (For ports, it is only when pull-up transistor is omitted.)
4 : The total of $I_{OL(peak)}$ of ports P0, P1, P2, and P3 should be 80mA max.
The total of $I_{OH(peak)}$ of port P4 should be 80mA max.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage, $P4_0$~$P4_7$	I_{OH} = −10mA		3			V
V_{OH}	"H" output voltage, ϕ, $\overline{RESET_{OUT}}$	I_{OH} = −2.5mA		3			V
V_{OL}	"L" output voltage, $P0_0$~ $P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR	I_{OL} = 10mA				2	V
V_{OL}	"L" output voltage, ϕ, $\overline{RESET_{OUT}}$	I_{OL} = 5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_6$	When used as CLK input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, CNTR, $\overline{INT_1}$, $\overline{INT_2}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis, X_{IN}			0.1		0.5	V
I_{IL}	"L" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$	V_I = 0V without pull-up transistor				−5	μA
I_{IL}	"L" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$	V_I = 0V with pull-up transistor		−40	−70	−125	μA
I_{IL}	"L" input current, $P4_0$~$P4_7$	V_I = 0V				−5	μA
I_{IL}	"L" input current, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	V_I = 0V				−5	μA
I_{IH}	"H" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$	V_I = 12V without pull-up transistor				12	μA
I_{IH}	"H" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$	V_I = 5V with pull-up transistor				5	μA
I_{IH}	"H" input current, $P4_0$~$P4_7$	V_I = 5V without pull-down transistor				5	μA
I_{IH}	"H" input current, $P4_0$~$P4_7$	V_I = 5V with pull-down transistor		40	70	125	μA
I_{IH}	"H" input current, CNTR, $\overline{INT}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	V_I = 5V				5	μA
V_{RAM}	RAM retention voltage	at clock stop		2			V
I_{CC}	Supply current	P-channel open-drain output pins are to V_{CC}, output pins are open, other I/O pins are connected to V_{SS}.	$f_{(X_{IN})}$ = 4MHz square wave		3	6	mA
			T_a = 25℃ at clock stop			1	μA
			T_a = 70℃ at clock stop			10	μA

TIMING REQUIREMENTS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	270			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time	20			ns
t_C	External clock input cycle time	250			ns
t_W	External clock input pulse width	75			ns
t_r	External clock rising edge			25	ns
t_f	External clock falling edge			25	ns

Memory expanding mode and eva-chip mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(\overline{RDY}-\phi)}$	$\overline{RDY}$ input setup time	150			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-\overline{RDY})}$	$\overline{RDY}$ input hold time	500			ns

Microprocessor mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(\overline{RDY}-\phi)}$	$\overline{RDY}$ input setup time	150			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-\overline{RDY})}$	$\overline{RDY}$ input hold time	500			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.18			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time	Fig.19			230	ns

Memory expanding mode and eva-chip mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.18			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns

Microprocessor mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.18			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P0QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

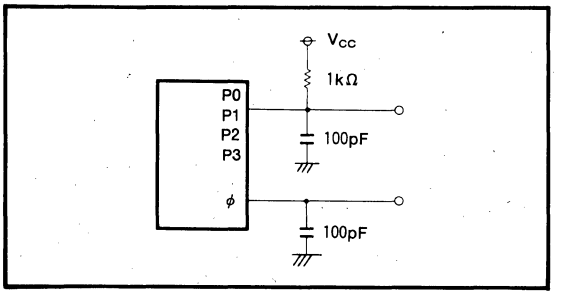


Fig.18 Ports P0~P3 test circuit

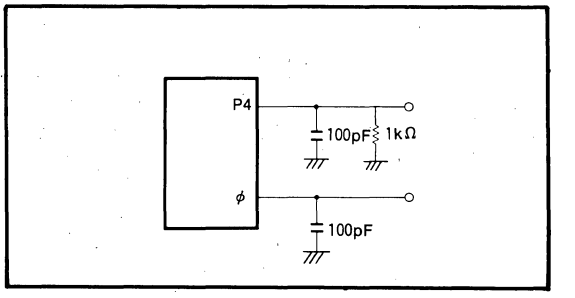
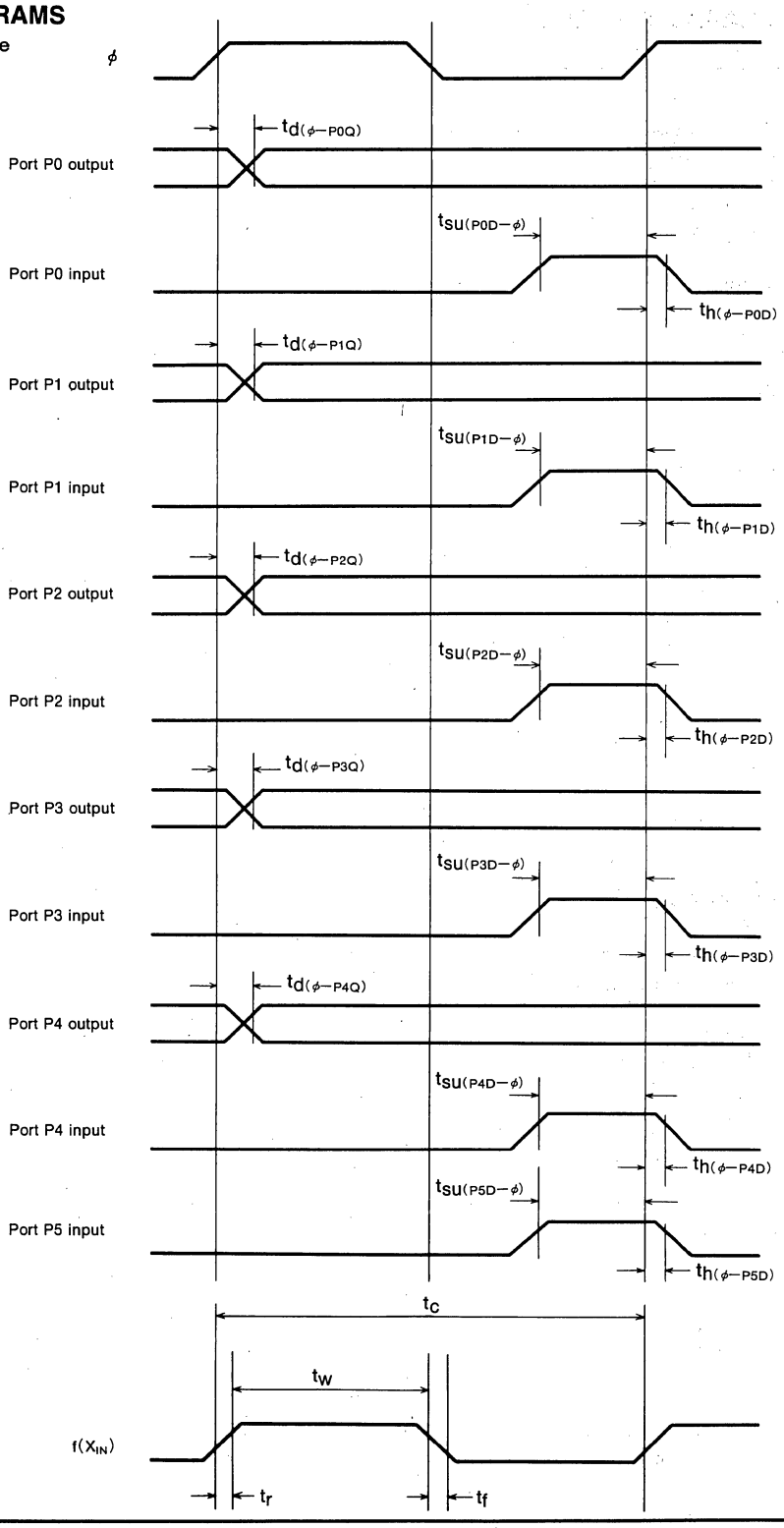


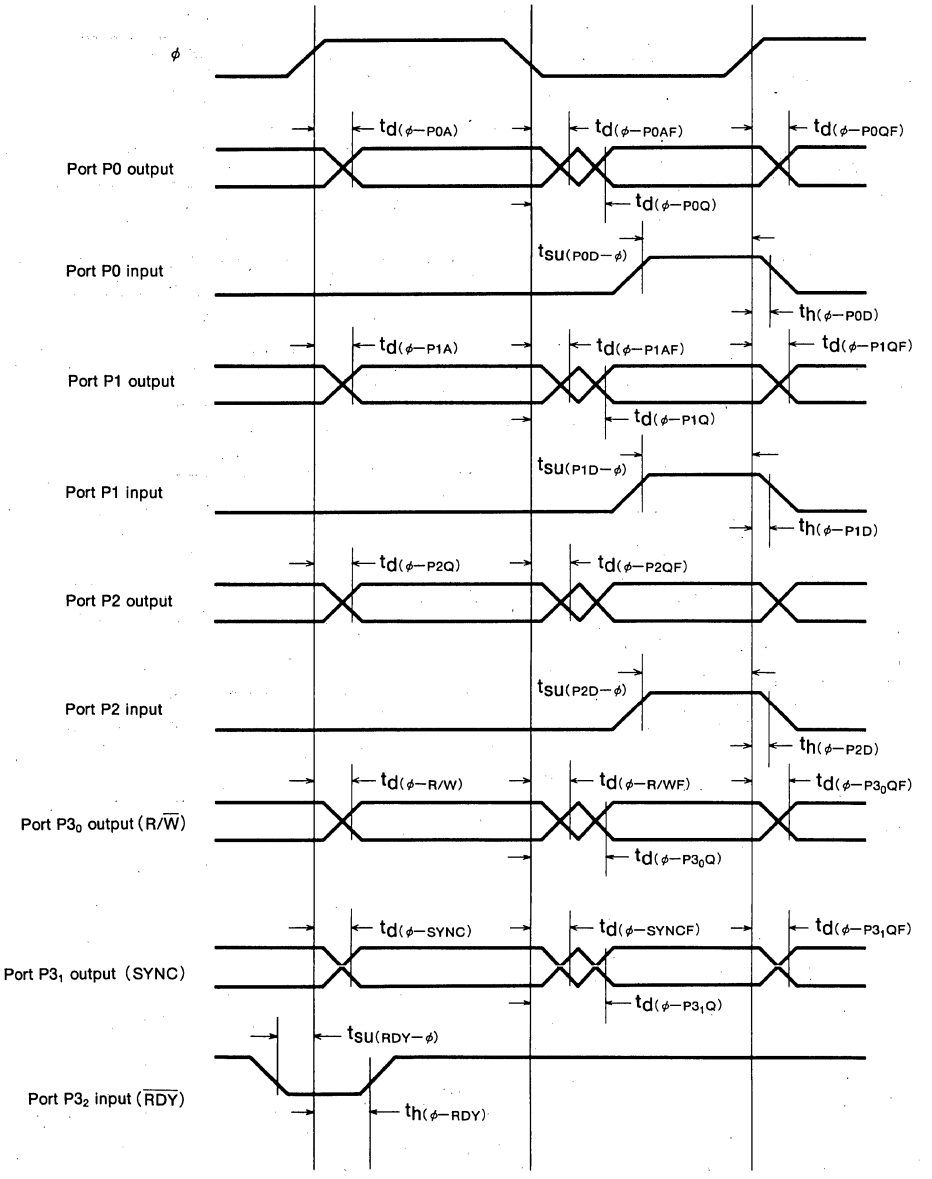
Fig.19 Port P4 test circuit

TIMING DIAGRAMS

In single-chip mode

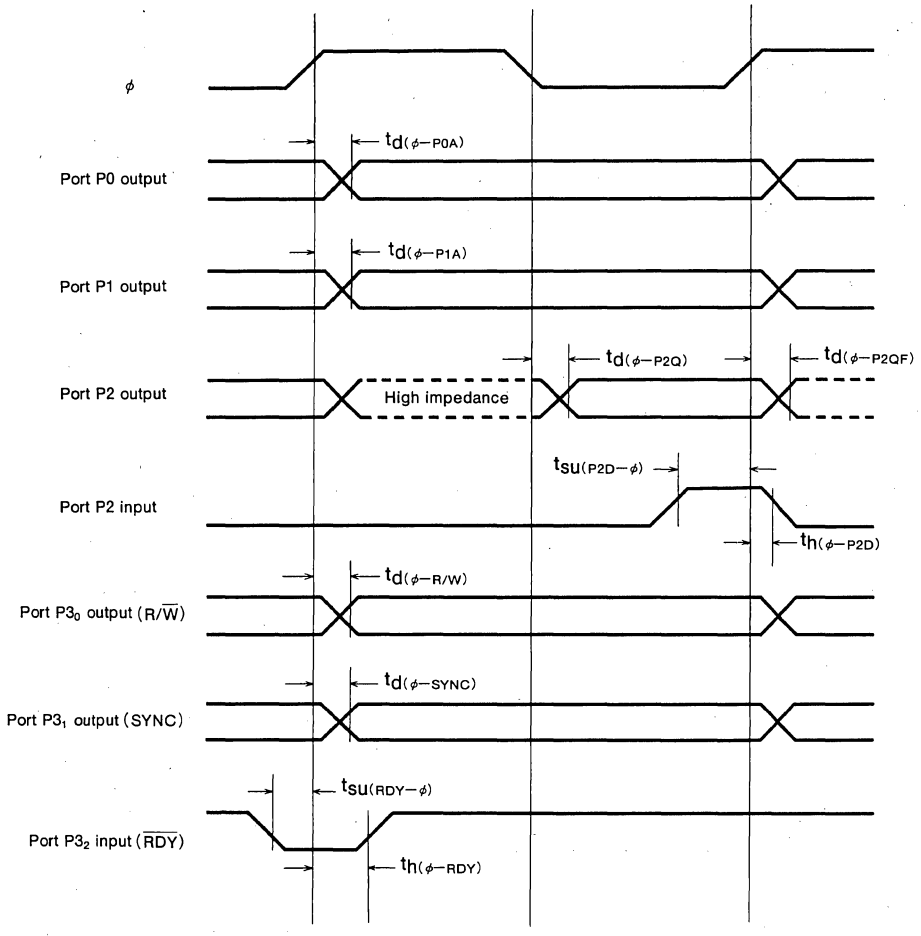


In memory expanding mode and eva-chip mode



MITSUBISHI ELECTRIC

In microprocessor mode



M50747-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50747-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP (flat package type also available). This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50747-XXXSP and the M50747-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

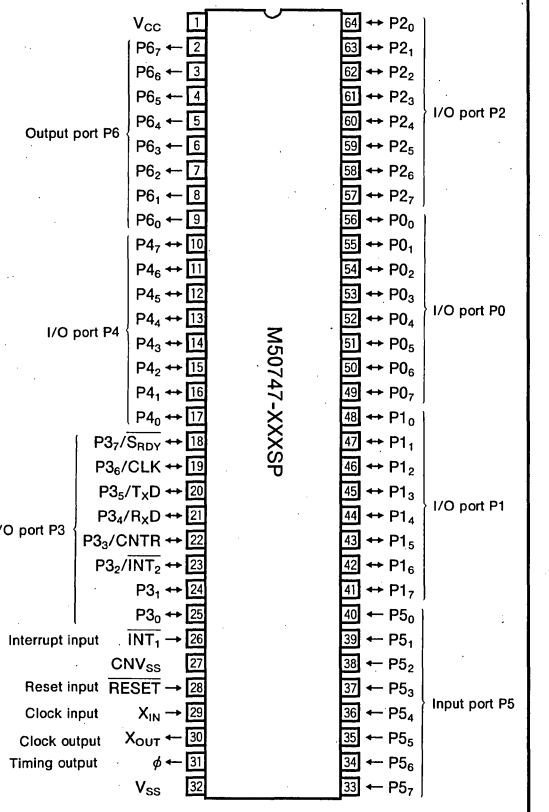
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 8192 bytes
  RAM ..... 256 bytes
- Instruction execution time
  ..... 1 μs (minimum instructions at 8MHz frequency)
- Single power supply f(X_{IN})=8MHz ..... 5V$\pm$10%
- Power dissipation
  normal operation mode (at 8MHz frequency) 30mW
- Subroutine nesting ..... 128 levels (max.)
- Interrupt ..... 7 types, 5 vecters
- 8-bit timer ..... 3 (2 when used as serial I/O)
- Programmable I/O (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Output ports (Port P6) 8
- Serial I/O (Clock synchronized or UART) 1

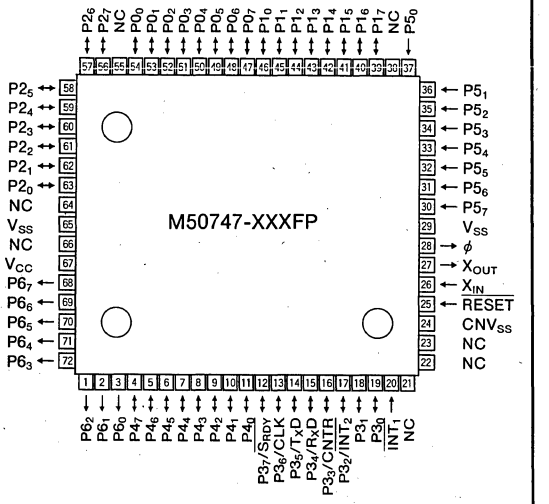
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

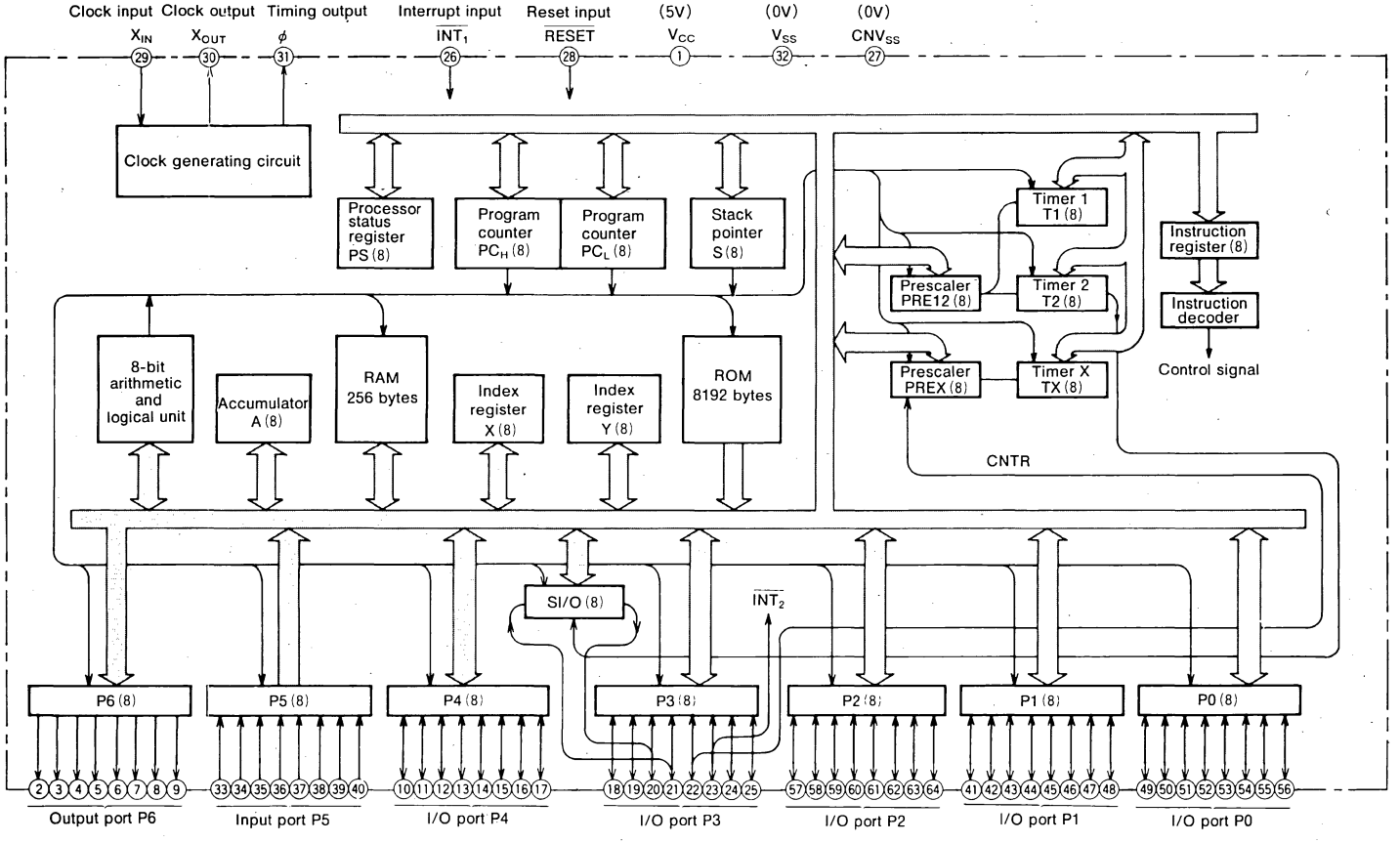


Outline 72P6

NC : No connection

MITSUBISHI ELECTRIC

M50747-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M50747-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 8MHz of frequency)
Clock frequency			8MHz
Memory size	ROM		8192bytes
	RAM		256bytes
Input/Output port	$\overline{INT_1}$	Input	1-bit×1
	P0, P1, P2, P3, P4	I/O	8-bit×5 (Part of P3 are in common with Input/output of serial I/O, timer I/O and $\overline{INT_2}$ interrupt input)
	P5	Input	8-bit×1
	P6	Output	8-bit×1
Serial I/O			8-bit or 9-bit×1
Timers			8-bit prescaler×2+8-bit timer×3 (8-bit timer×2 when serial I/O is used)
Subroutine nesting			128 levels (max.)
Interrupts			Two external interrupts (1 of external interrupt is in common with port $P3_2$) Three timer interrupts (or timer×2, serial I/O×1)
Clock generating circuit			Built-in (Ceramic or Quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	at high-speed operation		30mW (at 8MHz frenquency)
Input/Output characteristics	Input/output voltage		5V
	Output current		5mA (Ports P3, P4, P6)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package	M50747-XXXSP		64-pin shrink plastic molded DIP
	M50747-XXXFP		72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an I/O pin for the timer X.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_6$, $P3_5$, and $P3_4$ work as CLK, T_XD pins, respectively. When clock synchronous serial I/O is used, $P3_7$ works as $\overline{S_{RDY}}$. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest order interrupt input pin ($\overline{INT_2}$), respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
$P6_0$~$P6_7$	Output port P6	Output	Port P6 is an 8-bit output port. The output structure is CMOS output.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50747-XXXSP is shown in Figure 1. Addresses $E000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 8192 bytes.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $013F_{16}$ are assigned to the built-in RAM and respectively consist of 192 bytes and 64 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

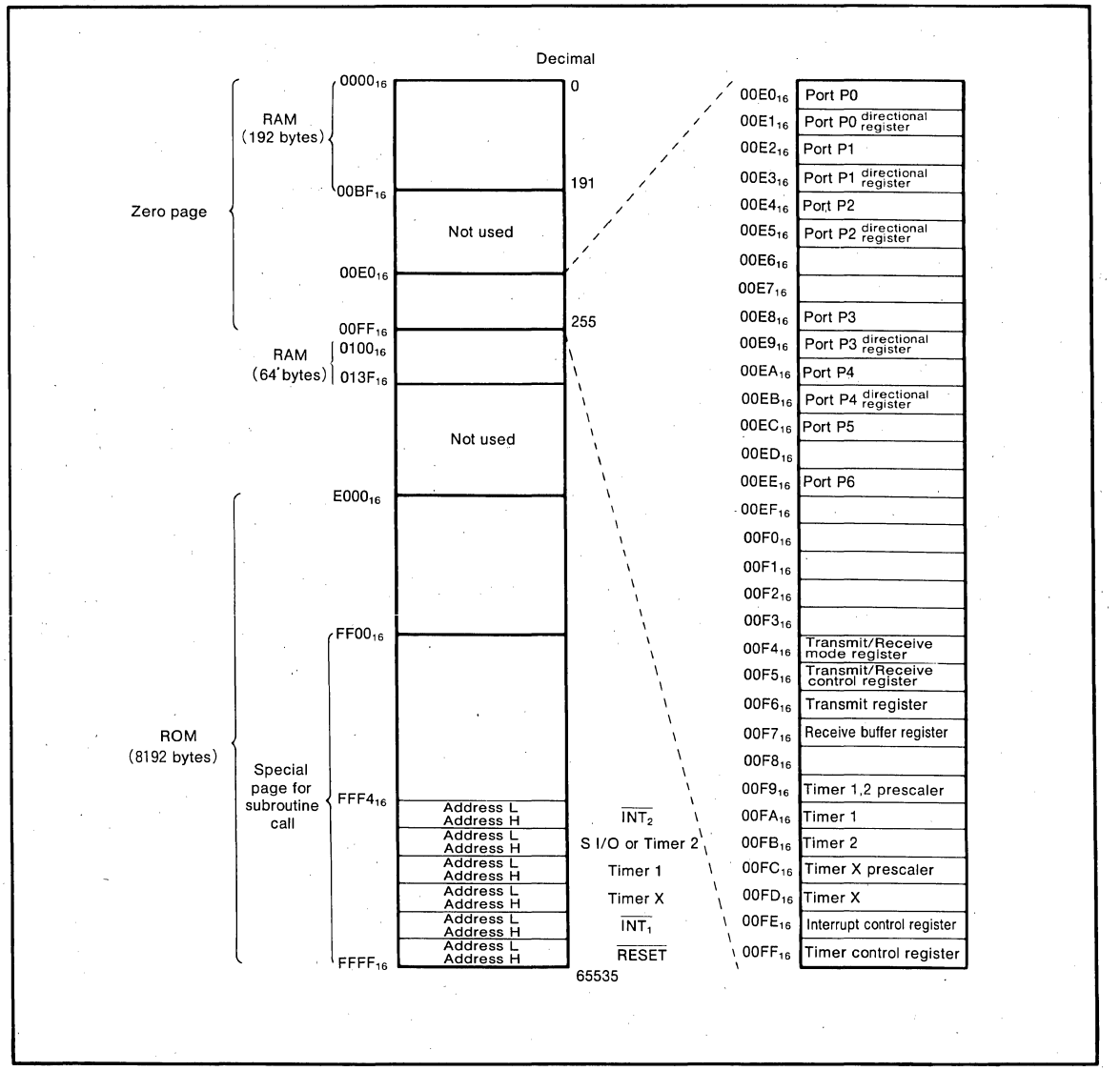


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

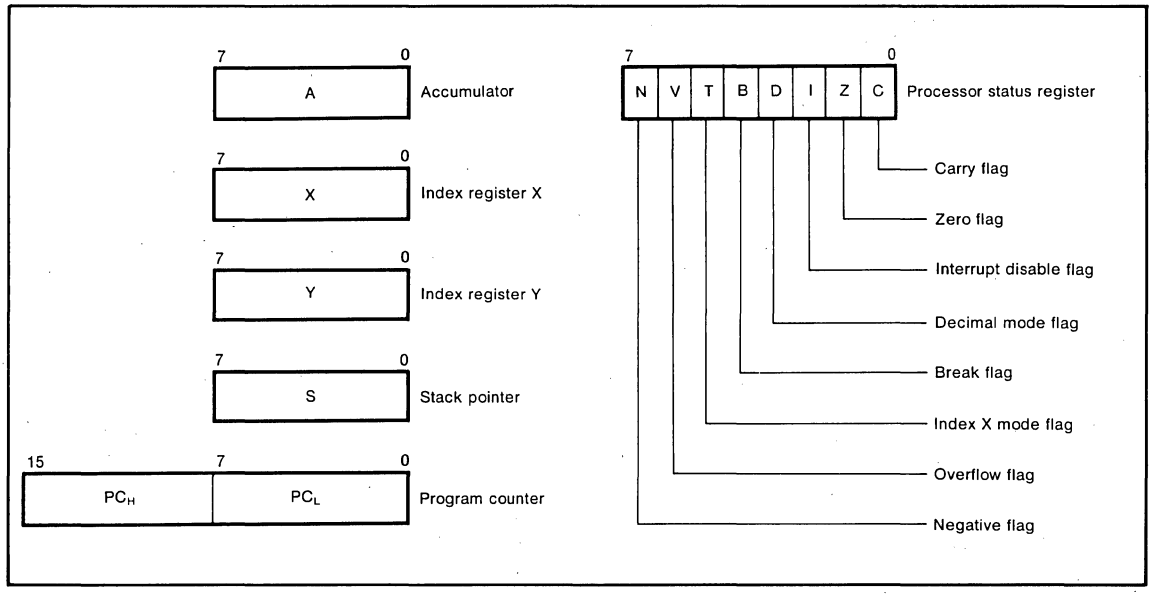


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The location of the stack can be determined by the stack page bit (bit 4 at address $00FF_{16}$). When bit 4 is "0" and the contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When bit 4 is "1", the stack address is set to $01XX_{16}$. When using this microcomputer in the single-chip mode, the stack page bit must be "0" and the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{\text{INT}_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1	4	$FFF9_{16}$, $FFF8_{16}$
Timer 2 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{\text{INT}_2}$ (BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50747-XXXSP can be interrupted from seven souces; $\overline{\text{INT}_1}$, timer X, timer 1, timer 2/serial I/O, or $\overline{\text{INT}_2}$/BRK instruction.

However, the $\overline{\text{INT}_2}$ pin is used with port $P3_2$ and the corresponding directional register bit should be set to "0" when $P3_2$ is used as an interrupt input pin.

The value of bit 2 and bit 3 of the transmit/receive mode register (address $00F4_{16}$) determine whether the interrupt is from timer 2 or from serial I/O. When these bits are "00" the interrupt is from timer 2, otherwise the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure

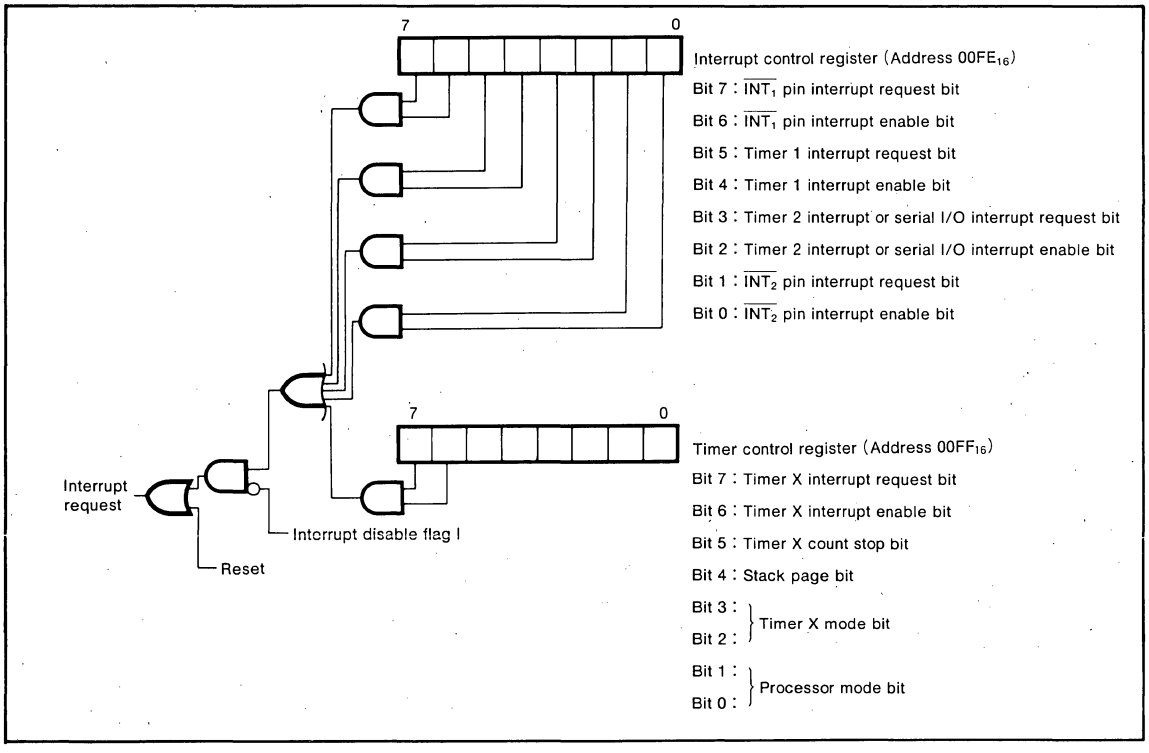


Fig.3 Interrupt control

3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"

(2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

The interrupt from serial I/O is used switching with that from timer 2. This interrupt is slightly different from the others. When serial I/O is selected, the interrupt becomes automatically the interrupt from serial I/O. Because the interrupt request bit of timer 2 is edge-senced and not level-senced, when interrupts are generated from both transmit and receive sides as illustrated in Figure 5, transmit interrupts will not be accepted by only taking OR of receive interrupt flag RI and transmit flag TI. Even if RI is cleared to "0" by executing receive interrupt processing and is returned to the main routine, TI is "1" and its level will not be changed. In order to accept interrupts in the above state, when RI or TI is cleared from "1" to "0" the pulse is generated automatically and lets the request bit go from "H" to "L". By doing so, the level will be changed. The interrupt processing routine of serial I/O is shown in Figure 4.

Since the BRK instruction and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

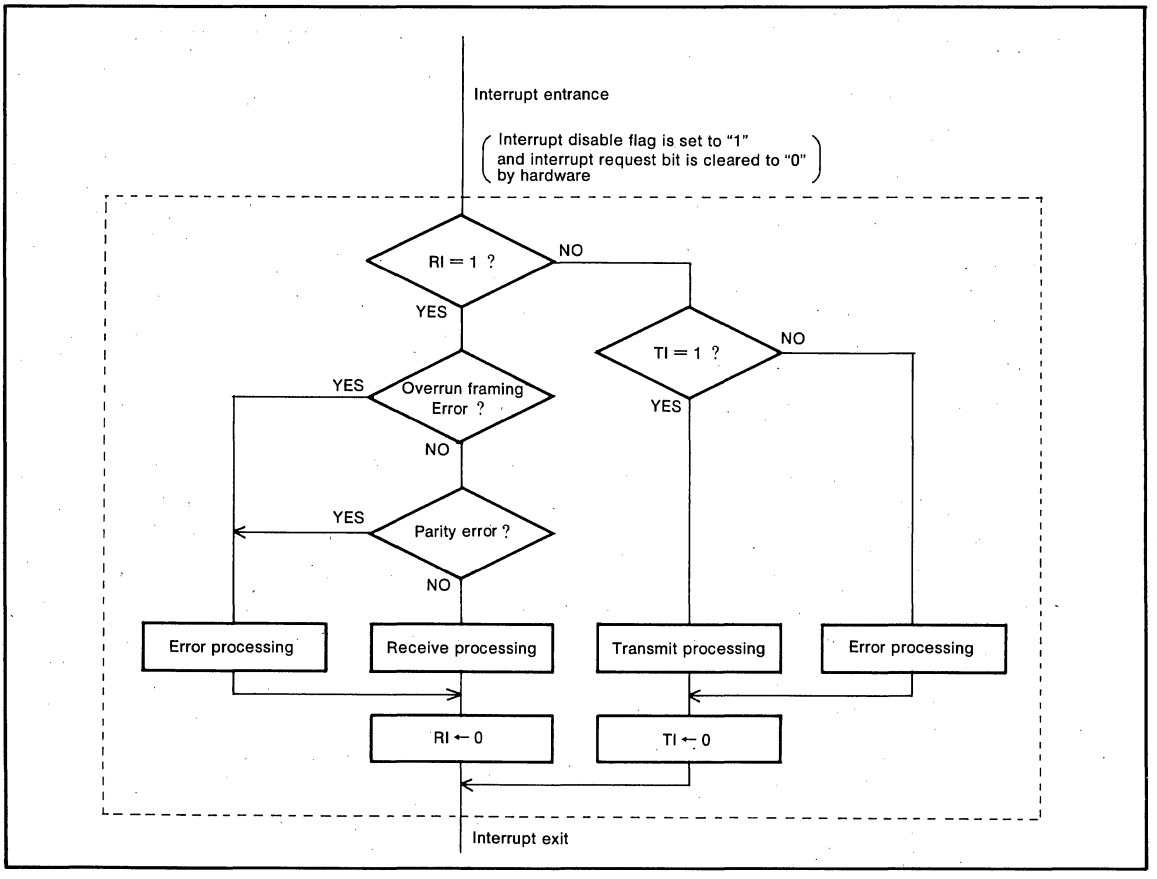


Fig.4 Interrupt processing routine

TIMER

The M50747-XXXSP has three timers; timer X, timer 1, and timer 2. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section). Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in.

A block diagram of timer X, timer 1, timer 2 and serial I/O is shown in Figure 5.

The $P3_3$/CNTR pin cannot be used as CNTR when $P3_3$ is being used in the normal I/O mode.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section).

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

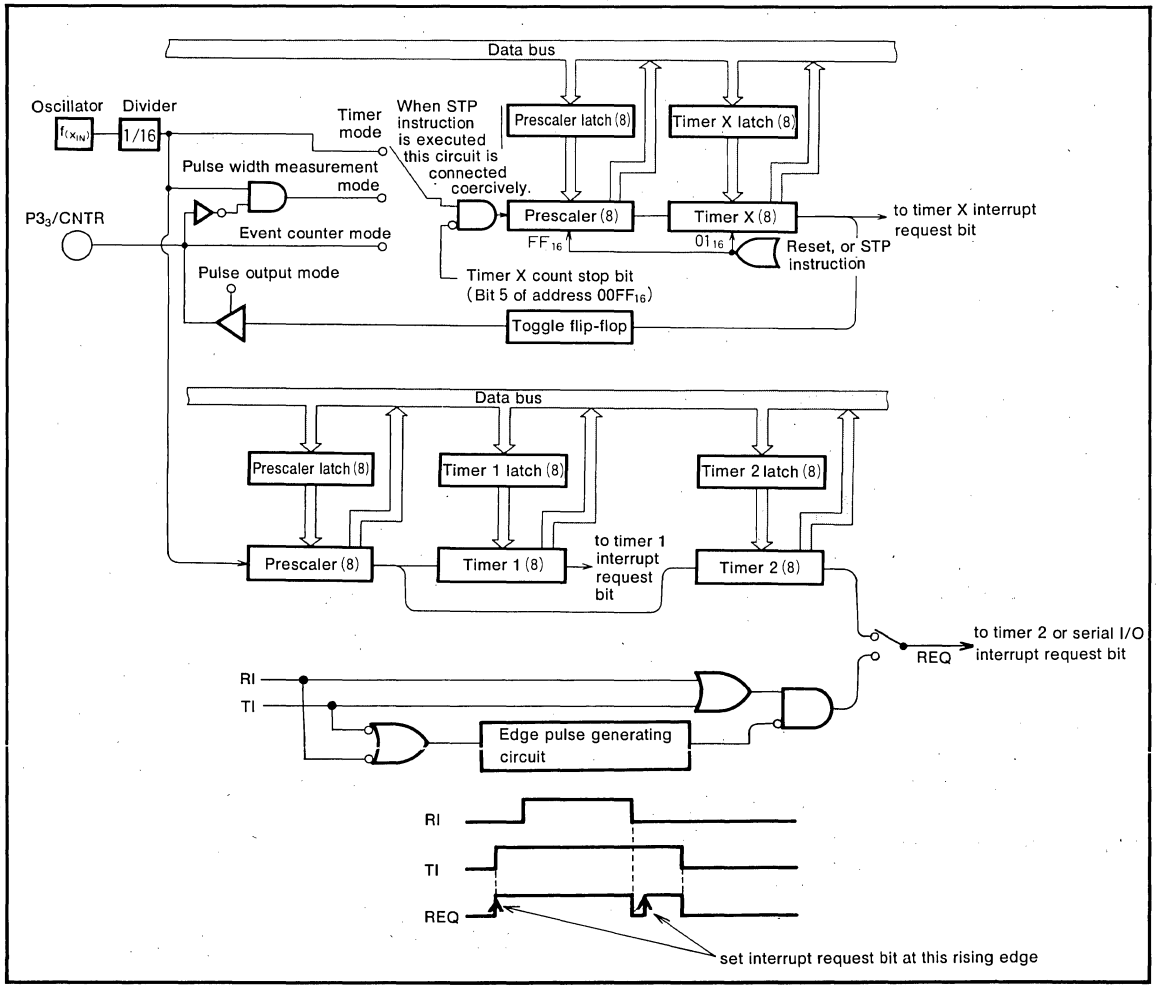


Fig.5 Interrupt block diagram of timer X, timer 1, timer 2 and serial I/O

(3) Event counter mode [10]

This mode operates in the same manner as the timer mode except the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock source.

(4) Pulse width measurement mode [11]

This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 6.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

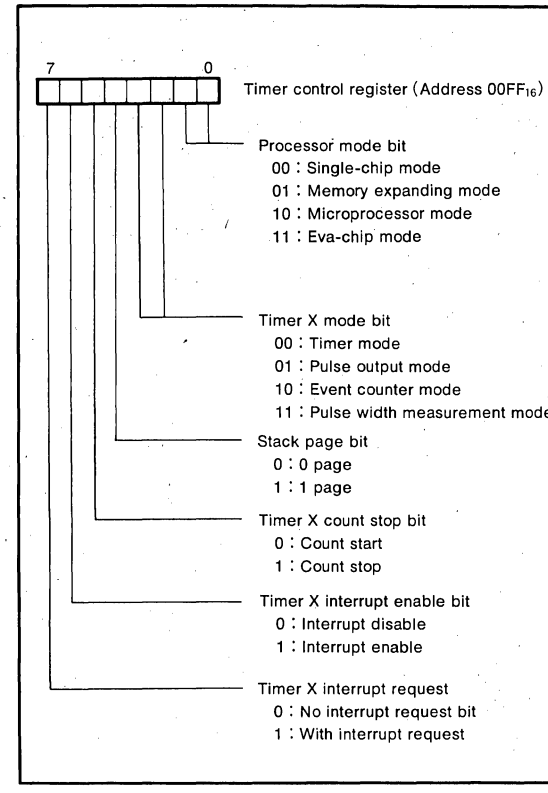


Fig.6 Structure of timer control register

SERIAL I/O

Figure 7 is a block diagram of the serial I/O. Two types exist in serial data transfer: the clock synchronous type in which data is transferred, synchronized with the clock, and the asynchronous type (UART) in which data is transferred using the start and stop bits. The user can choose either type. There are two asynchronous type modes: 8-bit data transfer and 9-bit data transfer. The receive ready signal ($\overline{S_{RDY}}$), clock I/O (CLK), data I/O (T_XD and R_XD) pins share the same pins as $P3_7$, $P3_6$, $P3_5$, $P3_4$.

Figure 8 gives the bit configuration for the transmisson/receive mode register and transmisson/receive control register. The transmit/receive mode register ($00F4_{16}$) is a 5-bit register. Bits 1 and 0 are used to define the clock source for synchronization. When the contents of bits 1 and 0 are [00] or [01], respectively, the external clock is used. The external clock is input to pin $P3_6$. Use an external clock with a 50% duty cycle and a frequency lower than 500kHz.

When the contents of bits 1 and 0 are [10] or [11], respectively, the built-in clock is used.

When the contents are [10], the overflow signal from timer 2 is used for the clock source. Therefore, by changing the division rate, the data transfer speed can be controlled.

When the contents are [11], the frequency obtained by dividing the oscillation frequency by 16 is used as the clock source.

Bits 2 and 3 are used to define which pins on port P3 are to be used as serial I/O, and which type of serial I/O to used.

When the contents are [00], respectively, port P3 is used as a normal parallel port.

When the contents are [01], respectively, the clock synchronous type serial I/O is used.

$P3_7/\overline{S_{RDY}}$ on port P3 is used as the receive ready signal pin. $P3_6$/CLK is used as the input or output pin. When an external clock is to be used, the signal from the clock is connected to this pin. When the built-in clock is to be used, the signal from the clock is output to this pin. $P3_5/T_XD$ is used as the serial data output pin. $P3_4/R_XD$ is used as the serial data input pin. When this pin is not used as the serial data input pin, it can be used as the normal input/output pin. When this pin is used as the serial data input pin, set the directional register to the input mode.

When the contents are [10], this serial I/O is used as an 8-bit asynchronous serial I/O. If the external clock source is selected together with the bit contents [10], the clock signal is input to $P3_6$/CLK on port P3. The data transfer speed is 1/16 of the clock frequency. When the built-in clock is used, this can be used as the normal input/output pin. $P3_5/T_XD$ is used as the serial data output pin. $P3_4/R_XD$ is used as the serial data input pin. When this is not used as the serial data input pin, it can be used as a normal input/output pin. When this pin is used as a serial data input pin, set the directional register to the input mode. When the contents are [11], a 9-bit asynchronous serial I/O is selected. The functions on port P3 are the same as in the 8-bit case.

Bit 4 is used to select the sleep mode. The sleep mode is valid only for asynchronous transmission. See the section on the sleep mode for further explanation. When the contents are "0", the sleep mode is disabled. When the contents are "1", the sleep mode is enabled.

The transmission/receive control register is an 8-bit register. Bits 1, 3, 4, 5 and 7 are for read only. Each bit is explained as follows.

Transmit enable bit (TE)

When this bit is set to "0", the send clock is pulled up to "H", the transmit completion bit (TI) is cleared to "0", transmission is terminated, and the serial I/O is initialized. When this bit is set to "1", transmission starts. Therefore, send data must be written into the transmission register prior to setting it to "1". When the transmission is completed, the serial I/O stops and the transmission clock is pulled up to "H" automatically.

Once the above operation has been peformed, transmission starts by writing data into the transmission register.

Transmit completion bit (TI)

This bit is cleared to "0" when the transmit enable bit (TE) is set to "0", or when data is written into the transmission register. When transmission is completed, this bit is set to "1". An OR operation is performed between the transmit completion bit (TI) and the receive completion bit (RI), and the result is input into the interrupt request bit (bit 3 of address $00FE_{16}$). See the section on interrupts for more information.

Receive enable bit (RE)

When this bit is cleared to "0", the receive completion bit (RI), the overrun framing error (OFR), and the receive parity error bit (PER) are cleared and initialized. When this bit is set to "1", the I/O enters the receive enable status. For the clock synchronous type serial I/O, data is fetched from the $P3_4/R_XD$ pin and the contents of the receive register are shifted by 1 bit every time the receive clock changes from "L" to "H". For the asynchronous type I/O, receiving starts when a start bit is forwarded to $P3_4/R_XD$.

Receive completion bit (RI)

This bit is cleared to "0" when the receive enable bit is set to "0", or when writing is performed to the receive buffer register. If the receive buffer is written to, no data is written in the register and the previous data is preserved. When a set of data arrives in the receive buffer, and the receive completion bit (RI) is "0", data is transferred to the receive buffer register. With this operation, receiving terminates and the receive completion bit (RI) is set to "1". An OR operation is performed between the receive completion bit (RI), the transmit completion bit (TI), and the result is input to the interrupt request bit (bit 3 at address $00FE_{16}$). For more information on the interrupts, see the corresponding section.

Overrun framing error bit (OFR)

When the receive enable bit (RE) is set to "0" or when writing is performed to the receive buffer register, this bit is cleared to "0". If an overrun or framing error occurs, this bit is set to "1". An overrun error occurs when the receive completion bit (RI) remains set to "1" and the next data is transferred from the receive register to the receive buffer register. A framing error occurs when data arrives in the receive register, (which should be transferred to the receive buffer register), and no stop bit exists. This bit is valid only for asynchronous transmission.

Receive parity error bit (PER)

When the number of "1"s is in the received data register is odd, this bit is set to "1". This bit is cleared to "0" when the receive enable bit (RE) is set to "0" or when writing is performed to the receive buffer register.

Receive data bit (T8)

For 9-bit asynchronous transmission, this bit is transmitted as bit 8 data.

Receive data bit 8 (R8)

For 9-bit asynchronous transmission, this bit is used to receive the bit 8 data.

The operation of each transmission method is described below.

CLOCK SYNCHRONOUS TYPE SERIAL TRANSMISSION

Receiving starts when the receive enable bit (RE) is set to "1". Every time the receive clock changes from "L" to "H", data is fetched from $P3_4/R_XD$ pin and, simultaneously, the contents of the receive register are shifted by 1 bit. Data transmission starts from the least significant bit. When 8 bits of data are received, the receive completion bit (RI) is set to "1". When RI changes from "0" to "1", the interrupt request bit is set to "1". When the internal clock is used, the receive clock stops in the "H" condition. When the external clock is used, the clock does not stop. In this case, control this clock using external devices. Once the receive enable bit (RE) is set to "1", writing to the receive buffer register clears the receive completion bit (RI) and receiving restarts. Set a "0" in the transmission enable bit during receiving.

Setting "1" in the transmission enable bit (TE) starts the transmission. Accordingly, write data in the transmission register before setting TE to "1". Every time the transmission clock changes from "H" to "L", data is output from the $P3_5/T_XD$ pin. Data transmission starts from the least significant bit. The transmission completion bit (TI) is set to "1" for each 8 bits of data transmitted. When TI changes from "0" to "1", the interrupt request bit is set to "1". When the internal clock is used, the clock stops in the "H" position after transmitting 8 bits of data. When an external clock is used, the clock does not stop. In this case, control this clock using external devices. Once the transmission enable bit is set to "1", writing data to the transmission register clears the transmission completion bit to "0" and starts the transmission. Set a "0" in the receive enable bit during transmission. When the external clock is used, the transmission speed is the same as that of the clock. When the internal clock is used, the clock frequency obtained by dividing the clock source by 16 is used for the transmission speed. Figure 9 gives the transmission timing. This figure also gives the timings for 8-bit and 9-bit asynchronous transmission, which is explained below.

8-BIT ASYNCHRONOUS TRANSMISSION

Setting the receive enable bit (RE) to "1" brings the I/O into the receiving ready status. Transmission starts when the first data that changes the level from "H" to "L" is received, and data is forwarded to the receive register. When 8 bits of data are received and the receive completion bit (RI) is set to "1", the 8-bits of data are transferred to the receive buffer register, and RI is set to "1". See the section on the interrupts for more information. If RI is set to "1", no transfer is performed. The overrun framing error bit (OFR) is set to "1" when RI is set to "1" and the next data is received. When the stop bit is set to "0", the OFR bit is set to "1" regardless of the RI bit status. No other condition will change the contents of this bit. When the number of "1"s in the received data register is odd, the receive error bit (PER) is set to "1". No other condition will change the contents of this bit. Bits RI, OFR, and PER are cleared to "0" when writing is performed to the receive buffer register. When 8-bits of data are received, receiving automatically halts and the start bit of the next data is ready.

When the transmission enable bit (TE) is set to "1" (after writing data to the transmit register), transmission starts. First, the start bit "0" is sent, and data is transferred starting from the least significant bit. When the stop bit "1" is sent, the transmission completion bit (TI) is set to "1" and the transmission terminates. For more information on the interrupt, see the corresponding section. After the above operation has been performed, the transmission completion bit (TI) is cleared to "0" and transmission restarts after writing to the transmit register is performed.

9-BIT ASYNCHRONOUS TRANSMISSION

Operation for 9-bit asynchronous transmission is same as 8-bit asynchronous transmission except that the transmission data consists of 9 bits. When receiving data, bit 8 of the received data is input to bit 7 on address $00F5_{16}$ (transmit/receive control register). When transmitting data, the contents of bit 6 in the transmit/receive control register is output as bit 8 of the send data.

SLEEP MODE

For 9-bit asynchronous transmission, when bit 4 (SM_4) of the transmit/receive mode register ($00F4_{16}$) is set to "1" and bit 8 of the receive data is "0", the received data is ignored. When bit 8 of the receive data is set to "1", data is received. When the contents of SM_4 is "0", data is received, regardless of the contents of bit 8 of the received data. For 8-bit asynchronous transmission, the stop bit works as bit 8 of the received data. The sleep mode is used when several local microcomputers are to be connected to a single host computer through the serial I/O.

First, the host computer sets T8 to "1" and sends data. The data contains the address of the local microcomputer to be accessed. All the local microcomputers receive the same data. Each local microcomputer checks the data (address), and if the address is that assigned to the local microcomputer, bit 4 of the transmit/receive mode register is set to "0". Bit 4 of the registers of all the other local microcomputers is set to "1". Then, the host computer starts transmission by setting T8 to "0". The local microcomputer whose SM_4 is "0" receives the transmitted data, while the other local microcomputers continue program execution without being interrupted by serial I/O. This is because SM_4 on these computers set to "1". Thus, the host computer can communicate with a specific microcomputer.

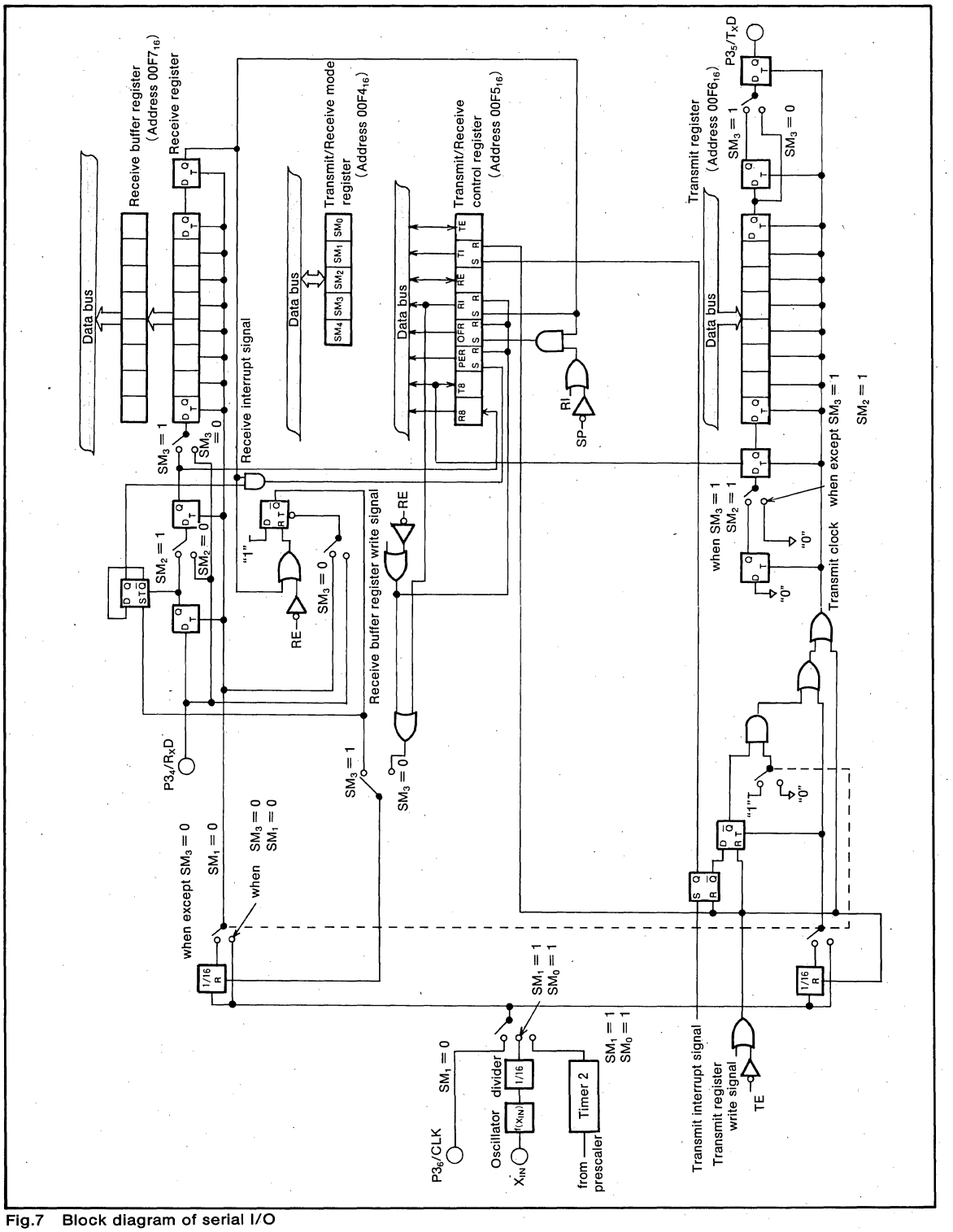


Fig.7 Block diagram of serial I/O

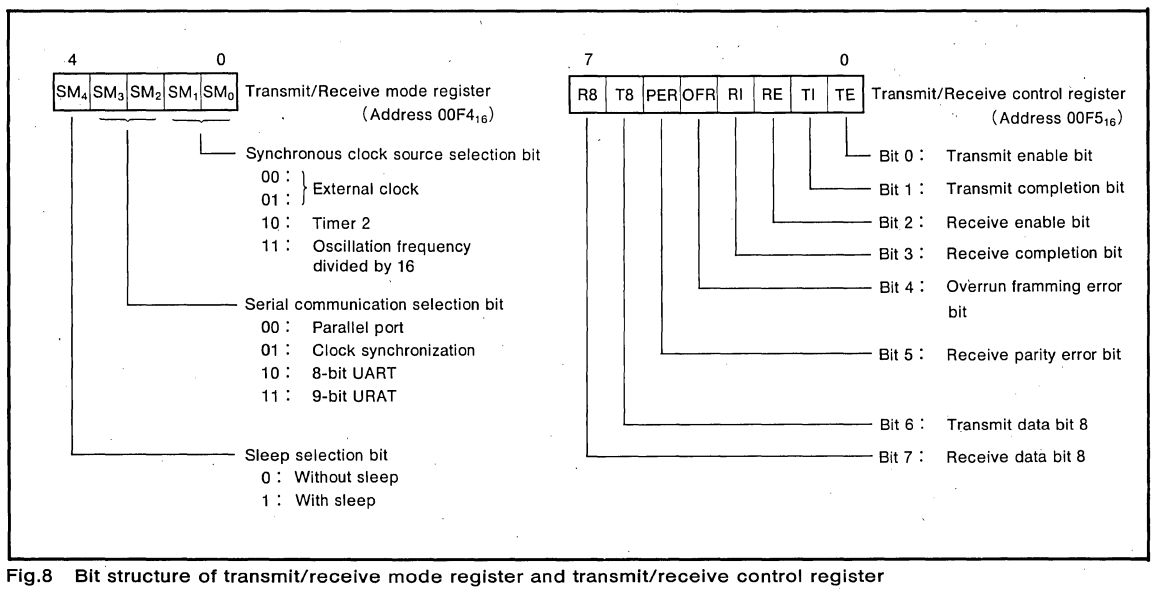


Fig.8 Bit structure of transmit/receive mode register and transmit/receive control register

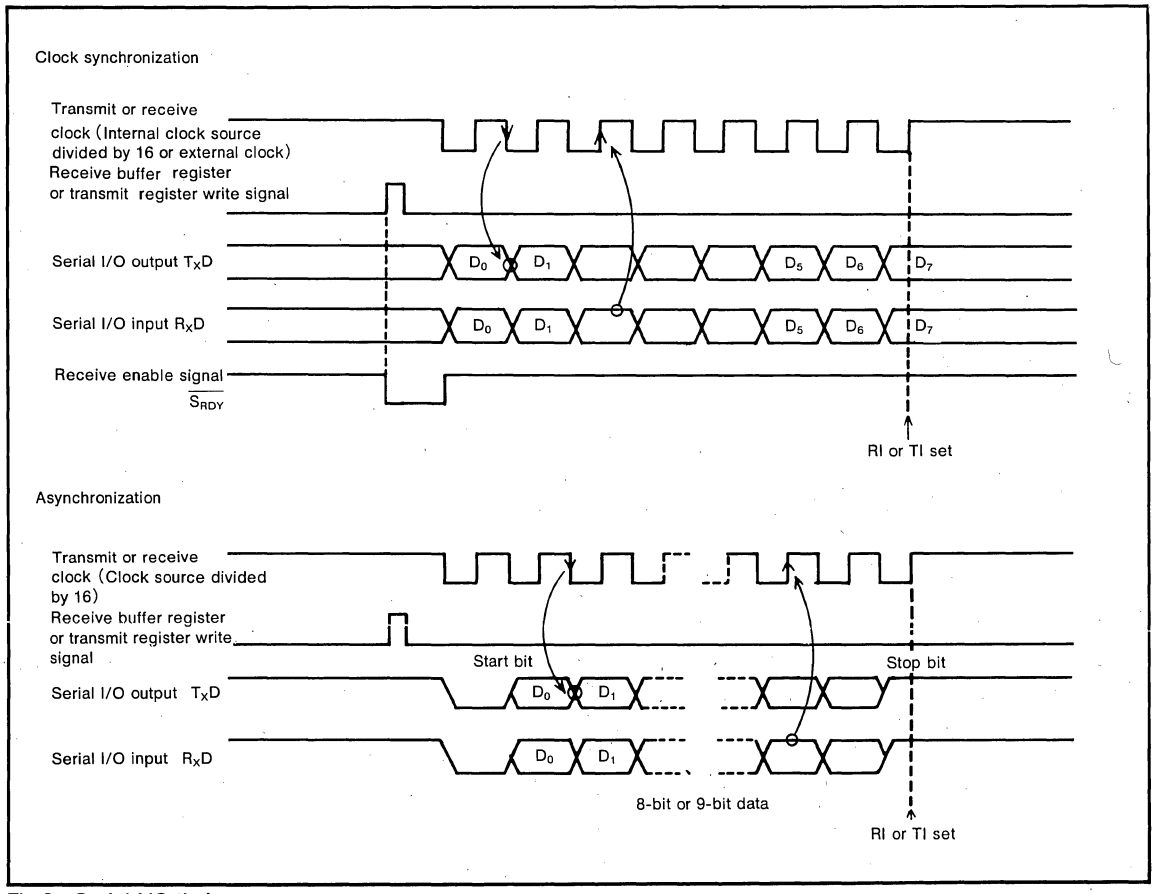


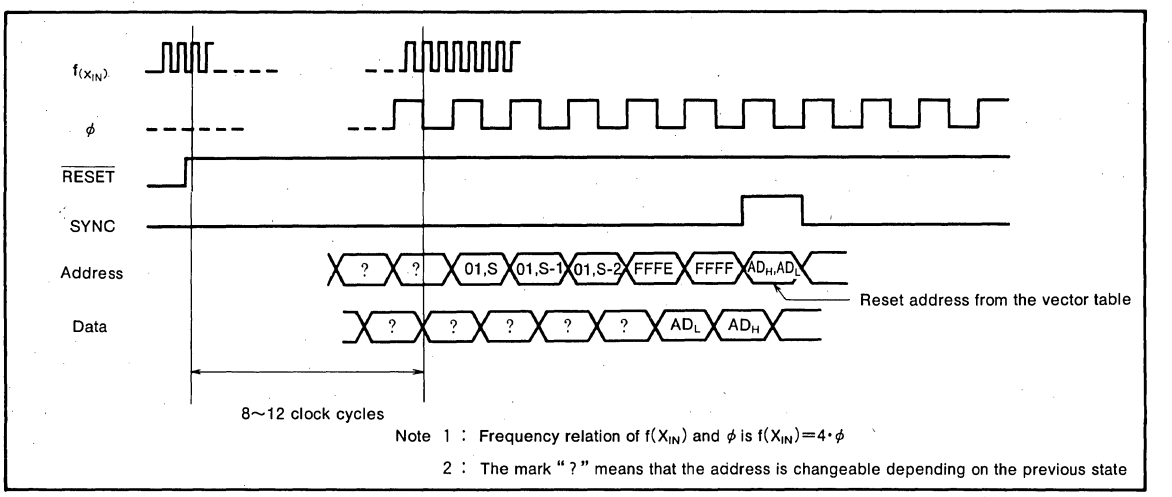
Fig.9 Serial I/O timing

RESET CIRCUIT

The M50747-XXXSP is reset according to the sequence shown in Figure 10. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 11.

An example of the reset circuit is shown in Figure 12.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.



Note 1 : Frequency relation of $f(X_{IN})$ and ϕ is $f(X_{IN})=4\cdot\phi$

2 : The mark "?" means that the address is changeable depending on the previous state

Fig.10 Timing diagram at reset

Address		
(1) Port P0 directional register	(E 1 16) ···	0 0 16
(2) Port P1 directional register	(E 3 16) ···	0 0 16
(3) Port P2 directional register	(E 5 16) ···	0 0 16
(4) Port P3 directional register	(E 9 16) ···	0 0 16
(5) Port P4 directional register	(E B 16) ···	0 0 16
(6) Port 6 (Note 1)	(E E 16) ···	F F 16
(7) Transmit/Receive mode register	(F 4 16) ···	X X X 0 0 0 0 0
(8) Transmit/Receive control register	(F 5 16) ···	0 0 0 0 0 0 0 0
(9) Prescaler X	(F C 16) ···	F F 16
(10) Timer X	(F D 16) ···	0 1 16
(11) Interrupt control register	(F E 16) ···	0 0 16
(12) Timer control register	(F F 16) ···	1 0 16
(13) Interrupt disable flag for processor status register	(P S) ···	1
(14) Program counter	(P C H) ···	Contents of address FFFF16
	(P C L) ···	Contents of address FFFE16

Note 1 : Port P6 is the high-impedance state during reset. After return from reset, it is "FF_{16}".

Fig.11 Internal state of microcomputer at reset

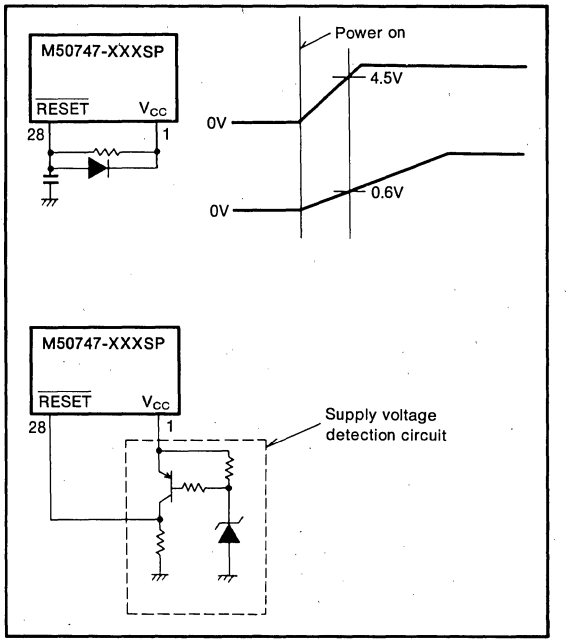


Fig.12 Example of reset circuit

MITSUBISHI ELECTRIC

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as serial I/O, $\overline{INT_2}$ and I/O pins for timer X. For more details, see the processor mode information.

(5) Port P4

Port P4 has the same function as port P0 in the single-chip mode. This function does not change even though the processor mode changes.

(6) Port P5

Port P5 is an input.

(7) Port P6

Port P6 is a CMOS output port. See Figure 13 for more details.

(8) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ.

(9) $\overline{INT_1}$ pin

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

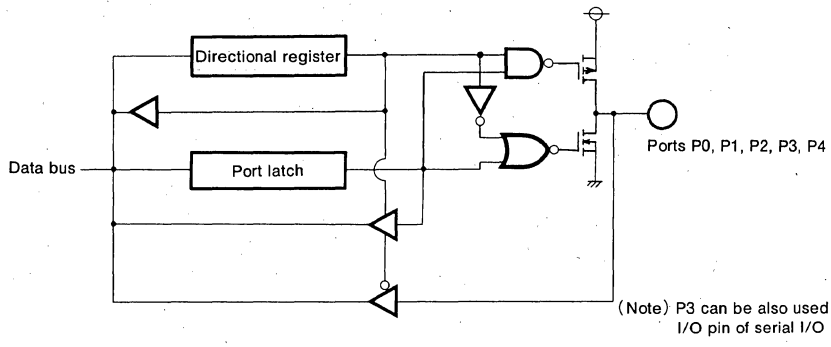
(10) $\overline{INT_2}$ pin ($P3_2/\overline{INT_2}$ pin)

The $\overline{INT_2}$ pin is an interrupt input pin used with $P3_2$. To use this pin as an interrupt pin, set the corresponding bit in the directional register to input ("0"). When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1".

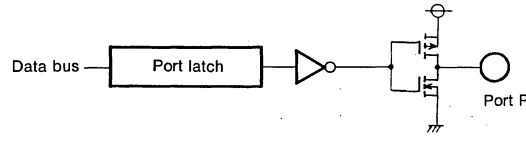
(11) CNTR pin ($P3_3$/CNTR pin)

The $P3_3$/CNTR pin is an I/O pin of timer X. To use this pin as the timer X input pin, set the corresponding directional register bit to input ("0"). In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

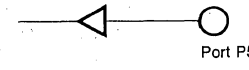
Ports P0, P1, P2, P3, P4



Port P6



Port P5



ϕ

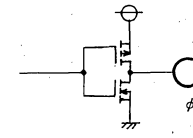


Fig.13 Block diagram of ports P0~P6 (single-chip mode), and ϕ output format

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 15 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 14.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

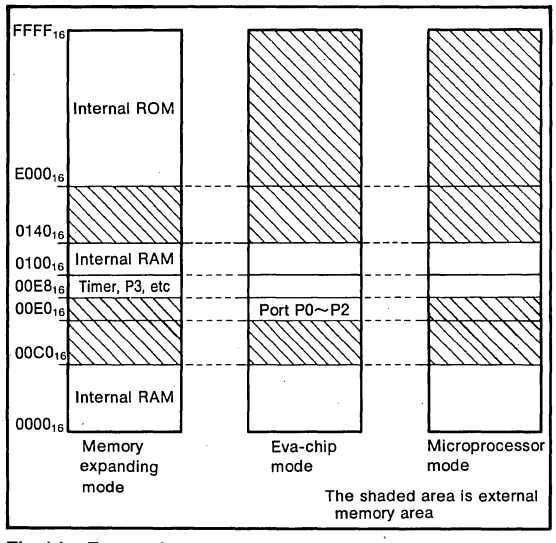


Fig.14 External memory area in processor mode

(1) Single-chip mode [00]
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Memory expanding mode [01]
The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.
In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost. Port P2 becomes the data bus of D_7～D_0 (including instruction code) and loses its normal I/O functions. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively when ϕ enters into the "H" state. Port $P3_2$ functions as an input port during this same transition.

(3) Microprocessor mode [10]
After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode.
In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the data bus (D_7～D_0) and loses its normal I/O functions. Port $P3_1$ and $P3_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]
When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.
In this mode, the internal ROM is inhibited so the external memory is requierd.
The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.
Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_1$ and $P3_0$ retain their original I/O function.
The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.
The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.
The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

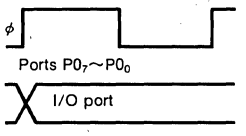
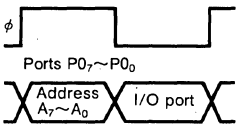
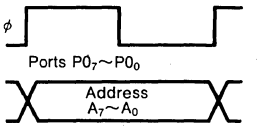
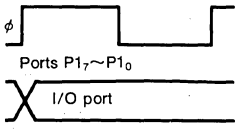
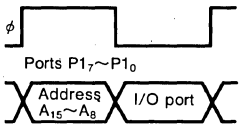
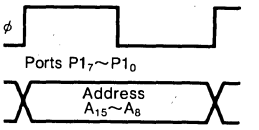
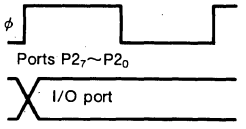
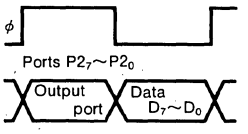
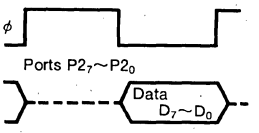
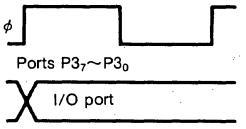
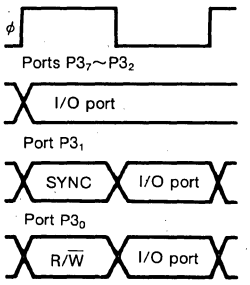
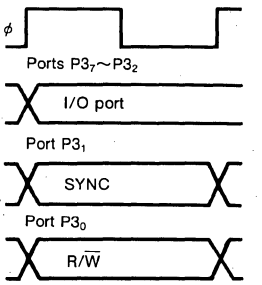
Port \ Mode	CM_1 = 0, CM_0 = 0 Single-chip mode	CM_1 = 1, CM_0 = 1 Eva-chip mode	CM_1 = 0, CM_0 = 1 Memory expanding mode	CM_1 = 1, CM_0 = 0 Microprocessor mode
Port P0				Same as left
Port P1				Same as left
Port P2				Same as left
Port P3				Same as left

Fig.15 Processor mode and functions of ports P0~P3

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 18.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleard when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 16.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock uasge is shown in Figure 17. X_{IN} is the input, and X_{OUT} is open.

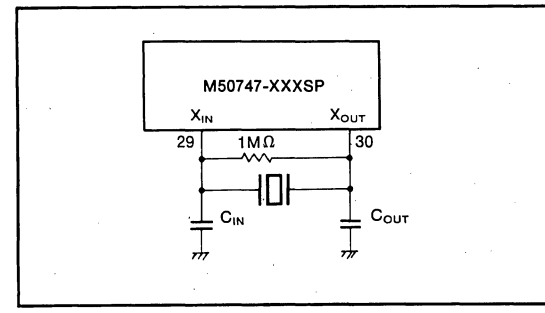


Fig.16 External ceramic resonator circuit

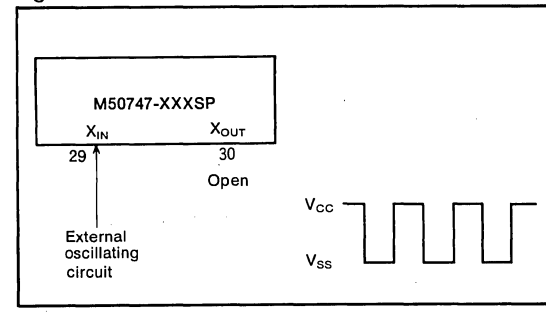


Fig.17 External clock input circuit

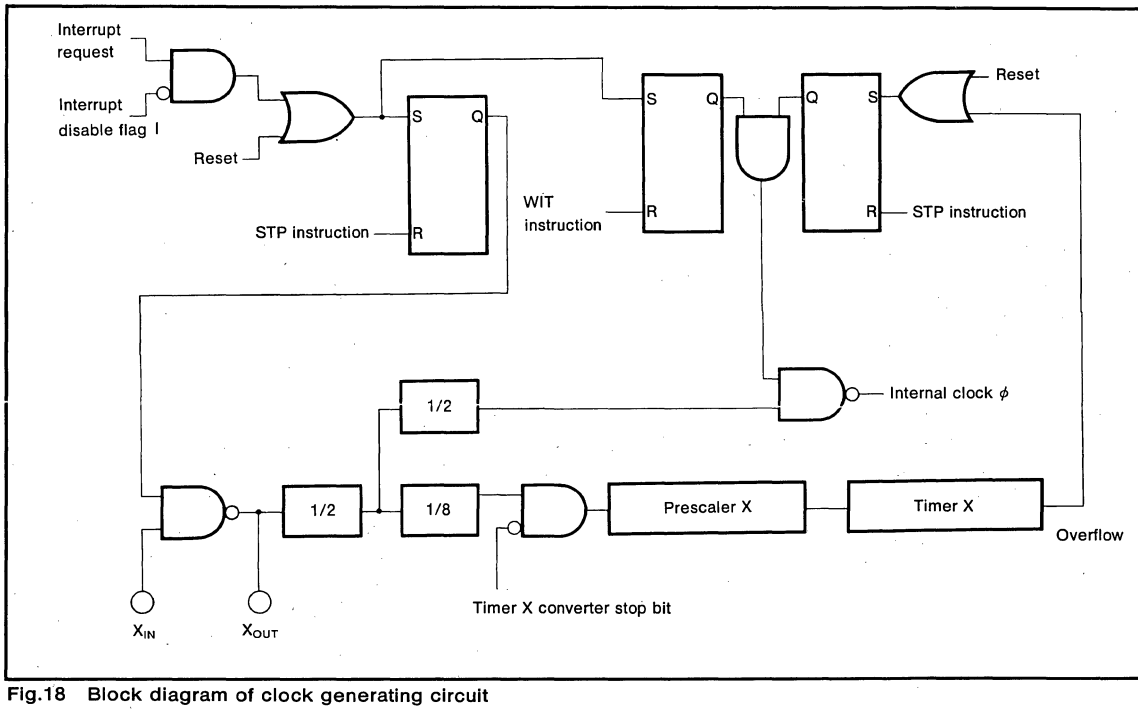


Fig.18 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(5) A NOP instruction must be used after the execution of a PLP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ..... EPROM 3sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off	−0.3~7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, $\overline{INT_1}$, $P5_0$~$P5_7$		−0.3~7	V
V_I	Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$,		−0.3~V_{CC}+0.3	V
V_I	Input voltage, CNV_{SS}		−0.3~13	V
V_O	Output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$, X_{OUT}, ϕ		−0.3~V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
T_{opr}	Operating temperature		−10~70	℃
Tstg	Storage temperature		−40~125	℃

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$ (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7P6_0$~$P6_7$, (Note 2)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			8	MHz

Note 2 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms
3 : Total of $I_{OL(peak)}$, of ports P0, P1, and P2 is 20mA
Total of $I_{OH(peak)}$, of ports P0, P1, and P2 is 20mA
Total of $I_{IL(peak)}$, of ports P3, P4, and P6 is 80mA
Total of $I_{OH(peak)}$, of ports P3 and P4 is 20mA
Let the total of $I_{OH(peak)}$, of ports P6 below 60mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OH} = −10mA		3			V
V_{OH}	"H" output voltage, ϕ	I_{OH} = −2.5mA		3			V
V_{OL}	"L" output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OL} = 10mA				2	V
V_{OL}	"L" output voltage, ϕ	I_{OL} = 5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_6$	When used as CLK input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{INT_1}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_7$	When used as $\overline{INT_2}$ pin		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_3$	When used as CNTR input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis, X_{IN}			0.1		0.5	V
I_{IL}	"L" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 0V				−5	μA
I_{IH}	"H" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 5V				5	μA
V_{RAM}	RAM retention voltage	At stop mode		2			V
I_{CC}	Supply current	Output terminals are opened, others to V_{SS}	$f_{(X_{IN})}$ = 8MHz Square wave		6	12	mA
			At stop mode T_a = 25℃			1	μA
			At stop mode T_a = 70℃			10	μA

TIMING REQUIREMENTS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time	200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time	20			ns
t_C	External clock input cycle time	125			ns
t_W	External clock input pulse width	62			ns
t_r	External clock rising edge time			20	ns
t_f	External clock falling edge time			20	ns

Eva-chip mode and microprocessor mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	150			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Memory expanding mode and microprocessor mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	150			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.19			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns

Eva-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.19			150	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				150	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				150	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				150	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				150	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				150	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				150	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				150	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				150	ns

Memory expanding mode and microprocessor mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.19			150	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time		30		150	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				150	ns

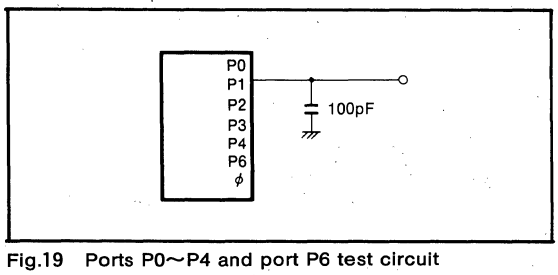
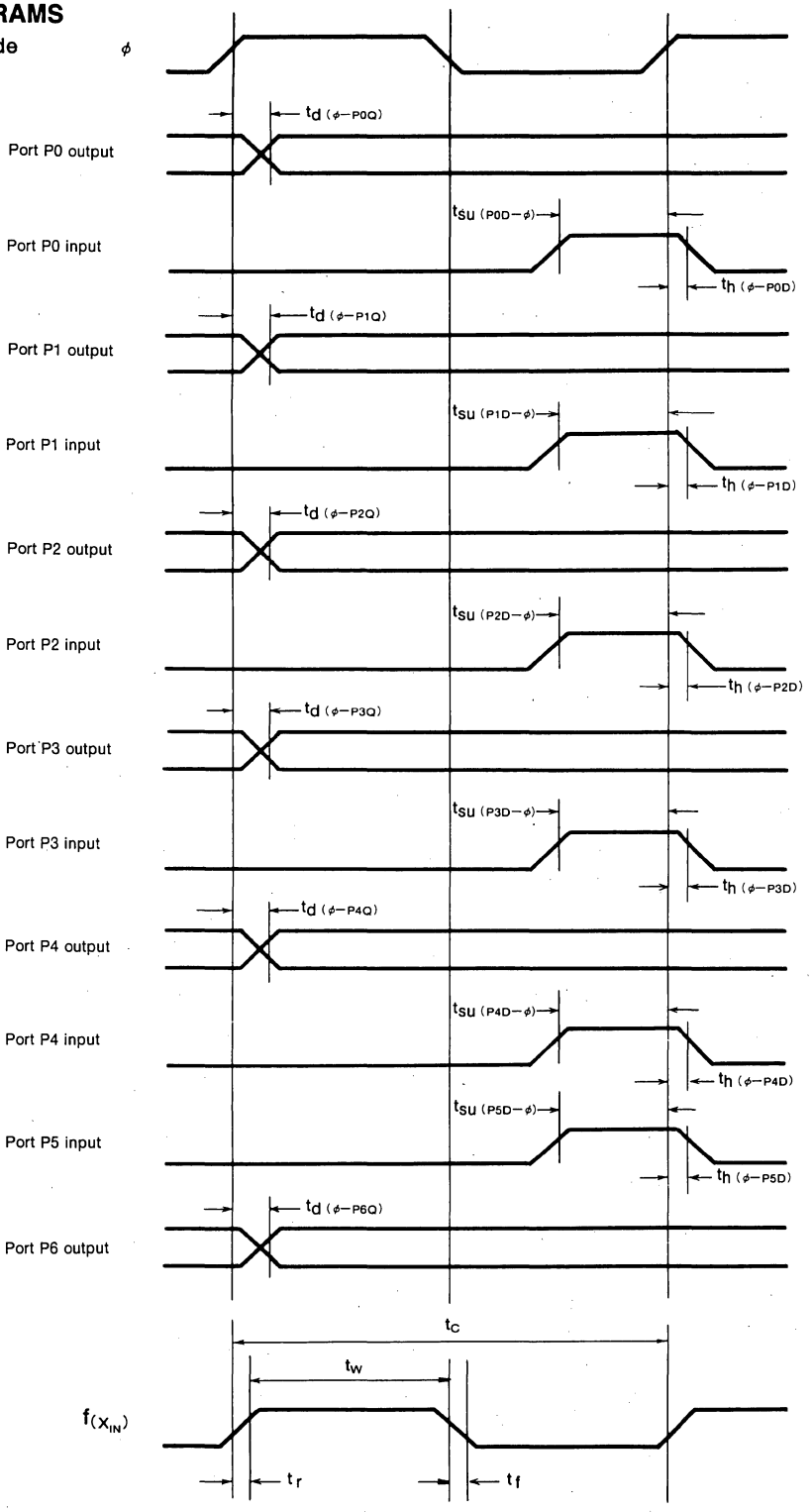


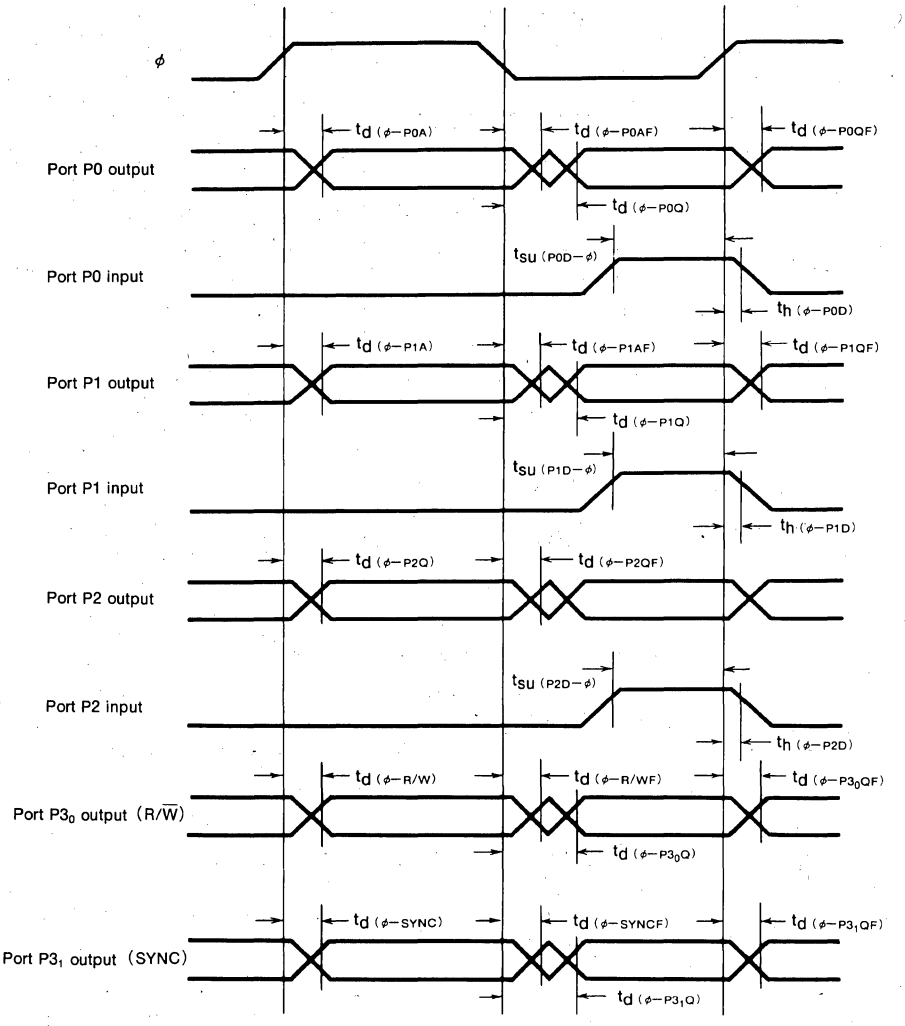
Fig.19 Ports P0~P4 and port P6 test circuit

TIMING DIAGRAMS

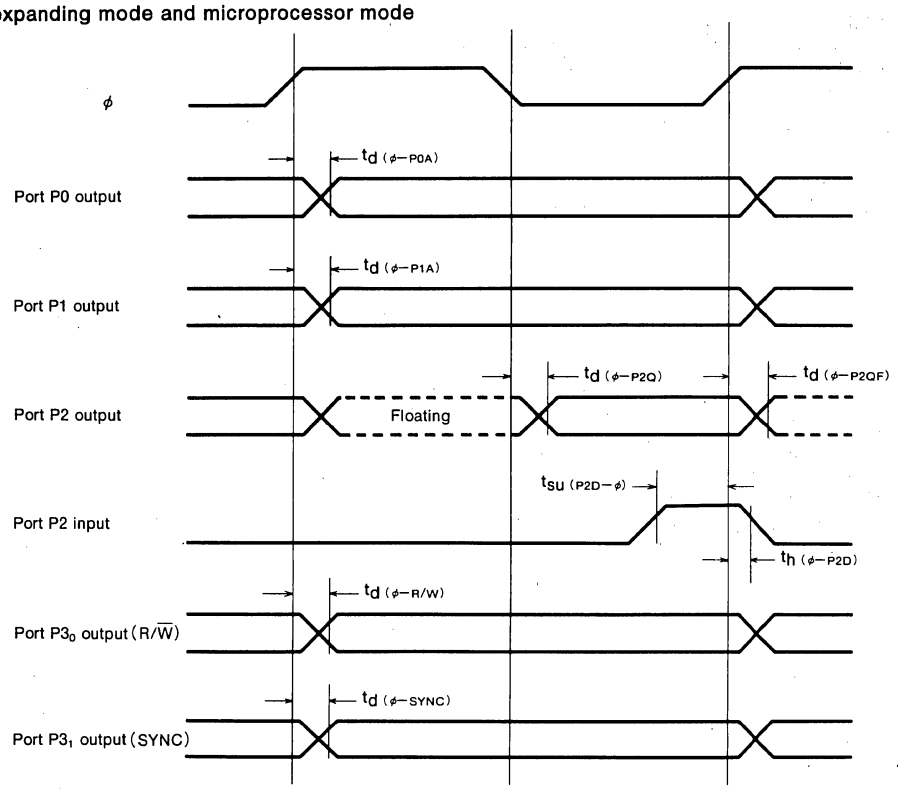
In single-chip mode



In eva-chip mode



In memory expanding mode and microprocessor mode



M50747H-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50747H-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP (flat package type also available). This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

In this section, the following explanations apply to the differences between the M50747-XXXSP and the M50747H-XXXSP. Other functions are explained in the M50747-XXXSP's section in detail.

Type name	Maximum value of clock generating frequency
M50747-XXXSP	8MHz
M50747H-XXXSP	12MHz

The differences between the M50747H-XXXSP and the M50747H-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

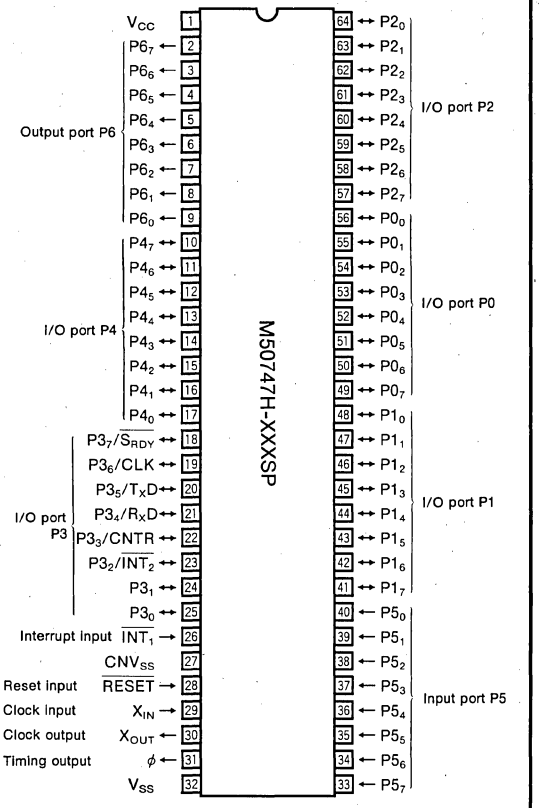
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 8192 bytes
  RAM ..... 256 bytes
- Instruction execution time
  .....0.66μs (minimum instructions at 12MHz frequency)
- Single power supply f(X_{IN})=12MHz ..... 5V±5%
- Power dissipation
  normal operation mode (at 12MHz frequency) 45mW
- Subroutine nesting ..... 128 levels (Max.)
- Interrupt ..... 7 types, 5 vecters
- 8-bit timer ..... 3 (2 when used as serial I/O)
- Programmable I/O (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Output ports (Port P6) 8
- Serial I/O (Clock synchronized or UART) 1

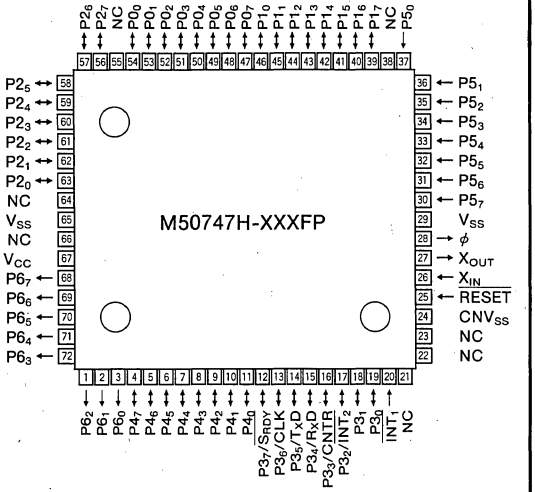
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

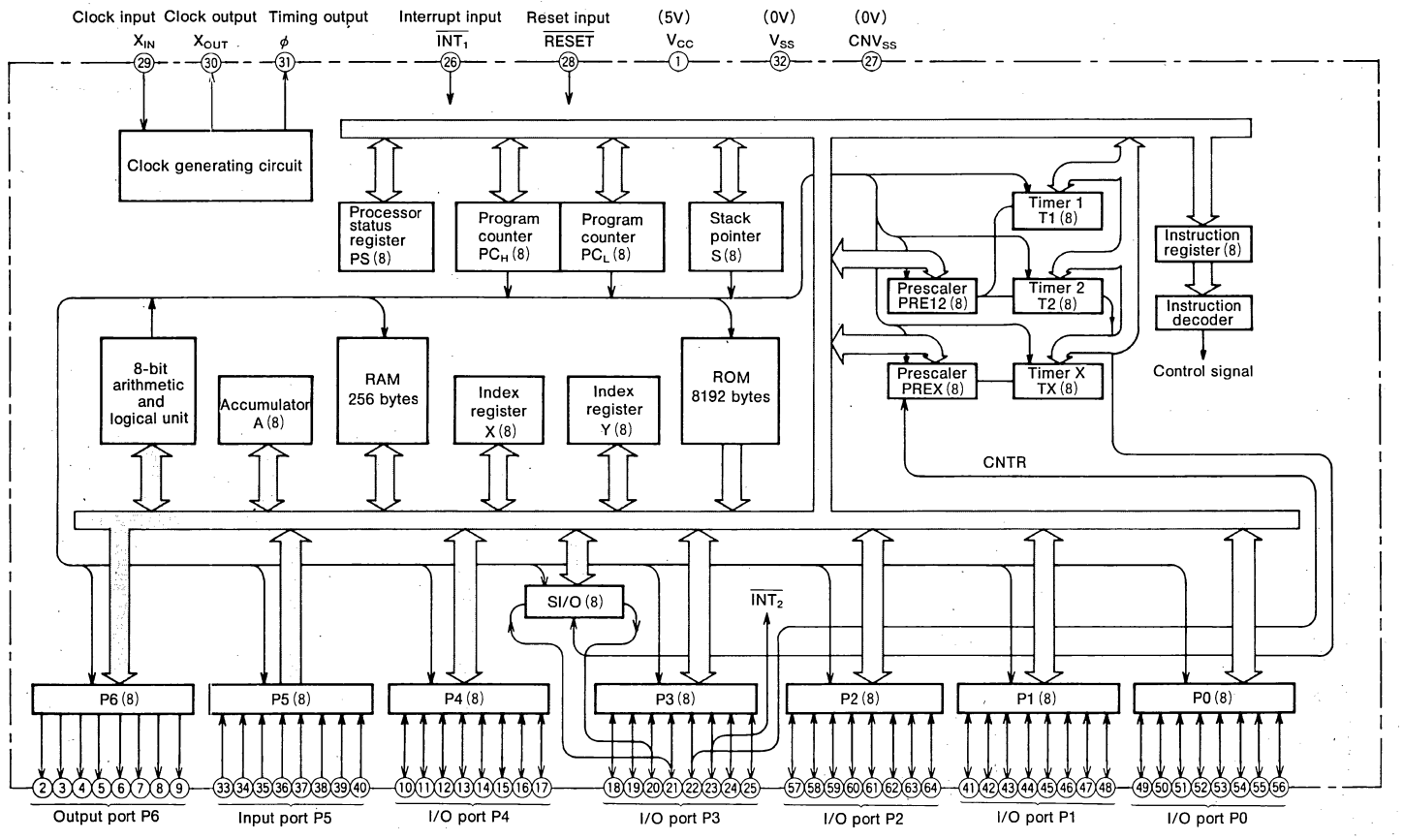


Outline 72P6

NC : No connection

MITSUBISHI ELECTRIC

M50747H-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M50747H-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			0.66μs (minimum instructions, at 12MHz of frequency)
Clock frequency			12MHz
Memory size	ROM		8192bytes
	RAM		256bytes
Input/output port	$\overline{INT_1}$	Input	1-bit×1
	P0, P1, P2, P3, P4	I/O	8-bit×5 (Part of P3 are in common with Input/output of serial I/O, timer I/O and $\overline{INT_2}$ interrupt input)
	P5	Input	8-bit×1
	P6	Output	8-bit×1
Serial I/O			8-bit or 9-bit×1
Timers			8-bit prescaler×2+8-bit timer×3 (8-bit timer×2 when serial I/O is used)
Subroutine nesting			128levels (max.)
Interrupts			Two external interrupts (1 of external interrupt is in common with port $P3_2$) Three timer interrupts (or timer×2, serial I/O×1)
Clock generating circuit			Built-in (Ceramic or Quartz crystal oscillator)
Supply voltage			5V±5%
Power dissipation	at high-speed operation		45mW (at 12MHz frenquency)
Input/output characteristics	Input/output voltage		5V
	Output current		10mA (Ports P3, P4, P6)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package	M50747H-XXXSP		64-pin shrink plastic molded DIP
	M50747H-XXXFP		72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_6$, $P3_5$, and $P3_4$ work as CLK, T_XD pins, respectively. When clock synchronous serial I/O is used, $P3_7$ works as $\overline{S_{RDY}}$. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest order interrupt input pin ($\overline{INT_2}$), respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
$P6_0$~$P6_7$	Output port P6	Output	Port P6 is an 8-bit output port. The output structure is CMOS output.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off	−0.3~7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, $\overline{INT_1}$, $P5_0$~$P5_7$		−0.3~7	V
V_I	Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$,		−0.3~V_{CC}+0.3	V
V_I	Input voltage, CNV_{SS}		−0.3~13	V
V_O	Output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$, X_{OUT}, ϕ		−0.3~V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000 (Note 1)	mW
T_{opr}	Operating temperature		−10~70	℃
Tstg	Storage temperature		−40~125	℃

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5V±5%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$ (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7P6_0$~$P6_7$, (Note 2)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			12	MHz

Note 2 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms
3 : Total of $I_{OL(peak)}$, of ports P0, P1, and P2 is 20mA
Total of $I_{OH(peak)}$, of ports P0, P1, and P2 is 20mA
Total of $I_{IL(peak)}$, of ports P3, P4, and P6 is 80mA
Total of $I_{OH(peak)}$, of ports P3 and P4 is 20mA
Let the total of $I_{OH(peak)}$, of ports P6 below 60mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 12MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OH} = −10mA		3			V
V_{OH}	"H" output voltage, ϕ	I_{OH} = −2.5mA		3			V
V_{OL}	"L" output voltage, $P0_0$~ $P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OL} = 10mA				2	V
V_{OL}	"L" output voltage, ϕ	I_{OL} = 5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_6$	When used as CLK input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{INT_1}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_2$	When used as $\overline{INT_2}$ pin		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_3$	When used as CNTR input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis, X_{IN}			0.1		0.5	V
I_{IL}	"L" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 0V				−5	μA
I_{IH}	"H" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 5V				5	μA
V_{RAM}	RAM retention voltage	At stop mode		2			V
I_{CC}	Supply current	Output terminals are opened, others to V_{SS}	$f_{(X_{IN})}$ = 12MHz Square wave		9	18	mA
			At stop mode T_a = 25℃			1	μA
			At stop mode T_a = 70℃			10	μA

TIMING REQUIREMENTS

Single-chip mode (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 12MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	100			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	100			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	100			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	100			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	100			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time	100			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time	20			ns
t_c	External clock input cycle time	83			ns
t_w	External clock input pulse width	41			ns
t_r	External clock rising edge time			20	ns
t_f	External clock falling edge time			20	ns

Eva-chip mode and microprocessor mode

(V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 12MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	100			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	100			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	75			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Memory expanding mode and microprocessor mode

(V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 12MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	75			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 12MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 1			150	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				150	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				150	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				150	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				150	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				150	ns

Eva-chip mode (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 12MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 1			140	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				140	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				150	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				140	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				140	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				140	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				150	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				140	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				150	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				140	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				140	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				140	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				150	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				140	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				140	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				140	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				150	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				140	ns

Memory expanding mode and microprocessor mode

(V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 12MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 1			140	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				140	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				155	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time		40		140	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				140	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				140	ns

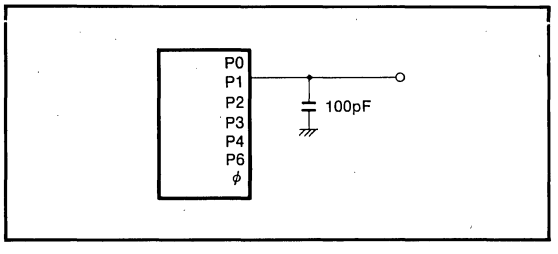
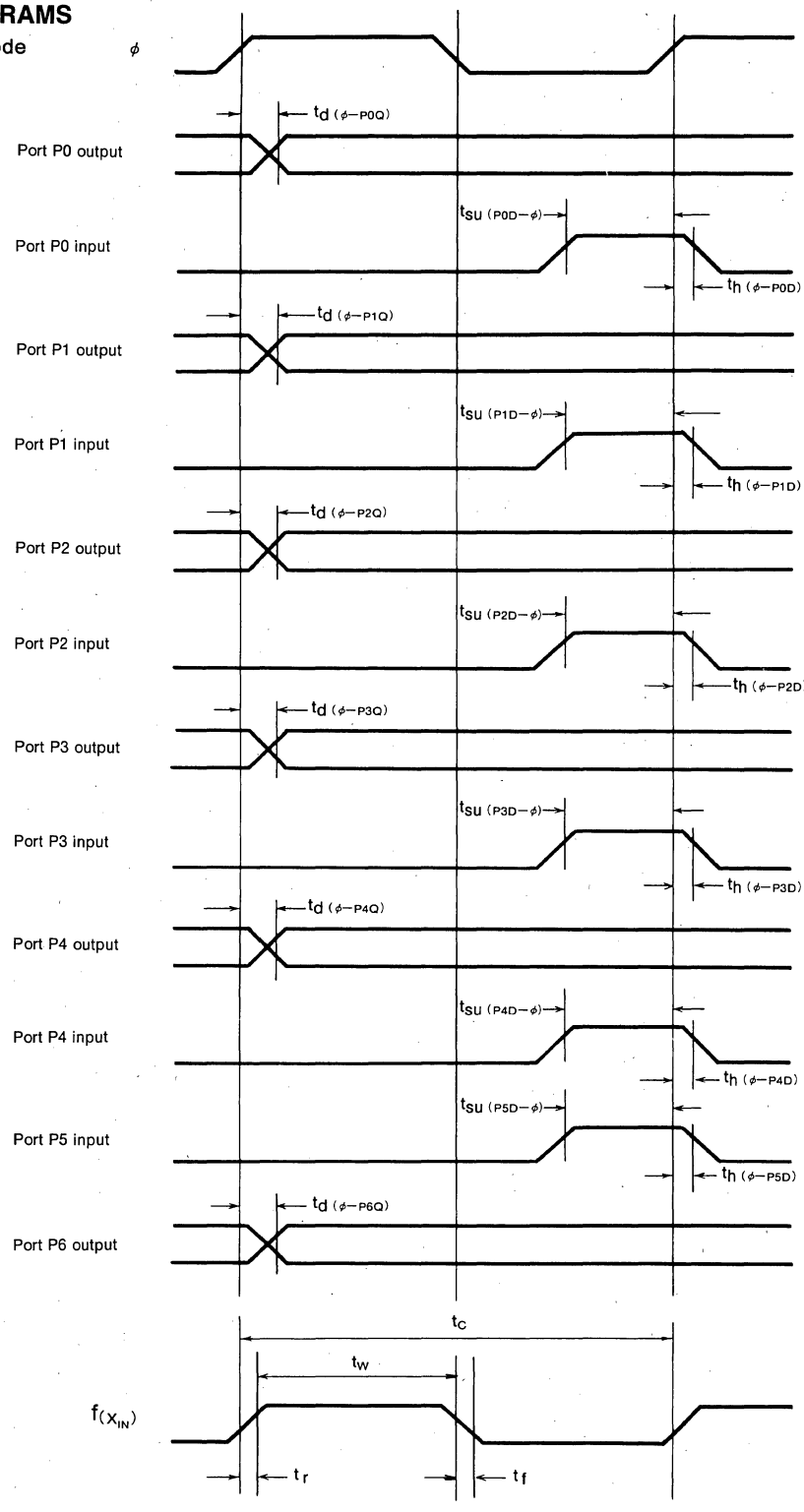


Fig.1 Ports P0～P4 and port P6 test circuit

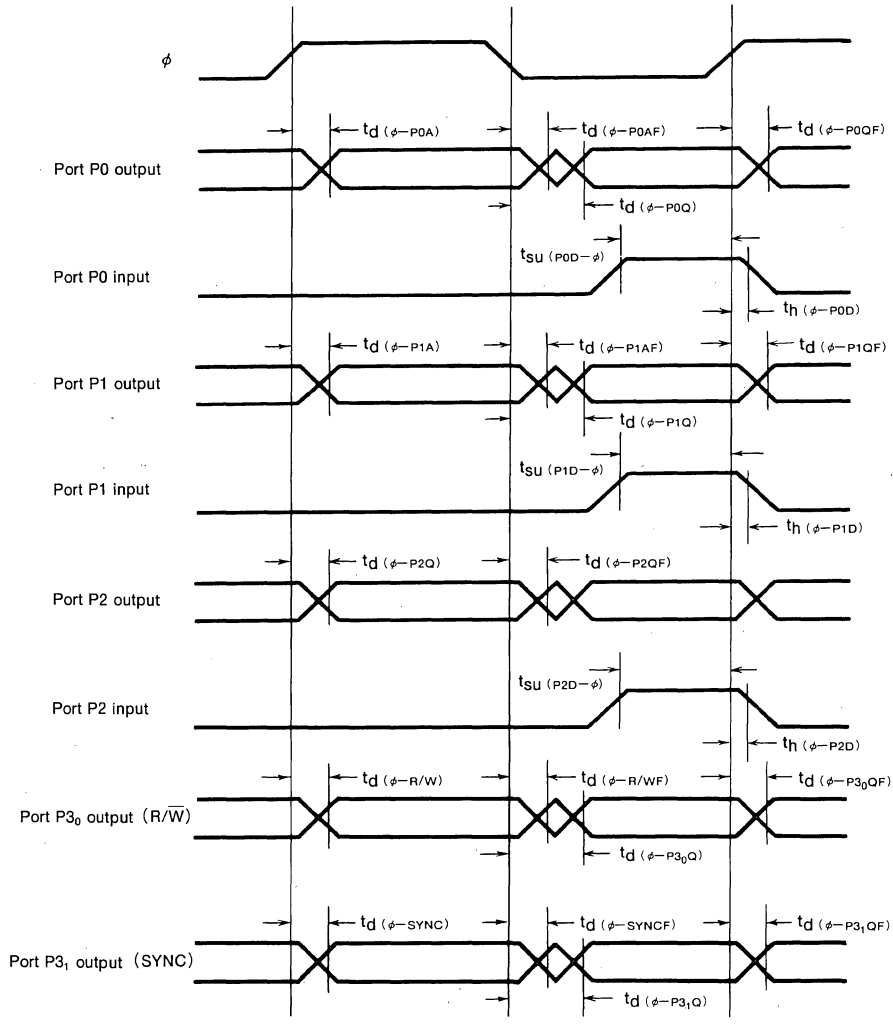
TIMING DIAGRAMS

In single-chip mode

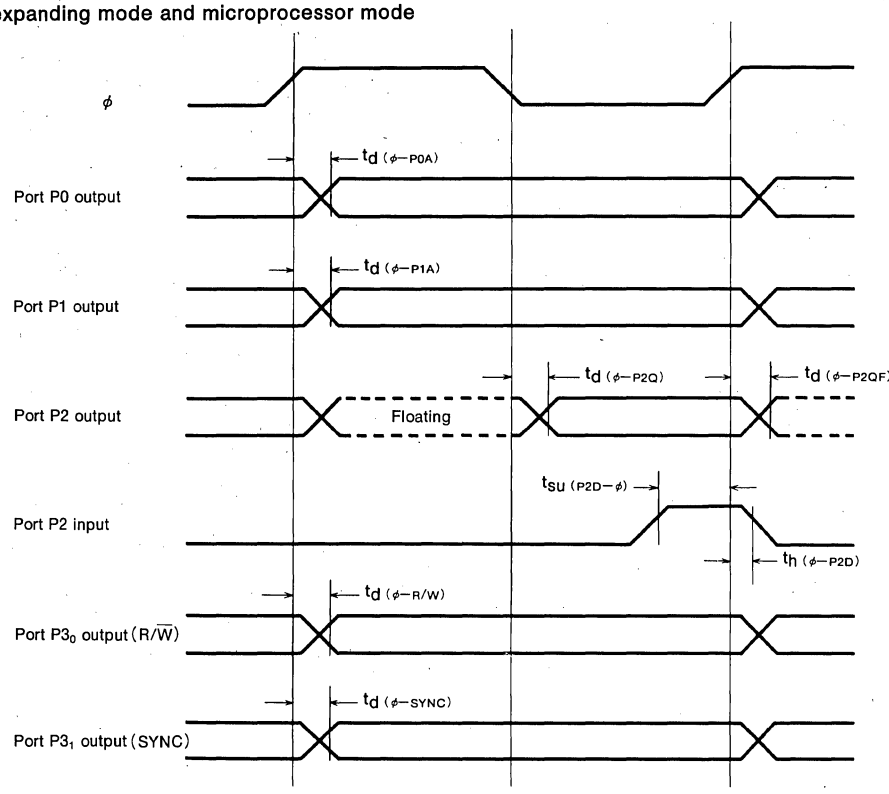


MITSUBISHI ELECTRIC

In eva-chip mode



In memory expanding mode and microprocessor mode



M50752-XXXSP, M50757-XXXSP M50758-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50752-XXXSP, M50757-XXXSP and the M50758-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. These are housed in a 52-pin shrink plastic molded DIP.

These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences among M50752-XXXSP, M50757-XXXSP and M50758-XXXSP are noted below. The difference between M50757-XXXSP and M50758-XXXSP is the clock oscillating circuit only.

Type name	ROM size	RAM size	51 pin name
M50752-XXXSP	4096bytes	128bytes	V_{CC}
M50757-XXXSP	3072bytes	96bytes	NC
M50758-XXXSP	3072bytes	96bytes	NC

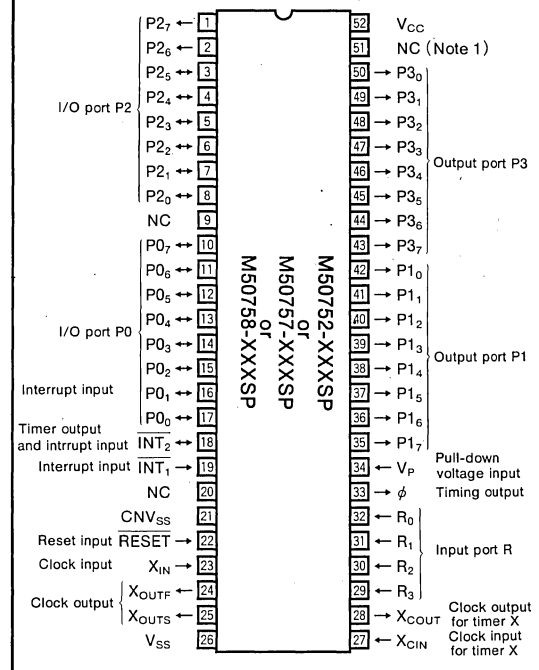
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size
  ROM ..... 3072 bytes (M50757-XXXSP, M50758-XXXSP)
  4096 bytes (M50752-XXXSP)
  RAM ..... 96 bytes (M50757-XXXSP, M50758-XXXSP)
  128 bytes (M50752-XXXSP)
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz ..... 5V±10%
- Power dissipation
  normal operation mode, at 4MHz frequency 15mW
- Subroutine nesting ..... 48 levels (Max.)
- Interrupt ..... 6 types, 5 vecters
- 8-bit timer 3
- Programmable I/O ports (Ports P0, $P2_0$~$P2_5$) 14
- Input port (Port R) 4
- High-voltage output ports (Ports P1, P3, $P2_6$, $P2_7$) 18

APPLICATION

VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)

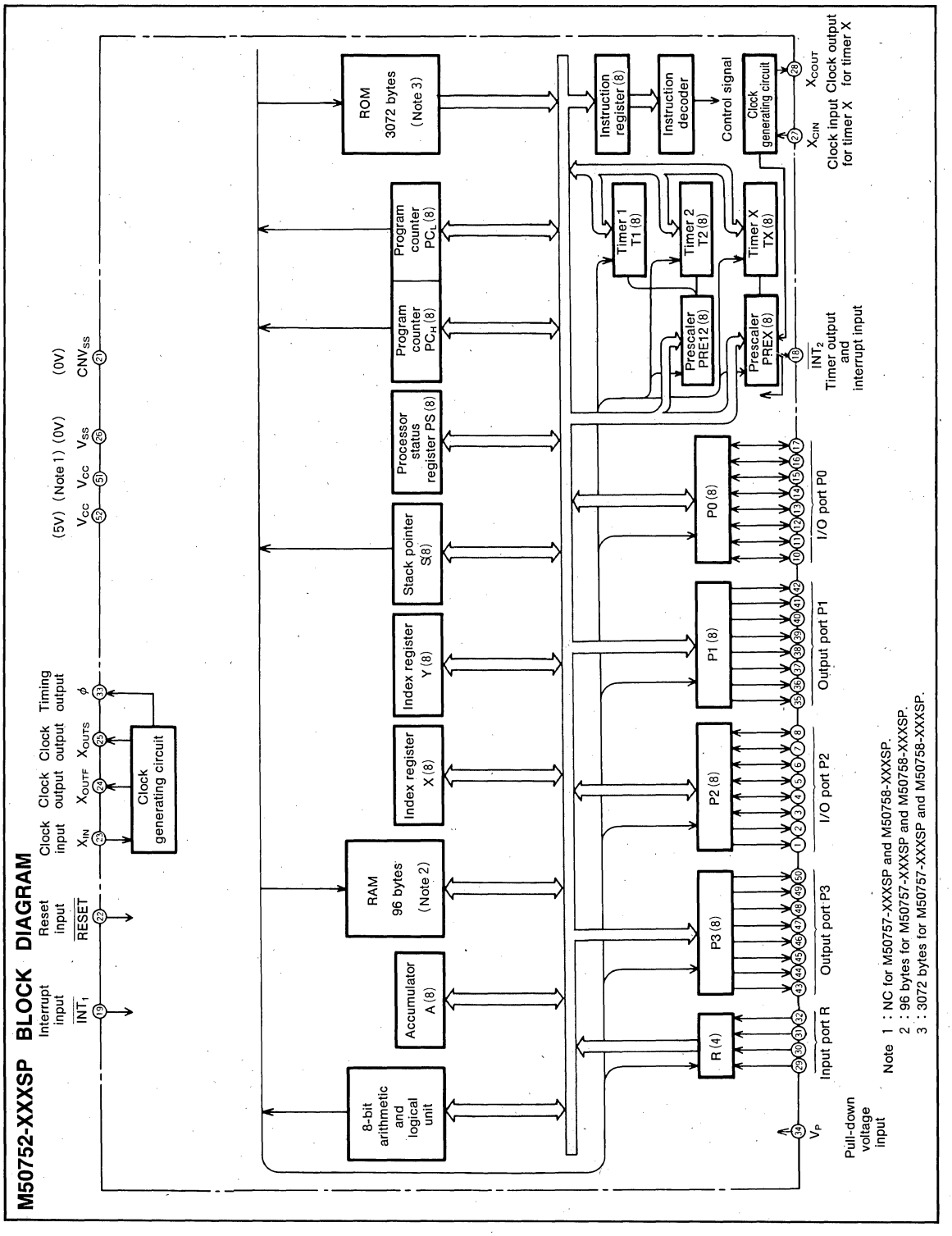


Outline 52P4B

NC : No connection

Note 1 : Pin number 51 is V_{CC} for M50752-XXXSP

M50752-XXXSP BLOCK DIAGRAM



Note 1 : NC for M50757-XXXSP and M50758-XXXSP.
2 : 96 bytes for M50757-XXXSP and M50758-XXXSP.
3 : 3072 bytes for M50757-XXXSP and M50758-XXXSP.

M50752-XXXSP, M50757-XXXSP M50758-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M50752-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory size	ROM		4096bytes (3072bytes for M50757-XXXSP and M50758-XXXSP)
	RAM		128bytes (96bytes for M50757-XXXSP and M50758-XXXSP)
Input/Output ports	R	Input	4-bit×1
	$\overline{INT_1}$	Input	1-bit×1
	P1, P3, $P2_6$, $P2_7$	Output	8-bit×2+2bit
	$\overline{INT_2}$	I/O	1-bit×1
	P0, $P2_0$~$P2_5$	I/O	8-bit×1+6-bit
Timers			8-bit prescaler×2+8-bit timer×3
Subroutine nesting			64 levels (max)(48levels for M50757-XXXSP and M50758-XXXSP)
Interrupts			Two external interrupts, Three internal timer interrupts
Clock generating circuit	for system clock		Built-in (RC oscillation, ceramic oscillator for M50758-XXXSP)
	for timer X		Built-in (quartz crystal oscillator)
Supply voltage	at normal operating		5V±10%
Power dissipation	at high-speed operation		15mW (at 4MHz frequency)
	at low-speed operation		4mW (at 20kH frequency)
Input/Output characteristics	Input/Output voltage		V_{CC}−33V (Ports P1, P3, $P2_6$~$P2_7$)
	Output current		10mA (Ports P0, $P2_0$~$P2_5$), −12mA (Ports P1, P3, $P2_6$~$P2_7$)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package			52-pin shrink plastic molded DIP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P1, P3, $P2_6$ and $P2_7$.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, a resistor is connected between the X_{IN} and X_{OUTS} or the X_{OUTF} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUTS} and X_{OUTF} pins should be left open.
X_{OUTS}	Clock output	Output	This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a resistor between this pin and X_{IN} pin.
X_{OUTF}	Clock output	Output	This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a resistor between this pin and X_{IN} pin.
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock I/O for timer X	Input	These are I/O pins of the clock oscillating circuit for the timer X. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN}pin and X_{COUT} pin.
X_{COUT}		Output	
$\overline{INT_1}$	Interrupt input	Input	This is the lowest order interrupt input pin.
$\overline{INT_2}$	Time output or interrupt input	I/O	This is in common with an output for the time X and an interrupt input pin.
R_0~R_3	Input port R	Input	Port R is a 4-bit input port.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port. The output structure is P-channel open drain.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. For $P2_6$ and $P2_7$ pins, output structure is P-channel open drain, and a pull-down transistor is built in between the V_P pin.
$P3_0$~$P3_7$	Output port P3	Output	Port P3 is an 8-bit output port and has basically the same functions as port P1.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50752-XXXSP is shown in Figure 1. Addresses 1000_{16} to $1FFF_{16}$ are assigned to the built-in ROM area which consists of 4096 bytes.

Addresses 1400_{16} to $1FFF_{16}$ are the ROM address area assigned to the M50757-XXXSP and M50758-XXXSP.

Addresses $1F00_{16}$ to $1FFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $1FF4_{16}$ to $1FFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $007F_{16}$ are assigned to the built-in RAM and consist of 128 bytes of static RAM. Address 0000_{16} to $005F_{16}$, an area of 96 bytes, assigned to M50757-XXXSP and M50758-XXXSP. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

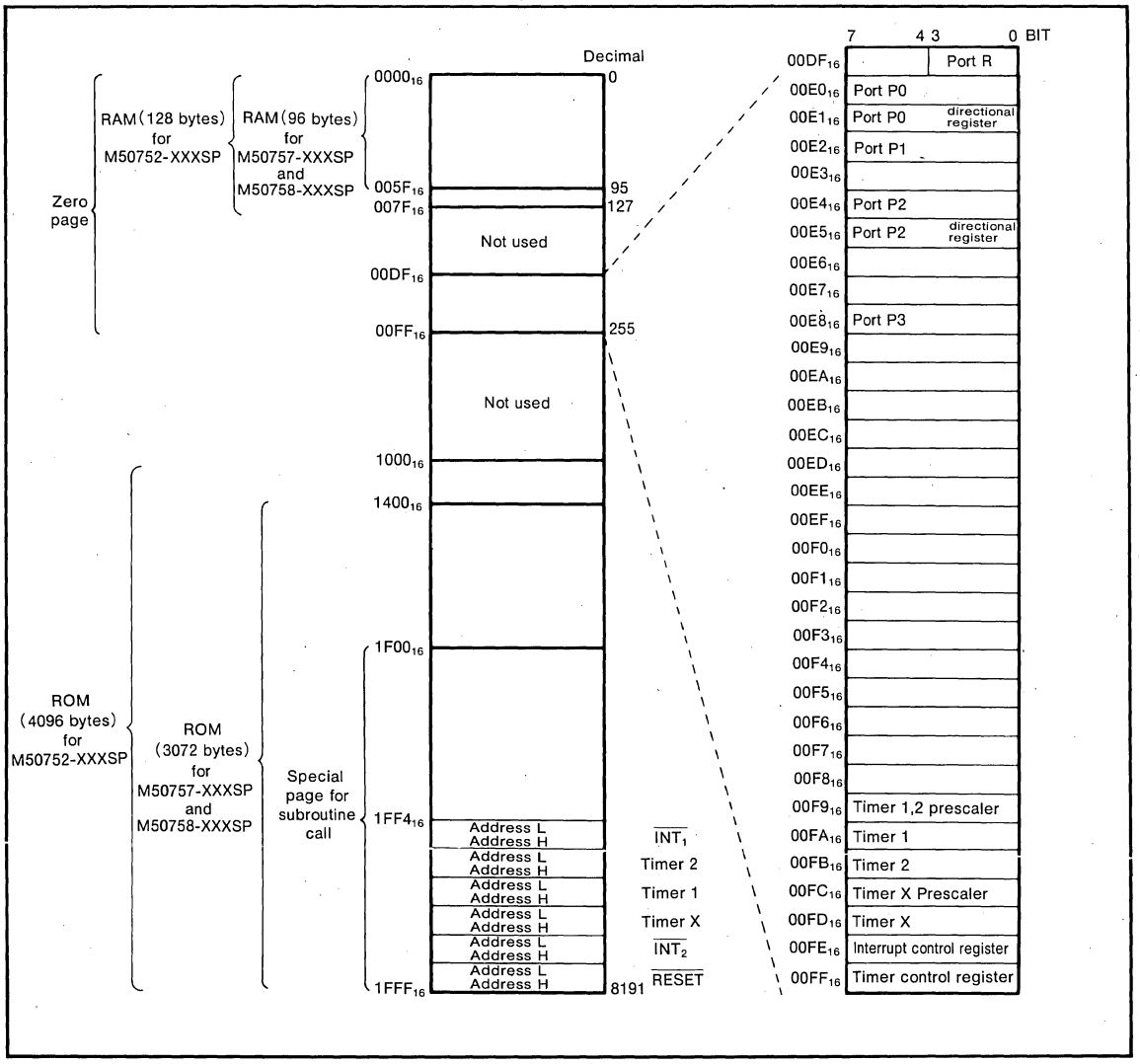


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, input/output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

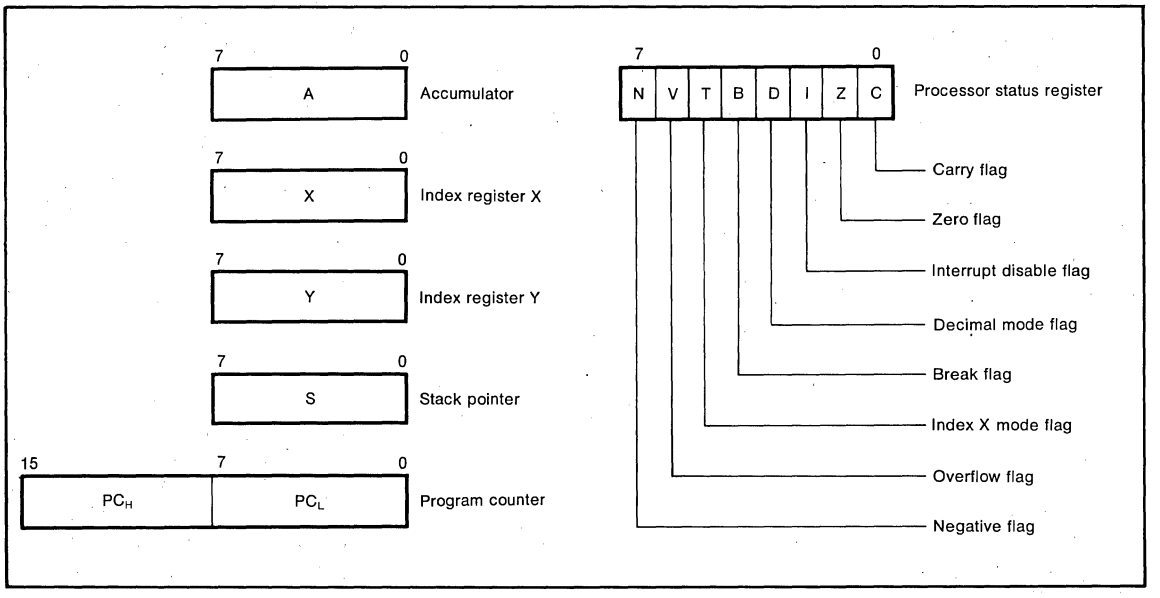


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When using this microcomputer in the single-chip mode, the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$1FFF_{16}$, $1FFE_{16}$
$\overline{\text{INT}_2}$	2	$1FFD_{16}$, $1FFC_{16}$
Timer X	3	$1FFB_{16}$, $1FFA_{16}$
Timer 1	4	$1FF9_{16}$, $1FF8_{16}$
Timer 2	5	$1FF7_{16}$, $1FF6_{16}$
$\overline{\text{INT}_1}$ (BRK)	6	$1FF5_{16}$, $1FF4_{16}$

INTERRUPT

The M50752-XXXSP can be interrupted from seven souces; $\overline{\text{INT}_2}$, timer X, timer 1, timer 2 or $\overline{\text{INT}_1}$/BRK instruction.

These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3.

An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{\text{INT}_1}$ or $\overline{\text{INT}_2}$ pins go from "H" to "L"

(2) When the contents of timer X, timer 1, timer 2 go to "0"

These request bits can be reset by the program but can not be set by the progream. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the $\overline{\text{INT}_1}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{\text{INT}_1}$ generated the interrupt.

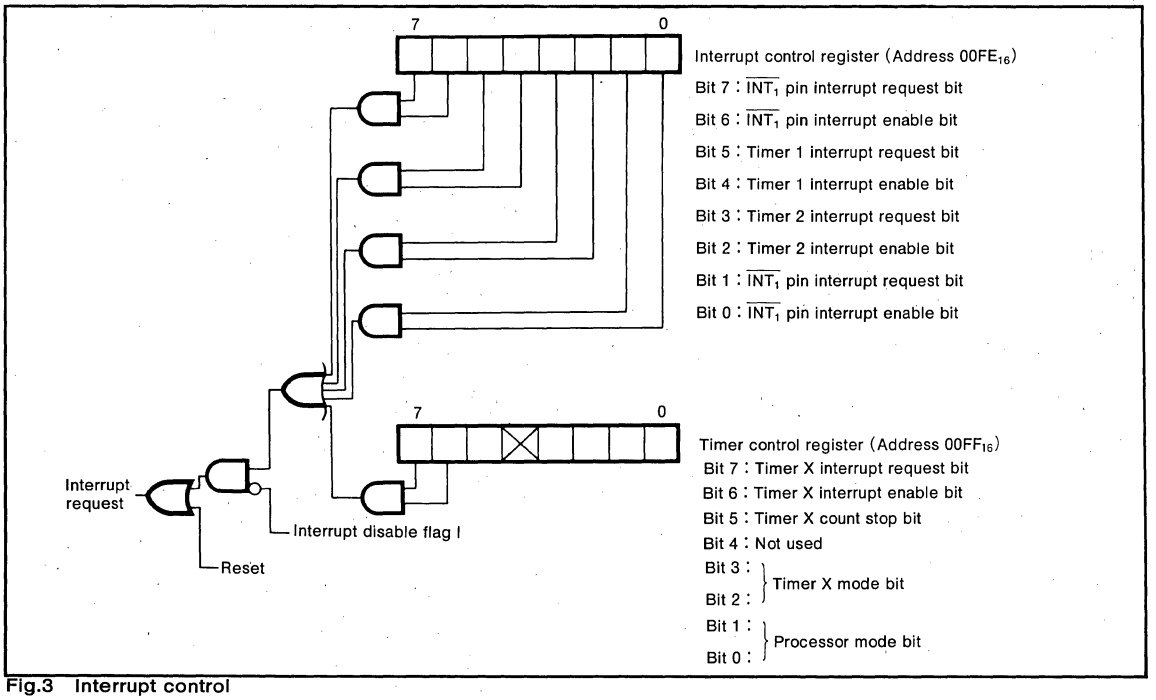


Fig.3 Interrupt control

TIMER

The M50752-XXXSP has three timers; timer X, timer 1, and timer 2. Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1 and timer 2 is shown in Figure 4.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+2)$, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see Interrupt section). The prescaler latch and timer latch can be loaded with any number except zero.

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the $\overline{INT_2}$ signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the X_{CIN} pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock sourse.

(4) Pulse width measurement mode [11]
This mode measures the pulse width (between lows) input to the X_{CIN} pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the X_{CIN} pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively.

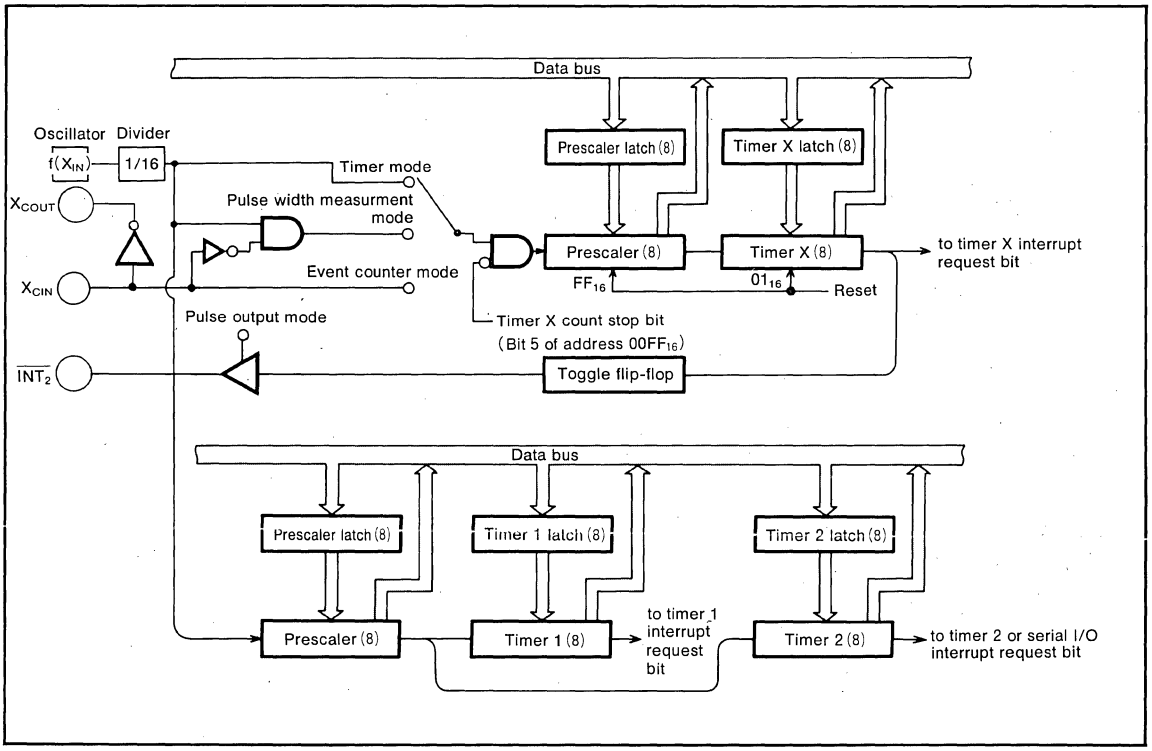


Fig.4 Block diagram of timer X, timer 1, timer 2

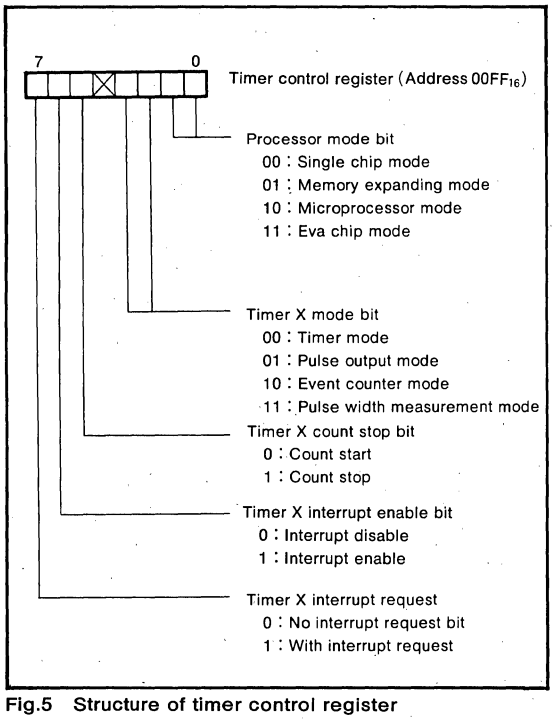


Fig.5 Structure of timer control register

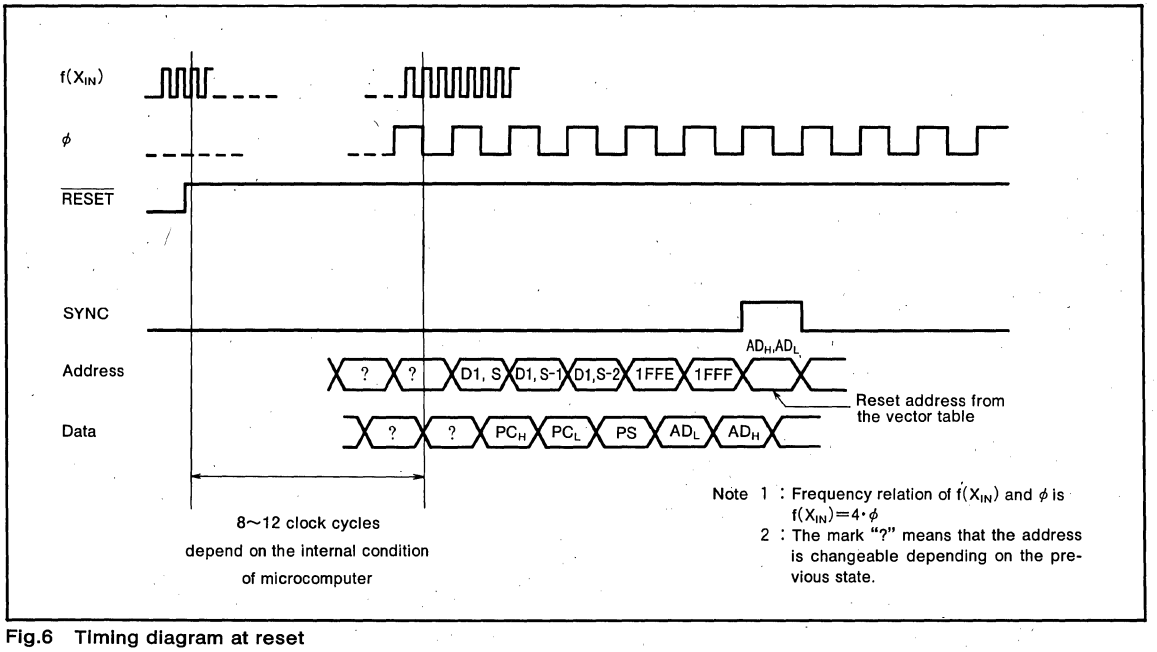


Fig.6 Timing diagram at reset

RESET CIRCUIT

The M50752-XXXSP is reset according to the sequence shown in Figure 6. It starts the program from the address formed by using the content of address $1FFF_{16}$ as the high order address and the content of the address $1FFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than $2\mu s$ while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 7.

An example of the reset circuit is shown in Figure 8.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

	Address	
(1) Port P0 directional register	($E1_{16}$) ···	00_{16}
(2) Port P1	($E2_{16}$) ···	00_{16}
(3) Port P2 directional register	($E5_{16}$) ···	00_{16}
(4) Port P3	($E8_{16}$) ···	00_{16}
(5) Prescaler X	(FC_{16}) ···	FF_{16}
(6) Timer X	(FD_{16}) ···	01_{16}
(7) Interrupt control register	(FE_{16}) ···	00_{16}
(8) Timer control register	(FF_{16}) ···	00_{16}
(9) Interrupt disable flag on the processor status register	(PS) ···	1
(10) Program counter	(PC_H) ···	Contents of address $FFFF_{16}$
	(PC_L) ···	Contents of address $FFFE_{16}$
(11) Internal oscillator output is connected to X_{OUTF} (same condition after FST instruction is excuted)		

Fig.7 Internal state of microcomputer at reset

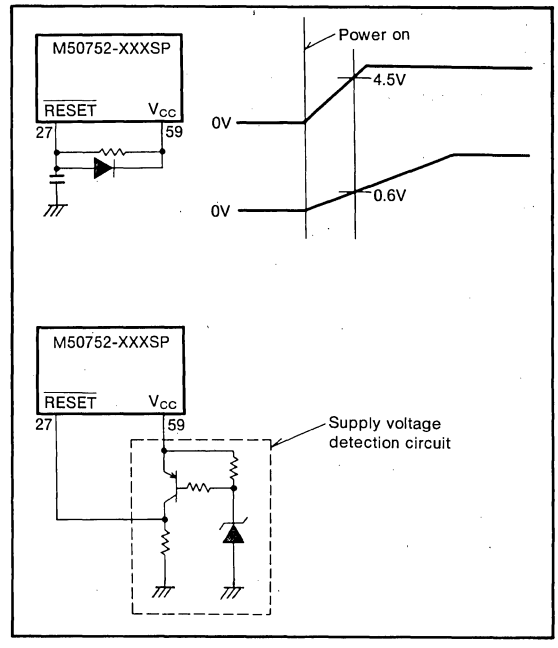


Fig.8 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

Port P1 is an 8-bit output port with high-breakdown voltage p-channel open-drain outputs featuring a breakdown voltage of V_{CC}-33V. Each pin contains a pull-down resistor making V_P a negative power source. As shown in the memory map in Figure 1, port P0 is used on the zero page at address $00E2_{16}$ in memory.

Except in the single-chip mode, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single chip mode, port $P2_6$, $P2_7$ has the same function as P1. And $P2_0 \sim P2_5$ has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0. This function does not change even though the processor mode changes. See Figure 9 for more details.

(5) Port R

Port R is an 4-bit input port. As shown in the memory map (Figure 1), port R can be accessed at the lower order 4 bits of zero page memory address $00DF_{16}$.

(6) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ.

(7) $\overline{INT_1}$ pin

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

(8) $\overline{INT_2}$ pin

The $\overline{INT_2}$ pin is an interrupt input pin. When this signal level changes from "H" to "L", the interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1". In the pulse output mode, the $\overline{INT_2}$ output changes polarity each time the contents of timer X goes to "0".

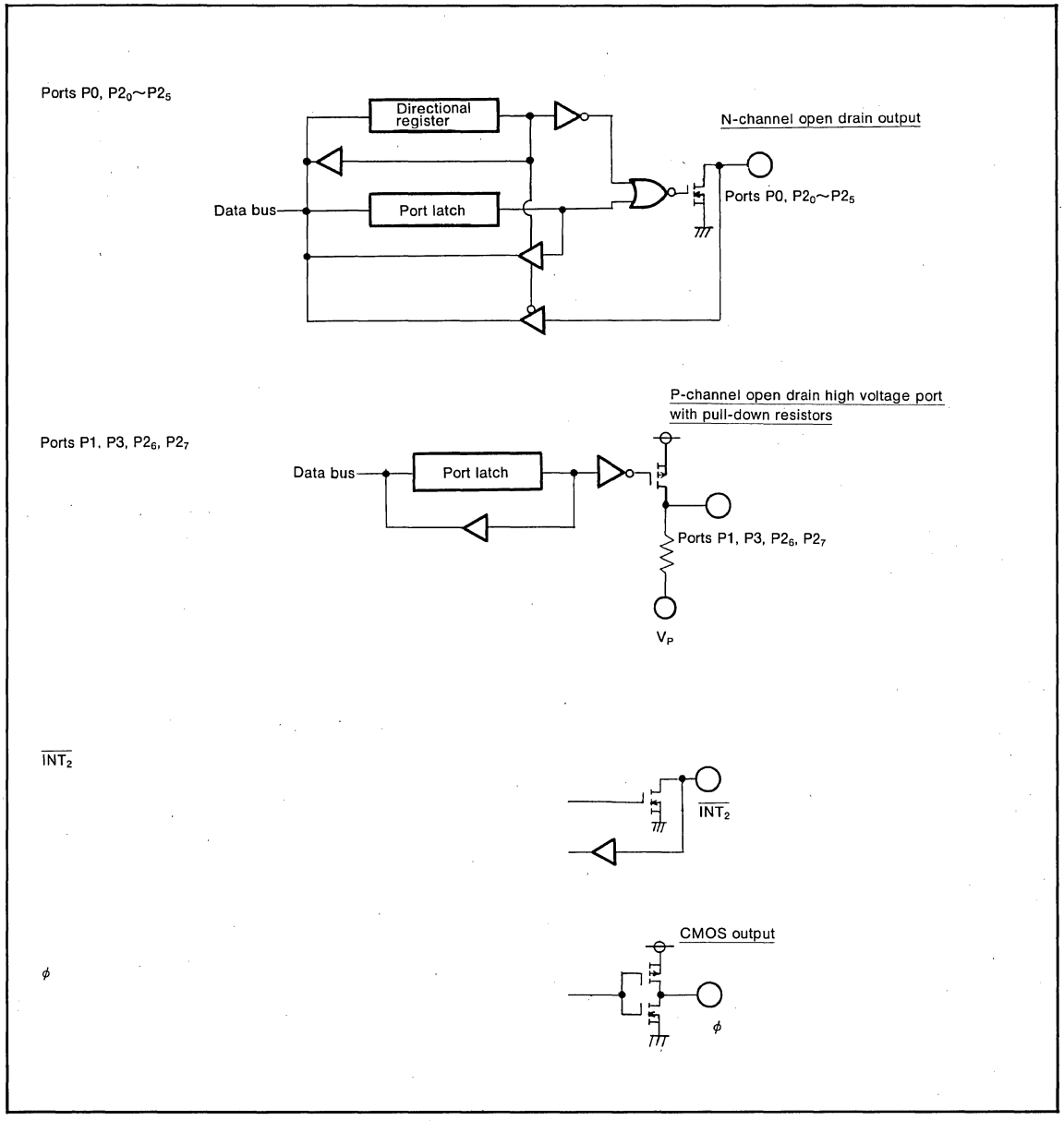


Fig.9 Block diagram of port P0~P3 (single-chip mode) and output formats of $\overline{INT_2}$, ϕ

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P2 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 11 shows the functions of ports P0～P2.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 10.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits.

Supplying "H" level to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

(1) Single-chip mode [00]
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P2 will work as original I/O ports.

(2) Memory expanding mode [01]
The microcomputer will be placed in the memory expansion mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.
The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.
Port P1's higher 5 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions.
Pins $P1_6$ and $P1_5$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P1_5$, $P1_6$ and $P1_7$ retain their original I/O function.
The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.
The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.
Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of $D_7 \sim D_0$ (including instruction code) while at the "L" state.

(3) Microprocessor mode [10]
In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port $P1_5$ and $P1_6$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost. Port P2 becomes the databus ($D_7 \sim D_0$) and loses its normal I/O functions. Insternal memory ($E1_{16}$ to $E0_{16}$) cannot be used, and an external memory is needed if the address where normal I/O function have lost.

(4) Eva-chip mode [11]
When "H" level is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.
With the exceptions that the internal ROM is disabled and that external memory must be attached in this mode is the same as the memory expanding mode.
The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

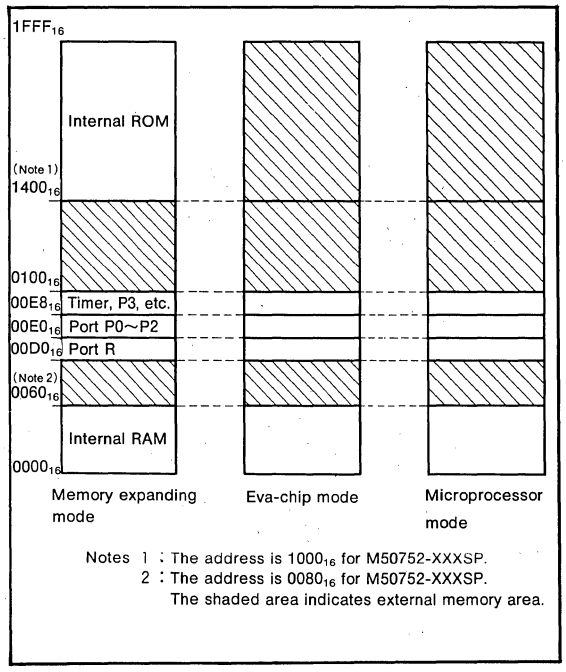


Fig.10 External memory area in processor mode

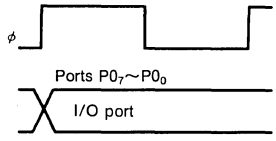
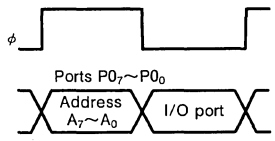
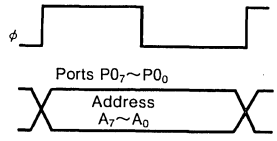
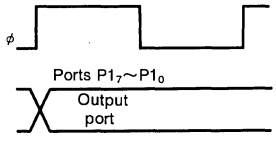
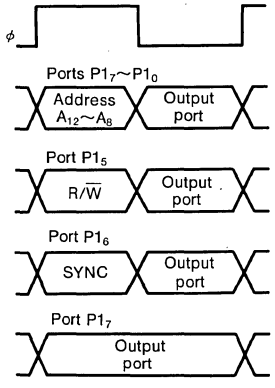
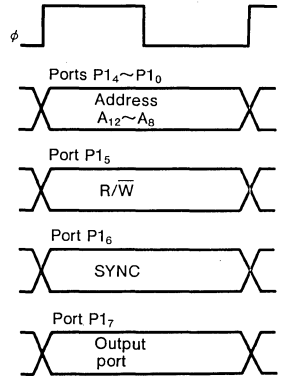
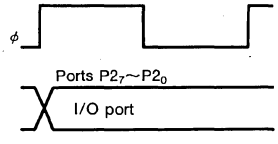
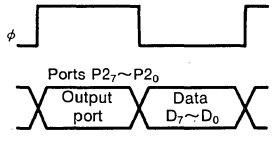
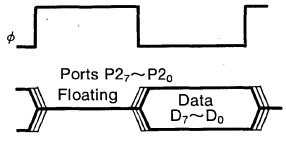
Port \ Mode	CM_1 = 0, CM_0 = 0 Single-chip mode	CM_1 = 0, CM_0 = 1 Memory expanding mode	CM_1 = 1, CM_0 = 1 Eva-chip mode	CM_1 = 1, CM_0 = 0 Microprocessor mode
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	

Fig.11 Processor mode and functions of ports P0~P2

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
"H" level	• Eva-chip mode	Eva-chip mode can be also selected by changing the processor mode bit with the program.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 12. When FST instruction is executed, SW_{OSC} is closed and when SLW instruction is executed, SW_{OSC} is open. These instructions are used, when CR oscillation is required, to change the oscillation frequency.

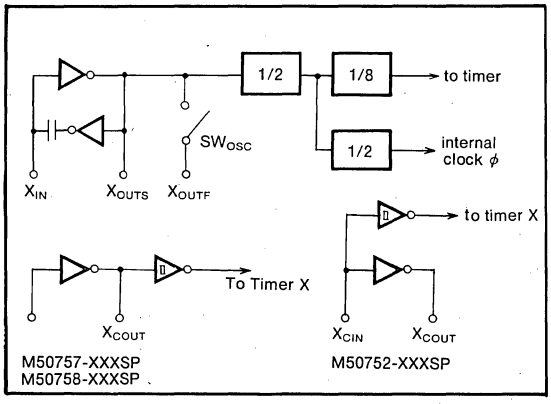


Fig.12 Block diagram of clock generating circuit

The circuit examples of clock generator are shown in Figures 13 ~ 17. The example when system clock signal is supplied from outside is shown in Figures 13 and 14. When clock signal is supplied from outside, let X_{IN} be the input, and open X_{OUTS} and X_{OUTF} (Figure 15).

The clock signal for Timer X can be supplied by planing the ceramic oscillation (or a quartz crystal oscillation) in outside. The constant of capacitance differs depending on oscillators. Therefore, try to adjust the recommended value of each oscillator manufactuer (Figure 16). In order to supply the clock signal from outside, let X_{CIN} be the input, and open X_{COUT} (Figure 17).

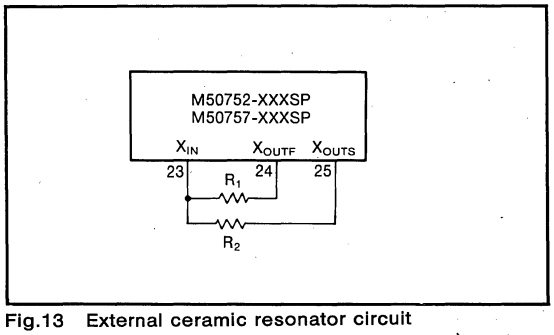


Fig.13 External ceramic resonator circuit (M50752-XXXSP and M50757-XXXSP)

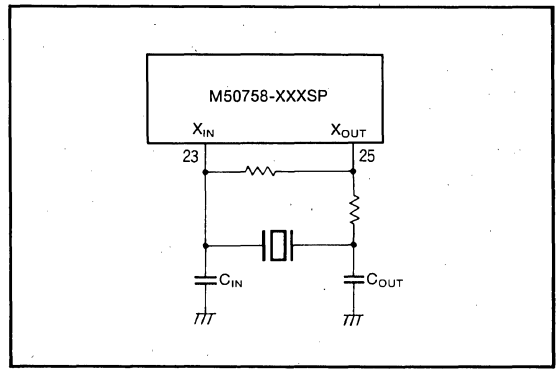


Fig.14 External oscillator circuit (M50758-XXXSP)

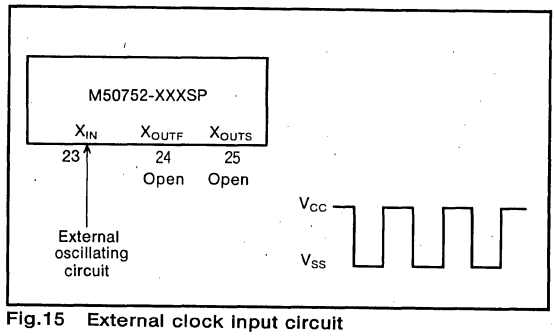


Fig.15 External clock input circuit

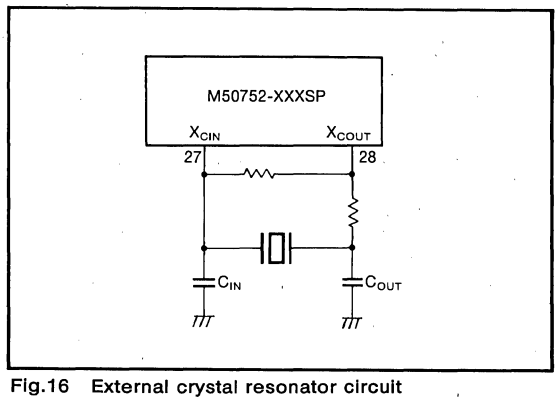


Fig.16 External crystal resonator circuit

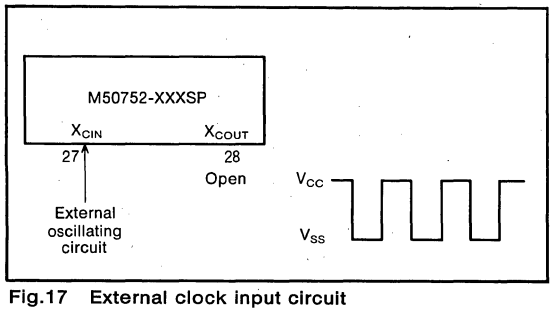


Fig.17 External clock input circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+2).
(2) Set a value other than "0" for the timer and the prescaler.
(3) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(4) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
(5) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(6) A NOP instruction must be used after the execution of a PLP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ..... EPROM 3sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power voltage	With respect to V_{SS}. Output transistors cut-off.	−0.3∼7	V
V_P	Power voltage		V_{CC}−35∼V_{CC}+0.3	V
V_I	Input voltage, R_3∼R_0, CNV_{SS}, $\overline{RESET}$, X_{IN}, X_{CIN}		−0.3∼7	V
V_I	Input voltage, $\overline{INT_1}$, $\overline{INT_2}$, $P0_0$∼$P0_7$, $P2_5$∼$P2_0$		−0.3∼13	V
V_O	Output voltage, X_{OUTF}, X_{COUT}, X_{OUTS}, ϕ		−0.3∼V_{CC}+0.3	V
V_O	Output voltage, $\overline{INT_2}$, $P0_7$∼$P0_0$, $P2_5$∼$P2_0$		−0.3∼13	V
V_O	Output voltage, $P1_7$∼$P1_0$, $P3_7$∼$P3_0$, $P2_7$, $P2_6$		V_{CC}−35∼V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
T_{opr}	Operating temperture		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −10∼70℃, V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Power voltage	4.5	5.0	5.5	V
V_P	Power voltage	V_{CC}−33		V_{CC}	V
V_{SS}	Power voltage		0		V
V_{IH}	"H" input voltage, $P0_0$∼$P0_7$, $P2_0$∼$P2_5$, $\overline{INT_1}$, $\overline{INT_2}$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, CNV_{SS}, X_{CIN}, $\overline{RESET}$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, X_{IN}	0.9V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, R_0∼R_3	0.4V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$∼$P0_7$, $P2_0$∼$P2_5$, CNV_{SS}, $\overline{INT_1}$, $\overline{INT_2}$ X_{CIN}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, R_0∼R_3, X_{IN}	0		0.12V_{CC}	V
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage, ϕ	V_{CC} = 5V, T_a = 25℃, I_{OH} = −2.5mA	3			V
V_{OH}	"H" output voltage, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P2_6$, $P2_7$	V_{CC} = 5V, T_a = 25℃, I_{OH} = −12mA	3			V
V_{OL}	"L" output voltage, ϕ	V_{CC} = 5V, T_a = 25℃, I_{OL} = 5mA			2	V
V_{OL}	"L" output voltage, $P0_0$∼$P0_7$, $P2_0$∼$P2_5$, $\overline{INT_2}$	V_{CC} = 5V, T_a = 25℃, I_{OL} = 10mA			2	V
V_{T+}−V_{T-}	Hysterisis, $\overline{INT_1}$, $\overline{INT_2}$	V_{CC} = 5V, T_a = 25℃	0.3		1	V
V_{T+}−V_{T-}	Hysterisis, $\overline{RESET}$	V_{CC} = 5V, T_a = 25℃		0.4	0.7	V
I_{OL}	"L" output current (Pull-down resistance) $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P2_6$, $P2_7$	V_P = V_{CC}−33V, V_{OL} = V_{CC}, T_a = 25℃	150		900	μA
I_{IL}	input leakage current, $\overline{INT_1}$, $\overline{INT_2}$, $P0_0$∼$P0_7$ $P2_0$∼$P2_5$	V_{CC} = 5V, T_a = 25℃ 0≦V_I≦5V	−5		5	μA
I_{IL}	input leakage current, CNV_{SS}, $\overline{RESET}$, X_{IN} X_{CIN}, R_0∼R_3	V_{CC} = 5V, T_a = 25℃ 0≦V_I≦5V	−5		5	μA
I_{IL}	input leakage current, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P2_6$, $P2_7$	V_{CC} = 5V, T_a = 25℃ V_{CC}−33≦V_I≦V_{CC}, V_I = V_P	−33		33	μA
I_{CC}	Supply current	V_{CC}=5V, T_a=25℃ $P2_6$, $P2_7$: V_{CC}, Output pins open Input and I/O pins other than $P2_6$, $P2_7$: V_{SS}		3	6	mA

TIMING REQUIREMENTS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(RD-\phi)}$	Port R input setup time	330			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	0			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	0			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	0			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	0			ns
$t_{h(\phi-RD)}$	Port R input hold time	0			ns
t_c	External clock input cycle time	250			ns
t_w	External clock input pulse width	75			ns
t_r	External clock rising edge			25	ns
t_f	External clock falling edge			25	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	0			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	0			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	0			ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	0			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.18			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time	Fig.19			230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.18, Fig.19			230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig.19			200	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.18			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address and control signal delay time	Fig.19			250	ns
$t_{d(\phi-P1AF)}$	Port P1 address and control signal delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.18, Fig.19			200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				200	ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.18			250	ns
$t_{d(\phi-P1A)}$	Port P1 address and control signal delay time	Fig.19			250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.18, Fig.19			200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				200	ns

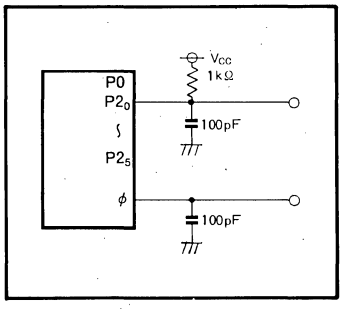


Fig.18 Port P0, $P2_0$~$P2_5$ test circuit

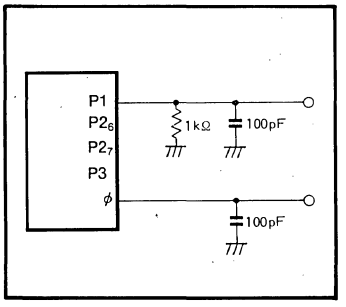
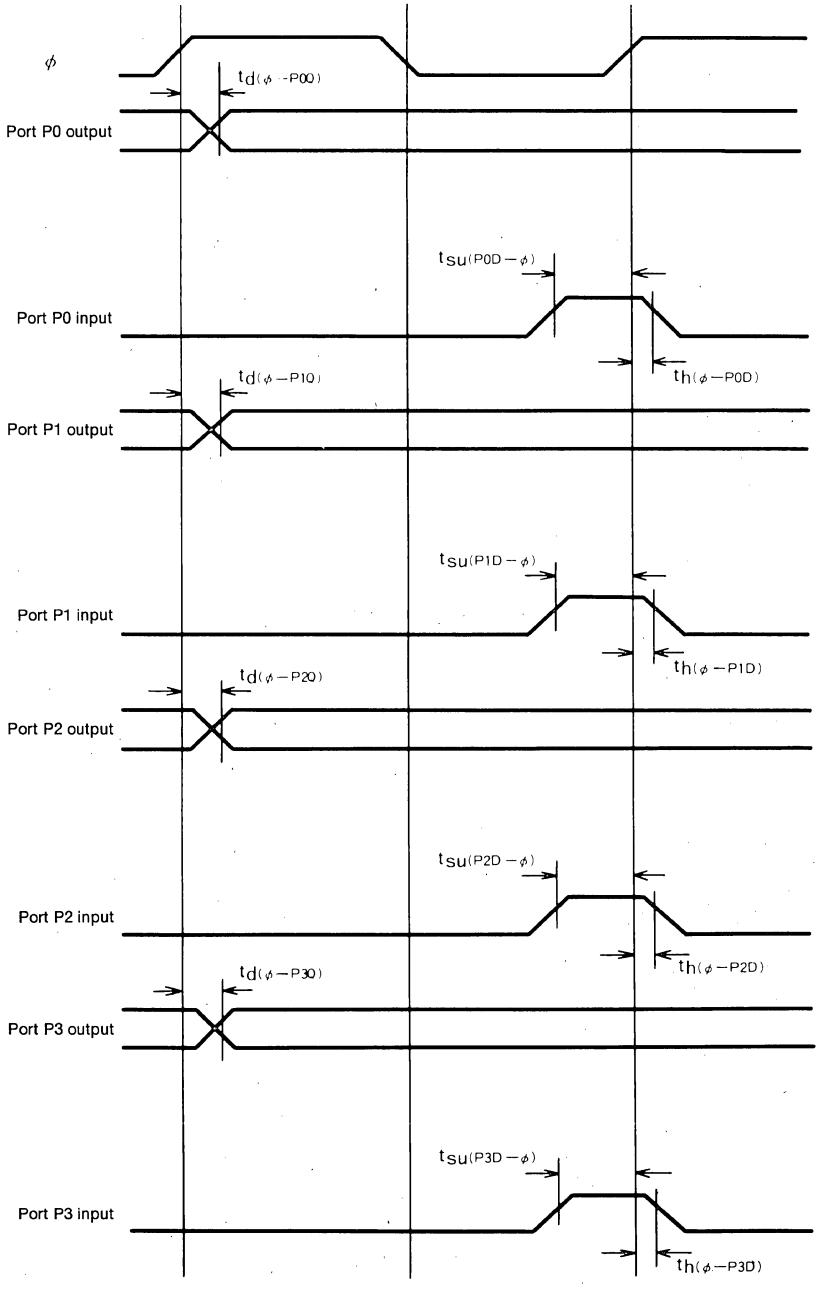


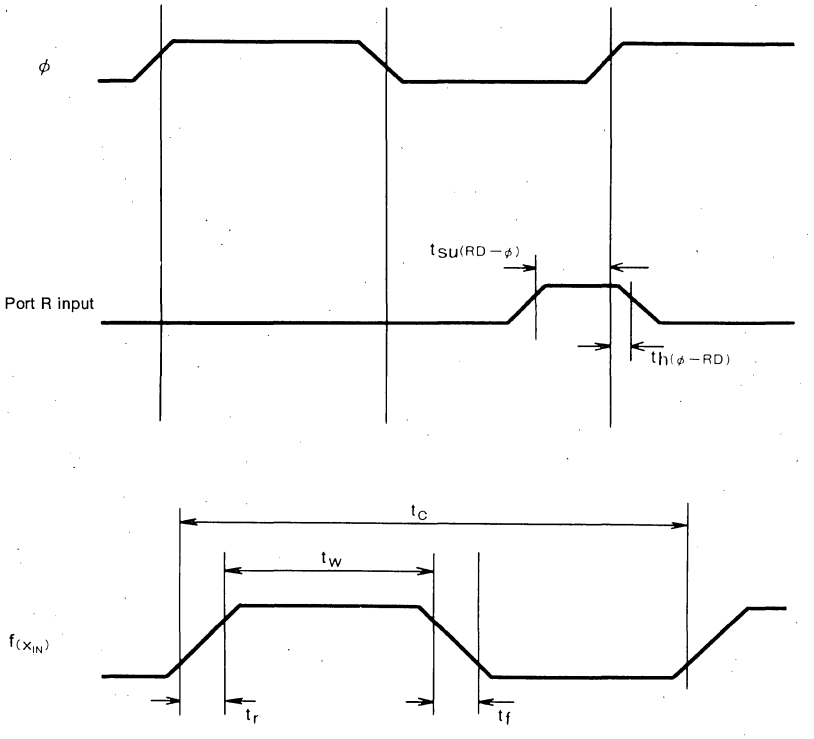
Fig.19 Port P1, $P2_6$, $P2_7$, P3 test circuit

TIMING DIAGRAMS

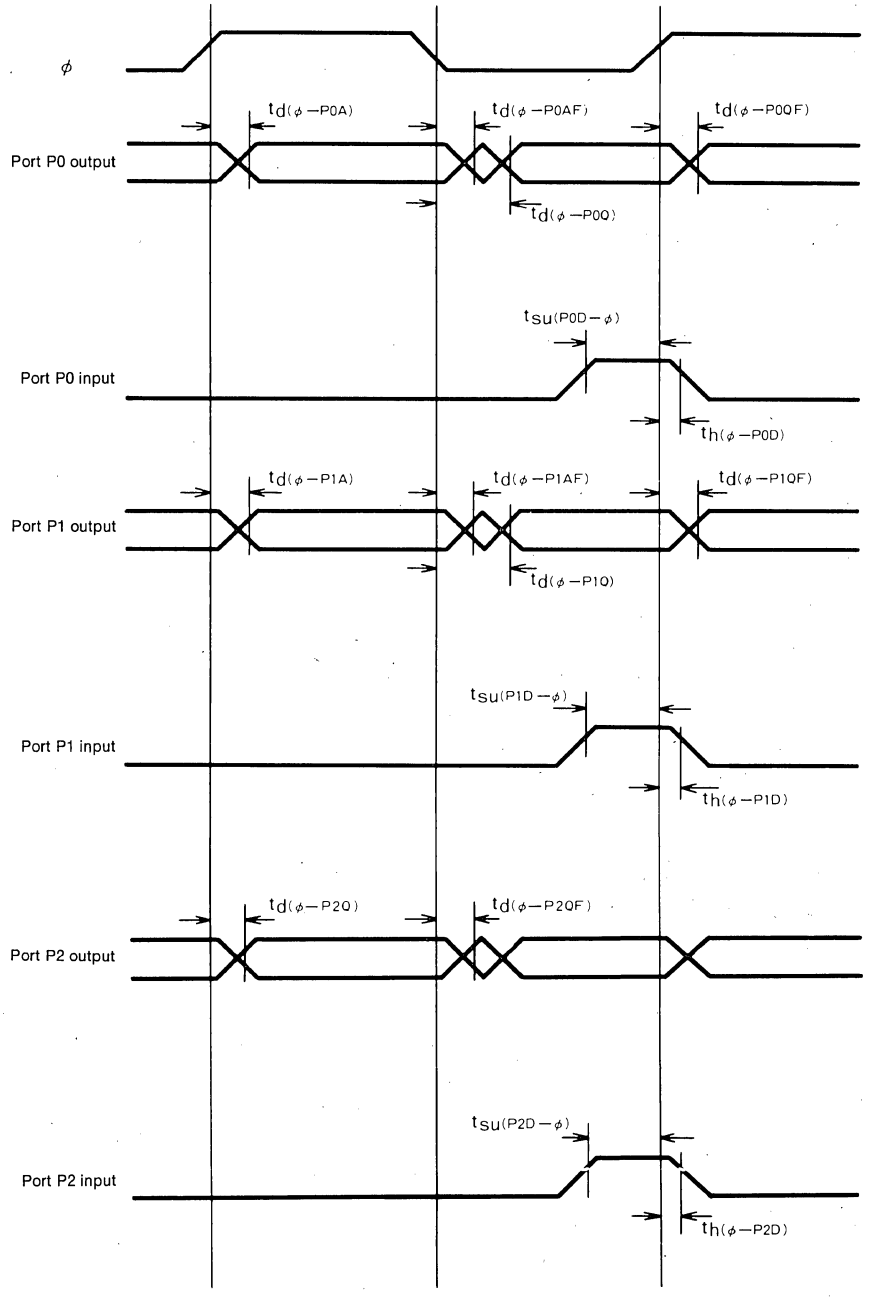
In single-chip mode



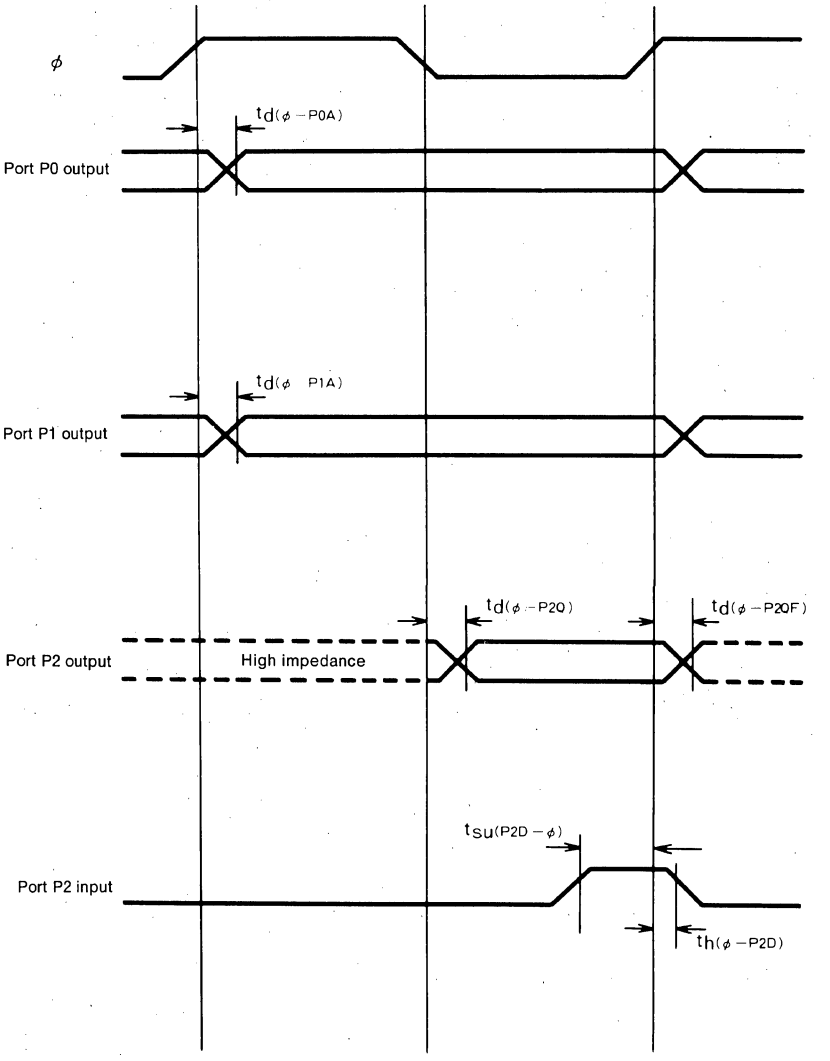
In single-chip mode (continued from the preceding page)



In memory expanding mode and eva-chip mode



In microprocessor mode



M50753-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50753-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP (flat package type also available). This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50753-XXXSP and the M50753-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

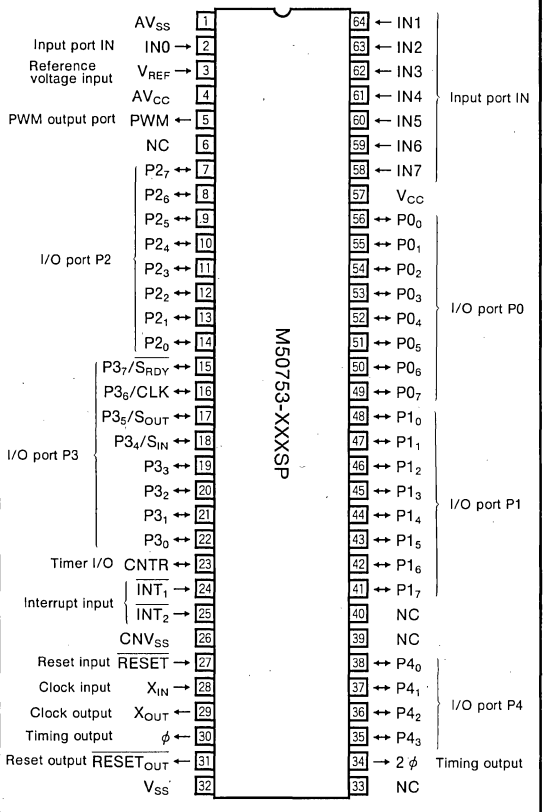
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 6144 bytes
  RAM ..... 192 bytes
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz ..... 5V$\pm$10%
- Power dissipation
  normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 8 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as A-D or serial I/O)
- Programmable I/O ports (Ports P0, P1, P2, P3, P4) 36
- Input ports (Port IN) 8
- Serial I/O (8-bit) 1
- A-D converter ..... 8-bit successive approximation
- PWM function 1

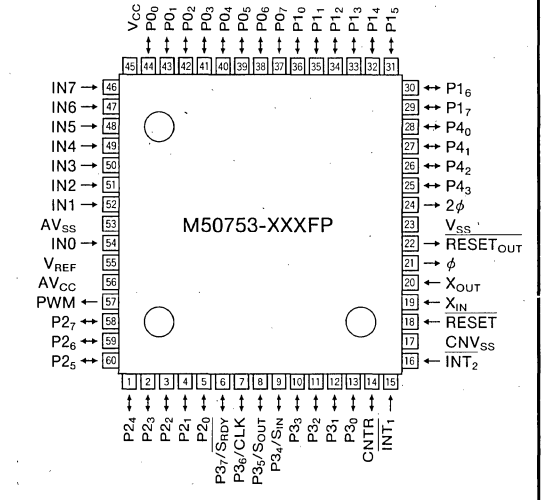
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



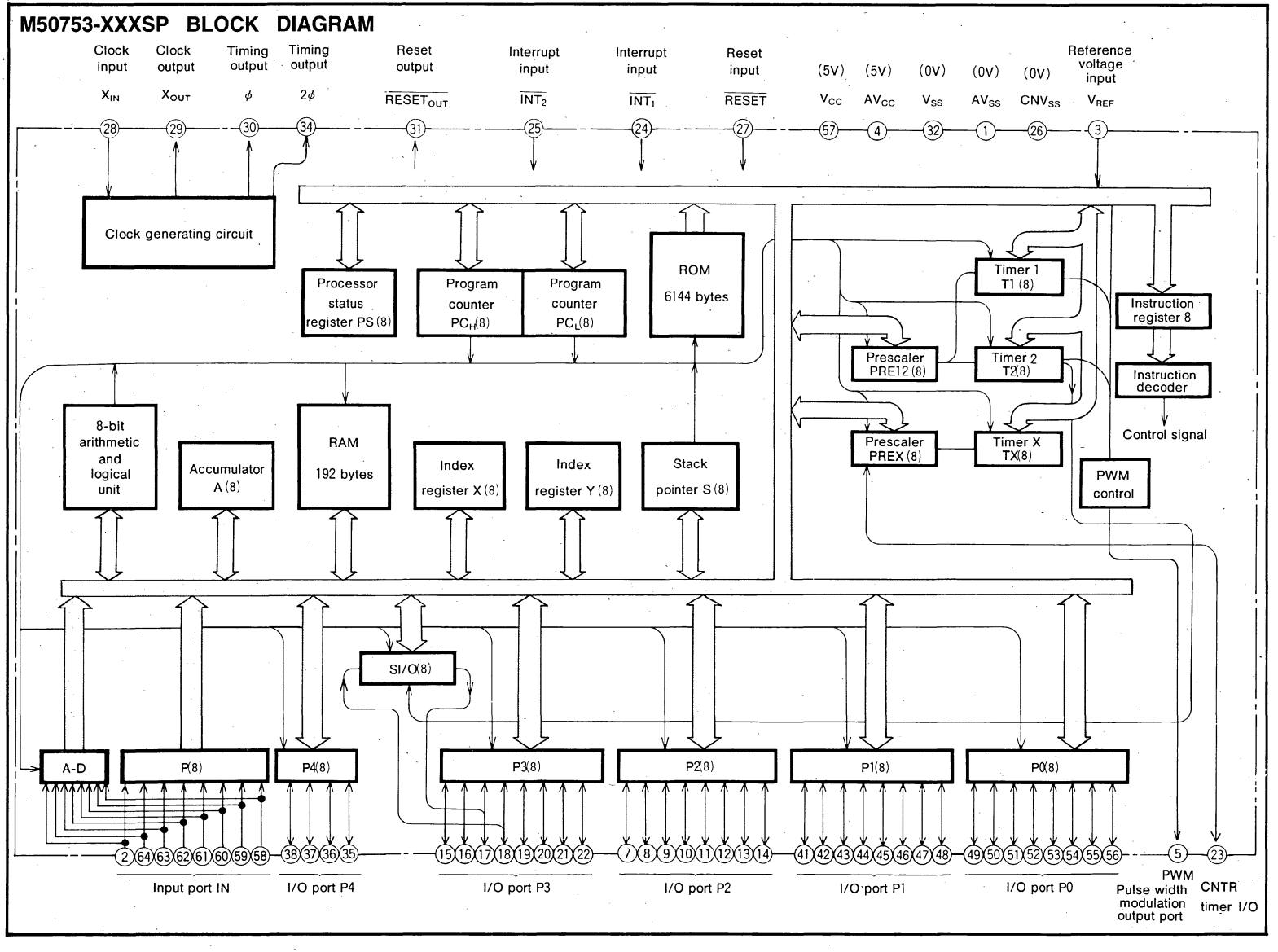
Outline 64P4B



Outline 60P6

NC : No connection

M50753-XXXSP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONS OF M50753-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory size	ROM		6144bytes
	RAM		192bytes
I/O port	$\overline{INT_1}$, $\overline{INT_2}$	Input	1-bit×2
	P0, P1, P2, P3, P4	I/O	4-bit×1
			8-bit×4 (Part of P3 are in common with serial I/O)
	IN	Input	8-bit×1 (Input and analog input for A-D)
	CNTR	I/O	1-bit×1
Serial I/O			8-bit×1
Timers			8-bit prescaler×2+8-bit timer×3 (2 when A-D convertion or serial I/O is used)
Subroutine nesting			96 levels (max)
Interrupts			two external interrupts three timer interrupts (2 of timer interrupts are in common with serial I/O and A-D)
Clock generating circuit			Built-in (Ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	At high-speed operation		15mW (at 4MHz frequency)
I/O characteristics	Input/output voltage		12V (Ports P0, P1, P2, P3, P4, $\overline{INT_1}$, $\overline{INT_2}$, CNTR)
	Output current		10mA (Ports P0, P1, P2, P3, P4)
Memory expansion			possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
A-D converter			eight analog inputs, 8-channel successive approximation
PWM function			One output
Package	M50753-XXXSP		64-pin shrink plastic molded DIP
	M50753-XXXFP		60-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ, 2ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an output pin for the timer X.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$\overline{INT_2}$	Interrupt input	Input	This is the lowest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
PWM	PWM output	Output	This is output pin from the pulse width modulator. The output structure is N-channel open drain.
$\overline{RESET_{OUT}}$	Reset output	Output	This pin outputs the reset signal for peripheral devices.
IN0~IN7	Analog input port IN	Input	This is an 8-bit analog input port for the A-D converter, and can be used as normal input port.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.
AV_{CC}	Voltage input for A-D		This is the power supply input pin for the A-D converter.
AV_{SS}	Voltage input for A-D		This is GND input pin for the A-D or D-A converter.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50753-XXXSP is shown in Figure 1. Addresses $E800_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 6144 bytes.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $00BF_{16}$ are assigned to the built-in RAM and consist of 192 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

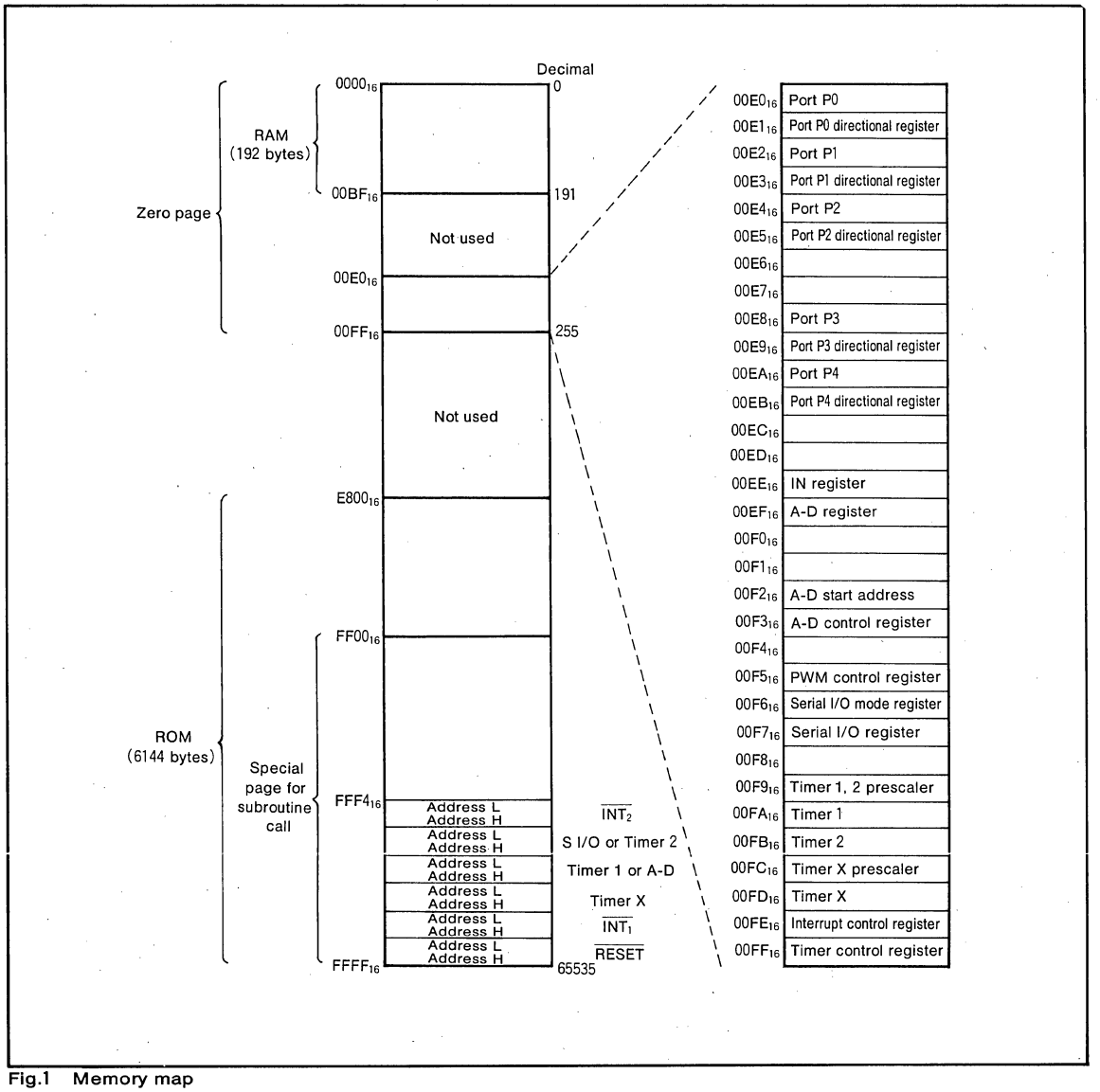


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

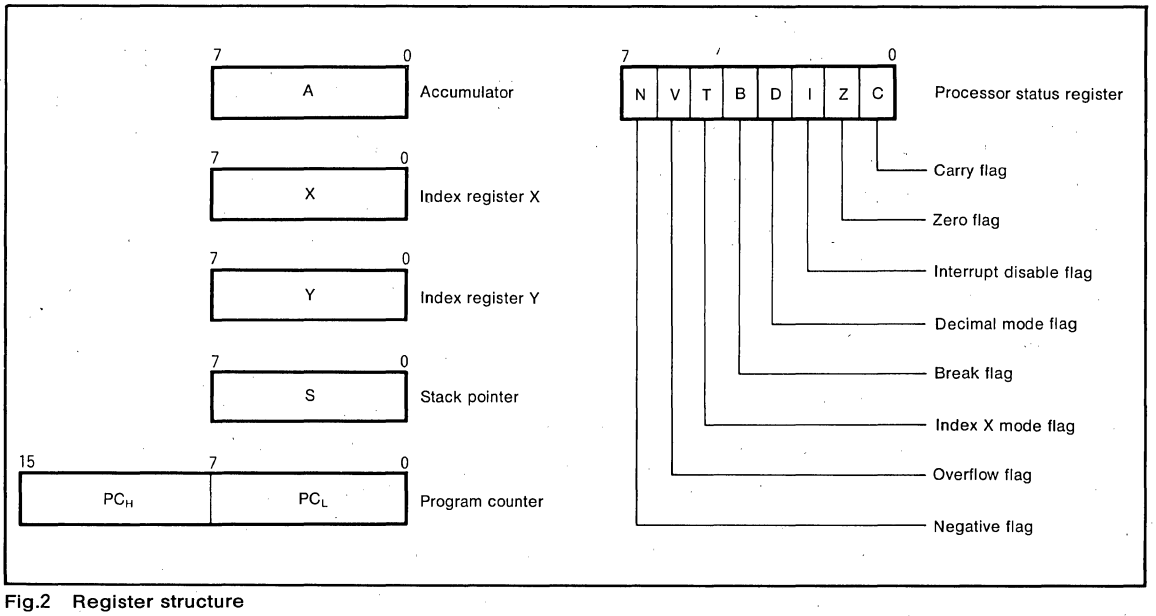


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The location of the stack can be determined by the stack page bit (bit 4 at address $00FF_{16}$). When bit 4 is "0" and the contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When bit 4 is "1", the stack address is set to $01XX_{16}$. When using this microcomputer in the single-chip mode, the stack page bit must be "0" and the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{\text{INT}_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1 or A-D	4	$FFF9_{16}$, $FFF8_{16}$
Timer 2 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{\text{INT}_2}$ (BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50753-XXXSP can be interrupted from eight sources; $\overline{\text{INT}_1}$, Timer X, Timer 1/A-D, Timer 2/Serial I/O, or the $\overline{\text{INT}_2}$/$\overline{\text{BRK}}$ instruction.

The value of bit 2 of the serial I/O register (address $00F6_{16}$) determines whether the interrupt is from timer 2 or from serial I/O. When bit 2 is "1" the interrupt is from serial I/O, and when bit 2 is "0" the interrupt is from timer 2. Also, when bit 2 is "1", parts of port 3 are used for serial I/O. Bit 3 of the A-D control (address $00F3_{16}$) register determines if an interrupt is from timer 1 or from the A-D. When bit 3 is "0", the interrupt is from timer 1, when bit 3 is "1" the interrupt is from the A-D. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as an interrupt.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt inhibit flag (I) is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupts are inhibited when the interrupt inhibit flag is set to "1". All of the other interrupts can further be controlled indi-

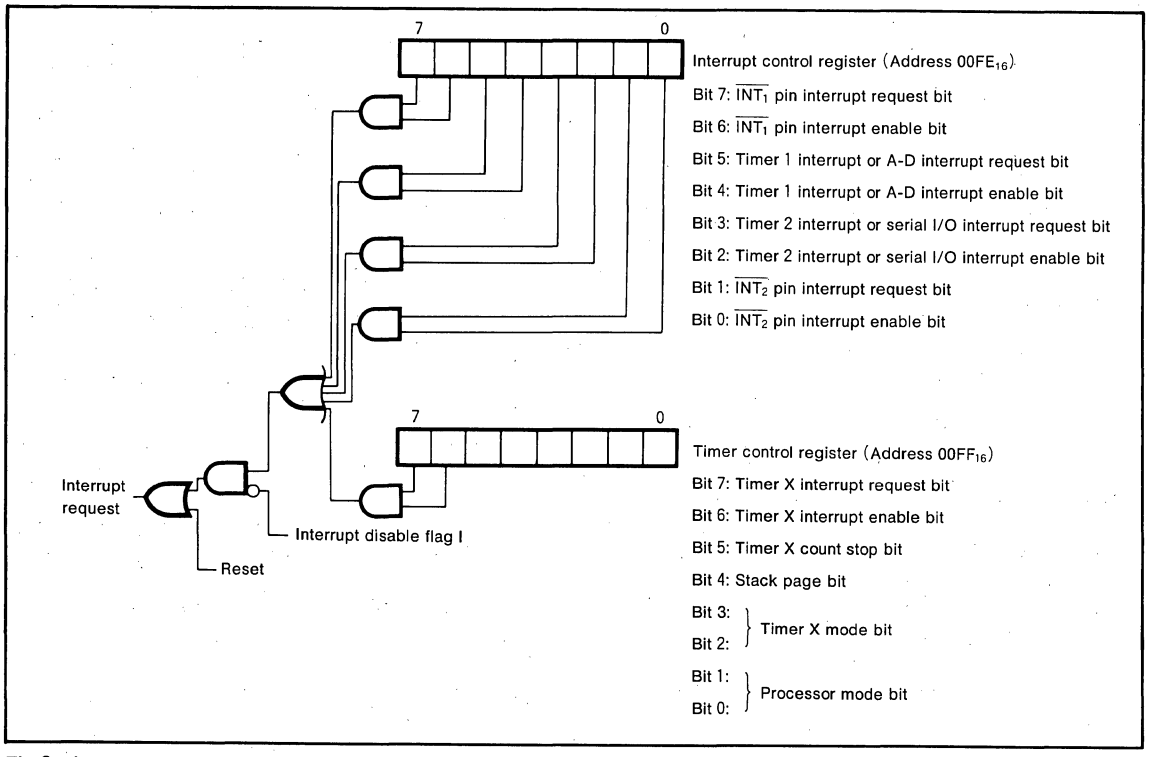


Fig.3 Interrupt control

MITSUBISHI ELECTRIC

vidually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt inhibit flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"
(2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"
(3) A-D conversion is finished.

These request bits can be reset by the program but can not be set.

Since the BRK instruction and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

TIMER

The M50753-XXXSP has three timers; timer X, timer 1, and timer 2. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section). Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1"; the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1 and timer 2 is shown in Figure 4.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as 1/n, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

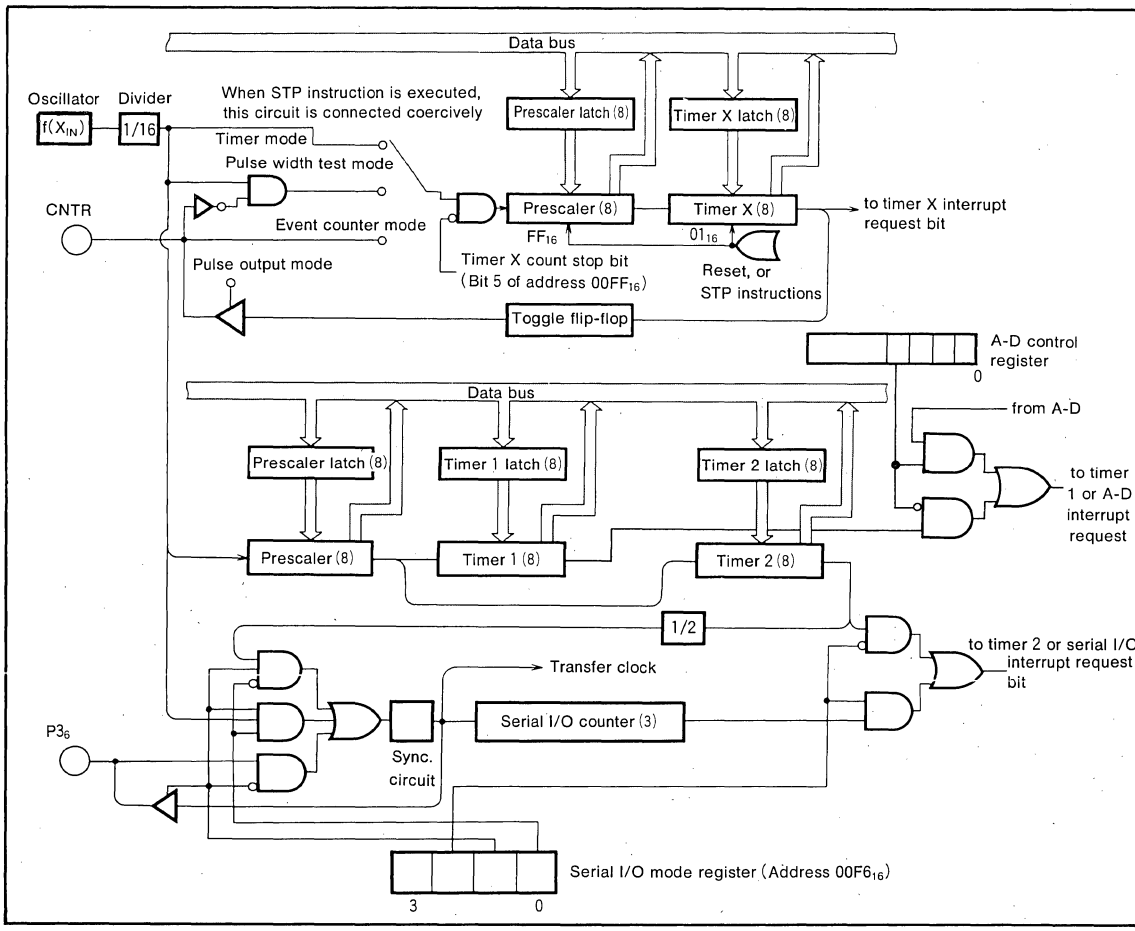


Fig.4 Block diagram of timer X, timer 1, and timer 2

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section). The prescaler latch and timer latch can be loaded with any number except zero and 1.

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock source.

(4) Pulse width measurement mode [11]
This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

When timer 1 or 2 is used, the bit 0 of PWM control register must be set to "0". For details, refer to the PWM section.

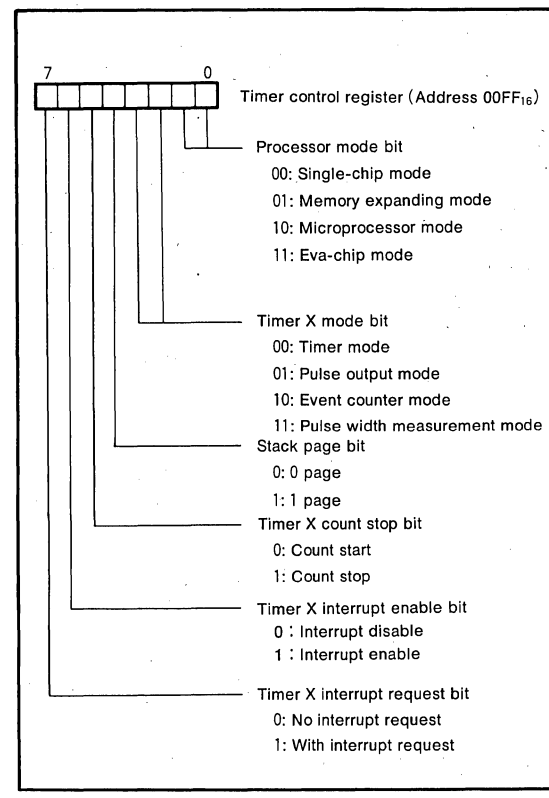


Fig.5 Structure of timer control register

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 6.

In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input /output clock (CLK), and the serial I/O pins (S_{OUT}, S_{IN}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F6_{16}$) is a 4-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 2, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the oscillator frequency divided by 16, becomes the clock.

Bit 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is a "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 2. Bit 3

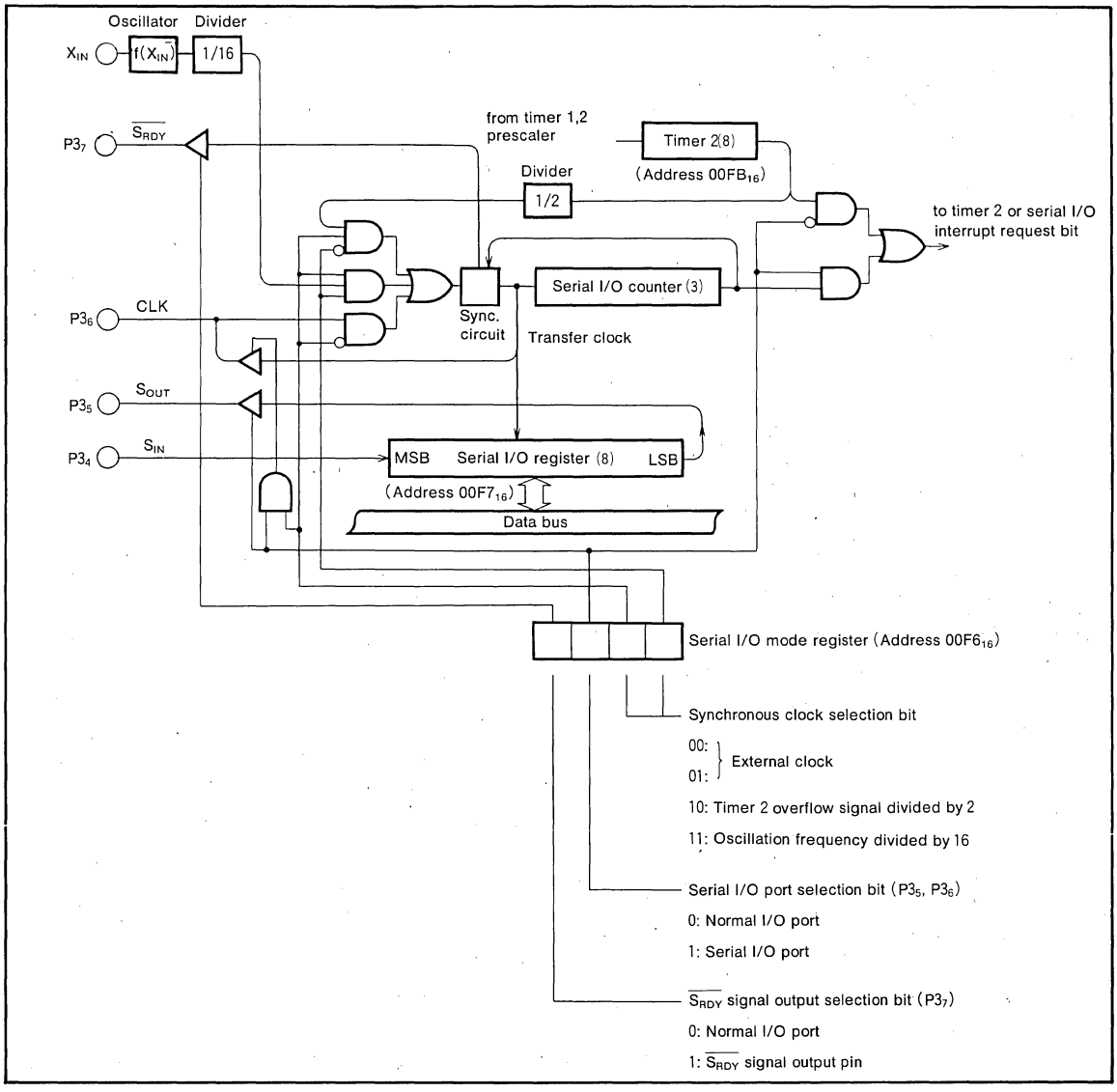


Fig.6 Block diagram of serial I/O

determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3=1, $\overline{S_{RDY}}$) or used as normal I/O pin (bit 3=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address $00F7_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50753-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrpt request bit will be set.

External Clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 7. An example of communication between two M50753-XXXSPs is shown in Figure 8.

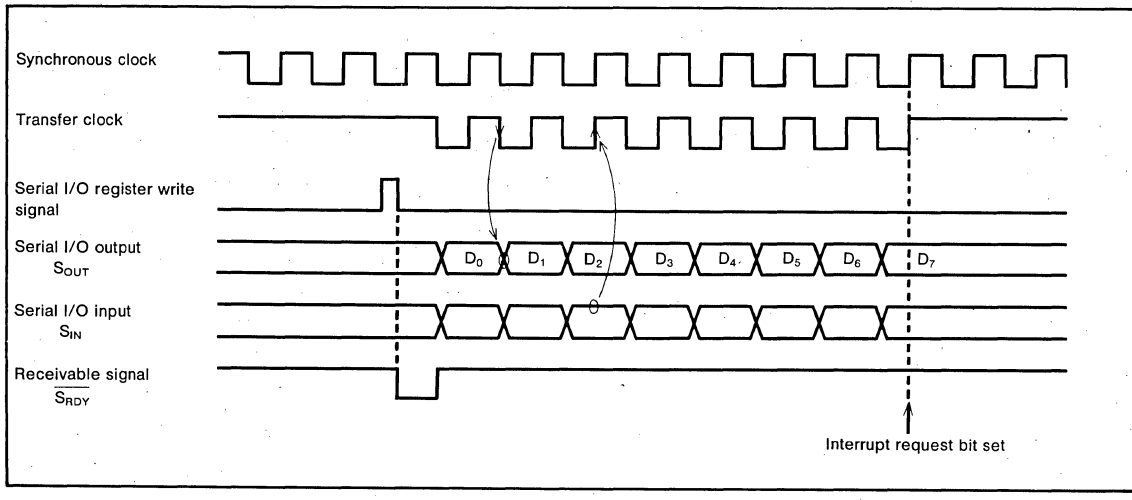


Fig.7 Serial I/O timing

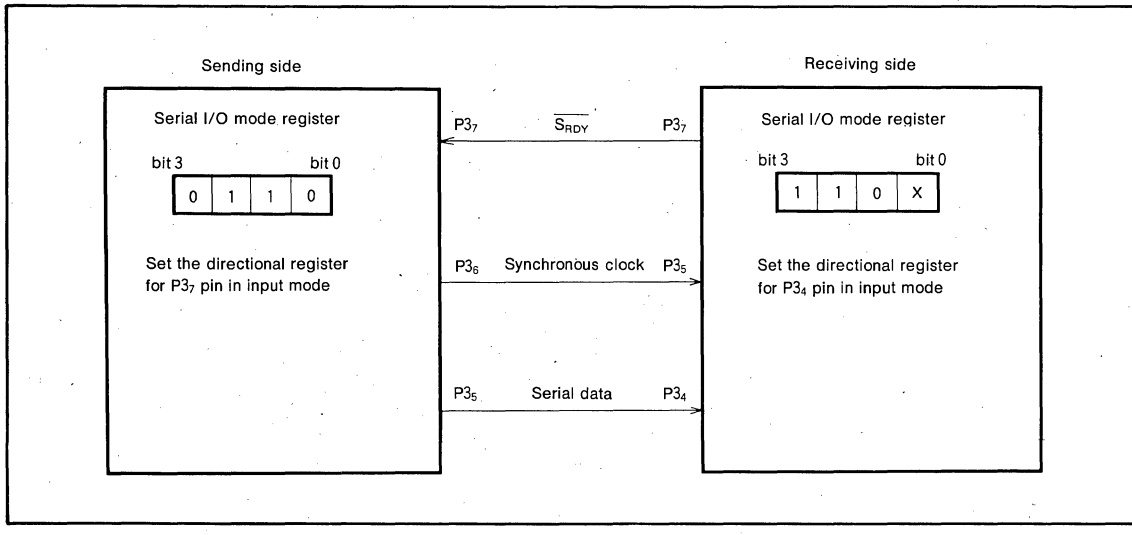


Fig.8 Example of serial I/O connection

A-D CONVERTER

The A-D converter circuit is shown in Figure 9. The analog input ports of the A-D converter (IN0~IN7) are in common with input ports of the data bus.

The 4-bit A-D control register is located at address $F3_{16}$. One of the eight analog inputs is selected by bits 0, 1 and 2 of this register. The correspondence of the analog input pins with bits 0~2 is shown in Figure 10. Bit 3 selects the interrupt source, either from timer 1 or the A-D itself. If bit 3 is "0", then the interrupt request is from timer 1, if it is a "1", then it is from the A-D.

A-D conversion is accomplished by first selecting the analog channel (bit 0, 1) to be converted. Bit 3 should also be set to "1" to select the A-D as the interrupt source. The conversion is started when dummy data is written into address $00F2_{16}$. When the conversion is finished, an interrupt is generated by the A-D and the digital data can be read from the A-D register (address $00EF_{16}$).

Port IN can also be used as an input port by reading data into address EE_{16}. However, this cannot be done during A-D conversions.

2	1	0	A-D control register (Address $00F3_{16}$)
0	0	0	····· IN0
0	0	1	····· IN1
0	1	0	····· IN2
0	1	1	····· IN3
1	0	0	····· IN4
1	0	1	····· IN5
1	1	0	····· IN6
1	1	1	····· IN7

Fig10 A-D control register bit 0, 1, 2 vs analog input

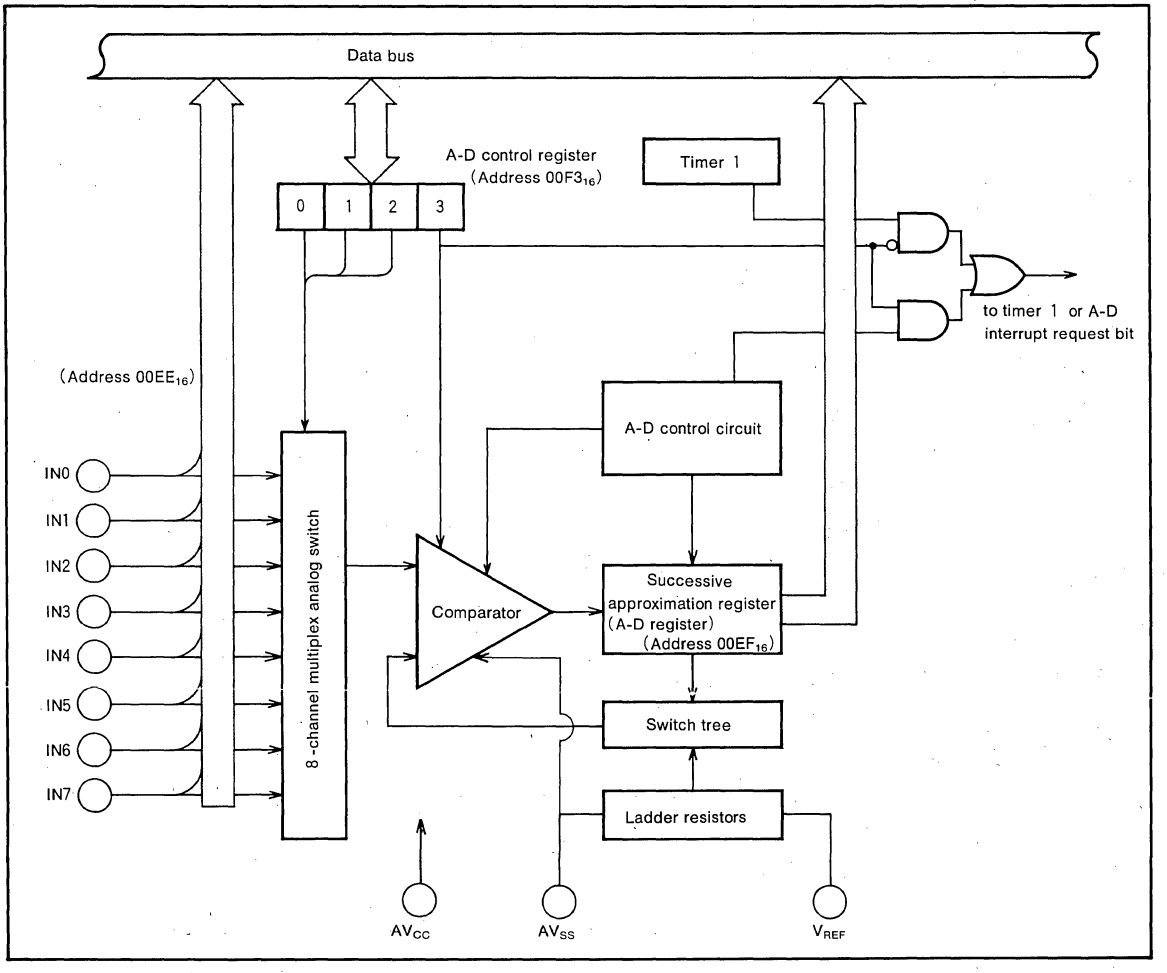


Fig.9 A-D converter circuit

PWM

The M50753-XXXSP has a pulse width modulated (PWM) output control circuit. The circuit outputs a variable duty cycle signal that can be used for a programmable pulse width and frequency. Timers 1 and 2 are used for the PWM. The block diagram of the PWM is shown in Figure 11.

The PWM is composed of N-channel open drain transistors. When bit 0 of the PWM control register is "0", the output transistors are turned off. When timers 1 and 2 are not used for PWM control, they operate in the normal timer modes.

When bit 0 of the PWM control register is "1", a rectangular wave is output according to the value set in timer 1 and 2. The clock source frequency for the PWM is the oscillator frequency divided by 16.

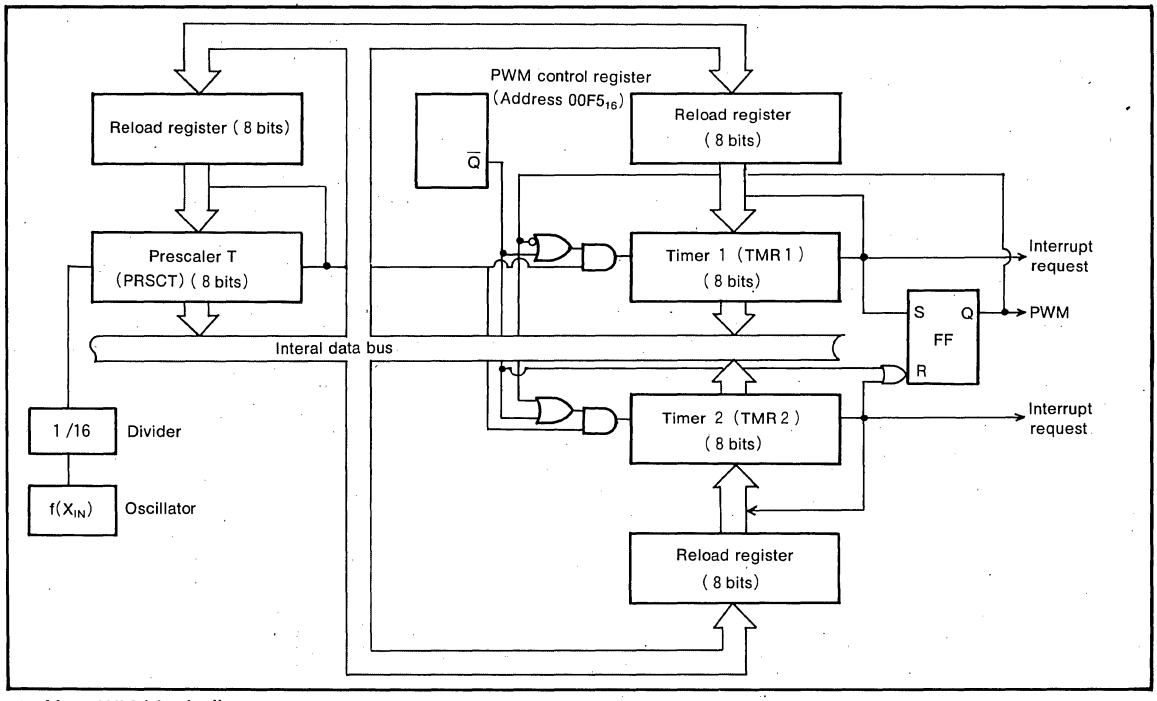


Fig.11 PWM block diagram

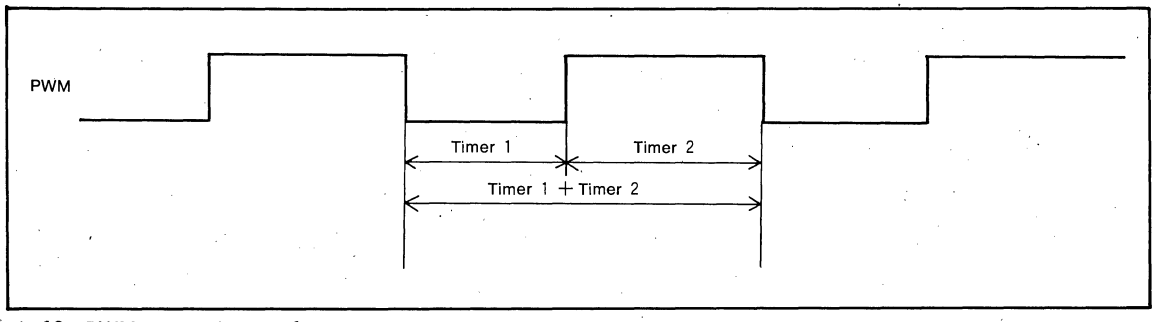


Fig.12 PWM rectangle waveform

RESET CIRCUIT

The M50753-XXXSP is reset according to the sequence shown in Figure 15. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 14.

An example of the reset circuit is shown in Figure 13.
When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

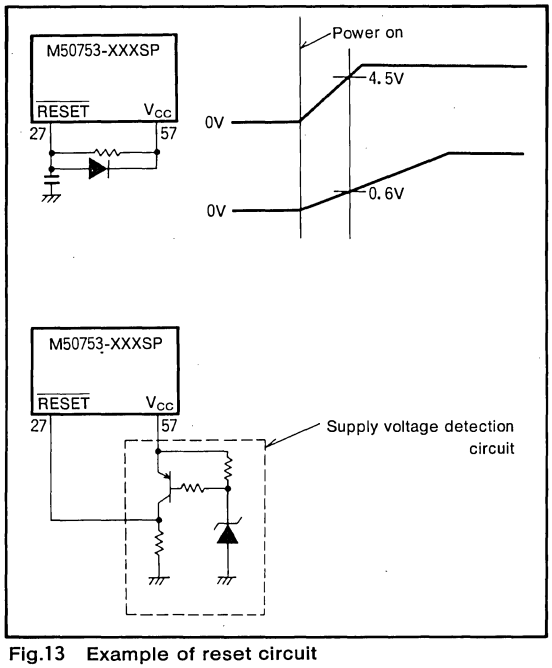


Fig.13 Example of reset circuit

			Address
(1)	Port P0 directional register	($E1_{16}$) ···	00_{16}
(2)	Port P1 directional register	($E3_{16}$) ···	00_{16}
(3)	Port P2 directional register	($E5_{16}$) ···	00_{16}
(4)	Port P3 directional register	($E9_{16}$) ···	00_{16}
(5)	Port P4 directional register	(EB_{16}) ···	00_{16}
(6)	Serial I/O mode register	($F6_{16}$) ···	0 0 0 0
(7)	Prescaler X	(FC_{16}) ···	FF_{16}
(8)	Timer X	(FD_{16}) ···	01_{16}
(9)	Interrupt control register	(FE_{16}) ···	00_{16}
(10)	Timer control register	(FF_{16}) ···	00_{16}
(11)	Interrupt disable flag on processor status register	(PS) ···	1
(12)	Program counter	(PC_H) ···	Contents of address $FFFF_{16}$
		(PC_L) ···	Contents of address $FFFE_{16}$
(13)	A-D control register	($F3_{16}$) ···	0 0 0 0
(14)	PWM control register	($F5_{16}$) ···	0

Fig.14 Internal state of microcomputer at reset

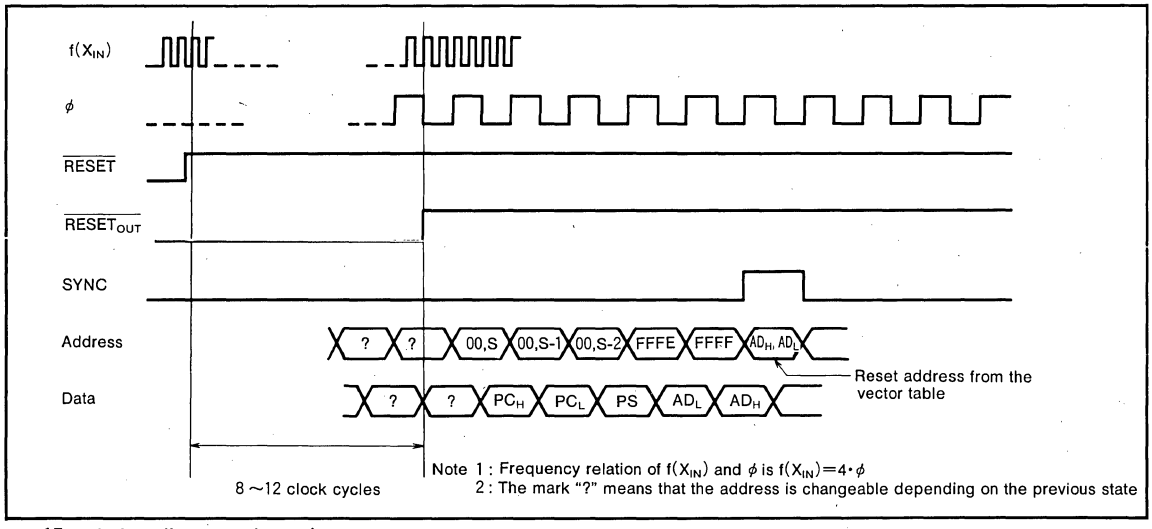


Fig.15 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

Pull-up transistor can be specified as an option. As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as serial I/O pins. For more details, see the processor mode information.

(5) Port P4

Port P4 is an 4-bit I/O port with N-channel open drain outputs. This port also has the pull-up transistor option.

(6) Clock 2 ϕ output pin

In normal conditions, the oscillator frequency divided by two is output as 2 ϕ.

(7) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ.

(8) $\overline{\text{RESET}_{\text{OUT}}}$ pin

When the $\overline{\text{RESET}}$ pin goes to level "L", the $\overline{\text{RESET}_{\text{OUT}}}$ pin also goes to "L". On the other hand, when the $\overline{\text{RESET}}$ pin goes to level "H", the $\overline{\text{RESET}_{\text{OUT}}}$ pin also goes to "H" after 8 clock cycles. This output is used to reset the external circuits.

(9) $\overline{\text{INT}_1}$ pin

The $\overline{\text{INT}_1}$ pin is an interrupt input pin. The $\overline{\text{INT}_1}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

(10) $\overline{\text{INT}_2}$ pin

The $\overline{\text{INT}_2}$ pin is an interrupt input pin. When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1".

(11) CNTR pin

The CNTR pin is an I/O pin of timer X. In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

(12) Port IN

Port IN is an 8-bit input port to the A-D converter. The input contents of the port can be read to as the contents of address $00EE_{16}$. The read operation is inhibited during A-D conversion.

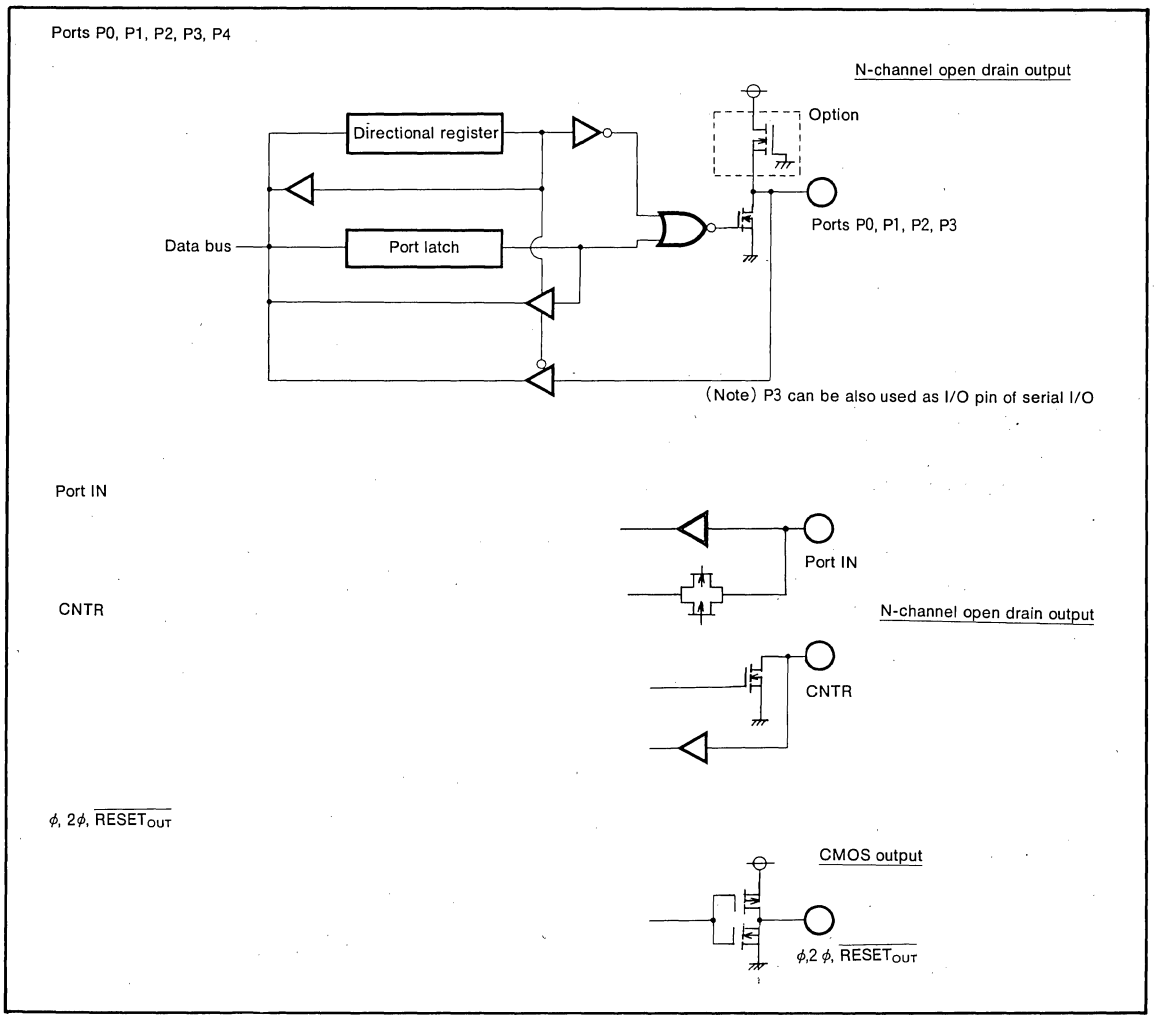


Fig.16 Block diagram of ports P0~P5 (single-chip mode), and output and input formats CNTR, ϕ, $\overline{\text{RESET}_{\text{OUT}}}$, 2 ϕ, and port IN

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0 ~ P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 14 shows the functions of ports P0~P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 17.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

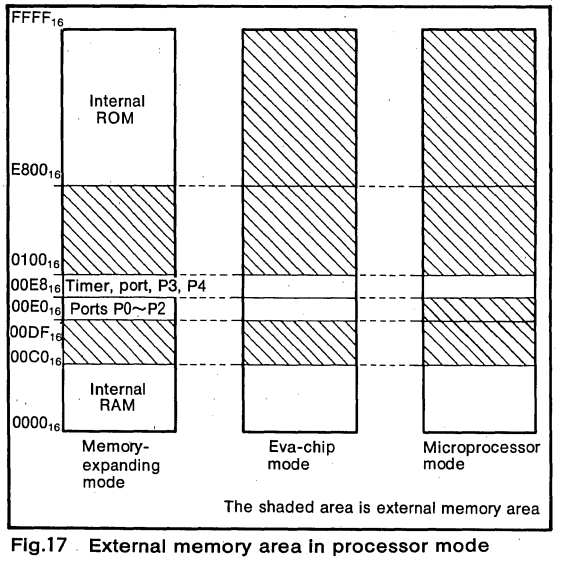


Fig.17 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0 ~ P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of $D_7 \sim D_0$ (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state, and $\overline{RDY}$ signal is input form $P3_2$ pin. When in the "L" state, $P3_2$, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The $\overline{RDY}$ is ready signal input and, when it goes to "L", internal clock stops and the CPU waits the data. However, the oscillation does not stop.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode.

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the data bus ($D_7 \sim D_0$) and loses its normal I/O functions. Port $P3_2$, $P3_1$, and $P3_0$ become the $\overline{RDY}$, SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is required.

This mode has almost the same function as the memory expanding mode except that it needs to attach all program memories to the outside. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

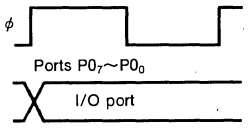
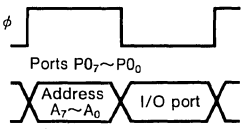
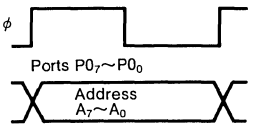
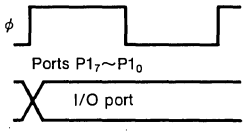
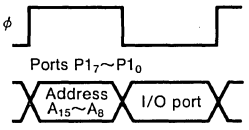
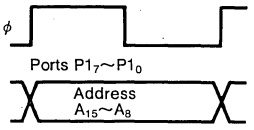
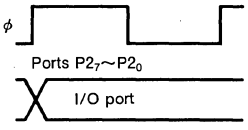
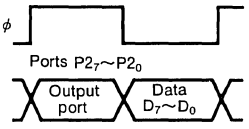
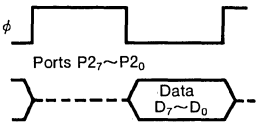
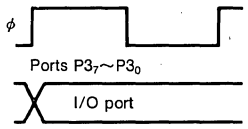
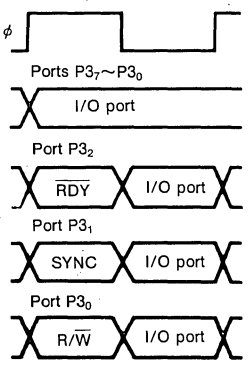
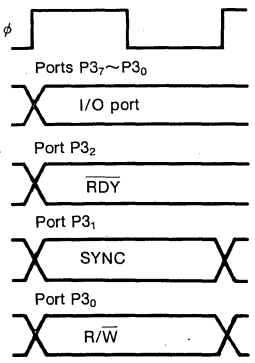
Port \ Mode	CM_1 = 0, CM_0 = 0 Single-chip mode	CM_1 = 0, CM_0 = 1 Memory expanding mode	CM_1 = 1, CM_0 = 1 Eva-chip mode	CM_1 = 1, CM_0 = 0 Microprocessor mode
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	
Port P3			Same as left	

Fig.18 Processor mode and functions of ports P0~P3

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the rese. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 21.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleared when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 19.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock uasge is shown in Figure 20. X_{IN} is the input, and X_{OUT} is open.

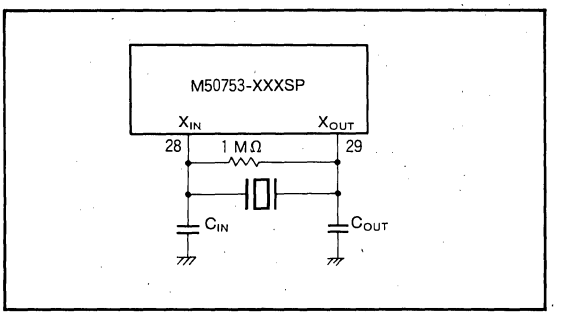


Fig.19 External ceramic reasonator circuit

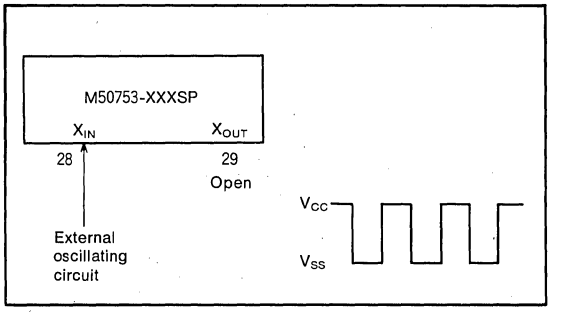


Fig.20 External clock input circuit

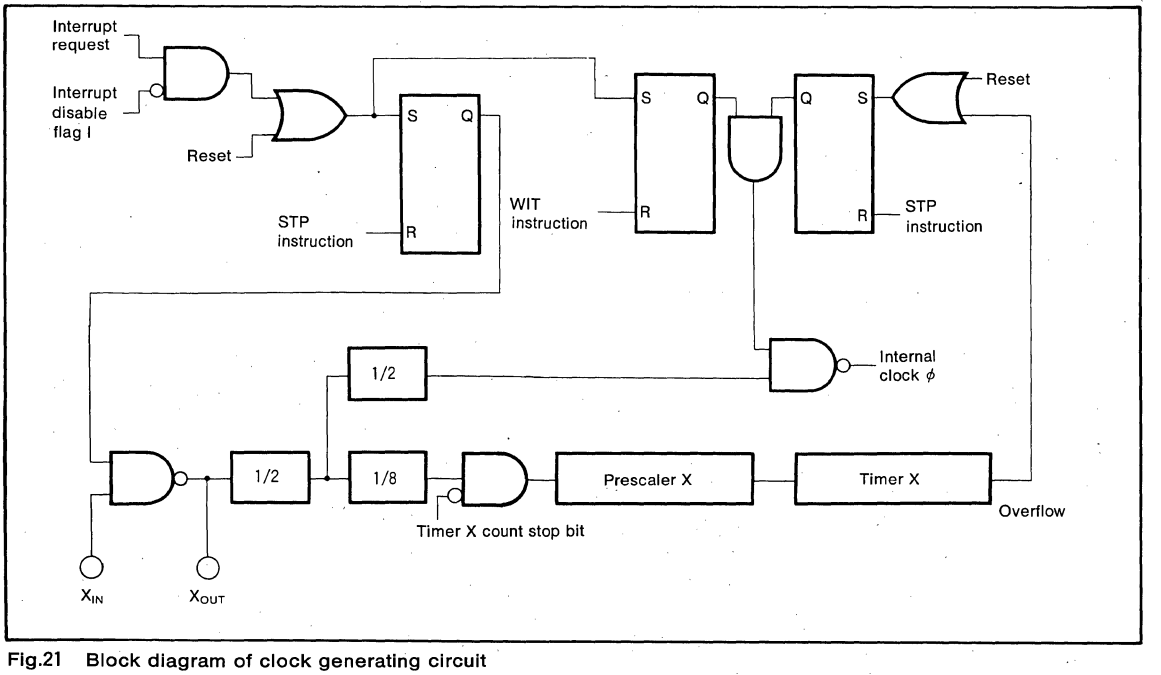


Fig.21 Block diagram of clock generating circuit

MITSUBISHI ELECTRIC

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/n.
(2) Set a value other than "2" for the timer and the prescaler.
(3) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(4) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
(5) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(6) A NOP instruction must be used after the execution of a PLP instruction.
(7) Notes on serial I/O
① Set "0" in the serial I/O interrupt enable bit (bit 2 of address $00FE_{16}$) before setting the serial I/O mode.
② Insert at least one instruction and set "0" in the serial I/O interrupt request bit (bit 3 of address $00FE_{16}$) after setting the serial I/O mode.
③ Set "1" in the serial I/O interrupt enable bit after the operation described in ②.
(8) The timer X and prescaler X must be set "FF_{16}" immediately before the execution of a STP instruction.
(9) Notes on A-D conversion
① Set "0" in the A-D interrupt enable bit (bit 4 of address $00FE_{16}$) before setting A-D conversion.
② Insert at least one instruction and set "0" in the A-D interrupt request bit (bit 5 of address $00FE_{16}$) after setting the A-D conversion.
③ Set "1" in the A-D interrupt enable bit after the operation described in ②.
④ Set "0" in bit 3 of the A-D control register (address $00F3_{16}$) before using a STP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ..... EPROM 3sets
Write the following option on the mask ROM confirmation form
- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port P4 pull-up transistor bit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	with respect to V_{SS} Output transistors are at "off" state	−0.3~7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3~7	V
V_I	Input voltage IN0~IN7		−0.3~V_{CC}+0.3	V
V_I	Input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}		−0.3~13	V
V_O	Output voltage 2 ϕ, X_{OUT}, ϕ, $\overline{RESET_{OUT}}$		−0.3~V_{CC}+0.3	V
V_O	Output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, CNTR, PWM		−0.3~13	V
Pd	Power dissipation	T_a=25℃	1000(Note 1)	mW
T_{opr}	Operating temperature		−10~70	℃
T_{stg}	Storage temperature		−40~125	℃

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, IN0~IN7, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, IN0~IN7, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

Note 2 : "H" input voltage of ports P0, P1, P2, P3, P4, CNTR, $\overline{INT_1}$, and $\overline{INT_2}$ is available up to +12V.
(However, these ports are without pull-up transistor)

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage ϕ, $\overline{RESET_{OUT}}$, 2ϕ	I_{OH}=−2.5mA	3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, CNTR, $P4_0$~$P4_3$, PWM	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage ϕ, $\overline{RESET_{OUT}}$, 2ϕ	I_{OL}=5mA			2	V
$V_{T+}-V_{T-}$	Hysterisis $P3_6$	when used as CLK input	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis CNTR, $\overline{INT_1}$, $\overline{INT_2}$		0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, PWM	V_I=0V without pull-up tranpistor			−5	μA
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, PWM	V_I=0V with pull-up transistor	−40	−70	−125	μA
I_{IL}	"L" input current IN0~IN7	V_I=0V			−5	μA
I_{IL}	"L" input current CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	V_I=0V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, PWM	V_I=12V without pull-up transistor			12	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, PWM	V_I=5V with pull-up transistor			5	μA
I_{IH}	"H" input current IN0~IN7	V_I=5V (when A-D not selection)			5	μA
I_{IH}	"H" input current CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	V_I=5V			5	μA
I_{IH}	"H" input current V_{REF}	V_I=5V			5	mA
I_{CC}	Supply current	output pins are open, input and I/O pins are connected to V_{SS}		3	6	mA
I_{ACC}	Supply current for A-D	during A-D conversion		2	4	mA

A-D CONVERTER CHARACTERISTICS (V_{CC}=AV_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=V_{REF}=5.12V			±3	LSB
R_{LADDER}	Ladder resistance value		1			kΩ
t_{CONV}	Conversion time				72	μs
V_{REF}	Reference input voltage				V_{CC}	V
V_{IA}	Analog input voltage				V_{REF}	V

TIMING REQUIREMENTS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	270			ns
$t_{su(IND-\phi)}$	Port IN input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-IND)}$	Port IN input hold time	20			ns
t_C	External clock input cycle time	250			ns
t_W	External clock input pulse width	75			ns
t_r	External clock rising edge			25	ns
t_f	External clock falling edge			25	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(RDY-\phi)}$	$\overline{RDY}$ input setup time	150			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-RDY)}$	$\overline{RDY}$ input hold time	500			ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(RDY-\phi)}$	$\overline{RDY}$ input setup time	150			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-RDY)}$	$\overline{RDY}$ input hold time	500			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.22			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				230	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.22			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns

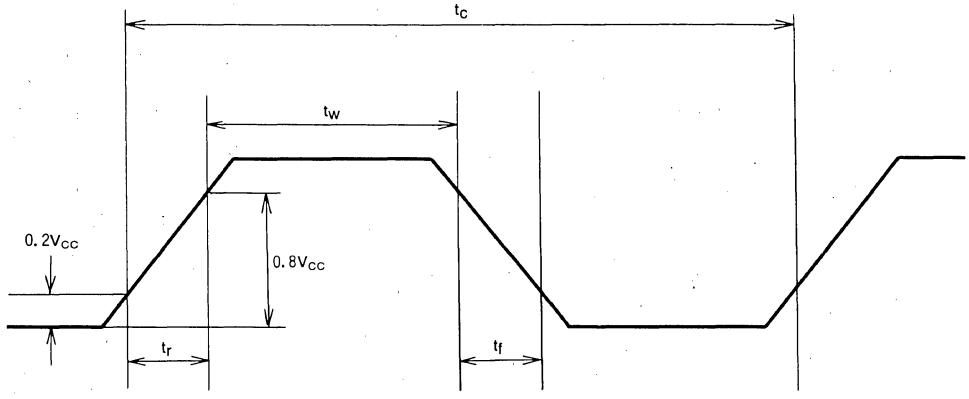
Microprocessor mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.22			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

2ϕ PIN AC CHARACTERISTICS (V_{CC}=5.0V, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_C	Clock output cycle time	Fig.23		500		ns
t_W	Clock output pulse width		150			ns
t_r	Clock rising time				75	ns
t_f	Clock falling time				50	ns

Timing diagram of 2ϕ



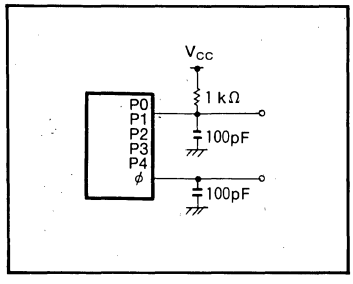


Fig.22 Ports P0～P4 test circuit

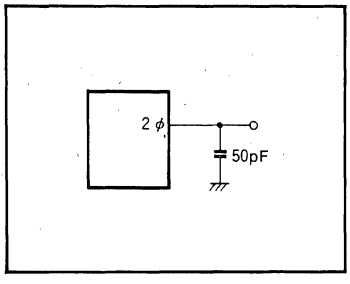
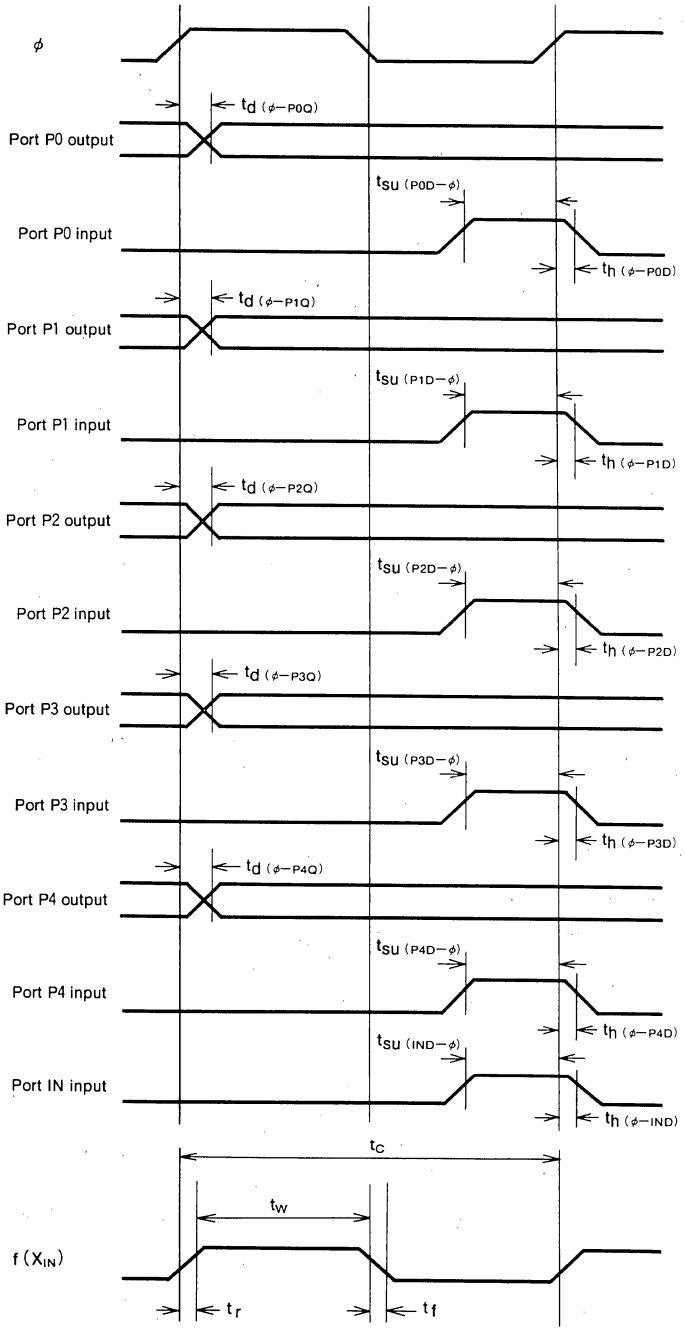


Fig.23 2ϕ test circuit

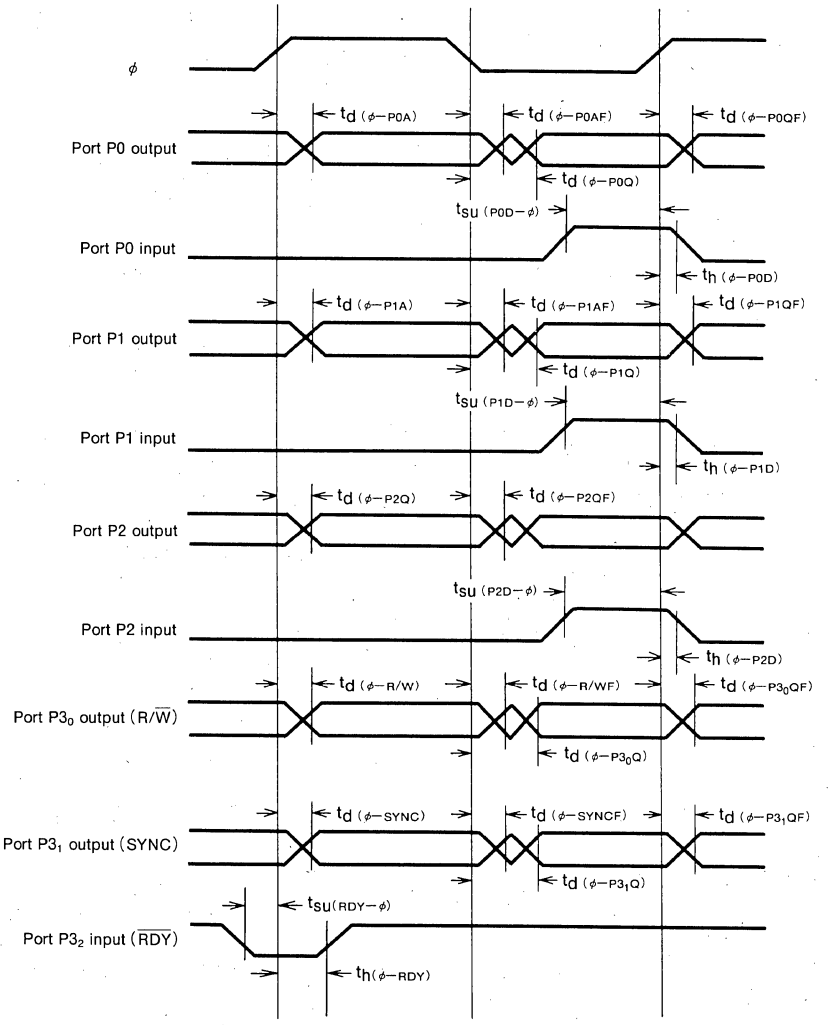
MITSUBISHI ELECTRIC

TIMING DIAGRAMS

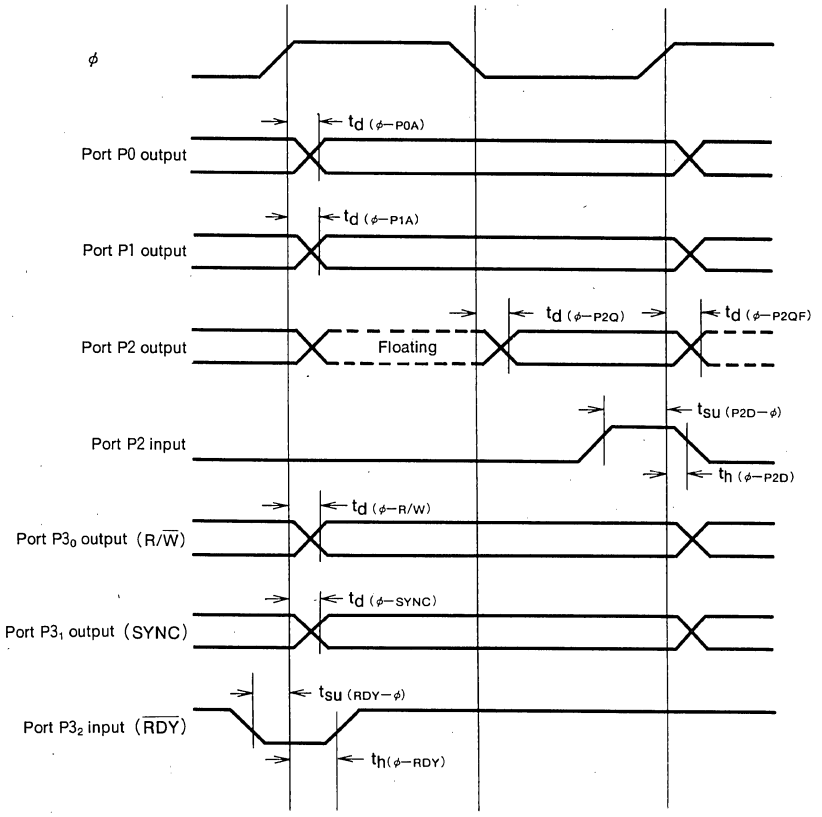
In single-chip mode



In memory expanding and eva-chip mode



In microprocessor mode



M50754-XXXSP/FP/GP, M50954-XXXSP/FP/GP, M50955-XXXSP/FP/GP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50754-XXXSP, M50954-XXXSP and the M50955-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 64-pin shrink plastic molded DIP (flat package type also available). These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences among the M50754-XXXSP, M50954-XXXSP and the M50955-XXXSP are noted below. The following explanations apply to the M50754-XXXSP. Specification variations for other chips are noted accordingly.

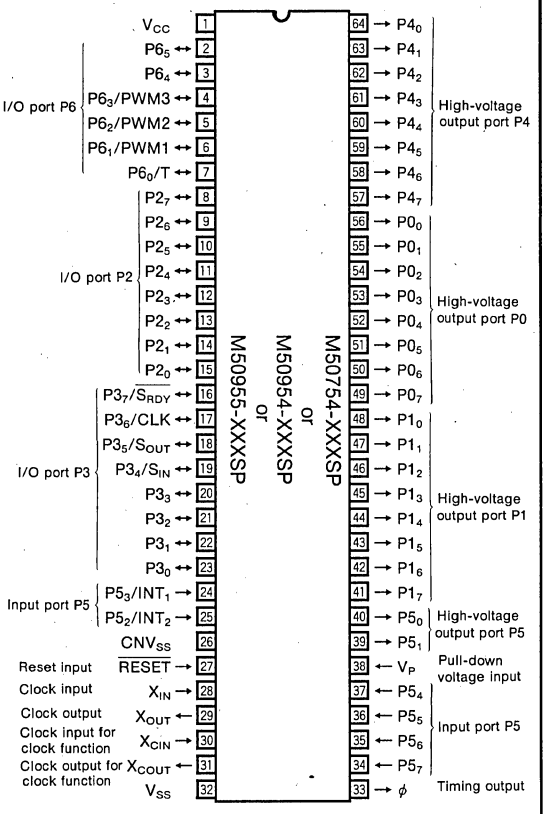
Type name	ROM size	RAM size
M50754-XXXSP	6144bytes	160bytes
M50954-XXXSP	8192bytes	192bytes
M50955-XXXSP	10240bytes	192bytes

The differences between the M50754-XXXSP and the M50754-XXXFP are the package outline and power dissipation ability (absolute maximum ratings). And the differences between the M50754-XXXFP and the M50754-XXXGP are only the package outline.

DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM .....6144 bytes (M50754-XXXSP)
  8192 bytes (M50954-XXXSP)
  10240 bytes (M50955-XXXSP)
  RAM ..... 160 bytes (M50754-XXXSP)
  192 bytes (M50954-XXXSP, M50955-XXXSP)
- Instruction execution time
  1.9μs (minimum instructions, at 4.2MHz frequency)
- Single power supply 4.0~5.5V(at f(X_{IN})=4.2MHz)
  3.0~5.5V(below f(X_{IN})=1.0MHz)
- Power dissipation
  normal operation mode, at 4MHz frequency 15mW
  low speed operation mode,
  at 32kHz frequency for clock function 0.3mW
- Subroutine nesting ... 80 levels (max.) (M50754-XXXSP)
  96 levels (max.) (M50954-XXXSP, M50955-XXXSP)
- Interrupt ..... 7 types, 5 vecters
- 8-bit timer ..... 3 (2 when used as serial I/O)
- Programmable I/O (Ports P2, P3, P6) 22
- Input ports (Port $P5_2$~$P5_7$) 6
- High-voltage output ports
  (Ports P0, P1, P4, $P5_0$, $P5_1$) 26
- Serial I/O (8-bit) 1
- PWM function ..... 14-bit×1
  6-bit×2

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

- Two clock generator circuits (One is for main clock, the other is for clock function)
- Generating function for clock input of EAROM

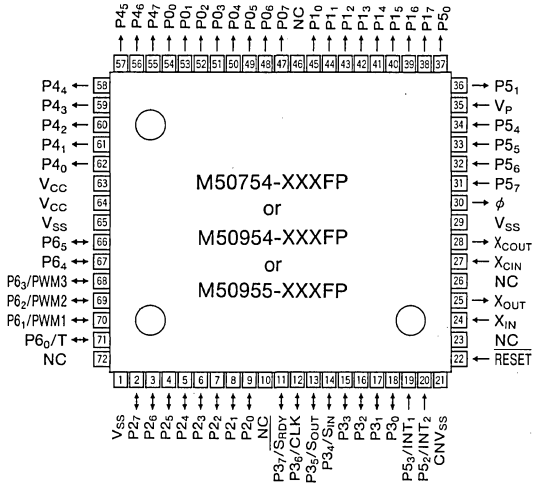
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

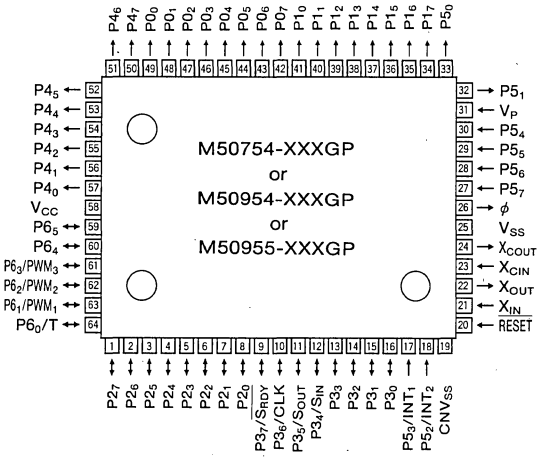
M50754-XXXSP/FP/GP, M50954-XXXSP/FP/GP, M50955-XXXSP/FP/GP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN CONFIGURATION (TOP VIEW)



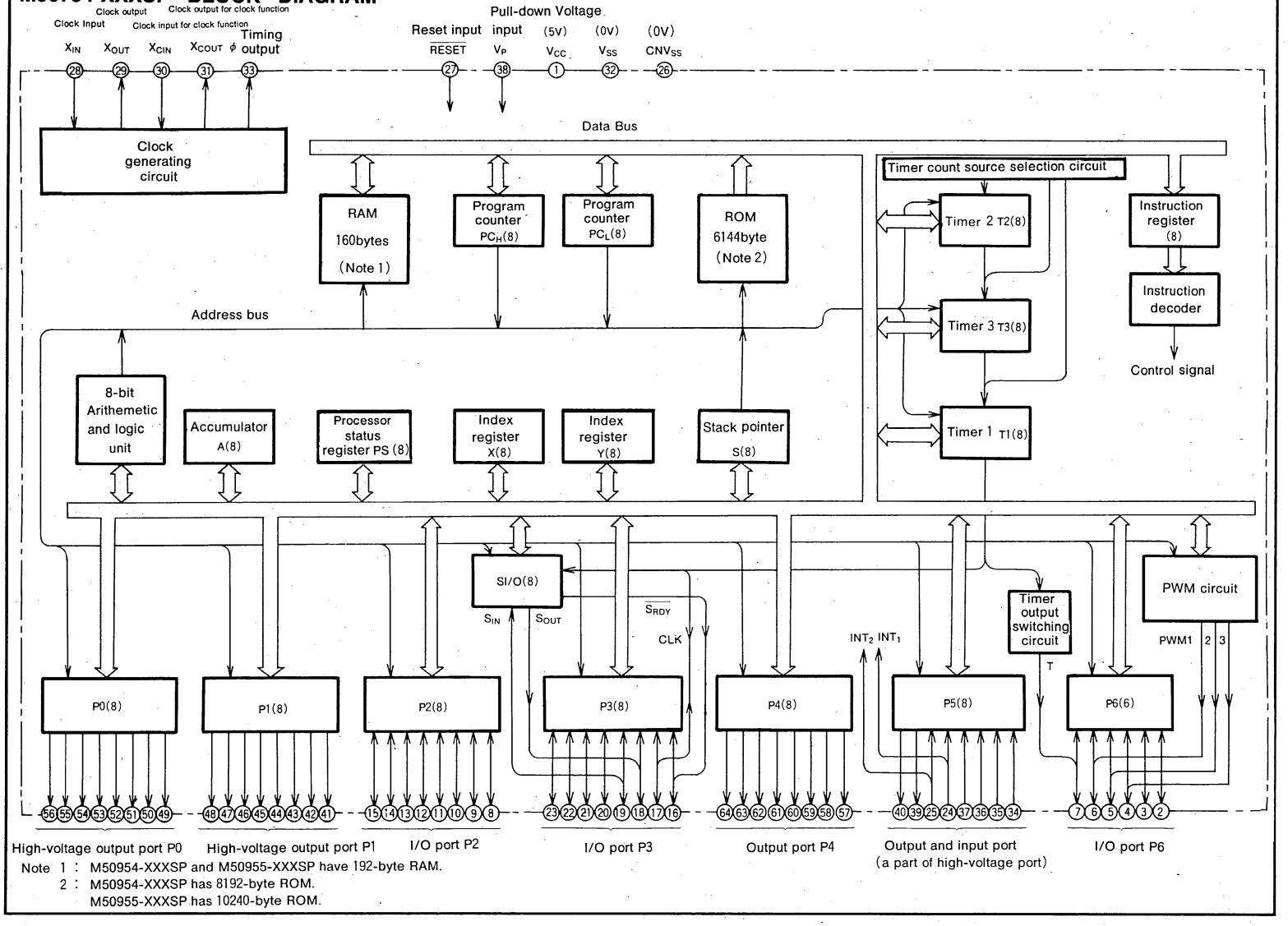
Outline 72P6



Outline 64P6W

NC : No connection

M50754-XXXSP BLOCK DIAGRAM



Note 1 : M50954-XXXSP and M50955-XXXSP have 192-byte RAM.
2 : M50954-XXXSP has 8192-byte ROM.
M50955-XXXSP has 10240-byte ROM.

FUNCTIONS OF M50754-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1.9μs (minimum instructions, at 4.2MHz frequency)
Clock frequency			4.2MHz
Memory size	ROM		6144bytes (8192bytes for M50954-XXXSP, 10240 bytes for M50955-XXXSP)
	RAM		160bytes (192bytes for M50954-XXXSP and M50955-XXXSP)
Input/Output ports	P0, P1, P4	Output	8-bit×3 (High voltage P-channel open drain; V_{CC}—38V)
	P2, P3	I/O	8-bit×2 (P3 can partially be used as both serial I/O and normal I/O.)
	$P5_0$, $P5_1$	Output	2-Bit×1 (High voltage P-channel open drain; V_{CC}—38V)
	$P5_2$, $P5_3$	Input	2-bit×1 (Can be used as an input for either INT_2 or INT_1.)
	$P5_4$~$P5_7$	Input	4-bit×1
	P6	I/O	6-bit×1 (Can be used as T_1 output or PWM output.)
Serial I/O			8-bit×1
Timers			8-bit timer×3 (×2, when used as serial input/output)
Subroutine nesting			80levels (max) (96 levels for M50954-XXXSP and M50955-XXXSP)
Interrupt			Two external interrupts, three internal timer interrupts (or timer×2, serial input/output×1)
Clock generating circuit			Two built-in circuits (externally connected ceramic or quartz crystal oscillator)
Supply voltage	at f(X_{IN})=4.2MHz		4.0~5.5V
	below f(X_{IN})=1.0MHz		3.0~5.5V
Power dissipation	at high-speed operation		15mW (clock frequency X_{IN}=4kHz)
	at low-speed operation		0.3mW (clock frequency X_{CIN}=32kHz)
	at stop mode		5μA (when clock is stopped)
Input/Output characteristics	Input/Output voltage		12V (Input/Output P2, P3, $P5_2$~$P5_7$)
			V_{CC}—38V (P0, P1, P4, $P5_0$, $P5_1$)
			—0.3V~V_{CC}+0.3V (Input/Output P6)
	Output current		10mA (P2, P3 : Nch open drain)
			—18mA (P0, P1 : high voltage P-ch open drain)
			—12mA (P4, $P5_0$, $P5_1$: high voltage P-ch open drain)
			0.5~—0.5mA (P6 : CMOS tri-states)
Memory expansion			Possibe
Operating temperature range			—10~70℃
Device structure			CMOS silicon gate process
Package	M50754-XXXSP/M50954-XXXSP/M50955-XXXSP		64-pin shrink plastic molded DIP
	M50754-XXXFP/M50954-XXXFP/M50955-XXXFP		72-pin plastic molded QFP
	M50754-XXXGP/M50954-XXXGP/M50955-XXXGP		64-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 4.0~5.5V at f(X_{IN})=4.2MHz and 3.0~5.5V below f(X_{IN})=1.0MHz to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P0, P1, P4, $P5_0$ and $P5_1$.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open. This clock can be used as the program controlled system clock.
X_{COUT}	Clock output for clock function	Output	
$P0_0$~$P0_7$	Output port P0	Output	Port P0 is an 8-bit output port. Output structure is high-voltage P-channel open drain. A pull-down transistor is built in between the V_P pin and this port. At reset, this port is set to a "L" level.
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P2. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively.
$P4_0$~$P4_7$	Output port P4	Output	Port P4 is an 8-bit output port and has basically the same functions as port P0.
$P5_0$, $P5_1$	Output port P5	Output	Bit 0 and 1 of port P5 are 2-bit output port and has basically the same functions as port P0.
$P5_2/INT_2$ $P5_3/INT_1$	Input port P5	Input	Bit 2 and 3 of port P5 are 2-bit input port and are in common with interrupt inputs.
$P5_4$~$P5_7$		Input	Bit 4~7 of port P5 are 4-bit input port.
$P6_0$~$P6_7$	I/O port P6	I/O	Port P6 is a 6-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. The output structure is CMOS tri-state output. $P6_0$, $P6_1$, $P6_2$, $P6_3$ can be programmed to function as timer output pin (T), PWM output pins (PWM_1, PWM_2, and PWM_3), respectively.

M50754-XXXSP/FP/GP, M50954-XXXSP/FP/GP, M50955-XXXSP/FP/GP

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50754-XXXSP is shown in Figure 1. Addresses $E800_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 6144 bytes.

Addresses $E000_{16}$ to $FFFF_{16}$ are the ROM address area assigned to the M50954-XXXSP.

Addresses $D800_{16}$ to $FFFF_{16}$ are the ROM address area assigned to the M50955-XXXSP.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $009F_{16}$ are assigned to the built-in RAM and consist of 160 bytes of static RAM. Addresses 0000_{16} to $00BF_{16}$ are the RAM address area assigned to the M50954-XXXSP and M50955-XXXSP. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

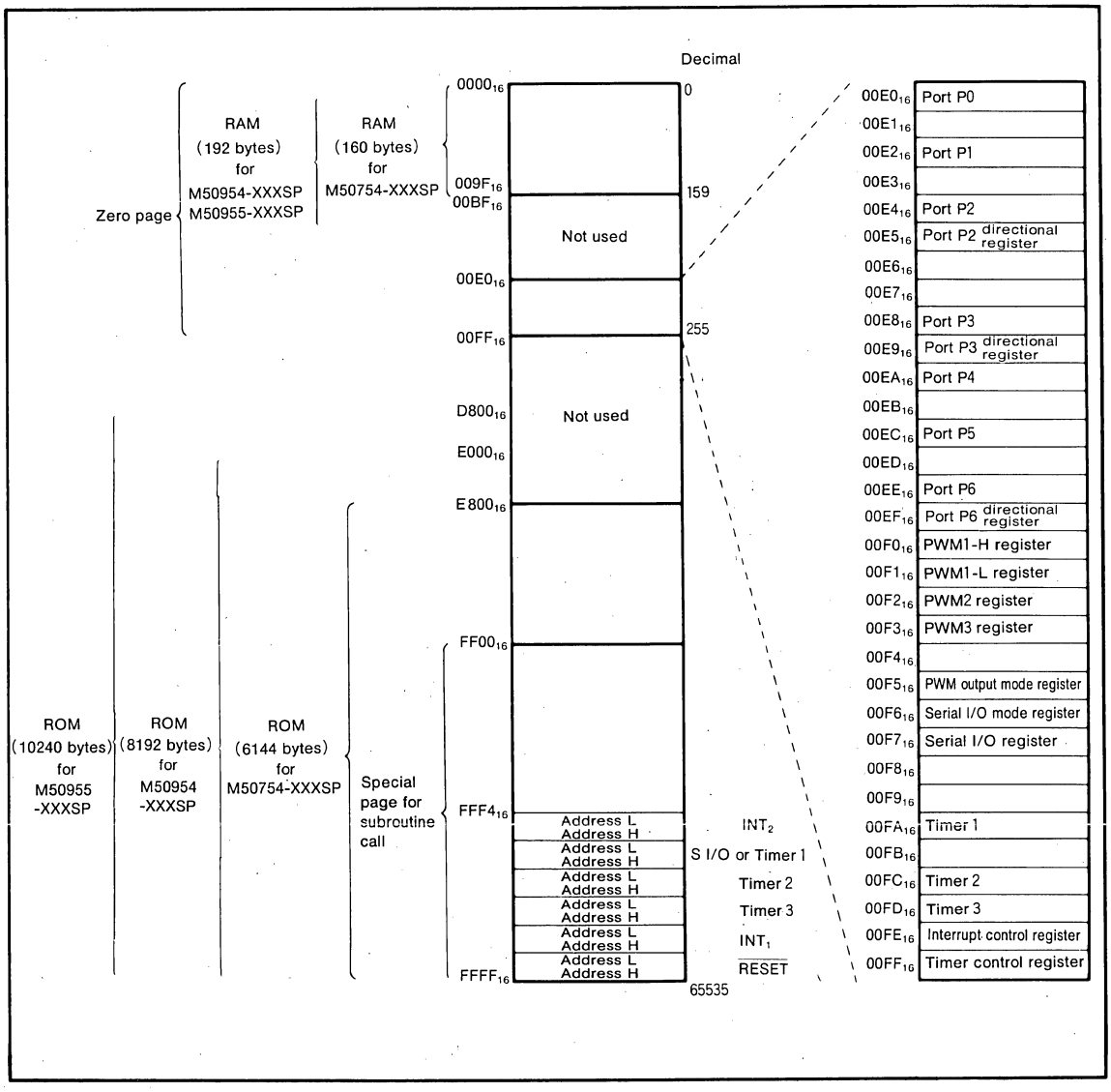


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

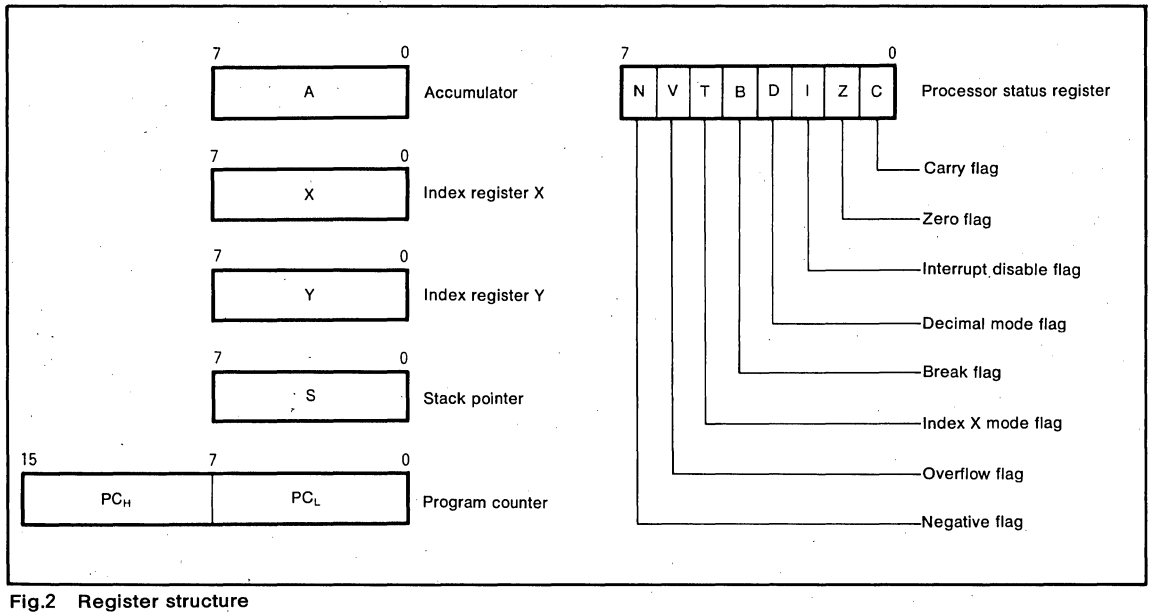


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When using this microcomputer in the single-chip mode, the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
INT_1	2	$FFFD_{16}$, $FFFC_{16}$
Timer 3	3	$FFFB_{16}$, $FFFA_{16}$
Timer 2	4	$FFF9_{16}$, $FFF8_{16}$
Timer 1 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
INT_2(BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50754-XXXSP can be interrupted from seven souces; INT_1, timer 3, timer 2, timer 1/serial I/O, or INT_2/BRK instruction.

The value of bit 2 of the serial I/O mode register (address $00F6_{16}$) determine whether the interrupt is from timer 1 or from serial I/O. When bit 2 is "0" the interrupt is from timer 1, and when bit 2 is "1" the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag I is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

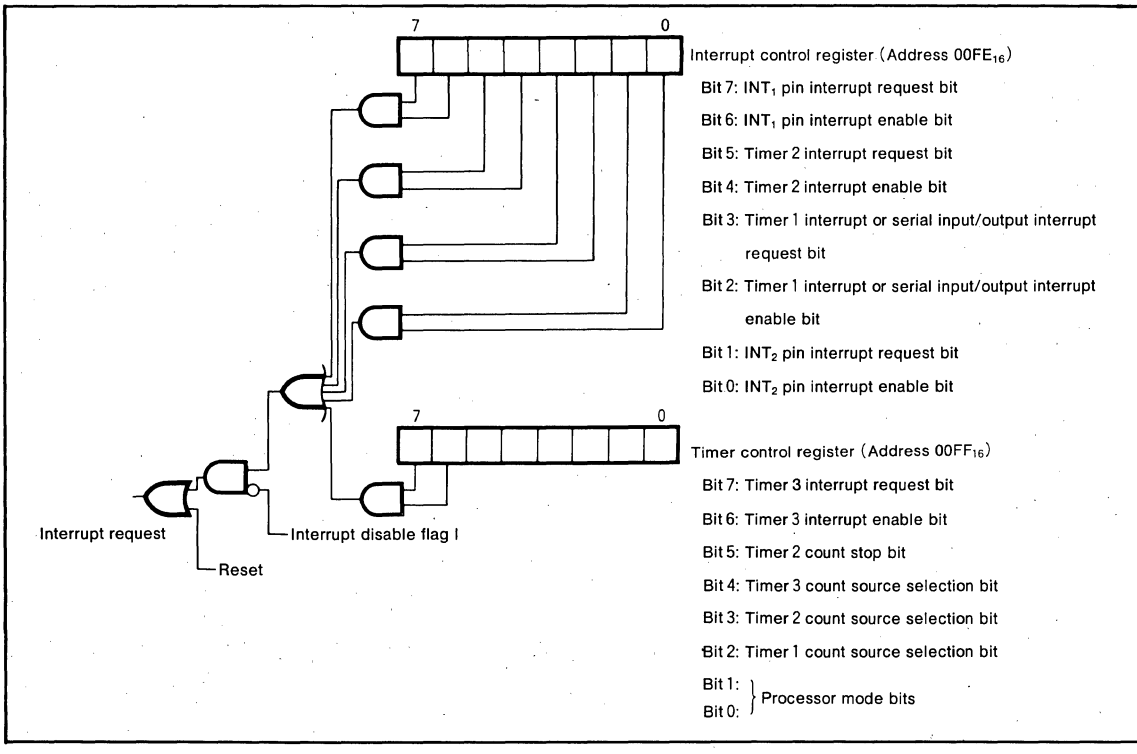


Fig.3 Interrupt control

The interrupt request bits are set when the following conditions occur:

(1) When the level of pins INT_1 and INT_2 change.
(2) When the contents of timer 3, timer 2, timer 1 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but can not be set by the progream. However, the interrupt enable bit can be set and reset by the program.

The change in level at which the INT pins generate a interrupt varies according to the content of bits 4 and 5 of the PWM output mode register (address $00F5_{16}$). When these bits are "0", the interrupt request is generated when INT changes from high-level to low-level. When these bits are "1", the interrupt request is generated when INT changes from low-level to high-level. Bits 4 (PM_4) and 5 (PM_5) correspond to INT_1 and INT_2 respectively.

Since the BRK instruction and the INT_2 interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if INT_2 generated the interrupt.

TIMER

The M50754-XXXSP has three timers; timer 1, timer 2, and timer 3. Since P3 (in serial I/O mode) and timer 1 use some of the same architecture, they cannot be used at the same time (see serial I/O section). The count source for each timer can be selected by using bit 2, 3 and 4 of the timer control register (address $00FF_{16}$), as shown in Figure 5.

A block diagram of timer 1 through 3 is shown in Figure 4.

All of the timers are down count timers and have 8-bit latchs. When a timer counter reaches "0", the contents of the reload latch are loaded into the timer at the next clock pulse. The division ratio of the timers is $1/(n+1)$, where n is the contents of the timer latch.

The timer interrupt request bit is set to "1" at the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section). The starting/stopping of timer 2 can be controlled by bit 5 of the timer control register. If bit 5 (address $00FF_{16}$) is "0", the timer starts counting and when bit 5 is "1", the timer stops.

When the STP instruction is executed, or after reset, the timer 2 and timer 3 latch are set to FF_{16} and 07_{16}, respectivery.

After a STP instruction is executed, timer 2, timer 3, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 4 of the timer control register). This state is canceled if the timer 3 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 2 count stop bit) and bit 4 of the interrupt control register (timer 2 interrupt enable bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

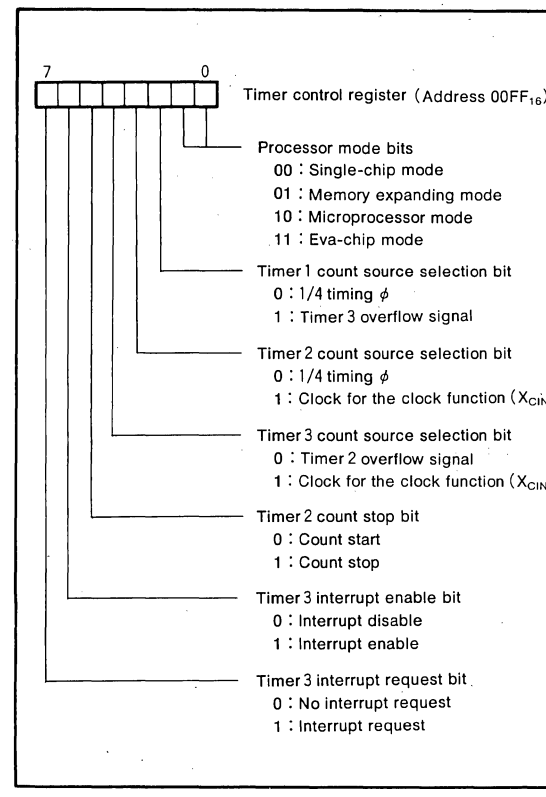


Fig.4 Structure of timer control register

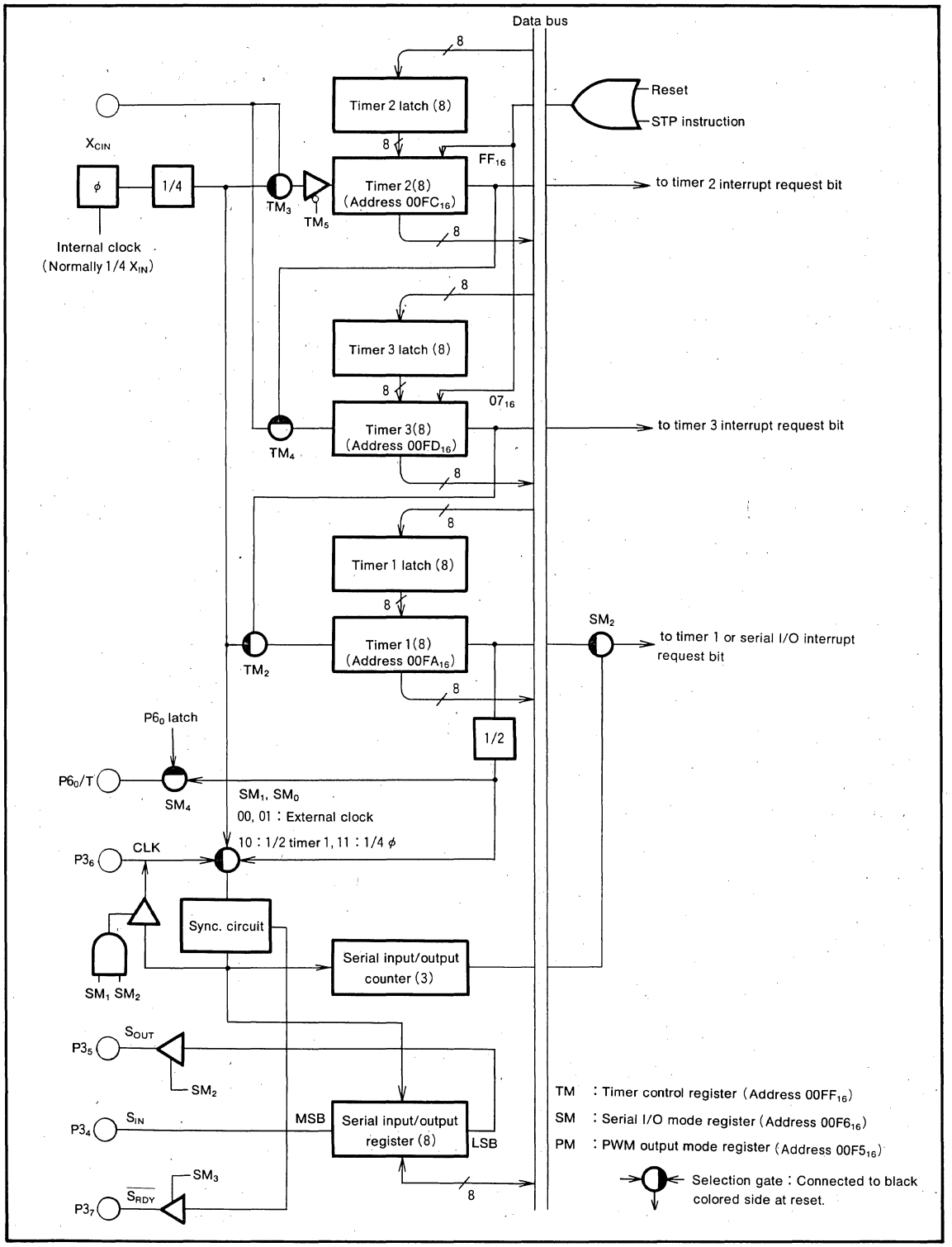


Fig.5 Block diagram of timer 1, timer 2, timer 3

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 6.

In the serial I/O mode the receive raady signal ($\overline{S_{RDY}}$), synchronous input /output clock (CLK), and the serial I/O pins (S_{OUT}, S_{IN}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F6_{16}$) is 8-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 1, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], timing ϕ divided by 4, becomes the clock.

Bit 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is a "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 1. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3=1, $\overline{S_{RDY}}$) or used as normal I/O pin

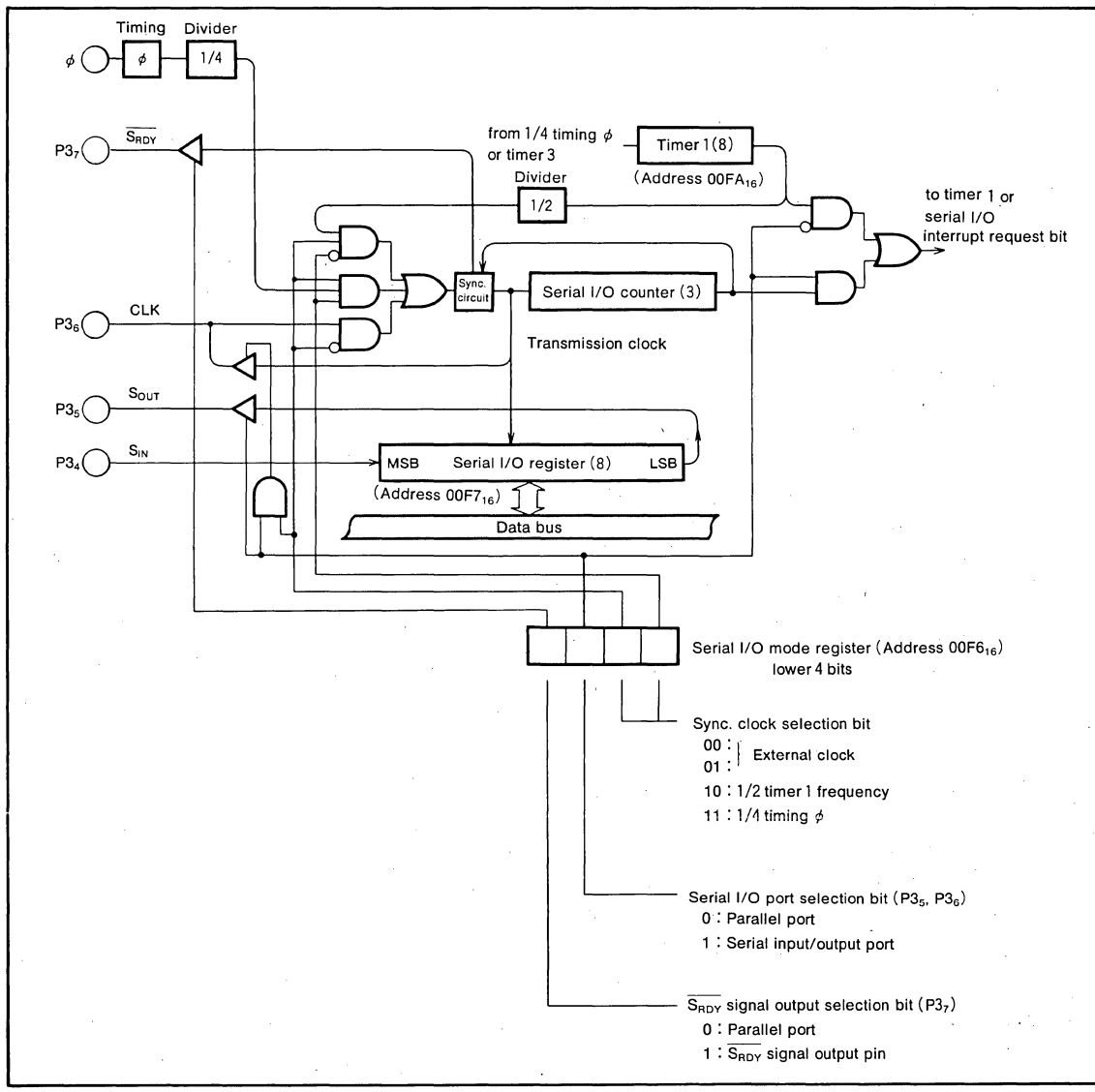


Fig.6 Block diagram of serial I/O

(bit 3=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address $00F7_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50754-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrpt request bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 7. An example of communication between two M50754-XXXSPs is shown in Figure 8.

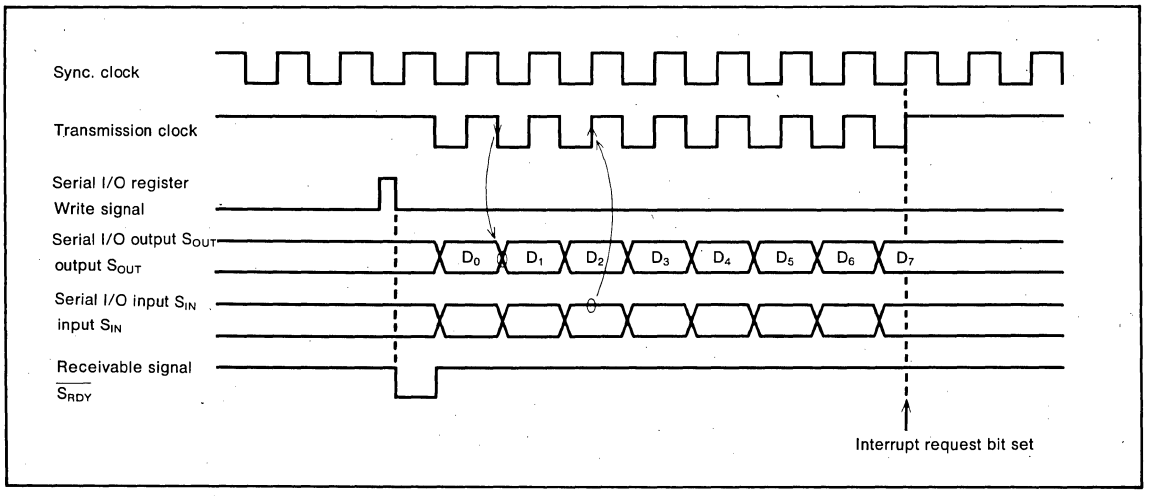


Fig.7 Serial I/O timing

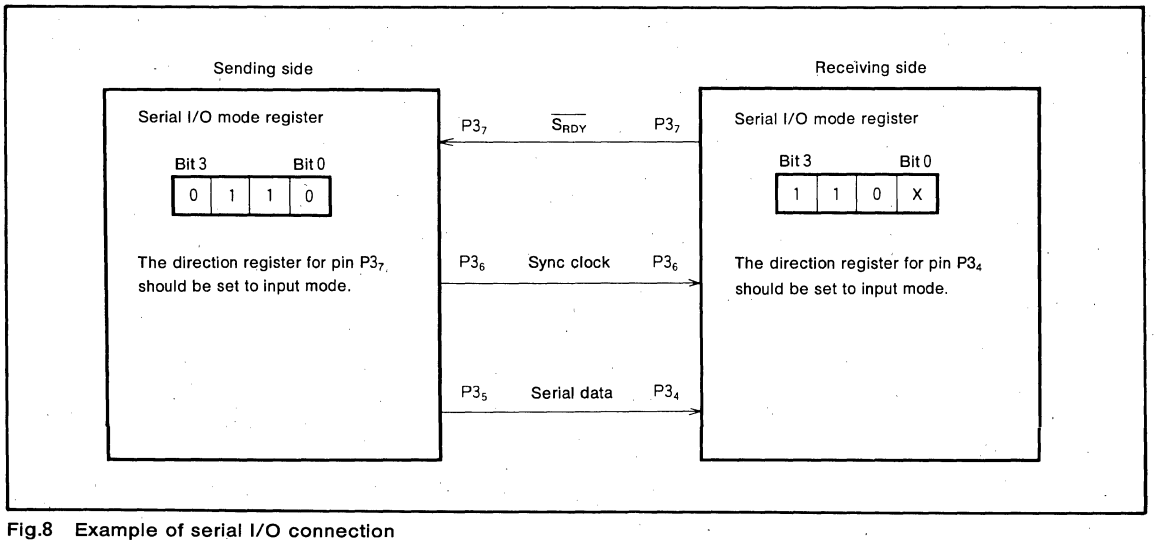


Fig.8 Example of serial I/O connection

PWM OUTPUT CIRCUIT

(1) Introduction

The M50754-XXXSP is equipped with one 14-bit and two 6-bit PWMs. The 14-bit resolution gives PWM1 the minimum resolution bit width of 500ns (for X_{IN}=4MHz) and a repeat period of 8192μs. PWM2 and PWM3 have a 6-bit resolution with minimum resolution bit width of 16μs and repeat period of 1024μs.

Block diagram of the PWM is shown in Figure 9.

The PWM timing generator section applies individual control signals to PWM 1~3, using clock input X_{IN} divided by 2 as a reference signal.

(2) Data setting

The output pins PWM1, PWM2 and PWM3 are in common with pins $P6_1$, $P6_2$ and $P6_3$ of port P6 (i.e. for PWM output, PM1~PM3 of the PWM control register and the P6 directional register $D6_1$~$D6_3$ should be set). When PWM1 is used for output, first set the higher 8-bit of the PWM1-H register (address $00F0_{16}$), then the lower 6-bit of the PWM1-L register (address $00F1_{16}$). When either PWM2 or PWM3 is used for output, set the 6-bit in the PWM2 (address $00F2_{16}$) or PWM3 (address $00F3_{16}$) register, respectively. Note that the higher 2 bits of these 8-bit registers are ignored when used 6-bit register.

(3) Transferring data from registers to latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period. The signals output to the PWM pins correspond to the contents of these latches. When data at addresses $00F0_{16}$ ~ $00F3_{16}$ is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. When the 6-bit latch is being read, the upper 2 bits of the register becomes undefined. However, bit 7 of the PWM1-L register indicated the completion of the data transfer from the PWM1 register to the PWM1 latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) Operation of the 6-bit PWMs

The timing diagram of the two 6-bit PWMs (PWM2 and PWM3) is shown in Figure 10. One period (T) is composed of 64 (2^6) segments.

There are six different pulse types configured from bits 0~5 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 10(a).

Six different pulses can be output from the PWM. These can be selected by bits 0 through 5. Depending on the content of the 6-bit PWM latch, pulses from 5~0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 10(b). Changes in the contents of the PWM latch allows the selection of 64 lengths of high-level area outputs varying from 0/64 to 63/64. An length of entirely high-level output cannot be output, i.e. 64/64.

(5) 14-bit PWM operation

The timing diagram of the 14-bit PWM1 is shown in Figure 11. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length N times τ is output every short area of t=256 τ =128μs as determined by data N of the higher 8 bits. (Refer to PWM output ② in the lower part of Figure 11.)

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that plus τ. As a result, the short-area period t(=128μs, approx. 7.8kHz) becomes an approximately repetitive period.

(6) Output after reset

At reset the output of port P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2 Relation between the 6 lower-order bits of data and the space set by the ADD bit

6 lower-order bits of data (LSB)	Area longer by τ than that of other t_m(m = 0 ~63)
0 0 0 0 0 0	Nothing
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m= 8, 24, 40, 56
0 0 1 0 0 0	m= 4, 12, 20, 28, 36, 42, 50, 58
0 1 0 0 0 0	m= 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m= 1, 3, 5, 7, ·····57, 59, 61, 63

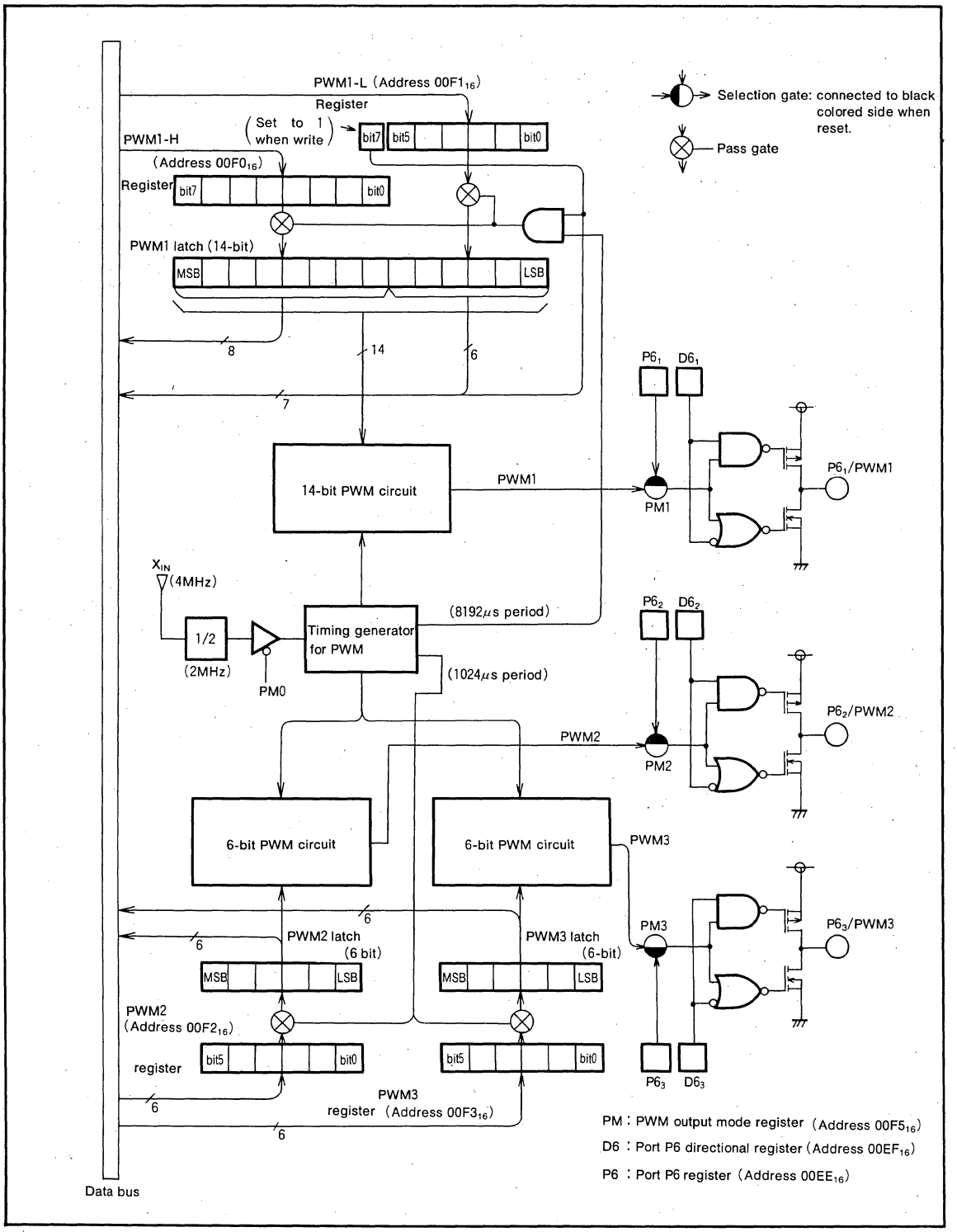


Fig.9 Bloock diagram of the PWM circuit

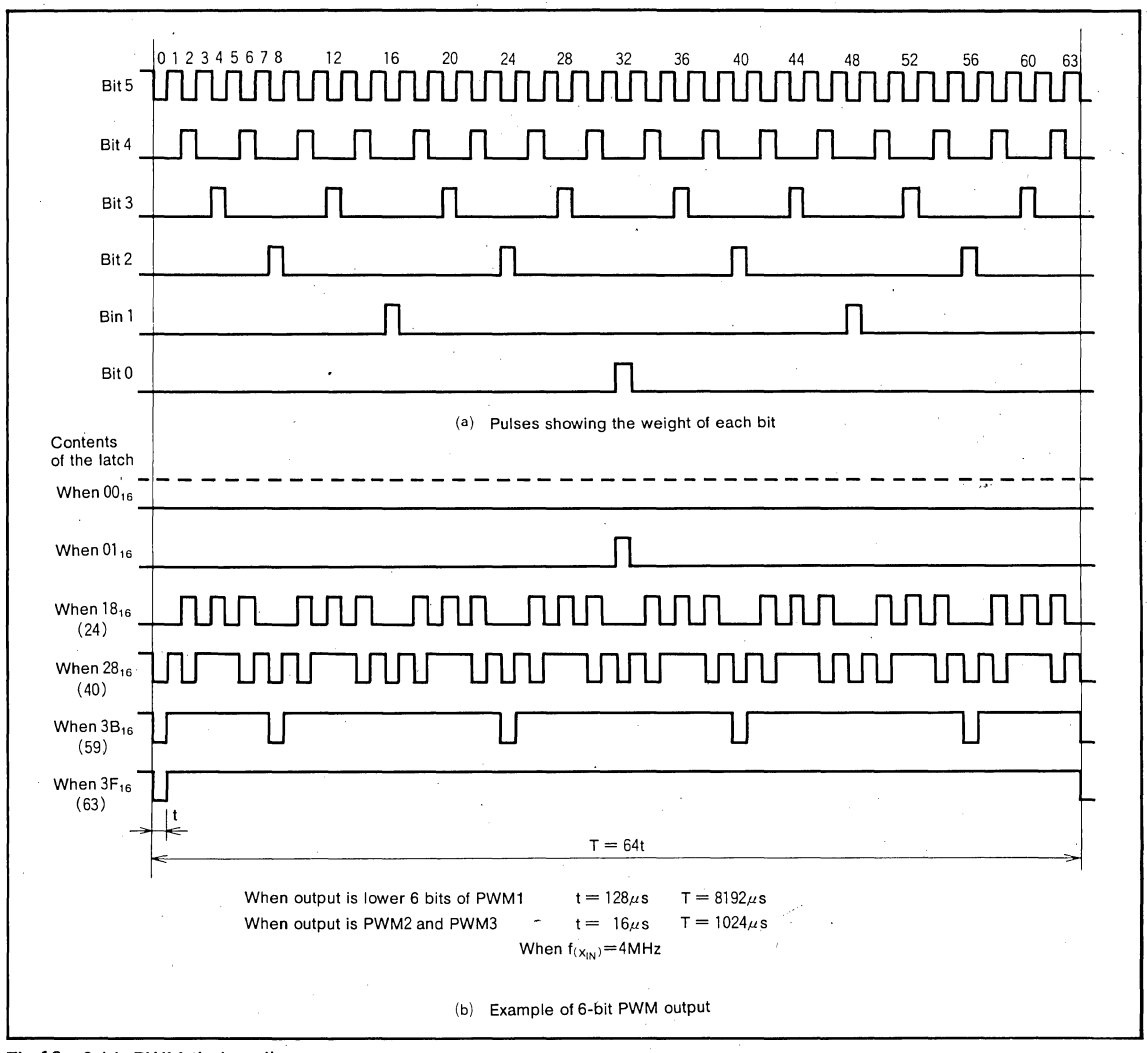


Fig.10 6-bit PWM timing diagram

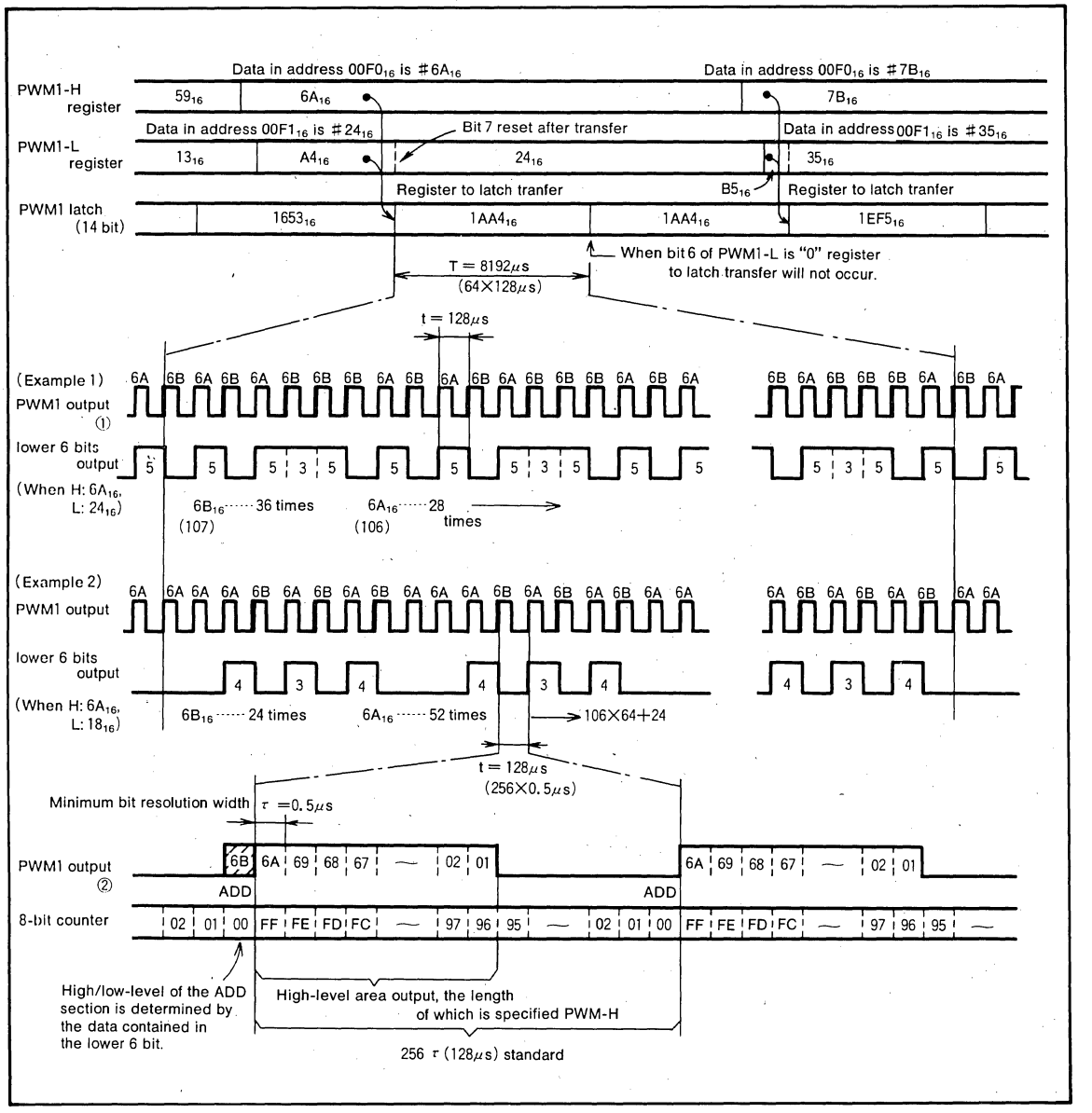


Fig.11 14-bit PWM timing diagram

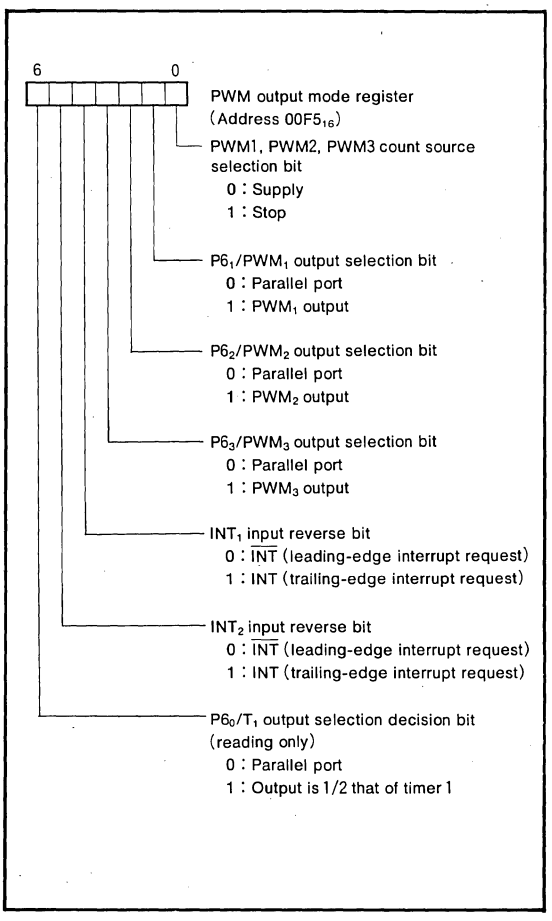


Fig.12 Structure of PWM output mode register

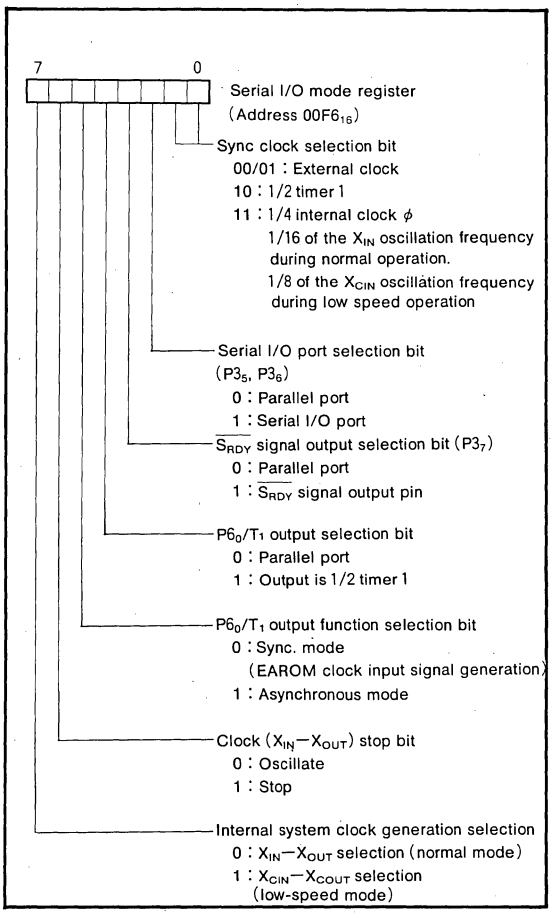
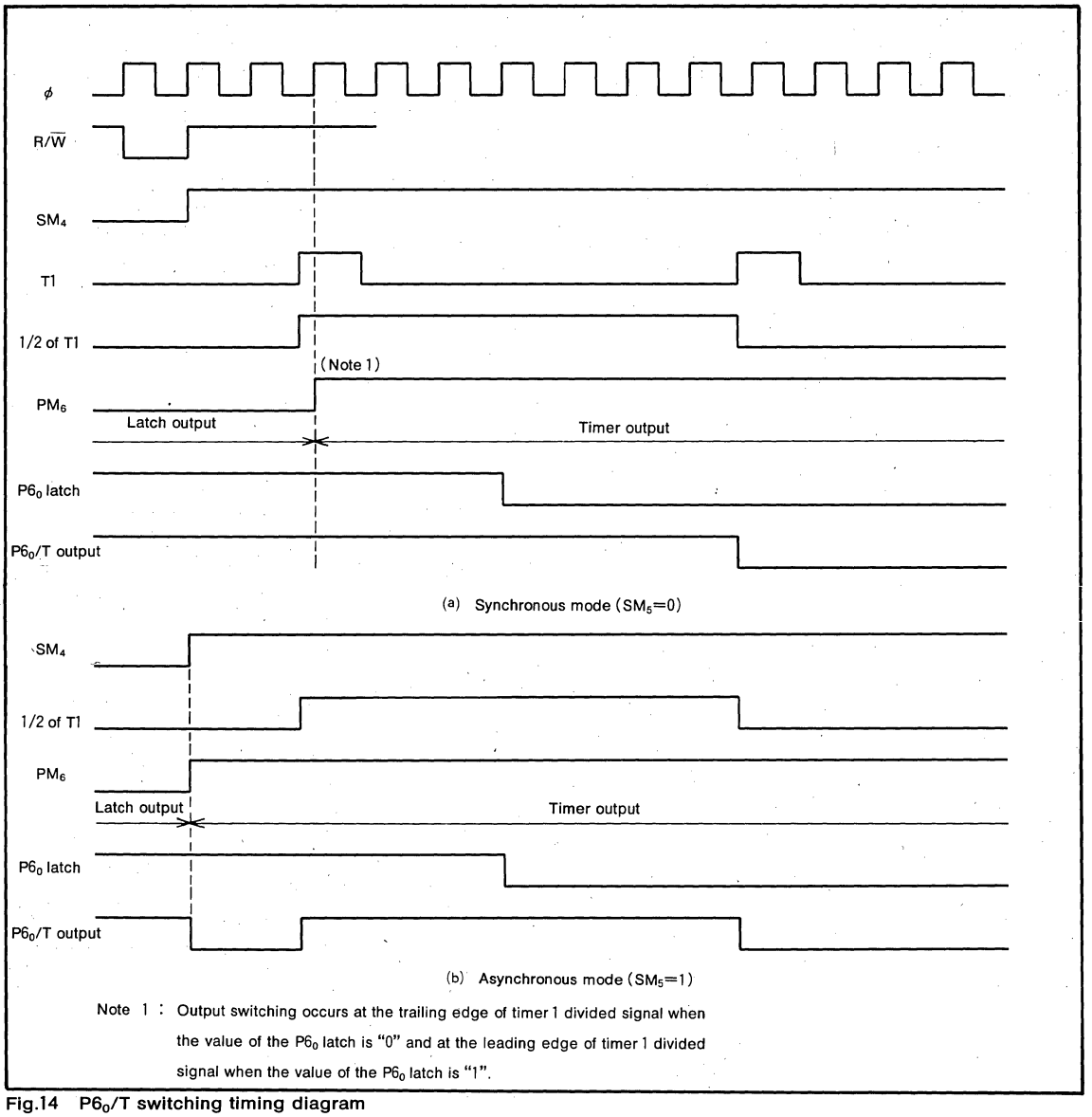


Fig.13 Structure of serial I/O mode register



Note 1 : Output switching occurs at the trailing edge of timer 1 divided signal when the value of the $P6_0$ latch is "0" and at the leading edge of timer 1 divided signal when the value of the $P6_0$ latch is "1".

Fig.14 $P6_0$/T switching timing diagram

PORT $P6_0$/TIMER 1 OUTPUT

Bit 0 of port P6 outputs 1/2 the frequency of timer 1 when $00F6_{16}$ bit 4 of the serial I/O mode register (address $00F6_{16}$) is changed. The output switching can be accomplished with either of two procedures, synchronous mode or asynchronous mode, depending on the setting of bit 5 (SM_5) of the serial I/O mode register.

When SM_5 is set to "0" the synchronous mode is set. In such a case, after SM_4 has been changed, synchronization is set to the 1/2 frequency of timer 1 and switching between the port latch and timer takes place. It is possible to ascertain whether switching actually occurred by reading the value of bit 6 (PM_6) of the PWM output mode register.

From the time that the contents of SM_4 was changed to the point where switching completes, the contents of neither SM_4 nor $P6_0$ may be changed. Use of the synchronous mode prevents the generation of a pulse shorter than the timer output during swiching. Figure 14 (a) gives an example of timing in the synchronous mode. Use of the synchronous mode allows generation of an EAROM clock input signal through the use of a simple program.

When SM_5 is set to "1", the asynchronous mode is set. In this case, the output switching occurs directly after SM_4 has been changed. Figure 14 (b) gives an example of timing in the asynchronous mode.

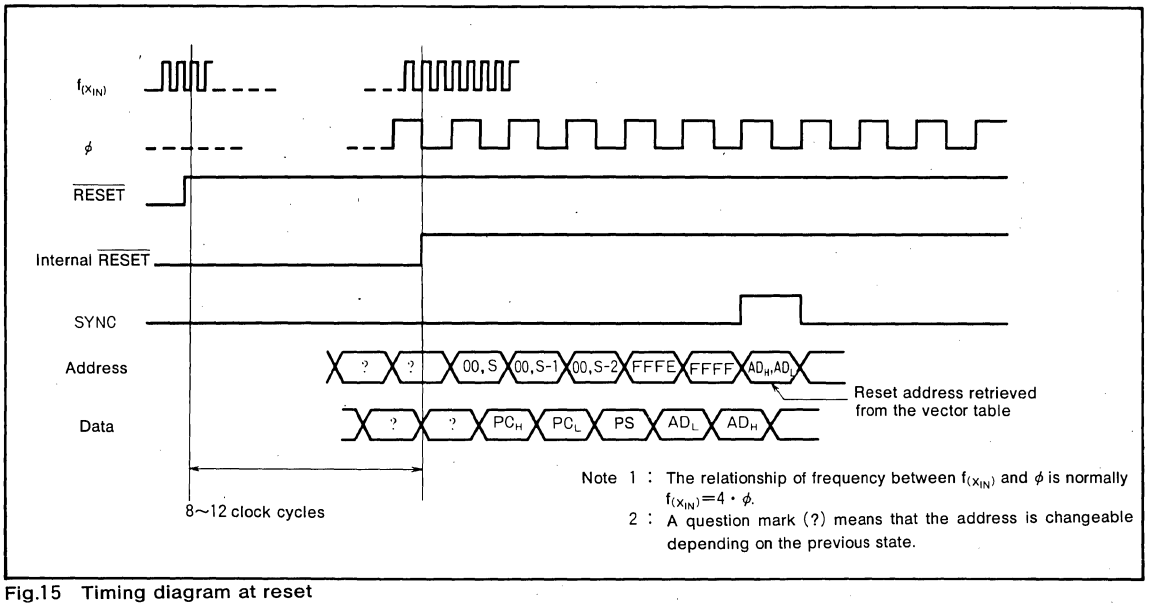


Fig.15 Timing diagram at reset

RESET CIRCUIT

The M50754-XXXSP is reset according to the sequence shown in Figure 15. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 16. An example of the reset circuit is shown in Figure 17. When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

		Address
(1) Port 0 register	(P0) ($E0_{16}$) ···	00_{16}
(2) Port 1 register	(P1) ($E2_{16}$) ···	00_{16}
(3) Port P2 directional register	(D2) ($E5_{16}$) ···	00_{16}
(4) Port P3 directional register	(D3) ($E9_{16}$) ···	00_{16}
(5) Port 4 register	(P4) (EA_{16}) ···	00_{16}
(6) Port 5 register	(P5) (EC_{16}) ···	00
(7) Port P6 directional register	(D6) (EF_{16}) ···	00_{16}
(8) PWM output mode register	(PM) ($F5_{16}$) ···	0 0 0 0 0 0 0 0
(9) Serial I/O mode register	(SM) ($F6_{16}$) ···	00_{16}
(10) Timer 2	(T2) (FC_{16}) ···	FF_{16}
(11) Timer 3	(T3) (FD_{16}) ···	07_{16}
(12) Interrupt cotrol register	(IM) (FE_{16}) ···	00_{16}
(13) Timer control register	(TM) (FF_{16}) ···	00_{16}
(14) Processor status register (only the interrupt disable flag is set.)	(PS) ···	1
(15) Program counter	(PC_H) ···	Contents of address $FFFF_{16}$
	(PC_L) ···	Contents of address $FFFE_{16}$

Since the contens of both registers other than those listed above (including timer 1 and the serial I/O registers) and the RAM are undefined at reset, it is necessary to set initial values.

Fig.16 Internal state of the microcomputer at reset

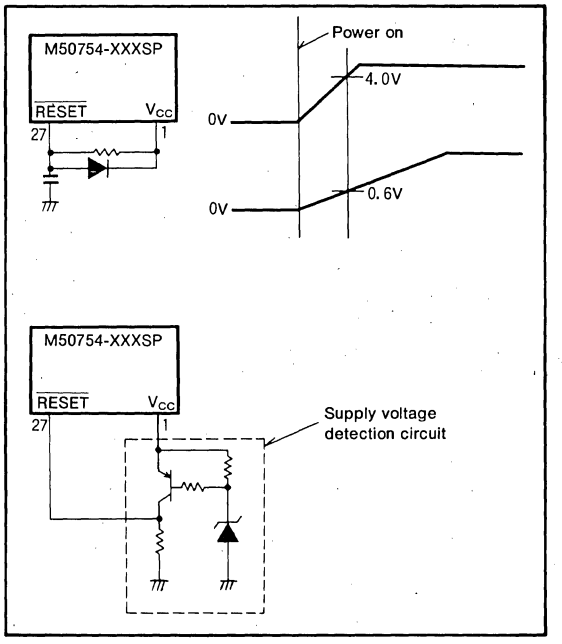


Fig.17 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit output port with high-breakdown voltage p-channel open-drain outputs featuring a breakdown voltage of V_{CC}-36V. Each pin contains a pull-down resistor making V_P a negative power source. As shown in the memory map in Figure 1, port P0 is used on the zero page at address $00E0_{16}$ in memory.

Depending on the content of the processor mode bit (bits 0 and 1 of address $00FF_{16}$), four modes can be selected, single-chip mode, memory expanding mode, microprocessor mode, memory expanding mode, microprocessor mode, and eva-chip mode. Modes other than the single-chip mode also have functions as address output pins besides their original functions. For details, refer to the section on the processor mode.

(2) Port P1

Port P1 has the same functions as port P0 in the single-chip mode. In modes other than the single-chip mode, functions vary slightly. For details, see the section on the processor mode.

(3) Port P2

Port P2 is an 8-bit I/O port with N-channel open drain outputs As shown in Figure 1, port P2 is used at address $00E4_{16}$ in the memory.

Port P2 has a data direction register (address $00E5_{16}$ on zero page) and programming can be undertaken for an individual bit to use the port for input or output. The pins where the data direction register is programmed to "1" are for output and those where the register is programmed to "0" are for input.

The data written into the pin programmed as an output pin are written into the port latch and supplied directly to the output pin. When reading the data from a pin programmed as an output pin, it is not the output pin contents which are read but the port latch contents. Consequently, since an LED or other similar part is driven directly, the value output previously can be read correctly even if the low-level output voltage goes high. The pin programmed as an input pin remains floating, so external signals can be read. When data is written, it is written into the port latch only and the pin remains floating.

This port has the same functions as port P0 except for the single-chip mode. For details, see the section on the processor mode.

(4) Port P3

Apart from the fact that part of the pins are also used as serial input/output pins, its functions are the same as those of port P2 in the single-chip mode. This port has the same functions as port P0 except in the single-chip mode. For details, see the section on the processor mode.

(5) Port P4

Port P4 has the same functions as port P0 in the single-chip mode. The functions of this port do not change regardless of though the processor mode.

(6) Port P5

Bits 0 and 1 of port P5 have the same functions as port P4.

Bits 2 and 3 are exclusively used as inputs for mutual use as interrupt inputs. These pins feature hysteresis characteristics. These pins can also be used for fetching inputs even when being used as interrupt inputs.

The interrupt request bits (bit 7 and 1 of address $00FE_{16}$ = INT_1 and INT_2, respectively) are set to "1" when the inputs of ports $P5_3$ (INT_1) and $P5_2$ (INT_2) change. Depending on the contents of bits 4 and 5 of the PWM output mode register PM (address $00F5_{16}$), either a raising-edge interrupt or a falling-edge interrupt may be selected as the interrupt source. (Refer to Figure 12.)

Since interrupt input and normal input ports are used together in the M50754-XXXSP, unwanted noise may mistakenly cause interrupts. This problem can be overcome by programming.

When changing either bit 4 (PM_4) or bit 5 (PM_5) of the PWM output mode register, it is necessary for the interrupt request enable bit (either bit 6 or 0 of address $00FE_{16}$) to be set to the interrupt disable condition ("0"). If this is not done, an interrupt will be generated when either PM_4 or PM_5 is changed.

Bits 4 through 7 of port P5 is a 4-bit input port.

(7) Port P6

Port P6 is a 6-bit I/O port having the same functions as Port P2. The output is CMOS three-state. Bit 0 is used in common with the timer output. Bits 1~3 are used in common with PWMs 1~3.

The functions of this port do not change, being the same as in the single-chip mode, even though the processor mode may change.

A block diagram of ports P0 through P6 are shown in Figure 18.

(8) Clock ϕ output pin

The clock frequency, divided by four, is output (X_{IN}). However, in the low-speed mode 1/2 the clock frequency for timer (X_{CIN}) is output.

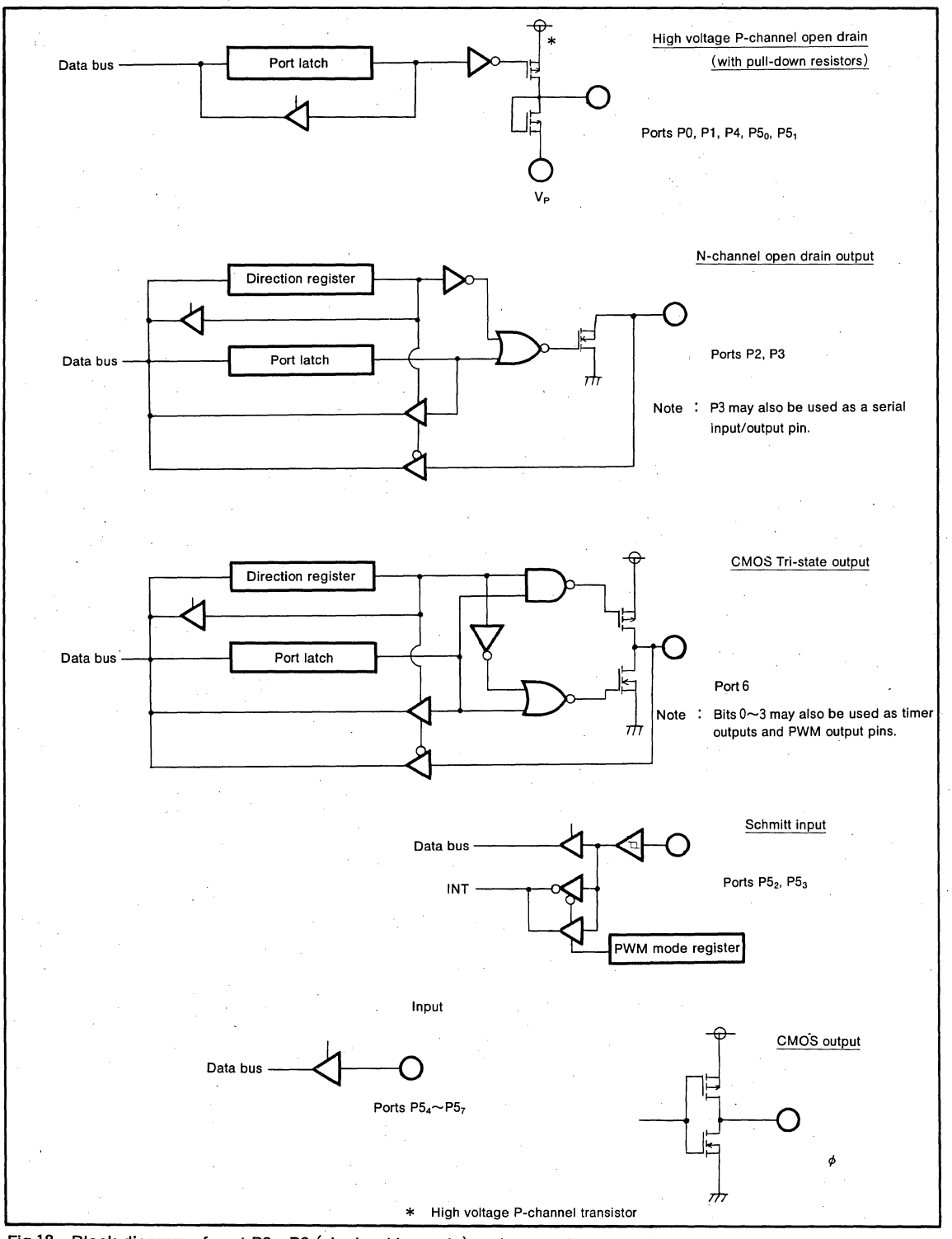


Fig.18 Block diagram of port P0~P6 (single-chip mode) and output format of ϕ

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 20 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 19.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

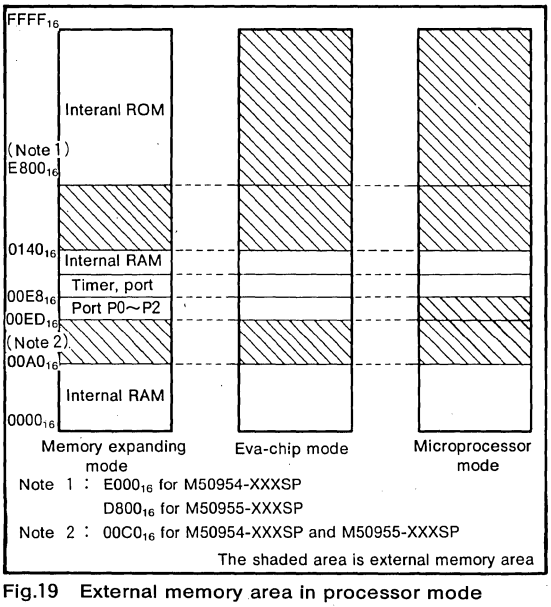


Fig.19 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode.

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the data bus (D_7～D_0) and loses its normal I/O functions. Port $P3_1$ and $P3_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is requierd.

This mode has almost the same function as the memory expanding mode except that it needs to attach all program memories to the outside.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

Port \ Mode	Single-chip mode (TM_1=0, TM_0=0)	Memory expanding mode (TM_1=0, TM_0=1)	Eva-chip mode (TM_1=1, TM_0=1)	Microprocessor mode (TM_1=1, TM_0=0)
Port P0	Ports $P0_7$~$P0_0$: I/O port	Ports $P0_7$~$P0_0$: Address A_7~A_0 / I/O port	Same as left	Ports $P0_7$~$P0_0$: Address A_7~A_0
Port P1	Ports $P1_7$~$P1_0$: I/O port	Ports $P1_7$~$P1_0$: Address A_{15}~A_8 / I/O port	Same as left	Ports $P1_7$~$P1_0$: Address A_{15}~A_8
Port P2	Ports $P2_7$~$P2_0$: I/O port	Ports $P2_7$~$P2_0$: Output port / Data D_7~D_0	Same as left	Ports $P2_7$~$P2_0$: Data D_7~D_0
Port P3	Ports $P3_7$~$P3_0$: I/O port	Ports $P3_7$~$P3_2$: I/O port; Port $P3_1$: SYNC / I/O port; Port $P3_0$: R/$\overline{W}$ / I/O port	Same as left	Ports $P3_7$~$P3_2$: I/O port; Port $P3_1$: SYNC; Port $P3_0$: R/$\overline{W}$

Fig.20 Processor mode and functions of ports P0~P3

Table 3 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The M50754-XXXSP has two internal clock generating circuit. Figure 23 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ. Bit 7 of serial I/O mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 21 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacture's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input form the $X_{IN}(X_{CIN})$ pin and leave the $X_{OUT}(X_{COUT})$ pin open. A circuit example is shown in Figure 22.

The M50754-XXXSP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 2 and timer 3 are forcibly connected and $\phi/4$ is selected as timer 2 input. Also, timer 2 and timer 3 loaded with FF_{16} and 07_{16} respectively to enable the oscillator to stabilize when restarting oscillation. Before executing the STP instruction, the timer 2 count stop bit must be set to supply ("0"), timer 2 interrupt enable bit and timer 3 interrupt enable bit must be set to disable ("0"), and timer 3 interrupt request bit must be set to no request ("0").

Oscillation is resarted (release the stop mode) when INT_1, INT_2, or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 3 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the $\overline{RESET}$ pin until the oscillattion stabilizes because no wait time is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock (200μA(max.) at $f(X_{CIN}) = 32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of serial I/O mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 24 shows the transition of states for the system clock.

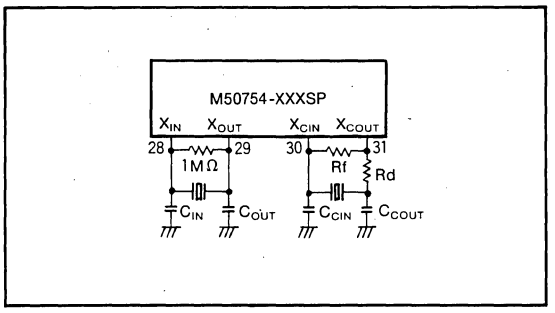


Fig.21 Example ceramic resonator circuit

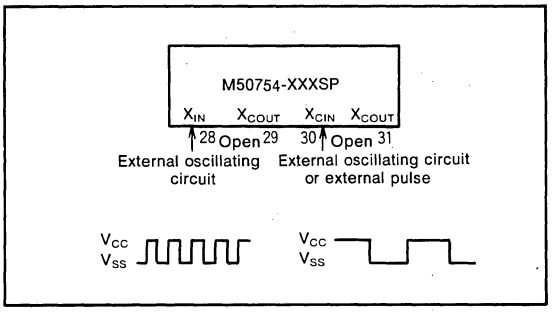


Fig.22 Example clock input circuit

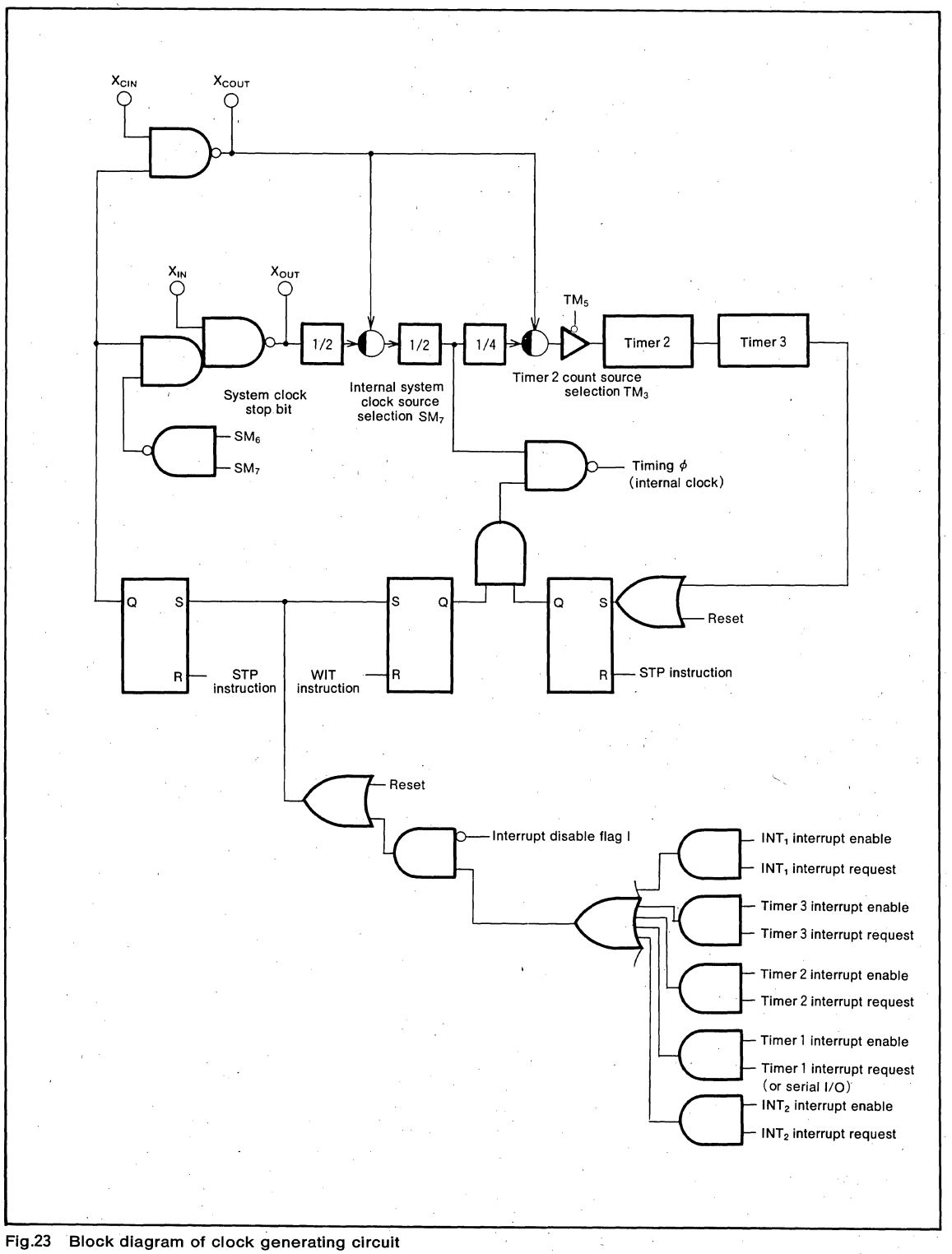
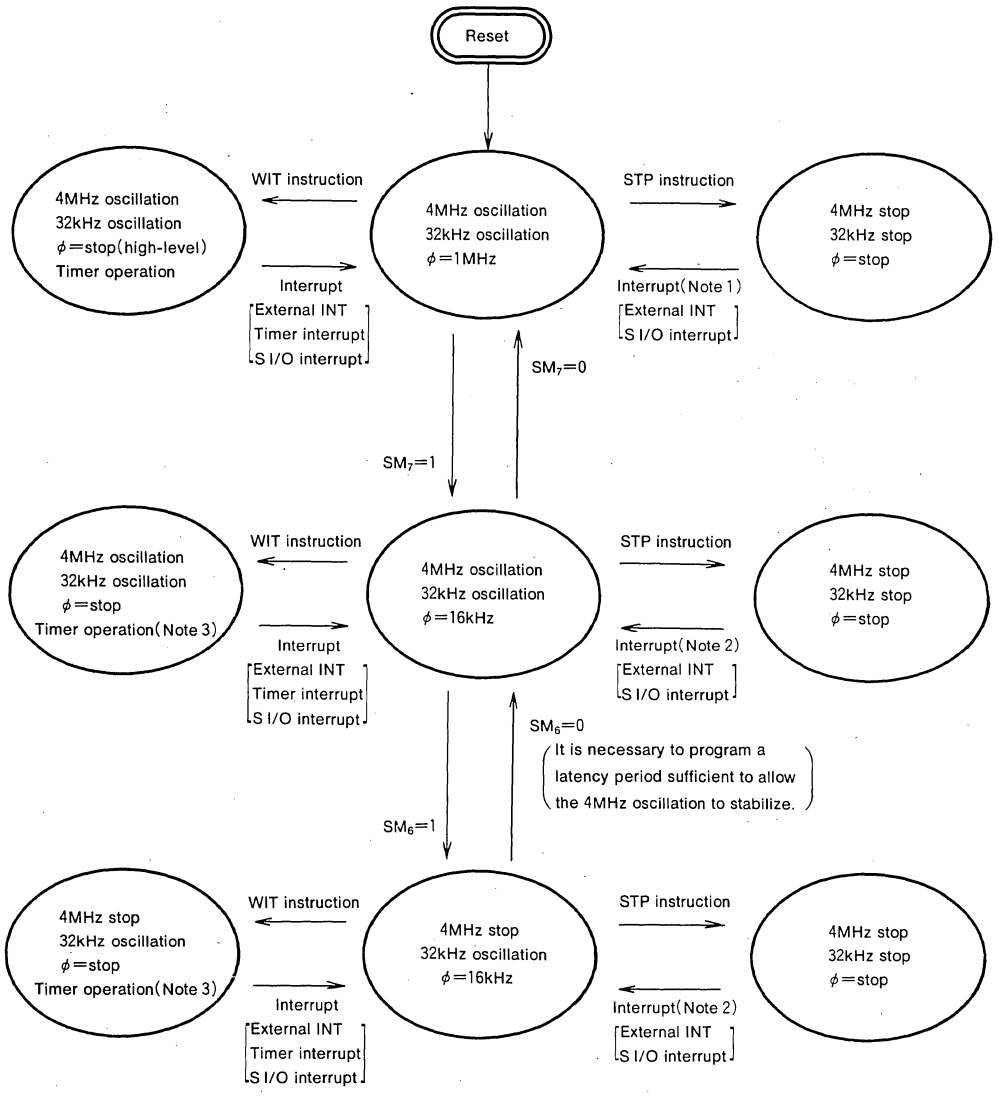


Fig.23 Block diagram of clock generating circuit

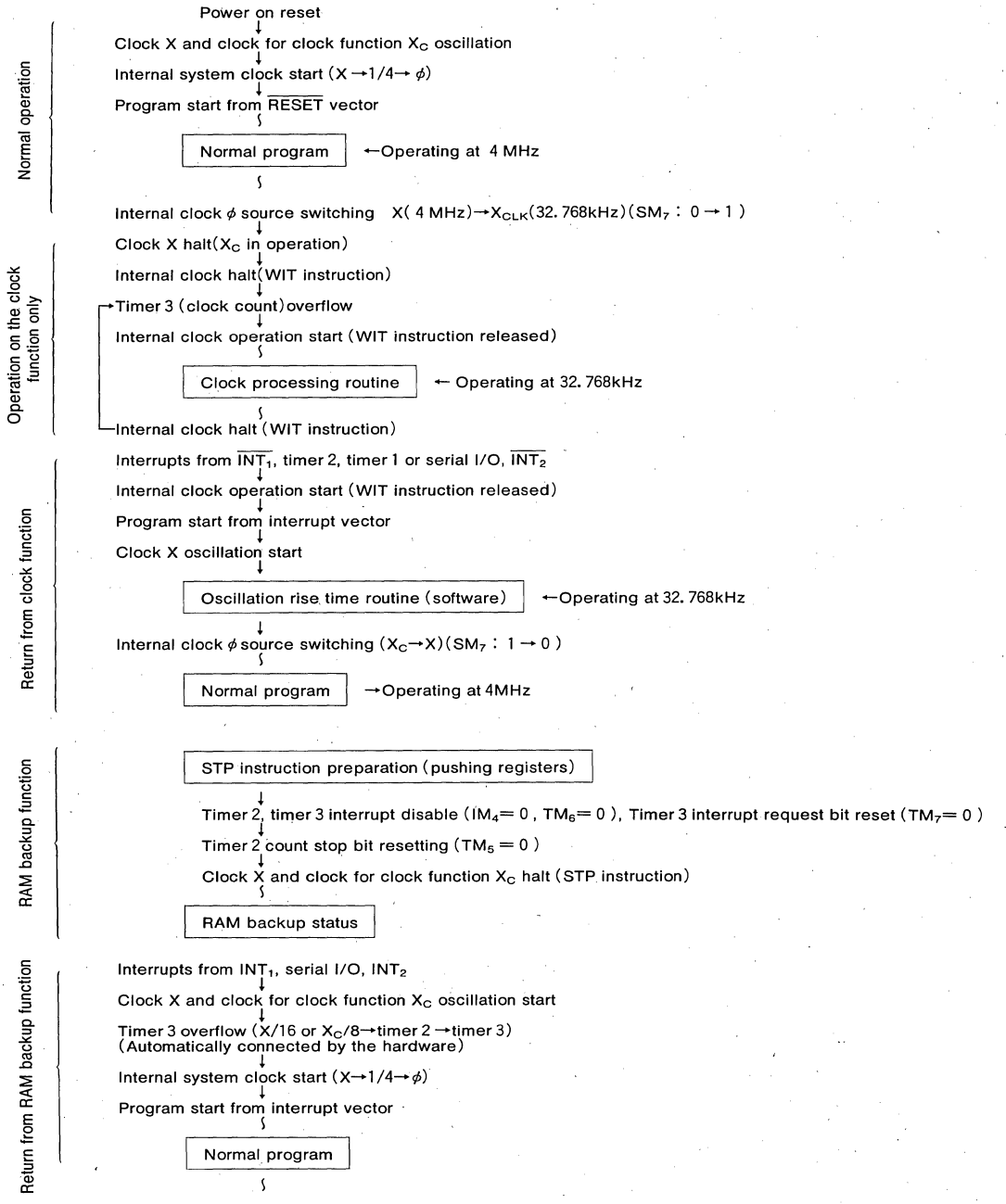


The above example assumes that signals of 4MHz and 32kHz are being applied to pins X_{IN} X_{CIN} respectively. ϕ signifies the internal clock.

(Note 1) Approximately 8ms of latency time are automatically generated upon release from the STP instruction due to the connections of timer 2 and 3.
(Note 2) Approximately 500ms of latency time exists after the release of the STP instruction.
(Note 3) When the internal clock 1/4 frequency is connected as a timer count source the count source becomes 4kHz.

Fig.24 Transition of states for the system clock

≪An example of flow for system≫



PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When $\phi/4$ or it divided by timer are used as clock for timer, the contents of the timer can be read at voluntary timing.
However, when an other clock (except above clocks) is input to timer, read the contents of timer either while the input of the timer is not changing or after timer count is stopped.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confiramation form.

(2) mark specification form.

(3) ROM data ····· EPROM 3sets.

Write the following option on the mask ROM confirmation from.

• ϕ output stop option.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off.	−0.3∼7	V
V_P	Pull-down input voltage		V_{CC}−40∼V_{CC}+0.3	V
V_I	Input voltage, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNV_{SS}, $P5_2/INT_2$, $P5_3/INT_1$		−0.3∼13	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, X_{CIN}		−0.3∼7	V
V_I	Input voltage, $P6_0$∼$P6_5$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage, $P5_4$∼$P5_7$		−0.3∼13	V
V_O	Output voltage, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$		−0.3∼13	V
V_O	Output voltage, $P6_0$∼$P6_5$, X_{OUT}, X_{COUT}, ϕ		−0.3∼V_{CC}+0.3	V
V_O	Output voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P4_0$∼$P4_7$, $P5_0$, $P5_1$		V_{CC}−40∼V_{CC}+0.3	V
Pd	Power dissipation	T_a = 25℃	1000(Note 1)	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : 600mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Nom.	Limits Max.	Unit
V_{CC}	Supply voltage	$f_{(X_{IN})}$=4.2MHz	4	5	5.5	V
		$f_{(X_{IN})}$=less than1MHz	3	5	5.5	V
V_P	Pull-down supply voltage		V_{CC}−38		V_{CC}	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNV_{SS}(Note 2) $P5_2/INT_2$, $P5_3/INT_1$, $P6_0$∼$P6_5$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P5_4$∼$P5_7$		0.4V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNV_{SS} $P5_2/INT_2$, $P5_3/INT_1$, $P6_0$∼$P6_5$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P5_4$∼$P5_7$		0		0.12V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P4_0$∼$P4_7$ $P5_0$, $P5_1$				−120	mA
$I_{OH(sum)}$	"H" sum output current $P6_0$∼$P6_5$				−5	mA
$I_{OL(sum)}$	"L" sum output current $P2_0$∼$P2_7$, $P3_0$∼$P3_7$				50	mA
$I_{OL(sum)}$	"L" sum output current $P6_0$∼$P6_5$				5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$∼$P0_4$				−30	mA
$I_{OH(peak)}$	"H" peak output current $P0_5$∼$P0_7$, $P1_0$∼$P1_7$				−30	mA
$I_{OH(peak)}$	"H" peak output current $P4_0$∼$P4_7$, $P5_0$, $P5_1$				−30	mA
$I_{OH(peak)}$	"H" peak output current $P6_0$∼$P6_5$				−3	mA
$I_{OL(peak)}$	"L" peak output current $P2_0$∼$P2_7$, $P3_0$∼$P3_7$				15	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$∼$P6_5$				3	mA
$I_{OH(avg)}$	"H" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$(Note7)				−12	mA
$I_{OH(avg)}$	"H" average output current $P4_0$∼$P4_7$, $P5_0$, $P5_1$				−12	mA
$I_{OH(avg)}$	"H" average output current $P6_0$∼$P6_5$				−1.5	mA
$I_{OL(avg)}$	"L" average output current $P2_0$∼$P2_7$, $P3_0$∼$P3_7$				10	mA
$I_{OL(avg)}$	"L" average output current $P6_0$∼$P6_5$				1.5	mA
$f_{(X_{IN})}$	Clock input oscillating frequency (Note 3, 4, 6)				4.2	MHz
$f_{(X_{CIN})}$	Clock oscillating frequency for clock function				500	kHz

Note 2 : High-level input voltage of up to +12V may be applied to permissible for ports $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNV_{SS}, and $P5_2$∼$P5_7$.
3 : Oscillation frequency is at 50% duty cycle.
4 : When used in the low-speed mode, the timer clock input frequency should be $f_{(XIN)} < f_{(XIN)}/3$.
5 : When external clock input is used, the timer clock input frequency should be $f_{(XCIN)} \leqq 50kHz$.
6 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are in period of 100ms.
7 : −18mA for M50954-XXXSP, M50955-XXXSP.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P6_0$~$P6_5$	I_{OH}=−0.5mA	V_{CC}−0.4			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA	V_{CC}−2			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$	I_{OH}=−12mA(M50754-XXXSP)	V_{CC}−2			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$	I_{OH}=−18mA(M50954-XXXSP, M50955-XXXSP)	V_{CC}−2			V
V_{OH}	"H" output voltage $P4_0$~$P4_7$, $P5_0$, $P5_1$	I_{OH}=−12mA	V_{CC}−2			V
V_{OL}	"L" output voltage $P2_0$~$P2_7$, $P3_0$~$P3_7$	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage $P6_0$~$P6_5$	I_{OL}=0.5mA			0.4	V
V_{OL}	"L" output voltage ϕ	I_{OL}=2.5mA			2	V
$V_{T+}-V_{T-}$	Hysteresis $P5_2/INT_2$, $P5_3/INT_1$		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P2_0$~$P2_7$, $P3_0$~$P3_7$	V_I=0V			−5	μA
I_{IL}	"L" input current $P6_0$~$P6_5$	V_I=0V			−5	μA
I_{IL}	"L" input current $P5_4$~$P5_7$	V_I=0V			−5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}	V_I=0V			−5	μA
I_{IL}	"L" input current $P5_2/INT_2$, $P5_3/INT_1$	V_I=0V			−5	μA
I_{IH}	"H" input current $P2_0$~$P2_7$, $P3_0$~$P3_7$	V_I=5V			5	μA
		V_I=12V			12	μA
I_{IH}	"H" input current $P6_0$~$P6_5$	V_I=5V			5	μA
I_{IH}	"H" input current $P5_4$~$P5_7$	V_I=5V			5	μA
		V_I=12V			12	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}	V_I=5V			5	μA
I_{IH}	"H" input current $P5_2/INT_2$, $P5_3/INT_1$	V_I=5V			5	μA
		V_I=12V			12	μA
I_{OL}	"L" output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$	V_P=V_{CC}−36V, V_{OL}=V_{CC}	150	500	900	μA
		V_P=V_{CC}−36V, V_{OL}=V_{CC}−36V			30	μA
V_{RAM}	RAM retention voltage	At clock stop	2		5.5	V
I_{CC}	Supply current	Output pins open (output OFF) V_P=V_{CC}, V_P=V_{SS} Input and I/O pins all at V_{SS} X_{IN}=4MHz (system operation)		3	6	mA
		Ditto (at wait mode)		1		mA
		X_{IN}−X_{OUT} stop X_{CIN}=32kHz (at system operation) all other conditions same as above.		60	200	μA
		Ditto (at wait mode)		40		μA
		Oscillation all stopped. (at STOP mode) T_a=25℃			1	μA
		Oscillation all stopped. (at STOP mode) T_a=70℃			10	μA

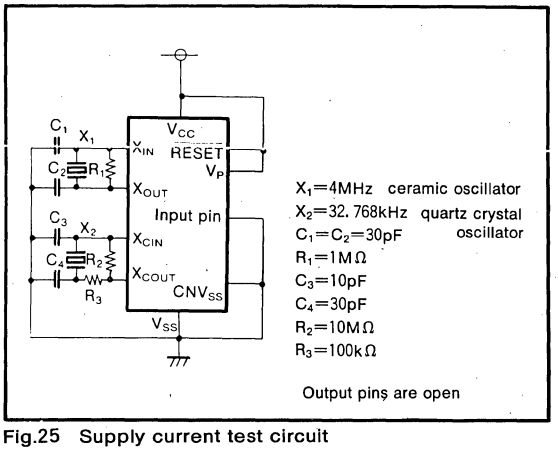


Fig.25 Supply current test circuit

TIMING REQUIREMENTS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input set-up time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input set-up time	270			ns
$t_{su(P5D-\phi)}$	Port $P5_2/INT_2$, $P5_3/INT_1$ input set-up time	270			ns
$t_{su(P5D-\phi)}$	Port $P5_{4-7}$ input set-up time	500			ns
$t_{su(P6D-\phi)}$	Port P6 input set-up time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port $P5_2/INT_2$, $P5_3/INT_1$ input hold time	20			ns
$t_{h(\phi-P5D)}$	Port $P5_{4-7}$ input hold time	50			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time	20			ns
$t_{C(X_{IN})}$	External clock input cycle time (X_{IN} input)	235			ns
$t_{W(X_{IN})}$	External clock input pulse width (X_{IN} input)	75			ns
$t_{C(X_{CIN})}$	External clock input cycle time (X_{CIN})	2.0			ms
$t_{W(X_{CIN})}$	External clock input pulse width (X_{CIN})	1.0			ms
t_r	External clock rise time			25	ns
t_f	External clock fall time			25	ns

Memory expanding mode and eva-chip mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input set-up time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Microprocessor mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25°C, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 27			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 26			230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time	Fig. 27			230	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time	Fig. 26			230	ns

Memory expanding mode and eva-chip mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25°C, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.26			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/\overline{W})}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-R/\overline{W}F)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns

Microprocessor mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25°C, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.26			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/\overline{W})}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

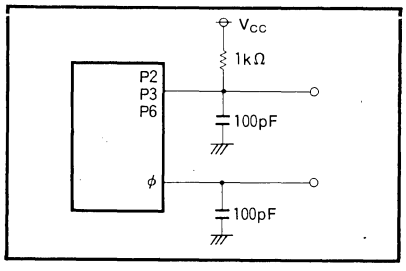


Fig.26 Port P2, P3, P6 test circuit

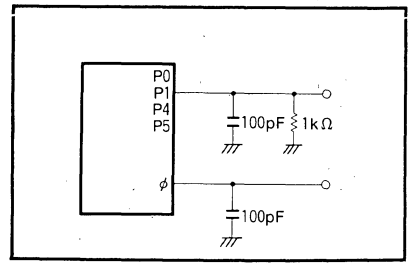
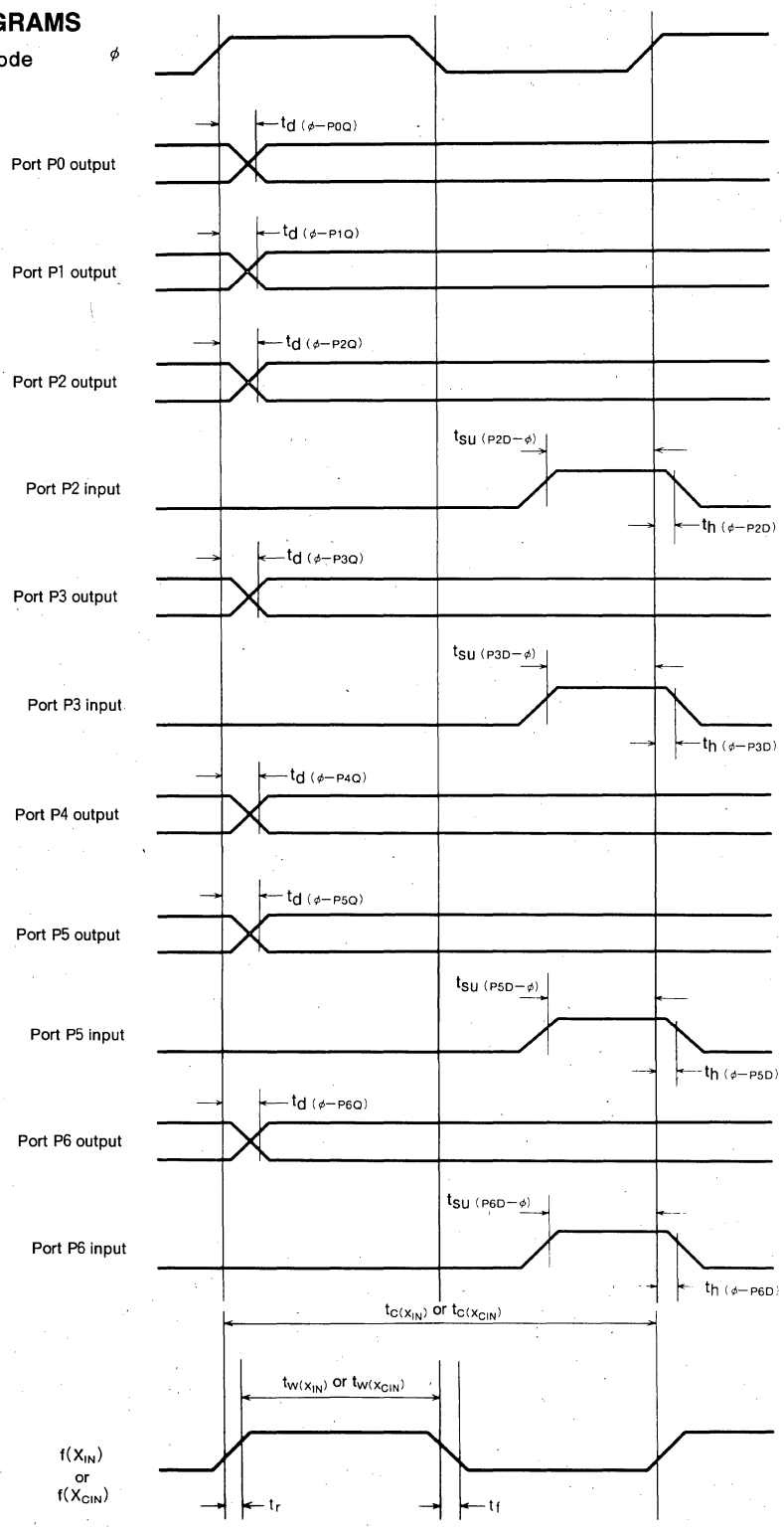


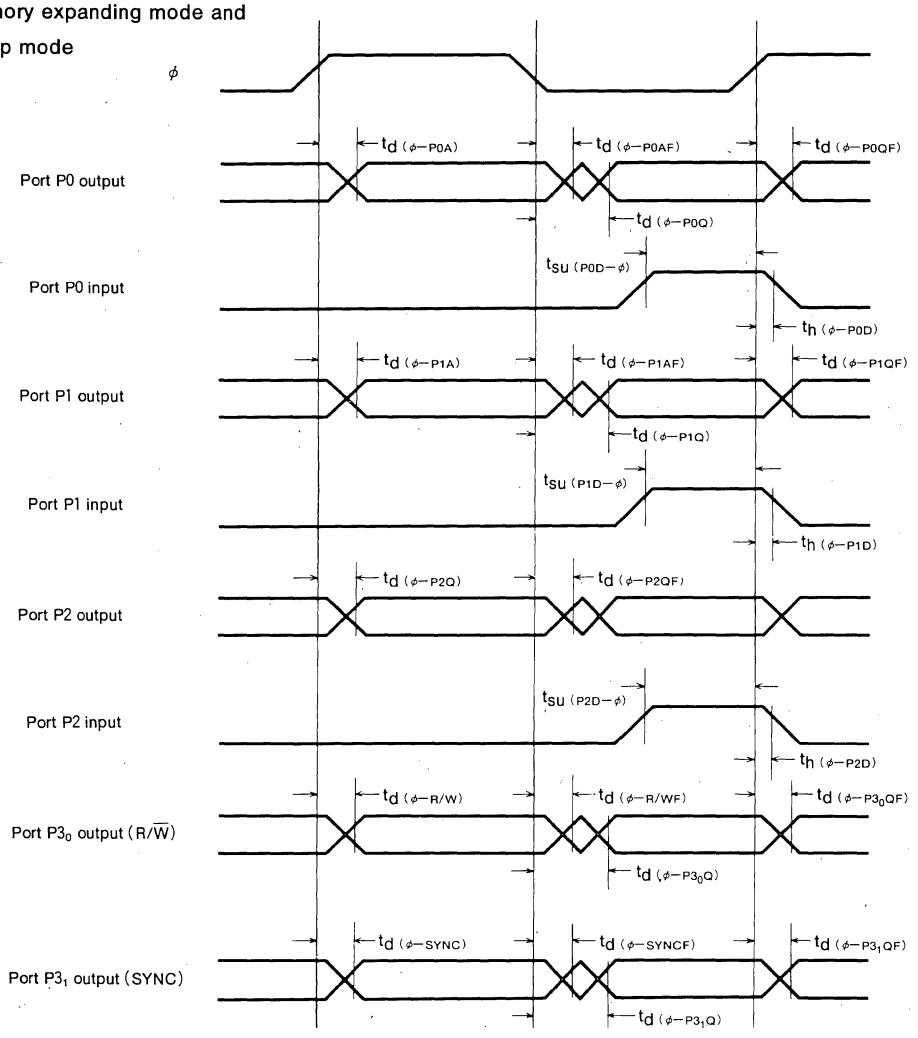
Fig.27 Port P0, P1, P4, P5 test circuit

TIMING DIAGRAMS

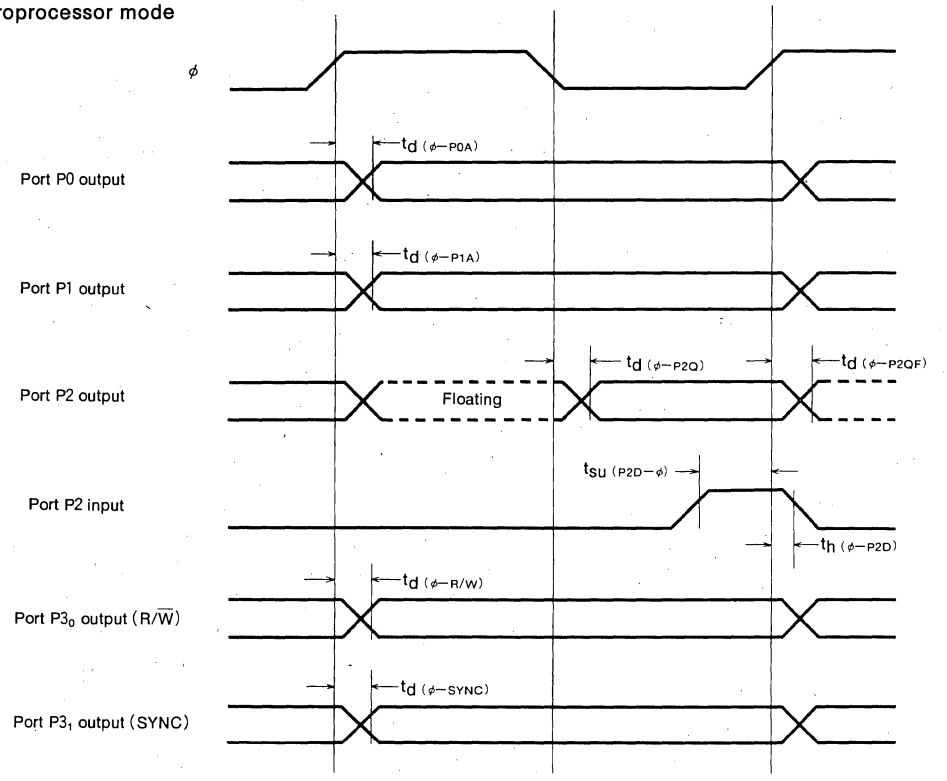
In single-chip mode



In memory expanding mode and
Eva-chip mode



In microprocessor mode



M50930-XXXFP, M50931-XXXFP M50932-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50930-XXXFP, M50931-XXXFP and the M50932-XXXFP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 80-pin plastic molded QFP. These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

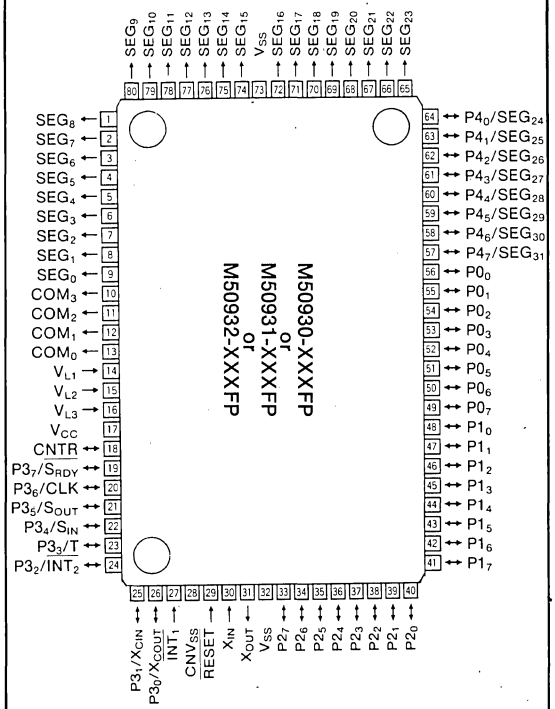
These microcomputers are also suitable for applications which require controlling LCDs.

The differences among the M50930-XXXFP, M50931-XXXFP and the M50932-XXXFP are noted below. The following explanations apply to the M50930-XXXFP. Specification variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M50930-XXXFP	4096 bytes	128 bytes
M50931-XXXFP	4096 bytes	512 bytes
M50932-XXXFP	8192 bytes	512 bytes

M50932-XXXFP only has pull-up transistor option for CNTR pin.

PIN CONFIGURATION (TOP VIEW)



Outline 80P6

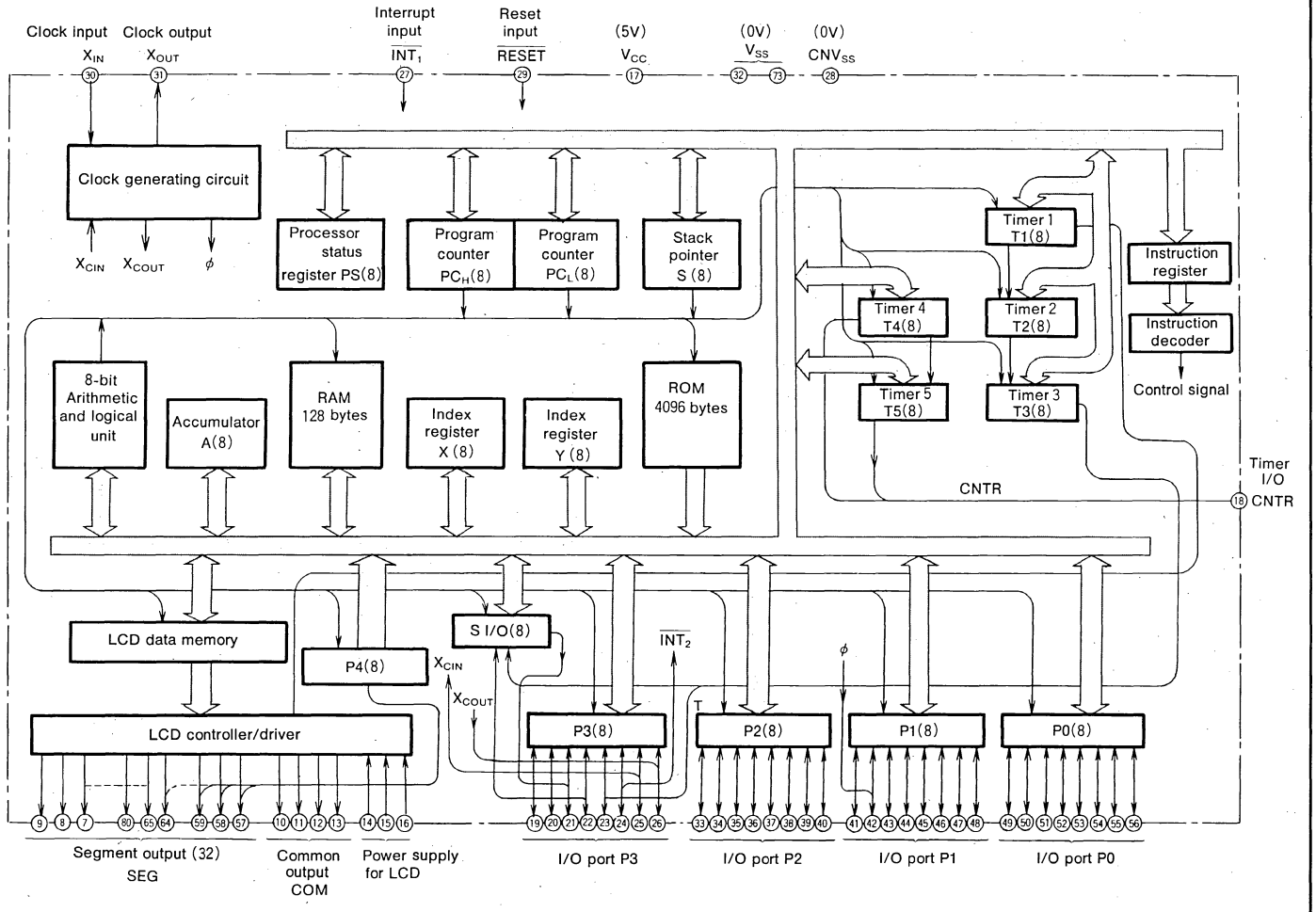
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size
  - ROM ... 4096 bytes (M50930-XXXFP, M50931-XXXFP)
    8192 bytes (M50932-XXXFP)
  - RAM ..... 128 bytes (M50930-XXXFP)
    512 bytes (M50931-XXXFP, M50932-XXXFP)
- Instruction executing time
  ..... 2μs (minimum instructions, at 4MHz frequency)
- Single power supply
  - f(X_{IN})=4MHz ..... 5V±10%
  - f(X_{IN})=1MHz ..... 2.7V ≦ V_{CC} ≦ 5.5V(Typ.)
- Power dissipation
  - normal operation mode (at 4MHz frequency)
    ..... 15mW(V_{CC}=5V, Typ.)
  - low-speed operation mode (at 32kHz frequency for clock function) ..... 225μW (V_{CC}=5V, Typ.)
  - stop mode(at 25℃) ..... 5μW (V_{CC}=5V, Max.)
- RAM retention voltage (stop mode)
  ..... 2.0V ≦ V_{RAM} ≦ 5.5V
- Subroutine nesting ..... 64 levels (Max.)
- Interrupt ..... 8 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as serial I/O)
- 16-bit timer ..... 1 (Two 8-bit timers make one set)
- Programmable I/O ports
  (Port P0, P1, P2, P3) 32
- Input ports (Port P4) 8
- Serial I/O (8-bit) 1
- LCD controller/driver (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty)
  - segment output 32
  - common output 4
- Two clock generator circuits (One is for main clock, the other is for clock function)

APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment
Telephone

M50930-XXXFP BLOCK DIAGRAM



Note 1 : Program counter PC_H is only 6 bits long.
2 : M50932 has 8192 bytes ROM.
3 : M50931 and M50932 have 512 bytes RAM.

MITSUBISHI ELECTRIC

FUNCTIONS OF M50930-XXXFP

Parameter			Functions
Number of basic instructions			69
Instruction excution time			2μs (minimum instructions, at 4MHz frequency).
Clock frequency			4.3MHz
Memory size	ROM		4096 bytes (8192 bytes for M50932-XXXFP)
	RAM		128 bytes (512 bytes for M50931-XXXFP and M50932-XXXFP)
	RAM for display LCD		16 bytes
Input/output port	P0, P1, P2, P3	I/O	8-bit×4
	P4	Input	8-bit×1 (Port P4 are in common with SEG)
	SEG	LCD output	32-bit×1
	COM	LCD output	4-bit×1
Serial I/O			8-bit×1
Timers			8-bit timer×3 (2 when serial I/O is used)
			16-bit timer×1 (combination of two 8-bit timers)
LCD controller/driver	Bias		1/2, 1/3 bias selectable
	Duty ratio		1/2, 1/3, 1/4 duty selectable
	Common output		4
	Segment output		32 (SEG_{24}~SEG_{31} are in common with port P4)
Subroutine nesting			64 (max.)
Interrupt			Two external interrupts, Three timer interrupts (or two timer, one serial I/O)
Clock generating circuit			Two built-in circuit (ceramic or quartz crystal oscillator)
Supply voltage			2.7~5.5V (RAM retention voltage at clock stop is 2~5.5V)
Power dissipation	At high-speed operation V_{CC}=5V		15mW (at clock frequency X_{IN}=4MHz, typ.)
	At low-speed operation V_{CC}=5V		225μW (at clock frequency X_{CIN}=32kHz, typ.)
	At STOP mode		5μW (at clock stop, max.)
Input/output characteristics	Input/output voltage		5V
	Output current		I_{OH}=−2mA (V_{OH}=3V)
			I_{OL}=10mA (V_{OL}=2V)
			Pull-up current : Min. −30μA, max. −140μA, typ −70μA (V_{CC}=5V input voltage 0V)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package			80-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connect to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$, $P3_2$, $P3_1$, and $P3_0$ work as timer 3 overflow signal divided by 2 output pin (T), $\overline{INT_2}$ pin, X_{CIN} and X_{COUT} pins, respectively.
$P4_0$~$P4_7$	Input port P4	I/O	Port P4 is an 8-bit input port and can be used as segment output pins.
V_{L1}~V_{L3}	Voltage input for LCD	Input	These are voltage input pins for LCD. Supply voltage as $0V \leqq V_{L1} \leqq V_{L2} \leqq V_{L3} \leqq V_{CC}$. 0V~$V_{L3}$ is supplied to LCD.
COM_0~ COM_3	Common output	Output	These are LCD common output pins. At 1/2 duty, COM_2 and COM_3 pins are not used. At 1/3 duty, COM_3 is not used.
SEG_0~ SEG_{23}	Segment output	Output	These are LCD segment output pins.
CNTR	Timer I/O	I/O	This is an output pin for the timer 4 and 5.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50930-XXXFP is shown in Figure 1. Address 3000_{16} to $3FFF_{16}$ are assigned for the built-in ROM area which consists of 4096 bytes (Addresses 2000_{16} to $3FFF_{16}$ are assigned for the built-in ROM area which consists of 8192 bytes for M50932-XXXFP). Addresses $3F00_{16}$ to $3FFF_{16}$ are a special address area (special page). By using the special page addressing mode of JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $3FF4_{16}$ to $3FFF_{16}$ are vector addresses used for the reset and interrupts (See interrupts chapter).

Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required.

The RAM, I/O port, timer, etc. addresses are already assigned for the zero page. Addresses 0000_{16} to $007F_{16}$ are assigned for the built-in RAM which consists of 128 bytes (Addresses 0000_{16} to $007F_{16}$ and 0100_{16} to $027F_{16}$ are assigned for the built-in RAM which consists of 512 bytes for M50931-XXXFP and M50932-XXXFP). This RAM is used as the stack during subroutine calls and interrupts, in addition to data storage.

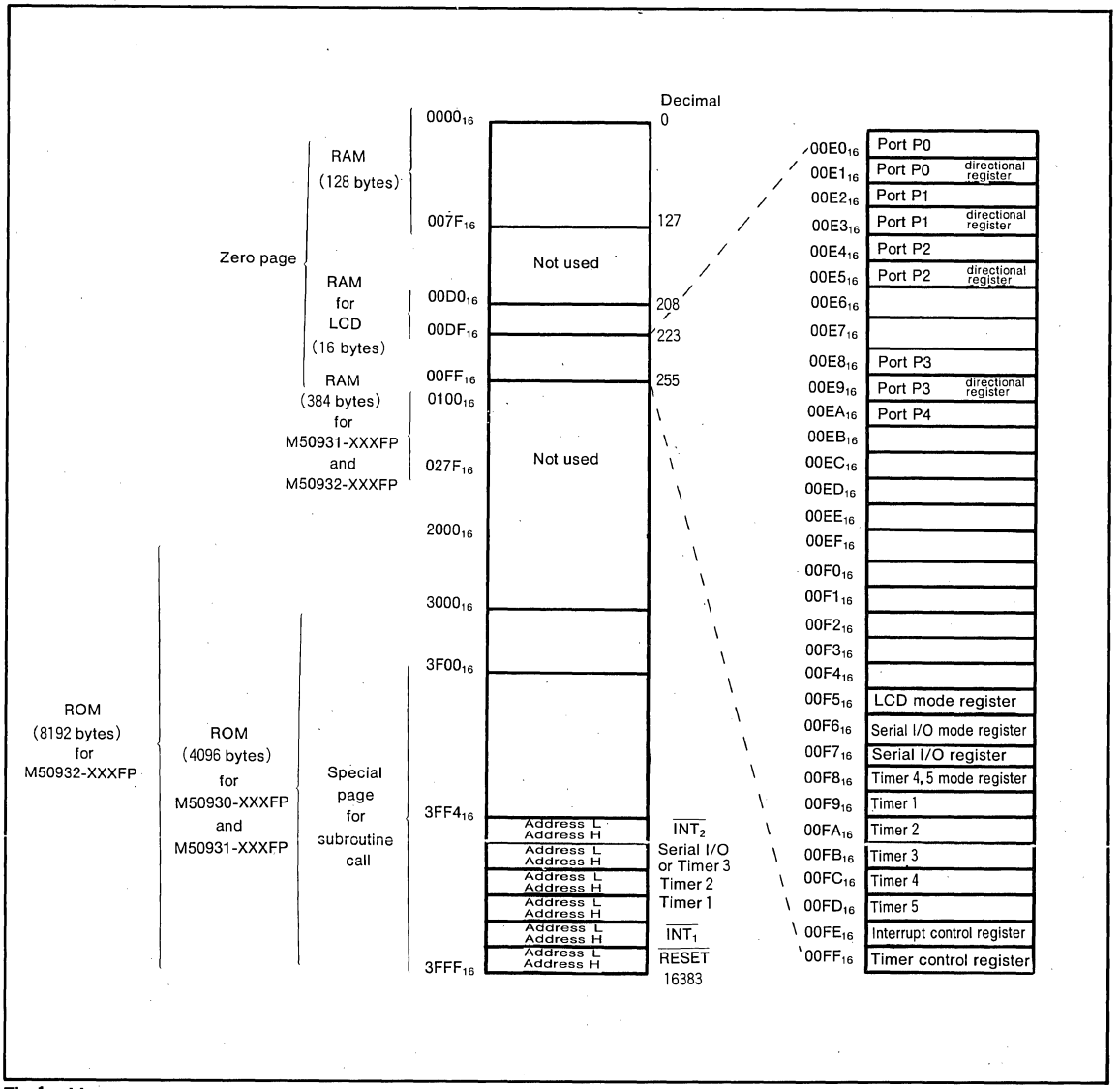


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, input/output, etc., is executed mainly through the accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register. In the index register X addressing mode, the value of the OPERAND added to the contents of the index register X specifies the real address. When the T flag in the processors status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register. In the index register Y addressing mode, the value of the OPERAND added to the contents of the index register Y specifies the real address.

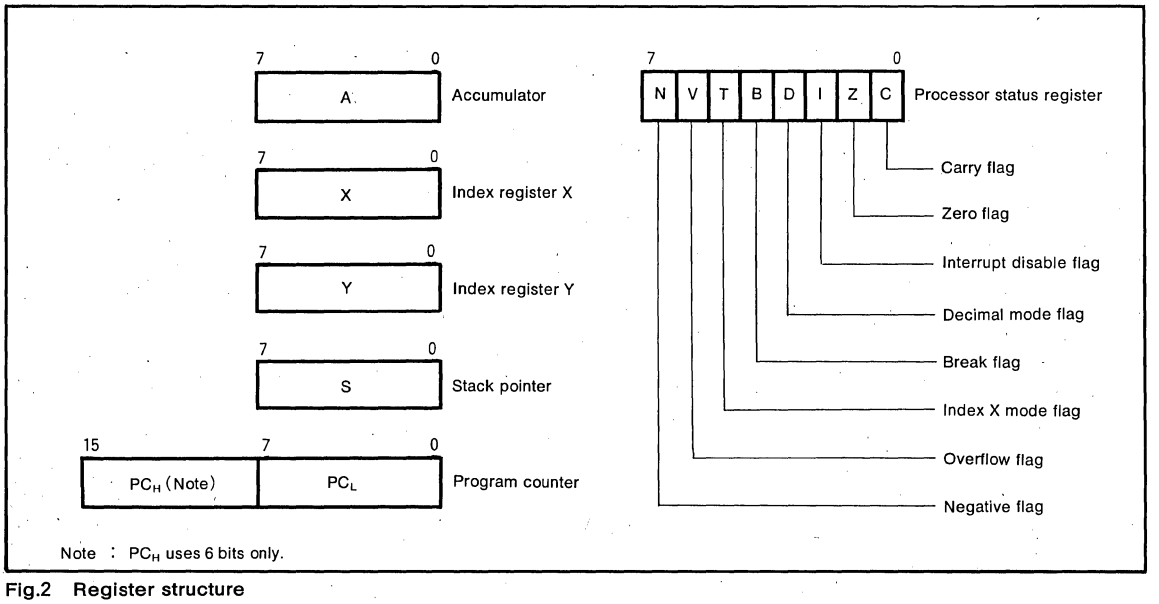


Fig.2 Register structure

STACK POINTER (S)

The stack pointer is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

When an interrupt occurs, the higher 8 bits of the program counter is pushed into the stack first, the stack pointer is decremented, and then the lower 8 bits of the program counter is pushed into the stack. Next the contents of the processor status register is pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter and processor status register data is popped off the stack in reverse order from above.

The accumulator is never pushed into the stack automatically, so a Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pop Accumulator instruction (PLA). It is executed in the reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed and popped to and from the stack with the PHP and PLP instructions, respectively.

During a subroutine call, only the Program Counter is pushed into the stack. Therefore, any registers that should not be destroyed should be pused into the stack manually. To return from a subroutine call, the RTS instruction is used.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PC_H is only 6 bits long.

PROCESSOR STATUS REGSITER (PS)

The 8-bit PS is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flags (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic Logic Unit (ALU) immediately after an operation. It is also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "0". If the result is not zero, the zero flag will be set to "1".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt is accepted, this flag is automatically set to "1" to prevent from other interrupts until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the B flag will be "1", otherwise, it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly, without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the T flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the V flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the N flag. There are no instructions for directly setting or resetting the N flag.

INTERRUPT

The M50930-XXXFP can be interrupted from eight sources; $\overline{INT_1}$, Timer 1, Timer 2, Timer 3 or Serial I/O, $\overline{INT_2}$ or Key on wake up, and BRK instruction.

The value of bit 2 of the serial I/O register (address $00F6_{16}$) determines whether the interrupt is from timer 3 or from serial I/O. When the bit 2 is "1" the interrupt is from serial I/O, and when bit 2 is "0" the interrupt is from timer 3. Also, when bit 2 is "1", parts of Port 3 are used for serial I/O. Bit 7 of the serial I/O register determines if an interrupt is from $\overline{INT_2}$ or from "Key on wake up". When bit 7 is "0", the interrupt is from $\overline{INT_2}$. When bit 7 is "1" the interrupt is from "key on wake up". "key on wake up" can only be used at power down by the STP or WIT instruction. These interrupts are vectored and thier priorities are shown in Table 1. Reset is included in this table since it has the same function as an interrupt.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, as discussed in the stack pointer section, and the interrupt disable flag (I) is set, and the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The Reset interrupt is the highest priority interrupt and can never be inhibited. Except for the Reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0". The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"
(2) When the levels any pin of P2 goes "L" (at power down mode)
(3) When the contents of timer 1, timer 2, timer 3 or the counter of serial I/O go to "0"

These request bits can be reset by a program but can not be set.

Since the BRK instruction interrupt and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

Table 1. Interrupt vector address and priority.

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$3FFF_{16}$, $3FFE_{16}$
$\overline{INT_1}$	2	$3FFD_{16}$, $3FFC_{16}$
Timer 1	3	$3FFB_{16}$, $3FFA_{16}$
Timer 2	4	$3FF9_{16}$, $3FF8_{16}$
Timer 3 or serial I/O	5	$3FF7_{16}$, $3FF6_{16}$
$\overline{INT_2}$ or key on wake up (BRK)	6	$3FF5_{16}$, $3FF4_{16}$

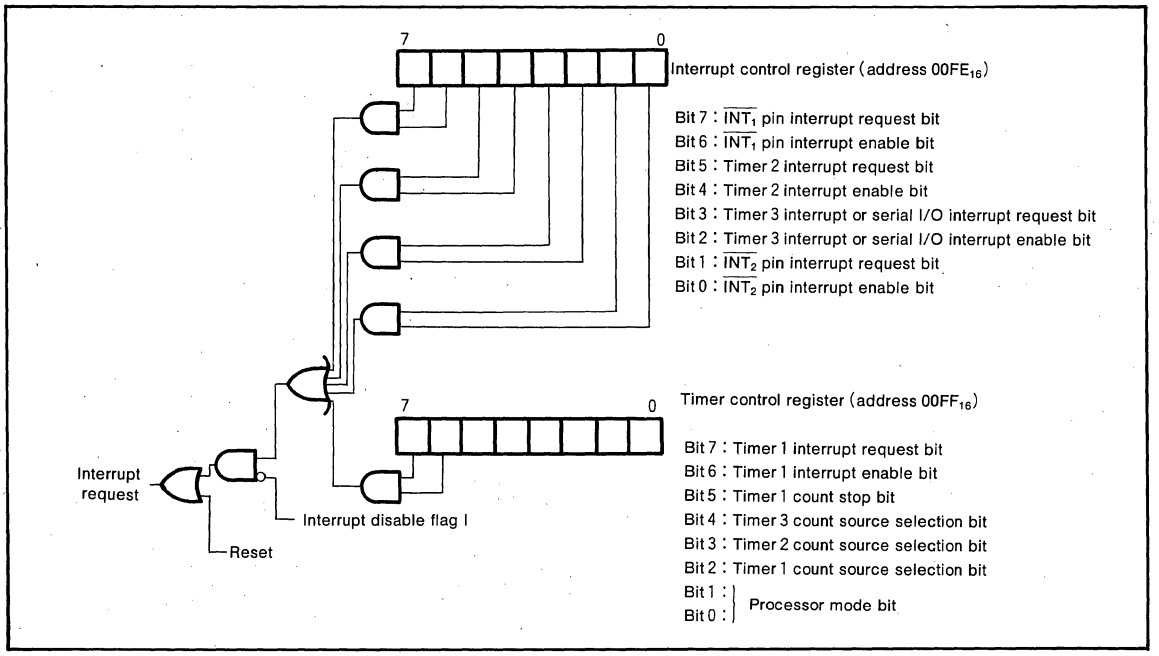


Fig. 3 Interrupt control

TIMER

The M50930-XXXFP has five timers; timer 1, timer 2, timer 3, timer 4 and timer 5. Timer 3 cannot be used when serial I/O is used (see serial I/O section). The count source for each timer can be selected by using bit 2, 3 and 4 of the timer control register (address $00FF_{16}$), as shown in Figure 4.

A block diagram of timer 1 through 5 is shown in Figure 6. All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timers is 1/(n +1), where n is the contents of timer latch.

The timer interrupt request bit is set at the next count pulse after the timer reaches "0". The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see Interrupt section). The starting and stopping of timer 1 is controlled by bit 5 of the timer control register. If bit 5 (address $00FF_{16}$) is "0", the timer starts counting. When bit 5 is "1", the timer stops.

After a STP instruction is executed, timer 2, timer 1, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 4 of the timer control register). This state is canceled if timer 2 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 1, count stop bit), bit 6 of the timer control register (timer 1 interrupt enable bit), and bit 4 of interrupt control register (timer 2 interrupt enable bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

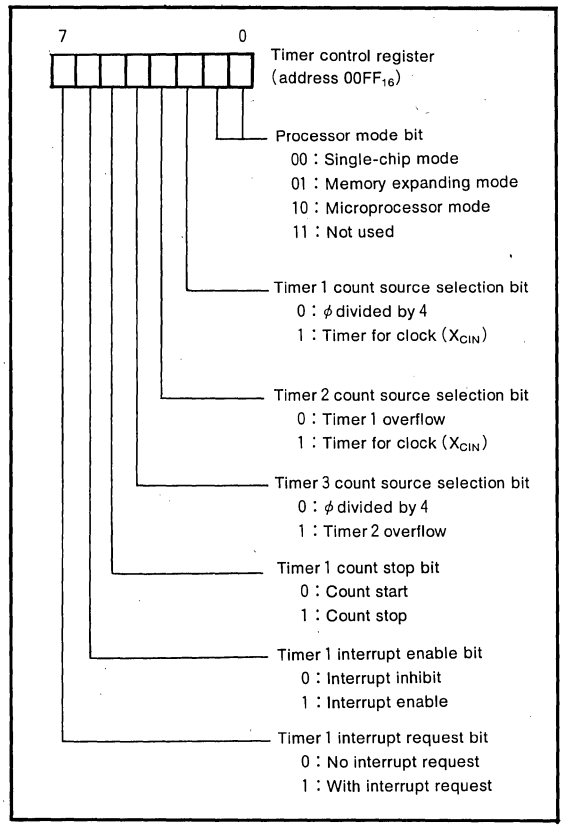


Fig.4 Structure of timer control register

TIMER 4 AND TIMER 5 MODES

(1) Timer Mode (00).
The internal clock divided by 4 is counted. When the timer counts to "0", the interrupt request bit is set to "1", the contents of the timer latch is reloaded, and the counting starts again.

(2) Pulse Output Mode (01).
The output level of the CNTR pin inverts each time the timer contents to zero.

(3) Event Counter Mode (10).
The same function is executed as that of mode "00", except that the counting source is input from the CNTR pin. The count decremented each time the CNTR input goes from "L" to "H".

(4) Pulse Width Measurement Mode (11).
This mode is used to measure the pulse width of a signal (between "L"s) input into the CNTR pin. The counting is done using the oscillation frequency divided by 4, and only while the CNTR pin is at a low level. When the contents of the counter reaches zero, the timer 5 overflow flag is set to "1", the timer is reloaded from the reload latch, and counting starts again. The overflow flag can be reset by writing a "0" to bit 7 of address $00F8_{16}$. The structure of timer 4, 5 mode register is shown in Figure 5.

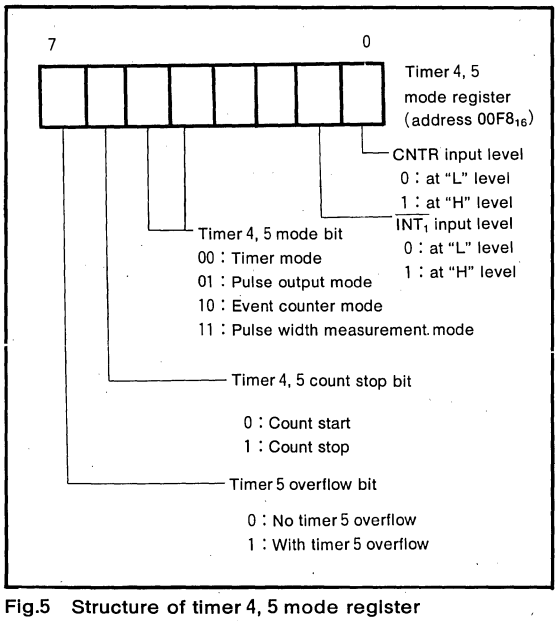


Fig.5 Structure of timer 4, 5 mode register

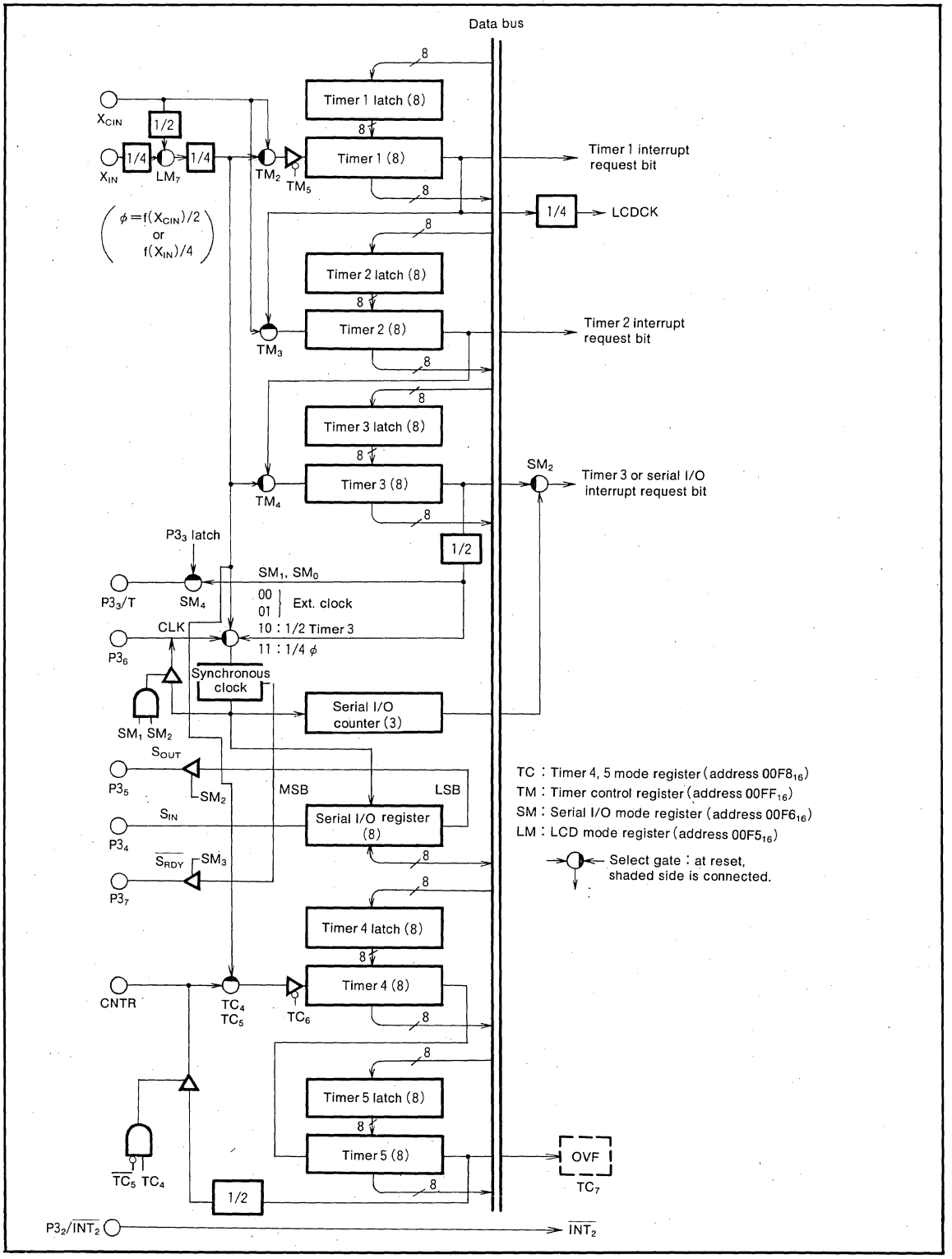


Fig.6 Block diagram of timers 1 through 5

PORT $P3_3$/TIMER 3 OUTPUT

The signal that timer 3 is divided by 2 is output from $P3_3$ (T), at the contents of bit 4 of the serial I/O mode register (address $00F6_{16}$) is "1".

WATCHDOG TIMER FUNCTION

Timer 4 and 5 can be used as a watchdog timer by connecting the CNTR pin and the $\overline{\text{RESET}}$ pin as shown in Figure 7, and by setting bit 4 and 5 of address $00F8_{16}$ to 01. At this time the output of the 1/2 divider counter (connected to timer 5) is initialized to "1" when data is written to timer 5. After a delay of 2.5 to 3.0μs (at $f(X_{IN})=4$MHz) after the reset is input, bits 4, 5, and 6 of the timer 4,5 mode register are initialized to 0. The initialization program to set the watchdog timer mode should have the following sequence:

(1) Set the pulse output mode after writing a value to timer 4 and 5 registers.

(2) If the program is running correctly, the CNTR pin should never go low due to data being continuously written to timer 5. If the program sequence is interrupted, timer 5 will overflow and the CNTR pin will output a "L" and retain this value until the Reset is executed.

(3) 2.5 to 3.5μs (at $f(X_{IN})=4$MHz) after a reset, the CNTR pin will be in high impedance state.

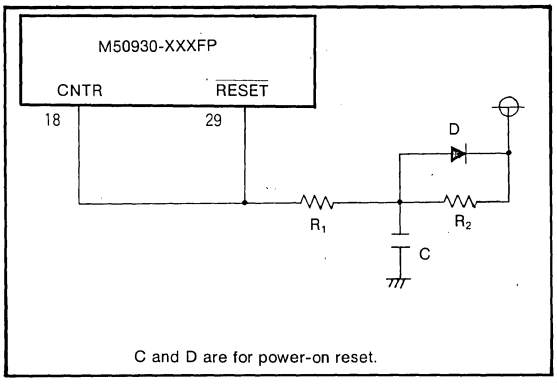


Fig.7 Reset circuit with the watchdog timer

SERIAL I/O

The block diagram of serial I/O is shown in Figure 8. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O (S_{OUT}, S_{IN}) pins are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively.

The serial I/O mode register (address $00F6_{16}$) is an 8-bit register. Bit 0 and 1 of this register is used to select a synchronous clock source. When these bits are (00) or (01), an external clock from $P3_6$ is selected. When these bits are (10), the overflow signal divided by two from timer 3 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are (11), the internal clock ϕ divided by 4 (ie. 4μs at 4MHz) becomes the clock.

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If the external synchronous clock is selected, the clock is input to $P3_6$. And $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0"

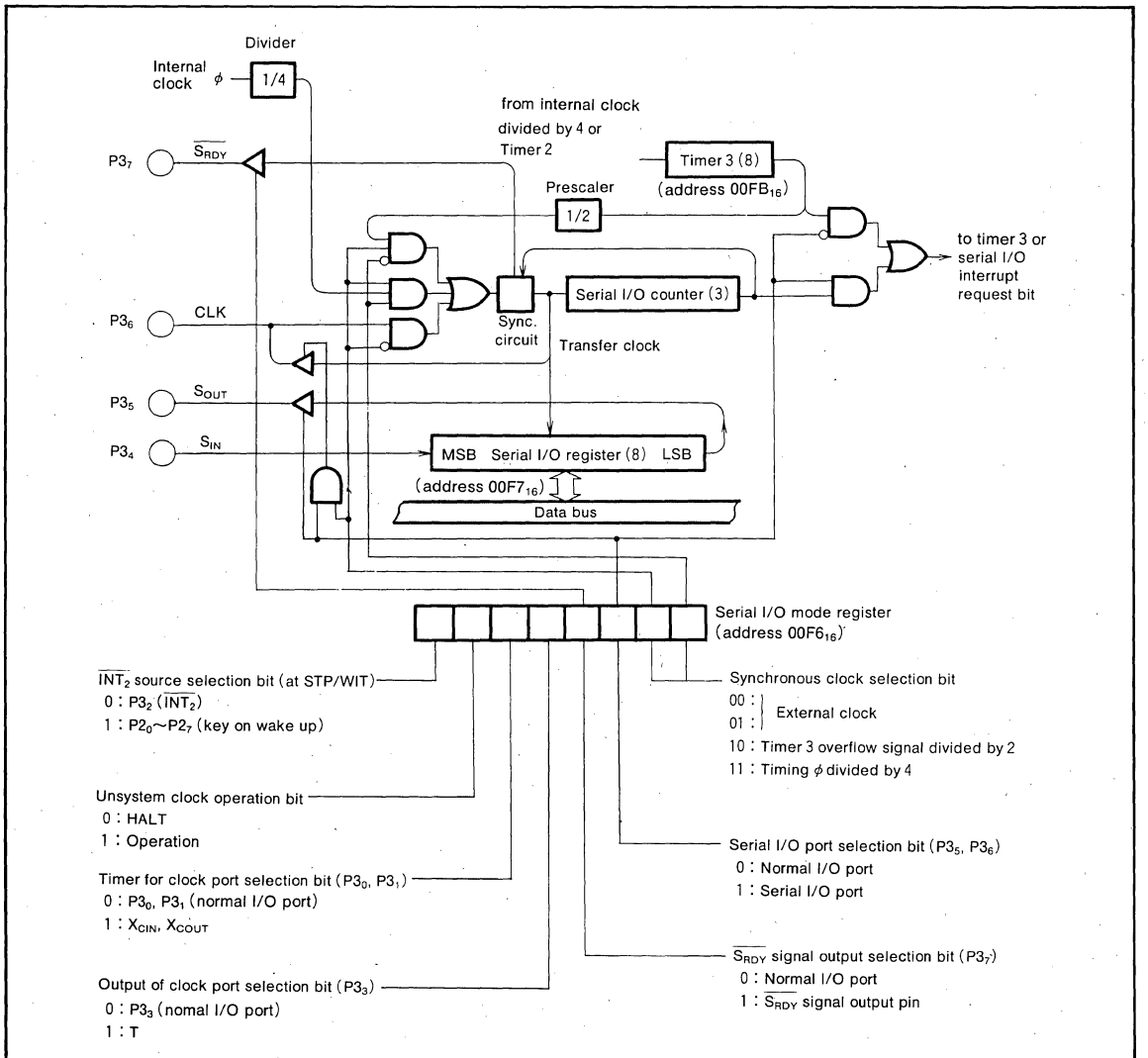


Fig.8 Block diagram of serial I/O

$P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 3. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDY}}$) or used as a nomal I/O pin (bit 3="0").

The function of serial I/O differs depending on the clock source: external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50930-XXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock—If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 9, and connection between two M50930-XXXFPs' are shown in Figure 10. When using an external clock for transfer, the external clock must be held at "H" level when the serial I/O counter is initialized. When switching between the internal clock and external clock, the switching must not be performed during transfer. Also, the serial I/O counter must be initialized after switching.

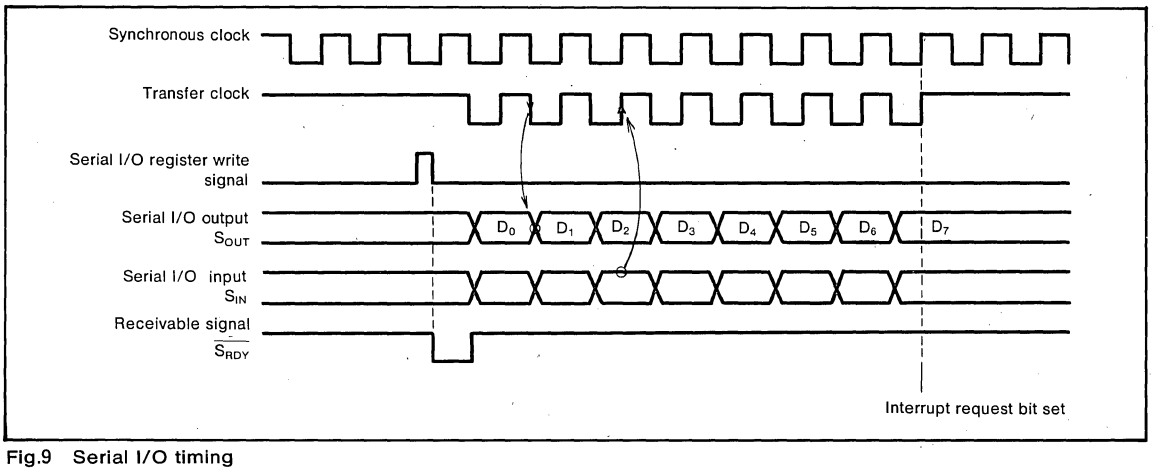


Fig.9 Serial I/O timing

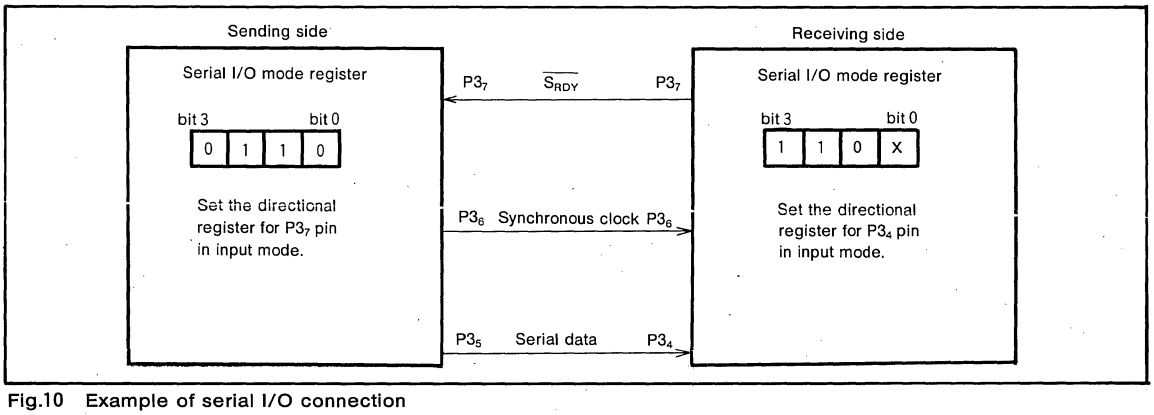


Fig.10 Example of serial I/O connection

LCD CONTROLLER/DRIVER

The M50930-XXXFP has internal LCD controllers and drivers. A Block diagram of LCD circuit is shown in Figure 13. The terminals for LCD consist of 4 common-pin and 32 segments pin. $SEG_{24} \sim SEG_{31}$ are in common with input P4. These pins are selected by bit 4 of the LCD mode register (LM_4, address $00F5_{16}$). Two biases (1/2 and 1/3) can also be selected. When bit 2 of the LCD mode register is "1", 1/2 bias is selected. When bit 2 is "0", 1/3 bias is selected. A 1/2, 1/3, or 1/4 duty cycle can also be selected. When bits 0 and 1 of the LCD mode register (LM_0, LM_1) is n, the duty ratio is 1/(n+1).

Address $00D0_{16} \sim 00DF_{16}$ is the designated RAM for the LCD display. When 1s' are written to these addresses, the corresponding segments of the LCD display panel are turned on. A map of the LCD display RAM is shown in Figure 12.

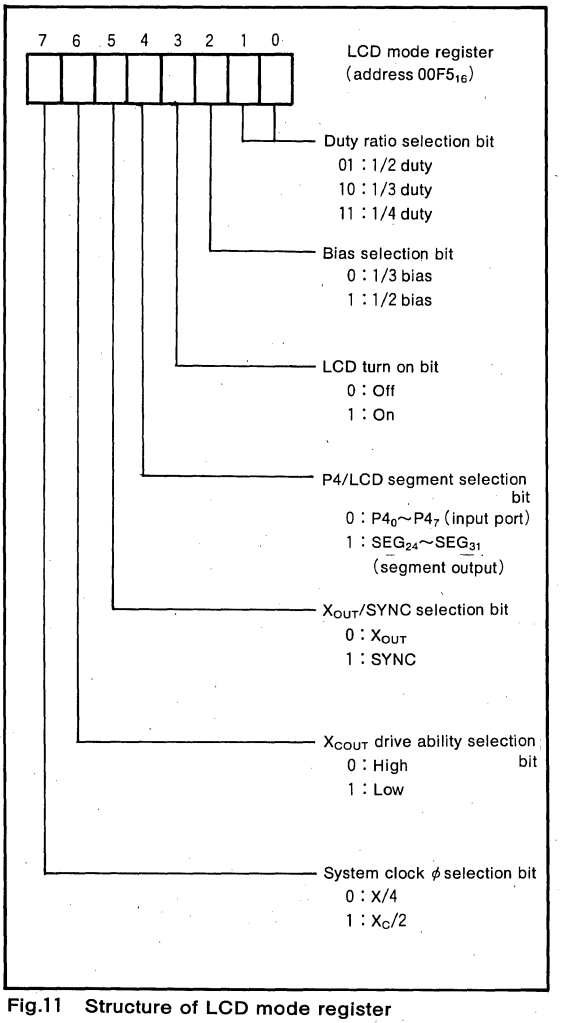


Fig.11 Structure of LCD mode register

The ON/OFF function for the LCD controller is controlled by bit 3 of the LCD mode register (LM_3). When this bit is "1" all the segments of the LCD are turned on. When this bit is "0" all the segments are turned off.

When a 1/2 bias is used, V_{L1} and V_{L2} should be shorted together. An example circuit for each bias is shown in Figure 14. Also Figure 15 shows an example of 1/2 bias, 1/4 duty drive waveforms and resulting voltage differential between SEG_n and COM_n and Figure 16 shows examples of drive waveforms for each bias and duty.

The LCDCK timing frequency (LCD driver timing) is generated internally and the frame frequency can be determined with the following equation:

$$f(LCDCK) = \frac{\text{(frequency of timer 1 count source)}}{((\text{timer 1 setting}+1)\times 4)}$$

$$\text{Frame frequency} = \frac{f(LCDCK)}{n}\text{; at 1/n duty}$$

Bit / Address	7	6	5	4	3	2	1	0
D0	1	1	1	1	0	0	0	0
D1	3	3	3	3	2	2	2	2
D2	5	5	5	5	4	4	4	4
D3	7	7	7	7	6	6	6	6
D4	9	9	9	9	8	8	8	8
D5	11	11	11	11	10	10	10	10
D6	13	13	13	13	12	12	12	12
D7	15	15	15	15	14	14	14	14
D8	17	17	17	17	16	16	16	16
D9	19	19	19	19	18	18	18	18
DA	21	21	21	21	20	20	20	20
DB	23	23	23	23	22	22	22	22
DC	25	25	25	25	24	24	24	24
DD	27	27	27	27	26	26	26	26
DE	29	29	29	29	28	28	28	28
DF	31	31	31	31	30	30	30	30
	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0

*Number in data memory area indicates corresponding segment.

Fig. 12 Map of RAM for LCD segment

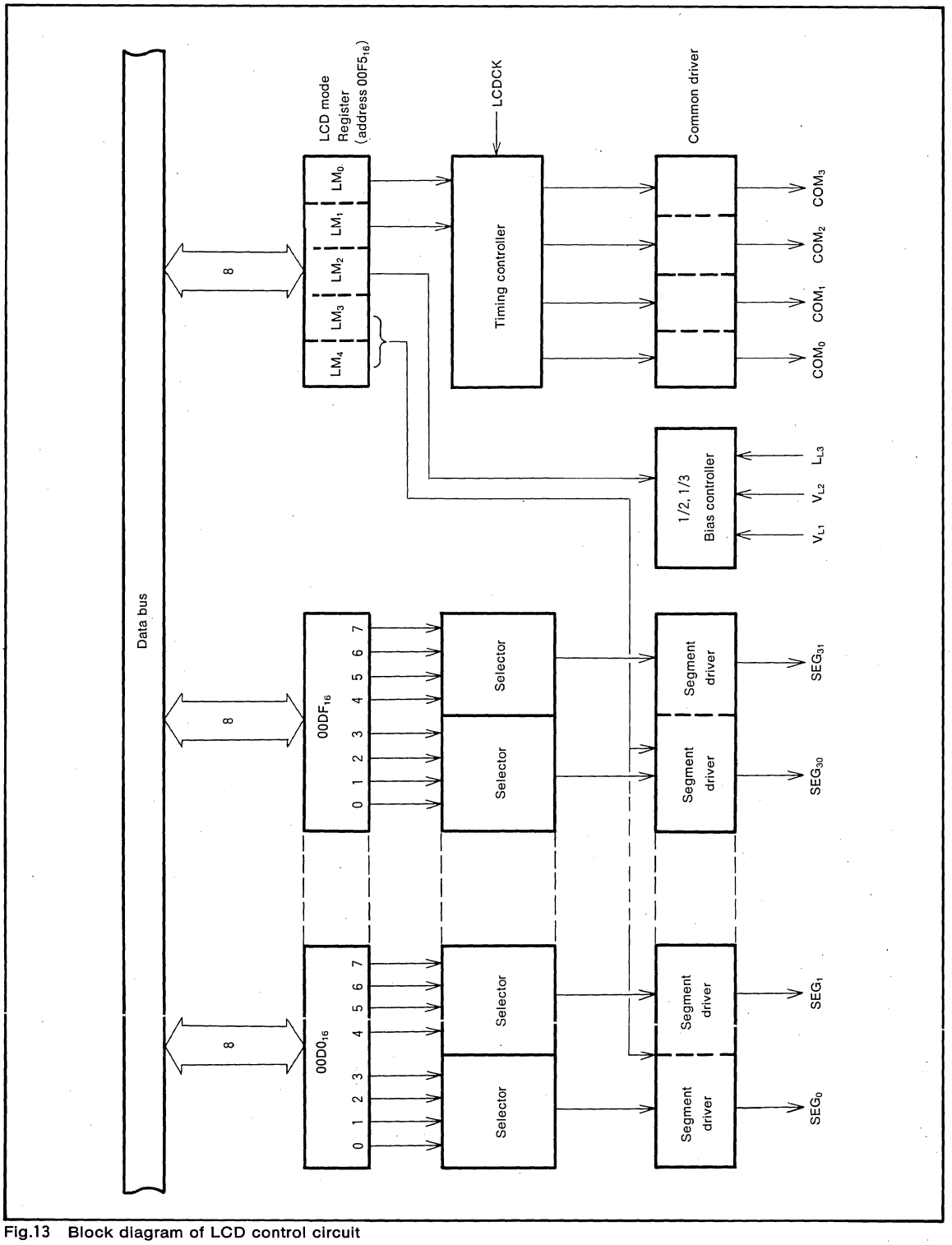


Fig.13 Block diagram of LCD control circuit

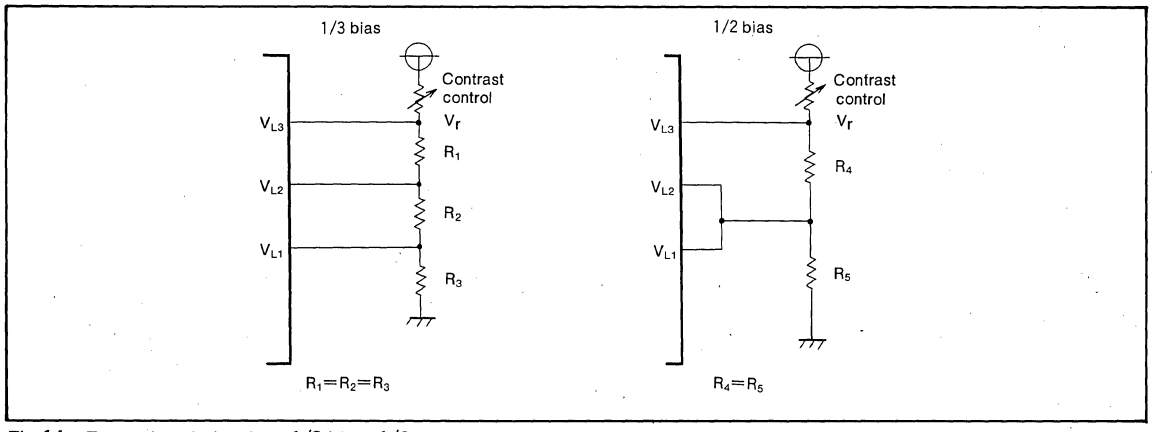


Fig.14 Example of circuit at 1/3 bias, 1/2 bias

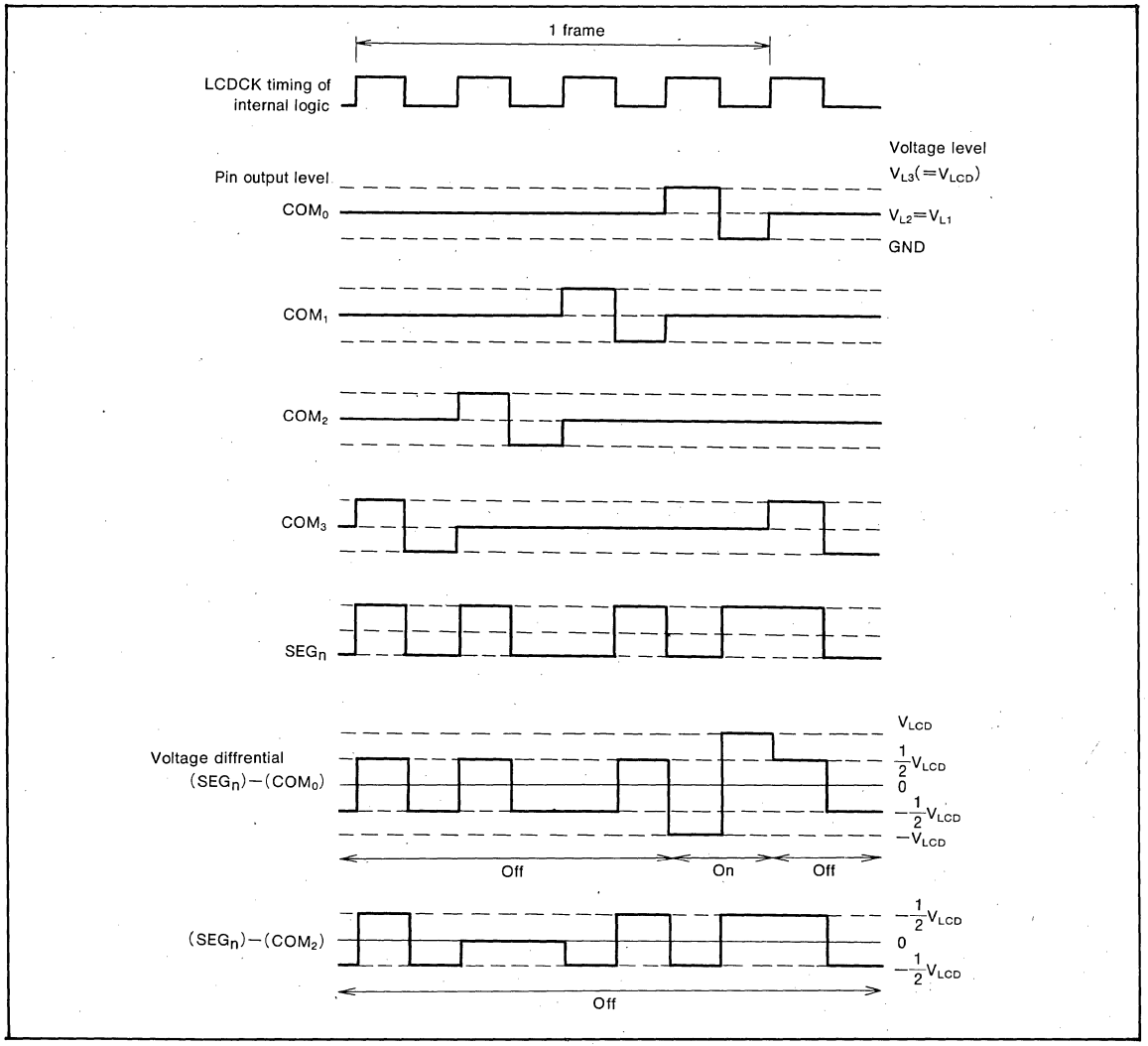


Fig.15 Example of 1/2 bias, 1/4 duty waveforms and resulting voltage differential between SEG_n and COM_n.

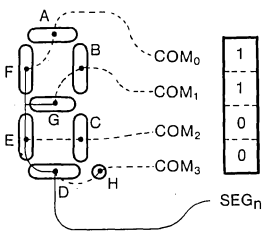
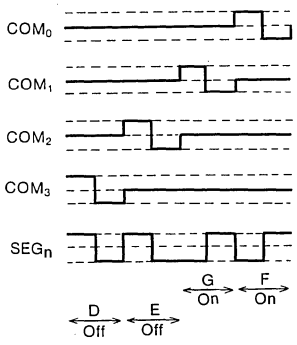
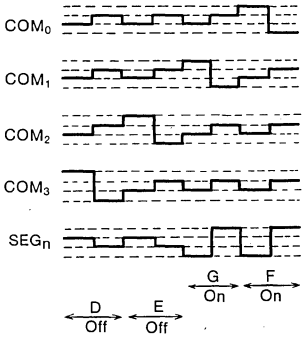
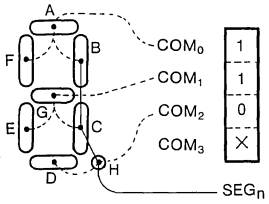
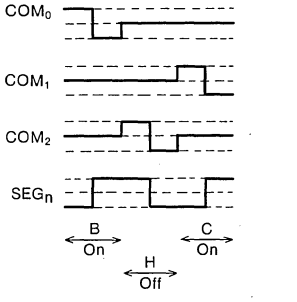
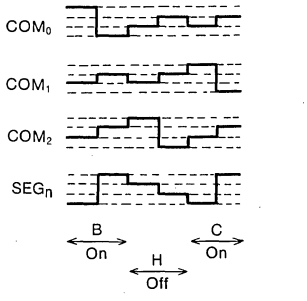
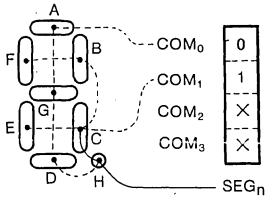
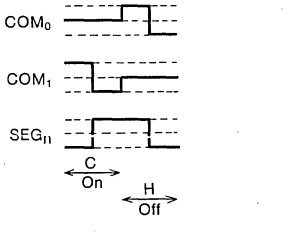
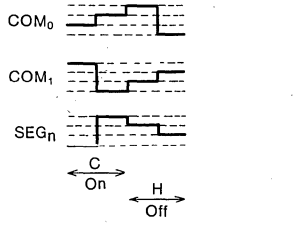
Bias / Duty	Display pattern: Connection	Display pattern: LCD RAM	1/2 bias	1/3 bias
			LCDCK timing of internal logic	LCDCK timing of internal logic
1/4 duty				
Maximum number of display segments	128(32 segments×4 commons) (16 digits max. in the above panel)			
1/3 duty	 COM3 : No connection			
Maximum number of display segments	96(32 segments×3 commons) (10 digits max. in the above panel)			
1/2 duty	 COM2, COM3 : No connection			
Maximum number of display segments	64(32 segments×2 commons) (8 digits max. in the above panel)			

Fig.16 Example of drive waveforms for each bias and duty

KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P2 has a "L" level applied, after bit 7 of the serial I/O mode register (SM_7) is set to "1", an interrupt is generated and the microcomputer is returned to the nomal operatinge state. As shown in Figure 17, a key matrix can be connected to port P2 and the microcomputer can be returned to a normal state by pushing any key.

The key on wake up interrupt is common with the $\overline{INT_2}$ interrupt. When SM_7 is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and $\overline{INT_2}$ are invalid.

In order to enter the power down state generated by the STP or WIT instruction at the interrupt disable flag (I) is "0" and SM_7 is "1", all of port P2 must be input "H".

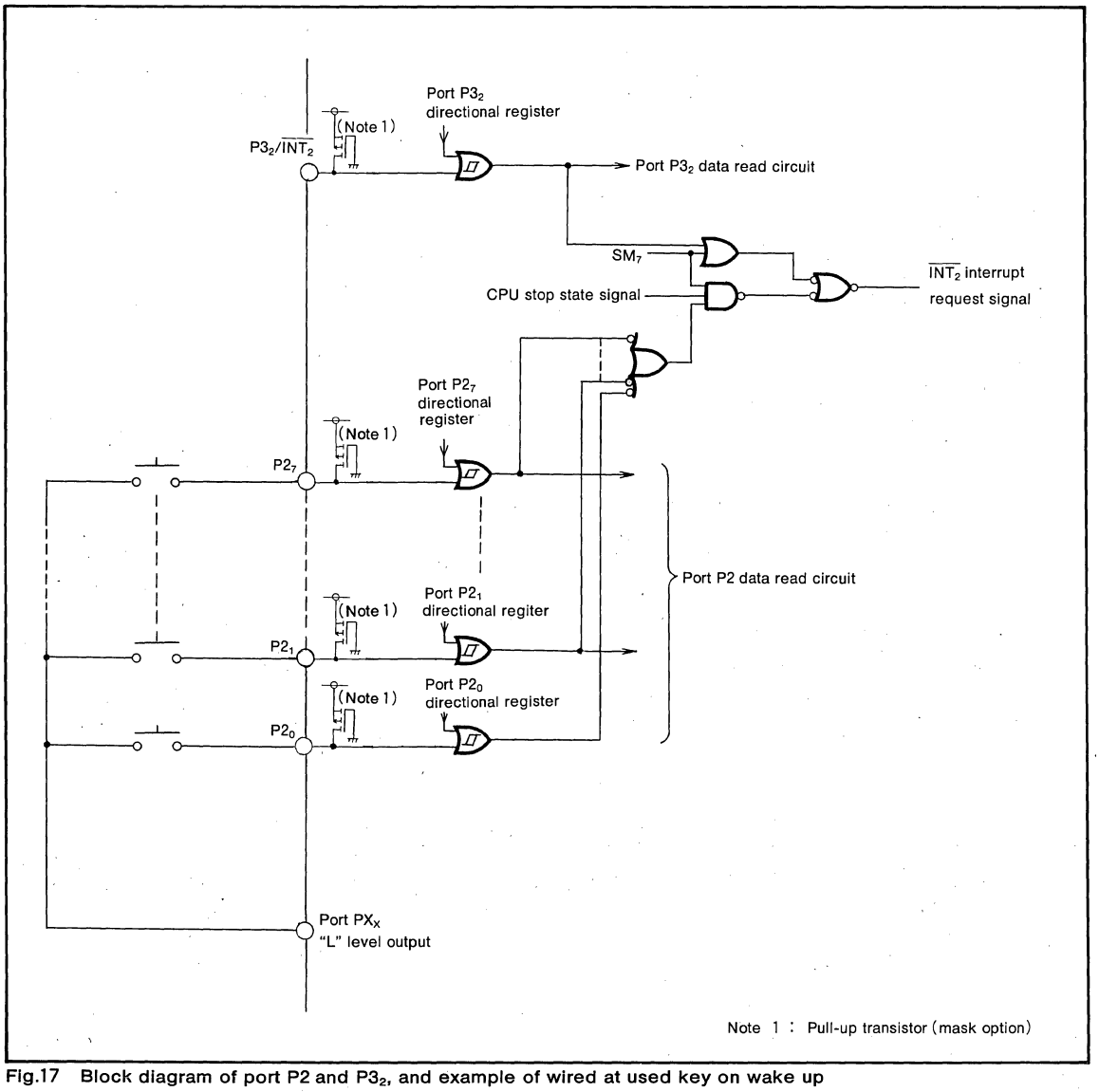


Fig.17 Block diagram of port P2 and $P3_2$, and example of wired at used key on wake up

RESET CIRCUIT

The M50930-XXXFP is reset according to the sequence shown in Figure 20. It starts the program from the address formed by using the content of address $3FFF_{16}$ as the high order address and the content of the address $3FFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for at least 8 rising edges from X_{IN} while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 18.

An example of the reset circuit is shown in Figure 19.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

		Address	
(1)	Port P0 directional register	($E1_{16}$)	00_{16}
(2)	Port P1 directional register	($E3_{16}$)	00_{16}
(3)	Port P2 directional register	($E5_{16}$)	00_{16}
(4)	Port P3 directional register	($E9_{16}$)	00_{16}
(5)	LCD mode register	($F5_{16}$)	00_{16}
(6)	Serial I/O mode register	($F6_{16}$)	00_{16}
(7)	Timer 4, 5 mode register	($F8_{16}$)	0 0 0 0
(8)	Interrupt control register	(FE_{16})	00_{16}
(9)	Timer control register	(FF_{16})	00_{16}
(10)	Interrupt disable flag for processor status register	(PS)	1
(11)	Program counter	(PC_H)	Contents of address $3FFF_{16}$
		(PC_L)	Contents of address $3FFE_{16}$

Since the contents of both registers other than those listed above (including timers and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values.

Fig.18 Internal state of microcomputer at reset

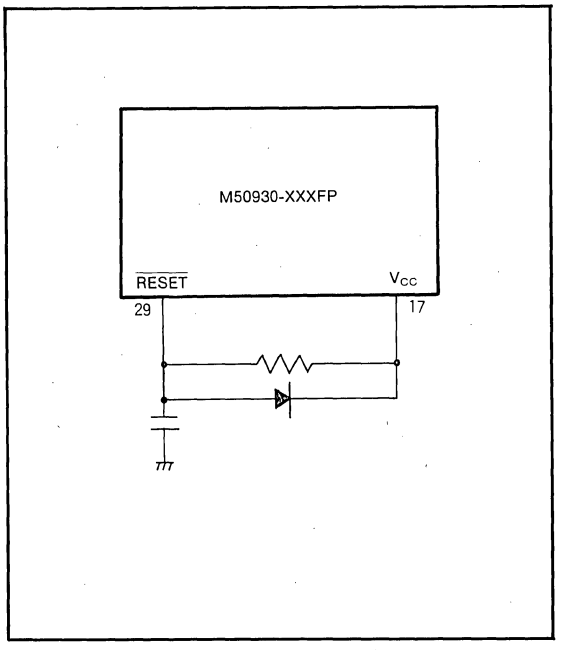
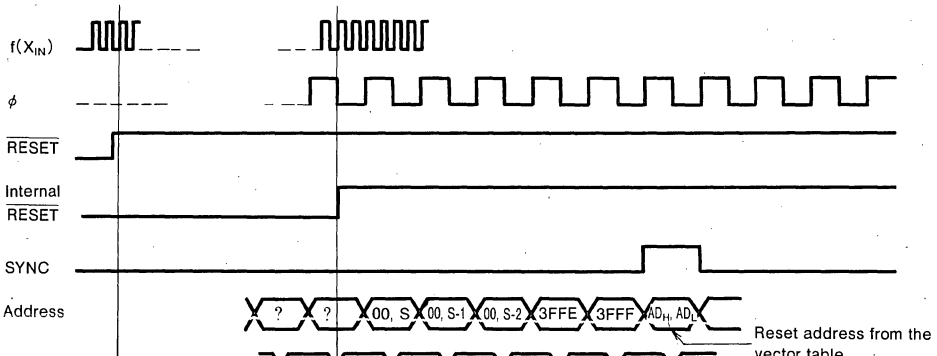


Fig.19 Example of reset circuit



Note 1 : Frequency relation of $f(X_{IN})$ and ϕ is $f(X_{IN}) = 4 \cdot \phi$.
Note 2 : The mark "?" means that the address is changeable depending upon the previous state.

Fig.20 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs and pull-up transistor options available. As shown in Figure 1, P0 can be accessed as memory through zero page address $00E0_{16}$. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address $00E1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port register and output. When data is read from the output port, the output pin level is not read, only the latched data of the port register is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

Depending on the status of the processor status bits (bit 0 and bit 1 of address $00FF_{16}$), three different modes can be selected; single-chip mode, memory expanding mode and microprocessor mode. For more details, refer to the timing diagram shown in Figure 24.

(2) Port P1

In the single chip mode, Port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's. For more details, see the processor mode information. Following the execution of STP or WIT instruction, P2 can be used to generate the "wake up mode". This mode is used to bring the microcomputer back in its normal operating mode after being in the power- down mode.

(4) Port P3

Port P3 has the same functions as P0 except that part of P3 is common with the serial I/O lines (ie. output of timer 3, input/output of timer clock, and interrupt input).

(5) Segment Output (SEG_0~SEG_{23})

These ports drive and control the LCD segments.

(6) Port P4

Port P4 is an 8-bit input port which can be used as a LCD segment output port.

(7) Common output (COM_0~COM_3)

These port provides output drive and control for the LCD common lines.

(8) Power Supply for LCD. (V_{L1}~V_{L3})

Supplies power to the LCD terminals.

(9) $\overline{INT_1}$

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 7 of address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L". This input level is read into bit 1 of the timer 4 and 5 mode register (address $00F8_{16}$).

(10) $\overline{INT_2}$ ($\overline{INT_2}$/$P3_2$)

The $\overline{INT_2}$ pin is an interrupt input pin common with $P3_2$. When $P3_2$'s directional register is set for input ("0"), this pin can be used as an interrupt input. The $\overline{INT_2}$ interrupt request bit (bit 1 of address $00FE_{16}$) is automatically set to "1" when the input level of this pin changes from "H" to "L".

(11) CNTR

The CNTR pin is an I/O pin of timers 4 and 5. The input level is read into bit 0 of the timer 4 and 5's mode register (address $00F8_{16}$).

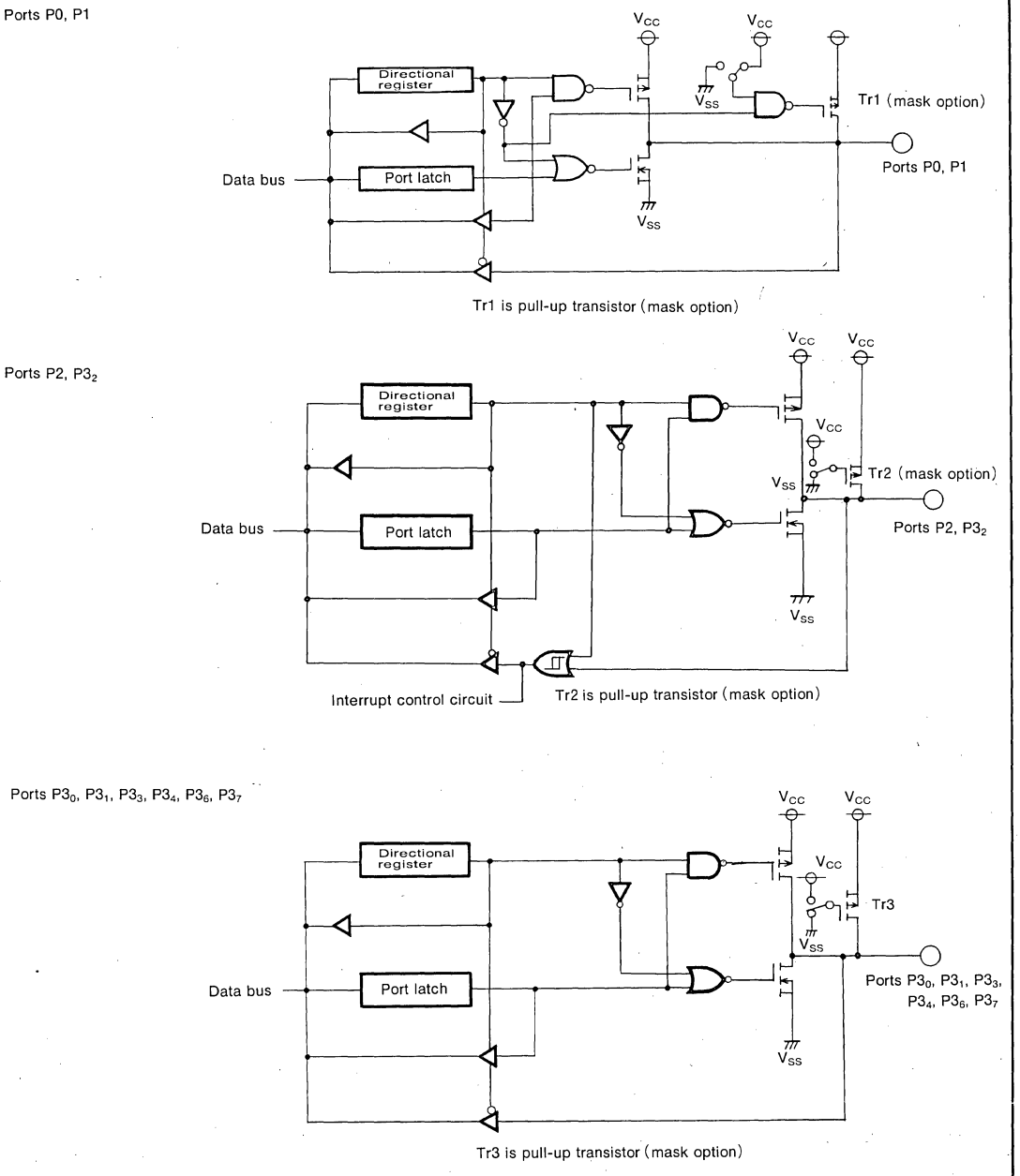


Fig.21 Block diagram of ports P0~P3

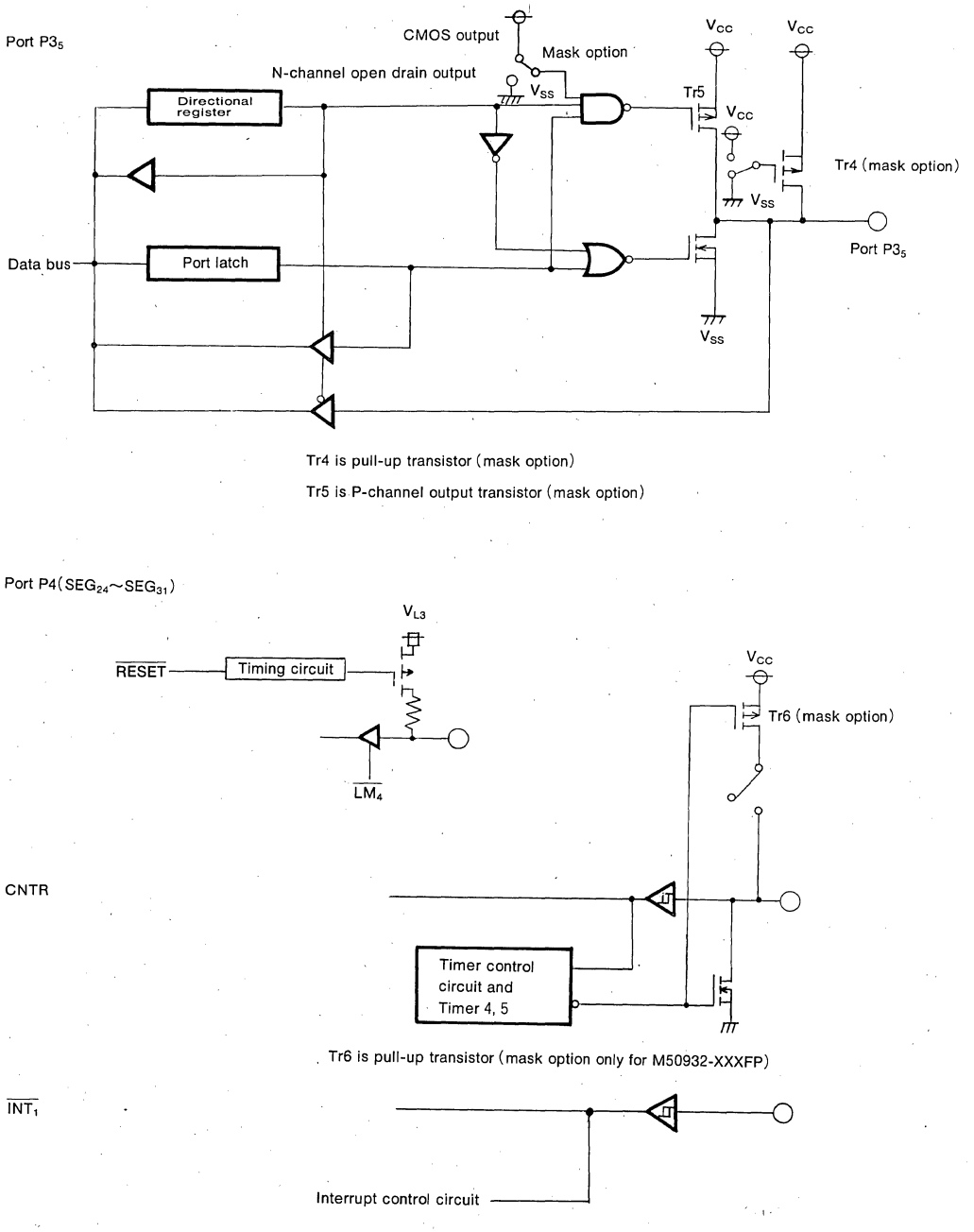
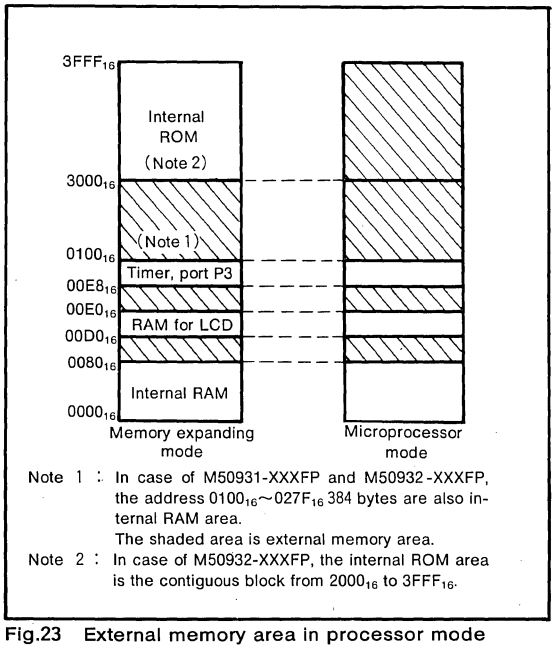


Fig.22 Block diagram of ports P3, P4, CNTR, and $\overline{INT_1}$

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 of address $00FF_{16}$), three different operation modes can be selected; single-chip mode, memory expanding mode and microprocessor mode. In the memory expanding mode and microprocessor mode, ports P0~P2 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports. The function of the X_{OUT} pin can also be changed. For more details see Figure 24.

The memory map of the single-chip mode is illustrated in Figure 1, and the other modes are shown in Figure 23. By connecting the CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode register. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. The three different modes are explained as follows:



Note 1 : In case of M50931-XXXFP and M50932-XXXFP, the address 0100_{16}~$027F_{16}$ 384 bytes are also internal RAM area.
The shaded area is external memory area.

Note 2 : In case of M50932-XXXFP, the internal ROM area is the contiguous block from 2000_{16} to $3FFF_{16}$.

Fig.23 External memory area in processor mode

(1) Single-chip mode [00]
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0~P2 will work as original I/O ports.

(2) Memory expanding mode [01]
The microcomputer will be changed to the memory expanding mode if CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient. Ports P0 and P1 are used as address output with the original I/O function lost. Port P2 is used as D_7~D_0 data I/O with the original I/O function lost. Port $P1_7$ and $P1_6$ works as R/$\overline{W}$ and ϕ.

(3) Microprocessor mode [10].
After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode. This mode is the same as the memory expanding mode except that the internal ROM is disable and external ROM is needed. The relationship between the input level of the CNV_{SS} and the processor mode is shown in Table 2.
The SYNC signal is output from the X_{OUT} pin in every mode except the single-chip mode, when 10V is supplied to the $\overline{RESET}$ pin or when bit 5 of the LCD mode register is set to "1". The SYNC signal becomes a synchronous signal that goes to "H" level while the Op code is being fetched. When the SYNC output signal is selected, the original function of the X_{OUT} pin is lost. In addition, if LM_7=1 and SM_6=0, the SYNC signal is not output from the X_{OUT} pin.

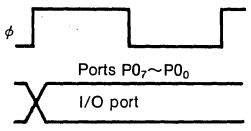
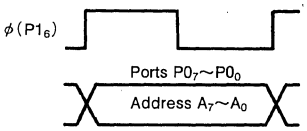
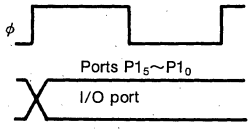
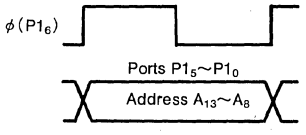
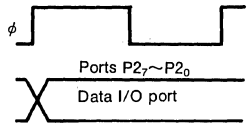
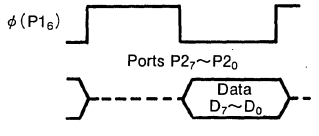
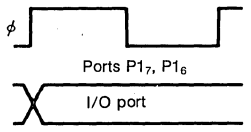
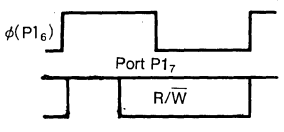
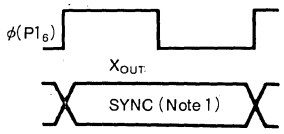
Port \ Mode	TM_1 / TM_0	Single-chip mode	Memory expanding mode	Microprocessor mode
	TM_1	0	0	1
	TM_0	0	1	0
Port P0				Same as left
Port P1 lower 6 Bits				Same as left
Port P2				Same as left
Port P1 higher 2 bits				Same as left
X_{OUT}				Same as left

Fig.24 Processor mode and functions of ports P0~P2 and X_{OUT}

Note 1 : In order to use X_{OUT} pin as SYNC output, put $\overline{RESET}$ to 10V or set bit 5 of the address $00F5_{16}$ to "1".

When LM_7=1 and SM_6=0, X_{OUT} does not output SYNC.

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Microprocessor mode	The microprocessor mode is set by the reset.

CLOCK GENERATING CIRCUIT

The M50930-XXXFP has two internal clock generating circuit. Figure 27 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ. Bit 7 of LCD mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 25 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacture's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input form the $X_{IN}(X_{CIN})$ pin and leave the $X_{OUT}(X_{COUT})$ pin open. A circuit example is shown in Figure 26.

The M50930-XXXFP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 1 and timer 2 are forcibly connected and $\phi/4$ is selected as timer 1 input. Before executing the STP instruction, appropriate values must be set in timer 1 and timer 2 to enable the oscillator to stabilize when restarting oscillation. Before executing the STP instruction, the timer 1 count stop bit must be set to supply ("0"), timer 1 interrupt enable bit and timer 2 interrupt enable bit must be set to disable ("0"), and timer 2 interrupt request bit must be set to no request ("0").

Oscillation is resarted (release the stop mode) when INT_1, INT_2, or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 2 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the $\overline{RESET}$ pin until the oscillattion stabilizes because no wait time is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock (45μA Typ. at $f(X_{CIN})=32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of LCD mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 28 shows the transition of states for the system clock.

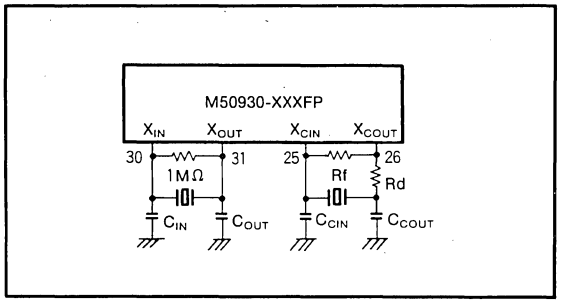


Fig.25 External ceramic resonator circuit

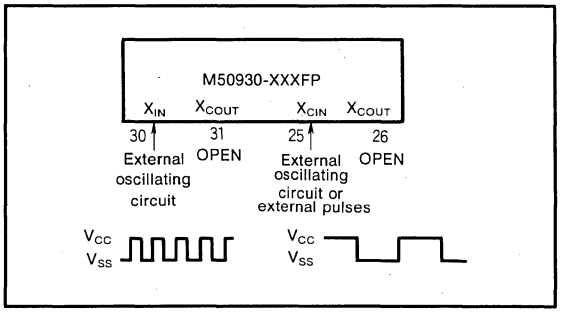


Fig.26 External clock input circuit

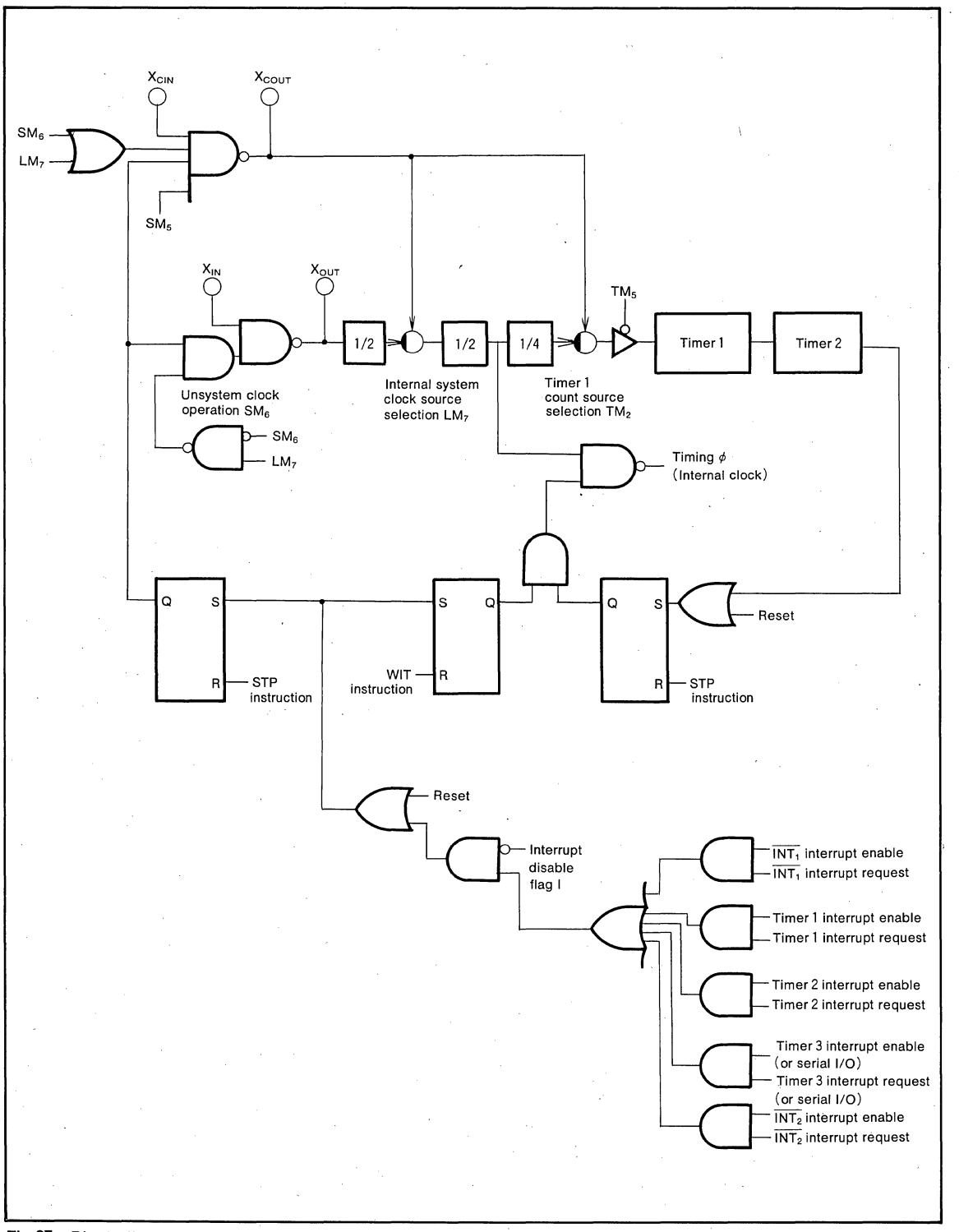
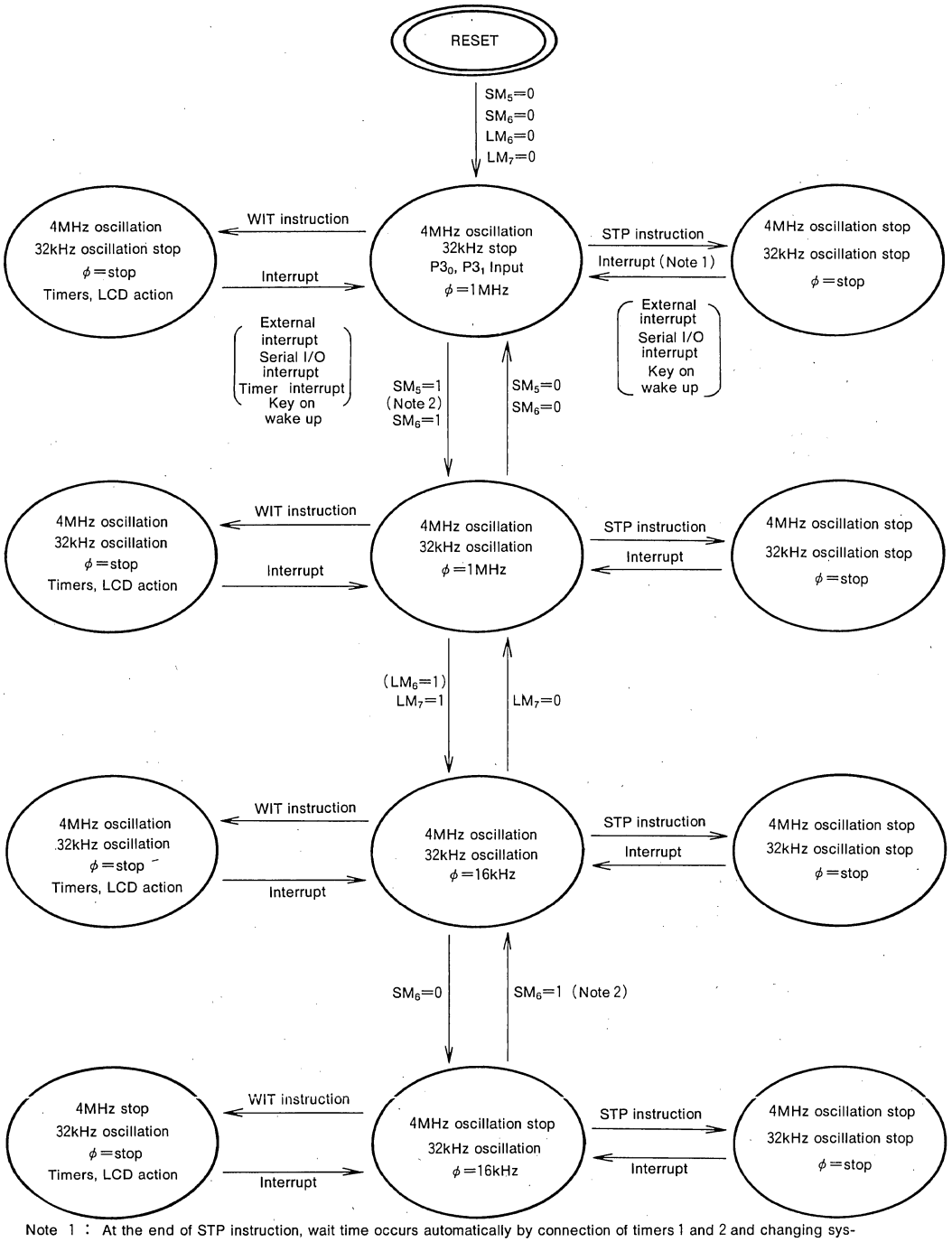


Fig.27 Block diagram of clock generating circuit



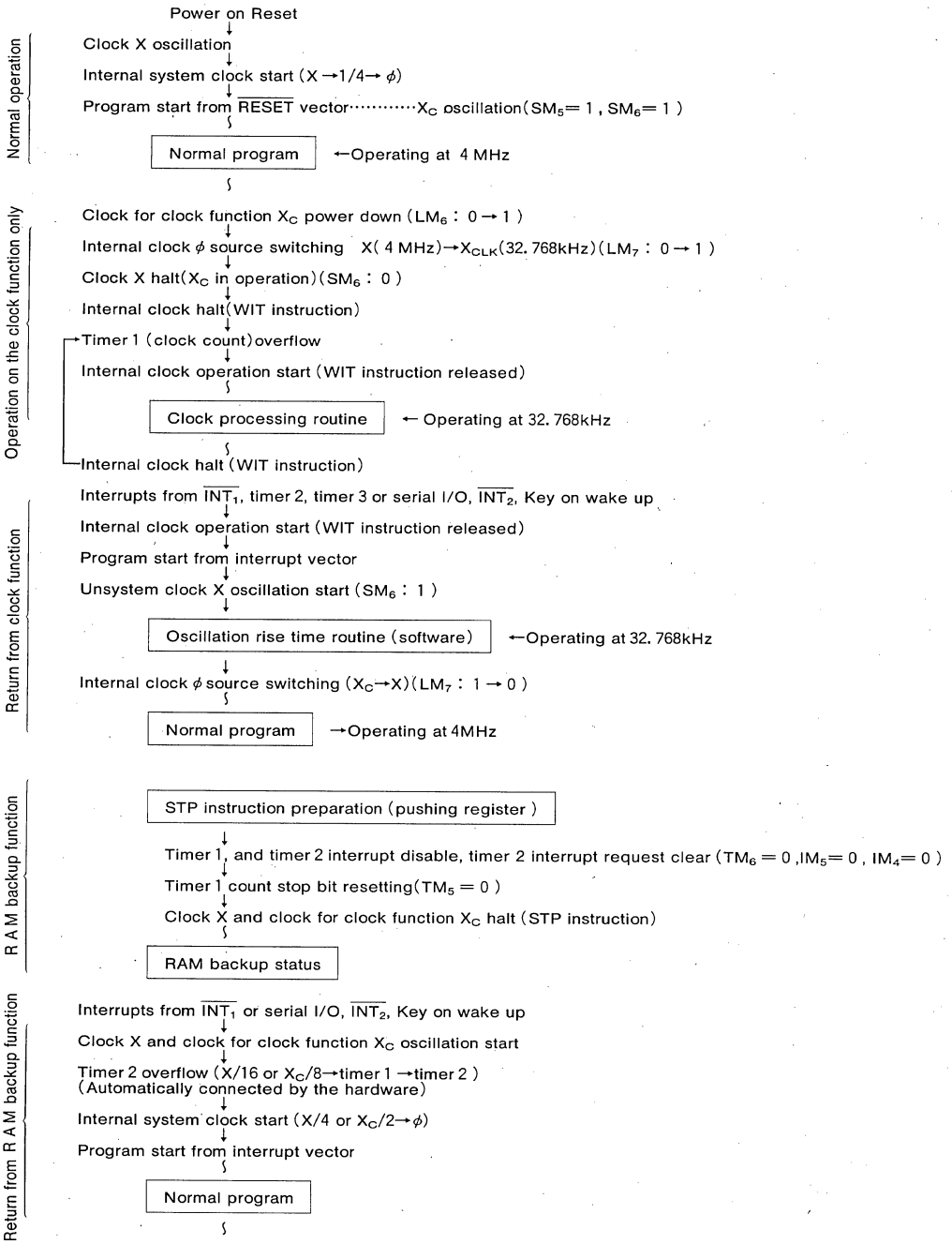
Note 1 : At the end of STP instruction, wait time occurs automatically by connection of timers 1 and 2 and changing system clock. This time is set by program.

2 : When $SM_6=1$ and unsystem clock is operated, wait time necessary by program until oscillation becomes stable.

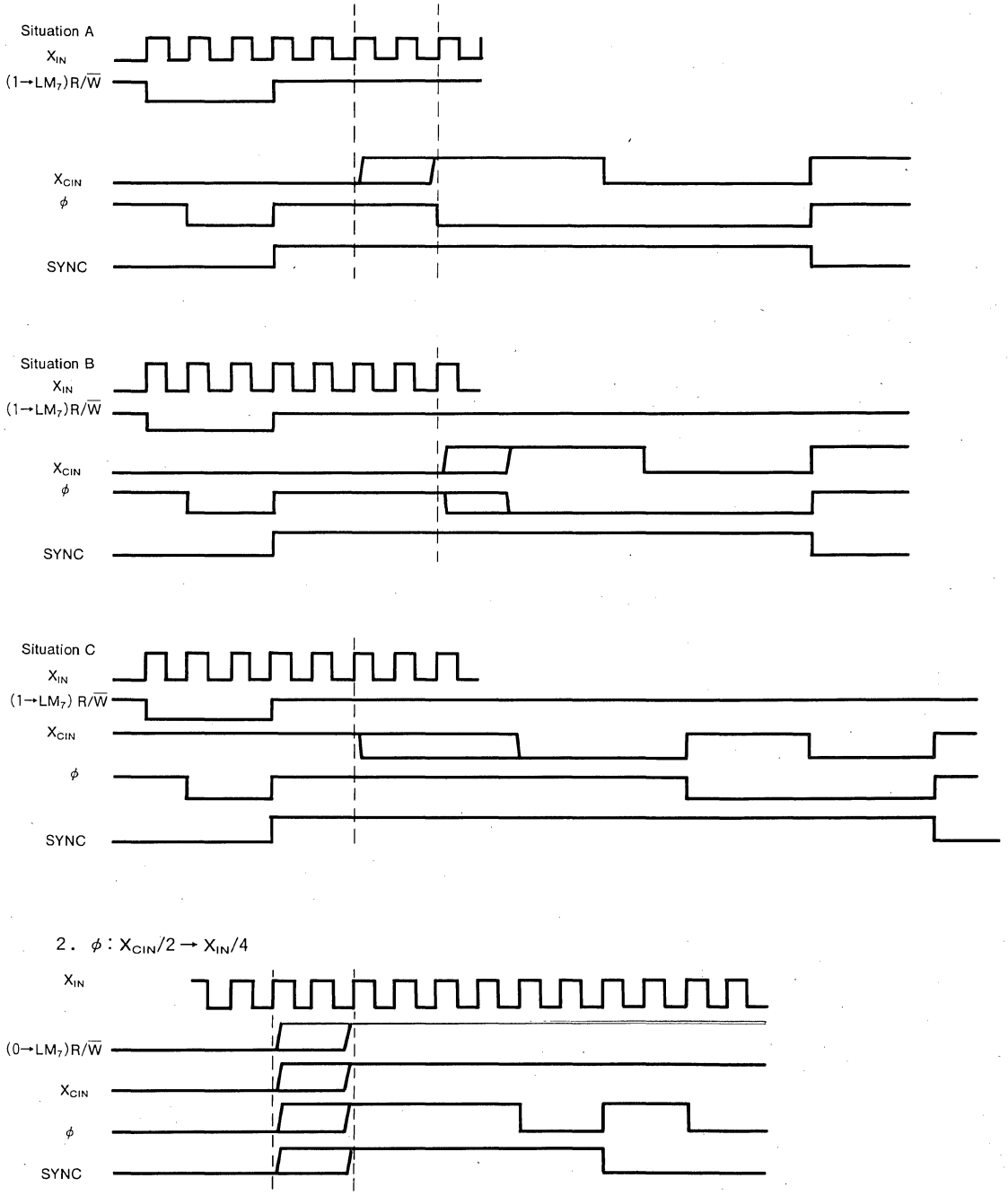
3 : The case of example clock X=4MHz, clock X_C=32kHz.

Fig.28 Transition of states for the system clock

≪An example of flow for system≫



1. ϕ : $X_{IN}/4 \rightarrow X_{CIN}/2$ (timing diagrams are shown situation A~C, because there are three kinds of waveform by the timing)



2. ϕ : $X_{CIN}/2 \rightarrow X_{IN}/4$

Note 1 : The "L" period of the R/$\overline{W}$ signal is shown the writling timing of setting value to LM_7.
2 : The delay of timing is ignored.

Fig.29 Timing diagram of the changing system clock

PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When the timer 4 and the timer 5 are used at event counter mode, read the contents of these timers either while the input of the these timers are not changing or after timer 4, 5 count stop bit (bit 6 of address $00F8_{16}$) is set to "1".
Also, when the timer 1, timer 2, or timer 3 is input the clock except $\phi/4$ or it divided by timer, control the same as above.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC,CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) When LCD turn-on bit (bit 3 of address $00F5_{16}$) of the LCD mode register is "1", don't stop the timers or count source for timers.

(7) The serial I/O counter must be initialized (write to $00F7_{16}$) after switching the transfer clock source.

(8) When using an external clock as the transfer clock source, the serial I/O counter must be initialized while the external clock is at "H" level.

(9) The timer 1 and timer 2 must be set the necessary value immediately before the execution of a STP instruction.

(10) When using pins $P3_0$ and $P3_1$ as clock I/O pins, the pull-up option must not be used.

(11) Notes on controlling the clock generation circuit

① When system clock is changed $X_{IN}/4$ to $X_{CIN}/2$, set LM_7 to "1" after oscillation is stable by the software in side of clock X_C.

② When system clock is changed $X_{CIN}/2$ to $X_{IN}/4$, set LM_7 to "0" after oscillation is stable by the software in side of clock X.

③ When SM_5 is "0" or when LM_7 is "0" and SM_6 is "0", LM_6 is automatically set to "0" by the hardware.

④ When system clock selection bit (bit 7 of address $00F5_{16}$) of the LCD mode register is "1", don't set SM_5 to "0".

⑤ In single-chip mode, the X_{OUT} pin uses as X_{OUT} output except setting value of LM_5.

⑥ The other than single-chip mode and the input voltage for $\overline{RESET}$ pin is 10V, X_{OUT} pin uses as SYNC output except setting value of LM_5.

Just for reference, timing diagram of the changing system clock are shown in Figure 29.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3sets

Write the following option on the mask ROM confirmation from

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port $P3_5/S_{OUT}$ output format
- CNTR pin pull-up transistor (M50932-XXXFP only)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Output transistor are "off"	−0.3∼7	V
V_I	Supply voltage for LCD V_{L1}∼V_{L3}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, X_{IN}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $\overline{INT_1}$, CNV_{SS}		−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, CNTR		−0.3∼13	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, COM_0∼COM_3, SEG_0∼SEG_{31}, X_{OUT}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage CNTR		−0.3∼7	V
P_d	Power dissipation	T_a = 25℃	300	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Strage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=2.7∼5.5V, V_{SS}=0V, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Nom.	Max.	
V_{CC}	Supply voltage (Note 1)	f(X_{IN})=4.3MHz	4.5		5.5	V
		f(X_{IN})=1.1MHz	2.7		5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ (Note 2), $P3_3$∼$P3_7$ (Note3), $P4_0$∼$P4_7$, $\overline{RESET}$, X_{IN}, CNV_{SS}		0.7V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$ (Note 4), $\overline{INT_1}$, CNTR		0.74V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ (Note 2), $P3_3$∼$P3_7$ (Note 3), $P4_0$∼$P4_7$, CNV_{SS}		0		0.3V_{CC}	V
V_{IL}	"L" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$ (Note 4), $\overline{INT_1}$, CNTR		0		0.26V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16V_{CC}	V
I_{OH}	"H" output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$ (Note 5), X_{OUT}				−2	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, X_{OUT} (Note 6)				10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, X_{OUT} (Note 7)				5	mA
f(X_{IN})	Clock oscillating frequency (Note 8)	V_{CC}=4.5∼5.5V	64		4300	kHz
		V_{CC}=2.7∼5.5V	64		1100	
f(X_{CIN})	Clock oscillating frequency for clock function (Note 8)		32		50	kHz

Note 1 When only maintaining the RAM data, minimum value of V_{CC} is 2V.
2 When using port $P3_1$ as X_{CIN}, $0.85V_{CC} \leqq V_{IH} \leqq V_{CC}$, $0 \leqq V_{IL} \leqq 0.15V_{CC}$ for port $P3_1$.
3 In this case of using port $P3_6$ as normal input.
4 In this case of using port $P3_6$ as CLK input.
Especially when the input oscillation frequency is more than 50kHz, recommend the following :
$0.8V_{CC} \leqq V_{IH} \leqq V_{CC}$, $0 \leqq V_{IL} \leqq 0.2V_{CC}$
5 The total of I_{OH} of port P0, P1, P2, P3 and X_{OUT} should be 35mA max.
6 The total of I_{OL} (peak) of port P0, P1, P2, P3 should be 55mA max, and the total of I_{OL} (peak) of port P3, CNTR, and X_{OUT} should be 45mA max.
7 I_{OL} (avg) is the average current in 100ms.
8 When changing the contents of the most significant bit at address $00F5_{16}$, f(X_{IN}) needs the following range : f(X_{IN})>3f(X_{CIN}).

ELECTRICAL CHARACTERICS (V_{SS}= 0 V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$(Note 9)(Note10)	V_{CC}=5V, I_{OH}=−2mA		3			V
		V_{CC}=3V, I_{OH}=−0.7mA		2			
V_{OH}	"H" output voltage X_{OUT}	V_{CC}=5V, I_{OH}=−1.5mA		3			V
		V_{CC}=3V, I_{OH}=−0.3mA		2			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$(Note10), CNTR	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
V_{OL}	"L" output voltage X_{OUT}	V_{CC}=5V, I_{OL}=1.5mA				2	V
		V_{CC}=3V, I_{OL}=0.3mA				1	
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$, CNTR	V_{CC}=5V		0.25		1	V
		V_{CC}=3V		0.15		0.7	
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.4		
$V_{T+}-V_{T-}$	Hysteresis $P3_1$	When used as X_{CIN} input	V_{CC}=5V		0.7		V
			V_{CC}=3V		0.5		
$V_{T+}-V_{T-}$	Hysteresis $P2_0$~$P2_7$, $P3_2$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.4		
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5	0.7	V
		V_{CC}=3V			0.35		
$V_{T+}-V_{T-}$	Hysteresis X_{IN}	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.35		
I_{IL}	"L" input current $P4_0$~$P4_7$ (except reset state) {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR (Note 12)} without pull-up Tr. CNTR (Note 11), $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_{CC}=5V, V_I=0V				−5	μA
		V_{CC}=3V, V_I=0V				−4	
I_{IL}	"L" input current {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR (Note 12)} with pull-up Tr.	V_{CC}=5V, V_I=0V		−30	−70	−140	μA
		V_{CC}=3V, V_I=0V		−6	−25	−45	
I_{IL}	"L" input current $P4_0$~$P4_7$ (at reset state)	V_{CC}=5V, V_{L3}=5V, V_I=0V		−30		−140	μA
		V_{CC}=3V, V_{L3}=3V, V_I=0V		−6		−45	
I_{IH}	"H" input current $P4_0$~$P4_7$ (except reset state) $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_{CC}=5V, V_I=5V				5	μA
		V_{CC}=3V, V_I=3V				4	
I_{IH}	"H" input current $P4_0$~$P4_7$ (at reset state)	V_{CC}=5V, V_{L3}=5V, V_I=5V				5	μA
		V_{CC}=3V, V_{L3}=3V, V_I=3V				4	
R_{COM}	Output impedance COM_0~COM_3	V_{L1}=V_{CC}/3, V_{L2}=2V_{L1}, V_{L3}=V_{CC}, Other COM, SEG pins are opend.	V_{CC}=5V	30	200	2000	Ω
			V_{CC}=3V	70	500	4000	
R_S	Output impedance SEG_0~SEG_{31}		V_{CC}=5V		2		kΩ
			V_{CC}=3V		3		
I_{CC}	Supply current (at operation)	Output pin are opened. $\overline{RESET}$, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, and $P3_0$~$P3_7$ are connected to V_{CC}. Except the above pins are connected to V_{SS}. However, X_{IN} and X_{CIN} are input signal according to the conditions.	f(X_{IN})=4MHz, V_{CC}=5V		3	6	mA
			f(X_{IN})=1MHz, V_{CC}=3V		0.4		
			T_a=25℃, X_{IN}=0V, f(X_{CIN})=32.8kHz at low power mode (LM_6=1)	V_{CC}=5V	45		μA
				V_{CC}=3V	18		
I_{CC}	Supply current (at wait state)		f(X_{IN})=4MHz, V_{CC}=5V		1		mA
			f(X_{IN})=1MHz, V_{CC}=3V		0.2		
			T_a=25℃, X_{IN}=0V, f(X_{CIN})=32.8kHz at low power mode (LM_6=1)	V_{CC}=5V	20	60	μA
				V_{CC}=3V	4	12	
I_{CC}	Supply current		f(X_{IN})=0, f(X_{CIN})=0, V_{CC}=5V	T_a=25℃	0.1	1	μA
				T_a=70℃		10	
V_{RAM}	RAM retention voltage	f(X_{IN})=0, f(X_{CIN})=0		2		5.5	V

Note 9 Except when the output type of $P3_5$ is N-channel open drain (mask option).
10 If $P3_0$ is used as X_{COUT}, capability of load driving is lower than the above.
11 for M50930-XXXFP and M50931-XXXFP
12 for M50932-XXXFP

TIMING REQUIREMENTS
Memory expanding mode and microprocessor mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{su}(P2D−ϕ)	Port P2 input setup time		270			ns
t_{su}(P3D−ϕ)	Port P3 input setup time		270			ns
t_{su}(P4D−ϕ)	Port P4 input setup time		270			ns
t_{WI}	$\overline{INT_1}$, $\overline{INT_2}$ external clock input pulse width		1			μs
		V_{CC}=2.7V	4			μs
t_{WR}	$\overline{RESET}$ external clock input pulse width (Note 13)		2			μs
		V_{CC}=2.7V	8			μs
t_h(ϕ−P2D)	Port P2 input hold time		20			ns
t_h(ϕ−P3D)	Port P3 input hold time		20			ns
t_h(ϕ−P4D)	Port P4 input hold time		20			ns
t_C	External clock input cycle time (X_{IN} pin)		250			ns
t_W	External clock input pulse width (X_{IN} pin)		75			ns
t_r	External clock rising edge time (X_{IN} pin)				25	ns
t_f	External clock falling edge time (X_{IN} pin)				25	ns
t_{CC}	External clock input cycle time ($P3_1/X_{CIN}$ pin, X_{CIN})		20			μs
t_{WC}	External clock input pulse width ($P3_1/X_{CIN}$ pin, X_{CIN})		5			μs
t_{rc}	External clock rising edge time ($P3_1/X_{CIN}$ pin, X_{CIN})				6.2	μs
t_{fc}	External clock falling edge time ($P3_1/X_{CIN}$ pin, X_{CIN})				6.2	μs

Note 13 : Hold $\overline{RESET}$ to "L" level while eight or more rise pulses are input from X_{IN}.

SWITCHING CHARACTERISTICS
Memory expanding mode and microprocessor mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_d(ϕ−P0A)	Port P0 address output delay time	Fig. 30			250	ns
t_d(ϕ−P1A)	Port P1 address output delay time				250	ns
t_d(ϕ−P2Q)	Port P2 data output delay time				330	ns
t_d(ϕ−P2QF)	Port P2 data output delay time				300	ns
t_d(ϕ−R/W)	R/$\overline{W}$ signal output delay time				tcyc/4 +200	ns
t_d(ϕ−R/WF)	R/$\overline{W}$ signal output delay time				250	ns
t_d(ϕ−SYNC)	SYNC signal output delay time				250	ns
t_d(ϕ−P3Q)	Port P3 data output delay time				250	ns

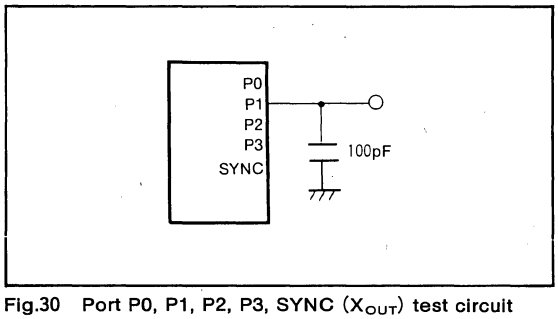
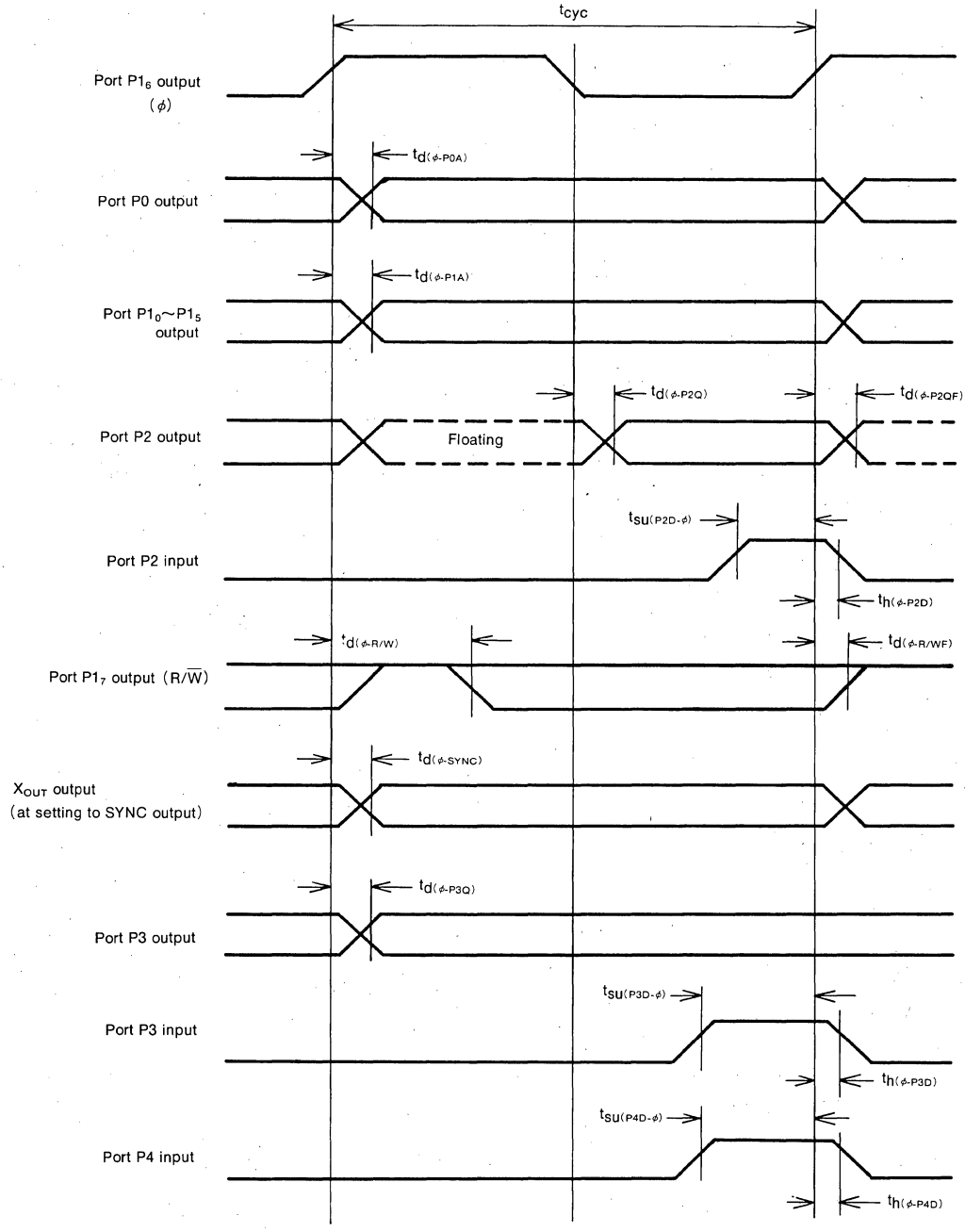
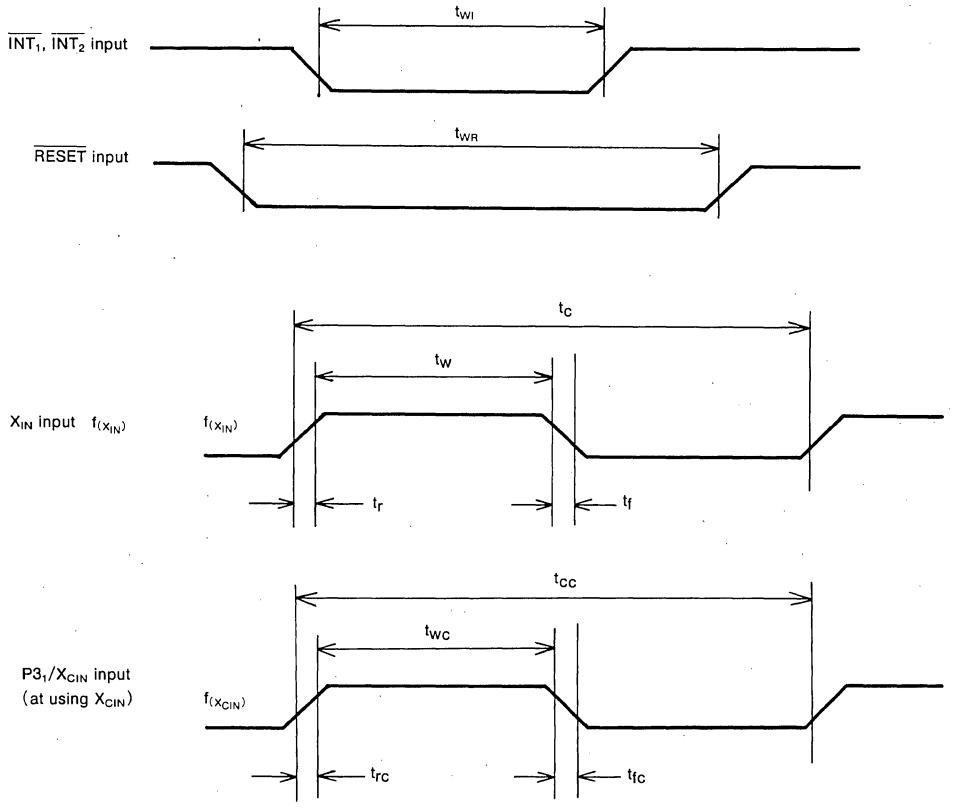


Fig.30 Port P0, P1, P2, P3, SYNC (X_{OUT}) test circuit

TIMING DIAGRAMS

In memory expanding mode and microprocessor mode




$\overline{INT_1}$, $\overline{INT_2}$ input
t_{WI}
$\overline{RESET}$ input
t_{WR}
X_{IN} input $f_{(X_{IN})}$
t_C
t_W
t_r
t_f
$P3_1/X_{CIN}$ input
(at using X_{CIN})
t_{CC}
t_{WC}
t_{rc}
t_{fc}

M50940-XXXSP/FP
M50941-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50940-XXXSP and the M50941-XXXSP are single-chip microcomputer designed with CMOS silicon gate technology. Both are housed in a 64-pin shrink plastic molded DIP.

These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50940-XXXSP and the M50941-XXXSP are noted below. The following explanations apply to the M50940-XXXSP. Specification variations for other chips, these are noted accordingly.

Type name	ROM size	RAM size
M50940-XXXSP	4096 bytes	128 bytes
M50941-XXXSP	8192 bytes	192 bytes

The differences between the M50940-XXXSP and the M50940-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

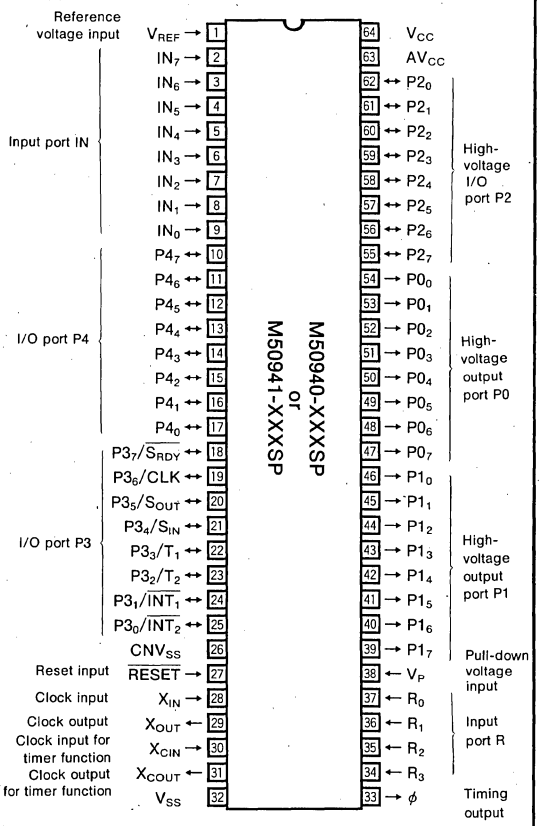
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 4096 bytes (M50940-XXXSP)
  8192 bytes (M50941-XXXSP)
  RAM ..... 128 bytes (M50940-XXXSP)
  192 bytes (M50941-XXXSP)
- Instruction executing time
  ..... 2μs (minimum instructions, at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz ..... 5V±10%
  f(X_{IN})=1MHz ..... 3~5.5V
- Power dissipation
  normal operation mode (at 4MHz frequency) 15mW
  low-speed operation mode (at 32kHz frequency for clock function) 0.3mW
- Subroutine nesting ..... 64 levels (Max.)
- Interrupt ..... 8 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as serial I/O)
- 16-bit timer ..... 1 (Two 8-bit timers make one set)
- Programmable I/O ports (Ports P3, P4) 16
- Input ports (Ports IN, R) 12
- High-voltage output ports (Ports P0, P1) 16
- High-voltage programmable I/O ports (Port P2) 8
- Serial I/O (8-bit) 1
- A-D conversion ..... 8-bit, 8 channel
- PWM function 1
- Two clock generator circuits (One is for main clock, the other is for clock function)

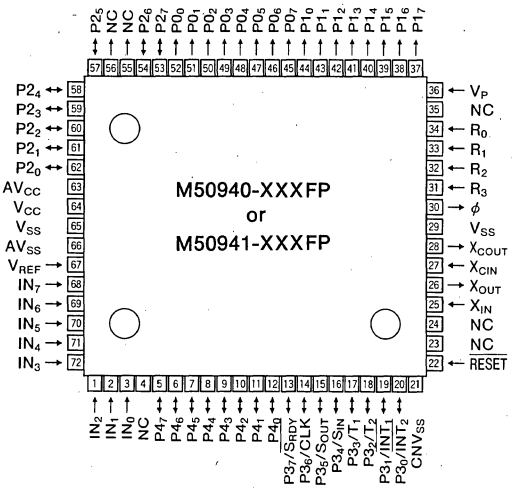
APPLICATION

Microwave oven, Air conditioner, Fan heater
Office automation equipment, Copying machine, Medical instruments
VCR, TV, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

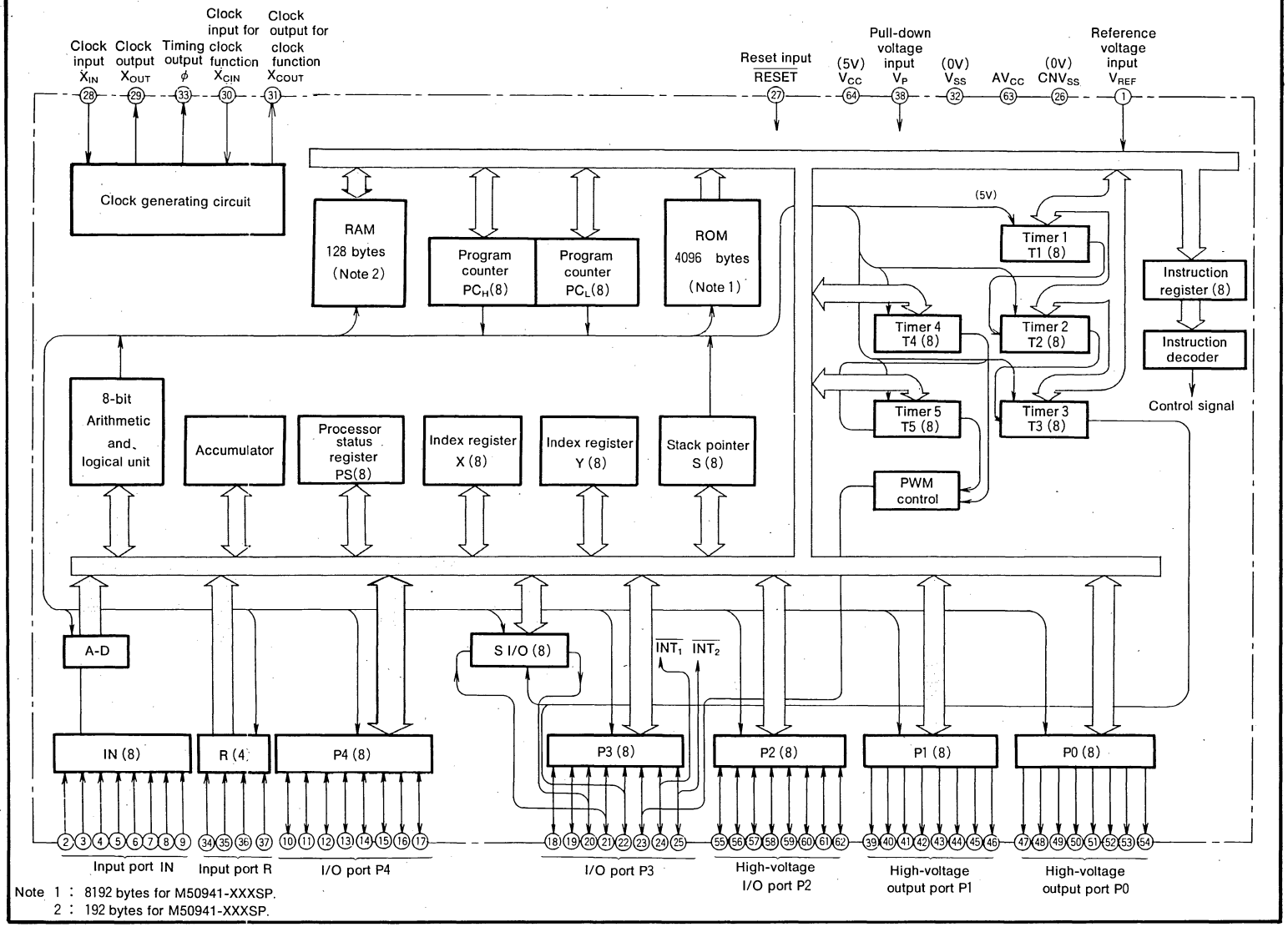


Outline 72P6

NC : No connection

MITSUBISHI ELECTRIC

M50940-XXXSP BLOCK DIAGRAM



Note 1 : 8192 bytes for M50941-XXXSP.
2 : 192 bytes for M50941-XXXSP.

MITSUBISHI ELECTRIC

FUNCTIONS OF M50940-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency)
Clock frequency			4.2MHz (main clock input), 32kHz (for clock function)
Memory size	ROM		4096bytes (8192bytes for M50941-XXXSP)
	RAM		128bytes (192bytes for M50941-XXXSP)
Input/Output port	P0, P1	Output	8-bit×2
	P2	I/O	8-bit×1
	P3, P4	I/O	8-bit×2
	IN	Input	8-ch analog input (This port is in common with 8-bit parallel digital input)
	R	Input	4-bit×1
Serial I/O			8-bit×1
Timers			8-bit timer×3, (2 when serial I/O is used)
			16-bit timer×1, (combination of two 8-bit timers)
Subroutine nesting			64 Levels (max) (96 Levels (max.) for M50941-XXXSP)
Interrupts			Two external interrupts, three timer interrupts (or two timers, one serial I/O)
Clock generating circuit			Two built-in circuits (ceramic or quartz crystal oscillator)
Supply voltage			5V±10%(at f(X_{IN})=4MHz), 3.0~5.5V(at f(X_{IN})≦1.0MHz)
Power dissipation	At high-speed operation		15mW (at f (X_{IN})=4MHz)
	At low-speed operation		0.3mW (at f (X_{CIN})=32kHz)
	At stop mode		1μA (at clock stop)
Input/Output characteristics	Input/Output voltage		5V (port P3, P4)
			V_{CC}−36V (port P0, P1, P2)
	Output current		−12mA (port P0, P1, P2: high-voltage P-channel open drain output)
			−5~+10mA (port P3, P4: CMOS tri-state output)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package	M50940-XXXSP, M50941-XXXSP		64-pin shrink plastic molded DIP
	M50940-XXXFP, M50941-XXXFP		72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P0, P1 and P2.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillatior to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open. This clock can be used as a program controlled the system clock.
X_{COUT}	Clock output for clock function	Output	
$P0_0$~$P0_7$	Output port P0	Output	Port P0 is an 8-bit output port. Output structure is high-voltage P-channel open drain. A pull-down transistor is built-in between the V_P pin and this port. At reset, this port is set to a "L" level.
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is P-channel open drain. A pull-down transistor is built-in between the V_P pin and this port.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port with CMOS tri-state output. The other functions are basically the same as port P2. $P3_0$, $P3_1$, $P3_2$ and $P3_3$ pins are in common with $\overline{INT_2}$, $\overline{INT_1}$, T_2, and T_1, respectively. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN}, pins, respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port with CMOS tri-state output. The other functions are basically the same as port P2.
R_0~R_3	Input port R	Input	Port R is a 4-bit input port.
IN_0~IN_7	Analog input port IN	Input	Port IN is the analog input pin to the A-D converter. It also has a dual function and works as a normal input port.
AV_{CC}	Voltage input for A-D		This is the power supply input pin for the A-D conveter.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin for the A-D conveter.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50940-XXXSP is shown in Figure 1. Addresses $F000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 4096 bytes (8192 bytes for M50941-XXXSP). Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required.

The RAM, I/O port, timer, etc. addresses are already assigned for the zero page. Addresses 0000_{16} to $007F_{16}$ are assigned for the built-in RAM which consists of 128 bytes (192 bytes for M50941-XXXSP) of static RAM. This RAM is used as the stack during subroutine calls and interrupts, in addition to data storage.

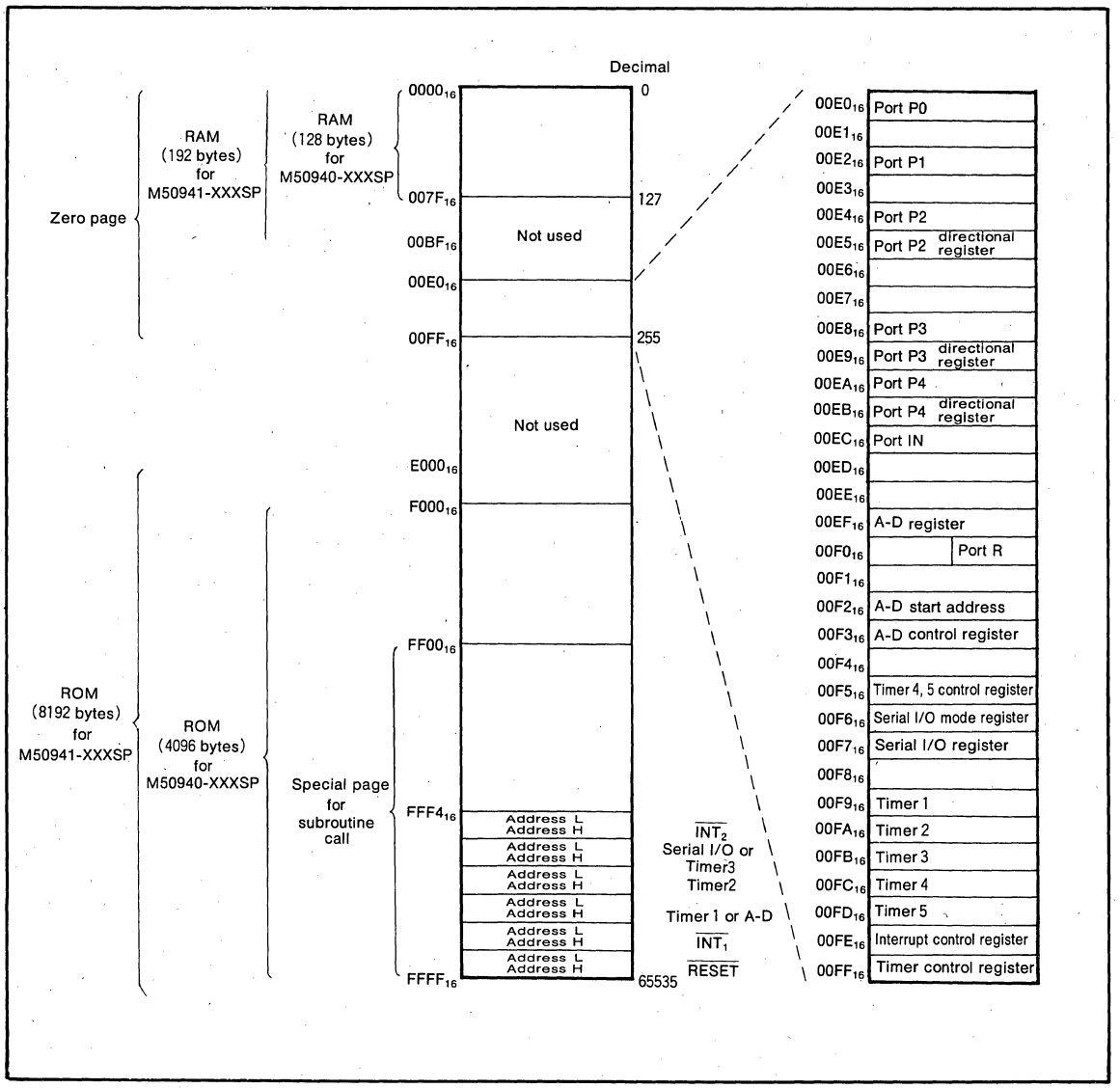


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, input/output, etc., is executed mainly through the accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register. In the index regsiter X addressing mode, the value of the OPERAND added to the contents of the index register X specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGSITER Y (Y)

The index register Y is an 8-bit register. In the index register Y addressing mode, the value of the OPERAND added to the contents of the index register Y specifies the real address.

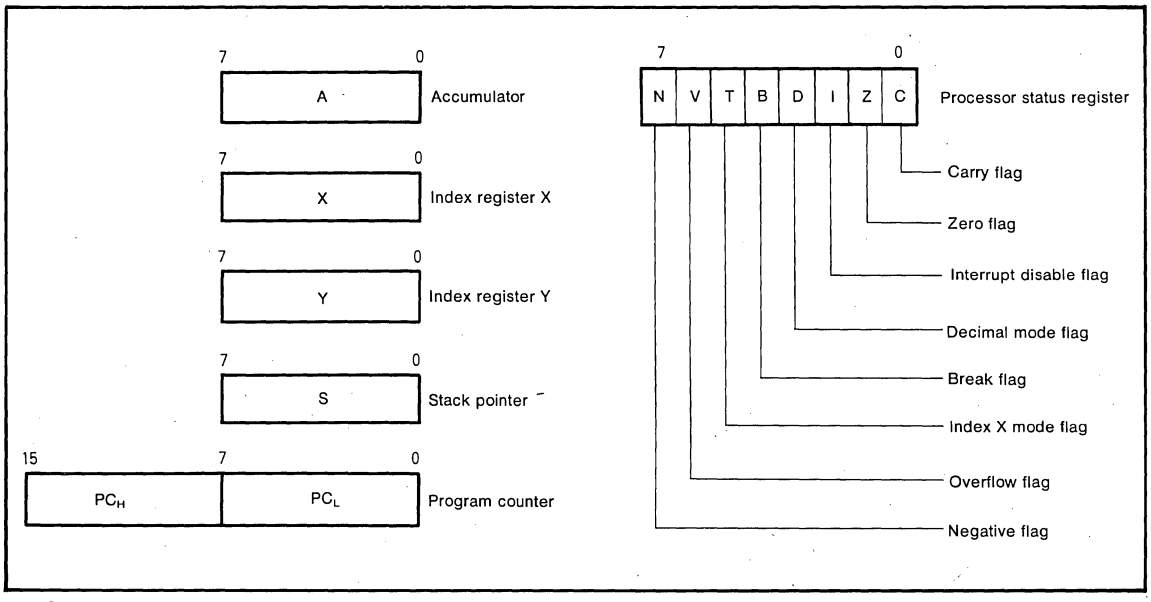


Fig.2 Register structure

STACK POINTER (S)

The stack pointer is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

When an interrupt occurs, the higher 8 bits of the program counter is pushed into the stack first, the stack pointer is decremented, and then the lower 8 bits of the program counter is pushed into the stack. Next the contents of the processor status register is pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter and processor status register data is popped off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically, so a Push Accumulator instruction (PHA) is provided to execute this function. Restoring the accumulator to its previous value is accopmlished by the Pop Accumulator instruction (PLA). It is executed in the reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed and popped to and frome the stack with the PHP and PLP instructions, respectively.

During a subroutine call, only the Program Counter is pushed into the stack. Therefore, any registers that should not be destroyed should be pushed into the stack manually. To return from a subroutine call, the RTS instruction is used.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The 8-bit PS is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explanined below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic Logic Unit (ALU) immediately after an operation. It is also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero falg will be set to "0". If the result is not zero, the zero flag will be set to "1".

3. Interrupt disable flag (I)

This falg is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt is accepted, this flag is automatically set to "1" to prevent from other interrupts until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the B flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the T flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the V flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the N flag. There are no instuctions for directly setting or resetting the N flag.

INTERRUPT

The M50940-XXXSP can be interrupted from eight sources; $\overline{INT_1}$, timer 1 or A-D, timer 2, timer 3 or serial I/O, and the $\overline{INT_2}$ or BRK instruction.

The value of bit 2 of the serial I/O mode register (address $00F6_{16}$) determines whether the interrupt is from timer 3 or from serial I/O. When bit 2 is "1" the interrupt is from serial I/O, and when bit 2 is "0" the interrupt is from timer 3. Also, when bit 2 is "1", parts of port 3 are used for serial I/O. Bit 3 of the A-D control register (address $00F3_{16}$) determines if an interrupt is from timer 1 or from the A-D. When bit 3 is "0", the interrupt is from timer 1, when bit 3 is "1" the interrupt is from the A-D. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as an interrupt.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag (I) is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The Reset interrupt is the highest priority interrupt and can never be inhibited. Except for the Reset interrupt, all interrupt are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0". The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"
(2) When the contents of timer 1, timer 2, timer 3 (or the serial I/O counter) go to "0".

These request bits can be reset by the program but can not be set.

Since the BRK instruction and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

Table 1. Interrupt vector address and priority.

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{INT_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer 1 or A-D	3	$FFFB_{16}$, $FFFA_{16}$
Timer 2	4	$FFF9_{16}$, $FFF8_{16}$
Timer 3 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{INT_2}$(BRK)	6	$FFF5_{16}$, $FFF4_{16}$

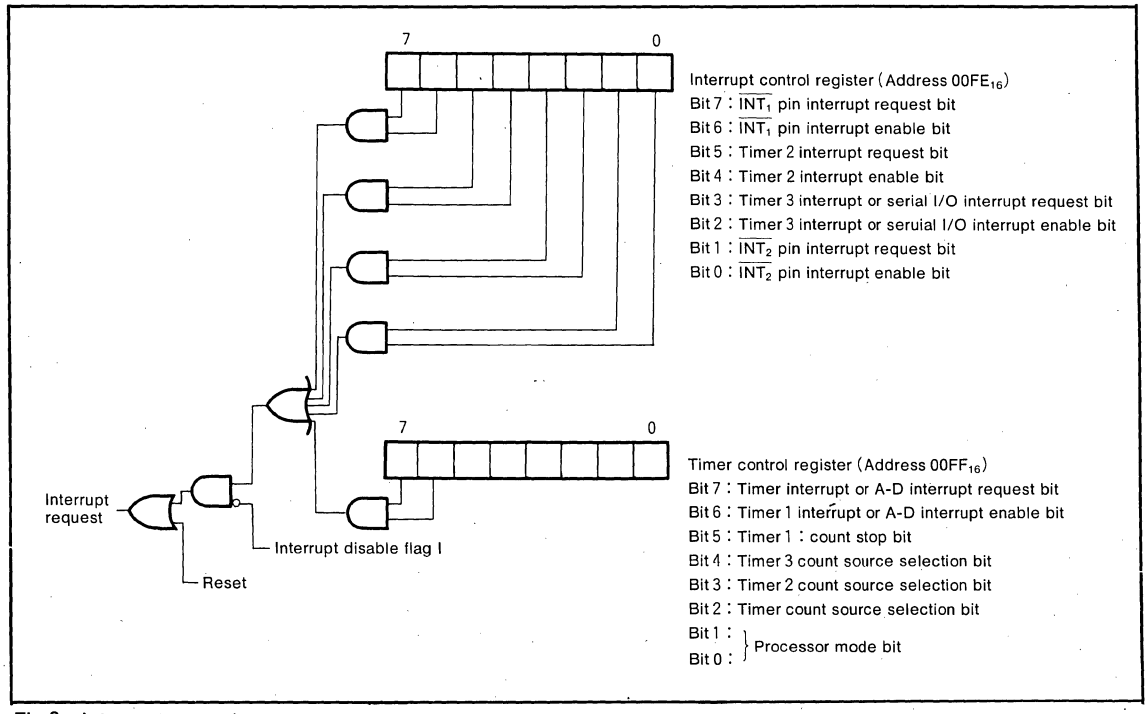


Fig.3 Interrupt control

TIMER

The M50940-XXXSP has five timers; timer 1, timer 2, timer 3, timer 4 and timer 5. Since P_3 (in serial I/O mode) and timer 3 use some of the same architecture, they cannot be used at the same time (see serial I/O section). The count source for each timer can be selected by using bit 2, 3 and 4 of the timer control register (address $00FF_{16}$), as shown in Figure 5. For more details about timer 4 and timer 5, see the PWM section.

A block diagram of timer 1 through 5 is shown in Figure 5. All of the timers are down count timers and have 8-bit latches. When a timer counter reaches "0", the contents of the reload latch are loaded into the timer and the next count pulse is input to a timer. The division ratio of the timers is $1/(n+1)$, where n is the contents of the timer latch.

The timer interrupt request bit is set to "1" at the next clock pulse after the timer reaches "0". The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see Interrupt section). The starting/stopping of timer 1 can be controlled by bit 5 of the timer control regsiter. If bit 5 (address $00FF_{16}$) is "0", the timer starts counting and when bit 5 is "1", the timer stops.

After a STP instruction is executed, timer 2, timer 1, and the clock (ϕ divided by 4) are connected in series (regardless of the status of the 2 through 3 of the timer control register). This state is canceled if the timer 2 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 1, count stop bit), and bit 4 of interrupt control register (timer 2 interrupt enable bit) bit 6 of the timer control register (timer 1 interrupt enable bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

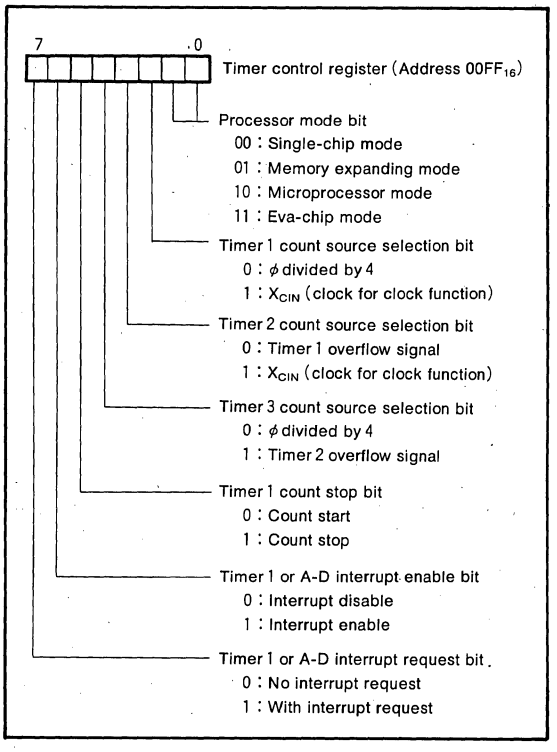


Fig.4 Structure of timer control register

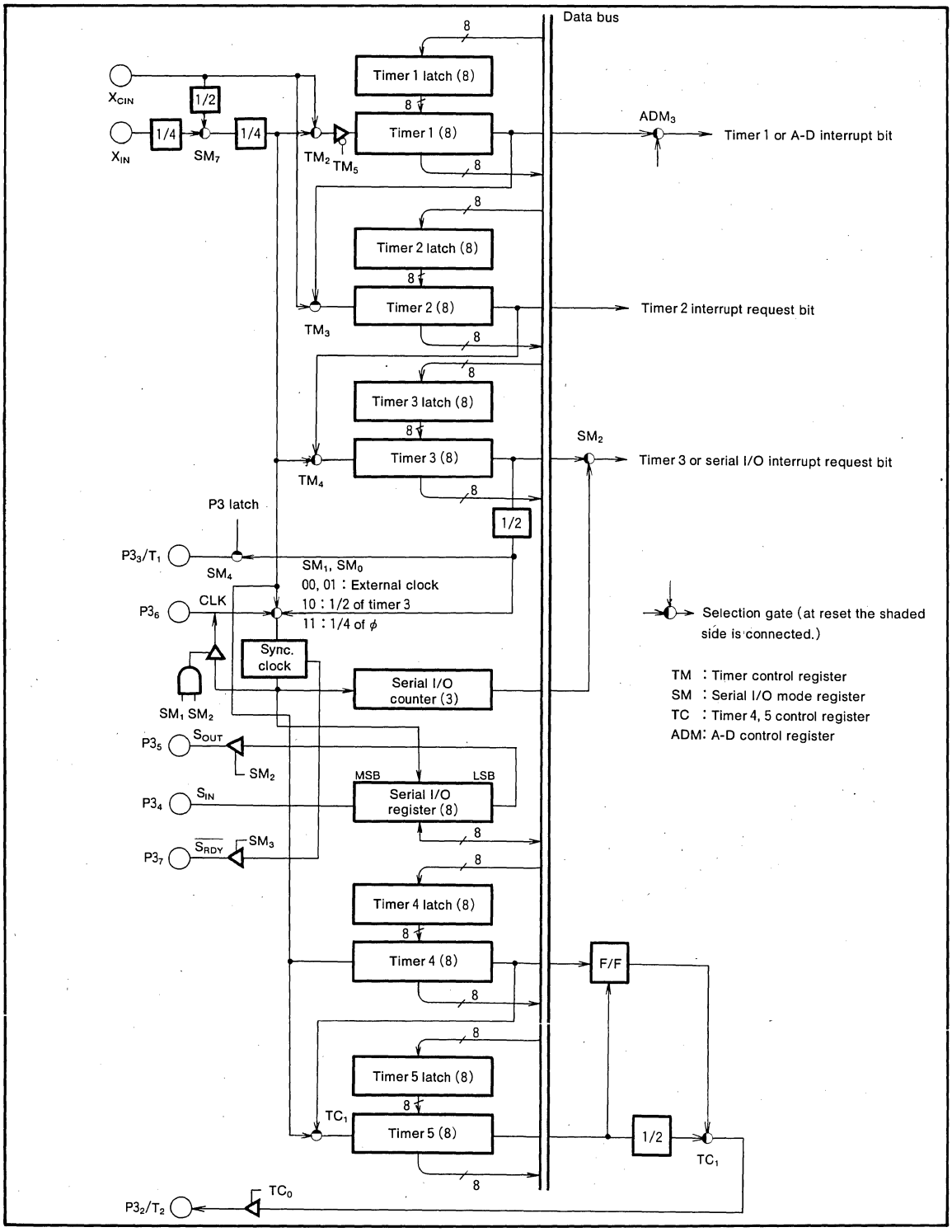


Fig.5 Block diagram of timer 1 through 5

PWM

The M50940-XXXSP has a pulse width modulated (PWM) output control circuit. The circuit outputs a variable duty cycle signal that can be used for a programmable pulse width and frequency. Timers 4 and 5 are used for the PWM. The control of these timers is explained in Figure 6 and the rectangular waveform is shown in Figure 7.

At reset, the PWM output is in a floating state. When timers 4 and 5 are not used for PWM control, they can be cascaded and used as a 16-bit timer. However, when used as a 16-bit timer, the interrupt function (such as timer 1 through timer 3) cannot be used.

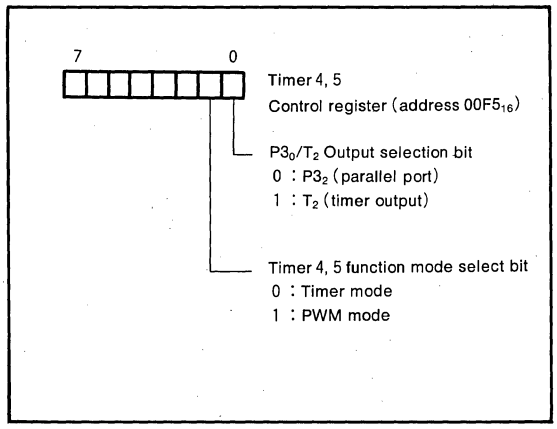


Fig.6 Structure of timer 4, 5 control register

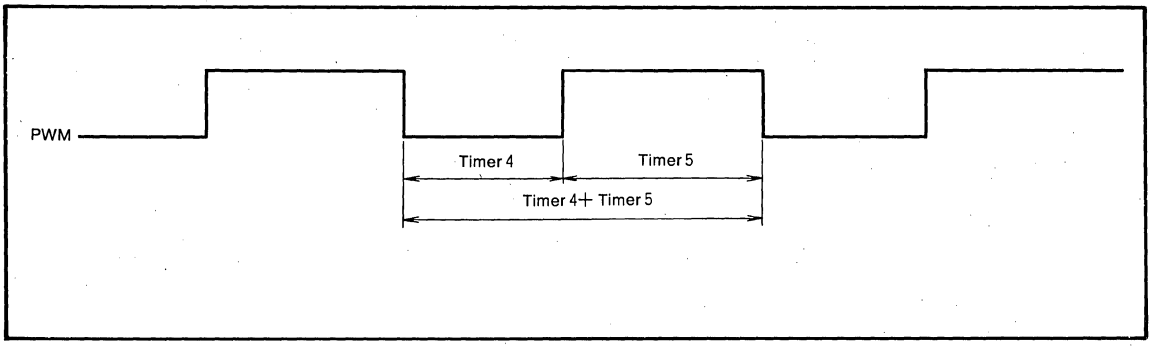


Fig.7 PWM rectangular wave form

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 8. In the serial I/O mode, the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O (S_{OUT}, S_{IN}) pins are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively.

The serial I/O mode register (address $00F6_{16}$) is an 8-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source. When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal (from timer 3) divided by two becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 (ie. 4μs at 4MHz) becomes the clock.

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$. And $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

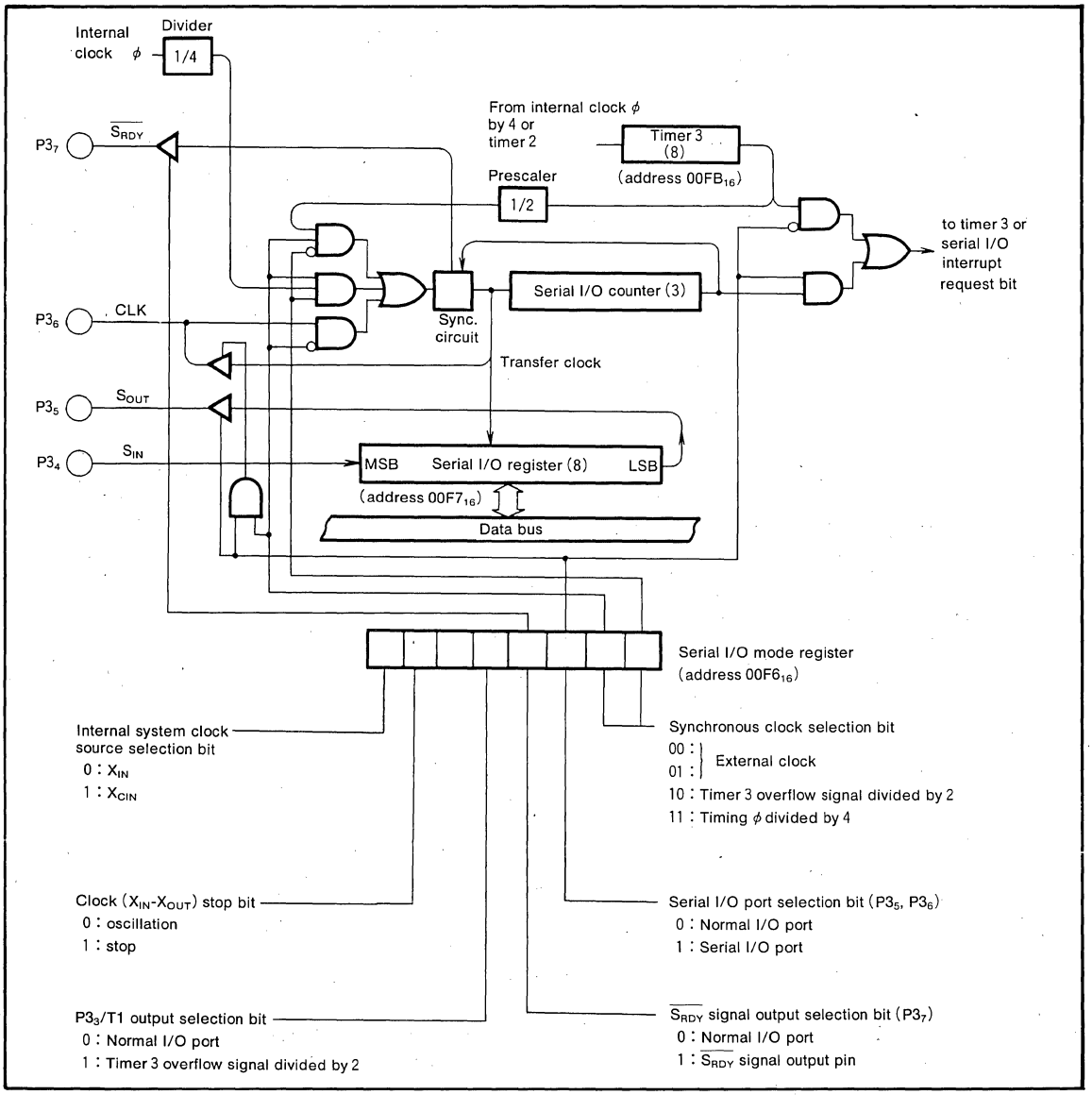


Fig.8 Block diagram of serial I/O

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 3. bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 3="0").

The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50940-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1-bit. Data is output starting with the LSB. After the transfter clock has counted 8 times, the serial I/O register will be empty and the transfter clock will remain at a high level. At this time the interrupt request bit will be set.

External clock—If an external clock is used, the interrupt request will be set after the transfter clock has counted 8 times but the transfter clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 9, and connections between two M50940-XXXSPs' are shown in Figure 10.

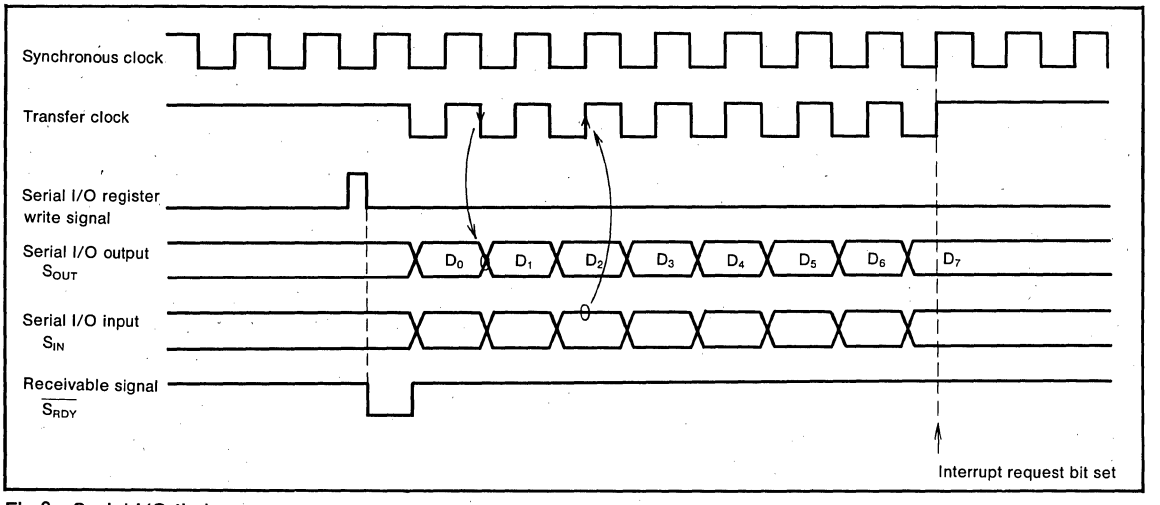


Fig.9 Serial I/O timing

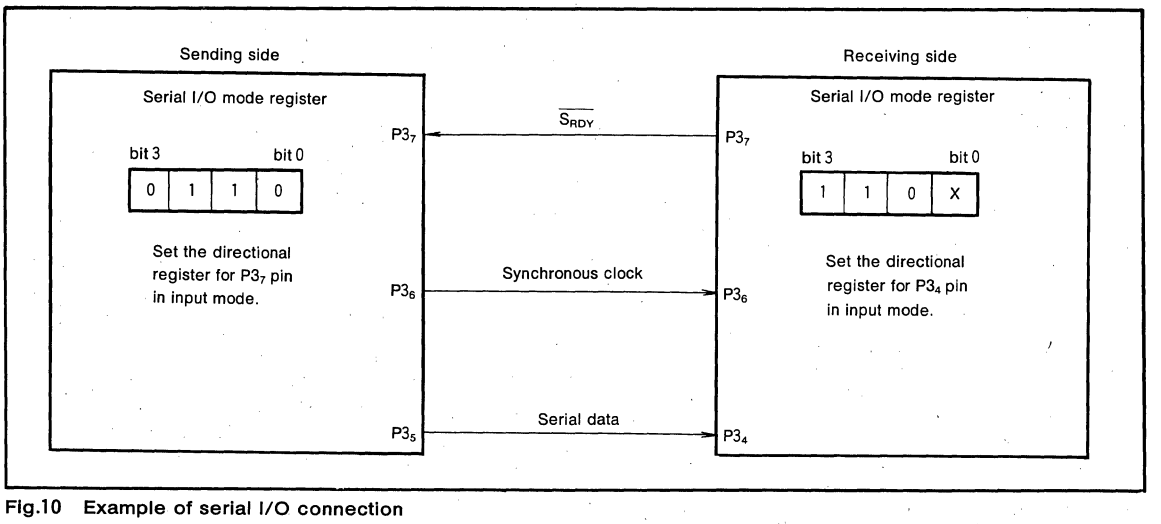


Fig.10 Example of serial I/O connection

A-D CONVERTER

The A-D converter circuitry is shown in Figure 11. The analog input ports of the A-D converter (IN_0~IN_7) are in common with the input ports of the data bus.

The 6-bit A-D control register is located at address $00F3_{16}$. One of the eight analog inputs is selected by bits 0, 1 and 2 of this register. bit 3 selects the interrupt source, either from timer 1 or the A-D itself. It bit 3 is "0", then the interrupt request is from timer 1, if it is "1", then it is from the A-D.

A-D conversion is accomplished by first selecting the analog channel (bit 0, 1) to be converted. bit 3 should also be set to "1" to select the A-D as the interrupt source. The conversion is started when dummy data is written into address $00F2_{16}$. When the conversion is finished, an interrupt is generated by the A-D and the digital data can be read from the A-D register (address $00EF_{16}$). The end of the conversion is determined by either the A-D conversion end bit (bit 5 of the A-D control regiser) or an A-D interrupt request bit (Address $00FF_{16}$).

The A-D conversion can also be programmed for high or low speed conversions. This is accomplished by using the A-D conversion speed switch bit (bit 4 of the A-D control register). For more information on the electrical characteristics of the high and low speed conversions, refer to the electrical characteristics section.

Port IN can also be used as an input port by reading data into address $00EC_{16}$. However, this cannot be done during A-D conversions.

The A-D control register is shown in Figure 12.

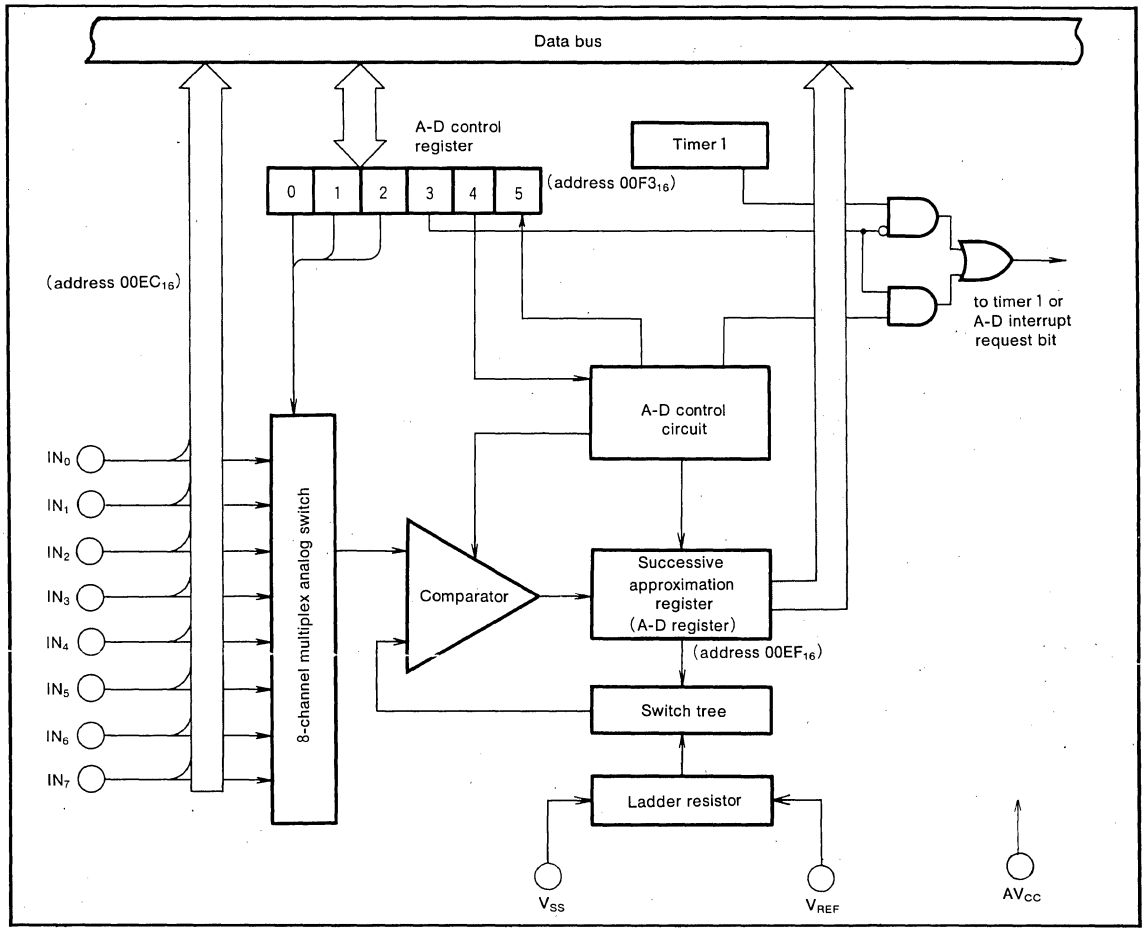


Fig.11 A-D conversion circuit

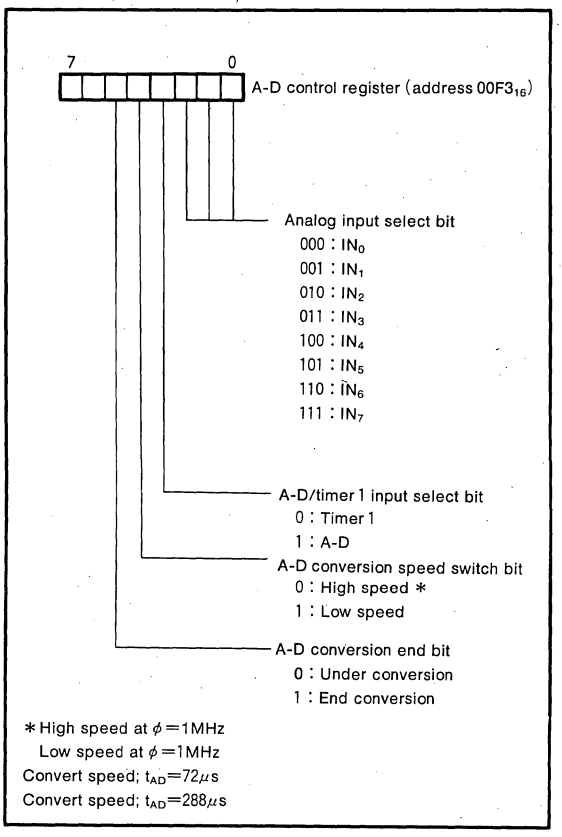


Fig.12 Structure of A-D control register

RESET CIRCUIT

The M50940-XXXSP is reset according to the sequence shown in Figure 15. And starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level.

		Address	
(1)	Port P0 register	($E0_{16}$) ···	00_{16}
(2)	Port P1 register	($E2_{16}$) ···	00_{16}
(3)	Port P2 directional register	($E5_{16}$) ···	00_{16}
(4)	Port P3 directional register	($E9_{16}$) ···	00_{16}
(5)	Port P4 directional register	(EB_{16}) ···	00_{16}
(6)	Serial I/O mode register	($F6_{16}$) ···	00_{16}
(7)	A-D control register	($F3_{16}$) ···	10000 0
(8)	Timer 4, 5 control register	($F5_{16}$) ···	00
(9)	Interrupt control register	(FE_{16}) ···	00_{16}
(10)	Timer cotrol register	(FF_{16}) ···	00_{16}
(11)	Interrupt disable flag for precessor status register	(PS) ·····	1
(12)	Program counter	(PC_H) ·····	Contents of address $FFFF_{16}$
		(PC_L) ·····	Contents of address $FFFE_{16}$

Since the contents of both registers other than those listed above (including timer 1, timer 2, timer 3, and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values.

Fig.13 Internal state of microcomputer at reset

The internal initializations following reset are shown in Figure 13.

An example of the reset circuit is shown in Figure 14.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

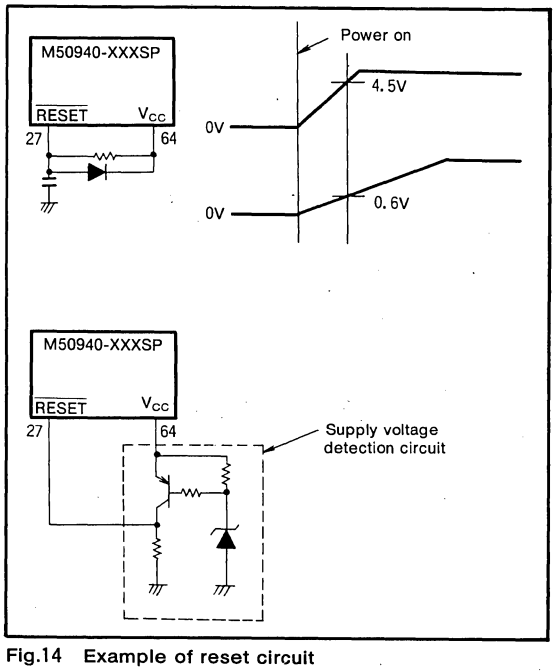


Fig.14 Example of reset circuit

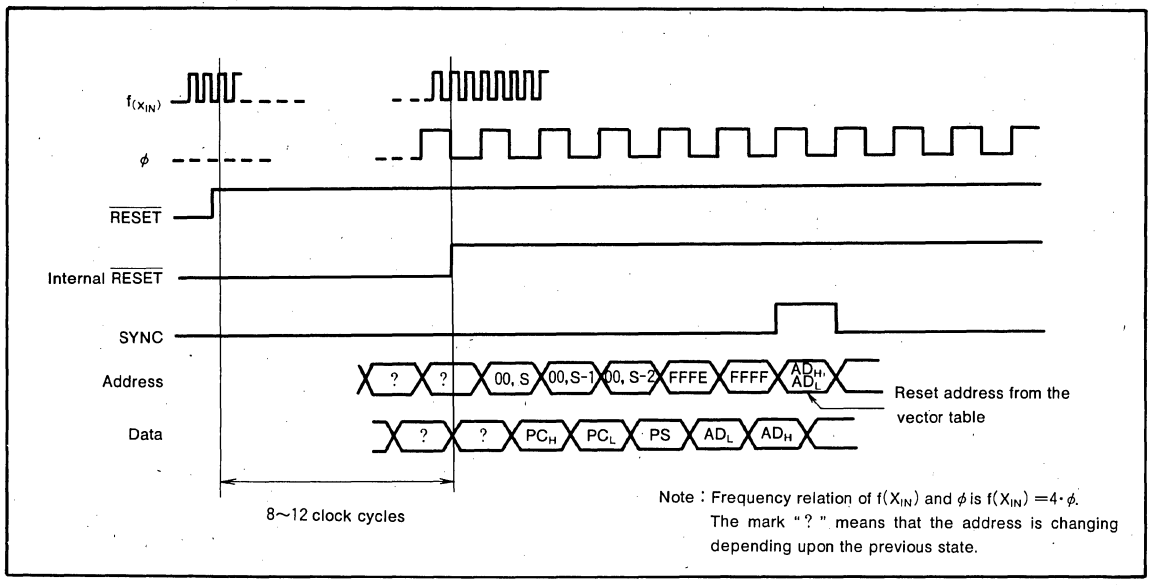


Fig.15 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit output port with P-channel open drain and high voltage outputs (V_{CC}-36V). Each pin has a built-in pull-down transistor connected to V_P. As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$.

Depending on the status of the processor status register (bit 0 and bit 1 of address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode, and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode section.

(2) Port P1

In the single-chip mode, Port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode section.

(3) Port P2

Port P2 is an 8-bit I/O port with P-channel open drain outputs. As shown in the memory map of Figure 1, port P2 can be accessed as memory at address $00E4_{16}$ of zero page. Port P2 has a directioanl register (address $00E5_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the high impedance state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

(4) Port P3

Port P3 is an 8-bit I/O port having CMOS outputs. Each pin is shared with serial I/O, timer overflow (T1, T2) and external interrupt input functions. These functions remain the same even if the device is used in other modes.

(5) Port P4

Port P4 is an 8-bit I/O port with CMOS outputs. During all modes except single chip mode, $P4_1$ and $P4_0$ function as both SYNC and R/$\overline{W}$ outputs as well as I/O ports (see processor mode section).

(6) Port R

Port R is a 4-bit input port.

(7) Port IN

Port IN is an 8-bit input port to the A-D converter. It can also be used as an input port by reading the input data into address $00EC_{16}$. However, this port cannot be read during A-D conversion.

(8) Clock φ output pin

This is the timing output pin. When selected the main clock (X_{IN}-X_{OUT}) as the internal system clock, the clock frequency divided by four is outputed. However, when selected the clock for clock function (X_{CIN}-X_{COUT}), the clock frequency divided by two is outputed.

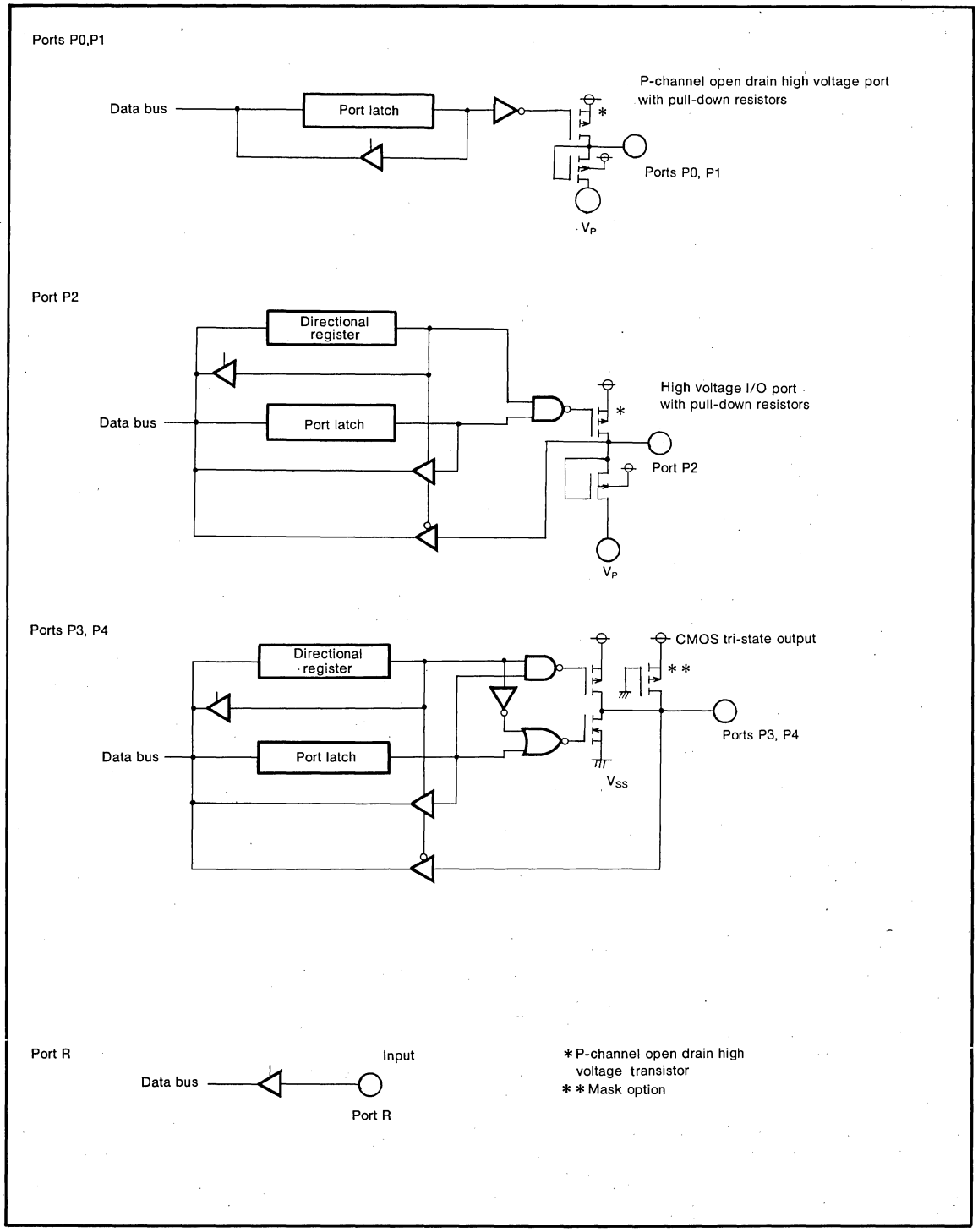


Fig.16 Block diagram of port P0~P4 and port R (single-chip mode)

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 of address $00FF_{16}$), four different operation modes can be selected; single chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, P0~P2 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports. Figure 18 shows the functions of ports P0~P2, and P4 corresponding to each mode.

The memory map of the single-chip mode is illustrated in Figure 1, and the other modes are shown in Figure 17. By connecting the CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode regsiter. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

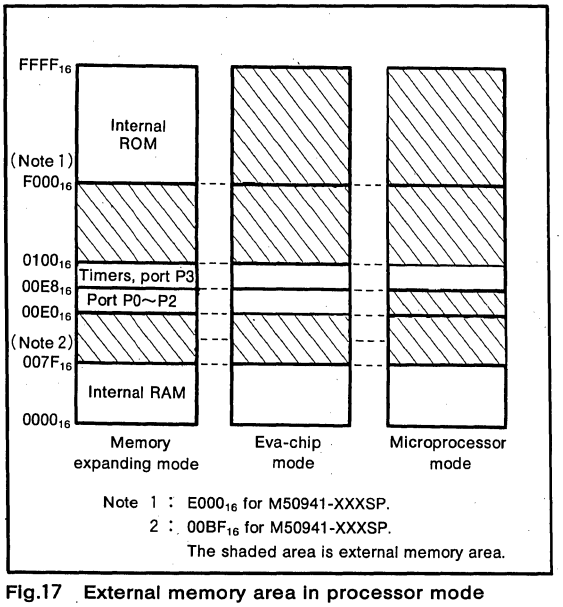


Fig.17 External memory area in processor mode

(1) Single-chip mode [00]
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0~P4 will work as original I/O ports.

(2) Memory expanding mode [01]
The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memroy when the internal memory is not sufficient.
The lower 8 bits of address data for port P0 is output when ϕ goes to the "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.
Port P1's higher 8 bits of address data are output when ϕ goes to the "H" state and as it changes back to the "L" state it retains its original I/O functions.
Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of $D_7 \sim D_0$ (including instruction code) while at the "L" state.
Pins $P4_1$ and $P4_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state.
When in the "L" state, $P4_1$ and $P4_0$ retain their original I/O functins.
The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.
The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

(3) Microprocessor mode [10]
After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.
In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pin is lost. Port P2 becomes the data bus ($D_7 \sim D_0$) and loses its normal I/O functions. Port $P4_1$ and $P4_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]
When 10V is supplied to the CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. This mode has almost the same function as the memory expanding mode except that it needs all its programs to come from the outside (including ROM programs). The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

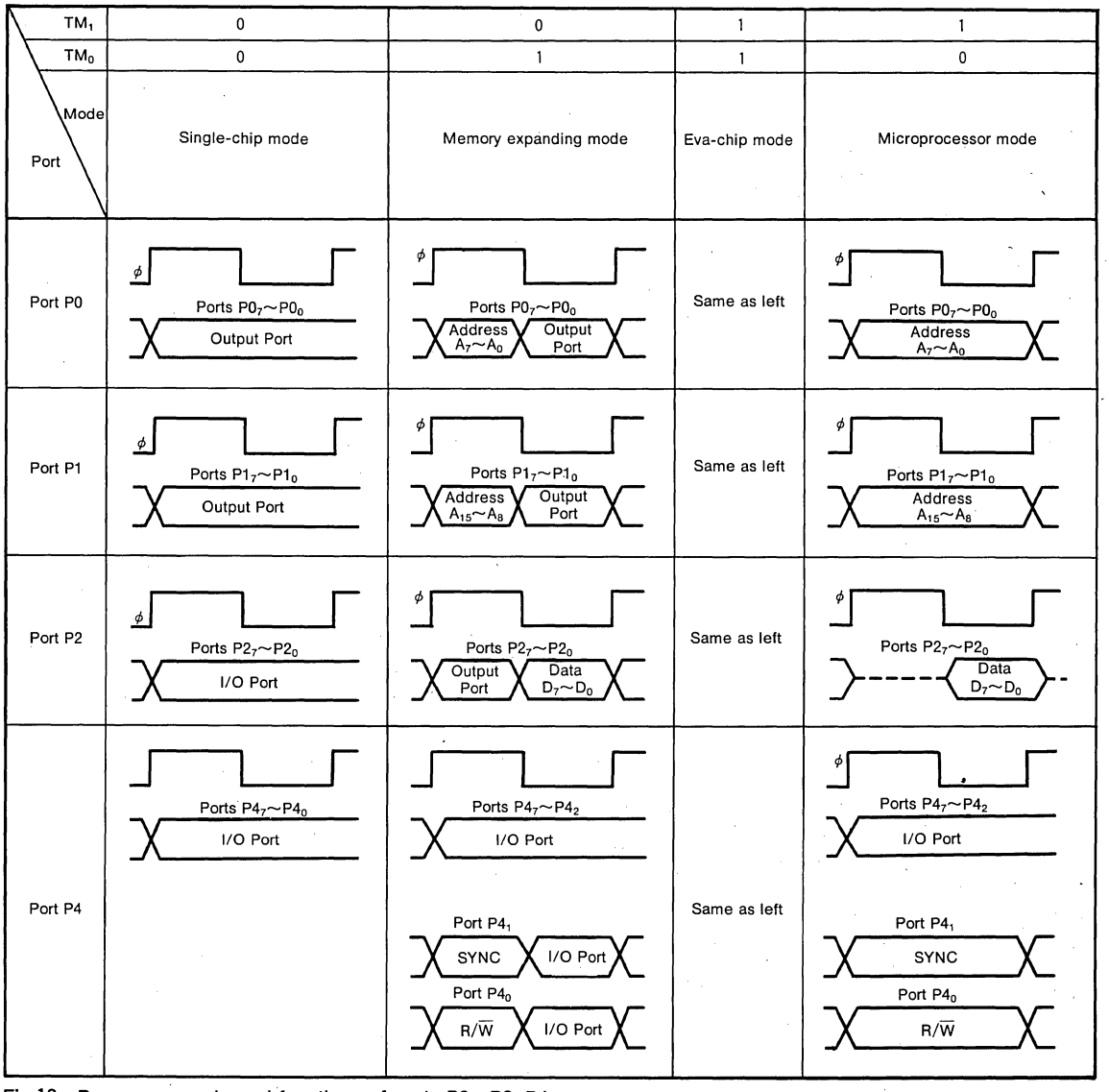


Fig.18 Processor mode and functions of ports P0~P2, P4

Table 2. Relationship between CNV_{SS} Pin Input Level and Processor Mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The M50940-XXXSP has two internal clock generating circuit. Figure 21 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ. Bit 7 of serial I/O mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 19 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacture's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input form the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 20.

The M50940-XXXSP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 1 and timer 2 are forcibly connected and $\phi/4$ is selected as timer 1 input. Before executing the STP instruction, appropriate values must be set in timer 1 and timer 2 to enable the oscillator to stabilize when restarting oscillation. Before executing the STP instruction, the timer 1 count stop bit must be set to supply ("0"), timer 1 interrupt enable bit and timer 2 interrupt enable bit must be set to disable ("0"), and timer 2 interrupt request bit must be set to no request ("0").

Oscillation is restarted (release the stop mode) when $\overline{INT_1}$, $\overline{INT_2}$, or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 2 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes because no wait time is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock (120μA max. at $f(X_{CIN}) = 32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of serial I/O mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 22 shows the transition of states for the system clock.

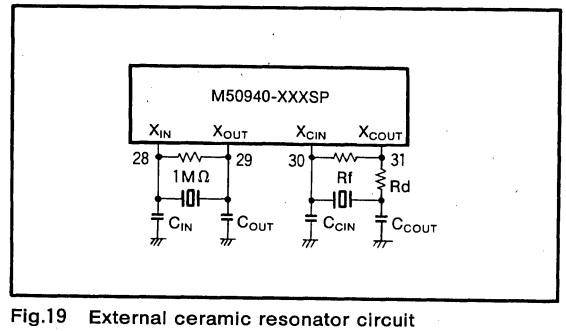


Fig.19 External ceramic resonator circuit

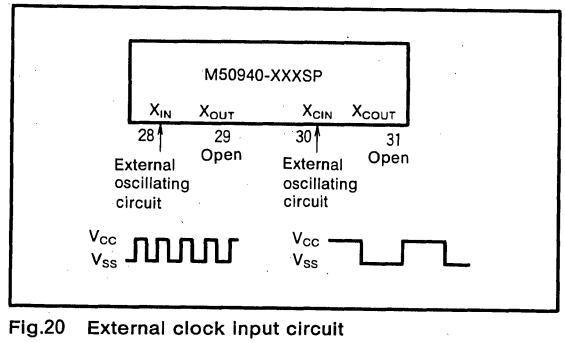


Fig.20 External clock input circuit

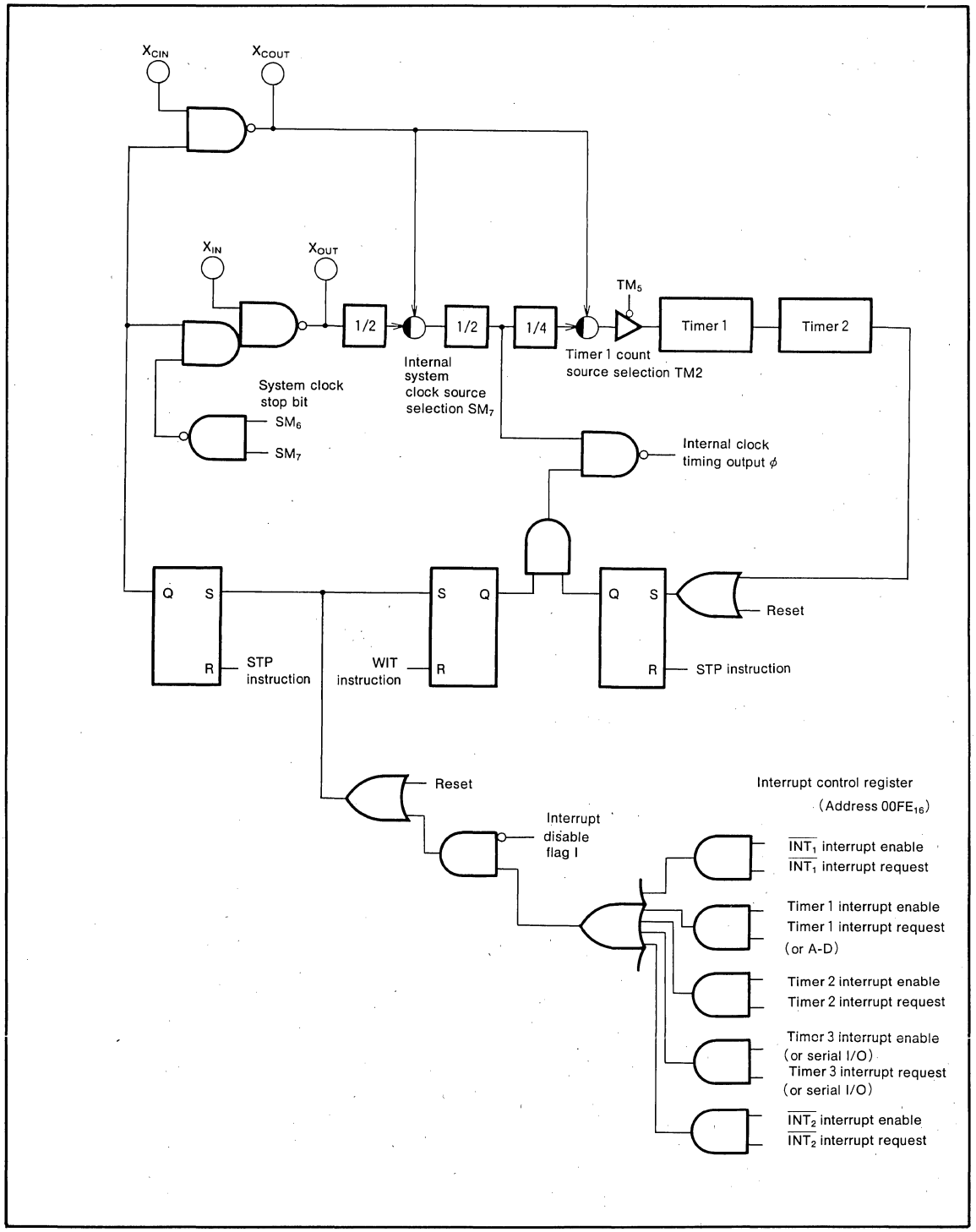
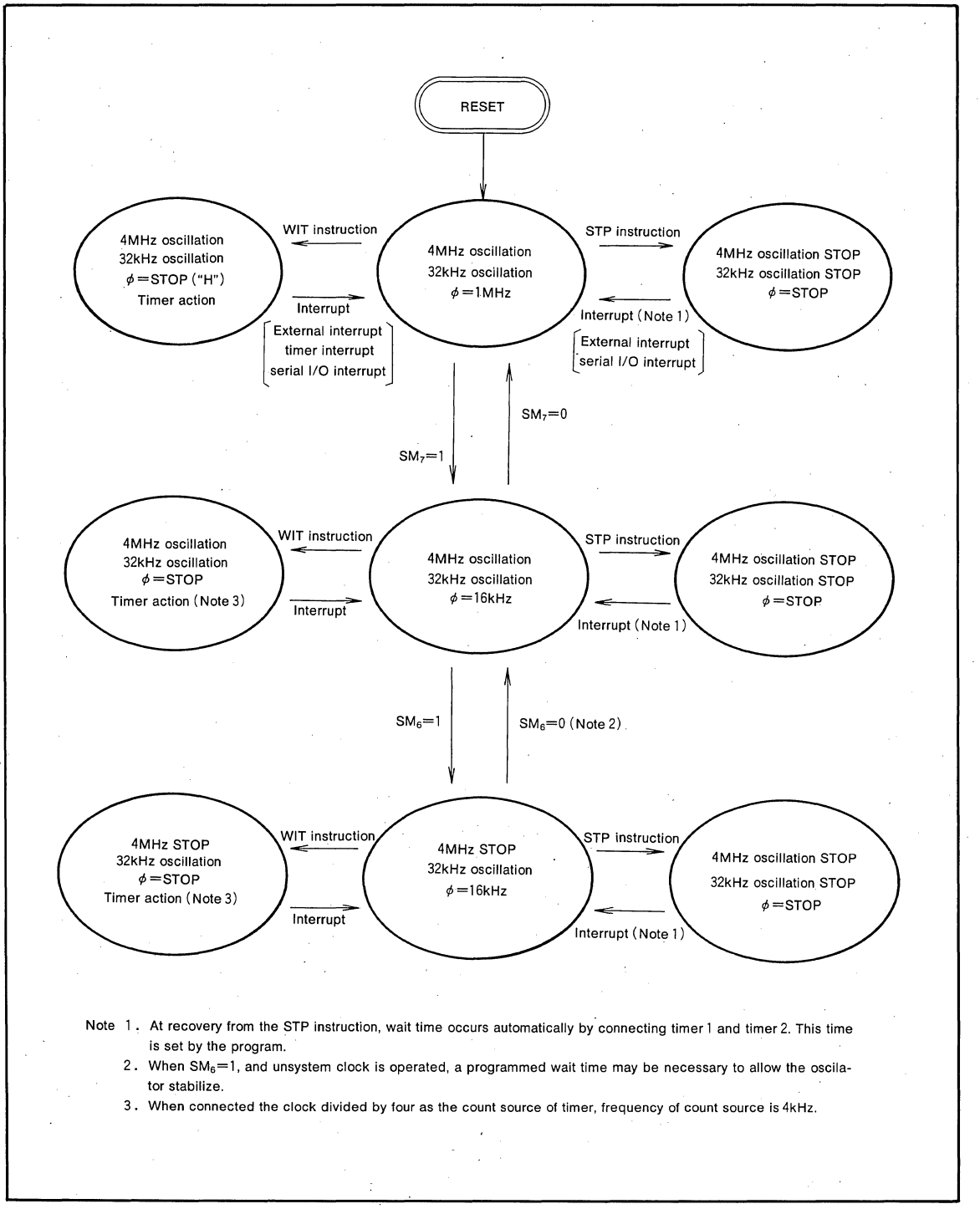


Fig.21 Block diagram of clock generating circuit



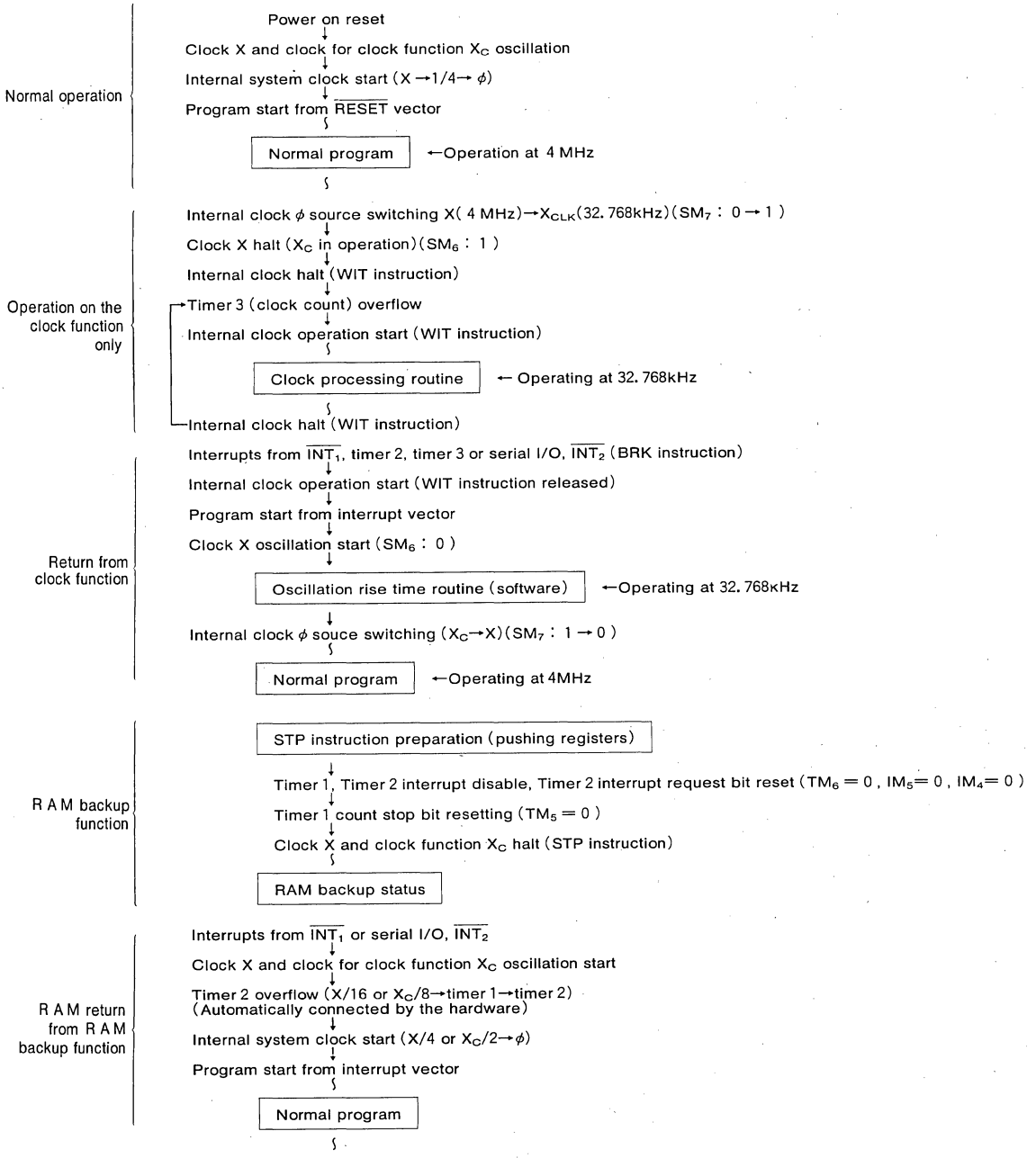
Note 1. At recovery from the STP instruction, wait time occurs automatically by connecting timer 1 and timer 2. This time is set by the program.

2. When $SM_6=1$, and unsystem clock is operated, a programmed wait time may be necessary to allow the oscillator stabilize.

3. When connected the clock divided by four as the count source of timer, frequency of count source is 4kHz.

Fig.22 Transition of states for the system clock

≪An example of flow for system≫



PROGRAMING NOTES

(1) The frequency ratio of the timer is 1/(n+1). (n=0~255)
(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) When the timer 1, timer 2, or timer 3 is input the clock except $\phi/4$ or it divided by timer, read the contents of these timers either while the input of these timers are not changing or after counting of timers are stoped.
(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed befoer the SEC, CLC, or CLD intructions are executed.
(5) A NOP instruction must be used after the execution of a PLP instruction.
(6) Notes on serial I/O
① Set "0" in the serial I/O interrupt enable bit (bit 2 of address $00FE_{16}$) before setting the serial I/O mode.
② Insert at least one instruction and set "0" in the serial I/O interrupt request bit (bit 3 of address $00FE_{16}$) after setting the serial I/O mode.
③ Set "1" in the serial I/O interrupt enable bit after the operation described in ②.
(7) The timer 1 and the timer 2 must be set the necessary value immediately before the execution of a STP instruction.
(8) Notes on A-D conversion
① Set "0" in the A-D interrupt enable bit (bit 6 of address $00FF_{16}$) before setting A-D conversion.
② Insert at least one instruction and set "0" in the A-D interrupt request bit (bit 7 of address $00FF_{16}$) after setting the A-D conversion.
③ Set "1" in the A-D interrupt enable bit after the operation described in ②.
④ Set "0" in bit 3 of the A-D control register (address $00F3_{16}$) before using a STP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ····· EPROM 3 sets
Write the following option on the mask ROM confirmation form

- Port P3 pull-up transistor bit
- Port P4 pull-up transistor bit

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} output transistors are at "OFF" state.	−0.3~7	V
V_P	Pull-down input voltage		V_{CC}−38~V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3~13	V
V_I	Input voltage R_0~R_3, X_{IN}, X_{CIN}, $\overline{RESET}$		−0.3~7	V
V_I	Input voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$, IN_0~IN_7, V_{REF}		−0.3~V_{CC}+0.3	V
V_I	Input voltage $P2_0$~$P2_7$		V_{CC}−38~V_{CC}+0.3	V
V_O	Output voltage $P3_0$~$P3_7$,$P4_0$~$P4_7$, X_{COUT}, X_{OUT}, ϕ		−0.3~V_{CC}+0.3	V
V_O	Output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$		V_{CC}−38~V_{CC}+0.3	V
Pd	Power dissipation	T_a=25℃	1000(Note 1)	mW
Topr	Operating temperature		−10~70	℃
Tstg	Strage temperature		−40~125	℃

Note 1. 600mW for QFP type.

RECOMMEND OPERATING CONDITIONS

(V_{CC}=5V±10%, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Nom.	Max.	
V_{CC}	Supply voltage	$f(X_{IN})$=4MHz	4.5	5	5.5	V
		$f(X_{IN})$≦1MHz	3	5	5.5	V
V_P	Pull-down supply voltage		V_{CC}−36		V_{CC}	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$, IN_0~IN_7,CNV_{SS}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage R_0~R_3		0.4V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$~$P2_7$		0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$, IN_0~IN_7, CNV_{SS}		0		0.2V_{CC}	V
V_{IL}	"L" input voltage R_0~R_3		0		0.12V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P2_0$~$P2_7$		V_{CC}−36		0.2V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$				−120	mA
$I_{OH(sum)}$	"H" sum output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				−30	mA
$I_{OL(sum)}$	"L" sum output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				60	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$				−24	mA
$I_{OH(peak)}$	"H" peak output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				−10	mA
$I_{OL(peak)}$	"L" peak output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				20	mA
$I_{OH(avg)}$	"H" average output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$				−12	mA
$I_{OH(avg)}$	"H" average output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				−5	mA
$I_{OL(avg)}$	"L" average output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				10	mA
$f_{(X_{IN})}$	Clock oscillating frequency	V_{CC}=5V			4.3	MHz
		V_{CC}=3V			1.1	MHz
$f_{(X_{CIN})}$	Clock oscillating frequency for clock function	V_{CC}=5V			500	kHz
		V_{CC}=3V			300	kHz

Note 1. The maximum "H" input voltage for CNV_{SS} is +12V.
2. The duty cycle for these oscillation frequency is 50%.
3. When the low speed mode is used, the clock input oscillation frequency for the timer must satisfy the following expression :
$f(X_{CIN}) < f(X_{IN})/3$
4. The avarage output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms cycle.
5. $f_{(X_{IN})}$ must be less than 50kHz when the external clock is to be used.

ELECTRICAL CHARACTERISTICS (V_{CC}= 5 V±10%, V_{SS}= 0 V, T_a=25℃, f(X_{IN})= 4 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			V
V_{OH}	"H" output voltage ϕ	V_{CC}=5V, I_{OH}=−2.5mA		3			V
		V_{CC}=3V, I_{OH}=−0.8mA		2			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$	V_{CC}=5V, I_{OH}=−12mA		3			V
		V_{CC}=3V, I_{OH}=−3mA		2			V
V_{OL}	"L" output voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	V
V_{OL}	"L" output voltage ϕ	V_{CC}=5V, I_{OL}=2.5mA				2	V
		V_{CC}=3V, I_{OL}=0.8mA				1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_0/\overline{INT_2}$, $P3_1/\overline{INT_1}$	use as interrupt input	V_{CC}=5V	0.3		1	V
			V_{CC}=3V	0.15		0.7	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5	0.7	V
		V_{CC}=3V			0.35		V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$/CLK	use as CLK input	V_{CC}=5V	0.3		1	V
			V_{CC}=3V	0.15		0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}	V_{CC}=5V		0.1		0.5	V
		V_{CC}=3V		0.06		0.3	V
$V_{T+}-V_{T-}$	Hysteresis X_{CIN}	V_{CC}=5V		0.1		0.5	V
		V_{CC}=3V		0.06		0.3	V
I_{IL}	"L" input current $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_I=0V without pull-up T_r.	V_{CC}=5V			−5	μA
			V_{CC}=3V			−4	μA
		V_I=0V, with pull-up T_r.	V_{CC}=5V	−35	−70	−140	μA
			V_{CC}=3V	−12	−25	−40	μA
I_{IL}	"L" input current IN_0~IN_7	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−4	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}, R_0~R_3	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−4	μA
I_{IL}	"L" input current $P2_0$~$P2_7$	V_I=0V				−5	μA
		V_I=V_{CC}−36V				−30	μA
I_{IH}	"H" input current $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_I=5V, without pull-up transistor				5	μA
I_{IH}	"H" input current IN_0~IN_7	V_I=5V, not use as analog input				5	μA
I_{IH}	"H" input current $P2_0$~$P2_7$	reading operation V_I=5V				100	μA
		normal operation V_I=5V				5	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}, R_0~R_3	V_I=5V				5	μA
I_{IH}	"H" input current V_{REF}	V_I=5V				5	mA
I_{OL}	"L" output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$	V_P=V_{CC}−36V, V_{OL}=V_{CC}		150	500	900	μA
I_{CC}	Supply current	Open output ports, V_P=V_{CC}, input port is V_{SS}, at normal operation.	X_{IN}=4MHz, V_{CC}=5V		3	6	mA
			X_{IN}=1MHz, V_{CC}=3V		0.4		mA
		Open output ports, V_P=V_{CC}, input port is V_{SS}, at wait mode.	X_{IN}=4MHz, V_{CC}=5V		1		mA
			X_{IN}=1MHz, V_{CC}=3V		0.2		mA
		Open output ports, V_P=V_{CC}, input port is V_{SS}, at normal operation, stop X_{IN} and X_{OUT}, X_{CIN}=32kHz.	V_{CC}=5V		60	200	μA
			V_{CC}=3V		25		μA
		Open output ports, V_P=V_{CC}, input port is V_{SS}, at wait mode, stop X_{IN} and X_{OUT}, X_{CIN}=32kHz.	V_{CC}=5V		40		μA
			V_{CC}=3V		15		μA
		Stop all oscillation.	T_a=25℃, V_{CC}=5V		0.1		μA
			T_a=25℃, V_{CC}=3V		0.06		μA
			T_a=70℃, V_{CC}=5V		1	10	μA
			T_a=70℃, V_{CC}=3V		0.6		μA
I_{ACC}	Supply current for A-D	at A-D converting time			2	4	mA

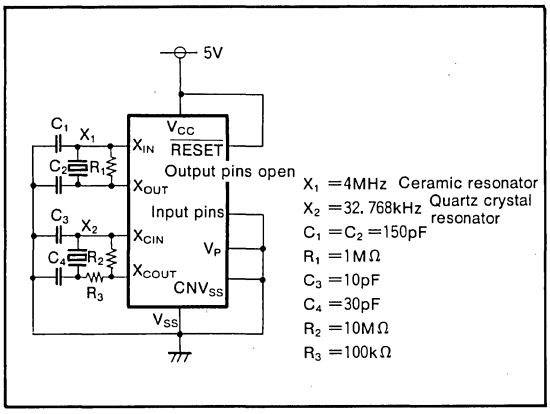


Fig.23 Test circuit for measuring supply current

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	bits
—	Absolute accuracy	V_{CC}=AV_{CC}=V_{REF}=5.12V			±3	LSB
R_{LADDER}	Ladder resistor value		1			kΩ
t_{CONV}	Conversion time	High-speed : ϕ=1MHz			72	μs
		Low-speed : ϕ=1MHz			288	μs
V_{REF}	Reference input voltage				V_{CC}	V
V_{IA}	Analog input voltage				V_{REF}	V

TIMING REQUIREMENTS

Single-chip mode (V_{CC}= 5 V±10%, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless other wise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		270			ns
$t_{su(RD-\phi)}$	Port R input setup time		270			ns
$t_{su(IND-\phi)}$	Port IN input setup time		270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		20			ns
$t_{h(\phi-RD)}$	Port R input hold time		20			ns
$t_{h(\phi-IND)}$	Port IN input hold time		20			ns
$t_{C(X_{IN})}$	External clock input cycle time (X_{IN})		230			ns
$t_{W(X_{IN})}$	External clock input pulse width (X_{IN})		75			ns
$t_{C(X_{CIN})}$	External clock input cycle time (X_{CIN})		2			ms
$t_{W(X_{CIN})}$	External clock input pulse width (X_{CIN})		1			ms
t_r	External clock rising edge time				25	ns
t_f	External clock falling edge time				25	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 25			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig. 24			230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				230	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 25			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig. 24			250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P4_0Q)}$	Port $P4_0$ data output delay time				200	ns
$t_{d(\phi-P4_0QF)}$	Port $P4_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P4_1Q)}$	Port $P4_1$ data output delay time				200	ns
$t_{d(\phi-P4_1QF)}$	Port $P4_1$ data output delay time				200	ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 25			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig. 24			250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

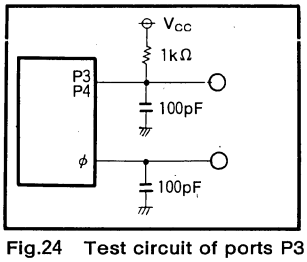


Fig.24 Test circuit of ports P3 and P4

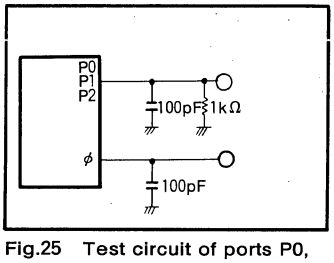
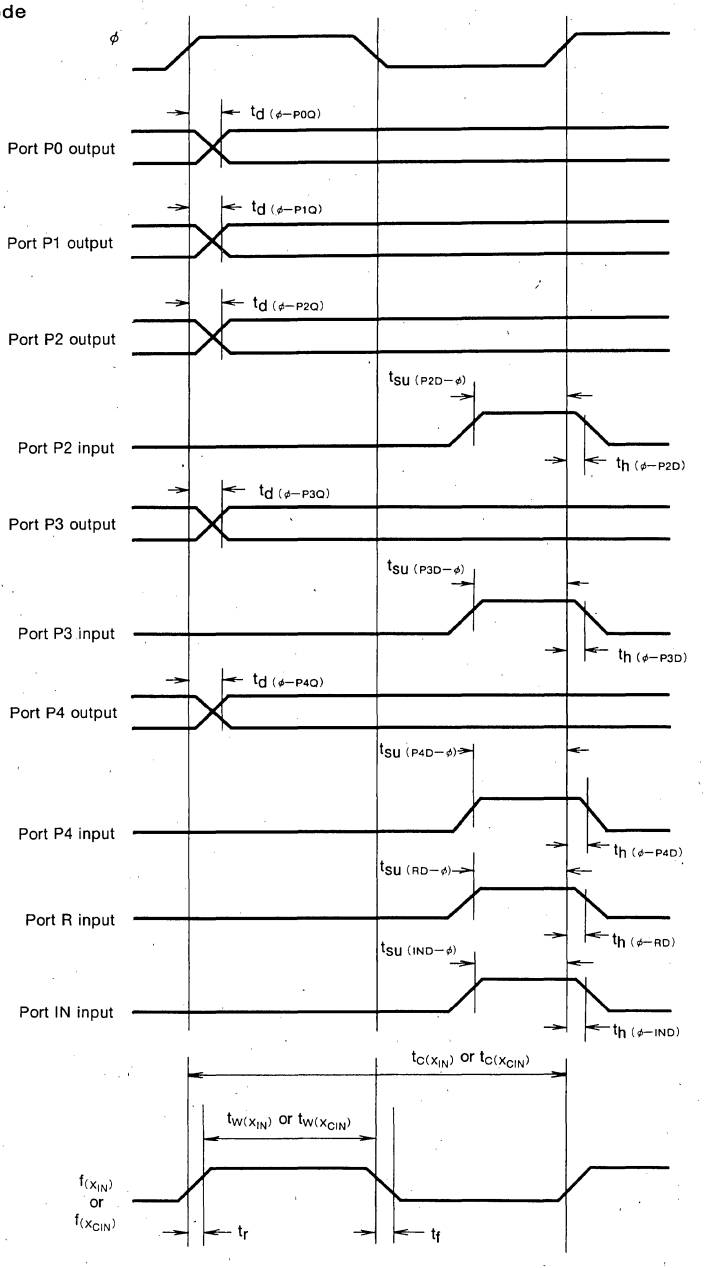


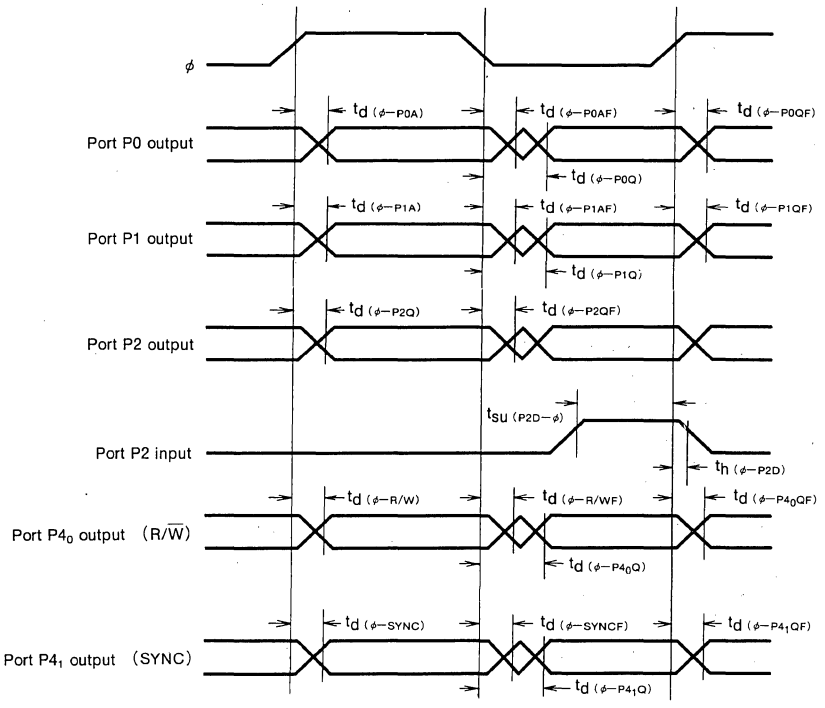
Fig.25 Test circuit of ports P0, P1, and P2

TIMING DIAGRAMS

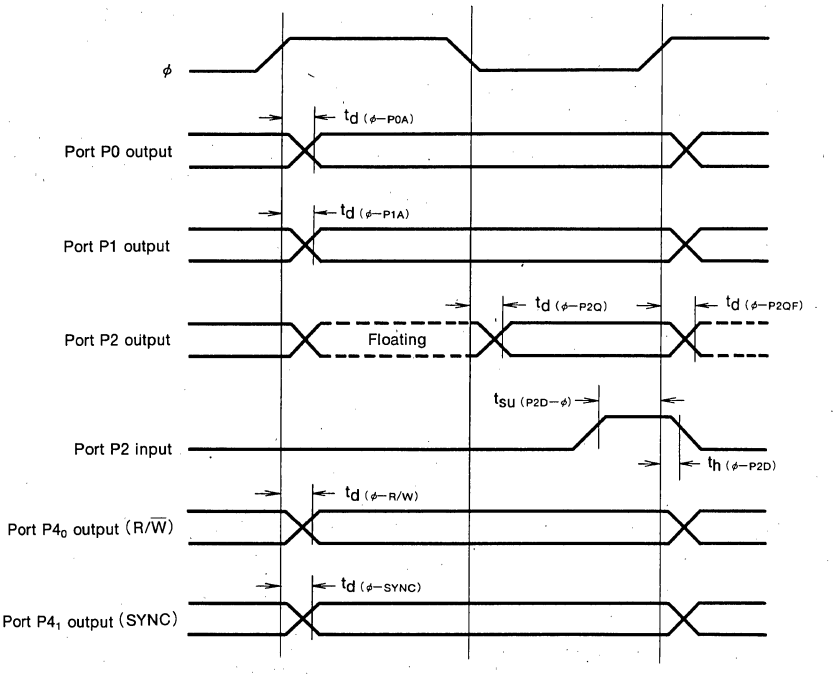
In single-chip mode



In memory expanding mode and eva-chip mode



In microprocessor mode



M50943-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50943-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP (flat package type also available). This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50943-XXXSP and the M50943-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

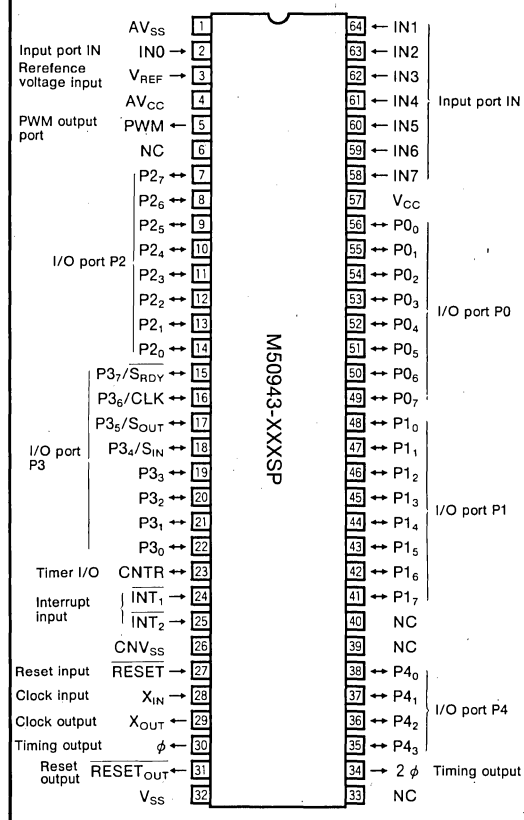
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 8192 bytes
  RAM ..... 192 bytes
- Instruction execution time
  ..... 1 μs (minimum instructions at 8MHz frequency)
- Single power supply f(X_{IN})=8MHz ..... 5V$\pm$10%
- Power dissipation
  normal operation mode (at 8MHz frequency) 30mW
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 8 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as A-D or serial I/O)
- Programmable I/O ports (Ports P0, P1, P2, P3, P4) 36
- Input ports (Port IN) 8
- Serial I/O (8-bit) 1
- A-D converter ..... 8-bit successive approximation
- PWM function 1

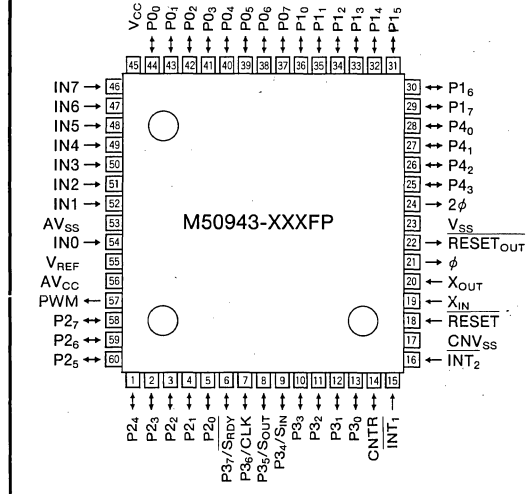
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment
Camera, Air conditioner

PIN CONFIGURATION (TOP VIEW)

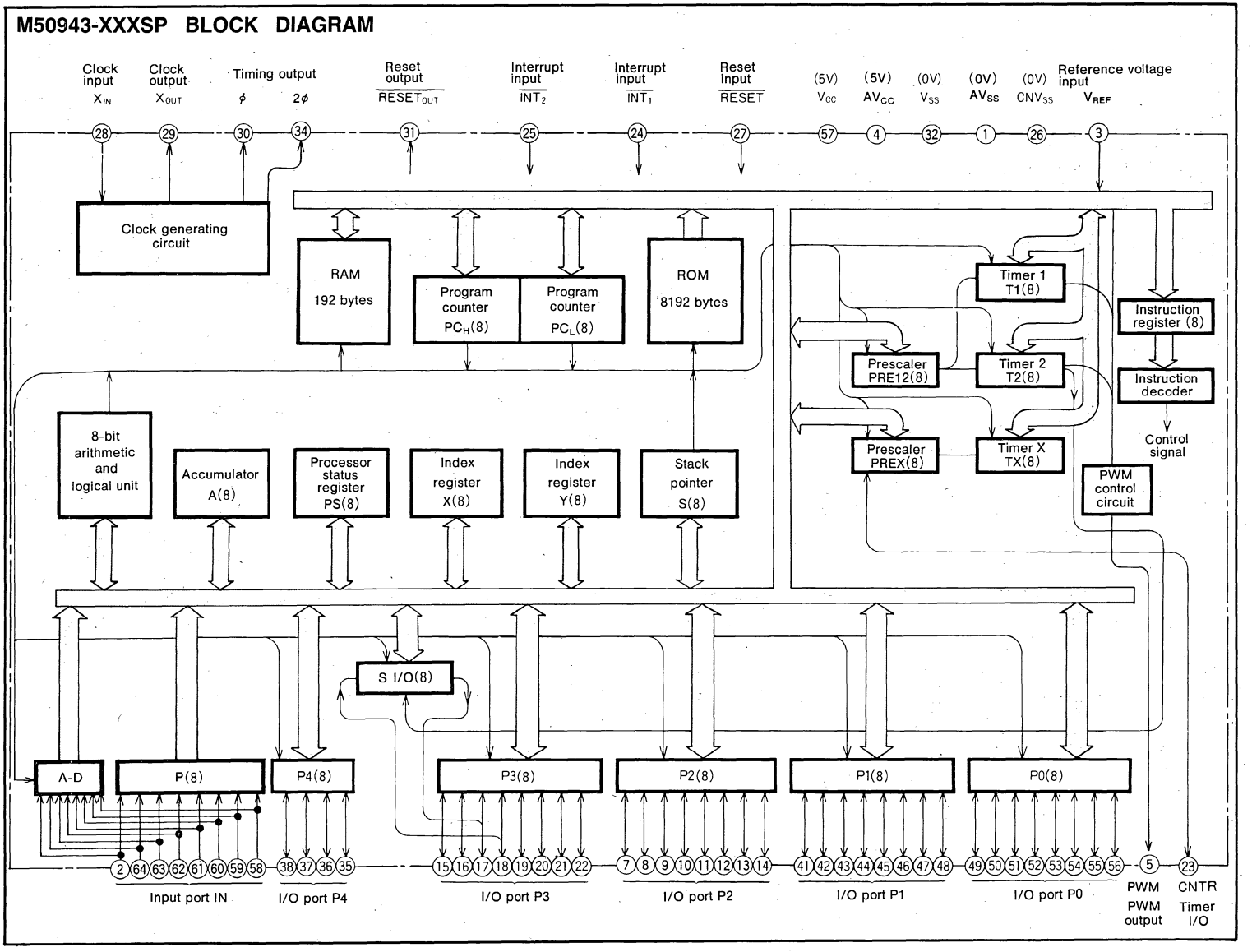


Outline 64P4B



Outline 60P6 NC : No connection

M50943-XXXSP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONS OF M50943-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 8MHz frequency)
Clock frequency			8MHz
Memory size	ROM		8192bytes
	RAM		192bytes
Input/Output ports	$\overline{INT_1}$, $\overline{INT_2}$	Input	1-bit×2
	P0, P1, P2, P3, P4	I/O	4-bit×1 (P4)
			8-bit×4 (a part of P3 are common with serial I/O)
	IN	Input	8-bit×1 (input, and analog input for A-D)
	CNTR	I/O	1-bit×1
Serial I/O			8-bit×1
Timers			8-bit prescaler×2+8-bit timer×3 (2 when A-D conversion or serial I/O is used)
Subroutine nesting			96 levels (max.)
Interrupts			Two external interrupts, Three internal timer interrupts (2 of timer interrupts are in common with A-D conversion and serial I/O)
Clock generating circuit			Built-in (ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	at high-speed operation		30mW (at 8MHz frequency)
Input/Output characteristics	Input/Output voltage		5V
	output current		10mA (ports P0, P1, P2, P3, P4)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M50943-XXXSP		64-pin shrink plastic molded DIP
	M50943-XXXFP		60-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ, 2ϕ	Timing output	Output	This is the timing output pins.
CNTR	Timer I/O	I/O	This is an output pin for the timer X.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$\overline{INT_2}$	Interrupt input	Input	This is the lowest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
PWM	PWM output	Output	This is output pin from the pulse width modulator. The output structure is N-channel open drain.
IN0~IN7	Analog input port IN	Input	This is an 8-bit analog input port for the A-D converter, and can be used as normal input port.
$\overline{RESET_{OUT}}$	Reset output	Output	This pin outputs the reset signal for peripheral devices.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.
AV_{CC}	Voltage input for A-D		This is the power supply input pin for the A-D converter.
AV_{SS}	Voltage input for A-D		This is GND input pin for the A-D converter.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50943-XXXSP is shown in Figure 1. Addresses $E000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 8192 bytes.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $00BF_{16}$ are assigned to the built-in RAM and consist of 192 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

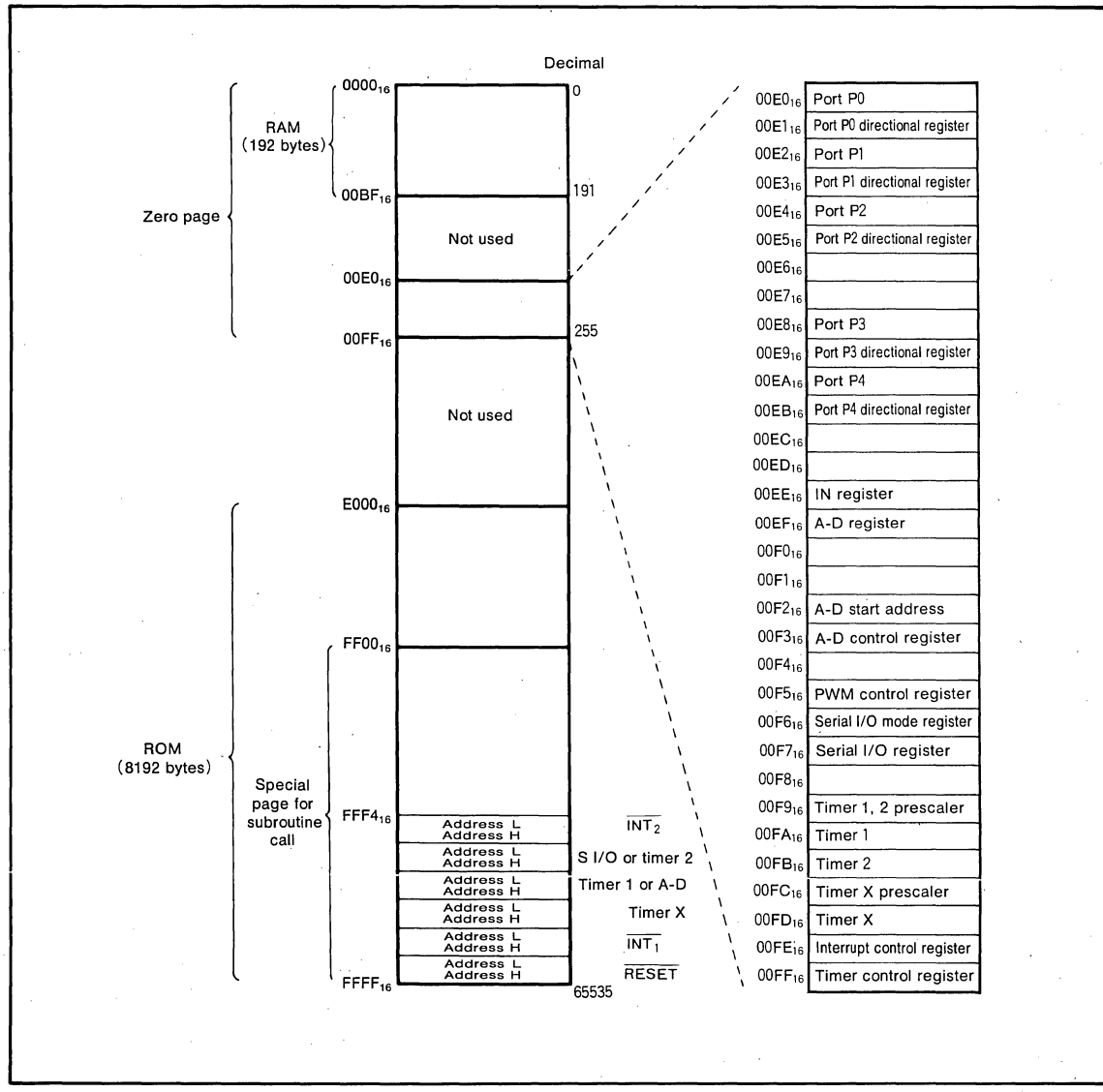


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

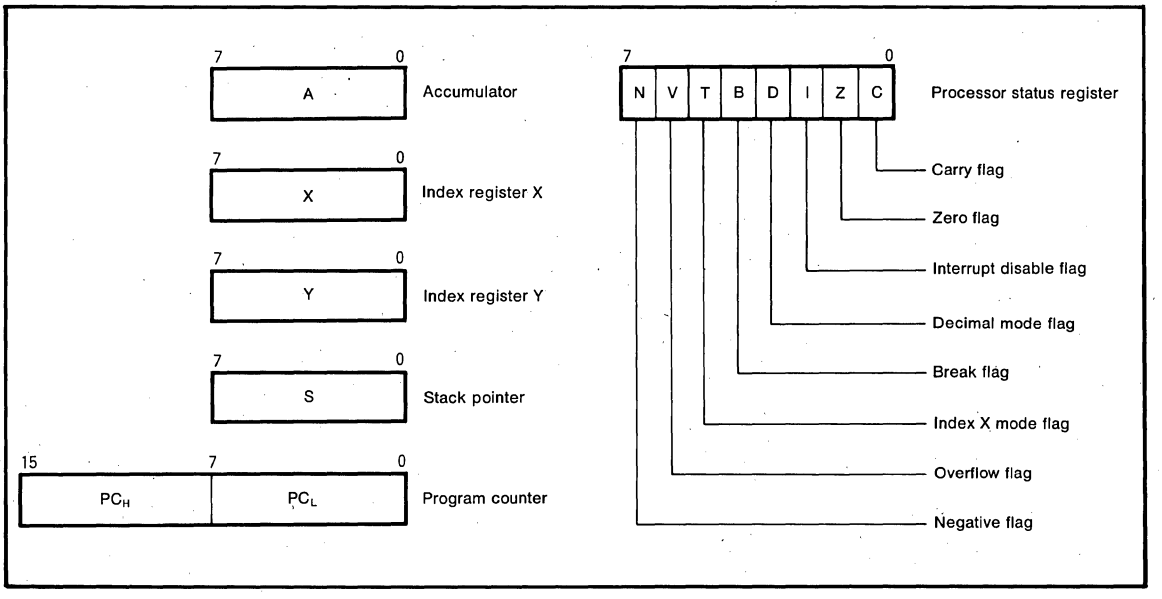


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The location of the stack can be determined by the stack page bit (bit 4 at address $00FF_{16}$). When bit 4 is "0" and the contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When bit 4 is "1", the stack address is set to $01XX_{16}$. When using this microcomputer in the single-chip mode, the stack page bit must be "0" and the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{INT_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1 or A-D	4	$FFF9_{16}$, $FFF8_{16}$
Timer 2 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{INT_2}$ (BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50943-XXXSP can be interrupted from seven sources; $\overline{INT_1}$, timer X, timer 1/A-D, timer 2/serial I/O, or $\overline{INT_2}$/BRK instruction.

The value of bit 2 of the serial I/O mode register (address $00F6_{16}$) determine whether the interrupt is from timer 2 or from serial I/O. When bit 2 is "0" the interrupt is from timer 3, and when bit 2 is "1" the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. The value of bit 3 of the A-D control register (address $00F3_{16}$) determine whether the interrupt is from timer 1 or from A-D converter. When bit 3 is "0" the interrupt is from timer 1, and when bit 3 is "1" the interrupt is from A-D converter. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupts are inhibited when the interrupt disable flag I is set

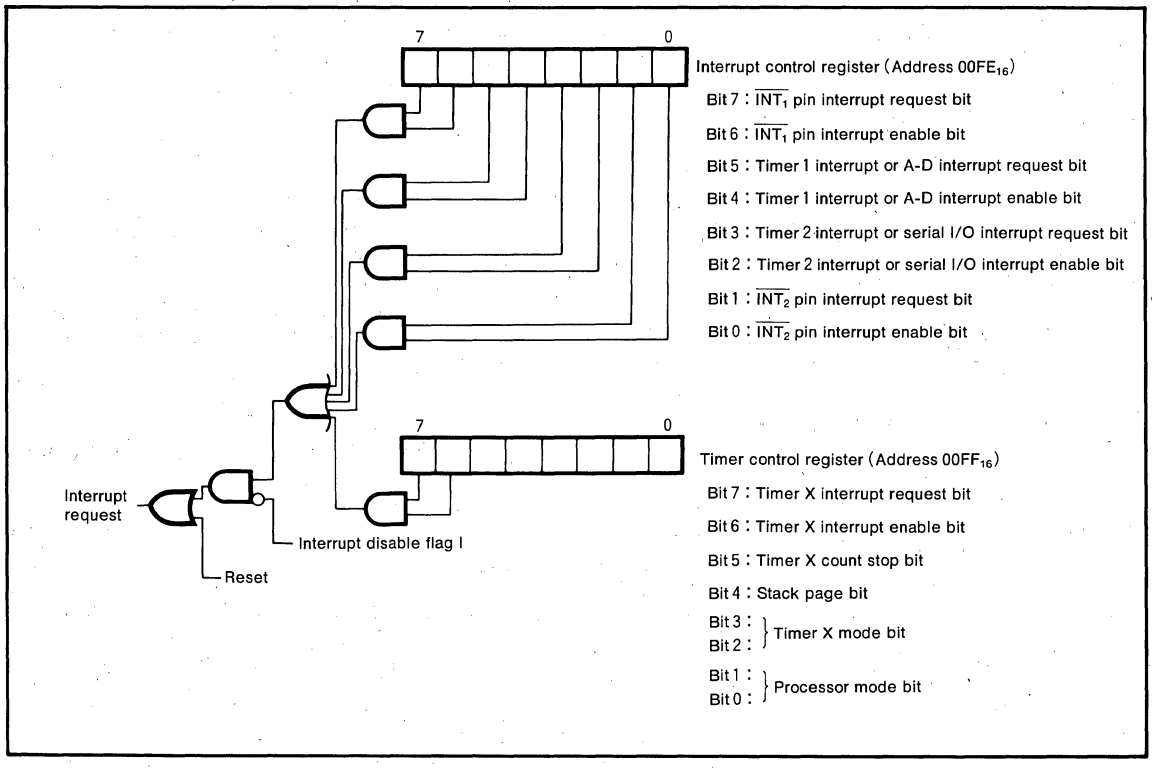


Fig. 3 Interrupt control

to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"
(2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"
(3) When the A-D conversion ends

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

TIMER

The M50943-XXXSP has three timers; timer X, timer 1, and timer 2. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section). Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1 and timer 2 is shown in Figure 4.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All three timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and

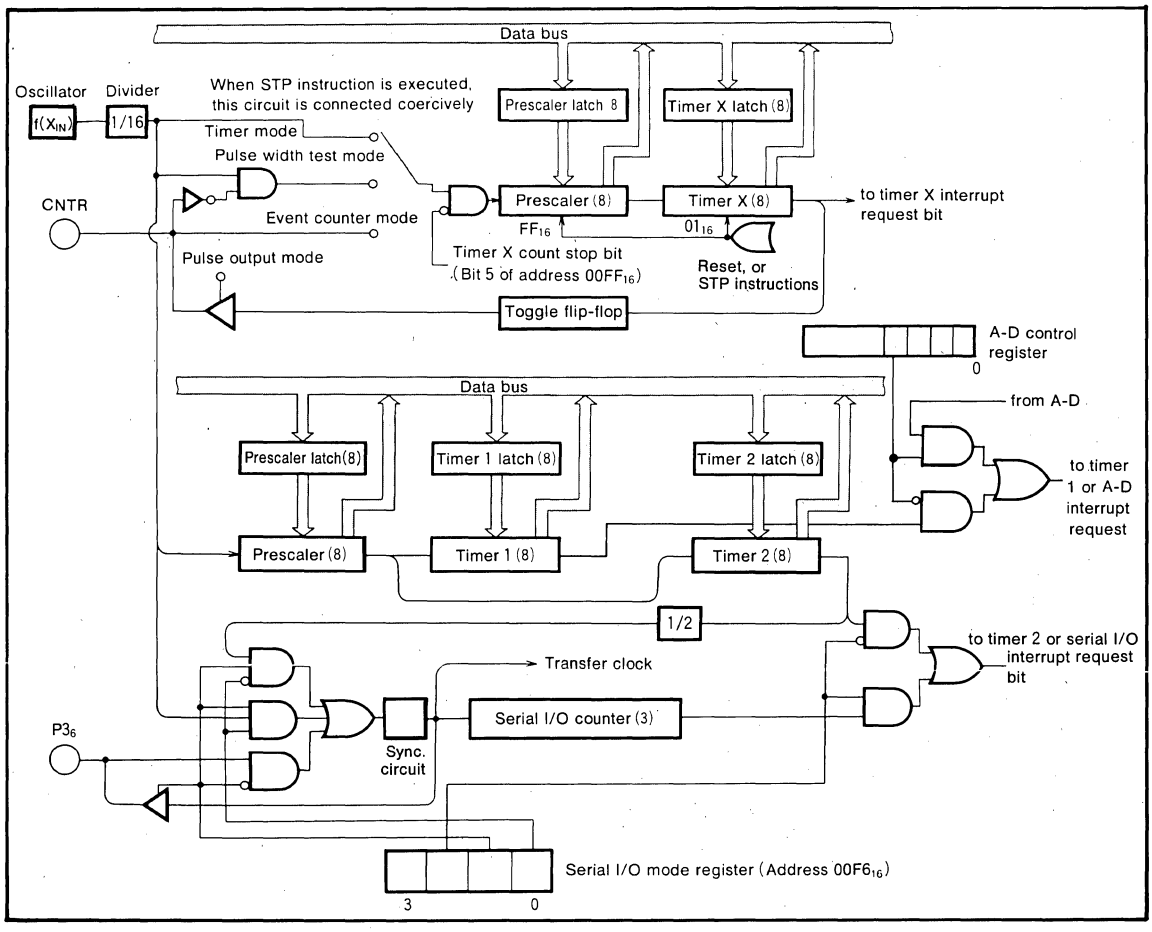


Fig.4 Block diagram of timer X, timer 1, and timer 2

timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section). The prescaler latch and timer latch can be loaded with any number except zero.

The four modes of timer X as follows:

(1) Timer mode [00]

In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]

In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]

This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock source.

(4) Pulse width measurement mode [11]

This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

To use timer 1 and timer 2, set the bit 0 of the PWM control register to "0". For more details, refer to PWM section.

The structure of the timer control register is shown in Figure 5.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

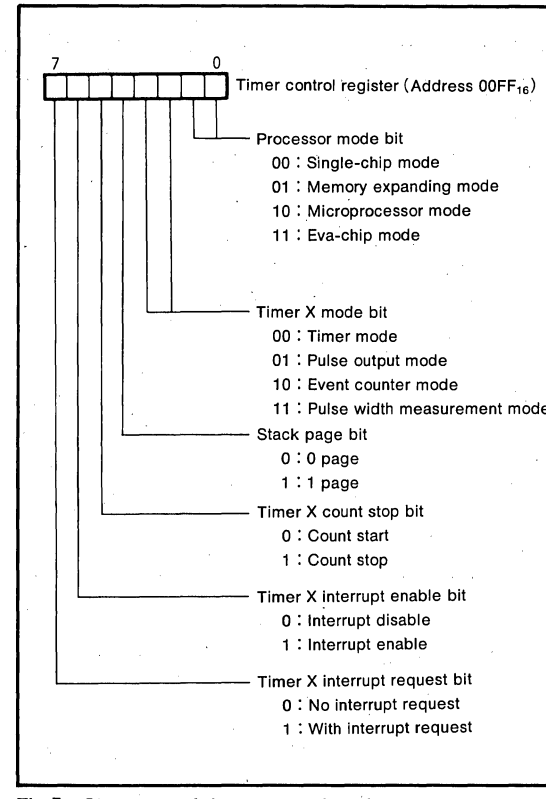


Fig.5 Structure of timer control register

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 6.

In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input /output clock (CLK), and the serial I/O pins (S_{OUT}, S_{IN}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F6_{16}$) is a 4-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 2, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the oscillator frequency divided by 16, becomes the clock.

Bit 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is a "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 2. Bit 3

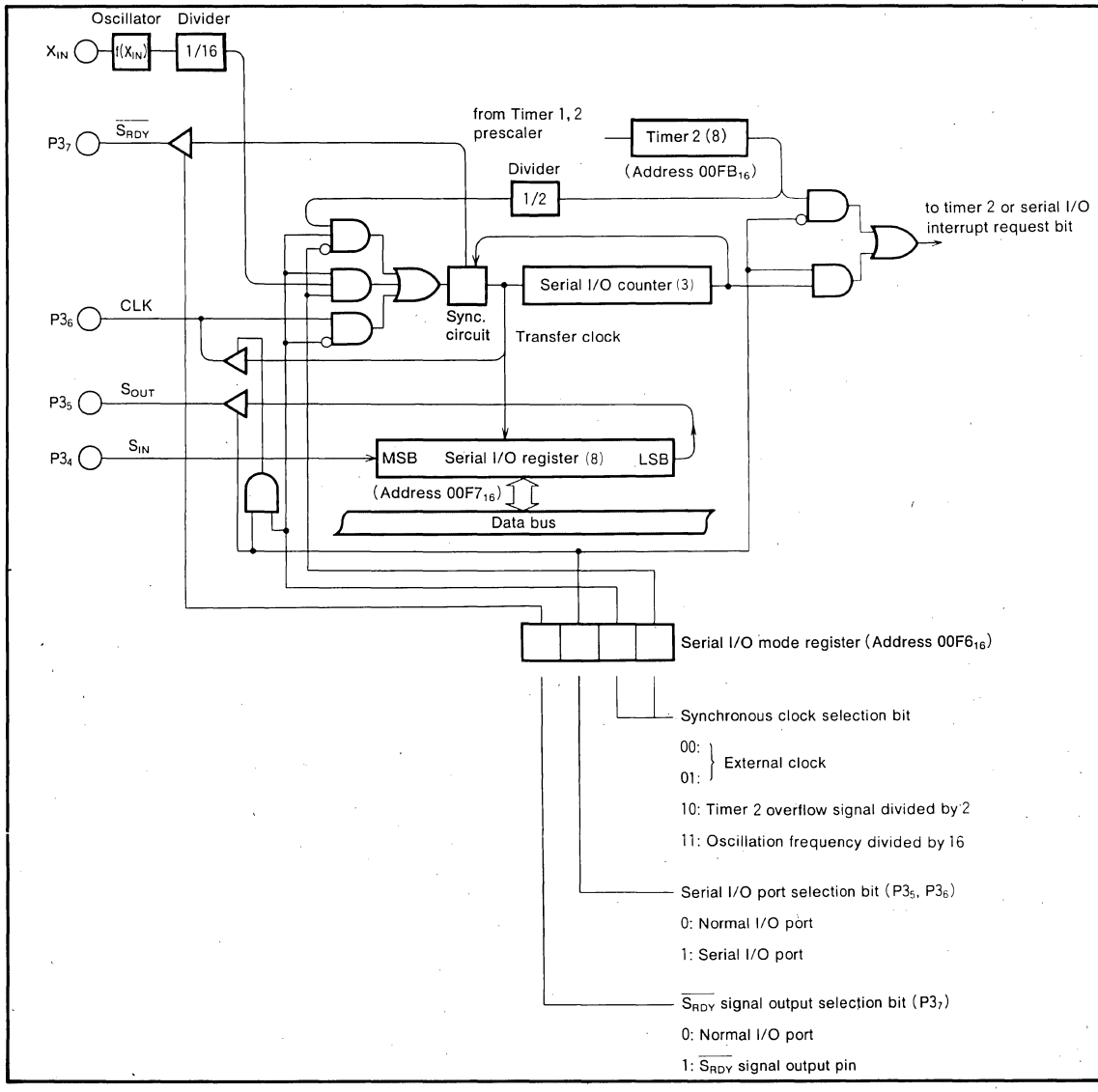


Fig.6 Block diagram of serial I/O

determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3=1, $\overline{S_{RDY}}$) or used as normal I/O pin (bit 3=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address $00F7_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50943-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrpt request bit will be set.

External Clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but the transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 7. An example of communication between two M50943-XXXSPs is shown in Figure 8.

For the port type of S_{OUT} ($P3_5$), N-channel open darain type or CMOS type can be selected by option. At the case of example of serial I/O connection-2, (Figure 9) N-channel open drain type must be selected.

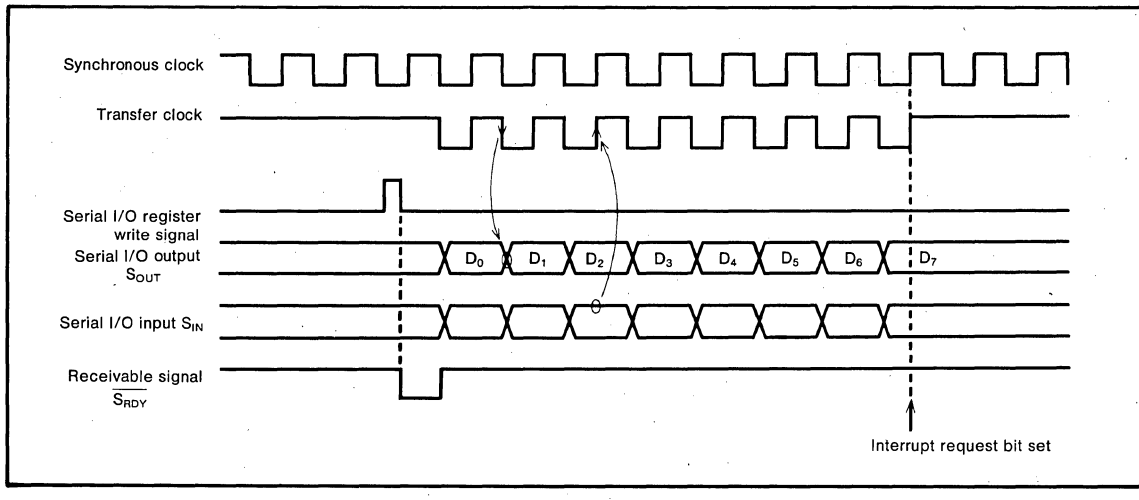


Fig.7 Serial I/O timing

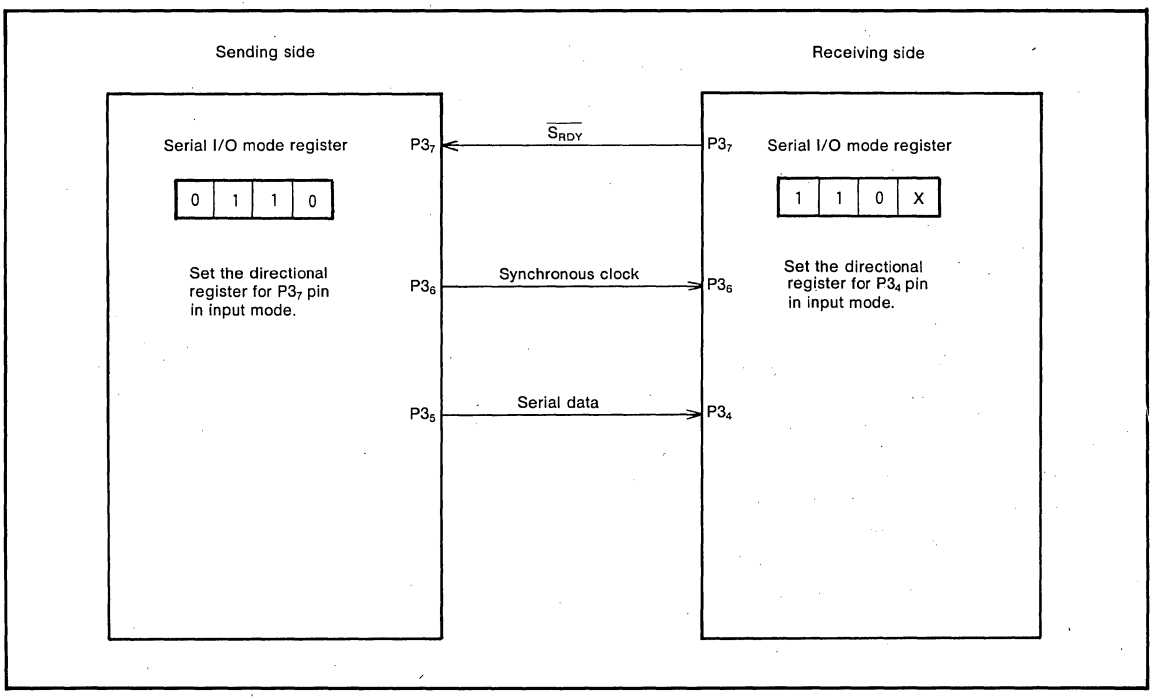


Fig.8 Example of serial I/O connection-1

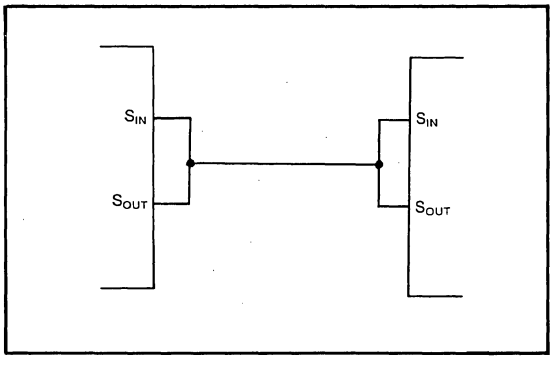


Fig.9 Example of serial I/O connection-2

A-D CONVERTER

The A-D converter circuit is shown in Figure 11. The analog input ports of the A-D converter (IN0~IN7) are in common with input ports of the data bus.

The 5-bit A-D control register is located at address $00F3_{16}$. One of the eight analog inputs is selected by bits 0, 1 and 2 of this register. Bit 3 selects the interrupt source, either from timer 1 or the A-D itself. If bit 3 is "0", then the interrupt request is from timer 1, if it is a "1", then it is from the A-D.

A-D conversion is accomplished by first selecting the analog channel (bit 0, 1 and 2) to be converted. Bit 3 should also be set to "1" to select the A-D as the interrupt source. The conversion is started when dummy data is written into address $00F2_{16}$. When the conversion is finished, an interrupt is generated by the A-D and the digital data can be read from the A-D register (address $00EF_{16}$). The end of the conversion is determined by an A-D interrupt request bit (address $00FF_{16}$).

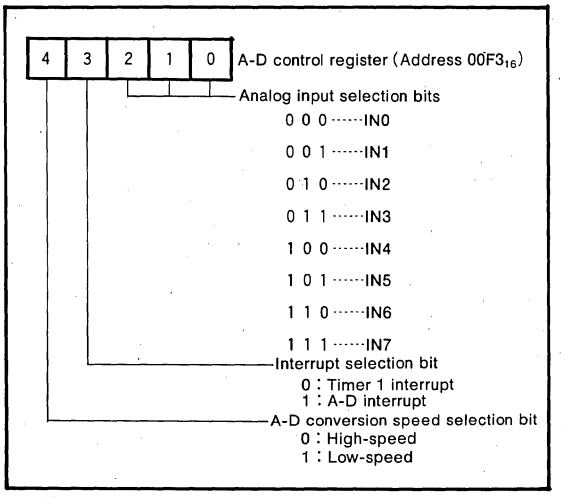


Fig.10 Structure of A-D control register

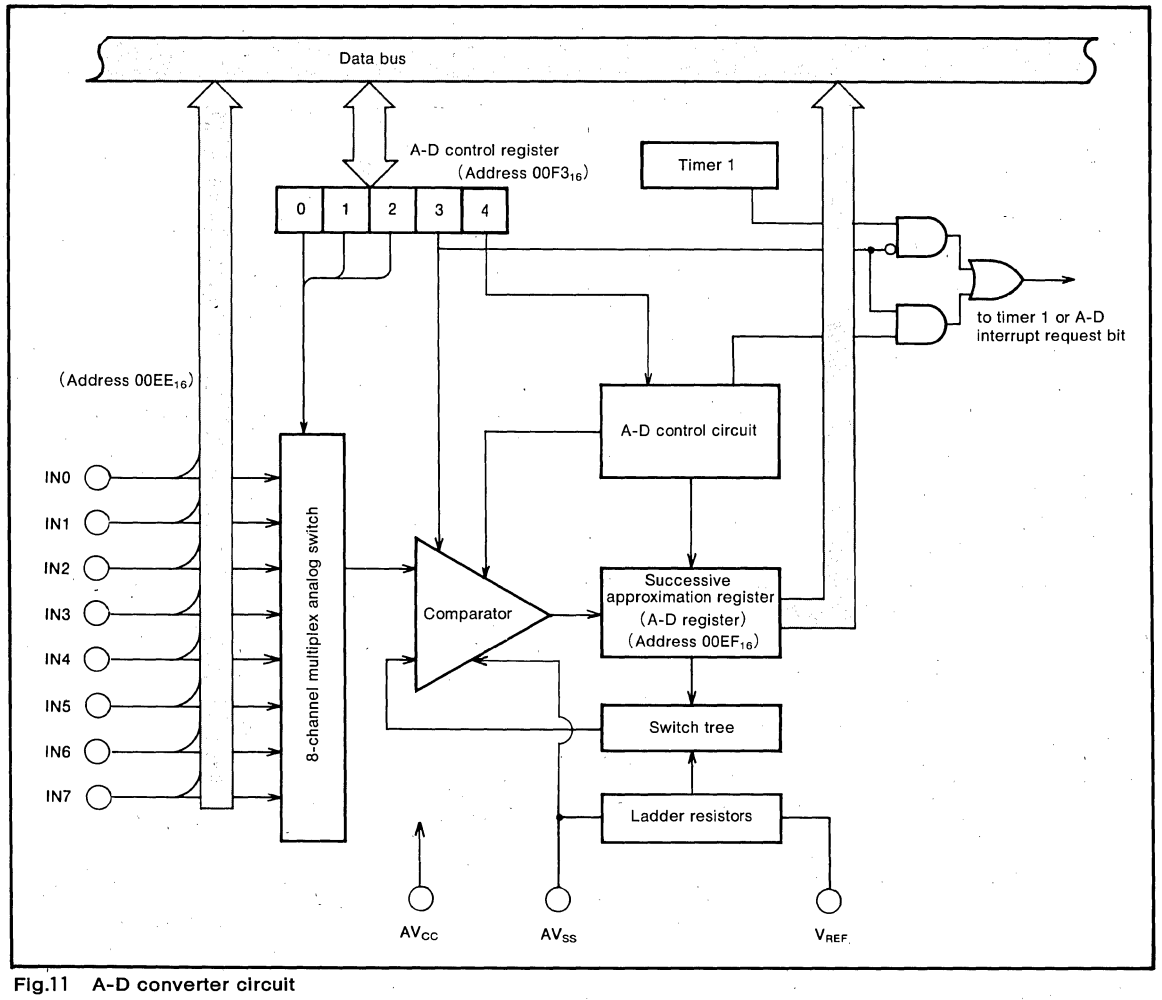


Fig.11 A-D converter circuit

MITSUBISHI ELECTRIC

The A-D conversion can also be programmed for high or low speed conversions. This is accomplished by using the A-D conversion speed switch bit (bit 4 of the A-D control register). If this bit is "0", then the speed is high (36μs at $f(X_{IN})=8MHz$). If it is "1", then it is low speed (144μs at $f(X_{IN})=8MHz$).

Port IN can also be used as an input port by reading data into address $00EE_{16}$. However, this cannot be done during A-D conversions.

The A-D control register is shown in Figure 10.

PWM

The M50943-XXXSP has a pulse width modulated (PWM) output control circuit. The circuit outputs a variable duty cycle signal that can be used for a programmable pulse width and frequency. Timers 1 and 2 are used for the PWM. The block diagram of the PWM is shown in Figure 12.

The PWM is composed of N-channel open drain transistors. When bit 0 of the PWM control register is "0", the output transistors are turned off. When timers 1 and 2 are not used for PWM control, they operate in the normal timer modes. When bit 0 of the PWM control register is "1", a rectangular wave is output according to the value set in timer 1 and 2 (Figure 13.). The clock source frequency for the PWM is the oscillator frequency divided by 16.

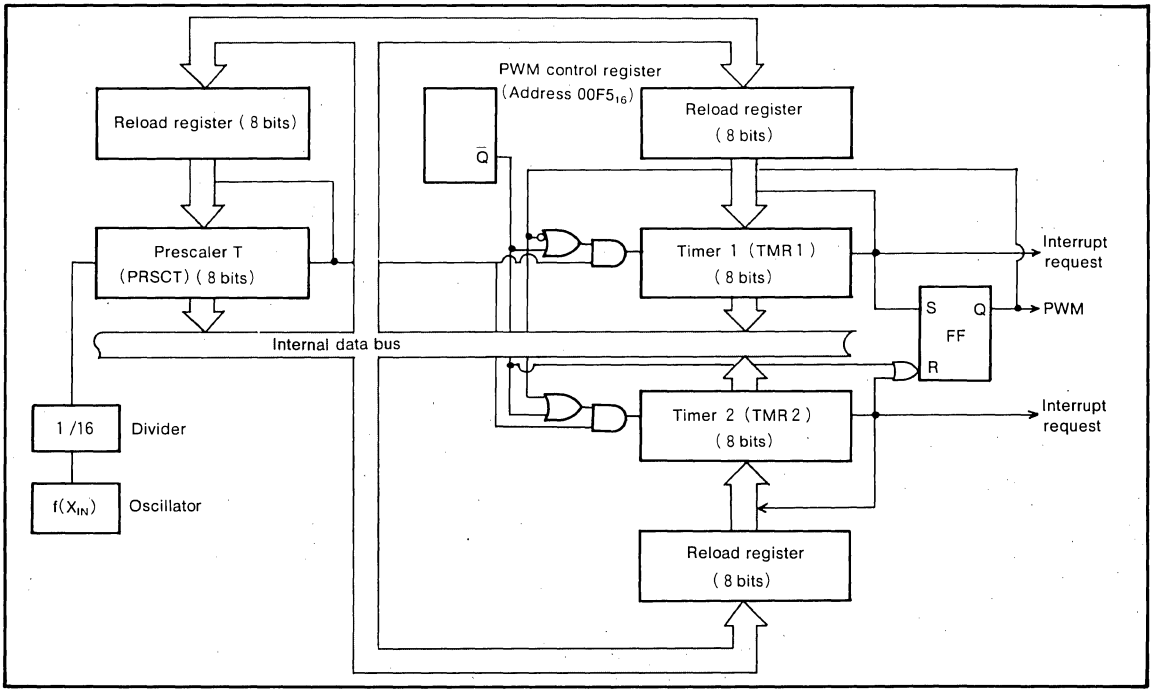


Fig.12 Block Diagram of PWM

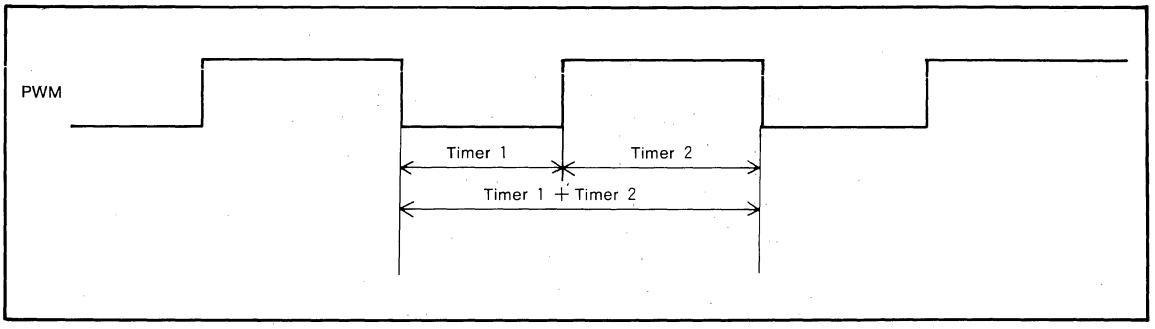


Fig.13 PWM rectangle wave form

RESET CIRCUIT

The M50943-XXXSP is reset according to the sequence shown in Figure 16. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than $2\mu s$ while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 15.

An example of the reset circuit is shown in Figure 14.
When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

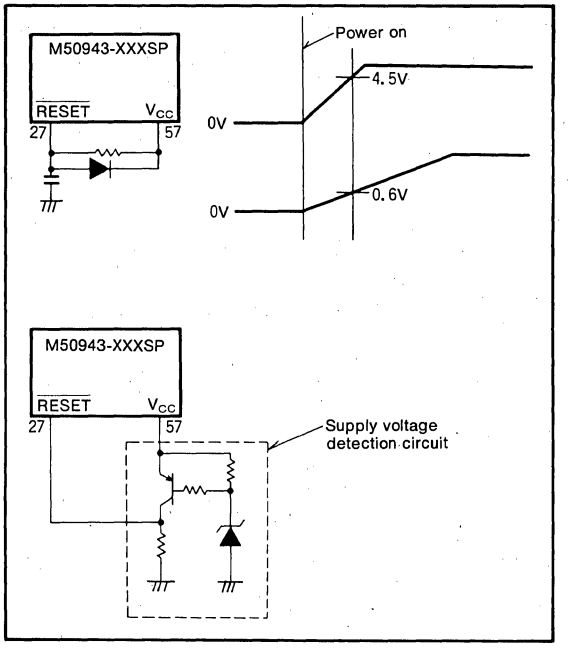


Fig.14 Example of reset circuit

			Address
(1)	Port P0 directional register	($E1_{16}$) ···	00_{16}
(2)	Port P1 directional register	($E3_{16}$) ···	00_{16}
(3)	Port P2 directional register	($E5_{16}$) ···	00_{16}
(4)	Port P3 directional register	($E9_{16}$) ···	00_{16}
(5)	Port P4 directional register	(EB_{16}) ···	00_{16}
(6)	Serial I/O mode register	($F6_{16}$) ···	0 0 0 0
(7)	Prescaler X	(FC_{16}) ···	FF_{16}
(8)	Timer X	(FD_{16}) ···	01_{16}
(9)	Interrupt control register	(FE_{16}) ···	00_{16}
(10)	Timer control register	(FF_{16}) ···	00_{16}
(11)	Interrupt disable flag on processor status register	(PS) ···	1
(12)	Program counter	(PC_H) ···	Contents of address $FFFF_{16}$
		(PC_L) ···	Contents of address $FFFE_{16}$
(13)	A-D control register	($F3_{16}$) ···	0 0 0 0 0
(14)	PWM control register	($F5_{16}$) ···	0

Fig.15 Internal state of microcomputer at reset

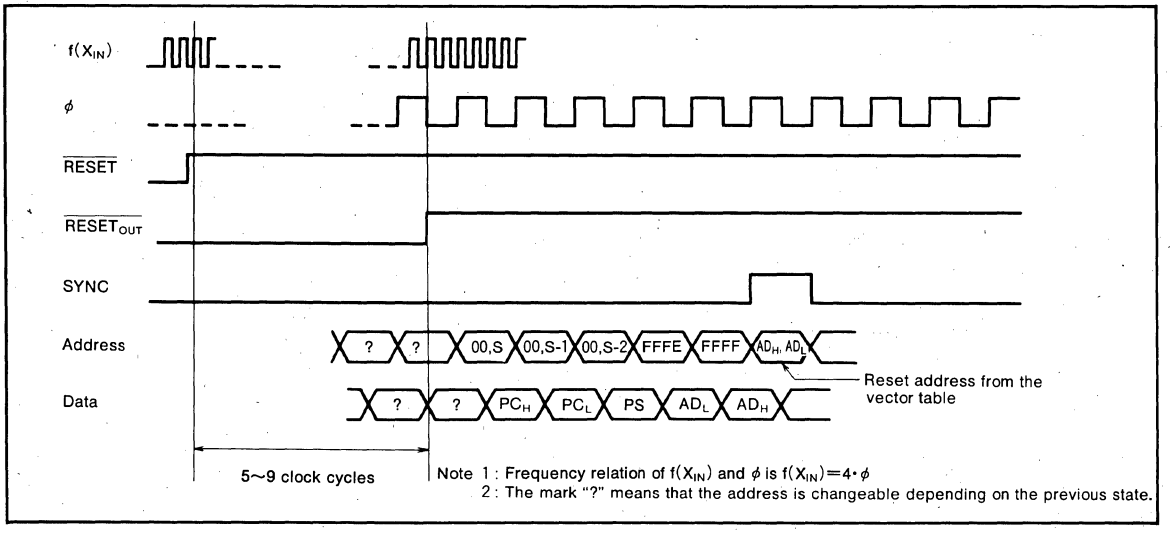


Fig.16 Timing diagram at reset

MITSUBISHI ELECTRIC

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

Pull-up transistor can be specified as an option. As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as serial I/O pins. For more details, see the processor mode information.

The output type of port $P3_5$ can be specified N-channel open drain output as an option.

(5) Port P4

Port P4 is a 4-bit I/O port with CMOS outputs. This port also has the pull-up transistor option.

(6) Clock 2ϕ output pin

In normal conditions, the oscillator frequency divided by two is output as 2ϕ.

(7) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ.

(8) $\overline{RESET_{OUT}}$ pin

When the $\overline{RESET}$ pin goes to level "L", the $\overline{RESET_{OUT}}$ pin also goes to "L". On the other hand, when the $\overline{RESET}$ pin goes to level "H", the $\overline{RESET_{OUT}}$ pin also goes to "H" after 5～9 clock cycles. This output is used to reset the external circuits.

(9) $\overline{INT_1}$ pin

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

(10) $\overline{INT_2}$ pin

The $\overline{INT_2}$ pin is an interrupt input pin. When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1".

(11) CNTR pin

The CNTR pin is an I/O pin of timer X. In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

(12) Port IN

Port IN is an 8-bit input port to the A-D converter. The input contents of the port can be read to as the contents of address $00EE_{16}$. The read operation must be inhibited during A-D conversion.

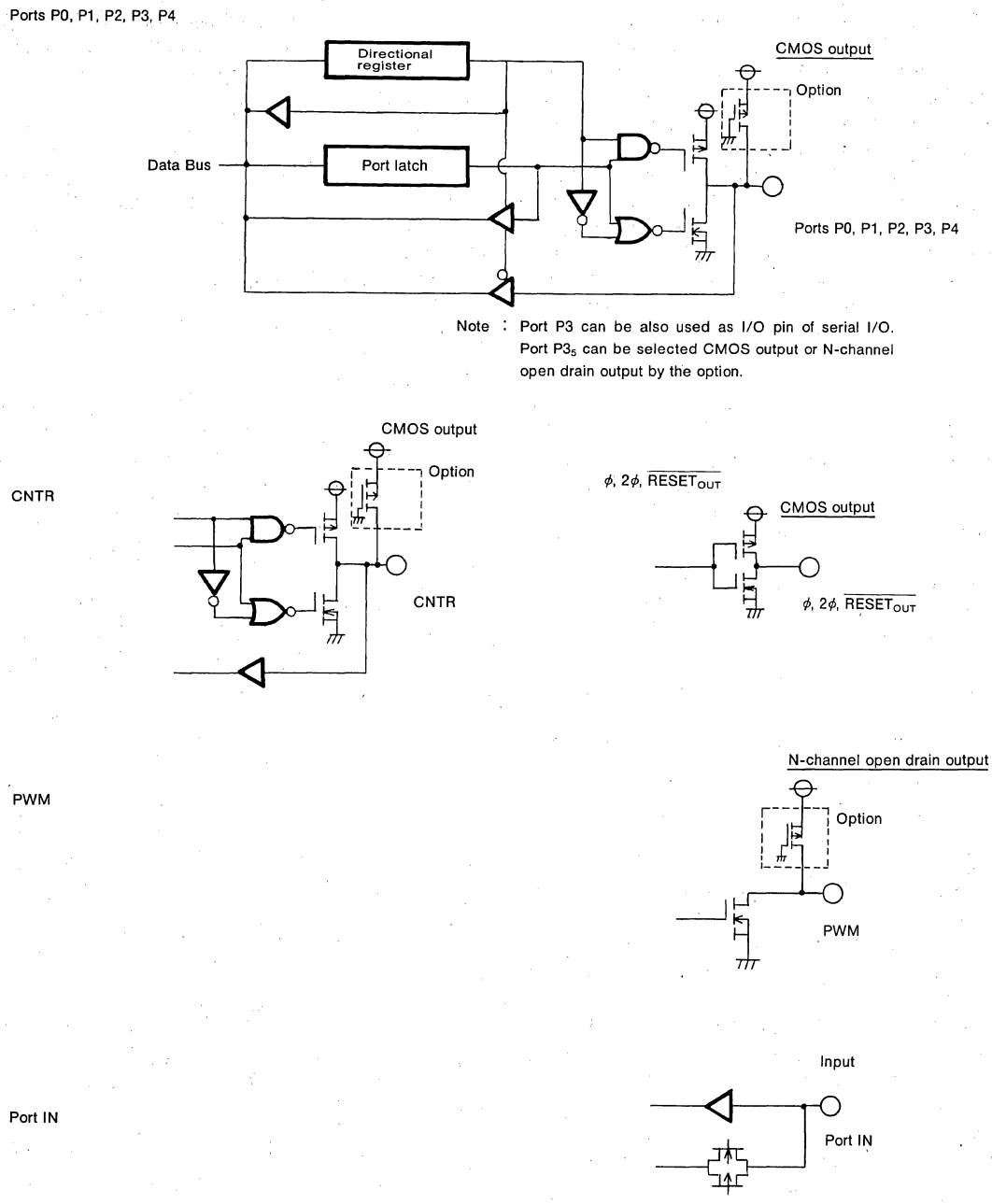


Fig.17 Block diagram of ports P0~P4 (in single-chip mode), and input and output formats of CNTR, ϕ, 2ϕ $\overline{\text{RESET}_{\text{OUT}}}$, PWM, port IN

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0 ~ P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 19 shows the functions of ports P0~P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 13.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

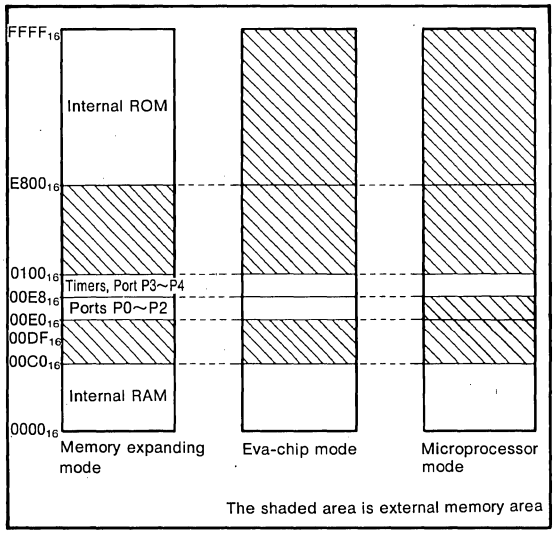


Fig.18 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0 ~ P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost. Port P2 becomes the data bus ($D_7 \sim D_0$) and loses its normal I/O functions. Port $P3_1$ and $P3_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode. With the exceptions that the internal ROM is disabled and that external memory must be attached in this mode, this mode is the same as the memory expanding mode.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is required.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original I/O functions while ϕ is at the "H" state, and works as a data bus of $D_7 \sim D_0$ (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_2$, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

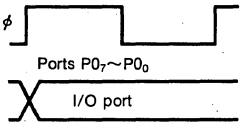
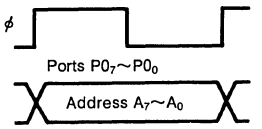
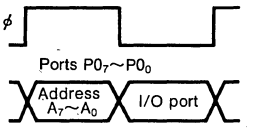
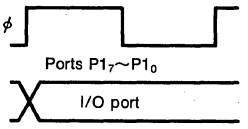
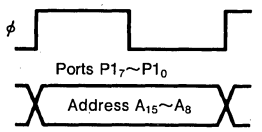
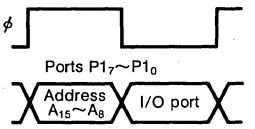
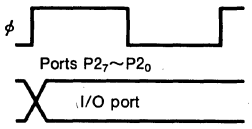
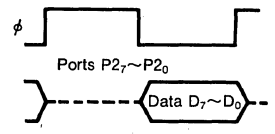
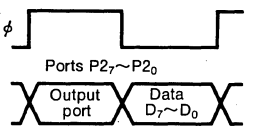
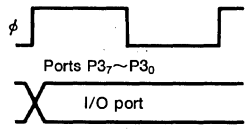
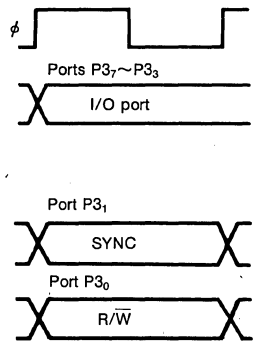
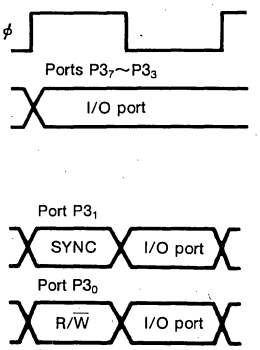
Port \ Mode	CM_1 = 0, CM_0 = 0 Single-chip mode	CM_1 = 0, CM_0 = 1 Memory expanding mode	CM_1 = 1, CM_0 = 0 Microprocessor mode	CM_1 = 1, CM_0 = 1 Eva-chip mode
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	
Port P3			Same as left	

Fig.19 Processor mode and functions of ports P0~P3

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 22.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleared when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 20.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufacturers suggested value.

The example of external clock usage is shown in Figure 21. X_{IN} is the input, and X_{OUT} must be open.

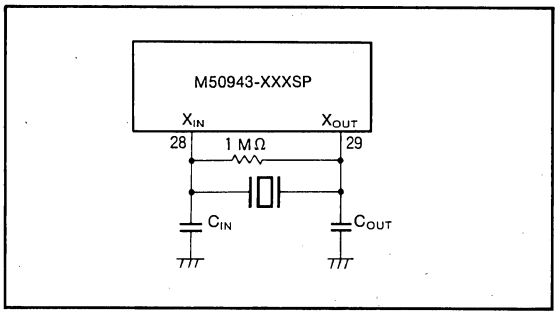


Fig.20 External ceramic reasonator circuit

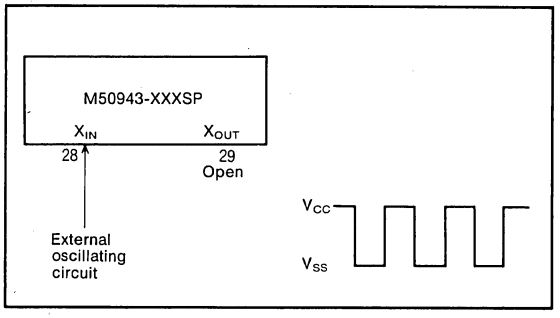


Fig.21 External clock input circuit

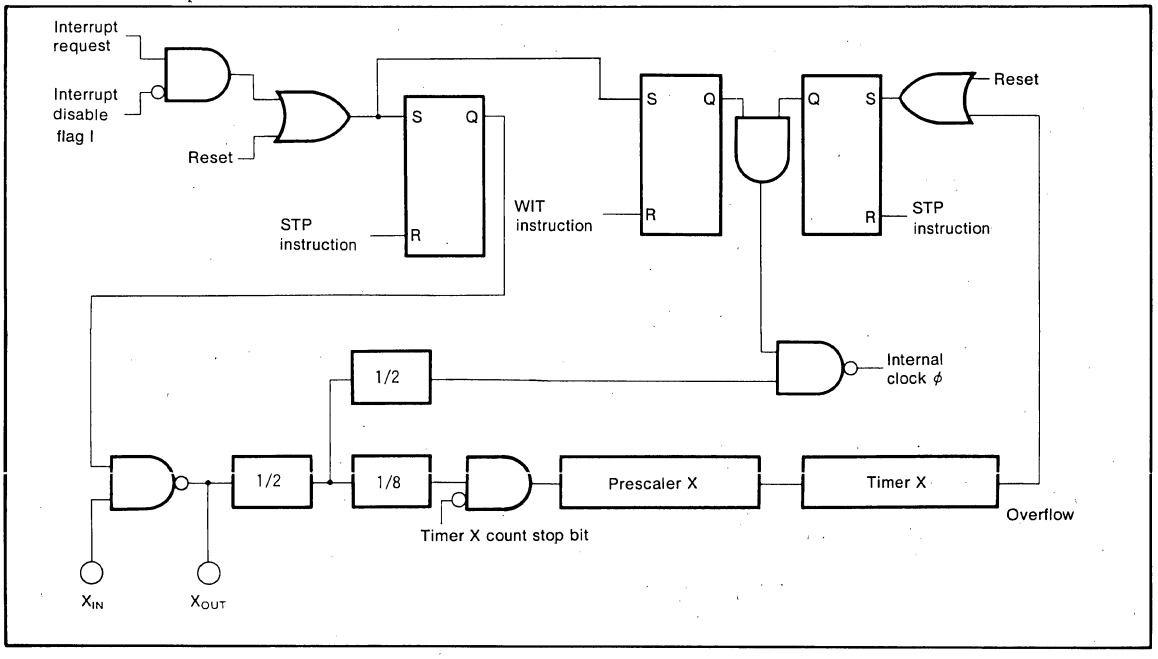


Fig.22 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).
(2) Set a value other than "0" for the timer and the prescaler.
(3) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(4) Reading the timer and the prescaler must be avoided while the input to the prescaler is changing.
(5) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(6) A NOP instruction must be used after the execution of a PLP instruction.
(7) Notes on serial I/O
① Set "0" in the serial I/O interrupt enable bit (bit 2 of address $00FE_{16}$) before setting the serial I/O mode.
② Insert at least one instruction and set "0" in the serial I/O interrupt request bit (bit 3 of address $00FE_{16}$) after setting the serial I/O mode.
③ Set "1" in the serial I/O interrupt enable bit after the operation described in ②.
(8) The timer X and prescaler X must be set "FF_{16}" immediately before the execution of a STP instruction.
(9) Notes on A-D conversion
① Set "0" in the A-D interrupt enable bit (bit 4 of address $00FE_{16}$) befor setting A-D conversion.
② Insert at least one instruction and set "0" in the A-D interrupt request bit (bit 5 of address $00FE_{16}$) after setting the A-D conversion.
③ Set "1" in the A-D interrupt enable bit after the operation described in ②.
④ Set "0" in bit 3 of the A-D control register (address $00F3_{16}$) before using a STP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ····· EPROM 3sets

Write the following option on the mask ROM confirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port P4 pull-up transistor bit
- Port PWM pull-up transistor bit
- Port CNTR pull-up transistor bit
- Port $P3_5$ (S_{OUT}) output type

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	−0.3～7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}, $\overline{INT_1}$, $\overline{INT_2}$		−0.3～7	V
V_I	Input voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$ $P3_0$～$P3_7$, $P4_0$～$P4_3$, CNTR IN0～IN7		−0.3～V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3～13	V
V_O	Output voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$ $P3_0$～$P3_7$, $P4_0$～$P4_3$, PWM, X_{OUT} ϕ, 2ϕ, $\overline{RESET_{OUT}}$, CNTR		−0.3～V_{CC}+0.3	V
P_d	Power dissipation	T_a=25℃	1000(Note 1)	mW
Topr	Operating temperature		−10～70	℃
Tstg	Storage temperature		−40～125	℃

Note 1 : 300mW for QFP type.

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10～70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$ $P3_0$～$P3_7$, $P4_0$～$P4_3$, IN0～IN7 CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$ X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$ $P3_0$～$P3_7$, $P4_0$～$P4_3$, IN0～IN7 CNTR, $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$～$P0_7$, $P1_0$～$P1_7$, PWM $P2_0$～$P2_7$, $P3_0$～$P3_7$ $P4_0$～$P4_3$, CNTR			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$～$P0_7$, $P1_0$～$P1_7$, PWM $P2_0$～$P2_7$, $P3_0$～$P3_7$ $P4_0$～$P4_3$, CNTR (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$～$P0_7$, $P1_0$～$P1_7$ $P2_0$～$P2_7$, $P3_0$～$P3_7$ $P4_0$～$P4_3$, CNTR			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$～$P0_7$, $P1_0$～$P1_7$ $P2_0$～$P2_7$, $P3_0$～$P3_7$ $P4_0$～$P4_3$, CNTR (Note 2)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			8	MHz

Note 2 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
3 : The total of $I_{OL(peak)}$ should be 80mA max, for ports P0, P1, P2, P3, P4, CNTR, and PWM.
The total of $I_{OH(peak)}$ should be 80mA max, for ports P0, P1, P2, P3, P4, and CNTR.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, CNTR	I_{OH}=−10mA (at $P3_5$ is CMOS output)	3			V
V_{OH}	"H" output voltage ϕ, 2ϕ, $\overline{RESET_{OUT}}$	I_{OH}=−2.5mA	3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, CNTR, PWM	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage ϕ, 2ϕ, $\overline{RESET_{OUT}}$	I_{OL}=5mA			2	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis CNTR, $\overline{INT_1}$, $\overline{INT_2}$		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, CNTR, PWM	V_I= 0 V without pull-up transistor			−5	μA
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, CNTR, PWM	V_I= 0 V with pull-up transistor	−40	−70	−125	μA
I_{IL}	"L" input current IN0~IN7	V_I= 0 V			−5	μA
I_{IL}	"L" input current $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	V_I= 0 V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, CNTR, PWM	V_I=5V			5	μA
I_{IH}	"H" input current IN0~IN7(at unselect)	V_I = 5 V			5	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	V_I = 5 V			5	μA
I_{IH}	"H" input current V_{REF}	V_I = 5 V			1	mA
I_{CC}	Supply current	Output pins are open, ports P0, P1, P2, P3 and P4 are connected to V_{CC}, all other input and I/O pins are connected to V_{SS}.		6	12	mA
I_{ACC}	Supply current for A-D	during A-D conversion		4	8	mA

A-D CONVERTER CHARACTERISTICS (V_{CC}=AV_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=5V, 5V≧V_{REF}≧3V			±3	LSB
R_{LADDER}	Ladder resistance value		5			kΩ
t_{CONV}	Conversion time				36/144	μs
V_{REF}	Reference input voltage		3		V_{CC}	V
V_{IA}	Analog input voltage				V_{REF}	V

TIMING REQUIREMENTS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	200			ns
$t_{su(IND-\phi)}$	Port IN input setup time	200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-IND)}$	Port IN input hold time	20			ns
t_C	External clock input cycle time	125			ns
t_W	External clock input pulse width	62			ns
t_r	External clock rising edge time			20	ns
t_f	External clock falling edge time			20	ns

Eva-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Memory expanding mode and microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	150			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.23			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				200	ns

Eva-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.23			150	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				150	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				150	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				150	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				150	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				150	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				150	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				150	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				150	ns

Memory expanding mode and microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.23			150	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time		30		150	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				150	ns

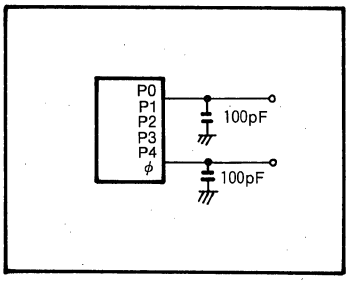
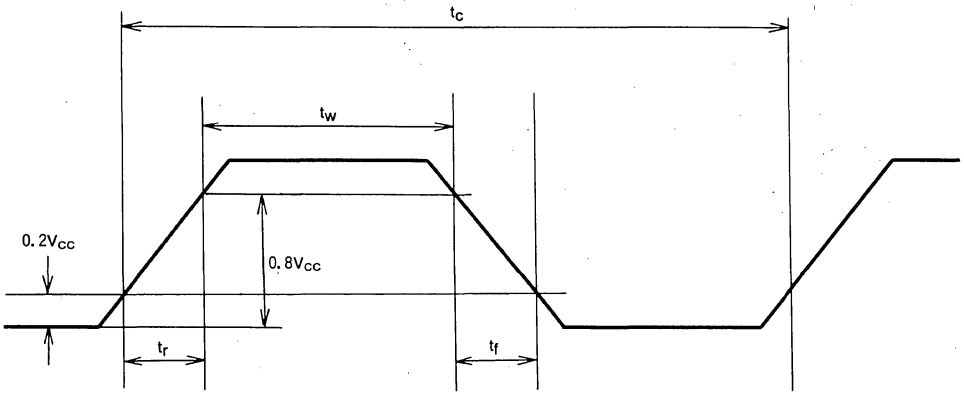


Fig.23 Ports P0～P4 test circuit

2ϕ PIN AC CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, $f_{(X_{IN})}$=8MHz, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_C	Clock output cycle time	Fig.24		250		ns
t_W	Clock output pulse width		25			ns
t_r	Clock rising time				75	ns
t_f	Clock falling time				50	ns

Timing diagram of 2ϕ



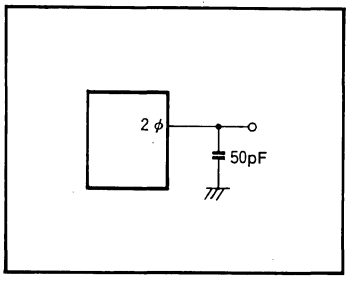
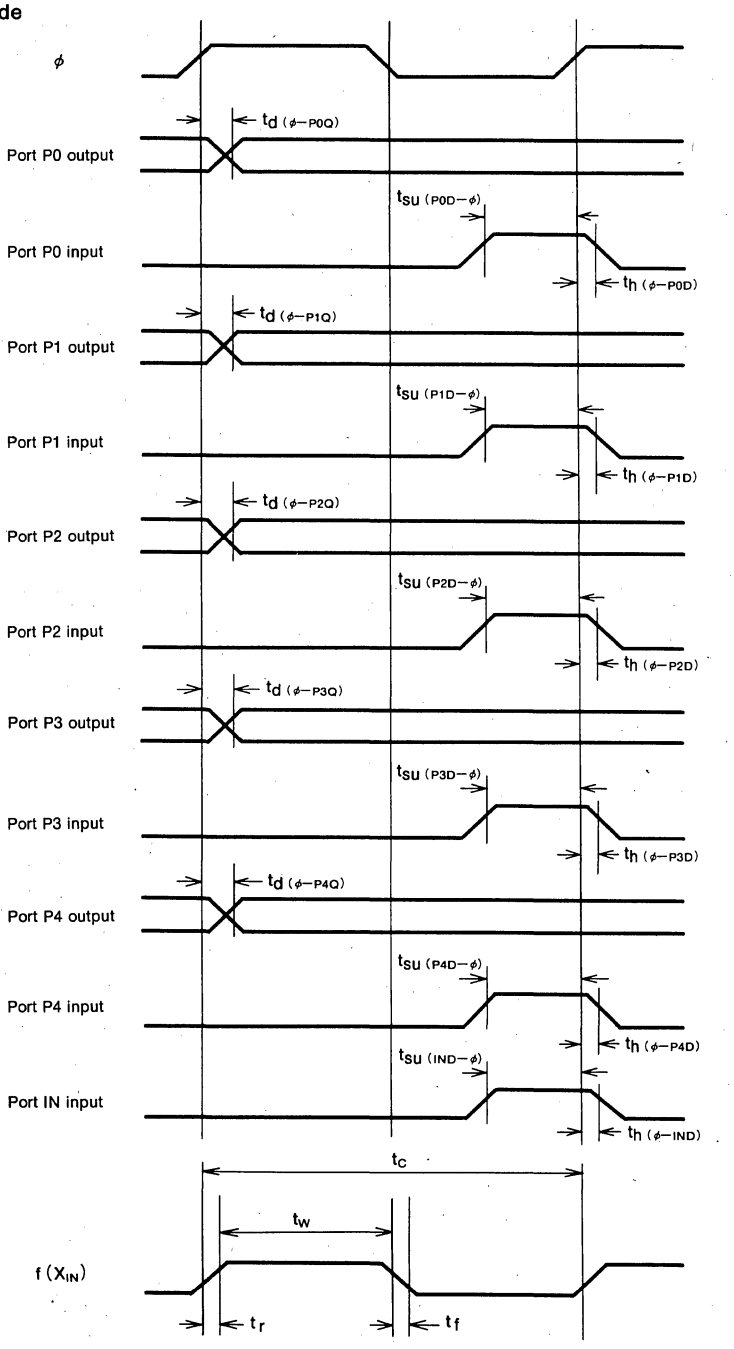


Fig.24 Test circuit of 2ϕ

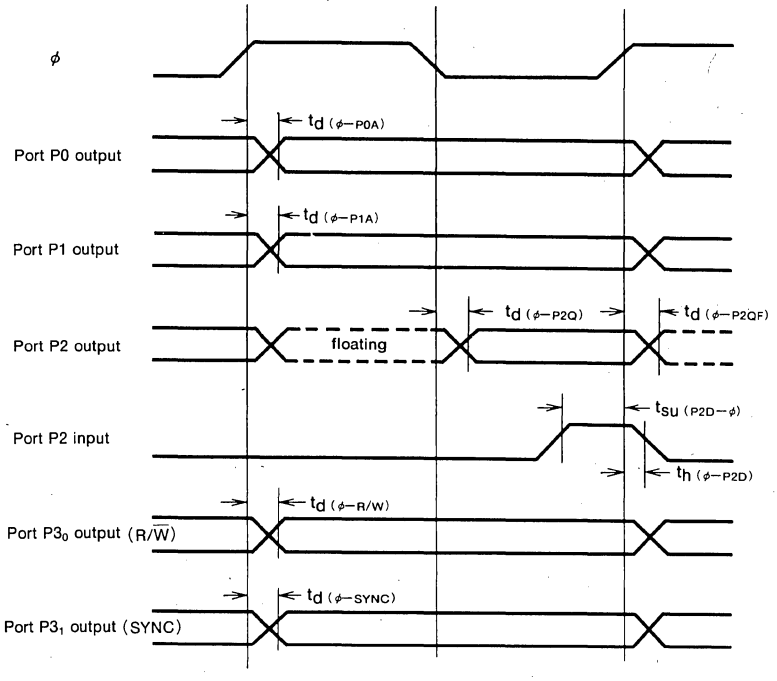
TIMING DIAGRAMS

In single-chip mode

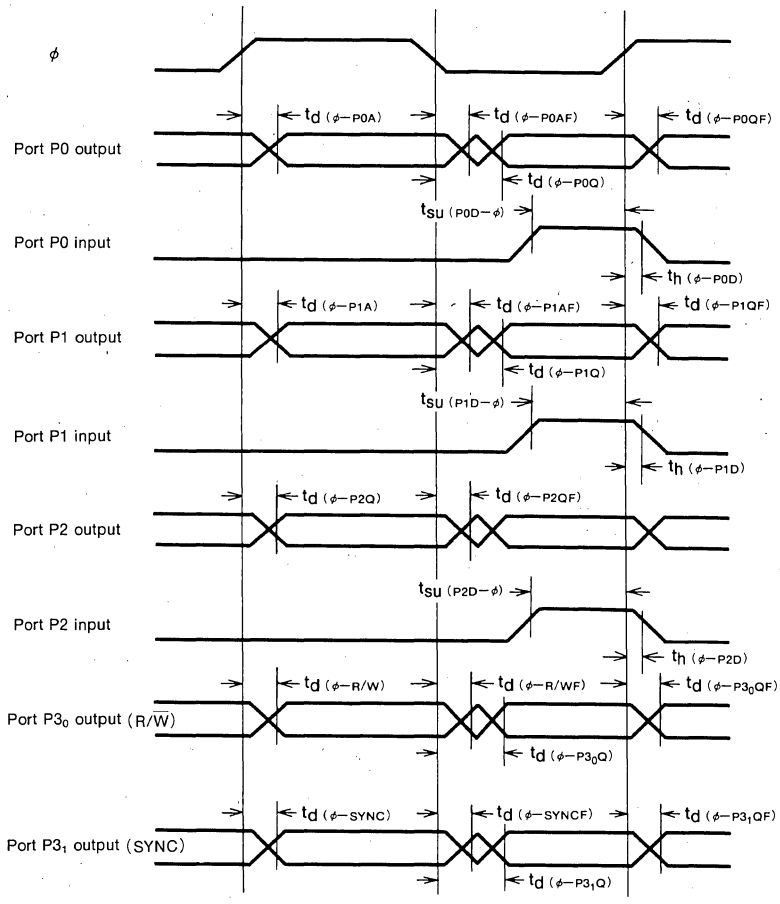


MITSUBISHI ELECTRIC

In memory expanding mode and microprocessor mode



In eva-chip mode



M50944-XXXSP/FP

PRELIMINARY

Notice: These are not a final specification. Some parametric limits are subject to change.

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50944-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP.

This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50944-XXXSP and the M50944-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

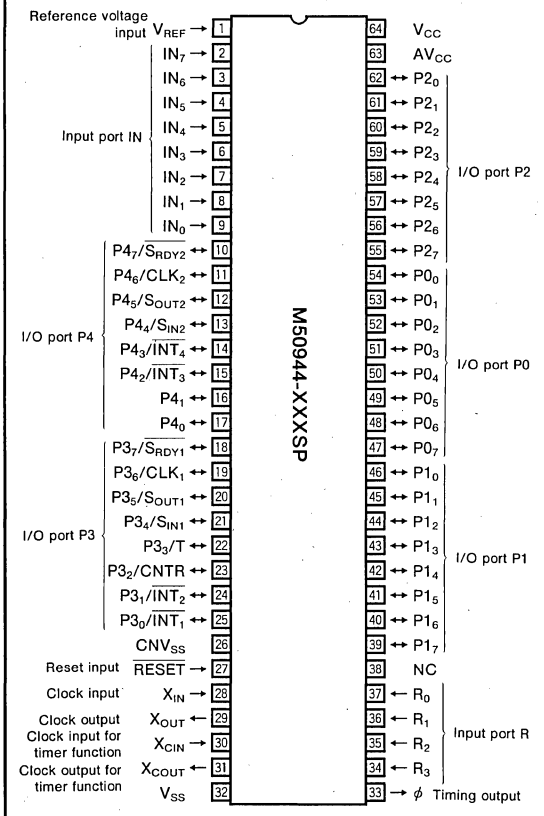
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 12288 bytes
  RAM ..... 192 bytes
- Instruction executing time
  ..... 2μs (minimum instructions, at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz ..... 5V±10%
  f(X_{IN})=1MHz ..... 3~5.5V
- Power dissipation
  normal operation mode (at 4MHz frequency)
  ..... 15mW
  low-speed operation mode (at 32kHz frequency for clock function) 0.3mW
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 10 types, 5 vectors
- 8-bit timer ..... 7 (6 when used as serial I/O)
- Serial I/O ..... 8-bit×2
- Devider for serial I/O 1
- Interrupt request distinguish register ..... 8-bit×2
- Programmable I/O ports (Ports P3, P4) 16
- Middle-voltage programmable ports
  (Ports P0, P1, P2) 24
- Input port (Ports R, IN) 12
- A-D conversion 8-bit, 8-channel
- Two clock generator circuits (One is for main clock, the other is for clock function)

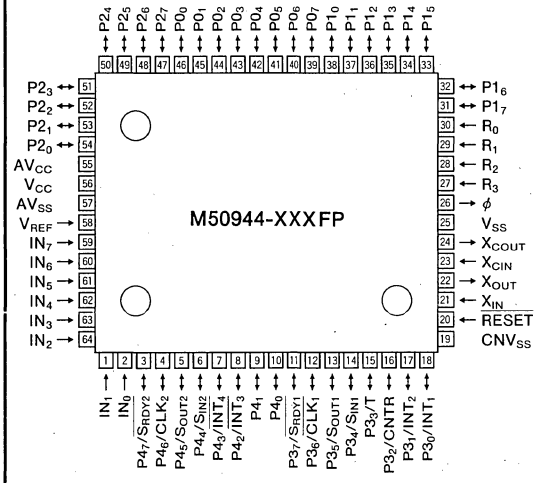
APPLICATION

Camera, Office automation equipment, VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



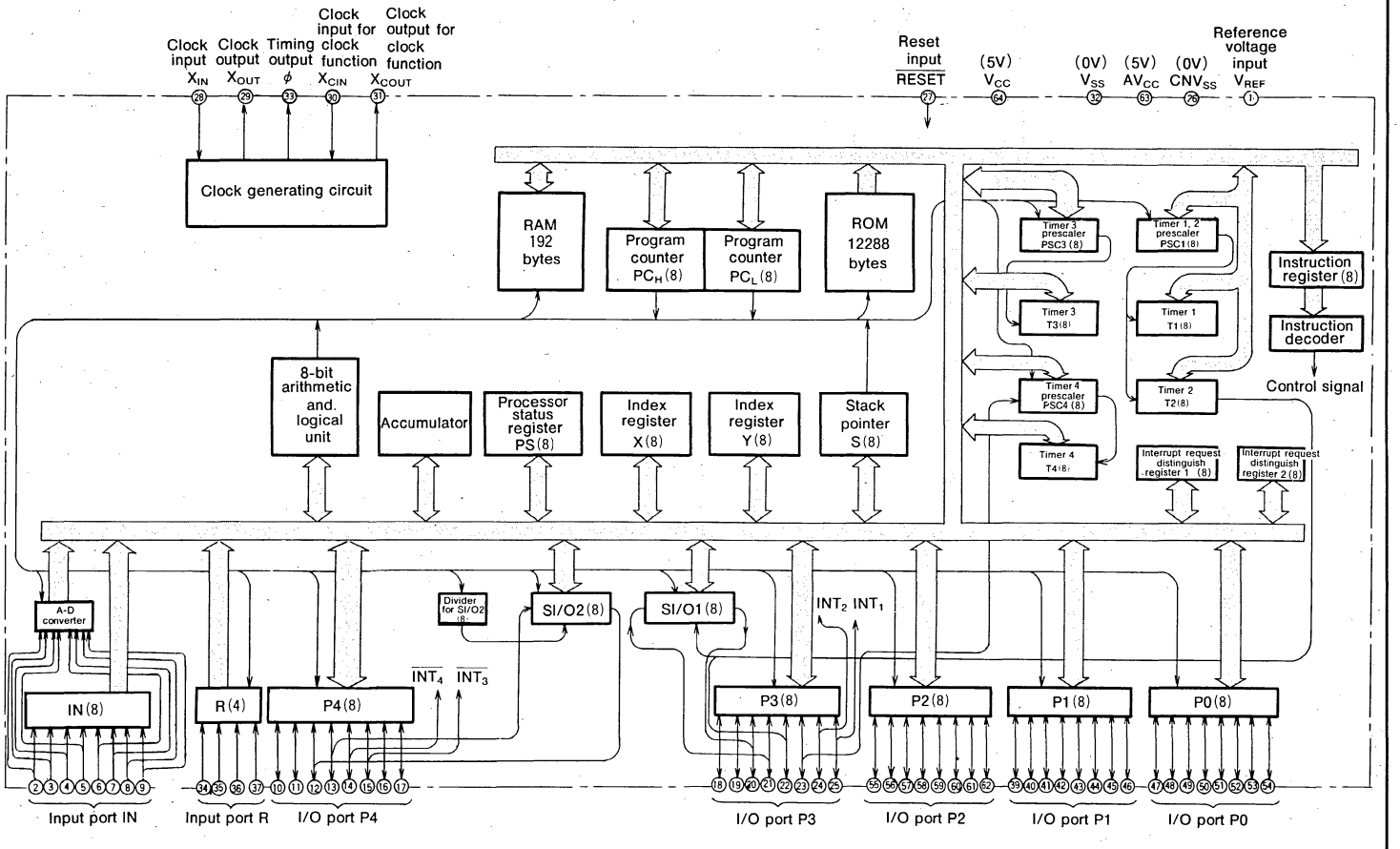
Outline 64P4B



Outline 64P6S

NC : No connection

M50944-XXXSP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONS OF M50944-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency).
Clock frequency			4.2MHz (main clock input), 32kHz (for clock function)
Memory size	ROM		12288bytes
	RAM		192bytes
Input/Output port	P0, P1, P2, P3, P4	I/O	8-bit×5
	IN	Input	8-bit×1
	R	Input	4-bit×1
Serial I/O			8-bit×2
Timers			8-bit prescaler×3+8-bit timer×4 (3 when serial I/O is used)
Subroutine nesting			96 levels (max.)
Interrupts			Four external interrupts, Four timer interrupts (or three timers, one serial I/O)
Clock generating circuit			Two built-in circuits (ceramic or quartz crystal oscillator).
Supply voltage			5V±10% (at f(X_{IN})=4MHz), 3.0~5.5V (at f(X_{IN})≦1.0MHz)
Power dissipation	At high-speed operation		15mW (at f(X_{IN})=4MHz).
	At low-speed operation		0.3mW (at f(X_{CIN})=32kHz).
	At stop mode		1μA (at clock stop)
Input/Output Characteristics	Input/Output voltage		5V (ports P3, P4)
			12V (ports P0, P1, P2)
	Output current		10mA (ports P0, P1, P2: middle voltage N-channel open drain output).
			−5~10mA (ports P3, P4: CMOS tri-state output)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package	M50944-XXXSP		64-pin shrink plastic molded DIP
	M50944-XXXFP		64-pin shrink plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillatior to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open. This clock can be used as a program controlled the system clock.
X_{COUT}	Clock output for clock function	Output	
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-ch open drain. A pull-up transistor is built-in between the V_{CC} pin and this port.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port with CMOS output. The other functions are basically the same as port P0. $P3_0$, $P3_1$, $P3_2$ and $P3_3$ pins are in common with INT_2, INT_1, CNTR and T respectively. When serial I/O_1 is used, $P3_4$, $P3_5$, $P3_6$ and $P3_7$ work as S_{IN1}, S_{OUT1}, CLK1 and $\overline{S_{RDY1}}$ pin respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. $P4_2$ and $P4_3$ pins are in common with $\overline{INT_3}$ and $\overline{INT_4}$ respectively. When serial I/O_2 is used, $P4_4$, $P4_5$, $P4_6$ and $P4_7$ work as S_{IN2}, S_{OUT2}, CLK_2 and $\overline{S_{RDY2}}$ pin respectively.
R_0~R_3	Input port R	Input	Port R is a 4-bit input port.
IN_0~IN_7	Analog input port IN	Input	Port IN is the analog input pin to the A-D converter. It also has a dual function and works as a normal input port.
AV_{CC}, AV_{SS} (Note)	Voltage input for A-D		This is the power supply input pin for the A-D conveter.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin for the A-D conveter.

Note. This pin is for flat package only.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50944-XXXSP is shown in Figure 1. Addresses $D000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 12288 bytes. Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (See interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required.

The RAM, I/O port, timer, etc. addresses are already assigned for the zero page. Addresses 0000_{16} to $00BF_{16}$ are assigned for the built-in RAM which consists of 192 bytes of static RAM. This RAM is used as the stack during subroutine calls and interrupts, in addition to data storage.

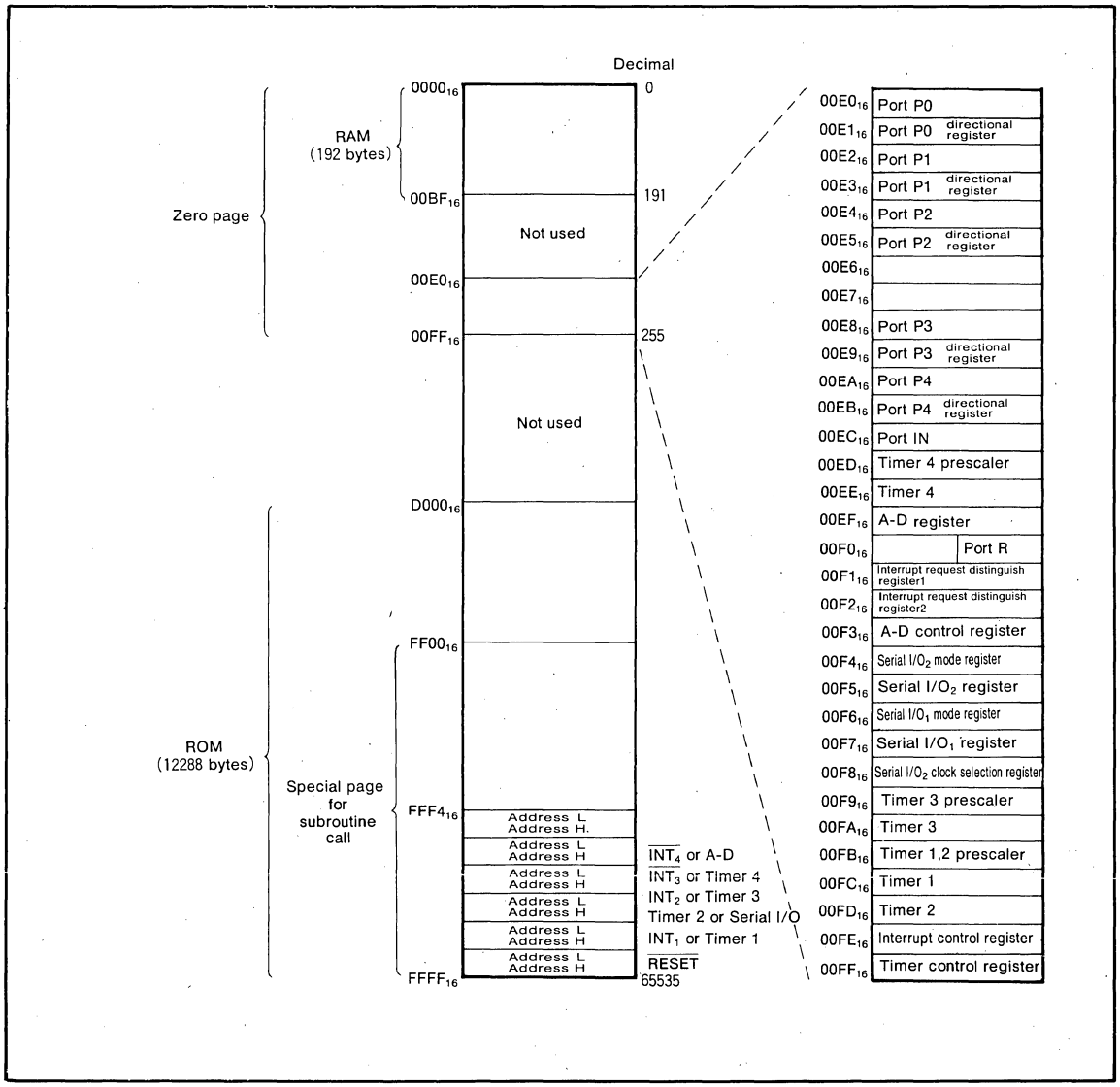


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, input/output, etc., is executed mainly through the accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register. In the index regsiter X addressing mode, the value of the OPERAND added to the contents of the index register X specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGSITER Y (Y)

The index register Y is an 8-bit register. In the index register Y addressing mode, the value of the OPERAND added to the contents of the index register Y specifies the real address.

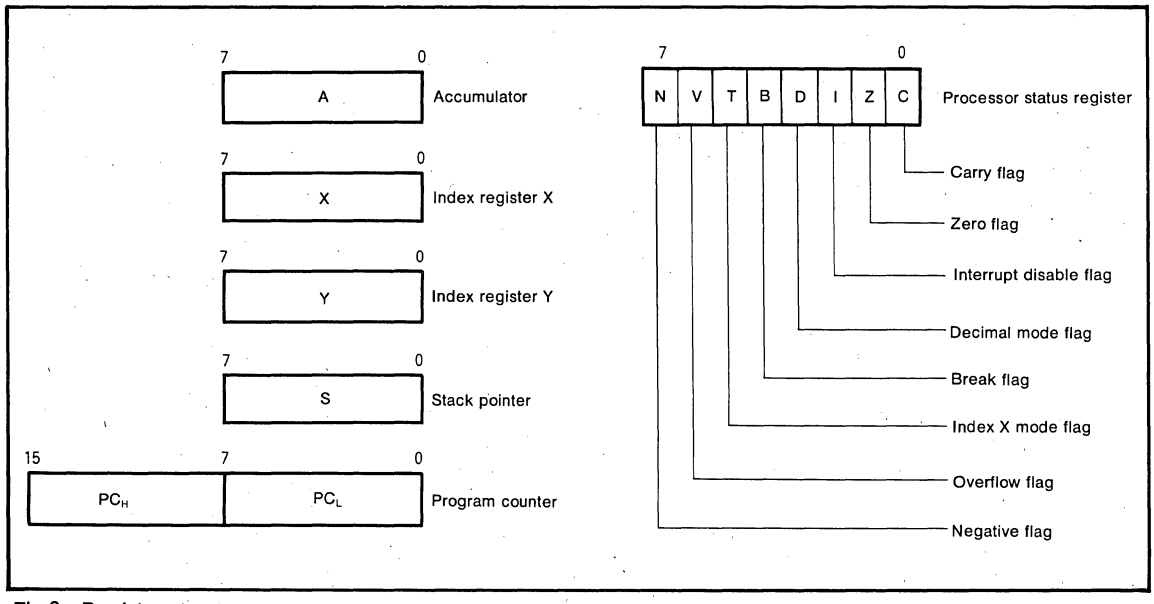


Fig.2 Register structure

STACK POINTER (S)

The stack pointer is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

When an interrupt occurs, the higher 8 bits of the program counter is pushed into the stack first, the stack pointer is decremented, and then the lower 8 bits of the program counter is pushed into the stack. Next the contents of the processor status register is pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter and processor status register data is popped off the stack in reverse order from above.

The accumulator is never pushed into the stack automatically, so a Push Accumulator instruction (PHA) is provided to execute this function. Restoring the accumulator to its previous value is accomplished by the Pop Accumulator instruction (PLA). It is executed in the reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed and popped to and from the stack with the PHP and PLP instructions, respectively.

During a subroutine call, only the program counter is pushed into the stack. Therefore, any registers that should not be destroyed should be pushed into the stack manually. To return from a subroutine call, the RTS instruction is used.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The 8-bit PS is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic Logic Unit (ALU) immediately after an operation. It is also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "0". If the result is not zero, the zero flag will be set to "1".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt is accepted, this flag is automatically set to "1" to prevent from other interrupts until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the B flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the T flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the V flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the N flag. There are no instuctions for directly setting or resetting the N flag.

INTERRUPT

The M50944-XXXSP can be interrupted from ten sources; INT_1 or timer 1, timer 2 or serial I/O_1, INT_2 or timer 3, $\overline{INT_3}$ or timer 4, $\overline{INT_4}$ or A-D or BRK instruction. The value of bit 2 of the serial I/O_1 mode register (address $00F6_{16}$) determines whether the interrupt is from timer 2 or from serial I/O_1. When bit 2 is "1" the interrupt is from serial I/O_1, and when bit 2 is "0" the interrupt is from timer 2. Also, when bit 2 is "1", parts of port 3 are used for serial I/O_1. Bit 7 and bit 5 of the interrupt request distinguish regisrer 1 (address $00F1_{16}$) distinguish whether the interrupt request is from INT_1 pin or timer 1. When bit 7 is "1", the interrupt is requested from INT_1 pin and bit 5 is "1", the interrupt is requested from timer 1. Bit 3 and bit 1 of the interrupt request distinguish register 1 (address $00F1_{16}$) distinguish whether the interrupt request is from INT_1 pin or timer 1. When bit 3 is "1", the interrupt is requested from INT_2 pin and bit 1 is "1", the interrupt is requested from timer 3. Also, bit 7 and bit 5 or bit 3 and bit 1 of the interrupt request distinguish register 2 distinguish whether the interrupt request is from $\overline{INT_3}$ pin or timer 4 and $\overline{INT_4}$ or A-D, respectively.

These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as an interrupt. When an interrupt is accepted, the contents of certain registers are pushed into specified locations, as discussed in the stack pointer section, and the interrupt disable flag (I) is set, and the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0". The interrupt request bits are set when the following conditions occur:

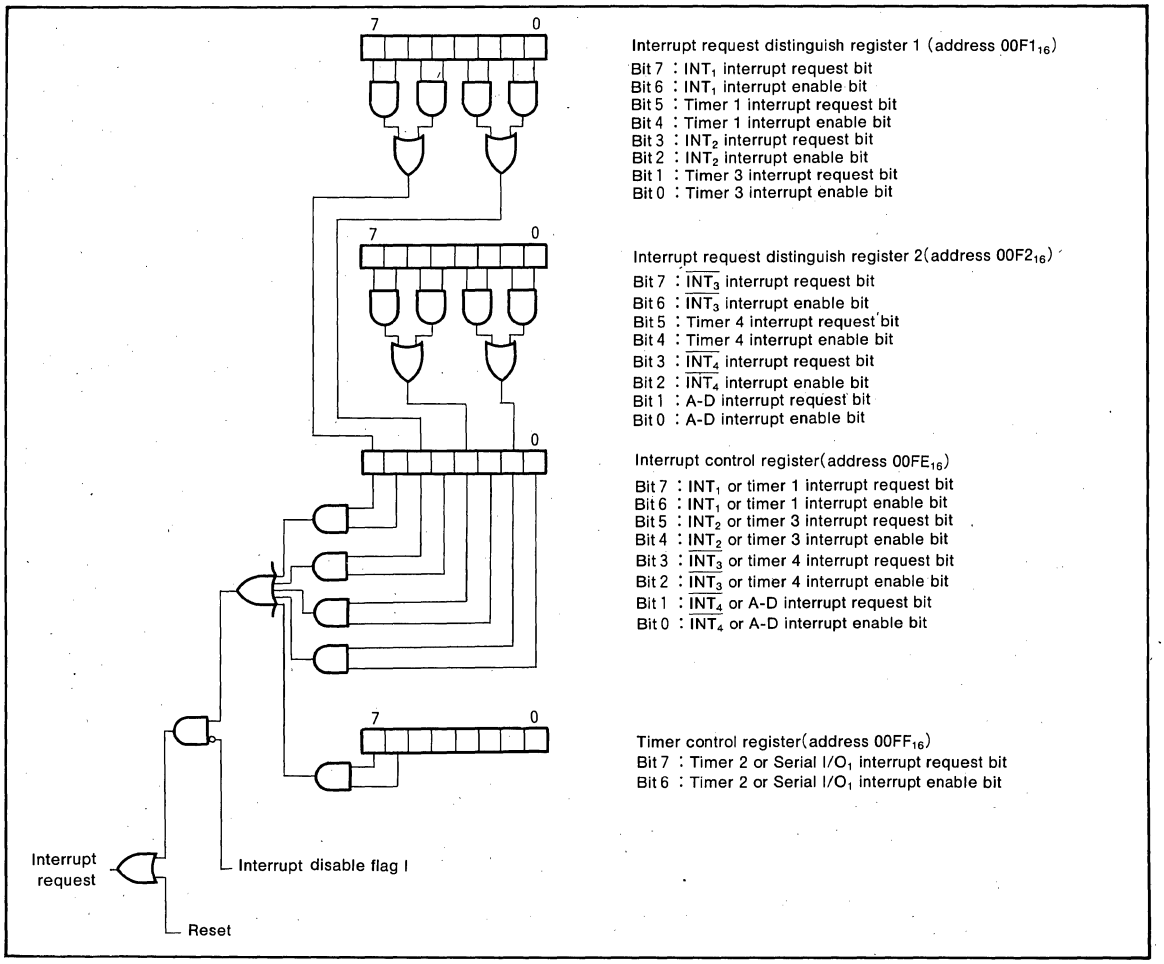


Fig. 3 Interrupt control

(1) When the level of INT_1, INT_2, $\overline{INT_3}$ or $\overline{INT_4}$ pin changed
(2) When the contents of timer 1, timer 2 (or the serial I/O_1 counter), or timer 4 goes to "0"

When the two interrupt requests, which are the same priority, are at the same sampling, the priority process is processed by interrupt request distinguish register 1 and 2.

These request bits can be reset by a program but can not be set. Since the BRK instruction interrupt and the A-D interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if A-D generated the interrupt.

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$FFFF_{16}$, $FFFE_{16}$
INT_1 or timer 1	2	$FFFD_{16}$, $FFFC_{16}$
Timer 2 or serial I/O_1	3	$FFFB_{16}$, $FFFA_{16}$
INT_2 or timer 3	4	$FFF9_{16}$, $FFF8_{16}$
$\overline{INT_3}$ or timer 4	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{INT_4}$ or A-D(BRK)	6	$FFF5_{16}$, $FFF4_{16}$

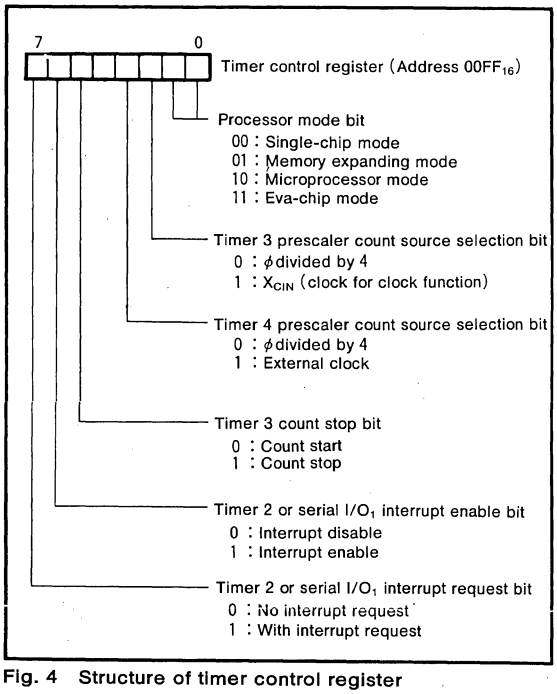


Fig. 4 Structure of timer control register

TIMER

The M50944-XXXSP has seven timers; timer 1, 2 prescaler, timer 1, timer 2, timer 3 prescaler, timer 3, timer 4 prescaler and timer 4. Interrupt from timer 2 cannot be used at using serial I/O (see serial I/O section).

A block diagram of timer 1 through 3 and timer 4 is shown in Figure 5 and Figure 6 respectively. The count source for timer 3 prescaler and timer 4 prescaler can be selected by using bit 2 and 3 of the timer control register (addres $00FF_{16}$), as shown in Figure 4.

All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timer is 1/(n +1), where n is the contents of timer latch.

Each timer has interrupt generating functions. The timer interrupt request bits (in the interrupt request distinguish register 1, the interrupt request distinguish register 2, the interrupt control register and the timer control register) is set at the next count pulse after the timer reaches "0". The interrupt distinguish register 1 and 2 are located at addresses $00F1_{16}$ and $00F2_{16}$ respectively.

The starting and stopping of timer 3 prescaler is controlled by bit 5 of the timer control register. If the corresponding bit is "0", the timer starts counting, when the corresponding bit is "1", the timer stops.

After a STP instruction is executed, timer 3 prescaler, timer 3, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 of the timer control register). This state is canceled if timer 3 interrupt request bit is set to "1", or if the system is reset, and it becomes a former count source decided with bit 2 of the timer control register. Before the STP instruction is executed, bit 5 of the timer control register must be set to "0", bit 0 of the interrupt request distinguish register 1 must be set to "1", bit 1 of the interrupt request distinguish register 1 must be set to "0", bit 4 of the interrupt control register must be set to "0" and bit 5 of the interrupt control register must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

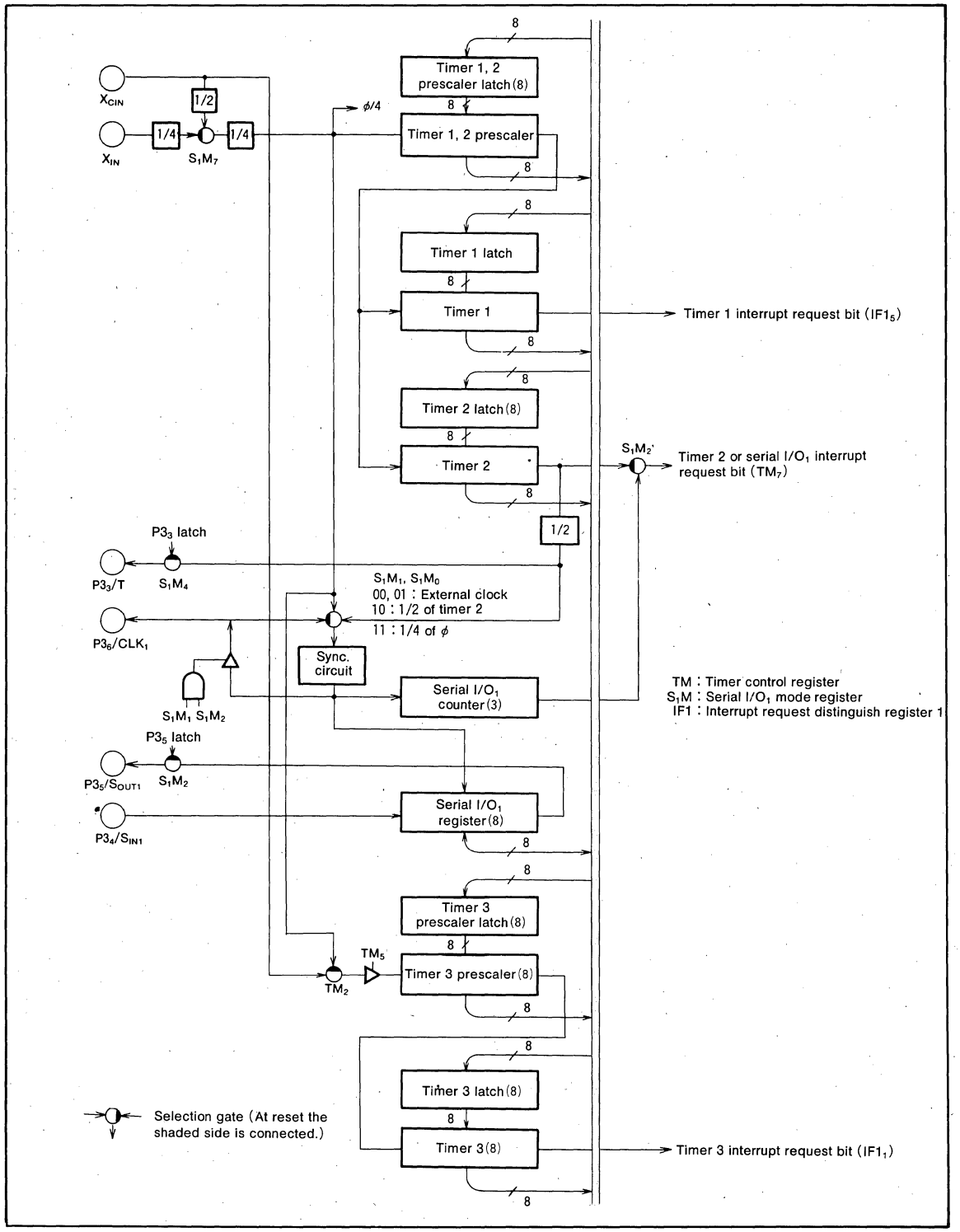


Fig. 5 Block diagram of timer 1 through timer 3

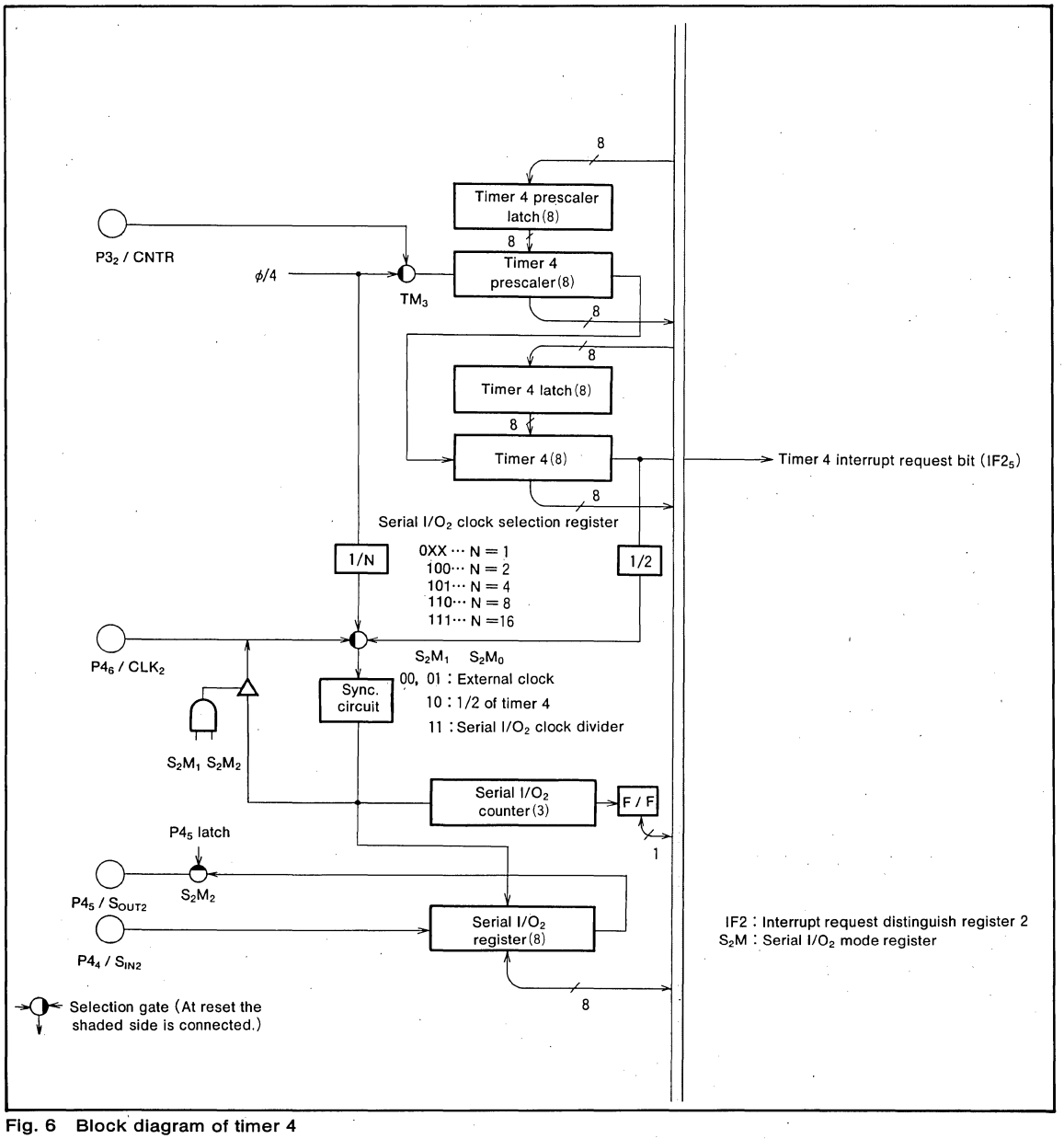


Fig. 6 Block diagram of timer 4

SERIAL I/O$_1$

A block diagram of the serial I/O$_1$ is shown in Figure 7. In the serial I/O$_1$ mode, the receive ready signal ($\overline{S_{RDY1}}$), synchronous input/output clock (CLK$_1$), and the serial I/O$_1$ (S_{OUT1}, S_{IN1}) pins are used as P3$_7$, P3$_6$, P3$_5$, and P3$_4$, respectively.

The serial I/O$_1$ mode register (address 00F6$_{16}$) is an 8-bit register. Bits 1 and 0 of this register are used to select a synchronous clock source. When these bits are [00] or [01], an external clock from P3$_6$ is selected. When these bits are [10], the overflow signal (from timer 2) divided by two becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 becomes the clock.

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", P3$_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous is selected, the clock is output from P3$_6$. If an external synchronous clock is selected, the clock is input to P3$_6$. And P3$_5$ will be a serial output and P3$_4$ will be a serial input. To use P3$_4$ as a serial input, set the directional register bit which corresponds to P3$_4$ to "0". For more information on the directional register, refer to the I/O pin section.

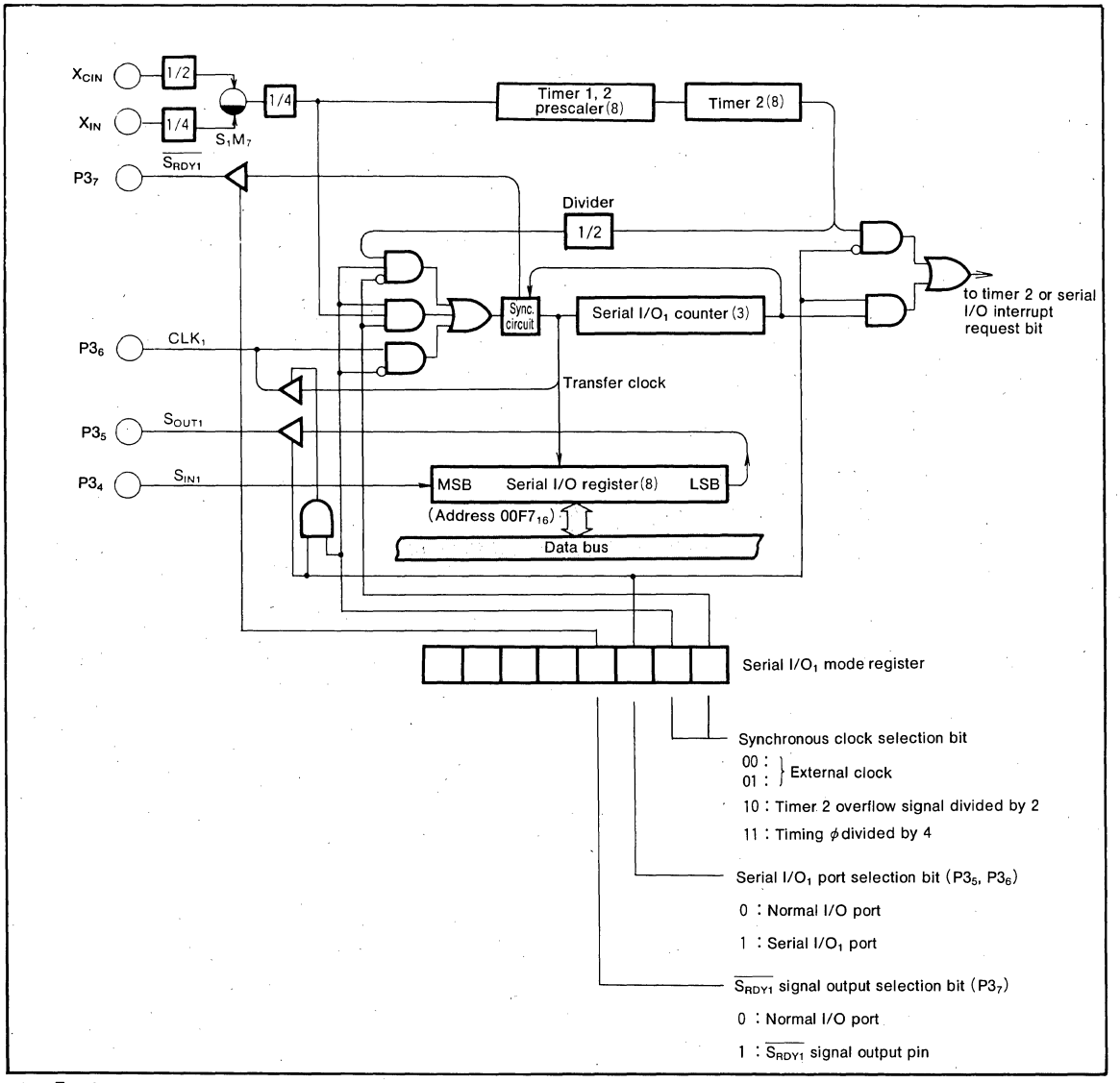


Fig. 7 Block diagram of serial I/O

To use the serial I/O_1, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O_1 counter instead of timer 1. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3 = "1", $\overline{S_{RDY1}}$) or used as a normal I/O pin (bit 3="0").

The function of the serial I/O_1 differs depending on the clock source; external clock or internal clock.

Internal Clock — The $\overline{S_{RDY1}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O_1 register. After the falling edge of the write signal, the $\overline{S_{RDY1}}$ signal becomes low signaling that the M50944-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY1}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O_1 counter is set to 7 when data is stored in the serial I/O_1 register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O_1 register will be shifted 1 bit. Data is output starting with the LSB. After the transfter clock has counted 8 times, the serial I/O_1 register will be empty and the transfter clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock — If an external clock is used, the interrupt request will be set after the transfter clock has counted 8 times but the transfter clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 8, and connections between two M50944-XXXSPs' are shown in Figure 9.

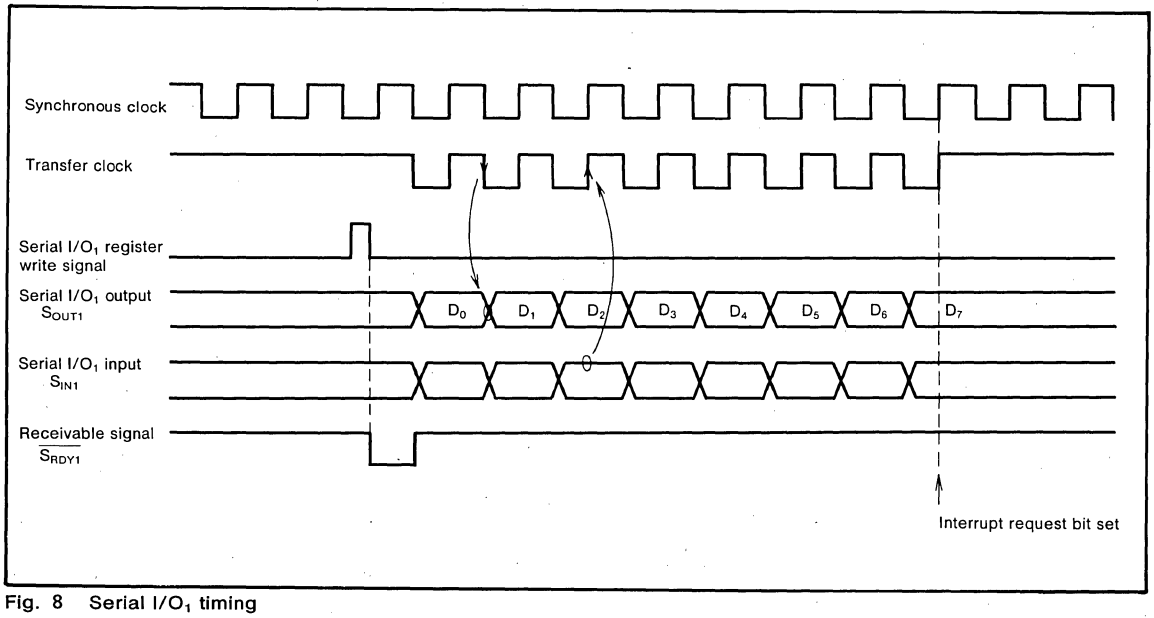


Fig. 8 Serial I/O_1 timing

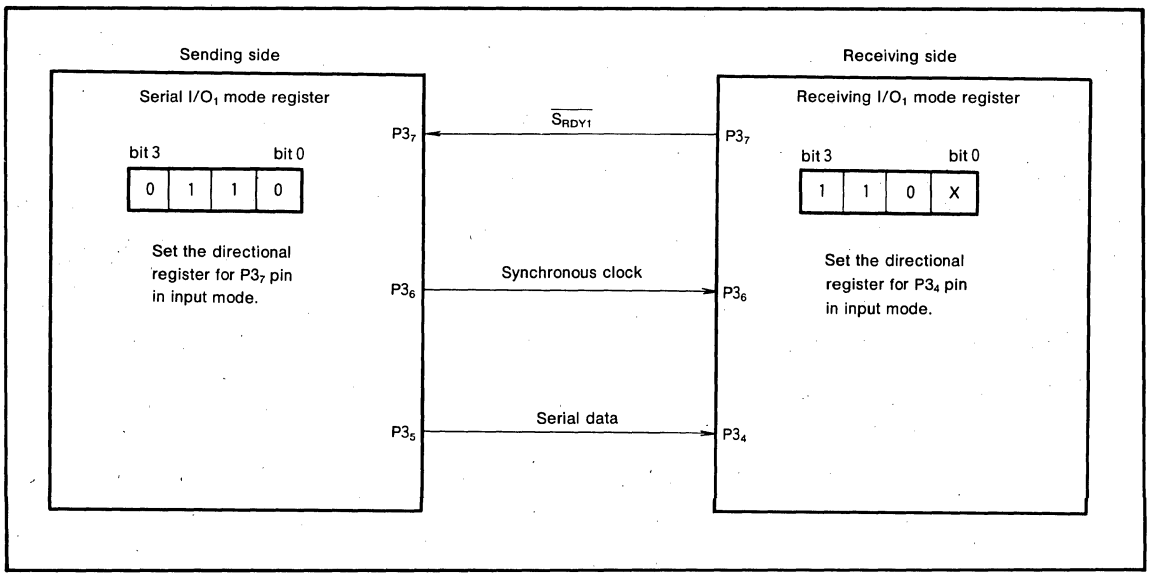


Fig. 9 Example of serial I/O1 connection

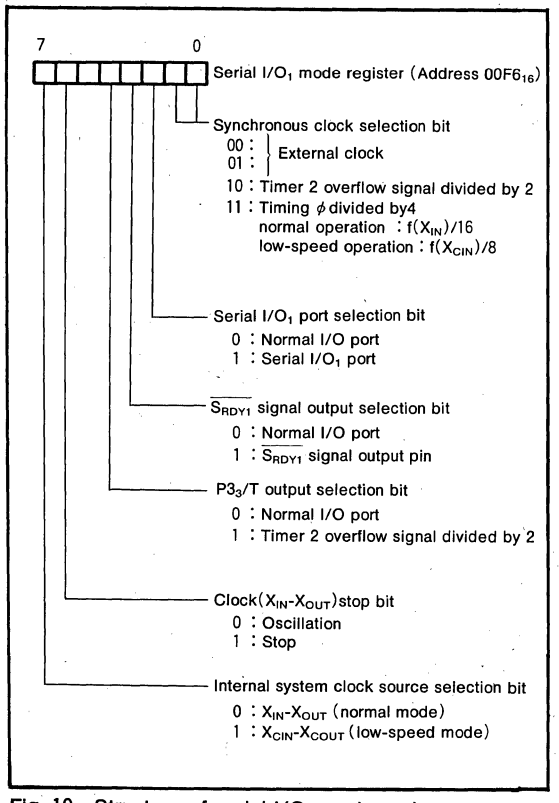


Fig. 10 Structure of serial I/O1 mode register

SERIAL I/O_2

A block diagram of the serial I/O_2 is shown in Figure 11.

In the serial I/O_2 mode the receive ready signal ($\overline{S_{RDY2}}$), synchronous input /output clock (CLK_2), and the serial I/O_2 pins (S_{OUT2}, S_{IN2}) are used as $P4_7$, $P4_6$, $P4_5$, and $P4_4$, respectively.

The serial I/O_2 mode register (address $00F4_{16}$) is an 8-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P4_6$ is selected. When these bits are [10], the overflow signal from timer 4, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the timing ϕ divided by 4, becomes the clock.

Bit 2 and 3 decide whether parts of P4 will be used as a serial I/O_2 or not. When bit 2 is a "1", $P4_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P4_6$. If an external synchronous clock is selected, the clock is input to $P4_6$ and $P4_5$ will be a serial output and $P4_4$ will be a serial input. To use $P4_4$ as a serial input, set the directional register bit which corresponds to $P4_4$ to "0". For more information on the directional register, refer to the I/O pin section.

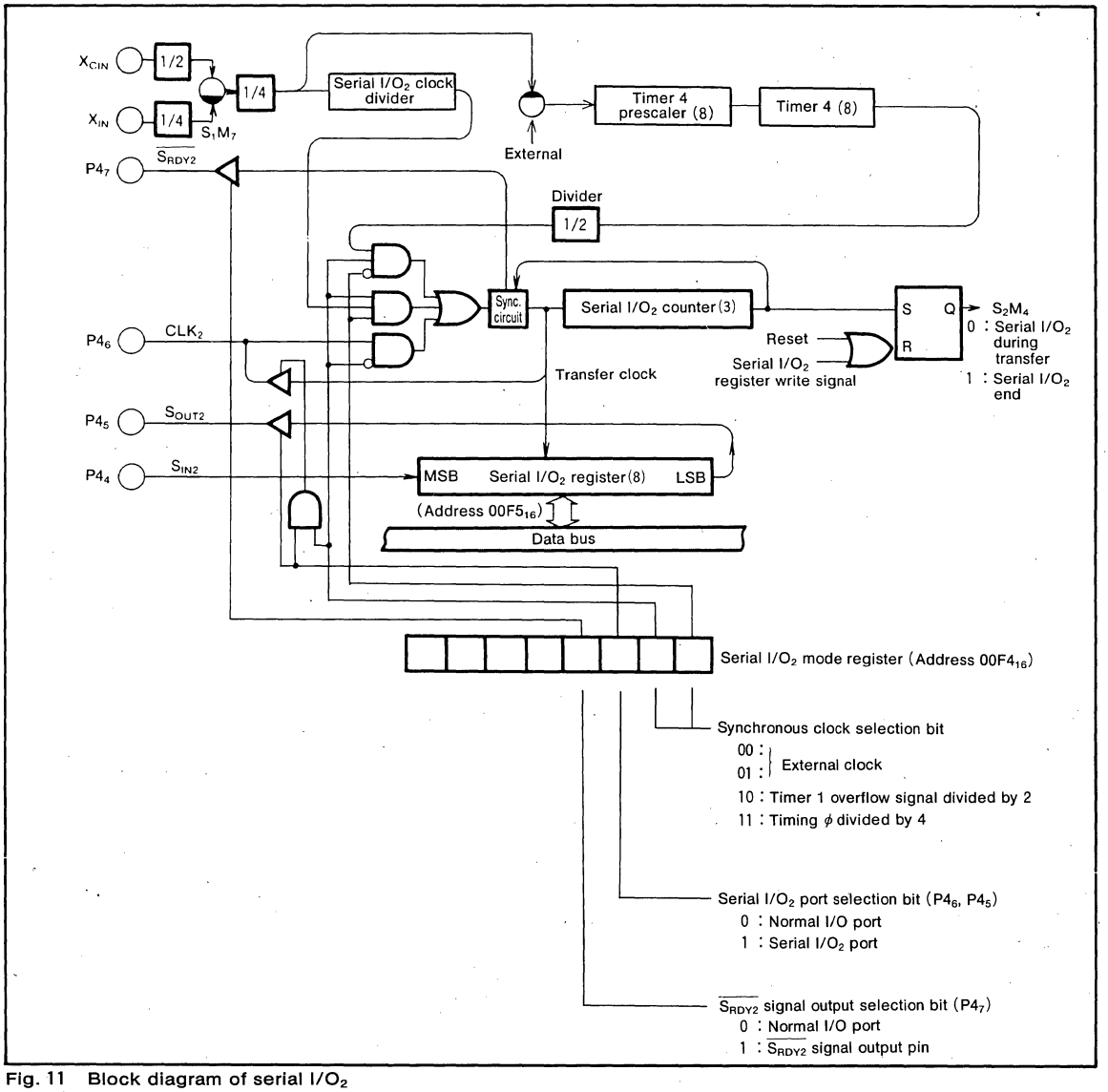


Fig. 11 Block diagram of serial I/O_2

To use the serial I/O_2, bit 2 needs to be set to "1", if it is "0" $P4_6$ will function as a normal I/O. Bit 3 determines if $P4_7$ is used as an output pin for the receive data ready signal (bit 3=1, $\overline{S_{RDY2}}$) or used as normal I/O pin (bit 3=0). The serial I/O_2 function is discussed below. The function of the serial I/O_2 differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY2}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O_2 register (address $00F5_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY2}}$ signal becomes low signaling that the M50944-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY2}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O_2 counter is set to 7 when data is stored in the serial I/O_2 register. At each falling edge of the transfer clock, serial data is output to $P4_5$. During the rising edge of this clock, data can be input from $P4_4$ and the data in the serial I/O_2 register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O_2 register will be empty and the transfer clock will remain at a high level. At this time the serial I/O_2 end bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 12.

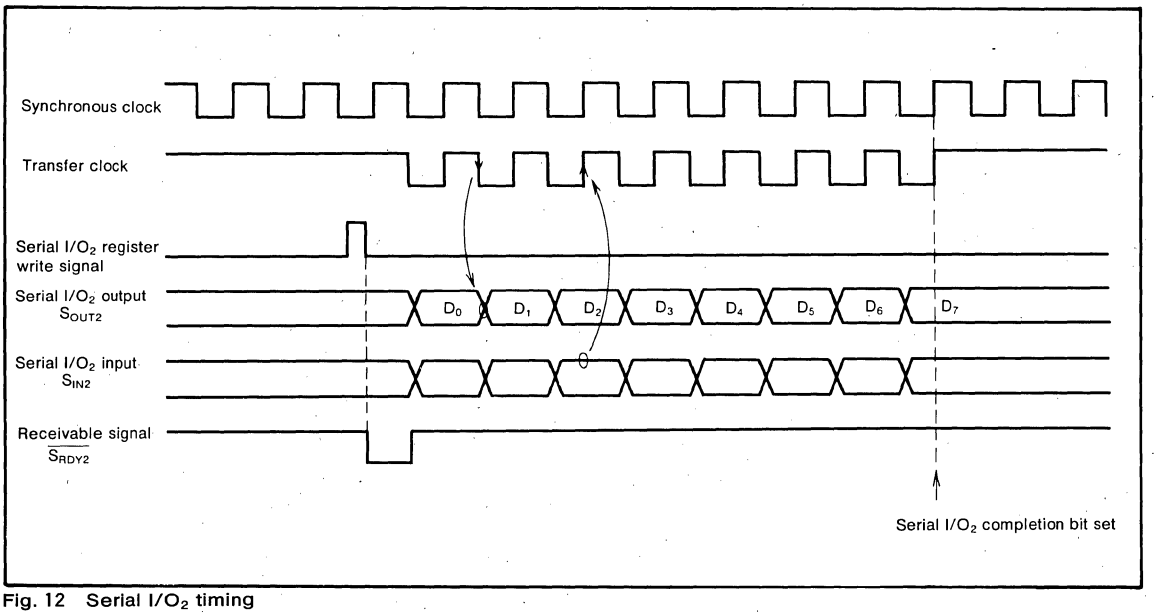


Fig. 12 Serial I/O_2 timing

A block diagram of clock divider for serial I/O_2 is shown in Figure 13. Bit 2, 1 and 0 of the serial I/O_2 clock selection register (address $00F8_{16}$) determine the dividing ratio of the serial I/O_2 clock. When these bits are [0XX], the timing ϕ divided by 4 is selected. When these bits are [100], [101], [110] and [111], the timing ϕ divided by 8, 16, 32 and 64 are selected respectively.

To use the clock divider for serial I/O_2, both bit 1 and bit 0 of the serial I/O_2 mode register (address $00F4_{16}$) need to be set to "1".

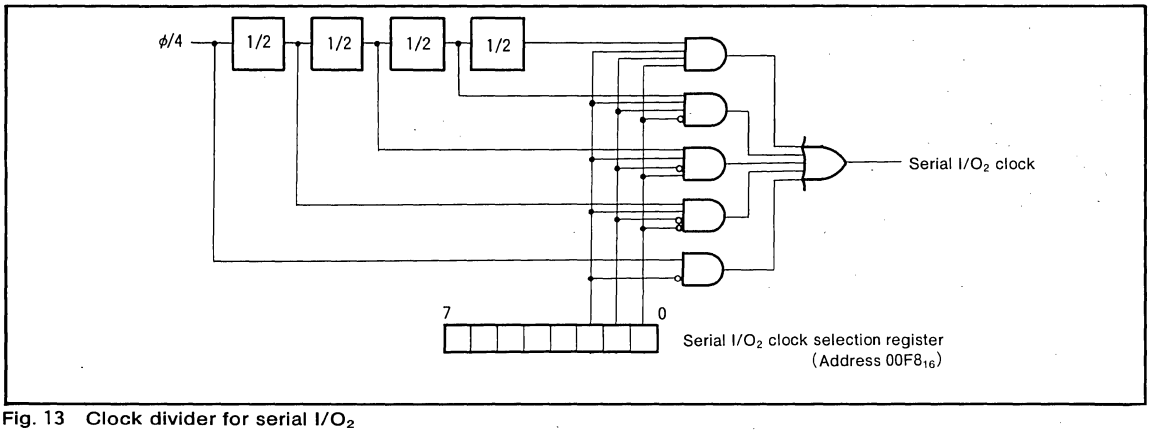


Fig. 13 Clock divider for serial I/O_2

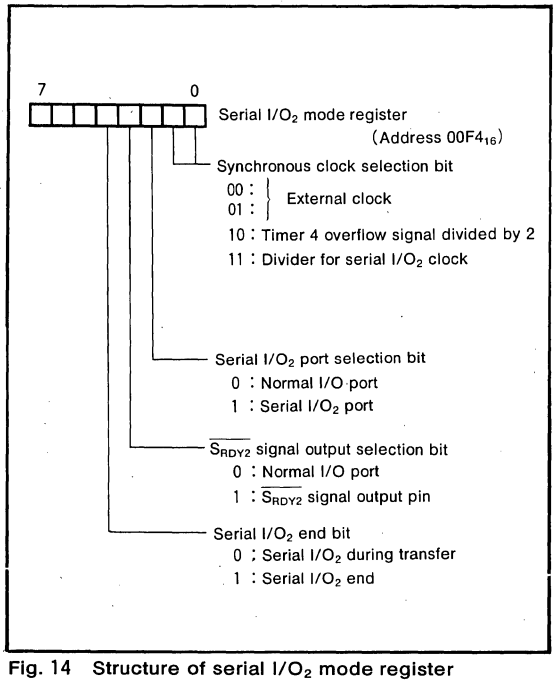


Fig. 14 Structure of serial I/O_2 mode register

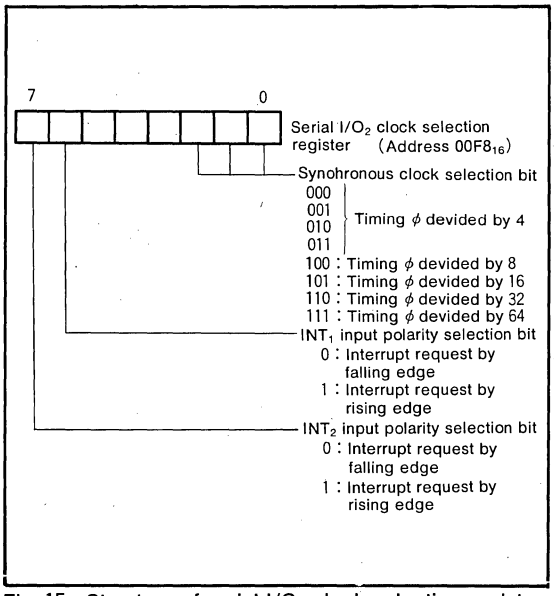


Fig. 15 Structure of serial I/O_2 clock selection register

A-D CONVERTER

The A-D converter circuit is shown in Figure 17. The analog input ports of the A-D converter ($IN_0 \sim IN_7$) are in common with the input ports of the data bus.

The 6-bit A-D control register is located at address $00F3_{16}$. One of the eight analog inputs is selected by bits 0, 1 and 2 of this register.

A-D conversion is accomplished by first selecting the analog channel (bit 0, 1 and 2) to be converted. The conversion is started when dummy data is written into address $00EF_{16}$. When the conversion is finished, an interrupt is generated by the A-D and the digital data can be read from the A-D register (address $00EF_{16}$). The end of the conversion is determined by either the A-D conversion end bit (bit 5 of the A-D control regiser) or an A-D interrupt request bit.

The A-D conversion can also be programmed for high or low speed conversions. This is accomplished by using the A-D conversion speed switch bit (bit 4 of the A-D control register). For more information on the electrical characteristics of the high and low speed conversions, refer to the electrical characteristics section.

Port IN can also be used as an input port by reading data into address $00EC_{16}$. However, this cannot be done during A-D conversions.

The A-D control register is shown in Figure 16.

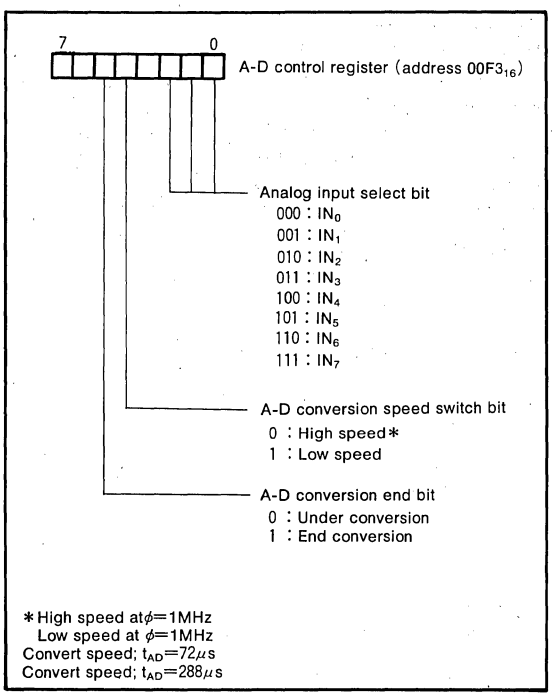


Fig. 16 Structure of A-D control register

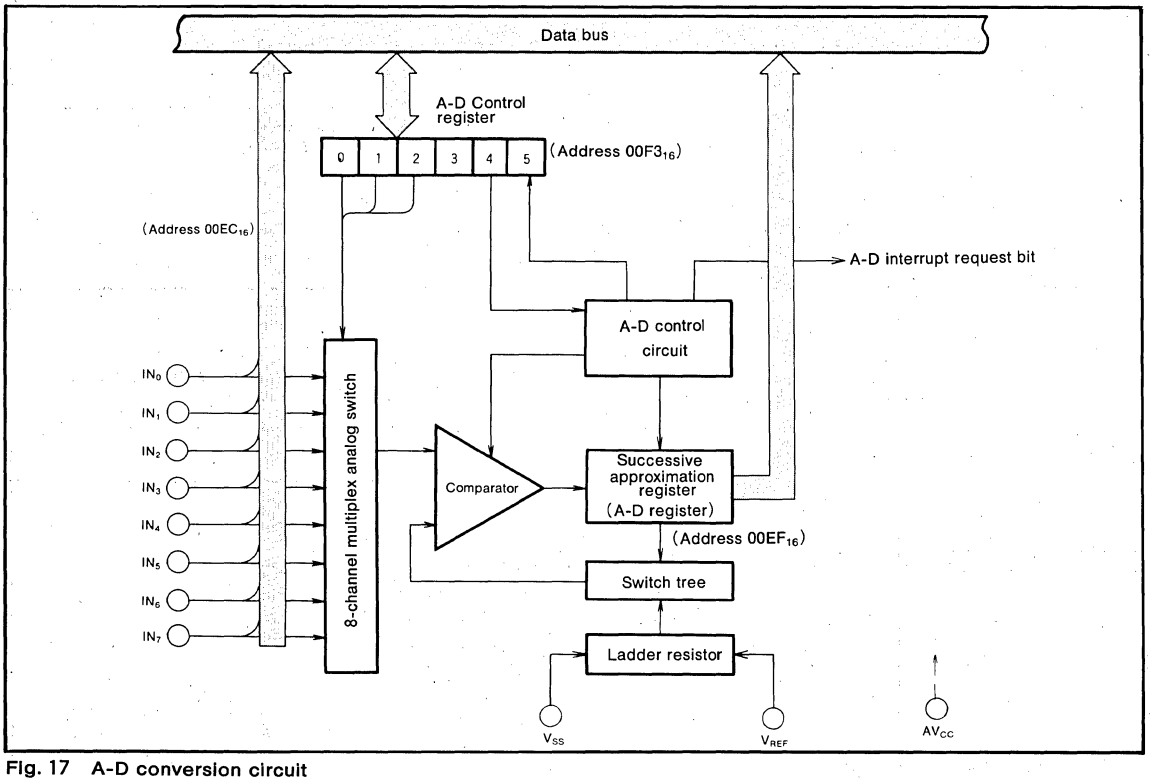


Fig. 17 A-D conversion circuit

MITSUBISHI ELECTRIC

RESET CIRCUIT

The M50944-XXXSP is reset according to the sequence shown in Figure 20. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 18.

An example of the reset circuit is shown in Figure 19.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

		Address	
(1)	Port P0 directional register	(D0) ($E1_{16}$) ···	00_{16}
(2)	Port P1 directional register	(D1) ($E3_{16}$) ···	00_{16}
(3)	Port P2 directional register	(D2) ($E5_{16}$) ···	00_{16}
(4)	Port P3 directional register	(D3) ($E9_{16}$) ···	00_{16}
(5)	Port P4 directional register	(D4) (EB_{16}) ···	00_{16}
(6)	Serial I/O_1 mode register	(S_1M)($F6_{16}$) ···	* * 0 0 0 0 0
(7)	Serial I/O_2 mode register	(S_2M)($F4_{16}$) ···	0 0 0 0 0
(8)	Serial I/O_2 clock selection register	($F6_{16}$)	0 0 0 0 0
(9)	A-D control register	($F3_{16}$)	1 0 0 0 0
(10)	Interrupt request distinguish register 1	(IF1)($F1_{16}$)	00_{16}
(11)	Interrupt request distinguish register 2	(IF2)($F2_{16}$) ···	00_{16}
(12)	Interrupt control register	(IM)(FF_{16}) ···	00_{16}
(13)	Timer control register	(TM)(FE_{16}) ···	00_{16}
(14)	Interrupt disable flag for processor status register	(PS) ···	1
(15)	Program counter	(PC_H) ···	Contents of address $FFFF_{16}$
		(PC_L) ···	Contents of address $FFFE_{16}$

Since the contents both registers other than those listed above (inclouding timer 1, timer 2, timer 3, and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values

Note : * means mask option

Fig. 18 Internal state of microcomputer at reset

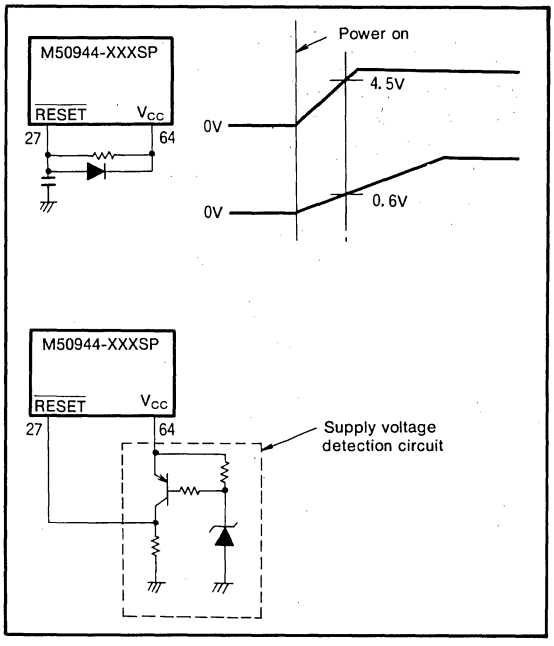


Fig. 19 Example of reset circuit

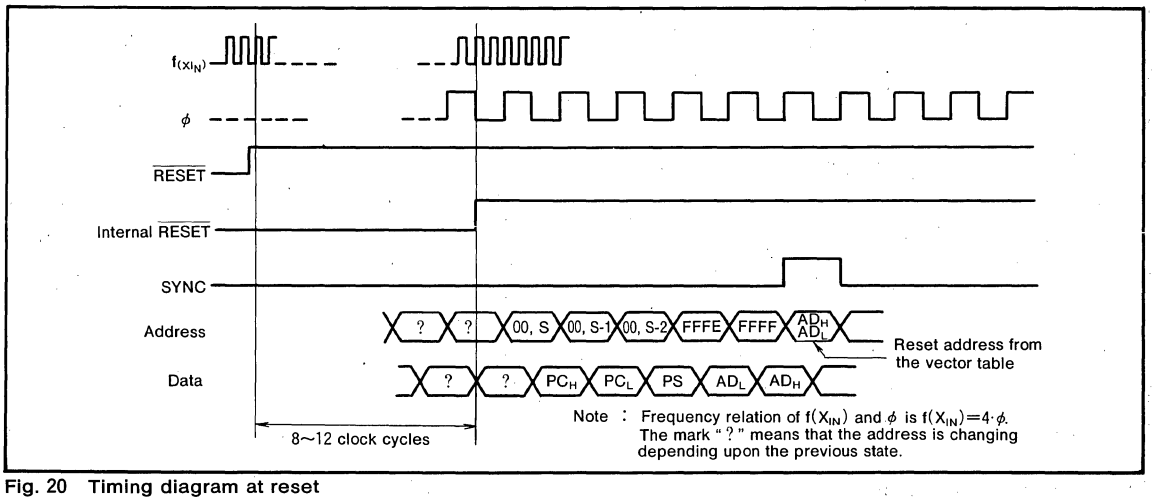


Fig. 20 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit output port with N-channel open drain and high voltage output. Each pin has a pull-up transistor option. As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$.

Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the high impedance state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

Depending on the status of the processor status register (bit 0 and bit 1 of address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode section.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode section.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's. For more details, see the processor mode section.

(4) Port P3

Port P3 is an 8-bit I/O port having CMOS output. Each pin is shared with serial I/O_1, timer overflow and external interrupt input functions. These functions remain the same even if the device is used in other modes.

(5) Port P4

Port P4 is an 8-bit I/O port with CMOS outputs. Each pin is shared with serial I/O_2, and external interrupt input functions. During all modes except single-chip mode, $P4_1$ and $P4_0$ function as both SYNC and $R/\overline{W}$ outputs as well as I/O ports (see processor mode section).

(6) Port R

Port R is a 4-bit input port.

(7) Port IN

Port IN is an 8-bit input port to the A-D converter. It can also be used as an input port by reading the input data into address $00EC_{16}$. However, this port cannot be read during A-D conversion.

(8) Clock ϕ output pin

This is the timing output pin. When selected the main clock (X_{IN}-X_{OUT}) as the internal system clock, the clock frequency divided by four is outputed. However, when selected the clock for clock function (X_{CIN}-X_{COUT}), the clock frequency divided by two is outputed.

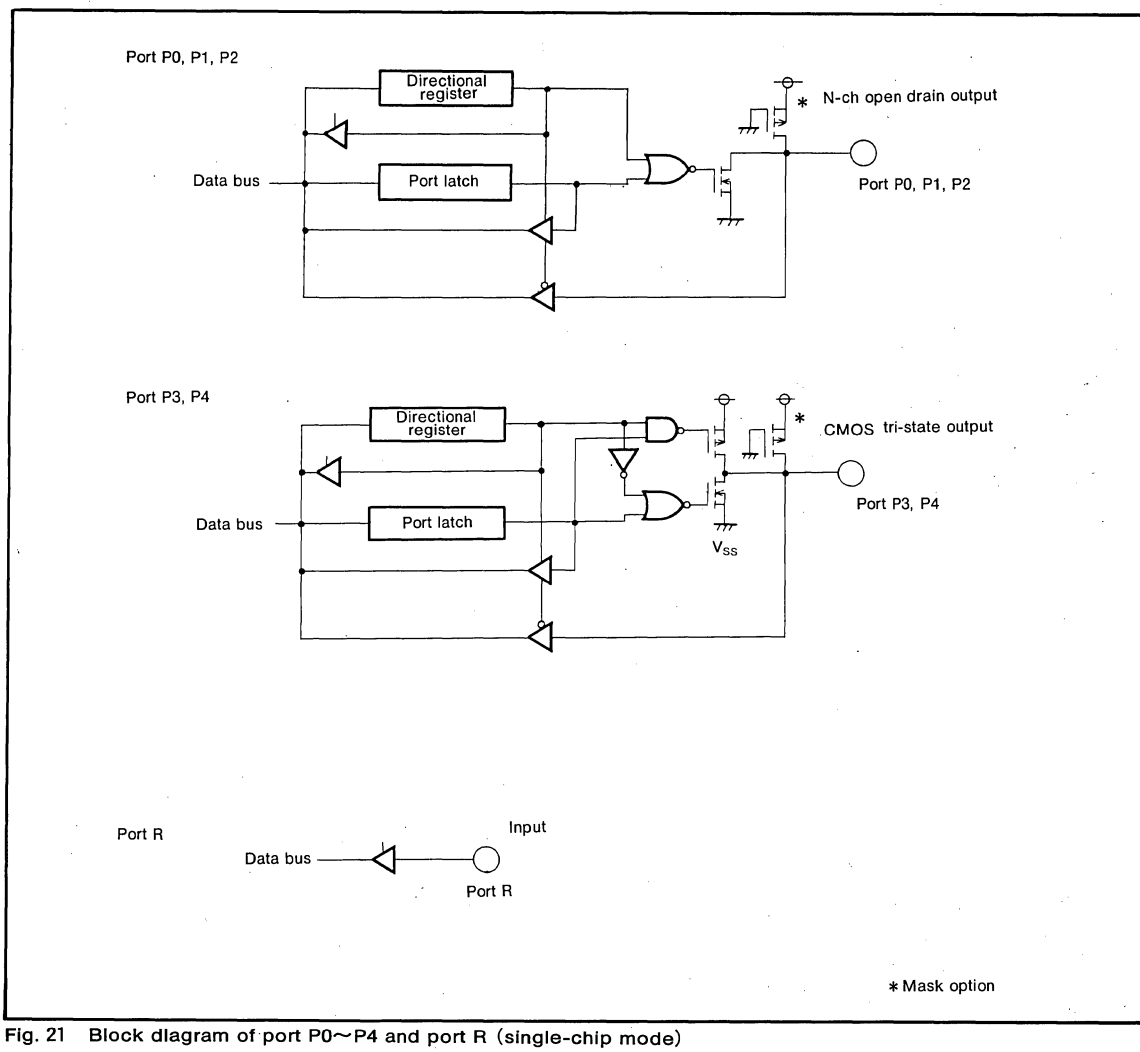


Fig. 21 Block diagram of port P0~P4 and port R (single-chip mode)

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 of address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, P0～P2 and P4 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports. Figure 23 shows the functions of ports P0～P2, and P4 corresponding to each mode.

The memory map of the single-chip mode is illustrated in Figure 1, and the other modes are shown in Figure 22. By connecting the CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode regsiter. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

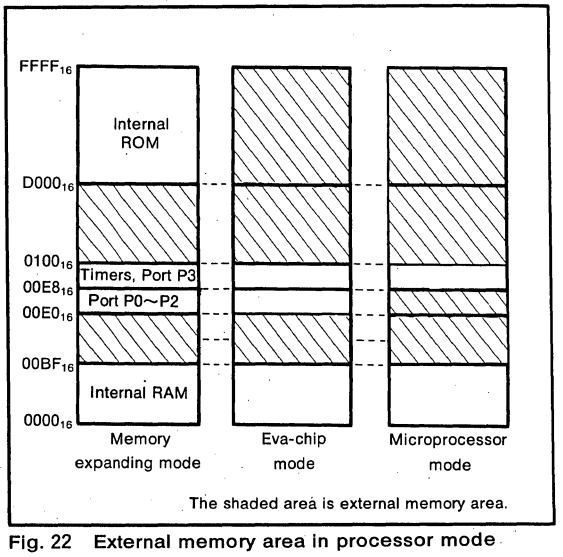


Fig. 22 External memory area in processor mode

(1) Single-chip mode [00]
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P4 will work as original I/O ports.

(2) Memory expanding mode [01]
The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.
The lower 8 bits of address data for port P0 is output when ϕ goes to the "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.
Port P1's higher 8 bits of address data are output when ϕ goes "H" state and as it changes back to the "L" state it retains its original I/O functions.
Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of $D_7 \sim D_0$ (including instruction code) while at the "L" state.
Pins $P4_1$ and $P4_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state.
When in the "L" state, $P4_1$ and $P4_0$ retain their original I/O functions.
The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.
The SYNC is a synchronous signal which goes "H" state when it fetches the OP code.

(3) Microprocessor mode [10]
After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.
In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pin is lost. Port P2 becomes the data bus ($D_7 \sim D_0$) and loses its normal I/O functions. Port $P4_1$ and $P4_0$ become the SYNC and R/$\overline{W}$ pins respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]
When 10V is supplied to the CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. This mode has almost the same function as the memory expanding mode except that it needs all its programs to come from the outside (including ROM programs). The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

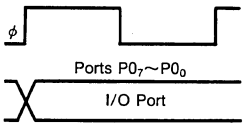
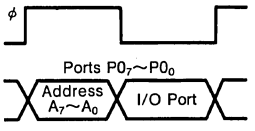
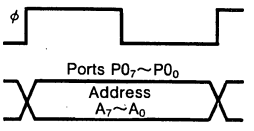
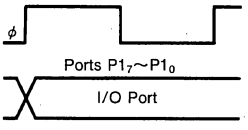
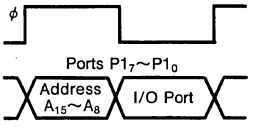
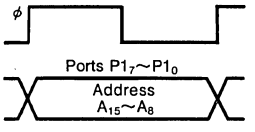
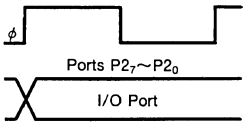
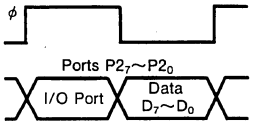
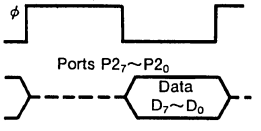
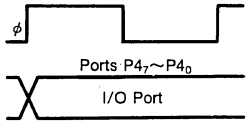
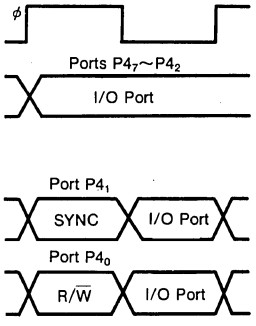
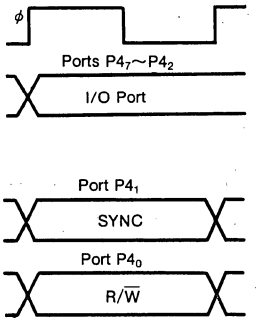
TM_1	0	0	1	1
TM_0	0	1	1	0
Mode / Port	Single-chip mode	Memory expanding mode	Eva-chip mode	Microprocessor mode
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	
Port P4			Same as left	

Fig. 23 Processor mode and functions of ports P0~P2, P4

Table 2. Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The M50944-XXXSP has two internal clock generating circuit. Figure 26 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ. Bit 7 of serial I/O_1 mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 24 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacture's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 25.

The M50944-XXXSP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case, $\phi/4$ is selected as timer 3 prescaler input. Before executing the STP instruction, appropriate values must be set in timer 3 prescaler and timer 3 to enable the oscillator to stabilize when restarting oscillation. And the timer 3 count stop bit must be set to supply ("0"), timer 3 interrupt enable bit must be set to enable ("1"), and timer 3 interrupt request bit must be set to no request ("0"), INT_2 or timer 3 interrupt enable bit must be set to disable ("0") and INT_2 or timer 3 interrupt request bit must be set to no request ("0").

Oscillation is restarted (release the stop mode) when INT_1, INT_2, $\overline{INT_3}$, $\overline{INT_4}$, or serial I/O_1 interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 3 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes because no wait time is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock (120μA max. at $f(X_{CIN}) = 32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of serial I/O_2 mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 27 shows the transition of states for the system clock.

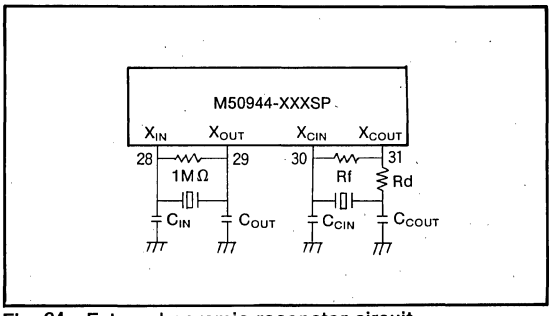


Fig. 24 External ceramic resonator circuit

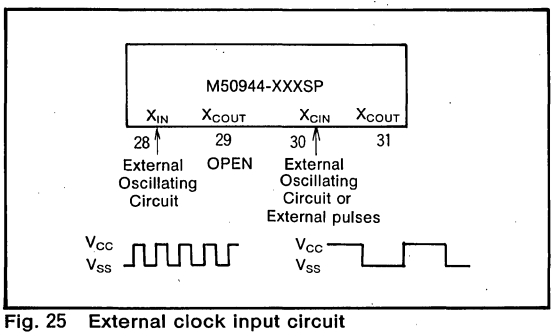


Fig. 25 External clock input circuit

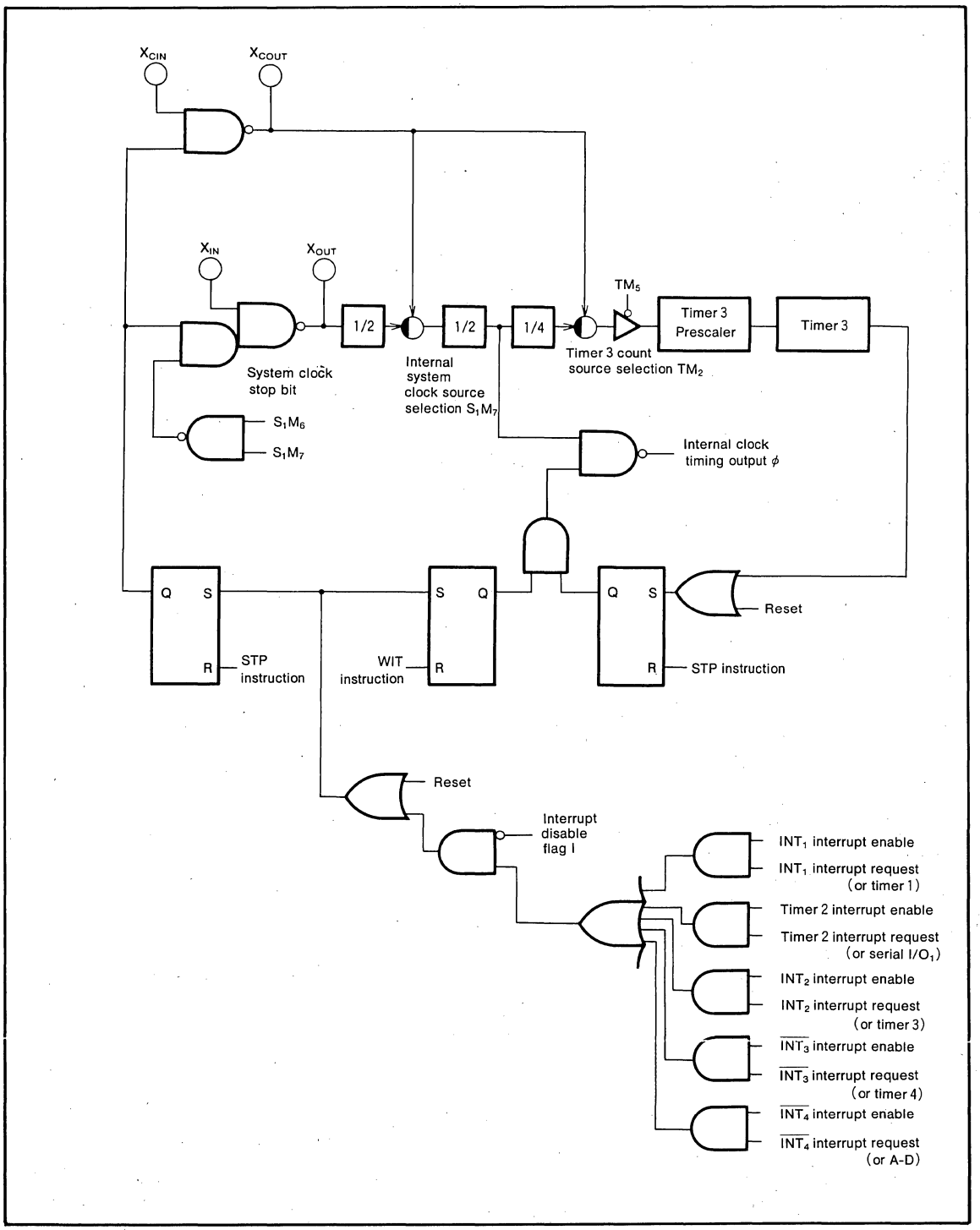
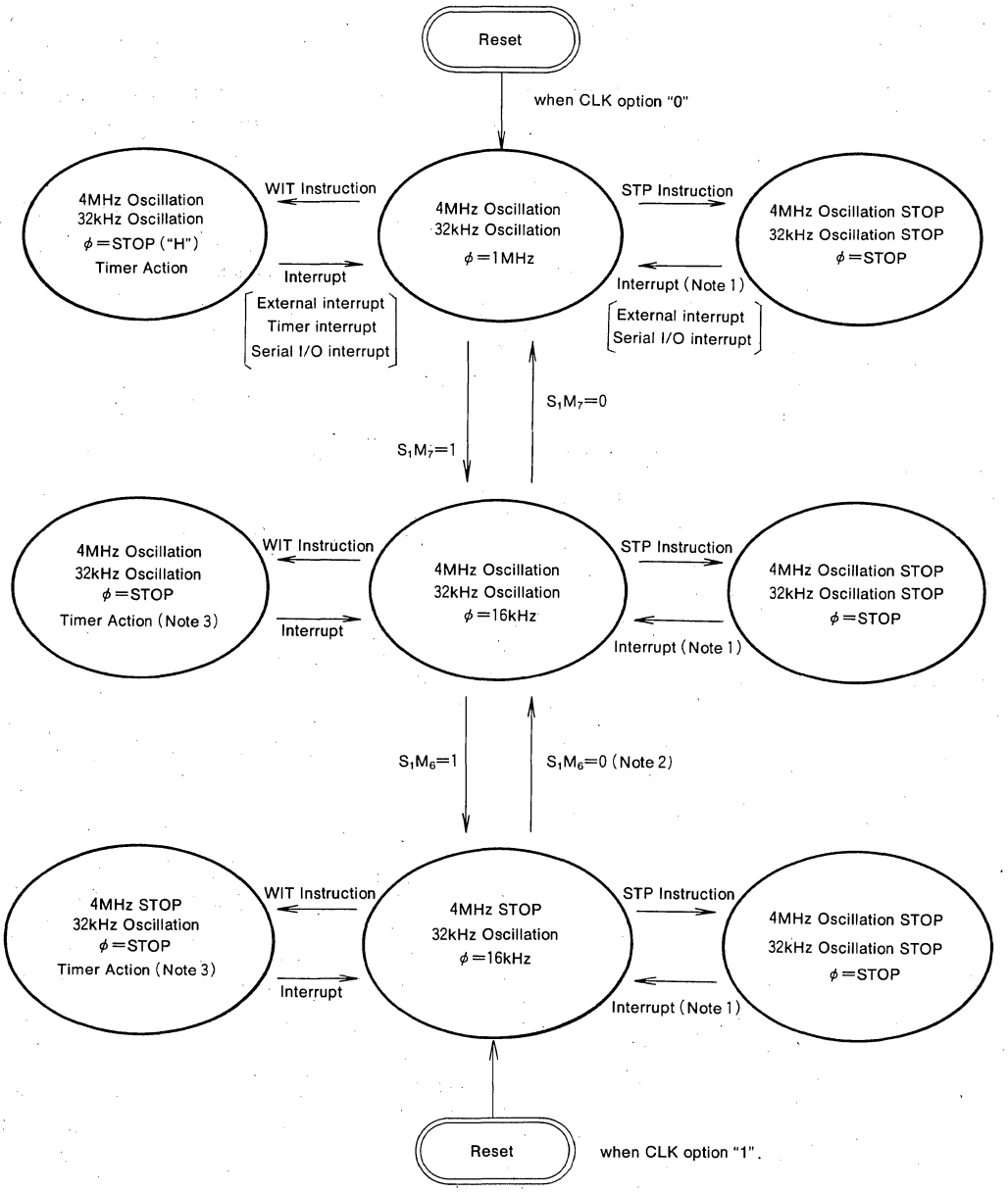


Fig. 26 Block diagram of clock generating circuit



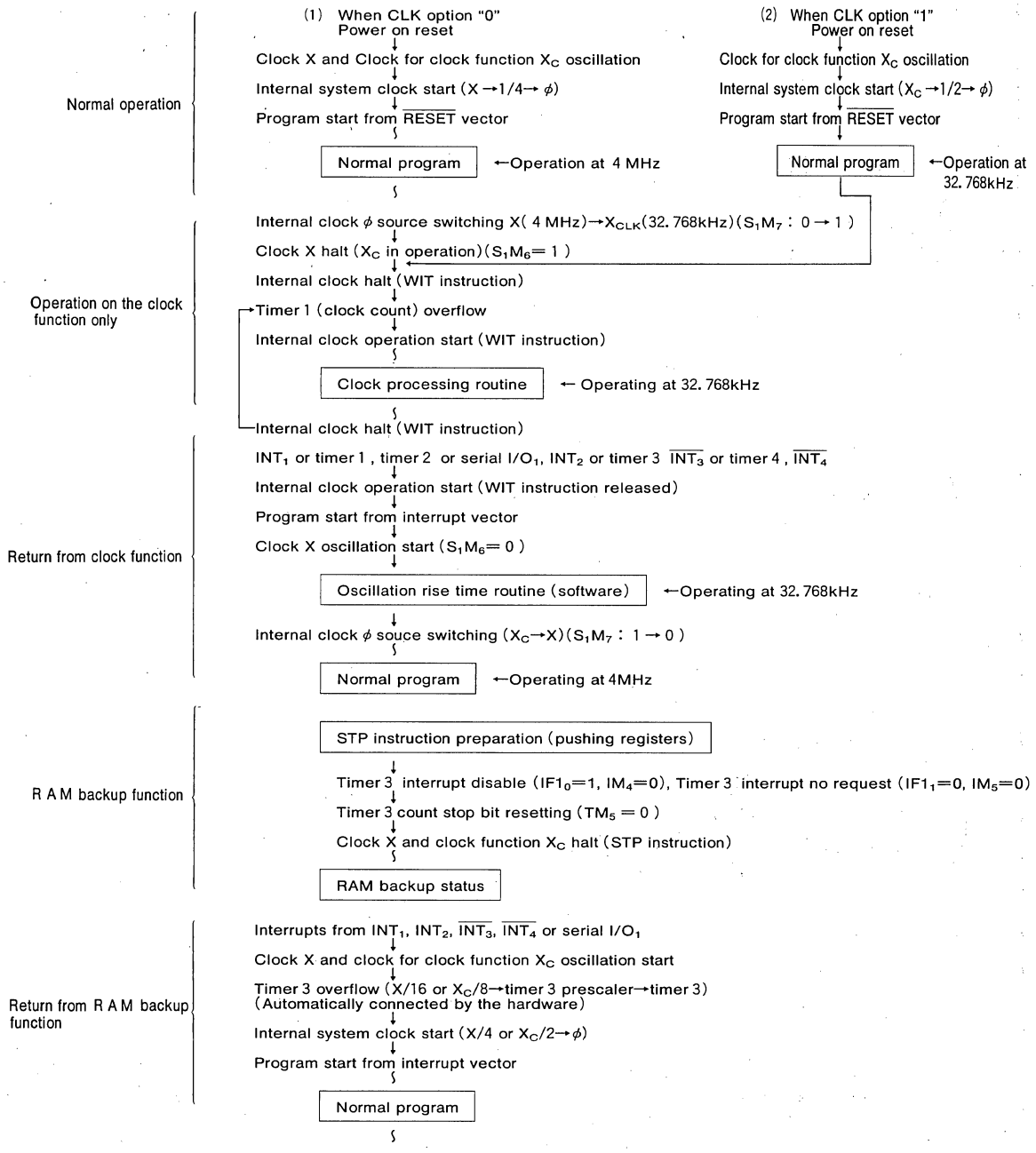
Note 1. At recovery from the STP Instruction, wait time occurs automatically by connecting timer 3 prescaler and timer 3. This time is set by the program.

2. When S_1M_6=1, and unsystem clock is operated, a programmed wait time may be necessary to allow the oscillator stabilize.

3. When connected the clock divided by four as the count source of timer, frequency of count source is 4kHz.

Fig.27 Transition of states for the system clock

≪An example of flow for system≫



PROGRAMING NOTES

(1) The frequency ratio of the timer is $1/(n+1)$. ($n=0\sim255$)
(2) When the timer 1, timer 2, timer 3 or timer 4 is input the clock except $\phi/4$ or it divided by timer, read the contents of these timers either while the input of these timers are not changing or after counting of timers are stopped.
(3) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD intructions are executed.
(5) A NOP instruction must be used after the execution of a PLP instruction.
(6) Notes on serial I/O_1
① Set "0" in the serial I/O_1 interrupt enable bit (bit 6 of address $00FF_{16}$) before setting the serial I/O_1 mode.
② Insert at least one instruction and set "0" in the serial I/O interrupt request bit (bit 7 of address $00FF_{16}$) after setting the serial I/O_1 mode.
③ Set "1" in the serial I/O_1 interrupt enable bit after the operation described in ②.
(7) The timer 3 prescaler and the timer 3 must be set the necessary value immediately before the execution of a STP instruction.
(8) The V_{REF} pin must be kept open or connected to V_{SS} at the low power dissipation mode.
(9) Use the LDA (immidiate, T = 1) instruction to modify the interrupt request distinguish register. SEB and CLB instructions can be used only when interrupts in the register are not generated at executing these instructions.
(10) Do not write any data into an address where no register nor port is assigned.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ····· EPROM 3 sets

Write the following option on the mask ROM cofirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port P4 pull-up transistor bit
- Clock source option at reset
- STP instruction

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output Transistors are at "OFF" state.	−0.3∼7	V
V_I	Input voltage CNV_{SS}, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$		−0.3∼13	V
V_I	Input voltage R_0∼R_3, X_{IN}, X_{CIN}, $\overline{RESET}$		−0.3∼7	V
V_I	Input voltage $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, IN_0∼IN_7, V_{REF}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P3_0$∼$P3_7$,$P4_0$∼$P4_7$, X_{COUT}, X_{OUT}, ϕ		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$		−0.3∼13	V
Pd	Power Dissipation	T_a=25℃	1000(Note 1)	mW
Topr	Operating Temperature		−10∼70	℃
Tstg	Storage Temperature		−40∼125	℃

Note 1. 600mW for QFP type.

RECOMMEND OPERATING CONDITIONS

(V_{CC}= 5 V±10%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Nom.	Max.	
V_{CC}	Supply voltage	$f(X_{IN})$=4MHz	4.5	5	5.5	V
		$f(X_{IN})$≦1MHz	3	5	5.5	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, IN_0∼IN_7,CNV_{SS}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage R_0∼R_3		0.4V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$		0.8V_{CC}		12	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, IN_0∼IN_7, CNV_{SS}		0		0.2V_{CC}	V
V_{IL}	"L" input voltage R_0∼R_3		0		0.12V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0.16V_{CC}	V
$I_{OL(sum)}$	"L" sum output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$				60	mA
$I_{OH(sum)}$	"H" sum output current $P3_0$∼$P3_7$, $P4_0$∼$P4_7$				−30	mA
$I_{OL(sum)}$	"L" sum output current $P3_0$∼$P3_7$, $P4_0$∼$P4_7$				60	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$				20	mA
$I_{OH(peak)}$	"H" peak output current $P3_0$∼$P3_7$, $P4_0$∼$P4_7$				−10	mA
$I_{OL(peak)}$	"L" peak output current $P3_0$∼$P3_7$, $P4_0$∼$P4_7$				20	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$				10	mA
$I_{OH(avg)}$	"H" average output current $P3_0$∼$P3_7$, $P4_0$∼$P4_7$				−5	mA
$I_{OL(avg)}$	"L" average output current $P3_0$∼$P3_7$, $P4_0$∼$P4_7$				10	mA
$f_{(X_{IN})}$	Clock oscillating frequency	V_{CC}=5V			4.3	MHz
		V_{CC}=3V			1.1	
$f_{(X_{CIN})}$	Clock oscillating frequency for clock function	V_{CC}=5V			500	kHz
		V_{CC}=3V			300	

Note 1. The maximum "H" input voltage for CNV_{SS} is +12V.
2. The duty cycle for these oscillation frequency is 50%.
3. When the low speed mode is used, the clock input oscillation frequency for the timer must satisfy the following expression : $f(X_{CIN}) < f(X_{IN})/3$
4. The avarage output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms cycle.
5. $f_{(X_{CIN})}$ must be less than 50kHz when the external clock is to be used.

ELECTRICAL CHARACTERISTICS (V_{CC}= 5 V±10%, V_{SS}= 0 V, T_a=25℃, f(X_{IN})= 4 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			
V_{OH}	"H" output voltage ϕ	V_{CC}=5V, I_{OH}=−2.5mA		3			V
		V_{CC}=3V, I_{OH}=−0.8mA		2			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
V_{OL}	"L" output voltage ϕ	V_{CC}=5V, I_{OL}=2.5mA				2	V
		V_{CC}=3V, I_{OL}=0.8mA				1	
V_{T+}−V_{T-}	Hysteresis $P3_0/INT_1$, $P3_1/INT_2$ $P4_2/\overline{INT_3}$, $P4_3/\overline{INT_4}$	use as interrupt input	V_{CC}=5V	0.3		1	V
			V_{CC}=3V	0.15		0.7	
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5	0.7	V
		V_{CC}=3V			0.35		
V_{T+}−V_{T-}	Hysteresis $P3_6/CLK_1$, $P4_6/CLK_2$	use as CLK input	V_{CC}=5V	0.3		1	V
			V_{CC}=3V	0.15		0.7	
V_{T+}−V_{T-}	Hysteresis X_{IN}	V_{CC}=5V		0.1		0.5	V
		V_{CC}=3V		0.06		0.3	
V_{T+}−V_{T-}	Hysteresis $P3_2$/CNTR	Use as CNTR input	V_{CC}=5V	0.3		1	V
			V_{CC}=3V	0.15		0.7	
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$ $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_I=0V without pull-up T_r.	V_{CC}=5V			−5	μA
			V_{CC}=3V			−4	
		V_I=0V, with pull-up T_r.	V_{CC}=5V	−35	−70	−140	
			V_{CC}=3V	−12	−25	−40	
I_{IL}	"L" input current IN_0~IN_7	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−4	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}, R_0~R_3	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−4	
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_I=5V, without pull-up transistor				5	μA
I_{IH}	"H" input current IN_0~IN_7	V_I=5V, not use as analog input				5	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}, R_0~R_3	V_I=5V				5	μA
I_{IH}	"H" input current V_{REF}	V_I=5V				5	mA
I_{CC}	Supply current	Open output ports, V_P=V_{CC}, Input port is V_{SS}, at normal operation.	X_{IN}=4MHz, V_{CC}=5V		3	6	mA
			X_{IN}=1MHz, V_{CC}=3V		0.4		
		Open output ports, V_P=V_{CC}, Input port is V_{SS}, at wait mode.	X_{IN}=4MHz, V_{CC}=5V		1		mA
			X_{IN}=1MHz, V_{CC}=3V		0.2		
		Open output ports, V_P=V_{CC}, Input port is V_{SS}, at normal operation, stop X_{IN} and X_{OUT}, X_{CIN}=32kHz.	V_{CC}=5V		60	200	μA
			V_{CC}=3V		25		
		Open output ports, V_P=V_{CC}, Input port is V_{SS}, at wait mode, stop X_{IN} and X_{OUT}, X_{CIN}=32kHz.	V_{CC}=5V		40		μA
			V_{CC}=3V		15		
		Stop all oscillation.	T_a=25℃, V_{CC}=5V		0.1	1	μA
			T_a=25℃, V_{CC}=3V		0.06		
			T_a=70℃, V_{CC}=5V		1	10	
			T_a=70℃, V_{CC}=3V		0.6		
I_{ACC}	Supply current for A-D	at A-D converting time			2	4	mA

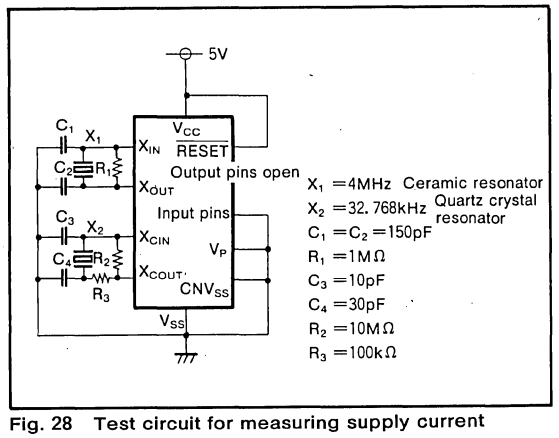


Fig. 28 Test circuit for measuring supply current

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Absolute accuracy	V_{CC}=AV_{CC}=V_{REF}=5.12V			±3	LSB
R_{LADDER}	Ladder resistor value		1			kΩ
t_{CONV}	Conversion time	High-speed : ϕ=1MHz			72	μs
		Low-speed : ϕ=1MHz			288	μs
V_{REF}	Reference input voltage				V_{CC}	V
V_{IA}	Analog input voltage				V_{REF}	V

TIMING REQUIREMENTS

Single-chip mode (V_{CC}= 5 V±10%, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless other wise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		270			ns
$t_{su(RD-\phi)}$	Port R input setup time		270			ns
$t_{su(IND-\phi)}$	Port IN input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		20			ns
$t_{h(\phi-RD)}$	Port R input hold time		20			ns
$t_{h(\phi-IND)}$	Port IN input hold time		20			ns
$t_{C(X_{IN})}$	External clock input cycle time (X_{IN})		230			ns
$t_{W(X_{IN})}$	External clock input pulse width (X_{IN})		75			ns
$t_{C(X_{CIN})}$	External clock input cycle time (X_{CIN})		2			ms
$t_{W(X_{CIN})}$	External clock input pulse width (X_{CIN})		1			ms
t_r	External clock rising edge time				25	ns
t_f	External clock falling edge time				25	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 29			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				230	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 29			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P4_0Q)}$	Port $P4_0$ data output delay time				200	ns
$t_{d(\phi-P4_0QF)}$	Port $P4_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P4_1Q)}$	Port $P4_1$ data output delay time				200	ns
$t_{d(\phi-P4_1QF)}$	Port $P4_1$ data output delay time				200	ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 29			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

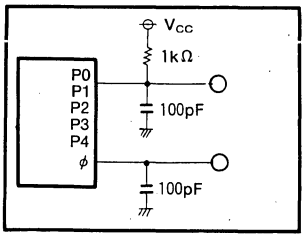
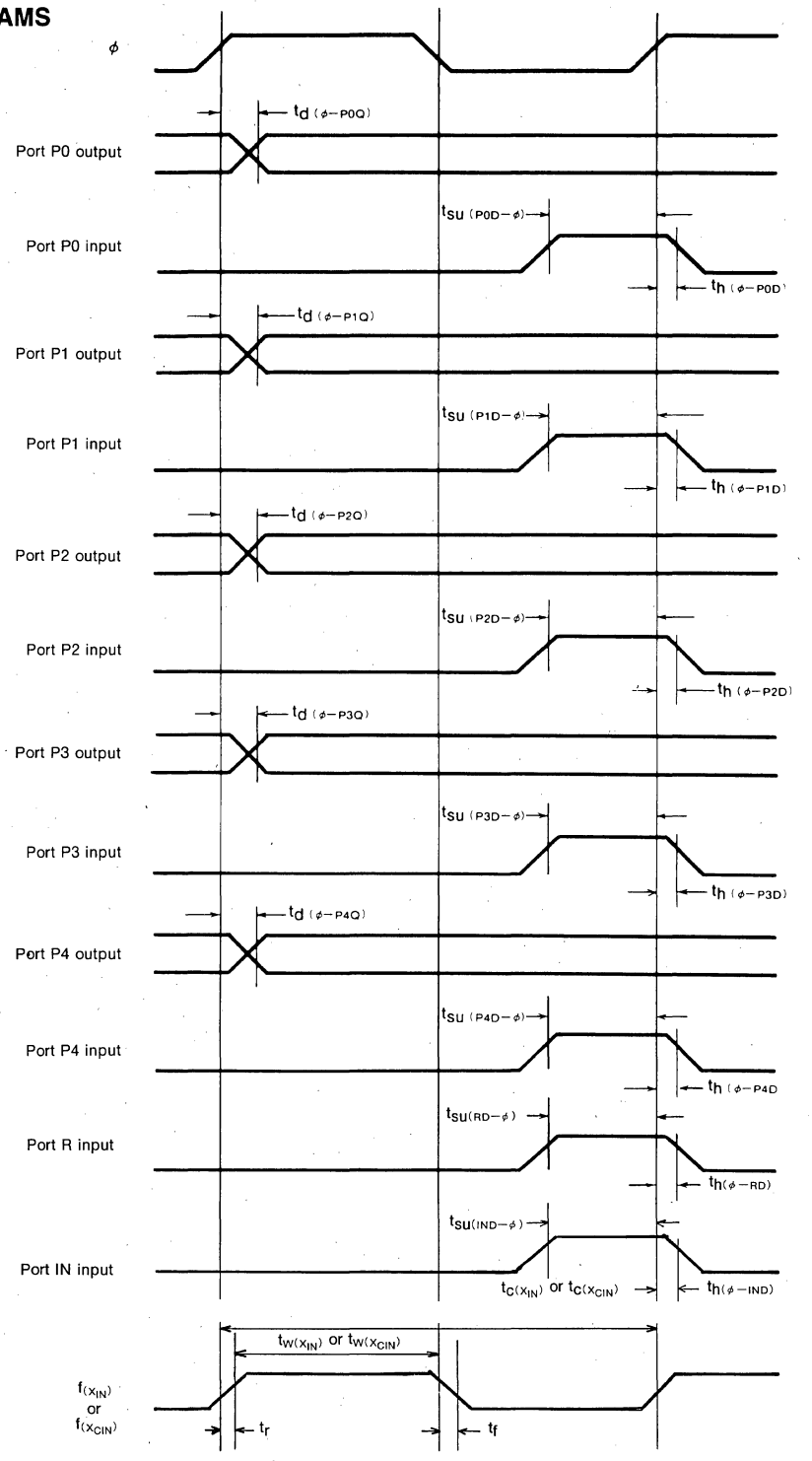


Fig. 29 Test circuit of ports P0～P4

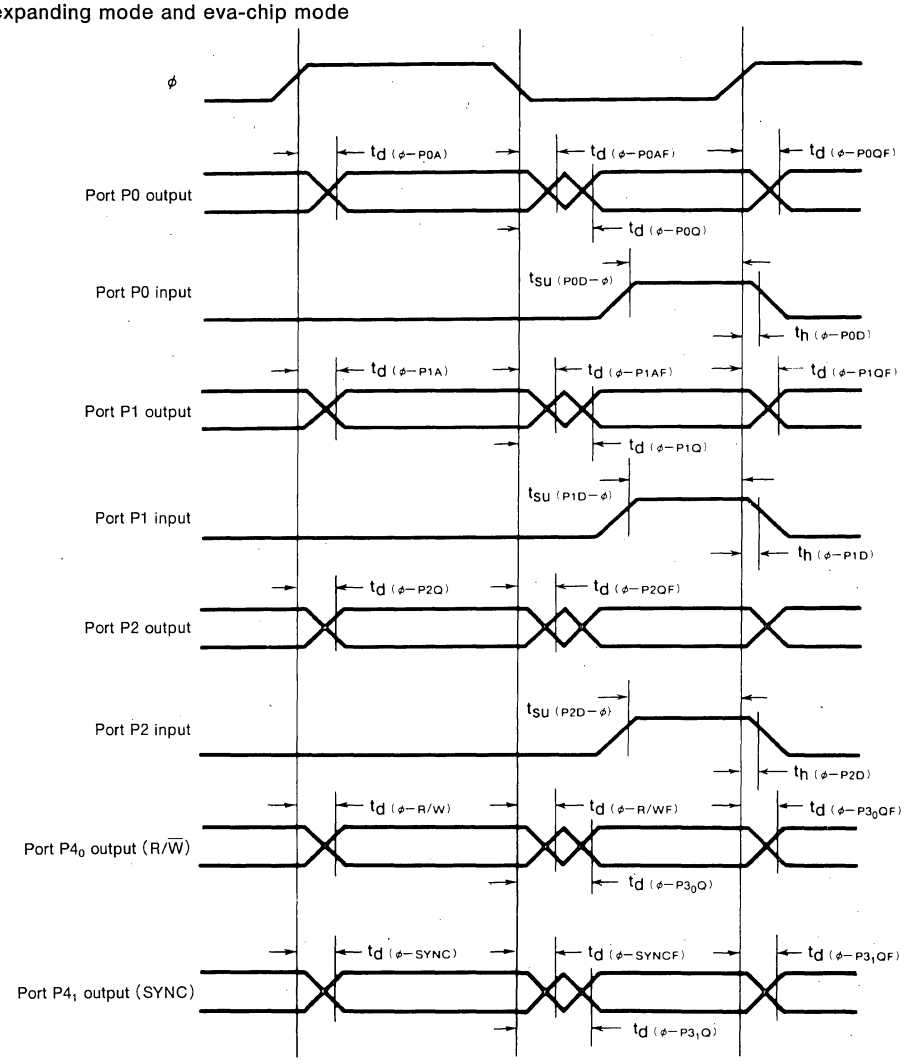
TIMING DIAGRAMS

In single-chip mode

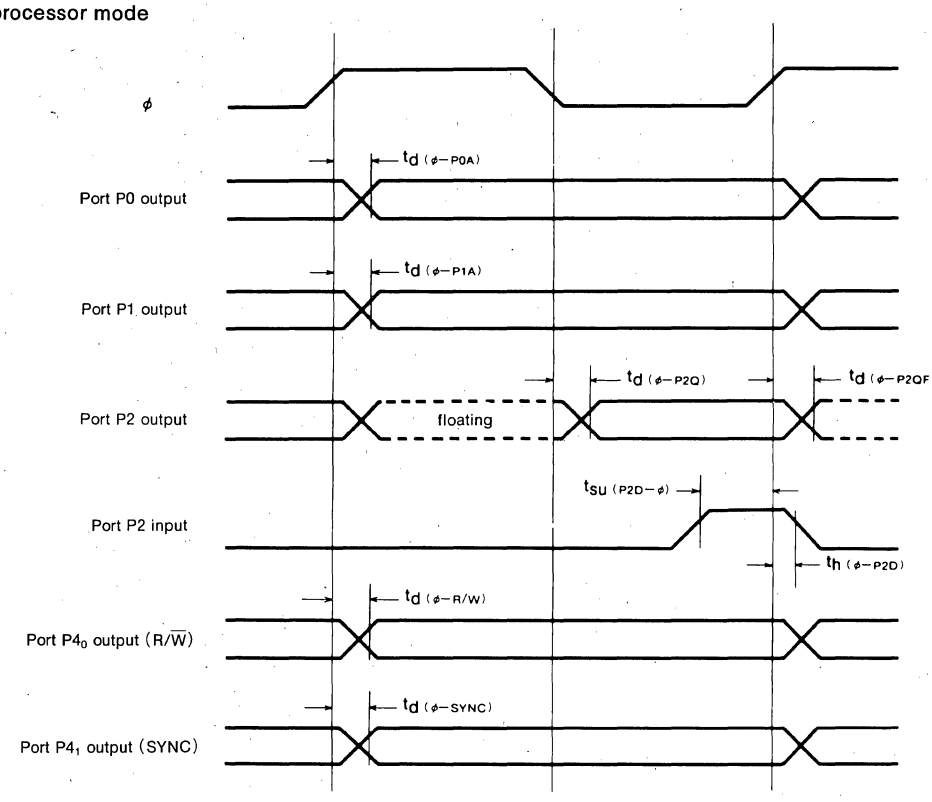


MITSUBISHI ELECTRIC

In memory expanding mode and eva-chip mode



In microprocessor mode



M50950-XXXSP
M50951-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50950-XXXSP and the M50951-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. Both are housed in a 52-pin shrink plastic molded DIP.

These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

These microcomputers are also suitable for applications which require fluorescent display tubes.

The differences between the M50950-XXXSP and the M50951-XXXSP are noted below. The following explanations apply to the M50950-XXXSP. Specification variations for other chips, these are noted accordingly.

Type name	ROM size
M50950-XXXSP	6144bytes
M50951-XXXSP	4096bytes

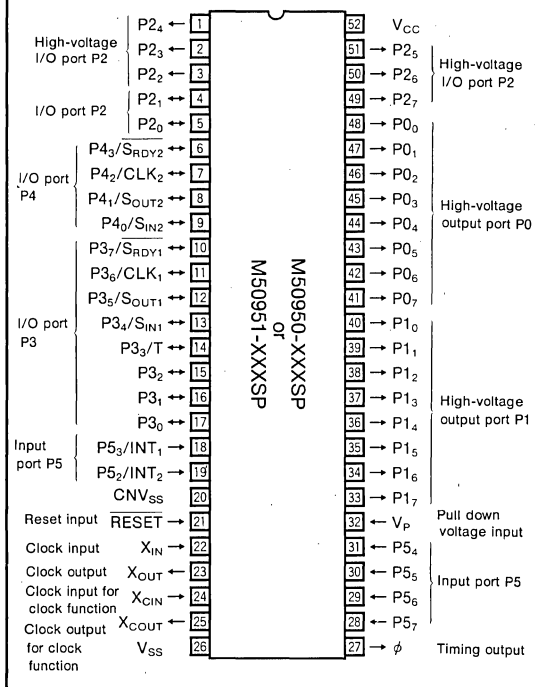
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 6144 bytes (M50950-XXXSP)
  4096 bytes (M50951-XXXSP)
  RAM ..... 144 bytes
- Instruction execution time
  ..... 1.6μs (minimum instructions, at 5MHz frequency)
- Single power supply f (X_{IN})=5MHz ..... 5V$\pm$10%
- Power dissipation
  normal operation mode (at 5MHz frequency) 20mW
  low-speed operation mode (at 32kHz frequency for clock function) 0.4mW
- Subroutine nesting ..... 72 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as serial I/O_1)
- Programmable I/O ports (Ports $P2_0$, $P2_1$, P3, P4) 14
- Input ports (Port P5) 6
- High-voltage output ports (Ports P0, P1, $P2_2$~$P2_7$) 22
- Serial I/O (8-bit) 2
- Two clock generator circuit (One is for main clock, the other is for clock function)

APPLICATION

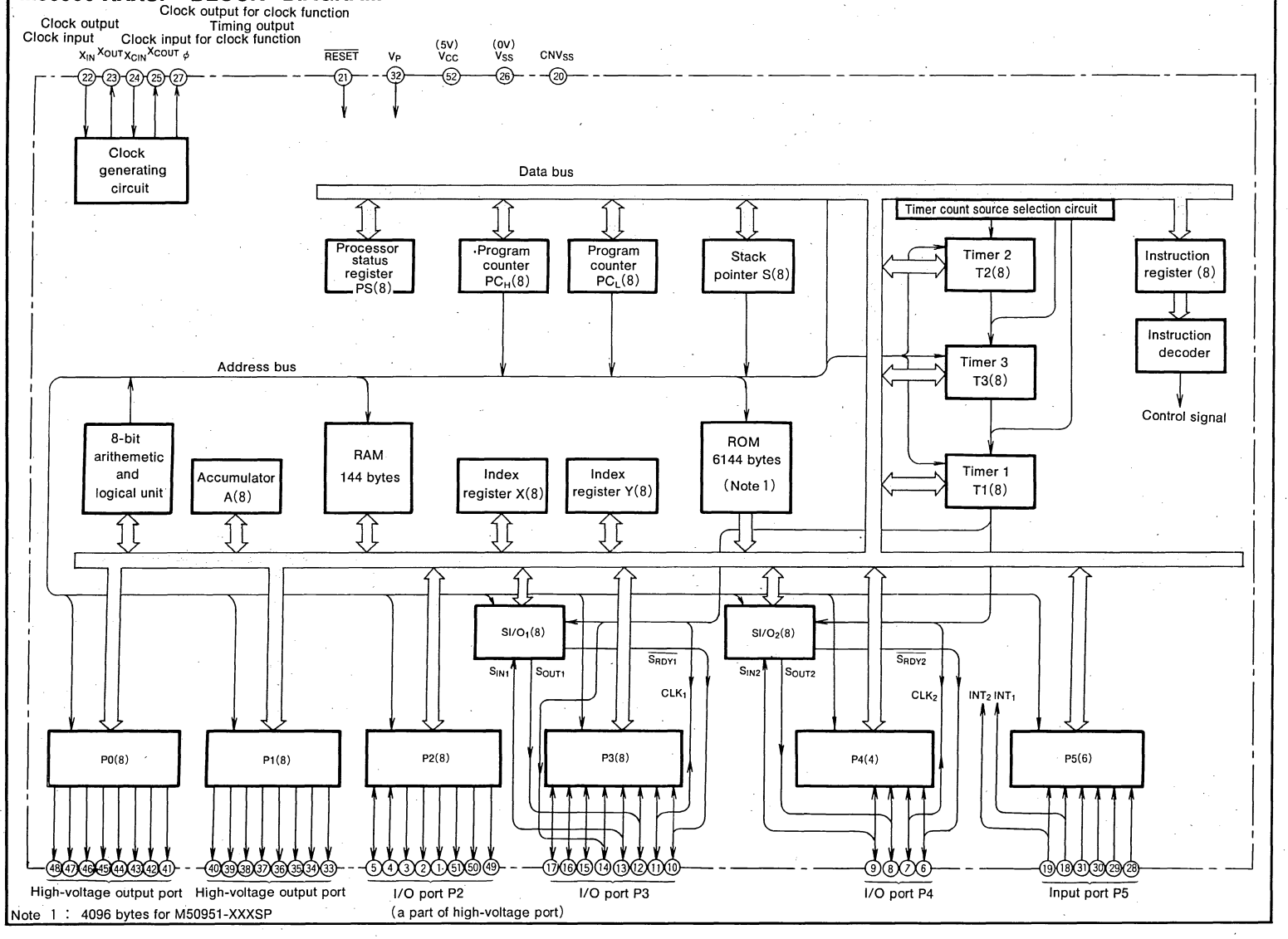
Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 52P4B

M50950-XXXSP BLOCK DIAGRAM



Note 1 : 4096 bytes for M50951-XXXSP

MITSUBISHI ELECTRIC

FUNCTIONS OF M50950-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1.6μs (minimum instructions, at 5MHz frequcncy)
Clock frequency			5MHz
Memory size	ROM		6144bytes (4096bytes for M50951-XXXSP)
	RAM		144bytes
Input/Output ports	P0, P1	Output	8-bitX2 (high-voltage P-channel transistor : V_{CC}−36V)
	$P2_2$~$P2_7$	Output	6-bitX1 (high-voltage P-channel transistor : V_{CC}−36V)
	$P2_0$, $P2_1$	I/O	2-bitX1 (N-channel open drain)
	P3	I/O	8-bitX1 (a part is used both as serial I/O_1 and I/O port)
	P4	I/O	4-bitX1 (used both as serial I/O_2 and I/O port)
	P5	Input	6-bitX1 (a part is used both as INT_1, INT_2 and I/O port)
Serial I/O			8-bitX2
Timers			8-bit timerX3 (2 when serial I/O is used)
Subroutine nesting			72 levels (max)
Interrupts			Two external interrupts, Three internal timer interrupts (or timerX2, S I/O_1X1)
Clock generating circuit			Two build-in circuits (ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	at high-speed operation		20mW (clock frequency X_{IN}=5MHz)
	at low-speed operation		0.4mW (clock frequency X_{CIN}=32kHz)
	at stop mode		1μA (at clock stop)
Input/Output characteristic	Input/Output voltage		12V (Input/Output $P2_0$, $P2_1$, P3, P4)
			V_{CC}−36V (output P0, P1, $P2_2$~$P2_7$)
	Output current		10mA ($P2_0$, $P2_1$, P3, P4)
			−12mA (P0, P1, $P2_2$~$P2_7$: high-voltage P-channel transistor)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package			52-pin shrink plastic molded DIP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P0, P1 and $P2_2$~$P2_7$.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open. This clock can be used as a program controlled the system clock.
X_{COUT}	Clock output for clock function	Output	
$P0_0$~$P0_7$	Output port P0	Output	Port P0 is an 8-bit output port. Output structure is high-voltage P-channel open drain. A pull-down transistor is built in between the V_P pin and this port. At reset, this port is set to a "L" level.
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is a 2-bit I/O port ($P2_0$, $P2_1$) and a 6-bit high-voltage P-channel outputt port ($P2_2$~$P2_7$). For $P2_0$ and $P2_1$, output structure is N-channel open drain. A pull-down transistor is built in between the V_P pin and $P2_2$~$P2_7$.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port. When serial I/O_1 is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY1}}$, CLK_1, S_{OUT1}, and S_{IN1} pins, respectively. $P3_3$ can be used as programmable output pin for the timer 1 overflow signal divided by 2.
$P4_0$~$P4_3$	I/O port P4	I/O	Port P4 is an 4-bit I/O port. When serial I/O_2 is used, $P4_3$, $P4_2$, $P4_1$, and $P4_0$ work as $\overline{S_{RDY2}}$,CLK_2, S_{OUT2}, and S_{IN2} pins, respectively.
$P5_2/INT_2$ $P5_3/INT_1$	Input port P5	Input	Bits 2 and 3 of port P5 are 2-bit input port and are in common with interrupt inputs.
$P5_4$~$P5_7$		Input	Bits 4~7 of port P5 are 4-bit input port.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50950-XXXSP is shown in Figure 1. Addresses $E800_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 6144 bytes.

Addresses $F000_{16}$ to $FFFF_{16}$ are the ROM address area assigned to the M50951-XXXSP.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $008F_{16}$ are assigned to the built-in RAM and consist of 144 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

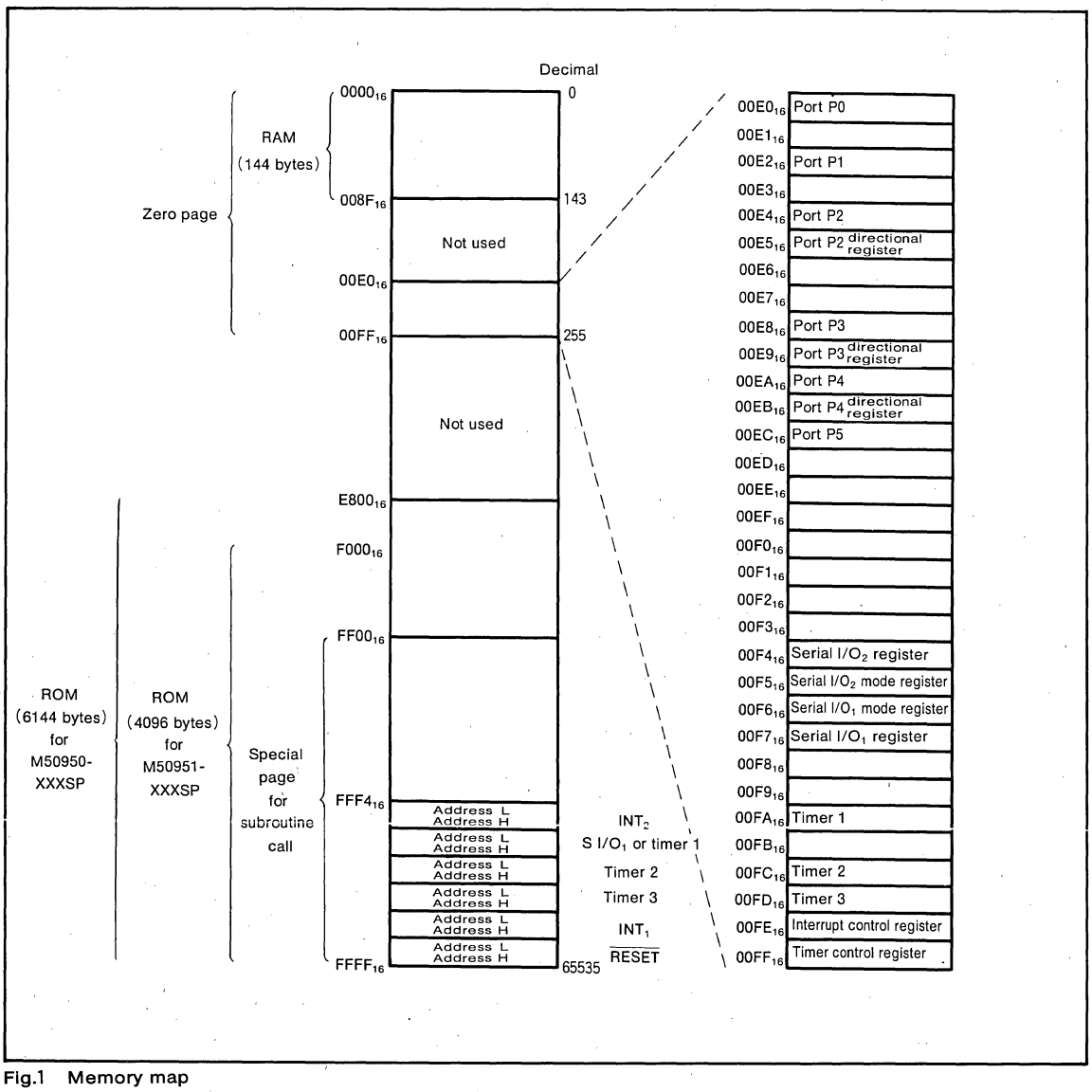


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

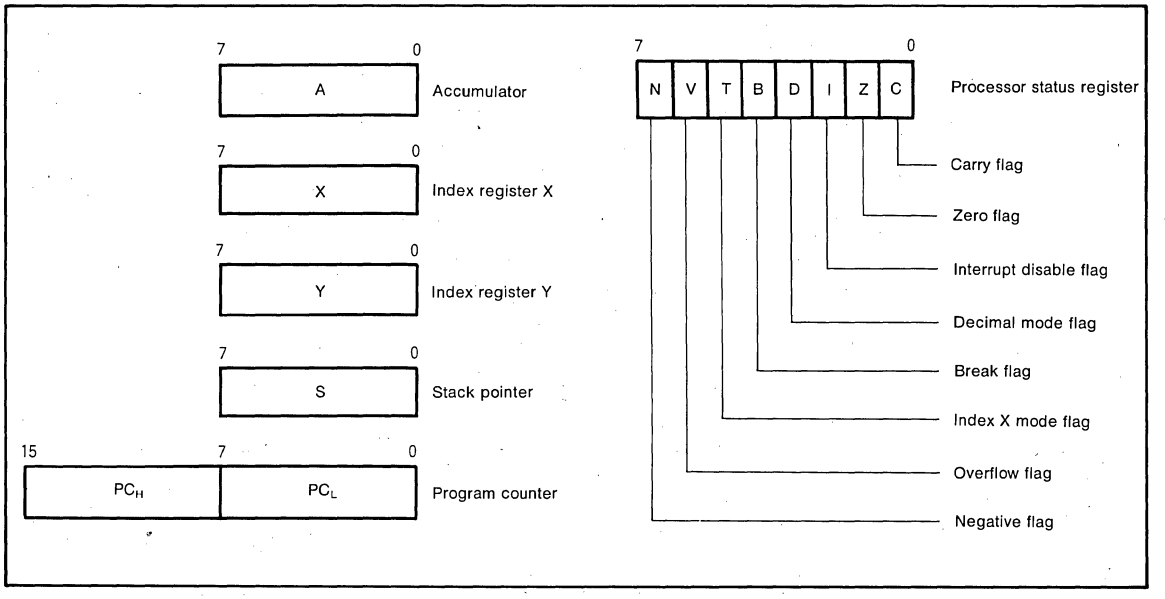


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When using this microcomputer in the single-chip mode, the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i. e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{\text{INT}_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer 3	3	$FFFB_{16}$, $FFFA_{16}$
Timer 2	4	$FFF9_{16}$, $FFF8_{16}$
Timer 1 or serial I/O_1	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{\text{INT}_2}$ (BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50950-XXXSP can be interrupted from seven sources; $\overline{\text{INT}_1}$, Timer 3, Timer 2, Timer 1/Serial I/O_1, or the $\overline{\text{INT}_2}$/BRK instruction.

The value of bit 2 of the serial I/O_1 mode register (address $00F6_{16}$) determines whether the interrupt is from timer 1 or from serial I/O_1. When bit 2 is "1" the interrupt is from serial I/O_1, and when bit 2 is "0" the interrupt is from timer 1. Also, when the bit 2 is "1", parts of port 3 are used for serial I/O_1. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupt.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt inhibit flag (I) is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupts are inhibited when the interrupt inhibit flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and

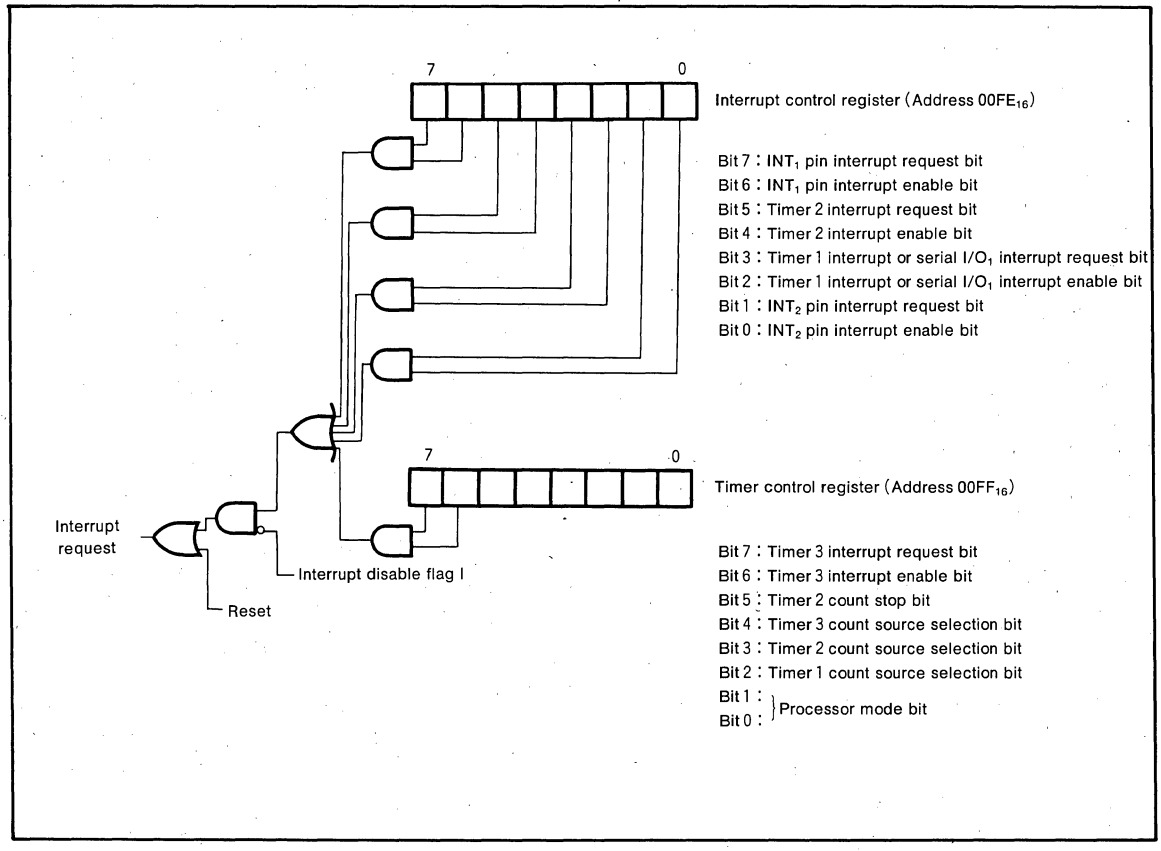


Fig.3 Interrupt control

the interrupt request bit are both "1" and the interrupt inhibit flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the levels of pins INT_1 and INT_2 change.
(2) When the contents of timer 3, timer 2, timer 1 (or the serial I/O_1 counter) go to "0".

The level shift on the INT pins causing an interrupt varies depending on the contents of bits 5 and 6 of the serial I/O_2 mode register (address $00F5_{16}$). When these bits are set to "0" and the INT level changes from "H" to "L", an interrupt is requested. When these bits are set to "1" and the INT level changes from "L" to "H", an interrupt is requested. Bits 5 (S_2M_5) and 6 (S_2M_6) correspond to INT_1 and INT_2, respectively.

These request bits can be reset by the program but can not be set.

Since the BRK instruction and the INT_2 interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if INT_2 generated the interrupt.

TIMER

The M50950-XXXSP has three timers; timer 1, timer 2, and timer 3. Since P3 (in serial I/O_1 mode) and timer 1 use some of the same architecture, they cannot be used at the same time (see serial I/O_1 section). The count source for each timer can be selected by using bit 2, 3 and 4 of the timer control register (address $00FF_{16}$), as shown in Figure 4.

A block diagram of timer 1 through 3 is shown in Figure 5. All of the timers are down count timers and have 8-bit latches. When a timer counter reaches "0", the contents of the reload latch are loaded into the timer at the next clock pulse. The division ratio of the timers is 1/(n+1), where n is the contents of the timer latch.

The timer interrupt request bit is set to "1" at the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section). The starting/stopping of timer 2 can be controlled by bit 5 of the timer control register. If bit 5 (address $00FF_{16}$) is "0", the timer starts counting and when bit 5 is "1", the timer stops.

When the STP instruction is executed, or after reset, the timer 2 and timer 3 latch are set to FF_{16} and 07_{16}, respectivery.

After a STP instruction is executed, timer 2, timer 3, and the clock (ϕ divied by 4) are connected in series (regardless of the status of bit 2 through 4 of the timer control register). This state is canceled if the timer 3 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 2 count stop bit) and bit 4 of the interrupt control register (timer 2 interrupt enable bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

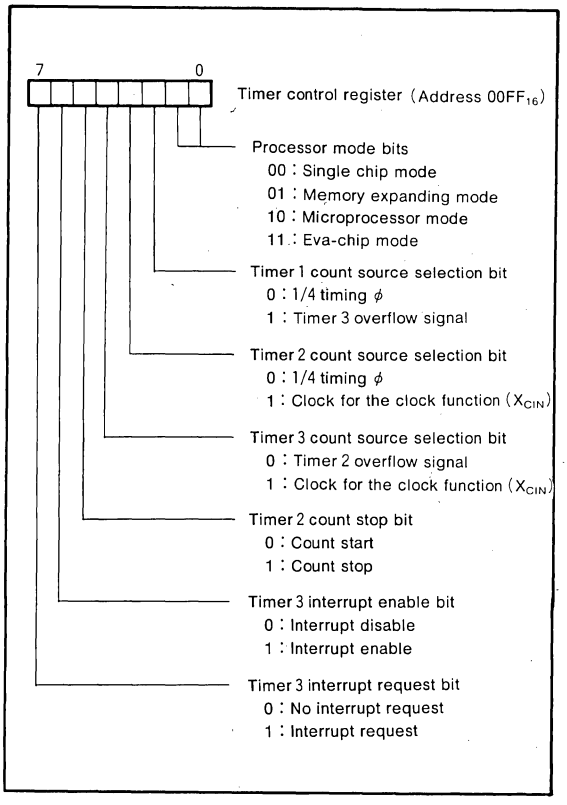


Fig.4 Configuration of timer control register

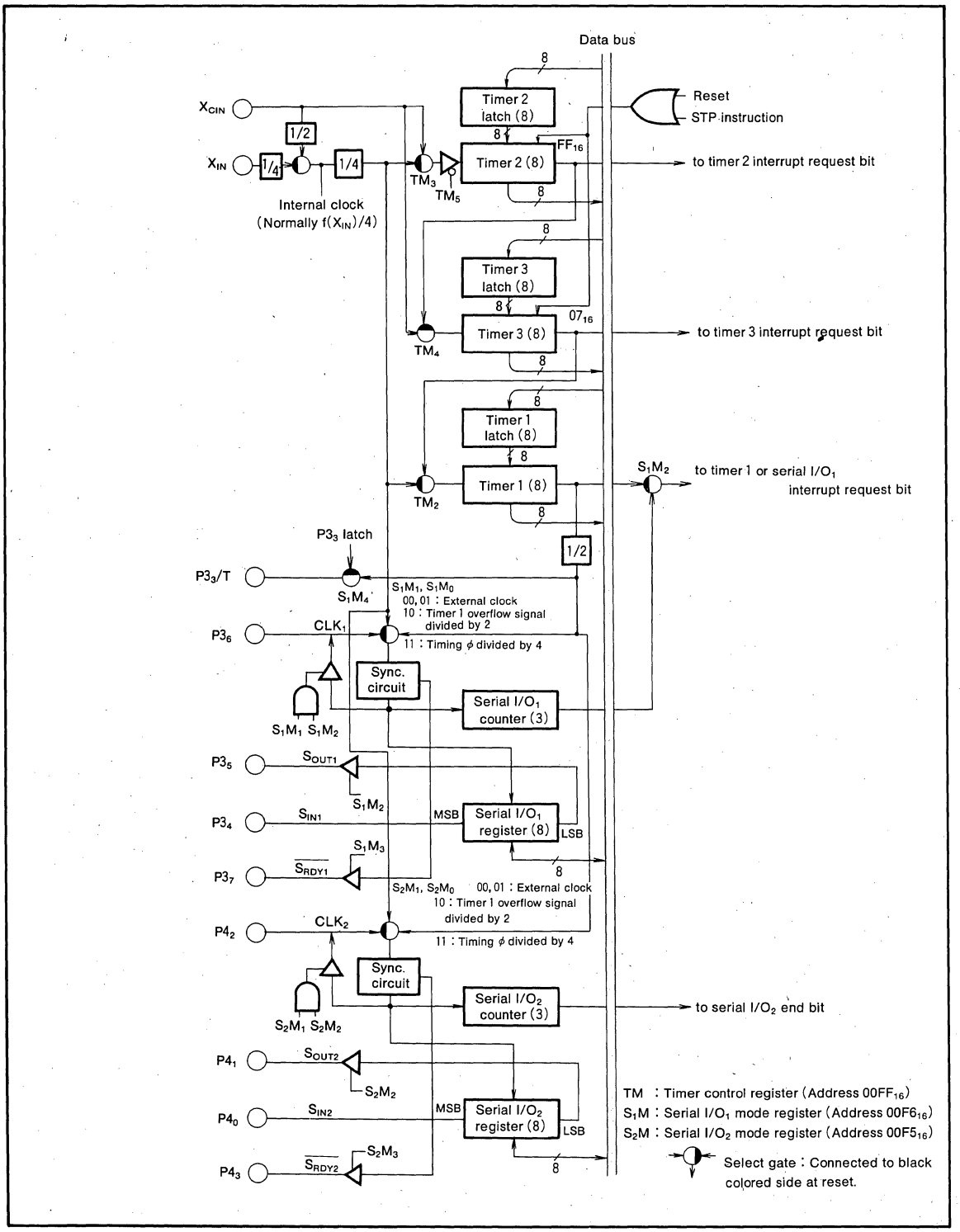


Fig.5 Block diagram of timer 1, timer 2 and timer 3

SERIAL I/O_1

A block diagram of the serial I/O_1 is shown in Figure 6.

In the serial I/O_1 mode the receive ready signal ($\overline{S_{RDY1}}$), synchronous input /output clock (CLK_1), and the serial I/O_1 pins (S_{OUT1}, S_{IN1}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively.

The serial I/O_1 mode register (address $00F6_{16}$) is an 8-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 1, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the timing ϕ divided by 4, becomes the clock.

Bit 2 and 3 decide whether parts of P3 will be used as a serial I/O_1 or not. When bit 2 is a "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

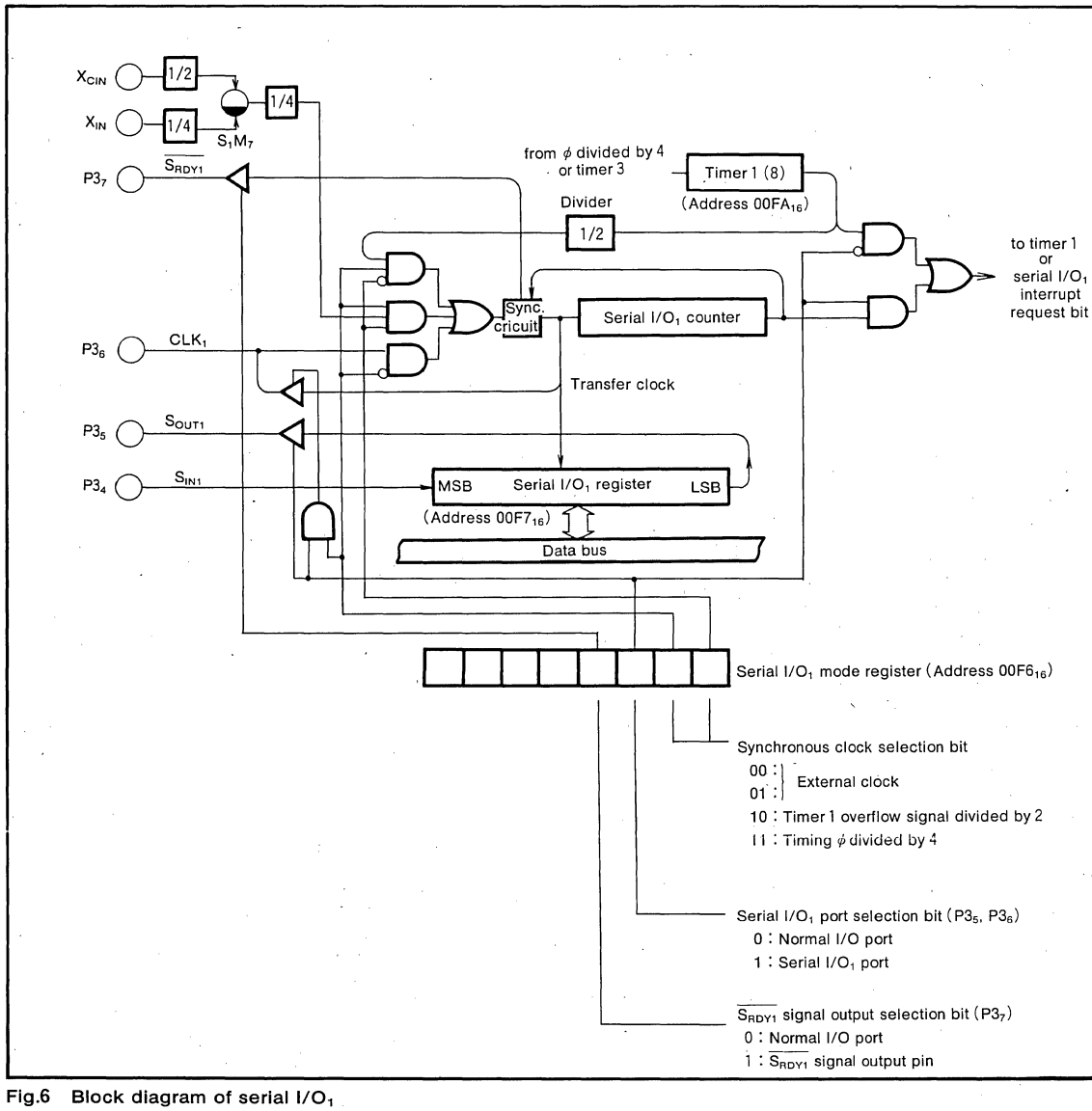


Fig.6 Block diagram of serial I/O_1

To use the serial I/O_1, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O_1 counter instead of timer 2. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3=1, $\overline{S_{RDY1}}$) or used as normal I/O pin (bit 3=0). The serial I/O_1 function is discussed below. The function of the serial I/O_1 differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY1}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O_1 register (address $00F7_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY1}}$ signal becomes low signaling that the M50950-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY1}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O_1 counter is set to 7 when data is stored in the serial I/O_1 register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O_1 register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O_1 register will be empty and the transfer clock will remain at a high level. At this time the interrpt request bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but the transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 7. An example of communication between two M50950-XXXSPs is shown in Figure 8.

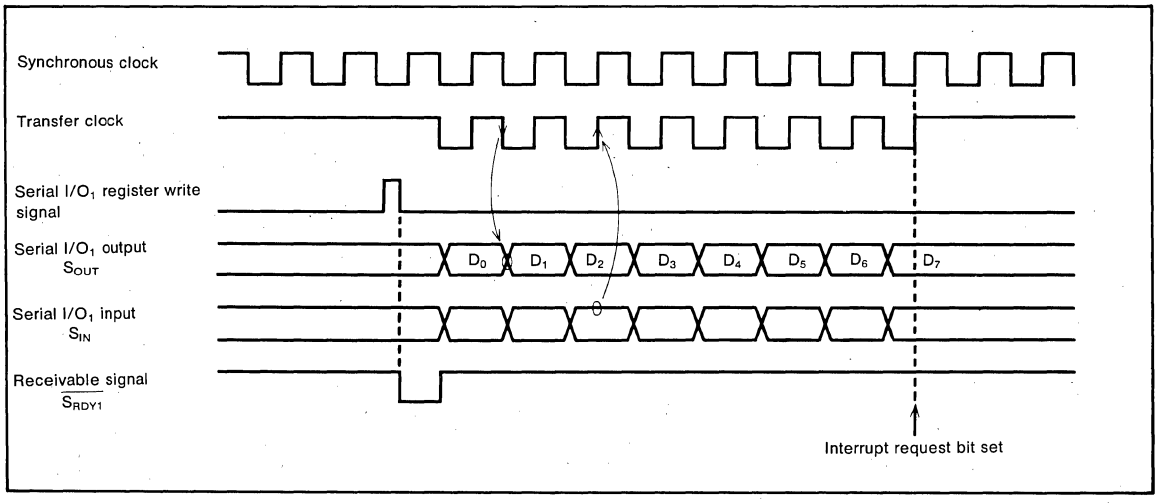


Fig.7 Serial I/O_1 timing

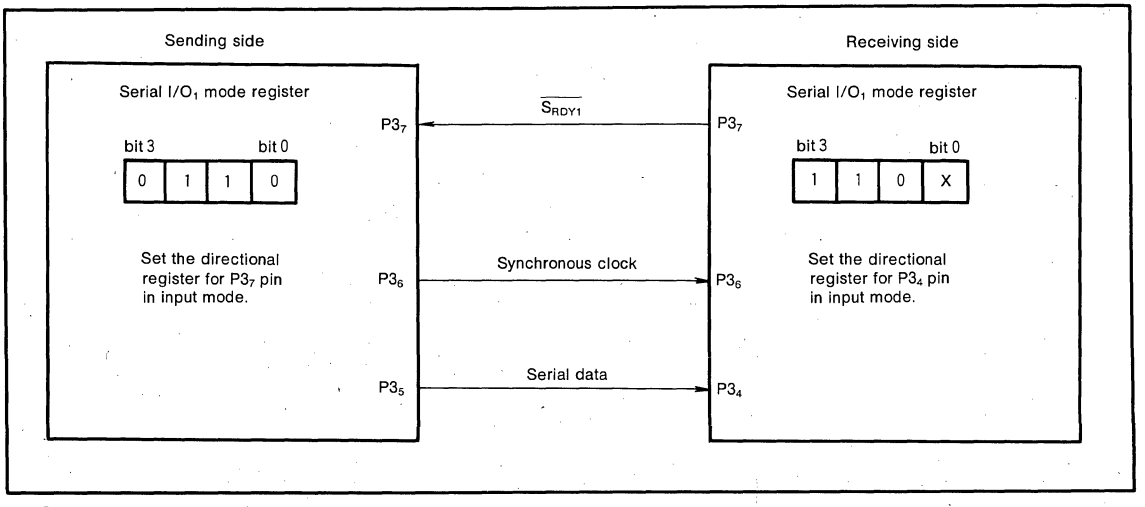


Fig.8 Example of serial I/O_1 connection

SERIAL I/O_2

A block diagram of the serial I/O_2 is shown in Figure 9.

In the serial I/O_2 mode the receive ready signal ($\overline{S_{RDY2}}$), synchronous input /output clock (CLK_2), and the serial I/O_2 pins (S_{OUT2}, S_{IN2}) are used as $P4_3$, $P4_2$, $P4_1$, and $P4_0$, respectively.

The serial I/O_2 mode register (address $00F5_{16}$) is an 8-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P4_2$ is selected. When these bits are [10], the overflow signal from timer 1, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the timing ϕ divided by 4, becomes the clock.

Bit 2 and 3 decide whether parts of P4 will be used as a serial I/O_2 or not. When bit 2 is a "1", $P4_2$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P4_2$. If an external synchronous clock is selected, the clock is input to $P4_2$ and $P4_1$ will be a serial output and $P4_0$ will be a serial input. To use $P4_0$ as a serial input, set the directional register bit which corresponds to $P4_0$ to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O_2, bit 2 needs to be set to "1", if it is "0" $P4_2$ will function as a normal I/O. Bit 3 determines if $P4_3$

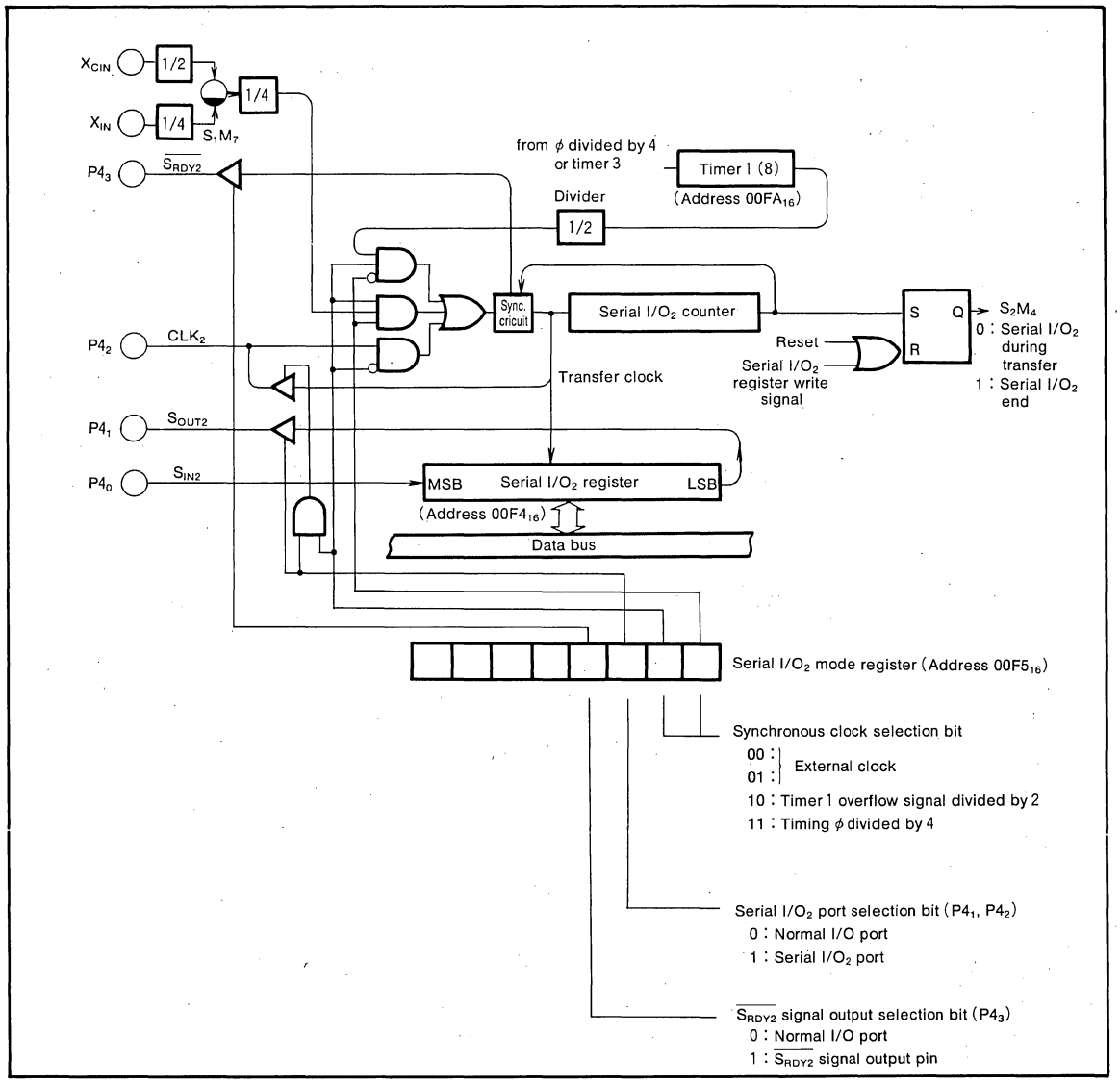


Fig.9 Block diagram of serial I/O_2

is used as an output pin for the receive data ready signal (bit 3=1, $\overline{S_{RDY2}}$) or used as normal I/O pin (bit 3=0). The serial I/O_2 function is discussed below. The function of the serial I/O_2 differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY2}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O_2 register (address $00F4_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY2}}$ signal becomes low signaling that the M50950-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY2}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O_2 counter is set to 7 when data is stored in the serial I/O_2 register. At each falling edge of the transfer clock, serial data is output to $P4_1$. During the rising edge of this clock, data can be input from $P4_0$ and the data in the serial I/O_2 register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O_2 register will be empty and the transfer clock will remain at a high level. At this time the serial I/O_2 end bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 9. An example of communication between two M50950-XXXSPs is shown in Figure 10.

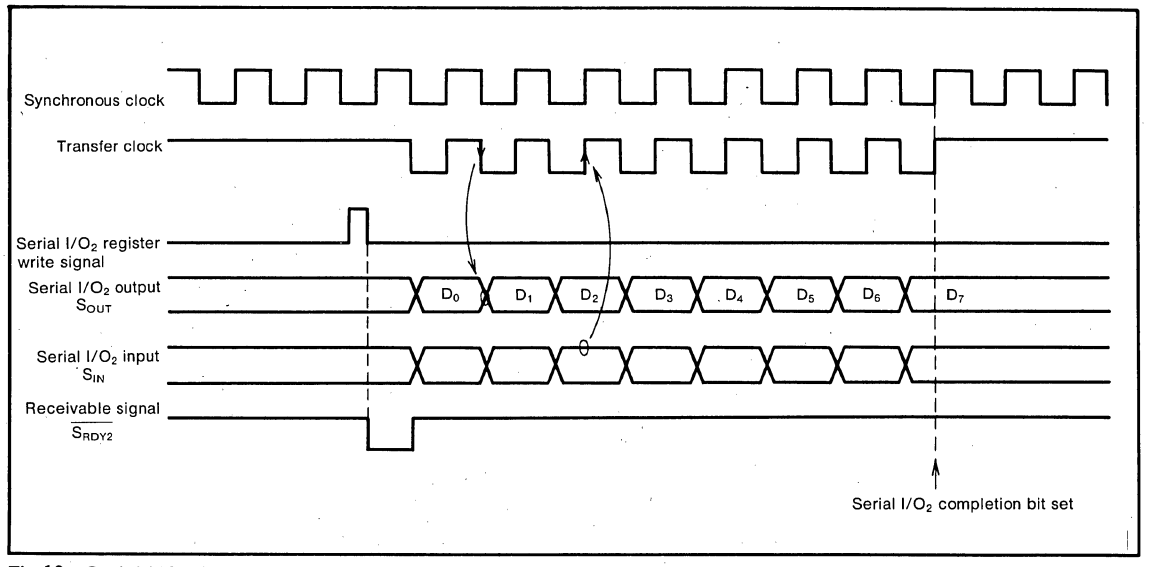


Fig.10 Serial I/O_2 timing

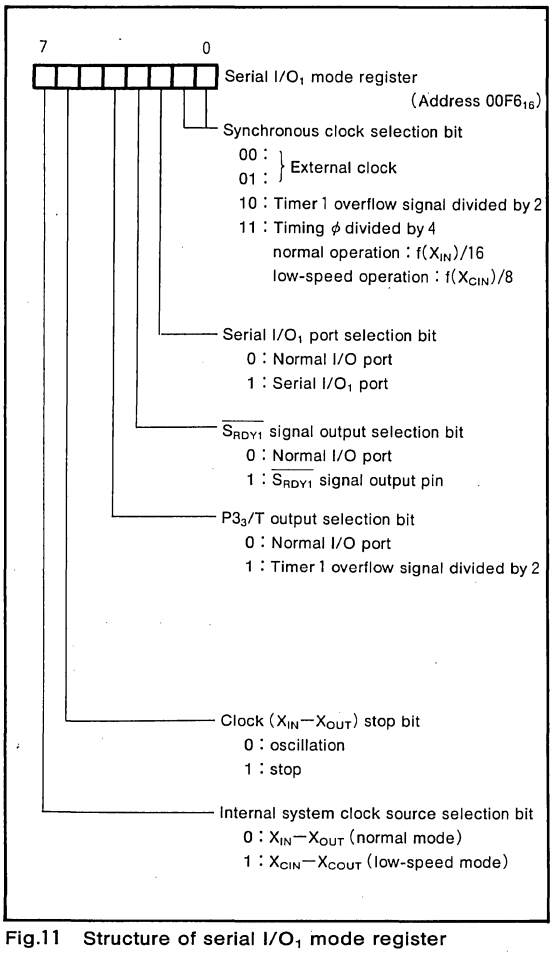


Fig.11 Structure of serial I/O1 mode register

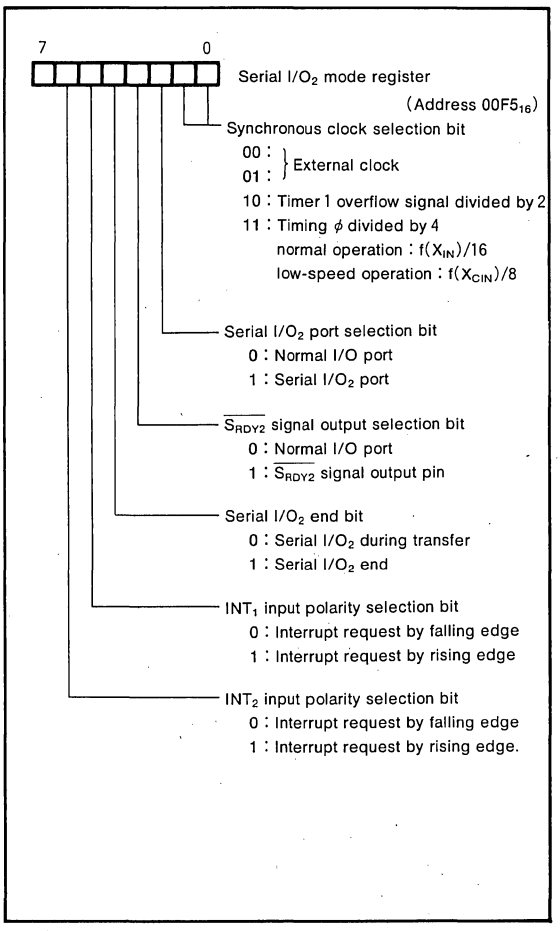


Fig.12 Structure of serial I/O2 mode register

RESET CIRCUIT

The M50950-XXXSP is reset according to the sequence shown in Figure 15. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 13.

An example of the reset circuit is shown in Figure 14.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

		Address	
(1)	Port P0 register	(P0) ($E0_{16}$) ···	00_{16}
(2)	Port P1 register	(P1) ($E2_{16}$) ···	00_{16}
(3)	Port P2 register	(P2) ($E4_{16}$) ···	0 0 0 0 0 0
(4)	Port P2 directional register	(D2) ($E5_{16}$) ···	0 0
(5)	Port P3 directional register	(D3) ($E9_{16}$) ···	00_{16}
(6)	Port P4 directional register	(D4) (EB_{16}) ···	0_{16}
(7)	Serial I/O_1 mode register	(S_1M) ($F6_{16}$) ···	00_{16}
(8)	Serial I/O_2 mode register	(S_2M) ($F5_{16}$) ···	0 0 0 0 0 0 0
(9)	Timer 2	(T2) (FC_{16}) ···	FF_{16}
(10)	Timer 3	(T3) (FD_{16}) ···	07_{16}
(11)	Interrupt control register	(IM) (FE_{16}) ···	00_{16}
(12)	Timer control register	(TM) (FF_{16}) ···	00_{16}
(13)	Processor status register (only the interrupt disable flag is set)	(PS) ···	1
(14)	Program counter	(PC_H) ···	Contents of Address $FFFF_{16}$
		(PC_L) ···	Contents of Address $FFFF_{16}$

Since the contents of both registers other than those listed above (including timer 1, serial I/O registers) and the RAM are undefined at reset, it is necessary to set initial value.

Fig.13 Internal state of microcomputer at reset

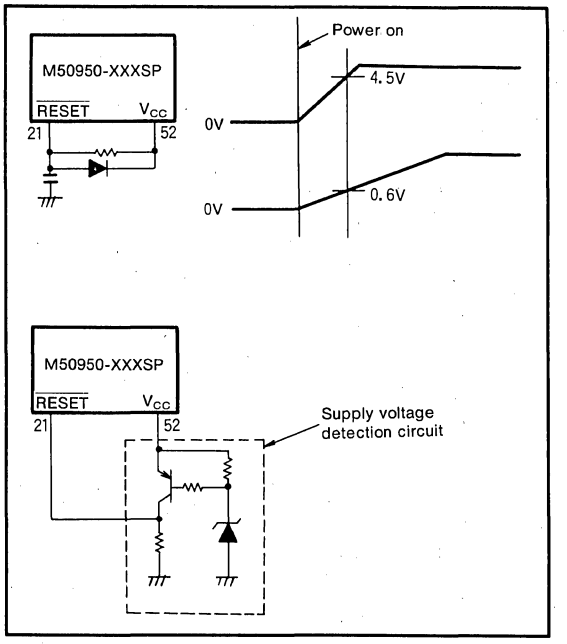


Fig.14 Example of reset circuit

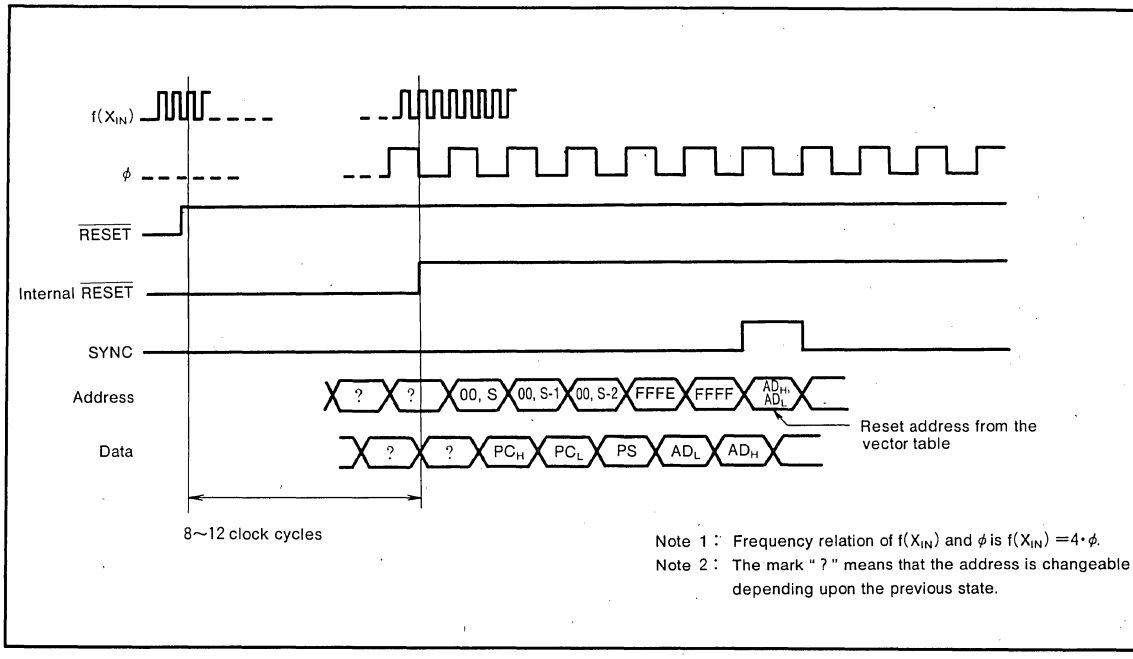


Fig.15 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit output port. The output type is high-voltage P-channel open drain output, and the break-down voltage is V_{CC} − 36V. Pull down resistors are built into each pin. The power source for each pin is V_P. Port P0 is treated as memory on page zero (address $00E0_{16}$), as shown in the memory map in Figure 1.

Depending on the contents of the processor mode bit (bits 0 and 1 at address $00FF_{16}$), four modes can be selected. These modes are: the single-chip mode, memory expanding mode, microprocessor mode, and eva-chip mode. Other than in the single-chip mode, the pins of this port can be used as the address output pins, in addition to their normal input/output function. For details, see the section on the processor mode.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0. Modes, the functions of port slightly differ from those of P0. For details, see the section on the processor mode.

(3) Port P2

Port P2 consists of 2-bit input/output ports $P2_0$ and $P2_1$ and 6-bit output ports $P2_2$ through $P2_7$. The output type for $P2_0$ and $P2_1$ is an N-channel open drain output. The output type for $P2_2$ through $P2_7$ is a high-voltage P-channel open drain output. The break down voltage is V_{CC} − 36V. Pull down resistors are built into each pin. The power source for these resistors is V_P.

Port P2 is treated as memory at address $00E4_{16}$, as shown in Figure 1.

Because port $P2_0$ and $P2_1$ have a direction register D2 (address $00E5_{16}$ on the zero page), each bit can be individually programmed for use as an input or output. A pin programmed to "1" is used for output and that programmed to "0" for input.

Data that is written on the programmed output pin is stored in the port latch and is transferred to the output pin. When data is read from the programmed output pin, data is read not from output pin but from output latch. Therefore, previously output data can be read correctly regardless of the logical level of the pin due to output loading.

Because the programmed input pin is floating, the value of the pin can be read correctly. When data is written to the programmed input pin, it is written only to the port latch and the pin remains floating.

For details, see the section on the processor mode.

(4) Port P3

Port P3 is an 8-bit input /output port. The output type is an N-channel open drain output. Port P3 is treated as memory on the zero page (address $00E8_{16}$).

Because port P3 has the direction register D3 (address $00E9_{16}$ on the zero page), each bit can be individually programmed to be used for input or output. The pin programmed to "1" is used for output and that programmed to "0" for input.

Data that is written to a programmed output pin is stored in the port latch and is transferred to the output pin. When data is read from a programmed output pin, data is read not from output pin but from the output latch. Therefore, previously output data can be read correctly regardless of logical level of the pin due to output loading (e.g., when driving an LED).

Because the programmed input pin is floating, the value of the pin can be read correctly. When data is written to the programmed input pin, it is written only to port latch and the pin remains floating.

The pins can also serve as serial I/O_1 pins.

For functions other than the single-chip mode, see the section on the processor mode.

(5) Port P4

Port P4 is a 4-bit input/output port. The output type is N-channel open drain output. Port P4 is treated as memory on the zero page (address $00EA_{16}$).

Because port P4 has the direction register D4 (address $00EA_{16}$ on the zero page), each bit can be individually programmed to be used for input or output. A pin which is set to "1" is used for output and that which is set to "0", for input.

As well as port P3, the pins can also serve as serial I/O_2 pins. This function is not affected by the processor mode.

(6) Port P5

Bits 2 and 3 are the dedicated input port that also serves as the interrupt pin, with hysteresis. Data can be fetched while this port is used for interrupt input.

The interrupt request bit (INT_1 : bit 7 of address $00FE_{16}$, INT_2 : bit 1 of address $00FE_{16}$) is set to "1" when the input level of ports $P5_3$ and $P5_2$ changes. The contents of bits 5 and 6 of the serial I/O_2 mode register S_2M (address $00F5_{16}$) define whether an "L" edge interrupt or an "H" edge interrupt is to be used as the interrupt factor.

For the M50950-XXXSP or M50951-XXXSP, interrupt inputs are also used as the normal input port.

When the chip is to be used in an environment where extraneous noise may cause an unwanted interrupt, the influence of noise can be eliminated by the program.

Note that the interrupt request enable bit (bit 6 or 0 of address $00FE_{16}$) must be set to "0" (the interrupt disable status) when the contents of bits 5 (S_2M_5) and 6 (S_2M_6) are to be modified.

If not, an undesirable interrupt may occur.

Bits 4 through 7 on port P5 are 4-bit input pins.

Figure 16 is a block diagram for ports P0 through P5.

(7) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ. When in the slow speed mode, the oscillator frequency for timer devided by two is output as ϕ.

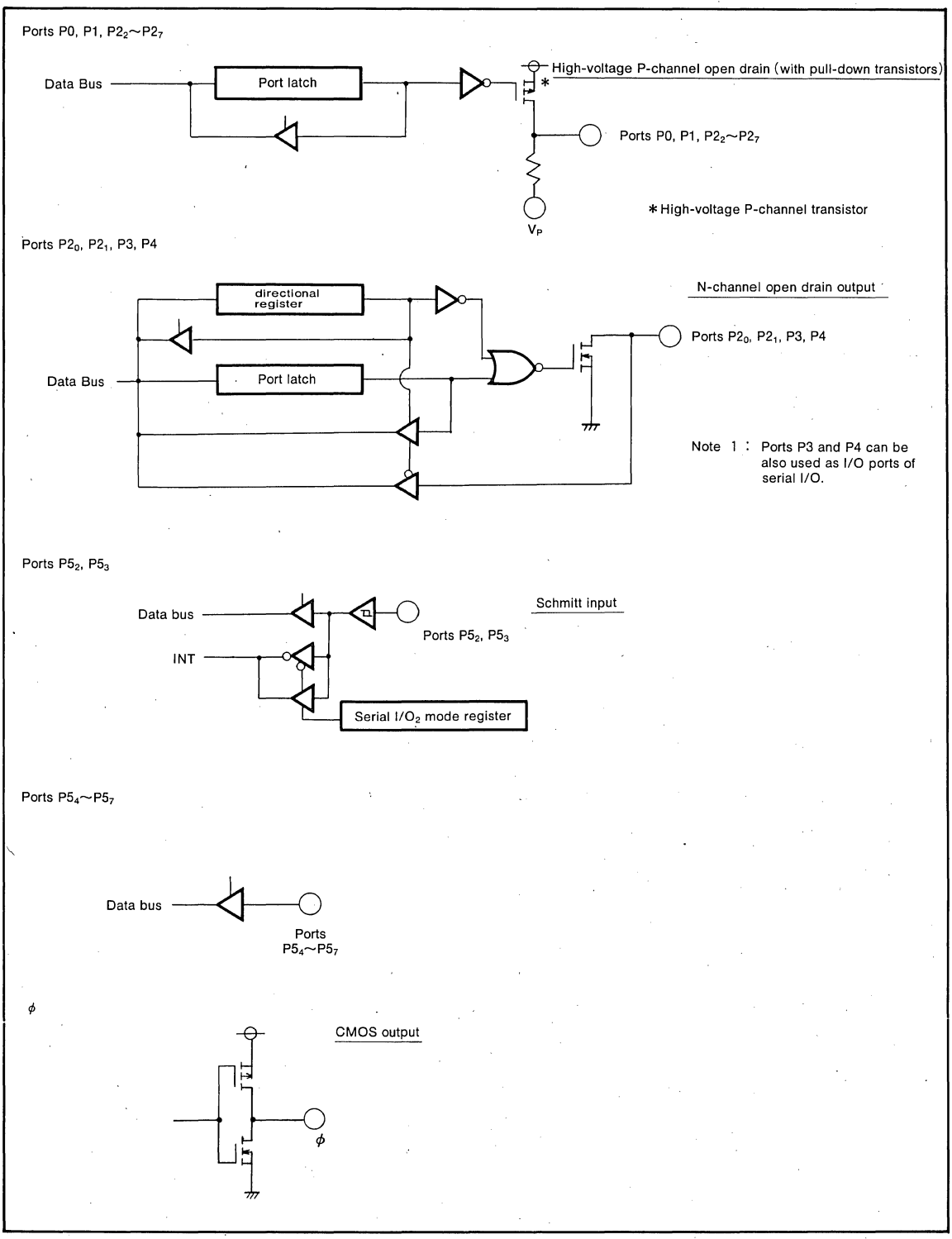


Fig.16 Block diagram of ports P0~P5 (in single-chip mode) and output format of ϕ.

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 18 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 17.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

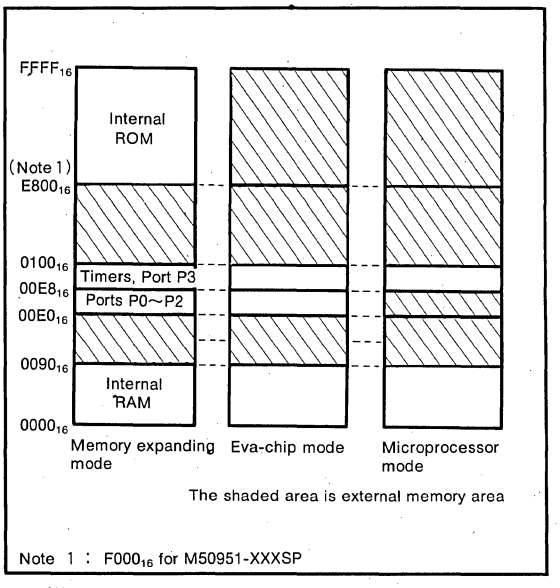


Fig.17 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

The lower 8 bits of address data for port P0 is output when ϕ goes "H" state. When ϕ goes the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when ϕ goes "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode.

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the data bus (D_7～D_0) and loses its normal I/O functions. Port $P3_1$ and $P3_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

With the exceptions that the internal ROM is disabled and that external memory must be attached in this mode, this mode is the same as the memory expansion mode.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

Mode / Port	Single-chip mode (TM_1=0, TM_0=0)	Memory expanding mode (TM_1=0, TM_0=1)	Eva-chip mode (TM_1=1, TM_0=1)	Microprocessor mode (TM_1=1, TM_0=0)
Port P0	Internal ϕ Ports $P0_7$~$P0_0$ Output port	ϕ Ports $P0_7$~$P0_0$ Address A_7~A_0 / Output port	Same as left	ϕ Ports $P0_7$~$P0_0$ Address A_7~A_0
Port P1	Internal ϕ Ports $P1_7$~$P1_0$ Output port	ϕ Ports $P1_7$~$P1_0$ Address A_{15}~A_8 / Output port	Same as left	ϕ Ports $P1_7$~$P1_0$ Address A_{15}~A_8
Port P2	Internal ϕ Ports $P2_7$~$P2_0$ I/O port	ϕ Ports $P2_7$~$P2_0$ Output port / Data D_7~D_0	Same as left	ϕ Ports $P2_7$~$P2_0$ Data D_7~D_0
Port P3	Internal ϕ Ports $P3_7$~$P3_0$ I/O port	ϕ Ports $P3_7$~$P3_2$ I/O port Port $P3_1$: SYNC / I/O port Port $P3_0$: R/$\overline{W}$ / I/O port	Same as left	ϕ Ports $P3_7$~$P3_2$ I/O port Port $P3_1$: SYNC Port $P3_0$: R/$\overline{W}$

Fig.18 Processor mode and functions of ports P0~P3

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The M50950-XXXSP has two internal clock generating circuit. Figure 21 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ. Bit 7 of serial I/O_1 mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 19 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacture's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the $X_{IN}(X_{CIN})$ pin and leave the $X_{OUT}(X_{COUT})$ pin open. A circuit example is shown in Figure 20.

The M50950-XXXSP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 2 and timer 3 are forcibly connected and $\phi/4$ is selected as timer 2 input. Also timer 2 and timer 3 are loaded with FF_{16} and 07_{16} respectively to enable the oscillator to stabilize when restarting oscillation. Before executing the STP instruction, the timer 2 count stop bit must be set to supply ("0"), timer 2 interrupt enable bit and timer 3 interrupt enable bit must be set to disable ("0"), and timer 3 interrupt request bit must be set to no request ("0").

Oscillation is resarted (release the stop mode) when INT_1, INT_2, or serial I/O_1 interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 3 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the $\overline{RESET}$ pin until the oscillattion stabilizes because no wait time is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock ($200\mu A$(max.) at $f(X_{CIN}) = 32kHz$). X_{IN} clock oscillation is stopped when the bit 6 of serial I/O_1 mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 22 shows the transition of states for the system clock.

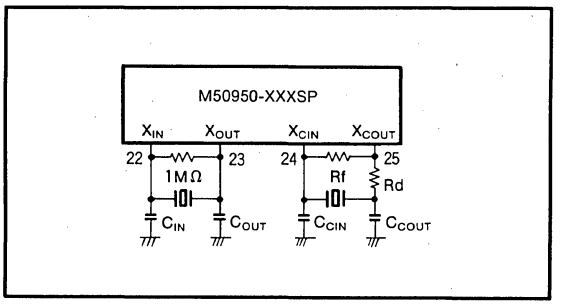


Fig.19 Externally ceramic resonator circuit

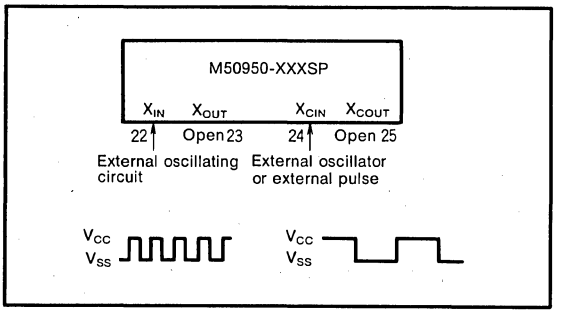


Fig.20 External clock input circuit

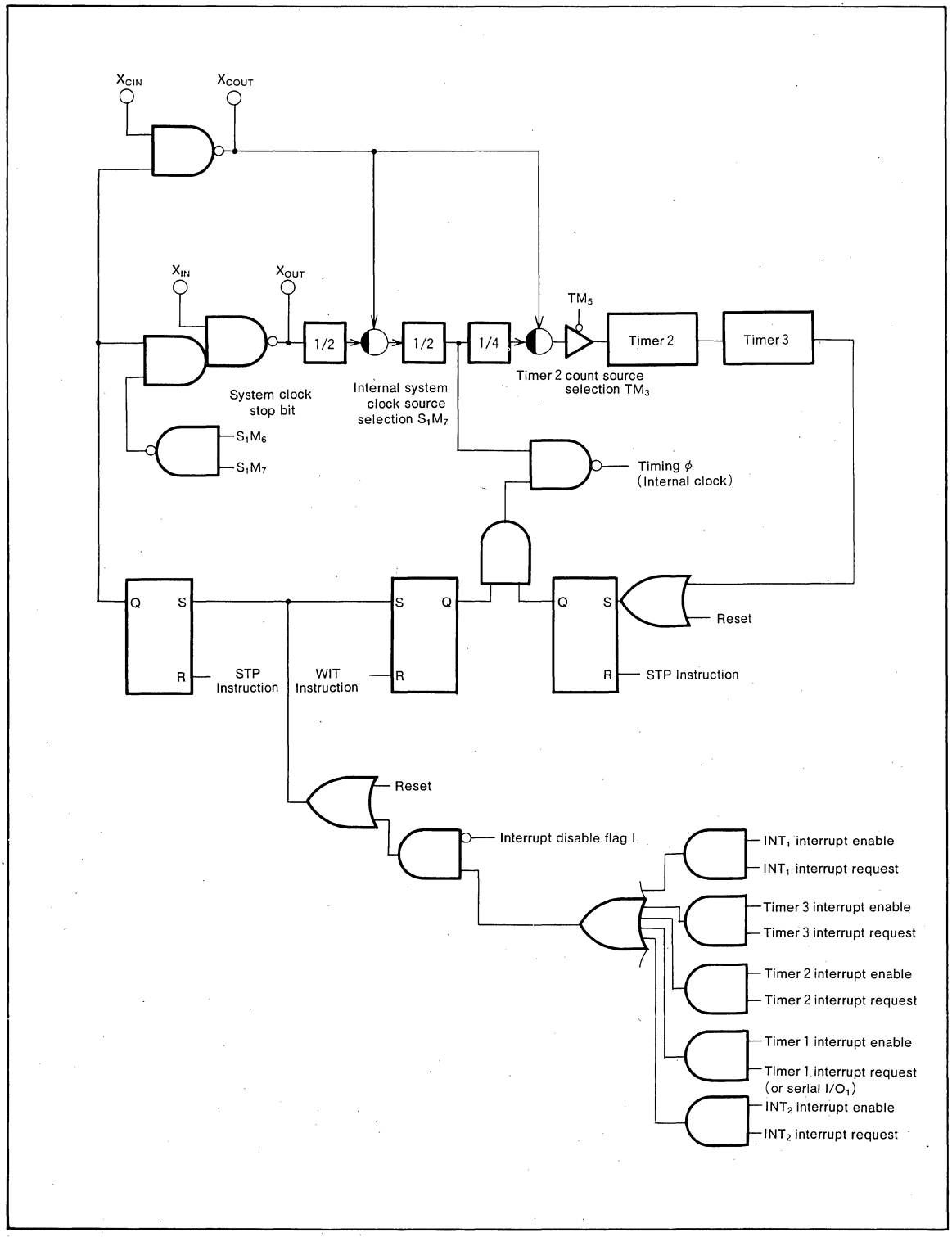
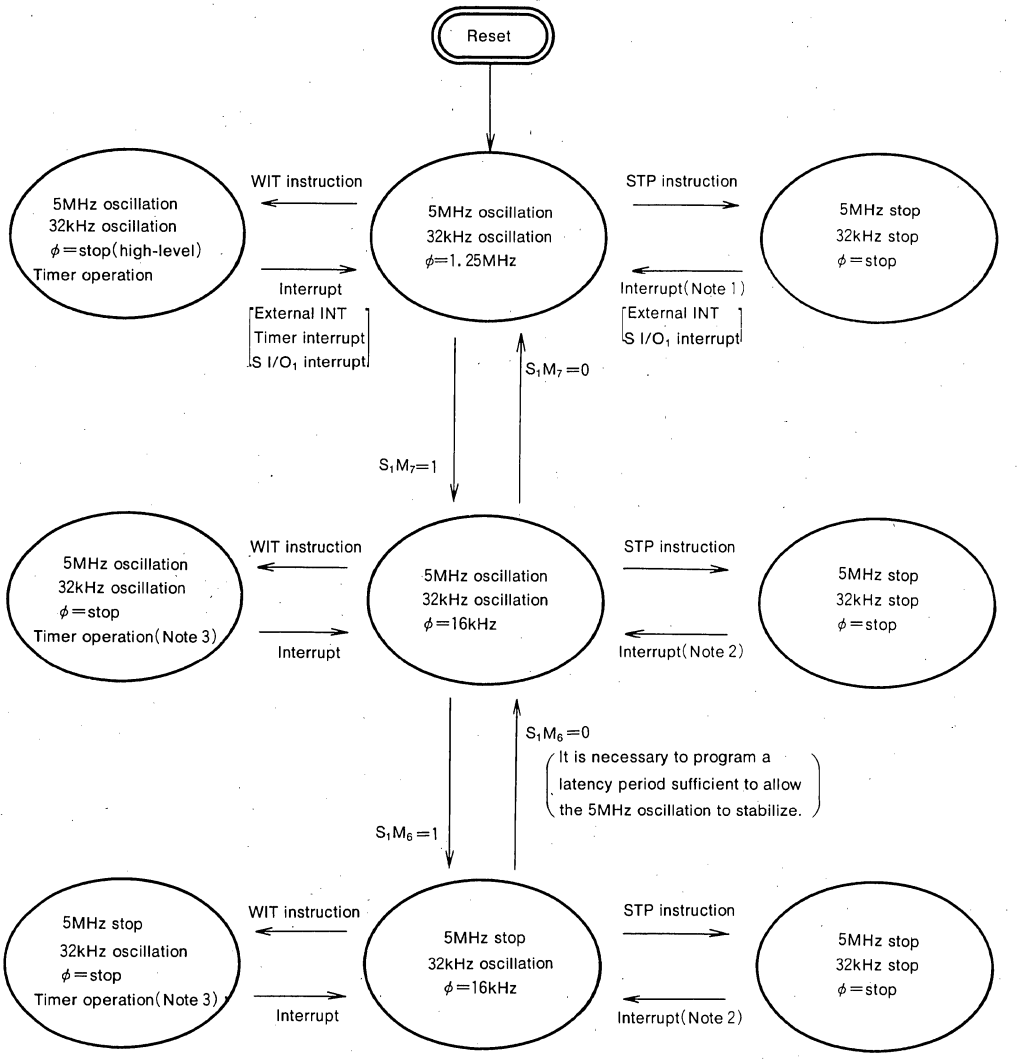


Fig.21 Block diagram of clock generating circuit

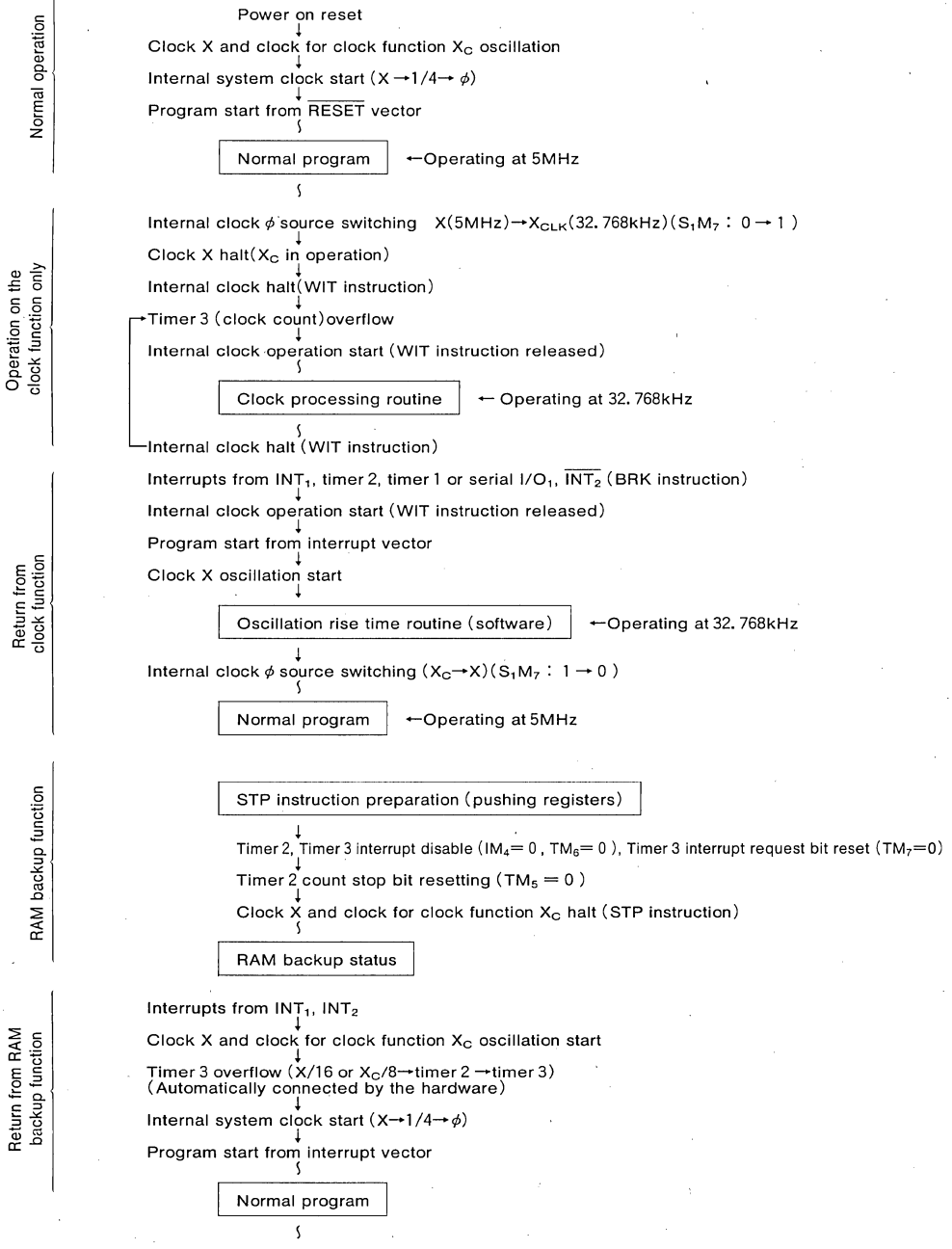


The above example assumes that signals of 5MHz and 32KHz are being applied to pins X_{IN} and X_{CIN}, respectively. ϕ signifies the internal clock.

(Note 1) Approximately 6.5ms of latency time are automatically generated upon release from the STP instruction due to the connections of timer 2 and 3.
(Note 2) Approximately 500ms of latency time exists after the release of the STP instruction.
(Note 3) When the internal clock 1/4 frequency is connected as a timer count source the count source becomes 4KHz.

Fig.22 Transition of states for the system clock

≪An example of flow for system≫



PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) Reading the timer must be avoided while the input to the timer is changing except using timing ϕ or it divided by timer as count source.
(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(5) A NOP instruction must be used after the execution of a PLP instruction.
(6) Notes on serial I/O
① Set "0" in the serial I/O_1 interrupt enable bit (bit 2 of address $00FE_{16}$) before setting the serial I/O_1 mode.
② Insert at least one instruction and set "0" in the serial I/O_1 interrupt request bit (bit 3 of address $00FE_{16}$) after setting the serial I/O_1 mode.
③ Set "1" in the serial I/O_1 interrupt enable bit after the operation described in ②.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ..... EPROM 3sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	−0.3∼7	V
V_P	Pull-down supply voltage		V_{CC}−38∼V_{CC}+0.3	V
V_I	Input voltage $P2_0$, $P2_1$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, CNV_{SS}, $P5_2/INT_2$, $P5_3/INT_1$		−0.3∼13	V
V_I	Input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		−0.3∼7	V
V_I	Input voltage $P5_4$∼$P5_7$		−0.3∼7	V
V_O	Output voltage $P2_0$, $P2_1$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$		−0.3∼13	V
V_O	Output voltage X_{OUT}, X_{COUT}, ϕ		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_2$∼$P2_7$		V_{CC}−38∼V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Nom.	Max.	
V_{CC}	Supply voltage	$f_{(X_{IN})}$=5MHz	4.5	5	5.5	V
		$f_{(X_{IN})}$=less than 1MHz	3		5.5	V
V_P	Pull-down supply voltage		V_{CC}−36		V_{CC}	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P2_0$, $P2_1$, $P3_0$∼$P3_7$, CNV_{SS}, $P5_2/INT_2$, $P5_3/INT_1$, $P4_0$∼$P4_3$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P5_4$∼$P5_7$		0.4V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P2_0$, $P2_1$, $P3_0$∼$P3_7$, CNV_{SS}, $P5_2/INT_2$, $P5_3/INT_1$, $P4_0$∼$P4_3$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16V_{CC}	V
V_{IL}	"L" input voltage X_{CIN}		0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P5_4$∼$P5_7$		0		0.12V_{CC}	V
$I_{OH(peak)}$	"H" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_2$∼$P2_7$				−24	mA
$I_{OL(peak)}$	"L" peak output current $P2_0$, $P2_1$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$				20	mA
$I_{OH(avg)}$	"H" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_2$∼$P2_7$				−12	mA
$I_{OL(avg)}$	"L" average output current $P2_0$, $P2_1$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$				10	mA
$f_{(X_{IN})}$	Clock input oscillating frequency				5	MHz
$f_{(X_{CIN})}$	Clock oscillating frequency for clock function			32	500	kHz

Note 1 : "H" input voltage of up to +12V may be applied to permissible for ports $P2_0$, $P2_1$, $P3_0$∼$P3_7$, $P5_2$, $P5_3$, $P4_0$∼$P4_3$ and CNV_{SS}.

2 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value of a period of 100ms. On output ports, the total of current dissipation should be 890mW max at T=25℃.

3 : Oscillation frequency is at 50% duty cycle.
When used low-speed mode, clock input generating frequency for clock function should be f (X_{CIN})<f(X_{IN})/3.
When used external clock, clock input generating frequency for clock function should be f(X_{CIN}) <50kHz.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=5MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA, T_a=−10~70℃	3			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_2$~$P2_7$	I_{OH}=−12mA, T_a=−10~70℃	3			V
V_{OL}	"L" output voltage $P2_0$, $P2_1$, $P3_0$~$P3_7$, $P4_0$~$P4_3$	I_{OL}=10mA, T_a=−10~70℃			2	V
V_{OL}	"L" output voltage ϕ	I_{OL}=2.5mA, T_a=−10~70℃			2	V
$V_{T+}-V_{T-}$	Hysteresis $P5_2/INT_2$, $P5_3/INT_1$		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$, $P4_2$	When used as CLK input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P2_0$, $P2_1$, $P3_0$~$P3_7$, $P4_0$~$P4_3$	V_I= 0 V			−5	μA
I_{IL}	"L" input current $P5_4$~$P5_7$	V_I= 0 V			−5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}	V_I= 0 V			−5	μA
I_{IL}	"L" input current $P5_2/INT_2$, $P5_3/INT_1$	V_I= 0 V			−5	μA
I_{IH}	"H" input current $P2_0$, $P2_1$, $P3_0$~$P3_7$, $P4_0$~$P4_3$	V_I= 5 V			5	μA
		V_I=12V			12	μA
I_{IH}	"H" input current $P5_4$~$P5_7$	V_I= 5 V			5	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}	V_I= 5 V			5	μA
I_{IH}	"H" input current $P5_2/INT_2$, $P5_3/INT_1$	V_I= 5 V			5	μA
		V_I=12V			12	μA
I_L	Pull-down current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_2$~$P2_7$	V_P=V_{CC}−36V, V_{OL}=V_{CC}	150	450	900	μA
I_{OL}	"L" Pull-down current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_2$~$P2_7$	V_P=V_{CC}−36V, V_{OL}=V_P			−30	μA
V_{RAM}	RAM retention voltage	at clock stop	2		5.5	V
I_{CC}	Supply current	Output pins open (output off) V_{PP}=V_{SS}, Input and I/O pins all at V_{SS} $f_{(X_{IN})}$=5MHz(at system operation)		4	8	mA
		ditto (at wait mode)		1		mA
		X_{IN}-X_{OUT} stop $f_{(X_{CIN})}$=32kHz(at system operation) all other conditions same as above		60	200	μA
		ditto (at wait mode)		40		μA
		Oscillation all stopped (at stop mode) T_a=25℃			1	μA
		Oscillation all stopped (at stop mode) T_a=70℃			10	μA

TIMING REQUIREMENTS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=5MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(P5D-\phi)}$	Port $P5_2$/INT_2, $P5_3$/INT_1 input setup time	270			ns
$t_{su(P5D-\phi)}$	Port $P5_4$~$P5_7$ input setup time	500			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port $P5_2$/INT_2, $P5_3$/INT_1 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port $P5_4$~$P5_7$ input hold time	50			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{C(X_{IN})}$	External clock input cycle time (X_{IN} input)	200			ns
$t_{W(X_{IN})}$	External clock input pulse width (X_{IN} input)	75			ns
$t_{C(X_{CIN})}$	External clock input cycle time (X_{CIN})	2			μs
$t_{W(X_{CIN})}$	External clock input pulse width (X_{CIN})	1			μs
t_r	External clock rising edge time			25	ns
t_f	External clock falling edge time			25	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=5MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=5MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25°C, $f_{(X_{IN})}$=5MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.24			250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.23, 24			250	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig.23			250	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				250	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25°C, $f_{(X_{IN})}$=5MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.24			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				250	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				250	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.23, 24			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig.23			250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				250	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				250	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				250	ns

Microprocessor mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25°C, $f_{(X_{IN})}$=5MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.24			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.23, 24			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig.23			250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

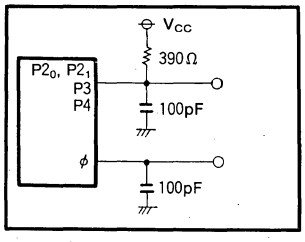


Fig.23 Ports $P2_0$, $P2_1$, P3 and P4 test circuit

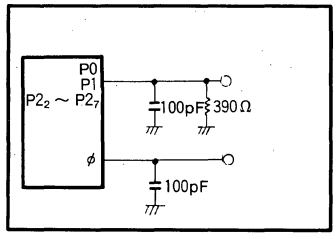
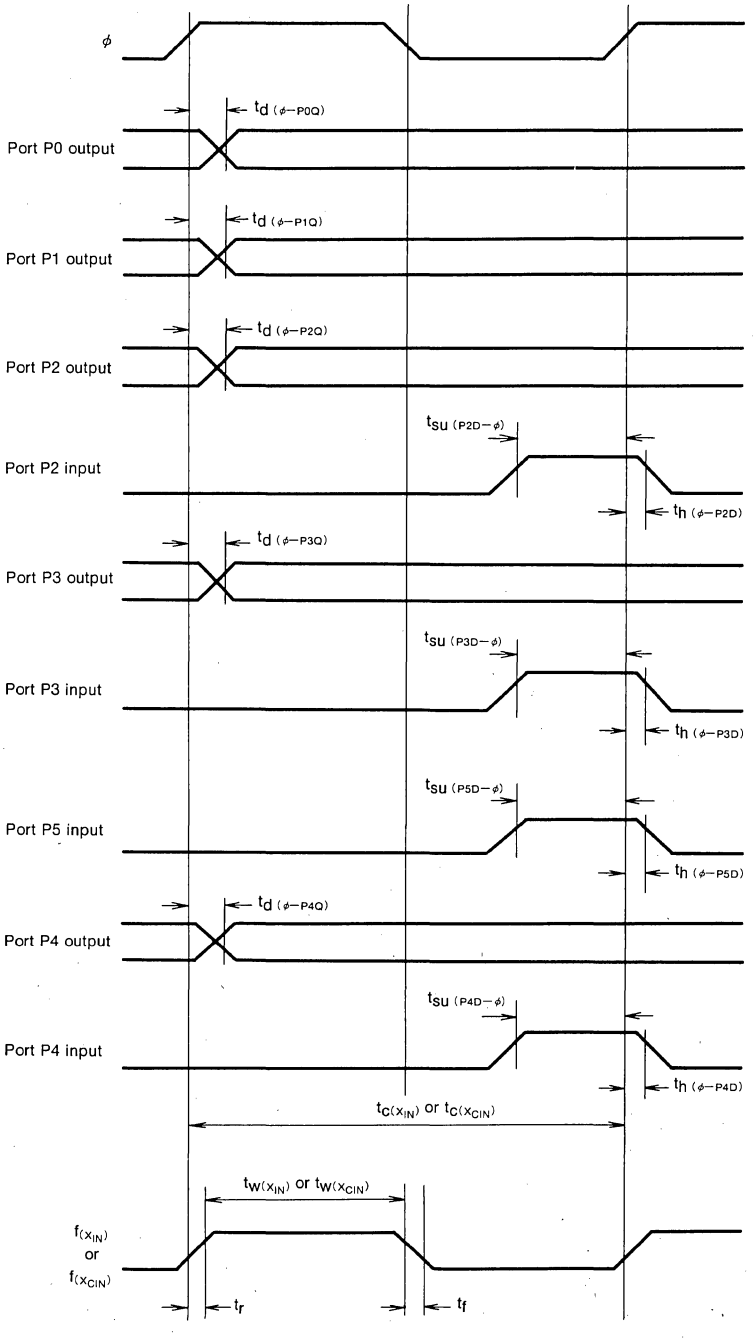


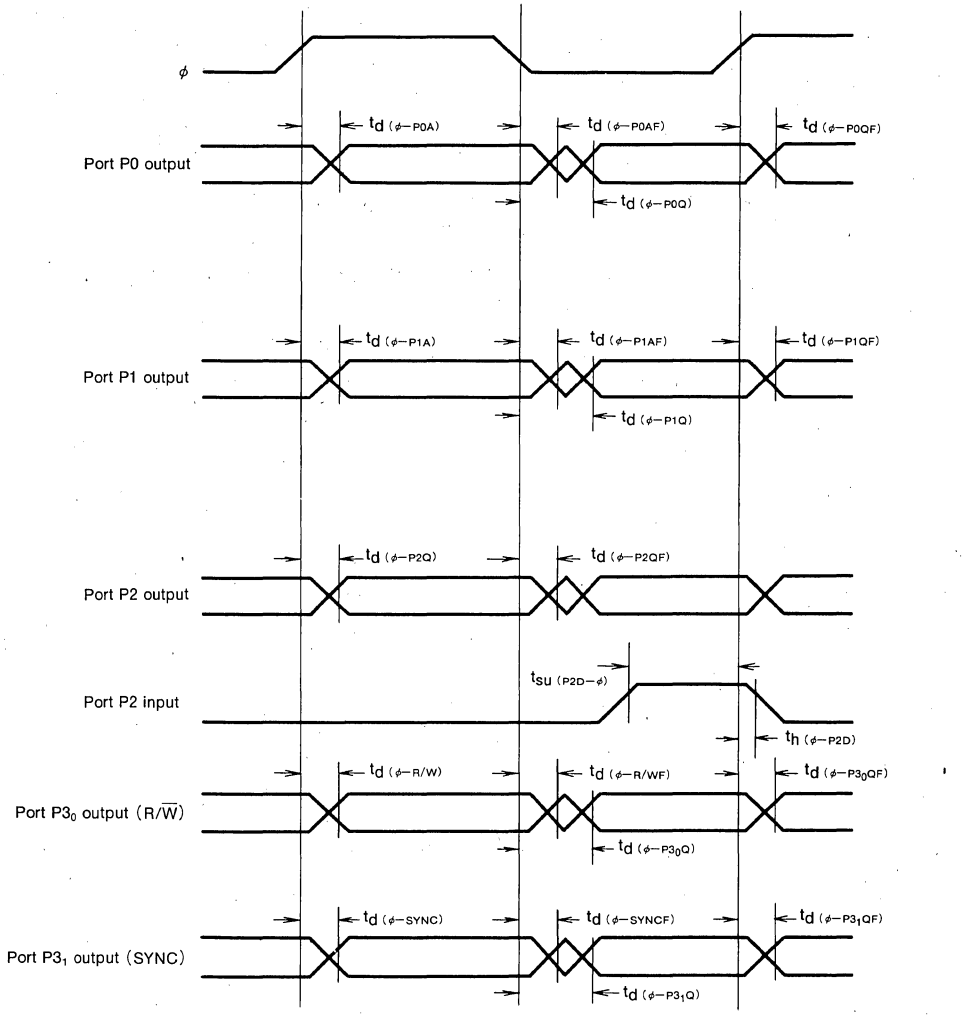
Fig.24 Ports P0, P1 and $P2_2$~$P2_7$ test circuit

TIMING DIAGRAMS

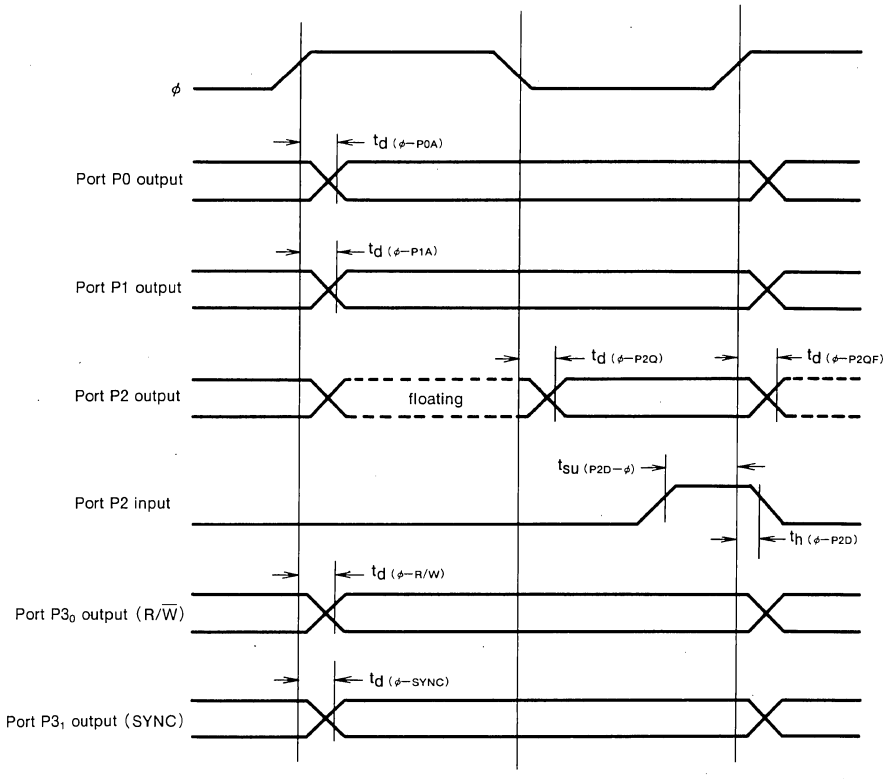
In single-chip mode



In memory expanding mode and eva-chip mode



In memory expanding mode and microprocessor mode



M50957-XXXSP/FP
M50959-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50957-XXXSP and the M50959-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 64-pin shrink plastic molded DIP (flat package type also available). These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50957-XXXSP and the M50959-XXXSP are noted below. The following explanations apply to the M50957-XXXSP. Specification variations for other chips are noted accordingly.

Type name	ROM size
M50957-XXXSP	10240bytes
M50959-XXXSP	16384bytes

The differences between the M50957-XXXSP and the M50957-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

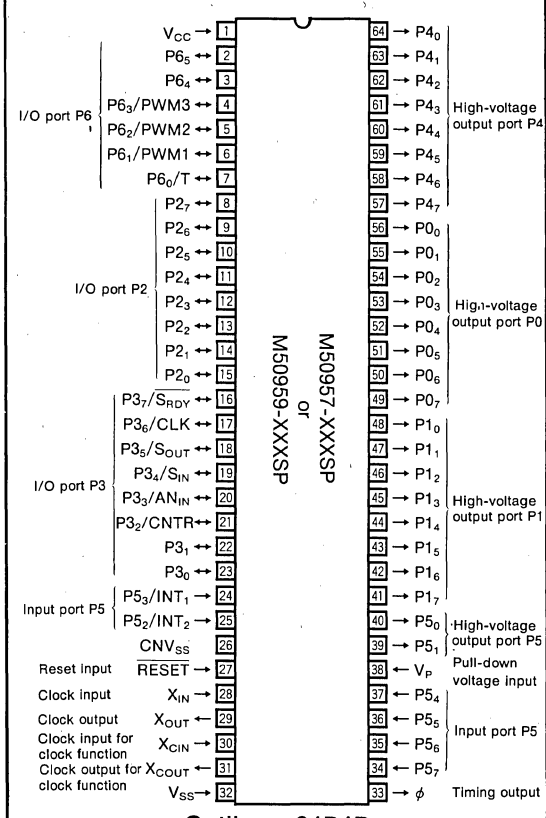
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 10240 bytes (M50957-XXXSP)
  16384 bytes (M50959-XXXSP)
  RAM ..... 256 bytes
- Instruction execution time
  ..... 1.9μs (minimum instructions, at 4.2MHz frequency)
- Single power supply 4.0~5.5V (at f(X_{IN})=4.2MHz)
  3.0~5.5V (below f(X_{IN})=1.0MHz)
- Power dissipation
  normal operation mode, at 4.2MHz frequency ··· 20mW
  low speed operation mode,
  at 32kHz frequency for clock function 0.3mW
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as serial I/O)
- Programmable I/O (Ports P2, P3, P6) 22
- Input ports (Port $P5_2$~$P5_7$) 6
- High-voltage output ports
  (Port P0, P1, P4, $P5_0$, $P5_1$) 26
- Serial I/O (8-bit) 1
- PWM function ..... 14-bit×1
  6-bit×2
- Two clock generator circuits (One is for main clock, the other is for clock function)
- Comparator 1
- Generating function for clock input of EAROM

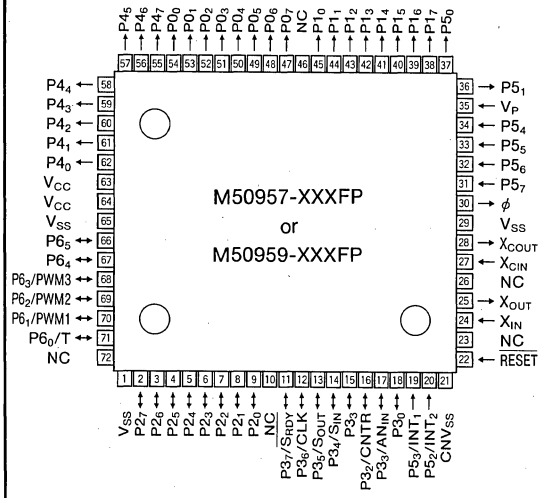
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

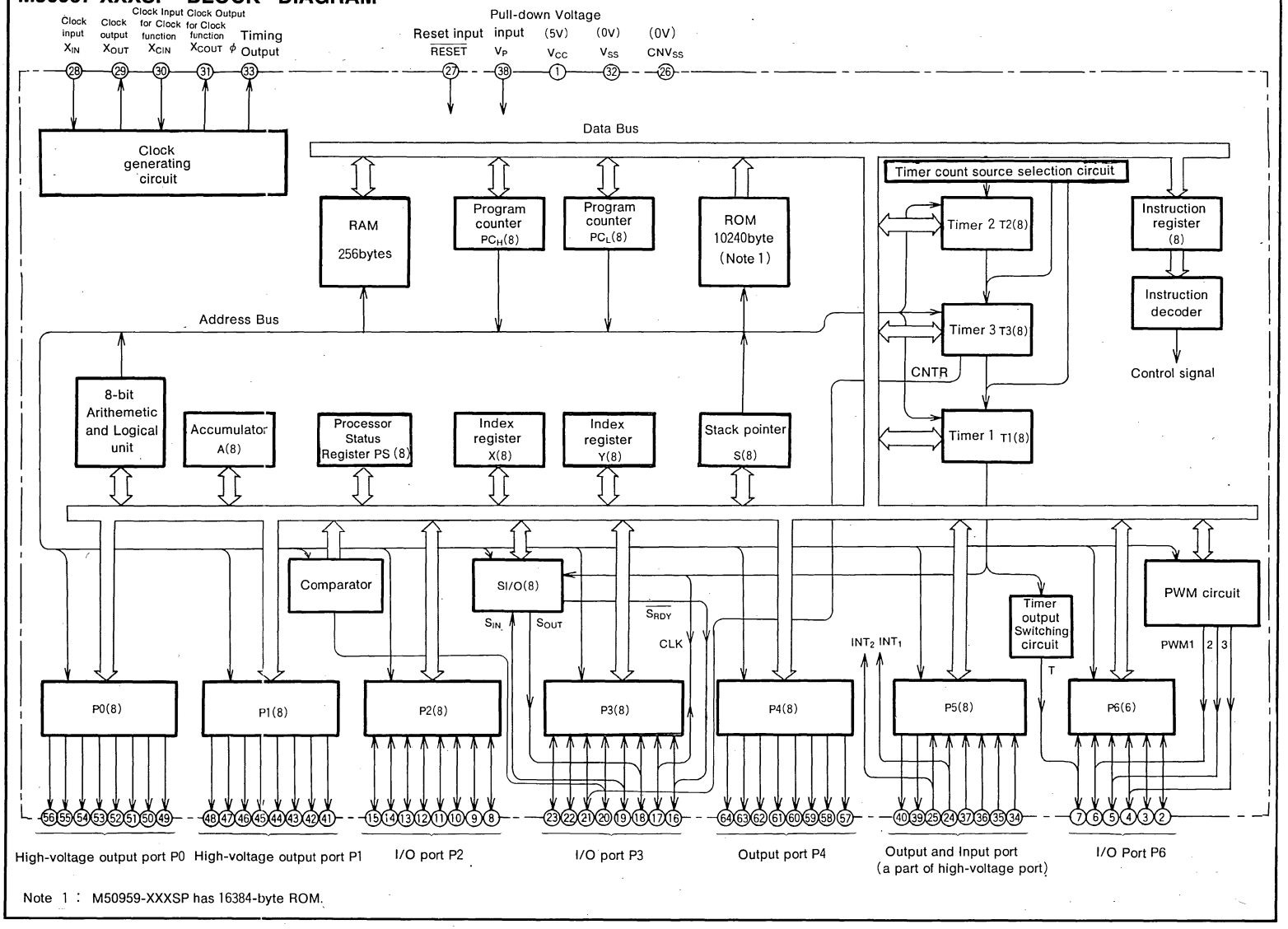


Outline 72P6

NC : No Connection

MITSUBISHI ELECTRIC

M50957-XXXSP BLOCK DIAGRAM



Note 1 : M50959-XXXSP has 16384-byte ROM.

FUNCTIONS OF M50957-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1.9μs (minimum instructions, at 4.2MHz frequency)
Clock frequency			4.2MHz
Memory size	ROM		10240bytes (16384bytes for M50959-XXXSP)
	RAM		256bytes
Input/output ports	P0, P1, P4	Output	8-bit×3 (high-voltage P-channel open drain; V_{CC}−38V)
	P2, P3	I/O	8-bit×2 (P3 can partially be used as among serial I/O, clock input for timer 3 and normal I/O.)
	$P5_0$, $P5_1$	Output	2-bit×1 (high-voltage P-channel open drain; V_{CC}−38V)
	$P5_2$, $P5_3$	Input	2-bit×1 (can be used as an input for either INT_2 or INT_1.)
	$P5_4$~$P5_7$	Input	4-bit×1
	P6	I/O	6-bit×1 (can be used as T_1 output or PWM output.)
Serial I/O			8-bit×1
Timers			8-bit timer×3 (×2, when used as serial I/O)
Subroutine nesting			96levels (max.)
Interrupt			Two external interrupts, three internal timer interrupts (or timer×2, serial I/O×1)
Clock generating circuit			Two built-in circuits (externally connected ceramic or quartz crystal oscillator)
Supply voltage	at f(X_{IN})=4.2MHz		4.0~5.5V
	below f(X_{IN})=1.0MHz		3.0~5.5V
Power dissipation	at high-speed operation		20mW (clock frequency X_{IN}=4.2MHz)
	at low-speed operation		0.3mW (clock frequency X_{CIN}=32kHz)
	at stop mode		5μW (when clock is stopped)
Input/Output characteristics	Input/Output voltage		12V (input/output P2, P3, $P5_2$, $P5_3$ except $P3_3$)
			V_{CC}−38V (P0, P1, P4, $P5_0$, $P5_1$)
			−0.3V~V_{CC}+0.3V (input/output P6)
	Output current		10mA (P2, P3 : N-channel open drain)
			−18mA (P0, P1 : high-voltage P-Channel open drain)
			−12mA (P4, $P5_0$, $P5_1$: high-voltage P-Channel open drain)
			0.5~−0.5mA (P6 : CMOS tri-states)
Memory expansion			Possibe
Operating temperature range			−10~70°C
Device structure			CMOS silicon gate process
Package	M50957-XXXSP, M50959-XXXSP		64-pin shrink plastic molded DIP
	M50957-XXXFP, M50959-XXXFP		72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 4.0~5.5V at $f(X_{IN})$=4.2MHz and 3.0~5.5V below $f(X_{IN})$=1.0MHz to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P0, P1, P4, $P5_0$ and $P5_1$.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open. This clock can be used as a program controlled the system clock.
X_{COUT}	Clock output for clock function	Output	
$P0_0$~$P0_7$	Output port P0	Output	Port P0 is an 8-bit output port. Output structure is high-voltage P-channel open drain. A pull-down transistor is built in between the V_P pin and this port. At reset, this port is set to a "L" level.
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P2. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. $P3_3$ works as an analog input for comparator, and $P3_2$ works as a clock input for timer 3.
$P4_0$~$P4_7$	Output port P4	Output	Port P4 is an 8-bit output port and has basically the same functions as port P2.
$P5_0$, $P5_1$	Output port P5	Output	Bit 0 and 1 of port P5 are 2-bit output port and has basically the same functions as port P0.
$P5_2/INT_2$ $P5_3/INT_1$	Input port P5	Input	Bit 2 and 3 of port P5 are 2-bit input port and are in common with interrupt inputs.
$P5_4$~$P5_7$		Input	Bit 4~7 of port P5 are 4-bit input port.
$P6_0$~$P6_7$	I/O port P6	I/O	Port P6 is a 6-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. The output structure is CMOS tri-state output. $P6_0$, $P6_1$, $P6_2$, $P6_3$ can be programmed to function as timer output pin (T), PWM output pins (PWM1, PWM2, and PWM3), respectively.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50957-XXXSP is shown in Figure 1. Addresses $D800_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 10240 bytes.

Addresses $C000_{16}$ to $FFFF_{16}$ are the ROM address area assigned to the M50959-XXXSP.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addreeses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $013F_{16}$ are assigned to the built-in RAM and consist of 256 bytes of static RAM. In addition to data storage, this RAM except the area in the page 1 is used for the stack during subroutine calls and interrupts.

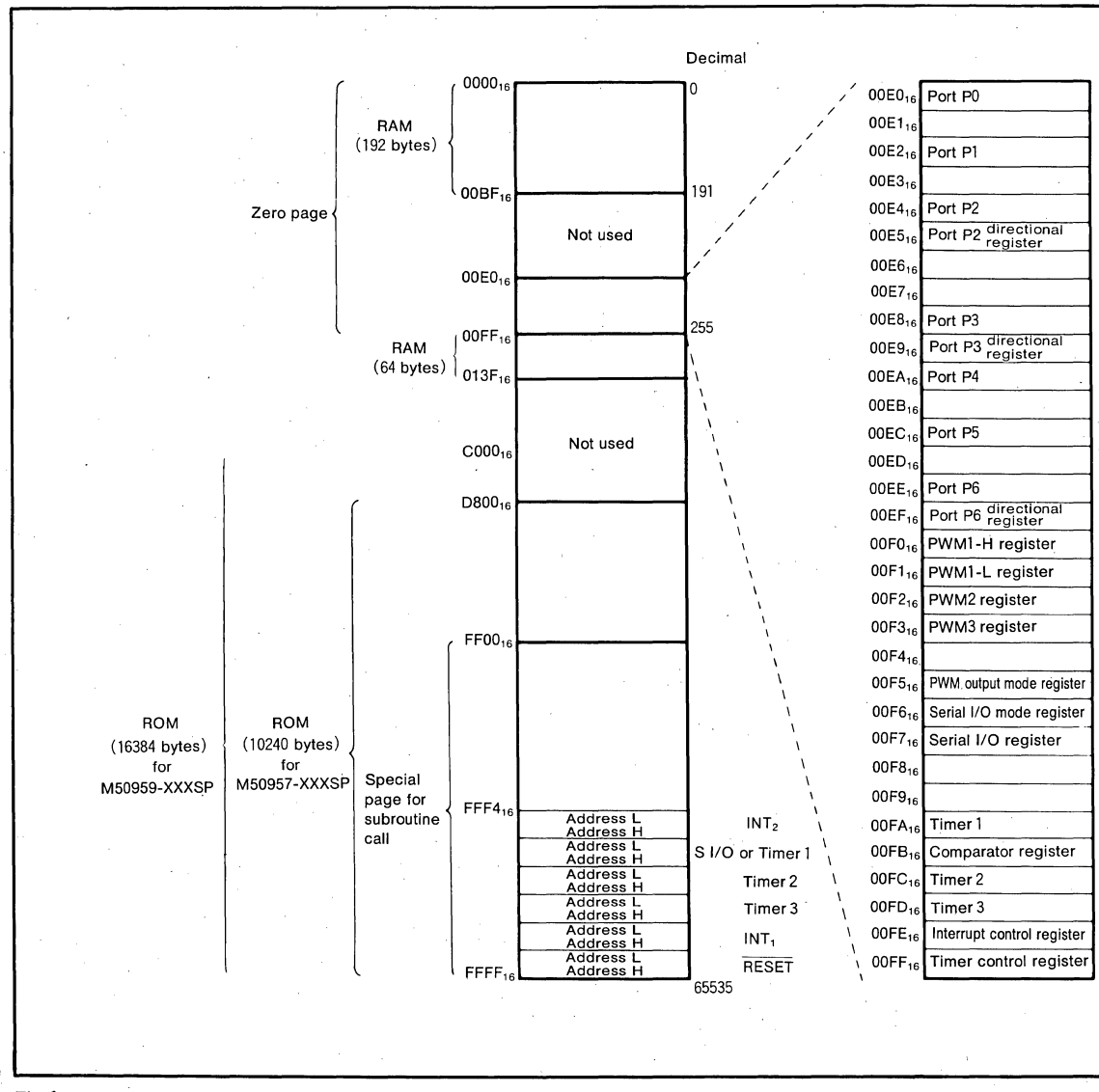


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

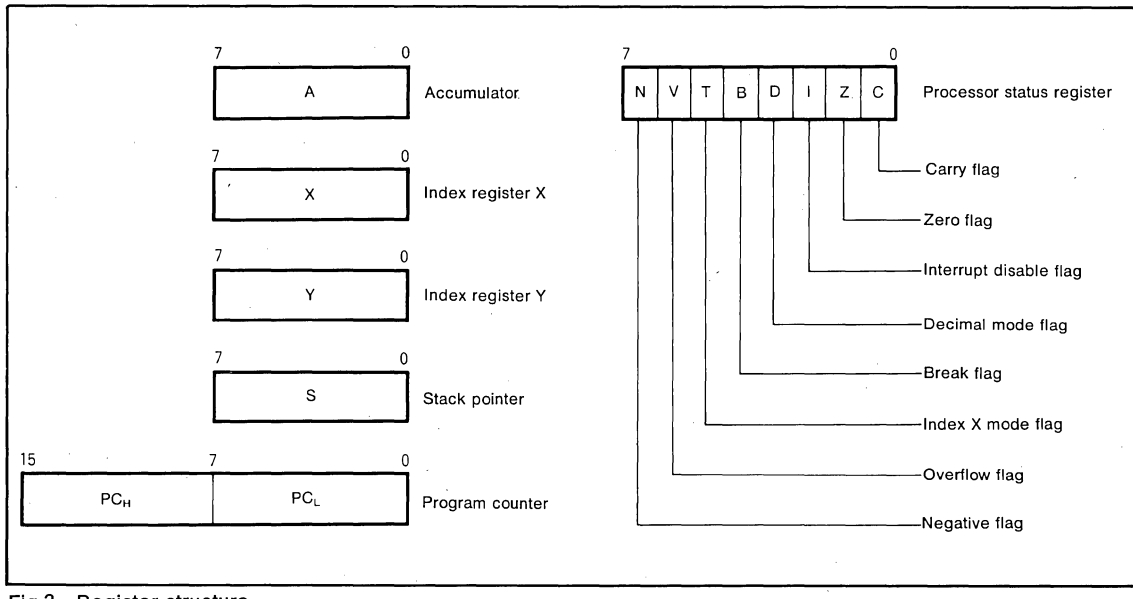


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When using this microcomputer in the single-chip mode, the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal arithmetic can be performed only with the ADC and SBC instructions. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a singed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directrly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
INT_1	2	$FFFD_{16}$, $FFFC_{16}$
Timer 3	3	$FFFB_{16}$, $FFFA_{16}$
Timer 2	4	$FFF9_{16}$, $FFF8_{16}$
Timer 1 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
INT_2(BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50957-XXXSP can be interrupted from seven souces; INT_1, timer 3, timer 2, timer 1/serial I/O, or INT_2/BRK instruction.

The value of bit 2 of the serial I/O mode register (address $00F6_{16}$) determine whether the interrupt is from timer 1 or from serial I/O. When bit 2 is "0" the interrupt is from timer 1, and when bit 2 is "1" the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag I is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

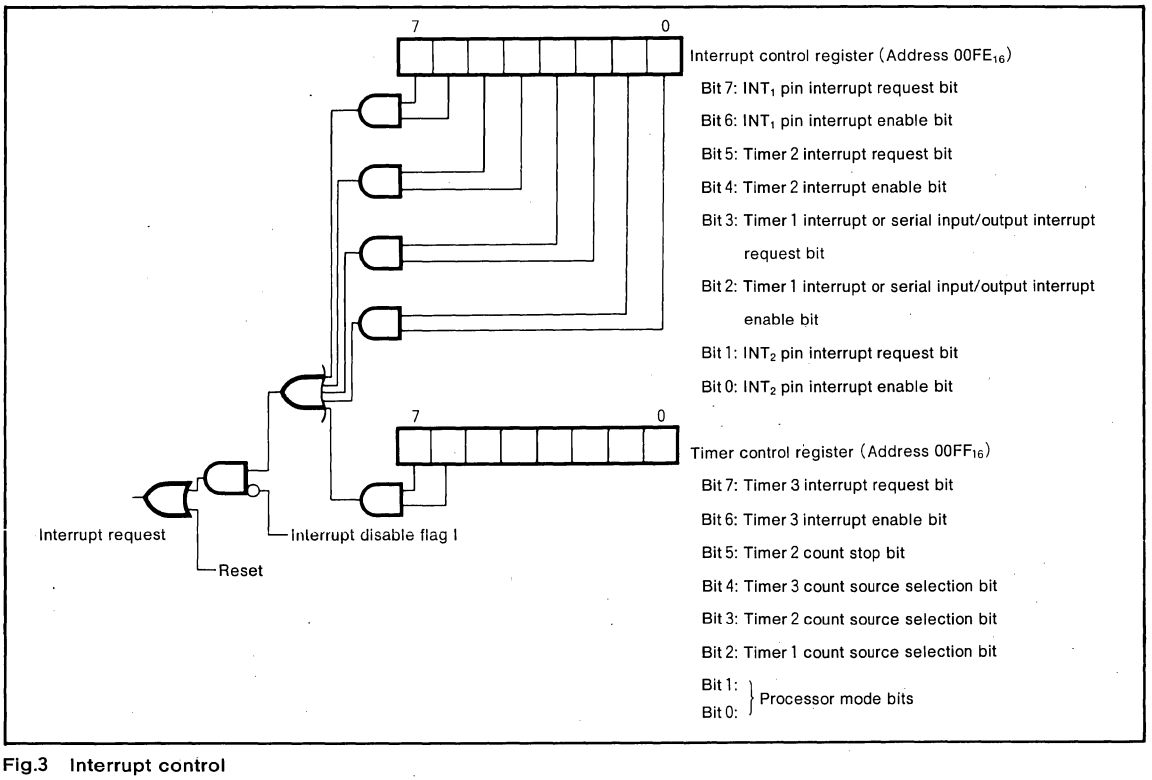


Fig.3 Interrupt control

The interrupt request bits are set when the following conditions occur:

(1) When the level of pins INT_1 and INT_2 change.
(2) When the contents of timer 3, timer 2, timer 1 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but cannot be set by the progream. However, the interrupt enable bit can be set and reset by the program.

The change in level at which the INT pins generate a interrupt varies according to the content of bits 4 and 5 of the PWM output mode register (address $00F5_{16}$). When these bits are "0", the interrupt request is generated when INT changes from high-level to low-level. When these bits are "1", the interrupt request is generated when INT changes from low-level to high-level. Bits 4 (PM_4) and 5 (PM_5) correspond to INT_1 and INT_2 respectively.

Since the BRK instruction and the INT_2 interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if INT_2 generated the interrupt.

TIMER

The M50957-XXXSP has three timers; timer 1, timer 2, and timer 3. Since P3 (in serial I/O mode) and timer 1 use some of the same architecture, they cannot be used at the same time (see serial I/O section). The count source for each timer can be selected by using bit 2, 3 and 4 of the timer control register (address $00FF_{16}$), as shown in Figure 5.

A block diagram of timer 1 through 3 is shown in Figure 4.

All of the timers are down count timers and have 8-bit latchs. When a timer counter reaches "0", the contents of the reload latch are loaded into the timer at the next clock pulse. The division ratio of the timers is $1/(n+1)$, where n is the contents of the timer latch.

The timer interrupt request bit is set to "1" at the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see Interrupt section). The starting/stopping of timer 2 can be controlled by bit 5 of the timer control register. If bit 5 (address $00FF_{16}$) is "0", the timer starts counting and when bit 5 is "1", the timer stops. The count source of timer 3 can be controlled by bit 4 of the timer control register. If bit 4 (address $00FF_{16}$) is "1", the timer counts from the $P3_2$/CNTR pin.

When the STP instruction is executed, or after reset, the timer 2 and timer 3 latch are set to FF_{16} and 07_{16}, respectivery.

After a STP instruction is executed, timer 2, timer 3, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 4 of the timer control register). This state is canceled if the timer 3 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 2 count stop bit) and bit 4 of the interrupt control register (timer 2 interrupt enable bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

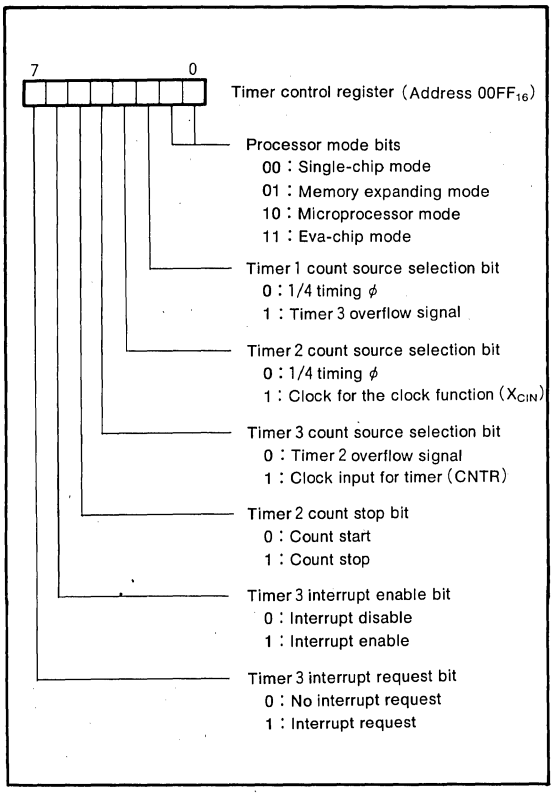


Fig.4 Structure of timer control register

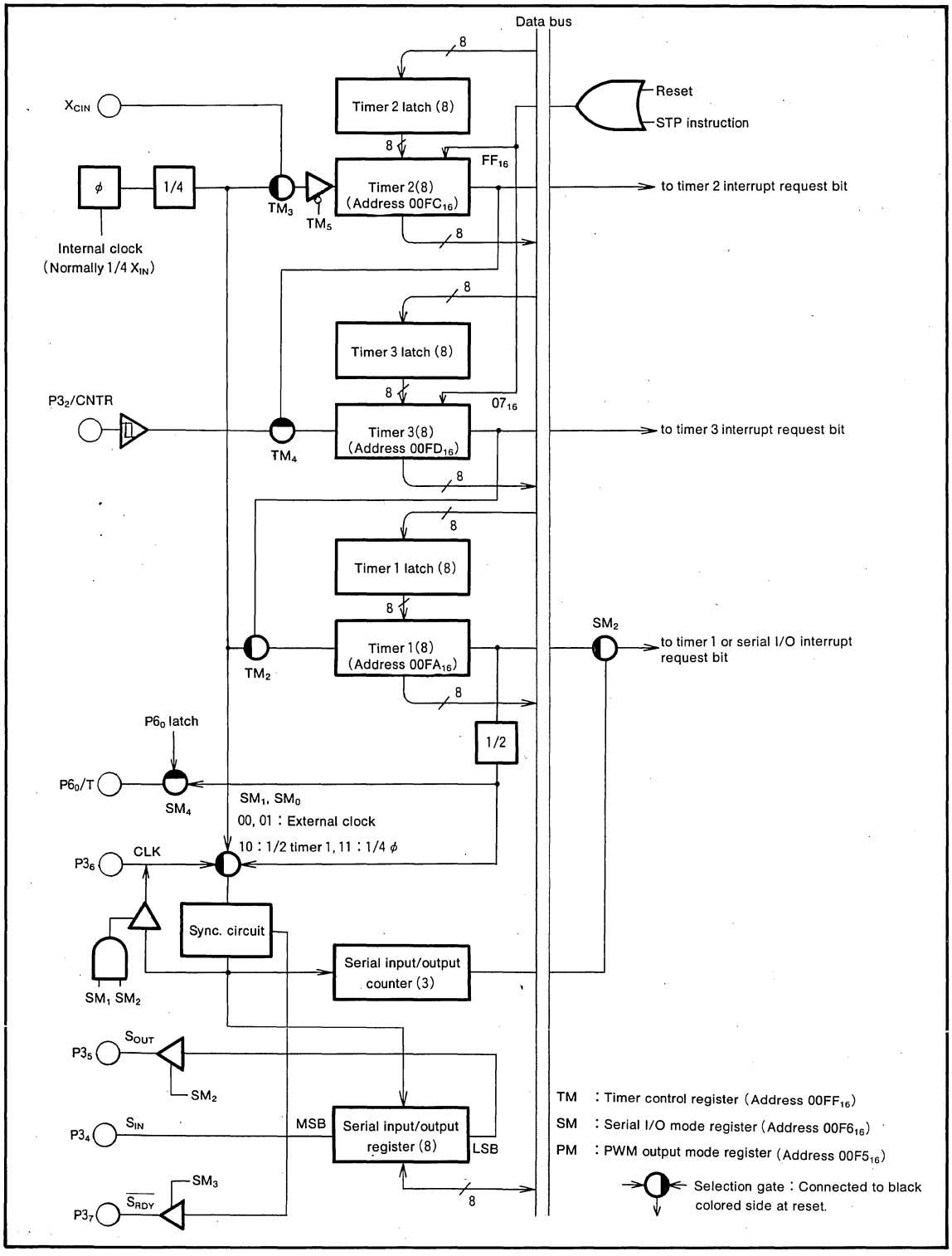


Fig.5 Block diagram of timer 1, timer 2, timer 3

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 6.

In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input /output clock (CLK), and the serial I/O pins (S_{OUT}, S_{IN}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F6_{16}$) is 8-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 1, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], timing ϕ divided by 4, becomes the clock.

Bit 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is a "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 1. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3=1, $\overline{S_{RDY}}$) or used as normal I/O pin

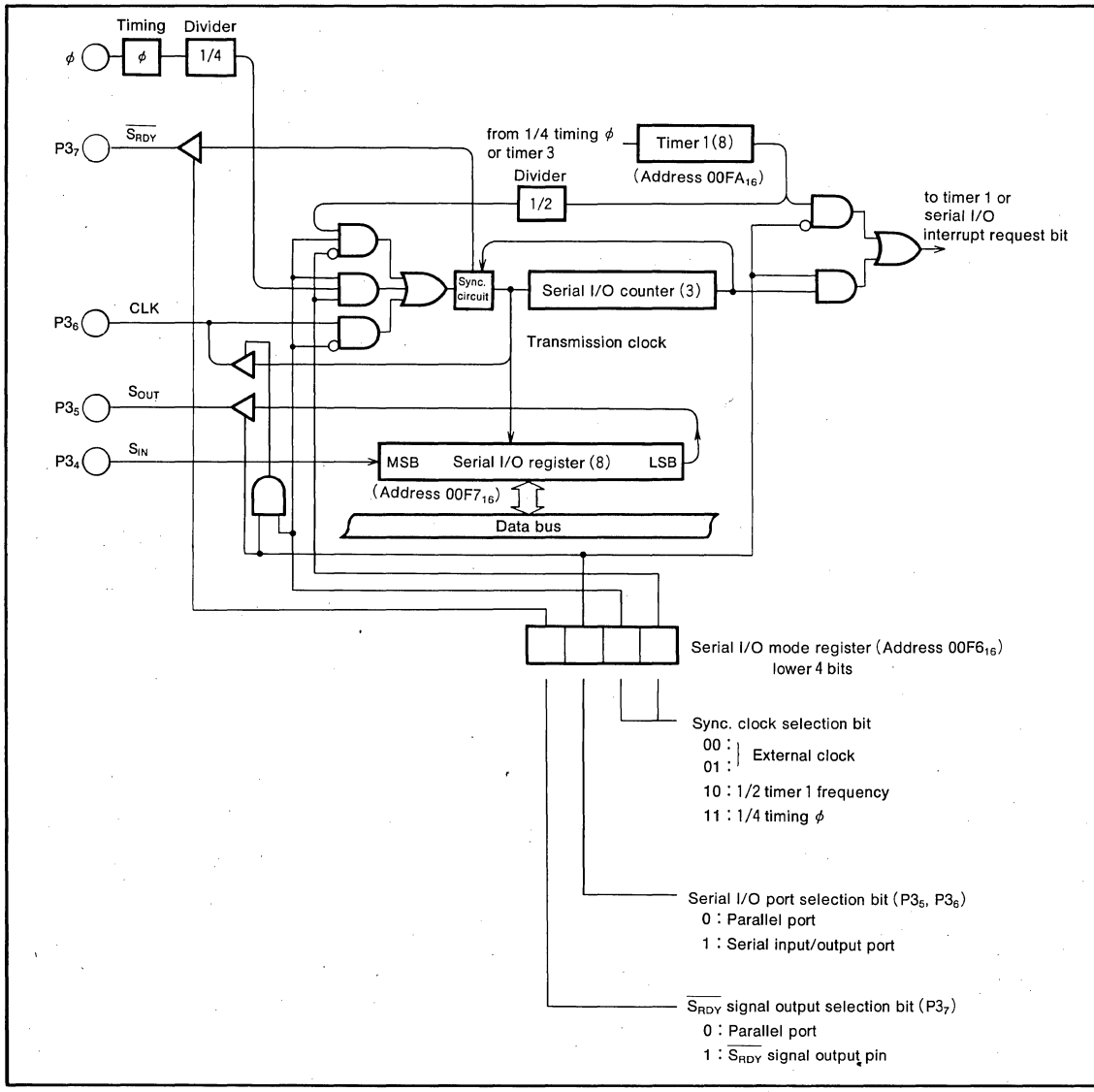


Fig.6 Block diagram of serial I/O

(bit 3=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address $00F7_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50957-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 7. An example of communication between two M50957-XXXSPs is shown in Figure 8.

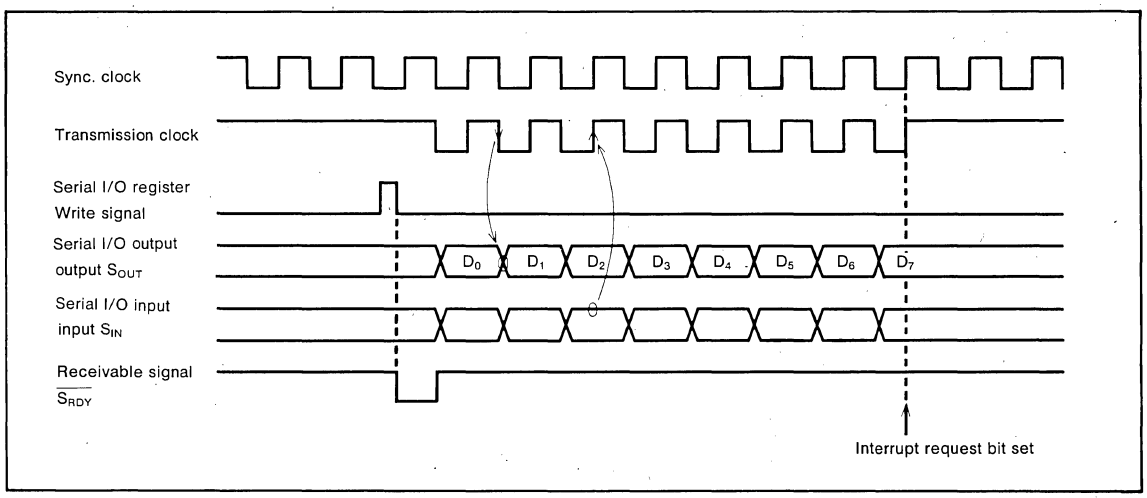


Fig.7 Serial I/O timing

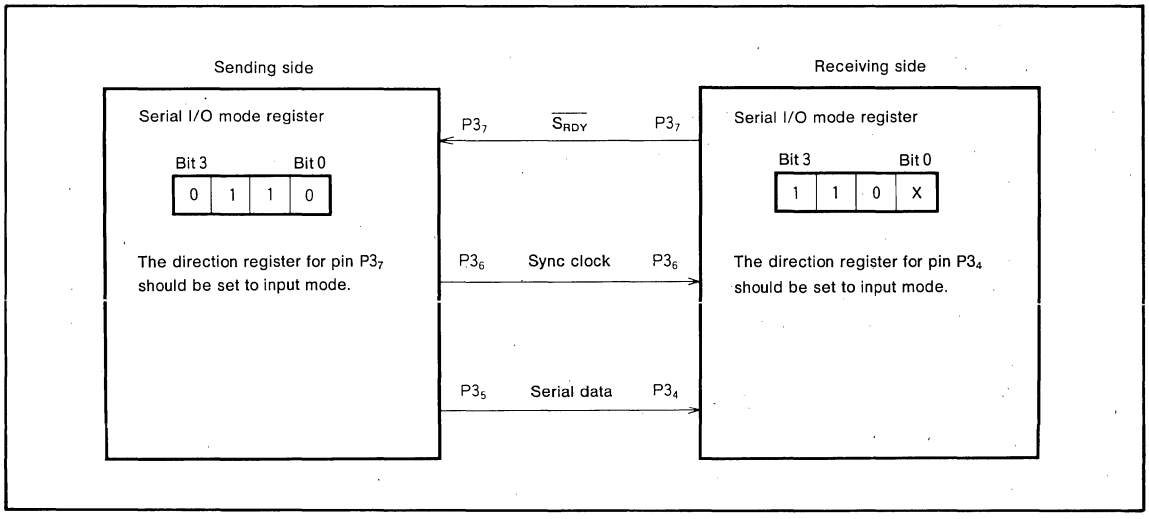


Fig.8 Example of serial I/O connection

PWM OUTPUT CIRCUIT

(1) Introduction

The M50957-XXXSP is equipped with one 14-bit PWM and two 6-bit PWMs. The 14-bit resolution gives PWM1 the minimum resolution bit width of 500ns (for X_{IN} = 4MHz) and a repeat period of 8192μs. PWM2 and PWM3 have a 6-bit resolution with minimum resolution bit width of 16μs and repeat period of 1024μs.

Block diagram of the PWM is shown in Figures 9 and 10.

The PWM timing generator section applies individual control signals to PWM 1~3, using clock input X_{IN} divided by 2 as a reference signal.

(2) Data setting

The output pins PWM1, PWM2 and PWM3 are in common with pins $P6_1$, $P6_2$ and $P6_3$ of port P6 (i.e. for PWM output, PM1~PM3 of the PWM control register and the P6 directional register $D6_1$~$D6_3$ should be set). When PWM1 is used for output, first set the higher 8-bit of the PWM1-H register (address $00F0_{16}$), then the lower 6-bit of the PWM1-L register (address $00F1_{16}$). In case of M50959-XXXSP, if the low-order 6 bits are the same, this is also possible by changing the H register only. When either PWM2 or PWM3 is used for output, set the 6-bit in the PWM2 (address $00F2_{16}$) or PWM3 (address $00F3_{16}$) register, respectively. Note that the higher 2 bits of these 8-bit registers are ignored when used 6-bit register.

(3) Transferring data from registers to latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period. The signals output to the PWM pins correspond to the contents of these latches. When data at addresses $00F0_{16}$ ~ $00F3_{16}$ is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. When the 6-bit latch is being read, the upper 2 bits of the register becomes undefined. However, bit 7 of the PWM1-L register indicated the completion of the data transfer from the PWM1 register to the PWM1 latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) Operation of the 6-bit PWMs

The timing diagram of the two 6-bit PWMs (PWM2 and PWM3) is shown in Figure 10. One period (T) is composed of 64 (2^6) segments.

There are six different pulse types configured from bits 0~5 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 11(a).

Six different pulses can be output from the PWM. These can be selected by bits 0 through 5. Depending on the content of the 6-bit PWM latch, pulses from 5~0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 11(b). Changes in the contents of the PWM latch allows the selection of 64 lengths of high-level area outputs varying from 0/64 to 63/64. An length of entirely high-level output cannot be output, i.e. 64/64.

(5) 14-bit PWM operation

The timing diagram of the 14-bit PWM1 is shown in Figure 11. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length N times τ is output every short area of t=256 τ =128μs as determined by data N of the higher 8 bits. (Refer to PWM output ② in the lower part of Figure 12 and 13.)

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that plus τ. As a result, the short-area period t(=128μs, approx. 7.8kHz) becomes an approximately repetitive period.

(6) Output after reset

At reset the output of port P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2 Relation between the 6 lower-order bits of data and the space set by the ADD bit

6 lower-order bits of data (LSB)	Area longer by τ than that of other t_m(m = 0 ~63)
0 0 0 0 0 0	Nothing
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m= 8, 24, 40, 56
0 0 1 0 0 0	m= 4, 12, 20, 28, 36, 42, 50, 58
0 1 0 0 0 0	m= 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m= 1, 3, 5, 7, ·····57, 59, 61, 63

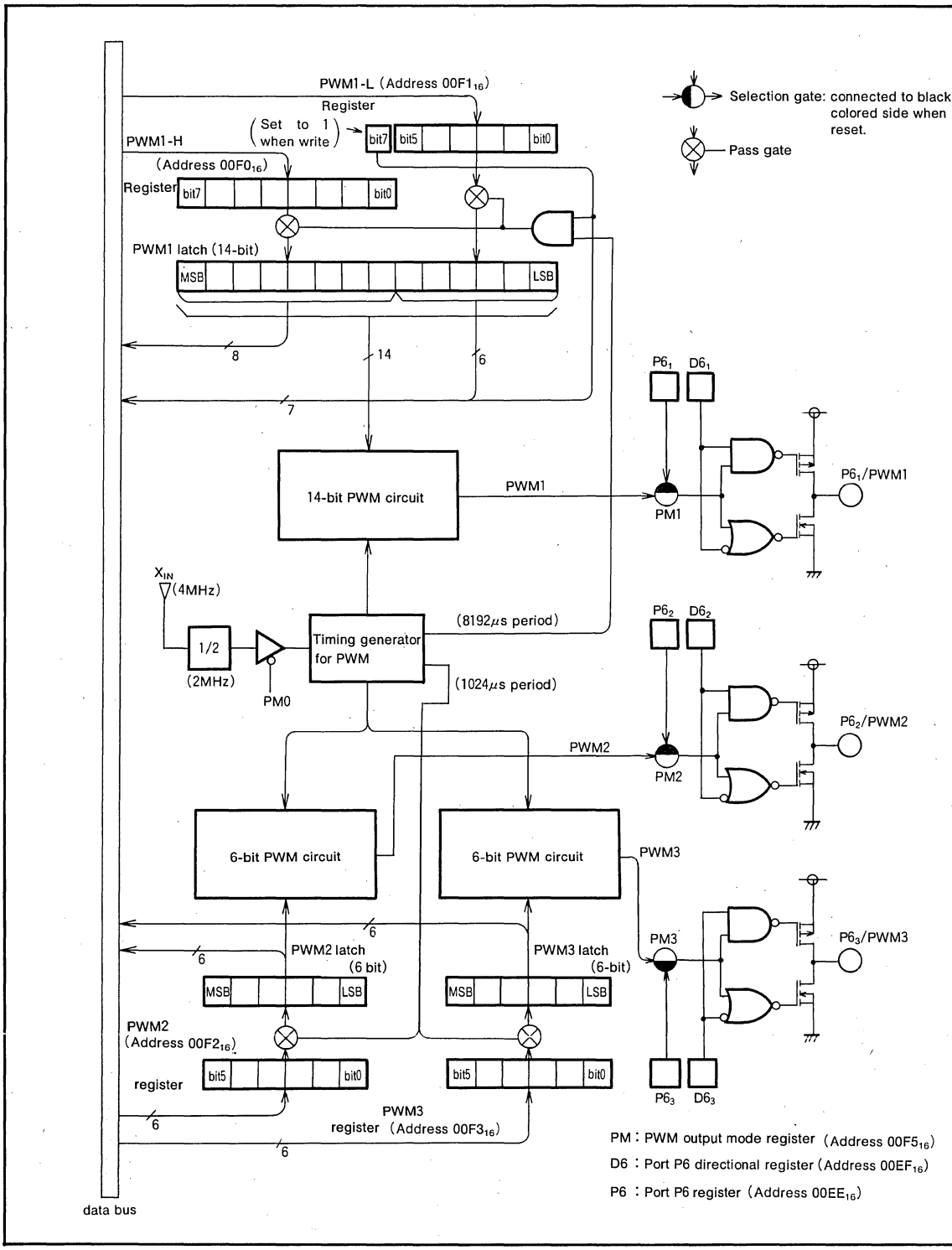


Fig.9 Bloock diagram of the PWM circuit (M50957-XXXSP)

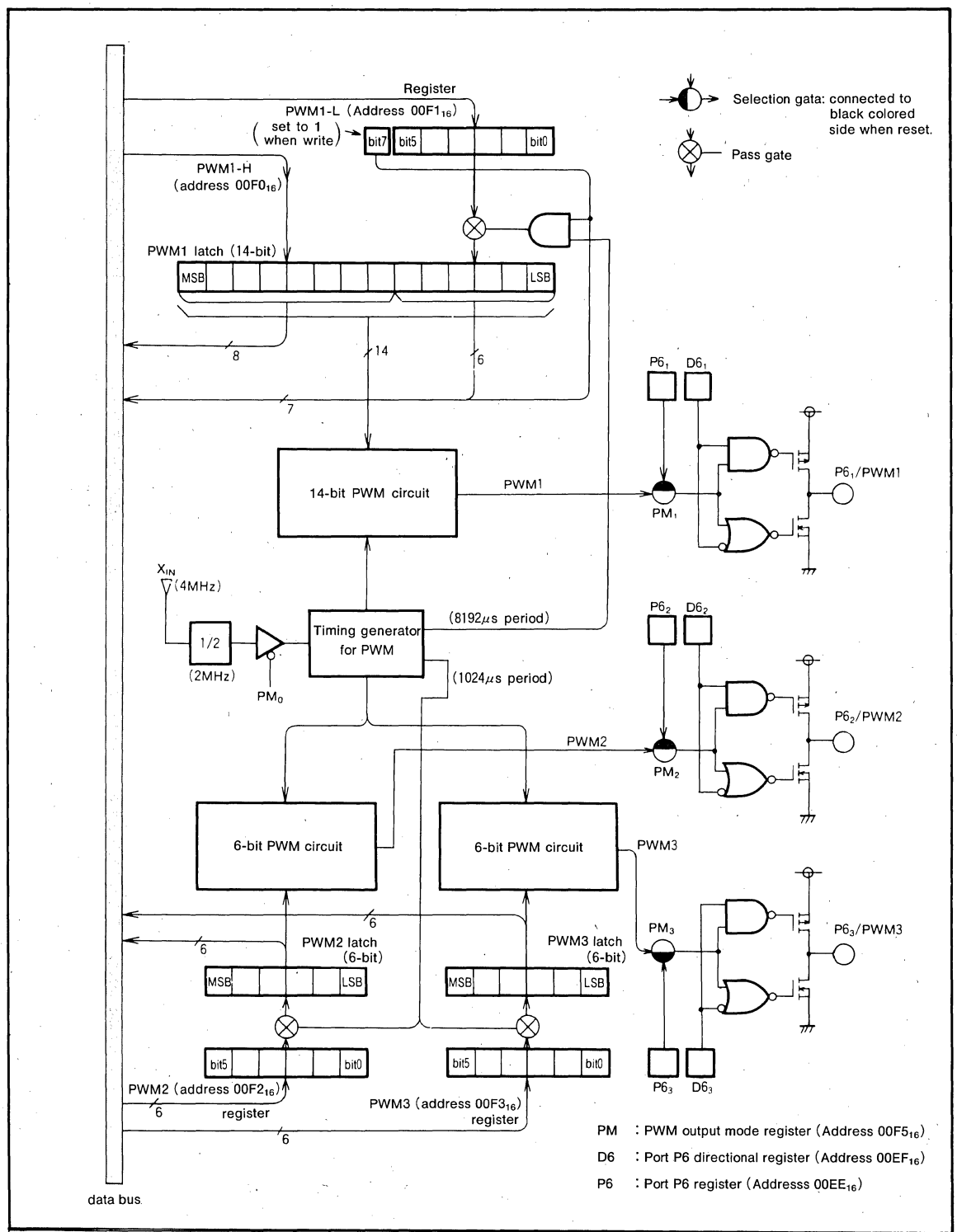


Fig.10 Block diagram of the PWM circuit (M50959-XXXSP)

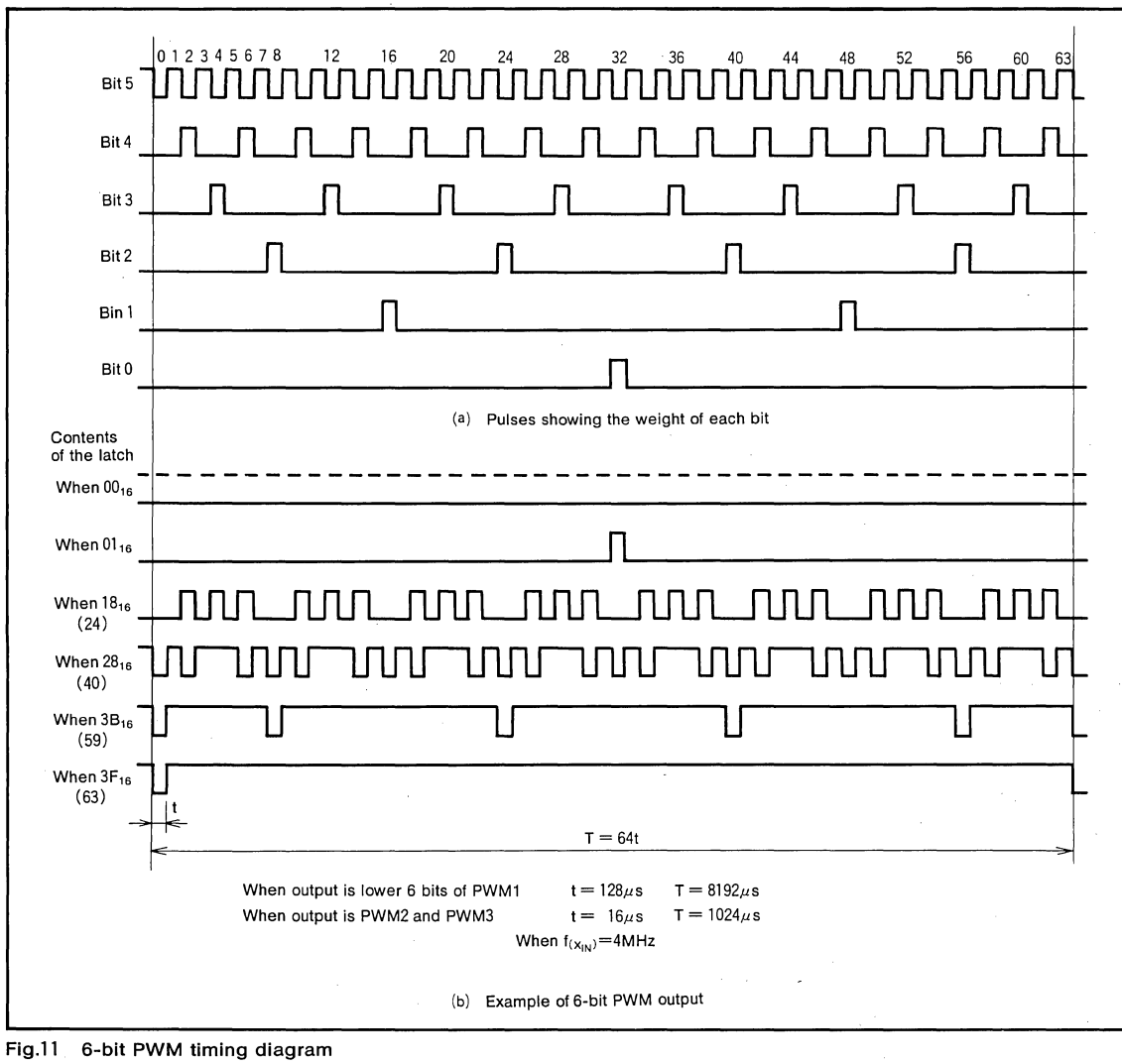


Fig.11 6-bit PWM timing diagram

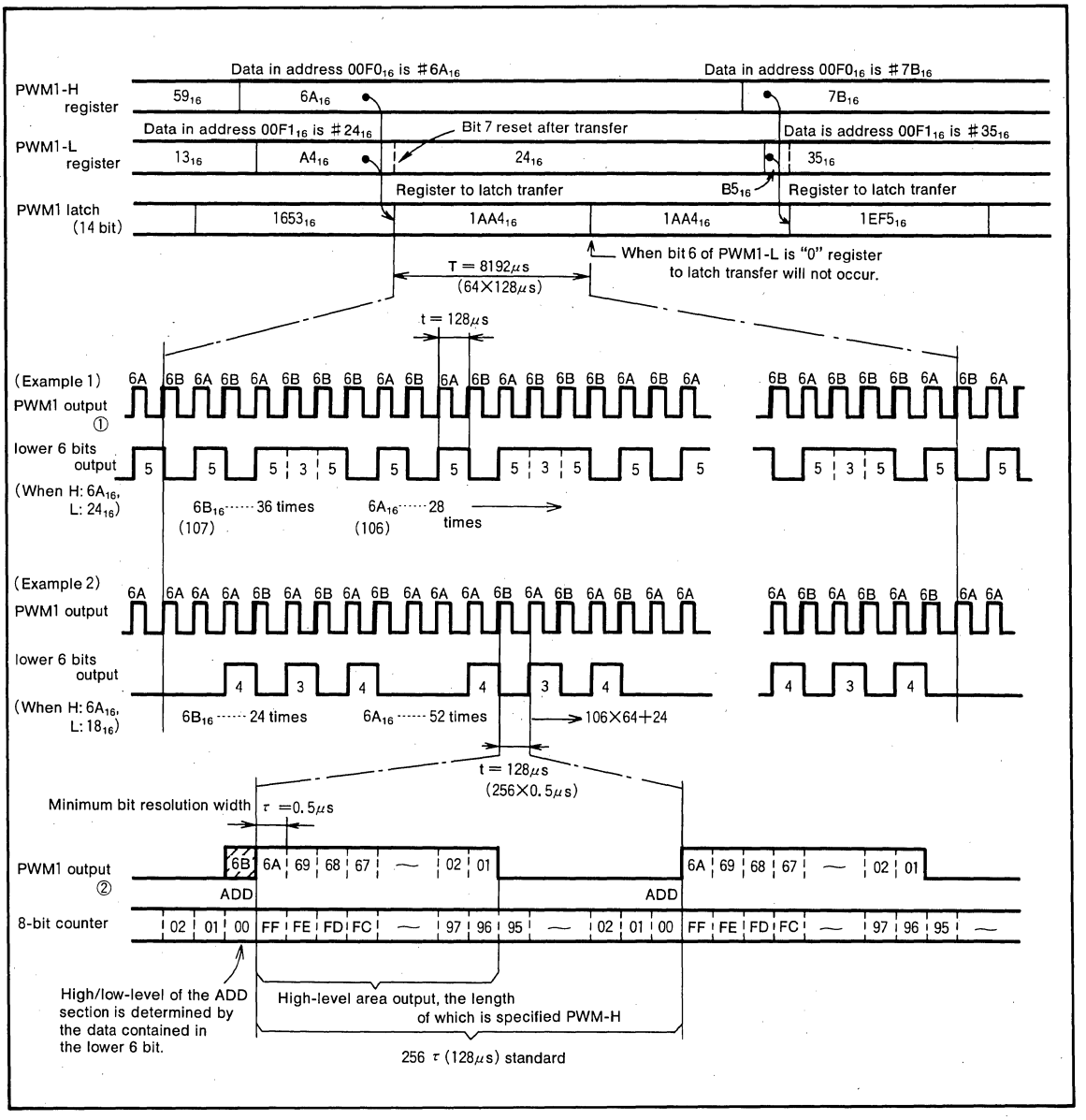


Fig.12 14-bit PWM timing diagram (M50957-XXXSP)

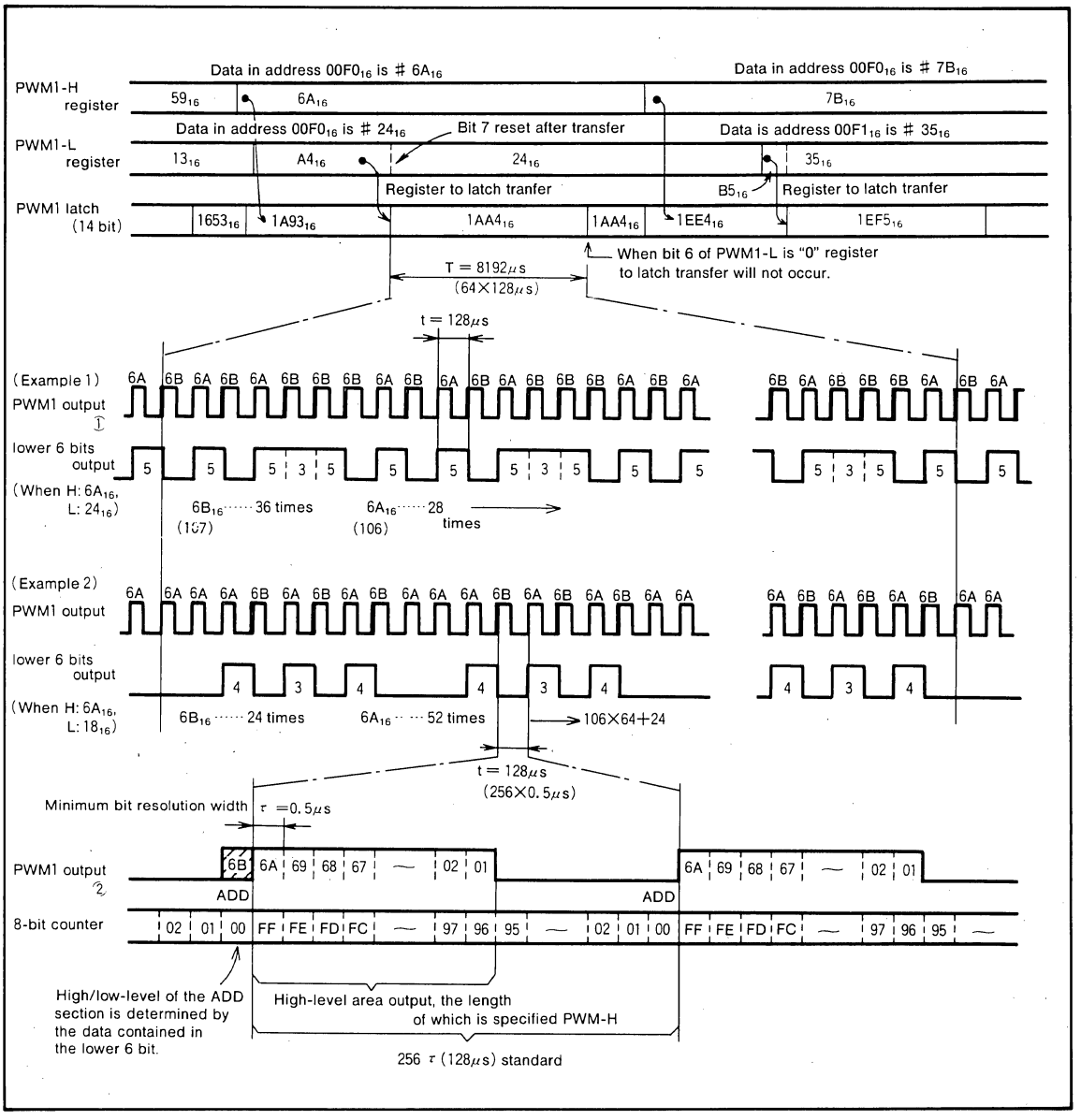


Fig.13 14-bit PWM timing diagram (M50959-XXXSP)

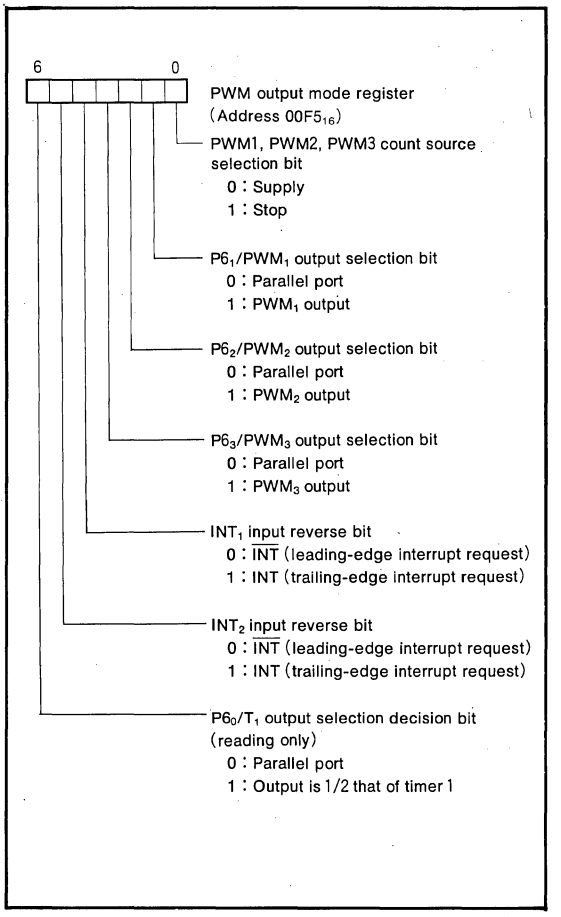


Fig.14 Structure of PWM output mode register

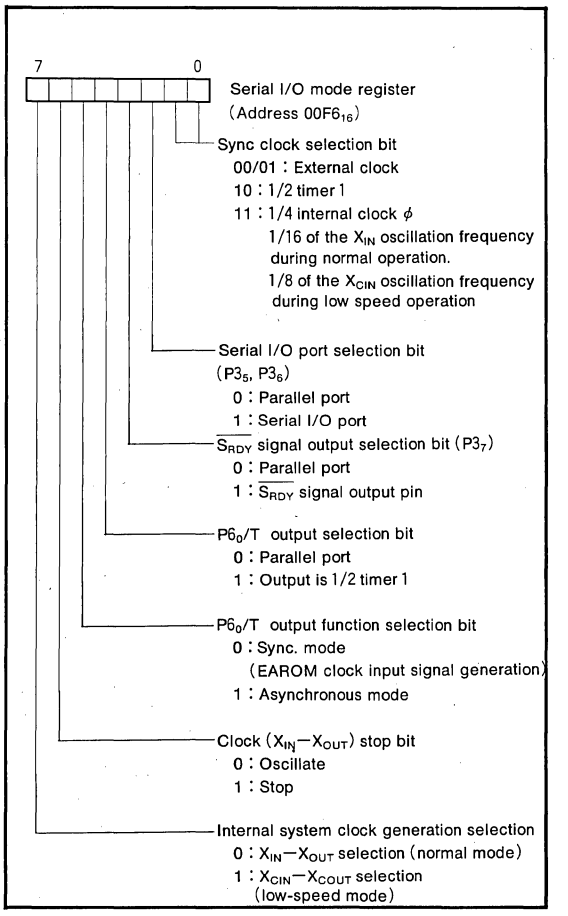


Fig.15 Structure of serial I/O mode register

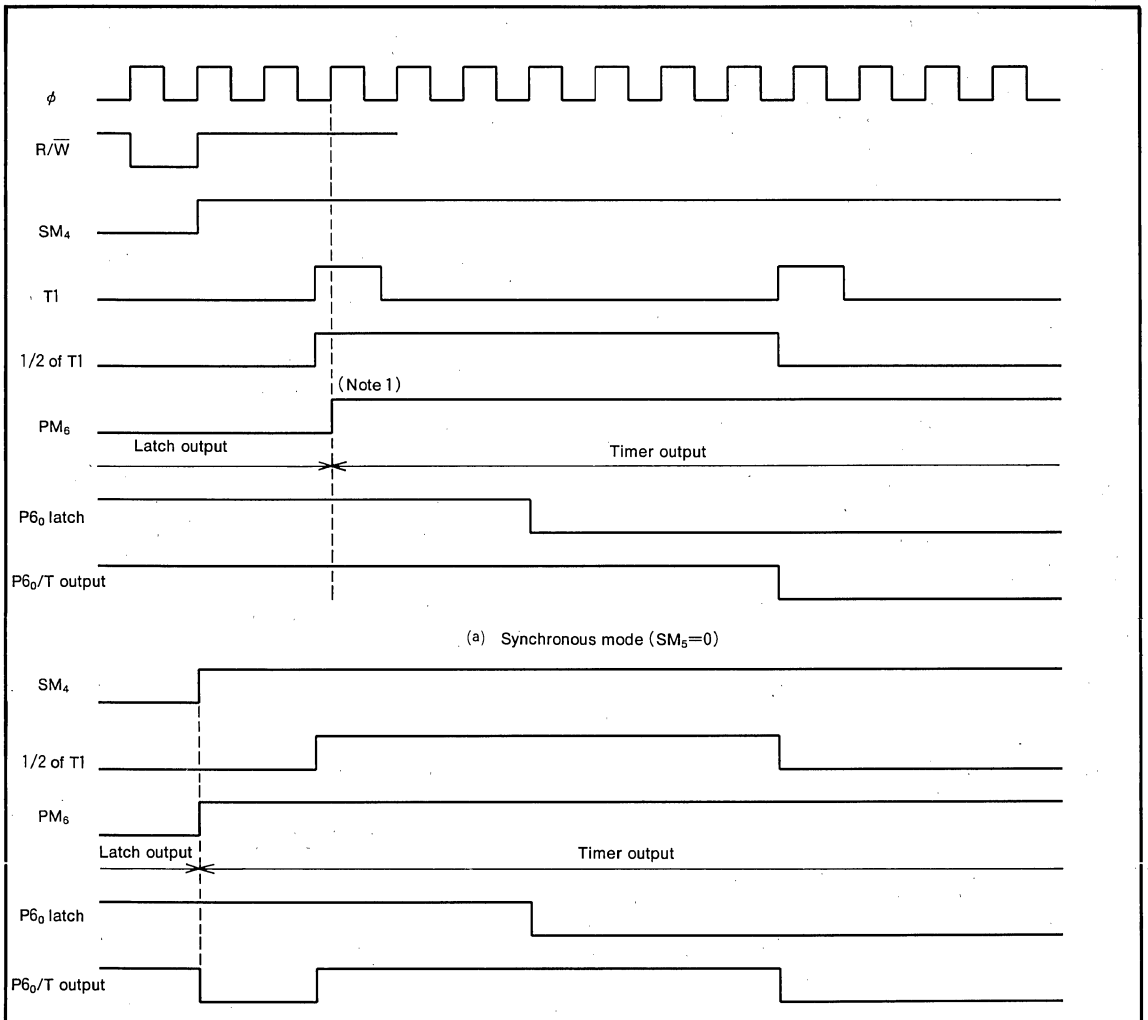
PORT $P6_0$/TIMER 1 OUTPUT

Bit 0 of port P6 outputs 1/2 the frequency of timer 1 when $00F6_{16}$ bit 4 of the serial I/O mode register (address $00F6_{16}$) is changed. The output switching can be accomplished with either of two procedures, synchronous mode or asynchronous mode, depending on the setting of bit 5 (SM_5) of the serial I/O mode register.

When SM_5 is set to "0" the synchronous mode is set. In such a case, after SM_4 has been changed, synchronization is set to the 1/2 frequency of timer 1 and switching between the port latch and timer takes place. It is possible to ascertain whether switching actually occurred by reading the value of bit 6 (PM_6) of the PWM output mode register.

From the time that the contents of SM_4 was changed to the point where switching completes, the contents of neither SM_4 nor $P6_0$ may be changed. Use of the synchronous mode prevents the generation of a pulse shorter than the timer output during swiching. Figure 16 (a) gives an example of timing in the synchronous mode. Use of the synchronous mode allows generation of an EAROM clock input signal through the use of a simple program.

When SM_5 is set to "1", the asynchronous mode is set. In this case, the output switching occurs directly after SM_4 has been changed. Figure 16 (b) gives an example of timing in the asynchronous mode.



Note 1 : Output switching occurs at the trailing edge of timer 1 divided signal when the value of the $P6_0$ latch is "0" and at the leading edge of timer 1 divided signal when the value of the $P6_0$ latch is "1".

Fig.16 $P6_0$/T switching timing diagram

COMPARATOR CIRCUIT

The comparator circuit is shown in Figure 17. The comparator circuit consists of the switch tree, ladder resistor, comparator, comparator control circuit, comparator register (address $00FB_{16}$), and analog signal input pin ($P3_3/AN_{IN}$). The analog input pin is common with the digital input/output terminal to the data bus.

The 5-bit comparator register can generate $1/16V_{CC}$-step internal analog voltage, based on the settings of bits 0 to 3. Table 3 gives the relation between the descriptions of comparator register bits 0 to 3 and the generated internal analog voltage. The comparator result of the analog input voltage and the internal analog voltage is stored in the comparator register, bit 4.

The data is compared by setting the directional register corresponding to board $P3_3$ to "0" (board $P3_3$ enters the input mode), to allow board $P3_3/AN_{IN}$ to be used as the analog input pin. The digital value corresponding to the internal analog voltage to be compared is then written in the comparision register (address $00FB_{16}$), bits 0 to 3. The voltage comparision starts as soon as the writing is completed. 4-cycle (required for comparating) later, the result of comparision is stored in the comparator register, bit 4. Bit 4 is "1" when analog input voltage > internal analog voltage and "0" when analog input voltage < internal analog voltage.

When voltage is compared to by setting bits 0 to 3 of the comparator register "0", bit 4 of the comparator register becomes "1" regardless of the analog input voltage.

Table 3 Relationship between the contents of comparator register and internal voltage

Comparator register				Internal analog voltage
bit 3	bit 2	bit 1	bit 0	
0	0	0	1	$1/16V_{CC}-1/32V_{CC}$
0	0	1	0	$2/16V_{CC}-1/32V_{CC}$
0	0	1	1	$3/16V_{CC}-1/32V_{CC}$
0	1	0	0	$4/16V_{CC}-1/32V_{CC}$
0	1	0	1	$5/16V_{CC}-1/32V_{CC}$
0	1	1	0	$6/16V_{CC}-1/32V_{CC}$
0	1	1	1	$7/16V_{CC}-1/32V_{CC}$
1	0	0	0	$8/16V_{CC}-1/32V_{CC}$
1	0	0	1	$9/16V_{CC}-1/32V_{CC}$
1	0	1	0	$10/16V_{CC}-1/32V_{CC}$
1	0	1	1	$11/16V_{CC}-1/32V_{CC}$
1	1	0	0	$12/16V_{CC}-1/32V_{CC}$
1	1	0	1	$13/16V_{CC}-1/32V_{CC}$
1	1	1	0	$14/16V_{CC}-1/32V_{CC}$
1	1	1	1	$15/16V_{CC}-1/32V_{CC}$

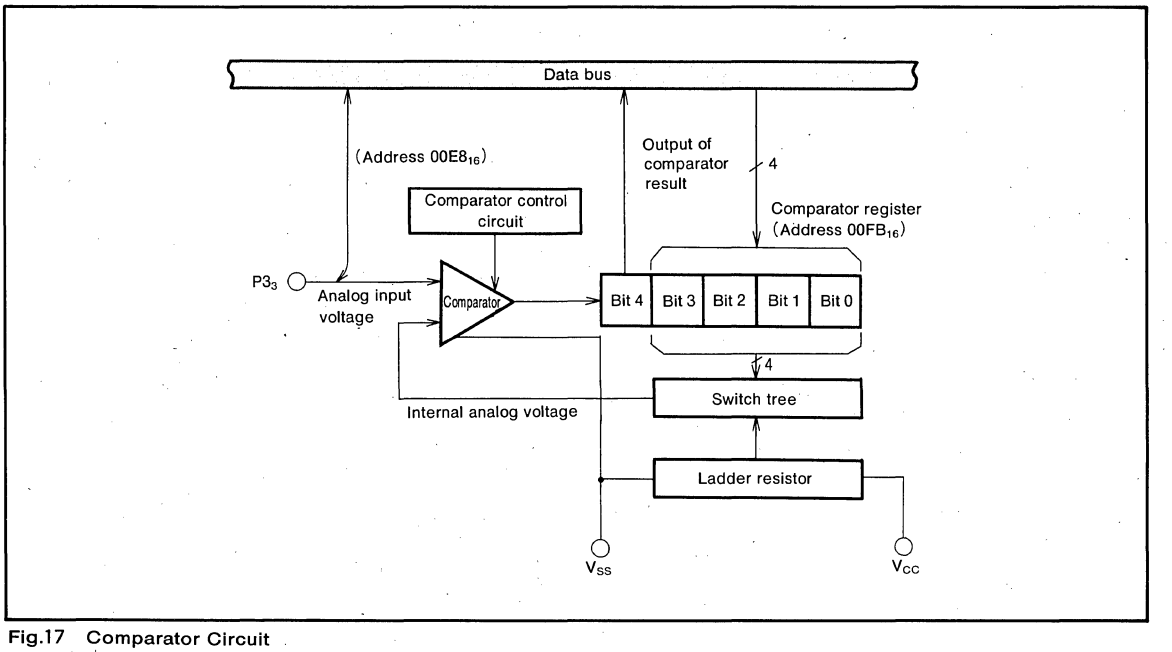


Fig.17 Comparator Circuit

RESET CIRCUIT

The M50957-XXXSP is reset according to the sequence shown in Figure 18. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for no less than 2 μs while the power voltage is between 4 and 5.5V and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 19.

An example of the reset circuit is shown in Figure 20. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.0V.

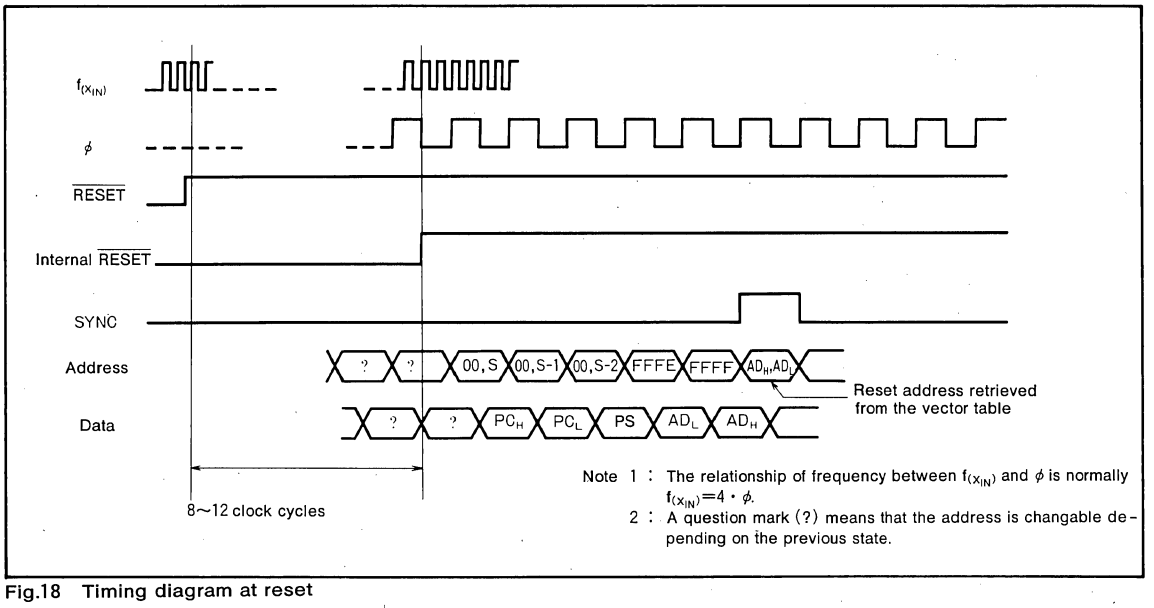


Fig.18 Timing diagram at reset

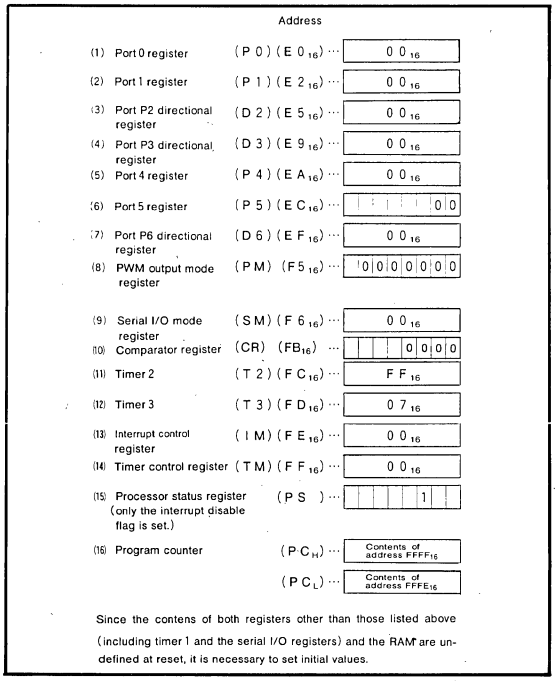


Fig.19 Internal state of the microcomputer at reset

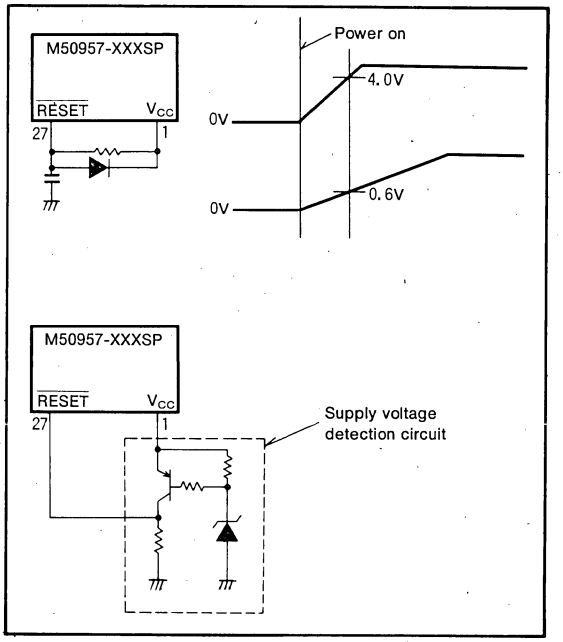


Fig.20 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit output port with high-breakdown voltage P-channel open drain outputs featuring a breakdown voltage of V_{CC}-36V. Each pin contains a pull-down resistor making V_P a negative power source. As shown in the memory map in Figure 1, port P0 is used on the zero page at address $00E0_{16}$ in memory.

Depending on the content of the processor mode bit (bits 0 and 1 of address $00FF_{16}$), four modes can be selected, single-chip mode, memory expanding mode, microprocessor mode, memory expanding mode, microprocessor mode, and eva-chip mode. Modes other than the single-chip mode also have functions as address output pins besides their original functions. For details, refer to the section on the processor mode.

(2) Port P1

Port P1 has the same functions as port P0 in the single-chip mode. In modes other than the single-chip mode, functions vary slightly. For details, see the section on the processor mode.

(3) Port P2

Port P2 is an 8-bit I/O port with N-channel open drain outputs As shown in Figure 1, port P2 is used at address $00E4_{16}$ in the memory.

Port P2 has a data direction register (address $00E5_{16}$ on zero page) and programming can be undertaken for an individual bit to use the port for input or output. The pins where the data direction register is programmed to "1" are for output and those where the register is programmed to "0" are for input.

The data written into the pin programmed as an output pin are written into the port latch and supplied directly to the output pin. When reading the data from a pin programmed as an output pin, it is not the output pin contents which are read but the port latch contents. Consequently, since an LED or other similar part is driven directly, the value output previously can be read correctly even if the low-level output voltage goes high. The pin programmed as an input pin remains floating, so external signals can be read. When data is written, it is written into the port latch only and the pin remains floating.

This port has the same functions as port P0 except for the single-chip mode. For details, see the section on the processor mode.

(4) Port P3

Apart from the fact that part of the pins are also used as serial input/output pins, analog input pin and timer 3 clock input pin, its functions are the same as those of port P2 in the single-chip mode. This port has the same functions as port P0 except in the single-chip mode. For details, see the section on the processor mode.

(5) Port P4

Port P4 has the same functions as port P0 in the single-chip mode. The functions of this port do not change regardless of though the processor mode.

(6) Port P5

Bits 0 and 1 of port P5 have the same functions as port P4.

Bits 2 and 3 are exclusively used as inputs for mutual use as interrupt inputs. These pins feature hysteresis characteristics. These pins can also be used for fetching inputs even when being used as interrupt inputs.

The interrupt request bits (bit 7 and 1 of address $00FE_{16}$ = INT_1 and INT_2, respectively) are set to "1" when the inputs of ports $P5_3$ (INT_1) and $P5_2$ (INT_2) change. Depending on the contents of bits 4 and 5 of the PWM output mode register PM (address $00F5_{16}$), either a raising-edge interrupt or a falling-edge interrupt may be selected as the interrupt source. (Refer to Figure 14.)

Since interrupt input and normal input ports are used together in the M50957-XXXSP, unwanted noise may mistakenly cause interrupts. This problem can be overcome by programming.

When changing either bit 4 (PM_4) or bit 5 (PM_5) of the PWM output mode register, it is necessary for the interrupt request enable bit (either bit 6 or 0 of address $00FE_{16}$) to be set to the interrupt disable condition ("0"). If this is not done, an interrupt will be generated when either PM_4 or PM_5 is changed.

Bits 4 through 7 of port P5 is a 4-bit input port.

(7) Port P6

Port P6 is a 6-bit I/O port having the same functions as Port P2. The output is CMOS three-state. Bit 0 is used in common with the timer output. Bits 1～3 are used in common with PWMs 1～3.

The functions of this port do not change, being the same as in the single-chip mode, even though the processor mode may change.

A block diagram of ports P0 through P6 are shown in Figure 21.

(8) Clock ϕ output pin

The clock frequency, divided by four, is output (X_{IN}). However, in the low-speed mode 1/2 the clock frequency for timer (X_{CIN}) is output.

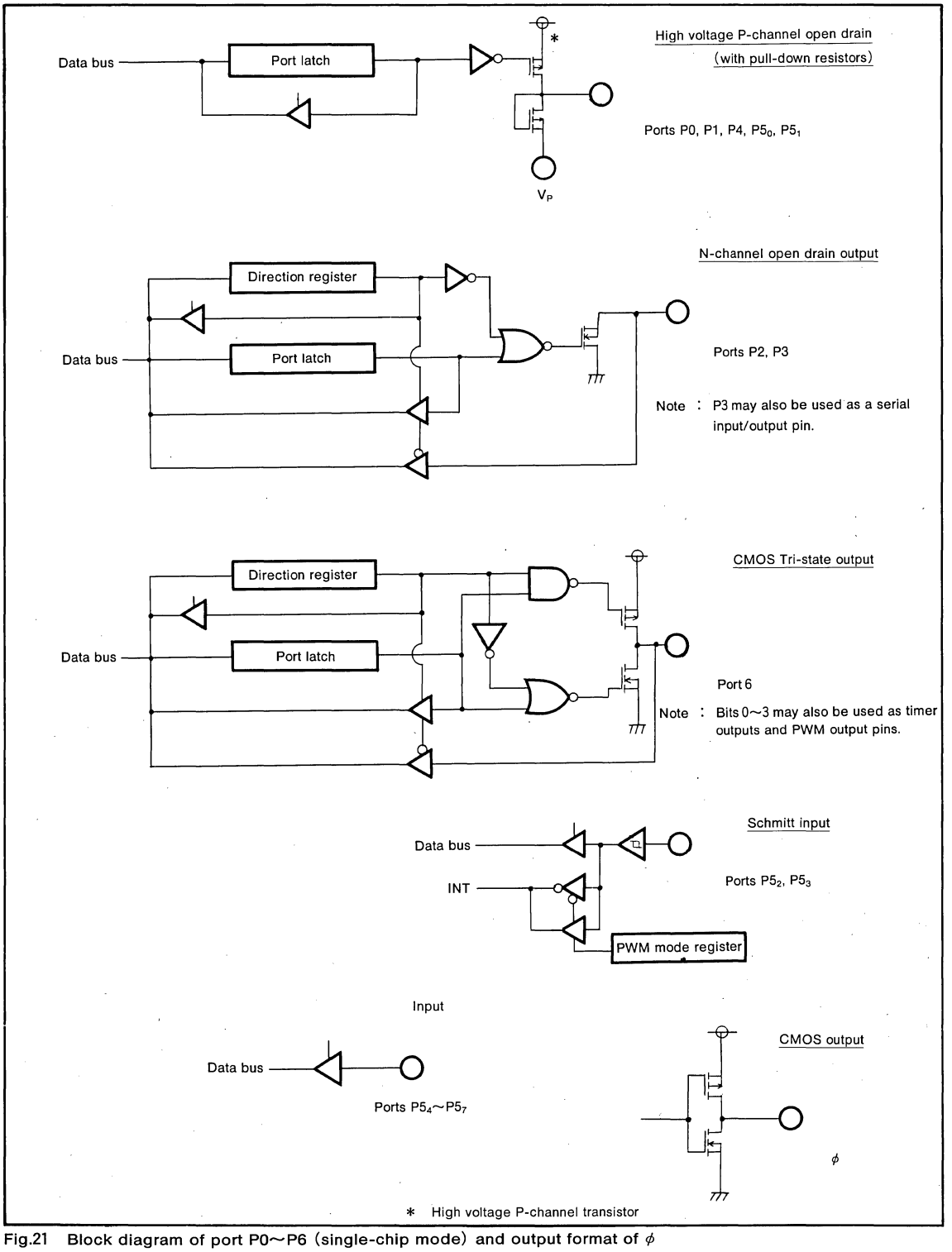


Fig.21 Block diagram of port P0~P6 (single-chip mode) and output format of ϕ

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 23 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 22.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

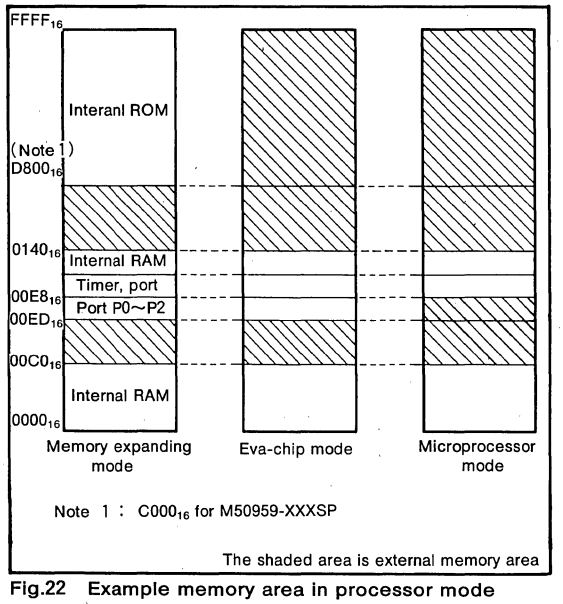


Fig.22 Example memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original output functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original output functions. Port P2 retains its original output functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode.

In this mode, port P0 and P1 are used as the system address bus and the original function of the I/O pins is lost. Port P2 becomes the data bus (D_7～D_0) and loses its normal output functions. Port $P3_1$ and $P3_0$ become the SYNC and R/$\overline{W}$ pins, respectively and the normal I/O functions are lost.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is required.

This mode has almost the same function as the memory expanding mode except that it needs to attach all program memories to the outside.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

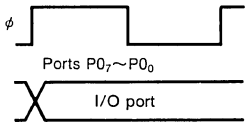
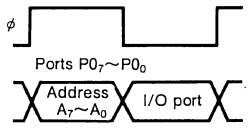
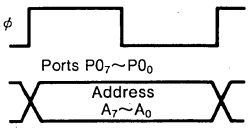
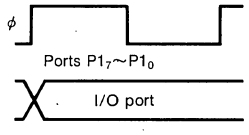
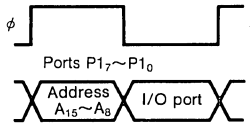
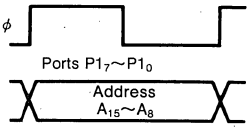
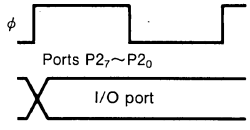
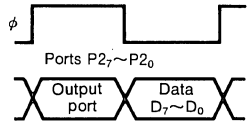
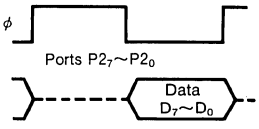
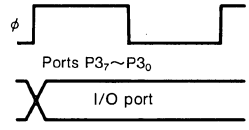
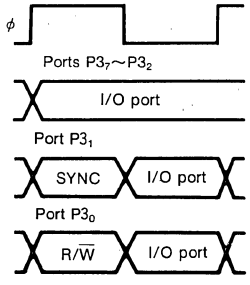
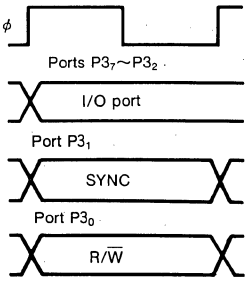
Port \ Mode	TM_1 = 0, TM_0 = 0 Single-chip mode	TM_1 = 0, TM_0 = 1 Memory expanding mode	TM_1 = 1, TM_0 = 1 Eva-chip mode	TM_1 = 1, TM_0 = 0 Microprocessor mode
Port P0			Same as left	
Port P1			Same as left	
Port P2			Same as left	
Port P3			Same as left	

Fig.23 Processor mode and functions of ports P0~P3

Table 4 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The M50957-XXXSP has two internal clock generating circuits. Figure 26 shows a block diagram of the clock generating circuits. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ. Bit 7 of serial I/O mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 24 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 25.

The M50957-XXXSP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 2 and timer 3 are forcibly connected and $\phi/4$ is selected as timer 2 input. When restarting oscillation, FF_{16} is automatically set in timer 2 and 07_{16} in timer 3 in order to enable the oscillator to stabilize. Before executing the STP instruction, the timer 2 count stop bit must be set to supply ("0"), timer 2 interrupt enable bit and timer 3 interrupt enable bit must be set to disable ("0"), and timer 3 interrupt request bit must be set to no request ("0").

Oscillation is restarted (release the stop mode) when INT_1, INT_2, or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 3 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the $\overline{RESET}$ pin until the oscillation stabilizes because no wait time is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it recieves an interrupt.

Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock (200μA or less at f(X_{CIN})=32kHz). X_{IN} clock oscillation is stopped when the bit 6 of serial I/O mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. An "L" level must be kept to the $\overline{RESET}$ pin unit the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 27 shows the transition of states for the system clock.

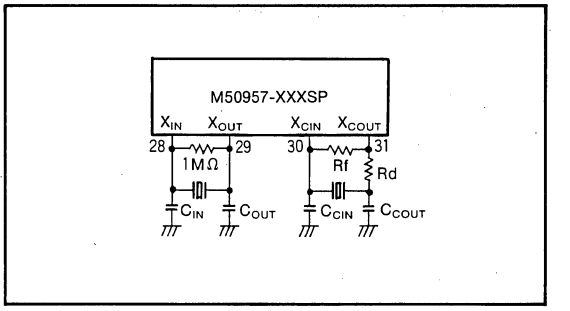


Fig.24 Example ceramic resonator circuit

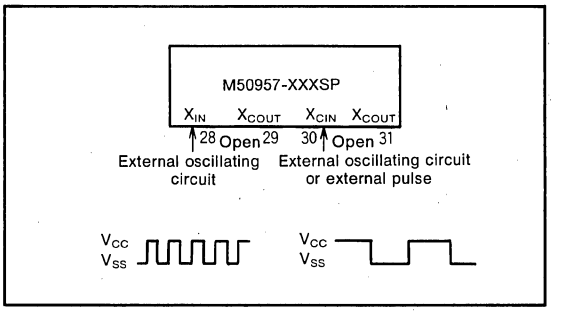


Fig.25 Example clock input circuit

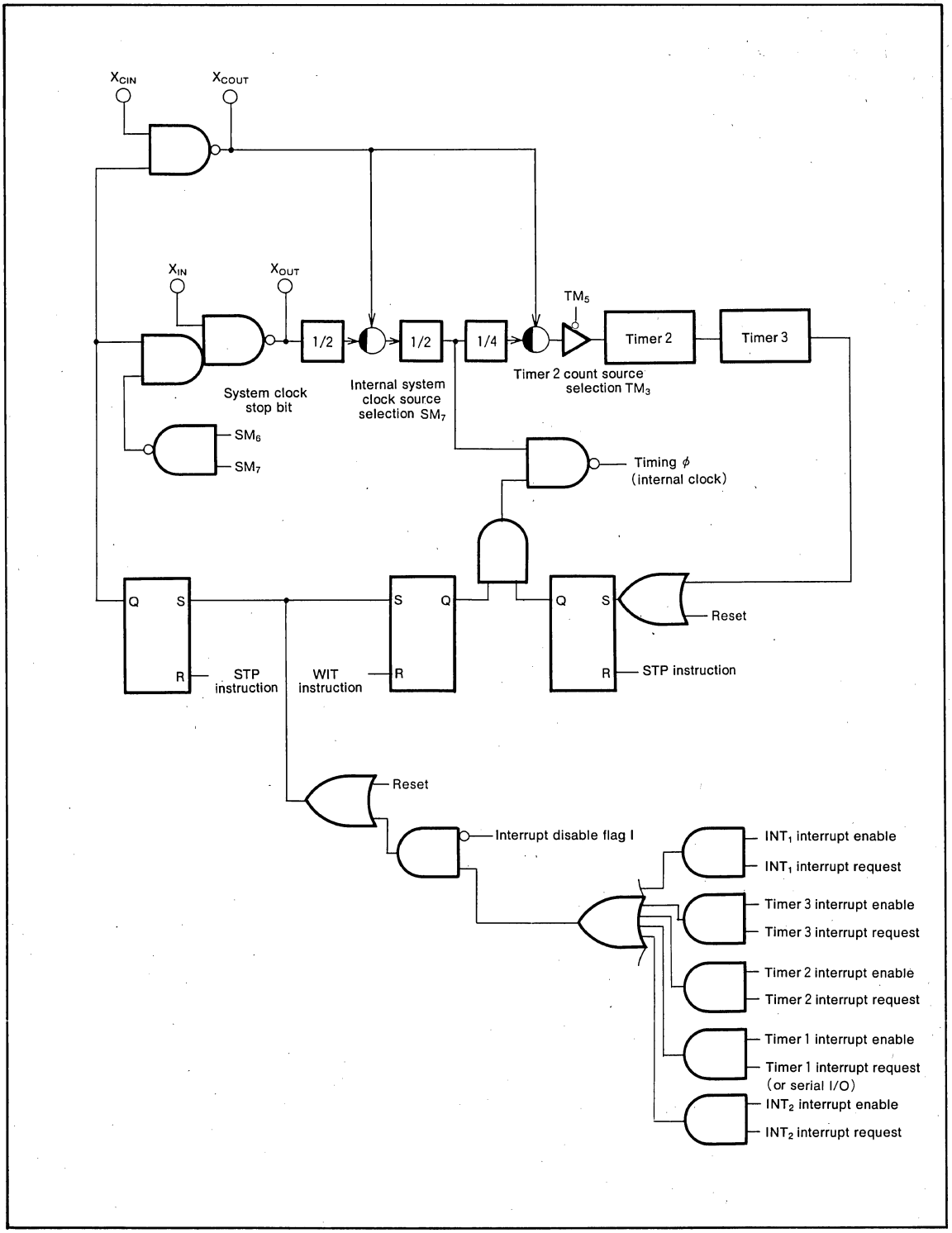
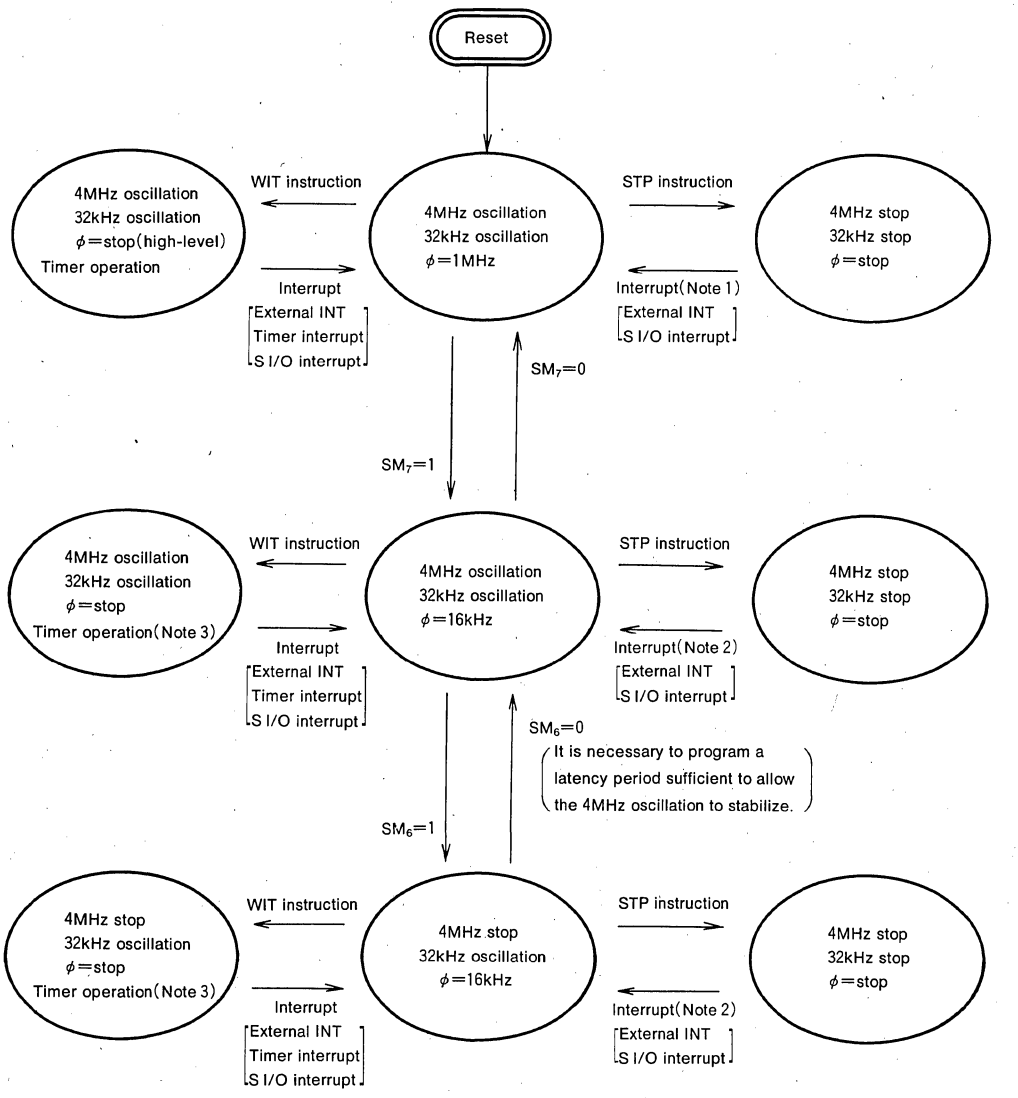


Fig.26 Block diagram of clock denerating circuit

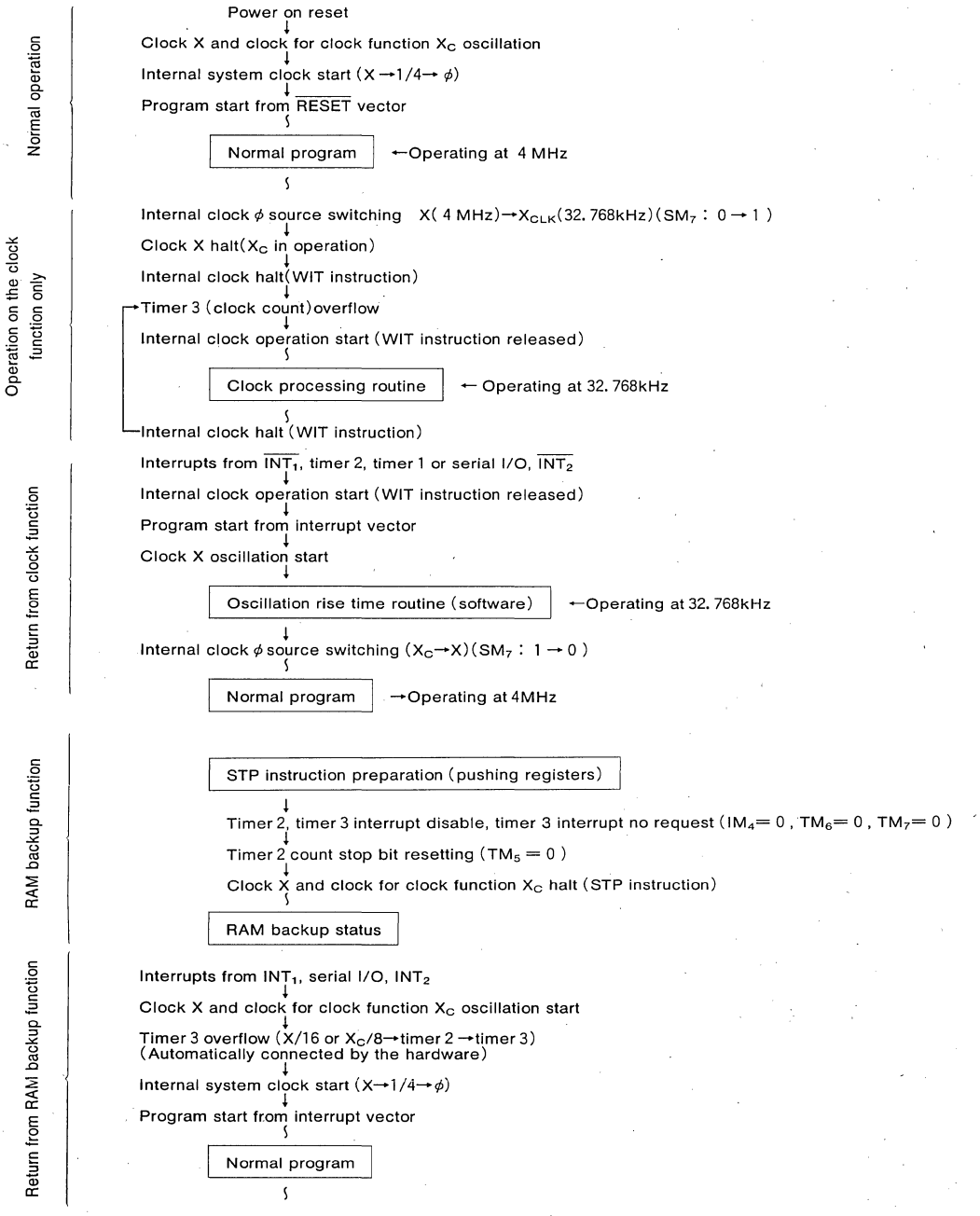


The above example assumes that signals of 4MHz and 32kHz are being applied to pins X_{IN} X_{CIN} respectively. φ signifies the internal clock.

(Note 1) Approximately 8ms of latency time are automatically generated upon release from the STP instruction due to the connections of timer 2 and 3.
(Note 2) Approximately 500ms of latency time exists after the release of the STP instruction.
(Note 3) When the internal clock 1/4 frequency is connected as a timer count source the count source becomes 4kHz.

Fig.27 Transition of states for the system clock

≪An example of flow for system≫



PROGRAM NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When $\phi/4$ or it divided by timer are used as clock for timer, the contents of the timer can be read at voluntary timing.
However, when an other clock (except above clocks) is input to timer, read the contents of timer either while the input of the timer is not changing or after timer count is stopped.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3 sets

Write the following option on the mask confirmation form

(1) ϕ output stop option

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off.	−0.3∼7	V
V_P	Pull-down input voltage		V_{CC}−40∼V_{CC}+0.3	V
V_I	Input voltage, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P3_4$∼$P3_7$ CNV_{SS}, $P5_2/INT_2$, $P5_3/INT_1$		−0.3∼13	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, X_{CIN}		−0.3∼7	V
V_I	Input voltage, $P6_0$∼$P6_5$, $P3_3$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage, $P5_4$∼$P5_7$		−0.3∼13	V
V_O	Output voltage, $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P3_4$∼$P3_7$		−0.3∼13	V
V_O	Output voltage, $P6_0$∼$P6_5$, X_{OUT}, X_{COUT}, ϕ, $P3_3$		−0.3∼V_{CC}+0.3	V
V_O	Output voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P4_0$∼$P4_7$, $P5_0$, $P5_1$		V_{CC}−40∼V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
T_{opr}	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : 600mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Nom.	Limits Max.	Unit
V_{CC}	Supply voltage	$f_{(X_{IN})}$=4.2MHz	4	5	5.5	V
		$f_{(X_{IN})}$=less than1MHz	3	5	5.5	V
V_P	Pull-down supply voltage		V_{CC}−38		V_{CC}	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNV_{SS}(Note 2) $P5_2/INT_2$, $P5_3/INT_1$, $P6_0$∼$P6_5$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P5_4$∼$P5_7$		0.4V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNV_{SS} $P5_2/INT_2$, $P5_3/INT_1$, $P6_0$∼$P6_5$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P5_4$∼$P5_7$		0		0.12V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P4_0$∼$P4_7$ $P5_0$, $P5_1$				−120	mA
$I_{OH(sum)}$	"H" sum output current $P6_0$∼$P6_5$				−5	mA
$I_{OL(sum)}$	"L" sum output current $P2_0$∼$P2_7$, $P3_0$∼$P3_7$				50	mA
$I_{OL(sum)}$	"L" sum output current $P6_0$∼$P6_5$				5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$∼$P0_4$				−40	mA
$I_{OH(peak)}$	"H" peak output current $P0_5$∼$P0_7$, $P1_0$∼$P1_7$				−30	mA
$I_{OH(peak)}$	"H" peak output current $P4_0$∼$P4_7$, $P5_0$, $P5_1$				−30	mA
$I_{OH(peak)}$	"H" peak output current $P6_0$∼$P6_5$				−3	mA
$I_{OL(peak)}$	"L" peak output current $P2_0$∼$P2_7$, $P3_0$∼$P3_7$				15	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$∼$P6_5$				3	mA
$I_{OH(avg)}$	"H" average output current $P0_0$∼$P0_4$				−18	mA
$I_{OH(avg)}$	"H" average output current $P0_5$∼$P0_7$, $P1_0$∼$P1_7$				−18	mA
$I_{OH(avg)}$	"H" average output current $P4_0$∼$P4_7$, $P5_0$, $P5_1$				−12	mA
$I_{OH(avg)}$	"H" average output current $P6_0$∼$P6_5$				−1.5	mA
$I_{OL(avg)}$	"L" average output current $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P6_0$∼$P6_5$				10	mA
$I_{OL(avg)}$	"L" average output current $P6_0$∼$P6_5$				1.5	mA
$f_{(P3_2/CNTR)}$	Timer 3 counter clock input oscillation frequency (Note 3)	$f_{(X_{IN})}$=4.2MHz			500	kHz
		$f_{(X_{IN})}$=1MHz			100	kHz
$f_{(X_{IN})}$	Clock input oscillating frequency (Note 3, 4, 6)				4.2	MHz
$f_{(X_{CIN})}$	Clock oscillating frequency for clock function				500	kHz

Note 2 : High-level input voltage of up to +12V may be applied to permissible for ports $P2_0$∼$P2_7$, $P3_0$∼$P3_2$, $P3_4$∼$P3_7$, CNV_{SS}, $P5_2$ and $P5_3$.
3 : Oscillation frequency is at 50% duty cycle.
4 : When used in the low-speed mode, the timer clock input frequency should be $f_{(XIN)} < f_{(XIN)}/3$.
5 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are in period of 100ms.
6 : When external clock input is used, the timer clock input frequency should be $f_{(XCIN)} \leqq 50kHz$.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P6_0$~$P6_5$		I_{OH}=−0.5mA	V_{CC}−0.4			V
V_{OH}	"H" output voltage ϕ		I_{OH}=−2.5mA	V_{CC}−2			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$		I_{OH}=−18mA	V_{CC}−2			V
V_{OH}	"H" output voltage $P4_0$~$P4_7$, $P5_0$, $P5_1$		I_{OH}=−12mA	V_{CC}−2			V
V_{OL}	"L" output voltage $P2_0$~$P2_7$, $P3_0$~$P3_7$		I_{OL}=10mA			2	V
V_{OL}	"L" output voltage $P6_0$~$P6_5$		I_{OL}=0.5mA			0.4	V
V_{OL}	"L" output voltage ϕ		I_{OL}=2.5mA			2	V
$V_{T+}-V_{T-}$	Hysteresis $P5_2/INT_2$, $P5_3/INT_1$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$		When used as CNTR input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$		When used as CLK input	0.3		1	V
I_{IL}	"L" input current $P2_0$~$P2_7$, $P3_0$~$P3_7$		V_I=0V			−5	μA
I_{IL}	"L" input current $P6_0$~$P6_5$		V_I=0V			−5	μA
I_{IL}	"L" input current $P5_4$~$P5_7$		V_I=0V			−5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}		V_I=0V			−5	μA
I_{IL}	"L" input current $P5_2/INT_2$, $P5_3/INT_1$		V_I=0V			−5	μA
I_{IH}	"H" input current	$P2_0$~$P2_7$, $P3_0$~$P3_7$	V_I=5V			5	μA
		$P2_0$~$P2_7$, $P3_0$~$P3_2$, $P3_4$~$P3_7$	V_I=12V			12	μA
I_{IH}	"H" input current $P6_0$~$P6_5$		V_I=5V			5	μA
I_{IH}	"H" input current $P5_4$~$P5_7$		V_I=5V			5	μA
			V_I=12V			12	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}		V_I=5V			5	μA
I_{IH}	"H" input current $P5_2/INT_2$, $P5_3/INT_1$		V_I=5V			5	μA
			V_I=12V			12	μA
I_{LOAD}	"L" output current	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$	V_P=V_{CC}−36V, V_{OL}=V_{CC}	150	500	900	μA
I_{LEAK}		$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$	V_P=V_{CC}−38V, V_{OL}=V_{CC}−38V			30	μA
V_{RAM}	RAM retention voltage		at clock stop	2		5.5	V
I_{CC}	Supply current		Output pins open (output OFF) V_P=V_{CC}, V_P=V_{SS} Input and I/O pins all at V_{SS} X_{IN}=4MHz (system operation)		4	8	mA
			ditto (at comparator mode)		5	10	mA
			ditto (at wait mode)		1		mA
			X_{IN}−X_{OUT} stop X_{CIN}=32kHz (at system operation) all other conditions same as above.		60	200	μA
			ditto (at wait mode)		40		μA
			Oscillation all stopped. (at STOP mode) T_a=25℃			1	μA
			Oscillation all stopped. (at STOP mode) T_a=70℃			10	μA

COMPARATOR CHARACTERISTICS (V_{CC}=5V±10%, V_{CC}=0V, T_a=25°C, $f_{(X_{IN})}$=4MHz)

Parameter	Limits			Unit
	Min.	Typ.	Max.	
Resolution	—	—	(1/16)V_{CC}	V
Internal analog voltage error	—	—	±(1/16)V_{CC}	V
Analog input voltage	0	—	V_{CC}	V

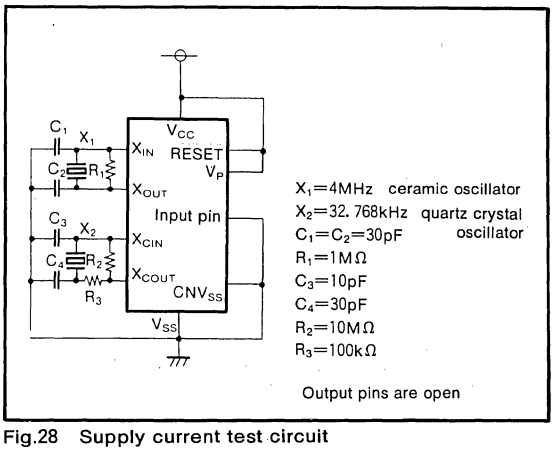


Fig.28 Supply current test circuit

TIMING REQUIREMENTS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(P5D-\phi)}$	Port $P5_2/INT_2$, $P5_3/INT_1$ input setup time	270			ns
$t_{su(P5D-\phi)}$	Port $P5_4$~$P5_7$ input setup time	270			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port $P5_2/INT_2$, $P5_3/INT_1$ input hold time	20			ns
$t_{h(\phi-P5D)}$	Port $P5_4$~$P5_7$ input hold time	50			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time	20			ns
$t_{C(X_{IN})}$	External clock input cycle time (X_{IN} input)	235			ns
$t_{W(X_{IN})}$	External clock input pulse width (X_{IN} input)	75			ns
$t_{C(X_{CIN})}$	External clock input cycle time (X_{CIN})	2.0			ms
$t_{W(X_{CIN})}$	External clock input pulse width (X_{CIN})	1.0			ms
t_r	External clock rise time			25	ns
t_f	External clock fall time			25	ns

Memory expanding mode and eva-chip mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Microprocessor mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25°C, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 30			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 29			230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time	Fig. 30			230	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time	Fig. 29			230	ns

Memory expanding mode and eva-chip mode

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25°C, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.29 Fig.30			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/\overline{W})}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-R/\overline{W}F)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns

Microprocessor mode (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = 25°C, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.29 Fig.30			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/\overline{W})}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

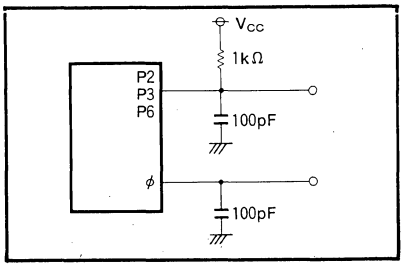


Fig.29 Port P2, P3, P6 test circuit

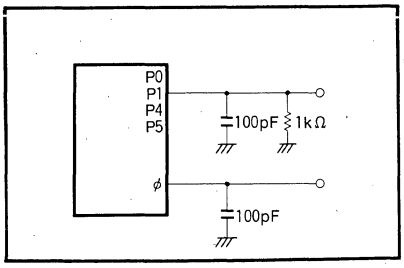
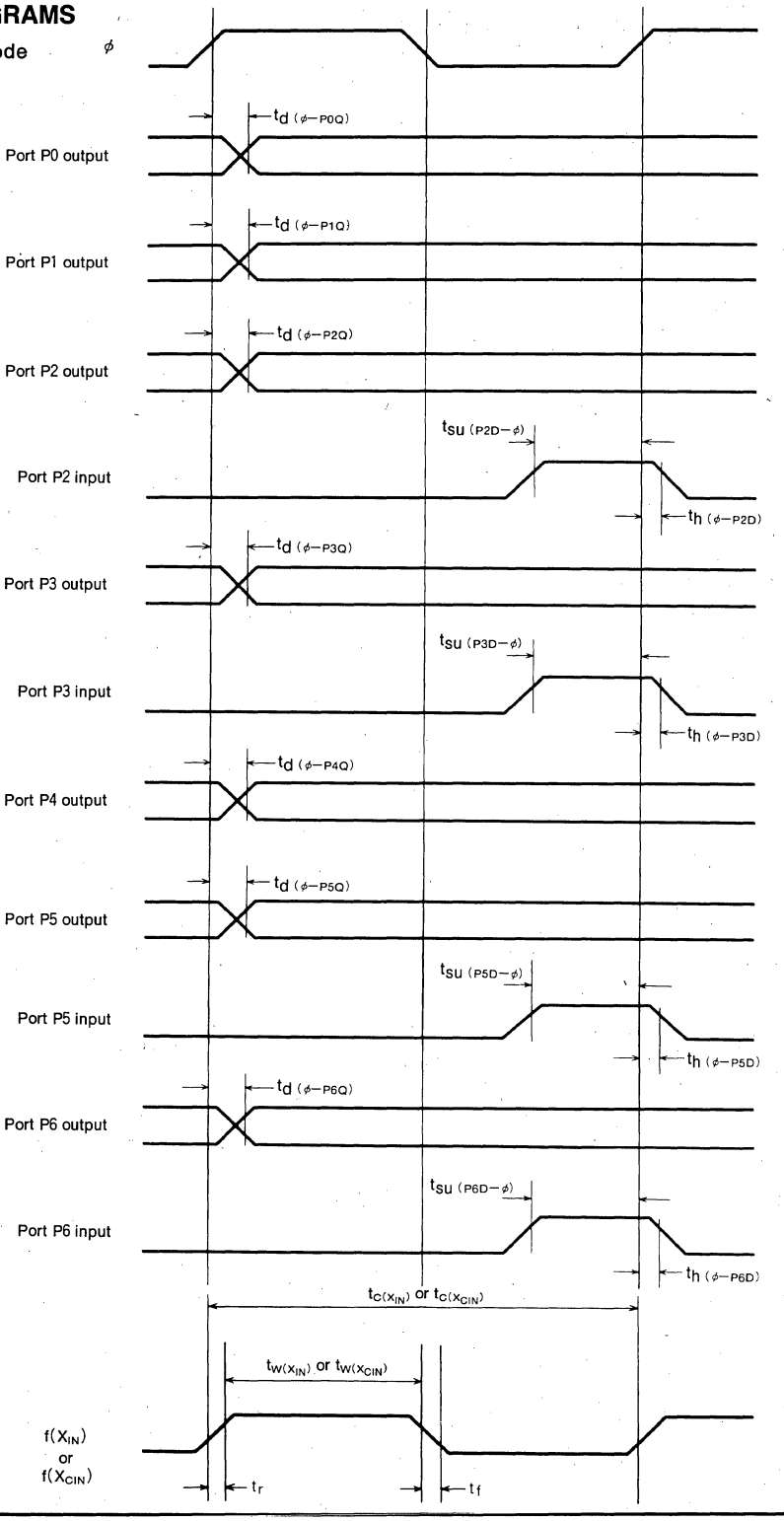


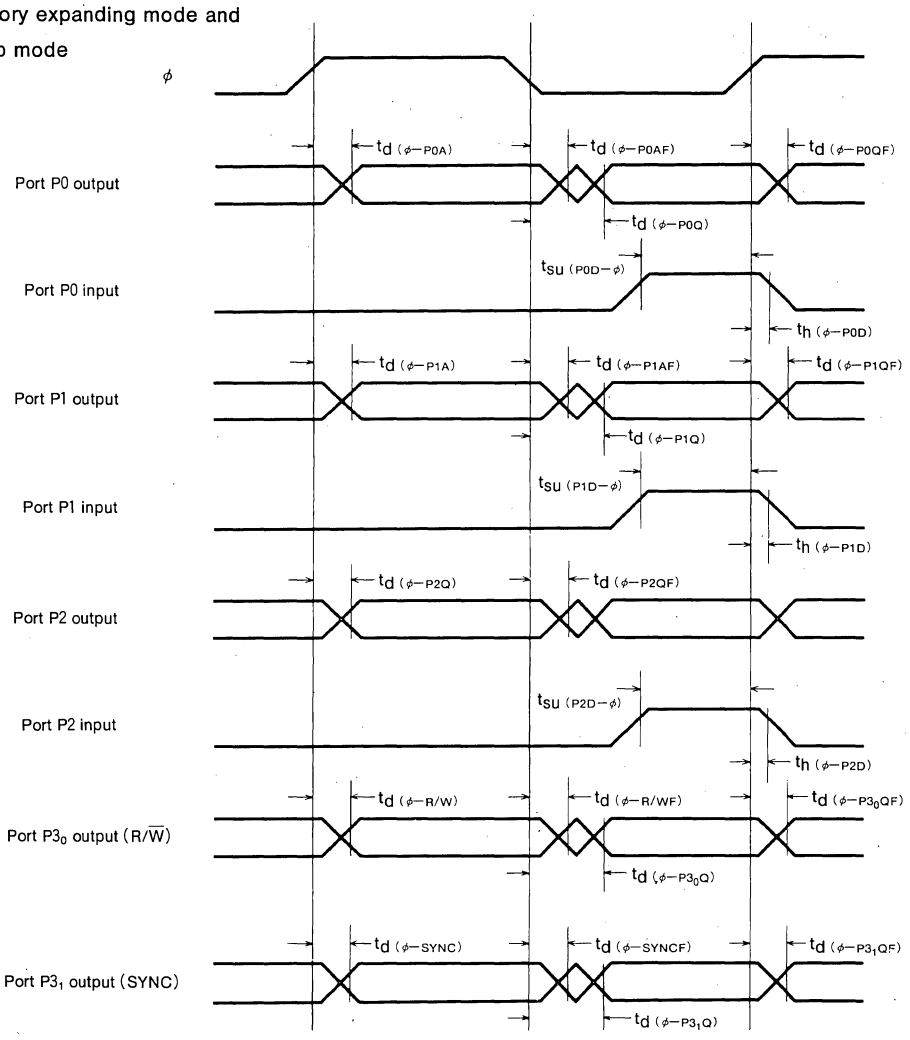
Fig.30 Port P0, P1, P4, P5 test circuit

TIMING DIAGRAMS

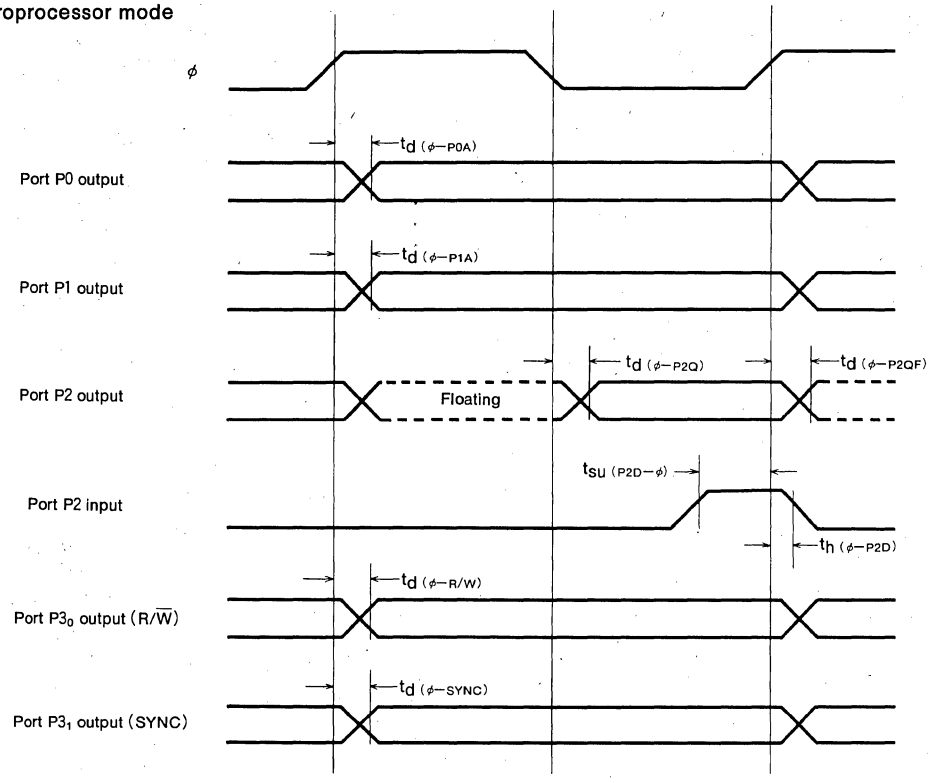
In single-chip mode



In memory expanding mode and Eva-chip mode



In microprocessor mode



M50964-XXXSP/FP
M50963-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50964-XXXSP and the M50963-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 64-pin shrink plastic molded DIP (flat package type also available).

These single-chip microcomputers are useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50964-XXXSP and the M50963-XXXSP are noted below. The following explanations apply to the M50964-XXXSP.

Specification variations for other chips are noted accordingly.

The differences between the M50964-XXXSP and the M50964-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

Type name	ROM size
M50964-XXXSP	6144bytes
M50963-XXXSP	10240bytes

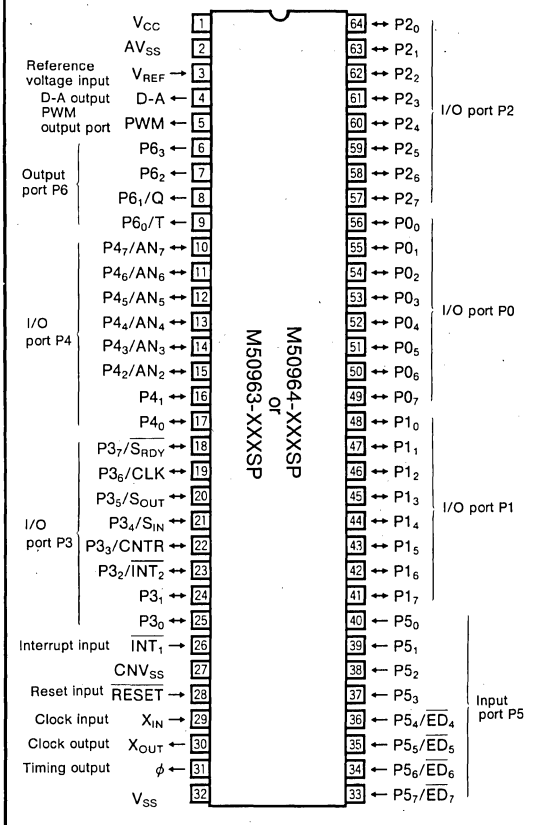
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 6144 bytes (M50964-XXXSP)
  10240 bytes (M50963-XXXSP)
  RAM ..... 160 bytes
- Instruction execution time
  ..... 2μs (minimum instructions, at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz ..... 5V$\pm$10%
- Power dissipation
  normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting ..... 80 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer 4
- Programmable I/O ports (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Output ports (Port P6) 4
- Serial I/O (8-bit) 1
- A-D converter ..... 8-bit successive approximation
- D-A converter
- 8-bit PWM function
- Watchdog timer

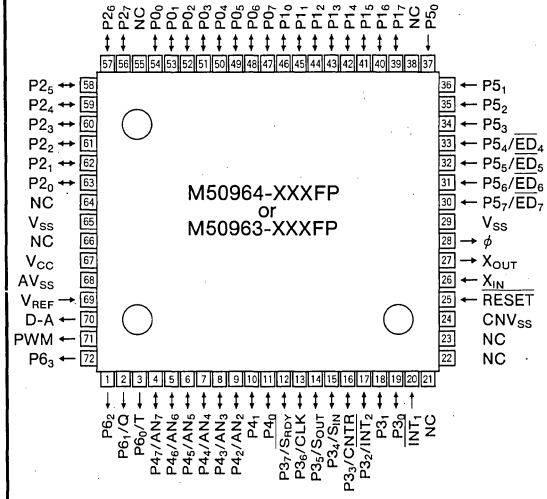
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)

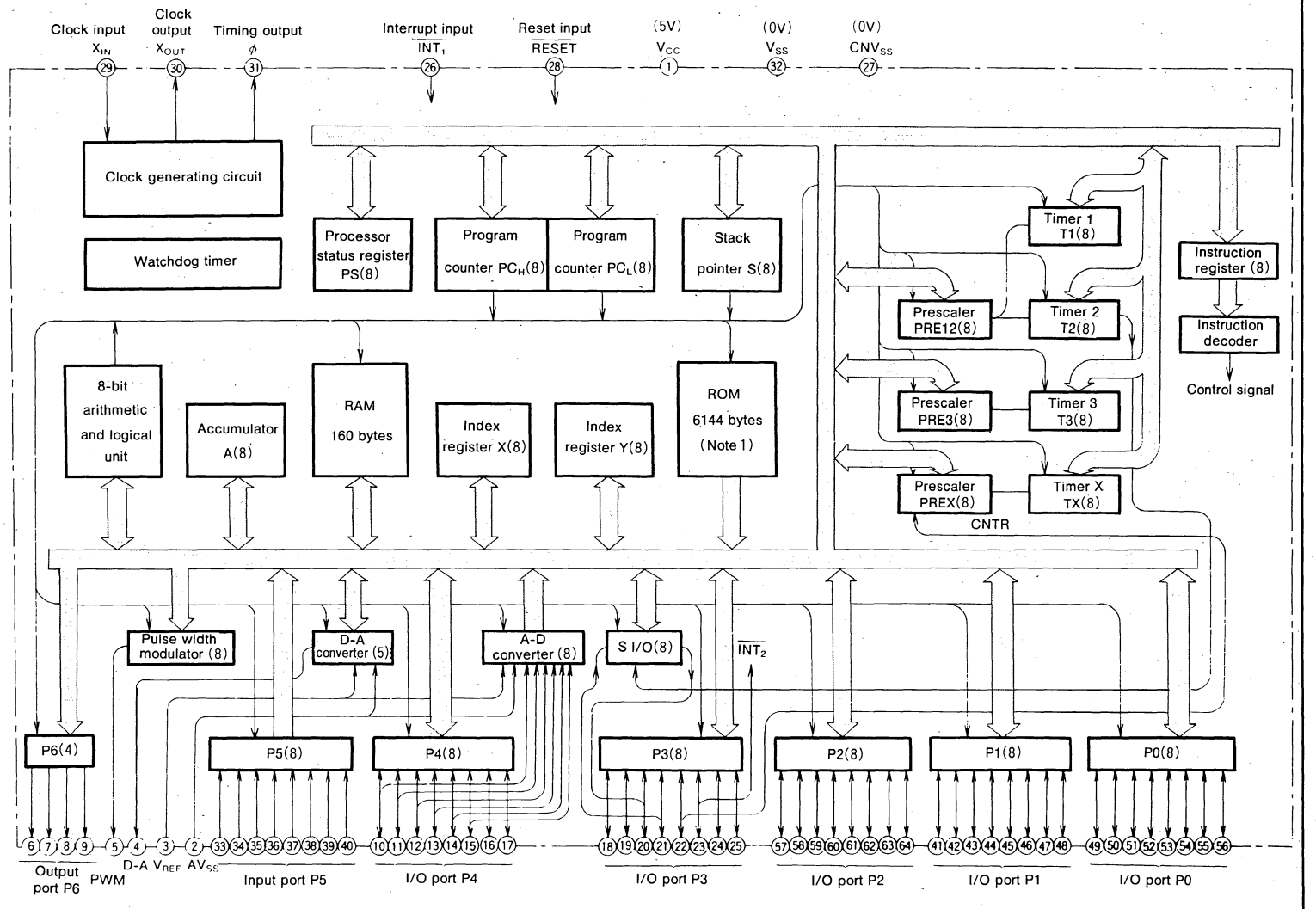


Outline 64P4B



Outline 72P6 NC : No connection

M50964-XXXSP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONS OF M50964-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory size	ROM		6144bytes
	RAM		160bytes
Input/Output ports	$\overline{INT_1}$	Input	1-bit×1
	P0, P1, P2, P3, P4	I/O	8-bit×5 (a part of P3 is common with serial I/O, timer I/O, and interrupt input)
	P5	Input	8-bit×1
	P6	Output	4-bit×1 (a part of P6 is in common with external trigger output pin)
Serial I/O			8-bit×1
Timers			8-bit prescaler×3+8-bit timer×4
A-D conversion			8-bit×1 (6 channels)
D-A conversion			5-bit×1
Pulse width modulator			8-bit×1
Watchdog timer			15-bit×1
Subroutine nesting			80 levels (max)
Interrupts			Two external interrupts, Three internal timer interrupts
Clock generating circuit			Built-in (ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	at high-speed operation		15mW (at 4MHz frequency)
Input/Output characteristics	Input/Output voltage		12V (Ports P0, P1, P3, P4, P5, P6, $\overline{INT_1}$)
	Output current		5mA (Ports P0, P1, P2, P3, P4)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M50964-XXXSP/M50963-XXXSP		64-pin shrink plastic molded DIP
	M50964-XXXFP/M50963-XXXFP		72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
AV_{SS}	Voltage input for A-D and A-D		This is GND input pin for the A-D and D-A converters.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D and D-A converters.
D-A	D-A output	Output	This is output pin from the D-A converter.
PWM	PWM output	Output	This is output pin from the pulse width modulator. The output structure is N-channel open drain.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open drain.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest interrupt input pin ($\overline{INT_2}$), respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. $P4_2$~$P4_7$ work as analog input port AN_2~AN_7.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port. $P5_4$~$P5_7$ can be used as the edge sense inputs.
$P6_0$~$P6_3$	Output port P6	Output	Port P6 is an 4-bit Output port. At external trigger output mode, $P6_0$ and $P6_1$ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively. The output structure is N-channel open drain.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M50964-XXXSP is shown in Figure 1. Addresses $E800_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 6144 bytes (Address $D800_{16}$ to $FFFF_{16}$ are assigned for the built-in ROM area which consists of 10240 bytes for M50963-XXXSP).

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $FFF4_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $009F_{16}$ are assigned to the built-in RAM and consist of 160 bytes of static RAM. In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.

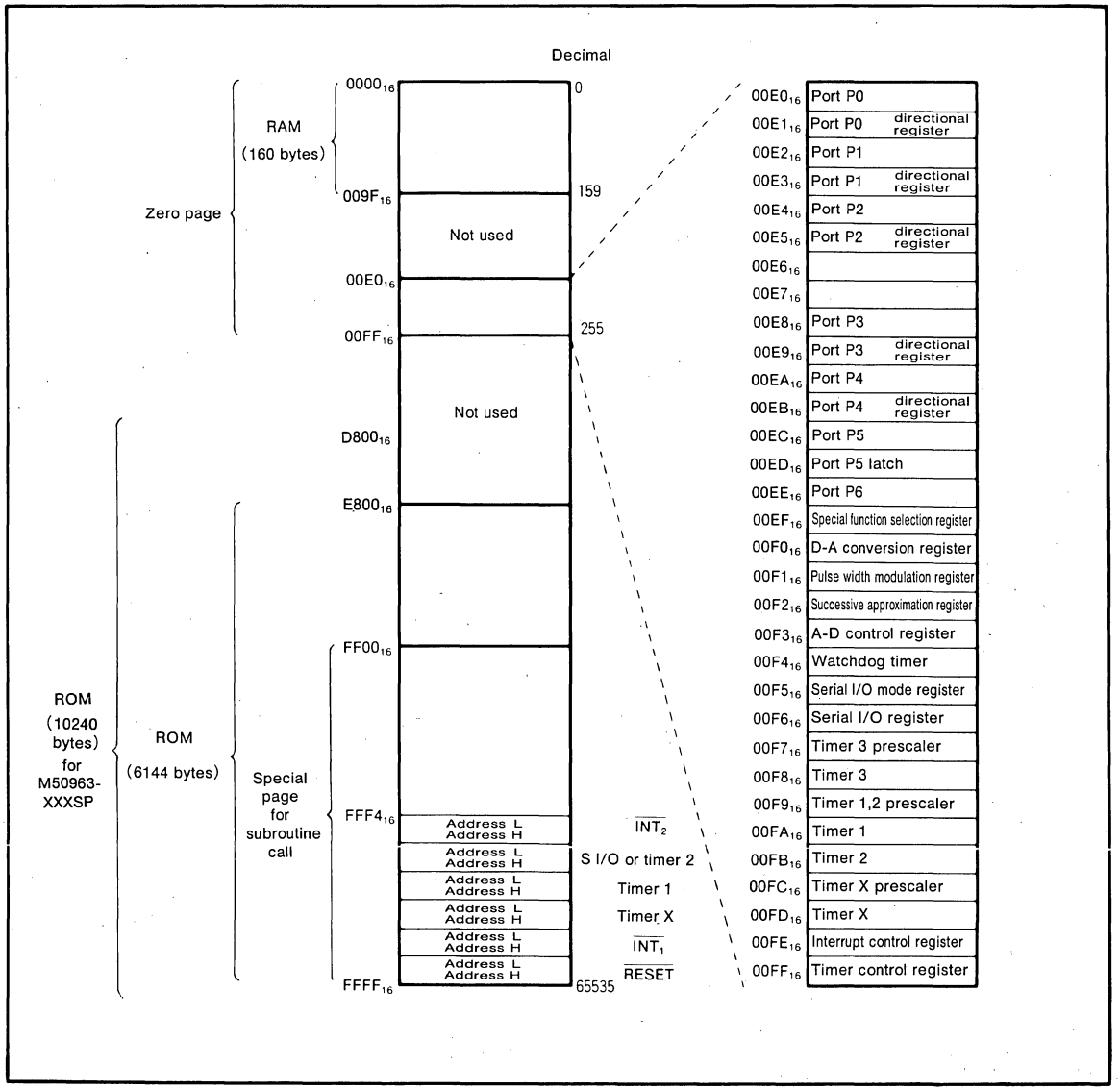


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

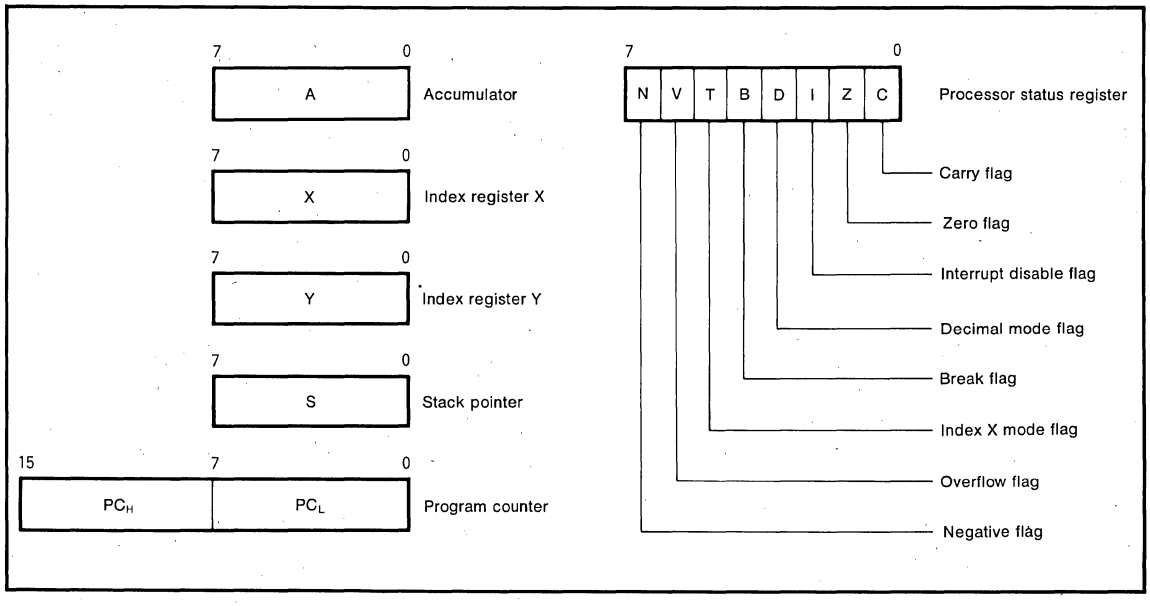


Fig.2 Register structure

STACK POINTER (S)

The stack pointer (S) is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

The location of the stack can be determined by the stack page bit (bit 4 at address $00FF_{16}$). When bit 4 is "0" and the contents of the stack pointer is XX_{16}, the stack address is set to $00XX_{16}$. When bit 4 is "1", the stack address is set to $01XX_{16}$. When using this microcomputer in the single-chip mode, the stack page bit must be "0" and the stack pointer should be set at the bottom address of the internal RAM.

When an interrupt occurs, the higher 8 bits of the program counter are pushed into the stack first, and then the lower 8 bits of the program counter are pushed into the stack. After each byte is pushed into the stack, the stack pointer is decremented by one. Next, the contents of the processor status register are pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter are processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed into the stack automatically. A Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed (pulled) to (from) the stack with the PHP and PLP instructions, respectively. Only the program counter is pushed into the stack during a subroutine call. Therefore, any registers that should not be destroyed should be pushed into the stack manually. The RTS instruction is used to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{\text{INT}_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1	4	$FFF9_{16}$, $FFF8_{16}$
Timer 2 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{\text{INT}_2}$ (BRK)	6	$FFF5_{16}$, $FFF4_{16}$

INTERRUPT

The M50964-XXXSP can be interrupted from seven sources; $\overline{\text{INT}_1}$, timer X, timer 1, timer 2/serial I/O, or $\overline{\text{INT}_2}$/BRK instruction.

However, the $\overline{\text{INT}_2}$ pin is used with port $P3_2$ and the corresponding directional register bit should be set to "0" when $P3_2$ is used as an interrupt input pin.

The value of bit 2 of the serial I/O mode register (address $00F6_{16}$) determine whether the interrupt is from timer 2 or from serial I/O. When bit 2 is "0" the interrupt is from timer 2, and when bit 2 is "1" the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, (as discussed in the stack pointer section) the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag I is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure

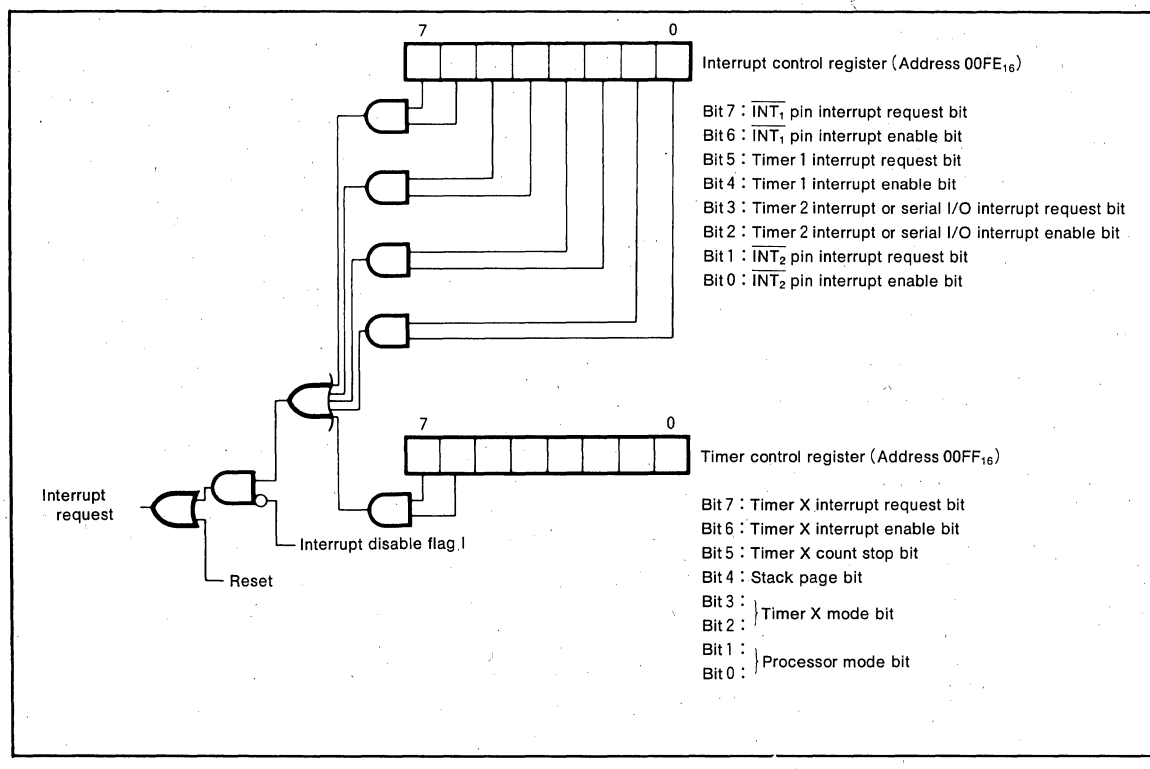


Fig.3 Interrupt control

3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"

(2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

TIMER

The M50964-XXXSP has three timers; timer X, timer 1, timer 2 and timer 3. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section). Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1, timer 2 and timer 3 is shown in Figure 4.

The $P3_3$/CNTR pin cannot be used as CNTR when $P3_3$ is being used in the normal I/O mode.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All four timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see Interrupt section). The prescaler latch and timer latch can be loaded with any number.

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock source.

(4) Pulse width measurement mode [11]
This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

The function of timer 3 is as same as that of timer 1 and timer 2, with the exception that the detection of its overflow is known by the overflow bit (bit 3 of address $00EF_{16}$). When the timer down-counts to zero, the overflow bit is set to "1" and the contents of the timer's latch is reloaded into the timer.

The reset of the overflow bit is made by;

a) hard ware reset

b) write "0" to overflow bit

c) write instruction to timer 3

The structure of special function selection register is shown in Figure 6.

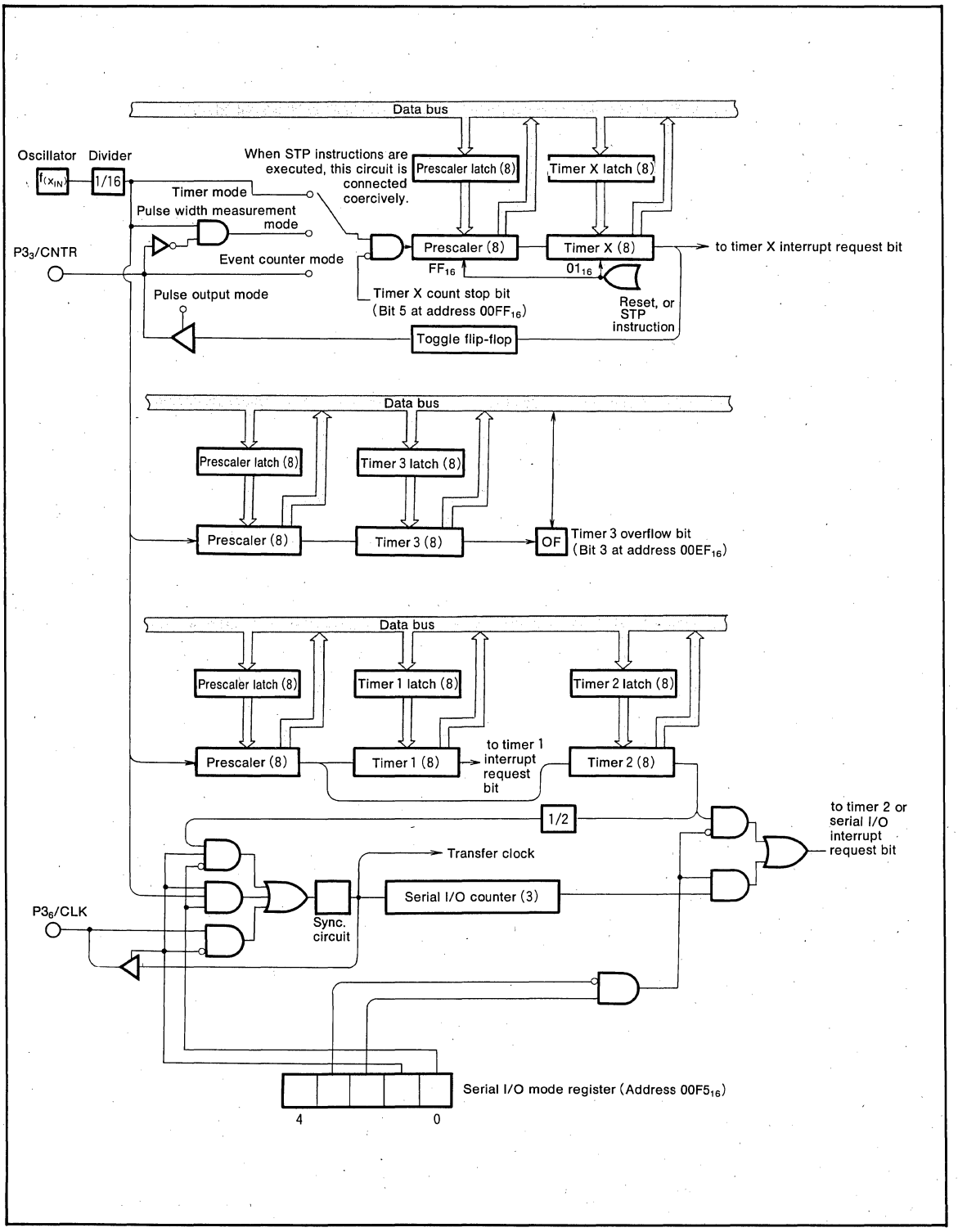


Fig.4 Block diagram of timer X, timer 1, timer 2, and timer 3

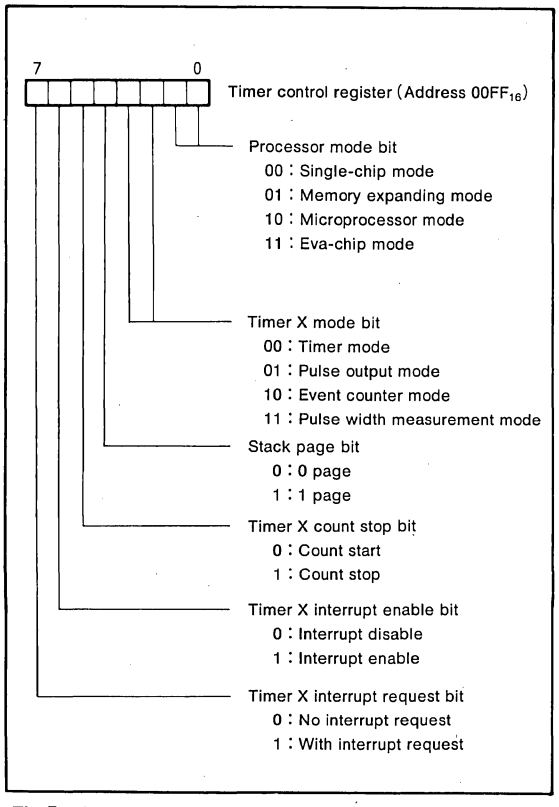


Fig.5 Structure of timer control register

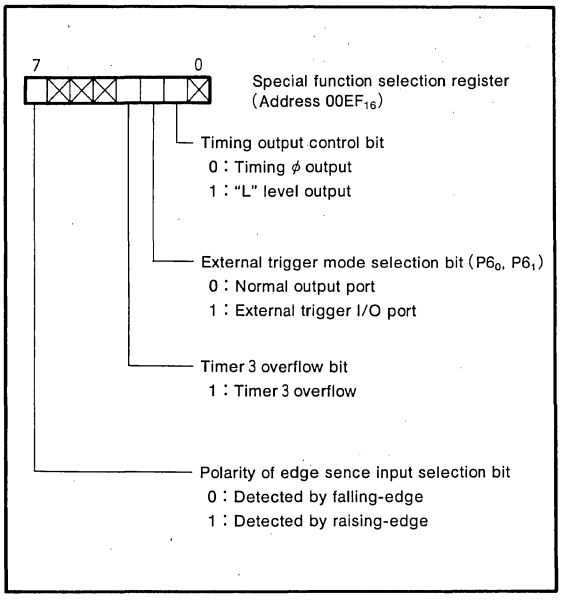


Fig.6 Structure of special function selection register

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 7.

In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input /output clock (CLK), and the serial I/O pins (S_{OUT}, S_{IN}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F5_{16}$) is a 5-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 2, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the oscillator frequency divided by 16, becomes the clock.

Bit 2 to 4 decide whether parts of P3 will be used as a serial I/O or not. When bit 3 is "0" and bit 2 is "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

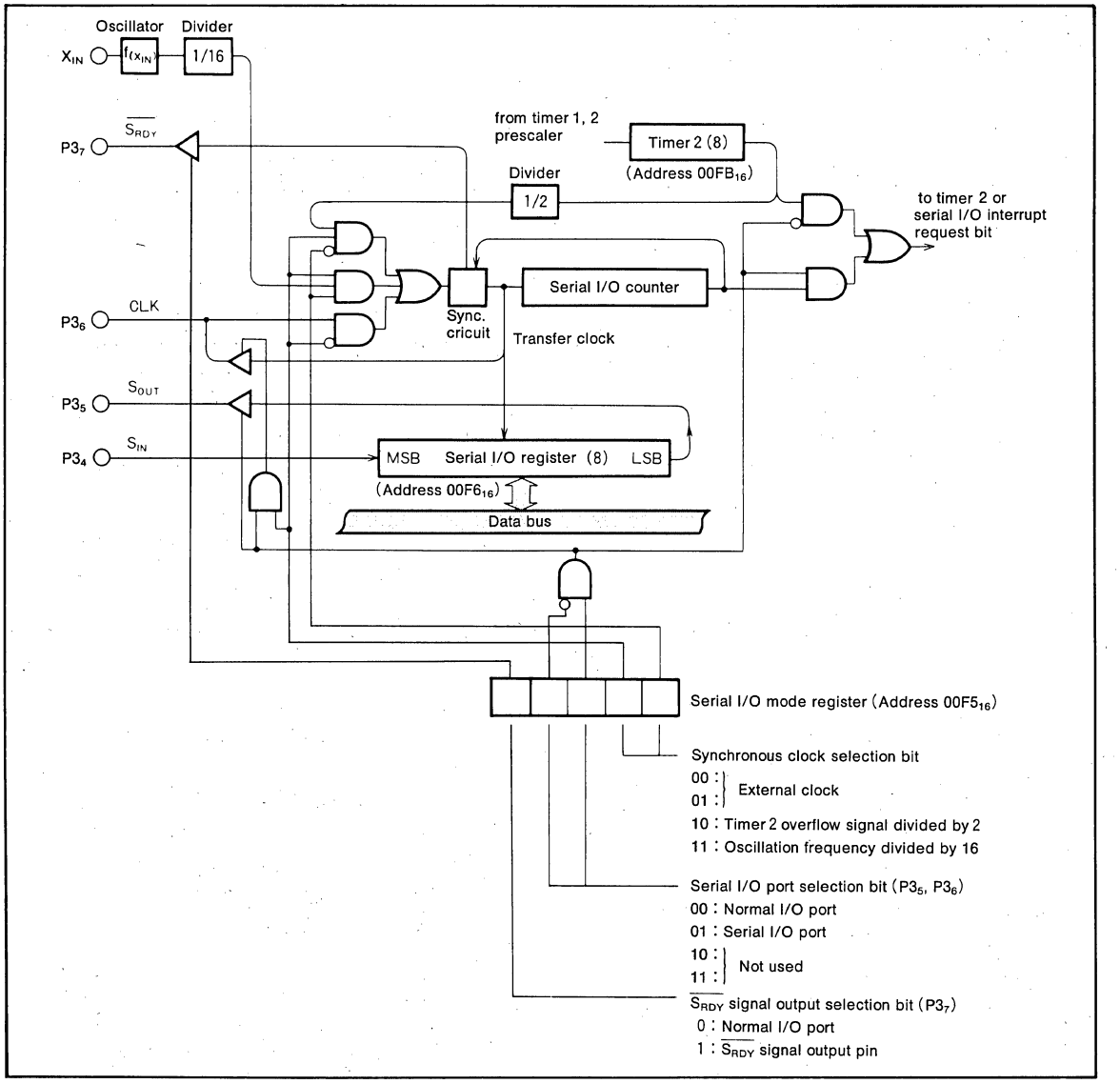


Fig.7 Block diagram of serial I/O

To use the serial I/O, bit 3 and bit 2 need to be set to "01", if they are "00" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 2. Bit 4 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 4=1, $\overline{S_{RDY}}$) or used as normal I/O pin (bit 4=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address $00F7_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M50964-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrpt request bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 8. An example of communication between two M50964-XXXSPs is shown in Figure 9.

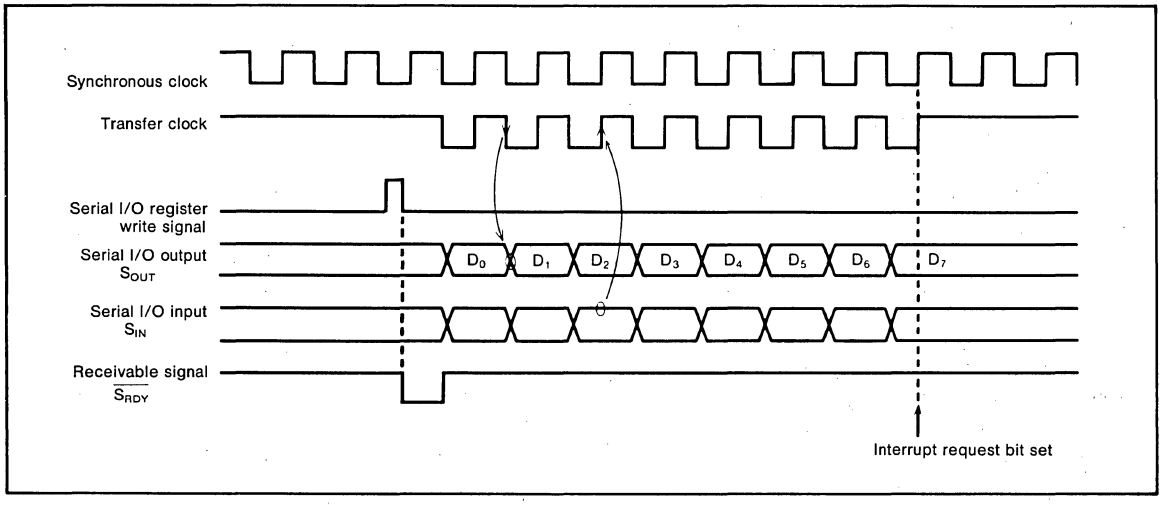


Fig.8 Serial I/O timing

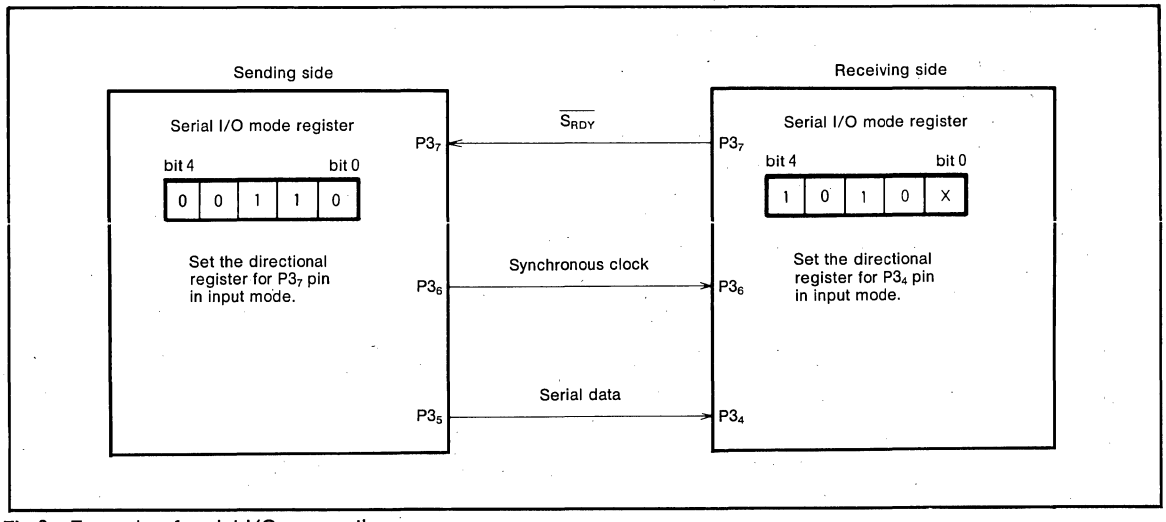


Fig.9 Example of serial I/O connection

A-D CONVERTER

An 8-bit successive approximation method of A-D conversion is employed providing a precision of ±3LSB. A block diagram of the A-D convertor is shown in Figure 10. Conversion is automatic once it is started with the program.

The six analog inputs are used in common with pins $P4_7$, $P4_6$, $P4_5$, $P4_4$, $P4_3$, and $P4_2$ of port 4. Bits 1 and 0 of the A-D control register (address $00F3_{16}$) are used to select which pins are used for A-D conversion. The input condition is accomplished by setting to "0" the bit in the directional register that corresponds to the pin where A-D conversion is to take place. Bit 4 of the A-D control register is the A-D conversion end bit. During A-D conversion, this bit is "0", and upon completion becomes "1". Thus, it can be ascertained whether or not A-D conversion has been completed or not by inspecting this bit. The relation between the contents of the A-D control register and the selection of input pins are shown in Figure 11.

The results of the conversion can be found be reading the contents of the successive approximation register address $00F2_{16}$ which stores the results of the conversion. The procedure for executing A-D conversion is next explained. Firstly, the pin that is to be used for the A-D conversion is selected by setting bit 1 and bit 0 of the A-D control register. Next, the successive approximation is written to upon which the A-D conversion starts. Since actual data is not written to the successive approximation, any type of may be written. Simultaneous with its being written, the A-D conversion end bit (bit 4 of address $00F3_{16}$) is cleared to "0" signifying that A-D conversion operations are being conducted. A-D conversion completes after 198 clock cycles upon which the A-D conversion end bit is set to "1" and the results of the conversion can be found in the successive approximation register. Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed larger than 1MHz during A-D conversion.

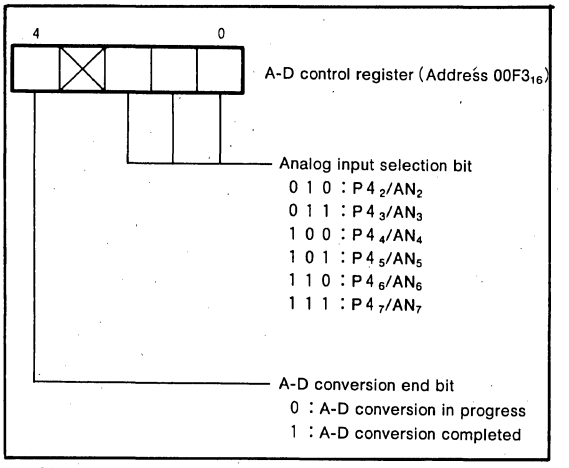


Fig.11 Structure of A-D control register

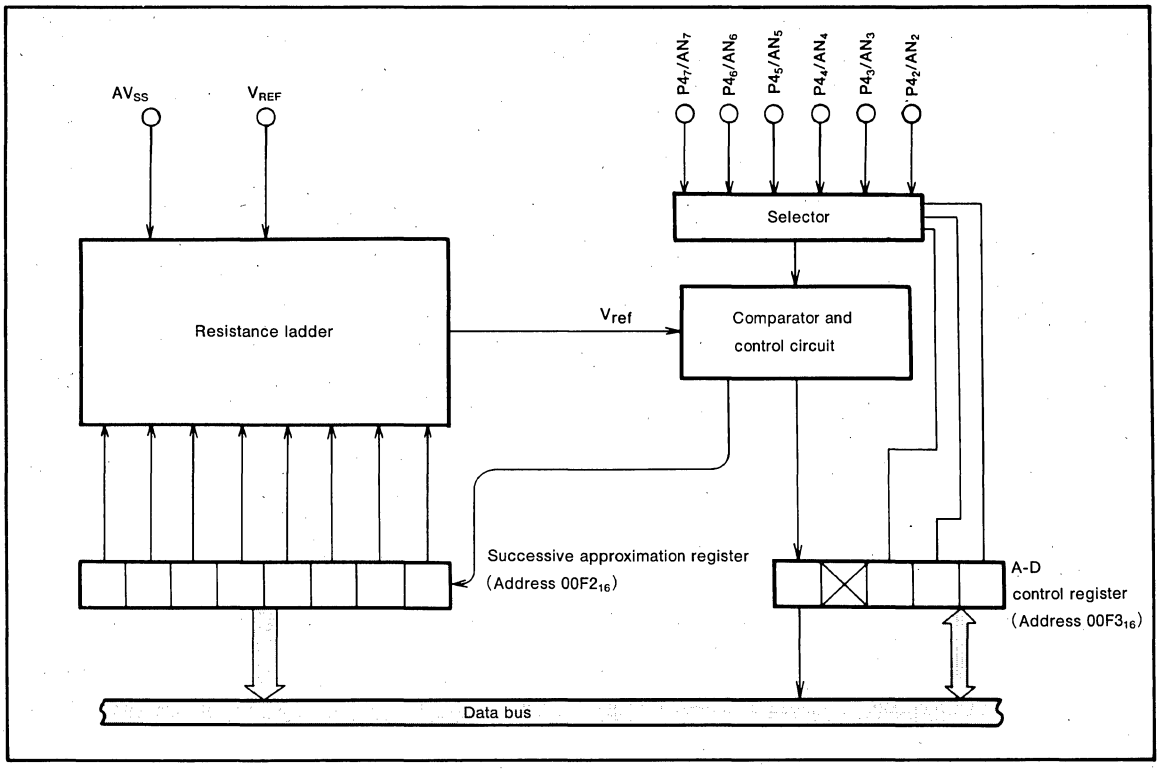


Fig.10 Block diagram of A-D converter

D-A CONVERTER

The R-2R method is used for D-A conversion. The block diagram is shown in Figure 12. An analog voltage is output that corresponds to the contents of the D-A conversion register (address $00F0_{16}$). Ideally, the relation of the analog output voltage V and the contents (n) of the D-A conversion register is $V=V_{REF} \times n/32 (n=0 \sim 31)$.

Reset operation clears the content n of the D-A conversion register to 0_{16}.

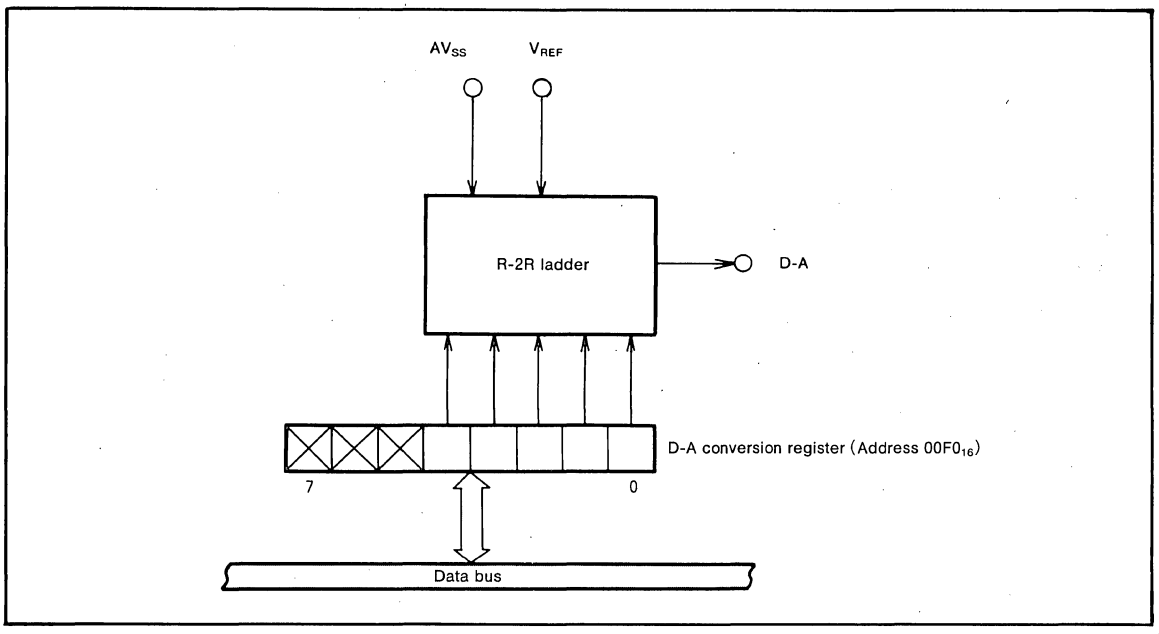


Fig.12 Block diagram of D-A converter

PULSE WIDTH MODULATOR

The pulse width modulation register (address $00F1_{16}$) is configured of an 8-bit counter. The period of repetition is 4080 clock cycles. With the content of the pulse width modulation register m, the PWM pin becomes high-level for the period of 4080 × m/255 (m=0~255). Figure 13 shows that relationship. An N-channel open drain output is used for the PWM pin.

Reset sets the content m of the pulse width modulation register to 00_{16}.

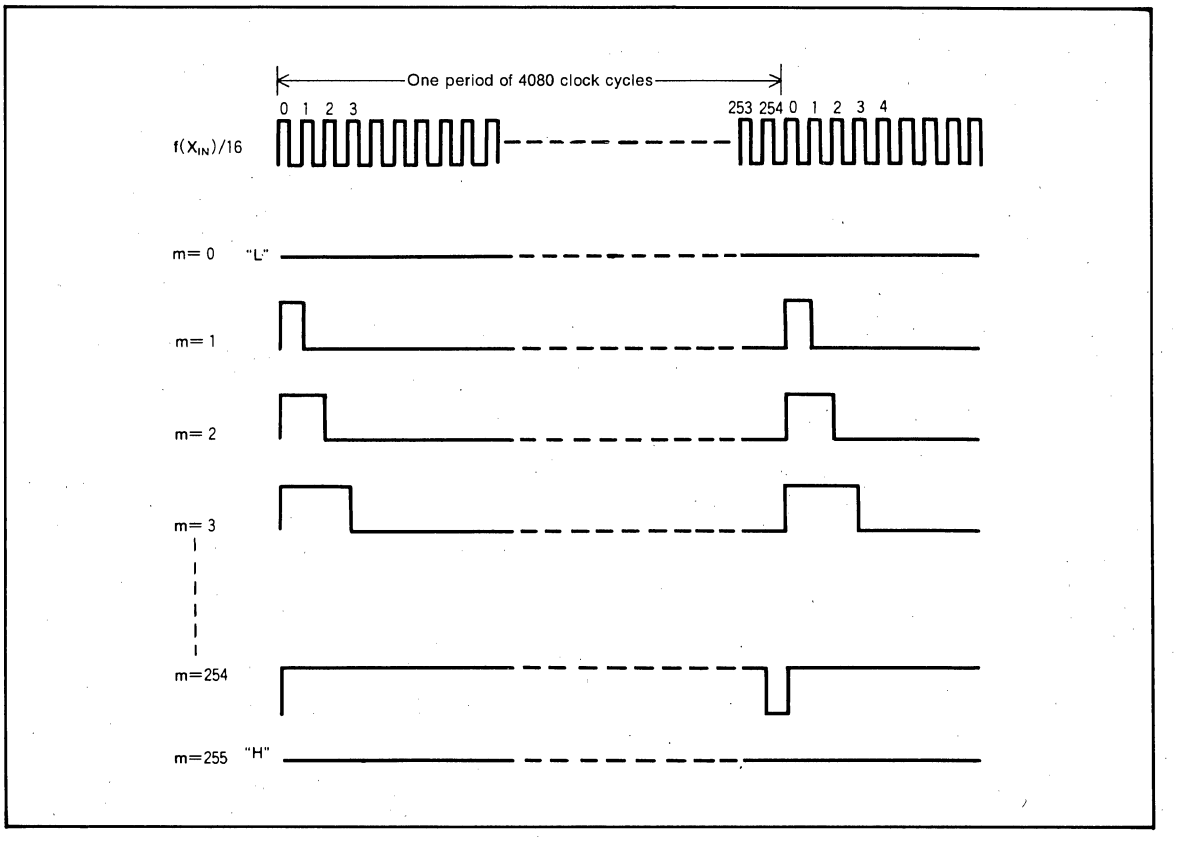


Fig.13 Relation between m and PWM output

WATCHDOG TIMER

The watchdog timer provides the means to return to a reset condition when a program runs wild and the program will not run the normal loops.

The watchdog timer (address $00F4_{16}$) is a 15-bit counter. The watchdog timer counts 1/16th the output frequency of the oscillator. The watchdog timer is set to $7FFF_{16}$ when a reset is accomplished a write operation has been made to it. As well as any of the instructions that generate a write signal, such as STA, LDM, and CLB, can be used to write data to the watchdog timer. An output of the most significant bits of the watchdog timer is input to the reset circuit. When 262144 clock cycles have been counted, the most significant bit becomes "0" and reset is carried out. When reset is carried out, the watchdog timer is set to $7FFF_{16}$ and reset is released. The program then begins again from reset vector address. Normally, the program is written so that a writing operation is made to the watchdog timer prior to the most significant bit's becoming "0". Application of a +10V to the $\overline{\text{RESET}}$ pin will disable the watchdog timer function.

Since execution of the STP instruction causes both the clock and the watchdog timer to stop, an option is offered where the STP instruciotn can be disabled.

RESET CIRCUIT

The M50964-XXXSP is reset according to the sequence shown in Figure 14. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 15.

An example of the reset circuit is shown in Figure 16.

When the power on reset is used, the $\overline{\text{RESET}}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

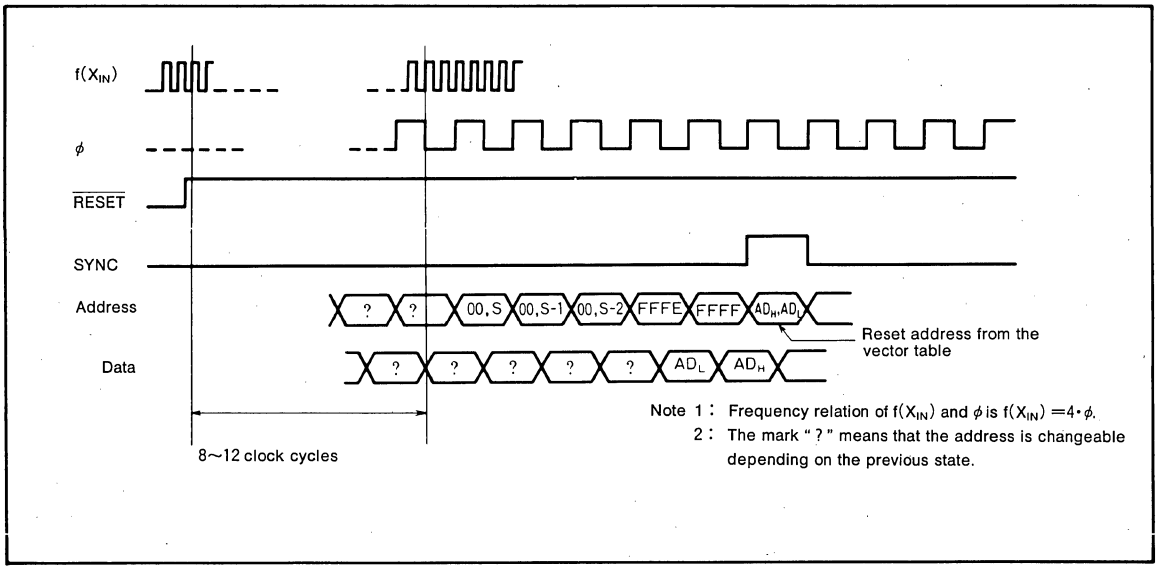


Fig.14 Timing diagram at reset

	Address	
(1) Port P0 directional register	($E1_{16}$) ···	00_{16}
(2) Port P1 directional register	($E3_{16}$) ···	00_{16}
(3) Port P2 directional register	($E5_{16}$) ···	00_{16}
(4) Port P3 directional register	($E9_{16}$) ···	00_{16}
(5) Port P4 directional register	(EB_{16}) ···	00_{16}
(6) Port P6	(EE_{16}) ···	FF_{16}
(7) Special function selection register	(EF_{16}) ···	0XXX000X
(8) D-A conversion register	($F0_{16}$) ···	00000
(9) Pulse width modulation register	($F1_{16}$) ···	00_{16}
(10) Watchdog timer	($F4_{16}$) ···	$7FFF_{16}$
(11) Serial I/O mode register	($F5_{16}$) ···	00000
(12) Prescaler X	(FC_{16}) ···	FF_{16}
(13) Timer X	(FD_{16}) ···	01_{16}
(14) Interrupt control register	(FE_{16}) ···	00_{16}
(15) Timer control register	(FF_{16}) ···	00_{16}
(16) Interrupt disable flag on processor status register	(PS) ···	1
(17) Program counter	(PC_H) ···	Contents of address $FFFF_{16}$
	(PC_L) ···	Contents of address $FFFE_{16}$

Note 1 : Port P6 is the high-impedance state during reset.
After return from reset, it is "FF_{16}".

Fig.15 Internal state of microcomputer at reset

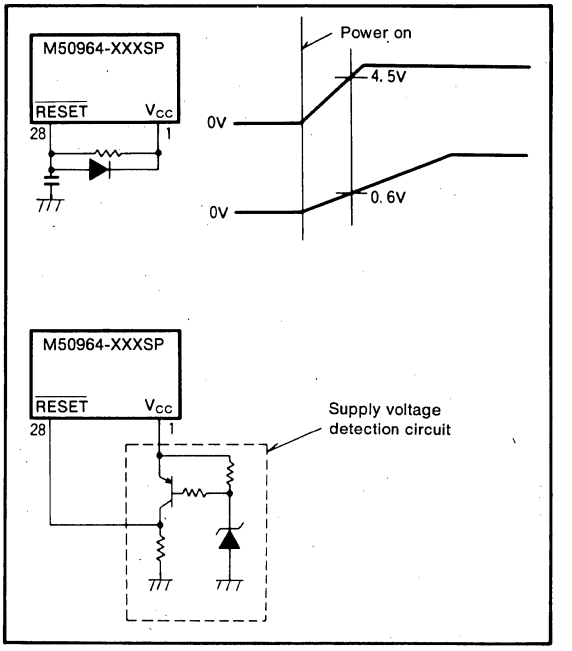


Fig.16 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1

In the single-chip mode, port P1 has the same function as P0, but it has CMOS output. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2

In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.

For more details, see the processor mode information.

(4) Port P3

In the single-chip mode, port P3 has the same function as P0. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as serial I/O, $\overline{INT_2}$ and I/O pins for timer X. For more details, see the processor mode information.

(5) Port P4

Port P4 has the same function as port P0 in the single-chip mode. But $P4_7$ through $P4_2$ can also be used as analog input pins AN_7 through AN_2.

(6) Port P5

Port P5 is an input port. $P5_4$ through $P5_7$ can also be used as edge sence inputs. In such a case, reading is begun from $00ED_{16}$. $00ED_{16}$ is provided with a latch which is set to "1" when the input changes from high-level to low-level.

And for $P5_7$, polarity of input edge can be selected by polarity of edge sense input selection bit (bit 7 of address $00EF_{16}$).

When this bit is set to "0", its latch is set to "1" at the input level goes to "L" from "H". When this bit is set to "1", its latch is set to "1" at the input level goes to "H" from "L". At the reset state, this bit is set to "0".

When content of polarity of edge sense input selection bit was set by program, the latch (bit 7 of address $00ED_{16}$) must be reset once.

The input pulse width must be at least 7 clock cycles wide. The latch is reset by using such instructions as LDM and CLB to write a "0" to the latch. When $00ED_{16}$ is read, the lower order 4 bits are always zero.

When port P5 is used as level sense input, read the contents of the address $00EC_{16}$.

(7) Port P6

Port P6 is a 4-bit output port. It has N-channel open drain output. $P6_0$ and $P6_1$ can be used as external trigger I/O pins, when external trigger mode selection bit (bit 2 of address $00EF_{16}$) is set to "1". In this case, $P6_0$ and $P6_1$ are trigger clock input pin and trigger output pin, respectively. Using external trigger mode, $P6_0$'s latch must be set to "1" in order to off the output transistor. In external trigger mode, the content of $P6_1$'s latch is output to pin when the rising or falling edge is input to $P6_0$ pin.

When external trigger mode selection bit is set to "0", $P6_0$ and $P6_1$ are normal output ports. At the reset state, this bit is set to "0".

See Figure 17 for more details.

(8) Clock ϕ output pin

In normal conditions, the oscillator frequency divided by four is output as ϕ. The timing output ϕ is fixed "L" state when the timing output control bit (bit 1 of address $00EF_{16}$) is set to "1". But in this case, except the timing output is active. The timing output ϕ is output again when the timing output control bit is set to "0". At reset state this bit is set to "0".

(9) $\overline{INT_1}$ pin

The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

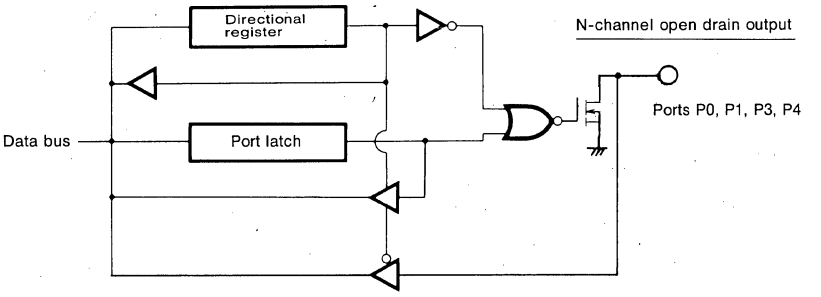
(10) $\overline{INT_2}$ pin ($P3_2/\overline{INT_2}$ pin)

The $\overline{INT_2}$ pin is an interrupt input pin used with $P3_2$. To use this pin as an interrupt pin, set the corresponding bit in the directional register to input ("0"). When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1".

(11) CNTR pin ($P3_3$/CNTR pin)

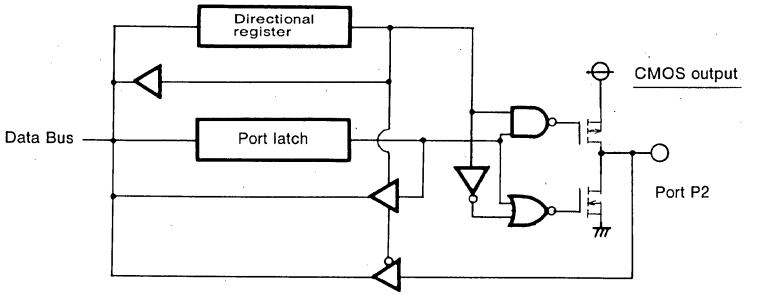
The $P3_3$/CNTR pin is an I/O pin of timer X. To use this pin as the timer X input pin, set the corresponding directional register bit to input ("0"). In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

Ports P0, P1, P3, P4

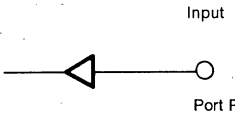


Note 1 : Port P3 can be also used as I/O pin of serial I/O, timer I/O, and interrupt input.
Port P4 can be also used as analog input.

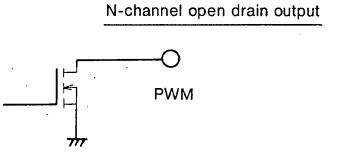
Ports P2



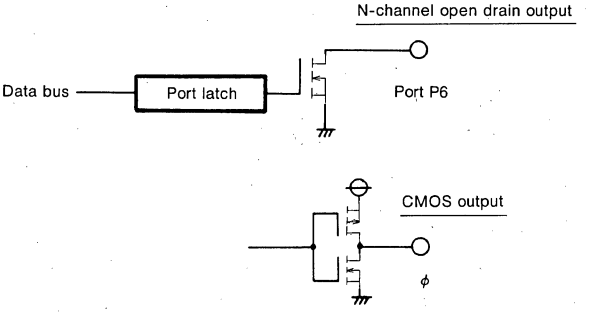
Port P5



PWM



Port P6



ϕ

Fig.17 Block diagram of ports P0~P6 (single-chip mode), and output format of ϕ.

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 19 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 18.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

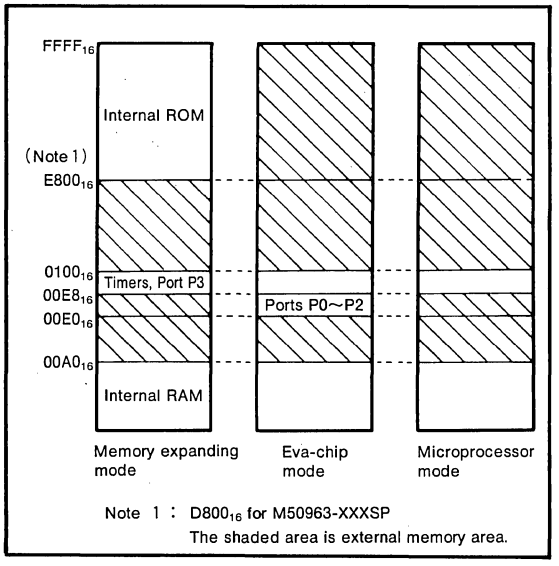


Fig.18 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost. P2 becomes the data bus (D_7～D_0) and loses its normal I/O functions. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode. With the exceptions that the internal ROM is disabled and that external memory must be attached in this mode, this mode is the same as the memory expanding mode.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is requierd.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original I/O functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

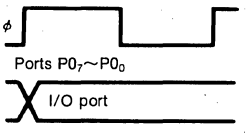
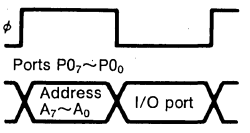
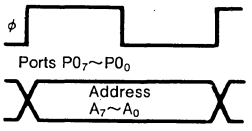
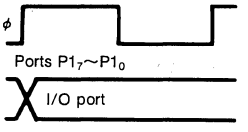
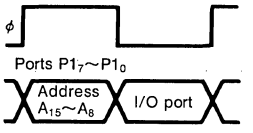
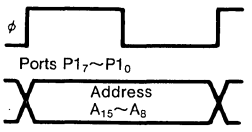
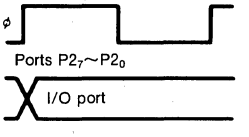
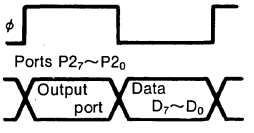
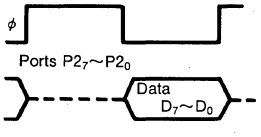
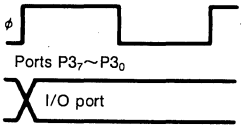
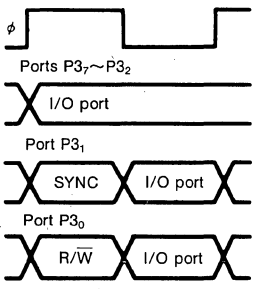
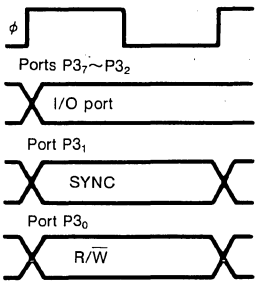
Port \ Mode	Single-chip mode (CM_1=0, CM_0=0)	Eva-chip mode (CM_1=1, CM_0=1)	Memory expanding mode (CM_1=0, CM_0=1)	Microprocessor mode (CM_1=1, CM_0=0)
Port P0				Same as left
Port P1				Same as left
Port P2				Same as left
Port P3				Same as left

Fig.19 Processor mode and functions of ports P0~P3

Table 2 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset. Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 22.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleared when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 20.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 21. X_{IN} is the input, and X_{OUT} is open.

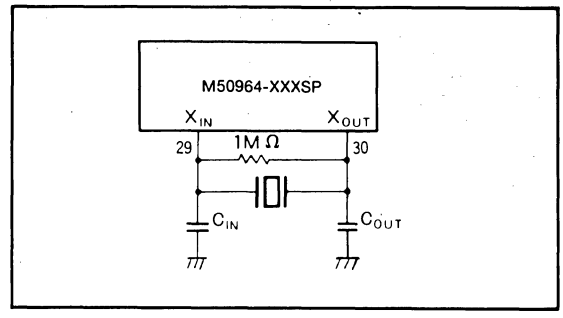


Fig.20 External ceramic resonator circuit

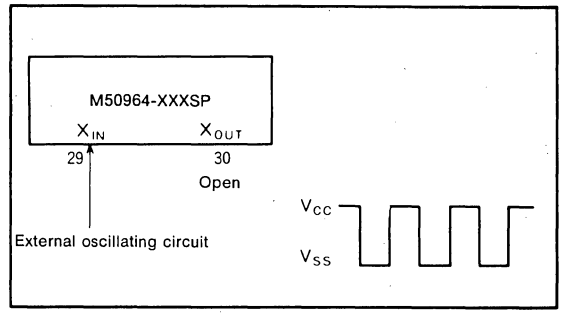


Fig.21 External clock input circuit

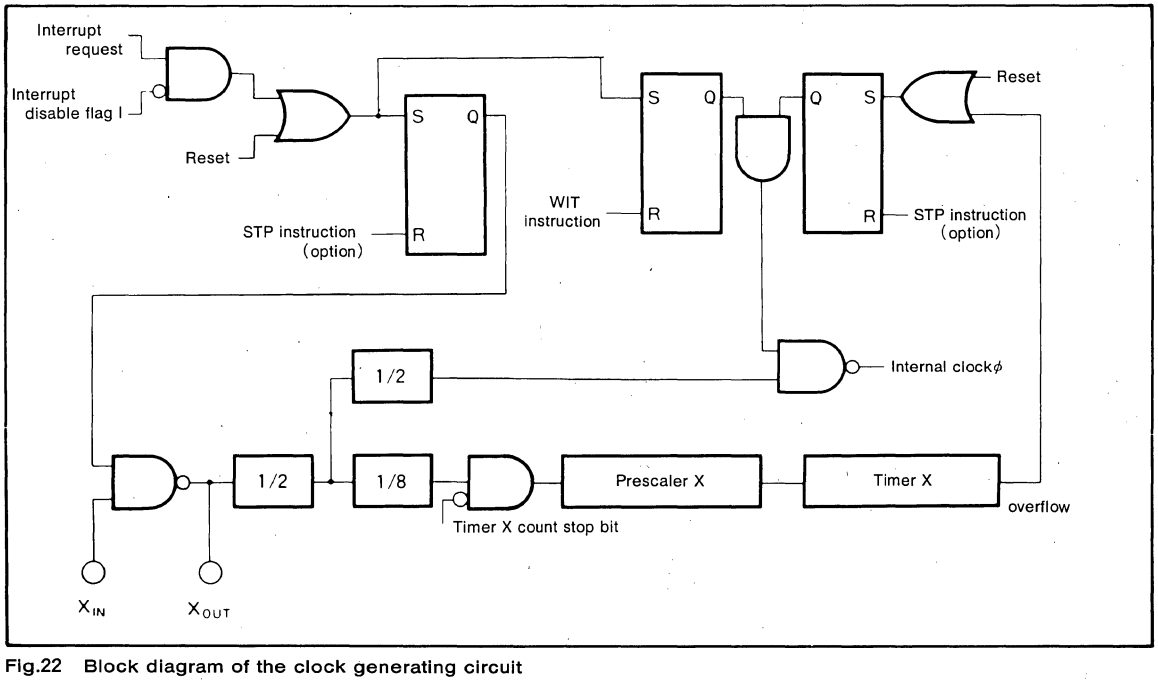


Fig.22 Block diagram of the clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(5) A NOP instruction must be used after the execution of a PLP instruction.
(6) Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed larger than 1MHz during A-D conversion. And during A-D conversion, don't use STP or WIT instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ..... EPROM 3sets
Write the following option on the mask ROM confirmation form
• STP instruction option

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	−0.3～7	V
V_I	Input voltage X_{IN}		−0.3～7	V
V_I	Input voltage $P2_0$～$P2_7$, $P4_2$～$P4_7$		−0.3～V_{CC}+0.3	V
V_I	Input voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P3_0$～$P3_7$, $P4_0$, $P4_1$, $P5_0$～$P5_7$, $\overline{INT_1}$		−0.3～13	V
V_I	Input voltage CNV_{SS}, $\overline{RESET}$		−0.3～13	V
V_O	Output voltage $P2_0$～$P2_7$, $P4_2$～$P4_7$, X_{OUT}, ϕ, D-A		−0.3～V_{CC}+0.3	V
V_O	Output voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P3_0$～$P3_7$, $P4_0$, $P4_1$, $P6_0$～$P6_3$, PWM		−0.3～13	V
P_d	Power dissipation	T_a=25℃	1000(Note 1)	mW
T_{opr}	Operating temperature		−10～70	℃
T_{stg}	Storage temperature		−40～125	℃

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10～70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, $P5_0$～$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}, $P6_0$	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, $P5_0$～$P5_7$, $\overline{INT_1}$, CNV_{SS}, $P6_0$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$ (Note 3)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$～$P6_3$ (Note 3)			15	mA
$I_{OL(peak)}$	"L" peak output current PWM (Note 3)			5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, (Note 2)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0$～$P6_3$ (Note 2)			7	mA
$I_{OL(avg)}$	"L" average output current PWM (Note 2)			2.5	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$～$P2_7$ (Note 3)			−10	mA
$I_{OH(avg)}$	"H" average output current $P2_0$～$P2_7$ (Note 2)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

Note 2 : Average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
3 : Total of "L" output current I_{OL}, of ports P0, P1, P2, P3, P4, P6, and PWM is 80mA max.
Total of "H" output current I_{OH}, of port P2 is 50mA max.
4 : "H" input voltage of ports P0, P1, P3, $P4_0$～$P4_3$, P5, and $\overline{INT_1}$ is available up to +12V.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P2_0$~$P2_7$	I_{OH}=−10mA		3			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA		3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_3$	I_{OL}=10mA				2	V
V_{OL}	"L" output voltage ϕ, PWM	I_{OL}=5mA				2	V
$V_{T+}-V_{T-}$,	Hysteresis $\overline{INT_1}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input		0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$	When used as $\overline{INT_2}$ input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_3$	When used as CNTR input		0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $P6_0$	When used as T input		0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}			0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=0V				−5	μA
I_{IL}	"L" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I=0V				−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=12V				12	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, $P2_0$~$P2_7$, $P4_4$~$P4_7$	V_I=5V				5	μA
V_{RAM}	RAM retention voltage	At clock stop		2			V
I_{CC}	Supply current	ϕ, X_{OUT}, and D-A pins opened, other pins at V_{SS}, and A-D converter in the finished condition.	$f_{(X_{IN})}$=4MHz Square wave		3	6	mA
			At clock stop T_a=25℃			1	μA
			At clock stop T_a=75℃			10	

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance value	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference input voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			5	Bits
—	Error in full scale range	V_{REF}=V_{CC}			±1	%
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
R_O	Output resistance	V_{REF}=V_{CC}			3	kΩ
V_{REF}	Reference voltage		4		V_{CC}	V

TIMING REQUIREMENTS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	270			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time	20			ns
t_c	External clock input cycle time	250			ns
t_w	External clock input pulse width	75			ns
t_r	External clock rising edge time			25	ns
t_f	External clock falling edge time			25	ns

Eva-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Memory expanding mode and microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	30			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.23			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.24			230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig.23			230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				230	ns

Eva-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.23			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.24			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig.23			250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns

Memory expanding mode and microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.23			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.24			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig.23			250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

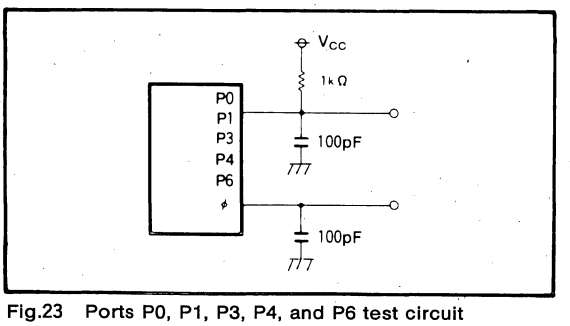


Fig.23 Ports P0, P1, P3, P4, and P6 test circuit

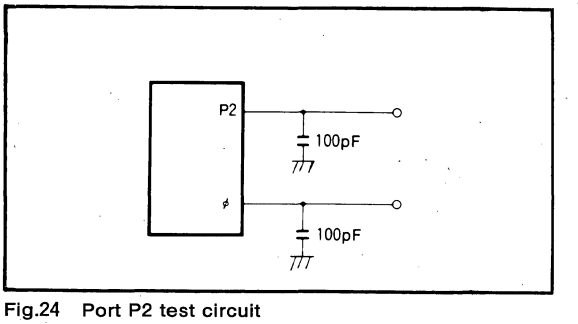
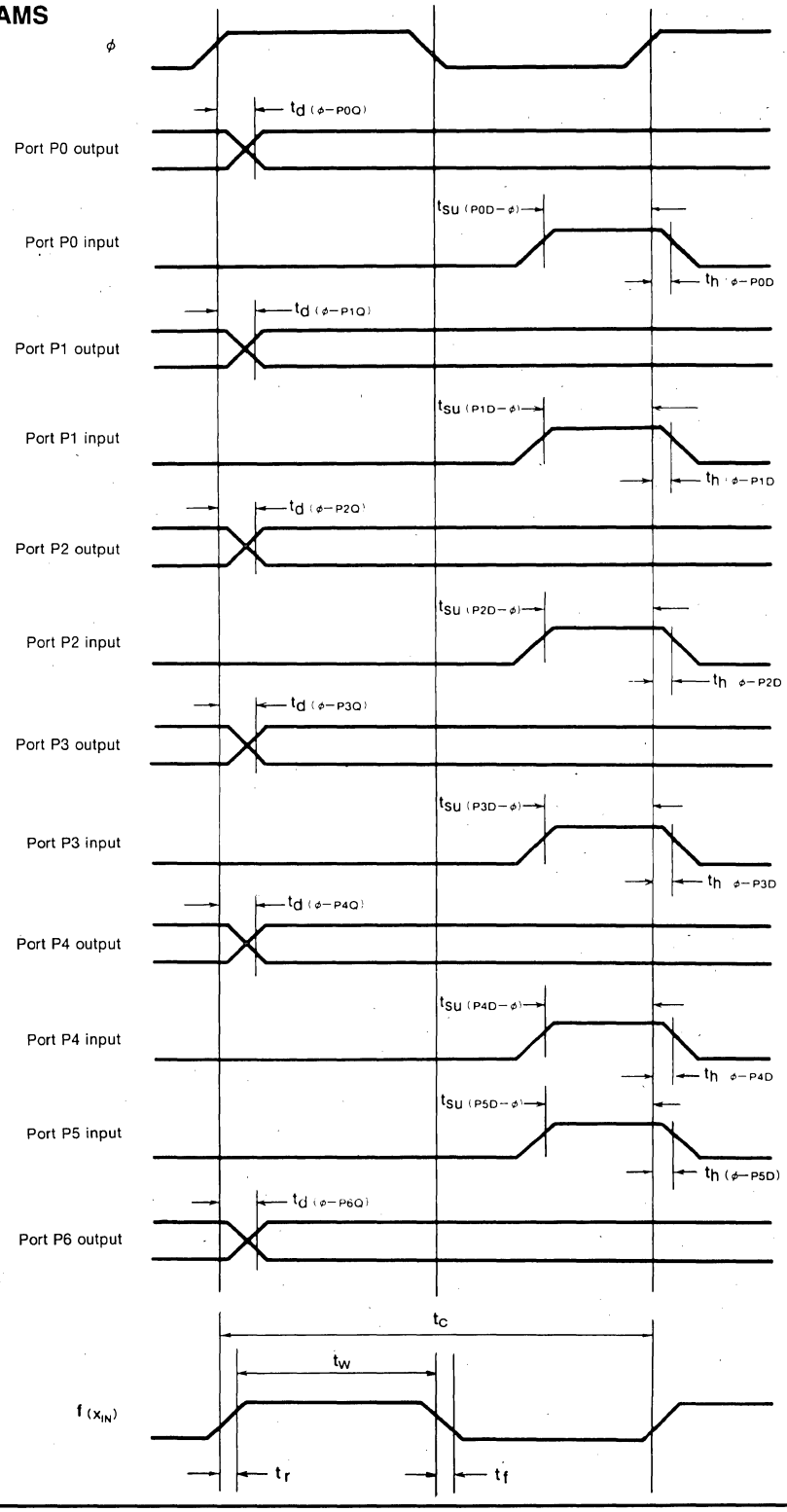


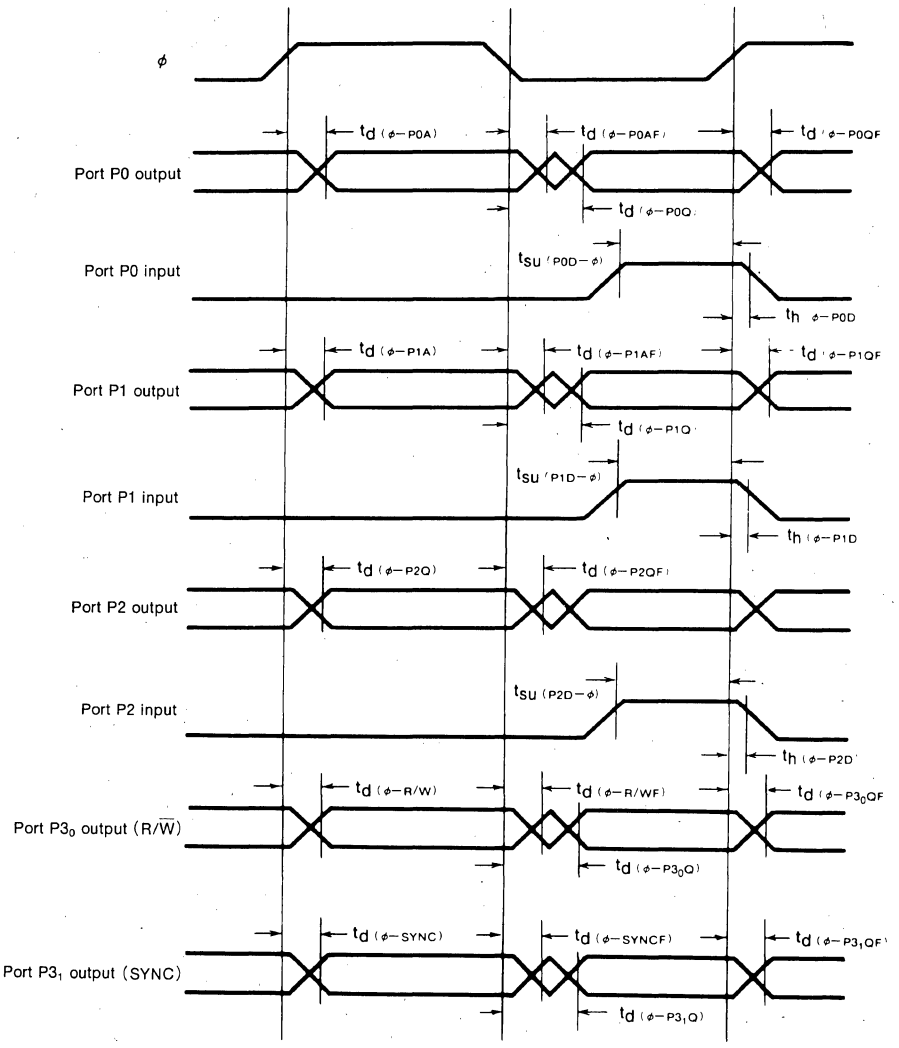
Fig.24 Port P2 test circuit

TIMING DIAGRAMS

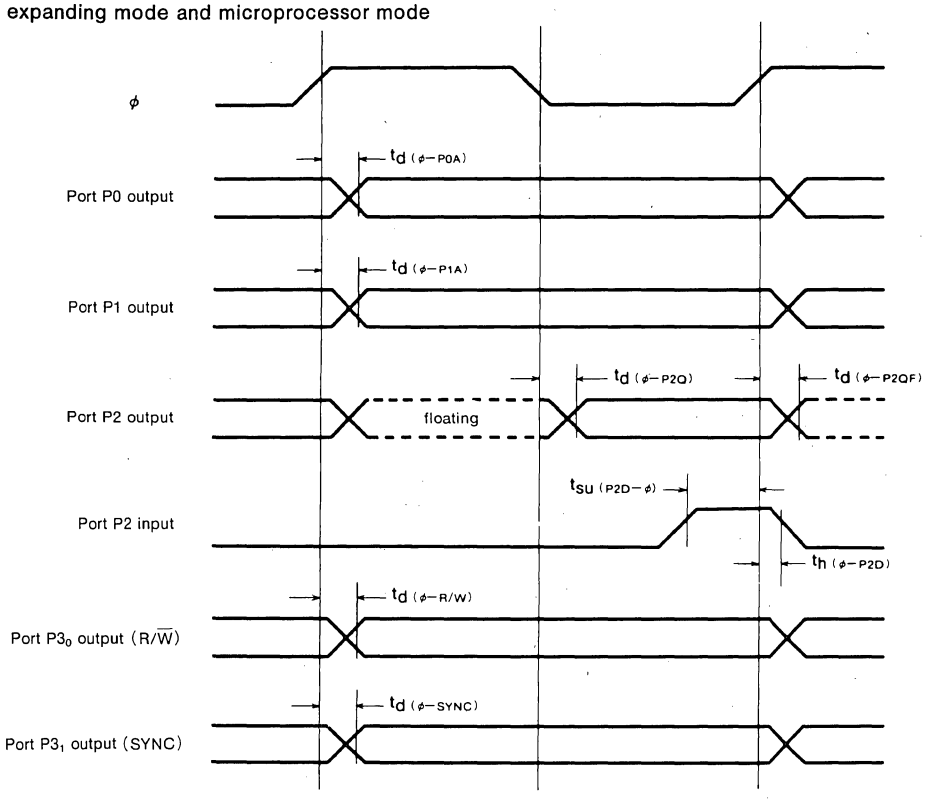
In single-chip mode



In eva-chip mode



In memory expanding mode and microprocessor mode



PRELIMINARY

Notice: These are not a final specification. Some parametric limits are subject to change.

M37410M3-XXXFP
M37410M4-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37410M3-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 80-pin plastic molded QFP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

This microcomputer is also suitable for applications which require controlling LCDs.

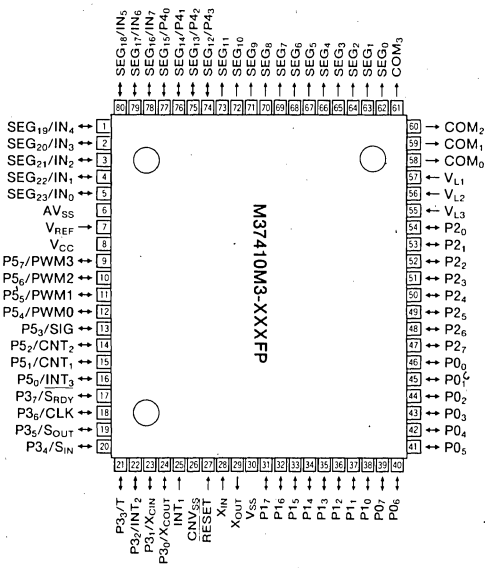
The differences between the M37410M3-XXXFP and the M37410M4-XXXFP are noted below. The following explanations apply to the M37410M3-XXXFP. Specification variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M37410M3-XXXFP	6144 bytes	192 bytes
M37410M4-XXXFP	8192 bytes	256 bytes

DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size
  - ROM ..... 6144 bytes (M37410M3-XXXFP)
    8192 bytes (M37410M4-XXXFP)
  - RAM ..... 192 bytes (M37410M3-XXXFP)
    256 bytes (M37410M4-XXXFP)
- Instruction execution time
  - at high-speed mode 1μs
  - at low-speed mode 4μs
- Single power supply
  - f(X_{IN})=8MHz ..... 4.5~5.5V
  - f(X_{IN})=2MHz ..... 2.5~5.5V
- Power dissipation
  - normal operation mode (at 8MHz frequency) ..... 30mW (V_{CC}=5V, Typ.)
  - low-speed operation mode (at 32kHz frequency for clock function) ..... 54μW (V_{CC}=3V, Typ.)
- RAM retention voltage (stop mode) ..... 2.0V$\leqq V_{RAM} \leqq$5.5V
- Subroutine nesting ..... 96levels (Max.)
- Interrupt 9types, 5vectors
- 8-bit timer 4
- 16-bit timer ..... 1 (Two 8-bit timers make one set)
- Programmable I/O ports (Ports P0, P1, P2, P3, P4) 40
- Serial I/O (8-bit) 1
- A-D converter ..... 8-bit, 8channel conversion speed (25μs)
- LCD controller/driver (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty)
  - segment output 24
  - common output 4
- Two clock generating circuits (One is for main clock, the other is for clock function)

PIN CONFIGURATION (TOP VIEW)



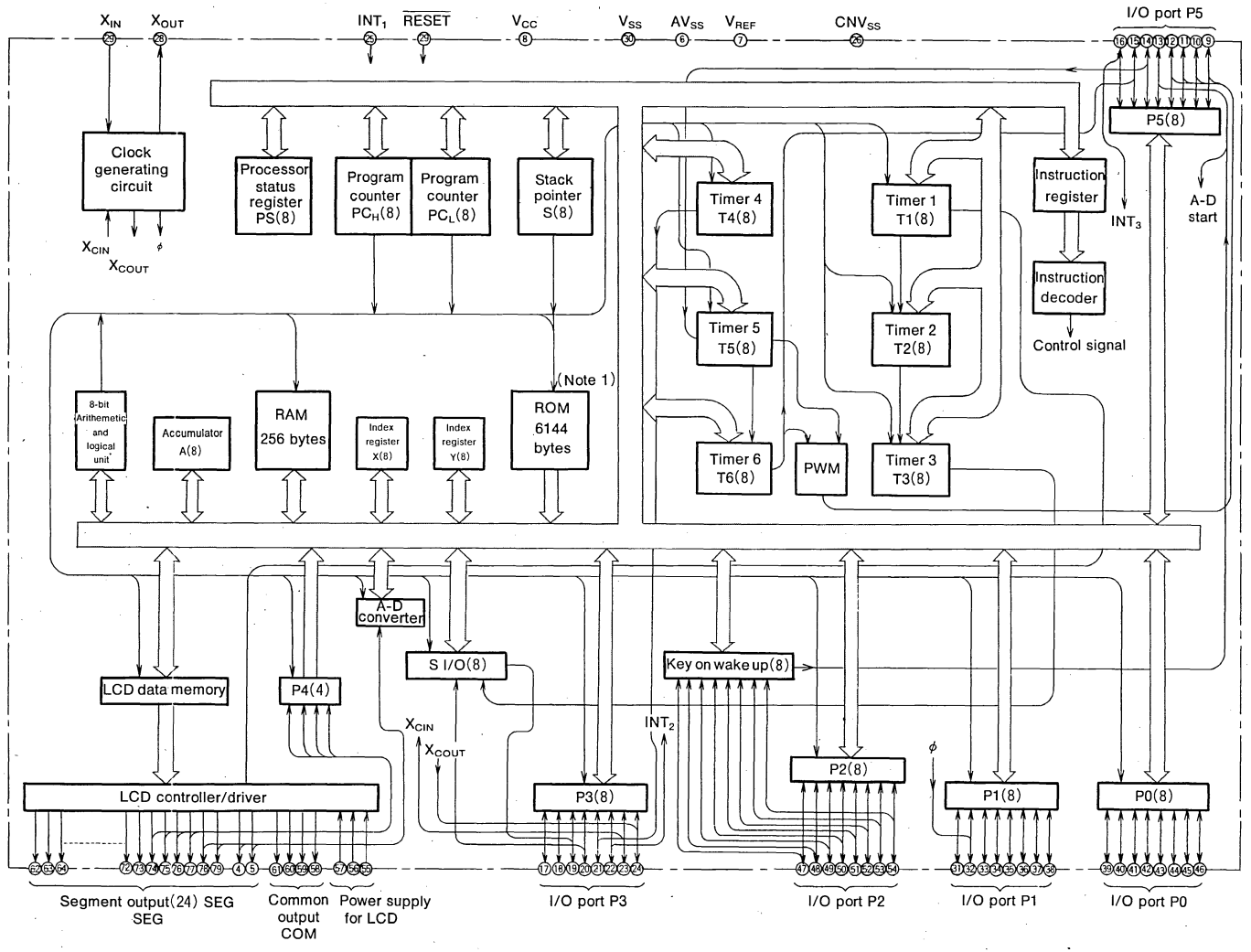
Outline 80P6S

APPLICATION

Audio-visual equipment
Remote control
Camera

MITSUBISHI ELECTRIC

M37410M3-XXXFP BLOCK DIAGRAM



Note 1 : 8192 bytes for M37410M4-XXXFP

FUNCTIONS OF M37410M3-XXXFP

Parameter			Functions
Number of basic instructions			69
Instruction excution time			1μs (minimum instructions, at 8MHz frequency).
Clock frequency			8MHz (at V_{CC}=5V±10%)
Memory size	ROM		6144bytes (8192bytes for M37410M4-XXXFP)
	RAM		192bytes (256bytes for M37410M4-XXXFP)
	RAM for display LCD		12bytes
Input/Output port	P0, P1, P2, P3, P5	I/O	8-bit×5
	P4	Input	4-bit×1 (port P4 are in common with SEG)
	SEG	LCD output	24-bit×1
	COM	LCD output	4-bit×1
Serial I/O			8-bit×1
Timers			8-bit timer×4
			16-bit timer×1 (combination of two 8-bit timers)
LCD controller/driver	Bias		1/2, 1/3 bias selectable
	Duty ratio		1/2, 1/3, 1/4 duty selectable
	Common output		4
	Segment output		24 (SEG_{12}~SEG_{23} are in common with port P4)
Subroutine nesting			96 (max)
Interrupt			Three external interrupts, Three timer interrupts
Clock generating circuit			Two built-in circuit (ceramic or quartz crystal oscillator)
Operating temperature range			−20~75℃
Device structure			CMOS silicon gate
Package			80-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is connect to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 16μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
INT_1	Interrupt input	Input	This is the highest order interrupt input pin.
AV_{SS}	Voltage input for A-D		This is GND input pin for the A-D converters.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converters.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-ch open drain.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 and also works as the key on wake up function with mask option.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P1. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$, $P3_2$, $P3_1$, and $P3_0$ work as timer 4 overflow signal divided by 2 output pin (T), INT_2 pin, X_{CIN} and X_{COUT} pins, respectively.
$SEG_{12}/P4_3$ ~ $SEG_{15}/P4_0$	Segment output /Input port P4	Output / Input	SEG_{12}~SEG_{15} work as input port P4 and also used by 2-bit unit as LCD segment output.
$P5_0$~$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as P1. $P5_0$, $P5_1$, $P5_2$ and $P5_3$ are in common with INT_3, timer3 input, timer5 input and A-D trigger input respectively. $P5_4$~$P5_7$ are also in common with PWM0~PWM3.
V_{L1}~V_{L3}	Voltage input for LCD	Input	These are voltage input pins for LCD. Supply voltage as $0V \leqq V_{L1} \leqq V_{L2} \leqq V_{L3} \leqq V_{CC}$. 0~$V_{L3}$V is supplied to LCD.
COM_0~ COM_3	Common output	Output	These are LCD common output pins. At 1/2 duty, COM_2 and COM_3 pins are not used. At 1/3 duty, COM_3 is not used.
SEG_0~ SEG_{11}	Segment output	Output	These are LCD segment output pins.
SEG_{16}/IN_7 ~ SEG_{23}/IN_0	Segment output /Analog input	I/O	SEG_{16}~SEG_{23} work as analog input pins IN_7~IN_0. SEG_{16}~SEG_{19} are used by 2-bit unit and SEG_{20}~SEG_{23} by 4-bit unit.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M37410M3-XXXFP is shown in Figure1. Addresses 2800_{16} to $3FFF_{16}$ are assigned for the built-ROM area which consists of 6144 byes (Addresses 2000_{16} to $3FFF_{16}$ are assigned for the built-in ROM area which consists of 8192 bytes for M37410M4-XXXFP). Addresses $3F00_{16}$ to $3FFF_{16}$ are a special address area (special page). By using the special page addressing mode of JSR instruction, subroutines addressed on this page can be called with only 2bytes. Addresses $3FF4_{16}$ to $3FFF_{16}$ are vector addresses used for reset and interrupts (see interrupts chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using zero pege addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required.

The RAM, I/O port, timer, etc. addresses are already assigned for the Zero Page. Addresses 0000_{16} to $00BF_{16}$ are assigned for the built-in RAM which consists of 192 bytes (Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $013F_{16}$ are assigned for the built-in RAM which consists of 256 bytes for M37410M4-XXXFP). This RAM is used as the stack during subroutine calls and interrups, in addition to data storage.

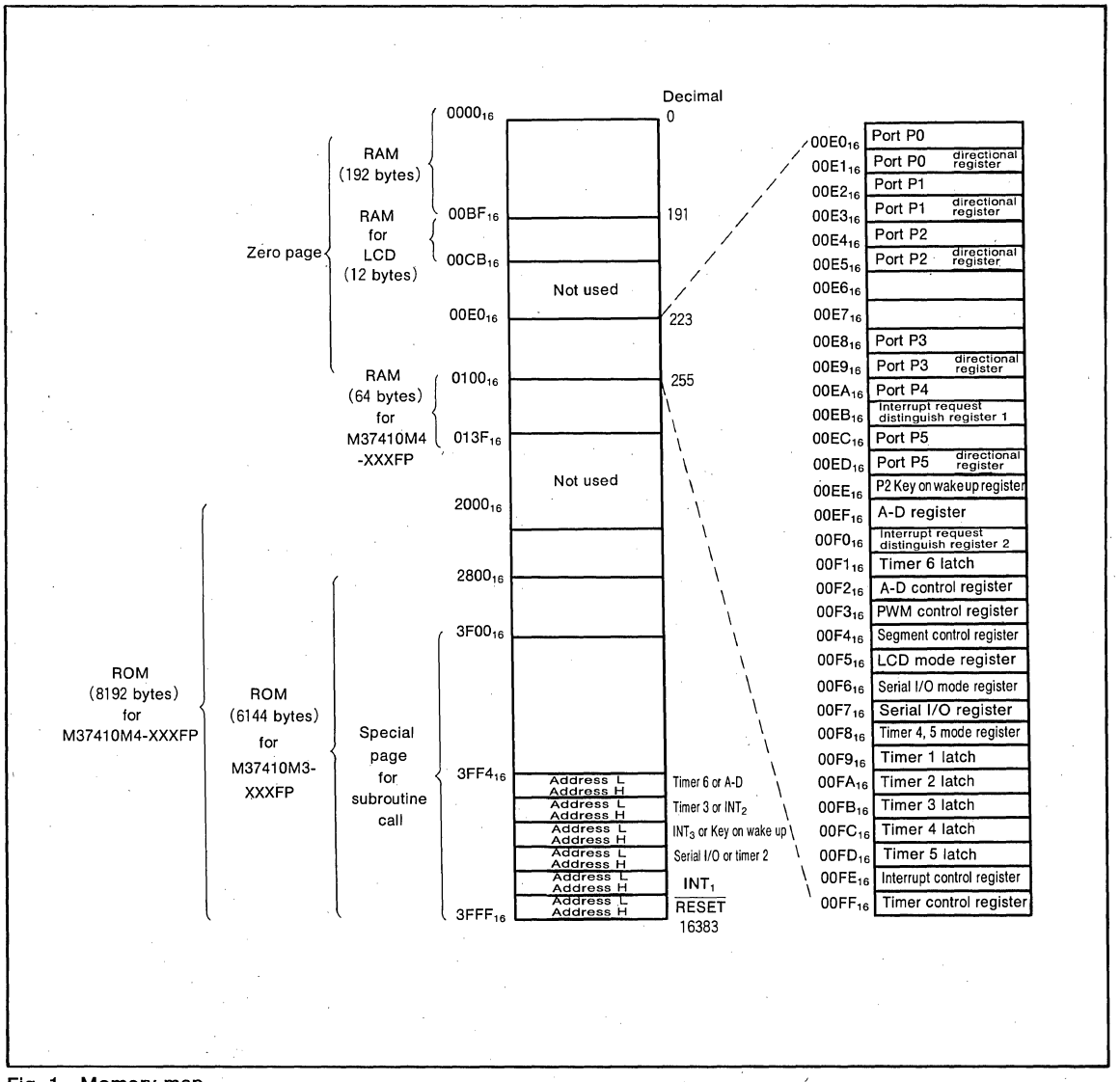


Fig. 1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown inFigure2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Date operations such as data transfer. input/output, etc., is executed mainly through the accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register. In the index register X addressing mode, the value of theOPERAND added to the contents of the index register X specifies the real address. When the T flag in the processors status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register. In the index register Y addressing mode, the value of the OPERAND added to the contents of the index register Y specifies the real address.

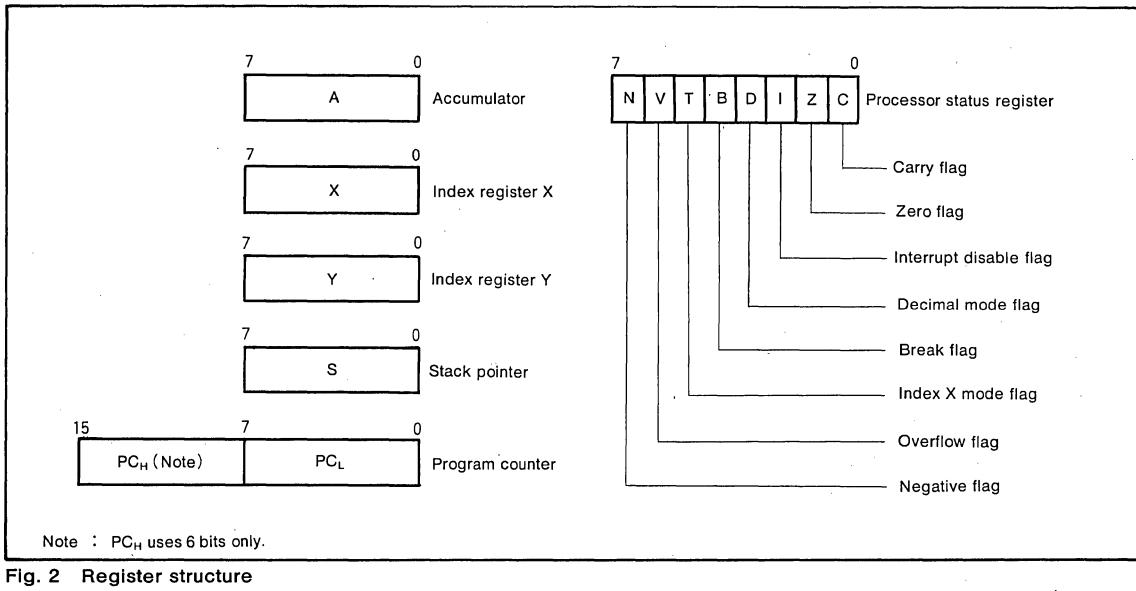


Fig. 2 Register structure

STACK POINTER (S)

The stack pointer is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

When an interrupt occurs, the higher 8-bit of the program counter is pushed into the stack first, the stack pointer is decremented, and then the lower 8-bits of the program counter is pushed into the stack. Next the contents of the processor status register is pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter and processor status register data is popped off the stack in reverse order from above.

The accumulator is never pushed into the stack automatically, so a Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pop Accumulator instruction (PLA) . It is executed in the revese order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed and popped to and from the stack with the PHP and PLP instructions, respectively.

During a subroutine call, only the program Counter is pushed into the stack. Therefore, any registers that should not be destroyed should be pused into the stack manually. To return from a subroutine call, the RTS instruction is used.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PC_H is used 6 bits.

PROCESSOR STATUS REGISTER (PS)

The 8-bit PS is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flags (C) , Zero flag (Z), Overflow fag (V) or the Negative flag (N) . Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic Logic Unit (ALU) immediately after an operation. It is also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediated operation generated a zero result or not. If the result is zero, the zero flag will be set to "0". If the result is not zero, the zero flag will be set to "1".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts This is accomplished by setting the flag to "1". When an interrupt is accepted, this flag is automatically set to"1" to prevent from other interrupts until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is "0", the operations are executed in binary. Decimal correction is automatically exected. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are preformed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the B flag will be "1", otherwise, it will be"0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly, without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the T flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a singed binary number. When the result exceeds+127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the V flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the N flag. There are no instructions for directly setting or resetting the N flag.

INTERRUPT

The M37410M3-XXXFP can be interrupted from ten sources; INT_1, Timer 2 or Serial I/O, INT_3 or Key on wake up, INT_2 or Timer 3, Timer 6 or A-D, and BRK instruction.

"Key on wake up" can only be used at power down state by STP instruction or WIT instruction. When one of the P2 is "L", an interrupt occurs.

These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as an interrupt.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, as discussed in the stack pointer section, and the interrupt disable flag (I) is set, and the program jumps to the address specified by the interrupt vector, and the interrupt request bit of the interrupt control register or timer control register is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the INT_1, INT_2 or INT_3 pins go from "H" to "L" or "L" to "H"

(2) When the levels any pin of P2 goes "L"(at power down mode)

(3) When the contents of timer 2, timer 3, timer 6 or the counter of serial I/O goes "0"

When the two interrupt requests, which are the same priority and are at the same sampling, the priority process is processed by interrupt request distinguish register 1 and 2.

These request bits can be reset by a program but can not be set. Since the BRK instruction interrupt and the timer6 or A-D, interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if timer 6 or A-D generated the interrupt.

Table 1. Interrupt vector address and priority.

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$3FFF_{16}$, $3FFE_{16}$
INT_1	2	$3FFD_{16}$, $3FFC_{16}$
Serial I/O or timer 2	3	$3FFB_{16}$, $3FFA_{16}$
INT_3 or key on wake up	4	$3FF9_{16}$, $3FF8_{16}$
INT_2 or timer 3	5	$3FF7_{16}$, $3FF6_{16}$
Timer 6 or A-D (BRK)	6	$3FF5_{16}$, $3FF4_{16}$

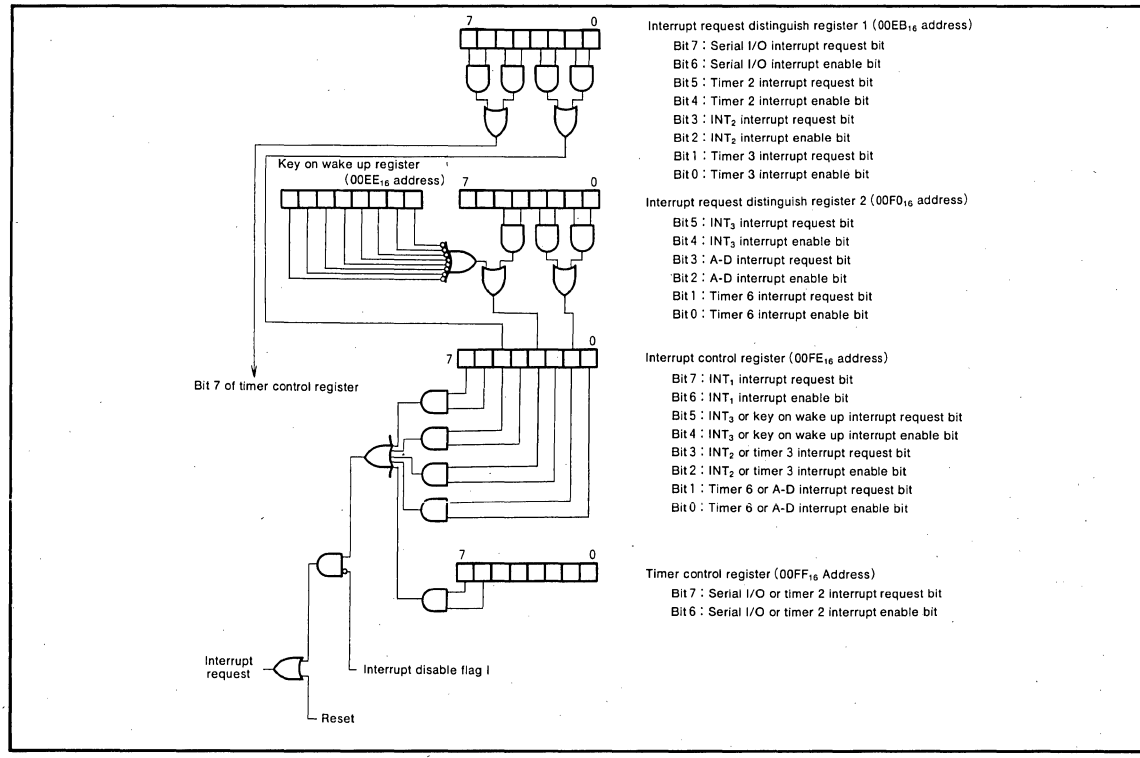


Fig. 3 Interrupt control

TIMER

The M37410M3-XXXFP has six timers; timer 1, timer 2, timer 3, timer 4, timer 5 and timer 6.

A block diagram of timer1 through 6 is shown in Figure 4.

The count source for timer 1 through 3 can be selected by using bit 2, 3, 4 and 5 of the timer control register (address $00FF_{16}$), as shown in Figure 5. All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timer is $1/(n+1)$, where n is the contents of timer latch.

Timer 2, 3 and 6 has interrupt generating functions. The timer interrupt request bit which is in the interrupt distinguish register 1 or 2 (located at addresses $00EB_{16}$ and $00F0_{16}$ respectively) is set at the next count pulse after the timer reaches "0" (see interrupt section).

The starting and stopping of timer1 is controlled by bit 7 of the interrupt distinguish register 2, timer 3 by bit 6 of the interrupt distinguish register 2 and timer 4 by bit 3 of timer 4, 5 and 6 mode register ($00F8_{16}$ address). If the corresponding bit is "0". the timer starts counting, and the corresponding bit is "1", the timer stops. The timer4 overflow signal divided by 2 can be outputed from port $P3_3$ by setting the bit 4 of the serial I/O mode register ($00F6_{16}$ address) to "1".

Timer 5 and 6 work as timer mode, event counter mode and PWM mode by changing the contents of bit 5 and bit 6 of the timer 4, 5 and 6 mode register.

(1) Timer Mode

This mode is the 16-bit timer, and the count source is $\phi/4$. When the bit 6 of PWM control register ($00F3_{16}$ address) is "1", the timer6 overflow singnal divided by 2 is output from CNT_2 pin (common with $P5_2$).

(2) Event Counter Mode

The count source is input from the CNT_2 pin. The count decremented each time the input goes from "L" to "H".

(3) PWM Mode

As shown in Figure 7, the output wave is controlled by the contents of the timer latch of timer 5 and 6.

PWM output can choose among PWM0, PWM1, PWM2 and PWM3 by bit 0, bit 1, bit 2 and bit 3 of PWM control register.

When the count value of all timers, from timer 1 to timer 6, are read, be careful not to change the input source.

When the count source is inputed from the external pin, the minimum pluse width should be 8μs.

After a STP instruction is executed, timer 2, timer 1, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 5 of the timer control register). This state is canceled if timer2 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 7 of the interrupt distinguish register2 (timer1 count stop bit), bit 5 of the interrupt distinguish register1, and bit 6 of the timer control register must be set to "0" (prohibition). And also bit 4 of the interrupt distinguish register1 must be set to "1". For more details on the STP instruction, refer to the oscillation circuit section.

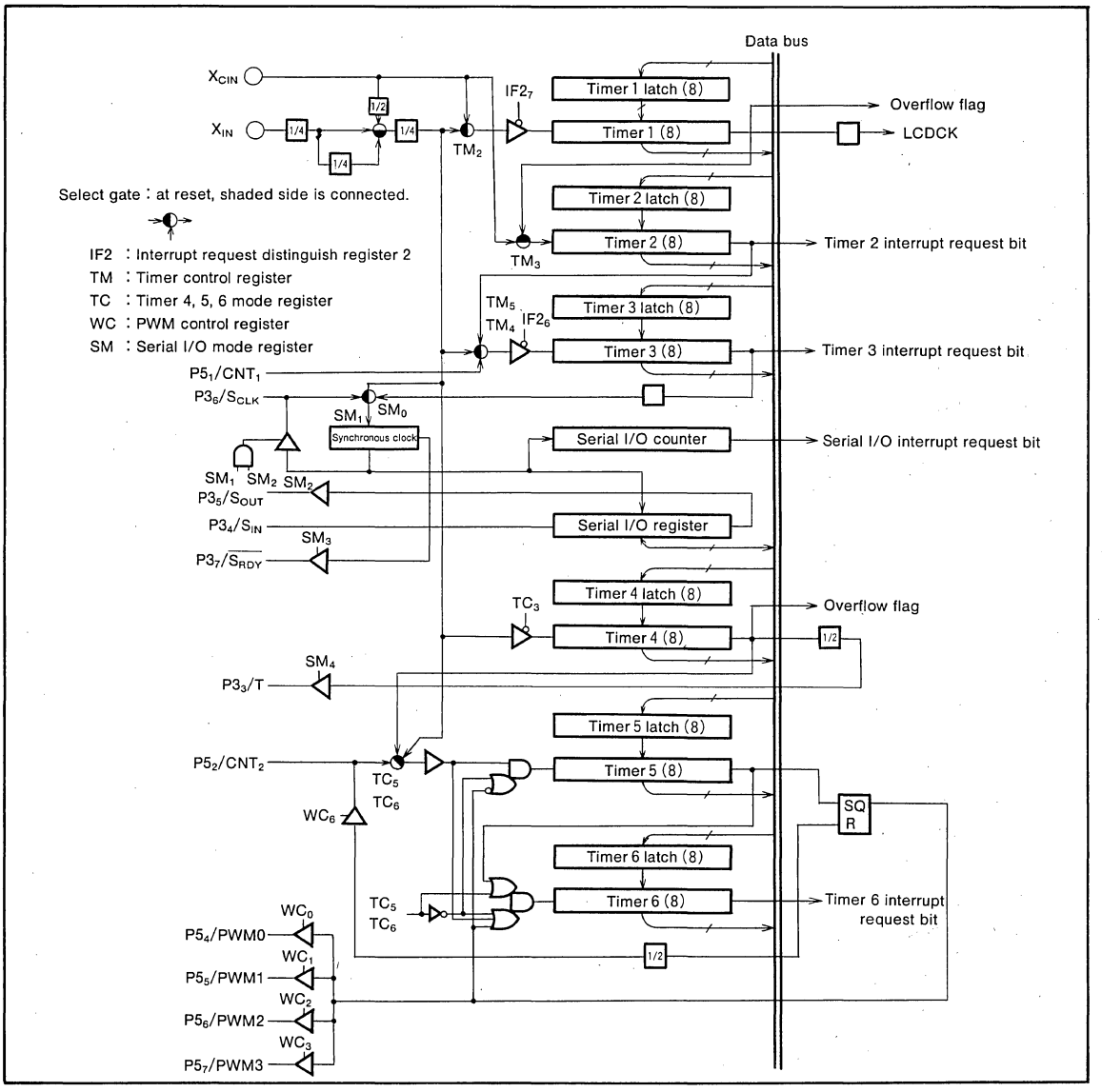


Fig. 4 Block diagram of timer 1 through 6

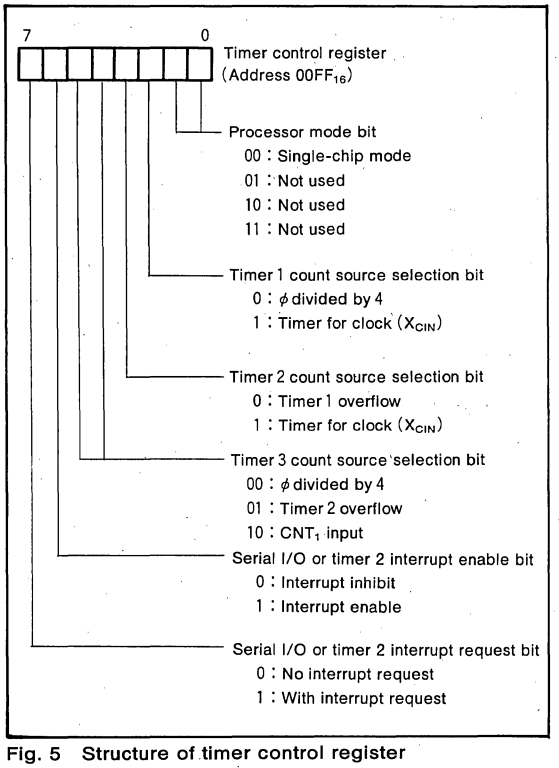


Fig. 5 Structure of timer control register

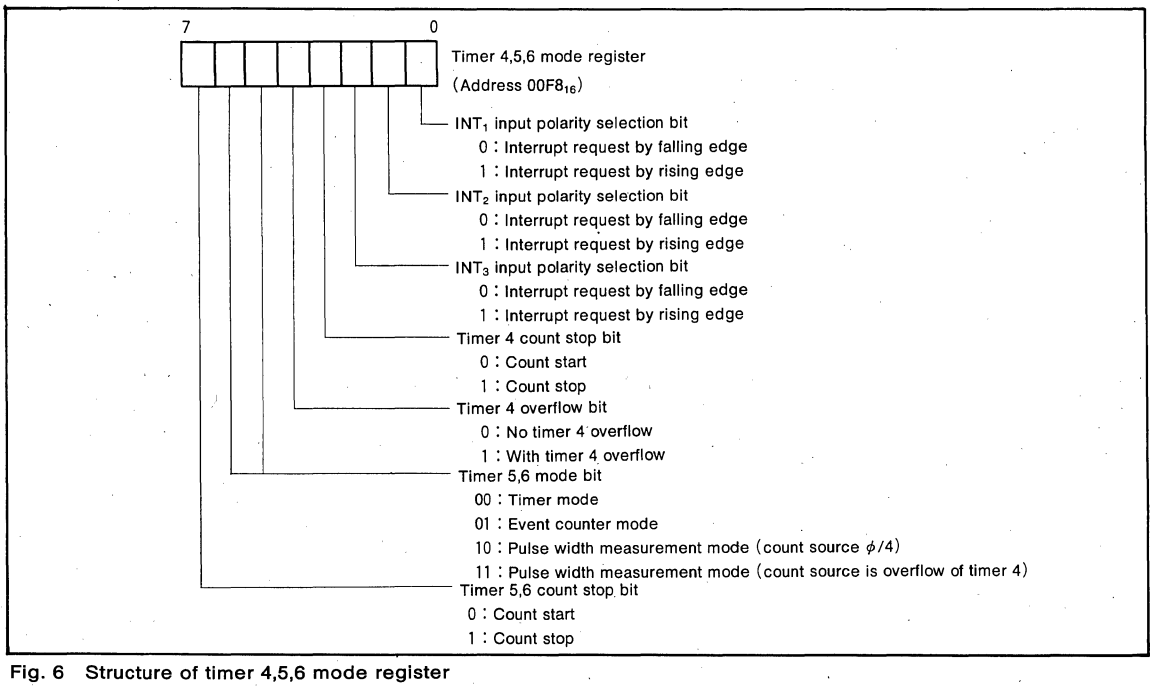


Fig. 6 Structure of timer 4,5,6 mode register

PWM

M37410M3-XXXFP has a pulse width modulated (PWM) output control circuit connecting with timer5 and timer6.

Figure 6 shows the structure of timer 4,5,6 mode register, Figure 7 shows the PWM rectangular wave form and Figure 8 shows the structure of PWM control register.

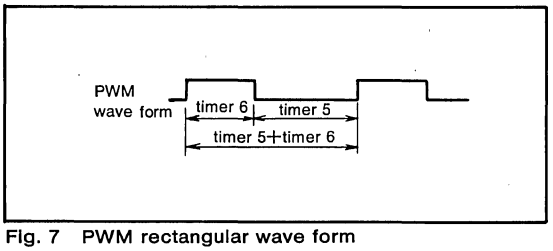


Fig. 7 PWM rectangular wave form

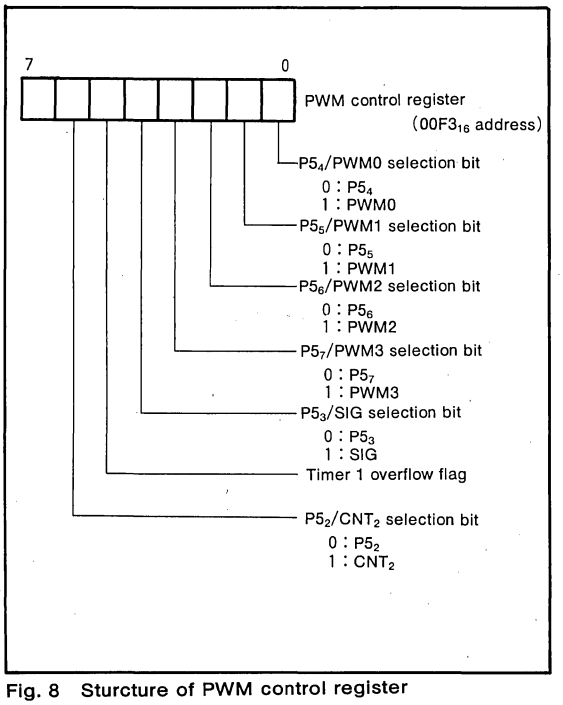


Fig. 8 Sturcture of PWM control register

SERIAL I/O

The block diagram of serial I/O is shown in Figure 9. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK). and the serial I/O (S_{OUT}, S_{IN}) pins are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively.

The serial I/O mode register (address $00F6_{16}$) is an 8-bit register. Bit 1 and 0 of this register is used to select a synchronous clock source. When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal divided by two from timer 3 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 becomes the clock.

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If the external synchronous clock is selected, the clock is input to $P3_6$. And $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Bit 3 determines if $P3_7$ is

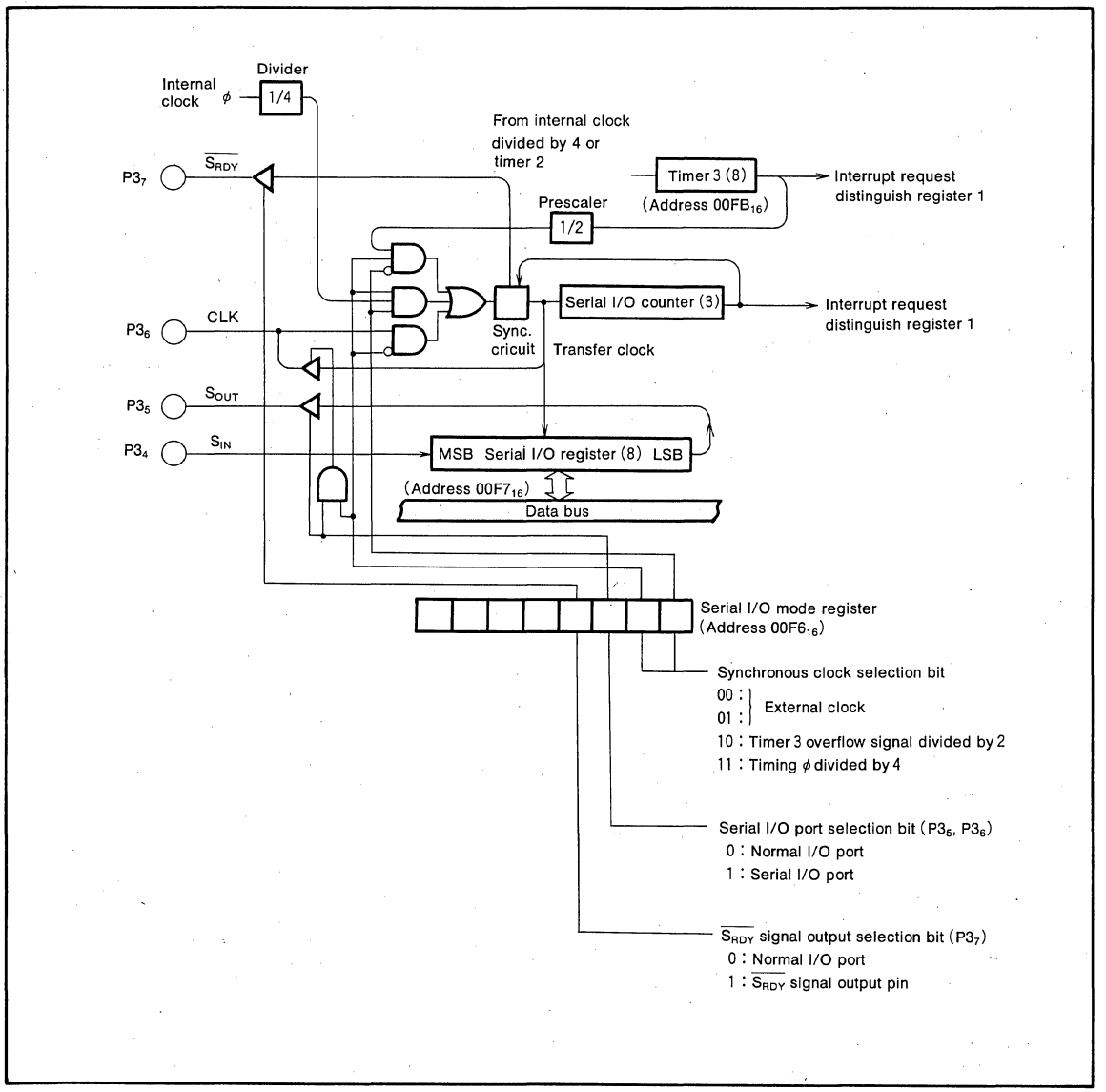


Fig. 9 Block diagram of serial I/O

used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDY}}$) or used as a nomal I/O pin (bit 3="0").

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock — The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37410M3-XXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock — If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 10, and connection between two M37410M3-XXXFP's are shown in Figure 11.

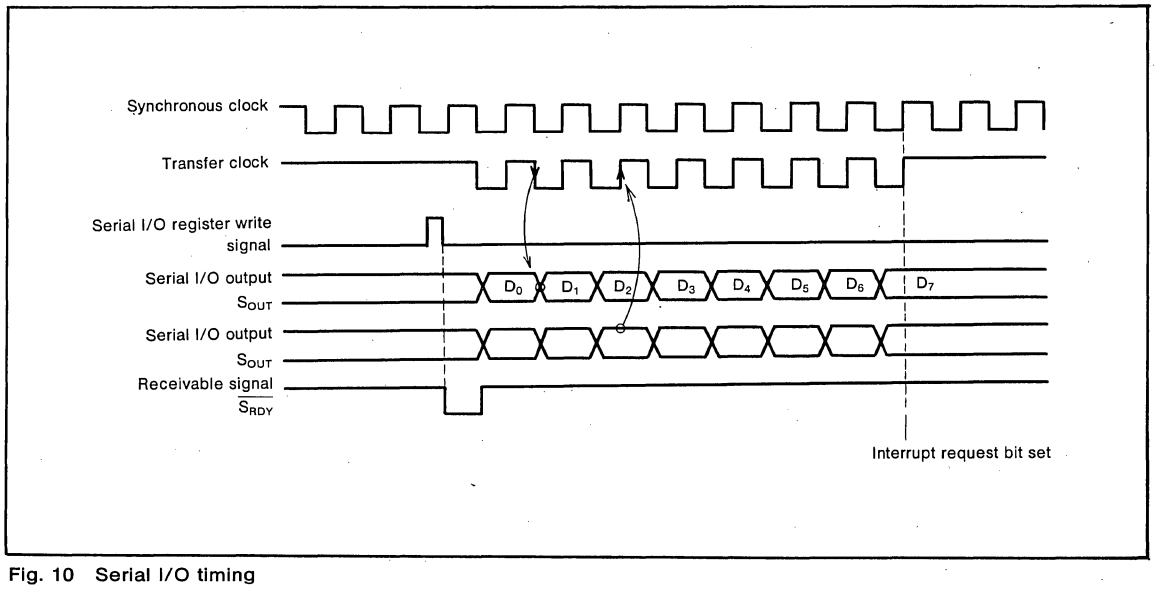


Fig. 10 Serial I/O timing

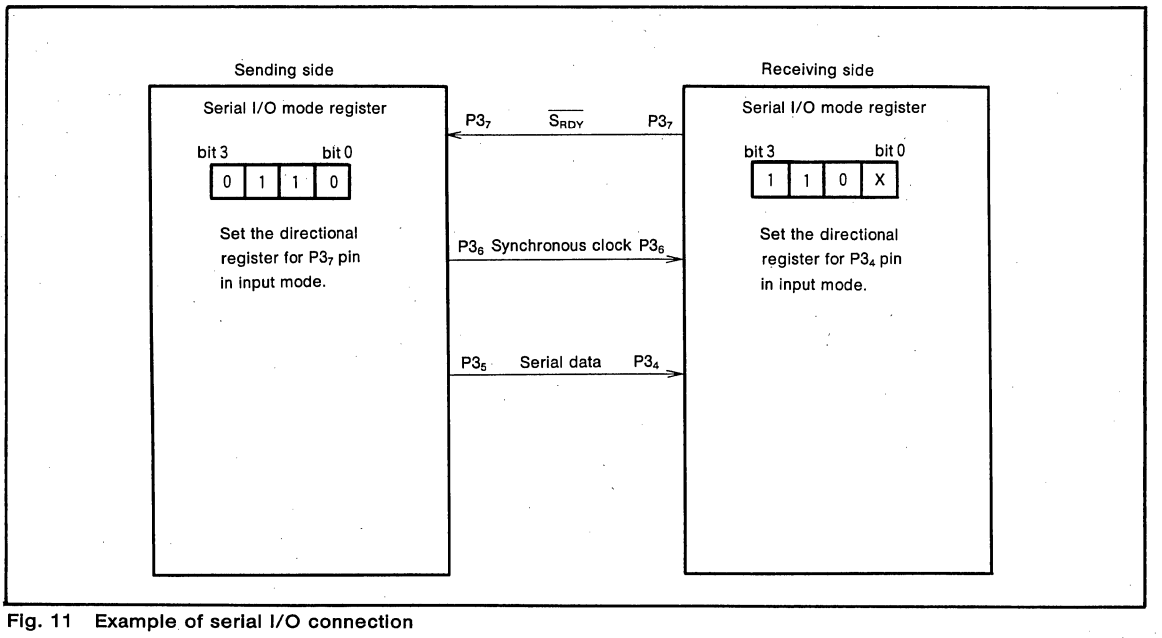


Fig. 11 Example of serial I/O connection

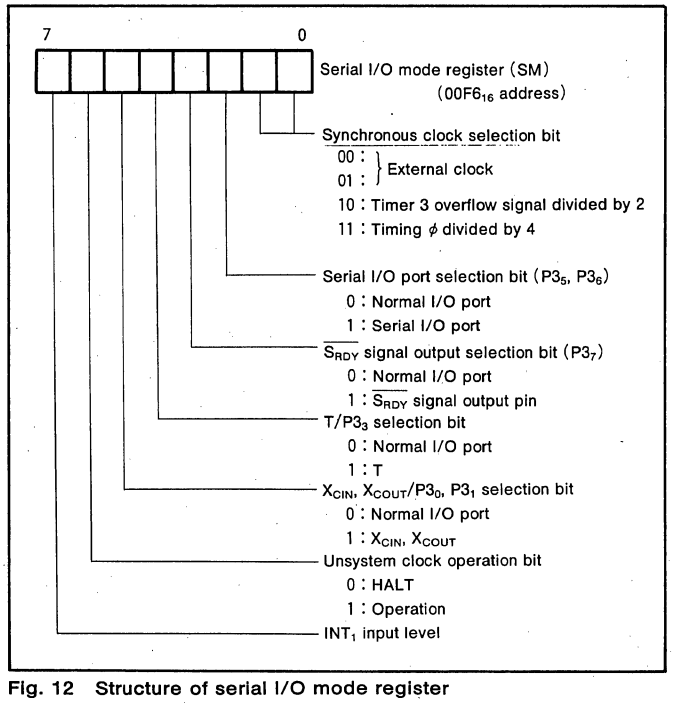


Fig. 12 Structure of serial I/O mode register

LCD CONTROLLER/DRIVER

The M37410M3-XXXFP has internal LCD controllers and drivers. A Block Diagram of LCD circuit is shown in Figure 15. The terminals for LCD consist of 4 common-pin and 24 segment-pin. SEG_{12}~SEG_{15} are in common with input P4. Also SEG_{16}~SEG_{23} are in common with IN_0~IN_7.These are selected by bit 3~7 of the LCD segment control register ($00F4_{16}$ address). Two biases (1/2 and1/3) can also be selected. When bit 2 of the LCD mode register is "1", 1/2 bias is selected. When bit 2 is "0", 1/3 bias is selected. 1,1/2,1/3, or 1/4 duty cycle can also be selected. When bits 0 and 1 of the LCD mode register (LM_0, LM_1) is n, the duty ratio is 1/(n+1).

Address $00C0_{16}$~$00CB_{16}$ is the designated RAM for the LCD display. When 1s' are written to these addresses, the corresponding segments of the LCD display panel are turned on. A map of the LCD display RAM is shown in Figure 13.

The ON/OFF function for the LCD controller is controlled by bit 3 of the LCD mode register (LM_3). When this bit is "1" all the segments of the LCD are turned on. When this bit is "0" all the segments are turned off.

The structure of the LCD mode register is shown in Figure 14.

Address \ Bit	7	6	5	4	3	2	1	0
C0	1	1	1	1	0	0	0	0
C1	3	3	3	3	2	2	2	2
C2	5	5	5	5	4	4	4	4
C3	7	7	7	7	6	6	6	6
C4	9	9	9	9	8	8	8	8
C5	11	11	11	11	10	10	10	10
C6	13	13	13	13	12	12	12	12
C7	15	15	15	15	14	14	14	14
C8	17	17	17	17	16	16	16	16
C9	19	19	19	19	18	18	18	18
CA	21	21	21	21	20	20	20	20
CB	23	23	23	23	22	22	22	22
	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0

*Number in data memory area indicates corresponding segment.

Fig. 13 Map of RAM for LCD segment

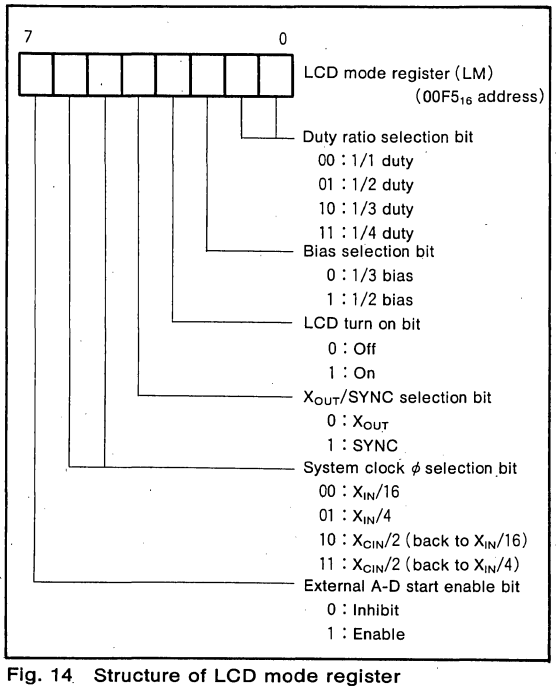


Fig. 14 Structure of LCD mode register

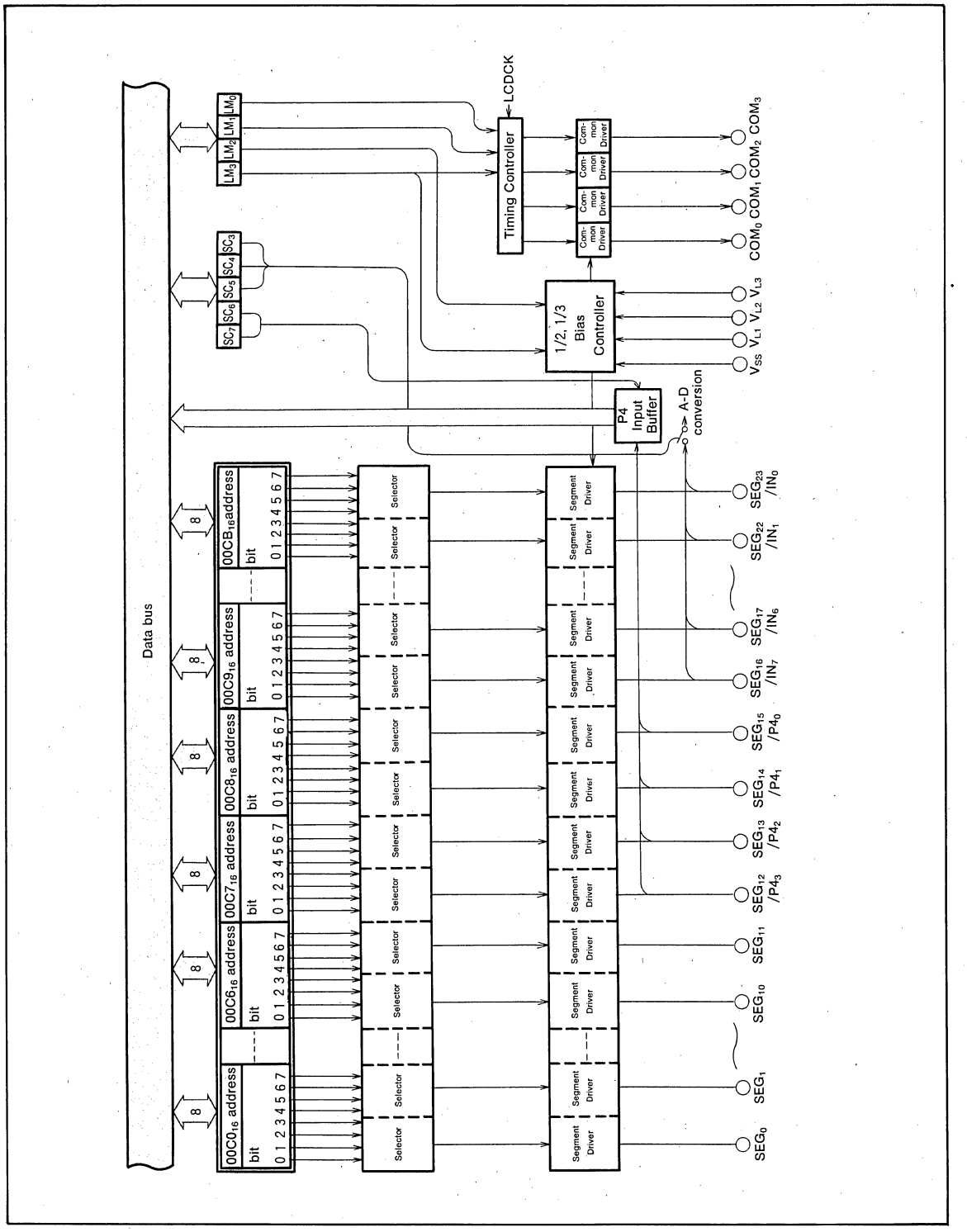


Fig. 15 Block diagram of LCD control circuit

A-D CONVERTER

The A-D converter circuit is shown in Figure 16. The analog input ports of the A-D converter (IN_0~IN_7) are in common with in the input ports of the data bus.

The segment control register is located at address $00F4_{16}$. One of the eight analog inputs is selected by bits 0, 1 and 2 of this register. The IN pins, not to use as analog input, uses as LCD segment output.

Bit 0, 1 and 2, and corresponding to analog input pin is shown in Figure 17. A-D conversion is accomplished by first selecting bit 0 and 1 of the A-D control register (address $00F2_{16}$) for the source of V_{REF}. And also the analog input pin is chosen by the analog input select bit of the segment control register. A-D conversion starts by writing a dummy data to the A-D register (address $00EF_{16}$) or changing the input level from SIG pin "H" to "L". When A-D conversion is finished, an interrupt is generated. After A-D interrupt is accepted, the result of A-D conversion can be read from the A-D register.

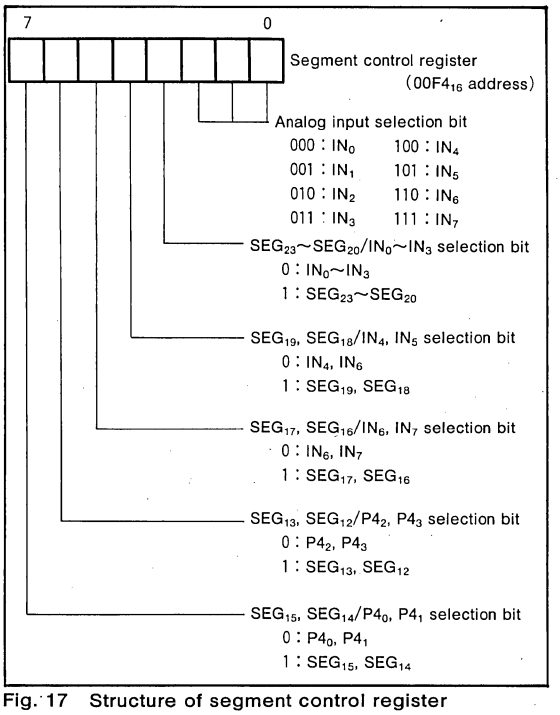


Fig. 17 Structure of segment control register

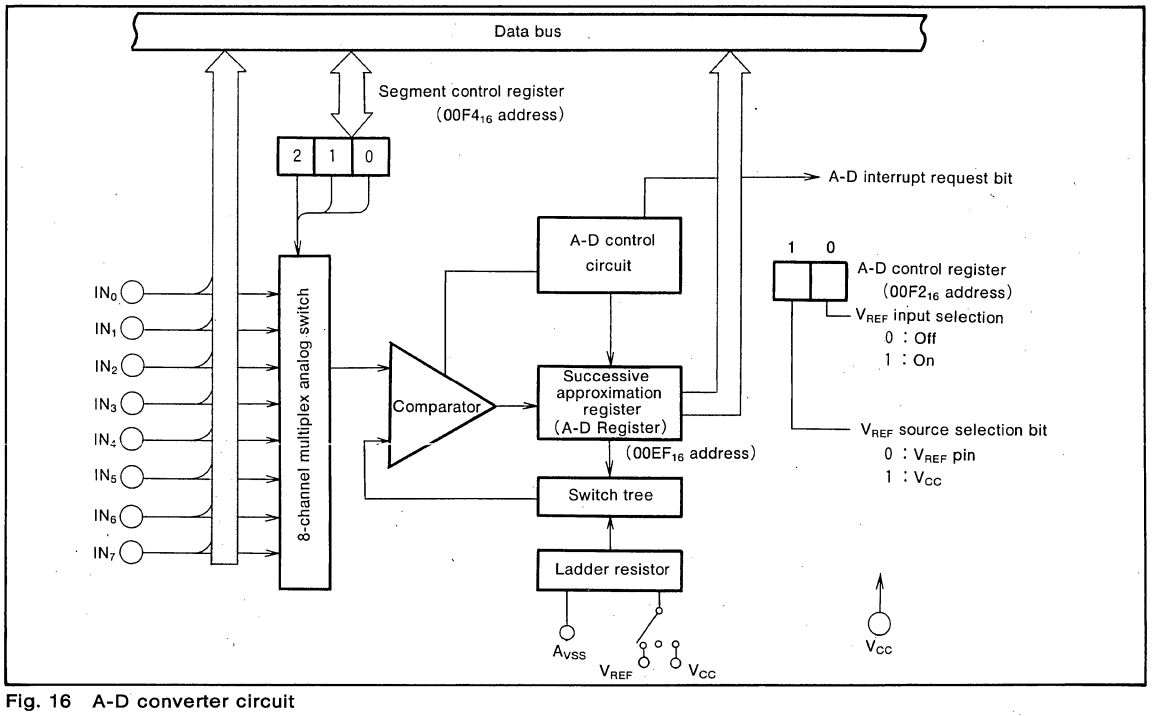


Fig. 16 A-D converter circuit

KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction.

When the key on wake up option of port P2 is designated and key on wake up interrupt enable bit (IC_2) is set to "1", if the key on wake up option pin of port P2 has "L" level applied, key on wake up interrupt is generated and the microcomputer is returned to the normal operating state.

When the bit 4 of PWM control register (address $00F3_{16}$) is set to "1", the pulse shown in Figure 18 is outputed from $P5_3$ pin.

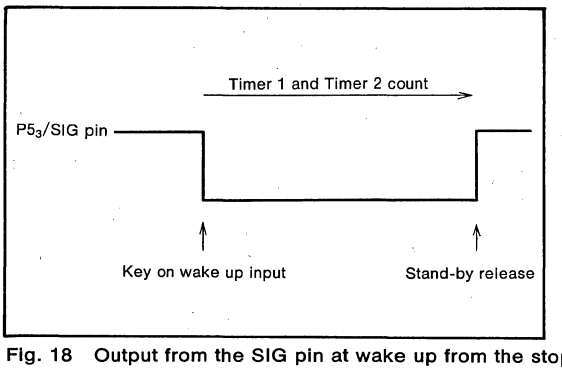


Fig. 18 Output from the SIG pin at wake up from the stop state

As shown in Figure 19, if the key matrix of active "L" to input port P2 is constructed, the microcomputer is returned to normal operating state by the key push. Refer to the section of intterrupt how to use the key on wake up function. In order to enter the power down state generated by the STP or WIT instruction at the interrupt disable flag (I) is "0" and IC_2 is "1", the input designated as key on wake up by option in port P2 must be all "H".

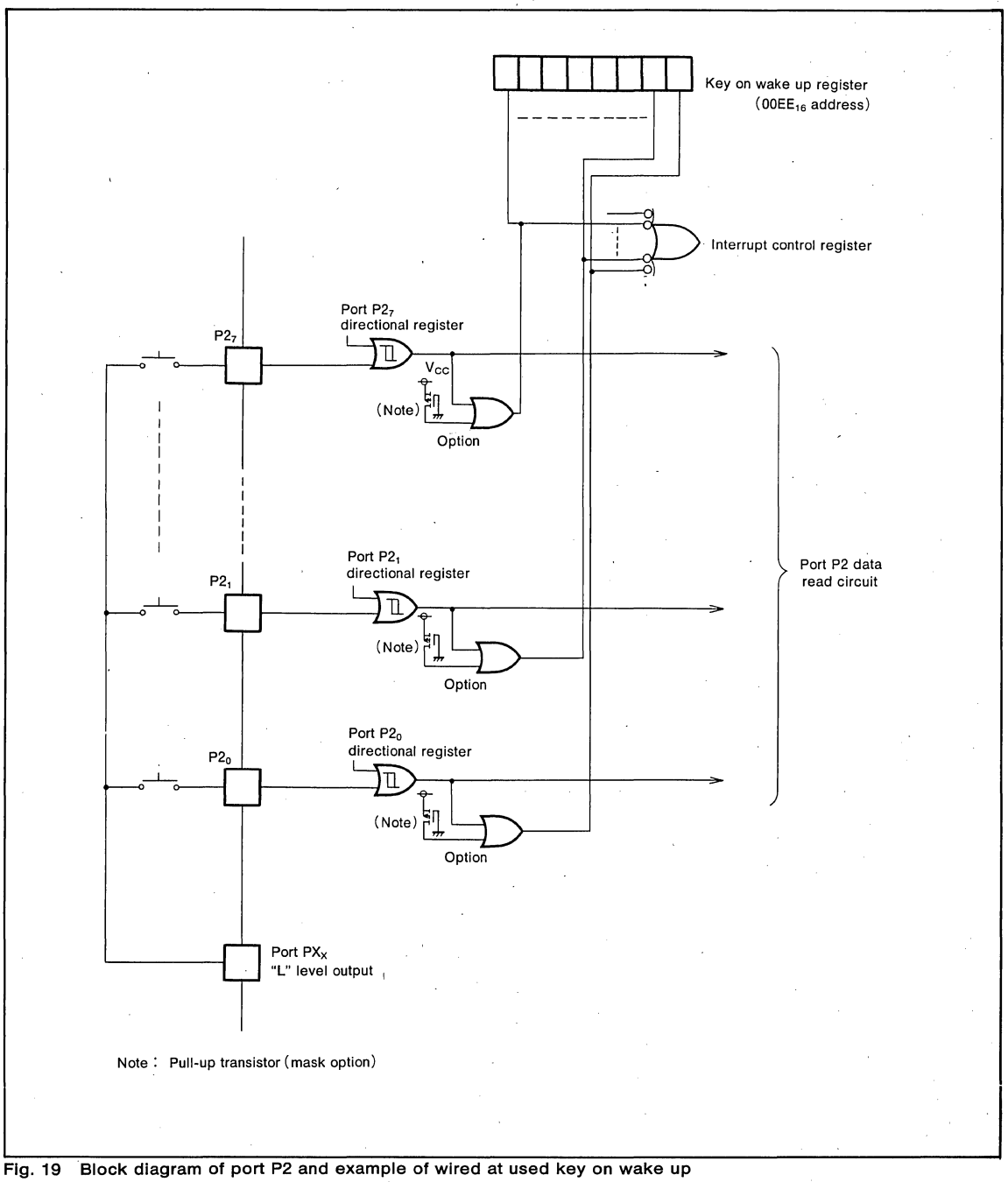


Fig. 19 Block diagram of port P2 and example of wired at used key on wake up

RESET CIRCUIT

The M37410M3-XXXFP is reset according to the sequence shown in Figure 22. It starts the program from the address formed by using the content of address $3FFF_{16}$ as the high order address and the content of the address $3FFE_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than 16 μs while the power voltage is between 4 and 5.5V and the crystal oscillator oscillation is stable and then returned to "H" level.

The internal initializations following reset are shown in Figure 20.

An example of the reset circuit is shown in Figure 21.

When the power on reset is used, the $\overline{\text{RESET}}$ pin must be input "H" after the oscillation of X_{IN}-X_{OUT} becomes stable.

	Address	
(1) Port P0 directional register	(D0) ($E1_{16}$)···	00_{16}
(2) Port P1 directional register	(D1) ($E3_{16}$)···	00_{16}
(3) Port P2 directional register	(D2) ($E5_{16}$)···	00_{16}
(4) Port P3 directional register	(D3) ($E9_{16}$)···	00_{16}
(5) Port P5 directional register	(D5) (ED_{16})···	00_{16}
(6) Interrupt request distinguish register 1	($F1_{16}$)···	00_{16}
(7) Interrupt request distinguish register 2	($F2_{16}$)···	00_{16}
(8) PWM control register	($F3_{16}$)···	0 0 0 0 0 0 0 0
(9) Segment control register	($F4_{16}$)···	0 0 0 0 0 – – –
(10) LCD mode register	($F5_{16}$)···	00_{16}
(11) Serial I/O mode register	(SM) ($F6_{16}$)···	– 0 0 0 0 0 0 0
(12) Timer 4, 5, 6 mode register	($F8_{16}$)···	00_{16}
(13) Interrupt control register	(IM) (FE_{16})···	00_{16}
(14) Timer control register	(TM) (FF_{16})···	00_{16}
(15) A-D control register	($F2_{16}$)···	0 0
(16) Processor status register		– – – – – 1 – –
(17) Program counter	(PC_H)···	Contens of address $3FFF_{16}$
	(PC_L)···	Contents of address $3FFE_{16}$

Note : Since the contents of both registers other than those listed above (including timers and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values.

Fig. 20 Internal state of microcomputer at reset

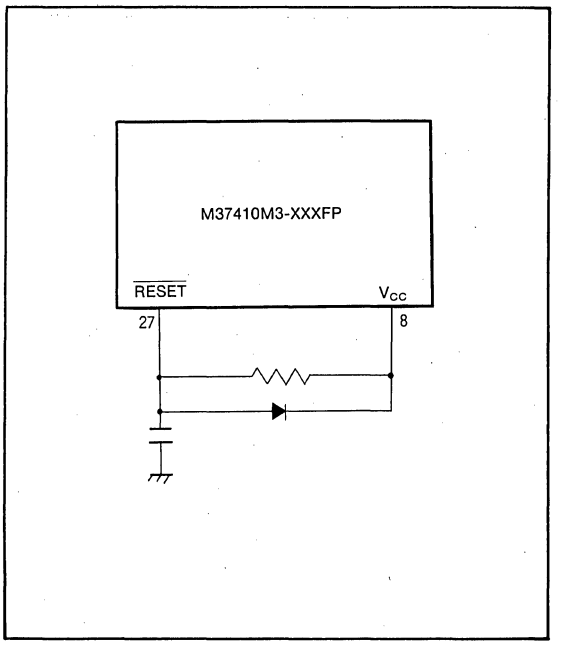


Fig. 21 Example of reset circuit

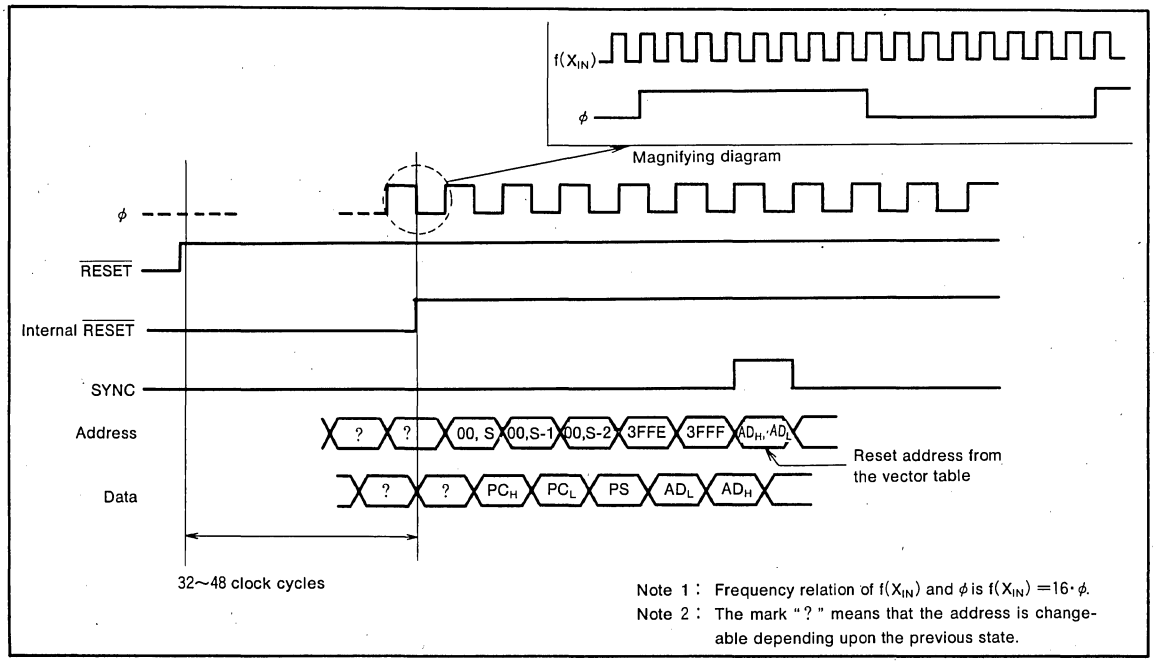


Fig. 22 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs and pull-up transistor options available. As shown in Figure 1, P0 can be accessed as memory through zero page address $00E0_{16}$. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address $00E1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port register and output. When data is read from the output port, the output pin level is not read, only the latched data of the port register is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

(2) Port P1

Port P1 has the same function as P0 but the output structure is N-ch open drain.

(3) Port P2

Port P2 has the same function as P0. Following the execution of STP or WIT instruction, key matrix with port P2 can be used to generate the interrupt to bring the microcomputer back in its normal state. The pin to be used as the key on wake up must be with key on wake up option and its value in directional register must be "0".

(4) Port P3

Port P3 has the same functions P0 except that part of P3 is common with the serial I/O, output of timer4, clock oscillation of timer clock and interrupt input.

The output is N-channel open drain. When $P3_0$ and $P3_1$ pins are used for X_{CIN} input, pull-up is inhibited.

(5) Port P4

Port P4 is an 4-bit input port which can be used as a segment output port. At reset, this port is pull-up to V_{L3}. Just after the reset, this port becomes high-impedance state. When port P4 is used as input port, the pull-up option to these pins are inhibits.

(6) Port P5

Port P5 has the same functions as P0 except that part of P5 is common with the counter input pin, SIG pin, and PWM output pin. The output is N-channel open drain output.

(7) Segment output(SEG_0~SEG_{11})

These ports drive and control the LCD segments. At reset, these output the level of V_{L3}.

(8) Analog input(IN_0~IN_7)

This is a port for an analog input of A-D converter. This can be used as the segment output. At reset, it is pull-up to V_{L3}. Just after the reset, this becomes high-impedance state.

(9) Common output(COM_0~COM_3)

These port provides output drive and control for the LCD common lines. At reset, this outputs the level of V_{L3}.

(10) Power Supply for LCD(V_{L1}~V_{L3})

Supplies power to the LCD terminals.

(11) INT_1

The INT_1 pin is an interrupt input pin. The INT_1 interrupt request bit (bit 7 of address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L" (or "L" to "H"). This input level is read in the bit 7 of serial I/O mode register (addresss $00F6_{16}$).

(12) INT_2($P3_2$/INT_2)

The INT_2 pin is an interrupt input pin common with $P3_2$. When $P3_2$'s directional register is set for input ("0"), this pin can be used as an interrupt input. The INT_2 interrupt request bit (bit 3 of address $00EB_{16}$) is automatically set to "1" when the input level of this pin changes from "H" to "L" (or from "L" to "H").

(13) INT_3($P5_0$/INT_3)

The INT_3 pin is an interrupt input pin common with $P5_0$. The other functions are the same as INT_2.

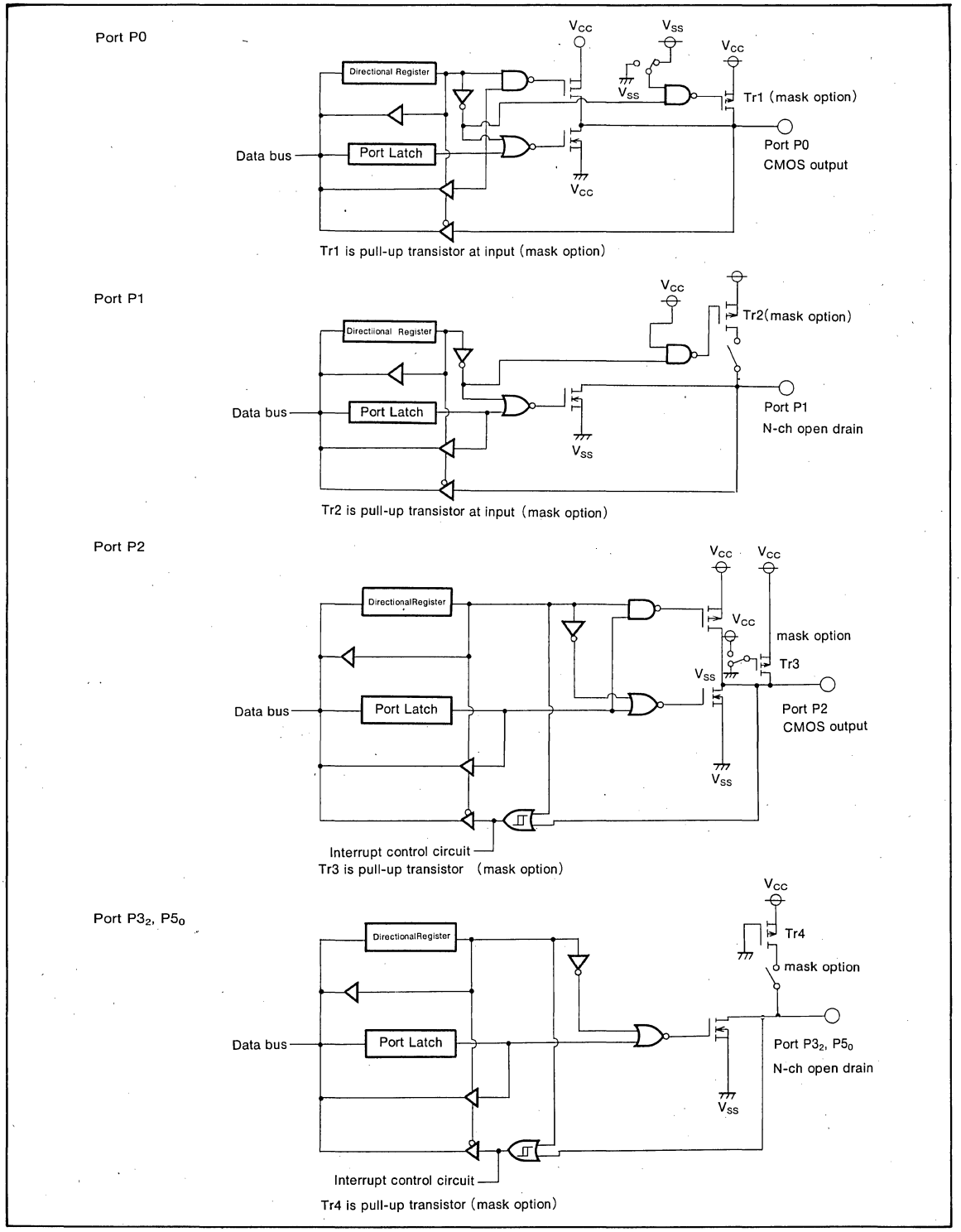


Fig. 23 Block diagram of ports P0~P2, $P3_2$ and $P5_0$

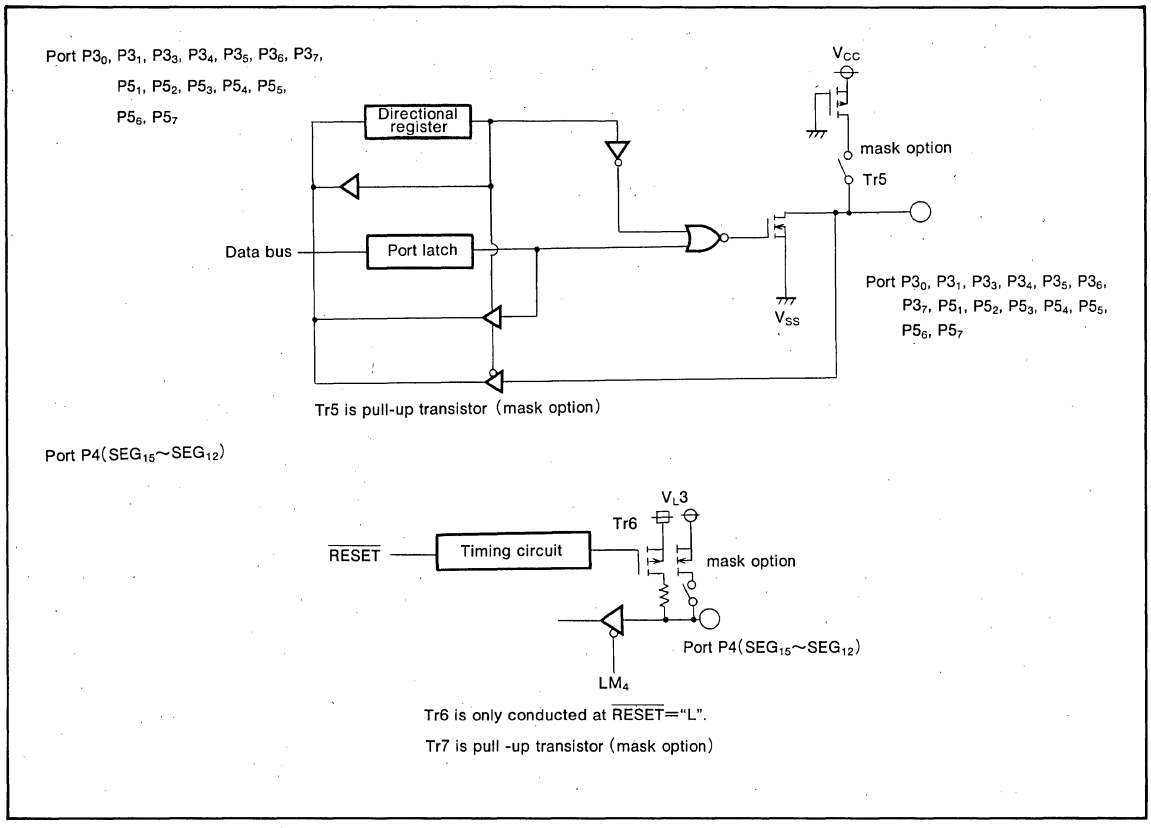


Fig. 24 Block diagram of Port P3 and P4

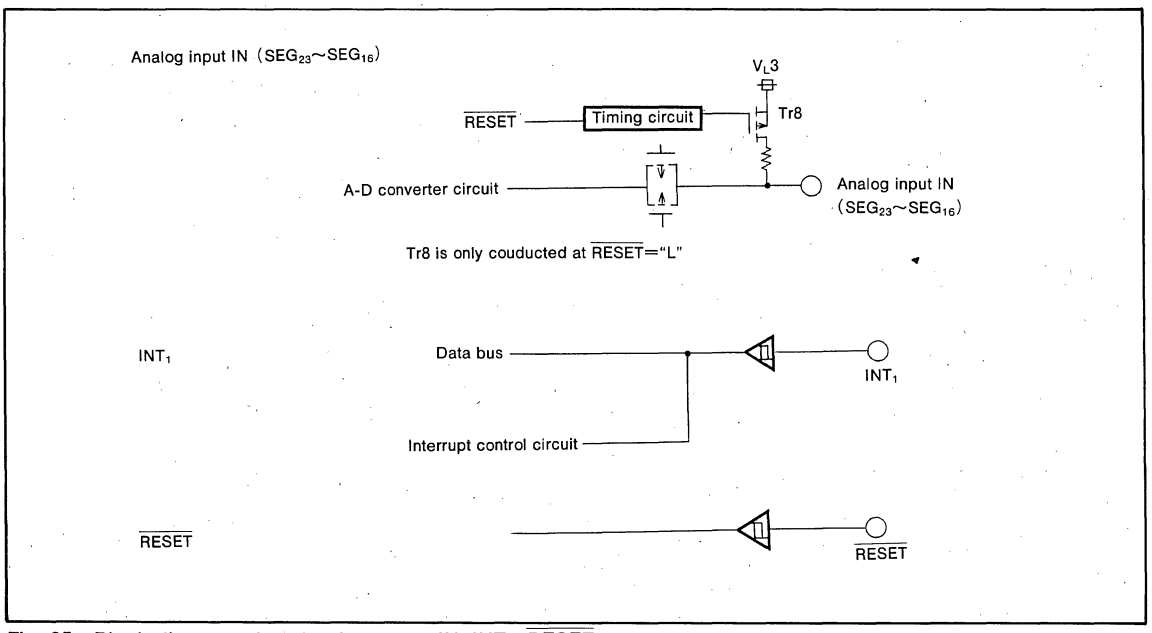


Fig. 25 Block diagram of analog input port IN, INT$_1$, RESET

CLOCK GENERATING CIRCUIT

The M37410M3-XXXFP has two internal clock generators. Figure 28 shows a block diagram of the clock generator. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output) ϕ. Serial I/O mode register bit 5 can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}. In this case, the pull-up option to these pins are inhibited.

These signals can also be changed via bit5 (LM_5) and bit6 (LM_6) of the LCD mode register. When LM_6 and LM_5 are [00], the internal clock is chosen $X_{IN}/16$. When they are [01], the internal clock is chosen $X_{IN}/4$. When they are [10] and [11], the internal clock is $X_{CIN}/2$. The one of clock X_{IN} and clock X_{CIN}, isn't in use for the internal clock (none system clock), stops when the bit6 (SM_6) of serial I/O mode register is "0". In order to restart the clock as the internal clock, SM_6 is set to "1" and wait until the oscillation becomes stability by the software then the internal clock is chosen LM_6 and LM_5.

Figure 26 shows a circuit exmple using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which is unique for each oscillator. when using an external clock signal, input from the X_{IN}(X_{CIN}) pin and leave the X_{OUT}(X_{COUT}) pin open. A circuit example is shown in Figure 27.

The M37410M3-XXXFP has two low power consumption modes, stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 1 and timer 2 are forcibly connected and $\phi/4$ is selected as timer 1 input. When restarting oscillation, set the suitable value for timer 1 and timer 2 in order to enable the oscillator to stabilize. Before executing the STP instruction, the timer 1 count stop bit must be set to supply ("0"), Timer 2 interrupt enable bit ($IF1_4$) of interrupt request distinguish register 1 must be set to enable ("1"), Timer 2 interrupt enable bit (TC_6) of timer control register must be set to disable ("0").

Oscillation is restarted (reset stop mode) when INT_1, INT_2, or INT_3 interrupt is received. The interrupt enable bit of the interrupt used to reset the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" until timer 2 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be applied to the $\overline{RESET}$ pin until the oscillation stabilizes because no wait time is generated.

The microcomputer enters a wait mode when WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode reset) when the processor is reset or when it receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

When the interrupt is accepted and after the interrupt subroutine is executed, the next instruction to STP or WIT is executed. It is possible to cancel stop and wait mode by reset. In this case, the execution is started from the address is set to reset vector.

Transition of states for the system clock is shown in Figure 29. The change order of the internal clock is shown in Figure 29.

When STP instruction is executed from the states of A, B, C, D and E, it will be the same state as H (stop state). If the interrupt is executed in stop state, it will return the state before STP instruction is executed.

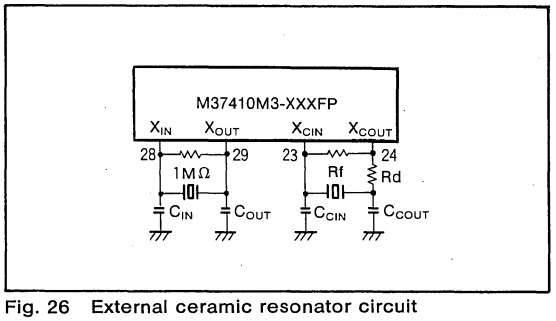


Fig. 26 External ceramic resonator circuit

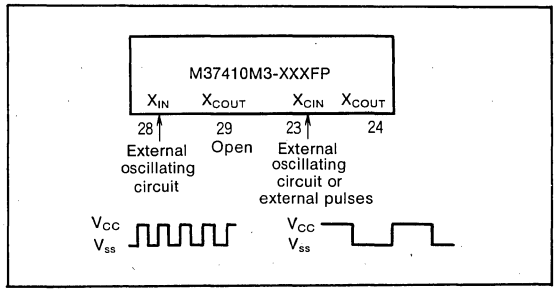


Fig. 27 External clock input circuit

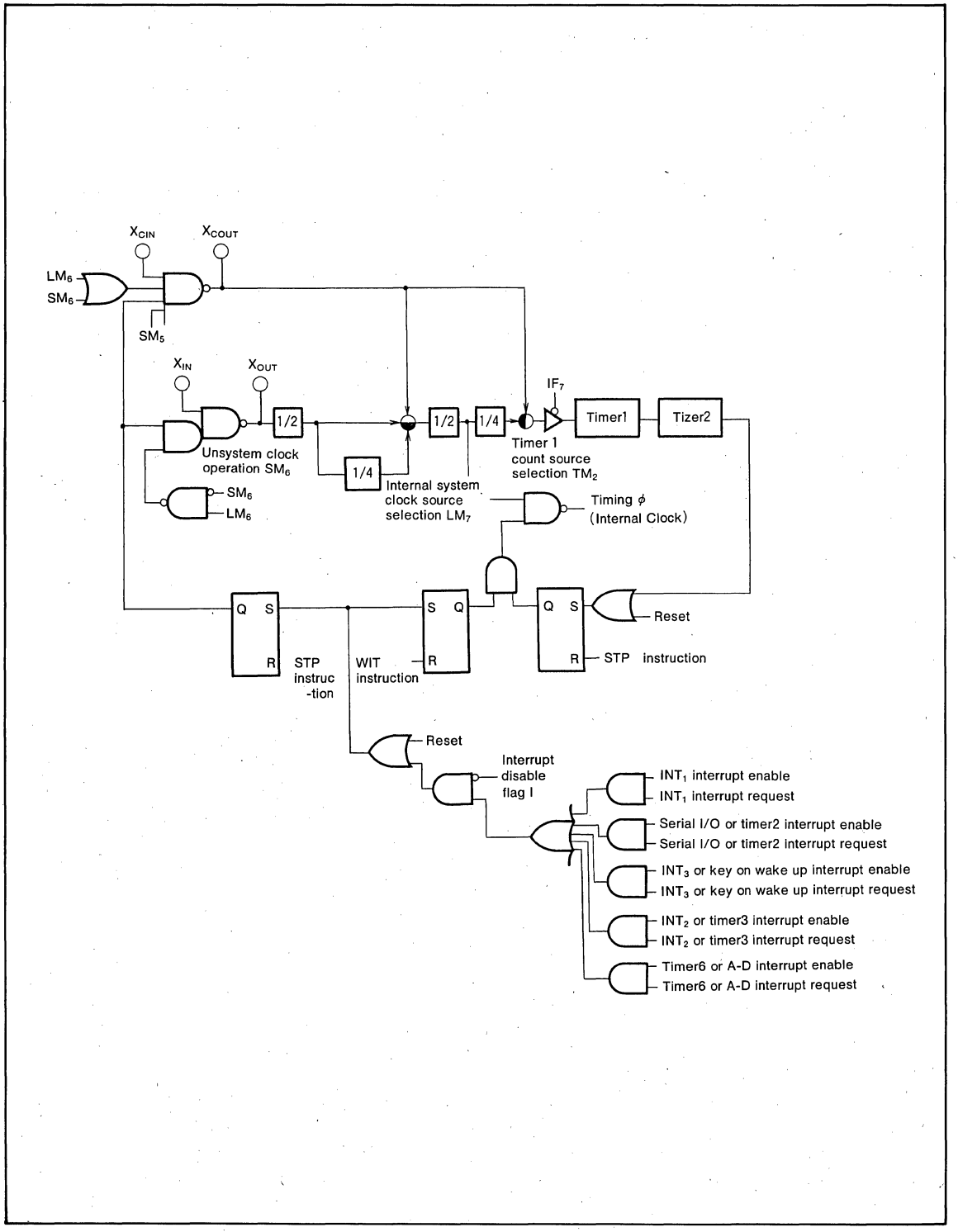
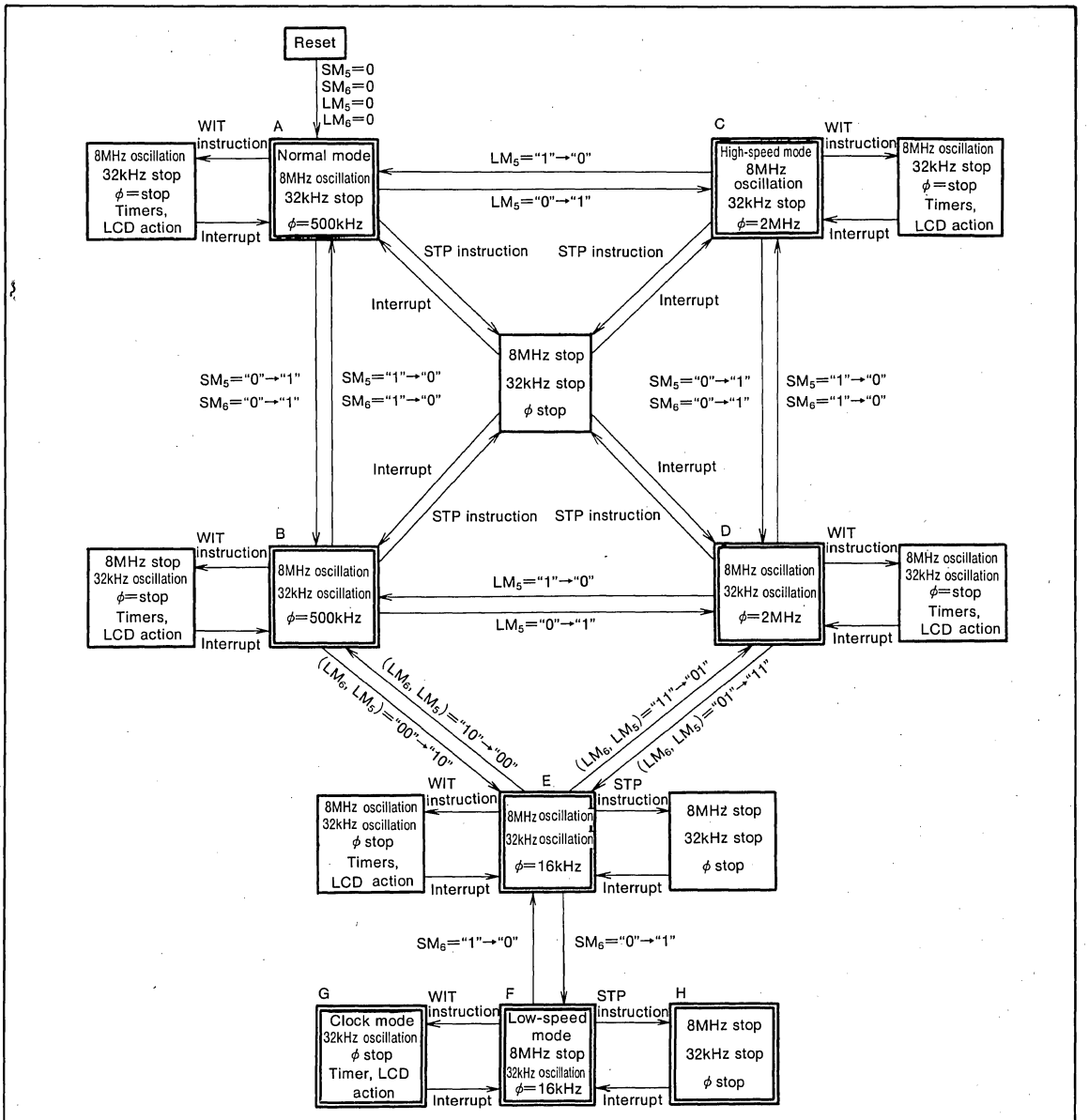


Fig. 28 Block diagram of clock generating circuit



The case of example clock X_{IN}=8MHz, clock X_{CIN}=32kHz.

Note : At the end of STP instruction, wait time occurs automatically by connection of timers 1 and 2 and changing system clock. This time is set by program.

When SM_6=1 and unsystem clock is operated, wait time necessary by program until oscillation becomes stable.

Return to the normal mode once in case changed to the low-speed mode from the normal mode.

Also return to the high-speed mode once in case changed to the low-speed mode from the high-speed mode.

Fig. 29 Transition of states for the system clock

PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those insructions are only valid for the contents before the modification. Also, at least one insturction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When the timer 4 and the timer 5 are used at event counter mode, read the contents of these timers either while the input of these timers are not changing or after timer 4, 5 count stop bit (bit 6 of address $00F8_{16}$) is set to "1".
Also, when the timer 1, timer 2, or timer 3 is input the clock except $\phi/4$ or it divided by timer, control the same as above.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the exection of a PLP instruction.

(6) When LCD trun-on bit (bit 3 of address $00F5_{16}$) of the LCD mode register is "1", don't stop the timers or count source for timers.

(7) The timer 1 and timer 2 must be set the necessary value immediately before the execution of a STP instruction.

(8) When the interrupt is processed, confirm the interrupt enable bit is enable state after into the interrupt routine. If so, check the request flag after that.

(9) The change of system clock of $X/16 \rightarrow X_C/2 \rightarrow X/4$ and $X/4 \rightarrow X_C/2 \rightarrow X/16$ are inhibited.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3sets

Write the following option on the mask ROM confirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port P4 pull-up transistor bit
- Port P5 pull-up transistor bit
- Port P2 key on wake up

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼7	V
V_I	Supply voltage for LCD V_{L1}∼V_{L3}	$V_{L1}<V_{L2}<V_{L3}$	−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P3_0$, $P3_1$, $P4_0$∼$P4_3$, IN_0∼IN_7, V_{REF}, X_{IN}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3∼7	V
V_I	Input voltage INT_1, $\overline{RESET}$, $P1_0$∼$P1_7$, $P3_2$∼$P3_7$, $P5_0$∼$P5_7$		−0.3∼10	V
V_O	Output voltage $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P3_0$, $P3_1$, COM_0∼COM_3, SEG_0∼SEG_{23}, X_{OUT}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P1_0$∼$P1_7$, $P3_2$∼$P3_7$, $P5_0$∼$P5_7$		−0.3∼10	V
P_d	Power Dissipation	T_a = 25℃	300	mW
Topr	Operating temperature		−20∼75	℃
Tstg	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=2.5∼5.5V, V_{SS}=0V, T_a=−20∼75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Nom.	Max.	
V_{CC}	Supply voltage (Note 1)	f(X_{IN})= 8 MHz High-speed mode (Note 2)	4.5		5.5	V
		f(X_{IN})= 8 MHz Low-speed mode or f(X_{IN})= 2 MHz High speed mode	2.5		5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P3_0$, $P3_1$, $P4_0$∼$P4_3$, X_{IN}, CNV_{SS} (Note 3)		0.7V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$∼$P2_7$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P1_0$∼$P1_7$, $P3_3$∼$P3_7$, $P5_1$∼$P5_7$, S_{IN}		0.7V_{CC}		10	V
V_{IH}	"H" input voltage $P3_2$, $P5_0$, INT_1, INT_2, INT_3, CNT_1, CNT_2, SIG, CLK		0.8V_{CC}		10	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0.85V_{CC}		10	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ $P3_3$∼$P3_7$, $P4_0$∼$P4_3$, $P5_1$∼$P5_7$, S_{IN}		0		0.3V_{CC}	V
V_{IL}	"L" input voltage $P2_0$∼$P2_7$, $P3_2$, $P5_0$, INT_1, INT_2, INT_3, CNT_1, CNT_2, SIG, CLK		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0		0.15V_{CC}	V
I_{OH}	"H" output current $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, X_{OUT} (Note 4)				−1	mA
I_{OL}	"L" output current $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$ $P5_0$∼$P5_7$, X_{OUT}, PWM0∼PWM3, T, S_{OUT}, CLK, $\overline{S_{RDY}}$, SIG (Note 5)				1	mA
I_{OL}	"L" output current $P1_0$∼$P1_7$ (Note 6)	V_{CC}=4.5∼5.5V			20	mA
f(X_{IN})	Clock oscillating frequency		0.2		8.2	MHz
f(X_{CIN})	Clock oscillating frequency for clock function		30		50	kHz

Note 1 When only maintaining the RAM data, minimum value of V_{CC} is 2V.
2 We say the high-speed mode, when the system clock is chosen X_{IN}/4, and the low-speed mode, when the system clock is chosen X_{IN}/16.
3 When $P3_1$ is used as X_{CIN}, V_{IH} and V_{IL} of $P3_1$ is $0.85V_{CC} \leqq V_{IH} \leqq V_{CC}$ and $0 \leqq V_{IL} \leqq 0.15V_{CC}$.
4 The total $I_{OH(peak)}$ of port P0, P2 and X_{OUT} is less than 35mA.
5 The total $I_{OH(peak)}$ of port P0, P2, P3 and P5 is less than 32mA.
6 The total peak current of I_{OL} of port P1 is less than 80mA and the average current of total I_{OL} of port P1 is less than 40mA.

ELECTRICAL CHARACTERICS (V_{SS}= 0 V, T_a=−20~75℃ f(X_{IN})= 8 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P2_0$~$P2_7$	V_{CC}=5V, I_{OH}=−0.5mA	4			V
		V_{CC}=3V, I_{OH}=−0.3mA	2.4			
V_{OH}	"H" output voltage X_{OUT}	V_{CC}=5V, I_{OH}=−0.3mA	4			V
		V_{CC}=3V, I_{OH}=−0.1mA	2.4			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$ $P5_0$~$P5_7$, T, S_{OUT}, CLK, $\overline{S_{RDY}}$, SIG, PWM0~PWM3	V_{CC}=5V, I_{OL}=1mA			1	V
		V_{CC}=3V, I_{OL}=0.5mA			0.6	
V_{OL}	"L" output voltage $P1_0$~$P1_7$	V_{CC}=5V, I_{OL}=20mA			2	V
		V_{CC}=3V, I_{OL}=10mA			1.5	
V_{OL}	"L" output voltage X_{OUT}	V_{CC}=5V, I_{OL}=0.3mA			1	V
		V_{CC}=3V, I_{OL}=0.1mA			0.6	
$V_{T+}-V_{T-}$	Hysteresis INT_1, INT_2, INT_3, CLK, CNT_1, CNT_2, SIG, S_{IN}, $P2_0$~$P2_7$,X_{CIN}	V_{CC}=5V		0.7		V
		V_{CC}=3V		0.5		
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5V		2		V
		V_{CC}=3V		1.2		
$V_{T+}-V_{T-}$	Hysteresis X_{IN}	V_{CC}=5V		0.5		V
		V_{CC}=3V		0.35		
I_{IL}	"L" input current {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$} without pull-up T_r (Note 1), IN_0~IN_7, INT_1, $\overline{RESET}$, X_{IN}	V_{CC}=5V V_I=0V			−5	μA
		V_{CC}=3V V_I=0V			−3	
I_{IH}	"H" input current $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$ $P4_0$~$P4_7$, IN_0~IN_7, X_{IN}, X_{CIN}, CNV_{SS}	V_{CC}=5V V_I=5V			5	μA
		V_{CC}=3V V_I=3V			3	
I_{IH}	"H" input current {$P1_0$~$P1_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$} without pull-up T_r, INT_1, INT_2, INT_3, CNT_1, CNT_2, SIG, $\overline{RESET}$, S_{IN}, CLK	V_I=10V			10	μA
R_{PL}	Pull-up T_r, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$	V_{CC}=5V, V_I=0V	35	70	140	kΩ
		V_{CC}=3V, V_I=0V	60	120	240	
R_{COM}	Output impedance COM_0~COM_3	V_{L1}=V_{CC}/3, V_{L2}=2V_{L1}, V_{L3}=V_{CC}, Other COM, SEG pins are opend. V_{CC}=5V		200		Ω
		V_{CC}=3V		500		
R_S	Output impedance SEG_0~SEG_{23}	V_{CC}=5V		2		kΩ
		V_{CC}=3V		3		
I_{CC}	Supply current — at operation	f(X_{IN})=8MHz High-speed mode V_{CC}=5V		6		mA
		f(X_{IN})=32kHz, V_{CC}=3V		18		μA
	— at wait mode	f(X_{IN})=32kHz, V_{CC}=3V		4		μA
	— at stop mode	T_a=25℃		0.1		
V_{RAM}	RAM retention voltage		2		5.5	V

Note 1 : Also the same when each port is used as INT_2, INT_3, CNT_1, CNT_2, SIG, S_{IN} and X_{CIN}, respectively.

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

M37415M4-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37415M4-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 80-pin plastic molded QFP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

This microcomputer is also suitable for applications which require controlling LCDs and generating DTMF.

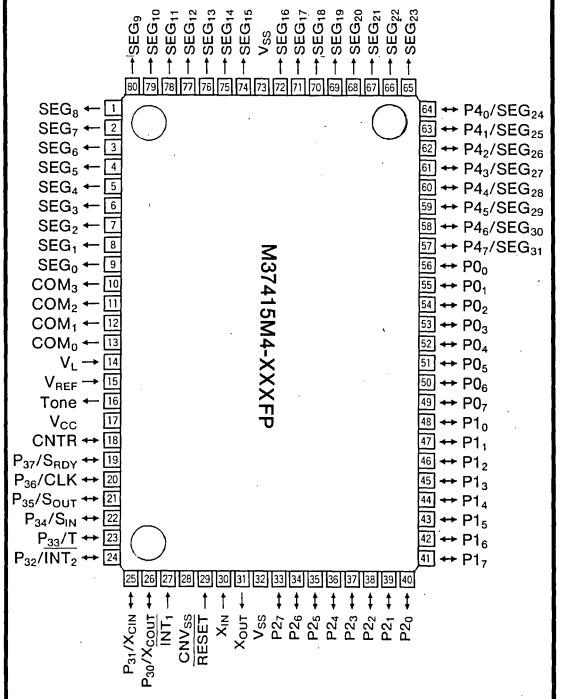
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size
  - ROM ..... 8192 bytes
  - RAM ..... 512 bytes
  - RAM for display LCD ..... 16 bytes
- Instruction executing time
  - minimum instructions, at 3.2 MHz frequency ..... 2.5 μs
  - minimum instructions, at 1.6MHz frequency 5μs
  - minimum instructions, at 800kHz frequency ..... 10 μs
  - minimum instructions, at 400kHz frequency 20μs
- Single power supply
  - $f(X_{IN})$=400kHz, or 800kHz ..... $2.5 \leqq V_{CC} \leqq 5.5V$
  - $f(X_{IN})$=1.6MHz, or 3.2MHz ..... $4.5V \leqq V_{CC} \leqq 5.5V$
- Power dissipation
  - normal operation mode (at 3.2MHz frequency)
    - ···4.0mA (DTMF output V_{CC}=5.0V typ.)
    - ···3.0mA (DTMF off V_{CC}=5.0V typ.)
  - low-speed operation mode (at 32kHz frequency for clock function)
    - ···45μA (V_{CC}=5.0V typ.)
  - stop mode (at 25℃) ..... 1μA (max.)
- RAM retention voltage (stop mode) ..... $2V \leqq V_{RAM} \leqq 5.5V$
- Subroutine nesting ..... 64 levels (max.)
- Interrupt ..... 8 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as serial I/O)
- 16-bit timer ..... 1 (Two 8-bit timers makes one set)
- Programmable I/O ports
  - (Ports P0, P1, P2, P3) 32
- Input port (Port P4) 8
- Serial I/O (8-bit) 1
- DTMF (Dual-Tone Multi-Frequency) generator ··· Built-in
- LCD controller/driver
  - (1/2, 1/3, bias, 1/2, 1/3, 1/4 duty)
  - segment output 32
  - common output 4
  - resistor for LCD power supply ..... Built-in
- Two clock generator circuits (One is for main clock, the other is for clock function.)

APPLICATION

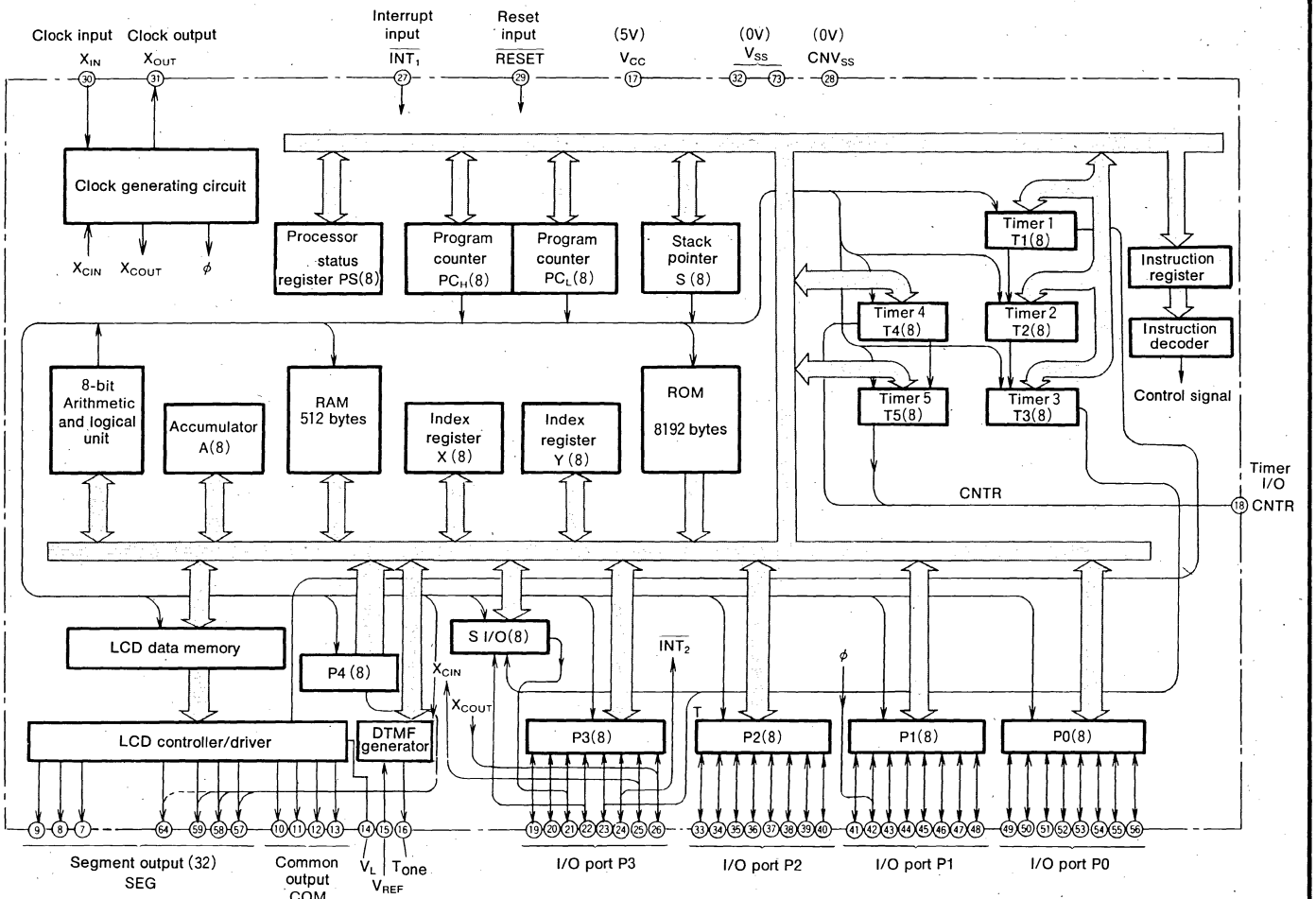
Home telephone, Multi function telephone

PIN CONFIGURATION (TOP VIEW)



Outline 80P6

M37415M4-XXXFP BLOCK DIAGRAM



Note 1 : Program counter PC_H is only 6 bits long.

FUNCTIONS OF M37415M4-XXXFP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2.5μs (minimum instructions, at 3.2MHz frequency) 5μs (minimum instructions, at 1.6MHz frequency) 10μs (minimum instructions, at 800kHz frequency) 20μs (minimum instructions, at 400kHz frequency)
Clock frequency			3.2MHz, 1.6MHz, 800kHz, 400kHz
Memory size	ROM		8192 bytes
	RAM		512 bytes
	RAM for display LCD		16 bytes
Input/Output ports	P0, P1, P2, P3	I/O	8-bit×4
	P4	Input	8-bit×1 (Port P4 are in common with SEG)
	SEG	LCD output	32-bit×1
	COM	LCD output	4-bit×1
Serial I/O			8-bit×1
Timers			8-bit timer×3 (×2, when serial I/O is used)
			16-bit timer×1 (combination of two 8-bit timers)
LCD controller/driver	Bias		1/2, 1/3, bias selectable
	Duty ratio		1/2, 1/3, 1/4 duty selectable
	Common output		4
	Segment output		32(SEG_{24}~SEG_{31} are in common with port P4)
Subroutine nesting			64 (max.)
Interrupt			Two external interrupts, Three timer internal interrupts (or two timer, one serial I/O)
Clock generating circuit			Two built-in circuits (ceramic or quartz crystal oscillator)
Supply voltage			2.5~5.5V (RAM retention voltage at clock stop is 2~5.5V)
Power dissipation	DTMF output	At high-speed operation V_{CC}=5V	20mW (at clock frequency f(X_{IN})=3.2MHz)
	DTMF off	At high-speed operation V_{CC}=5V	15mW (at clock frequency f(X_{IN})=800kHz)
		At low-speed operation V_{CC}=5V	255μW (at clock frequency f(X_{CIN})=32kHz)
		At stop mode	5μW (max. 25℃)
Input/Output characteristics	Input/Output voltage		5V
	Output current		I_{OH}=−2mA(V_{OH}=3V)
			I_{OL}=10mA(V_{OL}=2V)
			Pull-up current : Min.−30μA, Max.−140μA, Typ. −70μA (V_{CC}=5V input voltage 0V)
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package			80-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage input		Power supply inputs 5V±10% to V_{CC} and 0V to V_{SS}.
CNV_{SS}	CNV_{SS} input		Connect to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$, $P3_2$, $P3_1$, and $P3_0$ work as timer 3 overflow signal divided by 2 output pin (T), $\overline{INT_2}$ pin, X_{CIN} and X_{COUT} pins, respectively.
$P4_0$~$P4_7$	Input port P4	Input	Port P4 is an 8-bit input port and can be used as segment output pins.
V_L	Voltage input for LCD	Input	This is a voltage input pin for LCD. Supply voltage is $0V \leqq V_L \leqq V_{CC}$. 0V~$V_{LV}$ is supplied to LCD.
COM_0~ COM_3	Common output	Output	These are the LCD common output pins. At 1/2 duty, COM_2 and COM_3 pins are not use. At 1/3 duty, COM_3 pin is not used.
SEG_0~ SEG_{23}	Segment output	Output	These are LCD segment output pins.
CNTR	Counter I/O	I/O	This is an output pin for timer 4 and 5.
V_{REF}	D-A convert power supply for DTMF		Reference voltage input for A-D converter of DTMF.
Tone	DTMF output	Output	This is DTMF output pin.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M37415M4-XXXFP is shown in Figure 1. Addresses 2000_{16} to $3FFF_{16}$ are assigned for the built-in ROM area which consists of 8192 bytes. Addresses $3F00_{16}$ to $3FFF_{16}$ are a special address area (special page). By using the special page addressing mode of JSR instruction, subroutines address on this page can be called with only 2 bytes. Addresses $3FF4_{16}$ to $3FFF_{16}$ are vector addresses used for the reset and interrupts (see interrupts chapter).

Address 0000_{16} to $00FF_{16}$ are the zero page address area. By using zero page addressing mode, this area can also be accessed with 2 bytes. The use of these of these addressing methods will greatly reduce the object size required.

The RAM, I/O port, timer, etc. addresses are already assigned for the zero page. Addresses 0000_{16} to $007F_{16}$ and 0100_{16} to $027F_{16}$ are assigned for the built-in RAM which consists of 512 bytes. This RAM is used as the stack during subroutine calls and interrupts, in addition to data storage.

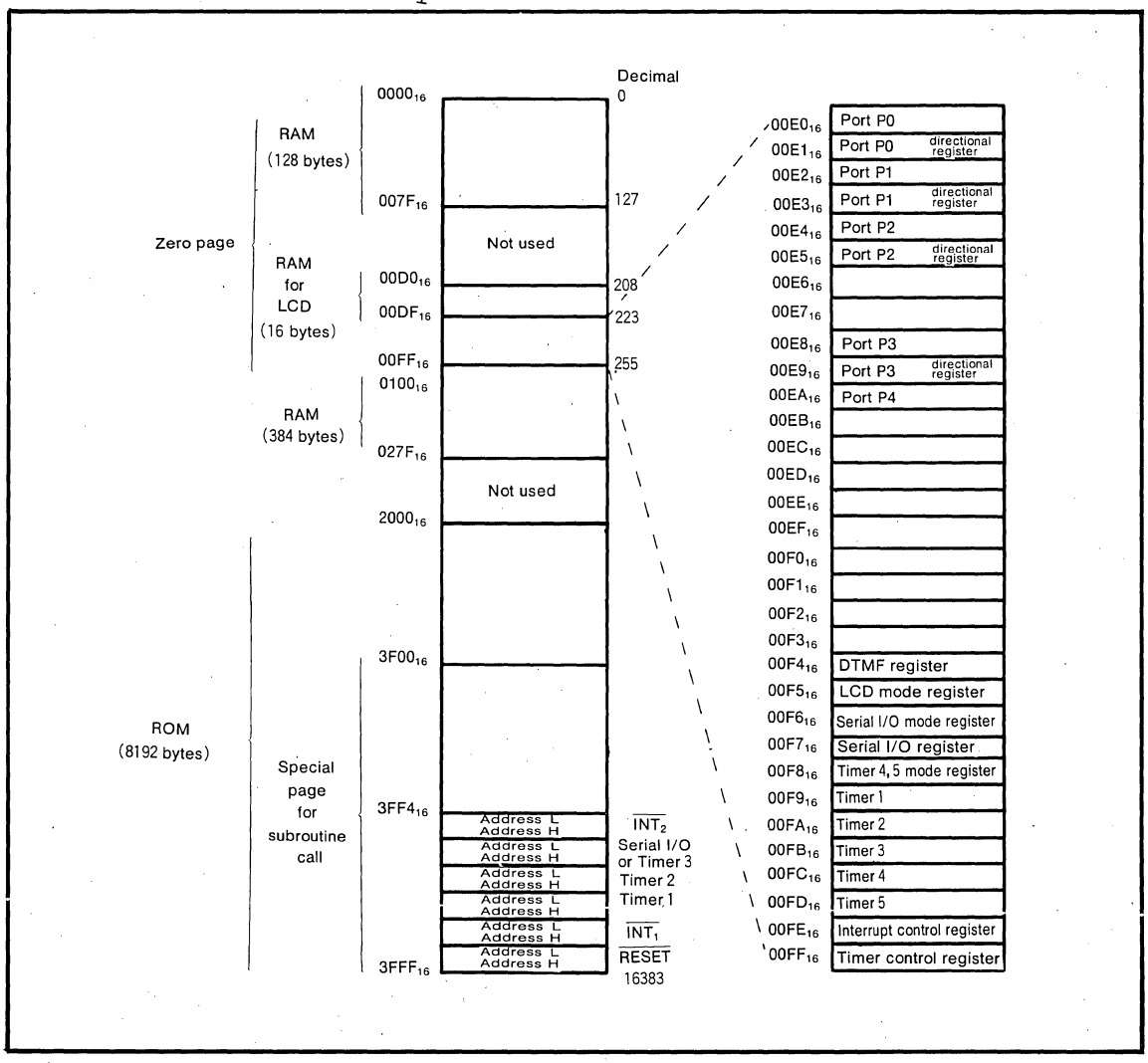


Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers are shown in Figure 2.

ACCUMULATOR(A)

The 8-bit accumulator A is the main register of the microcomputer. Data operations such as data transfer, input/output, etc., is executed mainly through the accumulator.

INDEX REGISTER X(X)

The index register X is an 8-bit register. In the index register X addressing mode, the value of the OPERAND added to the contents of the index register X speifies the real address. When the T flag in the processors status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y(Y)

The index register Y is an 8-bit register. In the index register Y addressing mode. the value of the OPERAND added to the contents of the index register Y specifies the real address.

STACK POINTER(S)

The stack pointer is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subrotine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

When an interrupt occurs, the higher 8 bits of the program counter is pushed into the stack first, the stack pointer is decremented, and then the lower 8 bits of the program counter is pushed into the stack. Next the contents of the processor status register is pushed into the stack. When the return from interrupt instruction (RTI) is executed, the program counter and processor status register data is popped off the stack it reverse order from above.

The accumulator is never pushed into the stack automatically, so a Push Accumulator instruction (PHA) is provided to execute this function. Restoring the accumulator to its previous value is accomplished by the Pop Accumulator instruction (PLA). It is executed in the reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed and popped to and from the stack with the PHP and PLP instructions, respectively.

During a subroutine call, only the Program Counter is pushed into the stack, Therefore, any registers that should not be destroyed should be pushed into the stack manually. To return from a subrotine call, the RTS instruction is used.

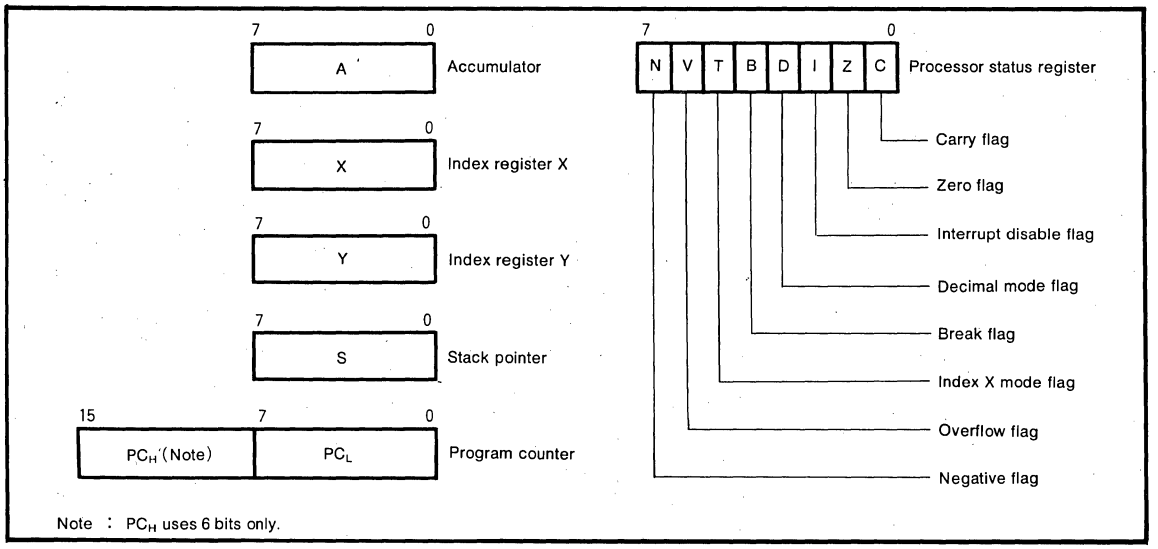


Fig.2 Register structure

MITSUBISHI ELECTRIC

PROGRAM COUNTER(PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.
PC_H is only 6 bits long.

PROCESSOR STATUS REGISTER(PS)

The 8-bit PS is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Nagative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic Logic Unit (ALU) immediately after an opration. It is also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate opration generated a zero result or not. If the result is zero, the zero flag will be set to"0". If the result is not zero, the zero flag will be set to "1".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt is accepted, this flag is automatically set to "1" to prevent from other interrupts until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is "0", the operations are executed in binary. Decimal, correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the B flag will be "1", otherwise, it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the memorry 1). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the T flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as signed binary number. When the result exceeds $+127$ or -128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the V flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or opration is negative (bit 7 is "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the N flag. There are no instructions for directly setting or resetting the N flag.

INTERRUPT

The M37415M4-XXXFP can be interrupted from eight sources; $\overline{INT_1}$, Timer 1, Timer 2, Timer 3 or Serial I/O, $\overline{INT_2}$ or key on wake up, and BRK inctruction.

The value of bit 2 of the serial I/O register (address $00F6_{16}$) determines whether the interrupt is from timer 3 or from serial I/O. When the bit 2 is "1" the interrupt is from serial I/O, and when bit 2 is "0" the interrupt is from timer 3. Also, when bit 2 is "1", parts of port 3 are used for serial I/O. Bit 7 of the serial I/O register determines if an interrupt is from $\overline{INT_2}$ or from "key on wake up". When bit 7 is "0", the interrupt is from $\overline{INT_2}$. When bit 7 is "1" the interrupt is from "key on wake up". "key on wake up" can only be used at power down by the STP or WIT instruction. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as interrupt.

Table 1 Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$3FFF_{16}$, $3FFE_{16}$
$\overline{INT_1}$	2	$3FFD_{16}$, $3FFC_{16}$
Timer 1	3	$3FFB_{16}$, $3FFA_{16}$
Timer 2	4	$3FF9_{16}$, $3FF8_{16}$
Timer 3 or serial I/O	5	$3FF7_{16}$, $3FF6_{16}$
$\overline{INT_2}$ or key on wake up(BRK)	6	$3FF5_{16}$, $3FF4_{16}$

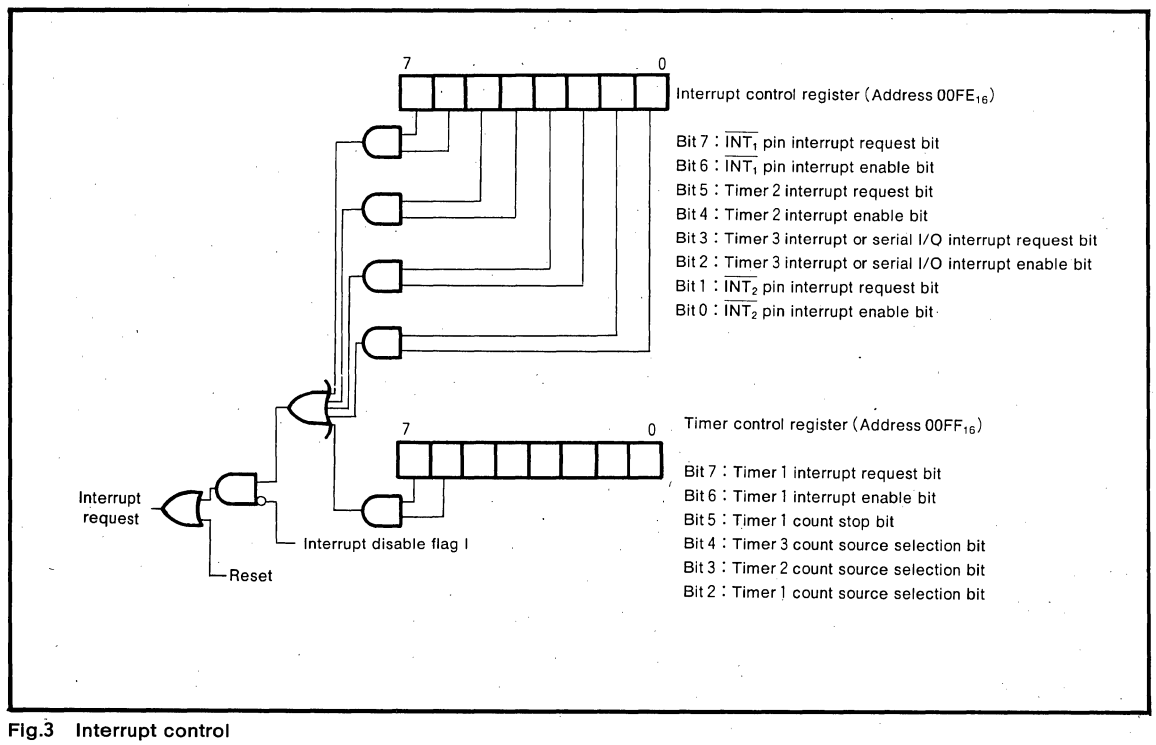


Fig.3 Interrupt control

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, as discussed in the stack pointer section, and the interrupt disable flag (I) is set, and the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Expect for the reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts except key on wake up function can further be controlled individually via the interrupt control register shown in Figure 3 An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0". The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins goes from "H" to "L"
(2) When the levels any pin of P2 goes "L" (at power down mode)
(3) When the contents of timer 1, timer 2, timer 3 or the counter of serial I/O goes to "0"

These request bits can be reset by a program but can not be set.

Since the BRK instruction interrupt and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt of if $\overline{INT_2}$ generated the interrupt.

TIMER

The M37415M4-XXXFP has five timers; timer 1, timer 2, timer 3, timer 4, and timer 5. The interrupt of timer 3 cannot be used when serial I/O is used (see serial I/O section). The count source for timer 1, timer 2, timer 3 can be selected by using bit 2, 3 and 4 of the timer control register (address $00FF_{16}$), as shown in Figure 5. A block diagram of timer 1 through 5 is shown in Figure 4. All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timers is $1/(n+1)$, where n is the contents of timer latch.

The timer interrupt request bit is set at the next count pulse after the timer reaches "0". The interrupt and timer control registers are located at addresses $00FE_{16}$, and $00FF_{16}$, respectively (see interrupt section). The starting and stopping of timer 1 is controlled by bit 5 of the timer control register. If bit 5 (address $00FF_{16}$) is "0", the timer starts counting. When bit 5 is "1", the timer stops.

After a STP instruction is executed, timer 2, timer 1, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 though 4 of the timer control register). This state is canceled if timer 2 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 5 of the timer control register (timer 1, count stop bit), bit 6 of the timer control register (timer 1 interrupt enable bit), and bit 4 of interrupt control register (timer 2 interrupt enable bit) must be set to "0". For more details on the STP instruction, refer to the oscillation circuit section.

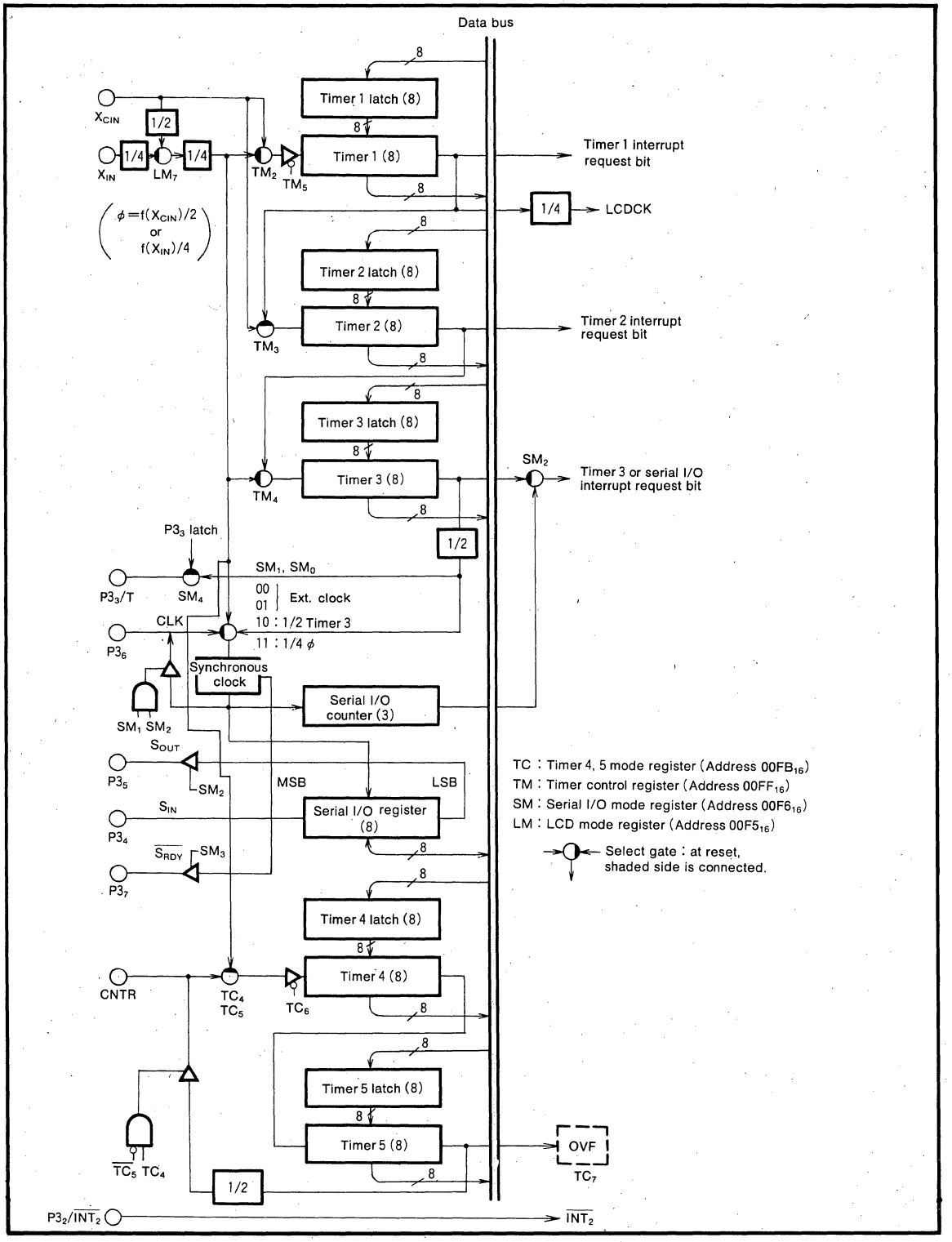


Fig.4 Block diagram of timers 1 through 5

MITSUBISHI ELECTRIC

TIMER 4 AND TIMER 5 MODES

(1) Timer mode [00].
The internal clock divided by 4 is counted. When the timer counts to "0", the interrupt request bit is set to "1", the contents of the timer latch is reloaded, and the counting starts again.

(2) Pulse output mode [01].
The output level of the CNTR pin inverts each timer the timer contents to zero.

(3) Event counter mode [10].
The same function is executed as that of mode "00", except that the counting source is input from the CNTR pin. The count decreased each time the CNTR input goes from "L" to "H".

(4) Pulse width measurement mode [11].
This mode is used to measure the pulse width of a signal (between "L"s) input into the CNTR pin. The counting is done using the oscillation frequency divided by 4, and only while the CNTR pin is at a low level. When the contents of the counter reaches zero, the timer 5 overflow flag is set to "1", the timer is reloaded from the reload latch, and counting starts again. The overflow flag can be reset by writing a "0" to bit 7 of address $00F8_{16}$.
The structure of timer 4, 5 mode register is shown in Figure 6.

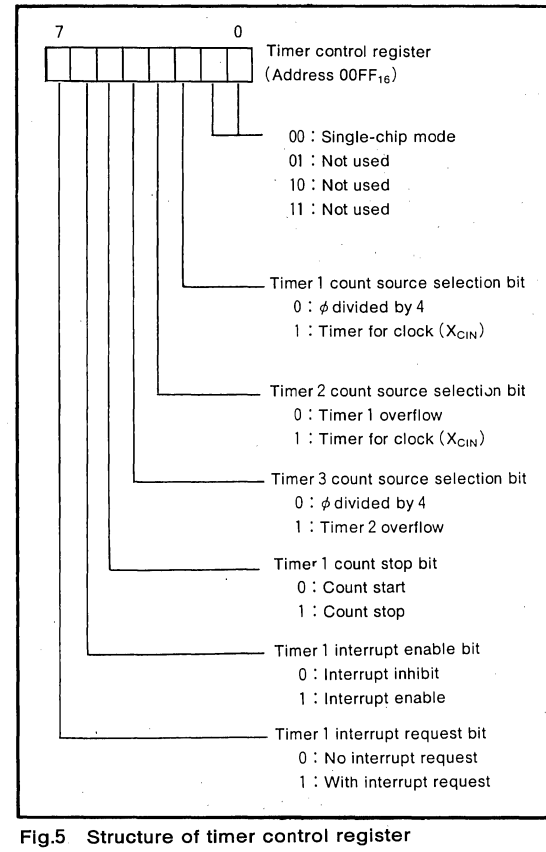


Fig.5 Structure of timer control register

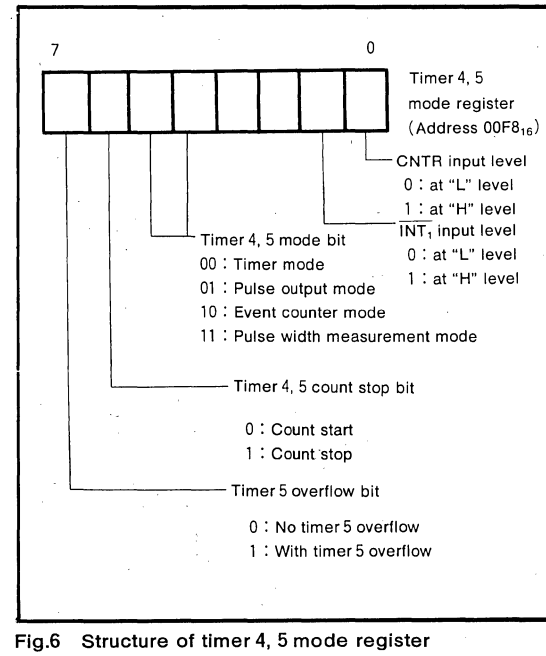


Fig.6 Structure of timer 4, 5 mode register

PORT $P3_3$/TIMER 3 OUTPUT

The signal that timer 3 is divided by 2 is output from $P3_3$ (T), at the contents of bit 4 of the serial I/O mode register (address $00F6_{16}$) is "1".

WATCHDOG TIMER FUNCTION

Timer 4 and 5 can be used as a watchdog timer by connecting the CNTR pin and the $\overline{\text{RESET}}$ pin as shown in Figure 7, and by setting bit 4 and 5 of address $00F8_{16}$ to "01". At this time the output of the 1/2 divider counter (connected to timer 5) is initialized to "1" when data is written to timer 5. After a delay of 12.5 to 15.0μs (at $f(X_{IN})$ =800kHz) after the reset is input, bits 4,5 and 6 of the timer 4,5 mode register are initialized to "0". The initialization program to set the watchdog timer mode should have the following sequence;

(1) Set the pulse output mode after writing a value to timer 4 and 5 registers.

(2) If the program is running correctly, the CNTR pin should never go low due to data being continuously written to timer 5. If the program sequence is interrupted timer 5 will overflow and the CNTR pin will output a "L" and retain this value until the reset is executed.

(3) 12.5 to 17.5μs (at $f(X_{IN})$ = 800kHz) after a reset, the CNTR pin will be in high impedance state.

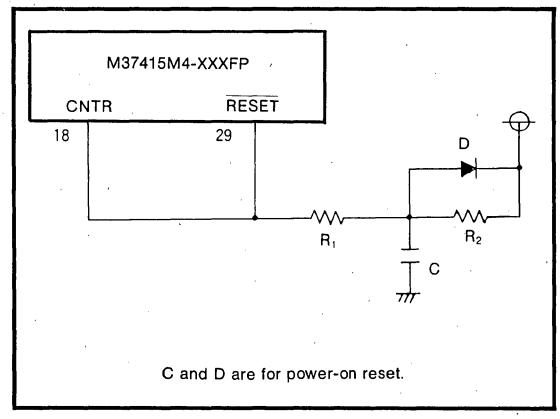


Fig.7 Reset circuit with the watchdog timer

SERIAL I/O

The block diagram of serial I/O is shown in Figure 8. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK), and the serial I/O (S_{OUT}, S_{IN}) pins are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F6_{16}$) is an 8-bit register. Bit 0 and 1 of this register is used to select a synchronous clock source. When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal divided by two from timer 3 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 becomes the clock.

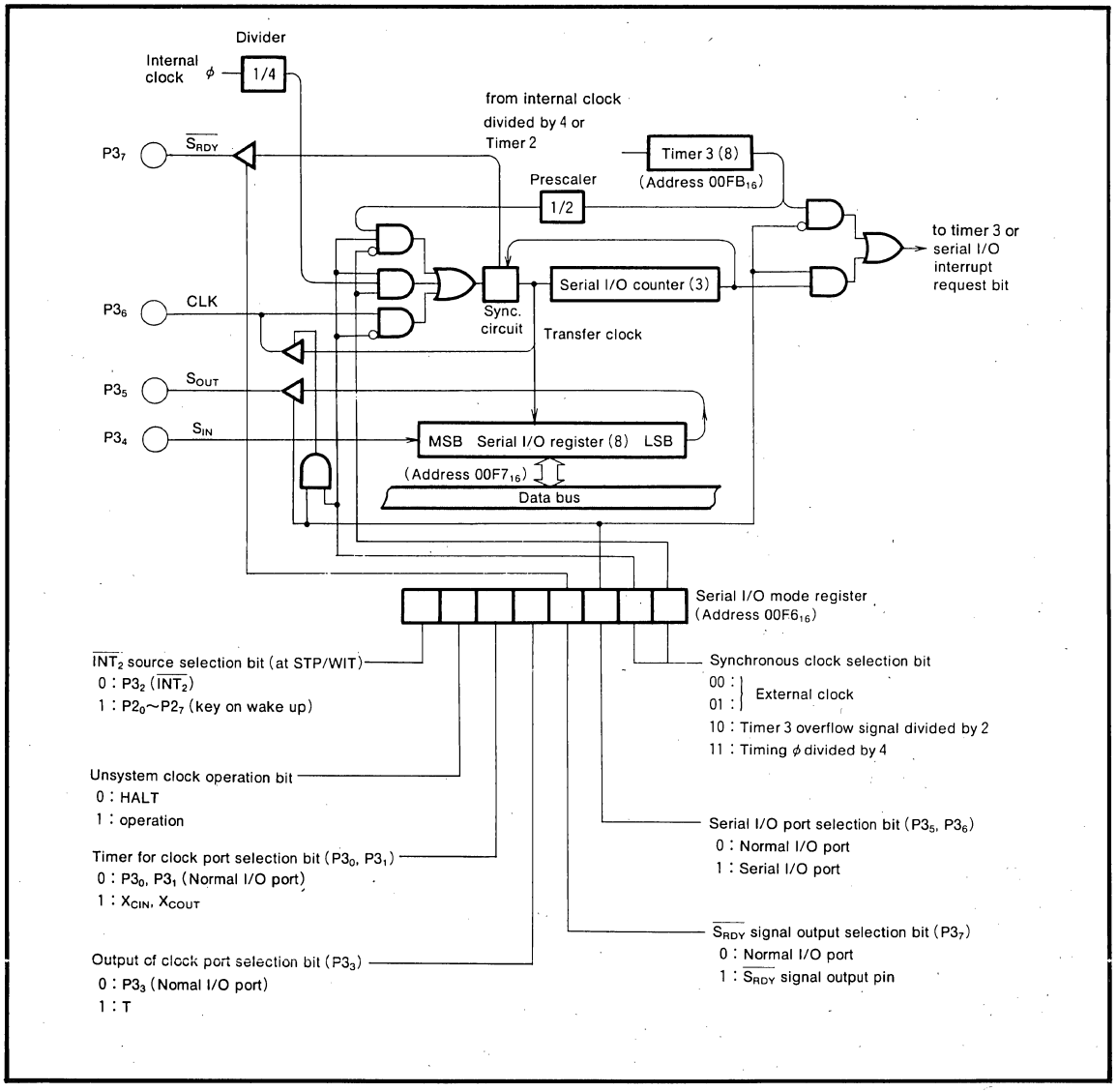


Fig.8 Block diagram of serial I/O

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If the external synchronous clock is selected, the clock is input to $P3_6$. And $P3_5$ will be a serial output, and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 3. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 3="0").

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock- The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the faling edge of write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37415M4-XXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock- If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 50kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 9, and connection between two M37415M4-XXXFP's are shown in Figure 10.

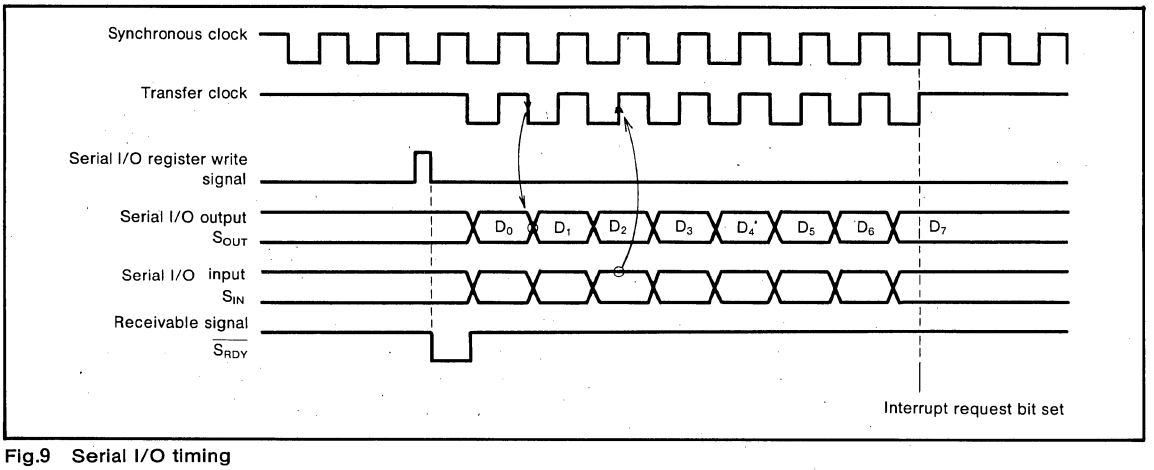


Fig.9 Serial I/O timing

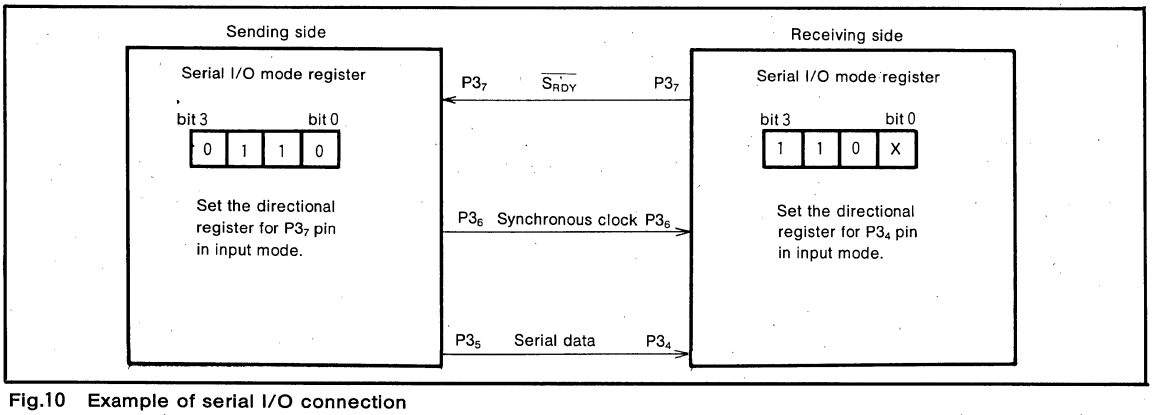


Fig.10 Example of serial I/O connection

DTMF FUNCTION

The M37415M4-XXXFP has the DTMF (Dual-Tone Multi-Frequency) output and control function. The value of bit 0, and bit 1 of DTMF register (address $00F4_{16}$) determines the low frequency band value. And the value of bit 2, and bit 3 of DTMF register determines the high frequency band value. The DTMF output can be controlled by the value of bit 4, and bit 5 of the DTMF register. When bit 4 is "1" the low frequency band is output to Tone, and when bit 4 is "0" the output of low frequency band is stopped. When bit 5 is "1" the high frequency band is output to Tone, and when bit 5 is "0" the output of high frequency band is stopped.

The value of bit 6, and 7 of DTMF register determines the basic frequency. The structure of the DTMF register is shown in Figure 11. The accuracy of DTMF output value is shown in Table 2 and 3.

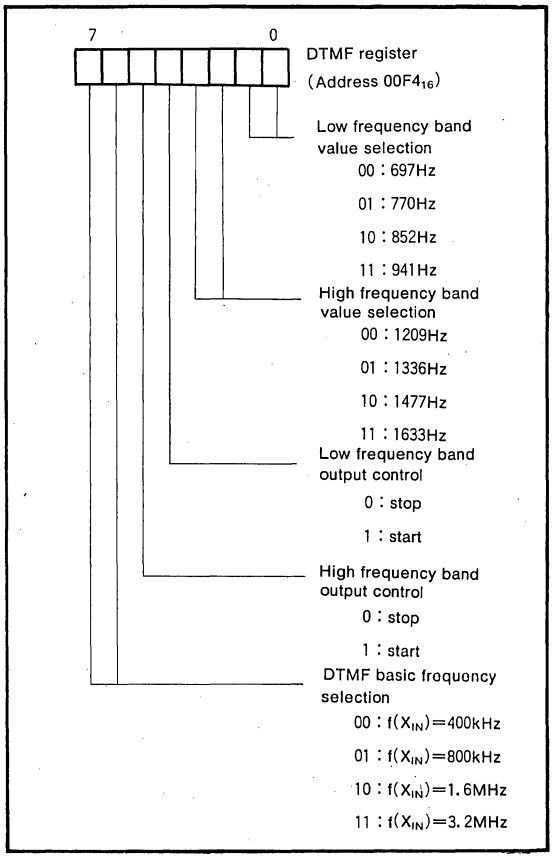


Fig.11 Structure of the DTMF register

Table 2 Accuracy of DTMF output (at low frequency band value)

Standard frequency value [Hz]	Output frequency value [Hz]	Deflection	Error [%]
697	694.44	−2.555	−0.367
770	769.23	−0.769	−0.1
852	854.7	2.7	0.317
941	938.97	−2.033	−0.216

Table 3 Accuracy of DTMF output (at high frequency band value)

Standard frequency value [Hz]	Output frequency value [Hz]	Deflection	Error [%]
1209	1204.8	−4.181	−0.346
1336	1333.3	−2.667	−0.2
1477	1470.6	6.412	0.434
1633	1639.3	6.344	−0.389

LCD CONTROLLER/DRIVER

The M37415M4-XXXFP has internal LCD controllers and drivers. A block diagram of LCD circuit is shown in Figure 15.

The terminals for LCD consist of 4 common-pin and 32 segments pin. SEG_{24}~SEG_{31} are in common with input P4. These pins are selected by bit 4 of the LCD mode register (LM_4, address $00F5_{16}$). Two biases (1/2 and 1/3) can also be selected. When bit 2 of the LCD mode register is "1", 1/2 bias is selected. When bit 2 is "0", 1/3 bias is selected. A 1/2, 1/3, or 1/4 duty cycle can also be selected. When bits 0 and 1 of the LCD mode register (LM_0, LM_1) is n, the duty ratio is 1/(n+1).

Address $00D0_{16}$ ~ $00DF_{16}$ is the designated RAM for the LCD display. When 1s' are written to these addresses, the corresponding segments of the LCD display panel are turned on. A map of the LCD display RAM is shown in Figure 13. The ON/OFF function for the LCD controller is controlled by bit 3 of the LCD mode register (LM_3). When this bit is "1" all the segments of the LCD are turned on. When this bit is "0" all the segments are turned off. An example circuit for each bias is shown in Figure 14 Figure 16 and Figure 17 describes the LCD driver waveforms for each bias and duty cycle.

The LCDCK timing frequency (LCD driver timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(\text{LCDCK}) = \frac{\text{(frequency of timer 1 count source)}}{\text{((timer 1 setting+1)}\times 4)}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{n} \quad ; \text{at } 1/n \text{ duty}$$

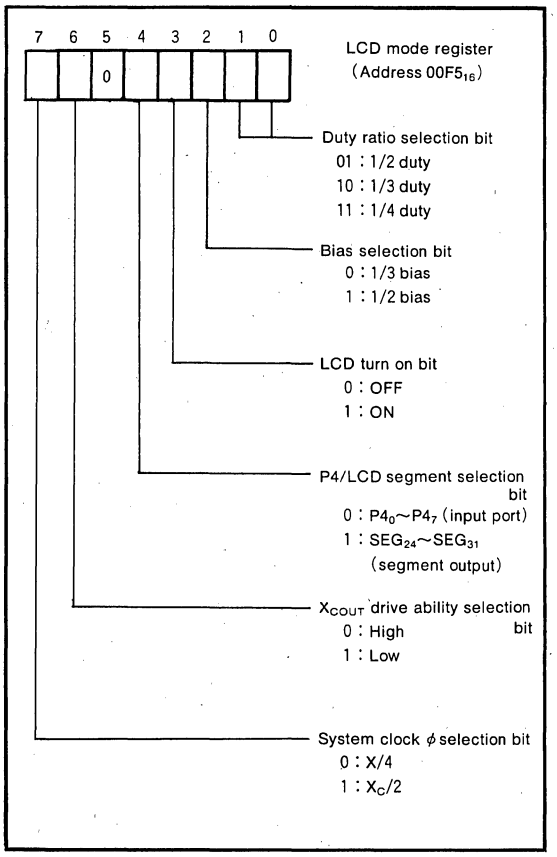
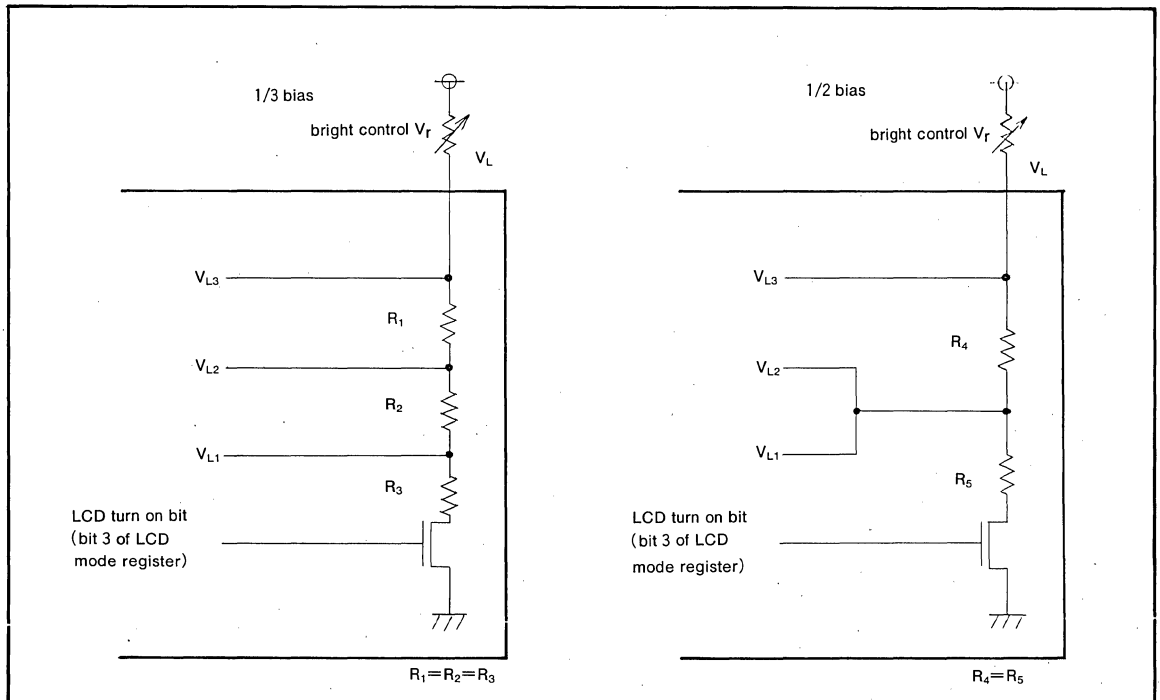


Fig.12 Structure of the LCD mode register

Bit / Address	7	6	5	4	3	2	1	0
D0	1	1	1	1	0	0	0	0
D1	3	3	3	3	2	2	2	2
D2	5	5	5	5	4	4	4	4
D3	7	7	7	7	6	6	6	6
D4	9	9	9	9	8	8	8	8
D5	11	11	11	11	10	10	10	10
D6	13	13	13	13	12	12	12	12
D7	15	15	15	15	14	14	14	14
D8	17	17	17	17	16	16	16	16
D9	19	19	19	19	18	18	18	18
DA	21	21	21	21	20	20	20	20
DB	23	23	23	23	22	22	22	22
DC	25	25	25	25	24	24	24	24
DD	27	27	27	27	26	26	26	26
DE	29	29	29	29	28	28	28	28
DF	31	31	31	31	30	30	30	30
	COM_3	COM_2	COM_1	COM_0	COM_3	COM_2	COM_1	COM_0

*Number in data memory area indicates corresponding segment.

Fig. 13 Map of RAM for LCD segment



Note 1 : The voltage for LCD bias (V_{L1}, V_{L2}, V_{L3}) are determined by internal voltage divided resistors.

2 : The voltage of V_{L1}, and V_{L2} are switched as following Fig. 16 automatically by bit 2 of LCD mode register.

3 : The current of the internal voltage divided resistors that are through by bit 3 of LCD mode register are controlled by internal transistor. When the LCD are turned on, the internal transistor is turened on, and the transistor is turned off auto-matically, if the LCD are turned off.

Fig.14 Example of circuit at 1/3 bias, 1/2 bias

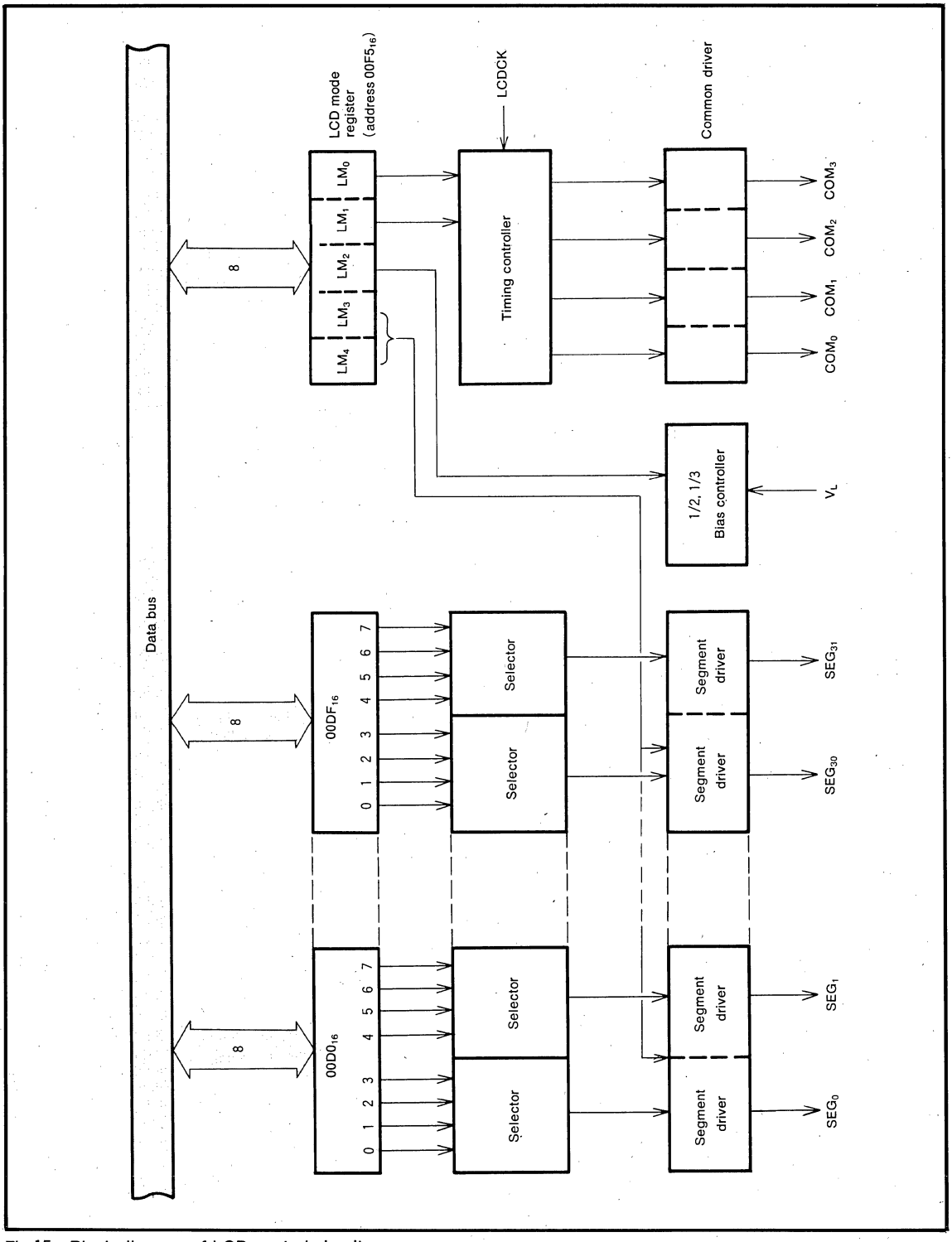


Fig.15 Block diagram of LCD control circuit

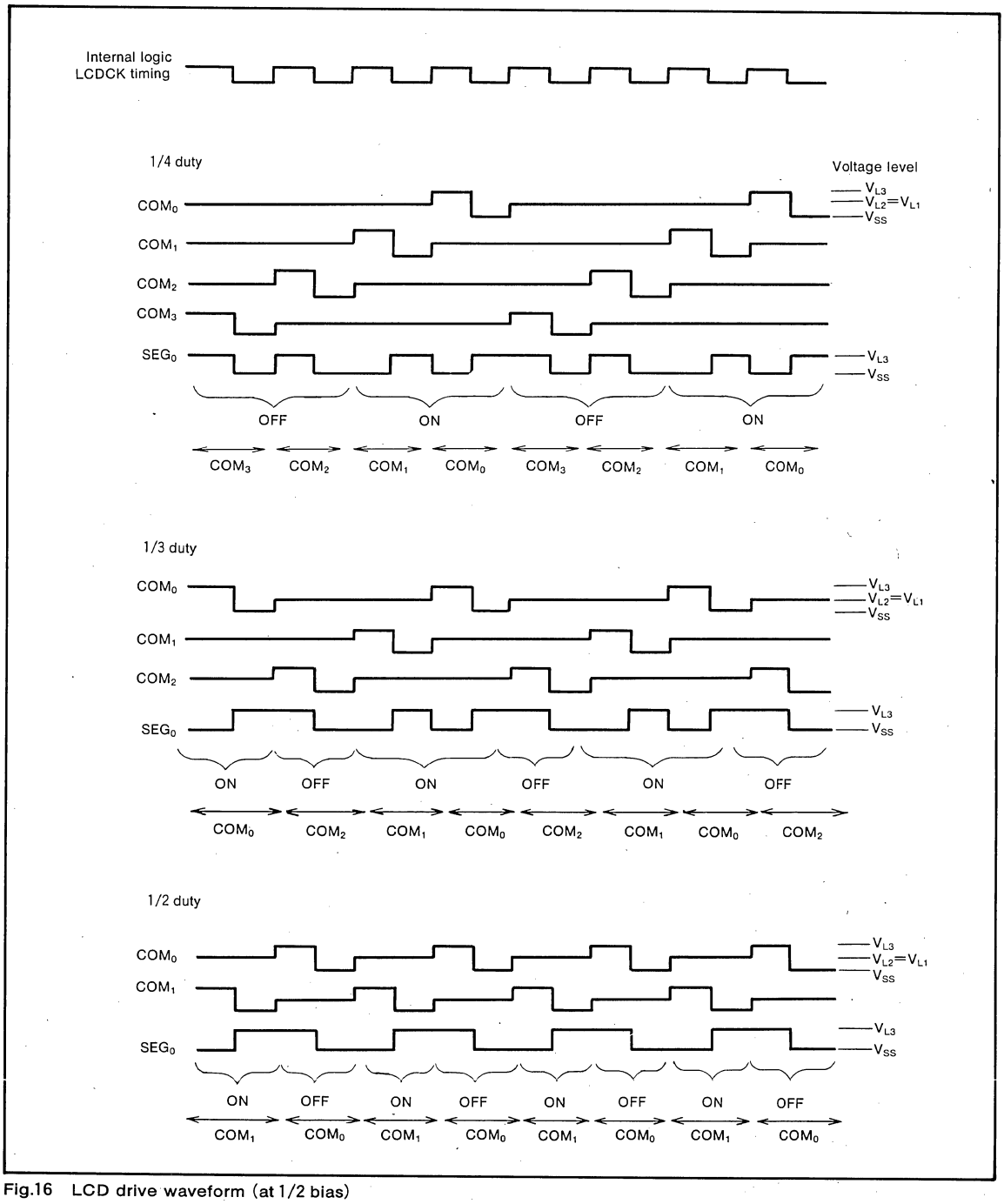


Fig.16 LCD drive waveform (at 1/2 bias)

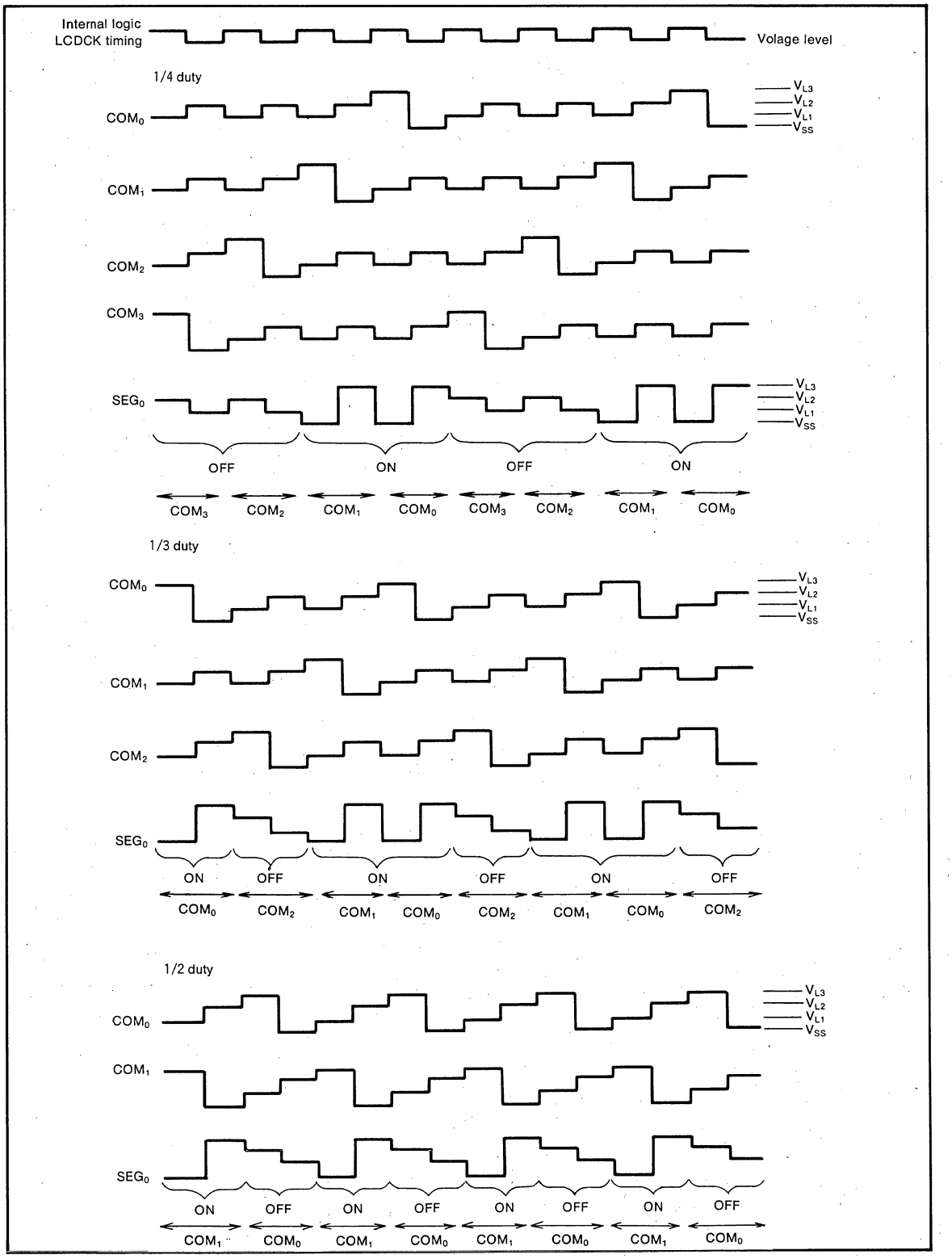


Fig.17 LCD drive waveform (at 1/3 bias)

KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P2 has a "L" level applied, after bit 7 of the serial I/O mode register (SM_7) is set to "1", an interrupt is generated and the microcomputer is returned to the normal operating state. As shown in Figure 18, a key matrix can be connected to port P2 and the microcomputer can be retuned to a normal state by pushing any key.

The key on wake up interrupt is common with the $\overline{INT_2}$ interrupt. When SM_7 is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and $\overline{INT_2}$ are invalid.

In order to enter the power down state generated by the STP or WIT instruction at the interrupt disable flag (I) is "0" and SM_7 is "1", all of port P2 must be input "H"

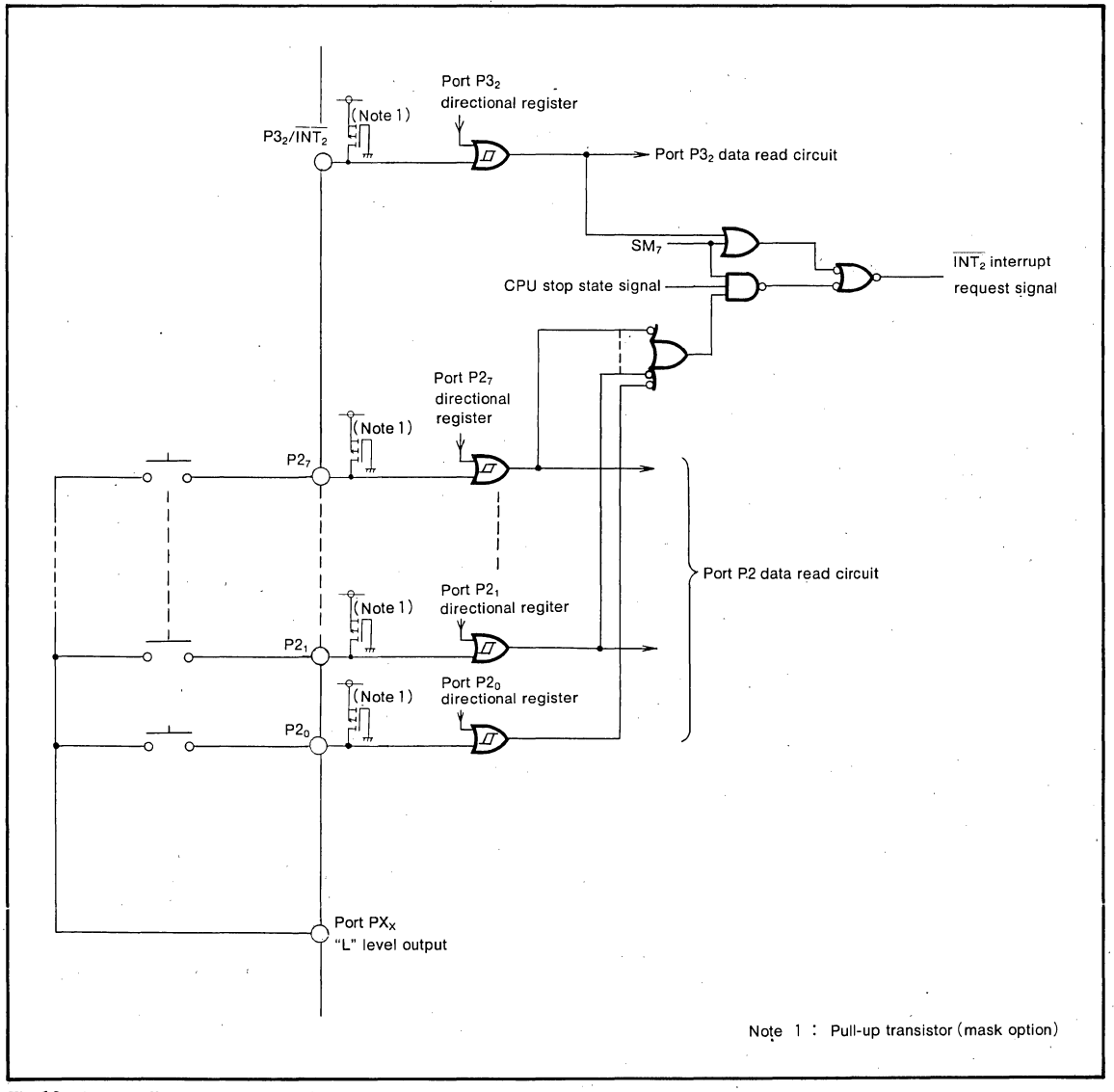


Fig.18 Block diagram of port P2 and $P3_2$, and example of wired at used key on wake up

RESET CIRCUIT

The M37415M4-XXXFP is reset according to the sequence shown in Figure 21. It starts the program from the address formed by using the content of address $3FFF_{16}$ as the high order address and the content of the address $3FFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for at least 8 rising edges of X_{IN} while the power voltage is in the recommended oprating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 19.

An example of the reset circuit is shown in Figure 20.

When the power on reset is used, the $\overline{RESET}$ pic must be held "L" unitil the oscillation of X_{IN}-X_{OUT} becomes stable.

		Address	
(1)	Port P0 directional register	($00E1_{16}$)	00_{16}
(2)	Port P1 directional register	($00E3_{16}$)	00_{16}
(3)	Port P2 directional register	($00E5_{16}$)	00_{16}
(4)	Port P3 directional register	($00E9_{16}$)	00_{16}
(5)	DTMF register	($00F4_{16}$)	0 0 0 0
(6)	LCD mode register	($00F5_{16}$)	00_{16}
(7)	Serial I/O mode register	($00F6_{16}$)	00_{16}
(8)	Timer 4, 5 mode register	($00F8_{16}$)	0 0 0 0
(9)	Interrupt control register	($00FE_{16}$)	00_{16}
(10)	Timer control register	($00FF_{16}$)	00_{16}
(11)	Interrupt disable flag for processor status register	(PS)	1
(12)	Program counter	(PC_H)	Contents of address $3FFF_{16}$
		(PC_L)	Contents of address $3FFE_{16}$

Note : Since the contents of both registers other than those listed above (including timers and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values.

Fig.19 Internal state of microcomputer at reset

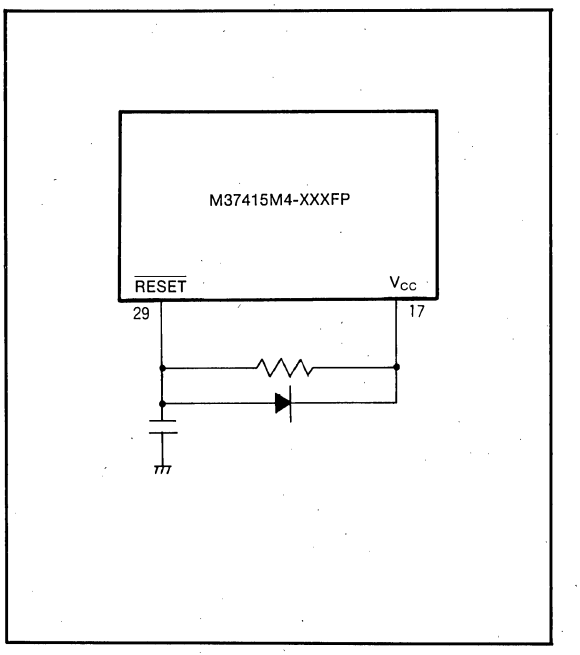
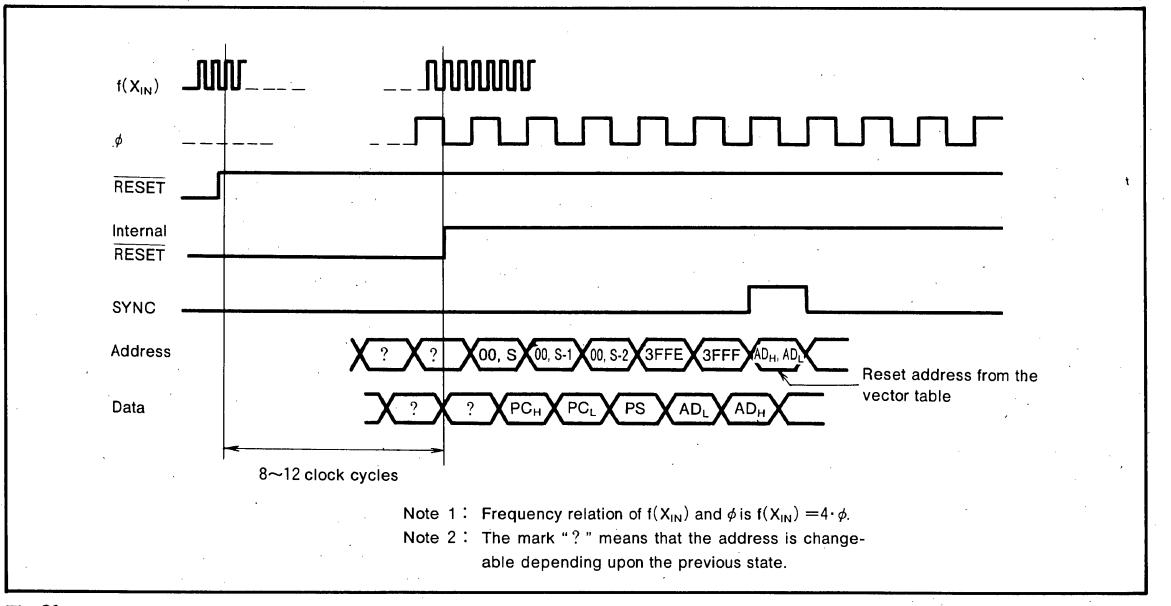


Fig.20 Example of reset circuit



Note 1 : Frequency relation of $f(X_{IN})$ and ϕ is $f(X_{IN}) = 4 \cdot \phi$.
Note 2 : The mark "?" means that the address is changeable depending upon the previous state.

Fig.21 Timing diagram at reset

MITSUBISHI ELECTRIC

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs and pull-up transistor options available. As shown in Figure 1, P0 can be accessed as memory through zero page address $00E0_{16}$. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address $00E1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port register and output. When data is read from the output port, the output pin level is not read, only the latched data of the port register is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

(2) Port P1

Port P1 has the same function as P0.

(3) Port P2

Port P2 has the same function as P0. Following the execution of STP or WIT instruction. P2 can be used to generate the "wake up mode". This mode is used to bring the microcomputer back in its normal oprating mode after being in the power-down mode.

(4) Port P3

Port P3 has the same function as P0 execept that part of P3 is common with the serial I/O lines (ie. output of timer 3, input/output of timer clock, and interrupt input).

(5) Segment output (SEG_0~SEG_{23})

These ports drive and control the LCD segments.

(6) Port P4

Port P4 is an 8-bit input port which can be used as a LCD segment output port.

(7) Common output (COM_0~COM_3)

These port provides output drive and control for the LCD common lines.

(8) Power supply for LCD (V_L)

Supplies power to the LCD terminals.

(9) $\overline{INT_1}$

The $\overline{INT_1}$ pin is an interrupt pin. The $\overline{INT_1}$ interrupt request bit (bit 7 of address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L". This input level is read into bit 1 of the timer 4 and 5 mode register (address $00F8_{16}$).

(10) $\overline{INT_2}$ ($\overline{INT_2}$/$P3_2$)

The $\overline{INT_2}$ pin is an interrupt input pin common with $P3_2$. When $P3_2$'s directional register is set for input ("0"), this pin can be used as an interrupt input. The $\overline{INT_2}$ interrupt request bit (bit 1 of address $00FE_{16}$) is automatically set to "1" when the input level of this pin changes from "H" to "L".

(11) CNTR

The CNTR pin is an I/O pin of timer 4 and 5. The input level is read into bit 0 of the timer 4 and 5's mode register (address $00F8_{16}$).

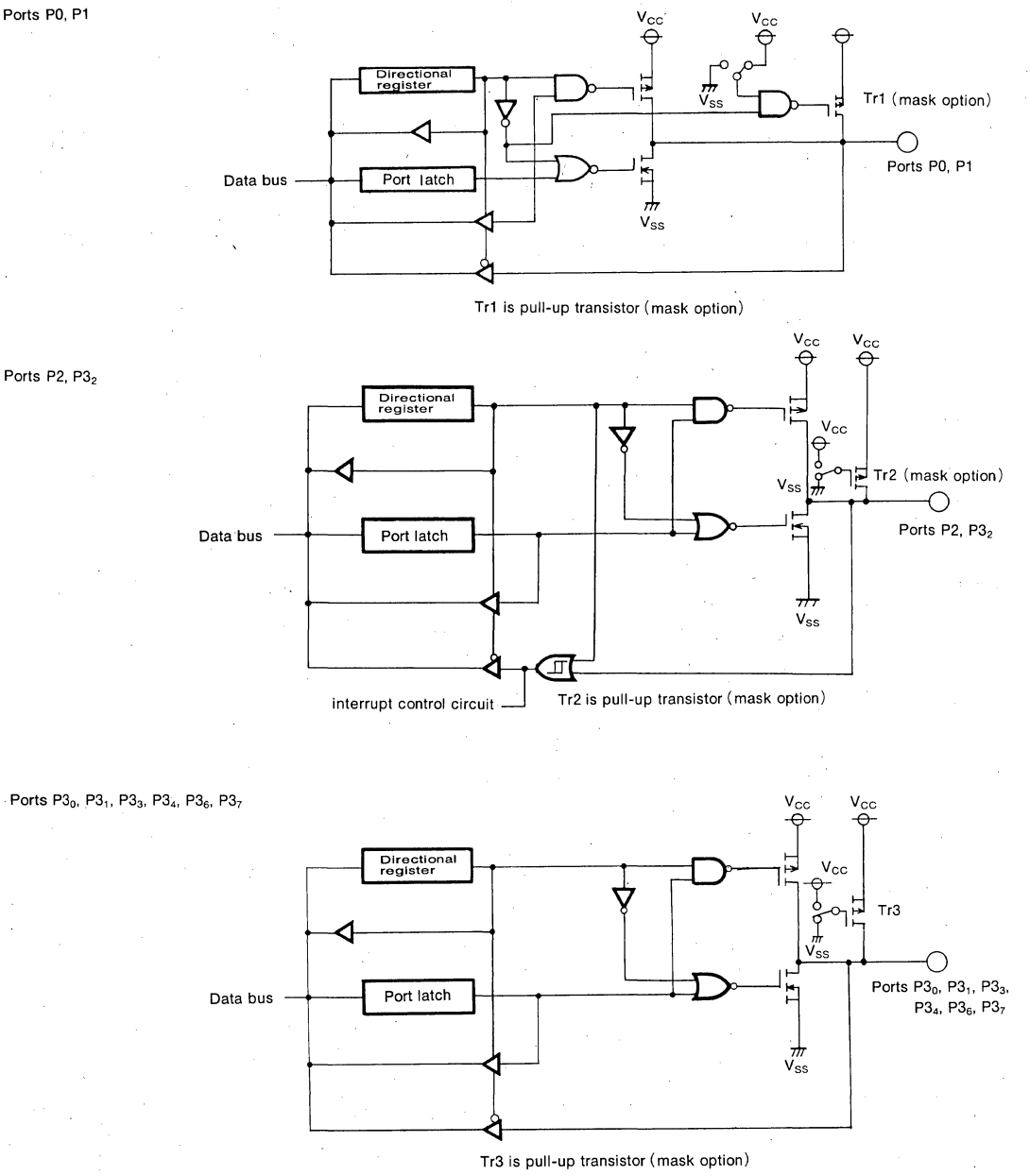
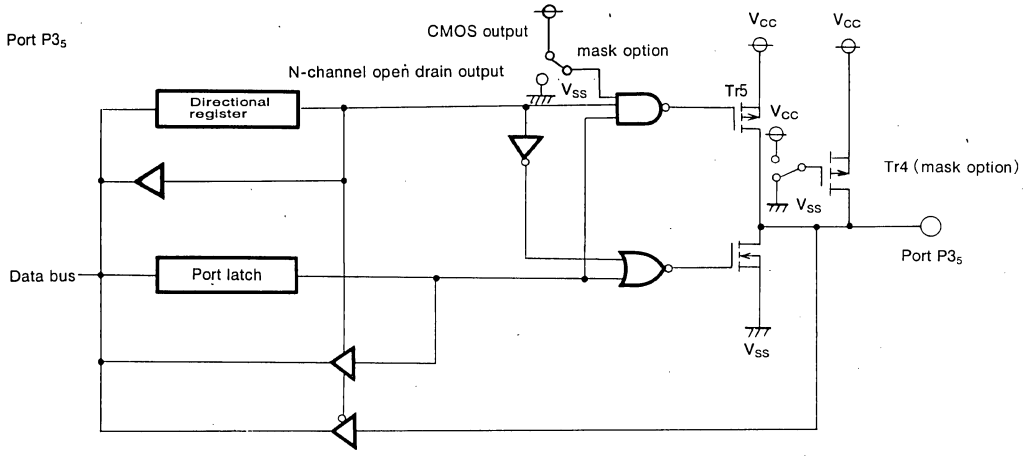
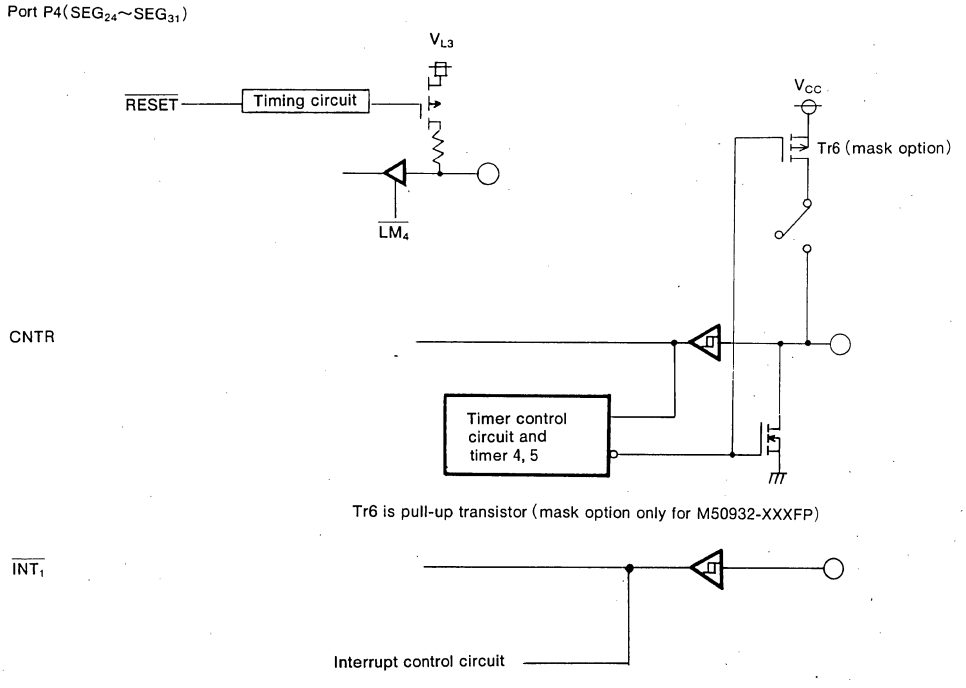


Fig.22 Block diagram of ports P0～P3



Tr4 is pull-up transistor (mask option)

Tr5 is P-channel output transistor (mask option)



Tr6 is pull-up transistor (mask option only for M50932-XXXFP)

Fig.23 Block diagram of ports P3, P4, CNTR, and $\overline{INT_1}$

CLOCK GENERATING CIRCUIT

The M37415M4-XXXFP has two internal clock generating circuit. Figure 26 shows a block diagram of the clock generating circuit. Normally, the frequency applied to the clock input pin X_{IN} divided by four is used as the internal clock (timing output)ϕ. Bit 7 of LCD mode register can be used to switch the internal clockϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 24 shows a circuit example using a ceramic (or cystal) oscillator. Use the manufacture's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input form the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 25.

The M37415M4-XXXFP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 1 and timer 2 are forcibly connected and $\phi/4$ is selected as timer 1 input. Before executing the STP instruction, appropriate values must be set in timer 1 and timer 2 to enable the oscillator to stabilize when restarting oscillation. Before executing the STP instruction, the timer 1 count stop bit must be set to supply ("0"), timer 1 interrupt enable bit and timer 2 interrupt enablb bit must be set to disable ("0"), and timer 2 interrupt request bit must be set to no request ("0").

Oscillation is resarted (release the stop mode) when INT_1 INT_2, key on wake up or serial I/O interrupt is received. The interrupt enaable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt, the internal clock ϕ is held "H" unitil timer 2 overflows and is not supplied to the CPU. When oscillation is restarted by reset, "L" level must be kept to the $\overline{\text{RESET}}$ pin unitil the oscillattion stabilizes because no wait timer is generated.

The microcomputer enters a wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power disspation operation is also achieved when the X_{IN} clock is stopped and tte internal clock ϕ is generated from the X_{CIN} clock. X_{IN} clock oscillation is stopped when the bit 6 of serial I/O mode register (address $00F6_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restaring. An "L" level must be kept to the $\overline{\text{RESET}}$ pin until the oscillation stabilizes when resetting while the X_{IN} clock is stopped. Figure 27 shows the transition states for the system clock.

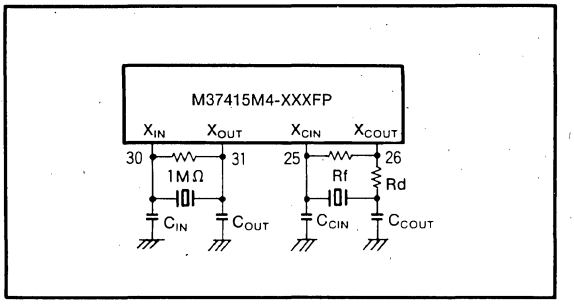


Fig.24 External ceramic resonator circuit

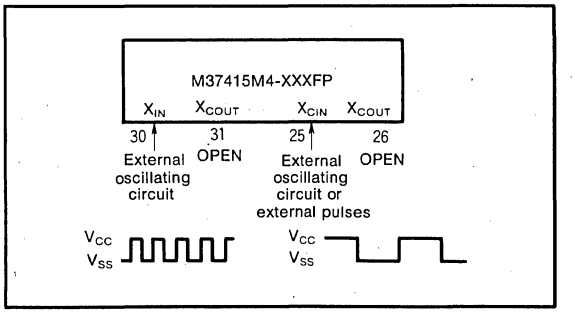


Fig.25 External clock input circuit

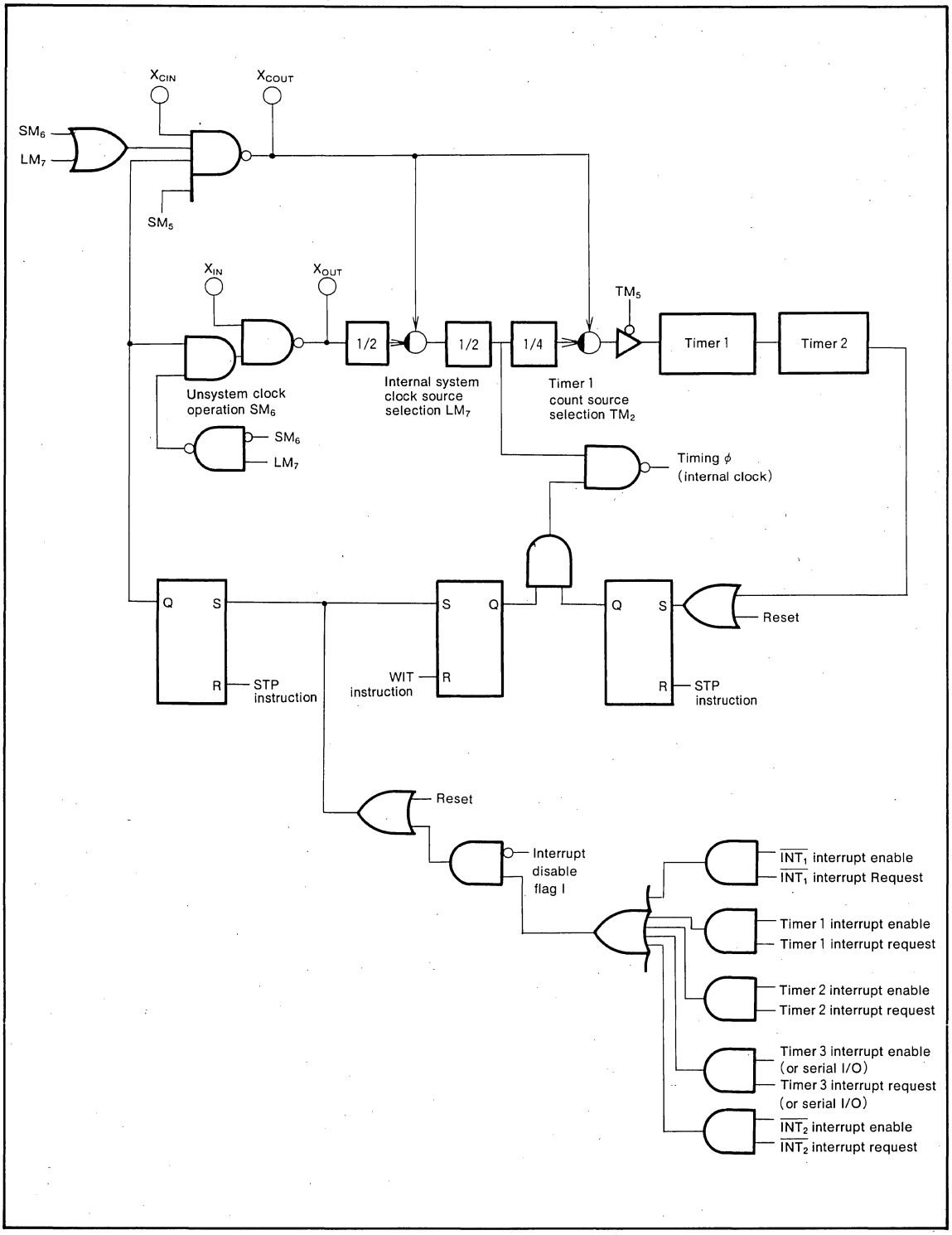
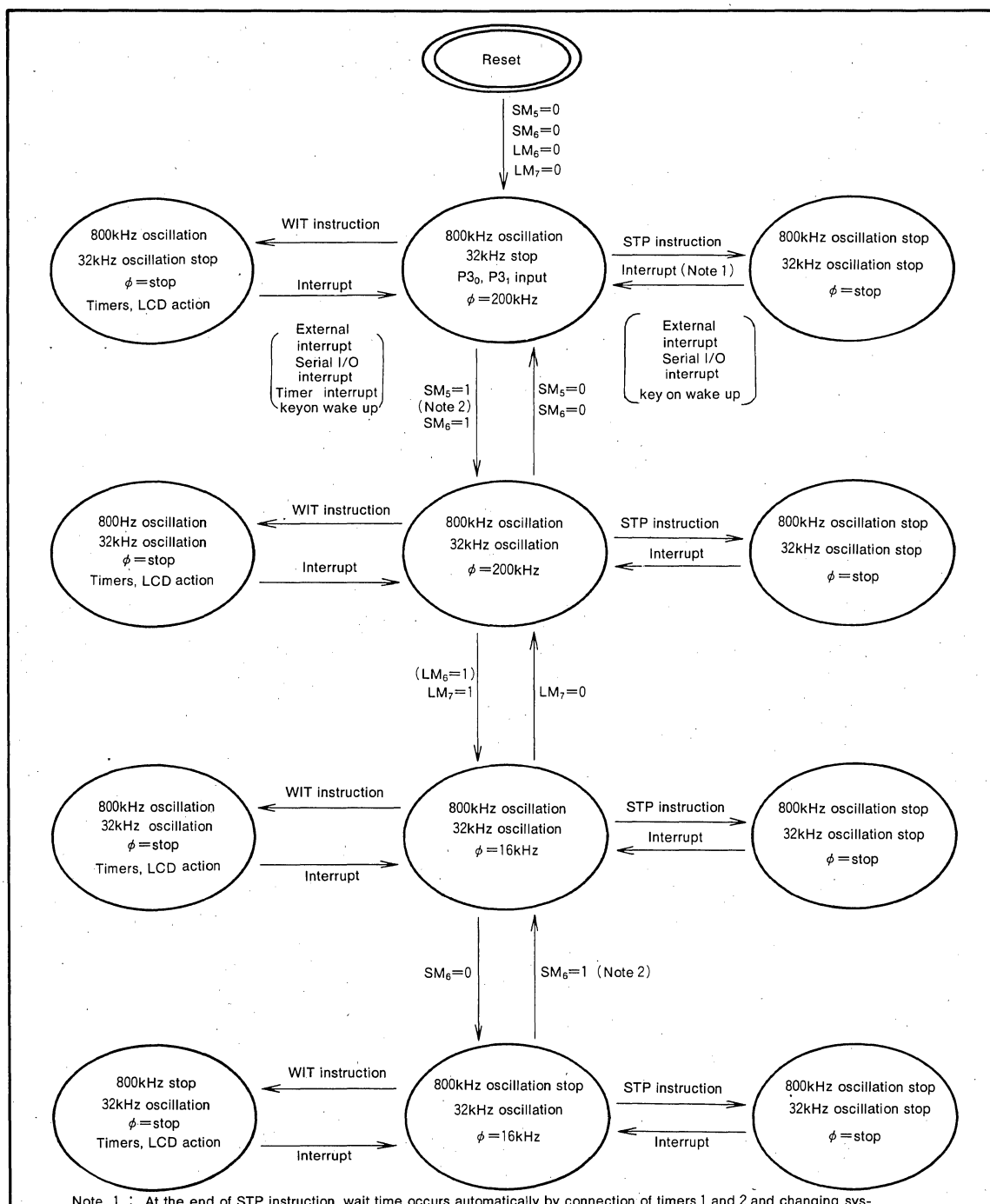


Fig.26 Block diagram of clock generating circuit



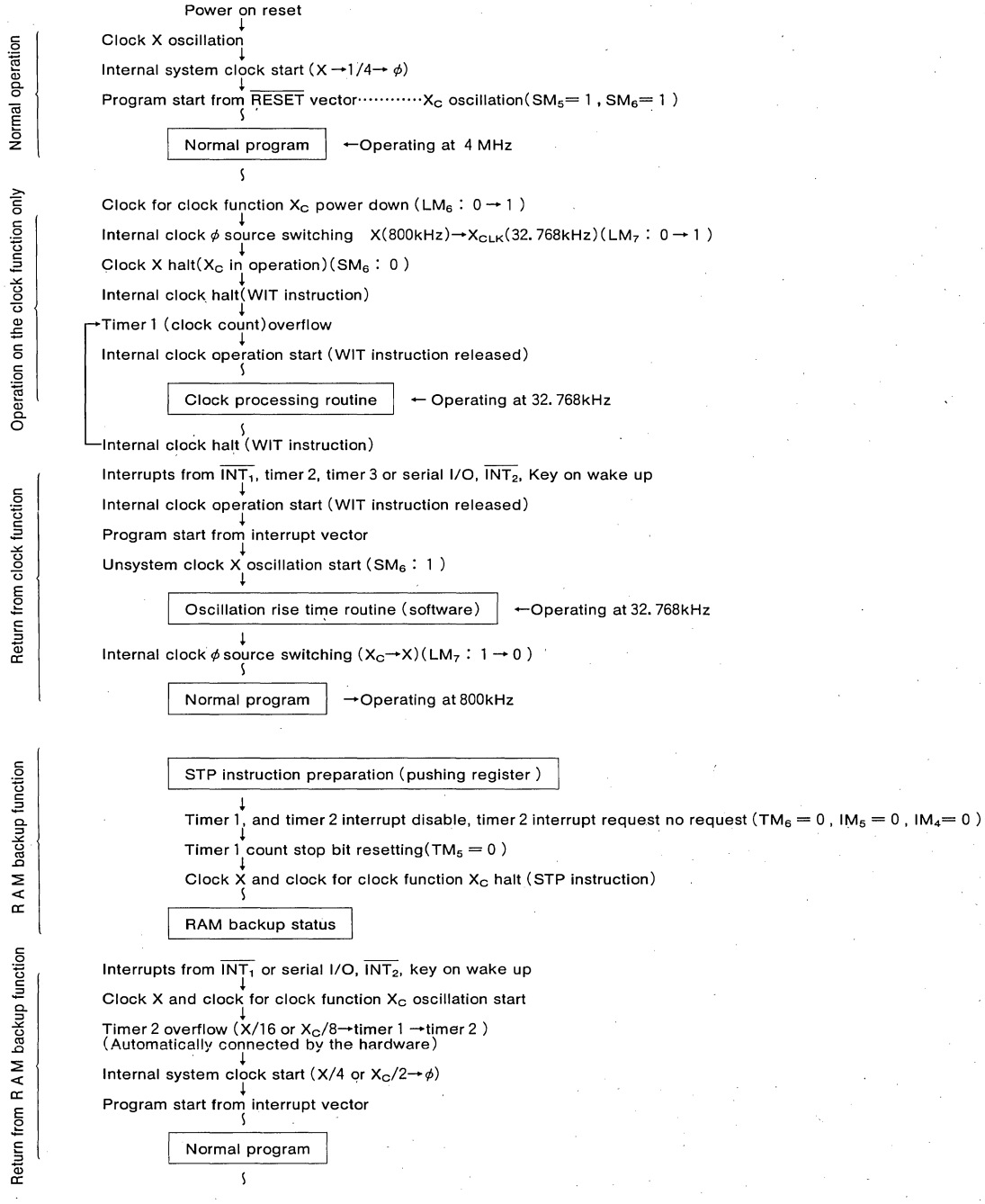
Note 1 : At the end of STP instruction, wait time occurs automatically by connection of timers 1 and 2 and changing system clock. This time is set by program.

2 : When $SM_6 = 1$ and unsystem clock is operated, wait time necessary by program until oscillation becomes stable.

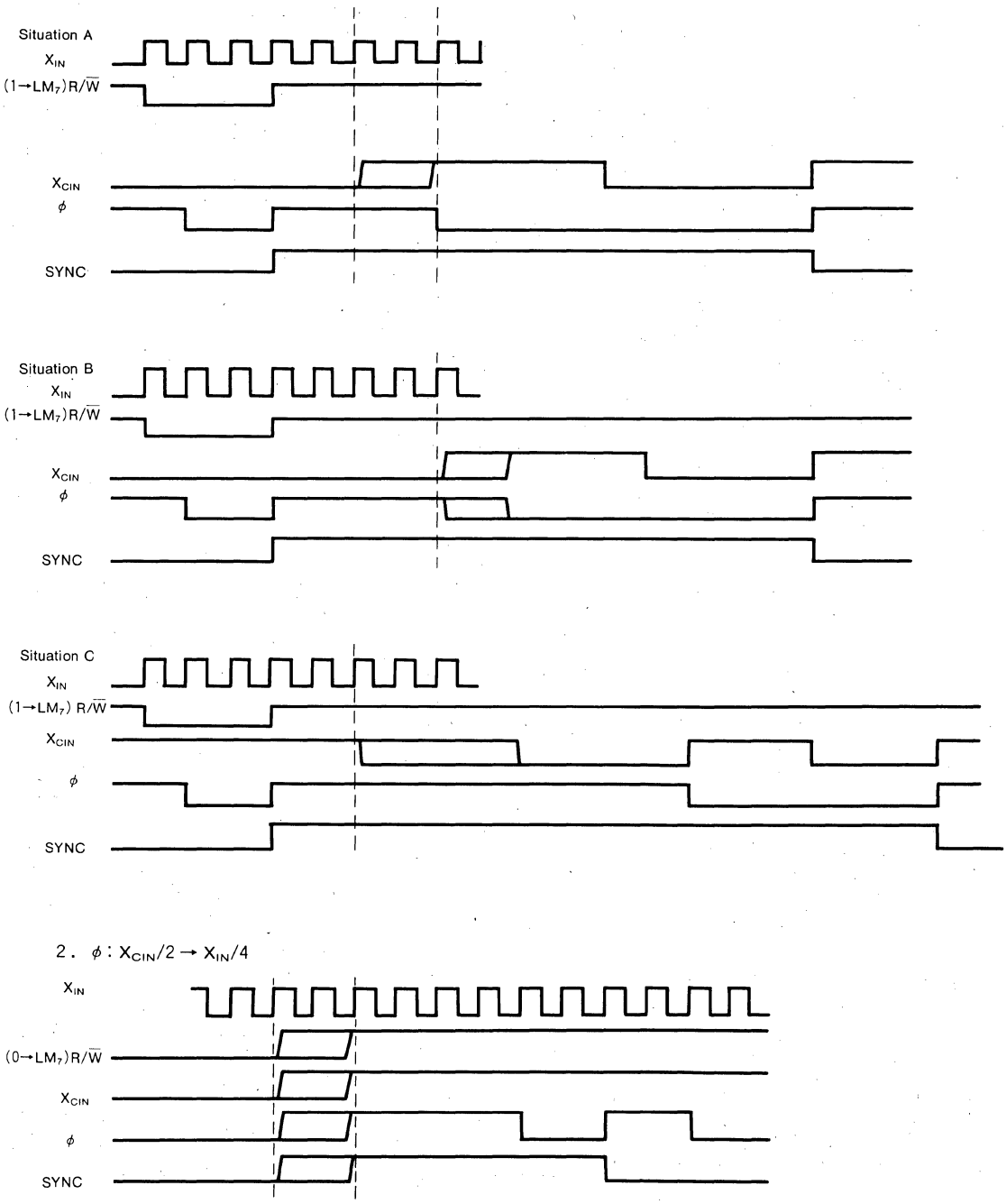
3 : The case of example clock X=800kHz, clock X_C=32kHz.

Fig.27 External clock input circuit

≪An example of flow for system≫



1. ϕ : $X_{IN}/4 \rightarrow X_{CIN}/2$ (timing diagrams are shown situation A~C, because there are three kinds of waveform by the timing)



2. ϕ : $X_{CIN}/2 \rightarrow X_{IN}/4$

Note 1 : The "L" period of the R/$\overline{W}$ signal is shown the writling timing of setting value to LM_7.
2 : The delay of timing is ignored.

Fig.28 Timing diagram of the changing system clock

PROGRAMMING NOTES

(1) The frequency ratio of the timer is $1/(n+1)$.

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instruction are only valid for the contents before the modifications are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When the timer 4 and the timer 5 are used at event counter mode, read the contents of these timers either while the input of the these timers are not changing or after timer 4, 5 count stop bit (bit 6 of address $00F8_{16}$) is set to "1".
Also, when the timer 1, timer 2, or timer 3 is input the clock except $\phi/4$ or it divided by timer, control the same as above.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) When LCD turn-on bit (bit 3 of address $00F5_{16}$) of the LCD mode register is "1", don't stop the timers or count source for timers.

(7) The timer 1 and timer 2 must be set the necessary value immediately before the execution of a STP instruction.

(8) Notes on controlling the clock generation circuit

① When system clock is changed $X_{IN}/4$ to $X_{CIN}/2$, set LM_7 to "1" after oscillation is stable by the software in side of clock X_C.

② When system clock is changed $X_{CIN}/2$ to $X_{IN}/4$, set LM_7 to "0" after oscillation is stable by the software in side of clock X.

③ When SM_5 is "0" or when LM_7 is "0" and SM_6 is "0", LM_6 is automatically set to "0" by the hardware.

④ When system clock selection bit (bit 7 of address $00F5_{16}$) of the LCD mode register is "1", don't set SM_5 to "0".

Just for reference, timing diagram of the changing system clock are shown in Figure 28.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation from

(2) mark specification from

(3) ROM data ..... EPROM 3 sets

Write the following option on the mask ROM confirmation from

- Port P0 pull-up transistor bit (see the confirmation form)
- Port P1 pull-up transistor bit (see the confirmation form)
- Port P2 pull-up transistor bit (see the confirmation form)
- Port P3 pull-up transistor bit (see the confirmation form)
- Port $P3_5/S_{OUT}$ output type (see the confirmation form)
- CNTR pin pull up transistor (see the confirmation form)

M37450M2-XXXSP/FP, M37450M4-XXXSP/FP M37450M8-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37450M2-XXXSP/FP is a single-chip microcomputer designed with CMOS sillicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 80-pin plastic molded QFP.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

It is suited for office automation equipment and control devices. The low power consumption made by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

The differences among M37450M2-XXXSP/FP, M37450M4-XXXSP/FP and M37450M8-XXXSP/FP are as shown below. The descriptions that follow describe the M37450M2-XXXSP/FP unless otherwise noted.

Type name	ROM size	RAM size
M37450M2-XXXSP/FP	4096 bytes	128 bytes
M37450M4-XXXSP/FP	8192 bytes	256 bytes
M37450M8-XXXSP/FP	16384 bytes	384 bytes

The number of analog input pins for the 80-pin model (FP version) is different from the 64-pin model (SP version). In addition, the 80-pin model has special pins for $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, DAV_{REF}, ADV_{REF}, AV_{CC} and the 64-pin model has a special V_{REF} pin.

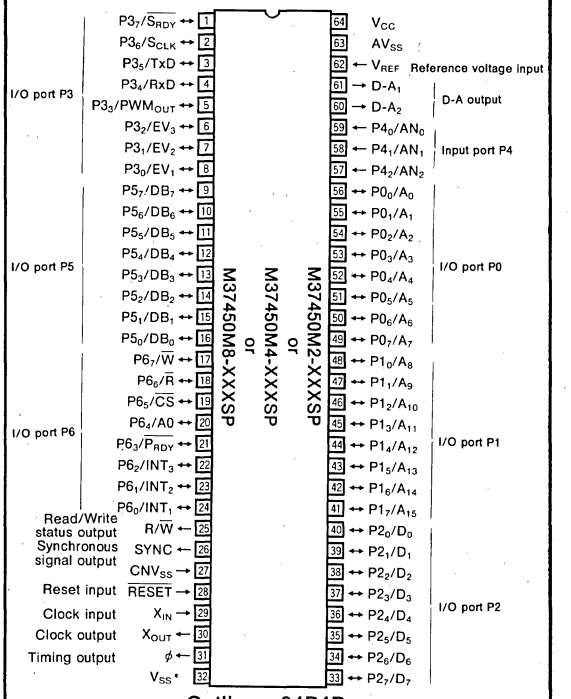
DISTINCTIVE FEATURES

- Number of basic instructions 71
  69 MELPS 740 basic instructions + 2 multiply/divide instructions
- Instruction execution time
  (Shortest instruction at 10MHz) ..... 0.8μs (min.)
- Single power supply ..... 5V$\pm$10%
- Power dissipation normal operation mode
  (at 10MHz frequency) 30mW
- Subroutine nesting ..... 64 levels max.(M37450M2)
- Interrupts ..... 15 events
- Master CPU bus interface ..... 1 byte
- 16-bit timer 3
- 8-bit timer (Serial I/O use) 1
- Serial I/O (UART or clock synchronous) 1
- A-D converter (8-bit resolution) ..... 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ..... 2 channels
- PWM output (8 bit or 16 bit) 1
- Programmable I/O
  (Ports P0, P1, P2, P3, P5, P6) 48
- Input (Port P4) ..... 3(DIP), 8(QFP)
- Output (Port D-A_1, D-A_2) 2

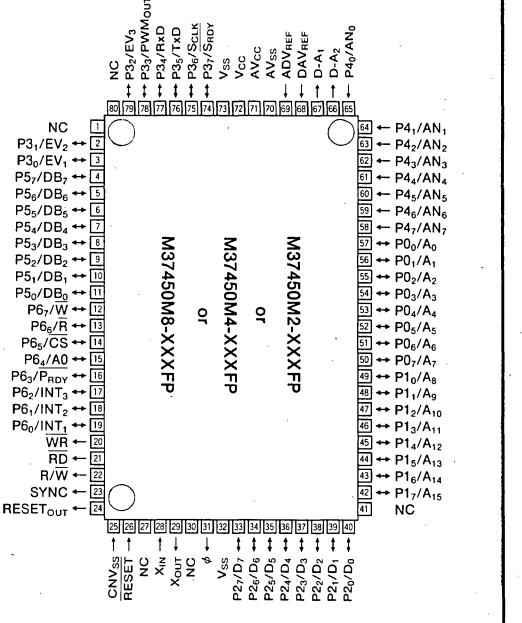
APPLICATION

Slave controller for PPCs, facsimiles, and page printers. HDD, optical disk, inverter, and industrial motor controllers. Industrial robots and machines.

PIN CONFIGURATION (TOP VIEW)



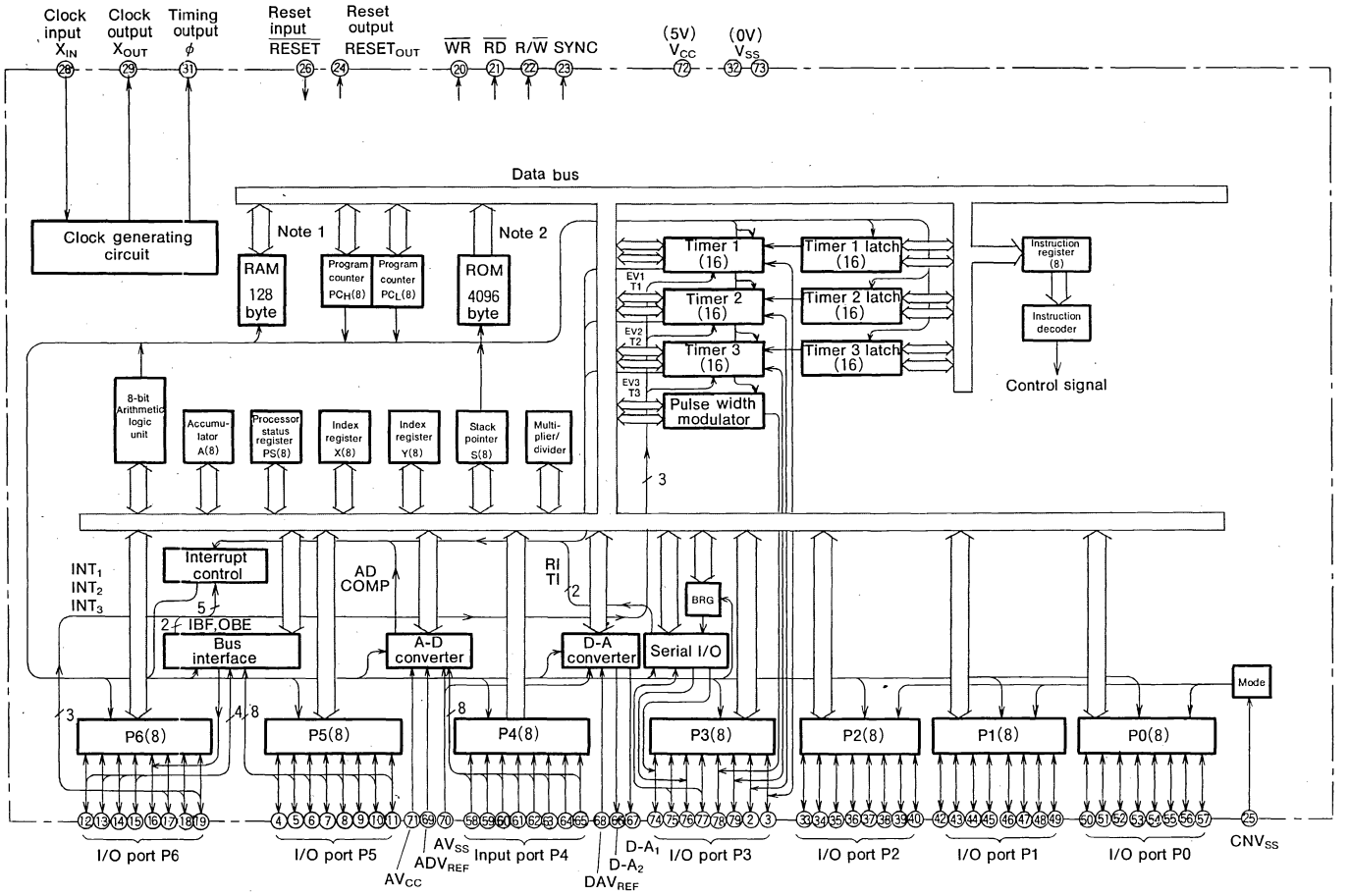
Outline 64P4B



Outline 80P6

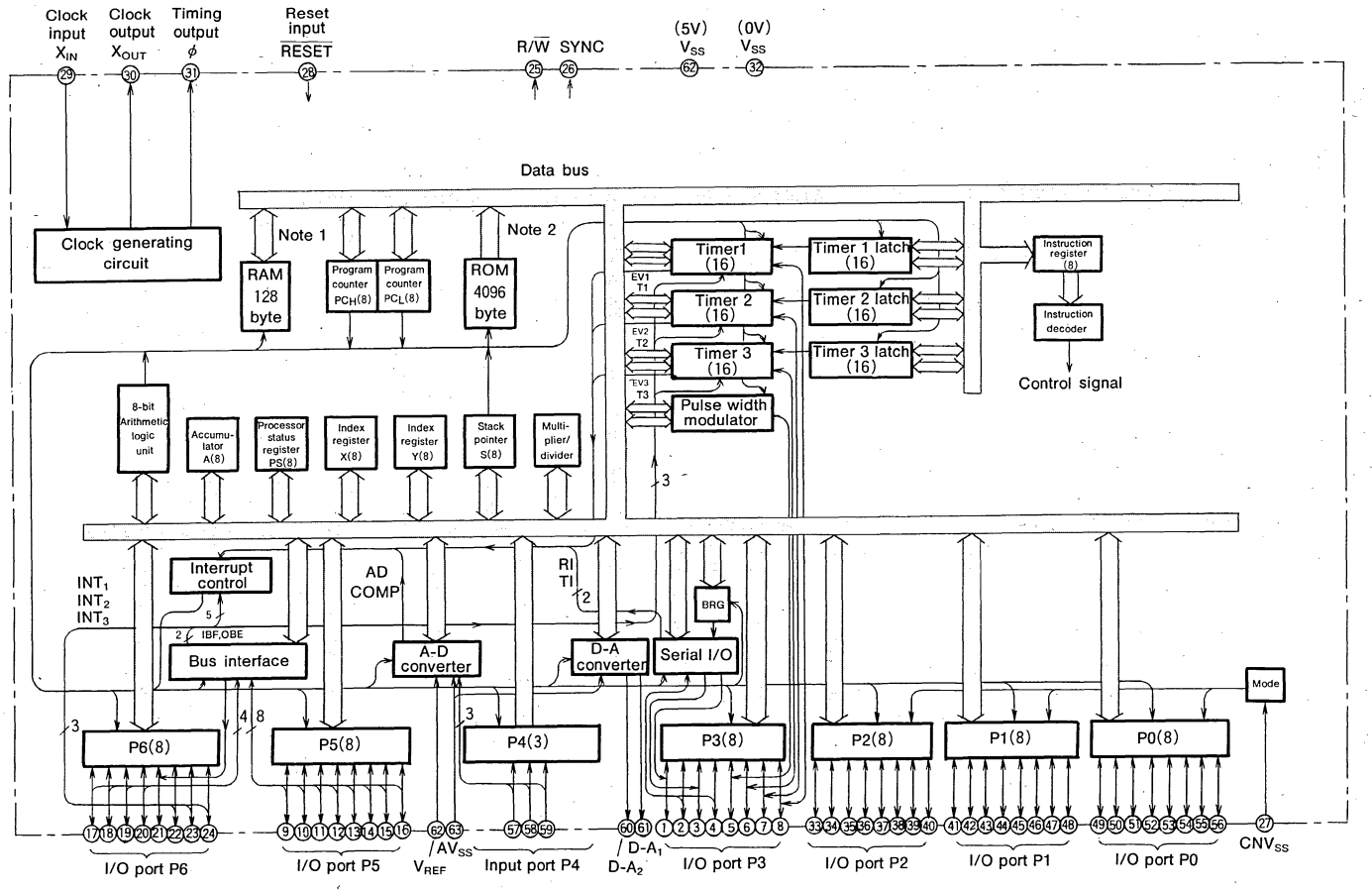
NC : No Connection

M37450M2-XXXFP BLOCK DIAGRAM



Note 1 : 256 bytes for M37450M4-XXXFP and 384 bytes for M37450M8-XXXFP.
2 : 8192 bytes for M37450M4-XXXFP and 16384 bytes for M37450M8-XXXFP.

M37450M2-XXXSP BLOCK DIAGRAM



Note 1 : 256 bytes for M37450M4-XXXSP and 384 bytes for M37450M8-XXXSP.
2 : 8192 bytes for M37450M4-XXXSP and 16384 bytes for M37450M8-XXXSP.

MITSUBISHI ELECTRIC

FUNCTIONS OF M37450M2-XXXSP/FP, M37450M4-XXXSP/FP, M37450M8-XXXSP/FP

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction excution time			0.8μs (minimum instructions, at 10MHz of frequency)
Clock frequency			10MHz (max.)
Memory size	M37450M2-XXXSP/FP	ROM	4096 bytes
		RAM	128 bytes
	M37450M4-XXXSP/FP	ROM	8192 bytes
		RAM	256 bytes
	M37450M8-XXXSP/FP	ROM	16384 bytes
		RAM	384 bytes
Input/Output port	P0~P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			64-levels (max. for M37450M2)
			96-levels (max. for M37450M4, M37450M8)
Interrupts			6 external interrupts, 8 internal interrupts 1 software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			30mW (at 10MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package	M37450M2-XXXSP		64-pin shrink plastic molded DIP
	M37450M4-XXXSP		
	M37450M8-XXXSP		
	M37450M2-XXXFP		80-pin plastic molded QFP
	M37450M4-XXXFP		
	M37450M8-XXXFP		

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		Controls the processor mode of the chip. Normally connected to V_{SS} or V_{CC}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four.
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs.
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus. It is "H" during read and "L" during write.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. The output structure is CMOS output. The low-order bits of the address are output except in single-chip mode.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The high-order bits of the address are output except in single-chip mode.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. Used as data bus except in single-chip mode.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. Serial I/O, PWM output, or event I/O function can be selected with a program.
$P4_0$~$P4_2$ ($P4_0$~$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter. The 64-pin model has three pins and the 80-pin model has eight pins. They may also be used as digital input pins.
$P5_0$~$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0. This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program.
$P6_0$~$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0. Pins $P6_3$~$P6_7$ change to a control bus for the master CPU when slave mode is selected with a program. Pins $P6_0$~$P6_2$ may be programmed as external interrupt input pins.
$D\text{-}A_1$, $D\text{-}A_2$	D-A output	Output	Analog signal from D-A converter is output.
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter. This pin is for 64-pin model only.
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter. This pin is for 80-pin model only.
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter. This pin is for 80-pin model only.
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter. Same voltage as V_{SS} is applied.
AV_{CC}	Analog power supply		Power supply input pin for A-D converter. This pin is for 80-pin model only. Same voltage as V_{CC} is applied. In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally.

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus. This pin is for 80-pin model only.
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component. This pin is for 80-pin model only.
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset. It is used as a reset output signal for peripheral components. This pin is for 80-pin model only.

BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M37450M2-XXXSP/FP is shown in Figure 1. Addresses $F000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 4096 bytes.

Address $E000_{16}$ to $FFFF_{16}$ are the ROM address area assigned to the M37450M4-XXXSP/FP. Addresses $C000_{16}$ to $FFFF_{16}$ are the ROM address area assigned to the M37450M8-XXXSP/FP.

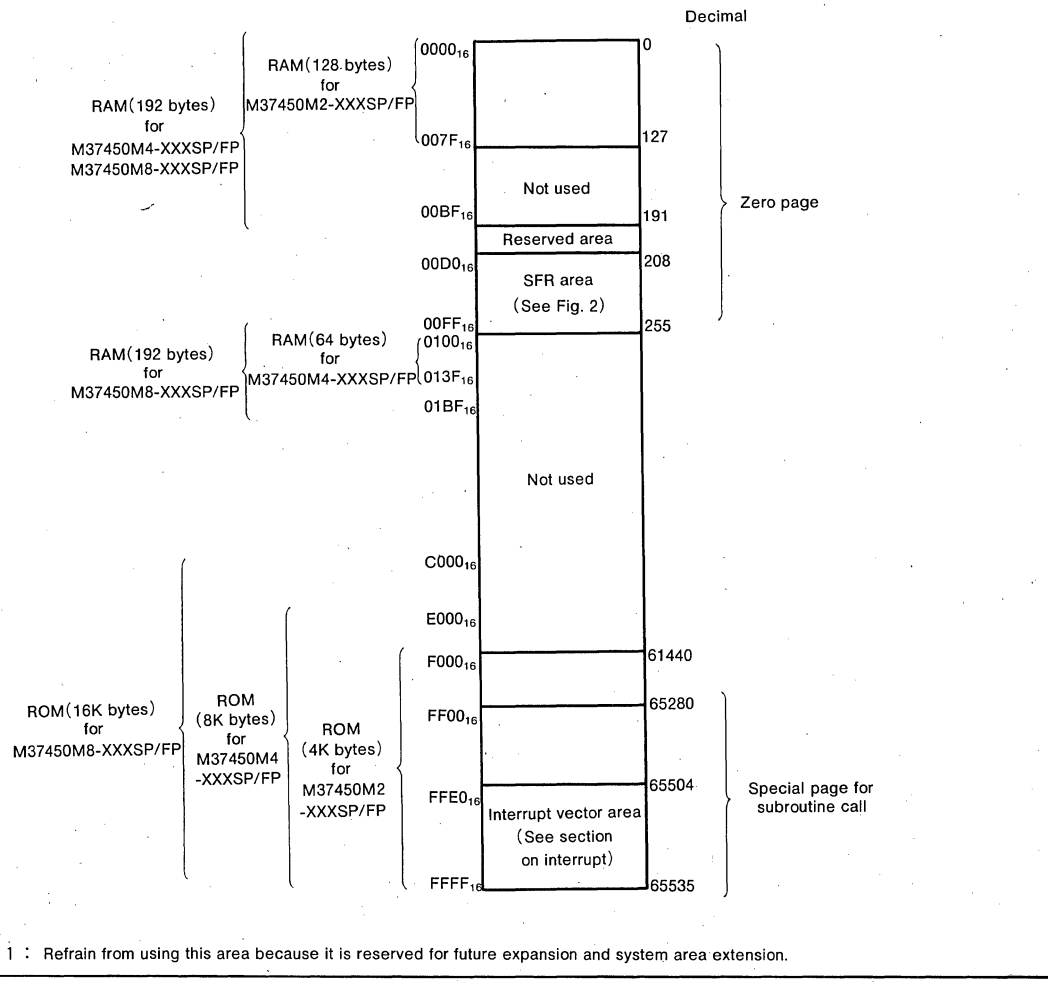
Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $FFE0_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (see interrupt section). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $007F_{16}$ are the RAM address area and consist of 128 bytes.

Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $013F_{16}$ are the RAM address area assigned to the M37450M4-XXXSP/FP and consist of 192 bytes and 64 bytes respectively.

Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $01BF_{16}$ are the RAM address area assigned to the M37450M8-XXXSP/FP and consist of 192 bytes and 192 bytes respectively.

In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.



Note 1 : Refrain from using this area because it is reserved for future expansion and system area extension.

Fig. 1 Memory map

$00D0_{16}$	P0 register
$00D1_{16}$	P0 directional register
$00D2_{16}$	P1 register
$00D3_{16}$	P1 directional register
$00D4_{16}$	P2 register
$00D5_{16}$	P2 directional register
$00D6_{16}$	P3 register
$00D7_{16}$	P3 directional register
$00D8_{16}$	P4 register
$00D9_{16}$	Reserved
$00DA_{16}$	P5 register
$00DB_{16}$	P5 directional register
$00DC_{16}$	P6 register
$00DD_{16}$	P6 directional register
$00DE_{16}$	MISRG1
$00DF_{16}$	MISRG2
$00E0_{16}$	D-A1 register
$00E1_{16}$	D-A2 register
$00E2_{16}$	A-D register
$00E3_{16}$	A-D control register
$00E4_{16}$	Data bus buffer register
$00E5_{16}$	Data bus buffer status register
$00E6_{16}$	Receive/Transmit buffer register
$00E7_{16}$	Serial I/O status register
$00E8_{16}$	Serial I/O control register
$00E9_{16}$	UART control register
$00EA_{16}$	Baud rate generator

$00EB_{16}$	PWM register (low-order)
$00EC_{16}$	PWM register (high-order)
$00ED_{16}$	Timer 1 control register
$00EE_{16}$	Timer 2 control register
$00EF_{16}$	Timer 3 control register
$00F0_{16}$	Timer 1 register (low-order)
$00F1_{16}$	Timer 1 register (high-order)
$00F2_{16}$	Timer 1 latch (low-order)
$00F3_{16}$	Timer 1 latch (high-order)
$00F4_{16}$	Timer 2 register (low-order)
$00F5_{16}$	Timer 2 register (high-order)
$00F6_{16}$	Timer 2 latch (low-order)
$00F7_{16}$	Timer 2 latch (high-order)
$00F8_{16}$	Timer 3 register (low-order)
$00F9_{16}$	Timer 3 register (high-order)
$00FA_{16}$	Timer 3 latch (low-order)
$00FB_{16}$	Timer 3 latch (high-order)
$00FC_{16}$	Interrupt request register 1
$00FD_{16}$	Interrupt request register 2
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Interrupt control register 2

Fig. 2 SFR (Special Function Register) memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 3.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.

In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the ingex register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.

In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

STACK POINTER (S)

The stack pointer (S) is an 8-bit register. It is used during subroutine calls and interrupts.

When there is an interrupts, the high-order contents of the program counter is pushed into the address formed by setting the high-order eight bits to 00_{16} or 01_{16} and the low-order eight bits to the content of the stack pointer. Next the stack pointer is decremented by one and the low-order content of the program counter is pushed into the address formed by setting the high-order eight bits to 00_{16} or 01_{16} and the low-order eight bits to the content of the stack pointer. Then the stack pointer is again decremented by one, the content of the processor status register is pushed into the address formed by setting the high-order eight bits to 00_{16} or 01_{16} and the low-order eight bits to the content of the stack pointer, and then the stack pointer is decremented by one once more. Whether to set 00_{16} or 01_{16} in the high-order eight bits is determined by bit 7 at address $00DF_{16}$. The high-order eight bits are set to 00_{16} if bit 7 at address $00DF_{16}$ is "0" and to 01_{16} if it is "1". At reset, it is set to "0", then can be changed by program. For M37450M2-XXXSP/FP, bit 7 at address $00DF_{16}$ must be "0" because there is no RAM within "01" page.

The push operation described above is performed automatically when an interrupt occurs. The RTI instruction is used to return from an interrupt routine.

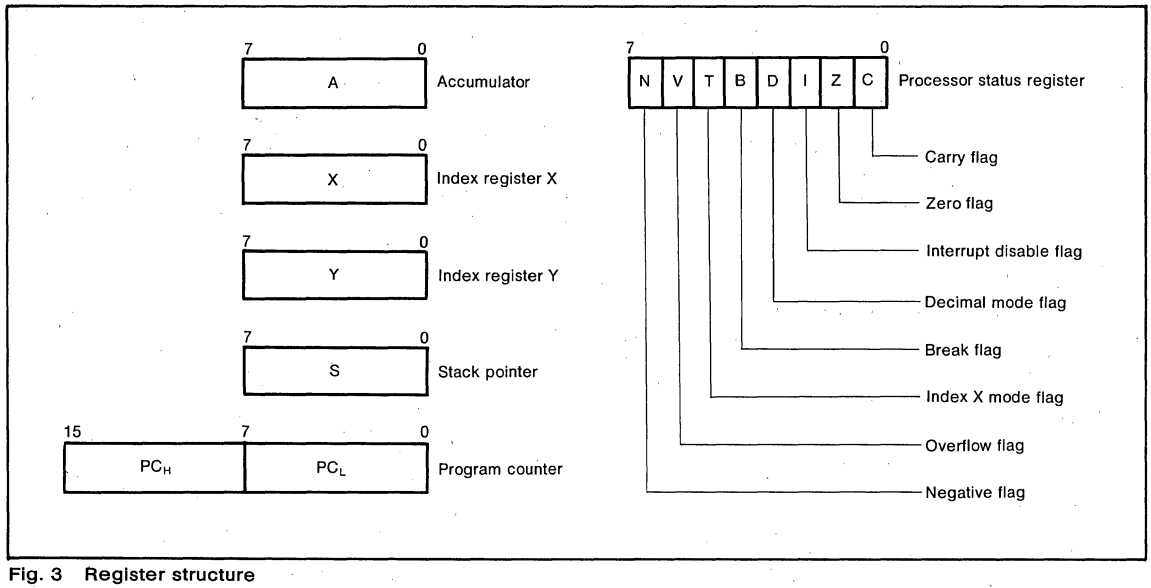


Fig. 3 Register structure

When an RTI instruction is executed, control is returned by reversing the above operation while incrementing the stack pointer by one. The PHA instruction is used to push the accumulator because it is not saved automatically. When the PHA instruction is executed, the content of the accumulator is pushed into the address formed by setting the high-order eight bits to 00_{16} or 01_{16} and the low-order eight bits to the content of the stack pointer. Then the content of the stack pointer is decremented by one. The PLA instruction is used to restore the accumulator. When the PLA instruction is executed, the stack pointer is incremented by one and the content of the address formed by setting the high-order eight bits to 00_{16} or 01_{16} and the low-order eight bits to the content of the stack pointer is stored in the accumulator. The processor status register is pushed and restored in the same manner with the PHP and PLP instructions. With subroutine calls, only the program counter is pushed. Therefore, registers that must be preserved must be pushed by the program. Use the RTS instruction to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is compleated. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break Flag B

The operation of a BRK instruction is similar to an interrupt. The BRK instruction is a non-maskable software interrupt that is used during program debugging. The break flag can be checked only by checking the content of the processor status register (PS) saved during an interrupt. The content of the processor status register (PS) is saved after setting flag B to "1" when the BRK instruction is used as an interrupt. It is cleared to "0" for other interrupts.

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a singed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

INTERRUPTS

Interrupts can be caused by 15 different events consisting of six external, eight internal, and one software event.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed as described in the stack pointer (S) section above, interrupt inhibit flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be inhibited. Other interrupts are disabled when the interrupt inhibit flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt inhibit bit is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
Input buffer full interrupt	2	$FFFD_{16}$, $FFFC_{16}$	Valid only in slave mode
Output buffer empty interrupt	3	$FFFB_{16}$, $FFFA_{16}$	Valid only in slave mode
INT_1 interrupt	4	$FFF9_{16}$, $FFF8_{16}$	External interrupt (phase programmable)
INT_2 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	External interrupt (phase programmable)
INT_3 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	External interrupt (phase programmable)
Timer 1 interrupt	7	$FFF3_{16}$, $FFF2_{16}$	
Timer 2 interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Timer 3 interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
EV_1 interrupt	10	$FFED_{16}$, $FFEC_{16}$	External event interrupt (phase programmable)
EV_2 interrupt	11	$FFEB_{16}$, $FFEA_{16}$	External event interrupt (phase programmable)
EV_3 interrupt	12	$FFE9_{16}$, $FFE8_{16}$	External event interrupt (phase programmable)
Serial I/O receive interrupt	13	$FFE7_{16}$, $FFE6_{16}$	Valid only when serial I/O is selected
Serial I/O transmit interrupt	14	$FFE5_{16}$, $FFE4_{16}$	Valid only when serial I/O is selected
A-D conversion completion flag	15	$FFE3_{16}$, $FFE2_{16}$	
BRK instruction interrupt	16	$FFE1_{16}$, $FFE0_{16}$	Non-maskable software interrupt

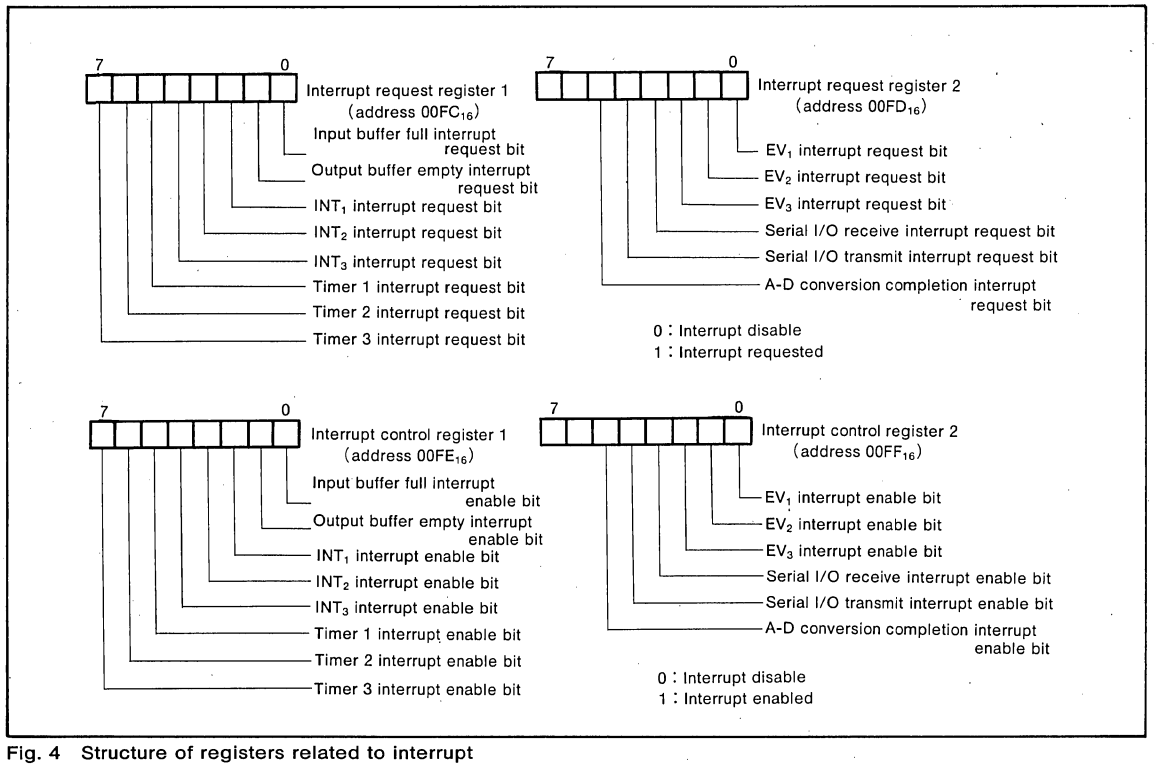


Fig. 4 Structure of registers related to interrupt

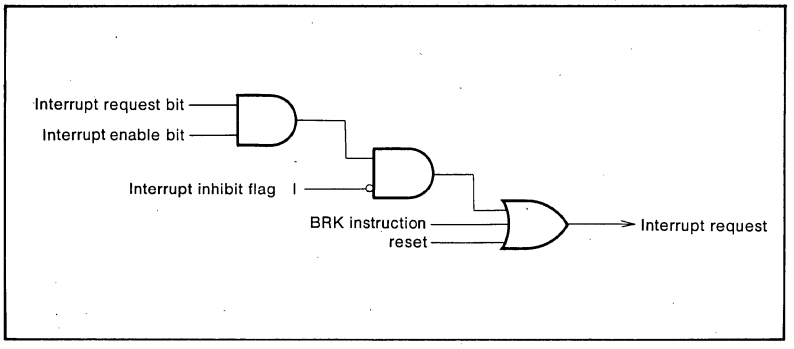


Fig. 5 Interrupt control

TIMER

The M37450 has three independent 16-bit internal timers as shown in Figure 6.

The timers are controlled by the timer i control register (i= 1, 2, 3) and MISRG1 shown in Figure 7 and 8.

The timer and the timer latch are independent of each other and a value must be written in both when setting a timer.

A write to a timer is performed in the order of T_L to T_H after setting the count enable bit to count inhibit "0".

A read from a timer is performed in the order of T_H to T_L. The value of T_L is latched in the read timer latch at the timing when T_H is read. All timers are decrement counters and are started by setting the timer i count enable bit to "1". When the value of the timer reaches 0000_{16}, and overflow occurs and the timer i interrupt request bit is set to "1" at the next count pulse.

During a reset or an STP instruction execution, the low-order byte of the timer 1 register is set to FF_{16} and the high-order byte is set to 03_{16}. Also, when an STP instruction is executed, a frequency obtained by dividing the oscillating frequency by four becomes the timer 1 input regardless of the timer 1 count source selection bit. This condition is canceled and the original count source is resumed when the timer i interrupt request bit is set to "1" or when a reset occurs. Refer to the section on the clock generator for details concerning the operation of the STP instruction.

The M37450 provides seven timer modes selectable with the timer mode selection bit in the timer i control register.

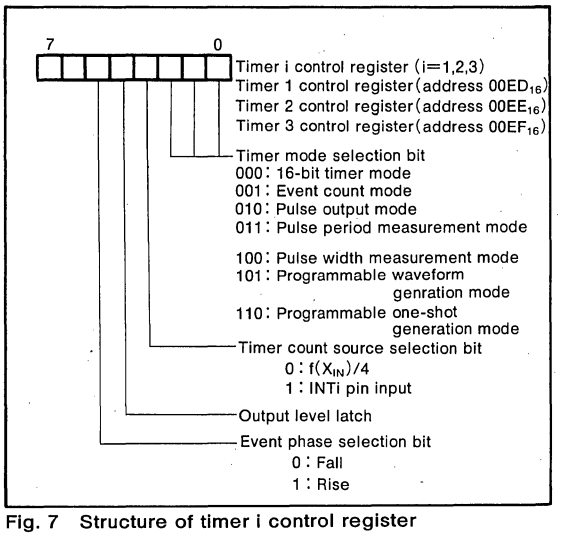


Fig. 7 Structure of timer i control register

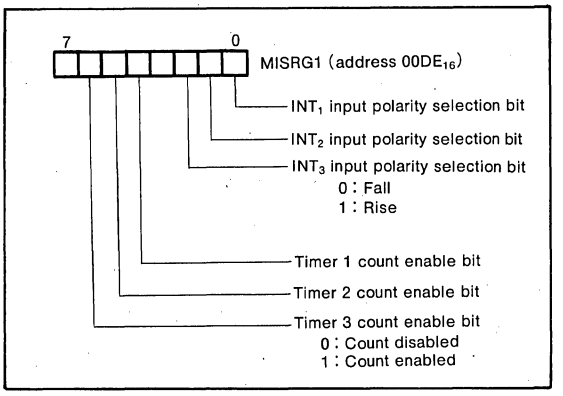


Fig. 8 Structure of MISRG1

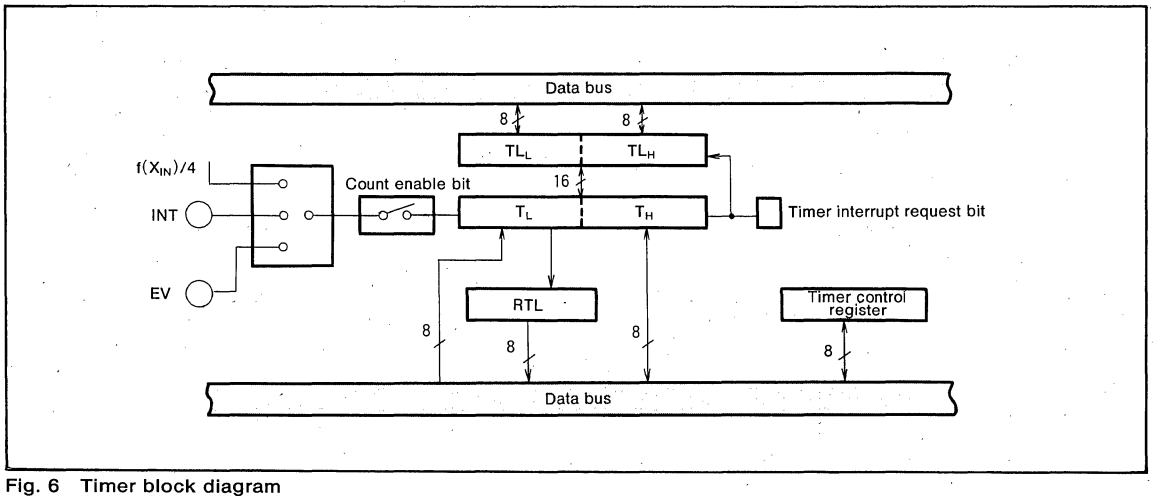


Fig. 6 Timer block diagram

(1) 16-bit Timer Mode [000]

In this mode, an interrupt request occurs and the value of the timer latch is loaded in the timer each time the timer overflows.

The timer count source is set to $f(X_{IN})$ divided by four regardless of the count sorce selection bit. Assuming that the timer latch is n, the frequency dividing ratio is $1/(n+1)$.

Figure 9 shows the timer operation duruing 16-bit timer mode.

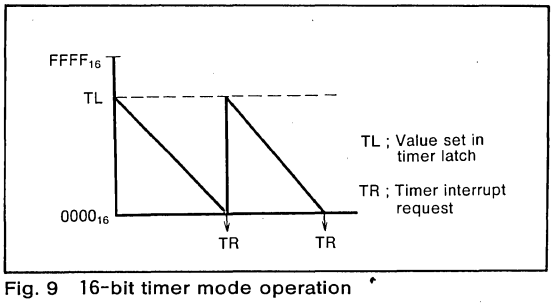


Fig. 9 16-bit timer mode operation

(2) Event Count Mode [001]

In this mode, the EVi pin input signal are counted in the direction selected by the event input polarity selection bit.

The input signal from the EVi pin is used as the count source regardless of the count source selection bit. The operation is the same as with the 16-bit timer mode except for the difference in the count source.

Both the "H" and "L" pulse width of the EVi pin input signal must be not less than $(4/f(X_{IN}))+100$ns.

Figure 10 shows the timer operation during event count mode.

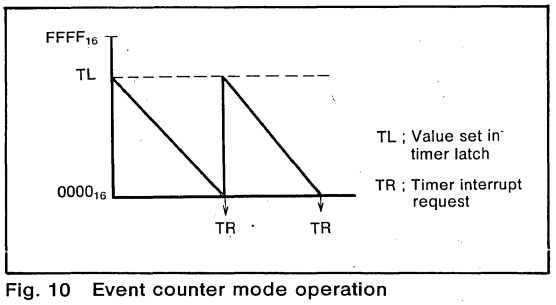


Fig. 10 Event counter mode operation

(3) Pulse Output Mode [010]

In this mode, a 50% duty pulse is output from the EVi pin.

The count source selected with the count source selection bit is counted. When it overflows, the phase of the EVi pin output level is reversed and the value of the timer latch is loaded in the timer.

When this mode is selected, the EVi pin output level is initialized to "L".

Figure 11 shows the timer operation during pulse output mode.

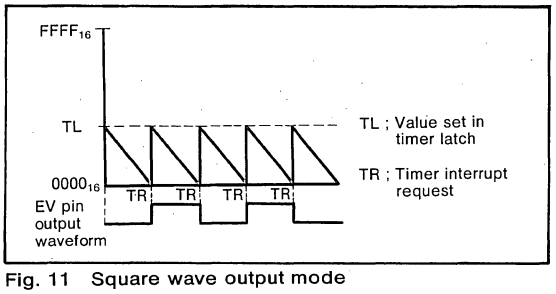


Fig. 11 Square wave output mode

(4) Pulse Period Measurement Mode [011]

This mode is used to measure the pulse period of the EVi pin input signal.

The timer counts the count source selected by the count source selection bit between the rise-to-rise or fall-to-fall interval (selected with the event input polarity selection bit in the timer i control register) of the EVi pin input signal.

At a valid edge on the EVi pin input, the 1's complement of the timer value is stored in the timer latch and the timer value is set to $FFFF_{16}$.

Figure 12 shows the timer operation during pulse frequency measurement mode.

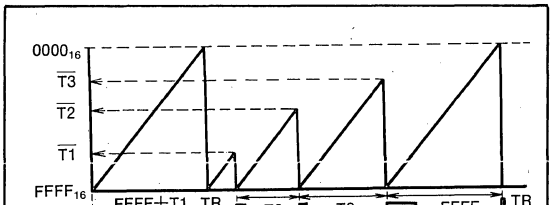


Fig. 12 Pulse period measurement mode

(5) Pulse Width Measurement Mode [100]

This mode measures the pulse width while the EVi pin input signal is "H" or "L".

Whether to measure the "H" or "L" interval is determined by the event input polarity selection bit. If this bit is "0", the count source selected with the count source selection bit is counted while the input pulse is "H". If it is "1", the count source is counted while the input pulse is "L". A 1's complement of the timer value is stored in the timer latch for a valid edge on the EVi pin input. In addition, the timer value is set to $FFFF_{16}$ for an edge (both rise and fall) on the EVi pin input. Figure 13 shows the timer operation during pulse width measurement mode.

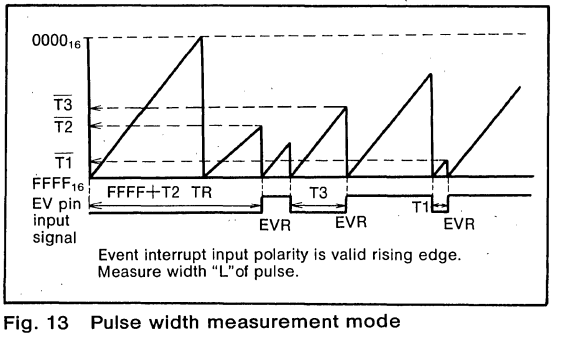


Fig. 13 Pulse width measurement mode

In pulse period measurement mode [011] and pulse width measurement mode [100], an EVi interrupt request is issued at the valid edge selected by the event phase selection bit. That is, an interrupt occurs at the end of the pulse period measurement or pulse width measurement. Also, when a timer overflow occurs, the count continues from $FFFF_{16}$ without the value of the timer latch being loaded in the timer.

Write to timer latch is inhibited in these modes. Furthermore, EVi interrupt is disabled during STP instruction execution.

(6) Programmable Waveform Generation Mode [101]

In this mode, the level set in the output level latch of the timer i control register is output to the EVi pin every time the timer overflows.

The timer counts the source selected by the count source selection bit and when it overflows, the value in the timer latch is loaded in the timer.

After it overflows, the value of the output level latch and the timer latch can be modified to generate any waveform from the EVi pin.

Figure 14 shows the timer operation during programmable waveform generation mode.

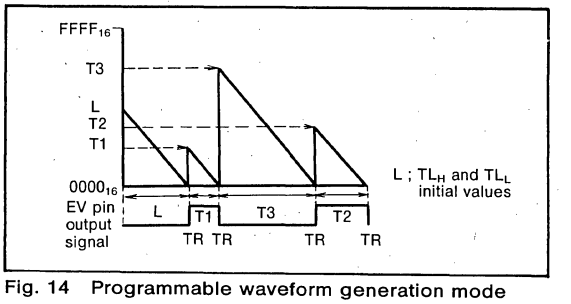


Fig. 14 Programmable waveform generation mode

(7) Programmable One-shot Generation Mode [110]

This mode uses the INTi pin input signal as a trigger and counts by writing the value of the timer latch in the timer.

The output level of the EVi pin goes "H" when the trigger is issued and goes "L" when the timer overflows.

The EVi pin level is initialized to "L" when this mode is selected.

The timer count souce is set to $f(X_{IN})$ divided by four regardless of the count source selection bit.

A valid edge of the INTi pin input trigger signal is determined by the INTi phase selection bit of MISRG1 ($00DE_{16}$).

Figure 15 shows the timer operation during programmable one-shot generation mode.

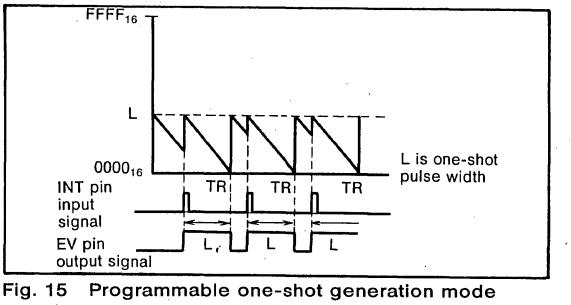


Fig. 15 Programmable one-shot generation mode

When the INTi pin input signal is selected as the count source for pulse output mode [010], pulse period measurement mode [011], pulse width measurement mode [100], and programmable waveform generation mode [101], the "H" and "L" pulse width of the input signal must not be less than $(6/f(X_{IN}))+100ns$.

SERIAL I/O

Serial I/O can operate in either clock synchronous or clock asynchronous (UART) mode. An exclusive baud rate generation timer (baud rate generator) is provided for serial I/O operation. Figure 16 shows the structure of the registers used for serial I/O.

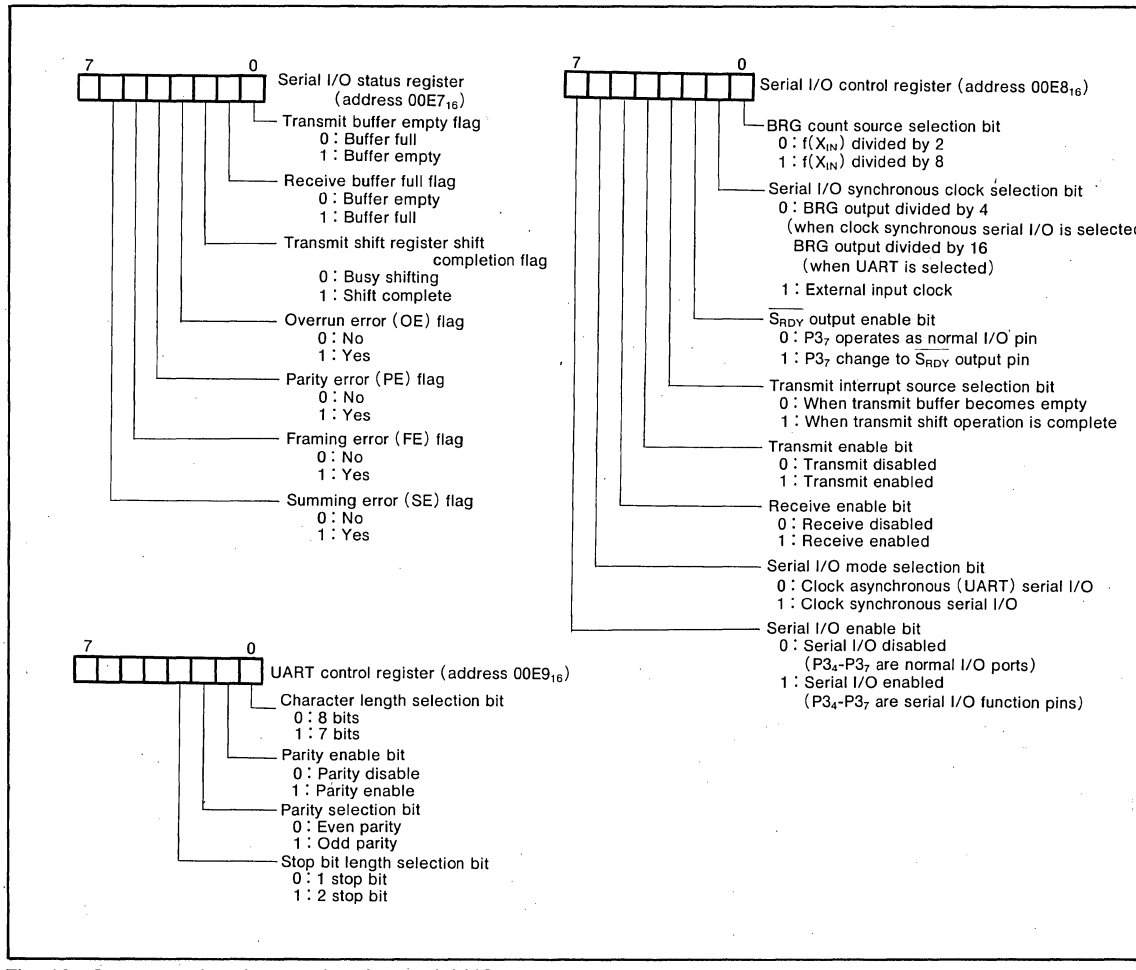


Fig. 16 Structure of registers related to serial I/O

(1) Clock Synchronous Serial I/O

Clock synchronous serial I/O is selected by setting the mode selection bit of the serial I/O control register to "1". Figure 17 shows a block diagram of clock synchronous serial I/O and Figure 18 shows its operation.

With clock synchronous serial I/O, the same clock is used as the operating clock between the transmitting and receiving microcomputers. If an internal clock is used for operating clock, transmit/receive is started by writing a signal in the transmit/receive buffer register.

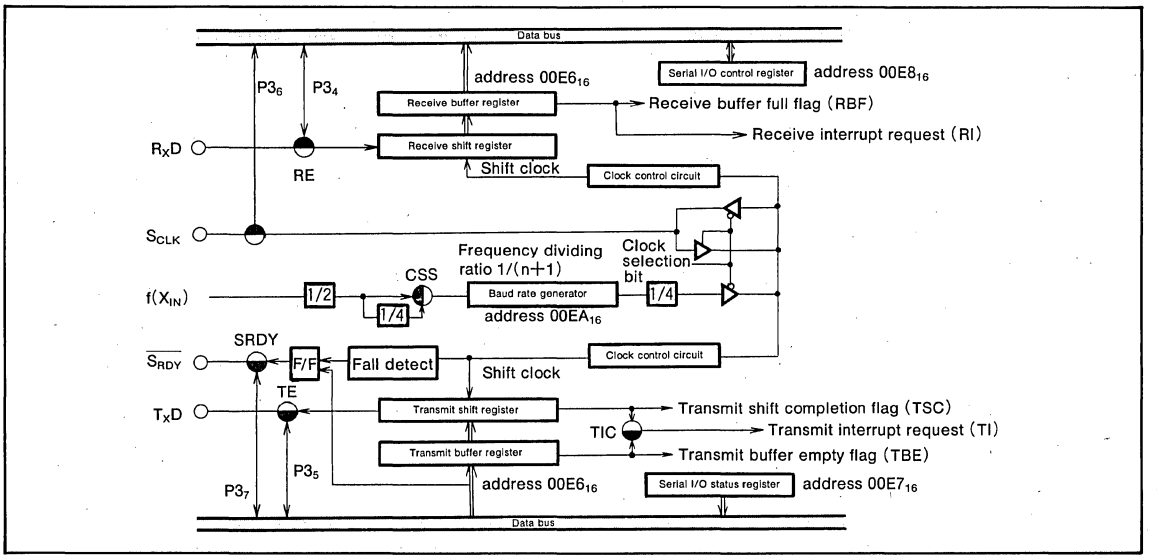
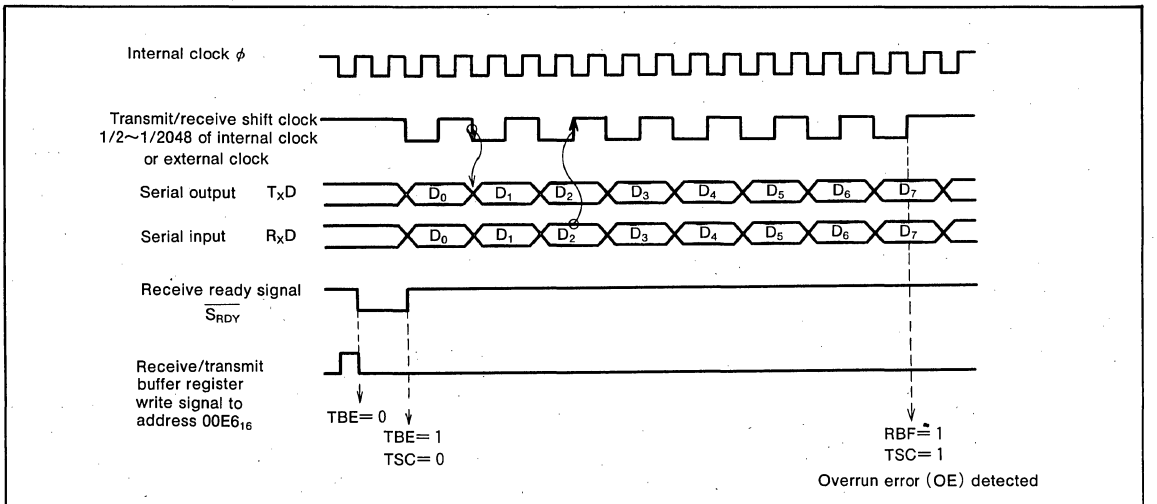


Fig. 17 Clock synchronous serial I/O block diagram



Note 1. Use the transmit interrupt source selection bit (TIC) in the serial I/O control register to specify whether to generate a transmit interrupt (TI) when the transmit buffer becomes empty (TBE=1) or when transmit shift operation completes (TSC=1).
Note 2. If data is written in the transmit buffer register when TSC=0, transmit clock is generated continuously and serial data is output continuously from the TxD pin.
Note 3. The receive interrupt (RI) is set when the receive buffer full flag (RBF) is set.

Fig. 18 Clock synchronous serial I/O operation

(2) Asynchronous Serial I/O (UART)

UART is selected by setting the mode selection bit of the serial I/O control register to "0". Figure 19 shows a block diagram of UART and Figure 20 shows its operation.

With the M37450, one of eight serial data transmission formats can be selected with the UART control register as shown in Figure 16. The transmission format must be agreed upon between the transmit side and the receive side.

The transmit shift register and the receive shift register has its buffer register respectively to perform serial data transfer (same memory addresses).

Data cannot be written or read directly to/from the shift registers. Therefore, the data to be transmitted is written to a buffer register and the received data is read from a buffer register. The buffer registers can also be used to store data to be transmitted next or to receive 2-byte data consecutively.

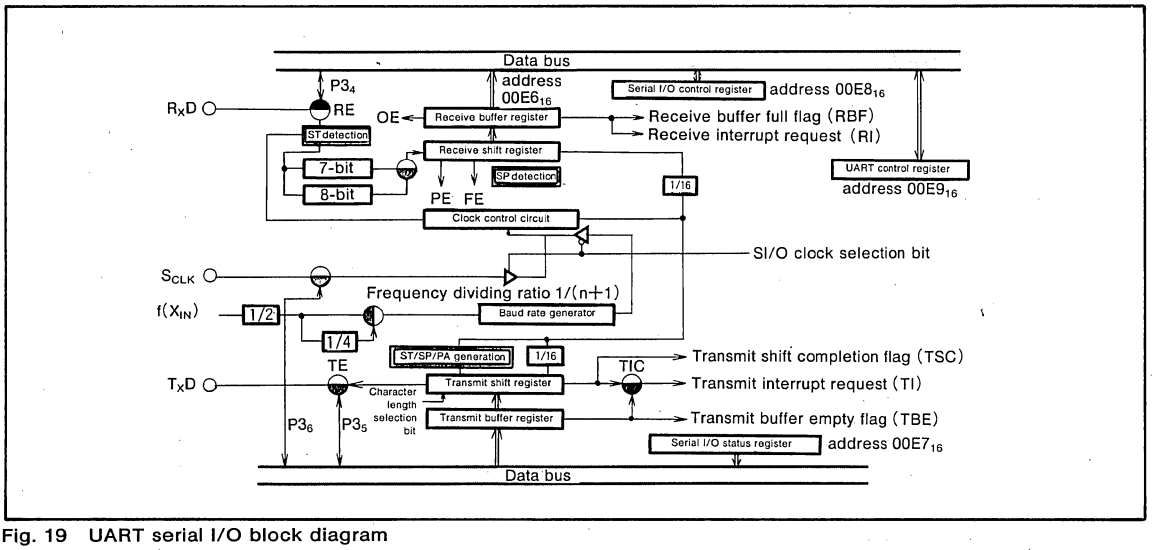
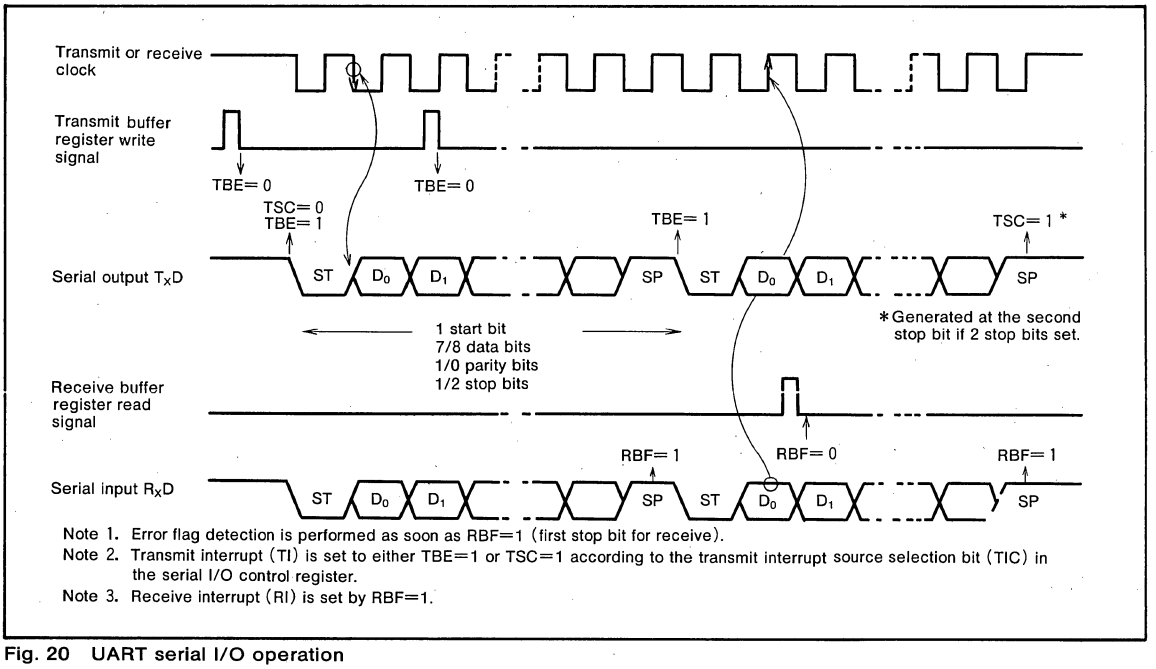


Fig. 19 UART serial I/O block diagram



Note 1. Error flag detection is performed as soon as RBF=1 (first stop bit for receive).
Note 2. Transmit interrupt (TI) is set to either TBE=1 or TSC=1 according to the transmit interrupt source selection bit (TIC) in the serial I/O control register.
Note 3. Receive interrupt (RI) is set by RBF=1.

Fig. 20 UART serial I/O operation

[Serial I/O Control Register] SIOCON

The serial I/O control register is an 8-bit register consisting of selection bits for controlling the serial I/O function.

• Serial I/O Enable Bit SIOE

When this bit is set to "1", serial I/O is enabled and pins $P3_4 \sim P3_7$ can be used as serial I/O function pins.

• Serial I/O Mode Selection Bit SIOM

This bit is used to select the serial I/O operation mode. When this bit is "0", asynchronous serial I/O (UART), which transfers data using start and stop bits, is selected. When it is "1", clock synchronous serial I/O which performs transmission and receive using the same clock is selected.

• Receive Enable Bit RE

Receive operation is enabled when this bit is set to "1" and pin $P3_4$ becomes a serial data input pin.

• Transmission Enable Bit TE

Transmission operation is enabled when this bit is set to "1". Pin $P3_5$ becomes a serial data output pin and shift data is output.

• Transmission Interrupt Source Selection Bit TIC

This bit is used to selelct events that can cause a transmission interrupt.

• $\overline{S_{RDY}}$ Output Enable Bit SRDY

If this bit is set to "1" when clock synchronous serial I/O is selected, pin $P3_7$ becomes an $\overline{S_{RDY}}$ signal output pin and $\overline{S_{RDY}}$ signal is output.

When an external clock is used during clock synchronous serial I/O, the $\overline{S_{RDY}}$ signal is used to notify the clock sender that it can send the serial clock signal. It goes "L" when data is written in the transmit/receive buffer register and goes "H" at the first fall of the receive clock. When using the $\overline{S_{RDY}}$ signal, the transmission enable bit must be set to "1" even when performing receive only.

• Serial I/O Synchronous Clock Selection Bit SCS

When this bit is "1", pin $P3_6$ becomes an input pin and the external clock input from the S_{CLK} pin is selected as the serial I/O synchronous clock. When this bit is "0", the baud rate generator (BRG) overflow signal is selected as the serial I/O synchronous clock. Also, when this bit is "0" during clock synchronous serial I/O, pin $P3_6$ becomes an output pin and the shift clock is output from the S_{CLK} pin.

When clock synchronous serial I/O is selected, the baud rate generator (BRG) output signal divided by four or an external clock input is used. When UART is selected, the BRG output signal divided by sixteen or an external clock input signal divided by sixteen is used.

• BRG Count Source Selection Bit CSS

The baud rate generator is an 8-bit counter with a reload register. By setting a value n in the BRG register (address $00EA_{16}$), the count source selected by the BRG count source selection bit is divided by (n+1).

[UART Control Register] UARTCON

The UART control regsiter is a 4-bit register consisting of control bits that are valid when UART is selected. The content of this register is used to set the data format for serial data transmission/receiving.

• Character Length Selection Bit CHAS

This bit is used to select the transmission/receiving character lenght.

• Parity Enable Bit PARE

When this bit is set to "1", a parity bit is added next to the most significant bit (MSB) of the transmission data and parity is checked during receive.

• Parity Selection Bit PARS

This bit is used to specify the type of parity to be generated during transmission and checked when data is received. The number of 1's in the data is set to even or odd according to this bit.

• Stop Bit Length Selection STPS

This bit is used to determine the number of stop bits to be used during transmission.

[Serial I/O Status Register] SIOSTS

The serial I/O status register is a 7-bit read only register consisting of serial I/O operation status flags and error flags. Bits 4 to 6 are valid only during UART mode.

All bits of this register are initialized to "0" at reset, and when the transmit enable bit in the serial I/O control register is set to "1", bits "0" and "2" change to "1".

• Transmission Buffer Empty Flag TBE

This bit is cleared to "0" when transmission data is written in the transmission buffer register and set to "1" when that data is transferred to the transmit shift register. It is also cleared when TE=0.

• Receive Buffer Full Flag RBF

When receiving serial data, data is transferred to the receive buffer register and this bit is set to "1" when the receive shift register completes receiving a data byte. This bit is cleared when the data is read. This bit is also cleared when RE=0.

• Transmit Shift Register Shift Completion Flag TSC

This bit is cleared to "0" when the data in the transmission buffer register is transferred to the transmit shift register and set to "1" when data shift completes. It is also set to "1" when TE=0.

• Overrun Error Flag OE

When continuously receiving serial data, this bit is set when the next data fill the receive shift register before the data in the receive buffer register has been read.

• Parity Error Flag PE

When receiving serial data with parity, this bit is set to "1 " if the parity of the received data differs from the specified parity.

• Framing Error Flag FE

This bit is set to "1" when there is no stop bit when transferring data from the receive shift register to the receive buffer.

• Summing Error Flag SE

This bit is set when either overrun, a parity, or a framing error occurs.

Tests for these errors are performed as soon as the data is transferred from the receive shift register to the receive buffer register and at the same time the receive buffer full flag is set. The error flags (OE, PE, FE, and SE) are cleared when any data is written in the serial I/O status register. Also, all status flags including error flags are cleared when SIOE=0.

BUS INTERFACE

The M37450 is equipped with a bus interface that is functionally similar to the MELPS 8-41 series. Its operation can be controlled with control signals from the host CPU (slave mode).

The M37450 bus interface can be connected directly to either a R/$\overline{W}$ type CPU or separate $\overline{RD}$, $\overline{WR}$ type CPU. Figure 21 shows a block diagram of the bus interface function. tion.

Slave mode is selected with MISRG2 (address $00DF_{16}$) bit 2 and 3 as shown in Figure 22.

An input buffer full interrpt occurs when data is received from the host CPU and an output buffer empty interrupt occurs when data is read by the host CPU.

In slave mode, ports $P5_0 \sim P5_7$ become a tri-state data bus used to transfer data, commands, and status to and from the host CPU.

Furthermore, ports $P6_4 \sim P6_7$ become host CPU control signal input pins and $P6_3$ becomes a slave status output pin.

[Data Bus Buffer Status Register] DBBSTS

This is an 8-bit register. Bits 0, 1, and 3 are read-only bits indicating the status of the data bus buffer. Bits 2, 4, 5, 6, and 7 are read/write enabled user-definable flags that can be set with a program. The host CPU can only read these flags by setting the A0 pin to "H".

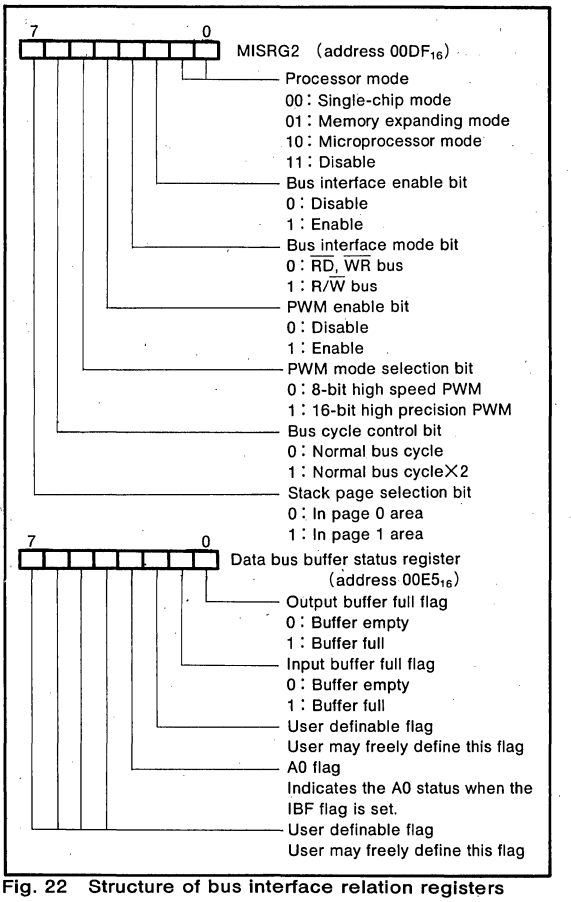


Fig. 22 Structure of bus interface relation registers

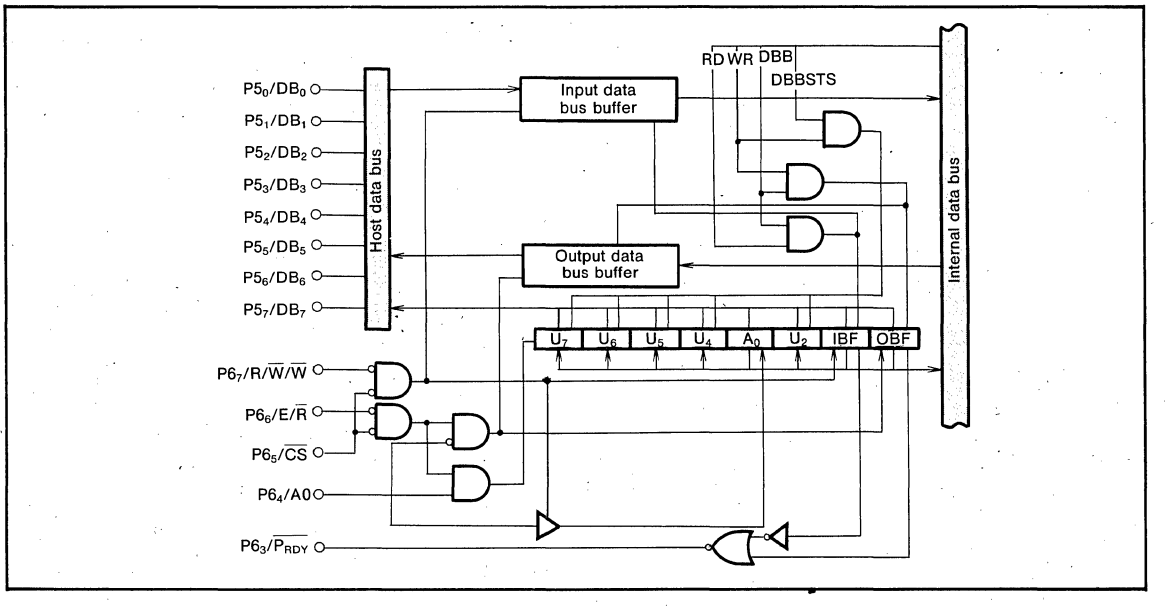


Fig. 21 Bus interface circuit diagram

MITSUBISHI ELECTRIC

• Output Buffer Full Flag OBF

This flag is set when data is written in the output data bus buffer and cleared when the host CPU reads the data in the output data bus buffer. It is initialized to "1" at reset and cleared to "0" when the slave mode is selected with the bus interface enable bit set.

• Input Buffer Full Flag IBF

This flag is set when the host CPU writes data in the input data bus buffer and cleared when the slave CPU reads the data in the input data bus buffer. This bit is initialized to "0" at reset.

A_0 Flag

The level of the A_0 pin is latched when the host CPU writes data in the input data bus buffer.

[Input Data Bus Buffer] DBBIN

Data on the data bus is latched in DBBIN when there is a write request from the host CPU. The data in DBBIN can be read from the data bus buffer register (SFR address $00E4_{16}$).

[Output Data Bus Buffer] DBBOUT

Data is written in DBBOUT by writing data in data bus buffer register (SFR address $00E4_{16}$). The data in DBBOUT is output to the data bus (P5) when the host CPU issues a read request with setting the A_0 pin to "L".

Table 2. Control I/O pin functions when bus interface function is selected

Pin	Name	Bus interface mode bit	Input/ Output	Function
$P6_3$	$\overline{P_{RDY}}$	—	Output	Status output. The NOR of OBF and IBE is outnput.
$P6_4$	A_0	—	Input	Address input. Used to select between DBBSTS and DBBOUT during host CPU read. Also used to identify commands and data during write.
$P6_5$	CS	—	Input	Chip select input. Used to select the data bus buffer. Select when "L".
$P6_6$	$\overline{R}$	0	Input	Timing signal used by the host CPU to read data from the data bus buffer.
	E	1	Input	Inputs a timing signal E or inverse of ϕ.
$P6_7$	$\overline{W}$	0	Input	Timing signal used by the host CPU to write data to the data bus buffer.
	R/$\overline{W}$	1	Input	Input R/$\overline{W}$ signal used to control the data transfer direction. When this signal is "L", data bus buffer write is synchronized with the E signal. When it is "H", data bus buffer read is synchronized with the E signal.

PWM

The PWM generator has two program-selectable modes; the high-speed mode (8-bit resolution) and the high-precision mode (16-bit resolution). Figure 23 shows a block diagram.

The register MISRG2 (address $00DF_{16}$) shown in Figure 22 is used to enable/disable the PWM and change its mode. When the PWM enable bit is set, the PWM timer starts from its initial state.

As shown in Figure 24, the output frequency is

$(2X255)/f(X_{IN})$ 51μs at $f(X_{IN})$=10MHz

in high-speed mode and

$(2X65535)/f(X_{IN})$ 13.107ms at $f(X_{IN})$=10MHz

in high-precision mode.

The "H" width of the output pulse is determined by setting a value only in the PWM_L register for high-speed mode and in both the PWM_H and PWM_L in this order for high-precision mode.

If the value set in the PWM register is m, the "H" width of the output pulse is

(PWM period×m)/255 for high-speed mode and

(PWM period×m)/65535 for high-precision mode.

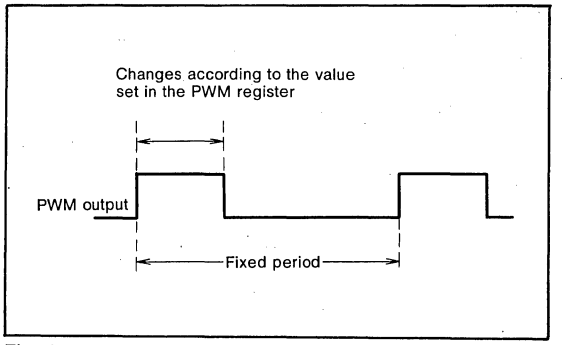


Fig. 24 PWM output

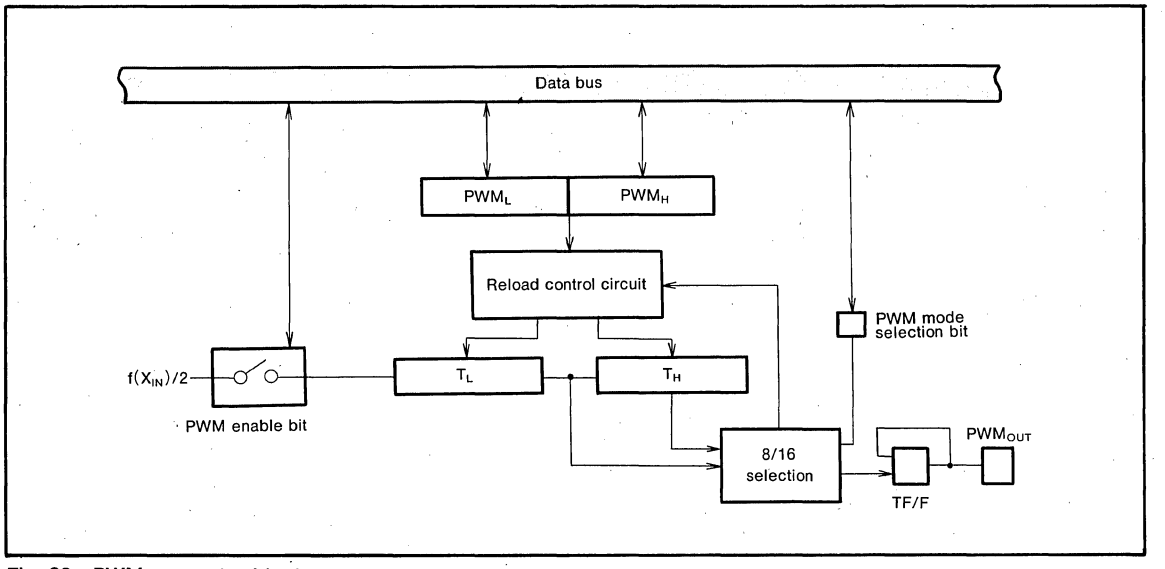


Fig. 23 PWM generator block diagram

A-D CONVERTER

An A-D converter is an 8-bit successive approximation method. Figure 25 shows a block diagram of the A-D converter.

The 64-pin model has three analog voltage input pins; the 80-pin model has eight.

A-D conversion is started by a write operation to the analog input pin selection bit of the A-D control register shown in Figure 26 and by selecting the analog voltage input pin. The A-D interrupt request bit in the interrupt request register 2 is set when A-D conversion completes. The result of A-D conversion is stored in the A-D register.

The contents of the A-D register must not be read during A-D conversion and f(X_{IN}) must be no less than 1 MHz during A-D conversion.

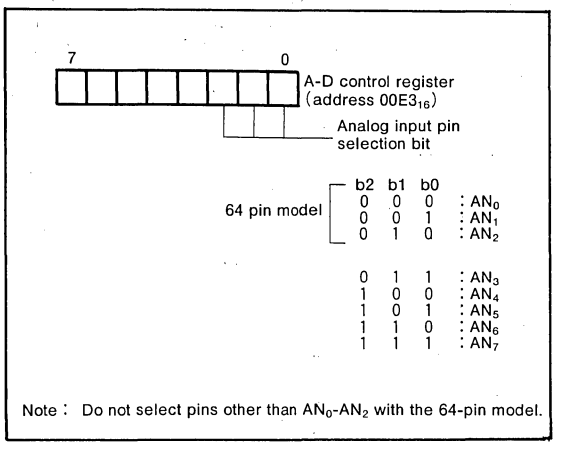


Fig. 26 Structure of A-D control register

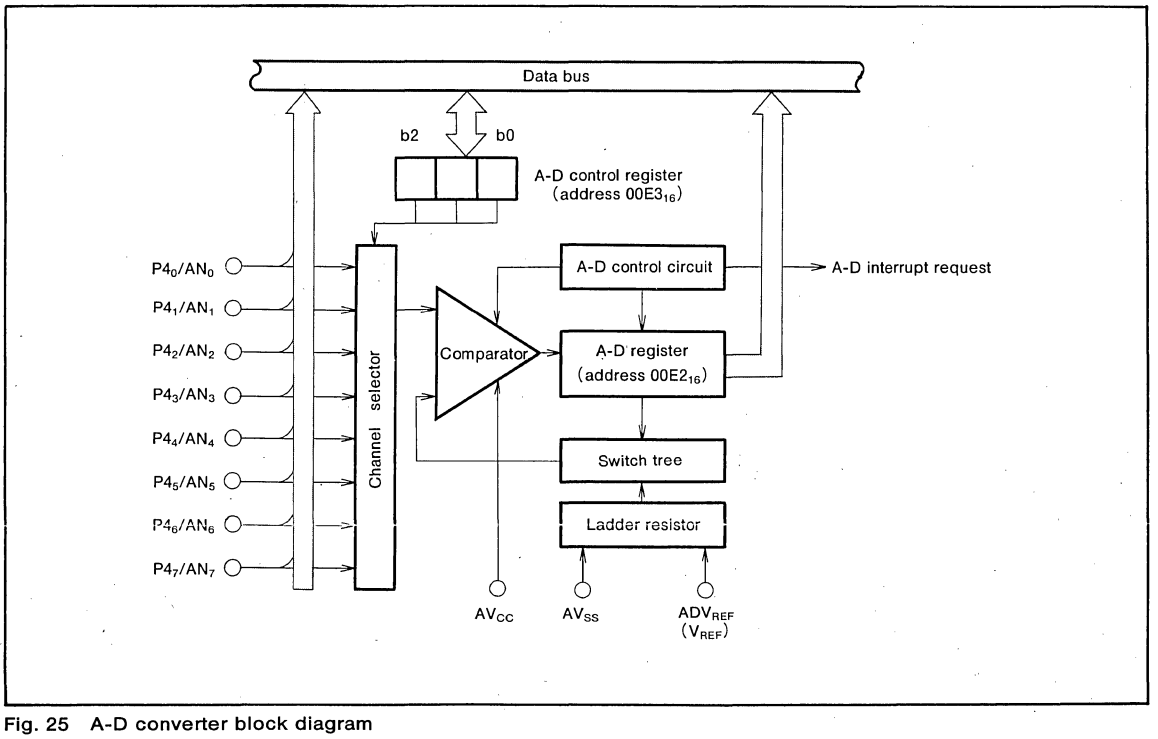


Fig. 25 A-D converter block diagram

D-A CONVERTER

Two 8-bit resolution D-A converter channels are provided. Figure 27 shows a block diagram of the D-A converter.

D-A conversion is performed by setting a value in the D-Ai register (addresses $00E0_{16}$ and $00E1_{16}$). The result of D-A conversion is output from the D-Ai output pin.

The output analog voltage V_{DA} is determined by the value n (decimal) set in the D-Ai register as follows:

$V_{DA} = DAV_{REF}{}^{*} \times n/256$

$^{*}V_{REF}$ for 64-pin model.

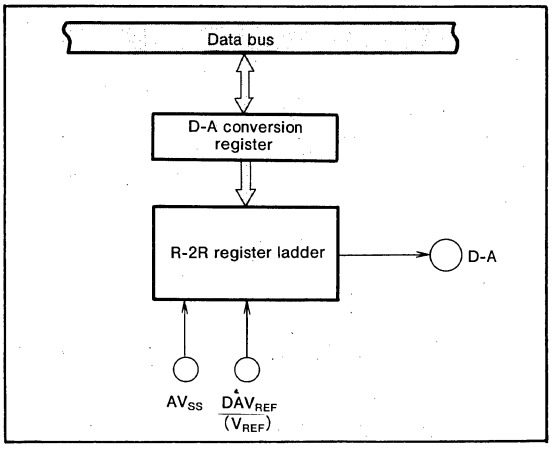


Fig. 27 D-A converter block diagram

RESET CIRCUIT

The M37450 is reset according to the sequence shown in Figure 30. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for no less than 2μs while the power voltage is 5V±10% and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 28.

An example of the reset circuit is shown in Figure 29. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.

	address	
(1) Port P0 directional register	$00D1_{16}$	00_{16}
(2) Port P1 directional register	$00D3_{16}$	00_{16}
(3) Port P2 directional register	$00D5_{16}$	00_{16}
(4) Port P3 directional register	$00D7_{16}$	00_{16}
(5) Port P4 directional register	$00DB_{16}$	00_{16}
(6) Port P5 directional register	$00DD_{16}$	00_{16}
(7) MISRG1	$00DE_{16}$	0 0 0 0 0 0
(8) MISRG2	$00DF_{16}$	00_{16}
(9) D-A1 register	$00E0_{16}$	00_{16}
(10) D-A2 register	$00E1_{16}$	00_{16}
(11) Data bus buffer status register	$00E5_{16}$	0 1
(12) Serial I/O status register	$00E7_{16}$	0 0 0 0 0 0 0
(13) Serial I/O control register	$00E8_{16}$	00_{16}
(14) UART control register	$00E9_{16}$	0 0 0 0
(15) Timer 1 control register	$00ED_{16}$	0 0 0 0 0 0
(16) Timer 2 control register	$00EE_{16}$	0 0 0 0 0 0
(17) Timer 3 control register	$00EF_{16}$	0 0 0 0 0 0
(18) Timer 1 register (low order)	$00F0_{16}$	FF_{16}
(19) Timer 2 register (high order)	$00F1_{16}$	03_{16}
(20) Interrupt request register 1	$00FC_{16}$	00_{16}
(21) Interrupt request register 2	$00FD_{16}$	0 0 0 0 0 0
(22) Interrupt control register 1	$00FE_{16}$	00_{16}
(23) Interrupt control register 2	$00FF_{16}$	0 0 0 0 0 0
(24) Processor status register	(PS)	1
(25) Program counter	(PC_H)	Contents of address $FFFF_{16}$
	(PC_L)	Contents of address $FFFE_{16}$

Note. Since the contents of both registers other than those listed above (including timer 1, timer 2, timer 3, and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values.

Fig. 28 Internal state of microcomputer at reset

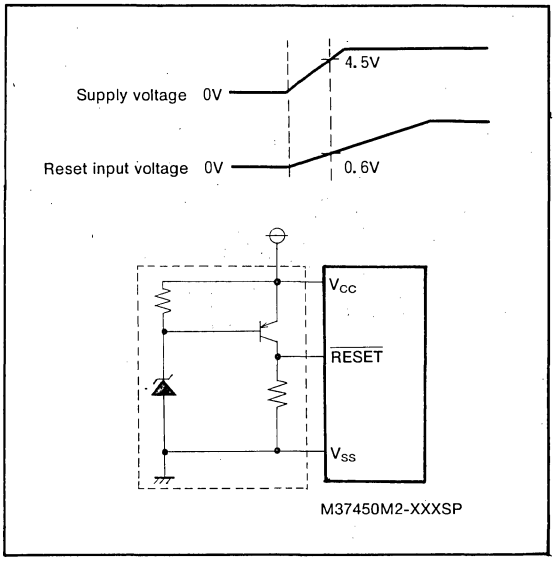


Fig. 29 Example of reset circuit

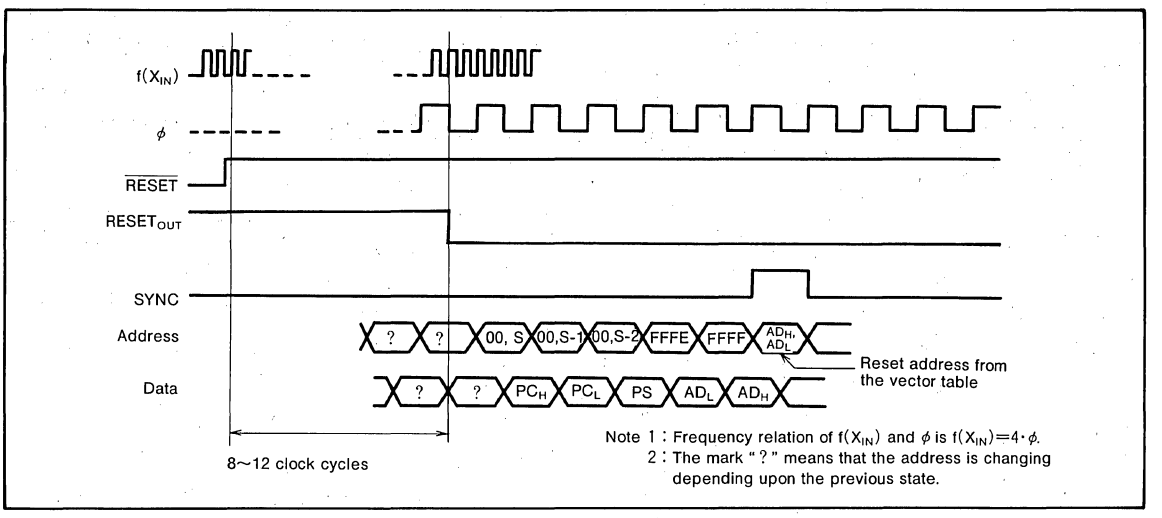


Fig. 30 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 2), port P0 can be accessed at zero page memory address $00D0_{16}$.

Port P0 has a directional register (address $00D1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously ouptut value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00DF_{16}$), three different modes can be selected; single-chip mode, memory expanding mode and microprocessor mode.

In these modes it functions as address ($A_7 \sim A_0$) output port (excluding single-chip mode). For more details, see the processor mode information.

(2) Port P1

In single-chip mode, port P1 has the same function as port P0. In other modes, it functions as address ($A_{15} \sim A_8$) output port.

Refer to the section on processor modes for details.

(3) Port P2

In single-chip mode, port P2 has the same function as port P0. In other modes, it functions as data ($D_0 \sim D_7$) input/output port. Refer to the section on processor modes for details.

(4) Port P3

Port P3 is an 8-bit I/O port with function similar to port P0. All pins have program selectable dual functions. When a serial I/O function is selected, the input and output from pins $P3_4 \sim P3_7$ are determined by the contents of the serial I/O registers.

This port is unaffected by the processor mode.

(5) Port P4

This is an input-only port and may be used as an analog votage input port. The number of ports is different for the 64-pin model and 80-pin model. The 64-pin model has three ports and the 80-pin model has eight ports.

(6) Port P5

This is an 8-bit I/O port with function similar to port P0.

When slave mode is selected with a program, all ports change to the data bus for the master CPU. In this case, port input/output is unaffected by the directional register.

This port is unaffected by the processor mode register.

(7) Port P6

This is an 8-bit input/output port with function similar to port P0.

When slave mode is selected with a program, ports $P6_3 \sim P6_7$ change to the control bus for the bus interface function. In this case, port input/output is unaffected by the directional register.

Ports $P6_0 \sim P6_2$ are shared with the external interrupt input pins ($INT_1 \sim INT_3$). The INT interrupt constantly monitors the status of this port and generates an interrupt at a valide edge. Therefore, if the INT interrupt is not used, it must be disabled and if it is used, this port must be set to input.

(8) Port D-A

Port D-A consists of two analog voltage output pins. Any analog voltage can be generated by setting a value in the D-A register.

(9) ϕ pin

The internal system clock (1/4 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) is output from this pin. If an STP or WIT instruction is executed, output stops after going "H".

(10) SYNC pin

This pin outputs a signal that is "H" during one cycle of the ϕ during operation code fetch.

(11) R/$\overline{W}$ pin

This is a control signal output pin that indicates the local bus direction in memory expanding and microprocessor modes.

(12) $\overline{RD}$, $\overline{WR}$ pins

These are local bus write and read timing signal output pins for memory expanding and microprocessor modes. A signal equivalent to the signal otuput from the R/$\overline{W}$ separated by the ϕ signal is output.

These pins are used exclusively by the 80-pin model.

(13) $RESET_{OUT}$ pin

This pin goes "H" while the microprocessor is being reset. It can be used as a reset signal output pin for peripheral devices.

This pin is used exclusively by the 80-pin model.

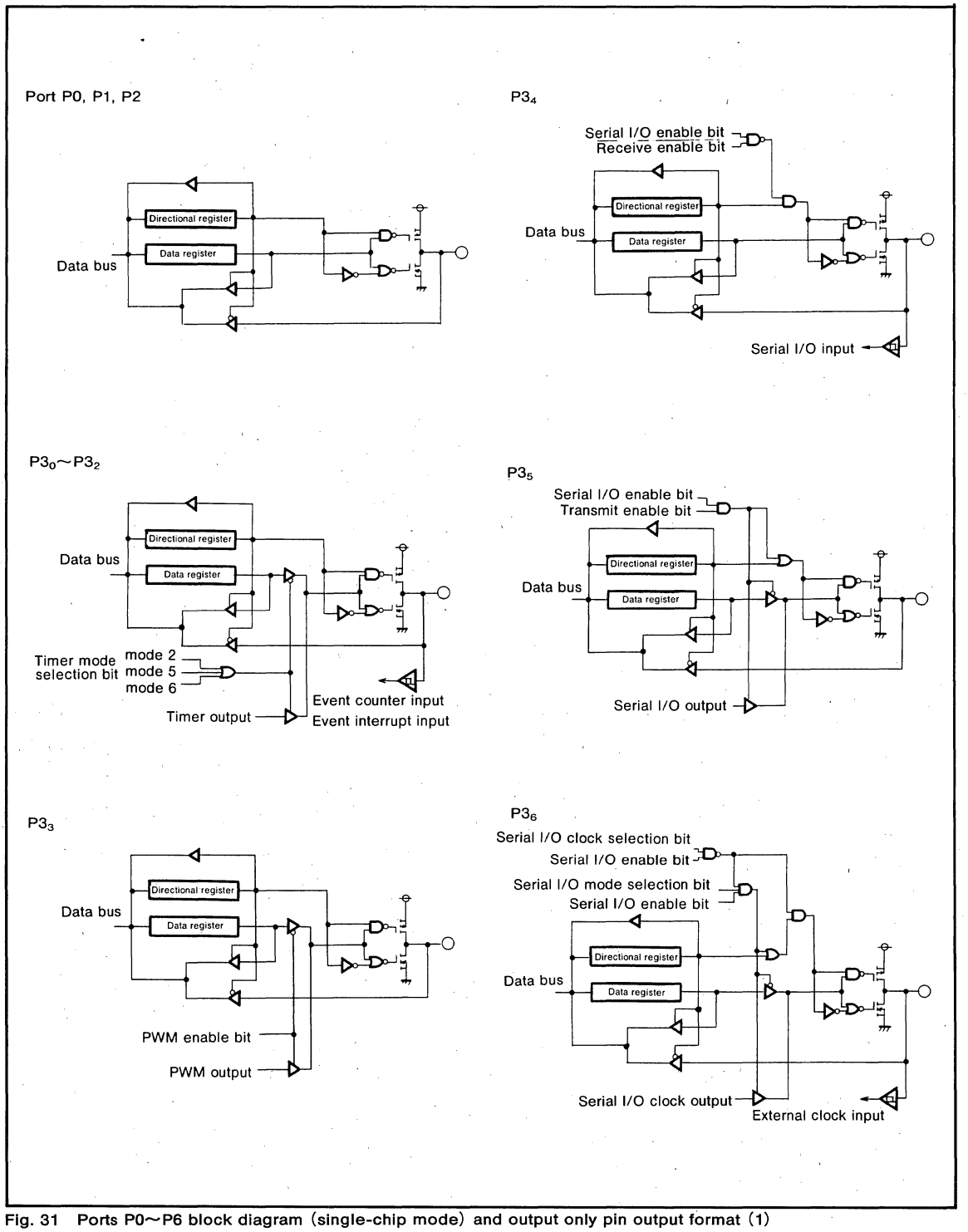


Fig. 31 Ports P0~P6 block diagram (single-chip mode) and output only pin output format (1)

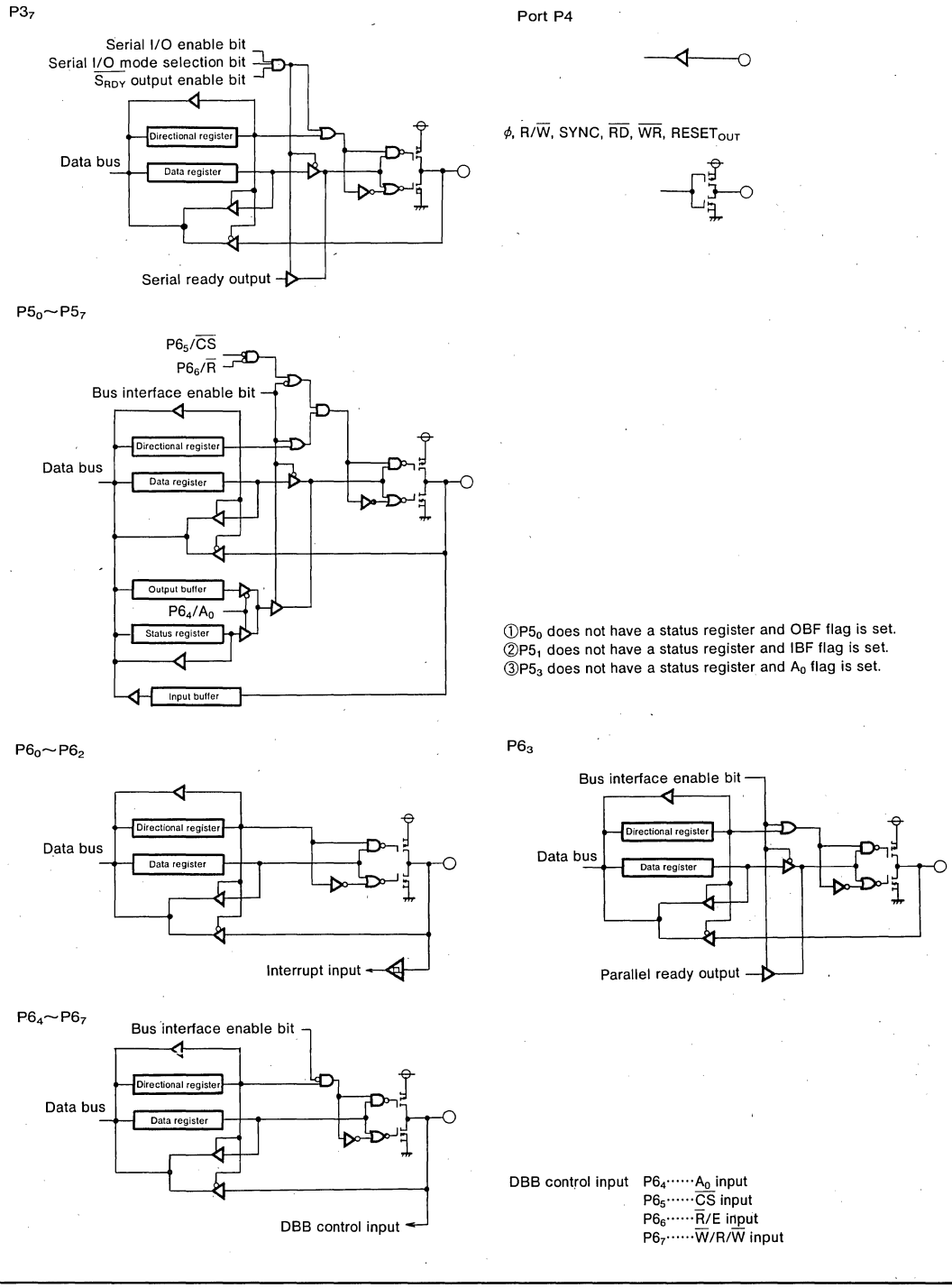


Fig. 32 Ports P0~P6 block diagram (single-chip mode) and output only pin output format (2)

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00DF_{16}$), three different operation modes can be selected; single-chip mode, memory expanding mode, and microprocessor mode.

In the memory expanding mode and the microprocessor mode, ports P0～P2 can be used as address, and data input/output pins.

Figure 34 shows the functions of ports P0～P2.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 33.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode.

The three different modes are explained as follows:

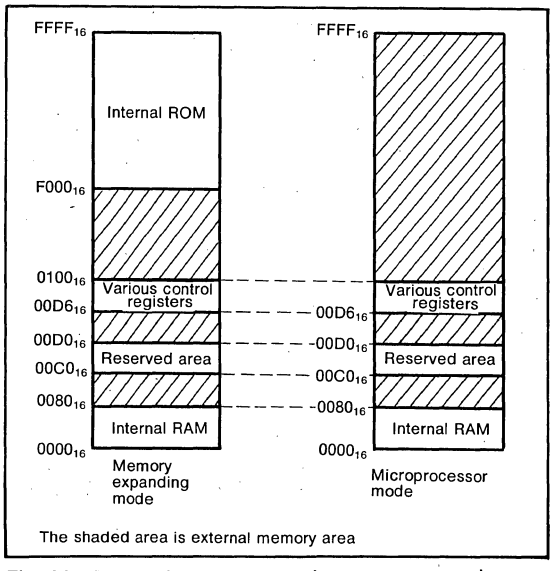


Fig. 33 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P2 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memroy expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost.

Port P2 becomes the data bus of D_7～D_0 (including instruction code) and loses its normal I/O functions.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset or connecting CNV_{SS} to V_{SS} and the processor mode bits are set to "10", the microcomputer will automatically default to this mode. In this mode, the internal ROM is inhibited so the external memory is required. Other functions are same as the memory expanding mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 3.

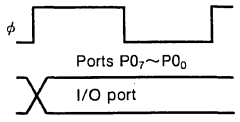
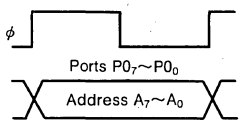
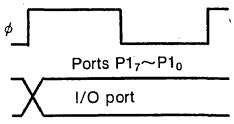
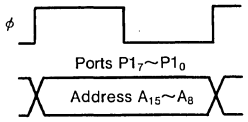
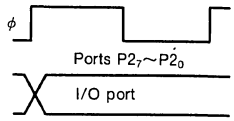
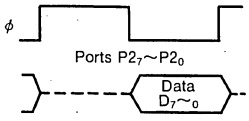
Mode / Port	CM_1 = 0, CM_0 = 0	CM_1 = 0, CM_0 = 1	CM_1 = 1, CM_0 = 0
	Single-chip mode	Memory expanding mode	Microprocessor mode
Port P0			Same as left
Port P1			Same as left
Port P2			Same as left

Fig. 34 Processor mode and function of port P0~P2

Table 3 Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Microprocessor mode	The microprocessor mode is set by the reset.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 37.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, FF_{16} is set in the low-order byte of timer 1, 03_{16} is set in the high-order byte, and timer 1 count source is forced to $f(X_{IN})$ divided by four. This connection is cleared when timer 1 overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the clock ϕ keeps its "H" level until timer 1 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer 1 count enable bit must be set to "1" and the timer 1 interrupt enable bit must be set to "0" before executing STP instruction.

With the M37450, the MISRG2 bit 6 shown in Figure 22 can be used to double the bus cycle. However, the timer, UART, and PWM operations are unafffected. This facilitates accessing of slow peripheral LSIs when external memory and I/O are extended in memory expanding mode or microprocessor mode. Note that this bit also affects the bus cycle in single-chip mode.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 35.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 36. X_{IN} is the input, and X_{OUT} is open.

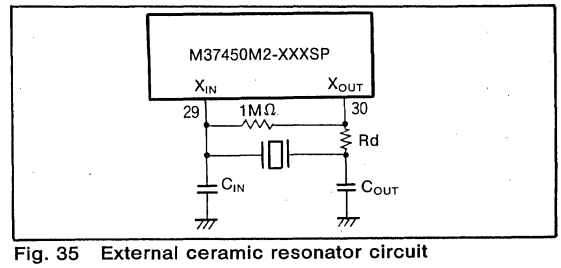


Fig. 35 External ceramic resonator circuit

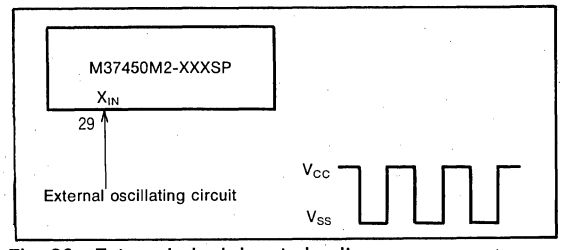


Fig. 36 External clock input circuit

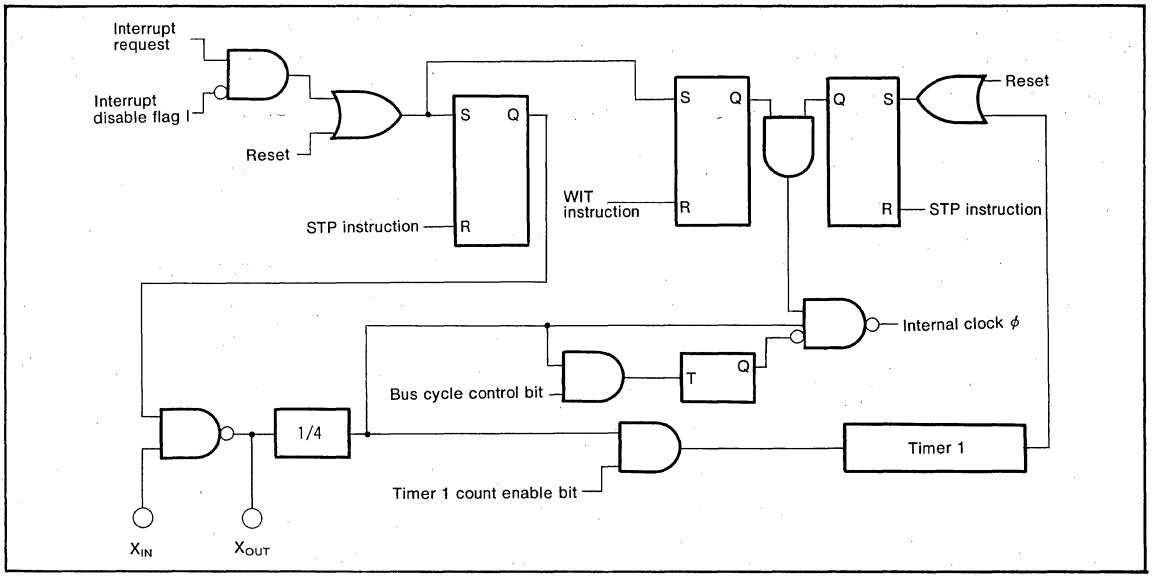


Fig. 37 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) Processor status register

1. Except for the interrupt inhibit flag (I) being set to "1", the content of the processor status register (PS) is unpredictable after a reset. Therefore, flags affecting program execution must be initialized.
   The T flag and D flag which affect arithmetic operations, must always be initialized.
2. A NOP instruction must be used after the execution of a PLP instruction.

(2) Interrupts

Even though the BBC and BBS instructions are executed just after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) Decimal operations

1. Decimal operations are performed by setting the decimal mode flag (D) and executing the ADC or SBC instruction. In this case, there must be at least one instruction following the ADC or SBC instruction before executing the SEC, CLC, or CLD instruction.
2. The N (Negative), V(Overflow), and Z(Zero) flags are ignored during decimal mode.

(4) Timers

1. The frequency dividing ratio when n (0～65535) is written in the timer latch is 1/(n+1).
2. When directly writing a value in the timer, set the count enable bit to count disable (0) and write in the low-order byte first and then in the high-order byte.
3. The timer value must be read from the high-order byte first.

(5) Serial I/O

In clock synchronous serial I/O mode, if the receiver is to output an $\overline{S_{RDY}}$ using an external clock, the receive enable bit, $\overline{S_{RDY}}$ output enable bit, and transmission enable bit must be set to "1".

(6) A-D conversion

The comparator consists of coupling capacitors that lose their charge when the clock frequency is low. Therefore,f(X_{IN})must be no less than 1MHz during A-D conversion. (If the bus cycle control bit is "1", the bus cycle is doubled and the A-D conversion time is also doubled, therefore, f (X_{IN}) must not be less than 2MHz.) Also, the STP and WIT instructions must not be executed during A-D conversion.

(7) STP instruciton

The STP instruction must be executed after setting the timer 1 count enable bit (bit 4 at address $00DE_{16}$) to enable ("1").

(8) Multiply/Divide instructions

1. The MUL and DIV instructions are not affected by the T and D flags.
2. The contents of the processor status register are unaffected by multiply or divide instructions.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- mask ROM order confirmation form
- mark specification form
- ROM data·····EPROM 3 sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state.	−0.3∼7	V
V_I	Input voltage X_{IN}, $\overline{RESET}$		−0.3∼7	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3∼13	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, X_{OUT}, ϕ, R/$\overline{W}$, $\overline{RD}$, $\overline{WR}$, SYNC, $RESET_{OUT}$		−0.3∼V_{CC}+0.3	V
Pd	Power dissipation	T_a = 25℃	1000(Note 1)	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : 500mW in case of the flat package

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−10∼70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 2)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (expect Note 2)	2.0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note 2)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (expect Note 2)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 3)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 3)			−5	mA
$f(X_{IN})$	Internal clock oscillating frequency	1		10	MHz

Note 2 : Ports operating as special function pins INT_1∼INT_3($P6_0$∼$P6_2$), EV_1∼EV_3($P3_0$∼$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)

Note 3 : $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average current in 100ms.

Note 4 : The total of I_{OL} of Port P0, P1 and P2 should be 40mA (max.).
The total of I_{OL} of Port P3, P5, P6, R/$\overline{W}$ SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ should be 40mA (max.).
The total of I_{OH} of Port P0, P1, and P2 should be 40mA (max.).
The total of I_{OH} of Port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$, and ϕ should be 40mA (max.).

ELECTRIC CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=−10~70℃, f(X_{IN})=10MHz)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH} = − 2 mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OH} = − 5 mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL} =2 mA			0.45	V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OL} =5 mA			1	V
V_{T+} − V_{T-}	Hysteresis INT_1~$_3$($P6_0$~$P3_2$), EV_1~$_3$($P3_0$~$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
V_{T+} − V_{T-}	Hysteresis $\overline{RESET}$				0.7	V
V_{T+} − V_{T-}	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I =V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I =V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	f(X_{IN})=10MHz At system operation		6	10	mA
		At stop mode (Note 5)		1	10	μA

Note 5 : The terminals $\overline{RD}$, $\overline{WR}$, SYNC, R/$\overline{W}$, $RESET_{OUT}$, ϕ, X_{OUT}, D-A_1 and D-A_2 are all open.The other ports, which are in the input mode, are connected to V_{SS}. A-D converter is in the A-D completion state. The current through ADV_{REF} and DAV_{REF} is not included. (Fig. 41)

A-D CONVERTER CHARACTERISTICS

(V_{CC}=AV_{CC}= 5 V, V_{SS}=AV_{SS}= 0 V, T_a =25℃, f(X_{IN})=10MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5.12V		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_{c(\phi)}$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}= 5 V	2	7.5	10	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}= 5 V	0.5	0.7	2.5	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC}= 5 V, V_{SS}=AV_{SS}= 0 V, T_a =25℃ unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Full scale deviation	V_{CC}=DAV_{REF}=5V			1.0	%
t_{SU}	Set time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current		0	2.5	5	mA

TIMING REQUIREMENTS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig.38	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_C(X_{IN})$	External clock input cycle time		100		1000	ns
$t_W(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_W(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig.39	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A_0 setup time		40			ns
$t_{su(A-W)}$	A_0 setup time		40			ns
$t_{h(R-A)}$	A_0 hold time		10			ns
$t_{h(W-A)}$	A_0 hold time		10			ns
$t_{W(R)}$	Read pulse width		160			ns
$t_{W(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig.39	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A_0 setup time		40			ns
$t_{h(E-A)}$	A_0 hold time		10			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		10			ns
$t_{W(EL)}$	Enable clock "L" pulse width		160			ns
$t_{W(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(D-\phi)}$	Data input setup time	Fig.40	130			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-RD)}$	Data input setup time		130			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

SWITCHING CHARACTERISTICS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.38			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{C(\phi)}$	Cycle time		400		4000	ns
$t_{W(\phi H)}$	ϕ clock pulse width ("H" level)		190			ns
$t_{W(\phi L)}$	ϕ clock pulse width ("L" level)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(R-D)}$	Data output enable time after read	Fig.39			120	ns
$t_{V(R-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(R-PR)}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(E-D)}$	Data output enable time after read	Fig.39			120	ns
$t_{V(E-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-A)}$	Address delay time after ϕ	Fig.40			150	ns
$t_{V(\phi-A)}$	Address effective time after ϕ		10			ns
$t_{V(RD-A)}$	Address effective time after $\overline{RD}$		10			ns
$t_{V(WR-A)}$	Address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	Data output delay time after ϕ				160	ns
$t_{d(WR-D)}$	Data output delay time after $\overline{WR}$				160	ns
$t_{V(\phi-D)}$	Data output effective time after ϕ		20			ns
$t_{V(WR-D)}$	Data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				150	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				150	ns
$t_{W(RD)}$	$\overline{RD}$ pulse width		170			ns
$t_{W(WR)}$	$\overline{WR}$ pulse width		170			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V
V_{IL} 0.45V
Output test level : V_{OH} 2.0V
V_{OL} 0.8V

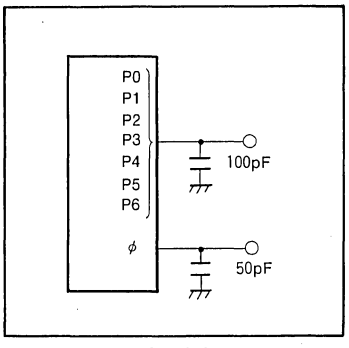


Fig. 38 Test circuit in single-chip mode

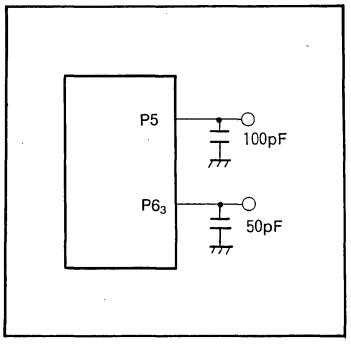


Fig. 39 Master CPU bus interface test circuit

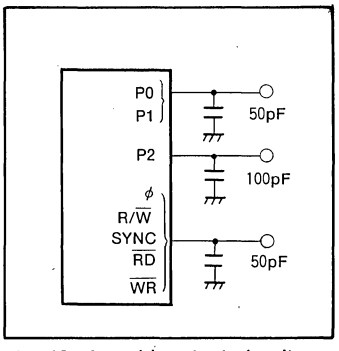


Fig. 40 Local bus test circuit

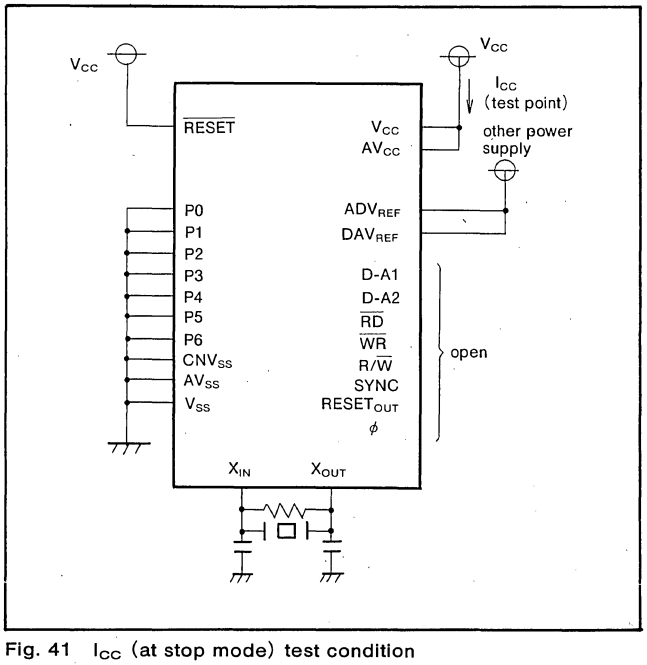
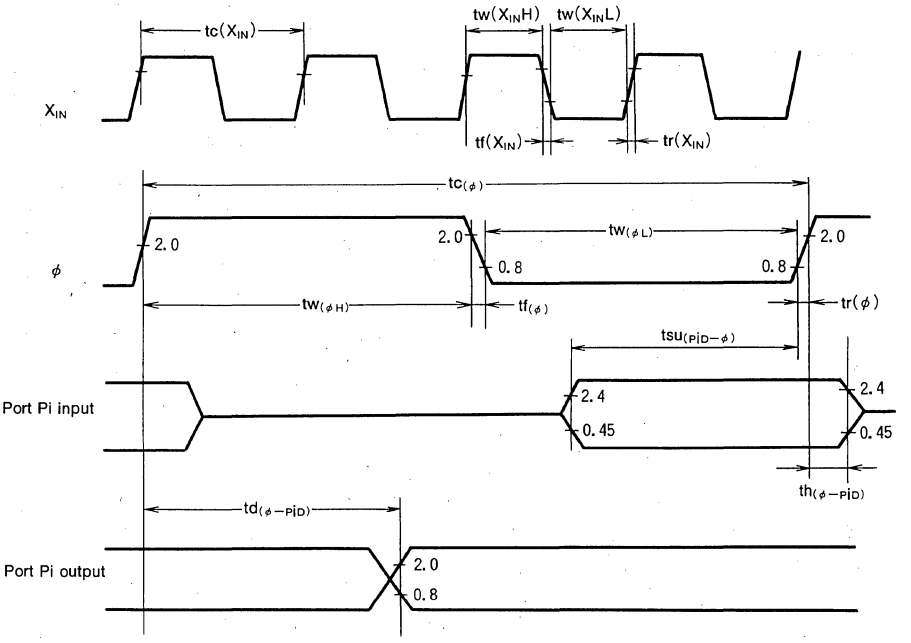


Fig. 41 I_{CC} (at stop mode) test condition

TIMING DIAGRAM

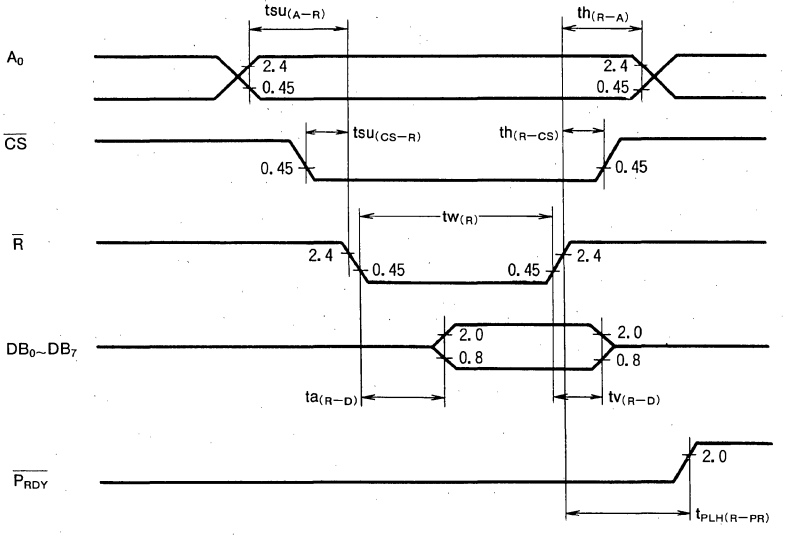
Port/single-chip mode timing diagram



Note : V_{IH}=0.8V_{CC}, V_{IL}=0.16V_{CC} of X_{IN}

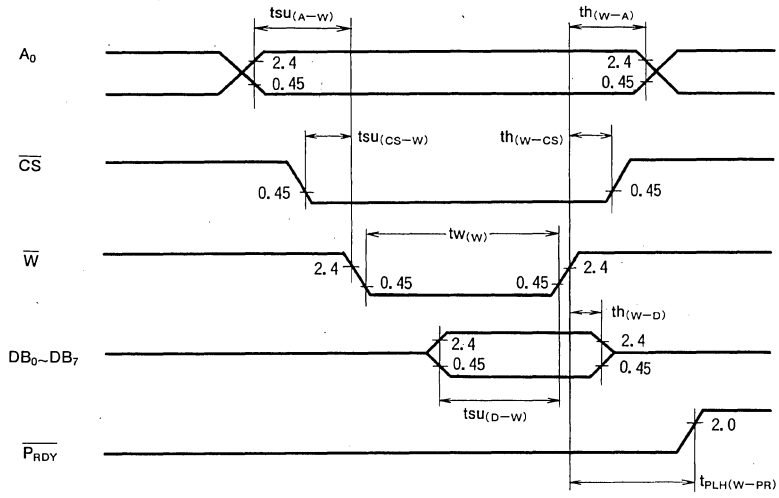
Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

Read

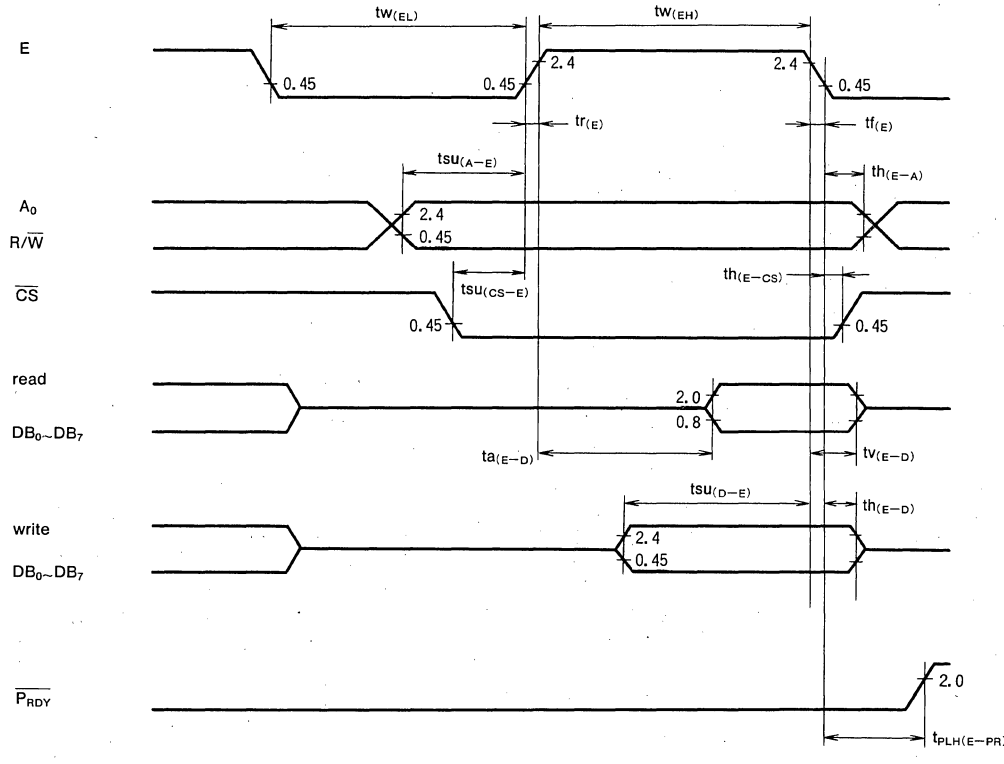


MITSUBISHI ELECTRIC

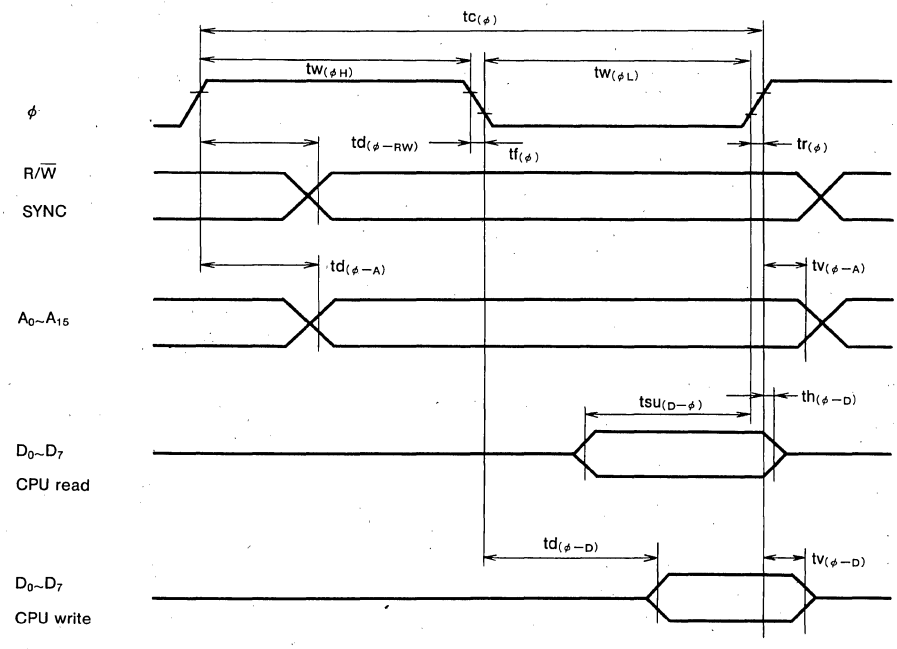
Write

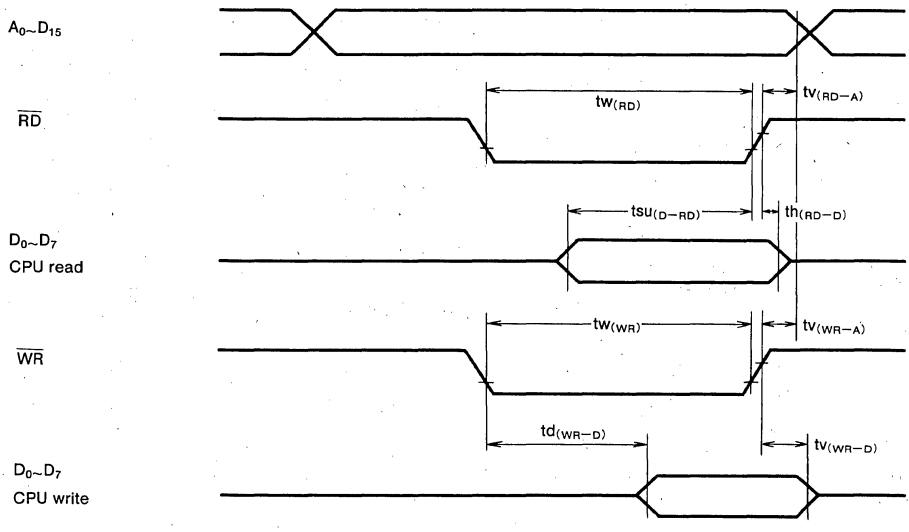


Master CPU interface/ R/$\overline{W}$ type timing diagram



Local bus timing diagram





M37450S1SP/FP, M37450S2SP/FP M37450S4SP/FP

8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37450S1SP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 80-pin plastic molded QFP. In addition to its simple instruction sets, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming. It is suited for office automation equipment and control devices. The low power consumption made possible by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

M37450S1SP/FP, M37450S2SP/FP and M37450S4SP/FP have basically the same functions as M37450M2-XXXSP/FP except the RAM size and the fact that these three need external ROM area. The differences among M37450S1SP/FP, M37450S2SP/FP and M37450S4SP/FP are as shown below.

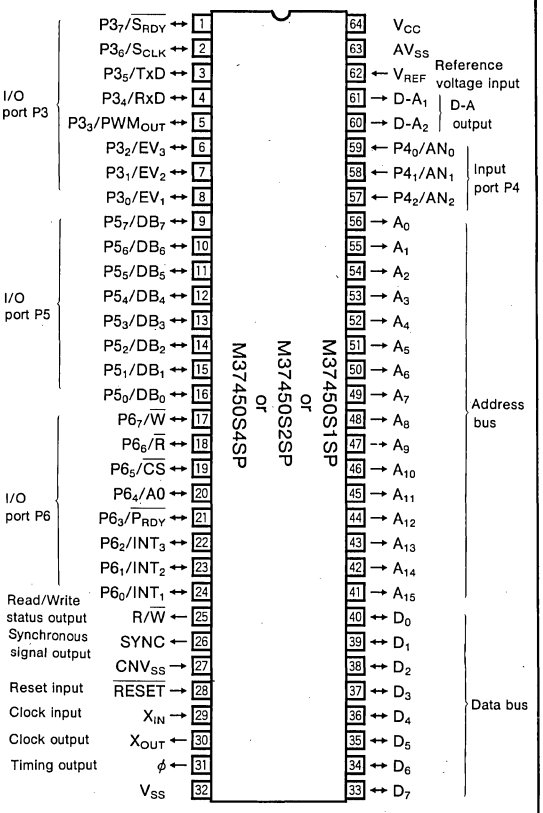
Type	RAM size
M37450S1SP/FP	128 bytes
M37450S2SP/FP	256 bytes
M37450S4SP/FP	448 bytes

Also M37450S1SP has the same function as M37450M2-XXXSP/FP in microprocessor mode and M37450S2SP/FP has the same function as M37450M4-XXXSP/FP in microprocessor mode.

DISTINCTIVE FEATURES

- Number of basic instructions 71
  69 MELPS 740 basic instructions + 2 multiply/divide instructions
- Memory size ROM ..... None
  RAM ..... 128 bytes (M37450S1SP/FP)
  256 bytes (M37450S2SP/FP)
  448 bytes (M37450S4SP/FP)
- Instruction execution time
  (Shortest instruction at 10 MHz) ..... 0.8μs(min.)
- Single power supply ..... 5V$\pm$10%
- Power dissipation normal operation mode
  (at 10MHz frequency) 30mW
- Subroutine nesting ..... 64 levels max. (M37450S1SP/FP)
- Interrupts ..... 15 events
- Master CPU bus interface ..... 1 byte
- 16-bit timer 3
- 8-bit timer (Serial I/O use) 1
- Serial I/O (UART or clock synchronous) 1
- A-D converter (8bit resolution) ..... 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ..... 2 channels
- PWM output (8-bit or 16-bit) 1
- Programmable I/O
  (Ports P0, P1, P2, P3, P5, P6) 48
- Input (Port P4) ..... 3 (DIP), 8 (QFP)
- Output (Port D-A_1, D-A_2) 2

PIN CONFIGURATION (TOP VIEW)

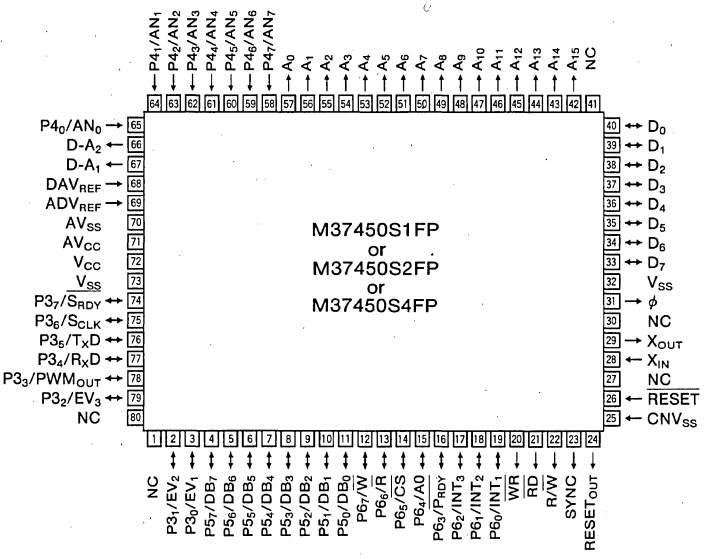


Outline 64P4B

APPICATION

Slave controller for PPCs, facsimiles and page printers
HDD, optical disk, inverter and industrial motor controllers
Industrial robots and machines

PIN CONFIGURATION (TOP VIEW)

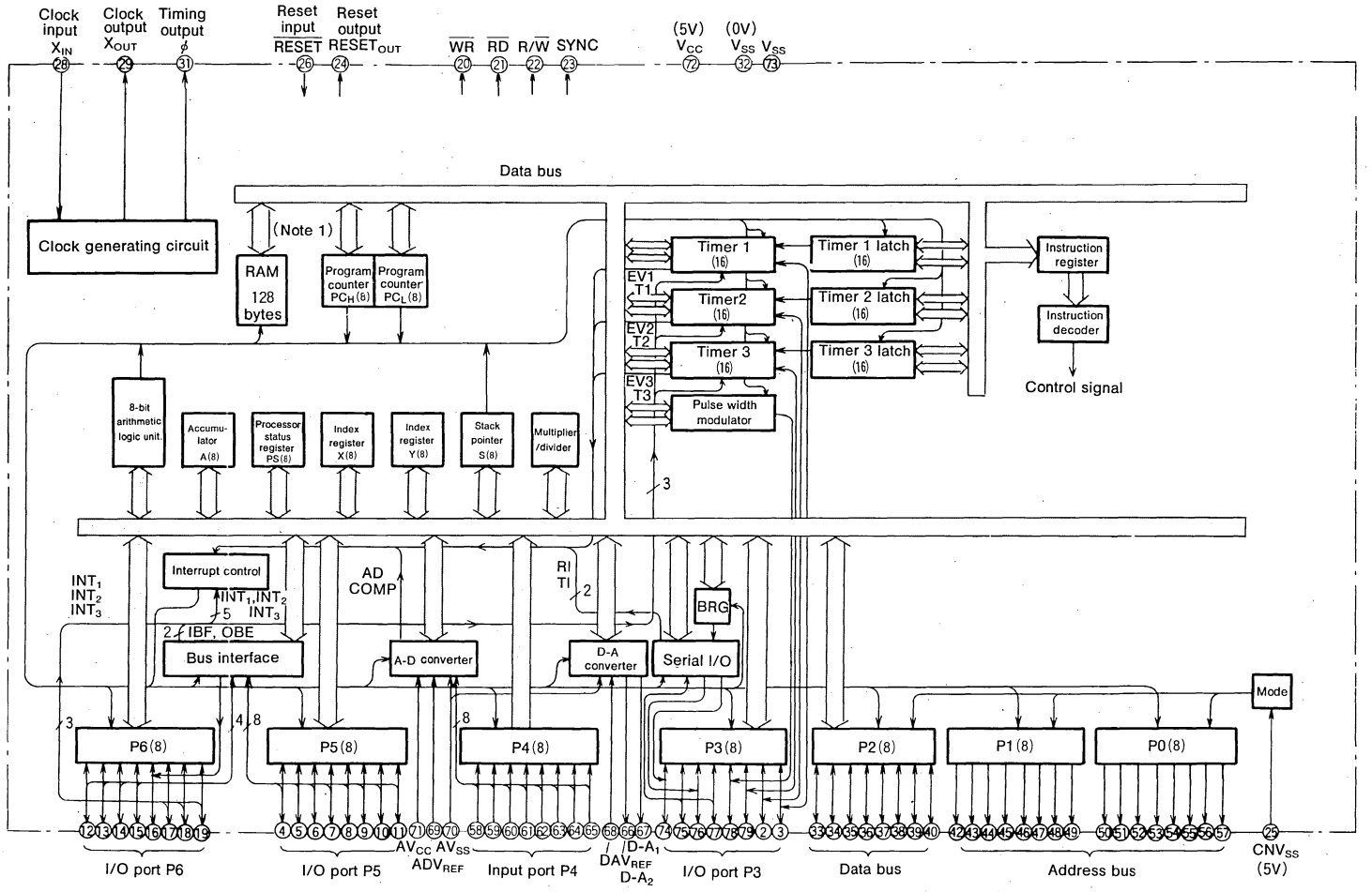


Outline 80P6

NC : No connection

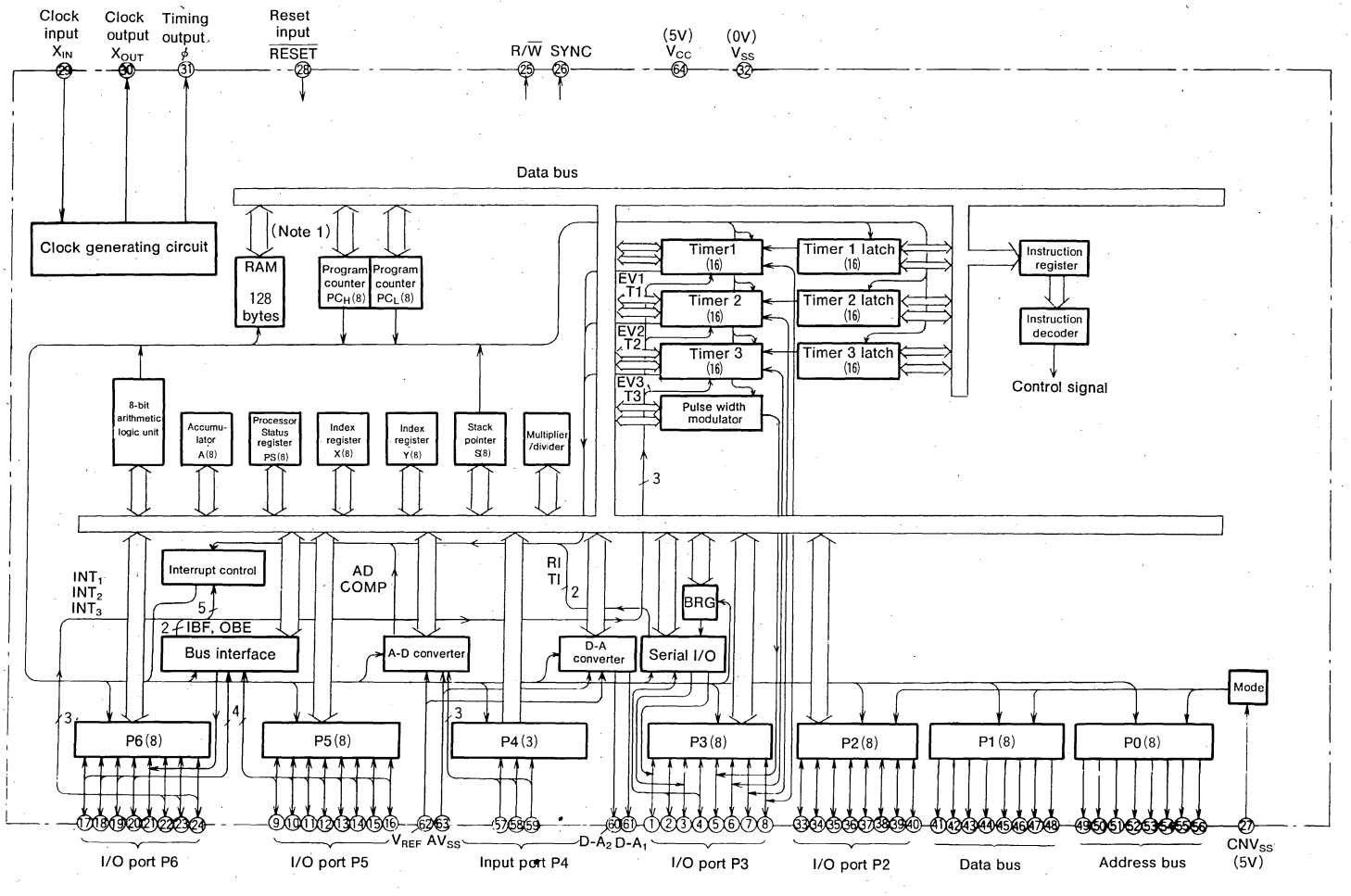
MITSUBISHI ELECTRIC

M37450S1FP BLOCK DIAGRAM



Note 1 : 256 bytes for M37450S2FP and 448 bytes for M37450S4FP.

M37450S1SP BLOCK DIAGRAM



Note 1 : 256 bytes for M37450S2SP and 448 bytes for M37450S4SP.

MITSUBISHI ELECTRIC

FUNCTIONS OF M37450S1SP/FP, M37450S2SP/FP, M37450S4SP/FP

Parameter			Function
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0.8μs(minimum instructions, at 10MHz of frequency)
Clock frequency			10MHz(max.)
RAM size	M37450S1SP/FP		128 bytes
	M37450S2SP/FP		256 bytes
	M37450S4SP/FP		448 bytes
Input/Output port	P3, P5, P6	I/O	8-bit×3
	P4	Input	3-bit×1(8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer(serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels(8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			64-levels(max. for M37450S1SP/FP)
			96-levels(max. for M37450S2SP/FP, M37450S4SP/FP)
Interrupts			6 external interrupts, 8 internal interrupts one software interrupt
Clock generating circuit			Built-in(ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			30mW(at 10MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA(max.)
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package	M37450S1SP, M37450S2SP, M37450S4SP		64-pin shrink plastic molded DIP
	M37450S1FP, M37450S2FP, M37450S4FP		80-pin plastic molded QFP

PIN DESCRIPTION

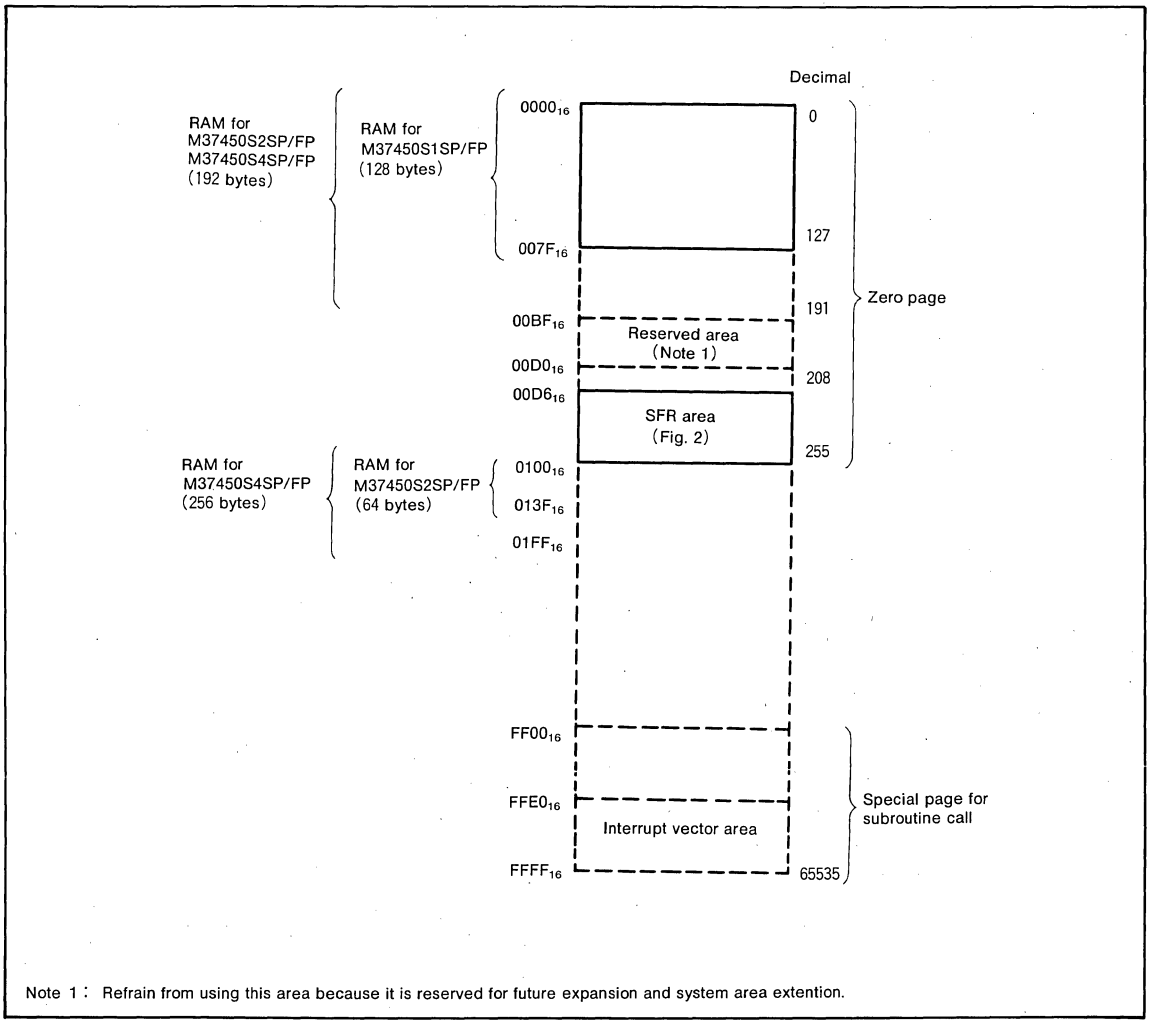
Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}	Input	This is connected to V_{CC}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four.
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs.
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus. It is "H" during read and "L" during write
A_0~A_{15}	Address bus	Output	This is 16-bit address bus.
D_0~D_7	Data bus	I/O	This is 8-bit data bus.
$P3_0$~$P3_7$	Input/Output port P3	I/O	Port P3 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programed as input or output. The output structure is CMOS output. Serial I/O, PWM output, or even I/O function can be selected with a program.
$P4_0$~$P4_2$ ($P4_0$~$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter. The 64-pin model has three pins and the 80-pin model has eight pins. They may also be used as digital input pins.
$P5_0$~$P5_7$	Input/Output port P5	I/O	An 8-bit input/output port with the same function as P3. This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program.
$P6_0$~$P6_7$	Input/Output port P6	I/O	An 8-bit input/output port with the same function as P0. Pins $P6_3$~$P6_7$ change to a control bus for the master CPU when slave mode is selected with a program. Pins $P6_0$~$P6_2$ may be programmed as external interrupt input pins.
$D\text{-}A_1$, $D\text{-}A_2$	D-A output	Output	Analog signal from D-A converter is output.
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter. This pin is for 64-pin model only.
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter. This pin is for 80-pin model only.
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter. This pin is for 80-pin model only.
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter. Same voltage as V_{SS} is applied.
AV_{CC}	Analog power supply		Power supply input pin for A-D converter. This pin is for 80-pin model only. Same voltage as V_{CC} is applied. In the case of the 64-pin model AV_{CC} is connected to V_{CC} internally.
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus. This pin is for 80-pin model only.
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component. This pin is for 80-pin model only.
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset. It is used as a reset output signal for peripheral components. This pin is for 80-pin model only.

BASIC FUNCTION BLOCKS

The differences between M37450M2-XXXSP/FP and M37450S1SP/FP are noted below. Other functions are the same as M37450M2-XXXSP/FP in microprocessor mode.

MEMORY

A memory map for the M37450S1SP/FP is shown in Figure 1. Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $FFE0_{16}$ to $FFFF_{16}$ are vector addresses used for the reset and interrupts (This area must be located in ROM area).
Addresses 0000_{16}~$00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.
Addresses 0000_{16} to $007F_{16}$ are the RAM address area assigned to the M37450S1SP/FP and consist of 128 bytes.
Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $013F_{16}$ are the RAM address area assigned to the M37450S2SP/FP and consist of 192 bytes and 64 bytes respectively.
Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $01FF_{16}$ are the RAM address area assigned to the M37450S4SP/FP and consist of 192 bytes and 256 bytes respectively.
In addition to data storage, this RAM is used for the stack during subroutine calls and interrupts.



Note 1 : Refrain from using this area because it is reserved for future expansion and system area extention.

Fig. 1 Memory map

$00D6_{16}$	P3 register
$00D7_{16}$	P3 directional register
$00D8_{16}$	P4 register
$00D9_{16}$	Reserved
$00DA_{16}$	P5 register
$00DB_{16}$	P5 directional register
$00DC_{16}$	P6 register
$00DD_{16}$	P6 directional register
$00DE_{16}$	MISRG1
$00DF_{16}$	MISRG2
$00E0_{16}$	D-A1 register
$00E1_{16}$	D-A2 register
$00E2_{16}$	A-D register
$00E3_{16}$	A-D control register
$00E4_{16}$	Data bus buffer register
$00E5_{16}$	Data bus buffer status register
$00E6_{16}$	Receive/transmit buffer register
$00E7_{16}$	Serial I/O status register
$00E8_{16}$	Serial I/O control register
$00E9_{16}$	UART control register
$00EA_{16}$	Baud rate generator

$00EB_{16}$	PWM register (low-order)
$00EC_{16}$	PWM register (high-order)
$00ED_{16}$	Timer 1 control register
$00EE_{16}$	Timer 2 control register
$00EF_{16}$	Timer 3 control register
$00F0_{16}$	Timer 1 register (low-order)
$00F1_{16}$	Timer 1 register (high-order)
$00F2_{16}$	Timer 1 latch (low-order)
$00F3_{16}$	Timer 1 latch (high-order)
$00F4_{16}$	Timer 2 register (low-order)
$00F5_{16}$	Timer 2 register (high-order)
$00F6_{16}$	Timer 2 latch (low-order)
$00F7_{16}$	Timer 2 latch (high-order)
$00F8_{16}$	Timer 3 register (low-order)
$00F9_{16}$	Timer 3 register (high-order)
$00FA_{16}$	Timer 3 latch (low-order)
$00FB_{16}$	Timer 3 latch (high-order)
$00FC_{16}$	Interrupt request register 1
$00FD_{16}$	Interrupt request register 2
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Interrupt control register 2

Fig. 2 SFR (Special Function Register) memory map

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state.	−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3∼7	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3∼13	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, $RESET_{OUT}$, SYNC		−0.3∼V_{CC}+0.3	V
Pd	Power dissipation	T_a = 25℃	1000 (Note 1)	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : 500mW for QFP type.

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−10∼70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 2)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (except Note 2)	2.0		V_{CC}	V
V_{IL}	"L" Input voltage CNV_{SS} (Note 2)	0		0.2V_{CC}	V
V_{IL}	"L" Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (except Note 2)	0		0.8	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 3)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 3)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		10	MHz

Note 2 : Ports operate as INT_1∼INT_3($P6_0$∼$P6_2$), EV_1∼EV_3($P3_0$∼$P3_2$), R_XD($P3_4$) and S_{CLK}($P3_6$)

Note 3 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms.

Note 4 : The total of "L" output current $I_{OL(peak)}$ of port P0, P1 and P2 is less than 40mA.
The total of "H" output current $I_{OH(peak)}$ of port P0, P1 and P2 is less than 40mA.
The total of "L" output current $I_{OL(peak)}$ of port P3, P5, P6, R/$\overline{W}$ SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA.
The total of "H" output current $I_{OH(peak)}$ of port P3, P5, P6, R/$\overline{W}$ SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, f(X_{IN}) = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, RESET$_{OUT}$, ϕ	I_{OH}=−2mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OH}=−5mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, RESET$_{OUT}$, ϕ	I_{OL}=2mA			0.45	V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OL}=5mA			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1~INT_3($P6_0$~$P6_2$), EV_1~EV_3($P3_0$~$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation f(X_{IN})=10MHz		6	10	mA
		At stop mode (Note 5)		1	10	μA

Note 5 : The terminals $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, RESET$_{OUT}$, ϕ, D-A_1 and D-A_2 are all open. The other ports, which are in the input mode, are connected to V_{SS}. A-D converter is in the A-D completion state. The current through ADV_{REF} and DAV_{REF} is not included(Fig.6).

A-D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, f(X_{IN})=10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5.12V		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_C(\phi)$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}=5V	2	7.5	10	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}=5V	0.5	0.7	2.5	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Abusolute accuracy	V_{CC}=DAV_{REF}=5.12V			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current		0	2.5	5	mA

TIMING REQUIREMENTS

Port/Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig. 3	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_C(X_{IN})$	External clock input cycle time		100		1000	ns
$t_W(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_W(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig. 3	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A_0 setup time		40			ns
$t_{su(A-W)}$	A_0 setup time		40			ns
$t_{h(R-A)}$	A_0 hold time		10			ns
$t_{h(W-A)}$	A_0 hold time		10			ns
$t_{W(R)}$	Read pulse width		160			ns
$t_{W(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig. 4	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A_0 setup time		40			ns
$t_{h(E-A)}$	A_0 hold time		10			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		10			ns
$t_{W(EL)}$	Enable clock "L" pulse width		160			ns
$t_{W(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

Local bus/Memory expansion mode, Microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(D-\phi)}$	Data input setup time	Fig. 5	100			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-RD)}$	Data input setup time		100			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

SWITCHING CHARACTERISTICS

Port/Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 3			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{C(\phi)}$	Cycle time		400		4000	ns
$t_{W(\phi H)}$	ϕ clock pulse width ("H" level)		190			ns
$t_{W(\phi L)}$	ϕ clock pulse width ("L" level)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(R-D)}$	Data output enable time after read	Fig. 4			120	ns
$t_{v(R-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(R-PR)}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(E-D)}$	Data output enable time after read	Fig. 4			120	ns
$t_{v(E-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/Memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-A)}$	address delay time after ϕ	Fig. 5			120	ns
$t_{v(\phi-A)}$	address effective time after ϕ		10			ns
$t_{v(RD-A)}$	address effective time after $\overline{RD}$		10			ns
$t_{v(WR-A)}$	address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	data output delay time after ϕ				140	ns
$t_{d(WR-D)}$	data output delay time after $\overline{WR}$				140	ns
$t_{v(\phi-D)}$	data output effective time after ϕ		20			ns
$t_{v(WR-D)}$	data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				120	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				120	ns
$t_{W(RD)}$	$\overline{RD}$ pulse width		170			ns
$t_{W(WR)}$	$\overline{WR}$ pulse width		170			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V
V_{IL} 0.45V
Output test level : V_{OH} 2.0V
V_{OL} 0.8V

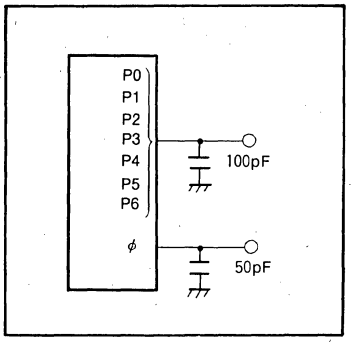


Fig. 3 Test circuit in single-chip mode

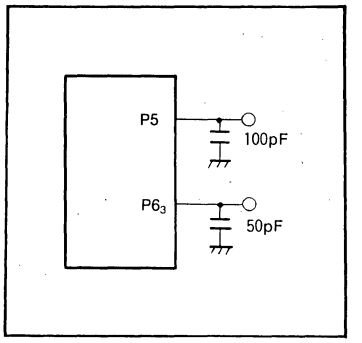


Fig. 4 Master CPU bus interface test circuit

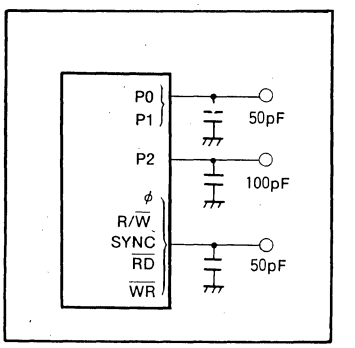


Fig. 5 Local bus test circuit

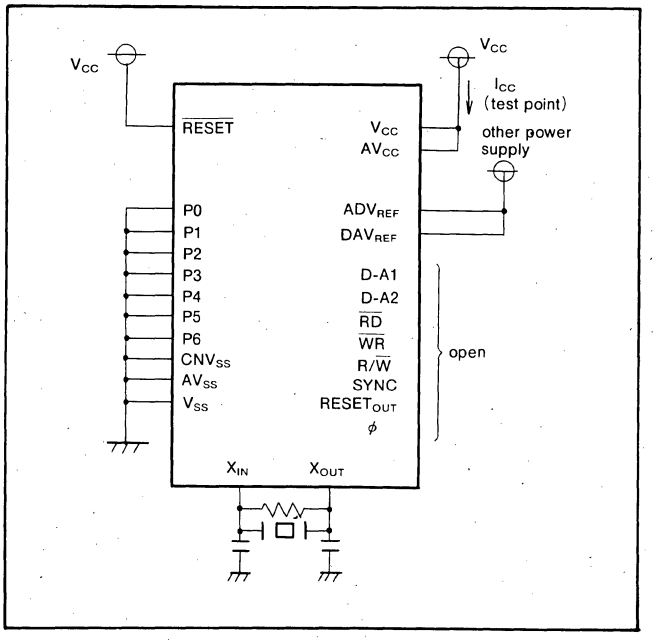
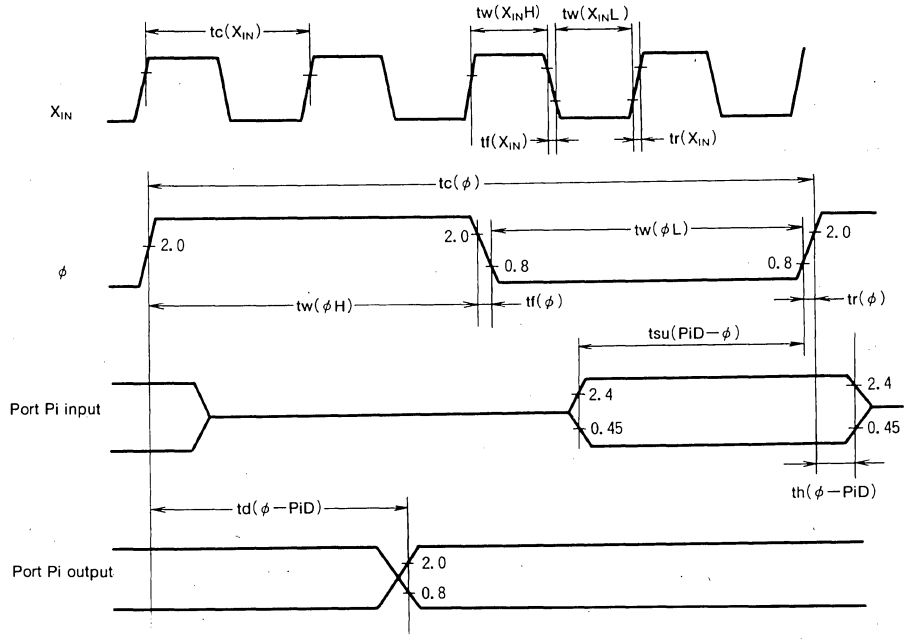


Fig. 6 I_{CC} (at stop mode) test condition

TIMING DIAGRAM

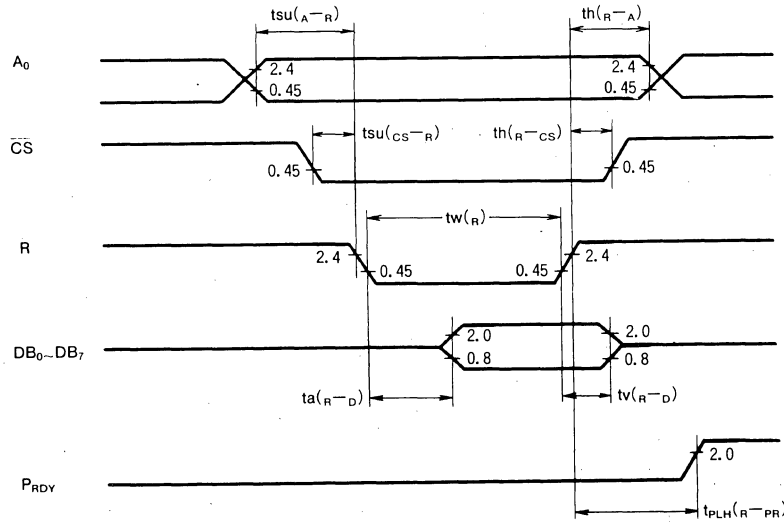
Port/single-chip mode timing diagram



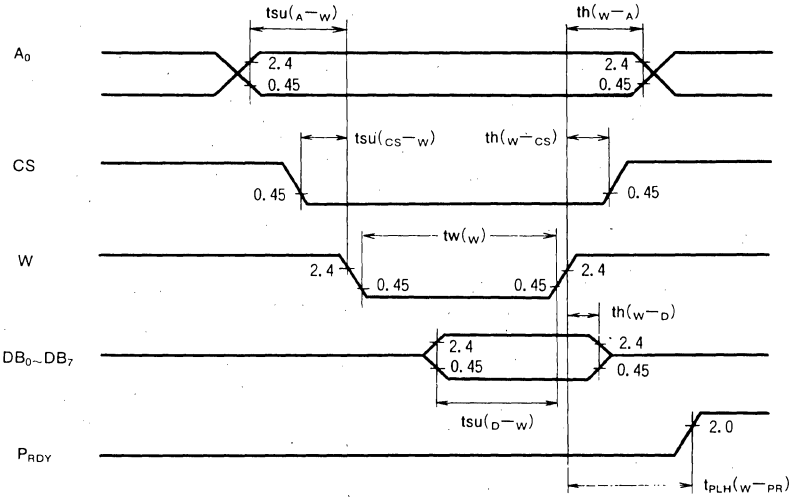
Note : V_{IH}=0.8V_{CC}, V_{IL}=0.16V_{CC} of X_{IN}

Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

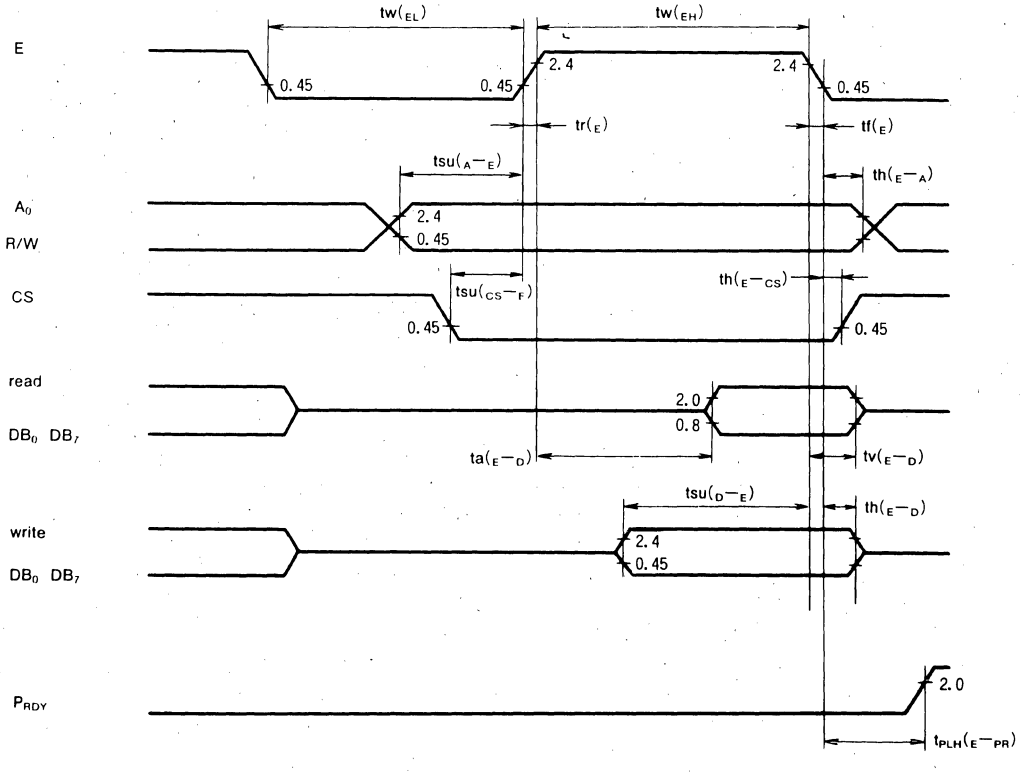
Read



Write

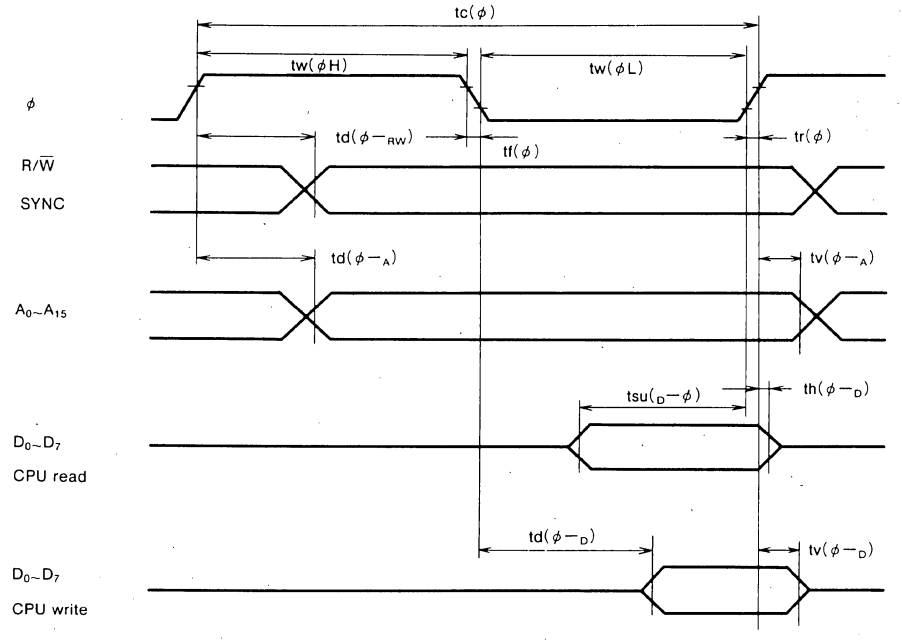


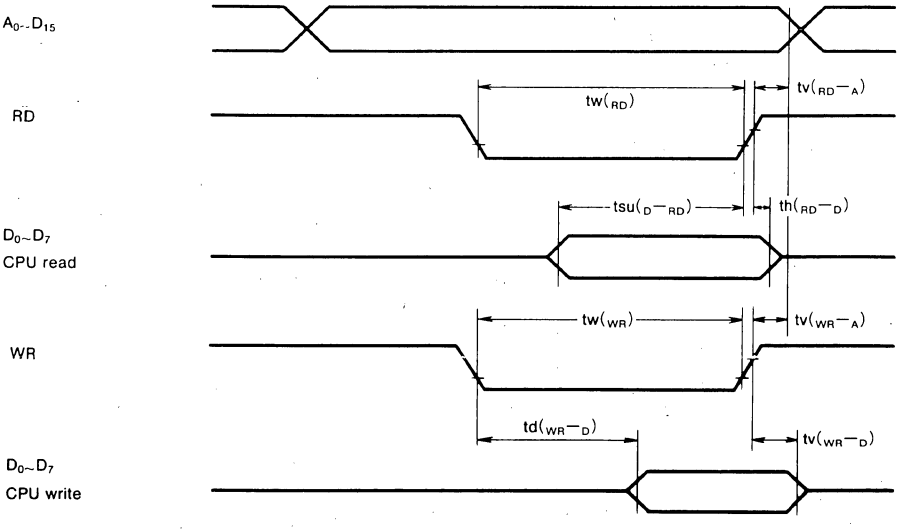
Master CPU interface/ R/W type timing diagram



MITSUBISHI ELECTRIC

Local bus timing diagram





M50734SP/FP

8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50734SP is a microcomputer designed with CMOS sillicon gate technology. It is housed in a 64-pin shrink plastic molded DIP (flat package type also available). This microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50734SP and the M50734FP are the package outline, the voltage input pins for A-D, and power dissipation ability (absolute maximum ratings).

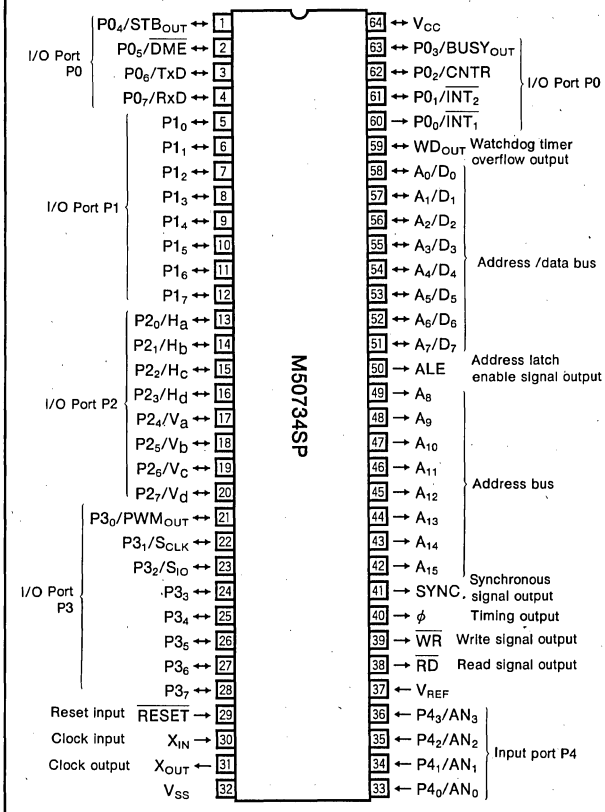
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size (internal memories are not provided)
  - Memory area programmable memory .....64K bytes
  - data memory .....64K bytes
- Instruction execution time
  - .....1μs (minimum instructions, at 8MHz frequency)
- Single power supply .....5V±10%
- Power dissipation
  - normal operation mode (at 8MHz frequency) 30mW
- Subroutine nesting ..... 128 levels (Max.)
- Interrupt .....11 types, 5 vectors
- Timers
  - 16-bit timer/event counter (general purpose) 1
  - 8-bit timer (general purpose) 3
  - 8-bit timer (watchdog timer) 1
  - 8-bit timer (strobe timer) 1
  - 8-bit timer (baud rate timer) 1
  - 8-bit counter (control for stepper motor) 2
- Stepper motor control circuit
  - ..... 1channel for the X or Y direction
- Programmable I/O ports (Ports P0, P1, P2, P3) 32
- Input ports (Port P4) 4
- Serial I/O
  - 8-bit clock synchronous 1
  - 8-bit UART 1
  - Baud rate (at 7.37MHz frequency) ...75bps~57600bps
- A-D converter ..... 8-bit successive approximation
- PWM function 1
- Multiplex-type bus
  - Address bus 16
  - Data bus (multiplexed with lower address bus) 8

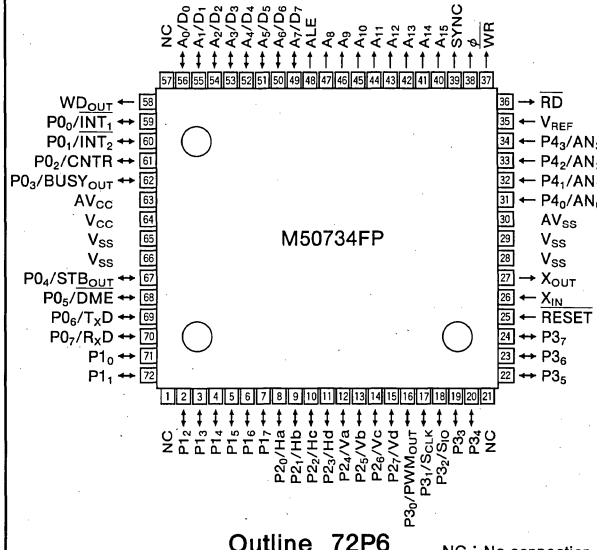
APPLICATION

Printer/plotter, Electronic typewriter, PPC, FAX, Portable word processor, Robotics

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

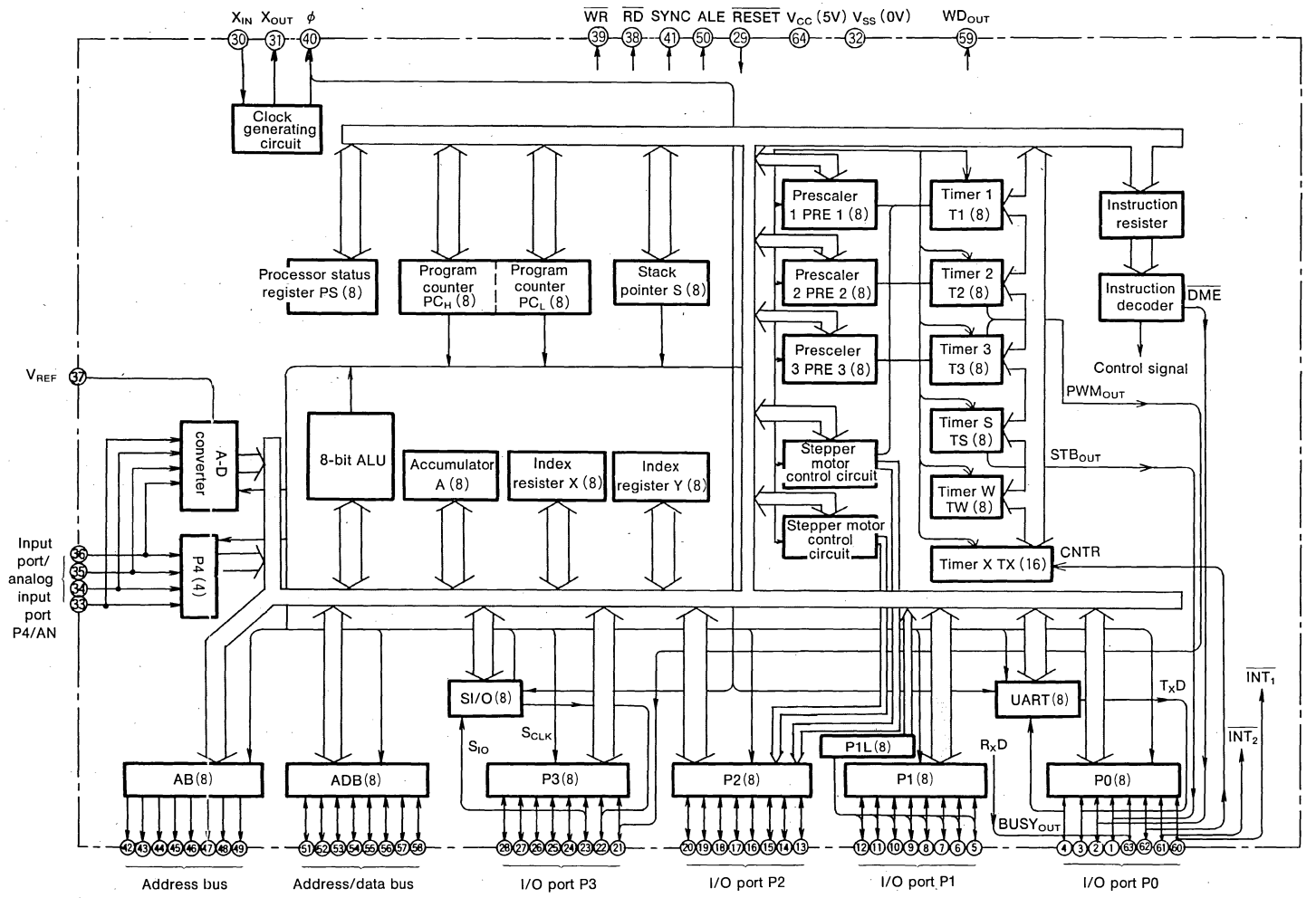


Outline 72P6

NC : No connection

MITSUBISHI ELECTRIC

M50734SP BLOCK DIAGRAM



FUNCTIONS OF M50734SP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 8MHz frequency)
Clock frequency			8MHz
Memory size			64K bytes (up to 128k bytes with DME signal)
Input/output port	P0, P1, P2, P3	I/O	8-bit×4 (all pins of P0, P2, and part of P3 have double functions)
	P4	input	4-bit×1 (P4 is in common with analog input)
UART			1 (built-in baud rate generator, 75~57600bps)
Clock synchronized serial I/O			8-bit×1
Timer	Timer X		16-bit×1
	Timer 1		8-bit×1 (with 8-bit prescaler)
	Timer 2		8-bit×1 (with 8-bit prescaler)
	Timer 3		8-bit×1 (with 8-bit prescaler)
	Timer S		8-bit×1 (with 1/4 frequency divider)
	Timer W		8-bit×1 (with 1/1024 frequency divider)
A-D converter			Four analog inputs, 8-bit successive approximation
Subroutine nesting			128 levels (max.)
Interrupts			Three external interrupts, four timer interrupts Two counter interrupts, one UART interrupt
Clock generating circuit			Built-in (externally connected to a ceramic resonater or a quartz crystal resonator)
Supply voltage			5V±10%
Power dissipation	at normal operation (at 8MHz frequency)		30mW
	at wait mode		5mW
	at stop mode		5μW
Operating temperature range			−10~70℃
Device structure			CMOS sillicon gate process
Package	M50734SP		64-pin shrink plastic molded DIP
	M50734FP		72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and V_{SS}
AV_{CC} AV_{SS}	Voltage input for A-D		This is the power supply input pin for the A-D converter. For M50734SP, this is not provided.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin. Clock oscillating frequency f(X_{IN}) divided by 4 signal is outputed.
SYNC	Synchronous signal output	Output	Synchronous signal is outputed when the op code is fetched, and is used to control the program's single-step operation.
$\overline{RD}$	Read signal output	Output	Control signal for read access to ROM, RAM and peripherals.
$\overline{WR}$	Write signal output	Output	Control signal for write access to RAM and peripherals.
ALE	Address latch enable signal output	Output	Address latch signal for address A_0~A_7.
A_{15}~A_8	Address bus	Output	The contents of the high-order 8 bits of the address bus are output (CMOS output).
A_7/D_7~ A_0/A_0	Address/Data bus	I/O	The contents of the lower-order 8 bits of the address bus and 8 bits of the address bus are output (CMOS output).
WD_{OUT}	Watchdog timer overflow output	Output	When the watchdog timer overflows, this pin is set to "H". Cleared only at reset.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with CMOS tri-state output. Each port has double function, and can switch by software.
$\overline{INT_1}$($P0_0$)	Interrupt input	Input	This is an interrupt input pin.
$\overline{INT_2}$($P0_1$)	Interrupt input	Input	This is an interrupt input pin.
CNTR($P0_2$)	Timer I/O	I/O	This is an output pin for the timer X.
$BUSY_{OUT}$($P0_3$)	Busy signal output	Output	When the falling edge is inputed to $\overline{INT_1}$ pin, this port is set by hardware.
$\overline{STB_{OUT}}$($P0_4$)	Strove pulse output	Output	This pin is used for the strobe input to the external driver IC.
$\overline{DME}$($P0_5$)	Data memory enable output	Output	This pin is used for external memory expansion.
TxD($P0_6$)	Transmission output	Output	This is an output pin for UART.
RxD($P0_7$)	Receive input	Input	This is an input pin for UART.
$P1_0$ ~ $P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port with CMOS tri-state output. It is also used as "latch input" to read data when a low level signal is inputed to $\overline{INT_1}$ pin.
$P2_0$ ~ $P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port with CMOS tri-state output. By software selection, it can also be used as an output port for the decoder logic of a stepper motor control circuit.
$P3_0$ ~ $P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port with CMOS tri-state output. The function of the $P3_0$~$P3_2$ can be selected by software.
S_{IO}($P3_2$)	Serial I/O	I/O	This pin is used as an I/O pin for serial I/O.
$P4_0/AN_0$~ $P4_3/AN_3$	Input port P4/ Analog input port AN	Input	Port P4 is a 4-bit input port, and is used as a 4-bit analog input port for A-D converter.

BASIC FUNCTION BLOCKS

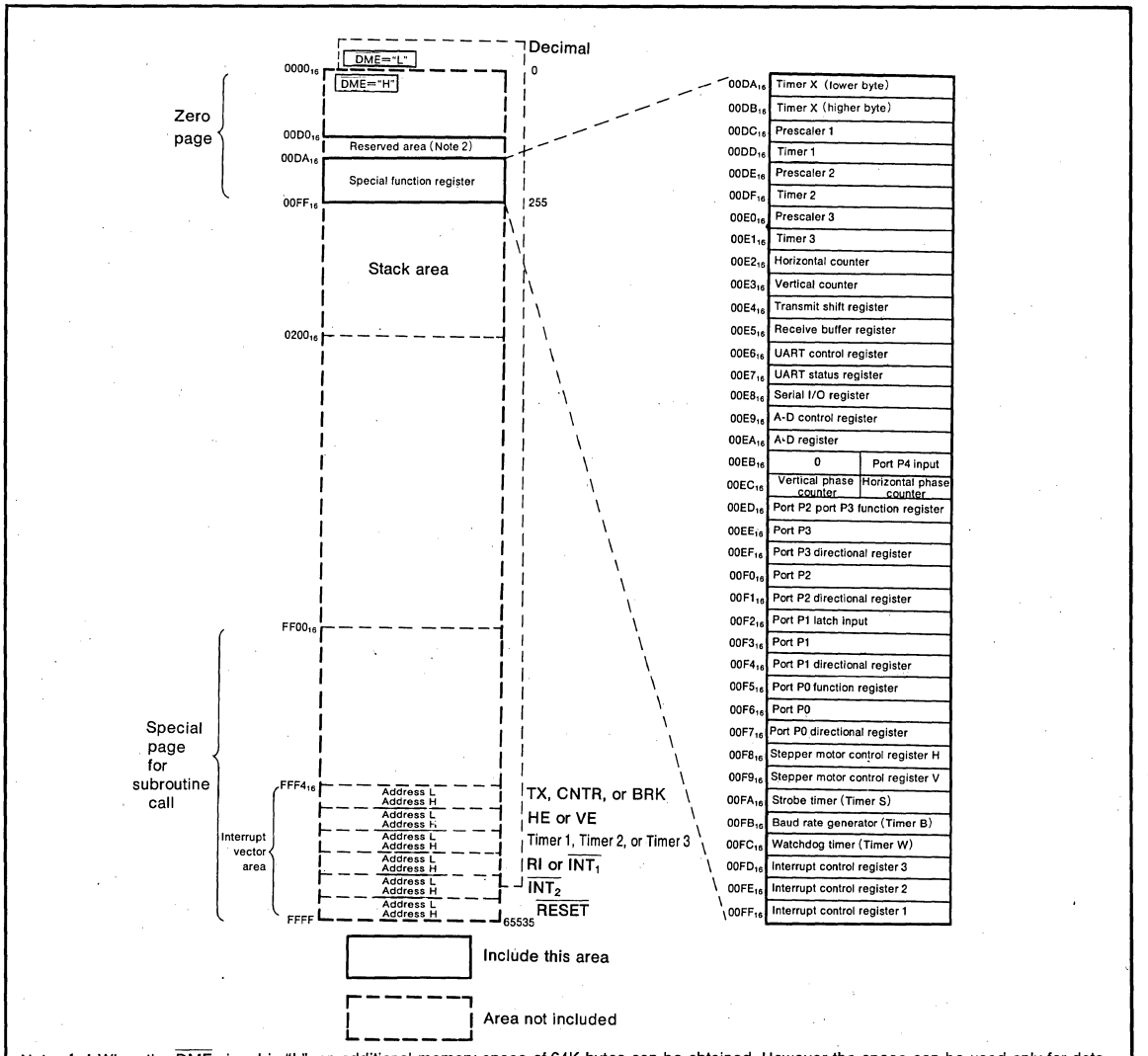
MEMORY

A memory map of the M50734SP is shown in Figure 1. Since the M50734SP contains no internal memory, the ROM and RAM must be connected externally. The addressable memory space is 64K bytes however, by using the $\overline{DME}$ signal, up to 128K bytes can be accessed.

The special address area is contained between addresses $FF00_{16}$ to $FFFF_{16}$. By using this special page addressing mode, subroutines located in this area can be called with only 2 bytes. The reset and interrupt vector addresses are contained within addresses $FFF4_{16}$ to $FFFF_{16}$.

The zero page address area is contained between 0000_{16} and $00FF_{16}$. Addresses within this area can be accessed with 1 byte. Frequently accessed addresses, such as in RAM, input/output ports and timers, are allocated to the zero page area.

Addresses 0100_{16} to $01FF_{16}$ are used mainly as the stack, and addresses 0200_{16} to $FEFF_{16}$ are used memories for the program and data.



Note 1 : When the $\overline{DME}$ signal is "L", an additional memory space of 64K bytes can be obtained. However the space can be used only for data memory such as ROM, RAM or peripherals.

2 : This area is reserved for system expansion.

Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

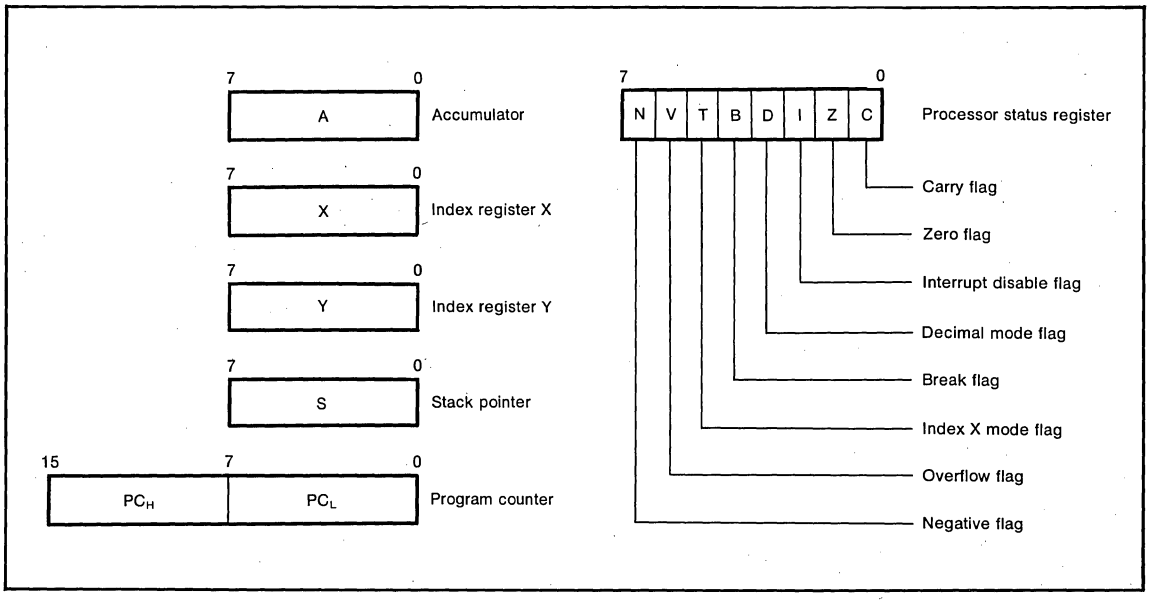


Fig.2 Register structure

STACK POINTER (S)

The stack pointer is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

When an interrupt occurs, the higher 8 bits of the program counter is pushed onto the stack first, the stack pointer is decremented by one, and then the lower 8 bits of the program counter is pushed onto the stack. Next the contents of the processor status register is pushed onto the stack. As each byte is pushed onto the stack. When the return from interrupt instruction (RTI) is executed, the program counter and processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed onto the stack automatically, so a Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in the reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed and pulled to and from the stack with the PHP and PLP instructions, respectively.

During a subroutine call, only the program counter is pushed onto the stack. Therefore, any registers that should not be destroyed should be pushed onto the stack manually. To return from a subroutine call, the RTS instruction is used.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (ie., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

INTERRUPTS

The M50734SP can be interrupted from 11 sources. The interrupts are vector interrupts, and their priorities and vector table is shown in Table 1. When the interrupt enable bit is set to "1", the interrupt request bit is set to "1" and the interrupt disable flag to "0", all interrupts except the reset and BRK instructions are acknowledged. The reset is treated as a nonmaskable interrupt of the highest priority.
This is shown in Figure 3.

Table 1. Interrupt vector address and priority

Interrupt source	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{\text{INT}_1}$	2	$FFFD_{16}$, $FFFC_{16}$
R1 or $\overline{\text{INT}_1}$	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1, timer 2 or timer 3	4	$FFF9_{16}$, $FFF8_{16}$
HE or VE	5	$FFF7_{16}$, $FFF6_{16}$
Timer X, CNTR or BRK	6	$FFF5_{16}$, $FFF4_{16}$

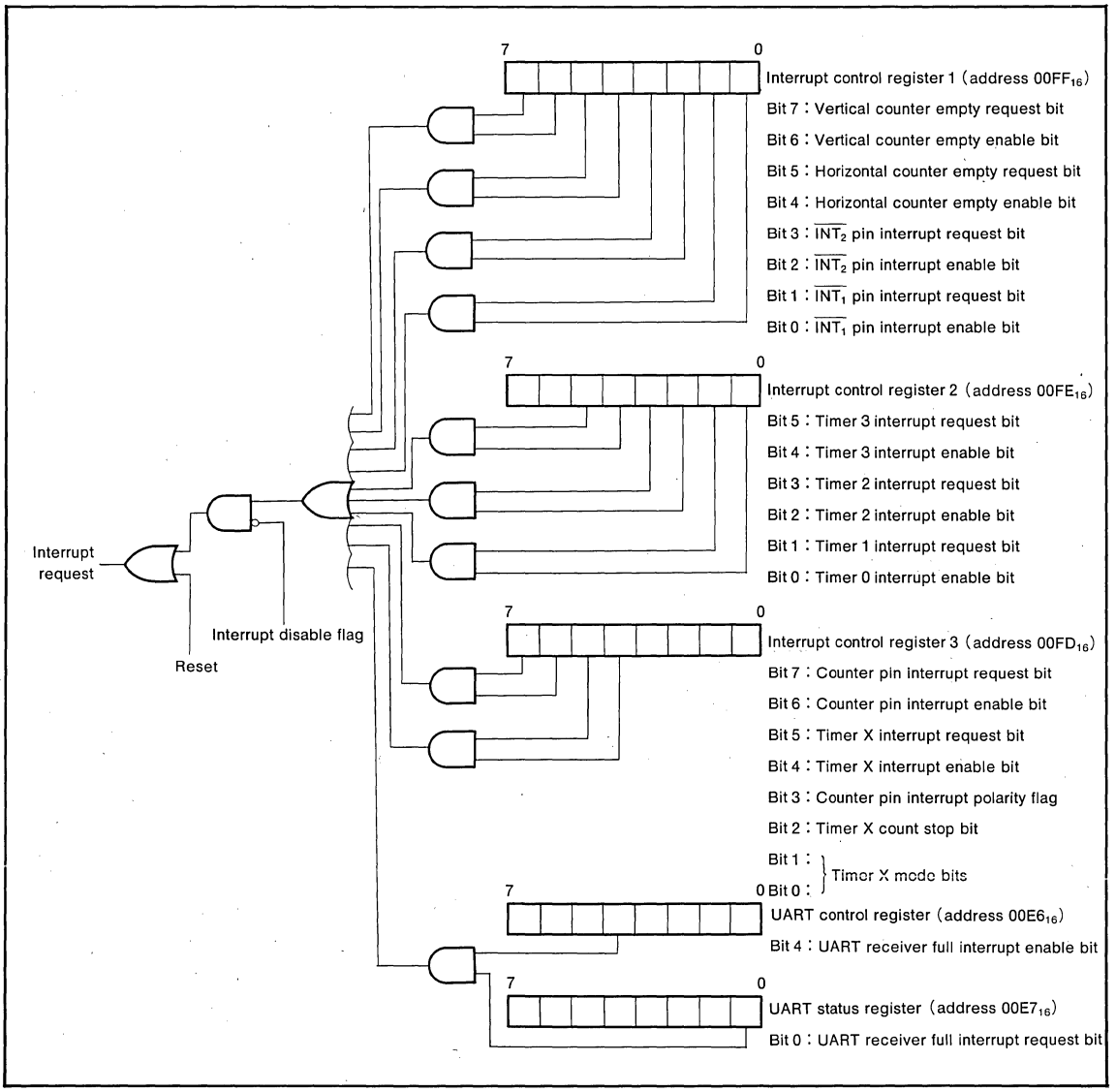


Fig.3 Interrupt control

TIMER (VCU)

The M50734SP provides a versatile control unit consisting of the timers and counters shown in Figure 4.
Each of the timers is described blow.

1. Timer X

The 16-bit timer X consists of timers X_H, X_L and their reload latches. This timer has four modes which are selected by bit 0 and bit 1 (timer X operation mode bits) of the interrupt control register 3 (address $00FD_{16}$). Figure 5 shows the structure of timer X and Figure 6 shows the structure of the interrupt control register 3.
Timer X can select the count source, either the oscillation frequency divided by 16 or the event clock which is input from the CNTR pin.
The timers are of the countdown type and the frequency ratio is 1/(n+1)(n:0~65535, decimal).

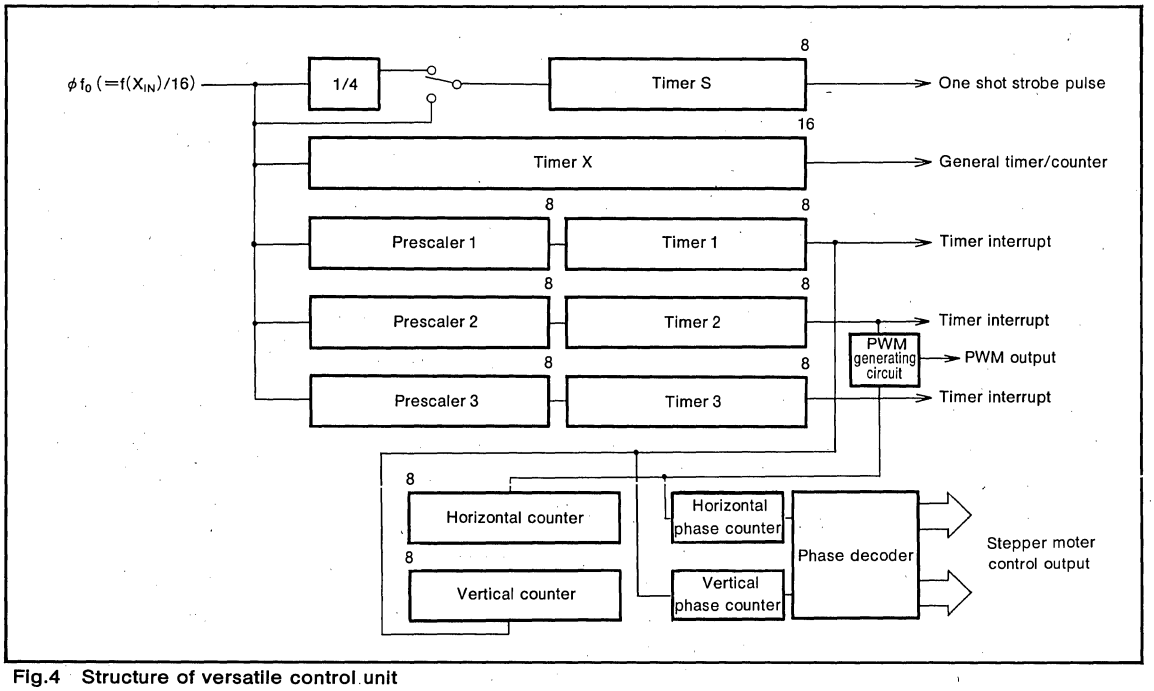


Fig.4 Structure of versatile control unit

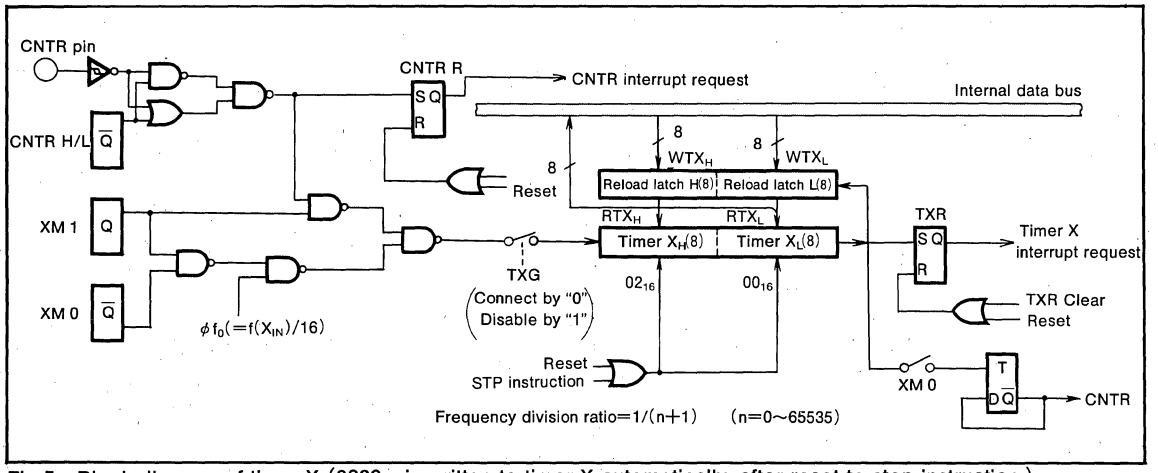


Fig.5 Block diagram of timer X (0200_{16} is written to timer X automatically, after reset to stop instruction.)

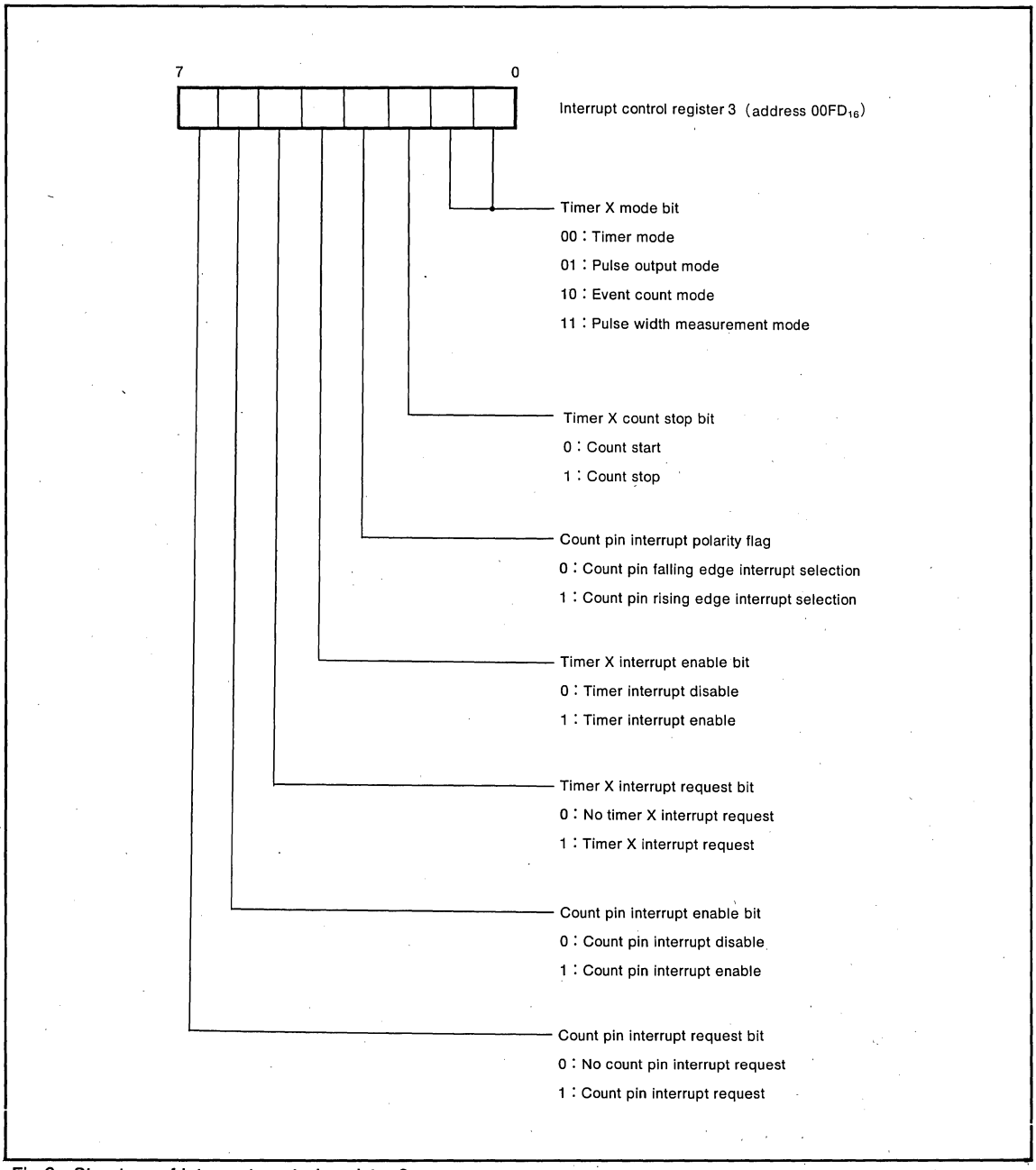


Fig.6 Structure of interrupt control register 3

The four modes of timer X are described below.

(1) Timer mode [00]

In this mode the oscillation frequency, divided by 16, is counted. When the contents of the timer reaches "0", the interrupt request bit is set to "1". At the next cycle, the contents of the timer latch are reloaded and the count continues. After resetting, this mode is set automatically.

(2) Pulse output mode [01]
Every time the contents of the timer reach "0", the output signal from the $P0_2$/CNTR pin changes polarity.
If this mode is used, bit 2 of port P0 function register and bit 2 of the port P0 directional register must be set to "1".

(3) Event counter mode [10]
The operation is the same as in the timer mode except that the input signal from pin $P0_2$/CNTR is counted. However, if this mode is used, bit 2 of port P0 directional register must be set to "0". The counter pin interrupt request bit is set by the event input signal. Therefore the counter pin interrupt enable bit must be set to "0" to prevent an interrupt.

(4) Pulse width measurement mode [11]
The oscillation frequency, divided by 16, is counted while the level of pin $P0_2$/CNTR is either low or high. The level of pin $P0_2$/CNTR is selected by interrupt control register 3, bit 3.

When the contents of the timer X reach "0", the interrupt request bit is set to "1". At the next cycle, the latches contents are reloaded and counting continues.
If this mode is used, the counter pin interrupt must be enabled and the timer X interrupt prohibited.

2. Timer 1, Timer 2, Timer 3

Timer 1, timer 2 and timer 3 each consist of an 8-bit prescaler, an 8-bit timer, a prescaler reload latch and a timer reload latch. The structure of timer 1, timer 2 and timer 3 is shown in Figure 7.

The count source for timer 1, timer 2 and timer 3 is the oscillation frequency divided by 16. These timers are of the countdown type and the frequency, ratio of the prescaler and timer is $1/(n+1)$ (n:0~255, decimal).

Timer 1 and timer 3 are also used to determine the step rate by connecting with the stepping motor control circuit and as timers for the PWM pulse output signal.

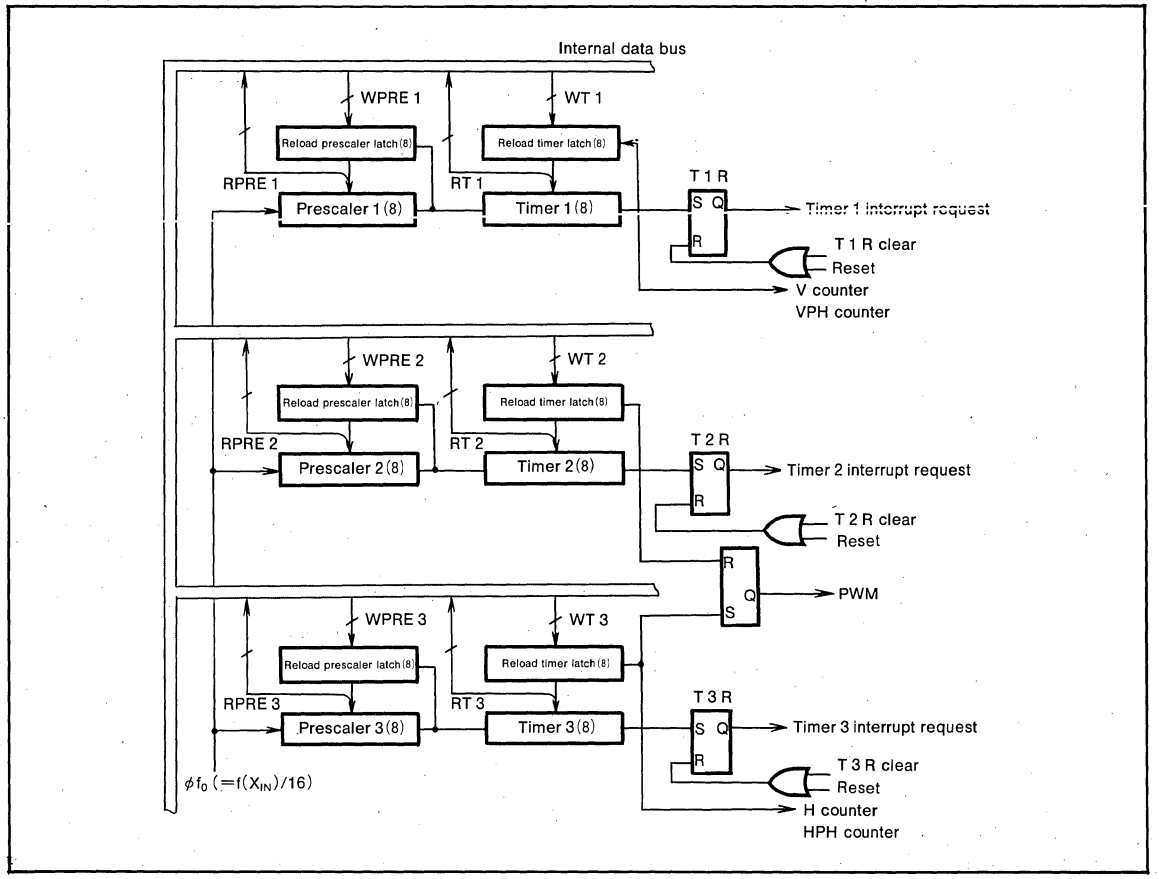


Fig.7 Block diagram of timer 1, timer 2 and timer 3

3. Timer S

The structure of timer S is shown in Figure 8. Timer S has no reload latch. Whether or not a 1/4 frequency divider should be put before the timer, is determined by bit 2 of the port P2 and port P3 function register (P2P3FR).

If the 1/4 frequency divider is bypassed, the clock produced by dividing the oscillation frequency by 16 becomes the count source for timers S. If it is built in, the oscillation frequency, divided by 16, (then divided by 4 once more), becomes the clock. This timer is of the countdown type and the frequency ratio is 1/(s+1)(s:0~255, decimal).

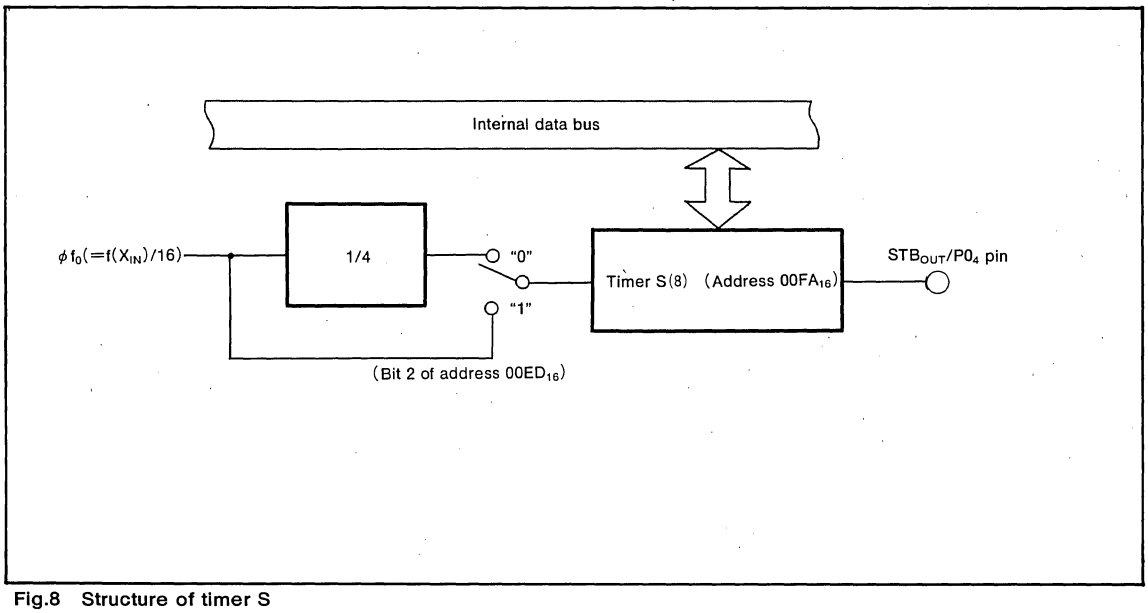


Fig.8 Structure of timer S

WATCHDOG TIMER

As shown in Figure 9, the watchdog timer is composed of a 10-bit prescaler and 8-bit timer counter. Timer W can be read from or written to by software. After a reset, this timer is set to FF_{16}. Every timer the prescaler overflows, timer W is decremented. When the contents of timer W (N_W) changes "00", the WD_{OUT} pin changes from "L" to "H".

If the oscillation frequency is 8MHz, the time (T_W) until the timer W underflows can be set by the following equation:

$T_W=16/f(X_{IN})\times1024\times(N_W\pm1/2)$ $(1\leqq N_W\leqq255$, decimal)

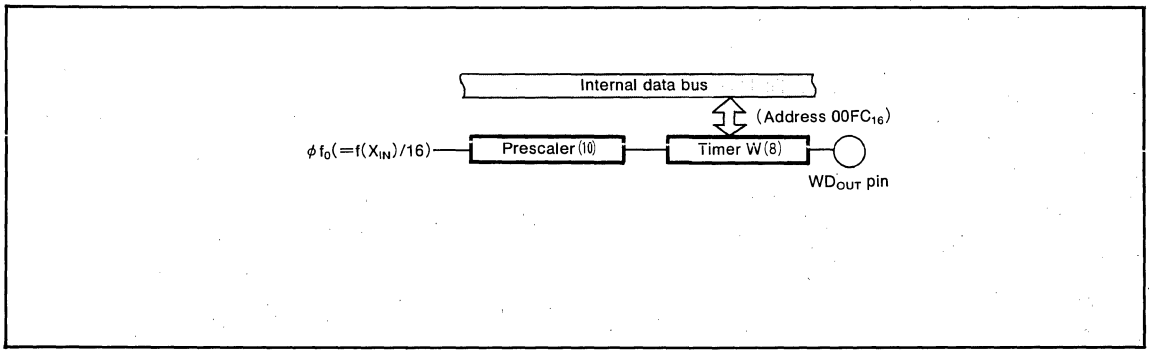


Fig.9 Structure of the watchdog timer

STEPPER MOTOR CONTROL CIRCUIT

Two identical circuits for the control of two stepper motors (for a horizontal and vertical direction) are built in to the M50734SP and can operate independently. The block diagram is shown in Figure 10.

The horizontal and vertical counters are both 8-bit binary counters which contain the number of steps. The horizontal phase counter (HPHC) and vertical phase counter (VPHC) are both 3-bit binary counters and perform phase decoding. The two stepping motor control registers are 4-bit registers controlling, start/stop, single-step, direction and 2-2 or 2-1 phase drive. The functions of these registers and the relation between the phase counter and the phase output signals are shown in Figure 11.

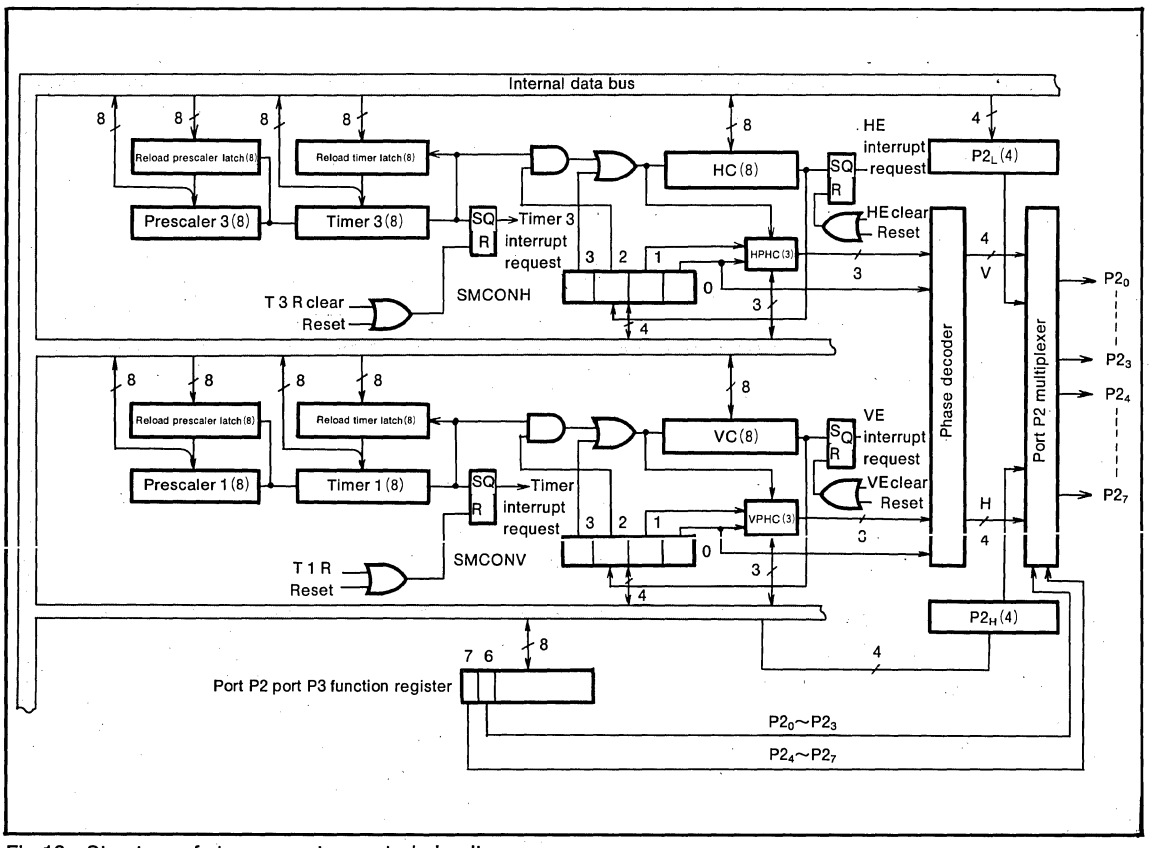


Fig.10 Structure of stepper motor control circuit
(Two identical circuits for horizontal and vertical direction.)

MITSUBISHI ELECTRIC

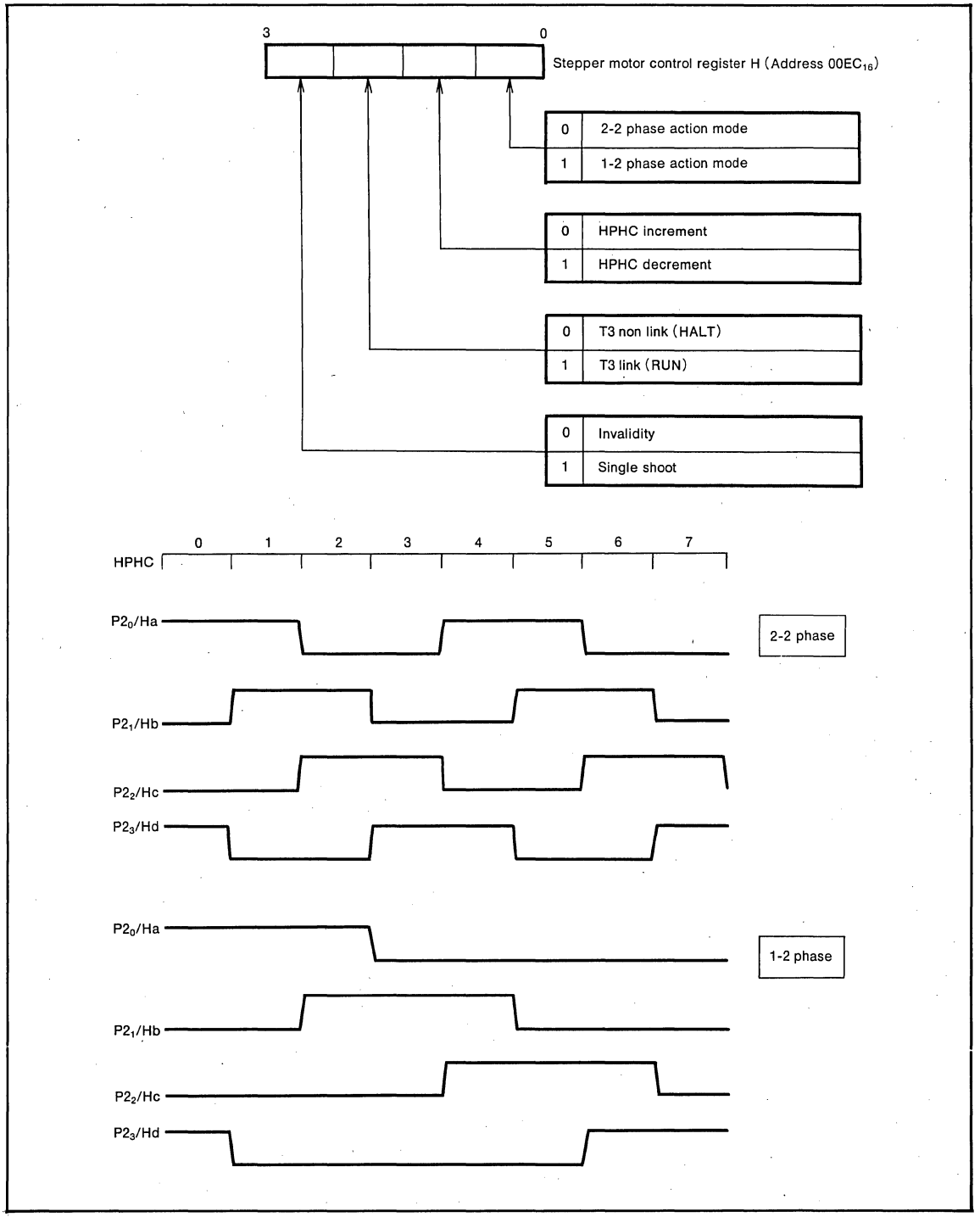


Fig.11 Bit functions of the stepper motor control register and relation between horizontal phase counter and phase output signals

PWM (Pulse width modulation)

The M50734SP includes a control circuit which generates pulses of various duty cycles utilizing timer 2 and 3.
The PWM signal is internally generated as shown in Figure 12.
W3 is the time interval (time from reload to zero) of timer 3 and W2 the time interval of timer 2.

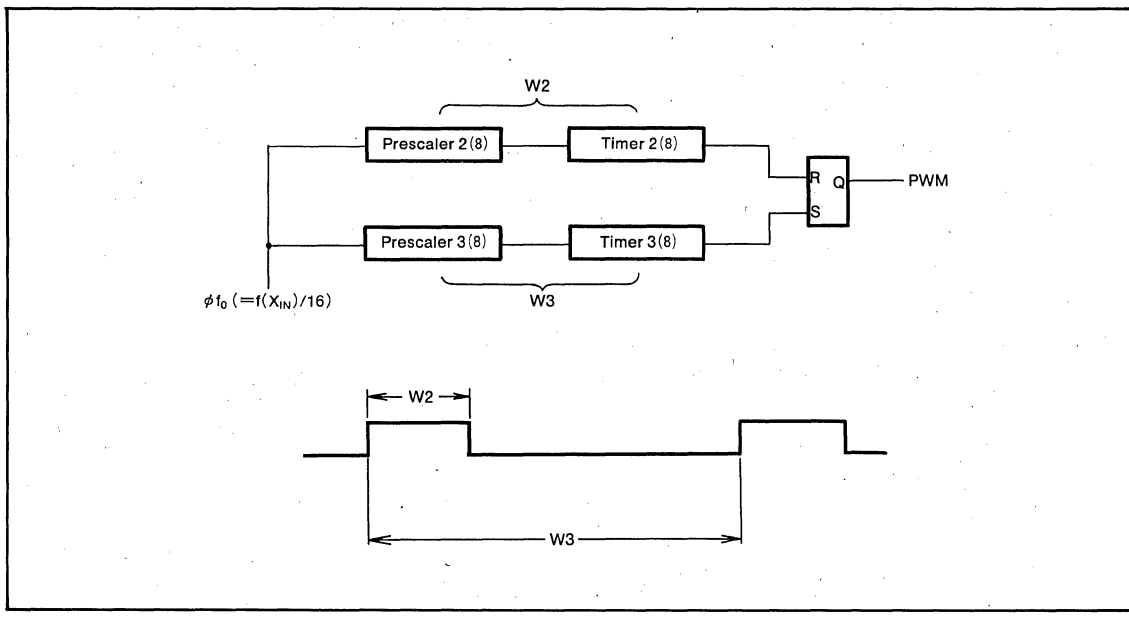


Fig.12 PWM signal generation

UART

The M50734SP has an 8-bit duplex UART. The block diagram is shown in Figure 13, and the bit structure of the UART control register and UART status register is shown in Figure 14. The UART control register can be read from or written to by software, but the UART status register can only be read.

Transmit/receive character length and parity addition are set by bit 0, 1 and 2 of the UART control register.

The four possible transmit/receive formats are as follows:

(1) 7-bit (no parity)
(2) 7-bit + parity (odd or even selectable)
(3) 8-bit (no parity).
(4) 8-bit + parity (odd and even selectable)

Each bit of the UART control register and UART status register is described in detail below.

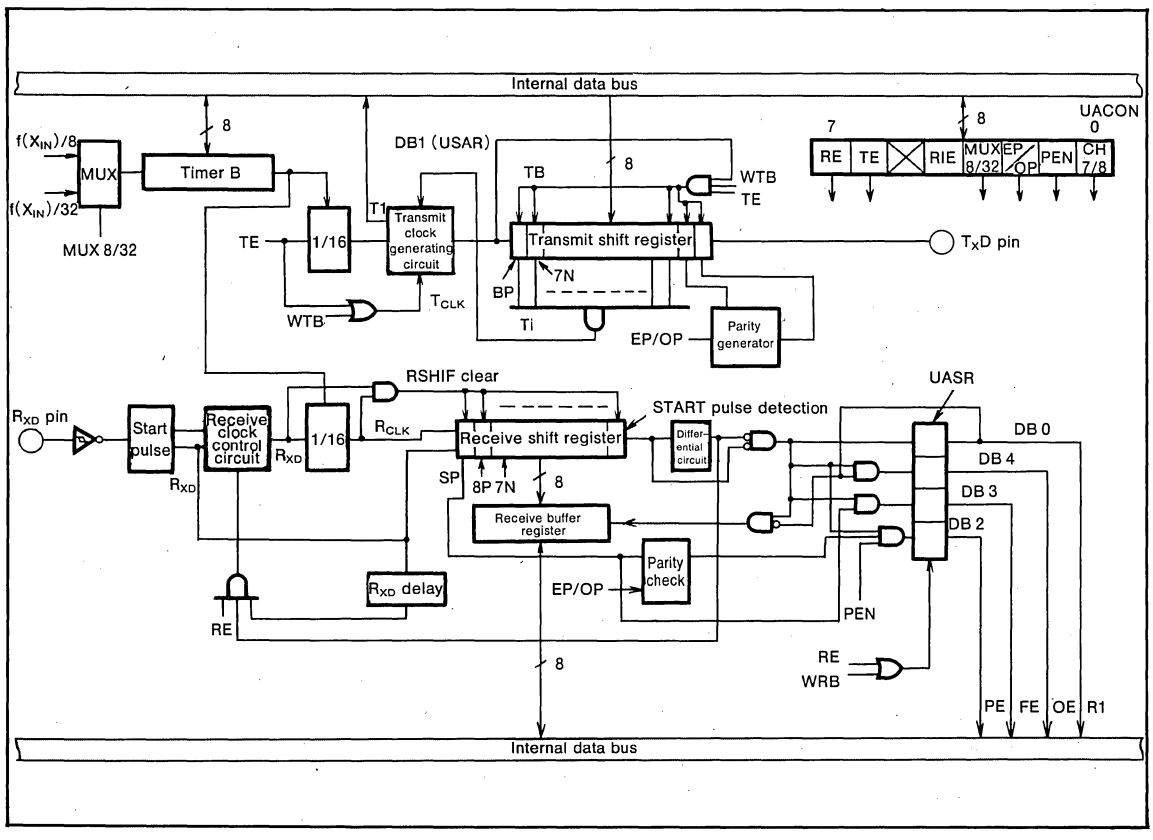


Fig.13 UART (timer B frequency ratio : 1/(B+1))

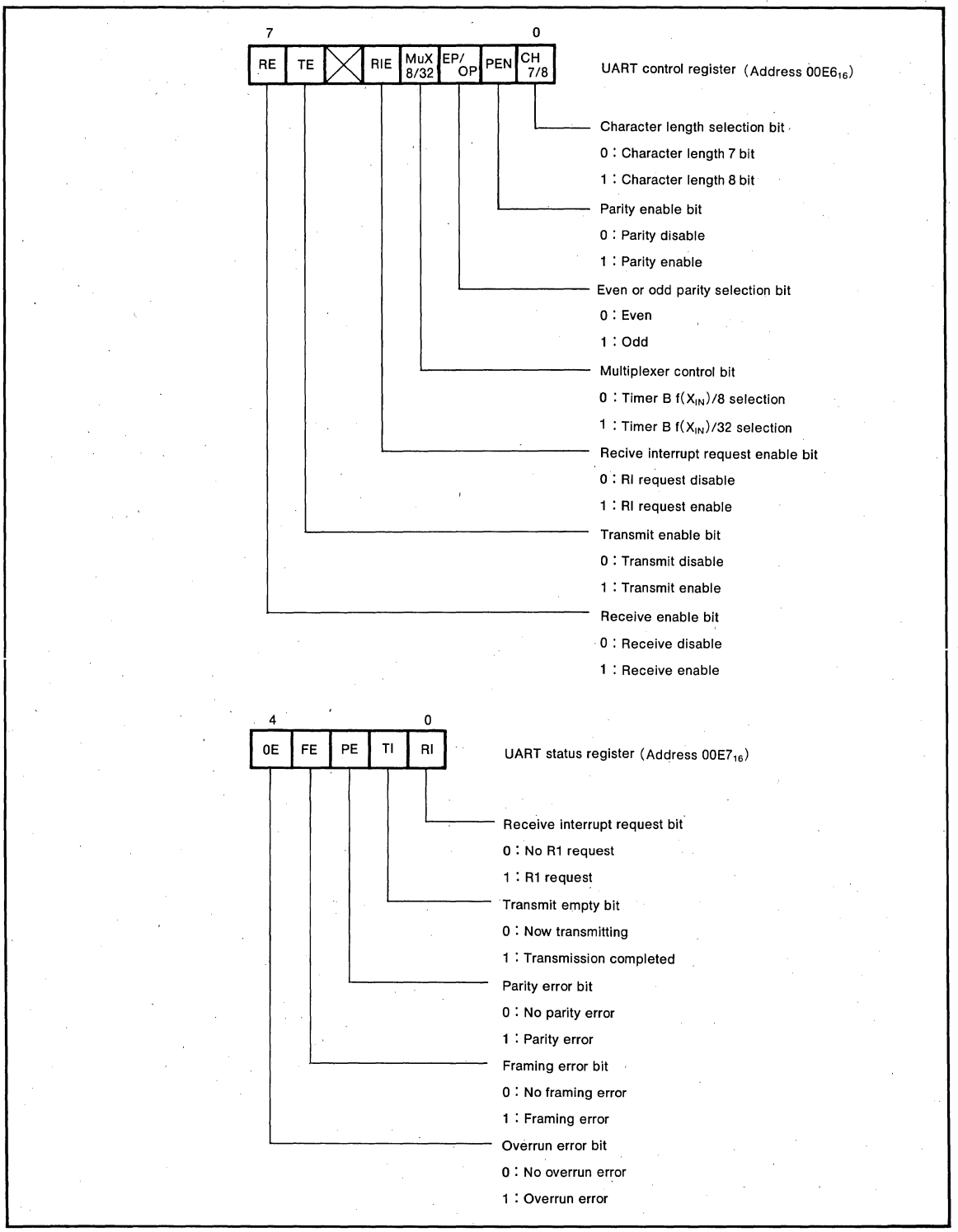


Fig.14 Bit structure of UART control register and UART status register

Character length selection bit (CH7/8)
If this bit is "0", the 7-bit character mode is selected;
If it is set to "1", the 8-bit character mode is selected.
It can be read from and written to by software.

Parity enable bit (PEN)
If this bit is "1", parity is added to the characters of the signal being transmitted or received. If this bit is to "0", parity is not added, and in the receive state a parity error can not occur.
If can be read from or written to by software.

Even or odd parity select bit (EP/OP)
If this bit is "0", even parity is selected, if set to "1", odd parity is selected. It can be read from or written to by software.

Multiplexer control bit (MuX 8/32)
This bit selects the count source of timer B. If it is "0", the oscillation frequency, divided by 8, is selected; if it is "1", the oscillation frequency divided by 32 is selected.
It can be read from or written to by software.

Receive interrupt request enable bit (RIE)
If this bit is "1", the receive interrupt request flag (RI) can be set; if it is cleared to "0", interrupts are inhibited. Even if the interrupts are inhibited, the RI flag remains as is.
It can be read from or written to by software.

Transmit enable bit (TE)
If this bit is "0", the transmit clock goes "H", the transmit interrupt bit is cleared "0" and goes to the initial state. When set to "1", transmission will start. It can be read from or written to by software.

Receive enable bit (RE)
If this bit is "0", the receive interrupt request bit (RI) parity error bit (PE), framing error bit (FE) and overrun error bit (OE) are cleared to the initial state. If it is "1", it will be in the receive enable state, and when the start bit is input into the $P0_7$/RxD pin, the receive operation will start.
This bit can be read from or written to by software.

Receive interrupt request bit (RI)
This bit is set to "1" when a receive interrupt request occurs. It is cleared to "0" when the receive enable bit (RE) is set to "0" or when data is written to the receive buffer register.

Transmit empty bit (TI)
This bit is cleared to "0" when the transmit enable bit (TE) is set to "0" or when data is written to the transmit shift register (TR). When the transmission is completed, it is set to "1".

Parity error bit (PE)
This bit is set to "1" when the parity odd or even selection bit is "0" and the number of is in the received data is even, or the parity odd or even selection bit is set to "1" and the number of "1"'s in the receive data is odd.
It is cleared to "0" when the receive enable bit (RE) is set to "0" or data is written to the receive buffer register.

Framing error bit (FE)
This bit is cleared to "0" when the receive enable bit (RE) is set to "0" or data is written to the receive buffer register. When a framing error occurs, this bit is set to "1". A framing error occurs when transmitting data from the receive shift register to the receive buffer register and the stop bit of the receive data does not exist.

Overrun error bit (OE)
This bit is cleared to "0" when the receive enable bit is set to "0" or data is written to the receive buffer register. When an overrun error occurs, this bit is set to "1".
An overrun error occurs when the next data is transmitted from the receive shift register to the receive buffer register while the receive interrupt request bit (RI) is "1".
The receive and transmit operations are shown in Figure 15 and Figure 16.

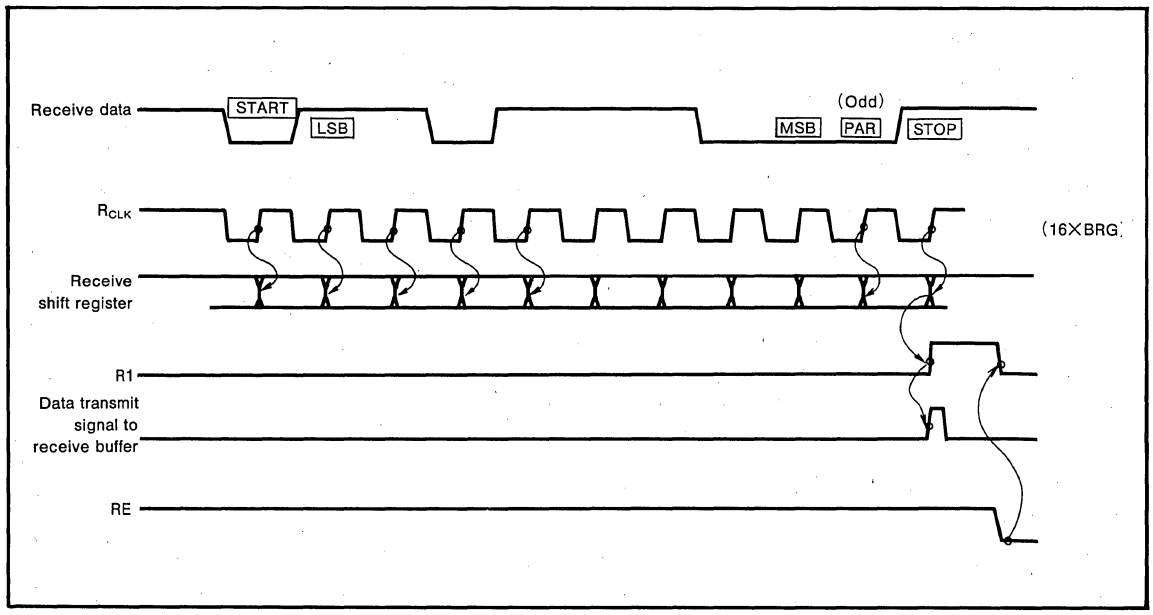


Fig.15 Receive operation (8-bit+1 parity mode)

(Each receive data bit is read by a master slave flip-flop when the R_{CLK} signal is "L". When the R_{CLK} signal goes from "L" to "H", it is transferred to the slave flip-flop and latched. When the start bit "0" (which is latched first), overflows from the last bit of the 11 bit shift register, it is detected as the stop bit and the RI bit is set.)

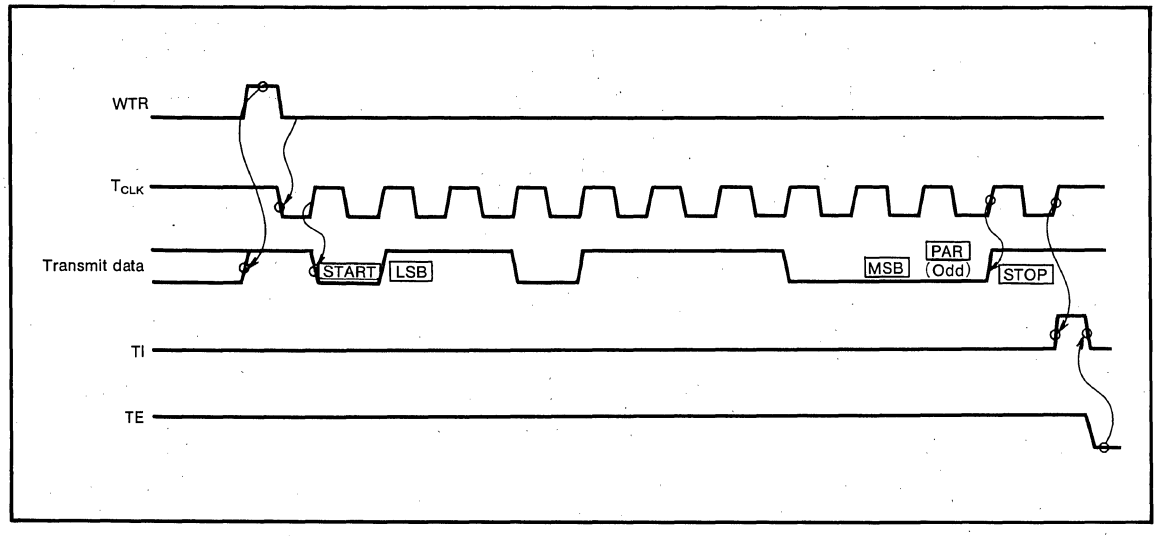


Fig.16 Transmit operation (8-bit+1 parity mode)

(When the T_{CLK} signal goes from "L" to "H", the transmit data is shifted. After the stop bit is transferred, the TI bit is set to "1". The TI bit is cleared when TE is set to "0" or when data is written to the transmit shift register (TR).)

MITSUBISHI ELECTRIC

CLOCKED SERIAL I/O

The M50734SP has one 8-bit clock serial I/O. Its structure and transmit/receive operation are shown in Figure 17. Data is transferred at a transmit speed of 1/4 the oscillation frequency.

Data is transferred and received beginning at the most significant bit.

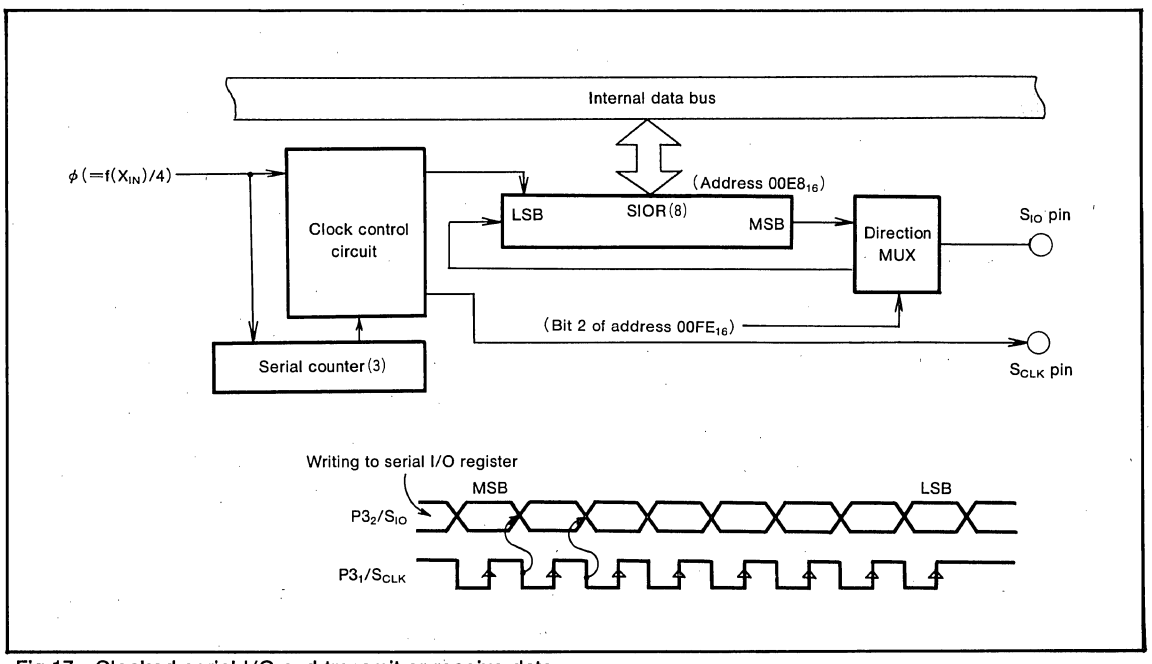


Fig.17 Clocked serial I/O and transmit or receive data

A-D CONVERTER

The A-D conversion circuit is shown in Figure 18. With the A-D analog input pins $P4_0/AN_0 \sim P4_3/AN_3$ are in common with the input pins of the data bus. The A-D control register (address $00E9_{16}$) is a 3-bit register. One of four analog input pins is selected by bit 0 and 1. The relation between bit 0, 1 and the selected analog input pin is shown in Figure 19. The A-D conversion speed is 36μs (at 8MHz frequency) with an absolute conversion precision of $\pm$ 3LSB.

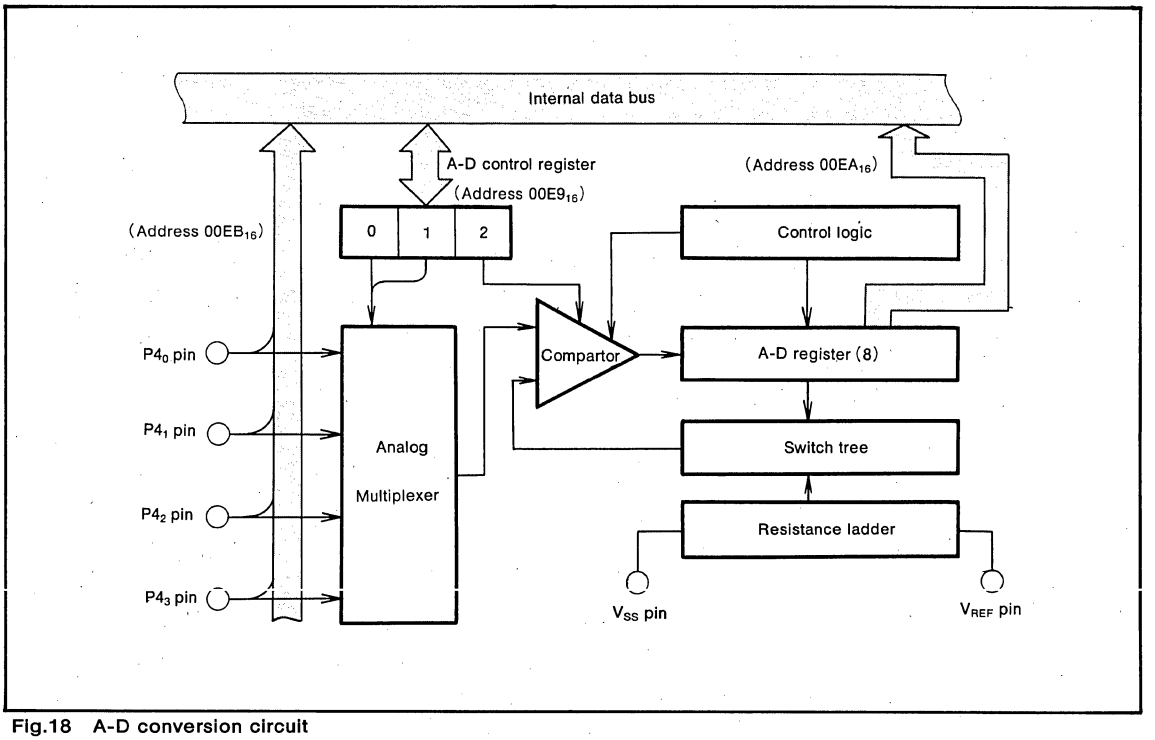


Fig.18 A-D conversion circuit

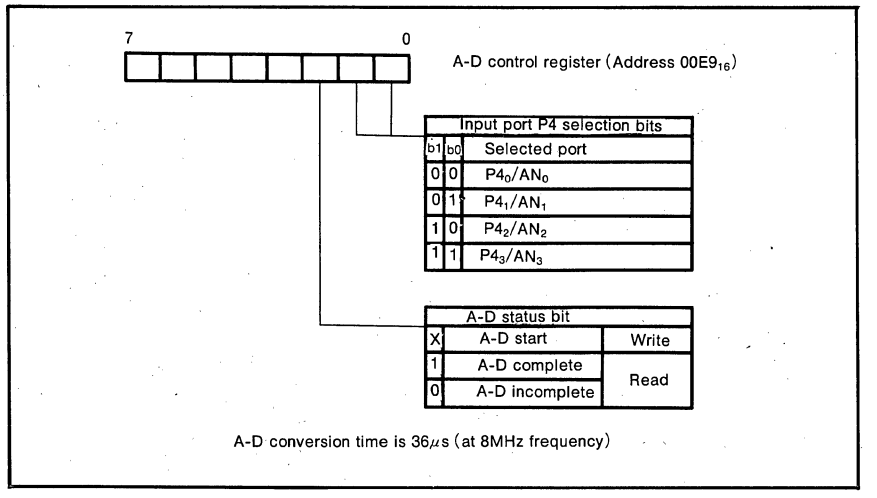
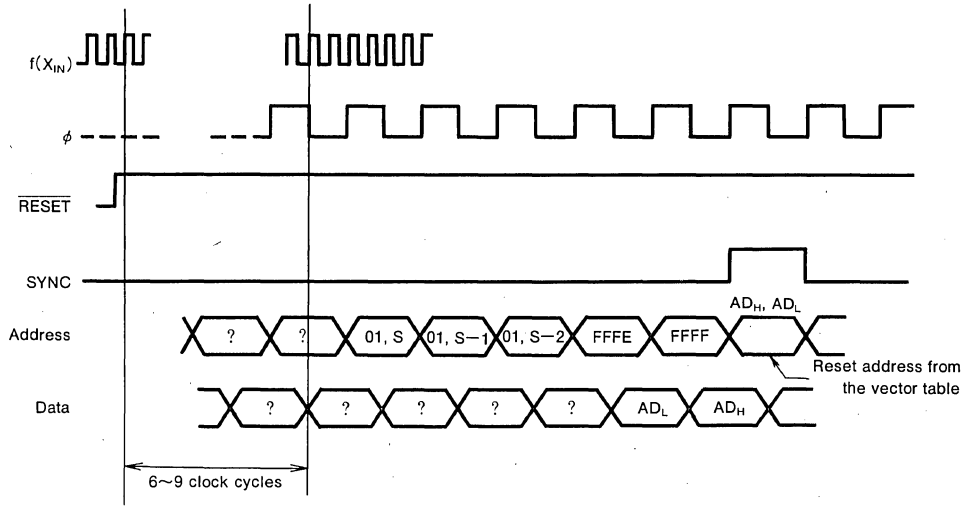


Fig.19 Structure of A-D control register

RESET CIRCUIT

The M50734SP is reset according to the sequence shown in Figure 20. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 22.
An example of the reset circuit is shown in Figure 21.
When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.



Note 1 : The relationship between $f(X_{IN})$ and ϕ is $f(X_{IN})=4 \cdot \phi$
2 : The mark " ? " means that the address is changeable depending on the previous state.

Fig.20 Timing diagram at reset

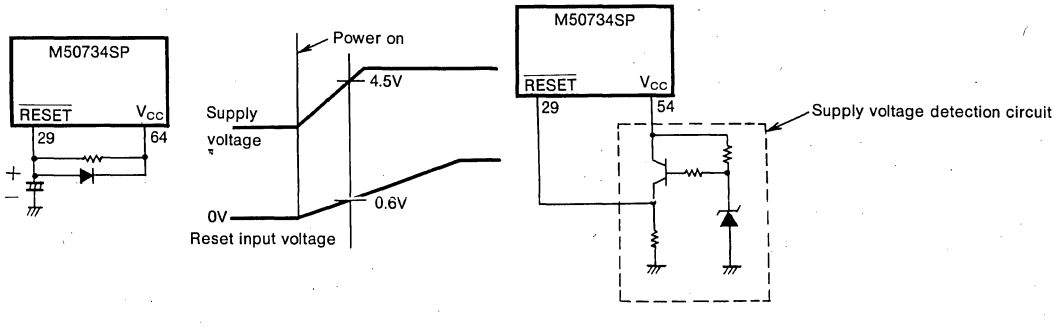


Fig.21 Example of reset circuit

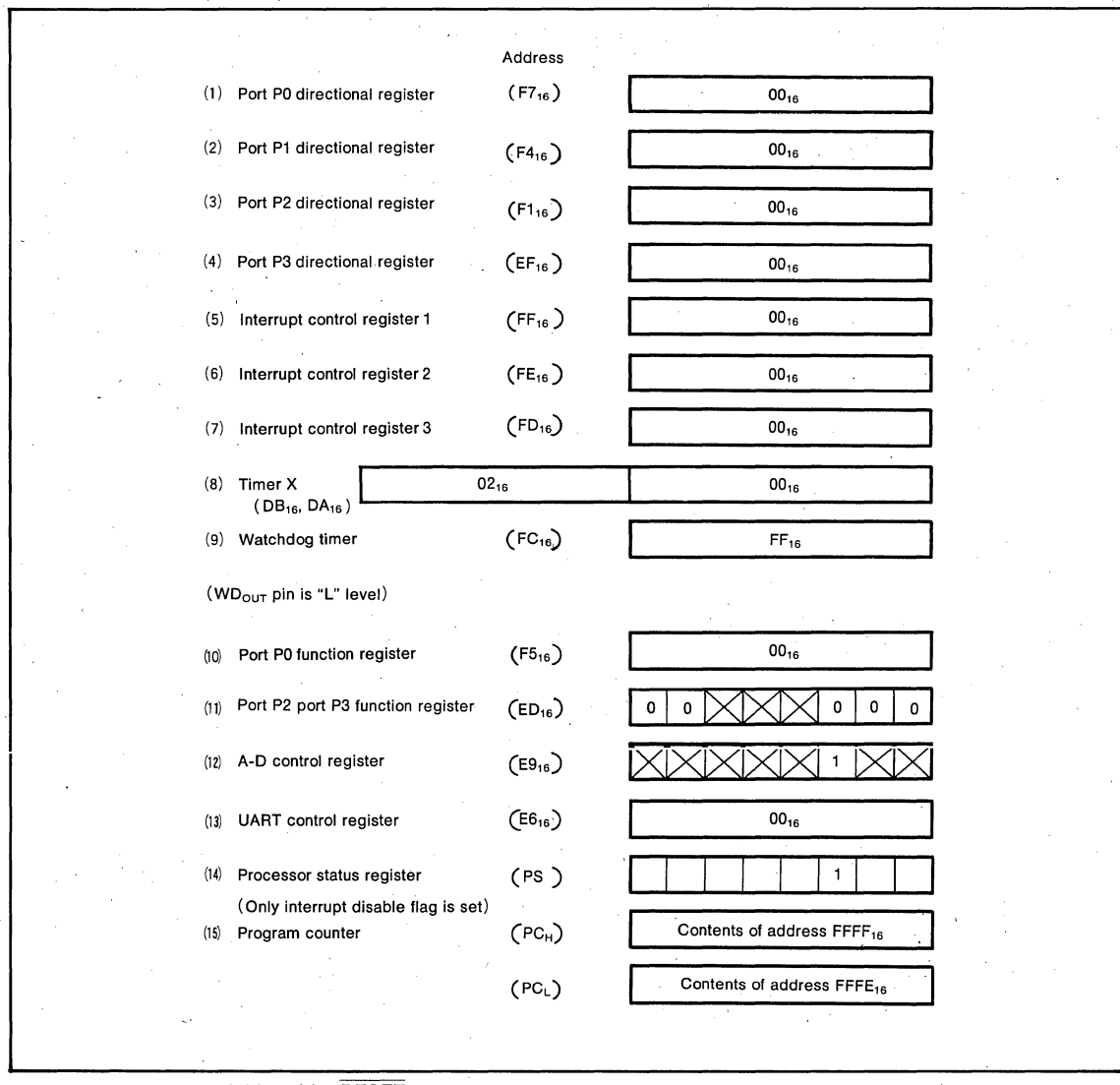


Fig.22 Register state initiated by $\overline{\text{RESET}}$

I/O PORTS

(1) Port P0

Port P0 is a CMOS three state 8-bit input/output port. As shown in the memory map of Figure 1, it is located at address $00F6_{16}$ on the zero page. Port P0 has a directional register (address $00F7_{16}$) to program each individual bit either for input or output. Those pins set to "1" are for output and those programmed to "0" are for input.

This port also has a double function which can be selected for individual bits by the port P0 function register (address $00F5_{16}$). If the contents of the port P0 function register are "0", this port is used as a normal port; if they are "1", this port is used as a special port for functions such as interrupt input, UART input/output etc.

The structure of the port P0 function register is shown in Figure 23.

(2) Port P1

Port P1 is a CMOS tri-state 8-bit input/output port. The I/O function can be selected in the same way as for port P0. An 8-bit input latch (address $00F2_{16}$) of the transparent type, is built into port P1. Therefore, port P1 can be used either by reading address $00F3_{16}$, for non-latched data, or address $00F2_{16}$, for latched data.

(3) Port P2

This port is a CMOS three state 8-bit input/output port. It can be set to input/output in the same way as port P0. By software 2 channels (1 channel=4-bit) from the stepping motor control circuit can be output simultaneously. Four-phase outputs can be selected by bit 6 and bit 7 of the port P2 port P3 function register (address $00ED_{16}$). The structure of the port P2 and P3 function register is shown in Figure 24.

(4) Port P3

Port P3 is an 8-bit CMOS three state input/output port. The pins of port P3 can be set to input/output in the same way as port P0. Ports P3, $P3_1$ and $P3_2$ have double functions, which are determined by bits 0 and 1 of the port P2 and port P3 function register (address $00ED_{16}$).

(5) Port P4

Port P4 is a 4-bit input port. It can be used not only a as 4-bit digital input port, but also as an analog input port for the A-D converter.

If it is used as a digital input port, the contents of address $00EB_{16}$ are read.

The 4 high-order bits of address $00EB_{16}$ are usually "0". If port P4 is used as analog input, the ports are multiplexed by the A-D control register and A-D conversion is executed. When digital input is performed during A-D conversion, care is necessary as the precision of A-D conversion can sometimes be affected.

(6) WD_{OUT} pin

This pin is set after the contents of the watchdog timer W resetting. It can not be cleared by software, only by reset.

(7) ϕ pin

The oscillation frequency, divided by 4, is output from this pin.

(8) Address bus and data bus

The 8 high order bits of the address bus are output directly from $A_{15} \sim A_8$. Addresses and data of $A_7/D_7 \sim A_0/D_0$ are multiplexed. When ϕ is "H", the 8 low order bits are output, and when ϕ is "L", data can be transferred between $A_7/D_7 \sim A_0/D_0$ and external memory. The 8 low order address bits must be latched in an external latch with the ALE signal.

(9) $\overline{RD}$ pin

While $\overline{RD}$ is "L", the M50734SP can read external memory.

(10) $\overline{WR}$ pin

While $\overline{WR}$ is "L", the M50734SP can write to external memory.

(11) ALE pin

The ALE pin outputs the ALE signal to latch the low order address bits. The ALE signal is always generated once during a every machine cycle.

The 8 low order bits of the address bus start output when ALE signal changes from low to high. A transparent latch is used to allow an address set-up time. The address is latched when the ALE signal changes from high to low.

(12) SYNC pin

The SYNC signal controls single step operation of the M50734SP. It is synchronized with the ϕ signal and is output when an op code is fetched.

(13) V_{REF} pin

V_{REF} serves as reference voltage for the A-D converter.

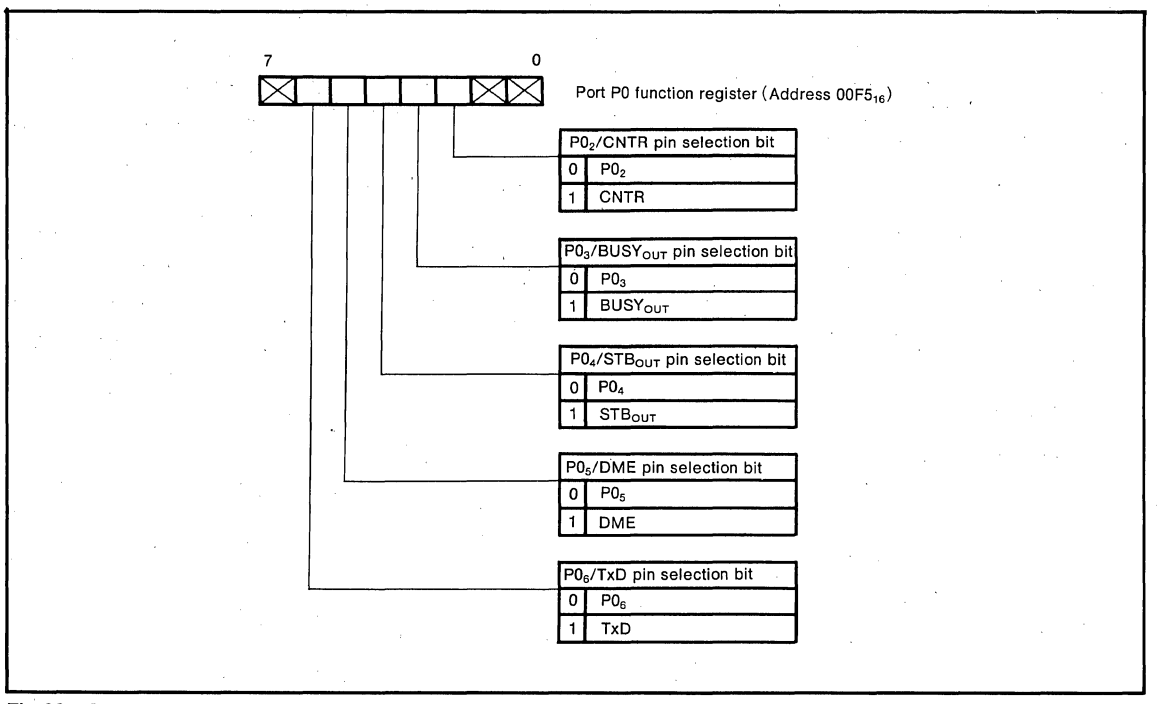


Fig.23 Structure of Port P0 function register

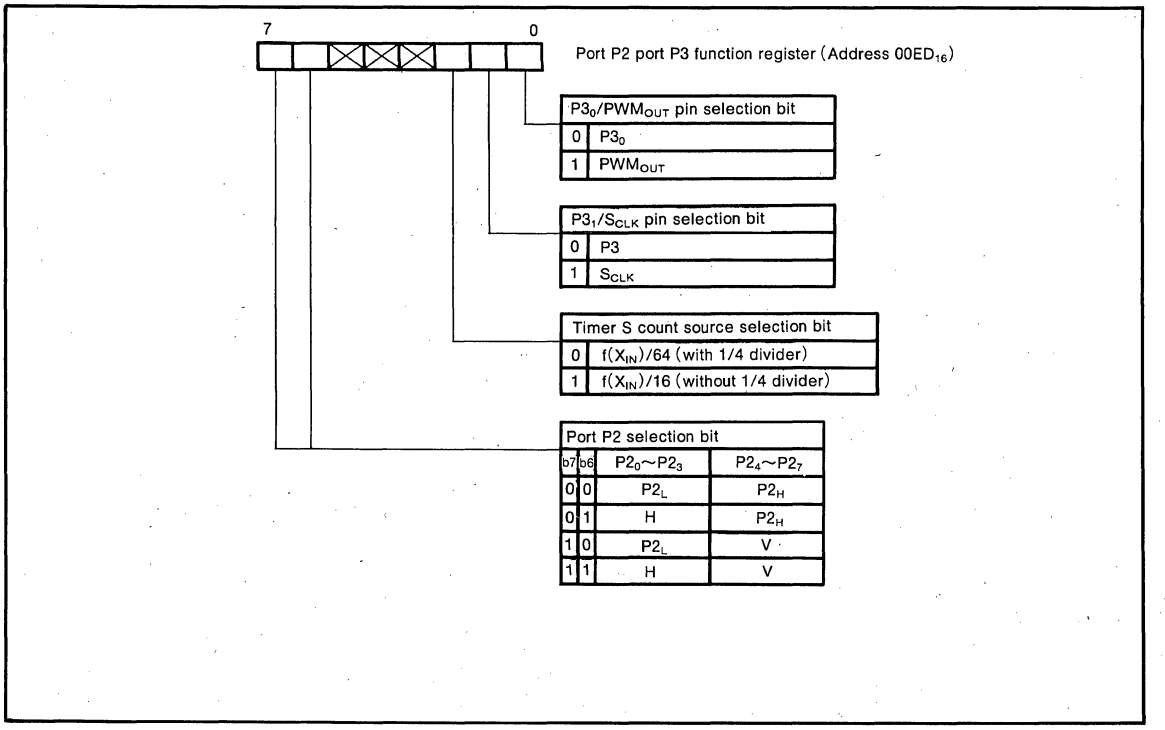


Fig.24 Structure of Port P2 and P3 function register

MITSUBISHI ELECTRIC

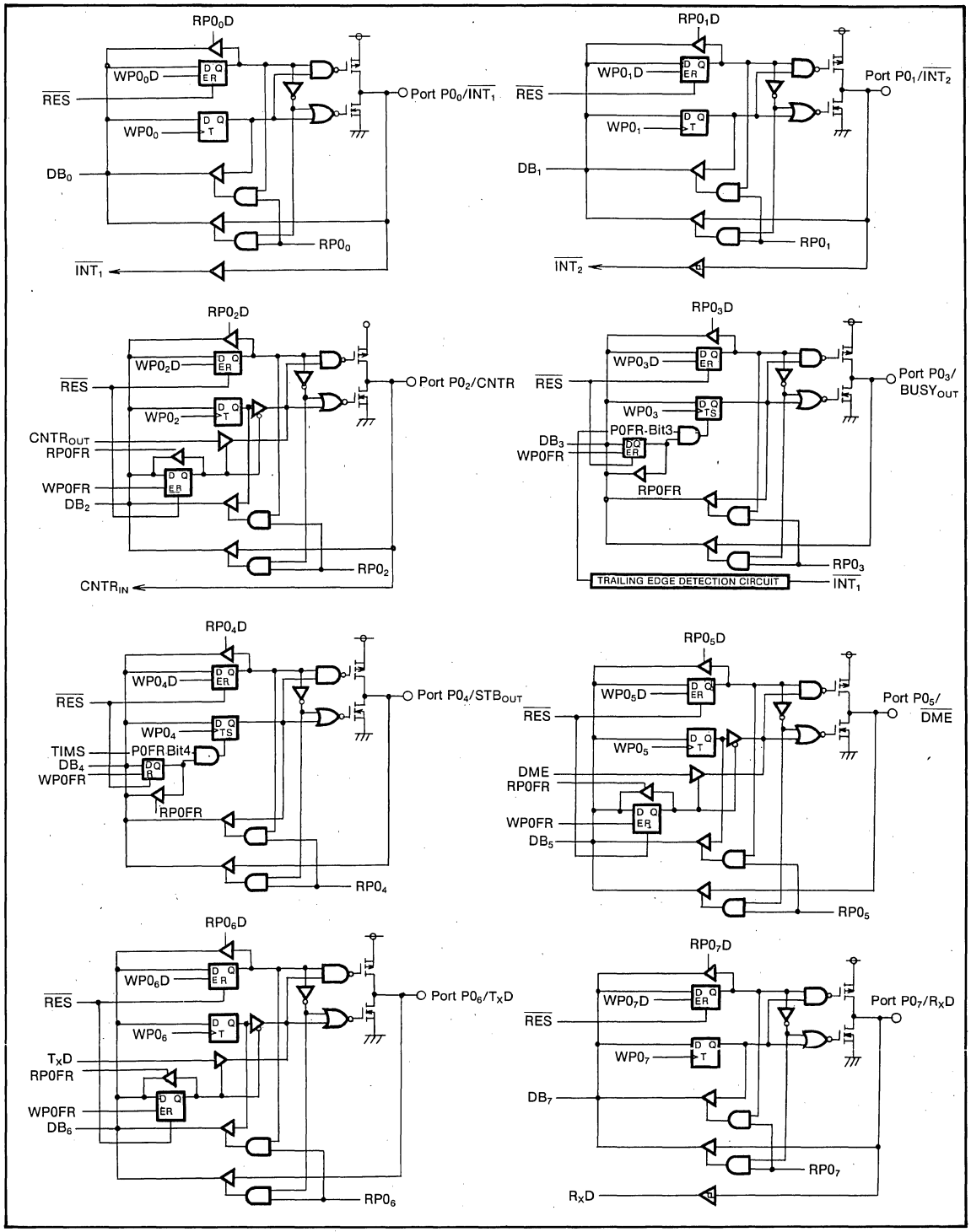


Fig.25 Block diagram-1 of input/output pins

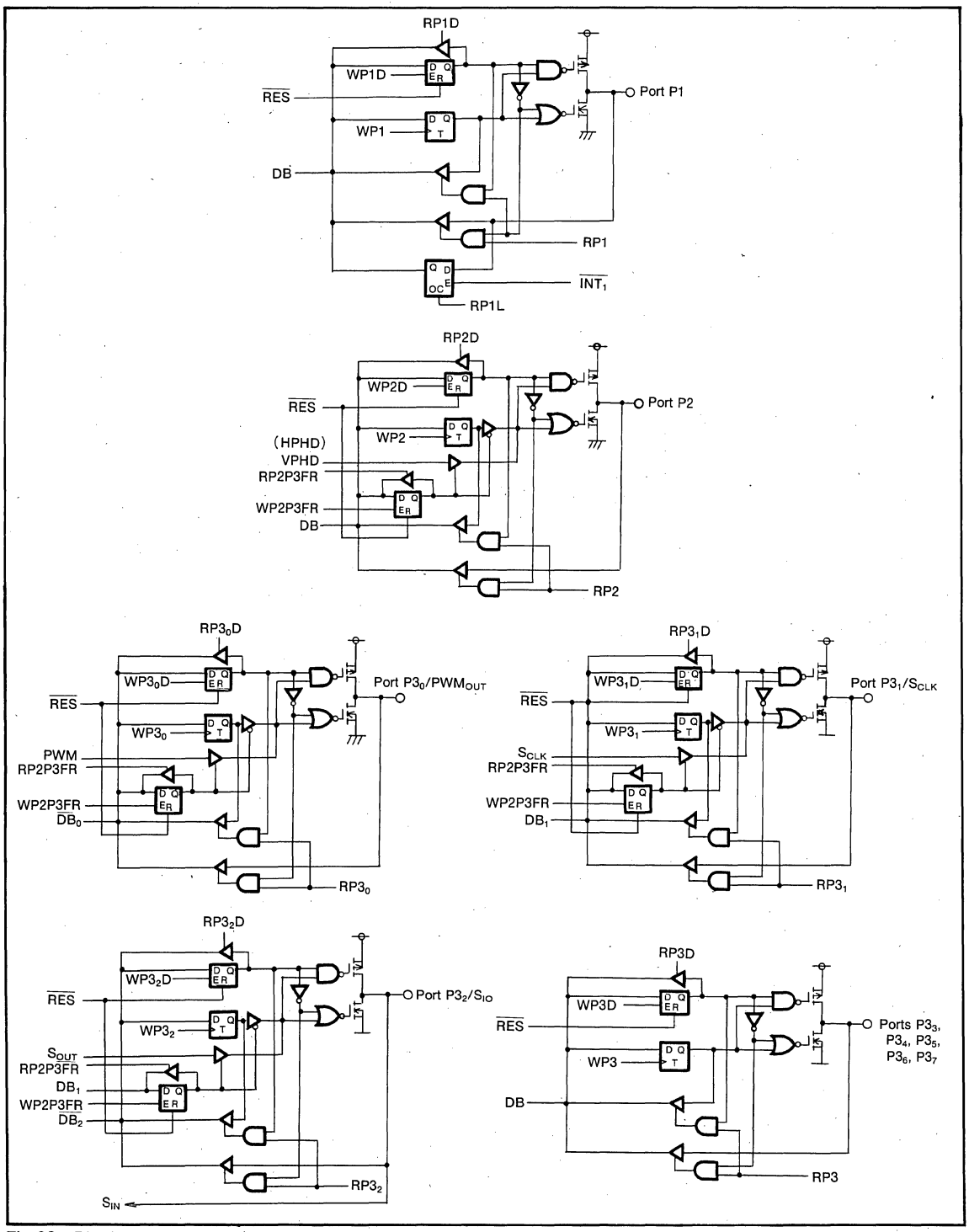


Fig.26 Block diagram-2 of input/output pins

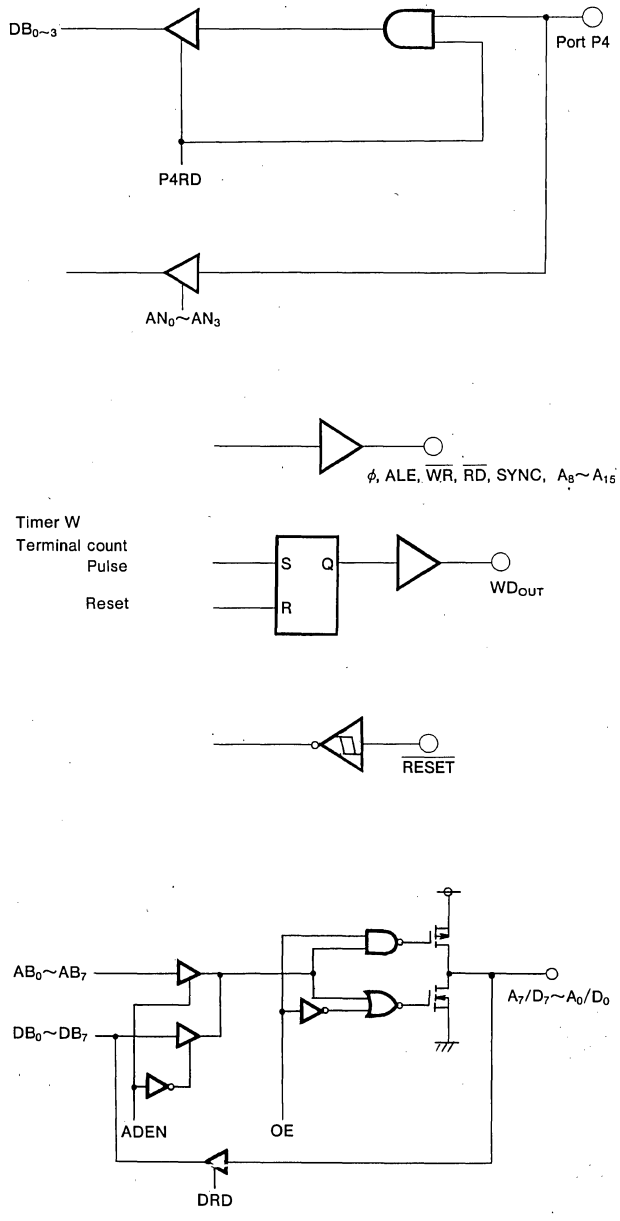


Fig.27 Block diagram-3 of input/output pins

CLOCK GENERATING CIRCUIT

The built-in clock generating ciruit is shown in Figure 28. When a STP instruction is executed, the oscillation stops at the "H" state of the internal clock ϕ. Moreover, timer X is set to 0200_{16}, and the oscillation output divided by 16 is connected to timer X. This connection is cleared when timer X overflows, or by resetting as discussed in the timer section.

The oscillation restarts after an interrupt is accepted, but the internal clock ϕ remains at "H" until timer X overflows. This is necessary because the oscillation needs a set-up period if a ceramic or a crystal oscillator is used. When the WIT instruction is executed, the internal clock ϕ stops at "H" but the oscillator will not stop. This wait state is cleared after an interrupt is accepted. Since the oscillation does not stopp, the following instruction will be executed immediately and not after a fixed time as for the STP instruction. The corresponding interrupt enable bit must be set to "1" before the STP or WIT instruction is executed.

When the STP state is cleared, timer X counts the oscillation frequency divided by 16. Therefore, timer X count stop bit (bit 2 of address $00FD_{16}$) must be set to "0" before the STP instruction is executed.

An example of ceramic oscillation (or quartz crystal oscillation) is shown in Figure 29. The value of the capacitance differs depending on the oscillator. Therefore, adjust the value as recommended by the each oscillator manufactures. An example where the clock signal is supplied from outside is shown in Figure 30. X_{IN} is the clock input, and X_{OUT} is open.

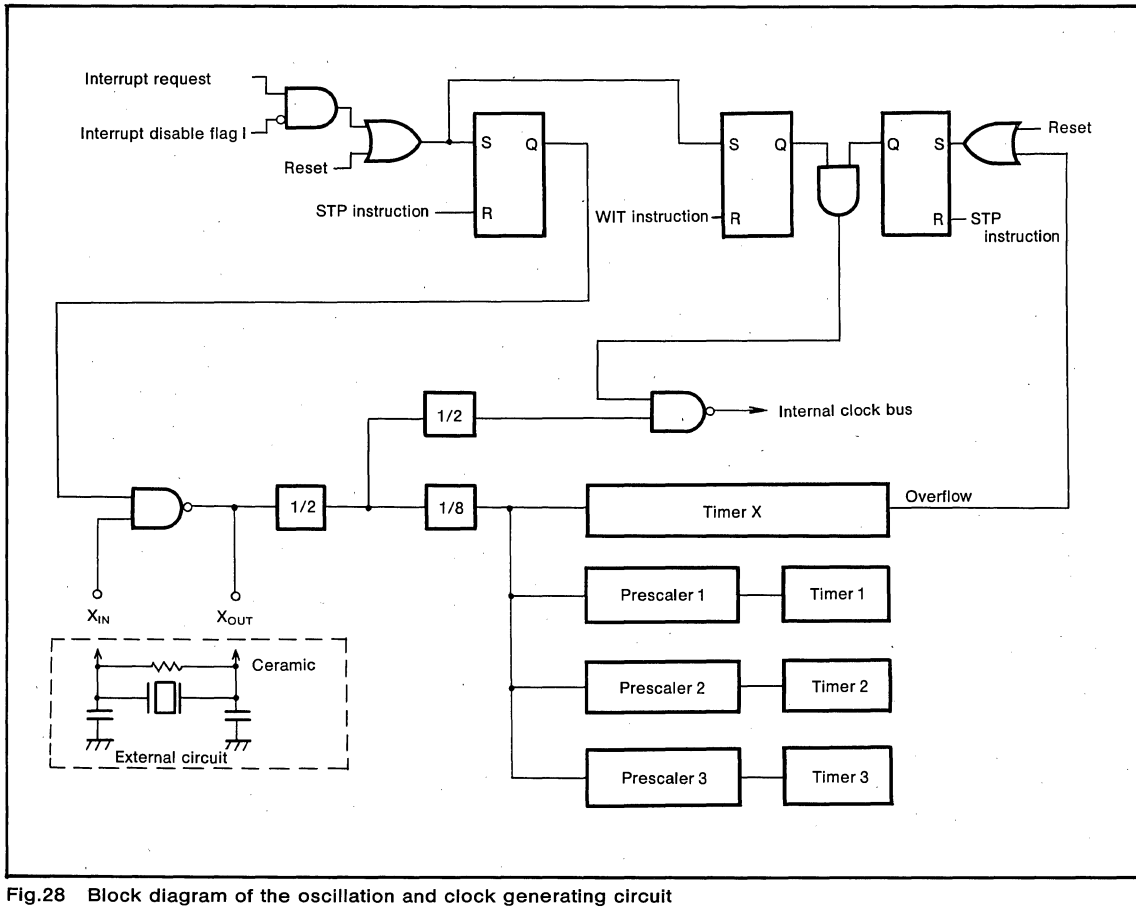


Fig.28 Block diagram of the oscillation and clock generating circuit

MITSUBISHI ELECTRIC

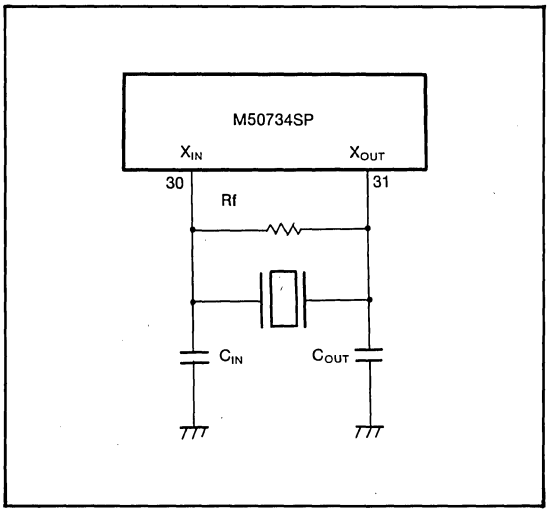


Fig.29 External ceramic resonator circuit

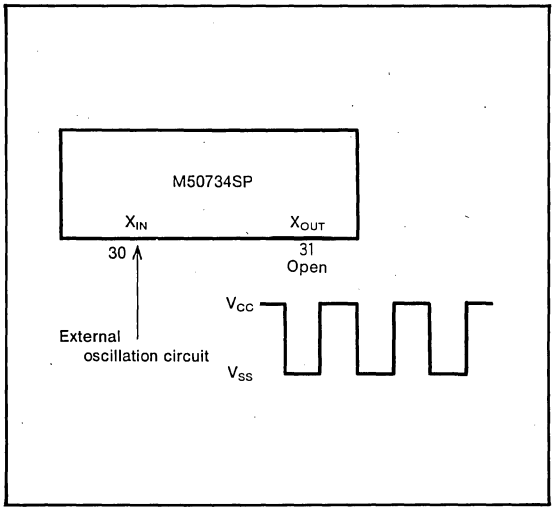


Fig.30 External clock input circuit

STANDBY MODE

The M50734SP can stop oscillation, preserving the contents of all registers, input/output ports and so on except timer X. Therefore, it can begin operation again in the same state as before it stopped; power dissipation is greatly reduced. The STP instruction is used to stop the oscillation. When the STP instruction is executed, it stops at the address fetch state of the next instruction. After RESET or an $\overline{INT_1}$, $\overline{INT_2}$ or CNTR interrupt is accepted, the oscillation starts again. Therefore, before the STP instruction is executed, one of the above interrupts must be enabled and the TXG (interrupt control register 3 (ICON 3), pin 2) must be cleared.

After the oscillation has been restarted by any means other than $\overline{RESET}$, the internal clock will start after timer X has counted 8208 cycles. When a ceramic oscillator is used, this time is needed to avoid instability at the oscillation rise. The block diagram of the standby mode is shown in Figure 31.

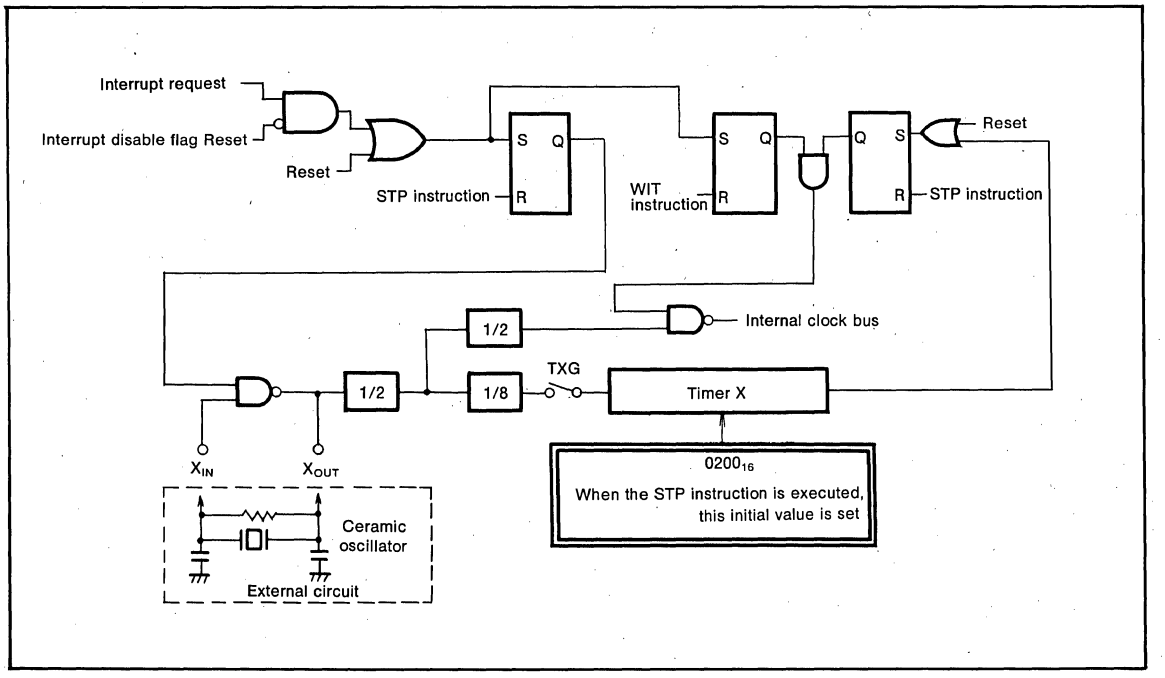


Fig.31 Block diagram of standby mode

MITSUBISHI ELECTRIC

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When the timer X is used at event counter mode, the contents of the timer X must be read after the TXG flag is cut off. If the TXG flag is not cut off, the plural reading data of the contents of the timer X must be compared and used as real data of the timer X.
When the timer X at the other modes, other timers and prescalers are used, the contents of data can be read at optional time.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, SED, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) Notes on the stepper motor control circuit

① The single-shot must not be used while the horizontal or vertical counter and the phase counter are linked with timers, because they can not rewrite data.

② When the stepper motor control register is set and reset, the bit set and bit reset instructions must be used.

(7) The area of addresses $00D0_{16} \sim 00D9_{16}$ can not be used, because those area are reserved for system expansion.

(8) When the port P0 function register is set and reset, CLB, SEB, and STA instructions must be used.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors are at "off" state.	−0.3~7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}		−0.3~7	V
V_{REF}	Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, AD_0~AD_7, V_{REF}		−0.3~V_{CC}+0.3	V
V_O	Onput voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}, X_{OUT}		−0.3~V_{CC}+0.3	V
P_d	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−10~70	℃
T_{stg}	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$ (During using as a port) $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, AD_0~AD_7	2.0		V_{CC}+0.3	V
V_{IH}	"H" input voltage, R_XD, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}+0.3	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$ (During using as a port) $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, AD_0~AD_7	−0.3		0.8	V
V_{IL}	"L" input voltage, R_XD, CNTR $\overline{INT_1}$, $\overline{INT_2}$	−0.3		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	−0.3		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	−0.3		0.16V_{CC}	V
V_{REF}	Standard voltage input	0.5V_{CC}		V_{CC}	V
V_{IA}	Analog input voltage, $P4_0$~$P4_3$	−0.3		V_{CC}+0.3	V
$I_{OL(perk)}$	"L" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			5	mA
$I_{OL(avg)}$	"L" average output current (Note1), $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, AD_0~AD_7, A_3~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			2	mA
$I_{OH(peak)1}$	"H" peak output current, $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			−5	mA
$I_{OH(peak)2}$	"H" peak output current, $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$			−10	mA
$I_{OH(avg)1}$	"H" average output current, (Note1) $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			−2	mA
$I_{OH(avg)2}$	"H" average output current, (Note1) $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$			−10	mA

Note 1 : $I_{OL(avg)}$, $I_{OH(avg)}$ is the average current in 100ms.

2 : The total of $I_{OL(peak)}$, of $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE and WD_{OUT} should be 80mA max

The total of $I_{OL(peak)}$, of $P1_0$~$P1_7$, $P2_0$~$P2_7$ and $P3_0$~$P3_7$ should be 80mA max

The total of $I_{OH(peak)}$, of $P0_0$~$P0_7$, AD_0~AD_7 and A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE and WD_{OUT} should be −60mA max

The total of $I_{OH(peak)}$, of $P1_0$~$P1_7$, $P2_0$~$P2_7$ and $P3_0$~$P3_7$ should be −80mA max

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage all output pin except X_{OUT} pin	I_{OH} = −200μA	2.4			V
		I_{OH} = −10μA	V_{CC}−0.7			
V_{OL}	"H" output voltage all output pin except X_{OUT} pin	I_{OL} = 1.6mA			0.5	V
I_I	Input leak current, P_0~$P4_3$, $\overline{RESET}$	$V_{SS} \leqq V_I \leqq V_{CC}$	−5		5	μA
I_{OZ}	Three state leak current, all input/output pin	V_{SS} + 0.5V ≦ V_O ≦ V_{CC} − 0.5V	−5		5	μA
$V_{T+}-V_{T-}$	Hysteresis width, $\overline{INT_1}$, $\overline{INT_2}$, CNTR, R_XD, $\overline{RESET}$	When used as function except port		0.6		V
I_{OH}	"H" output current, $P2_0$~$P2_7$	V_{OH} = 1.5V	−1		−10	mA
I_{CC}	Supply current	During operating (Output transistors cut-off)		6	15	mA
		Wait mode (Output transistors cut-off)		1	3	
		Stop mode (Output transistors cut-off)		1	20	μA
I_{ACC}	A/D supply current	During executing A/D convert			6	mA

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(D-\phi)}$	Data input set-up time	Fig.32	80			ns
$t_{SU(P0-\phi)}$	Port P0 input set-up time		250			ns
$t_{SU(P1-\phi)}$	Port P1 input set-up time		250			ns
$t_{SU(P2-\phi)}$	Port P2 input set-up time		250			ns
$t_{SU(P3-\phi)}$	Port P3 input set-up time		250			ns
$t_{SU(P4-\phi)}$	Port P4 input set-up time		250			ns
$t_{SU(P1-\overline{INT_1})}$	Port P1 latch input set-up time		250			ns
$t_{SU(S_{IN}-S_{CLK})}$	Serial input set-up time		250			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{h(\phi-P0)}$	Port P0 input hold time		50			ns
$t_{h(\phi-P1)}$	Port P1 input hold time		50			ns
$t_{h(\phi-P2)}$	Port P2 input hold time		50			ns
$t_{h(\phi-P3)}$	Port P3 input hold time		50			ns
$t_{h(\phi-P4)}$	Port P4 input hold time		50			ns
$t_{h(\overline{INT_1}-P1)}$	Port P1 latch input hold time		50			nS
$t_{h(S_{CLK}-S_{IN})}$	Serial input hold time		50			ns
$t_{WL(\overline{INT_1})}$	$\overline{INT_1}$ input "L" pulse width		250			ns
$t_{WL(\overline{INT_2})}$	$\overline{INT_2}$ input "L" pulse width		1			μs
$t_{WL(CNTR)}$	CNTR input "L" pulse width		1			μs
$t_{WH(\overline{INT_1})}$	$\overline{INT_1}$ input "H" pulse width		1			μs
$t_{WH(\overline{INT_2})}$	$\overline{INT_2}$ input "H" pulse width		1			μs
$t_{WH(CNTR)}$	CNTR input "H" pulse width		1			μs
$t_{C(X_{IN})}$	External clock input cycle time		125			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width		45			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width		45			ns
$t_{W(\overline{RESET})}$	$\overline{RESET}$ input "L" pulse width		2			μs

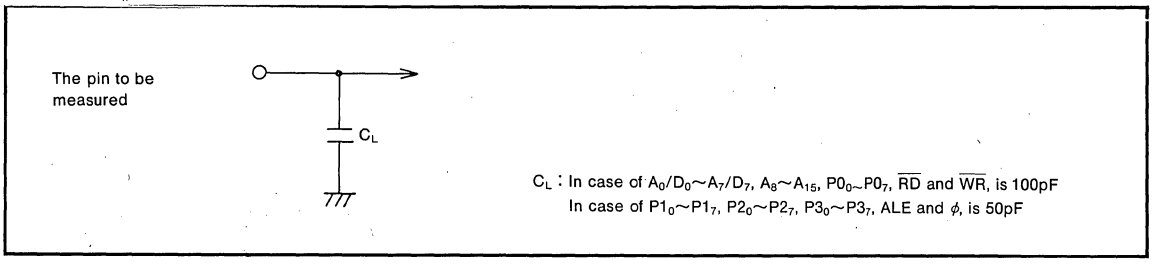


Fig.32 Measurement circuit diagram

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
※$t_{C(\phi)}$	Cycle time (Note 6)	Fid.32	500			ns
※$t_{WH(\phi)}$	ϕ clock pulse width (High level) (Note 2)		220			ns
※$t_{WL(\phi)}$	ϕ clock pulse width (Low level) (Note 2)		220			ns
$t_{r(\phi)}$	ϕ clock rising edge time				30	ns
$t_{f(\phi)}$	ϕ clock falling edge time				30	ns
※$t_{d(\phi\text{-ALE})}$	Address strobe pulse delay time (Note 4)				60	ns
※$t_{W(ALE)}$	Address strobe pulse width (Note 3)		100			ns
$t_{d(A\text{-ALE})}$	Address-ALE delay time		30			ns
$t_{v(ALE\text{-}A)}$	Address effective time after ALE		30			ns
$t_{d1(\phi\text{-}A)}$	Address delay time 1				130	ns
※$t_{d2(\phi\text{-}A)}$	Address delay time 2 (Note 1)				150	ns
$t_{v(\phi\text{-}A)}$	Address effective time after ϕ		10			ns
※$t_{W(RD)}$	$\overline{RD}$, $\overline{WR}$ pulse width (Note 2)		220			ns
$t_{d(\phi\text{-RD})}$	$\overline{RD}$, $\overline{WR}$ delay time				20	ns
$t_{v(\phi\text{-RD})}$	$\overline{RD}$, $\overline{WR}$ effective time after ϕ				10	ns
$t_{d(AZ\text{-RD})}$	address floating-$\overline{RD}$ delay time		0			ns
$t_{d(\phi\text{-D})}$	Data delay time (write cycle)				150	ns
※$t_{v(\phi\text{-D})}$	Data effective time after ϕ (Note 5)		40			ns
$t_{d(\phi\text{-P0})}$	Port P0 data output delay time				250	ns
$t_{d(\phi\text{-P1})}$	Port P1 data output delay time				250	ns
$t_{d(\phi\text{-P2})}$	Port P2 data output delay time				250	ns
$t_{d(\phi\text{-P3})}$	Port P3 data output delay time				250	ns
$t_{d(\phi\text{-}S_{CLK})}$	Serial clock delay time				60	ns
$t_{v(\phi\text{-}S_{CLK})}$	Serial clock effective time after ϕ				40	ns
$t_{d(S_{CLK}\text{-}S_{OUT})}$	Serial output delay time				150	ns
$t_{v(S_{CLK}\text{-}S_{OUT})}$	Serial output effective time after serial clock		0			ns
$t_{d(\overline{INT_1}\text{-BSY})}$	Busy output delay time				250	ns

※ This timing is changed by $t_C(X_{IN})$, The timing of this list is the value in $t_C(X_{IN})$ = 125ns

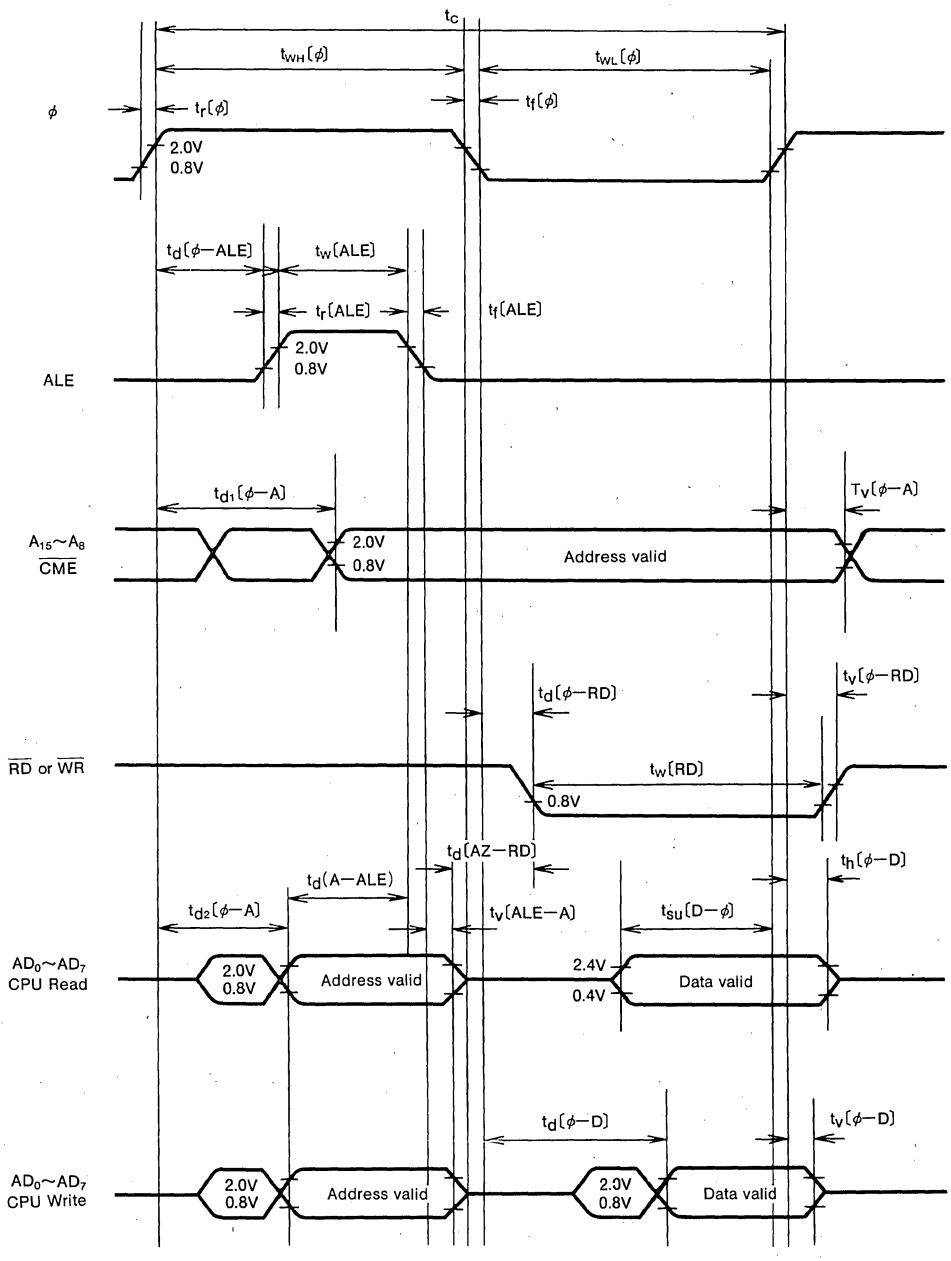
Note 1 : This value is defined as follows : $t_{dz}(\phi\text{—}A)=t_C(\phi)/8+8.75$
2 : This value is defined as follows : $t_W(RD)=t_C(\phi)/2-30$
3 : This value is defined as follows : $t_W(ALE)=t_C(\phi)/4-25$
4 : This value is defined as follows : $t_d(\phi\text{—}ALE)=t_C(\phi)/8-2.5$
5 : This value is defined as follows : $t_v(\phi\text{—}D)=t_C(\phi)/8-22.5$
6 : This value is defined as follows : $t_C(\phi)=4t_C(X_{IN})$

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, $f_{(X_{IN})}$=8MHz, unless otherwise noded)

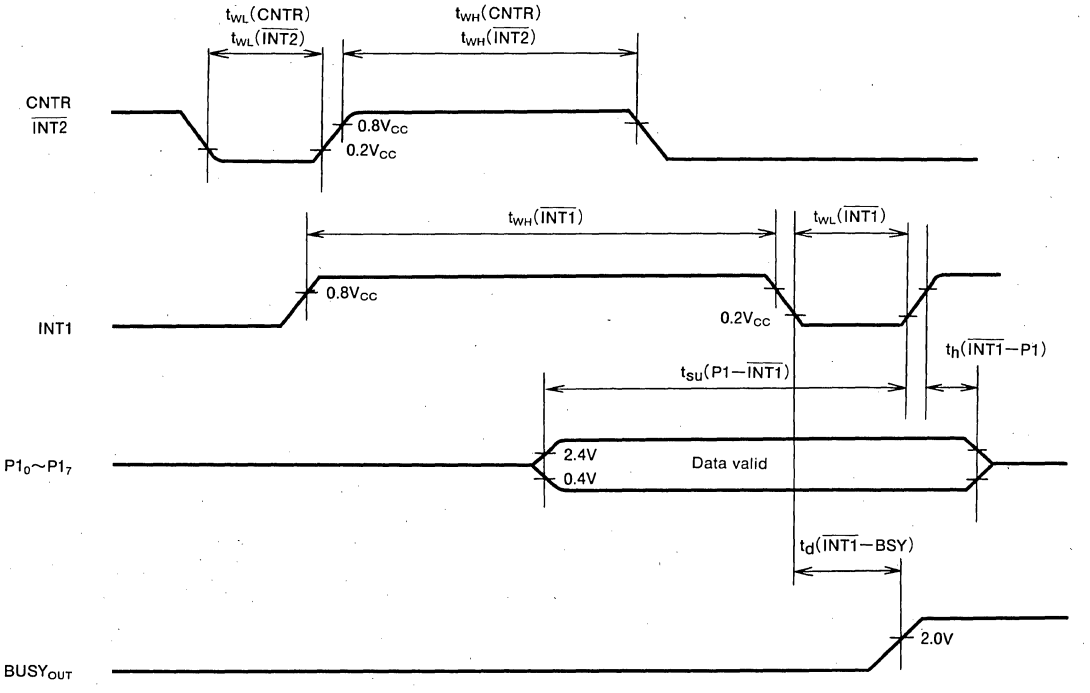
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution		8			Bits
—	Absolute accuracy	$V_{CC}=V_{REF}$=5.12V		±1 1/2	±3	LSB
R_{LADDER}	Ladder resistance value		1			KΩ
t_{CONV}	Conversion time				36	μs
$I_{I(AD)}$	Input current in A-D convert	$0 \leq V_I \leq V_{REF}$			50	μA

TIMING DIAGRAM

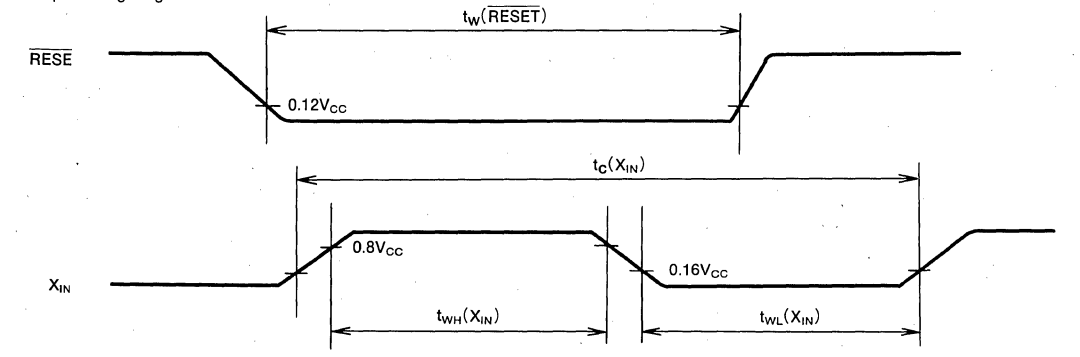
Bus timing diagram



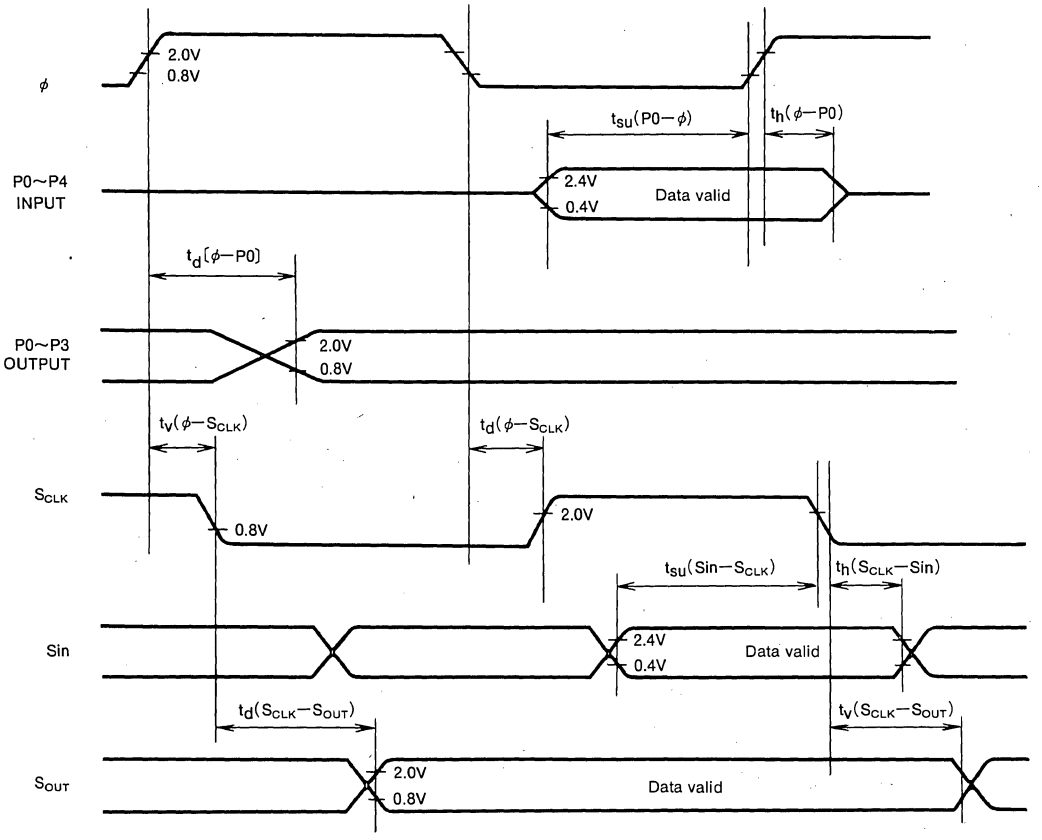
Port P1 latch input timing diagram



X_{IN}, RESET input timing diagram



Port P0~P4 input/output, serial I/O timing diagram



M50734SP-10

8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50734SP-10 is a microcomputer designed with CMOS sillicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. This microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50734SP-10 and the M50734SP are noted below.

Type name	maximum value of clock generating frequency
M50734SP	8MHz
M50734SP-10	10MHz

In this section, the following explanations apply to the differences between the M50734SP and the M50734SP-10. Other functions are explaned the M50734SP/FP's section in detail.

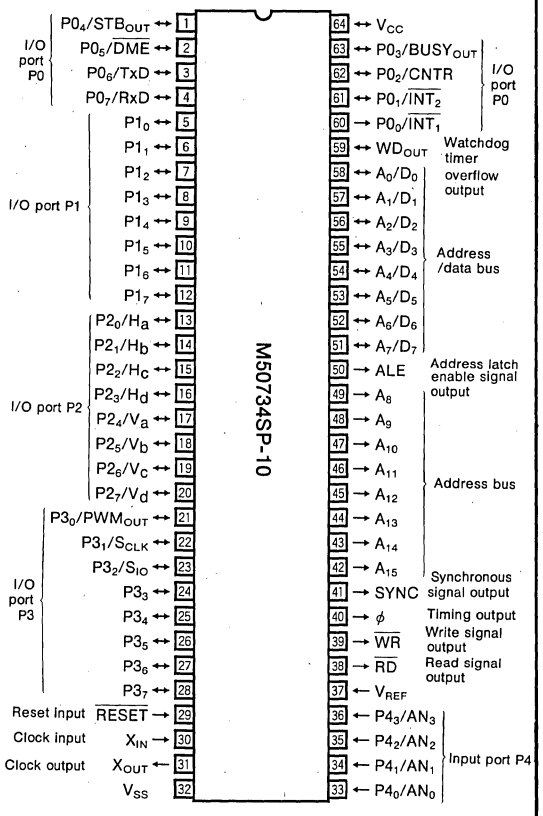
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size (internal memories are not provided)
  - Memory area programmable memory ..... 64k bytes
  - data memory ..... 64k bytes
- Instruction execution time
  - .....0.8μs (minimum instructions, at 10MHz frequency)
- Single power supply .....5V$\pm$10%
- Power dissipation normal operation mode
  - (at 10MHz frequency) 35mW
- Subroutine nesting ..... 128 levels (Max.)
- Interrupt ..... 11 types, 5 vectors
- Timers
  - 16-bit timer/event counter (general purpose) 1
  - 8-bit timer (general purpose) 3
  - 8-bit timer (watchdog timer) 1
  - 8-bit timer (strobe timer) 1
  - 8-bit timer (baud rate timer) 1
  - 8-bit counter (control for stepper motor) 2
- Stepper motor control circuit
  - ..... 1 channel for the X or Y direction
- Programmable I/O ports (Ports P0, P1, P2, P3) 32
- Input ports (Port P4) 4
- Serial I/O
  - 8-bit clock synchronous 1
  - 8-bit UART 1
  - Baud rate (at 9.83MHz frequency)...75bps~76800bps
- A-D converter ..... 8-bit successive approximation
- PWM function 1
- Multiplex-type bus
  - Address bus 16
  - Data bus (multiplexed with lower address bus) 8

APPLICATION

Printer/plotter, Electronic typewriter, PPC, FAX, Portable word processor, Robotics

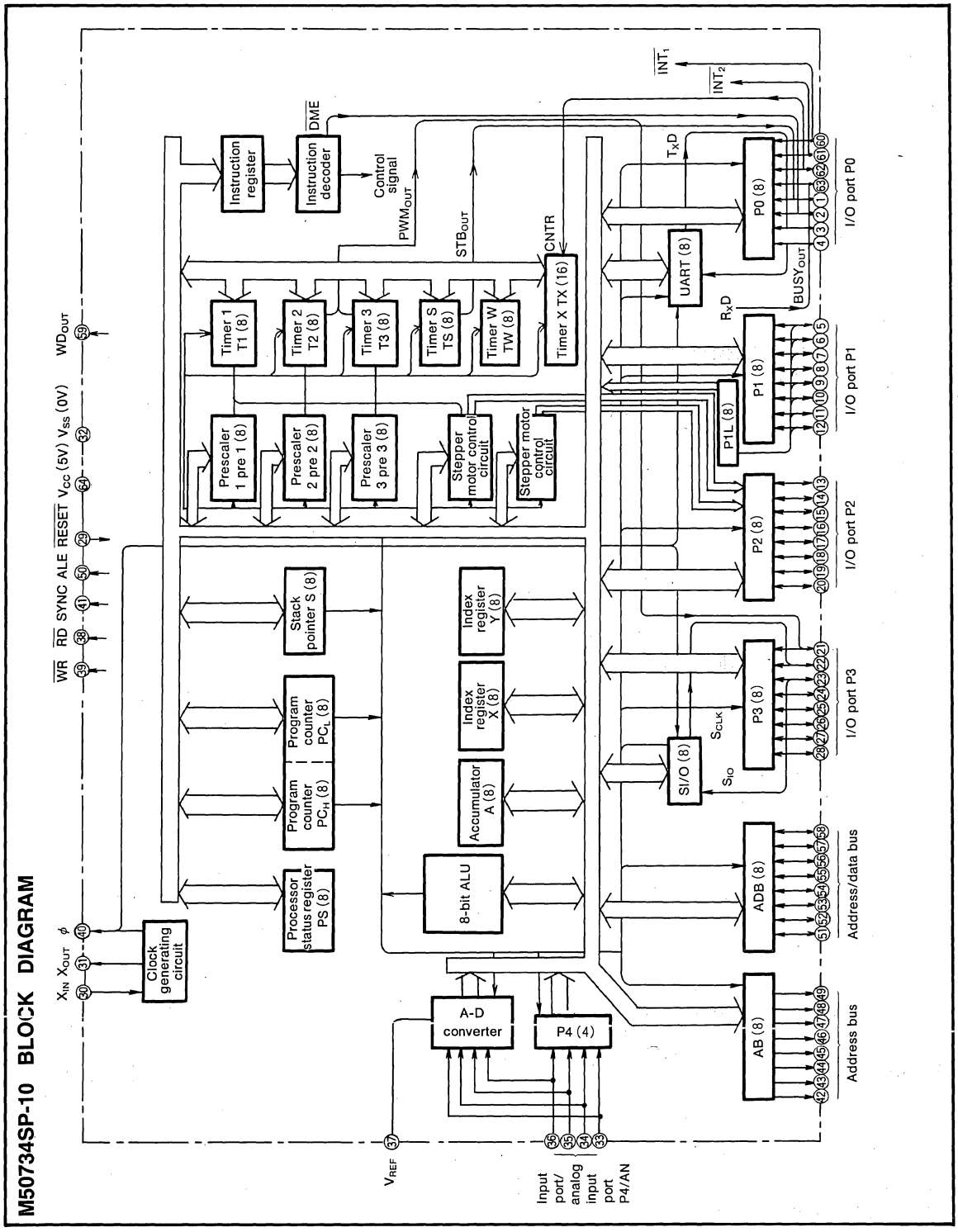
PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

MITSUBISHI ELECTRIC

M50734SP-10 BLOCK DIAGRAM



FUNCTIONS OF M50734SP-10

Parameter			Functions
Number of basic instructions			69
Instruction execution time			0.8μs (minimum instructions, at 10MHz frequency)
Clock frequency			10MHz
Memory size			64K bytes (up to 128k bytes with DME signal)
Input/Output ports	P0, P1, P2, P3	I/O	8-bit×4 (all pins of P0, P2, and part of P3 have double functions)
	P4	input	4-bit×1 (P4 is in common with analog input)
UART			1 (built-in baud rate generator, 75~76800bps)
Clock synchronized serial I/O			8-bit×1
Timer	Timer X		16-bit×1
	Timer 1		8-bit×1 (with 8-bit prescaler)
	Timer 2		8-bit×1 (with 8-bit prescaler)
	Timer 3		8-bit×1 (with 8-bit prescaler)
	Timer S		8-bit×1 (with 1/4 frequency divider)
	Timer W		8-bit×1 (with 1/1024 frequency divider)
A-D converter			Four analog inputs, 8-bit successive approximation
Subroutine nesting			128 levels (max.)
Interrupts			Three external interrupts, four timer interrupts Two counter interrupts, one UART interrupt
Clock generating circuit			Built-in (externally connected to a ceramic resonator or a quartz crystal resonator)
Supply voltage			5V±10%
Power dissipation	at normal operation (at 8MHz frequency)		35mW
	at wait mode		5mW
	at stop mode		5μW
Operating temperature range			−10~70℃
Device structure			CMOS sillicon gate process
Package			64-pin shrink plastic molded DIP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin. Clock oscillating frequency f(X_{IN}) divided by 4 signal is outputed.
SYNC	Synchronous signal output	Output	Synchronous signal is outputed when the op code is feched, and is used to control the program's single-step operation.
$\overline{RD}$	Read signal output	Output	Control signal for read access to ROM, RAM and peripherals.
$\overline{WR}$	Write signal output	Output	Control signal for write access to RAM and peripherals.
ALE	Address latch enable signal output	Output	Address latch signal for address A_0~A_7.
A_{15}~A_8	Address bus	Output	The contents of the high-order 8 bits of the address bus are output (CMOS output).
A_7/D_7~ A_0/A_0	Address/Data bus	I/O	The contents of the lower-order 8 bits of the address bus and 8 bits of the data bus are multiplexed and output/input (CMOS output).
WD_{OUT}	Watchdog timer overflow output	Output	When the watchdog timer overflows, this pin is set to "H". Cleared only at reset.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with CMOS tri-state output. Each port has double function, and can switch by software.
$\overline{INT_1}$($P0_0$)	Interrupt input	Input	This is an interrupt input pin.
$\overline{INT_2}$($P0_1$)	Interrupt input	Input	This is an interrupt input pin.
CNTR($P0_2$)	Timer I/O	I/O	This is an output pin for the timer X.
$BUSY_{OUT}$($P0_3$)	Busy signal output	Output	When the falling edge is inputed to $\overline{INT_1}$ pin, this port is set by hardware.
STB_{OUT}($P0_4$)	Strobe pulse output	Output	This pin is used for the strobe input to the external driver IC.
$\overline{DME}$($P0_5$)	Data memory enable output	Output	This pin is used for external memory expansion.
TxD($P0_6$)	Transmission output	Output	This is an output pin for UART.
RxD($P0_7$)	Receive input	Input	This is an input pin for UART.
$P1_0$ ~ $P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port with CMOS tri-state output. It is also used as "latch input" to read data when a low level signal is inputed to $\overline{INT_1}$ pin.
$P2_0$ ~ $P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port with CMOS tri-state output. By software selection, it can also be used as an output port for the decoder logic of a stepper motor control circuit.
$P3_0$ ~ $P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port with CMOS tri-state output. The function of the $P3_0$~$P3_2$ can be selected by software.
S_{IO}($P3_2$)	Serial I/O	I/O	This pin is used as an I/O pin for serial I/O.
$P4_0/AN_0$~ $P4_3/AN_3$	Input port P4/ Analog input port AN	Input	Port P4 is a 4-bit input port, and is used as a 4-bit analog input port for A-D converter.

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When the timer X is used at event counter mode, the contents of the timer X must be read after the TXG flag is cut off. If the TXG flag is not cut off, the plural reading data of the contents of the timer X must be compared and used as real data of the timer X.
When the timer X at the other modes, other timers and prescalers are used, the contents of data can be read at optional time.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, SED, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) Notes on the stepper motor control circuit

① The shingle-shot must not be used while the horizontal or vertical counter and the phase counter are linked with timers, because they can not rewrite data.

② When the stepper motor control register is set and reset, the bit set and bit reset instructions must be used.

(7) The area of addresses $00D0_{16} \sim 00D9_{16}$ can not be used, because those area are reserved for system expansion.

(8) When the port P0 function register is set and reset, CLB, SEB, and STA instructions must be used.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors are at "off" state.	−0.3∼7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}		−0.3∼7	V
V_{REF}	Input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$ $P4_0$∼$P4_3$, AD_0∼AD_7, V_{REF}		−0.3∼V_{CC}+0.3	V
V_O	Onput voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$ AD_0∼AD_7, A_8∼A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ SYNC, ALE, WD_{OUT}, X_{OUT}		−0.3∼V_{CC}+0.3	V
P_d	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−10∼70	℃
T_{stg}	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, $f_{(X_{IN})}$ = 10MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$ (During using as a port) $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$ $P4_0$~$P4_3$, AD_0~AD_7	2.0		V_{CC}+0.3	V
V_{IH}	"H" input voltage, R_XD, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$ X_{IN}	0.8V_{CC}		V_{CC}+0.3	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$ (During using as a port) $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$ $P4_0$~$P4_3$, AD_0~AD_7	−0.3		0.8	V
V_{IL}	"L" input voltage, R_XD, CNTR $\overline{INT_1}$, $\overline{INT_2}$	−0.3		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	−0.3		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	−0.3		0.16V_{CC}	V
V_{REF}	Standard voltage input	0.5V_{CC}		V_{CC}	V
V_{IA}	Analog input voltage, $P4_0$~$P4_3$	−0.3		V_{CC}+0.3	V
$I_{OL(perk)}$	"L" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, AD_0~AD_7, A_8~A_{15} $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			5	mA
$I_{OL(avg)}$	"L" average output current (Note1), $P0_0$~$P0_7$, $P1_0$~$P1_7$ $P2_0$~$P2_7$, $P3_0$~$P3_7$ AD_0~AD_7, A_3~A_{15} $\overline{RD}$, $\overline{WR}$, ϕ, SYNC ALE, WD_{OUT}			2	mA
$I_{OH(peak)1}$	"H" peak output current, $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15} $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			−5	mA
$I_{OH(peak)2}$	"H" peak output current, $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$			−10	mA
$I_{OH(avg)1}$	"H" average output current, (Note1) $P0_0$~$P0_7$, AD_0~AD_7 A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ SYNC, ALE, WD_{OUT}			−2	mA
$I_{OH(avg)2}$	"H" average output current, (Note1) $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$			−10	mA

Note 1 : $I_{OL(avg)}$, $I_{OH(avg)}$ is the average current in 100ms.

2 : The total of $I_{OL(peak)}$, of $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE and WD_{OUT} should be 80mA max

The total of $I_{OL(peak)}$, of $P1_0$~$P1_7$, $P2_0$~$P2_7$ and $P3_0$~$P3_7$ should be 80mA max

The total of $I_{OH(peak)}$, of $P0_0$~$P0_7$, AD_0~AD_7 and A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE and WD_{OUT} should be −60mA max

The total of $I_{OH(peak)}$, of $P1_0$~$P1_7$, $P2_0$~$P2_7$ and $P3_0$~$P3_7$ should be −80mA max

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, $f_{(X_{IN})}$ = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage all output pin except X_{OUT} pin	I_{OH} = −200μA	2.4			V
		I_{OH} = −10μA	V_{CC}−0.7			
V_{OL}	"H" output voltage all output pin except X_{OUT} pin	I_{OL} = 1.6mA			0.5	V
I_I	Input leak current, P_0~$P4_3$, $\overline{RESET}$	$V_{SS} \leqq V_I \leqq V_{CC}$	−5		5	μA
I_{OZ}	Three state leak current, all input/output pin	V_{SS} + 0.5V ≦ V_O ≦ V_{CC} − 0.5V	−5		5	μA
$V_{T+}-V_{T-}$	Hysteresis width, $\overline{INT_1}$, $\overline{INT_2}$, CNTR, R_XD, $\overline{RESET}$	When used as function except port		0.6		V
I_{OH}	"H" output current, $P2_0$~$P2_7$	V_{OH} = 1.5V	−1		−10	mA
I_{CC}	Supply current	During operating (Output transistors cut-off)		7	18	mA
		Wait mode (Output transistors cut-off)		1	4	
		Stop mode (Output transistors cut-off)		1	20	μA
I_{ACC}	A-D supply current	During executing A-D conversion			6	mA

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(D-\phi)}$	Data input set-up time	Fig.1	60			ns
$t_{SU(P0-\phi)}$	Port P0 input set-up time		250			ns
$t_{SU(P1-\phi)}$	Port P1 input set-up time		250			ns
$t_{SU(P2-\phi)}$	Port P2 input set-up time		250			ns
$t_{SU(P3-\phi)}$	Port P3 input set-up time		250			ns
$t_{SU(P4-\phi)}$	Port P4 input set-up time		250			ns
$t_{SU(P1-\overline{INT_1})}$	Port P1 latch input set-up time		250			ns
$t_{SU(S_{IN}-S_{CLK})}$	Serial input set-up time		250			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{h(\phi-P0)}$	Port P0 input hold time		50			ns
$t_{h(\phi-P1)}$	Port P1 input hold time		50			ns
$t_{h(\phi-P2)}$	Port P2 input hold time		50			ns
$t_{h(\phi-P3)}$	Port P3 input hold time		50			ns
$t_{h(\phi-P4)}$	Port P4 input hold time		50			ns
$t_{h(\overline{INT_1}-P1)}$	Port P1 latch input hold time		50			nS
$t_{h(S_{CLK}-S_{IN})}$	Serial input hold time		50			ns
$t_{WL(\overline{INT_1})}$	$\overline{INT_1}$ input "L" pulse width		250			ns
$t_{WL(\overline{INT_2})}$	$\overline{INT_2}$ input "L" pulse width		1			μs
$t_{WL(CNTR)}$	CNTR input "L" pulse width		1			μs
$t_{WH(\overline{INT_1})}$	$\overline{INT_1}$ input "H" pulse width		1			μs
$t_{WH(\overline{INT_2})}$	$\overline{INT_2}$ input "H" pulse width		1			μs
$t_{WH(CNTR)}$	CNTR input "H" pulse width		1			μs
$t_{C(X_{IN})}$	External clock input cycle time		100			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width		35			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width		35			ns
$t_{W(\overline{RESET})}$	$\overline{RESET}$ input "L" pulse width		2			μs

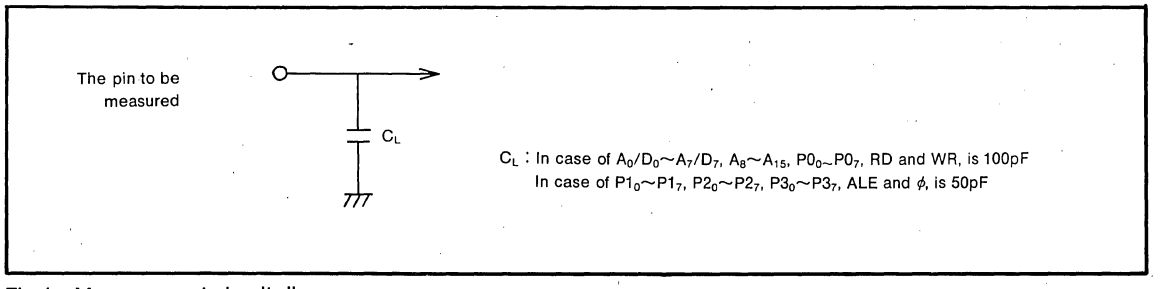


Fig.1 Measurement circuit diagram

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
※$t_{C(\phi)}$	Cycle time (Note 6)	Fig.1	400			ns
※$t_{WH(\phi)}$	ϕ clock pulse width (High level) (Note 2)		170			ns
※$t_{WL(\phi)}$	ϕ clock pulse width (Low level) (Note 2)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				30	ns
$t_{f(\phi)}$	ϕ clock falling edge time				30	ns
※$t_{d(\phi-ALE)}$	Address strobe pulse delay time (Note 4)				47.5	ns
※$t_{W(ALE)}$	Address strobe pulse width (Note 3)		75			ns
$t_{d(A-ALE)}$	Address-ALE delay time		10			ns
$t_{V(ALE-A)}$	Address effective time after ALE		30			ns
$t_{d1(\phi-A)}$	Address delay time 1				120	ns
※$t_{d2(\phi-A)}$	Address delay time 2 (Note 1)				140	ns
$t_{V(\phi-A)}$	Address effective time after ϕ		10			ns
※$t_{W(RD)}$	$\overline{RD}$, $\overline{WR}$ pulse width (Note 2)		170			ns
$t_{d(\phi-RD)}$	$\overline{RD}$, $\overline{WR}$ delay time				20	ns
$t_{V(\phi-RD)}$	$\overline{RD}$, $\overline{WR}$ effective time after ϕ				10	ns
$t_{d(AZ-RD)}$	Address floating-$\overline{RD}$ delay time		0			ns
$t_{d(\phi-D)}$	Data delay time (write cycle)				150	ns
※$t_{V(\phi-D)}$	Data effective time after ϕ (Note 5)		27			ns
$t_{d(\phi-P0)}$	Port P0 data output delay time				250	ns
$t_{d(\phi-P1)}$	Port P1 data output delay time				250	ns
$t_{d(\phi-P2)}$	Port P2 data output delay time				250	ns
$t_{d(\phi-P3)}$	Port P3 data output delay time				250	ns
$t_{d(\phi-S_{CLK})}$	Serial clock delay time				60	ns
$t_{V(\phi-S_{CLK})}$	Serial clock effective time after ϕ				40	ns
$t_{d(S_{CLK}-S_{OUT})}$	Serial output delay time				150	ns
$t_{V(S_{CLK}-S_{OUT})}$	Serial output effective time after serial clock		0			ns
$t_{d(\overline{INT_1}-BSY)}$	Busy output delay time				250	ns

※ This timing is changed by $t_C(X_{IN})$, The timing of this list is the value in $t_C(X_{IN})$ = 100ns

Note 1 : This value is defined as follows : $t_{d2(\phi-A)}=t_C(\phi)/8+77.5$ ($t_C(\phi)\geqq 500ns$)
$t_{d2(\phi-A)}=140ns$ ($400ns\leqq t_C(\phi)\leqq 500ns$)

2 : This value is defined as follows : $t_W(RD)=t_C(\phi)/2-30$

3 : This value is defined as follows : $t_W(ALE)=t_C(\phi)/4-25$

4 : This value is defined as follows : $t_d(\phi-ALE)=t_C(\phi)/8-2.5$

5 : This value is defined as follows : $t_V(\phi-D)=t_C(\phi)/8-22.5$

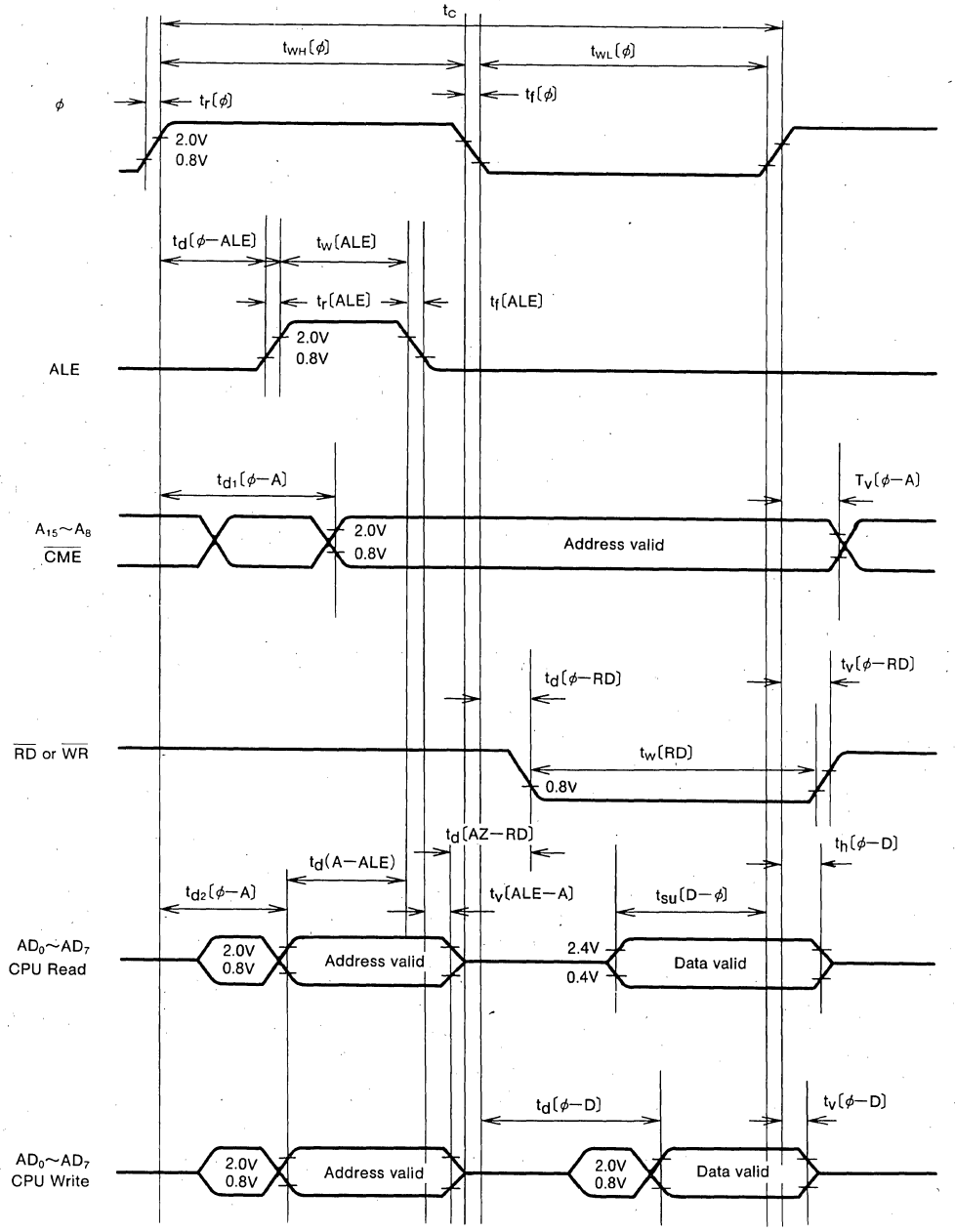
6 : This value is defined as follows : $t_C(\phi)=4t_C(X_{IN})$

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, $f_{(X_{IN})}$=10MHz, unless otherwise noded)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution		8			Bits
—	Absolute accuracy	$V_{CC}=V_{REF}$=5.12V		±1 1/2	±3	LSB
R_{LADDER}	Ladder resistance value		1			KΩ
t_{CONV}	Conversion time				36	μs
$I_{I(AD)}$	Input current in A-D convert	$0\leqq V_I\leqq V_{REF}$			50	μA

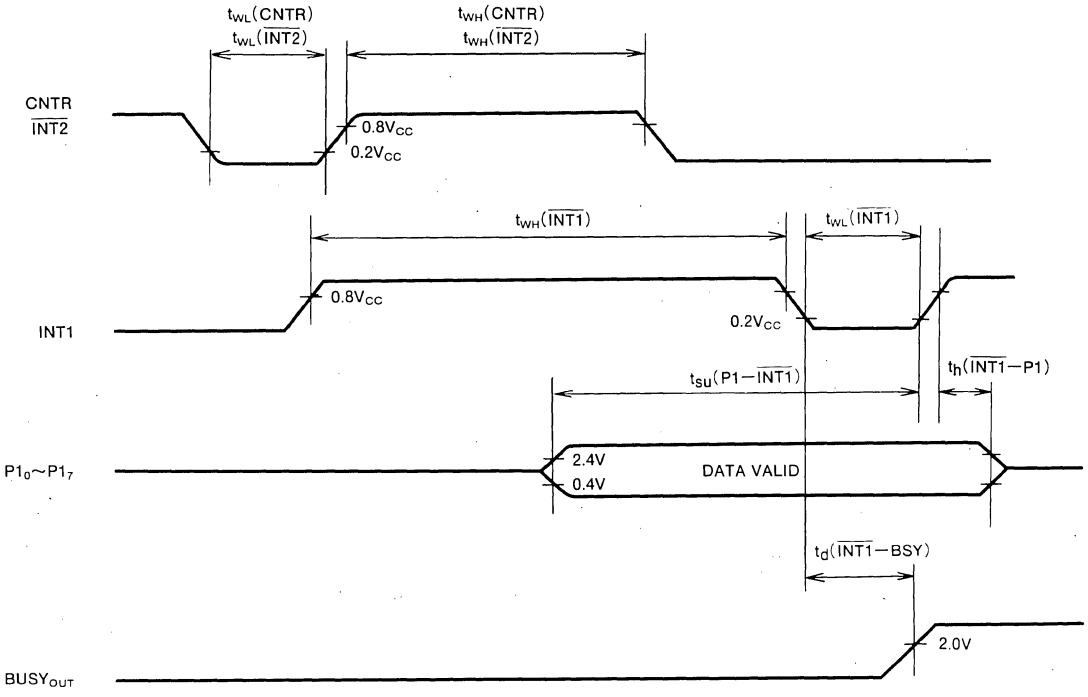
TIMING DIAGRAM

Bus timing diagram

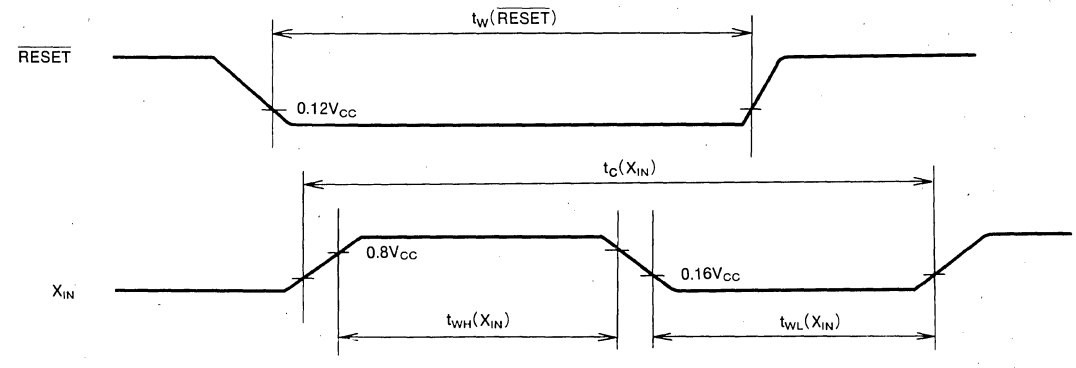


MITSUBISHI ELECTRIC

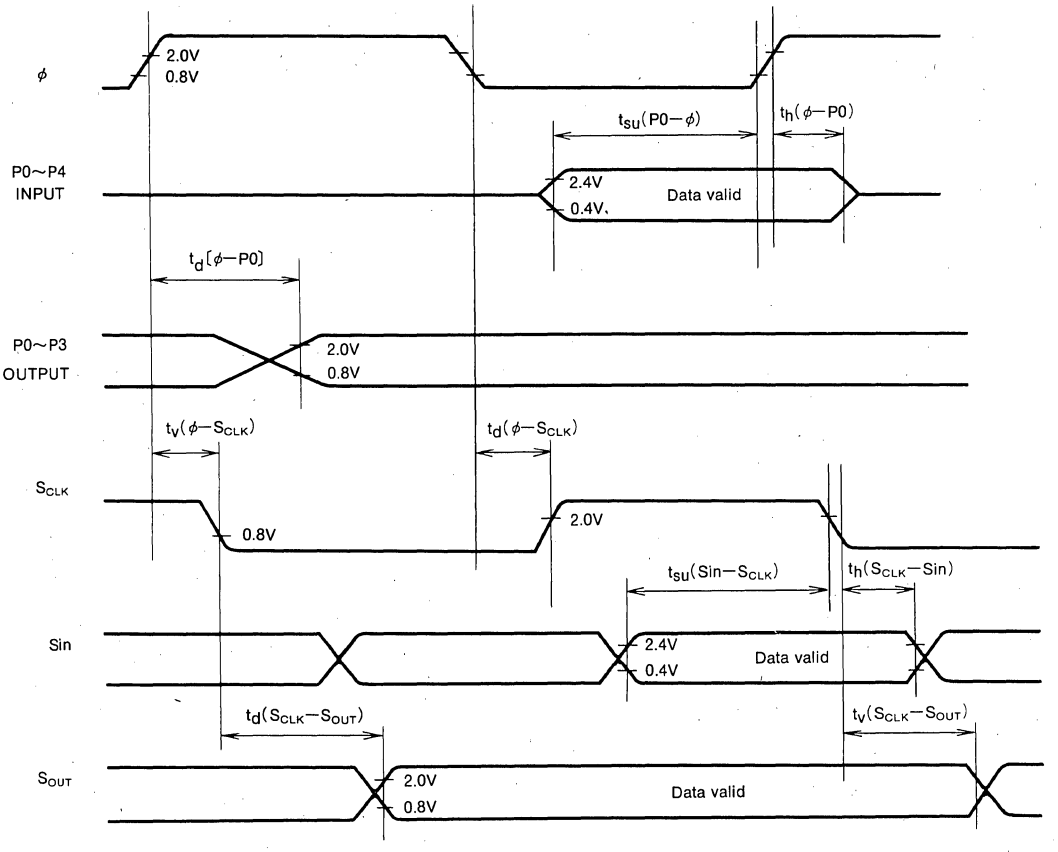
Port P1 latch input timing diagram



X_{IN}, RESET input timing diagram



Port P0~P4 input/output, serial I/O timing diagram



SERIES MELPS 740 ADDRESSING MODES

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

ADDRESSING MODES

The series MELPS 740 has 17 addressing modes and an extremely powerful memory access capability.

When extracting data required for arithmetic and logic operations from the memory or when storing the results of such operations in a memory using the appropriate instructions for this purpose, the memory address must be specified. Even when jumping to an address during a program, that particular address must be specified. The specification of the memory address is called addressing. The data required for addressing and the registers involved are now described. The series MELPS 740 instructions can be classified into three kinds, as shown in Figure 1, by the byte number in the program memory required for configuring the instruction: 1-byte, 2-byte and 3-byte instructions. In each case, the first byte is known as the "operation code" which forms the basis of the instruction. The second or third byte is called the "operand" which affects the addressing. The contents of index registers X and Y also effect the addressing.

However many the addressing modes, there is no difference in the sense that a particular memory is specified. What differs is whether the operand or the index register contents or a combination of both should be used to specify the memory or jump destination. Based on these 3 methods, the range of variation is increased and the series 740 operation is enhanced by combinations of the bit operation instructions, jump instruction and arithmetic instructions. The accumulator or register is specified with a 1-byte instruction and so there is no operand byte, which is the part specifying the memory.

Actual addressing modes are now described by type.

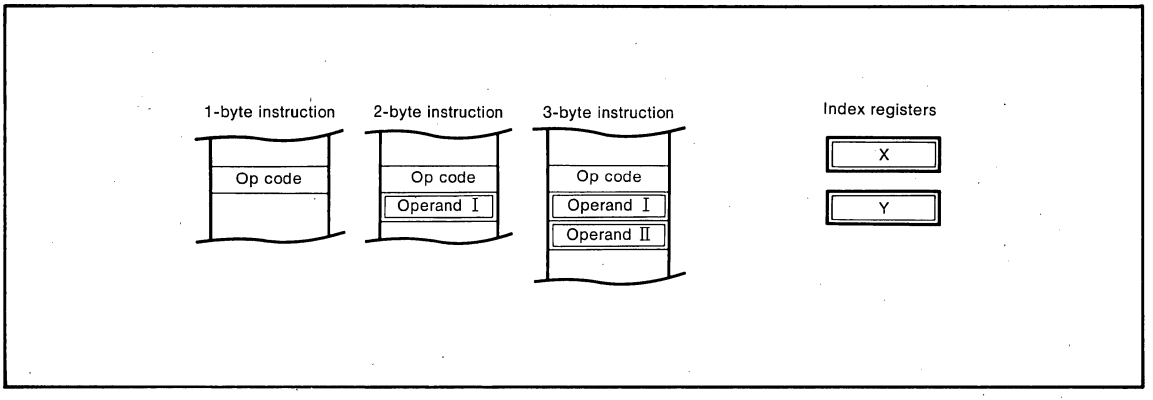
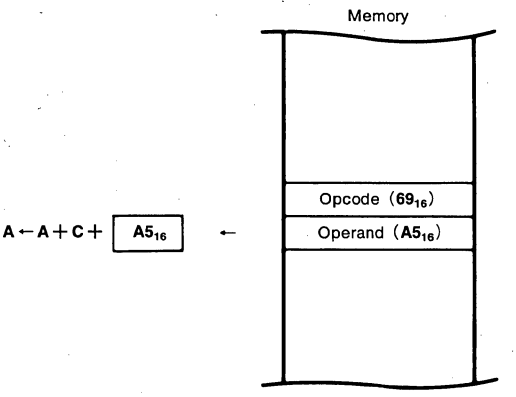


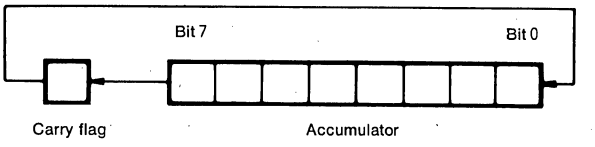
Fig.1 Instruction byte configuration

Name : Immediate addressing mode
Function : Operand follow immediate after opcode.
Instructions : **ADC, AND, CMP, CPX, CPY, EOR, LDA, LDX, LDY, ORA, SBC**
Example : Mnemonic Machine code
ADC #$A5 69_{16} $A5_{16}$

*This symbol designates the immediate addressing mode.



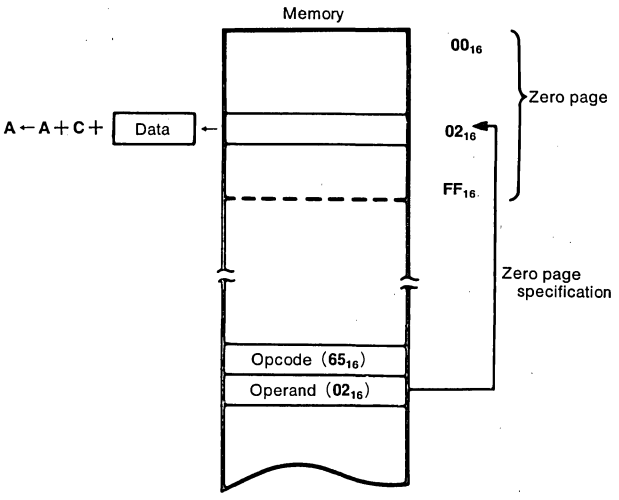
Name : Accumulator addressing mode
Function : Operation is performed on accumulator.
Instructions : **ASL, DEC, INC, LSR, ROL, ROR**
Example : Mnemonic Machine code
ROL A $2A_{16}$



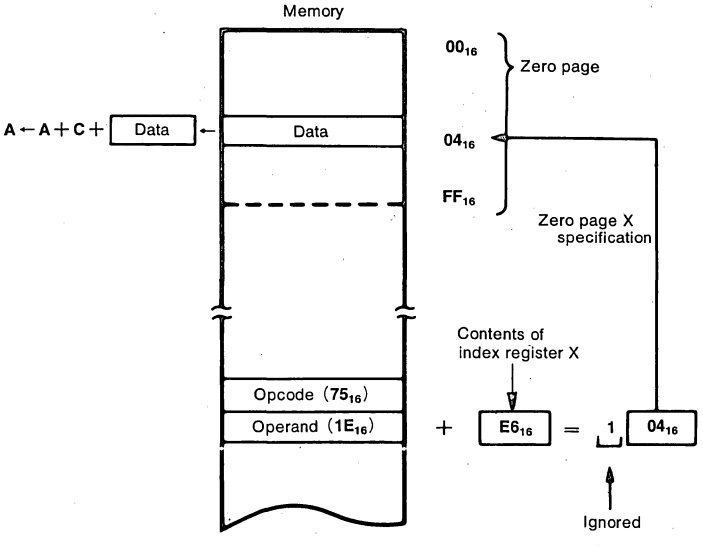
MITSUBISHI ELECTRIC

SERIES MELPS 740 ADDRESSING MODES

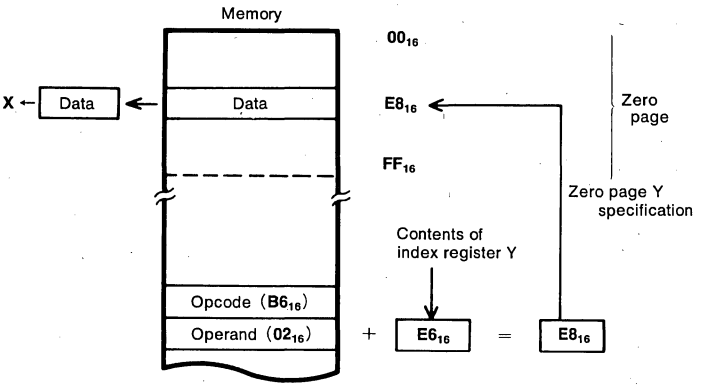
Name : Zero page addressing mode
Function : Operation is performed on the zero page memory (00_{16}~FF_{16})
Instructions : **ADC, AND, ASL, BIT, CMP, COM, CPX, CPY, DEC, EOR, INC, LDA, LDM, LDX, LDY, LSR, ORA, ROL, ROR, RRF, SBC, STA, STX, STY, TST**
Example : Mnemonic — Machine code
ADC $02 — 65_{16} 02_{16}



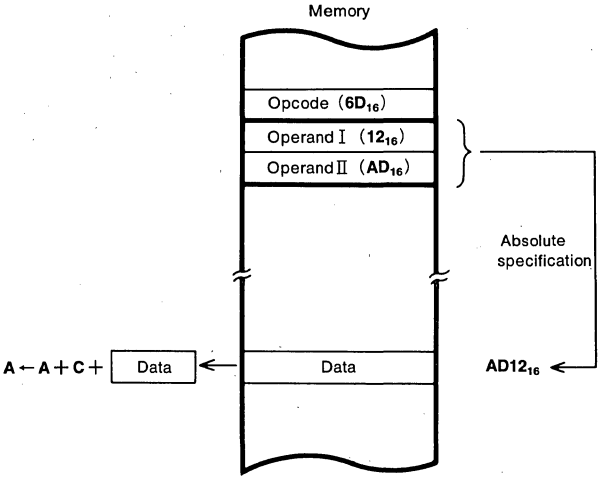
Name : Zero page X addressing mode
Function : Operation is performed on the memory which address is specified by adding the operand and contents of index register X.
Instructions : **ADC, AND, ASL, CMP, DEC, EOR, INC, LDA, LDY, LSR, ORA, ROL, ROR, SBC, STA, STY**
Example : Mnemonic — Machine code
ADC $1E,X — 75_{16} $1E_{16}$



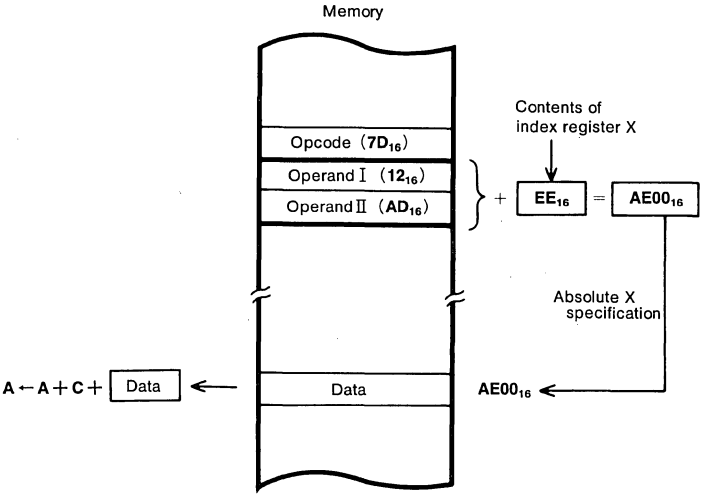
Name : Zero page Y addressing mode
Function : Operation is performed on the memory which address is specified by adding the operand and contents of index register Y.
Instructions : **LDX, STX**
Example : Mnemonic Machine code
LDX $02,Y **$B6_{16}$ 02_{16}**



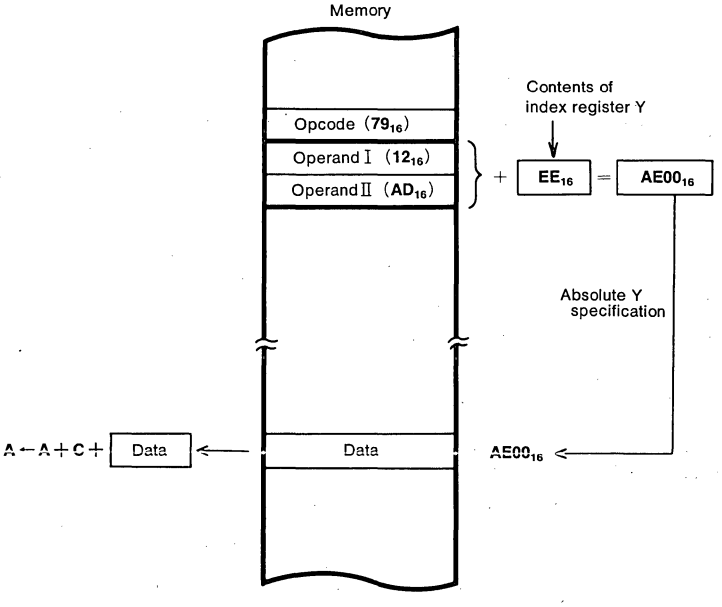
Name : Absolute addressing mode
Function : Operation is performed on the memory which address is specified by first and second operand.
Instructions : **ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, EOR, INC, JMP, JSR, LDA, LDX, LDY, LSR, ORA, ROL, ROR, SBC, STA, STX, STY**
Example : Mnemonic Machine code
ADC $AD12 **$6D_{16}$ 12_{16} AD_{16}**



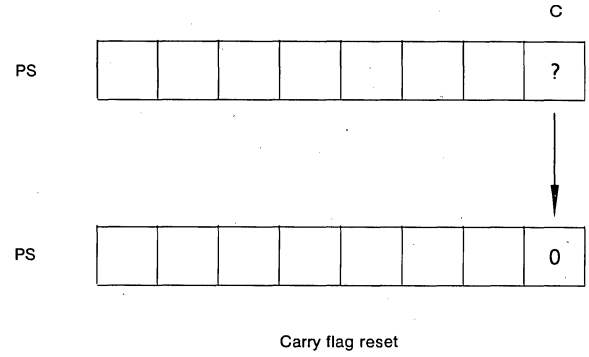
Name : Absolute X addressing mode
Function : Operation is performed on the memory which address is specified by adding the contents of index register X and value indicated first and second operand.
Instructions : **ADC, AND, ASL, CMP, DEC, EOR, INC, LDA, LDY, LSR, ORA, ROL, ROR, SBC, STA**
Example : Mnemonic Machine code
ADC $AD12,X $7D_{16}$ 12_{16} AD_{16}



Name : Absolute Y addressing mode
Function : Operation is performed on the memory which address is specified by adding the contents of index register Y and value indicated first and second operand.
Instructions : **ADC, AND, CMP, EOR, LDA, LDX, ORA, SBC, STA**
Example : Mnemonic Machine code
ADC $AD12,Y 79_{16} 12_{16} AD_{16}



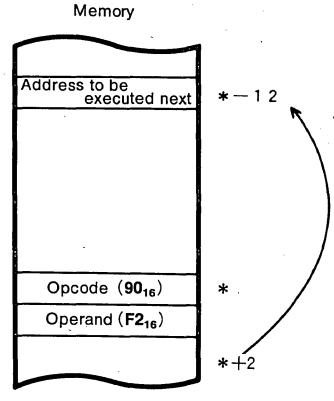
Name : Implied addressing mode
Function : Implied addressing mode need no operand.
Instructions : **BRK, CLC, CLD, CLI, CLT, CLV, DEX, DEY, FST, INX, INY, NOP, PHA, PHP, PLA, PLP, RTI, RTS, SEC, SED, SEI, SET, SLW, STP, TAX, TAY, TSX, TXA, TXS, TYA, WIT**
Example : Mnemonic Machine code
CLC 18_{16}



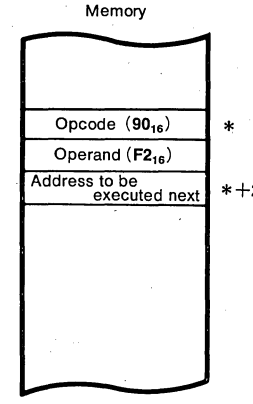
Carry flag reset

Name : Relative addressing mode
Function : Jumps to address which is produced by adding the contents of program counter and the contents of operand.
Instructions : **BCC, BCS, BEQ, BMI, BNE, BPL, BRA, BVC, BVS**
Example : Mnemonic Machine code
BCC ＊−12 90_{16} $F2_{16}$

Jumps to ＊−12 address when carry flag(c) is cleared.

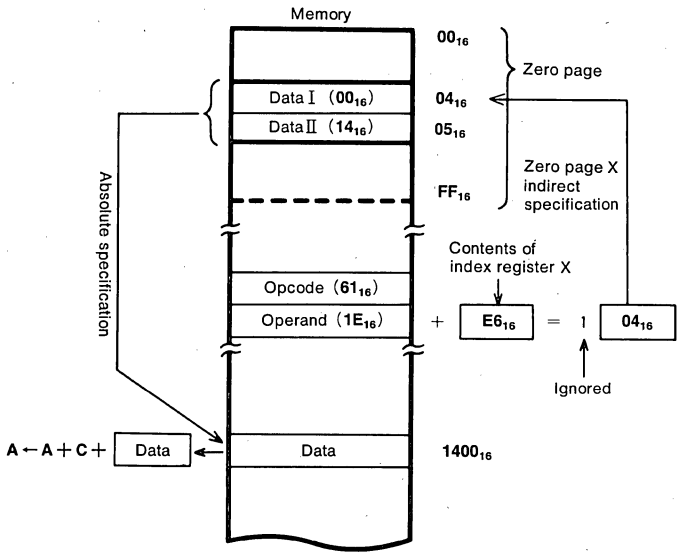


Proceed to next address when carry flag(c) is set.



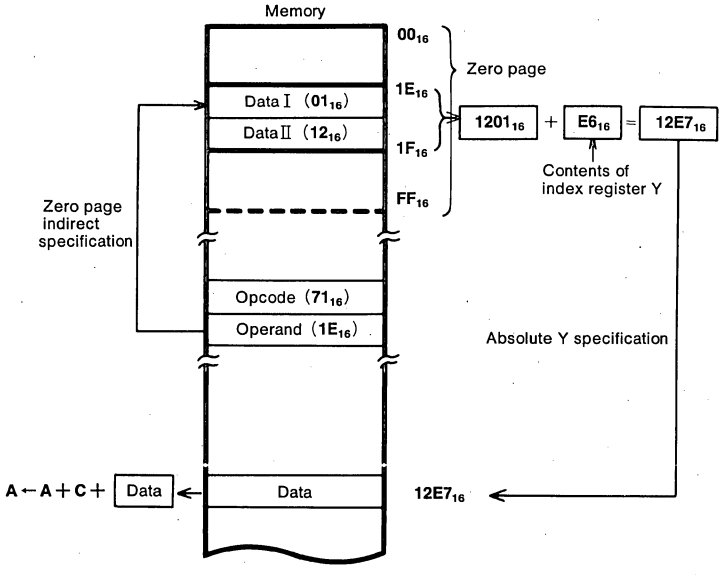
MITSUBISHI ELECTRIC

Name : Indirect X addressing mode
Function : Operation is performed on the memory at address indicated by contents of consecutive 2 byte memory which first address is formed by adding operand and contents of index register X.
Instructions : **ADC, AND, CMP, EOR, LDA, ORA, SBC, STA**
Example : Mnemonic Machine code
ADC ($1E,X) 61_{16} $1E_{16}$



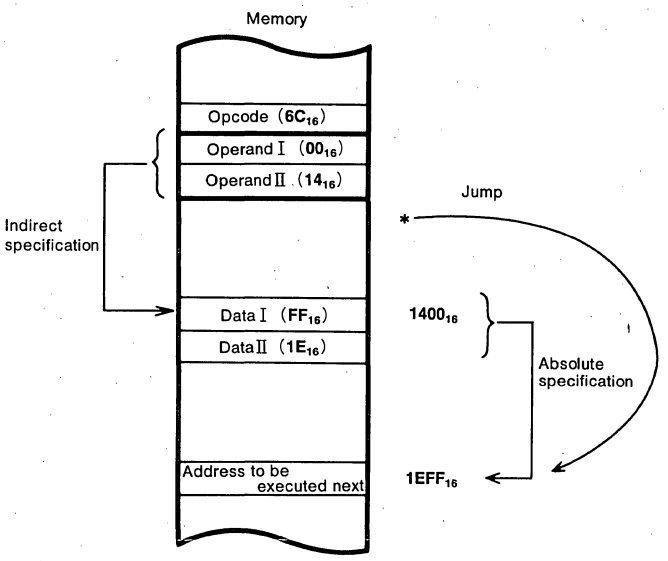
In this example, 00_{16} as data I and 14_{16} as data II have been stored beforehand.

Name : Indirect Y addressing mode
Function : Operation is performed on the memory addressed by adding the contents of index register Y and contents of consecutive 2 byte zero page memory which first address is specified by operand.
Instructions : **ADC, AND, CMP, EOR, LDA, ORA, SBC, STA**
Example : Mnemonic Machine code
ADC ($1E),Y 71_{16} $1E_{16}$



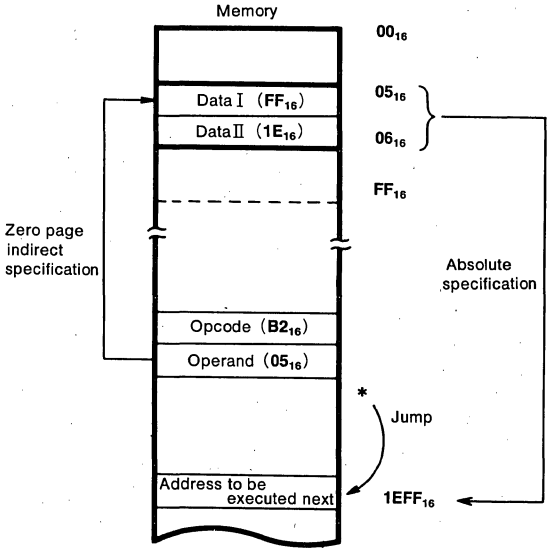
In this example, 00_{16} as data I and 12_{16} as Data II have been stored beforehand.

Name : Indirect absolute addressing mode
Function : Specifies consecutive 2-byte memories by contents of first and second operand and jumps to address indicated by contents of these memories.
Instructions : **JMP**
Example : Mnemonic — Machine code
JMP ($1400) — **$6C_{16}$ 00_{16} 14_{16}**



In this example, FF_{16} as data I and $1E_{16}$ as data II have been stored beforehand.

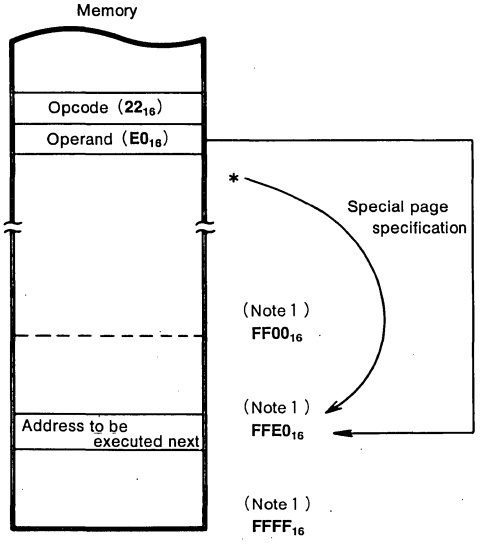
Name : Zero page indirect absolute addressing mode
Function : Specifies consecutive 2-byte memories in zero page area by operand contents and jumps to adddress indicated by contents of these memories.
Instructions : **JMP, JSR**
Example : Mnemonic — Machine code
JMP ($05) — **$B2_{16}$ 05_{16}**



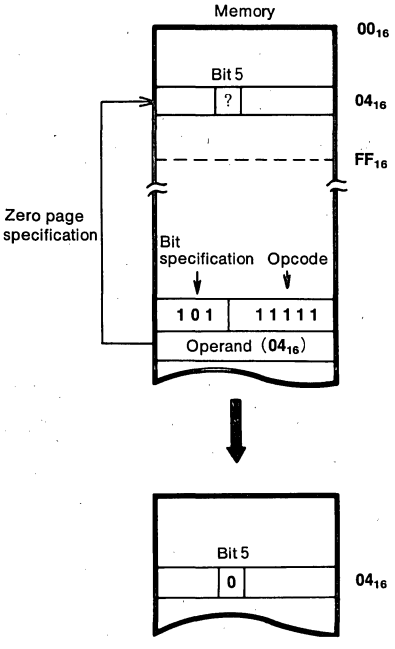
In this example, FF_{16} as data I and $1E_{16}$ as data II have been stored beforehand.

Name : Special page addressing mode
Function : Jumps to address in special page area. 8 high-order address and 8 low-order address of jump distination is $1F_{16}$ and contents of operand respectively.
Instruction : **JSR**
Example : Mnemonic Machine code
JSR \$1FE0 **22_{16} $E0_{16}$**
↑
*This symbol denotes special page mode.

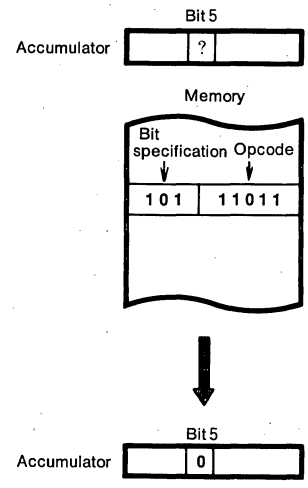
Note 1 The higher byte address is $1F_{16}$ for M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP and M50758-XXXSP, and is $3F_{16}$ for M50930-XXXFP, M50931-XXXFP, M50932-XXXFP, M37410M3-XXXFP and M37410M4-XXXFP.



Name : Zero page bit addressing mode
Function : Operation is performed on the bit specified by 3 high-order bits of opcode, memory address containing this bit is specified by operand.
Instructions : **CLB, SEB**
Example : Mnemonic Machine code
CLB 5,\$04 **BF_{16} 04_{16}**

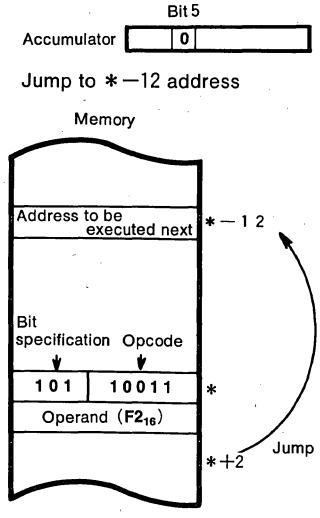


Name : Accumulator bit addressing mode
Function : Specifies bit in accumulator by 3 high-order bits of opcode.
Instructions : **CLB, SEB**
Example : Mnemonic Machine code
CLB 5,A **BB_{16}**

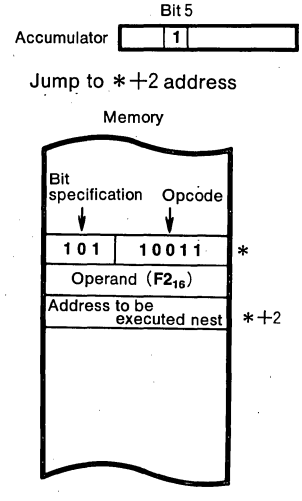


Name : Accumulator bit relative addressing mode
Function : The location of the accumulator bit is specified with the 3 high-order bits of the opcode and, depending on the state of this bit, a jump is mode to the address indicated by the value produced by adding the operand contents to that of the program counter.
Instructions : **BBC, BBS**
Example : Mnemonic Machine code
BBC 5,A,*−12 **$B3_{16}$ $F2_{16}$**

When accumulator bit 5 is cleared



When accumulator bit 5 is set



Name : Zero page bit relative addressing mode

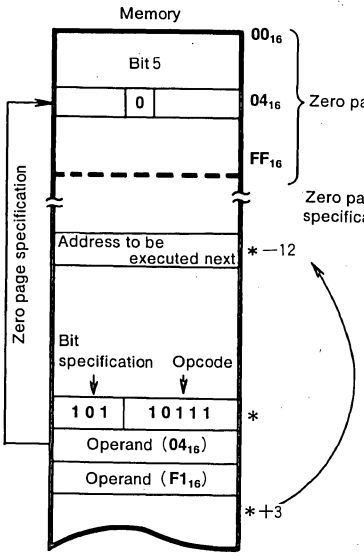
Function : Operation is performed on the bit specified by 3 high-order bits of opcode, memory address containing this bit is specified by first operand and, depending on the state of this special bit, jumps to the address indicated by the value produced by adding the second operand contents to the contents of the program counter.

Instructions : **BBC, BBS**

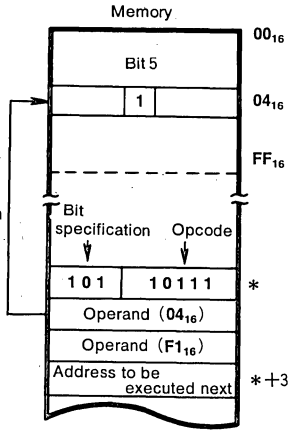
Example : Mnemonic — Machine code

BBC 5,$04,*−12 — **$B7_{16}$ 04_{16} $F1_{16}$**

Jump to * − 12 address when 04_{16} address bit 5 is cleared.



Advance to * +3 address when 04_{16} address bit 5 is set.



MACHINE INSTRUCTIONS

Symbol	Function	Details	Addressing mode																
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#
ADC (Note 1) (Note 9)	When T=0 A←A+M+C When T=1 M(X)←M(X)+M+C	Adds the carry, accumulator and memory contents. The results are entered into the accumulator. Adds the contents of the memory in the address indicated by index register X, the contents of the memory specified by the addressing modes in the columns on the right, and the contents of the carry. The results are entered into the memory at the address indicated by index register X.				69	2	2							65	3	2			
AND (Note 1)	When T=0 A←A∧M When T=1 M(X)←M(X)∧M	"AND-s" the accumulator and memory contents. The results are entered into the accumulator. "AND-s" the contents of the memory of the address indicated by index register X and the contents of the memory specified by the addressing modes in the columns on the right. The results are entered into the memory at the address indicated by index register X.				29	2	2							25	3	2			
ASL	7 0 C ← □ ←0	1-bit shifts the contents of accumulator or contents of memory to the left. "0" enters 0th bit of memory or accumulator and the contents of the 7th bit enter carry flag.							0A	2	1				06	5	2			
BBC (Note 4)	A_b or M_b=0?	Branches when the contents of the bit specified in the accumulator or memory are "0".										13+2i	4	2				17+2i	5	3
BBS (Note 4)	A_b or M_b=1?	Branches when the contents of the bit specified in the accumulator or memory are "1".										03+2i	4	2				07+2i	5	3
BCC (Note 4)	C=0?	Branches when the contents of carry flag are "0".																		
BCS (Note 4)	C=1?	Branches when the contents of carry flag are "1".																		
BEQ (Note 4)	Z=1?	Branches when the contents of zero flag are "1".																		
BIT	A∧M	"AND-s" the contents of accumulator and memory. The results are not entered anywhere.													24	3	2			
BMI (Note 4)	N=1?	Branches when the contents of negative flag are "1".																		
BNE (Note 4)	Z=0?	Branches when the contents of zero flag are "0".																		
BPL (Note 4)	N=0?	Branches when the contents of negative flag are "0".																		
BRA	PC←PC±offset	Jumps to address where offset has been added to the program counter.																		
BRK	B←1 $M(S)←PC_H$ S←S−1 $M(S)←PC_L$ S←S−1 M(S)←PS S←S−1 $PC_L←AD_L$ $PC_H←AD_H$	Executes software interrupt.	00	7	1															

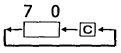
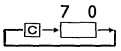
Addressing mode																													Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	N	V	T	B	D	I	Z	C
75	4	2				6D	4	3	7D	5	3	79	5	3							61	6	2	71	6	2							N	V	•	•	•	•	Z	C
35	4	2				2D	4	3	3D	5	3	39	5	3							21	6	2	31	6	2							N	•	•	•	•	•	Z	•
16	6	2				0E	6	3	1E	7	3																						N	•	•	•	•	•	Z	C
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
																											90	2	2				•	•	•	•	•	•	•	•
																											B0	2	2				•	•	•	•	•	•	•	•
																											F0	2	2				•	•	•	•	•	•	•	•
						2C	4	3																										M_7	M_6	•	•	•	•	Z	•
																											30	2	2				•	•	•	•	•	•	•	•
																											D0	2	2				•	•	•	•	•	•	•	•
																											10	2	2				•	•	•	•	•	•	•	•
																											80	4	2				•	•	•	•	•	•	•	•
																																	•	•	•	1	•	1	•	•

Symbol	Function	Details	Addressing mode															
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
BVC (Note 4)	V=0?	Branches when the contents of overflow flag are "0."																		
BVS (Note 4)	V=1?	Branches when the contents of overflow flag are "1."																		
CLB	A_b or M_b←0	Clears the contents of the bit specified in the accumulator or memory to "0."										1B+2i	2	1				1F+2i	5	2
CLC	C←0	Clears the contents of the carry flag to "0."	18	2	1															
CLD	D←0	Clears the contents of decimal mode flag to "0."	D8	2	1															
CLI	I←0	Clears the contents of interrupt disable flag to "0."	58	2	1															
CLT	T←0	Clears the contents of X-modified arithmetic mode flag to "0."	12	2	1															
CLV	V←0	Clears the contents overflow flag to "0."	B8	2	1															
CMP (Note 3)	When T=0 A−M When T=1 M(X)−M	Compares the contents of accumulator and memory. Compares the contents of the memory specified by addressing modes in the columns on the right with the contents of the address indicated by index register X.				C9	2	2							C5	3	2			
COM	M←$\overline{M}$	Formes one's complement of contents of memory, and store it into memory.													44	5	2			
CPX	X−M	Compares the contents of index register X and memory.				E0	2	2							E4	3	2			
CPY	Y−M	Compares the contents of index register Y and memory.				C0	2	2							C4	3	2			
DEC	A←A−1 or M←M−1	Decrements the contents of accumulator or memory by 1.							1A	2	1				C6	5	2			
DEX	X←X−1	Decrements the contents of index register X by 1.	CA	2	1															
DEY	Y←Y−1	Decrements the contents of index register Y by 1.	88	2	1															
DIV (Note 8)	A←(M(zz+X+1), M(zz+X))/A M(S) ← 1's complement of Remainder S←S− 1	Divides by accumulator the 16-bit data that is the contents of M(zz+x+1) for high byte and the contents of the next address memory for low byte, and stores the quotient in the accumulator and the remainder on the stack as 1's complement.																		
EOR (Note 1)	When T=0 A←A∀M When T=1 M(X)←M(X)∀M	"Exclusive-ORs" the contents of accumulator and memory. The results are stored into the accumulator. "Exclusive-ORs" the contents of the memory specified by the addressing modes in the columns on the right and the contents of the memory at the address indicated by index register X. The results are stored into the memory at the address indicated by index register X.				49	2	2							45	3	2			
FST (Note 5)		Connects oscillator output to X_{OUTF}.	E2	2	1															
INC	A←A+1 or M←M+1	Increments the contents of accumulator or memory by 1.							3A	2	1				E6	5	2			
INX	X←X+1	Increments the contents of index register X by 1.	E8	2	1															
INY	Y←Y+1	Increments the contents of index register Y by 1.	C8	2	1															

Addressing mode																														Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
																											50	2	2				•	•	•	•	•	•	•	•
																											70	2	2				•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	0
																																	•	•	•	•	0	•	•	•
																																	•	•	•	•	•	0	•	•
																																	•	•	0	•	•	•	•	•
																																	•	0	•	•	•	•	•	•
D5	4	2				CD	4	3	DD	5	3	D9	5	3							C1	6	2	D1	6	2							N	•	•	•	•	Z	C
																																	N	•	•	•	•	Z	•
						EC	4	3																									N	•	•	•	•	Z	C
						CC	4	3																									N	•	•	•	•	Z	C
D6	6	2				CE	6	3	DE	7	3																						N	•	•	•	•	Z	•
																																	N	•	•	•	•	Z	•
																																	N	•	•	•	•	Z	•
E2	16	2																															•	•	•	•	•	•	•	•
55	4	2				4D	4	3	5D	5	3	59	5	3							41	6	2	51	6	2							N	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•
F6	6	2				EE	6	3	FE	7	3																						N	•	•	•	•	Z	•
																																	N	•	•	•	•	Z	•
																																	N	•	•	•	•	Z	•

Symbol	Function	Details	Addressing mode																
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#
JMP	If addressing mode is ABS $PC_L \leftarrow AD_L$ $PC_H \leftarrow AD_H$ If addressing mode is IND $PC_L \leftarrow (AD_H, AD_L)$ $PC_H \leftarrow (AD_H, AD_L+1)$ If addressing mode is ZP, IND $PC_L \leftarrow (00, AD_L)$ $PC_H \leftarrow (00, AD_L+1)$	Jumps to new address.																		
JSR	$M(S) \leftarrow PC_H$ $S \leftarrow S-1$ $M(S) \leftarrow PC_L$ $S \leftarrow S-1$ After executing the above, if addressing mode is ABS, $PC_L \leftarrow AD_L$ $PC_H \leftarrow AD_H$ If addressing mode is SP, $PC_L \leftarrow AD_L$ $PC_H \leftarrow FF$ If addressing mode is ZP, IND, $PC_L \leftarrow (00, AD_L)$ $PC_H \leftarrow (00, AD_L+1)$	After storing contents of program counter in stack, and jumps to new address.																		
LDA (Note 2)	When T=0 A←M When T=1 M(X)←M	Load accumulator with contents of memory. Load memory indicated by index register X with contents of memory specified by addressing mode shown in right column.				A9	2	2							A5	3	2			
LDM	M←IMM	Load memory with immediate value.													3C	4	3			
LDX	X←M	Load index register X with contents of memory.				A2	2	2							A6	3	2			
LDY	Y←M	Load index register Y with contents of memory.				A0	2	2							A4	3	2			
LSR	7 0 0 → □ → C	Shift the contents of accumulator or memory to the right by one bit. 0th bit of accumulator or memory is stored in carry, 7th bit is cleared.							4A	2	1				46	5	2			
MUL (Note 8)	M(S)·A←AXM(zz+X) S←S− 1	Multiplies accumulator with the memory specified by the zero page X addrressing mode and stores the high byte of the result on the stack and the low byte in the accumulator.																		
NOP	PC←PC+1	No operation.	EA	2	1															
ORA (Note 1)	When T=0 A←AVM When T=1 M(X)←M(X)VM	Produce the logical OR of the contents of memory and accumulator. The result is stored in accumulator. produce the logical OR of contents of memory indicated by index register X and contents of memory specified by addressing mode shown in right column. The result is stored in memory of address specified by index register X.				09	2	2							05	3	2			

Addressing mode																												Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
						4C	3	3							6C	5	3	B2	4	2												•	•	•	•	•	•	•	•
						20	6	3										02	7	2										22	5	2	•	•	•	•	•	•	•	•
B5	4	2				AD	4	3	BD	5	3	B9	5	3							A1	6	2	B1	6	2							N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•
			B6	4	2	AE	4	3				BE	5	3																			N	•	•	•	•	•	Z	•
B4	4	2				AC	4	3	BC	5	3																						N	•	•	•	•	•	Z	•
56	6	2				4E	6	3	5E	7	3																						0	•	•	•	•	•	Z	C
62	15	2																															•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
15	4	2				0D	4	3	1D	5	3	19	5	3							01	6	2	11	6	2							N	•	•	•	•	•	Z	•

Symbol	Function	Details	Addressing mode																
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#
PHA	M(S)←A S←S−1	Saves the contents of the accumulator in the memory at the address indicated by the stack pointer and decrements the contents of stack pointer by 1.	48	3	1														
PHP	M(S)←PS S←S−1	Saves the contents of processor status register in the memory at the address indicated by the stack pointer and decrements the contents of stack pointer by 1.	08	3	1														
PLA	S←S+1 A←M(S)	Increments the contents of stack pointer by 1 and pulls from the memory at the address indicated by the stack pointer, and store it in accumulator.	68	4	1														
PLP	S←S+1 PS←M(S)	Increments the contents of stack pointer by 1 and pulls from the memory at the address indicated by the stack pointer, and store it in processor status register.	28	4	1														
ROL		Connects the carry flag and the accumulator or memory and rotates the contents to the left by 1 bit.							2A	2	1				26	5	2		
ROR		Connects the carry flag and the accumulator or memory and rotates the contents to the right by 1 bit.							6A	2	1				66	5	2		
RRF		Rotates the contents of memory to the right by 4 bits.													82	8	2		
RTI	S←S+1 PS←M(S) S←S+1 PC_L←M(S) S←S+1 PC_H←M(S)	Returns from the interrupt routine to the main routine.	40	6	1														
RTS	S←S+1 PC_L←M(S) S←S+1 PC_H←M(S)	Returns from the subroutine to the main routine.	60	6	1														
SBC (Note 1) (Note 9)	When T=0 A←A−M−C When T=1 M(X)←M(X)−M−C	Subtracts the contents of memory and carry flag from the contents of accumulator. The results are stored into the accumulator. Subtracts contents of carry flag and contents of the memory indicated by the addressing modes shown in the columns on the right from the memory at the address indicated by index register X. The results are stored into the memory of the address indicated by index register X.				E9	2	2							E5	3	2		
SEB	A_b or M_b←1	Sets the specified bit contents of accumulator or memory to "1."										0B+2i	2	1				0F+2i	5	2
SEC	C←1	Sets the contents of carry flag to "1."	38	2	1														
SED	D←1	Sets the contents of decimal mode flag to "1."	F8	2	1														
SEI	I←1	Sets the contents of interrupt disable flag to "1."	78	2	1														
SET	T←1	Sets the contents of X-modified arithmetic mode flag to "1."	32	2	1														
SLW (Note 5)		Releases the connection between the oscillator output and pin X_{OUT}.	C2	2	1														

Addressing mode																														Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
																																	N	•	•	•	•	•	Z	•
																																	(Value saved in stack)							
36	6	2				2E	6	3	3E	7	3																						N	•	•	•	•	•	Z	C
76	6	2				6E	6	3	7E	7	3																						N	•	•	•	•	•	Z	C
																																	•	•	•	•	•	•	•	•
																																	(Value saved in stack)							
																																	•	•	•	•	•	•	•	•
F5	4	2				ED	4	3	FD	5	3	F9	5	3							E1	6	2	F1	6	2							N	V	•	•	•	•	Z	C
																																	•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	1
																																	•	•	•	•	1	•	•	•
																																	•	•	•	•	•	1	•	•
																																	•	•	1	•	•	•	•	•
																																	•	•	•	•	•	•	•	•

Symbol	Function	Details	Addressing mode																	
			IMP			IMM			A			BIT,A			ZP			BIT,ZP		
			0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#	0P	n	#
STA	M←A	Stores the contents of accumulator in the memory.													85	4	2			
STP (Note 7)		Stops the oscillation of the oscillator.	42	2	1															
STX	M←X	Stores the contents of index register X in the memory.													86	4	2			
STY	M←Y	Stores the contents of index register Y in the memory.													84	4	2			
TAX	X←A	Transfers the contents of accumulator to index register X.	AA	2	1															
TAY	Y←A	Transfers the contents of accumulator to index register Y.	A8	2	1															
TST	M=0?	Tests whether the contents of memory are "0" or not.													64	3	2			
TSX	X←S	Transfers the contents of stack pointer to index register X.	BA	2	1															
TXA	A←X	Transfers the contents of index register X to the accumulator.	8A	2	1															
TXS	S←X	Transfers the contents of index register X to the stack pointer.	9A	2	1															
TYA	A←Y	Transfers the contents of index register Y to the accumulator.	98	2	1															
WIT (Note 6)		Stops the internal clock.	C2	2	1															

Note 1 : The number of cycles "n" is added by 3 when T is 1.
2 : The number of cycles "n" is added by 2 when T is 1.
3 : The number of cycles "n" is added by 1 when T is 1.
4 : The number of cycles "n" is added by 2 when branching has occurred.
5 : This instruction is not for any other models than M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP and M50758-XXXSP.
6 : This instruction is not provided for M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP, and M50758-XXXSP.
7 : This instruction is not provided for M50752-XXXSP, M50757-XXXSP and M50758-XXXSP.
8 : This instruction is not for any other models than M37450M2-XXXSP, M37450M4-XXXSP, M37450M8-XXXSP, M37450S1SP, M37450S2SP and M37450S4SP.
9 : N, V and Z flags are invalid at decimal operation mode.

Addressing mode																																Processor status register							
ZP,X			ZP,Y			ABS			ABS,X			ABS,Y			IND			ZP,IND			IND,X			IND,Y			REL			SP			7	6	5	4	3	2	1	0
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	N	V	T	B	D	I	Z	C
95	5	2				8D	5	3	9D	6	3	99	6	3							81	7	2	91	7	2							•	•	•	•	•	•	•	•
																																	•	•	•	•	•	•	•	•
			96	5	2	8E	5	3																									•	•	•	•	•	•	•	•
94	5	2				8C	5	3																									•	•	•	•	•	•	•	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•
																																	N	•	•	•	•	•	Z	•
																																	•	•	•	•	•	•	•	•

Symbol	Contents
IMP	Implied addressing mode
IMM	Immediate addressing mode
A	Accumulator or Accumulator addressing mode
BIT, A	Accumulator bit relative addressing mode
ZP	Zero page addressing mode
BIT, ZP	Zero page bit relative addressing mode
ZP, X	Zero page X addressing mode
ZP, Y	Zero page Y addressing mode
ABS	Absolute addressing mode
ABS, X	Absolute X addressing mode
ABS, Y	Absolute Y addressing mode
IND	Indirect absolute addressing mode
ZP, IND	Zero page indirect absolute addressing mode
IND, X	Indirect X addressing mode
IND, Y	Indirect Y addressing mode
REL	Relative addressing mode
SP	Special page addressing mode
C	Carry flag
Z	Zero flag
I	Interrupt disable flag
D	Decimal mode flag
B	Break flag
T	X-modified arithmetic mode flag
V	Overflow flag
N	Negative flag

Symbol	Contents
+	Addition
−	Subtraction
∧	Logical OR
∨	Logical AND
∀	Logical exclusive OR
—	Negation
←	Shows direction of data flow
X	Index register X
Y	Index register Y
S	Stack pointer
PC	Program counter
PS	Processor status register
PC_H	8 high-order bits of program counter
PC_L	8 low-order bits of program counter
AD_H	8 high-order bits of address
AD_L	8 low-order bits of address
(AD_H, AD_L)	Contents of memory at address indicated by AD_H and AD_L, in AD_H is 8 high-order bits and AD_L is 8 low-order bits.
(00, AD_L)	Contents of address indicated by zero page AD_L
FF	FF in Hexadecimal notation
M	Memory specified by address designation of any addressing mode
M (X)	Memory of address indicated by contents of index register X
M (S)	Memory of address indicated by contents of stack pointer
A_b	1 bit of accumulator
M_b	1 bit of memory
OP	Opcode
n	Number of cycles
#	Number of bytes

SERIES MELPS 740 LIST OF INSTRUCTION CODES

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

LIST OF INSTRUCTION CODES

D_7~D_4 \ D_3~D_0 (Hexadecimal notation)		0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	BRK	ORA IND, X	JSR ZP, IND	BBS 0, A	—	ORA ZP	ASL ZP	BBS 0, ZP	PHP	ORA IMM	ASL A	SEB 0, A	—	ORA ABS	ASL ABS	SEB 0, ZP
0001	1	BPL	ORA IND, Y	CLT	BBC 0, A	—	ORA ZP, X	ASL ZP, X	BBC 0, ZP	CLC	ORA ABS, Y	DEC A	CLB 0, A	—	ORA ABS, X	ASL ABS, X	CLB 0, ZP
0010	2	JSR ABS	AND IND, X	JSR SP	BBS 1, A	BIT ZP	AND ZP	ROL ZP	BBS 1, ZP	PLP	AND IMM	ROL A	SEB 1, A	BIT ABS	AND ABS	ROL ABS	SEB 1, ZP
0011	3	BMI	AND IND, Y	SET	BBC 1, A	—	AND ZP, X	ROL ZP, X	BBC 1, ZP	SEC	AND ABS, Y	INC A	CLB 1, A	LDM ZP	AND ABS, X	ROL ABS, X	CLB 1, ZP
0100	4	RTI	EOR IND, X	STP (Note4)	BBS 2, A	COM ZP	EOR ZP	LSR ZP	BBS 2, ZP	PHA	EOR IMM	LSR A	SEB 2, A	JMP ABS	EOR ABS	LSR ABS	SEB 2, ZP
0101	5	BVC	EOR IND, Y	—	BBC 2, A	—	EOR ZP, X	LSR ZP, X	BBC 2, ZP	CLI	EOR ABS, Y	—	CLB 2, A	—	EOR ABS, X	LSR ABS, X	CLB 2, ZP
0110	6	RTS	ADC IND, X	MUL (Note3)	BBS 3, A	TST ZP	ADC ZP	ROR ZP	BBS 3, ZP	PLA	ADC IMM	ROR A	SEB 3, A	JMP IND	ADC ABS	ROR ABS	SEB 3, ZP
0111	7	BVS	ADC IND, Y	—	BBC 3, A	—	ADC ZP, X	ROR ZP, X	BBC 3, ZP	SEI	ADC ABS, Y	—	CLB 3, A	—	ADC ABS, X	ROR ABS, X	CLB 3, ZP
1000	8	BRA	STA IND, X	RRF ZP	BBS 4, A	STY ZP	STA ZP	STX ZP	BBS 4, ZP	DEY	—	TXA	SEB 4, A	STY ABS	STA ABS	STX ABS	SEB 4, ZP
1001	9	BCC	STA IND, Y	—	BBC 4, A	STY ZP, X	STA ZP, X	STX ZP, Y	BBC 4, ZP	TYA	STA ABS, Y	TXS	CLB 4, A	—	STA ABS, X	—	CLB 4, ZP
1010	A	LDY IMM	LDA IND, X	LDX IMM	BBS 5, A	LDY ZP	LDA ZP	LDX ZP	BBS 5, ZP	TAY	LDA IMM	TAX	SEB 5, A	LDY ABS	LDA ABS	LDX ABS	SEB 5, ZP
1011	B	BCS	LDA IND, Y	JMP ZP, IND	BBC 5, A	LDY ZP, X	LDA ZP, X	LDX ZP, Y	BBC 5, ZP	CLV	LDA ABS, Y	TSX	CLB 5, A	LDY ABS, X	LDA ABS, X	LDX ABS, Y	CLB 5, ZP
1100	C	CPY IMM	CMP IND, X	SLW (Note1) / WIT	BBS 6, A	CPY ZP	CMP ZP	DEC ZP	BBS 6, ZP	INY	CMP IMM	DEX	SEB 6, A	CPY ABS	CMP ABS	DEC ABS	SEB 6, ZP
1101	D	BNE	CMP IND, Y	—	BBC 6, A	—	CMP ZP, X	DEC ZP, X	BBC 6, ZP	CLD	CMP ABS, Y	—	CLB 6, A	—	CMP ABS, X	DEC ABS, X	CLB 6, ZP
1110	E	CPX IMM	SBC IND, X	FST (Note2) / DIV	BBS 7, A	CPX ZP	SBC ZP	FST (Note2) DIV	BBS 7, ZP	INX	SBC IMM	NOP	SEB 7, A	CPX ABS	SBC ABS	INC ABS	SEB 7, ZP
1111	F	BEQ	SBC IND, Y	—	BBC 7, A	—	SBC ZP, X	INC ZP, X	BBC 7, ZP	SED	SBC ABS, Y	—	CLB 7, A	—	SBC ABS, X	INC ABS, X	CLB 7, ZP

Note 1

Instruction	type
SLW	M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP, M50758-XXXSP
WIT	other types

Note 2

Instruction	type
FST	M50740A-XXXSP, M50740ASP, M50741-XXXSP, M50752-XXXSP, M50757-XXXSP, M50758-XXXSP
DIV	M37450M2-XXXSP, M37450M4-XXXXSP, M37450M8-XXXSP, M37450S1SP, M37450S2SP, M37450S4SP
——	other types

Note 3

Instruction	type
MUL	M37450M2-XXXSP, M37450M4-XXXXSP, M37450M8-XXXSP, M37450S1SP, M37450S2SP, M37450S4SP
——	other types

Note 4

This instruction is not provided for M50752-XXXSP, M50757-XXXSP and M50758-XXXSP.

3-byte instruction

2-byte instruction

1-byte instruction

EXTENDED OPERATING TEMPERATURE VERSION OF MICROCOMPUTERS

3

M50744T-XXXSP

EXTENDED OPERATING TEMPERATURE VERSION of M50744-XXXSP

DESCRIPTION

The M50744T-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50744T-XXXSP and the M50744-XXXSP are some electrical characteristics depend on the expansion of operating temperature range. Other functions are explained in the M50744-XXXSP's section in detail.

FEATURES

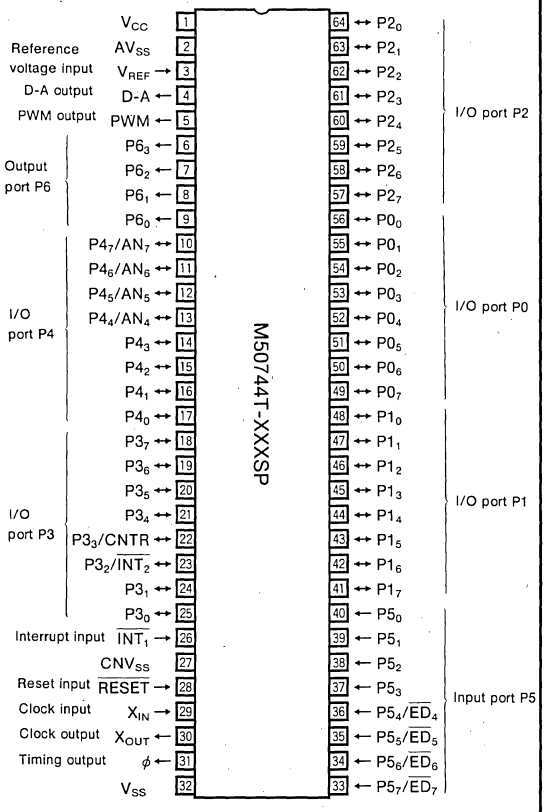
- Number of basic instructions 69
- Memory size ROM ..... 4096 bytes
  RAM 144bytes
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz ..... 5V±10%
- Power dissipation
  normal operation mode (at 4MHz frequency) 15mW
- Operating temperature range ..... −40~85℃
- Subroutine nesting ..... 72 levels (Max.)
- Interrupt ..... 6 types, 5 vecters
- 8-bit timer 3
- Programmable I/O (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Output ports (Port P6) 4
- A-D converter ..... 8-bit successive approximation
- D-A converter
- 8-bit PWM function
- Watchdog timer

APPLICATION

Office automation equipment

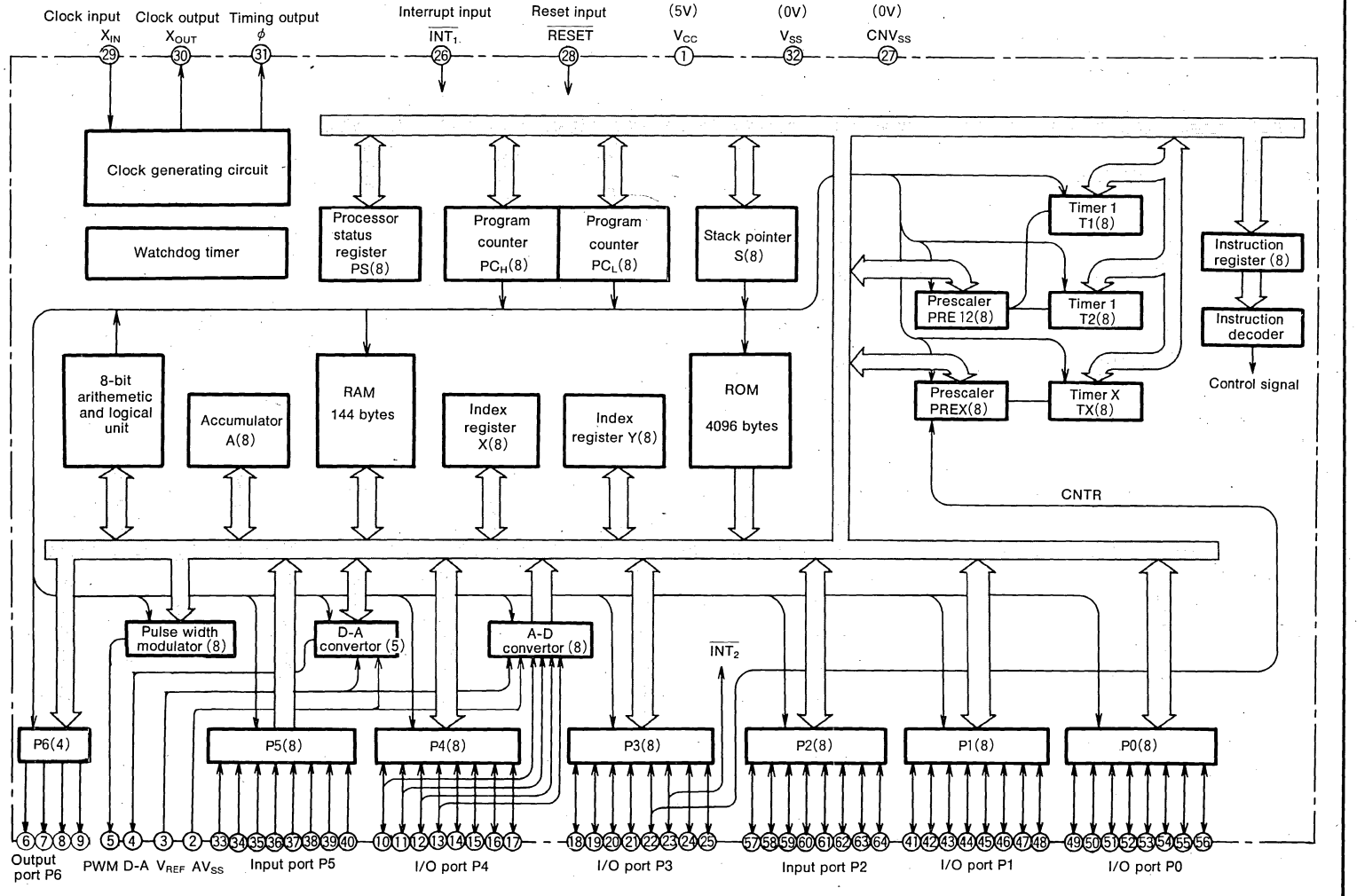
Automobile (Audio visual system, Instruction panel system, Air conditioner system)

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

M50744T-XXXSP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} With the output transistor cut-off	−0.3∼7	V
V_I	Input voltage X_{IN}		−0.3∼7	V
V_I	Input voltage $P2_0$∼$P2_7$, $P4_4$∼$P4_7$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, $P5_0$∼$P5_7$, $\overline{INT_1}$		−0.3∼13	V
V_I	Input voltage CNV_{SS}, $\overline{RESET}$		−0.3∼13	V
V_O	Output voltage $P2_0$∼$P2_7$, $P4_4$∼$P4_7$, X_{OUT}, ϕ, D-A		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, $P6_0$∼$P6_3$, PWM		−0.3∼13	V
P_d	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−40∼85	℃
Tstg	Storage temperature		−65∼150	℃

Note 1 : 300mW for QFP types

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−40∼85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, PWM (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$∼$P6_3$ (Note 2)			15	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, PWM (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0$∼$P6_3$ (Note 1)			7	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$∼$P2_7$ (Note 2)			−10	mA
$I_{OH(avg)}$	"H" average output current $P2_0$∼$P2_7$ (Note 1)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillator frequency			4	MHz

Note 1 : The average output currents $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
2 : Do not allow the combined low- level output current of ports P0, P1, P2, P3, P4, P6, and PWM to exceed 80mA.
Do not allow the combined high- level output current of port P2 to exceed 50mA.
3 : "H" input voltage of ports' P0, P1, P3, $P4_0$∼$P4_3$, P5 and $\overline{INT_1}$ is available up to +12V.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=−40~85℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P2_0$~$P2_7$	I_{OH}=−10mA		3			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA		3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_3$, PWM	I_{OL}=10mA				2	V
V_{OL}	"L" output voltage ϕ	I_{OL}=5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$	When used as $\overline{INT_2}$ input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_3$	When used as CNTR input		0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}			0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=0V				−5	μA
I_{IL}	"L" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I=0V				−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=12V				12	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, $P2_0$~$P2_7$, $P4_4$~$P4_7$	V_I=5V				5	μA
V_{RAM}	RAM retention voltage	When clock disabled		2			V
I_{CC}	Supply current	ϕ, X_{OUT}, and D-A pins opened, other pins at V_{SS}, and A-D converter in the finished condition.	$f_{(X_{IN})}$=4MHz Square wave		3	6	mA
			At clock stop T_a=25℃			1	μA
			At clock stop T_a=85℃			20	μA

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=−40~85℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute precision	V_{REF}=V_{CC}, with the output transistor cut-off			±3	LSB
R_{LADDER}	Ladder resistance	V_{REF}=V_{CC}	2		12	kΩ
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=−40~85℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			5	Bits
—	Error in full scale range	V_{REF}=V_{CC}, with the output transistor cut-off			±1	%
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
R_O	Output resistance	V_{REF}=V_{CC}			4	kΩ
V_{REF}	Reference voltage		4		V_{CC}	V

M50747T-XXXSP

EXTENDED OPERATING TEMPERATURE VERSION of M50747-XXXSP

DESCRIPTION

The M50747T-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50747T-XXXSP and the M50747-XXXSP are some electrical characteristics depend on the expansion of operating temperature range. Other functions are explained in the M50747-XXXSP's section in detail.

FEATURES

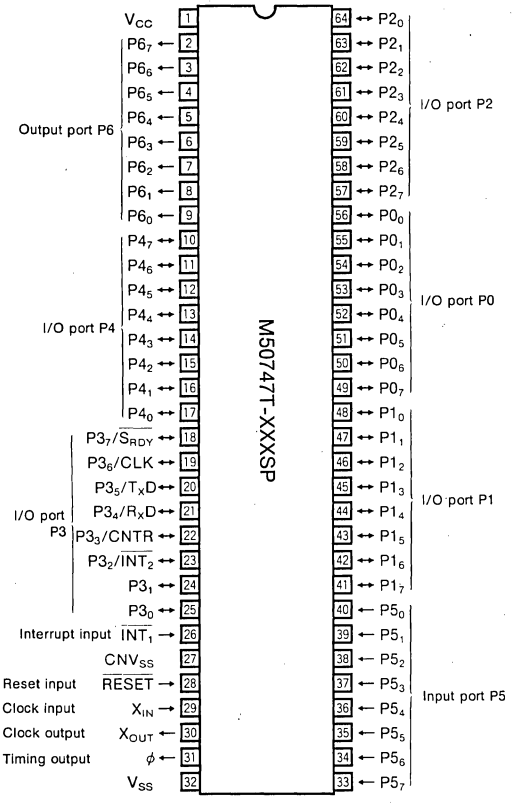
- Number of basic instructions 69
- Memory size ROM ..... 8192 bytes
  RAM ..... 256 bytes
- Instruction execution time
  ..... 1μs (minimum instructions at 8MHz frequency)
- Single power supply f(X_{IN})=8MHz ..... 5V±10%
- Operating temperature range ..... −40~85°C
- Power dissipation
  normal operation mode (at 8MHz frequency) 30mW
- Subroutine nesting ..... 128 levels (Max.)
- Interrupt ..... 7 types, 5 vecters
- 8-bit timer ..... 3 (2 when used as serial I/O)
- Programmable I/O (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Output ports (Port P6) 8
- Serial I/O (Clock synchronized or UART) 1

APPLICATION

Office automation equipment

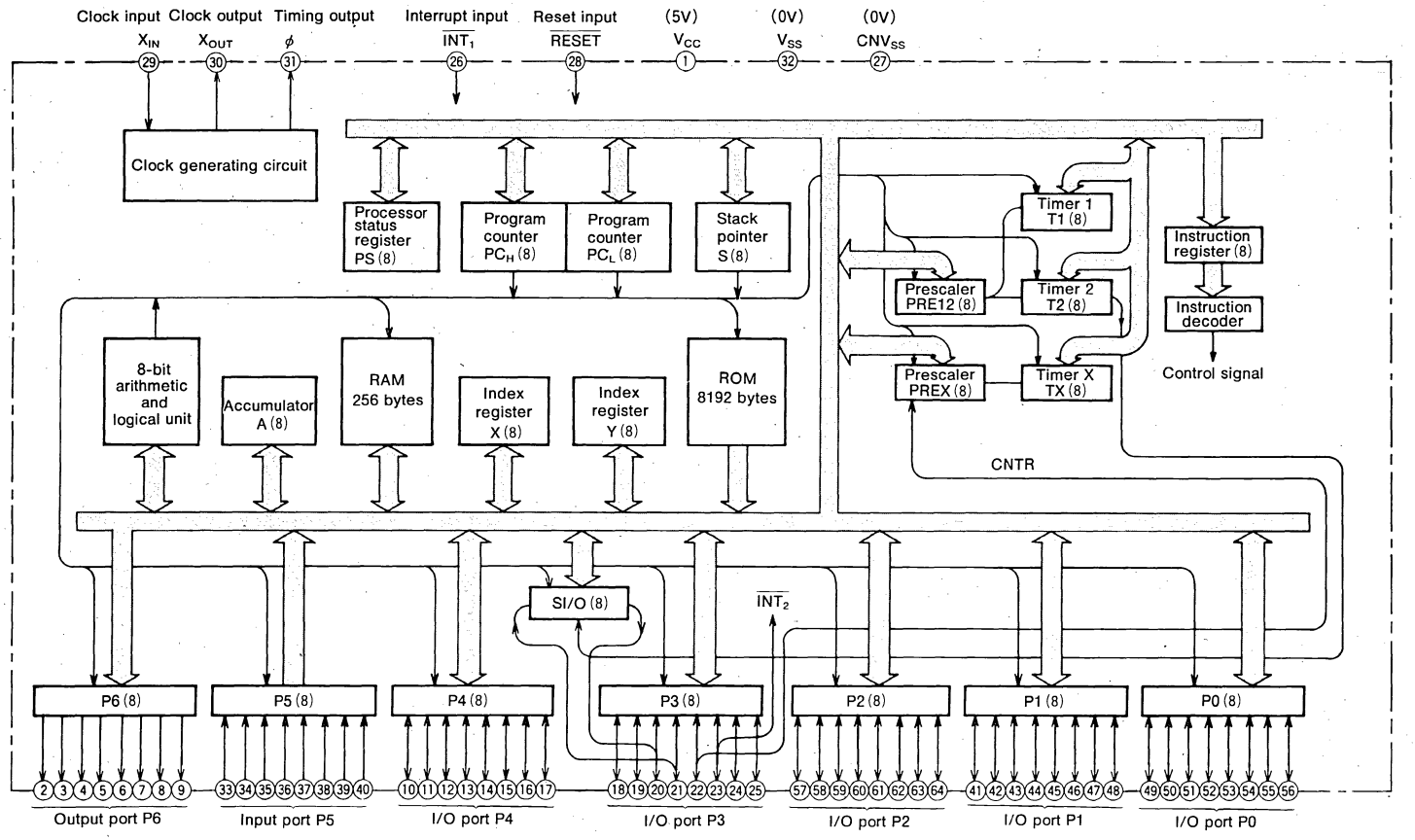
Automobile (Audio visual system, Instruction panel system, Air conditioner system)

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

M50747T-XXXSP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

EXTENDED OPERATING TEMPERATURE VERSION of M50747-XXXSP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off	−0.3~7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, $\overline{INT_1}$, $P5_0$~$P5_7$		−0.3~7	V
V_I	Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$,		−0.3~V_{CC}+0.3	V
V_I	Input voltage, CNV_{SS}		−0.3~13	V
V_O	Output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$, X_{OUT}, ϕ		−0.3~V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
T_{opr}	Operating temperature		−40~85	℃
Tstg	Storage temperature		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5V±10%, T_a = −40~85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$ (Note 1)			5	mA
$I_{OH(peak)}$	"H" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7P6_0$~$P6_7$, (Note 1)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			8	MHz

Note 1 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms
2 : Total of $I_{OL(peak)}$, of ports P0, P1, and P2 is 20mA
Total of $I_{OH(peak)}$, of ports P0, P1, and P2 is 20mA
Total of $I_{IL(peak)}$, of ports P3, P4, and P6 is 80mA
Total of $I_{OH(peak)}$, of ports P3 and P4 is 20mA
Let the total of $I_{OH(peak)}$, of ports P6 below 60mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{SS} = 0V, T_a = −40~85℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OH} = −10mA		3			V
V_{OH}	"H" output voltage, ϕ	I_{OH} = −2.5mA		3			V
V_{OL}	"L" output voltage, $P0_0$~ $P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OL} = 10mA				2	V
V_{OL}	"L" output voltage, ϕ	I_{OL} = 5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_6$	When used as CLK input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{INT_1}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_2$	When used as $\overline{INT_2}$ pin		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_3$	When used as CNTR input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis, X_{IN}			0.1		0.5	V
I_{IL}	"L" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 0V				−5	μA
I_{IH}	"H" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 5V				5	μA
V_{RAM}	RAM retention voltage	At stop mode		2			V
I_{CC}	Supply current	Output terminals are opened, others to V_{SS}	$f_{(X_{IN})}$ = 8MHz Square wave		6	12	mA
			At stop mode T_a = 25℃			1	μA
			At stop mode T_a = 85℃			20	μA

M50753T-XXXSP

EXTENDED OPERATING TEMPERATURE VERSION of M50753-XXXSP

DESCRIPTION

The M50753T-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50753T-XXXSP and the M50753-XXXSP are some electrical characteristics depend on the expansion of operating temperature range and the fact that this microcomputer works only in the single-chip mode.

FEATURES

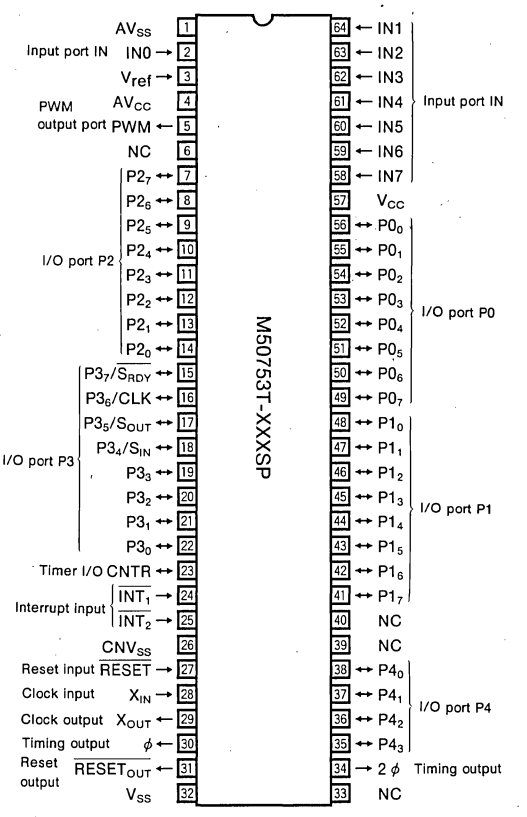
- Number of basic instructions 69
- Memory size ROM ..... 6144 bytes
  RAM ..... 192 bytes
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply f(X_{IN})=4MHz ..... 5V±10%
- Power dissipation
  normal operation mode (at 4MHz frequency) 22.5mW
- Operating temperature range ..... −40~85℃
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 8 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as A-D or serial I/O)
- Programmable I/O ports (Port P0, P1, P2, P3, P4) 36
- Input ports (Port IN) 8
- Serial I/O (8-bit) 1
- A-D converter ..... 8-bit successive approximation
- PWM function 1

APPLICATION

Office automation equipment

Automobile (Audio visual system, Instruction panel system, Air conditioner system)

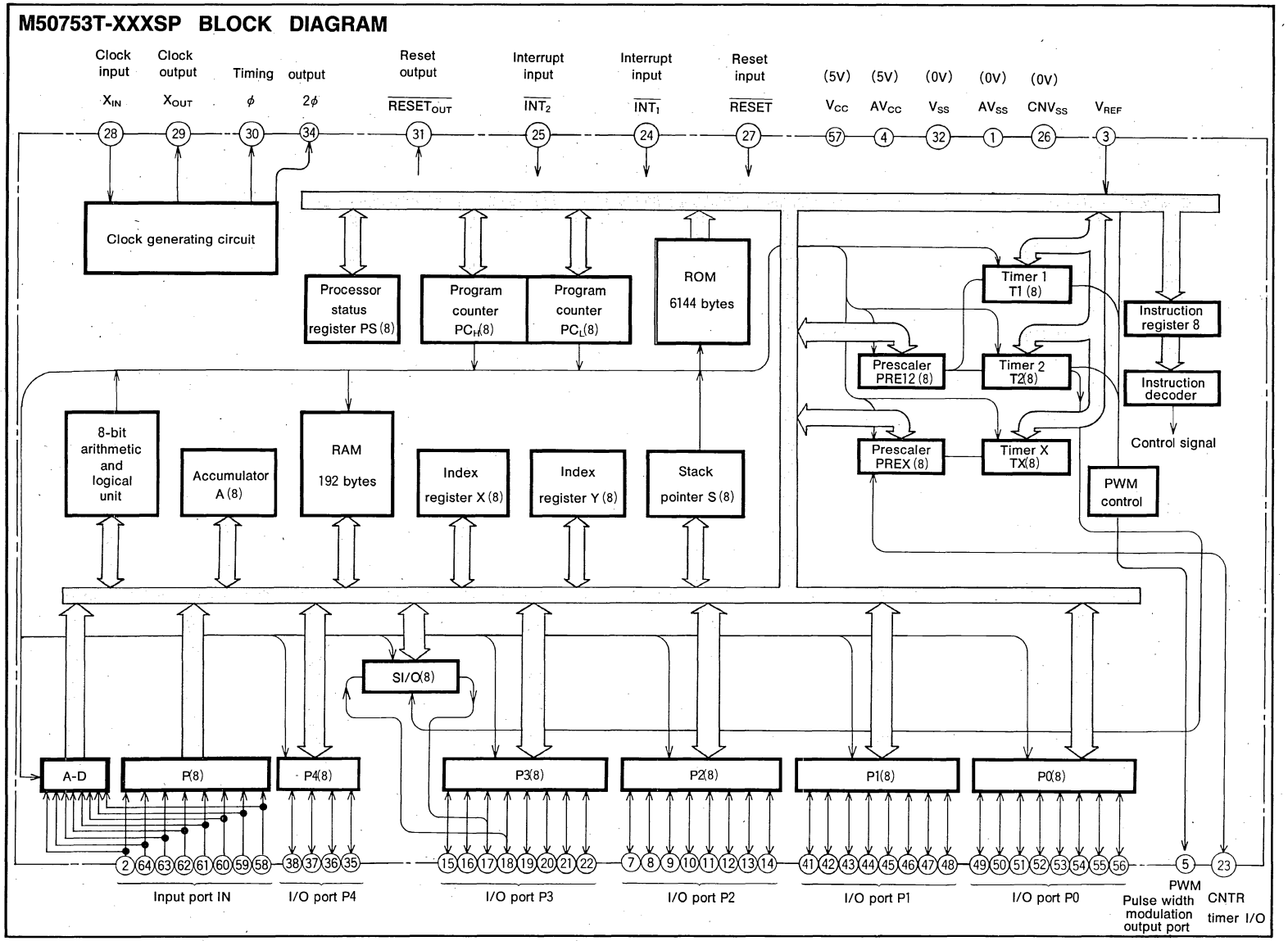
PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

NC : No connection

M50753T-XXXSP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

EXTENDED OPERATING TEMPERATURE VERSION of M50753-XXXSP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state	−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3∼7	V
V_I	Input voltage IN0∼IN7		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}		−0.3∼13	V
V_O	Output voltage 2 ϕ, X_{OUT}, ϕ, $\overline{RESET_{OUT}}$		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, CNTR, PWM		−0.3∼13	V
Pd	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−40∼85	℃
T_{stg}	Storage temperature		−65∼150	℃

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, T_a=−40∼85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, IN0∼IN7, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, IN0∼IN7, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

Note 1 : "H" input voltage of ports P0, P1, P2, P3, P4, CNTR, $\overline{INT_1}$, and $\overline{INT_2}$ is available up to +12V.
(However, these ports are without pull-up transistor)

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=−40~85℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage ϕ, $\overline{RESET_{OUT}}$, 2ϕ	I_{OH}=−2.5mA				V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, CNTR, $P4_0$~$P4_3$, PWM	I_{OL}=8mA			2	V
V_{OL}	"L" output voltage ϕ, $\overline{RESET_{OUT}}$, 2ϕ	I_{OL}=5mA			2	V
$V_{T+}-V_{T-}$	Hysterisis $P3_6$	When used as CLK input	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis CNTR, $\overline{INT_1}$, $\overline{INT_2}$		0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, PWM	V_I=0V Without pull-up transistor			−5	μA
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, PWM	V_I=0V With pull-up transistor	−40	−70	−190	μA
I_{IL}	"L" input current IN0~IN7	V_I=0V			−5	μA
I_{IL}	"L" input current CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	V_I=0V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, PWM	V_I=12V Without pull-up transistor			12	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, PWM	V_I=5V With pull-up transistor			5	μA
I_{IH}	"H" input current IN0~IN7	V_I=5V (when A-D not selection)			5	μA
I_{IH}	"H" input current CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	V_I=5V			5	μA
I_{IH}	"H" input current V_{REF}	V_I=5V			5	mA
I_{CC}	Supply current	Output pins are open, input and I/O pins are connected to V_{SS}		4.5	9	mA
I_{ACC}	Supply current for A-D	During A-D conversion		3	6	mA

A-D CONVERTER CHARACTERISTICS (V_{CC}=AV_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=−40~85℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution		—	—	8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=V_{REF}=5.12V			±3	LSB
R_{LADDER}	Ladder resistance value		1			kΩ
t_{CONV}	Conversion time				72	μs
V_{REF}	Reference input voltage				V_{CC}	V
V_{IA}	Analog input voltage				V_{REF}	V

TIMING REQUIREMENTS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−40~85℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{SU(P0D-\phi)}$	Port P0 input setup time	320			ns
$t_{SU(P1D-\phi)}$	Port P1 input setup time	320			ns
$t_{SU(P2D-\phi)}$	Port P2 input setup time	320			ns
$t_{SU(P3D-\phi)}$	Port P3 input setup time	320			ns
$t_{SU(P4D-\phi)}$	Port P4 input setup time	320			ns
$t_{SU(IND-\phi)}$	Port IN input setup time	320			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	40			ns
$t_{h(\phi-IND)}$	Port IN input hold time	40			ns
t_C	External clock input cycle time	250			ns
t_W	External clock input pulse width	75			ns
t_r	External clock rising edge			25	ns
t_f	External clock falling edge			25	ns

SWITCHING CHARACTERISTICS

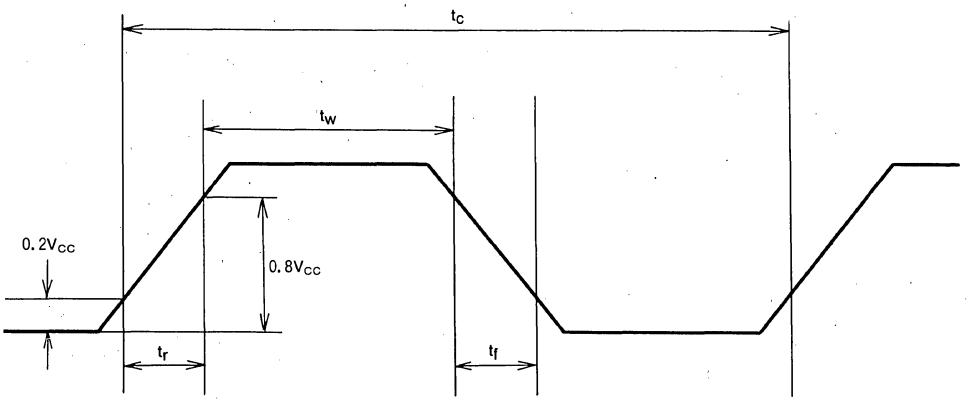
Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−40~85℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 1			300	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				300	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				300	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				300	ns

2ϕ PIN AC CHARACTERISTICS (V_{CC}=5.0V, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_C	Clock output cycle time	Fig. 2		500		ns
t_W	Clock output pulse width		150			ns
t_r	Clock rising time				75	ns
t_f	Clock falling time				50	ns

Timing diagram of 2ϕ



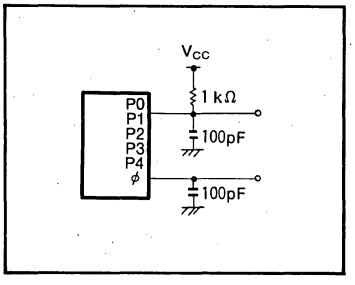


Fig.1 Ports P0～P4 test circuit

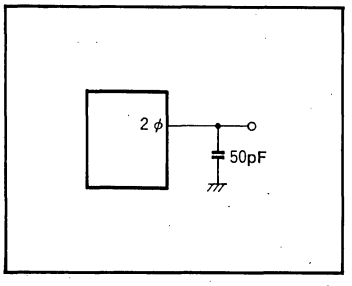
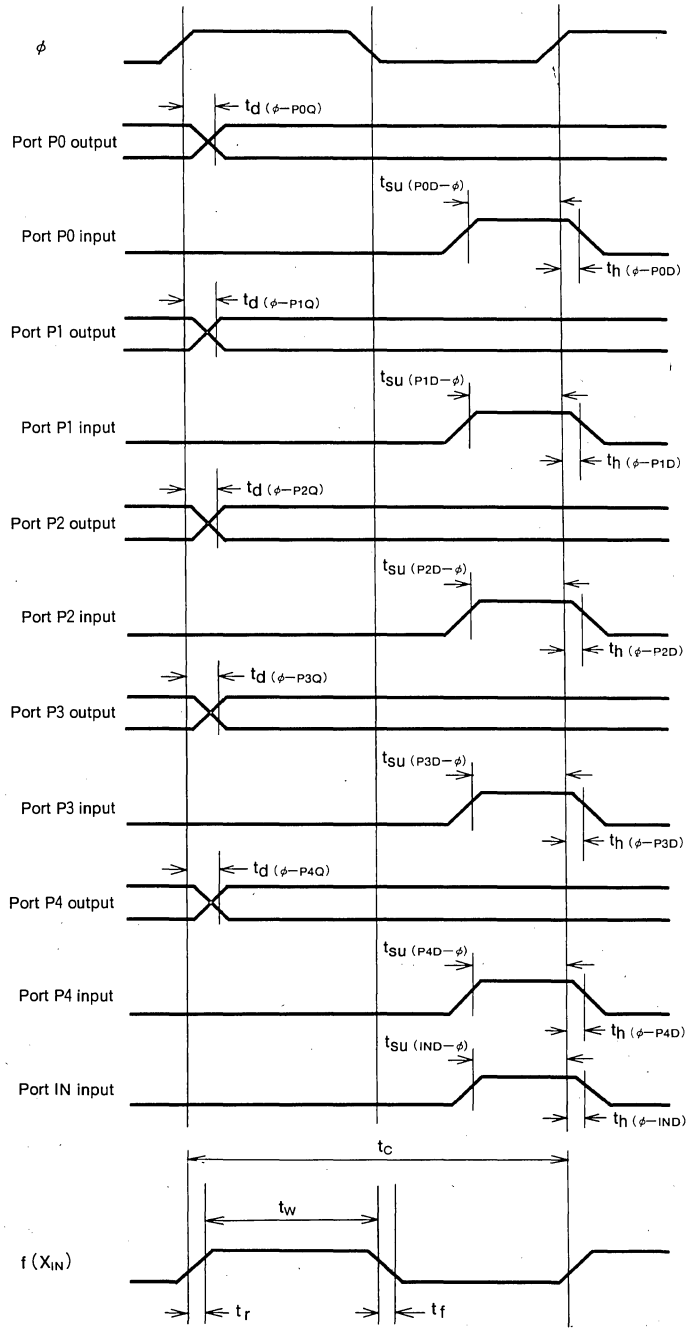


Fig.2 2ϕ test circuit

MITSUBISHI ELECTRIC

TIMING DIAGRAMS

In single-chip mode



M50930T-XXXFP

EXTENDED OPERATING TEMPERATURE VERSION of M50930-XXXFP

DESCRIPTION

The M50930T-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 80-pin plastic molded QFP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O address are placed on the same memory map to enable easy programming.

The differences between the M50930T-XXXFP and the M50930-XXXFP are some electrical characteristics depend on the expansion of operating temperature range. Other functions are explained in the M50930-XXXFP's section in detail.

FEATURES

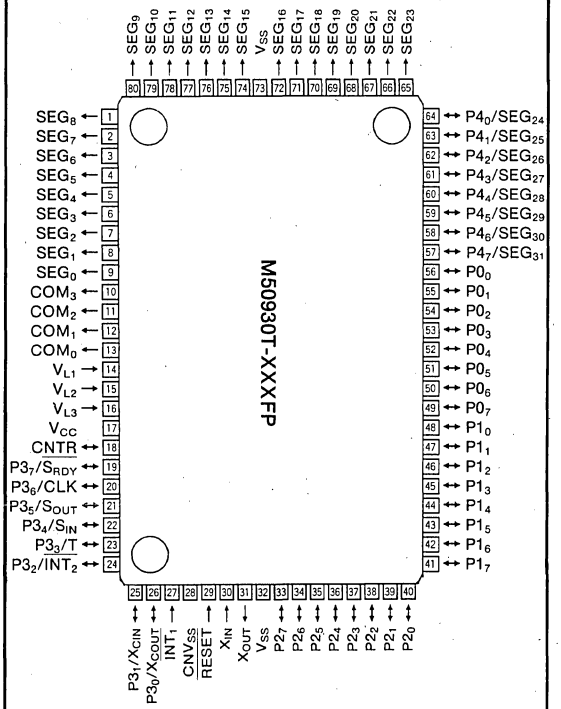
- Number of basic instructions 69
- Memory size
  - ROM ..... 4096 bytes
  - RAM ..... 128 bytes
- Instruction executing time
  - ..... 2μs (minimum instructions, at 4MHz frequency)
- Single power supply
  - f(X_{IN})=4MHz ..... 5V±10%
  - f(X_{IN})=1MHz ..... 2.7V ≦ V_{CC} ≦ 5.5V(Typ.)
- Power dissipation
  - nomal operation mode (at 4MHz frequency) ..... 15mW(V_{CC}=5V, Typ.)
  - low-speed operation mode (at 32kHz frequency for clock function) ..... 225μW (V_{CC}=5V, Typ.)
  - stop mode(at 25℃) ..... 5μW (V_{CC}=5V, Max.)
- RAM retention voltage (stop mode) ..... 2.0V ≦ V_{RAM} ≦ 5.5V
- Operating temperature range ..... −40∼85℃
- Subroutine nesting ..... 64 levels (Max.)
- Interrupt ..... 8 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as serial I/O)
- 16-bit timer ..... 1 (Two 8-bit timers make one set)
- Programmable I/O ports (Port P0, P1, P2, P3) 32
- Input ports (Port P4) 8
- Serial I/O (8-bit) 1
- LCD controller/driver (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty)
  - segment output 32
  - common output 4
- Two clock generator circuits (One is for main clock, the other is for clock function)

APPLICATION

Office automation equipment

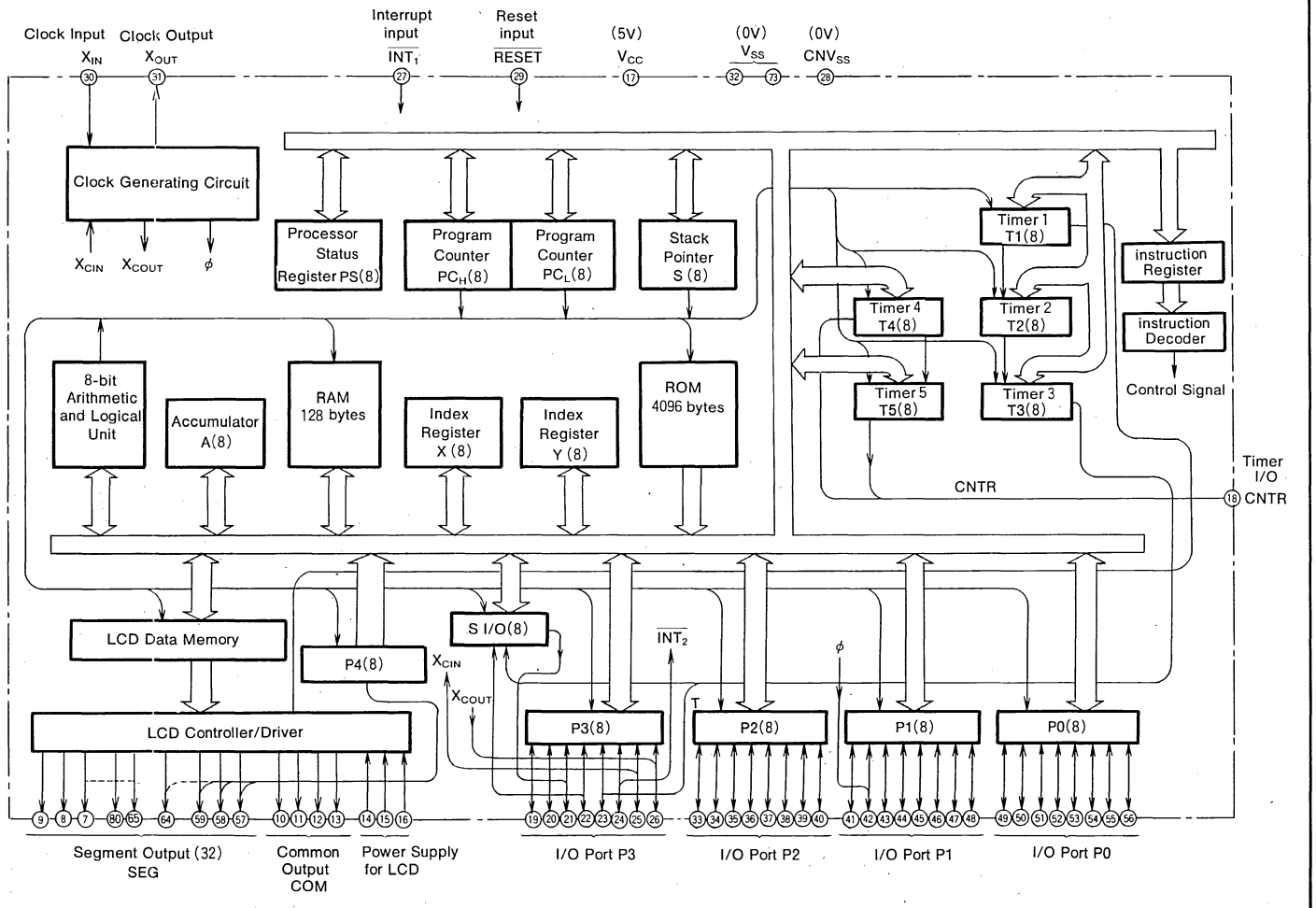
Automobile (Audio visual system, Instruction panel system, Air conditioner system)

PIN CONFIGURATION (TOP VIEW)



Outline 80P6

M50930T-XXXFP BLOCK DIAGRAM



EXTENDED OPERATING TEMPERATURE VERSION of M50930-XXXFP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Output transistor are "off"	−0.3∼7	V
V_I	Supply voltage for LCD V_{L1}∼V_{L3}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, X_{IN}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $\overline{INT_1}$, CNV_{SS}		−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, CNTR		−0.3∼13	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, COM_0∼COM_3, SEG_0∼SEG_{31}, X_{OUT}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage CNTR		−0.3∼7	V
Pd	Power Dissipation	T_a = 25℃	300	mW
Topr	Operating temperature		−40∼85	℃
Tstg	Strage temperature		−55∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=2.7∼5.5V, V_{SS}=0V, T_a=−40∼85℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Nom.	Max.	
V_{CC}	Supply voltage (Note 1)	f(X_{IN})=4.3MHz	4.5		5.5	V
	(in single-chip mode)	f(X_{IN})=1.1MHz	2.7		5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ (Note 2), $P3_3$∼$P3_7$ (Note3), $P4_0$∼$P4_7$, $\overline{RESET}$, X_{IN}, CNV_{SS}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$ (Note 4), $\overline{INT_1}$, CNTR		0.85V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ (Note 2), $P3_3$∼$P3_7$ (Note 3), $P4_0$∼$P4_7$, CNV_{SS}		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$ (Note 4), $\overline{INT_1}$, CNTR		0		0.15V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.1V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.14V_{CC}	V
I_{OH}	"H" Output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$ (Note 5), X_{OUT}				−2	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, X_{OUT} (Note 6)				10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, X_{OUT} (Note 7)				5	mA
f(X_{IN})	Clock oscillating frequency (Note 8)	V_{CC}=4.5∼5.5V	64		4300	kHz
		V_{CC}=2.7∼5.5V	64		1100	
f(X_{CIN})	Clock oscillating frequency for clock function (Note 8)		32		50	kHz

Note 1 Value of V_{CC} is 4.5≦V_{CC}≦5.5 in memory expanding and microprocessor mode. When only maintaining the RAM data, minimum value of V_{CC} is 2V.
2 When using port $P3_1$ as X_{CIN}, 0.9V_{CC}≦V_{IH}≦V_{CC}, 0≦V_{IL}≦0.1V_{CC} for port $P3_1$.
3 In this case of using port $P3_6$ as normal input.
4 In this case of using port $P3_6$ as CLK input.
5 The total of I_{OH} of port P0, P1, P2, P3 and X_{OUT} should be 35mA max.
6 The total of I_{OL} (peak) of port P0, P1, P2, P3 should be 55mA max, and the total of I_{OL} (peak) of port P3, CNTR, and X_{OUT} should be 45mA max.
7 I_{OL} (avg) is the average current in 100ms.
8 When changing the contents of the most significant bit at address $00F5_{16}$, f(X_{IN}) needs the following range : f(X_{IN})>3f(X_{CIN}).

ELECTRICAL CHARACTERICS (V_{SS}= 0 V, T_a=−40~85℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$(Note 9)(Note10)		V_{CC}=5V, I_{OH}=−2mA		3			V
			V_{CC}=3V, I_{OH}=−0. 7mA		2			
V_{OH}	"H" output voltage X_{OUT}		V_{CC}=5V, I_{OH}=−1. 5mA		3			V
			V_{CC}=3V, I_{OH}=−0. 3mA		2			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$(Note10), CNTR		V_{CC}=5V, I_{OL}=10mA				2	V
			V_{CC}=3V, I_{OL}=3mA				1	
V_{OL}	"L" output voltage X_{OUT}		V_{CC}=5V, I_{OL}=1. 5mA				2	V
			V_{CC}=3V, I_{OL}=0. 3mA				1	
V_{T+}−V_{T-}	Hysteresis $\overline{INT_1}$, CNTR		V_{CC}=5V		0. 25		1	V
			V_{CC}=3V		0. 15		0. 7	
V_{T+}−V_{T-}	Hysteresis $P3_6$		When used as CLK input	V_{CC}=5V		0. 5		V
				V_{CC}=3V		0. 4		
V_{T+}−V_{T-}	Hysteresis $P3_1$		When used as X_{CIN} input	V_{CC}=5V		0. 7		V
				V_{CC}=3V		0. 5		
V_{T+}−V_{T-}	Hysteresis $P2_0$~$P2_7$, $P3_2$		V_{CC}=5V			0. 5		V
			V_{CC}=3V			0. 4		
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$		V_{CC}=5V			0. 35	0. 5	V
			V_{CC}=3V			0. 25		
V_{T+}−V_{T-}	Hysteresis X_{IN}		V_{CC}=5V			0. 5		V
			V_{CC}=3V			0. 35		
I_{IL}	"L" input current $P4_0$~$P4_7$ (except reset state) {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$)} without pull-up Tr. CNTR, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}		V_{CC}=5V, V_I=0V				−5	μA
			V_{CC}=3V, V_I=0V				−4	
I_{IL}	"L" input current {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$)} with pull-up Tr.		V_{CC}=5V, V_I=0V		−30	−70	−140	μA
			V_{CC}=3V, V_I=0V		−6	−25	−45	
I_{IL}	"L" input current $P4_0$~$P4_7$ (at reset state)		V_{CC}=5V, V_{L3}=5V, V_I=0V		−30		−140	μA
			V_{CC}=3V, V_{L3}=3V, V_I=0V		−6		−45	
I_{IH}	"H" input current $P4_0$~$P4_7$ (except reset state) $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}		V_{CC}=5V, V_I=5V				5	μA
			V_{CC}=3V, V_I=3V				4	
I_{IH}	"H" input current $P4_0$~$P4_7$ (at reset state)		V_{CC}=5V, V_{L3}=5V, V_I=5V				5	μA
			V_{CC}=3V, V_{L3}=3V, V_I=3V				4	
R_{COM}	Output impedance COM_0~COM_3		V_{L1}=V_{CC}/3, V_{L2}=2V_{L1}, V_{L3}=V_{CC} Other COM, SEG pins are opend.	V_{CC}=5V	30	200	2000	Ω
				V_{CC}=3V	70	500	4000	
R_S	Output impedance SEG_0~SEG_{31}			V_{CC}=5V		2		kΩ
				V_{CC}=3V		3		
I_{CC}	Supply current (at operation)	Output pin are opend. $\overline{RESET}$, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, and $P3_0$~$P3_7$ are conected to V_{CC} Except the above pins are conected to V_{SS}. However, X_{IN} and X_{CIN} are input signal according to the conditions.	f(X_{IN})=4MHz, V_{CC}=5V			3	6	mA
			f(X_{IN})=1MHz, V_{CC}=3V			0. 7		
			T_a=25℃ X_{IN}=0V f(X_{CIN})=32. 8kHz at low power mode (LM_6=1)	V_{CC}=5V		45		μA
				V_{CC}=3V		18		
I_{CC}	Supply current (at wait state)		f(X_{IN})=4MHz, V_{CC}=5V			1		mA
			f(X_{IN})=1MHz, V_{CC}=3V			0. 4		
			T_a=25℃ X_{IN}=0V f(X_{CIN})=32. 8kHz at low power mode (LM_6=1)	V_{CC}=5V		20	60	μA
				V_{CC}=3V		4	12	
I_{CC}	Supply current		f(X_{IN})=0 f(X_{CIN})=0 V_{CC}=5V	T_a=25℃		0. 1	1	μA
				T_a=70℃			10	
V_{RAM}	RAM retention voltage		f(X_{IN})=0, f(X_{CIN})=0		2		5. 5	V

Note 9 Except when the output type of $P3_5$ is N-channel open drain (mask option).
10 If $P3_0$ is used as X_{COUT}, capability of load driving is lower than the above.

TIMING REQUIREMENTS

Memory expanding mode and microprocessor mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=−40~85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{su} (P2D−ϕ)	Port P2 input setup time		270			ns
t_{su} (P3D−ϕ)	Port P3 input setup time		270			ns
t_{su} (P4D−ϕ)	Port P4 input setup time		270			ns
t_{WI}	$\overline{INT_1}$, $\overline{INT_2}$ External clock input pulse width		1			μs
		V_{CC}=2.7V	4			μs
t_{WR}	$\overline{RESET}$ External clock input pulse width (Note 1)		2			μs
		V_{CC}=2.7V	8			μs
t_h (ϕ−P2D)	Port P2 input hold time		20			ns
t_h (ϕ−P3D)	Port P3 input hold time		20			ns
t_h (ϕ−P4D)	Port P4 input hold time		20			ns
t_C	External clock input cycle time (X_{IN} pin)		232			ns
t_W	External clock input pulse width (X_{IN} pin)		80			ns
t_r	External clock rising edge time (X_{IN} pin)				25	ns
t_f	External clock falling edge time (X_{IN} pin)				25	ns
t_{CC}	External clock input cycle time ($P3_1/X_{CIN}$ pin, X_{CIN})		20			μs
t_{WC}	External clock input pulse width ($P3_1/X_{CIN}$ pin, X_{CIN})		5			μs
t_{rc}	External clock rising edge time ($P3_1/X_{CIN}$ pin, X_{CIN})				6.2	μs
t_{fc}	External clock falling edge time ($P3_1/X_{CIN}$ pin, X_{CIN})				6.2	μs

Note 1 : Hold $\overline{RESET}$ to "L" level while eight or more rise pulse are input from X_{IN}.

SWITCHING CHARACTERISTICS

Memory expanding mode and microprocessor mode (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_d (ϕ−P0A)	Port P0 address output delay time	Fig. 1			250	ns
t_d (ϕ−P1A)	Port P1 address output delay time				250	ns
t_d (ϕ−P2Q)	Port P2 address output delay time				330	ns
t_d (ϕ−P2QF)	Port P2 address output delay time				300	ns
t_d (ϕ−R/W)	R/$\overline{W}$ signal output delay time				tcyc/4 +210	ns
t_d (ϕ−R/WF)	R/$\overline{W}$ signal output delay time				250	ns
t_d (ϕ−SYNC)	SYNC signal output delay time				250	ns
t_d (ϕ−P3Q)	Port P3 data output delay time				250	ns

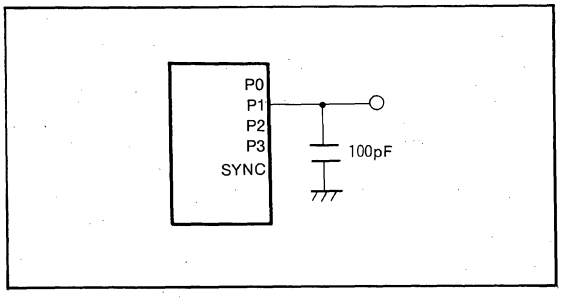
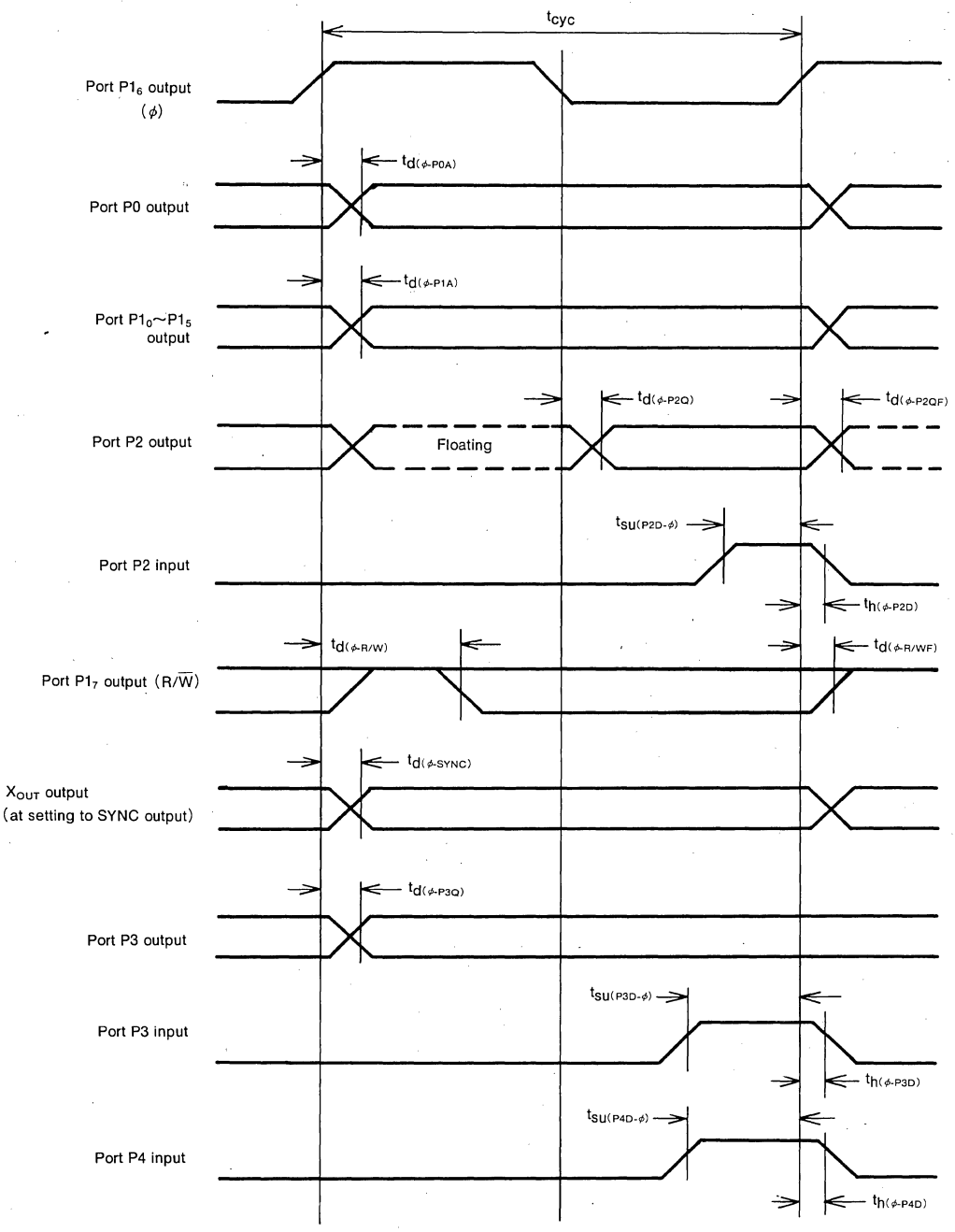
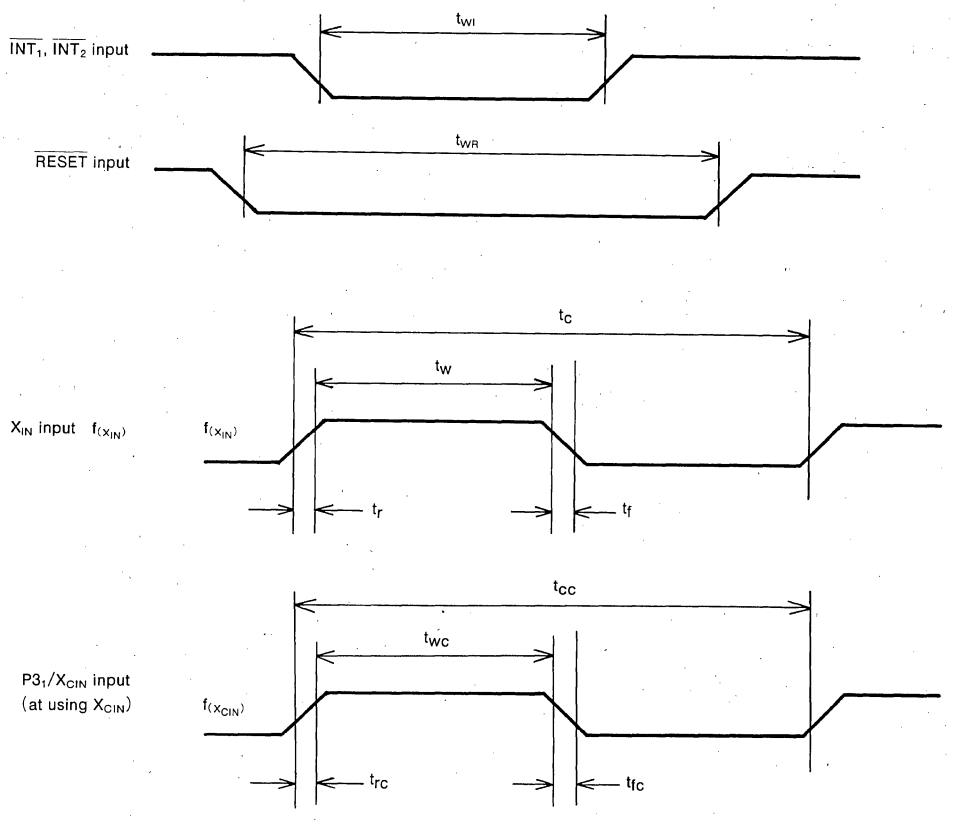


Fig.1 Port P0, P1, P2, P3, SYNC (X_{OUT}) test circuit

TIMING DIAGRAMS

In memory expanding mode and microprocessor mode




$\overline{INT_1}$, $\overline{INT_2}$ input
t_{WI}
$\overline{RESET}$ input
t_{WR}
X_{IN} input $f_{(X_{IN})}$
t_C
t_W
t_r
t_f
$P3_1/X_{CIN}$ input
(at using X_{CIN})
$f_{(X_{CIN})}$
t_{CC}
t_{WC}
t_{rc}
t_{fc}

PIGGYBACK TYPE MICROCOMPUTERS

M50740-PGYS

PIGGYBACK for M50740A-XXXSP, M50741-XXXSP

DESCRIPTION

The M50740-PGYS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip 8-bit microcomputers M50740A-XXXSP and M50741-XXXSP. The M50740-PGYS, being housed in a piggyback-type 52 pin shrink DIP, is compatible with the M50740A-XXXSP/M50741-XXXSP.

There is a 28 pin socket on the top surface so that the M5L2732K or the M5L2764K EPROM may be used.

The M50740-PGYS simplifies the development of programs for the M50740A-XXXSP/M50741-XXXSP and is excellent for making prototypes.

DISTINCTIVE FEATURES

- Differences with the M50740A-XXXSP/M50741-XXXSP are:

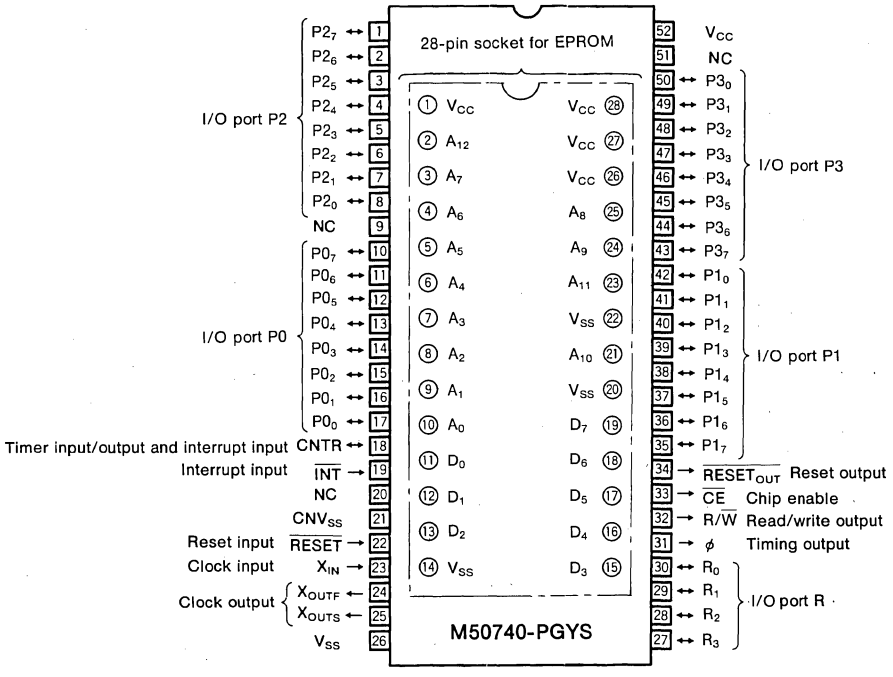
(1) ROMless, EPROM is attached externally

(2) Suitable EPROM is the M5L2732K or the M5L2764K.

APPLICATION

Development of programs for VCR, tuners and audio equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 52S1M

The symbol "○" indicates sockets for EPROM.
NC: No Connection.

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external RC circuit is connected between the X_{IN} and X_{OUTS} or the X_{OUTF} pins, and an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUTS} pins. If an external clock is used, the clock source shold be connected to the X_{IN} pin, and the X_{OUTS} and X_{OUTF} pins should be left open.
X_{OUTS}	Clock output	Output	This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a RC circuit, a ceramic or a quartz crystal oscillator between this pin and X_{IN} pin.
X_{OUTF}	Clock output	Output	This is output pin from internal clock generating circuit. The generating frequency can be controlled by connectting a RC circuit between this pin and X_{IN} pin.
ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O or interrupt input	I/O	This is in common with an I/O for the timer X and an interrupt input pin.
$\overline{INT}$	Interrupt input	Input	This is the lowest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is P-channel open drain.
R_0~R_3	I/O port R	I/O	Port R is a 4-bit I/O port, and is used to connect with an I/O expander. For M50740A-XXXSP, it can be only for input.
$R/\overline{W}$	Read/Write output	Output	This pin outputs read/write signal for I/O expander.
$\overline{CE}$	Chip enable output	Output	This pin outputs the chip enable signal for I/O expander.
$\overline{RESET_{OUT}}$	Reset output	Output	This pin outputs the reset signal for I/O expander.
A_0~A_{12}	Output port A	Output	Port A is for output addresses to an EPROM mounted on the top of the package.
D_0~D_7	Input port D	Input	Port D is for input data from an EPROM mounted on the top of the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M50740A-XXXSP/M50741-XXXSP are explained below. As all other points are the same, only the differences are explained.

MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is 0100_{16} to $1FFF_{16}$, having 7936 bytes. Other than this, the M50740A-XXXSP/M50741-XXXSP have the same functions. Note that the area of the ROM will change depending on the memory capacity of the EPROM.

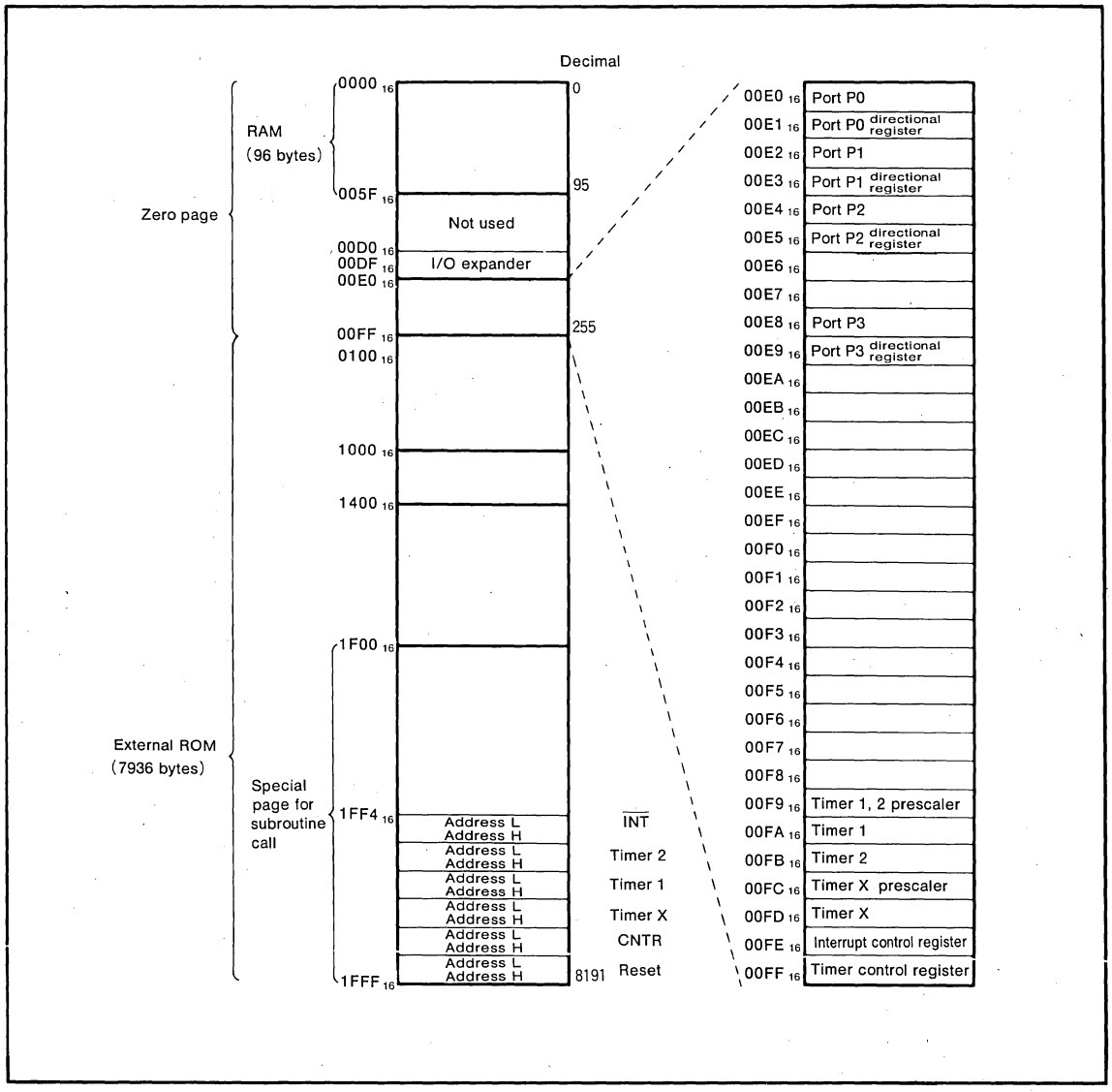


Fig.1 Memory map

PROCESSOR MODE

External memory area differs from the M50740A-XXXSP/M50741-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50740-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50740A-XXXSP/M50741-XXXSP.

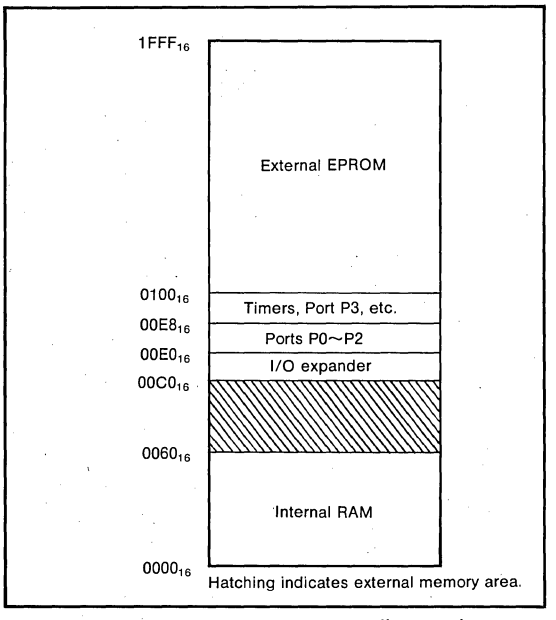


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) Because of the loading of the EPROM, the external dimensions differ from those of the M50740A-XXXSP/M50741-XXXSP, being 19.0×50.8mm. Lower pin measurements are the same.

(2) When developing programs with the M50740-PGYS, carefully consider the ROM capacity of the M50740A-XXXSP/M50741-XXXSP.
In the case of the M50740A-XXXSP, use the ROM area from 1400_{16} to $1FFF_{16}$ of the M50740-PGYS. (For the M5L2732K use from 0400_{16} to $0FFF_{16}$.)
In the case of the M50741-XXXSP, use the ROM area from 1000_{16} to $1FFF_{16}$ of the M50740-PGYS. (For the M5L2732K use from 0000_{16} to $0FFF_{16}$.)

(3) The M50740-PGYS has no options as the M50740A-XXXSP.
For the M50740-PGYS, port R is set the input/output port.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} pin. Output transistor off.	−0.3~7	V
V_I	Input voltage, R_0~R_3, CNV_{SS}, $\overline{RESET}$, X_{IN}, D_0~D_7		−0.3~7	V
V_I	Input voltage, $P3_0$~$P3_7$		−3.0~V_{CC}+0.3	V
V_I	Input voltage, $\overline{INT}$, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, CNTR		−0.3~13	V
V_O	Output voltage, R_0~R_3		−0.3~7	V
V_O	Output voltage, $P3_0$~$P3_7$, X_{OUTF}, X_{OUTS}, ϕ, R/$\overline{W}$, $\overline{CE}$, $\overline{RESET_{OUT}}$, A_0~A_{12}		−0.3~V_{CC}+0.3	V
V_O	Output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, CNTR		−0.3~13	V
P_d	Power dissipation	T_a = 25℃	1000	mW
T_{opr}	Operating temperature		−10~70	℃
T_{stg}	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −10~70℃, V_{CC} = 5V±5%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, CNTR, $\overline{INT}$	0.8V_{CC}		12	V
V_{IH}	"H" input voltage, $P3_0$~$P3_7$, R_0~R_3, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, $\overline{RESET}$	0.48V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, D_0~D_7	0.45V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, R_0~R_3, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, CNTR, $\overline{INT}$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, D_0~D_7	0		0.15V_{CC}	V
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

Note 1 : "H" input voltage of up to 12V is permissible for ports P0, P1 and P2 as well as CNTR and $\overline{INT}$.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±5%, V_{SS} = 0V, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage, $P3_0$~$P3_7$	V_{CC} = 5V, T_a = 25℃, I_{OH} = −10mA	3			V
V_{OH}	"H" output voltage, ϕ, R/$\overline{W}$, $\overline{CE}$, $\overline{RESET_{OUT}}$, A_0~A_{12}	V_{CC} = 5V, T_a = 25℃, I_{OH} = −2.5mA	3			V
V_{OL}	"L" output voltage, $P0_0$~ $P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, R_0~R_3, CNTR	V_{CC} = 5V, T_a = 25℃, I_{OL} = 10mA			2	V
V_{OL}	"L" output voltage, ϕ, R/$\overline{W}$, $\overline{CE}$, $\overline{RESET_{OUT}}$, A_0~A_{12}.	V_{CC} = 5V, T_a = 25℃, I_{OL} = 5mA			2	V
V_{T+}−V_{T-}	Hysteresis, CNTR, $\overline{INT}$	V_{CC} = 5V, T_a = 25℃	0.3		1	V
V_{T+}−V_{T-}	Hysteresis, $\overline{RESET}$	V_{CC} = 5V, T_a = 25℃		0.5	0.7	V
V_{T+}−V_{T-}	Hysteresis, X_{IN}	V_{CC} = 5V, T_a = 25℃	0.1		0.5	V
I_{IL}	Input leak current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $\overline{INT}$, CNTR	V_{CC} = 5V, T_a = 25℃, 0 ≦ V_I ≦ 12V	−12		12	μA
I_{IL}	Input leak current, $P3_0$~$P3_7$, R_0~R_3, CNV_{SS}, $\overline{RESET}$, X_{IN}, D_0~D_7	V_{CC} = 5V, T_a = 25℃, 0 ≦ V_I ≦ 5V	−5		5	μA
I_{CC}	Supply current	V_{CC} = 5V, T_a = 25℃, Connect $P3_0$~$P3_7$ to V_{CC}, open the output pin, and connect the input pin and input/output pin, other than $P3_0$~$P3_7$, to V_{SS}.		3	6	mA

M50742-PGYS

PIGGYBACK for M50742-XXXSP, M50708-XXXSP

DESCRIPTION

The M50742-PGYS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M50742-XXXSP/M50708-XXXSP. The M50742-PGYS, being housed in a piggyback-type 64-pin shrink DIP, is compatible with the M50742-XXXSP/M50708-XXXSP.

There is a 28-pin socket on the upper surface so that the M5L2764K or the M5L27128K EPROM may be used.

The M50742-PGYS simplifies the development of programs for the M50742-XXXSP/M50708-XXXSP and is excellent for making prototypes.

DISTINCTIVE FEATURES

- Differences with the M50742-XXXSP/M50708-XXXSP are:

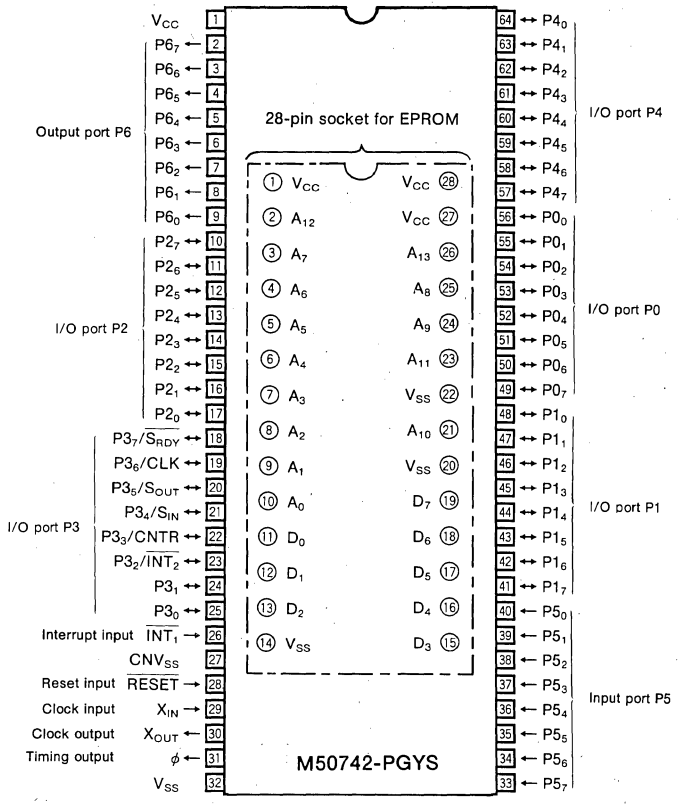
(1) ROMless, EPROM is attached externally

(2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

Development of programs for VCR, tuners, and audio equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol "○" indicates sockets for EPROM.

MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an I/O pin for the timer X.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest order interrupt input pin ($\overline{INT_2}$), respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is P-channel open drain.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
$P6_0$~$P6_7$	Output port P6	Output	Port P6 is an 8-bit output port. The output structure is N-channel open drain.
A_0~A_{13}	Output port A	Output	Port A is for addresses to an EPROM mounted on the top of the package.
D_0~D_7	Input port D	Input	Port D is for input data from an EPROM mounted on the top of the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M50742-PGYS and the M50742-XXXSP/M50708-XXXSP are explained below. As all other points are the same, only the differences are explained.

MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is $E000_{16}$ to $FFFF_{16}$, having 8K bytes. Other than this, the M50742-PGYS has the same functions as the M50742-XXXSP/M50708-XXXSP have.

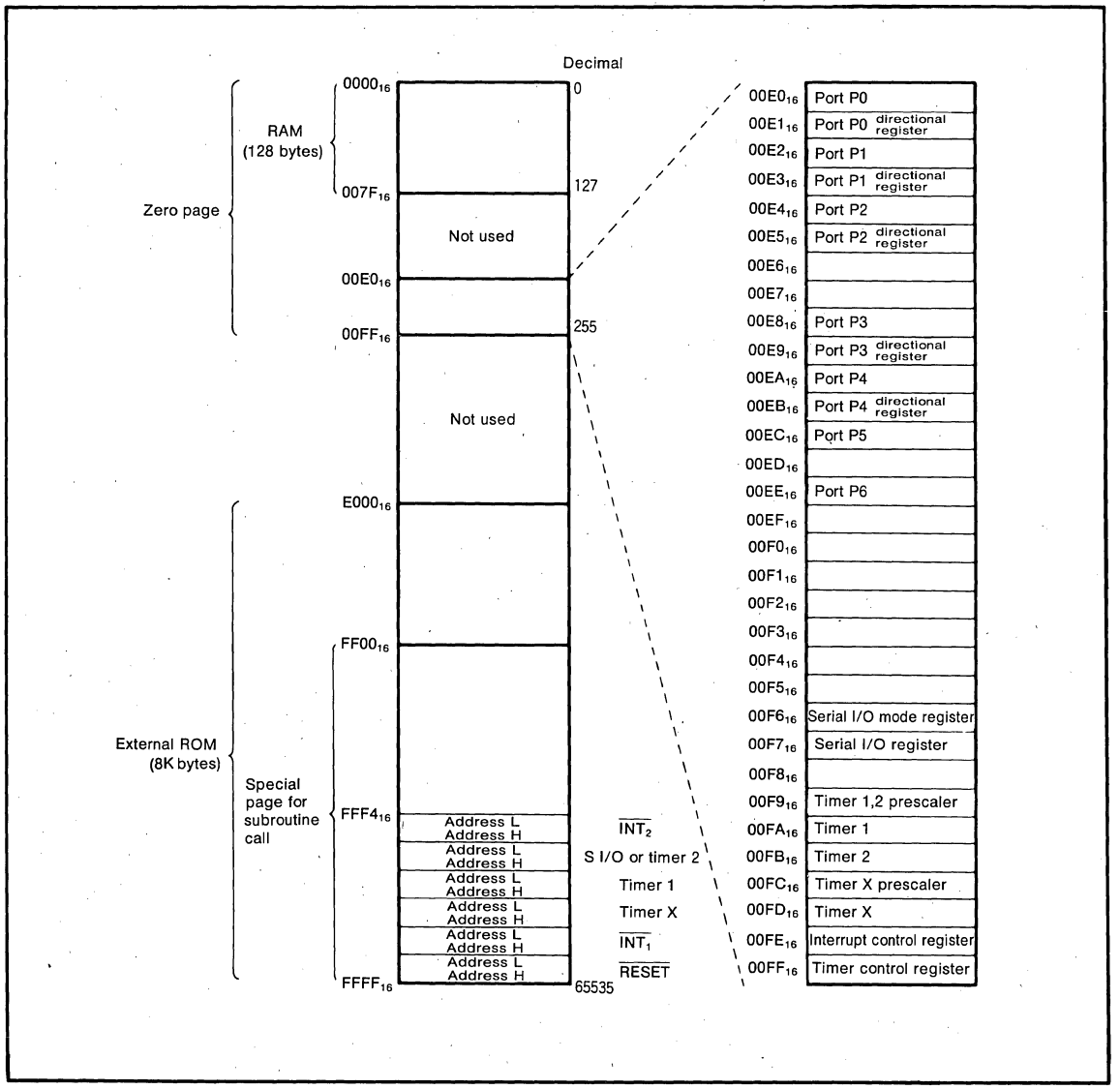


Fig.1 Memory map

PROCESSOR MODE

External memory area differs from the M50742-XXXSP/M50708-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50742-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50742-XXXSP/M50708-XXXSP.

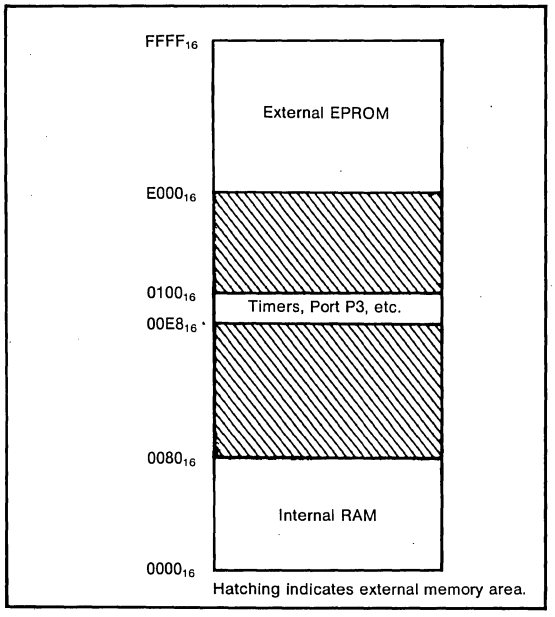


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) When developing programs with the M50742-PGYS use the ROM area from $F000_{16}$ to $FFFF_{16}$ as the capacity of the M50742-XXXSP/M50708-XXXSP ROM is 4k bytes.
(In the case of the M5L2764K and the M5L27128K use the areas from 1000_{16} to $1FFF_{16}$ and from 3000_{16} to $3FFF_{16}$, respectively.)

(2) The M50742-PGYS has no options as the M50742-XXXSP/M50708-XXXSP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} pin. Output transistor off.	−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}, D_0∼D_7		−0.3∼7	V
V_I	Input voltage $P4_0$∼$P4_7$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$		−0.3∼11	V
V_I	Input voltage CNV_{SS}		−0.3∼13	V
V_O	Output voltage $P4_0$∼$P4_7$, X_{OUT}, ϕ, A_0∼A_{13}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P6_0$∼$P6_7$		−0.3∼11	V
P_d	Power dissipation	T_a = 25℃	1000	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −10~70℃, V_{CC} = 5V±5%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage D_0~D_7	0.45V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
V_{IL}	"L" input voltage D_0~D_7	0		0.15V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P6_0$~$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P6_0$~$P6_7$ (Note 1)			5	mA
$I_{OH(peak)}$	"H" peak output current $P4_0$~$P4_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P4_0$~$P4_7$, (Note 1)			−5	mA
$f(X_{IN})$	Internal clock oscillating frequency			4	MHz

Note 1 : The average values of output currents $I_{OL(avg)}$, $I_{OH(avg)}$ are the average values taken over a period of 100ms.
2 : Ports P0, P1, P2, P3, P5, and $\overline{INT_1}$ can be input with high-level voltages up to 9V.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{SS} = 0V, T_a = 25℃, $f(X_{IN})$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P4_0$~$P4_7$	I_{OH} = −10mA	3			V
V_{OH}	"H" output voltage ϕ, A_0~A_{13}	I_{OH} = −2.5mA	3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P6_0$~$P6_7$	I_{OL} = 10mA			2	V
V_{OL}	"L" output voltage ϕ, A_0~A_{13}	I_{OL} = 5mA			2	V
V_{T+}−V_{T-}	Hysteresis $P3_6$	When used as CLK input	0.3		1	V
V_{T+}−V_{T-}	Hysteresis $\overline{INT_1}$		0.3		1	V
V_{T+}−V_{T-}	Hysteresis $P3_2$	When used as $\overline{INT_2}$ input	0.3		1	V
V_{T+}−V_{T-}	Hysteresis $P3_3$	When used as CNTR input	0.3		1	V
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$			0.5	0.7	V
V_{T+}−V_{T-}	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	V_I = 0V			−5	μA
I_{IL}	"L" input current $P4_0$~$P4_7$	V_I = 0V			−5	μA
I_{IL}	"L" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, D_0~D_7	V_I = 0V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	V_I = 9V			9	μA
I_{IH}	"H" input current $P4_0$~$P4_7$	V_I = 5V			5	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, D_0~D_7	V_I = 5V			5	μA
I_{CC}	Supply current	$P4_0$~$P4_7$ are connected to V_{CC}; output pins are open; input and input/output pins other than $P4_0$~$P4_7$ are connected to V_{SS}.		3	6	mA

Note 3 : Limit the sum $I_{OL(peak)}$ of ports P0, P1, P2, P3, and P6 to less than 80mA.

M50743-PGYS

PIGGYBACK for M50743-XXXSP

DESCRIPTION

The M50743-PGYS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputer M50743-XXXSP. The M50743-PGYS, being housed in a piggyback-type 64-pin shrink DIP, is compatible with the M50743-XXXSP.

There is a 28-pin socket on the upper surface so that the M5L2764K or the M5L27128K EPROM may be used.

The M50743-PGYS simplifies the development of programs for the M50743-XXXSP and is excellent for making prototypes.

DISTINCTIVE FEATURES

- Differences with the M50743-XXXSP are:

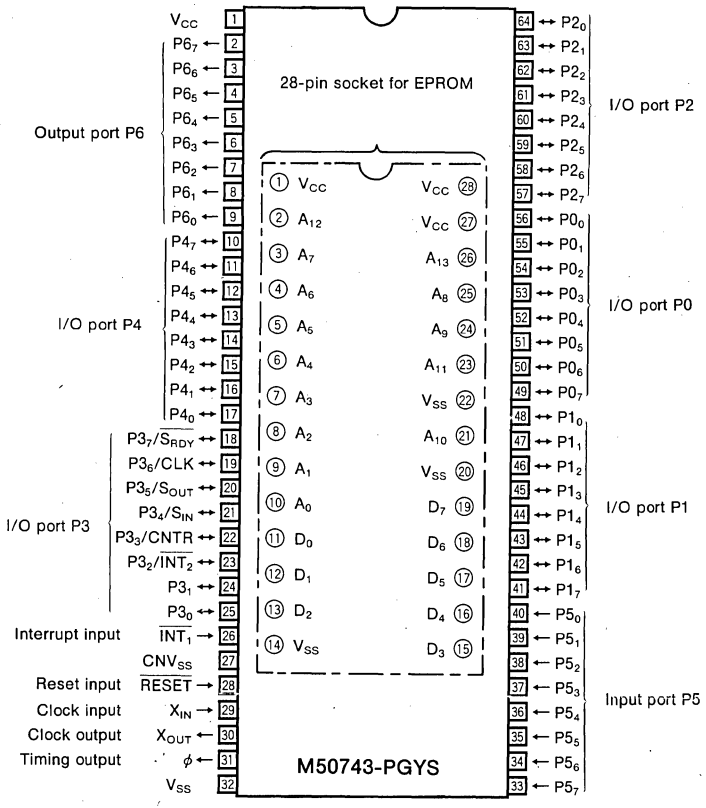
(1) ROMless, EPROM is attached externally

(2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

Development of programs for VCR, tuners, and audio equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol "○" indicates sockets for EPROM.

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an output pin for the timer X.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest order order interrupt input pin ($\overline{INT_2}$), respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
$P6_0$~$P6_7$	Output port P6	Output	Port P6 is an 8-bit output port. The output structure is CMOS output.
A_0~A_{13}	Output port A	Output	Port A outputs to the address of the EPROM mounted on top of the package.
D_0~D_7	Input port D	Input	Port D inputs from the address of the EPROM mounted on top of the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M50743-PGYS and the M50743-XXXSP are explained below. As all other points are the same, only the differences are explained.

MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is $E000_{16}$ to $FFFF_{16}$, having 8k bytes. Other than this, the M50743-PGYS has the same functions as the M50743-XXXSP has.

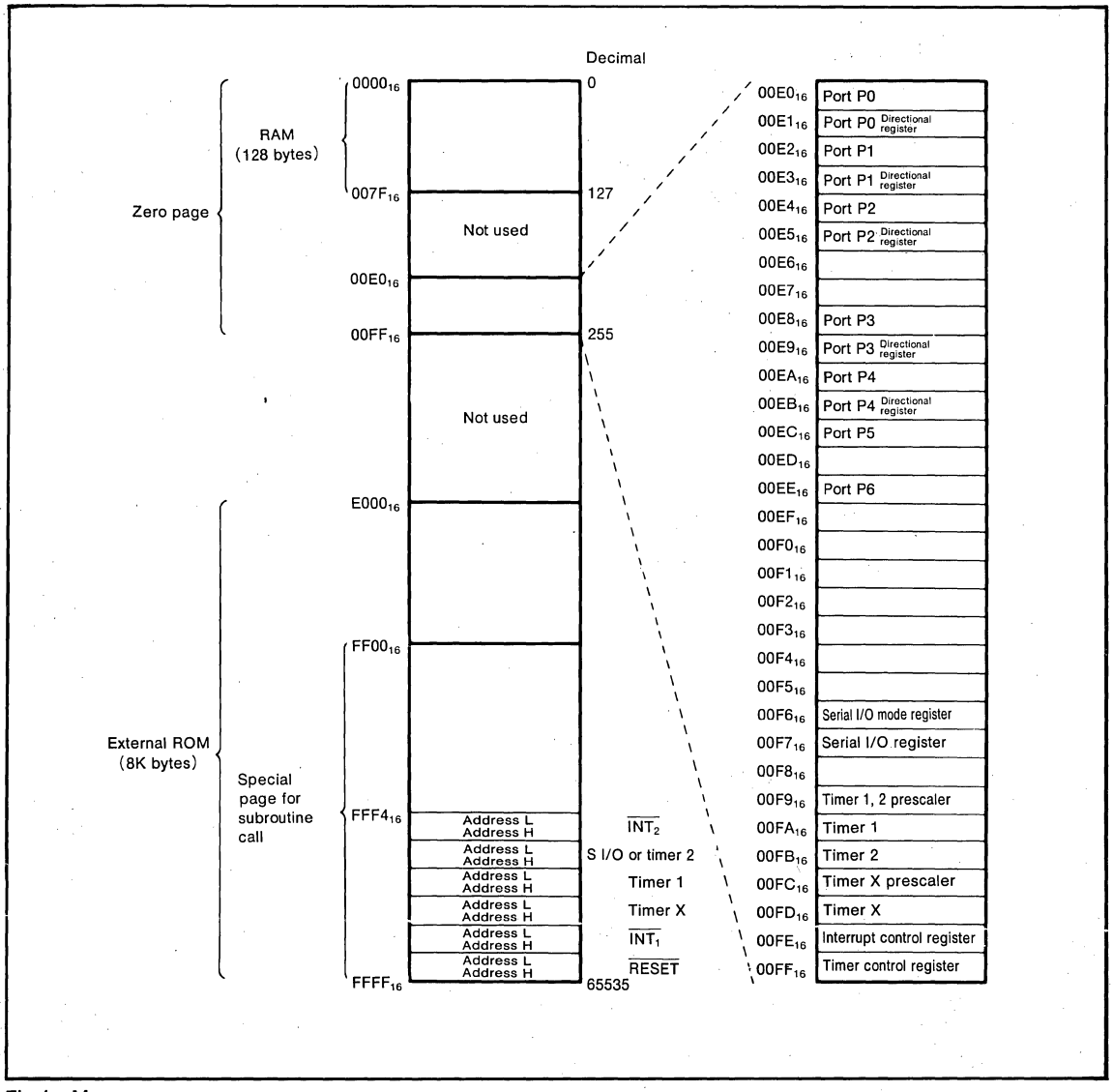


Fig.1 Memory map

PROCESSOR MODE

External memory area differs from the M50743-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50743-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50743-XXXSP.

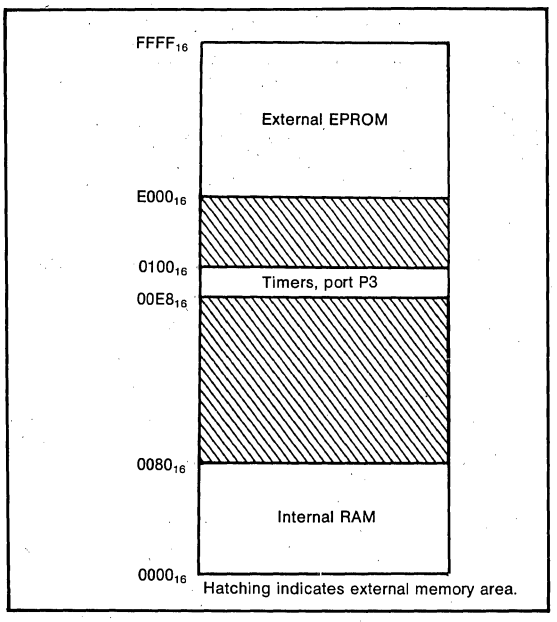


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

When developing programs with the M50743-PGYS, carefully consider the ROM capacity of the M50743-XXXSP.
In the case of the M50743-XXXSP, use the ROM area from $F000_{16}$ to $FFFF_{16}$.
(In the case of the M5L2764K and the M5L27128K use the areas from 1000_{16} to $1FFF_{16}$ and from 3000_{16} to $3FFF_{16}$, respectively.)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} With the output transistor isolated.	−0.3∼7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, $\overline{INT_1}$, $P5_0$∼$P5_7$, D_0∼D_7		−0.3∼7	V
V_I	Input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ $P3_0$∼$P3_7$, $P4_0$∼$P4_7$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage, CNV_{SS}		−0.3∼13	V
V_O	Output voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$ $P4_0$∼$P4_7$, $P6_0$∼$P6_7$, X_{OUT}, ϕ, A_0∼A_{13}		−0.3∼V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
T_{opr}	Operating temperature		−10∼70	℃
T_{stg}	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a = −10~70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$ $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, D_0~D_7	0.45V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$ $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	0		0.16V_{CC}	V
V_{IL}	"L" input voltage, D_0~D_7	0		0.15V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$~$P0_7$, $P1_0$~$P1_7$ $P2_0$~$P2_7$, $P3_0$~$P3_7$ $P4_0$~$P4_7$, $P6_0$~$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$~$P0_7$, $P1_0$~$P1_7$ $P2_0$~$P2_7$, $P3_0$~$P3_7$ $P4_0$~$P4_7$, $P6_0$~$P6_7$ (Note 1)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$~$P0_7$, $P1_0$~$P1_7$ $P2_0$~$P2_7$, $P3_0$~$P3_7$ $P4_0$~$P4_7$, $P6_0$~$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$~$P0_7$, $P1_0$~$P1_7$ $P2_0$~$P2_7$, $P3_0$~$P3_7$ $P4_0$~$P4_7$, $P6_0$~$P6_7$ (Note 1)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			8	MHz

Note 1 : The average output currents $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.

2 : Do not allow the combined current of the fllowing ports to exceed stated values.
$I_{OL(peak)}$ of P0, P1, P2, P3, P4 and P6 not to exceed 80mA. $I_{OH(peak)}$ of P2 not to exceed 50mA.
$I_{OH(peak)}$ of P0 and P1 not to exceed 30mA. $I_{OH(peak)}$ of P3, P4 and P6 not to exceed 30mA.

ELECTRICAL CHARACTERISTICS (T_a = 25℃, V_{CC} = 5V, V_{SS} = 0V, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OH} = −10mA	3			V
V_{OH}	"H" output voltage, ϕ, A_0~A_{13}	I_{OH} = −2.5mA	3			V
V_{OL}	"L" output voltage, $P0_0$~ $P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OL} = 10mA			2	V
V_{OL}	"L" output voltage, ϕ, A_0~A_{13}	I_{OL} = 5mA			2	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_6$	When used as CLK input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{INT_1}$		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_2$	When used as $\overline{INT_2}$ input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_3$	When used as CNTR input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis, X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$ $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN} D_0~D_7	V_I = 0V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$ $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN} D_0~D_7	V_I = 5V			5	μA
I_{CC}	Supply current	Output pins opened, input and input/output pins at V_{SS} and a square wave input at X_{IN}.		6	12	mA

M50745-PGYS

PIGGYBACK for M50745-XXXSP

DESCRIPTION

The M50745-PGYS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputer M50745-XXXSP. The M50745-PGYS, being housed in a piggyback-type 64-pin shrink DIP, is compatible with the M50745-XXXSP.

There is a 28-pin socket on the upper surface so that the M5L2764K or the M5L27128K EPROM may be used.

The M50745-PGYS simplifies the development of programs for the M50745-XXXSP and is excellent for making prototypes.

DISTINCTIVE FEATURES

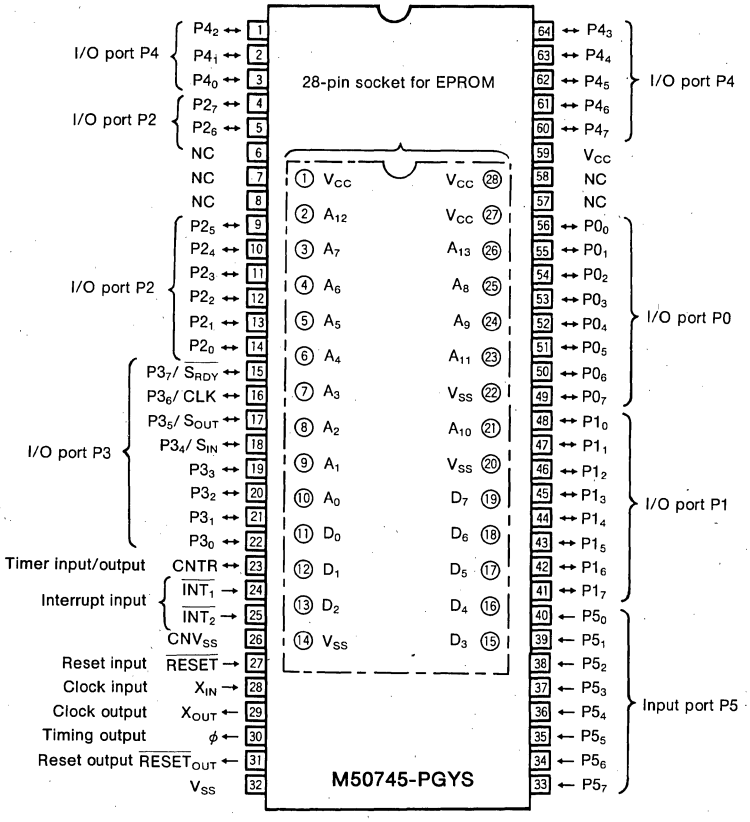
- Differences with the M50745-XXXSP are:

(1) ROMless, EPROM is attached externally.
(2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

Development of programs for VCR, tuners, and audio equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol "○" indicates sockets for EPROM.
NC: No connection.

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an output pin for the timer X.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$\overline{INT_2}$	Interrupt input	Input	This is the lowest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is P-channel open drain.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
$\overline{RESET_{OUT}}$	Reset output	Output	This pin outputs the reset signal for peripheral devices.
A_0~A_{13}	Output port A	Output	Port A outputs to the address of the EPROM mounted on top of the package.
D_0~D_7	Input port D	Input	Port D inputs from the address of the EPROM mounted on top of the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M50745-PGYS and the M50745-XXXSP are explained below. As all other points are the same, only the differences are explained.

MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is $E000_{16}$ to $FFFF_{16}$, having 8K bytes. Other than this, the M50745-PGYS has the same functions as the M50745-XXXSP has.

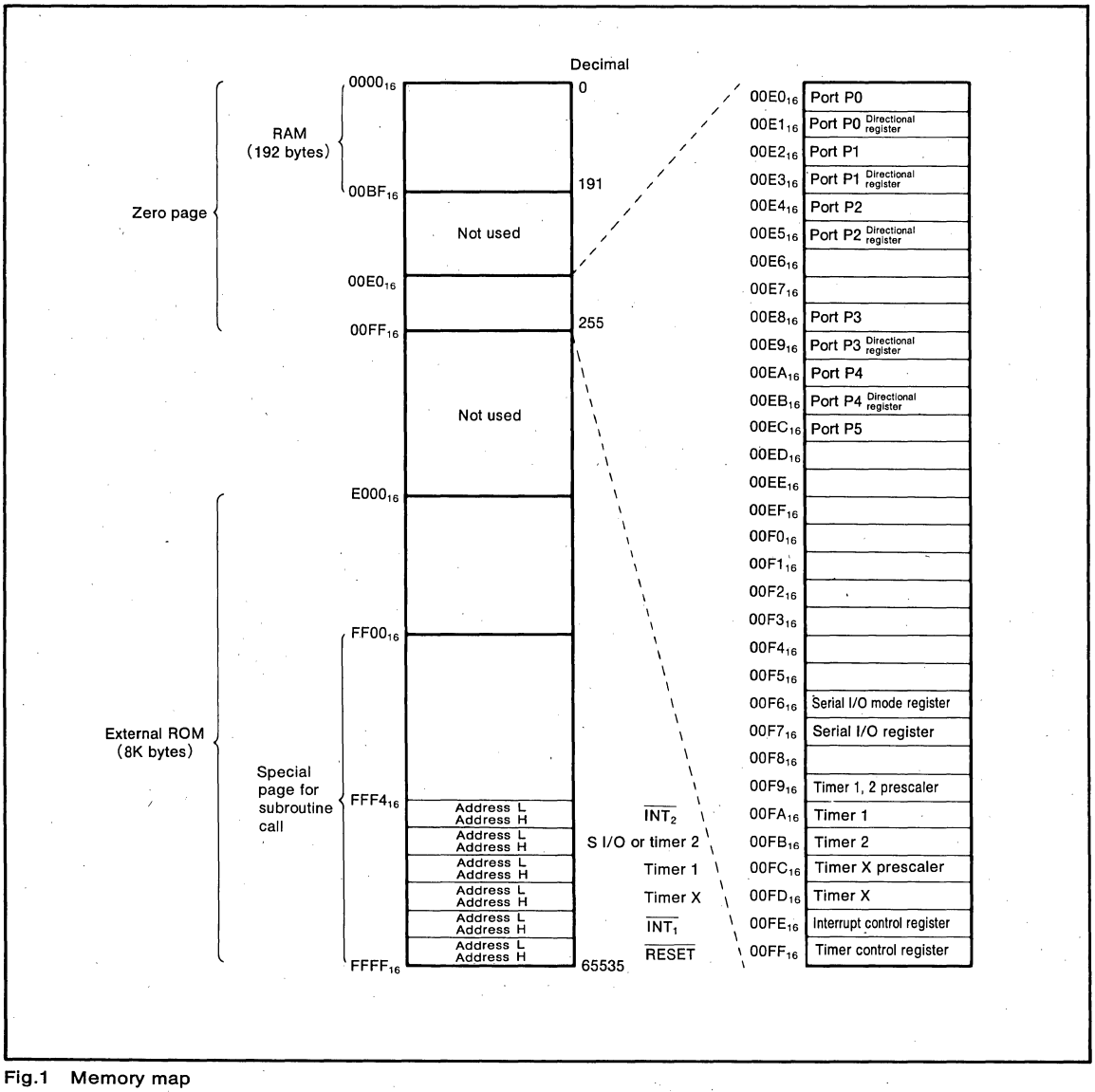


Fig.1 Memory map

MITSUBISHI ELECTRIC

PROCESSOR MODE

External memory area differs from the M50745-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50745-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50745-XXXSP.

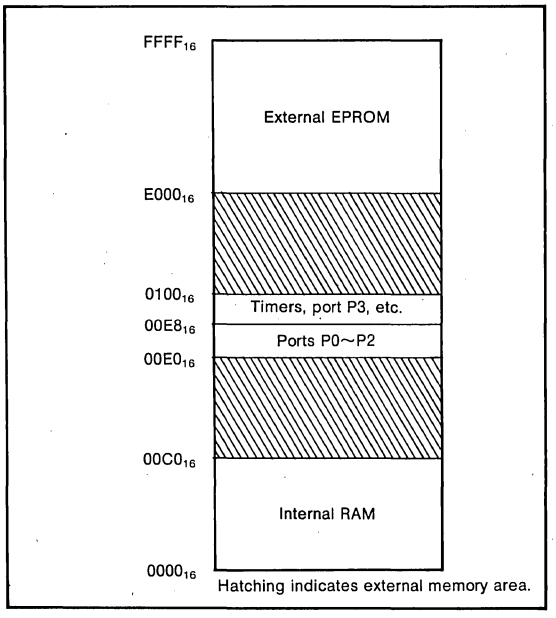


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) When developing programs with the M50745-PGYS, carefully consider the ROM capacity of the M50745-XXXSP.
In the case of the M50745-XXXSP, use the ROM area from $E800_{16}$ to $FFFF_{16}$.
(In the case of the M5L2764K and the M5L27128K use the areas from 0800_{16} to $1FFF_{16}$ and from 2800_{16} to $3FFF_{16}$, respectively.)

(2) The M50745-PGYS has no options as the M50745-XXXSP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} With the ottput transistor isolated.	−0.3~7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, D_0~D_7		−0.3~7	V
V_I	Input voltage, $P4_0$~$P4_7$		−3.0~V_{CC}+0.3	V
V_I	Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}		−0.3~13	V
V_O	Output voltage, $P4_0$~$P4_7$, X_{OUT}, ϕ, $\overline{RESET_{OUT}}$, A_0~A_{13}		−0.3~V_{CC}+0.3	V
V_O	Output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR		−0.3~13	V
P_d	Power dissipation	T_a = 25℃	1000	mW
T_{opr}	Operating temperature		−10~70	℃
Tstg	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a = −10~70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage, D_0~D_7	0.45V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	0		0.16V_{CC}	V
V_{IL}	"L" input voltage, D_0~D_7	0		0.15V_{CC}	V
$f(X_{IN})$	Internal clock oscillating frequency			4	MHz

Note 1 : A high-level input voltage of up to +12V may be applied to ports P0, P1, P2, P3, P5, CNTR, $\overline{INT_1}$ and $\overline{INT_2}$.

ELECTRICAL CHARACTERISTICS (T_a = 25℃, V_{CC} = 5V, V_{SS} = 0V, $f(X_{IN})$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage, $P4_0$~$P4_7$	I_{OH} = −10mA	3			V
V_{OH}	"H" output voltage, ϕ, $\overline{RESET_{OUT}}$, A_0~A_{13}	I_{OH} = −2.5mA	3			V
V_{OL}	"L" output voltage, $P0_0$~ $P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR	I_{OL} = 10mA			2	V
V_{OL}	"L" output voltage, ϕ, $\overline{RESET_{OUT}}$, A_0~A_{13}	I_{OL} = 5mA			2	V
$V_{T+}-V_{T-}$	Hysteresis, $P3_6$	When used as a CLK input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, CNTR, $\overline{INT_1}$, $\overline{INT_2}$		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis, $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis, X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$	V_I = 0V			−5	μA
I_{IL}	"L" input current $P4_0$~$P4_7$	V_I = 0V			−5	μA
I_{IL}	"L" input current CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}, D_0~D_7	V_I = 0V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$	V_I = 12V			12	μA
I_{IH}	"H" input current $P4_0$~$P4_7$	V_I = 5V			5	μA
I_{IH}	"H" input current CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}, D_0~D_7	V_I = 5V			5	μA
I_{CC}	Supply current	$P4_0$ ~ $P4_7$ at V_{CC}, output pins opened, and input and input/output pins other than $P4_0$~ $P4_7$ at V_{SS}.		3	6	mA

M50752-PGYS

PIGGYBACK for M50752-XXXSP, M50757-XXXSP

DESCRIPTION

The M50752-PGYS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M50757-XXXSP/M50752-XXXSP. The M50752-PGYS, being housed in a piggyback-type 52-pin shrink DIP, is compatible with the M50752-XXXSP.

There is a 28-pin socket on the upper surface so that the M5L2732K or the M5L2764K EPROM may be used.

The M50752-PGYS simplifies the development of programs for the M50757-XXXSP/M50752-XXXSP and is excellent for making prototypes.

DISTINCTIVE FEATURES

- Differences with the M50752-XXXSP/M50757-XXXSP are:

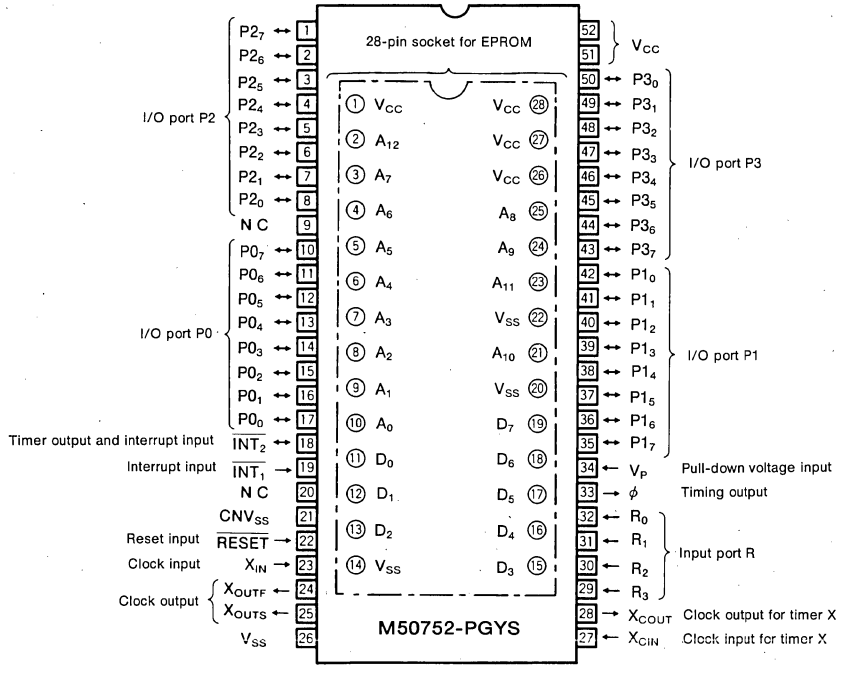
(1) ROMless, EPROM is attached externally

(2) Suitable EPROM is the M5L2732K or the M5L2764K.

APPLICATION

Development of programs for VCR, tuners, and audio equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 52S1M

The symbol "○" indicates socket for EPROM.
NC: No connection.

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P1, P3, $P2_6$ and $P2_7$.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, a resistor is connected between the X_{IN} and X_{OUTS} or the X_{OUTF} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUTS} and X_{OUTF} pins should be left open.
X_{OUTS}	Clock output	Output	This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a resistor between this pin and X_{IN} pin.
X_{OUTF}	Clock output	Output	This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a resistor between this pin and X_{IN} pin.
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock I/O for timer X	Input	These are I/O pins of the clock oscillating circuit for the timer X. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN}pin and X_{COUT} pin.
X_{COUT}		Output	
$\overline{INT_1}$	Interrupt input	Input	This is the lowest order interrupt input pin.
$\overline{INT_2}$	Time output or interrupt input	I/O	This is in common with an output for the time X and an interrupt input pin.
R_0~R_3	Input port R	Input	Port R is a 4-bit input port.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port. The output structure is P-channel open drain.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. For $P2_6$ and $P2_7$ pins, output structure is P-channel open drain, and a pull-down transistor is built in between the V_P pin.
$P3_0$~$P3_7$	Output port P3	Output	Port P3 is an 8-bit output port and has basically the same functions as port P1.
A_0~A_{12}	Output port A	Output	Port A outputs the address of the EPROM loaded on the top side of the package.
D_0~D_7	Input port D	Input	Port D takes the input data from the EPROM loaded on the top side of the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M50752-PGYS and the M50757-XXXSP/M50752-XXXSP are explained below. As all other points are the same, only the differences are explained.

MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is 0100_{16} to $1FFF_{16}$, having 7936 bytes. Other than this, the M50752-PGYS has the same functions as the M50752-XXXSP has. Actually, ROM area depends on EPROM capacity.

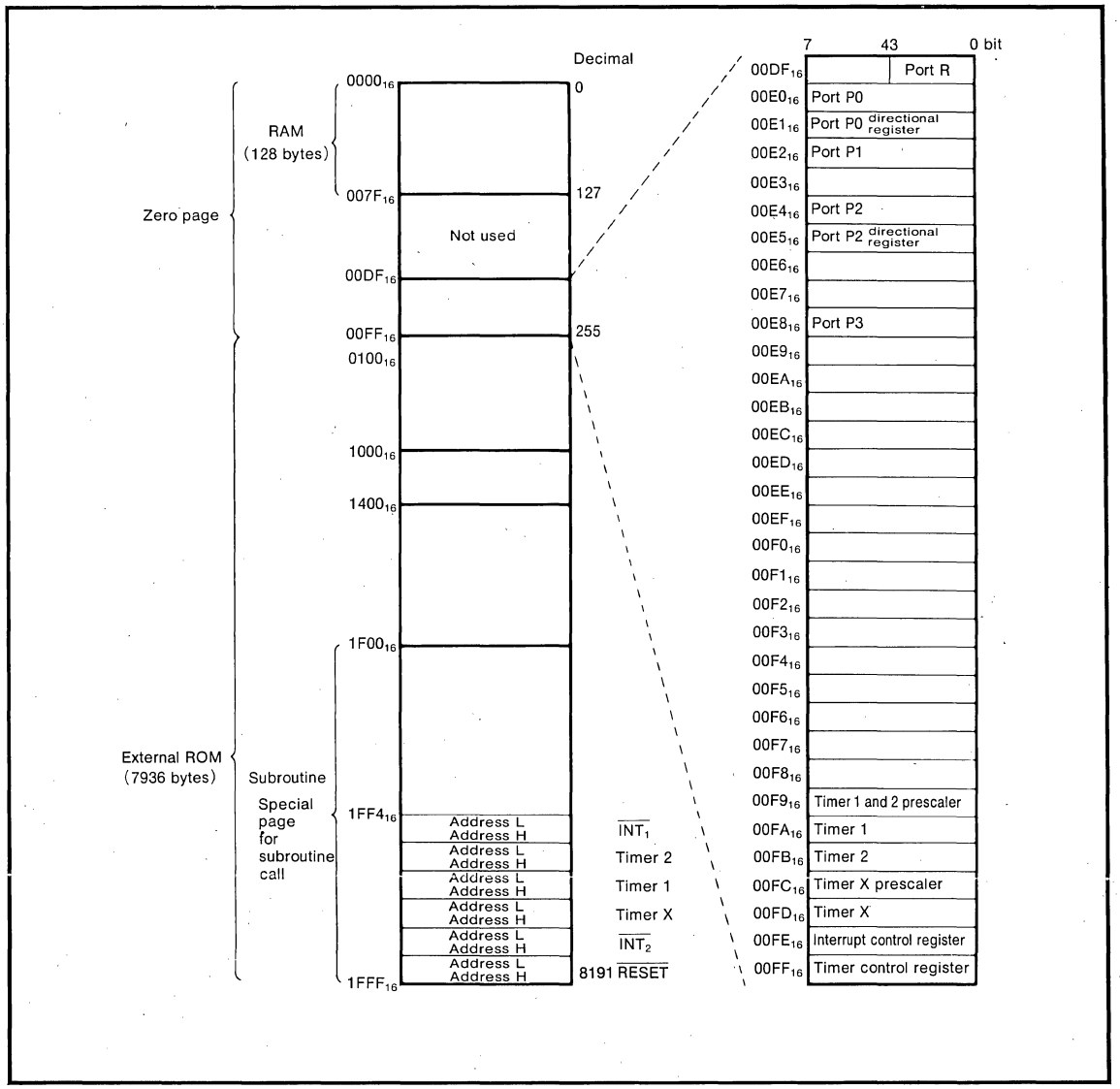


Fig.1 Memory map

PROCESSOR MODE

External memory area differs from the M50757-XXXSP/M50752-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50752-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50757-XXXSP/M50752-XXXSP.

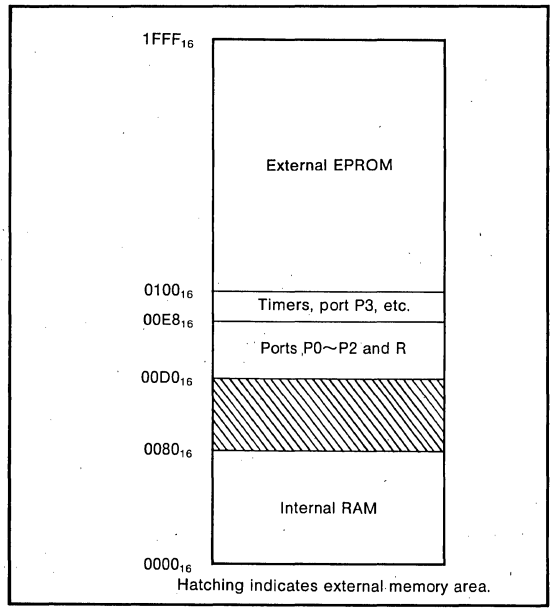


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) Because of the loading of the EPROM, the external dimensions differ from those of the M50757-XXXSP/M50752-XXXSP, being 19.0 × 50.8mm. Lower pin measurements are the same.

(2) When developing programs with the M50752-PGYS, carefully consider the ROM capacity of the M50757-XXXSP/M50752-XXXSP.
In the case of the M50757-XXXSP, use the ROM area from 1400_{16} to $1FFF_{16}$.
(In the case of the M5L2732K use the areas from 0400_{16} to $0FFF_{16}$.)
In the case of the M50752-XXXSP, use the ROM area from 1000_{16} to $1FFF_{16}$.
(In the case of the M5L2732K use the areas from 0000_{16} to $0FFF_{16}$.)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Measured using V_{SS} as standaard. Output transistor is interrupted.	−0.3∼7	V
V_P	Supply voltage		V_{CC}−35∼V_{CC}+0.3	V
V_I	Input voltage R_0∼R_3, CNV_{SS}, $\overline{RESET}$, X_{IN}, X_{CIN}, D_0∼D_7		−0.3∼7	V
V_I	Input voltage $\overline{INT_1}$, $\overline{INT_2}$, $P0_0$∼$P0_7$, $P2_0$∼$P2_5$		−0.3∼13	V
V_O	Output voltage X_{OUTF}, X_{OUTS}, X_{COUT}, ϕ, A_0∼A_{12}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $\overline{INT_2}$, $P0_0$∼$P0_7$, $P2_0$∼$P2_5$		−0.3∼13	V
V_O	Output voltage $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P2_6$, $P2_7$		V_{CC}−35∼V_{CC}+0.3	V
P_d	Power consumption	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−10∼70	℃
T_{stg}	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −10∼70℃ and V_{CC}=5V±5% unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_P	Supply voltage	V_{CC}−33		V_{CC}	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage R_0∼R_3	0.4V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage $\overline{RESET}$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage CNV_{SS}, X_{IN}, X_{CIN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage $\overline{INT_1}$, $\overline{INT_2}$, $P0_0$∼$P0_7$, $P2_0$∼$P2_5$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage D_0∼D_7	0.45V_{CC}		V_{CC}	V
V_{IL}	"L" Input voltage R_0∼R_3, X_{IN}, X_{CIN}	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage CNV_{SS}, $\overline{INT_1}$, $\overline{INT_2}$, $P0_0$∼$P0_7$, $P2_0$∼$P2_5$	0		0.2V_{CC}	V
V_{IL}	"L" Input voltage D_0∼D_7	0		0.15V_{CC}	V
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±5%, V_{SS} = 0V, and $f_{(X_{IN})}$ = 4MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	Output voltage $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P2_6$, $P2_7$	V_{CC}=5V, T_a=25℃ I_{OH}=−12mA	3			V
V_{OH}	Output voltage, ϕ, A_0∼A_{12}	V_{CC}=5V, T_a=25℃ I_{OH}=−2.5mA	3			V
V_{OL}	Output voltage $\overline{INT_2}$, $P0_0$∼ $P0_7$, $P2_0$∼$P2_5$	V_{CC}=5V, T_a=25℃ I_{OL}=10mA			2	V
V_{OL}	Output voltage ϕ, A_0∼A_{12}	V_{CC}=5V, T_a=25℃ I_{OL} = 5mA			2	V
V_{T+}−V_{T-}	Hysteresis $\overline{INT_1}$, $\overline{INT_2}$	V_{CC}=5V, T_a=25℃	0.3		1	V
V_{T+}−V_{T-}	Hysteresis RESET	V_{CC}=5V, T_a=25℃		0.4	0.7	V
I_{IL}	Input leak current P0∼P3, CNV_{SS}, $\overline{RESET}$, X_{IN}, X_{CIN}	V_{CC}=5V, T_a=25℃ 0≦V_I≦5V	−5		5	μA
I_{IL}	Input current $\overline{INT_1}$, $\overline{INT_2}$, D_0∼D_7, $P0_0$∼$P0_7$, $P2_0$∼$P2_5$	V_{CC}=5V, T_a=25℃ 0≦V_I≦5V	−5		5	μA
I_{IL}	Input leak current $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P2_6$, $P2_7$	V_{CC}=5V, T_a=25℃ V_{CC}−33V≦V_I≦V_{CC}	−33		33	μA
I_{CC}	Supply current	V_{CC}=5V, T_a=25℃ $P2_6$ and $P2_7$ are V_{CC}, output pins are left open Input and I/O pins except $P2_6$ and $P2_7$ are V_{SS}		3	6	mA

M50753-PGYS

PIGGYBACK for M50753-XXXSP

DESCRIPTION

The M50753-PGYS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M50753-XXXSP. The M50753-PGYS, being housed in a piggyback-type 64-pin shrink DIP, is compatible with the M50753-XXXSP.

There is a 28-pin socket on the upper surface so that the M5L2764K or the M5L27128K EPROM may be used.

The M50753-PGYS simplifies the development of programs for the M50753-XXXSP and is excellent for making prototypes.

DISTINCTIVE FEATURES

- Differences with the M50753-XXXSP are:

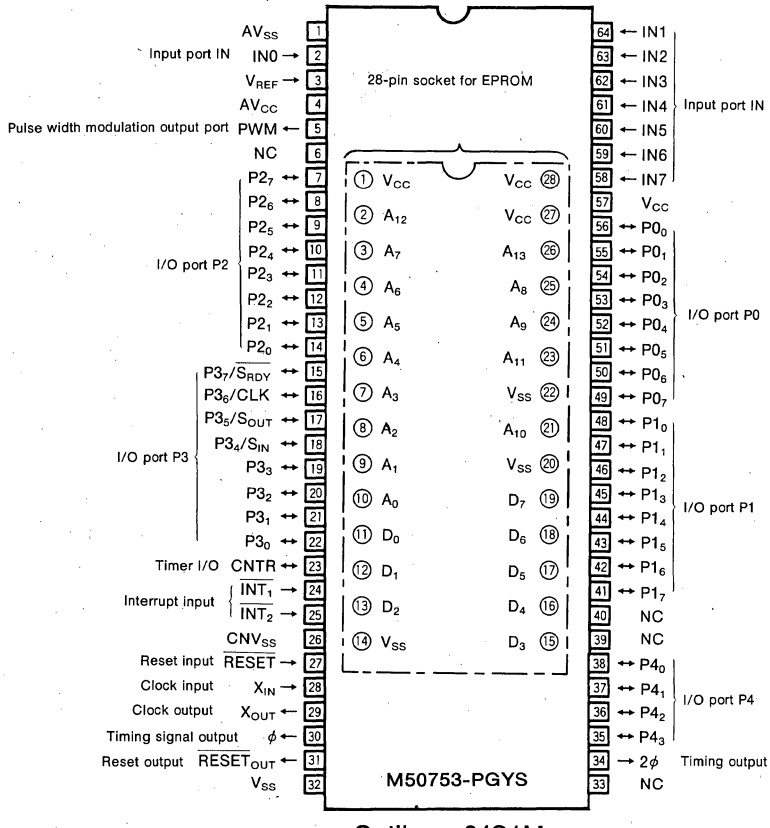
(1) ROMless, EPROM is attached externally

(2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

Development of programs for VCR, tuners, and audio equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol "○" indicates sockets for EPROM.
NC: No connection.

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ, 2ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an I/O pin for the timer X.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
$\overline{INT_2}$	Interrupt input	Input	This is the lowest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively.
$P4_0$~$P4_3$	I/O port P4	I/O	Port P4 is an 4-bit I/O port and has basically the same functions as port P0.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port.
PWM	PWM output	Output	This is output pin from the pulse width modulator. The output structure is N-channel open drain.
$\overline{RESET_{OUT}}$	Reset output	Output	This pin outputs the reset signal for peripheral devices.
IN0~IN7	Analog input port IN	Input	This is an 8-bit analog input port for the A-D converter, and can be used as normal input port.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin the for the A-D converter.
AV_{CC}	Voltage input for A-D		This is the power supply input pin for the A-D converter.
AV_{SS}	Voltage input for A-D		This is GND input pin for the A-D or D-A converter.
A_0~A_{13}	Output port A	Output	Port A carries the output address to the EPROM loaded on the top side of the package.
D_0~D_7	Input port D	Input	Port D takes the input data from the EPROM loaded on the top side of the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M50753-PGYS and the M50753-XXXSP are explained below. As all other points are the same, only the differences are explained.

MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is $E000_{16}$ to $FFFF_{16}$, having 8K bytes. Other than this, the M50753-PGYS has the same functions as the M50753-XXXSP has.

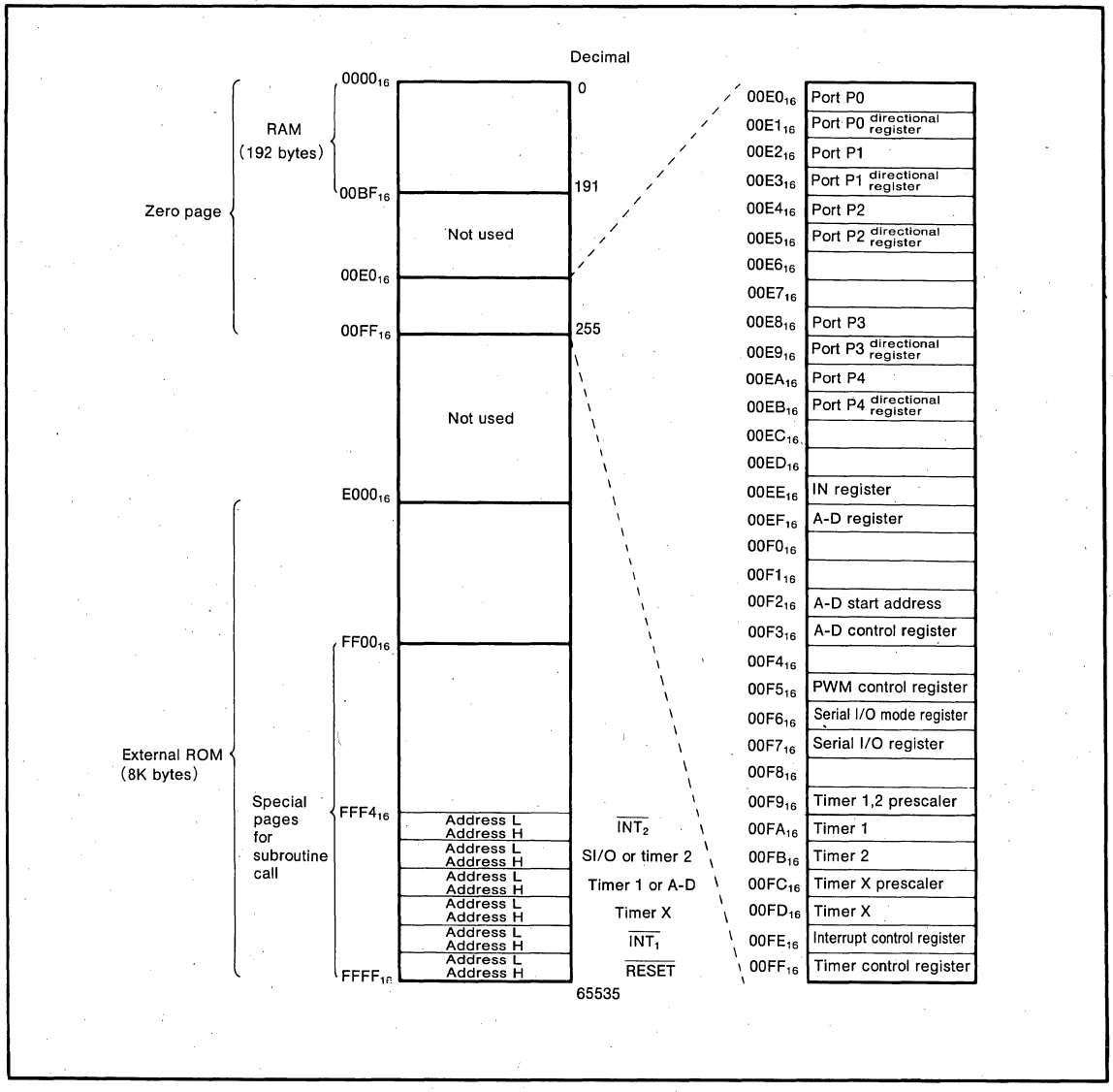


Fig.1 Memory map

PROCESSOR MODE

External memory area differs from the M50753-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50753-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50753-XXXSP.

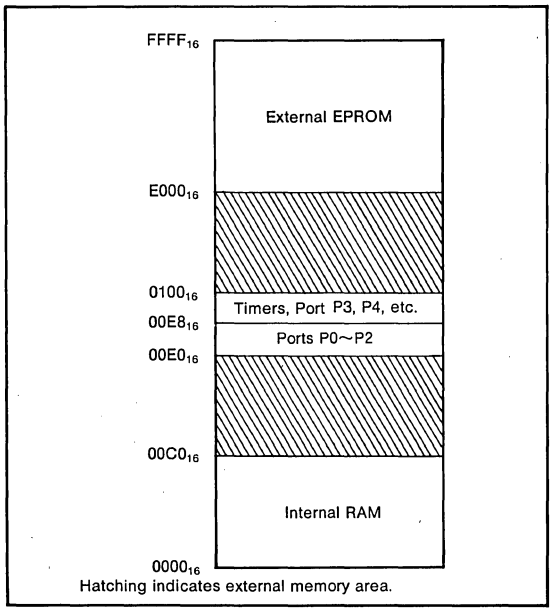


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) When developing programs with the M50753-PGYS, carefully consider the ROM capacity of the M50753-XXXSP.
In the case of the M50753-XXXSP, use the ROM area from $E800_{16}$ to $FFFF_{16}$.
(In the case of the M5L2764K and the M5L27128K use the areas from 0800_{16} to $1FFF_{16}$ and from 2800_{16} to $3FFF_{16}$, respectively.)

(2) The M50753-PGYS has no options as the M50753-XXXSP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Measured using V_{SS} as base. Output transistor is interrupted.	−0.3~7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}, D_0~D_7		−0.3~7	V
V_I	Input voltage IN_0~IN_7		−0.3~V_{CC}+0.3	V
V_I	Input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$ $P4_0$~$P4_3$, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}		−0.3~13	V
V_O	Output voltage X_{OUT}, ϕ, 2ϕ, $\overline{RESET_{OUT}}$, A_0~A_{13}		−0.3~V_{CC}+0.3	V
V_O	Output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, CNTR, PWM		−0.3~13	V
P_d	Power consumption	T_a = 25℃	1000	mW
T_{opr}	Operating temperature		−10~70	℃
T_{stg}	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5% and T_a = −10~70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, IN_0~IN_7 CNTR, $\overline{INT_1}$, $\overline{INT_2}$ $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage D_0~D_7	0.45V_{CC}		V_{CC}	V
V_{IL}	"L" Input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, IN_0~IN_7 CNTR $\overline{INT_1}$, $\overline{INT_2}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage X_{IN}	0		0.16V_{CC}	V
V_{IL}	"L" Input voltage D_0~D_7	0		0.15V_{CC}	V
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

Note 1 : "H" input voltage for ports P_0, P_1, P_2, P_3, P_4 and CNTR, $\overline{INT_1}$ and $\overline{INT_2}$ is up to 12V.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a = 25℃ and $f_{(X_{IN})}$=4MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage ϕ, $\overline{RESET_{OUT}}$, A_0~A_{13}, 2ϕ	I_{OH}=−2.5mA	3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, CNTR, $P4_0$~$P4_3$, PWM	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage ϕ, $\overline{RESET_{OUT}}$, A_0~A_{13}, 2ϕ	I_{OL}=5mA			2	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis CNTR, $\overline{INT_1}$, $\overline{INT_2}$		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, PWM	V_I=0V			−5	μA
I_{IL}	"L" input current IN_0~IN_7	V_I=0V			−5	μA
I_{IL}	"L" input current CNTR, $\overline{INT_1}$, $\overline{INT_2}$ $\overline{RESET}$, X_{IN}, D_0~D_7	V_I=0V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_3$, PWM	V_I=12V			12	μA
I_{IH}	"H" input current IN_0~IN_7	V_I=5V (when not selected)			5	μA
I_{IH}	"H" input current CNTR, $\overline{INT_1}$, $\overline{INT_2}$ $\overline{RESET}$, X_{IN}	V_I=5V			5	μA
I_{IH}	"H" input current V_{REF}	V_I=5V			5	mA
I_{CC}	Supply current	The output pin is left open, P0, P1, P2, P3 and P4 are connected to V_{CC} and all other input and I/O pins are connected to V_{SS}.		3	6	mA
I_{ACC}	A-D supply current	During A/D converter operation		2	4	mA

A-D CONVERTER CHARACTERISTICS (V_{CC}=AV_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25°C and $f_{(X_{IN})}$=4MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=V_{REF}=5.12V			±3	LSB
						LSB
R_{LADDER}	Ladder resistance value		1			kΩ
t_{CONV}	Conversion time				72	μs
V_{REF}	Reference input voltage				V_{CC}	V
V_{IA}	Analog input voltage				V_{REF}	V

M50931-PGYS

PIGGYBACK for M50930-XXXFP ,M50931-XXXFP ,M50932-XXXFP

DESCRIPTION

The M50931-PGYS is an EPROM mounted-type microcomputer which utilizes CMOS technology, and is designed for developing programs for single-chip, 8-bit microcomputers M50930-XXXFP, M50931-XXXFP and the M50932-XXXFP. It is housed in a piggyback-type 80-pin QFP.

There is a 32-pin socket on the package.

The M50931-PGYS simplifies the development of programs for the M50930-XXXFP, M50931-XXXFP, and the M50932-XXXFP and is excellent for making prototypes.

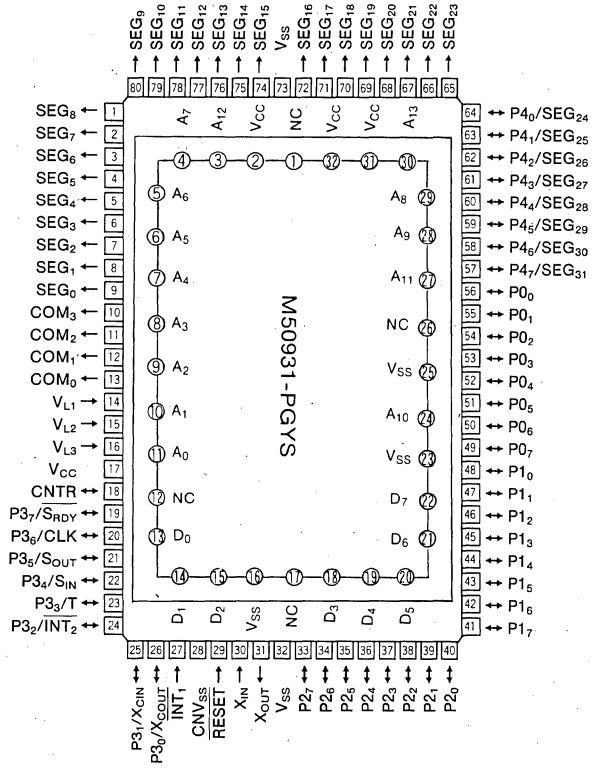
DISTINCTIVE FEATURES

- Diffierence with the M50930-XXXFP, M50931-XXXFP and the M50932-XXXFP are:
  ROMless, EPROM is attached externally.

APPLICATION

Development of programs for office automation equipment, VCR, tuner, audio-visual equipment, and telephone

PIN CONFIGURATION (TOP VIEW)



Outline 80S6M

The symbol "○" indicates sockets for EPROM.
NC: No connection.

MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
INT_1	Interrupt input	Input	This is the highest order interrupt input pin.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$, $P3_2$, $P3_1$, and $P3_0$ work as timer 3 overflow signal divided by 2 output pin (T), $\overline{INT_2}$ pin, X_{CIN} and X_{COUT} pins, respectively.
$P4_0$~$P4_7$	Input port P4	I/O	Port P4 is an 8-bit input port and can be used as segment output pins.
V_{L1}~V_{L3}	Voltage input for LCD	Input	These are voltage input pins for LCD. Supply voltage as $0V \leqq V_{L1} \leqq V_{L2} \leqq V_{L3} \leqq V_{CC}$. 0~$V_{L3}$V is supplied to LCD.
COM_0 ~COM_3	Common output	Output	These are LCD common output pins. At 1/2 duty, COM_2 and COM_3 pins are not used. At 1/3 duty, COM_3 pin is not used.
SEG_0 ~SEG_{23}	Segment output	Output	These are LCD segment output pins.
CNTR	Timer I/O	I/O	This is an output pin for the timer 4 and 5.
A_0~A_{13}	Output port A	Output	These are for addresses to an EPROM mounted on the package.
D_0~D_7	Input port D	Input	These are for input data from the EPROM mounted on the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M50931-PGYS and the M50930-XXXFP, M50931-XXXFP and the M50932-XXXFP are noted below. The following explanations apply to the M50931-PGYS. Specification variations for other chips are noted accordingly.

MEMORY

The memory map is shown in Figure 1. The M50931-PGYS is mounted an EPROM instead of an internal ROM. The address of an EPROM is from 1000_{16} to $3FFF_{16}$, and this memory size is 12288 bytes. The memory size of a RAM is 512 bytes as same as the M50931-XXXFP or the M50932-XXXFP has.

Other than these, the M50931-PGYS has the same functions as the M50930-XXXFP, M50931-XXXFP or the M50932-XXXFP has.

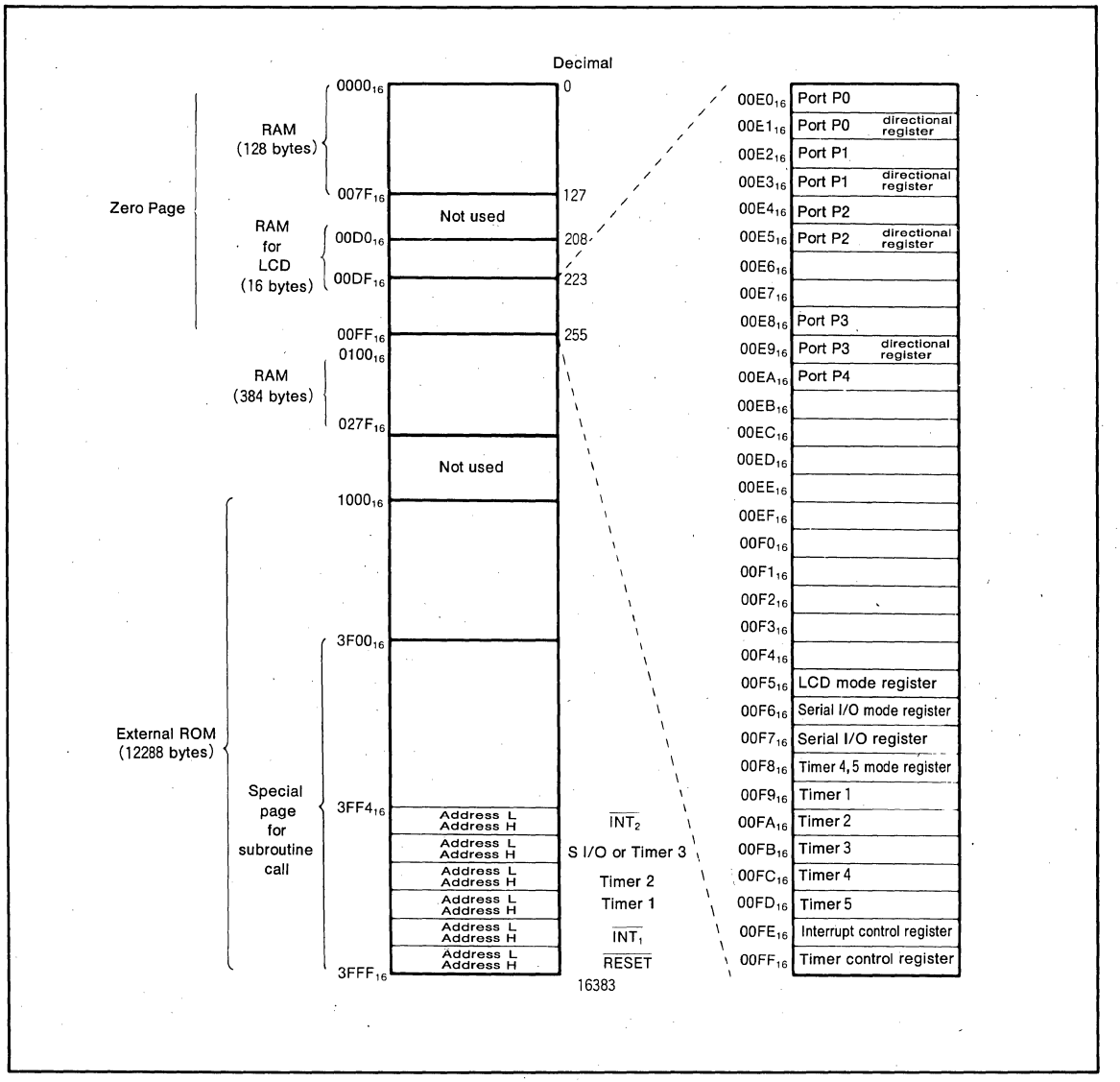


Fig.1 Memory map.

PROCESSOR MODE

External memory area differs from the M50930-XXXFP, M50931-XXXFP and the M50932-XXXFP in the memory expanding mode. And, external memory area differs from only the M50930-XXXFP in microprocessor mode. External memory map is shown in Figure 2.

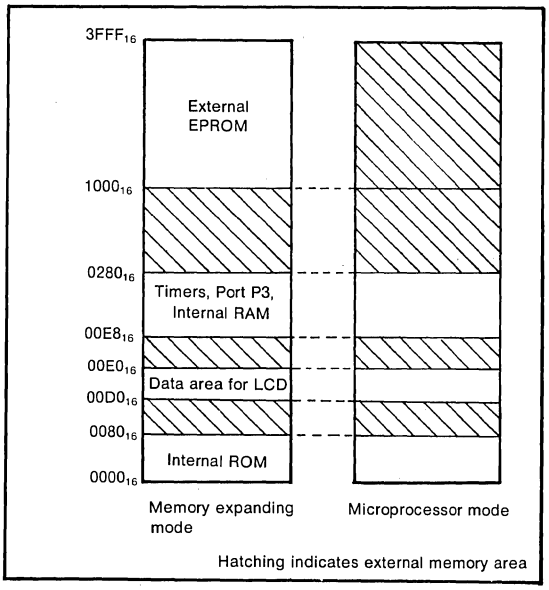


Fig.2 Memory map in memory expanding mode and microprocessor mode

PRECAUTION FOR USE

(1) In case of the MBM27C64-20, the MBM27C64-25, or the MBM27C128-25 EPROM use the following areas (refer to Figure 1):

- For the M50930XXXFP and the M50931-XXXFP, usable ROM area are 3000_{16}~$3FFF_{16}$.

MBM27C64-20, MBM27C64-25·· addresses 1000_{16}~$1FFF_{16}$
MBM27C128-25····· addresses 3000_{16}~$3FFF_{16}$

- For the M50932-XXXFP, usable ROM area are 2000_{16}~$3FFF_{16}$.

MBM27C64-20, MBM27C64-25·· addresses 0000_{16}~$1FFF_{16}$
MBM27C128-25····· addresses 2000_{16}~$3FFF_{16}$

(2) The M50931-PGYS has no options as the M50930-XXXFP, M50931-XXXFP and the M50932-XXXFP. The condition of ports P0~P3 and CNTR is noted below.
P0~P3, CNTR ····· without the pull-up transistor
$P3_5/S_{OUT}$ ····· N-channel open drain output

(3) The way of mounting an EPROM is shown in Figure 3.

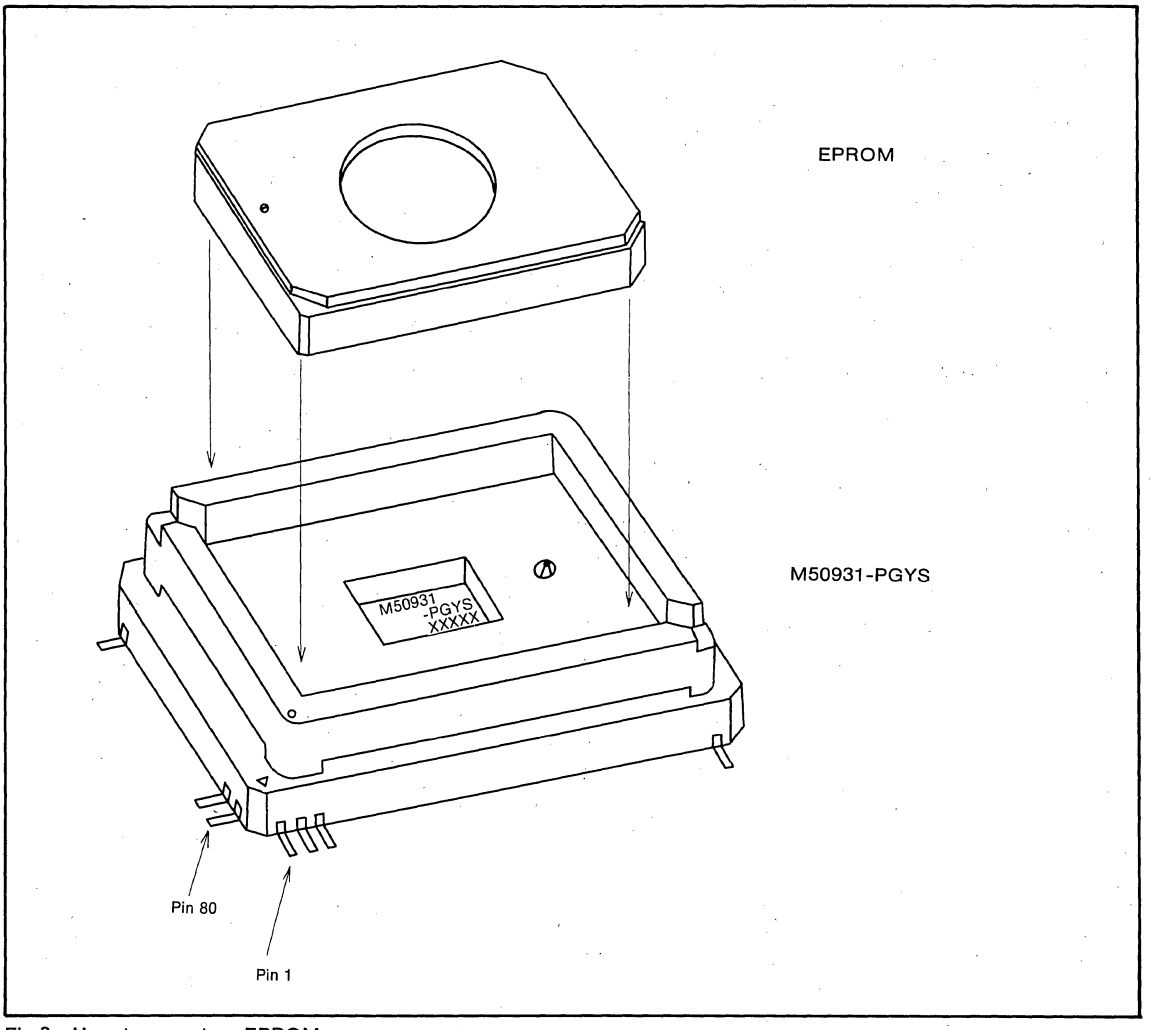


Fig.3 How to mount an EPROM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Output transistor are "off"	−0.3∼7	V
V_I	Supply voltage for LCD V_{L1}∼V_{L3}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, X_{IN}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $\overline{INT_1}$, CNV_{SS}		−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, CNTR		−0.3∼13	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, COM_0∼COM_3, SEG_0∼SEG_{31}, X_{OUT}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage CNTR		−0.3∼7	V
P_d	Power Dissipation	T_a = 25℃	300	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Strage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=3.0(Note 0)∼5.5V, V_{SS}= 0 V, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Nom.	Max.	
V_{CC}	Supply voltage (Note 1)	f(X_{IN})=4.3MHz	4.5		5.5	V
		f(X_{IN})=1.1MHz	3.0(Note 0)		5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ (Note 2), $P3_3$∼$P3_7$ (Note 3), $P4_0$∼$P4_7$, $\overline{RESET}$, X_{IN}, CNV_{SS}		0.7V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$ (Note 4), $\overline{INT_1}$, CNTR		0.74V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ (Note 2), $P3_3$∼$P3_7$ (Note 3), $P4_0$∼$P4_7$, CNV_{SS}		0		0.3V_{CC}	V
V_{IL}	"L" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$ (Note 4), $\overline{INT_1}$, CNTR		0		0.26V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16V_{CC}	V
I_{OH}	"H" Output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$ (Note 5), X_{OUT}				−2	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, X_{OUT}(Note 6)				10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, X_{OUT}(Note 7)				5	mA
f(X_{IN})	Clock oscillating frequency (Note 8)	V_{CC}=4.5∼5.5V	64		4300	kHz
		V_{CC}=2.7∼5.5V	64		1100	
f(X_{CIN})	Clock oscillating frequency for clock function (Note 8)		32		50	kHz

Note 0 Minimum value of V_{CC} is dependent on the EPROM used. At normal temperature, this value is about 2.7∼2.8V. Therefore, 3.0V is dependent on the proper operation of the EPROM at that voltage.
1 When only operating the RAM data retention, minimum value of V_{CC} is 2 V.
2 When using port $P3_1$ as X_{CIN}, 0.85≦V_{CC}≦V_{IH}≦V_{CC}, 0≦V_{IL}≦0.15V_{CC} for port $P3_1$.
3 In this case of using port $P3_6$ as normal input.
4 In this case of using port $P3_6$ as CLK input.
Especially when the input oscillation frequency is more than 50kHz, recommend the following :
0.8V_{CC}≦V_{IH}≦V_{CC}, 0≦V_{IL}≦0.2V_{CC}
5 The total of I_{OH} of port P0, P1, P2, P3 and X_{OUT} should be 35mA max.
6 The total of I_{OL} (peak) of port P0, P1, P2, P3 should be 55mA max, and the total of I_{OL} (peak) of port P3, CNTR, and X_{OUT} should be 45mA max.
7 I_{OL} (avg) is the average current in 100ms.
8 When changing the contents of the most significant bit at address $00F5_{16}$, f(X_{IN}) needs the following range : f(X_{IN})>3f(X_{CIN}).

ELECTRICAL CHARACTERICS (V_{SS}= 0 V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_4$(Note 9), $P3_6$, $P3_7$	V_{CC}=5V, I_{OH}=−2mA		3			V
		V_{CC}=3V, I_{OH}=−0.7mA		2			
V_{OH}	"H" output voltage X_{OUT}	V_{CC}=5V, I_{OH}=−1.5mA		3			V
		V_{CC}=3V, I_{OH}=−0.3mA		2			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$(Note 9), CNTR	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
V_{OL}	"L" output voltage X_{OUT}	V_{CC}=5V, I_{OL}=1.5mA				2	V
		V_{CC}=3V, I_{OL}=0.3mA				1	
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$, CNTR	V_{CC}=5V		0.25		1	V
		V_{CC}=3V		0.15		0.7	
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.4		
$V_{T+}-V_{T-}$	Hysteresis $P3_1$	When used as X_{CIN} input	V_{CC}=5V		0.7		V
			V_{CC}=3V		0.5		
$V_{T+}-V_{T-}$	Hysteresis $P2_0$~$P2_7$, $P3_2$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.4		
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5	0.7	V
		V_{CC}=3V			0.35		
$V_{T+}-V_{T-}$	Hysteresis X_{IN}	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.35		
I_{IL}	"L" input current $P4_0$~$P4_7$ (except reset state) {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR} without pull-up Tr. $\overline{INT_1}$ $\overline{RESET}$, X_{IN}	V_{CC}=5V, V_I=0V				−5	μA
		V_{CC}=3V, V_I=0V				−4	
I_{IL}	"L" input current $P4_0$~$P4_7$ (at reset state)	V_{CC}=5V, V_{L3}=5V, V_I=0V		−30		−140	μA
		V_{CC}=3V, V_{L3}=3V, V_I=0V		−6		−45	
I_{IH}	"H" input current $P4_0$~$P4_7$ (except reset state) $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNTR, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_{CC}=5V, V_I=5V				5	μA
		V_{CC}=3V, V_I=3V				4	
I_{IH}	"H" input current $P4_0$~$P4_7$ (at reset state)	V_{CC}=5V, V_{L3}=5V, V_I=5V				5	μA
		V_{CC}=3V, V_{L3}=3V, V_I=3V				4	
R_{COM}	Output impedance COM_0~COM_3	V_{L1}=V_{CC}/3, V_{L2}=2V_{L1}, V_{L3}=V_{CC} Other COM, SEG pins are opend.	V_{CC}=5V	30	200	2000	Ω
			V_{CC}=3V	70	500	4000	
R_S	Output impedance SEG_0~SEG_{31}		V_{CC}=5V		2		kΩ
			V_{CC}=3V		3		
I_{CC}	Supply current (at operation)	Output pins are opend. $\overline{RESET}$, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, and $P3_0$~$P3_7$ are conected to V_{CC}. Except the above pins are conected to V_{SS}. However, X_{IN} and X_{CIN} are input signal according to the conditions without supply current for EPROM.	f(X_{IN})=4MHz, V_{CC}=5V		3		mA
			f(X_{IN})=1MHz, V_{CC}=3V		0.4		
			T_a=25℃, X_{IN}=0V, f(X_{CIN})=32.8kHz at low power mode (LM_6=1)	V_{CC}=5V	45		μA
				V_{CC}=3V	18		
I_{CC}	Supply current (at wait state)		f(X_{IN})=4MHz, V_{CC}=5V		1		mA
			f(X_{IN})=1MHz, V_{CC}=3V		0.2		
			T_a=25℃, X_{IN}=0V, f(X_{CIN})=32.8kHz at low power mode (LM_6=1)	V_{CC}=5V	20		μA
				V_{CC}=3V	4		
I_{CC}	Supply current		f(X_{IN})=0, f(X_{CIN})=0, V_{CC}=5V	T_a=25℃	0.1		μA
				T_a=70℃			
V_{RAM}	RAM retention voltage		f(X_{IN})=0, f(X_{CIN})=0		2		5.5	V

Note 9 If $P3_0$ is used as X_{COUT}, capability of load driving is lower than the above.

M50941-PGYS

PIGGYBACK for M50940-XXXSP, M50941-XXXSP

DESCRIPTION

The M50941-PGYS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M50940-XXXSP/M50941-XXXSP. The M50941-PGYS, being housed in a piggyback-type 64-pin shrink DIP, is compatible with the M50940-XXXSP/M50941-XXXSP.

There is a 28-pin socket on the upper surface so that the M5L2764K or the M5L27128K EPROM may be used.

The M50941-PGYS simplifies the development of programs for the M50940-XXXSP/M50941-XXXSP and is excellent for making prototypes.

DISTINCTIVE FEATURES

- Differences with the M50940-XXXSP/M50941-XXXSP are:

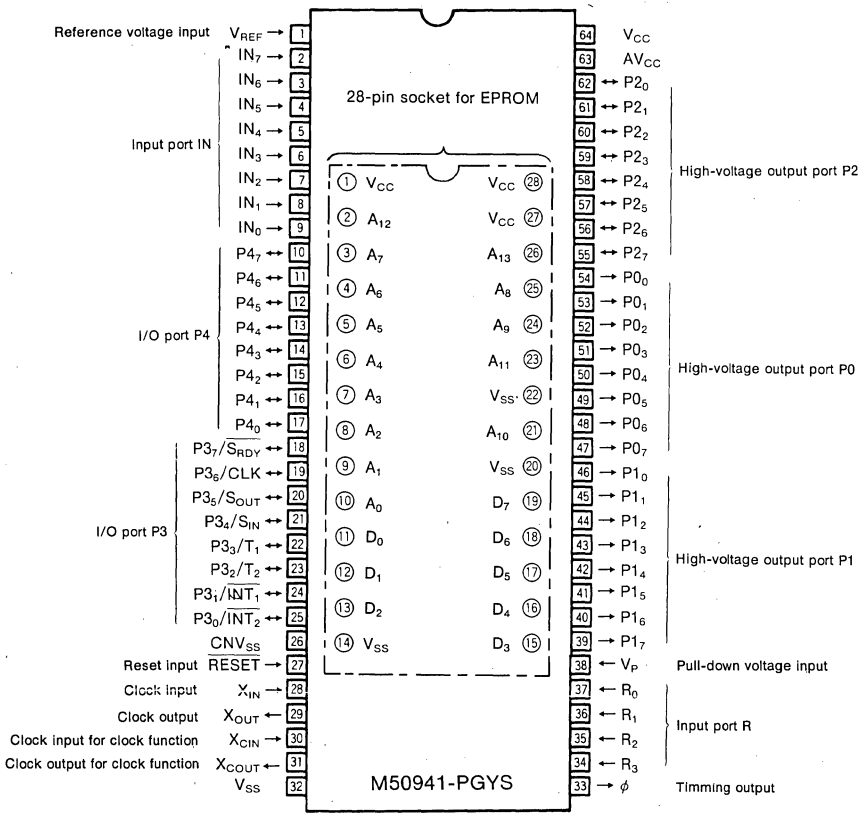
(1) ROMless, EPROM is attached externally

(2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

Development of programs for VCR, tuners, and audio equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol "○" indicates sockets for EPROM.

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P0, P1 and P2.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillatior to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open. This clock can be used as a program controlled the system clock.
X_{COUT}	Clock output for clock function	Output	
$P0_0$~$P0_7$	Output port P0	Output	Port P0 is an 8-bit output port. Output structure is high-voltage P-channel open drain. A pull-down transistor is built in between the V_P pin and this port. At reset, this port is set to a "L" level.
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is P-channel open drain. A pull-down transistor is built in between the V_P pin and this port.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port with CMOS tri-state output. The other functions are basically the same as port P2. Pins $P3_0$, $P3_1$, $P3_2$ and $P3_3$ pins are in common with $\overline{INT_2}$, $\overline{INT_1}$, T_2, and T_1, respectively. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN}, pins, respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port with CMOS tri-state output. The other functions are basically the same as port P2.
R_0~R_3	Input port R	Input	Port R is a 4-bit input port.
IN_0~IN_7	Analog input port IN	Input	Port IN is the analog input pin to the A-D converter. It also has a dual function and works as a normal input port.
AV_{CC}	Voltage input for A-D		This is the power supply input pin for the A-D conveter.
V_{REF}	Reference voltage Input	Input	This is the reference voltage input pin for the A-D conveter.
A_0~A_{13}	Output port A	Output	Port A outputs the addresses to the EPROM mounted on the top of the package.
D_0~D_7	Input port D	Input	Port D takes the input data from the EPROM mounted on the top of the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M50941-PGYS and the M50940-XXXSP/M50941-XXXSP are explained below. As all other points are the same, only the differences are explained.

MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is $C000_{16}$ to $FFFF_{16}$, having 16k bytes. Other than this, the M50941-PGYS has the same functions as the M50940-XXXSP/M50941-XXXSP have.

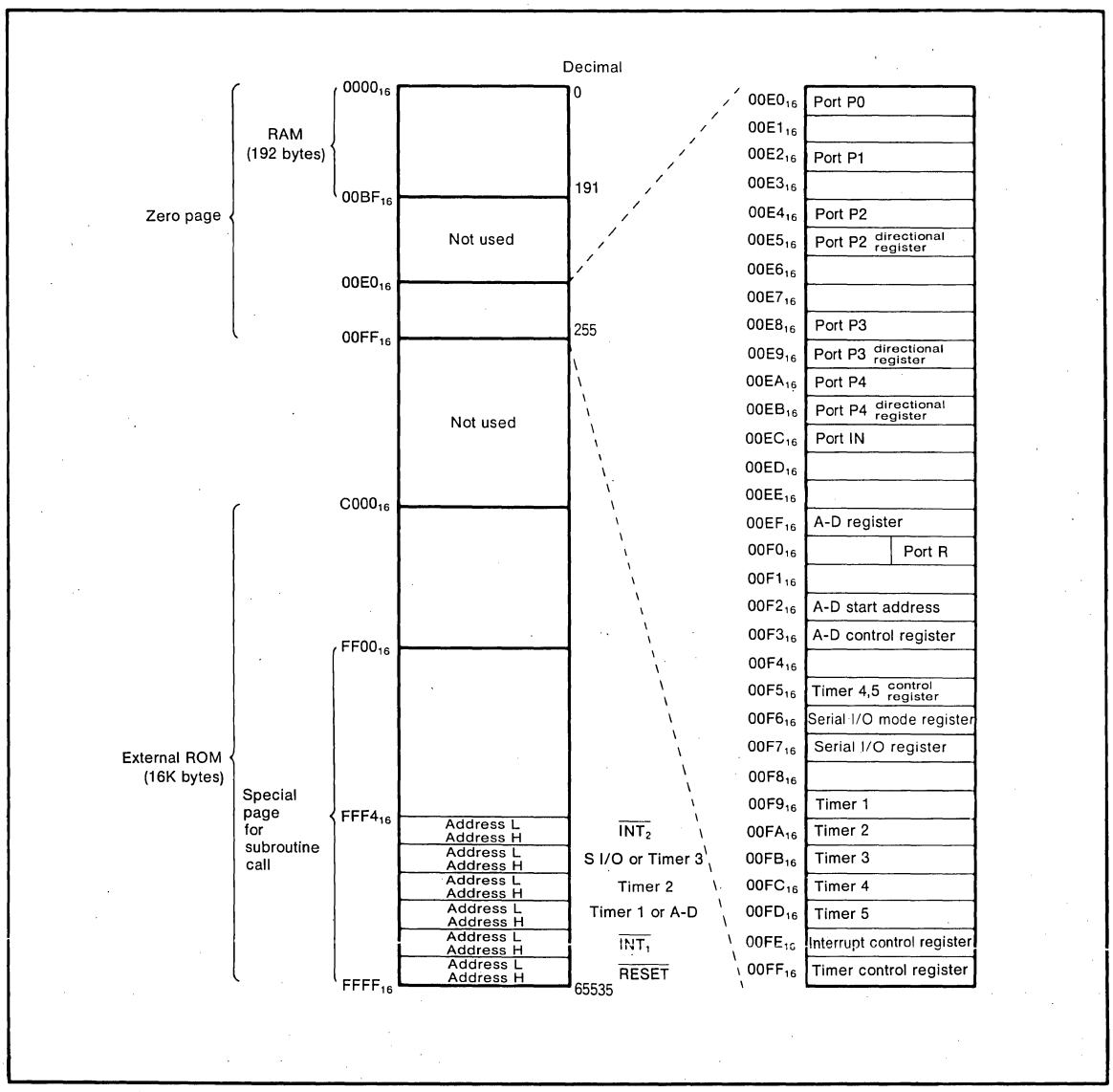


Fig.1 Memory map

PROCESSOR MODE

External memory area differs from the M50940-XXXSP/M50941-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50941-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50940-XXXSP/M50941-XXXSP.

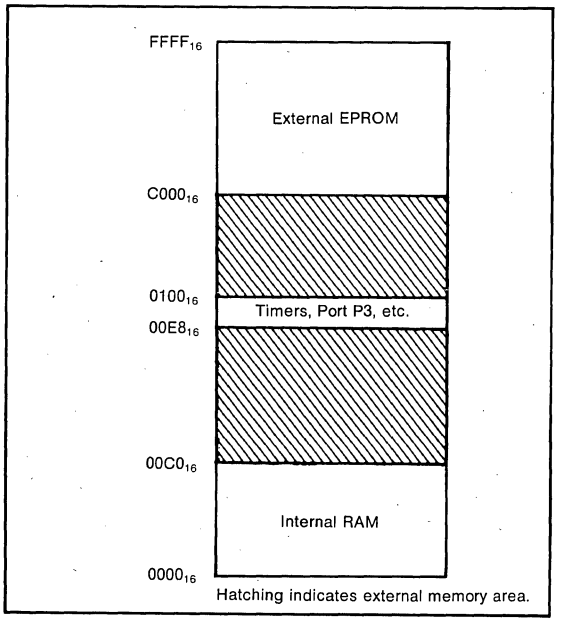


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) When developing programs with the M50941-PGYS, carefully consider the ROM capacity of the M50940-XXXSP/M50941-XXXSP.
In the case of the M50940-XXXSP, use the ROM area from $F000_{16}$ to $FFFF_{16}$.
(In the case of the M5L2764K and the M5L27128K use the areas from 1000_{16} to $1FFF_{16}$ and from 3000_{16} to $3FFF_{16}$, respectively.)
In the case of the M50941-XXXSP, use the ROM area from $E000_{16}$ to $FFFF_{16}$.
(In the case of the M5L2764K and the M5L27128K use the areas from 0000_{16} to $1FFF_{16}$ and from 2000_{16} to $3FFF_{16}$, respectively.)

(2) The M50941-PGYS has no options as the M50940-XXXSP/M50941-XXXSP.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output Transistors are at "OFF" state.	−0.3~7	V
V_P	Pull-down input voltage		V_{CC}−38~V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3~13	V
V_I	Input voltage IN_0~IN_7, R_0~R_3, X_{IN}, X_{CIN}, $\overline{RESET}$, V_{REF}		−0.3~7	V
V_I	Input voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$		−0.3~V_{CC}+0.3	V
V_I	Input voltage $P2_0$~$P2_7$		V_{CC}−38~V_{CC}+0.3	V
V_O	Output voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$, X_{COUT}, X_{OUT}, ϕ		−0.3~V_{CC}+0.3	V
V_O	Output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$		V_{CC}−38~V_{CC}+0.3	V
P_d	Power Dissipation	T_a=25℃	1000	mW
Topr	Operating Temperature		−10~70	℃
Tstg	Storage Temperature		−40~125	℃

RECOMMEND OPERATING CONDITIONS

(V_{CC}=5V±5%, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Nom.	Max.	
V_{CC}	Supply voltage f(X_{IN})=4MHz		4.75	5	5.25	V
V_P	Pull-down supply voltage		V_{CC}−36		V_{CC}	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage Port $P3_0$~$P3_7$, $P4_0$~$P4_7$, IN_0~IN_7, CNV_{SS}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage Port R_0~R_3		0.4V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage Port $P2_0$~$P2_7$		0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage Port $P3_0$~$P3_7$, $P4_0$~$P4_7$, IN_0~IN_7, CNV_{SS}		0		0.2V_{CC}	V
V_{IL}	"L" input voltage Port R_0~R_3		0		0.12V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0.16V_{CC}	V
V_{IL}	"L" input voltage Port $P2_0$~$P2_7$		V_{CC}−36		0.2V_{CC}	V
$I_{OH(sum)}$	"H" sum output current Port $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$				−120	mA
$I_{OH(sum)}$	"H" sum output current Port $P3_0$~$P3_7$, $P4_0$~$P4_7$				−30	mA
$I_{OL(sum)}$	"L" sum output current $P3_0$~$P3_7$, $P4_0$~$P4_7$				60	mA
$I_{OH(peak)}$	"H" peak output current Port $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$				−24	mA
$I_{OH(peak)}$	"H" peak output current Port $P3_0$~$P3_7$, $P4_0$~$P4_7$				−10	mA
$I_{OL(peak)}$	"L" peak output current Port $P3_0$~$P3_7$, $P4_0$~$P4_7$				20	mA
$I_{OH(avg)}$	"H" average output current Port $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$				−12	mA
$I_{OH(avg)}$	"H" average output current Port $P3_0$~$P3_7$, $P4_0$~$P4_7$				−5	mA
$I_{OL(avg)}$	"L" average output current Port $P3_0$~$P3_7$, $P4_0$~$P4_7$				10	mA
$f_{(X_{IN})}$	Clock input oscillating frequency	V_{CC}=5V			4.3	MHz
$f_{(X_{CIN})}$	Clock oscillating frequency for clock function	V_{CC}=5V			500	kHz

Note 1. The maximum "H" input voltage for CNV_{SS} is +12V.
2. The duty cycle for these oscillating frequency is 50%.
3. When the low speed mode is used, the clock input oscillating frequency for the timer must satisfy the following expression :
$f(X_{CIN}) < f(X_{IN})/3$
4. The avarage output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms cycle.
5. $f_{(X_{IN})}$ must be less than 50kHz when the external clock is to be used.

ELECTRICAL CHARACTERISTICS (V_{CC}= 5 V±5%, V_{SS}= 0 V, T_a=25℃, f(X_{IN})= 4 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage Port $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_{CC}=5V, I_{OH}=−5mA		3			V
V_{OH}	"H" output voltage ϕ	V_{CC}=5V, I_{OH}=−2.5mA		3			V
V_{OH}	"H" output voltage Port $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$	V_{CC}=5V, I_{OH}=−12mA		3			V
V_{OL}	"L" output voltage Port $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_{CC}=5V, I_{OL}=10mA				2	V
V_{OL}	"L" output voltage ϕ	V_{CC}=5V, I_{OL}=2.5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis $P3_0/\overline{INT_2}$, $P3_1/\overline{INT_1}$	Use as interrupt input	V_{CC}=5V	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$/CLK	Use as CLK input	V_{CC}=5V	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}	V_{CC}=5V		0.1		0.5	V
$V_{T+}-V_{T-}$	Hysteresis X_{CIN}	V_{CC}=5V		0.1		0.5	V
I_{IL}	"L" input current Port $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_I=0V without pull-up T_r.	V_{CC}=5V			−5	μA
		V_I=0V, with pull-up T_r.	V_{CC}=5V	−35	−70	−140	μA
I_{IL}	"L" input current Port IN_0~IN_7	V_I=0V	V_{CC}=5V			−5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}, R_0~R_3	V_I=0V	V_{CC}=5V			−5	μA
I_{IL}	"L" input current $P2_0$~$P2_7$	V_I=0V				−5	μA
		V_I=V_{CC}−36V				−30	μA
I_{IH}	"H" input current Port $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_I=5V, without pull-up transistor				5	μA
I_{IH}	"H" input current Port IN_0~IN_7	V_I=5V, not use as analog input				5	μA
I_{IH}	"H" input current Port $P2_0$~$P2_7$	Reading operation V_I=5V				100	μA
		normal operation V_I=5V				5	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}, R_0~R_3	V_I=5V				5	μA
I_{IH}	"H" input current V_{REF}	V_I=5V				5	mA
I_{OL}	"L" output current Port $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$	V_P=V_{CC}−36V, V_{OL}=V_{CC}		150	500	900	μA
I_{CC}	Supply current	Note 1	X_{IN}=4MHz, V_{CC}=5V		3	6	mA
I_{ACC}	Supply current for A-D	at A-D converting time			2	4	mA

Note 1. Open output ports, V_P=V_{CC}, input port is V_{SS}, at normal operation.

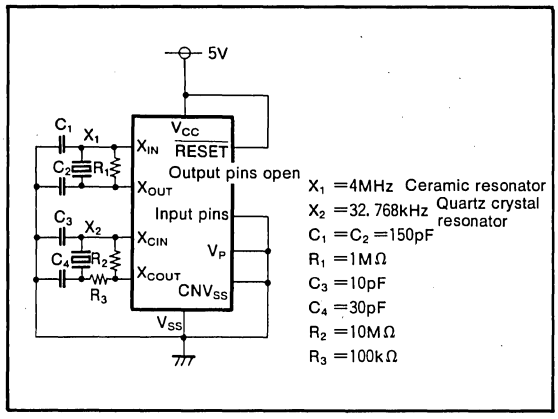


Fig.3 Test circuit for measuring supply current

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Absolute accuracy	V_{CC}=AV_{CC}=V_{REF}=5.12V			±3	LSB
R_{LADDER}	Ladder resistor value		1			kΩ
t_{CONV}	Conversion time	High-speed : ϕ=1MHz			72	μs
		Low-speed : ϕ=1MHz			288	μs
V_{REF}	Reference input voltage				V_{CC}	V
V_{IA}	Analog input voltage				V_{REF}	V

M50950-PGYS

PIGGYBACK for M50950-XXXSP ,M50951-XXXSP

DESCRIPTION

The M50950-PGYS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M50950-XXXSP/M50951-XXXSP. The M50950-PGYS, being housed in a piggyback-type 52-pin shrink DIP, is compatible with the M50950-XXXSP/M50951-XXXSP.

There is a 28-pin socket on the upper surface so that the M5L2764K or the M5L27128K EPROM may be used.

The M50950-PGYS simplifies the development of programs for the M50950-XXXSP/M50951-XXXSP and is excellent for making prototypes.

DISTINCTIVE FEATURES

- Differences with the M50950-XXXSP/M50951-XXXSP are:

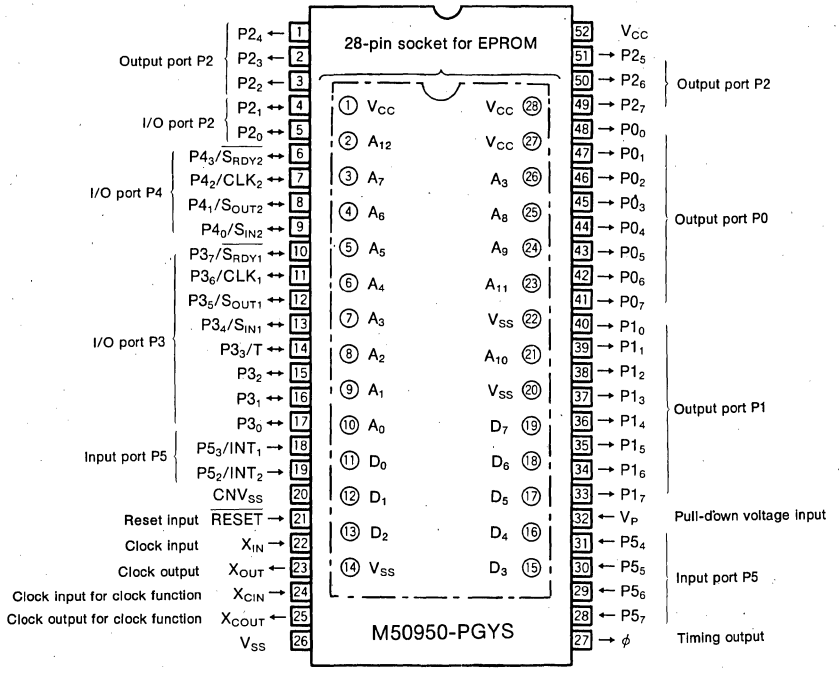
(1) ROMless, EPROM is attached externally

(2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

Development of programs for VTR, tuners, and audio equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 52S1M

The symbol "○" indicates sockets for EPROM.

MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P0, P1 and $P2_2$~$P2_7$.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open. This clock can be used as a program controlled the system clock.
X_{COUT}	Clock output for clock function	Output	
$P0_0$~$P0_7$	Output port P0	Output	Port P0 is an 8-bit output port. Output structure is high-voltage P-channel open drain. A pull-down transistor is built in between the V_P pin and this port. At reset, this port is set to a "L" level.
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is a 2-bit I/O port ($P2_0$, $P2_1$) and a 6-bit high-voltage P-channel outputt port ($P2_2$~$P2_7$). For $P2_0$ and $P2_1$, output structure is N-channel open drain. A pull-down transistor is built in between the V_P pin and $P2_2$~$P2_7$.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port. When serial I/O_1 is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY1}}$, CLK_1, S_{OUT1}, and S_{IN1} pins, respectively. $P3_3$ can be used as programmable output pin for the timer 1 overflow signal divided by 2.
$P4_0$~$P4_3$	I/O port P4	I/O	Port P4 is an 8-bit I/O port. When serial I/O_2 is used, $P4_3$, $P4_2$, $P4_1$, and $P4_0$ work as $\overline{S_{RDY2}}$,CLK_2, S_{OUT2}, and S_{IN2} pins, respectively.
$P5_2/INT_2$ $P5_3/INT_1$	Input port P5	Input	Bits 2 and 3 of port P5 are 2-bit input port and are in common with interrupt inputs.
$P5_4$~$P5_7$		Input	Bits 4~7 of port P5 are 4-bit input port.
A_0~A_{13}	Output port A	Output	Port A outputs the adresses to the EPROM mounted on the top of the package.
D_0~D_7	Input port D	Input	Port D takes the input data from the EPROM mounted on the top of the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M50950-PGYS and the M50950-XXXSP/M50951-XXXSP are explained below. As all other points are the same, only the differences are explained.

MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is $E000_{16}$ to $FFFF_{16}$, having 8K bytes. Other than this, the M50950-PGYS has the same functions as the M50950-XXXSP/M50951-XXXSP has.

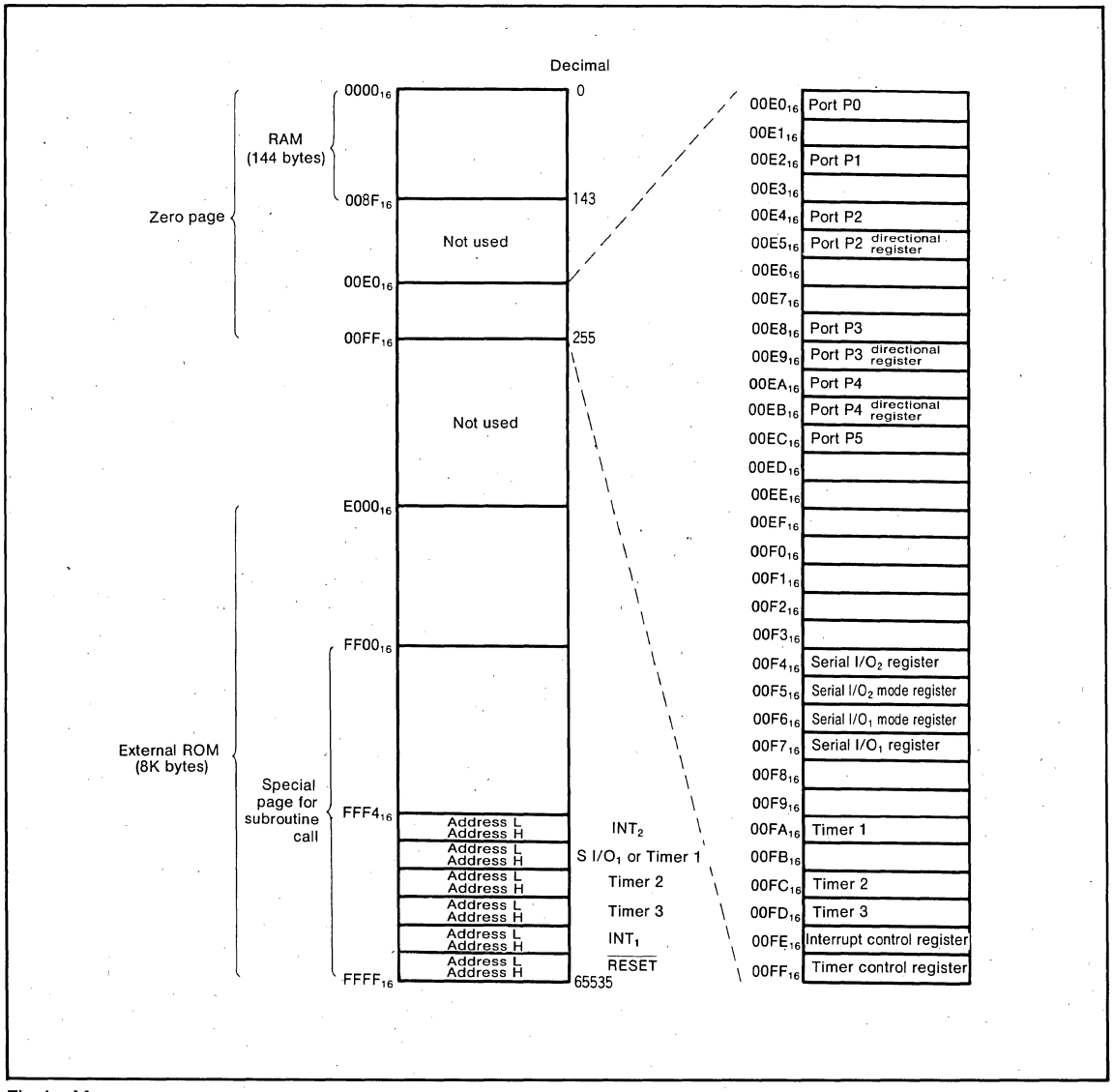


Fig.1 Memory map

MITSUBISHI ELECTRIC

PROCESSOR MODE

External memory area differs from the M50950-XXXSP/M50951-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50950-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50950-XXXSP/M50951-XXXSP.

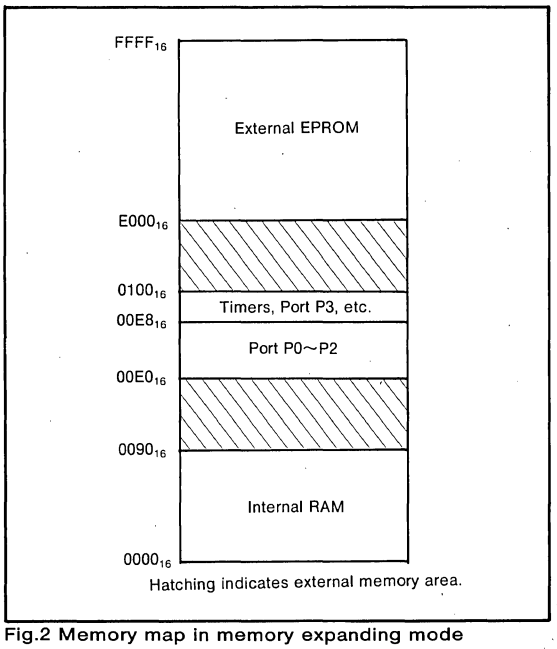


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) Because of the loading of the EPROM, the external dimensions differ from those of the M50950-XXXSP/M50951-XXXSP, being 19.0 × 50.8mm. Lower pin measurements are the same.

(2) When developing programs with the M50950-PGYS, carefully consider the ROM capacity of the M50950-XXXSP/M50951-XXXSP.

In the case of the M50950-XXXSP, use the ROM area from $E800_{16}$ to $FFFF_{16}$.

(In the case of the M5L2764K and the M5L27128K use the areas from 0800_{16} to $1FFF_{16}$ and from 2800_{16} to $3FFF_{16}$, respectively.)

In the case of the M50951-XXXSP, use the ROM area from $F000_{16}$ to $FFFF_{16}$.

(In the case of the M5L2764K and the M5L27128K use the areas from 1000_{16} to $1FFF_{16}$ and from 3000_{16} to $3FFF_{16}$, respectively.)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	−0.3∼7	V
V_P	Pull-down supply voltage		V_{CC}−38∼V_{CC}+0.3	V
V_I	Input voltage $P2_0$, $P2_1$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, CNV_{SS} $P5_2/INT_2$, $P5_3/INT_1$		−0.3∼13	V
V_I	Input voltage $\overline{RESET}$, X_{IN}, X_{CIN}, D_0∼D_7		−0.3∼7	V
V_I	Input voltage $P5_4$∼$P5_7$		−0.3∼7	V
V_O	Output voltage $P2_0$, $P2_1$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$		−0.3∼13	V
V_O	Output voltage X_{OUT}, X_{COUT}, ϕ, A_0∼A_{13}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_2$∼$P2_7$		V_{CC}−38∼V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Nom.	Max.	
V_{CC}	Supply voltage	$f_{(X_{IN})}$=5MHz	4.75	5	5.25	V
V_P	Pull-down supply voltage		V_{CC}−36		V_{CC}	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P2_0$, $P2_1$, $P3_0$∼$P3_7$, CNV_{SS} $P5_2/INT_2$, $P5_3/INT_1$, $P4_0$∼$P4_3$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P5_4$∼$P5_7$		0.4V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage D_0∼D_7		0.45V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P2_0$, $P2_1$, $P3_0$∼$P3_7$, CNV_{SS} $P5_2/INT_2$, $P5_3/INT_1$, $P4_0$∼$P4_3$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16V_{CC}	V
V_{IL}	"L" input voltage X_{CIN}		0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P5_4$∼$P5_7$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage D_0∼D_7		0		0.15V_{CC}	V
$I_{OH(peak)}$	"H" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_2$∼$P2_7$				−24	mA
$I_{OL(peak)}$	"L" peak output current $P2_0$, $P2_1$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$				20	mA
$I_{OH(avg)}$	"H" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_2$∼$P2_7$				−12	mA
$I_{OL(avg)}$	"L" average output current $P2_0$, $P2_1$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$				10	mA
$f_{(X_{IN})}$	Clock input oscillating frequency				5	MHz
$f_{(X_{CIN})}$	Clock oscillating frequency for clock function			32	500	kHz

Note 1 : "H" input voltage of up to +12V may be applied to permissible for ports $P2_0$, $P2_1$, $P3_0$∼$P3_7$, $P5_2$, $P5_3$, $P4_0$∼$P4_3$ and CNV_{SS}.

2 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value of a period of 100ms. On output ports, the total of current dissipation should be 890mW max at T=25℃.

3 : Oscillation frequency is at 50% duty cycle.
When used low-speed mode, clock input oscillating frequency for clock function should be $f(X_{CIN}) < f(X_{IN})/3$.
When used external clock, clock input oscillating frequency for clock function should be $f(X_{CIN}) <$ 50kHz.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=5MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage ϕ, A_0~A_{13}	I_{OH}=−2.5mA, T_a=−10~70℃	3			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_2$~$P2_7$	I_{OH}=−12mA, T_a=−10~70℃	3			V
V_{OL}	"L" output voltage $P2_0$, $P2_1$, $P3_0$~$P3_7$, $P4_0$~$P4_3$	I_{OL}=10mA, T_a=−10~70℃			2	V
V_{OL}	"L" output voltage ϕ, A_0~A_{13}	I_{OL}=2.5mA, T_a=−10~70℃			2	V
$V_{T+}-V_{T-}$	Hysteresis $P5_2/INT_2$, $P5_3/INT_1$		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$, $P4_2$	When used as CLK input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P2_0$, $P2_1$, $P3_0$~$P3_7$, $P4_0$~$P4_3$	V_I= 0 V			−5	μA
I_{IL}	"L" input current $P5_4$~$P5_7$	V_I= 0 V			−5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}, D_0~D_7	V_I= 0 V			−5	μA
I_{IL}	"L" input current $P5_2/INT_2$, $P5_3/INT_1$	V_I= 0 V			−5	μA
I_{IH}	"H" input current $P2_0$, $P2_1$, $P3_0$~$P3_7$, $P4_0$~$P4_3$	V_I= 5 V			5	μA
		V_I=12V			12	μA
I_{IH}	"H" input current $P5_4$~$P5_7$	V_I= 5 V			5	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}, D_0~D_7	V_I= 5 V			5	μA
I_{IH}	"H" input current $P5_2/INT_2$, $P5_3/INT_1$	V_I= 5 V			5	μA
		V_I=12V			12	μA
I_L	Pull-down current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_2$~$P2_7$	V_P=V_{CC}−36V, V_{OL}=V_{CC}	150	450	900	μA
I_{OL}	"L" Pull-down current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_2$~$P2_7$	V_P=V_{CC}−36V, V_{OL}=V_P			−30	μA
V_{RAM}	RAM retention voltage	at clock stop	2		5.5	V
I_{CC}	Supply current	Output pins open (output off) V_{PP}=V_{SS}, Input and I/O pins all at V_{SS} $f_{(X_{IN})}$=5MHz(at system operation)		4	8	mA

M50955-PGYS

PIGGYBACK for M50754-XXXSP,M50954-XXXSP,M50955-XXXSP

DESCRIPTION

The M50955-PGYS is an EPROM mounted-type microcomputer which utilizes CMOS technology, and is designed for developing programs for single-chip 8-bit microcomputer the M50955-XXXSP. It is housed in a piggyback-type 64-pin shrink DIP.

There is a 28-pin socket on the package for the M5L2764K or the M5L27128K EPROM.

The M50955-PGYS simplifies the development of programs for the M50955-XXXSP and is excellent for making prototypes.

The differences among the M50754-XXXSP, M50954-XXXSP, and the M50955-XXXSP are only ROM size.

Therefor the M50955-PGYS can be used for the development of programs for the M50754-XXXSP and the M50954-XXXSP.

DISTINCTIVE FEATURES

- Differences with the M50955-XXXSP are:

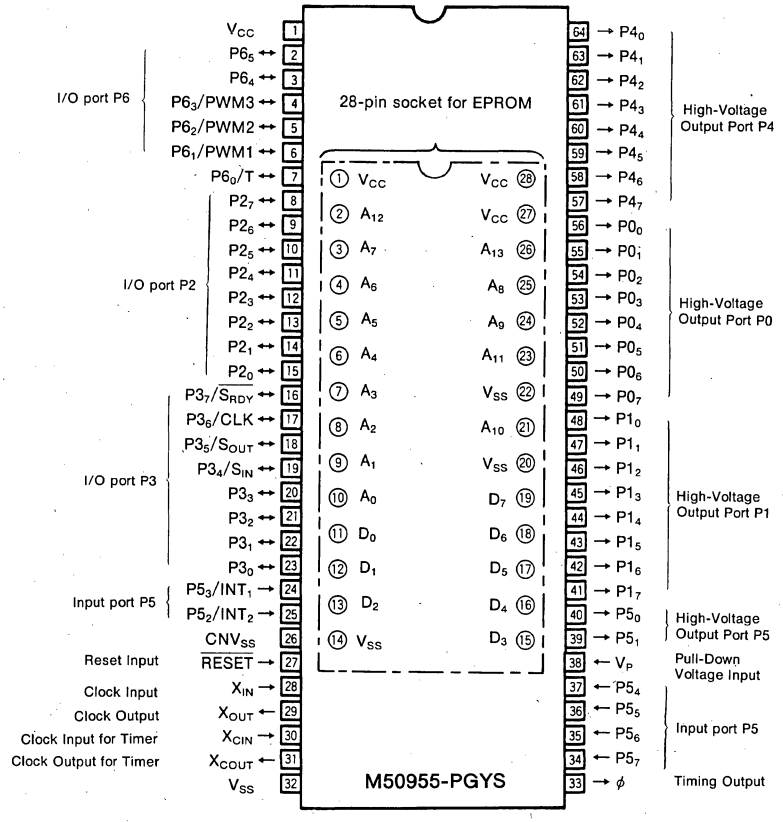
(1) ROMless, EPROM is attached externally.

(2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

Development of programs for VCR, tuners, and audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol "○" indicates sockets for EPROM.

MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P0, P1, P4, $P5_0$ and $P5_1$.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions.) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin, and the X_{COUT} pin should be left open: This clock can be used as a program controlled the system clock.
X_{COUT}	Clock output for clock function	Output	
$P0_0$~$P0_7$	Output port P0	Output	Port P0 is an 8-bit output port. Output structure is high-voltage P-channel open drain. A pull-down transistor is built in between the V_P pin and this port. At reset, this port is set to a "L" level.
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P2. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$. CLK, S_{OUT}, and S_{IN} pins, respectively.
$P4_0$~$P4_7$	Output port P4	Output	Port P4 is an 8-bit output port and has basically the same functions as port P2.
$P5_0$, $P5_1$	Output port P5	Output	Bit 0 and 1 of port P5 are 2-bit output port and has basically the same functions as port P0.
$P5_2/INT_2$ $P5_3/INT_1$	Input port P5	Input	Bit 2 and 3 of port P5 are 2-bit input port and are in common with interrupt inputs.
$P5_4$~$P5_7$		Input	Bit 4~7 of port P5 are 4-bit input port.
$P6_0$~$P6_5$	I/O port P6	I/O	Port P6 is a 6-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. The output structure is CMOS tri-state output. $P6_0$, $P6_1$, $P6_2$, $P6_3$ can be programmed to function as timer output pin (T), PWM output pins (PWM1, PWM2, and PWM3), respectively.
A_0~A_{13}	Output port A	Output	These are for addresses to an EPROM mounted on the package.
D_0~D_7	Input port D	Input	These are for input data from an EPROM mounted on the package.

BASIC FUNCTION BLOCK

The differences between the M50955-PGYS and the M50955-XXXSP are noted below. The following explanations apply to the M50955-PGYS.
Specification variations for other chips are noted accordingly.

MEMORY

The memory map is shown in Figure 1. The M50955-PGYS is mounted an EPROM instead of an internal ROM.
The address of an EPROM is $C000_{16} \sim FFFF_{16}$, and this memory size is 16384 bytes. Other than these, the M50955-PGYS has the same functions as the M50955-XXXSP has.

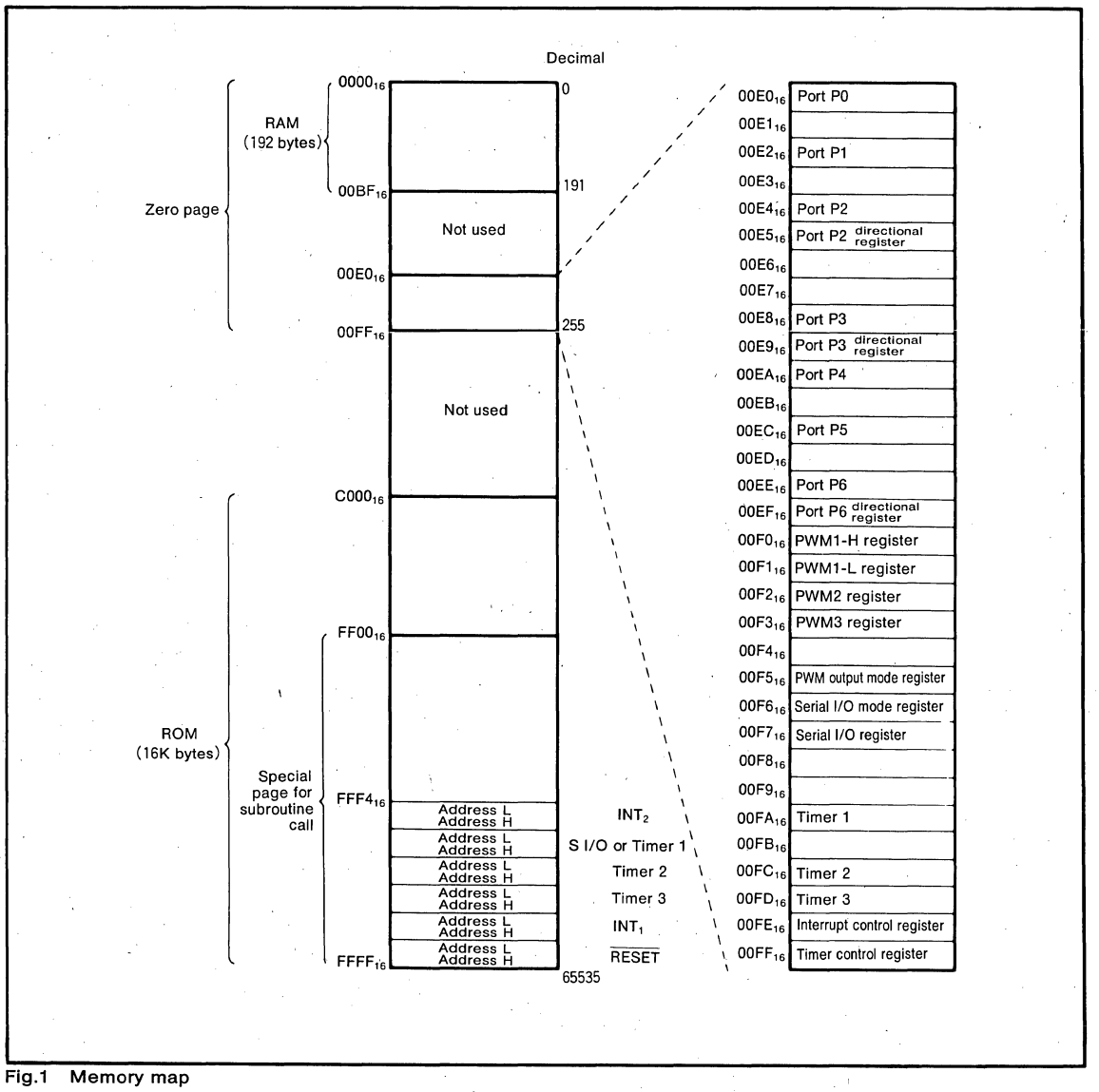


Fig.1 Memory map

PROCESSOR MODE

External memory area differs from the M50955-XXXSP in the memory expanding mode.

External memory map in the memory expanding mode is shown in Figure 2.

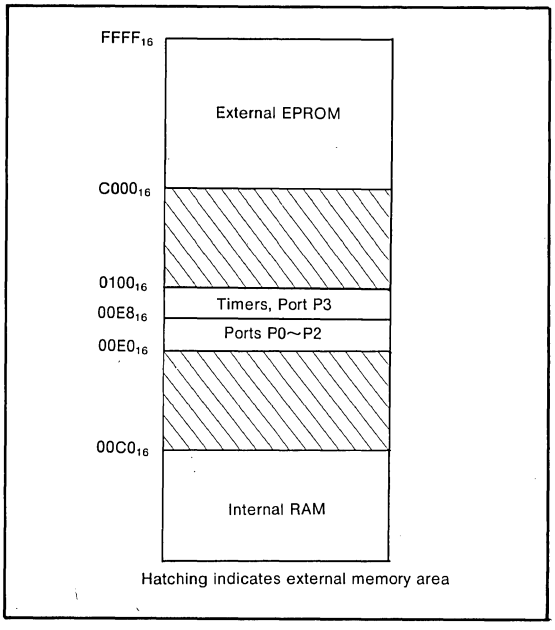


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) In case of the M5L2764K or the M5L27128K EPROM use the following areas (refer to Figure 1):

- For the M50754-XXXSP, usable ROM area are $E800_{16}$~$FFFF_{16}$.

M5L2764K····· addresses 0800_{16}~$1FFF_{16}$
M5L27128K····· addresses 2800_{16}~$3FFF_{16}$

- For the M50954-XXXSP, usable ROM area are $E000_{16}$~$FFFF_{16}$.

M5L2764K····· addresses 0000_{16}~$1FFF_{16}$
M5L27128K····· addresses 2000_{16}~$3FFF_{16}$

- For the M50955-XXXSP, usable ROM area $D800_{16}$ ~$FFFF_{16}$.

M5L27128K····· addresses 1800_{16}~$3FFF_{16}$

(2) The M50955-PGYS has no options as the M50754-XXXSP, the M50954-XXXSP and the M50955-XXXSP. Therefore for the M50955-PGYS, the ϕ output cannot be stopped.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off.	−0.3～7	V
V_P	Pulldown input voltage		V_{CC}−40～V_{CC}+0.3	V
V_I	Input voltage, $P2_0$～$P2_7$, $P3_0$～$P3_7$ CNV_{SS}, $P5_2/INT_2$, $P5_3/INT_1$		−0.3～13	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, X_{CIN}		−0.3～7	V
V_I	Input voltage, $P6_0$～$P6_5$		−0.3～V_{CC}+0.3	V
V_I	Input voltage, $P5_4$～$P5_7$		−0.3～13	V
V_O	Output voltage, $P2_0$～$P2_7$, $P3_0$～$P3_7$		−0.3～13	V
V_O	Output voltage, $P6_0$～$P6_5$, X_{OUT}, X_{COUT}, ϕ		−0.3～V_{CC}+0.3	V
V_O	Output voltage, $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P4_0$～$P4_7$, $P5_0$, $P5_1$		V_{CC}−40～V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
T_{opr}	Operating temperature		−10～70	℃
T_{stg}	Storage temperature		−40～125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=−10～70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_P	Pull-down supply voltage	V_{CC}−38		V_{CC}	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P2_0$～$P2_7$, $P3_0$～$P3_7$, CNV_{SS}(Note 2) $P5_2/INT_2$, $P5_3/INT_1$, $P6_0$～$P6_5$	0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P5_4$～$P5_7$	0.4V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P2_0$～$P2_7$, $P3_0$～$P3_7$, CNV_{SS} $P5_2/INT_2$, $P5_3/INT_1$, $P6_0$～$P6_5$	0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}	0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P5_4$～$P5_7$	0		0.12V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P4_0$～$P4_7$ $P5_0$, $P5_1$			−120	mA
$I_{OH(sum)}$	"H" sum output current $P6_0$～$P6_5$			−5	mA
$I_{OL(sum)}$	"L" sum output current $P2_0$～$P2_7$, $P3_0$～$P3_7$			50	mA
$I_{OL(sum)}$	"L" sum output current $P6_0$～$P6_5$			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$～$P0_4$			−30	mA
$I_{OH(peak)}$	"H" peak output current $P0_5$～$P0_7$, $P1_0$～$P1_7$			−30	mA
$I_{OH(peak)}$	"H" peak output current $P4_0$～$P4_7$, $P5_0$, $P5_1$			−30	mA
$I_{OH(peak)}$	"H" peak output current $P6_0$～$P6_5$			−3	mA
$I_{OL(peak)}$	"L" peak output current $P2_0$～$P2_7$, $P3_0$～$P3_7$			15	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$～$P6_5$			3	mA
$I_{OH(avg)}$	"H" average output current $P0_0$～$P0_7$, $P1_0$～$P1_7$			−12	mA
$I_{OH(avg)}$	"H" average output current $P4_0$～$P4_7$, $P5_0$, $P5_1$			−12	mA
$I_{OH(avg)}$	"H" average output current $P6_0$～$P6_5$			−1.5	mA
$I_{OL(avg)}$	"L" average output current $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P6_0$～$P6_5$			10	mA
$I_{OL(avg)}$	"L" average output current $P6_0$～$P6_5$			1.5	mA
$f(x_{IN})$	Clock input oscillating frequency (Note 3, 4, 6)			4.2	MHz
$f(x_{CIN})$	Clock oscillating frequency for clock function			500	kHz

Note 2 : High-level input voltage of up to +12V may be applied to permissible for ports $P2_0$～$P2_7$, $P3_0$～$P3_7$, CNV_{SS}, and $P5_2$～$P5_7$.
3 : Oscillation frequency is at 50% duty cycle.
4 : When used in the low-speed mode, the timer clock input frequency should be $f_{(XIN)} < f_{(XIN)}/3$.
5 : When external clock input is used, the timer clock input frequency should be $f_{(XCIN)} \leqq 50kHz$.
6 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are in period of 100ms.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P6_0$~$P6_5$	I_{OH}=−0.5mA	V_{CC}−0.4			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA	V_{CC}−2			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$	I_{OH}=−18mA	V_{CC}−2			V
V_{OH}	"H" output voltage $P4_0$~$P4_7$, $P5_0$, $P5_1$	I_{OL}=−12mA	V_{CC}−2			V
V_{OL}	"L" output voltage $P2_0$~$P2_7$, $P3_0$~$P3_7$	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage $P6_0$~$P6_5$	I_{OL}=0.5mA			0.4	V
V_{OL}	"L" output voltage ϕ	I_{OL}=2.5mA			2	V
$V_{T+}-V_{T-}$	Hysteresis $P5_2/INT_2$, $P5_3/INT_1$		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P2_0$~$P2_7$, $P3_0$~$P3_7$	V_I=0V			−5	μA
I_{IL}	"L" input current $P6_0$~$P6_5$	V_I=0V			−5	μA
I_{IL}	"L" input current $P5_4$~$P5_7$	V_I=0V			−5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}	V_I=0V			−5	μA
I_{IL}	"L" input current $P5_2/INT_2$, $P5_3/INT_1$	V_I=0V			−5	μA
I_{IH}	"H" input current $P2_0$~$P2_7$, $P3_0$~$P3_7$	V_I=5V			5	μA
		V_I=12V			12	μA
I_{IH}	"H" input current $P6_0$~$P6_5$	V_I=5V			5	μA
I_{IH}	"H" input current $P5_4$~$P5_7$	V_I=5V			5	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}	V_I=5V			5	μA
I_{IH}	"H" input current $P5_2/INT_2$, $P5_3/INT_1$	V_I=5V			5	μA
		V_I=12V			12	μA
I_{OL}	"L" output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$	V_P=V_{CC}−36V, V_{OL}=V_{CC}	150	450	900	μA
		V_P=V_{CC}−36V, V_{OL}=V_{CC}−36V			30	μA
V_{RAM}	RAM retention voltage	at clock stop	2		5.5	V
I_{CC}	Supply current	Output pins open (output OFF) V_P=V_{CC}, V_P=V_{SS} Input and I/O pins all at V_{SS} X_{IN}=4MHz (system operation)		3	6	mA

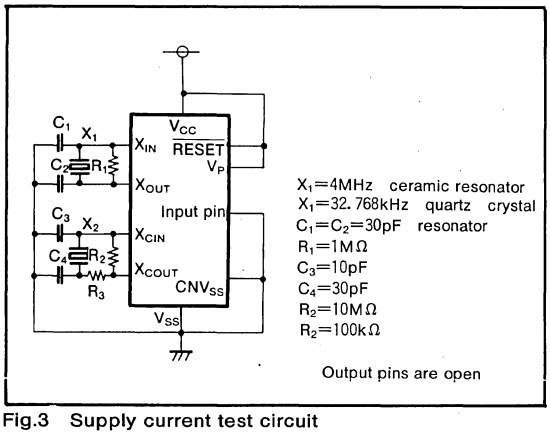


Fig.3 Supply current test circuit

M50964-PGYS

PIGGYBACK for M50964-XXXSP,M50963-XXXSP

DESCRIPTION

The M50964-PGYS is an EPROM mounted-type microcomputer which utilizes CMOS technology, and is designed for developing programs for single-chip 8-bit microcomputers the M50964-XXXSP/M50963-XXXSP. It is housed in a piggyback-type 64-pin shrink DIP.

There is a 28-pin socket on the package for the M5L2764K or the M5L27128K EPROM.

The M50964-PGYS simplifies the development of programs for the M50964-XXXSP/M50963-XXXSP, and is excellent for making prototypes.

The differences between the M50964-XXXSP and the M50963-XXXSP are only ROM size.

Therefor the M50964-PGYS can be used for the development of programs for the M50964-XXXSP/M50963-XXXSP.

DISTINCTIVE FEATURES

- Differences with the M50964-XXXSP/M50963-XXXSP are:

(1) ROMless, EPROM is attached externally.

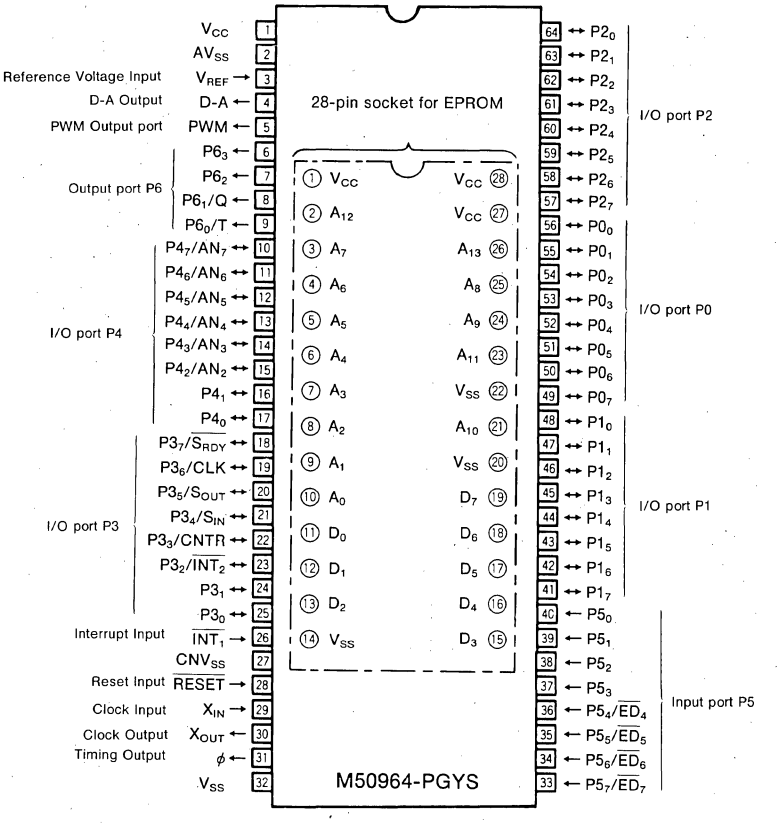
(2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

Development of programs for the following systems;

- Office automation equipment
- VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol "○" indicates sockets for EPROM.

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions.) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
AV_{SS}	Voltage input for A-D and D-A		This is GND input pin for the A-D and D-A converters.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D and D-A converters.
D-A	D-A output	Output	This is output pin from the D-A convereter.
PWM	PWM output	Output	This is output pin from the pulse width modulator. The output structure is N-channel open drain.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open drain.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest interrupt input pin ($\overline{INT_2}$), respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. $P4_4$~$P4_7$ work as analog input port AN_4~AN_7.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port. $P5_4$~$P5_7$ can be used as the edge sense inputs.
$P6_0$~$P6_3$	Output port P6	Output	Port P6 is a 4-bit output port. At external trigger output mode, $P6_0$ and $P6_1$ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively. The output structure is N-channel open drain.
A_0~A_{13}	Output port A	Output	These are for addresses to an EPROM mounted on the package.
D_0~D_7	Input port D	Input	These are for input data from an EPROM mounted on the package.

BASIC FUNCTION BLOCK

The differences between the M50964-PGYS and the M50964-XXXSP/M50963-XXXSP are noted below. The following explanations apply to the M50964-PGYS.
Specification variations for other chips are noted accordingly.

MEMORY

The memory map is shown in Figure 1. The M50964-PGYS is mounted an EPROM instead of an internal ROM.
The address of an EPROM is $C000_{16} \sim FFFF_{16}$, and this memory size is 16384 bytes. Other than these, the M50964-PGYS has the same functions as the M50964-XXXSP/M50963-XXXSP have.

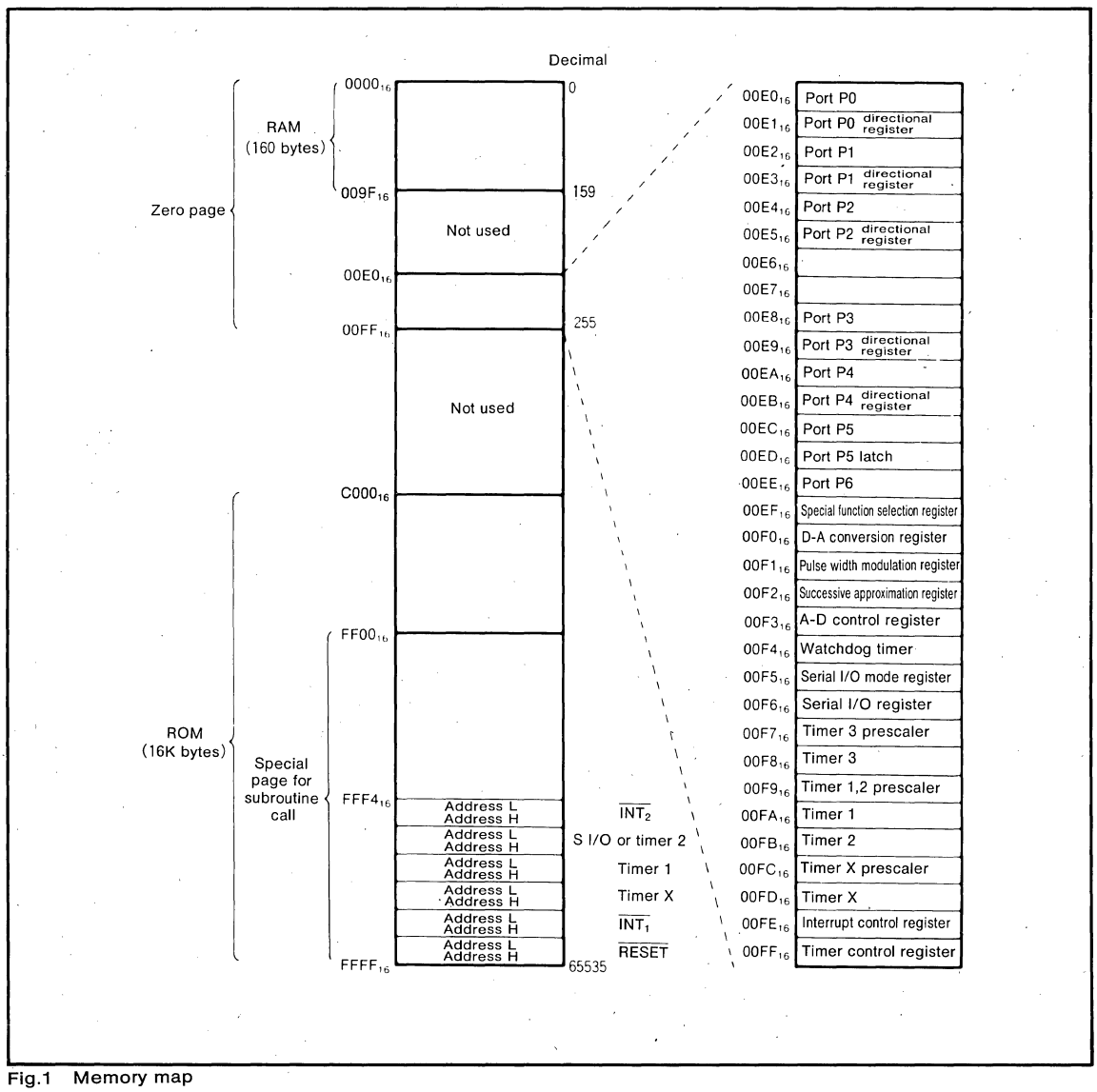


Fig.1 Memory map

PROCESSOR MODE

External memory area differs from the M50964-XXXSP/M50963-XXXSP in the memory expanding mode.

External memory map in the memory expanding mode is shown in Figure 2.

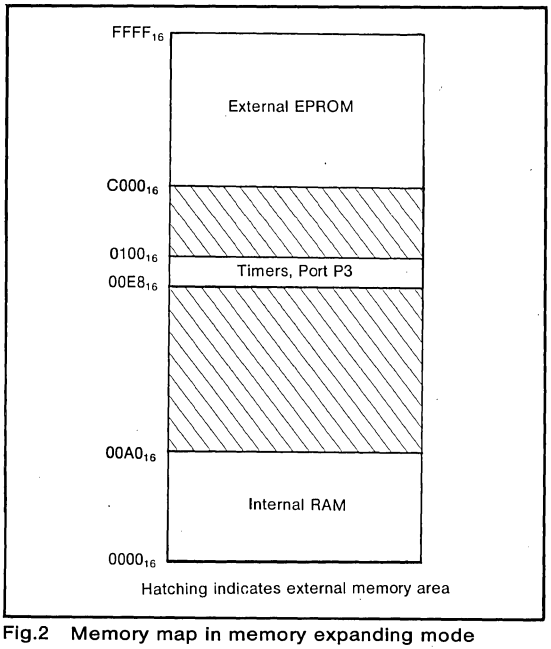


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) In case of the M5L2764K or the M5L27128K EPROM use the following areas (refer to Figure 1):

- For the M50964-XXXSP, usable ROM area are $E800_{16}$~$FFFF_{16}$.

M5L2764K ····· addresses 0800_{16}~$1FFF_{16}$

M5L27128K ····· addresses 2800_{16}~$3FFF_{16}$

- For the M50963-XXXSP, usable ROM area are $D800_{16}$~$FFFF_{16}$.

M5L27128K ····· addresses 1800_{16}~$3FFF_{16}$

(2) The M50964-PGYS has no options as the M50964-XXXSP/M50963-XXXSP. But, the M50964-PGYS can use the STP instruction.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	−0.3～7	V
V_I	Input voltage X_{IN}		−0.3～7	V
V_I	Input voltage $P2_0$～$P2_7$, $P4_2$～$P4_7$		−0.3～V_{CC}+0.3	V
V_I	Input voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P3_0$～$P3_7$, $P4_0$, $P4_1$, $P5_0$～$P5_7$, $\overline{INT_1}$		−0.3～13	V
V_I	Input voltage CNV_{SS}, $\overline{RESET}$		−0.3～13	V
V_O	Output voltage $P2_0$～$P2_7$, $P4_2$～$P4_7$, X_{OUT}, ϕ, D-A		−0.3～V_{CC}+0.3	V
V_O	Output voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P3_0$～$P3_7$, $P4_0$, $P4_1$, $P6_0$～$P6_3$, PWM		−0.3～13	V
P_d	Power dissipation	T_a=25℃	1000(Note 1)	mW
Topr	Operating temperature		−10～70	℃
Tstg	Storage temperature		−40～125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=−10～70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, $P5_0$～$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}, $P6_0$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$～$P0_7$	0.45V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, $P5_0$～$P5_7$, $\overline{INT_1}$, CNV_{SS}, $P6_0$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
V_{IL}	"L" output voltage $P0_0$～$P0_7$	0		0.15V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$～$P6_3$ (Note 2)			15	mA
$I_{OL(peak)}$	"L" peak output current PWM (Note 2)			5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P4_0$～$P4_7$, (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0$～$P6_3$ (Note 1)			7	mA
$I_{OL(avg)}$	"L" average output current PWM (Note 1)			2.5	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$～$P2_7$ (Note 2)			−10	mA
$I_{OH(avg)}$	"H" average output current $P2_0$～$P2_7$ (Note 1)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

Note 1 : Average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
2 : Total of "L" output current I_{OL}, of ports P0, P1, P2, P3, P4, P6, and PWM is 80mA max.
Total of "H" output current I_{OH}, of port P2 is 50mA max.
3 : "H" input voltage of ports P0, P1, P3, $P4_0$～$P4_3$, P5, and $\overline{INT_1}$ is available up to +12V.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P2_0$~$P2_7$	I_{OH}=−10mA		3			V
V_{OH}	"H" output voltage ϕ, A_0~A_{13}	I_{OH}=−2.5mA		3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_3$	I_{OL}=10mA				2	V
V_{OL}	"L" output voltage ϕ, PWM, A_0~A_{13}	I_{OL}=5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input		0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$	When used as $\overline{INT_2}$ input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_3$	When used as CNTR input		0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $P6_0$	When used as T input		0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}			0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$ $P6_0$~$P6_3$, PWM	V_I=0V				−5	μA
I_{IL}	"L" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, D_0~D_7	V_I=0V				−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_7$ $P4_0$~$P4_3$, $P5_0$~$P5_7$, $P6_0$~$P6_3$ PWM	V_I=12V				12	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, $P2_0$~$P2_7$ $P4_4$~$P4_7$, D_0~D_7	V_I=5V				5	μA
V_{RAM}	RAM retention voltage	When clock stopped		2			V
I_{CC}	Supply current	ϕ, X_{OUT}, and D-A pins opened, other pins at V_{SS}, and A-D converter in the finished condition.	$f_{(X_{IN})}$=4MHz Square wave		3	6	mA
			When clock stopped T_a=25℃			1	μA
			When clock stopped T_a=75℃			10	

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance value	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference input voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			5	Bits
—	Error in full scale range	V_{REF}=V_{CC}			±1	%
t_{SU}	Set up time	V_{REF}=V_{CC}			3	μs
R_O	Output resistance	V_{REF}=V_{CC}			3	kΩ
V_{REF}	Reference voltage		4		V_{CC}	V

M37450PSS

PIGGYBACK for M37450M2-XXXSP,M37450M4-XXXSP,M37450M8-XXXSP

DESCRIPTION

The M37450PSS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M37450M2-XXXSP, M37450M4-XXXSP and M37450M8-XXXSP. The M37450PSS, being housed in a piggyback-type 64-pin shrink DIP, is compatible with the M37450M2-XXXSP, M37450M4-XXXSP and M37450M8-XXXSP.

There is a 28-pin socket on the upper surface so that the M5M27C256K-12 or the M5M27C256K-15 EPROM may be used.

The M37450PSS simplifies the development of programs for the M37450M2-XXXSP, M37450M4-XXXSP and M37450 M8-XXXSP and is excellent for making prototypes.

DISTINCTIVE FEATURES

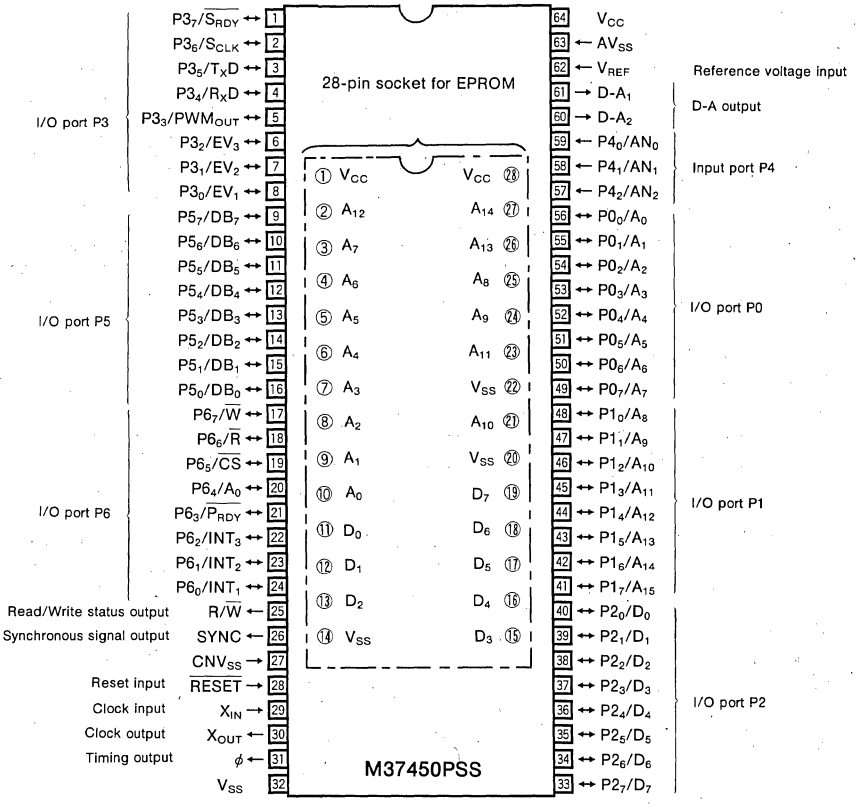
- Differences with the M37450M2-XXXSP, M37450M4-XXXSP and M37450M8-XXXSP are:
  (1) ROMless, EPROM is attached externally.
  (2) Suitable EPROM is M5M27C256K-12, M5M27C256K -15.

APPLICATION

Development of programs for the following systems;

- Slave controller for PPCs, facsimiles, and page printers
- HDD, optical disk, inverter, and industrial motor controllers
- Industrial robots and machines

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol "○" indicates sockets for EPROM.

MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC} and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		Controls the processor mode of the chip. Normally connected to V_{SS} or V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under nomal V_{CC} conditions). If more time is needed for the crystal oscillator to stabillize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four.
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs.
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus. It is "H" during read and "L" during write.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programed as input or output. The output structure is CMOS output. The low-order bits of the address are output except in single-chip mode.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same function as port P0. The high-order bits of the address are output except in single-chip mode.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as P0. Used as data bus except in single-chip mode.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same function as P0. Serial I/O, PWM output, or even I/O function can be selected with a program.
$P4_0$~$P4_2$	Input port P4	Input	Analog input pin for the A-D converter. They may also be used as digital input pins.
$P5_0$~$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as P0. This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program.
$P6_0$~$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as P0. Pins $P6_3$~$P6_7$ change to control bus for the master CPU when slave mode is selected with a program. Pins $P6_0$~$P6_2$ may be programed as external interrupt input pins.
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Refference voltage input	Input	Reference voltage input pin for A-D and D-A converter.
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter.
A_0~A_{14}	Output port A	Output	Port A outputs the adresses to the EPROM mounted on the top of the package.
D_0~D_7	Input port D	Input	Port D takes the input data from the EPROM mounted on the top of the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M37450PSS and the M37450M2-XXXSP, M37450M4-XXXSP and M37450M8-XXXSP are explained below. As all other points are the same, only the differences are explained.

MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The addresses of EPROM are 8000_{16} to $FFFF_{16}$, having 32K bytes. Internal RAMs are provided from 0000_{16} to $00BF_{16}$ (192 bytes) and from 0100_{16} to $01FF_{16}$ (256 bytes) for a total of 448 bytes. However, the 64-byte area from $01C0_{16}$ to $01FF_{16}$ cannot be used when creating masked ROM. The rest of the functions are equivalent to the M37450M2-XXXSP, M37450M4-XXXSP and M37450M8-XXXSP.

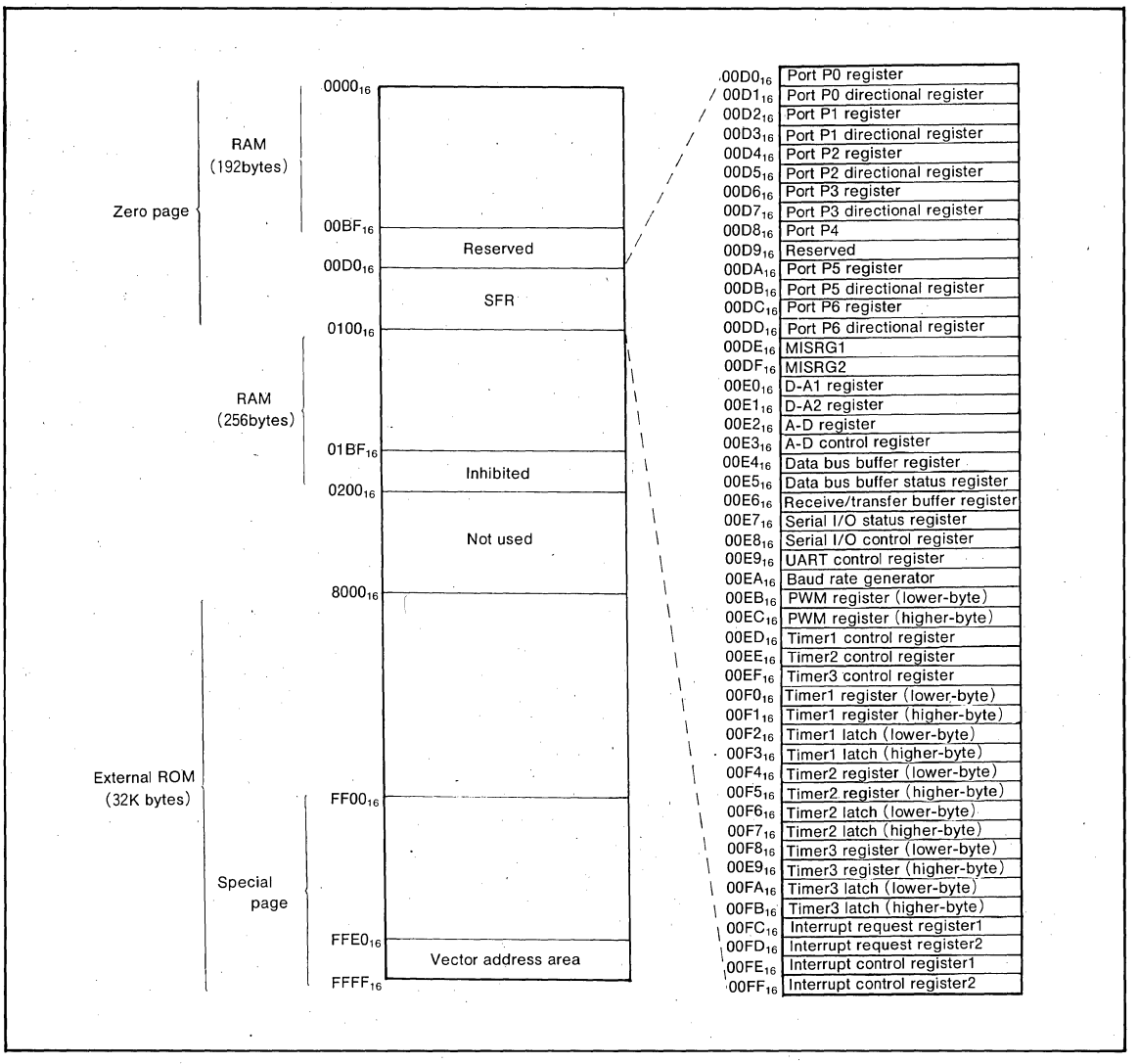


Fig. 1 Memory map

PROCESSOR MODE

External memory area differs from the M37450M2-XXXSP, M37450M4-XXXSP and M37450M8-XXXSP.

Figure 2 shows the external memory area when the M37450PSS is in the memory expanding mode and Fig. 3 shows the external memory area when the M37450PSS is in the microprocessor mode.

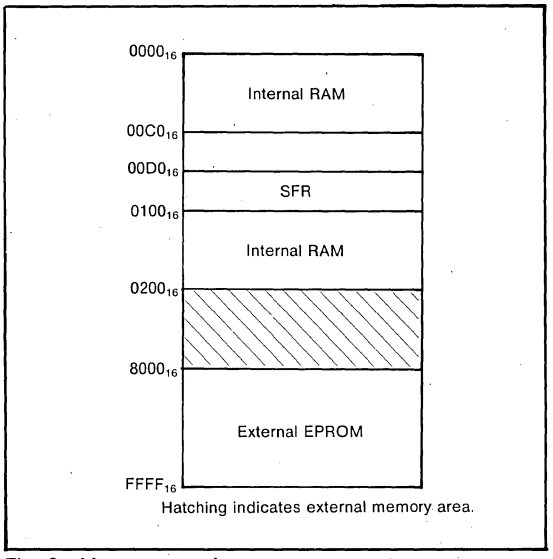


Fig. 2 Memory map in memory expanding mode

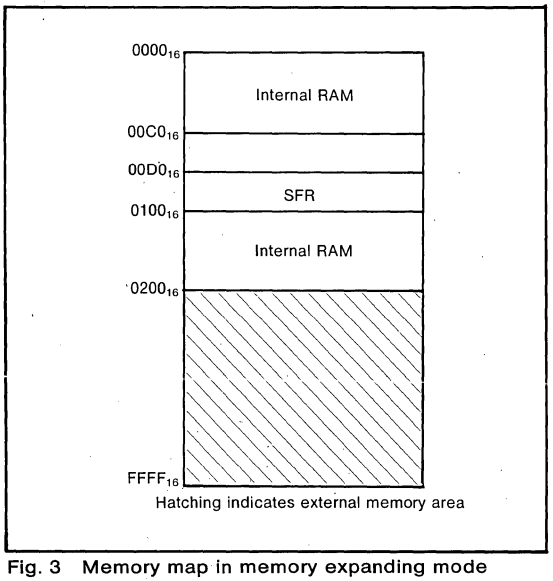


Fig. 3 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) Program area

When developing programs on the M37450PSS, the ROM and RAM sizes of the M37450M2-XXXSP, M37450M4-XXXSP, and M37450M8-XXXSP must be considered.

For the M37450M2-XXXSP, use the M37450PSS ROM program area from $F000_{16}$ to $FFFF_{16}$. (Write the program from 7000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M2-XXXSP is 128 bytes from 0000_{16} to $007F_{16}$.

For the M37450M4-XXXSP, use the M37450PSS ROM program area from $E000_{16}$ to $FFFF_{16}$. (Write the program from 6000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M4-XXXSP is 192 bytes from 0000_{16} to $00BF_{16}$ and 64 bytes from 0100_{16} to $013F_{16}$ for a total of 256 bytes.

For the M37450M8-XXXSP, use the M37450PSS ROM program area from $C000_{16}$ to $FFFF_{16}$. (Write the program from 4000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M8-XXXSP is 192 bytes from 0000_{16} to $00BF_{16}$ and 192 bytes from 0100_{16} to $01BF_{16}$ for a total of 384 bytes.

The 64 byte area from $01C0_{16}$ to $01FF_{16}$ can also be used as internal RAM. However, it cannot be used when creating masked ROMs because there is no corresponding device.

(2) External memory

When developing programs, note that the external memory area of the M37450PSS is as described in the previous section.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3∼7	V
V_I	Input voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$ $P6_0$∼$P6_7$, V_{REF}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3∼13	V
V_O	Output voltage, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ X_{OUT}, ϕ, R/$\overline{W}$, SYNC		−0.3∼V_{CC}+0.3	V
Pd	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−10∼70	℃
T_{stg}	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5V±10%, T_a = −10∼70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$ $P6_0$∼$P6_7$ (except Note1)	2.0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note1)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$ $P6_0$∼$P6_7$ (except Note1)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$ $P2_0$∼$P2_7$, $P3_0$∼$P3_7$ $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note2)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$ $P2_0$∼$P2_7$, $P3_0$∼$P3_7$ $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note2)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		10	MHz

Note 1 : Ports operate as INT_1∼INT_3($P6_0$∼$P6_2$), EV_1∼EV_3($P3_0$∼$P3_2$), R_xD($P3_4$)and S_{CLK}($P3_6$).
2 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms.
3 : The total of "L" output $I_{OL(peak)}$ of port P0, P1 and P2 is 40mA max.
The total of "H" output $I_{OH(peak)}$ of port P0, P1 and P2 is 40mA max.
The total of "L" output $I_{OL(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC and ϕ is 40mA max.
The total of "H" output $I_{OH(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC and ϕ is 40mA max.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, $f_{(X_{IN})}$ = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output R/$\overline{W}$, SYNC, ϕ	I_{OH}=−2mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OH}=−5mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$ R/$\overline{W}$, SYNC, ϕ	I_{OL}=2mA			0.45	V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OL}=5mA			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1~INT_3($P6_0$~$P6_2$), EV_1~EV_3($P3_0$~$P3_2$) R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" Input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$ $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{SS}	−5		5	μA
I_{IH}	"H" Input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$ $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation $f(X_{IN})$=10MHz(Note 4)		6	10	mA

Note 4 : Only for M37450PSS (not contact in EPROM dissipation current).

A-D CONVERTER CHARACTERISTICS (V_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=V_{REF}=5.12V		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_C(\phi)$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{VREF}	Reference analog input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	V_{REF}=5V	2	7.5	10	kΩ
I_{IVREF}	Reference analog input current	V_{REF}=5V	0.5	0.7	2.5	mA
V_{AVSS}	Analog power input			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, f(X_{IN}) = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Abusolute accuracy	V_{CC}=V_{REF}=5.12V			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power input			0		V
V_{VREF}	Analog power input		4		V_{CC}	V
I_{VREF}	Reference power input current		0	2.5	5	mA

M37450PFS

PIGGYBACK for M37450M2-XXXFP,M37450M4-XXXFP,M37450M8-XXXFP

DESCRIPTION

The M37450PFS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP. The M37450PFS, being housed in a piggyback-type 80-pin plastic QFP is compatible with the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP.

There is a 32-pin socket on the upper surface so that EPROM may be used.

The M37450PSS simplifies the development of programs for the M37450M2-XXXFP, M37450M4-XXXFP and M37450 M8-XXXFP and is excellent for making prototypes.

DISTINCTIVE FEATURES

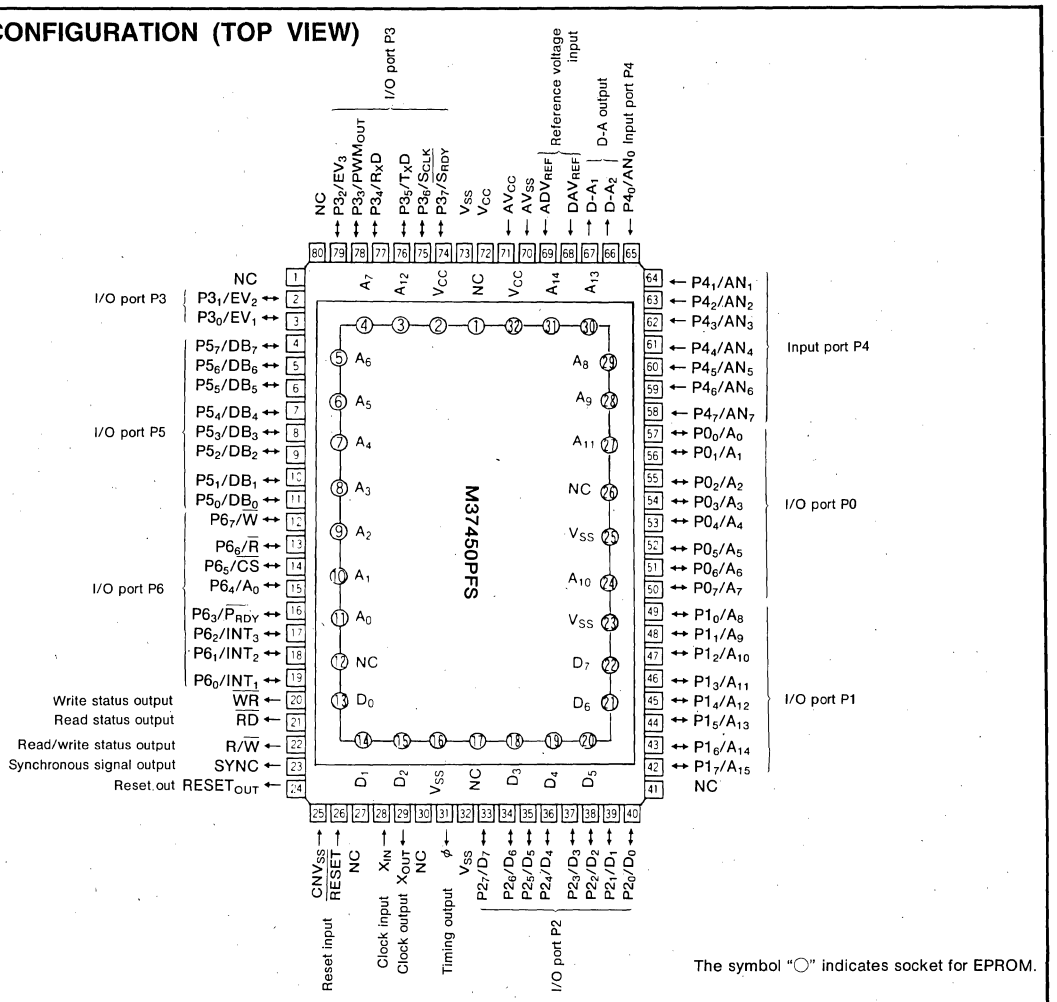
- Difference with the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP is:
  (1) ROMless, EPROM is attached externally.

APPLICATION

Development of programs for the following systems:

- Slave controller for PPCs, facsimiles, and page printers
- HDD, optical disk, inverter, and industrial motor controllers
- Industrial robots and machines

PIN CONFIGURATION (TOP VIEW)



The symbol "○" indicates socket for EPROM.

Outline 80S6M

NC : No Connection

PIGGYBACK for M37450M2-XXXFP,M37450M4-XXXFP,M37450M8-XXXFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC} and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		Controls the processor mode of the chip. Normally connected to V_{SS} or V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under nomal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four.
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs.
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus. It is "H" during read and "L" during write.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programed as input or output. The output structure is CMOS output. The low-order bits of the address are output except in single-chip mode.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same function as port P0. The high-order bits of the address are output except in single-chip mode.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as P0. Used as data bus except in single-chip mode.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same function as P0. Serial I/O, PWM output, or even I/O function can be selected with a program.
$P4_0$~$P4_7$	Input port P4	Input	Analog input pin for the A-D converter. They may also be used as digital input pins.
$P5_0$~$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as P0. This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program.
$P6_0$~$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as P0. Pins $P6_3$~$P6_7$ change to control bus for the master CPU when slave mode is selected with a program. Pins $P6_0$~$P6_2$ may be programed as external interrupt input pins.
$D\text{-}A_1$, $D\text{-}A_2$	D-A output	Output	Analog signal from D-A converter is output
ADV_{REF}	A-D refference voltage input	Input	Reference voltage input pin for A-D converter.
DAV_{REF}	D-A refference voltage input	Input	Reference voltage input pin for D-A converter.
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter.
AV_{CC}	Analog power supply		Power supply input pin for A-D converter.
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when vailed data is read from data bus.
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component.
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset. It is used as a reset output signal for perpheral components.
A_0~A_{14}	Output port A	Output	Port A outputs the adresses to the EPROM mounted on the top of the package.
D_0~D_7	Input port D	Input	Port D takes the input data from the EPROM mounted on the top of the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M37450PFS and the M37450-M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP are explained below. As all other points are the same, only the differences are explained.

MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The addresses of EPROM are 8000_{16} to $FFFF_{16}$, having 32K bytes. Internal RAMs are provided from 0000_{16} to $00BF_{16}$ (192 bytes) and from 0100_{16} to $01FF_{16}$ (256 bytes) for a total of 448 bytes. However, the 64-byte area from $01C0_{16}$ to $01FF_{16}$ cannot be used when creating masked ROM. The rest of the functions are equivalent to the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP.

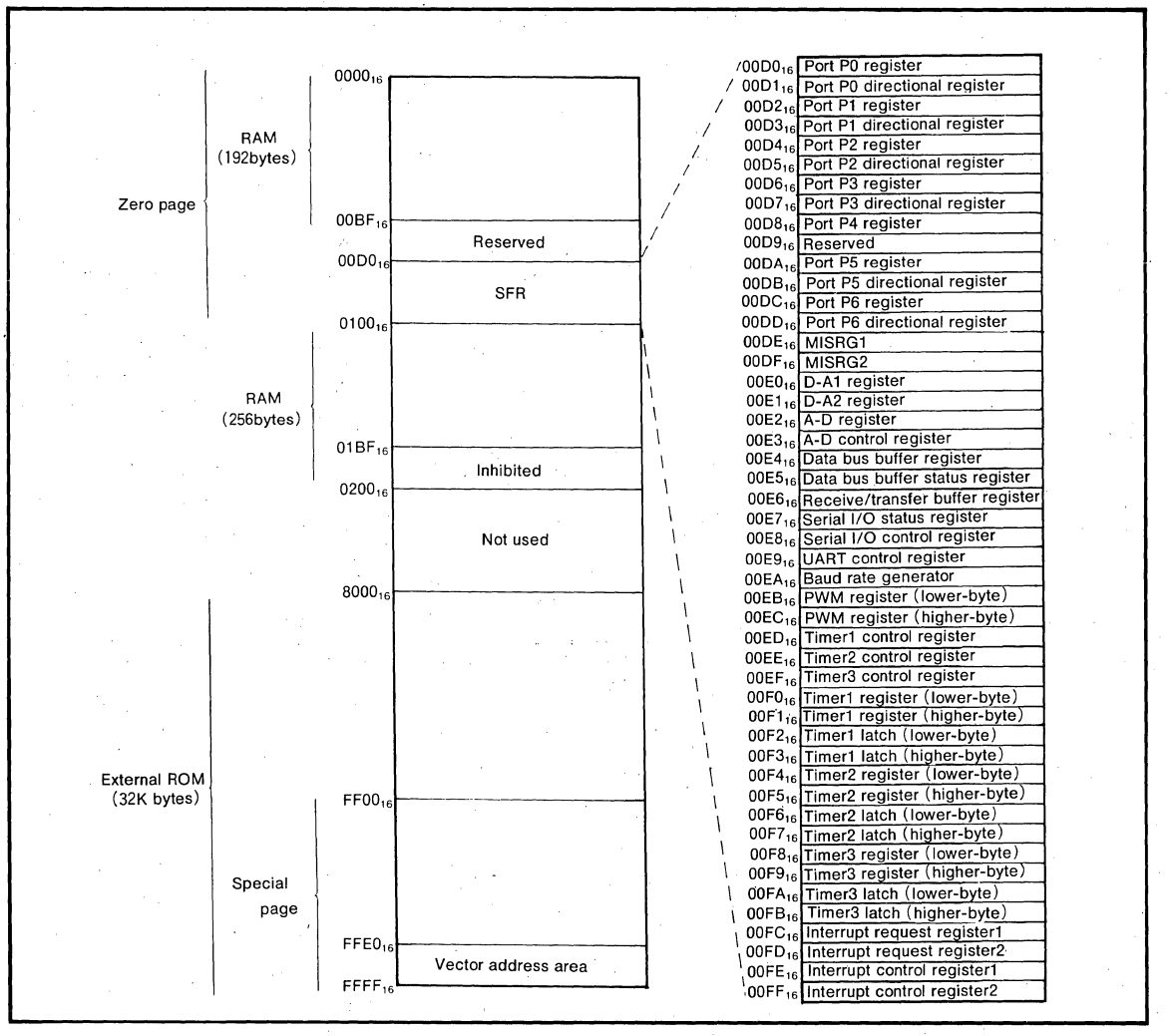


Fig. 1 Memory map

MITSUBISHI ELECTRIC

PROCESSOR MODE

External memory area differs from the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP.

Figure 2 shows the external memory area when the M37450PFS is in the memory expanding mode and Figure 3 shows the external memory area when the M37450PFS is in the microprocessor mode.

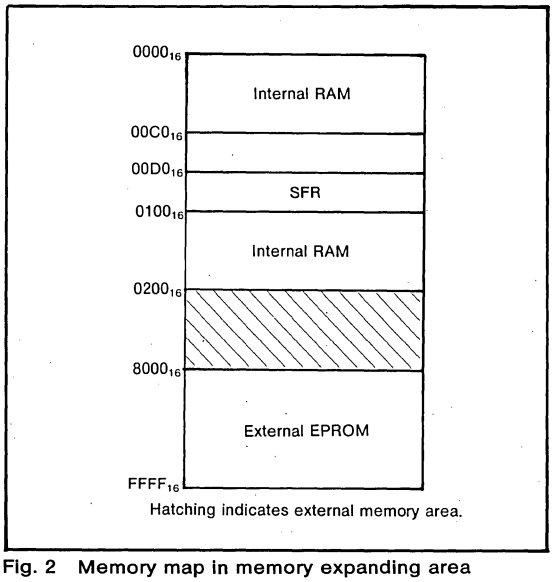


Fig. 2 Memory map in memory expanding area

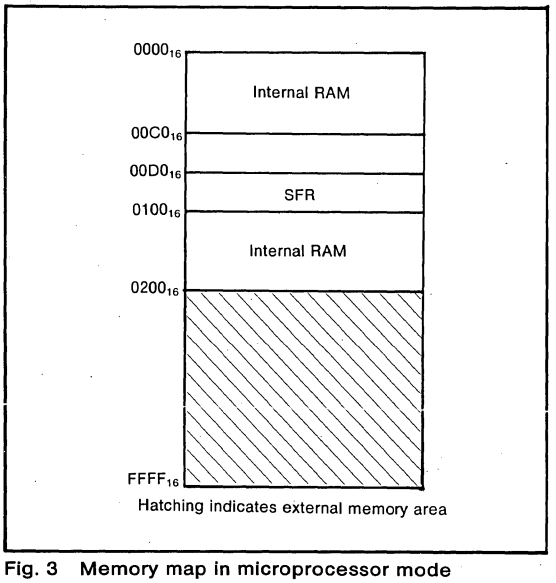


Fig. 3 Memory map in microprocessor mode

PRECAUTION FOR USE

(1) Program area

When developing programs on the M37450PFS, the ROM and sizes of the M37450M2-XXXFP, M37450M4-XXXFP, and M37450M8-XXXFP must be considered.

For the M37450M2-XXXFP, use the M37450PFS ROM program area from $F000_{16}$ to $FFFF_{16}$. (Write the program from 7000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M2-XXXFP is 128 bytes from 0000_{16} to $0007F_{16}$.

For the M37450M4-XXXFP, use the M37450PFS ROM program area from $E000_{16}$ to $FFFF_{16}$. (Write the program from 6000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M4-XXXFP is 192 bytes from 0000_{16} to $00BF_{16}$ and 64 bytes from 0100_{16} to $013F_{16}$ for a total of 256 bytes.

For the M37450M8-XXXFP, use the M37450PFS ROM program area from $C000_{16}$ to $FFFF_{16}$. (Write the program from 4000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M8-XXXFP is 192 bytes from 0000_{16} to $00BF_{16}$ and 192 bytes from 0100_{16} to $01BF_{16}$ for a total of 384 bytes.

The 64 byte area from $01C0_{16}$ to $01FF_{16}$ can also be used as internal RAM. However, it cannot be used when creating masked ROMs because there is no corresponding device.

(2) External memory

When developing programs, note that the external memory area of the M37450PFS is as described in the previous section.

(3) EPROM orientation

Figure 4 shows the orientation when mountting the EPROM on the M37450PFS. Insert the EPROM firmly until it hits bottom.

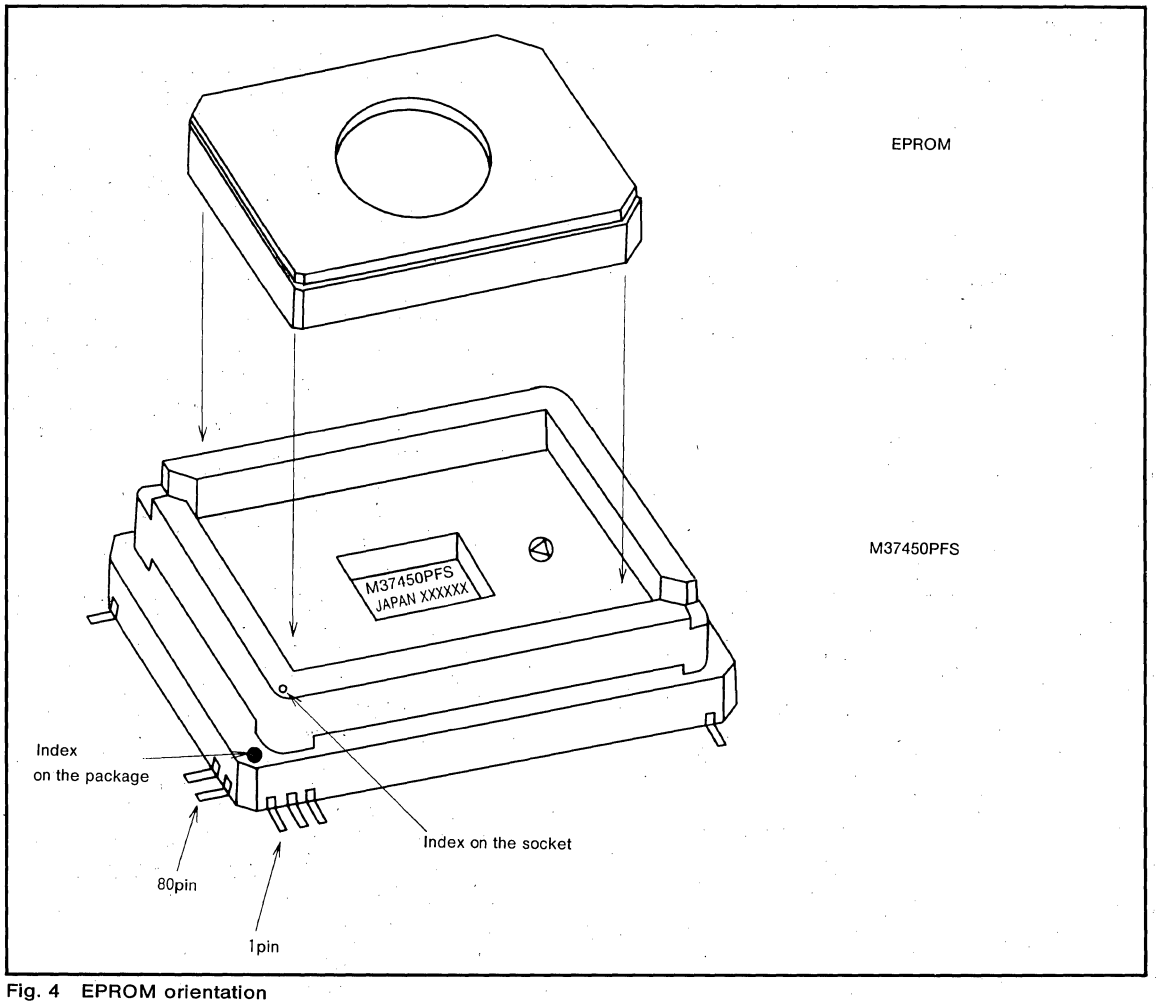


Fig. 4 EPROM orientation

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors are at "OFF" state	−0.3~7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3~7	V
V_I	Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, ADV_{RFF}, DAV_{RFF}, AV_{CC}		−0.3~V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3~13	V
V_O	Output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, SYNC		−0.3~V_{CC}+0.3	V
Pd	Power dissipation	T_a=25℃	500	mW
T_{opr}	Operating temperature		−10~70	℃
T_{stg}	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$ (except Note1)	2.0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note1)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$ (except Note1)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$ (Note2)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$ (Note2)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		10	MHz

Note 1 : Ports operate as INT_1~INT_3($P6_0$~$P6_2$), EV_1~EV_3($P3_0$~$P3_2$), R_XD($P3_4$)and S_{CLK}($P3_6$).
2 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms.
3 : The total of "L" output $I_{OL(peak)}$ of port P0, P1 and P2 is 40mA max.
The total of "H" output $I_{OH(peak)}$ of port P0, P1 and P2 is 40mA max.
The total of "L" output $I_{OL(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is 40mA max.
The total of "H" output $I_{OH(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is 40mA max.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70°C, $f_{(X_{IN})}$ = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output $\overline{RD}$, $\overline{WR}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH}=−2mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OH}=−5mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$ R/$\overline{W}$, $\overline{RD}$, $\overline{WR}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL}=2mA			0.45	V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OL}=5mA			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1~INT_3($P6_0$~$P6_2$), EV_1~EV_3($P3_0$~$P3_2$) R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" Input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$ $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{SS}	−5		5	μA
I_{IH}	"H" Input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$ $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation $f(X_{IN})$=10MHz(Note 4)		6	10	mA

Note 4 : Only for M37450PFS (not contact in EPROM dissipation current).

A-D CONVERTER CHARACTERISTICS (V_{CC}=AV_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25°C, $f_{(X_{IN})}$=10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5.12V		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_C(\phi)$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference analog input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}=5V	2	7.5	10	kΩ
$I_{IADVREF}$	Reference analog input current	ADV_{REF}=5V	0.5	0.7	2.5	mA
V_{AVCC}	Analog power input			V_{CC}		V
V_{AVSS}	Analog power input			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Abusolute accuracy	V_{CC}=DAV_{REF}=5.12V			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power input			0		V
V_{DAVREF}	Analog power input		4		V_{CC}	V
I_{DAVREF}	Reference power input current		0	2.5	5	mA

BUILT-IN EPROM TYPE MICROCOMPUTERS

M50746E-XXXSP/FP
M50746ES/EFS

EPROM VERSION of M50746-XXXSP/FP

DESCRIPTION

The M50746E-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. The features of this chip are similar to those of the M50746-XXXSP except that this chip has a 49152-bit (6144 words×8 bits) EPROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the EPROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose EPROM writers can be used for the built-in EPROM, this chip is suitable for small quantity production runs.

The M50746ES and the M50746EFS are the window type.

The differences between the M50746E-XXXSP and the M50746E-XXXFP and between the M50746ES and the M50746EFS are the package outline and the power dissipation ability (absolute maximum ratings).

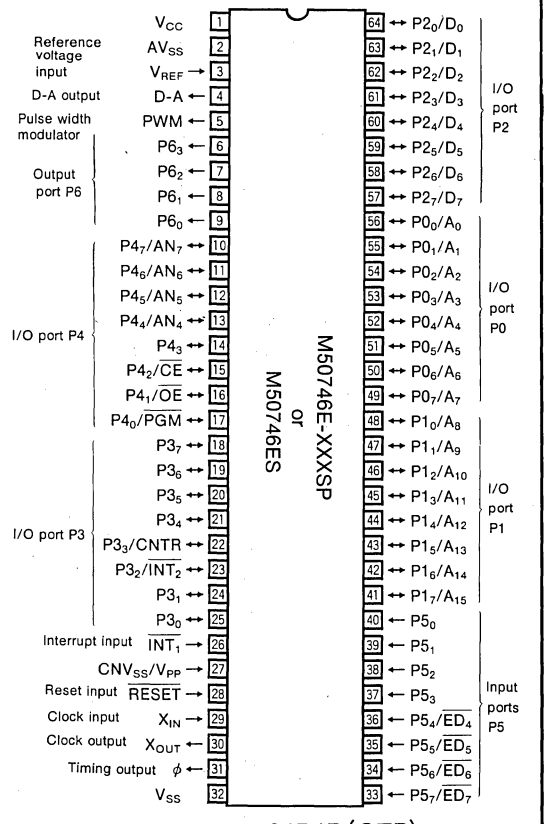
FEATURES

- Number of basic instructions 69
- Memory size EPROM ..... 6144 bytes
  RAM ..... 144 bytes
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply ..... 5V±5%
- Power dissipation
  normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting ..... 72 levels (Max.)
- Interrupt ..... 6 types, 5 vectors
- 8-bit timer 3
- Programmable I/O ports (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Output ports (Port P6) 4
- A-D converter ..... 8-bit successive approximation
- D-A converter
- 8-bit PWM function
- Watchdog timer
- EPROM (equivalent to the M5L2764)
  program voltage 21V

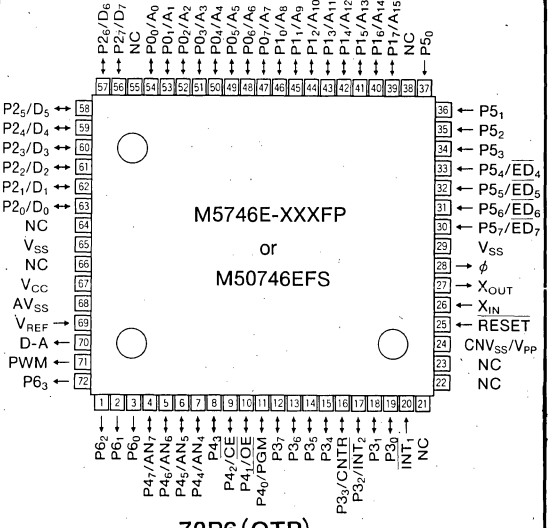
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



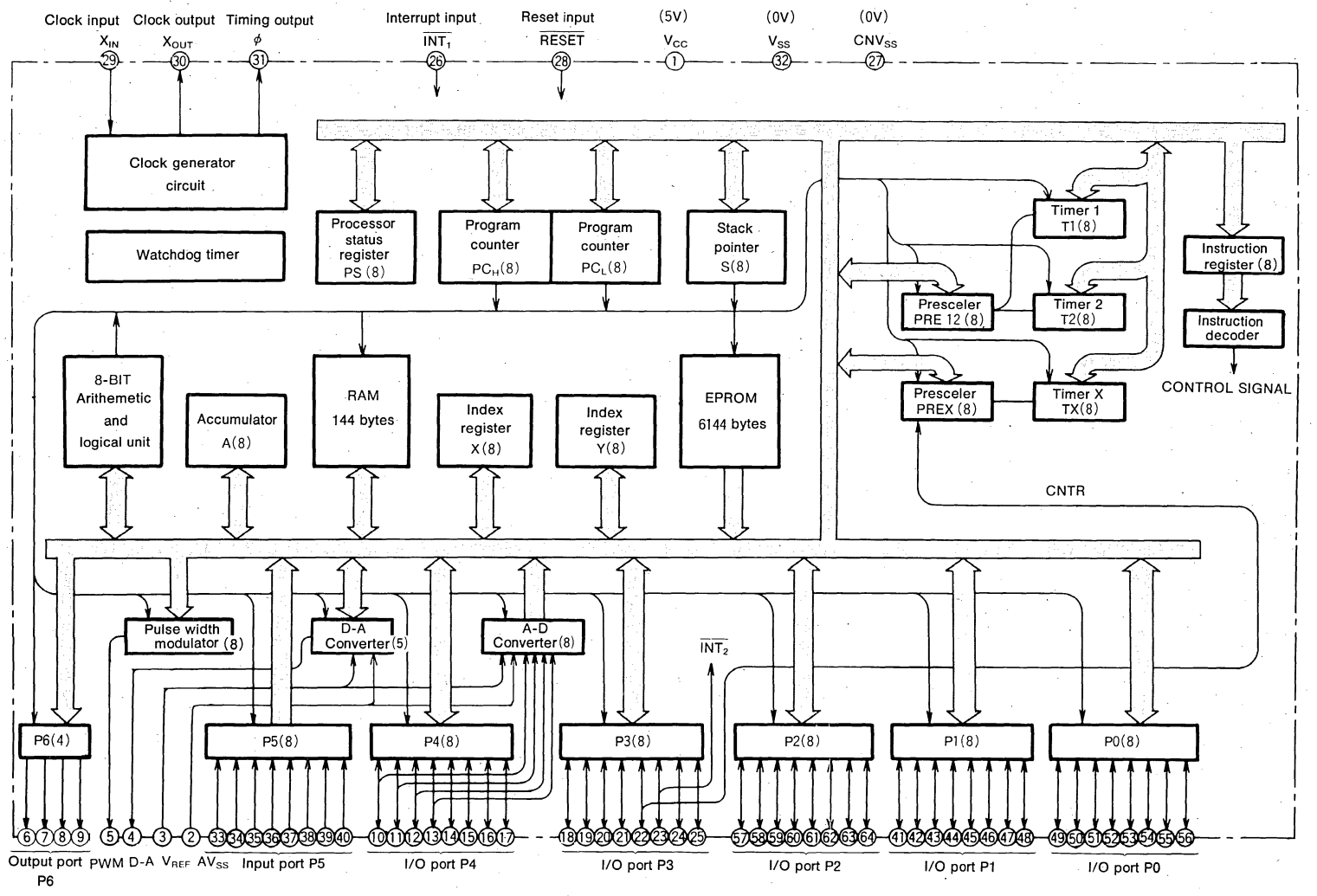
Outline 64P4B (OTP)
64S1B (Window)



Outline 72P6 (OTP)
72S6 (Window)

NC : No connection

M50746E-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M50746E-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction excution time			2μs (minimum instructions, at 4MHz frequency)
Memory capacity	EPROM		6144bytes (Note 1)
	RAM		144bytes
I/O ports	$\overline{INT_1}$	Input	1-bit×1
	P0, P1, P2, P3, P4	Input/output	8-bit×5(portion of P3 used with timer I/O and interrupt input)
	P5	Input	8-bit×1
	P6	Output	4-bit×1
Timers			8-bit prescaler×2+8-bit timer×3
A-D converter			8-bit× 1 (4 channels)
D-A converter			5-bit×1
Pulse width modulator			8-bit×1
Watchdog timer			15-bit×1
Subroutine nesting			72levels (max)
H nterrupt			2external interrupts, 3internal timer interrupts
Clock generating circuit			Built-in (externally connected ceramic or quartz crystal oscillator)
Supply voltage			5V±5%
Power dissipation	High-speed operation		15mW (at 4MHz frequency)
I/O characteristics	I/O voltage		12V (Ports P0, P1, P3, P4, P5, P6, $\overline{INT_1}$)
	Output current		5mA (Ports P0, P1, P2, P3, P4)
Memory expansion			Possibe
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M50746E-XXXSP	One time programming type	64-pin shrink plastic molded DIP
	M50746ES	Window type	64-pin shrink ceramic DIP
	M50746E-XXXFP	One time programming type	72-pin plastic molded QFP
	M50746EFS	Window type	72-pin ceramic QFP

Note 1 : The EPROM programming voltage is 21V (equivalent to the M5L2764).

PIN DESCRIPTION

Terminal	Mode	Name	Input/ Output	Functions
V_{CC} V_{SS}	Singl-chip /EPROM	Power supply		Supply 5V±5% to V_{CC} and 0V to V_{SS}.
CNV_{SS}	Singl-chip	CNV_{SS} input	Input	Connect to 0V.
	EPROM	V_{PP} input		Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V_{CC} conditions. If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
	EPROM	RESET input		Connect to V_{SS}.
X_{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation. If an external clock input is used, connect the clock input to the X_{IN} pin and open the X_{OUT} pin.
X_{OUT}		Clock output	Output	
ϕ	Single-chip /EPROM	Timing output	Output	For timing output.
$\overline{INT_1}$	Single-chip	Interrupt input	Input	Interrupt input INT_1.
	EPROM	Interrupt input	Input	Connect to 0V.
$P0_0$~$P0_7$	Singl-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction registers which can program each bit as input or output. It is set to input mode at reset. The output format is N-ch open drain.
	EPROM	Address input A_0~A_7	Input	P0 works as the lower 8 bit address input (A_0~A_7).
$P1_0$~$P1_7$	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port which has the same function as Port P0.
	EPROM	Address input A_8~A_{12}	Input	$P1_0$~$P1_4$ works as the higher 5 bit address inputs (A_8~A_{12}). Connect $P1_5$~$P1_7$ to V_{CC}.
$P2_0$~$P2_7$	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port which has the same function as Port P0. The output format is CMOS.
	EPROM	Data input/ output D_0~D_7	I/O	Port 2 works as an 8 bit data bus (D_0~D_7).
$P3_0$~$P3_7$	Single-chip	I/O port P3	I/O	Port P3, is an 8-bit I/O port, has the same function as Port P0. $P3_3$ and $P3_2$ are commonly used with I/O pin CNTR of timer X and the lowest interrupt input $\overline{INT_2}$, respectively.
	EPROM	Input Port P3	Input	Connect to 0V.
$P4_0$~$P4_7$	Single-chip	I/O port P4	I/O	Port P4 is an 8-bit I/O port which has the same function as Port P0. Ports $P4_7$~$P4_4$ are common with Analog inputs AN_7~AN_4.
	EPROM	Select mode	Input	$P4_2$, $P4_1$, $P4_0$ work as $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ inputs, respectively. Connect $P4_5$~$P4_7$ to 0V and $P4_4$ and $P4_3$ to 5V.
$P5_0$~$P5_7$	Single-chip	Input port	Input	Port P5 is an 8-bit input port. Ports $P5_7$~$P5_4$ have edge sence functions.
	EPROM	Input port	Input	Connect to 0V.
$P6_0$~$P6_3$	Single-chip	Output port	Output	Port P6 is a 8-bit output port. The output format is N-ch open drain.
	EPROM	Output port	Output	Connect to 0V.

PIN DESCRIPTION

Terminal	Mode	Name	Input/ Output	Functions
AV_{SS}	Single-chip	Analog voltage input	Input	GND pin for the A-D and D-A converters.
	EPROM	Analog voltage input	Input	Connect to 0V.
V_{REF}	Single-chip	Reference voltage input	Input	Referrence input for A-D and D-A converters.
	EPROM	Reference voltage input	Input	Connect to 0V.
D-A	Single-chip	D-A output	Output	D-A converter output pin
	EPROM	D-A output	Output	Connect to 0V.
PWM	Single-chip	PWM output	Output	Pulse width modulation output pin (N-ch open drain format).
	EPROM	PWM output	Output	Connect to 0V.

EPROM MODE

The M50746E-XXXSP features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 and Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P4_0 \sim P4_2$, and CNV_{SS} are used for the EPROM (equivalent to the M5L2764). When in this mode, the built-in EPROM can be written to or read from using these pins in the same way as with the M5L2764. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1 Pin function in EPROM programming mode

	M50746E-XXXSP/FP	M5L2764
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0 \sim P1_4$	$A_0 \sim A_{12}$
Data I/O	Port P2	$D_0 \sim D_7$
$\overline{CE}$	$P4_2/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P4_1/\overline{OE}$	$\overline{OE}$
$\overline{PGM}$	$P4_0/\overline{PGM}$	$\overline{PGM}$

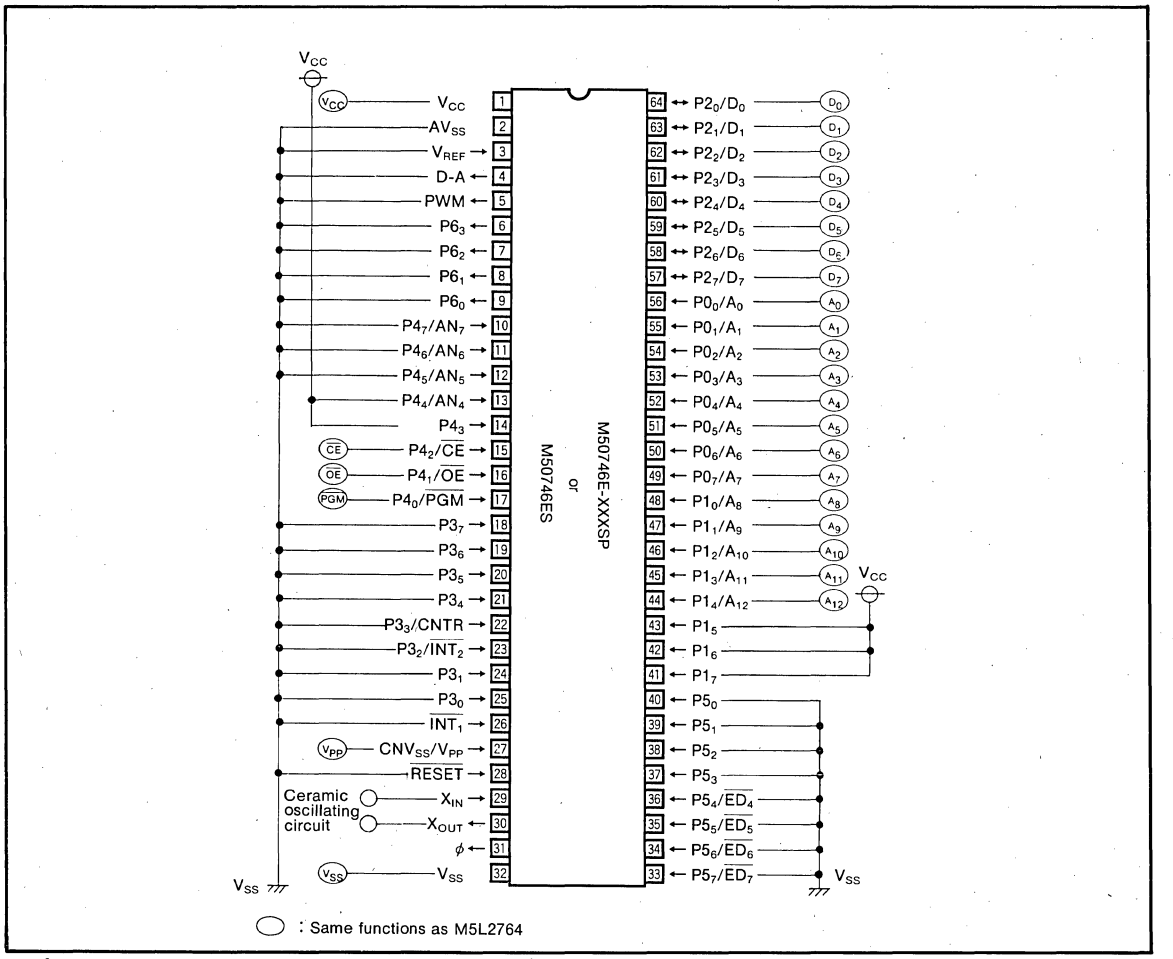


Fig.1 Pin connection in EPROM programming mode (M50746E-XXXSP, M50746ES)

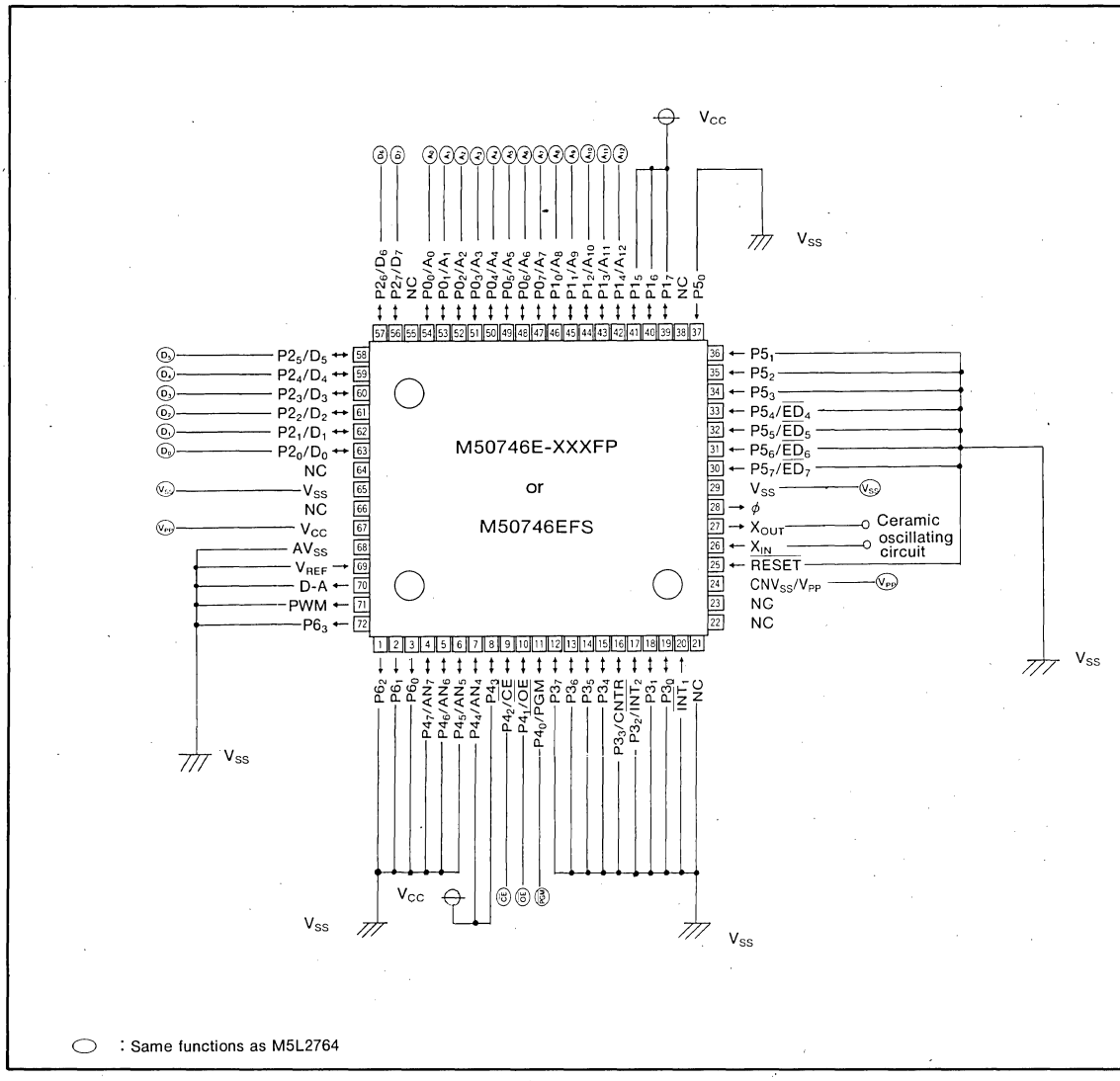


Fig.2 Pin connection in EPROM progamming mode (M50746E-XXXFP, M50746EFS)

EPROM READING, WRITING AND ERASING

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and the $\overline{PGM}$ pin to a "H" level. Input the address of the data ($A_0 \sim A_{12}$) to be read and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the EPROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{12}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the $\overline{PGM}$ pin to a "L" level to begin writing.

Notes on Writing

When using an EPROM writer, the address range should be between 0800_{16} and $1FFF_{16}$. When data is written between addresses 0000_{16} and $1FFF_{16}$, fill addresses 0000_{16} to $07FF_{16}$ with 00_{16}.

Erasing

Data can only be erased on the M50746ES and the M50746EFS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is $15W \cdot s/cm^2$.

NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage (21V) is used to write data, care should be taken when turning on the EPROM writer's power.

Table 2 I/O signal in each mode

Mode \ Pin	$\overline{CE}$(15)	$\overline{OE}$(16)	$\overline{PGM}$(17)	V_{PP}(27)	V_{CC}(1)	Data I/O (57~64)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse($V_{IH} \rightarrow V_{IL}$)	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} With the output transistor cut-off	−0.3∼7	V
V_I	Input voltage X_{IN}		−0.3∼7	V
V_I	Input voltage $P2_0$∼$P2_7$, $P4_4$∼$P4_7$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, $P5_0$∼$P5_7$, $\overline{INT_1}$		−0.3∼13	V
V_I	Input voltage CNV_{SS}, $\overline{RESET}$		−0.3∼13 (Note 1)	V
V_O	Output voltage $P2_0$∼P2, $P4_4$∼$P4_7$, X_{OUT}, ϕ, D-A		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, $P6_0$∼$P6_3$, PWM		−0.3∼13	V
P_d	Power dissipation	T_a=25℃	1000(Note2)	mW
T_{opr}	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : In EPROM programming mode, CNV_{SS} is 22.0V
Note 2 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, PWM (Note 4)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$∼$P6_3$ (Note 4)			15	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, PWM (Note 3)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0$∼$P6_3$ (Note 3)			7	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$∼$P2_7$ (Note 4)			−10	mA
$I_{OH(avg)}$	"H" average output current $P2_0$∼$P2_7$ (Note 4)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

Note 3 : The average output currents $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
4 : Do not allow the combined low- level output current of ports P0, P1, P2, P3, P4, P6, and PWM to exceed 80mA.
Do not allow the combined high- level output current of port P2 to exceed 50mA.
5 : "H" input voltage of ports' P0, P1, P3, $P4_0$∼$P4_3$, P5 and $\overline{INT_1}$ is available up to +12V.

ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=5V, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P2_0$~$P2_7$	I_{OH}=−10mA		3			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA		3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_3$, PWM	I_{OL}=10mA				2	V
V_{OL}	"L" output voltage ϕ	I_{OL}=5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$	When used as $\overline{INT_2}$ input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_3$	When used as CNTR input		0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}			0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=0V				−5	μA
I_{IL}	"L" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I=0V				−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=12V				12	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, $P2_0$~$P2_7$, $P4_4$~$P4_7$	V_I=5V				5	μA
V_{RAM}	RAM retention voltage	When clock disabled		2			V
I_{CC}	Supply current	ϕ, X_{OUT}, and D-A pins opened, other pins at V_{SS}, and A-D converter in the finished condition.	$f_{(X_{IN})}$=4MHz Square wave		3	6	mA
			At clock stop Ta=25°C			1	μA
			At clock stop Ta=70°C			10	μA

A-D CONVERTER CHARACTERISTICS (T_a=25°C, V_{CC}=5V, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute precision	V_{REF}=V_{CC},			±3	LSB
R_{LADDER}	Ladder resistance	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS (T_a=25°C, V_{CC}=5V, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			5	Bits
—	Error in full scale range	V_{REF}=V_{CC},			±1	%
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
R_O	Output resistance	V_{REF}=V_{CC}			3	kΩ
V_{REF}	Reference voltage		4		V_{CC}	V

TIMING REQUIREMENTS

Single-Chip mode (T_a=25℃, V_{CC}=5V±5%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		270			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		20			ns
t_c	External clock input cycle time		250			ns
t_w	External clock input pulse width		75			ns
t_r	External clock rise-time				25	ns
t_f	External clock fall-time				25	ns

Eva-Chip mode (T_a=25℃, V_{CC}=5V±5%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

Memory expanding mode microprocessor mode

(T_a=25℃, V_{CC}=5V±5%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		30			ns

SWITCHING CHARACTERISTICS

Single-Chip mode (T_a=25℃, V_{CC}=5V±5%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 2			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time	Fig. 2			230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 3			230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig. 2			230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time	Fig. 2			230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time	Fig. 2			230	ns

Eva-Chip mode (T_a=25℃, V_{CC}=5V±5%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 2			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 3			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig. 2			250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns

Memory expanding mode microprocessor mode

(T_a=25℃, V_{CC}=5V±5%, V_{SS}=0V, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 2			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 3			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig. 2			250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

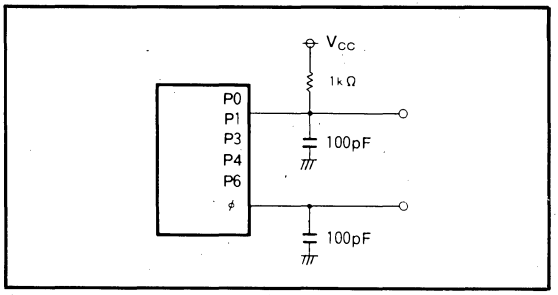


Fig.2 Measurement circuit for ports P0, P1, P3, P4, P6

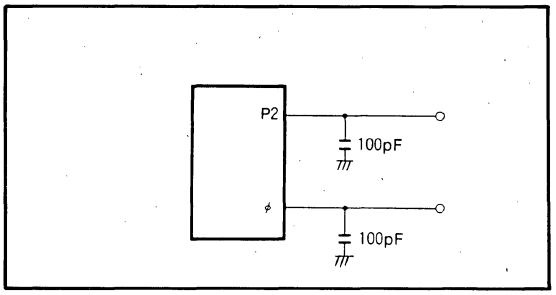
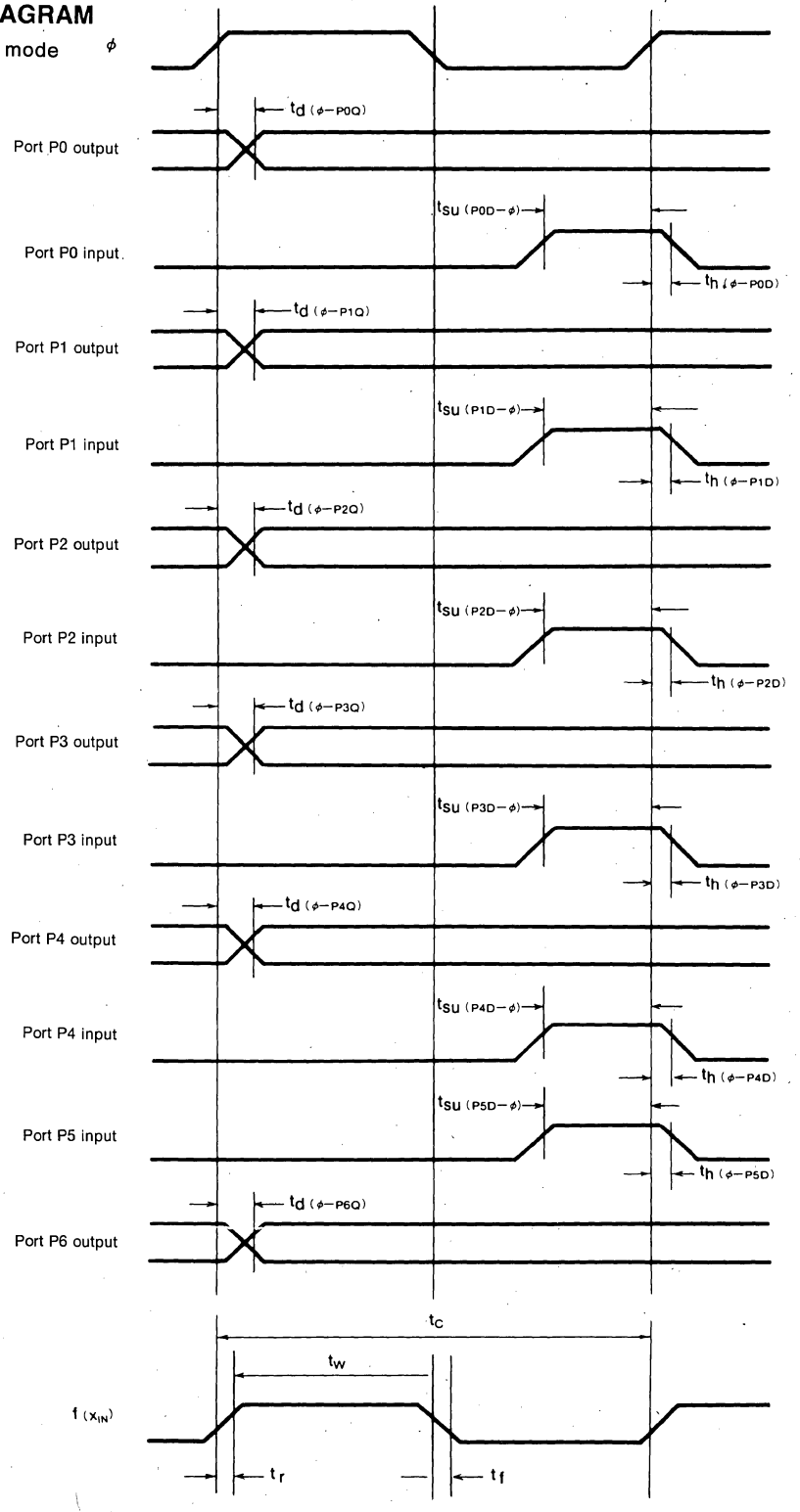


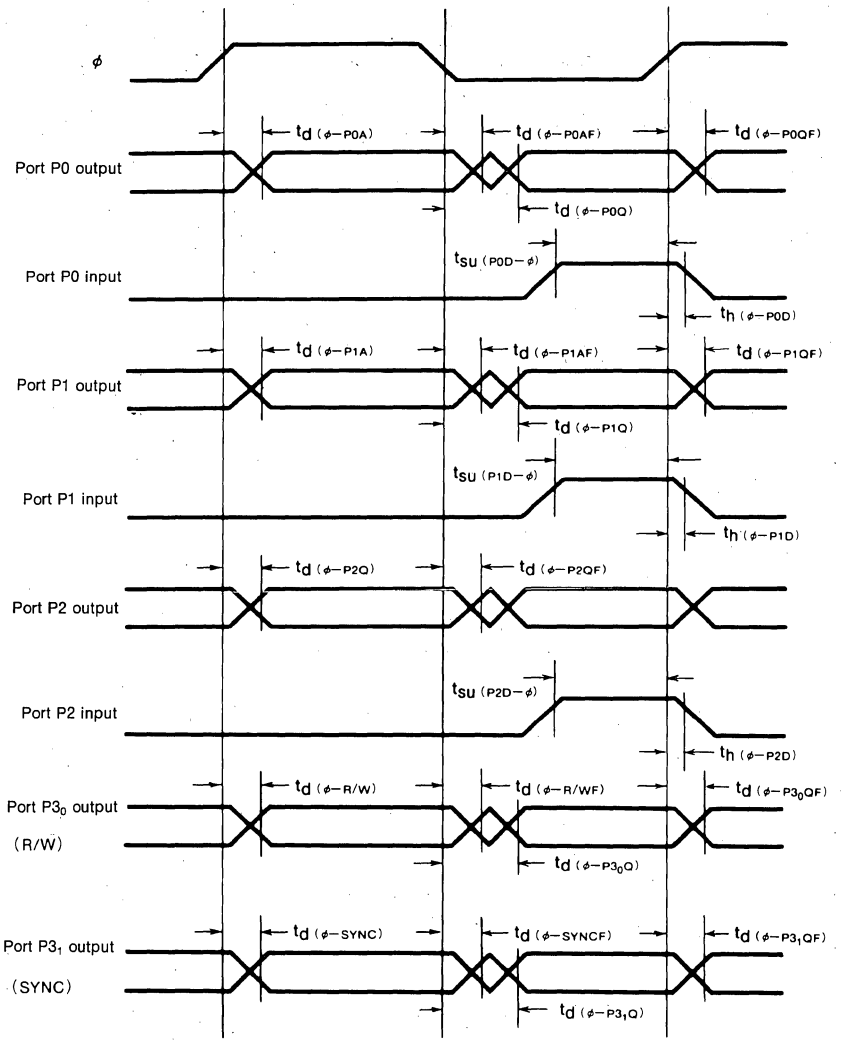
Fig.3 Measurement circuit for port P2

TIMING DIAGRAM

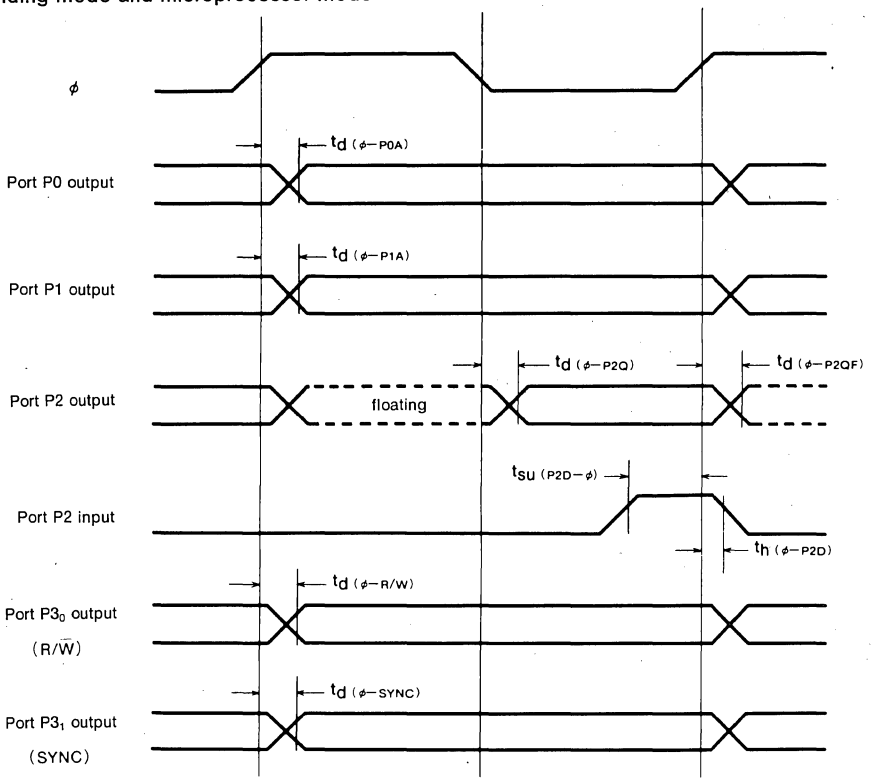
In single-chip mode



In eva-chip mode



In memory expanding mode and microprocessor mode



M50747E-XXXSP/FP
M50747ES/EFS

EPROM VERSION of M50747-XXXSP/FP

DESCRIPTION

The M50747E-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. The features of this chip are similar to those of the M50747-XXXSP except that this chip has a 65536-bit (8192 words×8 bits) EPROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the EPROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose EPROM writers can be used for the built-in EPROM, this chip is suitable for small quantity production runs.

The M50747ES and the M50747EFS are the window type. The differences between the M50747E-XXXSP and the M50747E-XXXFP and between the M50747ES and the M50747EFS are the package outline and the power dissipation ability(absolute maximum ratings).

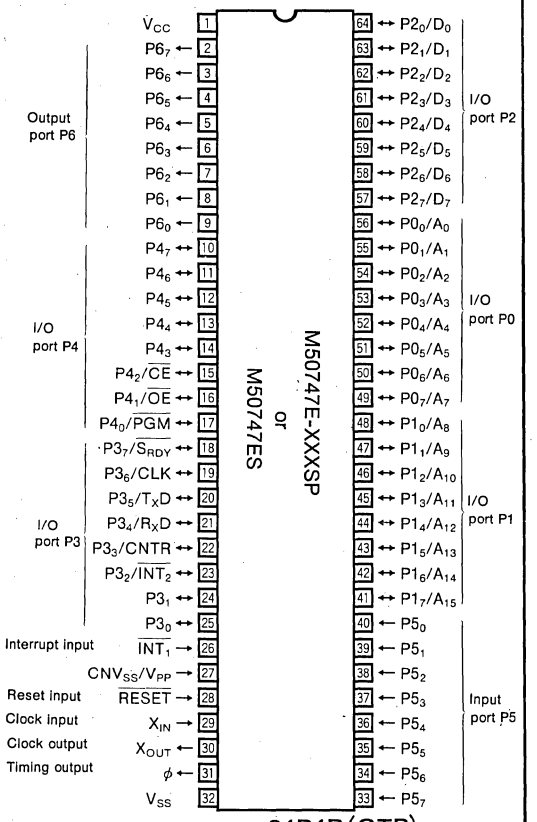
FEATURES

- Number of basic instructions 69
- Memory size EPROM ..... 8192 bytes
  RAM ..... 256 bytes
- Instruction execution time
  ..... 1μs (minimum instructions at 8MHz frequency)
- Single power supply ..... 5V±5%
- Power dissipation
  normal operation mode (at 8MHz frequency) 30mW
- Subroutine nesting ..... 128 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as serial I/O)
- Programmable I/O ports (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Output ports (Port P6) 8
- Serial I/O (Clock synchronized or UART) 1
- EPROM (equivalent to the M5L2764)
  program voltage 21V

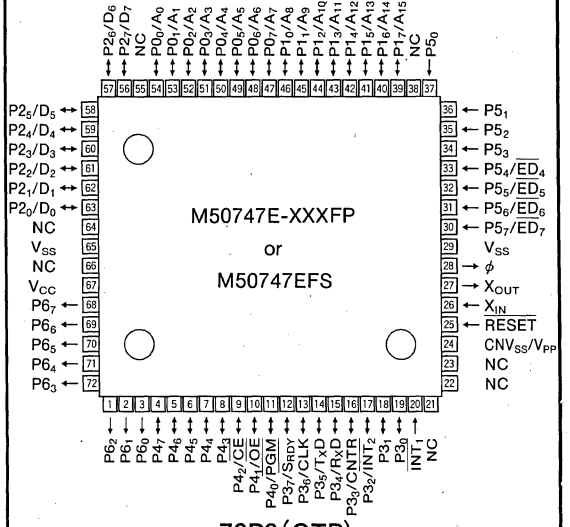
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B (OTP)
64S1B (Window)

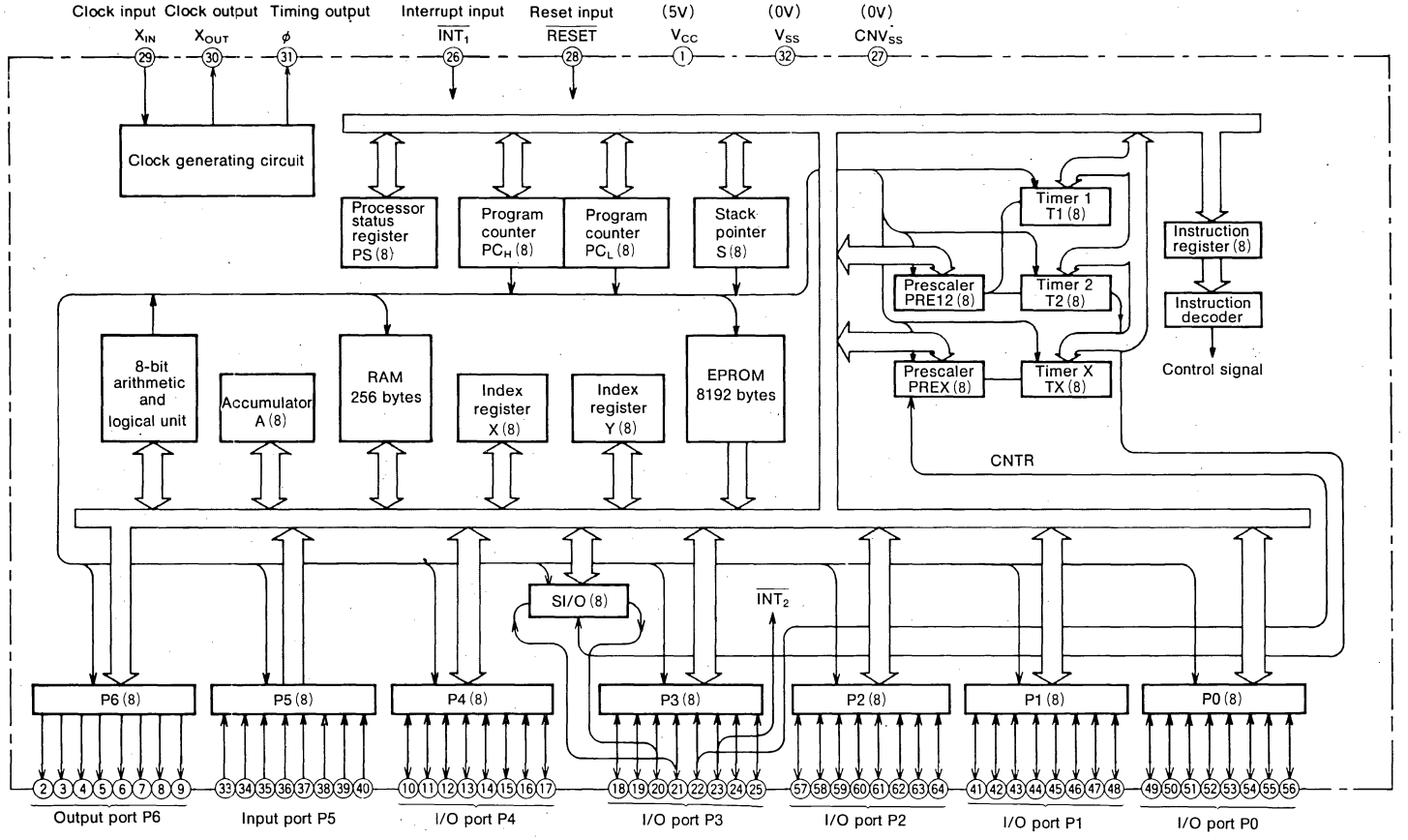


Outline 72P6 (OTP)
72S6 (Window)

NC : No connection

MITSUBISHI ELECTRIC

M50747E-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M50747E-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 8MHz of frequency)
Clock frequency			8MHz
Memory size	EPROM		8192bytes (Note 1)
	RAM		256bytes
Input/output port	$\overline{INT_1}$	Input	1-bit×1
	P0, P1, P2, P3, P4	Input/Output	8-bit×5 (Part of P3 are common with Input/output of serial I/O, timer I/O, and $\overline{INT_2}$ interrupt input)
	P5	Input	8-bit×1
	P6	Output	8-bit×1
Serial I/O			8-bit or 9-bit×1
Timers			8-bit prescaler×2+8-bit timer×3 (8-bit timer×2 when serial I/O is used)
Subroutine nesting			128levels (max.)
Interrupts			Two external interrupt (1 of external interrupt is in common with port $P3_2$) Three timer interrupt (or timer×2, serial I/O×1)
Clock generating circuit			Built-in (externally connected ceramic or quartz crystal oscillator)
Supply voltage			5V±5%
Power dissipation	at high-speed operation		30mW (at 8MHz frenquency)
Input/Output characteristics	Input/output voltage		5V
	Output current		10mA (Ports P3, P4, P6)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package	M50747E-XXXSP	One time programming type	64-pin shrink plastic molded DIP
	M50747ES	Window type	64-pin shrink ceramic DIP
	M50747E-XXXFP	One time programming type	72-pin plastic molded QFP
	M50747ES	Window type	72-pin ceramic QFP

Note 1 : The EPROM programming voltage is 21V (equivalent to the M5L2764).

PIN DESCRIPTION

Terminal	Mode	Name	Input/ Output	Functions
V_{CC} V_{SS}	Singl-chip /EPROM	Power supply		Supply 5V±5% to V_{CC} and 0V to V_{SS}.
CNV_{SS} /V_{PP}	Singl-chip	CNV_{SS} input		Connect to 0V.
	EPROM	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V_{CC} conditions. If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
	EPROM	RESET input		Connect to V_{SS}.
X_{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation. If an external clock input is used, connect the clock input to the X_{IN} pin and open the X_{OUT} pin.
X_{OUT}		Clock output	Output	
ϕ	Single-chip /EPROM	Timing output	Output	For timing output.
$\overline{INT_1}$	Single-chip	Interrupt input	Input	Interrupt input $\overline{INT_1}$.
	EPROM	Interrupt input	Input	Connect to 0V.
$P0_0$~$P0_7$	Singl-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with an I/O direction register which can program each bit as input or output. It is set to input mode at reset. The output format is CMOS.
	EPROM	Address input A_0~A_7	Input	P0 works as the lower 8 bit address input (A_0~A_7).
$P1_0$~$P1_7$	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port which has the same function as Port P0.
	EPROM	Address input A_8~A_{12}	Input	$P1_0$~$P1_4$ works as the higher 5 bit address inputs (A_8~A_{12}). Connect $P1_5$~$P1_7$ to V_{CC}.
$P2_0$~$P2_7$	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port which has the same function as Port P0.
	EPROM	Data input/ output D_0~D_7	I/O	Port 2 works as an 8 bit data bus (D_0~D_7).
$P3_0$~$P3_7$	Single-chip	I/O port P3	I/O	Port P3, is an 8-bit I/O port, has the same function as Port P0. When serial I/O is used, $P3_6$, $P3_5$ and $P3_4$ work as CLK, TxD, RxD pins respectively. When clock synchronous serial I/O is used, $P3_7$ works as $\overline{S_{RDY}}$. $P3_3$ and $P3_2$ are commonly used with I/O pin CNTR of timer X and the lowest interrupt input $\overline{INT_2}$, respectively.
	EPROM	Input Port P3	Input	Connect to 0V.
$P4_0$~$P4_7$	Single-chip	I/O port P4	I/O	Port P4 is an 8-bit I/O port which has the same function as Port P0.
	EPROM	Select mode	Input	$P4_2$, $P4_1$, $P4_0$ work as $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ inputs, respectively. Connect $P4_5$~$P4_7$ to 0V and $P4_4$ and $P4_3$ to 5V.
$P5_0$~$P5_7$	Single-chip	Input port	Input	Port P5 is an 8-bit input port.
	EPROM	Input port	Input	Connect to 0V.
$P6_0$~$P6_7$	Single-chip	Output port	Output	Port P6 is a 8-bit output port. The output format is CMOS.
	EPROM	Output port	Output	Connect to 0V.

EPROM MODE

The M50747E-XXXSP features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 and Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P4_0$~$P4_2$, and CNV_{SS} are used for the EPROM (equivalent to the M5L2764). When in this mode, the built-in EPROM can be written to or read from using these pins in the same way as with the M5L2764. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1 Pin function in EPROM programming mode

	M50747E-XXXSP/FP	M5L2764
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0$~$P1_4$	A_0~A_{12}
Data I/O	Port P2	D_0~D_7
$\overline{CE}$	$P4_2/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P4_1/\overline{OE}$	$\overline{OE}$
$\overline{PGM}$	$P4_0/\overline{PGM}$	$\overline{PGM}$

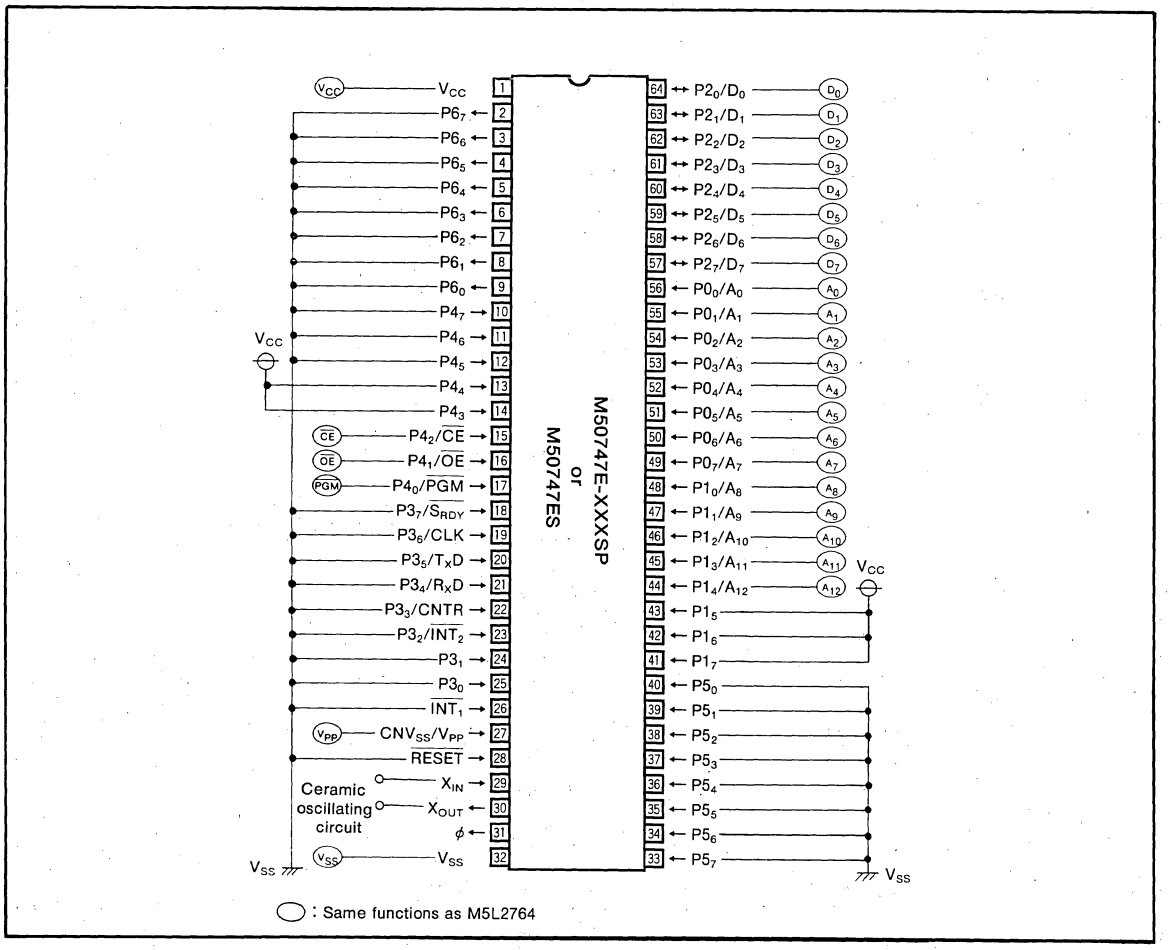


Fig.1 Pin connection in EPROM programming mode (M50747E-XXXSP, M50747ES)

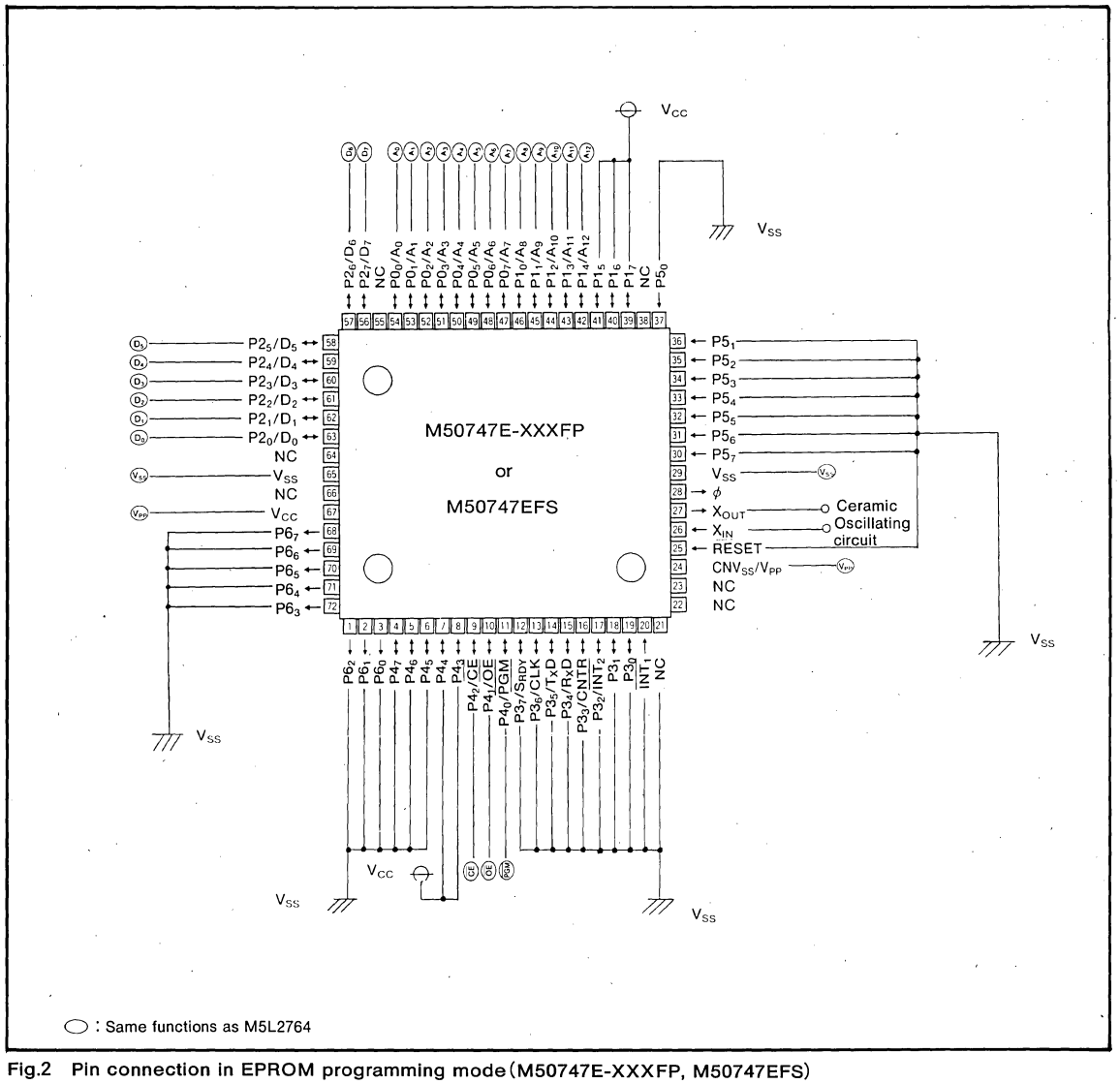


Fig.2 Pin connection in EPROM programming mode (M50747E-XXXFP, M50747EFS)

EPROM READING, WRITING AND ERASING

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and the $\overline{PGM}$ pin to a "H" level. Input the address of the data (A_0~A_{12}) to be read and the data will be output to the I/O pins D_0~D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the EPROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0~A_{12}, and the data to be written is input to pins D_0~D_7. Set the $\overline{PGM}$ pin to a "L" level to begin writing.

Erasing

Data can only be erased on the M50747ES and the M50747EFS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15W·s/cm^2.

NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage (21V) is used to write data, care should be taken when turning on the EPROM writer's power.

Table 2 I/O signal in each mode

Mode \ Pin	$\overline{CE}$(15)	$\overline{OE}$(16)	$\overline{PGM}$(17)	V_{PP}(27)	V_{CC}(1)	Data I/O (57~64)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse(V_{IH}→V_{IL})	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off	−0.3~7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, $\overline{INT_1}$, $P5_0$~$P5_7$		−0.3~7	V
V_I	Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$,		−0.3~V_{CC}+0.3	V
V_I	Input voltage, CNV_{SS}		−0.3~13 (Note 1)	V
V_O	Output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$, X_{OUT}, ϕ		−0.3~V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 2)	mW
T_{opr}	Operating temperature range		−10~70	℃
Tstg	Storage temperature range		−40~125	℃

Note 1 : In EPROM programming mode, CNV_{SS} is 22.0V.
2 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5V±5%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$ (Note 3)			5	mA
$I_{OH(peak)}$	"H" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7P6_0$~$P6_7$, (Note 3)			−5	mA
$f(X_{IN})$	Internal clock oscillating frequency			8	MHz

Note 3 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms
4 : Total of $I_{OL(peak)}$, of ports P0, P1, and P2 is below 20mA
Total of $I_{OH(peak)}$, of ports P0, P1, and P2 is below 20mA
Total of $I_{IL(peak)}$, of ports P3, P4, and P6 is below 80mA
Total of $I_{OH(peak)}$, of ports P3 and P4 is 20mA
Total of $I_{OH(peak)}$, of ports P6 is below 60mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OH} = −10mA		3			V
V_{OH}	"H" output voltage, ϕ,	I_{OH} = −2.5mA		3			V
V_{OL}	"L" output voltage, $P0_0$~ $P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$	I_{OL} = 10mA				2	V
V_{OL}	"L" output voltage, ϕ	I_{OL} = 5mA				2	V
V_{T+}−V_{T-}	Hysteresis, $P3_6$	When used as CLK input		0.3		1	V
V_{T+}−V_{T-}	Hysteresis, $\overline{INT_1}$			0.3		1	V
V_{T+}−V_{T-}	Hysteresis, $P3_2$	When used as $\overline{INT_2}$ pin		0.3		1	V
V_{T+}−V_{T-}	Hysteresis, $P3_3$	When used as CNTR input		0.3		1	V
V_{T+}−V_{T-}	Hysteresis, $\overline{RESET}$				0.5	0.7	V
V_{T+}−V_{T-}	Hysteresis, X_{IN}			0.1		0.5	V
I_{IL}	"L" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 0V				−5	μA
I_{IH}	"H" input current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I = 5V				5	μA
V_{RAM}	RAM retention voltage	STOP mode		2			V
I_{CC}	Supply current	Output pins are opened others to V_{SS}	$f_{(X_{IN})}$=8MHz Square wave		6	12	mA
			At clock stop T=25℃			1	μA
			At clock stop T_a=70℃			10	μA

TIMING REQUIREMENTS

Single-chip mode (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input set-up time		200			ns
$t_{su(P1D-\phi)}$	Port P1 input set-up time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input set-up time		200			ns
$t_{su(P3D-\phi)}$	Port P3 input set-up time		200			ns
$t_{su(P4D-\phi)}$	Port P4 input set-up time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input set-up time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		20			ns
t_C	External clock input cycle time		125			ns
t_W	External clock input pulse width		62			ns
t_r	External clock rising edge time				20	ns
t_f	External clock falling edge time				20	ns

Eva-chip mode and microprocessor mode

(V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input set-up time		200			ns
$t_{su(P1D-\phi)}$	Port P1 input set-up time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input set-up time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

Memory expanding mode and microprocessor mode

(V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input set-up time		150			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25°C, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.2			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns

Eva-chip mode (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25°C, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.2			150	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				150	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				150	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				150	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				150	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				150	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				150	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				150	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				150	ns

Memory expanding mode and microprocessor mode

(V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25°C, $f_{(X_{IN})}$ = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig.2			150	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				150	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time		30		150	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time				150	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				150	ns

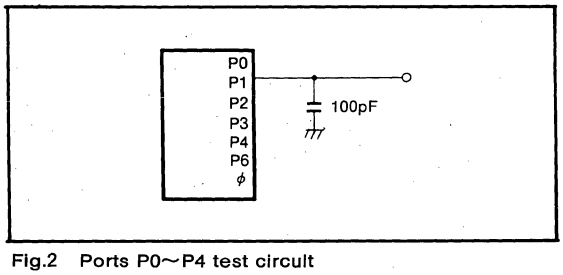
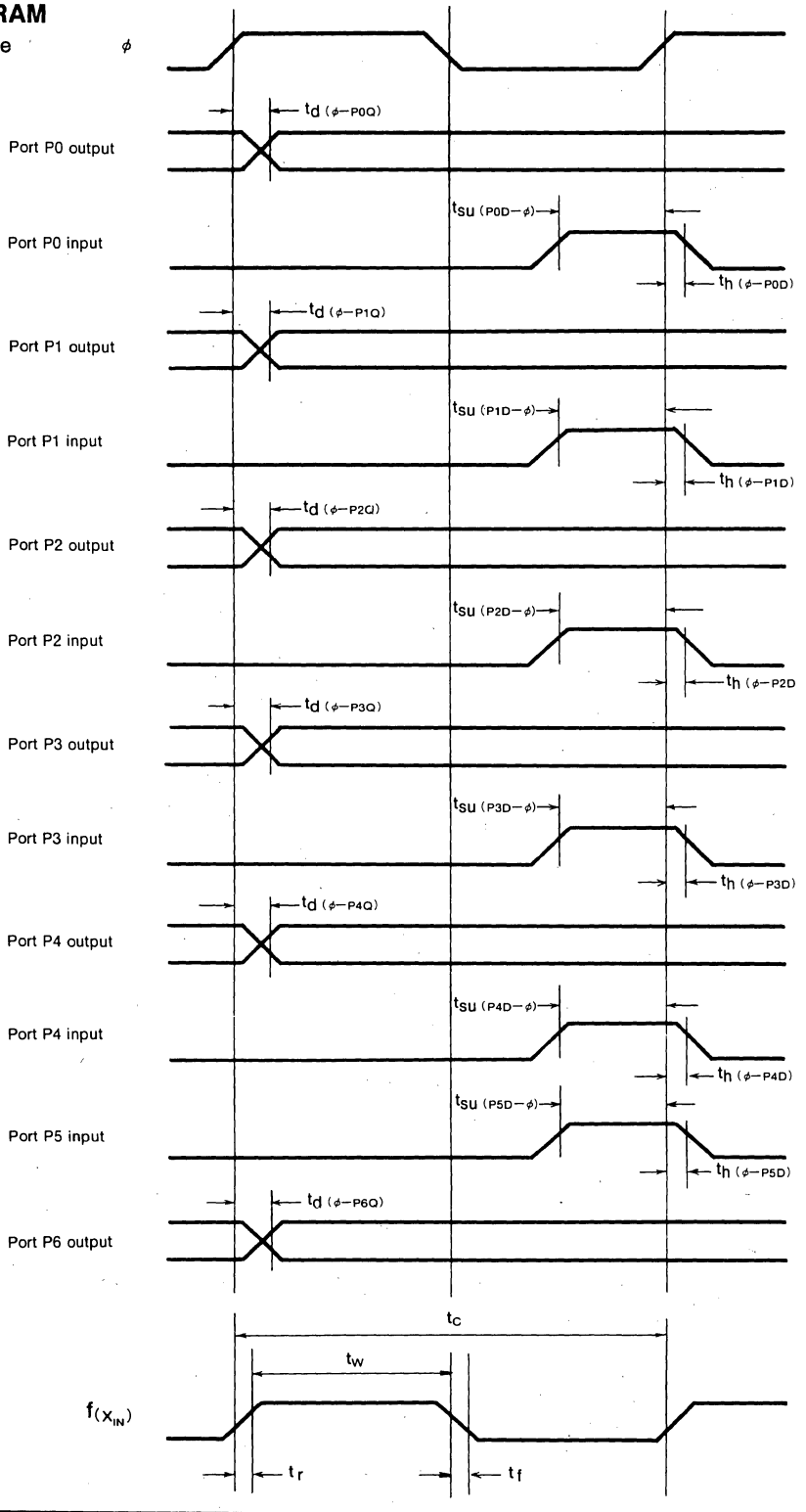


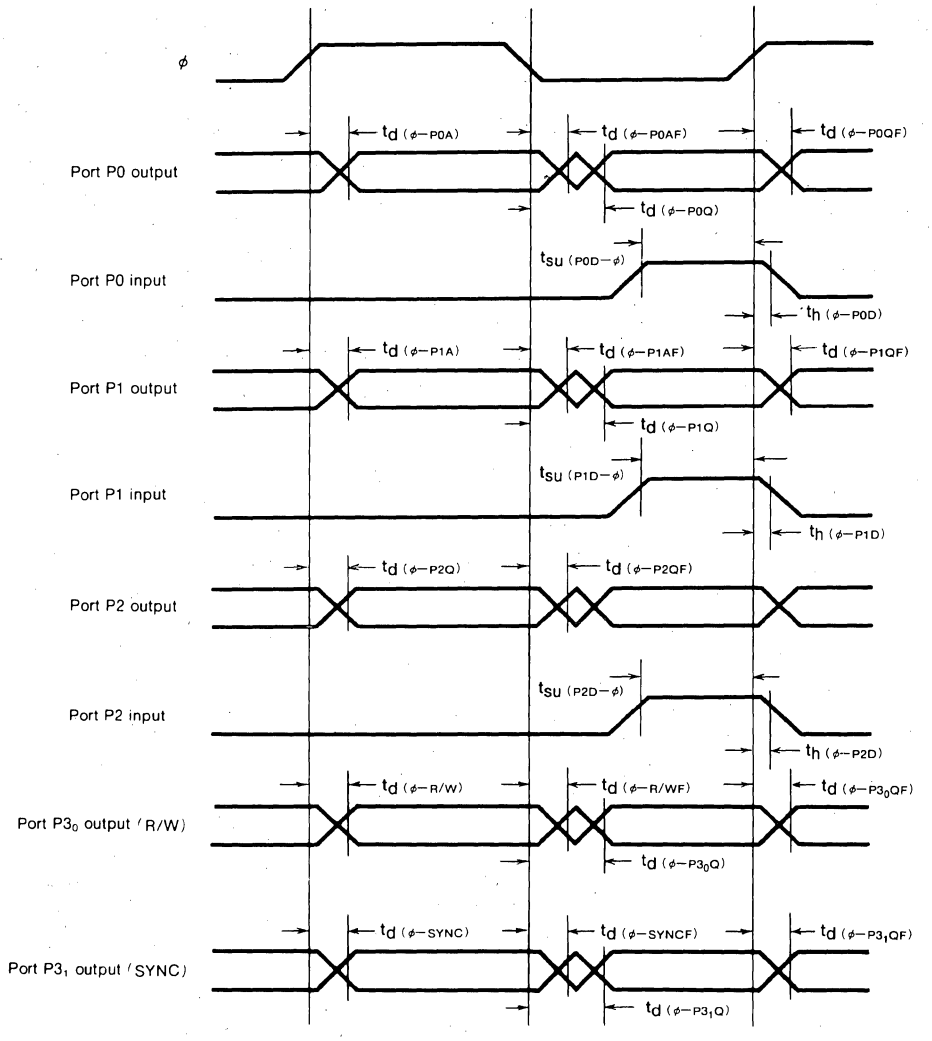
Fig.2 Ports P0~P4 test circuit

TIMING DIAGRAM

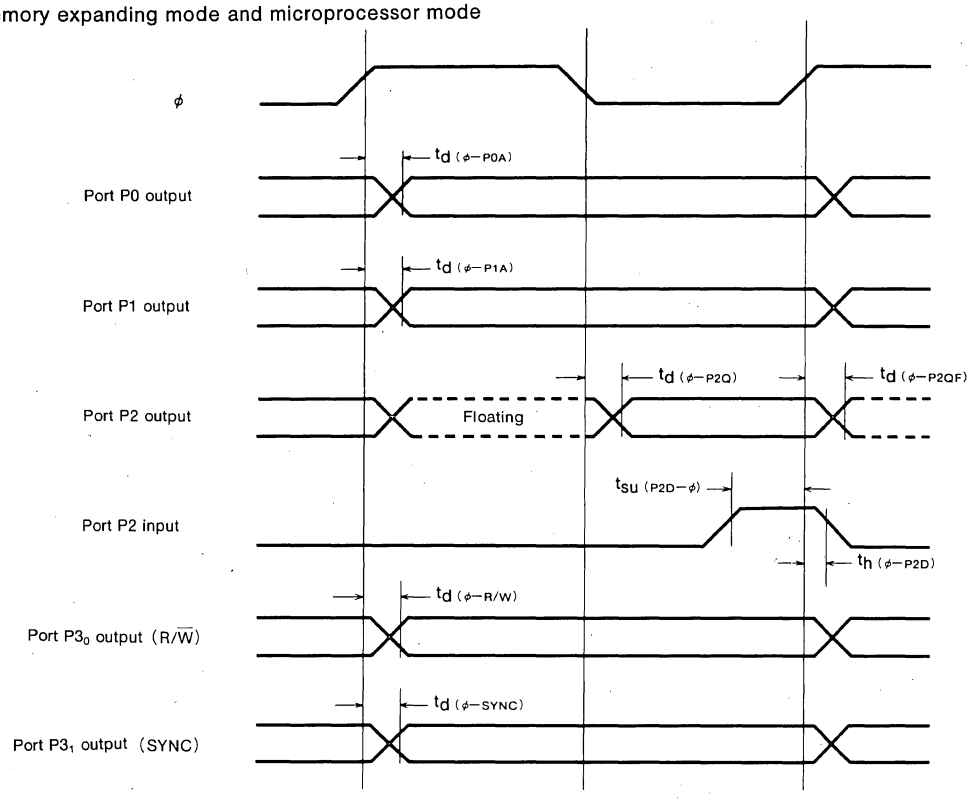
In single-chip mode



In eva-chip mode



In memory expanding mode and microprocessor mode



PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

M50944E-XXXSP/FP
M50944ES

EPROM VERSION of M50944-XXXSP/FP

DESCRIPTION

The M50944E-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. The features of this chip are similar to those of the M50944-XXXSP except that this chip has a 98304-bit (12288 words×8 bits) EPROM built-in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the EPROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose EPROM writers can be used for the build-in EPROM, this chip is suitable for small quantity production runs.

The M50944ES is the window type. The differences between the M50944E-XXXSP and the M50944E-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

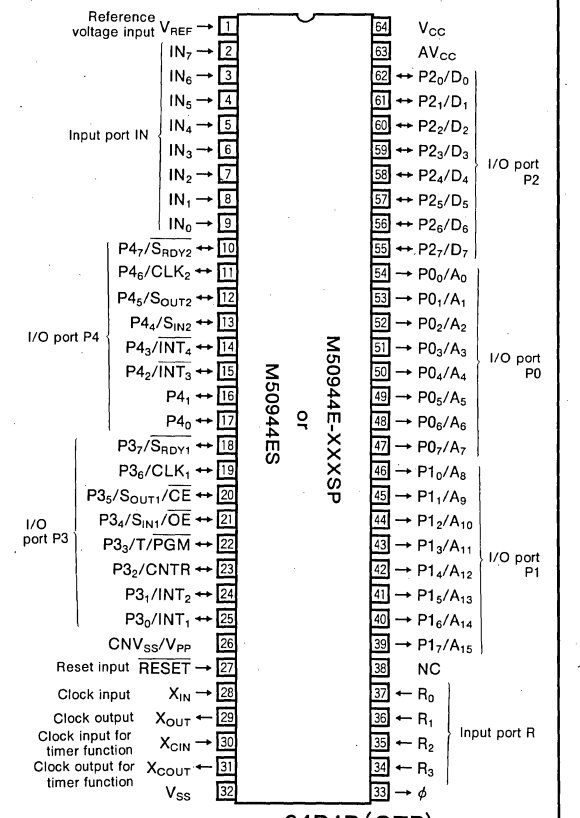
FEATURES

- Number of basic instructions 69
- Memory size EPROM ..... 12288 bytes
  RAM ..... 192 bytes
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply ..... 5V±5%
- Power dissipation
  normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 10 types, 5 vectors
- 8-bit timer ..... 7 (6 when used as serial I/O)
- Serial I/O ..... 8-bit×2
- Devider for serial I/O 1
- Interrupt request distinguish register ..... 8-bit×2
- Programmable I/O ports (Ports P3, P4) 16
- Middle-voltage programmable ports
  (Ports P0, P1, P2) 24
- Input port (Ports R, IN) 12
- A-D coversion 8-bit, 8-channel
- Two clock generator circuits (One is for main clock, the other is for clock function)
- EPROM (equivalent to the M5L27128)
  program voltage 21V

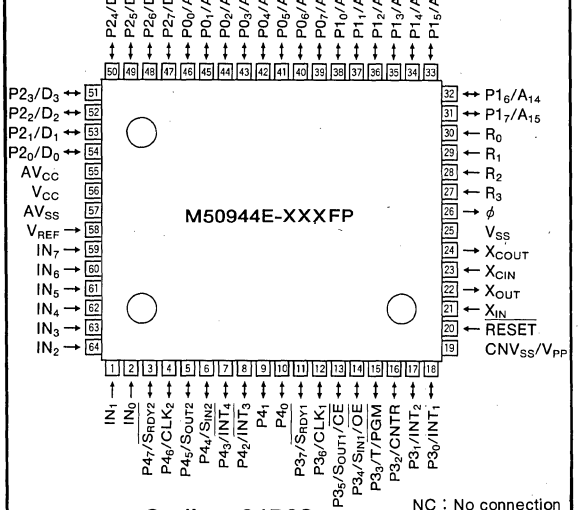
APPLICATION

Camera, Office automation equipment, VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B (OTP)
64S1B (Window)

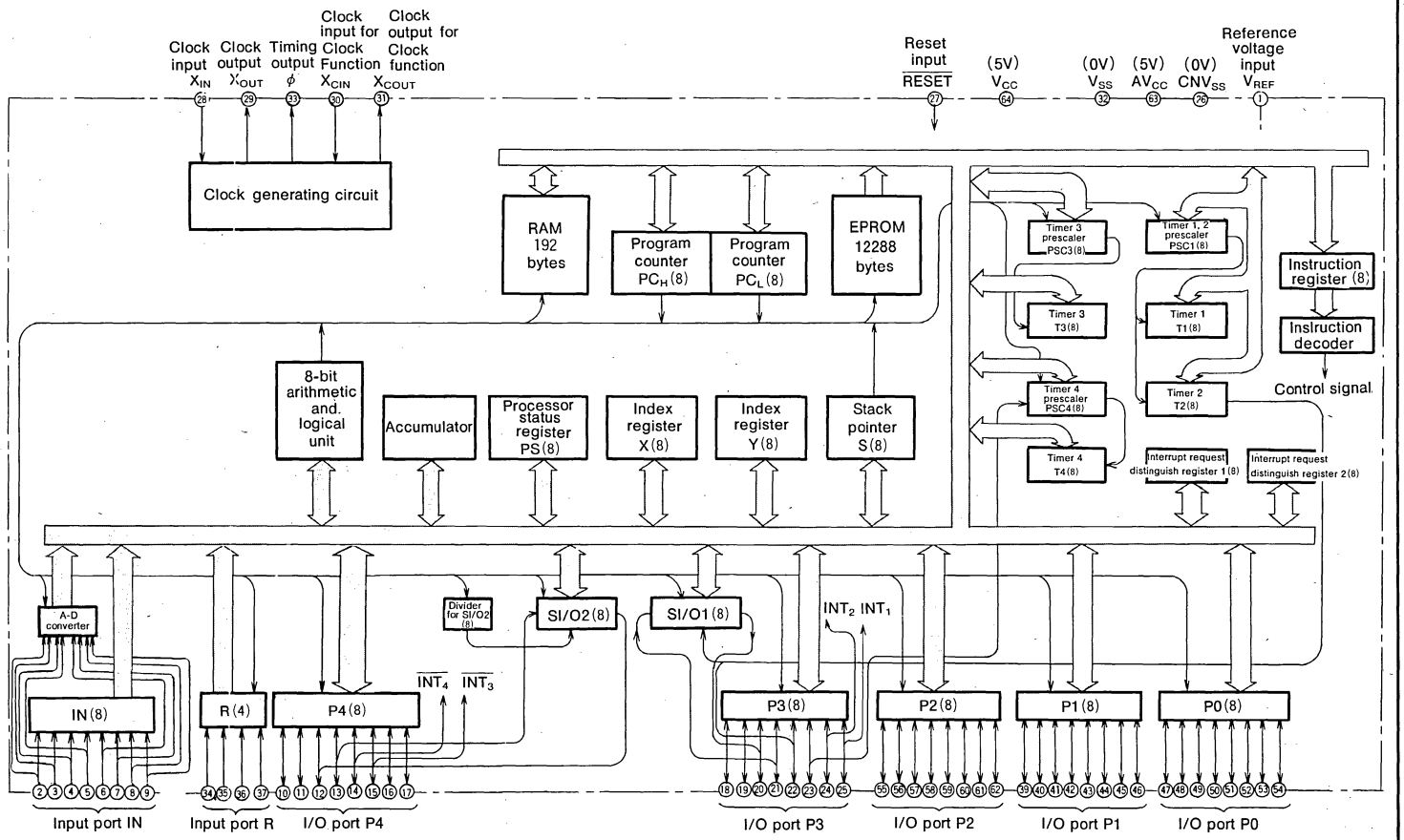


Outline 64P6S

NC : No connection

MITSUBISHI ELECTRIC

M50944E-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M50944E-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency).
Clock frequency			4.2MHz (main clock input), 32kHz (for clock function)
Memory size	EPROM		12288bytes (Note 1)
	RAM		192bytes
Input/Output port	P0, P1, P2, P3, P4	I/O	8-bit×5
	IN	Input	8-bit×1
	R	Input	4-bit×1
Serial I/O			8-bit×2
Timers			8-bit prescaler×3+8-bit timer×4(3 when serial I/O is used)
Subroutine nesting			96 Levels (max)
Interrupts			Four external interrupts, four timer interrupts (or three timers, One serial I/O)
Clock generating circuit			Two built-in circuits (ceramic or quartz crystal oscillator).
Supply Voltage			5V±5%
Power dissipation	At high-speed operation		15mW (at f (X_{IN})=4MHz).
	At low-speed operation		0.3mW (at f (X_{CIN})=32kHz).
	At stop mode		1μA (at clock stop)
Input/Output characteristics	Input/Output voltage		5V (port P3, P4)
			12V (port P0, P1, P2)
	Output current		10mA (port P0, P1, P2: Middle voltage N-channel open drain output).
			−5~−10mA (port P3, P4: CMOS tri-state output)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS Silicon gate
Package	M50944E-XXXSP	One time programming type	64-pin shrink plastic molded DIP
	M50944ES	Window type	64-pin shrink ceramic DIP
	M50944E-XXXFP	One time programming type	64-pin shrink plastic molded QFP

Note 1 : The EPROM programming voltage is 21V (equivalent to the M5L27128).

PIN DESCRIPTION

Terminal	Mode	Name	Input/ Output	Functions
V_{CC} V_{SS}	Singl-chip /EPROM	Power supply		Power supply inputs 5V±5% to V_{CC} and 0V to V_{SS}.
CNV_{SS} /V_{PP}	Singl-chip	CNV_{SS} input		Connect to 0V.
	EPROM	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V_{CC} conditions. If more time is needed for the crystal oscillator to stabilize, this "L" condition should be meintained for the required time.
	EPROM	RESET input		Connect to V_{SS}.
X_{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation. If an external clock input is used, connect the clock input to the X_{IN} pin and open the X_{OUT} pin.
X_{OUT}		Clock output	Output	
ϕ	Single-chip /EPROM	Timing output	Output	This is the timing output pin.
X_{CIN}	Single-chip /EPROM	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function. To control generating frequency, an external ceramic or quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open. This clock can be used as a program controlled the system clock.
X_{OUT}	Single-chip /EPROM	Clock output for clock function	Output	
$P0_0$~$P0_7$	Singl-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-ch open drain.
	EPROM	Address input A_0~A_7	Input	P0 works as the lower 8 bit address input (A_0~A_7).
$P1_0$~$P1_7$	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as Port P0.
	EPROM	Address input A_8~A_{15}	Input	$P1_0$~$P1_5$ works as the higher 6-bit address inputs (A_8~A_{13}).
$P2_0$~$P2_7$	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as Port P0.
	EPROM	Data input/ output D_0~D_7	I/O	Port 2 works as an 8-bit data bus (D_0~D_7).
$P3_0$~$P3_7$	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port with CMOS output. The other functions are basically the same as port P0. $P3_0$, $P3_1$, $P3_2$ and $P3_3$ pins are in common with INT_2 INT_1, CNTR and T respectively. When serial I/O_1 is used, $P3_4$, $P3_5$, $P3_6$ and $P3_7$ work as S_{IN1}, S_{OUT1}, CLK1 and S_{RDY1} pin respectively.
	EPROM	Select mode	Input	$P3_5$, $P3_4$, $P3_3$ work as $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ inputs, respectively. Connect $P3_2$~$P3_0$ to 0V and $P3_7$ and $P3_6$ to V_{CC}.
$P4_0$~$P4_7$	Single-chip	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as Port P0. $P4_2$ and $P4_3$ pins are in common with $\overline{INT_3}$ and $\overline{INT_4}$ respectively. When serial I/O_2 is used, $P4_4$, $P4_5$, $P4_6$ and $P4_7$ work as S_{IN2}, S_{OUT2}, CLK_2 and $\overline{S_{RDY2}}$ pin respectively.
	EPROM	Input Port P4	Input	Connect to V_{SS}.
R_0~R_3	Single-chip	Input port R	Input	Port R is a 4-bit input port.
	EPROM			Connect to V_{SS}.
IN_0~IN_7	Single-chip	Analog input port IN	Input	Port IN is the analog input pin to the A-D converter. It also has a dual function and works as a normal input port.
	EPROM	Input port IN	Input	Connect to V_{SS}.
AV_{CC} (Note)	Single-chip	Voltage input for A-D		This is the power supply input pin for the A-D converter.
	EPROM	Voltage Input		Connect to V_{CC}.
V_{REF}	Single-chip	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.
	EPROM	Input	Input	Connect to V_{SS}.

Note : The AV_{SS} pin of M50944E-XXXFP is connected to V_{SS}.

EPROM MODE

The M50944E-XXXSP features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 and Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P3_3$~$P3_5$, and CNV_{SS} are used for the EPROM (equivalent to the M5L27128). When in this mode, the built-in EPROM can be written to or read from using these pins in the same way as with the M5L27128. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1 Pin function in EPROM programming mode

	M50944E-XXXSP/FP	M5L27128
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0$~$P1_5$	A_0~A_{13}
Data I/O	Port P2	D_0~D_7
$\overline{CE}$	$P3_5/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P3_6/\overline{OE}$	$\overline{OE}$
$\overline{PGM}$	$P3_7/\overline{PGM}$	$\overline{PGM}$

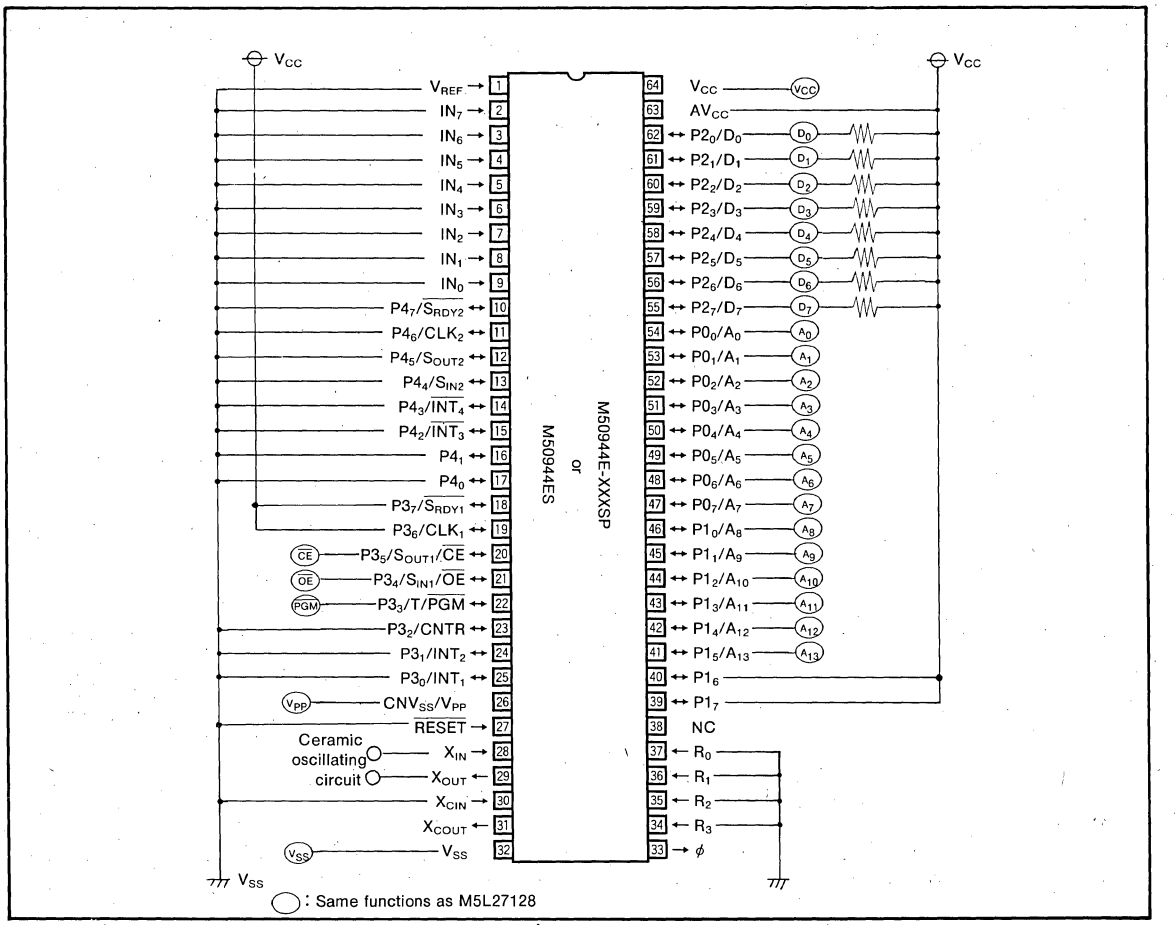


Fig.1 Pin connection in EPROM programming mode (M50944E-XXXSP, M50944ES)

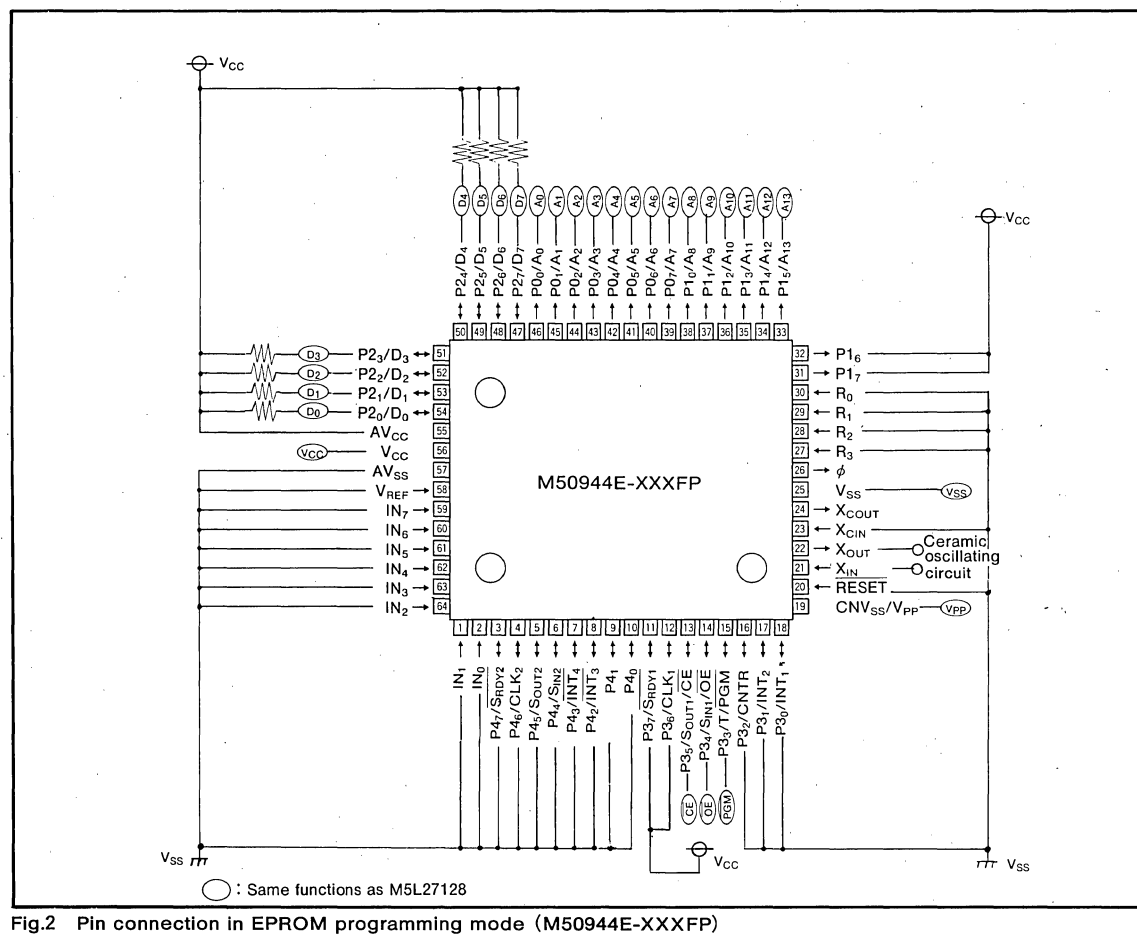


Fig.2 Pin connection in EPROM programming mode (M50944E-XXXFP)

EPROM READING, WRITING AND ERASING

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and the $\overline{PGM}$ pin to a "H" level. Input the address of the data (A_0~A_{13}) to be read and the data will be output to the I/O pins D_0~D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the EPROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0~A_{13}, and the data to be written is input to pins D_0~D_7. Set the $\overline{PGM}$ pin to a "L" level to begin writing.

Erasing

Data can only be erased on the M50944ES ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15W·s/cm^2.

NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage (21V) is used to write data, care should be taken when turning on the EPROM writer's power.

Table 2 I/O signal in each mode

Mode \ Pin	$\overline{CE}$(20)	$\overline{OE}$(21)	$\overline{PGM}$(22)	V_{PP}(26)	V_{CC}(1)	Data I/O (55~62)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse(V_{IH}→V_{IL})	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output Transistors are at "OFF" state.	−0.3~7	V
V_I	Input voltage CNV_{SS}		−0.3~13(Note1)	V
V_I	Input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$		−0.3~13	V
V_I	Input voltage R_0~R_3, X_{IN}, X_{CIN}, $\overline{RESET}$		−0.3~7	V
V_I	Input voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$, IN_0~IN_7, V_{REF}		−0.3~V_{CC}+0.3	V
V_O	Output voltage $P3_0$~$P3_7$,$P4_0$~$P4_7$, X_{COUT}, X_{OUT}, ϕ		−0.3~V_{CC}+0.3	V
V_O	Output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$		−0.3~13	V
P_d	Power Dissipation	T_a=25℃	1000(Note2)	mW
Topr	Operating Temperature		−10~70	℃
Tstg	Strage Temperature		−40~125	℃

Note 1. In EPROM programming mode, CNV_{SS} is 22.0V.
2. 600mW for QFP type.

RECOMMEND OPERATING CONDITIONS

(V_{CC}=5V±5%, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$, IN_0~IN_7,CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage R_0~R_3	0.4V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$	0.8V_{CC}		12	V
V_{IL}	"L" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$, IN_0~IN_7, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	"L" input voltage R_0~R_3	0		0.12V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}	0		0.16V_{CC}	V
$I_{OL(sum)}$	"L" sum output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$			60	mA
$I_{OH(sum)}$	"H" sum output current $P3_0$~$P3_7$, $P4_0$~$P4_7$			−30	mA
$I_{OL(sum)}$	"L" sum output current $P3_0$~$P3_7$, $P4_0$~$P4_7$			60	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$			20	mA
$I_{OH(peak)}$	"H" peak output current $P3_0$~$P3_7$, $P4_0$~$P4_7$			−10	mA
$I_{OL(peak)}$	"L" peak output current $P3_0$~$P3_7$, $P4_0$~$P4_7$			20	mA
$I_{OL(avg)}$	"L" average output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$			10	mA
$I_{OH(avg)}$	"H" average output current Port $P3_0$~$P3_7$, $P4_0$~$P4_7$			−5	mA
$I_{OL(avg)}$	"L" average output current Port $P3_0$~$P3_7$, $P4_0$~$P4_7$			10	mA
$f_{(X_{IN})}$	Clock oscillating frequency			4.3	MHz
$f_{(X_{CIN})}$	Clock oscillating frequency for clock function			500	kHz

Note 1. The maximum "H" input voltage for CNV_{SS} is +21V.
2. The duty cycle for these oscillation frequency is 50%.
3. When the low speed mode is used, the clock input oscillation frequency for the timer must satisfy the following expression :
$f(X_{CIN}) < f(X_{IN})/3$
4. The avarage output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms cycle.
5. $f_{(X_{IN})}$ must be less than 50kHz when the external clock is to be used.

ELECTRICAL CHARACTERISTICS (V_{CC}= 5 V± 5 %, V_{SS}= 0 V, T_a=25℃, f(X_{IN})= 4 MHz, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P3_0$~$P3_7$, $P4_0$~$P4_7$	I_{OH}=−5mA		3			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA		3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$	I_{OL}=10mA				2	V
V_{OL}	"L" output voltage ϕ	I_{OL}=2.5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis $P3_0/INT_1$, $P3_1/INT_2$, $P4_2/\overline{INT_3}$, $P4_3/\overline{INT_4}$	use as interrupt input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6/CLK_1$, $P4_6/CLK_2$	use as CLK input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}			0.1		0.5	V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$/CNTR	use as CNTR input		0.3		1	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_I=0V				−5	μA
I_{IL}	"L" input current IN_0~IN_7	V_I=0V				−5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}, R_0~R_3	V_I=0V				−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$	V_I=5V				5	μA
I_{IH}	"H" input current IN_0~IN_7	V_I=5V, not use as analog input				5	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}, R_0~R_3	V_I=5V				5	μA
I_{IH}	"H" input current V_{REF}	V_I=5V				5	mA
I_{CC}	Supply current	Open output ports, V_P=V_{CC}, Input port is V_{SS}, at normal operation.	X_{IN}=4MHz		3	6	mA
		Open output ports, V_P=V_{CC}, Input port is V_{SS}, at wait mode.	X_{IN}=4MHz		1		mA
		Open output ports, V_P=V_{CC}, Input port is V_{SS}, at normal operation, stop X_{IN} and X_{OUT}, X_{CIN}=32kHz.			60	200	mA
		Open output ports, V_P=V_{CC}, Input port is V_{SS}, at wait mode, stop X_{IN} and X_{OUT}, X_{CIN}=32kHz.			40		mA
		Stop all oscillation.	T_a=25℃, V_{CC}=5V		0.1	1	μA
			T_a=70℃, V_{CC}=5V		1	10	μA
I_{ACC}	Supply current for A-D	at A-D converting time			2	4	mA

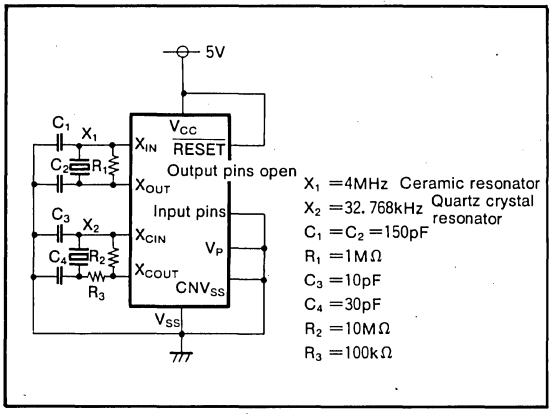


Fig.3 Test circuit for measuring supply current

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Absolute accuracy	V_{CC}=AV_{CC}=V_{REF}=5.12V			±3	LSB
R_{LADDER}	Ladder resistor value		1			kΩ
t_{CONV}	Conversion time	High-speed : ϕ=1MHz			72	μs
		Low-speed : ϕ=1MHz			288	μs
V_{REF}	Reference input voltage				V_{CC}	V
V_{IA}	Analog input voltage				V_{REF}	V

TIMING REQUIREMENTS

Single-chip mode (V_{CC}= 5 V± 5 %, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless other wise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	270			ns
$t_{su(RD-\phi)}$	Port R input setup time	270			ns
$t_{su(IND-\phi)}$	Port IN input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-RD)}$	Port R input hold time	20			ns
$t_{h(\phi-IND)}$	Port IN input hold time	20			ns
$t_{C(X_{IN})}$	External clock input cycle time (X_{IN})	230			ns
$t_{W(X_{IN})}$	External clock input pulse width (X_{IN})	75			ns
$t_{C(X_{CIN})}$	External clock input cycle time (X_{CIN})	2			ms
$t_{W(X_{CIN})}$	External clock input pulse width (X_{CIN})	1			ms
t_r	External clock rising edge time			25	ns
t_f	External clock falling edge time			25	ns

Memory expanding mode and eva-chip mode

(V_{CC}=5V± 5 %, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless otherwise noted)

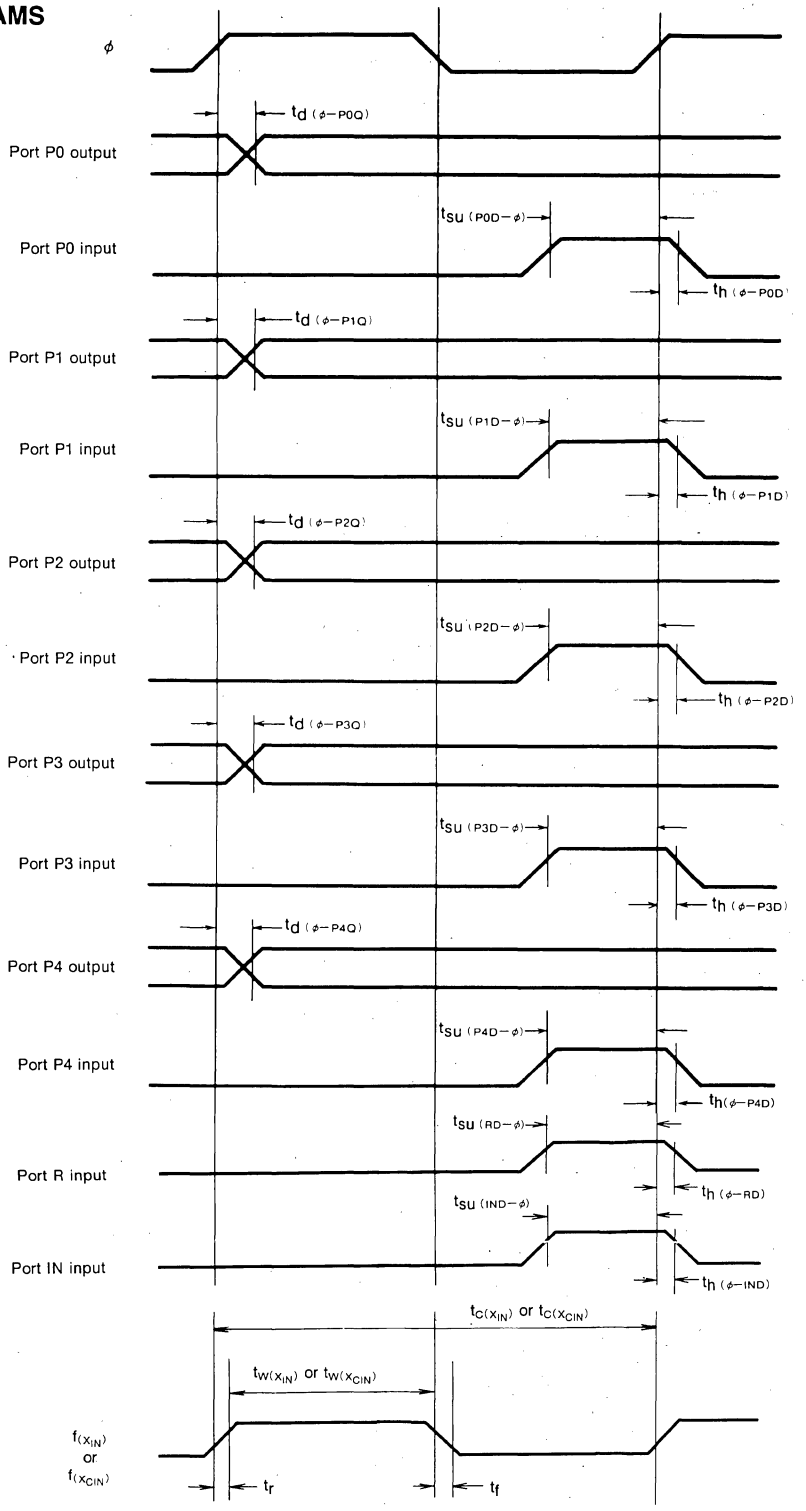
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

Microprocessor mode (V_{CC}=5V± 5 %, V_{SS}= 0 V, T_a=25℃, $f_{(X_{IN})}$= 4 MHz unless otherwise noted)

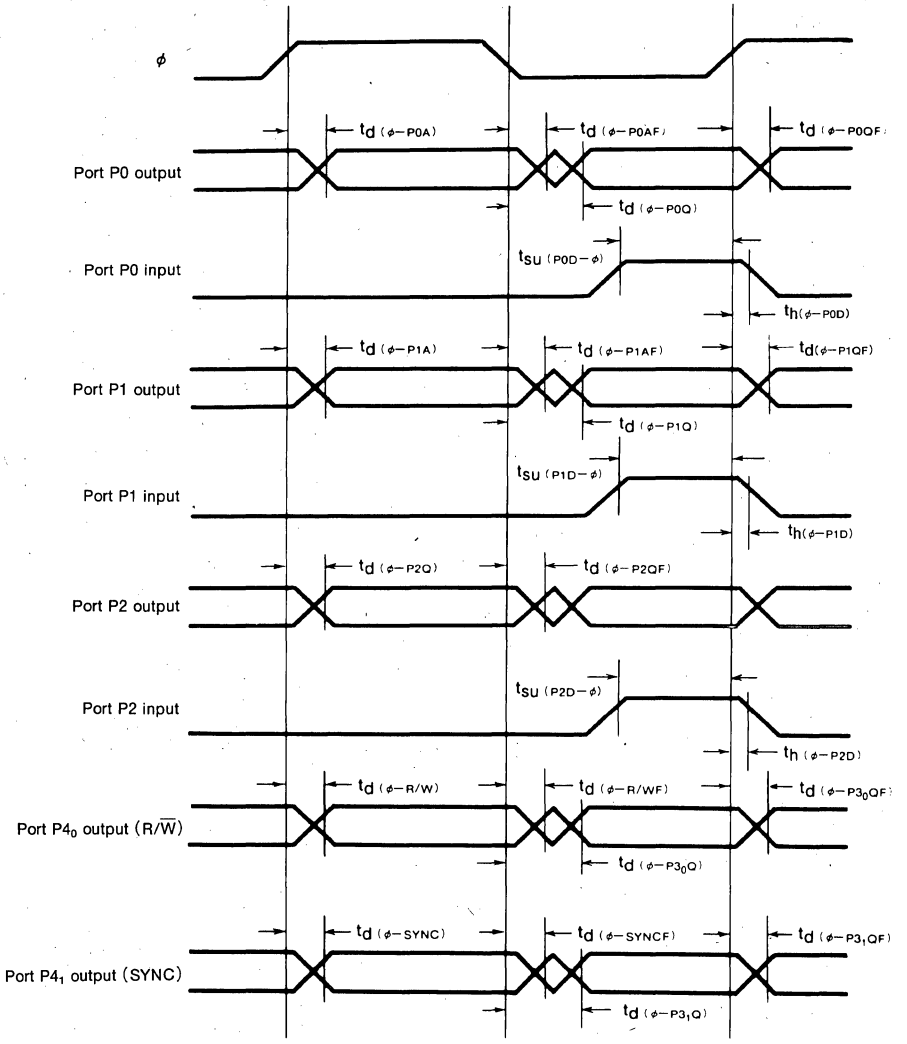
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

TIMING DIAGRAMS

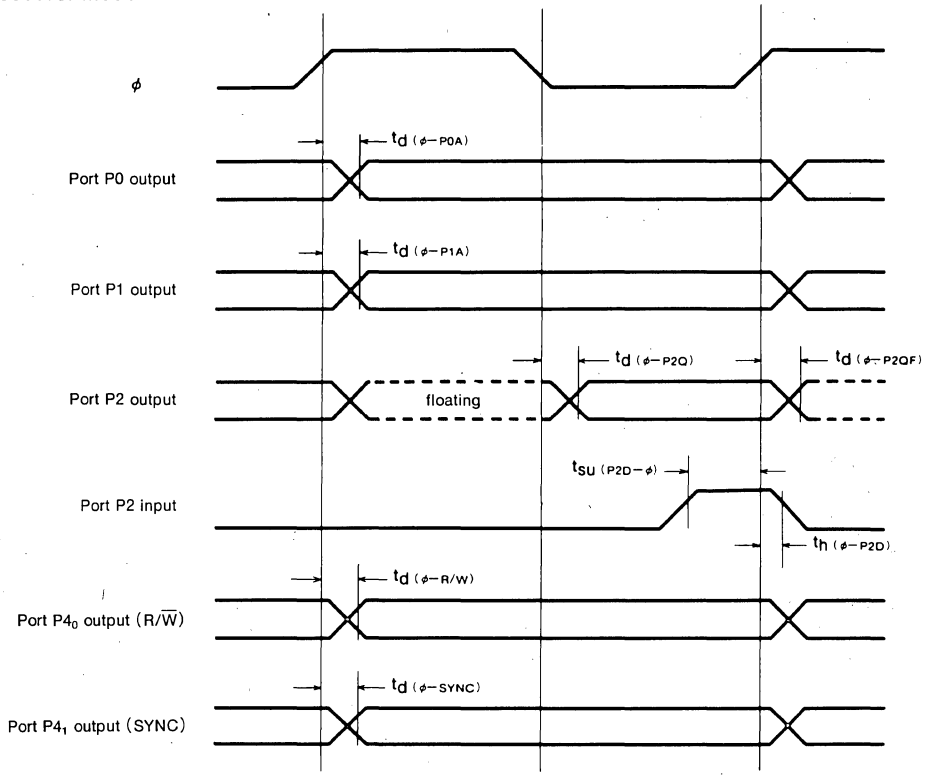
In single-chip mode



In memory expanding mode and eva-chip mode



In microprocessor mode



PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

M50957E-XXXSP
M50957ES

EPROM VERSION of M50957-XXXSP

DESCRIPTION

The M50957E-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. The features of this chip are similar to those of the M50957-XXXSP except that this chip has a 81920-bit (10240 words×8 bits) EPROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the EPROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose EPROM writers can be used for the built-in EPROM, this chip is suitable for small quantity production runs.

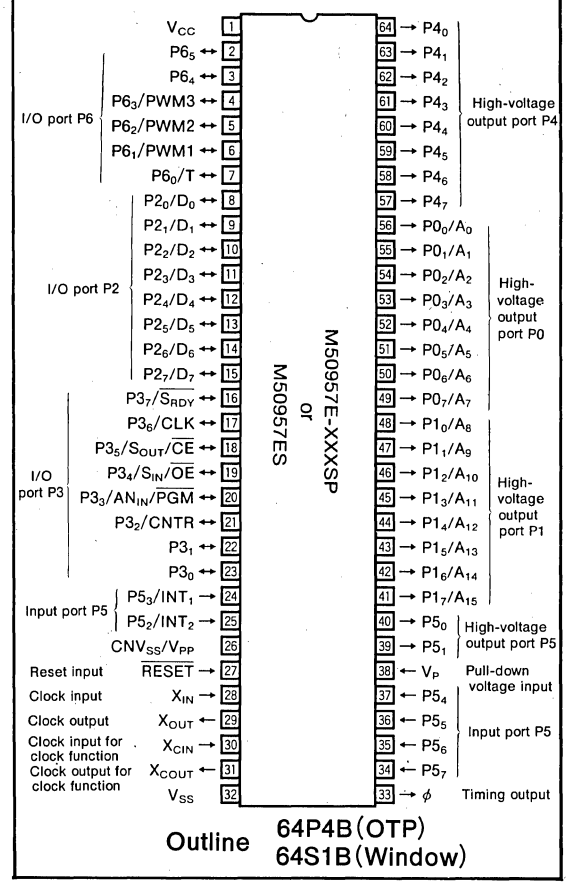
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size EPROM ..... 10240 bytes
  RAM ..... 256 bytes
- Instruction execution time
  ···1.9μs (minimum instructions at 4.2MHz frequency)
- Single power supply ..... 4.0~5.5V (at $f_{(X_{IN})}$=4.2MHz)
  3.5 ~ 5.5V (below $f_{(X_{IN})}$ = 1.0MHz)
- Power dissipation
  normal operation mode (at 4.2MHz frequency) 20mW
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer ..... 3 (2 when used as serial I/O)
- Programmable I/O (Ports P2, P3, P6) 22
- Input ports (Port $P5_2$~$P5_7$) 6
- High-voltage output ports
  (Port P0, P1, P4, $P5_0$, $P5_1$) 26
- Serial I/O (8-bit) 1
- PWM function ..... 14-bit×1
  6-bit×2
- Two clock generator circuits (One is for main clock, the other is for clock function)
- Generating function for clock input of EAROM
- Comparator 1
- EPROM (equivalent to the M5L27128)
  program voltage 21V

APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

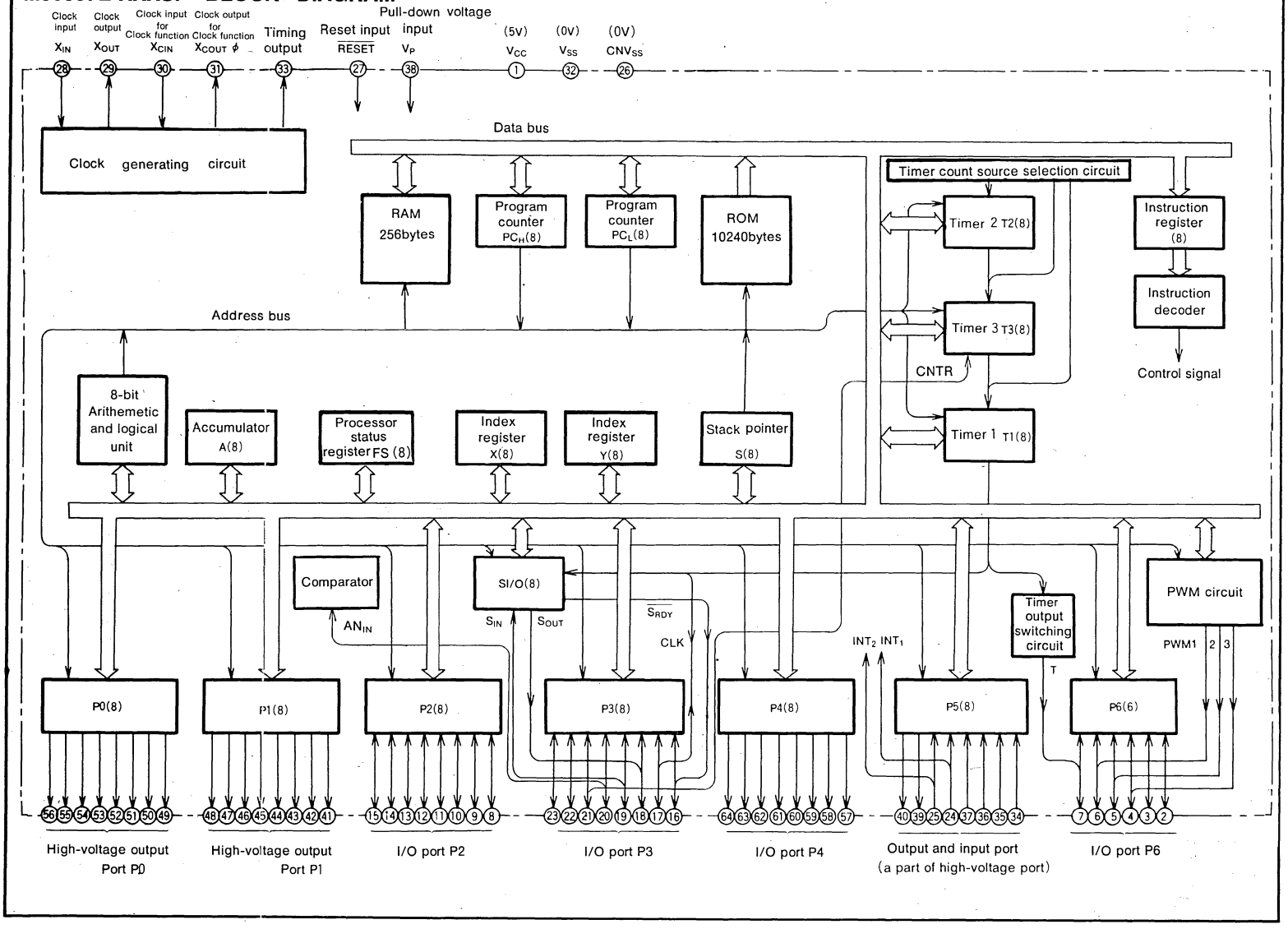
PIN CONFIGURATION (TOP VIEW)



Outline 64P4B (OTP)
64S1B (Window)

MITSUBISHI ELECTRIC

M50957E-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M50957E-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1.90μs (minimum instructions, at 4.2MHz frequency)
Clock frequency			4.2MHz
Memory size	EPROM		10240bytes (Note 1)
	RAM		256bytes
Input/Output ports	P0, P1, P4	Output	8-bit×3 (High voltage P-channel open drain; V_{CC}−38V)
	P2, P3	I/O	8-bit×2 (P3 can partially be used as among serial I/O, clock input for timer 3 and normal I/O.)
	$P5_0$, $P5_1$	Output	2-bit×1 (High voltage P-channel open drain; V_{CC}−38V)
	$P5_2$, $P5_3$	Input	2-bit×1 (Can be used as an input for either INT_2 or INT_1.)
	$P5_4$~P_7	Input	4-bit×1
	P6	I/O	6-bit×1 (Can be used as T_1 output or PWM output.)
Serial I/O			8-bit×1
Timers			8-bit timer×3 (×2, when used as serial I/O)
Subroutine nesting			96levels (max)
Interrupt			Two external interrupts, three internal timer interrupts (or timer×2, serial I/O×1)
Clock generating circuit			Two built-in circuits (externally connected ceramic or quartz crystal oscillator)
Supply voltage	at f(X_{IN})=4.2MHz		4.0~5.5V
	below f(X_{IN})=1.0MHz		3.5~5.5V
Power dissipation	at high-speed operation		20mW (clock frequency X_{IN}=4.2MHz)
	at low-speed operation		0.3mW (clock frequency X_{CIN}=32kHz)
	at stop mode		5μW (when clock is stopped)
Input/Output characteristics	Input/Output voltage		12V (Input/output P2, P3, $P5_2$~$P5_7$ except $P3_3$)
			V_{CC}−38V (P0, P1, P4, $P5_0$, $P5_1$)
			−0.3V~V_{CC}+0.3V (Input/output P6)
	Output current		10mA (P2, P3 : N-channel open drain)
			−18mA (P0, P1 : high-voltage P-channel open drain)
			−12mA (P4, $P5_0$, $P5_1$: high-voltage P-channel open drain)
			0.5~−0.5mA (P6 : CMOS tri-states)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M50957E-XXXSP	One time programming type	64-pin shrink plastic molded DIP
	M50957ES	Window type	64-pin shrink ceramic DIP

Note 1 : The EPROM programing voltage is 21V (equivalent to the M5L27128).

PIN DESCRIPTION

Terminal	Mode	Name	Input/ Output	Functions
V_{CC} V_{SS}	Singl-chip /EPROM	Power supply		Power supply inputs 4.0～5.5V at f(X_{IN}) = 4.2MHz and 3.5～5.5V below f(X_{IN}) = 1.0MHz to V_{CC}, and 0V to V_{SS}.
CNV_{SS} /V_{PP}	Singl-chip	CNV_{SS} input		Connect to 0V.
	EPROM	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V_{CC} conditions. If more is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
	EPROM	RESET input	Input	Connect to 0V.
X_{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation. If an external clock input is used, connect the clock input to the X_{IN} pin and open the X_{OUT} pin.
X_{OUT}		Clock output	Output	
ϕ	Single-chip /EPROM	Timing output	Output	For timing output.
X_{CIN}	Single-chip	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the function. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins. If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open. This clock can be used as a program controlled the system clock.
X_{COUT}		Clock output for clock function	Output	
	EPROM			X_{CIN} and X_{COUT} pins are left open.
$P0_0$～$P0_7$	Singl-chip	Output port P1	Output	Port P0 is an 8-bit output port. Output structure is high-voltage P-channel open drain. A pull-down transistor is built in between the V_P pin and this port. At reset, this port is set to a "L" level.
	EPROM	Address input A_0～A_7	Input	P0 works as the lower 8 bit address input (A_0～A_7).
$P1_0$～$P1_7$	Single-chip	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0.
	EPROM	Address input A_8～A_{13}	Input	$P1_0$～$P1_5$ works as the higher 5 bit address inputs (A_8～A_{13}). Connect $P1_6$, $P1_7$ to V_{CC}.
$P2_0$～$P2_7$	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
	EPROM	Data input/ Output D_0～D_7	I/O	Port P2 works as an 8-bit data bus (D_0～D_7) but needs 10kΩ pull-up resister.
$P3_0$～$P3_7$	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P2. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respecitively. $P3_3$ works as an analog input for comparator, and $P3_2$ works as a clock input for timer 3.
	EPROM	Select mode	Input	$P3_5$, $P3_4$, $P3_3$, work as $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ input, respectively. Connect $P3_2$～$P3_0$ to 0V and $P3_7$ and $P3_6$ to 5V.
$P4_0$～$P4_7$	Single-chip	Output port P4	Output	Port P4 is an 8-bit output port which has the same function as Port P0.
	EPROM	Output port P4	Output	Connect to 0V.

PIN DESCRIPTION

Terminal	Mode	Name	Input/ Output	Functions
$P5_0$, $P5_1$	Single-chip	Output port P5	Output	Bit 0 and 1 of port P5 are 2-bit output port and has basically the same functions as port P0.
	EPROM	Output port P5	Output	Connect to 0V.
$P5_2/INT_2$ $P5_3/INT_1$	Single-chip	Input port P5	Input	Bit 2 and 3 of port P5 are 2-bit input port and are in common with interrupt inputs.
$P5_4 \sim P5_7$			Input	Bit 4~7 of port P5 are 4-bit input port.
	EPROM	Input port P5	Input	Connect to 0V.
$P6_0 \sim P6_7$	Single-chip	I/O port P6	I/O	Port P6 is a 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. The output structure is CMOS tri-state output. $P6_0$, $P6_1$, $P6_2$, $P6_3$ can be programmed to function as timer output pin (T), PWM output pins (PWM1, PWM2, and PWM3), respectively.
	EPROM	Output port	Output	Connect to 0V.

EPROM MODE

The M50957E-XXXSP features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 gives the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P3_3 \sim P3_5$, and CNV_{SS} are used for the EPROM (equivalent to the M5L27128). When in this mode, the built-in EPROM can be written to or read from using these pins in the same way as with the M5L27128. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1 Pin function in EPROM programming mode

	M50957E-XXXSP	M5L27128
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0 \sim P1_5$	$A_0 \sim A_{13}$
Data I/O	Port P2	$D_0 \sim D_7$
$\overline{CE}$	$P3_5/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P3_4/\overline{OE}$	$\overline{OE}$
$\overline{PGM}$	$P3_3/\overline{PGM}$	$\overline{PGM}$

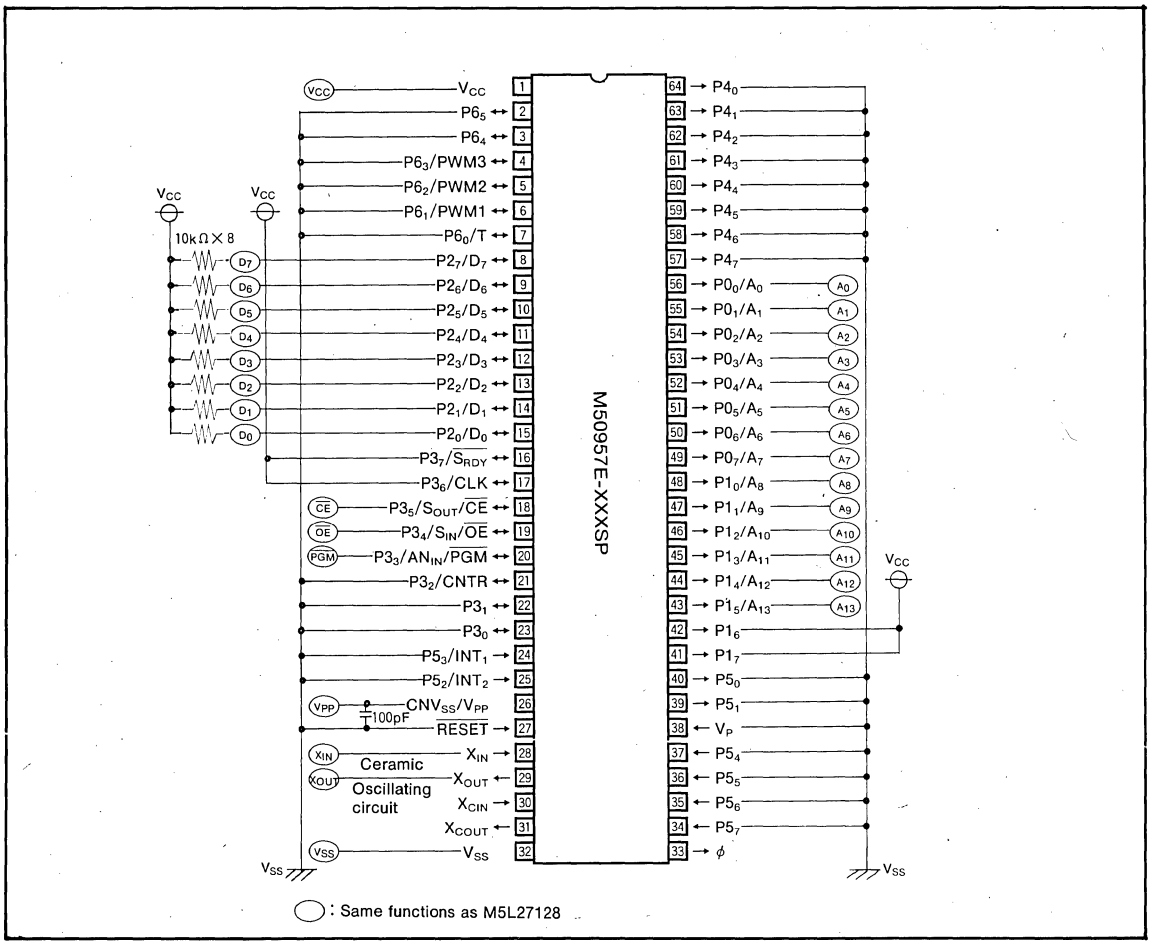


Fig.1 Pin connection in EPROM programming mode

EPROM READING, WRITING AND ERASING

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and the $\overline{PGM}$ pin to a "H" level. Input the address of the data (A_0~A_{13}) to be read and the data will be output to the I/O pins D_0~D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the EPROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0~A_{13}, and the data to be written is input to pins D_0~D_7. Set the $\overline{PGM}$ pin to a "L" level to begin writing.

Erasing

Data can only be erased on the M50957ES ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15W•s/cm^2.

NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage (21V) is used to write data, care should be taken when turning on the EPROM writer's power.

Table 2 I/O signal in each mode

Mode \ Pin	$\overline{CE}$(18)	$\overline{OE}$(19)	$\overline{PGM}$(20)	V_{PP}(26)	V_{CC}(1)	Data I/O (8~15)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse(V_{IH}→V_{IL})	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors cut-off.	−0.3～7	V
V_P	Pull-down input voltage		V_{CC}−40～V_{CC}+0.3	V
V_I	Input voltage, $P2_0$～$P2_7$, $P3_0$～$P3_2$, $P3_4$～$P3_7$, $P5_2/INT_2$, $P5_3/INT_1$		−0.3～13	V
V_I	Input voltage, CNV_{SS}		−0.3～22	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, X_{CIN}		−0.3～7	V
V_I	Input voltage, $P6_0$～$P6_5$, $P3_3$		−0.3～V_{CC}+0.3	V
V_I	Input voltage, $P5_4$～$P5_7$		−0.3～13	V
V_O	Output voltage, $P2_0$～$P2_7$, $P3_0$～$P3_2$, $P3_4$～$P3_7$		−0.3～13	V
V_O	Output voltage, $P6_0$～$P6_5$, X_{OUT}, X_{COUT}, ϕ, $P3_3$		−0.3～V_{CC}+0.3	V
V_O	Output voltage, $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P4_0$～$P4_7$, $P5_0$, $P5_1$		V_{CC}−40～V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
T_{opr}	Operating temperature		−10～70	℃
Tstg	Storage temperature		−40～125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=−10～70℃, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Nom.	Limits Max.	Unit
V_{CC}	Supply voltage	$f_{(X_{IN})}$=4.2MHz	4	5	5.5	V
		$f_{(X_{IN})}$=less than1MHz(Note 6)	3.5	5	5.5	V
V_P	Pull-down supply voltage		V_{CC}−38		V_{CC}	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P2_0$～$P2_7$, $P3_0$～$P3_7$, CNV_{SS}(Note 1) $P5_2/INT_2$, $P5_3/INT_1$, $P6_0$～$P6_5$		0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P5_4$～$P5_7$		0.4V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P2_0$～$P2_7$, $P3_0$～$P3_7$, CNV_{SS} $P5_2/INT_2$, $P5_3/INT_1$, $P6_0$～$P6_5$		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}		0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P5_4$～$P5_7$		0		0.12V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$～$P0_7$, $P1_0$～$P1_7$, $P4_0$～$P4_7$ $P5_0$, $P5_1$				−120	mA
$I_{OH(sum)}$	"H" sum output current $P6_0$～$P6_5$				−5	mA
$I_{OL(sum)}$	"L" sum output current $P2_0$～$P2_7$, $P3_0$～$P3_7$				50	mA
$I_{OL(sum)}$	"L" sum output current $P6_0$～$P6_5$				5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$～$P0_4$				−40	mA
$I_{OH(peak)}$	"H" peak output current $P0_5$～$P0_7$, $P1_0$～$P1_7$				−30	mA
$I_{OH(peak)}$	"H" peak output current $P4_0$～$P4_7$, $P5_0$, $P5_1$				−24	mA
$I_{OH(peak)}$	"H" peak output current $P6_0$～$P6_5$				−3	mA
$I_{OL(peak)}$	"L" peak output current $P2_0$～$P2_7$, $P3_0$～$P3_7$				15	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$～$P6_5$				3	mA
$I_{OH(avg)}$	"H" average output current $P0_0$～$P0_7$, $P1_0$～$P1_7$				−18	mA
$I_{OH(avg)}$	"H" average output current $P4_0$～$P4_7$, $P5_0$, $P5_1$				−12	mA
$I_{OH(avg)}$	"H" average output current $P6_0$～$P6_5$				−1.5	mA
$I_{OL(avg)}$	"L" average output current $P2_0$～$P2_7$, $P3_0$～$P3_7$, $P6_0$～$P6_5$				10	mA
$I_{OL(avg)}$	"L" average output current $P6_0$～$P6_5$				1.5	mA
$f(P3_2/CNTR)$	Timer 3 counter clock input oscillation frequency (Note 2)	$f_{(X_{IN})}$=4.2MHz			400	kHz
		$f_{(X_{IN})}$=1MHz			100	kHz
$f_{(X_{IN})}$	Clock input oscillating frequency (Note 2, 3, 5)				4.2	MHz
$f_{(X_{CIN})}$	Clock oscillating frequency for clock function				500	kHz

Note 1 : High-level input voltage of up to +12V may be applied to permissible for ports $P2_0$～$P2_2$, $P3_0$～$P3_2$, $P3_4$～$P3_7$, $P5_2$ and $P5_3$, and +21V for port CNV_{SS}.
2 : Oscillation frequency is at 50% duty cycle.
3 : When used in the low-speed mode, the timer clock input frequency should be $f_{(XIN)} < f_{(XIN)}/3$.
4 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are in period of 100ms.
5 : When external clock input is used, the timer clock input frequency should be $f_{(XCIN)} \leqq 50kHz$.
6 : 4.0～5.5V at comparator mode.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25℃, $f_{(X_{IN})}$ = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P6_0$~$P6_5$	I_{OH}=−0.5mA	V_{CC}−0.4			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA	V_{CC}−2			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$	I_{OH}=−18mA	V_{CC}−2			V
V_{OH}	"H" output voltage $P4_0$~$P4_7$, $P5_0$, $P5_1$	I_{OH}=−12mA	V_{CC}−2			V
V_{OL}	"L" output voltage $P2_0$~$P2_7$, $P3_0$~$P3_7$	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage $P6_0$~$P6_5$	I_{OL}=0.5mA			0.4	V
V_{OL}	"L" output voltage ϕ	I_{OL}=2.5mA			2	V
V_{T+}−V_{T-}	Hysteresis $P5_2/INT_2$, $P5_3/INT_1$		0.3		1	V
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$			0.5	0.7	V
V_{T+}−V_{T-}	Hysteresis $P3_6$	When used as CLK input	0.3		1	V
I_{IL}	"L" input current $P2_0$~$P2_7$, $P3_0$~$P3_7$	V_I=0V			−5	μA
I_{IL}	"L" input current $P6_0$~$P6_5$	V_I=0V			−5	μA
I_{IL}	"L" input current $P5_4$~$P5_7$	V_I=0V			−5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}	V_I=0V			−5	μA
I_{IL}	"L" input current $P5_2/INT_2$, $P5_3/INT_1$	V_I=0V			−5	μA
I_{IH}	"H" input current $P2_0$~$P2_7$, $P3_0$~$P3_7$	V_I=5V			5	μA
	"H" input current $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P3_4$~$P3_7$	V_I=12V			12	μA
I_{IH}	"H" input current $P6_0$~$P6_5$	V_I=5V			5	μA
I_{IH}	"H" input current $P5_4$~$P5_7$	V_I=5V			5	μA
		V_I=12V			12	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}	V_I=5V			5	μA
I_{IH}	"H" input current $P5_2/INT_2$, $P5_3/INT_1$	V_I=5V			5	μA
		V_I=12V			12	μA
I_{LOAD}	Load current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$	V_P=V_{CC}−36V, V_{OL}=V_{CC}	150	500	1000	μA
I_{LEAK}	Leakage current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$	V_P=V_{CC}−38V, V_{OL}=V_{CC}−38V			30	μA
V_{RAM}	RAM retention voltage	at clock stop	2		5.5	V
I_{CC}	Supply current	Output pins open (output OFF) V_P=V_{CC}, V_P=V_{SS} Input and I/O pins all at V_{SS} X_{IN}=4MHz (system operation)		4	8	mA
		ditto (at comparator operating)		5	10	mA
		ditto (at wait mode)		1		mA
		X_{IN}−X_{OUT} stop X_{CIN}=32kHz (at system operation) all other conditions same as above.		60	200	μA
		ditto (at wait mode)		40		μA
		Oscillation all stopped. (at STOP mode) T_a=25℃			1	μA
		Oscillation all stopped. (at STOP mode) T_a=70℃			10	μA

COMPARATOR CHARACTERISTICS (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25°C, $f_{(X_{IN})}$ = 4MHz)

Parameter	Test conditions	Limits			Unit
		Min.	Typ.	Max.	
Resolution				$(1/16)V_{CC}$	V
Internal analog voltage inaccuracy				$\pm(1/16)V_{CC}$	V
Analog input voltage				V_{CC}	V

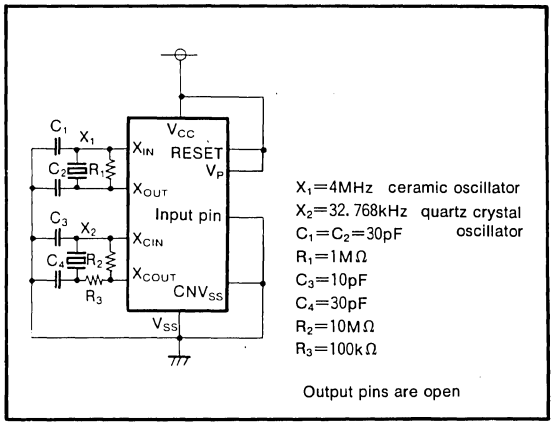


Fig.2 Supply current test circuit

M50963E-XXXSP/FP
M50963ES/EFS

EPROM VERSION of M50963-XXXSP/FP

DESCRIPTION

The M50963E-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. The features of this chip are similar to those of the M50963-XXXSP except that this chip has a 81920-bit (10240 words×8 bits) EPROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the EPROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose EPROM writers can be used for the built-in EPROM, this chip is suitable for small quantity production runs.

The M50963ES and the M50963EFS are the window type.

The differences between the M50963E-XXXSP and the M50963EFS are the package outline and the power dissipation ability(absolute maximum ratings).

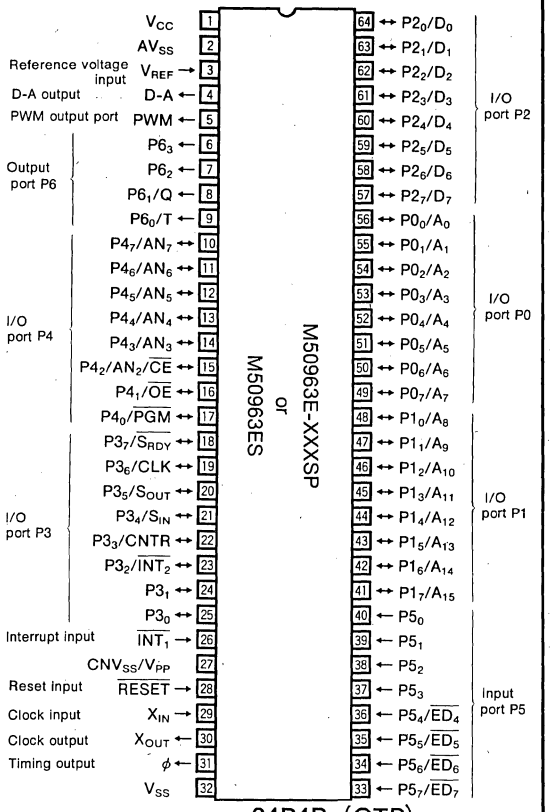
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 10240 bytes
  RAM ..... 160 bytes
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply ..... 5V±5%
- Power dissipation
  normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting ..... 80 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer 4
- Programmable I/O ports (Ports P0, P1, P2, P3, P4) 40
- Input ports (Port P5) 8
- Output ports (Port P6) 4
- Serial I/O (8-bit) 1
- A-D converter ..... 8-bit successive approximation
- D-A converter
- 8-bit PWM function
- Watchdog timer
- EPROM (equivalent to the M5L27128)
  program voltage 21V

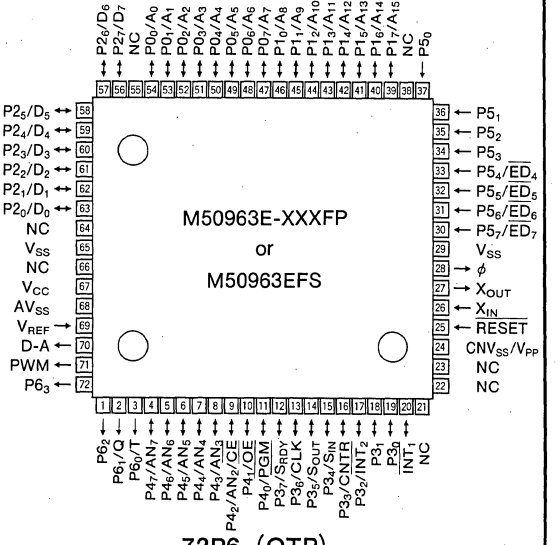
APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B (OTP)
64S1B (Window)

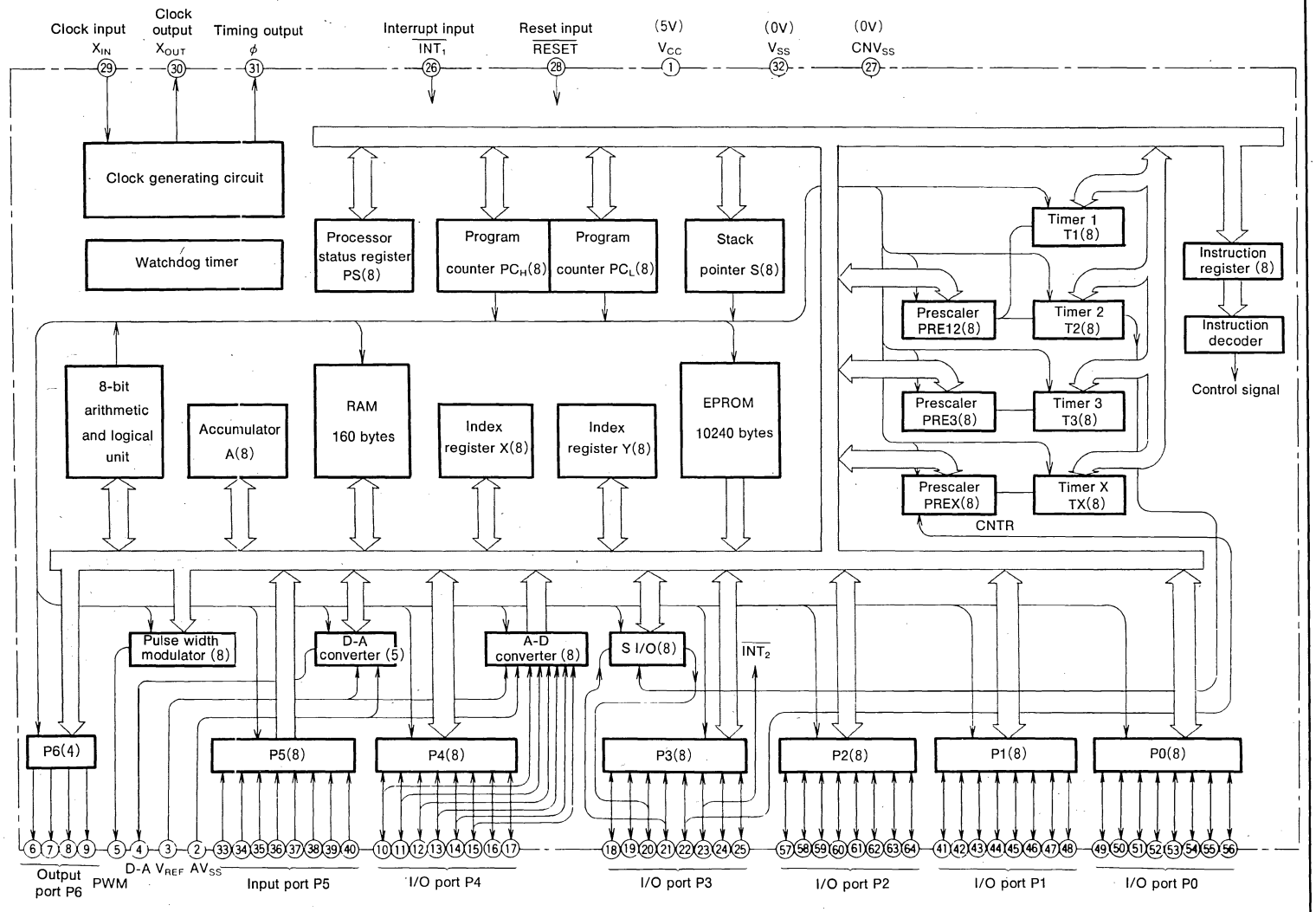


Outline 72P6 (OTP)
72S6 (Window)

NC : No connection

MITSUBISHI ELECTRIC

M50963E-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M50963E-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory Size	EPROM		10240bytes (Note 1)
	RAM		160bytes
Input/Output ports	$\overline{INT_1}$	Input	1-bit×1
	P0, P1, P2, P3, P4	I/O	8-bit×5 (a part of P3 is common with serial I/O, timer I/O, and interrupt input)
	P5	Input	8-bit×1
	P6	Output	4-bit×1 (a part of P6 is in common with external trigger output pin)
Serial I/O			8-bit×1
Timers			8-bit prescaler×3+8-bit timer×4
A-D conversion			8-bit×1 (6 channels)
D-A conversion			5-bit×1
Pulse width modulator			8-bit×1
Watchdog timer			15-bit×1
Subroutine nesting			80 levels (max)
Interrupts			Two external interrupts, three internal timer interrupts
Clock generating circuit			built-in (ceramic or quartz crystal oscillator)
Supply voltage			5V±5%
Power dissipation	at high-speed operation		15mW (at 4MHz frequency)
Input/Output characteristics	Input/Output voltage		12V (Ports P0, P1, P3, P4, P5, P6, $\overline{INT_1}$)
	Output current		5mA (Ports P0, P1, P2, P3, P4)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package	M50963E-XXXSP	One time programming type	64-pin shrink plastic molded DIP
	M50963ES	Window type	64-pin shrink ceramic DIP
	M50963E-XXXFP	One time programming type	72-pin plastic molded QFP
	M50963EFS	Window type	72-pin ceramic QFP

Note 1 : The EPROM programing voltage is 21V (equivalent to the M5L27128).

PIN DESCRIPTION

Terminal	Mode	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Singl-chip /EPROM	Power supply		Supply 5V±5% to V_{CC} and 0V to V_{SS}.
CNV_{SS}	Singl-chip	CNV_{SS} input	Input	Connect to 0V.
	EPROM	V_{PP} input		Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V_{CC} conditions. If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
	EPROM	RESET input		Connect to V_{SS}.
X_{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation. If an external clock input is used, connect the clock input to the X_{IN} pin and open the X_{OUT} pin.
X_{OUT}		Clock output	Output	
ϕ	Single-chip /EPROM	Timing output	Output	For timing output.
$\overline{INT_1}$	Single-chip	Interrupt input	Input	Interrupt input INT_1.
	EPROM	Interrupt input	Input	Connect to 0V.
$P0_0$~$P0_7$	Singl-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction registers which can program each bit as input or output. It is set to input mode at reset. The output format is N-ch open drain.
	EPROM	Address input A_0~A_7	Input	P0 works as the lower 8 bit address input (A_0~A_7).
$P1_0$~$P1_7$	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port which has the same function as Port P0.
	EPROM	Address input A_8~A_{13}	Input	$P1_0$~$P1_4$ works as the higher 5 bit address inputs (A_8~A_{13}). Connect $P1_5$~$P1_7$ to V_{CC}.
$P2_0$~$P2_7$	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port which has the same function as Port P0. The output format is CMOS.
	EPROM	Data input/ output D_0~D_7	I/O	Port 2 works as an 8 bit data bus (D_0~D_7).
$P3_0$~$P3_7$	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions Port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest interrupt pin ($\overline{INT_2}$), respectively. The output format is N-ch open drain.
	EPROM	Input Port P3	Input	Connect to 0V.
$P4_0$~$P4_7$	Single-chip	I/O port P4	I/O	Port P4 is an 8-bit I/O port which has the same function as Port P0. Ports $P4_7$~$P4_2$ are common with Analog inputs AN_7~AN_2. The output format is N-ch open drain.
	EPROM	Select mode	Input	$P4_2$, $P4_1$, $P4_0$ work as $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ inputs, respectively. Connect $P4_5$~$P4_7$ to 0V and $P4_4$ and $P4_3$ to V_{CC}.
$P5_0$~$P5_7$	Single-chip	Input port	Input	Port P5 is an 8-bit input port. Ports $P5_7$~$P5_4$ have edge sence functions.
	EPROM	Input port	Input	Connect to 0V.

PIN DESCRIPTION

Terminal	Mode	Name	Input/ Output	Functions
$P6_0$~$P6_3$	Single-chip	Output port	Output	Port P6 is an 4-bit output port. At external trigger output mode, $P6_0$ and $P6_1$ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively. The output structure is N-channel open drain.
	EPROM	Output port	Output	Connect to 0V.
AV_{SS}	Single-chip	Analog voltage input	Input	GND pin for the A-D and D-A converters.
	EPROM	Analog voltage input	Input	Connect to 0V.
V_{REF}	Single-chip	Reference voltage input	Input	Referrence input for A-D and D-A converters.
	EPROM	Reference voltage input	Input	Connect to 0V.
D-A	Single-chip	D-A output	Output	D-A converter output pin
	EPROM	D-A output	Output	Connect to 0V.
PWM	Single-chip	PWM output	Output	Pulse width modulation output pin (N-ch open drain format).
	EPROM	PWM output	Output	Connect to 0V.

EPROM MODE

The M50963E-XXXSP features an EPROM mode in addition to its normal modes. When the $\overline{\text{RESET}}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 and Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P4_0$~$P4_2$, and CNV_{SS} are used for the EPROM (equivalent to the M5L27128). When in this mode, the built-in EPROM can be written to or read from using these pins in the same way as with the M5L27128. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1 Pin function in EPROM programming mode

	M50963E-XXXSP/FP	M5L27128
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0$~$P1_5$	A_0~A_{13}
Data I/O	Port P2	D_0~D_7
$\overline{CE}$	$P4_2/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P4_1/\overline{OE}$	$\overline{OE}$
$\overline{PGM}$	$P4_0/\overline{PGM}$	$\overline{PGM}$

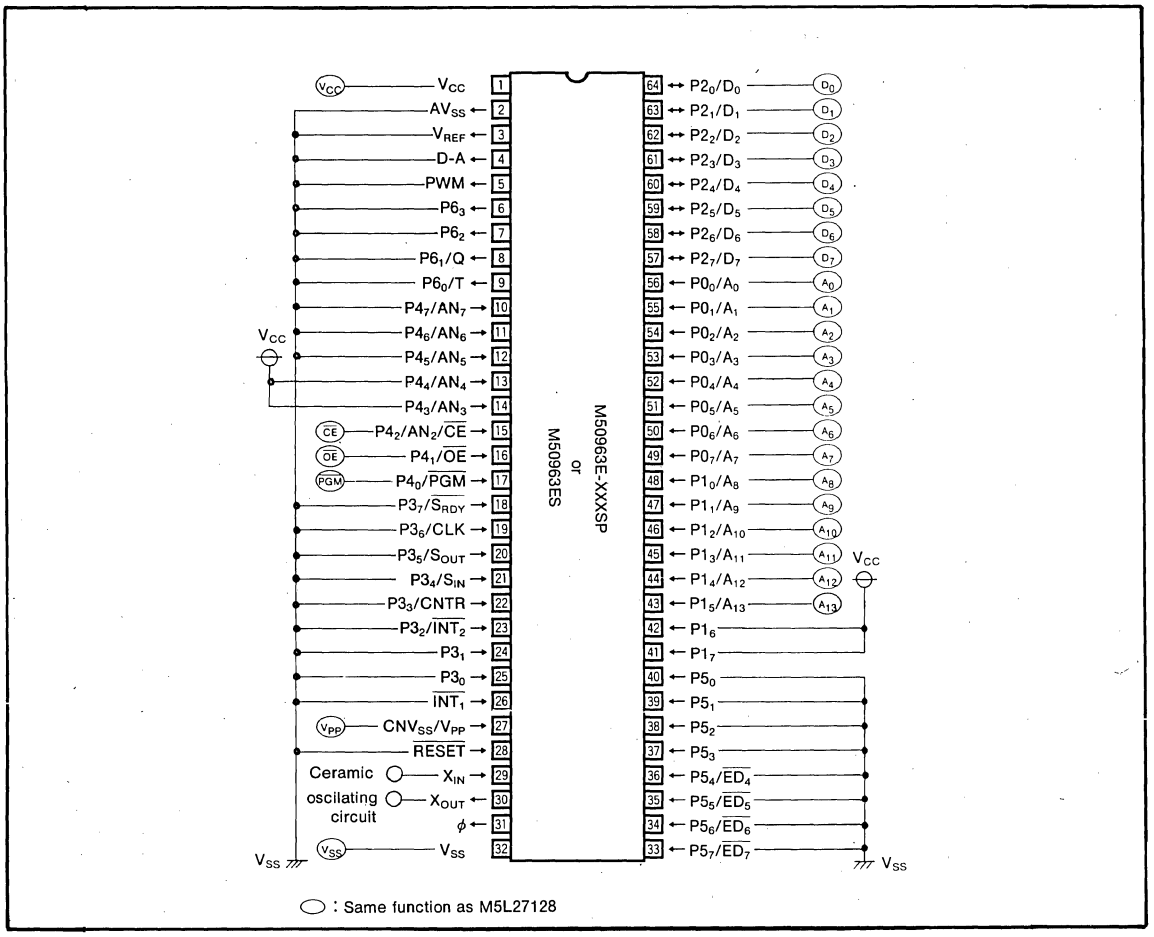


Fig. 1 Pin connection in EPROM programming mode (M50963E-XXXSP, M50963ES)

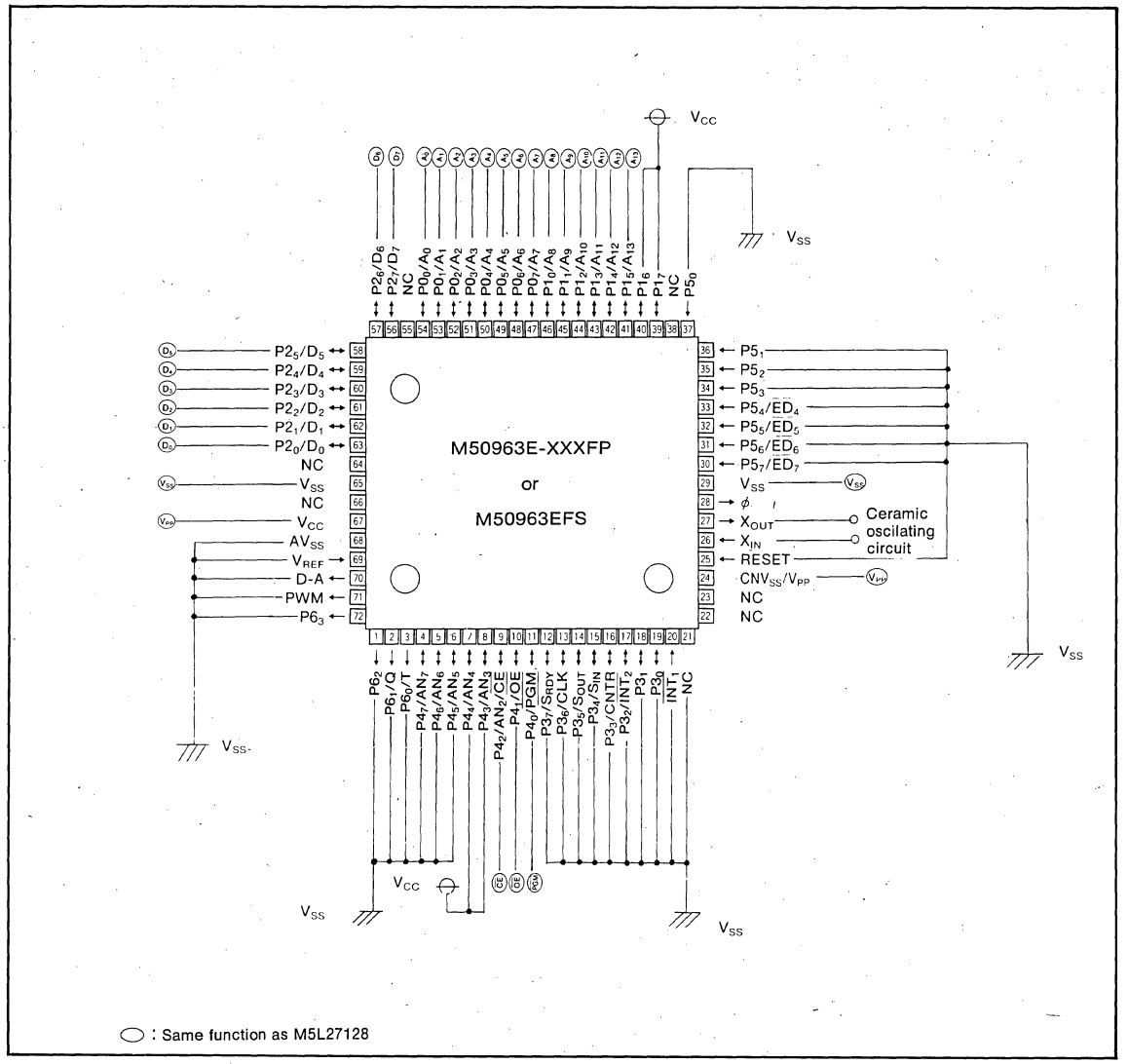


Fig. 2 Pin connection in EPROM programing mode (M50963E-XXXFP, M50963EFS)

EPROM READING, WRITING AND ERASING

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and the $\overline{PGM}$ pin to a "H" level. Input the address of the data (A_0~A_{13}) to be read and the data will be output to the I/O pins D_0~D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the EPROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0~A_{12}, and the data to be written is input to pins D_0~D_7. Set the $\overline{PGM}$ pin to a "L" level to begin writing.

Notes on Writing

When using an EPROM writer, the address range should be between 1800_{16} and $3FFF_{16}$. When data is written between addresses 0000_{16} and $3FFF_{16}$, fill addresses 0000_{16} to $17FF_{16}$ with 00_{16}.

Erasing

Data can only be erased on the M50963ES and the M50963EFS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15W•s/cm^2.

NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage (21V) is used to write data, care should be taken when turning on the EPROM writer's power.

Table 2 I/O signal in each mode

Mode \ Pin	$\overline{CE}$(15)	$\overline{OE}$(16)	$\overline{PGM}$(17)	V_{PP}(27)	V_{CC}(1)	Data I/O (57~64)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse(V_{IH}→V_{IL})	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} With the output transistor cut-off	−0.3∼7	V
V_I	Input voltage X_{IN}		−0.3∼7	V
V_I	Input voltage $P2_0$∼$P2_7$, $P4_4$∼$P4_7$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, $P5_0$∼$P5_7$, $\overline{INT_1}$		−0.3∼13	V
V_I	Input voltage CNV_{SS}, $\overline{RESET}$		−0.3∼13 (Note 1)	V
V_O	Output voltage $P2_0$∼$P2_7$, $P4_4$∼$P4_7$, X_{OUT}, ϕ, D-A		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_3$, $P6_0$∼$P6_3$, PWM		−0.3∼13	V
P_d	Power dissipation	T_a=25℃	1000 (Note 2)	mW
T_{opr}	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : In EPROM programming mode, CNV_{SS} is 22.0V
2 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}, $P6_0$	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, CNV_{SS}, $P6_0$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$ (Note 4)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$∼$P6_3$ (Note 4)			15	mA
$I_{OL(peak)}$	"L" peak output current PWM (Note 4)			5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$ (Note 3)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0$∼$P6_3$ (Note 3)			7	mA
$I_{OL(avg)}$	"L" average output current PWM (Note 3)			2.5	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$∼$P2_7$ (Note 4)			−10	mA
$I_{OH(avg)}$	"H" average output current $P2_0$∼$P2_7$ (Note 3)			−5	mA
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

Note 3 : The average output currents $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
4 : Do not allow the combined low- level output current of ports P0, P1, P2, P3, P4, P6, and PWM to exceed 80mA.
Do not allow the combined high- level output current of port P2 to exceed 50mA.
5 : "H" input voltage of ports' P0, P1, P3, $P4_0$∼$P4_3$, P5 and $\overline{INT_1}$ is available up to +12V.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P2_0$~$P2_7$	I_{OH}=−10mA		3			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA		3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_3$	I_{OL}=10mA				2	V
V_{OL}	"L" output voltage ϕ, PWM	I_{OL}=5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input		0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$	When used as $\overline{INT_2}$ input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_3$	When used as CNTR input		0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $P6_0$	When used as T input		0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}			0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=0V				−5	μA
I_{IL}	"L" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I=0V				−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=12V				12	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, $P2_0$~$P2_7$, $P4_4$~$P4_7$	V_I=5V				5	μA
V_{RAM}	RAM retention voltage	At clock stop		2			V
I_{CC}	Supply current	ϕ, X_{OUT}, and D-A pins opened, other pins at V_{SS}, and A-D converter in the finished condition.	$f_{(X_{IN})}$=4MHz Square wave		3	6	mA
			At clock stop T_a=25℃			1	μA
			At clock stop T_a=75℃			10	μA

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance value	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference input voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF}=V_{CC}			5	Bits
—	Error in full scale range	V_{REF}=V_{CC}			±1	%
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
R_O	Output resistance	V_{REF}=V_{CC}			3	kΩ
V_{REF}	Reference voltage		4		V_{CC}	V

TIMING REQUIREMENTS

Single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		270			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		20			ns
t_c	External clock input cycle time		250			ns
t_w	External clock input pulse width		75			ns
t_r	External clock rising edge time				25	ns
t_f	External clock falling edge time				25	ns

Eva-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

Memory expanding mode and microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=25℃, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		30			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=25°C, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 3			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 4			230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig. 3			230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				230	ns

Eva-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=25°C, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 3			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 4			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig. 3			250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns

Memory expanding mode and microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=25°C, $f_{(X_{IN})}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 3			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig. 4			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig. 3			250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

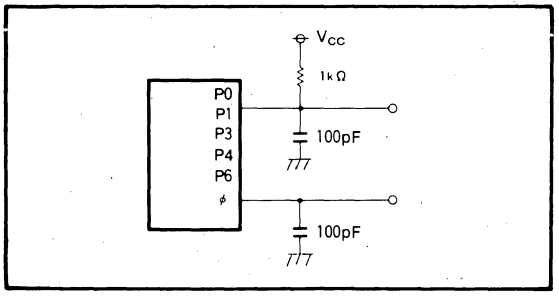


Fig. 3 Ports P0, P1, P3, P4, and P6 test circuit

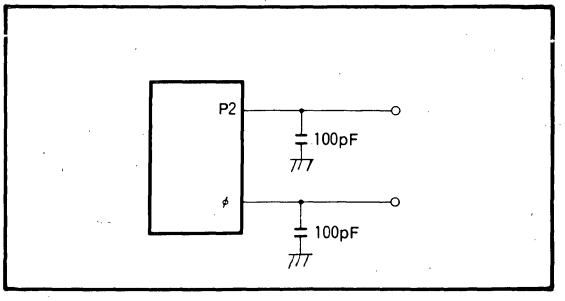
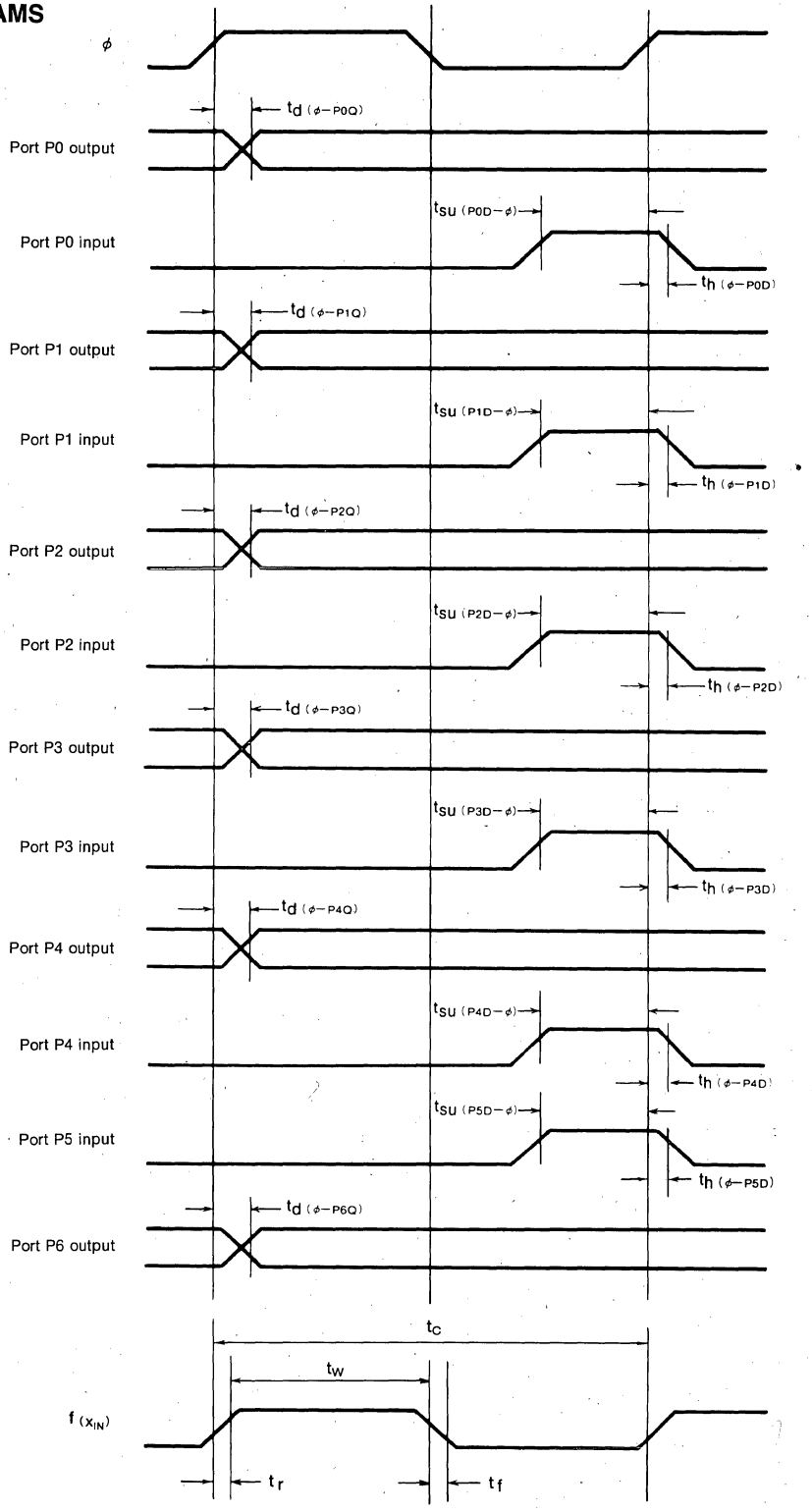


Fig. 4 Port P2 test circuit

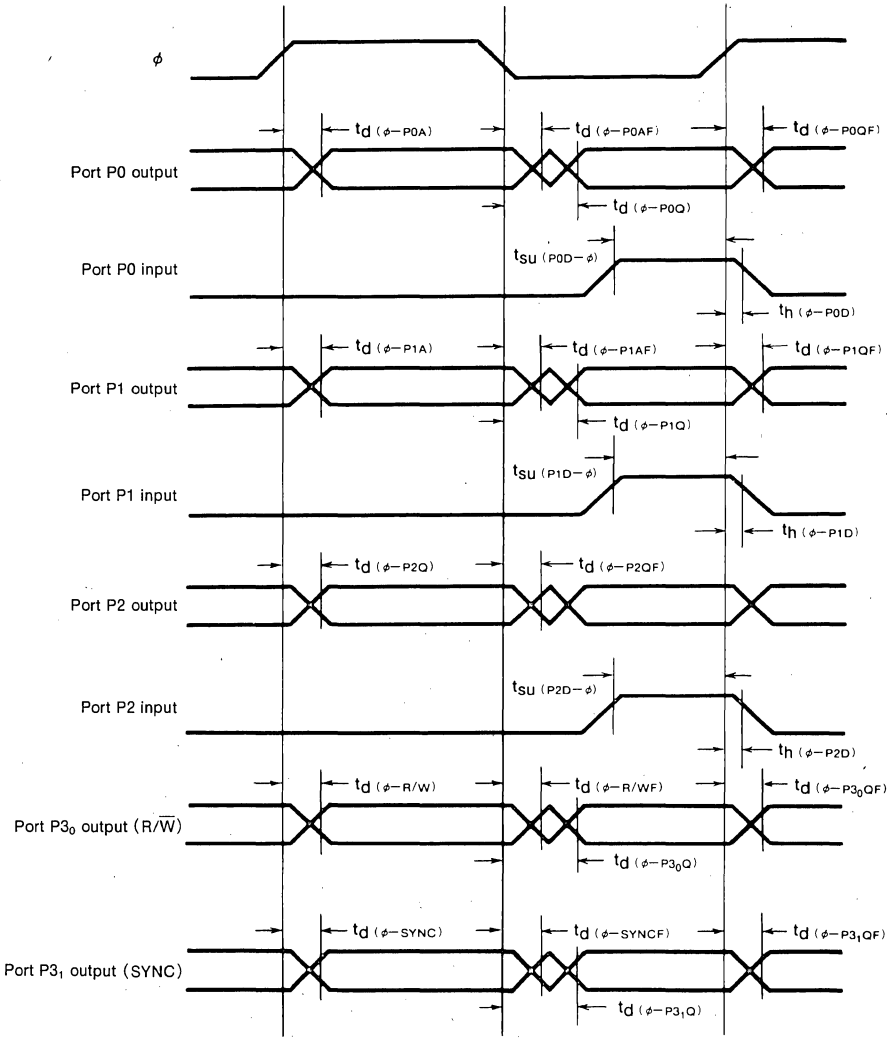
TIMING DIAGRAMS

In single-chip mode

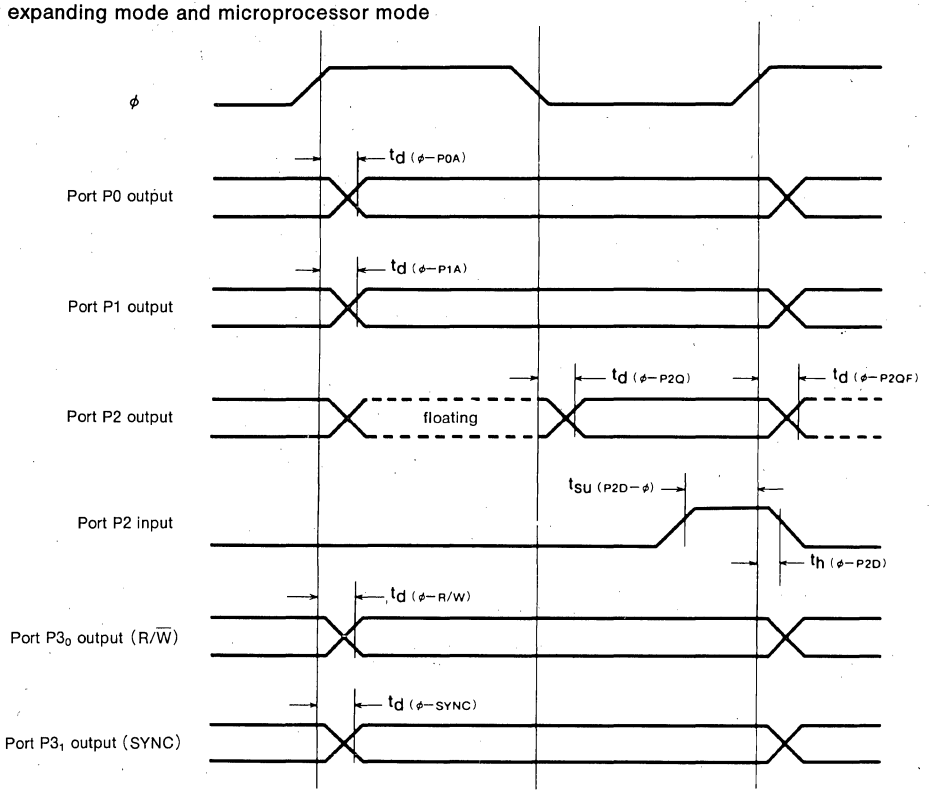


MITSUBISHI ELECTRIC

In eva-chip mode



In memory expanding mode and microprocessor mode



M37410E6-XXXFP

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

EPROM VERSION of M37410M3-XXXFP,M37410M4-XXXFP

DESCRIPTION

The M37410E6-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 80-pin shrink plastic molded QFP. The features of this chip are similar to those of the M37410M4-XXXFP except that this chip has a 98304-bit (12288 words × 8 bits) EPROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the EPROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose EPROM writers can be used for the built-in EPROM, this chip is suitable for small quantity production runs.

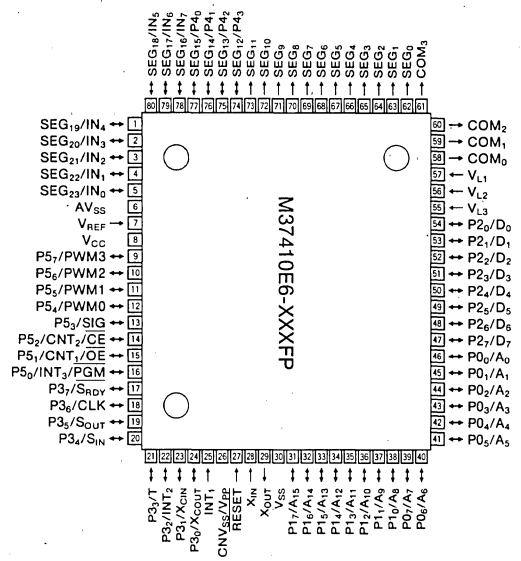
DISTINCTIVE FEATURES

- Number of basic instructions 69
- Memory size EPROM ..... 12288 bytes
  RAM ..... 256 bytes
- Instruction execution time
  (minimum instructions at 8MHz frequency)
  at high-speed mode ..... 1 μs
  at low-speed mode ..... 4 μs
- Single power supply
  f(X_{IN})=8MHz ..... 4.75~5.25V
- Power dissipation
  normal operation mode (at 8MHz frequency)
  ..... 30mW (V_{CC}=5V, Typ.)
  low-speed operation mode (at 32kHz frequency for clock function) ..... 54μW(V_{CC}=3V, Typ.)
- RAM retention voltage (stop mode)
  ..... 2.0V≦V_{RAM}≦5.5V
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 9 types, 5 vectors
- 8-bit timer 4
- 16-bit timer ..... 1 (Two 8-bit timers make one set)
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P4) 40
- Serial I/O (8-bit) 1
- A-D converter 8-bit, 8-channel
  conversion speed (25μs)
- LCD controller/driver (1/2, 1/3 bias, 1/2, 1/3, 1/4 duty)
  segment output 24
  common output 4
- Two clock generating circuits (One is for main clock, the other is for clock function)
- EPROM (equivalent to the M5L27128)
  program voltage 21V

APPLICATION

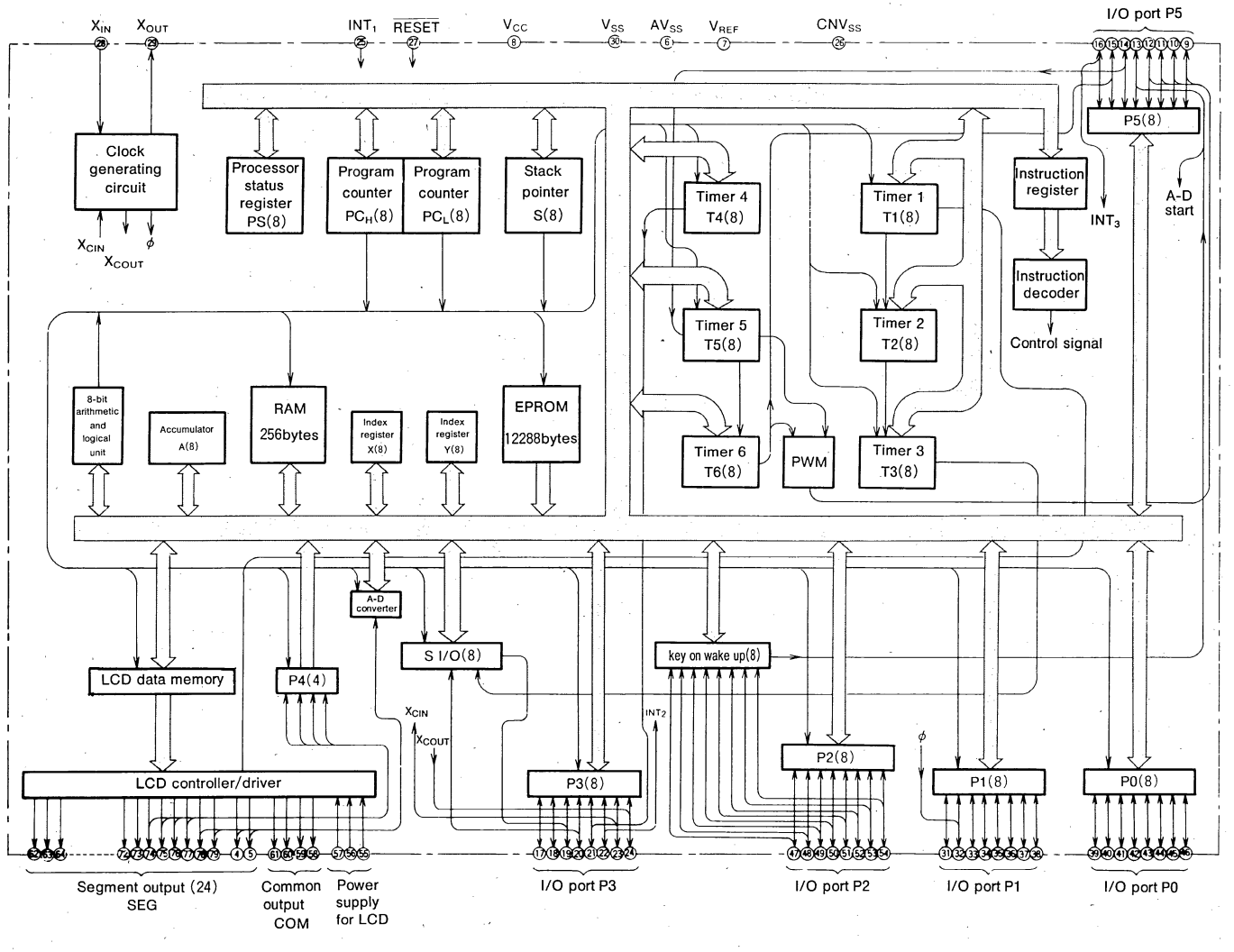
Audio-visual equipment
Remote control
Camera

PIN CONFIGURATION (TOP VIEW)



Outline 80P6S

M37410E6-XXXFP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONS OF M37410E6-XXXFP

Parameters			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 8MHz of frequency)
Clock frequency			8MHz
Memory size	EPROM		12288bytes (Note 1)
	RAM		256bytes
	RAM for display LCD		12bytes
Input/Output port	P0, P1, P2, P3, P5	I/O	8-bitX5
	P4	Input	4-bitX1 (Port P4 are in common with SEG)
	SEG	LCD output	24-bitX1
	COM	LCD output	4-bitX1
Serial I/O			8-bitX1
Timers			8-bit timerX4
			16-bit timerX1 (combination of two 8-bit timers)
LCD controller/driver	Bias		1/2, 1/3 bias selectable
	Duty ratio		1/2, 1/3, 1/4 duty selectable
	Common output		4
	Segment output		24(SEG_{12}~SEG_{23} are in common with port P4)
Subrotine nesting			96(max)
Interrupt			Three external Interrupts, Three timer interrupts (or two timer, one serial I/O)
Clock generating circuit			Two built-in circuit (ceramic or quartz crystal oscillator)
Operating temperature range			−20~75℃
Device structure			CMOS silicon gate
Package			80-pin plastic molded QFP

Note 1 : The EPROM programming voltage is 21V (equivalent to the M5L27128)

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V_{CC} V_{SS}	Single-chip /EPROM	Power supply		Supply 5V±5% to V_{CC} and 0V to V_{SS}.
CNV_{SS}/ V_{PP}	Single-chip	CNV_{SS} input	Input	Connect to V_{SS}.
	EPROM	V_{PP} input		Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Single-chip	Reset input	Input	To reset, keep this input terminal low for more than 16μs (min) under normal V_{CC} conditions. If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
	EPROM	Reset input		Connect to 0V.
X_{IN}	Single-chip /EPROM	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}		Clock output	Output	
INT_1	Single-chip	Interrupt input	Input	This is the highest order interrupt input pin.
	EPROM	Interrupt input	Input	Connect to 0V.
$P0_0$~$P0_7$	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
	EPROM	Address input A_0~A_7	Input	P0 works as the lower 8 bit address input (A_0~A_7).
$P1_0$~$P1_7$	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open drain.
	EPROM	Address input A_8~A_{13}	Input	$P1_0$~$P1_5$ works as the higher 6 bit address inputs (A_8~A_{13}). Connect $P1_6$~$P1_7$ to V_{CC}.
$P2_0$~$P2_7$	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as port P0. Also all bits are for key on wake up input pins.
	EPROM	Data input/ output D_0~D_7	I/O	Port P2 works as an 8 bit data bus (D_0~D_7).
$P3_0$~$P3_7$	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$ and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$, $P3_2$, $P3_1$, and $P3_0$ work as timer 4 overflow signal divided by 2 output pin (T), INT_2 pin, X_{CIN} and X_{COUT} pins, respectively.
	EPROM	Input port P3	Input	Connect to 0V.
$SEG_{12}/P4_3$ { $SEG_{15}/P4_0$	Single-chip	Segment output /input port P4	Output /Input	SEG_{12}~SEG_{15} are segment output pins. Also these work as input port P4 by 2-bit unit.
	EPROM	Input port P4	Input	Conect to V_{CC}.
$P5_0$~$P5_7$	Single-chip	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as P1. $P5_0$, $P5_1$, $P5_2$ and $P5_3$ are in common with INT_3, timer3 input, timer5 input and A-D trigger input, respectively.
	EPROM	Select mode	Input	$P5_2$, $P5_1$, $P5_0$ work as $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$, respectively. Connect to $P5_5$~$P5_7$ to 0V, and $P5_3$~$P5_4$ to V_{CC}.

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V_{L1}~V_{L3}	Single-chip	Voltage input for LCD	Input	These are voltage input pins for LCD. Supply voltage as $0V \leqq V_{L1} \leqq V_{L2} \leqq V_{L3} \leqq V_{CC}$. $0 \sim V_{L3}V$ is supplied to LCD.
	EPROM	Voltage input for LCD	Input	Connect to V_{CC}.
COM_0~ COM_3	Single-chip	Common output	Output	These are LCD common output pins.
	EPROM	Common output	Output	Connect to V_{CC}.
SEG_0~ SEG_{11}	Single-chip	Segment output	Output	These are LCD segment output pins.
	EPROM	Segment output	Output	Connect to V_{CC}.
SEG_{16}/IN_7 ⟆ SEG_{23}/IN_0	Single-chip	Segment output /analog input	I/O	SEG_{16}~SEG_{23} work as analog input pins IN_7~IN_0. SEG_{16}~SEG_{19} are used by 2-bit unit and SEG_{20}~SEG_{23} by 4-bit unit.
	EPROM	Analog input	Input	Connect to V_{CC}.
AV_{SS}	Single-chip	Analog voltage input	Input	GND input pin for the A-D converters.
	EPROM	Analog voltage input	Input	Connect to V_{SS}.
V_{REF}	Single-chip	Reference voltage input	Input	Referrence input pin for A-D converters.
	EPROM	Reference voltage input	Input	Connect to V_{CC}.

EPROM MODE

The M37410E6-XXXFP features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L"), the chip automatically enters the EPROM programming mode. Table 1 list the correspondence between pins and Figure 1 gives the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P5_0$~$P5_2$, and CNV_{SS} are used for the EPROM (equivalent to the M5L27128). When in this mode, the built-in EPROM can be written to or read from using these pins in the same way as with the M5L27128. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1 Pin function in EPROM programming mode

	M37410E6-XXXFP	M5L27128
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0$~$P1_5$	A_0~A_{13}
Data I/O	Port P2	D_0~D_7
$\overline{CE}$	$P5_2/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P5_1/\overline{OE}$	$\overline{OE}$
$\overline{PGM}$	$P5_0/\overline{PGM}$	$\overline{PGM}$

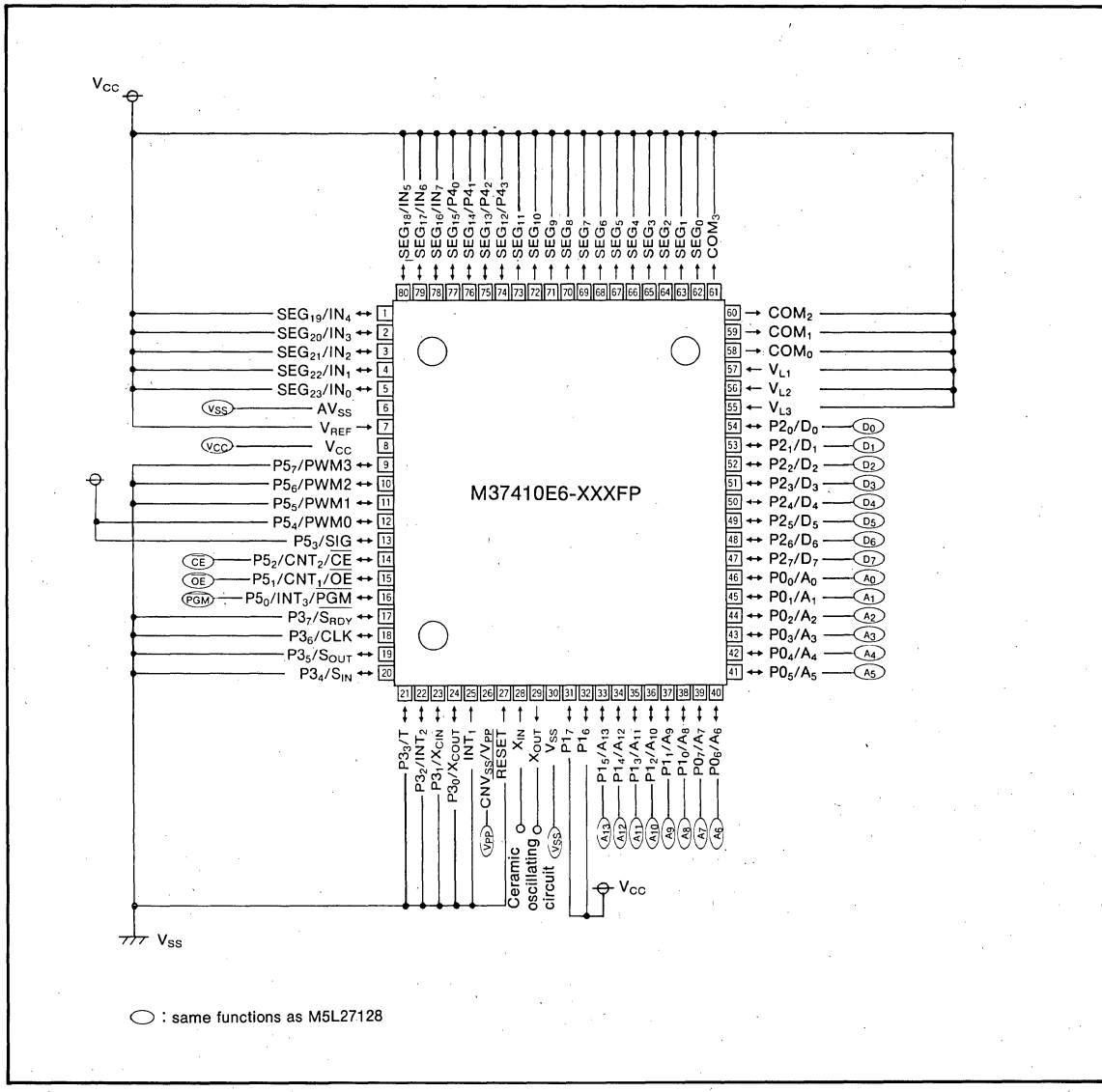


Fig.1 Pin connection in EPROM programming mode

MITSUBISHI ELECTRIC

EPROM READING, WRITING AND ERASING

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and the $\overline{PGM}$ pin to a "H" level. Input the address of the data (A_0~A_{13}) to be read and the data will be output to the I/O pins D_0~D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the EPROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0~A_{13}, and the data to be written is input to pins D_0~D_7. Set the $\overline{PGM}$ pin to a "L" level to begin writing.

NOTES ON HANDLING

Since a high voltage (21V) is used to write data, care should be taken when turning on the EPROM writer's power.

Table 2 I/O signal in each mode

Mode \ Pin	$\overline{CE}$(14)	$\overline{OE}$(15)	$\overline{PGM}$(16)	V_{PP}(26)	V_{CC}(8)	Data I/O (23~54)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse(V_{IH}→V_{IL})	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼7	V
V_I	LCD supply V_{L1}∼V_{L3}	$V_{L1}<V_{L2}<V_{L3}$	−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P3_0$, $P3_1$, $P4_0$∼$P4_3$ IN_0∼IN_7, V_{REF}, X_{IN}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}, (Note 1)		−0.3∼7	V
V_I	Input voltage INT_1, $\overline{RESET}$, $P1_0$∼$P1_7$, $P3_2$∼$P3_7$, $P5_0$∼$P5_7$		−0.3∼10	V
V_O	Output voltage $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P3_0$, $P3_1$ COM_0∼COM_3, SEG_0∼SEG_{23}, X_{OUT}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P1_0$∼$P1_7$, $P3_2$∼$P3_7$, $P5_0$∼$P5_7$		−0.3∼10	V
Pd	Power dissipation	T_a = 25℃	300	mW
Topr	Operating temperature		−20∼75	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : In EPROM programming mode, CNV_{SS} is 22.0V

RECOMMENDED OPERATING CONDITIONS (V_{CC}= 5 V± 5 %, T_a=−10∼75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Nom.	Max.	
V_{CC}	Supply voltage (Note 2)		4.75	5	5.25	V
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P3_0$, $P3_1$, $P4_0$∼$P4_3$, X_{IN}, CNV_{SS} (Note 3)		0.7V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$∼$P2_7$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P1_0$∼$P1_7$, $P3_3$∼$P3_7$, $P5_1$∼$P5_7$, S_{IN}		0.7V_{CC}		10	V
V_{IH}	"H" input voltage $P5_0$, INT_1, INT_2, INT_3, $P3_2$∼$P3_7$, CNT_1, CNT_2, SIG, CLK		0.8V_{CC}		10	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{CIN}		0.85V_{CC}		10	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ $P4_0$∼$P4_3$, $P5_1$∼$P5_7$, S_{IN}		0		0.3V_{CC}	V
V_{IL}	"L" input voltage $P2_0$∼$P2_7$, $P3_2$∼$P3_7$, $P5_0$, INT_1, INT_2, INT_3, CNT_1, CNT_2, SIG, CLK		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0		0.15V_{CC}	V
I_{OH}	"H" output current $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, X_{OUT}				−1	mA
I_{OL}	"L" output current $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, X_{OUT}, PWM_0∼PWM_3, T, S_{OUT}, CLK, $\overline{S_{RDY}}$, SIG (Note 5)				1	mA
I_{OL}	"L" output current $P1_0$∼$P1_7$ (Note 6)	V_{CC}=4.75∼5.25V			20	mA
f(X_{IN})	Clock input oscillating frequency		0.2			MHz
f(X_{CIN})	Clock oscillating frequency for clock function		30		50	kHz

Note 2 : When only maintaining the RAM data, minimum value of V_{CC} is 2V.
3 : When P3 is X_{CIN} mode, the limits of V_{IH} of $P3_1$ is $0.85V_{CC} \leqq V_{IH} \leqq V_{CC}$, $0 \leqq V_{IL} \leqq 0.15V_{CC}$.
4 : Total of $I_{OH(peak)}$ of ports P0, P2 and X_{OUT} is less than 35mA.
5 : Total of $I_{OL(peak)}$ of ports P0, P2, P3 and P5 is less than 32mA.
6 : Total of $I_{OL(peak)}$ of P1 is less than 80mA.
Total of $I_{OL(avg.)}$ of P1 is less than 40mA.

ELECTRICAL CHARACTERISTICS (T_a=25℃, V_{CC}=5V, V_{SS}=0V, $f_{(X_{IN})}$=8MHz, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P2_0$~$P2_7$		V_{CC}=5V, I_{OH}=−0.5mA		4			V
V_{OH}	"H" output voltage X_{OUT}		V_{CC}=5V, I_{OH}=−0.3mA		4			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, T, S_{OUT}, CLK, $\overline{S_{RDY}}$ SIG, PWM0~PWM3		V_{CC}=5V				1	V
V_{OL}	"L" output voltage $P1_0$~$P1_7$		V_{CC}=5V, I_{OL}=20mA				2	V
V_{OL}	"L" output voltage X_{OUT}		V_{CC}=5V, I_{OL}=0.3mA				1	V
V_{T+}−V_{T-}	Hysteresis	INT_1, INT_2, INT_3, CLK, CNT_1 CNT_2, SIG, S_{IN}, $P2_0$~$P2_7$, X_{CIN}	V_{CC}=5V			0.7		V
V_{T+}−V_{T-}	Hysteresis	$\overline{RESET}$	V_{CC}=5V			2		V
V_{T+}−V_{T-}	Hysteresis	X_{IN}	V_{CC}=5V			0.5		V
I_{IL}	"L" input current	{$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$} Without pull-up T_r.(Note 1) IN_0~IN_7, INT_1, $\overline{RESET}$, X_{IN}	V_{CC}=5V V_I=0V				−5	μA
I_{IH}	"H" input current	$P0_0$~$P0_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$ $P4_0$~$P4_7$, IN_0~IN_7 X_{IN}, X_{CIN}, CNV_{SS}	V_{CC}=5V V_I=5V				5	μA
I_{IH}	"H" input current	{$P1_0$~$P1_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$} Without pull-up T_r. INT_1, INT_2, INT_3, CNT_1, CNT_2 SIG, $\overline{RESET}$, S_{IN}, CLK	V_I=10V				10	μA
R_{PL}	Pull-up T_r	$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$	V_{CC}=5V, V_I=0V		35	70	140	kΩ
R_{COM}	Output impedance COM_0~COM_3		V_{L1}=V_{CC}/3, V_{L2}=2V_{L1}, V_{L3}=V_{CC} Other COM, SEG pins are opend	V_{CC}=5V		200		Ω
R_S	Output impedance SEG_0~SEG_{23}			V_{CC}=5V		2		kΩ
I_{CC}	Supply current	at operation	$f(X_{IN})$=8MHz High-speed mode V_{CC}=5V			6		mA
			$f(X_{CIN})$=32kHz, V_{CC}=3V			18		μA
		at wait state	$f(X_{IN})$=32kHz, V_{CC}=5V			4		
		at stop state	V_{CC}=5V,all clock stop.	T_a=25℃		0.1		
V_{RAM}	RAM retention voltage				2		5.25	V

Note 1 : Also the same as when each pin is used as INT_2, INT_3, CNT1, CNT2, SIG, S_{IN} and X_{IN}, respectively.

M37450E4-XXXSP/FP
M37450E4SS/FS

EPROM VERSION of M37450M4-XXXSP/FP

DESCRIPITION

The M37450E4-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. The features of this chip are simiar to those of the M37450M4-XXXSP except that this chip has a 65536-bit (8192 words × 8 bits) EPROM built-in. This single-chip microcomputer is useful for office automation appliances and consumer appliance controllers.

In addition to its simple instruction sets, the EPROM, RAM and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose EPROM writes can be used for small quantity production runs. It also has a unique feature that enables it to be used as a slave microcomputer.

The M37450E4SS and the M37450E4FS are the window type. The differences between the M37450E4-XXXSP and the M37450E4-XXXFP, and between the M37450E4SS and the M37450E4FS are the package outline and the power dissipation ability (absolute maximum ratings).

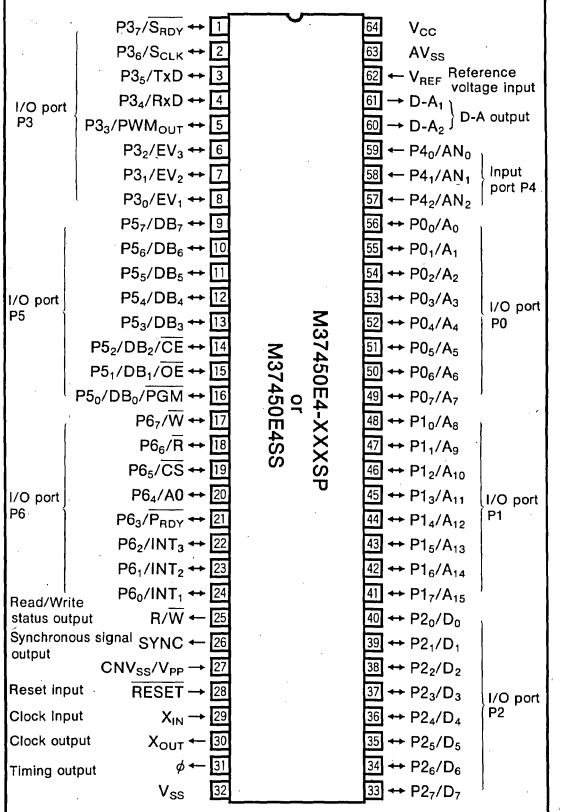
DISTINCTIVE FEATURES

- Number of basic instructions 71
  69 MELPS 740 basic instructions + 2 multiply/divide instructions
- Memory size EPROM ..... 8192 bytes
  RAM ..... 256 bytes
- Instruction execution time
  (shortest instruction at 10 MHz) ..... 0.8 μs (min.)
- Single power supply ..... 5V ± 5%
- Power dissipation normal operation mode
  (at 10 MHz frequency) 30mW
- Subroutine nesting ..... 96 levels max.
- Interrupts ..... 15 events
- Master CPU bus interface ..... 1 byte
- 16-bit timer 3
- 8-bit timer (Serial I/O use) 1
- Serial I/O (UART or clock synchronous) 1
- A-D converter (8-bit resolution) ..... 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ..... 2 channels
- PWM output (8-bit or 16-bit) 1
- Programmble I/O
  (Ports P0, P1, P2, P3, P5, P6) 48
- Input (Port P4) ..... 3 (DIP), 8 (QFP)
- Output (Port D-A_1, D-A_2) 2
- EPROM (equivalent to the M5L2764)
  program voltage 21V

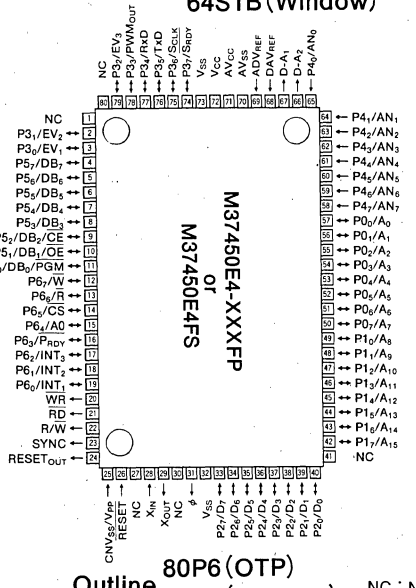
APPLICATION

Slave controller for PPCs, facsimiles, and page printers
HDD, optical disk, inverter, and industrial motor controllers
Industrial robots and machines

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B (OTP)
64S1B (Window)

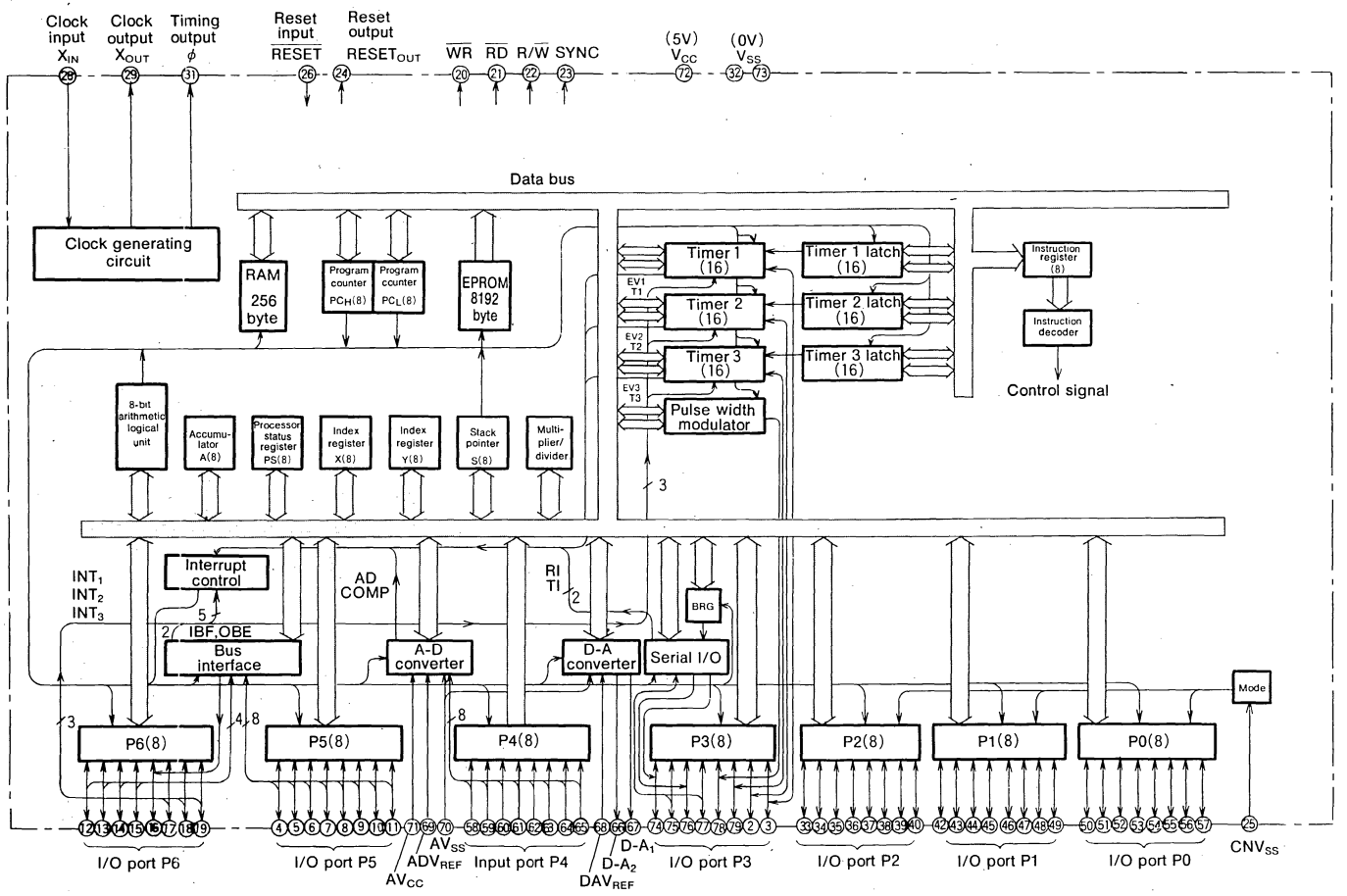


Outline 80P6 (OTP)
80S6 (Window)

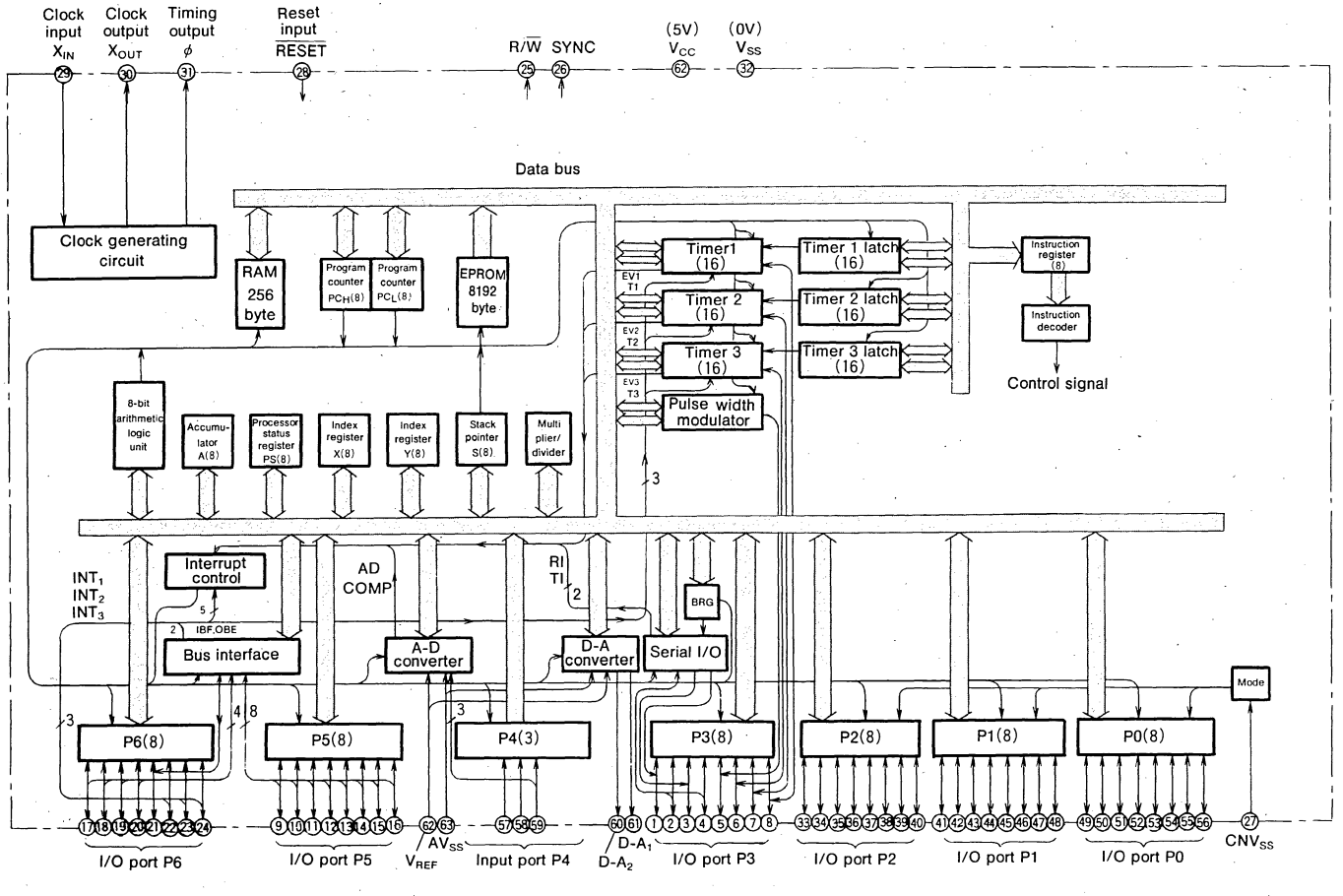
NC : No connection

MITSUBISHI ELECTRIC

M37450E4-XXXFP, M37450E4FS BLOCK DIAGRAM



M37450E4-XXXSP, M37450E4SS BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONS OF M37450E4-XXXSP/FP, M37450E4SS/FS

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0.8μs (minimum instructions, at 10MHz of frequency)
Clock frequency			10MHz (max.)
Memory size	EPROM		8192 bytes
	RAM		256 bytes
Input/Output port	P0~P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (Serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			96-levels
Interrupts			6 external interrupts, 8 internal interrupts One software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±5%
Power dissipation			30mW (at 10MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate
Package	M37450E4-XXXSP		64-pin shrink plastic molded DIP
	M37450E4-XXXFP		80-pin plastic molded QFP
	M37450E4SS		64-pin shrink ceramic DIP
	M37450E4FS		80-pin ceramic QFP

PIN DESCRIPTION (normal operation mode)

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}/V_{PP}	CNV_{SS}		Controls the processor mode of the chip. Normally connected to V_{SS} or V_{CC}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four.
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs.
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus. It is "H" during read and "L" during write.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. The output structure is CMOS output. The low-order bits of the address are output except in single-chip mode.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The high-order bits of the address are output except in single-chip mode.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. Used as data bus except in single-chip mode.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. Serial I/O, PWM output, or event I/O function can be selected with a program.
$P4_0$~$P4_2$ ($P4_0$~$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter. The 64-pin model has three pins and the 80-pin model has eight pins. They may also be used as digital input pins.
$P5_0$~$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0. This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program.
$P6_0$~$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0. Pins $P6_3$~$P6_7$ change to a control bus for the master CPU when slave mode is selected with a program. Pins $P6_0$~$P6_2$ may be programmed as external interrupt input pins.
$D\text{-}A_1$, $D\text{-}A_2$	D-A output	Output	Analog signal from D-A converter is output.
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter. This pin is for 64-pin model only.
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter. This pin is for 80-pin model only.
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter. This pin is for 80-pin model only.
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter. Same voltage as V_{SS} is applied.
AV_{CC}	Analog power supply		Power supply input pin for A-D converter. This pin is for 80-pin model only. Same voltage as V_{CC} is applied. In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally.

PIN DESCRIPTION (normal operation mode)

Pin	Name	Input/ Output	Functions
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus. This pin is for 80-pin model only.
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component. This pin is for 80-pin model only.
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset. It is used as a reset output signal for peripheral components. This pin is for 80-pin model only.

PIN DESCRIPTION (EPROM mode)

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}/V_{PP}	V_{PP}	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}
X_{IN}	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	For timing output
SYNC	Synchronous signal output	Output	Kept to open ("L" signal is output).
R/$\overline{W}$	Read/Write status output	Output	Kept to open ("H" signal is output).
$P0_0$~$P0_7$	I/O port P0	Input	P0 works as the lower 8-bit address input.
$P1_0$~$P1_7$	I/O port P1	Input	P1 works as the higher 8-bit address input.
$P2_0$~$P2_7$	I/O port P2	I/O	P2 works as an 8-bit data bus.
$P3_0$~$P3_7$	I/O port P3	Input	Connect to V_{SS}
$P4_0$~$P4_2$	Input port P4	Input	Connect to V_{SS}
$P5_0$~$P5_7$	I/O port P5	Input	$P5_0$, $P5_1$, $P5_2$ works as $\overline{PGM}$, $\overline{OE}$, and $\overline{CE}$ inputs respectively. Connect $P5_3$ and $P5_4$ to V_{CC} and $P5_5$~$P5_7$ to V_{SS}.
$P6_0$~$P6_7$	I/O port P6	Input	Connect to V_{SS}.
V_{REF}	Reference voltage input	Input	Connect to V_{SS}.
ADV_{REF}	A-D reference voltage input	Input	Connect to V_{SS}.
DAV_{REF}	D-A reference voltage input	Input	Connect to V_{SS}.
AV_{SS}	Analog power	Input	Connect to V_{SS}.
AV_{CC}	Analog power	Input	Connect to V_{SS}.
$\overline{RD}$	Read signal output	Output	Kept to open ("H" signal is output)
$\overline{WR}$	Write signal output	Output	Kept to open ("H" signal is output)
$RESET_{OUT}$	Reset output	Output	Kept to open ("H" signal is output)

EPROM MODE

The M37450E4-XXXSP/FP, M37450E4SS/FS features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L") and CNV_{SS}/V_{PP} signal level is high ("H"), the chip automatically enters the EPROM programming mode. Table 1 list the correspondence between pins and Figure 1 and Figure 2 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P5_0 \sim P5_2$ and CNV_{SS} are used for the EPROM (equivalent to the M5L2764). When in this mode, the built-in EPROM can be written to or read from using these pins in the same way as with the M5L2764. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1 Pin function in EPROM programming mode

	M37450E4-XXXSP/FP, M37450E4SS/FS	M5L2764
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0 \sim P1_4$	$A_0 \sim A_{12}$
Data I/O	Port P2	$D_0 \sim D_7$
$\overline{CE}$	$P5_2/DB_2/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P5_1/DB_1/\overline{OE}$	$\overline{OE}$
$\overline{PGM}$	$P5_0/DB_0/\overline{PGM}$	$\overline{PGM}$

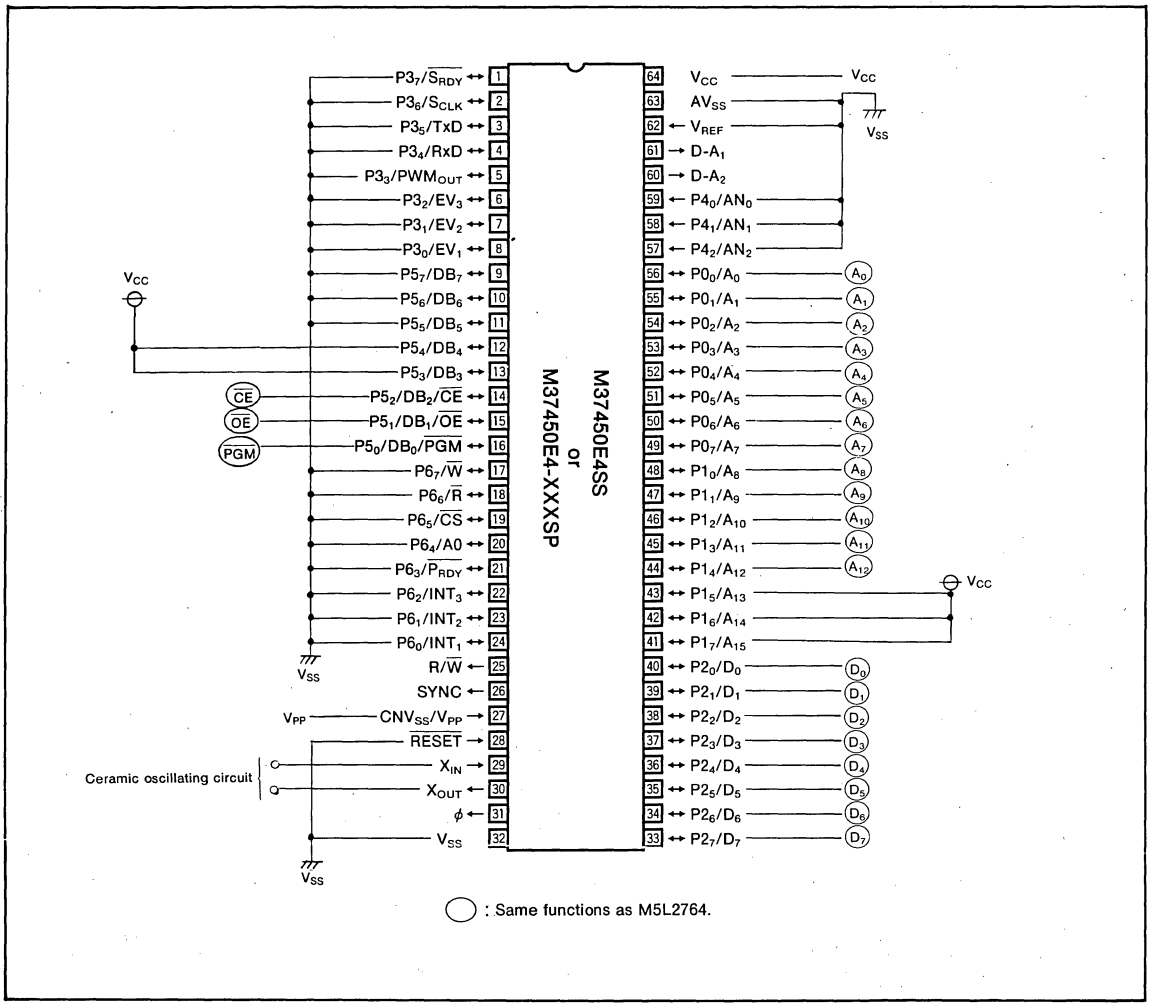


Fig. 1 Pin connection in EPROM programming mode (64-pin model)

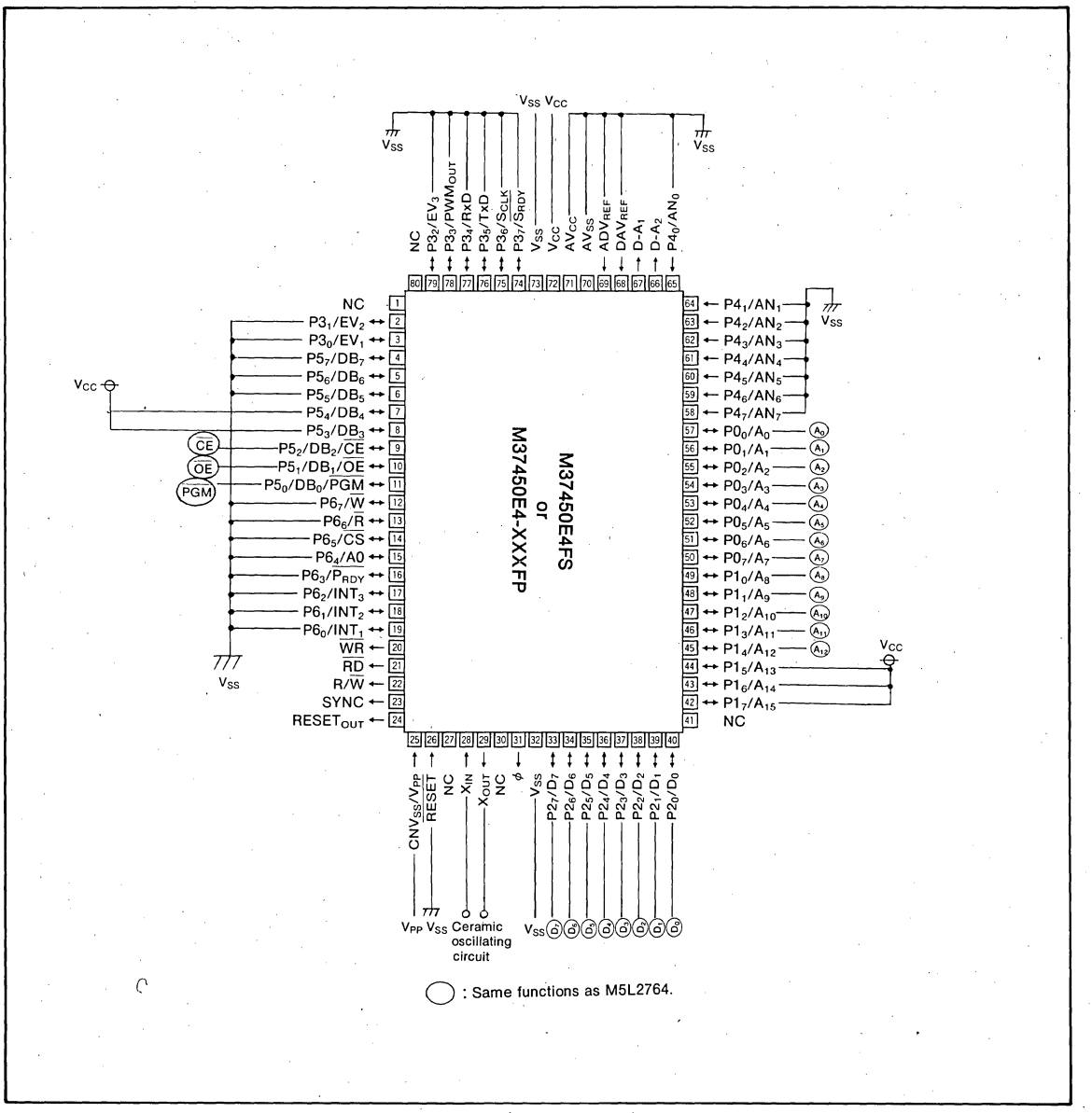


Fig. 2 Pin connection in EPROM programming mode (80-pin model)

EPROM READING, WRITING AND ERASING

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and the $\overline{PGM}$ pin to a "H" level. Input the address of the data ($A_0 \sim A_{12}$) to be read and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the EPROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{12}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the $\overline{PGM}$ pin to a "L" level to begin writing.

Erasing

Data can only erased on the M37450E4SS/FS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is $15W \cdot s/cm^2$.

NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage (21V) is used to write data, care should be taken when turning on the EPROM writer's power.

Table 2 I/O signal in each mode

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Port P2
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse($V_{IH} \rightarrow V_{IL}$)	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state.	−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3∼7	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3∼13	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, $RESET_{OUT}$, SYNC		−0.3∼V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000 (Note 1)	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : 500mW for QFP type.

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±5%, Ta=−10∼70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 2)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (except Note 2)	2.0		V_{CC}	V
V_{IL}	"L" Input voltage CNV_{SS} (Note 2)	0		0.2V_{CC}	V
V_{IL}	"L" Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (except Note 2)	0		0.8	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 3)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 3)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		10	MHz

Note 2 : Ports operate as INT_1∼INT_3($P6_0$∼$P6_2$), EV_1∼EV_3($P3_0$∼$P3_2$), R_XD($P3_4$) and S_{CLK}($P3_6$)

Note 3 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms.

Note 4 : The total of "L" output current $I_{OL(peak)}$ of port P0, P1 and P2 is less than 40mA.
The total of "H" output current $I_{OH(peak)}$ of port P0, P1 and P2 is less than 40mA.
The total of "L" output current $I_{OL(peak)}$ of port P3, P5, P6, R/$\overline{W}$ SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA.
The total of "H" output current $I_{OH(peak)}$ of port P3, P5, P6, R/$\overline{W}$ SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = −10~70℃, f(X_{IN}) = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH}=−2mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OH}=−5mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL}=2mA			0.45	V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OL}=5mA			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1~INT_3($P6_0$~$P6_2$), EV_1~EV_3($P3_0$~$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation f(X_{IN})=10MHz		6	10	mA
		At stop mode (Note 5)		1	10	μA

Note 5 : The terminals $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ, D-A_1 and D-A_2 are all open. The other ports, which are in the input mode, are connected to V_{SS}. A-D converter is in the A-D completion state. The current through ADV_{REF} and DAV_{REF} is not included(Fig.6).

A-D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, f(X_{IN})=10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5.12V		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_C(\phi)$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}=5V	2	7.5	10	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}=5V	0.5	0.7	2.5	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Abusolute accuracy	V_{CC}=DAV_{REF}=5.12V			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current		0	2.5	5	mA

TIMING REQUIREMENTS

Port/single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig. 3	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_C(X_{IN})$	External clock input cycle time		100		1000	ns
$t_W(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_W(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig. 3	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A_0 setup time		40			ns
$t_{su(A-W)}$	A_0 setup time		40			ns
$t_{h(R-A)}$	A_0 hold time		10			ns
$t_{h(W-A)}$	A_0 hold time		10			ns
$t_{W(R)}$	Read pulse width		160			ns
$t_{W(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig. 4	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A_0 setup time		40			ns
$t_{h(E-A)}$	A_0 hold time		10			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		10			ns
$t_{W(EL)}$	Enable clock "L" pulse width		160			ns
$t_{W(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(D-\phi)}$	Data input setup time	Fig. 5	130			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{SU(D-RD)}$	Data input setup time		130			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

SWITCHING CHARACTERISTICS

Port/single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig. 3			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{C(\phi)}$	Cycle time		400		4000	ns
$t_{W(\phi H)}$	ϕ clock pulse width ("H" level)		190			ns
$t_{W(\phi L)}$	ϕ clock pulse width ("L" level)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(\overline{R}-D)}$	Data output enable time after read	Fig. 4			120	ns
$t_{v(\overline{R}-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(R-\overline{PR})}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-\overline{PR})}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±5%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{a(E-D)}$	Data output enable time after read	Fig. 4			120	ns
$t_{v(E-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(E-\overline{PR})}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(\phi-A)}$	address delay time after ϕ	Fig. 5			150	ns
$t_{v(\phi-A)}$	address effective time after ϕ		10			ns
$t_{v(\overline{RD}-A)}$	address effective time after $\overline{RD}$		10			ns
$t_{v(\overline{WR}-A)}$	address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	data output delay time after ϕ				160	ns
$t_{d(\overline{WR}-D)}$	data output delay time after $\overline{WR}$				160	ns
$t_{v(\phi-D)}$	data output effective time after ϕ		20			ns
$t_{v(\overline{WR}-D)}$	data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				150	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				150	ns
$t_{W(\overline{RD})}$	$\overline{RD}$ pulse width		170			ns
$t_{W(\overline{WR})}$	$\overline{WR}$ pulse width		170			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V
V_{IL} 0.45V
Output test level : V_{OH} 2.0V
V_{OL} 0.8V

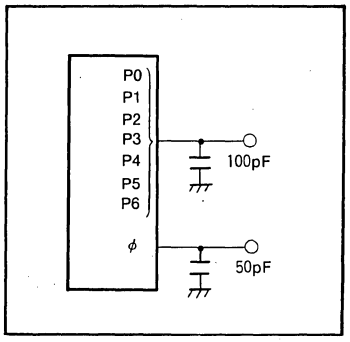


Fig. 3 Test circuit in single-chip mode

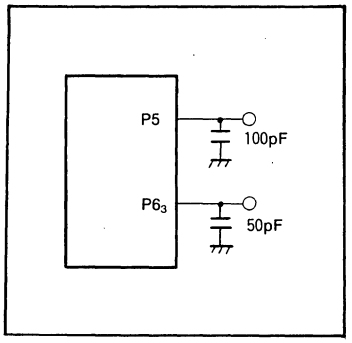


Fig. 4 Master CPU bus interface test circuit

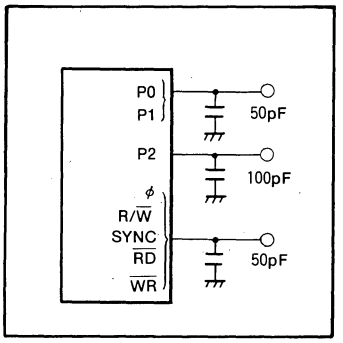


Fig. 5 Local bus test circuit

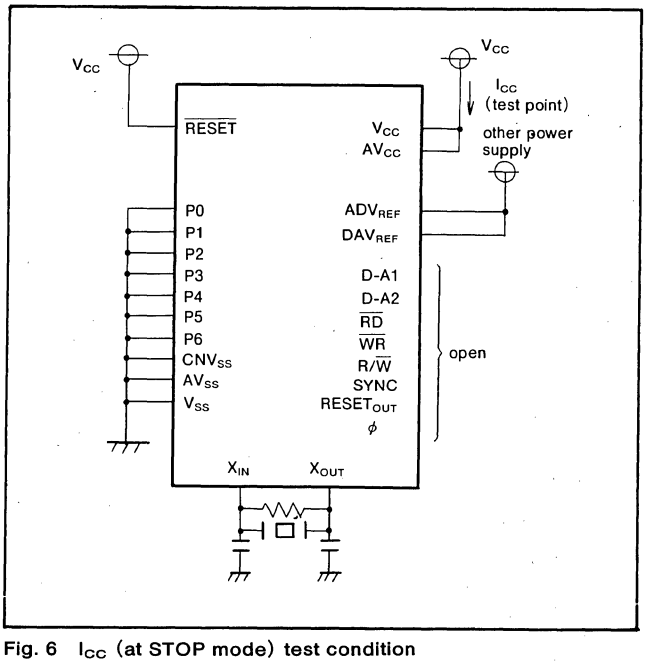
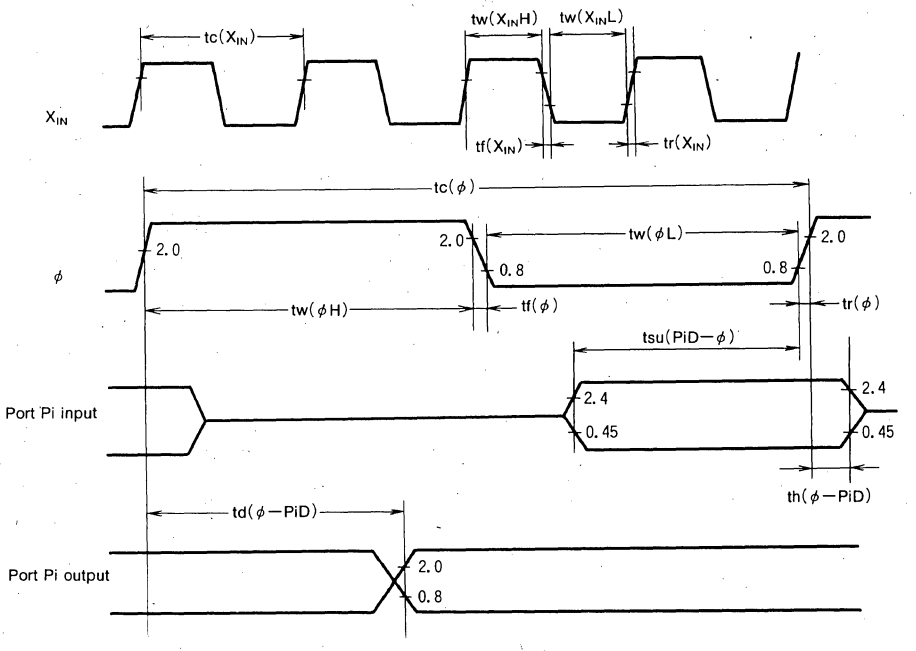


Fig. 6 I_{CC} (at STOP mode) test condition

TIMING DIAGRAM

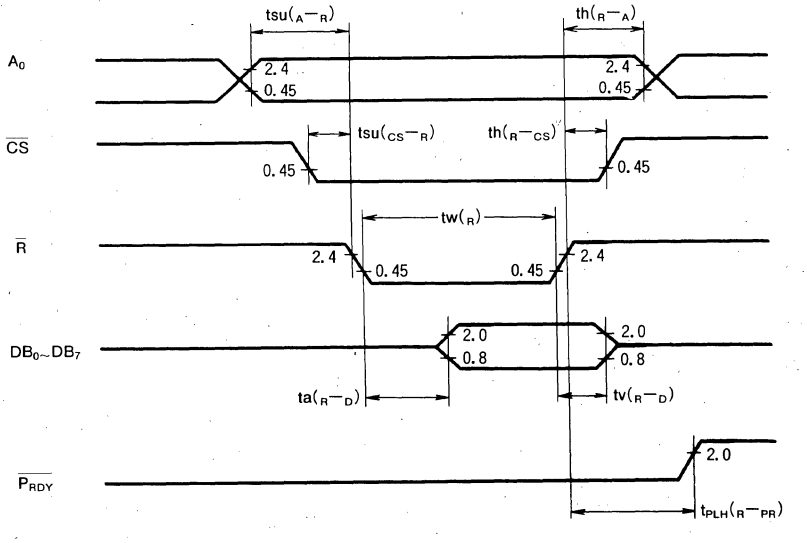
Port/single-chip mode timing diagram



Note : V_{IH}=0.8V_{CC}, V_{IL}=0.16V_{CC} of X_{IN}

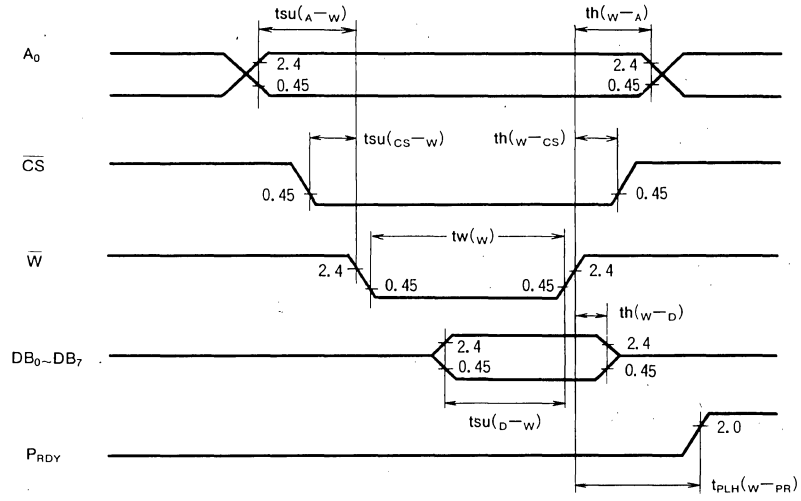
Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

Read

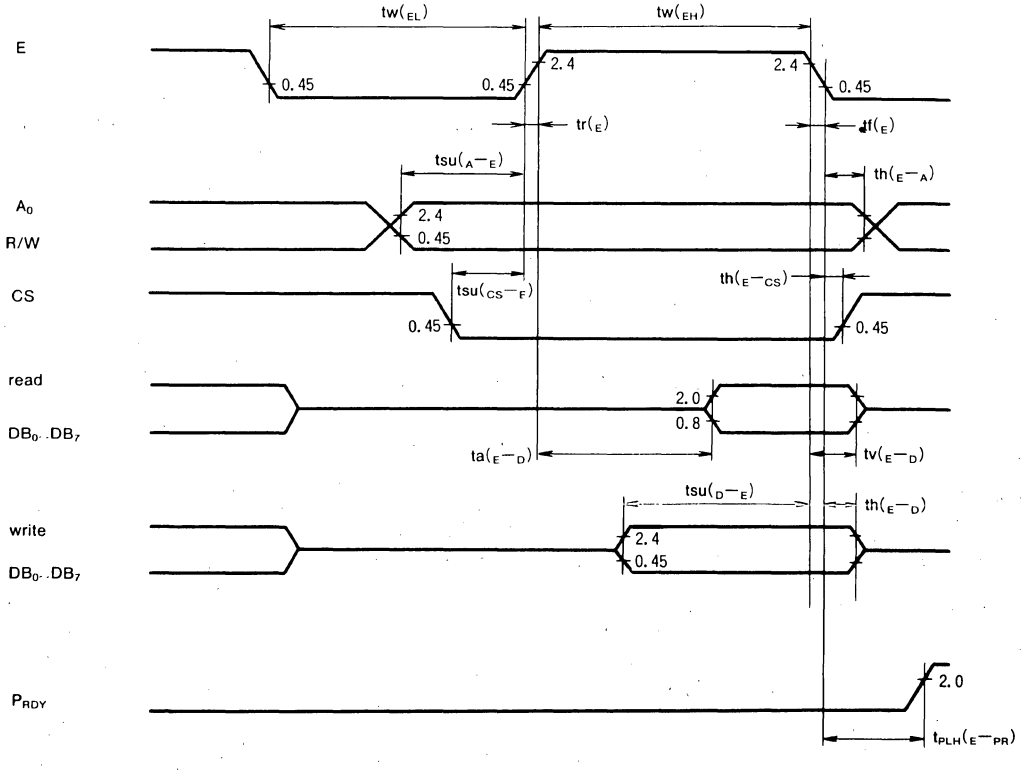


MITSUBISHI ELECTRIC

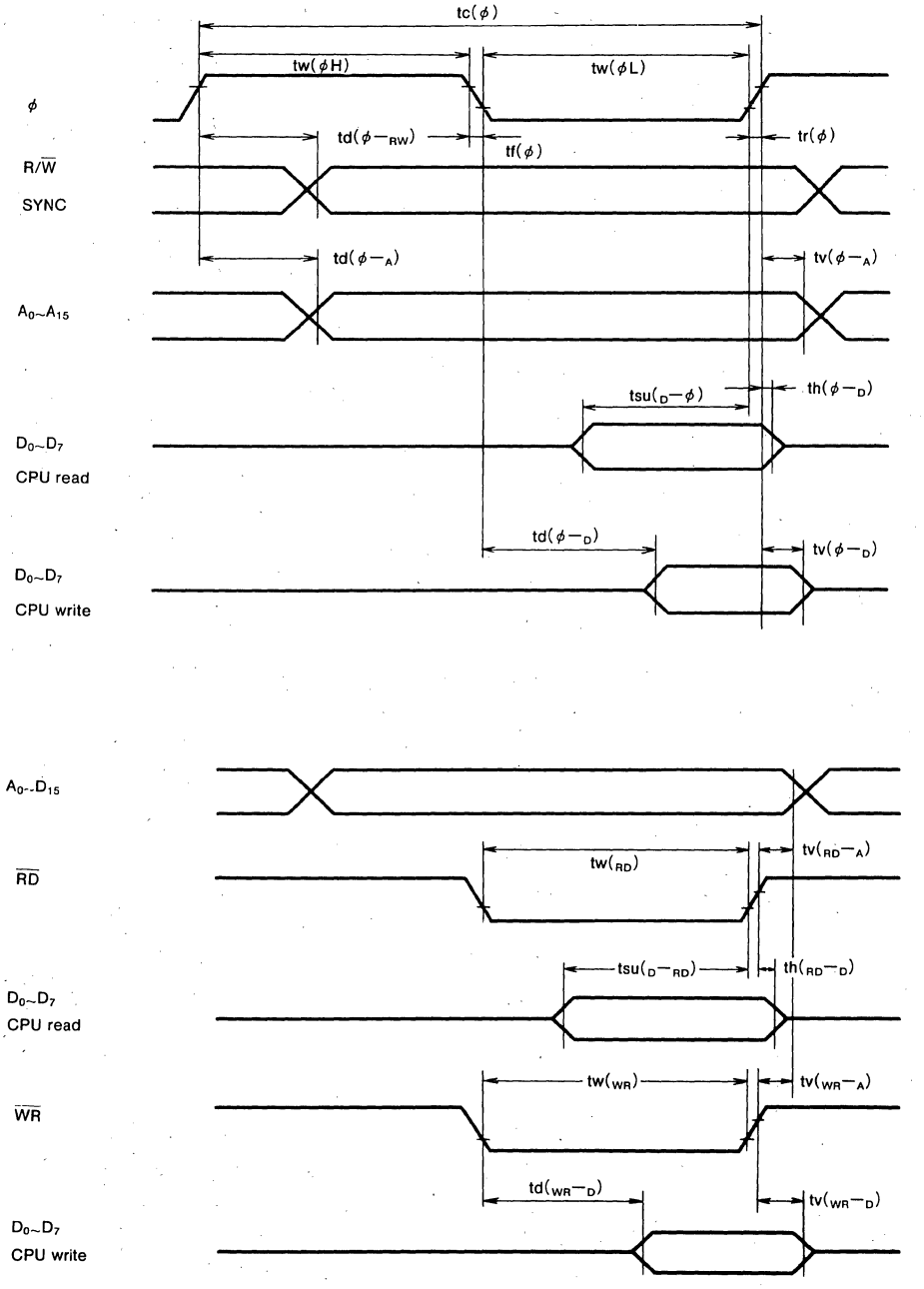
Write



Master CPU interface/ R/W type timing diagram



Local bus timing diagram



APPENDICES

SERIES MELPS 740 MASK ROM ORDERING METHOD

SERIES MELPS 740 MASK ROM ORDERING METHOD

Mitsubishi Electric corp. accepts order to transfer EPROM supplied program data into the mask ROM in single-chip 8-bit microcomputers.

When placing such order, please submit the information described below.

(1) Mask ROM confirmation form·····1 set
(There is a specific form to be used for each model.)

(2) Data to be written into mask ROM····· EPROM
(Please provide three sets containing the identical data.)

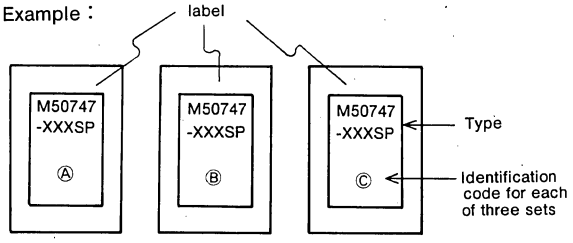
(3) Mark specification form·····1 set

NOTES

(1) Acceptable EPROM type
Any EPROM made by Mitsubishi that is listed in the mask ROM confirmation form may be used.

(2) EPROM window labeling
Please write the model name and the identification code (A, B, C) on the label for each of the three sets of data EPROMs provided.

Example :



(3) Calculation and indication of checksum code
Please calculate the total number of data in words in the EPROM, and write the number in 4-digit hexadecimal form in the checksum code field of the mask ROM confirmation form.

(4) Options
Refer to the appropriate data book entry and write the desired options on the mask ROM confirmation form.

(5) Mark specification method
The permissible mark specifications differ depending on the shape of package. Please fill out the mark specification form and attach it to the mask ROM confirmation form.

OUTLINE OF ORDER PROCESSING

Mitsubishi will produce the mask ROM if at least two of the three EPROM sets submitted contain identical data.

If we find error when the submitted EPROMs are compared, we will contact your representative.

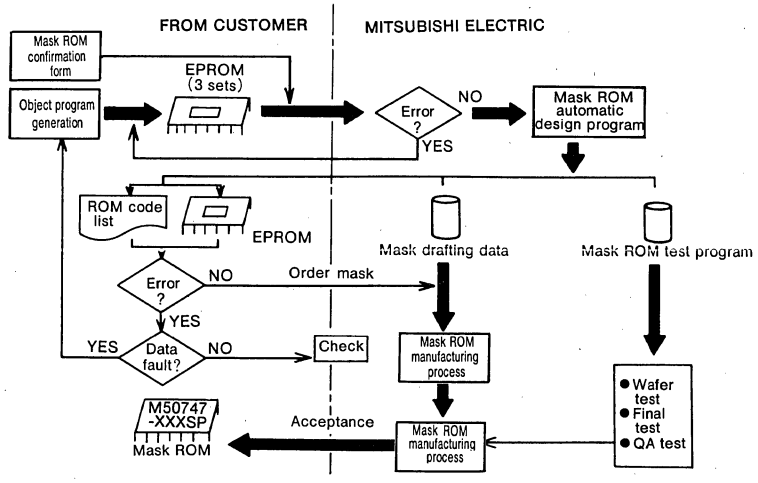
Thus, we assume responsibility only when we produce the mask ROM that contain data other than the data correctly provided by the customer.

Mitsubishi uses an automatic mask ROM design program to generated the following :

1. Drafting data for mask ROM production;
2. ROM code listing or EPROM for mask ROM production error check work;
3. Mask ROM test program.

The chart below shows the flow of mask ROM production.

SERIES MELPS 740 MASK ROM DEVELOPMENT CAD SYSTEM



SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—68A〈55B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50708-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

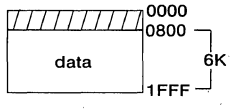
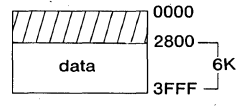
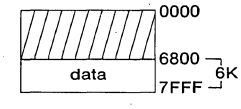
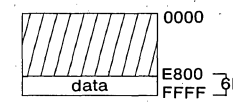
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50708-XXXSP ☐ M50708-XXXFP

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50708-XXXSP ; 72P6 for M50708-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—68A〈55B0〉

※4. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

$P0_0$	$P0_1$	$P0_2$	$P0_3$	$P0_4$	$P0_5$	$P0_6$	$P0_7$

※5. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

$P1_0$	$P1_1$	$P1_2$	$P1_3$	$P1_4$	$P1_5$	$P1_6$	$P1_7$

※6. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$

※7. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※8. Port P4 pull-down transistor (if built-in is desired write 1, if not write 0)

$P4_0$	$P4_1$	$P4_2$	$P4_3$	$P4_4$	$P4_5$	$P4_6$	$P4_7$

※9. Port P5 pull-up transistor (if built-in is desired write 1, if not write 0)

$P5_0$	$P5_1$	$P5_2$	$P5_3$	$P5_4$	$P5_5$	$P5_6$	$P5_7$

※10. Port P6 pull-up transistor (if built-in is desired write 1, if not write 0)

$P6_0$	$P6_1$	$P6_2$	$P6_3$	$P6_4$	$P6_5$	$P6_6$	$P6_7$

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—47A〈3XB0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50740A-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

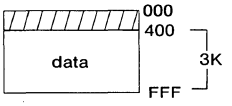
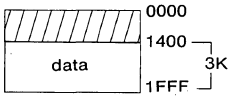
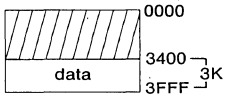
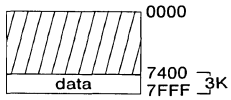
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50740A-XXXSP ☐ M50740A-XXXFP

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128	☐ 27256
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M50740A-XXXSP ; 50P6 for M50740A-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ—SH00—47A〈3XB0〉

※4. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

$P0_0$	$P0_1$	$P0_2$	$P0_3$	$P0_4$	$P0_5$	$P0_6$	$P0_7$

※5. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

$P1_0$	$P1_1$	$P1_2$	$P1_3$	$P1_4$	$P1_5$	$P1_6$	$P1_7$

※6. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$

※7. Port P3 pull-down transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※8. Port R I/O mode (if port R is to be used as an input port only write 1, otherwise 0. If the M50790P is to be connected, this entry must be 0.)

R

GZZ—SH00—41A〈32B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50741-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

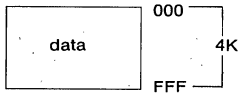
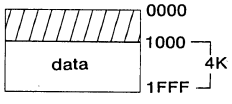
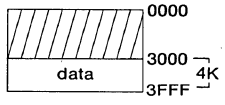
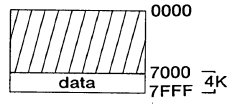
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50741-XXXSP ☐ M50741-XXXFP

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128	☐ 27256
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M50741-XXXSP ; 50P6 for M50741-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

MITSUBISHI ELECTRIC

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—54A〈3ZB0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50742-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
	Date issued	Date :			

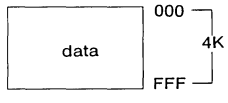
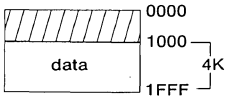
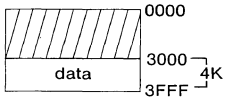
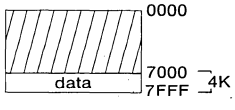
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50742-XXXSP ☐ M50742-XXXFP

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128	☐ 27256
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50742-XXXSP ; 72P6 for M50742-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ—SH00—54A〈3ZB0〉

※4. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

$P0_0$	$P0_1$	$P0_2$	$P0_3$	$P0_4$	$P0_5$	$P0_6$	$P0_7$

※5. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

$P1_0$	$P1_1$	$P1_2$	$P1_3$	$P1_4$	$P1_5$	$P1_6$	$P1_7$

※6. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$

※7. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※8. Port P4 pull-down transistor (if built-in is desired write 1, if not write 0)

$P4_0$	$P4_1$	$P4_2$	$P4_3$	$P4_4$	$P4_5$	$P4_6$	$P4_7$

※9. Port P5 pull-up transistor (if built-in is desired write 1, if not write 0)

$P5_0$	$P5_1$	$P5_2$	$P5_3$	$P5_4$	$P5_5$	$P5_6$	$P5_7$

※10. Port P6 pull-up transistor (if built-in is desired write 1, if not write 0)

$P6_0$	$P6_1$	$P6_2$	$P6_3$	$P6_4$	$P6_5$	$P6_6$	$P6_7$

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—61A〈4YB0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50743-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

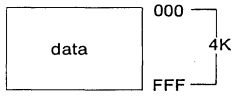
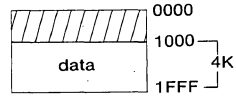
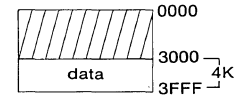
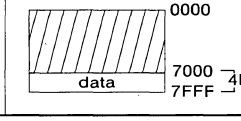
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50743-XXXSP ☐ M50743-XXXFP

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128	☐ 27256
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50743-XXXSP ; 72P6 for M50743-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—69A〈5XB0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50744-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

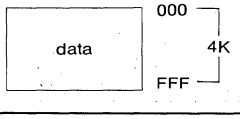
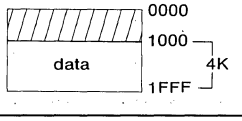
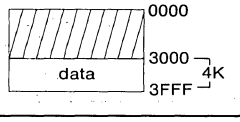
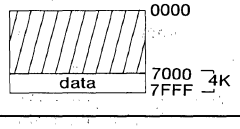
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50744-XXXSP ☐ M50744-XXXSP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128	☐ 27256
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50744-XXXSP ; 72P6 for M50744-XXXSP) and attach to the mask ROM confirmation form.

※3. Comments

※4. STP instruction option (if enable is desired write 1, if not write 0)

STP ☐

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—42A〈81A0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50744T-XXXSP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

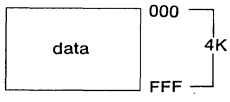
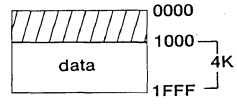
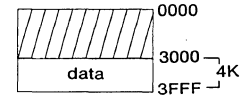
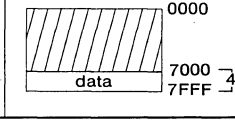
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50744T-XXXSP

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128	☐ 27256
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50744T-XXXSP) and attach to the mask ROM confirmation form.

※3. Comments

※4. STP instruction option (if enable is desired write 1, if not write 0)

STP ☐

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—46A〈37B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50745-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

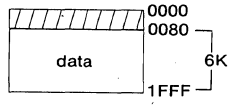
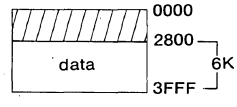
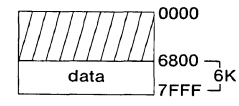
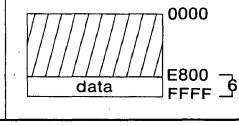
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50745-XXXSP ☐ M50745-XXXFP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50745-XXXSP ; 60P6 for M50745-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ—SH00—46A〈37B0〉

※4. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

$P0_0$	$P0_1$	$P0_2$	$P0_3$	$P0_4$	$P0_5$	$P0_6$	$P0_7$

※5. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

$P1_0$	$P1_1$	$P1_2$	$P1_3$	$P1_4$	$P1_5$	$P1_6$	$P1_7$

※6. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$

※7. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※8. Port P4 pull-down transistor (if built-in is desired write 1, if not write 0)

$P4_0$	$P4_1$	$P4_2$	$P4_3$	$P4_4$	$P4_5$	$P4_6$	$P4_7$

※9. Port P5 pull-up transistor (if built-in is desired write 1, if not write 0)

$P5_0$	$P5_1$	$P5_2$	$P5_3$	$P5_4$	$P5_5$	$P5_6$	$P5_7$

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—70A〈5XB0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50746-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

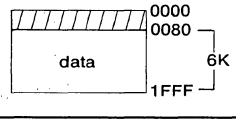
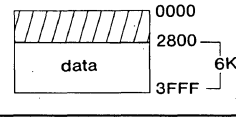
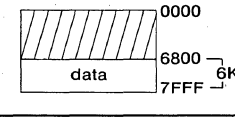
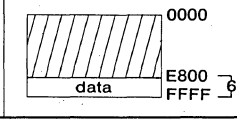
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50746-XXXSP ☐ M50746-XXXFP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50746-XXXSP ; 72P6 for M50746-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

※4. STP instruction option (if enable is desired write 1, if not write 0)

STP ☐

MITSUBISHI ELECTRIC

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—57A〈44B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50747-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

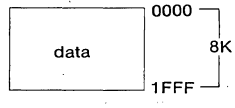
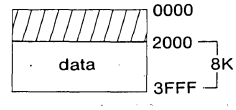
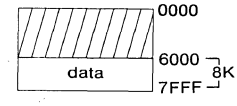
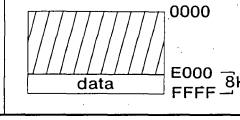
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50747-XXXSP ☐ M50747-XXXFP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50747-XXXSP ; 72P6 for M50747-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—27A〈7ZA0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50747H-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

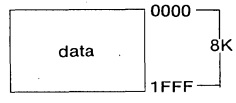
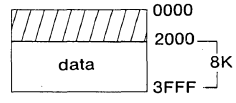
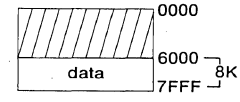
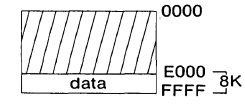
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50747H-XXXSP ☐ M50747H-XXXFP

Checksum code for entire EPROM areas [ ][ ][ ][ ] (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50747H-XXXSP ; 72P6 for M50747H-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—26A〈7ZA0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50747T-XXXSP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

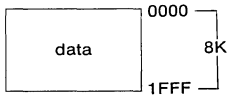
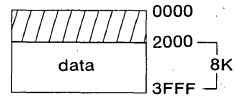
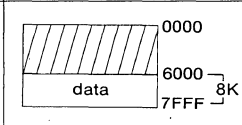
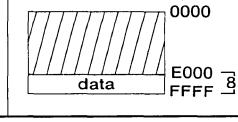
※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50747T-XXXSP) and attach to the mask ROM confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—65A〈52B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50752-XXXSP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

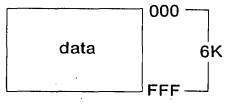
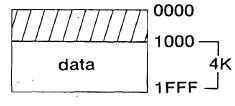
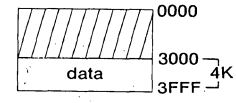
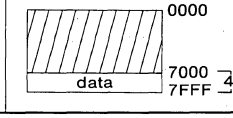
※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128	☐ 27256
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M50752-XXXSP) and attach to the mask ROM confirmation form.

※3. Comments

MITSUBISHI ELECTRIC

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—52A〈3ZB0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50753-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

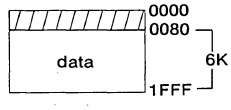
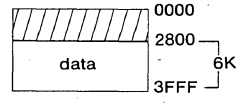
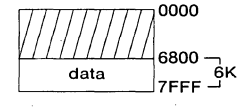
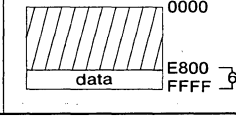
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50753-XXXSP ☐ M50753-XXXFP

Checksum code for entire EPROM areas [ ][ ][ ][ ] (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50753-XXXSP ; 60P6 for M50753-XXXFP) and attach to the mask ROM confirmation form.

※3. Commenis

GZZ—SH00—52A〈3ZB0〉

※4. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

$P0_0$	$P0_1$	$P0_2$	$P0_3$	$P0_4$	$P0_5$	$P0_6$	$P0_7$

※5. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

$P1_0$	$P1_1$	$P1_2$	$P1_3$	$P1_4$	$P1_5$	$P1_6$	$P1_7$

※6. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$

※7. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※8. Port P4 pull-down transistor (if built-in is desired write 1, if not write 0)

$P4_0$	$P4_1$	$P4_2$	$P4_3$

※9. Port PWM pull-up transistor (if built-in is desired write 1, if not write 0)

PWM

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—38A〈81A0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50753T-XXXSP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

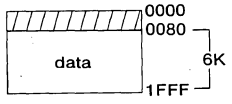
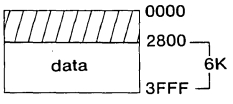
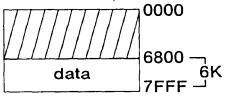
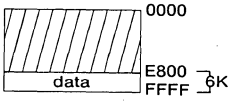
※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50753T-XXXSP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ—SH01—38A〈81A0〉

※4. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

$P0_0$	$P0_1$	$P0_2$	$P0_3$	$P0_4$	$P0_5$	$P0_6$	$P0_7$

※5. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

$P1_0$	$P1_1$	$P1_2$	$P1_3$	$P1_4$	$P1_5$	$P1_6$	$P1_7$

※6. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$

※7. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※8. Port P4 pull-down transistor (if built-in is desired write 1, if not write 0)

$P4_0$	$P4_1$	$P4_2$	$P4_3$

※9. Port PWM pull-up transistor (if built-in is desired write 1, if not write 0)

PWM

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—64A〈52B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50754-XXXSP/FP/GP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

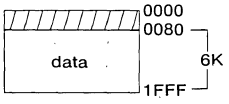
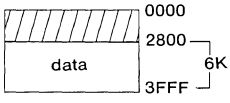
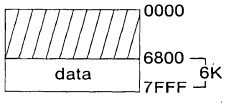
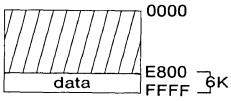
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50754-XXXSP ☐ M50754-XXXFP ☐ M50754-XXXGP

Checksum code for entire EPROM areas [ ][ ][ ][ ] (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50754-XXXSP ; 72P6 for M50754-XXXFP ; 64P6W for M50754-XXXGP) and attach to the mask ROM confirmation form.

※3. Comments

※4. ϕ output halt option (if output halt is desired write 1, if not write 0.)

PHI0 ☐

MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—60A〈44B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50757-XXXSP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

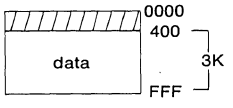
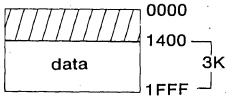
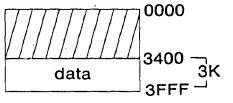
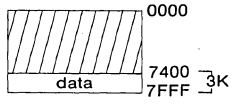
※ Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
	Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128	☐ 27256
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M50757-XXXSP) and attach to the mask ROM order confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—63A〈4ZB0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50758-XXXSP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

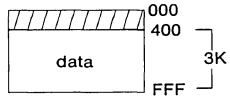
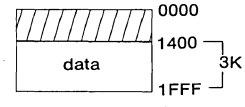
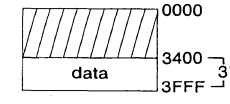
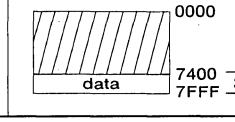
※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128	☐ 27256
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M50758-XXXSP) and attach to the mask ROM order confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—71A〈5XB0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50930-XXXFP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

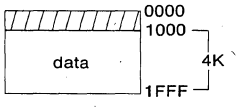
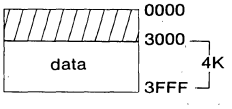
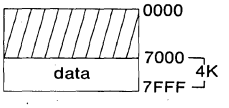
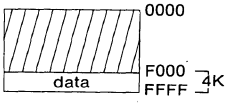
※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6 for M50930-XXXFP) and attach to the mask ROM order confirmation form.

※3. Comments

GZZ—SH00—71A〈5XB0〉

※4. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

$P0_0$	$P0_1$	$P0_2$	$P0_3$	$P0_4$	$P0_5$	$P0_6$	$P0_7$

※5. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

$P1_0$	$P1_1$	$P1_2$	$P1_3$	$P1_4$	$P1_5$	$P1_6$	$P1_7$

※6. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$

※7. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※8. Port $P3_5/S_{OUT}$ output type (if Nch open drain is desired write 1, if CMOS write 0)

S_{OUT}

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—37A〈81A0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50930T-XXXFP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

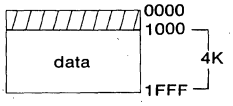
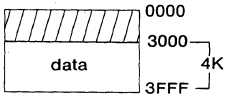
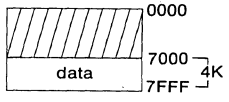
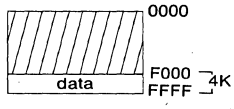
※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6 for M50930T-XXXFP) and attach to the mask ROM order confirmation form.

※3. Comments

GZZ—SH01—37A〈81A0〉

※4. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

$P0_0$	$P0_1$	$P0_2$	$P0_3$	$P0_4$	$P0_5$	$P0_6$	$P0_7$

※5. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

$P1_0$	$P1_1$	$P1_2$	$P1_3$	$P1_4$	$P1_5$	$P1_6$	$P1_7$

※6. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$

※7. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※8. Port $P3_5/S_{OUT}$ output type (if Nch open drain is desired write 1, if CMOS write 0)

S_{OUT}

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—17A〈7YA0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50931-XXXFP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

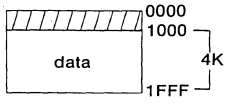
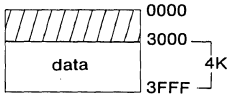
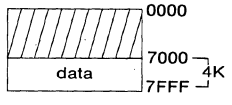
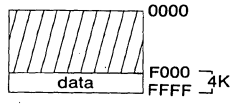
※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6 for M50931-XXXFP) and attach to the mask ROM order confirmation form.

※3. Comments

GZZ—SH01—17A〈7YA0〉

※4. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

$P0_0$	$P0_1$	$P0_2$	$P0_3$	$P0_4$	$P0_5$	$P0_6$	$P0_7$

※5. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

$P1_0$	$P1_1$	$P1_2$	$P1_3$	$P1_4$	$P1_5$	$P1_6$	$P1_7$

※6. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$

※7. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※8. Port $P3_5/S_{OUT}$ output type (if Nch open drain is desired write 1, if CMOS write 0)

S_{OUT}

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—88A〈72B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50932-XXXFP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

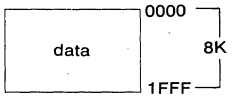
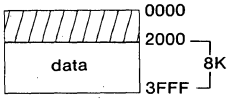
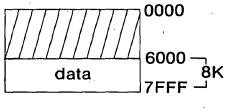
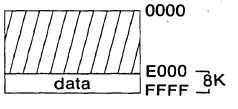
※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6 for M50932-XXXFP) and attach to the mask ROM order confirmation form.

※3. Comments

GZZ—SH00—88A〈72B0〉

※4. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

$P0_0$	$P0_1$	$P0_2$	$P0_3$	$P0_4$	$P0_5$	$P0_6$	$P0_7$

※5. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

$P1_0$	$P1_1$	$P1_2$	$P1_3$	$P1_4$	$P1_5$	$P1_6$	$P1_7$

※6. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$

※7. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※8. Port $P3_5/S_{OUT}$ output type (if Nch open drain is desired write 1, if CMOS write 0)

S_{OUT}

※9. CNTR pin pull-up transistor (if built-in is desired write 1, if not write 0)

CNTR

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—11A〈7YA0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50940-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

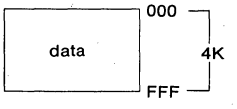
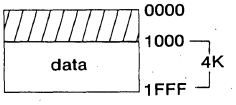
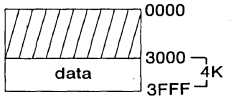
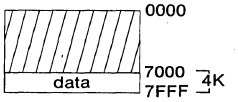
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50940-XXXSP ☐ M50940-XXXFP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128	☐ 27256
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50940-XXXSP ; 72P6 for M50940-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ—SH01—11A〈7YA0〉

※4. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※5. Port P4 pull-up transistor (if built-in is desired write 1, if not write 0)

$P4_0$	$P4_1$	$P4_2$	$P4_3$	$P4_4$	$P4_5$	$P4_6$	$P4_7$

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—10A〈7YA0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50941-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

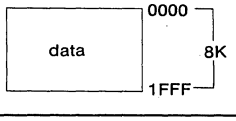
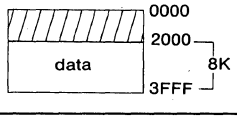
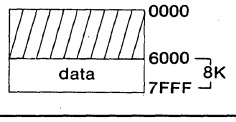
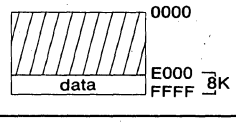
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50941-XXXSP ☐ M50941-XXXFP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50941-XXXSP ; 72P6 for M50941-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ—SH01—10A〈7YA0〉

※4. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※5. Port P4 pull-up transistor (if built-in is desired write 1, if not write 0)

$P4_0$	$P4_1$	$P4_2$	$P4_3$	$P4_4$	$P4_5$	$P4_6$	$P4_7$

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—12A〈7YA0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50943-XXXSP/FP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

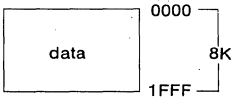
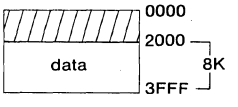
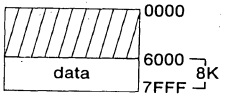
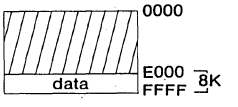
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50943-XXXSP ☐ M50943-XXXFP

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50943-XXXSP ; 60P6 for M50943-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ—SH01—12A〈7YA0〉

※4. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

$P0_0$	$P0_1$	$P0_2$	$P0_3$	$P0_4$	$P0_5$	$P0_6$	$P0_7$

※5. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

$P1_0$	$P1_1$	$P1_2$	$P1_3$	$P1_4$	$P1_5$	$P1_6$	$P1_7$

※6. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$

※7. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※8. Port P4 pull-up transistor (if built-in is desired write 1, if not write 0)

$P4_0$	$P4_1$	$P4_2$	$P4_3$

※9. Port PWM pull-up transistor (if built-in is desired write 1, if not write 0)

PWM

※10. Port CNTR pull-up transistor (if built-in is desired write 1, if not write 0)

CNTR

※11. Port $P3_5$ (S_{OUT}) output type (if Nch open drain is desired write 1, if CMOS write 0)

S_{OUT}

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—18A〈7YA0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50944-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
	Date issued	Date :			

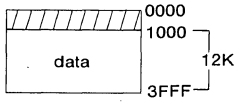
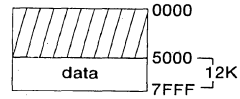
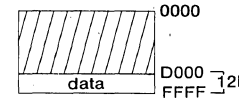
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50944-XXXSP ☐ M50944-XXXFP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50944-XXXSP ; 64P6S for M50944-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

GZZ—SH01—18A〈7YA0〉

※4. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

$P0_0$	$P0_1$	$P0_2$	$P0_3$	$P0_4$	$P0_5$	$P0_6$	$P0_7$

※5. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

$P1_0$	$P1_1$	$P1_2$	$P1_3$	$P1_4$	$P1_5$	$P1_6$	$P1_7$

※6. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

$P2_0$	$P2_1$	$P2_2$	$P2_3$	$P2_4$	$P2_5$	$P2_6$	$P2_7$

※7. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※8. Port P4 pull-up transistor (if built-in is desired write 1, if not write 0)

$P3_0$	$P3_1$	$P3_2$	$P3_3$	$P3_4$	$P3_5$	$P3_6$	$P3_7$

※9. Clock source option at reset (if X_{CIN} write 1, if X_{IN} write 0)

CLK

※10. STP instruction option (if enable is desired write 1, if not write 0)

STP

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—73A〈61B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50950-XXXSP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

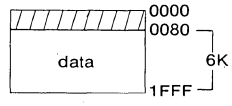
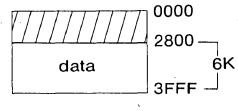
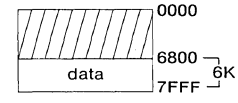
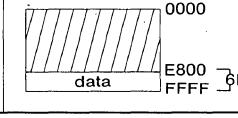
※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M50950-XXXSP) and attach to the mask ROM order confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—74A〈61B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50951-XXXSP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※

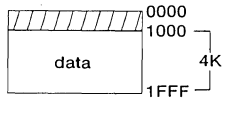
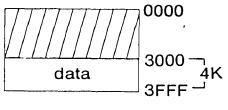
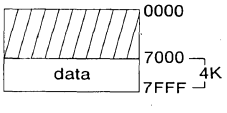
※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (52P4B for M50951-XXXSP) and attach to the mask ROM confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—13A〈7YA0〉

Mask ROM number	

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50954-XXXSP/FP/GP
MITSUBISHI ELECTRIC

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

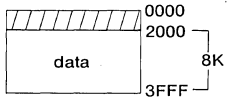
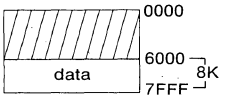
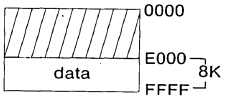
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50954-XXXSP ☐ M50954-XXXFP
☐ M50954-XXXGP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50954-XXXSP ; 72P6 for M50954-XXXFP ; 64P6W for M50954-XXXGP) and attach to the mask ROM confirmation form.

※3. Comments

※4. ϕ output halt option (if output halt is desired write 1, if not write 0.)

PHI0 ☐

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—14A〈7YA0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50955-XXXSP/FP/GP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

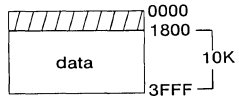
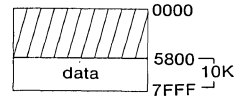
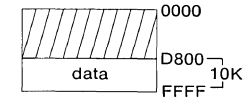
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50955-XXXSP ☐ M50955-XXXFP ☐ M50955-XXXGP

Checksum code for entire EPROM areas [ ][ ][ ][ ] (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50955-XXXSP ; 72P6 for M50955-XXXFP ; 64P6W for M50955-XXXGP) and attach to the mask ROM confirmation form.

※3. Comments

※4. ϕ output halt option (if output halt is desired write 1, if not write 0.)

PHI0 [ ]

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—15A〈7YA0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50957-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
	Date issued	Date :			

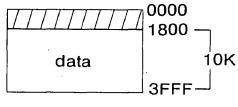
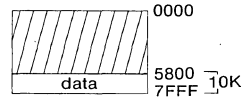
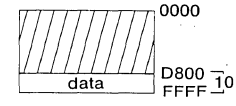
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50957-XXXSP ☐ M50957-XXXFP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50957-XXXSP ; 72P6 for M50957-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

※4. ϕ output halt option (if output halt is desired write 1, if not write 0.)

PHI0 ☐

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—19A〈7YA0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50959-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

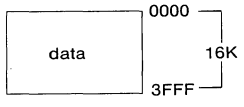
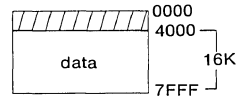
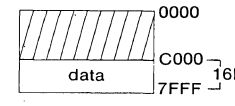
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50959-XXXSP ☐ M50959-XXXFP

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50959-XXXSP ; 72P6 for M50959-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

※4. ϕ output halt option (if output halt is desired write 1, if not write 0.)

PHI0 ☐

GZZ—SH00—85A〈71B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50963-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

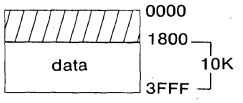
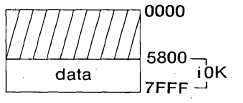
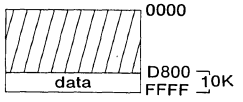
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50963-XXXSP ☐ M50963-XXXFP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50963-XXXSP ; 72P6 for M50963-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

※4. STP instruction option (if enable is desired write 1, if not write 0.)

STP ☐

MITSUBISHI ELECTRIC

GZZ—SH01—83A〈6ZB0〉

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M50964-XXXSP/FP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

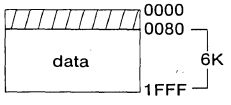
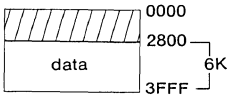
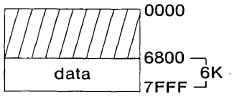
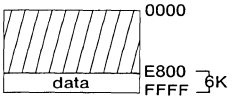
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M50964-XXXSP ☐ M50964-XXXFP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256	☐ 27512
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M50964-XXXSP ; 72P6 for M50964-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

※4. STP instruction option (if enable is desired write 1, if not write 0.)

STP ☐

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37410M3-XXXFP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

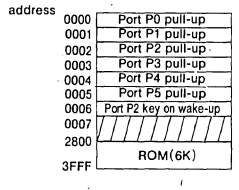
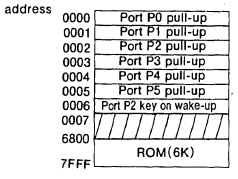
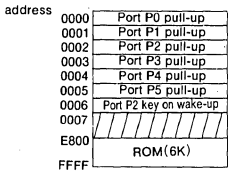
※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas [ ][ ][ ][ ] (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6S for M37410M3-XXXFP) and attach to the mask ROM order confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

Please write the option data also at the specified address in the EPROM

※1. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

	$P0_7$	$P0_6$	$P0_5$	$P0_4$	$P0_3$	$P0_2$	$P0_1$	$P0_0$
address 0000_{16}								

※2. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

	$P1_7$	$P1_6$	$P1_5$	$P1_4$	$P1_3$	$P1_2$	$P1_1$	$P1_0$
address 0001_{16}								

※3. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

	$P2_7$	$P2_6$	$P2_5$	$P2_4$	$P2_3$	$P2_2$	$P2_1$	$P2_0$
address 0002_{16}								

※4. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

	$P3_7$	$P3_6$	$P3_5$	$P3_4$	$P3_3$	$P3_2$	$P3_1$	$P3_0$
address 0003_{16}								

※5. Port P4 pull-up transistor (if built-in is desired write 1, if not write 0)

					$P4_3$	$P4_2$	$P4_1$	$P4_0$
address 0004_{16}	0	0	0					

※6. Port P5 pull-up transistor (if built-in is desired write 1, if not write 0)

	$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$
address 0005_{16}								

※7. Port P2 key on wake-up (if built-in is desired write 1, if not write 0)

	KW_7	KW_6	KW_5	KW_4	KW_3	KW_2	KW_1	KW_0
address 0006_{16}								

SERIES MELPS 740 MASK ROM ORDERING METHOD

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37410M4-XXXFP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※ Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor	
	Date issued	Date :				

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas [ ][ ][ ][ ] (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
address	address	address
0000 Port P0 pull-up	0000 Port P0 pull-up	0000 Port P0 pull-up
0001 Port P1 pull-up	0001 Port P1 pull-up	0001 Port P1 pull-up
0002 Port P2 pull-up	0002 Port P2 pull-up	0002 Port P2 pull-up
0003 Port P3 pull-up	0003 Port P3 pull-up	0003 Port P3 pull-up
0004 Port P4 pull-up	0004 Port P4 pull-up	0004 Port P4 pull-up
0005 Port P5 pull-up	0005 Port P5 pull-up	0005 Port P5 pull-up
0006 Port P2 key on wake-up	0006 Port P2 key on wake-up	0006 Port P2 key on wake-up
0007	0007	0007
2000 ROM(8K) 3FFF	6000 ROM(8K) 7FFF	E000 ROM(8K) FFFF

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6S for M37410M4-XXXFP) and attach to the mask ROM order confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

Please write the option data also at the specified address in the EPROM

※1. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

address 0000_{16}

$P0_7$	$P0_6$	$P0_5$	$P0_4$	$P0_3$	$P0_2$	$P0_1$	$P0_0$

※2. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

address 0001_{16}

$P1_7$	$P1_6$	$P1_5$	$P1_4$	$P1_3$	$P1_2$	$P1_1$	$P1_0$

※3. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

address 0002_{16}

$P2_7$	$P2_6$	$P2_5$	$P2_4$	$P2_3$	$P2_2$	$P2_1$	$P2_0$

※4. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

address 0003_{16}

$P3_7$	$P3_6$	$P3_5$	$P3_4$	$P3_3$	$P3_2$	$P3_1$	$P3_0$

※5. Port P4 pull-up transistor (if built-in is desired write 1, if not write 0)

address 0004_{16}

				$P4_3$	$P4_2$	$P4_1$	$P4_0$
0	0	0	0				

※6. Port P5 pull-up transistor (if built-in is desired write 1, if not write 0)

address 0005_{16}

$P5_7$	$P5_6$	$P5_5$	$P5_4$	$P5_3$	$P5_2$	$P5_1$	$P5_0$

※7. Port P2 key on wake-up (if built-in is desired write 1, if not write 0)

address 0006_{16}

KW_7	KW_6	KW_5	KW_4	KW_3	KW_2	KW_1	KW_0

SERIES MELPS 740 MASK ROM ORDERING METHOD

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37415M4-XXXFP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

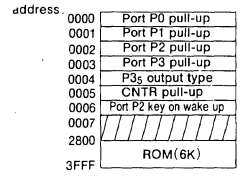
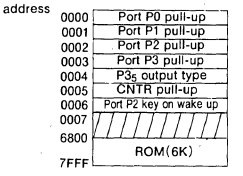
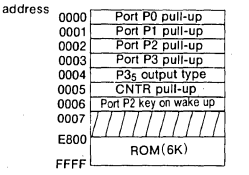
※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas [ ][ ][ ][ ] (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256	☐ 27512
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (80P6 for M37415M4-XXXFP) and attach to the mask ROM order confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

Please write the option data also at the specified address in the EPROM

※1. Port P0 pull-up transistor (if built-in is desired write 1, if not write 0)

	$P0_7$	$P0_6$	$P0_5$	$P0_4$	$P0_3$	$P0_2$	$P0_1$	$P0_0$
address 0000_{16}								

※2. Port P1 pull-up transistor (if built-in is desired write 1, if not write 0)

	$P1_7$	$P1_6$	$P1_5$	$P1_4$	$P1_3$	$P1_2$	$P1_1$	$P1_0$
address 0001_{16}								

※3. Port P2 pull-up transistor (if built-in is desired write 1, if not write 0)

	$P2_7$	$P2_6$	$P2_5$	$P2_4$	$P2_3$	$P2_2$	$P2_1$	$P2_0$
address 0002_{16}								

※4. Port P3 pull-up transistor (if built-in is desired write 1, if not write 0)

	$P3_7$	$P3_6$	$P3_5$	$P3_4$	$P3_3$	$P3_2$	$P3_1$	$P3_0$
address 0003_{16}								

※5. Port $P3_5$ output type (if Nch open drain is desired write 1, if CMOS write 0)

								$P3_5$
address 0004_{16}	0	0	0	0	0	0	0	

※6. CNTR pin pull-up transistor (if built-in is desired write 1, if not write 0)

								CNTR
address 0005_{16}	0	0	0	0	0	0	0	

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—95A〈75B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37450M2-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

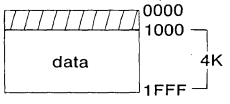
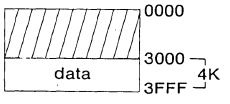
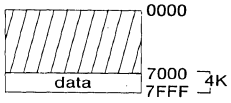
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37450M2-XXXSP ☐ M37450M2-XXXFP

Checksum code for entire EPROM areas [ ][ ][ ][ ] (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37450M2-XXXSP ; 80P6 for M37450M2-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH00—99A〈75B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37450M4-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

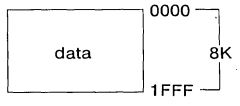
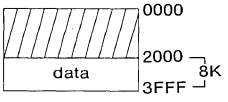
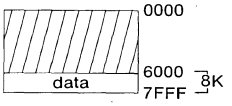
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37450M4-XXXSP ☐ M37450M4-XXXFP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 2764	☐ 27128	☐ 27256
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37450M4-XXXSP ; 80P6 for M37450M4-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

SERIES MELPS 740 MASK ROM ORDERING METHOD

GZZ—SH01—00A〈76B0〉

SERIES MELPS 740 MASK ROM CONFIRMATION FORM
SINGLE-CHIP MICROCOMPUTER M37450M8-XXXSP/FP
MITSUBISHI ELECTRIC

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

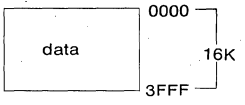
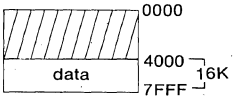
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M37450M8-XXXSP ☐ M37450M8-XXXFP

Checksum code for entire EPROM areas | | | | | (hexadecimal notation)

EPROM type

☐ 27128	☐ 27256
	

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (64P4B for M37450M8-XXXSP ; 80P6 for M37450M8-XXXFP) and attach to the mask ROM confirmation form.

※3. Comments

SERIES MELPS 8-48 and MELPS 8-41 MASK ROM ORDERING METHOD

SERIES MELPS 8-48 AND MELPS 8-41 MASK ROM ORDERING METHOD

Mitsubishi Electric corp. accepts order to transfer EPROM supplied program data into the mask ROM in single-chip 8-bit microcomputers.

When placing such order, please submit the information described below.

(1) Mask ROM confirmation form ..... 1 set
(There is a specific form to be used for each model.)

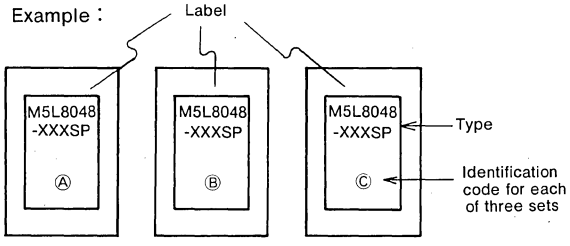
(2) Data to be written into mask ROM ..... EPROM
(Please provide three sets containing the identical data.)

(3) Mark specification form ..... 1 set

NOTES

(1) Acceptable EPROM type
Any EPROM made by Mitsubishi that is listed in the mask ROM confirmation form may be used.

(2) EPROM window labeling
Please write the model name and the identification code (A, B, C) on the label for each of the three sets of data EPROMs provided.



(3) Calculation and indication of checksum code
Please calculate the total number of data in words in the EPROM, and write the number in 4-digit hexadecimal form in the checksum code field of the mask ROM order confirmation form.

(4) Options
Refer to the appropriate data book entry and write the desired options on the mask ROM order confirmation form.

(5) Mark specification method
The permissible mark specifications differ depending on the shape of package. Please fill out the mark specification form and attach it to the mask ROM confirmation form.

OUTLINE OF ORDER PROCESSING

Mitsubishi will produce the mask ROM if at least two of the three EPROM sets submitted contain identical data.

If we find error when the submitted EPROMs are compared, we will contact your representative.

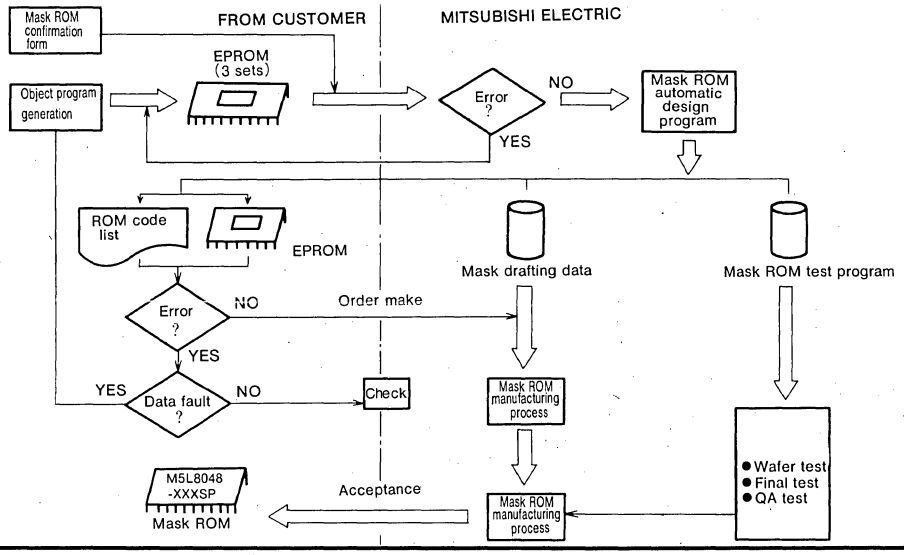
Thus, we assume responsibility only when we produce the mask ROM that contain data other than the data correctly provided by the customer.

Mitsubishi uses an automatic mask ROM design program to generated the following :

1. Drafting data for mask ROM production;
2. ROM code listing or EPROM for mask ROM production error check work;
3. Mask ROM test program.

The chart below shows the flow of mask ROM production.

SERIES MELPS 8-48 AND MELPS 8-41 MASK ROM DEVELOPMENT CAD SYSTEM



SERIES MELPS 8-48 and MELPS 8-41 MASK ROM ORDERING METHOD

GZZ—SH01—21A〈7ZA0〉

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

SERIES MELPS 8-48 and MELPS 8-41 MASK ROM CONFIRMATION FORM
SINGLE-CHIP 8-BIT MICROCOMPUTER
M5L8048-XXXP
M5L8041A-XXXP
M5L8041AH-XXXP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked※.

					Issuance signature	Responsible officer	Supervisor
※	Customer	Company name	TEL ( )				
		Date issued	Date :				

※1. Confirmation

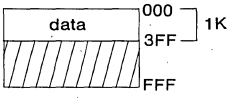
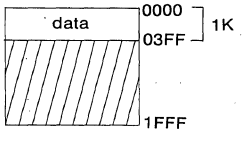
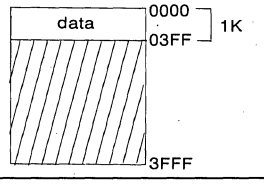
Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name :

- ☐ M5L8048-XXXP
- ☐ M5L8041A-XXXP
- ☐ M5L8041AH-XXXP

Checksum code for entire EPROM areas ☐☐☐☐ (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128	☐ 8741 ☐ 8741A ☐ 8748 ☐ 8748H
			

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (40P4) and attach to the mask ROM confirmation form.

※3. Outline of the final products (Please enter as far as to be allowed)

※4. Comments

SERIES MELPS 8-48 and MELPS 8-41 MASK ROM ORDERING METHOD

GZZ—SH01—22A〈7ZA0〉

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

SERIES MELPS 8-48 and MELPS 8-41 MASK ROM CONFIRMATION FORM
SINGLE-CHIP 8-BIT MICROCOMPUTER
M5L8042-XXXP
M5L8049-XXXP, M5L8049-XXXP-6
M5L8049H1-XXXP
M5M80C49A-XXXP, M5M80C49H-XXXP
M5MC49A-XXXFP, M5MC49H-XXXFP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked※.

※	Customer	Company name	TEL ( )	Issuance signature	Responsible officer	Supervisor
		Date issued	Date :			

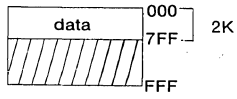
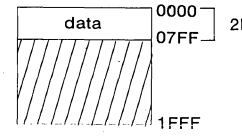
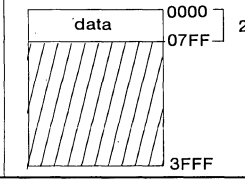
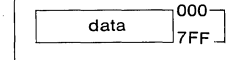
※1. Confirmation
Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name :

- ☐ M5L8042-XXXP
- ☐ M5L8049-XXXP
- ☐ M5L8049-XXXP-6
- ☐ M5L8049H1-XXXP
- ☐ M5M80C49A-XXXP
- ☐ M5M80C49H-XXXP
- ☐ M5MC49A-XXXFP
- ☐ M5MC49H-XXXFP

Checksum code for entire EPROM areas [ ][ ][ ][ ] (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128	☐ 8742 ☐ 8749 ☐ 8749H
			

Set "FF_{16}" in the shaded area.

※2. Mark specification
Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (42P6 for M5MC49A-XXXFP and M5MC49H-XXXFP, and 40P4 for other type) and attach to the mask ROM confirmation form.

※3. Outline of the final products (Please enter as far as to be allowed)

※4. Comments

SERIES MELPS 8-48 and MELPS 8-41 MASK ROM ORDERING METHOD

GZZ—SH01—23A〈7ZA0〉

Mask ROM number	

Receipt	Date :	
	Section head signature	Supervisor signature

SERIES MELPS 8-48 and MELPS 8-41 MASK ROM CONFIRMATION FORM
SINGLE-CHIP 8-BIT MICROCOMPUTER
M5M8050H-XXXP
M5M8050L-XXXP
MITSUBISHI ELECTRIC

Note : Please fill in all items marked※.

					Issuance signature	Responsible officer	Supervisor
※	Customer	Company name		TEL ( )			
		Date issued	Date :				

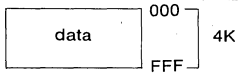
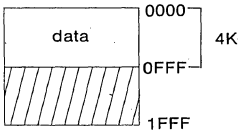
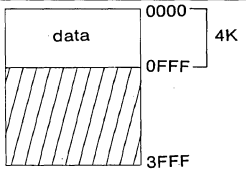
※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.
Three sets of EPROMs are required for each pattern (Check @ in the appropriate box).
If at least two of the three sets of EPROMs submitted contain the identical data, we will produce masks based in this data. We shall assume the responsibility for errors only if the mask ROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Microcomputer name : ☐ M5M8050HXXXP ☐ M5M8050L-XXXP

Checksum code for entire EPROM areas [ ][ ][ ][ ] (hexadecimal notation)

EPROM type

☐ 2732	☐ 2764	☐ 27128
		

Set "FF_{16}" in the shaded area.

※2. Mark specification

Mark specification must be submitted using the correct form for the type package being ordered fill out the appropriate mark specification form (40P4) and attach to the mask ROM confirmation form.

※3. Outline of the final products (Please enter as far as to be allowed)

※4. Comments

MARK SPECIFICATION FORM

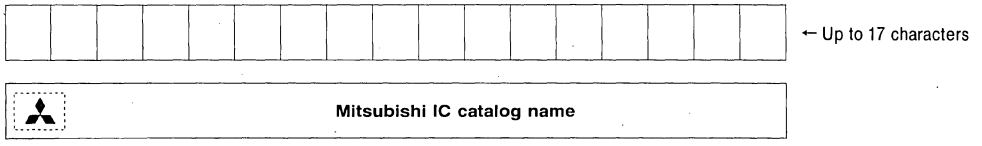
MARK SPECIFICATION FORM

Mark specification form differs depending on the package type. Fill out the mark specification form for the package type being ordered, and submit the form with the mask ROM confirmation form.

40P4 (40-PIN DIP) MARK SPECIFICATION FORM

1. Standard Mitsubishi mark
2. Standard mark+Customer's parts number
3. Special mark required

For 2 :



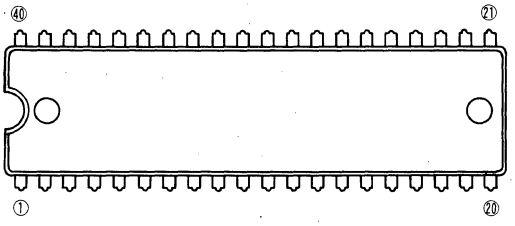
2-a. Mitsubishi logo required
2-b. Mitsubishi logo not required

Note 1 : The mark field should be written to the right.
2 : The identification mark can be up to 17 alphanumeric characters (except J, I and O) and hyphens.

For 3 :

Note 3 : If the special character fonts (ex. customer's trademark logo) must be used in special mark, a clean font original (ideally a logo drawing) must be submitted.

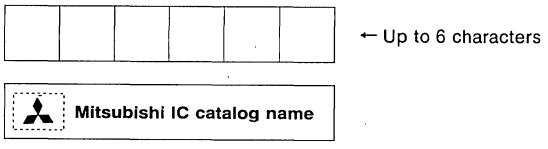
4 : If special mark is to be printed, indicate the desired layout on the package drawing below. The layout will be duplicated as closely as technically possible.



42P6 (42-PIN QFP) MARK SPECIFICATION FORM

1. Standard Mitsubishi mark
2. Standard mark+Customer's parts number
3. Special mark required

For 2 :



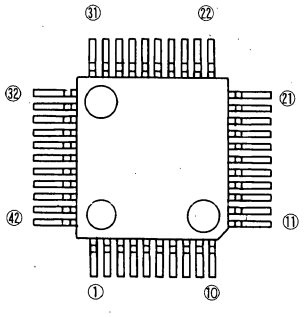
2-a. Mitsubishi logo required
2-b. Mitsubishi logo not required

Note 1 : The mark field should be written to the right.
2 : The identification mark can be up to 6 alphanumeric characters (except J, I and O) and hyphens.

For 3 :

Note 3 : If the special character fonts (ex. customer's trademark logo) must be used in special mark, a clean font original (ideally a logo drawing) must be submitted.

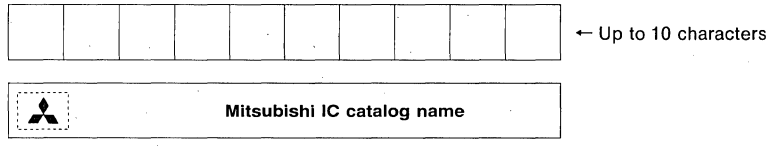
4 : If special mark is to be printed, indicate the desired layout on the package drawing below. The layout will be duplicated as closely as technically possible.



50P6 (50-PIN QFP) MARK SPECIFICATION FORM

1. Standard Mitsubishi mark
2. Standard mark+Customer's parts number
3. Special mark required

For 2 :



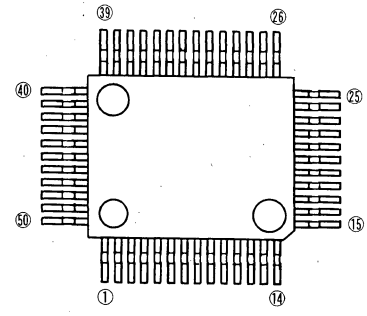
2-a. Mitsubishi logo required
2-b. Mitsubishi logo not required

Note 1 : The mark field should be written to the right.
2 : The identification mark can be up to 10 alphanumeric characters (except J, I and O) and hyphens.

For 3 :

Note 3 : If the special character fonts (ex. customer's trademark logo) must be used in special mark, a clean font original (ideally a logo drawing) must be submitted.

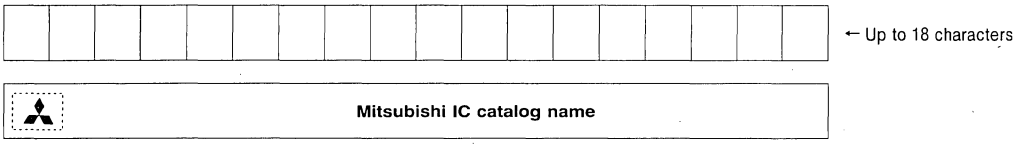
4 : If special mark is to be printed, indicate the desired layout on the package drawing below. The layout will be duplicated as closely as technically possible.



52P4B (52-PIN SHRINK DIP) MARK SPECIFICATION FORM

1. Standard Mitsubishi mark
2. Standard mark+Customer's parts number
3. Special mark required

For 2 :



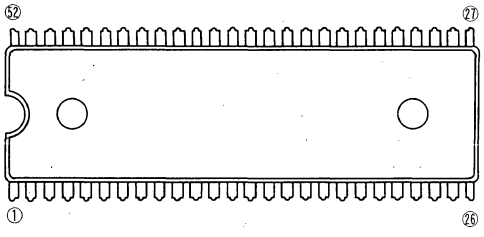
2-a. Mitsubishi logo required
2-b. Mitsubishi logo not required

Note 1 : The mark field should be written to the right.
2 : The identification mark can be up to 18 alphanumeric characters (except J, I and O) and hyphens.

For 3 :

Note 3 : If the special character fonts (ex. customer's trademark logo) must be used in special mark, a clean font original (ideally a logo drawing) must be submitted.

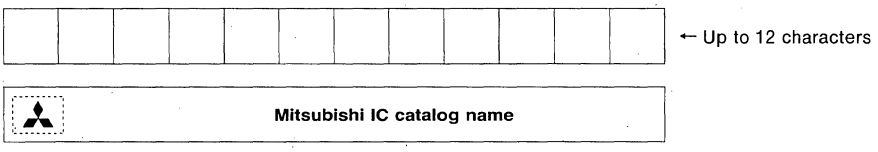
4 : If special mark is to be printed, indicate the desired layout on the package drawing below. The layout will be duplicated as closely as technically possible.



60P6 (60-PIN QFP) MARK SPECIFICATION FORM

1. Standard Mitsubishi mark
2. Standard mark+Customer's parts number
3. Special mark required

For 2 :



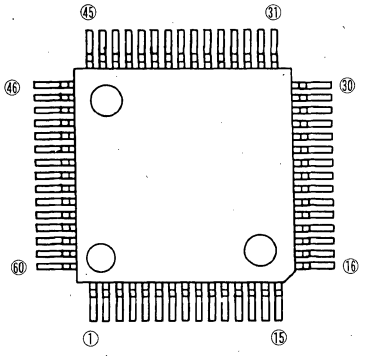
2-a. Mitsubishi logo required
2-b. Mitsubishi logo not required

Note 1 : The mark field should be written to the right.
2 : The identification mark can be up to 12 alphanumeric characters (except J, I and O) and hyphens.

For 3 :

Note 3 : If the special character fonts (ex. customer's trademark logo) must be used in special mark, a clean font original (ideally a logo drawing) must be submitted.

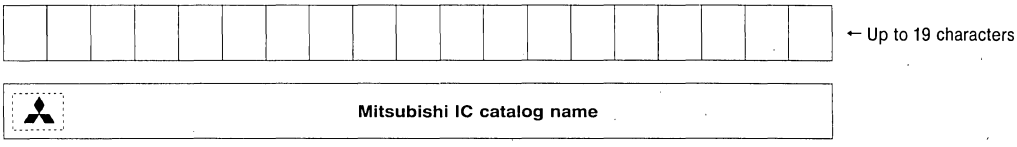
4 : If special mark is to be printed, indicate the desired layout on the package drawing below. The layout will be duplicated as closely as technically possible.



64P4B (64-PIN SHRINK DIP) MARK SPECIFICATION FORM

1. Standard Mitsubishi mark
2. Standard mark+Customer's parts number
3. Special mark required

For 2 :



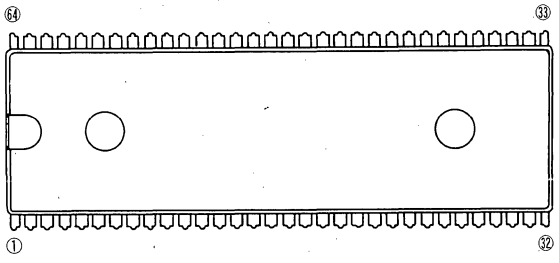
2-a. Mitsubishi logo required
2-b. Mitsubishi logo not required

Note 1 : The mark field should be written to the right.
2 : The identification mark can be up to 19 alphanumeric characters (except J, I and O) and hyphens.

For 3 :

Note 3 : If the special character fonts (ex. customer's trademark logo) must be used in special mark, a clean font original (ideally a logo drawing) must be submitted.

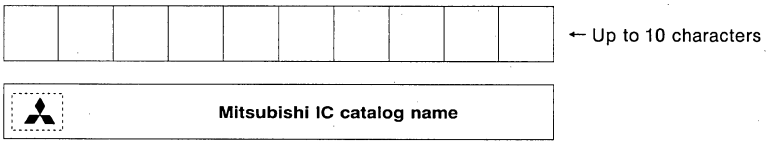
4 : If special mark is to be printed, indicate the desired layout on the package drawing below. The layout will be duplicated as closely as technically possible.



64P6S (64-PIN QFP) MARK SPECIFICATION FORM

1. Standard Mitsubishi mark
2. Standard mark+Customer's parts number
3. Special mark required

For 2 :



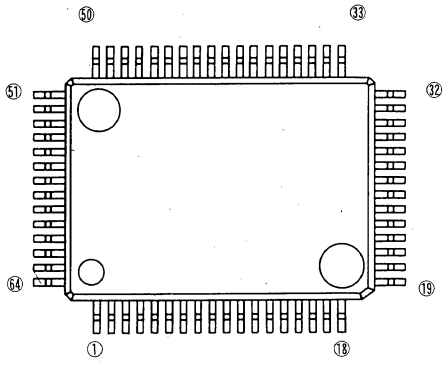
2-a. Mitsubishi logo required
2-b. Mitsubishi logo not required

Note 1 : The mark field should be written to the right.
2 : The identification mark can be up to 10 alphanumeric characters (except J, I and O) and hyphens.

For 3 :

Note 3 : If the special character fonts (ex. customer's trademark logo) must be used in special mark, a clean font original (ideally a logo drawing) must be submitted.

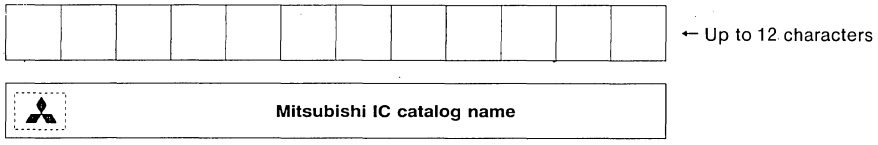
4 : If special mark is to be printed, indicate the desired layout on the package drawing below. The layout will be duplicated as closely as technically possible.



64P6W (64-PIN QFP) MARK SPECIFICATION FORM

1. Standard Mitsubishi mark
2. Standard mark+Customer's parts number
3. Special mark required

For 2 :



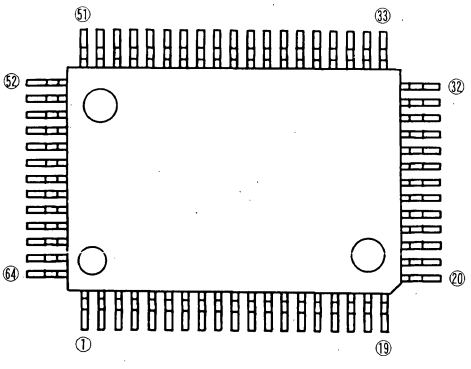
2-a. Mitsubishi logo required
2-b. Mitsubishi logo not required

Note 1 : The mark field should be written to the right.
2 : The identification mark can be up to 12 alphanumeric characters (except J, I and O) and hyphens.

For 3 :

Note 3 : If the special character fonts (ex. customer's trademark logo) must be used in special mark, a clean font original (ideally a logo drawing) must be submitted.

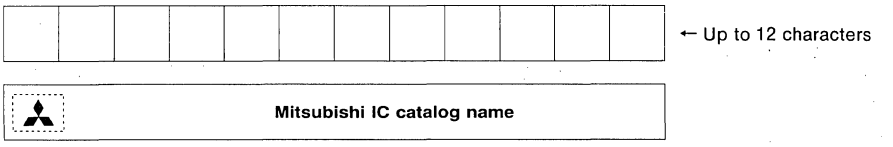
4 : If special mark is to be printed, indicate the desired layout on the package drawing below. The layout will be duplicated as closely as technically possible.



72P6 (72-PIN QFP) MARK SPECIFICATION FORM

1. Standard Mitsubishi mark
2. Standard mark+Customer's parts number
3. Special mark required

For 2 :



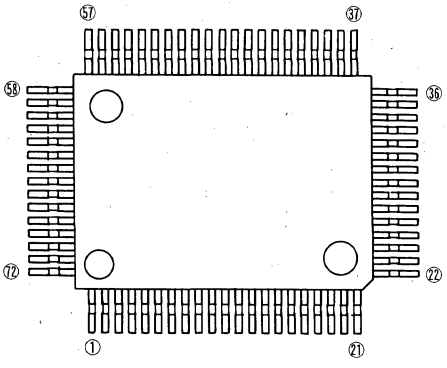
2-a. Mitsubishi logo required
2-b. Mitsubishi logo not required

Note 1 : The mark field should be written to the right.
2 : The identification mark can be up to 12 alphanumeric characters (except J, I and O) and hyphens.

For 3 :

Note 3 : If the special character fonts (ex. customer's trademark logo) must be used in special mark, a clean font original (ideally a logo drawing) must be submitted.

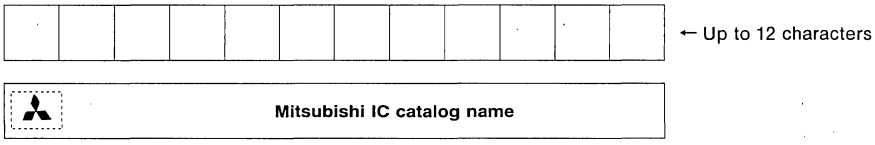
4 : If special mark is to be printed, indicate the desired layout on the package drawing below. The layout will be duplicated as closely as technically possible.



80P6 (80-PIN QFP) MARK SPECIFICATION FORM

1. Standard Mitsubishi mark
2. Standard mark+Customer's parts number
3. Special mark required

For 2 :



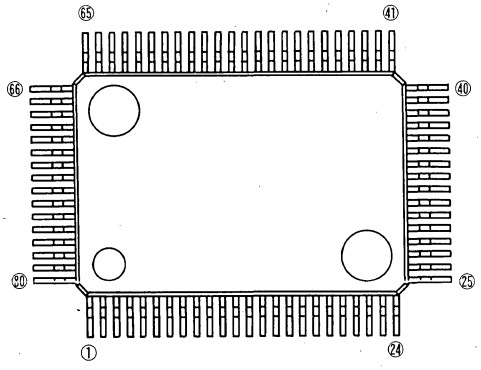
2-a. Mitsubishi logo required
2-b. Mitsubishi logo not required

Note 1 : The mark field should be written to the right.
2 : The identification mark can be up to 12 alphanumeric characters (except J, I and O) and hyphens.

For 3 :

Note 3 : If the special character fonts (ex. customer's trademark logo) must be used in special mark, a clean font original (ideally a logo drawing) must be submitted.

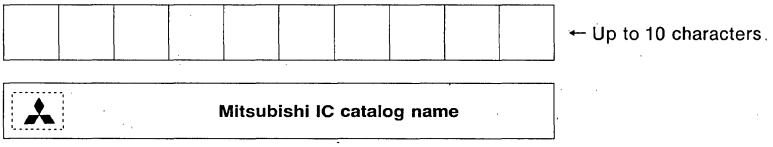
4 : If special mark is to be printed, indicate the desired layout on the package drawing below. The layout will be duplicated as closely as technically possible.



80P6S (80-PIN QFP) MARK SPECIFICATION FORM

1. Standard Mitsubishi mark
2. Standard mark+Customer's parts number
3. Special mark required

For 2 :



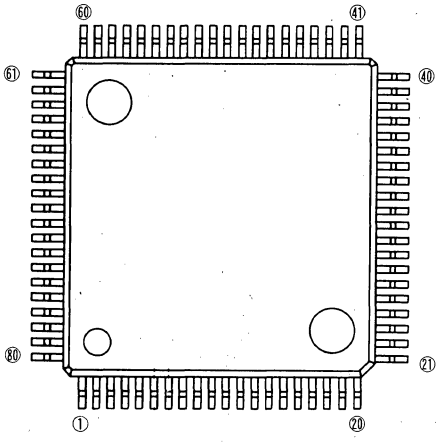
2-a. Mitsubishi logo required
2-b. Mitsubishi logo not required

Note 1 : The mark field should be written to the right.
2 : The identification mark can be up to 10 alphanumeric characters (except J, I and O) and hyphens.

For 3 :

Note 3 : If the special character fonts (ex. customer's trademark logo) must be used in special mark, a clean font original (ideally a logo drawing) must be submitted.

4 : If special mark is to be printed, indicate the desired layout on the package drawing below. The layout will be duplicated as closely as technically possible.



CONTACT ADDRESSES FOR FURTHER INFORMATION

JAPAN

Semiconductor Marketing Division
Mitsubishi Electric Corporation
2-3, Marunouchi 2-chome
Chiyoda-ku, Tokyo 100, Japan
Telex: 24532 MELCO J
Telephone: (03) 218-3473
(03) 218-3499
Facsimile: (03) 214-5570

Overseas Marketing Manager
Kita-Itami Works
4-1, Mizuhara, Itami-shi,
Hyogo-ken 664, Japan
Telex: 526408 KMELCO J
Telephone: (0727) 82-5131
Facsimile: (0727) 72-2329

HONG KONG

MITSUBISHI ELECTRIC (H.K.) LTD.
25 Floor, Leighton Centre,
77, Leighton Road. Causeway Bay.
Hong Kong
Telex: 60800 MELCO HX
Telephone: (5) 773901-3
Facsimile: (852) 123-4345

SINGAPORE

MELCO SALES SINGAPORE PTE. LTD.
230 Upper Bukit Timah Road #03-01/15
Hock Soon Industrial Complex
Singapore 2158
Telex: RS 20845 MELCO
Telephone: 4695255
Facsimile: 4695347

TAIWAN

MELCO-TAIWAN CO., Ltd.
1st fl., Chung-Ling Bldg.,
363, Sec. 2, Fu-Hsing S Road,
Taipei R.O.C.
Telephone: (02) 735-3030
Facsimile: (02) 735-6771
Telex: 25433 CHURYO "MELCO-TAIWAN"

U.S.A.

NORTHWEST
Mitsubishi Electronics America, Inc.
1050 East Arques Avenue
Sunnyvale, CA 94086, U.S.A.
Telex: 172296 MELA SUVL
Twx: 910-339-9549
Telephone: (408) 730-5900
Facsimile: (408) 730-4972

SOUTHWEST
Mitsubishi Electronics America, Inc.
991 Knox Street
Torrance, CA 90502, U.S.A.
Telex: 664787 MELA TRNC
Telephone: (213) 515-3993
Facsimile: (213) 324-6578

SOUTH CENTRAL
Mitsubishi Electronics America, Inc.
2105 Luna Road, Suite 320
Carrollton, TX 75006, U.S.A.
Telephone: (214) 484-1919
Facsimile: (214) 243-0207

NORTHERN
Mitsubishi Electronics America, Inc.
15612 Highway 7 #243
Minnetonka, MN 55345, U.S.A.
Telex: 291115 MELA MTKA
Telephone: (612) 938-7779
Facsimile: (612) 938-5125

NORTH CENTRAL
Mitsubishi Electronics America, Inc.
800 N. Bierman Circle
Mt. Prospect, IL 60056, U.S.A.
Telex: 270636 MESA CHIMPCT
Telephone: (312) 298-9223
Facsimile: (312) 298-0567

NORTHEAST
Mitsubishi Electronics America, Inc.
200 Unicorn Park Drive
Woburn, MA 01801, U.S.A.
Telex: 951796 MELA WOBN
Twx: 710-348-1229
Telephone: (617) 938-1220
Facsimile: (617) 938-1075

MID ATLANTIC
Mitsubishi Electronics America, Inc.
45 Knightsbridge Road Piscataway,
NJ 08854, U.S.A.
Telephone: (201) 981-1001
Facsimile: (201) 981-1218

SOUTH ATLANTIC
Mitsubishi Electronics America, Inc.
6100 Atlantic Blvd.
P.O. Box 2447
Norcross, GA 30091
Telephone: (404) 368-4850
Facsimile: (404) 662-5206

SOUTHEAST
Mitsubishi Electronics America, Inc.
Town Executive Center
6100 Glades Road #210
Boca Raton, FL 33433, U.S.A.
Twx: 510-953-7608
Telephone: (305) 487-7747
Facsimile: (305) 487-2046

WEST GERMANY

Mitsubishi Electric Europe GmbH
Headquarters:
Gothear Str. 6
4030 Ratingen 1, West Germany
Telex: 8585070 MED D
Telephone: (02102) 4860
Facsimile: (02102) 486-115

Munich Office:
Arabellastraße 31
8000 München 81, West Germany
Telex: 5214820
Telephone: (089) 919006-09
Facsimile: (089) 9101399

FRANCE

Mitsubishi Electric Europe GmbH
55, Avenue de Colmar
92563 Rueil Malmaison Cedex
Telex: 632326
Telephone: 47087871
Facsimile: 47513622

ITALY

Mitsubishi Electric Europe GmbH
Centro Direzionale Colleoni
Palazzo Cassiopea 1
20041 Agrate Brianza I-Milano
Telephone: (039) 636011
Facsimile: (039) 6360120

SWEDEN

Mitsubishi Electric Europe GmbH
Lastbilsvägen 6B
5-19149 Sollentuna, Sweden
Telex: 10877 (meab S)
Telephone: (08) 960468
Facsimile: (08) 966877

U.K.

Mitsubishi Electric (U.K.) Ltd.
Travellers Lane
Hatfield
Herts AL10 8XB, England, U.K.
Telephone: (0044) 7072 76100
Facsimile: (0044) 7072 78692

AUSTRALIA

Mitsubishi Electric Australia Pty. Ltd.
73-75, Epping Road, North Ryde,
P.O. Box 1567, Macquarie Centre,
N.S.W., 2113, Australia
Telex: MESYD AA 26614
Telephone: (02) (888) 5777
Facsimile: (02) (887) 3635

MITSUBISHI ELECTRIC

MITSUBISHI DATA BOOK
SINGLE-CHIP 8-BIT MICROCOMPUTERS

January, First Edition 1989

Editioned by
Committee of editing of Mitsubishi Semiconductor Data Book

Published by
Mitsubishi Electric Corp., Semiconductor Division

MITSUBISHI SEMICONDUCTORS
SINGLE-CHIP 8-BIT MICROCOMPUTERS

MITSUBISHI ELECTRIC CORPORATION
HEAD OFFICE : MITSUBISHI DENKI BLDG, MARUNOUCHI, TOKYO 100. TELEX : J24532 CABLE MELCO TOKYO

H-D4424-A KI-8901 Printed in Japan (ROD)

New publication, effective Jan. 1989.
Specifications subject to change without notice.