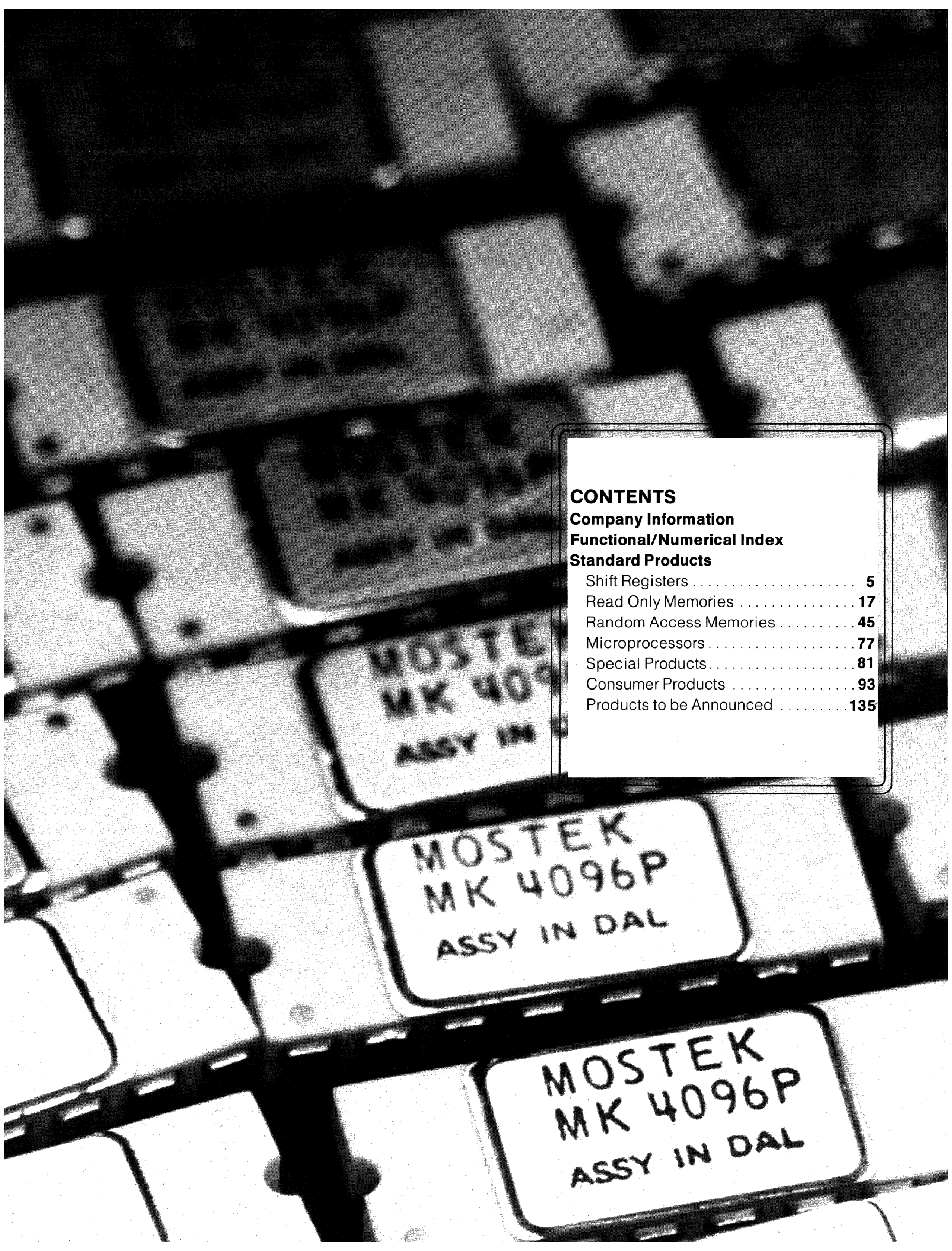
INTEGRATED CIRCUIT GUIDE



CONTENTS

THE COMPANY Since formation in 1969, MOSTEK has grown dramatically in product development, geographic scope and technological capability. Sales have advanced from $1 million in 1970 to an excess of $40 million in 1973.

Geographic expansion has been just as rapid. Sales representation is virtually worldwide and manufacturing plants are now operating in Carrollton, Texas; Worcester, Massachusetts; and Penang, Malaysia. A complete MOSTEK circuit design facility is located in Stuttgart, West Germany.

Engineering strengths have been particularly important to this growth pattern. The superior engineering design capabilities at MOSTEK have regularly increased the state-of-the-art of the entire industry.

MOSTEK "firsts" include...

- First production of low threshold PMOS by ion-implantation
- First single-chip calculator
- First production of MOS/LSI having both enhancement and depletion transistors on the same chip
- First TTL compatible 1024-bit RAM
- First single 5-volt supply PMOS
- First MOS/LSI circuit combining N-channel, silicon-gate and ion-implanted depletion load processes
- First 4096-bit Random Access Memory

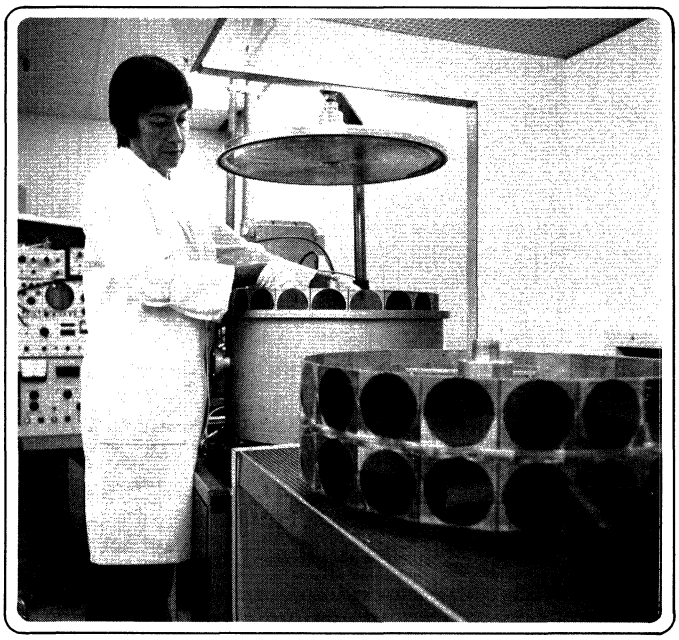
FACILITIES

MOSTEK's continued growth is evidenced by the recent addition of 40,000 square feet to the Dallas facility and the purchase of a 273,000 square foot plant in Lowell, Massachusetts. This will bring MOSTEK's total facilities to approximately 449,000 square feet.

Dallas area MOSTEK	136,000
Worcester	8,000
GMBH Stuttgart, West Germany	5,000
Penang, Malaysia	27,000
Lowell, Massachusetts	273,000
	449,000

MANUFACTURING

OPERATIONS PLANNING, PURCHASING AND INVENTORY CONTROL To organize MOSTEK's explosive product output, a complex system of computerized information has been developed for planning and control purposes. These systems include a long-range linear programming model for forecasting manufacturing capacity constraints in relation to anticipated sales; a complex system of scheduling production and inventory control reports; and product yield and costing reports. This information is routed to company locations in Worcester, Massachusetts; Penang, Malaysia; and three subcontract offshore assembly facilities as well as all sales offices.



MANUFACTURING ENGINEERING

The two major operations within MOSTEK manufacturing engineering are test equipment engineering and product engineering. Both efforts begin early in the product design state and continue throughout the product life. At MOSTEK, new product designs are quickly evaluated using a sophisticated computer system including Fairchild 500 and 600 units and an STS Venture II. In addition, MOSTEK developed unique parametric measuring and timing units to complement the computer evaluation network.

In order to offer the most thorough testing of MOS/LSI circuits, MOSTEK designed and built the "Bluebird" series of IC testers. MOSTEK now operates eleven of these sophisticated systems, testing 100% of all units shipped.

PROCESSING TECHNOLOGY

With the incorporation in 1969 of ion-implantation into standard PMOS processing, MOSTEK pioneered a technique enabling the use of both depletion and enhancement transistors on the same device. This technique gave improved performance and allowed process optimization for lowering device costs. MOSTEK has recently expanded its production processing capabilities to offer ion-implanted N-channel MOS and CMOS devices having improved electrical characteristics over non-implanted versions.

MOSTEK currently operates two separate wafer fabrication facilities devoted to high volume production of MOS devices. The original facility located in Worcester, Massachusetts has approximately 8,000

square feet primarily utilized for processing two-inch and three-inch silicon slices. The second facility, located at MOSTEK headquarters in Carrollton, has approximately 28,000 square feet primarily utilized for processing of three-inch slices. An additional 63,000 square feet is being prepared for occupancy in 1975 in Lowell, Massachusetts as a third process area.

At MOSTEK's Worcester facility, more than one million wafer implants have been performed, making this facility the world's largest supplier of ion-implanted MOS wafers.

All photomask shipments are sampled by Quality Control for geometry control, etch accuracy and physical damage. Each set of newly shipped masks is checked for proper registration. MOSTEK has found that well-defined and tightly controlled mask specifications have a high impact on circuit yield.

Each assembly piece part shipment (packages, gold wire, preforms, lids, etc.) is checked for physical dimensions, plating thickness, bondability, tensile strength, wetability and hermetic seal before release to the manufacturing department.

WORKMANSHIP QUALITY CONTROL

MOSTEK's wafer processing is performed in class 100 environments having humidity and temperature control. These operations are performed by highly skilled manufacturing personnel and are continuously monitored by quality control operators to insure conformance to all specifications.

Each die receives a manufacturing 100% visual inspection and a QC Lot Acceptance prior to its submission to the Assembly process. The assembled unit is then subjected to another manufacturing 100% inspection and a QC Lot Acceptance immediately prior to the sealing (encapsulation) process. MOS is a surface oriented technology and most defects can be detected by well-trained assembly and QC operators.

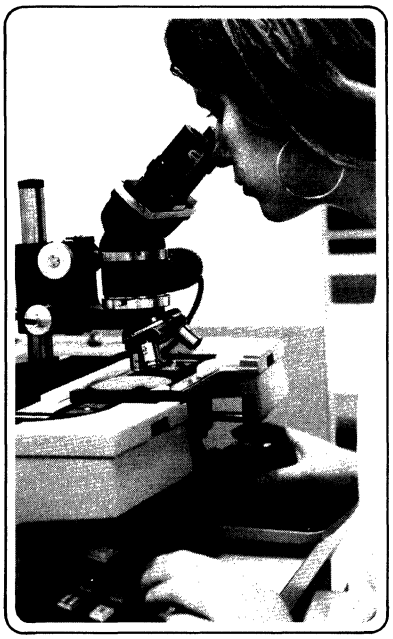
Each completed device receives an electrical test by the manufacturing department; additionally all material is submitted to sample electrical testing by Quality Assurance personnel. All lots rejected are rescreened 100%.

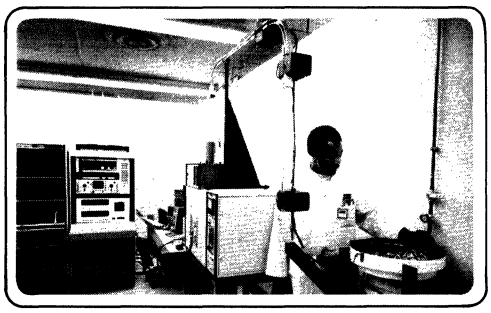
The MOSTEK Quality Department uses one of the most powerful analytical tools available today. This instrument, the Scanning Electron Microscope (SEM), allows an order of magnitude improvement in resolving power over standard light microscope equipment. Uses include:

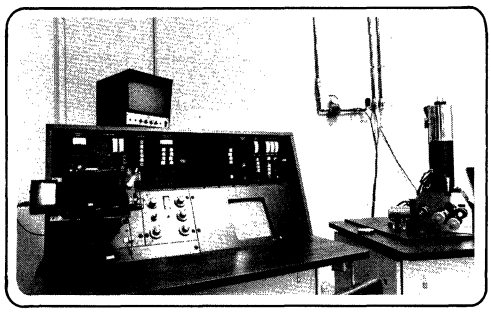
(1) Real time process control for the wafer fabrication areas
(2) Design and prototype analysis of new products
(3) Wafer processing research and development
(4) Wafer/lot analysis
(5) Failure analysis

QUALITY ASSURANCE

MOSTEK places unusual emphasis on product quality evidenced by the ratio of manufacturing to QC personnel of 10:1. The common industry ratio is 20-30:1. And at MOSTEK 30% of the QC staff are high technology professionals.







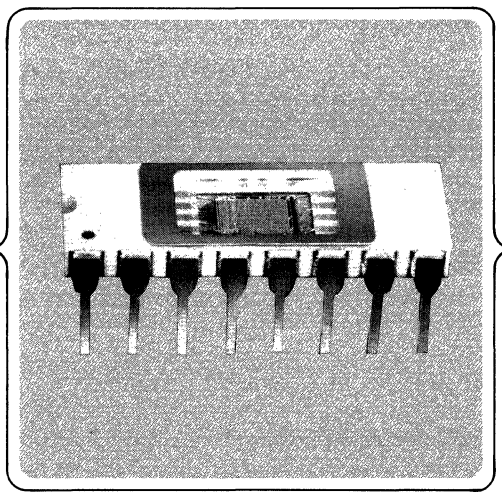
INCOMING MATERIAL QUALITY CONTROL

Polished silicon wafers are purchased under specifications including wafer thickness, resistivity, diameter, crystal orientation and dislocation distribution. Each shipment is sampled by Quality Control prior to release to production.

Electronic grade chemicals are used exclusively. Proprietary solutions, such as oxide and metal etch solutions, are checked with respect to etch rate and discoloration prior to release to the manufacturing line.

Functional Numerical Index

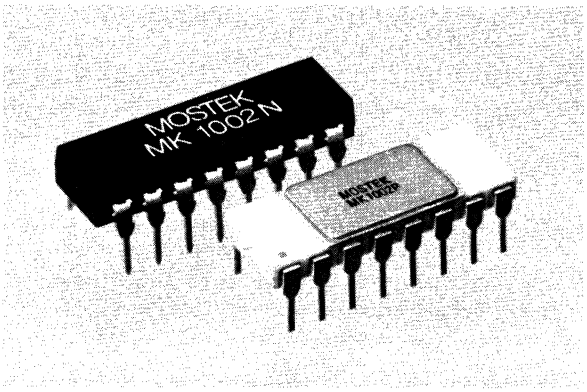
Shift Registers



Shift Registers

DUAL 128-BIT MOS Static Shift Register

MOSTEK



FEATURES:

- ☐ Ion-implanted for full TTL/DTL compatibility — no interface circuitry required
- ☐ Single-phase, TTL/DTL compatible clocks
- ☐ Dual 128-bit static shift registers — 256 bits total
- ☐ Dual sections have independent clocks
- ☐ Recirculate logic built in
- ☐ DC to 1 MHz clock rates
- ☐ Low power dissipation — 130 mW
- ☐ 16-pin dual-in-line package

APPLICATIONS

- ☐ Delay lines
- ☐ Buffer data storage
- ☐ Recycling test data sequencer
- ☐ Digital filtering

DESCRIPTION

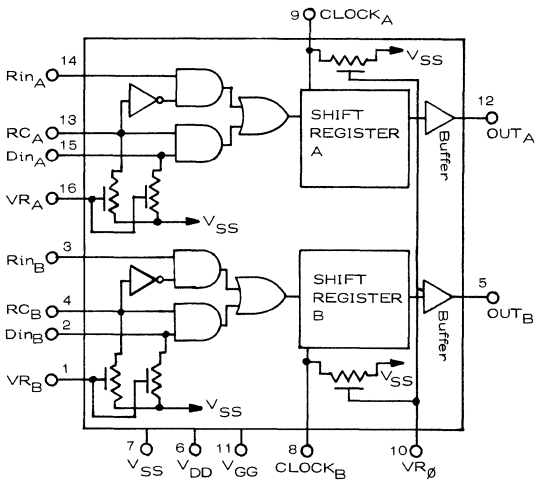
The MK 1002 is a P-channel MOS static shift register utilizing low threshold-voltage processing and ion-implantation to achieve full TTL/DTL compatibility. Each of the two independent 128 bit sections has a built-in clock generator to generate three internal clock phases from a single-phase TTL-level external input. In addition, each section has input logic for loading or recirculating data within the register. (See Functional Diagram.) The positive-logic Boolean expression for this action is:

$$\text{OUT (delayed 128 bits)} = (R_C)(D_{in}) + (\overline{R_C})(R_{in})$$

The Data, Recirculate Control, and Clock inputs are provided with internal pull-up resistors to V_{SS} (+5V) for use when driving from TTL. These resistors can be disabled when driving from circuitry with larger output-voltage swings, such as DTL. Enabling of pull-up resistors is accomplished by connecting the appropriate terminal to V_{GG}; disabling by connecting to V_{SS}. The Recirculate inputs are not provided with pull-up resistors since they are generally driven from MOS.

Shifting data into the register is accomplished while the Clock input is low. Output data appears following the positive-going Clock edge. Data in each register can be held indefinitely by maintaining the Clock input high.

FUNCTIONAL DIAGRAM



OPERATING NOTES

R_C	R_{in}	D_{in}	DATA ENTERED
1	X	1	1
1	X	0	0
0	1	X	1
0	0	X	0

"1" = V_{SS} = +5V
"0" = V_{DD} = Grd
X = No Effect
Output Logic: See Description.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} . . . . . V_{SS} — 10.0 V
Supply Voltage, V_{GG} . . . . . V_{SS} — 20.0 V
Voltage at any Input or Output . . . . . V_{SS} + 0.3 V to V_{SS} — 10.0 V
Operating Free-air Temperature Range . . . . . 0°C to +75°C
Storage Temperature Range . . . . . —55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply Voltage	4.75	5.0	5.25	V	$V_{DD} = 0$ V
	V_{GG}	Supply Voltage[1]	—12.6	—12.0	—11.4	V	
INPUTS	V_{IL}	Input Voltage, Logic 0[2]		0	V_{SS}—4	V	
	V_{IH}	Input Voltage, Logic 1	V_{SS}—1	5.0	V_{ss}	V	
INPUT TIMING	f	Clock Repetition Rate	DC		1	MHz	
	$t_{\phi p}$	Clock Pulse Width	0.35		10	μs	
	$t_{\phi d}$	Clock Pulse Delay	0.4			μs	See
	$t_{\phi r}$	Clock Pulse Risetime	.010		0.2	μs	Timing
	$t_{\phi f}$	Clock Pulse Falltime	.010		0.2	μs	Diagram
	t_{dld}	Data Leadtime	50			ns	
	t_{dlg}	Data Lagtime	200			ns	
	t_{rld}	Recirculate Control Leadtime	100			ns	
	t_{flg}	Recirculate Control Lagtime	300			ns	

ELECTRICAL CHARACTERISTICS

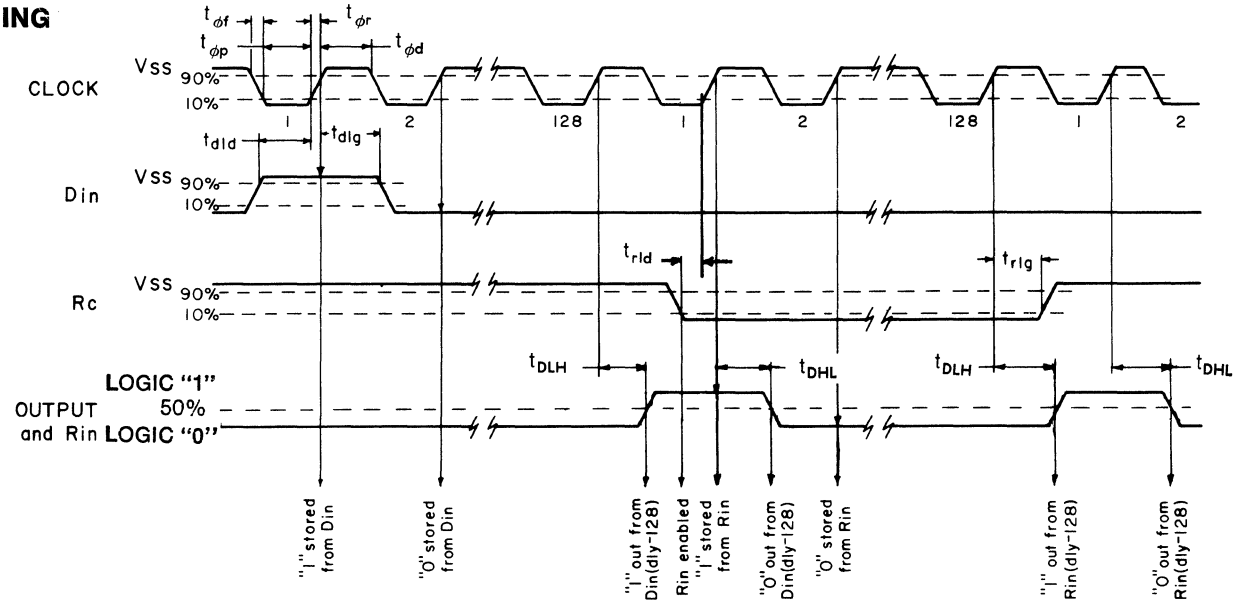
($V_{SS} = +5 \pm 0.25V, V_{GG} = -12 \pm 0.6V, V_{DD} = 0V, T_A = 0°C$ to $+75°C$, using test circuit shown, unless otherwise noted.)

		PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Power Supply Current, V_{SS}		14	25	mA	$f_\phi = 1$ MHz Inputs & Outputs open
	I_{GG}	Power Supply Current, V_{GG}		5	10	mA	
INPUTS	C_i	Input Capacitance, any Input		3	10	pF	$V_I = V_{SS}$, f = 1 MHz $T_A = 25°C$
	I_{IL}	Input Current, Logic 0: Resistors Disabled[2]			−40	μA	$V_I = V_{SS} - 5V$
		Resistors Enabled[2]	−0.3		−1.6	mA	$V_I = +0.4V$
	I_{IH}	Input Current, Logic 1, Any Input			40	μA	$VR_A, VR_B, VR\phi = V_{SS}$ $V_I = V_{SS}$
	$I_{IR(on)}$	Input Current at Recirculate Inputs[2]			−40	μA	$VR_A, VR_B, VR\phi = V_{GG}$ $V_I = V_{SS} - 5V$
OUTPUTS	V_{OL}	Output Voltage, Logic 0 (3)			0.4	V	$I_L = -1.6$ mA
	V_{OH}	Output Voltage, Logic 1 (3)	$V_{SS} - 1$			V	$I_L = +100\ \mu A$
DYNAMIC CHAR.	t_{DLH}	Output Delay, Low to High (3)			450	ns	See Timing Diagram and Test Circuit
	t_{DHL}	Output Delay, High to Low (3)			450	ns	
	t_{VOR}	Output Voltage Rise Time (3)		100	150	ns	
	t_{VOF}	Output Voltage Fall Time (3)		100	150	ns	

NOTES:

1. Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., $V_{SS} = 0V$, $V_{DD} = -5 \pm 0.25V$, $V_{GG} = -17 \pm 0.85V$.
2. MOS pull-up resistors to +5V are provided internally. These MOS resistors are enabled by connecting VR_A, VR_B and $VR\phi$ to V_{GG}, and disabled by connecting VR_A, VR_B and $VR\phi$ to V_{SS}. Pull-up resistors not provided at recirculate inputs.
3. At $T_A = 25°C$.

TIMING



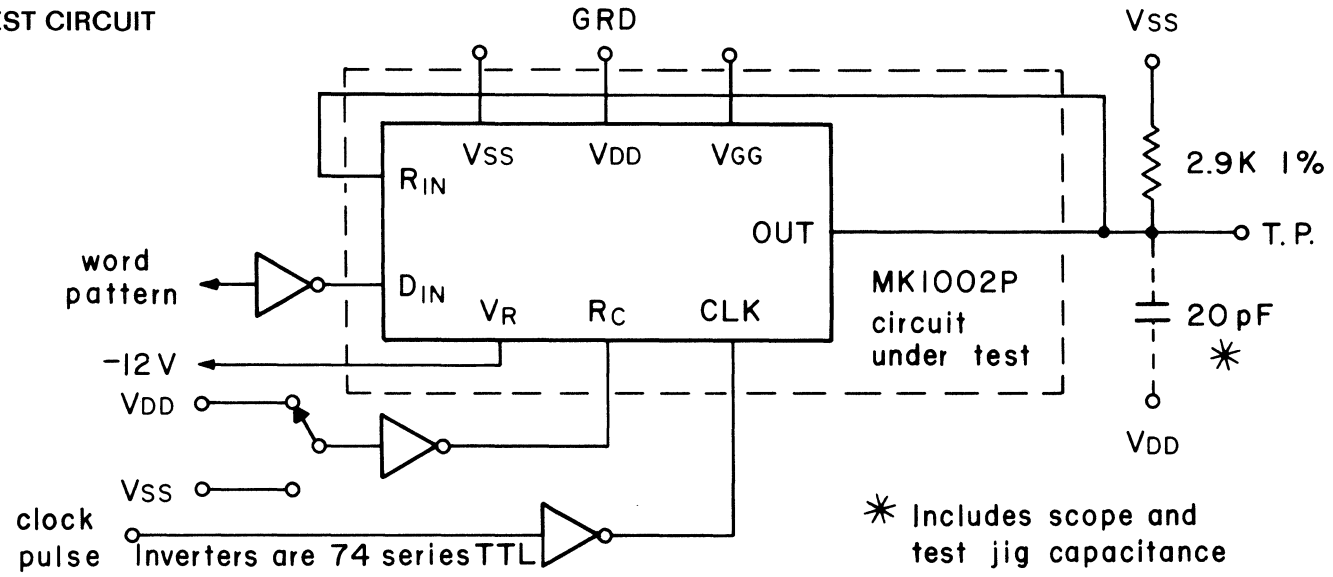
The timing diagram applies to either section of the dual shift register. The test conditions for these waveforms are illustrated below. A logic "1" is defined as +5 V and a logic "0" is defined as 0V

As long as R_C is at a "1", R_{in} is disabled and D_{in} is enabled. The data that is present at D_{in} while the clock is at "0" is shifted in and will be stored as the clock goes to a "1" This data must have been present t_{dld} time prior to the clock "1" edge. The data must also remain in that same state for t_{dlg} time after that edge. These times are necessary to insure proper data storage in the first register-cell.

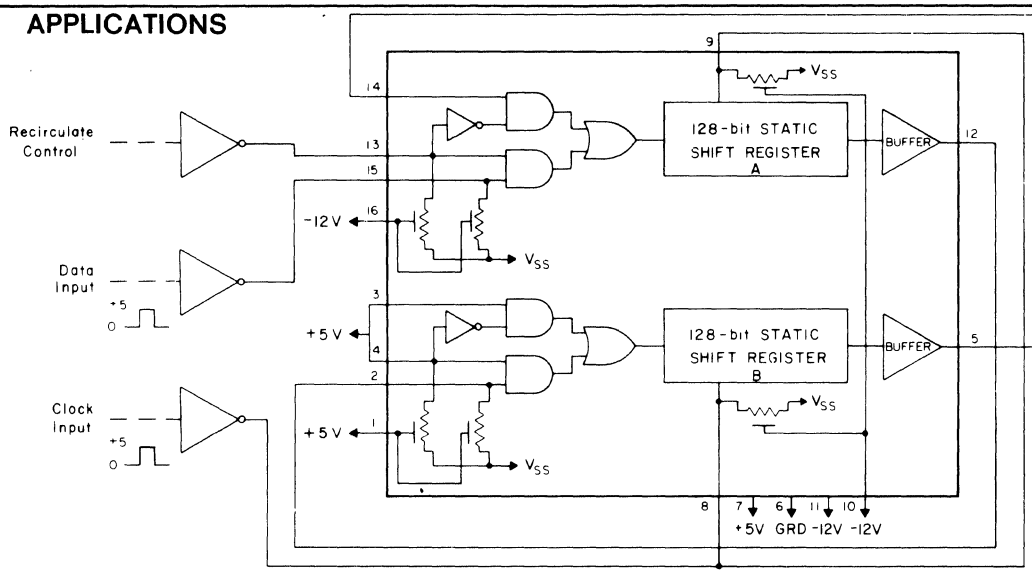
On the clock "1" edge, data is shifted through the register causing bit 127 to be shifted to position 128. This cell's output is buffered and appears at the output in the same logic polarity that appeared at the input 128 clocks prior. This data appears within t_{pd} time of the clock "1" edge.

R_{in} may be hardwired to the data output. When R_C is at a "0", R_{in} is enabled and D_{in} is disabled. Therefore, the output data will appear at the input of the first cell. When R_{in} is tied to the data output, the output delay will insure t_{dlg} and t_{dld} times. R_C "0" time must lead the clock "1" edge by t_{rld} time and must lag that edge by t_{rlg} time to insure proper data storage when recirculate storage is desired.

TEST CIRCUIT



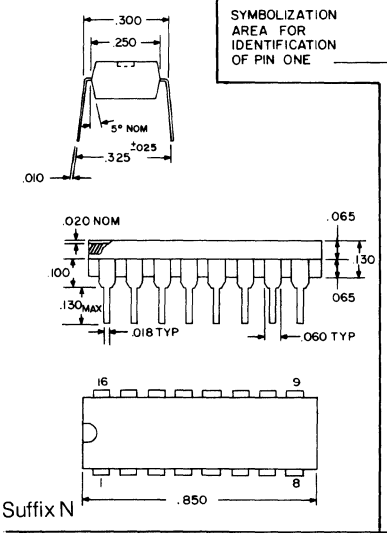
APPLICATIONS



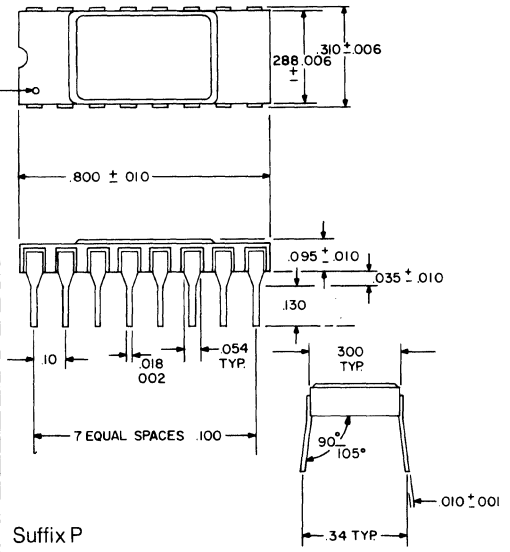
This shows the MK 1002 P connected to operate as a single, 256-bit, static shift register. Pull-up resistors are enabled at TTL driven inputs and disabled at MOS or DTL driven inputs. Any similar TTL/DTL device may be used in place of the inverters shown.

Inverters are 74-series TTL

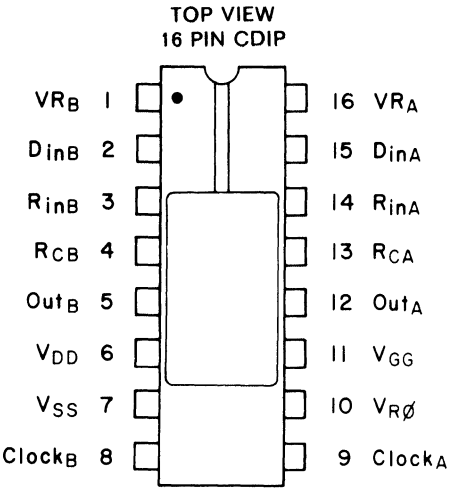
PACKAGE 16-pin plastic dual-in-line



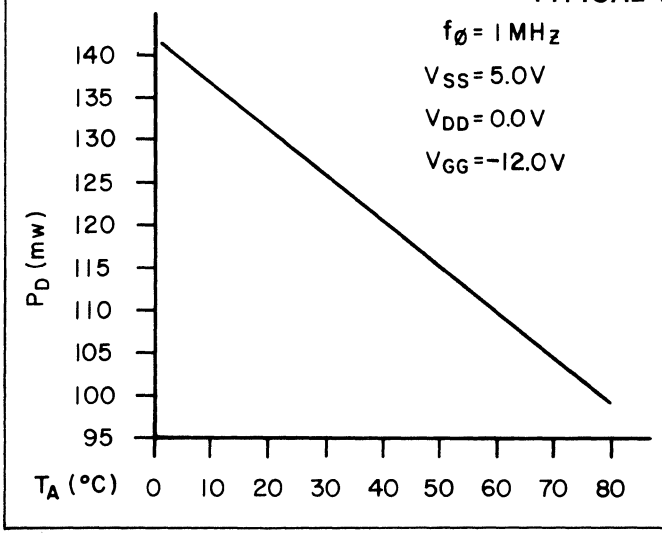
PACKAGE 16-pin ceramic dual-in-line

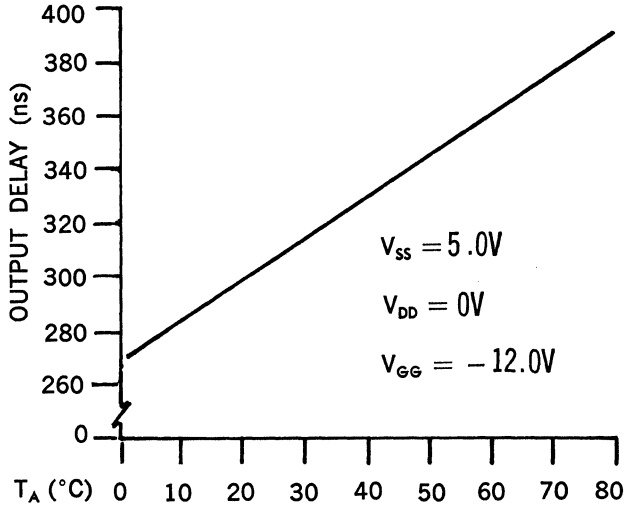


PIN CONNECTIONS



TYPICAL PERFORMANCE





MK 1002 L

DUAL 128 BIT
MOS Static Shift Register

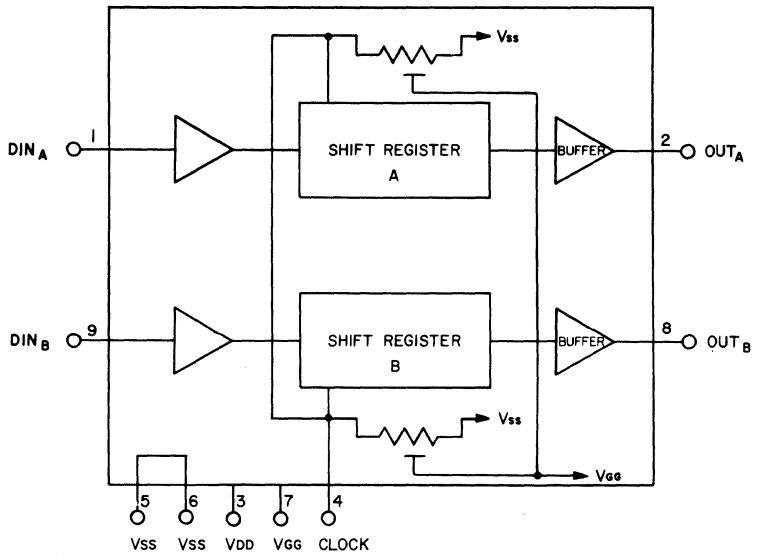
MOSTEK

DESCRIPTION

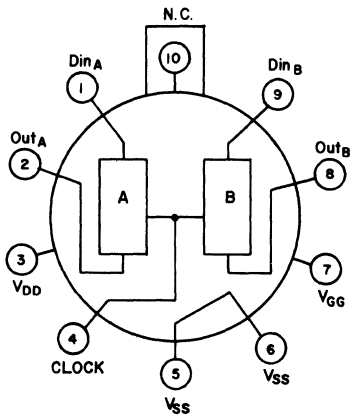
The MK 1002 is a P-channel MOS static shift register utilizing ion implant, low-threshold voltage processing to achieve full TTL/DTL compatibility. Each of the two independent 128-bit sections has a built-in clock generator to generate three internal clock phases from a single-phase TTL level external input.

Shifting data into the register is accomplished while the clock input is low. Output data appears following the positive-going clock edge. Data in each register can be held indefinitely by maintaining the clock input high.

FUNCTIONAL DIAGRAM

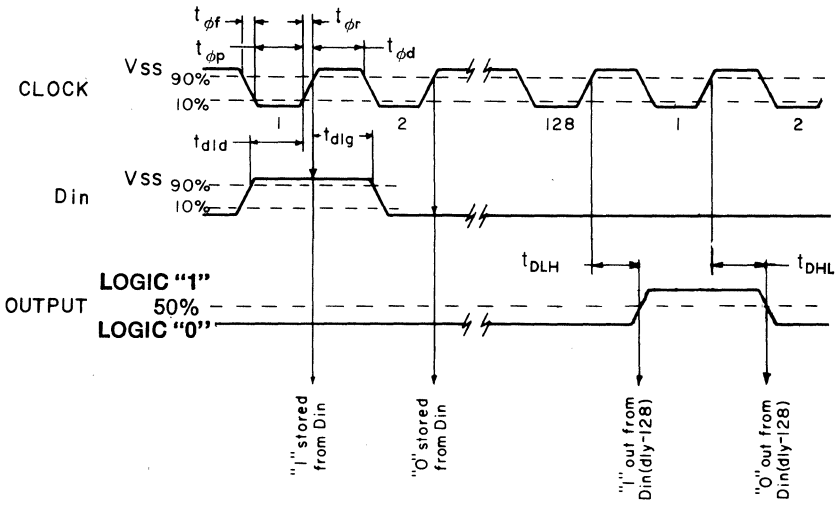


PIN CONNECTIONS

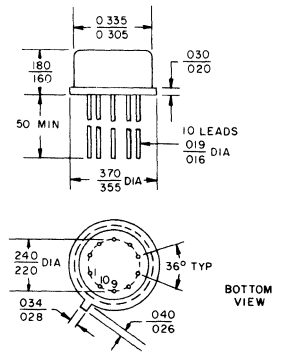


TOP VIEW
N.C. = no connection

TIMING



PACKAGE



NOTES
A. ALL DIMENSIONS IN INCHES UNLESS OTHERWISE SPECIFIED
B. ALL LEADS WELDABLE AND SOLDERABLE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} . . . . . V_{SS} — 10.0 V
Supply Voltage, V_{GG} . . . . . V_{SS} — 20.0 V
Voltage at any Input or Output . . . . . V_{SS} + 0.3 V to V_{SS} — 10.0 V
Operating Free-air Temperature Range . . . . . 0°C to +75°C
Storage Temperature Range . . . . . —55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
POWER	V_{SS}	Supply Voltage	4.75	5.0	5.25	V	V_{DD} = 0 V
	V_{GG}	Supply Voltage[1]	—12.6	—12.0	—11.4	V	
INPUTS	V_{IL}	Input Voltage, Logic 0[2]		0	V_{SS}—4	V	
	V_{IH}	Input Voltage, Logic 1	V_{SS}—1	5.0	V_{ss}	V	
INPUT TIMING	f_ϕ	Clock Repetition Rate	DC		1	MHz	
	$t_{\phi p}$	Clock Pulse Width	0.35		10	μs	
	$t_{\phi d}$	Clock Pulse Delay	0.4			μs	See
	$t_{\phi r}$	Clock Pulse Risetime	.010		0.2	μs	Timing
	$t_{\phi f}$	Clock Pulse Falltime	.010		0.2	μs	Diagram
	t_{dld}	Data Leadtime	50			ns	
	t_{dlg}	Data Lagtime	200			ns	

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5 ±0.25V, V_{GG} = −12 ±0.6V, V_{DD} = 0V, T_A = 0°C to +75°C, unless otherwise noted.)

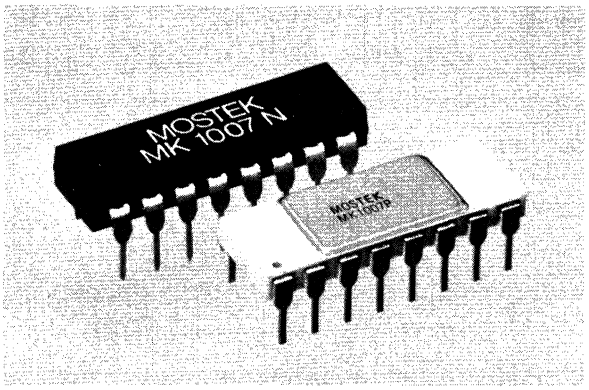
		PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Power Supply Current, V_{SS}		14	25	mA	f_ϕ = 1 MHz Inputs & Outputs open
	I_{GG}	Power Supply Current, V_{GG}		5	10	mA	
INPUTS	C_i	Input Capacitance, any Input		6	10	pF	$V_I = V_{SS}$, f = 1 MHz
		Clock		12	20	pF	T_A = 25°C
	I_{IL}	Input Current, Logic 0,					
		Data			−40	μA	$V_I = V_{SS}$ —5V
		Clock	-0.6		−3.2	mA	V_I = +0.4V
	I_{IH}	Input Current, Logic 1, Any Input			40	μA	$V_I = V_{SS}$
OUTPUTS	V_{OL}	Output Voltage, Logic 0[3]			0.4	V	I_L = −1.6 mA
	V_{OH}	Output Voltage, Logic 1[3]	V_{SS} − 1			V	I_L = +100 μA
DYNAMIC CHAR.	t_{DLH}	Output Delay, Low to High[3]			450	ns	
	t_{DHL}	Output Delay, High to Low[3]			450	ns	See Timing
	t_{VOR}	Output Voltage Rise Time[3]		100	150	ns	Diagram
	t_{VOF}	Output Voltage Fall Time[3]		100	150	ns	

NOTES:
1. Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., V_{SS} = OV, V_{DD} = −5±0.25V, V_{GG} = −17±0.85V.
2. Pull-up resistances to +5V are provided internally at Clock Input.
3. At T_A = 25°C.

MK 1007P
MK 1007N

320 Bits (4x80)
MOS Dynamic Shift Register

MOSTEK



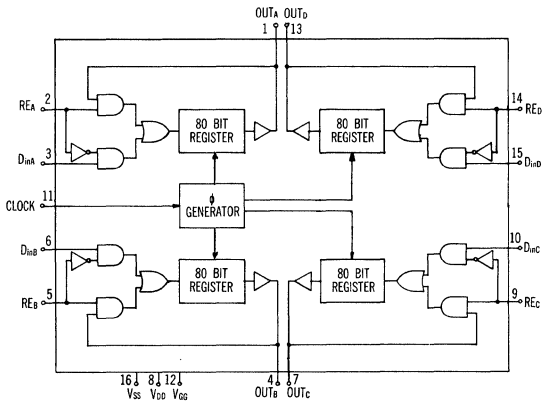
FEATURES:

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Single-phase, TTL/DTL-compatible clock
- ☐ Internal pull-up resistors
- ☐ Clock frequency 10 kHz to 2.5 MHz
- ☐ Built-in recirculate logic for each register
- ☐ Power Supplies: +5V and −12V

APPLICATIONS:

- ☐ CRT display systems
- ☐ Buffer data storage
- ☐ Delay lines
- ☐ Digital filtering

FUNCTIONAL DIAGRAM



DESCRIPTION

The MK 1007 P contains four separate 80-bit MOS dynamic shift registers on a single chip, using ion-implantation in conjunction with P-channel processing to achieve low threshold voltage and direct TTL/DTL compatibility. All logic inputs, including the single-phase Clock, can be driven directly from DTL or TTL logic. Pull-up resistors to +5V are provided for worst-case TTL inputs.

Each 80-bit register has independent inputs and outputs and a control input (RE) which allows external data to be shifted into the register (at logical 0) or data at the output to be recirculated into the register (at logical 1).

All four registers use a common (external) Clock input. With the Clock high (1), data is shifted into the registers. Following the negative-going edge of the Clock, data shifting is inhibited and output data appears. Output data is True, delayed 80 bits.

Since the MK 1007 P has zero lag-time requirements for data inputs, devices may be cascaded, i.e., the output of one device may be fed directly to the input of another device. All inputs are protected to prevent damage due to static charge accumulation.

OPERATING NOTES:

1. Recirculate Enable (RE) = Logic 1 = output data recirculated.
2. Output data (delayed 80 bits) maintains same logic state when RE = 1.
3. Recirculate Enable (RE) = Logic 0 = Data In (D_{in}) enabled.
4. Output data (delayed 80 bits) attains same logic state as D_{in} when RE = 0.
5. Output data follows the clock negative edge.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD} . . . . . V_{SS} + 0.3 V to V_{SS} − 20 V
Supply Voltage V_{GG} . . . . . V_{SS} + 0.3 V to V_{SS} − 20 V
Voltage at any Input or Output . . . . . V_{SS} + 0.3 V to V_{SS} − 20 V
Operating Free-air Temperature Range . . . . . 0°C to 75°C
Storage Temperature Range . . . . . −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

(0°C ≤ T_A ≤ 75°C)

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS} Supply Voltage	4.75	5.0	5.25	V	V_{DD} = 0 V
	V_{GG} Supply Voltage[1]	−12.6	−12.0	−11.4	V	
INPUTS	V_{IL} Logic "0" Voltage, any input		0.0	0.8	V	
	V_{IH} Logic "1" Voltage, any input [2]	V_{SS} − 1.5	+5.0	V_{SS}	V	
INPUT TIMING	$f\phi$ Clock Repetition Rate	.01		2.5	MHz	
	$t\phi_p$ Clock Pulse Width	.150		100	μs	NOTE: Total permitted clock times will be determined by clock frequency, $f\phi$.
	$t\phi_d$ Clock Pulse Delay	.150		100	μs	
	$t\phi_r$ Clock Pulse Risetime	.010		5	μs	
	$t\phi_f$ Clock Pulse Falltime	.010		5	μs	
	t_{dld} Data Leadtime	150			ns	
	t_{dlg} Data Lagtime	0			ns	
	t_{rld} Recirculate Control Leadtime	200			ns	
	t_{rlg} Recirculate Control Lagtime	50			ns	

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5 ±0.25 V, V_{GG} = −12 ±0.6V, V_{DD} = 0V, T_A = 0°C to +75°C, unless otherwise specified.)

	PARAMETER	MIN	TYP[3]	MAX	UNITS	CONDITIONS
POWER	I_{SS} V_{SS} Power Supply Current[4][5]		22.0	40.0	mA	$f\phi$ = 2.5 MHz;
	I_{GG} V_{GG} Power Supply Current[5]		9.0	16.0	mA	outputs open
INPUTS	C_{IN} Capacitance at Data, RE, and Clock Inputs[5]		3	6	pF	V_I = V_{SS}, $f\phi$ = 1 MHz
	I_{IL} Logic "0" Current, any input[5]	0.6	1.1	1.6	mA	V_I=0.4 V
	$I_{I(lk)}$ Leakage Current, any input			1	μA	V_I=V_{SS}−5.5V; V_{SS}=V_{DD}=V_{GG}
	R_{IN} Input Pullup Resistance[5]	3.0		8.4	kΩ	V_I=0.4 V
OUTPUTS	V_{OL} Logic "0" Output Voltage[5]			0.4	V	I_L = −1.6 mA
	V_{OH} Logic "1" Output Voltage[5]	V_{SS} − 1			V	I_L = +100 μA
DYN. CHAR.	t_{DLH} Output Delay, Low to High		75	200	ns	See Timing Diagrams
	t_{DHL} Output Delay, High to Low		75	200	ns	
POWER DIS.	$P_{D(1)}$ Power Dissipation[4]		220		mW	$f\phi$ = 2.5 MHz
	$P_{D(2)}$ Power Dissipation[4]		195		mW	$f\phi$ = 1 MHz
	$P_{D(3)}$ Power Dissipation[4]		170		mW	$f\phi$ = 10 kHz

NOTES:

(1) Other supply voltages are permissible providing that supply and input voltages are adjusted to maintain the same potential relative to V_{SS}, e.g., V_{SS}=0 V, V_{DD}= −5V, V_{GG}= −17 V.
(2) Pull-up resistances to +5V are provided internally.
(3) Typical values at T_A=25°C, V_{SS}=+5.0 V, V_{DD}=−12.0 V.
(4) I_{SS} will increase a maximum of 1.6 mA for each input at logic "0."
(5) At T_A=25°C.

TIMING

CONDITIONS:

1. All timing relationships apply to any of the four registers.
2. Logic 0 is defined as V_{DD} or ground; logic 1 as V_{SS} or +5V.

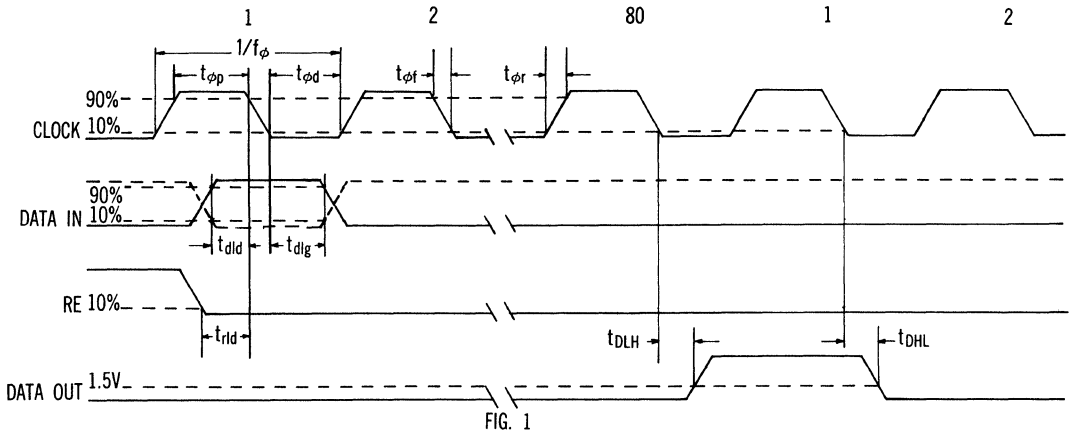


FIG. 1

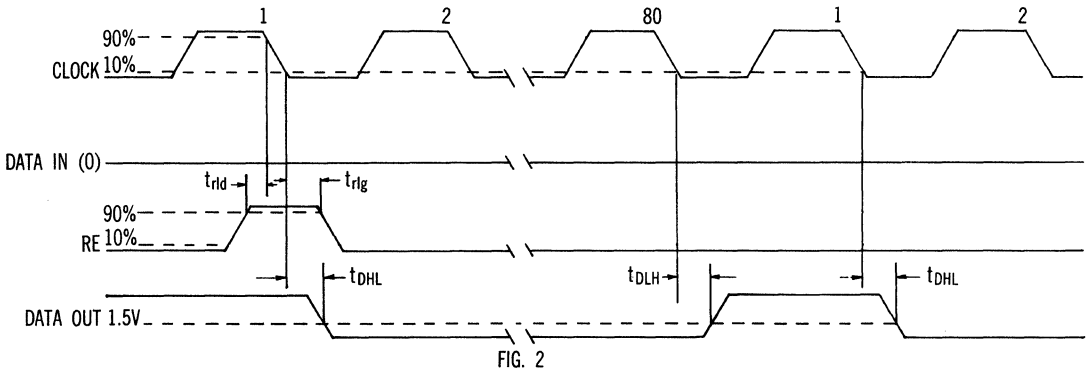
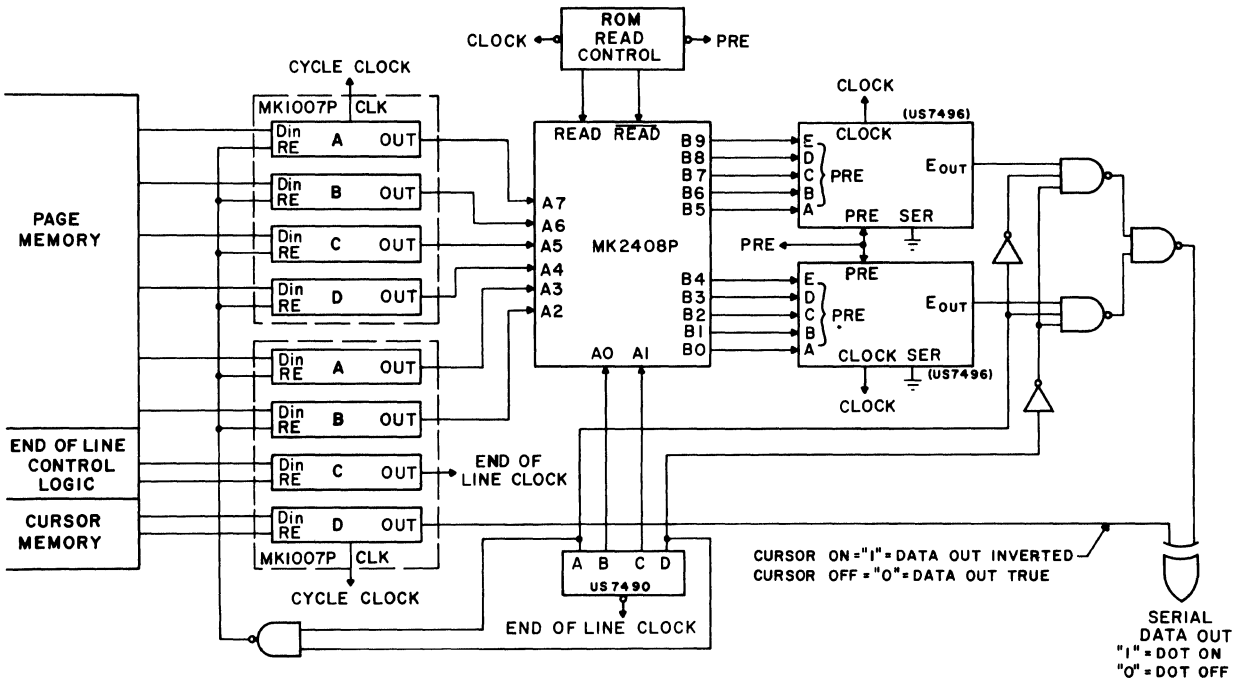


FIG. 2

SHIFT: Fig. 1 illustrates shifting a logic 1 bit from the Data Input (D_{in}) through one of the 80-bit registers. RE (Recirculate Enable) at logic 0 enables D_{in}. RE must go to logic 0 for t_{rld} time (Recirculate Control Leadtime) prior to the Clock's negative edge, and must maintain that state at least until the Clock's negative edge (t_{dlg}) to insure proper data shifting. This data bit entered will appear 80 clock pulses later within Output Delay Time (t_D) of that Clock's negative edge.

RECIRCULATE: Fig. 2 illustrates recirculating a bit present at the output back through the register. RE must attain a logic 1 for t_{rld} time (Recirculate Control Leadtime) prior to the Clock's negative edge, and must maintain that state at least until the Clock's negative edge (t_{rlg}) to insure proper data recirculation. The bit entered will appear 80 clocks later as shown.

APPLICATIONS



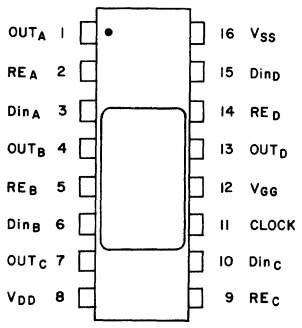
LINE REFRESH MEMORY FOR CRT DISPLAY

This application shows the MK 1007 P used as the Line Refresh Memory, driving MOSTEK's MK 2408 P TTL-compatible character generator. The MK 1007 P receives new data from the Page Memory (which may also consist of MK 1007 P's) on the tenth row of any character line, this being the third vertical space between rows of characters. The MK 1007 P recirculates the character-address data as these characters are scanned and displayed on a CRT screen.

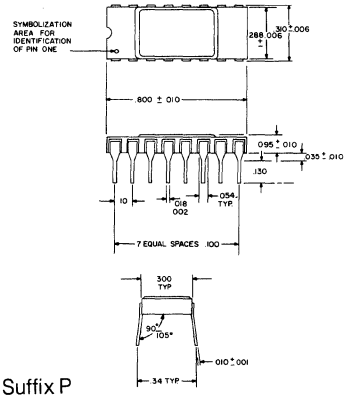
The decade counter selects the appropriate rows from the character generator which outputs two rows of the addressed character at one time (see MK 2408 P data sheet), and also controls the multiplexed output of the character generator so that only one row of the addressed characters is displayed on any CRT horizontal sweep.

One stage of the MK 1007 P may be used to shift a single data bit, which may be used to determine the end of the horizontal sweep. Another stage may be used as a cursor control and, as shown above, may blank the cursored character dots while surrounding dots are on, to give a reverse image of that particular character.

TOP VIEW
16 PIN CDIP

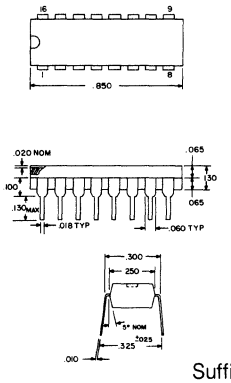


PACKAGE
16-pin ceramic dual-in-line



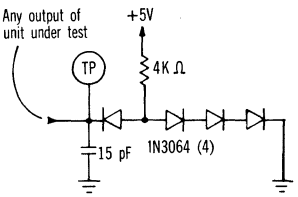
Suffix P

PACKAGE
16-pin plastic dual-in-line

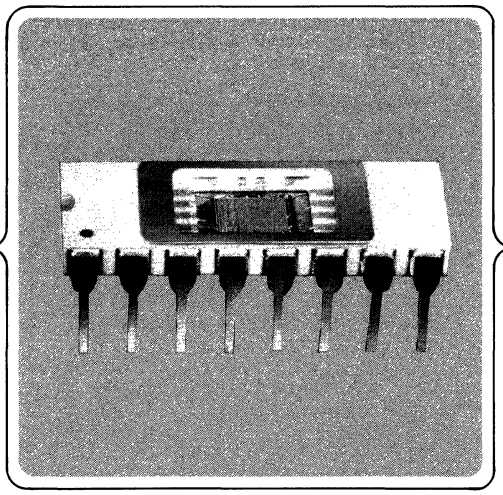


Suffix N

TEST CIRCUIT

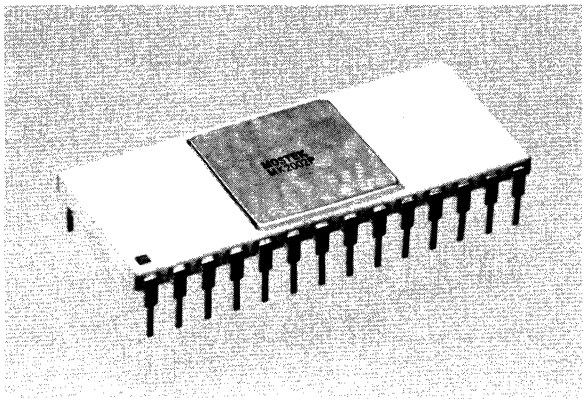


Read Only Memories



MOS Read-Only Memory Character Generators

MOSTEK



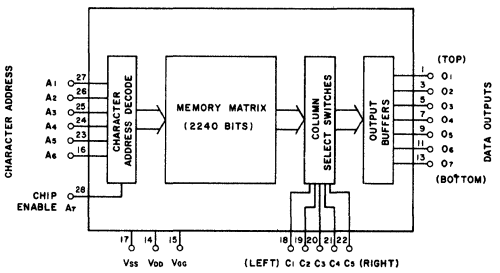
FEATURES:

- ☐ 64 dot-matrix (5×7) characters with column-by-column output
- ☐ High speed character access time and column select access time
- ☐ Completely static operation—no clocks required
- ☐ MK 2002 P is pre-programmed with ASCII encoding
- ☐ Easy interfacing to TTL/DTL
- ☐ Single mask custom programming

APPLICATIONS

- ☐ CRT alphanumeric displays
- ☐ Light-Emitting Diode (LED) array driver
- ☐ Billboard and stock market displays

FUNCTIONAL DIAGRAM



DESCRIPTION

This MK 2000 P Series MOS Read-Only Memories (ROMs) is designed specifically for dot-matrix character generation where column-by-column data output is desired. Each ROM contains 2240 bits of programmable storage, organized as 64 characters, each having 5 columns of 7 bits. P-channel, enhancement-mode, MOS technology is employed in this series. All inputs are protected to prevent damage due to static charge accumulation.

Programming is accomplished during the manufacturing process by modification of a single mask in accordance with customer specifications. The MK 2002 P is pre-programmed with ASCII-encoded characters with the font shown on the back page.

Memory operation is static and no refresh clocks are required to maintain output information. Character selection is achieved by presenting a seven-bit binary word at the address inputs. The most significant bit (A_7) is generally used as a Chip Enable. (See Operating Notes.) Column select lines, C_1 through C_5, select the column information that appears at the seven data outputs. (See Operating Notes.) By sequentially strobing C_1 through C_5, the font for the addressed character would be displayed. The output buffers are open-ended current sources, sourcing current from the V_{SS} supply only in the "dot-on" condition.

OPERATING NOTES

"1" = V_{DD} "0" = V_{SS}						
A_7	C_1	C_2	C_3	C_4	C_5	Column Selected
0	X	X	X	X	X	None*
1	0	0	0	0	0	None*
1	1	0	0	0	0	1 (left)
1	0	1	0	0	0	2
1	0	0	1	0	0	3
1	0	0	0	1	0	4
1	0	0	0	0	1	5 (right)

X=No effect on columns
* Outputs open-circuited

ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} ..... +0.3V to −30V
Operating temperature range ..... −25°C to +85°C
Storage temperature range ..... −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS (−0°C<T_A<70°C)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage		0.0		V	
	V_{DD}	Supply voltage	−12.0	−14.0	−16.0	V	See note 1
	V_{GG}	Supply voltage	−24.0	−28.0	−29.0	V	
INPUTS	$V_{in(0)}$	Input voltage, logic "0"	V_{SS}−3	V_{SS}		V	
	$V_{in(1)}$	Input voltage, logic "1"		V_{DD}	V_{SS}−11	V	

ELECTRICAL CHARACTERISTICS (V_{SS}=0.0V; V_{DD}=−14.0V; V_{GG}=−28.0V, T_A=25°C unless noted otherwise)

		PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS	
POWER	I_{DD}	Supply current (V_{DD})		13	25	mA	Outputs unconnected	
	I_{GG}	Supply current (V_{GG})		1.5	3.0	mA	See note 2	
INPUTS	C_{in}	Input capacitance			10	pF	$V_{in}=V_{SS}$, f_{meas}=1MHz	
	I_{in}	Input leakage current			10	μA	$V_{in}=V_{SS}$−14V	
OUTPUTS	V_{out}	Output voltage			V_{SS}−2	V	I_{out}=2.0 mA	See Figure #3
					V_{SS}−5	V	I_{out}=4.0 mA	
	$I_{out(on)}$	Output current, "dot-on"	6	12		mA	$V_{out}=V_{SS}$−14V	
	$I_{out(off)}$	Output current, "dot-off"			+10	μA		
DYNAMIC CHARACTERISTICS	$t_{A(on)}$	Character access time, I_{off} to I_{on}		320	700	ns	V_{DD}=−14V, V_{GG}=−28V	See Figures #1, #2 and Timing
				380	700	ns	V_{DD}=−12, V_{GG}=−24V	
	$t_{A(off)}$	Character access time, I_{on} to I_{off}		190	700	ns	V_{DD}=−14V, V_{GG}=−28V	
				220	700	ns	V_{DD}=−12V, V_{GG}=−24V	
	$t_{C(on)}$	Column select delay time, I_{off} to I_{on}		90	250	ns	V_{DD}=−14V, V_{GG}=−28V	See Figure #1 and Timing
				95	300	ns	V_{DD}=−12V, V_{GG}=−24V	
	$t_{C(off)}$	Column select delay time, I_{on} to I_{off}		180	250	ns	V_{DD}=−14V, V_{GG}=−28V	
				205	300	ns	V_{DD}=−12V, V_{GG}=−24V	
	t_{OE}	Output enable/disable delay time		320	700	ns	V_{DD}=−14V, V_{GG}=−28V	
	t_{AV}	Character access time (V_{out})		500		ns	V_{SS}=+14V, V_{DD}=0V, V_{GG}=−14V See Figure #4 and Timing	

NOTES: 1. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., V_{SS} = +14.0V, V_{DD} = 0.0V, V_{GG} = −14.0V.
2. $I_{SS}=I_{DD}+I_{GG}$

TIMING

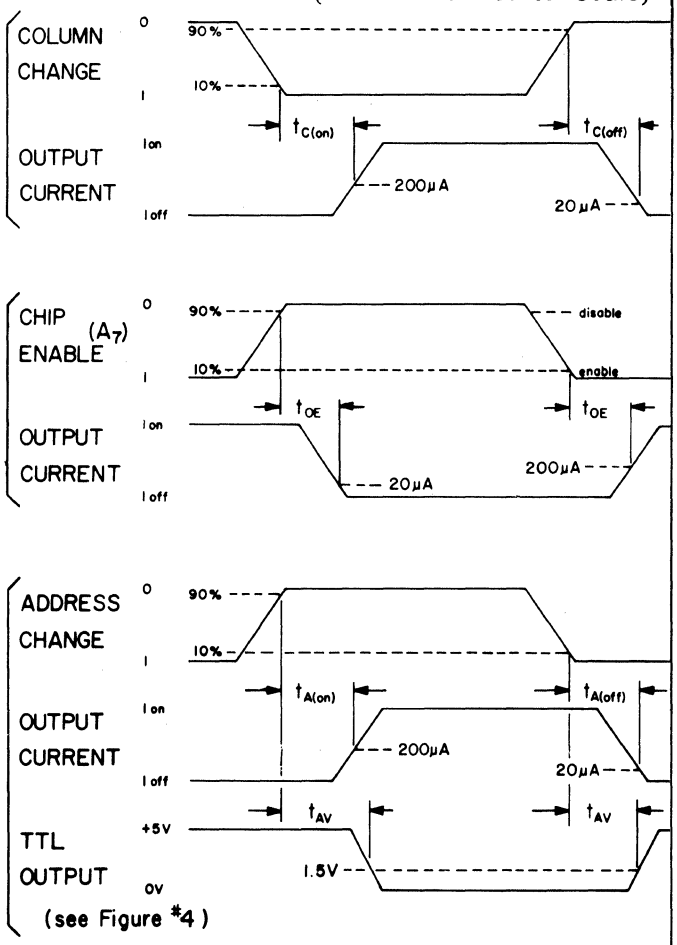
The A_7 input on The MK 2000 P Series may be programmed as a seventh address bit or as a chip enable, in which case either logic level may be chosen to enable the circuit.

When the A_7 input on The MK 2002 P is at a logical "O" (V_{SS}), the output buffers are turned off (I_{off}). When re-enabled, the chip will respond to the address and column selected at that time.

Columns are selected by applying a logical "1" (V_{DD}) to the appropriate select line while the other four select lines are at "0". Column selection may change while the address is held constant or addresses may be changed while any column is selected, or both may be changed simultaneously.

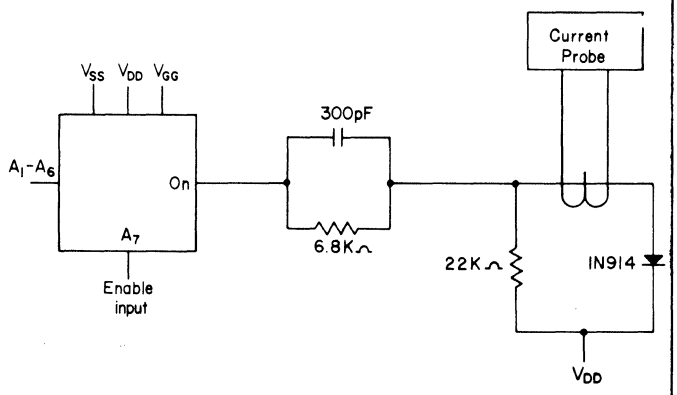
The MK 2000 P Series output buffers source current from the V_{SS} supply as indicated in Figure 3. Figure 4 is a suggested TTL/DTL interface. Delay time, t_{AV}, is measured to the output of the TTL shown in Figure 4.

(waveforms not to scale)



TEST CIRCUIT

FIGURE #1



TYPICAL PERFORMANCE

FIGURE #2

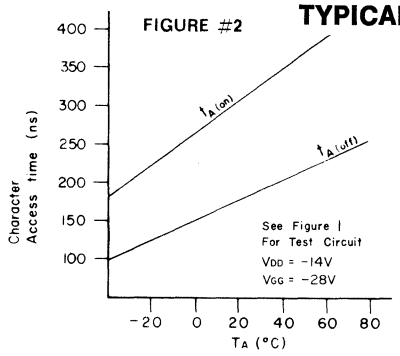
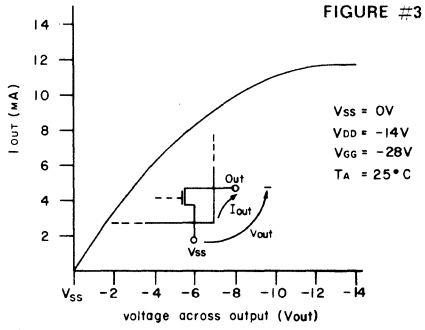
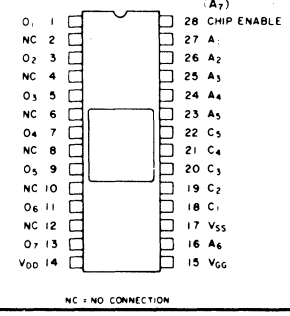


FIGURE #3



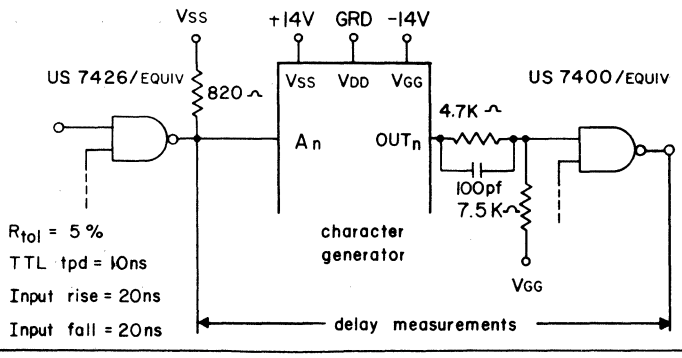
PIN CONNECTIONS

Top View, 28 Pin CDIP



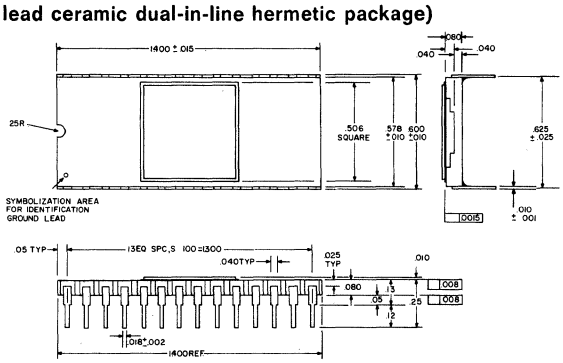
INTERFACE DIAGRAM/TEST CIRCUIT

FIGURE #4



PHYSICAL DESCRIPTION

(28 lead ceramic dual-in-line hermetic package)

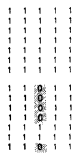
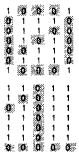
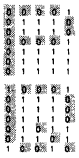


CODING AND CHARACTER FONTS

The MK 2002 P is a pre-programmed member of the MK 2000 P Series with ASCII encoding and the character fonts shown below. A logic "0" represents an input voltage equal to V_{SS}, or an output I_{ON}, and a logic "1" represents a voltage equal to V_{DD}, or an output I_{off}.

An example demonstrating the correspondence of device outputs and sequence to the 5 x 7 dot matrix fonts is shown below:

	C_1	C_2	C_3	C_4	C_5 ← Column Selected
O_1	0	1	1	1	0
O_2	0	0	1	0	0
O_3	0	1	0	1	0
O_4	0	1	0	1	0
O_5	0	1	1	1	0
O_6	0	1	1	1	0
O_7	0	1	1	1	0

MK 2002 P				A_6	1	1	0	0
				A_5	0	1	0	1
A_4	A_3	A_2	A_1	COL / ROW	2	3	4	5
0	0	0	0	0				
0	0	0	1	1				
0	0	1	0	2				
0	0	1	1	3				
0	1	0	0	4				
0	1	0	1	5				
0	1	1	0	6				
0	1	1	1	7				
1	0	0	0	8				
1	0	0	1	9				
1	0	1	0	10				
1	0	1	1	11				
1	1	0	0	12				
1	1	0	1	13				
1	1	1	0	14				
1	1	1	1	15				

MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2000 P

Cols. Information Field

First Card

1-30 Customer
31-50 Customer Part Number
60-72 Mostek Part Number[1]

Second Card

1-30 Engineer at Customer Site
31-50 Direct Phone Number for Engineer

Third Card

1-5 Mostek Part Number[1]
10-15 Organization[2]

Fourth Card

0-6 Data Format[3] — "MOSTEK"
15-28 Logic — "Negative Logic" only
35-57 Verification Code[4]

Data Cards

1-6 Binary Address
8-12 First row of character
14-18 Second row of character
20-24 Third row of character
26-30 Fourth row of character
32-36 Fifth row of character
38-42 Sixth row of character
44-48 Seventh row of character

Notes: 1. Assigned by Mostek Marketing Department; may be left blank.

2. Punched as 64x5x07 or 32x5x14.

3. "MOSTEK" format only is accepted on this part.

4. Punched as:
   (a) VERIFICATION HOLD — i.e. the customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.

2240 BIT

MOS Read-Only Memory Character Generators

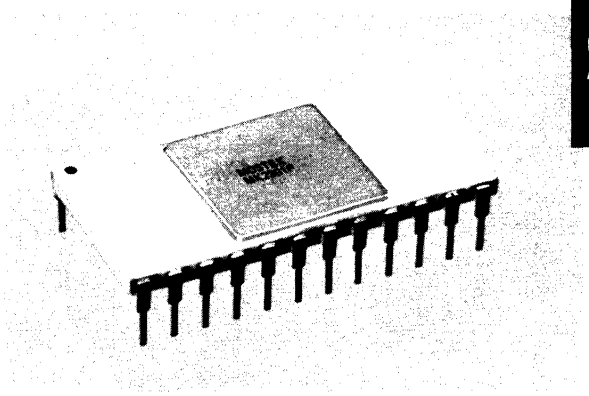
MOSTEK

FEATURES

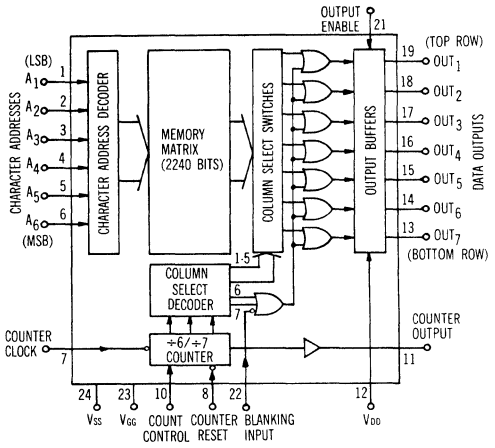
- ☐ Ion-implantation processing for full TTL/DTL compatibility
- ☐ 2240 bits of storage organized as 64 5x7 dot matrix characters with column-by-column output
- ☐ MK 2302 P is pre-programmed with ASCII encoding
- ☐ Internal counter provides clocked column selection
- ☐ Counter output for updating external character address registers
- ☐ Internal provision for one- or two-column intercharacter spacing
- ☐ Output enable and blanking capability
- ☐ Operates from +5V and —12V supplies

APPLICATIONS

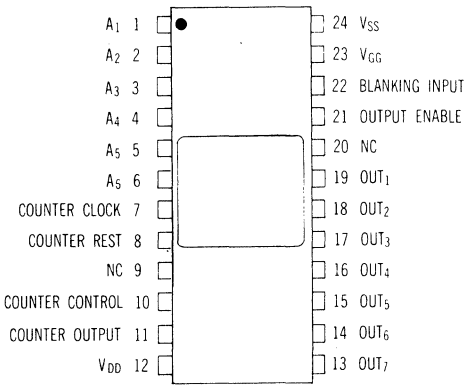
- ☐ CRT alphanumeric displays
- ☐ Light-Emitting Diode (LED) array driver
- ☐ Billboard and stock market displays



FUNCTIONAL DIAGRAM



PIN CONNECTIONS



NC = NO CONNECTION

DESCRIPTION

The MK 2300 P Series MOS, TTL / DTL-compatible read-only memories (ROMs) are designed specifically for dot-matrix character generation. Each ROM provides 2240 bits of programmable storage, organized as 64 characters each having 5 columns of 7 bits. A row output capability for 64 7x10 characters is possible, as illustrated on the back page.

Low threshold-voltage processing, utilizing ion-implantation, is used with P-channel, enhancement-mode MOS technology to provide direct input/output interface with TTL and DTL logic families. All inputs are protected to prevent damage from static charge accumulation.

The MK 2302 P is preprogrammed with ASCII-encoded characters (font shown on back page). Other ROMs in the series are programmed during manufacture to customer specifications by modification of a single mask.

Characters are selected by a six-bit binary word at the Character Address inputs. Each character consists of five columns, the columns selected by an internal counter which is clocked by the Counter Clock input. Column information appears sequentially beginning with the left-most column. Two additional intercharacter spacing columns are available, selectable for one or two spaces by the Count Control Input. During spacing, the Data Outputs are high (+5V), or the "dot-off" condition. After the last space, the modulo counter automatically increments to the leftmost column.

Synchronizing other system components with the ROM is possible using the Counter Reset Input to reset the counter to the last intercharacter spacing column, or using the Counter Output which occurs only on the last spacing column.

The Blanking Input allows all Data Outputs to be driven high (+5V) without affecting any other ROM functions. The Output Enable input allows the outputs to be open-circuited for wire-ORing.

Memory operation is static; refresh clocks are not required to maintain output information. The Counter Clock input is used only to select columns and need not be pulsed continuously.

ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} ..... +0.3V to −20V
Operating temperature range ..... 0°C to +75°C
Storage temperature range ..... −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage	+4.75	+5.0	+5.25	V	
	V_{DD}	Supply voltage	—	0.0	—	V	See note 1
	V_{GG}	Supply voltage	−12.6	−12.0	−11.4	V	
INPUTS	$V_{in(0)}$	Input voltage, logic "0"			+0.6	V	See note 2
	$V_{in(1)}$	Input voltage, logic "I"	$V_{SS}-1.5$			V	Count control input should be returned to V_{GG} for ÷ 6 operation, or V_{SS} for ÷ 7 operation
	$V_{in(cc)}$	Count Control input voltage, ÷ 6		−12.0	−11.4	V	
		÷ 7	+4.75	+5.0		V	
COUNTER TIMING	f_{clk}	Counter Clock input frequency	0		200	kHz	
	$t_{clk(0)}$	Clock time at logic "0"	2			μs	
	$t_{clk(1)}$	Clock time at logic "I"	2			μs	See timing diagrams
	$t_{r(clk)}$	Clock rise time			0.1	μs	
	$t_{f(clk)}$	Clock fall time			0.1	μs	
	t_{rp}	Reset pulse width	1.0			μs	
	t_{crd}	Clock-to-reset pulse delay	0.4			μs	See note 4

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5.0V ±0.25V, V_{GG} = −12.0V ±0.6V, $0°C \leq T_A \leq +75°C$, unless noted otherwise)

		PARAMETER	MIN	TYP*	MAX	UNITS	CONDITIONS
POW	I_{SS}	Supply current (V_{SS})		20	40	mA	Outputs unconnected
	I_{GG}	Supply current (V_{GG})		20	40	mA	f_{clk} = 200 kHz
INPUTS	C_{in}	Input capacitance			10	pF	$V_{in}=V_{SS}$, f_{meas} = 1MHz
	I_{in}	Input leakage current			10	μA	$V_{in}=V_{SS}-6V$, $T_A=25°C$
							See note 2
OUTPUTS	$V_{out(0)}$	Output voltage, logical "0"		0.2	0.4	V	I_{out} = 2.0 mA (into output)
	$V_{out(1)}$	Output voltage, logical "I"	2.4			V	I_{out} = 0.6 mA (out of output)
							See note 3
	I_{out}	Data Output leakage current	−10		+10	μA	$V_{SS}-6V \leq V_{out} \leq V_{SS}$, $T_A=25°C$ (outputs disabled)
DYNAMIC CHARACTERISTICS	t_{AO}	Address-to-output delay time			1	μs	
	t_{CO}	Clock-to-output delay time			1	μs	
	t_{CCO}	Clock-to-counter output delay time			1	μs	Rise and fall times included in delay times — See timing diagrams
	t_{BO}	Blanking/unblanking delay time			1	μs	
	t_{OEO}	Output enable/disable delay time			1	μs	
	t_{CRO}	Counter reset delay time			1	μs	R_L = 4 kΩ to V_{SS}
	t_{CRCO}	Reset-to-counter output delay time			1	μs	C_L = 15 pF to V_{DD}
	t_F	Output fall time			0.3	μs	T_A = 25°C
	t_R	Output rise time			0.3	μs	

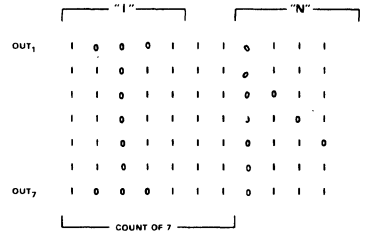
*Typical values apply at V_{SS} = +5.0V, V_{GG} = −12.0V, T_A = 25°C

NOTES:
1. Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., V_{SS} = 0V, V_{DD} = −5V, V_{GG} −17V. Input voltages would also need to be adjusted accordingly.
2. These parameters apply to the character address, counter clock, counter reset, blanking, and output enable inputs.
3. These parameters apply to both the data outputs and counter output.
4. The counter clock must not make a negative transition within the period tcrd, before or after a positive counter reset transition. The counter reset negative edge may occur any time.

TIMING

(waveforms not to scale)

Timing diagram (1) shows the time relationships between character address, data output, counter clock, and counter output during typical operation of an MK 2300 P Series character generator. An output sequence from the MK 2302 P is shown to help clarify operation. This sequence can be seen from the top rows (OUT_1) of the characters "I" and "N".



All timing relationships shown in diagram (1) apply to any other output or combination of characters as well.

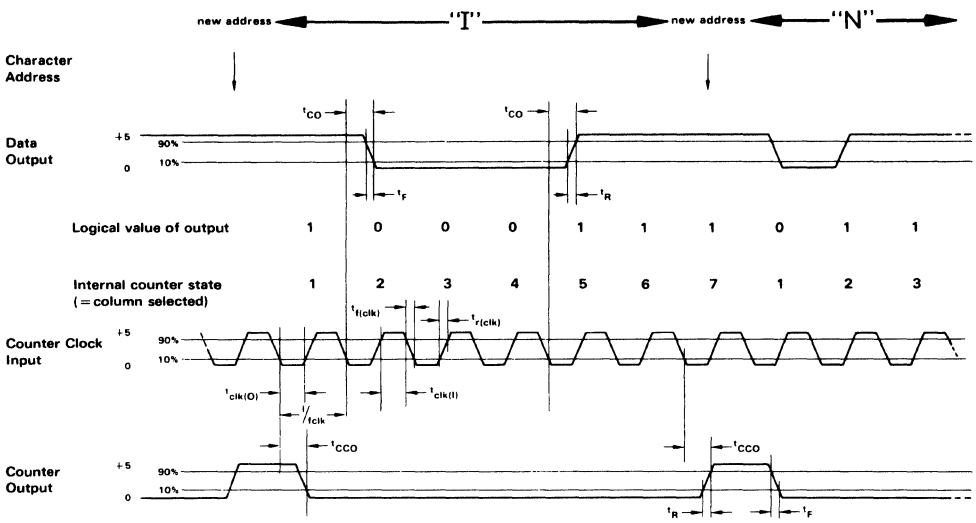
Relevant input conditions assumed but not shown in timing diagram (1) are as follows:

Count Control,	+5V
Counter Reset,	+5V
Blanking Input,	+5V
Output Enable,	+5V

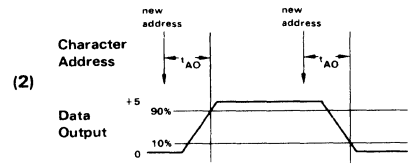
Had the Count Control input been at −12V, the counter sequence would have been six positions instead of seven and the Counter Output would have been high during the sixth position.

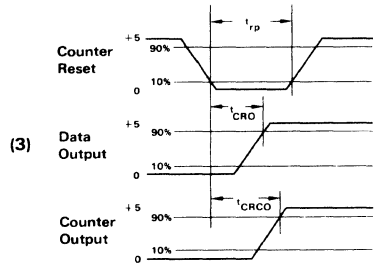
New character addresses are shown coinciding with the rising edge of the Counter Output waveform in diagram (1). This condition was selected to demonstrate use of the Counter Output to advance an external input register to a new character address. Character addresses can be changed at any other time as well. Timing diagram (2) depicts output response to a character address change when, for example, the counter is stationary in one of the five character column positions.

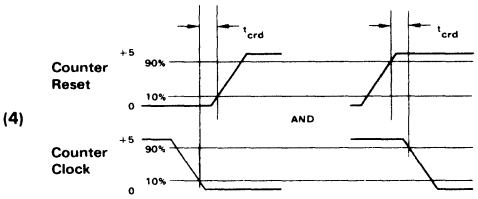
Timing diagrams (3) through (6) show timing relationships for the Counter Reset, Blanking Input, and Output Enable. The "open" condition in (6) implies that both the pull-up and pull-down devices in each data output push-pull buffer are turned off.

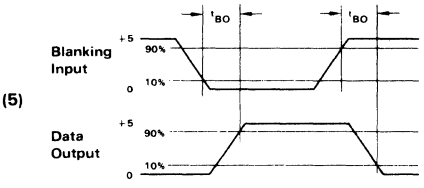


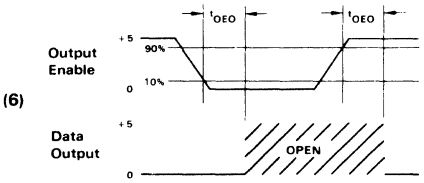
(1)











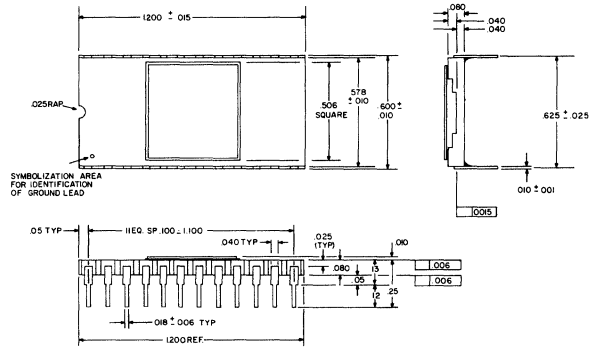
OPERATING NOTES

The following table summarizes the MK 2300 P Series input control states and corresponding drive levels:

Count Control	
÷6	−12V
÷7	+5V
Counter Reset	
operate	+5V
reset	0V
Blanking Input	
unblank	+5V
blank*	0V
Output Enable	
enable	+5V
disable**	0V

*All data outputs high (+5V)
**All data outputs open-circuited

PHYSICAL DESCRIPTION (24 lead ceramic dual-in-line hermetic package)

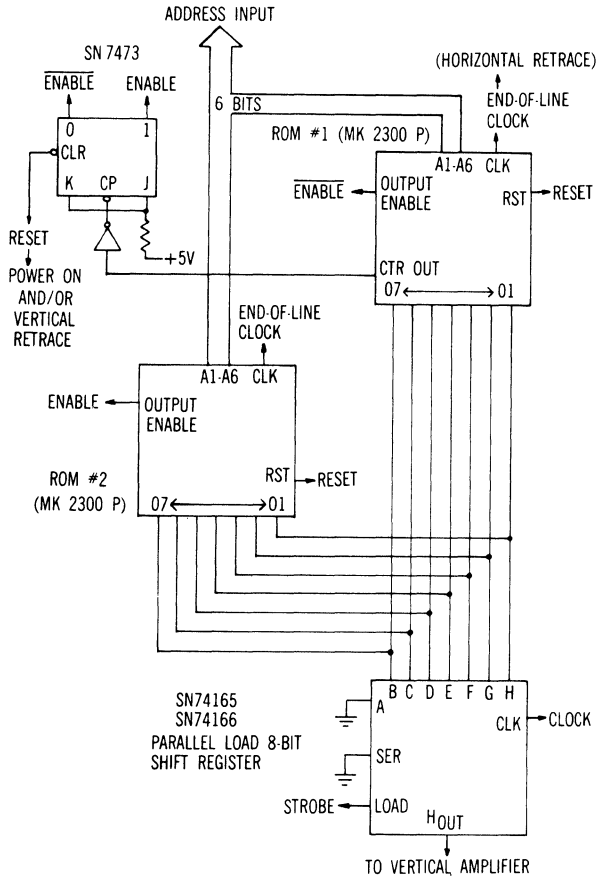


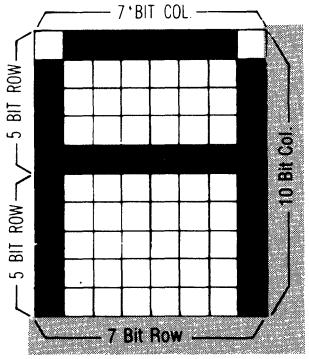
APPLICATION: 7x10 CHARACTER GENERATOR

ROM CODING

7x10 Non-Interlace Configuration: (As illustrated) For row-out (7-bit) horizontal raster-scan application, code ROM #1 for Rows 1 through 5; and ROM #2 for Rows 6 through 10.

7x10 Interlace (525-line): Code ROM #1 for Rows 1, 3, 5, 7, 9; Code ROM #2 for Rows 2, 4, 6, 8, 10. The Enable Flip-flop should be changed to clock only at vertical retrace time, thus allowing ROM #1 to be enabled for the 1st page sweep (262 ½ lines) and then allowing ROM #2 to be enabled for the interlaced 2nd page sweep of 262 ½ lines.



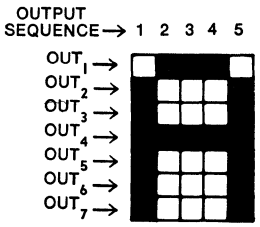


Combining two 5x7 column-output ROMs provides a 7x10 row output.

MK 2302 P

Logic 1 = input @ +5V
Logic 0 = input @ 0V

Output dot "on" = 0V
Output dot "off" = +5V



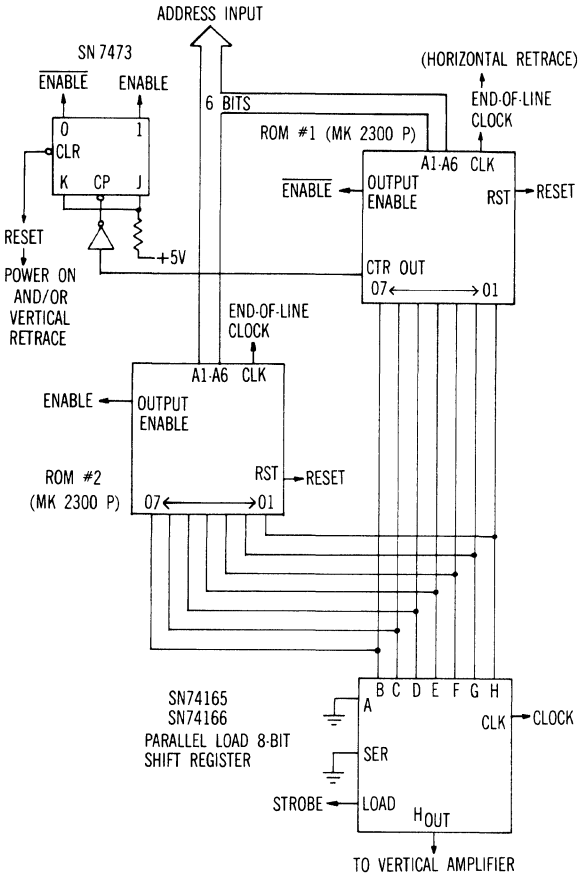
A_4	A_3	A_2	A_1	A_6 1 1 0 0 / A_5 0 1 0 1
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

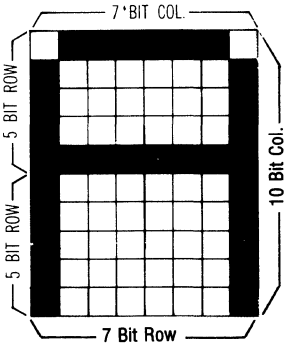
APPLICATION: 7x10 CHARACTER GENERATOR

ROM CODING

7x10 Non-Interlace Configuration: (As illustrated) For row-out (7-bit) horizontal raster-scan application, code ROM #1 for Rows 1 through 5; and ROM #2 for Rows 6 through 10.

7x10 Interlace (525-line): Code ROM #1 for Rows 1, 3, 5, 7, 9; Code ROM #2 for Rows 2, 4, 6, 8, 10. The Enable Flip-flop should be changed to clock only at vertical retrace time, thus allowing ROM #1 to be enabled for the 1st page sweep (262 ½ lines) and then allowing ROM #2 to be enabled for the interlaced 2nd page sweep of 262 ½ lines.



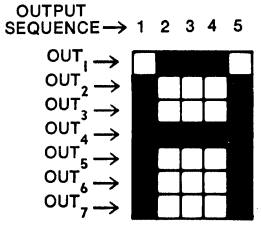


Combining two 5x7 column-output ROMs provides a 7x10 row output.

MK 2302 P

Logic 1 = input @ +5V
Logic 0 = input @ 0V

Output dot "on" = 0V
Output dot "off" = +5V



A_4	A_3	A_2	A_1	A_6 1 1 0 0 / A_5 0 1 0 1
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2300 P

Cols. Information Field

First Card

1-30 Customer
31-50 Customer Part Number
60-72 Mostek Part Number[2]

Second Card

1-30 Engineer at Customer Site
31-50 Direct Phone Number for Engineer

Third Card

1-5 Mostek Part Number[1]
10-15 Organization[2]

Fourth Card

1-6 Data Format[3] — "MOSTEK"
15-28 Logic[4] — "Positive Logic" or
35-57 Verification Code[5]

Data Cards [4]

1-6 Binary Address
8-12 First row of character
14-18 Second row of character
20-24 Third row of character
26-30 Fourth row of character
32-36 Fifth row of character
38-42 Sixth row of character
44-48 Seventh row of character

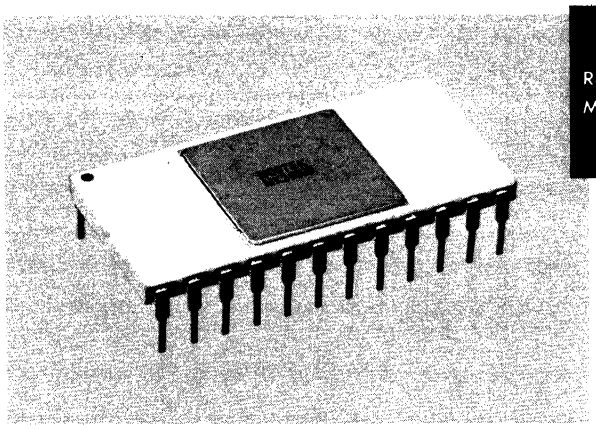
Notes: 1. Assigned by Mostek Marketing Department; may be left blank.

2. Punched as 64x5x7.
3. "MOSTEK" format only is accepted on this part.
4. A dot "ON" should be coded as a "1".
5. Punched as: (a) VERIFICATION HOLD — i.e. the customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.

2560 BITS (256x10)

MOS Read Only Memory

MOSTEK



FEATURES

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Chip enable permits wire-ORing
- ☐ Custom-programmed memory requires single mask modification
- ☐ 550 ns cycle time ($0° \leq T_A \leq 75°C$)
- ☐ Static output storage latches
- ☐ Optional 3-bit, chip-select decoder available
- ☐ 2560 bits of storage, organized as 256 10-bit words
- ☐ Operates from +5V and −12V supplies

APPLICATIONS

- ☐ Look-up table
- ☐ Code converter
- ☐ Stroke character generator
- ☐ Dot-matrix character generator

DESCRIPTION

The MK 2400 P Series TTL/DTL-compatible MOS Read-Only Memories (ROM's) are designed for a wide range of general-purpose memory applications where large quantity bit storage is required. Each ROM provides 2560 bits of programmable storage, organized as 256 words of 10 bits each. Low threshold-voltage processing, utilizing ion implantation with P-channel enhancement-mode MOS technology, provides direct input/output interface with TTL and DTL logic.

Programming is accomplished during manufacture by modification of a single mask, according to customer specifications. The MK 2400 P Series is available in either 24-lead or 28-lead ceramic dual-in-line packages. On the 28-pin ROM, an optional Chip Select Decoder may also be programmed according to customer specifications to provide a 3-bit Chip Select Code.

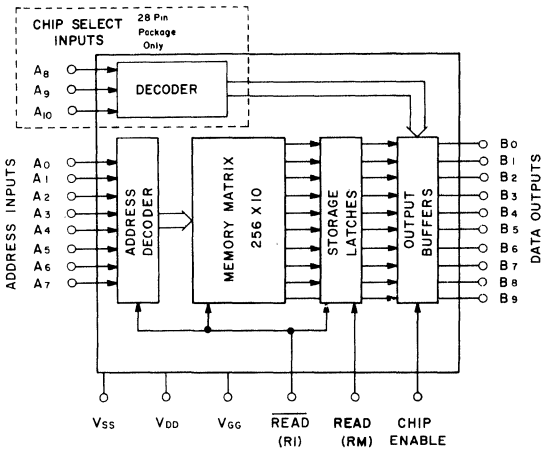
Operation involves transferring addressed information from the memory matrix into the storage latches using the READ and $\overline{\text{READ}}$ inputs (see Timing). Information stored in the latches will remain despite address changes or chip disabling until the READ and $\overline{\text{READ}}$ inputs are again cycled. READ and $\overline{\text{READ}}$ input signals may be generated from separate timing circuits if desired, or either may be the inverse of the other.

The Chip Enable input forces the normally push-pull output buffer stages to an open-circuit condition when disabling the chip. If desired, new data can be stored in the storage latches while the chip is disabled. When the chip is re-enabled, this data would be present at the outputs.

All inputs are protected against static charge accumulation. Pull-up resistors on all inputs are available as a programmable option.

For additional information regarding custom programming and coding sheets, contact your nearest Mostek representative.

FUNCTIONAL DIAGRAM



OPERATING NOTES

CHIP ENABLE	READ	$\overline{\text{READ}}$	OUTPUT
0	X	X	A
1	0	1	B
1	1	0	C

"1" = V_{SS} (+5V); "0" = V_{DD} (0V)

X = No effect on output

A = Output open-circuited

B = Output retains data last stored in latches

C = Output assumes state of addressed cells

ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} ..... +0.3V to −10V
Operating temperature range ..... 0°C to +75°C
Storage temperature range ..... −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 75°C$)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{SS}	Supply voltage	+4.75	+5.0	+5.25	V	
	V_{DD}	Supply voltage	—	0.0	—	V	See note 1
	V_{GG}	Supply voltage	−12.6	−12.0	−11.4	V	
INPUTS	$V_{in(o)}$	Input voltage, logic "0"		0	+0.8	V	Pull-up resistors (≈5KΩ) to
	$V_{in(l)}$	Input voltage, logic "1"	$V_{SS}-1.5$	V_{SS}		V	V_{SS} available as programmable option.
INPUT TIMING	t_{cyc}	Address change cycle time	550			ns	See Timing Section
	t_{ld}	Address to $\overline{\text{Read}}$ lead time	250			ns	
	t_{lg1}	Read lag time 1	−.05		.05	μs	
	t_{lg2}	Read lag time 2	−.05		.05	μs	
	$t_{\overline{rd}}$	$\overline{\text{Read}}$ pulse width	300			ns	
	t_{rd}	Read pulse width	0.3		100	μs	
	t_r	Rise time, any input			100	ns	
	t_f	Fall time, any input			100	ns	

ELECTRICAL CHARACTERISTICS ($V_{SS}= +5.0V \pm 0.25V$, $V_{GG}= -12.0V \pm 0.6V$, $0°C \leq T_A \leq +75°C$, unless noted otherwise. Pull-up resistors not programmed.)

		PARAMETER	MIN	TYP*	MAX	UNITS	CONDITIONS
POWER	I_{SS}	Supply current (V_{SS})		12	25	mA	Outputs unconnected
	I_{GG}	Supply current (V_{GG})		−12	−25	mA	See Note 2 and Note 3
INPUTS	C_{in}	Input capacitance		5	10	pF	$V_{in}=V_{SS}$, $f_{meas}=$ 1MHz
	I_{in}	Input leakage current			10	μA	$V_{in}=V_{SS}-6V$ $T_A=25°C$
OUTPUTS	$V_{out(o)}$	Output voltage, logical "0"			0.4	V	$I_{out}=1.6$ mA (into output)
	$V_{out(l)}$	Output voltage, logical "1"	2.4			V	$I_{out}=0.4$ mA (out of output)
							$V_{SS}-6V \leq V_{out} \leq V_{SS}$
	I_{out}	Output leakage current	−10		+10	μA	$T_A=25°C$ (outputs disabled)
							See note 3 and Figure #1
DYNAMIC CHARACTERISTICS	t_{ACC}	Address-to-output access time			600	ns	$t_{ld}=250$ns, $t_{lg1}=0$, $t_{lg2}=0$, See note 4 — See timing Section and Figure #1
	t_{OD}	Output delay time			350	ns	
	t_{OEO}	Output enable/disable time		125	300	ns	
	t_{CS}	Chip Select to Output Delay			600	ns	
	t_{CD}	Chip Deselect to Output Delay			600	ns	

*Typical values apply at $V_{SS}= +5.0V$, $V_{GG}= -12.0V$, $T_A=25°C$

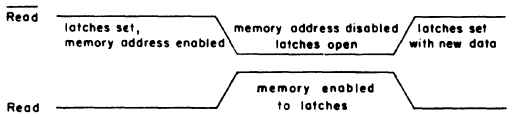
NOTES:
1. Supply voltages shown are for operation in a TTL/DTL system. Other supply voltages may be used if V_{DD} and V_{GG} maintain the same relationship to V_{SS}, e.g., $V_{SS}=0V$, $V_{DD}= -5V$, $V_{GG}=-17V$. Input voltages would also need to be adjusted accordingly.
2. Max measurements at 0°C. (MOS supply currents increase as temperature decreases.) I_{SS} will increase 1.6mA (max) for each input at logic 0 when pull-up resistors are programmed.
3. Unit operated at minimum specified cycle time.
4. The outputs become open circuited when disabled or deselected. As shown in Fig. 1, an output with a "1" expected out does not transition through the 1.5V point when enabled (selected) or disabled (deselected); this is true because the TTL equivalent load pulls the open-circuited output to approximately 2 volts.

TIMING

Notes:

1. All times are referenced to the 1.5V point relative to V_{DD} (ground) except rise and fall time measurements.
2. Chip enable = V_{SS} for all measurements except when measuring T_{OEO}.
3. Logic 0 is defined as V_{DD} or ground; logic 1 as V_{SS} or +5V.

INTERNAL FUNCTION OF READ/$\overline{\text{READ}}$ SIGNALS

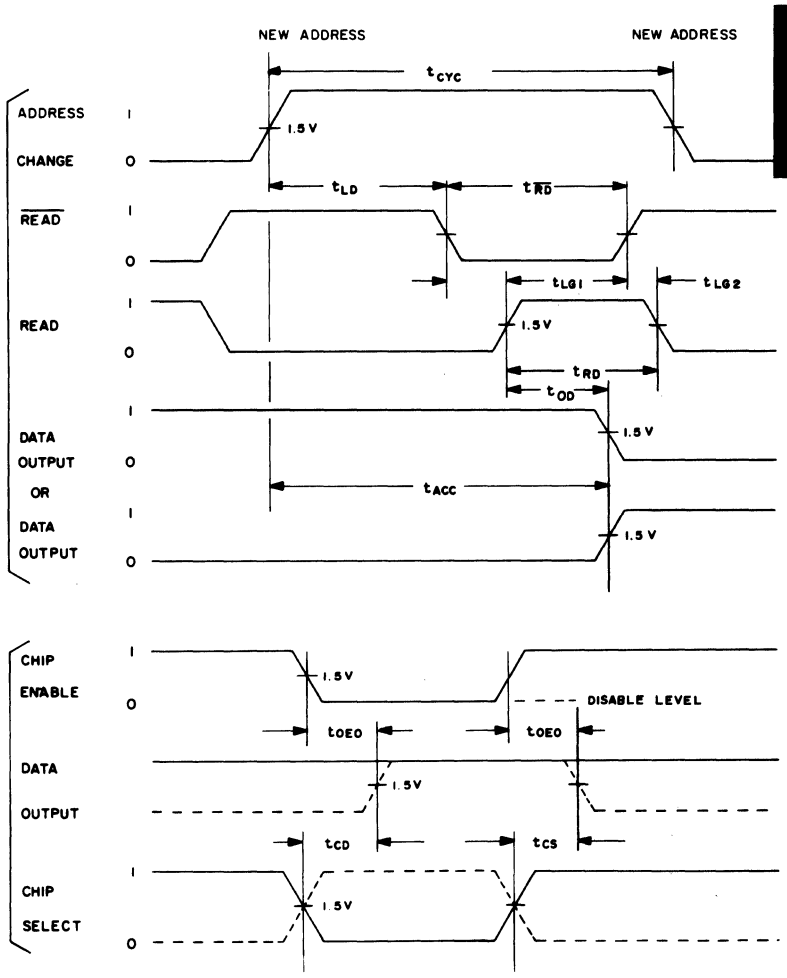


Set up time, t_{id}, allows the input address to propagate through the address decoder and memory matrix prior to $\overline{\text{READ}}$ logic 0 time. As indicated above, $\overline{\text{READ}}$ at a logic 0 internally disables the input address so that an external address change may occur without affecting the location previously selected. The latches are also readied to receive new data which is enabled from the matrix when $\overline{\text{READ}}$ is at a logic 1. Data is set in the latches when READ is allowed to rise back to its logic 1 state. In actual use, the READ rising and falling edges can precede the falling and rising edges of $\overline{\text{READ}}$, respectively, as implied by the specification of negative read lag times. This allows a very flexible timing relation between the two pulses, in that either input can be the inversion of the other or both may be generated from separate timing circuits.

Output data appears following the rise of the READ pulse but correct output data will not appear until $\overline{\text{READ}}$ has gone low. For this reason, $\overline{\text{READ}}$ is shown preceding READ even though other relationships are allowed. If READ is made to precede $\overline{\text{READ}}$, delay time, t_{OD}, should be referenced to the fall of $\overline{\text{READ}}$ rather than as shown.

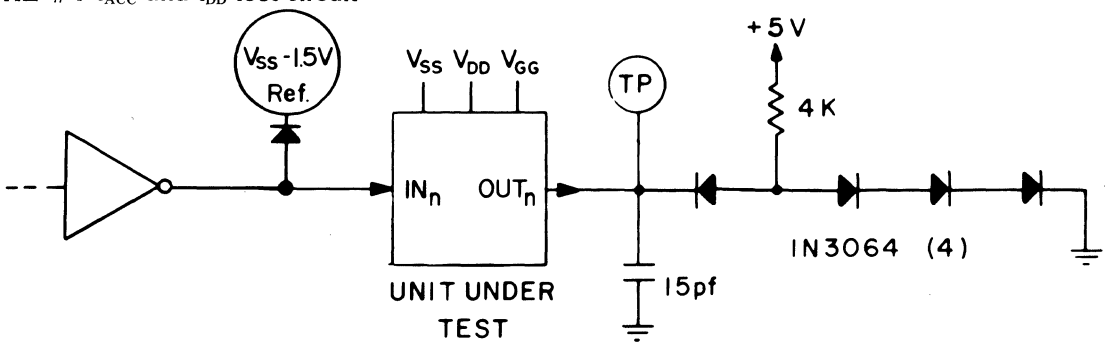
The chip is disabled by applying a logical 0 to the chip enable input, forcing the outputs to an open-circuit condition. The output data present at the time of disable will again be present upon re-enabling unless a new read cycle was initiated for a different address while the chip was disabled, in which case the new data would be present at the outputs.

The programmable 3-bit chip select timing would be the same as the address inputs.

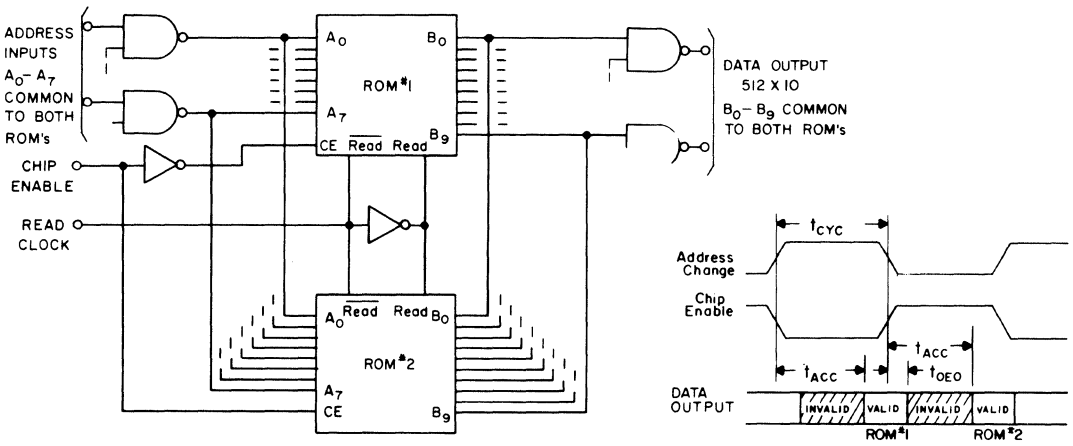


NOTE: Wave forms are not to scale.

FIGURE #1 t_{ACC} and t_{DD} test circuit



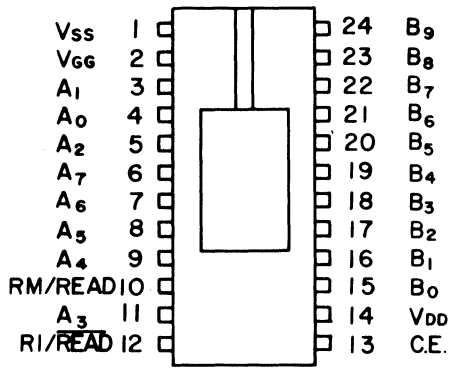
APPLICATIONS



Application shows wire-Or'ing for expansion to a 512 X 10 memory. Further expansion is possible by 1 of N decoding to the Chip Enable input (or with the optional 3-bit decoder) while maintaining the time relationships shown. t_{cyc} should include the desired data-valid time. Interface devices may be TTL or DTL.

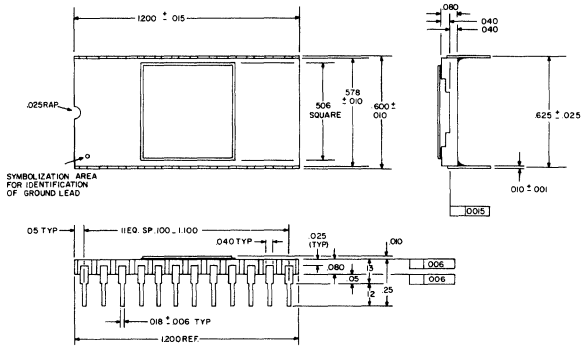
PIN CONNECTIONS

top view, 24 pin CDIP



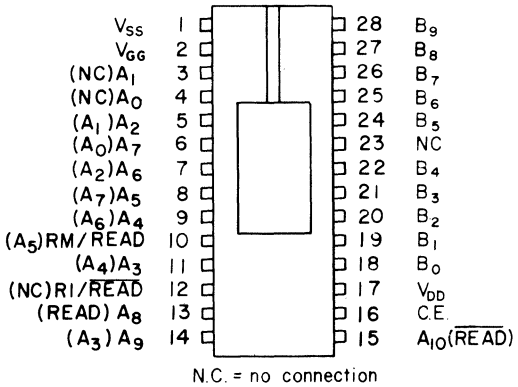
PHYSICAL DESCRIPTION

(24 lead ceramic dual-in-line hermetic package)



PIN CONNECTIONS

top view, 28 pin CDIP

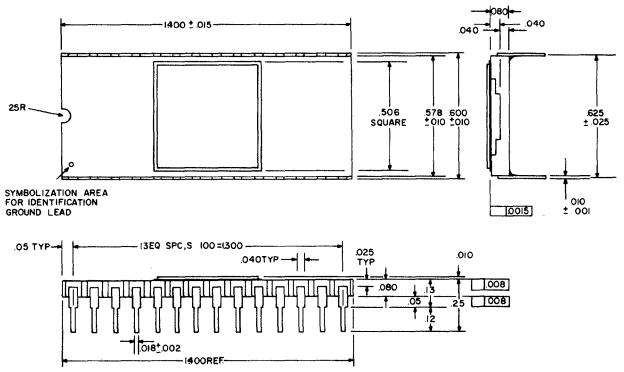


N.C. = no connection

( ) OPTIONAL PIN ARRANGEMENT

PHYSICAL DESCRIPTION

(28 lead ceramic dual-in-line hermetic package)



MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2400 P

Cols.	Information Field
First Card	
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]
Second Card	
1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer
Third Card	
1-5	Mostek Part Number[2]
10-16	Organization[3]
29	A8[4]
30	A9[4]
31	A10[4]
32	Pull-up Resistor[5]
Fourth Card	
0-6	Data Format[4] — "MOSTEK"
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]
60-74	Package Choice[8]
Data Cards	
1-3	Decimal Address
5	Output B9
6	Output B8
7	Output B7
8	Output B6
9	Output B5
10	Output B4
11	Output B3
12	Output B2
13	Output B1
14	Output B0
16	Octal Equivalent of: B9[9]
17	Octal Equivalent of: B8, B7, B6[9]
18	Octal Equivalent of: B5, B4, B3[9]
19	Octal Equivalent of: B2, B1, B0[9]

Notes:

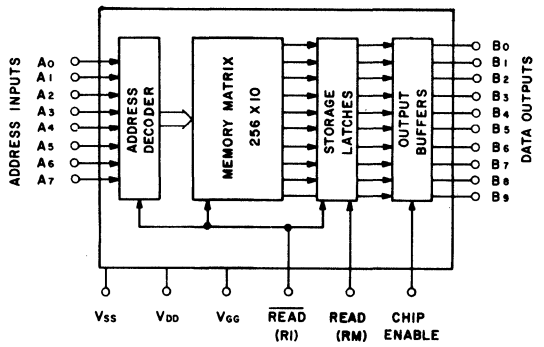
1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by Mostek Marketing Department; may be left blank.
3. Punched as 0256x10.
4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.
5. A "1" indicates pull-ups; a "0" indicates no pull-ups.
6. "MOSTEK" format only is accepted on this part.
7. Punched as:
   (a) VERIFICATION HOLD — i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.
8. "24 PIN", "28 PIN STANDARD", or "28 PIN OPTIONAL" (left justified to column 60).
9. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 1010011110 would be separated into groups 1/010/011/110 and the resulting octal equivalent number is 1236.

2560 Bit

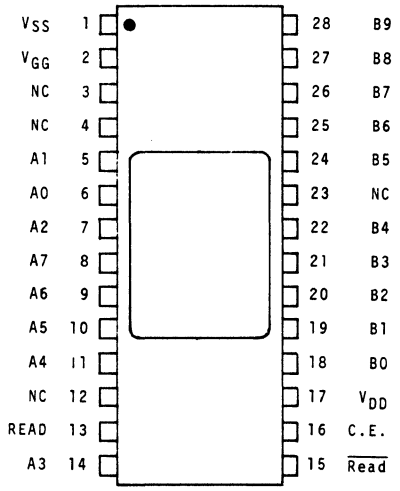
MOS Read-Only Memory Character Generator

MOSTEK

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



NC= NO CONNECTION

DESCRIPTION

The MK 2408 P is a pre-programmed member of the MK 2400 P Series. It is programmed as a dot-matrix character generator (64 characters) with ASCII encoded inputs and row (5-bit) outputs. The MK 2408 P outputs two rows at the same time. Row 1 is available at outputs B9 (left), B8, B7, B6, and B5 (right) while row 2 is available at outputs B4 (left), B3, B2, B1, and B0 (right). Row 3 is available at B9 through B5 while row 4 is available at B4 through B0. Row 5 and row 6 are available at B9 through B5 and B4 through B0. Row 5 and row 6 are available at B9 through B5 and B4 through B0. Row selection is determined by the address combination of bits A0 and A1.

The MK 2408 P meets and operates by the specifications outlined in the MK 2400 P Series data sheet (DS-24001270-2)

The example in Figure 1 demonstrates the correspondence of the device outputs and row select sequence to the 7 x 5 dot-matrix font. The complete character font patterns (truth table) are illustrated on the back. A logic 1 or a DOT represents an input or output voltage equal to V_{SS} (+5V) and a logic 0 or a blank represents a voltage equal to V_{DD} (OV). The eighth row outputs (B4 through B0 when inputs A1 and A0 equal logic 1) are not illustrated since in each case they are equal to all 0's.

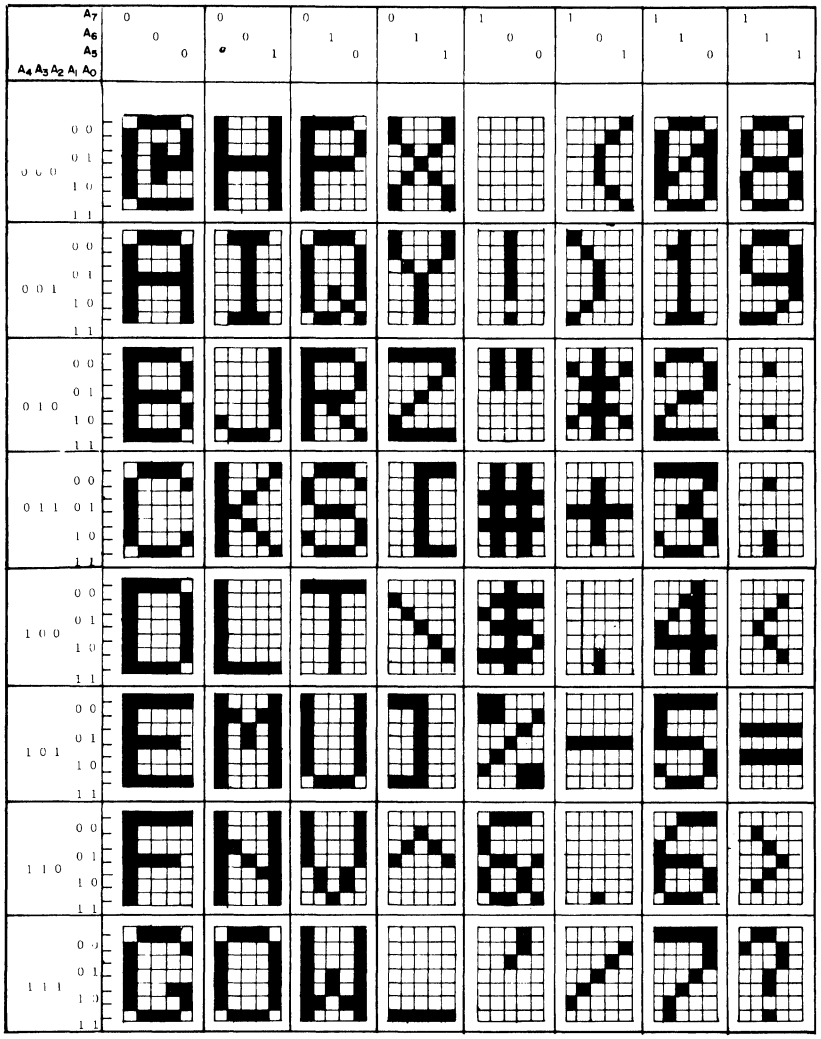
A1	A0	B9 B4	B8 B3	B7 B2	B6 B1	B5 B0	
0	0	1	0	0	0	1	-- B9-B5
		1	1	0	1	1	-- B4-B0
0	1	1	0	1	0	1	-- B9-B5
		1	0	1	0	1	-- B4-B0
1	0	1	0	0	0	1	-- B9-B5
		1	0	0	0	1	-- B4-B0
1	1	1	0	0	0	1	-- B9-B5
		0	0	0	0	0	-- B4-B0

A7 = 0
A6 = 0
A5 = 1

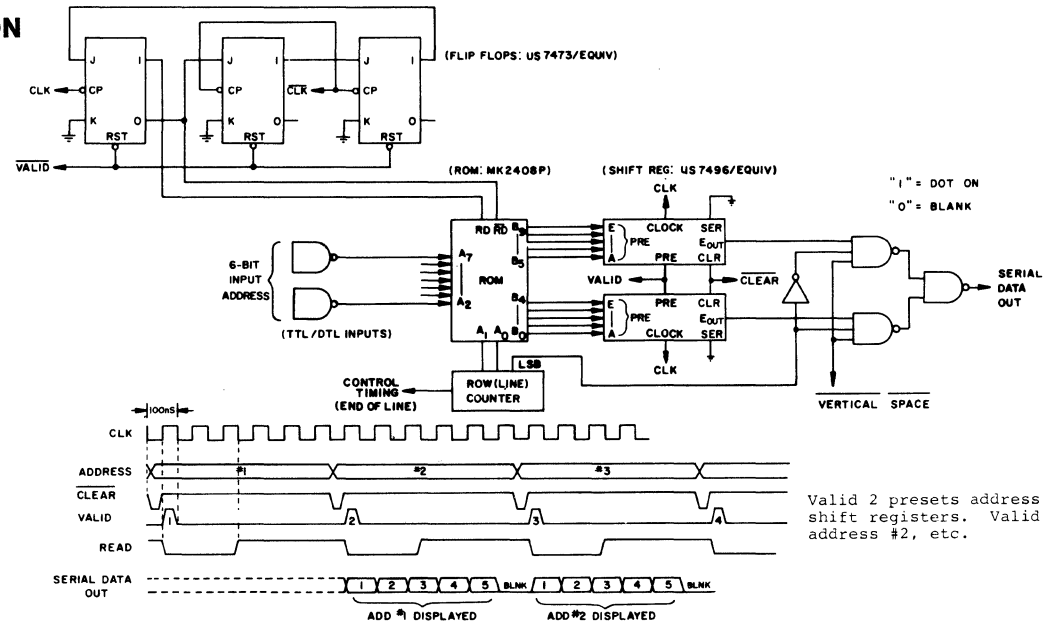
A4 = 1
A3 = 0
A2 = 1

FIGURE 1

CODING & CHARACTER FONTS



APPLICATION



Valid 2 presets address #1 data in shift registers. Valid 3 presets address #2, etc.

MK 2500 P
MK 2600 P

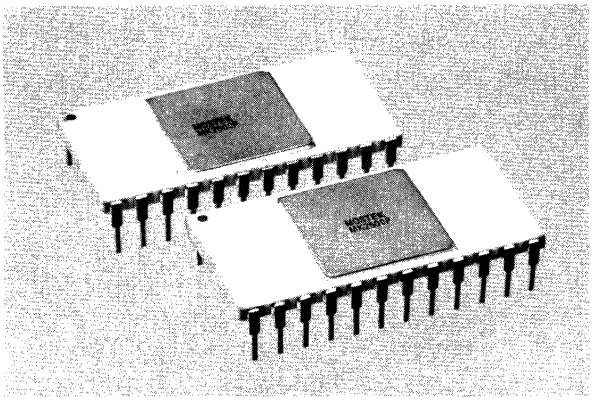
4096-BIT
MOS Read-Only Memory

MOSTEK

Read Only Memories

FEATURES

- ☐ High-speed, static operation — 400 nsec. typical access time
- ☐ Active input pull-ups provide worst-case TTL compatibility
- ☐ Push-pull outputs provide three output states: one, zero, and open
- ☐ Ion-implantation for constant current loads and lower power
- ☐ Standard power supplies: +5V, —12V
- ☐ MK 2500 P is pin-for-pin replacement for National 5232
- ☐ MK 2600 P is pin-for-pin replacement for Fairchild 3514



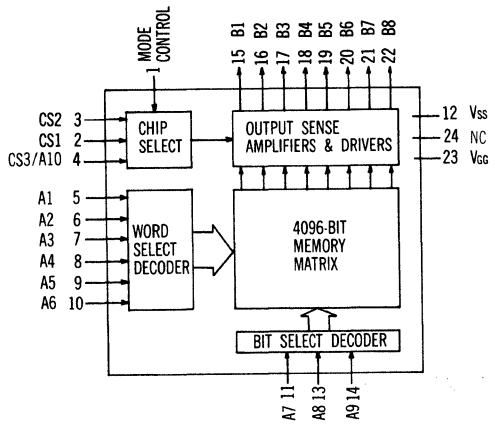
DESCRIPTION

The MK 2500 P and MK 2600 P series of TTL/DTL compatible MOS read-only memories (ROMs) are designed to store 4096 bits of information by programming one mask pattern. The word and bit organization of these ROM series is either 512W X 8B or 1024W X 4B.

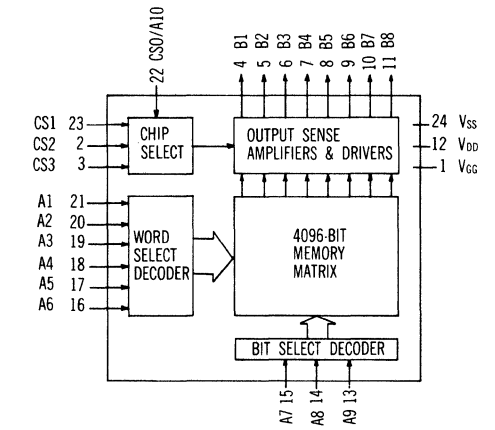
The MK 2500/2600 P series has push-pull outputs that can be in one of three states: logic one, logic zero, or open or unselected state. This, plus the programmable Chip Selects, enables the use of several ROMS in parallel with no external components. Since the ROM is a static device, no clocks are required, making the MK 2500/2600 P series of ROMS very versatile and easy to use.

Low threshold-voltage processing, utilizing ion-implantation, is used with P-channel, enhancement-mode MOS technology to provide direct input/output interfacing with TTL and DTL logic families. All inputs are protected to prevent damage from static charge accumulation.

FUNCTIONAL DIAGRAMS



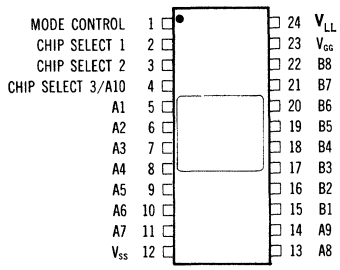
MK 2500P



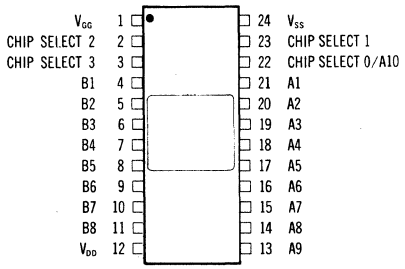
MK 2600 P

PIN CONNECTIONS

MK 2500 P



MK 2600 P



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} (except V_{GG}) ..... +0.3V to −10V
Voltage on V_{GG} Terminal Relative to V_{SS} ..... +0.3V to −20V
Operating Temperature Range (Ambient) ..... 0°C to +70°C
Storage Temperature Range (Ambient) ..... −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+4.75	+5.0	+5.25	V	
V_{DD}	Supply Voltage	——	0.0	——	V	Note 1
V_{GG}	Supply Voltage	−11.4	−12.0	−12.6	V	
V_{IL}	Input Voltage, Logic "0"			+0.8	V	
V_{IH}	Input Voltage, Logic "1"	$V_{SS}-1.5$			V	Note 2
V_{IH}	Input Voltage, Logic "1"	2.4			V	Note 3

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5.0V \pm 5\%$; $V_{DD} = 0$ V; $V_{GG} = -12V \pm 5\%$; $0°C \leq T_A \leq 70°C$ unless noted otherwise)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{SS}	Supply Current, V_{SS}		19.0	28.0	mA	Note 4
I_{GG}	Supply Current, V_{GG}		19.0	28.0	mA	Note 4
$I_{I(L)}$	Input Leakage Current, Any Input			10.0	μA	$V_I = V_{SS}-6.0V$. Note 2
I_{IL}	Input Current, Logic 0, Any Input			−100.0	μA	$V_I=.4V$. Note 3
I_{IH}	Input Current, Logic 1, Any Input			−600.0	μA	$V_I=2.4V$. Note 3
V_{OL}	Output Voltage, Logic "0"			0.4	V	$I_{OL}=1.6mA$
V_{OH}	Output Voltage, Logic "1"	2.4			V	$I_{OH}=-40\mu A$
$I_{O(L)}$	Output Leakage Current			+10	μA	Outputs disabled ($V_O=V_{SS}-6V$)
C_{IN}	Input Capacitance			10	pF	Note 5
C_O	Output Capacitance			10	pF	Note 5
t_{ACCESS}	Address to Output Access Time	100	400	700	nsec	Refer to
t_{CS}	Chip Select to Output Delay	100	250	500	nsec	Test
t_{CD}	Chip Deselect to Output Delay	100	250	800	nsec	Note 6 Circuit

Notes: 1. This is V_{LL} on MK2500P.

2. This parameter is for inputs without active pull-ups (programmable).

3. This parameter is for inputs with active pull-ups (programmable) for TTL interfaces. As the TTL driver goes to a logic 1 it must only provide 2.4V (this voltage must not be clamped) and the circuit pulls the input to V_{SS}. Refer to the Input pull-up figure for a graphical description of the active pull-up's operation.

4. Inputs at V_{SS}, outputs unloaded.

5. $V_{Bias} - V_{SS} = OV$; $f = 1$ MHz.

6. t_{CD} is primarily dependent on the RC time constant of the load (i.e. the outputs become open circuited upon being disabled). As noted in the Timing Diagram, disabling or enabling an output with a "1" expected out does not yield a transition through the 1.5V point; this is true because the TTL equivalent load pulls the open-circuited output to approximately 2 volts.

PROGRAMMING OPTIONS

MK 2500 P

OPTIONS

Function	512 X 8	1024 X 4
Mode Control	1	0
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3/A10	1 or 0	address A10

1 = Most Positive = High Level Voltage

Pin 1 in the MK 2500 P is used as a Mode Control, setting the circuit in the 1024x4 or 512x8 mode. In the 1024x4 mode a tenth address bit is required, which is provided at Pin 4. If the circuit is in the 512x8 mode, then Pin 4 may be used for a third chip select.

Additional Options: The MK 2500 P can have the address and control inputs set by the user so that:

512x8: Mode Control — High
A10 — Low

1024x4: Mode Control — Low
A10 aid as an address
See Note 9, following page

MK 2600 P

OPTIONS

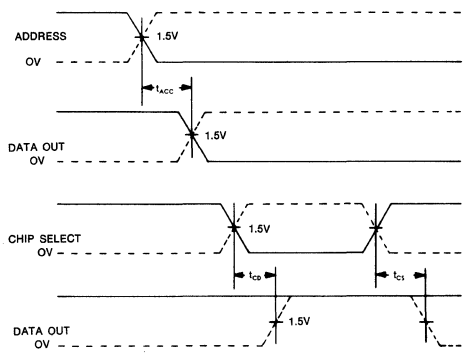
Function	512 X 8	1024 X 4
Chip Select 0/A10	1 or 0	A10
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3	1 or 0	1 or 0

1 = Most Positive = High Level Voltage

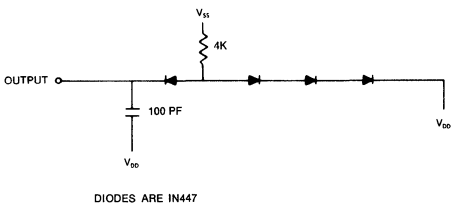
The MK 2600 P is programmed either as a 512x8 array or a 1024x4 array. In the 1024x4 arrays, Pin 22 provides the tenth address bit. When A10 is low the four bits are present at the even outputs (B2, B4, B6, and B8); when A10 is high, the bits are at the odd outputs (B1, B3, B5, and B7).

In 512x8 arrays, Pin 22 may be used to provide a fourth chip select. Thus, with four programmable chip selects, sixteen MK 2600 P ROMS in the 512x8 configuration can be arranged in an 8192x8 array requiring no external decoding.

TIMING

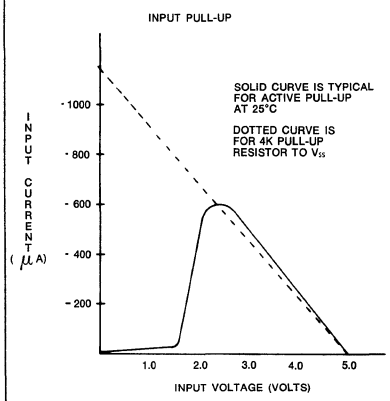


T_{ACCESS} TEST CIRCUIT

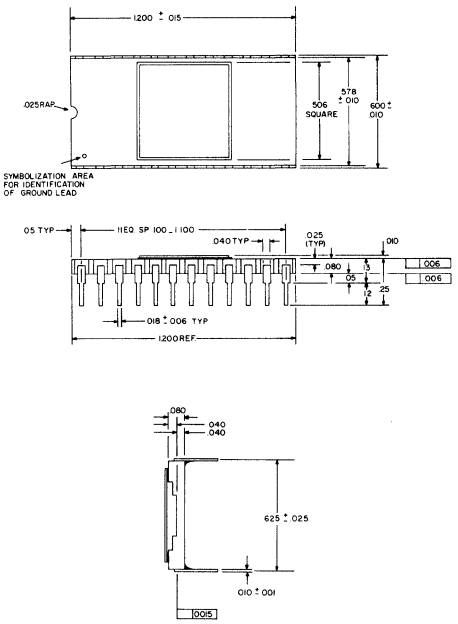


DIODES ARE IN447

INPUT



PACKAGE 24-lead ceramic dual-in-line hermatic



MOSTEK ROM PUNCHED-CARD CODING FORMAT[1]

MK 2500 P

First Card

Cols.	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	Mostek Part Number[2]
10-16	Organization[3]
29	CS3[10]
30	CS2[4]
31	CS1[4]
32	Active Pull-ups[5]

Fourth Card

1-9	Data Format[6]
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]
60-67	"A10 EVEN" or "A10 ODD" (left justified)[9]

Data Cards/512x08 Organization

1-4	Decimal Address
6-13	Output B8- B1 (MSB thru LSB)
15-17	Octal Equivalent of output data[8]

Data Cards/1024x04 Organization

1-4	Decimal Address (0-1022), even addresses
6-9	Output (MSB-LSB)
11-12	Octal Equivalent of output data[8]
50-53	Decimal Address (1-1023), odd addresses
55-58	Output (MSB-LSB)
60-61	Octal Equivalent of output data[8]

MK 2600 P

First Card

Cols.	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	Mostek Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	Mostek Part Number[2]
10-16	Organization[3]
29	CS3[4]
30	CS2[4]
31	CS1[4]
32	CS0[10]
33	Active Pull-ups[5]

Fourth Card

1-9	Data Format[6]
15-28	Logic — "Positive Logic" or "Negative Logic"
35-57	Verification Code[7]

Data Cards/512x08 Organization

1-4	Decimal Address
6-13	Output B8- B1 (MSB thru LSB)
15-17	Octal Equivalent of output data[8]

Data Cards/1024x04 Organization

1-4	Decimal Address (0-1022), even addresses
6-9	Output (MSB-LSB)
11-12	Octal Equivalent of output data[8]
50-53	Decimal Address (1-1023), odd addresses
55-58	Output (MSB-LSB)
60-61	Octal Equivalent of output data[8]

Notes:

1. Positive or negative logic formats are accepted as noted in the fourtn card.
2. Assigned by Mostek Marketing Department; may be left blank.
3. Punched as "0512x08" or "1024x04".
4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.
5. A "1" indicates active pull-ups; a "0" indicates no pull-ups.
6. MOSTEK, Fairchild, or National Punched-Card Coding Format may be used. Specify which punched card format used by punching either "MOSTEK", "Fairchild", or "National". Start name at column one.
7. Punched as: (a) VERIFICATION HOLD — i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS — i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED — i.e. the customer will not receive a CVDS and production will begin immediately.
8. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 10011110 would be separated into groups 10/011/110 and the resulting octal equivalent number is 236.
9. "A10 EVEN" and "A10 ODD" applies to the 1024 x 4 mode. "A10 EVEN" means the even outputs are enabled when A10 is high. "A10 ODD" means the odd outputs are enabled when A10 is high.
10. Punched as "2" for 1024 x 4 organization.

ASCII-TO-EBCDIC CODE CONVERTER
EBCDIC-TO-ASCII CODE CONVERTER

A_1 = LSB B_1 = LSB
A_9 = MSB B_8 = MSB

MK 2503 P

Function	512 X 8
Mode Control	1
Chip Select 1	0
Chip Select 2	0
Chip Select 3/A10	0

MK 2601 P

Function	512 X 8
Chip Select 0/A10	0
Chip Select 1	0
Chip Select 2	0
Chip Select 3	0

ASCII (ADDRESS) TO EBCDIC (DATA)

0	00000000	1	00000001	2	00000010	3	00000011	128	00100000	129	00100001	130	00100010	131	00100011
4	00110111	5	00101101	6	00101110	7	00101111	132	00100100	133	00010101	134	00000110	135	00010111
8	00010110	9	00000101	10	00100101	11	00001011	136	00101000	137	00101001	138	00101010	139	00101011
12	00001100	13	00001101	14	00001110	15	00001111	140	00101100	141	00001001	142	00001010	143	00011011
16	00010000	17	00010001	18	00010010	19	00010011	144	00110000	145	00110001	146	00011010	147	00110011
20	00111100	21	00111101	22	00110010	23	00100110	148	00110100	149	00110101	150	00110110	151	00001000
24	00011000	25	00011001	26	00111111	27	00100111	152	00111000	153	00111001	154	00111010	155	00111011
28	00011100	29	00011101	30	00011110	31	00011111	156	00000100	157	00010100	158	00111110	159	11100001
32	01000000	33	01001111	34	01111111	35	01111011	160	01000001	161	01000010	162	01000011	163	01000100
36	01011011	37	01101100	38	01010000	39	01111101	164	01000101	165	01000110	166	01000111	167	01001000
40	01001101	41	01011101	42	01011100	43	01001110	168	01001001	169	01010001	170	01010010	171	01010011
44	01101011	45	01100000	46	01001011	47	01100001	172	01010100	173	01010101	174	01010110	175	01010111
48	11110000	49	11110001	50	11110010	51	11110011	176	01011000	177	01011001	178	01100010	179	01100011
52	11110100	53	11110101	54	11110110	55	11110111	180	01100100	181	01100101	182	01100110	183	01100111
56	11111000	57	11111001	58	01111010	59	01011110	184	01101000	185	01101001	186	01110000	187	01110001
60	01001100	61	01111110	62	01101110	63	01101111	188	01110010	189	01110011	190	01110100	191	01110101
64	01111100	65	11000001	66	11000010	67	11000011	192	01110110	193	01110111	194	01111000	195	10000000
68	11000100	69	11000101	70	11000110	71	11000111	196	10001010	197	10001011	198	10001100	199	10001101
72	11001000	73	11001001	74	11010001	75	11010010	200	10001110	201	10001111	202	10010000	203	10011010
76	11010011	77	11010100	78	11010101	79	11010110	204	10011011	205	10011100	206	10011101	207	10011110
80	11010111	81	11011000	82	11011001	83	11100010	208	10011111	209	10100000	210	10101010	211	10101011
84	11100011	85	11100100	86	11100101	87	11100110	212	10101100	213	10101101	214	10101110	215	10101111
88	11100111	89	11101000	90	11101001	91	01001010	216	10110000	217	10110001	218	10110010	219	10110011
92	11100000	93	01011010	94	01011111	95	01101101	220	10110100	221	10110101	222	10110110	223	10110111
96	01111001	97	10000001	98	10000010	99	10000011	224	10111000	225	10111001	226	10111010	227	10111011
100	10000100	101	10000101	102	10000110	103	10000111	228	10111100	229	10111101	230	10111110	231	10111111
104	10001000	105	10001001	106	10010001	107	10010010	232	11001010	233	11001011	234	11001100	235	11001101
108	10010011	109	10010100	110	10010101	111	10010110	236	11001110	237	11001111	238	11011010	239	11011011
112	10010111	113	10011000	114	10011001	115	10100010	240	11011100	241	11011101	242	11011110	243	11011111
116	10100011	117	10100100	118	10100101	119	10100110	244	11101010	245	11101011	246	11101100	247	11101101
120	10100111	121	10101000	122	10101001	123	11000000	248	11101110	249	11101111	250	11111010	251	11111011
124	01101010	125	11010000	126	10100001	127	00000111	252	11111100	253	11111101	254	11111110	255	11111111

EBCDIC (ADDRESS) TO ASCII (DATA)

256	00000000	257	00000001	258	00000010	259	00000011	384	11000011	385	01100001	386	01100010	387	01100011
260	10011100	261	00001001	262	10000110	263	01111111	388	01100100	389	01100101	390	01100110	391	01100111
264	10010111	265	10001101	266	10001110	267	00001011	392	01101000	393	01101001	394	11000100	395	11000101
268	00001100	269	00001101	270	00001110	271	00001111	396	11000110	397	11000111	398	11001000	399	11001001
272	00010000	273	00010001	274	00010010	275	00010011	400	11001010	401	01101010	402	01101011	403	01101100
276	10011101	277	10000101	278	00001000	279	10000111	404	01101101	405	01101110	406	01101111	407	01110000
280	00011000	281	00011001	282	10010010	283	10001111	408	01110001	409	01110010	410	11001011	411	11001100
284	00011100	285	00011101	286	00011110	287	00011111	412	11001101	413	11001110	414	11001111	415	11010000
288	10000000	289	10000001	290	10000010	291	10000011	416	11010001	417	01111110	418	01110011	419	01110100
292	10000100	293	00001010	294	00010111	295	00011011	420	01110101	421	01110110	422	01110111	423	01111000
296	10001000	297	10001001	298	10001010	299	10001011	424	01111001	425	01111010	426	11010010	427	11010011
300	10001100	301	00000101	302	00000110	303	00000111	428	11010100	429	11010101	430	11010110	431	11010111
304	10010000	305	10010001	306	00010110	307	10010011	432	11011000	433	11011001	434	11011010	435	11011011
308	10010100	309	10010101	310	10010110	311	00000100	436	11011100	437	11011101	438	11011110	439	11011111
312	10011000	313	10011001	314	10011010	315	10011011	440	11100000	441	11100001	442	11100010	443	11100011
316	00010100	317	00010101	318	10011110	319	00011010	444	11100100	445	11100101	446	11100110	447	11100111
320	00100000	321	10100000	322	10100001	323	10100010	448	01111011	449	01000001	450	01000010	451	01000011
324	10100011	325	10100100	326	10100101	327	10100110	452	01000100	453	01000101	454	01000110	455	01000111
328	10100111	329	10101000	330	01011011	331	00101110	456	01001000	457	01001001	458	11101000	459	11101001
332	00111100	333	00101000	334	00101011	335	00100001	460	11101010	461	11101011	462	11101100	463	11101101
336	00100110	337	10101001	338	10101010	339	10101011	464	01111101	465	01001010	466	01001011	467	01001100
340	10101100	341	10101101	342	10101110	343	10101111	468	01001101	469	01001110	470	01001111	471	01010000
344	10110000	345	10110001	346	01011101	347	00100100	472	01010001	473	01010010	474	11101110	475	11101111
348	00101010	349	00101001	350	00111011	351	01011110	476	11110000	477	11110001	478	11110010	479	11110011
352	00101101	353	00101111	354	10110010	355	10110011	480	01011100	481	10011111	482	01010011	483	01010100
356	10110100	357	10110101	358	10110110	359	10110111	484	01010101	485	01010110	486	01010111	487	01011000
360	10111000	361	10111001	362	01111100	363	00101100	488	01011001	489	01011010	490	11110100	491	11110101
364	00100101	365	01011111	366	00111110	367	00111111	492	11110110	493	11110111	494	11111000	495	11111001
368	10111010	369	10111011	370	10111100	371	10111101	496	00110000	497	00110001	498	00110010	499	00110011
372	10111110	373	10111111	374	11000000	375	11000001	500	00110100	501	00110101	502	00110110	503	00110111
376	11000010	377	01100000	378	00111010	379	00100011	504	00111000	505	00111001	506	11111010	507	11111011
380	01000000	381	00100111	382	00111101	383	00100010	508	11111100	509	11111101	510	11111110	511	11111111

PRELIMINARY

MK 28000 P

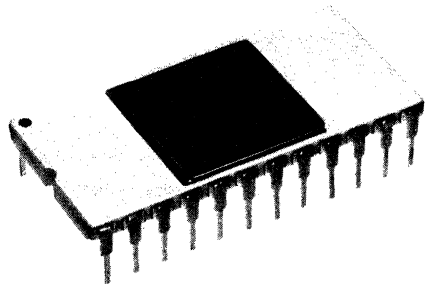
16K-BIT
MOS Read—ONLY Memory

MOSTEK

Read Only Memories

FEATURES:

- ☐ 850 ns Maximum Access Time
- ☐ 1.1 μs Maximum Cycle Time
- ☐ Low Power Dissipation —.02 mW/bit Typ.
- ☐ EA 4800/4900 Pin-for-Pin Replacement
- ☐ Options Include 2Kx8 Organization with Three-State TTL Output Capability
- ☐ 2Kx8 or 4Kx4 Organization with Open Drain Outputs
- ☐ Standard Supplies +5 Volts, — 12 Volts
- ☐ Ion-Implanted for Full TTL/DTL Compatibility



DESCRIPTION:

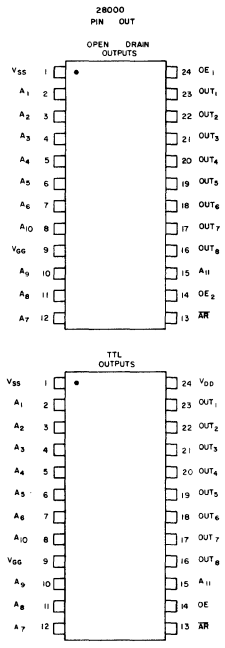
The MK 28000 is a mask programmable read only memory utilizing low-threshold Ion-Implant, P-channel technology. The 28000 is a pin-for-pin replacement for the EA 4800/4900. The organization may be either 2Kx8 or 4Kx4 with open drain outputs. The 2Kx8 organization may have TTL three-state outputs with only one output enable.

Output data is stored indefinitely after each memory access. If the output enables are held low during access, the outputs will be in a high impedance state.

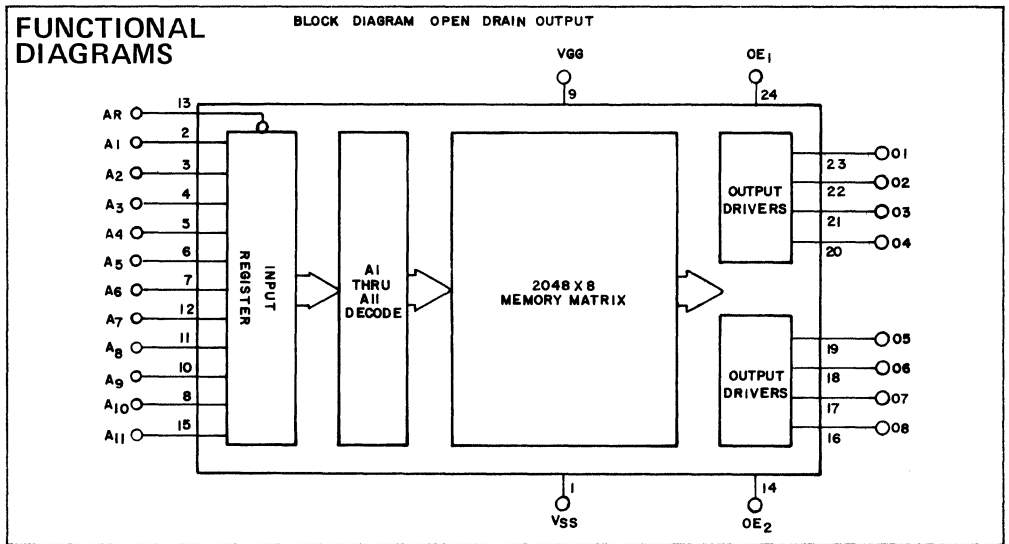
All inputs are protected against static charge accumulation. Pullup resistors on all inputs are available as a programmable option.

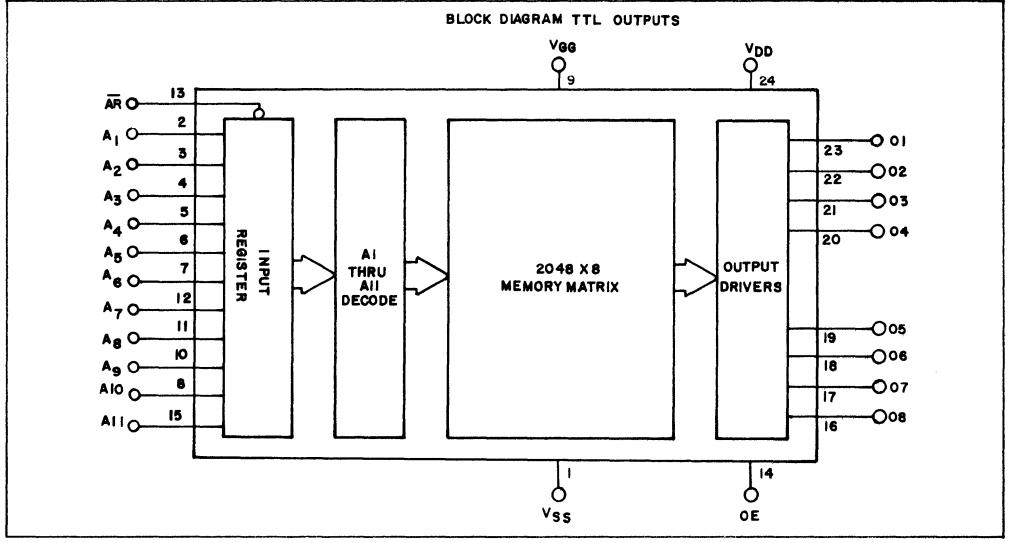
PIN CONNECTIONS

MK 28000 P



FUNCTIONAL DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

Voltage on any terminal relative to V_{SS} . . . . . +0.3V to −20V

Operating temperature range (Ambient). . . . . 0°C to 70°C

Storage temperature range (Ambient). . . . . −55°C to 150°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leqslant T_A \leqslant 70°C$)

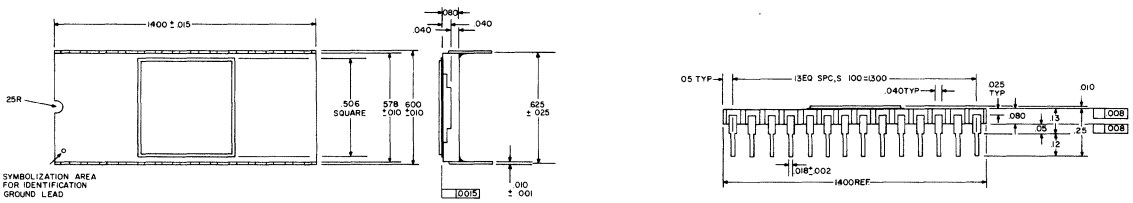
	PARAMETER	MIN	TYP	MAX	COMMENTS
V_{SS}	Supply Voltage	+4.75V	+5V	+5.25V	
V_{DD}	Supply Voltage	—	0	—	
V_{GG}	Supply Voltage	−12.6V	−12V	−11.4V	
V_{IL}	Input Voltage, Logic "0"			+.8V	
V_{IH}	Input Voltage, Logic "1"	V_{SS} − 1.5V			Pullup resistors to V_{SS} (≈5K) available as an option

ELECTRICAL CHARACTERISTICS

(V_{SS} = +5.0V ±5%; V_{DD} = 0V; V_{GG} = −12V ±5%; $0°C \leqslant T_A \leqslant 70°C$)

	PARAMETER	MIN	TYP	MAX	COMMENTS
I_{SS}	Supply Current		12 mA	20 mA	Outputs unconnected
I_{GG}	Supply Current		12 mA	20 mA	Inputs at V_{SS}
C_{IN}	Input Capacitance			10 pF	See Note 1
I_{IN}	Input Leakage			10 μA	See Note 2
R_{IN}	Input Pullup Resistors	3 KΩ		9 KΩ	Optional
V_{OL}	Output Voltage, Logic "0"			0.4V	I_{OL} = 1.6 mA See Note 3
V_{OH}	Output Voltage, Logic "1"	2.5V			See Note 4
I_{OL}	Output Leakage Current	−10 μA		+ 10 μA	$V_O = V_{SS} - 6V$, $T = 25°C$ (outputs disabled)

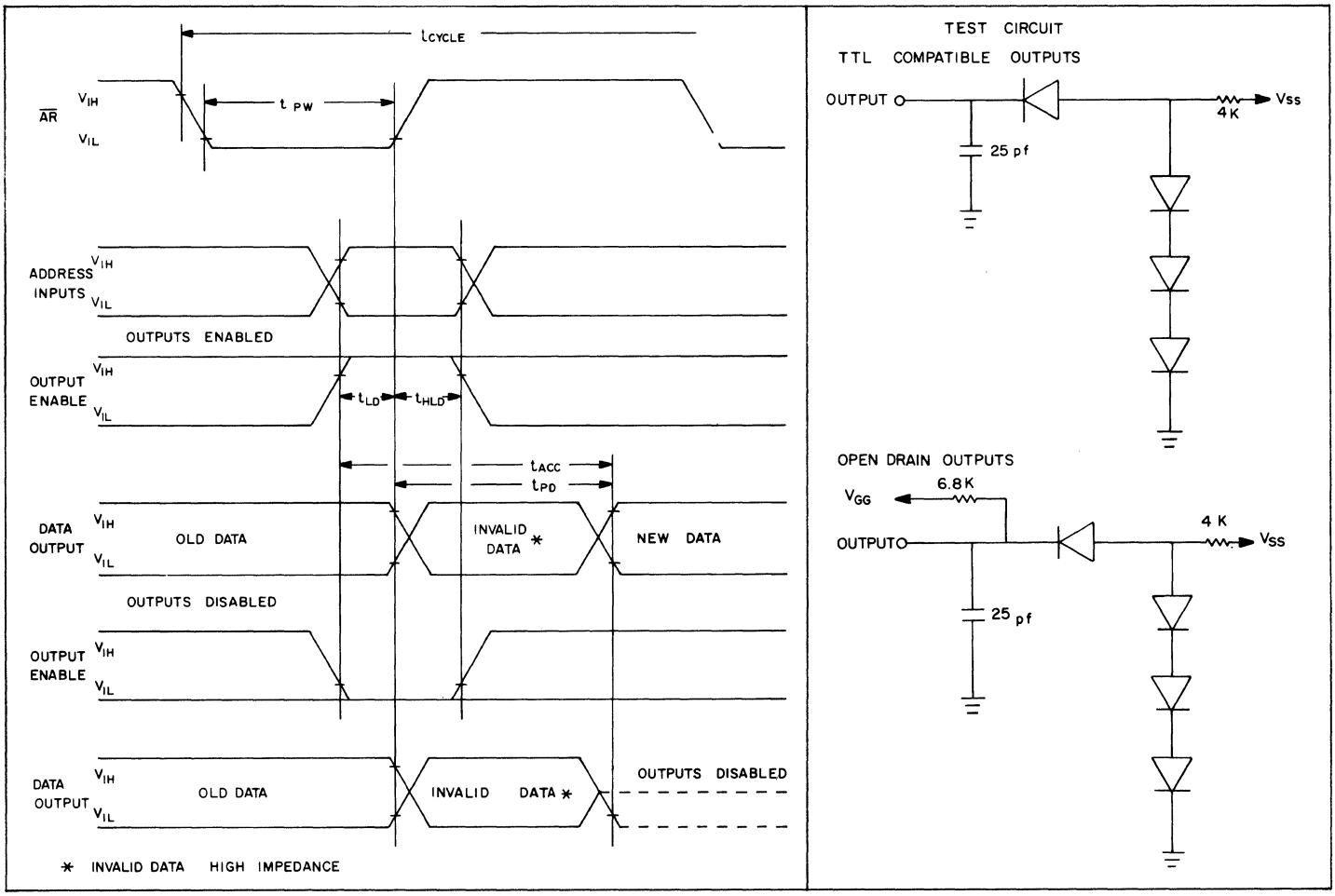
PACKAGE 28-pin ceramic dual-in-line



	PARAMETER	MIN	TYP	MAX	COMMENTS
t_{PW}	$\overline{AR}$ Pulse Width	400 ns			See timing and test circuit
t_{LD}	Address Lead Time	200 ns			
t_{HLD}	Address Hold Time	200 ns			
t_{PD}	$\overline{AR}$ to Output Delay	650 ns			
t_{ACC}	Access Time			850 ns	$t_{acc} = t_{ld} + t_{pd}$
t_{CYCLE}	Cycle Time	1.1 μs			$t_{cycle} = t_{pw} + t_{pd}$

NOTES:
1. $V_{BIAS} - V_{SS} = 0v$; f = 1 MHz
2. This parameter is for inputs without pullups (optional)
3. This parameter is for outputs with TTL compatible outputs.
4. For open drain outputs, a 6.8K Ω load to V_{GG} is assumed. (See test circuits)

TIMING



MOSTEK 28000 ROM Punched Card Coding Format[1]

First Card

Cols	Information Field
1-30	Customer
31-50	Customer Part Number
60-72	MOSTEK Part Number[2]

Second Card

1-30	Engineer at Customer Site
31-50	Direct Phone Number for Engineer

Third Card

1-5	MOSTEK Part Number[2]
10-16	Organization (2048X8 or 4096X4)
29	Outputs (1=Open Drain, ϕ=Push Pull TTL)
31	Number of Output Enable Pins (1 or 2)
33	Input Pullups (1=yes, ϕ=no)

Fourth Card

1-9	Data Format[3]
15-28	Logic – ("Positive Logic" or "Negative Logic")
35-57	Verification Code[4]

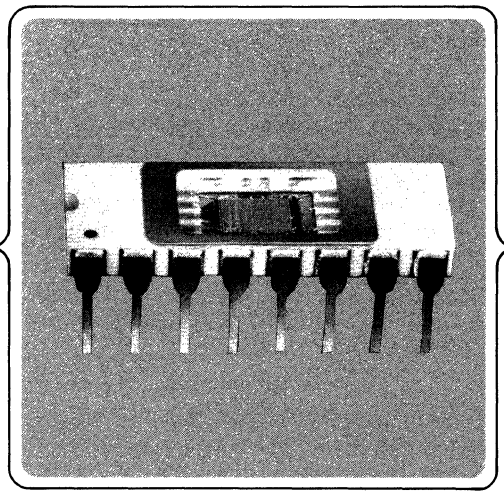
Data Cards

MOSTEK Format		or	EA Format (for EA Pin-for-Pin Replacement only)
1-4	Decimal Address		
6-13	Output B8-B1 (MSB Thru LSB)		
15-17	Octal Equivalent of Output Data		

NOTES:

1. Positive or negative logic formats are accepted as noted in the fourth card.
2. Assigned by MOSTEK; may be left blank
3. MOSTEK or Electronic Arrays Punched card coding format may be used. Specify which card format used by punching either "MOSTEK" or "EA". Start at column one.
4. Punched as: (a) VERIFICATION HOLD – i.e. customer verification of the data as reproduced by MOSTEK is required prior to production of the ROM. To accomplish this MOSTEK supplies a copy of its Customer Verification Data Sheet (CVDS) to the customer.
   (b) VERIFICATION PROCESS – i.e. the customer will receive a CVDS but production will begin prior to receipt of customer verification.
   (c) VERIFICATION NOT NEEDED – i.e. the customer will not receive a CVDS and production will begin immediately.

Random Access Memories



MK 4006 P-6
MK 4008 P-6

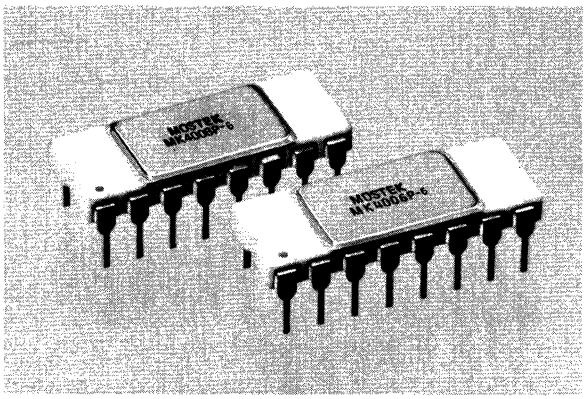
1024x1 BIT DYNAMIC

MOS Random Access Memory

MOSTEK

FEATURES:

- ☐ TTL/DTL compatible inputs
- ☐ No clocks required
- ☐ Access time:
  MK 4006 P–6 under 400 ns
  MK 4008 P–6 under 500 ns
- ☐ Standby power: under 50 mW
- ☐ 16-pin standard CDIP
- ☐ Supply voltage: +5V and −12V



DESCRIPTION

This is a family of MOS dynamic 1024x1 random-access memories having identical functional characteristics, differing only in speed. Access time in the MK 4006 P-6 is less than 400 ns; in the MK 4008 P-6 less than 500.

Full address decoding is provided internally. Information is read out non-destructively (NDRO) and has the same polarity as the input data.

TTL/DTL compatibility at all inputs allows economical use in small systems by eliminating the need for special interface circuitry. Large main-memory applications also benefit from the low drive-voltage swings as well as the packing density afforded by the standard 16-pin dual-in-line packaging and low standby power.

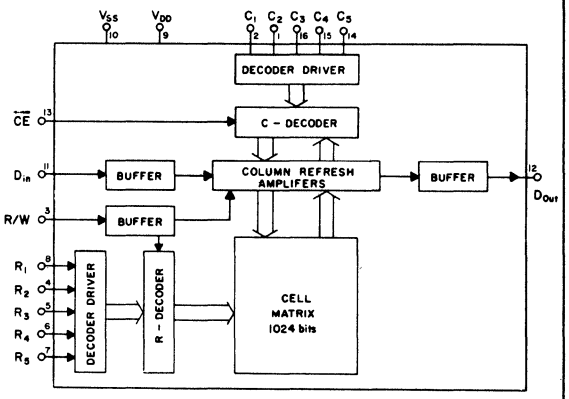
The internal memory element of this RAM is a capacitance, and refreshing must be periodically initiated (see TIMING). However, all internal decoding and sensing is static, so that precharging or clocking normally associated with dynamic memories is not required. From the user's viewpoint, memory control and addressing are essentially those of a static device.

Noise suppression measures normally employed in DTL or TTL systems are sufficient. High voltage input swings and high peak-current line drivers are unnecessary for driving memory inputs, and the memory itself does not exhibit large supply current transients.

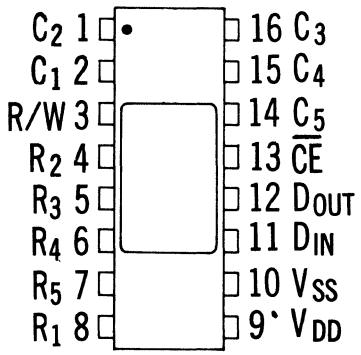
Data output is single-ended to minimize propagation delay. Output current is sourced from V_{SS} (+5V), and easily sensed using readily available components. A logic 1 at the output terminal appears as a 5,000 Ohm resistor (MK 4006) to +5V; a logic 0 as an open circuit.

The performance of this RAM is made possible by Mostek's ion-implantation process. In addition to offering low threshold voltages for TTL/DTL compatibility and utilizing conventional P-channel processing, ion-implantation allows both enhancement (normally OFF) and depletion (normally ON) MOS transistors to be fabricated on the same chip. By replacing conventional MOS load resistors with constant-current depletion transistors, operational speeds and functional density are increased.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... +0.3 to −20V

Operating Temperature ..... 0°C to +70°C

Storage Temperature Range ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS

(0° C $\leq T_A \leq$ 70°C)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
V_{SS}	Supply Voltage		+4.75		+5.25	V	
V_{DD}	Supply Voltage		−11.4		−12.6	V	
V_{IL}	Input Voltage, Logic 0				+0.8	V	
V_{IH}	Input Voltage, Logic 1		$V_{SS}-1$		V_{SS}	V	
V_{SB}	Standby Supply Voltage (Fig. 4)		$V_{SS}-4$		$V_{SS}-6$	V	Note 1

RECOMMENDED AC OPERATING CONDITIONS[2]

(0° C $\leq T_A \leq$ 70°C)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
t_{RC}	Read Cycle Time (Fig. 1)	400		500		ns	
t_{WC}	Write Cycle Time (Fig. 2)	650		900		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{WP}	Write Pulse Width (Fig. 2)	250		400		ns ns	t_{AW}=400 ns t_{AW}=500 ns
t_{AW}	Address-to-Write Delay (Fig. 2)	400		500		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{DLD}	Data-to-Write Lead Time (Fig. 2)	300		400		ns ns	t_{WP}=250 ns t_{WP}=400 ns
t_{RDLY}	Refresh Time (Fig. 3)		2		2	ms	See Note 3.
t_{CDPD}	Chip-Disable-to-Power-Down Delay (Fig. 4)	200		200		ns	See Note 1 See Note 4

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C $\leq T_A \leq$ 70°C unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
I_{SS}, I_{DD}	Supply Current: At T_A=0°C		32		32	mA	Output
	At T_A=70°C		27		27	mA	Open
P_{SDBY}	Power Dissipation, Standby		50		50	mW	$V_{SS}-V_{DD}$ = 5V; Note 1
I_{IH}	Input Current, Logic 1. Any Input	−5	+5	−5	+5	μA	$V_I=V_{SS}-1V$
I_{IL}	Input Current, Logic 0, Any Input	−5	+5	−5	+5	μA	V_I=0.8V
I_{OH}	Output Current, Logic 1	1.0		0.8		mA	Note 5
I_{OL}	Output Current, Logic 0		5		5	μA	

AC ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 5\%$; $V_{DD} = -12V \pm 5\%$; $0°C \leq T_A \leq 70°C$ unless otherwise noted)

	PARAMETER	MK 4006P-6 MIN	MK 4006P-6 MAX	MK 4008P-6 MIN	MK 4008P-6 MAX	UNITS	NOTES
t_{ACCESS}	Read Access Time (Fig. 1 & 1-A)		400		500	ns	Note 2
t_{CE}	Chip Enable Time (Fig. 1A & 5)		350		450	ns	Note 2
t_{CD}	Chip Disable Time (Fig. 1A & 5)		350		450	ns	
C_I	Input Capacitance, Any Input		5.0		5.0	pF	$T_A=25°C$; $V_I=V_{SS}$; f=1MHz
C_O	Output Capacitance		10		10	pF	$T_A=25°C$; $V_O=V_{SS}-5V$; f=1MHz
C_{DD}	V_{DD} Capacitance		75		75	pF	$T_A = 25°C$; Note 6

Random Access Memories

NOTES:

(1) Applies to MK 4006-6 and MK 4008-6 only.

(2) Measurement Criteria: Input voltage swing, all inputs: 0.8V to $V_{SS} - 1$
Input rise and fall times: 20 ns
Measurement point on input signals: +1.5V above ground
Measurement point on output signal: +60 mV above ground, using a load circuit of a 200 ohm resistor in parallel with a 100 pF capacitance connected to ground.

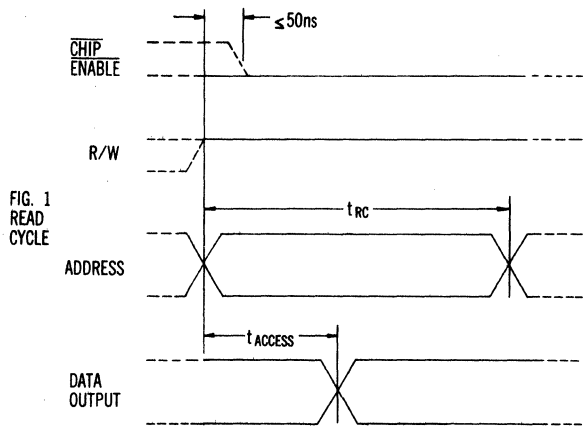
(3) t_{RDLY} is the time between refresh cycles for a given row address.

(4) The rise time of V_{DD} must not be faster than 20 ns.

(5) Steady-state values. (Refer to Fig. 1A for clarification)

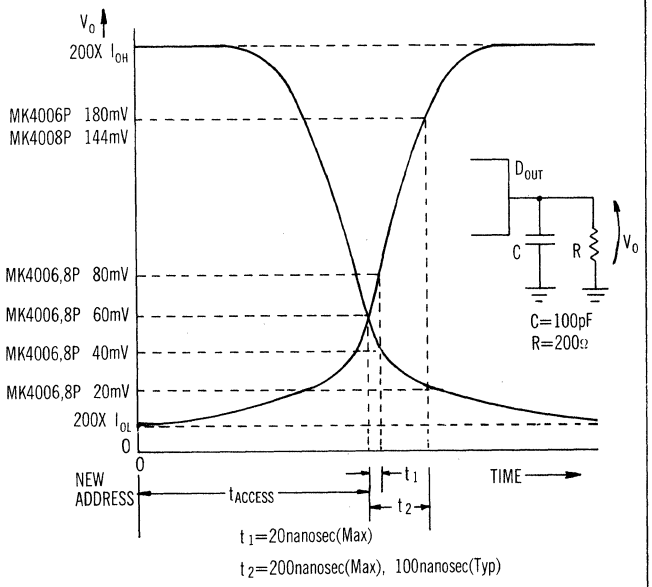
(6) Average capacitance of the V_{DD} terminal relative to the V_{SS} terminal. Measured by switching the V_{DD} terminal from OV to —12V with an applied $V_{SS} = 5V$. Peak I_{DD} is observed and the circuit replaced by a capacitance which yields the same peak current as the circuit under test.

TIMING (Note 2)



READING (Fig. 1)

Reading is accomplished with the Read/Write input held high. Data output directly follows the application of an address. As long as the address is unchanged and the chip enabled, data output will remain valid until the next refresh cycle. Input addresses can be changed as soon as output data is accessed. Any address can be applied repetitively without degrading stored data, providing that the refresh period of 2 ms is observed.



ACCESS TIME (Fig. 1-A)

Figure 1-A illustrates the measurement of access time after application of new address for the MK 4006 P and the MK 4008 P.

TIMING
(Note 2)

WRITING (Fig. 2)

Writing is accomplished by bringing the Read/Write input low with valid data present at the data input and the Chip-Enable input low (chip enabled). Following the return of the Read/Write line to a high state, new address and input data can be applied. If a read-after-write operation is desired, valid data will appear at the output within one read access time following the rising edge of the Write Pulse. Read-modify-write operation is easily achieved by delaying the Write Pulse until data has been read and modification is complete.

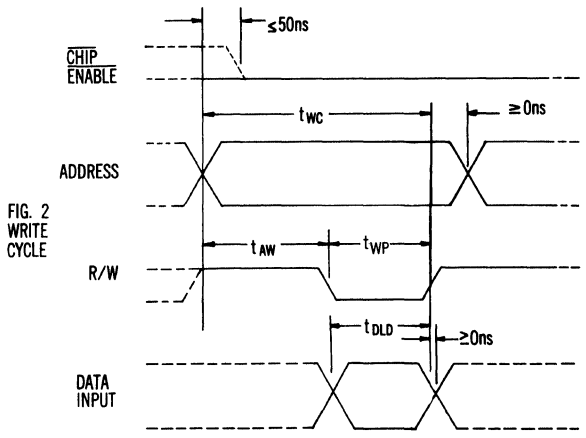


FIG. 2 WRITE CYCLE

REFRESHING (Figs. 2 & 3)

The dynamic memory cell employed in the MK 4006 P and MK 4008 P will not store data indefinitely. Stored data must be written back into the cell at least once every 2 ms. Rewriting is accomplished internally without the need to reapply external data. This rewriting operation is called *refreshing.*

Refreshing of the MK 4006 P and MK 4008 P is accomplished during both *write cycles* and *refresh cycles.* During a write cycle the state of the Row Address (R_1-R_5) determines which of the 32 memory matrix rows will be internally refreshed. An entire row (32 bits) is refreshed during one write cycle. Since it is difficult in practice to assure that each of the 32 possible R addresses is associated with a write cycle in every 2 ms period, a separate refresh cycle is normally employed.

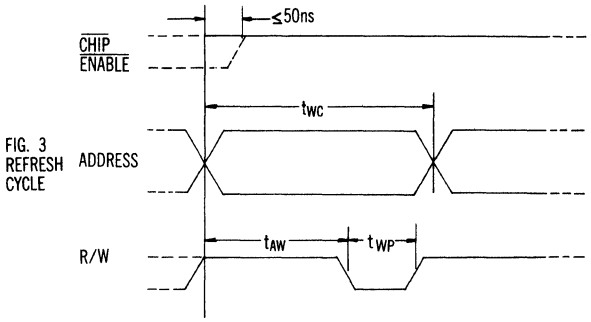


FIG. 3 REFRESH CYCLE

The refresh cycle is identical to the write cycle except that the chip is disabled while the Read/Write line is pulsed. Disabling the chip removes the data output and prevents data at the data input from being written into the memory. An entire refresh cycle consists of 32 address changes and associated write pulses, involving a total time of approximately 20 microseconds.

STANDBY MODE (Fig. 4)

Power dissipation of the MK 4006-6 P and MK 4008-6 P can be reduced below 50 mW without loss of stored data by lowering the V_{DD} supply voltage to system ground (V_{SS}-5V). Figure 4 illustrates the proper input conditions that should be observed when reducing V_{DD}. If the standby mode is maintained as long as 2 milliseconds, the V_{DD} supply should be returned to −12V and a refresh cycle initiated. Read or write cycles can commence immediately following the return of V_{DD} to −12V.

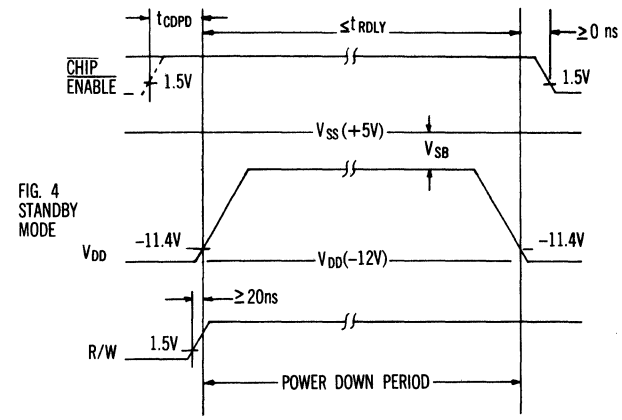


FIG. 4 STANDBY MODE

TIMING
(Note 2)

CHIP ENABLING (Fig. 5)

The negative-going $\overline{CE}$ enables the chip, and output data becomes valid within t_{CE} time. Return of the $\overline{CE}$ input to logic 1 disables the chip; data out remains for t_{CD} time.

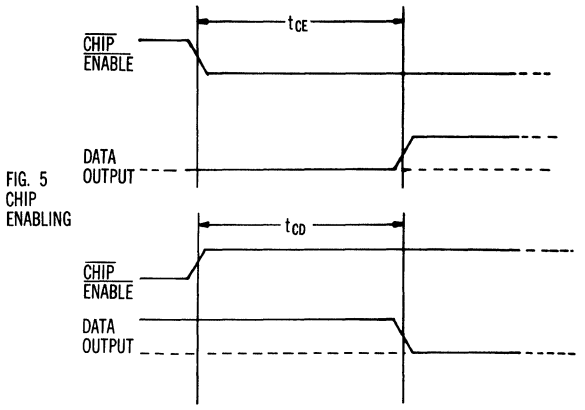


FIG. 5 CHIP ENABLING

TESTING CONSIDERATIONS

For a complete discussion of testing this memory, see Mostek's Applications Note AN-103.

The functional diagram (Fig. 6) indicates signal flow for selected row and column.

A simplified listing of functional tests is shown in Table 1. (high = Logic 1; low = Logic 0)

Tests are performed in an address sequence which requires the maximum number of changes in the row and column decoders between addresses. Addressing Rows 0 through 31 is accomplished by using the binary equivalent of the row address. The internal organization of the memory matrix requires the logic shown in Fig. 7 for column addresses; this logic provides the necessary conversion from inary equivalent to column address.

Fig. 6

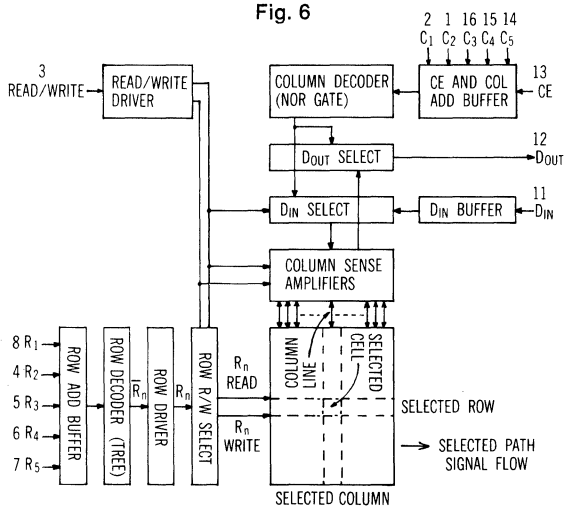


Fig. 7

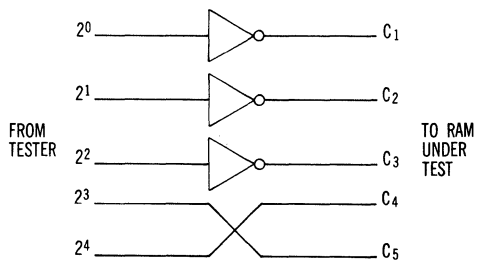
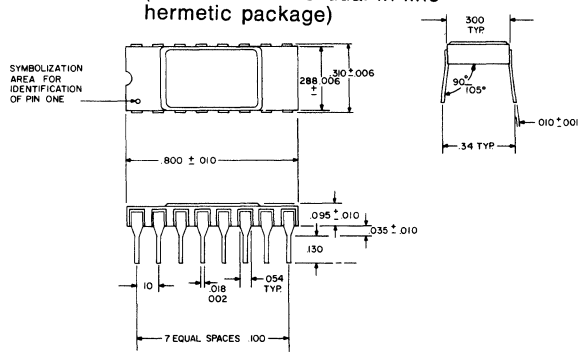


TABLE 1: FUNCTIONAL TESTS (SIMPLIFIED)

TEST DESC.	TEST SEQ.	OPER.	CHIP ENABLE	DATA INPUT	COMPARE DATA
Bit & Decoder Test[1]	First	Write	E	Parity	
	Next	Read	E		Parity
Column Shorts & No Write During Disable	First	Write	E	V-Bar	
	Next	Write	D	$\overline{\text{V-Bar}}$	
	Next	Read	E		V-Bar
Row Shorts, No Read During Disable, & Max. Power	First	Write	E	H-Bar	
	Next	Read	D	1	0
	Next	Read	E	0	H-Bar
Access Time, Refresh, Write Cycle, & Standby[1]	First	Write, Write	E	V-Bar, $\overline{\text{V-Bar}}$	
	Next	Delay	D	0	
	Next	Read	E		$\overline{\text{V-Bar}}$
Disturb Test	First	Write Row of 1's	E	1	
	Next	Write Adj. Row with 0's	E	0	
	Next	Continue Writing Same Row for Max. Refresh Delay	E	0	
	Next	Read original Row of 1's	E		1

1. Test performed as shown and repeated with complementary data.

PACKAGE (16-lead ceramic dual-in-line hermetic package)



ORDERING INFORMATION

MK 4006 P–6 1024x1 RAM/w/400 ns access time with power down
MK 4008 P–6 1024x1 RAM/w/500 ns access time with power down

APPLICATION

SENSE AMPLIFIERS FOR MK 4006/4008 RAM's

Since the interface circuitry used to convert memory signals to system logic levels strongly influences system access times, this circuitry should always be designed to meet the speed and cost requirements of the particular application.

Fig. 1-A (See "Timing") is shown to assist in the design of such amplifiers. This figure shows output voltage (across a specified load) vs. time from application of new address with several points indicated where specified voltage levels are referenced to specific times. Although all the various access times vs. output current levels cannot be shown, a few guidelines are given for interpolation between the specified points.

In Fig. 1-A, the two points at t_{access} + 20 nsec give the minimum "1" level and the maximum "0" level for this particular time (80 mV and 40 mV respectively). At t_{access} + 200 nsec, voltage levels are specified for the 90% and 10% points of the minimum "1" and maximum "0" levels.

INTERPOLATION

These interpolation guidelines are selected to give the designer a high level of confidence in his sense amplifier design.

From O to 1: This portion of the access curve can be estimated by two linear portions: (1) from the 60 mV to the 80 mV level; and (2) from the 80 mV level to 180/144 mV level.

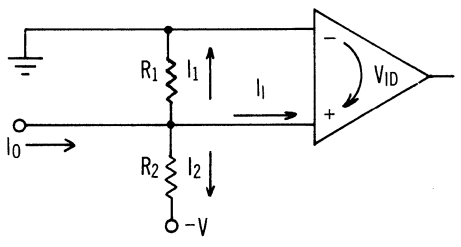
From 1 to O: This portion of the access curve can be estimated by a semi-logarithmic plot decreasing 20 mV for each decade or 10 nsec of time added to t_{access}, with the end points being 60 mV at 2 nsec and 20 mV at 200 nsec.

EXAMPLE: Let us consider how this data can be used in a sense amplifier design utilizing the 75107/108 Dual-Line-Receiver-and-Driver.

The manufacturer's data sheet for this circuit shows us that at strobe time, three conditions of the line receiver can exist: (1) the input voltage differential can be more positive than 25 mV, resulting in a logic 1 at the output (Input differential voltage is referenced to the inverting terminal); (2) the input differential can be more negative than 25 mV, resulting in a logic O at the output; (3) the input differential is less than 25 mV (absolute value), which will result in an output of an undetermined state. In other words, the line receiver has a 50 mV "window" centered around zero, and a signal must fall outside this window to provide reliable information at the output.

The standard configuration for using the 75107/108 as a sense amp is shown in Fig. 8 with the voltage and current conventions used in this analysis.

FIG. 8: Illustrating use of 75107/108 Line Receivers as sense amplifiers for the MK 4006/4008 P.



From the worst-case access at the *chip* level, one can use the interpolation technique described above to determine maximum "O" current level [I_{OLC}(MAX)] and the minimum "1" current level [I_{OH}(MIN)].

However, to use a worst-case approach to this design, in addition to the chip's characteristics, one must include in the "O" level current the effect of leakage from all outputs that are wired together. Also the input currents required by the 75107/108 (75 mA and 10 mA) must be included. Let us call this I_{OLT}(MAX):

$$I_{OLT}(MAX) = I_{OLC}(MAX) + (N\text{-}1)\ (5\ \mu A) \quad [1]$$

where N = number of outputs wired together

Using the maximum zero level at the line receiver input ($V_{ID} \leq -25mV = V_{ID}^{-}$), the following equation is derived:

$$I_{OLT}(MAX) = I_1 - I_2 + I_{IL}(MIN)$$

and $I_{IL}(MIN) = O\ \mu A$ [2]

therefore:

$$I_{OLT}(MAX) = \frac{V_{ID}^{-}}{R1} + \frac{V + V_{ID}^{-}}{R2} \quad [3]$$

Using the minimum "1" level at the line receiver input ($V_{ID} \geq +25\ mV = V_{ID}^{+}$), the equation becomes

$$I_{OH}(MIN) = I_1 - I_2 + I_{IH}(MAX) \quad [4]$$

and $I_{IH}(MAX) = 75\ \mu A$

$$I_{OH}(MIN) = \frac{V_{ID}^{+}}{R1} + \frac{V + V_{ID}^{+}}{R2} + 75\ \mu A \quad [5]$$

Solving these equations ([3] and [5]) simultaneously yields R1 and R2.

As an example, assume a memory system with 4 outputs wired-ORed to a sense amplifier, requiring a chip access time of 460 nsec. Then the associated current and resistor values are:

$I_{OLT}(MAX) = 152.3\ \mu A + 3\ (5\ \mu A) = 167.3\ \mu A$

$I_{OH}(MIN) = 511.12\ \mu A$

Therefore:

$R1 = 190\ \Omega$

$R2 = 16.5\ K\Omega$

Sense amplifiers vary from the very fast, low-threshold types to the slower, high-threshold kind. The ideal choice will depend on the application. Fig. 1-A and the guidelines in this note are intended to help the designer tailor his sense amplifier design to meet the speed and cost requirements of his particular application.

It should also be noted that a portion of the output current from the memory chip is used to charge the capacitance on the data output. If the output impedance differs greatly from the specified load, this current must also be calculated.

SUPPLEMENT **MK 4008P-9**

1024 x 1 BIT DYNAMIC

MOS Random Access Memory

MOSTEK

Random Access Memories

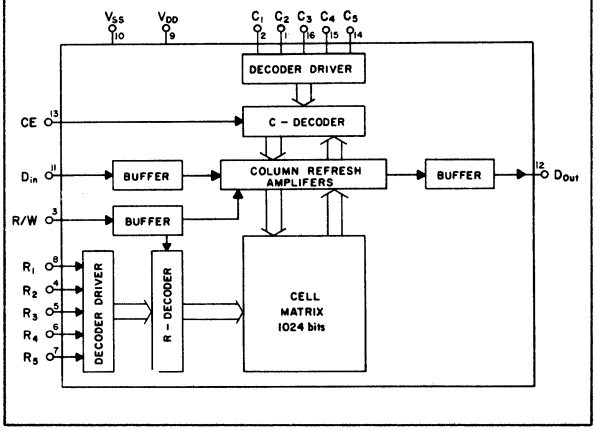
FEATURES

- ☐ 1024x1 RAM in 16-pin package
- ☐ Functionally equivalent to Mostek MK4006/4008 RAM's

DESCRIPTION

This 1024x1 Bit Dynamic Ram is selected from Mostek's MK4006 and MK4008 RAMs. See the MK4006/4008 data sheet for additional information, including timing diagrams.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin (except V_{GG}) relative to V_{SS} ..... +0.3 to −10V
Voltage on V_{GG} pin relative to V_{SS} ..... +0.3 to −20V
Operating Temperature ..... 0 °C to +70°C
Storage Temperature Range ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS

(0° C $< T_A <$ 70°C)

	PARAMETER	MIN	MK 4008 P-9 MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+4.75	+5.25	V	
V_{DD}	Supply Voltage	−11.4	−12.6	V	
V_{IL}	Input Voltage, Logic 0		+0.8	V	
V_{IH}	Input Voltage, Logic 1	V_{SS}−1	V_{SS}	V	

RECOMMENDED AC OPERATING CONDITIONS[1]

(0° C $< T_A <$ 70°C)

	PARAMETER	MK 4008P-9 MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time (Fig. 1)	800		ns	
t_{WC}	Write Cycle Time (Fig. 2)	1		us	t_{WP}= 450 ns
t_{WP}	Write Pulse Width (Fig. 2)	450		ns	t_{AW}=550 ns
t_{AW}	Address-to-Write Delay (Fig. 2)	550		ns	t_{WP}=450 ns
t_{DLD}	Data-to-Write Lead Time (Fig. 2)	500		ns	t_{WP}=450 ns
t_{RDLY}	Refresh Time (Fig. 3)		1	ms	See Note 2

DC ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C < T_A < 70° C unless otherwise noted)

	PARAMETER	MK 4008 P-9 MIN	MAX	UNITS	NOTES
I_{SS}, I_{DD}	Supply Current: At T_A=0°C		32	mA	Output
	At T_A=70°C		27	mA	Open
I_{IH}	Input Current, Logic 1, Any Input	−5	+5	μA	$V_I = V_{SS}$−1V
I_{IL}	Input Current, Logic 0, Any Input	−5	+5	μA	V_I=0.8V
I_{OH}	Output Current, Logic 1	0.6		mA	Note 3
I_{OL}	Output Current, Logic 0		5	μA	

AC ELECTRICAL CHARACTERISTICS

(V_{SS} = +5V ± 5%; V_{DD} = −12V ± 5%; 0°C < T_A < 70° C unless otherwise noted)

	PARAMETER	MK 4008 P-9 MIN	MAX	UNITS	NOTES
t_{ACCESS}	Read Access Time		800	ns	Note 1
t_{CE}	Chip Enable Time		450	ns	Note 1
t_{CD}	Chip Disable Time		450	ns	
C_I	Input Capacitance, Any Input		5.0	pF	T_A=25°C; $V_I = V_{SS}$; f=1MHz
C_O	Output Capacitance		10	pF	T_A=25°C; $V_O = V_{SS}$−5V; f=1MHz

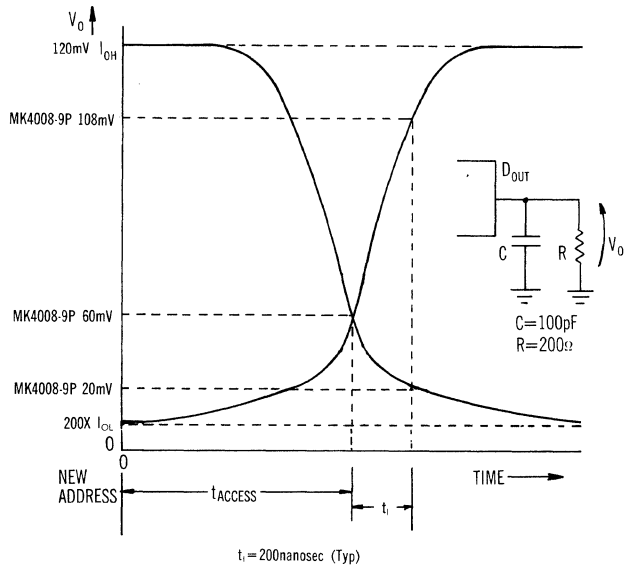
NOTES:

(1) Measurement Criteria: Input voltage swing, all inputs: 0.8V to V_{SS} — 1
Input rise and fall times: 20 ns
Measurement point on input signals: +1.5V above ground
Measurement point on output signal: +60 mV above ground, using a load circuit of a 200 ohm resistor in parallel with a 100 pF capacitance connected to ground.

(2) t_{RDLY} is the time between refresh cycles for a given row address.

(3) Steady-state values. (Refer to Fig. 1A for clarification)

TIMING



ACCESS TIME (Fig. 1-A)

Figure 1-A illustrates the measurement of access time after application of new address for the MK 4008 P-9.

DESIGNING AN ASYNCHRONOUS MEMORY SYSTEM USING THE MOSTEK MK 4008-9 RAM

by ERNIE FINK*

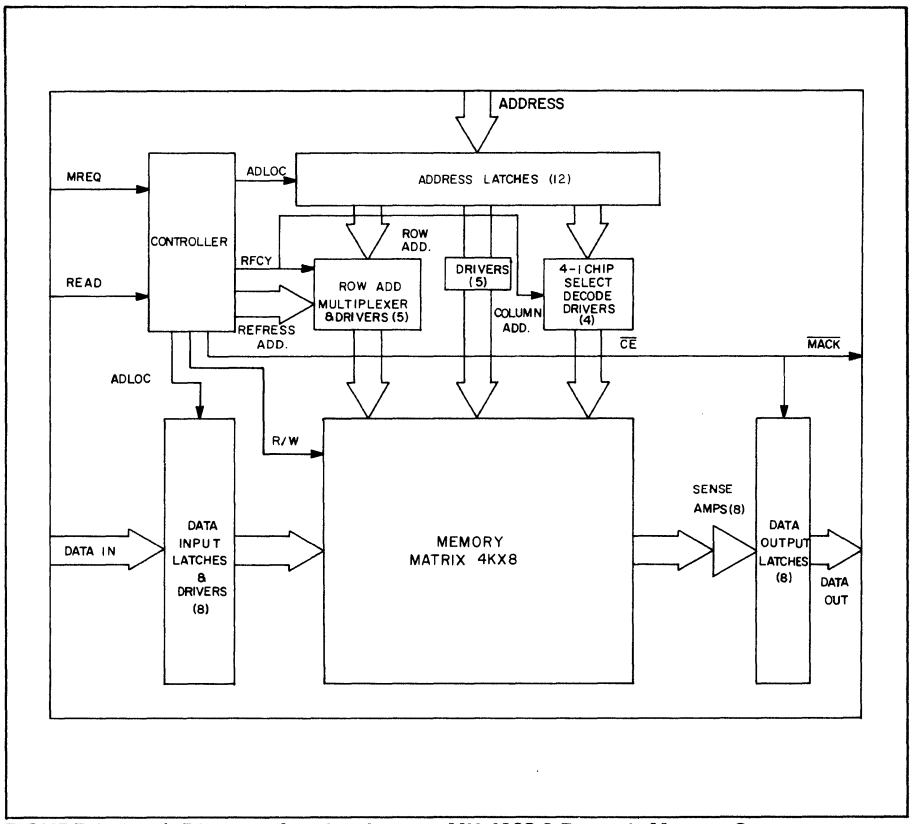


FIGURE 1 - Block Diagram of an Asychronous MK 4008-9 Dynamic Memory System. The memory configuration shown is 4K x 8.

INTRODUCTION

The asynchronous memory system is popular with memory users since it generates its own internal timing signals and interfaces at the system level via handshaking or demand techniques. The user simply makes a request for a memory cycle and applies address and data to the interface. The memory system performs the requested cycle and provides an acknowledge signal to the user indicating that the cycle is complete and data is available. The memory does not require external clock signals or specific cycle request rates from the user. This allows both high and low cycle rate users such as a CPU and its peripherals to share the same memory without complicated control logic.

This note describes the design of as asynchronous memory system using the MOSTEK MK 4008-9 dynamic RAM. The system is organized as 4K-words by 8-bits and has a cyle time of 1.155 microseconds. The block diagram of the memory system is shown in Figure 1. The controller and other functional blocks of the diagram will be discussed after a review of the characteristics of the MK 4008-9.

MK 4008-9 CHARACTERISTICS

The MK 4008-9 is a 1024 X 1 random access memory. The storage matrix is arranged as 32 rows of 32 bits. The matrix is dynamic and required that each bit be refreshed every millisecond. The refreshing is accomplished by disabling the chip(s) and performing a write cycle at each of the 32 row addresses. All 32 bits in a row are refreshed during the refresh cycle.

The inputs on the MK 4008-9 are all TTL compatible with the aid of a pull-up resistor. The inputs look like 5 pf capacitors. A 4K X 8 bit memory would have the address lines running to each of the 32 chips. This would look like 160 pf without considering the wiring capacitance. For this reason high current input drivers are used on the address lines to provide the speed that is required of the memory system. The memory system shown in Figure 1 uses Signetics 8T09 Quad Bus Drivers for the address and read/write inputs. The 160 pf from the 32 chips plus approximately 40 pf from the wiring presents 200 pf to the input drivers. The input "1" level to the MK 4008-9 must be 4 volts. The 8T09 will drive 300 pf with a propagation delay of 20 nsec. A pullup resistor must be used to insure the 4 volt level on the input. The pullup resistor also serves to terminate the driven signal line minimizing signal distortion due to reflections. The resistor value should be chosen with the trade-off of power dissipation versus termination efficiency in mind. Care must be taken to prevent overshoot of the signal above the V_{ss} level.

A write cycle for the MK 4008-9 consists of a 450 nsec (min) negative-going pulse on the R/W line following a 500 nsec (min) time during which the address is stable and the chip is enabled. The input data must be true at the time the R/W line goes low. A refresh cycle is the same without the chip being enabled. In this case, data on the inputs will not be written into the memory.

For a read cycle, the data will appear at the output 800 nsec (max) after the address is stable

*Mostek Corp. 1215 West Crosby Road, Carrollton, Tex.

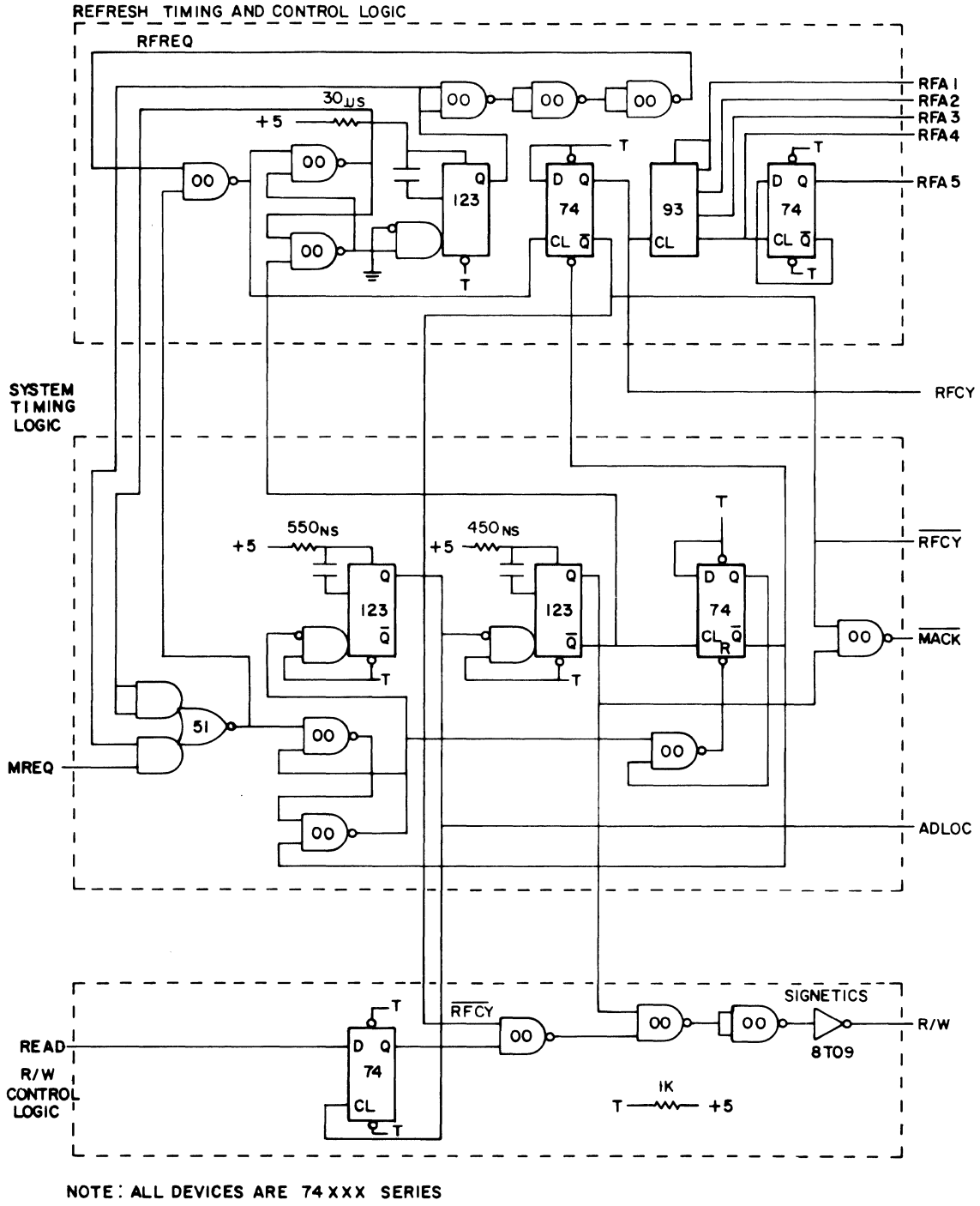


FIGURE 2 - Complete Diagram of an Asynchronous Memory Controller. The controller has three main blocks: refresh timing and control logic, system timing logic, and read/ write control logic.

if the chip is enabled. If the chip is not enabled, the output will appear as an open circuit. This feature allows several MK 4008-9 to be wire-ORed together with only one chip being enabled at a time. The use of a sense amp to detect the current output will be discussed later.

CONTROLLER

A detailed drawing of an asynchronous memory controller for an MK 4008-9 is shown in Figure 2. The controller has three basic parts: refresh timing and control logic, cycle timing logic and read control logic.

The refresh timing and control logic must be able to time the period between refreshes, increment a five bit binary counter (refresh row address) and gain priority control over the cycle timing logic to perform a refresh cycle

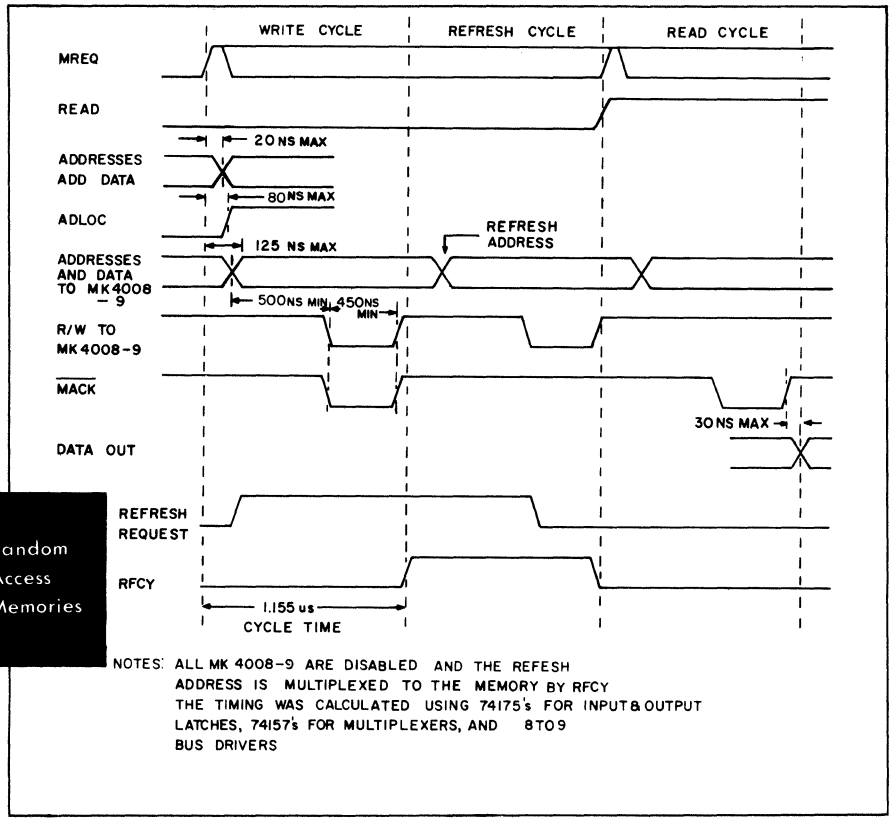


FIGURE 3 - Timing Diagram showing a write cycle, refresh cycle and read cycle.

(RECY). The refresh of the 32 rows every millisecond is separated into the refresh of a different row every 31.2 μsec (distributed refresh technique). The refresh could be accomplished on all rows at one interrupt if desired (burst refresh technique).

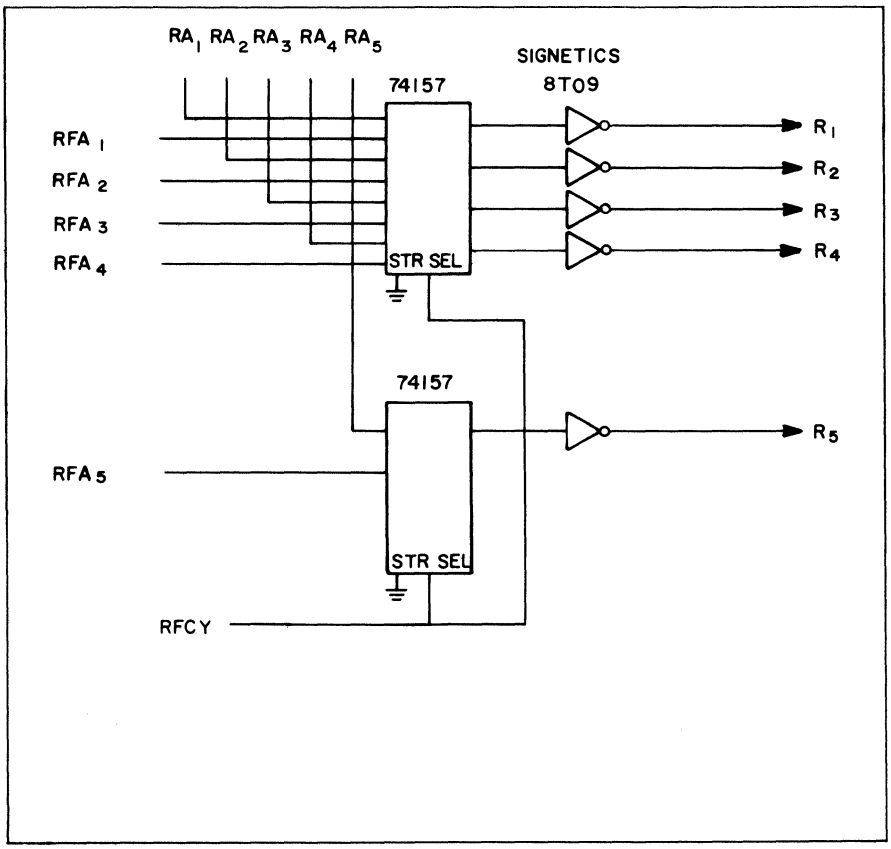


FIGURE 4 - Complete diagram of row address multiplexers and line drivers.

The refresh timing and control logic uses a one-shot to time-out the period between refresh cycles. When the time has expired, a Refresh Request (RFREQ) is issued to the cycle timing logic. If the cycle timing logic is timing out a cycle when the Refresh Request is received, it will wait until the cycle in progress has ended and then begin the refresh cycle. If a Memory Request (MREQ) is issued while a refresh cycle is in progress, the refresh cycle will finish and then the memory request will be accepted. This is illustrated in the timing diagram in Figure 3. When a refresh cycle is begun, the refresh timing and control logic must multiplex the row address from the binary counter to the memory (figure 4), tell the read control logic that the cycle requires a write pulse, inhibit the Memory Acknowledge signal and disable all MK 4008-9's. Upon completing the refresh cycle, the one-shot is retriggered to start the time-out until the next refresh cycle and increment the refresh address counter.

The cycle timing logic generates all the timing signals that are needed for a cycle whether it is a write, read or refresh cycle. When a memory request is issued to the memory system, the cycle timing logic generates a signal, ADLOC, that latches addresses, input data and Read. For each cycle, a write pulse is generated and is routed to the read control logic. The read control gates the write pulse to the memory matrix. For a read cycle the write pulse is not gated to the memory matrix. For a write cycle or a refresh cycle, a memory acknowledge (MACK) is generated. Memory acknowledge goes low to indicate the memory request is being performed and goes high to indicate the cycle is completed. Data will be true on the output 30 ns after memory acknowledge goes high.

Figure 3 is a timing diagram showing three cycles for the MK 4008-9 memory system. The first cycle is a write cycle, the second is a refresh and the third is a read cycle.

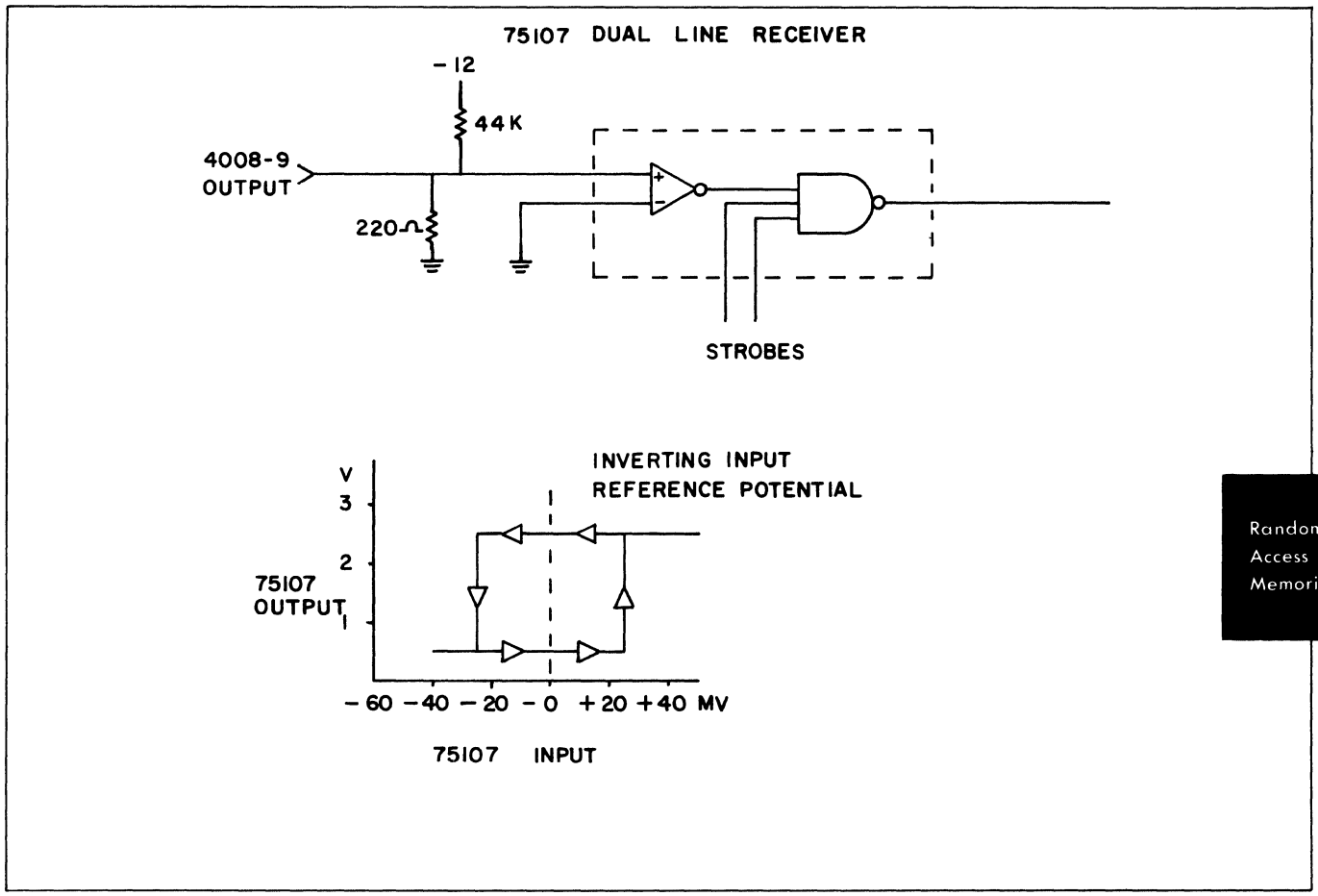


FIGURE 5 - 75107 sense amplifier application diagram.

When a read cycle is completed, the output data is latched at the memory system output. Note the output data remains true for a minimum of one cycle. For some applications, the input and output latches would not be needed. Seven 74175 latches would be eliminated in this case and approximately 100 ns subtracted from the overall system cycle time.

SENSE AMP

The MK 4008-9 output is an open drain configuration and is specified to produce $\leq$ 60 mV for a "0" and $\geq$ 60 mV for a "1" across a 200 Ω resistor and 100 pf capacitor in parallel to GND at the 800 ns access time. This small signal must be converted to a TTL level. The system shown in Figure 1 uses a sense amp (TI 75107 Dual Line Receiver) to perform this function. The 75107 has the sensitivity, ease of use and the availability to be selected to convert the output to a TTL level and maintain the economy of this system. The 75107 is used in the circuit as shown in Figure 4. When the 75107 non-inverting (+) input becomes more positive, by 25 mW, than the inverting (—) input, the output will switch to a TTL "1" level. The opposite occurs when the non-inverting becomes more negative than the inverting input by 25 mV. The 75107 has a 50 mV window where the output is in an indeterminate state. Figure 4 shows the inverting input of the 75107 to be at GND. The non-inverting input, when the MK 4008-9 output is off, is biased to —60 mV. As the MK 4008-9 output turns on, the non-inverting input will change from a negative to a positive potential. Upon reaching +25 mV the 75107 output will begin switching to a TTL "1" level. At this point, the MK 4008-9 will be sourcing 475μA and will have produced an 85 mV change across the 220Ω resistor. When the MK 4008-9 output is falling from a "1" to a "0", the 75107 will switch when the output reaches —25 mV. Using the method described in the applications note on the MK 4006/8 data sheet, the access time is 940 ns using this set of resistors. This gives an access with sufficient time for propagation through the 75107 and 74175 data output latch.

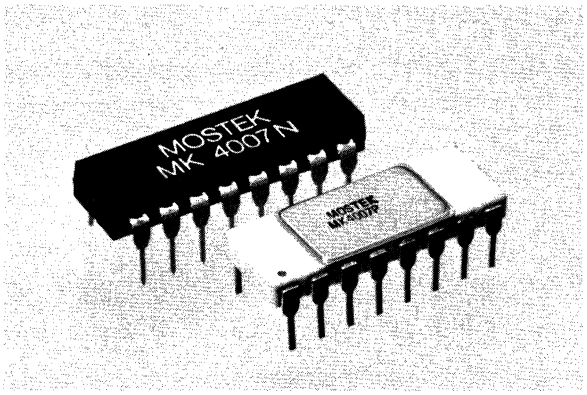
CONCLUSION

The design presented in this note is typical of asynchronous memory systems and the design principles discussed are applicable to memory systems of other sizes. The MK 4008-9 was chosen for this design because it is readily available and priced at only $3.50 in quantities over one thousand. This low pricing coupled with the ease of use and competitive performance of the device make it an excellent choice for new and replacement memory system designs. The total system cost including the refresh control logic and sense amplifiers will generally be significantly lower than the equivalent system using the available 1K static RAM devices.

MK 4007P
MK 4007N

256 BIT
MOS Random Access Memory

MOSTEK



FEATURES:

- ☐ Versatile RAM can replace any existing 1101-type 256x1 MOS RAM pin for pin.
- ☐ Ion-implanted for superior performance.
- ☐ **Lower power dissipation:** TOTAL 370 mW max over entire temperature range.
- ☐ **Faster access time:** Typically 525 ns with V_D and V_{DD} at −9V.
- ☐ **Less temperature-sensitive:** specified over entire AMBIENT temperature range 0° to 75°C.
- ☐ **Tight control of output sink current capabilities:** made possible by use of depletion-mode transistors.
- ☐ **No restrictions** on address input sequence, skew, or rise and fall times.
- ☐ Full DTL/TTL compatibility.
- ☐ Wide power supply range: +5V; −6.5 to −15V.

APPLICATIONS:

Ideal for small buffer storage requiring low cost, superior performance, and bipolar compatibility, such as:

- ☐ Scratchpad memories
- ☐ Data link buffers
- ☐ Key-to-tape buffers
- ☐ Tape-to-printer buffers
- ☐ Editing memories.

DESCRIPTION

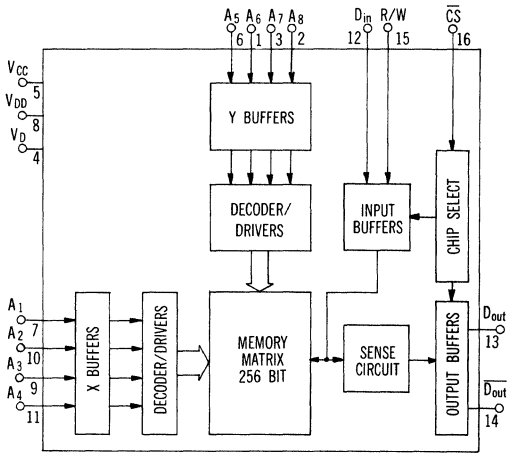
Ion-implantation processes used in manufacturing the Mostek MK 4007 P Random Access MOS Memory result in a low-cost device with performance exceeding other industry types over the entire temperature and voltage supply ranges. It may be used to replace any existing 1101 type RAM pin for pin.

The depletion-load ion-implantation technique allows the fabrication of both depletion and enhancement mode transistors on the same chip. The result is not only superior operating characteristics within the region usually specified for devices of this type, but also wider operational areas without severe performance degradation. For example, while specifications for this device are given for V_D and V_{DD} from −7 to −13.2V, V_D and V_{DD} may actually range from −6.5 to −15 V (see DC Operating Conditions and Fig. 1). Access times are improved (see Fig. 2); power dissipation is reduced (see Fig. 3) and output sink current capabilities are improved (see Fig. 4). The device is less temperature-dependent (see Figures 5 and 6) and is specified over the *entire* ambient temperature range of 0° to 75°C.

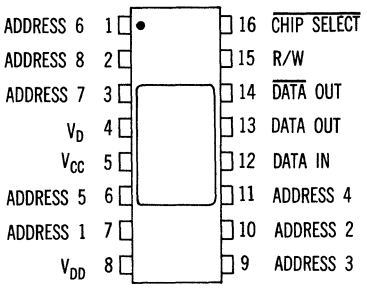
The ion-implantation process also makes the MK 4007 P RAM fully TTL/DTL compatible at all inputs and outputs.

The 4007 P is a static memory, requiring no clocks or refreshing. Data is written into the address location by applying a logic "1" to the R/W input. Addressing the desired location, with the chip enabled and R/W at logic "0", provides a non-destructive read-out (NDRO) of true and complement data. A "Chip Select" allows output buffers to be open-circuited during disable time for wire ORing. All inputs are protected against static charge accumulation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{CC} . . . . . + 0.3 V to −25 V
Operating Temperature Range (Ambient) . . . . . 0°C to +75°C
Storage Temperature Range (Ambient) . . . . . −55° to +150°C

DC OPERATING CONDITIONS

(Ambient Temperature Range: 0°C to +75°C)

		PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
POWER	V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
	V_{DD}	Supply Voltage	−6.5	−9.0	−15.0	V	See Fig. 1 for
	V_D	Supply Voltage	−6.5	−9.0	−15.0	V	V_D, V_{DD} differential
INPUTS	V_{IL}	Logic "0" Voltage, any input		0	+0.8	V	
	V_{IH}	Logic "1" Voltage, any input	V_{CC} −2.0	V_{CC}	V_{CC}+0.3	V	

ELECTRICAL CHARACTERISTICS

(Ambient Temperature Range: 0°C to +75°C. V_{CC} = +5 V ±5%;
$V_D = V_{DD}$ = −7 V to −13.2 V, unless otherwise specified.)

		PARAMETER	MIN	TYP(1)	MAX	UNITS	CONDITIONS
POWER	I_D	Supply Current. V_D		8.0	16	mA	$V_D = V_{DD}$ = −9V ± 5%
	I_{DD}	Supply Current, V_{DD}		4.0	9	mA	Outputs open-circuited.
	P_D	Power Dissipation, Total		170	370	mW	
	I_D	Supply Current. V_D			19	mA	$V_D = V_{DD}$ = −13.2 V
	I_{DD}	Supply Current, V_{DD}			10	mA	V_{CC} = +5.25 V
	P_D	Power Dissipation, Total			535	mW	Outputs open-circuited.
	P_{SDBY}	Power Dissipation, Standby		30	75	mW	$V_D = V_{CC}$; V_{DD} = −9V ±5%
INPUTS	$I_{I(L)}$	Input Leakage Current			1.0	μA	V_{IN} = 0 V, T_A = 25°C
	C_{IN}	Input Capacitance, Any Logic Input		7	10	pF	T_A = 25°C, F. meas. =
	$C_{V(D)}$	Capacitance, V_D Power Supply		35		pF	1 MHz; Tested input = V_{CC}
OUTPUTS	I_{OL}	Output Current, Logic "0"	3.2	5.6		mA	V_O = +0.40 V
	I_{OH}	Output Current, Logic "1"	−1.0	−4.2		mA	V_O = +2.6 V
	I_{OLC}	Output Clamp Current, Logic "0"			8.0	mA	V_O = −1.0 V
	$I_{O(L)}$	Output Leakage Current			1.0	μA	$V_O = V_{CC}$ −5V; $\overline{CS}$ = Logic 1; T_A = 25°C.
	C_{OUT}	Output Capacitance		7	10	pF	T_A = 25°C; F meas. = 1 MHz; $V_O = V_{CC}$

NOTES:

(1) Typical values at V_{CC} = +5 V, $V_D = V_{DD}$ = −9.0 V*, T_A = 25°C.
(*Except Standby Power)

TIMING

(Ambient Temperature Range: 0°C to 75°C; V_{CC} = +5 V ±5%; $V_D = V_{DD}$ = −7V to −13.2 V, unless otherwise specified. See Notes 1 and 2.)

		PARAMETER	MIN	TYP	MAX	UNITS	
OPERATING CONDITIONS	t_{wc}	Write Cycle Time	700			ns	
	t_{wd}	Write Set-up Delay	300			ns	
	t_{wp}	Write Pulse Width	400			ns	
	t_{dld}	Data Lead Time	300			ns	
	t_{dlg}	Data Lag Time	0			ns	
	t_{cw}	Chip Select Pulse Width	400			ns	
DYNAMIC CHAR.	t_{ACC}	Access Time		525	900	ns	$V_D = V_{DD}$ = −9V ±5%.
	t_{RC}	Read Cycle Time			800	ns	(See Note 3.)
	t_{ACC}	Access Time			1.0	µs	$V_D = V_{DD}$ = −7V to −13.2V.
	t_{RC}	Read Cycle Time			900	ns	(See Note 3.)
	t_{OH}	Data Output Hold Time	100			ns	
	t_{CSE}	Chip-Select-to-Output Enable			300	ns	
	t_{CSD}	Chip-Select-to-Output Disable			300	ns	

Random Access Memories

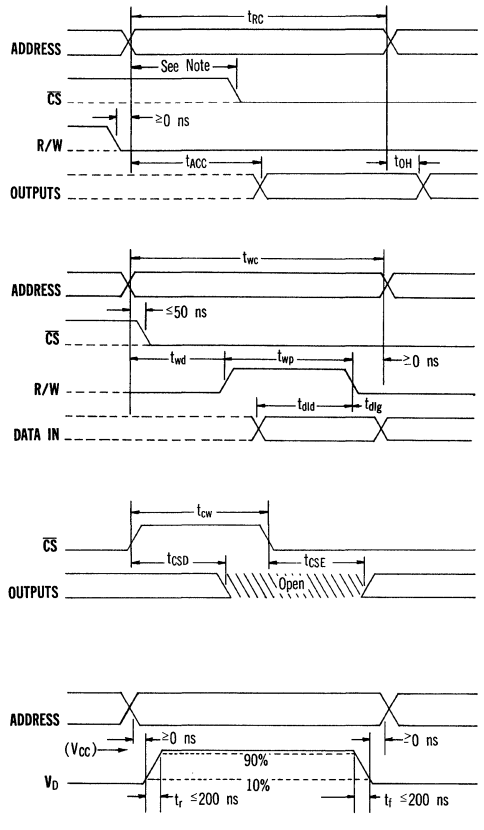
NOTES:

(1) All measurements to the 1.5 V level; inputs for test are 0 to 5 V and ≤10 ns rise and fall times; output is loaded with 1 TTL and approx. 20 pF.

(2) R/W should be brought to logical "0" whenever address bits are changed; however, there are no restrictions on rise and fall times of address bits, nor on the sequence (or skew) of address bit changes.

(3) Read Cycle may be "pipe-lined," i.e., the minimum hold time (t_{OH}) may be subtracted from the maximum access time (t_{ACC}).

TIMING



READ CYCLE

Reading is accomplished with R/W (Read/Write) and $\overline{CS}$ (Chip Select) at logical "0."

NOTE: $\overline{CS}$ logical "1" overlap time shown must be 300 ns (max t_{CSE}) less than the desired access time; e.g., if desired access time t_{ACC} = 1.2 µs, then $\overline{CS}$ should go to logical "0" no later than 900 ns following address change.

WRITE CYCLE

Writing is accomplished with R/W at logical "1" and $\overline{CS}$ at logical "0." $\overline{CS}$ at logical "1" may overlap the address change as much as 50 ns. R/W may be taken to logical "0" coincidentally with an address change, but should not overlap an address change while in the logical "1" state.

CHIP SELECT

$\overline{\text{Chip Select}}$ at logical "1" causes the normal push-pull output buffers to be open-circuited for purposes of wire-ORing. The $\overline{\text{Chip Select}}$ may be used to access the memory at a faster rate by maintaining a constant address and selecting individual chips with the $\overline{\text{Chip Select}}$ input.

POWER SWITCHING

During standby operation the MK 4007 P will dissipate only 30 mW of power (typically) if the peripheral power supply, V_D, is reduced to V_{CC}. The R/W input may be maintained at logical "0" or "1"; however, if R/W is at logical "1," Chip Select should also be logical "1" (to disable chip during standby operation). With the return of power, either read or write cycles may commence as described above.

TYPICAL PERFORMANCE CURVES

FIG. 1: POWER SUPPLY OPERATING REGION & DIFFERENTIAL

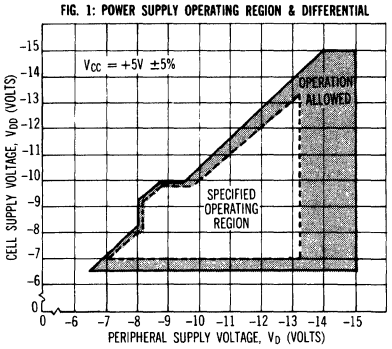


FIG. 2: ACCESS TIME VS SUPPLY VOLTAGE, (V_D)

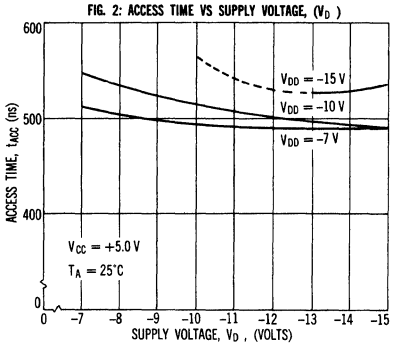


FIG. 3: TOTAL POWER DISSIPATION, (P_D), VS SUPPLY VOLTAGE, (V_D and V_{DD})

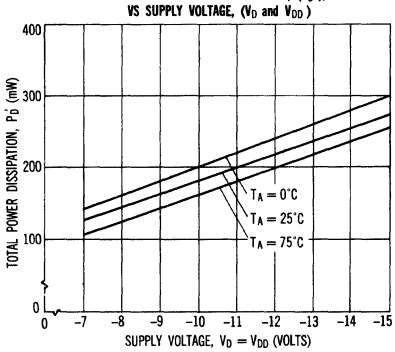


FIG. 4: OUTPUT CURRENT VS OUTPUT VOLTAGE

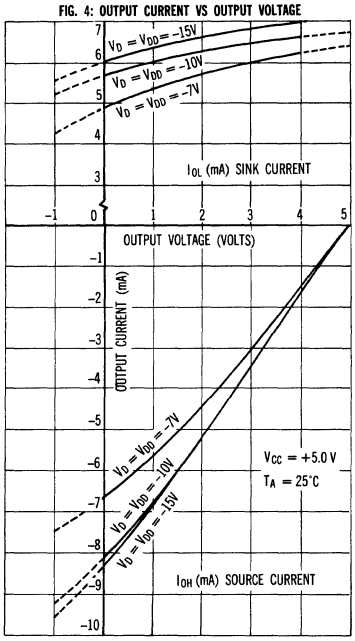


FIG. 5: OUTPUT CURRENT VS AMBIENT TEMPERATURE

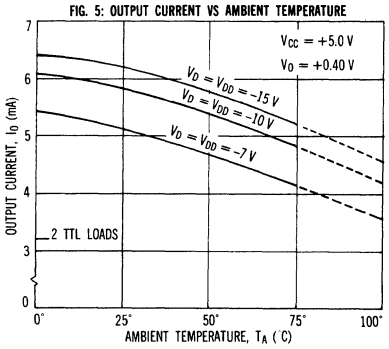


FIG. 6: WORST-CASE ACCESS TIME VS SUPPLY VOLTAGE (At Various Capacitances and Ambient Temperatures)

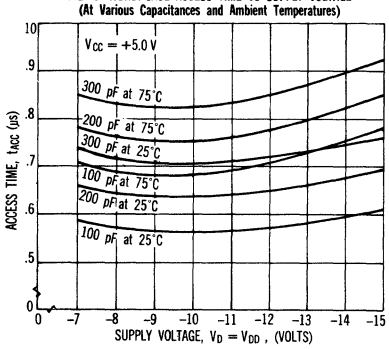


FIG. 7: SUPPLY CURRENT, (I_D and I_{DD}), VS SUPPLY VOLTAGE (V_D and V_{DD})

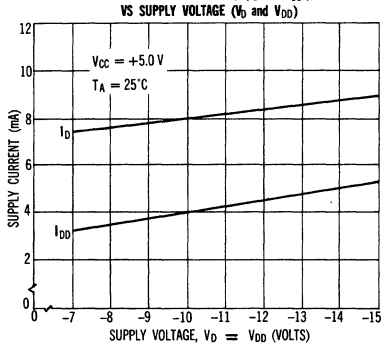
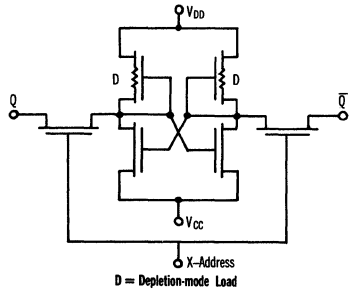
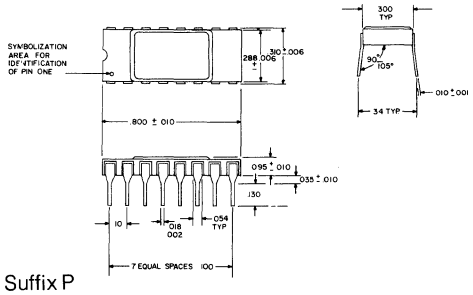


FIG. 8: MK 4007 P MEMORY CELL



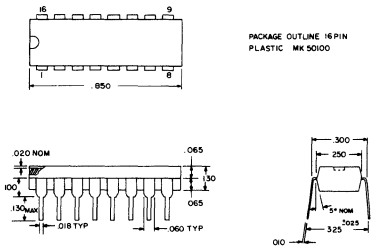
D = Depletion-mode Load

PACKAGE
16-pin ceramic dual-in-line



Suffix P

PACKAGE
16-pin plastic dual-in-line



Suffix N

SUPPLEMENT MK 4007P -4 MK 4007N -4

256-BIT
MOS Random Access Memory

MOSTEK

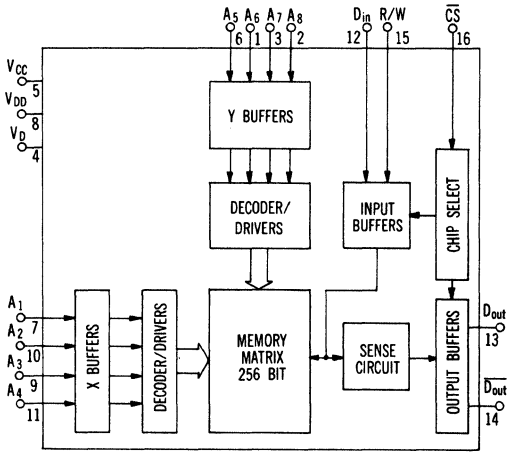
Random Access Memories

- ☐ Low-cost 256x1 RAM in 16-pin package.
- ☐ Identical with Mostek's MK 4007 P in all specifications except output current

DESCRIPTION

This economical version of Mostek's 256x1 bit RAM is identical with the MK 4007 P in all electrical characteristics except output current. Performance, operating conditions, timing characteristics, package, and all other specifications are identical with the MK 4007 P. See the MK 4007 P Data Sheet for additional information.

FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

(Ambient Temperature Range: 0°C to +75°C. V_{CC} = +5 V ±5%; V_D = V_{DD} = −7 V to −13.2 V, unless otherwise specified.)

		PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
POWER	I_D	Supply Current, V_D		8.0	16	mA	V_D = V_{DD} = −9 V ±5%
	I_{DD}	Supply Current, V_{DD}		4.0	9	mA	Outputs open-circuited.
	P_D	Power Dissipation, Total		170	370	mW	
	I_D	Supply Current, V_D			19	mA	V_D = V_{DD} = −13.2 V
	I_{DD}	Supply Current, V_{DD}			10	mA	V_{CC} = +5.25 V
	P_D	Power Dissipation, Total			535	mW	Outputs open-circuited.
	P_{SDBY}	Power Dissipation, Standby		30	75	mW	V_D = V_{CC}; V_{DD} = −9V ±5%
INPUTS	$I_{I(L)}$	Input Leakage Current			1.0	μA	V_{IN} = O V, T_A = 25°C
	C_{IN}	Input Capacitance, Any Logic Input		7	10	pF	T_A = 25°C, F. Meas. =
	$C_{V(D)}$	Capacitance, V_D Power Supply		35		pF	1 MHz; Tested input = V_{CC}
OUTPUTS	I_{OL}	Output Current, Logic "0": @ T_A = 25°C	3.0	5.6		mA	V_O = +0.40 V (V_{CC} = 5.0 V ±5%)
		Output Current, Logic "0": @ T_A = 70°C	2.0			mA	V_O = +0.40 V (V_D = V_{DD} = −9.0 V ±10%)
	I_{OH}	Output Current, Logic "1"	−1.0	−4.2		mA	V_O = +2.6 V
	I_{OLC}	Output Clamp Current, Logic "0"			8.0	mA	V_O = −1.0 V
	$I_{O(L)}$	Output Leakage Current			1.0	μA	V_O = V_{CC} −5V; $\overline{CS}$ = Logic 1; T_A = 25°C.
	C_{OUT}	Output Capacitance		7	10	pF	T_A = 25°C; F meas. = 1 MHz; V_O = V_{CC}

NOTES:

(1) Typical values at V_{CC} = +5 V, V_D = V_{DD} = −9.0 V*, T_A = 25°C.
(*Except Standby Power)

PRELIMINARY

MK 4096 P

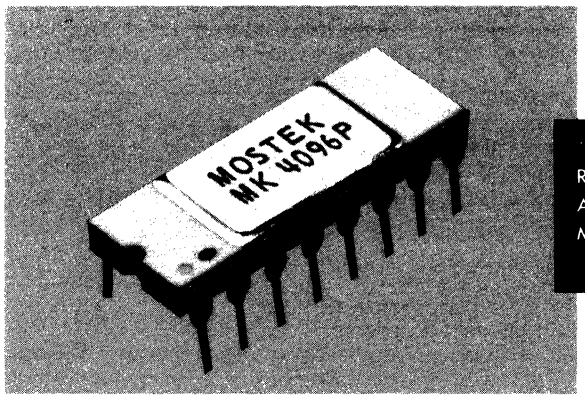
4096x 1 **BIT DYNAMIC**

MOS Random Access Memory

MOSTEK

FEATURES

- ☐ Standard 16-pin DIP
- ☐ All inputs TTL compatible, including the strobes
- ☐ On-chip latches for addresses, chip select, and data in
- ☐ Three-state TTL compatible output
- ☐ Chip select decode does not add to access time
- ☐ Output data latched and valid into next cycle
- ☐ Random read or write cycles under 500 nsec
  random access under 350 nsec
- ☐ Low power: active power under 400 mW
  standby power under 12 mW



DESCRIPTION

The MK 4096 is a 4096x1 bit dynamic random access memory circuit fabricated with MOSTEK's special Self-aligned, Poly-Interconnect, N-channel (SPIN) process to minimize cell area and optimize circuit performance. The single transistor cell uses a dynamic storage technique and each of the 64 row addresses requires refreshing every 2 milliseconds.

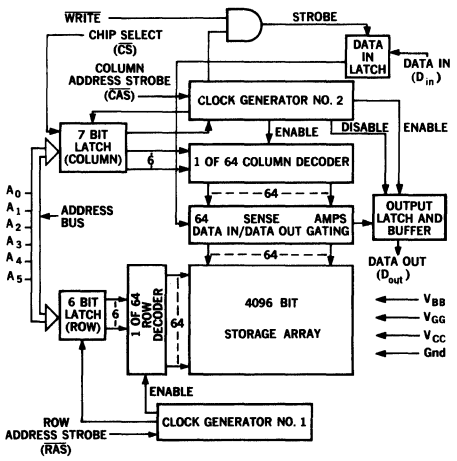
A unique multiplexing and latching technique for the address inputs permits the MK 4096 to be packaged in a standard 16-pin DIP on 0.3-inch centers. This package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features of the MK 4096 include direct interfacing capability with TTL, 6 instead of 12 address lines to drive, on-chip registers which can eliminate the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the speed/power characteristics of his memory system.

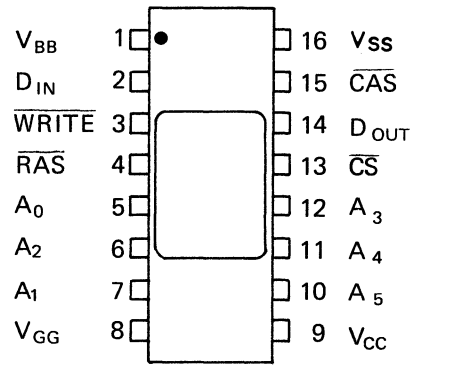
ADDRESSING

The 12 address bits required to decode 1 of 4096 cell locations are multiplexed onto the 6 address pins and latched into the on-chip row and column address latches. The Row Address Strobe ($\overline{RAS}$) latches the 6 row address bits into the chip. The Column Address Strobe ($\overline{CAS}$) latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. Since the Chip Select signal is not required until well into the cycle, its decoding time does not add to the system access or cycle time.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{BB} ..... −0.5V to +30.0V
Operating Temperature (Ambient) ..... 0°C to 70°C
Storage Temperature (Ambient) ..... −55°C to 150°C

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{GG}	Supply Voltage	11.4	12.0	12.6	volts	1
V_{CC}	Supply Voltage	V_{SS}	5.0	V_{GG}	volts	1, 11
V_{SS}	Supply Voltage	0	0	0	volts	1
V_{BB}	Supply Voltage	−9.9	−9.0	−8.1	volts	1
V_{IH}	Logic 1 Voltage, all inputs	2.4	5.0		volts	1, 13
V_{IL}	Logic 0 Voltage, all inputs	−1.0	0	.8	volts	1, 13

RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$) ($V_{GG} = 12.0V \pm 5\%$; $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $V_{BB} = -9.0V \pm 10\%$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{RC}	Random Read or Write Cycle Time	500			nsec	2
t_{RP}	Row Address Strobe Precharge Time	150			nsec	
t_{RCL}	Row to Column Strobe Lead Time	150			nsec	2
t_{CPW}	Column Address Strobe Pulse Width	200			nsec	
t_{AS}	Address Set-Up Time	0			nsec	2, 3
t_{AH}	Address Hold Time	100			nsec	2, 3
t_{RCS}	Read Command Set-Up Time	0			nsec	3
t_{RCH}	Read Command Hold Time	0			nsec	4
t_{RPW}	Read Command Pulse Width	200			nsec	
t_{WCH}	Write Command Hold Time	150			nsec	3, 5
t_{WP}	Write Command Pulse Width	200			nsec	
t_{CRL}	Column to Row Strobe Lead Time	−50		+50	nsec	6
t_{CWL}	Write Command to Column Strobe Lead Time	200			nsec	12
t_{DS}	Data In Set-Up Time	0			nsec	12
t_{DH}	Data In Hold Time	150			nsec	12
t_{RFSH}	Refresh Period			2	msec	
t_{MOD}	Modify Time	0		10	μsec	7

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) ($V_{GG} = 12.0V \pm 5\%$; $V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $V_{BB} = -9.0V \pm 10\%$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{GG1}	Average V_{GG} Power Supply Current (Random Cycle)		10	30	mA	15
I_{CC}	V_{CC} Power Supply Current				mA	8
I_{BB}	Average V_{BB} Power Supply Current (Random Cycle)			100	μA	
I_{GG2}	Standby V_{GG} Power Supply Current			1	mA	
$I_{I(L)}$	Input Leakage Current (any input)			10	μA	9
$I_{O(L)}$	Output Leakage Current			10	μA	10
V_{OH}	Output Logic 1 Voltage @ $I_{OUT} = -5$ mA	2.4			volts	
V_{OL}	Output Logic 0 Voltage @ $I_{OUT} = 2$ mA			0.4	volts	

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) ($V_{GG} = 12.0V \pm 5\%$, $V_{CC} = 5.0 \pm 10\%$, $V_{SS} = 0V$, $V_{BB} = -9.0V \pm 10\%$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{RAC}	Access Time from Row Address Strobe			350	nsec	2, 14
t_{CAC}	Access Time from Column Address Strobe			200	nsec	3
t_{OFF}	Output Buffer Turn-Off Delay	0		100	nsec	3
C_{I1}	Input Capacitance ($A_0 - A_5$)			10	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, D_{IN}, $\overline{WRITE}$, $\overline{CS}$)			7	pF	
C_O	Output Capacitance (D_{OUT})			8	pF	

NOTES

1. All voltages referenced to V_{SS}.
2. Referenced to $\overline{RAS}$ leading edge.
3. Referenced to $\overline{CAS}$ leading edge.
4. Referenced to $\overline{CAS}$ trailing edge.
5. Write Command Hold Time is important only when performing normal random write cycles. During read-write or read-modify write cycles, the Write Command Pulse Width is the limiting parameter.
6. Referenced to the $\overline{RAS}$ trailing edge.
7. Referenced to access time.
8. Depends upon output loading. The V_{CC} supply is connected only to the output buffer.
9. All device pins at 0 volts except V_{BB} at −9 volts and pin under test which is at +10 volts.
10. Output disabled by chip select input.
11. Output voltage will swing from V_{SS} to V_{CC} independent of differential between V_{SS} and V_{CC}.
12. These parameters are referenced to the $\overline{CAS}$ leading edge in random write cycle operation and to the $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
13. Input voltages greater than TTL levels (0 to 5V) require device operation at reduced speed.
14. Assumes $t_{RCL} = 150$ nsec.
15. Typical V_{GG} current at 1.0 MHz cycle rate. Current is proportional to speed with maximum current measured at 2.0 MHz cycle rate.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register. The data is strobed into the register by a combination of $\overline{WRITE}$ and $\overline{CAS}$. The last of these signals making its negative transition is the strobe for the Data In register. This flexibility in timing permits several options in the write timing. In a write cycle, if the $\overline{WRITE}$ input is activated at the beginning of a cycle, then the Data In is strobed by $\overline{CAS}$ and the set-up and hold time are referenced to this signal. In this instance the output will unconditionally go to a logic 1 at access time. If the cycle was to be a read-write cycle or read-modify-write cycle, then the $\overline{WRITE}$ input would not go to a logic 0 until after access time. But now, because $\overline{CAS}$ is already at a logic 0, the Data In is strobed in by $\overline{WRITE}$ and the set-up and hold time are referenced to it. The only other timing constraint in write-type cycles besides Data In set-up and hold time is that both $\overline{WRITE}$ and $\overline{CAS}$ be at a logic 0 for a sufficient time to accomplish the write.

At the beginning of a memory cycle the state of the Data Out latch and buffer depend on the previous memory cycle. If during the previous cycle the chip was unselected, the output buffer will be in its open-circuit condition. If the previous cycle was a read, read-write, or read-modify-write cycle and the chip was selected, then the output latch and buffer will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the previous cycle was a write cycle ($\overline{WRITE}$ active low before access time) and the chip was selected, then the output latch and buffer will contain a logic 1. Regardless of the state of the output it will remain valid until $\overline{CAS}$ goes negative. At that time the output will unconditionally go to its open-circuit state. It will remain open circuit until access time. At access time the output will assume the proper state for the type of cycle performed. If the chip is unselected, it will not accept a $\overline{WRITE}$ command and the output will remain in the open-circuit state.

INPUT/OUTPUT LEVELS

All inputs, including the two address strobes, will interface directly with TTL. The high impedance, low capacitance (<10pF) input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. The three-state output buffer is a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced.

POWER DISSIPATION/STANDBY MODE

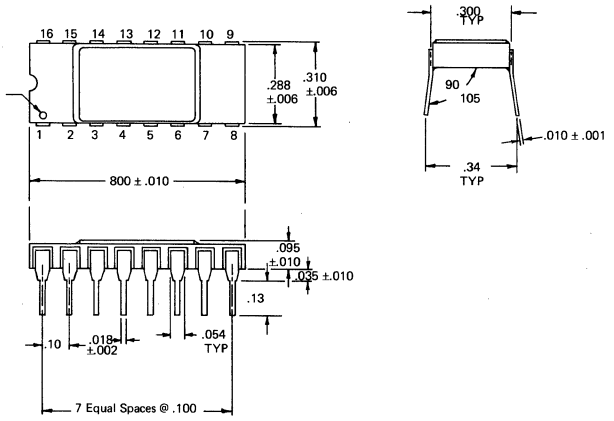
Most of the circuitry used in the MK 4096 is dynamic and draws power only as the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency. Typically, the power is 120mW at a 1 μsec cycle time; with a worst case power of less than 400 mW at a 500 nsec cycle time. To reduce the overall system power the Row Address Strobe ($\overline{RAS}$) must be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected outputs). But those chips that did not receive a $\overline{RAS}$ will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the output. If the $\overline{RAS}$ is decoded and supplied to the selected chips, then the Chip Select input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input.

REFRESH

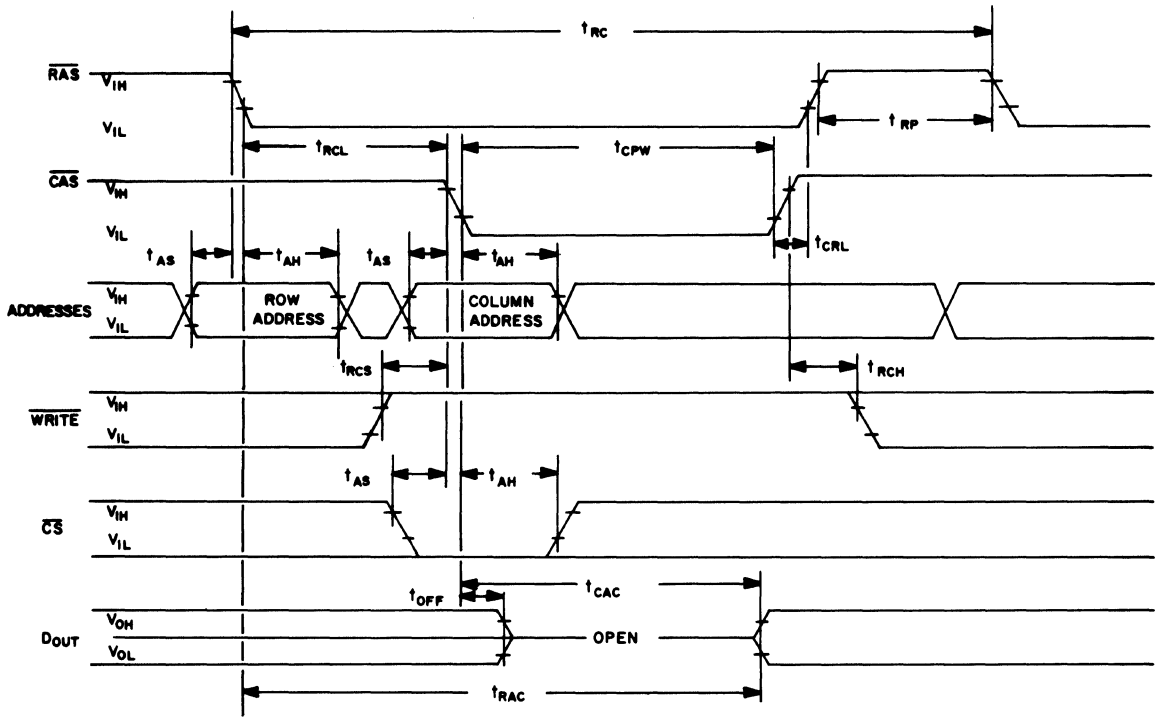
Refresh of the cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses every 2 milliseconds or less. Any read cycle refreshes the selected row, regardless of the state of the Chip Select. A write, read-write, or read-modify-write cycle also refreshes the selected row but the chip should be unselected to prevent writing data into the selected cell.

PACKAGE DESCRIPTION

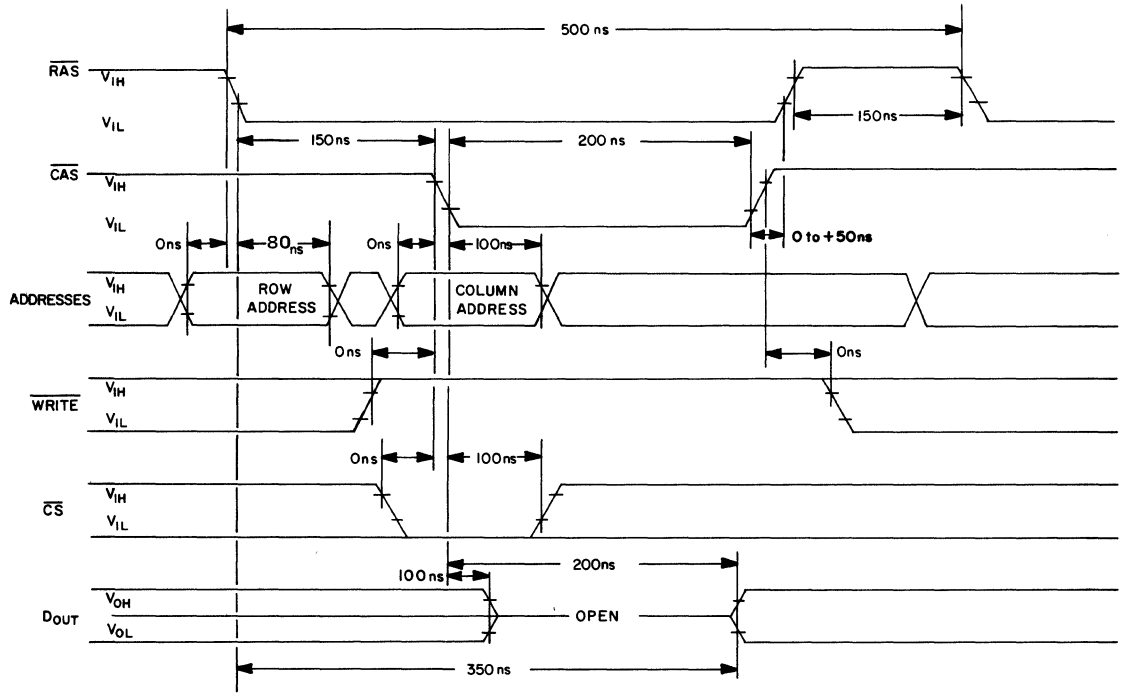
16-lead side-brazed ceramic dual-in-line hermetic package



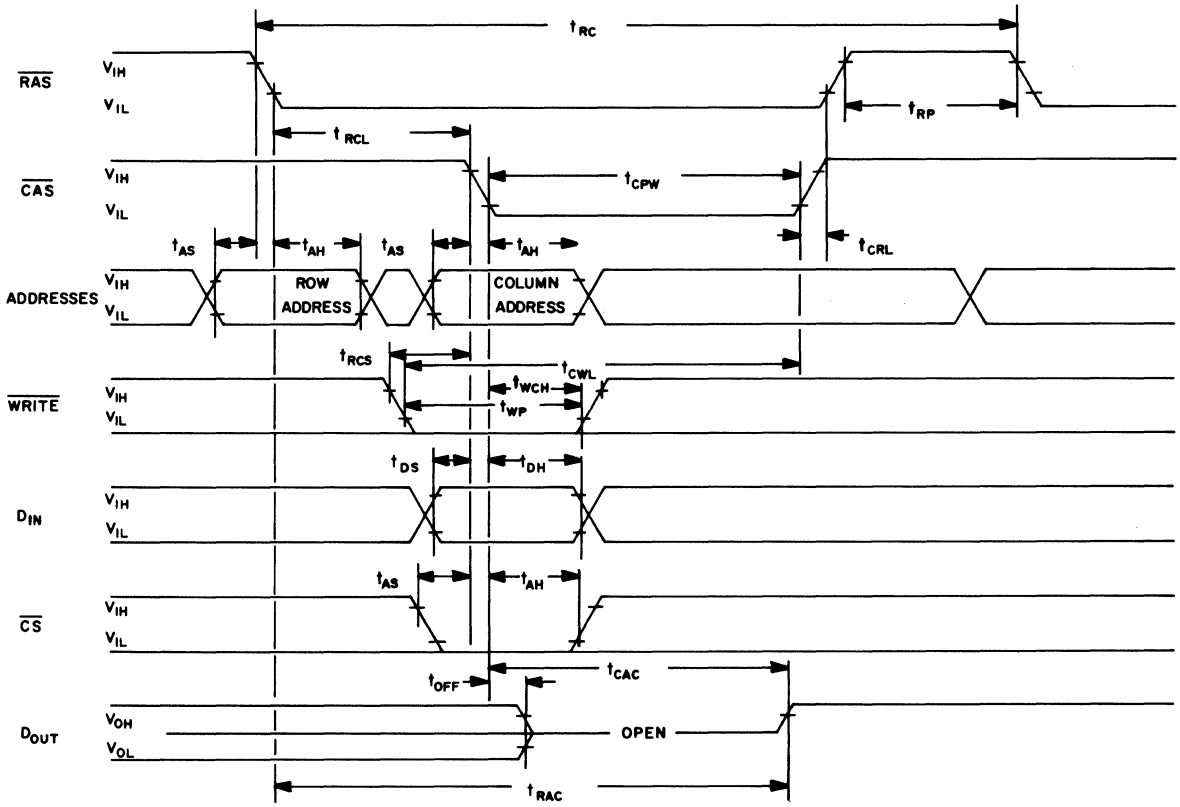
READ CYCLE



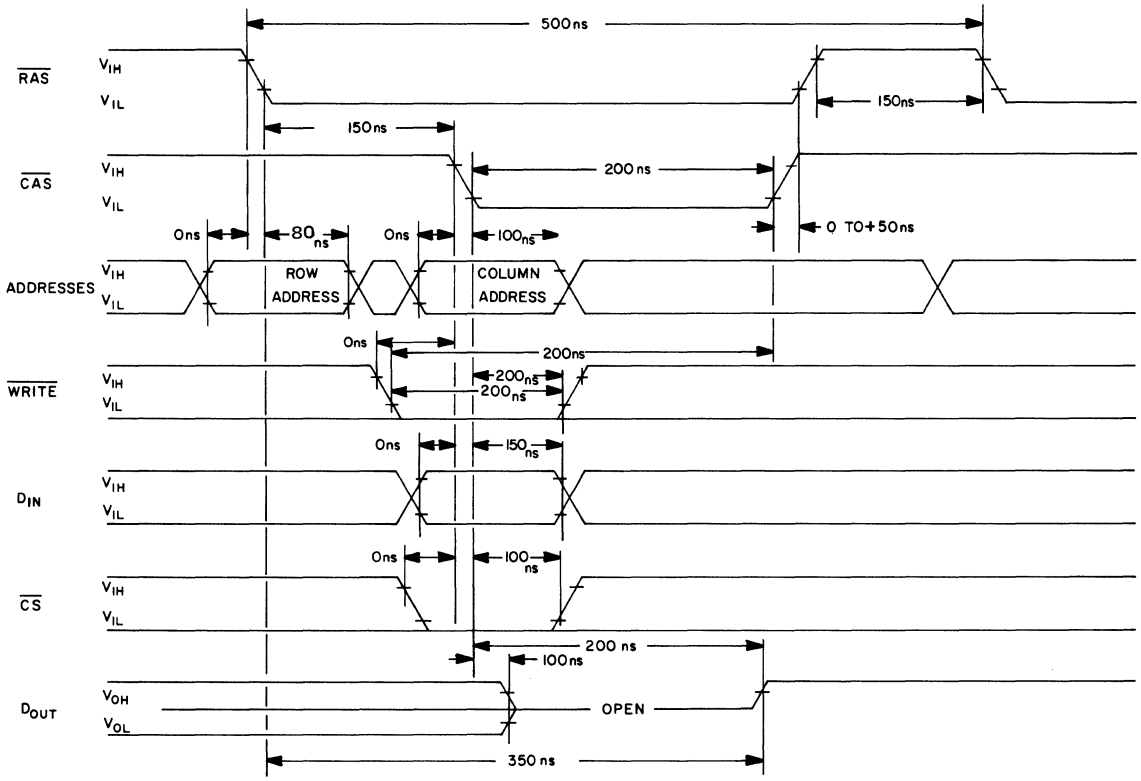
READ CYCLE (minimum timing)



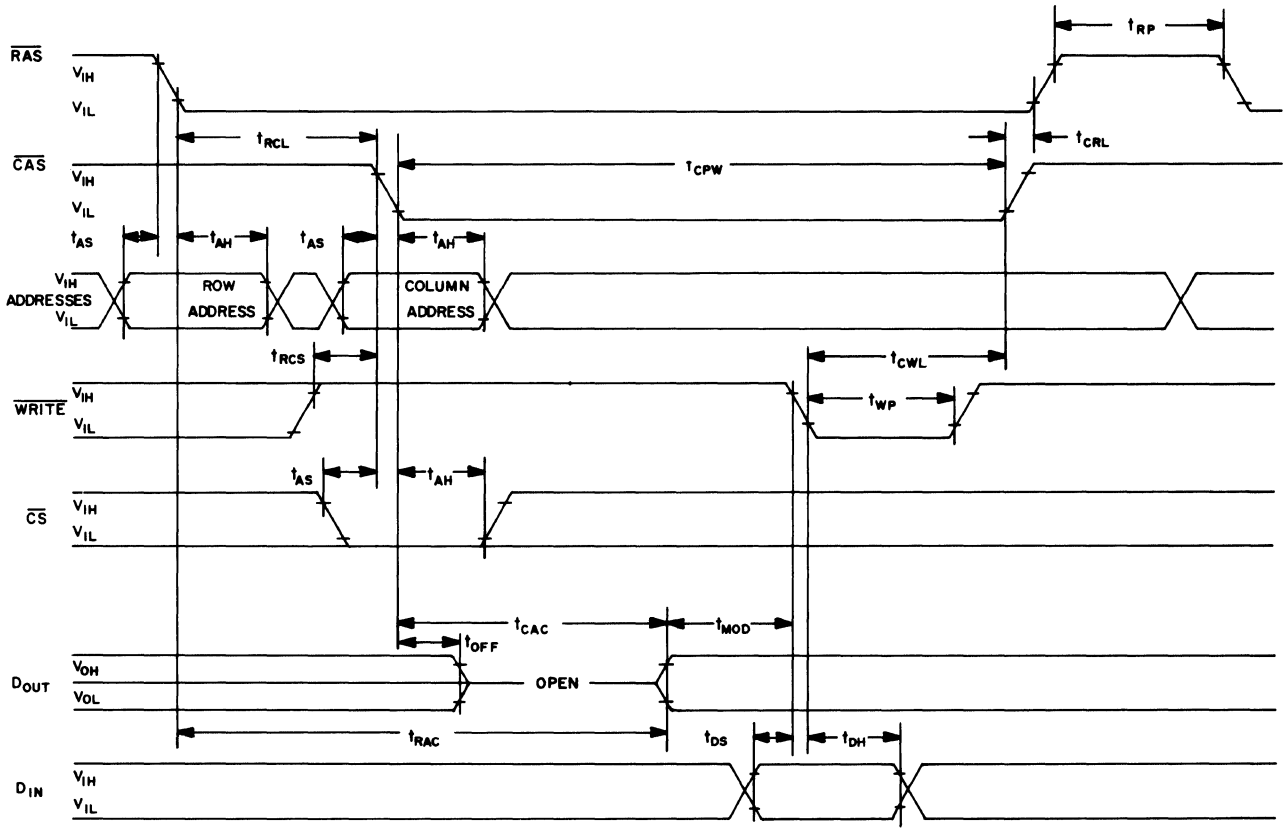
WRITE CYCLE



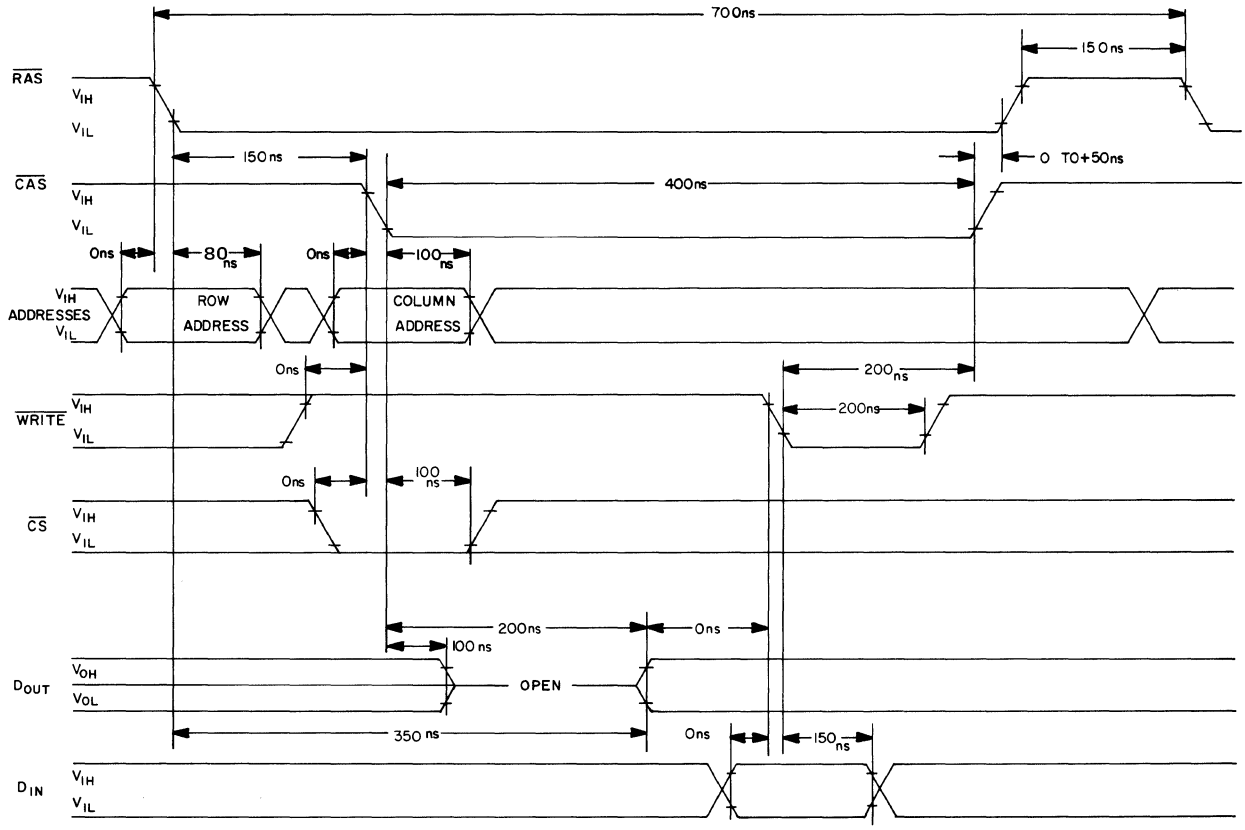
WRITE CYCLE (minimum timing)



READ-MODIFY-WRITE CYCLE



READ-MODIFY-WRITE CYCLE (minimum timing)



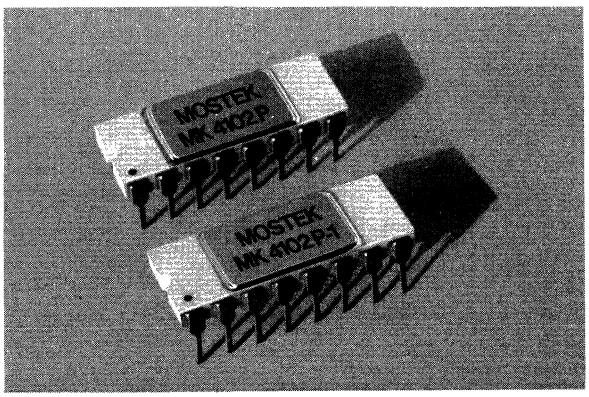
MK 4102 P
MK 4102 P-1

1024x 1 BIT STATIC
MOS Random Access Memory

MOSTEK

FEATURES

- ☐ Direct TTL compatibility — all inputs and output
- ☐ Three-State Output
- ☐ Single supply: +5V
- ☐ Fast access and cycle time:
  MK 4102P 1 μs; MK 4102P-1 450 ns
- ☐ Standard 16-pin DIP
- ☐ Completely static: no clocks or refreshing required



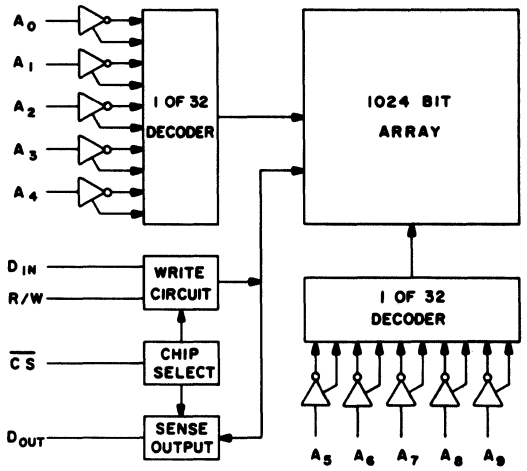
DESCRIPTION

The MOSTEK MK 4102 is a completely static 1024x1 bit random access memory circuit. It is constructed with N-channel silicon gate depletion mode technology.

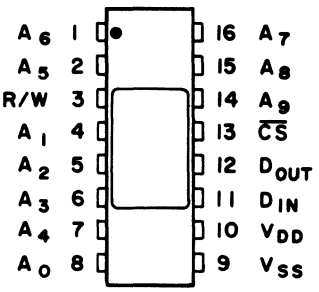
All inputs are directly compatible with TTL circuitry. The output of the memory is a three-state buffer. The high impedance "OFF" state coupled with the Chip Select ($\overline{CS}$) input permits the construction of large memory arrays with a minimum of additional circuitry. The static operation requires very little system overhead and makes the MK 4102 ideally suited to small and medium size memory applications.

The pin connections and functional operation are similar to MOSTEK's popular 1024x1 bit dynamic random access memory chips, the MK 4006 and the MK 4008. By eliminating the dynamic storage the refreshing is not required. This point, in conjunction with the direct TTL compatibility in and out of the memory chip, makes memory system design with the MK 4102 less complicated.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... −0.5V to 7V
Operating Temperature (Ambient) ..... 0°C to 70°C
Storage Temperature (Ambient) ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4102 P — MK 4102 P-1 MIN	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	4.75	5.25	volts	
V_{SS}	Supply Voltage	0	0	volts	
V_{IH}	Input Voltage, Logic 1	2.2	5.25	volts	
V_{IL}	Input Voltage, Logic 0	0	.65	volts	

RECOMMENDED AC OPERATING CONDITIONS[1] ($0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4102 P-1 MIN	MAX	MK 4102 P MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle	450		1000		nsec	
t_{WC}	Write Cycle	450		1000		nsec	
t_{WP}	Write Pulse Width	300		750		nsec	
t_{AW}	Address to Write Pulse Delay	100		200		nsec	
t_{DS}	Data Set-Up Time	330		800		nsec	
t_{DH}	Data Hold Time	50		100		nsec	
t_{CW}	Chip Select Pulse Width	200		300		nsec	
t_{ACW}	Address To Chip Select Delay		50		50	nsec	Write Cycle
t_{ACR}	Address To Chip Select Delay		250		700	nsec	Read Cycle
t_{WA}	Write Pulse to Address Delay	50		50		nsec	

DC ELECTRICAL CHARACTERISTICS ($V_{DD} = +5V \pm 5\%$, $V_{SS} = OV$, $0°C \leq T_A \leq 70°C$)

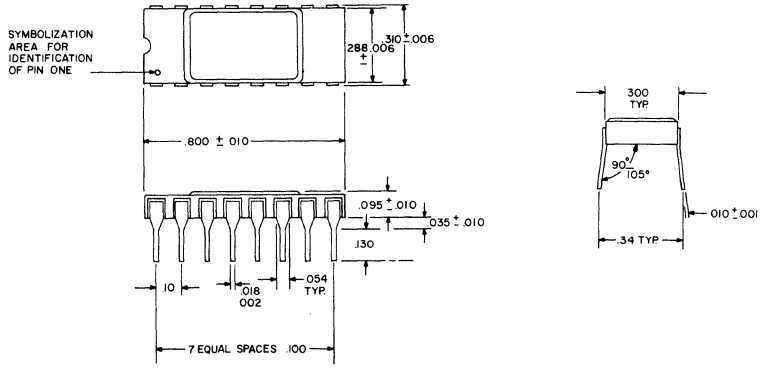
	PARAMETER	MK 4102 P — MK 4102 P-1 MIN	MAX	UNITS	NOTES
I_{DD}	Supply Current		70	mA	output open
I_{LI}	Input Leakage Current		10	μA	$V_{IN} = OV$ to 5.25V[2]
I_{LO}	Output Leakage Current		10	μA	$V_O = 0.4V$ to 5.25V[3]
V_{OH}	Output Voltage, Logic 1	2.2		volts	$I_{OH} = -100\mu A$
V_{OL}	Output Voltage, Logic 0		.40	volts	$I_{OL} = +3.2mA$

AC ELECTRICAL CHARACTERISTICS[1] ($V_{DD} = +5V \pm 5\%$, $V_{SS} = OV$, $0°C \leq T_A \leq 70°C$)

	PARAMETER	MK 4102 P-1 MIN	MAX	MK 4102 P MIN	MAX	UNITS	NOTES
t_{ACC}	Access Time		450		1000	nsec	
t_{CS}	Chip Select Time		200		300	nsec	
t_{CD}	Chip Deselect Time		200		300	nsec	
C_I	Input Capacitance (Any Input)		6		6	pF	f = 1MHz $V_I = OV$@25°C
C_O	Output Capacitance		10		10	pF	f = 1MHz $V_I = OV$@25°C

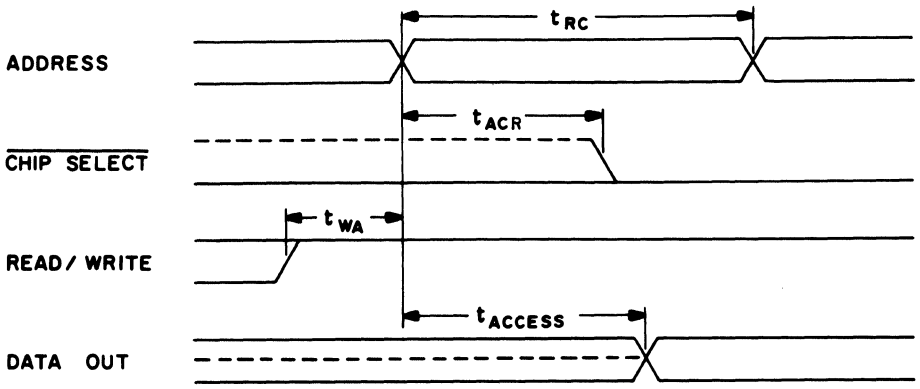
Notes: (1) AC Test Conditions: input voltage swings = +.4V to 2.4V, input rise and fall times = 20 nsec; measurement point on signals = 1.5V; and output load = 1 standard TTL load +100pF.
(2) $V_{SS} = V_{DD} = OV$
(3) Chip disabled

PACKAGE (16-lead ceramic dual-in-line hermetic package)

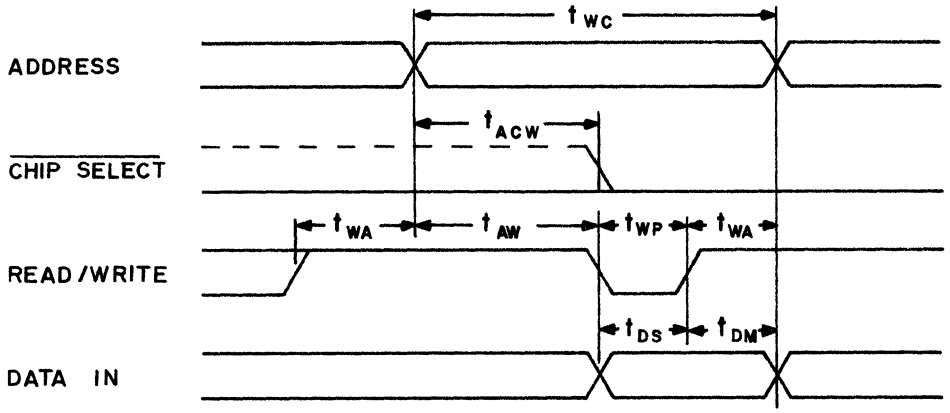


TIMING

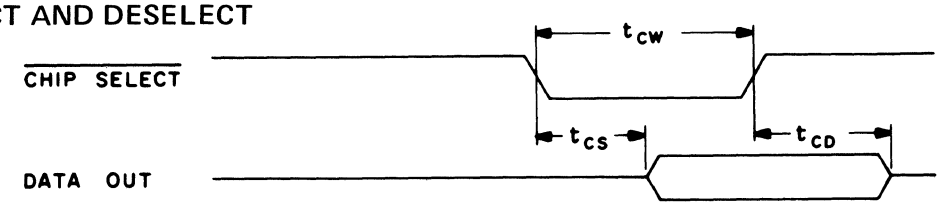
READ CYCLE



WRITE CYCLE



CHIP SELECT AND DESELECT



This timing assumes that the addresses for at least t_{ACR} prior to $\overline{\text{Chip Select}}$.

PRELIMINARY

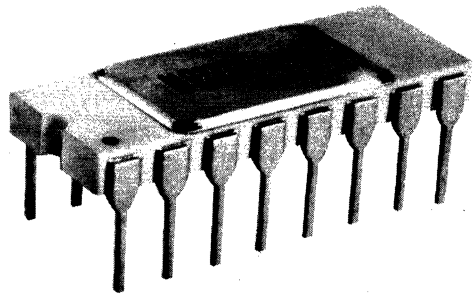
MK 4102P-6

1024x1 BIT STATIC
MOS Random Access Memory

MOSTEK

FEATURES:

- ☐ Direct TTL compatibility – all inputs and output
- ☐ Three-State Output
- ☐ Single supply: +5V
- ☐ Fast access and cycle time: 275 ns
- ☐ Standard 16-pin DIP
- ☐ Completely static: no clocks or refreshing required



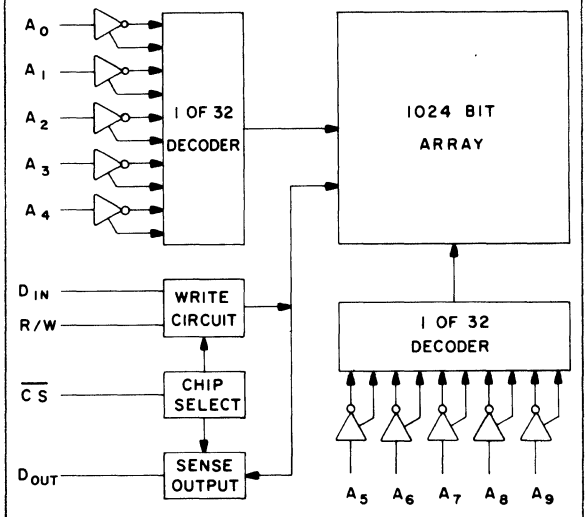
DESCRIPTION:

The MOSTEK MK 4102-6 is a completely static 1024x1 bit random access memory circuit. It is constructed with N-channel silicon gate depletion mode technology.

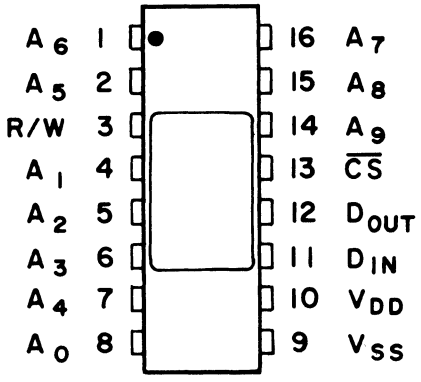
All inputs are directly compatible with TTL circuitry. The output of the memory is a three-state buffer. The high impedance "OFF" state coupled with the Chip Select (CS) input permits the construction of large memory arrays with a minimum of additional circuitry. The static operation requires very little system overhead and makes the MK 4102-6 ideally suited to small and medium size memory applications.

The pin connections and functional operation are similar to MOSTEK's popular 1024x1 bit dynamic random access memory chips, the MK 4006 and the MK 4008. By eliminating the dynamic storage the refreshing is not required. This point, in conjunction with the direct TTL compatibility in and out of the memory chip, makes memory system design with the MK 4102-6 less complicated.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... −0.5V to 7V

Operating Temperature (Ambient) ..... 0°C to 70°C

Storage Temperature (Ambient) ..... −55°C to +150°C

RECOMMENDED DC OPERATING CONDITIONS ($0°C < T_A < 70°C$)

	PARAMETER	MIN	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	4.75	5.25	volts	
V_{SS}	Supply Voltage	0	0	volts	
V_{IH}	Input Voltage, Logic 1	2.2	5.25	volts	
V_{IL}	Input Voltage, Logic 0	0	.65	volts	

RECOMMENDED AC OPERATING CONDITIONS ($0°C < T_A < 70°C$)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle	275		nsec	
t_{WC}	Write Cycle	275		nsec	
t_{WP}	Write Pulse Width	200		nsec	
t_{AW}	Address to Write Pulse Delay	0		nsec	
t_{DS}	Data Set-Up Time	175		nsec	
t_{DH}	Data Hold Time	50		nsec	
t_{CW}	Chip Select Pulse Width	175		nsec	
t_{WA}	Write Pulse To Address Delay	50	50	nsec	Write Cycle
t_{ACR}	Address to Chip Select Delay		125	nsec	Read Cycle
t_{OH}	Output Hold Time	50		nsec	Chip Must Remain Selected
t_{ACW}	Address to Chip Select Delay		50	nsec	Write Cycle

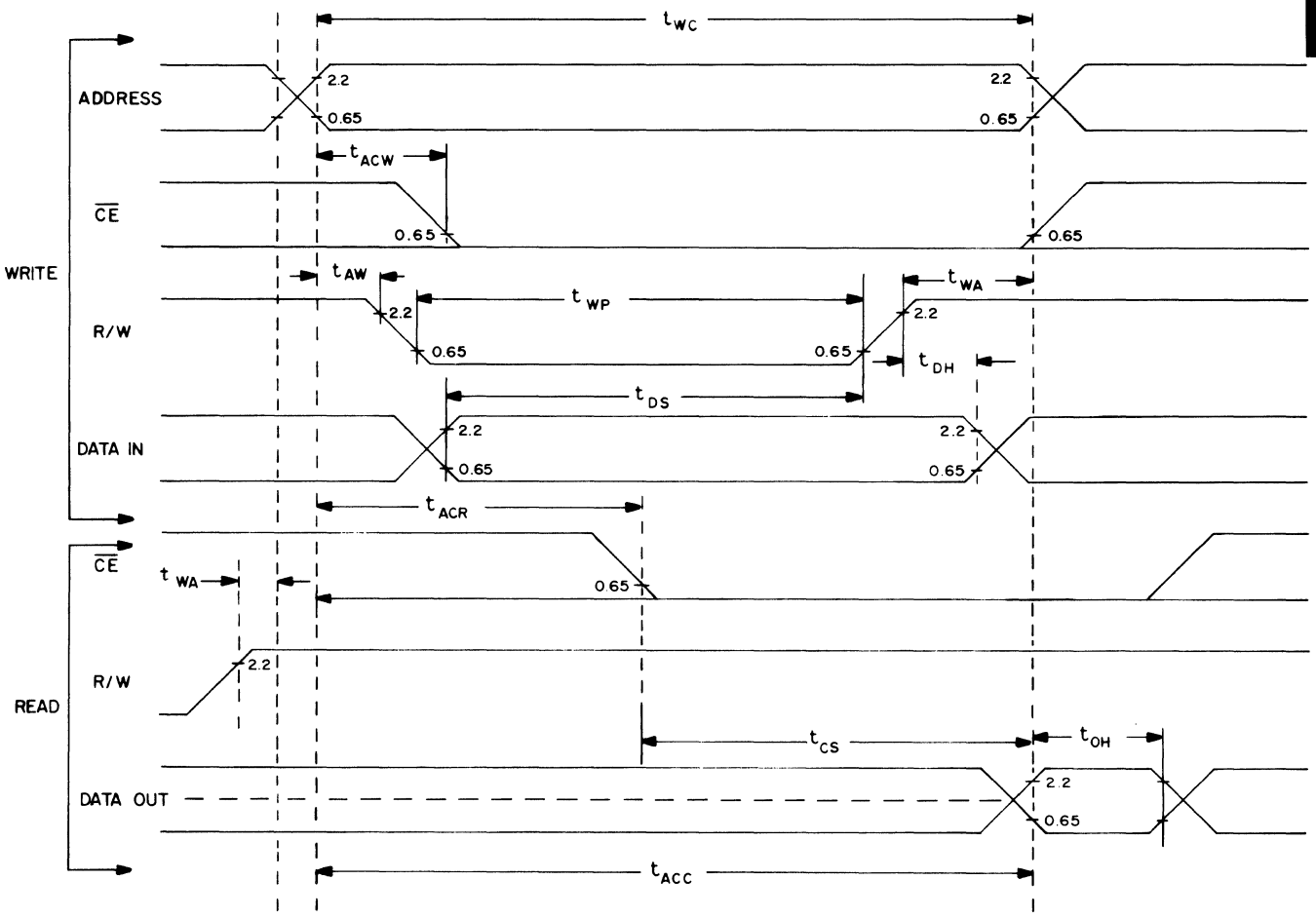
DC ELECTRICAL CHARACTERISTICS (V_{DD}= +5V ± 5%, V_{SS} = 0V, $0°C < T_A < 70°C$)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD}	Supply Current		80	mA	output open
I_{LI}	Input Leakage Current		10	µA	V_{IN} = 0V to 5.25 V
I_{LO}	Output Leakage Current		10	µA	V_O = 0.4V to 5.25V
V_{OH}	Output Voltage, Logic 1	2.2		volts	I_{OH}= -100 µA
V_{OL}	Output Voltage, Logic 0		.40	volts	I_{OL} = +3.2 mA

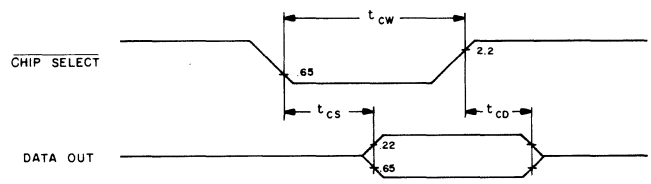
AC ELECTRICAL CHARACTERISTICS (V_{DD}= +5V ± 5%, V_{SS} = 0V, 0°C < T_A < 70°C)

	PARAMETER	MIN	MAX	UNITS	NOTES
t_{ACC}	Access Time		275	nsec	
t_{CS}	Chip Select Time		150	nsec	Address stable for T_{ARC}
t_{CD}	Chip Deselect Time		100	nsec	
C_I	Input Capacitance (Any Input)		5	pF	f = 1MHz V_I = 0V@25°C
C_O	Output Capacitance		10	pF	f = 1MHz V_I =0V@25°C

TIMING

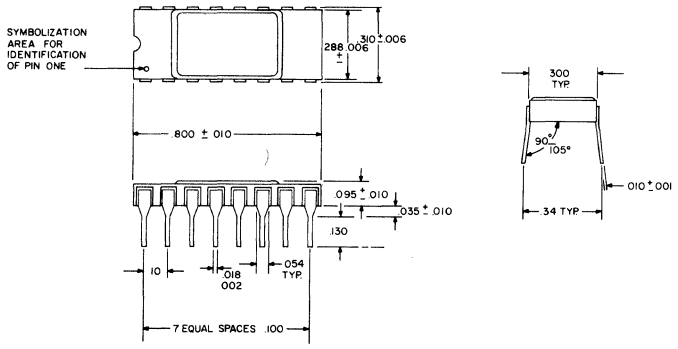


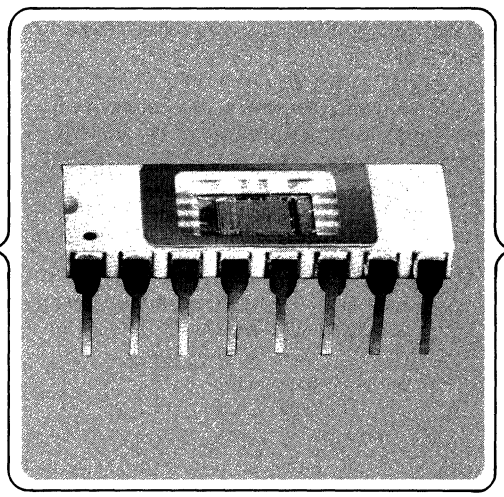
CHIP SELECT AND DESELECT



This timing assumes that the addresses for at least t_{ACR} prior to $\overline{\text{Chip Select}}$.

PACKAGE (16-lead ceramic dual-in-line hermetic package)





Microprocessors

PRELIMINARY

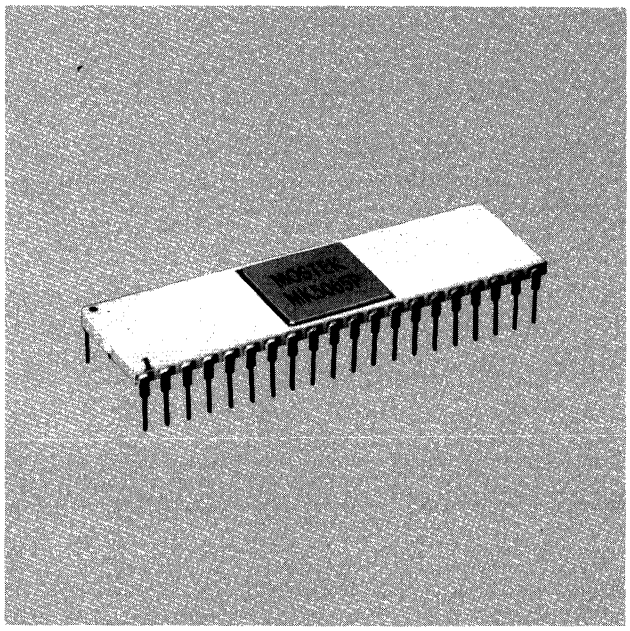
MK 5065P

8-BIT Microprocessor

MOSTEK

FEATURES:

- ☐ 8-bit parallel microprocessor on a single chip
- ☐ 51 basic instructions/81 instructions with modifications
- ☐ TTL compatible inputs and outputs
- ☐ Directly addresses 32Kx8 bit memory
- ☐ Triple level architecture for rapid interrupt servicing
- ☐ Single 40-pin package
- ☐ DMA capability
- ☐ Requires standard power supply voltages
- ☐ Indirect addressing capability



DESCRIPTION

Instructions and data are transmitted to the CPU on a bidirectional 8-bit bus. An 8-bit outbut bus is used along with the bidirectional bus to provide simultaneous memory addresses for addressing up to 32KX8 bits of memory.

Six control input signals provide control of the CPU and seven status output signals indicate the current status of the CPU.

Up to 32KX8 bits of memory may be addressed either directly or indirectly by the CPU. The memory is addressed in a page mode. Each page of memory consists of 256 locations, and there are 128 pages of memory. If subroutine call and return instructions are to be used, the first page of memory must be implemented with RAM because page zero is used as a subroutine return address stack. Thus up to 128 subroutine levels may be nested.

The MK 5065 is capable of executing 51 basic instructions. These basic instructions may be modified by instruction modification fields in the instruction format to expand the total number of executable instructions to 81. These instructions are divided into ten functional instruction categories:

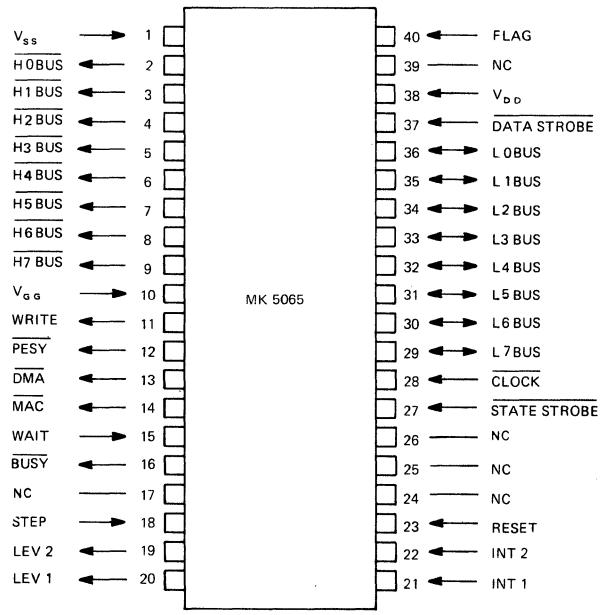
1. Accumulator Instructions
2. Immediate Instructions
3. Memory Instructions
4. Jump Instructions
5. Shift Instructions
6. Exchange Instructions
7. Skip Instructions
8. Status Change Instructions
9. Accumulator/Link Instructions
10. Input/Output Instructions

Seven instruction formats provide direct or indirect, page or entire memory addressing capability. Additionally operations involving immediate data may be performed. A 4-bit "free field" in the I/O instruction allows the user to define a program controlled peripheral communication language set.

Two independent interrupt lines which are selectively enabled under program control select one of three operating levels for the CPU.

DMA capability is provided by a wait input signal and a DMA output signal which indicates when the CPU has completed the last memory cycle in the current instruction execution.

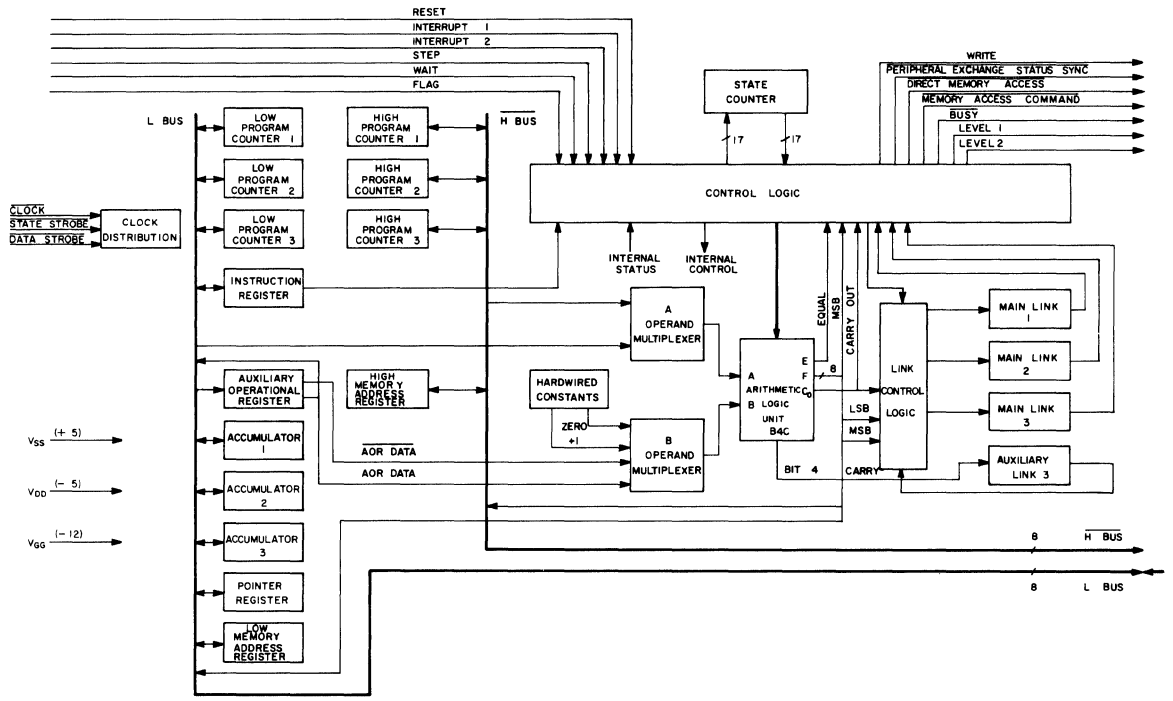
PIN CONNECTION



NC = NO CONNECTION

Micro processors

BLOCK DIAGRAM



Micro processors

BLOCK DIAGRAM DESCRIPTION

As shown in the CPU Block Diagram above, the MK 5065 is organized as a triple level parallel central processing unit. Each of the three operating levels contains a program counter, accumulator, and main link. In addition to these elements, level 3 also has an auxiliary link for storage of carrys and borrows beyond the fourth bit.

Since each level has a program counter, accumulator, and main link for that level there is no need to store in memory the contents of the program counter, accumulator, and machine status information when servicing interrupts. Thus interrupt response is very rapid, the only delay being the time required for the CPU to complete the execution of the current instruction.

The CPU uses two 8-bit buses to communicate with the external devices that comprise the remainder of the system. The HBUS (High Bus) is an 8-bit parallel output bus that transmits the most significant byte of the memory address register contents to the program memory during memory read or write cycles. The LBUS (Low Bus) is a parallel 8-bit bidirectional bus that is used to transmit the least significant byte of the memory address register contents to the program memory during memory read or write cycles. Accumulator data is transmitted to the program memory during a memory write cycle over the LBUS too. This same bidirectional bus is also used to load memory instructions into the instruction register and immediate memory data into the accumulator.

A parallel arithmetic logic unit provides the capability of performing arithmetic or logical operations on two operands selected by the two operand multiplexers.

Instruction execution is controlled by the control logic and state counter.

The 32Kx8 bit memory is organized as eight 4K blocks. Each block consists of 16 pages. Each page consists of 256 words of 8 bits. The memory may be composed of a mix of ROM and RAM although page zero must be implemented with RAM if subroutine instructions are to be used. Page zero of the memory is used as subroutine return address stack. Each adjacent pair of bytes stores the absolute subroutine return address. Thus, up to a maximum of 128 subroutines may be nested. An 8-bit pointer register is used to store the address of the next free position in the stack.

Both direct and indirect memory addressing modes are available. In the direct addressing mode, an absolute memory address on either the current page or on page zero is specified by the second byte of the instruction. In the indirect mode of addressing, the second byte of the instruction specifys the absolute address on either the current page or page zero of the first of two adjacent bytes that contain the address of the operand. The most significant bit of this 16 bit address specifys whether the address is a direct or an indirect address. Since any memory location may contain either an operand or another indirect address, a chain of addresses in memory may specify the actual location of the operand referenced by an instruction.

Multiple interrupt handling capability is provided by two interrupt input signals. Level 3 is the lowest priority operating level. If the CPU is operating on level 3 and an interrupt two (INT2) signal is received, the CPU begins operating on level 2 at the completion of the execution of the instruction currently being executed on level 3 if the interrupt two input has been previously enabled by an Interrupt On or (ION) instruction.

Since the program counter, accumulator, and main links exist in triplicate it is not necessary to go through the usual procedure of saving the contents of these elements when servicing an interrupt or executing a subroutine call instruction. Similarly when executing a return from a subroutine it is not necessary to restore the contents of these units since their previous contents have been preserved in the hardware dedicated to that particular level.

Interrupt one (INT 1) has the highest priority level. Two Level signals (LEV 1 and LEV 2) define the level on which the CPU is operating. If the LEV 1 output signal is a logical one, the CPU is operating on level one. If the LEV 2 signal is a logical one, then the CPU is operating on Level two. If neither the LEV 1 nor the LEV 2 signal is a logical one, then the CPU is operating on Level 3.

I/O operations use the HBUS and the LBUS for transmitting data and commands to the peripherals and for transmitting data and status from the peripherals to the CPU. During the first state strobe pulse the least significant six bit byte of the input or output instruction and the contents of the accumulator are transmitted to the peripheral. During the second state strobe pulse peripheral data is clocked into the peripheral output register if an input instruction is being executed. During the third-state strobe pulse data in the peripheral output register is clocked into the CPU. Finally the fourth state strobe pulse defines the end of the transfer and may be used to reset the peripheral.

Instructions are grouped into ten classifications:

1. Accumulator Instructions — Instructions involving the accumulator.
2. Immediate Instructions — Instructions in which the operand is immediate data.
3. Memory Instructions — Instructions that modify memory contents.
4. Jump Instructions — Jump instructions and subroutine call and return instructions.
5. Shift Instructions — Instructions which rotate accumulator contents.
6. Exchange Instructions — Instructions which cause internal register and byte transfers.
7. Skip Instructions — Conditional instructions which cause the next instruction to be skipped.
8. Status Change Instructions — Instructions which modify machine status.
9. Accumulator/Link Instructions — Instructions which modify the accumulator and/or link contents.
10. Input/Output Instructions — Instructions that input and output data to and from the CPU.

Seven instruction formats are used in the instruction set. There are three two byte instruction formats and four single byte instruction formats.

In the first instruction format, the most significant six bits of the first byte of the instruction contain the instruction code. The two least significant bits of the first byte of the instruction are instruction modification bits. The least significant bit of the first byte of the instruction specifies that the operand address contained in the second byte of the instruction is on the current page when this bit is a logical one. When the LSB of the first byte is a logical zero, the address specified by the second byte is on page zero of the memory. The next MSB of the first byte of the instruction specifies direct addressing mode when this bit is a logical zero. A logical one specifies indirect addressing mode. The second byte of the instruction is an eight bit address field that contains the address of the operand or jump location on the specified page.

The second instruction format is also a two byte format. The four most significant bits of the first byte of the instruction contain the instruction code. The four least significant bits of the first byte of the instruction and the entire eight bit field of the second byte of the instruction form a 12-bit address field. This format is used for jump immediate and call subroutine immediate instructions. The location specified by the address field is located in the same 4KX8 block of memory as the instruction. That is, the four most significant bits of the address are the same as the four most significant bits of the memory address of the instruction.

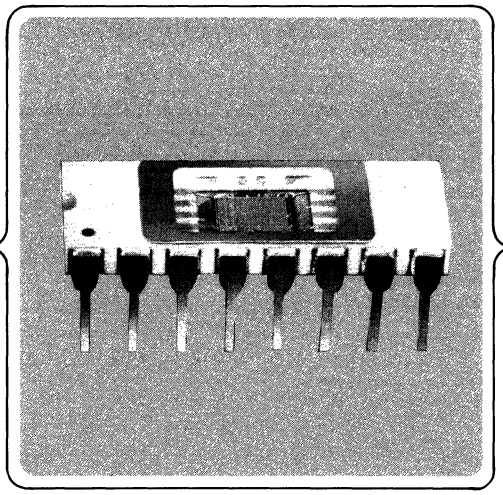
The first byte of the third instruction format contains the instruction code. The second byte contains the immediate operand.

Jump shift, exchange, skip and status change instructions use the fourth instruction format. The entire eight bit field of this single byte instruction contains the instruction code.

I/O instructions use the fifth instruction format. The most significant four bits of the instruction contains the instruction code. The second four bit byte of the instruction is a free field. The CPU does not make use of this field of the instruction. Thus, this free field may be used to define an I/O peripheral communication code.

The accumulator/link instruction makes use of the sixth instruction format. The three most significant bits of the instruction contain the instruction code. The five least significant bits of the instruction specify one of 28 possible instruction modifications.

Interrupts may be selectively enabled or disabled using the seventh instruction format. The six most significant bits of this instruction contain the instruction code. The two least significant bits define the interrupt that is to be enabled or disabled by the instruction. The least significant bit specifys interrupt one and the second modifier bit specifies interrupt two.

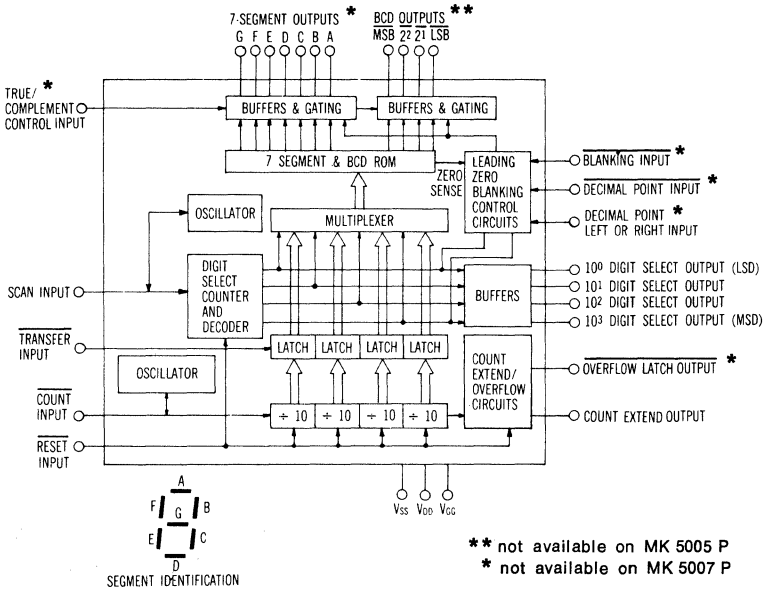


Special Products

MOS 4-Digit Counter/Display Decoder

MOSTEK

FUNCTIONAL DIAGRAM



** not available on MK 5005 P
* not available on MK 5007 P

Special Products

GENERAL DESCRIPTION

The MK 5002/5/7 P is an ion-implanted, P-channel MOS four-decade synchronous counter with latches, multiplexing circuits, and a read-only memory programmed for seven-segment outputs and BCD outputs. In addition, many on-chip control circuits provide flexibility of use with a minimum of external components.

The MK 5002/5/7 P provides a means of counting up to 9999, transferring the count into latches without interrupting the counting operation, and supplying the latched information to the outputs one decade at a time. Scanning is controlled by the Scan Input which increments a one-of-four counter on its negative edge, thereby scanning the latches from MSD (Most Significant Digit) to LSD (Least Significant Digit).

Low threshold voltages for input DTL/TTL compatibility are achieved through Mostek's ion-implantation process. Enhancement mode, as well as depletion-mode, devices are fabricated on the chip, allowing it to operate from a single +5V power supply. Depletion-mode technology also allows the entire circuit to operate on less than 25 mW of power.

The functional diagram shows all options available on the MK 5002 P MOS/LSI. Other members of this family which are different pin-outs of this same chip are the MK 5005 P and MK 5007 P. The MK 5005 P is supplied in a 24 pin package and does not include the BCD outputs. The MK 5007 P is supplied in a 16 pin package. (See the pin diagrams for these members of the counter/display decoder family.)

TRUTH TABLES

INPUT TRUTH TABLE

Input	Logic Condition to Activate
$\overline{\text{Count}}$	Negative Edge
$\overline{\text{Reset}}$	0
$\overline{\text{Transfer}}$	0
Scan	1 (Negative Edge increments Digit Select Counter)
True/Complement	1 = True Data 0 = Complementary Data
$\overline{\text{Decimal Point}}$	0
$\overline{\text{Blanking}}$	0
Decimal Point Left or Right	1 = Left 0 = Right

7-SEGMENT & BCD OUTPUTS TRUTH TABLE

		DISPLAY SEGMENT							BCD			
Digit	Scan	a	b	c	d	e	f	g	MSB	2^2	2^1	LSB
0	1	0	0	0	0	0	0	1	1	1	1	1
1	1	1	0	0	1	1	1	1	1	1	1	0
2	1	0	0	1	0	0	1	0	1	1	0	1
3	1	0	0	0	0	1	1	0	1	1	0	0
4	1	1	0	0	1	1	0	0	1	0	1	1
5	1	0	1	0	0	1	0	0	1	0	1	0
6	1	0	1	0	0	0	0	0	1	0	0	1
7	1	0	0	0	1	1	1	1	1	0	0	0
8	1	0	0	0	0	0	0	0	0	1	1	1
9	1	0	0	0	0	1	0	0	0	1	1	0
X	0	1	1	1	1	1	1	1	1	1	1	1

True/Complement = Logic 1

TRUTH TABLE, OTHER OUTPUTS

Output	True Logic State	Time of Occurrence
Digit Select Outputs	1	One-of-four, following Scan Input rising edge; all off when Scan Input is low.
$\overline{\text{Overflow Latch}}$	0	Occurs on the 10,000th Count Input following a reset. Remains true until an external reset is accomplished.
Count Extend	1	Occurs each time the counter state attains 9,999 count. Remains true only until the next Count Input or Reset occurs (when the counter returns to 0,000).

RECOMMENDED OPERATING CONDITIONS

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
T_A	Operating Temperature Range	0		75	°C	
V_{SS}	Supply Voltage	4.5		7.5	V	1, 2
V_{GG}	Supply Voltage	V_{DD}		-13.2	V	1, 2

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 5\%$; $V_{GG} = V_{DD} = 0$ V; $0° C \leq T_A \leq 70° C$ unless otherwise noted)

		PARAMETER	MIN	TYP	MAX	UNITS	NOTES
D. C. CHARACTERISTICS	V_{IL}	Input Voltage, Logic 0 (Low)		V_{DD}	$V_{DD}+0.8$	V	
	V_{IH}	Input Voltage, Logic 1 (High)	$V_{SS}-1$	V_{SS}	$V_{SS}+0.3$	V	3
	I_{SS}	Supply Current, V_{SS}		2.5	5.0	mA	4, Inputs open
	I_{GG}	Supply Current, V_{GG}		0.2	0.5	mA	V_{GG}=-12V
	C_{in}	Input Capacitance		3	10	pF	T_A=25°C; f=1MHz; $V_{IN}=V_{SS}$
	I_{IL}	Input Current, Logic 0, Count Input			1.6	mA	5
		Scan Input			1.6	mA	5
		Decimal Point Input			1.0	µA	
		Other Logic Inputs			1.0	mA	
	I_{OL}	Output Current, Logic 0	0.5			mA	6, V_{GG}=-12V
	I_{OH}	Output Current, Logic 1	0.5			mA	6, V_{GG}=-12V
	V_{OL}	Output Voltage, Logic 0			$V_{DD}+0.2$	V	4
	V_{OH}	Output Voltage, Logic 1	$V_{SS}-0.2$			V	4
DYNAMIC CHARACTERISTICS	f_{CI}	Count Input Frequency	DC		250	KHz	
	f_{SI}	Scan Input Frequency	DC		50	KHz	
	t_{RD}	Reset to Any Output Delay			15	µs	
	t_{PW}	Logic 0 Pulse Width, Reset Input	1.0			µs	
		Count Input	1.0			µs	
		Scan Input	10.0			µs	
		Transfer Input	2.5			µs	
	t_{PH}	Logic 1 Time, Count Input	3.0			µs	
		Scan Input	10.0			µs	
	t_{SD}	Scan to Output Disable Time					
		Digit Select Outputs			15	µs	7
		All Data Outputs			15	µs	7
	t_{SE}	Scan to Output Enable Time					
		Digit Select Outputs			15	µs	8
		All Data Outputs			15	µs	8
	t_{CE}	Count Input to Count Extend Delay to 1 or 0			15	µs	9
	t_{OF}	Count Input to Overflow Delay (On)			15	µs	9
	t_{ROF}	Reset Input to Overflow Delay (Off)			5	µs	

NOTES:
1. V_{DD} = 0 V
2. V_{SS}/V_{GG} differential no more than 25 V.
3. Internal pull-up resistors (approx 10 K Ohm) are provided at all inputs other than Count Input, Scan Input, & Decimal Point Input.
4. V_{GG} = -12V ± 10%. Outputs open.
5. Measurement made at $V_I = V_{DD} + 0.4$ V. This condition is sufficient to represent a logic 0 and hold off or override the internal oscillators. Maximum current at V_I = +0.4V is 1.6 mA. 400 µA source current at V_{SS}-1.0 is sufficient to represent a logic 1 and hold off or override the internal oscillators.
6. I_{OL} measured at $V_O = V_{SS} - 0.75$ V. I_{OH} measured at $V_O = V_{DD} + 0.75$ V. (See MK 5002 P Application Note for output characteristics.)
7. Delay measured from the negative edge of the Scan Input.
8. Delay measured from the rising edge of the Scan Input.
9. Delay measured from the negative edge of the Count Input.

DESCRIPTION OF OPERATION

(Further information on the operation of Mostek's family of 4-digit Counter/Decoders may be found in the MK 5002 P Application Report.)

COUNTER LOGIC & TIMING

The Decade counters are *synchronously* incremented on the negative edge of the Count Input. The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{SS}.

SCAN CONTROL LOGIC & TIMING

The Digit Select Counter is incremented by a negative edge on the Scan Input. During the time the Scan Input is at O, the 7-segment and Digit Select outputs are forced off and the complement BCD outputs are forced to logic 1. (See Truth Tables.) This remains until the Scan Input returns to logic 1.

The Digit Select Counter is a one-of-four counter, scanning from MSD (Most Significant Digit) to LSD (Least Significant Digit), enabling one quad latch output at a time, and presenting a logic 1 to the corresponding Digit Select output.

The internal oscillator on this input may be overridden by an external signal source or may be allowed to oscillate at a frequency set by a single capacitor tied to this input from the V_{SS} or V_{DD} supply. In systems with considerable noise, better oscillator stability exists when the capacitor is tied to V_{SS}.

TRANSFER LOGIC & TIMING

While the Transfer input is a logic 0, data in the decade counters is transferred to the static storage latches. This input may be left at 0 for a continuous transfer-and-display mode, or may be pulsed periodically to store only on command.

Termination of a transfer command occurs internally when the input is taken to a logic 1 and the next Count Input negative edge occurs. This allows asynchronous Count and Transfer operation since the transfer is terminated prior to incrementing the counters. This means that a Count Input negative edge must follow a Transfer command before a Reset is applied to prevent transfer of invalid data. An external Reset Command must be delayed at least one Count Input negative edge following a Transfer. External transfer should terminate at least 1 μs prior to this Count negative edge and Reset should occur no sooner than 1 μs following that edge.

RESET CONTROL

The decade counters are reset to 0,000 when the Reset Input is at logic 0. The Reset Input at logic 0 also forces the Scan to the MSD output and resets the Overflow Latch output to a logic 1 (if previously latched to a logic 0). It maintains this condition as long as the logic 0 is present at the Reset Input and overrides all other associated inputs. As indicated previously, the decade counters should not be reset until a transfer has been terminated.

Since the Reset Input resets the Scan Counter to MSD the scan rate must be much faster than the reset rate to allow the lesser significant digits to be enabled. Therefore, F_{Scan}, must be much greater than four times F_{Reset}.

Ideally, the Reset pulse should also be made narrow, to prevent its duration from causing the MSD to be ON much longer than the other digits and thus appear to be brighter.

LEADING ZERO BLANKING

At the start of each MSD to LSD scan, blanking of leading zeros occurs until the first non-zero number occurs in the display or the Decimal Point Input is clocked. Any number following will be displayed. Leading zero blanking does not affect the BCD outputs or the LSD in the display which is displayed even if zero. The LSD output resets the blanking circuitry to begin blanking zeros in the next scan cycle.

The Decimal Point Input pin should be brought to logic 0 at the time the character is enabled that contains the decimal point. The first non-zero number or the Decimal Point Input signal in the scan cycle puts the blanking circuitry in the unblanking mode. If the Reset In (forces the Scan Counter to the MSD) occurs when the circuit is in the unblanked mode the first complete MSD to LSD scan will be done in the unblanked mode. This could result in a dimly displayed leading zero. A simple solution to this problem would be to force the Blanking Input low during a reset and release it only after an LSD has occurred.

Leading zero blanking may be inhibited by wiring the Decimal Point Input to ground. The MK 5007 P does not have a pin for Decimal Point Input and therefore does not have leading zero blanking.

OTHER INPUTS

The Blanking Input at logic 0 forces the 7-segment outputs to the off-state and the BCD to the equivalent of the number zero. This condition is maintained on a DC basis as long as the Blanking Input is 0. The Digit Select outputs continue to operate at the scan rate as described.

A True/Complement control inverts both BCD and 7-segment outputs when at logic 0. Depending upon the display used, combinations of the Blanking Input and True/Complement Control can be chosen to give a lamp test.

The Decimal Point Left or Right control allows the use of displays with the decimal point physically located on the left or right of the numeral. Logic 1 is decimal-point-right. In the right mode, even though the Decimal point input is clocked, unblanking is delayed until the following digit is enabled.

OUTPUTS

All output buffers on the MK 5002 family are push-pull. A negative power supply terminal, V_{GG}, is provided to increase the drive capabilities of these output buffers. Since the V_{GG} supply is connected only to these output buffers, it has no effect on any other device characteristics.

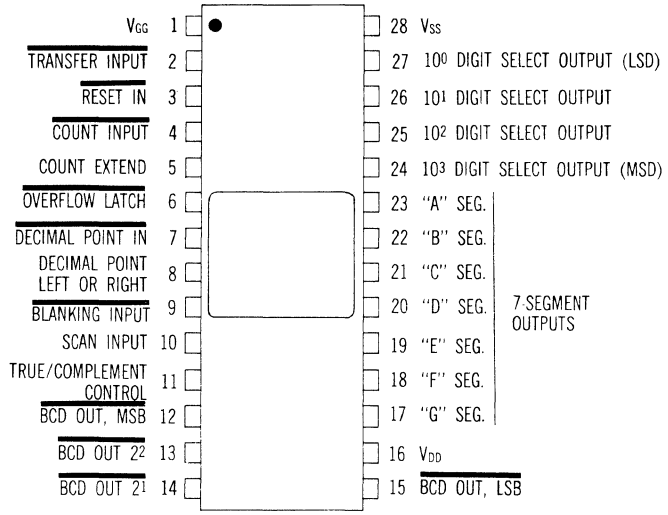
Output characteristics are covered in the MK 5002 Application Report which illustrates the effects of V_{GG} with current to be expected at various output voltages.

The outputs are designed to drive directly to the base of common-emitter transistors, so that output voltage is clamped or maintained at a potential where the MK 5002 P is able to sink or source its greater amount of current.

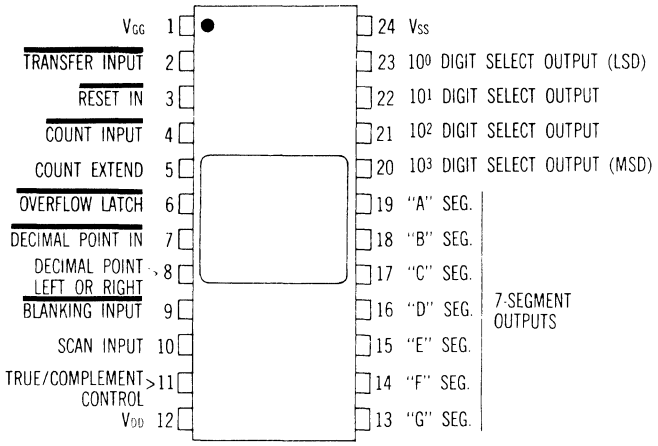
PIN CONNECTIONS

The MK 5002/5/7P is available in a 28-pin dual-in-line package, a 24-pin dual-in-line package, and a 16-pin dual-in-line package. Only the 28-pin package contains all available functions.

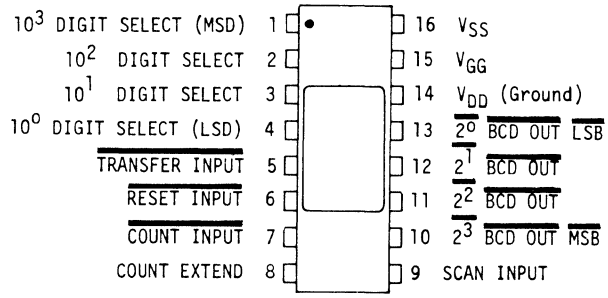
MK 5002 P



MK 5005 P



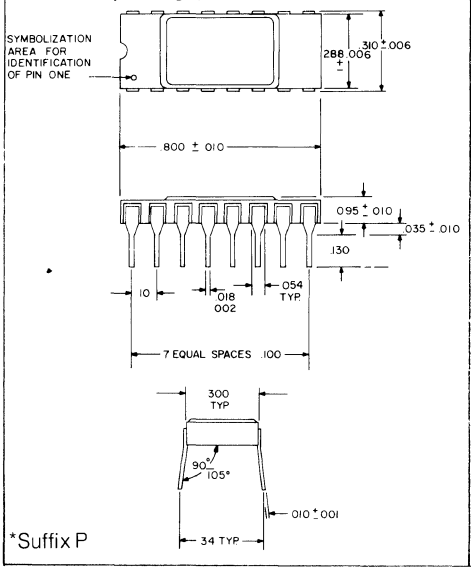
MK 5007 P



Special Products

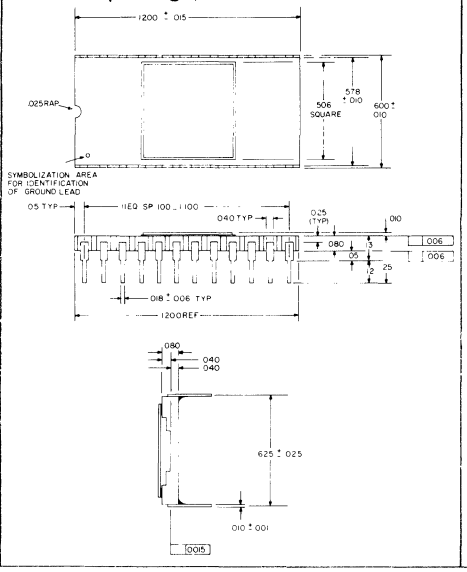
PHYSICAL DESCRIPTIONS

(16-lead ceramic dual-in-line hermetic package)*

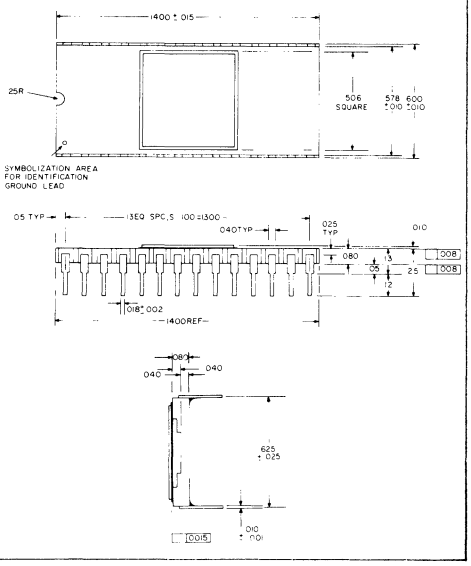


*Suffix P

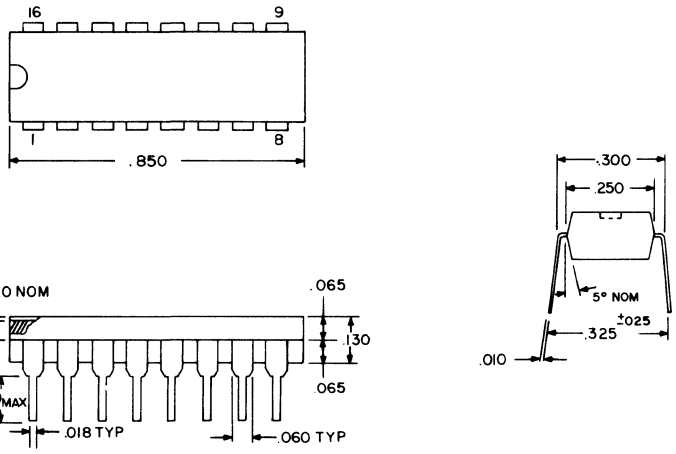
(24 lead ceramic dual-in-line hermetic package)*



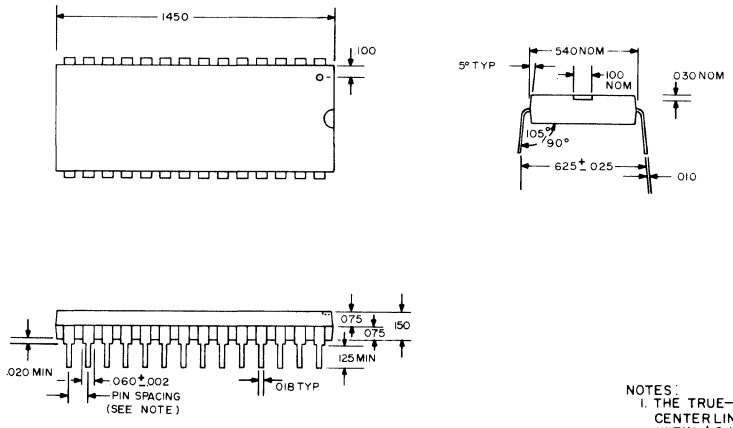
(28 lead ceramic dual-in-line hermetic package)*



PACKAGE 16-pin plastic dual-in-line *



PACKAGE 28-pin plastic dual-in-line *



NOTES:
1. THE TRUE-POSITION PIN SPACING IS 0.100 BETWEEN CENTERLINES. EACH PIN CENTERLINE IS LOCATED WITIN ±0.100 OF ITS TRUE LONGITUDINAL POSITION RELATIVE TO PINS 1 AND 28.

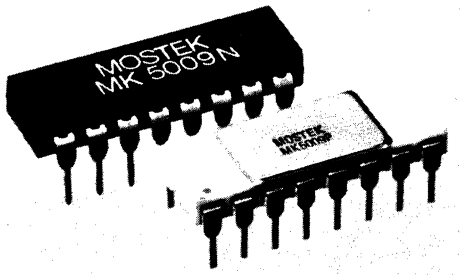
*Suffix N

MK 5009 P
MK 5009 N

MOS Counter Time-Base Circuit

MOSTEK

- Ion-implanted for full TTL/DTL compatibility
- Internal clock operates from:
  - External signal
  - External RC network
  - External crystal
- Operates DC to above 1 MHz
- Binary-encoded for frequency selection



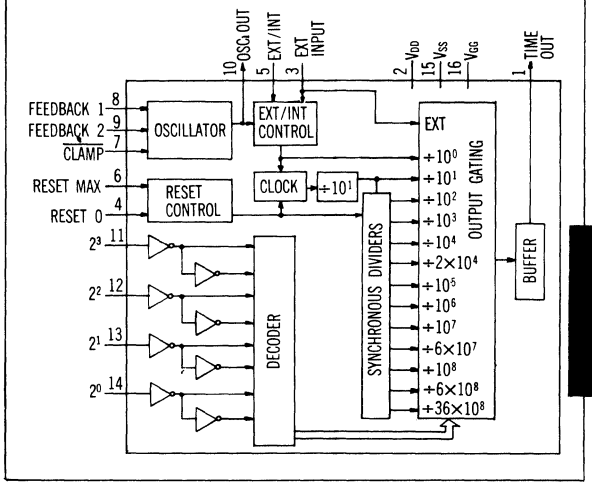
DESCRIPTION

The MK 5009 P is a highly versatile MOS oscillator and divider chain manufactured by Mostek using its depletion-load, ion-implantation process and P.-channel technology. The 16-pin DIP package provides frequency division ranges from 1 to 36×10^8. The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination; the internal oscillator with an external crystal; or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instruments, timers, and clocks.

With an input frequency of 1 MHz, the MK 5009 P provides the basic time periods necessary for most frequency measuring instruments, i.e., 1 μs through 100 seconds. One-minute, ten-minute, and one-hour periods are also available using a 1 MHz input. Using a 1/1.2 MHz input, the MK 5009 P can also provide a 50/60 Hz output for accurate generation of line frequencies in portable instruments or clocks.

The time-base output (TIME OUT) is a square wave, its frequency determined by the selected counter division, and by the oscillator frequency or external input. The falling edge of the output square wave should be used to control external gating circuitry.

FUNCTIONAL DIAGRAM



Special Products

TIME OUT

ADDRESS INPUTS				WITHOUT RESET	RESET		BYPASS MODES (see page 3)		
					Reset Max.	Reset Min.	Mode 1	Mode 2	Mode 3
				R_{MAX} = 0	R_{MAX} = 1	R_{MAX} = 0	R_{MAX} = V_{GG}	R_{MAX} = 0	R_{MAX} = V_{GG}
2^3	2^2	2^1	2^0	R_O = 0	R_O = 0	R_O = 1	R_O = 0	R_O = V_{GG}	R_O = V_{GG}
0	0	0	0	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$
0	0	0	1	$\div 10^1$			$\div 10^1$	$\div 10^1$	$\div 10^1$
0	0	1	0	$\div 10^2$	Resets	Resets	$\div 10^2$	$\div 10^2$	$\div 10^2$
0	0	1	1	$\div 10^3$			$\div 10^3$	$\div 10^3$	$\div 10^3$
0	1	0	0	$\div 10^4$	Counters	Counters	$\div 10^4$	$\div 10^4$	$\div 10^4$
0	1	0	1	$\div 10^5$			$\div 10^2$	$\div 10^5$	$\div 10^2$
0	1	1	0	$\div 10^6$	to their	to their	$\div 10^3$	$\div 10^6$	$\div 10^3$
0	1	1	1	$\div 10^7$			$\div 10^4$	$\div 10^7$	$\div 10^4$
1	0	0	0	$\div 10^8$	Highest	Lowest	$\div 10^5$	$\div 10^5$	$\div 10^2$
1	0	0	1	$\div 6 \times 10^7$			$\div 6 \times 10^4$	$\div 6 \times 10^4$	$\div 6 \times 10^1$
1	0	1	0	$\div 36 \times 10^8$	States	States	$\div 36 \times 10^5$	$\div 36 \times 10^5$	$\div 36 \times 10^2$
1	0	1	1	$\div 6 \times 10^8$			$\div 6 \times 10^5$	$\div 6 \times 10^5$	$\div 6 \times 10^2$
	*			—			—	—	—
1	1	1	0	$\div 2 \times 10^4$			$\div 2 \times 10^1$	$\div 2 \times 10^1$	$\div 2 \times 10^1$
1	1	1	1	Ext. In.	Ext. In.	Ext. In.	Ext. Int.	Ext. Int.	Ext. Int.

*Addresses 1100 and 1101 result in Logic 0 at the output regardless of the state of the Reset Max. and Reset 0 inputs.

Logic 1 = High = V_{SS}

Logic 0 = Low = V_{DD}

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} . . . . . + 0.3V to − 20V
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Storage Temperature Range (Ambient) . . . . . − 55°C to + 150°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{SS}	Supply Voltage	+ 4.5		+ 5.5	V	
V_{DD}	Supply Voltage	0.0		0.0	V	
V_{GG}	Supply Voltage	− 9.6		− 14.4	V	
f_{XTAL}	Crystal Frequency	0.1		2.0	MHz	
f_{RC}	RC Frequency	DC		200	kHz	
f_{EXT}	External Frequency	DC		2.0	MHz	
t_{PL}	Logic 0 Pulse Width, $\overline{CLAMP}$	—				Note 5
	Ext. Input	200			nsec	
t_{PH}	Logic 1 Pulse Width, Ext. Input	200			nsec	
	Reset Max	10.0			μsec	
	Reset 0	10.0			μsec	
R	Feedback Resistance	.01		2.5	MΩ	Fig. 1
V_{IL}	Input Voltage, Logic 0, Reset Inputs	0.0		0.8	V	
	Reset (Bypass Mode)	V_{GG}		V_{GG} + 1.0	V	Note 2
	All Other Logic Inputs			0.8	V	
V_{IH}	Input Voltage, Logic 1, All Logic Inputs	V_{SS}-1.0	V_{SS}	V_{SS} + 0.3	V	

Special Products

ELECTRICAL CHARACTERISTICS

($V_{SS} = +5V \pm 10\%$; $V_{DD} = 0V$; $V_{GG} = -12.0V \pm 20\%$; $0°C \leq T_A \leq 70°C$)

	PARAMETER	MIN	TYP†	MAX	UNITS	NOTES
I_{SS}	Supply Current, V_{SS}		6.0	11.0	mA	Note 1
I_{GG}	Supply Current, V_{GG}		6.0	11.0	mA	
I_{IL}	Input Current, Logic 0			− 1.6	mA	Note 2; $V_I = 0.4V$
V_{OL}	Output Voltage, Logic 0			0.4	V	$I_{OL} = 1.6mA$*
V_{OH}	Output Voltage, Logic 1	2.4			V	$I_{OH} = -40\mu A$*
f_{STA}	Frequency Stability w/ Volt. Change, RC Mode		± 3.0		%/V	Note 3
	/ Temp. Change, RC Mode		− 0.2		%/°C	
	Crystal Mode		—			Note 4
t_{e-e}	Jitter, Edge-to-Edge Variation		<15		nsec	Temp. & Supply Voltage Constant

†Typical values at $V_{SS} = +5V$, $V_{DD} = 0V$, $V_{GG} = -12V$, and $T_A = 25°C$

1. Logic inputs at V_{SS}, output open circuited. Each logic input (see Note 2) contributes an additional 1.6 mA (max.) to I_{SS} when at logic 0.
2. Logic Inputs are: Reset Max; Reset 0; Address Inputs; Ext. Input; Ext/Int Select; and $\overline{Clamp}$.
3. Frequency variations due to power supply changes only.
4. Crystal mode stability is dependent upon crystal.
5. Minimum logic 0 time at clamp input is 50% of oscillator period.

*V_{OH}, V_{OL} apply only to Time Out.

DESCRIPTION OF OPERATION

The MK 5009 P consists basically of a series of counters, selectable via an internal multiplexer. The $\div 10^1$ counter output is used to generate an internal clock signal for the 10^2 through 36×10^8 counter stages, which are fully synchronous with each other.

OSCILLATOR CONTROLS

Operation in the RC oscillator mode is achieved as shown in Figure 1. Frequency, f, is approximately 0.8/RC. The clamp circuit can be used in the RC mode to provide one-shot or accurate start-up operations. When Clamp goes to a logic 0, the internal circuitry is held at a reference level so that upon release of the Clamp (return to logic 1), the oscillator's first cycle will be a full cycle.

The crystal oscillator mode is shown in Figure 2. Values for the resistors are chosen to bias the internal circuitry for optimum performance. The two capacitors are chosen to provide the loading capacitance (C_L) specified for the selected crystal. It is recommended that C1 = C2 = 2 C_L.

RESET/BYPASS CONTROLS

The MK 5009 P provides two different reset conditions. A positive-going pulse of 10 μs or longer on Reset 0 will reset counters to their lowest state, while a positive-going pulse at Reset Max will reset counters to their highest state. The Reset Max control enables the user to set up the counters to provide a falling edge at the next oscillator cycle or negative-going external input, regardless of which divider chain is selected.

In addition, taking one or both Reset Inputs to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes (see table on page 1).

EXTERNAL/INTERNAL FREQUENCY SOURCE

When using an external signal source to operate the MK 5009 P, that signal should be applied at the External Input (Pin 3), and the External/Internal Select (Pin 5) should be brought to logic 1.

For operation with an internal signal, the External/Internal Select should be at logic 0.

OSCILLATOR OUTPUT

The oscillator output, provided at Pin 10, is not a true logic output, but may be used to drive a high impedance device such as a junction FET or other MOS circuitry.

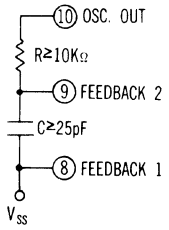


FIG. 1

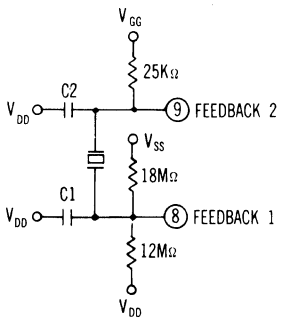
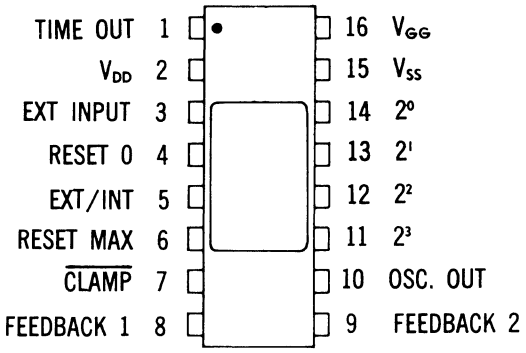
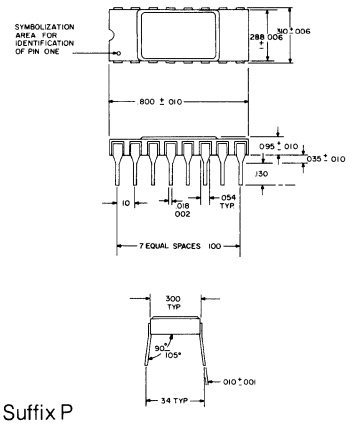


FIG. 2

PIN CONNECTIONS

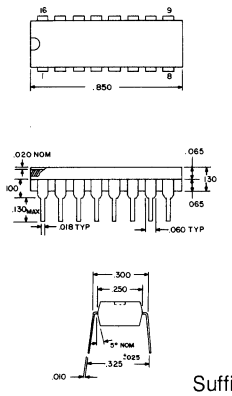


PACKAGE
16-pin ceramic dual-in-line



Suffix P

PACKAGE
16-pin plastic dual-in-line



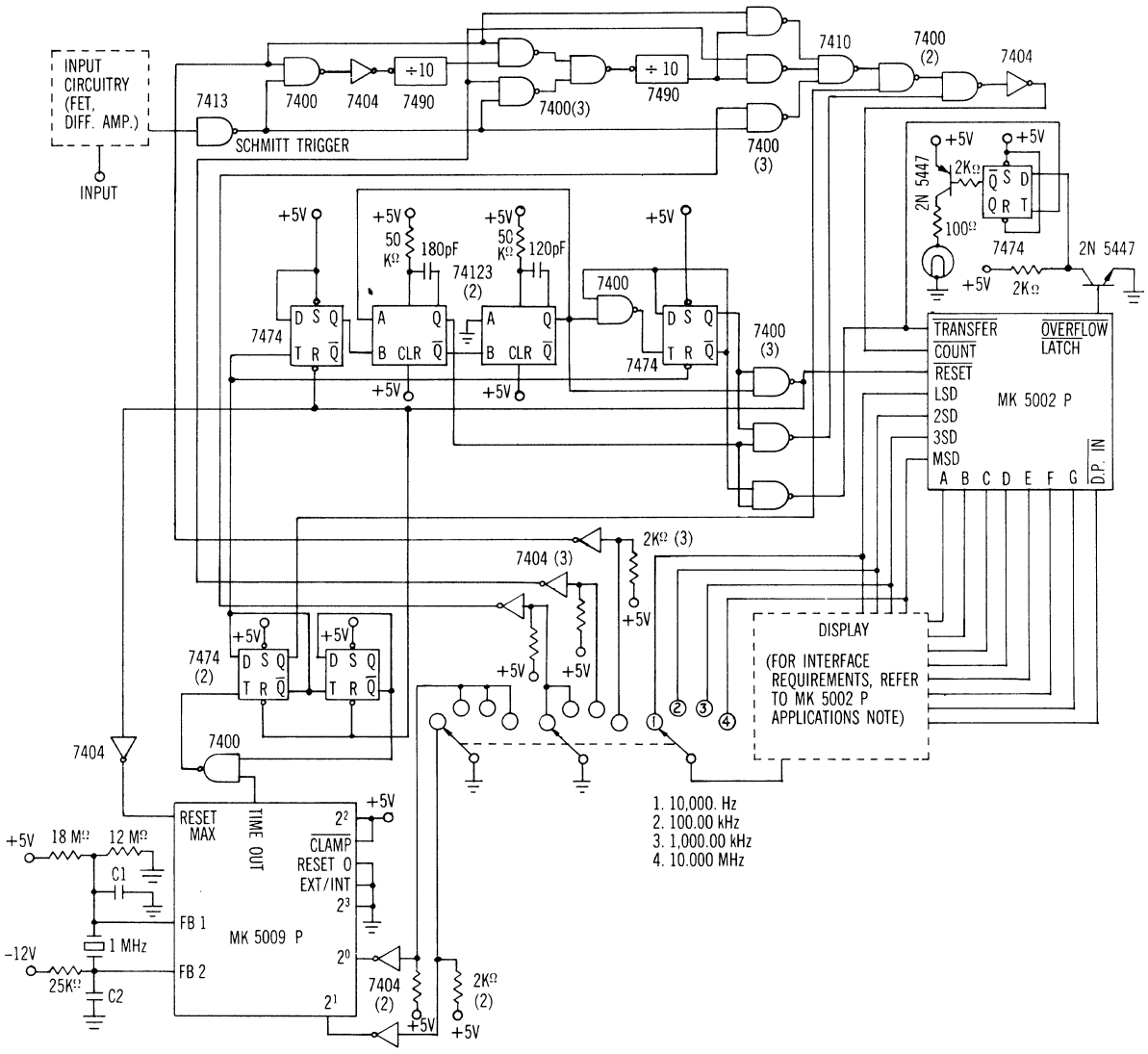
Suffix N

Special Products

APPLICATION — 10 MHz Frequency Counter

The circuit shown below is a frequency counter capable of counting input rates up to 10 MHz, selected in four ranges. The MK 5009 P provides the time base intervals while the Mostek MK 5002 P counter circuit provides counting, storage, and display functions. Two decades of prescaling using TTL are employed. TTL one-shots provide proper timing for the 5002.

To replace the functions of the MK 5009 P, an active device and Schmitt trigger for the crystal oscillator would be needed, plus six 7490's to achieve the correct time out. Replacing the functions of the MK 5002 would require four 7490's, four 7475's, and four BCD-to-seven-segment decoders.



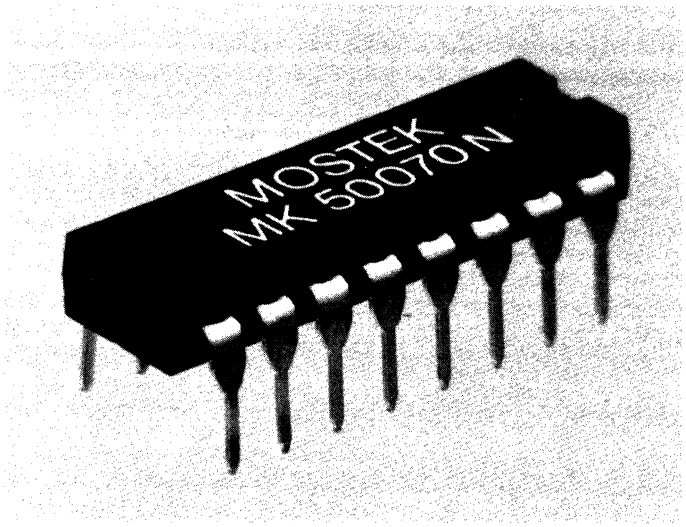
MK 50070 N

CMOS Oscillator and Divider

MOSTEK

FEATURES:

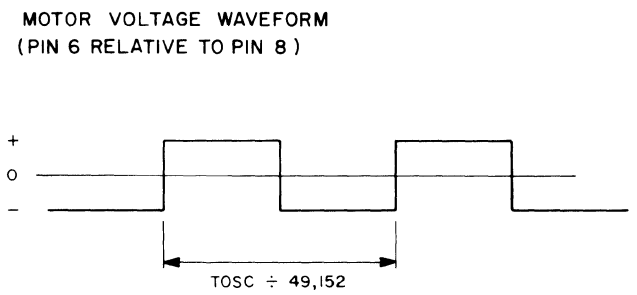
- Low Power Dissipation
- 4-18 Volt Operating Range
- Internal Zener Regulation
- Internal Oscillator



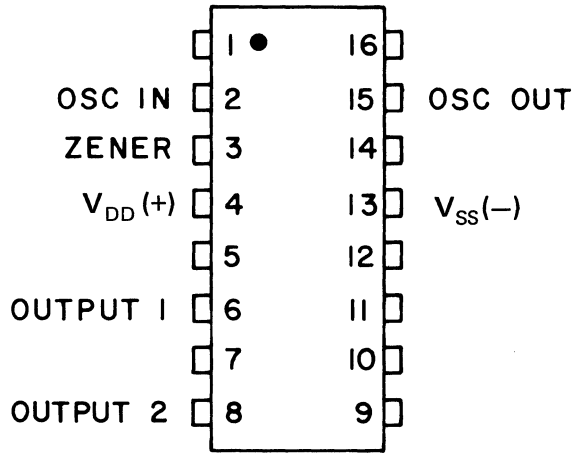
DESCRIPTION:

The MOSTEK 50070 circuit is an oscillator and divider circuit for specialized applications. An external quartz crystal determines the oscillator frequency and the chip divides this frequency by 49152. The output is buffered by a 4 transistor bridge.

MOTOR VOLTAGE WAVEFORM

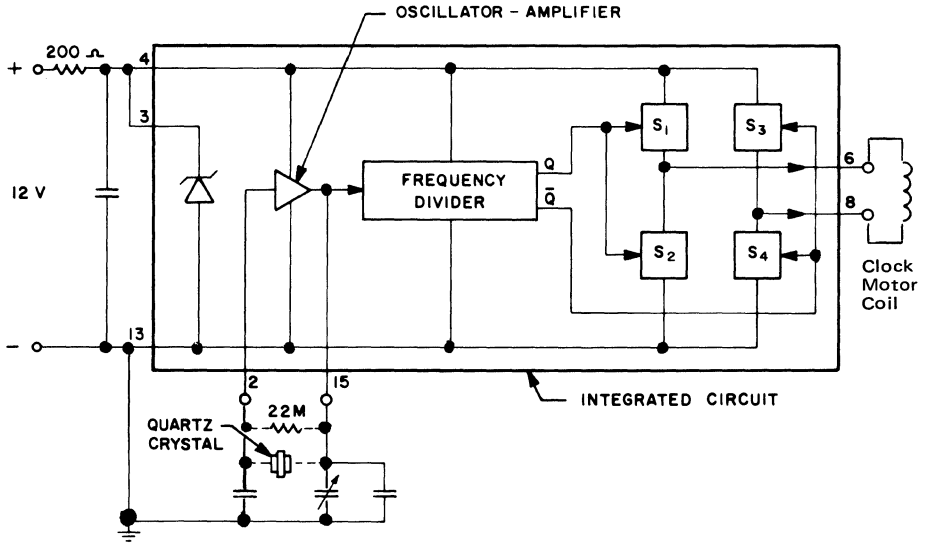


PIN CONNECTIONS



Special Products

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS OVER FREE-AIR TEMPERATURE RANGE

Voltage on Any Pin Relative to V_{SS} . . . . . +22V

Operating Free-Air Temperature Range . . . . . 0°C to 70°C

Storage Temperature Range . . . . . −40°C to +100°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$)

PARAMETER	MIN	MAX	UNITS	NOTES
Operating Voltage with 200 Ω resistor	+4	+18	Volts	1
Maximum non-recurring Transient	−75	+110	Volts	2

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$)

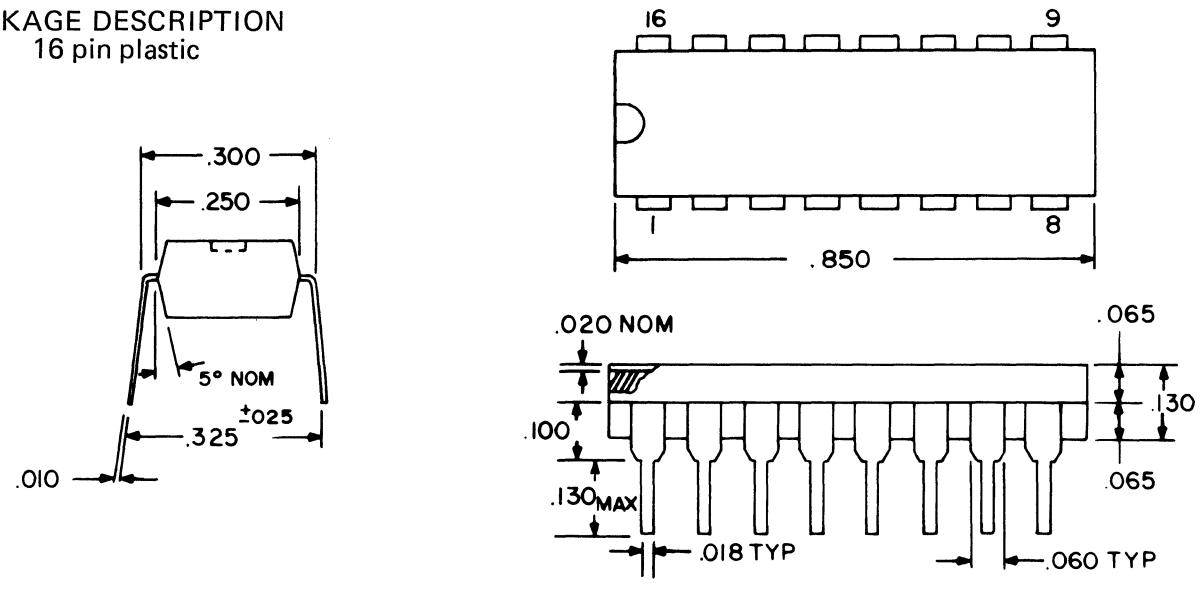
PARAMETER	MIN	MAX	UNITS	NOTES
Zener Voltage at I_Z = 100 μA	10	14	Volts	
Power Drain		30	mW	3
Total driver Voltage Drop S_1 and S_4 or S_2 and S_3		1	Volt	4
Maximum Frequency		3.145728	MHz	

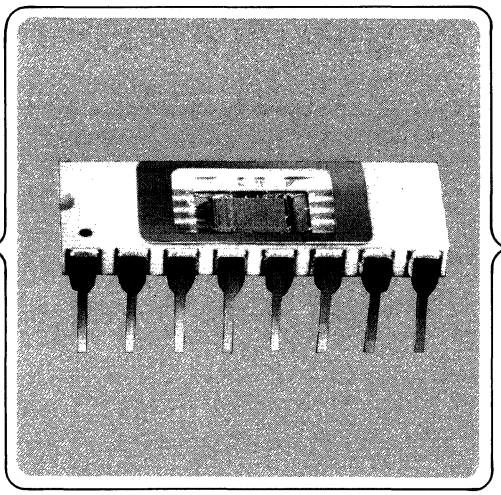
Special Products

NOTES:

1. Pin 3 tied to Pin 4.
2. Time Constant Equals 45 milliseconds
3. With no load and $V_{DD} - V_{SS}$ = 10 volts
4. $V_{DD} - V_{SS}$ = 4V, I_L = 2mA

PACKAGE DESCRIPTION
16 pin plastic





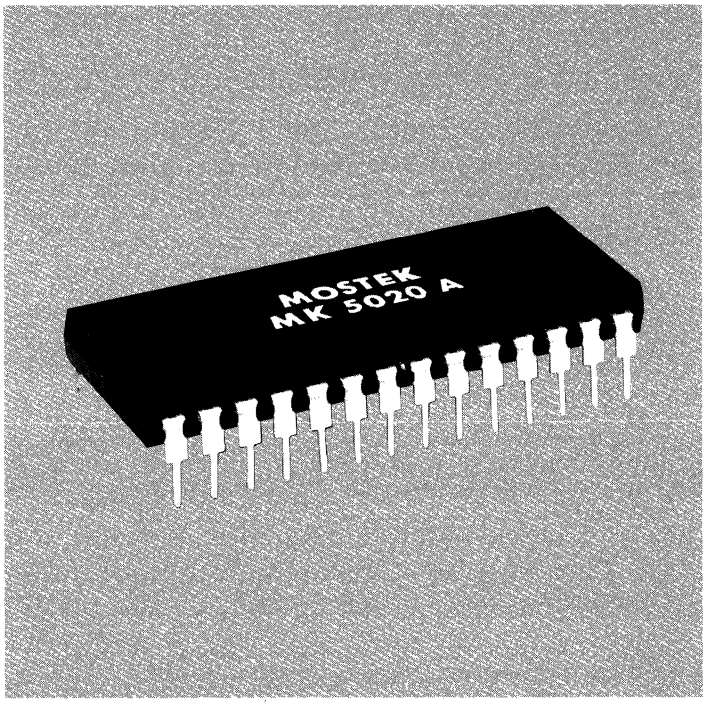
Consumer

MOS Calculator Series

MOSTEK

FEATURES:

- ☐ Direct Segment Drive for LED's
- ☐ Low Power Consumption
- ☐ Single Power Supply Voltage
- ☐ Internal Encoding of Keyboard Inputs
- ☐ Internal Debouncing of Keyboard Inputs
- ☐ Single 28-pin, Dual-in-line Package
- ☐ ROM controlled

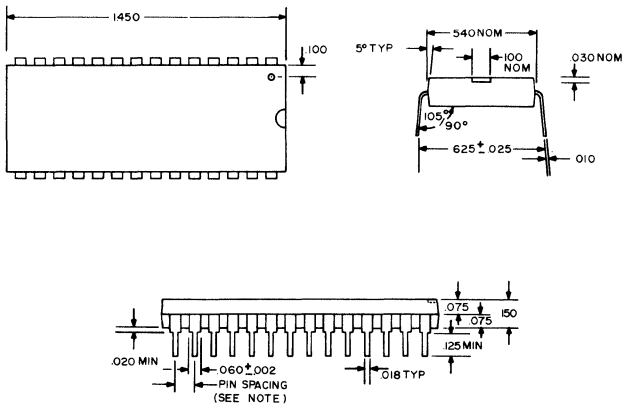


STANDARD PRODUCTS:

☐ MK 5020 A	8-digit, six-function (+, −, X, ÷, %, √) with constant
☐ MK 5021 C	10-digit, six-function (+, −, X, ÷, %, √) with constant
☐ MK 5022 A	8-digit, five-function (+, −, X, ÷, %) with constant fully independent memory, and store/recall memory.
☐ MK 50203	8-digit, five-function (+, −, X, ÷, %) with constant, fully independent memory, reciprocal, and constant register exchange

Consumer

PACKAGE 28-pin dual-in-line plastic



NOTES:
1. THE TRUE-POSITION PIN SPACING IS 0.100 BETWEEN CENTERLINES EACH PIN CENTERLINE IS LOCATED WITIN ±0.100 OF ITS TRUE LONGITUDINAL POSITION RELATIVE TO PINS 1 AND 28.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE

(All voltages relative to V_{SS})

Supply Voltage Range V_{GG} ..... +0.3V to −20V

Input Voltage Range ..... +0.3V to −20V

Output Voltage Breakdown SA-SG ..... +0.3V to −7V

DI-DII ..... +0.3V to −17V

Operating Free-Air Temperature Range ..... 0°C to +55°C

Storage Temperature Range ..... −40 °C to + 100°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 55°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{GG}	Supply Voltage	−12	−14.5	−17	volts	1
V_{IH}	Input Voltage, Logic 1	V_{SS} −1.2			volts	2, 8
V_{IL}	Input Voltage, Logic 0	V_{GG}		V_{SS} −5	volts	2
ϕ	Clock Period	5.5		11	μsec	3

ELECTRICAL CHARACTERISTICS ($12 \leq V \leq 17$; $0°C \leq T_A \leq 55°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{GG}	Supply Current		6		mA	
I_I	Input Current @ V_{IN} V_{SS}		150	300	μA	2
$R_{ON(SEG)}$	Segment Output "On" Resistance		300	750	Ω	4, 7
$R_{ON(DIG)}$	Digit Output "On" Resistance		250	600	Ω	4, 8
$I_{OL(SEG)}$	Segment Output Leakage Current		.1	10	μA	5, 9
$I_{OL(DIG)}$	Digit Output Leakage Current		.1	10	μA	6, 9

Notes:

(1) This parameter is relative to V_{SS}.

(2) This parameter applies to the KN, KO, KP, and KQ inputs.

(3) The maximum clock period is related to the worst-case keyboard entry time. 11 μsec corresponds to approximately 44 msec "key down" time. Any increases in the clock period will affect this entry time proportionately.

(4) Voltage across the output (relative to V_{SS}) is 0 volts to 1.5 volts.

(5) Voltage across the output (relative to V_{SS}) is 0 volts to 7 volts.

(6) Voltage across the output (relative to V_{SS}) is 0 volts to 17 volts.

(7) Segment output current must be limited to less than 7 mA per output.

(8) Because digit output voltages are used in scanning keyboard inputs, external circuitry (e.g., a display driver) must require less than 2 mA from each digit output in order that the minimum value of V_{IH} can be satisfied in all applications.

(9) Segment and digit outputs are open drain transistors.

Consume

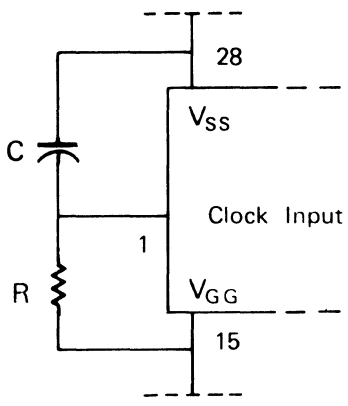
INTERNAL CLOCK OSCILLATOR

R = 390 K 10%

C = 22 pF 5%

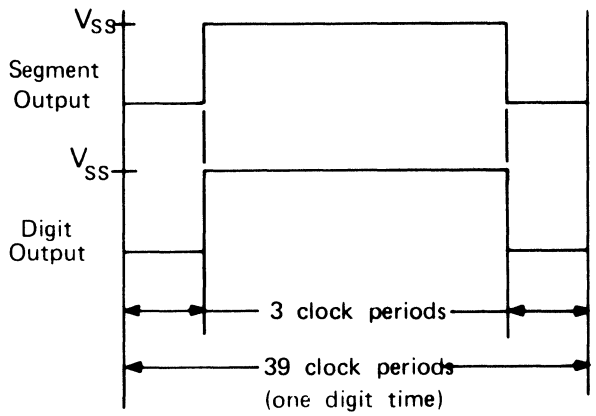
for nominal

140 KHz clock



The oscillator waveforms appears as a "sawtooth" voltage variation swinging between V_{SS} and V_{GG} /2.

SEGMENT AND DIGIT TIMING AND POLARITY



Note: Segment and digit outputs are turned on to V_{SS} for a displayed segment.

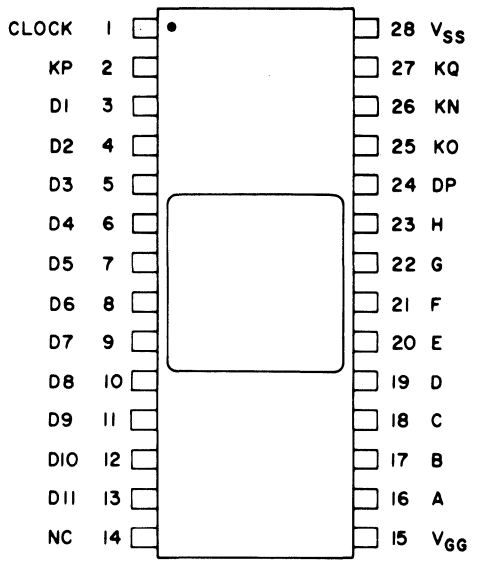
MK 5020AN

DESCRIPTION

The MK 5020 A is a six-function (+, −, X, ÷, %, √) 8-digit calculator, featuring selectable constant, floating or fixed decimal point (selectable to eight positions), selectable roundoff, algebraic or business entry, credit balance, chain calculations, leading zero suppression, and internal debouncing and encoding of keyboard inputs.

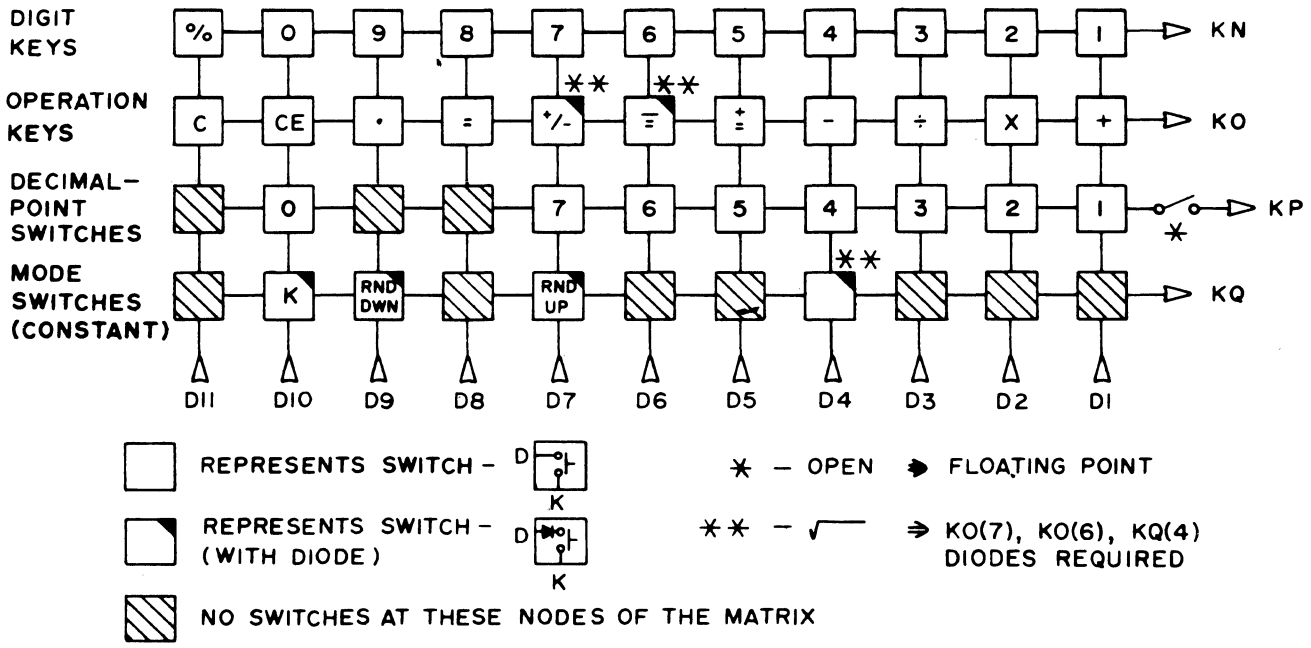
Low power dissipation, broad supply voltage range, a single power supply, and an internal clock oscillator makes the MK 5020 A ideal for battery-operated, hand-held calculators with lower system costs.

PIN CONNECTION

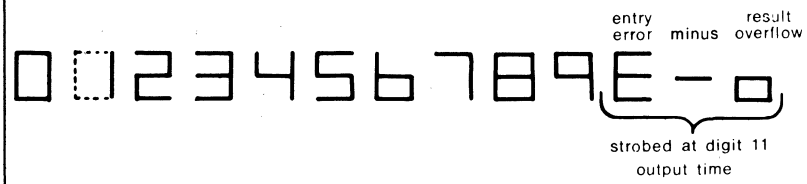


NC = NO CONNECTION

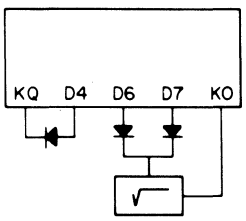
KEY MATRIX



DISPLAY FONT

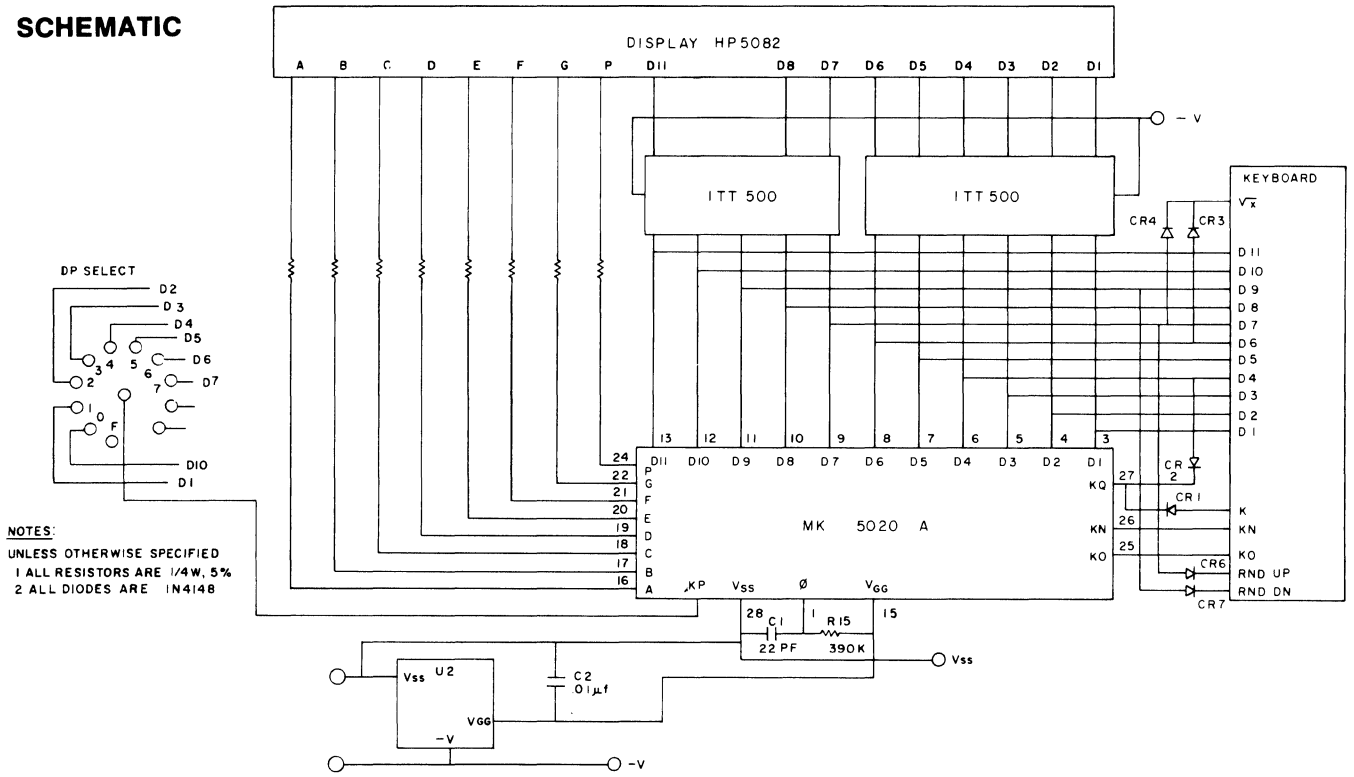


CONNECTIONS FOR SQUARE ROOT KEY



Consumer

SCHEMATIC



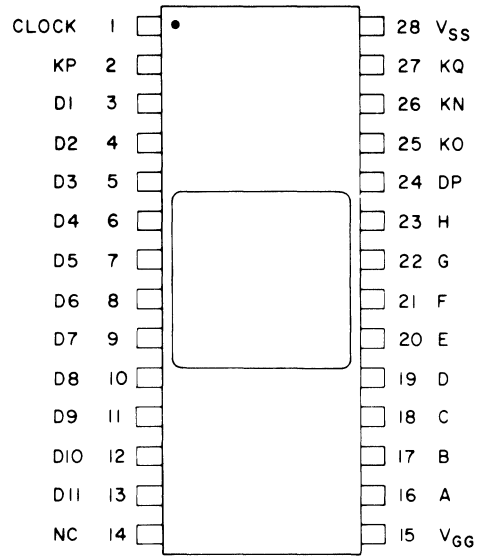
PROBLEM	FIXED POINT OR FLOATING	CONSTANT	KEY ENTRIES	REMARKS	DISPLAY
PERCENT KEY					
Find 15% of 200	Floating	*	C		0.
			15		15.
			%		0.15
			X		0.15
			200		200.
			=		30.
Find 15% of 200	Floating	*	C		0.
			200		200.
			X		200.
			15		15.
			%		30.
Find 15% mark up on $200 and total	Floating	*	C		0.
			200		200.
			+		200.
			15		15.
			%	This gives the mark up	30.
			=	This gives the total	230.
Find 22% discount and selling price on $526	Floating	*	C		0.
			526		526.
			-		526.
			22		22.
			%	This is the discount	115.72
			=	This is the selling price	410.28
CONSTANT PERCENT					
Find 15% of: 200, 450, 372	Floating	on	C		0.
			15		15.
			%		0.15
			X		0.15
			200		200.
			=		30.
			450		450.
			=		67.5
			372		372.
			=		55.8

MK 5021CN

The MK 5021 C is a six-function (+, −, X, ÷, %, √) 10-digit calculator featuring selectable constant, floating decimal point (selectable to ten positions), floating negative sign, algebraic or business entry, credit balance, chain calculations, display blanking during claculations, leading zero suppression, and internal debouncing and encoding of keyboard inputs.

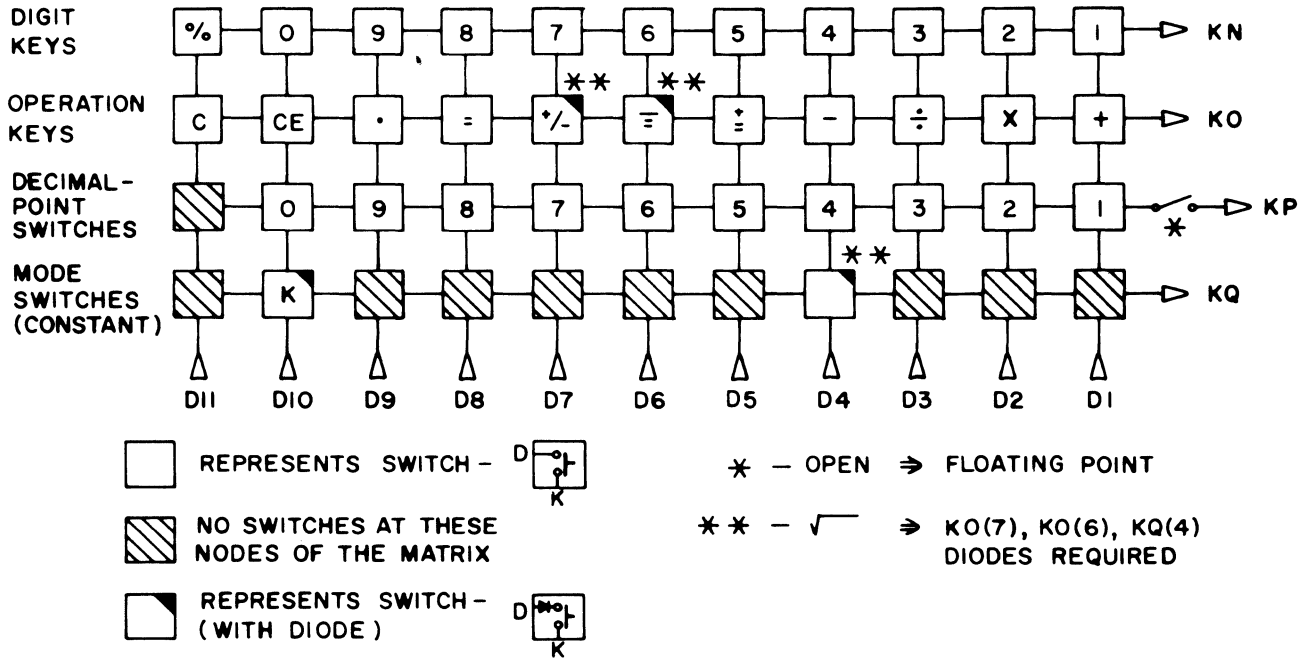
Low power dissipation, broad supply voltage range, a single power supply, and an internal clock oscillator make the MK 5021 C ideal for battery-operated, hand-held calculators with lower system costs.

PIN CONNECTION

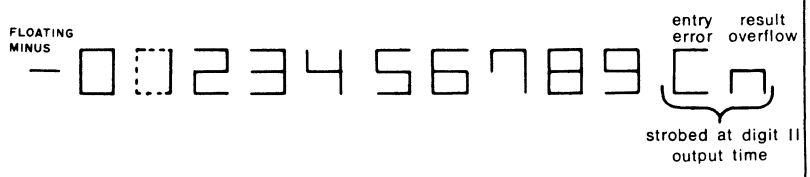


NC = NO CONNECTION

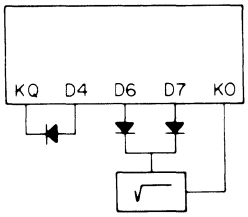
KEY MATRIX



DISPLAY FONT

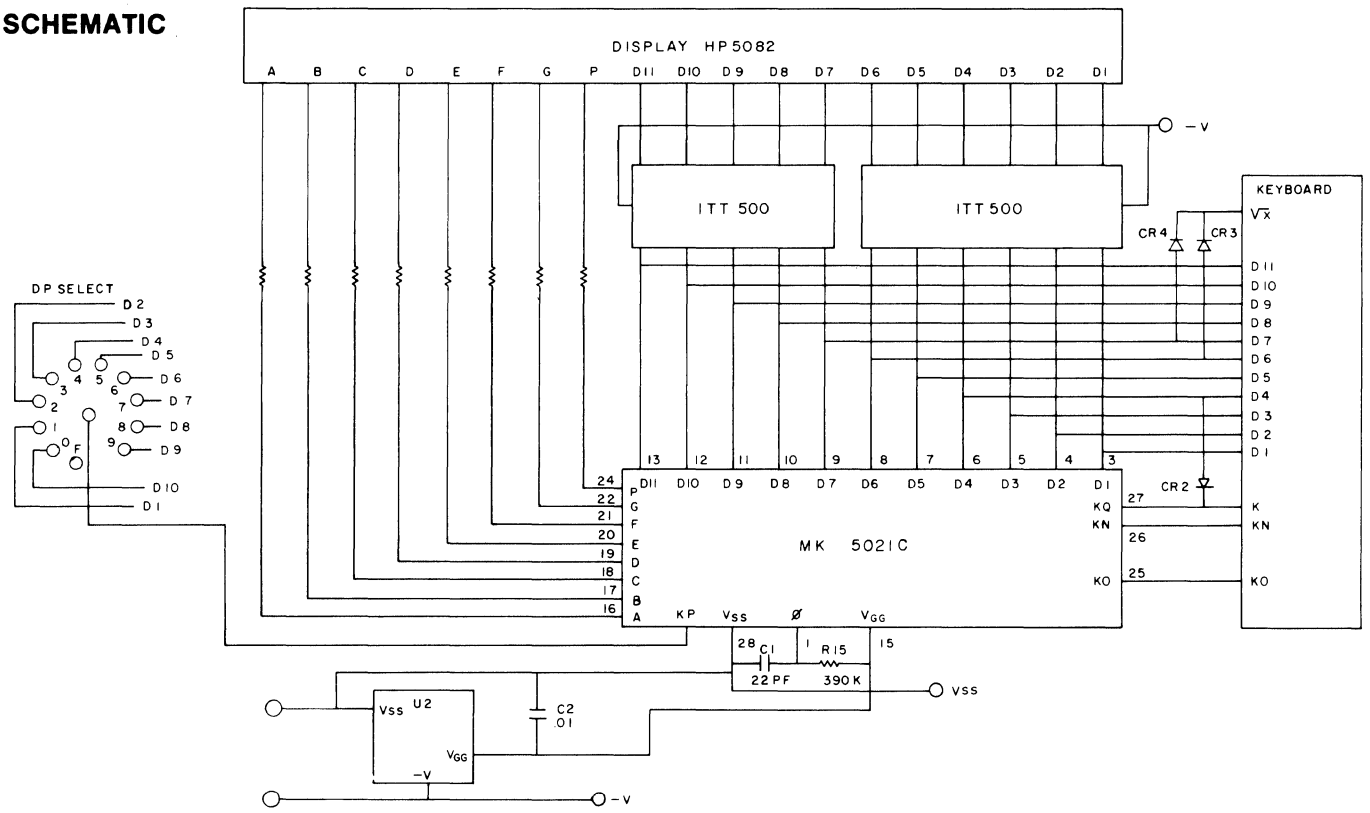


CONNECTIONS FOR SQUARE ROOT KEY



Consumer

SCHEMATIC



PROBLEM	FIXED POINT OR FLOATING	CONSTANT	KEY ENTRIES	REMARKS	DISPLAY
PERCENT KEY					
Find 15% of 527	Floating	*	C		0.
			15		15.
			%		0.15
			X		0.15
			527		527.
			±		79.05
Find 15% of 527	Floating	*	C		0.
			527		527.
			X		527.
			15		15.
			%		79.05
Find 12.5% mark up and selling price on $450 item	Floating	*	C		0.
			450		450.
			X		450.
			12.5		12.5
			%	This is the mark up	56.25
			±	This is the selling price	506.25
Find 8.3% discount and selling price on $200 item	Floating	*	C		0.
			200		200.
			X		200.
			8.3		8.3
			%	This is the discount	16.6
			±	This is the selling price	183.4
CONSTANT PERCENT					
Find 15% of: 200, 450, 372	Floating	on	C		0.
			15		15.
			%		0.15
			X		0.15
			200		200.
			=		30.
			450		450.
			=		67.5
			372		372.
			=		55.8

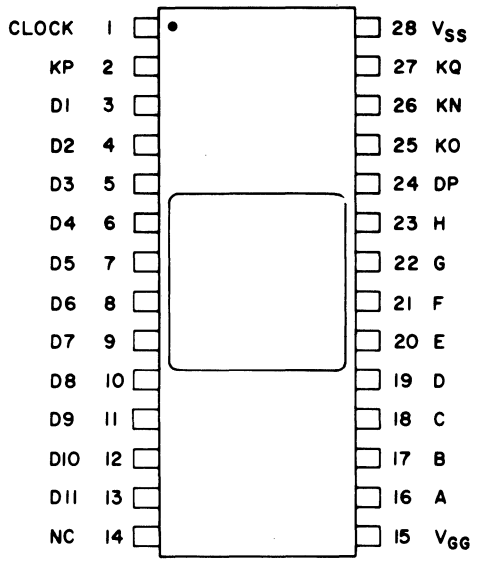
MK 5022AN

DESCRIPTION

The MK 5022 A is a five-function (+, −, X, ÷, %), 8-digit calculator with fully independent memory. Only 20 keys are required to implement the five functions with memory, resulting in a unit which is compact, economical, and simple to operate. Additional features are automatic constant, floating negative sign, algebraic entry, floating decimal point, chain calculations, credit balance, leading zero suppression, display blanking during calculations, and internal debouncing and encoding of keyboard inputs.

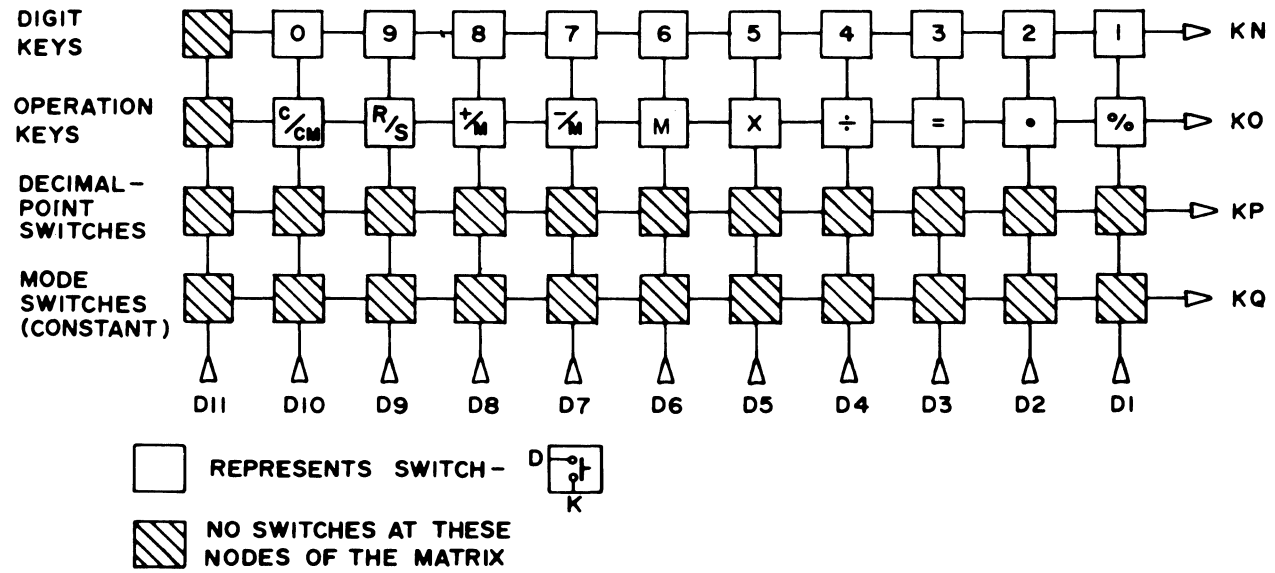
Low power dissipation, broad supply voltage range, a single power supply, and an internal clock oscillator make the MK 5022 A ideal for battery-operated handheld calculators with lower system costs.

PIN CONNECTION



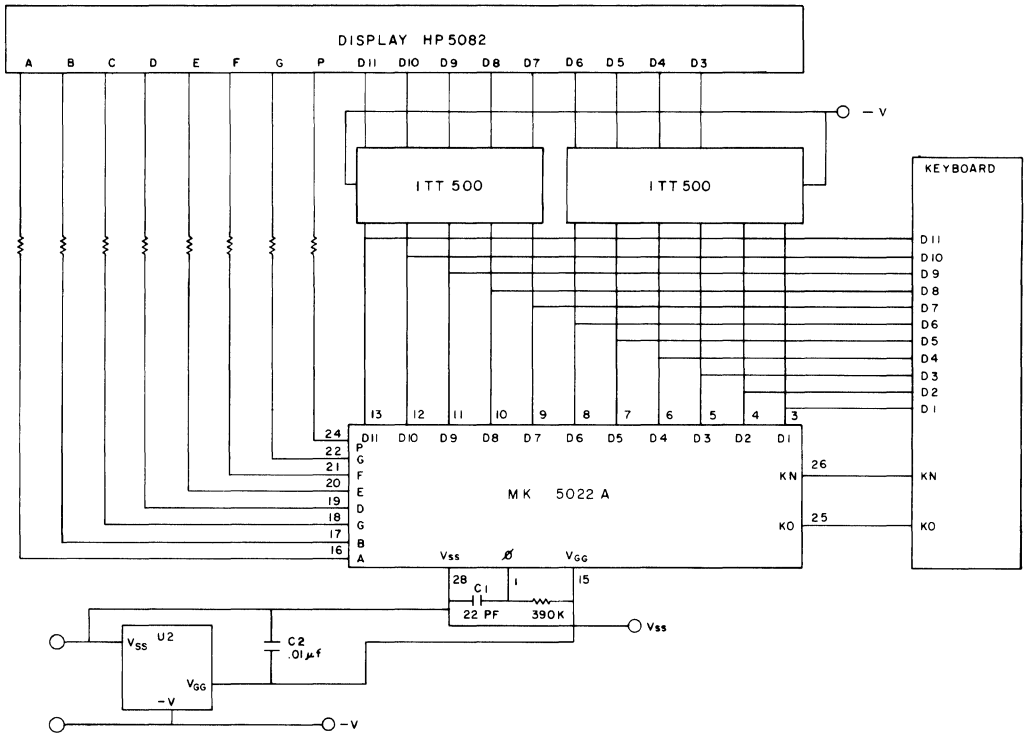
NC = NO CONNECTION

KEY MATRIX



DISPLAY FONT

SCHEMATIC



PROBLEM	KEY ENTRIES	REMARKS	DISPLAY
MEMORY ADD	M C	Clears Memory	
+27.84	C	Clears display	0.
+56.352	27.84		27.84
	M		27.84
	+	Memory in use indicator	L 27.84
	56.352		L 56.352
	M +	adds display to memory	L 56.352 L 56.352
	R/S	recals total	L 84.192
MEMORY SUBTRACT	M C	clears memory	84.192
+27.20	C	clears display	0.
-56.35	27.20		27.20
	M +	adds display to memory	27.20 L 27.20
	56.35		L 56.35
	M –	subtracts display from memory	L 56.35 L 56.35
	R/S	recalls difference memory has credit balance	L -29.15
MEMORY STORE	M C	Scratchpad	 -29.15
	C		0.
9/4, 9/5, 9/6, 9X4	9	constant dividend	9.
	M	stores	9.
	R/S	in memory	L 9.
	÷		L 9.
	4	division # 1	L 4.
	=	quotient # 1	L 2.25
MEMORY RECALL	R/S	recalls memory	L 9.
	÷		L 9.
	5	divisor # 2	L 5.
	=	quotient # 2	L 1.8
	R/S	recalls memory	L 9.
	÷		L 9.
	6	divisor # 3	L 6.
	=	quotient # 3	L 1.5
	R/S		L 9.
	X		L 9.
	4	multiplier	L 4.
	=	product	L 36.

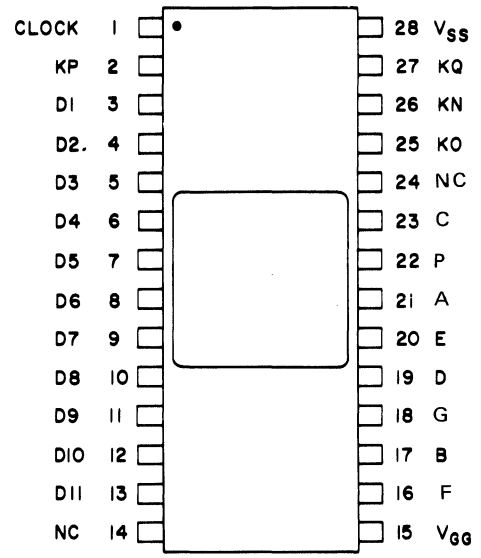
MK 50203 N

DESCRIPTION

The MK 50203 is a six-function (+, –, X, ÷, %, 1/X), 8-digit calculator with fully independent memory. Additional features are automatic constant, repeat add, exchange, floating negative sign, algebraic entry, floating decimal point, chain calculations, credit balance, leading zero suppression, display blanking during calculations, and internal debouncing and encoding of keyboard inputs.

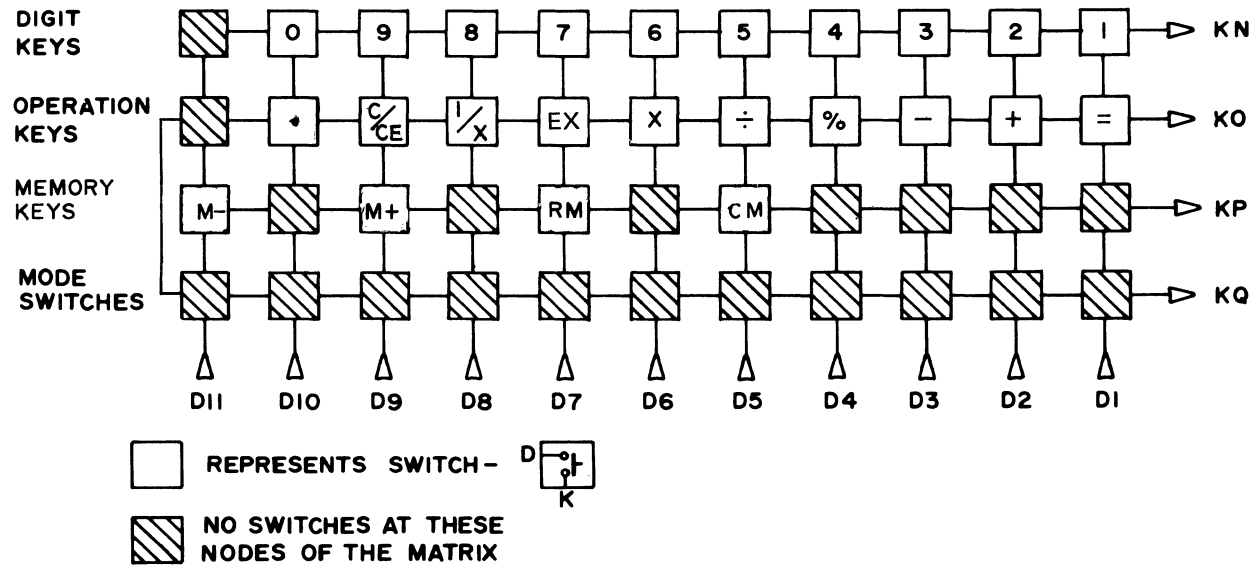
Low power dissipation, broad supply voltage range, a single power supply, and an internal clock oscillator make the MK 50203 ideal for battery-operated handheld calculators with lower system costs.

PIN CONNECTION



NC = NO CONNECTION

KEY MATRIX

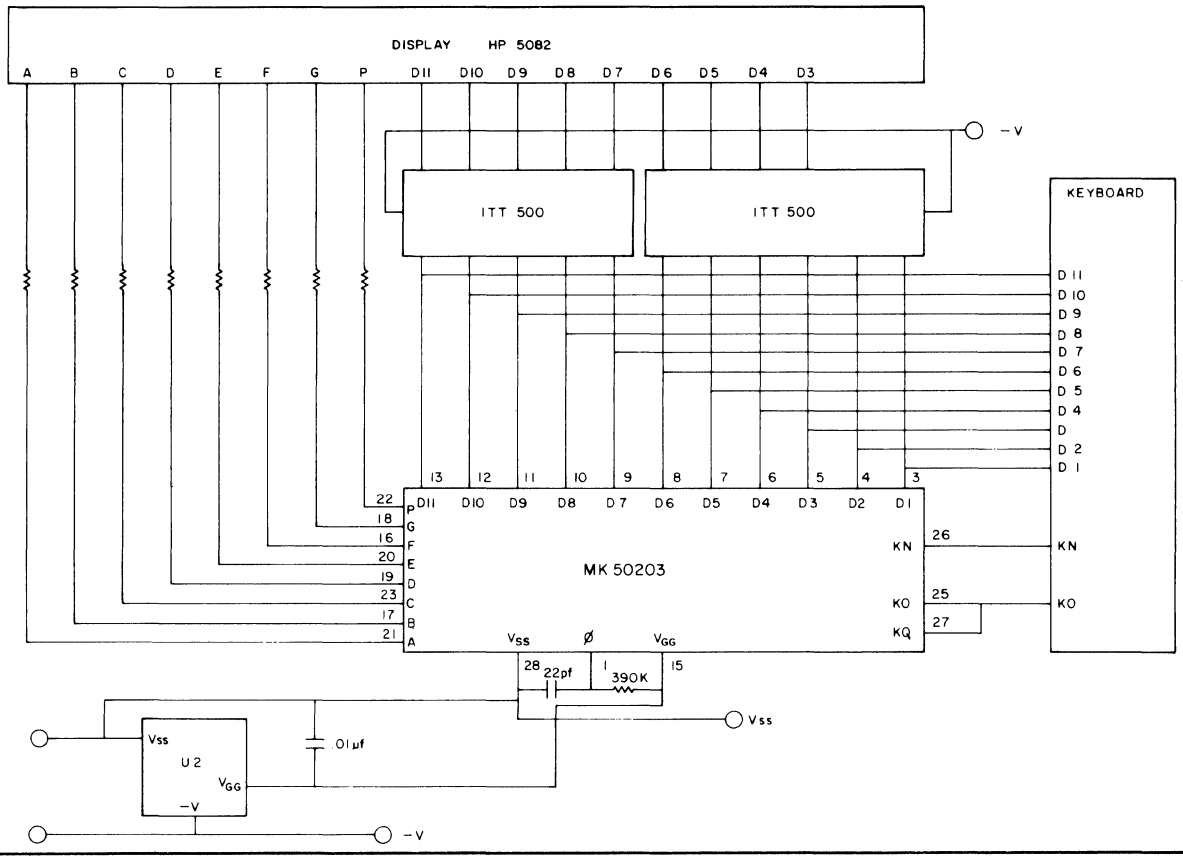


EXTERNALLY CONNECT KQ AND KO

DISPLAY FONT

Consumer

SCHEMATIC


DISPLAY HP 5082
A B C D E F G P D11 D10 D9 D8 D7 D6 D5 D4 D3
-V
ITT 500
ITT 500
KEYBOARD
D 11
D 10
D 9
D 8
D 7
D 6
D 5
D 4
D
D 2
D 1
MK 50203
KN
KO
KQ
Vss
Ø
VGG
28
22pf
1
390K
15
Vss
U 2
VGG
-V
01µf
-V

REMARKS	KEY ENTRIES	REMARKS	DISPLAY
MEMORY ADD			
	M }	{ Clears	1.0
	C }	{ Memory	0.
+27.84	C	Clears display	27.84
+56.352	27.84		27.84
	M		L 27.84
	+	Memory in use indicator	L 56.352
	56.352		L 56.352
	M }	{ adds display	L 56.352
	+ }	{ to memory	L 84.192
	R/S	recals total	
Exchange Operands			
26.3 ÷ 2.18 =	C		0.
	26.3		26.3
	÷		26.3
	2.18		2.18
	=		12.06422
2.18 ÷26.3 =	C		0.
	26.3		26.3
	÷		26.3
	2.18		2.18
	EX	1st entry will be stored as constant	26.3
	=		0.0828897
39.7 ÷ 26.3=	39.7		39.7
	=		1.5095057
2X3 =	C		0.
4X2 =	2		2.
5X2 =	X		2.
	3		3.
	EX	1st entry will be stored as constant	2.
	=		6.
	4		4.
	=		8.
	5		5.
	=		10.

PRELIMINARY

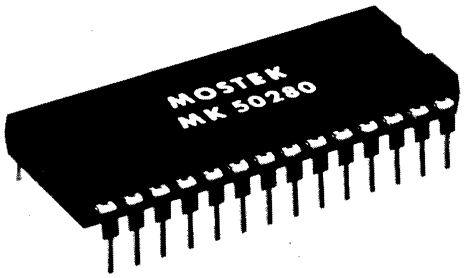
MK 50280 N Series

8-Digit Calculator Series

MOSTEK

FEATURES

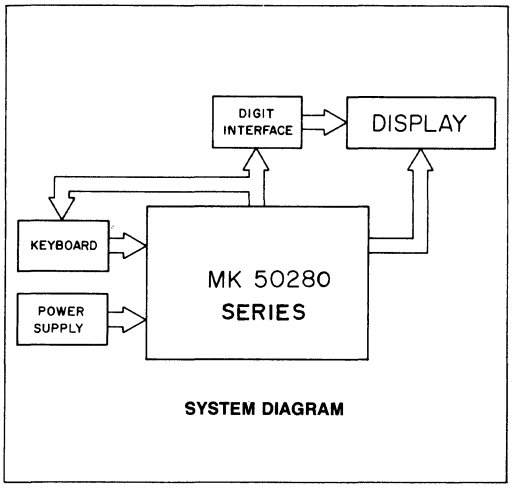
- ☐ Direct Segment Drive for LED's
- ☐ Low Power Consumption
- ☐ Single Power Supply Voltage
- ☐ Internal Clock Requiring No External Components
- ☐ Single 28-pin, Dual-in-line Package
- ☐ Internal Encoding of Keyboard Inputs
- ☐ Internal Debouncing of Keyboard Inputs
- ☐ Regulated Segment Outputs
- ☐ ROM Controlled



STANDARD PRODUCTS

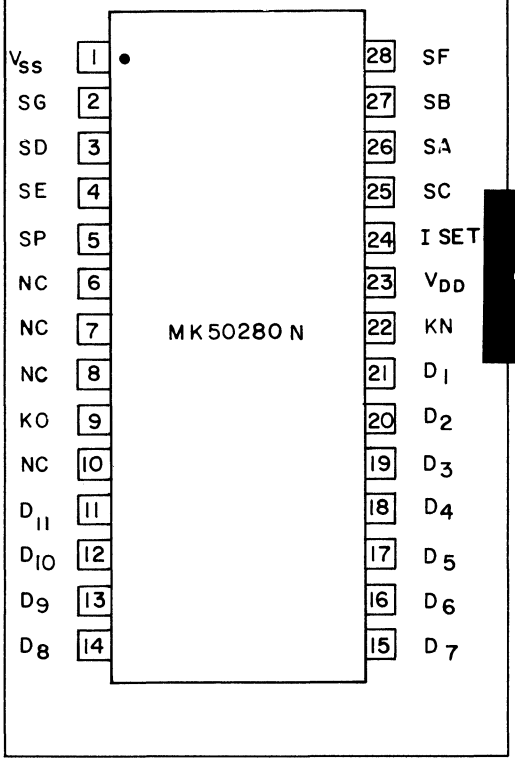
- ☐ MK 50281 8-digit, five-function (+, –, X, ÷, %) with automatic constant and store/recall memory
- ☐ MK 50282 8-digit, five-function (+, –, X, ÷, %) with automatic constant, average function and item counter.
- ☐ MK 50283 8-digit, six-function (+, –, X, ÷, %, √) with automatic constant

8-DIGIT CALCULATOR



SYSTEM DIAGRAM

PIN CONNECTION



Consumer

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE
(All voltages relative to V_{SS})

Supply Voltage Range V ..... +0.3V to −20V

Input Voltage Range ..... +0.3V to −20V

Output Voltage Breakdown SA−SG ..... +0.3V to −17V

DI−DII ..... +0.3V to −17V

Operating Free-Air Temperature Range ..... 0°C to +55°C

Storage Temperature Range ..... −40°C to +100°C

RECOMMENDED OPERATING CONDITIONS ($0°C < T_A < 55°C$)

	PARAMETERS	MIN	TYP	MAX	UNITS
V_{GG}	Supply Voltage	−12	−14.5	−17	volts
V_{IH}	Input Voltage, Logic 1	V_{SS}−1.2			volts
V_{IL}	Input Voltage, Logic 0				volts
ϕ	Clock Period		Internal		μ sec

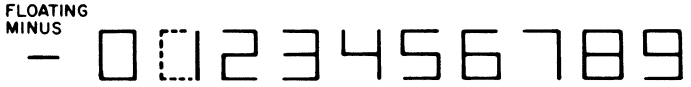
ELECTRICAL CHARACTERISTICS ($12 < V < 17; 0°C < T_A < 55°C$)

	PARAMETERS	MIN	TYP	MAX	UNITS
I_{GG}	Supply Current		6		mA
I_I	Input Current @ $V_{in} = V_{ss}$		150		μA
$R_{ON\ (SEG)}$	Segment Output "On" Resistance		Programmable		Ω
$R_{ON\ (DIG)}$	Digit Output "On" Resistance				Ω
$I_{OL\ (SEG)}$	Segment Output Leakage Current		.1	10	μA
$I_{OL\ (DIG)}$	Digit Output Leakage Current		.1	10	μA

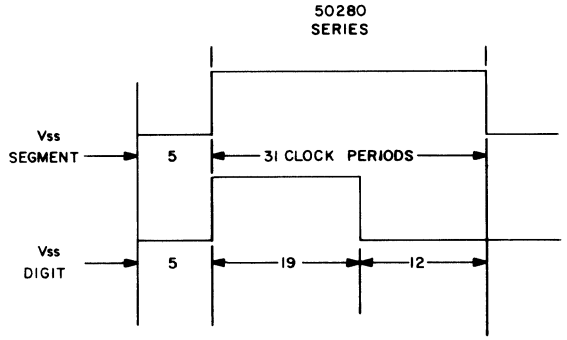
Consumer

DISPLAY FONT

FLOATING MINUS



NOTE: DISPLAY FLASHES FOR OVERFLOW



DESCRIPTION

The MK 50281 is a five-function (+, −, X, ÷, %), 8-digit calculator featuring automatic constant, floating negative sign, algebraic entry, floating decimal point, chain calculations, credit balance, leading zero suppression, display blanking during calculations and internal clock oscillator. A floating negative sign eliminates the need for a ninth digit. A store/recall memory allows the contents of the display register to be placed in memory for subsequent recall on demand.

OUTPUTS

The digit outputs, D_1–D_{11}, are selected (conduct to V_{ss}) sequentially. Note that there is inter-digit blanking. The digit lines are also fed back to the chip (min. level =) as keyboard inputs.

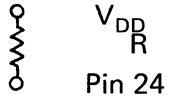
The segment outputs (SA–SG, Sdp) select the appropriate seven-segment code (with decimal point) for each digit as that digit is selected. ** A segment output conducts to V_{ss} when selected. When not selected, a segment output is in an open-drain state. The resultant display font is shown. * Segment output current is controlled by the I_{set} input (see direct drive).

*leading zeros are blanked
**The floating negative sign is always selected during the digit position to the immediate left of the most significant digit

DIRECT DRIVE

The regulated segment outputs of the MK 50281 are capable of sourcing up to mA for the purpose of driving the segments of common cathode LED displays. I_{set} (pin 24) regulates the segment output current. Placing a resistor between pin 24 and V_{DD} determines the peak segment current in the following manner

$$\text{Peak current} = 10 \times \frac{V_{DD}}{R}$$

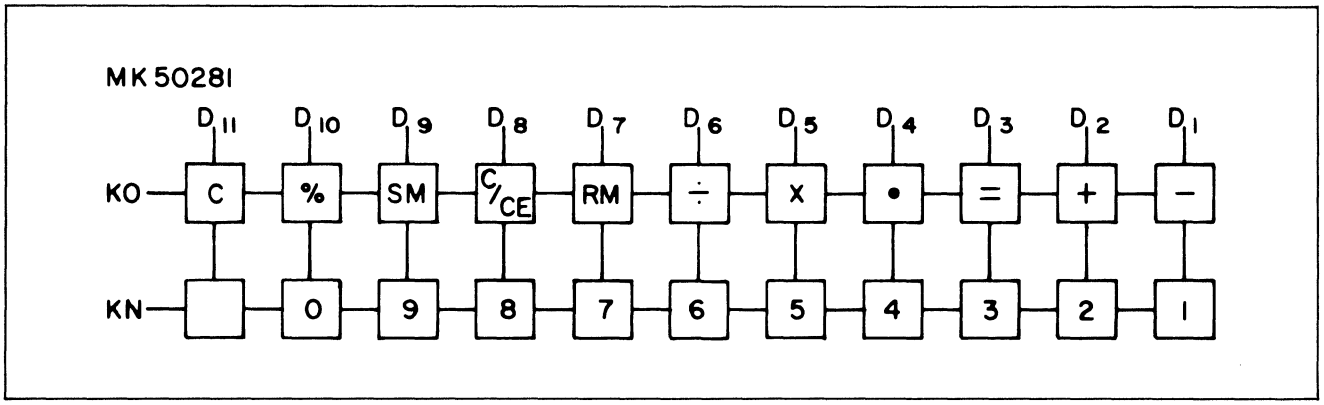


OVERFLOW

Attempting an entry of more than 8 digits exceeds the capacity of the MK 50281 and results in an entry overflow condition. This causes the display to blink repetitively as an overflow indication. All keys except C/CE will be inoperative. These, however, may be used to clear the overflow condition in the course of their usual function.

A calculated result in excess of 8 digits exceeds the capacity of the MK 50281 and produces a result overflow condition. This causes the display to blink repetitively as an overflow condition. The display will contain the correct answer (÷ by 10^8 to 8 significant decimal places). All keys except C/CE will be inoperative. This may be used to clear the overflow condition in the course of its usual function.

KEY MATRIX



% - Computes and displays a percentage of a number which may be added to (tax) or subtracted from (discount) the original value.

SM - Store the display to the memory register.

RM - Recalls the memory register to the display.

Consumer

DESCRIPTION:

The MK 50282 is a five-function (+, –, X, ÷, %), -8-digit calculator with an average value function, an item counter function and automatic constant. Additional features are floating negative sign, algebraic entry, floating decimal point, chain calculations, credit balance, leading zero suppression, display blanking during calculations, and internal clock oscillator. A floating negative sign eliminates the need for a ninth digit.

OUTPUTS

The digit outputs, D_1–D_{11}, are selected (conduct to V_{SS}) sequentially. Note that there is inter-digit blanking. The digit lines are also fed back to the chip (min. level =) as keyboard inputs.

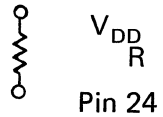
The segment outputs (SA–SG, Sdp) select the appropriate seven-segment code (with decimal point) for each digit as that digit is selected. ** A segment output conducts to V_{SS} when selected. When not selected, a segment output is in an open-drain state. The resultant display font is shown.* Segment output current is controlled by the I_{set} input (see direct drive).

*leading zeros are blanked
**The floating negative sign is always selected during the digit position to the immediate left of the most significant digit

DIRECT DRIVE

The regulated segment outputs of the MK 50282 are capable of sourcing up to mA for the purpose of driving the segments of common cathode LED displays. I_{set} (pin 24) regulates the segment output current. Placing a resistor between pin 24 and V_{DD} determines the peak segment current in the following manner

$$\text{Peak current} = 10 \times \frac{V_{DD}}{R}$$



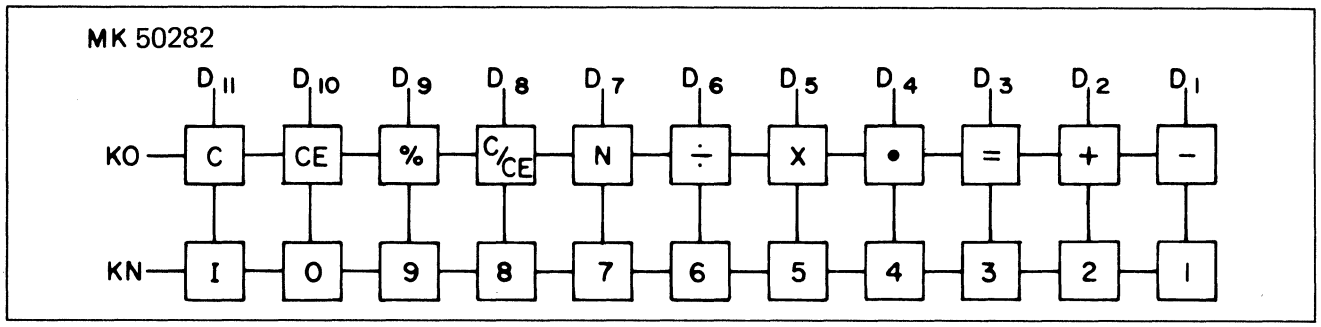
OVERFLOW

Attempting an entry of more than 8 digits exceeds the capacity of the MK 50282 and results in an entry overflow condition. This causes the display to blink repetitively as an overflow indication. All keys except C/CE will be inoperative. These, however, may be used to clear the overflow condition in the course of their usual function.

A calculated result in excess of 8 digits exceeds the capacity of the MK 50282 and produces a result overflow condition. This causes the display to blink repetitively as an overflow indication. The display will contain the correct answer (÷ by 10^8 to 8 significant decimal places). All keys except C/CE will be inoperative. This may be used to clear the overflow condition in the course of its usual function.

Consumer

KEY MATRIX



% - Computes and displays a percentage of a number which may be added to (tax) or subtracted from (discount) the original value.

N - Recalls the number of entries in a list. This may be divided into the total to compute the average value.

I - Permits the calculator to be used as a counter. Each depression of the key increments the display by one.

DESCRIPTION

The MK 50283 is a six-function (+, −, X, ÷, %, √), 8-digit calculator featuring automatic constant, floating negative sign, algebraic entry, floating decimal point, chain calculations, credit balance, leading zero suppression, display blanking during calculations, and completely internal clock oscillator. A floating negative sign eliminates the need for a ninth digit.

OUTPUTS

The digit outputs, D_1—D_{11}, are selected (conduct to V_{ss}) sequentially. Note that there is inter-digit blanking. The digit lines are also fed back to the chip (min level =) as keyboard inputs

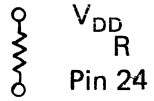
The segment outputs (SA—SG, Sdp) select the appropriate seven-segment code (with decimal point) for each digit as that digit is selected. ** A segment output conducts to V_{ss} when selected. When not selected, a segment output is in an open-drain state. The resultant display font is shown.* Segment output current is controlled by the I_{set} input (see direct drive).

*leading zeros are blanked
**The floating negative sign is always selected during the digit position to the immediate left of the most significant digit

DIRECT DRIVE

The regulated segment outputs of the MK 50283 are capable of sourcing up to mA for the purpose of driving the segments of common cathode LED displays. I_{set} (pin 24) regulates the segment output current. Placing a resistor between pin 24 and V determines the peak segment current in the following manner

$$\text{Peak current} = 10 \times \frac{V_{DD}}{R}$$

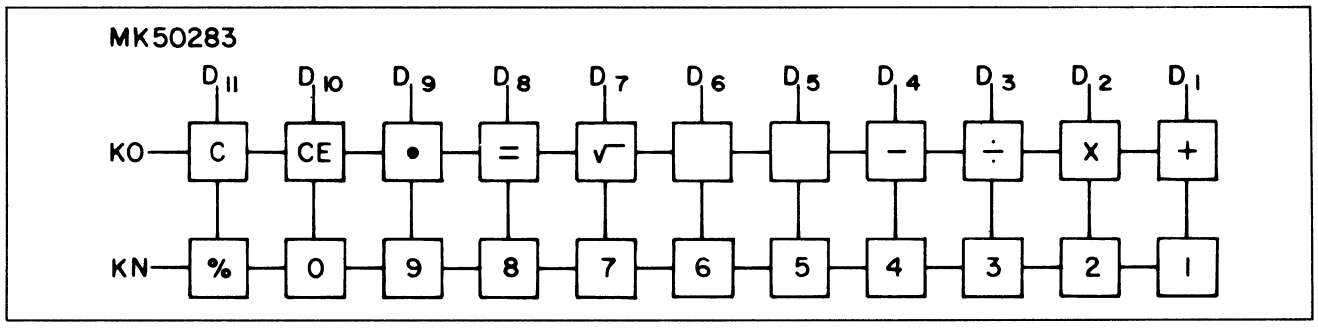


OVERFLOW

Attempting an entry of more than 8 digits exceeds the capacity of the MK 50283 and results in an entry overflow condition. This causes the display to blink repetitively as an overflow condition. All keys except C/CE will be inoperative. These, however, may be used to clear the overflow condition in the course of their usual function.

A calculated result in excess of 8 digits exceeds the capacity of the MK 50283 and produces a result overflow condition. This causes the display to blink repetitively as an overflow indication. The display will contain the correct answer (÷ by 10^8 to 8 significant decimal places). All keys except C/CE will be inoperative. This may be used to clear the overflow condition in the course of its usual function.

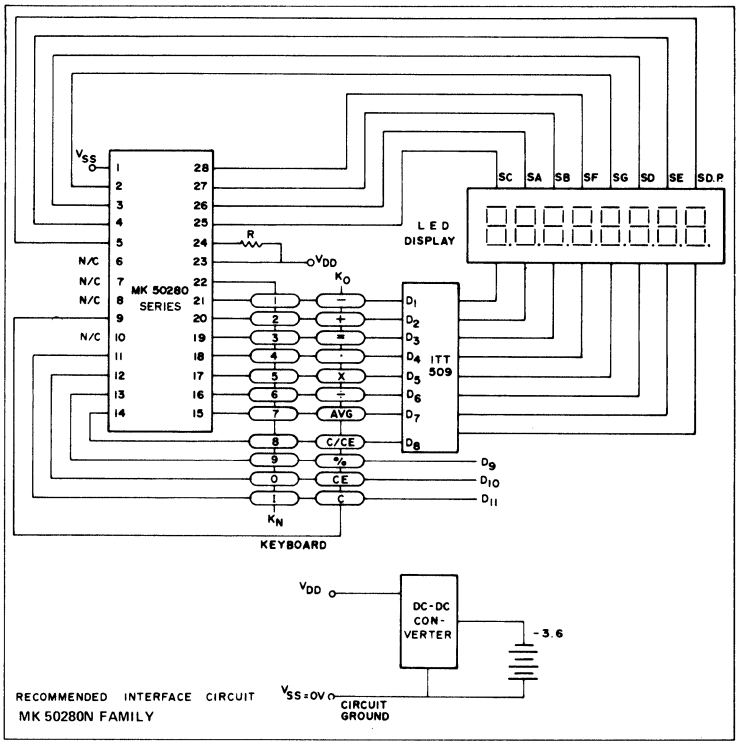
KEY MATRIX

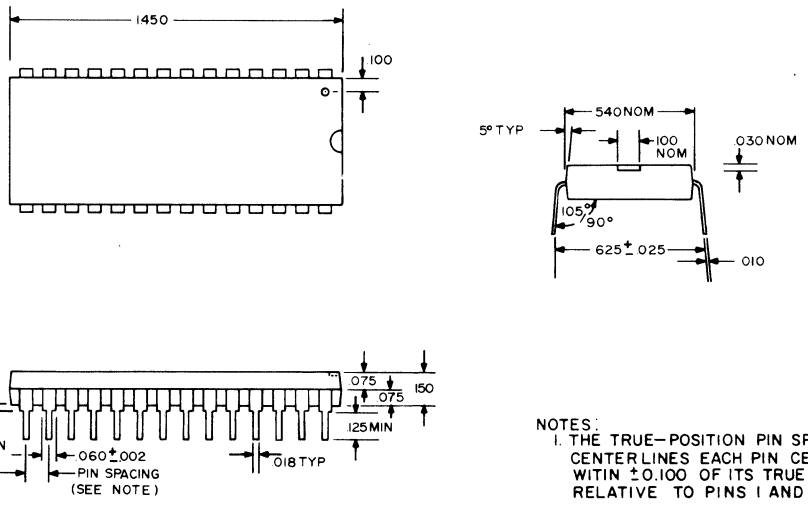


% - Computes and displays a percentage of a number which may be added to (tax) or subtracted from (discount) the original value.

√ Computes the square root of the display.

Consumer





NOTES:
1. THE TRUE-POSITION PIN SPACING IS 0.100 BETWEEN CENTERLINES EACH PIN CENTERLINE IS LOCATED WITIN ±0.100 OF ITS TRUE LONGITUDINAL POSITION RELATIVE TO PINS 1 AND 28.

Consumer

MK 50040F-1
MK 50040F-2

CMOS Oscillator/Divider

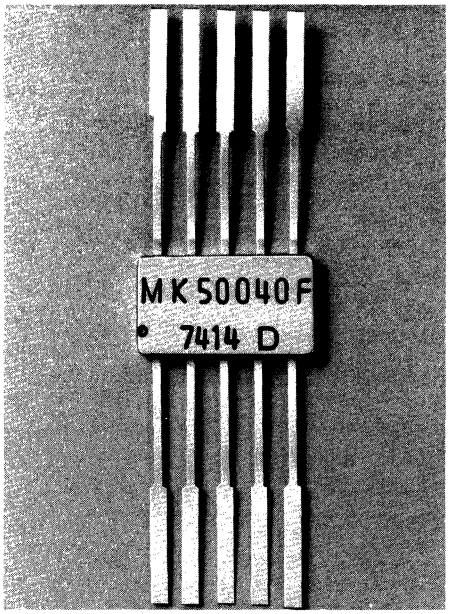
MOSTEK®

FEATURES:

Low power dissipation

Direct replacement for SCL 5437

Inverter for crystal controlled oscillator with external frequency determination

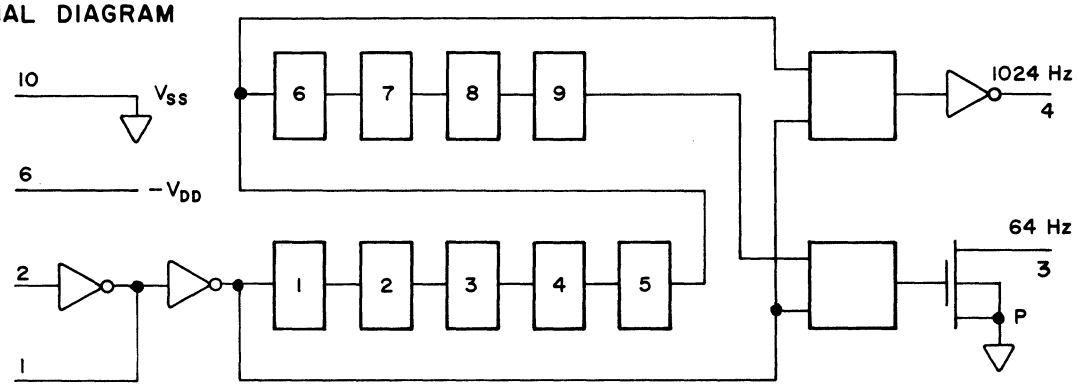


DESCRIPTION:

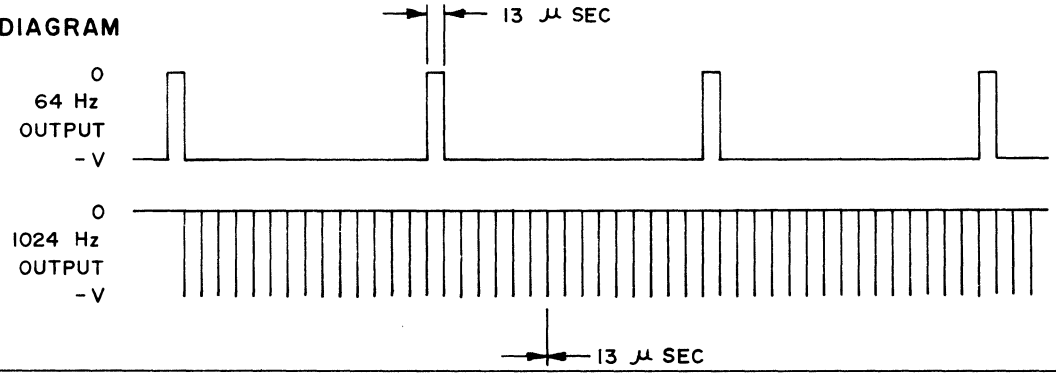
The MK 50040 is a CMOS nine stage binary ripple divider useful in timekeeping applications. The chip has two output frequencies of 64 Hz and 1024 Hz with an input frequency of 32768 Hz determined by a crystal. The 64Hz provides the main timekeeping pulses and the 1024Hz is used to operate a dc-dc converter.

The 64 Hz output device is an open-drain P-channel device which will deliver 50 μA with -1 volt drop when on and less than 50 na at -15 volts (for MK 50040F-1) or -10 volts (for MK 50040F-2) when off. The 1024 Hz output is a CMOS inverter.

FUNCTIONAL DIAGRAM



TIMING DIAGRAM



Consumer

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range −40° to +100°C

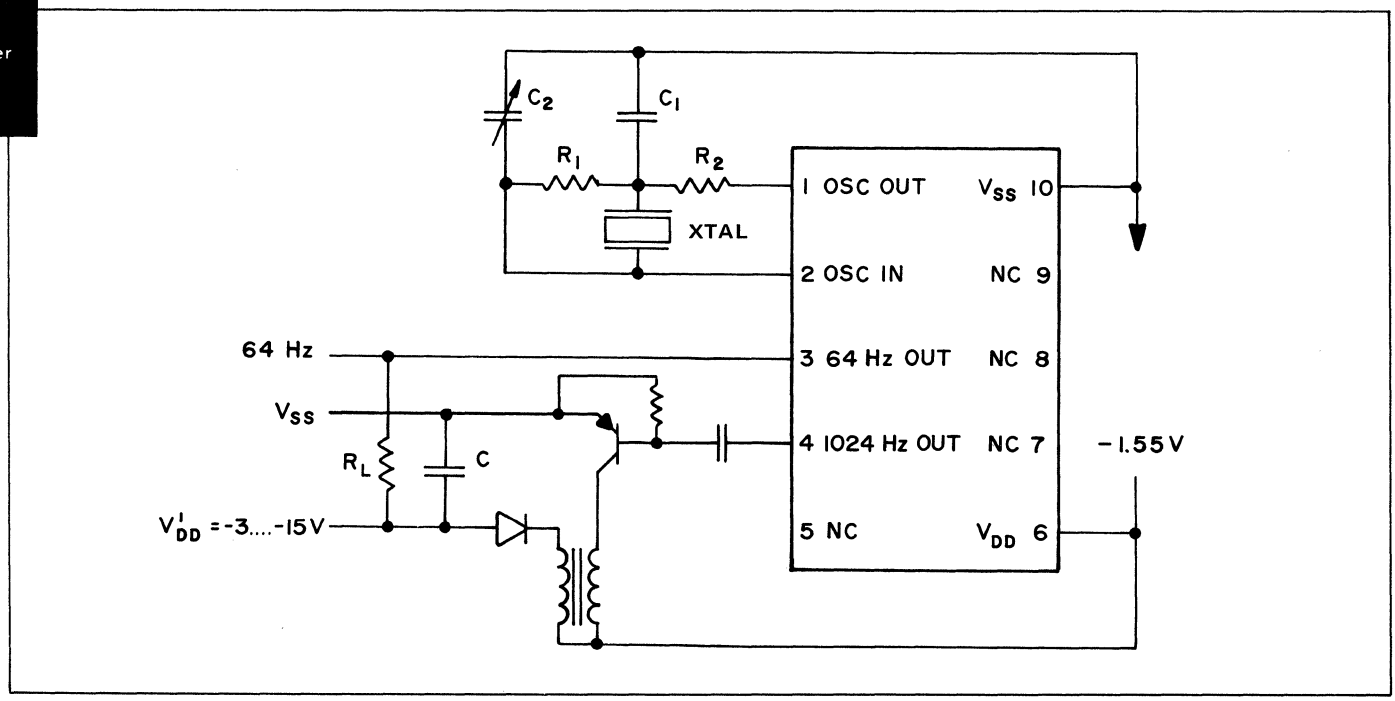
Operating Temperature Range −10° to +60°C

DYNAMIC OPERATING CHARACTERISTICS at T_A = 25°C, V_{DD} = −1.55V

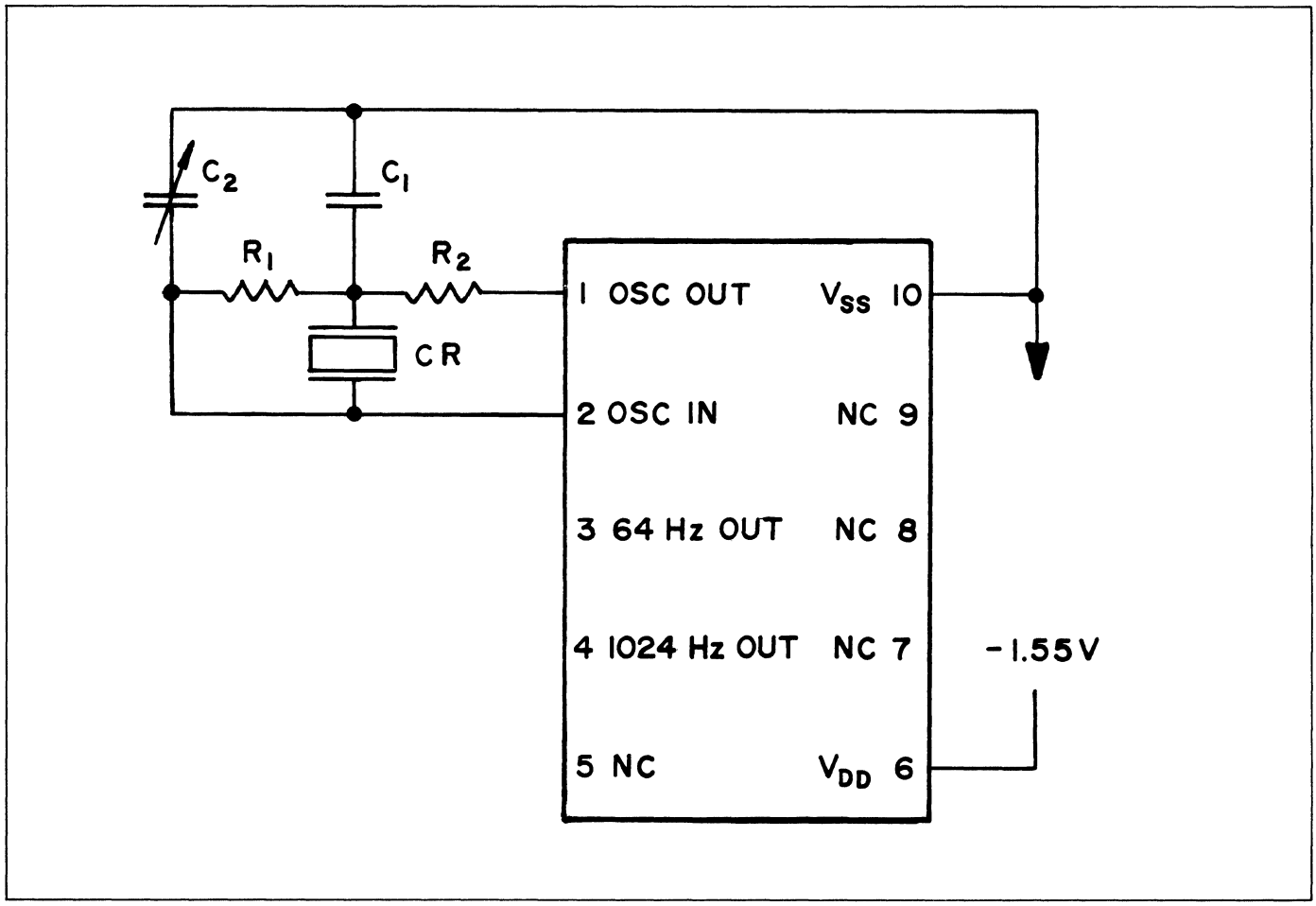
CHARACTERISTICS		SYMBOL	TEST CONDITIONS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Operating Current		I_L	Oscillator Frequency 32768 Hz No Load			3	5	µA
Minimum Starting Voltage		V_S			−1.35			Volt
Output Current MK 50040F-1		I_1	64 Hz output Pin 3	ON V_{OUT} = −1 volt	50	75	—	µA
				OFF V_{OUT} = −15 volt	—	0.01	0.05	
Output Current MK 50040F-2		I_1	64 Hz output Pin 3	ON V_{OUT} = −1 volt	50	75	—	µA
				OFF V_{OUT} = −10 volt	—	0.01	0.05	
Pulse Width		$t_{w(64)}$	Pin 3		8	13	18	µsec
Output Current	Sink	I_2	Pin 4 1024 Hz output	"0" V_{OUT} = V_{DD} +.7V	200	—		µA
	Source			"1" V_{OUT} = −.2V	20	—	—	
Pulse Width		$t_{w(1024)}$	Pin 4		8	13	18	µsec

It is very important in testing and application of low power time base IC's that external wiring or interconnection capacitance be minimal since such capacitance can cause significantly increased power consumption.

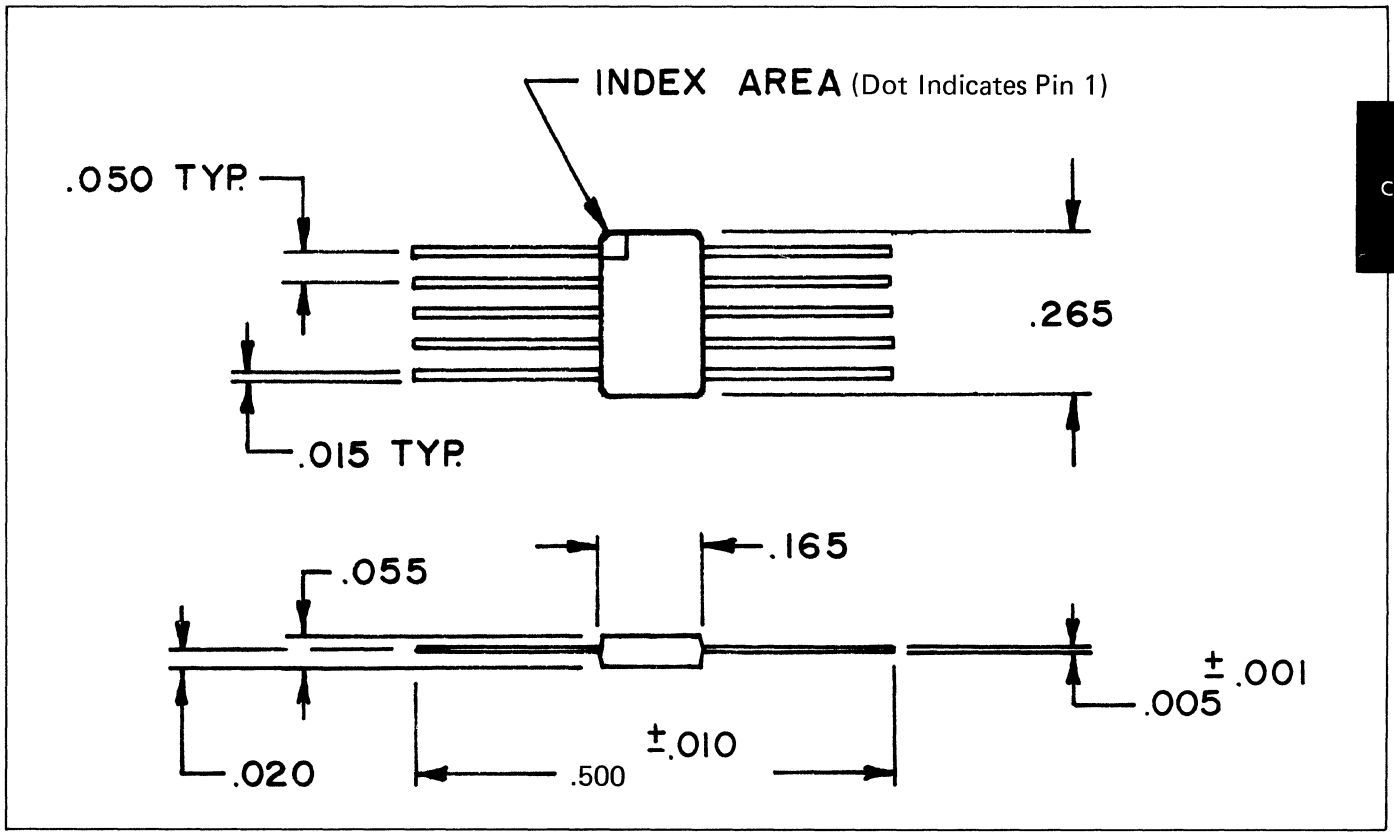
RECOMMENDED CIRCUIT
for 32768 Hz crystal



SCHEMATIC



PACKAGE



Consumer

PRELIMINARY

MK 50250N Series

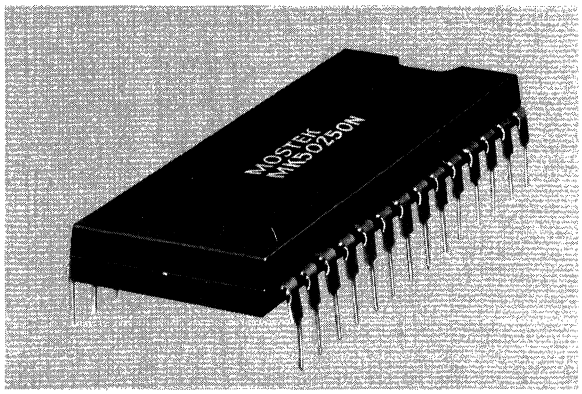
MOS Digital Alarm Clock

MOSTEK

FEATURES

Single Voltage Power Supply
Intensity Control
Simple Time Setting
4 or 6 Digit Display
AM/PM and Activity Indicator
Selectable Input Frequency and Output Mode
- MK 50250 – 12 hr/60 Hz or 24 hr/50 Hz
- MK 50253 – 12 hr/50 Hz or 24 hr/50 Hz
- MK 50254 – 12 hr/60 Hz or 24 Hr/60 Hz

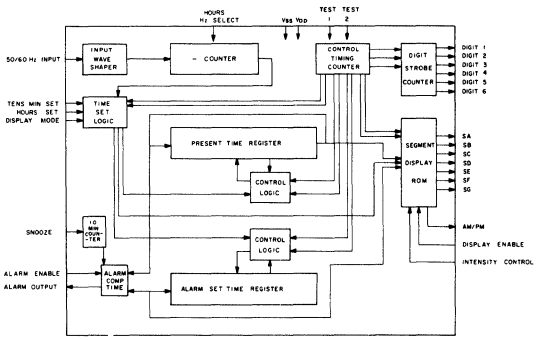
24 hr. Alarm
Snooze Alarm



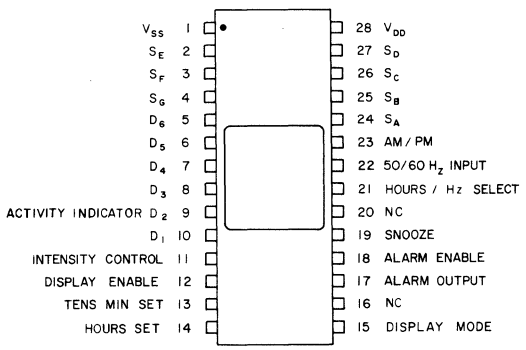
DESCRIPTION

The MK 50250 is a versatile MOS/LSI clock circuit manufactured by MOSTEK using its depletion-load, ion implantation process and P-channel technology. The circuit can be used to construct a digital alarm clock with the addition of only a simple power supply, display, and standard interfacing components. (See Typical Circuit Configuration). The circuit is compatible with 4 or 6 digit seven segment multiplexed displays. An AM/PM and circuit activity signal is generated by the chip. The alarm operates in a 24 hour mode, which allows the alarm to be disabled and immediately reenabled to activate 24 hours later. The snooze inhibits an activated alarm for 10 minutes.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



Consumer

ABSOLUTE MAXIMUM RATING OVER OPERATING FREE-AIR TEMPERATURE RANGE

Voltage on any pin relative to V_{SS}	+0.3 to −18.0 V
Output Voltage Breakdown on any output relative to V_{SS}	−18.0V @ 10 μA
Operating Free-Air Temperature Range	0°C to 55°C
Storage Temperature Range	−40°C to + 100°C

RECOMMENDED OPERATING CONDITIONS ($0°C \leq T_A \leq 55°C$)

PARAMETER	MIN	MAX	UNITS	NOTES
Operating Voltage V_{DD} Relative to V_{SS}	−18.0	−9.0	volts	9
Input Logic Levels				1, 2
"1" Logic Level	V_{SS}−0.3	V_{SS}+0.3	volts	
"0" Logic Level	−18.0	V_{DD}+0.5	volts	

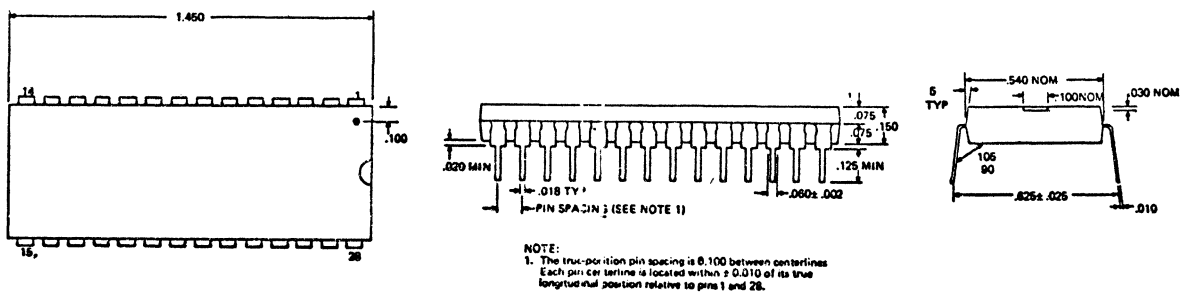
ELECTRICAL CHARACTERISTICS ($9V \leq V_{SS} - V_{DD} \leq 18V, 0°C \leq T_A \leq 55°C$)

PARAMETER	MIN	MAX	UNITS	NOTES
Output Current S_A–S_G, D_6–D_1, AM/PM				
"1" Logic Level	0.5		mA	3
"0" Logic Level				4
Alarm Output Current				
"1" Logic Level	0.5		mA	3
"0" Logic Level	−5.0		μA	5
Supply Current, I_{DD}		10	mA	8
Input Current				
Tens Min Set, Hours Set	50	1000	μA	6
Hours/Hz Select	5	100	μA	
Alarm Enable, Snooze	5	100	μA	
50/60 Hz Input, Display Enable	−15	−200	μA	7

Notes:
1. 50/60 Hz Input has 3 volts of hysteresis for noise protection
2. "Display Mode" and "Intensity" are three state inputs which will self seek third state if left open.
3. Output voltage equal to V_{SS}−2.0 volts.
4. Open drain output.
5. Output voltage equal to V_{DD} +4.0 volts.
6. For power up clear, capacitance to V_{SS} must not exceed 20pF.
7. Pull-up device provided on 50/60 Hz input.
8. Outputs open
9. Pins 16 and 20 may be tied to V_{SS} or left floating.

PACKAGE DESCRIPTION

28-lead dual-in-line plastic package

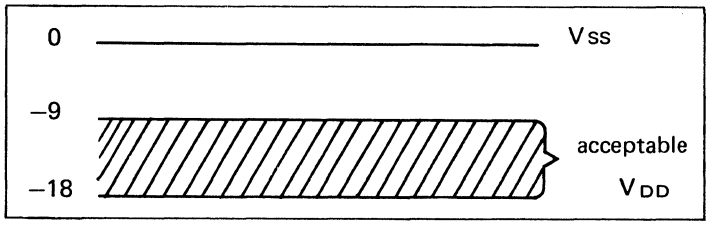


NOTE:
1. The true position pin spacing is 0.100 between centerlines. Each pin centerline is located within ± 0.010 of its true longitudinal position relative to pins 1 and 28.

Consumer

OPERATION

The MK 50250 requires a single power supply with a voltage range from $9V \leq V_{SS} - V_{DD} \leq 18$.

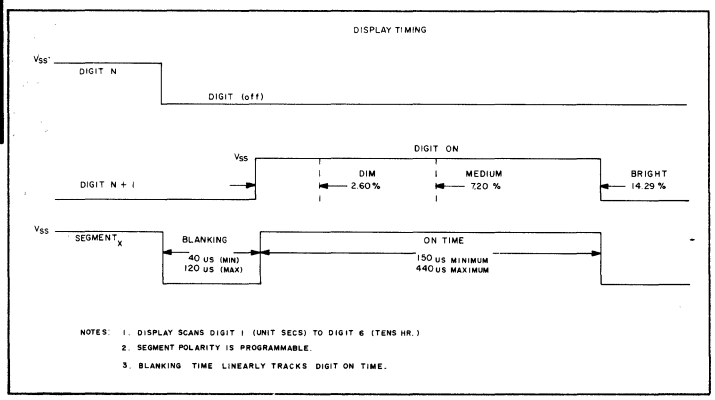


A Three State Input is one of the features which MOSTEK has employed on the MK 50250 to reduce system expense and simplify operation for the consumer. By switching Display Mode to one of three possible states the mode of operation is as follows:

Display Mode Input	Mode
V_{SS}	Alarm Set
Open	Real Time
V_{DD}	Count Inhibit

When in alarm set mode the alarm time is displayed and may be altered using the time set procedure (see setting). In the real time mode the real time is displayed andmay also be altered using the same procedure. Count inhibit halts the counting of the clock. The display shows the halted time and may be altered by the time set procedure.

The display outputs of the MK 50250 requires the use of segment displays which can be multiplexed. The scaning oscillator is completely internal and requires no external components. As can be seen in the timing diagram each digit is on 14.29% of the time required to scan all 6 possible digits when the intensity mode switch is on bright.



The Intensity Control Input provides the following degrees of display intensity:

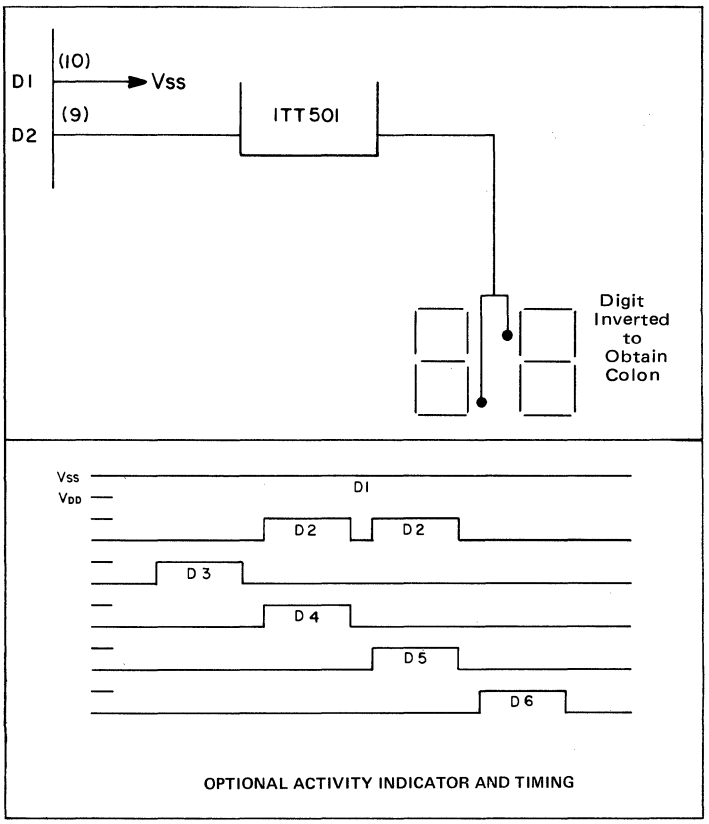
Intensity Control Input	Mode	Duty Cycle
V_{SS}	Bright	14.29%
Open	Medium	7.20%
V_{DD}	Dim	2.60%

The intensity can be controlled either manually or automatically (see "Automatic Intensity Control diagram").

The display can be blanked by an external control by connecting the Display Enable input to V_{DD}. Leaving this pin open allows internal pull-up to V_{SS} which enables the display. This feature allows the display to be time shared with other information.

When power is initially applied both real time and alarm time will be at 12:00:00 midnight in the 12 hr. mode and 00:00:00 in the 24 hr. mode. The units minutes digit can be advanced at a 2 Hz rate by connecting both the hours set pin and the tens minute set pin to V_{SS}, this also resets seconds to zero. The tens minute digit will advance at a 2 Hz rate when the tens minute set pin is connected to V_{SS}. The hours digit will be advanced by connecting the hr. set pin to V_{SS}. The carry from one digit to the next more significant digit does occur so setting should be performed from the least significant digit to the most significant. Both pins have internal pull-down resistors and can be either left open or tied to V_{DD} when not being used.

The chip can be used with either a 4 or 6 digit display. If digits D_1 and D_2 are not used to display seconds and tens of seconds, the user is unable to tell if the circuit is active until the minutes digit changes. In order to more quickly determine clock activity, a colon or other indicator can be flashed at a 1 Hz rate by connecting D_1 to V_{ss}. D_2 can then be used to drive the colon or activity indicator. The D_2 output used in this mode occurs during D_4 and D_5 time so that the decimal point for digits D_4 and D_5 can be used as a colon.



OPTIONAL ACTIVITY INDICATOR AND TIMING

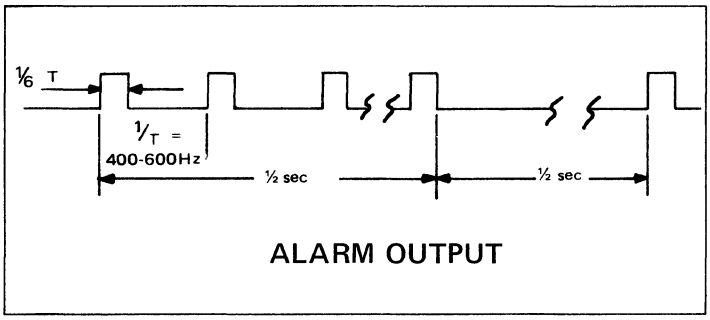
The AM/PM output operates with an 85% duty cycle at full intensity and conducts to V_{SS} for PM indication.

If a "brown out" occurs, the AM/PM indicator will flash at a 1 Hz rate to signify an incorrect display time. This low power indication continues until proper power is restored and the clock is reset.

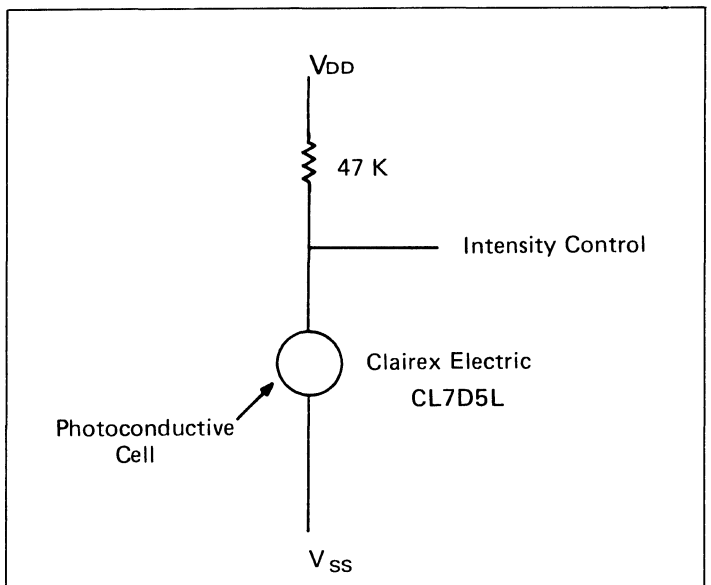
The Hours/Hz Select input is provided with an internal pull-down resistor to V_{DD}. On the MK 50250 if this pin is left open or connected to V_{DD} the clock will be in the 12 hour/60 Hz mode; if it is connected to V_{SS}, it will be in the 24 hour/50 Hz mode. For the MK 50253 an open or V_{DD} causes the clock to be in the 12 hour/60 Hz mode. The MK 50254 requires an open or V_{SS} level for the 12 hour/60 Hz mode and a V_{SS} level for the 24 hour/60 Hz mode.

The Alarm Enable pin enables the alarm when connected to V_{SS}. If it is left open it will disable the alarm due to an internal pull down resistor to V_{DD}. When alarm occurs it may be disabled and immediately re-enabled and will activate 24 hours later at the alarm time. The output tone will be in the range of 400-600 Hz, and has a 1/6 duty cycle which conducts to V_{SS} 50% of the time at a 1 Hz rate.

The Snooze feature will temporarily turn off an activated alarm signal to allow an additional 10 minutes sleep Momentarily connecting snooze to V_{SS} will activate the snooze. If left open an internal pull down resistor to V_{DD} will maintain the snooze feature inoperative.



ALARM OUTPUT



AUTOMATIC INTENSITY CONTROL

TYPICAL CIRCUIT CONFIGURATION

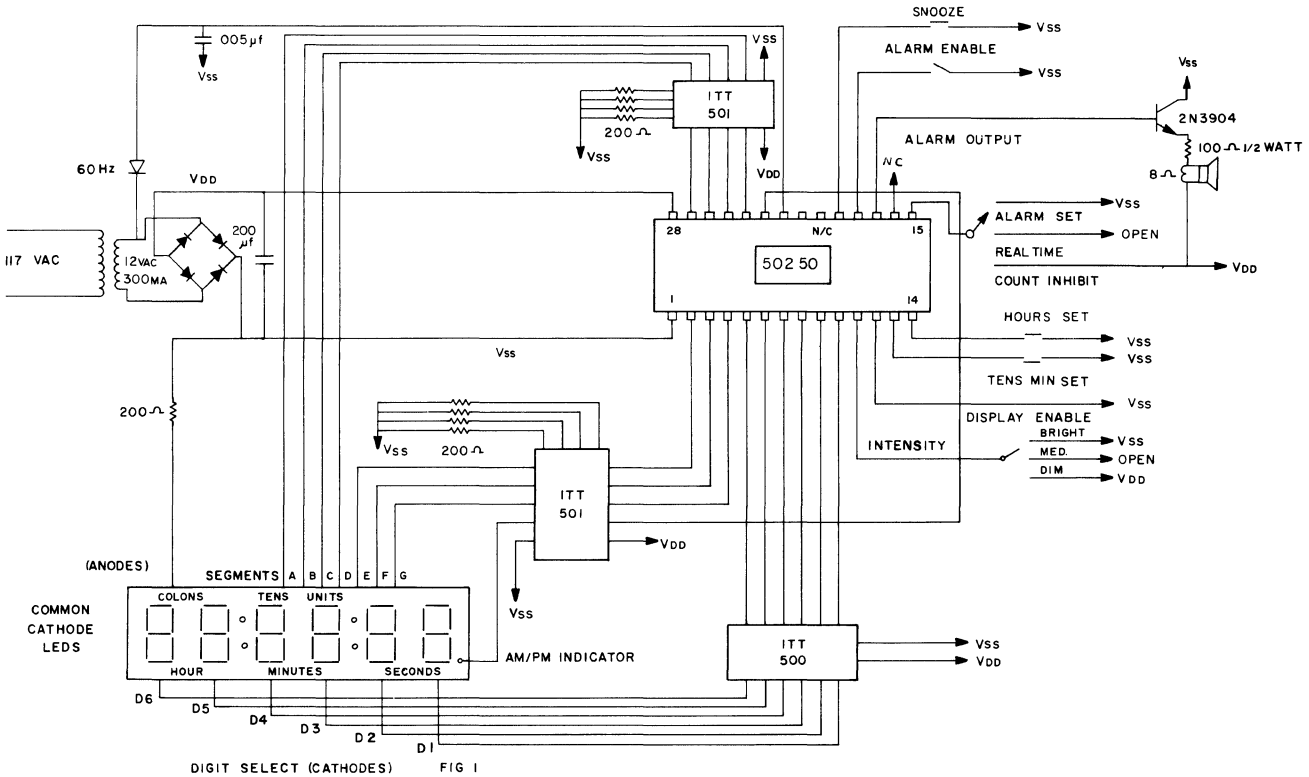


FIG 1

PRELIMINARY

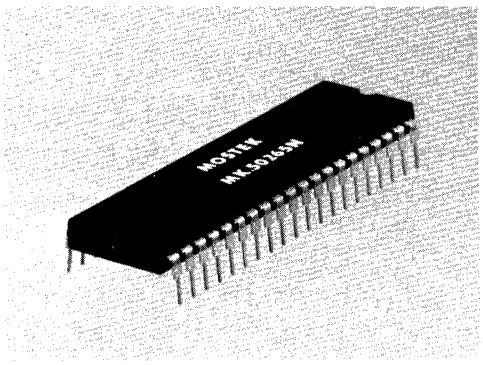
MK 50265 N

MOS Digital Radio Alarm Clock

MOSTEK®

FEATURES:

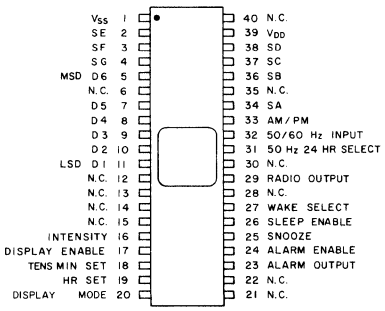
- Clock Radio Application, Special Waveform Timing to Reduce RFI
- Single Voltage Power Supply
- Simple Time Setting
- Intensity Control
- 4 or 6 Digit Display
- AM/PM and Activity Indicator
- 12 hr. — 60 Hz or 24 hr. — 50 Hz Capability
- 24 hr. Alarm
- Snooze Alarm
- Three Function Wake Select
- Incremental Sleep
- Count Inhibit



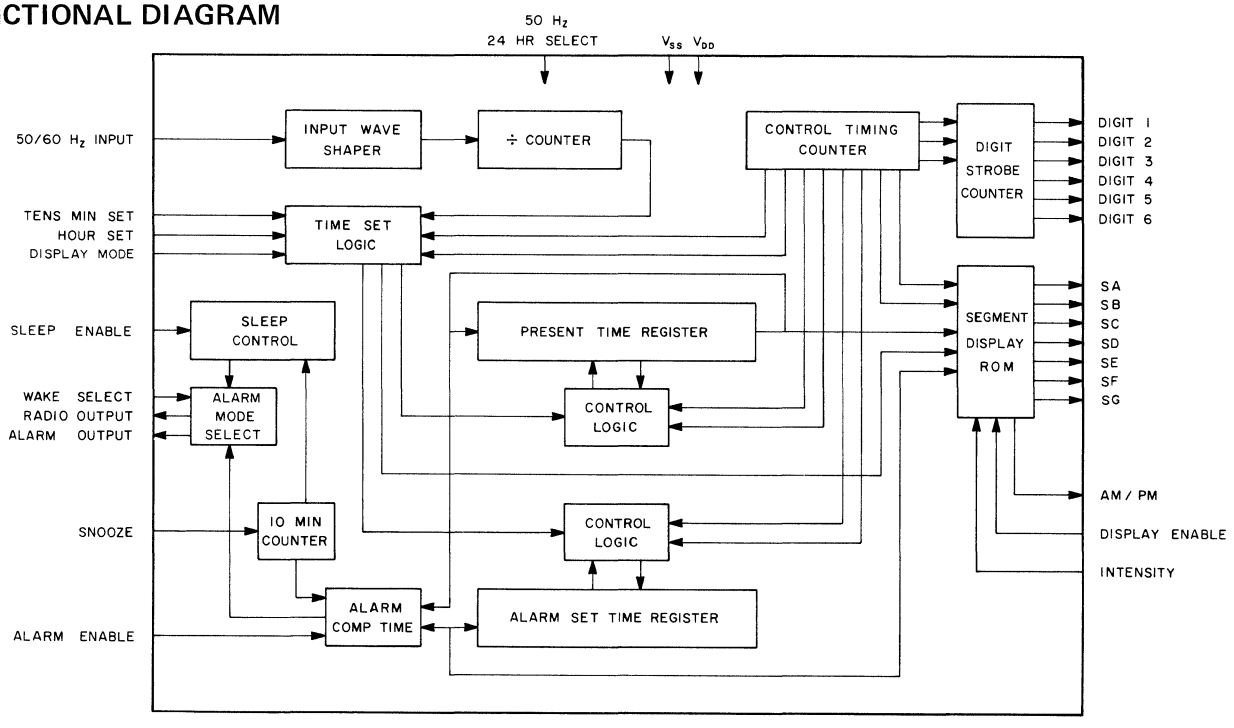
DESCRIPTION:

The MK 50265 is a versatile MOS/LSI clock circuit manufactured by MOSTEK using its depletion-load, ion implantation process and P-channel technology. The circuit can be used to construct a digital radio alarm clock with the addition of only a simple power supply, display, and standard interfacing components. The circuit is compatible with 4 or 6 digit seven segment multiplexed displays. An AM/PM and circuit activity signal is generated by the chip. The alarm has three modes of operation, tone only, radio only, and radio followed by a tone. The alarm operates in a 24 hour mode which allows the alarm to be disabled and immediately reenabled to activate 24 hours later. The snooze inhibits an activated alarm for 10 minutes. The sleep feature activates the radio for an adjustable period of time.

PIN CONNECTION



FUNCTIONAL DIAGRAM



Consumer

ABSOLUTE MAXIMUM RATING OVER OPERATING FREE-AIR TEMPERATURE RANGE

Voltage on any pin relative to V_{SS} . . . . . +0.3 to −18.0 V

Output Voltage Breakdown on any output relative to V_{SS} . . . . . −18.0V @ 10 μA

Operating Free-Air Temperature Range . . . . . 0°C to 55°C

Storage Temperature Range . . . . . −40°C to + 100°C

RECOMMENDED OPERATING CONDITIONS ($0° C \leq T_A \leq 55° C$)

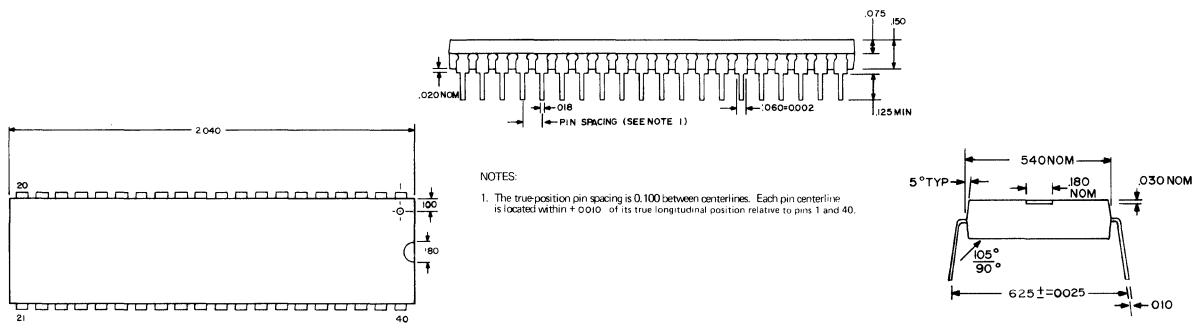
PARAMETER	MIN	MAX	UNITS	NOTES
Operating Voltage V_{DD} Relative to V_{SS}	−18.0	−9.0	volts	9
Input Logic Levels				1, 2
"1" Logic Level	V_{SS} −0.3	V_{SS} +0.3	volts	
"0" Logic Level	−18.0	V_{DD}+0.5	volts	

ELECTRICAL CHARACTERISTICS ($9V \leq V_{SS} - V_{DD} \leq 18V$, $0° C \leq T_A \leq 55° C$)

PARAMETER	MIN	MAX	UNITS	NOTES
Output Current $S_A - S_G$, $D_6 - D_1$, AM/PM				
"1" Logic Level	0.5		mA	3
"0" Logic Level				4
Tone Out and Radio Out Current				
"1" Logic Level	0.5		mA	3
"0" Logic Level	−5.0		μA	5
Supply Current, I_{DD}		10	mA	8
Input Current				
Tens Min Set, HRS SET	50	1000	μA	6
50 Hz-24 Hr. Select	5	100	μA	
Alarm Enable,Snooze	5	100	μA	
50/60 Hz Input, Display Enable	−15	−200	μA	7
Sleep	15	200	μA	

Notes:
1. 50/60 Hz Input has 1½ volts of hysteresis for noise protection.
2. "Display Mode" and "Intensity" and "Wake Select" are three state inputs which will self seek third state if left open.
3. Output voltage equal to V_{SS}−2.0 volts.
4. Open drain output.
5. Output voltage equal to V_{DD} +4.0 volts.
6. For power up clear, capacitance to V_{SS} must not exceed 20pF.
7. Pull-up device provided on 50/60 Hz input.
8. Outputs open
9. Pins 22 and 30 must be tied to V_{SS} or left floating.

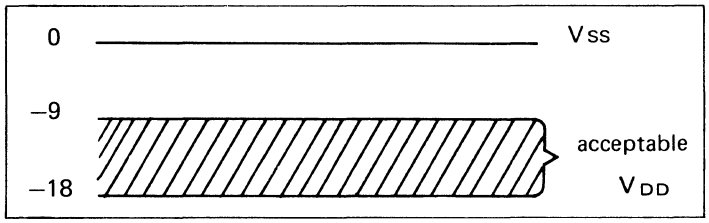
PACKAGE DESCRIPTION 40-lead dual-in-line plastic package



Consumer

OPERATION

The MK 50265 requires a single power supply with a voltage range from $9V \leq V_{SS} - V_{DD} \leq 18$.



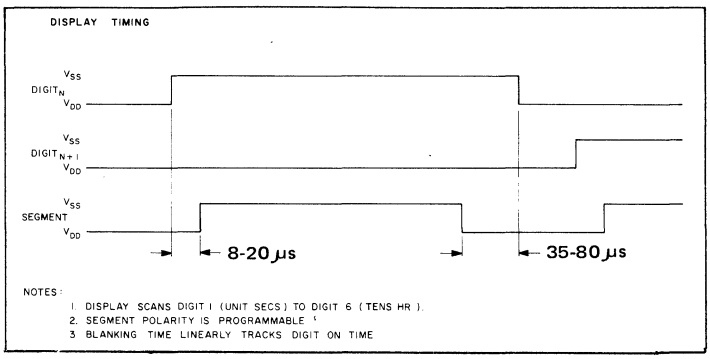
A Three State Input is one of the features which MOSTEK has employed on the MK 50265 to reduce system expense and simplify operation for the consumer. By switching Display Mode to one of three possible states the mode of operation is as follows:

Display Mode Input	Mode
V_{SS}	Alarm Set
Open	Real Time
V_{DD}	Count Inhibit

When in alarm set mode the alarm time is displayed and may be altered using the time set procedure (see setting). In the real time mode the real time is displayed and may also be altered using the same procedure. Count inhibit halts the counting of the clock. This display shows the halted time and may be altered by the time set procedure.

The display outputs of the MK 50265 require the use of segment displays which can be multiplexed. The scaning oscillator is completely internal and requires no external components. As can be seen in the timing diagram each digit is on 11.3% of the time required to scan all 6 possible digits when the intensity mode switch is on bright.

Segment on time lags digit on time and segment off time leads digit off time so that RFI reduction R-C networks can be added to the segment lines.



The Intensity Control Input provides the following degrees of display intensity:

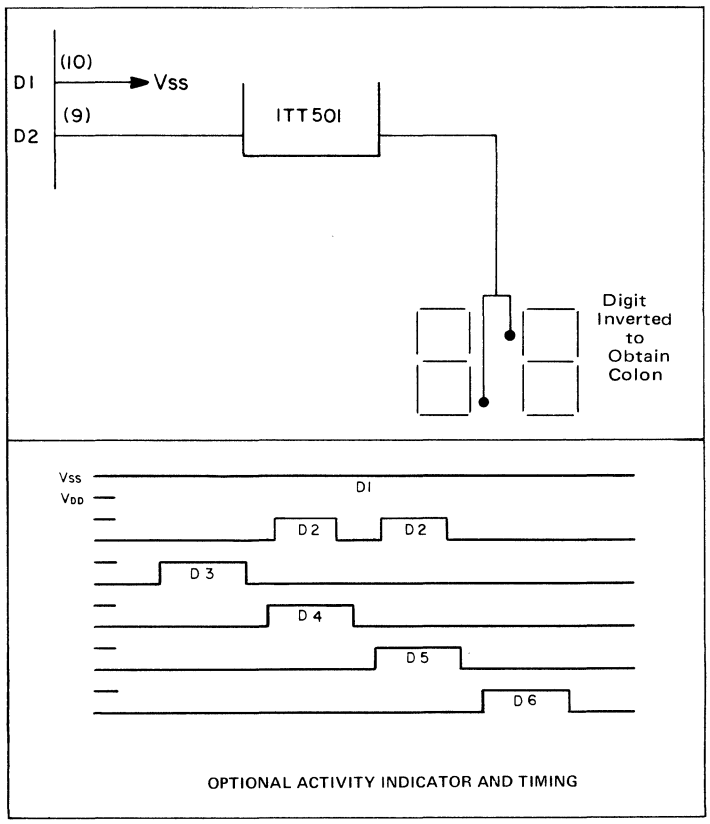
MODE	INPUT	DUTY CYCLE
Bright	V_{SS}	19/168=11.3%
Medium	Open	11/168=6.5%
Dim	V_{DD}	3/168=1.8%

The intensity can be controlled either manually or automatically.

The display can be blanked by an external control by connecting the Display Enable input to V_{DD}. Leaving this pin open allows internal pull-up to V_{SS} which enables the display. This feature allows the display to be time shared with other information.

When power is initially applied both real time and alarm time will be at 12:00:00 midnight in the 12 hr. 60 Hz mode and 00:00:00 in the 24 hr. 50 Hz mode. The units minutes digit can be advanced at a 2 Hz rate by connecting both the hours set pin and the tens minute set pin to V_{SS}, this also resets seconds to zero. The tens minute digit will advance at a 2 Hz rate when the tens minute set pin is connected to V_{SS}. The hours digit will be advanced by connecting the hr. set pin to V_{SS}. The carry from one digit to the next more significant digit does occur so setting should be performed from the least significant digit to the most significant. Both pins have internal pull-down resistors and can be either left open or tied to V_{DD} when not being used.

The chip can be used with either a 4 or 6 digit display. If digits D_1 and D_2 are not used to display seconds and tens of seconds, the user is unable to tell if the circuit is active until the minutes digit changes. In order to more quickly determine clock activity, a colon or other indicator can be flashed at a 1 Hz rate, by connecting D_1 to V_{ss}. D_2 can then be used to drive the colon or activity indicator. The D_2 output used in this mode occurs during D_4 and D_5 time so that the decimal point for digits D_4 and D_5 can be used as a colon.



OPTIONAL ACTIVITY INDICATOR AND TIMING

Consumer

The AM/PM output operates with a 68% duty cycle at full intensity that conducts to V_{SS} for PM indication.

If a "brown out" occurs, the AM/PM indicator will flash at a 1 Hz rate to signify an incorrect display time. This low power indication continues until proper power is restored and the clock is reset.

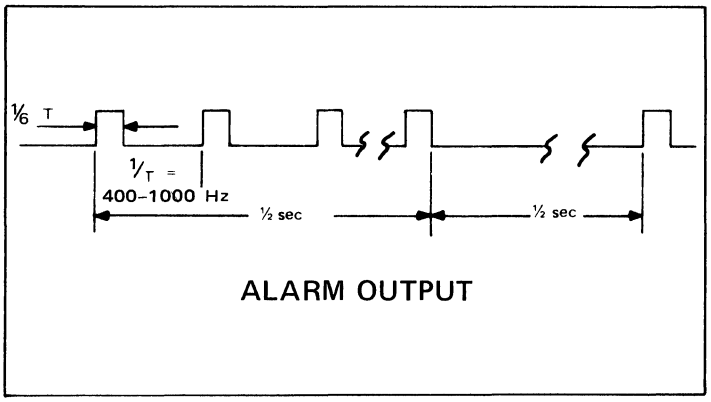
The 50 Hz/24 Hr. select pin is provided with an internal pull down resistor to V_{DD} and if left open will cause the clock to operate in the 12 hour mode requiring a 60 Hz input. If it is connected to V_{SS} it will operate in a 24 hour mode requiring a 50 Hz input.

The Alarm can operate in three modes according to the voltage on the wake select pin. The states are defined as:

Wake Select Input	Mode
V_{SS}	Radio and Tone
Open	Tone Only
V_{DD}	Radio Only

The Alarm Enable pin enables the alarm when connected to V_{SS}. If it is left open it will disable the alarm due to an internal pull down resistor to V_{DD}. When alarm occurs it may be disabled and immediately reenabled and will activate 24 hours later at the alarm time. The output tone will be in the range of 400-1000 Hz, and has a 1/6 duty cycle which conducts to V_{SS} 50% of the time at a 1 Hz rate.

The radio out pin, when activated by either the alarm or sleep function, will conduct to V_{SS}.



ALARM OUTPUT

When the radio tone mode is selected the radio out pin conducts to V_{SS} at alarm time. Three minutes later the tone output will be enabled. Both remain on until inhibited by the alarm enable control. Snooze will inhibit the alarm tone only.

The Snooze feature will temporarily turn off an activated alarm signal to allow an additional 10 minutes sleep. Momentarily connecting snooze to V_{SS} will activate the snooze. If left open an internal pull down resistor to V_{DD} will maintain the snooze feature inoperative.

The Sleep pin provides a means to turn the radio on for a specific period of time (10 minute increments to a maximum of 60 minutes). Adjustment of the time is accomplished by momentarily connecting the Sleep pin to V_{SS}. This causes the entire display to blink once for each 10 minutes of accumulated radio on time. This time may be reset and the radio turned off at any time by depressing the snooze button.

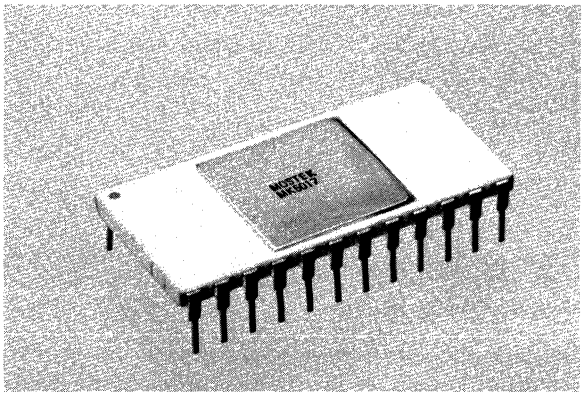
MOS Clock Circuit

MOSTEK

FEATURES

- ☐ 6-digit display
- ☐ 12/24 hour operation and display
- ☐ 50/60 Hz input
- ☐ Single power supply operation
- ☐ Easy to set
- ☐ Standard products available

Alarm Clock	MK 5017 P AA
Clock Radio Clock	MK 5017 P AN
Calendar Clock	MK 5017 P BB



SEGMENT IDENTIFICATION

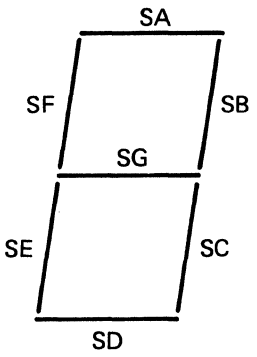


FIGURE 1

SEGMENT CODING

	SA	SB	SC	SD	SE	SF	SG
0	1	1	1	1	1	1	
1		1	1				
2	1	1		1	1		1
3	1	1	1	1			1
4		1	1			1	1
5	1		1	1		1	1
6	1		1	1	1	1	1
7	1	1	1				
8	1	1	1	1	1	1	1
9	1	1	1	1		1	1

DESCRIPTION

The MK 5017 P is a versatile MOS/LSI clock circuit manufactured by MOSTEK using its depletion-load, ion-implantation process and P Channel technology. Intended for a wide range of timing applications, all of these clock circuits may be used with either four or six digit displays. Operation from either a 50 Hz or 60 Hz input frequency may be selected. Another MOSTEK circuit (the MK 5009 P) is available to provide a 50 Hz signal from a 1 MHz crystal, where line frequency control is unavailable or inaccurate. A 50/60 Hz oscillator on the chip provides a temporary time base during momentary line frequency interruptions so that timekeeping can continue if a backup battery is provided to maintain V_{DD}.

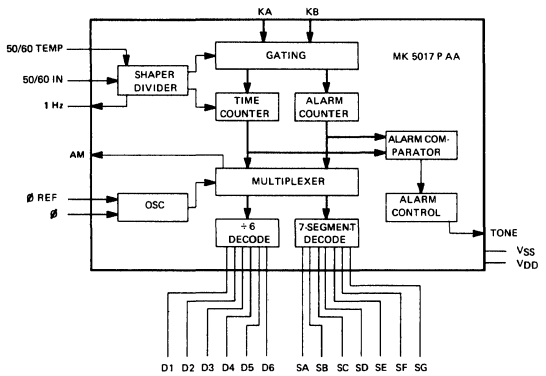
Only a single power supply is required for operation. All segments are turned on (pulled toward V_{SS}) causing an all "8's" display as a power failure indication when V_{DD} is below the operating range.

Data is multiplexed out of the clock in the form of six sequential seven-segment decoded digits. The segment coding is shown in figure 1.

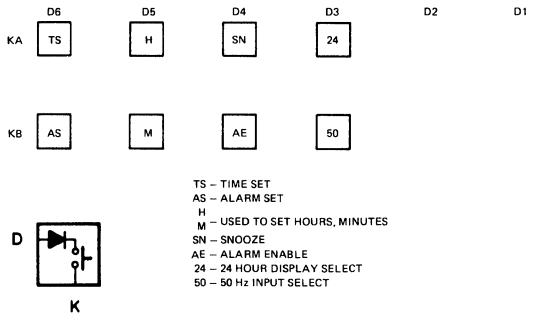
A scanning technique is employed to sense control switch closures in order to minimize input pin connections. Using this method only two pins, KA and KB, are required to sense up to 12 control switch closures.

Consumer

FUNCTIONAL DIAGRAM

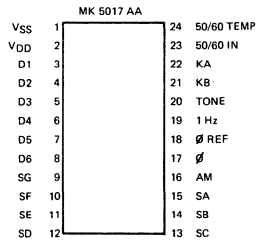


INPUT MATRIX



TS – TIME SET
AS – ALARM SET
H
M – USED TO SET HOURS, MINUTES
SN – SNOOZE
AE – ALARM ENABLE
24 – 24 HOUR DISPLAY SELECT
50 – 50 Hz INPUT SELECT

MOS/LSI DIGITAL ALARM CLOCK



FEATURES

- ☐ Alarm with 24 hour operation
- ☐ Alarm tone generated on-chip
- ☐ AM/PM indication
- ☐ Snooze
- ☐ 1 Hz output

DESCRIPTION

Time may be set in the Run mode while the clock circuit is counting or the clock may be set in the Time Set mode while the counters are stopped. Contents of the time counters is displayed in both the Time Set and Run modes. The clock is in the Time Set mode when the (TS) switch located at the intersection of the KA and D6 lines in the input matrix is closed. In the Time Set mode the time counters are stopped and the seconds and tens of seconds digits are reset to zero.

The clock is in the Run mode when both the (TS) and the Alarm Set (AS) switches are open. In the Run mode, counters less significant than the one being set continue counting.

Switches (M) and (H) in the input matrix are closed to cause individual digits to be incremented. The (M) switch causes the minutes digit to be incremented. The (H) switch causes the hours digits to be incremented. Closing both the (H) and (M) switches simultaneously causes the tens of minutes digit to be incremented. Incrementing of a selected digit occurs at a 2 Hz rate and with the exception of the tens of hours digit, digits more significant than the one being set will not increment.

In order to accurately set the time to the nearest second the clock should be placed in the Time Set mode. After setting the time ahead, the clock should then be returned to the Run mode at the proper time in order to start the clock.

The clock must be placed in the Alarm Set mode by closing the (AS) switch to set the alarm. In the Alarm Set mode the time counters continue timekeeping and the contents of the alarm counter is displayed. The alarm may be set to the nearest minute by manipulating the (H) and (M) switches in the same manner as when setting the time.

Both the time counters and the alarm counters have an AM/PM indication which allows the time and the alarm to be set on a 24 hour basis, rather than a 12 hour basis.

The Tone output occurs when coincidence between the alarm counters and the time counters is detected internally, if the alarm is enabled. The Tone output signal is a train of positive going pulses whose nominal frequency is equal to the frequency of the scan oscillator divided by 140

and modulated at a 1 Hz rate. For a scan rate oscillator frequency of 100 KHz the Tone output frequency is approximately 700 Hz. The duty cycle of the Tone output pulses is approximately 3%. This signal suitably buffered may be used to drive a speaker, eliminating the need for mechanical buzzers or external alarm oscillators. Unless the alarm is disabled, the Tone output lasts for one hour after coincidence is detected.

The alarm is enabled while the (AE) switch in the input matrix is closed. To disable the alarm the (AE) switch should be opened. After the alarm is disabled, it may be immediately enabled again in order to utilize the 24 hour capability.

The Snooze feature provides a temporary reset to allow "sleep over". When the (SN) switch is momentarily closed, the Tone output ceases for a period of seven minutes. After this period the Tone output becomes active again unless the alarm has been disabled. This temporary reset may be utilized repeatedly up to one hour.

Either a 12 or 24 hour display may be selected by the (24) switch located at the intersection of the D3 and KA lines in the input matrix. When the (24) switch is closed a 24 hour display sequence from 00:00:00 to 23:59:59 is selected. When the (24) switch is open or absent a 12 hour display mode is selected.

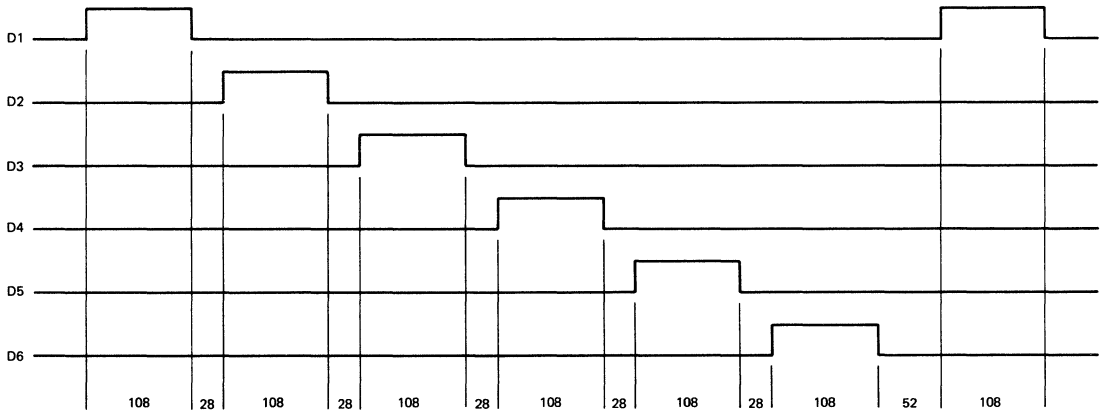
An AM output is provided to distinguish between AM and PM during 12 hour display. The AM output is at a logical one to indicate AM and is at a logical zero to indicate PM. This output switches logic levels every 12 hours in both 12 and 24 hour display modes.

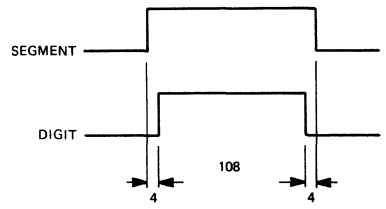
The (50) switch located at the intersection of the D3 and KB lines in the input matrix should be closed for operation from a 50 Hz reference frequency. The (50) switch should be omitted or left open for operation from a 60 Hz reference frequency.

A 1 Hz output is also provided as a time reference signal or it may be used to blink an indicator as an indication that the clock is counting, if the seconds and tens of seconds digits are not displayed. This 1 Hz output is modulated by digit strobe D4 to maintain constant relative intensity between the blinking indicator and the remainder of the display.

Six sequential digit strobes identify the segment information being presented. Figure 2 shows the digit strobe timing and the timing relationship between the digit and segment data.

DIGIT AND SEGMENT TIMING



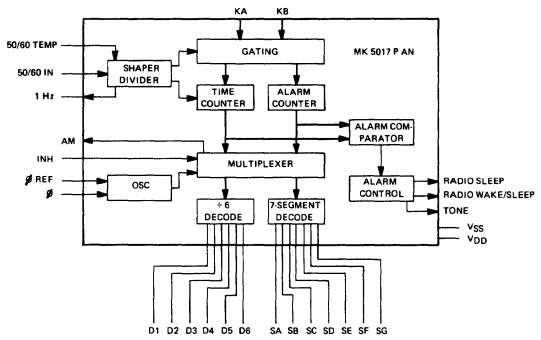


NOTES:

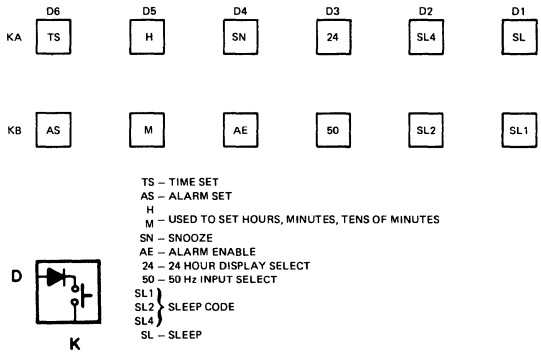
1. TIMES SHOWN ARE IN CLOCK PERIODS.

FIGURE 2

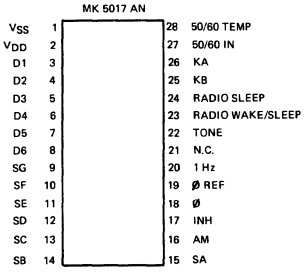
FUNCTIONAL DIAGRAM



INPUT MATRIX



MOS/LSI DIGITAL CLOCK WITH RADIO CONTROL



FEATURES

- ☐ Radio wake
- ☐ Radio sleep delay
- ☐ Snooze control
- ☐ Display inhibit
- ☐ Alarm with 24 hour operation
- ☐ Alarm tone generated on-chip
- ☐ AM/PM indication
- ☐ 1 Hz output

DESCRIPTION

Time may be set in the Run mode while the clock circuit is counting or the clock may be set in the Time Set mode while the counters are stopped. Contents of the time counters is displayed in both the Time Set and Run modes. The clock is in the Time Set mode when the (TS) switch located at the intersection of the KA and D6 lines in the input matrix is closed. In the Time Set mode the time counters are stopped and the seconds and tens of seconds digits are reset to zero.

The clock is in the Run mode when both the (TS) and the Alarm Set (AS) switches are open. In the Run mode, counters less significant than the one being set continue counting.

Switches (M) and (H) in the input matrix are closed to cause individual digits to be incremented. The (M) switch causes the minutes digit to be incremented. The (H) switch causes the hours digits to be incremented. Closing both the (H) and (M) switches simultaneously causes the tens of minutes digit to be incremented. Incrementing of a selected digit occurs at a 2 Hz rate and with the exception of the tens of hours digit, digits more significant than the one being set will not increment.

In order to accurately set the time to the nearest second the clock should be placed in the Time Set mode. After setting the time ahead, the clock should then be returned to the Run mode at the proper time in order to start the clock.

The clock must be placed in the Alarm Set mode by closing the (AS) switch to set the alarm. In the Alarm Set mode the time counters continue timekeeping and the contents of the alarm counter is displayed. The alarm may be set to the nearest minute by manipulating the (H) and (M) switches in the same manner as when setting the time.

Both the time counters and the alarm counters have an AM/Pm indication which allows the time and the alarm to be set on a 24 hour basis, rather than a 12 hour basis.

The Tone output occurs when coincidence between the alarm counters and the time counters is detected internally, if the alarm is enabled. The Tone output signal is a pulse train whose nominal frequency is equal to the frequency of the scan oscillator divided by 140 and modulated at a 1 Hz rate. For a scan rate oscillator frequency of 100 KHz the Tone output frequency is approximately 700 Hz. The duty cycle of the Tone output pulses is approximately 3%. This signal suitably buffered may be used to drive a speaker, eliminating the need for mechanical buzzers or external alarm oscillators. Unless the alarm is disabled, the Tone output lasts for one hour after coincidence is detected.

The alarm is enabled while the (AE) switch in the input matrix is closed. To disable the alarm the (AE) switch should be opened. After the alarm is disabled, it may be immediately enabled again in order to utilize the 24 hour capability.

The Snooze feature provides a temporary reset to allow "sleep over". When the (SN) switch is momentarily closed, the Tone output ceases for a period of seven minutes. After this period the Tone output becomes active again unless the alarm has been disabled. This temporary reset may be utilized repeatedly up to one hour.

Either a 12 or 24 hour display may be selected by the (24) switch located at the intersection of the D3 and KA lines in the input matrix. When the (24) switch is closed a 24 hour display sequence from 00:00:00 to 23:59:59 is selected. When the (24) switch is open or absent a 12 hour display mode is selected.

An AM output is provided to distinguish between AM and PM during 12 hour display. The AM output is at a logical one to indicate AM and is at a logical zero to indicate PM. This output switches logic levels every 12 hours in both 12 and 24 hour display modes.

The (50) switch located at the intersection of the D3 and KB lines in the input matrix should be closed for operation from a 50 Hz reference frequency. The (50) switch should be omitted or left open for operation from a 60 Hz reference frequency.

A 1 Hz output is also provided as a time reference signal or it may be used to blink an indicator as an indication that the clock is counting, if the seconds and tens of seconds digits are not displayed. This 1 Hz output is modulated by digit strobe D4 to maintain constant relative intensity between the blinking indicator and the remainder of the display.

Radio sleep time is selected by application of a binary code to the three sleep time select switches, SL1, SL2, and SL4. The sleep times that may be selected and the codes for selecting them are shown below.

RADIO SLEEP TIME TABLE

SLEEP TIME	SELECTION CODE		
	SL4	SL2	SL1
10 MIN	0	0	0
20 MIN	0	0	1
30 MIN	0	1	0
40 MIN	0	1	1
50 MIN	1	0	0
60 MIN	1	0	1
90 MIN	1	1	0
120 MIN	1	1	1

0 — AN OPEN SWITCH

1 — A CLOSED SWITCH

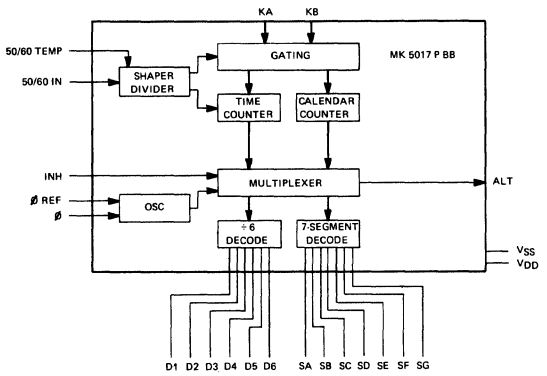
After selecting the desired time, the Sleep Switch (SL) is closed. This starts the proper interval and causes the RADIO SLEEP and RADIO WAKE/SLEEP outputs to switch to a logical zero. To terminate the count before the end of the sleep time, the SL switch is opened. If the SL switch is closed again, the selected sleep interval begins again.

The RADIO WAKE/SLEEP (RWS) output also switches toward V_{DD} whenever coincidence between the time and alarm counters is detected, if the Alarm Enable switch (AE) is closed. RWS remains at a logical zero for one hour after detection of coincidence and then switches to a logical one, toward V_{SS}.

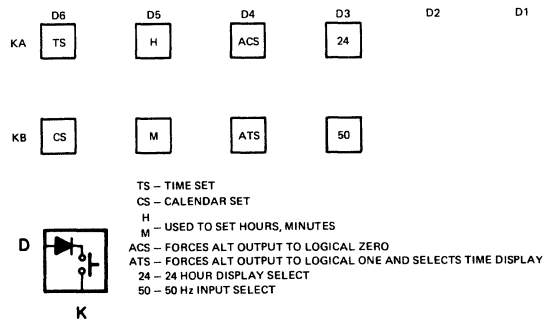
An inhibit input is provided to disable the digit and segment outputs so that they do not switch to V_{SS}. This input may be used to "wire or" multiple chips together. The output transistors are disabled when the INH input is connected to V_{SS}.

Six sequential digit strobes identify the segment information being presented. Figure 2 shows the digit strobe timing and the timing relationship between the digit and segment data.

FUNCTIONAL DIAGRAM

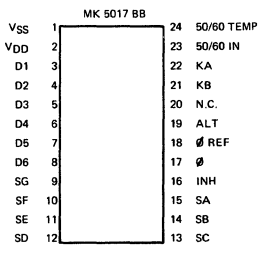


INPUT MATRIX



TS – TIME SET
CS – CALENDAR SET
H
M – USED TO SET HOURS, MINUTES
ACS – FORCES ALT OUTPUT TO LOGICAL ZERO
ATS – FORCES ALT OUTPUT TO LOGICAL ONE AND SELECTS TIME DISPLAY
24 – 24 HOUR DISPLAY SELECT
50 – 50 Hz INPUT SELECT

MOS/LSI DIGITAL CLOCK/CALENDAR



FEATURES

- ☐ Alternating time/calendar display
- ☐ Display inhibit

DESCRIPTION

Time may be set only in the Time Set mode. Contents of the time counter are displayed in the Time Set mode and the clock continues counting. The clock is in the Time Set mode when the (TS) switch, located at the intersection of the KA and D6 lines in the input matrix, is closed.

Switches (M) and (H) in the input matrix are closed to cause individual digits to be incremented. The (M) switch causes the minutes digit to be incremented. Closing the (H) switch causes the hours digit to be incremented. Closing the (H) and (M) switches simultaneously causes the tens of minutes digit to be incremented in the Time Set mode. Incrementing of a selected digit occurs at a 2 Hz rate. With the exception of the tens of hours digit, digits more significant than the one being set will not increment.

The clock must be placed in the Calendar Set mode by closing the (CS) switch in the input matrix to set the calendar. In the Calendar Set mode the contents of the calendar counter are displayed. When the (M) switch in the input matrix is closed in the Calendar Set mode, the days digit is incremented. Closing the (H) switch causes the months digit to be incremented. Closing both the (H) and (M) switches simultaneously has no effect in the Calendar Set mode. Incrementing of the digits being set occurs at a 2 Hz rate. Digits more significant than the one being set will increment.

When the day is changed during calendar setting, the time display resets to the AM portion of the day. Thus, the date continues to change at 12:00 A.M. instead of noon.

The clock is in the Run mode when both the (TS) and the calendar set (CS) switches are open. Neither the time counter nor the calendar counter can be set in the Run mode.

An inhibit input is provided to disable the digit and segment outputs so that they do not switch to V_{SS}. This input may be used to

"wire or" multiple clock circuit outputs together. A logical one on the inhibit input disables the outputs.

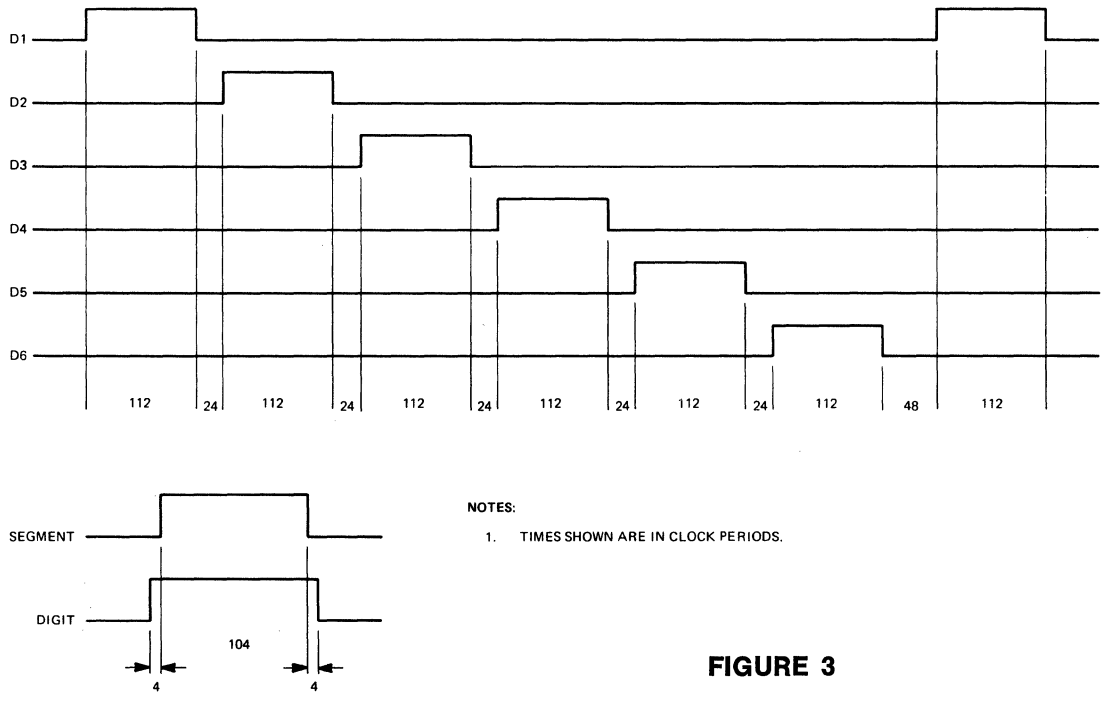
The ALT output indicates whether time or date is being displayed in the Run mode. Whie time is being displayed the ALT output is at a logical one. In either the Time Set or Calendar Set modes the ALT output continues alternating between a logical one and a logical zero. The ALT output is forced to remain at a logical one when the Alternate Time Set switch (ATS) is closed. Only time is displayed when the (ATS) switch is closed. When the Alternate Calendar Set switch (ACŞ) is closed, the ALT output is forced to remain at a logical zero.

In the Run mode the display alternates between the time display and the calendar display, displaying time for 8 seconds and calendar information for 2 seconds.

Closing the 50/60 Hz (50) switch located at the intersection of the D3 and KB lines in the input matrix allows a 50 Hz reference frequency to be used. When the (50) switch is open, a 60 Hz reference frequency should be used.

Six sequential digit strobes identify the segment information being presented. Figure 3 shows the digit strobe timing relationship between the digit and segment data.

DIGIT AND SEGMENT TIMING



NOTES:

1. TIMES SHOWN ARE IN CLOCK PERIODS.

FIGURE 3

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE
(All voltages relative to V_{SS})

Supply Voltage Range
- V_{DD} . . . . . +0.3 to −20 Volts

Input Voltage Range
- KA, KB . . . . . +0.3 to −20 Volts
- 1NH, 50/60 IN, TEMP, Ø . . . . . +0.3 to −20 Volts

Output Voltage Breakdown
- D1–D6, SA–SG, AM . . . . . −35 Volts
- 1 Hz, RS, RSW, TN, Ø Ref, ALT . . . . . −25 Volts

Operating Free-Air Temperature Range . . . . . 0°C to +70°C

Storage Temperature Range . . . . . −55°C to 150°C

RECOMMENDED OPERATING CONDITIONS
(0°C to +70°C—All voltages relative to V_{SS})

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Operating Voltages V_{DD}	−11.0		−18.0	Volts	
Input Logic Levels					
KA, KB					
"1" Logic Level	− 4.0		+ 0.3	Volts	
"0" Logic Level	V_{DD} +1.0		−35	Volts	
50/60 In, Temp, Ø					
"1" Logic Level	− 3.0		+ 0.3	Volts	
"0" Logic Level	V_{DD} +0.3		−20	Volts	
INH					
"1" Logic Level	− 1		+0.3	Volts	
"0" Logic Level	− 5		V_{DD}	Volts	
Scan Oscillator Frequency (using external driver)	25		100	KHz	

ELECTRICAL CHARACTERISTICS—5017 AA/AN/BB
($11V \leq V_{DD} \leq 18V$; $0°C \leq T_A \leq 70°C$)

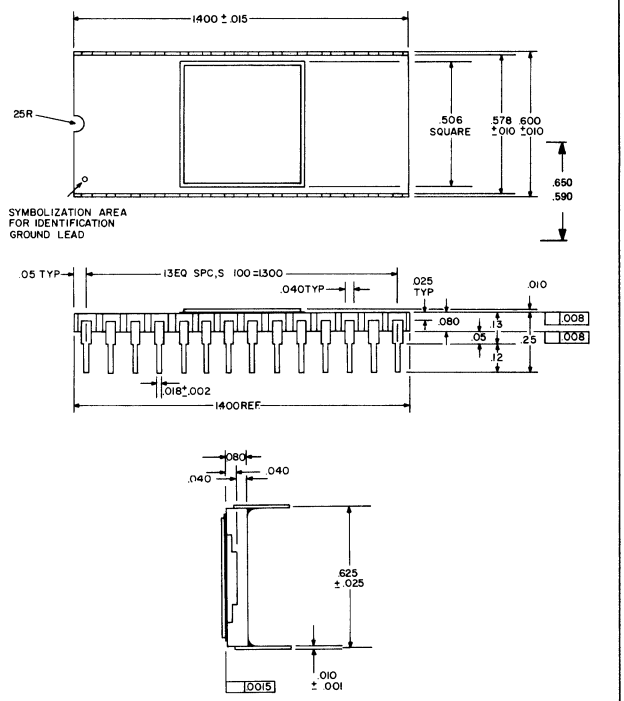
PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Output Current					
D1–D6, 1 Hz, ALT					
"1" Logic Level	8			mA	3
"0" Logic Level					2
SA–SG, AM					
"1" Logic Level	200			µA	4
"0" Logic Level					2
TN, RWS, RS					
"1" Logic Level	0.8			mA	5
"0" Logic Level	50			µA	6
Supply Current, I_{DD}		10	16	mA	
Leakage, D1–D6, SA–SG, AM			10	µA	7
Leakage, 1 Hz, ALT			10	µA	8
Scan Oscillator Frequency	60		210	KHz	1
Input Current, KA, KB			0.5	mA	9
Input Current, INH			1.0	mA	10

Note 1 RØ = 18K, CØ = 51PF, T_A = 25°C
Note 2 External Resistor Required
Note 3 Output voltage equal to V_{SS}−3.0V
Note 4 Output voltage equal to V_{SS}−0.5V
Note 5 Output voltage equal to V_{SS}−2.0V
Note 6 Output voltage equal to V_{DD}+4.0V
Note 7 $V_{DD} = V_{SS}$ = 0 volts, output voltage equal to −35 volts
Note 8 $V_{DD} = V_{SS}$ = 0 volts, output voltage equal to −20 volts
Note 9 Input voltage equal to V_{SS}−3.0V
Note 10 Input voltage equal to V_{SS}

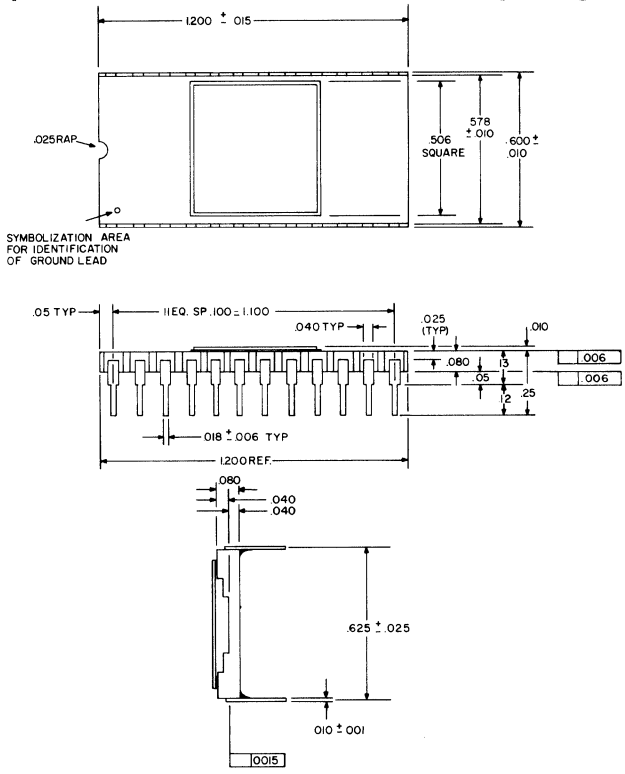
CLOCK CIRCUIT TYPES

PIN DESIGNATION	CLOCK CIRCUIT AA	AN	BB	FUNCTION
V_{SS}	X	X	X	Supply Voltage
V_{DD}	X	X	X	Supply Voltage
D1	X	X	X	Digit Strobe 1 Sec/Blank
D2	X	X	X	Digit Strobe, 10 Sec/Blank
D3	X	X	X	Digit Strobe, 1 Min/1 Day
D4	X	X	X	Digit Strobe, 10 Min/10 Day
D5	X	X	X	Digit Strobe, 1 Hr/1 Month
D6	X	X	X	Digit Strobe, 10 Hr/10 Month
SA	X	X	X	Segment A Data
SB	X	X	X	Segment B Data
SC	X	X	X	Segment C Data
SD	X	X	X	Segment D Data
SE	X	X	X	Segment E Data
SF	X	X	X	Segment F Data
SG	X	X	X	Segment G Data
Ø	X	X	X	Scan Oscillator Input
Ø Ref	X	X	X	Scan Oscillator Feedback
KA	X	X	X	Multiplexed Input
KB	X	X	X	Multiplexed Input
50/60 In	X	X	X	Input Count Frequency
50/60 Temp	X	X	X	Temporary Oscillator
AM	X	X		AM/PM Indication
1 Hz	X	X		Optional Output
Tone	X	X		Alarm Tone
INH		X	X	Inhibit
RS		X		Radio Sleep
RWS		X		Radio Wake/Sleep
ALT			X	Alternate

PHYSICAL DESCRIPTION
(28 lead ceramic dual-in-line hermetic package)



PHYSICAL DESCRIPTION
(24 lead ceramic dual-in-line hermetic package)



Consumer

MK 50240/1/2P
MK 50240/1/2N

MOS Top Octave Frequency Generator

MOSTEK®

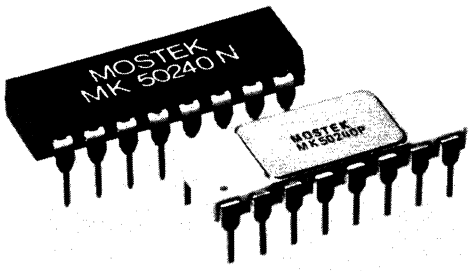
FEATURES

- ☐ Single Power supply
- ☐ Broad supply voltage operating range
- ☐ Low power dissipation
- ☐ High output drive capability

MK 50240 – 50% Output Duty Cycle

MK 50241 – 30% Output Duty Cycle

MK 50242 – 50% Output Duty Cycle



DESCRIPTION

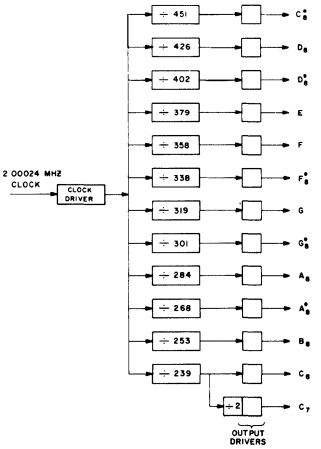
The MK 50240 is one of a family of ion-implanted, P-channel MOS, synchronous frequency dividers.

Each output frequency is related to the others by a multiple $12\sqrt{2}$ providing a full octave plus one note on the equal tempered scale.

Low threshold voltage enhancement-mode, as well as depletion mode devices, are fabricated on the same chip allowing the MK 50240 family to operate from a single, wide tolerance supply. Depletion-mode technology also allows the entire circuit to operate on less than 600 mW of power. The circuits are packaged in 16-pin ceramic dual-in-line packages.

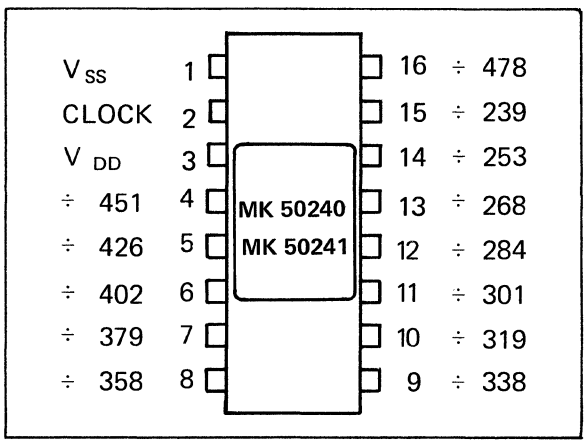
RFI emination and feed-through is minimized by placing the input clock between the V_{DD} and V_{SS} pins. Internally the layout of the chip isolates the output buffer circuitry from the divisor circuit clock lines. Also, the output buffers limit the minimum rise-time under no load conditions to reduce the R.F. harmonic content of each output signal.

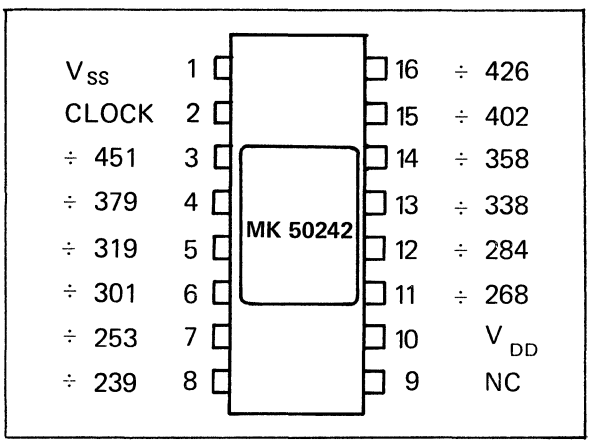
FUNCTIONAL DIAGRAM



Consumer

PIN CONNECTIONS





ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} ..... +0.3V to −20V

Operating Temperature (Ambient)..... 0°C to 50°C

Storage Temperature (Ambient)..... −40°C to 100°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leq T_A \leq 50°C$)

	PARAMETER	MIN	TYP	MAX	UNITS	FIGURE
V_{SS}	Supply Voltage	0		0	V	
V_{DD}	Supply Voltage	−11.0	−15.0	−16.0	V	

ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 50°C$; V_{SS} = 0, V_{DD} = −11 to −16V unless otherwise specified)

	PARAMETER	MIN	TYP	MAX	UNITS	FIGURE
V_{IL}	Input Clock, Low	0		−1.0	V	FIG. 1
V_{IH}	Input Clock, High	V_{DD} + 1.0		V_{DD}	V	
f_I	Input Clock Frequency	100	2000.240	2500	kHz	
t_r , t_f	Input Clock Rise & Fall Times 10% to 90% @ 2.5 MHz			30	nsec	FIG 1
t_{on} , t_{off}	Input Clock On and Off Times @ 2.5 MHz		200		nsec	FIG. 1
C_I	Input Capacitance		5	10	pF	
V_{OH}	Output, High @ .70 mA	V_{DD} + 1.5		V_{DD}	V	FIG. 2
V_{OL}	Output, Low @ .75 mA	V_{SS} − 1.0		V_{SS}	V	FIG. 2
t_{ro}, t_{fo}	Output Rise & Fall Times, 500 pF Load	250		2500	nsec	FIG. 3
t_{on}, t_{off}	Output Duty Cycle MK 50240P & MK 50242P MK 50241P (Pin 16 50%)		50 30		% %	
I_{DD}	Supply Current		24	37	mA	outputs unloaded

Consumer

FIGURE 1
INPUT CLOCK WAVEFORM

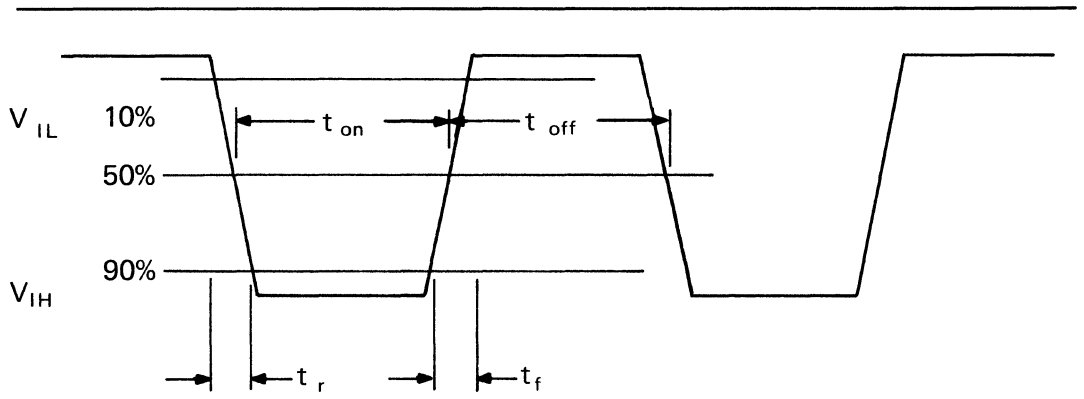
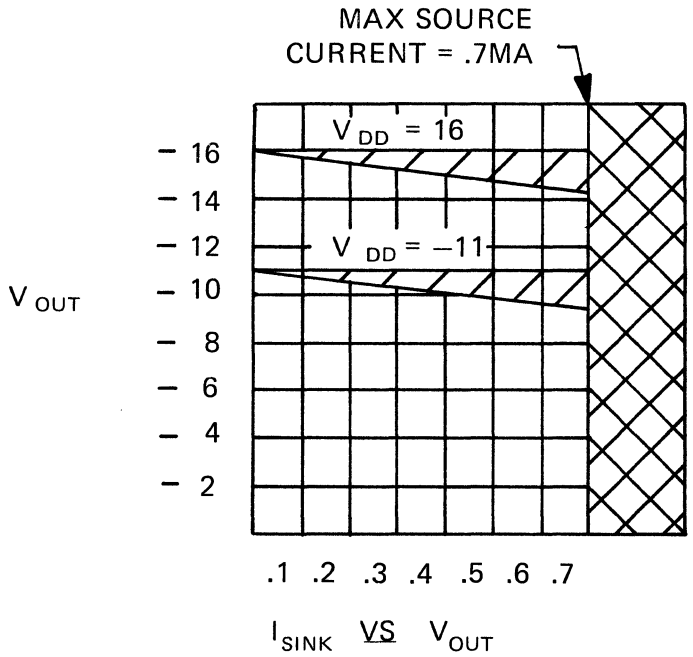
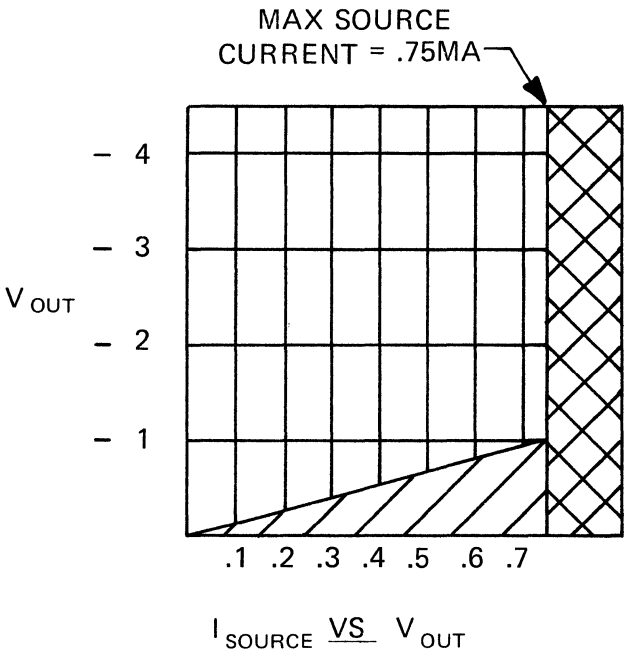


FIGURE 2
OUTPUT SIGNAL D. C. LOADING



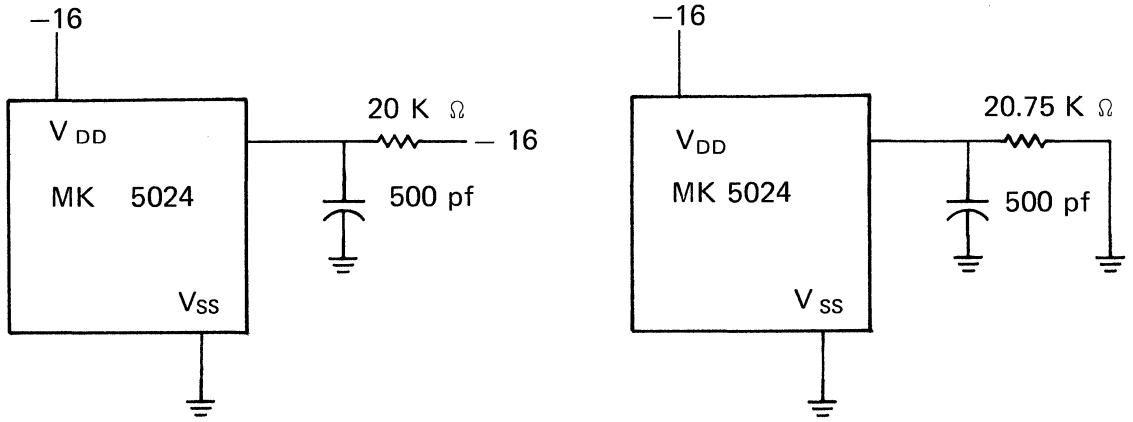


SINK CURRENT TO CHIP V_{DD} — (OPERATING AREA)

SINK CURRENT FROM CHIP V_{SS} — (CURRENT OVERLOAD AREA)

Consumer

FIGURE 3
OUTPUT LOADING

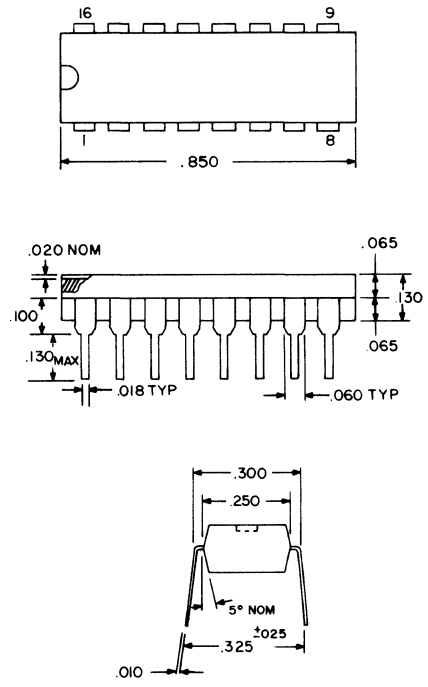


t_{fo} Test

t_{ro} Test

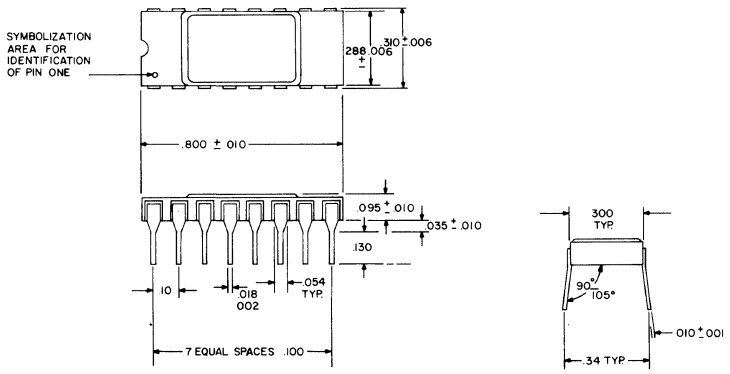
PHYSICAL DESCRIPTION

16–lead plastic dual-in-line hermetic package



Suffix N

16–lead side brazed ceramic dual-in-line hermetic package



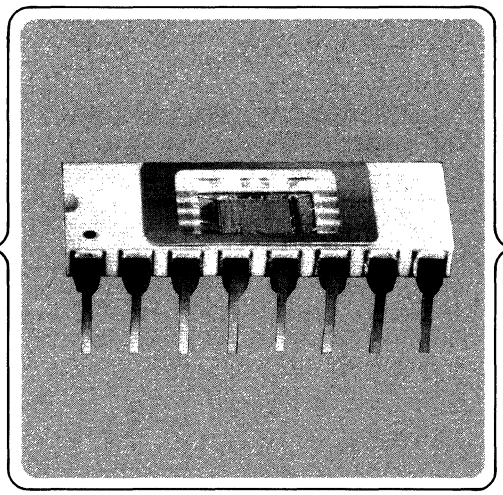
Suffix P

NOTE:

A. Pin 1 indicated by index dot
B. All dimensions in inches

Consumer

MOSTEK



Products to be Announced

MK 50010/1/2

FEATURES:

- ☐ Hours, Minutes — Date, Seconds
- ☐ 32,768 Hz quartz oscillator time base operation for both dynamic and field effect liquid crystals
- ☐ Build-in gated pulse-generator with sense-input for voltage conversion
- ☐ Microwatt power dissipation
- ☐ One-half to 1 sec delay in the updating commands for better human interaction
- ☐ Debounced update
- ☐ Single-pole grounding switches for display change and update
- ☐ Low - V_{DD} - sense that turns display off to avoid destruction of liquid crystal display
- ☐ Special synchronizing mode that enables user to synchronize the watch in a simple operation if error is less than 30 seconds
  Pinout matches most existing displays
- ☐ 64 Hz input to operate as decoder only

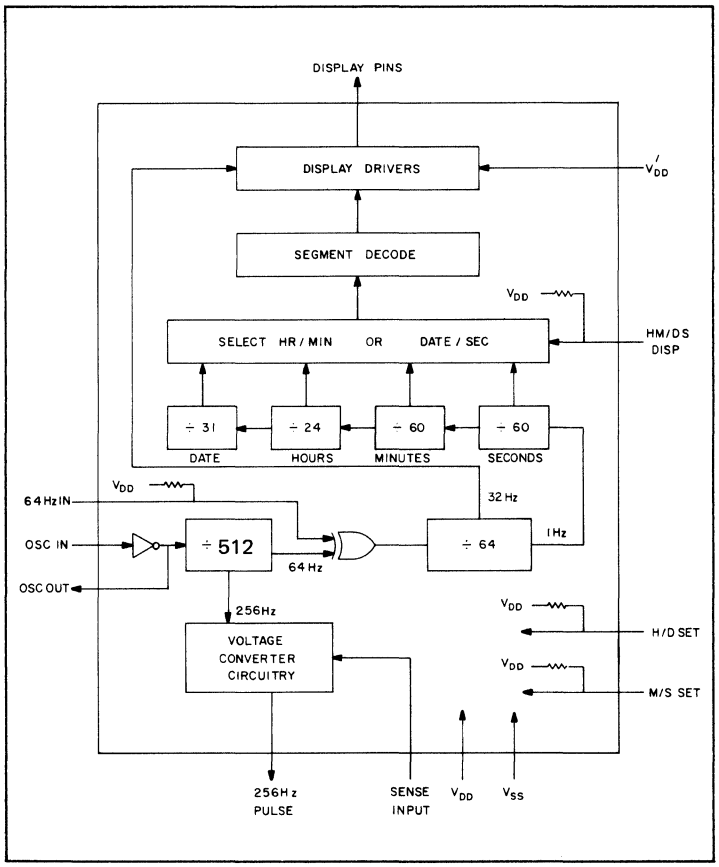
DESCRIPTION:

These three circuits are designed for a single chip CMOS watch/click with liquid crystal display.

MK 50010 — 4-digit, 12-hours with date and seconds
MK 50011 — 4-digit, 24 hours with date and seconds
MK 50012 — 3 1/2-digit, 12 hours with seconds

All versions display continously HRS on the left two or one-and-half digits and MIN on the right two digits. By pressing the display button, the types 50010 and 50011 will change the display to DATE on the left and SEC on the right, while version 50012 is blanked on the left and displays SEC on the right. The digits may be separated by a colon that blinks with a 1 Hz rate if the watch is running.

LIQUID CRYSTAL WATCH CIRCUIT



MOSTEK

MK 50075 RALU
MK 50100 ROM

DESCRIPTION:

- ☐ Modular Design allows function expansion by adding ROM
- ☐ Minimum set consists of RALU and one ROM
- ☐ ROM expansion up to 16 ROMs
- ☐ Programmable 14 digit display field for result, sign and special characters
- ☐ Seven segment display output
- ☐ Direct segment drive with current set capability
- ☐ Self-contained oscillator and timing.
- ☐ Requires no external components.
- ☐ 52 possible keys (scanned matrix
- ☐ 13 X 14), each key function is programmable

RALU processes BCD or HEX data

FEATURES:

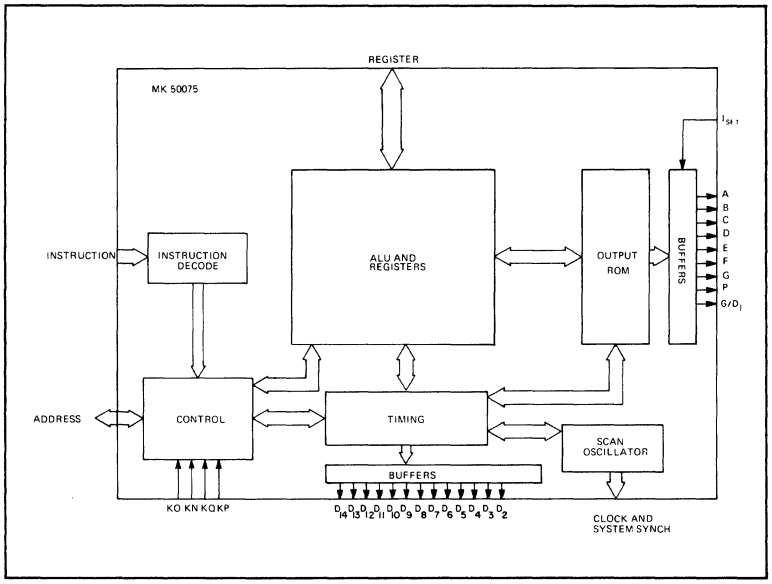
The MK 50075 RALU contains timing logic, arithmetic logic, four working registers, and control logic to perform instruction stored in the MK 50100 ROM(s).

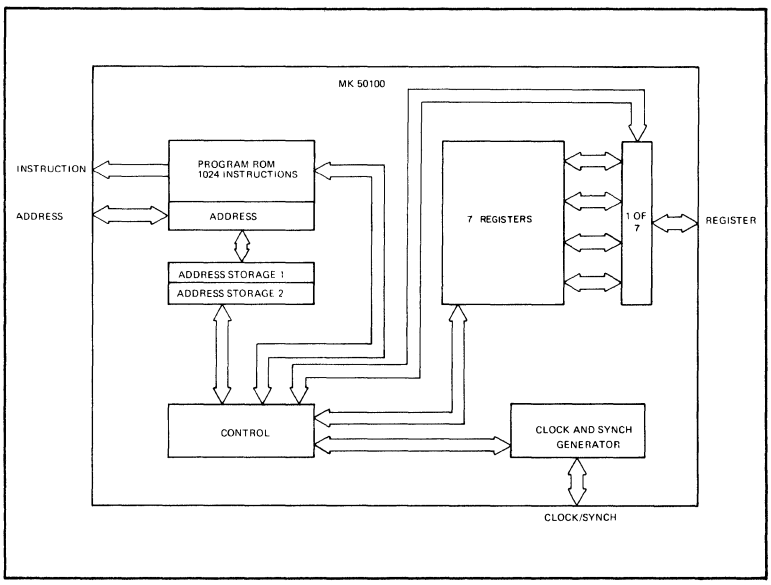
The MK 50100 ROM contains 1K words of instruction or data plus seven 15 digit registers of read/write storage. The maximum configuration is one RALU and 16 ROMs, resulting in a directly addressable 16K words of instruction or data and 112 registers of read/write storage.

Calculator functions are performed in ROM to cover a wide range of user requirements. The MK 50100 interfaces directly to the MK 50075 with no external components.

Low power dissipation, broad supply voltage range, a single power supply, direct segment drive, and an internal clock oscillator make the MK 50075, MK 50100 set ideal for battery operated, hand-held, multifunction calculators with low system costs.

12-DIGIT MOS CALCULATOR SET



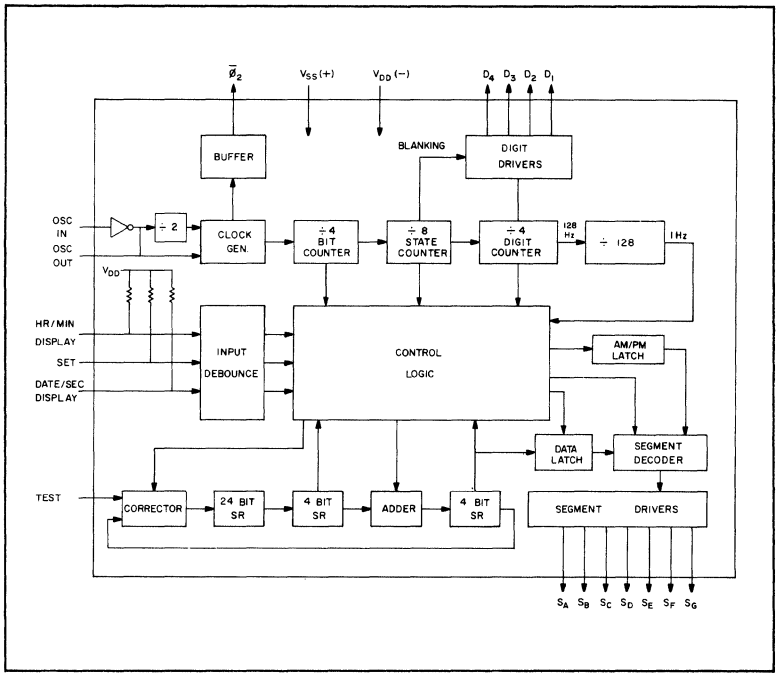


Products to be Announced

MOSTEK

MK 5030-5031

CMOS LED WATCH



DESCRIPTION:

- ☐ Hours, minutes, seconds, data
- ☐ Oscillator inverter for 32,768 Hz quartz crystal
- ☐ Direct segment drive
- ☐ Operation from 2.7 to 3.4 volts
- ☐ Microwatt power dissipation

FEATURES:

The MK 5030 and MK 5031 are single-chip, ion-implanted, metal gate CMOS circuits for multiplexed four-digit LED display watches. The MK 5030 is for 12-hour timekeeping and the MK 5031 for 24-hour timekeeping. On-chip pull up resistors and debounce circuitry allow the use of simple normally open "close-to-case" input switches. Two switches are used for commanding the display and in conjunction with a third switch for time setting. The setting of minutes does not distrub the hours; and the setting of hours does not disturb the date. Low resistance segment drivers eliminate the need for seven external bipolar transistors.

Products to be Announced

MOSTEK

MK 4096-6

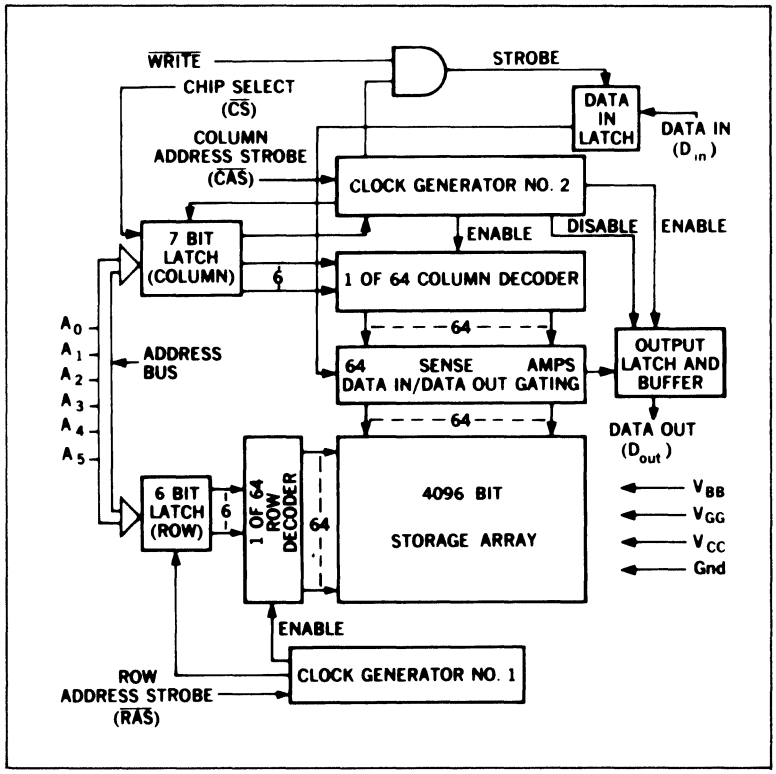
FEATURES:

- ☐ Access Time: 200 nsec
- ☐ Cycle Time: 350 nsec
- ☐ Pin-for-pin compatibility with the 16-pin MK 4096
- ☐ All inputs including clocks are TTL compatible with low capacitance of 8 picofarads
- ☐ Voltage pins are loacted on the corners to simplify PCB layout
- ☐ Output is TTL compatible, three-state
- ☐ Readily available automatic insertion equipment can be used in board assembly

DESCRIPTION:

The MK 4096 is a 4096x1 bit dynamic random access memory circuit. System oriented features include direct TTL compatibility and low capacitance at all inputs, three-state TTL compatible latched output that remains valid into the next cycle, and a chip select decoding time that does not have to add to the access time. A unique multiplexing and latching operation for the address inputs permits this circuit to be packaged in a standard 16-pin DIP on .3 inch centers.

4096-BIT RANDOM ACCESS MEMORY



MK 5085

DESCRIPTION:

- ☐ Uses 3.58 MHz crystal as frequency reference
- ☐ Better than 1% accuracy of standardized audio frequencies

Nominal frequencies:

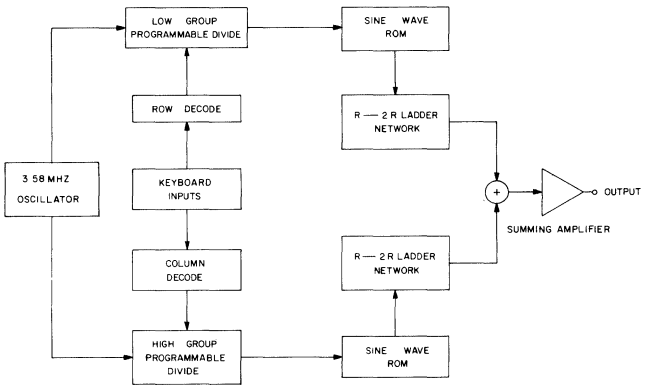
Low Group	High Group
697 Hz	1209 Hz
770 Hz	1336 Hz
852 Hz	1477 Hz
941 Hz	1633 Hz

- ☐ Uses CMOS processing for low power operation and high noise margins

FEATURES:

The MK 5085 generates dual-tone-multifrequency wafeforms of low harmonic distortion suitable for telephone signaling or other applications. It operates from telephone lines or fixed dc supply from 3 to 12 volts. This circuit is designed for economy in system applications as few external components are required.

TELEPHONE TONE GENERATOR



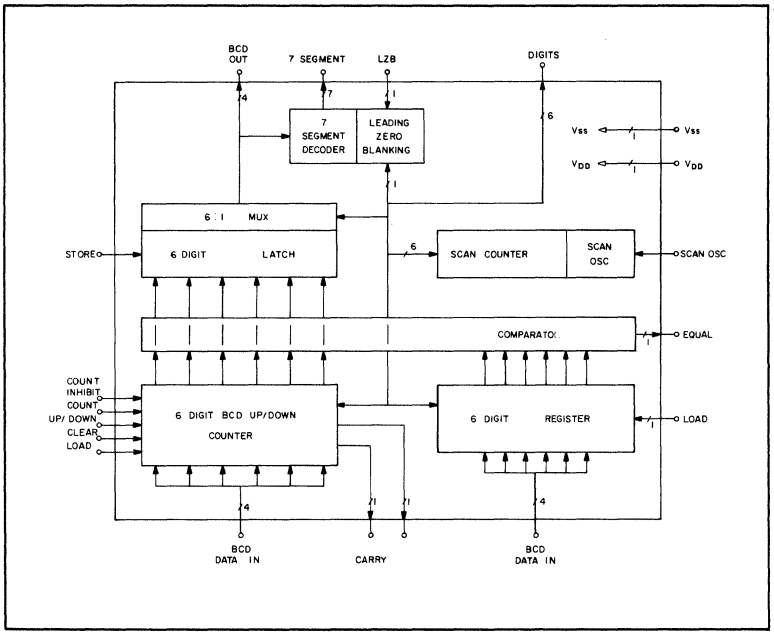
MOSTEK

MK 50395

FEATURES:

- ☐ Single power supply 12 to 18 volts
- ☐ Synchronous up/down counting
- ☐ Presetable compare register with comparator output
- ☐ Multiplexed BCD and seven-segment outputs
- ☐ Internal or external scan (to D.C.) for free choice of output frequency

6-BIT UP/DOWN COUNTER



DESCRIPTION:

The MK 50395 is an ion-implanted P-channel MOS six-decade synchronous up/down counter/display driver with compare register, latches and output multiplexer. The counter, as well as the register, can be loaded digit-by-digit with BCD data. The counter has asychronous clear and count inhibit functions. All six counter stages can be separately mask-programmed to divide by 10 (BCD), by 6 or by 12.

Scanning is controlled by the scan oscillator input which is self-oscillating or can be overdriven by an external signal. The six-digit register is constantly compared to the state of the up/down counter; and when both the register and the counter have the same contents, an equal signal is generated. A particular state of the counter can be latched into the 6-digit latch which is then multiplexed from MSD to LSD in BCD and 7 segment format to the output. The seven-segment decoder incorporates a leading zero blanking circuit which can be turned off by an external signal.

MOSTEK®

MOSTEK Corporation, 1215 West Crosby Road
Carrollton, Texas 75006, (214) 242-0444