MOSTEK 1983 COMPUTER PRODUCTS DATA BOOK

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PRINTED IN USA March 1983

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TECHNOLOGY

From its beginning, Mostek has been an innovator. From the developments of the 1K dynamic RAM and the single-chip calculator in 1970 to the current 64K dynamic RAM, Mostek technological breakthroughs have proved the benefits and cost-effectiveness of metal oxide semiconductors. Today, Mostek represents one of the industry's most productive bases of MOS/LSI technology, including Direct-Step-on-Wafer processing.

The addition of the Microelectronics Research Center in Colorado Springs adds a new dimension to Mostek circuit design capabilities. Using the latest computer-aided design techniques, center engineers are keeping ahead of the future with new technologies and processes.

QUALITY

The worth of a product is measured by how well it is designed, manufactured and tested, and by how well it works in your system.

In design, production and testing, the Mostek goal is meeting specifications the first time on every product. This goal requires a collective discipline from the company as well as individual efforts. Discipline, coupled with very personal pride, has enabled Mostek to build in quality at every level of production.

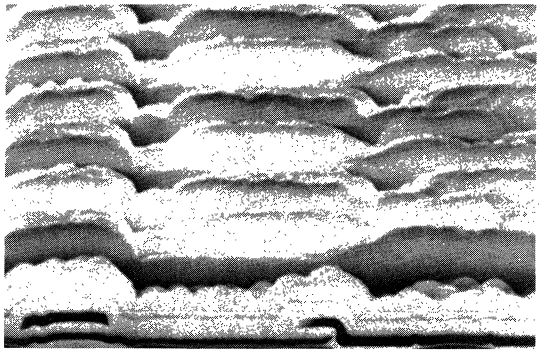
PRODUCTION CAPABILITY

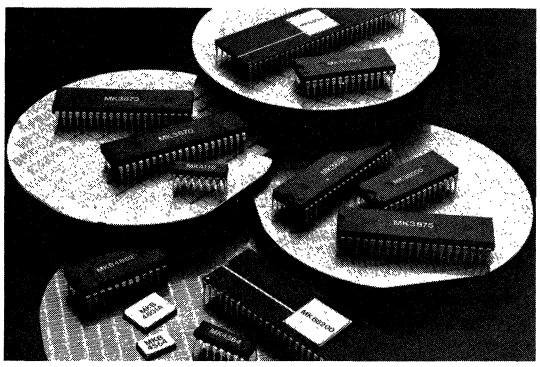
The commitment to increasing production capability has made Mostek one of the world's largest manufacturers of dynamic RAMs. Mostek capital expenditures as a percentage of sales are one of the highest in the industry, enabling us to provide high volumes of quality state-of-the-art products.

THE PRODUCTS

Memory Products

Through innovations in circuit design, wafer processing and production, Mostek has become one of the industry's leading suppliers of dynamic RAMs.





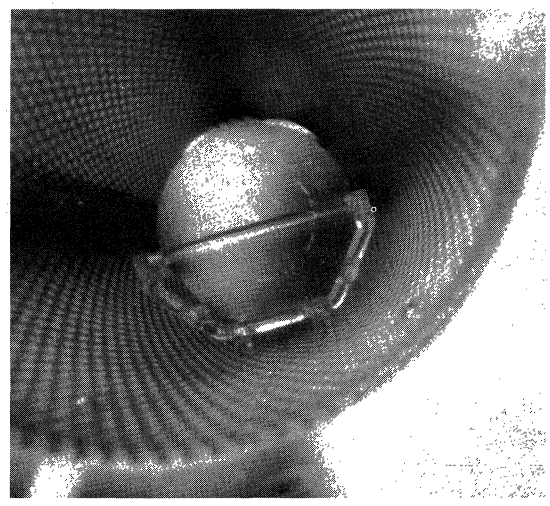
Examples of Mostek leadership are families of x1 and x8 high-performance static RAMs and our extremely successful 64K ROMs with more codes processed than any other mask-ROM in the industry. Another performance and density milestone is our 256K ROM, the MK38000.

Advanced circuit techniques and design used in our fast MK4564 64K dynamic RAM enhance manufacturability to satisfy the demands of a huge marketplace. This year Mostek introduced a new generation of 64K dynamic RAMs, operating at previously unheard-of speeds and breaking yet another barrier in VLSI technology.

Memory Systems

Taking full advantage of our leadership in memory components technology, Mostek offers a broad line of memory systems products, all with the performance and reliability to match our industry-standard circuits. Mostek offers add-in memory boards for popular DEC, Data General, and Perkin-Elmer minicomputers.

Mostek also offers general-purpose and custom memory boards for special applications.



Military Products

An extension of the high quality in fabrication and design inherent in Mostek's product line allows many of our ICs to be made available screened to MIL-STD-883. In addition, select parts are qualified to the rigors of MIL-M-38510 and are processed on our QPL certified lines.

The MKB product line begins with the complete memory products offering, and extends into microprocessors and gate arrays. Leadless Chip Carrier (LCC) packaging and prepared customer SCDs address the particular needs of the military community.

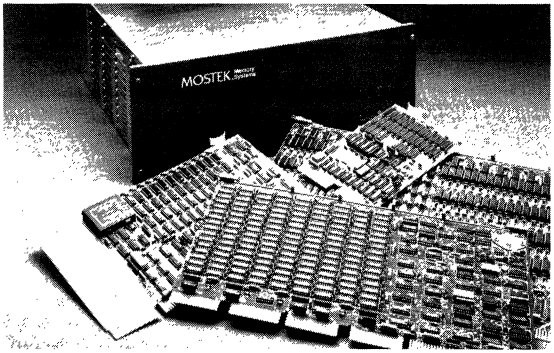
Telecommunications Products

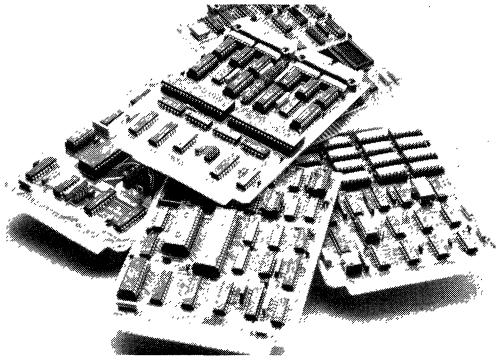
Mostek is a leading supplier of tone dialers, pulse dialers and CODEC devices. As each new generation of telecommunications systems emerges, Mostek is ready with new generation components, including PCM filters, tone decoders, repertory dialers, new integrated tone dialers, and pulse dialers.

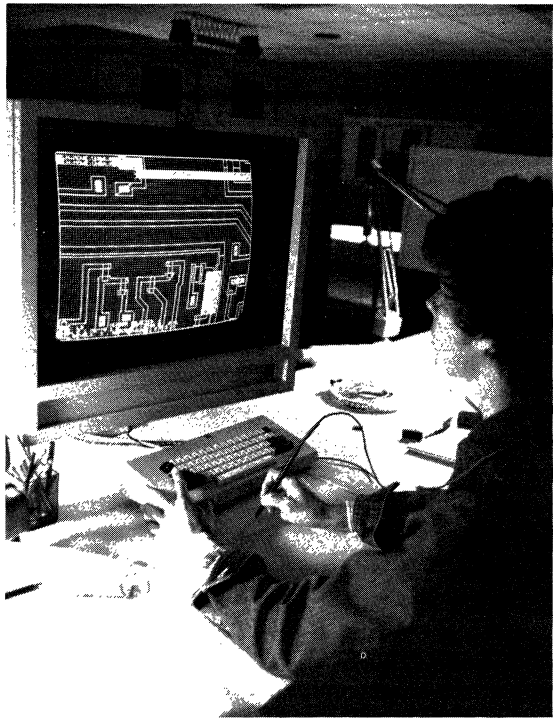
These products, many of them using CMOS technology, represent the most modern advancements in telecommunications component design.

Industrial Products

Mostek's line of Industrial Products offers a high degree of versatility per device. This family of components includes various microprocessor-compatible A/D converters,







a counter/time-base circuit for the division of clock signals, and combined counter/display decoders. A low parts count provides an economical alternative to discrete logic systems.

Microcomputer Components

Mostek's microcomputer components cover the entire spectrum of microcomputer applications.

Our MK68000 16-bit microprocessor family is designed for high-performance, memory-intensive systems.

Our Z80 is today's industry-standard 8-bit microprocessor. The Mostek 3870 family of single-chip microcomputers offers upgrade options in ROM, RAM and I/O—all in the same socket. The MK38P70 EPROM piggyback microcomputer emulates the entire family and is ideal for low-volume applications.

Development systems include the RADIUS™ remote development station that lets you use your host minicomputer to develop the applications software. The program is then downloaded into the RADIUS which then lets you perform real-time in-circuit emulation and debug. The Mostek MATRIX™ Development System is a stand-alone hardware and software debug and integration system.

Microcomputer Systems

Mostek is the world's leading manufacturer of Z80-based STD BUS system components. This year Mostek introduced a new line of microsystems using the VMEbus and based on the MK68000.

Computer systems include our MATRIX line, which uses STD BUS cards to let you custom-design your own system.

Semicustom Circuits

Using the technology developed by Mostek and United Technologies' Microelectronics Research Center, Mostek is the leader in semicustom circuit design. The Mostek HIGHLAND℠ Design System is one of the most user-friendly, highly-automated, state-of-the-art semicustom circuit development tools in the industry. Mostek combines this highly-developed CAD system with high-volume CMOS production capability, enabling us to offer you quality gate arrays at a low cost.

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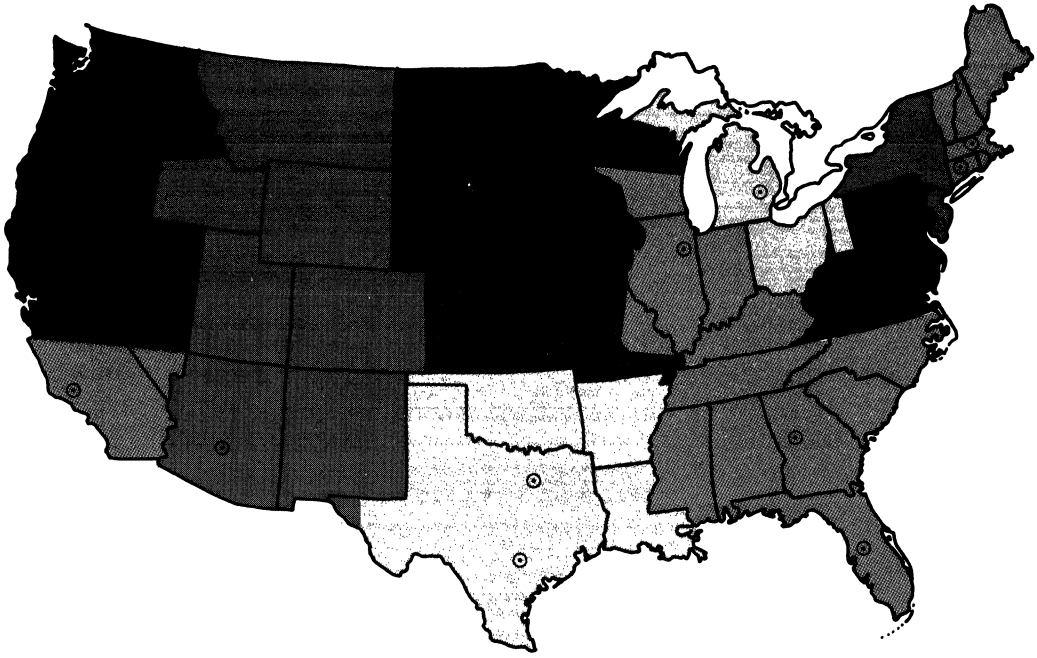

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III VMEbus

PRELIMINARY

VME-SBC

FEATURES

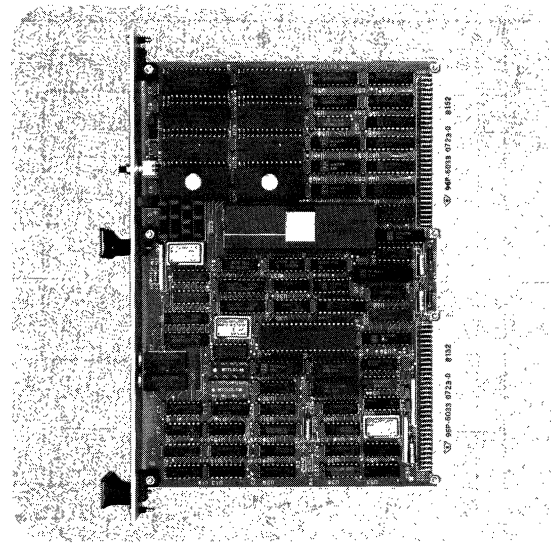
The SBC board serves as a stand alone module or as the System Controller/Master (slot 1 type CPU) on the VMEbus. It contains the following features:

- ☐ VMEbus Master/Slave
- ☐ CPU MK68000 (8 MHz to 12 MHz)
- ☐ Eight BYTEWYDE Sockets
  - 2 EPROM/ROM dedicated
  - 2 RAM dedicated
  - 4 option EPROM/ROM or RAM
- ☐ Provides VMEbus utilities
  - Power and Pushbutton Reset
  - System 16 MHz clock
  - Programmable Bus-Time-Out
  - 1 Level Arbiter utilizing the CPU's BR*, BG*, and BGACK* lines
- ☐ CSR Register
- ☐ Selection Switches (With Remote Capability)
- ☐ Interrupt Handler
- ☐ Two Timer/Counters
- ☐ Serial I/O (D.C.E.)
  - One channel modified RS-232
  - Asynchronous only (to 19.2K Baud)
  - Receive Data, Transmit Data, RTS, CTS, DTR, DSR, and DCD
- ☐ On Board Vectored Interrupts
- ☐ Self-Test LED

VME SYSTEM DESCRIPTION

The VMEbus was designed jointly by Mostek, Motorola, and Signetics, and was introduced in October, 1981. It offers an attractive combination of high performance timing parameters, compact form factor, and the advanced functional capability appropriate for today's applications of 16-bit microprocessors such as the MK68000. With features such as expansion to 32-bit address and data, an independent serial communications bus, and open-ended transaction coding, it provides for tomorrow's applications as well, assuring the user of a compatible upward growth path for years to come. The international-standard compact board size promotes functional modularity and low board cost, and allows the user to select only those functions needed for his application.

VME-SBC
Figure 1



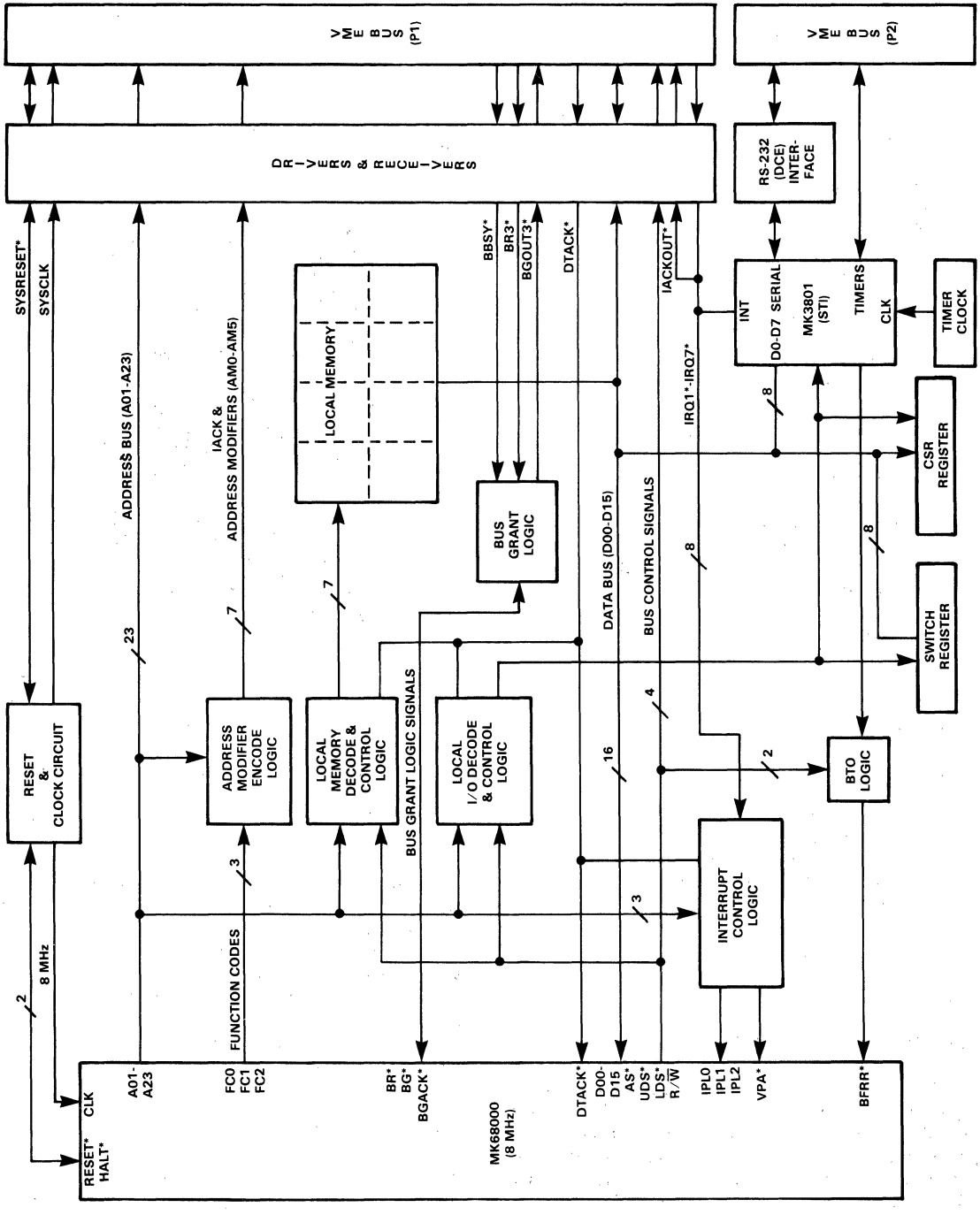
Mostek's VME board product line provides an ever-expanding family of powerful general-purpose modules, applicable to a wide variety of systems and applications including data, word, and image processing, communications, industrial automation and robotics, data acquisition, and software development. For specialized functions provided by other vendors or by the user, Mostek VME boards are totally compatible with the VMEbus specification, ensuring fully functional operation with all other VMEbus compatible modules.

VME-SBC DESCRIPTION

The Mostek VME-SBC, based on the powerful 68000 microprocessor, features eight 28-pin memory sockets which enable the user to populate the module with any

SBC BLOCK DIAGRAM

Figure 2



combination of designated ROM, RAM, and EPROM devices.

Flexible address decoding allows the user to configure each memory device within any 4K byte boundary of the 16M byte addressing space. The user can choose one of the two preselected memory configurations or, by programming a decoder PAL, may assign any of the eight sockets to any address range. In addition, a memory controller PAL is utilized to accommodate different speed memory devices, taking advantage of fast RAM access times.

The on-board I/O includes a Mostek Serial/Timer/Interrupt chip (STI, MK3801) which provides an RS-232C serial channel, two counter/timer channels, programmable Baud rate, and programmable bus time out. In addition, the VME-SBC contains an 8-bit switch input register and a Command Status Register (CSR). The CSR register allows software control of the following: STI interrupt level (1-7), Bus-Time-Out status, Self Test LED control (RED/GREEN), and Individual interrupt enable bits (1-7).

MEMORY SOCKET POPULATION

The VME-SBC is offered in two memory configurations. MK75601-X-01 is populated with two 2764's (16Kb EPROM) containing a software debugger monitor (MON68K), and six 6116's (12Kb RAM). MK75601-X-02 is populated with two 6116's (4Kb RAM) and the remaining sockets are configured for but not populated to accommodate six 2764's, allowing the user 48Kb of EPROM. The memory socket population is shown in Figure 3.

The memory access time of the on-board RAM and EPROM required by the VME-SBC is determined by the processor speed. Refer to Figure 4 to determine the memory speed requirements:

MK75601-X-01 SOCKET POPULATION (2-2764s 6-6116s)

Figure 3

MEMORY DEVICE	EVEN BYTE #	ODD BYTE #	ASSOC JUMPER
2764 (EPROM)	U09	U24	J3
6116 (RAM)	U10	U25	J2
6116 (RAM)	U11	U26	J1
6116 (RAM)	U12	U27	J4

MK75601-X-02 SOCKET POPULATION (6-2764s 2-6116s)

MEMORY DEVICE	EVEN BYTE #	ODD BYTE #	ASSOC JUMPER
2764 (EPROM)	U09	U24	J3
6116 (RAM)	U10	U25	J2
2764 (EPROM)	U11	U26	J1
2764 (EPROM)	U12	U27	J4

MEMORY SPEED REQUIREMENTS

Figure 4

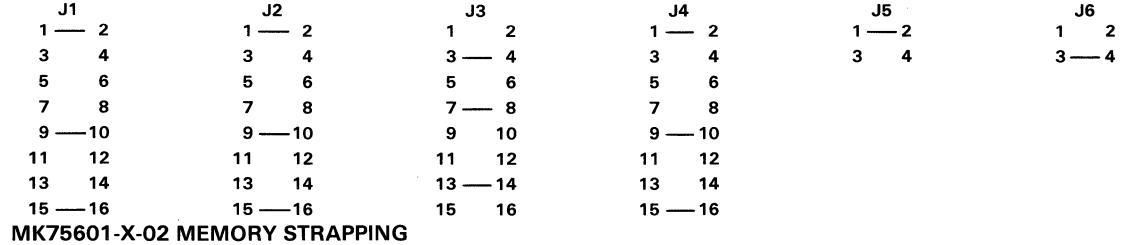
VME-SBC MK #	EPROM ACCESS TIME Min (nsec)	RAM ACCESS TIME Min (nsec)
MK75601-8-01	300	150
MK75601-8-02	300	150
MK75601-10-01	250	150
MK75601-10-02	250	150
MK75601-12-01	200	120
MK75601-12-02	200	120

MEMORY CONFIGURATION STRAPS

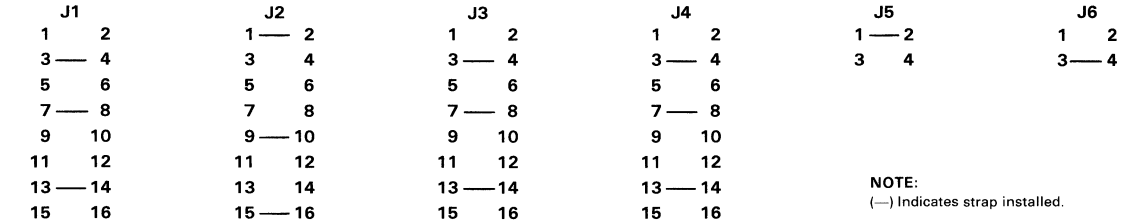
The memory configurating straps are installed at shipment. Each configuration is shown in Figure 5.

MK75601-X-01 MEMORY STRAPPING (2-2764s 6-6116s)

Figure 5



MK75601-X-02 MEMORY STRAPPING (6-2764s 2-6116s)



NOTE:
(—) Indicates strap installed.

I/O Adapter

The VME-SBC provides the RS-232C, Timer/Control, Remote Reset, and Remote Selection inputs on the P2 connector. In order to interface to the I/O connector, one must construct either a custom cable or purchase an I/O adapter MK75901, which allows use of a standard RS-232C cable. The I/O adapter contains four DB-25 connectors where one is dedicated for the serial interface and the second for remoting the selection switch, timer inputs/outputs, and Reset. The other two DB-25's are unused. The I/O adapter also contains jumper blocks to allow timer "chaining" and Baud rate measurement. Appendix A contains the connections needed to interface P2 to EIA RS-232C and Appendix B contains the P2 pinout.

Baud Rate Measurement Strap

When using the Mostek debugger monitor (MON68K), it is necessary to strap P2-A3 to P2-A4. This strapping arrangement routes the serial in data to a timer input of the STI (Serial Timer Interface) to allow Baud rate measurement.

External Push Button Reset Option

The VME-SBC provides an input on P2-A18 for a remote reset switch, so that the system can be reset from either the on-board push button or an external one.

Remote Selection Switches

The two selection switches located on the SBC provide eight bits of information that can be read by the CPU. The switch inputs (S7-S0) are routed to P2 to allow inputs other than from the on-board switches. To use external inputs, one must set the on-board switches to a value of FF. Refer to Appendix B to determine the P2 locations of the inputs.

Parallel Output Bit

The STI (Serial Timer Interface), bit I7 is buffered as an output and routed to P2-A17.

Timer Input/Output Bits

The SBC provides four counter/timers via the STI. Two of the timers (TA0 and TB0), provide full service features including delay timer operation, event counter operation, pulse width measurement and pulse generation. The other two timers (TC0 and TD0) provide delay timer operation only, and are used for programmable bus time out and Baud rate generation, respectively. Timers TA0 and TB0, however, are for user use and have their outputs and inputs routed to P2. These locations can be found in the P2 pinout table in Appendix B. The bus time out clock is routed to P2-A6 to allow chaining this timer to either Timer A or B to increase the maximum time out of Timer A or B. When using this feature, one must realize that the bus time out clock still retains its function of bus time out.

ARBITRATION

The VME-SBC provides a one level arbiter on Bus Request Level 3 utilizing the CPU's BR*, BG*, and BGACK* pins. The SBC will not acknowledge requests on any other levels.

MEMORY MAP

The VME-SBC MK75601-X-01 has 16Kb of EPROM (2764's) containing the software debugger monitor (MON68K) and 12Kb of RAM. In addition it contains a 16-bit CSR (Command Status Register), an 8-bit selection switch register, and a Mostek STI. The local memory map is shown in Figure 6.

The VME-SBC MK75601-X-02 can be populated to have 48Kb of EPROM (2764's) containing user firmware and 4Kb of RAM. Similar to the VME-SBC MK75601-X-01, it contains a 16-bit CSR and an STI. It has a local memory map as shown in Figure 7.

Application Note #4420XXX provides necessary information if the pre-configured memory map needs to be changed to meet a particular application.

VME-SBC MK75601-X-01 MEMORY MAP
Figure 6

DEVICE	ADDRESS	SUP/USER	WORD/BYTE
RAM (U10,25)	000000 - 000FFF	SUP	WORD OR BYTE
RAM (U11,26)	001000 - 001FFF	SUP/USER	WORD OR BYTE
RAM (U12,27)	002000 - 002FFF	SUP/USER	WORD OR BYTE
EPROM (U9,24)	FEC000 - FEFFFF	SUP	WORD OR BYTE
SWITCHES	FFF801	SUP	BYTE ONLY
CSR	FFF802 - FF803	SUP	WORD OR BYTE
STI (U34)	FFF821 - FFF83F	SUP	BYTE ONLY

VME-SBC MK75601-X-02 MEMORY MAP

Figure 7

DEVICE	ADDRESS	SUP/USER	WORD/BYTE
RAM (U10,25)	000000 - 000FFF	SUP	WORD OR BYTE
EPROM (U11,26)	FE4000 - FE7FFF	SUP	WORD OR BYTE
EPROM (U12,27)	FE8000 - FEBFFF	SUP	WORD OR BYTE
EPROM (U9,24)	FEC000 - FEFFFF	SUP	WORD OR BYTE
SWITCHES	FFF801	SUP	BYTE ONLY
CSR	FFF802 - FFF803	SUP	WORD OR BYTE
STI (U34)	FFF821 - FFF83F	SUP	BYTE ONLY

III

RESET VECTOR LOCATION

The MK68000 reserves the first 1Kb of memory starting at address 000000H for the exception vectors, including the power-on reset vector and initial supervisor stack pointer. The VME-SBC contains logic that enables the EPROM to provide the processor with the reset vector and supervisor stack pointer upon either push button reset or system power up. The power up vectors are located at address FEC000-FEC007 on the MK75601-X-01 version and at FE4000-FE4007 on the MK75601-X-02 version. The user SHOULD BE AWARE that when a write access to RAM addresses 000000-000007 is made, a bus error will result because the on-board logic will interpret this cycle as a write operation to the EPROM.

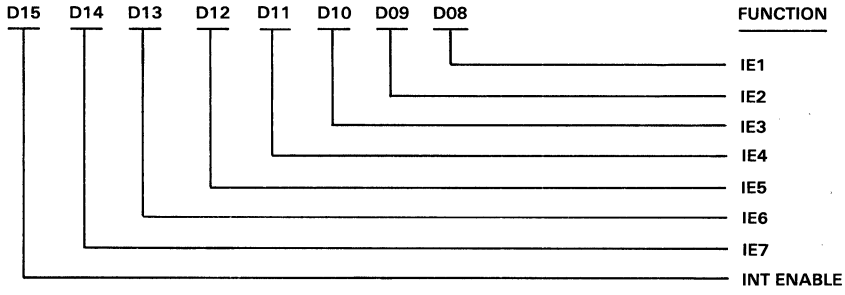
A PROM is used to implement the logic that determines if the exception vector is fetched from RAM or EPROM. The Application Note referenced describes how to program this PROM to allow exception vectors in addition to Reset to reside in EPROM.

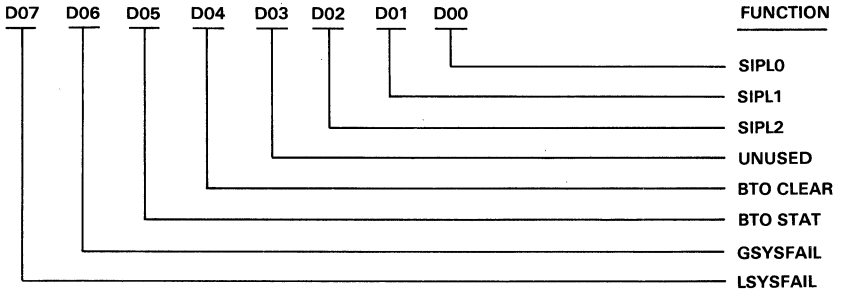
COMMAND STATUS REGISTER

The CSR has a fixed address of FFF802 and can only be addressed locally in the Supervisor State. The register is initialled to 00H on reset and is a Read-Write Register. The bit definitions are defined in Figure 8.

BIT DEFINITIONS

Figure 8





D15 Interrupt Enable

The interrupt enable bit controls all interrupt requests for the VMEbus and on-board devices, including SYSFAIL* and ACFAIL*. The power up condition is all interrupts disabled. Setting this bit to a "1" allows all enabled interrupts.

D08-D14 Interrupt Enable Bits

If Interrupt Enable (D15 = 1) is on, setting these bits to a "1" enables the specified interrupt level. The ACFAIL* (Level 7 Autovector) and SYSFAIL* (Level 6 Autovector) interrupts are enabled whenever the INT ENABLE bit is set (D15).

D07 Local SYSFAIL

This bit controls the board's contribution to the VME SYSFAIL* signal and the state of the red/green LED. When set to 1, the SYSFAIL* signal is not driven and the LED is green. When cleared, the SYSFAIL* signal is asserted and the LED is red.

D06 Global SYSFAIL

This is a read only bit and reflects the status of the VMEbus SYSFAIL* signal. A low-going edge on SYSFAIL*, subsequent to RESET, also causes a level 6 autovector. A "0" indicates a system fail condition.

D05 BTO Status

The BTO (Bus Time Out) status bit is set when the on-board BTO logic detects a BTO and asserts BERR*. It is cleared by writing a 1 to the BTO CLEAR bit (D04).

D04 BTO Clear

Writing a "1" to the bit clears the BTO status bit. This bit will always be "0" when it is read.

D00-D02 STI Interrupt Priority

The interrupt priority bits sets the priority of the STI. This allows programming the interrupt level from 0 to 7. The power-up reset level is 000 which disables STI interrupts. 111 equals a level of 7.

SELECTION SWITCH REGISTER

The VME-SBC contains an 8-bit switch input register to accommodate two 4-bit switches. This register has a local address of FFF801 (Byte Register) and is read only in the Supervisor State. The register inputs are also routed to P2 to allow remote selection switches. The location of the P2 register inputs can be found in Appendix B.

Baud Rates

Baud rates on the SBC are fully programmable and are generated by the Timer D output of the STI. Table 1 contains the Timer D data register values for the various Baud rates. Refer to Appendix C for a software example that sets the Baud rate. Timer D should be programmed to a prescaler of divide by 4.

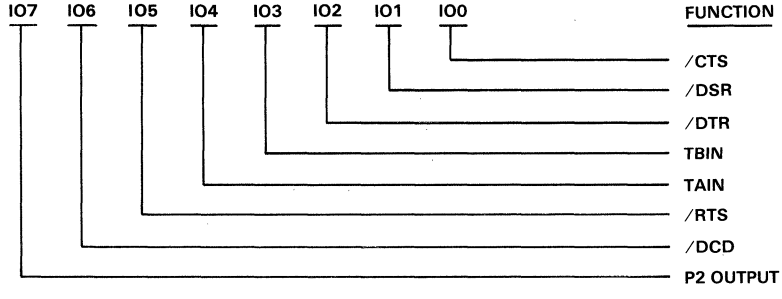
BAUD RATE SELECTION
(TIMER D PRESCALER = DIVIDE BY 4)
Table 1

TIMER D DATA REGISTER HEX VALUE (TDDR)	BAUD RATE (x16)
$AE	110
$40	300
$20	600
$10	1200
$08	2400
$04	4800
$02	9600
$01	19200

RS-232C Control Signals

The STI parallel input/outputs are used to implement the RS-232C control signals. Appendix C contains a software example which will aid in programming the control bits.

STI PARALLEL INPUT/OUTPUT DEFINITIONS
Figure 9



STI (MK3801) Operation

The Mostek MK3801 (STI) internal registers are available to the programmer starting at hex address FFF820 as shown in Appendix C, which contains a simple software driver. For specific programming of these registers, refer to the MK3801 Technical Manual.

PROGRAMMABLE BUS-TIME-OUT

The STI Timer C output is used to provide the bus time out clock. The first positive clock is used to sample the state of the data strobes. If either data strobe is sampled low for two clock periods, the bus time out logic drives BERR* active and sets the status bit in the CSR. Since the bus time out clock is asynchronous to the assertion of the data strobes the bus time out is only accurate to + one clock period due to the synchronization of the data strobes with the bus time out clock. Below is the BTO range, depending on the prescaler value selected. Once a prescaler value is chosen, one can specify a bus time out period and compute the correct counter data value with the formula given in Figure 10. One must convert the base ten value given by the formula to base 2 for the actual counter value. Appendix C contains a software example for programming the bus time out in the Initialization routine.

COUNTER DATA VALUE

Figure 10

PRESCALER	MIN BTO	MAX BTO
4	3.26 μsec	0.84 msec
10	8.13 μsec	2.08 msec
16	13.02 μsec	3.33 msec
50	40.69 μsec	10.42 msec
64	52.08 μsec	13.33 msec
100	81.38 μsec	20.83 msec
200	162.76 μsec	41.76 msec

$$\text{COUNTER VALUE}_{10} = \frac{(\text{BTO})\,(2457600)}{(\text{PRESCALER})\,(2)}$$

SPECIFICATIONS

Electrical Specifications

VMEbus DRIVERS

Totem-Pole	V_{OL} = 0.6 V Max @ 48 ma V_{OH} = 2.4 V Min @ 3 ma
Three-State	V_{OL} = 0.6 V Max @ 48 ma V_{OH} = 2.4 V Min @ 3 ma I_{OZ} = +50 μa Max @ 2.4 V or 0.5 V
Open-Collector	V_{OL} = 0.6 V Max @ 48 ma I_{OH} = 50 μa Max @ 5 V

VMEbus RECEIVERS

V_{IL} = 0.8 V Max
V_{IH} = 2.0 V Min
I_{IL} = –400 μa Max @ $0 < V < 0.5$
I_{IH} = 50 μa Max @ $5.0 > V > 2.7$

VOLTAGE REQUIREMENTS

+5 V @ 4 A MAX
+12 V @ 150 mA MAX (RS232 only)
–12 V @ 150 mA MAX (RS232 only)

Mechanical Specifications

Length	6.30 in. (160 mm)
Width	9.20 in. (233.7 mm) .68 ± .38 mm)
Board Thickness	.062 in. (1.57 mm)
Component Lead Protrusion	.100 (2.54 mm) Max
Connector	96 Pin, IEC Standard (603-2 IEC-c096-M)

Environmental Specifications

Temperature Range	0-60° C
Relative Humidity	10-90% (non-condensing)

APPENDICES

APPENDIX A
RS-232C PIN OUT AND CABLE WIRING LIST

RS232C SIGNAL	DB25 PIN #	P2-PIN NUMBER
BA (TXDATA)	2	7a
BB (RXDATA)	3	8a
CA (DSR)	4	8c
CB (CTS)	5	9c
CC (DCD)	6	10a
AB (GND)	7	10c
CF (DCD)	8	11c
CD (DTR)	20	11a

APPENDIX B
P2 PINOUT

PIN NUMBER	ROW A	ROW B	ROW C
1	TAOUT	5VOLT	NC
2	TAIN	GND	NC
3	SI	NC	NC
4	TBIN	NC	NC
5	TBOUT	NC	NC
6	BTOCLK	NC	NC
7	BA(TXDATA)	NC	NC
8	BB(RXDATA)	NC	CA(RTS)
9	NC	NC	CB(CTS)
10	CC(DSR)	NC	AB(GND)
11	CD(DTR)	NC	CF(DCD)
12	NC	GND	NC
13	S0	5VOLT	S4
14	S1	NC	S5
15	S2	NC	S6
16	S3	NC	GND
17	I7OUT	NC	S7
18	EXTRESET*	NC	NC
19	NC	NC	NC
20	NC	NC	NC
21	NC	NC	NC
22	NC	NC	GND
23	NC	NC	NC
24	NC	NC	NC
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	GND	GND
29	NC	NC	NC
30	NC	NC	NC
31	NC	GND	NC
32	NC	5VOLT	NC

```
MOTOROLA MK68000 ASM VERSION 1.20 SYS :  12      .SBCOPS  .SA  08/26/82  14:16:28  PAGE 1

                         *
                         *
                         *
                         *          SBC SERIAL SOFTWARE DRIVER EXAMPLE
                         *
                         *
                         *
00001000                 *          ORG     $1000
                         *
                         *          PROGRAM DEFINITIONS
                         *
00000002    BAUD         EQU     $02          ; BAUD RATE = 9600
000000FF    BTO          EQU     $FF          ; BUS TIME OUT CONSTANT
00000000    RXFULL       EQU     $0           ; RECEIVER FULL BIT
00000002    TXEMPTY      EQU     $2           ; TRANSMITTER EMPTY BIT
                         *
                         *
                         *          STI DIRECT REGISTER DEFINITIONS
                         *
00FFF821    STI          EQU     $FFF821      ; STI BASE ADDRESS
00000000    IDR          EQU     $0           ; INDIRECT DATA REGISTER
00000002    GPIP         EQU     $2           ; GENERAL PURPOSE I/O INTERRUPT
00000004    IPRB         EQU     $4           ; INTERRUPT PENDING REGISTER B
00000006    IPRA         EQU     $6           ; INTERRUPT PENDING REGISTER A
00000008    ISRB         EQU     $8           ; INTERRUPT IN-SERVICE REGISTER B
0000000A    ISRA         EQU     $A           ; INTERRUPT IN-SERVICE REGISTER A
0000000C    IMRB         EQU     $C           ; INTERRUPT MASK REGISTER B
0000000E    IMRA         EQU     $E           ; INTERRUPT MASK REGISTER A
00000010    PVR          EQU     $10          ; POINTER VECTOR REGISTER
00000012    TABCR        EQU     $12          ; TIMER A AND B CONTROL REGISTER
00000014    TBDR         EQU     $14          ; TIMER B DATA REGISTER
00000016    TADR         EQU     $16          ; TIMER A DATA REGISTER
00000018    UCR          EQU     $18          ; USART CONTROL REGISTER
0000001A    RSR          EQU     $1A          ; RECEIVER STATUS REGISTER
0000001C    TSR          EQU     $1C          ; TRANSMITTER STATUS REGISTER
0000001E    UDR          EQU     $1E          ; USART DATA REGISTER
                         *
                         *          STI INDIRECT REGISTER DEFINITIONS
                         *
00000000    SCR          EQU     $0           ; SYNC CHARACTER
00000001    TDDR         EQU     $1           ; TIMER D DATA REGISTER
00000002    TDCR         EQU     $2           ; TIMER C DATA REGISTER
00000003    AER          EQU     $3           ; ACTIVE EDGE READY
00000004    IERB         EQU     $4           ; INTERRUPT ENABLE REGISTER B
00000005    IERA         EQU     $5           ; INTERRUPT ENABLE REGISTER A
00000006    DDR          EQU     $6           ; DATA DIRECTION REGISTER
00000007    TCDCR        EQU     $7           ; TIMER C AND D CONTROL REGISTER


                         *
                         *          LOOP TO ECHO CHARACTERS AND SET UP BUS TIME OUT VALUE
                         *          TO SERVE AS AN EXAMPLE OF USE OF THE THREE SUBROUTINES
                         *          TO FOLLOW
                         *
                         *
                         *
```

```
                                *
                                *
00001000 6106           START   BSR.S   INIT            ; SET BAUD RATE,BTO, AND USART
00001002 614C           LOOP    BSR.S   RDCHR           ; GET TERMINAL INPUT
00001004 615E                   BSR.S   WRTCHR          ; OUTPUT TO TERMINAL
00001006 60FA                   BRA.S   LOOP
                                *
                                *


                                *
                                *
                                *     INITIALIZATION: SETS BAUD RATE, BUS TIME OUT CONSTANT,
                                *     AND USART THROUGH THE STI
                                *
                                *
                                *
                                *
                                *
00001008 43F900FFF821   INIT    LEA     STI,A1          ; STI BASE ADDRESS
0000100E 137C00060010           MOVE.B  #DDR,PVR(A1)    ; POINT TO DATA DIRECTION REGISTER
00001014 12BC0043               MOVE.B  #$43,IDR(A1)    ; SET OUTPUTS
00001018 137C00000002           MOVE.B  #$00,GPIP(A1)   ; RS-232 CONTROL OUTPUTS ACTIVE
0000101E 137C00010010           MOVE.B  #TDDR,PVR(A1)   ; POINT TO BAUD RATE COUNTER
00001024 12BC0002               MOVE.B  #BAUD,IDR(A1)   ; SET BAUD RATE
00001028 137800070010           MOVE.B  TCDCR,PVR(A1)   ; POINT TO TIMER C AND D CONTROL REG.
0000102E 12BC0021               MOVE.B  #$21,IDR(A1)    ; DIV BY 4 (TIM D), DIV BY 10 (TIM C)
00001032 137C00980018           MOVE.B  #$98,UCR(A1)    ; DIV BY 16, 2 STOP BITS
00001038 137C0001001A           MOVE.B  #$1,RSR(A1)     ; ENABLE RECEIVER
0000103E 137C0005001C           MOVE.B  #$5,TSR(A1)     ; ENABLE TRANSMITTER
00001044 137C00020010           MOVE.B  #$TDCR,PVR(A1)  ; POINT TO BUS TIME OUT COUNTER
0000104A 12BC00FF               MOVE.B  #BTO,IDR(A1)    ; SET BUS TIME OUT CONSTANT
0000104E 4E75                   RTS
                                *
                                *
                                *


                                *
                                *
                                *     RDCHR: READS CHARACTER FROM STI AND RETURNS ASCII
                                *     VALUE IN D0.
                                *
                                *
                                *
                                *
                                *
00001050 43F900FFF821   RDCHR   LEA     STI,A1          ; STI BASE ADDRESS
00001056 08290000001A   RXPOOL  BTST.B  #RXFULL(A1)     ; RECEIVER FULL?
0000105C 67F8                   BEQ.S   RXPOOL          ; CONTINUE POLL
0000105E 1029001E               MOVE.B  UDR(A1),D0      ; GET ASCII INPUT
00001062 4E75                   RTS
                                *
                                *
                                *


                                *
                                *
                                *     WRTCHR: OUTPUTS CHARACTER IN D0 TO TERMINAL
                                *
                                *
```

```
114                             *
115                             *
116  00001064 43F900FFF821  WRTCHR  LEA      STI,A1              ; STI BASE ADDRESS
117  0000106A 08290002001C  TXPOOL  BTST.B   #TXEMPTY,TSR(A1)   ; TRANSMITTER EMPTY?
118  00001070 67F8                  BEQ.S    TXPOOL
119  00001072 1340001E              MOVE.B   D0,UDR(A1)          ; OUTPUT CHARACTER
120  00001076 4E75                  RTS
121                             *
122                             *
123                             *
124                                      END

****** TOTAL ERRORS    0--    0
****** TOTAL WARNINGS  0--    0
```


SYMBOL TABLE LISTING

SYMBOL NAME	SECT VALUE	SYMBOL NAME	SECT VALUE
AER	00000003	RSR	0000001A
BAUD	00000002	RXFULL	00000000
BTO	000000FF	RXPOOL	00001056
DDR	00000006	SCR	00000000
GPIP	00000002	START	00001000
IDR	00000000	STI	00FFF821
IERA	00000005	TABCR	00000012
IERB	00000004	TADR	00000016
IMRA	0000000E	TBDR	00000014
IMRB	0000000C	TCDCR	00000007
INIT	00001008	TDCR	00000002
IPRA	00000006	TDDR	00000001
IPRB	00000004	TSR	0000001C
ISRA	0000000A	TXEMPTY	00000002
ISRB	00000008	TXPOOL	0000106A
LOOP	00001002	UCR	00000018
PVR	00000010	UDR	0000001E
RDCHR	00001050	WRTCHR	00001064

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
VME-SBC	VME 8 MHz Single Board Computer with Technical Manual (MON68K Debugger Monitor, 12K bytes RAM)	MK75601-8-01
VME-SBC	VME 8 MHz Single Board Computer with Technical Manual (4K bytes RAM, configured for 48K bytes EPROM)	MK75601-8-01
VME-SBC Technical Manual	Technical Manual only	4420342

III

FEATURES

- VMEbus Master/Slave
- DMA can transfer up to 64K byte data blocks
- Programmable Bus Request and Interrupt Priority Request level
- Interface to SASI compatible controllers
- Up to eight Controllers can interface to the VMEbus through the VME-SASI
- Byte or Word DMA data transfer capability or Programmed byte data transfers
- Automatic SASI handshake control for communication with controller
- End of command interrupt
- Selectable I/O address on P2 connector

VME SYSTEM DESCRIPTION

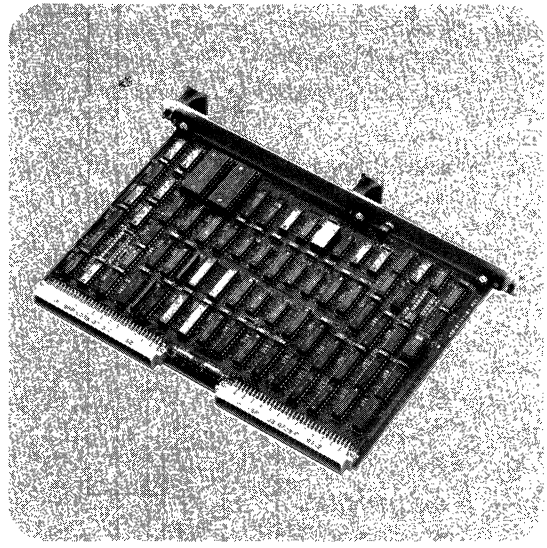
The VMEbus was designed jointly by Mostek, Motorola, and Signetics and was introduced in October, 1981. It offers a combination of high performance timing parameters, a compact form factor, and the advanced functional capability appropriate for today's applications of 16-bit microprocessors such as the MK68000. The international-standard compact board size promotes functional modularity and low board cost, and it allows the user to select only those functions needed for his application.

VME-SASI DESCRIPTION

The VME-SASI interfaces the VMEbus with a non-arbitrating Shugart Associates System Interface (SASI) bus, which is compatible with many hard disk and floppy disk controllers. SASI handshake control signals are monitored and acknowledged automatically by the VME-SASI, thus minimizing software overhead. The condition of the interface is available through a status register.

Data transfers with a controller can be performed on a programmed byte basis or by using the DMA modes. A byte DMA mode is provided for DMA transfers to or from other byte oriented I/O devices. The word DMA mode allows data transfers in standard addressed memory.

VME-SASI BOARD
Figure 1



Interrupts report the conditions of controller status available and the end of DMA transfer.

The daisy chain bus request and interrupt request configuration of the VMEbus allows multiple VME-SASI boards to be used in a system. Each VME-SASI board address, within short I/O address space, is selected (8 word increments) by strapping on the P2 connector.

A control register provides the capability to select the Interrupt priority level, bus request level, User/Supervisor access, DMA mode, and diagnostic status.

A red/green bi-color LED provides a visual indication of the diagnostic status of the board.

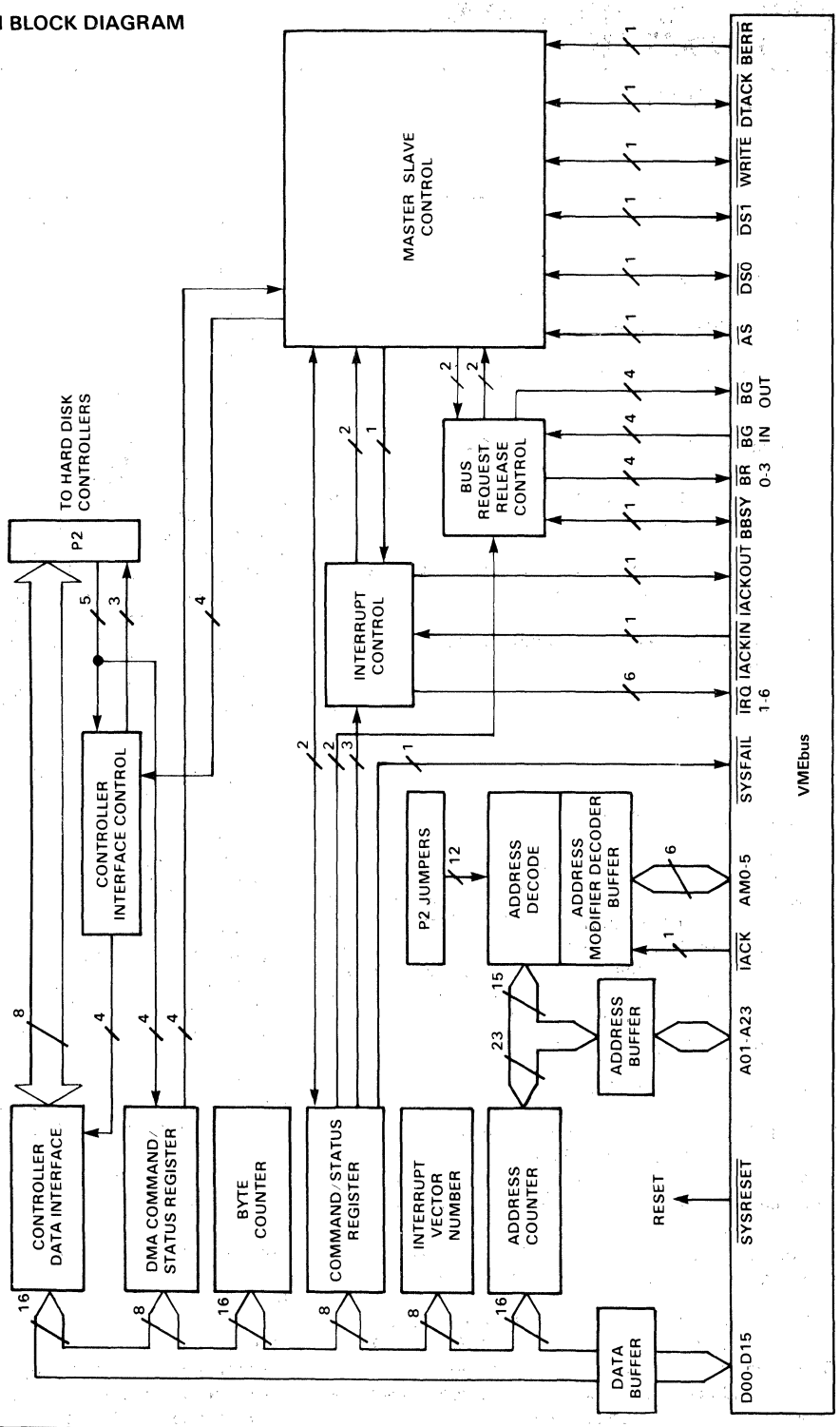
The VME-SASI Block Diagram is shown in Figure 2.

INSTALLATION

The VME-SASI mates with the VMEbus standard connections as defined by the VMEbus Technical Specification. The SASI bus connections are made through the P2 connector. The P2 signals are defined in Table 1.

VME-SASI BLOCK DIAGRAM

Figure 2



P2 CONNECTOR

Table 1

VME-SASI P2 CONNECTOR SIGNALS			
PIN NO.	**ROW A**	**ROW B**	**ROW C**
1	CA 15	+5 V	CA 14
2	CA 13	GND	CA 12
3	CA 11	R'SVED	CA 10
4	CA 9	A24	CA 8
5	CA 7	A25	CA 6
6	CA 5	A26	CA 4
7	GND	A27	GND
8	DATA 0*	A28	SIGGND
9	DATA 1*	A29	SIGGND
10	DATA 2*	A30	SIGGND
11	DATA 3*	A31	SIGGND
12	DATA 4*	GND	SIGGND
13	DATA 5*	+5 V	SIGGND
14	DATA 6*	D16	SIGGND
15	DATA 7*	D17	SIGGND
16	NU	D18	NU
17	NU	D19	NU
18	NU	D20	NU
19	NU	D21	NU
20	NU	D22	NU
21	NU	D23	NU
22	NU	GND	NU
23	NU	D24	NU
24	NU	D25	NU
25	BSY*	D26	SIGGND
26	ACK*	D27	SIGGND
27	RST*	D28	SIGGND
28	MSG*	D29	SIGGND
29	SEL*	D30	SIGGND
30	C*/D	D31	SIGGND
31	REQ*	GND	SIGGND
32	I/O*	+5 V	SIGGND

NU - NOT USED
CA - COMPARED ADDRESS Strap address lines to ground to select the desired SASI short I/O address.
SIGGND - SIGNAL GROUND To be used when a ground is desired for each signal such as a twisted pair, or alternating grounds in a flat cable.

Address Strapping

The VME-SASI slave address resides in short I/O addressing space and is strappable to any sixteen byte I/O address boundary. Base address selection is made by strapping the desired address via the P2 connector.

The P2 address pins are a logic high (true) when left open. Therefore, to select the desired base address, strap the address bits required to be logic low (false) to ground. If all pins are left open, the base address will be FFFFF0. If all pins are grounded, the base address will be FF0000. The P2 address pins are listed in Table 2.

SASI P2 Interface

The SASI signal pinout on the P2 connector is shown in Table 3. The P2 - GND column indicates the ground associated with each signal for cabling purposes. Note that the pinouts are compatible with a 50 pin flat cable to interface directly to a SASI bus.

P2 ADDRESS STRAPPING PINS

Table 2

A 4	P2-6c
A 5	P2-6a
A 6	P2-5c
A 7	P2-5a
A 8	P2-4c
A 9	P2-4a
A10	P2-3c
A11	P2-3a
A12	P2-2c
A13	P2-2a
A14	P2-1c
A15	P2-1a

P2 SASI SIGNALS

Table 3

SASI SIGNAL	P2 - PIN	P2 - GND
DATA 0*	a 8	c 8
DATA 1*	a 9	c 9
DATA 2*	a10	c10
DATA 3*	a11	c11
DATA 4*	a12	c12
DATA 5*	a13	c13
DATA 6*	a14	c14
DATA 7*	a15	c15
BSY*	a25	c25
ACK*	a26	c26
RST*	a27	c27
MSG*	a28	c28
SEL*	a29	c29
C/D*	a30	c30
REQ*	a31	c31
I/O*	a32	c32

* indicates true low signals

TECHNICAL INFORMATION

Register Map

All registers on the VME-SASI are accessed through short I/O addressing. The exact address block (8 words) is selected by address strapping (A4-A15) on the P2 connector. All registers may be accessed as word registers on even addresses. All registers, except the upper byte registers that are "don't cares", may be accessed as byte registers. If an attempt is made to access a "don't care" upper byte register as a byte, the SASI will not respond and a bus timeout will occur. The upper byte "don't care" registers are shown in Figure 3 as X's.

The registers are listed below in the order of their offset from the base address selected by the address straps on P2. The register map is shown in Figure 3.

OFFSET	REGISTER
0 -	DMA STATUS
2 -	DMA COMMAND
4 -	UPPER BYTE COUNT
6 -	DON'T CARE
8 -	MIDDLE BYTE DMA ADDRESS
A -	DON'T CARE
C -	DON'T CARE
E -	DON'T CARE

OFFSET	REGISTER
1 -	INTERRUPT VECTOR
3 -	CSR
5 -	LOWER BYTE COUNT
7 -	UPPER BYTE DMA ADDRESS
9 -	LOWER BYTE DMA ADDRESS
B -	CONTROLLER COMMAND/STATUS
D -	CONTROLLER SELECT
F -	CONTROLLER DATA

REGISTER MAP

Figure 3

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
DMA COMP *	BERR	RE SET*	REQ*	I/O	C/D	BSY*	MSG*	INTERRUPT VECTOR NUMBER							
TMSG	TBSY	TC/D	MODE U	MODE L	R/W ---- TI/O	DMA EN	RE SET	SYS FAIL	U/S	BRQ PRI U	BRQ PRI L	TEST ENA BLE	IRQ LEV U	IRQ LEV M	IRQ LEV L
BYTE								COUNTER							
X	X	X	X	X	X	X	X	UPPER BYTE OF DMA ADDRESS							
MIDDLE BYTE OF DMA ADDRESS								LOWER BYTE OF DMA ADDRESS							
X	X	X	X	X	X	X	X	CONTROLLER COMMAND/STATUS							
X	X	X	X	X	X	X	X	CONTROLLER SELECT							
X	X	X	X	X	X	X	X	CONTROLLER DATA							

III

Register Descriptions

Referring to the register map, the top word register resides at the base address (XXX0). The low byte is the VECTOR NUMBER register. Each register and its bit functions are defined below.

Interrupt Vector Register

D00 - D00 the interrupt vector register is programmed by the user to contain the vector number for the SASI interrupt service routine.
POWER UP/RESET VALUE - Indeterminate/ Unchanged

DMA Status Register (Read Only)

D15 - DMA COMPLETE* indicates when a DMA operation has been completed by a '0' being placed in this bit. When a new DMA operation is started, the DMA COMPLETE bit is set automatically to '1'.

D14 - BERR indicates that a bus error occurred during a DMA operation while the SASI was the master. When a bus error occurs, the DMA operation is terminated, and an interrupt request is issued. The address at which the bus error occurred remains the DMA address registers. BERR is reset when the DMAEN bit is set in the CSR register.

D13 - RESET* is a read only bit which is the state of the SASI bus RESET* signal. Normally, this bit is used for diagnostic purposes.

D12 - REQ* is the SASI request line. When this bit is low, the controller is requesting or presenting data on the SASI bus. During polled operation, this bit must be low for the SASI data to be valid. This is true when the controller is inserting data on the SASI bus, and when he is requesting data on the SASI bus.

D11 - I/O indicates the direction the SASI bus is presently being set by the controller. A '0' means is inputting data from the controller. A '1' indicates the SASI is outputting data to the SASI bus.

D10 - C/D indicates the type of data being transferred over the SASI bus. A '0' means a command or command status is being transferred.

D09 - BSY* bit indicates the active status of the controller. BSY* set to '0' indicates the controller is selected and ready to conduct transactions over the SASI bus. BSY* set to '1' indicates the controller is waiting for a new command.

D08 - MSG* indicates that a command has been completed by the controller.
POWER UP/RESET VALUE - indeterminate

CSR Register

D07 - SYSTEM FAIL* is a status bit that can be set (1) or reset (0) to turn on a red (0) or green (1) LED. The system fail LED is set to red by a hardware system reset or by programmed access. The LED is set to green by programmed access only. This LED is intended to be used as a diagnostic indicator.

D06 - U/S allows user or supervisor mode access when set to '1'. When set to '0', the SASI registers can only be accessed in supervisor mode.

D05 - BUS REQUEST PRIORITY high bit

D04 - BUS REQUEST PRIORITY low bit
The two bus request priority bits select the level that will be used to request the bus during DMA operations.
00 - level 0, 01 - level 1, 10 - level 2, 11 - level 3

D03 - TEST ENABLE bit provides selection of the test mode. By setting this bit to '1', the SASI control signals are controlled by bits in the DMA COMMAND register. and provide wrap-around of the data transfer handshake bits. Do not set the test enable bit high when a controller is connected. See the test mode section for more details.

D02 - INTERRUPT REQUEST PRIORITY level select high bit

D01 - INTERRUPT REQUEST PRIORITY level select middle bit

D00 - INTERRUPT REQUEST PRIORITY level select low bit. The interrupt request priority level bits select the level (1-6) to be used for interrupts. The interrupt request priority bits are binary coded. If level 0 or 7 is selected, the interrupt requests are disabled.
POWER UP/RESET VALUE - 00

DMA Control Register

D15 - TMSG is a test control bit for the SASI bus MSG* signal. The MSG* signal will assume the opposite state of this bit when the TEST ENABLE bit is high.

D14 - TBSY is a test control bit for the SASI BSY* signal. The BSY* signal will assume the opposite state of this bit when the TEST ENABLE bit is high.

D13 - TC/D is a test control bit for the SASI C/D signal. The C/D signal will assume the opposite state of this bit when the TEST ENABLE bit is high.

D12 - MODE selection high bit

D11 - MODE selection low bit
Mode bits select the operating mode of the SASI. The four modes are selected by setting the high and low bits to the binary value of the mode.

00 - MODE 0	01 - MODE 1
10 - MODE 2	11 - MODE 3

D10 - R/W selects the DMA direction
1 - DMA read is selected. Data is DMA'ed from memory to the controller.
0 - DMA write is selected. Data is DMA'ed from the controller to the memory.
When TEST ENABLE = 1, this bit is also the TI/O test control bit for the SASI I/O signal. The I/O signal will assume the opposite state of this bit.

D09 - DMAEN enables the SASI to start a DMA transfer. DMAEN is automatically reset to '0' when the DMA transfer is completed or a bus error occurs.

D08 - RESET is used to reset the controller. This bit must be set to '1' then to '0' to reset the controller.
POWER UP/RESET VALUE - 00

Byte Count Register

D15 - D00 The byte count register is used to set the number of bytes to be transferred during a DMA operation.
POWER UP/RESET VALUE - 0000

DMA Address Upper Byte Register

D07 - D00 DMA access will begin in the upper address.This register represents A23 - A16.
POWER UP/RESET VALUE - Indeterminate/ Unchanged

DMA Address Lower Word Register

D15 - D00 DMA access will begin in the lower address. These bits represent A15 - A01. Bit 0 of this register is always set to 0 (even address) by the hardware.
POWER UP/RESET VALUE - Indeterminate Unchanged

Controller Command/Status Register

D07 - D00 All command and command status transfers with the controller are transferred through this register.
POWER UP/RESET VALUE - Indeterminate

Controller Select Register

D07 - D00 Up to eight controllers can be selected, one at a time, by setting one of the eight bits of this register '1'. A '1' must be assigned to one bit in this register before each controller command. This register may be read to determine which controller was last selected.
POWER UP/RESET VALUE - Indeterminate

Controller Data Register

D07 - D00 All data transfers with the controller must be through this register. Data is specified as any

bytes (except for the controller select, the command bytes, or the command status bytes) transferred to or from the controller.
POWER UP/RESET VALUE - Indeterminate

Register Access

All registers are read/write except the DMA STATUS register which is read only. The byte registers which contain all "don't care" bits are not accessible as byte registers. If access to these "don't care" registers is attempted, the SASI will not respond with a bus DTACK*.

Registers can be accessed as byte registers, with the above restrictions, or as word registers on even addresses.

While DMA operations are in progress (DMAEN bit set in DMA CONTROL register), the writes and reads of some registers are inhibited to prevent the DMA operation from being corrupted. If an illegal access is attempted, the SASI will not respond with a bus DTACK*. Illegal register reads and writes, occurring during DMA operations, are listed in Table 4.

ILLEGAL/LEGAL REGISTER ACCESS DURING DMA
Table 4

REGISTER	(I = ILLEGAL, WRITE	L = LEGAL) READ
CSR	I	L
DMA COMMAND	L	L
INTERRUPT VECTOR	I	L
DMA STATUS	I	L
BYTE COUNT	I	L
DMA ADDRESS UPPER	I	L
DMA ADDRESS LOWER	I	L
CONTROLLER COMMAND/STATUS	I	L
CONTROLLER SELECT	I	L
CONTROLLER DATA	I	I

A restriction for slave access to the controller register, when the DMA is not enabled, is that they be accessed per SASI protocol. That is, the COMMAND/STATUS register can only be accessed when a command or status transfer is required; the SELECT register may be accessed only when the controller is to be selected; the DATA register may only be accessed when data is to be transferred. If access to any of these registers is attempted when the SASI interface is in the wrong phase, the VME-SASI will not respond with a DTACK*. Table 5 specifies the SASI signal conditions required for legal access to the controller registers. Note that for any slave access to be legal, the DMA must not be enabled (DMAEN=0 in CSR).

CONTROLLER REGISTER LEGAL ACCESS CONDITIONS
Table 5

REGISTER	BSY*	I/O	C*/D	REQ*
WRITE SELECT	1	X	X	X
WRITE COMMAND	0	1	0	0
WRITE DATA	0	1	1	0
READ SELECT	X	X	X	X
READ STATUS	0	0	0	0
READ DATA	0	0	1	0

X - DON'T CARE

Interrupt Requests

Interrupt requests can be programmed to levels 1-6 via the CSR register. Programming the interrupt level to 0 or 7 disables any interrupt requests from being generated.

Interrupt requests are issued for the following conditions:

a) After any DMA operation is completed. Completion of a DMA is defined to be when the byte counter counts down to zero or the controller has completed a command.
b) After a bus error occures during a DMA operation. The address where the error occurred remains in the DMA address register.

Operating Modes

One of four operating modes can be selected for DMA operations. The mode is selected by setting the MODE bits of the CSR register to the binary value of the mode number desired. The four modes are described below.

Mode 0

This mode allows data transfers with the controller actually transferring the data to memory. Each data transfer from or to the controller requires a handshake sequence to be performed. When the DMA is enabled, handshakes are performed until the byte counter goes to zero. Then an interrupt request is issued, and the DMA is disabled.

Mode 1

This is the byte DMA mode. The SASI performs DMA byte data transfers to the same short I/O address in the DMA address register. The Address Modifier codes placed on the bus are for short I/O. The DMA is complete when the byte count goes to zero or when the controller command is completed. An intrrupt request is issued and the DMAEN bit is reset on completion of the DMA operation. The DMA address does not increment in this mode; the same address is used for all byte data transfers.

Mode 2

This is the word DMA mode. The SASI performs word DMA transfers to the address in the DMA address register. The Address Modifiers are set for Data accesses. The DMA is complete when the byte count goes to zero or when the controller command is completed. An interrupt request is issued and the DMAEN bit is reset on completion of the DMA operation. The DMA address continues to the next even address after a DMA transfer.

Mode 3

This mode is similar to MODE 0; however, the handshakes are performed with the controller until the command has been completed. In Mode 0, they are performed until the byte count goes to zero. DMA data transfers do not occur in this mode; the data is thrown away. An interrupt request is issued when the controller command is completed.

User/Supervisor Access

The level of access to the SASI is determined by the state of the U/S bit in the CSR register. When the U/S bit is '0', only the supervisor may access the SASI. When the U/S bit is '1', both the user and supervisor may access the SASI.

When both the user and supervisor are allowed access, the mode of the DMA operation is the same as the mode of the master that programmed the SASI to do the DMA operation. That is, if the SASI is programmed in the user mode to do a DMA transfer, then the address modifier code used for the DMA transfer will be a user code. If the SASI is programmed in the supervisor mode, the address modifier codes for the DMA will be a supervisory code.

Using the Test Mode of the SASI

The SASI provides a diagnostic test mode which allows the SASI to test the SASI interface and perform DMA operations without a controller connected. The test mode should be used only when the controller is disconnected. When the TEST ENABLE bit in the CSR is set high, the test mode is selected and the SASI signals are controlled as follows:

REQ* - ACK* is connected to REQ*
BSY* - SEL* and TBSY are logically or'ed and inverted and then connected to BSY*
I/O - R/W is connected to I/O
C/D - TC/D is inverted and then connected to C/D
MSG* - TMSG is inverted and then connected to MSG*
RESET* - RESET* is controlled normally through the CSR register. The RESET* signal itself is read through the DMA STATUS register.

When the TEST ENABLE bit is selected, a DMA read or write transfer may be performed by setting the SASI signals to the proper state and then enabling the DMA. Since the SASI data bus is not connected to anything, all '0's will be written into write DMA's. During read DMA's, the data at the SASI bus ry during is going out and cannot be checked.

This test mode allows the user to verify most of the DMA master logic used during an actual DMA operation.

Using the VME-SASI with a SASI Controller

An example of how to use the VME-SASI with a SASI controller for programming purposes is given in this section.

The basic SASI protocol must always be followed, or errors will occur. The basic SASI protocol is described below, and an example of a DMA read or write is presented.

SASI Protocol

The protocol discussed here is only applicable to the software and hardware protocol which must be monitored by the user program while using the VME-SASI. Interface signals, which provide status of the present condition of the interface, are available in the DMA status register. The description of the status bits is given in the register definition section. Table 6 presents typical interface phases identified by the state of the status bits.

The DMA STATUS BSY* bit signifies that the controller is selected and is either awaiting a command or executing a command. When the BSY* bit returns high, the command has been completed, including all of the data and status transfers to and from the controller.

If the controller is in an unknown state, or if execution is beginning from power up, the controller should be reset. To reset the controller, set the reset bit of the DMA CONTROL register high then low. The STATUS register bits BSY*, I/O, C/D, and MSG* should be '1' following a reset.

The controller sequence to execute a command is constant. The sequence is as follows. When reading or writing bytes to the controller command/status, select, or data registers, ensure that the REQ* bit in the DMA status register is '0'. REQ* low means the controller either wants data or has data ready. If the controller registers are accessed before the controller is ready, a bus timeout will probably occur.

1) Set the byte count - Write the number of bytes to be transferred by a DMA operation into the BYTE COUNT register.

2) Set the DMA address - Write the starting address for the DMA operation into the DMA ADDRESS register.

3) Select the controller - The controller is selected by writing a '1' to the bit number representing the controller to be selected. Controller selection is done through the CONTROLLER SELECT register.

SASI INTERFACE PHASES
Table 6

BSY*	I/O	C/D	MSG*	INTERFACE CONDITION
1	1	1	1	After a RESET has been issued, or after command status bytes have been read.
0	1	0	1	The controller is receiving or is ready for a command from the SASI. This condition exists after controller selection.
0	1	1	1	The controller requests data from the SASI.
0	0	1	1	The controller is putting data on the bus for the SASI.
0	0	0	1	The controller command status byte is available to the SASI.
0	0	0	0	The controller sends a message byte to inform the SASI that the command is complete including the status byte. The next state of the status bits will be all 1's indicating the controller is ready for selection.

ENDING STATUS: I/O = 1, C/D = 0, BSY* = 0, MSG* = 1

4) Send command to the controller - The controller expects a six or ten byte command. All command bytes must be written through the CONTROLLER COMMAND register. The format and exact data for specific commands are controller dependent.

ENDING STATUS after:
Write command - I/O = 1, C/D = 1, BSY* = 0, MSG* = 1
Read command - I/O = 0, C/D = 1, BSY* = 0, MSG* = 1
End of command - I/O = 0, C/D = 0, BSY* = 0, MSG* = 1

5) For DMA transfers (reads or writes), set DMA direction, DMA mode, and enable DMA. The final step to initiate the command sent to the controller and perform the associated DMA transfers is to set the appropriate DMA MODE, DMA direction (read or write), and DMAEN bits in the DMA CONTROL register. The mode and direction should be set prior to this step. The DMA operation is actually started by setting the DMAEN bit to '1'. This is the last step. When the DMA is completed, the SASI will issue an interrupt request.

ENDING STATUS: The completion of a DMA operation may not actually be the completion of the command. This condition may occur if the set byte count is less than the number of sectors commanded to be read or written. Therefore, two status conditions can exist at this point.

End of Command Status: I/O = 0, C/D = 0, BSY* = 0, MSG* = 1
Not End of Command Status: I/O = X, C/D = 1, BSY* = 0, MSG* = 1
X = 1 for DMA read, 0 for DMA write

6) If the command was completed, the controller presents one byte of status which must always be read to complete the transaction for any command. The status byte must be zero for a no error status. The status bytes must be read through the CONTROLLER COMMAND/STATUS register. When reading the status byte, the REQ* signal must be true for valid status. The DMA STATUS register bits are given below.

STATUS AFTER Error Status Byte read:
I/O = 0, C/D = 0, BSY* = 0, MSG* = 0

7) After the status byte is read, the controller presents a message to the SASI indicating that the controller is through with both the command and status phases and will be ready for a new command after the message is read. The message must be read through the CONTROLLER COMMAND/STATUS register. Note that when reading the message byte, the REQ* signal must be true for a valid message. The DMA status bits after reading the message are given below.

STATUS AFTER reading message byte:
I/O = 1, C/D = 1, BSY* = 1, MSG* = 1

Notice that the BSY* bit went high after the last status byte was read, indicating that the command was completed.

8) In step 5, if the command data transfer was not completed, the rest of the data must be transferred by resetting the byte count to the number of bytes left to be transferred, or by using MODE 3. If MODE 3 is used, the data is not used. Handshaking with the controller is performed simply to complete the data transfer. Status is then available when the end of the command is reached. If status is not required, reset could be issued to the controller to setup for a new command.

ELECTRICAL SPECIFICATIONS

VMEbus Drivers

Totem-Pole
V_{OL} = 0.6 V Max @ 48 MA
V_{OH} = 2.4 V Min @ 3 MA

Three State
V_{OL} = 0.6 V Max @ 48 MA
V_{OH} = 2.4 V Min @ 3 MA
I_{OZ} = +50 μA Max @ 2.4 V or 0.5 V

Open-Collector
V_{OH} = 0.6 V Max @ 48 MA
I_{OH} = 50 μA Max @ 5 V

VMEbus Receivers

V_{IL} = 0.8 V Max
V_{IH} = 2.0 V Min
V_{IL} = -400 μA Max @ $0 < V < 0.5$
V_{IH} = 50 μA Max @ $5.0 > V > 2.7$

SASI Bus Drivers (Open-Collector)

Bus terminated with 220/330 Ohms

V_{OL} = 0.5 V Max @ 48 MA
V_{OH} = 2.5 V Min

SASI Bus Receivers

Bus terminated with 220/330 Ohms

V_{IL} = 0.8 V Max @ 0.8 MA
V_{IH} = 2.0 V Min

Power Requirements

+5 V 4.75 V to 5.25 V @ 3.5 A Typ, 4.5 A Max

MECHANICAL SPECIFICATIONS

Length:	630 inches (160 mm)
Width:	9.20 inches (233.68 mm)
Board Thickness:	0.062 inches (1.57 mm)
Component Height:	0.5 inches (14.73 mm)
Connectors:	96 pin DIN 41612 Compliant

ENVIRONMENTAL SPECIFICATIONS

Operating:

Temperature Range	0°C to 60°C
Relative Humidity	0 to 90% non-condensing

Storage:

Temperature Range -10°C to 85°C

ORDERING INFORMATION

Designator	Description	Part No.
VME-SASI	VME SASI Interface Board with Technical Manual	MK75802
VME-SASI Technical Manual	VME-SASI Technical Manual only	4420341

PRELIMINARY

VME-SIO

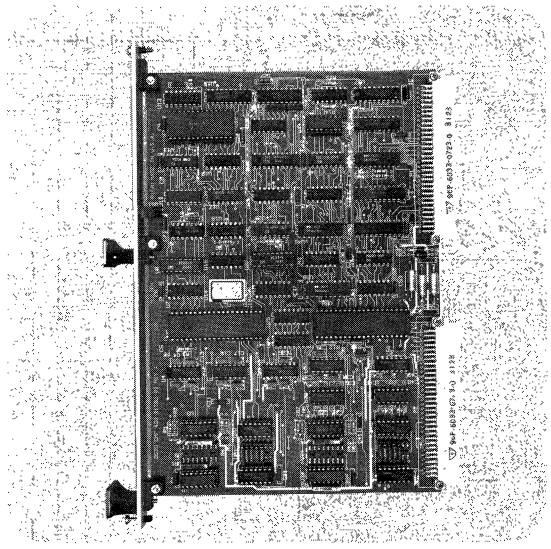
FEATURES

- ☐ Four independent full-duplex serial channels
  - RS-232 Data Rates to 19.2 K Baud
  - RS-422 Data Rates to 307.2 K Baud
- ☐ VMEbus compatible
- ☐ Software programmable Baud Rates
- ☐ Software Controllable front panel status LED
- ☐ Read/Write Control Register
- ☐ Software programmable self test mode
- ☐ All I/O via Back Plane Connectors
- ☐ Asynchronous Operation
  - 5, 6, 7, or 8 bits/character
  - 1, 1½, or 2 stop bits
  - Even, odd, or no parity
  - X16, X32 and X64 clock modes
  - Break generation and detection
  - Parity, overrun, and framing error detection
- ☐ Binary Synchronous Operation
  - Internal or external character synchronization
  - Monosync or bisync operation
  - Automatic sync character insertion
  - CRC generation and checking
- ☐ HDLC and IBM SDLC Operation
  - Abort sequence generation and detection
  - Automatic zero insertion and detection
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - Valid message protected from overrun
  - CRC generation and checking

VME SYSTEM

The VMEbus was designed jointly by Mostek, Motorola, and Signetics and introduced in Oct. 1981. It offers a combination of high performance timing parameters, compact form factor, and advanced functional capability appropriate for today's application of 16-bit microprocessors such as the MK68000.

VME-SIO
Figure 1



VME-SIO

The VME-SIO (MK75801-0-01/02) serves as a four channel full duplex serial communication module for the VMEbus. The VME-SIO block diagram is shown in Figure 2. A typical system configuration is shown in Figure 3.

The MK75801-0-01 offers four channels of RS-232(DCE); the MK75801-0-02 offers two channels of RS-232(DCE) and two channels of RS422 data communications.

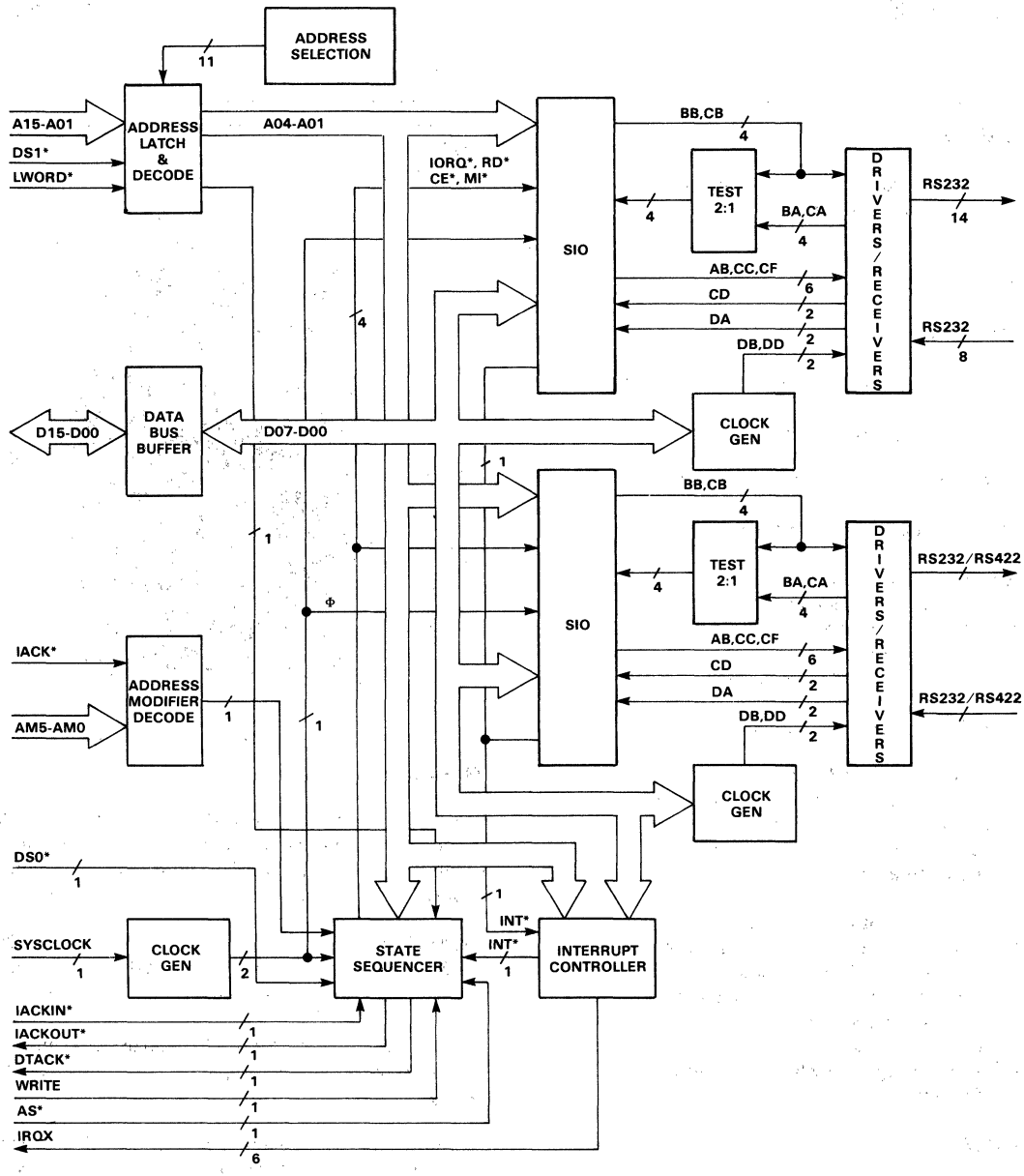
Each of the four channels is a full duplex serial link. Each channel is supported with separately programmable Baud Rate generation.

The VME-SIO can generate and check CRC codes in synchronous mode and can be programmed to check data integrity in various modes.

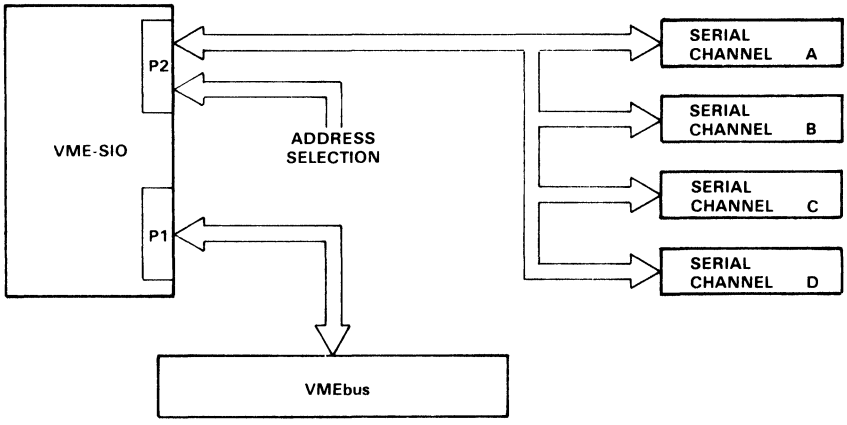
The VME-SIO is programmable for supervisor/user access. When selected for user access, the SIO can be accessed in either the supervisor or user state. However, when the VME-SIO is selected for supervisor space, the module can

VME-SIO BLOCK DIAGRAM

Figure 2



SYSTEM CONFIGURATION DIAGRAM
Figure 3



only be accessed in the supervisor state. When accessed by the user state when programmed for supervisor state, the module will not respond with DTACK*. Programming of the user/supervisor state is via the module's control register (CR).

The VME-SIO is programmable for interrupt priority levels via the module's control register (CR). The module provides an interrupt vector as described by the VMEbus Technical Specification. Each MK3887-4 SIO chip may provide a unique vector, thereby allowing separate service routines for the RS-232 and RS-422 I/O ports.

The module's address strapping is accomplished via the P2 (J2 backplane) connector. The address strapping allows the VME-SIO module to exist anywhere within the short I/O addressing space on 32 byte boundaries. Only Byte (8 bit) data transfers are supported. If a word or longword transfer is attempted, the VME-SIO will not respond with a DTACK*.

A facility for on-line self test mode is provided via the self test bit in the modules control register. When this bit is set, the transmit of each channel is looped back into the receive side of the same channel, thus enabling the use of self test diagnostics. The switching is on the MK3887 side of the channel driver/receivers, so it is not required that the module be disconnected from the serial transmission lines in order to use this feature.

VMEbus INTERFACE INSTALLATION

The VME-SIO mates with the VMEbus Standard connections as defined by the VMEbus Technical Specification. The P1 signals are defined in Table 1. The P2 signals are defined in Table 2.

Table 1 identifies the VMEbus backplane J1/P1 connector pin assignments for the VME-SIO. The table lists the pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.) All signal pins defined by the VMEbus Technical Specification are listed; those not used by the VME-SIO are indicated as (NC).

J1/P1 PIN ASSIGNMENTS VME-SIO

Table 1

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	D01	BBSY* (NC)	D08 (NC)
2	D01	BCLR* (NC)	D09 (NC)
3	D02	ACFAIL* (NC)	D10 (NC)
4	D03	BG0IN*	D11 (NC)
5	D04	BG0OUT*	D12 (NC)
6	D05	BG1IN*	D13 (NC)
7	D06	BG1OUT*	D14 (NC)
8	D07	BG2IN*	D15 (NC)
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0* (NC)	SYSRESET*
13	DS0*	BR1* (NC)	LWORD*
14	WRITE*	BR2* (NC)	AM5
15	GND	BR3* (NC)	A23 (NC)
16	DTACK*	AM0	A22 (NC)
17	GND	AM1	A21 (NC)
18	AS*	AM2	A20 (NC)
19	GND	AM3	A19 (NC)
20	IACK*	GND	A18 (NC)
21	IACKIN*	SERCLK(1) (NC)	A17 (NC)
22	IACKOUT*	SERDAT (1) (NC)	A16 (NC)
23	AM4	GND	A15
24	A07	IRQ7* (NC)	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	−12 V	+5 V STDBY (NC)	+12 V
32	+5 V	+5 V	+5 V

NOTE:
SERCLK and SERDAT represent provision for a special serial communication bus protocol still being finalized.

Table 2 identifies the VMEbus backplane J2/P2 pin assignments for the VME-SIO. The table lists the pin assignments by pin number order. (The connector consists of three rows of pins labeled A, B, C.)

J2/P2 PIN ASSIGNMENTS VME-SIO
Table 2

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	CA15	+5	CA14
2	CA13	GND	CA12
3	CA11	(N/C)	CA10
4	CA09	(N/C)	CA08
5	CA07	(N/C)	CA06
6	CA05	(N/C)	(N/C)
7	(TXA)BA	(N/C)	(TSETA)DB
8	(RXA)BB	(N/C)	(RTSA)CA
9	(RSETA)DD	(N/C)	(CTSA)CB
10	(DSRA)CC	(N/C)	(GNDA)AB
11	(DTRA)CD	(N/C)	(RSLDA)CF
12	(TSETA)DA	GND	(N/C)
13	(TXB)BA	+5	(TSETB)DB
14	(RXB)BB	(N/C)	(RTSB)CA
15	(RSETB)DD	(N/C)	(CTSB)CB
16	(DSRB)CC	(N/C)	(GNDB)AB
17	(DTRB)CD	(N/C)	(RSLDB)CF
18	(TSETB)DA	(N/C)	(N/C)
19	(TXC)BA	(N/C)	(TSETC)DB
20	(RXC)BB	(N/C)	(RTSC)CA
21	(RSETC)DD	(N/C)	(CTSC)CB
22	(DSRC)CC	GND	(GNDC)AB
23	(DTRC)CD	(N/C)	(RSLDC)CF
24	(TSETC)DA	(N/C)	(N/C)
25	(TXD)BA	(N/C)	(TSETD)DB
26	(RXD)DD	(N/C)	(RTSD)CA
27	(RSETD)DD	(N/C)	(CTSD)CB
28	(DSRD)CC	(N/C)	(GND DD)AB
29	(DTRD)DD	(N/C)	(RSL DD)CF
30	(TSETD)DA	(N/C)	(N/C)
31	(N/C)	GND	(N/C)
32	(N/C)	+5	(N/C)

ADDRESS STRAPPING

The VME-SIO module may be configured to reside on any 32 byte boundary within the short I/O page. The short I/O page is at base hex address FF0000 through FFFFFF. Therefore, eleven address lines must be configured by the installer, A15-A5.

All of these address straps are available on the P2 connector per Table 3. By having the straps on P2, the system is configured one time at the backplane and the VME-SIO has no configuration straps at all.

These pins may be configured in any convenient manner on the backplane. The polarity of the pins is logically true. Strap the pins to ground if a zero address is desired; otherwise, allow the pin to remain open. For example, the base address with all pins open is FFFFE0; all pins strapped to ground results in a base address of FF0000.

ADDRESS STRAPPING PINS

Table 3

A5	P2-6a
A6	P2-5c
A7	P2-5a
A8	P2-4c
A9	P2-4a
A10	P2-3c
A11	P2-3a
A12	P2-2c
A13	P2-2a
A14	P2-1c
A15	P2-1a

TEST POINTS

The 8-pin header labeled J1 on the silkscreen is intended for factory test purpose only. No user strapping is required.

SCRAMBLER CABLING

Because of the use of P2 as the interface connector, a cable must be constructed to obtain EIA RS-232 standard pin outs or Mostek standard RS-422 pin outs. This may be done in any manner convenient to the installer.

In order to connect the MK75801-0-01 (4 channels RS-232) to standard RS-232 connectors, refer to Table 4.

In order to make standard connectors to the MK75801-0-02 (2 channels RS-232, 2 channels RS-422), refer to Tables 5 and 6.

MK75602-0-01 TO RS-232 CONNECTOR

Table 4

SIGNAL NAME RS-232	PIN NO. EIA RS-232	VME-SIO P2 PIN CHANNEL NO. a	b	c	d
BA	2	7a	13a	19a	25a
BB	3	8a	14a	20a	26a
CA	4	8c	14c	20c	26c
CB	5	9c	15c	21c	27c
CC	6	10a	16a	22a	28a
AB	7	10c	16c	22c	28c
CF	8	11c	17c	23c	29c
DB	15	7c	13c	19c	25c
DD	17	9a	15a	21a	27a
CD	20	11a	17a	23a	29a
DA	24	12a	18a	24a	30a

MK758010-0-02 2 CHANNELS TO RS-232 CONNECTOR

Table 5

SIGNAL NAME RS-232	PIN NO. EIA RS-232	VME-SIO P2 PIN CHANNEL NO. a	b
BA	2	7a	13a
BB	3	8a	14a
CA	4	8c	14c
CB	5	9c	15c
CC	6	10a	16a
AB	7	10c	16c
CF	8	11c	17c
DB	15	7c	13c
DD	17	9a	15a
CD	20	11a	17a
DA	24	12a	18a

NOTE:
The EIA RS-232 connector is a DB-25 type.

MK758010-0-02 2 CHANNELS TO MOSTEK RS-422 CONNECTOR

Table 6

PIN NO. MOSTEK RS-422	SIGNAL SIGNAL RS-422	SIO PIN ON P2 CHANNEL NO. c	d
5	TXD+	19a	25a
1	TXC+	20a	26a
2	TXC–	20c	26c
8	RXD–	21c	27c
9,10	GND	22c	28c
4	RXC–	23c	29c
6	TXD–	19c	25c
7	RXD+	21a	27a
3	RXC+	23a	29a
		24a	30a

NOTES:
1. The RS-422 pin outs only apply to channels 2 and 3.
2. The Mostek RS-422 connector is a 10 pin header.

APPLICATIONS

The registers of the VME-SIO are summarized in Table 7. Their uses are detailed in the following section.

M1 REGISTER

Since the VME-SIO uses a Z80 serial I/O chip to perform its function, a means of synthesizing the Z80 interrupt behavior was devised. The MK3887 needs a signal called M1* to allow interrupts to be enabled. A Z80 CPU normally would provide this signal. A register is available at hex address 01 relative to the board base address for this purpose.

After enabling interrupts on the MK3887, this register must be written to. The data that is written to this register should be a zero.

If hex data ED followed by 4D is written to this port, the MK3887 serial I/O chip will perform a return from interrupt, resetting all interrupt hardware.

CONTROL REGISTER

The VME-SIO has a Control Register (CR) which contains a variety of functions. It has an offset from the board base address of 03 hex.

CR-LED CONTROL

Bit D7 in the CR controls the led on the edge of the card. A logical zero loaded in this bit lights red, a one lights green. This lamp is intended for use as an indicator for diagnostics performed on the VME-SIO module, but may be used for any indicating function.

CR-SELF TEST

Bit D5 causes the transmit data to be connected to the receive data for each channel. This allows diagnostics to be written to test the VME-SIO.

CR-USER/SUPERVISOR ENABLE

Programming CR bit D6 to a logical one allows the card to be available in user mode. The card is available to the bus in supervisory mode at all times. If programmed to a zero, only the supervisor can access the card. User requests will not generate a DTACK* on the VMEbus when D6 = 0.

CR-INTERRUPT PRIORITY

Bus interrupt priority levels 1-6 may be produced on the VME-SIO. The desired priority level is programmed in CR bits D2, D1, D0.

REGISTER SUMMARY VME-SIO
Table 7

ADDR OFFSET FROM BASE ADDR.	D7	D6	D5	D4	D3	D2	D1	D0	SIO REGISTER
01									M1
03	STATUS LED	USER SUPV	SELF TEST	X	X	IP	NR	TI	CONTROL
05									NOT USED
07									NOT USED
09	X	X	X	SYNC	BR	AA	UT	DE	CHANNEL 0
0B	X	X	X	SYNC	BR	AA	UT	DE	CHANNEL 1
0D	X	X	X	SYNC	BR	AA	UT	DE	CHANNEL 2
0F	X	X	X	SYNC	BR	AA	UT	DE	CHANNEL 3
11									CHANNEL 0 DATA
13									CHANNEL 0 COMMAND
15									CHANNEL 1 DATA
17									CHANNEL 1 COMMAND
19									CHANNEL 2 DATA
1B									CHANNEL 2 COMMAND
1D									CHANNEL 3 DATA
1F									CHANNEL 3 COMMAND

NOTE:
X = bit not used.

BAUD RATE REGISTERS

Baud rates on the VME-SIO are fully programmable. Each channel has an independent register consisting of five bits. Bit 4 selects the source of the Baud rate clock. When programmed to a one level, the clock is provided via the interface. This is the normal case in the synchronous mode. When programmed as a zero, the clock is produced by an on board generator. The rate of this clock is programmed by the remaining four bits in the register as shown in Table 8.

BAUD SELECTION RATE
Table 8

D3	D2	D1	D0	X1	X16	X32	X64
0	0	0	0	800	50	25	12.5
0	0	0	1	1200	75	37.5	18.75
0	0	1	0	1760	110	55	27.5
0	0	1	1	2152	134.5	67.25	33.63
0	1	0	0	2400	150	75	37.5
0	1	0	1	4800	300	150	75
0	1	1	0	9600	600	300	150
0	1	1	1	19200	1200	600	300
1	0	0	0	28800	1800	900	450
1	0	0	1	32000	2000	1000	500
1	0	1	0	38400	2400	1200	600
1	0	1	1	57600	3600	1800	900
1	1	0	0	76800	4800	2400	1200
1	1	0	1	115200	7200	3600	1800
1	1	1	0	153600	9600	4800	2400
1	1	1	1	307200	19200	9600	4800

NOTE:
The selection of the X1, X16, X32, X64 divisor modes is a function of the MK3887 serial I/O chip.

III

CHANNEL DATA REGISTERS

The channel data registers are the actual data registers on the MK3887 SIO components. Refer to the Mostek Z80 Microcomputer Data Book for detailed programming information.

CHANNEL COMMAND REGISTERS

The channel command registers are the actual command (WW0-->WW7, RW0-->RW3) on the MK3887 SIO components. Refer to the Mostek Z80 Microcomputer Data Book for detailed programming information.

ELECTRICAL SPECIFICATIONS

VMEbus DRIVERS

Totem-Pole
V_{OL} = 0.6 V MAX @ 48 ma
V_{OH} = 2.4 V MIN @ 3 ma

Three-state
V_{OL} = 0.6 V MAX @ 48 ma
V_{OH} = 2.4 V MIN @ 3 ma
I_{OH} = 50 μa MAX @ 2.4 V or 0.5 V

Open Collector
V_{OL} = 0.7 V MAX @ 40 ma
I_{OH} = 50 μ MAX @ 5.0 > V > 2.7 V

RS-232 PROTOCOL
RS-422 PROTOCOL

POWER REQUIREMENTS

+5 volts +5%, -2.5% @ 3.5 A max

+12 volts +5%, -3% @ 300 ma typical

-12 volts +5%, -3% @ 300 ma typical

PHYSICAL SPECIFICATIONS

LENGTH	6.30 inches (160 mm)
WIDTH	9.20 inches (233.68 mm)
BOARD THICKNESS	0.062 inches (1.57 mm)
WEIGHT	0.83 lbs. (0.37 kg)

CONNECTORS

96 pin, IEC Standard (603-2 IEC-C096-M)

OPERATING TEMPERATURE RANGE

0 - 60°C

RELATED PUBLICATIONS

The following technical publications may be helpful in using the VME-SIO:

VMEbus TECHNICAL SPECIFICATION
Z80 MICROCOMPUTER DATA BOOK

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
VME-SIO	4 channels RS-232 VMEbus compatible serial I/O board with Technical Manual	MK75801-01-01
VME-SIO	2 channels RS-232, 2 channels RS-422 VMEbus compatible serial I/O board with Technical Manual	MK75801-0-02
VME-SIO Technical Manual	Technical Manual only	4420343

VME-FDC
VME FLOPPY DISK CONTROLLER
MK75803

FEATURES

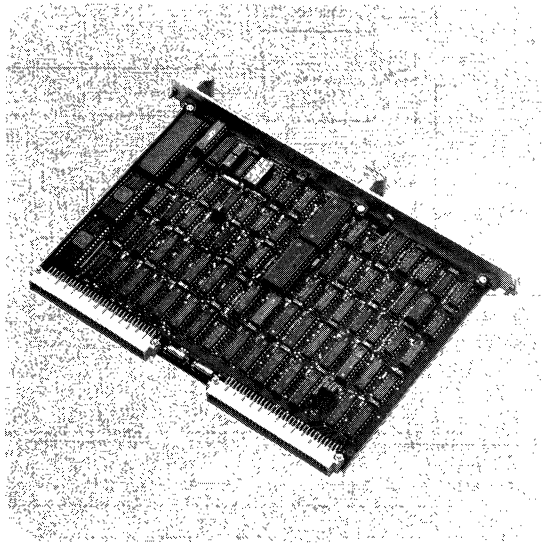
- ☐ VMEbus compatible
- ☐ Word DMA or programmed byte data transfer over VMEbus
- ☐ Programmable to control up to four 8 inch or four 5¼ inch drives
- ☐ Programmable VME Interrupt Priority levels
- ☐ Jumper selectable VMEbus Request level
- ☐ Selectable I/O address on P2 connector
- ☐ Single and Double density formats
- ☐ 5¼ inch Quad density capability
- ☐ Controls single and double sided disk drives
- ☐ Soft sector operation, including variable-length sectors
- ☐ IBM 3740 and System 34 diskette formatting capability
- ☐ Automatic track seek with verification
- ☐ Programmable step rate
- ☐ Single sector, multi sector or full track data transfers
- ☐ Automatic CRC generation and checking
- ☐ Interrupt driven or polled operation
- ☐ Programmable write precompensation
- ☐ 1 Year Warranty

DESCRIPTION

VME-FDC is a floppy disk drive controller board for the VMEbus. The VME-FDC board provides all required controlling, formatting, and interface logic between the VMEbus and one to four floppy disk drives.

VME-FDC can control single or double sided 5¼ or 8 inch Shugart compatible disk drives. Also 8 inch or 5¼ inch drives may be used. All controls to configure the VME-FDC

VME-FDC
Figure 1



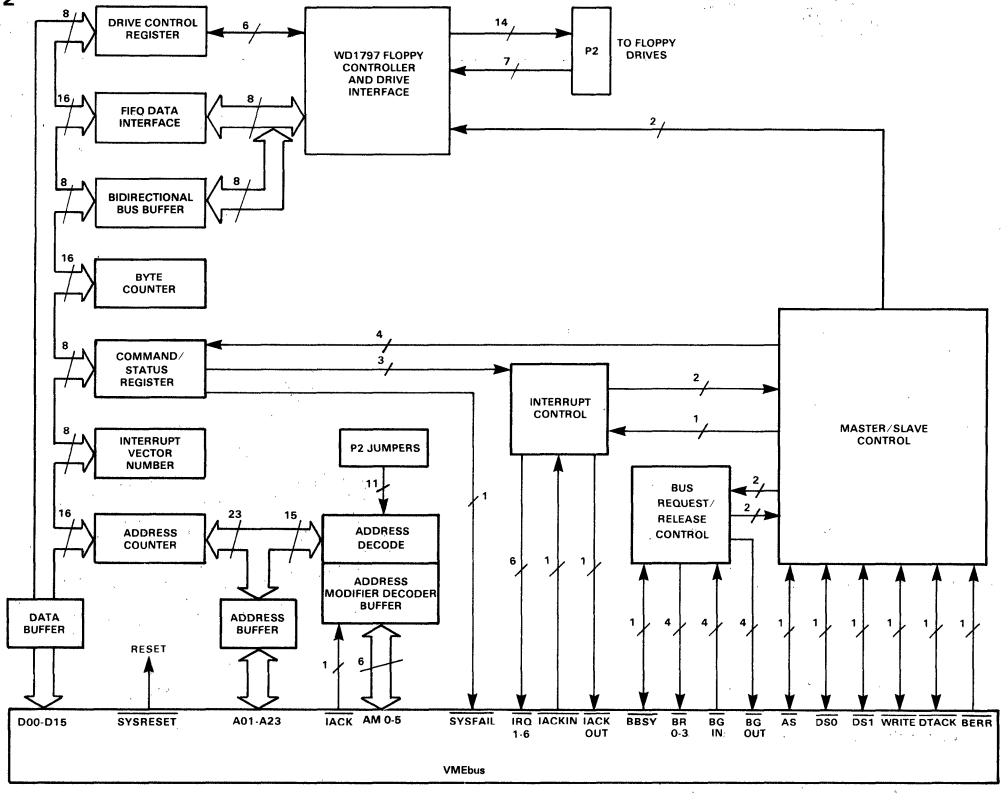
for single or double density format, and 8 inch or 5¼ inch drives and selection of write precompensation are programmable through the on-board drive control register. The capability to use 5¼ Quad density drives is provided by jumper selections.

Transfers are normally performed between the disk and memory in standard addressing space, in a Direct Memory Access (DMA) mode. DMA operations transfer 16 bit words to conserve VMEbus time. Programmed data transfers can also be performed using byte transfers. End of command interrupt requests can be generated on one of the IRQ1-6 lines. Selection of the Interrupt Request level is programmable through the control register. Bus request levels for the DMA transfers are selected by on board jumpers.

The VME-FDC provides a 256 byte FIFO data buffer. The DMA controller writes data to or reads data from the FIFO until the specified number of words are transferred. The FIFO data buffer allows floppy data transfer rates to be buffered between the VMEbus and the disk preventing data overflow/underflow conditions. The FIFO data buffer is not used during programmed data transfers.

VME-FDC BLOCK DIAGRAM

Figure 2



The VME-FDC includes a WD1797 Floppy Disk Contoller chip which provides advanced features including IBM 3740 or IBM System 34 diskette formatting capability, automatic track seek with verification, programmable step rate, and automatic CRC generation and checking. In addition, single sector, multi-sector, or complete track transfers are possible.

The daisy chain bus request and interrupt request configuration of the VMEbus allow multiple VME-FDC boards to be used in a system. Each VME-FDC board I/O address, within short I/O address space, is selected (16 word increments) by jumpering on the P2 connector of the board.

Functional control of the VME-FDC is provided through a control register. Specific control for selection of Interrupts levels, DMA mode, User/Supervisor access, and diagnostic status is provided. A red/green bi-color LED provides the user a means of displaying the diagnostic status of the board.

PHYSICAL SPECIFICATIONS

Board Dimension

Length	6.30 in. (160 mm)
Width	9.20 in. (233.7 mm)
Board Thickness	.062 in. (1.57 mm)

Connectors

96 Pin, IEC Standard (603-2 IEC-C096-M)

ELECTRICAL SPECIFICATIONS

VMEbus compatible
Shugart compatible floppy disk drive interface

Power Supply Requirements

+5 V +5%, -2.5% @ 3.5 A TYP.
+12 V ±5% @ 1 ma Max.

OPERATING TEMPERATURE

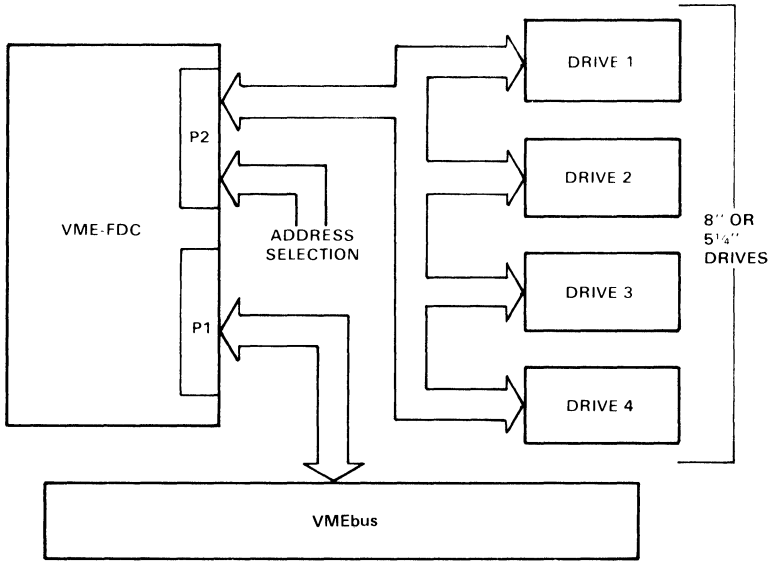
0 to 60°C

HUMIDITY

10% to 90% non-condensing

SYSTEM CONFIGURATION DIAGRAM

Figure 3



ORDERING INFORMATION

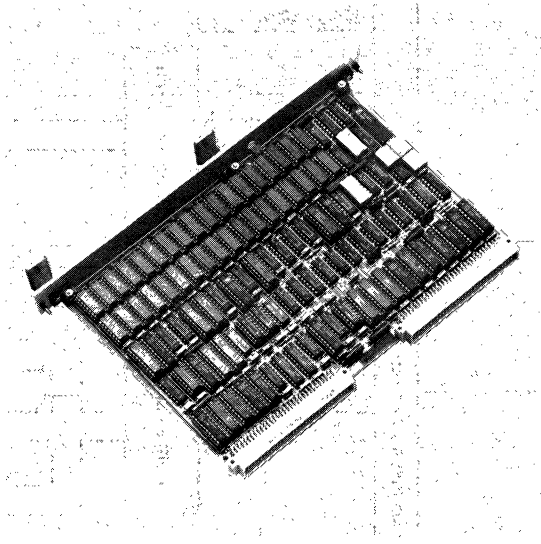
Designator	Description	Part No.
VME-FDC	VME Floppy Disk Controller with Technical Manual	MK75803
VME-FDC Technical Manual	VME-FDC Technical Manual only	4420341

VME-DRAM256
VME DYNAMIC RAM MEMORY CARD
MK75701

FEATURES

- ☐ 256KB of Dynamic RAM
- ☐ 5 V only
- ☐ Byte parity with diagnostic support
- ☐ Control and Status register
- ☐ VMEbus slave
- ☐ 23 bit address
- ☐ Address and data-in latches
- ☐ On-board refresh
- ☐ LED indicates board status
- ☐ Software programmable starting address
- ☐ Byte, word, and longword transfer
- ☐ Dual connector, 160 MM Euro-card format

MK75701
Figure 1



DESCRIPTION

The MK75701 is Mostek's VMEbus compatible dynamic RAM board. The board features self-contained parity generation and checking on all data stored in its array. The Control and Status Register allows software control and diagnosis of board functionality, thus facilitating system diagnostics. The programmable starting address register allows automatic system configuration. Address modifiers are decoded in a PAL which allows the possibility of custom changes in the use of the modifiers. A board edge mounted LED glows green to indicate proper operation of the card and red in the event of a parity error. All refreshing of the dynamic RAM's is controlled automatically by on-board circuits.

SPECIFICATIONS

Power: +5 Vdc at 4.9 A

Capacity: 64K x 36 or 256 K byte

Memory Cycle Types: Read, write, and read-modify-write

Performance:

	Access Time		Cycle Time	
Cycle Type	**Typ**	**Max**	**Typ**	**Max**
Read, Non-parity	388	430	418	460
Read, parity	434	484	464	514
Write	200	236	377	413
Read/Modify/Write	680	776	710	806

Operating Temperature: 0 to 60°C

Storage Temperature: -40 to 125°C

Humidity: 10 to 90% without condensation

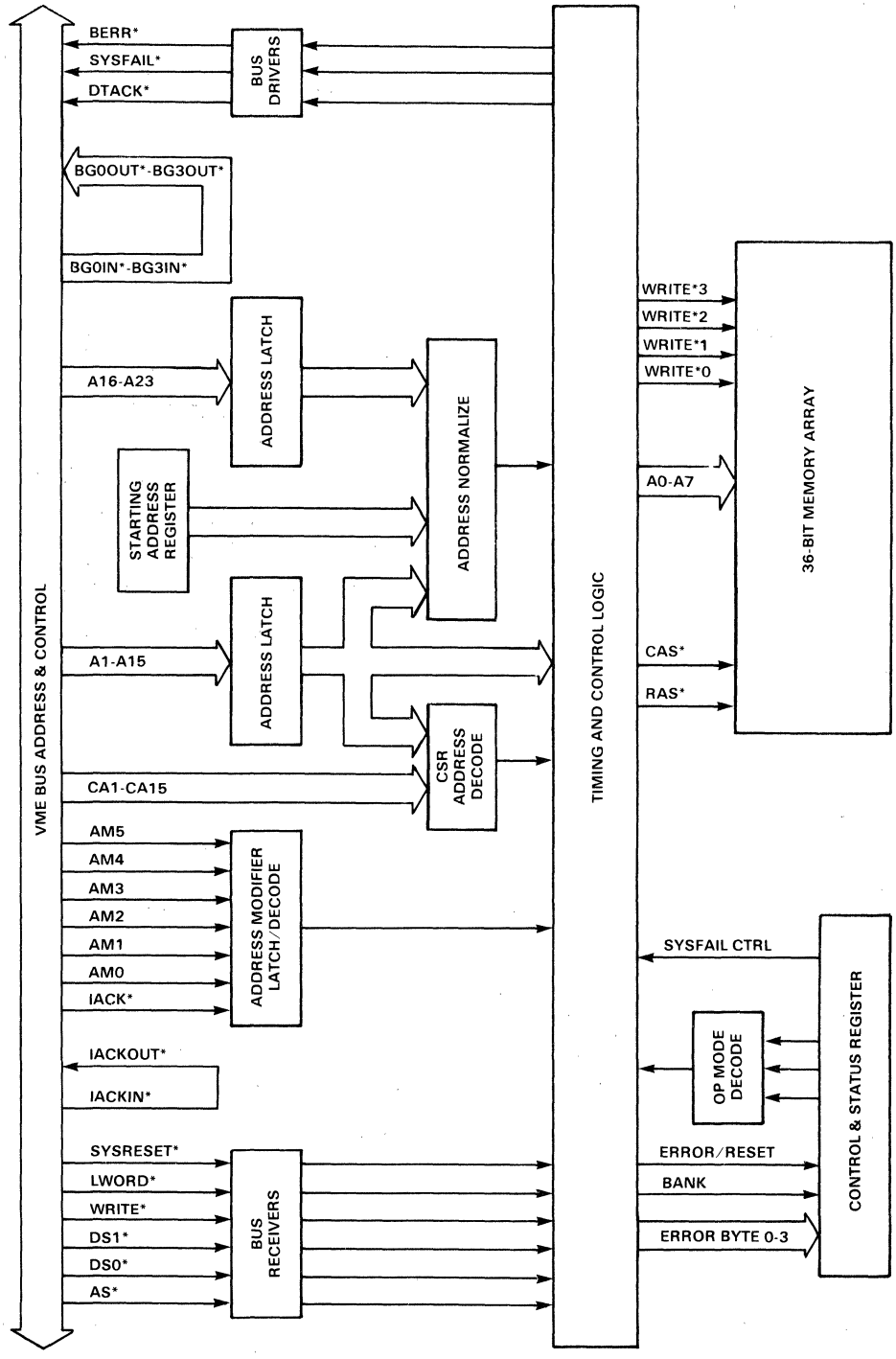
Operating Altitude: 10,000 feet

Dimensions: 160 x 233 mm (6.3 x 9.2 inches)

Compatiblity: VMEbus compatible

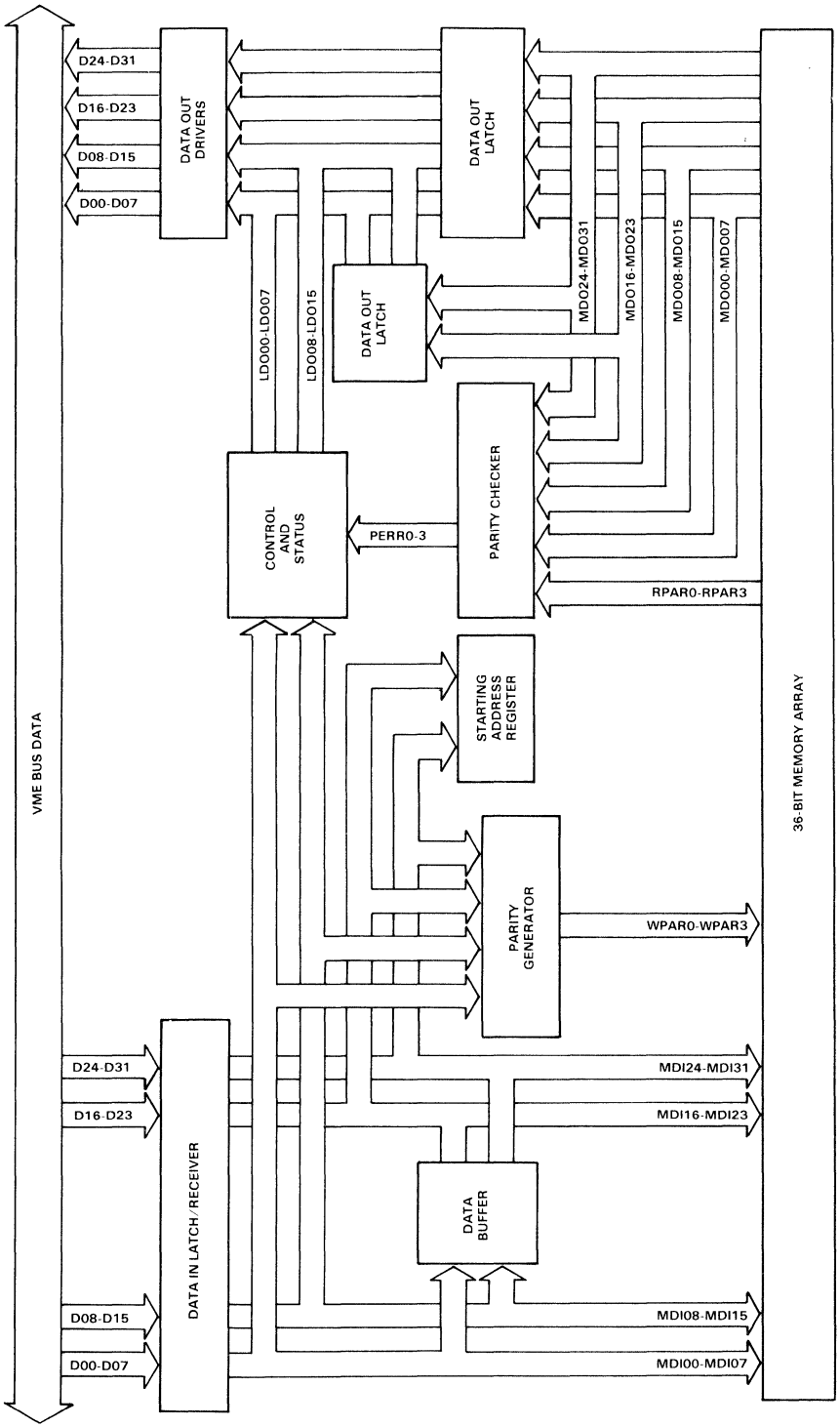
BLOCK DIAGRAM - ADDRESS AND CONTROL

Figure 2



BLOCK DIAGRAM - DATA PATH

Figure 3



III

ORDERING INFORMATION

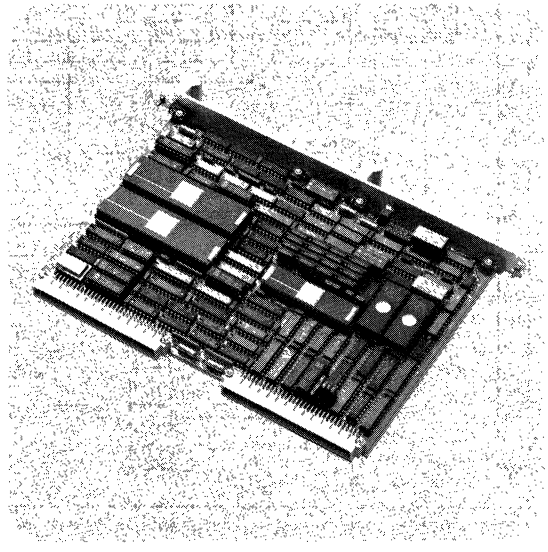
Designator	Description	Part No.
VME-DRAM256	VMEbus compatible memory board with 256 K bytes of Dynamic RAM and Bytewyde parity; includes Technical Manual	MK75701-A-00
VME-DRAM256	VMEbus compatible memory board with 256 K bytes of Dynamic RAM, without parity; includes Technical Manual	MK75701-B-00
VME-DRAM256 TM	Technical Manual only	MK75701-0-ZZ

VME-MMCPU
MEMORY MANAGING CENTRAL PROCESSING UNIT
MK75602

FEATURES

- ☐ VMEbus compatible
- ☐ 68000 Processor and 68451 Memory Management Unit
- ☐ 128K bytes (to 512K bytes) on-board Dynamic Random Access Memory (RAM)
- ☐ Byte parity generation and checking for RAM
- ☐ Dual-port RAM; accessible from 68000 and from VMEbus
- ☐ Programmable VMEbus base address for RAM
- ☐ Programmable response to VMEbus Interrupt Requests 1-7
- ☐ Two on-board (EP)ROM sockets, 16K bytes (to 64K bytes)
- ☐ 8 MHz operation
- ☐ +5 V only
- ☐ 1 year warranty
- ☐ Suitable for multiprocessor systems

VME-MMCPU
Figure 1



The VMEbus was designed jointly by Mostek, Motorola, and Signetics, and was introduced in October, 1981. It offers an attractive combination of high performance timing parameters, compact form factor, and the advanced functional capability appropriate for today's applications of 16-bit microprocessors such as the MK68000. With features such as expansion to 32-bit address and data, an independent serial communications bus, and open-ended transaction coding, it provides for tomorrow's applications as well, assuring the user of a compatible upward growth path for years to come. The international-standard compact board size promotes functional modularity and low board cost, and allows the user to select only those functions needed for his application.

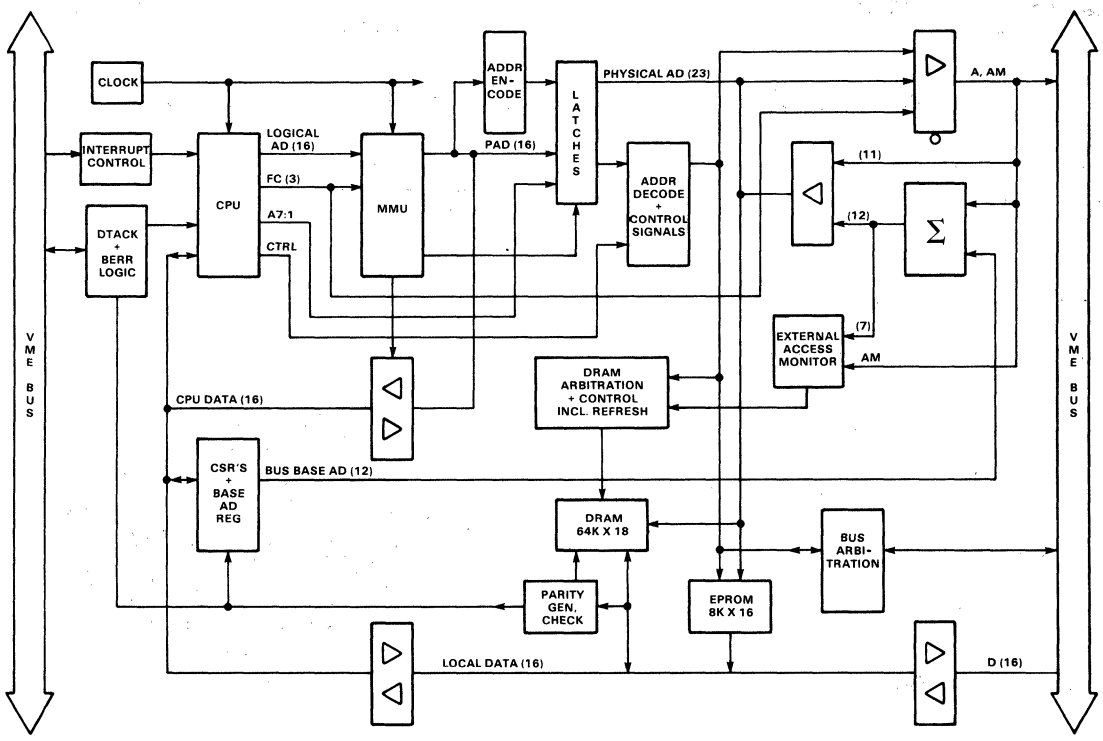
Mostek's VME board product line provides an ever-expanding family of general-purpose modules, applicable to a wide variety of systems and applications including data, word, and image processing, communications, industrial automation and robotics, data acquisition, and software development. For specialized functions provided by other vendors or by the user, Mostek VME boards are totally compliant with the VMEbus Specification, ensuring fully functional operation with all other VMEbus compatible modules.

VME-MMCPU DESCRIPTION

The VME-MMCPU is a state-of-the-art, high density processing element which includes a 68000 processor, a 68451 Memory Management Unit (MMU), and 128K bytes of read-write memory. The DRAM subsystem includes byte parity checking, and can be programmed to be accessible to privileged external masters on the VMEbus. The base address of DRAM on the VMEbus can also be programmed to start at any multiple of 4K bytes.

The MMU stands between the 68000 and all on-board and off-board elements of the system, providing address mapping and access privilege checking on all cycles. The MMU "completes" the architecture of the 68000 by providing a meaningful distinction between the Supervisor (operating system) and User (application) modes of operation, as well as allowing a distinction between Code (program) and Data address spaces and segments. Use of a Memory Management facility is essential to prevent inter-

VME-MMCPU BLOCK DIAGRAM
Figure 2



program interference in multi-user systems, and promotes system integrity and thorough checkout of modular software even in dedicated multi-tasking among co-operative programs.

Several features of the MMCPU enhance its applicability to multi-processor systems: the MMU facility, the VMEbus accessibility of on-board RAM at a programmable base address, and the fact that the MMCPU does not request or use the VMEbus except as necessary. Once it has acquired use of the VMEbus, the MMCPU will retain VMEbus control if no other master is requesting the bus, thereby improving performance for subsequent cycles on the VMEbus. Performance in a multi-master or multi-processor system is further enhanced by the fact that the MMCPU will release the Bus Busy signal during a cycle on the VMEbus, allowing overlap of arbitration for the next master with the current data transfer cycle by the MMCPU.

The MMCPU design includes provision for future expansibility in several areas to provide the user with a product with compatible growth potential as future LSI and VLSI devices become available. The design includes provision for the following types of expansion:

RAM: Nine multiplexed address lines are provided, allowing use of 256K DRAM chips when available, for a total on-board read-write memory of 512K bytes.

(EP)ROM: Address jumpering is provided for MK38000 masked ROMs, and for 27128 and projected 27256 type EPROMs, for a total non-volatile memory of 32K bytes (27128) or 64K bytes (MK38000 or 27256).

Speed: The basic design comprehends 10 and 12 MHz operation, with some parts changes, when enhanced-speed MMU's become available.

Additional MMCPU versions including these enhancements are in the planning stages at this time.

In the standard notation put forth by the VMEbus Manufacturers' Group in the VMEbus Specification, the MMCPU is described as follows:

MASTER A24:D16: Drives 23 address lines (16 Mbytes) for Standard Address Space transactions.
Drives 15 address lines (64K bytes) for Short IO transactions.
Drives and monitors 16 data lines, Word and Byte transfers.

SLAVE A24:D16:	Decodes 23 address lines for Standard Address Space transactions. Drives and monitors 16 data lines, Word and Byte transfers.
REQUESTER:	Release on Request (ROR) Early Release capability (during AS* low) Any of R(3), R(2), R(1), R(0) (STAT, jumpered)
INTERRUPT HANDLER:	Any one of IH (x - y) (DYN, programmed) where $1 \leq x \leq 7$ and $x \leq y \leq 7$
ENVIRONMENTAL OPERATING TEMPERATURE:	0 to 60°C ambient (allows for 10°C local rise) HUMIDITY: 0-90% RH.
POWER:	5.5 A max @ + 5.25 VDC (4.3 A typ at +5 VDC)
PHYSICAL CONFIGURATION:	EXP (for power not bus expansion)
PHYSICAL:	Length 6.30 in. (160 mm) Width 9.20 in. (233.7 mm) Board Thickness .062 in. (1.6 mm) Weight 1.15 lb. (0.52 Kg)

III

ORDERING INFORMATION

Designator	Description	Part Number
VME-MMCPU	VME-MMCPU with Technical Manual	MK75602-8 (8 MHz)
VME-MMCPU Data Sheet	VME-MMCPU Data Sheet only	4420374
VME-MMCPU Technical Manual	VME-MMCPU Technical Manual only	4420375

VME BASELINE SYSTEM MK75101

FEATURES

- ☐ 68000 CPU
- ☐ Down load firmware
- ☐ Five RS-232 Channels
- ☐ Two Timer Counters
- ☐ 256K Bytes of Dynamic RAM with byte parity
- ☐ 12.25" high x 19" rack mount or Table Top Enclosure
- ☐ VMEbus compatible backplane with extended address and data paths
- ☐ Seven VMEbus slots available for expansion
- ☐ Two I/O Panels (for serial I/O)
- ☐ Provision for six additional I/O panels
- ☐ 500 watt power supply
- ☐ Provisions for mounting three 5¼" disk drives
- ☐ Monitor/debugger firmware
- ☐ Interfaces optional DEC-host cross-assembler

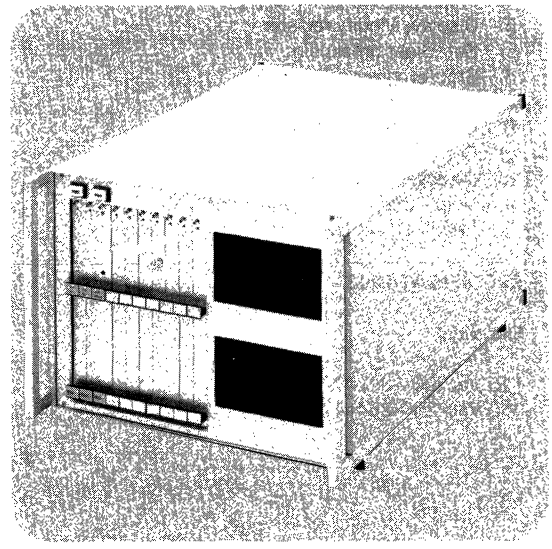
BASELINE DESCRIPTION

The VMEbus Baseline System is intended for use by those people who are developing VMEbus compatible boards. It also allows for evaluation of the VMEbus by providing an electrical baseline, as well as facilitating development of dedicated applications. The system comes standard with a 10 slot VMEbus compatible backplane equipped with three VMEbus boards:

VME-SBC
VME-SIO
VME-DRAM

Together, they provide the 68000 processor, five serial I/O channels, 256K bytes of DRAM, 12K bytes of static RAM, interrupt control, and two timer/counters. The seven remaining slots allow for ample system expansion and board development. There is also provision for mounting three 5¼" disk drives. The standard 500 watt power supply has 420 watts remaining to power drives and additional boards.

VME BASELINE SYSTEM
Figure 1



The system comes standard with a firmware monitor/debugger program. Optional DEC-host software is available for cross-development of 68000 programs.

FIRMWARE

The monitor performs the following functions:

a) Initialization - Sets up and conditions the proto system for use; includes I/O ports and memory boards.

b) Diagnostics - Performs minimal memory confidence tests and a checksum test on the firmware.

c) Transport mode - Allows interfacing to a host system and provides serial down line loading of

68000 binary files in Mostek Hex format or Motorola EXORmacs S-Record format.

d) Error Processing - Handles errors from bus timeout, sysfail, acfail, and I/O errors.

e) I/O Drivers - Provides interface to console device and serial down line load channel.

The debugger supports the following commands:

a) Display/Modify memory
b) Display/Modify register
c) Set/Clear breakpoint
d) Start program execution
e) Step program
f) Fill, Locate, Verify memory contents
g) Convert hex to/from decimal
h) Disassembler
i) Help - Command usage summary
j) Read - Down load a program

SPECIFICATIONS

Electrical

115 Vac (90-132) 47-63 Hz
230 Vac (180-264) 47-63 Hz

~115 watts (this configuration)
720 watts (maximum)

Physical

Height - 12.4 inches (315 mm)
Length - 25.9 inches (658 mm)
Width - 17.9 inches (455 mm)
Weight - 65 Pounds (29.5 kgs)

Environmental

Maximum ambient temp. with disk drives - 30°C
Maximum ambient temp. without disk drives - 45°C

ORDERING INFORMATION

DESCRIPTION	PART NO.
Baseline 115 V Table Top	MK75101-8-11
Baseline 115 V Rack Mount	MK75101-8-21
Baseline 230 V Table Top	MK75101-8-12
Baseline 230 V Rack Mount	MK75101-8-22

IV STD-Z80 Bus

STD-Z80 BUS SYSTEMS

INTRODUCTION

The STD BUS concept is a joint design between Mostek and Pro-Log to satisfy the need for cost-effective OEM Microcomputer Systems. The definition of the STD BUS and the MD Series™ of OEM microcomputer modules is a result of years of microcomputer component and module manufacturing experience. The STD BUS uses a motherboard interconnect system concept and is designed to handle any MD Series™ card in any card slot. Modules for the STD BUS range from CPU, RAM, and EPROM Modules to Input, Output, A/D, and TRIAC control modules.

Printed circuit modules for the STD BUS are a compact 4.5 x 6.5 inches providing for system partitioning by function (RAM, PROM, I/O). This smaller module size makes system packaging easier while increasing MOS-LSI densities provide high functional capability per module. Mostek has defined the STD-Z80 BUS which is a subset of the general-purpose STD BUS. This bus is defined extensively for the Z80 microprocessor and its supporting peripherals. By specifying the STD-Z80 BUS, exact functional pin descriptions and bus timing can be given. A STD-Z80 system will be guaranteed to work with all STD-Z80-designed boards. The STD-Z80 BUS fully supports the powerful Mode 2 interrupt capability of the Z80 microprocessor.

The MD Series™ provides both STD-Z80 BUS expandable modules, designated as MDX, and single-board stand-alone modules, designated as MD. For those applications requiring bus expandability, the MDX-CPU series provides that capability; if a single-board microcomputer is sufficient, the MD-SBC1 provides the system designer with a powerful Z80-based microcomputer solution.

The MD Series™ of OEM microcomputer boards and the STD-Z80 BUS offer the most cost-effective system configuration available to the OEM system designer.

BUS PIN	MNEMONIC	DESCRIPTION
1	+5 V	+5 Vdc system power
2	+5 V	+5 Vdc system power
3	GND	Ground-System signal ground and DC return
4	GND	Ground-System signal ground and DC return
5	-5 V	-5 Vdc system power (see Note 1)
6	-5 V	-5 Vdc system power
7	D3	Data Bus (Tri-state™, input/output, active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices.
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	
15	A7	Address Bus (Tri-state™, bidirectional active high). A0-A15 make up a 16-bit address bus. The address bus provides the address for memory (up to 65K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to select directly up to 256 input or 256 output ports. A0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories.
16	A15	
17	A6	
18	A14	
19	A5	
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	
25	A2	
26	A10	
27	A1	
28	A9	
29	A0	
30	A8	
31	WR*	Write (Tri-state™, active low). WR* indicates that the data bus holds valid data to be stored in the addressed memory or I/O device.
32	RD*	Read (Tri-state™, bidirectional, active low). RD* indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	IORQ*	Input/Output Request (Tri-state™, bidirectional active low). The IORQ* signal indicates that the address bus holds a valid I/O address for an I/O read or write operation. If STATUS 1* is also asserted, the IORQ* signal indicates the vector acquisition phase of the interrupt acknowledge cycle. Interrupt Acknowledge operations occur during M1* time, while I/O operations never occur during M1* time.

Tri-state is a trademark of National Semiconductor Corporation.
*following the signal nmemonic means a low active state.

NOTE:
1. Pin #5 may be redesignated as Battery Voltage (V_{BAT}) in the future by the STD-BUS Manufacturer's Group.

BUS PIN	MNEMONIC	DESCRIPTION
34	MEMRQ*	Memory Request (Tri-state™, bidirectional, active low). The MEMRQ* signal indicates that the address bus holds a valid address for a memory read or memory write operation. It is used on memory cards and is gated with RD*, REFRESH*, or WR* to designate memory operations.
35	IOEXP	I/O Expansion (high expand). A low signal enables primary I/O operations. When high, this signal expands I/O port addressing.
36	MEMEX	Memory Expansion (high expand). A low signal enables primary system memory. When high, this signal expands memory addressing.
37	REFRESH*	REFRESH (Tri-state, output, active low). REFRESH* indicates that the lower 7-bits of the address bus contain a refresh address for dynamic memories and the MEMRQ* signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle, A7 is a logic 0 and the upper 8-bits of the address bus contain the I register.
38	MCSYNC*	Not generated by the MOSTEK CPU cards. MCSYNC* can be generated by gating the following signals: RD* + WR* + INTAK*. By connecting a jumper on the MDX-CPU1, 1A, 2, 2A, this line becomes DEBUG* (Input). DEBUG* is used in conjuction with the DDT-80 operating system on the MDX-DEBUG card and the MDX-SST card for implementing a hardware single step function. When pulled low, the DEBUG* line will set an address modification latch which will force the upper three address lines A15, A14, and A13 to a logic 1. These address lines will remain at a logic 1 until reset by performing any I/O operation.
39	STATUS 1 (M1)*	Machine Cycle One. (Tri-state, output, active low.) M1* indicates that the current machine cycle is in the op code fetch cycle of an instruction. Note that during the execution of two byte opcodes, M1* will be generated as each op code is fetched. These two byte opcodes always begin with a CBh, DDh, EDh, or FDh. M1* also occurs with IORQ* to indicate an interrupt acknowledge cycle.
40	STATUS 0*	Not used on Mostek MD cards.
41	BUSAK*	Bus Acknowledge (Output, active low). Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.
42	BUSRQ*	Bus Request (Input, active low). The BUSRQ* signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When BUSRQ* is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated and the BUSAK* signal is activated.

BUS PIN	MNEMONIC	DESCRIPTION
43	INTAK*	Interrupt Acknowledge (Tri-state, output, active low). The INTAK* signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus. The INTAK* signal is equivalent to an IORQ* during an M1*.
44	INTRQ*	Interrupt Request (Input, active low). The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip flop (IFF) is enabled and if the BUSRQ* signal is not active. When the CPU accepts the interrupt, an interrupt acknowledge signal INTAK* (IORQ* during an M1*) is sent out at the beginning of the next instruction
45	WAITRQ*	Wait Request (Input, active low). Wait Request indicates to the CPU that the addressed memory or I/O device is not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU. Use of this signal postpones refresh as long as it is held active.
46	NMIRQ*	Non-Maskable Interrupt Request (Input, negative edge triggered). The Non-Maskable Interrupt Request line has a higher priority than the INTRQ* line and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. NMIRQ* automatically forces the CPU to restart to location 0066H. The program counter is saved automatically in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a BUSRQ* will override a NMIRQ*.
47	SYSRESET*	System Reset (Output, active low). The System Reset line indicates that a reset has been generated either from an external reset or the power on reset circuit. The system reset will occur only once per reset request and will be approximately 2us in duration. A system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H, and set Interrupt Mode 0.
48	PBRESET*	Push Button Reset (Input, active low). The Push Button Reset will generate a debounced system reset.
49	CLOCK*	Processor Clock (Output, active low.) Single phase system clock.
50	CNTRL*	Not used on MOSTEK MD cards.
51	PCO*	Priority Chain Output (Output, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

BUS PIN	MNEMONIC	DESCRIPTION
52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bused)
54	AUX GND	Auxiliary Ground (Bused)
55	+12 V	+12 Vdc system power
56	-12 V	-12 Vdc system power

NOTES:

2. Input/Output references of each signal are made with respect to MDX-CPU module.
3. The following signals should have pull-up resistors on the processor board: WR*, RD*, IORQ*, MEMRQ*, REFRESH*, DEBUG*, M1*, BUSRQ*, INTAK*, INTRQ*, WAITRQ*, NMIRQ*, SYSRESET*, PBRESET*, and CLOCK*.

IVA STD Bus Microcomputer Systems

INTRODUCTION

The Mostek MATRIX-80/OEM is a single floppy disk drive based microcomputer system. The system includes the following:

- MATRIX-80/OEM enclosure with power supply
- Fan
- Six-slot card cage (MD-CC6)
- Power cord
- Fuse
- 8-inch floppy disk drive
- MDX-CPU3
- MDX-FLP2 module

System Documentation

A complete set of system documentation is supplied with the MATRIX-80/OEM. This includes the following documents:

GENERAL INFORMATION
MDX-CPU3 Technical Manual. Pub # 4420261
MDX-FLP2 Technical Manual. Pub # 4420262
Schematics MDX-CPU3 #450-01065-10
MDX-FLP2 #450-00923-00

This manual gives a general introduction, unpacking instructions, installation instructions, AC power selection, flexible diskette handling instructions, and maintenance guidelines. Appendix A details the preventive maintenance procedures. Appendix B provides interfacing information to standard terminal equipment.

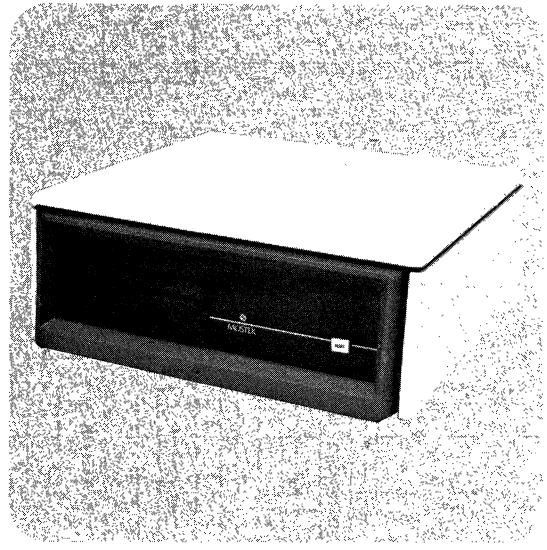
System Software

The MATRIX-80/OEM does not come bundled with any software. The decision as to which software package will be run on the MATRIX-80/OEM is left up to the purchaser. However, it does come with the M/OS-80-5 boot PROM installed on the MDX-CPU3 board for ease of installation of Mostek's operating system M/OS-80.

M/OS-80 is a disk operating system designed to make user computer interaction as simple and self-explanatory as possible. For program development, a set of sub-systems is available to allow user programming. These include FORTRAN, BASIC, PASCAL, and Assembler. For normal use, many packaged applications are available from many sources.

M/OS-80 is "upwards"-compatible with the popular 8080 operating system, CP/M™. M/OS-80 will run virtually all programs designed to run under CPM (version 1.4 through version 2.2). Programs written for other similar systems, such as a Cromemco's CDOS™, are also generally compatible. For a more-complete understanding of the compatibility issue, consult the M/OS-80 Operations Manual Publications #4420064.

MATRIX-80/OEM
Figure 1



IVA

Hardware Description

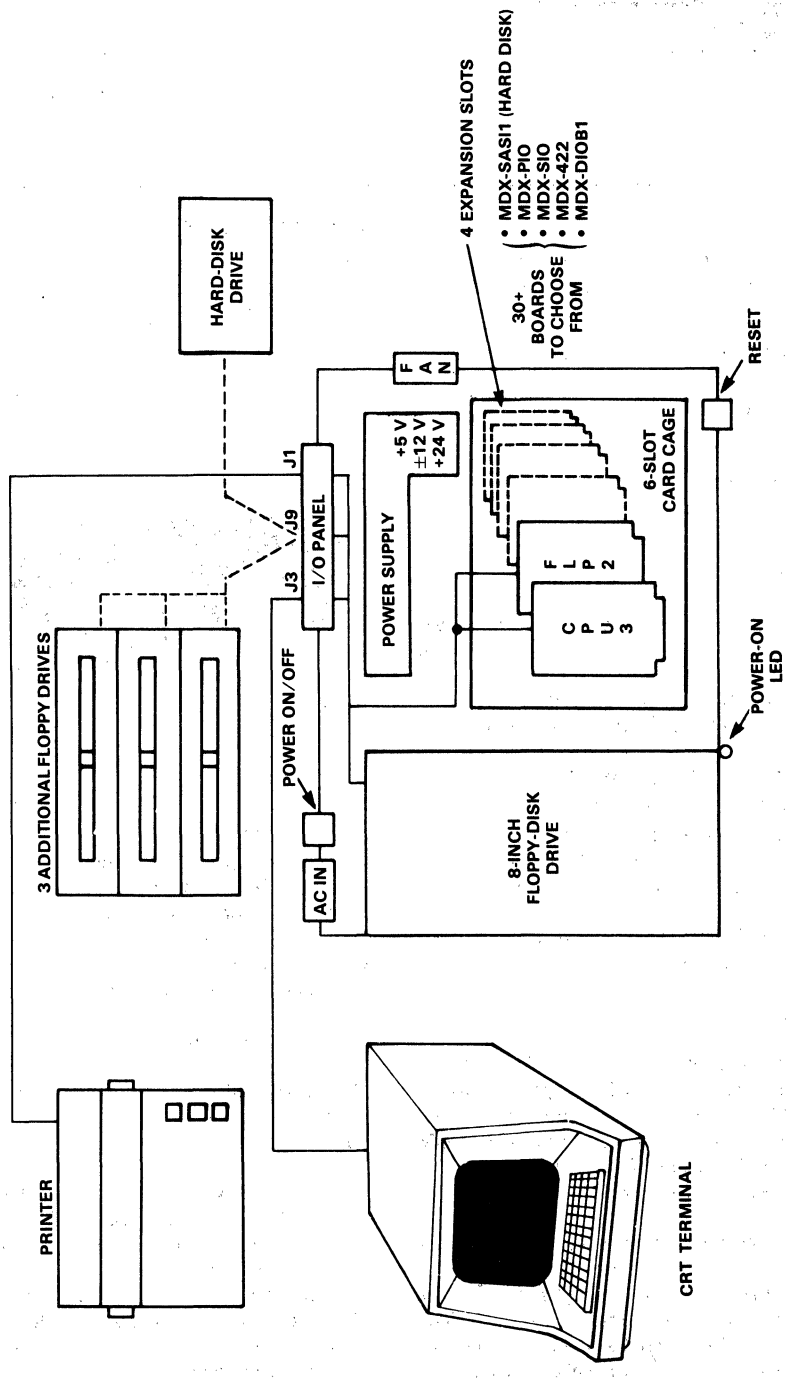
The MATRIX-80/OEM system is based on the MDX family of Microcomputer modules. The two modules used are described below.

1. MDX-CPU3 (MK77857). This circuit board is a STD BUS compatible, Z80 based processing board that contains 64K bytes of Random Access Memory (RAM). It also contains the Z80-STI (Serial Timer Interrupt) device which, with additional on-board circuitry, provides a full function serial I/O port with programmable MODEM controls, an 8-bit parallel printer port, and two timers. A single BYTEWYDE (28-Pin) socket can be strapped to accept most industry-standard memory devices. See Table 1.

The M/OS-80-5 system boot PROM (2716 EPROM) comes installed in the MDX-CPU3 as shipped from the factory. The

MATRIX-80/OEM SYSTEM BLOCK DIAGRAM

Figure 2



STANDARD MEMORY DEVICES

Table 1

EPROMs	ROMs
2716 (2K x 8)	MK34000 (2K x 8)
2732 (4K x 8)	
2764 (8K x 8)	MK37000 (8K x 8)
	MK38000 (32K x 8)

2716 contains the system boot routine to load tracks 0 and 1 from the floppy diskette. It also contains a rudimentary debug monitor to allow the user to:

1. (E)xecute from any location
2. (M)odify and tabulate memory locations
3. (P)ort modify and tabulate

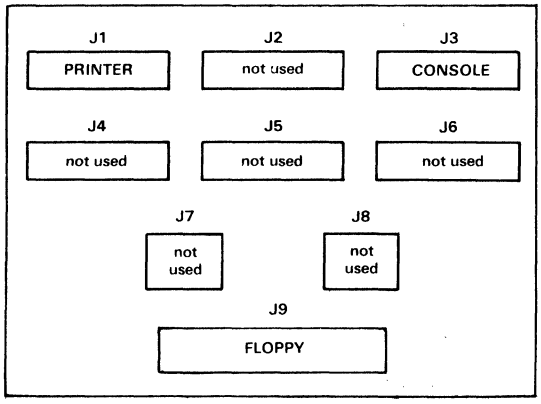
2. MDX-FLP2 (MK77677). This module contains the Western Digital 1797 LSI floppy disk controller and a Mostek MK3883 Direct Memory Access (DMA) device. It provides all required controlling/formatting/interfacing logic between the STD-Z80 BUS and the floppy diskette drives. It can control both single-density, single-sided and double-density, double-sided Shugart compatible drives. In addition, the MDX-FLP2 can control up to four 8-inch or up to three 5¼-inch disk drives. The floppy disk controller is IBM 3740 compatible.

I/O Rear Panel

The input/output (I/O) panel for the MATRIX-80/OEM has cutouts for six (6) 25-pin "D"-type connectors, two (2) 9-pin "D" type connectors, and a 50-pin ribbon connector. The cutouts are labeled J1 through J9. A view of the I/O panel is shown in Figure 3. J3, the serial I/O connector, is compatible with RS-232-C terminal devices. J2, and J4 thru J8 are not used. J9 is an expansion connector for use with additional disk drives and is compatible with the Mostek 60 Hz Dual Floppy Enclosure (MK78183-RMDFSS), or the 50 Hz enclosure (MK78185-RMDFSS-50). Pinouts for J3 are found in Figure 4. The pinouts for J9 are shown in Figure 6.

I/O PANEL (REAR VIEW)

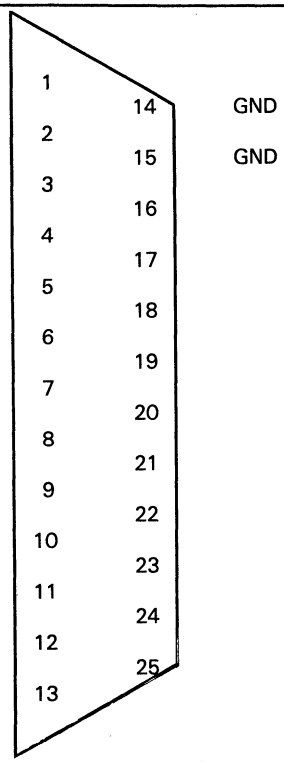
Figure 3



IVA

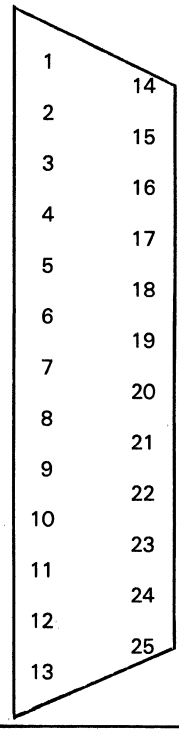
J1 PINOUT (VIEWED FROM MATING SIDE)

Figure 4



J3 PINOUT (VIEWED FROM MATING SIDE)

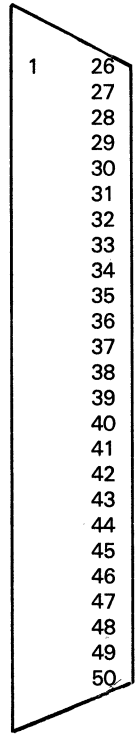
Figure 5



CHASSIS GND			
RECEIVE DATA (input) (RS-232) (BB) from terminal	RDX		
TRANSMITTED DATA (output) (RS-232) (BA) to terminal	TDX		
REQUEST TO SEND (input) (RS-232) (CA)	RTS		
CLEAR TO SEND (output) (RS-232) (CB)	CTS		
DATA SET READY (output) (RS-232) (CC)	DSR		
GROUND	GND		
CARRIER DETECT (output) (RS-232) (CF)	RLSD		
/TIMER C OUTPUT	TCO		
			/TAO (TIMER A OUTPUT)
			DTR DATA TERMINAL RDY (in) (RS-232) (CD)

J9 PINOUT (VIEWED FROM MATING SIDE)

Figure 6



26	/TG43 (TRACK GREATER THAN 43)
27	N/C
28	N/C
29	N/C
30	/2 SIDED
31	N/C
32	/SELECT SIDE 1
33	N/C
34	/HEAD LOAD
35	/INDEX 8-INCH
36	/READY
37	/INDEX 5-INCH
38	/DRIVE SELECT 0
39	/DRIVE SELECT 1
40	/DRIVE SELECT 2
41	/DRIVE SELECT 3
42	/DIRECTION CONTROL
43	/STEP
44	/WRITE DATA
45	/WRITE GATE
46	/TRACK 00
47	/WRITE PROTECT
48	/READ DATA
49	/SELECT SIDE 1
50	N/C

Pins 1 thru 25 are Ground

/ = Active Low

ELECTRICAL SPECIFICATIONS

WORD SIZE - 8 Bits Z80 Microprocessor

MEMORY CAPACITY - 64K bytes

STORAGE CAPACITY - 486K Bytes flexible disk formatted

SYSTEM CLOCK - 3.6864 MHz internal oscillator

BUS - Mostek STD-Z80 BUS

POWER REQUIREMENTS (MAX) - 110 V AC at 2 AMP or
220 V AC at 1 AMP.

OPERATING TEMPERATURE RANGE - 15 - 49° Ambient Celsius

INTERRUPTS - STD-Z80 BUS Prioritized Interrupts

MECHANICAL SPECIFICATIONS

DIMENSIONS -	HEIGHT:	8 inches (20.32 cm)
	WIDTH:	21.1 inches (53.59 cm)
	DEPTH:	20.7 inches (52.57 cm)

WEIGHT - 47 lbs (21.32 kg)

INSTALLATION

This section provides installation instructions for the Mostek MATRIX-80/OEM single disk microcomputer system. Procedures described include unpacking, preliminary checks, and system power up. For more details, refer to specific Technical Manuals (e.g. MDX-CPU3 or MDX-FLP2.)

Unpacking

The MATRIX-80/OEM system should be removed from the shipping container by removing the foam packing material surrounding the enclosure carefully. The soft foam inserts located in the diskette opening should be removed. Open the system by pulling the front bezel off of the system and remove the foam packing supporting the inside enclosure.

Inspection

Inspect the system for shipping damage. Check the printed circuit boards located in the card cage to assure that they are properly seated in the connectors. Check for loose connectors or wires which may have unseated during shipment. In case of shipping damage, place a claim against the shipping agent who delivered the system.

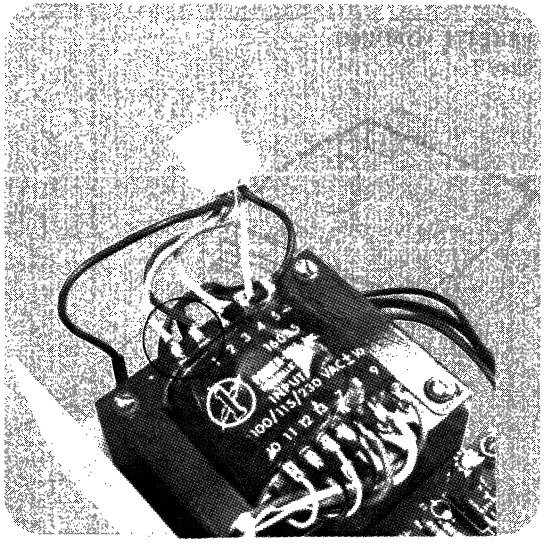
Power Selection

The system has a 115/230 volt power selection switch S2 on the lower right-hand section of the rear panel to select between 115 V ac ± 10% operation or 230 V ac ± 10% operation. Set the switch so that the primary voltage available shows through the hole in the rear panel. The disk drive must be factory configured for either 50 Hz or 60 Hz (verify correct frequency for your installation on the rear panel label).

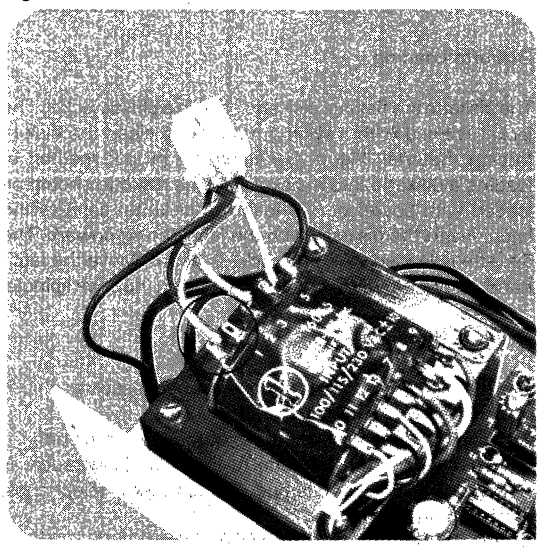
The system can be operated at 100 V ac ± 10%; However, the following wiring changes must be made.

1. Disconnect AC power at the line cord.
2. Remove the top of the unit.
3. Use drawing in Figure 8 to help identify the wires to be moved.

POWER SUPPLY PRIMARY WIRING 115/230 Vac
Figure 7



POWER SUPPLY PRIMARY WIRING 100 Vac
Figure 8



4. Unsolder and move all wires except the blue with white stripe wire from pin 1 on the power transformer to pin 2 of that power transformer.
5. Place the power selection switch (S2) in the 115 volt position.
6. Replace top lid. The system is now configured for 100 volt ± 10% operation.

Baud Rate Selection

Th MDX-CPU3 has the capability of software selectable Baud rates. The system frequency of 3.6864 MHz was chosen to make the range 110 to 9600 Baud rate possible. If the user chooses to use M/OS-80, the driver routine will select the Baud rate set by the terminal within the 110 to 9600 Baud rate range automatically. If a fixed Baud rate is desired, refer to Applications Note # 10 for the fixed Baud rate driver routine.

OPERATION

The MATRIX-80/OEM has been fully tested and burned-in by Mostek prior to shipment. If the unit fails to perform, proceed according to steps outlined in the warranty policy.

Floppy Diskette

The following are recommendations for extending the life of diskettes used in the MATRIX-80/OEM system. Every attempt has been made to design the system for maximum diskette life. However, poor handling practices may cause premature failure of diskette media and/or loss of valuable data.

CAUTION: Do not power the system up or down with a diskette inserted in a disk drive unit. Doing so may destroy the integrity of the data on the diskette. Spurious write pulses may occur which could destroy data on the disk. Also, "RESET" should not be pressed during disk accesses.

Diskette Loading

The diskette is a flexible disk enclosed in a plastic jacket. The jacket is lined with a wiping material to clean the disk of foreign material. Figure 9 shows the proper method of loading a diskette into a disk drive. The diskette should be loaded with power on. To load the diskette, depress the latch, insert the diskette with the label facing upward. The diskette is loaded when a "click" is heard. Move the latch handle down slowly to lock the diskette on the drive spindle.

Diskette Handling

The following are important handling suggestions:

1. Avoid touching exposed areas of magnetic medium.
2. Avoid exposure of diskette to magnetic fields such as motors, fluorescent lamps, transformers, telephones, and so on.
3. Avoid exposure of diskette to direct sunlight. Do not allow its temperature to be changed suddenly over large ranges. Store flexible diskette in an environment that is between 50 degrees F and 125 degrees F with a relative humidity between 0 and 80%.
4. Avoid contamination and warpage by returning the diskette to its envelope when not in use. Store envelope in its box. (verticle is better than horizontal)
5. Avoid placing heavy objects on the diskette.
6. Do not write on the diskette except on label with a felt-tipped pen.
7. Do not attempt to clean the diskette.
8. The flexible diskette should be in the same temperature and humidity enviroment as the disk drive for a minimum of five minutes.

Diskette Unloading

Diskettes are removed from the disk unit by depressing the latch button. The disk unit door will open and the diskette will be pushed out of the unit.

MAINTENANCE

This section deals with the maintenance of the various sub units of the MATRIX-80/OEM system.

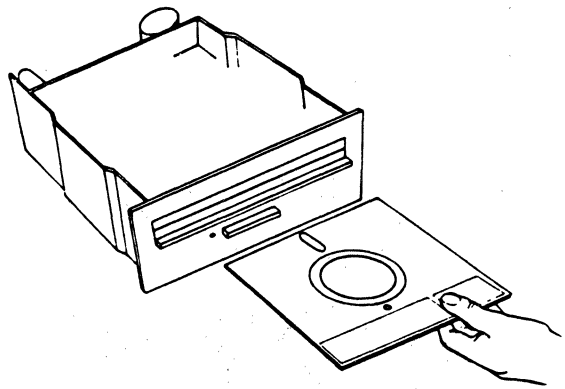
Power Supply

The power supply assembly requires no periodic maintenance. If it is noticed that DC voltages have drifted from the nominal values, adjustment facilities are available on each regulator card. However, this determination should be made only with a high impedance voltmeter at normal operating temperature.

Fan

The temperature within the MATRIX-80/OEM is very important to achieve error-free operation. The diskette

DISKETTE LOADING
Figure 9



material has an operating range of 10 degrees C (50 degrees F) to 49 degrees C (120 degrees F) for prolonged life and error free operation. It is, therefore, important to keep the fans located on the side of each subsystem free from obstructions and in good working order. The power supplies have a 180 degree F thermal breaker and should the temperature inside the unit get too high, the breaker will shut down the system. The fan screen should be cleaned monthly.

CAUTION: Do not operate the MATRIX-80/OEM if the fan is not functioning correctly.

Disk Drive Maintenance

The disk drive requires preventive maintenance every 12 months under normal usage. See Appendix B for complete details. Cleanliness is very important to successful operation of the MATRIX-80/OEM system. The fan should be free from dirt, lint, and so on. Do not lubricate the disk drive unit; oil will allow dust to accumulate. The read/write heads on the disk drive unit should be cleaned only when signs of oxide build-up are present. Oxide build-up will cause premature failure of diskette material. Occasional inspection of read/write heads and diskette will monitor this condition.

Disk Drive Removal

Preventive maintenance or inspection of the drive unit may require its removal from the enclosure. The following procedure describes how to remove the drive.

1. Remove all power from the MATRIX-80/OEM system. **CAUTION: High AC voltages are present within the system even with the AC switch OFF. Remove the line cord from the wall outlet.**
2. Pop off the lid of the system by pulling upward.
3. Remove P1 (signal), P4 (AC), and P5 (DC) connectors from back of the drive. The P4 and P5 connectors are removed by depressing the tabs extending from the side of the connectors.
4. Carefully remove the bezel from around the face of the unit by pulling forward.
5. Remove the front and rear screws (3) holding the bracket below the drive to the baseplate.
6. Remove the disk drive unit out the front of the enclosure.
7. Lay the drive unit upside down on its top and remove the four screws that hold the mounting bracket to the drive frame.
8. To replace the disk drive unit, use the reverse procedure.

TROUBLE-SHOOTING

This section contains a trouble-shooting guide for some specific problems which might occur with the MATRIX-80/OEM system.

SYMPTOMS	THINGS TO CHECK
1. POWER ON indicator does not illuminate.	1. Is there Power to line cord? 2. Is Fuse F1 good? 3. Is LED defective?
2. POWER ON indicator illuminates, fan runs, drive spindle does not turn.	1. Drive belt broken or off pulley 2. AC wiring
3. POWER ON indicator OK fan runs, system returns garbage characters or no characters to the CRT.	1. Is the Baud rate correct? 2. Are the Cable connections good?
4. POWER ON indicator OK fan runs, upon carriage return from the terminal, the floppy diskette seems to read only the first two tracks and quits.	1. Ensure jumpers on FLP2 are correctly installed. J12 should be pins 2-3. 2. Ensure pins 1-8, and 20 are connected from the terminal. (MODEM lines must be connected.)

APPENDIX A
DISK DRIVE PREVENTIVE MAINTENANCE

INTRODUCTION

The prime objective of any Preventive Maintenance (PM) activity is to provide maximum machine availability to the user. Every preventive maintenance operation should assist in realizing this objective. Unless a preventive maintenance operation cuts machine downtime, it is unecessary.

Visual inspection is the first step in every scheduled maintenance operation. Always look for corrosion, dirt, wear, binds, and loose connections. Noticing these items during PM may save downtime later.

Remember, do not do more than recommended preventive maintenance on equipment that is operating satisfactorily.

Preventive Maintenance Procedures

Details of preventive maintenance operations are listed in Figure A1. During the normal preventive maintenance, perform only those operations listed on the chart for that preventive maintenance period. Observe all safety procedures.

Cleanliness

Cleanliness cannot be over-emphasized in maintaining the disk drive unit. Do not lubricate the disk drive; oil will allow dust and dirt to accumulate. The read/write head should be cleaned only when signs of oxide build-up are present.

MAINTENANCE PROCEDURES
Figure A-1

UNIT	FREQ. MONTHS	OBSERVE	ACTION
Read/Write Head	12	Oxide Build-up	Clean Read/Write Head ONLY IF NECESSARY
R/W Head Load Button	12		Replace
Stepper Motor and Lead Screw	12	Inspect for nicks burrs.	Clean off all oil, dust and dirt.
Belt	12	Frayed or weakened areas	Replace
Base	12	Inspect for loose screws, screws, connectors, and switches.	Clean base
Read/Write Head	12	Check for proper Alignment.	

APPENDIX B
PERIPHERAL INTERFACING INFORMATION

INTRODUCTION

This appendix provides peripheral interfacing information. The content of this section will vary according to the customized configuration.

Serial ASCII Terminal

The software driver port assignments will vary with the operating software to be installed by the user. However, the cable signal, and pin out will usually remain similar. The information to build a cable is shown in Table B-1. This cable is available from Mostek - order part number MK78152.

CABLE INFORMATION

Table B-1

RS-232-C/v.24 MDX-CPU3 SIGNAL	I/O CONNECTOR	ASCII TERMINAL	SIGNAL NAME
CHASIS GND	J3-1	EIA-1	AA
RECEIVE DATA	J3-2	EIA-2	BA
TRANSMIT DATA	J3-3	EIA-3	BB
REQUEST TO SEND	J3-4	EIA-4	CA
CLEAR TO SEND	J3-5	EIA-5	CB
DATA SET READY	J3-6	EIA-6	CC
GROUND	J3-7	EIA-7	AB
CARRIER DETECT	J3-8	EIA-8	CF
DATA TERMINAL READY	J3-20	EIA-20	CD

The parts required to build the cable are listed below and are not available from Mostek.

25 pin "D" Connector	ANSLEY #609-25P (2 required)
25 conductor cable	#ANLSEY #171-26 (6 FT long)

Floppy Disk Drive

Table B-2 shows the pinout of various connectors to ease the interface of the floppy disk unit.

CONNECTORS PINOUT

Table B-2

MDX-FLP2 J3 CONNECTOR PIN NO.	I/O PANEL J9 CONNECTOR PIN NO.	FLOPPY DISK SIGNAL NAME
2	26	/TG43
4	27	N/C
6	28	N/C
8	29	N/C
10	30	/2 SIDED
12	31	N/C
14*	32	SELECT SIDE 1
16	33	N/C
18	34	/HEAD LOAD
20	35	/INDEX 8-INCH
22	36	/READY
24	37	/INDEX 5-INCH
26	38	/DRIVE SELECT 0
28	39	/DRIVE SELECT 1
30	40	/DRIVE SELECT 2
32	41	/DRIVE SELECT 3
34	42	/DIRECTION CONTROL
36	43	/STEP
38	44	/WRITE DATA
40	45	/WRITE GATE
42	46	/TRACK 00
44	47	/WRITE PROTECT
46	48	/READ DATA
48*	49	/SELECT SIDE 1
50	50	N/C

*** Pin 14 and 48 are tied together on the MDX-FLP2 board.**

On the MDX-FLP2 board, all odd pins are GND.

On the I/O Panel, pins 1 thru 25 are GND.

Logic Levels are defined at the MDX-FLP2 edge connector.

MATRIX 010, 100
MK78220, MK78221

FEATURES

- 8-inch single-sided, double-density floppy disk drive
- 10-slot card cage, STD BUS compatible
- Multi-disk expansion capabilities
- Fully integrated power supply
- 50 or 60 Hz operation
- 115/230 Vac operation (factory wired)
- Standard 19" rack-mountable chassis
- Optional table-top version
- Front panel power-on indicator

DESCRIPTION

The MATRIX unit is a user-configurable microcomputer system. It provides the user flexibility in packaging and disk storage requirements by offering several configuration options.

The MATRIX unit has a 10-slot card cage, utilizing the STD BUS, power supply, and fan. The power supply provides all the necessary voltages for both the card cage and floppy disk drive. The unit has a structural foam front bezel with quick release ball studs so it can be removed easily. The disk drive may be removed from the front for ease of maintenance. The rear panel has a hinged door for easy access to the 10-slot card cage and has an adjustable strain relief mechanism for cabling to peripherals.

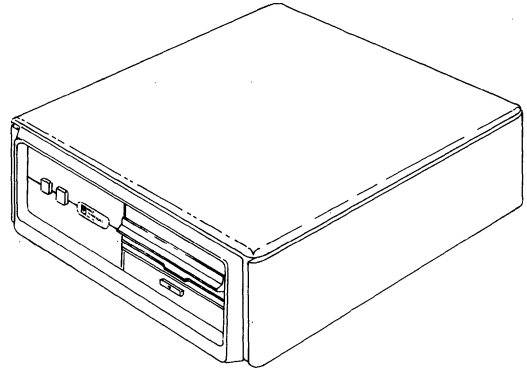
The MATRIX 010 (MK78220) has no disk drive, which allows the unit to be used as a non-disk based system, or the user can add a floppy-disk drive.

The MATRIX 100 (MK78221) has an 8-inch single-sided, double-density floppy-disk drive.

The MATRIX units are available in rack mount or table top versions, with standard 115 or 230 volt operation. The table top version has structural foam side skins and lid.

MATRIX 100, TABLE TOP VERSION

Figure 1



PACKAGING CONFIGURATION

POWER SUPPLY

The power supply provides all the necessary voltages for both the card cage and floppy disk drive. The power supply has the following voltages available:

+5 volts dc at 15 amps maximum
+12 volts dc at 0.5 amp maximum
-12 volts dc at 0.25 amp maximum
+24 volts dc at 3.4 amps maximum

The floppy disk drive (provided on the MATRIX 100) uses +5 volts at 1.0 amp maximum, and +24 volts at 1.7 amps, leaving the following voltages available to the card cage:

+5 volts at 14 amps
+12 volts at 0.5 amp
-12 volts at 0.25 amp

****CAUTION****

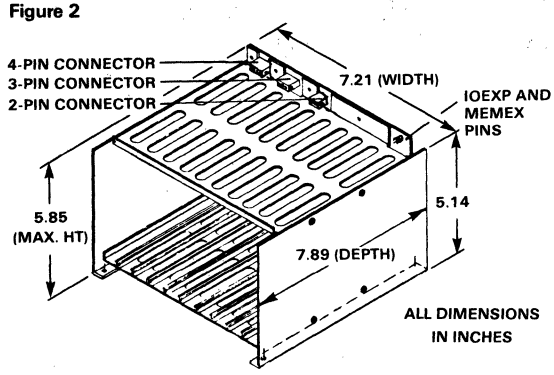
A minimum load of 1.5 amps is required on the primary +5 volt supply in order to ensure proper regulation on the other outputs.

CARD CAGE

The 10-slot card cage is a vertical board mount cage and is fabricated from steel. The card cage is mounted in the rear left-hand side of the MATRIX unit (facing the rear). The back panel contains a hinged door for access to the card cage. Figure 2 is an illustration with dimensions of the card cage.

Power connections to the card cage are provided on the motherboard by a 2-pin and 4-pin AMP Universal MATE-N-LOK connector. There is also a 3-pin AMP Universal MATE-N-LOK connector for connecting a remote power lamp and reset button. The pin assignments for these connectors are shown in Table 1, with holes denoted from the component side left to right.

10-SLOT CARD CAGE
Figure 2



POWER CONNECTOR PIN ASSIGNMENTS
Table 1

CONNECTOR PINS (LEFT TO RIGHT)	DESIGNATOR	STD BUS PIN DESIGNATOR
4-Pin		
1	+5 V	1, 2
2	GND	3, 4
3	-12 V	56
4	+12 V	55
2-Pin		
1	AUX GND	53, 54
2	-5 V	5, 6
3-Pin		
1	GND	3, 4
2	+12 V	55
3	/PBRESET	48

I/O Expand/Memory Expansion

The 10-slot card cage motherboard has two stake pins ($\overline{\text{IOEXP}}$ and $\overline{\text{MEMEX}}$) that are connected to bus pins 35 ($\overline{\text{IOEXP}}$) and 36 ($\overline{\text{MEMEX}}$). If the $\overline{\text{IOEXP}}$ (I/O Expand) pin is not used it should be strapped to the logic ground stake pin opposite pin $\overline{\text{IOEXP}}$. If the $\overline{\text{MEMEX}}$ (memory expansion) is not used it should be strapped to the logic ground stake pin opposite pin $\overline{\text{MEMEX}}$.

Interrupt Priority

The interrupt priority for the 10-slot card cage is from right to left as viewed from the front of the card cage, with the highest priority at the right-most side.

FLOPPY DISK DRIVE

The floppy-disk drive provided on the MATRIX 100 is a Shugart SA800-2 single-sided, double-density unit. A cable is provided with a 50-pin card-edge connector that connects to the internal disk drive, and a 50-pin socket connector for connecting to a controller board (board not provided). The floppy-disk drive is mounted in the front right-hand side of the MATRIX 100 unit.

The MATRIX unit has two mating connectors from the power supply that provide AC and DC power to the floppy disk drive. The DC power mating connector is a 6-pin AMP P/N 1-480270-0 utilizing AMP pins P/N 60619-1. See Table 2 for the 6-pin power designators.

The AC mating connector is a 3-pin AMP P/N 1-480303-0 or 1-480304-0 both utilizing pins P/N 50519-1. See Table 3 for the 3-pin power designators.

6-PIN DC POWER DESIGNATORS
Table 2

PIN	DC VOLTAGE DESIGNATOR
1	+24 Vdc
2	+24 V Return*
3	-12 V Return
4	-12 Vdc
5	+5 Vdc
6	+5 V Return

*The +24 Vdc power requires a separate ground return line. All DC grounds must be connected together near the power supply. One line from this common ground DC connection must go to one common frame ground connection.

3-PIN AC POWER DESIGNATORS

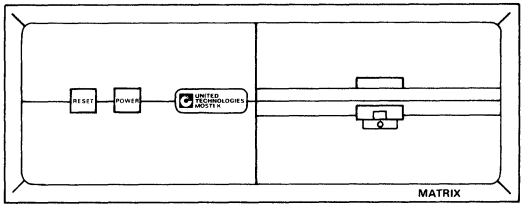
PIN	AC VOLTAGE DESIGNATOR
1	115 Vac
2	Safety GND
3	115 Vac Return

CONTROLS AND INDICATORS

The operator controls and indicators are located on the front panel of the MATRIX unit. This panel contains the POWER ON/OFF and system RESET switches.

The POWER switch, when pressed, applies AC power to the MATRIX unit. This switch is illuminated when the power is on. The RESET switch asserts the $\overline{\text{PBRESET}}$ signal on the STD BUS. Figure 3 illustrates the front panel of the MATRIX unit.

FRONT PANEL OF THE MATRIX UNIT
Figure 3

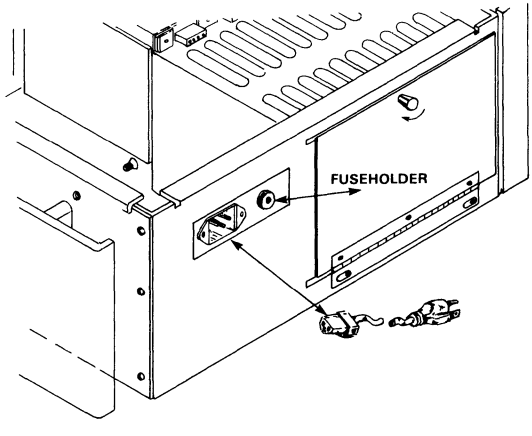


REAR PANEL

The rear panel of the MATRIX unit has a hinged door for easy access to the 10-slot card cage. The hinged door also has an adjustable strain relief mechanism for the cables which connect to peripherals. Figure 4 is an illustration of the MATRIX rear panel.

The left side of the rear panel contains a fuseholder (with fuse) and an AC power cable connector. The MATRIX unit is shipped with a power cord.

REAR PANEL OF THE MATRIX UNIT
Figure 4



DESIGN OPTIONS

The MATRIX unit is designed for use with Mostek MD Series microcomputer boards. A complete line of data processing, memory, input/output boards, and accessories are available from Mostek (see the current Mostek catalog for ordering information).

Mostek also offers a complete line of compatible software products for use with the configured MATRIX unit. Refer to the Mostek Software Catalog for available software.

All Mostek software is available through a licensing agreement to those users who wish to sell it as a part of their own system. All Mostek software is copyrighted and unauthorized copying is prohibited.

*CP/M is a product of Digital Research Corporation

INSTALLATION

UNPACKING AND INSPECTION

The MATRIX unit should be removed from the shipping container by carefully removing the foam packing material surrounding the enclosure.

Inspect the MATRIX unit for shipping damage. Remove the top and check for loose connectors or wires which may have been disconnected during shipment. In case of shipping damage, place a claim against the shipping agent who delivered the unit.

POWER SELECTION

The MATRIX unit is shipped factory wired for either 115 V or 230 V operation.

The 50/60 Hz configuration for the MATRIX is a function of the disk drive selected.

MAINTENANCE

POWER SUPPLY

The power supply assembly requires no periodic maintenance. If the DC voltages drift from nominal values, adjustments can be made. However, this determination should be made only with a high impedance voltmeter at normal operating ambient temperature under load.

FAN

The temperature within the MATRIX unit is very important to achieve error-free operation. The diskette material used on the floppy-disk drive has an operating temperature range of 10°C (50°F) to 49°C (120°F) for prolonged life and error free operation. Therefore, it is important to keep the fan located on the side of the unit free from obstructions and in good working order. The fan screen should be cleaned monthly.

****NOTE****

Do not operate the MATRIX if the fan is not functioning properly.

FLOPPY-DISK DRIVE

Cleanliness cannot be overemphasized in maintaining the disk drive (MATRIX 100). Do not lubricate the disk drive; oil will allow dust and dirt to accumulate. The Read/Write head should be cleaned only when signs of oxide build-up are present. Table 3 provides preventive maintenance procedures and schedule.

Figure 5 shows open space inside the MATRIX 100. When using this space, care should be taken to avoid restricting the air flow and changing the temperature characteristics of the unit.

SPECIFICATIONS

BUS

STD-Z80 BUS

POWER REQUIREMENTS (MAX)

INPUT Power;

115/230 Vac ± 10%, 50 or 60 Hz

DC POWER SUPPLIED:

+5 Vdc at 15 A max.
+12 Vdc at 0.5 A max.
−12 Vdc at 0.25 A max.
+24 Vdc at 3.4 A max.

FUSING

3 Amp, 3 AG for 100/110/115 volts
1.5 Amp, 3AG for 230 volts

OPERATING TEMPERATURE RANGE

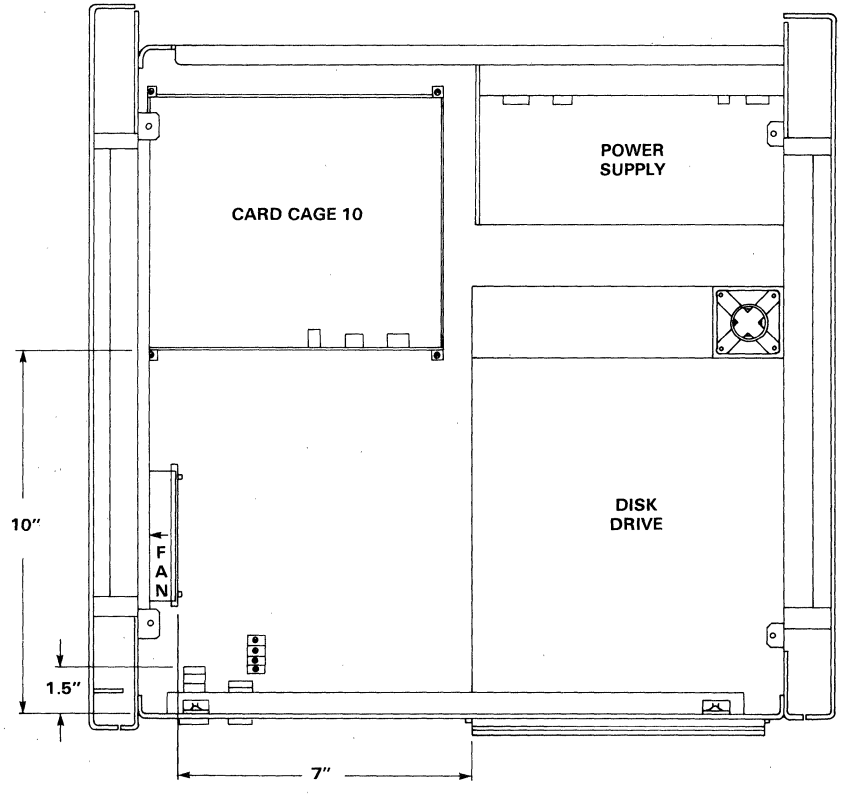
Matrix 010

0°C to 60°C

Matrix 100

4.4°C to 35°C (disk drive limitation) or disk media specification, whichever is more stringent.

INSIDE OF MATRIX UNIT
Figure 5



SPECIFICATIONS (Continued)

INTERRUPTS

STD-Z80 BUS prioritized interrupts

DIMENSIONS

Rack Mount:

Height: 7¾"
Width: 19"
Depth: 22½"

Table Top:

Height: 8¼"
Width: 21"
Depth: 22½"

WEIGHT

45 pounds (21.32 kg.)

DISK DRIVE

Shugart SA800-2 or equivalent (MATRIX 100)

INDICATORS AND CONTROLS

FRONT PANEL INDICATORS

Power-on

FRONT PANEL CONTROL

Power-on switch
Reset switch

REAR PANEL CONTROLS

AC Fuse Holder (with appropriate fuse)
AC Line Receptable/Filter

MOSTEK STD-Z80 BUS PINOUT

COMPONENT SIDE PIN	COMPONENT SIDE MNEMONIC	CIRCUIT SIDE PIN	CIRCUIT SIDE MNEMONIC
1	+5 V	2	+5 V
3	GND	4	GND
5	-5 V	6	-5 V
7	D3	8	D7
9	D2	10	D6
11	D1	12	D5
13	D0	14	D4
15	A7	16	A15
17	A6	18	A14
19	A5	20	A13
21	A4	22	A12
23	A3	24	A11
25	A2	26	A10
27	A1	28	A9
29	A0	30	A8
31	/WR	32	/RD
33	/IORQ	34	/MEMRQ
35	/IOEXP	36	/MEMEX
37	/REFRESH	38	/MCSYNC
39	/STATUS 1	40	/STATUS 0
41	/BUSAK	42	/BUSRQ
43	/INTAK	44	/INTRQ
45	/WAITRQ	46	/NMIRQ
47	/SYSRESET	48	/PBRESET
49	/CLOCK	50	/CNTRL
51	/PCO	52	PCI
53	AUX GND	54	AUX GND
55	+12 V	56	-12 V

PREVENTIVE MAINTENANCE PROCEDURES
Table 3

UNIT	FREQ. MONTHS	OBSERVE	ACTION
Read/Write head	12	Oxide build-up	Clean Read/Write Head ONLY IF NECESSARY
		Check for proper alignment	Align
Read/Write Head Load Button	12	Excessive wear	Replace
Stepper Motor and Lead Screw	12	Inspect for nicks and burrs	Clean off oil, dust, and dirt
Belt	12	Frayed or weakened areas	Replace
Base	12	Inspect for loose screws, connectors, and switches	Tighten screws, connectors, and switches

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MATRIX 010	Rack mountable, user-configurable unit with 10-slot card cage, fan, power supply. 115 V, 60 Hz operation. (Cards not included.)	MK78220-00-00
	Same as above with 230 V, 50 Hz operation	MK78220-01-00
	Table-top version, same as above with 115 V, 60 Hz operation.	MK78220-04-00
	Table-top version, same as above with 230 V, 50 Hz operation.	MK78220-05-00
MATRIX 100	Rack mountable, MATRIX 010 with 8-inch single-sided, double-density disk drive with 115 V, 60 Hz operation.	MK78221-10-00
	Same as above with 230 V, 50 Hz operation.	MK78221-11-00
	Table-top version, same as above with 115 V, 60 Hz operation.	MK78221-14-00
	Table-top version, same as above with 230 V, 50 Hz operation.	MK78221-15-00
SLD-KIT	Slide mounting kit	MK78193

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his measures may be required to correct the interference.

ORDERING INFORMATION

Designator	Description	Part Number
Matrix 80/OEM-RMUS	Single floppy disk drive based Microcomputer System (115 Vac 5 Hz)	MK78231-10
Matrix 80/OEM-RME	Rack mount single floppy disk drive based Microcomputer System (230 Vac 50 Hz)	MK78231-11
Matrix 80/OEM-TTUS	Table top single floppy disk drive based Microcomputer System (115 Vac 60 Hz)	MK78231-14
Matrix 80/OEM-TTE	Rack mount single floppy disk drive based Microcomputer System (115 Vac 50 Hz)	MK78231-15
Matrix 80/OEM Technical Manual	Matrix 80/OEM Technical Manual only	4420345
CPU3 Technical Manual	CPU3 Technical Manual only	4420261
FLP2 Technical Manual	FLP2 Technical Manual only	4420262

MATRIX 200 USER-EXPANDABLE COMPUTER MK78222

FEATURES

- ☐ Z80-based, using STD Bus
- ☐ 64 KB memory
- ☐ Two 8-inch, double-sided, double-density floppy-disk drives
- ☐ 3.2 MB storage capacity (unformatted)
- ☐ Includes:
  - Two cards (MDX-CPU3 single-board computer and MDX-FLP2 floppy disk controller), leaving 8 of 10 slots available for user expansion
  - Centronics-compatible parallel printer interface
  - RS-232C-compatible serial interface
- ☐ Power supply: 115 VAC, 60 Hz or 230 VAC, 50 Hz
- ☐ Standard 19" rack-mount chassis or table-top version
- ☐ M/OS-80, Mostek's CP/M™-compatible operating system is available, providing access to large application software base
- ☐ Also available: Microsoft's Z80 Assembler, BASIC and FORTRAN

DESCRIPTION

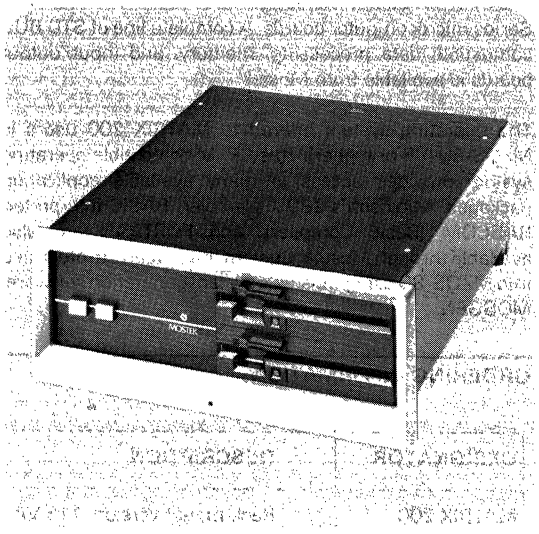
MATRIX 200 is a Z80 based user-expandable micro-computer system targeted for, but not limited to, industrial control and instrumentation applications. It is designed around the industry-proven STD BUS. Both rack-mount and table-top versions are available.

The system contains 64 KBytes of memory. It has two thin-line 8-inch double-sided double-density floppy-disk drives, providing 3.2 MBytes of storage capacity (unformatted). A Centronics parallel printer interface and an RS-232C compatible serial interface are standard with the system.

A card cage with ten slots, only two of which are used, provides for user expansion options. The power supply will operate on 115 VAC, 60 Hz or 230 VAC, 50 Hz. MATRIX 200 complies with FCC requirements.

MATRIX 200, RACK-MOUNT VERSION

Figure 1



The system runs M/OS-80, Mostek's CP/M compatible operating system, thus providing access to a large application software base. Also available through Mostek are Microsoft's Z80 Assembler, BASIC, and FORTRAN.

The boot firmware for M/OS-80 is provided as part of the system. This allows for "phantom" operation, which means that once the system boots, the boot PROM is removed from the address space yielding full 64 KByte address space for program execution.

Another feature included in firmware is a minimum debugger. This provides the capability for memory access, port access, and execution at a given address.

CONTROLS AND INDICATORS

The operator controls and indicators are located on the front panel of the MATRIX 200 unit. This panel contains the POWER and system RESET switches.

The POWER switch, when pressed, applies AC power to the unit. The switch is illuminated when the power is on. The RESET switch resets the SYSRESET signal on the STD BUS.

™ CP/M is a trademark of Digital Research Corporation.

REAR PANEL

The rear panel of the MATRIX 200 unit has a hinged door for easy access to the ten-slot card cage. The hinged door also has an adjustable strain relief mechanism for the cables which connect to peripherals.

The left side of the rear panel contains a fuseholder and an AC power cable connector. (A power cord is shipped with the MATRIX 200.)

DESIGN OPTIONS

The MATRIX 200 unit is designed for use with Mostek MD Series microcomputer boards. A complete line of STD BUS compatible data processing, memory, and input/output boards is available from Mostek.

The operating system offered to MATRIX 200 users is M/OS-80 (V5 or higher). This CP/M compatible operating system provides access to many available application packages. Microsoft's Z80 Assembler, BASIC interpreter, BASCOM (Basic Compiler), and FORTRAN are also available through Mostek. Custom drivers can be integrated into M/OS-80 using Mostek's system generation software, MOSGEN.

POWER

Input: 115/230 VAC 50/60 Hz @ 355 VA

Output: +5 VDC @ 12 A
+12 VDC @ 1.5 A
-12 VDC @ 1.5 A

Available for expansion options:
+5 VDC @ 7.5 A
+12 VDC @ 1.375 A
-12 VDC @ 1.475 A

PHYSICAL DIMENSIONS

Rack Mount:
Height: 7¾"
Width: 19"
Depth: 22½"

Table-Top:
Height: 8¼"
Width: 21"
Depth: 22½"

OPERATING ENVIRONMENT

Temperature: 10°C - 35°C

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MATRIX 200	Rack-mount version; 115 VAC, 60 Hz operation	MK78222-0-20
	Rack-mount version; 230 VAC, 50 Hz operation	MK78222-0-21
	Table-top version; 115 VAC, 60 Hz operation	MK78222-0-24
	Table-top version; 230 VAC, 50 Hz operation	MK78222-0-25

NOTE:
1. All software items must be ordered separately.
2. Other system configurations are available.

1983 COMPUTER PRODUCTS DATA BOOK

MDX-CPU1 AND MDX-CPU1A

FEATURES

- ☐ STD-Z80 BUS-compatible
- ☐ 4K x 8 EPROM (two 2716's, customer-provided)
- ☐ 256 x 8 Static RAM (compatible with DDT-80 debugger)
- ☐ Flexible Memory decoding for EPROM and RAM
- ☐ Four counter/timer channels
- ☐ Restart to 0000H or E0000H (strapping option)
- ☐ Debug-compatible for single step in DDT-80
- ☐ 2.5 MHz version (-0) or 4 MHz version (-4)
- ☐ +5 V only
- ☐ Fully-buffered signals for system expansibility

GENERAL DESCRIPTION

The Mostek MDX-CPU1 is the heart of an MD Series Z80 system. Based on the powerful Z80 microprocessor, the MDX-CPU1 can be used with great versatility in an OEM microcomputer system application. This is done simply by inserting EPROM memories into the sockets provided on the board and configuring them virtually anywhere within the Z80 memory.

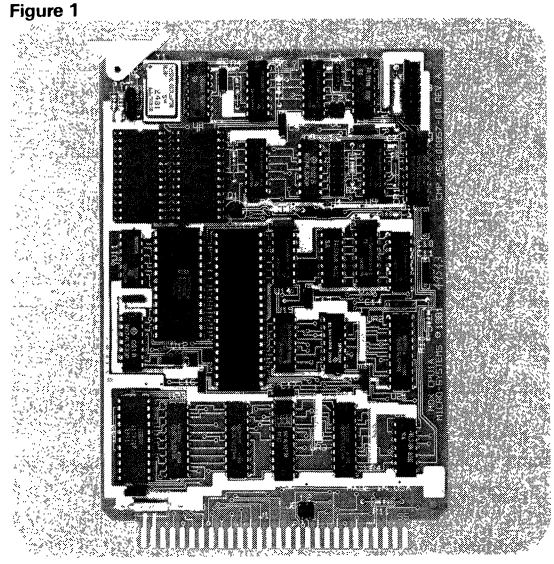
256 bytes of scratchpad RAM are provided on the board and 4K of EPROM can be user provided (2 2716s). In addition, an MK3882 Counter Timer Circuit is included on the MDX-CPU1 to provide counting and timing functions for the Z80.

The MDX-CPU1 can be used in conjunction with the MDX-DEBUG and MDX-DRAM modules to utilize DDT-80 and ASMB-80 in system development.

The MDX-CPU1 is also available in a 4MHz version (MDX-CPU1-4). In this version, one wait state is inserted automatically each time on board memory is accessed by a read or write cycle. This is necessary to make the access times of the 2716 PROMs and the 3539 scratchpad RAM compatible with the MK3880-4 4 MHz Z80-CPU.

MDX-CPU1 AND MDX-CPU1A

Figure 1



There is also a version of this board, CPU1A, which is targeted for the industrial control area. The CPU1A allows system reset to be generated off the board, i.e., from the MDX-PFD. CPU1 does not incorporate this feature. Due to this difference, the user must be aware of the "one-way" compatiblity of these two products. A CPU1A will work in any application in which a CPU1 has been used but the opposite is not the case.

FUNCTIONAL DESCRIPTION

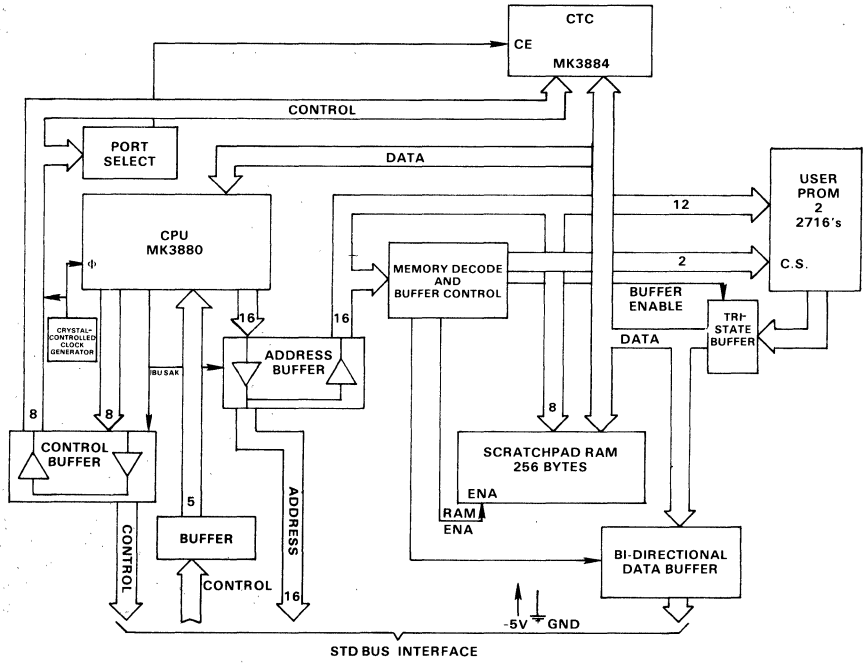
The MDX-CPU1 is designed around the powerful Z80 CPU (3880) chip. A Block Diagram is shown in Figure 2.

CPU

Z80 (MK3880) generates the address and control signals, communicates with memory I/O and peripherals, fetches and executes instructions, and provides most of the timing signals for proper operation of the system.

BLOCK DIAGRAM

Figure 2



COUNTER/TIMER CIRCUIT (CTC)

The counter/timer circuit provides a four channel counter/timer function under software control.

EPROM

Two 24-pin sockets are provided for use with 2716 EPROMs (+5 V only) for an EPROM memory capacity of 4K x 8. This 4K x 8 of EPROM can be strapped on any 2K boundary within any 16K block.

RAM

A 256 x 8 static RAM is provided for general purpose storage and stack pointer operations. The 256 x 8 RAM is located at FF00 to FFFF and can be enabled or disabled via a user installed strap.

CLOCK GENERATOR

The MDX-CPU1 comes with a crystal-controlled clock generator. This clock drives all the necessary components on the board, and is buffered to drive off the board to the other system peripherals. The crystal frequency for the standard MDX-CPU1 card is 5.0 MHz or 8.0 MHz respectively and is divided by two to yield a 2.5 MHz, or to 4.0 MHz or 8.0 MHz respectively.

RESET/RESTART

The MDX-CPU1 can be strapped so that reset execution begins at either 0000H or E000H. This logic is required for use of standard Mostek hardware and software products including DDT-80, FLP-80DOS/, MDX-SST, and MDX-DEBUG.

BUS LINES, (DATA, ADDRESS, CONTROL)

All lines going onto or off of the board are TTL buffered and/or terminated. The data bus lines are bidirectional so that data can go in two directions. The direction of the data bus buffer is controlled by the CPU, so that the data bus buffer will always be enabled out when the CPU is accessing on board memory or the CTC. The data bus buffer will be enabled pointing onto the CPU card when an off-board memory, I/O, or interrupt vector is addressed. The data bus buffer will go to a high impedance whenever a bus-acknowledge signal is issued from the CPU. The address and control lines are unidirectional buffers and will go to a high impedance level whenever a bus acknowledge signal is issued by the CPU.

WAIT STATE GENERATOR

This function, if selected, causes on board memory read and write cycles or I/O cycles to be lengthened by one clock

period in order to allow sufficient access time when slow memory of I/O devices is utilized.

MEMORY INTERFACE

The MDX-CPU can be populated with up to 4K x 8 of EPROM (two 2716s). It comes with a 256 x 8 static RAM that is decoded at FF00H to FFFFH.

EPROM ADDRESS SELECTION
MDX-CPU1 AND MDX-CPU1A

Table 1

	CPU1	CPU1A	CPU1	CPU1A	CPU1	CPU1A
Decoded Address	**U5 Jumpers EPROM U6**	**J3 Jumpers EPROM U6**	**U5 Jumpers EPROM U7**	**J3 Jumpers EPROM U7**	**U10 Jumpers**	**J4 Jumpers**
	Pins	**Pins**	**Pins**	**Pins**	**Pins**	**Pins**
0-7FF	5 to 9	9 to 16	4 to 9	7 to 16	2 to 12	3 to 6
800-FFF	" to 10	" to 14	" to 10	" to 14	and	and
1000-17FF	" to 11	" to 12	" to 11	" to 12	5 to 9	9 to 12
1800-1FFF	" to 12	" to 10	" to 12	" to 10		
2000-27FF	" to 13	" to 8	" to 13	" to 8		
2800-2FFF	" to 14	" to 6	" to 14	" to 6		
3000-37FF	" to 15	" to 4	" to 15	" to 4		
3800-3FFF	" to 16	" to 2	" to 16	" to 2		
4000-47FF	" to 9	" to 16	" to 9	" to 16	Pins	Pins
4800-4FFF	" to 10	" to 14	" to 10	" to 14	9 to 10	12 to 10
5000-57FF	" to 11	" to 12	" to 11	" to 12	and	and
5800-5FFF	" to 12	" to 10	" to 12	" to 10	2 to 12	3 to 6
6000-67FF	" to 13	" to 8	" to 13	" to 8		
6800-6FFF	" to 14	" to 6	" to 14	" to 6		
7000-77FF	" to 15	" to 4	" to 15	" to 4		
7800-7FFF	" to 16	" to 2	" to 16	" to 2		
8000-87FF	" to 9	" to 16	" to 9	" to 16	Pins	Pins
8800-8FFF	" to 10	" to 14	" to 10	" to 14	5 to 9	9 to 12
9000-97FF	" to 11	" to 12	" to 11	" to 12	and	and
9800-9FFF	" to 12	" to 10	" to 12	" to 10	2 to 3	3 to 5
A000-A7FF	" to 13	" to 8	" to 13	" to 8		
A800-AFFF	" to 14	" to 6	" to 14	" to 6		
B000-B7FF	" to 15	" to 4	" to 15	" to 4		
B800-BFFF	" to 16	" to 2	" to 16	" to 2		
C000-C7FF	" to 9	" to 16	" to 9	" to 16	Pins	Pins
C800-CFFF	" to 10	" to 14	" to 10	" to 14	9 to 10	12 to 10
D000-D7FF	" to 11	" to 12	" to 11	" to 12	and	and
D800-DFFF	" to 12	" to 10	" to 12	" to 10	2 to 3	3 to 5
E000-E7FF	" to 13	" to 8	" to 13	" to 8		
E800-EFFF	" to 14	" to 6	" to 14	" to 6		
F000-F7FF	" to 15	" to 4	" to 15	" to 4		
F800-FFFF	" to 16	" to 2	" to 16	" to 2		

There are no EPROMs shipped with these assemblies.

MEMORY DECODING JUMPERS

Decoding for each of the EPROMs is shown in Table 1. The 256 x 8 static RAM may be disabled by disconnecting U5 Pin 2 from U5 Pin 3.

I/O PORTS

Counter/Timer I/O Ports

The CTC I/O ports are hardwired to respond to I/O Ports 7CH, 7DH. 7EH, and 7FH as shown in Table 2. For detailed information on how to program the CTC, refer to the Mostek CTC Technical Manual.

I/O PORT NO. VS. CTC CHANNEL NO.
Table 2

I/O PORT	CTC CHANNEL
$7C_H$	0
$7D_H$	1
$7E_H$	2
$7F_H$	3

RESET/RESTART JUMPERS

The MDX-CPU1 has the capability to reset and begin execution at location 0000H or E000H. Table 3 shows the jumpers for selecting 0000H to E000H was to allow the use of Mostek's DDT-80 (Designer's Development Tool) operating system. However, if DDT-80 is not used, then the reset to E000H can be used for user programs. The jump to E000H is implementing in hardware and must be reset after it is activated. To reset the jump circuitry, the following code must be placed at E0000H:

E000H CS 03 50
E003H DB FF (Any I/O operation will reset the address modification latch)
E000H (User program begins)

When using DDT-80, it is not necessary to execute this code since it is already in the ROM.

RESTART JUMPERS
Table 3

Desired Reset Location	On CPU1 Connect	On CPU1A
0000H	U10 Pin 6 to 7	J4 Pin 11 to 13
E000H	U10 Pin 6 to 8	J4 Pin 11 to 14

WAIT STATE GENERATOR

The wait state circuitry was added to allow 4 MHz operation with standard memory and standard I/O devices. When the wait state circuit is enabled as shown in Table 4, one wait state is inserted in the current timing sequence, either in memory access or I/O operation. Refer to the CPU (MK3880) section of the manual for wait state timing. The wait state circuitry is normally not enabled for 2.5 MHz operation.

Jumper pins, labeled E7 Pins 1-4 have been provided to allow the Memory Expansion and I/O Expansion lines to be tied to ground. This option can be implemented by jumpering these pins as shown in Table 5.

WAIT-STATE JUMPERS
Table 4

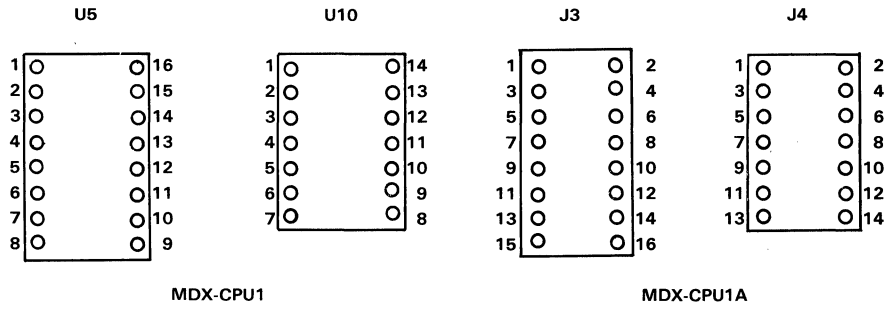
Operation	Wait State	On MDX-CPU1	On MDX-CPU1A
Memory Access	Disabled	(Open) U10 P13-14 E3 to E4	—
Memory Access	Enabled	(Connect) U10 P13 to 14 E3 to E4	(Connect) J4 Pin 2 to 4 J2 Pin 1 to 3
I/O	Disabled	(Open) U10 P13 to 14 E5 to E6	—
I/O	Enabled	(Connect) U10 P13 to 14 E5 to E6	(Connect) J4 Pin 2 to 4 J2 Pin 2 to 4

MEMEX AND IOEXP JUMPERS
Table 5

MEMEX IOEXP	On MDX-CPU1	On MDX-CPU1A
Memory Expansion (MEMEX)	Connect E7 Pin 3 to 4	Connect J6 Pin 2 to 4
I/O Expansion	Connect E7 Pin 1 to Pin 2	Connect J6 Pin 3 to Pin 1

CPU1 AND CPU1A STRAPPING OPTIONS

Figure 3



ASSEMBLY DESIGNATOR DIFFERENCES

Figure 4

Signal	E7	J6	J2	
GND	Pin 1	Pin 1	Pin 1	E3
GND	Pin 3	Pin 4	Pin 2	E6
IOEXP	Pin 2	Pin 3	Pin 3	E4
MEMEX	Pin 4	Pin 4	Pin 4	E5
	MDX-CPU1, MDX-CPU1A		MDX-CPU1A, MDX-CPU1	

IVB

STRAPPING: MDX-CPU1 AND MDX—CPU1A

Both assemblies have the same physical placement of the strapping options. Figure 3 does denote the difference in the numbering scheme used for each assembly. Please note that only the numbering of the headers have been changed and not the routing of the signals to the headers.

Figure 4 further illustrates the difference in these two assemblies designators.

ELECTRICAL SPECIFICATIONS

Word Size

Instruction: 8, 16, 24, or 32 bits
Data: 8 bits
Address: 16 bits

Cycle Time

Clock period or T state
= 0.4 microsecond @ 2.5 MHz for MDX-CPU
= 0.25 microsecond @ 4.0 MHz for MDX-CPU1-4
Instructions require from 4 to 23 T States

Memory Addressing

On-Board EPROM: jumper selectable for any 2K boundary within a 16K block of memory map.
On-Board RAM: FF00-FFFF

Memory Capacity

On-Board EPROM - 4K bytes (sockets only)
On-Board RAM - 256K bytes
Off-Board Expansion - Up to 65,536 bytes, with user-specified combinations of RAM, ROM, PROM

Memory Speed Required

Memory	Access Time	Cycle Time
2716*	450 ns	450 ns

*Single 5-Volt type required

I/O Addressing

On-Board Programmable Timer

PORT ADDRESS (HEX)	MK3882 CHANNEL
7C	0
7D	1
7E	2
7D	3

I/O Capacity

Up to 252 Port addresses can be decoded off-board. (Four port addresses are on-board. 252 + 4 = 256 total I/O ports).

Interrupts

Multi-level with three vectoring modes (Modes 0, 1, 2). Interrupt requests may originate from user-specified I/O or from the on-board MK3882 CTC.

STD-Z80 BUS Interface

Inputs	One 74LS load max
Outputs	I_{OH} = -3 mA min. at 2.4 Volts
	I_{OL} = 24 mA min. at 0.4 Volts

System Clock

	MIN.	MAX.
MDX-CPU1	500 KHz	2.5 MHz
MDX-CPU 1-4	500 KHz	4.0 MHz

Power Supply Requirements

5 V ± 5% at 1.1 A maximum

Operating Temperature

0°C to 60°C

MECHANICAL SPECIFICATIONS

Card Dimensions

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
0.48 in. (1.22 cm) maximum profile thickness
0.062 in. (0.61 cm) printed-circuit-board thickness

Connectors

Function	Configuration	Mating Connector
STD Bus	56-pin dual	Printed Circuit Viking 3VH28/ICE5
	0.125 in. centers	Wire Wrap Viking 3VH28/ICND5 Solder Lug Viking 3VH28/ICN5

ORDERING INFORMATION

Designator	Description	Part No.
MDX-CPU1	Module with Technical Manual less EPROMs. 2.5 MHz version.	MK77850-0
MDX-CPU1	Module with Technical Manual less EPROMs. 4.0 MHz version.	MK77850-4
MDX-CPU1 and 1A Technical Manual	MDX-CPU1 and 1A Technical Manual only.	4420031
MDX-CPU1A	Module with Technical Manual less EPROMs. 2.5 MHz version with Bi-directional SYSRESET	MK77855-0
MDX-CPU1A 4 MHz	Module with Technical Manual less EPROMs. 4.0 MHz version with Bi-directional SYSRESET.	MK77855-4

MDX-CPU2A
MK77856-0, MK77856-4
Z80 CENTRAL PROCESSOR MODULE

FEATURES

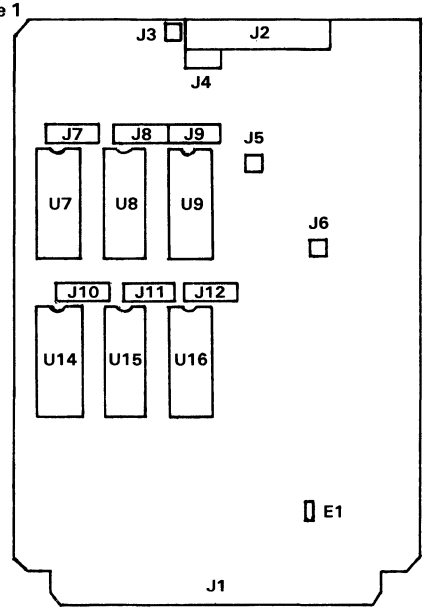
- Utilizes the powerful Z80 Microprocessor
- Six 24-pin sockets are provided which may be strapped to accept any combination of the following industry-standard memory devices:

EPROM	STATIC RAM	ROM
2758 (1K x 8)	MK4118 (1K x 8)	MK34000 (2K x 8)
2716 (2K x 8)	MK4801 (1K x 8)	
2732 (4K x 8)	MK4802 (2K x 8)	

- Memory decoding on any 1K boundary
- Bidirectional address, data, and control busses to permit external DMA
- Four cascadable counter/timer channels
- Automatic, transparent dynamic memory refresh
- Fully buffered signals for system expandablility
- Selectable reset address to either 0000H or E000H
- Selectable wait-state generator
- Bidirectional reset which allows operation with the MDX-PFD (Power Fail Detect)
- 4 MHz version available
- Single +5 Volt supply
- STD-Z80 BUS compatible

CONNECTOR AND HEADER LAYOUT

Figure 1



MDX-CPU2A DESCRIPTION

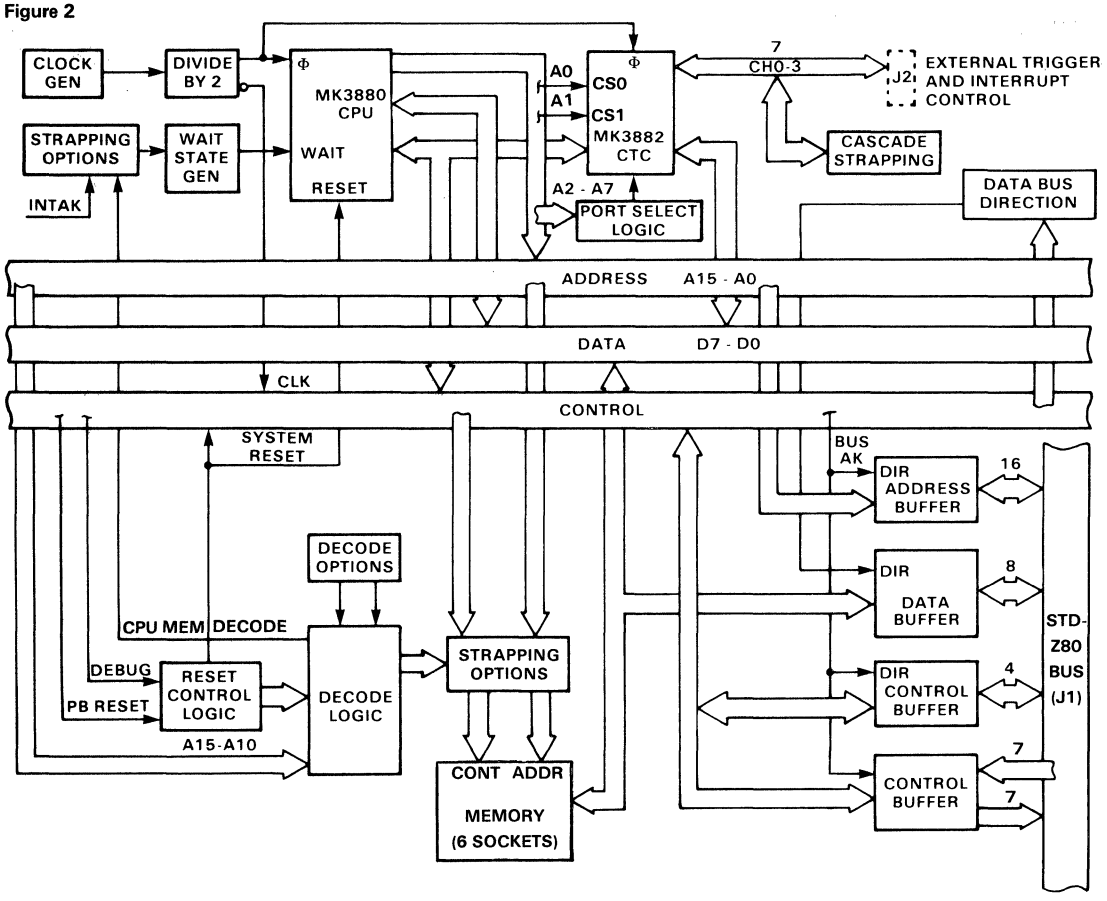
The MDX-CPU2A features six 24-pin memory sockets which enable the user to populate the module with various combinations of ROM, RAM, and EPROM. Flexible address decoding allows the user to configure each memory device within any 1K boundary of the 64K memory map. A decoder PROM is supplied which will allow the user to choose one of four preselected memory configurations or, if desired, the user may, by programming a new decoder PROM, assign any of the six sockets to memory addresses as required by his application needs. Address, data, and control busses have been made bidirectional to allow external masters to directly access CPU memory.

A 4-channel counter/timer circuit (MK3882) is included on board for software controlled counting and timing functions. The counter/timer circuit (CTC) Trigger inputs and Zero Count outputs are buffered and brought out to a connector for external access. In addition, a strapping option makes it possible to cascade the four CTC channels for longer count sequences.

A 4 MHz version of MDX-CPU2A is also available (MDX-CPU2A-4). To ensure sufficient memory access time at 4 MHz operation, a jumper option enables automatic insertion of one WAIT state for those memory devices idenified as "slow" by the decoder PROM. The standard decoder PROM supplied with MDX-CPU2A-4 is pre-programmed for use with MK2716 EPROMs and MK4118 Static RAMs, and identifies 2716 sockets as "slow" and 4118 sockets as "fast".

MDX-CPU2A DIAGRAM

Figure 2



MEMORY REFRESH:

The MDX-CPU2A generates all address and control signals necessary to refresh dynamic RAM (such as MDX-DRAM) modules. Refresh occurs automatically during each OP code fetch cycle and is, therefore, transparent to system throughput.

I/O ADDRESSING

The on-board 4-channel programmable timer is hard-wired to the following port addresses:

MK3882 Channel	Port Address (Hex)
0	7C
1	7D
2	7E
3	7F

I/O CAPACITY:

The MK3880 (Z80-CPU) utilizes the lower 8-bits of its address bus for I/O addressing yielding a total of 256 possible port addresses.

INTERRUPTS:

The MK3880 (Z80-CPU) may be programmed to process interrupts in any of three different modes (mode 0, 1, or 2).

Multi-level interrupt processing is also possible with the MK3880. The level of stacking is limited only by available memory space.

The MDX-CPU2A will also accept nonmaskable interrupts which force a restart at location 0066H.

CONNECTORS AND HEADERS

J1 STD-Z80 BUS

56-Pin (see STD-Z80 BUS description). Pins not connected: 5, 6, 35, 36, 40, 50, 53-56.

J2 CTC Connector

The CTC signals are buffered and brought out to connector J2.
Logical low .5 V at 24 mA
Logical high 2.4 V at –3 mA

Pin	Function
1	CLK/TRG 0
2	ZC/TO 0
3	CLK/TRG 1
4	ZC/TO 1
5	CLK/TRG 2
6	ZC/TO 2
7	CLK/TRG 3
8	NC
9	*NMI
10-13	NC
14-26	GND

*The CPU will respond to an externally generated non-maskable interrupt. The signal is logically OR'ed with NMIRQ, (pin 46) on the STD-Z80 BUS.

J3 Memory Address Decoder

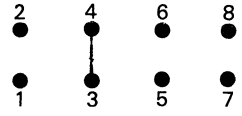
One of four different memory configurations is selected by J3. Additional memory may be added on the STD-Z80 BUS to a maximum of 64K byte total. See Table 1 for J3 strapping.

J4 CTC Channel Cascading

J4 allows cascading of the CTC channels.

Pin	Function
1	NMI (see J2)
2	CLK/TRG 0
3	ZC/TO 0
4	CLK/TRG 1
5	ZC/TO 1
6	CLK/TRG 2
7	ZC/TO 2
8	CLK/TRG 3

J4 Strapping



Example showing channels 0 & 1 cascaded

Note: If the CTC channels are cascaded on J4, the corresponding pins of J2 must be left open.

IVB

J3 STRAPPING

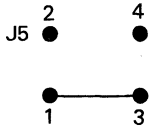
Table 1

	Option 0			Option 1			Option 2			Option 3		
												
	BEG			BEG			BEG			BEG		
	Size	ADDR	Speed	Size	ADDR	Speed	Size	ADDR	Speed	Size	ADDR	Speed
U7	2K	0000	Slow	2K	0000	Slow	2K	E000	Slow	2K	0000	Slow
U8	2K	0800	Slow	2K	0800	Slow	2K	E800	Slow	2K	0800	Slow
U9	1K	F000	Fast	1K	1000	Slow	1K	F000	Fast	1K	1000	Slow
U14	1K	F400	Fast	1K	1800	Slow	1K	F400	Fast	1K	1800	Slow
U15	1K	F800	Fast	1K	F800	Fast	1K	F800	Fast	1K	2000	Slow
U16	1K	FC00	Fast	1K	FC00	Fast	1K	FC00	Fast	1K	FC00	Fast

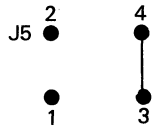
J5 Reset Address Strapping

J5 sets the reset address to 0000H or E000H. If reset address E000H is selected the first instruction in the program at E000H must be a jump to E003H. Then, an I/O read must be performed before any address below E000 is accessed. If no I/O access is required in the program, then a "dummy" I/O read or write to an unused port address must be inserted.

Example	Address	Code	Instruction
	E000	C303E0	JP E003H
	E003	DBnn	IN A, (nn)
	E005		First instruction of user program.



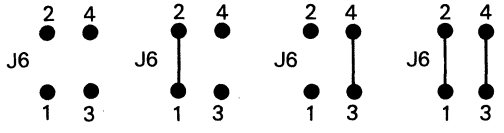
Reset Address 0000H



Reset Address E000H

J6 Wait State Generator

One wait state must be inserted for on-board memories which are designated "slow" for memory access time.



No wait states

One wait state for selected on-board memories.

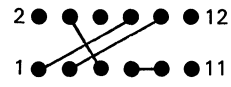
One wait state for interrupt acknowledge cycles.

One wait state inserted for both cases.

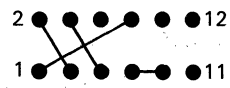
J7-J12 Memory Configuration Headers

Each header configures one socket for a particular type of memory device.

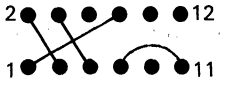
Jumper	J7	J8	J9	J10	J11	J12
Socket	U7	U8	U9	U14	U15	U16



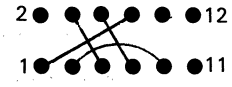
2758 EPROM



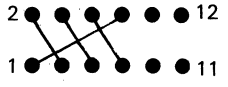
2716 EPROM
MK34000 ROM



2732 EPROM



MK4118/4801 SRAM



MK4802 SRAM

E1

Pin 1 and 2 of the E1 header must be connected when the MDX-SST is used.

MEMORY ACCESS TIME

The time required to access on-board CPU2A memory by external DMA controllers is typically 106 ns plus the access time of the memory device. This is defined as the time interval between the time memory address is valid on the STD BUS and the time output data is valid on the STD BUS.

Maximum Memory Access Time From Chip Enable

System Clock	No Wait States (Fast)	One Wait State (Slow)
2.5	517ns	917ns
4.0	252ns	502ns

CUSTOMIZING THE MEMORY DECODER PROM

The user may find that the decoder PROM supplied with the MDX-CPU2A does not have a preprogrammed memory map suitable for the user's particular application. In this case, a custom decoder PROM can be programmed.

The primary functions of this PROM are to provide the chip enable for each of the six on-board sockets, indicate whether the device in that particular socket will require a wait-state (should the device have a slow access time or require it for 4 MHz operation), and control the direction of the bus buffers (inward for on-board memory accesses and outward for off-board memory accesses). In addition, this memory decoder PROM will permit four separate memory schemes or maps.

The 256 x 8 PROM can be visualized as four separate 64 x 8 blocks. The two most significant input pins to the PROM (A6 & A7) determine which of the four blocks you will be operating in. The lower six input pins (A0 through A5) are connected to A10 through A15 of the Address Bus. Because it takes address lines (A0 through A10) to address 1024 memory locations, the A10 through A15 address lines will split memory into multiples of 1024 (1K bytes). Each location in the PROM represents a 1K boundary. This is ideal case since we have 64 bytes in each section; each byte will decode a 1K boundary, and we wish to decode a 64K memory map.

Selecting option number 3 (no jumpers on J3), the memory decode PROM is set up for five 2K EPROMs (2716's) to be addressed from 0000H to 27FFH and one 1K device (MK4118 Static RAM) to be addressed from FC00H to FFFFH.

PROM DATA

Table 2

	WAIT STATES WITH	WAIT STATES WITHOUT
CS1 =	3E	7E
CS2 =	3D	7D
CS3 =	3B	7B
CS4 =	37	77
CS5 =	2F	6F
CS6 =	1F	5F
$\overline{CS}$ =	FF	

(All selected memory is off-board)

Looking at Table 2 and the Figure below, we see that the data that should be programmed in the PROM for option #3 should be as follows:

PROM DATA CALCULATIONS

Figure 3

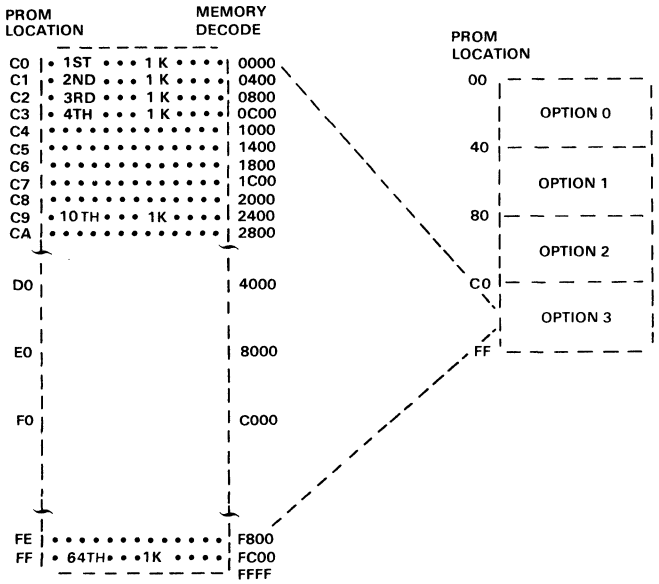
LOCATION	DATA		SOCKET
C0	3E	{	U7 (2716)
C1	3E		
C2	3D	{	U8 (2716)
C3	3D		
C4	3B	{	U9 (2716)
C5	3B		
C6	37	{	U14 (2716)
C7	37		
C8	2F	{	U15 (2716)
C9	2F		
CA - FE	FF	—	No On-board Sockets Selected
FF	1F	—	U16 (MK4118)

This can be verified by comparing this table data to the data found in the MK6289 listing. (The shipped PROM is configured for slow devices, ie wait states are inserted.)

The data to be entered into the PROM is computed by the chart in Table 3. The signal to enable a particular socket is an active low signal. This is indicated by the bar over the signal name (/CS1 etc.) To select the first socket U7, a 0 (low) is the desired condition from output bit 0. Output Bits 1-6 will be 1's to ensure that only one socket is selected at a

MEMORY MAP

Figure 4



particular time. Output Bit 6 is a 0 if the user wants a wait state to be inserted every time this particular socket is accessed. Output Bit 7 controls the buffer direction, so if any socket is selected on-board, this output bit must be a 0 (low.)

PROM DATA CALCULATION

Table 3

OUTPUT BIT	7	6	5	4	3	2	1	0	
FUNCTION	$\overline{\text{ANY CS}}$	$\overline{\text{WAIT}}$	$\overline{\text{CS6}}$	$\overline{\text{CS5}}$	$\overline{\text{CS4}}$	$\overline{\text{CS3}}$	$\overline{\text{CS2}}$	$\overline{\text{CS1}}$	
LOCATION	——	——	U16	U15	U14	U9	U8	U7	
with wait states	0	0	1	1	1	1	1	0	=3E
	0	0	1	1	1	1	0	1	=3D
	0	0	1	1	1	0	1	1	=3B
	0	0	1	1	0	1	1	1	=37
	0	0	1	0	1	1	1	1	=2F
	0	0	0	1	1	1	1	1	=1F
without wait states	0	1	1	1	1	1	1	0	=7E
	0	1	1	1	1	1	0	1	=7D
	0	1	1	1	1	0	1	1	=7B
	0	1	1	1	0	1	1	1	=77
	0	1	1	0	1	1	1	1	=6F
	0	1	0	1	1	1	1	1	=5F
no select	1	1	1	1	1	1	1	1	=FF

PROM DATA PATTERN
MK6289
(NMI 6309-1J 256 x 8)

Table 4

LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA
00	3E	20	FF	40	3E	60	FF	80	FF	A0	FF	C0	3E	E0	FF
01	3E	21	FF	41	3E	61	FF	81	FF	A1	FF	C1	3E	E1	FF
02	3D	22	FF	42	3D	62	FF	82	FF	A2	FF	C2	3D	E2	FF
03	3D	23	FF	43	3D	63	FF	83	FF	A3	FF	C3	3D	E3	FF
04	FF	24	FF	44	3B	64	FF	84	FF	A4	FF	C4	3B	E4	FF
05	FF	25	FF	45	3B	65	FF	85	FF	A5	FF	C5	3B	E5	FF
06	FF	26	FF	46	37	66	FF	86	FF	A6	FF	C6	37	E6	FF
07	FF	27	FF	47	37	67	FF	87	FF	A7	FF	C7	37	E7	FF
08	FF	28	FF	48	FF	68	FF	88	FF	A8	FF	C8	2F	E8	FF
09	FF	29	FF	49	FF	69	FF	89	FF	A9	FF	C9	2F	E9	FF
0A	FF	2A	FF	4A	FF	6A	FF	8A	FF	AA	FF	CA	FF	EA	FF
0B	FF	2B	FF	4B	FF	6B	FF	8B	FF	AB	FF	CB	FF	EB	FF
0C	FF	2C	FF	4C	FF	6C	FF	8C	FF	AC	FF	CC	FF	EC	FF
0D	FF	2D	FF	4D	FF	6D	FF	8D	FF	AD	FF	CD	FF	ED	FF
0E	FF	2E	FF	4E	FF	6E	FF	8E	FF	AE	FF	CE	FF	EE	FF
0F	FF	2F	FF	4F	FF	6F	FF	8F	FF	AF	FF	CF	FF	EF	FF

PROM DATA PATTERN (Continued)
MK6289
(NMI 6309-1J 256 x 8)
Table 4

LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA
10	FF	30	FF	50	FF	70	FF	90	FF	B0	FF	D0	FF	F0	FF
11	FF	31	FF	51	FF	71	FF	91	FF	B1	FF	D1	FF	F1	FF
12	FF	32	FF	52	FF	72	FF	92	FF	B2	FF	D2	FF	F2	FF
13	FF	33	FF	53	FF	73	FF	93	FF	B3	FF	D3	FF	F3	FF
14	FF	34	FF	54	FF	74	FF	94	FF	B4	FF	D4	FF	F4	FF
15	FF	35	FF	55	FF	75	FF	95	FF	B5	FF	D5	FF	F5	FF
16	FF	36	FF	56	FF	76	FF	96	FF	B6	FF	D6	FF	F6	FF
17	FF	37	FF	57	FF	77	FF	97	FF	B7	FF	D7	FF	F7	FF
18	FF	38	FF	58	FF	78	FF	98	FF	B8	3E	D8	FF	F8	FF
19	FF	39	FF	59	FF	79	FF	99	FF	B9	3E	D9	FF	F9	FF
1A	FF	3A	FF	5A	FF	7A	FF	9A	FF	BA	3D	DA	FF	FA	FF
1B	FF	3B	FF	5B	FF	7B	FF	9B	FF	BB	3D	DB	FF	FB	FF
1C	FF	3C	7B	5C	FF	7C	FF	9C	FF	BC	7B	DC	FF	FC	FF
1D	FF	3D	77	5D	FF	7D	FF	9D	FF	BD	77	DD	FF	FD	FF
1E	FF	3E	6F	5E	FF	7E	6F	9E	FF	BE	6F	DE	FF	FE	FF
1F	FF	3F	5F	5F	FF	7F	5F	9F	FF	BF	5F	DF	FF	FF	1F

TECHNICAL SPECIFICATIONS

Card Dimensions:

4.50 in. (11.43 cm) wide by 6.50 in.(16.51 cm) long
0.675 in. (1.71 cm) maximum profile thickness
0.062 in. (0.16 cm) printed circuit board thickness

STD BUS Edge Connector:

56-Dual Readout; 0.125 in. centers

Mating Connectors

PCB - Viking 3VH28/1CE5
Wirewrap - Viking 3VH28/1CND5
Solder lug - Viking 3VH28/1CN5

ELECTRICAL SPECIFICATIONS

STD Bus Compatible

System Interrupt Units:

1 SIU

System Clock

MDX-CPU2A: 2.5 MHz ± 0.05%

MDX-CPU2A-4: 4.0 MHz ± 0.05%

Operating Temperature:
0°C to 60°C

POWER SUPPLY REQUIREMENTS

5 V ± 5% @ 1.2A (excluding memory power requirements)

RELATED PUBLICATIONS

The following are related publications:
System Design Using the Mostek STD-Z80 BUS (User's Manual) - Publication No. 4420237

Z80 Microcomputer Data Book - Publication No. MK79602

ORDERING INFORMATION

Designator	Description	Part No.
MDX-CPU2A	2.5 MHz CPU2A module (less memory and mating connectors)	MK77856-0
MDX-CPU2A-4	4.0 MHz CPU2A module (less memory and mating connectors)	MK77856-4
MDX-CPU2A Data Sheet	Data sheet for MDX-CPU2A and MDX-CPU2A-4	4420259

MDX-CPU3

FEATURES

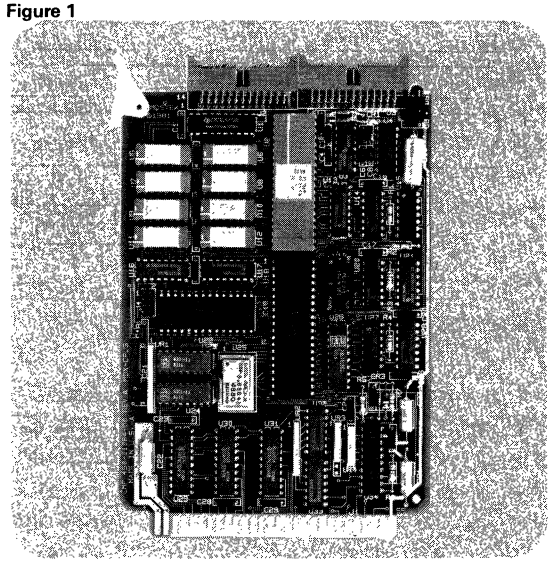
- Z80-STD Bus compatible CPU board
- A 28 pin socket for industry standard Bytewide ROMs or EPROMs
- Flexible memory decoding of ROM/EPROM memory on any 2K boundary
- 64K x 8 of onboard dynamic RAM
- Phantom ROM capability
- Bidirectional address, data, and control busses to permit external DMA to onboard memory
- 8 bit output port with handshake (Centronics printer interface)
- Full handshake serial RS232 I/O Port
- Software programmable Baud rates to 9600 Baud
- Bidirectional power on reset which allows operation with power fail controllers
- Two programmable 8-bit timers with output
- Fully buffered signals for system expansibility
- Supports multiple memory banks
- Supports MEMEX capability

MDX-CPU3 DESCRIPTION

The MDX-CPU3 is a STD-Z80 Bus compatible single board computer with 64K bytes of dynamic RAM, 2K to 32K bytes of ROM/EPROM, an RS232-C serial port, and an 8 bit output port with handshake for connection to a printer. The CPU3 supports a very flexible memory map configuration by the use of a memory configuration PROM. This allows the RAM to be enabled/disabled in 2K byte increments and the ROM/EPROM to be mapped on 2K boundaries anywhere in the 64K memory map. Each different map is selectable under software control. Address, data, and control busses are bidirectional to allow external masters to access memory on CPU3 directly.

MDX-CPU3

Figure 1



The 8 bit parallel output port with handshake lines is configured to accomodate direct connection to a Centronics type printer interface.

The RS232 serial port is configured to accommodate full handshake capabilities (interface type D).

ELECTRICAL SPECIFICATIONS

STD-Z80 BUS COMPATIBLE

SYSTEM INTERRUPT UNITS:

1SIU

SYSTEM CLOCK:

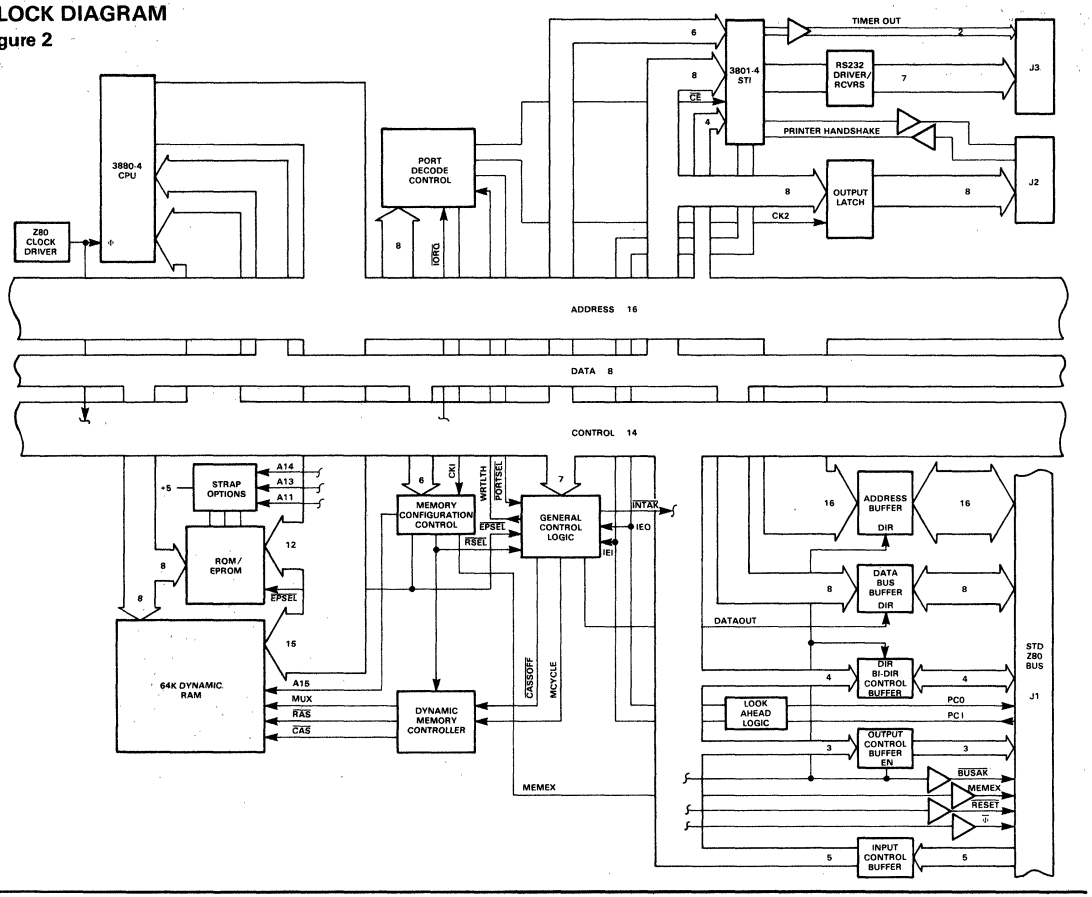
3.6864 MHz $\pm$ 0.05%

OPERATING TEMPERATURE:

0°C to 60°C

BLOCK DIAGRAM

Figure 2



POWER SUPPLY REQUIREMENTS

+5 V ± 5% @ 2.3 A max
+12 V ± 5% @ 50 ma max
–12 V ± 5% @ 50 ma max

MECHANICAL SPECIFICATIONS

CARD DIMENSIONS

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm.) long
0.675 in. (1.71 cm.) maximum profile thickness
0.062 in. (0.16 cm.) printed circuit board thickness

STD BUS EDGE CONNECTOR (J1)

56 pin dual readout; 0.125 in. centers

MATING CONNECTORS (P1)

PCB - Viking 3VH28/1CE5
WIREWRAP - Viking 3VH28/1CND5
SOLDER LUG - Viking 3VH28/1CN5

SERIAL I/O CONNECTOR (J3)

26 pin dual readout; 0.100 in. grid

MATING CONNECTORS (P3)

FLAT RIBBON - Ansley 609-2600M
DISCRETE WIRES - Winchester PGB13A (housing)
Winchester 100-70020S
(contacts 20-24 AWG)
Winchester 100-72026S
(contacts 26-30 AWG)

PRINTER CONNECTOR (J2)

Same as Serial I/O Connector

I/O CAPACITY

The MDX-CPU3 utilizes 18 of the possible 256 port addresses, leaving 238 port addresses available for expansion by the user.

MEMORY REFRESH

All address and control signals necessary to refresh external dynamic RAM modules are generated by MDX-CPU3.

I/O ADDRESSING

The onboard ports are preprogrammed to the following port addresses:

PORT ADDRESS
Figure 3

DEVICE	PORT ADDRESS (HEX)
MK3801 STI	BO - BF
Parallel Output Latch	DO
Memory Configuration	FF

I/O MAP PROM PROGRAMMING GUIDELINES

If it is desired to use port addresses other than those which are supplied, then the following procedure should be used:

Each address in the I/O Map PROM corresponds directly to a port address. The bits of the 4 bit control word are defined as shown in Figure 4. Select the desired port address and corresponding output bit definitions for that address and program a new I/O Map PROM with the new data.

BIT DEFINITIONS
Figure 4

OUTPUT BIT DEFINITIONS	ACTIVE STATE
01 - Select STI	High
02 - Select Output	High
03 - Select Memory Config. Latch	High
04 - Any of the above Ports selected	Low

PROGRAMMING SERIAL CHANNEL AND TIMERS

Programming information for the serial channel and timers can be found in the SERIAL TIMER INTERRUPT CONTROLLER (STI) Technical Manual, Mostek publication number 4420250.

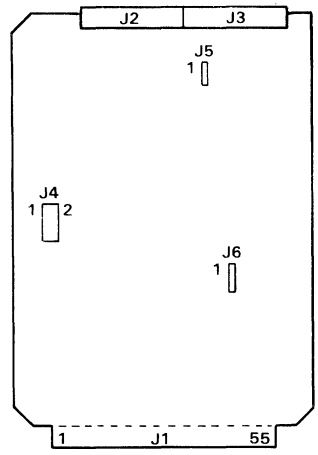
INTERRUPTS

The MDX-CPU3 will process external interrupts in the Z80-CPU interrupt modes 0, 1, and 2. Internal (onboard) interrupts can be processed only in modes 1 or 2.

SYSTEM RESET PRECAUTIONS

Data in DYNAMIC RAM is not guaranteed to be valid after a PUSHBUTTON RESET has been initiated.

CONNECTOR AND HEADER POSITIONS
Figure 5



STD BUS CONNECTOR

J1 The standard Bus pins used are buffered and brought out to a 56 pin edge connector as shown:

SIGNAL NAME	PIN	J1	PIN	SIGNAL NAME
+5 V	2		1	+5 V
GND	4		3	GND
NC	6		5	NC
D7	8		7	D3
D6	10		9	D2
D5	12		11	D1
D4	14		13	D0
A15	16		15	A7
A14	18		17	A6
A13	20		19	A5
A12	22		21	A4
A11	24		23	A3
A10	26		25	A2
A9	28		27	A1
A8	30		29	A0
RD*	32		31	WR*
MEMRQ*	34		33	IORQ*
MEMEX (Note)	36		35	NC
NC	38		37	REFRESH*
NC	40		39	STATUS 1*
BUSRQ*	42		41	BUSAK*
INTRQ*	44		43	INTAK*
NMIRQ*	46		45	WAITRQ*
PBRESET*	48		47	SYSRESET*
NC	50		49	CLOCK*
PCI	52		51	PCO
NC	54		53	NC
-12 V	56		55	+12 V

Note: If MEMEX is grounded on the motherboard, the ground strap should be removed.

IVB

PRINTER CONNECTOR

J2 The printer port data and control signals are brought out to a 26 pin connector as shown:

SIGNAL NAME	PIN	J2	PIN	SIGNAL NAME
/STB	1	O O	14	GND
D1	2	O O	15	GND
D2	3	O O	16	NC
D3	4	O O	17	NC
D4	5	O O	18	NC
D5	6	O O	19	NC
D6	7	O O	20	NC
D7	8	O O	21	NC
D8	9	O O	22	NC
NC	10	O O	23	NC
BUSY	11	O O	24	NC
PE	12	O O	25	NC
NC	13	O O	26	NC

SERIAL CONNECTOR

J3 The serial comunication signals to perform an RS232 type interface are buffered and brought out to a 26 pin connector as shown, the timer outputs are also buffered and brought out on pins 11 and 18:

SIGNAL NAME	PIN	J3	PIN	SIGNAL NAME
GND	1	O O	14	NC
RX	2	O O	15	NC
TX	3	O O	16	NC
RTS	4	O O	17	NC
CTS	5	O O	18	TAO
DSR	6	O O	19	NC
GND	7	O O	20	DTR
RLSD	8	O O	21	NC
NC	9	O O	22	NC
NC	10	O O	23	NC
TCO	11	O O	24	NC
NC	12	O O	25	NC
NC	13	O O	26	NC

PIN DEFINITION

Figure 6

J4

U22 PIN 23	1	O O	2	A11
U22 PIN 23	3	O O	4	+5 VDC
+5 VDC	5	O O	6	A13
U22 PIN 26	7	O O	8	U22 PIN 26
+5 VDC	9	O O	10	A14
U22 PIN 1	11	O O	12	U22 PIN 1

ROM/EPROM STRAPPING

J4 This header allows the ROM/EPROM socket U22 to be configured to accept various devices. Figure 7 shows the strapping needed for each device.

MEMORY STRAPPING CHART

Figure 7

DEVICE TYPE	STRAPS REQUIRED
2716	J4 (3-4), (5-7)
INTEL 2732	J4 (1-2), (5-7)
INTEL 2764	J4 (1-2), (9-11)
MK34000	J4 (5-7)
MK37000	J4 (1-2)
MK38000	J4 (1-2), (6-8), (10-12)

MEMORY MAP EXPANSION

The memory configuration PROM supplied with the MDX-CPU3 utilizes maps 0, 4, 5, and 6 to support two types of software packages. The first package is a system booted into RAM then executed out of that RAM. It utilizes maps 0 and 5. The second utilizes maps 0, 4, 5, and 6, and supports a bank memory scheme. If a custom map PROM which uses all 8 memory maps is desired, then install J5 to get this expansion.

MEMORY MAP PROM CONFIGURATION

The following chart shows the memory configuration maps as supplied with each MDX-CPU3 module.

MEMORY MAP
Figure 8

MEMORY ADDRESS	MAP 0	1	2	3	4	5	6	7
FFFF	RAM	NOT USED	NOT USED	NOT USED	RAM	RAM	RAM	RAM
F000								
	RAM & ROM							ROM
E000								
D000	RAM				OFF BOARD RAM		OFF BOARD RAM	RAM
C000								
B000								
A000								
9000								
8000								
7000								
6000								
5000								
4000								
3000								
2000								
1000								
0000	ROM							

IVB

MEMORY MAP PROM PROGRAMMING GUIDELINES

Each memory MAP in the Memory Configuration PROM consists of a series of nibbles which define which memory is enabled. Each of these nibbles is 4 bits wide. The function of each bit is defined by Figure 9.

BIT STATE CHART
Figure 9

OUTPUT BIT DEFINITIONS	ACTIVE STATE
01 - SELECT EPROM	LOW
02 - A15 ADDRESS LINE OUTPUT	
03 - SELECT RAM	LOW
04 - MEMORY EXPAND OUTPUT	HIGH

BIT DEFINITION LIST

1. SELECT EPROM: Causes the signal which enables the ROM/EPROM for reading.

2. A15 ADDRESS LINE OUTPUT: This bit generates the uppermost address line to the onboard RAM memory.

3. SELECT RAM: Enables the onboard RAM. If SELECT EPROM is also programmed, RAM will be write-only.

4. MEMORY EXPAND OUTPUT: This bit generates a signal which is defined by the STD-Z80 Bus specification for the MEMEX signal. In most single board configurations, this bit is programmed low.

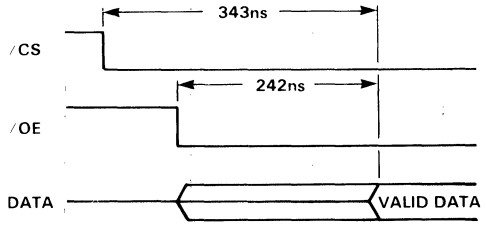
TEST CONNECTOR

J6 This header is used for testing purposes only and is strapped (Pin 2-3) at the factory. DO NOT REMOVE.

ROM/EPROM ACCESS TIME

The time required for the ROM memory to be accessed by the CPU is defined by two specifications; /CS and /OE. First, /CS access must be ≤ 343 ns. Second, access time from /OE must be ≤ 242 ns. These requirements must be met in order for data to meet the minimum setup time for the CPU under worst case timing conditions. See Figure 10.

ACCESS TIME
Figure 10



MULTIPLE MEMORY BANK OPERATION

The MDX-CPU3 supports a memory bank switching operation which allows memory expansion beyond the normal 64K byte limitation of the Z80.

Bank select is accomplished as follows. After the SYSTEM BOOT operation has been performed and the first bank has been selected, additional banks of memory can be enabled and disabled by outputting a bank select byte to port FFH. Figure 11 shows the control byte necessary to select each additional bank of memory.

MEMORY BANK OPERATION
Figure 11

SELECT BYTE	BANK NO.	SELECT BYTE	BANK NO.
01	1	10	5
02	2	20	6
04	3	40	7
08	4	80	8

PROGRAMMABLE LED

An LED is available to be programmed on/off at bit D4 (1X) of port FFH. This may be used as a visual self test indicator or other appropriate user functions. This bit is also used in the memory bank switching mode and the indicator will illuminate when addressing bank 5.

SOFTWARE PROGRAMMING GUIDELINES

The CPU3 can support a phantom ROM type of operation where the ROM has just enough code to bring a larger operating system into RAM, then by switching to another map, disables the ROM dynamically and begins operation in a purely RAM configuration. A very simple method to do this is to have memory map 0 in the configuration PROM act as the boot-up map and then switch to a desired map configuration. The following procedure is then followed:

A. Copy the ROM code into the RAM at the same address range as the ROM.

B. Switch maps by outputting a new map number to the Memory Configuration port (0FFH), allowing the copy of RAM code to enter the active memory.

C. Execution of the program will continue at the next instruction now in the RAM.

Related Publications

The following are related publications:

Customizing the MDX-CPU3 PROMs Application Note #5 (4420301)

MDX-CPU3/4 I/O Drivers Application Note #10

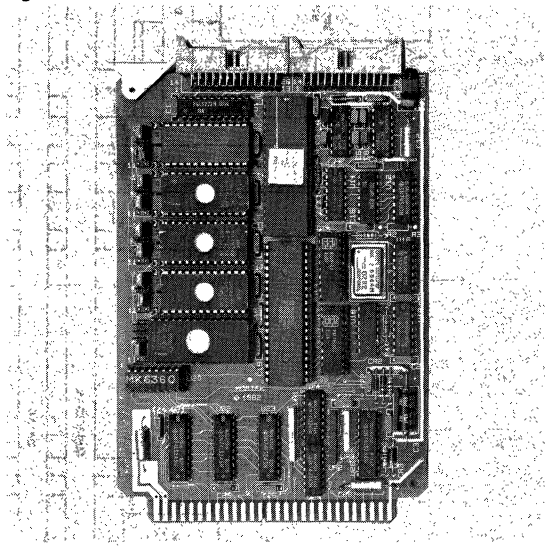
PRELIMINARY

MDX-CPU4

FEATURES

- ☐ STD-Z80 Bus compatible CPU board
- ☐ Five 28 pin sockets for industry standard BYTEWYDE™ ROMs, EPROMs, or RAMs
- ☐ Flexible memory decoding of RAM/ROM memory on any 2K boundary
- ☐ Phantom ROM capability
- ☐ Bidirectional address, data, and control busses to permit external DMA to onboard memory
- ☐ 8-bit output port with handshake (Centronics printer interface)
- ☐ Full handshake serial RS232-C I/O Port
- ☐ Software programmable Baud rates to 9600 Baud
- ☐ Bidirectional power-on reset allows operation with power-fail controllers
- ☐ Two programmable 8-bit timers with offboard outputs
- ☐ Fully buffered signals for system expansibility
- ☐ Supports memory bank switching
- ☐ Supports MEMEX (memory expand) capability

MDX-CPU4
Figure 1



MDX-CPU4 DESCRIPTION

The MDX-CPU4 is an STD-Z80 Bus compatible single board computer with five BYTEWYDE memory sockets for ROM, EPROM, or RAM, an RS232-C serial port, and an 8-bit parallel output port with handshake for connection to a printer. The CPU4 supports a very flexible memory map configuration by the use of a memory configuration PROM. This allows the RAM/ROM to be mapped on 2K boundaries anywhere in the 64K memory map. Each of the eight maps shipped is selectable under software control. Address, data, and control busses are bidirectional to allow external masters to access memory on CPU4 directly.

The 8-bit parallel output port with handshake lines is configured to accommodate direct connection to a Centronics type printer interface using mass terminated flat ribbon cable connectors.

The RS232-C serial port is configured to accommodate full handshake capabilities (interface type D).

All STD-Z80 signals are fully buffered to allow use of this board with other STD-Z80 compatible boards. This permits future expansion of functional capabilities.

ELECTRICAL SPECIFICATIONS

STD-Z80 BUS COMPATIBLE

SYSTEM INTERRUPT UNITS:
1 SIU

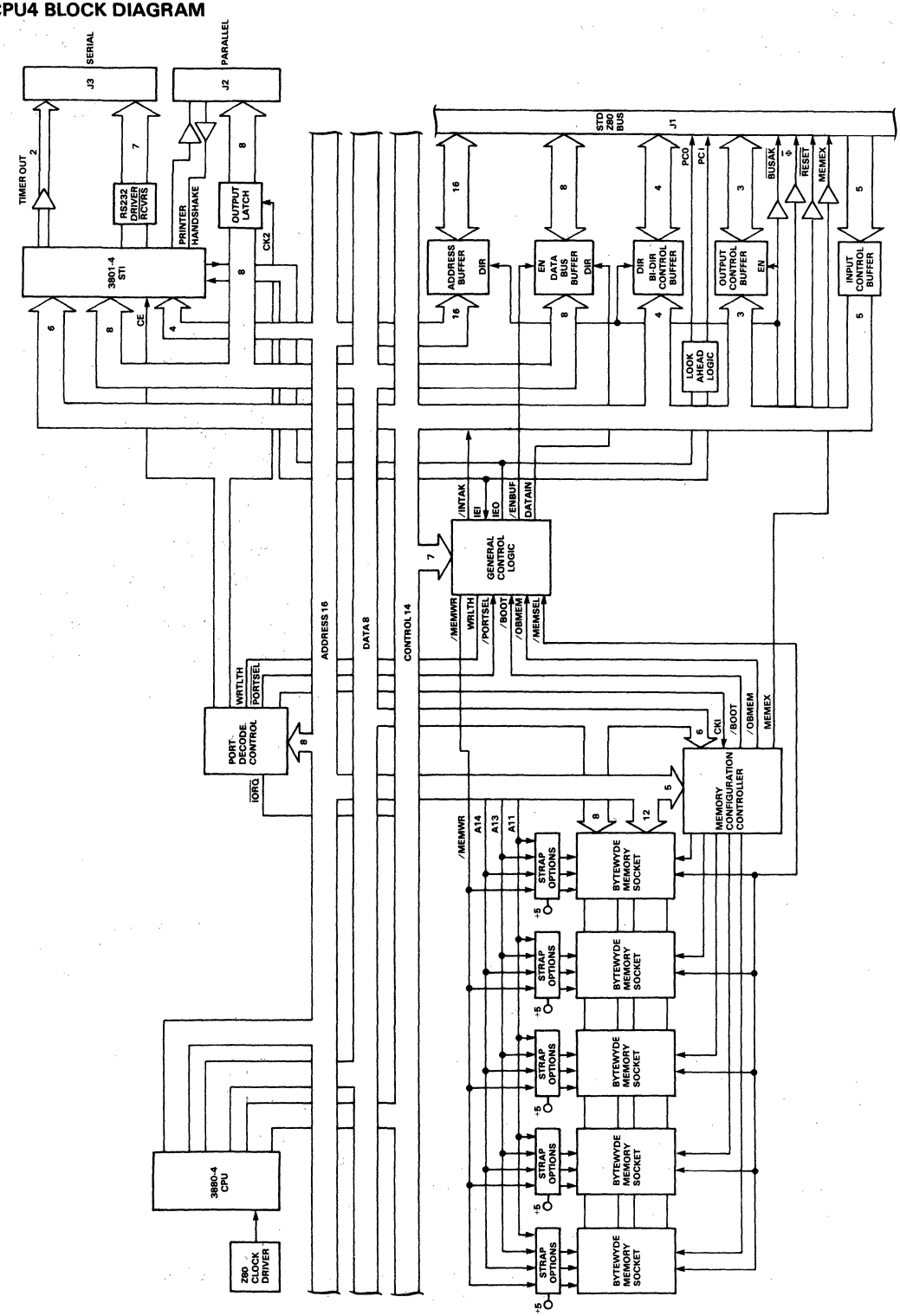
SYSTEM CLOCK:
3.6864 MHz ± 0.05%

OPERATING TEMPERATURE:
0°C to 60°C

BYTEWYDE™ is a UTC/Mostek registered trademark

MDX-CPU4 BLOCK DIAGRAM

Figure 2



POWER SUPPLY REQUIREMENTS:
+5 V ± 5% @ 1.8 A max (excluding BYTEWYDE sockets)
+12 V ± 5% @ 50 ma max
-12 V ± 5% @ 50 ma max

MECHANICAL SPECIFICATIONS

CARD DIMENSIONS
4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm.) long
0.675 in. (1.71 cm.) maximum profile thickness
0.062 in. (0.16 cm.) printed circuit board thickness

STD BUS EDGE CONNECTOR (J1)
56 pin dual readout; 0.125 in. centers
MATING CONNECTORS (P1)
PCB - Viking 3VH28/1CE5
WIREWRAP - Viking 3VH28/1CND5
SOLDER LUG - Viking 3VH28/1CN5

SERIAL I/O CONNECTOR (J3)
26 pin dual readout; 0.100 in. grid
MATING CONNECTORS (P3)
FLAT RIBBON - Ansley 609-2600M
DISCRETE WIRES - Winchester PGB13A (housing)
Winchester 100-72020S
(contacts 20-24 AWG)
Winchester 100-72026S
(contacts 26-30 AWG)

PRINTER CONNECTOR (J2)
Same as Serial I/O Connector

I/O CAPACITY

The MDX-CPU4 utilizes 18 of the possible 256 port addresses, leaving 238 port addresses available for expansion by the user.

MEMORY REFRESH

All address and control signals necessary to refresh external dynamic RAM modules are generated by MDX-CPU4.

I/O ADDRESSING

The onboard ports are preprogrammed to the port addresses shown in Figure 3.

PORT ADDRESSES
Figure 3

Device	Port Address (Hex)
MK3801 STI	B0-BF
Parallel Output Latch	D0
Memory Configuration	FF

I/O MAP PROM PROGRAMMING GUIDELINES

If it is desired to use port addresses other than those which are supplied, then the following procedure should be used.

Each address in the I/O Map PROM corresponds directly to a port address. The bits of the 4 bit control word are defined as shown in Figure 4. Select the desired port address and corresponding output bit definitions for that address and program a new I/O Map PROM with the new data.

I/O MAP BIT DEFINITIONS
Figure 4

OUTPUT BIT DEFINITIONS	ACTIVE STATE
01 - Select MK3801 STI	HIGH
02 - Select Parallel Output Latch	HIGH
03 - Select Memory Config. Latch	HIGH
04 - Any of the above ports selected	LOW

IVB

PROGRAMMING SERIAL CHANNEL AND TIMERS

Programming information for the serial channel and timers can be found in the SERIAL TIMER INTERRUPT CONTROLLER (STI) Technical Manual, Mostek publication number 4420250.

INTERRUPTS

The MDX-CPU4 will process external interrupts in Z80-CPU interrupt modes 0, 1, and 2. Internal (onboard) interrupts can be processed only in modes 1 or 2.

SYSTEM RESET PRECAUTIONS

Data in DYNAMIC RAM is not guaranteed to be valid after a PUSHBUTTON RESET has been initiated.

CONNECTORS AND HEADERS

The location of the connectors and headers is shown in Figure 5.

STD BUS CONNECTOR

J1 The STD Bus pins used are buffered and brought out to a 56 pin edge connector as shown:

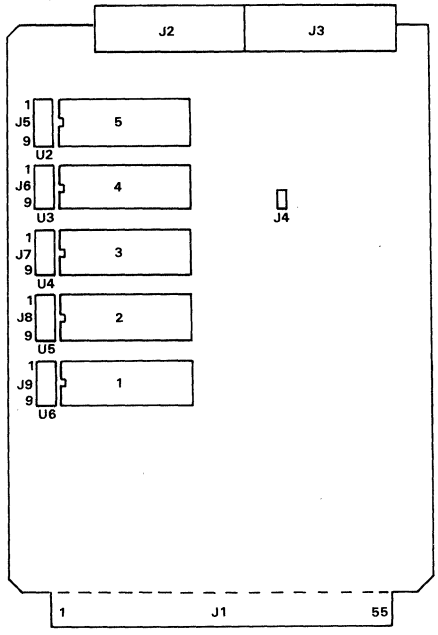
SIGNAL NAME	PIN	J1	PIN	SIGNAL NAME
+5 V	2		1	+5 V
GND	4		3	GND
NC	6		5	NC
D7	8		7	D3
D6	10		9	D2
D5	12		11	D1
D4	14		13	D0
A15	16		15	A7
A14	18		17	A6
A13	20		19	A5
A12	22		21	A4
A11	24		23	A3
A10	26		25	A2
A9	28		27	A1
A8	30		29	A0
RD*	32		31	WR*
MEMRQ*	34		33	IORQ*
MEMEX (NOTE)	36		35	NC
NC	38		37	REFRESH*
NC	40		39	STATUS 1*
BUSRQ*	42		41	BUSAK*
INTRQ	44		43	INTAK*
NMIRQ*	46		45	WAITRQ*
PBRESET*	48		47	SYSRESET*
NC	50		49	CLOCK*
PCI	52		51	PCO
NC	54		53	NC
-12 V	56		55	+12 V

***Indicates active low signal**

NOTE: If MEMEX is grounded on the motherboard, the groundstrap should be removed.

CONNECTOR, HEADER, AND BYTEWYDE SOCKET POSITIONS

Figure 5



PRINTER CONNECTOR

J2 The printer port data and control signals are brought out to a 26 pin connector as shown.

SIGNAL NAME	PIN	J2	PIN	SIGNAL NAME
/STB	1	0 0	14	GND
D1	2	0 0	15	GND
D2	3	0 0	16	NC
D3	4	0 0	17	NC
D4	5	0 0	18	NC
D5	6	0 0	19	NC
D6	7	0 0	20	NC
D7	8	0 0	21	NC
D8	9	0 0	22	NC
NC	10	0 0	23	NC
BUSY	11	0 0	24	NC
PE	12	0 0	25	NC
NC	13	0 0	26	NC

SERIAL CONNECTOR

J3 The serial communication signals to perform an RS232 type interface are buffered and brought out to a 26 pin connector as shown; the timer outputs are also buffered and brought out on pins 11 and 18.

SIGNAL NAME	PIN	J2	PIN	SIGNAL NAME
GND	1	0 0	14	NC
RX	2	0 0	15	NC
TX	3	0 0	16	NC
RTS	4	0 0	17	NC
CTS	5	0 0	18	TAO
DSR	6	0 0	19	NC
GND	7	0 0	20	DTR
RSLD	8	0 0	21	NC
NC	9	0 0	22	NC
NC	10	0 0	23	NC
TCO	11	0 0	24	NC
NC	12	0 0	25	NC
NC	13	0 0	26	NC

MEMORY MAP STRAP

J4 A jumper on J4 allows all eight memory maps in the memory configuration PROM (see section entitled MEMORY MAP PROM) to be accessed. With J4 open, access defaults to maps 4, 5, 6, and 7. The board is shipped with J4 open.

RAM/ROM/EPROM STRAPPING

J5-9 These headers allow the BYTEWYDE sockets 1-5 (U6-U2) to be configured to accept various devices. Figures 6 and 7 show the headers and strapping needed for each device. These are typical figures showing the relationship between J9 and socket 1 (U6). The same relationship applies between J8 and socket 2 (U5), J7 and socket 3 (U4),

J6 and socket 4 (U3), and J5 and socket 5 (U2). The board is shipped with no straps installed in J5, J6, J7, J8, or J9.

MEMORY CONFIGURATION HEADER

Figure 6

			J9		(TYPICAL)
AD13	-	1	0	0	2 - U6 pin 26
U6 pin 1	-	3	0	0	4 - +5 VDC
AD14	-	5	0	0	6 - +5 VDC
AD11	-	7	0	0	8 - U6 pin 23
NC	-	9	0	0	10- /MEMWR

CONFIGURATION STRAPPING CHART

Figure 7

DEVICE TYPE	STRAPS REQUIRED (TYPICAL)
2716	J9 (2-4), (6-8)
INTEL 2732	J9 (2-4), (7-8)
INTEL 2764	J9 (3-4), (7-8)
MK34000	J9 (2-4)
MK37000	J9 (7-8)
MK38000	J9 (1-2), (3-5), (7-8)
MK4802	J9 (2-4), (8-10)

MEMORY MAP PROM

The memory map PROM (U14) contains eight memory configuration maps. As the chart in Figure 8 indicates, resolution of the maps is 2K blocks. The numbers enclosed in brackets [ ], represent BYTEWYDE memory sockets on board as shown in Figure 5. The memory installed may be either RAM or ROM. The indication (RAM) represents off-board RAM.

If bank switching is desired, the section entitled MULTIPLE MEMORY BANK OPERATION describes the use of jumper J4 and the various memory maps in obtaining this.

MEMORY MAP PROM PROGRAMMING GUIDELINES

Each memory MAP in the Memory Configuration PROM consists of a series of bytes which define what memory is enabled. The function of each bit of the byte is defined by Figure 9.

BIT DEFINITION LIST

1. SELECT SOCKET ONE TO FIVE: These bits generate the

IVB

MEMORY CONFIGURATION MAPS

Figure 8

MEMORY ADDRESS	MAP 0	1	2	3	4	5	6	7
FFFF	(RAM)	(RAM)	(RAM)	(RAM)	(RAM)	(RAM)	(RAM)	[1]
F000	(RAM)							
E000	[1]							
D000	(RAM)							(RAM)
C000								
B000								
A000				[5]				
9000				[4]				
8000				[3]				
7000				[2]				
6000				[1]				
5000								
4000								
3000			[5]					
2000		[5]	[4]					
1000		[4]	[3]					
0000	[1]	[3]	[2]					
		[2]	[1]					
		[1]						

[ ] = CPU4 socket no. (RAM) = off board RAM

BIT STATE CHART

Figure 9

OUTPUT BIT DEFINITIONS	ACTIVE STATE
01 - Select Socket One	LOW
02 - Select Socket Two	LOW
03 - Select Socket Three	LOW
04 - Select Socket Four	LOW
05 - Select Socket Five	LOW
06 - MEMEX Output	HIGH
07 - Onboard Memory Selected	LOW
08 - System Boot Selected	LOW

signal which enables each BYTEWYDE socket for operation.

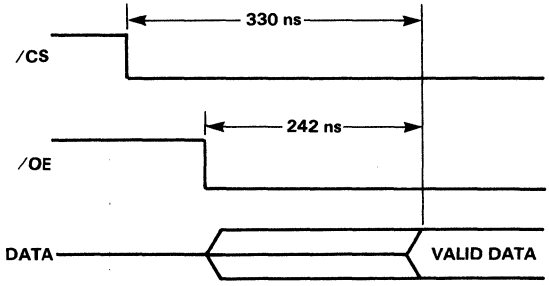
2. MEMORY EXPAND OUTPUT: This bit generates a signal which is defined by the STD-Z80 Bus specification for the MEMEX signal. In most single board configurations this bit is programmed low.
3. ONBOARD MEMORY SELECTED: This bit indicates that one of the onboard memory sockets has been selected.
4. SYSTEM BOOT SELECTED: This bit indicates that BYTEWYDE socket 1 is selected while in map 0.

RAM/ROM ACCESS TIME

The time required for the RAM/ROM memory to be accessed by the CPU is defined by two specifications; /CE and /OE. First, /CE access must be $\leq$ 330 ns. Second, access time from /OE must be $\leq$ 242 ns. These requirements must be met in order for data to meet the minimum setup time for the CPU under worst case conditions. See Figure 10.

ACCESS TIME

Figure 10



MULTIPLE MEMORY BANK OPERATION

The MDX-CPU4 supports a memory bank switching operation which allows memory expansion beyond the normal 64K byte limitation of the Z80.

There are two basic schemes of bank switching available. One method requires removal of jumper J4. With J4 removed, write a select byte to port FFH as shown in Figure 11. This selects one of eight different banks and utilizes memory maps 4, 5, and 6 (see Figure 8). This does not take advantage of any CPU4 memory except the bootup PROM. The alternative scheme leaves jumper J4 in position and has the PROM in socket 1 be a combination bootup PROM and kernel. After power-up, a 07H written to port FFH allows the user to have his kernel on CPU4 and do bank switching via any port except FFH.

PROGRAMMABLE LED

An LED is available to be programmed on/off at bit D4 (1X) of port FFH. This may be used as a visual self test indicator or other appropriate user functions. This bit is also used in the memory bank switching mode and the indicator will illuminate when addressing bank 4.

SOFTWARE PROGRAMMING GUIDELINES

The CPU4 can support a phantom ROM type of operation where the ROM has just enough code to bring a larger operating system into RAM, then by switching to another map, disables the ROM dynamically and begins operation in a purely RAM configuration. A very simple method to do this is to have memory map 0 in the configuration PROM act as the boot-up map and then switch to a desired map configuration. This procedure is then followed:

A. Copy the ROM code into the RAM at the same address range as the ROM.

B. Switch maps by outputting a new map number to the Memory Configuration port (0FFH), allowing the copy of ROM in RAM code to enter the active memory.

C. Execution of the program will continue at the next instruction now in the RAM.

MEMORY BANK SELECT

Figure 11

SELECT BYTE (HEX)	BANK NO.	MEMORY MAP	SELECT BYTE (HEX)	BANK NO.	MEMORY MAP
01	0	5	10	4	4
02	1	6	20	5	4
04	2	4	40	6	4
08	3	4	80	7	4

RELATED PUBLICATIONS

Application Note #10 MDX-CPU3/4 I/O Drivers Publication
No. 4420333

ORDERING INFORMATION

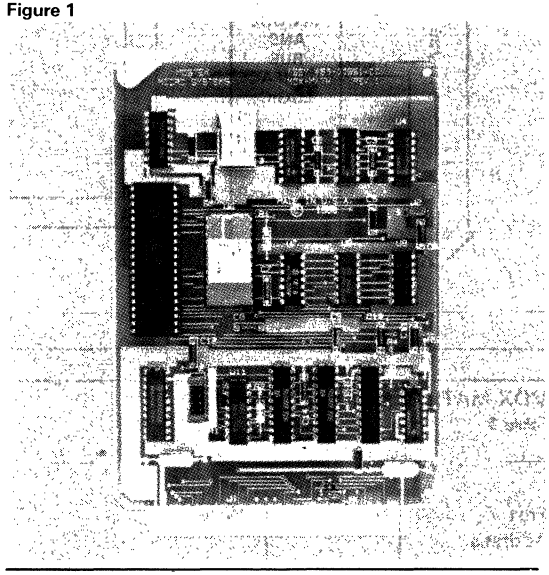
DESIGNATOR	DESCRIPTION	PART NO.
MDX-CPU4	STD-Z80 Bus single board computer with BYTEWYDE memory sockets	MK77858
MDX-CPU4 TM	MDX-CPU4 Technical Manual Only	4420285
CPU3/4 to CRT	Cable	MK79100
CPU3/4 to Centronics Printer	Cable	MK79098

MDX-MATH
MK77852

FEATURES

- ☐ STD-Z80 BUS compatible
- ☐ Fixed-point 16 and 32-bit operations
- ☐ Floating point 32-bit operations
- ☐ Binary data formats
- ☐ Add, Subtract, Multiply and Divide
- ☐ Trigonometric and inverse trigonometric functions
- ☐ Square roots, logarithms, exponentials
- ☐ Float-to-fixed and fixed-to-float conversions
- ☐ Stack-oriented operand storage
- ☐ On-board wait-state insertion circuitry

MDX-MATH BOARD PHOTO
Figure 1



DESCRIPTION

The MDX-MATH board is offered as one of Mostek's complete line of STD-Z80 BUS-compatible microcomputer modules. The MDX-MATH board, based on the AM9511A Arithmetic Processing Unit (APU), provides high performance fixed and floating point trigonometric and mathematical operations. It can be used to enhance the computational capability of a wide variety of STD-Z80 BUS systems.

Figure 2 is a block diagram which illustrates the functional elements of the MDX-MATH board.

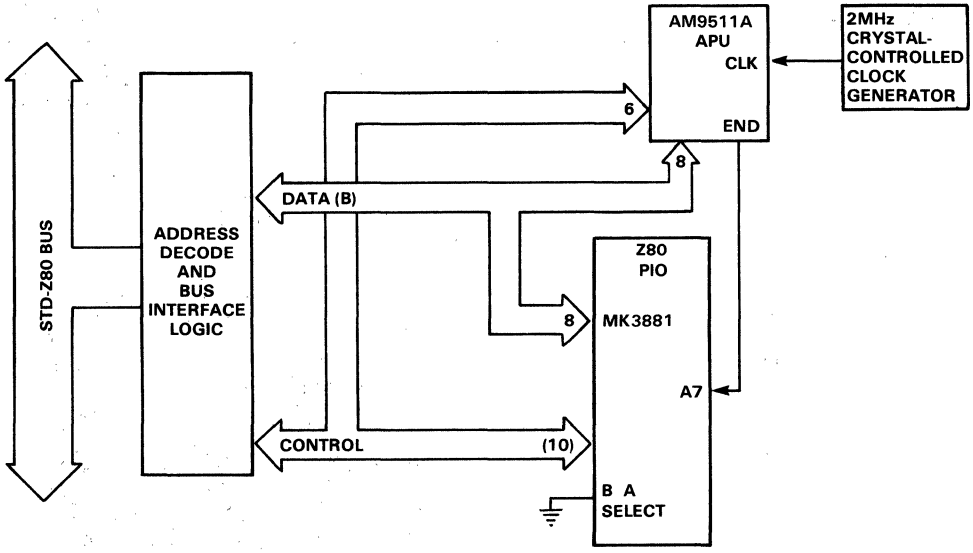
The Arithmetic Processing Unit (APU) is a monolithic MOS/LSI device that performs all of the mathematical operations. All transfers to and from the APU take place over the 8-bit, bi-directional data bus. Operands are pushed onto an internal stack within the APU and a command is issued to perform operations on the data in the stack. Results are then available to be retrieved from the stack, or additional commands may be entered.

Side A of the MK3881 PIO can be utilized to provide a Z80 Mode 2 interrupt response when the APU completes the execution of a command and pulls its END line low. If the PIO has been programmed to interrupt on the high-to-low transition of port bit A7, it will provide a vectored interrupt and maintain the daisy-chain-priority interrupt logic compatible with the STD-Z80 BUS.

Each MDX-MATH board has a total of five registers; three WRITE only and two READ only. These registers appear as three I/O port addresses and are defined in Table 1.

MDX-MATH BLOCK DIAGRAM

Figure 2



MDX-MATH REGISTERS

Table 1

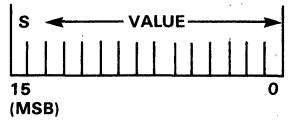
Port Address	Read	Write
X X X X X X 0 0	APU Status	APU Command
X X X X X X 0 1	Undefined	PIO Side A Control
X X X X X X 1 0	APU Stack	APU Stack

The "X" symbols are "don't cares" and are jumper-selectable. These port addresses are fully decoded.

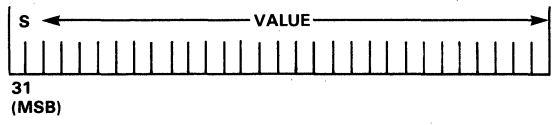
The MDX-MATH board APU operates from an independent 2 MHz, crystal-controlled, clock generator circuit. The time required by the AM9511A to execute some of its commands can exceed 4 milliseconds. Because of this, there is circuitry designed to block any access to the APU which would cause wait states to be inserted for such long periods of time during the execution of a command. This action prevents any interference with dynamic memory refresh as well as any sacrifice of Z80 processing time.

The Arithmetic Processing Unit handles operands in both fixed point and floating point formats. Fixed point operands may be represented in either single (16-bit operands) or double precision (32-bit operands) and are always represented as binary, two's complement values.

16-BIT FIXED POINT FORMAT

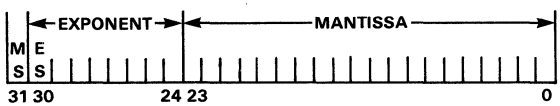


32-BIT FIXED POINT FORMAT



FLOATING POINT FORMAT

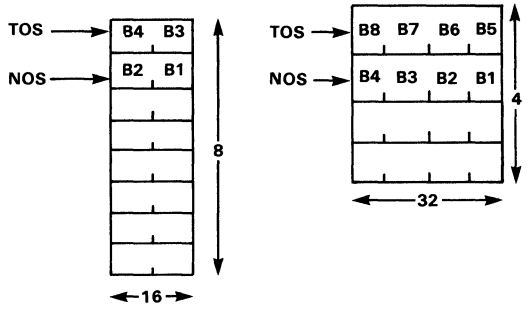
The format for floating point values is given. The mantissa is expressed as a 24-bit (fractional) value; the exponent is expressed as an unbiased two's complement 7-bit value having a range of -64 to +63. The most significant bit is the sign of the mantissa (0 = positive, 1 = negative), for a total of 32 bits. The binary point is assumed to be to the left of the most significant mantissa bit (bit 23). All floating point data values must be normalized. Bit 23 must be equal to 1, except for the value zero, which is represented by all zeros.



The range of values that can be represented in this format is $\pm(2.7 \times 10^{-20}$ to $9.2 \times 10^{18})$ and zero.

STACK CONTROL

The user interface includes access to an 8-level, 16-bit-wide data stack. Since single-precision, fixed-point operands are 16 bits in length, eight such values may be maintained in the stack. When using double-precision, fixed point or floating point formats, four values may be stored. The stack in these two configurations can be visualized as shown.

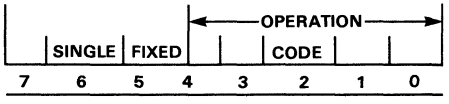


Data is written onto the stack, eight bits at a time, in the order shown (B1, B2, B3,. . .). Data is removed from the stack in reverse byte order (B8, B7, B6,. . .). Data should be transferred into or out of the stack in multiples of the number of bytes appropriate to the chosen data format.

COMMAND STRUCTURE

Figure 3 lists the commands and their mnemonics.

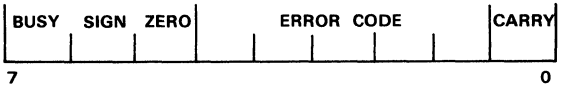
Each command consists of a single 8-bit byte having the format illustrated.



Bits 0-4 select the operation to be performed. Bits 5-6 select the data format for the operation. If bit 5 is a 1, a fixed point data format is specified. If bit 5 is a 0, the floating point format is specified. Bit 6 selects the precision of the data to be operated on by fixed point commands (if bit 5 = 0, bit 6 must be 0). If bit 6 is a 1, single-precision (16-bit) operands are indicated; if bit 6 is a 0, double-precision (32-bit) operands are indicated. Results are undefined for all illegal combinations of bits in the command byte.

DEVICE STATUS

Device status is provided by means of an internal status register whose format is shown.



BUSY: Indicates that the MDX-MATH board is currently executing a command (1 = Busy).

SIGN: Indicates that the value on the top of stack is negative (1 = Negative).

ZERO: Indicates that the value on the top of stack is zero (1 = Value is zero).

ERROR CODE: This field contains an indication of the validity of the result of the last operation. The error codes are:
0000 - No error
1000 - Divide by zero
0100 - Square root or log of negative number
1100 - Argument of inverse sine, cosine, or e^X too large
XX10 - Underflow
XX01 - Overflow

CARRY: Previous operation resulted in carry or borrow from most significant bit. (1 = Carry/Borrow, 0 = No Carry/No Borrow)

The BUSY bit in the status register can be read by the Z80 CPU at any time whether an operation is in progress or not.

COMMAND SUMMARY

Figure 3

ACOS	ARCCOSINE	LOG	COMMON LOGARITHM
ASIN	ARCSINE	LN	NATURAL LOGARITHM
ATAN	ARCTANGENT	NOP	NO OPERATION
CHSD	CHANGE SIGN DOUBLE	POPD	POP STACK DOUBLE
CHSF	CHANGE SIGN FLOATING	POPF	POP STACK FLOATING
CHSS	CHANGE SIGN SINGLE	POPS	POP STACK SINGLE
COS	COSINE	PTOD	PUSH STACK DOUBLE
DADD	DOUBLE ADD	PTOF	PUSH STACK FLOATING
DDIV	DOUBLE DIVIDE	PTOS	PUSH STACK SINGLE
DMUL	DOUBLE MULTIPLY LOWER	PUPI	PUSH
DMUU	DOUBLE MULTIPLY UPPER	PWR	POWER (X^Y)
DSUB	DOUBLE SUBTRACT	SADD	SINGLE ADD
EXP	EXPONENTIATION (e^X)	SDIV	SINGLE DIVIDE
FADD	FLOATING ADD	SIN	SINE
FDIV	FLOATING DIVIDE	SMUL	SINGLE MULTIPLY LOWER
FIXD	FIX DOUBLE	SMUU	SINGLE MULTIPLY UPPER
FIXS	FIX SINGLE	SQRT	SQUARE ROOT
FLTD	FLOAT DOUBLE	SSUB	SINGLE SUBTRACT
FLTS	FLOAT SINGLE	TAN	TANGENT
FMUL	FLOATING MULTIPLY	XCHD	EXCHANGE OPERANDS DOUBLE
FSUB	FLOATING SUBTRACT	XCHF	EXCHANGE OPERANDS FLOATING
		XCHS	EXCHANGE OPERANDS SINGLE

WORD SIZE

Data: 8 bits
I/O Addressing: 8 bits

I/O ADDRESSING

On-board programmable - See Table 1

I/O CAPACITY

Five parallel 8-bit ports. Three WRITE Only and two READ only. (See Table 1)

INTERRUPTS

Vectored interrupt generated. Daisy-chained interrupt priority. Interrupt vector programmable upon initialization.

SYSTEM INTERRUPT UNITS (SIU) = 1

SYSTEM CLOCK

MDX-MATH 2.5 MH_3 to 4 $MH_3 \pm .05\%$

OPERATING TEMPERATURE RANGE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+12V ± 5% at 120 mA max
+5V ± 5% at 0.9 A max

STD BUS INTERFACE

Inputs: One 74LS Load max
Outputs: I_{OH} = -3mA min at 2.4 Volts
I_{OL} = 24mA min at 0.5 Volts

CARD DIMENSIONS

4.5 in. (114.3 mm) high by 6.50 in. (165.1 mm) long
0.48 in. (12.2 mm) maximum profile thickness
0.062 in. (1.6 mm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin dual readout 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/1CE5 WIRE WRAP Viking 3VH28/ 1CND5 SOLDER LUG Viking 3VH28/ 1CN5

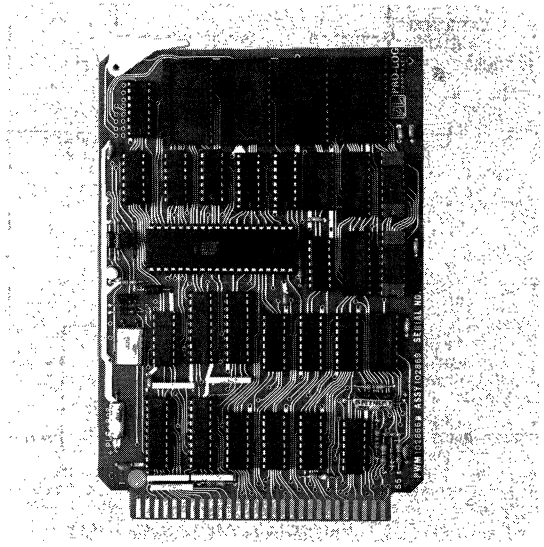
ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-MATH	Module with Operations Manual	MK77852
	MDX-MATH Operations Manual Only	MK79741

FEATURES

- Z80 Processor
- 2K Byte RAM capacity with 1K Included
- Sockets for 8K Bytes 2716 EPROM
- Three 8-Bit Output Ports
- Two 8-Bit Input Ports
- External Port Expansion to 16 Ports
- Single +5 Volt Supply

MD-SBC1
Figure 1



GENERAL DESCRIPTION

The MD-SBC1 is a complete Z80 microprocessor system on one 4.5 in. x 6.5 in. circuit card. The system provides a 56-pin card edge connector. The MD-SBC1 offers the capability of expanding program memory to 8192 bytes using 2048 byte, MK2716 PROM. The MD-SBC1 also comes with 1024 bytes of read/write memory but can be expanded to 2048 bytes by simply plugging in two additional 2114 RAMs. Included are three output ports and two input ports at the card; however, I/O can be expanded to eight input and output ports with a simple ribbon cable expansion system that accesses the data bus and I/O decoder strobes. The MD-SCB1 operates from a single +5 V supply.

The MD-SBC1 Z80 Processor includes all of the 8080A instructions as a subset. It also includes Bit, Relative, and Indexed addressing modes, powerful data block search and move instructions and a duplicate set of internal registers. The MD-SBC1 reduces program memory storage requirements and execution time significantly in many applications.

Z80/8080A COMPATIBILITY

The MD-SBC1 instruction set offers the 8080A instructions as a subset. 8080A programs execute normally in the MD-SBC1; however, the MD-SBC1 has shorter time states. Certain Z80 instructions execute in a different number of time states than identical 8080A instructions. Consequently, programmed timing adjustments may be necessary. Also, three Flag Register bits that were unused and constant in the 8080A are used by Z80. The Parity Flag assumes the dual role of Parity and Signed Binary Overflow with altered action after add and subtract instructions. Z80 Interrupt Mode 0 is identical to the 8080A interrupt system.

The MD-SBC1 executes 8085 programs except for those containing Read Interrupt Mask (RIM) and Set Interrupt Mask (SIM) instructions (with programmed timing adjustments as required).

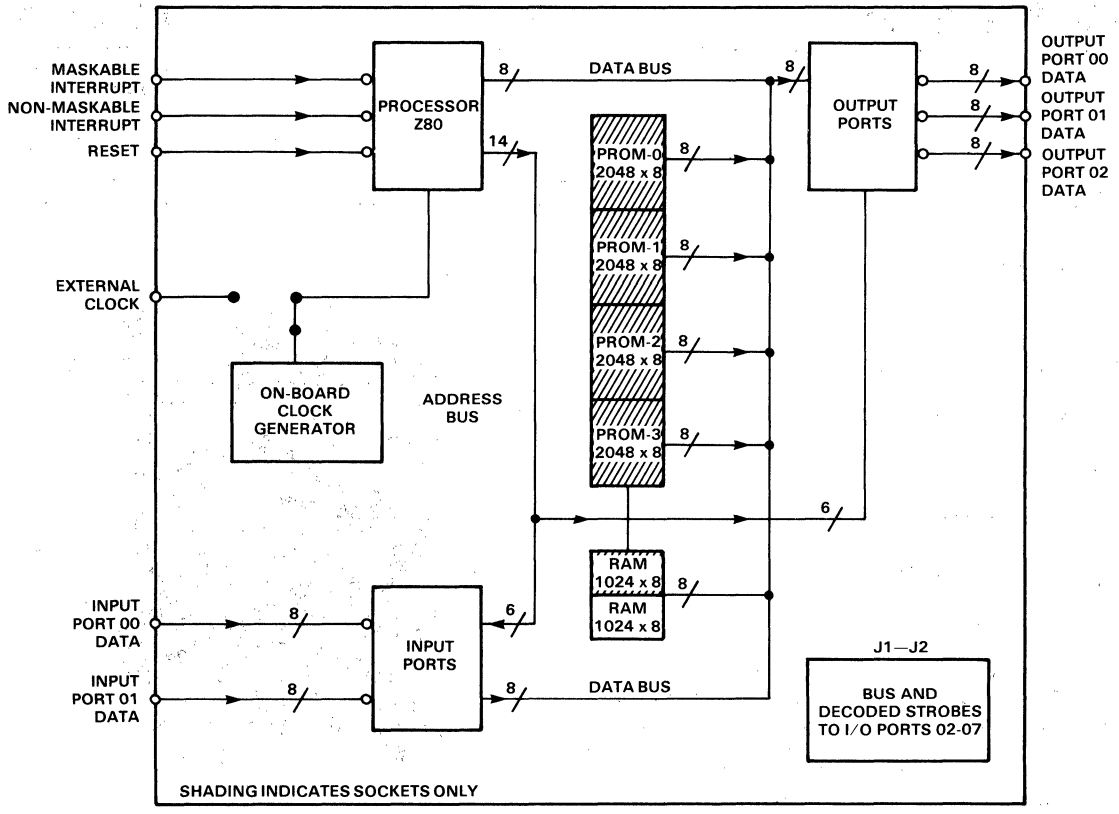
The Z80 Processor executes 158 instructions compared to the 8080A's 72. The additional Z80 instructions are identified by first word HEX, a code of 10, 18, 20, 28, 30, 38, CB, DD, ED or FD followed by 1, 2, or 3 words.

PROGRAM MEMORY

MD-SBC1 program memory consists of one to four MK2716 erasable PROM devices. Each 2716 contains 2048 eight-bit words organized as eight 256-word memory pages. MD-SBC1 program memory is assigned consecutive page locations as shown in Table 1.

MD-SBC1 BLOCK DIAGRAM

Figure 2



PROGRAM MEMORY LOCATIONS

Table 1

PROM NUMBER	ADDRESSES
0	0000H to 07FFH
1	0800H to 0FFFH
2	1000H to 17FFH
3	1800H to 1FFFH

DATA MEMORY

RAM data memory consists of two (standard) or four (optional) 2114 RAM devices. The 2114 is a 1024 x 4 RAM; each pair of 2114's provides 1024 eight-bit words organized as four 256-word memory pages. The standard MD-SBC1 provides RAM memory in pages 20 through 23. Two additional 2114 devices add RAM pages 24 through 27; these are implemented by plugging the devices in the sockets provided on the MD-SBC1.

RAM ADDRESSES

Table 2

RAM NUMBER	ADDRESSES
1, 2 (standard)	02000H to 023FFH
3, 4 (optional)	02400H to 027FFH

ON-CARD I/O PORTS

The MD-SBC1 provides two eight-bit input ports and three eight-bit output ports. These ports provide 16 input lines and 24 output lines that are available at the edge connector. They are TTL compatible.

ON-CARD PORT ADDRESS (HEX)

Input Ports	00 and 01
Output Ports	00, 01, and 02

PORT EXPANSION

MD-SBC1 can directly address additional I/O via two 16-pin dip sockets (J2 and J3). Dip connector terminated cables can interconnect user designed I/O boards such as A/D and D/A converters, or UARTs and USARTs. The MD-SBC1 can access additional six 8-bit input and five 8-bit output ports or devices in this manner. The control signals provided at J3 are input and output select lines. They combine a decoded port address with Z80's port Read or Write and timing signals. The Input Select lines (IS-2 through IS-7) apply directly to 3-state enable pins, which gate data to the Data In Bus (J2, DI-0, through DI-2); the Output Select lines normally clock output port latches loaded by the Data Out Bus (J2, DO-0 through DO-7). Figure 3 shows examples of external I/O port implementation.

I/O EXPANSION

A large number of external I/O ports may be multiplexed through the on-card MD-SBC1 I/O ports. However, this type of expansion requires more Processor execution time. Each I/O operation must be preceded by an output instruction, which selects the port and followed by output instructions, which provide the output strobes.

In this technique, one MD-SBC1 on-card input port and one output port are committed for use as data in and out busses. As required, other output port lines are used as I/O port select, port card select, and port strobes.

INTERRUPTS

The MD-SBC1 has two low activated, level sensitive interrupts with several designer options:

Nonmaskable Interrupt (NMI) has the highest priority and cannot be disabled.

Interrupt Request (IREQ) is enabled/disabled by the (EI)/(DI) instructions. The user can select one of three modes that define the action taken when IREQ is honored.

Mode 0 - Execute any instruction at Interrupt, but the instruction must be supplied by the interrupting device to the data in bus (D1 0-7), J2.

Mode 1 - Execute the RST 38H instruction.

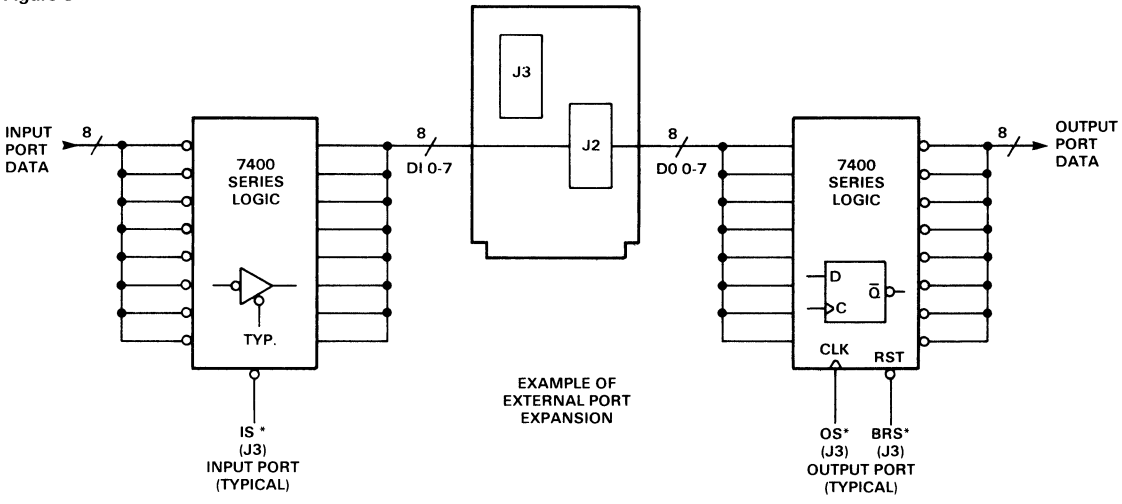
Mode 2 - Restart at any memory address according to a selected address vector (16 bits) stored in two memory locations. The interrupting device must supply the first 8 bits of the restart address vector. The page address is previously loaded by the program.

Modes 0 and 1 are summarized in Table 3.

MD-SBC1 INTERRUPT EXPANSION SUMMARY
Table 3

Interrupt	Priority	Restart Address (Hex)	Mode
Nonmaskable	Highest	Address 66H	Any
IREQ	Second	Address 38H	1

I/O EXPANSION
Figure 3



MD-SBC1 DESIGNER OPTIONS

The MD-SBC1 has 5 spare edge connector pins (5, 6, 52, 55, 56), which may be connected from pads provided to the signals listed below.

RESET (Active High Output)
EXTERNAL CLOCK INPUT
DECODED PAGES 28-2F, 30-37, 38-3F (3 lines)
ADDRESS Lines A13, A14, A15
BUFFERED WRITE, BWR (Active Low Output)

SPECIFICATIONS

Mechanical Specifications

CARD DIMENSIONS

4.50 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
0.48 in. (1.22 cm) maximum profile thickness
0.062 in. (0.16 cm) printed circuit board thickness

CARD INCLUDES

Card ejector
One Z80 Processor
1K 8-bit bytes, 2114 RAM plus sockets for an added 1K bytes
Four ROM sockets for 2716 PROMs
Crystal clock circuit and provisions for external clock
Power-on and external reset
2 Input ports (8-bit)
3 Output ports (8-bit)

Electrical Specifications

MEMORY

PROM: 2716 or equivlent (2K x 8) 300 ns max with no wait state
RAM: 2114 or equivalent (1K x 4) 267.6 ns max with no wait state

INPUTS

2 Interrupt requests
16 Data lines (2 input ports)
1 RDY control (active high)
1 Reset Control
Port Expansion Data Bus (J2; active high)
External clock input

OUTPUTS

24 Latched Output Data lines (3 output ports)
1 clock signal
2 system resets (J3 and card edge)
Port Expansion Data Bus (J2; active high)
6 Input port strobes (J3)
5 Output port strobes (J3)

POWER REQUIREMENTS

V_{CC} = 5 Volts $\pm$ 5% at 1.2 A maximum fully loaded (100 mA per ROM, 100 mA per RAM)
GND = 0 Volts

OPERATING TEMPERATURE RANGE

0°C to 60°C

CONNECTOR REQUIREMENTS

56 pin, 28 position dual-readout on 0.125 in. (0.318 cm) centers
Printed Circuit: Viking 3VH28/1CE5
Wire Wrap: Viking 3VH28/1CN5

MD-SBC1 J1 EDGE CONNECTOR PIN LIST

Table 4

Signal	Signal Flow	Pin Number	Pin Number	Signal Flow	Signal
+5 VOLTS	IN	2	1	IN	+5 VOLTS
GROUND	IN	4	3	IN	GROUND
SPARE	I/O	6	5	I/O	SPARE
$\overline{IN0\text{-}5}$	IN	8	7	I/O	$\overline{IN1\text{-}5}$
$\overline{IN0\text{-}6}$	IN	10	9	IN	$\overline{IN1\text{-}6}$
$\overline{IN0\text{-}7}$	IN	12	11	IN	$\overline{IN1\text{-}7}$
$\overline{IN0\text{-}8}$	IN	14	13	IN	$\overline{IN1\text{-}8}$
$\overline{IN0\text{-}4}$	IN	16	15	IN	$\overline{IN1\text{-}4}$
$\overline{IN0\text{-}3}$	IN	18	17	IN	$\overline{IN1\text{-}3}$
$\overline{IN0\text{-}2}$	IN	20	19	IN	$\overline{IN1\text{-}2}$
$\overline{IN0\text{-}1}$	IN	22	21	IN	$\overline{IN1\text{-}1}$
$\overline{OUT0\text{-}1}$	OUT	24	23	OUT	$\overline{OUT0\text{-}5}$
$\overline{OUT0\text{-}2}$	OUT	26	25	OUT	$\overline{OUT0\text{-}6}$
$\overline{OUT0\text{-}3}$	OUT	28	27	OUT	$\overline{OUT0\text{-}7}$
$\overline{OUT0\text{-}4}$	OUT	30	29	OUT	$\overline{OUT0\text{-}8}$
$\overline{OUT1\text{-}1}$	OUT	32	31	OUT	$\overline{OUT1\text{-}5}$
$\overline{OUT1\text{-}2}$	OUT	34	33	OUT	$\overline{OUT1\text{-}6}$
$\overline{OUT1\text{-}3}$	OUT	36	35	OUT	$\overline{OUT1\text{-}7}$
$\overline{OUT1\text{-}4}$	OUT	38	37	OUT	$\overline{OUT1\text{-}8}$
$\overline{OUT2\text{-}1}$	OUT	40	39	OUT	$\overline{OUT2\text{-}5}$
$\overline{OUT2\text{-}2}$	OUT	42	41	OUT	$\overline{OUT2\text{-}6}$
$\overline{OUT2\text{-}3}$	OUT	44	43	OUT	$\overline{OUT2\text{-}7}$
$\overline{OUT2\text{-}4}$	OUT	46	45	OUT	$\overline{OUT2\text{-}8}$
$\overline{INTA}$	I/O	48	47	IN	$\overline{IREQ}$
$\overline{NMI}$	IN	50	49	IN	RDY
SPARE	I/O	52	51	OUT	TTLI
$\overline{RESET}$	IN	54	53	OUT	$\overline{RST}$
SPARE	I/O	56	55	I/O	SPARE

I/O PORT EXPANSION SOCKETS

Table 5

J2 Data					
Signal	**Signal Flow**	**Pin Number**	**Pin Number**	**Signal Flow**	**Signal**
D1-4	IN	16	1	IN	D1-1
D0-2	OUT	15	2	IN	D1-8
D0-4	OUT	14	3	OUT	D0-6
D0-1	OUT	13	4	OUT	D0-7
D1-7	IN	12	5	OUT	D0-3
D0-5	OUT	11	6	IN	D1-5
D0-8	OUT	10	7	IN	D1-6
D1-3	IN	9	8	IN	D1-2

J3 Control And Power					
Signal	**Signal Flow**	**Pin Number**	**Pin Number**	**Signal Flow**	**Signal**
GND	OUT	16	1	OUT	GND
$\overline{\text{IS-2}}$	OUT	15	2	OUT	$\overline{\text{BRS}}$
$\overline{\text{IS-3}}$	OUT	14	3	OUT	$\overline{\text{OS-3}}$
$\overline{\text{IS-4}}$	OUT	13	4	OUT	$\overline{\text{OS-4}}$
$\overline{\text{IS-5}}$	OUT	12	5	OUT	$\overline{\text{OS-5}}$
$\overline{\text{IS-6}}$	OUT	11	6	OUT	$\overline{\text{IS-7}}$
$\overline{\text{OS-6}}$	OUT	10	7	OUT	+5 VOLTS
$\overline{\text{OS-7}}$	OUT	9	8	OUT	+5 VOLTS

ORDERING INFORMATION

Designator	Description	Part Number
MD-SBC1		MK77851
MD-SBC1 Technical Manual	MD-SBC1 Technical Manual only	4420083

IVC MDX Series Input/Output

SYSTEM INTERRUPT UNITS

Card	SIU's
MDX-A/D12	1
MDX-A/D8	1
MDX-AIO	0
MDX-BCLK	0
MDX-BRAM	0
MDX-CPU1/1A	1
MDX-CPU2/2A	1
MDX-CPU3	1
MDX-CPU4	1
MDX-D/A8	0
MDX-D/A12	0
MDX-DEBUG	0
DIOB1	0
DIOP	0
MDX-DRAM8/16/32/64/128	0
MDX-EPROM	0
MDX-EPROM/UART	0
MDX-FLP/FLP2	1
MDX-INT	1
MDX-ISIO	1
MDX-MATH	1
MDX-MODEM	1
MDX-PFD	0
MDX-PIO	2
MDX-SASI1/2	1
SBC1	0
MDX-SC/D	1
MDX-SIO/SIO2	1
MDX-SRAM4/8/16	0
MDX-SST	0
MDX-UMC/UMC2	0
MDX-422	1

MDX-FLP2

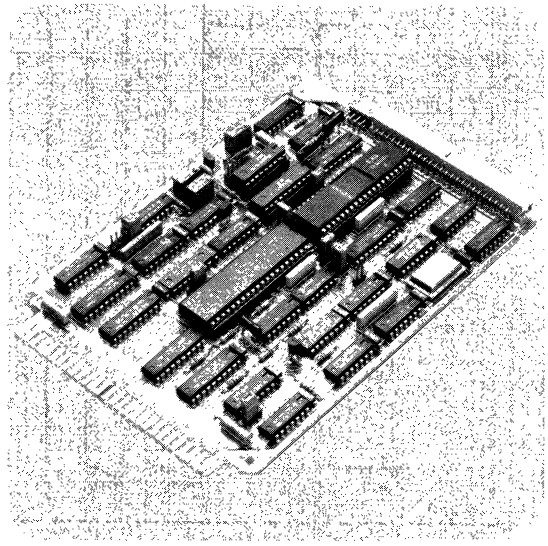
SUMMARY OF MDX-FLP2 FEATURES

- ☐ STD-Z80 Bus compatible
- ☐ Controls single and double density disk drives
- ☐ Controls single and double sided disk drives
- ☐ Controls up to four 8 inch drives; up to three 5¼ drives
- ☐ Jumper selectable to handle either 5¼ or 8 inch drives
- ☐ Up to 4 MHz operation
- ☐ Provision for priority DMA daisy chain operation
- ☐ Provision for external devices to use DMA Controller
- ☐ Jumper selectable port addresses in blocks of eight
- ☐ Jumper selectable in main port space or IOEXP space
- ☐ Jumper selectable write precompensation
- ☐ Soft sector operation, including variable-length sectors
- ☐ IBM 3740 and System 34 diskette formatting capability
- ☐ Automatic track seek with verification
- ☐ Programmable step rate
- ☐ DMA or programmed data transfer
- ☐ Interrupt driven or polled operation
- ☐ Automatic CRC generation and checking
- ☐ Single sector, multi sector or full track data transfers
- ☐ Compatible with Mostek's M/OS-80

INTRODUCTION TO MDX-FLP2

MDX-FLP2 is a floppy disk drive controller board for the STD-Z80 bus. The MDX-FLP2 board embodies all required controlling, formatting, and interface logic between the STD-Z80 bus and one to four floppy disk drives.

MDX-FLP2
Figure 1



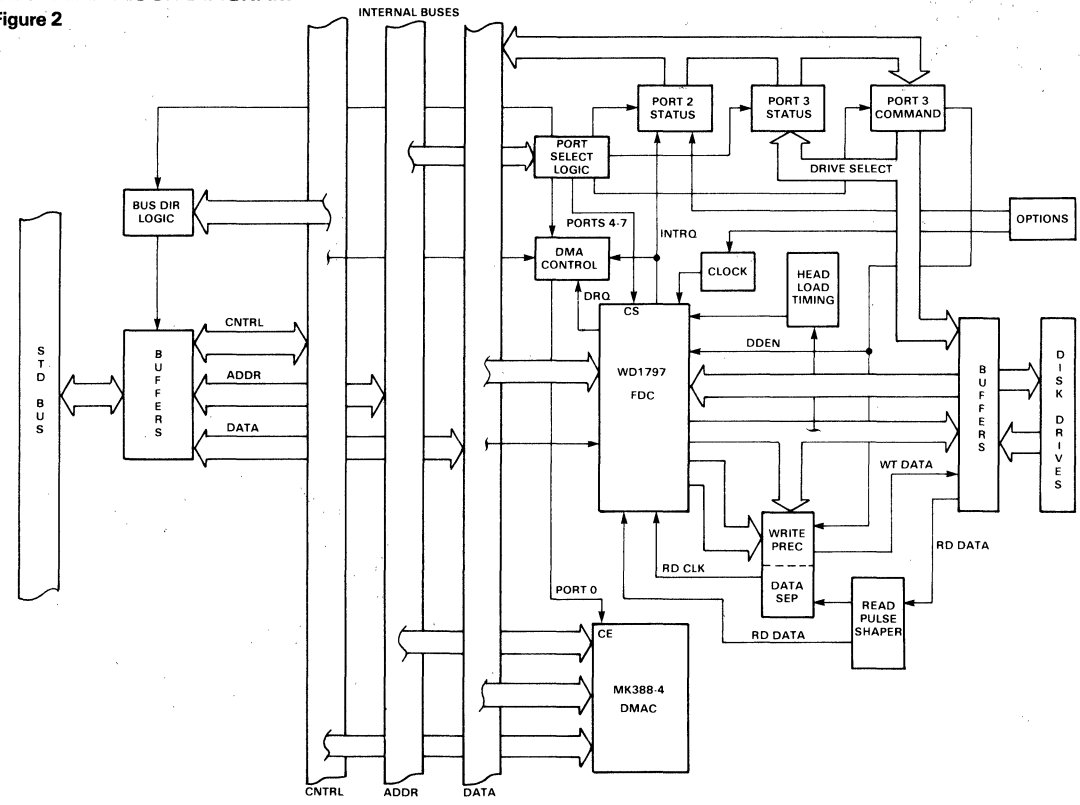
FLP2 can control both single-density, single-sided and double-density, double-sided Shugart compatible disk drives. In addition, either 5¼ or 8 inch drives may be used. Transfers to and from the disk are normally handled by the MK3883 DMA Controller; programmed data transfer is also possible. Multiple FLP2 boards can be operated simultaneously since daisy chained priority DMA operation is possible.

FLP2 operates with a wide variety of disk drives, such as drives by Shugart Associates and Remex. Either 5¼ or 8 inch drives may be used; a simple change of three straps converts FLP2 from a 5¼ inch controller to an 8 inch controller. Write precompensation is also strappable.

Since FLP2 is based on the WD1797 Floppy Controller, many advanced features are available. These include IBM 3740 or IBM System 34 diskette formatting capability, automatic track seek with verification, programmable step rate, and automatic CRC generation and checking. In addition, single sector, multi-sector, or complete track transfers are possible.

MDX-FLP2 BLOCK DIAGRAM

Figure 2



SPECIFICATIONS

Electrical Specifications

Data Bus:	8 bits, bidirectional
Address Bus:	16 bits, lower 8 bidirectional, upper 8 output during DMA activity
System Bus:	STD-Z80 Compatible
Inputs:	One 74 LS Load Max
Outputs:	I_{OH} = 15 mA min at 2.4 V
	I_{OL} = 24 mA min at 0.5 V
System Clock:	Up to 4 MHz
I/O Addressing:	8 ports on board selectable to any of 32 eight port slots by jumper options; board may be placed in main I/O space or expansion I/O space (IOEXP)
Memory Addressing:	On board DMA capable of addressing any memory address.
Power Requirements:	+12 V ± 5% @ 100 mA max + 5 V ± 5% @ 1.2 A max
Operating Temperature:	0°C to 60°C

Mechanical Specifications

Card Dimensions

4.5 in (11.43 cm) high by 6.50 in (16.51 cm) long

0.48 in (1.22 cm) maximum profile thickness

0.062 in (.16 cm) printed circuit board thickness

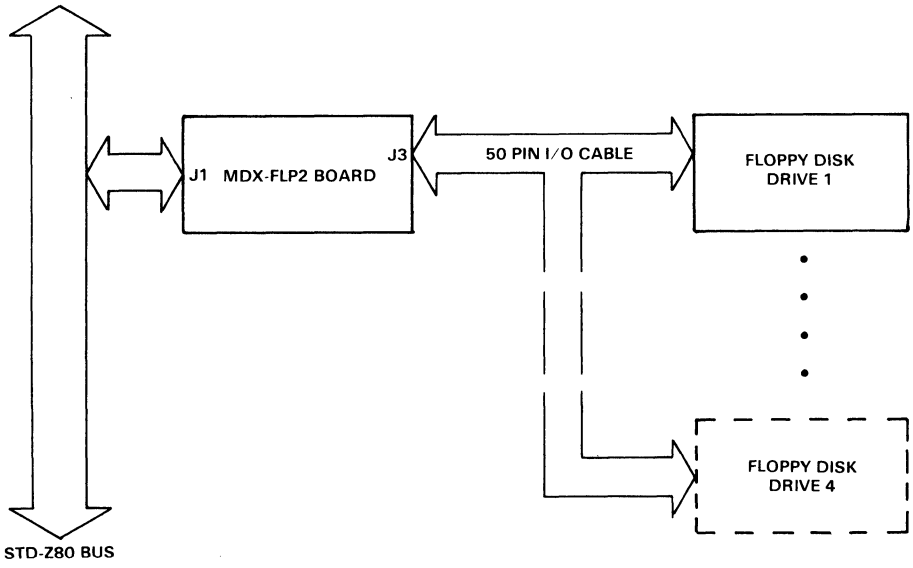
Connectors

STD-Z80 Bus (J1) - 56 pins with .125 in. center

Drive Interconnect (J3) - 50 pins with .1 in. center

SYSTEM INTER-CONNECTION DIAGRAM

Figure 3



DMA Daisy Chain (J2) - 8 pin dual right angle, .1 in. center

Mating Connector for STD Bus (J1)

P.C. 3VH28/1CE5 (Viking)

Soldertail 3VH28/1CN5 (Viking)

W. W. 3VH28/1CND5 (Viking)

Mating Connector for Drive Interconnect (J3)

609-5000 W/O Strain Relief (Ansley)

609-5001 with Strain Relief (Ansley)

Mating Connector for DMA Daisy Chain (J2)

1-86148-8 (AMP)

References

1. Western Digital 1797 Data Sheet
2. Z80A DMA Data Sheet
3. STD-Z80 Bus Technical Manual

STRAPPING OPTIONS

FLP2 is customized by changing straps. Figure 5 shows the locations of the straps, J4 - J12. The following discussion explains the purpose of each strap, and how the strap is set at the factory.

J4: Auto Precomp - When open, double density write precompensation is always in affect (provided DDEN* is low). This is primarily for 5¼ inch drives that require write precompensation on every track. When strapped, write data is precompensated only for tracks greater than 43; this is the factory setting.

J5: Test Points - Test points for factory use only.

J6: VCO Clock - This clock is either a 4 MHz clock (pins 1 and 2 strapped) for 8 inch drives or a 2 MHz clock (pins 3 and 4) for 5¼ inch drives.

J7: 8 inch Ready - When using an 8 inch drive, this strap connects the Ready signal to FLP2. When using a 5¼ inch drive, this strap is not connected. Thus 5¼ inch drives will always appear ready.

J8: 8 or 5¼ inch Clock - Strap for either a 4 MHz clock (pins 3 and 4) for 8 inch drives or a 2 MHz clock (pins 1 and 2) for 5¼ inch drives.

J9: 5¼ inch drive - This strap may be used by software to determine whether 5¼ or 8 inch drives are used. Strap J9 for 5¼ inch drives.

J10: Port Address Select - This option allows the user to place FLP2 on any of 32 possible 8-port boundaries. Figure 4 shows the various straps. Note that a strap installed implies a logic zero. The factory setting is E0H (11100XXX).

ADDRESS STRAPPING OPTIONS

Figure 4

Address	Corresponding Pins on J10	Factory Setting
A7	10 and 9	1 (not strapped)
A6	8 and 7	1 (not strapped)
A5	6 and 5	1 (not strapped)
A4	4 and 3	0 (strapped)
A3	2 and 1	0 (strapped)

J11: I/O Expand - IOEXP* is normally not used on Mostek boards. The factory straps pins 2 and 3. If the user desires to use IOEXP*, strap pins 1 and 2; also strap pins 3 and 4.

J12: EXT Ready Level - This jumper determines whether the EXT RDY input to the FLP2 DMA is active low or active high. For an active low EXT RDY, strap pins 2 and 3 (factory setting); for an active high EXT RDY, strap pins 1 and 2.

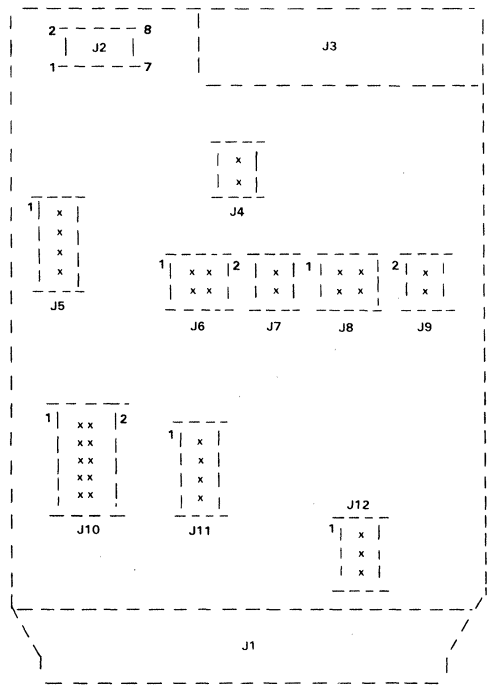
DMA DAISY CHAIN OPTION

MDX-FLP2 is designed to allow the option of multiple DMA boards in the same system. The two signals -- BAI (Bus Acknowledge In) and BAO (Bus Acknowledge Out) -- which create the priority DMA daisy chain are implemented by connecting the signals to J2, an 8-pin connector at the top of the board. In addition, pin 8 of J2 may be used for external devices -- for example a PIO or SIO -- to access the READY pin of the MK3883 DMA Controller.

The configuration of the connector is shown in Figure 6. Twisted pair cables with two-contact connectors at each end are used to connect the bus priority chain.

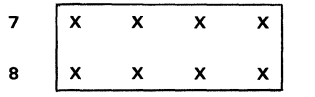
FLP2 STRAPPING LOCATIONS

Figure 5



DMA DAISY CHAIN CONNECTOR

Figure 6



J2 - TOP VIEW

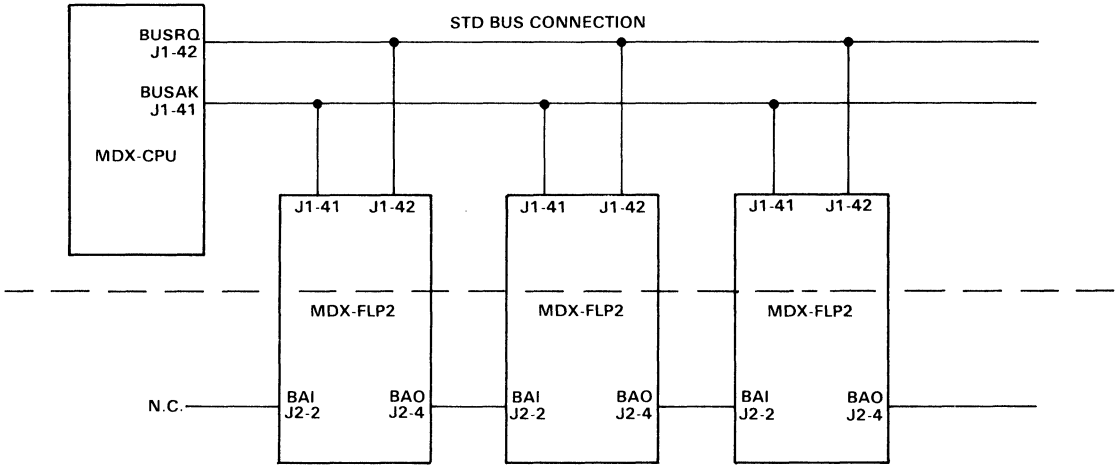
Pin No.	Function
1, 3, 5, 7	Ground
2	BAI (Bus ACK In)
4	BAO (Bus ACK Out)
6	No connection
8	External DMA Request Input

CONNECTION OF FLP2 TO DISK DRIVE

The logic interconnection from FLP2 to the disk drive is made from J3 on the FLP2 board to the appropriate connection on the drive. The connection is made with a standard .1 inch center 50 pin ribbon cable. Refer to Figure 8.

MDX-FLP2 MULTIPLE DMA BUS PRIORITY CONNECTIONS

Figure 7



NOTE: EACH MDX-FLP2 CONTROLLER MUST BE STRAPPED FOR DIFFERENT I/O ADDRESS

IVC

CABLE CONNECTION PIN DEFINITIONS FOR J3

Figure 8

Signal	Description	Pin Number
Drive Select 1,2,3,4	Output	26,28,30,32
Side Select	Output	14,48 (see note)
Step	Output	36
Write Data	Output	38
Write Gate	Output	40
Direction	Output	34
Head Load	Output	18
Track greater than 43	Output	2
Read Data	Input	46
Index	Input	24 (5 in.) or 20 (8 in.)
Track 00	Input	42
Write Protect	Input	44
Drive Ready	Input	22
2 Sided	Input	10

NOTES:

1. Please compare your drive interface connector prior to hooking up the MDX-FLP2. Some exclusions to the standard interface are listed below.
2. Some 8" drives have an optional DATA SEPARATOR output on pin 48. If this is true on your drive, cut the etch on the FLP2 board going to pin 48 on J3.
3. FLP2 board has J3 Pin 20 (INDEX 8") and J3 pin 24 (INDEX 5") tied together. Pin 20 is used as SECTOR output on some 8" drives. Pin 24 is used as the IN USE input on some 5¼" drives.
4. Drive SEL4 input is available on some 5¼" drives at the FLP2 connection J3 pin 22.
5. J3-12, a no-connect on the FLP2 board, is a disk change status indicator on some 8" drives.

I/O PORTS

The MDX-FLP2 board occupies a block of eight contiguous I/O port addresses. This block of eight can be strapped anywhere in the main or IOEXP* address space. As shipped from the factory, the eight ports reside at E0H through E7H in the main port address space. Figure 9 shows the utilization of the eight ports.

PORT UTILIZATION ON FLP2
Figure 9

	b7 b0	b7 b0
A2-A0	**Read**	**Write**
0 0 0	MK3883 DMA Controller IC	MK3883 DMA Controller
0 0 1	Undefined	Not used
0 1 0	XX FB SZ XX XX XX IR SS	Not used
0 1 1	XX XX XX XX D4 D3 D2 D1	SD RS XX XX D4 D3 D2 D1
1 0 0	1797 Status Register	1797 Command Register
1 0 1	1797 Track Register	1797 Track Register
1 1 0	1797 Sector Register	1797 Sector Register
1 1 1	1797 Data Register	1797 Data Register

Where:

xx = Don't care
FB = 1 FLP 1 Board; FB = 0 FLP2 board
SZ = 1 8 inch drive; SZ = 0 5 inch drive
IR = 1 1797 interrupt; IR = 0 no 1797 IRQ
SS = 1 2-sided disk; SS = 0 single sided
SD = 1 single density; SD = 0 double density
RS = 1 1797 active; RS = 0 1797 RESET
D4 = 1 select drive four; D4 = 0 no select
D3 = 1 select drive three; D3 = 0 no select
D2 = 1 select drive two; D2 = 0 no select
D1 = 1 select drive one; D1 = 0 no select

MDX-SASI*-1

SUMMARY OF MDX-SASI-1 FEATURES

- ☐ STD-Z80 Bus compatible
- ☐ Supports Shugart Associates System Interface (SASI*)
- ☐ Polled or interrupt driven
- ☐ Up to 4 MHz operation
- ☐ I/O EXP supported
- ☐ External ready output
- ☐ 5 Volt operation
- ☐ Four address I/O port block
- ☐ Auto acknowledge logic
- ☐ Activity LED

INTRODUCTION TO MDX-SASI-1

MDX-SASI-1 interfaces the STD-Z80 bus to Shugart Associates System Interface (SASI). SASI is a universal systems interface that lets OEMs upgrade, mix, and interchange peripherals without affecting software. SASI is an intelligent systems interface, which results in easy peripheral integration.

MDX-SASI-1 may be strapped on any four port boundary. In addition, the IOEXP signal is supported. The board contains an external READY output, which may be used with an external DMA board. For example, the external ready output of MDX-SASI-1 may be connected to the external ready input of the MDX-FLP2. Thus, the DMA on the MDX-FLP2 may be used with the MDX-SASI-1.

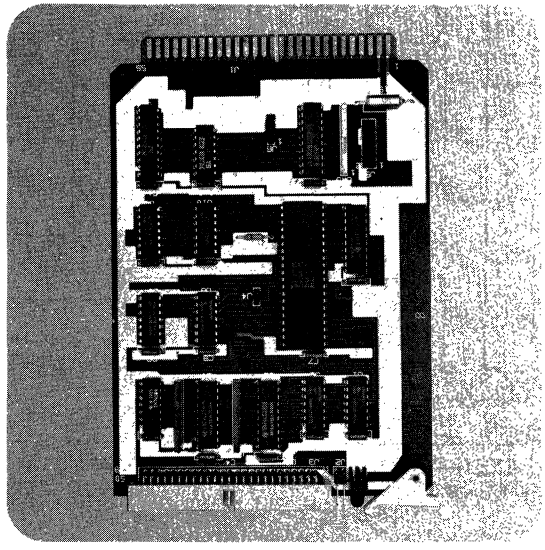
MDX-SASI-1 also contains an activity LED. The LED lights when the board is addressed. This is useful for debugging both software and hardware.

The board contains auto acknowledge logic. This logic may be strapped to automatically assert the ACK signal after reading or writing to/from the SASI bus. This allows an increase in throughput, since the software does not have to "bit toggle" the ACK signal.

MDX-SASI-1 is a low cost, medium performance interface.

*SASI is a trademark of Shugart Associates

MDX-SASI-1
Figure 1



At 4 MHz, MDX-SASI-1 has a maximum transfer rate of 1 byte/5 μsec. As a comparison, a double-sided, double-density floppy disk has a transfer rate of 1 byte/16 μsec.

SPECIFICATIONS

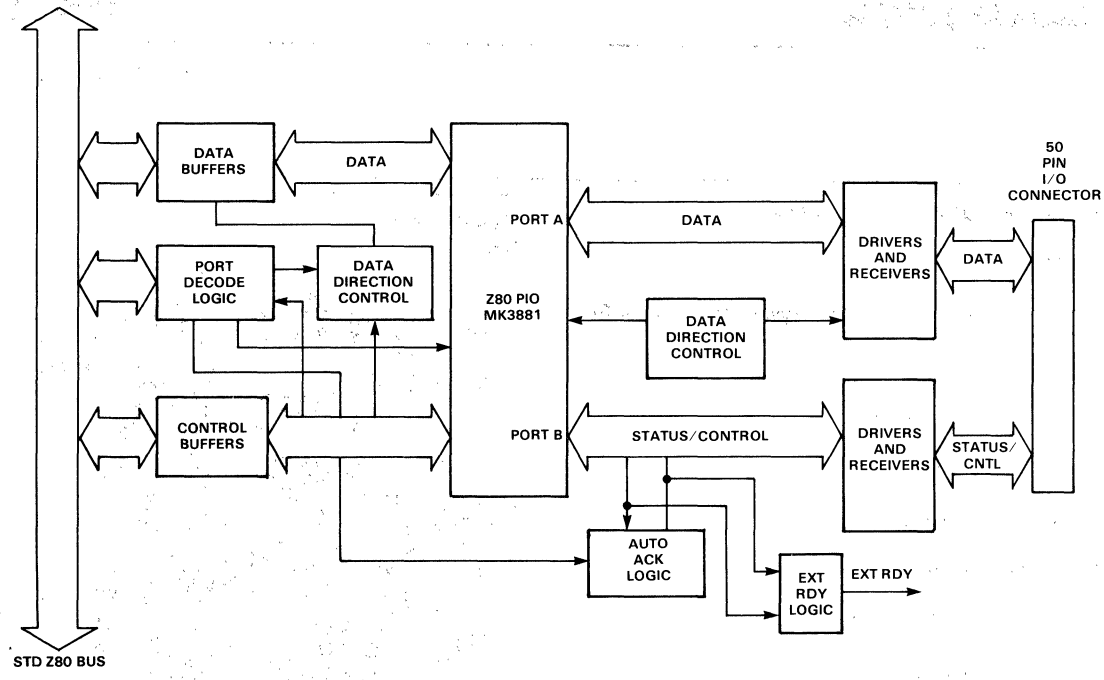
Electrical Specifications

Data Bus:	8 bits, bidirectional
Address Bus:	8 bits (plus optional IOEXP)
System Bus:	STD-Z80 compatible
Inputs:	One 74 LS Load Max
Outputs:	I_{OH} = 15 mA min at 2.5 V I_{OL} = 24 mA min at 0.5 V
Interrupts:	Mode 2 Vectored Interrupts generated. Interrupt vector programmable upon initialization. Daisy-chained interrupt priority.

IVC

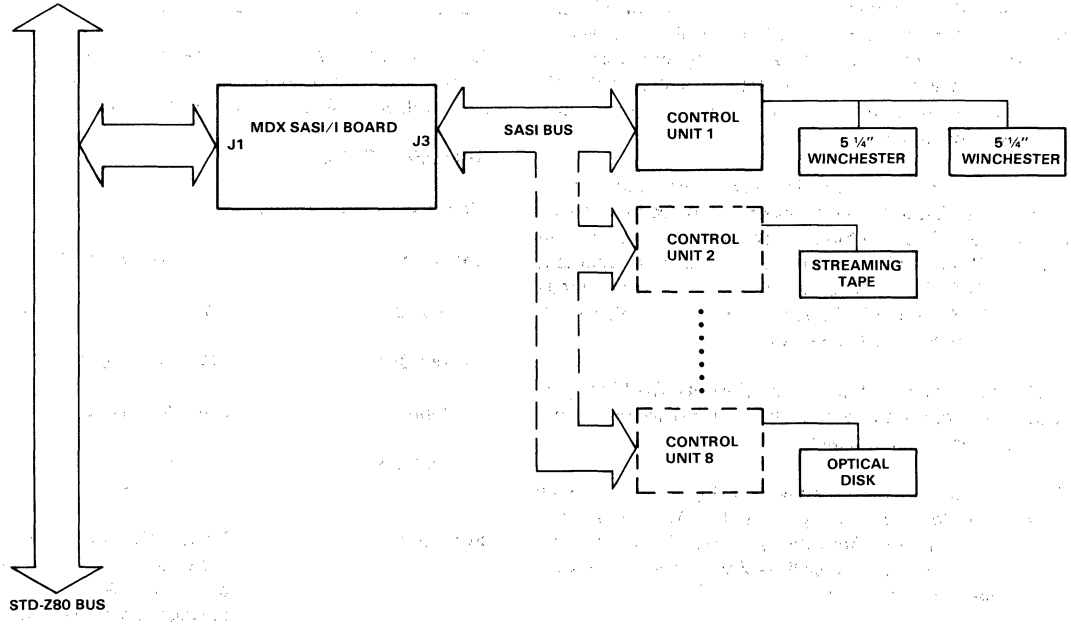
MDX-SASI-1 BLOCK DIAGRAM

Figure 2



SYSTEM INTER-CONNECTION DIAGRAM

Figure 3



SPECIFICATIONS CONT.

System Interrupt Units (S.I.U.) = 1

System Clock: Up to 4 MHz

I/O Addressing: 4 ports on board selectable to any of 64 four port slots by jumper options; board may be placed in main I/O space or expansion I/O space (IOEXP)

Power Requirements: +5 V ± 5% @ .8 A max

Operating Temperature: 0°C to 60°C

Mechanical Specifications

Card Dimensions

4.5 in (11.43 cm) high by 6.50 in (16.51 cm) long

0.48 in (1.22 cm) maximum profile thickness

0.062 in (.16 cm) printed circuit board thickness

Connectors

STD Bus (J1): 56 pins with .125 in. centers

SASI Interface: 50 pins with .1 in. centers

External Ready: 2 pin right angle, .1 in. centers

STRAPPING OPTIONS

Figure 5 shows the locations of the strapping options, J2, J4, J5 and J6. The following discussion explains the purpose of each strap, and how the strap is set at the factory.

J2: External Ready Output (J2 pin 2) - This is an active high signal which may be connected to an external DMA board. External Ready goes HIGH when the REQ (request) signal goes low, which signals that data is available on the SASI data bus. Clearing of External Ready occurs by reading from the MDX-SASI-1 data port (port 0). Note that pin 2 is the External Ready Output, while pin 1 is ground.

J4: Auto Acknowledge Enable - The factory straps J4 to enable the Auto Acknowledge logic. This results in the SASI ACK signal being automatically asserted when a read or write occurs from the data port (port 0); the ACK signal is cleared when the SASI REQ signal is deasserted. The auto acknowledge feature allows a higher throughput on the SASI bus, since the programmer does not have to "toggle" the SASI ACK signal. If Auto Acknowledge is not desired -- for example to debug a controller board -- remove J4.

J5: Port Select - The board may be placed on any four port boundary by changing J5. The factory setting is A0H. The pins on J5 are defined in Figure 4. Note that a jumper installed gives a logic zero.

J6: I/O Expand - IOEXP* is normally not used on Mostek boards. Thus, the factory straps pins 2 and 3. If the user desires to use the IOEXP*, strap pins 1 and 2; also strap pins 3 and 4.

ADDRESS STRAPPING OPTIONS

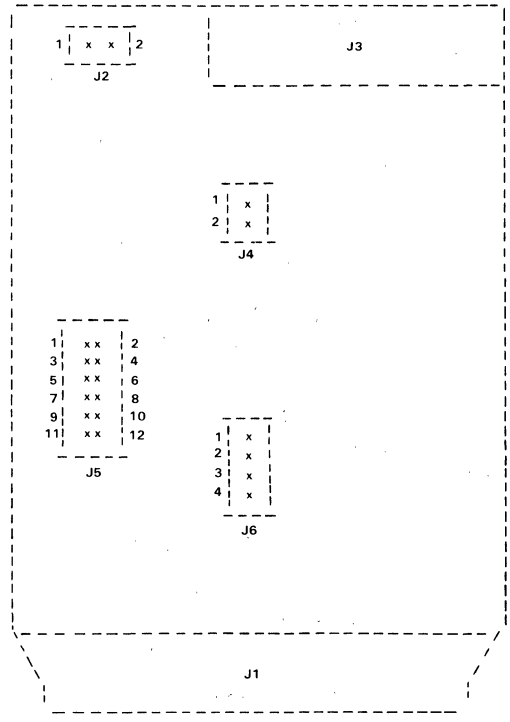
Figure 4

Address	Corresponding Pins on J5	Factory Strapping
A7	1 and 2	1 (not strapped)
A6	3 and 4	0 (strapped)
A5	5 and 6	1 (not strapped)
A4	7 and 8	0 (strapped)
A3	9 and 10	0 (strapped)
A2	11 and 12	0 (strapped)

NOTE: A jumper installed gives a logic zero.

MDX-SASI-1 STRAPPING LOCATIONS

Figure 5



IVC

CONNECTION TO THE SASI BUS

Figure 6 shows the pin definitions of J3, the 50 pin connector for connecting the MDX-SASI-1 to the SASI bus. Note that the SASI bus is divided into a data section and a control section. All but two of the SASI bus signals are supported by MDX-SASI-1. The data bus parity bit is not supported by MDX-SASI-1. Also, ATN (attention) is not suppported.

To connect MDX-SASI-1 to the SASI bus, connect a 50 pin cable from J3 on the MDX-SASI-1 board to the required connector on the SASI controller board.

STD BUS CONNECTOR (J1)

The STD Bus Connector is a standard 56 pin card edge connector. See STD-Z80 Bus Specification 4420094.

I/O PORTS

The MDX-SASI-1 board occupies a block of four contiguous I/O port addresses. The block of four can be strapped anywhere in the main or IOEXP* address space. As shipped from the factory, the four main ports reside at A0 hex through A3 hex in the main port address space. Figure 7 shows the utilization of the four ports.

J3 CONNECTIONS

Figure 6

Pin No.	Signal	
2	DB0 (data bit 0, LSB)	SASI Data Bus
4	DB1 (data bit 1)	
6	DB2 (data bit 2)	
8	DB3 (data bit 3)	
10	DB4 (data bit 4)	
12	DB5 (data bit 5)	
14	DB6 (data bit 6)	
16	DB7 (data bit 7, MSB)	
18	Not used (data bus parity)	
20	Not used	
22	Not used	
24	Not used	
26	Not used	
28	Not used	
30	Not used	
32	Not used	
34	Not used (ATN, attention)	SASI Control Bus
36	BSY (busy)	
38	ACK (acknowledge)	
40	RST (reset)	
42	MSG (message)	
44	SEL (select)	
46	C/D (control/data)	
48	REQ (request)	
50	I/O (input/output)	

NOTE: All odd pins are ground.

PORT UTILIZATION

Figure 7

A1	A0	Read/Write
0	0	PIO Port A Data (SASI Data Signals)
0	1	PIO Port B Data (SASI Control Signals)
1	0	PIO Port A Control Register
1	1	PIO Port B Control Register

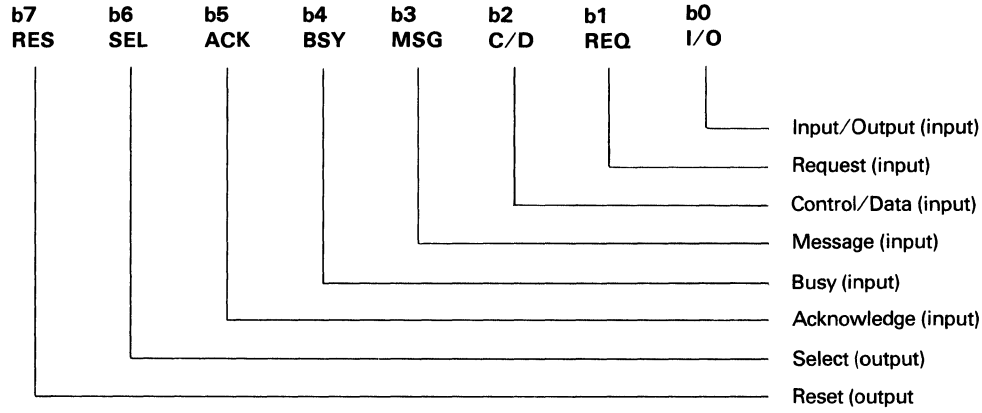
PROGRAMMING NOTES

REFERENCE INFORMATION

Z80 Data Book
Z80 Programming Manual
PIO Data Sheet
MOS/80 Users' Manual
SASI Bus Specification - Preliminary

PORT UTILIZATION ON MDX-SASI-1
Figure 8

Status Control Port Definitions (Port B on PIO):



Note that Port B is programmed for BIT CONTROL MODE. Bits b0-b5 are configured for inputs while b7 and b6 are outputs.

MDX-SASI-2

SUMMARY OF MDX-SASI-2 FEATURES

- ☐ STD-Z80 Bus Compatible
- ☐ 5 Volt Operation
- ☐ Supports Shugart Associates System Interface (SASI)*
- ☐ Polled or Interrupt Driven
- ☐ Mode 2 Interrupt Capability
- ☐ 2.5 to 4 MHz Operation
- ☐ Eight Address I/O Port Block
- ☐ I/O EXP Supported
- ☐ Auto Acknowledge Logic
- ☐ On-Board DMA Controller
- ☐ External DMA Request Supported
- ☐ DMA Daisy Chain Supported
- ☐ External Wait Request Supported

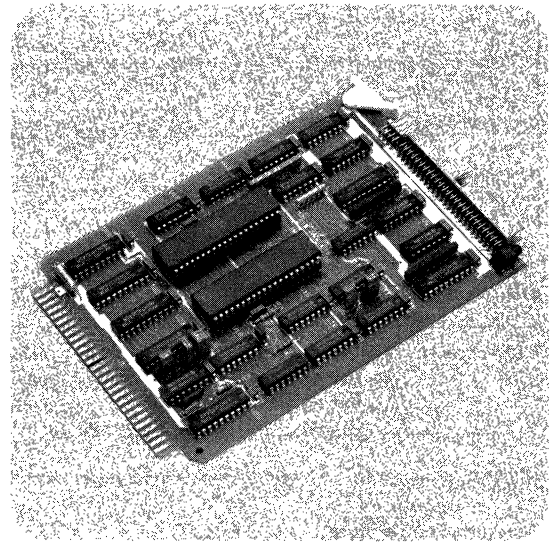
DESCRIPTION

The MDX-SASI-2 interfaces the STD-Z80 Bus to Shugart Associates System Interface (SASI). SASI is a universal systems interface that lets OEMs upgrade, mix, and interchange peripherals without affecting software. SASI is an intelligent systems interface, which results in easy peripheral integration.

MDX-SASI-2 addressing may be strapped for any eight port boundary in the STD-Z80 I/O space. In addition, the /IOEXP signal is supported for maximum configuration flexibility. The board contains an on-board DMA controller for increased throughput. An external request input allows other boards in the system to use this controller as well. The STD-Z80 /WAITRQ signal can be used to speed-match the DMA to slower memories, and DMA daisy-chaining is provided for via an additional connector.

The board also contains auto acknowledge logic. This strapping option provides automatic handshaking for SASI information transfers, and is essential to the board's DMA operation. If finer control is required for debugging purposes, the auto acknowledge can be disabled.

MDX-SASI-2
Figure 1



MDX-SASI-2 is a medium cost, high performance interface. At 4 MHz, MDX-SASI-2 has a maximum transfer rate of 570 Kbytes/sec. In comparison, a double-sided, double-density floppy disk has a transfer rate of 62.5 Kbytes/sec.

SPECIFICATIONS

Electrical Specifications

System Bus: STD-Z80 Compatible

Inputs: One 74 LS Load Max

Outputs: I_{OH} = 15 mA min at 2.5 V
I_{OL} = 24 mA min at 0.5 V

Interrupts: Mode 2 Vectored Interrupts generated. Interrupt vector programmable upon initialization. Daisy-chained interrupt priority.

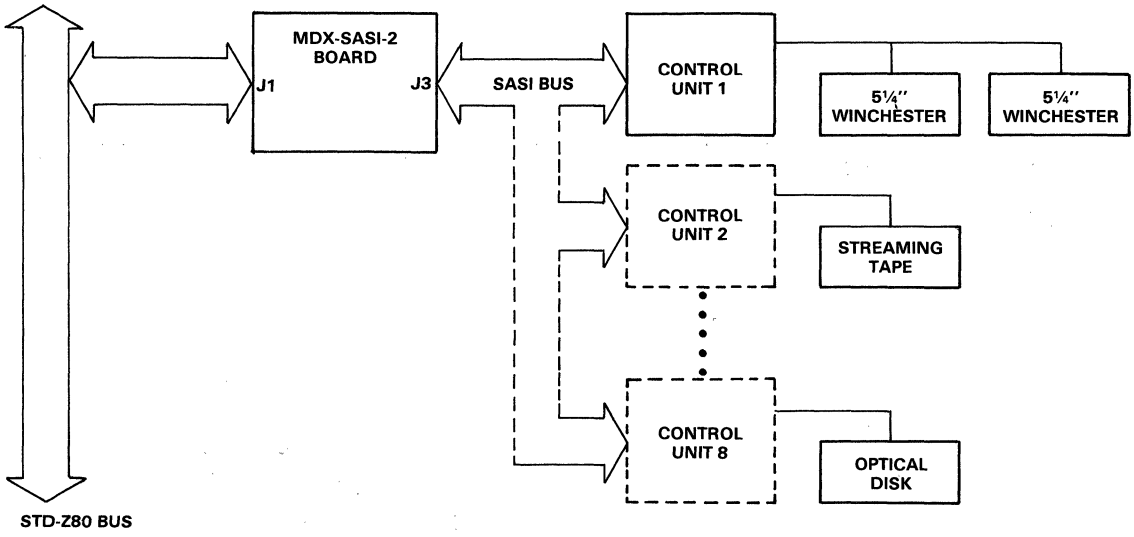
System Interrupt Units (S.I.U.) = 2

System Clock: 2.5 to 4 MHz

*SASI is a trademark of Shugart Associates.

SYSTEM INTER-CONNECTION DIAGRAM

Figure 2



I/O Addressing: 8 ports on board selectable to any of 32 eight port slots by jumper options; board may be placed in main I/O space or expansion I/O space (/IOEXP)

Power Requirements: +5 V ± 5% @ 1.1A max

Operating Temperature: 0°C to 60°C

Mechanical Specifications

Card Dimensions

4.5 in (11.43 cm) high by 6.50 in (16.51 cm) long

0.48 in (1.22 cm) maximum profile thickness

0.062 in. (.16 cm) printed circuit board thickness

Connectors

J1 - STD-Bus:
56 pin dual readout edge connector;
0.125 in. centers
Mating connectors:
PCB - Viking 3VH28/1CE5
W/W - Viking 3VH28/1CND5
SDR LUG - Viking 3VH28/1CN5

J2 - External Ready / DMA Daisy Chain:
2 x 4, 0.025" square pins;
0.1 inch centers, right angle

J3 - SASI Interface:
Shrouded 2 x 25, 0.025" square pins;
0.1 inch centers, right angle
Mating connectors:
Winchester 51-1150
Berg 65485-022

STRAPPING OPTIONS

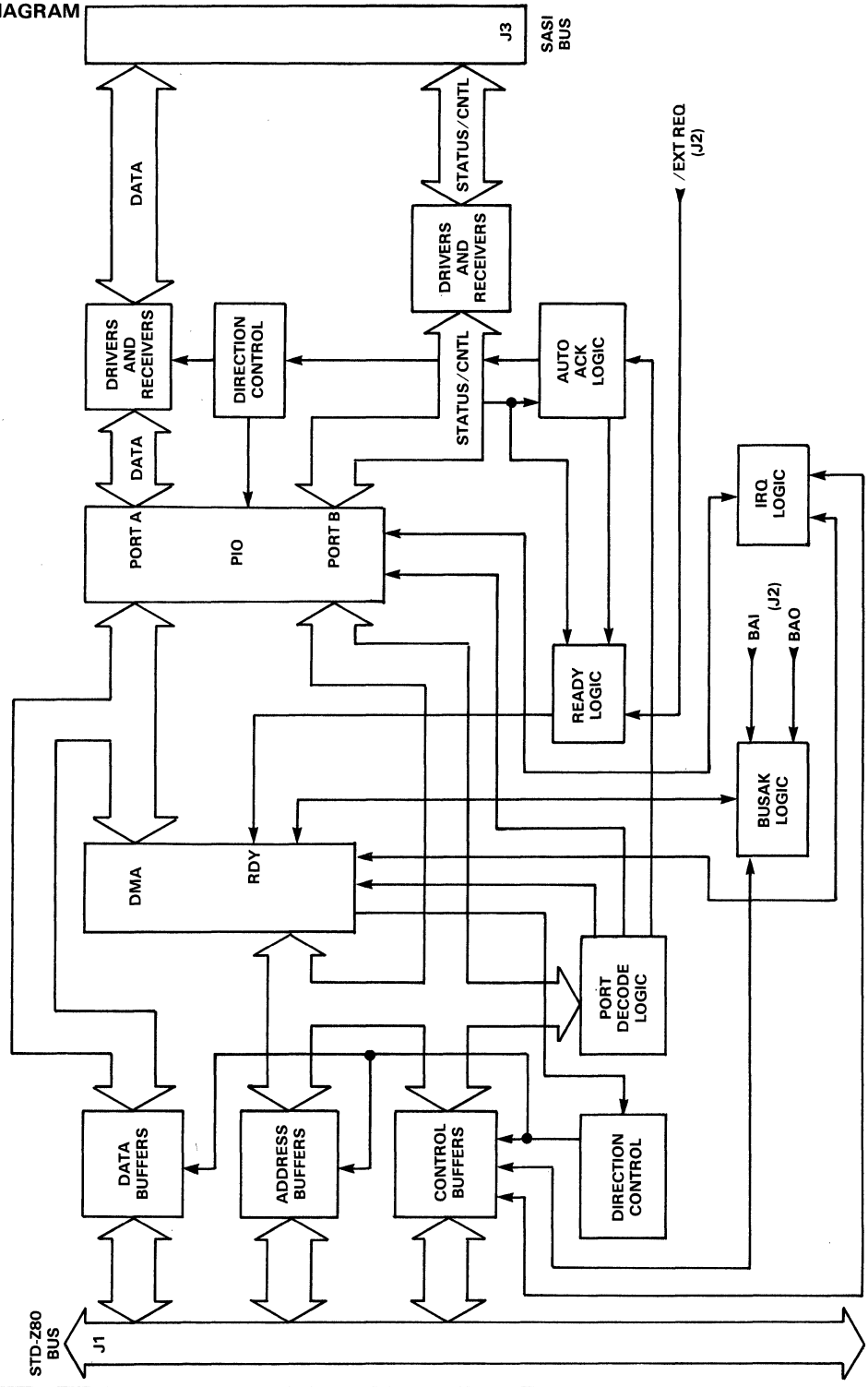
Figure 4 shows the location of the strapping options J4, J5, J6, and J7. The following discussion gives the purpose of each strap and how the strap is set at the factory.

J4: /EXT REQ Level - This jumper determines whether the /EXT REQ input to MDX-SASI-2 is active low or active high. For an active high /EXT REQ, strap pins 1 and 2; for an active low /EXT REQ, strap pins 2 and 3 (factory setting).

J5: Auto Acknowledge Enable - The factory straps J5 to enable the Auto Acknowledge logic. This circuit will carry out the SASI bus handshake on information transfers without requiring the CPU to bit toggle control lines (SASI ACK). J5 must be strapped if DMA operation is desired. If the user needs to explicitly bit toggle the SASI ACK line --e.g. to debug a contoller board -- the J5 strap should be removed.

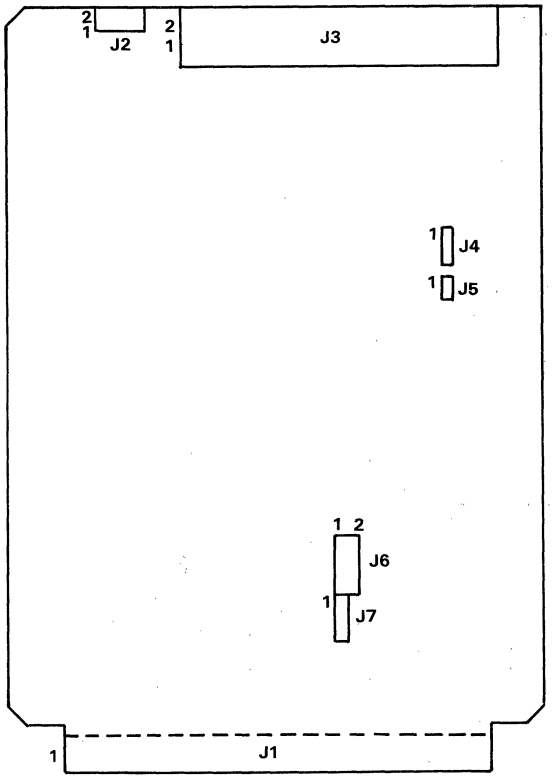
J6: Port Select - The board may be placed on any eight port boundary by changing J6. The factory setting is port A0H, for compatibility with Mostek's M/OS-80 Flexible Disk Operating System (see reference section). The pins on J6 are defined in Figure 5. Note that a strap installed implies a logic zero.

MDX-SASI-2
BLOCK DIAGRAM
Figure 3



MDX-SASI-2 BOARD OUTLINE AND HEADER LOCATIONS

Figure 4



ADDRESS STRAPPING OPTIONS

Figure 5

Address	Corresponding Pins on J6	Factory Setting (A0H)	
A3	1 and 2	strapped	(0)
A4	3 and 4	strapped	(0)
A5	5 and 6	not strapped	(1)
A6	7 and 8	strapped	(0)
A7	9 and 10	not strapped	(1)

J7: I/O Expand - This jumper allows the /IOEXP line to be included or ignored in the address decoding of MDX-SASI-2. Strapping pins 2 and 3 causes /IOEXP to be ignored (factory setting). If a given board is to be selected on /IOEXP = 0, strap pins 1 and 2, then pins 3 and 4. To cause board selection when /IOEXP = 1, strap pins 1 and 2 only.

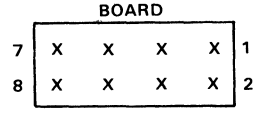
Multiple DMA Option

MDX-SASI-2 is designed to support the operation of multiple DMA devices in a system. Two signals -- BAI (Bus Acknowledge In) and BAO (Bus Acknowledge Out) -- provide for the connection of a priority DMA daisy chain. Figure 6 shows their locations on connector J2. As an example, suppose a system requires the use of four MDX-SASI-2 boards. As shown in Figure 7, the highest priority board would be DMA device 1, while the lowest priority board would be DMA device 4. Thus, MDX-SASI-2 boards are prioritized for multiple DMA operation by their electrical position in a system, as determined by their J2 interconnections, Typically, twisted pairs (signal + ground) are used to connect the bus priority chain.

Pin 8 of J2 provides an external request input (/EXT REQ), whereby other STD-Z80 I/O cards without on-board DMA capability can 'borrow' it from MDX-SASI-2. This is done by feeding a card's DMA request signal through /EXT REQ to the READY pin of the MK3883 Z80-DMA chip on MDX-SASI-2. /EXT REQ can be active low or active high (strap J4).

J2 CONNECTOR PIN DEFINITIONS

Figure 6

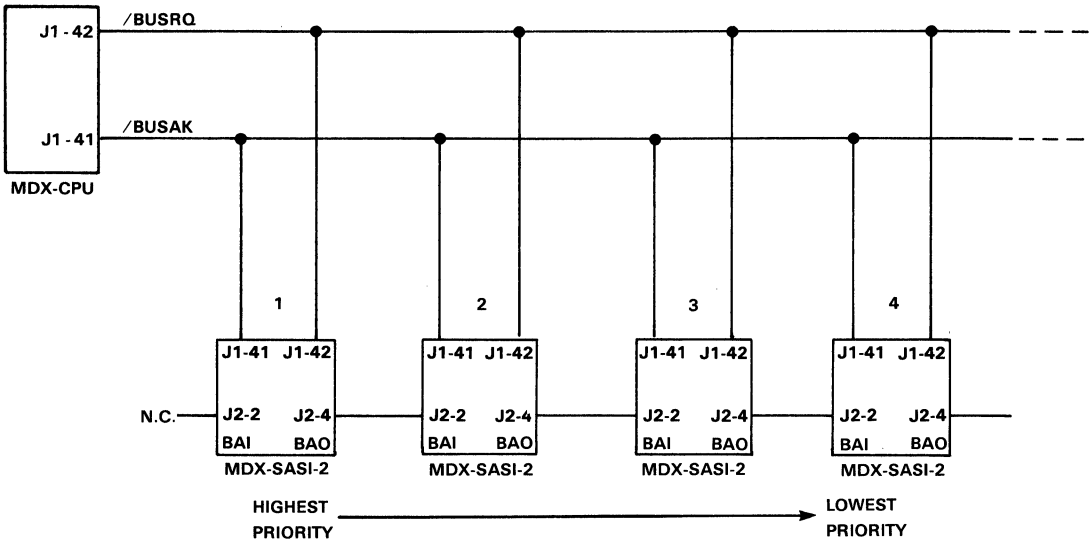


J2 - TOP VIEW

Pin No.	Function
1, 3, 5, 7	Ground
2	BAI (Bus ACK In)
4	BAO (Bus ACK Out)
6	No connection
8	External DMA Request Input (/EXT REQ)

CONNECTION OF DMA DAISY CHAIN

Figure 7



CONNECTION TO THE SASI BUS

The following shows the pin definitions of J3, the 50 pin connector to the SASI bus. Note that the SASI bus is divided into a data section and a control section. Except for the data bus parity line (pin 18) and the ATN (attention) line (pin 34). MDX-SASI-2 fully supports the SASI bus. Parity is a SASI bus option while ATN is not widely used by SASI peripheral controllers.

NOTE: All odd pins are ground.

Pin. No.	Signal	
2	DB0 (data bit 0, LSB)	SASI Data Bus
4	DB1 (data bit 1)	
6	DB2 (data bit 2)	
8	DB3 (data bit 3)	
10	DB4 (data bit 4)	
12	DB5 (data bit 5)	
14	DB6 (data bit 6)	
16	DB7 (data bit 7, MSB)	
18	Not used (data bus parity)	
20	Not used	
22	Not used	
24	Not used	
26	Not used	
28	Not used	
30	Not used	
32	Not used	
34	Not used (ATN, attention)	SASI Control Bus
36	BSY (busy)	
38	ACK (acknowledge)	
40	RST (reset)	
42	MSG (message)	
44	SEL (select)	
46	C/D (control/data)	
48	REQ (request)	
50	I/O (input/output)	

Programmer's Model of MDX-SASI-2

MDX-SASI-2 is compatible with any STD-Z80 bus system. The board consumes eight contiguous I/O port locations, beginning on any 8-byte boundary as strapped by the user. This is illustrated in the table below.

A7	A6	A5	A4	A3	A2	A1	A0	Function
X	X	X	X	X	0	0	0	PIO Port A Data (Bidirectional)
X	X	X	X	X	0	0	1	PIO Port B Data (Bit Control Mode)
X	X	X	X	X	0	1	0	PIO Port A Control
X	X	X	X	X	0	1	1	PIO Port B Control
X	X	X	X	X	1	0	0	DMA Controller
X	X	X	X	X	1	0	1	Reserved
X	X	X	X	X	1	1	0	Reserved
X	X	X	X	X	1	1	1	Reserved

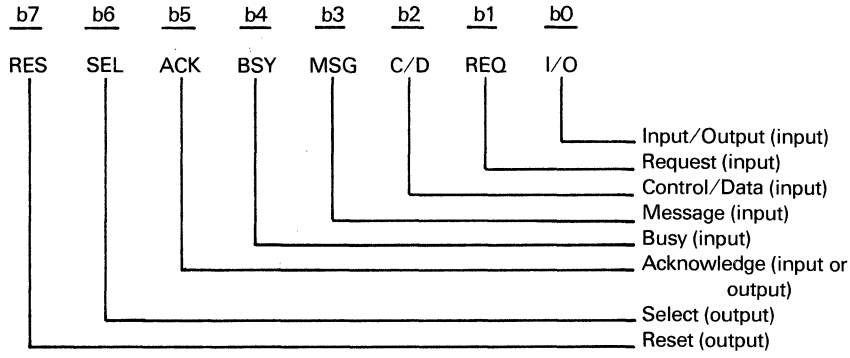
Where X = Port Strapping options on the MDX-SASI-2 Board.

PIO Port A Data is used as a bidirectional data port. It is connected in hardware to the data portion of the SASI bus. PIO Port B Data is used in bit control mode in order to implement the control portion of the SASI bus. The bit definitions of these two ports are shown below.

SASI Data Port Definitions (PIO Port A):

a7	a6	a5	a4	a3	a2	a1	a0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

SASI Control Port Definitions (PIO Port B):



Note that if auto ack is strapped for use, then b5 on the PIO should be programmed as an input. If auto ack is disabled, b5 should be programmed as an output.

STD-Z80 Bus Signals Used by MDX-SASI-2

The following is a list of STD-Z80 Bus signals used by the MDX-SASI-2 board. Pin numbers without a description are not used by MDX-SASI-2. The signals are accessed via J1, a 56 pin PC edge connector.

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	+5	5 VDC system power	2	+5	5 VDC system power
3	GND	System Ground	4	GND	System Ground
5			6		
7	D3	Data bit 3	8	D7	Data bit 7
9	D2	Data bit 2	10	D6	Data bit 6
11	D1	Data bit 1	12	D5	Data bit 5
13	D0	Data bit 0	14	D4	Data bit 4
15	A7	Address bit 7	16		
17	A6	Address bit 6	18		
19	A5	Address bit 5	20		
21	A4	Address bit 4	22		
23	A3	Address bit 3	24		
25	A2	Address bit 2	26		
27	A1	Address bit 1	28		
29	A0	Address bit 0	30		
31	/WR	Write	32	/RD	Read
33	/IORQ	IO Request	34		
35	/IOEXP	IO Expand	36		
37			38		
39	/M1	Machine Cycle	40		
41	/BUSAK	Bus Acknowledge	42	/BUSRQ	Bus Request
43	/INTAK	Interrupt Acknowledge	44	/INTRQ	Interrupt Request
45	/WAITRQ	Wait Request	46		
47	/SYSRST	System Reset	48		
49	/CLOCK	System Clock	50		
51	PCO	Priority Chain Out	52	PCI	Priority Chain In
53			54		
55			56		

REFERENCES

System Design Using the Mostek STD-Z80 Bus
-- Publication No. 4420237

Mostek 1982/1983 Microelectronic Data Book

M/OS-80 Flexible Disk Operating System - Operation Manual
-- Publication No. 4420064

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-SASI2	SASI2 module (including Technical Manual)	MK77679
MDX-SASI2 Technical Manual	SASI2 Technical Manual only	4420346

PRODUCT BRIEF

MDX-488

FEATURES

- ☐ IEEE 488-1978 INTERFACE (GPIB)
- ☐ Performs all functions of Talker, Listener, and Controller
- ☐ Onboard Z-80 for local intelligence
- ☐ Two BYTEWYDE™ sockets for ROM/RAM
- ☐ GPIB data rates of up to 400K bytes per second using onboard DMA
- ☐ STD-Z80 Bus compatable

MDX-488 DESCRIPTION

The MDX-488 is an intelligent STD-Z80 module designed to simplify the implementation of the IEEE 488 General Purpose Interface Bus. The board has a Z-80 microprocessor, memory, a DMA controller, and hardware to implement the full IEEE 488 specification for Talker, Listener, and Controller. When used as GPIB controller in multicontroller systems, the MDX-488 can be restricted from being the system controller.

ELECTRICAL SPECIFICATIONS

STD-Z80 Bus Compatable

System Interrupt Units:

1 SIU

Operating Temperature:

0°C to 60°C

Power Supply Requirements:

+5 VDC

PRODUCT BRIEF

MDX-ISIO

FEATURES

- ☐ STD-Z80 Bus compatible
- ☐ On-board processor
- ☐ On-board DMA controller for intra- and inter-bus data transfers
- ☐ Two BYTEWYDE™ memory sockets
- ☐ Inter-bus command transfer via a two port register array
- ☐ Two serial channels
- ☐ Multi-mode operation:
  - Full- and half-duplex operation
  - Synchronous and Asynchronous modes
  - Standard Baud rates to 19.2 K Baud
- ☐ Multi-protocol support
- ☐ Supports all Z80 interrupt modes
- ☐ Self-test capability with LED indicator

MDX-ISIO DESCRIPTION

The MDX-ISIO is a general purpose intelligent STD-Z80 module designed to simplify the implementation of serial communications networks. The board contains a microprocessor and required support hardware, a DMA controller, and a two port serial communications controller. The local processor and its support components make up the Local Intelligence Bus (LIB). The MDX-ISIO will appear to the STD-Z80 bus as a block of I/O mapped registers. Commands, command parameters, and status information may be passed between the STD-Z80 bus and the LIB through these registers. The on-board DMA controller may be used for transferring data between the serial communications controller and the local memory in a high speed communications link (intra-bus transfer), or for transferring data between the local memory and STD-Z80 system memory (inter-bus transfer).

The architecture of the MDX-ISIO allows the user to implement any level of control through his firmware and software. As a minimum, the local processor may be used to initialize the on-board components and take care of "house keeping" tasks. At the other extreme, the user might implement a high level algorithmic controller for the industrial environment.

ELECTRICAL SPECIFICATIONS

STD-Z80 Bus Compatible

System Interrupt Units:

1 SIU

Operating Temperature Range:

0°C to 60°C

Power Supply Requirements:

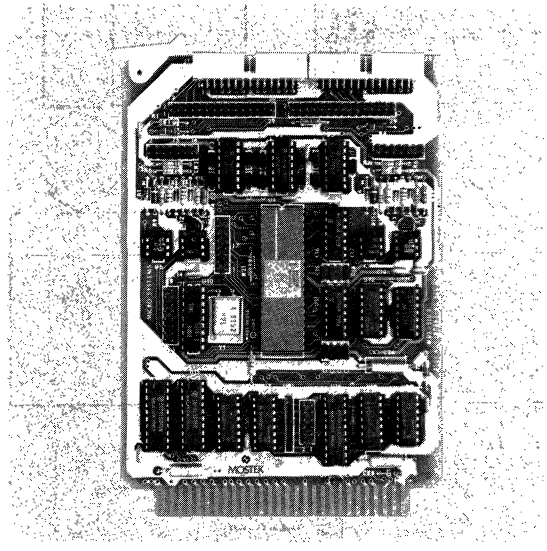
+5 Volts
+12 Volts
-12 Volts

MDX-SIO2

FEATURES

- ☐ Two independent full-duplex channels
- ☐ Independent programmable Baud rate clocks
- ☐ Asynchronous data rates, 12.5 to 19.2K bits per second
- ☐ Receiver data registers quadruply buffered
- ☐ Transmitter double buffered
- ☐ Asynchronous operation
- ☐ Binary synchronous operation
- ☐ HDLC or SDLC operation
- ☐ Both CRC-16 and CRC-CCITT (-0 and -1) hardware implemented
- ☐ Modem control
- ☐ Configurable as DTE or DCE
- ☐ Serial input and output as either RS-232 or 20mA current loop
- ☐ Current loop optically isolated
- ☐ Current loop selectable for either active or passive mode
- ☐ Address programmable
- ☐ Compatible with STD-Z80 Bus

MDX-SIO2
Figure 1



GENERAL DESCRIPTION

The Serial Input Output Module, MDX-SIO2, is designed to be a multiprotocol asynchronous or synchronous I/O module for the STD-Z80 Bus. The module is designed around the Mostek MK3887 Z80-SIO which provides two full duplex serial data channels. Each channel has an increase module flexibility. Both channels are capable of handling asynchronous, synchronous, and synchronous bit-oriented protocols such as BISYNC, SDLC, HDLC, and virtually any other serial protocol.

The MK3887 can generate and check CRC codes in any synchronous mode and can be programmed by the CPU for any traditional asynchronous format. The serial input and output is fully buffered and is provided at the connector as either 20mA current loop or RS-232-C levels. A modem control section is also provided for handshaking and status. The MDX-SIO2 module can be jumper-configured as a Data Terminal (DTE) or as a modem (DEC) in order to facilitate a variety of interface configurations.

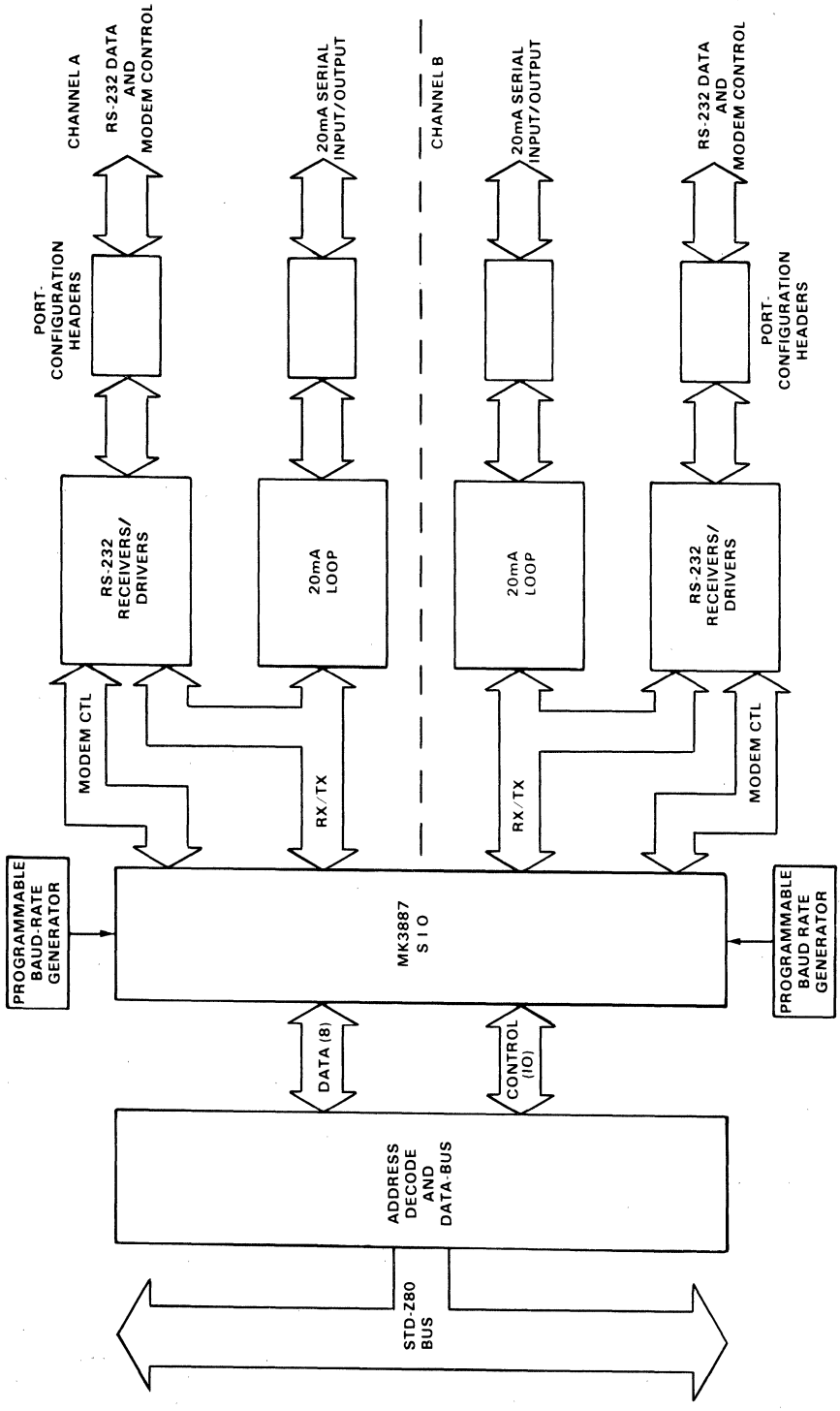
Figure 2 is a block diagram of the MDX-SIO2 module. It consists of five main elements. They are the channel-configuration headers, line drivers and receivers, MK3887 Z80-SIO, programmable Baud rate generator, and address-decode and data-bus buffers. Input and output to the board is provided via two 26-pin connectors. One connector is dedicated for each channel.

Several features are available as options that are selected via the channel-configuration headers. The headers are used to select the orientation of the data communication interface or the mode of the 20mA current loop. The MDX-SIO2 can be selected to act as either a terminal or processor (Data Terminal Equipment DTE) or as a modem (Data Communications Equipment DCE). The header allows

IVC

BLOCK DIAGRAM OF MDX-SIO2

Figure 2



J1 AND J2 CONNECTOR PINOUT

Table 1

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Protective Ground (AA)	13	TX+ (20mA Loop)
2	Transmitted Data (BA)	15	Transmission Signal Element Timing (DCE Source)
3	Received Data (BB)	17	Receive Signal Timing Element (DCE Source)
4	Request To Send (CA)	20	Data Terminal Ready (CD)
5	Clear To Send (CB)	22	Polarization Pin
6	Data Set Ready (CC)	24	RX+ (20mA Loop) or Transmission Signal Element Timing (DTE Source) (DA)
7	Signal GND (AB)		
8	Carrier Detect (CF)	25	TX- (20mA Loop)
12	RX-(20mA Loop)	26	Polarization Pin

configuration of both data interchange and modem control signals. This allows the increased flexibility necessary to link different hardware elements in OEM datalink systems and networks. The module is shipped from the factory wired as a DCE interface.

The MDX-SIO2 has different selectable options for the 20mA current loop. The receiver and transmitter input and output lines can be reconfigured on the modules to allow reorientation of these signals. Also, the receive and transmit circuits can be selected to function in either an active or passive mode. In the active mode, the MDX-SIO2 module provides the 20mA current source. In the passive mode, the module requires that the loop current be provided. The latter is the same mode as that of a teletype.

An EIA and 20mA current loop interface circuit is used to provide the necessary level shifting and signal conditioning between the MK3887 Z80-SIO and the connector. These line drivers and receivers provide the current electrical signal levels, slew rate, and impedance for interfacing RS-232-C and 20mA current loop peripherals. Additionally, optical isolation is provided for both transmit and receive circuits in the 20mA current loop mode.

The Mostek MK3887 Z80-SIO is the central element of this module. This device is a multifunction component designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic role is that of a serial-to-parallel, parallel-to-serial converter/controller. But within that role it is configured by software programming so that its function can be optimized for a given serial data communication application. The MK3887 provides two independent full-duplex channels, designated A and B. Each channel features the following:

Asynchronous operation
5, 6, 7, or 8 bits/character
1, 1½, or 2 stop bits
Even, odd, or no parity
X1, X16, X32, and X64 clock modes
Break generation and detection
Parity; Overrun and Framing-error detection

Binary Synchronous operation
Internal or external character synchronization
One or two Sync characters in separate registers
Automatic Sync character insertion
CRC generation and checking

HDLC or SDLC operation
Automatic Zero insertion and deletion
Automatic Flag
Address-field recognition
I-Field residue handling
Valid receive messages protected from overrun
CRC generation and checking

The MK3887 also provides modem control inputs and outputs as well as daisy-chain, priority-interrupt logic. Eight different interrupt vectors can be generated by the MK3887 in response to various conditions affecting the data communications channel transmission and reception. For more information concerning the MK3887, see the MK3887 Technical Manual in the 1982-1983 Microcomputer Components Designers' Guide.

Address decoding, STD-Z80 Bus interface, and bus management for the module is performed by the Address Decode and Data Bus circuit. The MDX-SIO2 contains command registers that are programmed to select the desired operational mode. The addressing scheme is as follows:

XXXXXX 00 Channel A Data
XXXXXX 01 Channel A Command/Status
XXXXXX 10 Channel B Data
XXXXXX 11 Channel B Command/Status

The XXXXXX indicates the binary code necessary to represent which of 64 starting port addresses is selected.

Each channel has an individual programmable Baud rate generator. The X1 multiplier on the MK3887 must be used in the synchronous modes. The X16, X32, or X64 MK3887 clock rate can be specified for asynchronous modes.

STRAPPING OPTIONS

Table 2 shows the strapping for different configurations of the RS-232 and 20mA loop interface. When the board is interfacing to a CRT or TTY, it should be strapped as DCE (Data Communications Equipment). The 20mA loop can be configured to sink or source current in addition to the ability to be DCE or DTE. Ports should not be strapped for both RS-232 and 20mA loop. Strapping both could result in circuit damage and erroneous data reception. The strapping is shown for port A; however, port B straps are identical except for the numbering of jumpers.

STRAPPING FOR J3 OR J4
Table 2

TYPE OF PORT	JUMPERS
RS-232 DCE (J3 and J4 as shipped)	1-2 13-20 15-22 11-18 17-12 21-14 19-16
RS-232 DTE	11-12 13-16 15-14 17-18 19-20 21-22
20mA Source-Loop DTE	23-24 25-26 27-28 29-30
20mA Source-Loop DCE	23-26 25-24 27-30 29-28
20mA Sink-Loop DTE	23-30 25-28 27-26 29-24
20mA Sink-Loop DCE	23-28 25-30 27-24 29-26

CLOCK CONFIGURATION STRAPPING

Each channel of the SIO chip used must be provided with clocking signals on particular input pins to determine the bit/Baud rate.

ASYNCHRONOUS CLOCKING

When a channel of the SIO is used for asynchronous communication, it is programmed for 16X clocking. Clocking is provided by the jumper-programmable Baud-Rate Generator. The rates for which the Baud-Rate Generator can be programmed (see Table 3) represent 16X multiples of commonly used communications Baud rates. For the Transmit side of an SIO channel, each serial bit is clocked out by every 16th transition on the clocking input. For the Receive, the clocking signal does not clock the data in itself, in the sense of being synchronized to it, but merely provides a framework in which transitions on the input data are considered. Thus, if an SIO channel is used for 16X asynchronous communications, and the Transmit and Receive Baud rates are the same (the typical case), there is no reason why the channel's Transmit and Receive clock input pins should not both be connected to the same output of the Baud-Rate Generator.

SYNCHRONOUS CLOCKING

EIA Standard RS-232-C defines the interface between a business machine (e.g. a computer), termed Data Terminal Equipment (DTE), and a piece of communications equipment (e.g. a modem), termed Data Communications Equipment (DCE). Within RS-232, the terms "Receive(d)" and "Transmit(ted)" are referenced to the DTE, so that the "Received Data" signal is provided by the DCE to the DTE, while the "Transmitted Data" signal is provided by the DTE to the DCE. In a synchronous environment, clocking information is in some way carried from one end of the link to the other. The "Receive Clock" signal (RS-232-C designation DD) is always provided by the DCE to the DTE, along with the data; each transition from RS-232 positive to negative voltage (SIO TTL ground to positive) serves to clock the Received Data signal into the DTE. Transmit clocking can be provided from either DCE to DTE, or vice versa. Separate connector pins/signals are provided depending on the direction: RS-232 designation DB is used for a Transmit Clock provided by the DCE to the DTE, whereas designation DA is used for a DTE-sourced Transmit Clock. Whichever the source, the negative-to-positive transition on the RS-232 signal is used by the DTE to change the data; the opposite transition is used by the DCE to sample it.

As noted previously, the MDX-SIO2 board can act as DTE or DCE; in each case it can also source or receive the Transmit Clock signal. For synchronous communication, the SIO chip always operates at a 1X clock rate, acting on transitions in the clocking signal(s) as described above.

When the MDX-SIO2 card sources an RS-232-C clock, it is from one of the outputs of the Baud-Rate Generator. The

BAUD RATE (Hz) PROGRAMMABILITY

Table 3

FREQUENCY CODE				SYNCHRONOUS	ASYNCHRONOUS		
D	C	B	A	X1	X16	X32	X64
0	0	0	0	800	50	25	12.5
0	0	0	1	1200	75	37.5	18.75
0	0	1	0	1760	110	55	27.50
0	0	1	1	2152	134.5	67.25	33.63
0	1	0	0	2400	150	75	37.50
0	1	0	1	4800	300	150	75
0	1	1	0	9600	600	300	150
0	1	1	1	19200	1200	600	300
1	0	0	0	28800	1800	900	450
1	0	0	1	32000	2000	1000	500
1	0	1	0	38400	2400	1200	600
1	0	1	1	57600	3600	1800	900
1	1	0	0	76800	4800	2400	1200
1	1	0	1	115200	7200	3600	1800
1	1	1	0	153600	9600	4800	2400
1	1	1	1	307200	19200	9600	4800

NOTE:
Current loop applications above 9600 Baud are not recommended
Strap = 0
No Strap = 1

transfer rates provided are commonly used for synchronous communication (1200, 2400, 4800, 9600, 19200). These rates are selectable from the X1 column of Table 3.

JUMPERS FOR BAUD-RATE GENERATOR FREQUENCIES

The clock frequencies for f_T and f_R are selected with straps on J8 as follows:

Pins	Channel A	Pins	Channel B
7-8	LSB - A f_R	15-16	LSB - A f_T
5-6	B f_R	13-14	B f_T
3-4	C f_R	11-12	C f_T
1-2	MSB - D f_R	9-10	MSB - D f_T

For frequencies selected refer to Table 3.

JUMPERS FOR CONNECTION OF BAUD-RATE-GENERATOR OUTPUTS TO SIO INPUTS

The clock configuration straps are defined as follows:

PINS
1-2 Connects f_r to TRANSMIT CLOCK PORT A
3-4 Connects f_r to RECEIVE CLOCK PORT A
5-6 Connects f_t to TRANSMIT CLOCK PORT B
7-8 Connects f_t to RECEIVE CLOCK PORT B
2-5 Connects f_r to TRANSMIT CLOCK PORT B
4-7 Connects f_r to RECEIVE CLOCK PORT B
1-6 Connects f_t to TRANSMIT CLOCK PORT A
3-6 Connects f_t to RECEIVE CLOCK PORT A

These straps are found on J7. Figures 3 thru 9 illustrate the use of these jumpers. Figure 10 is a worksheet useable during board configuration.

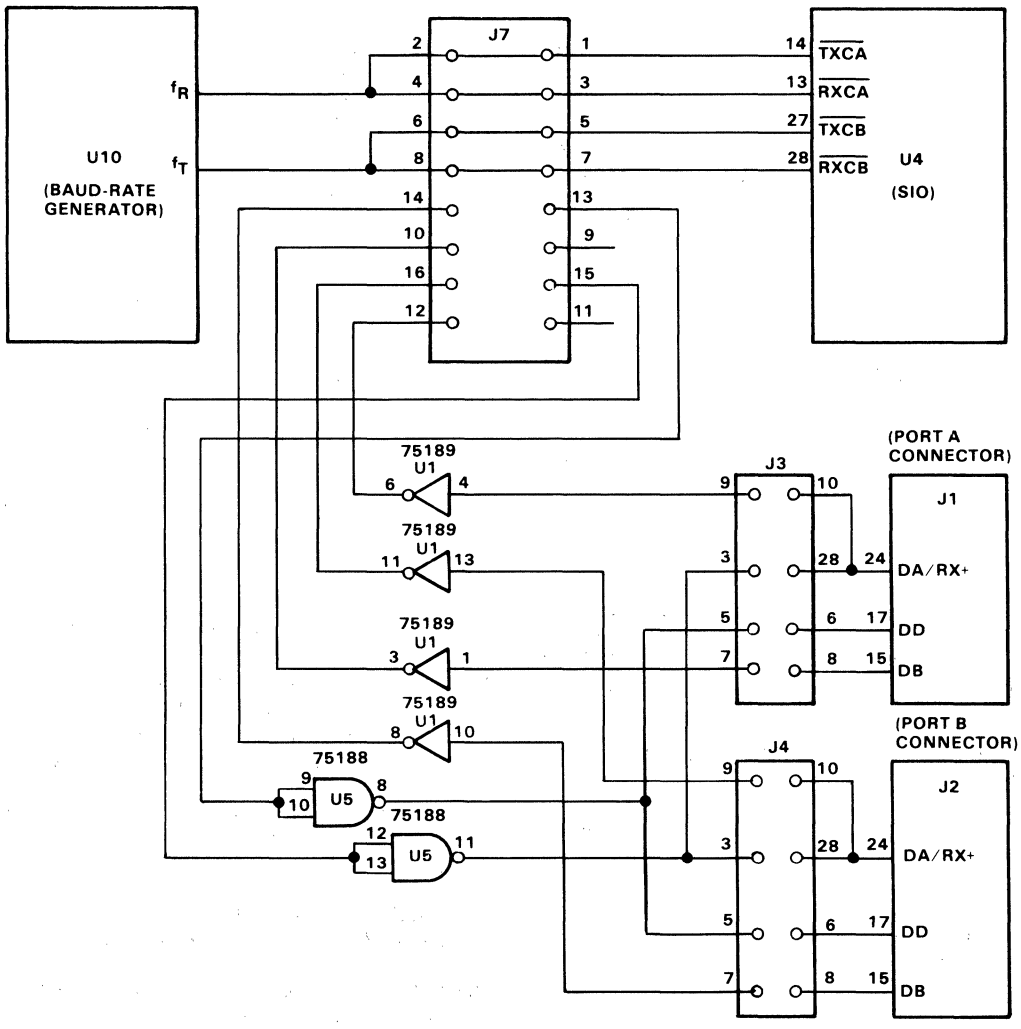
CONNECTION OF RS-232 SYNCHRONOUS CLOCK SIGNALS DA, DB, DD TO SIO INPUTS

The RS-232 DTE-supplied Transmit Clock signal DA shares the connector pin assignment of current loop signal RX+ (Port A = J1 pin 24 to J3 pins 28, 10; Port B = J2-24 to J4-28, 10). The DCE-supplied Transmit Clock signal DB is brought out from J1-15 to J3-8 (Port A) and J2-15 to J4-8 (Port B), and the (always DCE-supplied) Receive Clock DD from J1-17 to J3-6 (Port A) and J2-17 to J4-6 (Port B).

Connections for synchronous clocking are made from pins of J7 (which connect to the SIO clock inputs) to one side of an EIA driver or receiver. The other side of the driver or receiver is then connected to one of the clocks DA, DB, or DD. Various cases of such connections are presented in the following examples.

BOTH PORTS ASYNCHRONOUS

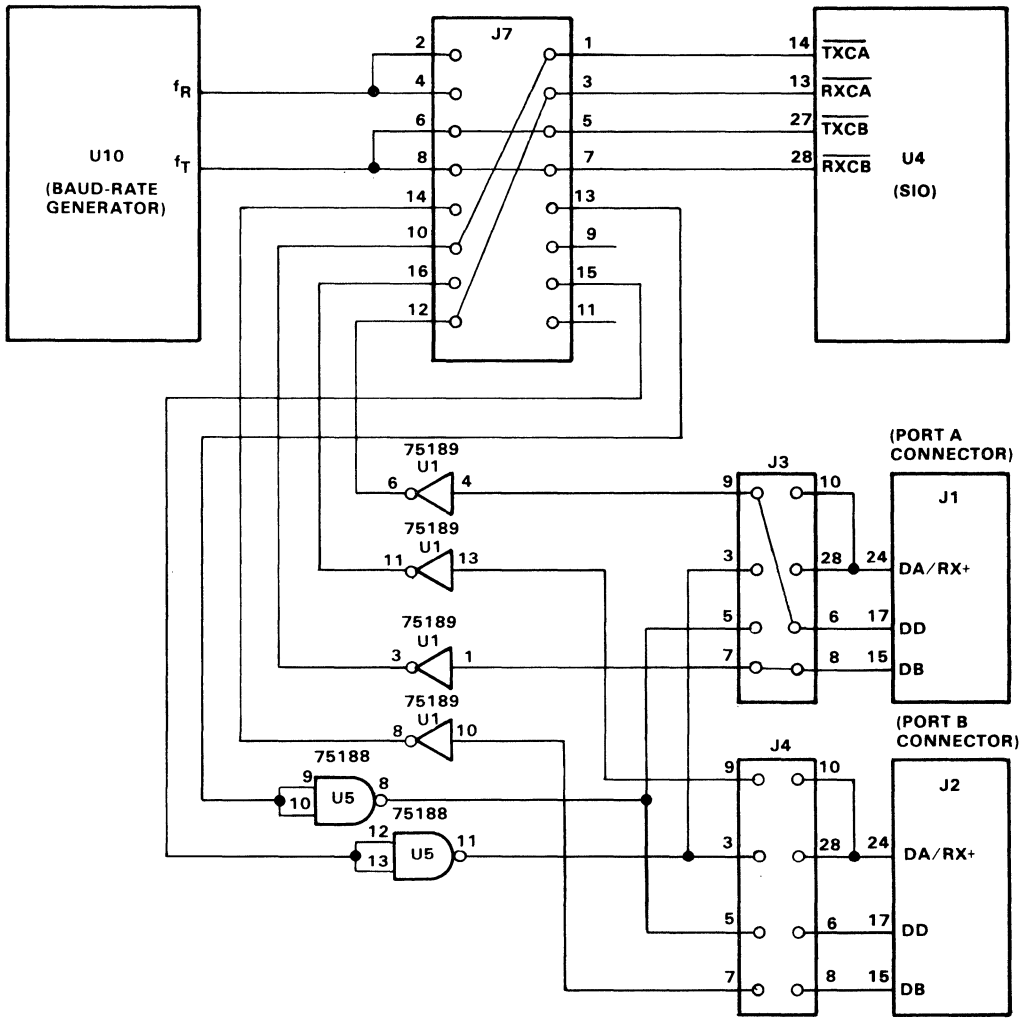
Figure 3



PORT A	PORT B
Asynchronous DTE or DCE RCV&XMIT@ Rate f_R	Asynchronous DTE or DCE RCV&XMIT @ Rate f_T

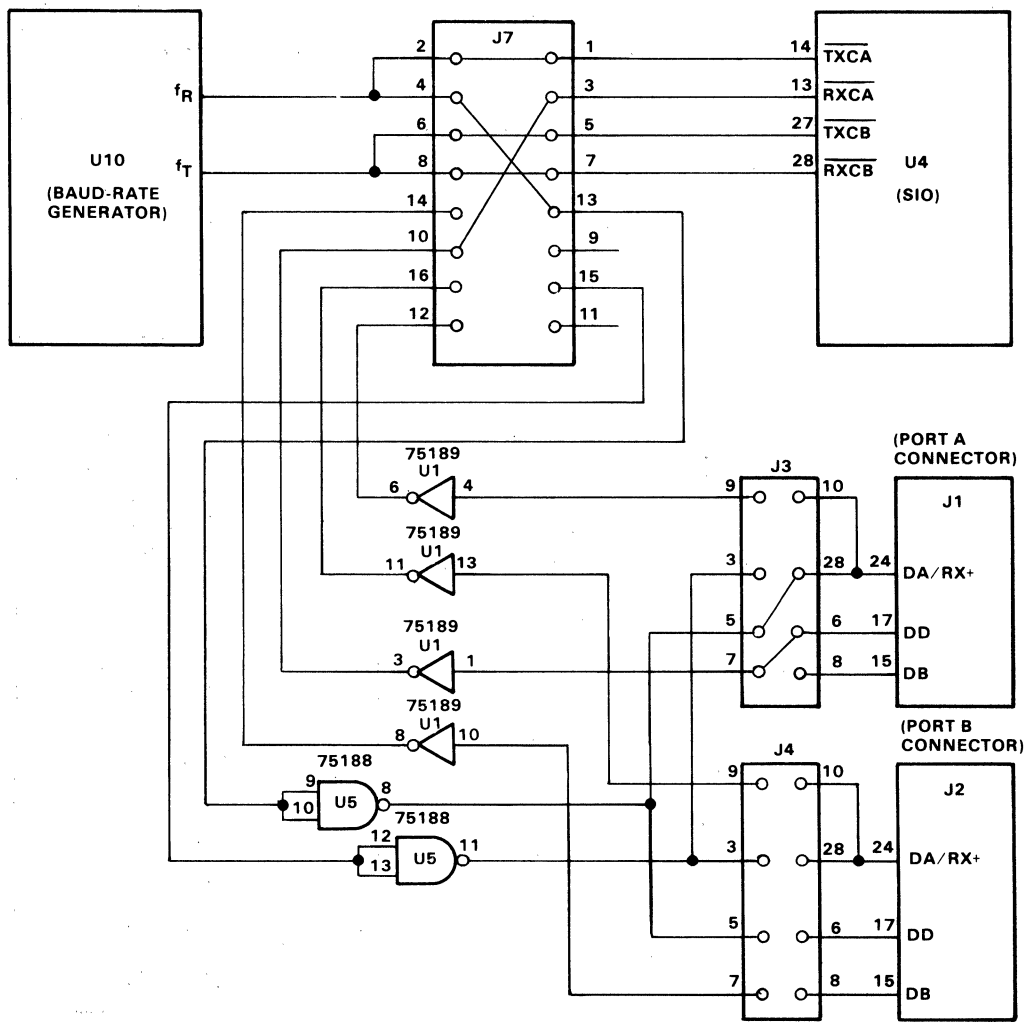
NOTE:
This configuration is suitable for J1-to-J2 loopback testing if $f_T = f_R$.

PORT A: SYNCHRONOUS, DTE, XMIT CLOCK FROM DCE
PORT B: ASYNCHRONOUS
Figure 4



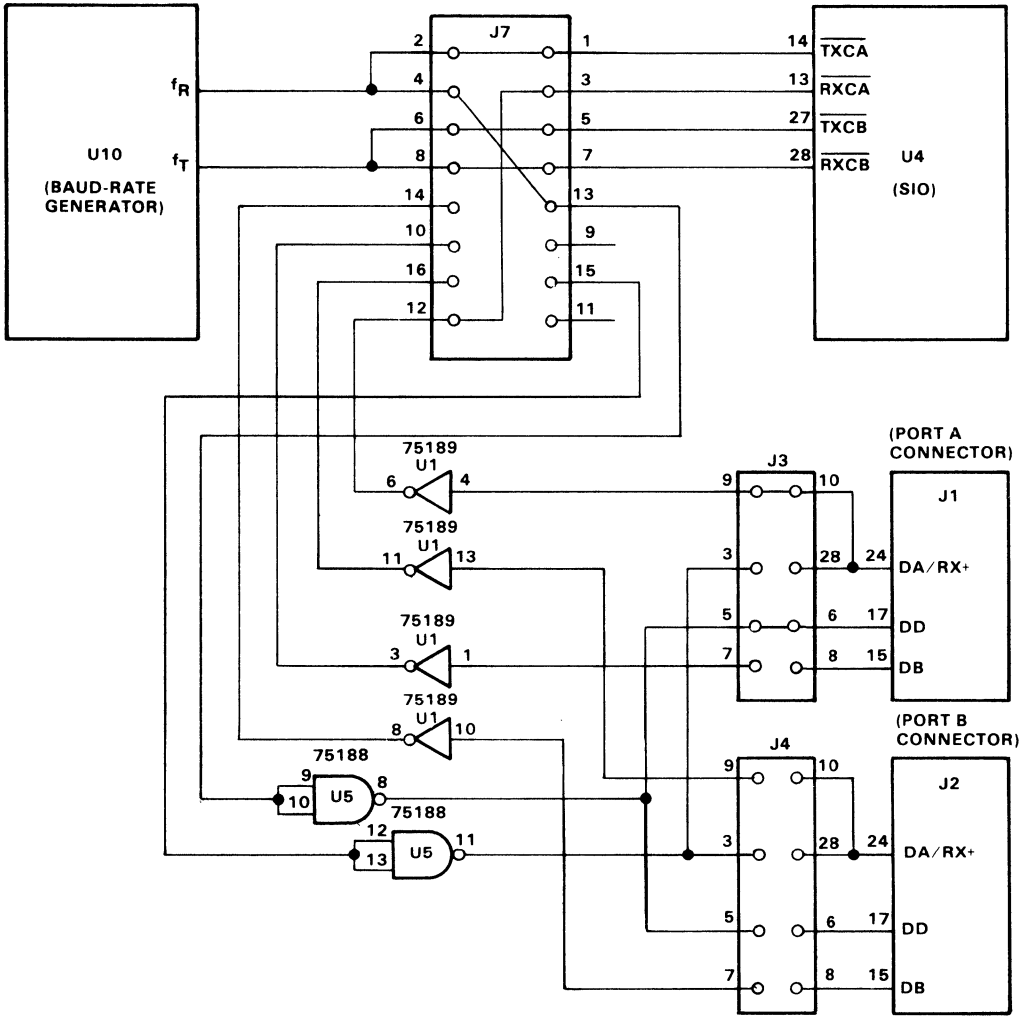
PORT A	PORT B
Synchronous DTE DCE Supplies XMIT Clock RCV & XMIT Rate External, Independent	Asynchronous DCE or DTE RCV & XMIT @ Rate f_T

PORT A: SYNCHRONOUS, DTE, XMIT CLOCK PROVIDED TO DCE
PORT B: ASYNCHRONOUS
Figure 5



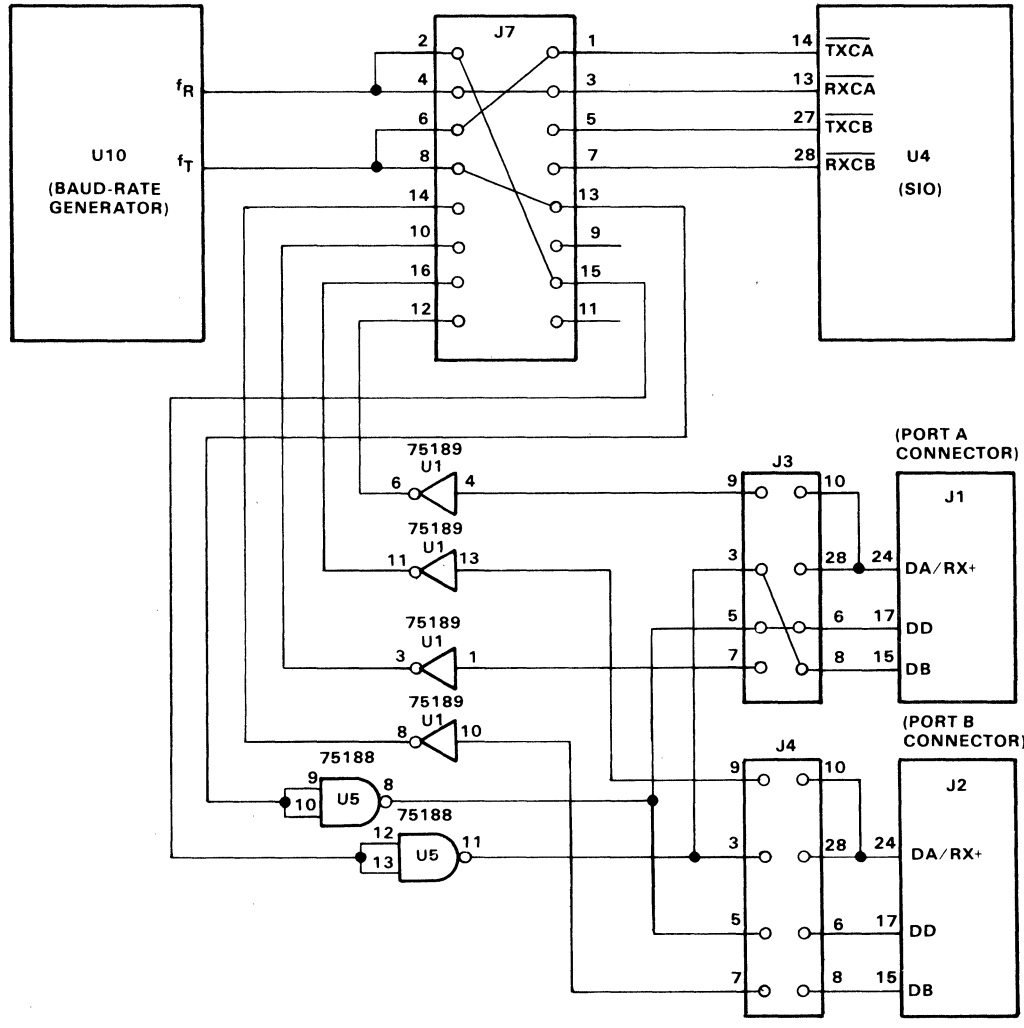
PORT A	PORT B
Synchronous DTE XMIT CLOCK SUPPLIED TO DCE XMIT Rate @ f_R RCV Rate External	Asynchronous DTE or DCE RCV&XMIT @ Rate f_T

PORT A: SYNCHRONOUS, DCE, XMIT CLOCK FROM DTE
PORT B: ASYNCHRONOUS
Figure 6



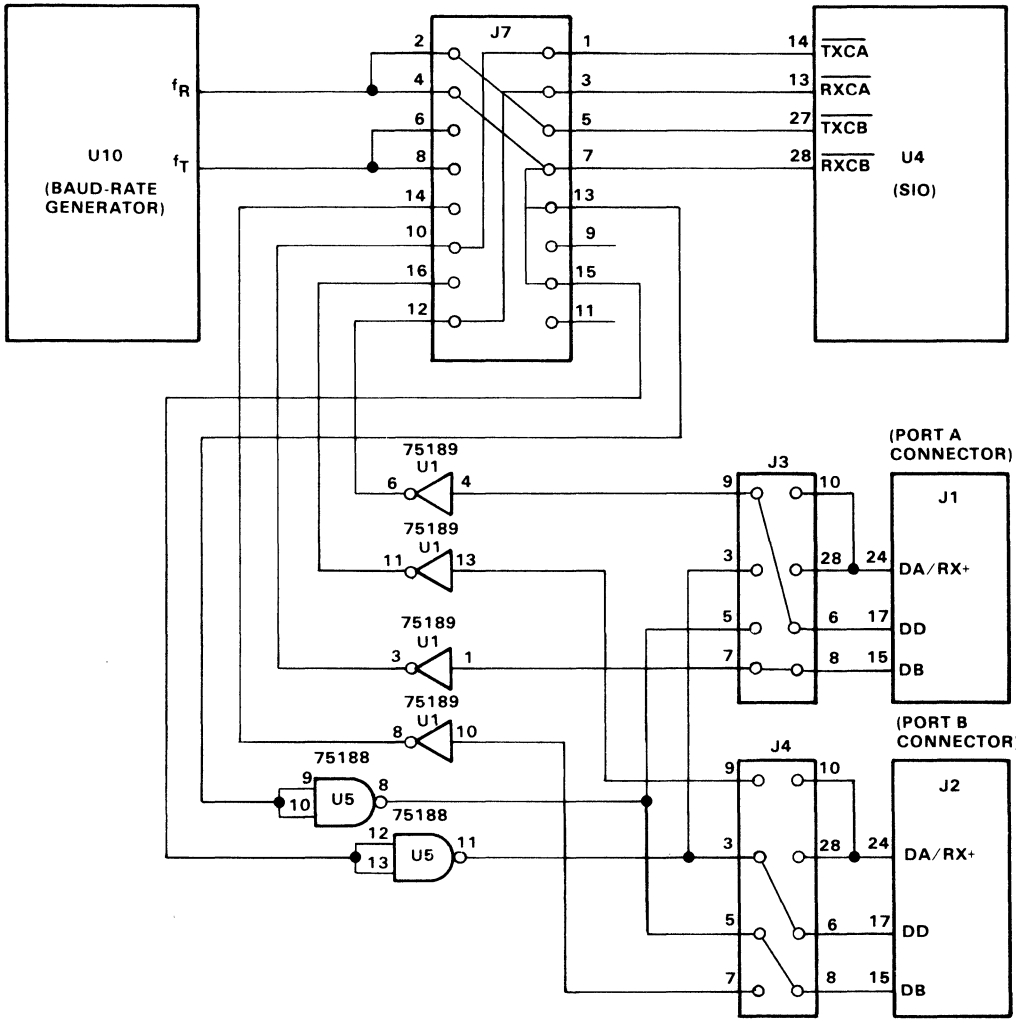
PORT A	PORT B
SYNCHRONOUS DCE DTE SUPPLIES XMIT CLOCK XMIT RATE (RCV CLOCK SIG) @ f_R RCV RATE (XMIT CLK SIG) EXT	ASYNCHRONOUS DTE OR DCE RCV & XMIT @ RATE f_T

PORT A: SYNCHRONOUS, DCE, XMIT CLOCK PROVIDED TO DTE
PORT B: UNUSED
Figure 7



PORT A	PORT B
SYNCHRONOUS DCE XMIT CLOCK SUPPLIED TO DTE RCV CLOCK SUPPLIED TO DTE XMIT RATE (RCV CLOCK SIG) @ f_T RCV RATE (XMIT CLOCK SIG) @ f_R	UNUSED

PORT A: SYNCHRONOUS, DTE, XMIT CLOCK PROVIDED FROM DCE
PORT B: SYNCHRONOUS, DCE, XMIT CLOCK PROVIDED TO DTE
Figure 8

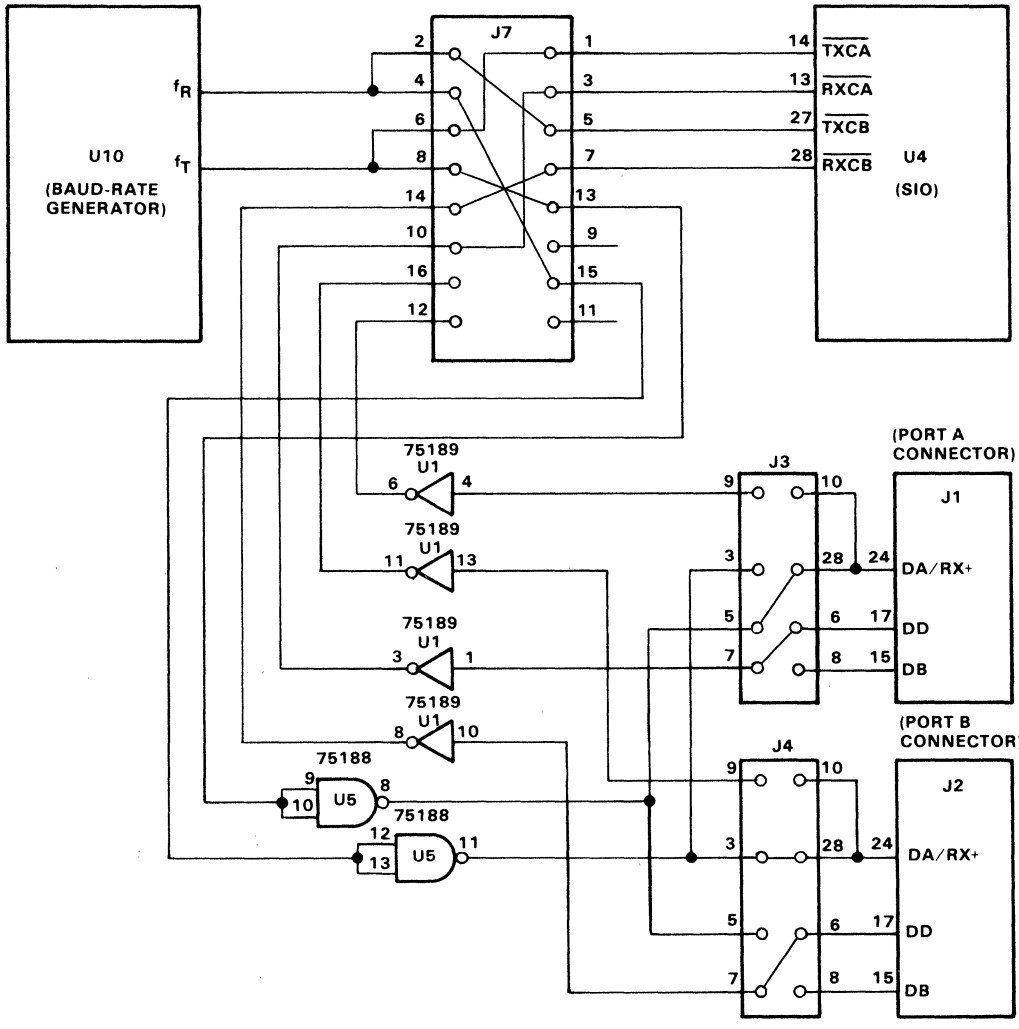


PORT A	PORT B
SYNCHRONOUS DTE XMIT CLOCK SUPPLIED FROM DCE XMIT & RCV RATE EXTERNAL, INDEPENDENT	SYNCHRONOUS DCE XMIT CLOCK SUPPLIED TO DTE RCV CLOCK SUPPLIED TO DTE XMIT RCV@ Rate f_R

NOTE:
This configuration is suitable for J1-J2 loopback testing if $f_R = f_T$.

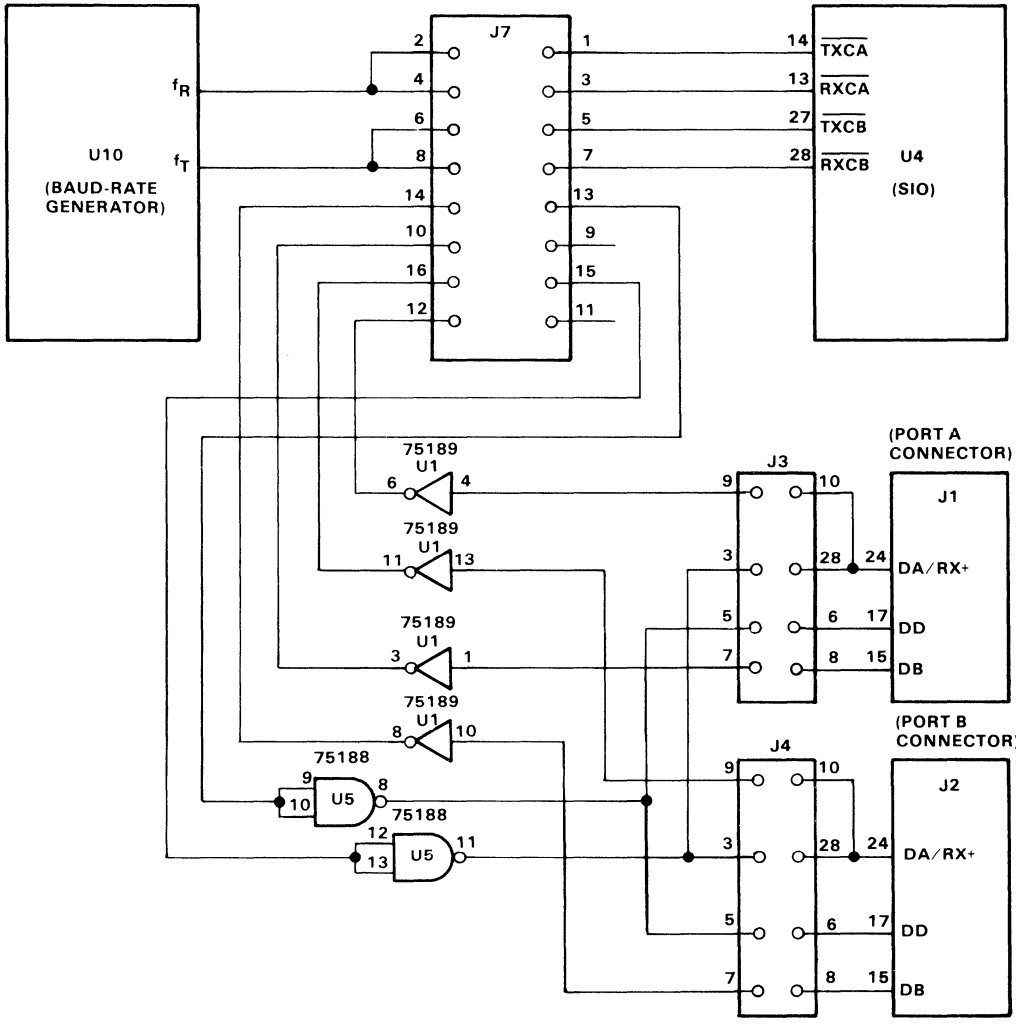
BOTH PORTS SYNCHRONOUS, DTE, XMIT CLOCK PROVIDED TO DCE

Figure 9



PORT A	PORT B
SYNCHRONOUS DTE XMIT CLOCK SUPPLIED TO DCE XMIT @ RATE f_T RCV RATE EXTERNAL	SYNCHRONOUS DTE XMIT CLOCK SUPPLIED TO DCE XMIT @ RATE f_R RCV RATE EXTERNAL

CLOCK-CONFIGURATION WORKSHEET
Figure 10



PORT A	PORT B

ADDRESS-CONFIGURATION STRAPPING

Address selection is done by wiring the proper straps on Header J9. Installing a strap causes the respective Address Bit to be compared for a zero. Address select straps are defined as follows:

Pins	
3-4	ADDRESS BIT 2
1-2	ADDRESS BIT 3
7-8	ADDRESS BIT 4
5-6	ADDRESS BIT 5
9-10	ADDRESS BIT 6
11-12	ADDRESS BIT 7

Address Bits 0 and 1 are predefined for the MDX-SIO2 board as follows:

A_1	A_0	
0	0	PORT A DATA
0	1	PORT A CONTROL/STATUS
1	0	PORT B DATA
1	1	PORT B CONTROL/STATUS

The Shipping Configuration for J9 is no jumpers installed.

INTERRUPT DESCRIPTION

The purpose of an interrupt is to allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start a peripheral service routine. Usually this service routine is involved with the exchange of data, or status and control information, between the CPU and the peripheral. Once the service routine is completed, the CPU returns to the operation from which it was interrupted. The block diagram of the interrupt circuitry of the MDX-SIO2 is shown in Figure 11.

Mode 2 interrupts are supported by the MDX-SIO2. This mode is the most powerful interrupt response mode. With a single 8-bit byte from the interrupting device, an indirect call can be made to any memory location.

With this mode, the programmer maintains a table of 16-bit starting addresses for every interrupt service routine. This table may be located anywhere in memory. When an interrupt is accepted, a 16-bit pointer must be formed to obtain the desired interrupt service routine starting address from the table. The upper eight bits of this pointer are formed from the contents of the I register. The lower eight bits of the pointer must be supplied by the interrupting device.

INTERRUPT SERVICING

At some predetermined condition, such as data being strobed into a SIO port, the SIO chip will generate a condition for interrupting the CPU. During this time, the common interrupt line ($\overline{INTRQ}$) will be pulled active low by the SIO requesting the interrupt.

Sometime later, the CPU will send out an interrupt acknowledge (INTAK). During INTAK, the interrupt logic of the various peripheral chips in the system will determine the highest-priority port which is requesting an interrupt. This device then places the contents of its 8-bit interrupt vector on the data bus for the CPU. The interrupt condition is maintained until the end of the INTAK cycle. Lower priority interrupts are inhibited until this device decodes an RETI instruction or an equivalent command.

If more than one peripheral chip requests interrupt servicing at the same time, a priority status is established. Priority is determined by the interrupt enable lines - IEI and IEO - and internal logic on each peripheral chip. The following table defines interrupt priority status:

IEI	IEO	STATUS
0	0	higher priority device requesting interrupt
0	1	undefined (not allowed)
1	0	requesting interrupt (no higher priority interrupt)
1	1	no interrupt

DAISY CHAIN

All Z-80 devices include daisy-chain priority-interrupt logic that automatically supplies the programmed vector (from the highest-priority interrupting peripheral) to the CPU during interrupt acknowledge. To ensure that more than the on-board SIO chip can be included in the interrupt priority loop, "look-ahead" logic has been implemented on the board. Both ends of the board daisy chain logic have been brought to edge connector P1 so that the board priority within a larger daisy chain system can be established. Board priority is determined in the same fashion as an individual peripheral chip i.e., through the high or low state of PCI or PCO.

ELECTRICAL SPECIFICATIONS

Word Size
Data: 8-bits
I/O Addressing: 8-bits

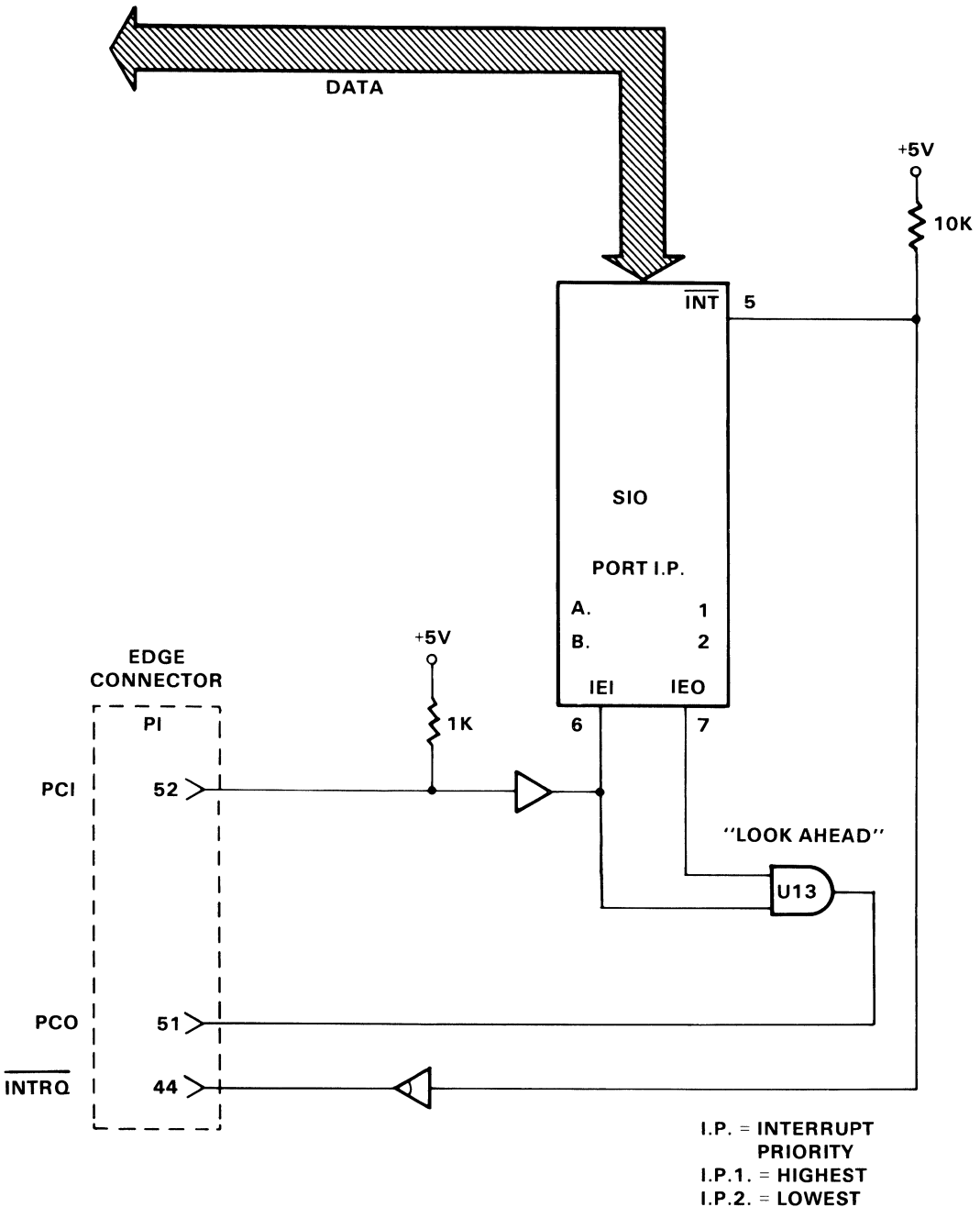
I/O Addressing

On-board fully-programmable

I/O Capacity

Serial - Two full-duplex serial ports, either synchronous or asynchronous. Special control register and circuitry to permit programmed implementation of SDLC, BiSync, Monosync, HDLC, and other formats.

PRIORITY INTERRUPT STRUCTURE
Figure 11



IVC

Serial Communication Interface

Two identical ports

SIGNAL	20mA LOOP	BUFFERED FOR 20mA LOOP	RS-232-C	RS-232-C
	DTE	DCE	DTE	DCE
Transmitted data	Output	Input	Output	Input
Received data	Input	Output	Input	Output
Data Terminal Ready (DTR)			Output	Input
Request to Send (RTS)			Output	Input
Clear to Send (CTS)			Input	Output
Carrier Detect (CDET)			Input	Output

Interrupts

Generates vectored interrupts to 8 different locations corresponding to conditions within both channels. Interrupt-vector location programmable. Daisy-chained-priority hardware interrupt circuitry.

System Interrupt Units

1

System Clock

	MIN	MAX
MDX-SIO2	250kHz	2.5 MHz
MDX-SIO2-4	250kHz	4.0 MHz

Parallel Bus Interface - STD-Z80 Bus Compatible

Inputs One 74LS load Max.

Bus Outputs I_{OH} = -3mA min. at 2.4 Volts
I_{OH} = 24mA min. at 0.5 Volts

Power Supply Requirements

+12 Volts ± 5% at 72 mA max.
-12 Volts ± 5% at 46 mA max.
+5 Volts ± 5% at 650 mA max.

Operating Temperature

0°C to 60°C

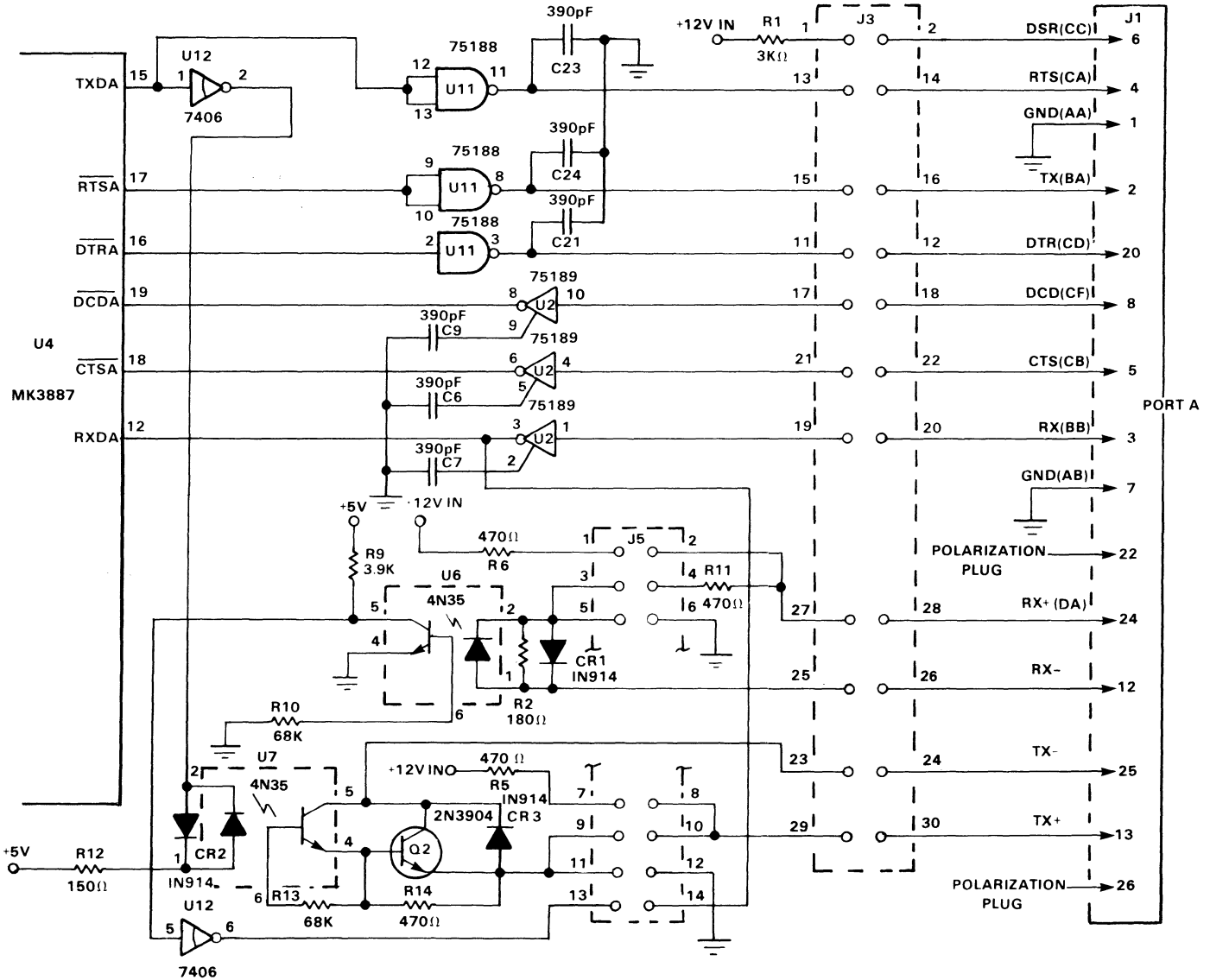
MECHANICAL SPECIFICATIONS

Card Dimensions

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
0.675 in. (1.71 cm) maximum profile thickness
0.062 in. (.016 cm) printed circuit board thickness

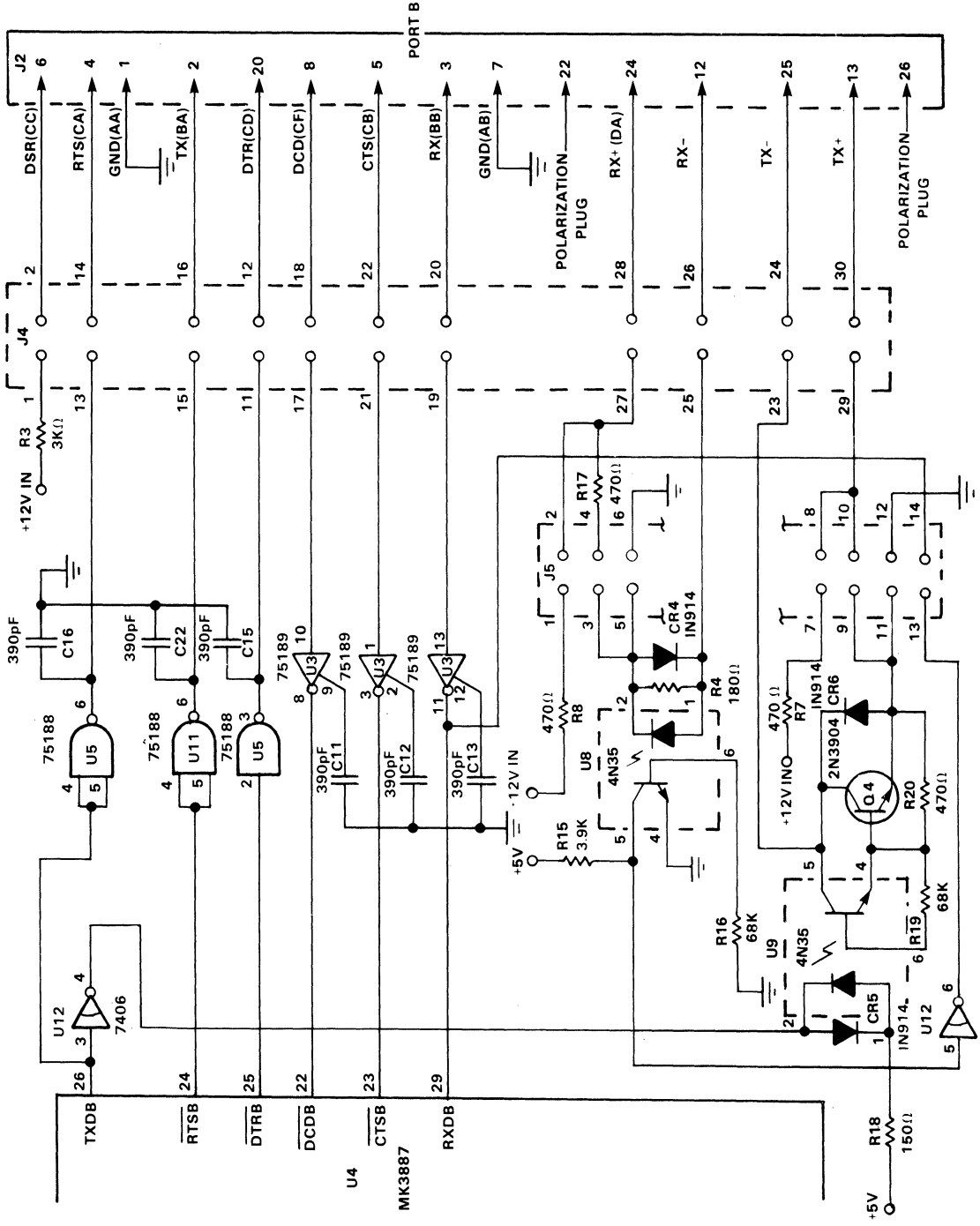
Connectors

FUNCTION	CONFIGURATION	MATING CONNECTOR (NOT SHIPPED)
STD-Z80 BUS	56-pin dual readout 0.125-in. centers	PC BOARD Viking 3VH28/1CE5 Wire Wrap Viking 3VH28/1CND5 Solder Lug Viking 3VH28/1CN5
SERIAL I/O	26-pin dual readout 0.100-in. grid	Flat Ribbon Ansley 609-2600M Discrete Wires WINCHESTER PGB26A (housing) WINCHESTER 100-70020S (contacts)



PORT A STRAP-OPTION WORK SHEET
Figure 12

PORT B STRAP-OPTION WORK SHEET
Figure 13



ORDERING INFORMATION

Designator	Description	Part Number
MDX-SIO2	MDX-SIO2 Serial Input/Output Module with Technical Manual	MK77670-0 (2.5 MHz.) MK77670-4 (4 MHz.)
MDX-SIO2 Technical Manual	MDX-SIO2 Technical Manual Only	4420129

MDX-422I
MK77671

FEATURES

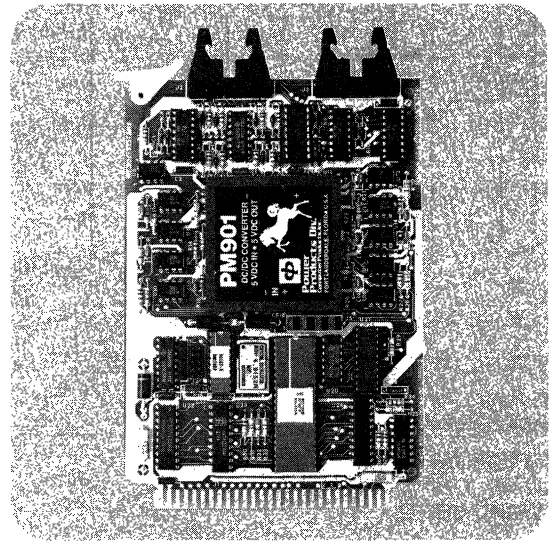
- ☐ STD-Z80 BUS compatible
- ☐ Two independent asynchronous/synchronous serial channels
- ☐ Independent software programmable baud rate clocks
- ☐ Asynchronous rates of 50 to 19.2K baud
- ☐ Synchronous rates of 800 to 307.2K baud
- ☐ Asynchronous half-duplex communications between serial control units and MDX-422's in any mix
- ☐ BiSync, HDLC or SDLC operation
- ☐ Both CRC-16 and CRC-CCITT error detection are hardware implemented
- ☐ Receive data registers are quadruply buffered
- ☐ Transmitter data registers are double buffered
- ☐ RS-422 compatible input and output
- ☐ Up to 4000' data communication over RS-422 twisted pair
- ☐ Common mode ground fault protection 400 Volts
- ☐ Port block selectable
- ☐ 2.5 and 4 MHz capability
- ☐ 400 Volt optically isolated

DESCRIPTION

The MDX-422I is a dual-channel, serial RS-422 interface for use with STD-Z80 microcomputer systems. The module incorporates RS-422 (balanced, differential) serial communication, allowing long-distance communication (4000 ft.) in noisy industrial environments between MDX-422I's and/or SCU's (Serial Control Units). Each MDX-422I channel is capable of driving forty devices in a party-line configuration. The module is designed around the Mostek

BOARD PHOTO

Figure 1



MK3887 Z80-SIO which provides both full- and half-duplex operation. Each channel has an independent programmable baud rate clock generator to increase module flexibility.

Figure 2 is a block diagram of the MDX-422I module. The figure consists of six main elements: address decode and data bus buffers, MK3887 Z80-SIO, isolated supply voltage, line drivers and receivers, programmable baud rate generator and channel configuration headers. Input and output to the board is provided via two 10-pin connectors. One connector is dedicated for each channel. Figure 1 shows the board with overlay.

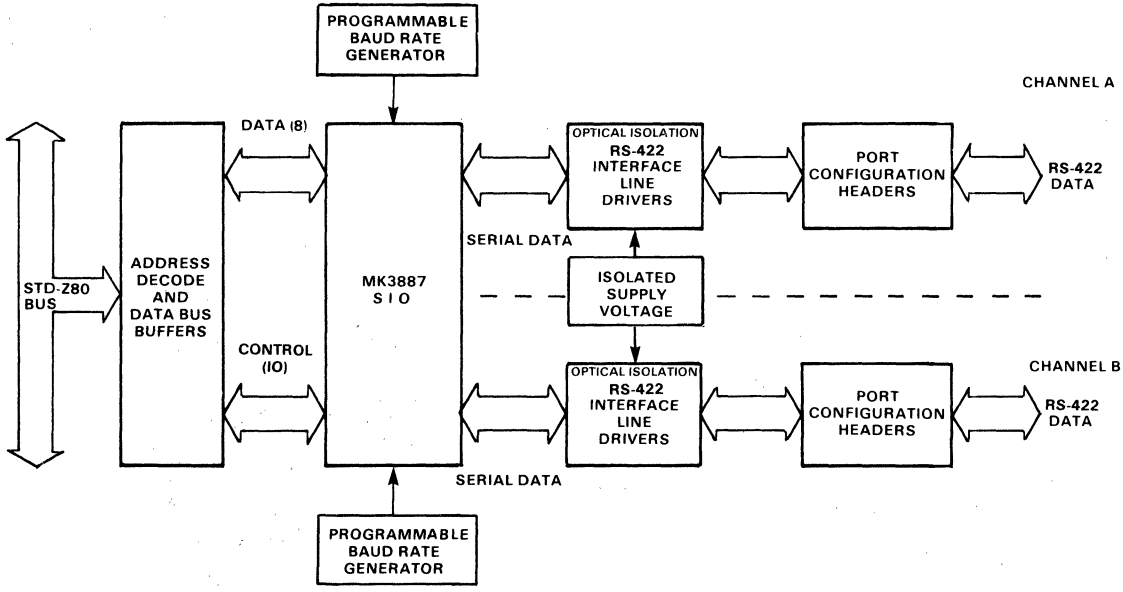
The RS-422 interface on the MDX-422I module is fully isolated up to 400 volts above and below ground. This is implemented to ensure protection from common mode ground potentials associated with long-distance communications. The transmitter/receiver section also has protection against transients of up to 150 watts peak pulse power for 1 ms. These transients are commonly induced on the transmission lines in noisy industrial environments.

IVC

™ MD Series is a trademark of Mostek Corporation

BLOCK DIAGRAM

Figure 2



SPECIFICATIONS

WORD SIZE

Data:	8 bits
I/O Addressing:	8 bits

I/O CAPACITY

Serial: Two full- or half-duplex serial ports both capable of either synchronous or asynchronous operation. Special control registers and circuitry to permit implementation of SDLC, BiSync, Monosync, HDLC and other formats which can be programmed.

I/O ADDRESSING

The high-order 5 bits of the I/O address are user-programmable through the use of selecting straps. The low-order three bits are decoded on-board, thus indicating the need for eight consecutive port addresses. These ports are assigned as follows:

A2	A1	A0	
0	0	0	Port A data
0	0	1	Port A control/status
0	1	0	Port B data
0	1	1	Port B control/status
*1	0	0	Baud rate generator
*1	0	1	Baud rate generator
*1	1	0	Baud rate generator
*1	1	1	Baud rate generator

*The baud rate generator is decoded from A2, therefore it may be programmed with any of the four available addresses. The high order 4 bits program channel A while the low order 4 bits program channel B.

INTERRUPTS

Generates vectored interrupts to 8 different locations corresponding to conditions within both channels. Interrupt vector locations are programmable. Daisy-chained interrupt priority.

SYSTEM INTERRUPT UNITS (SIUs) = 1

CLOCK

	Min.	Max.
MDX-422I	250 kHz	4.0 MHz

STD-Z80 BUS INTERFACE

Inputs:	One 74LS Load Max.
Outputs:	IOL=24mA Min. @ VOL = 0.5Volts
	IOH = -3mA Min. @ VOH = 2.4Volts

OPERATING TEMPERATURE

0 to 60 degrees C

POWER SUPPLY REQUIREMENTS

+5 Volts ± 5% at 2.0A max.
+12 Volts ± 5% at 25mA max.

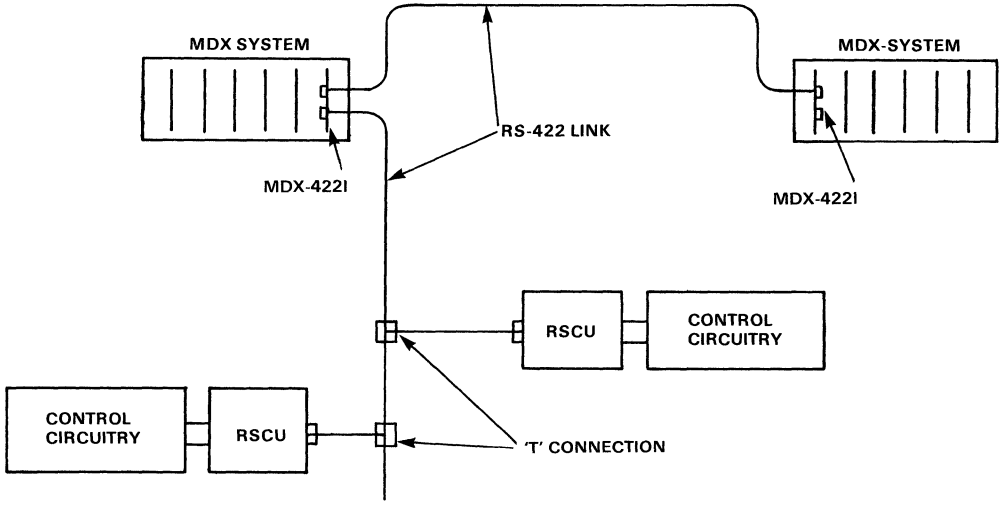
DIMENSIONS

4.5 inches (114.3 mm) high by 6.5 inches (165.1 mm) long
0.675 inches (17.1 mm) maximum profile thickness
0.062 inches (1.6 mm) printed-circuit-board thickness

CONNECTORS

FUNCTION	DESCRIPTION	MATING CONNECTOR
STD-Z80 BUS	56-pin, dual	Viking 3VH28/ 1CE5 (printed circuit) Viking 3VH28/ 1CND5 (wire-wrap) Viking 3VH28/ 1CN5 (solder lug)
RS-422	Socket conn. 10-pin	Winchester 51-1110-01

TYPICAL APPLICATION:



IVC

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-422I	RS-422 interface module with operations manual	MK77671
	Operations manual for the above	4420071
	Z80-SIO Technical Manual	MK78583

MDX-422N
MK77676

FEATURES

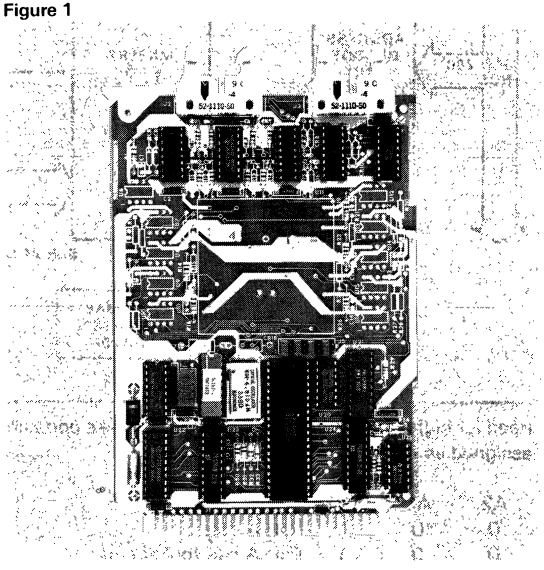
- ☐ Two independent asynchronous/synchronous serial channels
- ☐ Independent software programmable baud rate clocks
- ☐ Asynchronous rates of 50 to 19.2K baud
- ☐ Synchronous rates of 800 to 307.2K baud
- ☐ Asynchronous half-duplex communications between serial control units and MDX-422's in any mix
- ☐ BiSync, HDLC or SDLC operation
- ☐ Both CRC-16 and CRC-CCITT error detection are hardware implemented
- ☐ Receive data registers are quadruply buffered
- ☐ Transmitter data registers are double buffered
- ☐ RS-422 compatible input and output
- ☐ Port block selectable
- ☐ STD-Z80 BUS compatible
- ☐ 2.5 and 4 MHz capability

DESCRIPTION

The MDX-422N is a dual-channel, serial RS-422 interface for use with MDX microcomputer systems. The module incorporates RS-422 (balanced, differential) serial communication, allowing long-distance communication in noisy industrial environments between MDX-422's and MDX-422N's and/or RSCU's (Serial Control Units). Each MDX-422N channel is capable of driving forty devices in a party-line configuration. The module is designed around the Mostek MK3887 Z80-SIO which provides both full- and half-duplex operation. Each channel has an independent programmable baud rate clock generator to increase module flexibility.

Figure 2 is a block diagram of the MDX-422N module. The device consists of five main elements: address decode and data bus buffers, MK3887 Z80-SIO, line drivers and receivers, programmable baud rate generator, and channel configuration headers. Input and output to the board is provided via two 10-pin connectors. One connector is dedicated for each channel.

MDX-422N
Figure 1



IVC

SPECIFICATIONS

WORD SIZE

Data:	8 bits
I/O Addressing:	8 bits

I/O CAPACITY

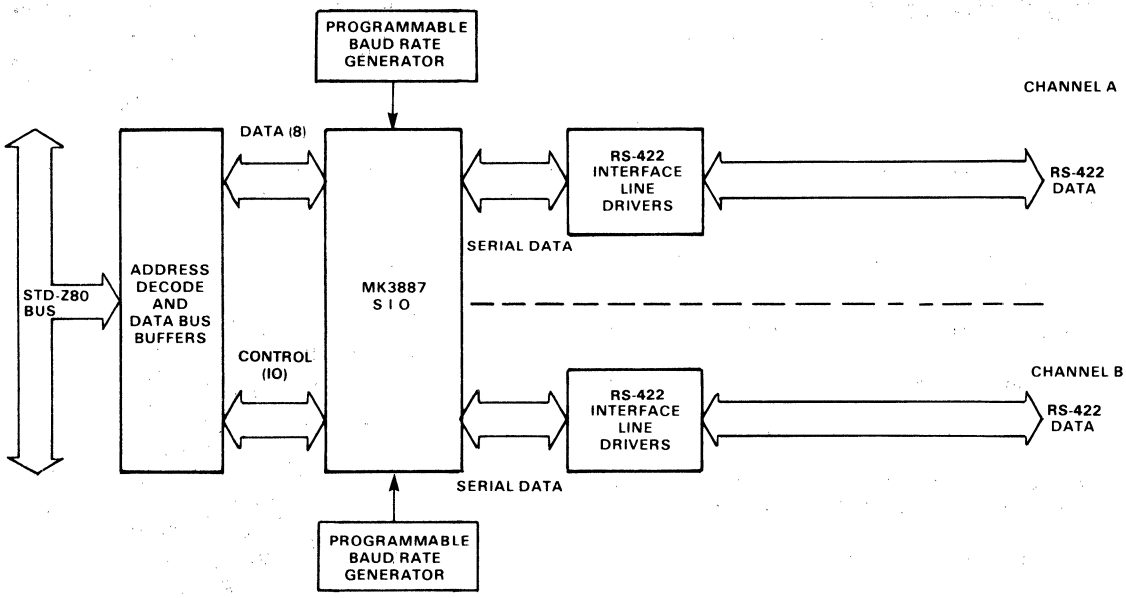
Serial: Two full- or half-duplex serial ports both capable of either synchronous or asynchronous operation. Special control registers and circuitry to permit implementation of SDLC, BiSync, Monosync, HDLC and other formats which can be programmed.

I/O ADDRESSING

The high-order 5-bits of the I/O address are user-programmable through the use of selecting straps. The low-order 3-bits are decoded on-board, thus indicating the

BLOCK DIAGRAM

Figure 2



need for eight consecutive port addresses. These ports are assigned as follows:

A2	A1	A0	
0	0	0	Port A data
0	0	1	Port A control/status
0	1	0	Port B data
0	1	1	Port B control/status
*1	0	0	Baud rate generator
*1	0	1	Baud rate generator
*1	1	0	Baud rate generator
*1	1	1	Baud rate generator

*The baud rate generator is decoded from A2, therefore it may be programmed with any of the four available addresses. The high-order 4-bits program channel A while the low-order 4-bits program channel B.

INTERRUPTS

Generates vectored interrupts to eight different locations corresponding to conditions within both channels. Interrupt vector location programmable. Daisy-chained interrupt priority.

SYSTEM INTERRUPT UNITS (SIUs) = 1

CLOCK

	Max.
MDX-422N	4.0 MHz

STD-Z80 BUS INTERFACE

Inputs: One 74LS Load Max.
Outputs: IOL= 24mA Min. @ VOL = 0.5 Volts
IOH = -3mA Min. @ VOH = 2.4 Volts

OPERATING TEMPERATURE

0 to 60 degrees C

POWER SUPPLY REQUIREMENTS

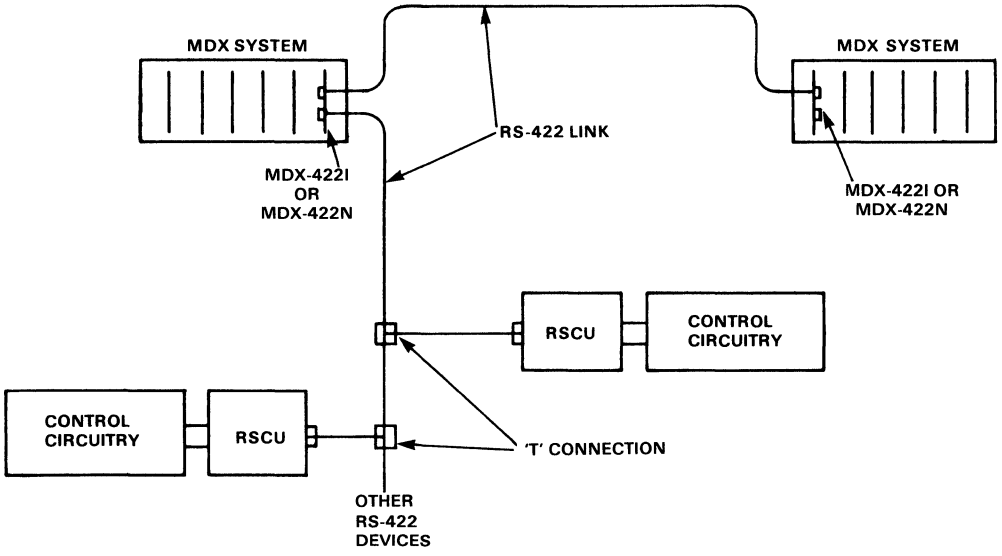
+5 Volts ± 5% at 1.0 A max.
+12 Volts ± 5% at 25 mA max.

DIMENSIONS

4.5 inches (114.3 mm) high by 6.5 inches (165.1 mm) long
0.675 inches (17.1 mm) maximum profile thickness
0.062 inches (1.6 mm) printed-circuit-board thickness

TYPICAL APPLICATION:

Figure 3



CONNECTORS

IVC

FUNCTION	DESCRIPTION	MATING CONNECTOR
STD-Z80 BUS	56-pin, dual	Viking 3VH28/ 1CE5 (printed circuit) Viking 3VH28/ 1CND5 (wire-wrap) Viking 3VH28/ 1CN5 (solder lug)
RS-422	Socket conn. 10-pin	Winchester 51-1110-01

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-422N	RS-422 interface module with operations manual	MK77676
	Operations manual,only.	4420053
	Z80-SIO Technical Manual	MK78583

RSCU
MK77983
REMOTE SERIAL CONTROL UNIT

FEATURES

- ☐ Utilizes the MK3873 Microprocessor
- ☐ Asynchronous Serial I/O
- ☐ Half-duplex operation
- ☐ Data rate of 9600 Baud
- ☐ 24 Parallel I/O bits individually strappable as input or output
- ☐ Single 5 Volt power supply
- ☐ Eight-bit selectable unit address
- ☐ Operation with up to 4000 feet of cable
- ☐ Up to 40 units on a RS-422 link
- ☐ Serial receiver/transmitter I/O protected against transients with up to 150 watts peak pulse power for 1 ms

DESCRIPTION

The RSCU (remote serial control unit) is an asynchronous serial-to-parallel conversion unit that is used for remote digital control over an RS-422 serial data link. Serial data is received and transmitted by using a half-duplex RS-422 (balanced differential) at 9600 Baud. The transmitter/receiver is capable of communicating up to 4000 feet from the host in noisy industrial environments. A system can use up to 40 RSCUs on one RS-422 link. See Figure 2 for an illustration of an RSCU system configuration.

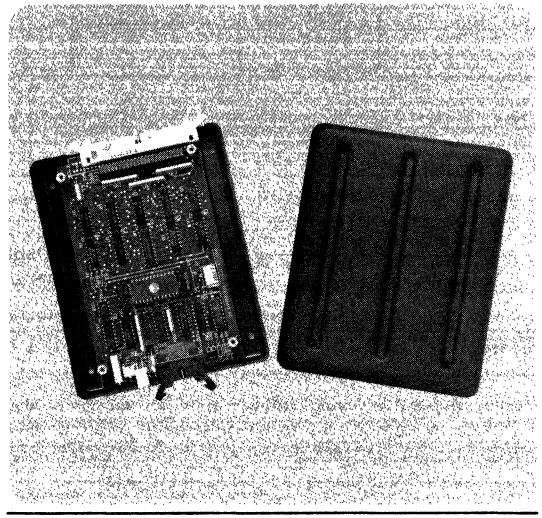
The RSCU is packaged in a black ABS plastic container for mounting purposes. The container also protects the board in industrial environments. Four mounting holes are provided in the back of the container. The mounting holes are easily accessed by removing four screws and the cover.

The unit's 24 parallel bits provide interface for up to 24 I/O devices such as optically isolated solid-state relays. Parallel devices, such as analog converters, may also be controlled.

The RSCU has five main elements: MK3873 microprocessor, address select logic, reset logic, serial line transmitter/receiver, and parallel I/O with data-direction jumpers (as illustrated in Figure 3).

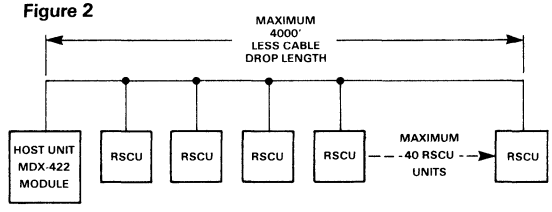
RSCU (MK77983) PHOTO

Figure 1



RSCU SYSTEM CONFIGURATION

Figure 2



MK3873

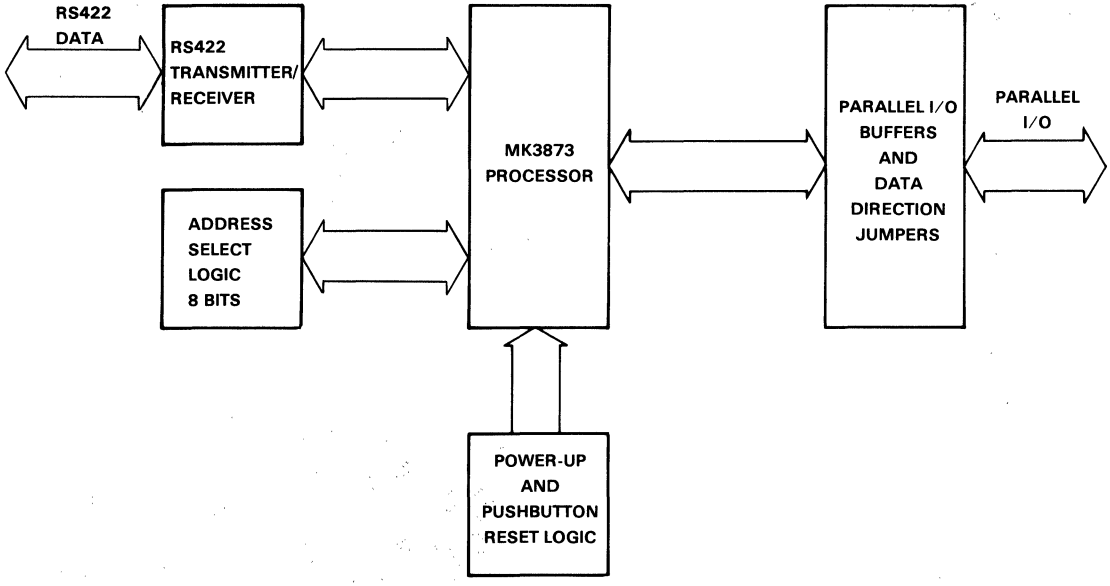
The MK3873 single-chip microprocessor has a serial I/O port that provides data for the RS-422 driver and receiver which communicates with the host system. The MK3873 also provides 29 bits of parallel I/O (Three bits used internally on the board and two that are unused.), of which 24 are available for off-board use.

ADDRESS SELECT LOGIC

The address select logic consists of an 8-bit parallel-in, serial-output shift register. The shift register inputs are jumper-selectable to the desired unit address for the RSCU. Power-up reset or push-button reset causes the microprocessor to load and read the shift register by serially shifting in the 8-address bits.

RSCU BLOCK DIAGRAM

Figure 3



RESET

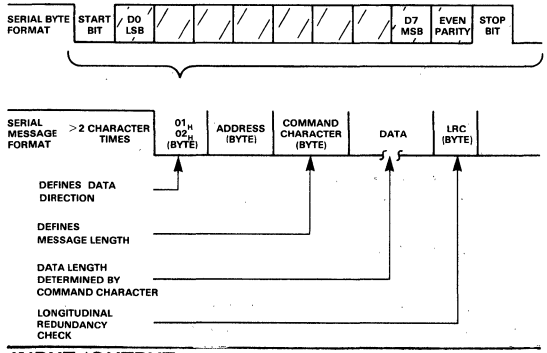
Power-up reset and push-button reset cause a reset pulse of approximately 20 ms to be generated. A comparator circuit also generates this reset signal and holds the reset line active if 5 Vdc power falls below 4.60 volts.

RS-422 RECEIVER AND TRANSMITTER

Bidirectional serial data is transmitted and received by an RS-422 line driver and receiver. Transient suppressors are provided to protect the serial I/O channel against transients of up to 150 watts peak for 1 ms duration. The serial data format is shown in Figure 4.

SERIAL DATA FORMAT

Figure 4



INPUT/OUTPUT

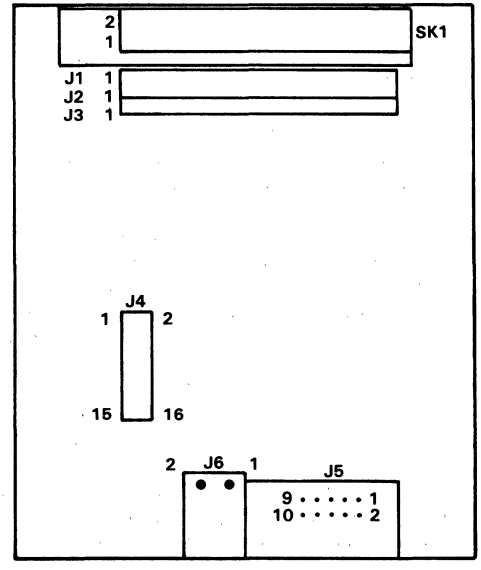
The 24-bit parallel I/O from the microprocessor is buffered in both input and output directions. Each bit must be selected as an input or output by installing a jumper in the appropriate position.

CONNECTORS AND HEADERS LAYOUT

Figure 5 illustrates the layout of connectors and headers on the RSCU board. Figures 6, 7, and 8 list the pinouts for SK1, J5, and J6, respectively.

CONNECTORS AND HEADERS LAYOUT

Figure 5



SK1 Pinout

Figure 6

Pin #		Pin #		Pin #		Pin #	
1	$\overline{P0\text{-}0}$	2	GND	27	$\overline{P4\text{-}5}$	28	
3	$\overline{P0\text{-}1}$	4		29	$\overline{P4\text{-}6}$	30	
5	$\overline{P0\text{-}2}$	6		31	$\overline{P4\text{-}7}$	32	
7	$\overline{P0\text{-}3}$	8		33	$\overline{P5\text{-}0}$	34	
9	$\overline{P0\text{-}4}$	10		35	$\overline{P5\text{-}1}$	36	
11	$\overline{P0\text{-}5}$	12		37	$\overline{P5\text{-}2}$	38	
13	$\overline{P0\text{-}6}$	14		39	$\overline{P5\text{-}3}$	40	
15	$\overline{P0\text{-}7}$	16		41	$\overline{P5\text{-}4}$	42	
17	$\overline{P4\text{-}0}$	18		43	$\overline{P5\text{-}5}$	44	
19	$\overline{P4\text{-}1}$	20		45	$\overline{P5\text{-}6}$	46	
21	$\overline{P4\text{-}2}$	22		47	$\overline{P5\text{-}7}$	48	
23	$\overline{P4\text{-}3}$	24		49	+5 V	50	GND
25	$\overline{P4\text{-}4}$	26					

J5 Pinout

Figure 7

Pin #

1	NC	6	$\overline{TXRX}$
2	NC	7	TXRX
3	NC	8	$\overline{TXRX}$
4	NC	9	GND
5	TXRX	10	GND

J6 Pinout

Figure 8

Pin #

1	GND
2	+5 V

STRAPPING

ADDRESS STRAPPING

A total of 255 (0 through 254) separate addresses may be chosen using the 8-address jumpers as shown in Figure 9. Address selection is accomplished by installing the address jumpers on header J4 in the desire configuration. Installing a jumper is equivalent to selecting the particular address bit to be zero.

NOTE: Jumpers must be placed on J4. All jumpers are installed on J4 when RSCU is shipped. Leaving J4 unstrapped gives the RSCU the address 0FFH which is not a recognized RSCU address.

Address bit A0 is the least significant bit, address A7 is the most significant and is the first bit shifted into the MK3873 when the address is loaded.

ADDRESS DECODING

Figure 9

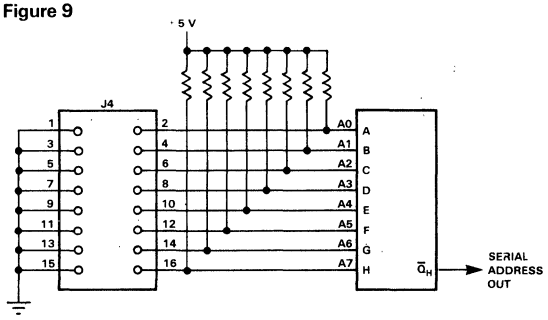
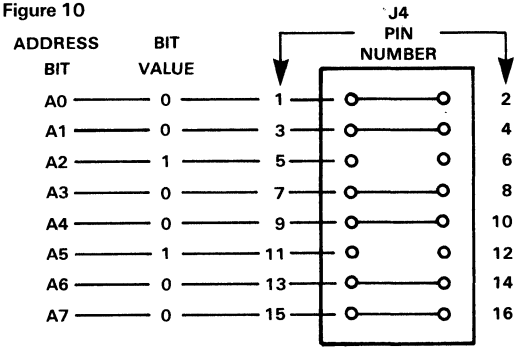


Figure 10 shows an example of strapping J4 for address 36 (24_H).

J4 STRAPPING EXAMPLE

Figure 10



DATA DIRECTION JUMPERS

The 24 parallel I/O signals are provided with jumpers so any bit may be configured as input or output. To configure the bit as input, jumpers are added between pins of J1 and J2. To configure the bit as output, jumpers are added between pins of J2 and J3. The RSCU board is shipped configured as input with jumpers installed between J1 and J2. See Figure 11.

DATA DIRECTION JUMPERS

Figure 11

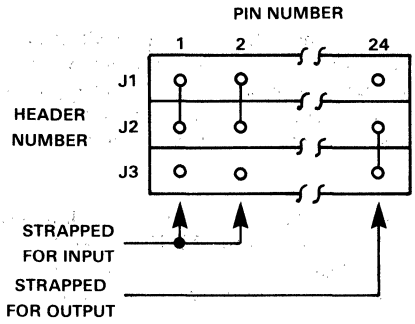


Table 1 is an example of data direction jumpering and the corresponding output signal mnemonic, associated jumper number, and I/O device (24-module opto I/O panel is used).

LINE TERMINATION RESISTOR

The RS-422 transmission line should be terminated on each end with a 200 ohm resistor. The purpose of this resistor is to reduce reflections from the end of the cable. Two printed circuit board holes are provided for a ¼ watt terminating resistor (R9). Only an RSCU placed on the extreme end of the transmission line requires termination.

LOW-VOLTAGE RESET ADJUSTMENT

Adjustment of R6 establishes the voltage level at which the MK3873 is reset on loss of power. This level is factory set at 4.6 volts and should not be changed. If R6 has been inadvertantly changed the following procedure should be used to reset the voltage level.

WARNING

Mostek does not assume any responsibility for module failure if this adjustment is made.

1. Adjust the power supply so that 4.6 volts is present on the 5 volt input (Pins 1 and 2 on J6).
2. Connect an oscilloscope or a voltmeter to the output of the ICL8211 (Pin 4 of U12).
3. Adjust R6 until the voltage on Pin 4 of the ICL8211 goes to a high level (greater than 2.4 V).
4. Slowly adjust the R6 in the opposite direction until the voltage goes to a low level (less than .7 V).

EXAMPLE OF DATA DIRECTION JUMPERING

Table 1

I/O PORT NUMBER	DATA DIRECTION JUMPER NUMBER	OPTO I/O MODULE NUMBER	OPTO I/O OUTPUT TERMINAL NUMBERS
P0-0	1	23	47-48
P0-1	2	22	45-46
P0-2	3	21	43-44
P0-3	4	20	41-42
P0-4	5	19	39-40
P0-5	6	18	37-38
P0-6	7	17	35-36
P0-7	8	16	33-34
P4-0	9	15	31-32
P4-1	10	14	29-30
P4-2	11	13	27-28
P4-3	12	12	25-26
P4-4	13	11	23-24
P4-5	14	10	21-22
P4-6	15	9	19-20
P4-7	16	8	17-18
P5-0	17	7	15-16
P5-1	18	6	13-14
P5-2	19	5	11-12
P5-3	20	4	9-10
P5-4	21	3	7-8
P5-5	22	2	5-6
P5-6	23	1	3-4
P5-7	24	0	1-2

SPECIFICATIONS

WORD SIZE

Data: 8-bits
I/O addressing: 8-bits

MEMORY CAPACITY

32 bytes RAM

UNIT ADDRESSING

On-board 8-bits jumper-selectable

I/O CAPACITY

Serial: One half-duplex serial port capable of asynchronous operation

SERIAL COMMUNICATION INTERFACE

One Port Signal:	RS-422
Transmitted Data:	Output
Received Data:	Input

CONNECTORS

FUNCTIONS	CONFIGURATION	MATING CONNECTOR
RS-422 Interface	Socket connector 10-Pin	Winchester 51-1110-01
I/O Bus Interface	Socket connector 50-Pin	Winchester 51-1150-01
Power	2-Pin connnector	Molex Connector 26-03-4020 Pins 08-50-0189

SERIAL BAUD RATE

9600 Baud

24-BIT PARALLEL INPUT/OUTPUT BUS

Inputs: I_{IL} = -2.7 ma
Bus Outputs: I_{OH} open collector
I_{OL} = 24 ma maximum at 0.5 volts

POWER SUPPLY REQUIREMENTS

+5 volts ± 5% at 1.5 A maximum

OPERATING TEMPERATURE

0°C to 60°C

ENCLOSURE DIMENSIONS

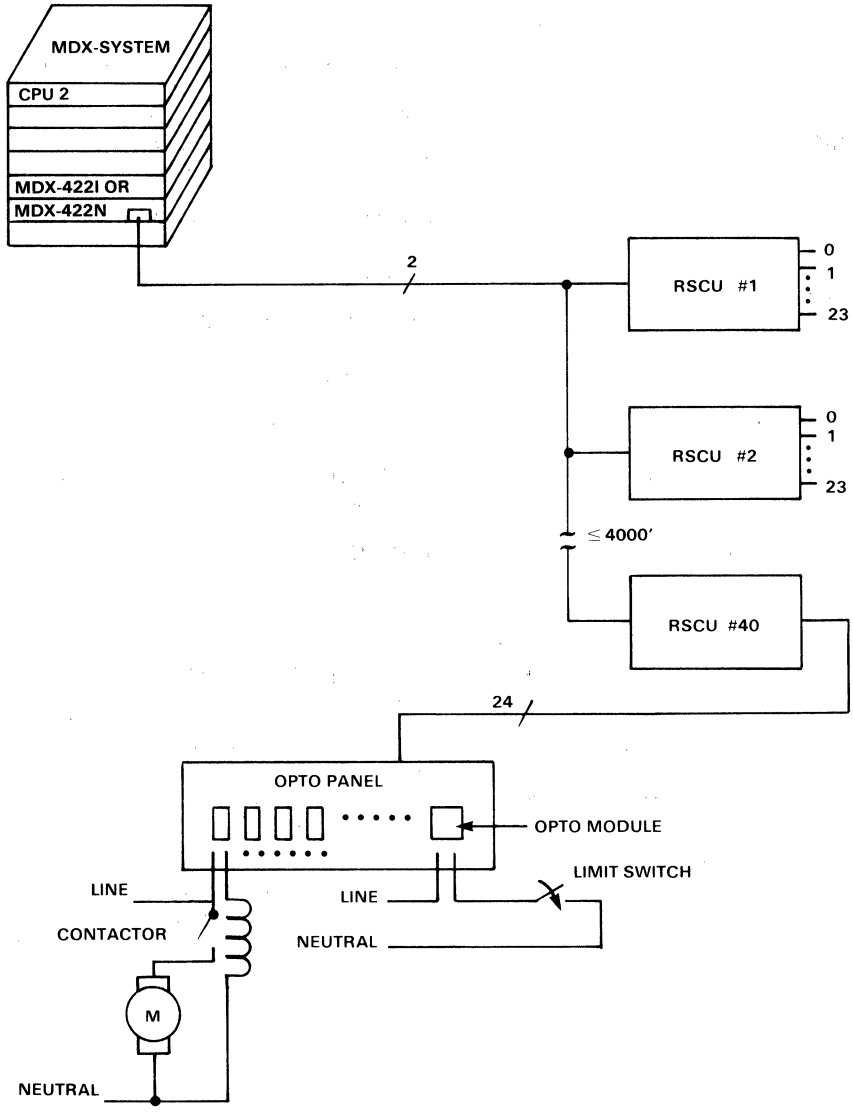
6.5" (165.1 mm) wide x 5.5" (139.7 mm) deep x 1.5" (38.1 mm) high

WEIGHT

1 lb.

TYPICAL APPLICATION

Figure 12



WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his measures may be required to correct the interference.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
RSCU	Microprocessor-based remote controller with Technical Manual	MK77983
MDX-422I	RS-422 interface card (isolated) with Operations Manual	MK77671
MDX-422N	RS-422 interface card (non-isolated) with Operations Manual	MK77676
	Technical Manual for RSCU	4420164
	Operations Manual for MDX-422I	4420071
	Operations Manual for MDX-422N	4420053
	ISCU User/Programming Manual (used with RSCU)	4420174

RIOC MK78208 REMOTE I/O CONTROLLER

FEATURES

- ☐ Utilizes the MK3873 Microprocessor
- ☐ Asynchronous Serial I/O
- ☐ Half-duplex operation
- ☐ Data rate of 9600 Baud
- ☐ 24 Parallel I/O bits individually strappable as input or output
- ☐ Single 5 Volt power supply
- ☐ Eight-bit selectable unit address
- ☐ Operation with up to 4000 feet of cable
- ☐ Up to 40 units on a RS-422 link
- ☐ Serial receiver/transmitter I/O protected against transients with up to 150 watts peak pulse power for 1 ms

DESCRIPTION

The RIOC (remote I/O controller) is an asynchronous serial-to-parallel conversion unit that is used for remote digital control over an RS-422 serial data link. Serial data is received and transmitted by the RIOC in the half-duplex mode at 9600 Baud. The transmitter/receiver (RS-422, balanced differential) is capable of communicating up to 4000 feet from the host in noisy industrial environments. A system can use up to 40 RIOCs on one RS-422 link. See Figure 2 for an illustration of an RIOC system configuration.

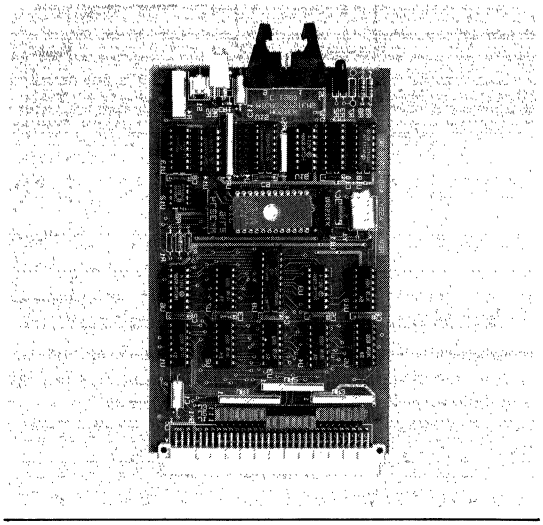
The unit's 24 parallel bits provide interface for up to 24 I/O devices such as optically isolated solid-state relays. Parallel devices, such as analog converters, may also be controlled.

The RIOC has five main elements: MK3873 microprocessor, address select logic, reset logic, serial line transmitter/receiver, and parallel I/O with data-direction jumpers (as illustrated in Figure 3).

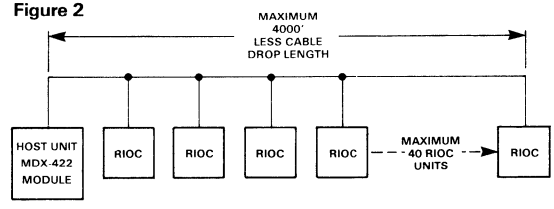
MK3873

The MK3873 single-chip microprocessor has a serial I/O port that provides data for the RS-422 driver and receiver which communicates with the host system. The MK3873 also provides 29 bits of parallel I/O (Three bits are used internally on the board and two are unused.), of which 24 are available for off-board use.

RIOC (MK78208) PHOTO
Figure 1



RIOC SYSTEM CONFIGURATION
Figure 2



ADDRESS SELECT LOGIC

The address select logic consists of an 8-bit parallel-in, serial-output shift register. The shift register inputs are jumper-selectable to the desired unit address for the RIOC. Power-up reset or push-button reset causes the microprocessor to load and read the shift register by shifting serially in the 8-address bits.

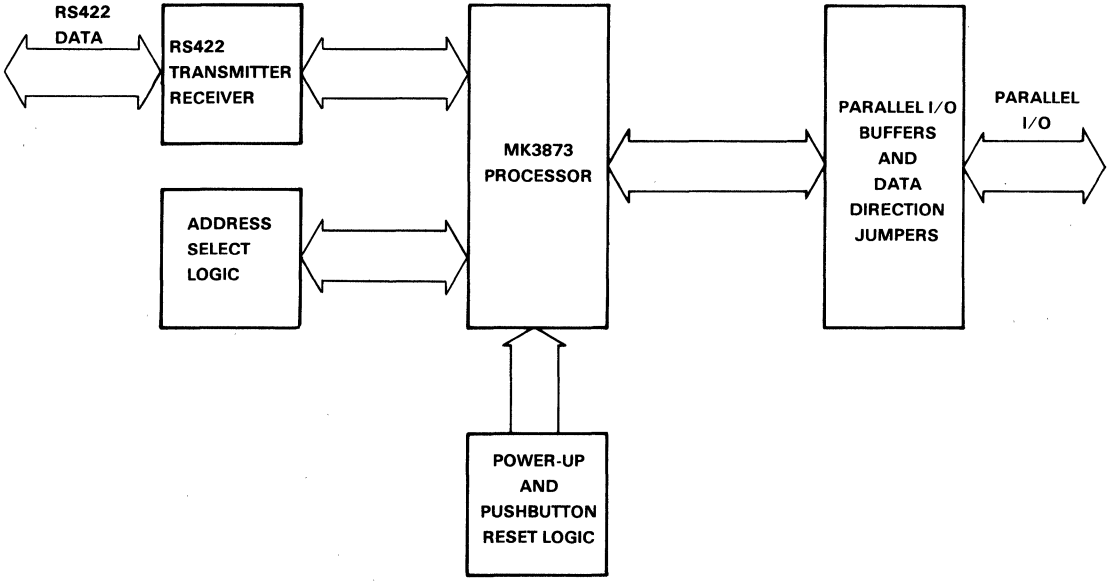
RESET

Power-up reset and push-button reset cause a reset pulse

IVC

RIOC BLOCK DIAGRAM

Figure 3



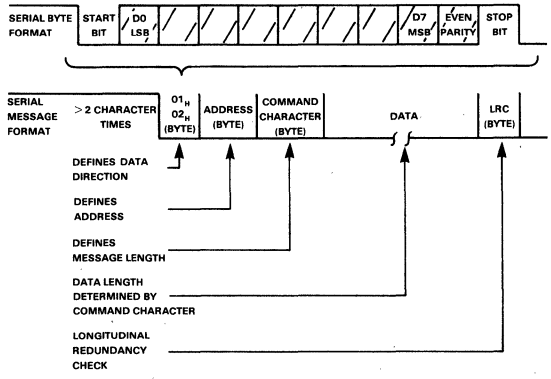
of approximately 20 ms to be generated. A comparator circuit also generates this reset signal and holds the reset line active if 5 Vdc power falls below 4.60 volts.

RS-422 RECEIVER AND TRANSMITTER

Bidirectional serial data is transmitted and received by an RS-422 line driver and receiver. Transient suppressors are provided to protect the serial I/O channel against transients of up to 150 watts peak for 1 ms duration. The serial data format is shown in Figure 4.

SERIAL DATA FORMAT

Figure 4



INPUT/OUTPUT

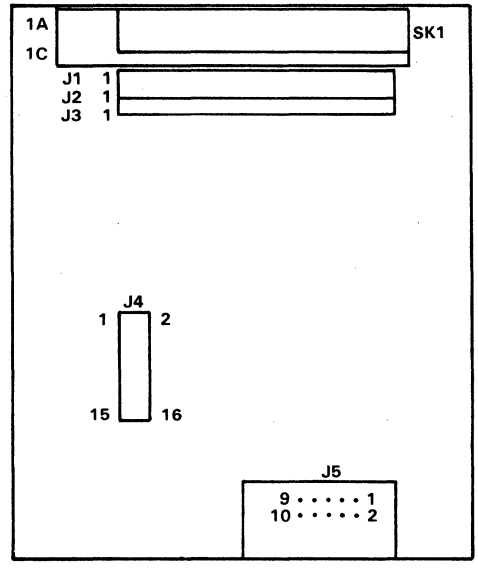
The 24-bit parallel I/O from the microprocessor is buffered in both input and output directions. Each bit must be selected as an input or output by installing a jumper in the appropriate position.

CONNECTORS AND HEADERS LAYOUT

Figure 5 illustrates the layout of the jumpers and headers on the RIOC board. Figures 6 and 7 list the pinout for SK1 and J5, respectively.

CONNECTORS AND HEADERS LAYOUT

Figure 5



SK1 Pinout
Figure 6

Pin #		Pin #		Pin #		Pin #	
1A	+5 V	1C	+5 V	17A	GND	17C	$\overline{P4\text{-}1}$
2A	+5 V	2C	+5 V	18A		18C	$\overline{P4\text{-}2}$
3A	NC	3C	NC	19A		19C	$\overline{P4\text{-}3}$
4A	GND	4C	GND	20A		20C	$\overline{P4\text{-}4}$
5A	GND	5C	GND	21A		21C	$\overline{P4\text{-}5}$
6A	NC	6C	NC	22A		22C	$\overline{P4\text{-}6}$
7A	NC	7C	NC	23A		23C	$\overline{P4\text{-}7}$
8A	GND	8C	$\overline{P0\text{-}0}$	24A		24C	$\overline{P5\text{-}0}$
9A		9C	$\overline{P0\text{-}1}$	25A		25C	$\overline{P5\text{-}1}$
10A		10C	$\overline{P0\text{-}2}$	26A		26C	$\overline{P5\text{-}2}$
11A		11C	$\overline{P0\text{-}3}$	27A		27C	$\overline{P5\text{-}3}$
12A		12C	$\overline{P0\text{-}4}$	28A		28C	$\overline{P5\text{-}4}$
13A		13C	$\overline{P0\text{-}5}$	29A		29C	$\overline{P5\text{-}5}$
14A		14C	$\overline{P0\text{-}6}$	30A		30C	$\overline{P5\text{-}6}$
15A		15C	$\overline{P0\text{-}7}$	31A		31C	$\overline{P5\text{-}7}$
16A	GND	16C	$\overline{P4\text{-}0}$	32A	GND	32C	+5 V

J5 Pinout
Figure 7

Pin #	
1	NC
2	NC
3	NC
4	NC
5	TXRX
6	$\overline{TXRX}$
7	TXRX
8	$\overline{TXRX}$
9	GND
10	GND

STRAPPING

ADDRESS STRAPPING

A total of 255 (0 through 254) separate addresses may be chosen using the address jumpers as shown in Figure 8. Address selection is accomplished by installing the address jumpers on header J4 in the desired configuration. Installing a jumper is equivalent to selecting the particular address bit to zero.

NOTES

Jumpers must be placed on J4. No jumpers on J4 is a condition which is not allowed.

All jumpers are installed on J4 when RIOC is shipped.

Address bit A0 is the least significant bit, address A7 is the most significant and is the first bit shifted into the MK3873 when the address is loaded.

ADDRESS DECODING
Figure 8

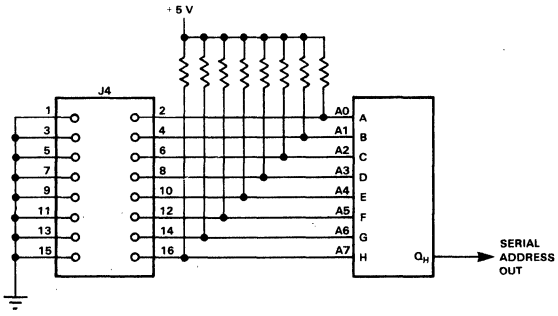
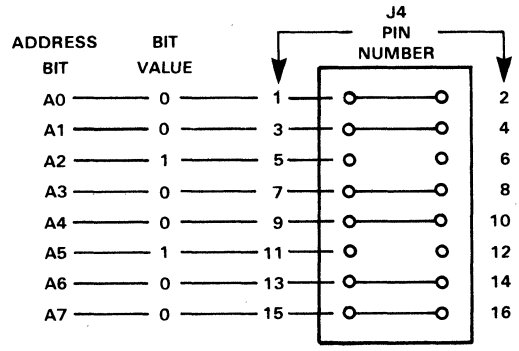


Figure 9 shows an example of strapping J4 for address 36 (24H).

J4 STRAPPING EXAMPLE
Figure 9



IVC

DATA DIRECTION JUMPERS

The 24 parallel I/O signals are provided with jumpers so any bit may be configured as input or output. To configure the bit as input jumpers are added between pins of J1 and J2. To configure the bit as output jumpers are added between pins of J2 and J3. The RIOC board is shipped configured as input with jumpers installed between J2 and J3. See Figure 10.

DATA DIRECTION JUMPERS

Figure 10

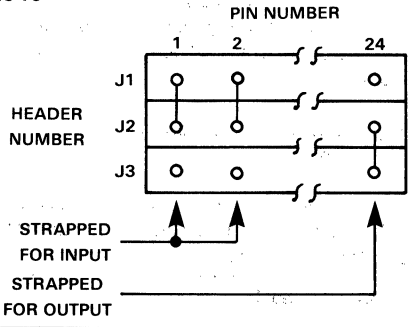


Table 1 is an example of data direction jumpering and the corresponding output signal mnemonic, associated jumper number, and I/O device (24-module opto I/O panel is used).

LINE TERMINATION RESISTOR

The RS-422 transmission line should be terminated on each end with a 200 ohm resistor. The purpose of this resistor is to reduce reflections from the end of the cable. Two printed circuit board holes are provided for a ¼ watt terminating resistor (R/9). Only an RIOC placed on the extreme end of the transmission line requires termination.

LOW-VOLTAGE RESET ADJUSTMENT

Adjustment of R6 establishes the voltage level at which the MK3873 is reset on loss of power. This level is factory set at 4.6 volts and should not be changed. If R6 has been inadvertantly changed the following procedure should be used to reset the voltage level.

WARNING

Mostek does not assume any responsibility for module failure if this adjustment is made.

1. Adjust the power supply so that 4.6 volts is present on the 5 volt input (Pins 1 and 2 on J6).
2. Connect an oscilloscope or a voltmeter to the output of the ICL8211 (Pin 4 of U12).
3. Adjust R6 until the voltage on Pin 4 of the ICL8211 goes to a high level (greater than 2.4 V).
4. Slowly adjust the R6 in the opposite direction until the voltage goes to a low level (less than .7 V).

SPECIFICATIONS

WORD SIZE

Data: 8-bits

I/O addressing: 8-bits

MEMORY CAPACITY

32 bytes RAM

UNIT ADDRESSING

On-board 8-bits jumper-selectable

I/O CAPACITY

Serial: One half-duplex serial port capable of asynchronous operation

SERIAL COMMUNICATIONS INTERFACE

One Port Signal:	RS-422
Transmitted Data:	Output
Received Data:	Input

EXAMPLE OF DATA DIRECTION JUMPERING

Table 1

I/O PORT	JUMPER	I/O PORT	JUMPER	I/O PORT	JUMPER
P0-0	1	P4-0	9	P5-0	17
P0-1	2	P4-1	10	P5-1	18
P0-2	3	P4-2	11	P5-2	19
P0-3	4	P4-3	12	P5-3	20
P0-4	5	P4-4	13	P5-4	21
P0-5	6	P4-5	14	P5-5	22
P0-6	7	P4-6	15	P5-6	23
P0-7	8	P4-7	16	P5-7	24

SERIAL BAUD RATE

9600 Baud

24-BIT PARALLEL INPUT/OUTPUT BUS

Inputs: I_{IL} = -2.7 ma

Bus Outputs: I_{OH} open collector output
I_{OL} = 24 ma maximum at 0.5 volts

POWER SUPPLY REQUIREMENTS

+5 volts ± 5% at 1.5 A maximum

OPERATING TEMPERATURE

0°C to 60°C

CARD DIMENSIONS

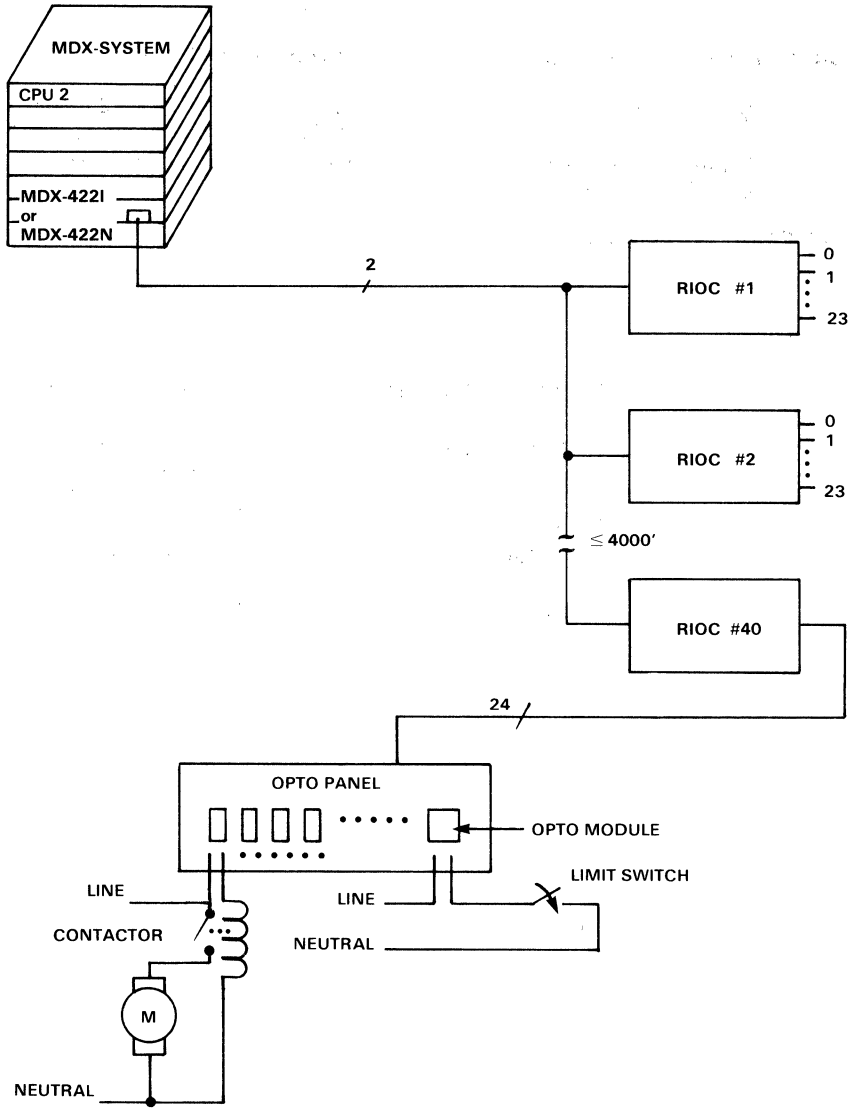
3.9 in (100 mm) high by 6.3 in (160 mm) long
0.675 in (1.71 cm) maximum profile thickness
0.062 in (0.16 cm) printed circuit board thickness

CONNECTORS

FUNCTIONS	CONFIGURATION	MATING CONNECTOR
RS-422 Interface	Socket connector 10-Pin	Winchester 51-1110-01
Power and I/O Bus Interface	Socket connector 64-Pin	Winchester 968-6033-0522-1

TYPICAL APPLICATION:

Figure 11



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ORDERING INFORMATION

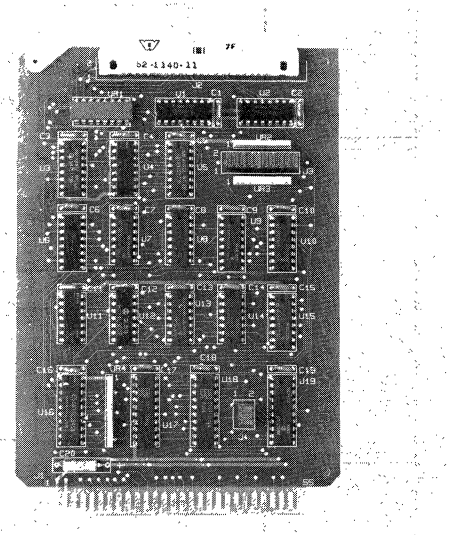
DESIGNATOR	DESCRIPTION	PART NO.
RIOC	Microprocessor-based remote controller with Technical Manual (European Version)	MK78208
MDX-422I	RS-422 interface card (isolated) with Operations Manual	MK77671
MDX-422N	RS-422 interface card (non-isolated) with Operations manual	MK77676
	Technical Manual for RIOC	4420165
	Operations Manual for MDX-422I	4420071
	Operations Manual for MDX-422N	4420053
	ISCU User/Programming Manual (used with RIOC)	4420174

MDX-DIOB1

FEATURES

- Provides parallel, memory-mapped Digital I/O Bus
- Services up to 64 8-bit I/O ports
- Services up to 16 Mostek DIOPs
- Balanced differential transmission with twisted-pair lines
- Up to 50 feet Digital I/O Bus length
- Address block selectable with jumpers
- One wait-state generator option
- 4 MHz capability
- Single +5 volt supply
- STD-Z80 Bus compatible

MDX-DIOB1
Figure 1



GENERAL DESCRIPTION

The Digital I/O Bus Interface Module (MDX-DIOB1) is a board that provides a simple interface between the STD-Z80 Bus and Mostek's Digital I/O Bus. It provides parallel, memory-mapped I/O to a maximum of 64 8-bit ports. Using 16 of Mostek's Digital I/O Panels (MDX-DIOP), MDX-DIOB1 is capable of servicing 256 relay modules.

Figure 2 is a block diagram illustrating the flow of address, data, and control signals on the MDX-DIOB1. The main elements of the board are address control, control logic, and differential bus transceivers and drivers. Input and output are handled by one 40-pin connector. A reset signal is encoded on the Digital I/O Bus so all MDX-DIOB1 output peripherals can be latched to their off state when a SYSRESET occurs.

ADDRESS DECODE

The address decode circuit is used to enable the board by comparing the upper ten address bits to preset strapping options. REFRESH is used in the comparison circiut to disable the board during a refresh cycle. A strapping option to include MEMEX is also provided to allow compatibility with MD systems using this signal.

CONTROL LOGIC

The control logic section is used to generate the control signals on the Digital I/O Bus and to enable the data bus transceivers in the proper direction. A one wait-state generator is provided as a strapping option to allow a 4 MHz operation with extended Digital I/O Bus lengths. All control logic functions are disabled by the address decode circuit with the exception of RESET which is enabled at all times.

DIFFERENTIAL TRANSCEIVER AND DRIVER CIRCUITS

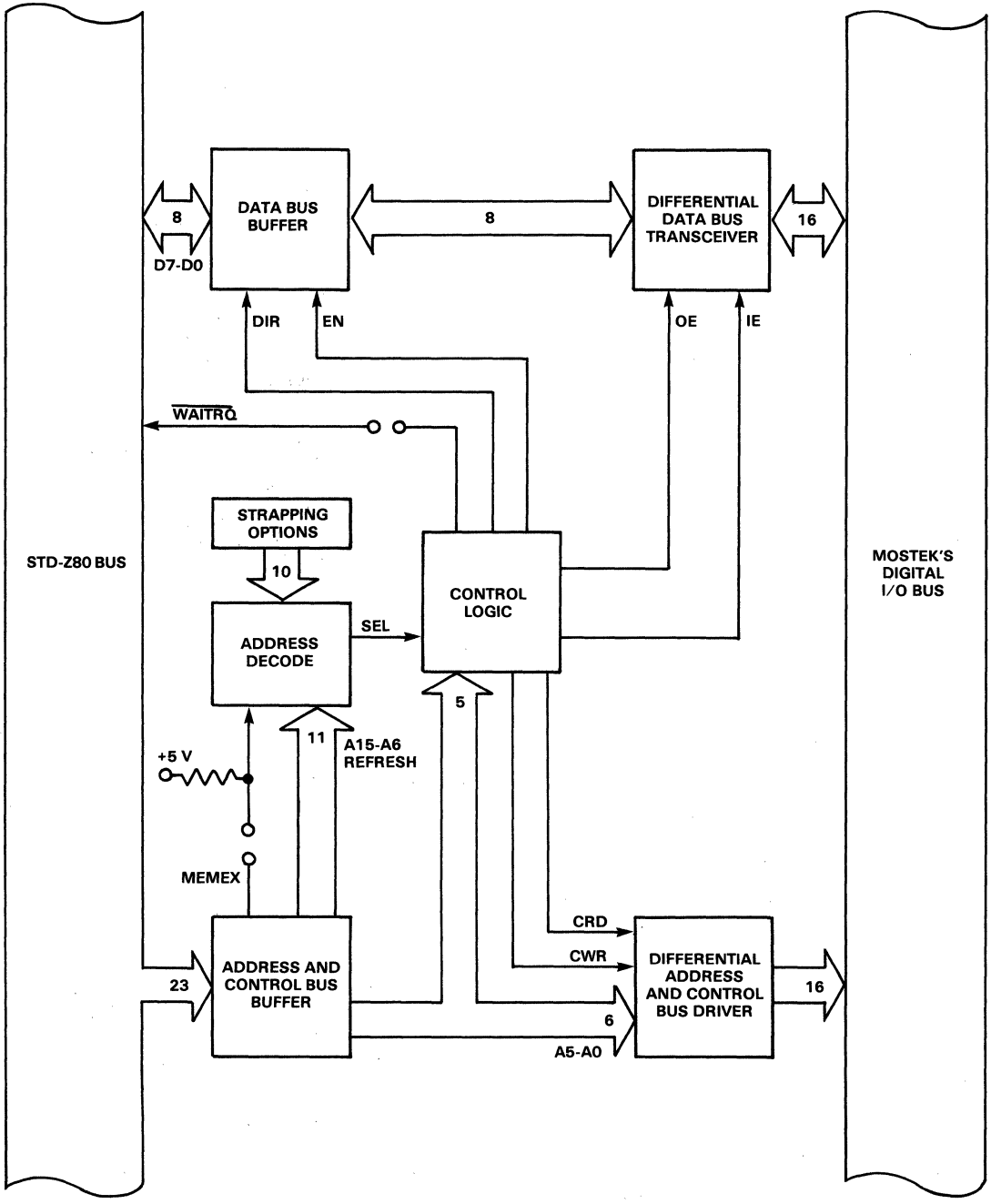
The differential transceiver and driver circuits are used to receive data signals and to transmit address, data, and control signals. Termination resistors are used at the data bus receivers to minimize signal reflections on the Digital I/O Bus.

ADDRESS CONFIGURATION STRAPPING

MDX-DIOB1 is address block selectable on 64 byte boundaries, providing for system flexibility. Address selection is done by matching the jumper plugs on J3 to the bit pattern for the desired address block. Inserting a jumper

MDX-DIOB1 BLOCK DIAGRAM

Figure 2



J3 HEADER PINOUT
Table 1

PINS	ADDRESS BIT
1 — 2	A15
3 — 4	A14
5 — 6	A13
7 — 8	A12
9 — 10	A11
11 — 12	A10
13 — 14	A9
15 — 16	A8
17 — 18	A7
19 — 20	A6

plug causes the corresponding address bit to be set low. The header pinout for J3 is defined in Table 1.

MEMORY EXPANSION

A memory expansion option is provided on MDX-DIOB1 to allow compatibility with systems that use the /MEMEX signal on the STD Bus. When this option is used, the address decode circuit on MDX-DIOB1 will generate its address select signal only when /MEMEX is active low. This option can be omitted by not installing a jumper plug between pins 1 and 2 on J4.

ONE WAIT-STATE GENERATOR

The one wait-state generator option is used with 4 MHz systems when the Digital I/O Bus length is greater than 25 feet. Otherwise, this option is not necessary and can be omitted by not installing a jumper between pins 3 and 4 on J4. The maximum recommended Digital I/O Bus length for 2.5 MHz or 4 MHz operation is 50 feet.

BUSAK TO STATUS 0

The BUSAK to STATUS 0 option is used to complete the priority daisy-chain when multiple DMAs are used in the system. Since multiple DMAs are not normally used in Mostek's MD systems, this option can be omitted by not installing a jumper between pins 5 and 6 on J4.

SHIPPING CONFIGURATION

All jumper locations are shipped open. A set of jumper plugs is supplied in a separate bag. A jumper option can be strapped using one of these jumper plugs or a wire-wrap connection.

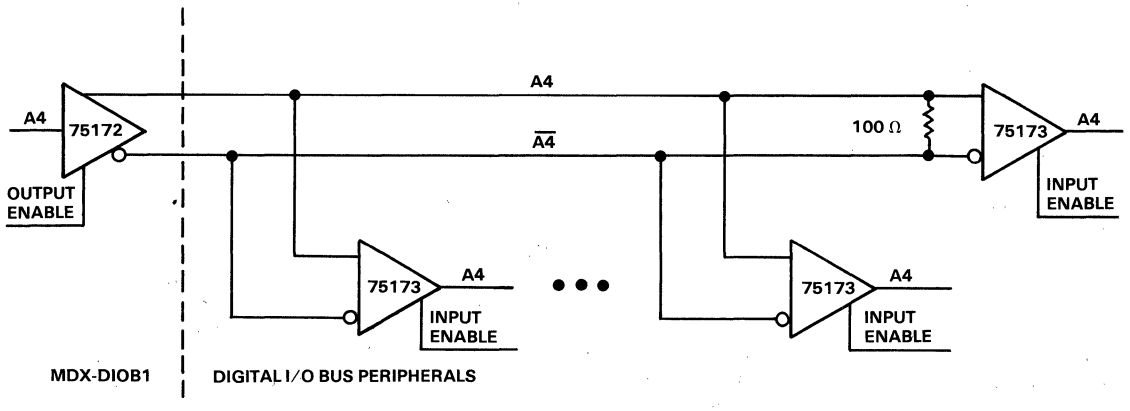
DIGITAL I/O BUS DESCRIPTION

All Digital I/O Bus lines are transmitted over balanced differential, twisted-pair lines with provisions for termination resistors at each end of the bus. This method ensures adequate noise immunity in industrial environments. A 10-pin latching type connector is used to provide positive locking to the Digital I/O Bus. A 40-conductor twisted-pair flat cable is used to interconnect Digital I/O Bus peripherals (Mostek's DIOP) and MDX-DIOB1. Figures 3 and 4 show the typical configurations for signals found on the Digital I/O Bus.

Address Signals

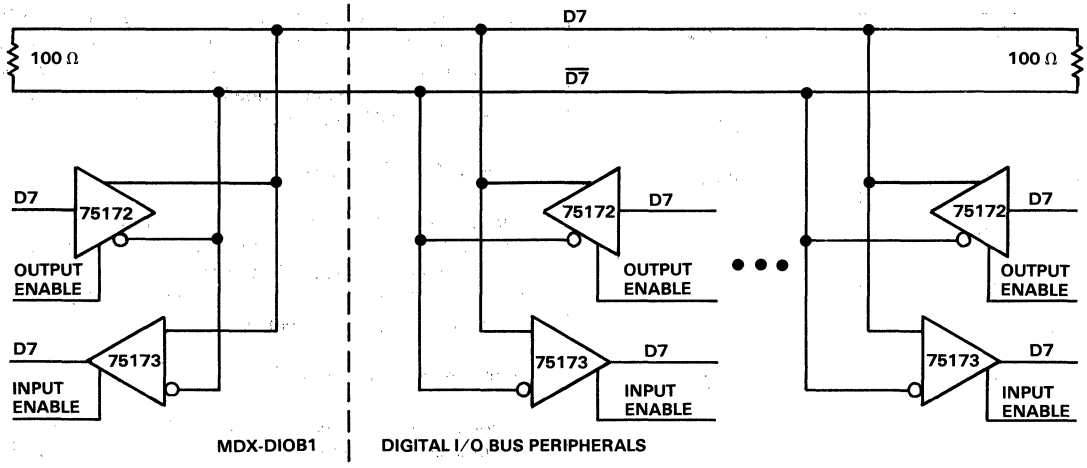
A5-A0 are used for port address selection. Each Digital I/O Bus peripheral compares these signals to its preset

TYPICAL ADDRESS OR CONTROL LINE
Figure 3



TYPICAL DATA LINE

Figure 4



strapping options to generate its address enable and port select signals. A5-A0 are always enabled on the Digital I/O Bus, which means a Digital I/O Bus peripheral will receive a valid address even though MDX-DIOB1 is disabled. This is of no consequence, however, since the control signals generated by MDX-DIOB1 will be inactive.

Control Signals

CRD and CWR are coded control signals. On receipt of a CRD command, the port selected by A5-A0 will place its data on D7-D0 of the Digital I/O Bus and hold it there until CRD is released. On receipt of a CWR command, the port selected by A5-A0 will capture the data on D7-D0 of the Digital I/O Bus at the trailing edge of CWR. If both CRD and CWR are active, a reset condition occurs which clears all Digital I/O Bus output peripherals. CRD and CWR are always enabled on the bus and are inactive unless one of the following conditions exist:

1. MDX-DIOB1 is enabled
2. SYSRESET is active
3. Digital I/O Bus is open-circuited

The differential receivers incorporate a fail-safe operation which will activate their outputs whenever their inputs are open-circuited. Note that this occurence generates a reset condition.

Data Signals

D7-D0 constitute the bidirectional data signals to and from all Digital I/O Bus peripherals. These lines are arranged in a party line configuration on the Digital I/O Bus and are always tri-stated unless MDX-DIOB1 is enabled.

Routing

The maximum recommended Digital I/O Bus length for 2.5 MHz operation is 50 feet, with or without the one wait-state generator option. For 4 MHz operation, the maxumim recommended length is 25 feet without the wait-state option, and 50 feet with the wait-state option. The 40-conductor twisted-pair flat cable can be tapped in 10-inch intervals, and should be laid out in a point-to-point, daisy-chain fashion. Branching from the Digital I/O Bus should be avoided. Termination resistors (100, 16 pin DIP packages) should be located only on the end of the Digital I/O Bus.

WARNING: If more than one Digital I/O Bus peripheral contains termination resistors, damage to the bus drivers will result.

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

Word Size

8 bits

Bus Interface

STD-Z80 BUS

Inputs	One 74 LS load maximum
Outputs	I_{OL} = 24 mA at 0.5 V maximum
	I_{OH} = -3 mA at 2.4 V minimum
	I_{OZL} = -200 μA maximum at 0.4 V
	I_{OZH} = 20 μA maximum at 2.7 V

DIGITAL I/O BUS

Inputs	V_{TH} = 0.2 V maximum (differential input sensitivity)
	I_{IN} = 1.0 mA maximum
Outputs	I_{OL} = 60 mA at 1.1 V maximum
	I_{OH} = –60 mA at 3.5 V minimum
	I_{OZ} = +100 μA maximum

Power Supply Requirements

+5 V ± 5% at 0.9 A maximum

Operating Temperature Range

0°C to 60°C

Interrupts

No interrupt capability

I/O Addressing

On board programmable on 64 byte boundaries

I/O Capacity

Provides parallel, memory-mapped I/O to a maximum of 64 8-bit ports, or 16 of Mostek's DIOPs

System Clock

250 KHz minimum
4.0 MHz maximum

MECHANICAL SPECIFICATIONS

Card Dimensions

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
0.675 in. (1.71 cm) maximum profile thickness
0.062 in. (0.16 cm) printed circuit board thickness

Connectors

Functions	Configuration	Mating Connectors
STD-Z80 BUS	56 pin dual readout 0.125 in. centers	Printed Circuit Viking 3VH28/1CE5
		Wire Wrap Viking 3VH28/1CND5
		Solder Lug Viking 3VH28/1CN5
DIGITAL I/O BUS	Socket Connector 40 pin dual readout 0.100 in. centers	3M 6040 Ansley 609-4001M

IVC

J2 CONNECTOR PINOUT

Table 3

	Component Side				Circuit Side			
	Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
	1	D7B	In/Out	High Order Data Bit	2	/D7B	In/Out	Inverted High Order Data Bit
	3	D6B	In/Out	High Order Data Bit	4	/D6B	In/Out	Inverted High Order Data Bit
	5	D5B	In/Out	High Order Data Bit	6	/D5B	In/Out	Inverted High Order Data Bit
Data	7	D4B	In/Out	High Order Data Bit	8	/D4B	In/Out	Inverted High Order Data Bit
Bus	9	D3B	In/Out	Low Order Data Bit	10	/D3B	In/Out	Inverted Low Order Data Bit
	11	D2B	In/Out	Low Order Data Bit	12	/D2B	In/Out	Inverted Low Order Data Bit
	13	D1B	In/Out	Low Order Data Bit	14	/D1B	In/Out	Inverted Low Order Data Bit
	15	D0B	In/Out	Low Order Data Bit	16	/D0B	In/Out	Inverted Low Order Data Bit
Control	17	CRDB	Out	Coded Read	18	/CRDB	Out	Inverted Coded Read
Bus	19	CWRB	Out	Coded Write	20	/CRWB	Out	Inverted Coded Write
	21	A5B	Out	Low Order Address Bit	22	/A5B	Out	Inverted Low Order Address Bit
	23	A0B	Out	Low Order Address Bit	24	/A0B	Out	Inverted Low Order Address Bit
Address	25	A4B	Out	Low Order Address Bit	26	/A4B	Out	Inverted Low Order Address Bit
Bus	27	A3B	Out	Low Order Address Bit	28	/A3B	Out	Inverted Low Order Address Bit
	29	A2B	Out	Low Order Address Bit	30	/A2B	Out	Inverted Low Order Address Bit
	31	A1B	Out	Low Order Address Bit	32	/A1B	Out	Inverted Low Order Address Bit
	33				34			
NOT	35				36			
USED	37				38			
	39				40			

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-DIOB1	Digital I/O Bus Interface with Technical Manual	MK77672
MDX-DIOB1 Technical Manual	Technical Manual only	4420069
DIOP	Digital I/O Panel	MK79863

DIOP

FEATURES

- ☐ Provides isolated computer interface to sixteen industrial I/O channels
- ☐ Uses plug compatible solid state or reed relay modules
- ☐ Wall or rack mountable
- ☐ Digital communication via balanced differential, twisted-pair lines
- ☐ Industrial barrier strip termination for field wiring
- ☐ Fuse holder provided for each relay
- ☐ LED status indicator for each relay
- ☐ Manual turn-on switch for each relay
- ☐ Quick disconnect from field wiring
- ☐ Data and data direction registers
- ☐ Single +5 volt supply
- ☐ Compatible with Mostek's DIGITAL I/O BUS
- ☐ Up to sixteen panels allowed on one DIGITAL I/O BUS

GENERAL INFORMATION

The DIGITAL I/O PANEL, DIOP, is a DIGITAL I/O BUS peripheral that provides a reliable interface between Mostek's DIGITAL I/O BUS and up to 16 industrial control signals. Solid state or reed relays are used to isolate the computer from the industrial signals. Each relay position is equipped with a fuse holder and LED status indicator. The relays can also be activated individually with momentary contact, manual override switches.

DIOP is designed for easy maintenance and low down time. The relay modules are socketed and can be replaced easily. The fuse holders for the relays accommodate standard 8AG (one inch) fuses. DIOP also features quick disconnect from the terminal strip so that the entire circuit board can be removed from its metal frame. This feature eliminates having to disconnect and reconnect 32 terminal screws whenever the board is replaced.

DIOP

Figure 1

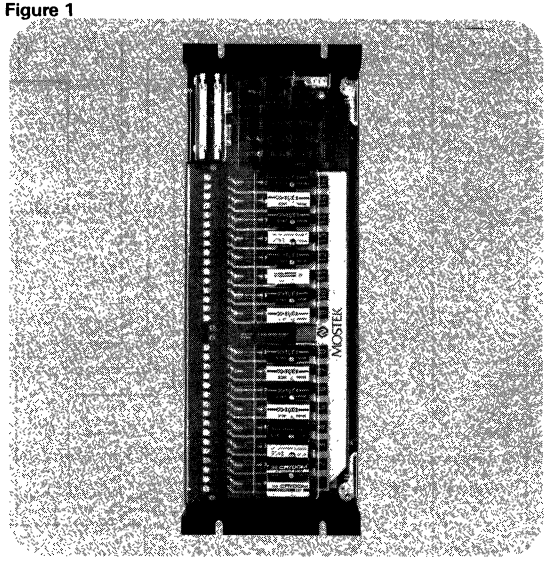


Figure 2 is a block diagram illustrating the flow of address, data, and control signals on the DIOP. The four main elements are the:

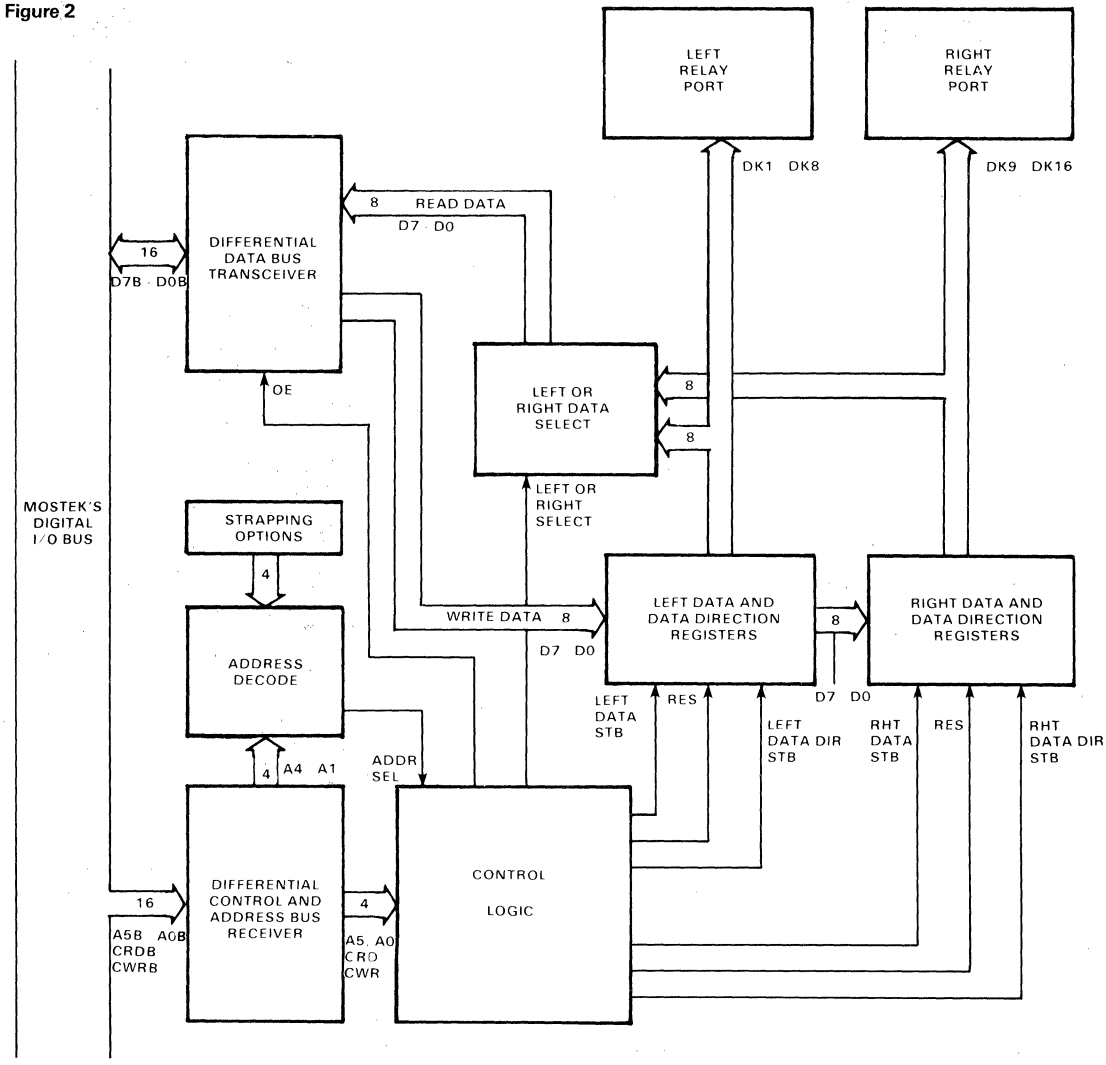
1) Differential bus transceiver and receiver circuit
2) Address decode and control logic circuit
3) Data and data direction registers
4) Relay ports

Input and output to the board are provided via two 40-pin connectors. Two connectors allow easy DIGITAL I/O BUS expansion (daisy-chaining). The differential transceiver and receiver circuits are used to transmit data signals and receive data, address, and control signals. Sockets for termination resistors are provided at the receiver inputs so that the DIGITAL I/O BUS can be terminated at the last DIGITAL I/O BUS peripheral on the bus.

The address decode and control logic circuit performs four functions. First, it enables the board by comparing A4-A1 to preset strapping options. Second, it strobes valid data into the proper data or data direction register during a write cycle. Third, it generates a left or right relay port select signal during a read cycle. Fourth, it generates a signal to reset all

BLOCK DIAGRAM

Figure 2



the data and data direction registers whenever a SYSTEM RESET occurs.

The data and data direction registers provide the output to the two 8-bit relay ports. The left and right data registers contain the actual output data for their respective relay ports, while the data direction registers mask the data registers from the input relay modules on a bit-by-bit basis. The output relay channels will be active only when the corresponding bit in both the data and data direction registers are in a "1" state. This hardware architecture supports the read-modify-write and bit control modes found in the Z80 microprocessor.

The relay ports constitute the I/O interface between the computer interface logic and the industrial control signals.

Each relay channel has associated with it:

1) Two terminal screws integral to a quick disconnect barrier strip.
2) A user-selectable 8AG (1 inch) fuse.
3) A user-selectable relay module.
4) An LED on/off indicator.
5) A momentary-contact, manual override switch.

Each manual override switch allows the simulation of I/O for debugging and troubleshooting purposes. If a channel is configured as an output, then a depressed switch will cause the relay to become active and the LED to light. If the channel is configured as an input, then a depressed switch will appear as "1 bit" within the appropriate data register, but the LED will not light.

J1, J2 CONNECTOR PINOUT

Table 1

	Component Side				Circuit Side			
	Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
Data Bus	1	D7B	In/Out	High Order Data Bit	2	/D7B	In/Out	Inverted High Order Data Bit
	3	D6B	In/Out	High Order Data Bit	4	/D6B	In/Out	Inverted High Order Data Bit
	5	D5B	In/Out	High Order Data Bit	6	/D5B	In/Out	Inverted High Order Data Bit
	7	D4B	In/Out	High Order Data Bit	8	/D4B	In/Out	Inverted High Order Data Bit
	9	D3B	In/Out	Low Order Data Bit	10	/D3B	In/Out	Inverted Low Order Data Bit
	11	D2B	In/Out	Low Order Data Bit	12	/D2B	In/Out	Inverted Low Order Data Bit
	13	D1B	In/Out	Low Order Data Bit	14	/D1B	In/Out	Inverted Low Order Data Bit
	15	D0B	In/Out	Low Order Data Bit	16	/D0B	In/Out	Inverted Low Order Data Bit
Control Bus	17	CRDB	In	Coded Read	18	/CRDB	In	Inverted Coded Read
	19	CWRB	In	Coded Write	20	/CWRB	In	Inverted Coded Write
Address Bus	21	A5B	In	Low Order Address Bit	22	/A5B	In	Inverted Low Order Address Bit
	23	A0B	In	Low Order Address Bit	24	/A0B	In	Inverted Low Order Address Bit
	25	A4B	In	Low Order Address Bit	26	/A4B	In	Inverted Low Order Address Bit
	27	A3B	In	Low Order Address Bit	28	/A3B	In	Inverted Low Order Address Bit
	29	A2B	In	Low Order Address Bit	30	/A2B	In	Inverted Low Order Address Bit
	31	A1B	In	Low Order Address Bit	32	/A1B	In	Inverted Low Order Address Bit
NOT USED	33				34			
	35				36			
	37				38			
	39				40			

J4 CONNECTOR PINOUT

Table 2

	Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
Power Bus	1	+5 V	In	Logic Power Supply	2	GND	In	Logic Ground
	3	+5 V	In	Logic Power Supply	4	GND	In	Logic Ground

NOTE:
All signals are referenced to DIOP.

Figure 3 is the mechanical assembly drawing for DIOP. The four main parts are the frame, side flanges, circuit board, and cover. The frame and side flanges are constructed of heavy-duty, black anodized aluminum. The side flanges can be oriented two different ways to allow wall or rack mounting of the assembly. The frame also contains the circuit board stand-offs and quick-disconnect terminal strips that mate to the edge connectors on the circuit board. The circuit board is inserted and removed from the frame by two latching ejectors. The connections to the DIGITAL I/O BUS and logic power supply (+5 V and GND) are made on the circuit board. The pop-off cover is intended to protect the high voltage lines on the circuit board from stray objects.

MOUNTING

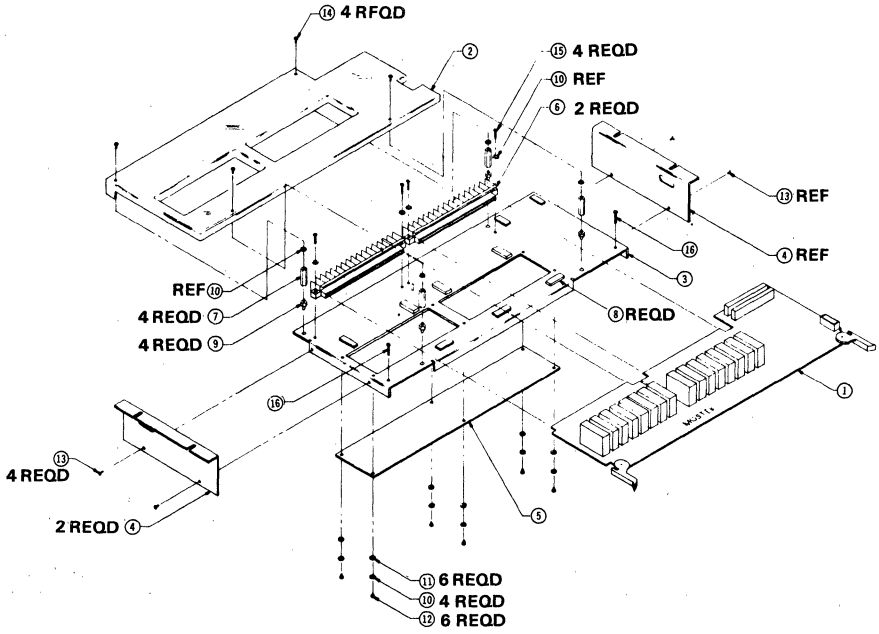
DIOP can be mounted on a wall or a 19-inch rack, depending on the orientation of the side flanges on the frame. The location of the unit should be chosen so that the DIGITAL I/O BUS (40-conductor, twisted-pair, flat cable) length is minimized. When many units are to be connected to the same DIGITAL I/O BUS, the units should be arranged so that they can be connected in a point-to-point, daisy-chain fashion with a minimum of cable length. Branching from the DIGITAL I/O BUS should be avoided. In any case, the DIGITAL I/O BUS should not exceed 50 feet in total length. See the DIOB1 Technical Manual for instructions on 4.0 MHz operation.

CONNECTIONS

The industrial field wiring is connected to terminal strips located on the metal frame. The fused (positive) line is on the right side of each terminal pair. The DIGITAL I/O BUS can

MECHANICAL ASSEMBLY DRAWING

Figure 3



be connected to either of the 40-pin headers (J1 and J2). It is recommended that a crimp-on connector with a strain relief be used so that all of the DIOP units can be connected without splicing the DIGITAL I/O BUS. A connector should never be placed in the twisted sections of the cable, only on the flat sections. The flat cable should be routed between units by looping the cable underneath the metal frame of each unit. Two headers are provided for the DIGITAL I/O BUS so the system can be expanded readily without making a new cable assembly for the entire DIGITAL I/O BUS. The +5 V and GND power supply lines are connected to J4. Pin 1 is used for +5 V and pin 2 is used for GND. Pins 3 (+5 V) and 4 (GND) can be used for optional remote sensing.

FUSING

DIOP provides fuse clips for user-selectable 8AG (1 inch) fuses for each relay module. Refer to the relay module manufacturer's specifications for the proper fuse ratings.

RELAY MODULES

DIOP is equipped to handle a variety of plug-in input and output relays. The different types include solid-state and reed relays. The user should be aware that certain output relay modules use zero-cross switching, sometimes a desirable feature, while others do not offer this feature. Manufacturers of pin compatible modules include OPTO-22, GORDOS, ELEC-TROL, MOTOROLA, and CRYDOM. The relay modules can be arranged in any mix on DIOP.

ADDRESS CONFIGURATION STRAPPING

Header J3 is used to configure the DIOP selection number when more than one DIOP is used on the DIGITAL I/O BUS. This is done by strapping the proper pins on J3 to match address bits A4-A1. Table 3 shows how the address bits are arranged on J3.

J3 HEADER PINOUT
Table 3

Pins	Address Bit
1-2	A4
3-4	A3
5-6	A2
7-8	A1

Strapping respective pins together causes the corresponding address bit to be set low. Table 4 shows all the strapping combinations for J3 that correspond to the 16 possible DIOP selection numbers on the DIGITAL I/O BUS. A "1" implies that the pins are open, while a "0" implies that the pins are closed, i.e., strapped. Figure 4 provides an optional work sheet for the strapping options on J3.

SHIPPING CONFIGURATION

All jumper locations are shipped open. Jumper plugs are included in a separate bag for user strapping.

POSSIBLE J3 HEADER CONFIGURATIONS

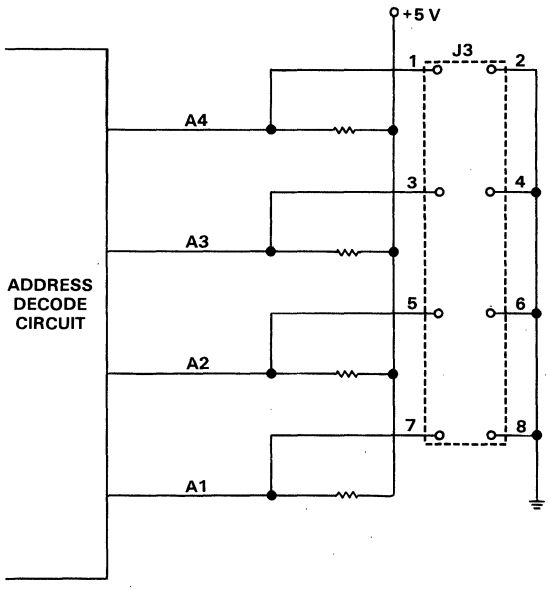
Table 4

Pins 1-2	Pins 3-4	Pins 5-6	Pins 7-8	DIOP Selection Number
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

0 = CLOSED 1 = OPEN

ADDRESS STRAPPING OPTION WORKSHEET

Figure 4



DIGITAL I/O BUS DESCRIPTION

All DIGITAL I/O BUS lines are transmitted over balanced differential, twisted pair lines with provisions for termination resistors at each end of the bus. This method ensures adequate noise immunity in industrial environments. A 40-pin latching type connector is used to provide positive locking to the DIGITAL I/O BUS. A 40-conductor, twisted-pair, flat cable is used to interconnect DIOP and other DIGITAL I/O BUS peripherals to DIOB1. The bus receivers are equipped with a fail-safe operation which will reset all data and data direction registers should the bus cable be interrupted. The data read by the CPU, however, will be FF. Figure 5 and Figure 6 show the bus configurations for the signals on the DIGITAL I/O BUS.

WARNING: If resistor termination packages are located on more than one DIOP on the same DIGITAL I/O BUS, damage to the bus drivers will result.

Address Signals

A4-A1 selects which DIOP unit on the DIGITAL I/O BUS communicates with DIOB1. Each DIOP compares these four address signals to on-board strapping options to generate its address enable signal. A0 is used to select the left (A0 low) or right (A0 high) relay port on the selected DIOP during a read or write cycle. A5 is used to select a data (A5 low) or data direction (A5 high) register on the selected DIOP during a write cycle. Table 5 shows the address bit patterns (A5-A0) used to select the ports in a system containing 16 DIOP units.

Control Signals

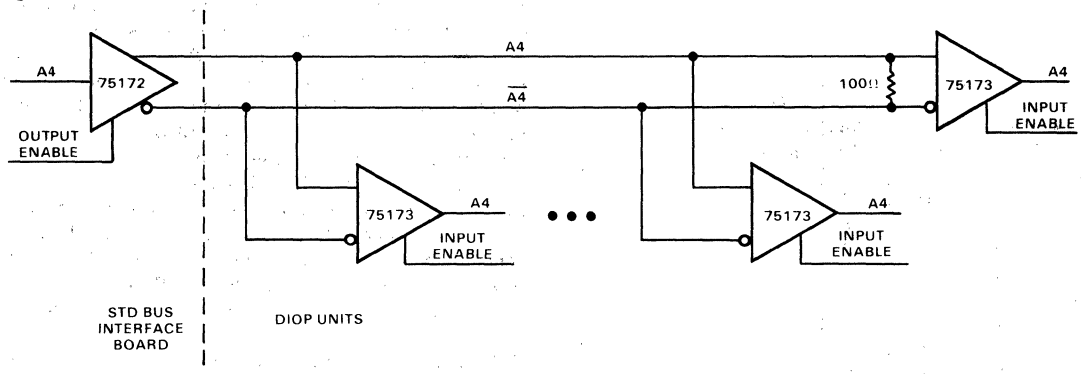
CRD and CWR are the coded control signals. On receipt of a CRD command, the relay port selected by A4-A0 will place its data on D7-D0 of the DIGITAL I/O BUS, and hold it there until CRD is released. A5 is a "don't care" signal during a read cycle. On receipt of a CWR command, the data or data direction register selected by A5-A0 will capture the data on D7-D0 of the DIGITAL I/O BUS at the trailing edge of CWR. The coincidence of CRD and CWR both active constitutes a reset condition which clears the data and data direction registers on all DIGITAL I/O BUS peripherals. The data direction registers are write only registers and should be set by the restart or power-up routine software. The data registers should be used to manipulate the output data during normal program execution.

Data Signals

D7-D0 serve as the bidirectional data signals to and from all DIGITAL I/O BUS peripherals. These lines are arranged in a party-line configuration on the DIGITAL I/O BUS. Table 6 shows the relationship between the relay channel designators (DK1-DK16) and the data signals on the DIGITAL I/O BUS.

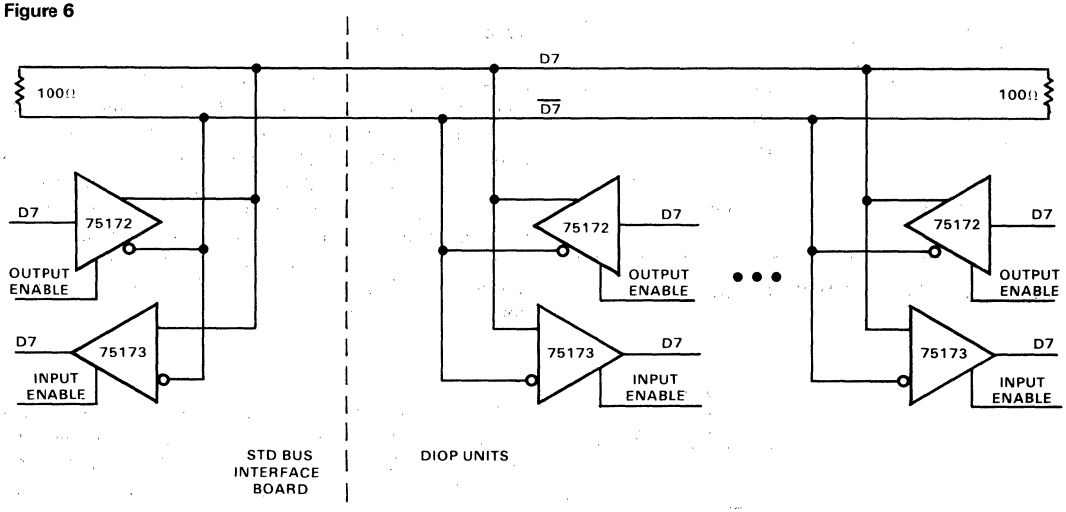
TYPICAL ADDRESS OR CONTROL LINE

Figure 5



TYPICAL DATA LINE

Figure 6



ADDRESS BIT PATTERNS FOR DIOP PORT SELECTION

Table 5

A5	A4	A3	A2	A1	A0	DIOP Port Selected
0	0	0	0	0	0	PANEL NO. 1 LEFT DATA PORT
0	0	0	0	0	1	PANEL NO. 1 RIGHT DATA PORT
0	0	0	0	1	0	PANEL NO. 2 LEFT DATA PORT
0	0	0	0	1	1	PANEL NO. 2 RIGHT DATA PORT
0	0	0	1	0	0	PANEL NO. 3 LEFT DATA PORT
0	0	0	1	0	1	PANEL NO. 3 RIGHT DATA PORT
0	0	0	1	1	0	PANEL NO. 4 LEFT DATA PORT
0	0	0	1	1	1	PANEL NO. 4 RIGHT DATA PORT
0	0	1	0	0	0	PANEL NO. 5 LEFT DATA PORT
0	0	1	0	0	1	PANEL NO. 5 RIGHT DATA PORT
0	0	1	0	1	0	PANEL NO. 6 LEFT DATA PORT

ADDRESS BIT PATTERNS FOR DIOP PORT SELECTION (Cont.)

Table 5

A5	A4	A3	A2	A1	A0	DIOP Port Selected
0	0	1	0	1	1	PANEL NO. 6 RIGHT DATA PORT
0	0	1	1	0	0	PANEL NO. 7 LEFT DATA PORT
0	0	1	1	0	1	PANEL NO. 7 RIGHT DATA PORT
0	0	1	1	1	0	PANEL NO. 8 LEFT DATA PORT
0	0	1	1	1	1	PANEL NO. 8 RIGHT DATA PORT
0	1	0	0	0	0	PANEL NO. 9 LEFT DATA PORT
0	1	0	0	0	1	PANEL NO. 9 RIGHT DATA PORT
0	1	0	0	1	0	PANEL NO. 10 LEFT DATA PORT
0	1	0	0	1	1	PANEL NO. 10 RIGHT DATA PORT
0	1	0	1	0	0	PANEL NO. 11 LEFT DATA PORT
0	1	0	1	0	1	PANEL NO. 11 RIGHT DATA PORT
0	1	0	1	1	0	PANEL NO. 12 LEFT DATA PORT
0	1	0	1	1	1	PANEL NO. 12 RIGHT DATA PORT
0	1	1	0	0	0	PANEL NO. 13 LEFT DATA PORT
0	1	1	0	0	1	PANEL NO. 13 RIGHT DATA PORT
0	1	1	0	1	0	PANEL NO. 14 LEFT DATA PORT
0	1	1	0	1	1	PANEL NO. 14 RIGHT DATA PORT
0	1	1	1	0	0	PANEL NO. 15 LEFT DATA PORT
0	1	1	1	0	1	PANEL NO. 15 RIGHT DATA PORT
0	1	1	1	1	0	PANEL NO. 16 LEFT DATA PORT
0	1	1	1	1	1	PANEL NO. 16 RIGHT DATA PORT
1	0	0	0	0	0	PANEL NO. 1 LEFT DATA DIRECTION PORT
1	0	0	0	0	1	PANEL NO. 1 RIGHT DATA DIRECTION PORT
1	0	0	0	1	0	PANEL NO. 2 LEFT DATA DIRECTION PORT
1	0	0	0	1	1	PANEL NO. 2 RIGHT DATA DIRECTION PORT
1	0	0	1	0	0	PANEL NO. 3 LEFT DATA DIRECTION PORT
1	0	0	1	0	1	PANEL NO. 3 RIGHT DATA DIRECTION PORT
1	0	0	1	1	0	PANEL NO. 4 LEFT DATA DIRECTION PORT
1	0	0	1	1	1	PANEL NO. 4 RIGHT DATA DIRECTION PORT
1	0	1	0	0	0	PANEL NO. 5 LEFT DATA DIRECTION PORT
1	0	1	0	0	1	PANEL NO. 5 RIGHT DATA DIRECTION PORT
1	0	1	0	1	0	PANEL NO. 6 LEFT DATA DIRECTION PORT
1	0	1	0	1	1	PANEL NO. 6 RIGHT DATA DIRECTION PORT
1	0	1	1	0	0	PANEL NO. 7 LEFT DATA DIRECTION PORT
1	0	1	1	0	1	PANEL NO. 7 RIGHT DATA DIRECTION PORT
1	0	1	1	1	0	PANEL NO. 8 LEFT DATA DIRECTION PORT
1	0	1	1	1	1	PANEL NO. 8 RIGHT DATA DIRECTION PORT
1	1	0	0	0	0	PANEL NO. 9 LEFT DATA DIRECTION PORT
1	1	0	0	0	1	PANEL NO. 9 RIGHT DATA DIRECTION PORT
1	1	0	0	1	0	PANEL NO. 10 LEFT DATA DIRECTION PORT
1	1	0	0	1	1	PANEL NO. 10 RIGHT DATA DIRECTION PORT
1	1	0	1	0	0	PANEL NO. 11 LEFT DATA DIRECTION PORT
1	1	0	1	0	1	PANEL NO. 11 RIGHT DATA DIRECTION PORT
1	1	0	1	1	0	PANEL NO. 12 LEFT DATA DIRECTION PORT
1	1	0	1	1	1	PANEL NO. 12 RIGHT DATA DIRECTION PORT
1	1	1	0	0	0	PANEL NO. 13 LEFT DATA DIRECTION PORT
1	1	1	0	0	1	PANEL NO. 13 RIGHT DATA DIRECTION PORT
1	1	1	0	1	0	PANEL NO. 14 LEFT DATA DIRECTION PORT
1	1	1	0	1	1	PANEL NO. 14 RIGHT DATA DIRECTION PORT
1	1	1	1	0	0	PANEL NO. 15 LEFT DATA DIRECTION PORT
1	1	1	1	0	1	PANEL NO. 15 RIGHT DATA DIRECTION PORT
1	1	1	1	1	0	PANEL NO. 16 LEFT DATA DIRECTION PORT
1	1	1	1	1	1	PANEL NO. 16 RIGHT DATA DIRECTION PORT

DATA BIT CONFIGURATION
Table 6

Data Bit	A0	Relay Channel Designator
D7	0	DK1
D6	0	DK2
D5	0	DK3
D4	0	DK4
D3	0	DK5
D2	0	DK6
D1	0	DK7
D0	0	DK8
D7	1	DK9
D6	1	DK10
D5	1	DK11
D4	1	DK12
D3	1	DK13
D2	1	DK14
D1	1	DK15
D0	1	DK16

ELECTRICAL SPECIFICATIONS

Word Size

8 bits

DIGITAL I/O BUS Interface

Inputs V_{TH} = 0.2 V maximum (Differential input sensitivity)
I_{IN} = 1.0 mA maximum

Outputs I_{OL} = 60 mA at 1.1 V maximum
I_{OH} = -60 mA at 3.5 V minimum
I_{OZ} = ±100 μA maximum

Power Supply Requirements

+5 V ±5% at 0.9 A maximum

Operating Temperature Range

0°C to 60° C

Interrupts

No interrupt capability

I/O Addressing

On board selectable (four address bits)

I/O Capacity

Each DIOP provides interface between a maximum of sixteen relay modules and Mostek's DIGITAL I/O BUS.

MECHANICAL SPECIFICATIONS

Dimensions

19 in. (48.26 cm) wide by 7 in. (17.78 cm) high by 2.5 in. (6.35cm) deep (rack mount).

Connectors

Function	Configuration	Reference Designator	Mating Connector
Power	Socket Connector 4 pin, PC mount 0.200 in. centers	J4	AMP 1-480-424-0
Control	2 socket connectors 40 pin dual, straight 0.100 in. centers	J1, 2	3M 6040 Ansley 609-4001M
Load	Edge connector 16 position terminal strip 0.375 in. centers	TB1, 2	14 AWG wire

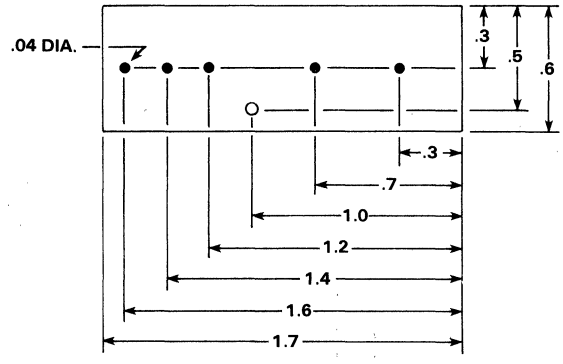
Fusing

Equipped with 8AG (1 inch) fuse clips for each relay module.

Relay Sockets

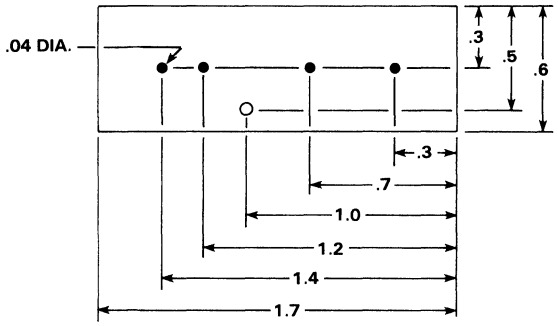
Figures 7 and 8 show the pin configurations for relay modules that are compatible with DIOP. A 4-40 screw is used to hold each module in place. DIOP is not compatible with buffered output relay modules.

PIN CONFIGURATION FOR INPUT RELAY MODULES
Figure 7



PIN CONFIGURATION FOR OUTPUT RELAY MODULES

Figure 8



SYSTEM, EXAMPLE

This section has been included to illustrate how a basic DIOB1/DIOP system could be configured and applied to a typical industrial control situation. The application chosen for this example is a motor driven conveyor equipped with one start push button and seven halt switches distributed along the conveyor. Also required is a RUNNING light, a STOPPED light, and a circuit to control the motor starter.

Assuming that it is desired to have the eight inputs connected to the right relay port of DIOP #1 and the two outputs connected to the left relay port of DIOP #2, the following program segments will control the process described above.

Example Setup

Table 6 shows the required strapping configuration on DIOB1, DIOP #1, and DIOP #2 and the corresponding HEX addresses. System memory must be configured so that there is a vacant 64-byte slot beginning at D000H for the memory-mapped DIOB1. Coincidentally, Header J3 is used for address strapping both DIOB1 and DIOP.

EXAMPLE STRAPPING

Table 7

Device	Port Address		J3 Address Strapping
	Data	Data Direction	
DIOB1	D000-D01F H	D020-D03F H	5- 6 9-10 11-12 13-14 15-16 17-18 19-20
DIOP #1 Left Relay Port (DK1-8)	D000 H	D020 H	1- 2 3- 4 5- 6
DIOP #1 Right Relay Port (DK9-16)	D001 H	D021 H	7- 8
DIOP #2 Left Relay Port (DK1-8)	D002 H	D022 H	1- 2 3- 4
DIOP #2 Right Relay Port (DK9-16)	D003 H	D023 H	5- 6

Table 8 shows the correspondence between the computer data bits and the field wiring configuration for the relay channels used on DIOP #1 and DIOP #2. The inclusion of an appropriate power source is necessary, of course, but has been omitted for simplicity.

EXAMPLE FIELD WIRING

Table 8

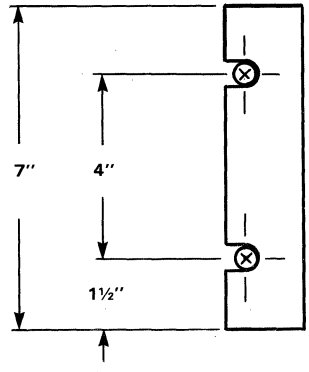
Data Bit	Address	Function	Corresponding Field Wiring
D6-D0	D001 H	"STOP CONVEYOR" INPUT (HALT BITS)	RELAY 10-16 DIOP #1 EACH WIRED TO MAINTAIN CONTACT, NORMALLY CLOSED SWITCH
D7	D001 H	"START CONVEYOR" INPUT (START BIT)	RELAY 9 OF DIOP #1 WIRED TO A MOMENTARY CONTACT, NORMALLY OPEN PUSHBUTTON
D6	D002 H	"STOPPED" INDICATOR OUTPUT (STOP BIT)	RELAY 2 OF DIOP #2 WIRED TO A RED "STOPPED" LIGHT
D7	D002 H	"RUNNING"INDICATOR OUTPUT (RUN BIT)	RELAY 1 OF DIOP #2 WIRED TO A GREEN "RUNNING" LIGHT AND MOTOR STARTER

EXAMPLE SOFTWARE

```
                                        MOSTEK MACRO-80 22-OCT-80 V2.3 PAGE 1
LOC OBJ.CODE      STMT-NR  SOURCE- STMT  PASS 2 DIOPEX   DIOPEX  REL
                                    .
                                    .
                                    .
0000'DD2100D0        1     SETUP   LD    IX,0D000H
0004 DD362100        2             LD    (IX+21H),0      ; SET DATA DIRECTION REGISTER FOR INPUTS
0008 DD3622E0        3             LD    (IX+22H),0E 0H  ; AND FOR OUTPUTS
                                    .
                                    .
                                    .
                                    .
                                    .
                                    .
                                    .
                                    .
000C'DD7E01          8     POLL    LD    A,(IX+1)        ; READ INPUTS
000F CBBF            9             RES   7,A             ; CLEAR START BIT (IF ON)
0011 DDCB027E       10             BIT   7,(IX+2)        ; IS RUN BIT ON?
0015 2011           11             JR    NZ,RUNNING      ; BRANCH IF SO

0017 FE7F           13             CP    7FH             ; TEST FOR ACTIVE HALT SWITCH(ES)-I.E. LOW
0019 2015           14             JR    NZ,EXIT         ; AND EXIT IF 1 OR MORE ARE
001B DDCB017E       15             BIT   7,(IX+1)        ; IS START BIT ACTIVE-I.E. HIGH?
001F 280F           16             JR    Z,EXIT          ; BRANCH IF NOT
0021 DD360280       17             LD    (IX+2),80H      ; ELSE SET RUN BIT AND CLEAR STOP BIT
0025 C33000'        18             JP    EXIT

0028'FE7F           20     RUNNG   CP    7FH             ; TEST FOR ACTIVE HALT SWITCH(ES)-I.E. LOW
002A 2804           21             JR    Z,EXIT          ; AND EXIT IF ALL ARE INACTIVE
002C  DD360240      22             LD    (IX+2),40H      ; ELSE CLEAR RUN BIT AND SET STOP BIT

0030'00             24     EXIT    NOP
                                    .
                                    .
                                    .
                                    .
                                    .
                                    .
```

19" RACK MOUNTING HOLE DIMENSIONS

Figure 9



ORDERING INFORMATION

Designator	Description	Part No.
DIOP	Digital I/O Bus Peripheral with Technical Manual	MK77673
DIOP Technical Manual	DIOP Technical Manual only	4420242

MDX-PIO

FEATURES

- □ STD-Z80 Bus compatible
- □ Four 8-bit I/O ports with two handshake lines per port
- □ All I/O lines fully buffered
- □ I/O lines TTL-compatible with provisions for termination resistor networks
- □ Jumper options for inverted or non-inverted handshake and Output data buffers drive
- □ Two 8-bit ports capable of true Bidirectional I/O
- □ Programmable In only, Out only, or Bidirectional modes
- □ Interrupt-driven programmability
- □ 2.5 MHz or 4.0 MHz options

MDX-PIO DESCRIPTION

The module has four independent 8-bit I/O ports with two handshake (data transfer) control lines per port. Two of the 8-bit ports are capable of true Bidirectional I/O. All port lines are brought to two 26 pin connectors, two ports per connector.

ELECTRICAL SPECIFICATIONS

BUS SPECIFICATION

STD-Z80 compatible

SYSTEM INTERRUPT UNITS

2 total; one for each channel of the MDX-PIO.

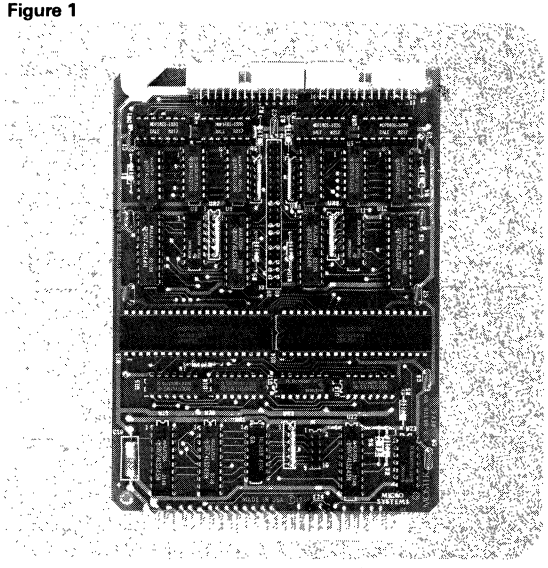
SYSTEM CLOCK

	MIN	MAX
MDX-PIO	500 kHz	2.5 MHz
MDX-PIO-4	500 kHz	4.0 MHz

PARALLEL BUS INTERFACE-STD BUS COMPATIBLE

INPUTS one 74 LS load max.

MDX-PIO
Figure 1



BUS OUTPUTS I_{OH} = -3 mA min at 2.4 Volts
I_{OL} = 24 mA min at 0.5 Volts

TERMINATOR

One 14-pin socket is provided per port for resistor termination (DIP packages) for the data lines. The parallel termination is provided for the 8-bit port data lines and the input strobe (/STB) handshake line. The MDX-PIO is shipped with 1K ohm pullup terminators. In addition to the parallel termination resistors, the ready (RDY) handshake output line is series terminated with a 47 ohm resistor. The series termination reduces any reflections on that line.

I/O CAPACITY

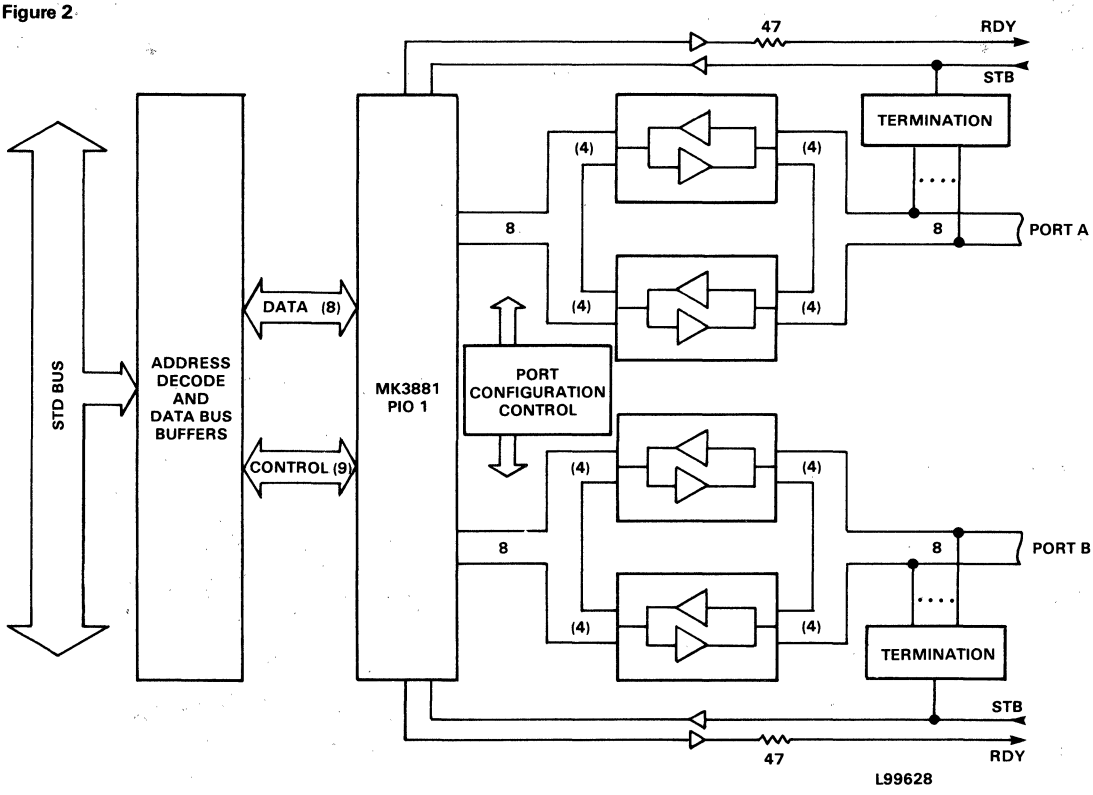
The MDX-PIO uses 8 of the possible 256 port addresses, leaving 248 port addresses available for expansion by the user.

I/O ADDRESSING

Each of the ports has two addresses, one for CONTROL and one for DATA. The port addresses are derived from the

BLOCK DIAGRAM OF MDX-PIO

Figure 2



lowest 8-address lines (A0-A7). A0 and A1 are fed directly to the PIO to select either control or data (A0) and port A or B (A1). The rest of the addresses, A2-A7 are selectably decoded to determine the address which provides the chip enable (CE) for the PIO. This CE function, with A0 and A1, create the proper address for each port.

I/O TRANSCEIVERS

The following line transceivers and terminations are compatible with the I/O driver sockets on the MDX-PIO.

SIGNALS	TYPE	OUTPUT	SINK CURRENT (mA)
Address, Data Bus & Control	74LS245	Non-Inverting Tri-state Bidirectional	24
I/O ports 1A and 2A	*74LS244	Non-inverting Tri-state Bidirectional	24
	74LS241	Inverting Tri-state Bidirectional	24
I/O ports 1B and 2B	*74LS243	Non-inverting Tri-state Bidirectional	24
	74LS242	Inverting Tri-state Bidirectional	24
Handshake	74LS86	Inverting or non-inverting (strap selectable)	8

*These TTL devices are shipped with the board. The devices may be exchanged with the other units listed to provide the alternate signal polarity.

OPERATING TEMPERATURE

0 Deg. C to 60 Deg. C

POWER SUPPLY REQUIREMENTS

+5 Volts ± 5% at 1.1 A max

MECHANICAL SPECIFICATIONS

CARD DIMENSIONS

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm.) long
0.675 in. (1.71 cm.) maximum profile thickness
0.062 in. (0.16 cm.) printed circuit board thickness

STD BUS EDGE CONNECTOR

56 pin dual readout; 0.125 in. centers

Mating connectors:

PCB - VIKING 3VH28/1CE5
WIREWRAP - VIKING 3VH28/1CND5
SOLDER LUG - VIKING 3VH28/1CN5

PARALLEL I/O CONNECTORS

26 pin dual 0.100 in. headers

Mating connectors:

Flat ribbon: ANSLEY 609-2600M

Discrete wires: WINCHESTER PGB13A (housing)
WINCHESTER 100-72020S (contacts 20-24 AWG)
WINCHESTER 100-72026S (contacts 26-30 AWG)

HANDSHAKE LINE POLARITY

Jumper options (J3) are provided on board to control the polarity or "sense" of each handshake signal independently to aid in the interfacing between the board and peripheral devices. See Figure 3.

HANDSHAKE LINE POLARITY AS SHIPPED

Data Line	Polarity of Buffer
ARDY (#1)	inverting
ASTB (#1)	inverting
BRDY (#1)	inverting
BSTB (#1)	non-inverting
ARDY (#2)	non-inverting
ASTB (#2)	non-inverting
BRDY (#2)	non-inverting
BSTB (#2)	non-inverting

DATA BUFFERS

Port A Data Buffers

Port A data lines are buffered using two quad-party-line non-inverting transceivers (74LS244). This allows true Bidirectional capability. Jumper options provide fixed IN, fixed OUT, and BIDIRECTIONAL under software control. Replacing the 74LS244 (U7, 9, 10, 12) with a 74LS240 changes the polarity of the Data bits. The drivers and receivers are enabled by jumpers on the option header J3 (Figure 6).

Port B Data Buffers

Port B data lines are arranged in such a fashion as to allow the user to determine the port direction, in groups of 4-bit sections. Again the buffers are socketed to allow polarity change by population of the sockets U1, 2, 3, 4, 5, 6. The types of devices are listed below:

Port B Buffer Options

Inverting	Non-inverting
74LS242	74LS243 (as shipped)

IVC

CONNECTORS AND OPTION HEADERS

For locations of all connectors and option headers, see Figure 5.

J1 and J2 Connectors

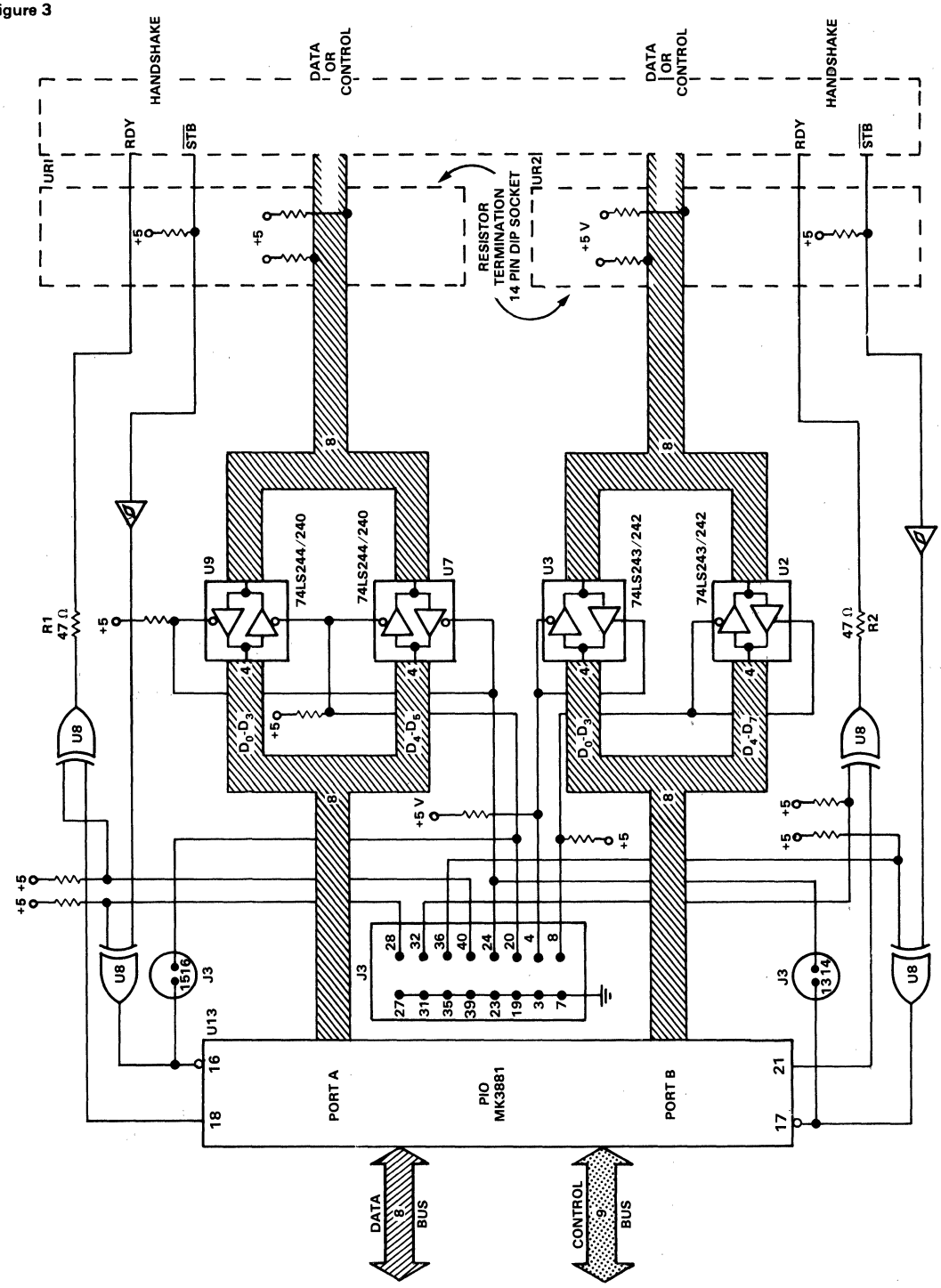
The two 26-pin header connectors are identified as parallel I/O 1 (J1) and Parallel I/O 2 (J2). Sixteen data lines are separated from two control lines on each end of the connector by two ground lines.

J1 and J2 Connector Pinout

Pin	Description	Pin	Description
1	ARDY	14	GND
2	/ASTB	15	GND
3	A7	16	A6
4	A5	17	A4
5	A3	18	A2
6	A1	19	A0
7	B0	20	B1
8	B2	21	B3
9	B4	22	B5
10	B6	23	B7
11	/BSTB	24	GND
12	BRDY	25	GND
13	N/C	26	N/C

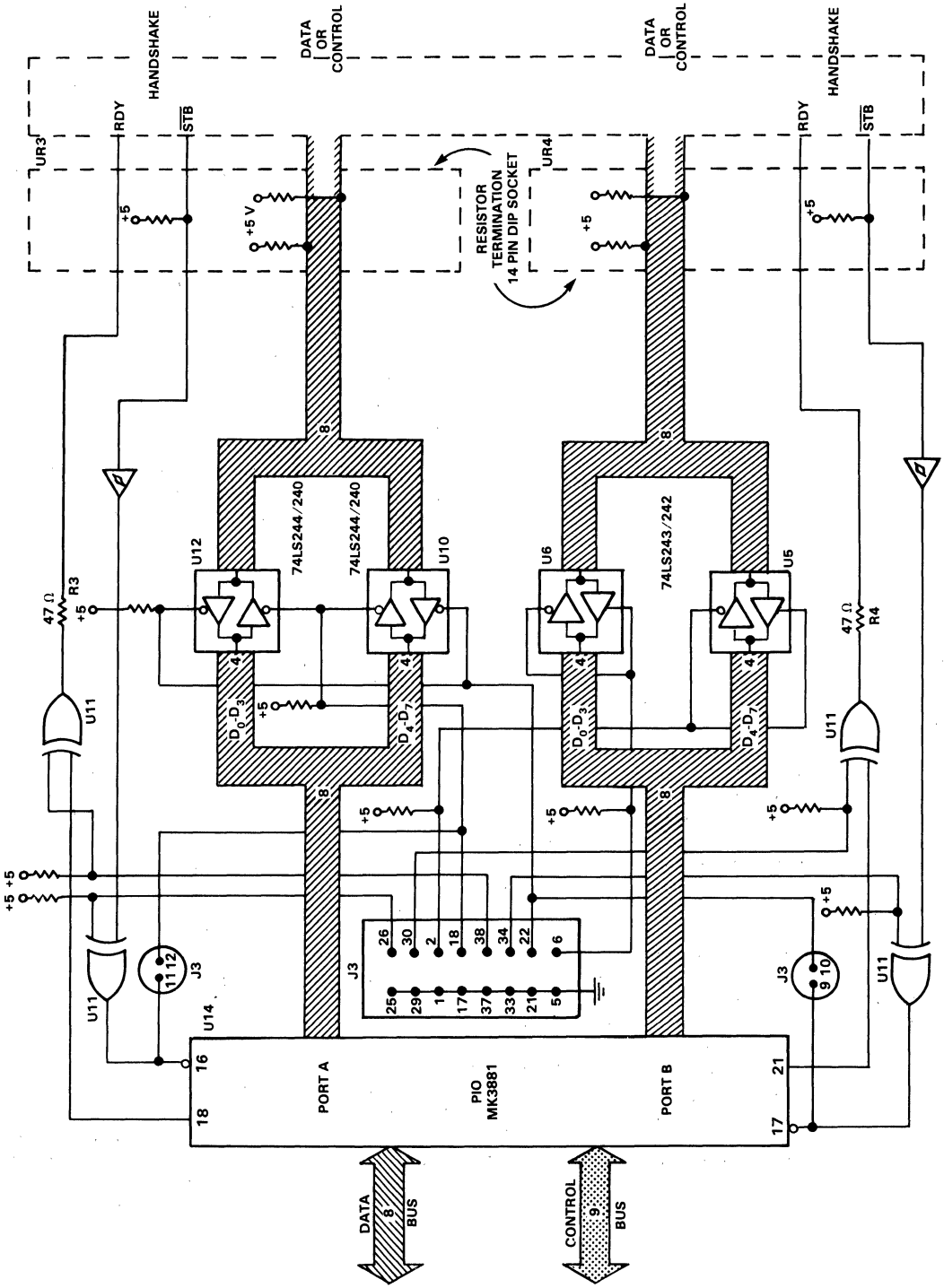
PIO #1 WORK SHEET

Figure 3



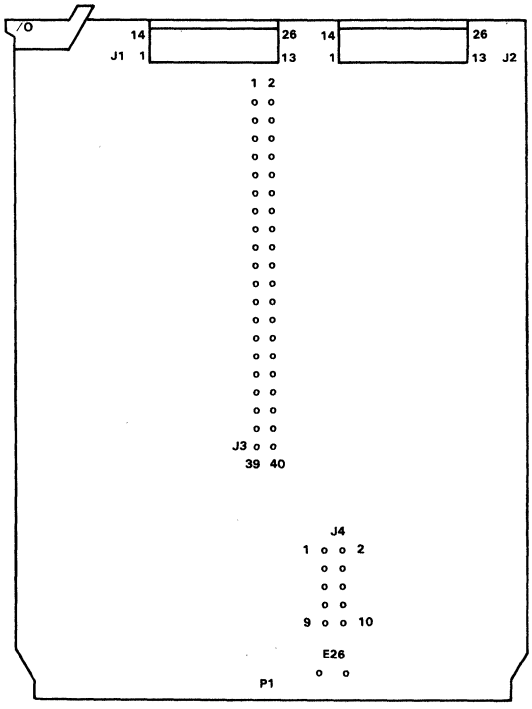
PIO #2 WORK SHEET

Figure 4



JUMPER AND OPTION LOCATIONS

Figure 5



J3 Option Header

The jumper options of header J3 determine handshake polarity, port B control lines of the buffers to determine receiver or driver operation in 4-bit groups, and J3 is also used to enable the receiver or driver portions of the port A buffer (All bits are selected the same). The jumpers on J3 are arranged in groups as defined by Figure 6, also see Figures 3 and 4.

The first four jumper options control the direction of port B of I/O #1 and I/O #2. The ports are divided into two 4-bit groups. The first jumper option, 1-2 on J3, controls whether I/O #2 port B bits 4-7 are input or output. No strap directs the buffer device, U5, to be an INPUT, whereas a strap makes bits 4-7 outputs. The jumper from 5-7 of J3 controls bits 0-3 of the same device. Again no strap directs the buffers inward for an INPUT and a strap makes the four bits an OUTPUT. Jumpers 3-4 and 7-8 control the direction for I/O #1. Option jumper 3-4 control bits 0-3 and option pins 7-8 controls bits 4-7 of the I/O #1. No straps make them INPUT, whereas straps make them OUTPUTS.

(J3) PINS	JUMPER	COMMENT
1-2	IN	I/O #2 Port B bits 4-7 Outputs
	OUT	I/O #2 Port B bits 4-7 Inputs
5-6	IN	I/O #2 Port B bits 0-3 Outputs
	OUT	I/O #2 Port B bits 0-3 Inputs
3-4	IN	I/O #1 Port B bits 0-3 Outputs
	OUT	I/O #1 Port B bits 0-3 Inputs
7-8	IN	I/O #1 Port B bits 4-7 Outputs
	OUT	I/O #1 Port B bits 4-7 Inputs

Option header jumpers 9-10 and 11-12, (/BSTB signal and /ASTB signal of I/O #2) and the option pins 13-14 and 15-16, (/BSTB and /ASTB signals of I/O #1), control the bidirectional capability of port A of each PIO. A jumper installed makes the port BIDIRECTIONAL. The direction of the ports follow the STB inputs. When the peripheral sends the ASTB signal it changes the direction and the BSTB signal changes the direction back. If the Bidirectional mode for I/O #2 port A is required then Jumpers 17-18, and 21-22 must not be strapped. Likewise if I/O #1 port A is Bidirectional then options 19-20, and 23-24 must not be strapped.

(J3) PINS	JUMPER	COMMENTS
9-10 and 11-12	IN	Makes Port A of I/O #2 BIDIRECTIONAL Jumpers 17-18 and 21-22 must be OUT
9-10 and 11-12	OUT	NOT BIDIRECTIONAL
13-14 and 15-16	IN	Makes Port A of I/O #1 BIDIRECTIONAL Jumpers 19-20 and 23-25 must be OUT
13-14 and 15-16	OUT	NOT BIDIRECTIONAL

The jumpers, 17-18 and 21-22, control the direction of port A of the I/O #2. With 17-18 strapped and 21-22 not strapped, port A of I/O #2, will be configured for OUTPUT mode. Jumper 21-22 strapped and 17-18 open configures the A port as INPUT mode. Both jumpers must be open if the port is to be configured in the BIDIRECTIONAL mode.

(J3) PINS	JUMPER	COMMENTS
17-18	IN	Port A of I/O #2 OUTPUT mode
21-22	OUT	
17-18	OUT	Port A of I/O #2 INPUT mode
21-22	IN	

The pins that control the direction of port A of I/O #1 are 19-20 and 23-24. A strap on pins 19-20 and no strap on 23-24 configures the port as OUTPUT. Whereas pins 19-20 open and 23-24 strapped will configure port A of I/O #1 as INPUT. Again, both jumpers 19-20 and 23-24 must be open to be configured as BIDIRECTIONAL mode.

(J3) PINS	JUMPER	COMMENTS
19-20	IN	Port A of I/O #1 OUTPUT mode
23-24	OUT	
19-20	OUT	Port A of I/O #1 INPUT mode
23-24	IN	

The remaining jumpers determine the polarity of the STB and RDY lines that the two I/O devices #1 and #2 receive from the peripherals. No strap installed on pins 25-26 will invert the /ASTB signal received by I/O #2, where a strap will not invert the STB. Pins 27-28 will invert or not invert the /ASTB of I/O #1. Again a strap doesn't invert and an open does invert the STB from the peripheral device for the I/O #1 device. The controls for the /BSTB of I/O #1 and #2 are jumpers 33-34 and 35-36. As before the strap makes the STB signal non-inverted and an open inverts the STB signal received from the peripheral.

(J3) PINS	JUMPER	COMMENTS
25-26	IN	Non-inverted /ASTB of I/O #2
	OUT	Inverted /ASTB of I/O #2
27-28	IN	Non-inverted /ASTB of I/O #1
	OUT	Inverted /ASTB of I/O #1
33-34	IN	Non-inverted /BSTB of I/O #1
	OUT	Inverted /BSTB of I/O #1
35-36	IN	Non-inverted /BSTB of I/O #2
	OUT	Inverted /BSTB of I/O #2

The next pins 29-30 and 31-32 determine the polarity of the handshake signals the peripheral device receives from port B of the I/O devices #1 and #2, the RDY signals. Pins 29-30 control the polarity of BRDY (port B) of I/O #2. No strap inverts the RDY signal delivered to the peripheral device and a strap delivers a non-inverted signal to the peripheral. Pins 31-32 control the BRDY of I/O #1. The last four pins control the RDY signal of port A of I/O #1 and #2. Pins 37-38 determine the polarity of ARDY for I/O #2 and pins 39-40 control ARDY for I/O #1. Again a strap is the non-inverted mode and no straps is the inverted condition for the RDY signal from port B of the I/ O #1.

(J3) PINS	JUMPER	COMMENTS
29-30	IN	Non-inverted BRDY of I/O #2
	OUT	Inverted BRDY of I/O #2
31-32	IN	Non-inverted BRDY of I/O #1
	OUT	Inverted BRDY of I/O #1
37-38	IN	Non-inverted ARDY of I/O #2
	OUT	Inverted ARDY of I/O #2
39-40	IN	Non-inverted ARDY of I/ O #1
	OUT	Inverted ARDY of I/O #1

J4 PORT ADDRESSING JUMPERS

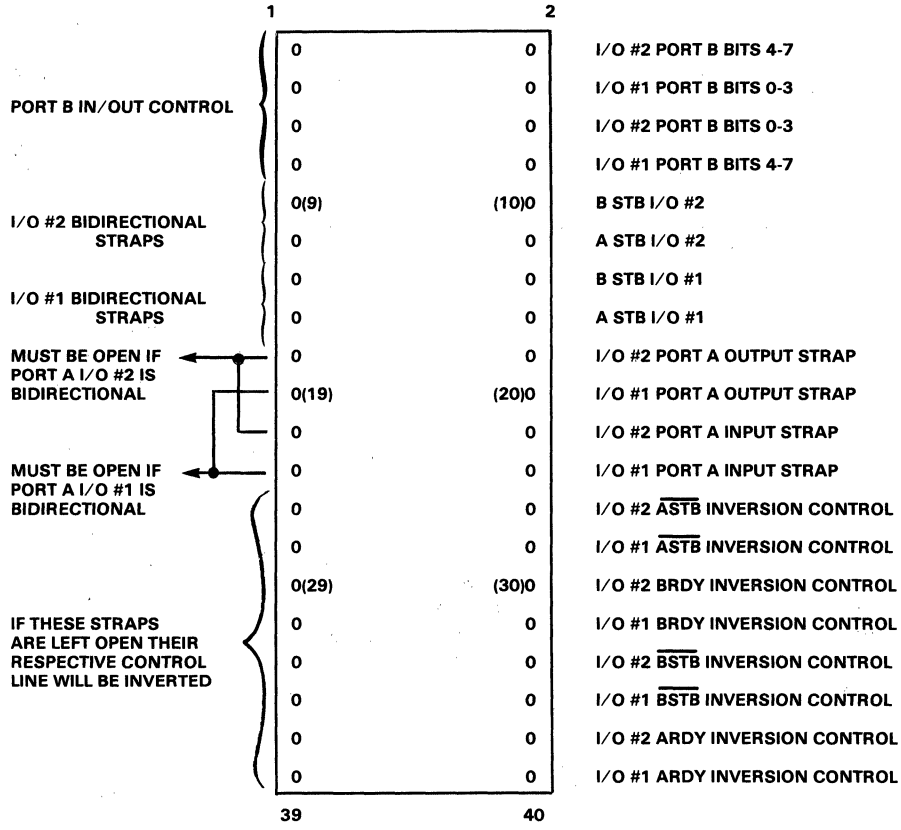
The upper five bits of the I/O channel address are determined by the strapping on J4. These bits are jumper selectable on the MDX-PIO board in order to provide address selectable ports. Both ports share the address and data bus buffer circuitry. The only differences are in the port address decoding, and PIO #2 is lower priority in the daisy chain interrupt structure.

	PIO 1 (U13)				PIO 2 (U14)			
	PORT A		PORT B		PORT A		PORT B	
Data	XXXX	X000	XXXX	X010	XXXX	X100	XXXX	X110
Control	XXXX	X001	XXXX	X011	XXXX	X101	XXXX	X111

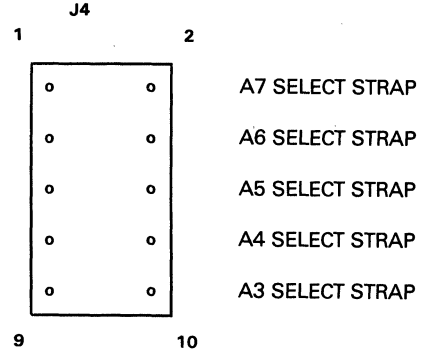
The XXXX X symbols stand for the upper 5 bits of the I/O channel address determined by the J4 jumpers.

J3 OPTION HEADER

Figure 6



J4 PORT ADDRESS JUMPER HEADER



NOTE
Leaving the strap open selects the address bit to be a "1"

PORT ADDRESSING AS SHIPPED

Addresses for the MDX-PIO as shipped are summarized below:

	PIO #1		PIO #2	
	Port A	Port B	Port A	Port B
Data	F8H (ex)	FAH	FCH	FEH
Control	F9H	FBH	FDH	FFH

J4

o o >------- A7 = > 1
o o >------- A6 = > 1
o o >------- A5 = > 1
o o >------- A4 = > 1
o o >------- A3 = > 1

	PORT A		
Data	1111	1000	= > F8H
Control	1111	1001	= > F9H

E26 - DMA DAISY CHAIN

The E26 option is to allow multiple DMA device users to continue the DMA daisy chain if the MDX-PIO was to break the daisy chain. Mostek doesn't use this option to date.

P1 STD-Z80 BUS

Pin definition is as shown in Figure 4. See STD-Z80 Bus description for signal functions.

P1 PIN DEFINITION

Figure 7

SIGNAL	PIN	PIN	SIGNAL
+5 V	1	2	+5 V
GND	3	4	GND
-5 V	5	6	-5 V
D3	7	8	D7
D2	9	10	D6
D1	11	12	D5
D0	13	14	D4
A7	15	16	A15
A6	17	18	A14
A5	19	20	A13
A4	21	22	A12
A3	23	24	A11
A2	25	26	A10
A1	27	28	A9
A0	29	30	A8
/WR	31	32	/RD
/IORQ	33	34	/MEMRQ
/IOEXP	35	36	/MEMEX
/REFRESH	37	38	/MCSYNC
/STATUS 1	39	40	/STATUS 0
/BUSAK	41	42	/BUSRQ
/INTAK	43	44	/INTRQ
/WAITRQ	45	46	/NMIRQ
/SYSRESET	47	48	/PBRESET
/CLOCK	49	50	/CNTRL
PCO	51	52	PCI
AUX GND	53	54	AUX GND
+12 V	55	56	-12 V

THE "/" MEANS A LOW ACTIVE SIGNAL.

INTERRUPT SERVICING

If more than one peripheral chip requests interrupt servicing at the same time, a priority status is established. Priority is determined by the interrupt enable lines - IEI and IEO - and the internal logic on each peripheral chip. The interrupt priority status is defined:

IEI	IEO	STATUS
0	0	higher priority interrupt being requested
0	1	undefined (Not allowed)
1	0	requesting interrupt, highest priority
1	1	no interrupt

For more information on the modes of interrupt (Mode 1, 2 and 3) provided by the MDX-PIO module refer to the MK3881 TECHNICAL MANUAL Pub. No. 78506, and the STD-Z80 SYSTEM DESIGN GUIDE Pub. No. MK79646.

DAISY CHAIN

Daisy chain priority interrupt logic automatically supplies the programmed vector (from the highest priority interrupting peripheral) to the CPU during interrupt acknowledge. Board priority is determined as an individual peripheral chip; i.e. through the high or low state of PCI or PCO. (Figure 7)

APPENDIX A

PARALLEL PRINTER CONFIGURATION

A standard parallel printer can be interfaced to the MDX-PIO to run with Mostek provided operating systems. The I/O port address is D0H, D3H (I/O #1), for operating systems FLP-80 DOS and M/OS-80.

Install jumpers:

```
(J3)  3-4      ;Buffer direction option header
      19-20

(J4)  5-6      ;Address option header
      9-10
```

Install IC 74LS242 in socket U2 (shipped as 74LS243).

PPG 8/16 PROM PROGRAMMER CONFIGURATION

The Mostek PPG 8/16 PROM PROGRAMMER can be interfaced to an MDX system with the use of an MDX-PIO module. The PPG software expects the PIO to be strapped at D0H and uses the addresses D4-D7H (I/O #2).

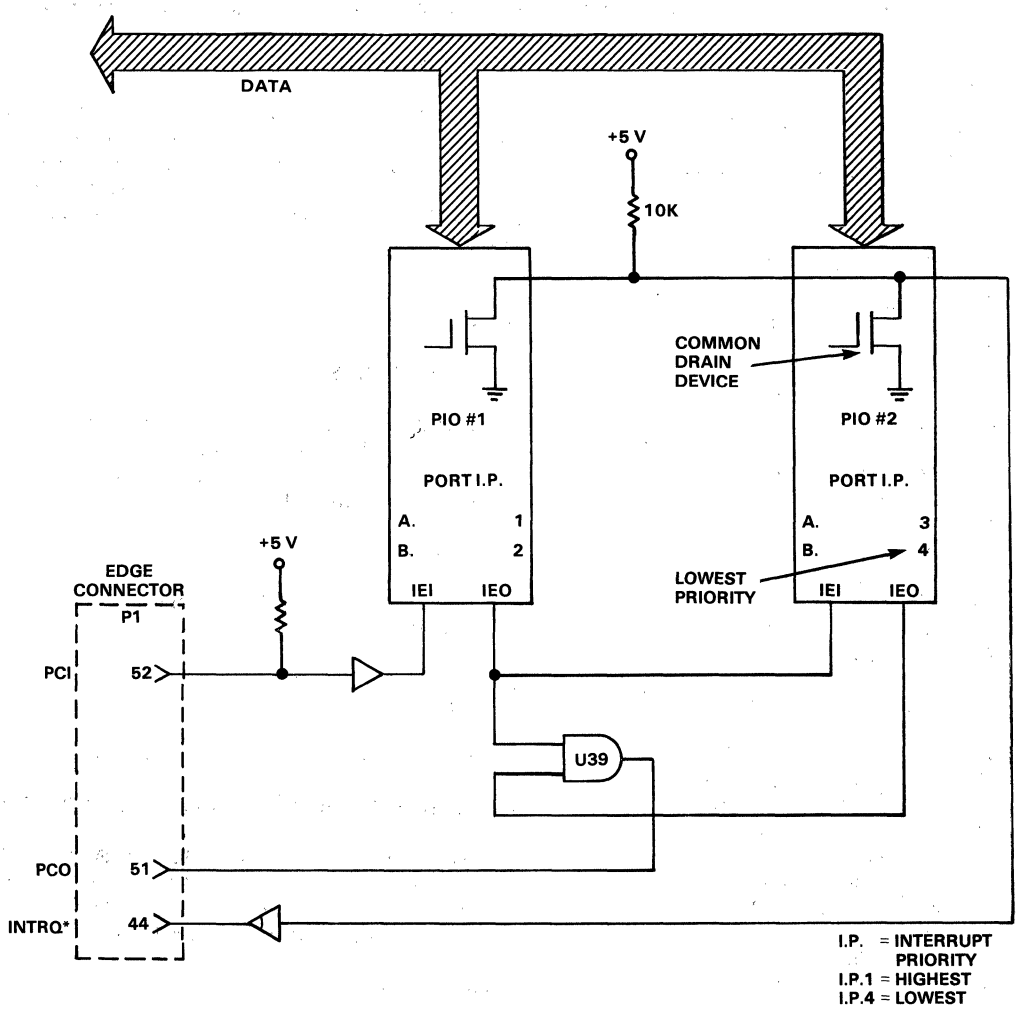
Install jumpers:

```
(J3)  1-2      ;J3 option header
      5-6
      9-10
      11-12
      25-26
      33-34

(J4)  5-6      ;Same address as printer
      9-10     ;Address option header
```

Remove IC UR3 and UR4 (1K resistor packages).

PRIORITY INT STRUCTURE

Figure 8



ORDERING INFORMATION

Designator	Description	Part Number
MDX-PIO	MDX-PIO Module with Technical Manual	MK77650
MDX-PIO Technical Manual	MDX-PIO Technical Manual only	4420030

1983 COMPUTER PRODUCTS DATA BOOK

MDX-DRAM

FEATURES

- STD-Z80 BUS compatible
- Two memory sizes:
  16K x 8 (MDX-DRAM16)
  32K x 8 (MDX-DRAM32)
- Selectable addressing on 4K boundaries
- 4 MHz version available (MDX-DRAM-4)

GENERAL DESCRIPTION

The MDX-DRAM is designed to be a RAM memory expansion board for the Mostek MD Series of Z80-based microcomputers. It is available in two memory capacities, 16K bytes (MDX-DRAM16) and 32K bytes (MDX-DRAM32A). The MDX-DRAM16 and the MDX-DRAM32A are available in both 2.5 MHz and 4 MHz versions. Thus, the designer can choose from the various options to add-on dynamic RAM memory to satisfy system requirements.

The MDX-DRAM block diagram, with the major functions of the MDX-DRAM, is shown in Figure 2. The MDX-DRAM provides a low cost way to expand RAM for the MDX system.

Memory Array

The memory array consists of either 8 or 16 MK4108 or MK4116 Dynamic Memories. The RAMs are organized into two banks of eight RAMs each. The eight RAMs of each bank contribute one byte to an addressable location. The total storage capacity of the MDX-DRAM is 32,768 bytes.

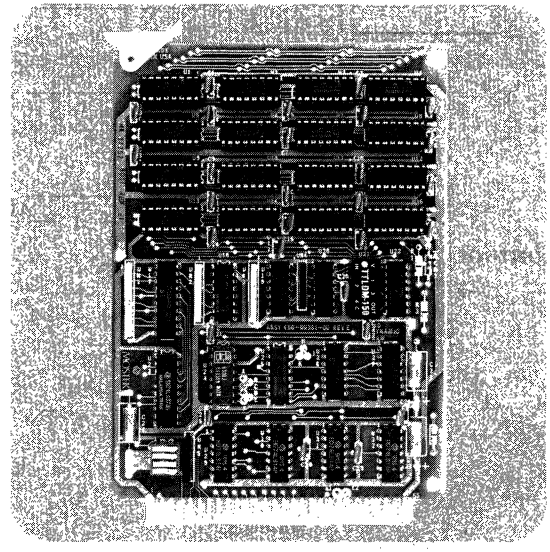
Memory Decode and Control

The memory decode and control section is responsible for generating the necessary timing signals of the memory array, mux, and data buffer. Timing within the memory decode and control section is generated by a TTL buffered delay line.

Address Multiplexer (MUX)

The address multiplexer is responsible for taking the address bits from the address buffers and converting them into a row and column address for the memory array. The address multiplexer is controlled by the memory decode and control section.

MDX-DRAM
Figure 1



Data Buffer

The data buffer isolates the memory array from the data bus and is controlled by the memory decode and control section.

Memory Device Selection Jumpers

Table 1 shows how jumpers A-K are configured for the different MDX-DRAM boards.

Memory Decoding

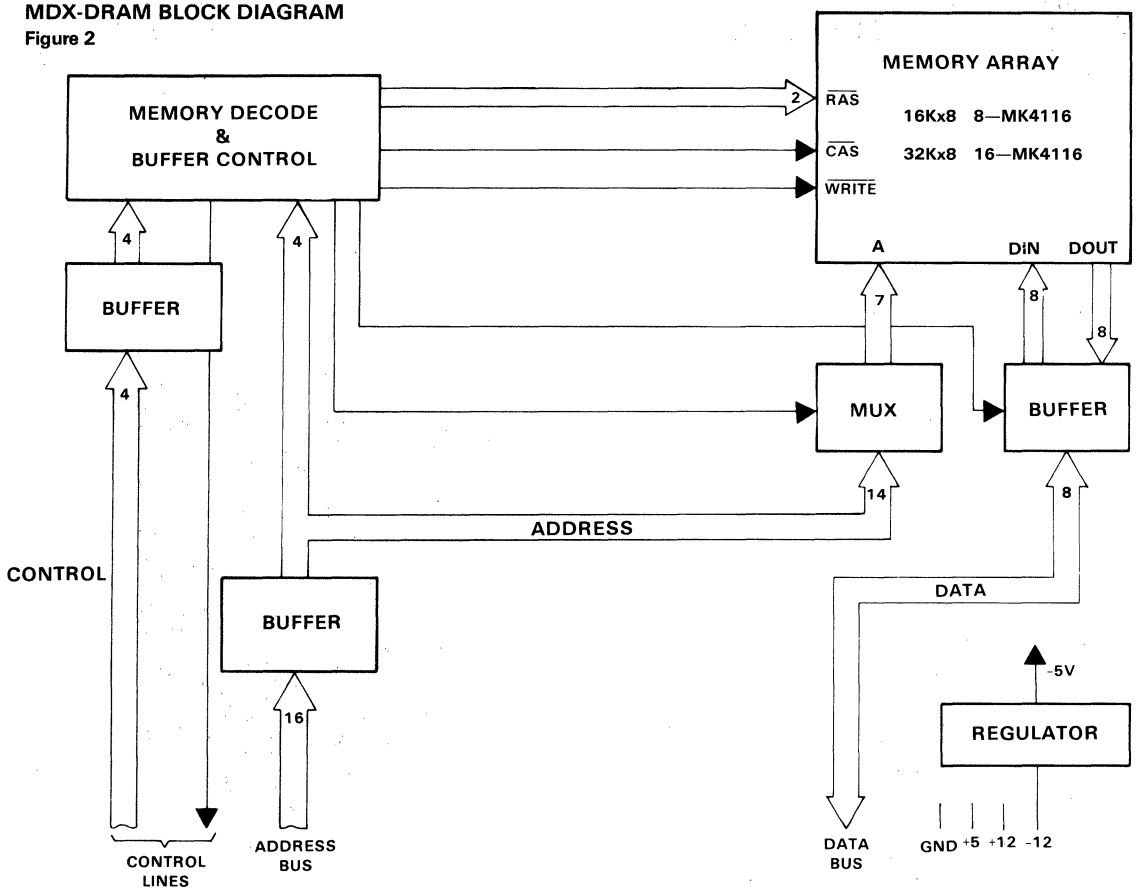
Memory decoding for the MDX-DRAM is on 4K boundaries, 0000H, 1000H, 2000H, and so on. The starting address for the MDX-DRAM is selected by a four-position DIP switch located in U28. Table 2 shows the switch setting for U28 versus starting address.

NOTE: The address select switch only sets the starting address for the memory board. If, for example, an MDX-DRAM32 board is positioned to start at F000H, the remaining 28K of memory will "roll over" at 0000H and continue up to 6FFFH.

IVD

MDX-DRAM BLOCK DIAGRAM

Figure 2



JUMPER CONFIGURATIONS

Table 1

BOARD	JUMPERS	
MDX-DRAM16	B to C H to J	
MDX-DRAM32 (U24 = MK6268)	B to C E to F H to J	
MDX-DRAM32-4 (U24 = MK6268)	B to C E to F H to J	
MDX-DRAM32A (U24 = MK6280)	A to B D to E H to J	Will notch out E000 to EFFFH when board is addressed at 8000H. Will be contiguous memory when addressed at 0000H.
MDX-DRAM32A-4 (U24 = MK6280)	A to B D to E H to J	Same as above

MK6280
PROM PATTERN
(MMI 6300-1J 256X4)

LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA
00	F	20	F	40	F	60	F	80	3	A0	3	C0	C	E0	C
01	F	21	F	41	F	61	F	81	7	A1	7	C1	D	E1	D
02	F	22	F	42	F	62	3	82	3	A2	C	C2	C	E2	F
03	F	23	F	43	F	63	3	83	3	A3	C	C3	C	E3	F
04	F	24	F	44	3	64	3	84	C	A4	C	C4	F	E4	F
05	F	25	F	45	3	65	3	85	C	A5	C	C5	F	E5	F
06	F	26	3	46	3	66	C	86	C	A6	F	C6	F	E6	F
07	F	27	3	47	3	67	C	87	C	A7	F	C7	F	E7	F
08	3	28	3	48	C	68	C	88	F	A8	F	C8	F	E8	F
09	3	29	3	49	C	69	C	89	F	A9	F	C9	F	E9	F
0A	3	2A	C	4A	C	6A	F	8A	F	AA	F	CA	F	EA	3
0B	F	2B	C	4B	C	6B	F	8B	F	AB	F	CB	F	EB	3
0C	C	2C	C	4C	F	6C	F	8C	F	AC	F	CC	3	EC	3
0D	C	2D	C	4D	F	6D	F	8D	F	AD	F	CD	3	ED	3
0E	C	2E	F	4E	F	6E	F	8E	F	AE	3	CE	3	EE	C
0F	C	2F	F	4F	F	6F	F	8F	F	AF	3	CF	3	EF	C
10	F	30	F	50	F	70	F	90	3	B0	3	D0	C	F0	C
11	F	31	F	51	F	71	7	91	7	B1	D	D1	D	F1	F
12	F	32	F	52	F	72	3	92	3	B2	C	D2	C	F2	F
13	F	33	F	53	3	73	3	93	C	B3	C	D3	F	F3	F
14	F	34	F	54	3	74	3	94	C	B4	C	D4	F	F4	F
15	F	35	3	55	3	75	C	95	C	B5	F	D5	F	F5	F
16	F	36	3	56	3	76	C	96	C	B6	F	D6	F	F6	F
17	3	37	3	57	C	77	C	97	B	B7	F	D7	F	F7	F
18	3	38	3	58	C	78	C	98	7	B8	F	D8	F	F8	F
19	3	39	C	59	C	79	F	99	7	B9	F	D9	F	F9	3
1A	3	3A	C	5A	C	7A	F	9A	7	BA	F	DA	F	FA	3
1B	C	3B	C	5B	F	7B	F	9B	7	BB	F	DB	3	FB	3
1C	C	3C	C	5C	F	7C	F	9C	F	BC	F	DC	3	FC	F
1D	C	3D	F	5D	F	7D	F	9D	F	BD	3	DD	3	FD	C
1E	C	3E	F	5E	F	7E	F	9E	F	BE	3	DE	3	FE	C
1F	F	3F	F	5F	F	7F	F	9F	3	BF	3	DF	C	FF	C

MK6268
PROM PATTERN
(MMI 6300-1J 256X4)

LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA
00	F	20	F	40	F	60	F	80	7	A0	7	C0	9	E0	C
01	F	21	F	41	F	61	F	81	7	A1	7	C1	9	E1	C
02	F	22	F	42	F	62	7	82	7	A2	9	C2	C	E2	F
03	F	23	F	43	F	63	7	83	7	A3	9	C3	C	E3	F
04	F	24	F	44	7	64	7	84	9	A4	C	C4	F	E4	F
05	F	25	F	45	7	65	7	85	9	A5	C	C5	F	E5	F
06	F	26	7	46	7	66	9	86	C	A6	F	C6	F	E6	F
07	F	27	7	47	7	67	9	87	C	A7	F	C7	F	E7	F
08	7	28	7	48	9	68	C	88	F	A8	F	C8	F	E8	F
09	7	29	7	49	9	69	C	89	F	A9	F	C9	F	E9	F
0A	7	2A	9	4A	C	6A	F	8A	F	AA	F	CA	F	EA	7
0B	7	2B	9	4B	C	6B	F	8B	F	AB	F	CB	F	EB	7
0C	9	2C	C	4C	F	6C	F	8C	F	AC	F	CC	7	EC	7
0D	9	2D	C	4D	F	6D	F	8D	F	AD	F	CD	7	ED	7
0E	C	2E	F	4E	F	6E	F	8E	F	AE	7	CE	7	EE	9
0F	C	2F	F	4F	F	6F	F	8F	F	AF	7	CF	7	EF	9
10	F	30	F	50	F	70	F	90	7	B0	7	D0	9	F0	C
11	F	31	F	51	F	71	7	91	7	B1	9	D1	C	F1	F
12	F	32	F	52	F	72	7	92	7	B2	9	D2	C	F2	F
13	F	33	F	53	7	73	7	93	9	B3	C	D3	F	F3	F
14	F	34	F	54	7	74	7	94	9	B4	C	D4	F	F4	F
15	F	35	7	55	7	75	9	95	C	B5	F	D5	F	F5	F
16	F	36	7	56	7	76	9	96	C	B6	F	D6	F	F6	F
17	7	37	7	57	9	77	C	97	F	B7	F	D7	F	F7	F
18	7	38	7	58	9	78	C	98	F	B8	F	D8	F	F8	F
19	7	39	9	59	C	79	F	99	F	B9	F	D9	F	F9	7
1A	7	3A	9	5A	C	7A	F	9A	F	BA	F	DA	F	FA	7
1B	9	3B	C	5B	F	7B	F	9B	F	BB	F	DB	7	FB	7
1C	9	3C	C	5C	F	7C	F	9C	F	BC	F	DC	7	FC	7
1D	C	3D	F	5D	F	7D	F	9D	F	BD	7	DD	7	FD	9
1E	C	3E	F	5E	F	7E	F	9E	F	BE	7	DE	7	FE	9
1F	F	3F	F	5F	F	7F	F	9F	7	BF	7	DF	9	FF	C

MEMORY DECODING

Table 2

STARTING ADDRESS	U28 SWITCH POSITION			
	1	2	3	4
0000	0	0	0	0
1000	0	0	0	1
2000	0	0	1	0
3000	0	0	1	1
4000	0	1	0	0
5000	0	1	0	1
6000	0	1	1	0
7000	0	1	1	1
8000	1	0	0	0
9000	1	0	0	1
A000	1	0	1	0
B000	1	0	1	1
C000	1	1	0	0
D000	1	1	0	1
E000	1	1	1	0
F000	1	1	1	1
0 = Closed		1 = Open		

ELECTRICAL SPECIFICATIONS

Word Size: 8 bits

Memory Size

MDX-DRAM16 - 16,384 bytes
MDX-DRAM32A - 32,768 bytes

Access Times

	SYSTEM CLOCK	MEMORY ACCESS TIMES	MEMORY CYCLE TIMES
MDX-DRAM	2.5 MHz	350 ns max.	465 ns min.
MDX-DRAM-4	4.0 MHz	200 ns max.	325 ns min.

Address Selection

Selection of 16K or 32K contiguous memory blocks to reside on any 4K boundary, 0000H, 1000H, 2000H, 3000H, and so on.

STD Bus Interface

Inputs One 74LS load max.
Outputs I_{OH} = -3 mA min. at 2.4 volts
I_{OL} = 24 mA min. at 0.5 volts

System Clock

	Min	Max
MDX-DRAM	1.25 MHz	2.5 MHz
MDX-DRAM-4	1.25 MHz	4.0 MHz

Power Supply Requirements

+5 V ± 5% at 0.6 A max.
+12 V ± 5% at 0.25 A max.
-12 V ± 5% at 0.03 A max.

Operating Temperature

0 to 60 degrees C

MECHANICAL SPECIFICATIONS

Card Dimensions

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
0.48 in. (1.22 cm) maximum profile thickness
0.062 in. (0.16 cm) printed-circuit-board thickness

Connectors

Function	Configuration	Mating Connector
STD BUS	56-pin dual 0.125-in. centers	Printed Circuit Viking 3VH28/1CE5 Wire wrap Viking 3VH28/1CND5 Solder Lug Viking 3VH28/1CN5

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-DRAM16	16K Bytes (4116's) 2.5 MHz	MK77754-0
MDX-DRAM32A	32K Bytes (4116's) 2.5 MHz	MK77752-0
MDX-DRAM16-4	16K Bytes (4116's) 4.0 MHz	MK77754-4
MDX-DRAM32A-4	32K Bytes (4116's) 4.0 MHz	MK77752-4
MDX-DRAM Technical Manual	MDX-DRAM Technical Manual Only	4420033

MDX-EPROM/UART

FEATURES

- ☐ STD Bus compatible
- ☐ Three 24-pin sockets for 2K x 8 ROM/EPROM device
- ☐ Memory addressing selectable or 2K boundaries
- ☐ Full-duplex UART
  - Start bit verification
  - Data word size variable from 5 to 8 bits
  - One or two stop bits may be selected
  - Odd, even, or no parity option
  - One word buffering on both transmit and receive
  - RS232 and 20 mA interface
  - 110 to 19,200 Baud

GENERAL DESCRIPTION

The MDX-EPROM/UART is a STD BUS-compatible microcomputer module. Designed as a universal EPROM add-on module for the STD BUS, the MDX-EPROM/UART provides the system designer with sockets to contain up to 10K Bytes of EPROM memory (five 2716s) as shown in the Block Diagram, Figure 2. The EPROM memories can be positioned to start on any 2K boundary within a 16K block of memory via a strapping option. Included on-board the MDX-EPROM/UART is a fully buffered asynchronous I/O port with a teletype reader step control. A full-duplex UART is used to receive and transmit data at the serial port. Operation and UART options are under software control. Once the unit has been programmed, no further changes are necessary unless there is a modification of the serial data format.

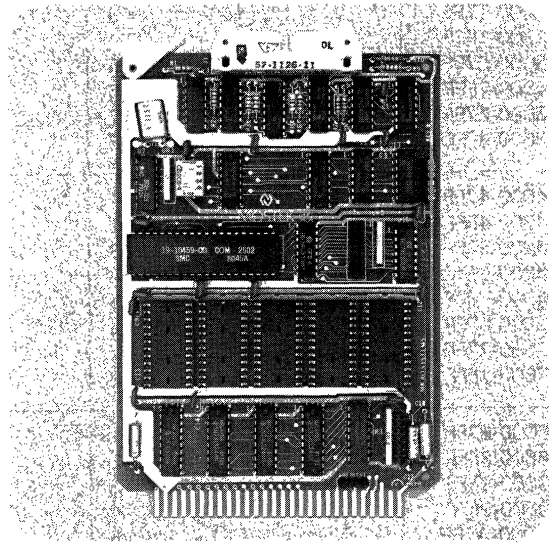
SPECIFICATIONS

Electrical Specifications

STD Bus Compatible

Memory Addressing

MDX-EPROM/UART
Figure 1



ROM/EPROM - 2K blocks jumper selectable for any 2K boundary within a given 16K boundary of the CPU memory map

Memory Speed Required without wait states (Address Access)

2716 (Single +5 V type required) -	515 ns	2.5 MHz
	265 ns	4.0 MHz

I/O Addressing

On-board fully programmable

System Clock

	Min.	Max.
MDX-EPROM/UART	250 kHz	2.5 MHz
MDX-EPROM/UART-4	250 kHz	4.0 MHz

Power Supply Requirements

+ 12 Volts ± 5% at 50 mA max.
- 12 Volts ± 5% at 35 mA max.
+ 5 Volts ± 5% at 1.2 A max.

IVD

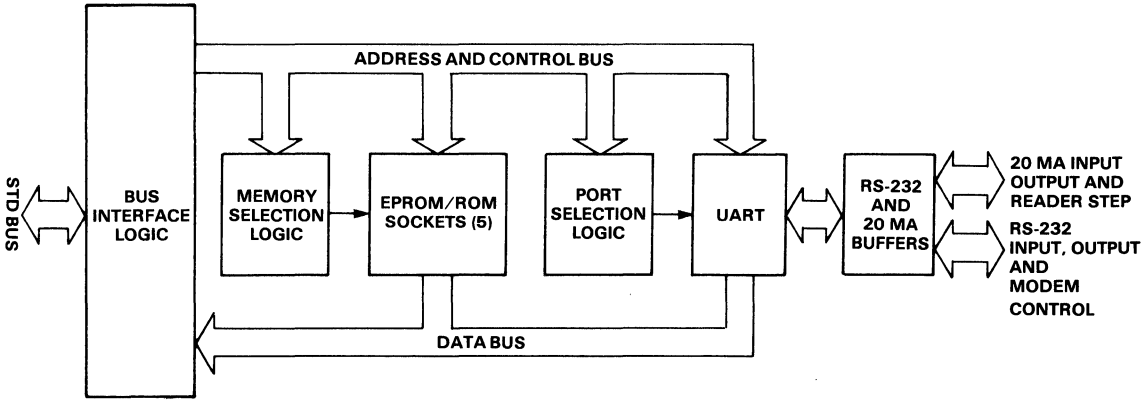
MEMORY DECODING JUMPER SELECTION

Table 1

J2 JUMPERS													JUMPERS E1 - E6
DECODED ADDRESS	EPROM U17			EPROM U18			EPROM U19			EPROM U20			EPROM U21			
	J2			J2			J2			J2			J2			
	Pin	to	Pin	Pin	to	Pin	Pin	to	Pin	Pin	to	Pin	Pin	to	Pin	
0000-07FF	16		1	15		1	14		1	13		1	12		1	
0800-0FFF	"		2	"		2	"		2	"		2	"		2	E1 to E6
1000-17FF	"		3	"		3	"		3	"		3	"		3	and
1800-1FFF	"		4	"		4	"		4	"		4	"		4	E4 to E5
2000-27FF	"		5	"		5	"		5	"		5	"		5	
2800-2FFF	"		6	"		6	"		6	"		6	"		6	
3000-37FF	"		7	"		7	"		7	"		7	"		7	
3800-3FFF	"		8	"		8	"		8	"		8	"		8	
4000-47FF	"		1	"		1	"		1	"		1	"		1	
4800-4FFF	"		2	"		2	"		2	"		2	"		2	E1 to E6
5000-57FF	"		3	"		3	"		3	"		3	"		3	and
5800-5FFF	"		4	"		4	"		4	"		4	"		4	E3 to E5
6000-67FF	"		5	"		5	"		5	"		5	"		5	
6800-6FFF	"		6	"		6	"		6	"		6	"		6	
7000-77FF	"		7	"		7	"		7	"		7	"		7	
7800-7FFF	"		8	"		8	"		8	"		8	"		8	
8000-87FF	"		1	"		1	"		1	"		1	"		1	
8800-8FFF	"		2	"		2	"		2	"		2	"		2	E2 to E6
9000-97FF	"		3	"		3	"		3	"		3	"		3	and
9800-9FFF	"		4	"		4	"		4	"		4	"		4	E4 to E5
A000-A7FF	"		5	"		5	"		5	"		5	"		5	
A800-AFFF	"		6	"		6	"		6	"		6	"		6	
B000-B7FF	"		7	"		7	"		7	"		7	"		7	
B800-BFFF	"		8	"		8	"		8	"		8	"		8	
C000-C7FF	"		1	"		1	"		1	"		1	"		1	
C800-CFFF	"		2	"		2	"		2	"		2	"		2	E2 to E6
D000-D7FF	"		3	"		3	"		3	"		3	"		3	and
D800-DFFF	"		4	"		4	"		4	"		4	"		4	E3 to E5
E000-E7FF	"		5	"		5	"		5	"		5	"		5	
E800-EFFF	"		6	"		6	"		6	"		6	"		6	
F000-F7FF	"		7	"		7	"		7	"		7	"		7	
F800-FFFF	"		8	"		8	"		8	"		8	"		8	

MDX-EPROM/UART BLOCK DIAGRAM

Figure 2



Operating Temperature Range

0 to 60°C

Mechanical Specifications

Card Dimensions

4.5 in. (11.43 cm) high by 6.5 in. (16.51 cm) long
0.48 in. (1.22 cm) maximum profile thickness
0.062 in. (0.16 cm) printed circuit board thickness

Connectors

STD Bus; 56 pin dual, 0.125 in. centers
Mating Connectors
PCB - Viking 3VH28/1CE5
WIREWRAP - Viking 3VH28/1CND5
SOLDER LUG - Viking 3VH28/1CN5

Serial I/O; 26 pin dual, 0.100 in. grid
Mating Connectors
FLAT RIBBON - Ansley 609-2600M
DISCRETE WIRES - Winchester PGB26A (housing)
Winchester 100-70029S (contacts)

UTILIZATION

EPROM Decoding Jumpers

Jumper Options for the EPROM decoding are shown in Table 1.

I/O Port Decoding Jumpers

The port decoding for the EPROM/UART board is jumper programmable to allow multiple EPROM/UART boards within an MDX system. The EPROM/UART board uses three Read/Write ports to interface to the UART. Figure 3 shows the format for strapping the I/O decoder.

IVD

8 BIT I/O ADDRESS DECODING

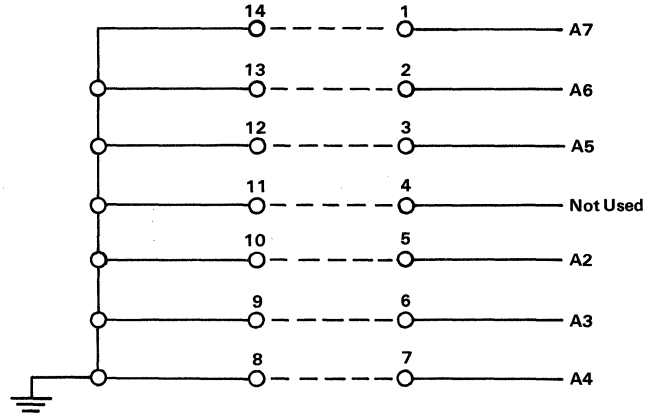
Table 2

I/O PORT ADDRESS BITS								OPERATION PERFORMED	
A7	A6	A5	A4	A3	A2	A1	A0	READ	WRITE
X	X	X	X	X	X	0	0	UART DATA	UART DATA
X	X	X	X	X	X	0	1	UART STATUS	UART CONTROL
X	X	X	X	X	X	1	0	MODEM STATUS	MODEM CONTROL
X	X	X	X	X	X	1	1	NOT USED	NOT USED

X = PROGRAMMABLE

I/O ADDRESS STRAPPING

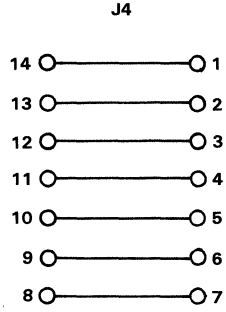
Figure 3



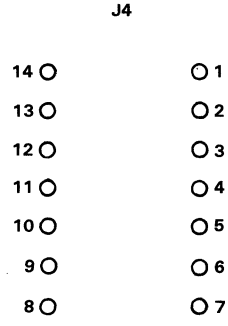
STRAP = LOGIC 0 NO STRAP = LOGIC 1

EXAMPLES:

Strap board so that serial channels occupy I/O ports 0, 1, and 2.



Strap board so that serial channels occupy ports FC, FD, and FE.



Baud Rate Selection

The Baud rate for the serial interface is generated by the Baud rate chip U7. The Baud rate is selected by DIP switch U8. Table 3 shows DIP switch setting versus Baud rates.

Programming the UART

A full-duplex UART is used to receive and transmit data at the serial port. Operation and UART options are under software control. Once the unit has been programmed, no further changes are necessary unless there is a modification of the serial format. Transmit and receive clock rates (Baud clock rate) must be 16 times the desired Baud rate. A programming model for the UART is shown in Figure 4.

BAUD RATE SWITCH SELECTION

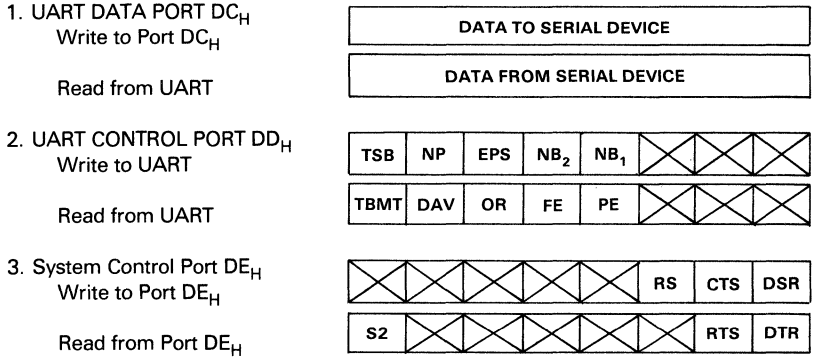
Table 3

U8 SWITCH POSITION				X16 CLOCK	BAUD RATE
4	3	2	1		
0	0	0	0	.8KHz	50
0	0	0	1	1.2	75
0	0	1	0	1.76	110
0	0	1	1	2.152	134.5
0	1	0	0	2.4	150
0	1	0	1	4.8	300
0	1	1	0	9.6	600
0	1	1	1	19.2	1200
1	0	0	0	28.8	1800
1	0	0	1	32.8	2000
1	0	1	0	38.4	2400
1	0	1	1	57.6	3600
1	1	0	0	76.8	4800
1	1	0	1	115.2	7200
1	1	1	0	153.6	9600
1	1	1	1	307.2	19,200

1 = OPEN **0 = CLOSED**

PROGRAMMING THE UART

Figure 4



Number Stop Bits (TSB) — This bit will select the number of stop bits, 1 or 2, to be appended immediately after the parity bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits.

No Parity (NP) — A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit.

Odd/Even Parity Select (EPS) — The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.

Figure 4

Number of Bits/Character (NB_2, NB_1) — These two bits will be internally decoded to select either 5, 6, 7 or 8 data bits, character.

NB_2	NB_1	Bits/Character
0	0	5
0	1	6
1	0	7
1	1	8

Transmitter Buffer Empty (TBMT) — The transmitter buffer empty flag goes to a logic "1" when the data buffer holding register may be loaded with another character.

Data Available (DAV) — This bit goes to a logic "1" when an entire character has been received and transferred to the receiver holding register.

Over-Run (OR) — This bit goes to a logic "1" if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register.

Framing Error (FE) — This bit goes to a logic "1" if the received character has no valid stop bit.

Parity Error (PE) — This bit goes to a logic "1" if the received character parity does not agree with the selected parity.

Reader Step (RS) — A logic 1 on this bit will activate the reader step current loop driver.

Clear to Send (CTS) — A logic 1 on this bit will set the CTS output to a +V RS-232 level.

Data Set Ready (DSR) — A logic 1 on this bit will set the DSR output to a +V RS-232 level.

Request to Send (RTS) — This bit goes to a logic 1 when the RS-232 RTS is in its active state.

Data Terminal Ready (DTR) — This bit goes to a logical 1 when the RS-232 DTR is in its active state.

Serial IN (SI) — This port line inputs the serial data stream from the EIA or teletype terminal that is required by DDT-80.

NOTE:
DDT-80 was written to automatically calculate and generate the baud rate for the UART using a CTC. However, the MDX-EPROM/UART and MDX-DEBUG cards do not use this feature. The baud rate for the MDX-EPROM/UART and MDX-DEBUG cards is generated by a switch selectable Baud rate generator.

Serial I/O Connector and Cable

All serial interface lines are brought out to a 26-pin connector J3. The serial cable is constructed of the following parts:

26-pin connector (Ansley No. 609-2600M)
26 wire flat cable (Ansley No. 171-26)
25-pin standard EIA-RS232 connector (Ansley No. 609-25P)

Table 4 shows the interconnection between the 26-pin connector and the 25-pin RS-232 connector.

RS-232 Interface

Because the MDX-EPROM/UART was designed to communicate with RS-232 terminals (as opposed to other types of communication peripherals), the serial interface looks like a receiving modem or computer port rather than a transmitting terminal port (such as a silent 700). The effect is to scramble three pairs of signals. For example:

a. Transmitted Data (RS-232) from Terminal (Pin 3) is an out-direction signal at the terminal but is shown as an in-direction signal at the serial port.

   Receive Data (RS-232) at Terminal (Pin 5) is an in-direction signal at the terminal but is shown as an out-direction signal at the serial port.

b. Request To Send (Pin 7) is an out-direction at the terminal but is shown as an in-direction signal at the serial port.

   Clear To Send (Pin 9) is an in-direction signal at the terminal but is shown as an out-direction signal at the serial port.

c. Data Terminal Ready (Pin 14) is an out-direction signal at the terminal but is shown as an in-direction signal at the serial port.

   Data Set Ready (Pin 11) is an in-direction signal at the terminal but it is shown as an out-direction signal at the serial port.

To change the sense of this port, i.e., to make it look like a transmitting terminal (as might be required in some OEM applications), the two signals in each pair above need to be interchanged.

SERIAL PORT TO RS-232 CONNECTOR
Table 4

SIGNAL NAME	J3 CONNECTOR Pin Number	RS-232 CONNECTOR Pin Number
Chassis GND	1	1
	14	14
Transmitted data	2	2
(RS-232) from terminal	15	15
Receive data (RS-232)	3	3
at terminal		
Reader Step +	16	16
Request to send	4	4
	17	17
Clear to send	5	5
	18	18
Data set ready	6	6
	19	19
GND	7	7
Data terminal ready	20	20
Carrier detect	8	8
Reader step -	21	21
	9	9
	22	22
	10	10
	23	23
	11	11
20 mA Receive (RX+)	24	24
20 mA Receive RET (RX-)	12	12
20 mA Send (TX-)	25	25
20 mA Send RET (TX+)	13	13
	26	Wire remove from 26 wire flat cable

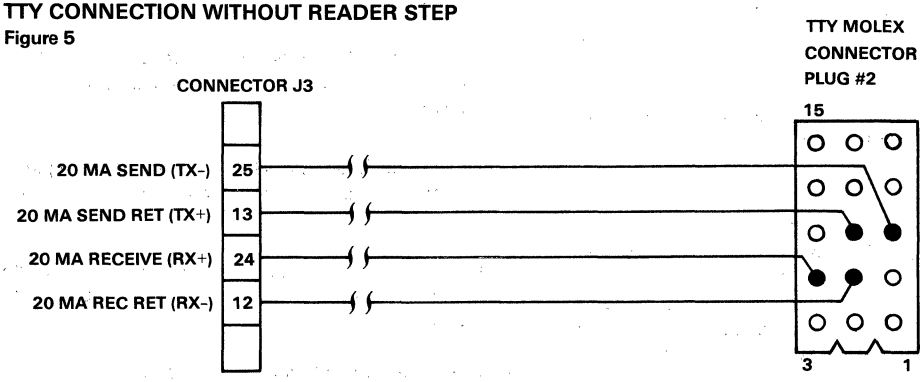
Teletype and Reader Step Interface

Figures 5 and 6 show how the MDX-EPROM/UART can be interfaced to an ASR-33 Teletype with and without reader step. The reader step function is controlled by lines RS+ and RS–. These lines control an optically isolated solid state relay which controls the 115 V ac teletype reader.

NOTE:
1. Under no circumstances should 110 V ac ever be applied to the MDX-EPROM/UART.

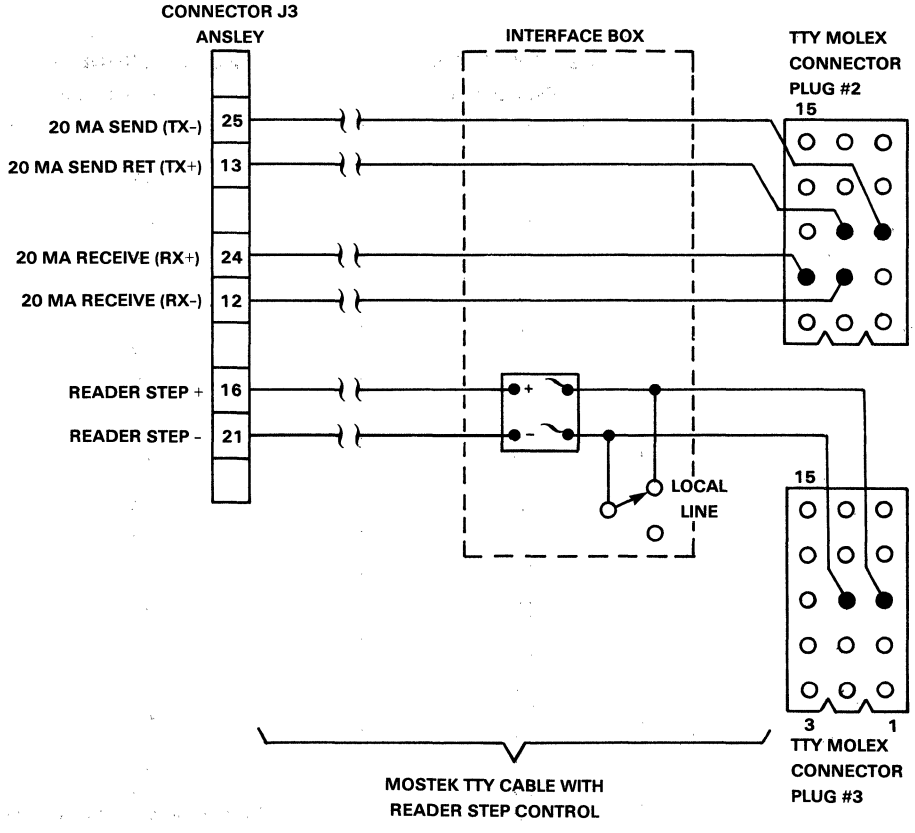
TTY CONNECTION WITHOUT READER STEP

Figure 5



TTY CONNECTION WITH A READER STEP

Figure 6



ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-EPROM/UART	MDX-EPROM/UART with Technical Manual 2.5 MHz	MK77753-0
MDX-EPROM/UART	MDX-EPROM/UART with Technical Manual 4.0 MHz	MK77753-4
MDX-EPROM/UART Technical Manual	MDX-EPROM/UART Technical Manual only	4420029

FEATURES

- STD and STD-Z80 Bus compatible
- Can be strapped to accept the following industry standard devices:

EPROM	STATIC RAM	ROM
2758 (1K x 8)	MK4118 (1K x 8)	MK34000 (2K x 8)
2716 (2K x 8)	MK4802 (2K x 8)	
2732 (4K x 8)		

- Memories can be mixed to form a combination memory board
- Operates at 2.5 MHz and 4.0 MHz system clocks speeds
- Wait-state generator provided
- Single +5 Volt supply

GENERAL DESCRIPTION

The MDX-UMC is a universal memory card for the STD Bus. The MDX-UMC provides the user with the capability of configuring the board to meet the system requirements of ROM/EPROM and/or RAM. By the use of strapping options, the user is able to configure pairs of sockets for ROM/EPROM/RAM to form a combination memory board.

Other MDX-UMC features include 4K boundary addressing and an optional wait-state generator to accommodate slower memories for 4 MHz system clock operations. A block diagram for the MDX-UMC is shown in Figure 2.

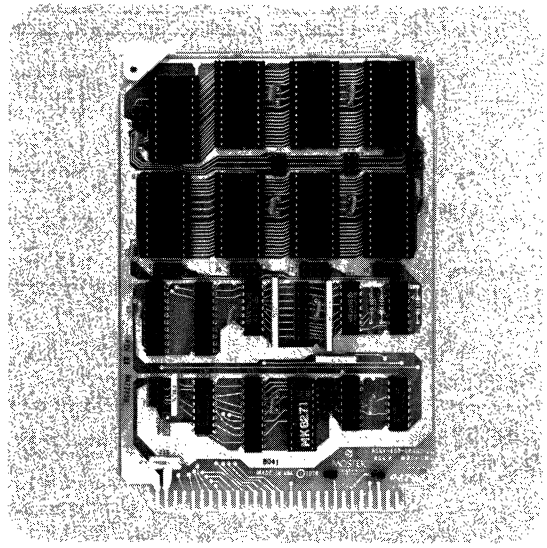
MEMORY ARRAY

The memory array consists of up to 8 RAM, EPROM, or ROM memories. The memories are organized into an array of eight devices with each device contributing one byte to an addressable location.

MEMORY DECODE AND CONTROL

The memory decode and control section is responsible for generating the necessary chip select and output enable signals for the memory arrays. Timing within the memory decode and control section is derived from the STD-Z80 Bus control signals /MEMRQ, /RD, /WR, and /CLOCK.

MDX-UMC
Figure 1



ADDRESS BUFFER

The address buffer is responsible for isolating the STD-Z80 address bus from the memory array.

DATA BUFFER

The data buffer isolates the memory array from the data bus and is controlled by the memory decode and control section.

MEMORY DEVICE SELECTION JUMPERS

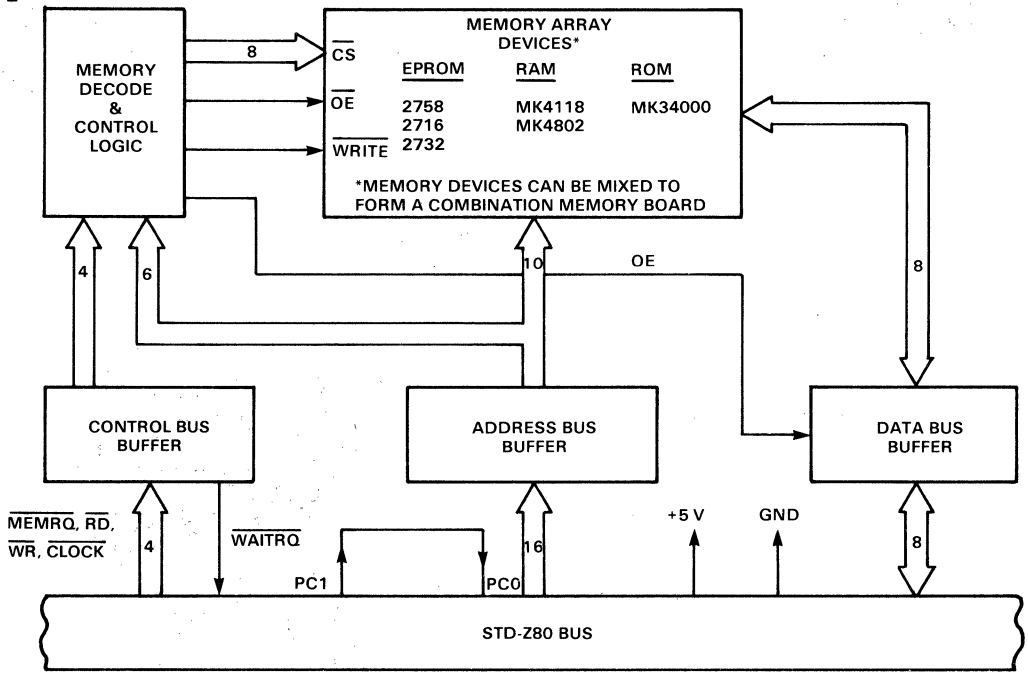
Figure 3 shows how J1-J8 are configured to accommodate the various RAMs, EPROMs, and ROMs.

Table 1 shows how the jumpers J1-J8 are related to memory sockets. It is important to note that the memory sockets are configured in pairs for a particular memory device.

IVD

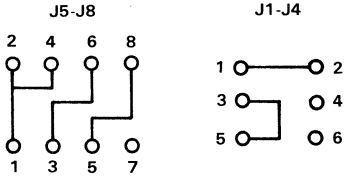
MDX-UMC BLOCK DIAGRAM

Figure 2

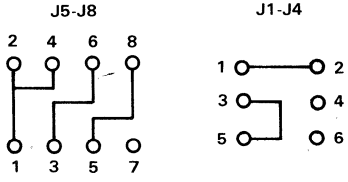


JUMPER CONFIGURATIONS

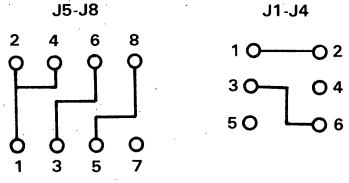
Figure 3



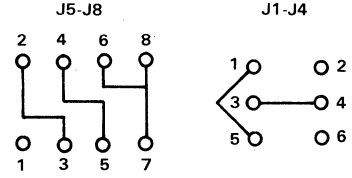
JUMPERS FOR USING 2758s



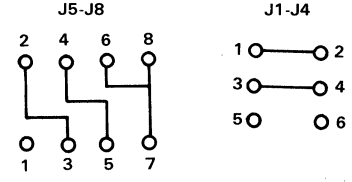
JUMPERS FOR USING 2716s OR MK34000



JUMPERS FOR USING 2732s



JUMPERS FOR USING MK4118s



JUMPERS FOR USING MK4802s

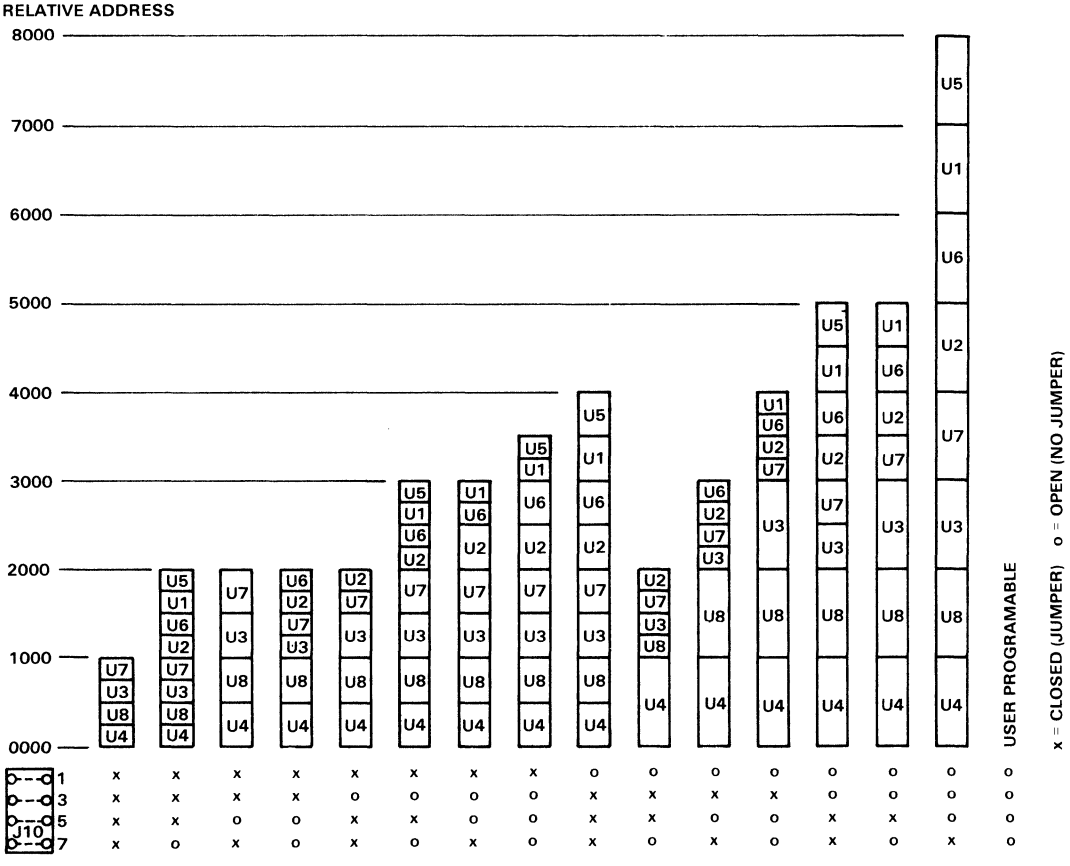
MEMORY DEVICE JUMPERS
Table 1

MEMORY SOCKETS	CONTROLLING JUMPERS
U4, U8	J4, J8
U3, U7	J3, J7
U2, U6	J2, J6
U1, U5	J1, J5

MEMORY SIZE SELECTION JUMPERS

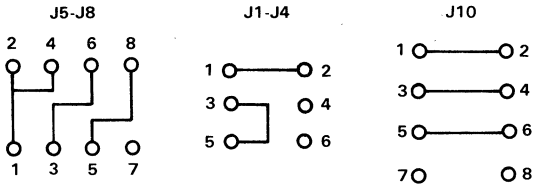
The size of the MDX-UMC memory can be adjusted by the use of J10. Before configuring the J10 jumpers, be sure that the memory device jumpers are in place. Figure 4 shows the possible combinations of J10 versus memory size.

MEMORY SIZE JUMPERS
Figure 4

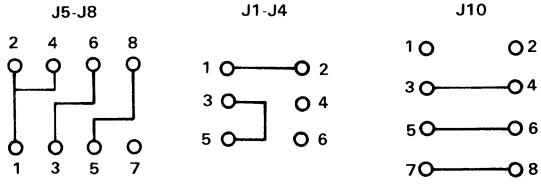


MEMORY DEVICE AND SIZE JUMPER EXAMPLES

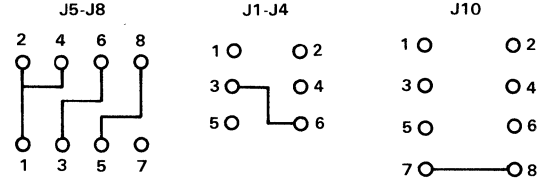
Figure 5



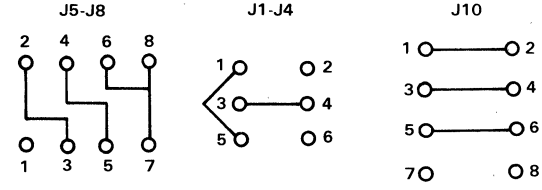
8K X 8 EPROM MEMORY USING 2758s



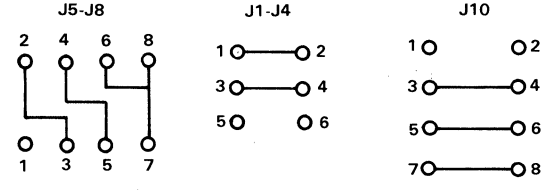
16K X 8 EPROM MEMORY USING 2716s OR MK34000s



32K x 8 EPROM MEMORY USING 2732s



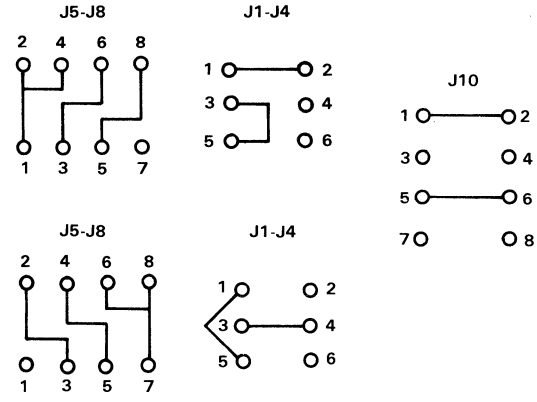
8K X 8 SRAM USING MK4118s



16K X 8 SRAM USING MK4802s

MEMORY DEVICE AND SIZE JUMPER EXAMPLES (Cont.)

Figure 5



COMBINATION 8K X 8 EPROM AND 4K X 8 SRAM (SEE FIGURE 4 FOR MEMORY ALLOCATION)

MEMORY DECODING

Memory decoding for the MDX-UMC is on 4K boundaries, i.e. 000H, 1000H, 2000H, and so on. The starting address for the MDX-UMC is selected by a four position jumper block, J11. Table 2 shows the jumper setting for J11 versus starting address.

MEMORY DECODING

Table 2

Starting Address				J11 Jumper Position				
				1	2	3	4	
0	0	0	0	MSB - 0	0	0	0	- LSB
1	0	0	0	1	1	1	1	
2	0	0	0	1	1	1	0	
3	0	0	0	1	1	0	1	
4	0	0	0	1	1	0	0	
5	0	0	0	1	0	1	1	
6	0	0	0	1	0	1	0	
7	0	0	0	1	0	0	1	
8	0	0	0	1	0	0	0	
9	0	0	0	0	1	1	1	
A	0	0	0	0	1	1	0	
B	0	0	0	0	1	0	1	
C	0	0	0	0	1	0	0	
D	0	0	0	0	0	1	1	
E	0	0	0	0	0	1	0	
F	0	0	0	0	0	0	1	

0 = JUMPERED 1 = OPEN

WAIT STATE GENERATOR

Since most MOS EPROMs cannot meet the required 275 ns access to allow the MDX-UMC to work at 4 MHz, a one wait state generator has been provided. Figure 5 shows how to enable the wait state generator for each memory socket. An example of how to enable the wait states for every memory socket is shown in Figure 6.

ENABLING THE WAIT STATE GENERATOR

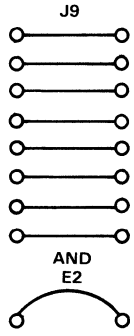
Figure 6

ADD ONE WAIT STATE FOR MEMORY IN SOCKET	CONNECT JUMPER BETWEEN
U4	J9 15 TO 16
U8	J9 13 TO 14
U3	J9 11 TO 12
U7	J9 9 TO 10
U2	J9 7 TO 8
U6	J9 5 TO 6
U1	J9 3 TO 4
U5	J9 1 TO 2

AND E2

EXAMPLE FOR ENABLING ONE WAIT STATE FOR EACH MEMORY SOCKET

Figure 7



ELECTRICAL SPECIFICATIONS

Word Size: 8 bits

Memory Size:

EPROM	RAM
8K x 8 using 2758	8K x 8 using MK4118
16K x 8 using 2716	16K x 8 using MK4802
32K x 8 using 2732	

ROM

16K x 8 using MK34000

Address Selection: Selection of 4K, 8K, or 16K contiguous memory blocks to reside on any 4K boundary, i.e. 000H, 1000H, 2000H, 3000H, and so on.

PARALLEL BUS INTERFACE-STD BUS COMPATIBLE:

Inputs	one 74LS load max
Bus Outputs	I_{OH} = -15 mA min at 2.4 volts
	I_{OL} = 24 mA min at 0.5 volts

System Clock:

	MIN	MAX
MDX-UMC	250 KHz	4 MHz

Power Supply Requirements:

+5 volts ±5% at 0.450A max (Does not include memories)

MECHANICAL SPECIFICATIONS

Card Dimension:

4.5 in (11.43 cm) high by 6.50 in. (16.51 cm) long
0.48 in. (1.22 cm) maximum profile thickness
0.062 in. (0.16 cm) printed circuit board thickness

Connectors:

Function	Configuration	Mating Connector
STD BUS	56 pin dual read out 0.125 in. centers	Printed Circuit Viking 3VH28/1CE5 Wire wrap Viking 3VH28/1CND5 Solder Lug Viking 3VH28/1CN5

Operating Temperature: 0°C to 60°C

REQUIRED MEMORY DEVICE ACCESS TIME

	Maximum Memory Device Access Time	
Clock	No Wait States	One Wait State
2.5 MHz	530 ns	930 ns
4.0 MHz	275 ns	525 ns

ORDERING INFORMATION

Designator	Description	Part Number
MDX-UMC	MDX-UMC module with Technical Manual (less mating connectors)	MK77759
MDX-UMC Technical Manual	Technical Manual only	4420084

MDX-UMC2

FEATURES

- ☐ STD-Z80 bus compatible BYTEWYDE memory card
- ☐ Up to 64K bytes of RAM, ROM, and EPROM in any mix
- ☐ Supports bank switching when multiple boards are used
- ☐ Board may function as common memory in a bank switched system
- ☐ Jumper option allows bank switching through any port
- ☐ Jumper option allows board to be selected upon system reset in multibank systems
- ☐ Jumper option allows memory to begin on any 4K boundary
- ☐ WAIT states selectable on a per socket basis
- ☐ 2.5 or 4 MHz operation
- ☐ Eight 28-pin sockets are provided which may be strapped to accept any combination of the industry-standard memory devices shown in Table 1

MEMORY DEVICES THAT MAY BE USED ON MDX-UMC2

Table 1

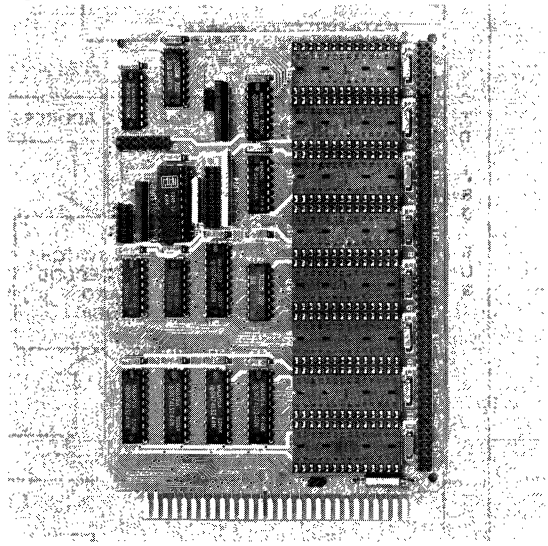
EPROM	STATIC RAM	ROM
2716 (2K x 8)	MK4118A (1K x 8)	MK34000 (2K x 8)
2732 (4K x 8)	MK4801 (1K x 8)	MK37000 (4K x 8)
2764 (8K x 8)	MK4802 (2K x 8)	MK38000 (32K x 8)
27128 (16K x 8)		
27256 (32K x 8)		

MDX-UMC2 DESCRIPTION

The MDX-UMC2 features eight 28-pin memory sockets which enable the user to populate the module with any combination of designated ROM, RAM, and EPROM. Flexible address decoding allows the user to configure each memory device within any 1K boundary of the memory block on board. The memory block may start on any 4K boundary of any (or all) of eight 64K banks. A PROM decoder

MDX-UMC2

Figure 1

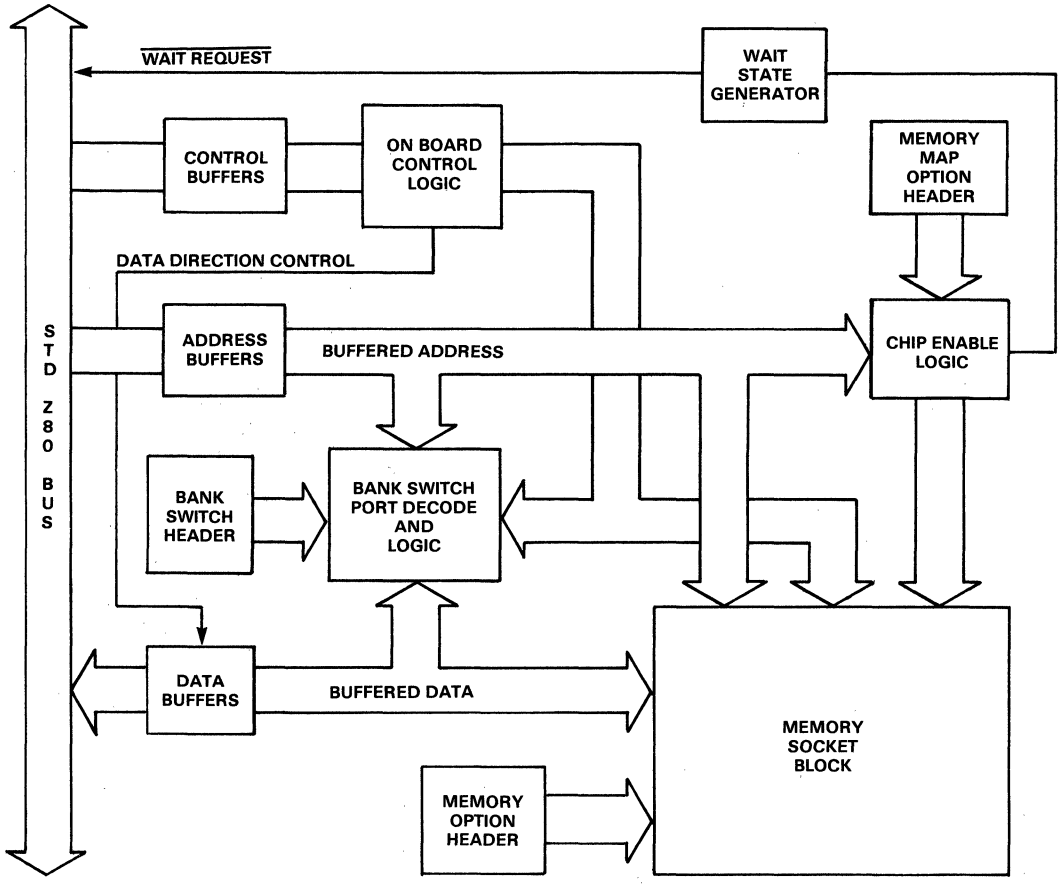


is supplied which will allow the user to choose one of eight preselected memory configurations or, by programming a decoder PROM, the user can assign any of the eight sockets to memory addresses as required by his application needs. To ensure sufficient memory access time at 4 MHz operation, a jumper option enables automatic insertion of one WAIT state for those memory devices identified as "slow" in the decoder PROM. The standard decoder PROM supplied with MDX-UMC2 identifies RAMs as "fast" parts (no WAIT states) and ROMs and EPROMs as "slow" parts (one WAIT state).

Also provided on the MDX-UMC2 is the circuitry to enable the board to be used in a multibank system. The board may occupy one entire 64K bank or as little as 1K of a 64K bank. The MDX-UMC2 can be used to provide the common memory in a multibank system. Bank selection is accomplished through writing to a user defined port. Each bit in the port activates a single bank, for example, bit 0 set enables bank 0, bit 1 set enables bank 1, etc. The user may strap the board to reside in any of the eight banks. For use as the common memory in a multibank system, the MDX-UMC2 must be jumpered so that it is active when any bank is selected. A header is provided for this purpose. The user may strap the board so that it will be active or inactive upon system reset.

MDX-UMC2 BLOCK DIAGRAM

Figure 2



MECHANICAL SPECIFICATIONS

Card Dimensions:

4.50 in. (11.43 cm) wide
6.50 in. (16.51 cm) long
0.675 in. (1.71 cm) maximum profile thickness
0.062 in. (0.16 cm) printed circuit board thickness

STD Bus Edge Connector:

56-pin dual readout; 0.125 in. centers
Mating Connectors:
PCB - Viking 3VH28/1CE5
WIREWRAP - Viking 3VH28/1CND5
SOLDER LUG - Viking - 3VH28/1CN5

ELECTRICAL SPECIFICATIONS

STD-Z80 Bus Compatible

System Interrupt Units:

This board does not generate any interrupts.

Operating Temperature:

0 to 60 degrees C.

Power Supply Requirements:

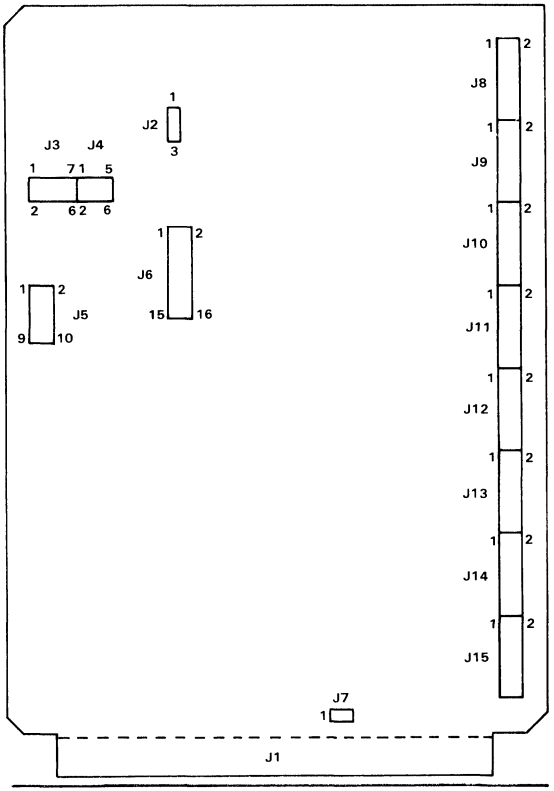
5 V ± 5% @ 1.1 A (excluding memory power requirements)

CONNECTORS AND OPTION HEADERS

For the location of all connectors and option headers, see Figure 3.

BOARD OUTLINE AND HEADER LOCATION

Figure 3



J1 PIN DEFINITION

Figure 4

SIGNAL		PIN		PIN		SIGNAL
+5 V		1		2		+5 V
GND		3		4		GND
-5 V	*	5		6	*	-5 V
D3		7		8		D7
D2		9		10		D6
D1		11		12		D5
D0		13		14		D4
A7		15		16		A15
A6		17		18		A14
A5		19		20		A13
A4		21		22		A12
A3		23		24		A11
A2		25		26		A10
A1		27		28		A9
A0		29		30		A8
/WR		31		32		/RD
/IORQ		33		34		/MEMRQ
/IOEXP	*	35		36	*	/MEMEX
/REFRESH	*	37		38	*	/MCSYNC
/STATUS 1	*	39		40	*	/STATUS 0
/BUSAK	*	41		42	*	/BUSRQ
/INTAK	*	43		44	*	/INTRQ
/WAITRQ		45		46	*	/NMIRQ
/SYSRESET		47		48	*	/PBRESET
/CLOCK		49		50	*	/CNTRL
PCO		51		52		PCI
AUX GND	*	53		54	*	AUX GND
+12 V	*	55		56	*	-12

The "*" indicates signals not used on MDX-UMC2

J1 STD-Z80 BUS

Pin definition is as shown in Figure 4. See STD-Z80 Bus description for signal functions.

J2 Active/Inactive on Reset

This header determines whether the MDX-UMC2 becomes active or inactive upon system reset. The memory bank selected to act as system boot memory in a bank switched system should become active upon reset, while all other banks should be inactive. For the board to be active upon reset, place jumper from pin 1 to pin 2. For the board to be inactive, place jumper from pin 2 to pin 3. If the board is to be used in a non bank switched system, a jumper should be placed between pins 1 and 2 as shown in the example. Shipping configuration is with no jumpers installed.

EXAMPLE:

```
1  2  3
*—*  *  J2
```

The board will be active upon reset.

J3 Memory Starting Address

This header determines the starting address for the on board memory. The memory may begin at any 4K boundary within a given bank, so the starting address takes on the form X000 hex. See Table 2 for starting addresss jumper configurations.

MEMORY STARTING ADDRESS

Table 2

STARTING ADDRESS (HEX)	1 * * * * 7 2 * * * * 8	STARTING ADDRESS (HEX)	1 * * * * 7 2 * * * * 8
0000	O O O O	8000	O O O I
1000	I O O O	9000	I O O I
2000	O I O O	A000	O I O I
3000	I I O O	B000	I I O I
4000	O O I O	C000	O O I I
5000	I O I O	D000	I O I I
6000	O I I O	E000	O I I I
7000	I I I O	F000	I I I I

I = JUMPER IN PLACE O = PINS LEFT OPEN

IVD

EXAMPLE:

```
1 * * * * 7
          J3
2 * * * * 8
```

The starting address is 0000 hex (shipping configuration).

J4 Memory Map Option Select

This header selects one of eight possible memory maps for the memory on the MDX-UMC2. The hexadecimal equivalent of the jumper sequence on J4 corresponds to the memory map selected. A jumper in place asserts a logic "0", while no jumper in place indicates a logic "1".

EXAMPLE:

```
1 * * * 5
        J4
2 * * * 6
  B B B
  I I I
  T T T
  0 1 2
```

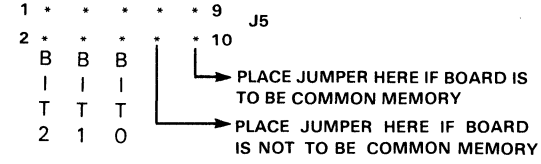
The binary number represented by the jumper sequence above is 111 or 7 hexadecimal so map 7 is selected (shipping configuration). For map definitions, see Table 3.

J5 Bank Select and Common Area Decode Header

This header selects the 64K bank in which the MDX-UMC2 resides and determines whether or not the board shall act as common memory. Pins 1-6 determine the bank in which the on-board memory will reside as defined in Figure 5. If the board is to act as common memory in a bank switched system, insert a jumper between pins 9 and 10, otherwise insert a jumper between pins 7 and 8. If the board is not to be used in a bank switched system, all pins on this header may be left open (shipping configuration).

J5 JUMPER OPTIONS

Figure 5



BANK (1 * * * * * * 9 / 2 * * * * * * 10)		BANK (1 * * * * * * 9 / 2 * * * * * * 10)	
0	I I I	4	O I I
1	I I O	5	O I O
2	I O I	6	O O I
3	I O O	7	O O O
I = JUMPER IN PLACE		O = PINS LEFT OPEN	

MEMORY MAP DEFINITION

Table 3

SOCKET	MAP OPTION 0		MAP OPTION 1		MAP OPTION 2		MAP OPTION 3	
	SIZE	ADDR	SIZE	ADDR	SIZE	ADDR	SIZE	ADDR
U 14	1K	0000	2K S	0000	4K S	0000	8K S	0000
U 15	1K	0400	2K S	0800	4K S	1000	8K S	2000
U 16	1K	0800	2K S	1000	4K S	2000	8K S	4000
U 17	1K	0C00	2K S	1800	4K S	3000	8K S	6000
U 18	1K	1000	2K S	2000	4K S	4000	2K	8000
U 19	1K	1400	2K S	2800	4K S	5000	2K	8800
U 20	1K	1800	2K S	3000	4K S	6000	2K	9000
U 21	1K	1C00	2K S	3800	4K S	7000	2K	9800

SOCKET	MAP OPTION 4		MAP OPTION 5		MAP OPTION 6		MAP OPTION 7	
	SIZE	ADDR	SIZE	ADDR	SIZE	ADDR	SIZE	ADDR
U 14	16K S	0000	32K S	0000	32K S	0000	8K S	0000
U 15	16K S	4000	2K	8000	2K S	8000	8K S	2000
U 16	2K	8000	2K	8800	2K S	8800	8K S	4000
U 17	2K	8800	2K	9000	2K S	9000	2K S	8000
U 18	2K	9000	2K	9800	2K	9800	2K S	8800
U 19	2K	9800	2K	A000	2K	A000	2K	9000
U 20	2K	A000	2K	A800	2K	A800	2K	9800
U 21	2K	A800	2K	B000	2K	F800	2K	F800

THE "S" INDICATES THAT THE DECODER PROM IDENTIFIES THESE PARTS AS "SLOW".

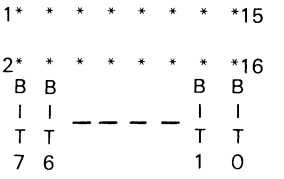
EXAMPLE:

The board will reside in bank 4 for use in a bank switched system. Common memory will reside on some other memory card in the system. For the board to become active, bit 4 of the byte written to the bank switch port must be set to a logic "1" while all other bits contain a logic "0".

J6 Bank Select Port Address

This set of jumpers selects the address of the port through which bank switching is accomplished. The port address will be the hexadecimal equivalent of the jumper sequence. Insert a jumper to assert a logic "0"; leave jumper off to indicate a logic "1".

EXAMPLE:

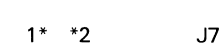


The hexadecimal equivalent of the jumper sequence is FF, so the port is located at address FF hex (shipping configuration).

J7 WAIT State Enable

This header enables WAIT states for memory parts identified as "slow" in the decoder PROM. A jumper between pins 1 and 2 of J7 will enable WAIT states.

EXAMPLE:



WAIT states are disabled (shipping configuration).

J8-J15 Socket Configuration Headers

These headers allow the user to configure each memory socket (U14-U21 respectively) so that it will accept one of the standard memory parts listed under the heading 'FEATURES'. The required jumpers for each of these parts are shown in Table 4.

For information on configuring the memory sockets for other types of memory components, see the heading "MEMORY SOCKET CONSIDERATIONS".

MEMORY SOCKET CONSIDERATIONS

The UMC2 card will accept many memory components other than those listed under the heading 'FEATURES'. The following information is provided to aid the user in configuring the memory sockets for components other than those listed. Each of the eight memory sockets have the pin configuration as shown in Figure 6. The numbers inside the parentheses are pin numbers for 24-pin memory components. When 24-pin packages are used, the memory should occupy the bottom part of the socket leaving pins 1, 2, 27, and 28 open.

The pins indicated by the "*" are "option pins". These pins may be defined by the user so that the socket will accept a particular memory type. This is accomplished by inserting jumpers into the socket configuration header (J8-J15) adjacent to the memory socket. The function of each pin of the header is shown in Figure 7.

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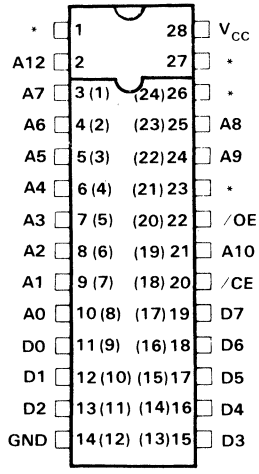
STANDARD MEMORY SOCKET CONFIGURATIONS

Table 4

MEMORY	JUMPERS REQUIRED	MEMORY	JUMPERS REQUIRED
4118A	1 * * * * * * * 13 2 * * * * * * * 14	27128	1 * * * * * * * 13 2 * * * * * * * 14
4801	1 * * * * * * * 13 2 * * * * * * * 14	27256	1 * * * * * * * 13 2 * * * * * * * 14
4802	1 * * * * * * * 13 2 * * * * * * * 14	34000	1 * * * * * * * 13 2 * * * * * * * 14
2716	1 * * * * * * * 13 2 * * * * * * * 14	37000	1 * * * * * * * 13 2 * * * * * * * 14
2732	1 * * * * * * * 13 2 * * * * * * * 14	38000	1 * * * * * * * 13 2 * * * * * * * 14
2764	1 * * * * * * * 13 2 * * * * * * * 14		

MEMORY SOCKET PIN CONFIGURATIONS

Figure 6



MEMORY ACCESS TIMES

The table below indicates the required access times for memory components for operation at 2.5 MHz and 4 MHz. If the component's access time is greater than that shown in Table 5, one WAIT state will be required. One WAIT state will add 250 ns to the required memory access time at 4 MHz. One WAIT state will add 400 ns to the required memory access time at 2.5 MHz.

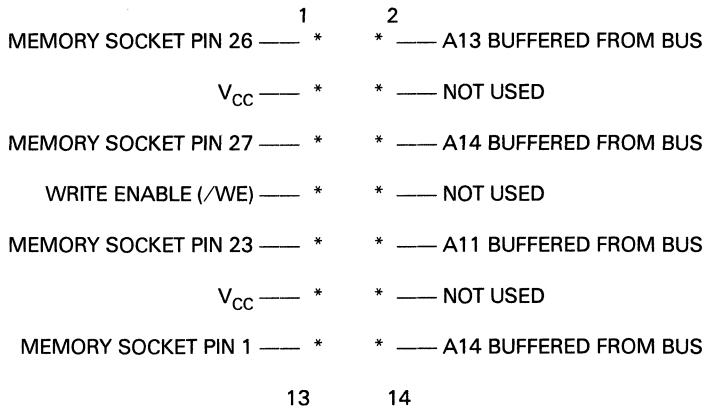
REQUIRED MEMORY ACCESS TIME

Table 5

SYSTEM CLOCK	ACCESS TIMES REQUIRED	
	/CE TO DATA	/OE TO DATA
2.5 MHz	< 438 ns	< 425 ns
4.0 MHz	< 188 ns	< 175 ns

PIN FUNCTION OF J8-J15

Figure 7



ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-UMC2	Universal Memory Card (less memory and mating connectors)	MK-77763
MDX-UMC2 Technical Manual	Technical Manual only	4420319

MDX-BRAM

FEATURES

- 2K or 4K bytes of memory
- 4K boundary selection
- Same board used with 2.5 MHz or 4.0 MHz systems
- Rechargeable batteries
- 4K of memory sustained for at least five days with fully charged batteries
- Wait state circuit allows sufficient access time for RAMs

GENERAL DESCRIPTION

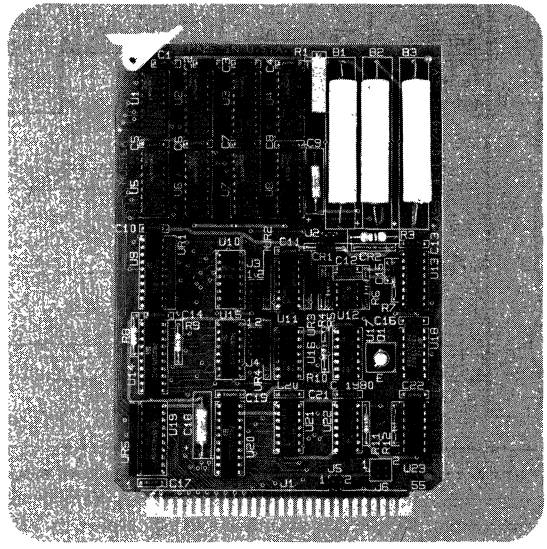
The MDX-BRAM is one of Mostek's complete line of STD Bus-compatible Z80 microcomputer modules. The MDX-BRAM is designed to save up to 4K bytes of memory during a power failure. Power degradation is detected by either the resident 5 volt monitoring circuitry or an external power fail detect module (MDX-PFD). When a power failure is detected, the on-board battery power is enabled to retain memory data.

The MDX-BRAM provides 4K bytes of random access memory (RAM). The addressing of the board is jumper selectable on 4K boundaries within a 64K address space. The MDX-BRAM2 provides 2K bytes of RAM.

The board has a DC power monitor circuit to detect when the 5 volt supply line is lower than a specified value. It also contains the interface circuitry to monitor an external signal (/SYSRESET) indicating a power failure has been detected by the MDX-PFD module. When a power failure is detected by either method, battery power is enabled and all access to the board is blocked until primary power is restored.

Battery power is supplied by three NiCad cells which can provide enough energy to retain memory data for up to five days. An on-board battery charging circuit is provided to ensure the batteries are kept fully charged while the board is in use. Duration of data retention may be considerably less when the batteries are not fully charged. An MDX-BRAM Block Diagram is shown in Figure 2.

MDX-BRAM
Figure 1



Address Decoder and Buffer

All the address lines are buffered. The first ten (A0-A9) go directly from the buffer to the array, and the other six (A10-A15) go through a compare circuit for the board address and a decode circuit to form the four chip select signals.

Control and I/F Circuit

The block generates the /WE, SYSPF, and data direction signals from the /RD, /WR, /WREQ, and /SYSRESET signals.

Data Buffer

The data into the board is buffered by a 74LS245. The bus is normally turned into the board, and is turned out for a read operation. The bus is normally enabled but is disabled during the system reset or power fail. This is done to prevent an invalid write to memory during power down and power up.

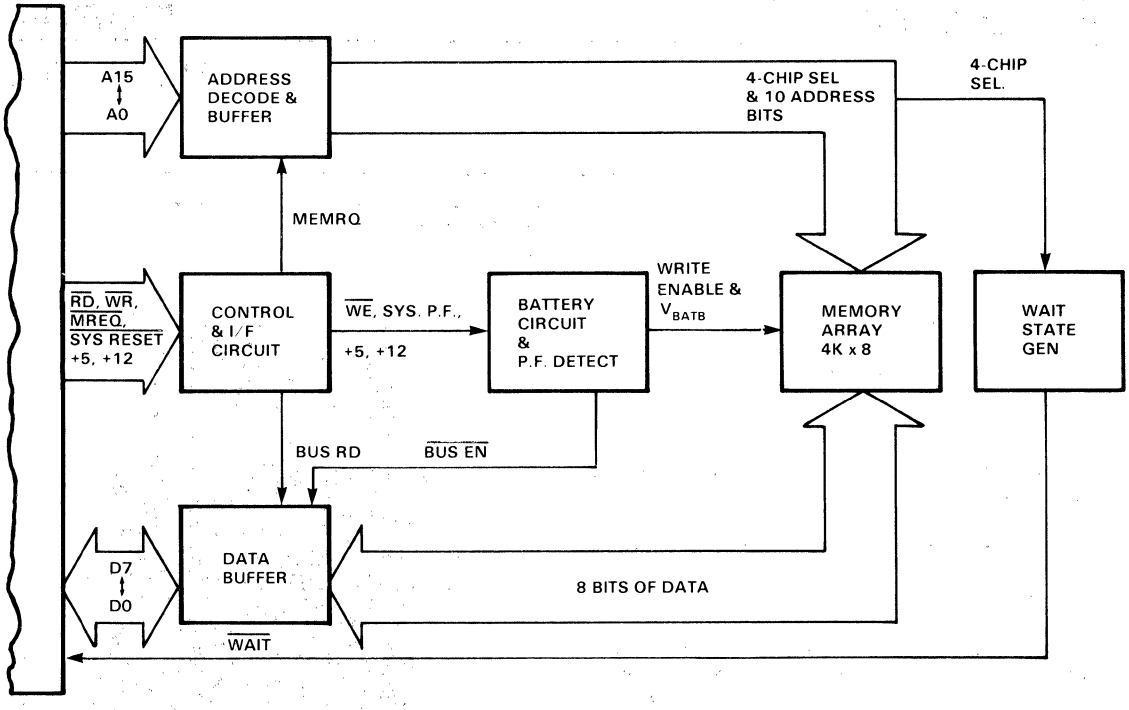
Memory Array

The memory array consists of CMOS RAMs. These RAMs

IVD

MDX-BRAM BLOCK DIAGRAM

Figure 2



are 1K x 4 bits in an eighteen pin package; they have a 300 nsec access time and a standby current drain of 50 microamps. The array is organized into logical pairs for each of the four chip selects. The total array when fully populated is 4K x 8 bits.

Battery Circuit and Power Fail Detect

The battery charger circuit can be viewed as three circuits which are overlaid to form one circuit. The first circuit (the major source of charge) is from the +12 V supply and provides a nearly constant input of approximately 9 mA. The second circuit comes from the +5 V line which will provide a nominal 9 mA and is cut off to a very small trickle as the batteries become fully charged. The third circuit is the discharge circuit which provides a low resistance path (120 ohms) or at most a diode drop when the VBAT current drain is large. The zener protects the CMOS circuitry if +5 V drops out and +12 V is still present. In addition, note that the VBAT is provided anytime +5 V is present. This provision protects the CMOS circuits by providing power to the CMOS whenever an input is possibly present.

Three AAA size NiCads supply power to the memory for five days when fully charged. It will take at least twenty-four hours of operation to charge the batteries to full capacity.

The power fail detect circuit will detect when the 5 volt supply to the board falls below 4.7 volts (the factory setting at ambient) and remains below 4.85 volts (maximum) for more than four microseconds. When this occurs, the board will block all access to the memory array. When the 5 volt supply rises above 4.85 volts, this circuit will again allow access to the memory.

WARNING: This circuit contains a potentiometer which should not generally be set in the field. It is set at the factory and requires equipment which may not be available to the user. Changing the setting of this circuit will void the warranty. If it is changed inadvertently, the following procedure may be used to reset it.

1. Adjust the 5 volt power supply to 4.70 volts.
2. Connect an oscilloscope or a voltmeter to the output (pin 4) of the ICL8211 (U12).
3. Adjust R2 until the voltage on pin 4 goes to an active level (>2.4 V).
4. Slowly adjust the pot in the opposite direction until the voltage goes low (>.7 V).
5. Readjust the 5 volt supply to 5 volts.

This circuit is also for the detection of /SYSRESET signal (pin 47 on the STD-Z80 Bus); when this signal is active, all access is blocked. This allows the board to interface to the power fail detect board (Mostek Part Number MK77760). The power fail detect board will detect A.C. power failures and "brown-outs" and give an early warning signal to the CPU to allow an orderly shut-down of the system.

The circuit also does memory access blocking. If a power failure is detected, either on this board or on the MDX-PFD, this circuit will prevent any bus access to the board. This turns off all interface of address, data, and read and write control signals and access is blocked as long as the /SYSRESET is asserted or the 5 volt supply is below 4.85 volts.

Wait State Generator

The wait state generator will insert one WAIT state during an access of the board to allow for the 300 nsec access time of the CMOS RAM.

BOARD ADDRESS

Starting memory addressing for the MDX-BRAM is selectable on 4K boundaries, i.e., 0000H, 1000H, 2000H, and so on. The starting address is selected using four jumper positions located at J5. Table 1 shows the jumpers to be used for various starting addresses.

ADDRESS JUMPERS

Table 1

Address	Jumpers installed at J5			
Most Significant Hex	1-2	3-4	5-6	7-8
0	Y	Y	Y	Y
1	Y	Y	Y	N
2	Y	Y	N	Y
3	Y	Y	N	N
4	Y	N	Y	N
5	Y	N	Y	N
6	Y	N	N	Y
7	Y	N	N	N
8	N	Y	Y	Y
9	N	Y	Y	N
A	N	Y	N	Y
B	N	Y	N	N
C	N	N	Y	Y
D	N	N	Y	N
E	N	N	N	Y
F	N	N	N	N
Add jumper for 'Y' and remove jumper for 'N'				

MEMORY EXPANSION

/MEMEX (pin 36 on the STD-Z80 Bus) is not used by the Mostek MDX-CPU1 and MDX-CPU2 and is held low by the backplane. The jumper at J7 allows use of this board in systems that do incorporate this feature. For the MDX-BRAM to provide primary memory (/MEMEX is low), jumper J7-1 to 2 is used; if it is not primary memory (enabled when /MEMEX is high), then J7-3 to 4 is jumpered.

WAIT STATE

The Wait State Jumper (located at J6-1 to 2) will normally be installed; however, if faster CMOS RAMs (sub 200 nsec for 4 MHz, and sub 350 nsec for 2.5 MHz) are used, this jumper may be removed to eliminate the wait state added to each memory access. (Note that the jumper may be removed for 2.5 MHz systems using the RAMs provided with the board.)

MEMORY SIZE

Four jumpers may be installed, depending on the memory size. When 1K of memory is installed (U4 and U8 only), jumper J4-1 to 2 is in place. With 2K of memory (U3, U4, U7, and U8), install jumpers J4-1 to 2 and J4-3 to 4, and J4-5 to 6. When all 4K of memories are installed (U1 through U8), place all four jumpers as follows: J4-1 to 2, J4-3 to 4, J4-5 to 6, and J4-7 to 8.

These four jumpers will select only those 1K increments of memory the user needs.

5 VOLT ONLY

A jumper at J2-1 to 2 is installed if and only if the system is operated with a 5 volt only supply, that is, if a 12 volt supply is unavailable. It should be noted, however, that this mode increases the charge time to 36 hours for full charge at 25°C.

BATTERY DISCONNECT

To remove the batteries from the circuit (for removal or addition of CMOS IC socketed on the board or for prolonged storage of 2 to 3 months), the jumper J3-1 to 2 will need to be removed. (Note: this jumper is not factory-installed and should be inserted before use.)

ELECTRICAL SPECIFICATIONS

System Clock

	MIN	MAX
MDX-BRAM	250 kHz	4.0 MHz

Bus Interface-STD-Z80 Compatible

Inputs: One 74LS load max

Outputs: I_{OH} = -3 mA min at 2.4 volts

I_{OL} = +24 mA min at 0.5 volts

Power Supply Requirements

+12 Volts ±5% at .2 A max
+5 Volts ±5% at 1.0 A max
-9 mA max on standby battery

Battery Type Used

3 AAA NiCads supplies with card

Battery Life

Three years or 200 full charge/discharge cycles (whichever is less)

Word Size

Data: 8 bits
I/O Addressing: 16 bits, jumper selection on 4K boundary

Access Time

Less than 400 nsec

Operating Temperature Range

0 to 60°C

Power Failure Detection Level

A power failure is registered when:

1. The 5 volt supply level drops below 4.7 volts and is then held less than 4.85 volts maximum for more than 4 microseconds, or
2. When the /SYSRESET signal is active.

MECHANICAL SPECIFICATIONS

Card Dimensions

4.5 in. (114.3 mm) wide by 6.5 in. (165.1 mm) long
0.675 in. (17.1 mm) maximum profile thickness
0.062 in. (1.6 mm) printed circuit board thickness

Connectors

Connector Function	Configuration	Connectors
STD BUS	56 Pin dual read out 0.125 in. centers	Printed Circuit Viking 3VH28/1CE5 Wire Wrap Viking 3VH28/1CND5 Solder Lug Viking 3VH28/1CN5

ORDERING INFORMATION

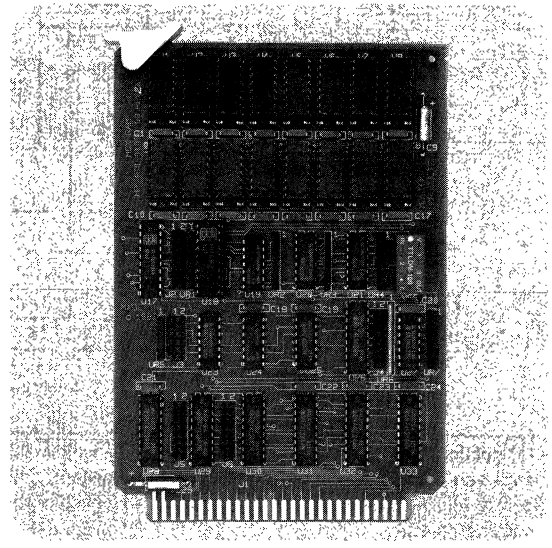
Designator	Description	Part Number
MDX-BRAM4	MDX-BRAM4 module with Technical Manual (4K memory)	MK77760
MDX-BRAM2	MDX-BRAM2 module with Technical Manual (2K memory)	MK77762
MDX-BRAM Technical Manual	Technical Manual only	4420066

MDX-RAM 64/128

FEATURES

- ☐ STD-Z80 Bus compatible
- ☐ 64K (MDX-RAM64) or 128K (MDX-RAM128) bytes of dynamic RAM
- ☐ +5 V only operation
- ☐ Automatic refresh accomplished through use of STD-Z80 /REFRESH signal
- ☐ 2.5 MHz or 4.0 MHz operation with no wait states
- ☐ Bank switching accomplished via a user designated I/O port
- ☐ Bank switching is hardware compatible with MDX-UMC2, MDX-CPU3, and MDX-CPU4
- ☐ Common memory area for bank switched systems may reside at any 256 byte boundary within the 64K memory map
- ☐ Common area size is user defined in 256 byte increments
- ☐ Common area can be made resident on any board
- ☐ Option allows the board to become active upon system reset for use as the system boot memory
- ☐ MEMEX and IOEXP are supported, polarity for each is user defined

MK77765
Figure 1



MDX-RAM DESCRIPTION

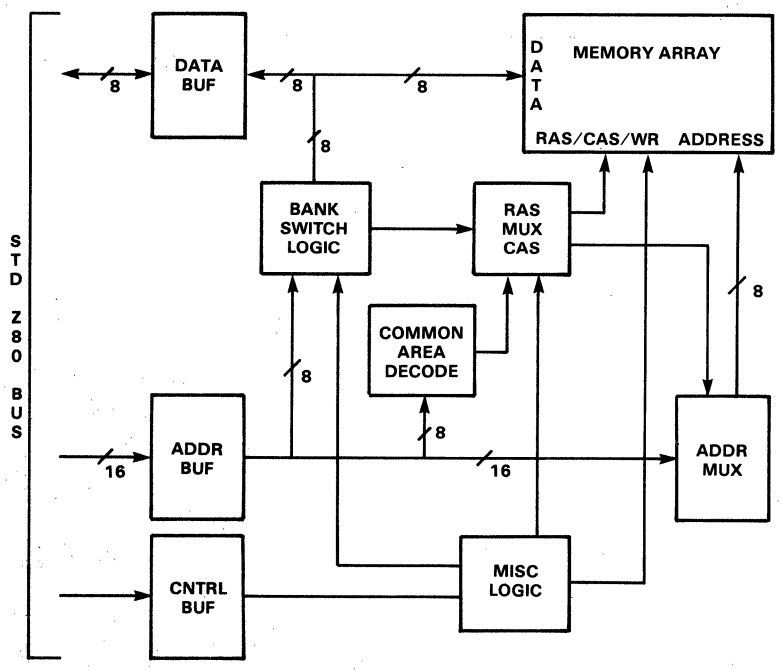
The MDX-RAM card features a capacity of 64K or 128K bytes of dynamic memory, and will support selection of multiple 64K banks under software control. Provision is made for an area of memory which will be common to all 64K banks, useable for operating system or applications software which is needed by all banks. The bank select structure is the same as that used on MDX-CPU3, MDX-CPU4, and MDX-UMC2 and is compatible with commercially available software packages. The board will function in 2.5 MHz and 4.0 MHz STD-Z80 systems with no WAIT states.

MDX-RAM has features designed to simplify implementation of multi-user operating systems such as MP/M™* or MULTI/OS™**. One of 8 banks of 64K bytes each is selected by writing a "1" to one of 8 bits at the bank switch port location. Setting bit 0 will select bank 0, setting bit 1 will select bank 1, and so on. Only one bank may be selected at a time. The actual bank switch port address may be jumper selected to reside at one of 256 locations. In addition, /MEMEX is decoded as a board enable (polarity jumper selectable) to double the number of banks that may be selected at each port location. /IOEXP is decoded as a port enable (polarity jumper selectable) to double the number of bank select port locations. A special option allows the user to select the board as the default system boot memory on reset without prior software intervention, enabling the board to be used as a standard 64K board without special software.

To facilitate switching from one bank to another, a special common memory area has been provided. This area of memory remains enabled regardless of which memory bank has been selected. The user may place a software monitor in this common memory area for communicating data between banks. This guarantees that the monitor will still be available when a new bank is selected. The common area may begin on any 256 byte boundary within the 64K memory map and is size selectable in 256 byte increments.

™* Digital Research
™** Infosoft

BLOCK DIAGRAM MDX-RAM
Figure 2



In addition, an option has been incorporated to allow the common area to reside on any board in the system. One board in the system must be selected to contain the common area.

Memory refresh circuitry has been provided on board, and makes use of the STD-Z80 /REFRESH signal. Memory will be refreshed even if it does not reside in the currently selected bank.

In addition, PCI is connected to PCO for preserving the Z80 interrupt priority chain.

MECHANICAL SPECIFICATIONS

Card Dimensions

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm.) long
0.675 in. (1.71 cm.) maximum profile thickness
0.062 in. (0.16 cm.) printed circuit board thickness

STD BUS Edge Connector

56 pin dual readout; 0.125 in. (0.32 cm.) centers
Mating Connectors:
PCB - Viking 3VH28/1CE5
WIREWRAP - Viking 3VH28/1CND5
SOLDER LUG - Viking 3VH28/1CN5

ELECTRICAL SPECIFICATIONS

STD-Z80 Bus Compatible

System Interrupt Units

No interrupts are generated by this board.

Operating Temperature

0 to 60 degrees C

Power Supply Requirements

MDX-RAM64 +5 V ± 5% @ 2.0 A MAX
MDX-RAM128 +5 V ± 5% @ 2.6 A MAX

CONNECTORS AND HEADERS

For the location of all connectors and option headers, see Figure 3.

J1 STD-Z80 Bus 56 Pin

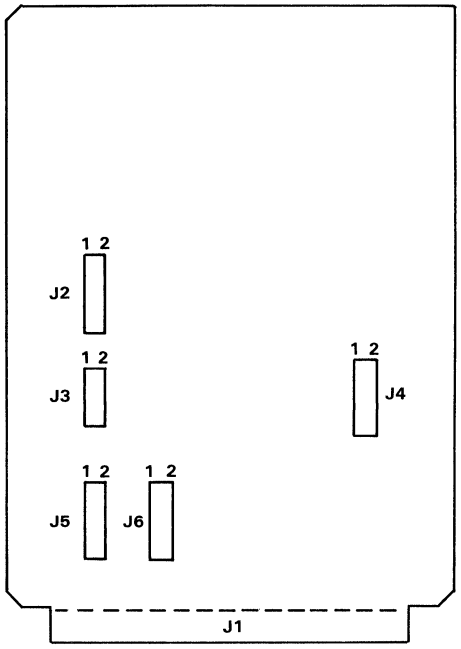
For J1 pin definition, see Figure 4. (See STD-Z80 Bus description for signal functions).

J2 Bank Select Header

This header determines which banks of memory will reside on board. The odd numbered pins correspond to the eight bits in the bank switch port. Two of the even numbered pins correspond to the enables of the two 64K rows of memory that may reside on board. Two of the even numbered pins are reserved for future expansion. The function of each pin

HEADER AND CONNECTOR LAYOUT

Figure 3



J1 PIN FUNCTION

Figure 4

SIGNAL	PIN		PIN	SIGNAL
+5 V	2		1	+5 V
GND	4		3	GND
-5 V	* 6		5 *	-5 V
D7	8		7	D3
D6	10		9	D2
D5	12		11	D1
D4	14		13	D0
A15	16		15	A7
A14	18		17	A6
A13	20		19	A5
A12	22		21	A4
A11	24		23	A3
A10	26		25	A2
A9	28		27	A1
A8	30		29	A0
/RD	32		31	/WR
/MEMRQ	34		33	/IORQ
MEMEX	36		35	IOEXP
/MCSYNC	* 38		37	/REFRESH
/STATUS 0	* 40		39 *	/STATUS 1
/BUSRQ	* 42		41 *	/BUSAK
/INTRQ	* 44		43 *	/INTAK
/NMIRQ	* 46		45 *	/WAITRQ
/PBRESET	* 48		47	/SYSRESET
/CNTRL	* 50		49 *	/CLOCK
PCI	52		51	PCO
AUX GND	* 54		53 *	AUX GND
-12 V	* 56		55 *	+12

The "*" indicates signals not used on MDX-RAM.

is shown below. To select the banks that will reside on board, place a jumper between the designated row enable and the bank select port bit that it should respond to.

J2

1	2
BANK 0 --- *	* --- NO CONNECTION
BANK 1 --- *	* --- NO CONNECTION
BANK 2 --- *	* --- ROW 0 (64K RAM)
BANK 3 --- *	* --- ROW 1 (64K RAM)
BANK 4 --- *	* --- RESERVED
BANK 5 --- *	* --- RESERVED
BANK 6 --- *	* --- NO CONNECTION
BANK 7 --- *	* --- NO CONNECTION
15	16

Row 0 may be used only if U1-U8 are populated with 4564 RAM's (MDX-RAM64 or MDX-RAM128).

Row 1 may be used only if U9-U16 are populated with 4564 RAM's (MDX-RAM128).

EXAMPLE:

If U1-U16 are populated with 4564 RAM's (MDX-RAM128), both rows of memory may be used, rows 0 and 1. To make these rows respond to banks 3 and 4 respectively, place a jumper between pins 6 and 7 and a jumper between pins 8 and 9.

EXAMPLE:

If U1-U8 are populated with 4564 RAM's (MDX-RAM64), only row 0 may be used. To make this row respond to bank 2, place a jumper between pins 5 and 6.

J3 IOEXP, MEMEX, Reset Status, Common Memory Location

This header selects the polarities of IOEXP and MEMEX that the board will respond to, whether or not the board will become active upon system reset, and whether or not the common memory area will reside on board or on some other board in the system. Place jumper between pins 1 and 2 to cause the board to respond to a logic 0 on IOEXP, or between pins 3 and 4 to cause the board to respond to a logic 1. If the host system does not support IOEXP, leave pins 1 through 4 open. A jumper between pins 5 and 6 indicates that the common memory area will reside on board. If this jumper is in place and the address bus contains an address within the range defined by J5 (common memory ending address) and J6 (common memory starting address), the memory in U1-U8 will become active. If this jumper is not in place and the address bus contains an address within range defined by J5 and J6, no memory on the MDX-RAM will become active. Place a jumper between pins 7 and 8 to cause the board to respond to a logic 0 on

MEMEX, or between pins 9 and 10 to cause the board to respond to a logic 1. If the host system does not support MEMEX, leave pins 7 through 10 open. A jumper between pins 11 and 12 will cause the board to become active upon system reset. If this jumper is in place and a system reset has occurred, the memory in U1-U8 will become active and will remain active until the bank select port is written to. If the address is within the common memory boundaries, the memory in U1-U8 will become inactive so that the memory designated to be the common memory may be accessed.

EXAMPLE:

```
     J3
 1     2
 *     * -- > BOARD ACTIVE WHEN IOEXP = 0
 *     * -- > BOARD ACTIVE WHEN IOEXP = 1
 * --  * -- > JUMPER IN FOR COMMON ON BOARD
 *     * -- > BOARD ACTIVE WHEN MEMEX = 0
 *     * -- > BOARD ACTIVE WHEN MEMEX = 1
 * --  * -- > JUMPER IN FOR ACTIVE ON RESET
11      12
```

As shown above, the board will become active when an address within the common memory area is accessed or when a system reset occurs. Since pins 1-4 and 7-10 are left open, the logic levels of IOEXP and MEMEX are ignored.

J4 Bank Select Port Address

This header selects the address of the port through which bank switching is accomplished. The port address will be the hexadecimal equivalent of the jumper sequence. A jumper in place will assert a logic "0", while no jumper in place indicates a logic "1".

EXAMPLE:

```
     J4
 1     2
 *     * --- BIT 0
 *  --- * --- BIT 1
 *  --- * --- BIT 2
 *  --- * --- BIT 3
 *     * --- BIT 4
 *     * --- BIT 5
 *     * --- BIT 6
 *     * --- BIT 7
15      16
```

The binary equivalent of the jumper sequence is 11110001 binary of F1 hex, so the port address is F1 hex.

J5 Common Area Ending Address

This header determines the ending address for the common memory area. The upper boundary of the common area takes on the form XXFF hex, so the common memory may end at the top of any 256 byte page. A jumper in place asserts a logic "0", while no jumper in place indicates a logic "1".

EXAMPLE:

```
     J5
 1     2
 *     * --- BIT 0
 *     * --- BIT 1
 *     * --- BIT 2
 *     * --- BIT 3
 *  --- * --- BIT 4
 *     * --- BIT 5
 *     * --- BIT 6
 *     * --- BIT 7
15      16
```

The binary number represented by the jumpers is 11101111, or EF hex, so the common area will end at EFFF hex.

J6 Common Area Starting Address

This header determines the starting address for the common memory area. The common area lower boundary takes the form of XX00 hex, so common memory may begin with any 256 byte page. A jumper in place asserts a logic "0", while no jumper in place indicates a logic "1".

EXAMPLE:

```
     J6
 1     2
 *  --- * --- BIT 0
 *  --- * --- BIT 1
 *  --- * --- BIT 2
 *  --- * --- BIT 3
 *  --- * --- BIT 4
 *     * --- BIT 5
 *     * --- BIT 6
 *     * --- BIT 7
15      16
```

The binary number represented by the jumpers is 11100000, or E0 hex, so the common area will begin at E000 hex.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-RAM64	64K byte dynamic memory card with bank switch capability with Technical Manual	MK77764
MDX-RAM128	128K byte dynamic memory card with bank switch capability with Technical Manual	MK77765
MDX-RAM Technical Manual	Technical Manual only	4420291

IVE MD Series Special Functions

MDX-DEBUG
MK77950-0, MK77950-4

HARDWARE FEATURES

- STD-Z80 BUS compatible
- 4 MHz version available
- Serial I/O Channel
- 10K bytes of ROM contain the following firmware: DDT-80, ASMB-80

DEBUGGER FEATURES

- Z80 Operating System with debug capability
- Channelized I/O for versatility
- I/O peripheral drivers supplied
- ROM-based

TEXT EDITOR FEATURES

- Input and modification of ASCII Text
- Line and character editing
- Alternate command buffers for pseudo-macro command capability
- ROM-based

ASSEMBLER FEATURES

- Assembles all Z80 mnemonics
- Object output in industry-standard hexadecimal format extended for Relocatable and Linkable Programs
- Over fifteen pseudo-ops
- Two-pass assembly
- ROM-based

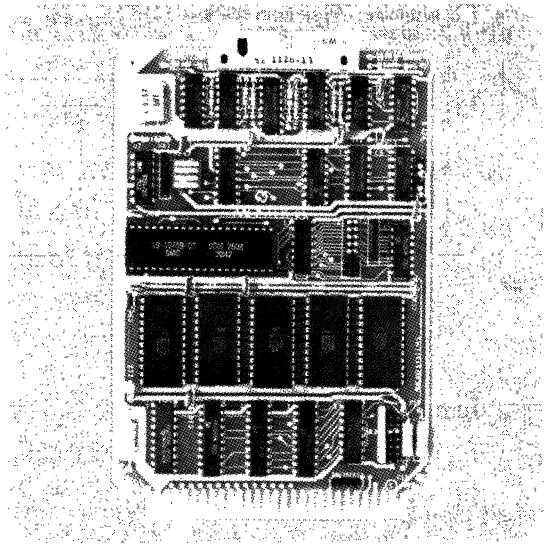
LINKING LOADER FEATURES

- Loads into memory both relocatable and non-relocatable object output of the assembler
- Loads Relocatable modules anywhere in memory
- Automatically provides linkage of global symbols between object modules as they are loaded
- Prints system load map
- ROM-based

HARDWARE DESCRIPTION

The MDX-DEBUG module has sockets for 10K bytes of masked ROM that are filled with a Z80 firmware package (DDT-80/ASMB-80). This module has a STD-Z80 BUS interface and is available in both 2.5 MHz and 4.0 MHz version. Included on-board is a fully buffered asynchronous I/O port capable of 110-19200 Baud rates. Serial data interfaces are available for 20 mA current loop (with reader-step control) and RS-232. The on-board Baud Rate Generator is selectable to all common Baud rates from 110 to 19,200 Baud. The address of the serial port is selectable via 6 on-board jumpers.

MDX-DEBUG BOARD PHOTO
Figure 1

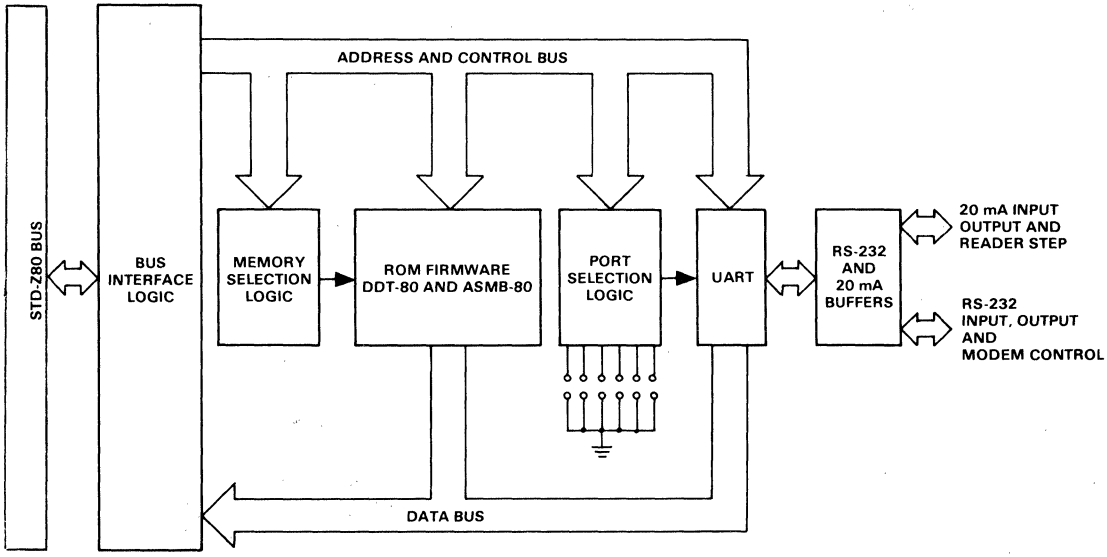


DEBUGGER DESCRIPTION

DDT-80 is the Operating System for the MDX-DEBUG Module, residing in a 2K ROM (MK34000 Series) on the module itself. It provides the necessary tools and techniques to operate the system, i.e., to efficiently and conveniently perform the tasks necessary to develop microcomputer software. DDT-80 is designed to support the user from initial design through production testing. It allows the user to display and update memory, registers, and ports, load and dump object files, set breakpoints, copy blocks of memory, and execute programs.

MDX-DEBUG BLOCK DIAGRAM

Figure 2



DDT-80 COMMAND SUMMARY

M s	-	Display and/or update the contents of memory location s.
M s, f	-	Tabulate the contents to memory locations s through f.
P s	-	Display and/or update the content of I/O ports.
D s, f	-	Dump the contents of memory locations s through f in a format suitable to be read by the L command.
L	-	Load, into memory, data which is in the appropriate format.
E s	-	Transfer control from DDT-80 to a user's program starting at location s.
H	-	Perform 16-bit hexadecimal addition and/or subtraction.
C s, f, d	-	Copy the contents of memory locations s through f to another location in memory starting at location d.
B s	-	Insert a breakpoint in a user's program (must be in RAM) at location s which transfers control back to DDT-80. This allows the user to intercept his program at a specific point (location s) and examine memory and CPU registers to determine if this program is working correctly.
Rx	-	Display the contents of the user registers.

The s, f, and d represent start, finish, and destination operands required for each command.

MEMORY, PORT AND REGISTER COMMANDS (M, P, R)

The M, P, and R commands provide the means for displaying the contents of specified memory locations, port addresses, or CPU registers. The M and P commands sequentially access memory locations or ports and display their contents. The user has the option of updating the content of the memory location or port. (Note some ports are output only and their contents cannot be displayed). The M command also gives the user access to the CPU registers through an area in RAM called the Register Map (discussed in the Execute and Breakpoint section below).

The M and R commands are used to tabulate blocks of memory locations (M) or the CPU registers (R). The M command will accept two operands, the starting and ending address of the block to be tabulated. The R command will accept either no operand or one. If no operand is specified, the CPU registers will be displayed without a heading. If an operand is specified, then a heading which labels the registers' contents will be displayed as well.

EXECUTE AND BREAKPOINT (E, B)

The E command is used to execute all programs, including aids such as the Assembler. The B command is used to set a breakpoint to exit from a program at some predetermined location for debugging purposes. At the instant of a breakpoint exit, the contents of all CPU registers are saved in a designated area of RAM called the Register Map. In the

Register Map, the register contents may be examined or mapped using the M command and a predefined mnemonic (or absolute address) of the storage location for that register (example :PC, :A, ..., :SP). The Register Map is also used to initialize the CPU registers whenever execution is initiated or resumed. Thus the E and B commands can be used together to initialize, execute, and examine the results of individual program segments.

The B command gives the user the option of having all CPU registers displayed when the breakpoint is encountered. This is done by entering a second operand to the B command. Otherwise, DDT-80 defaults to displaying the PC and AF registers. When all CPU registers are displayed, the format is the same as for the R command previously discussed.

LOAD, DUMP, AND COPY (L, D, C)

The L and D commands load and dump object files through the object I/O channel in standard Hex format. Checksums are used for error detection, and the addresses of questionable blocks are typed automatically while loading.

The C command will copy the contents of the memory block specified to another block of memory. There are no restrictions on the direction of the copy or on whether the blocks overlap.

HEXADECIMAL ARITHMETIC (H)

The H command is a dummy command used to allow hexadecimal addition and subtraction for expression evaluation without performing any other operation.

DDT-80 I/O CAPABILITIES

DDT-80 specifies I/O channels, designated 'Console', 'Object', and 'Source', to which any suitable devices may be assigned. The Channel Assignment Table is located in RAM where it may be examined or modified using the M command. The table addresses correspond to the I/O channels and the table contents correspond to the addresses of the peripheral driver routines. A channel which has a device assignment may have that device assignment changed using the M command. This is accomplished by merely modifying the table contents of that channel's table address to correspond to the new peripheral driver routine. A set of peripheral driver routines is supplied and listed below. This scheme also allows the user to write a driver routine for his own peripheral, load it into memory, and easily configure that peripheral into the system.

DDT-80 I/O PERIPHERAL DRIVERS

1. A serial input driver (usually a keyboard).
2. A serial output driver (usually a CRT or teletype typehead).
3. A serial input driver which sends out a reader-step signal (usually a teletype reader).
4. A serial output driver which forces a delay after a carriage return (usually a Silent 700 typehead).
5. A parallel input driver (usually for high-speed paper tape input).
6. A parallel output driver (usually for high-speed paper tape output).
7. A parallel output driver (usually for a line printer).

TEXT EDITOR DESCRIPTION

The Text Editor permits random-access editing of ASCII character strings. It can be used as a line or character-oriented editor. Individual characters may be located by position or context. The Editor works on blocks of characters which are typically read into memory from magnetic tape or paper tape. Each edited block can be output to magnetic tape or paper tape after editing is completed. While the primary application for the Text Editor is in editing assembly language source statements, it may be applied to any ASCII text delimited by "carriage returns".

The Editor has a macro command processing option. Up to two sets of commands may be stored and processed at any time during the editing process.

All I/O is done via the DDT-80 channels. The Editor can be used with the ASMB-80 Assembler and Loader to edit, assemble, and load programs in memory without the need for external media for intermediate storage.

The following commands are recognized by the Text Editor:

An -	Advance record pointer n records
Bn -	Backup record pointer n records
Cn dS1dS2d -	Change string S1 to string S2 for n occurrences
Dn -	Delete next n records
E -	Exchange current record with records to be inserted
I -	Insert records
Ln -	Go to line number n
Mn -	Enter command buffers (pseudo-macro)
N -	Print top, bottom, and current line number
Pn -	Punch n records from buffer
R -	Read source records into buffer
Sn dS1d -	Search for nth occurrence of string S1

ASSEMBLER DESCRIPTION

The Assembler reads Z80 source mnemonics and psuedo-ops and outputs an assembly listing and object code. The assembly listing shows address, machine code, statement number, and source statement. The object code is in industry-standard hexadecimal format modified for relocatable, linkable assemblies.

The Assembler supports conditional assemblies, global symbols, relocatable programs, and a printed symbol table. It can assemble any length program limited only by a symbol table size which is user-selectable. Expressions involving addition and subtraction are allowed. A global symbol is categorized as "internal" if it appears as a label in the program; otherwise it is an "external" symbol. The printed symbol table shows which symbols are internal and which are external. The Assembler allows the user to select relocatable or non-relocatable assembly via the "PSECT" pseudo-op. Relocation records are placed in the object output for relocatable assemblies (the Mostek object format is defined below). The Assembler can be run as a single-pass assembler or as a learning tool. (In this mode, global symbols and forward references are not allowed.)

The following pseudo-ops are recognized by the Assembler:

ORG -	program origin
EQU -	equate label
DEFL -	define label
DEFM -	define message
DEFB -	define byte
DEFW -	define word
DEFS -	define storage
END -	end statement
NAME -	program name definition
PSECT -	program section definition
GLOBAL -	global symbol definition
	Supports the following assembler pseudo-ops
EJECT -	eject a page of listing
TITLE -	place heading at top of each page
LIST -	turn listing on
NLIST -	turn listing off

RELOCATING LINKING LOADER DESCRIPTION

The Relocating Linking Loader provides state-of-the-art capability for loading programs into memory by allowing loading and linking of any number of relocatable and non-relocatable object modules. Non-relocatable modules are always loaded at their starting address as defined by the ORG pseudo-op during assembly. Relocatable object modules can be positioned anywhere in memory at an offset address.

The loader automatically links any relocator global symbols which are used to provide communication or linkage between program modules. As object programs are loaded, a table containing global symbol references and definitions is built up. At the end of each module, the loader resolves all references to global symbols which are defined by either the current or a previously loaded module. It also prints on the console device the number of defined global symbols that have been referenced. The symbol table can be printed to list all global symbols and their load addresses. The number of object modules which can be loaded by the Loader is limited only by the amount of RAM available for the modules and the symbol table. Space for the symbol table is allocated dynamically downward in memory from either the top of memory or from a specified address entered as an operand of the load command.

All I/O is done via the DDT-80 channels. Assemblies can be done from source statements stored in memory (by the Editor). The object output can be directed to a memory buffer rather than to an external device. Thus, assembly and loading can be done without external storage media.

The Loader prints the beginning and ending address of each module as it is loaded. The transfer address as defined by the END psuedo-ops is printed for the first module loaded. The Loader execute command (E) can be used to automatically start execution at the transfer address.

The Loader Commands are the following:

L offset -	load object module at address "off-set" plus program origin address
E -	execute loaded program at transfer address of first module
T -	print global symbol table

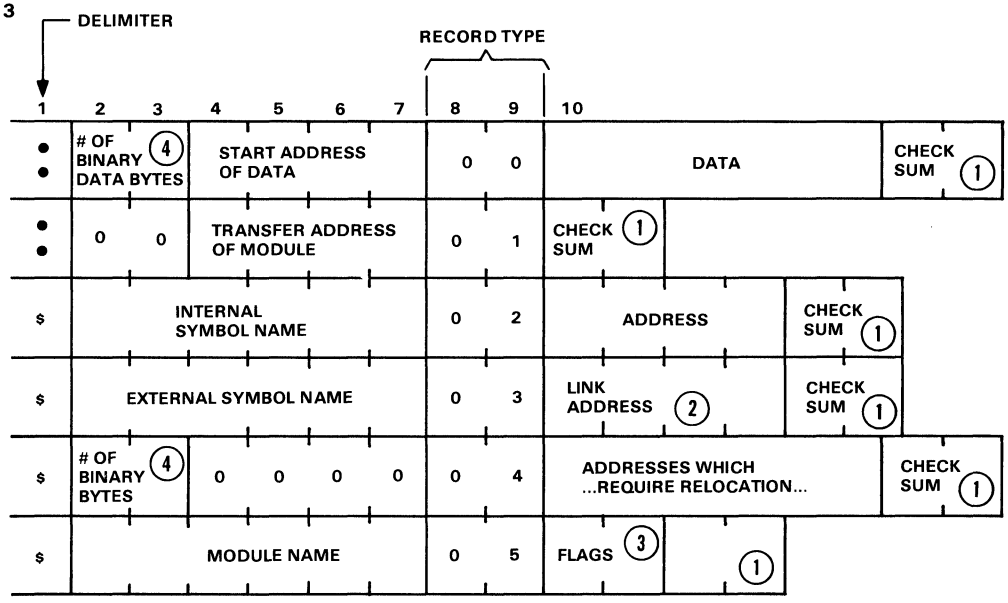
MOSTEK OBJECT OUTPUT DEFINITION

Each record of an object module begins with a delimiter (colon or dollar sign) and ends with carriage return and line feed. A colon (:) is used for data records and the end-of-file record. A dollar sign ($) is used for records containing relocation information and linking information. All information is in ASCII. Each record is identified by "type". The type is determined by the 8th and 9th bytes of the record which can take the following values:

00 - data
01 - end-of-file
02 - internal symbol
03 - external symbol
04 - relocation information
05 - module definition

OBJECT MODULE TYPES

Figure 3



NOTES:

1. Check Sum is negative of the binary sum of all bytes except delimiter and carriage return/line feed.
2. Link Address points to last address in the data which uses the external symbol. This starts a backward link list through the data records for that external symbol. The list terminates at 0FFFFH.
3. The flags are one binary byte. Bit 0 is defined as:
   0 - absolute module
   1 - relocatable module
4. Maximum of 64 ASCII bytes.

WORD SIZE

8 bits for PROM
5 to 8 bits for serial I/O

MEMORY SIZE

10K bytes of firmware

MEMORY ADDRESSING

2K blocks jumper-selectable for any 2K boundary within a given 16K block of the Z80 memory map. MDX-DEBUG has ROMS strapped every 2K beginning at C0000H.

I/O ADDRESSING

On board Serial I/O Port
Control Port: XXXXXX01
Data Port: XXXXXX00
Module and Reader Step Control Port: XXXXXX10
XXXXXX represents 6 strap-selectable address bits.

I/O TRANSFER RATE

110, 300, 600, 1200, 2400, 4800, 9600, 19200 BAUD

SERIAL COMMUNICATIONS INTERFACE

SIGNAL	BUFFERED FOR 20 mA Current Loop	BUFFERED FOR RS-232
Transmitted data	Output	Output
Received data	Input	Input
Data Terminal Ready (DTR)		Input
Request to Send (RTS)		Input
Carrier Detect (CDET)		Output
Clear to Send (CTS)		Output
Data Set Ready (DSR)		Output
Reader Step relay (RS)	Output (40 mA)	

SYSTEM CLOCK

MDX-DEBUG	2.5 MHz ± .05%
MDX-DEBUG-4	4.0 MHz ± .05%

SYSTEM INTERRUPT UNITS (SIU) = 0

STD BUS INTERFACE

Inputs: One 74LS load max.
Outputs: I_{OH} = -3 mA min. at 2.4 Volts
I_{OL} = 24 mA min. at 0.5 Volts

OPERATING TEMPERATURE

0°C to +60°C

POWER SUPPLY REQUIREMENT

+12 Volts ± 5% at 50 mA max.
-12 Volts ± 5% at 35 mA max.
+5 Volts ± 5% at 1.2 A max.

CARD DIMENSIONS

4.5 in. (114.3 mm) wide by 6.5 in. (165.1 mm) long
0.48 in. (12.2 mm) maximum profile thickness
0.063 in. (1.6 mm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/1CE5 WIRE WRAP Viking 3VH28/1CND5 SOLDER LUG Viking 3VH28/1CN5
Serial I/O	26-pin 0.1 in. grid	FLAT RIBBON Ansley 609-2600M DISCRETE WIRES Winchester PGB26A (housing) Winchester 100-70020S (contacts)

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-DEBUG	Module with 10K bytes of firmware and Operations Manual. No mating connectors. 2.5 MHz version.	MK77950-0
MDX-DEBUG-4	Module with 10K bytes of firmware and Operations Manual. No mating connectors. 4.0 MHz version	MK77950-4
	MDX-DEBUG Operations Manual only.	MK79611
	Program Source Listing of 10K byte firmware package (DDT/ASMB-80) including comments and flow charts. (Available free with purchase of either MDX-DEBUG Module.)	MK78536 and MK78534

* The DDT-80 and ASMB-80 listings are available directly from Mostek by filling out a copy of the Software Licensing Agreement and returning it with the appropriate payment of Customer Purchase Order to:

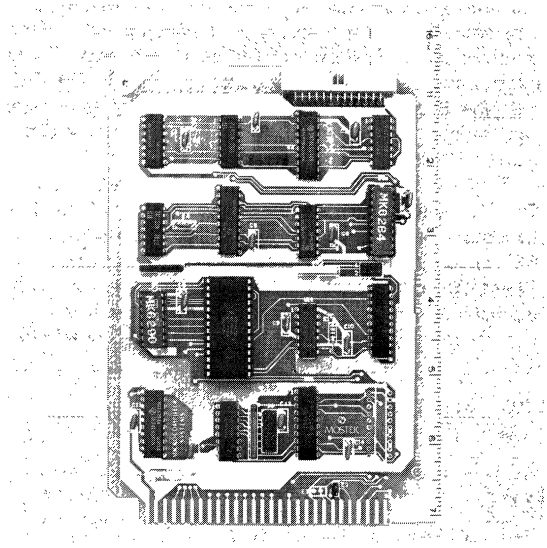
Mostek Corporation
Microcomputer Systems Div.
1215 West Crosby Road
Carrollton, Texas 75006

MDX-INT

FEATURES

- ☐ STD-Z80 Bus compatible
- ☐ User-programmable CTC provides:
  - Four external vectored interrupts
    or
  - Four cascadable counter/timer channels
    or
  - any combination of the above
- ☐ Z80 Daisy Chain Interrupt Expansion
  - Allows up to 40 interrupt devices
  - User selectable expansion of System Interrupt Units (SIU)
  - Required for systems over five SIUs
- ☐ Nonmaskable Interrupt Input
- ☐ All input/output signals buffered
- ☐ 2.5 and 4 MHz compatible
- ☐ +5 volt operation

MDX-INT
Figure 1



DESCRIPTION

The Interrupt-Timer Expansion Module, MDX-INT (MK77967), is designed to be a versatile multimode unit. It provides external interrupt expansion of up to four lines, a nonmaskable interrupt input, up to four cascadable timer channels, and internal interrupt expansion capability of up to 40 System Interrupt Units. All interrupts are Z80 compatible with full Mode 2 interrupt capability.

The MDX-INT permits up to four external interrupt inputs. This is possible by programming the MK3882 Counter Timer to function as an interrupt controller. When programming the CTC, the selected input channel is programmed to be in the counter mode with count set to one. The active edge as well as the interrupt vector locations are also specified by the user's program. When an active input occurs, a Mode 2 interrupt is generated by the CTC and the MDX-CPU can vector directly to a service routine. After the interrupt, the CTC down counter is reloaded automatically with a count of one and the CTC begins looking for another active edge. Therefore, once initialized, a channel will provide external interrupt capability automatically.

Up to four channels can be used to provide external interrupts. Input is provided through the TRG0 to TRG3 lines for channels zero through three. When multiple channels are used, priorities are resolved within the CTC if more than one interrupt request is made simultaneously. Each channel has a unique vector address and each channel can be masked independently by disabling that channel's local interrupt.

The nonmaskable interrupt is also provided as an input through this board. This line is tested by the MDX-CPU at the end of each instruction. It has priority over the normal interrupt and cannot be disabled under software control. Its usual function is to provide response to signals requiring immediate response, such as an impending power failure.

Each of the four CTC channels has an 8-bit Prescaler and 8-bit Down Counter that allows the circuit to be used as a counter of a timer rather than an interrupt generator. In the counter mode, a Zero Count output is provided that allows cascading of successive counters. In the counter mode, external inputs can be counted automatically by the CTC and interrupt the processor after a predefined number of

counts. In the timer mode, the CTC can generate timing intervals that are integer multiples of the system clock period. The Zero Count output can generate a uniform pulse train of the precise period. Therefore, precise time measurements can be made that are a function of a crystal clock's accuracy and stability.

The MDX-INT also provides internal interrupt expansion through a concept of System Interrupt Units (SIU). The interrupt system of the STD-Z80 compatible CPUs will allow up to five System Interrupt Units without need of expansion. The MDX-INT has circuitry to allow expansion of board with up to 40 SIUs. It must be the last card (the lowest priority) in the interrupt daisy chain. An SIU is defined as an interval of time equivalent to the worst-case propagation delay of the priority daisy chain through an MD board. A board with one interrupting peripheral component, such as an MDX-SIO, has one SIU. A board with two interrupting peripheral components, such as an MDX-PIO, has two SIUs. A board with no interrupt capability has zero SIUs.

The SIU expansion circuitry on the MDX-INT card monitors the data bus and PCI lines. Wait states are added during the RETI opcode to allow the PCI and PCO lines to stabilize. The Wait state generator on the MDX-INT is enabled when an interrupt is pending or under service and will insert a predetermined number of wait states for 15, 25, or 40 SIUs.

SYSTEM INTERRUPT UNITS

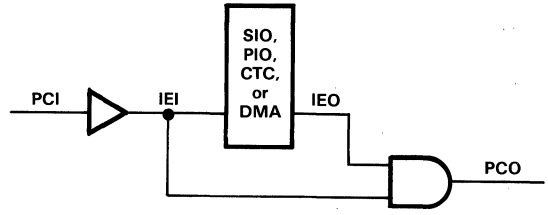
Table 1

Card	SIU's
MDX-A/D12	1
MDX-A/D8	1
MDX-AIO	0
MDX-CPU1/1A	1
MDX-CPU2/2A	1
MDX-CPU3	1
MDX-CPU4	1
MDX-D/A8	0
MDX-D/A12	0
MDX-DEBUG	0
MDX-DRAM8/16/32/64/128	0
MDX-EPROM	0
MDX-EPROM/UART	0
MDX-FLP/FLP2	1
MDX-INT	1
MDX-ISIO	1
MDX-MATH	1
MDX-MODEM	1
MDX-PIO	2
MDX-SASI1/2	1
MDX-SC/D	1
MDX-SIO/SIO2	1
MDX-SRAM4/8/16	0
MDX-SST	0
MDX-UMC/UMC2	0

The number of SIUs that the system can handle is hardware selectable on-board. A Block Diagram of the MDX-INT board is shown in Figure 3.

WORST-CASE PRIORITY CHAIN INTERFACE PROPAGATION DELAY

Figure 2



2.5 MHz	20 nsec	220 nsec	20 nsec
4.0 MHz	20 nsec	160 nsec	20 nsec

4.0 MHz SIU = 200 nsec = 20 + 160 + 20
2.5 MHz SIU = 260 nsec = 20 + 220 + 20

CTC Address Decode

This address logic compares the six most significant I/O address bits (A7-A2) with the J4 address location jumper. If these are equal, and an I/O request has been made to the board, then the CTC will be enabled. A0 and A1 are decoded directly by the CTC and used to select the specific CTC channel, as shown in Table 2.

MDX-INT BOARD PORT ASSIGNMENTS

Table 2

A1	A0	CTC Channel
0	0	0
0	1	1
1	0	2
1	1	3

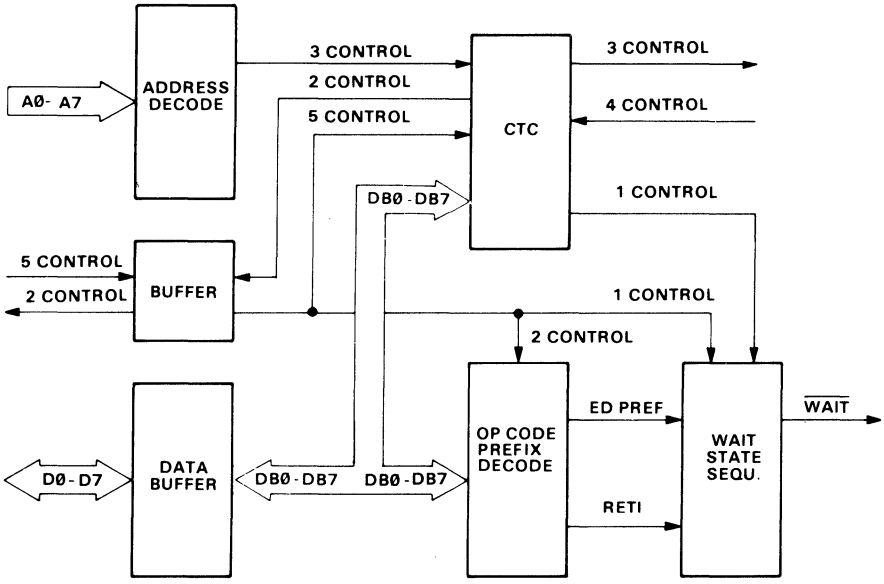
Bus and Buffer Control

All signals are buffered going to or coming from the board.

Data Buffering

Data signals are buffered by a SN74LS245 octal transceiver. The turnaround of the bus is handled either by the decode of an I/O Read or by a Read of the interrupt vector.

MDX-INT BLOCK DIAGRAM
Figure 3



Op-Code Prefix Decode

The Op-Code Prefix Decoder searches the data bus for two things: an ED two-byte instruction, and an RETI instruction. When an ED two-byte instruction is decoded, a WAIT state is inserted. Next the data is inspected for a 4D, the second part of the RETI. If a 4D is present, additional WAIT states are added corresponding to the number of SIUs selected. If not, no additional wait states are added.

WAIT State Sequencer

This micro-programmed sequencer is a state controller designed to add wait states in conjunction with the op-code prefix decoder. It allows the decode of a RETI (ED-4D) instruction and the propagation of a correct PCI to all boards in the system. If WAIT states are not required, the interrupt expansion capability can be disabled by removing jumper E2. This prohibits WAIT states from being introduced on the bus.

CTC

The MK3882 is a flexible Z80 peripheral that allows operation as either a counter or timer on to 4 channels. The outputs of the CTC are buffered and wired to connector J2. The outputs are the ZC/TO from channels 0 through 2. Clock and Trigger inputs are buffered and provided for all four channels.

ADDRESS DECODE

Table 3 shows the assignment of address decoder select. A pullup resistor is on the board which selects a logical 1 in the address bit field. Each address bit that is to be programmed to a zero must have a jumper installed.

IVE

JUMPER ADDRESS PIN ASSIGNMENTS
Table 3

Address Bit	J4 Jumper Pin
A7	1- 2
A6	3- 4
A5	5- 6
A4	7- 8
A3	9-10
A2	11-12

SIU Selection

The pins 1 to 2 and 3 to 4 of J3 select the maximum SIUs in a system. Table 4 shows the options of system, speed selection, and jumpers required.

One More WAIT State

If there is an extra Wait state in the CPU for memory cycles, the jumper for one more (at J3 5-6) must be removed.

SIU JUMPER ASSIGNMENTS

Table 4

Max SIU's		J3 Jumper Pins
2.5 MHz	**4 MHz**	
15	14	3-4 and 1-2
25	24	3-4
40	34	NONE

SPECIFICATIONS

ELECTRICAL

System Clock

Part Number	Board	Min.	Max.
MK77967	MDX-INT	250 KHz	2.5 MHz
MK77967-4	MDX-INT-4	250 KHz	4.0 MHz

Bus Interface, STD-Z80 Compatible

Inputs: One 74LS load Max.
Outputs: I_{OH} = -15 mA Min. at 2.4 Volts
I_{OL} = +24 mA Min. at 0.5 Volts

Power Supply Requirements

+ 5 Volts ± 5% at 1.2 A max

Word Size

DATA: 8 bits

I/O ADDRESS: 8 bits using 4 ports with 6 bits jumper option

Operating Temperature Range

0° to 60° Centigrade

MODE OF OPERATION

Interrupts are handled to provide prioritized interrupts compatible with the STD-Z80 Bus requirements, and be capable of polled operation when interrupts are disabled for the CTC. The interrupt expander is code-transparent to software when the CTC is not used.

SIU's

1

MECHANICAL

Card Dimensions

4.5 in. (11.43 cm) wide by 6.5 in. (16.51 cm) long
0.48 in (1.22 cm) maximum profile thickness
0.062 in. (0.16 cm) printed circuit board thickness

Connectors

Function	Configuration	Mating Connectors
STD Bus	56 Pin dual 0.125 in. centers	Printed Circuit Viking 3VH28/1CE5 Wire Wrap: Viking 3VH28/1CND5
		Solder Lug: Viking 3VH28/1CN5
Parallel I/O	26 pin dual 0.100 in. grid	Flat Ribbon: Ansley 609-2600M Discrete Wires: Winchester: PGB26A (housing) Winchester: 100-70020S (contacts)

CTC I/O PIN ASSIGNMENTS

1	CLK/TRG0	14	GND
2	ZCT/TO0	15	GND
3	CLK/TRG1	16	GND
4	ZCT/TO1	17	GND
5	CLK/TRG2	18	GND
6	ZCT/TO2	19	GND
7	CLK/TRG3	20	GND
8	N.C.	21	GND
9	/NMI	22	GND
10	N.C.	23	GND
11	N.C.	24	GND
12	N.C.	25	GND
13	N.C.	26	GND

ORDERING INFORMATION

Designator	Description	Part Number
MDX-INT	MDX-INT Interrupt Expander Module with Technical Manual (2.5 MHz)	MK77967
MDX-INT	MDX-INT Interrupt Expander Module with Technical Manual (4.0 MHz)	MK77967-4
MDX-INT Technical Manual	Technical Manual only	4420069

MDX-SC/D
MK77963-0, MK77963-4

FEATURES

- ☐ STD-Z80 BUS compatible
- ☐ Provides an operator interface; switches and lamps
- ☐ 10K x 8 EPROM (2716's not included)
- ☐ Dual-purpose card, memory and/or diagnostic interface
- ☐ Interrupt-driven programmability
- ☐ Strap-selectable address
- ☐ 4 MHz Option
- ☐ Fully-buffered for MD Series expandability
- ☐ Diagnostic software package

DESCRIPTION

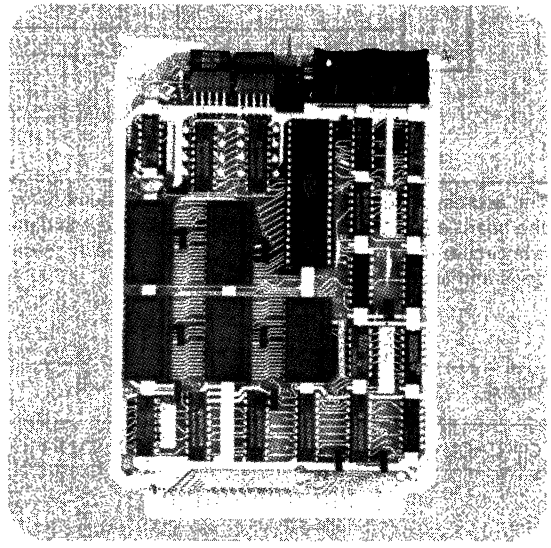
Designed as a system controller/diagnostics board, it provides the user with Reset/Interrupt lines to the CPU, as well as the capability to run tests placed in EPROM on board, to verify the operation of other MD boards on the bus. The board is equipped with sockets to contain up to 10K x 8 of EPROM memory (5-2716's) as shown in the Block Diagram. The EPROM's can contain the diagnostic programs necessary for testing the modules or can contain user application programs.

The EPROM memories can be positioned to start on any 2K boundary within a 16K block of memory via a strapping option provided on the board.

For the 4MHZ version, circuitry is provided to force one wait state each time on-board EPROM's are accessed.

A three-position switch is provided at the top of the board.

MDX-SC/D BOARD PHOTO
Figure 1

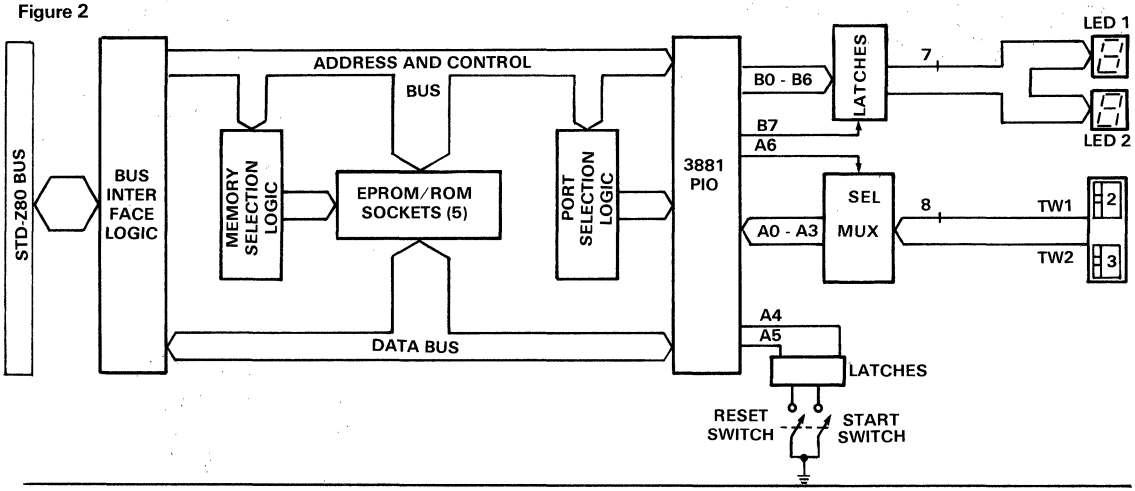


The switch is springloaded to the OFF position. The RESET position initializes the hardware and software diagnostics elements. The START position begins the diagnostic test which had been preset by the thumbwheel switches, also on the top of the board. At the conclusion of the test, the results are displayed by the LED Readouts. Data transfers from the switches to the bus and from the bus to the readouts are accomplished by the MK3881 PIO.

The PIO also permits total interrupt control so that full usage of the CPU interrupt capabilities can be utilized during data transfers. The PIO provides vectored interrupts and maintains the daisy-chain, priority interrupt logic compatible with the STD-Z80 BUS.

MDX-SC/D BLOCK DIAGRAM

Figure 2



The address decoding, interface and bus management for the board are performed by the address decode and data bus circuit. The PIO ports have two addresses each; these are summarized below.

	PORT A	PORT B
DATA	XXXX X000	XXXX X010
CONTROL	XXXX X001	XXXX X011

The XX symbols stand for the upper five bits of the I/O channel address. These bits are jumper-selectable on the board in order to provide address-selectable, fully decoded ports.

MEDEX-80

MEDEX-80 is a diagnostic software package designed to operate with the MDX-SC/D card's thumbwheels, switch and display. The package consists of a control monitor, MDX-SC/D card interface handler, and numerous diagnostic tests for the MDX series cards. The package can operate as a stand-alone program or can be integrated with a user program. MEDEX-80 is designed to allow user-developed diagnostics to be adapted as extensions to the package.

WORD SIZE

8 bits

MEMORY SIZE

10K bytes of 2716 memory (2716's not included)

MEMORY ADDRESSING

EPROM - 2K blocks jumper-selectable for any 2K boundary within a given 16K boundary of Z80 memory map.

MEMORY SPEED REQUIRED

Memory	Access Time	Cycle Time
* 2716	450 ns	450 ns

* Single 5-Volt type required

INPUT/OUTPUT

Controlled by spring-loaded RESET/START switch with center off.
Test selected by two thumbwheel switches.
Test results indicated by two 7-segment LEDs.

INTERRUPTS

Vectored interrupts generated. Interrupt vector programmable upon initialization. Daisy-chained interrupt priority. Selected bit channels can be masked out under program control.

SYSTEM CLOCK

MDX-SC/D	2.5 MHz ± .05%
MDX-SC/D-4	4.0 MHz ± .05%

STD BUS INTERFACE

Inputs: One 74LS Load max.
Outputs: I_{OH} = -3mA min. at 2.4 Volts
I_{OL} = 24mA min. at 0.5 Volts

OPERATING TEMPERATURE RANGE

0°C to 60°C

POWER SUPPLY REQUIREMENTS

+5 Volts ± 5% at 1.2 A max.

CARD DIMENSIONS

4.5 in. (114.3 mm) high by 6.50 in. (165.1 mm) long
0.48 in. (12.2 mm) maximum profile thickness
0.062 in. (1.6 mm) printed-circuit-board thickness

CONNECTORS

Function	Configuration	Mating Connector
STD-Z80 BUS	56-pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/1CE5 WIRE WRAP Viking 3VH28/1CND5 SOLDER LUG Viking 3VH28/1CN5

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-SC/D	Module with Operation Manual, 2.5 MHZ version	MK77963-0
MDX-SC/D-4	Module with Operation Manual, 4.0 MHZ version	MK77963-4
	MDX-SC/D Operation Manual Only	MK79678
MEDEX-80	Diagnostic software for various MDX Series cards, distributed on diskette in Z80 Assembly source form	MK77968

MDX-PFD

FEATURES

- Detects loss of AC power after one half cycle
- Detects brownout condition (AC below 95 V)
- Contains logic to sequence pushbutton reset and non-maskable interrupt
- Battery backup for up to five days via rechargeable Ni Cads
- STD-Z80 Bus compatible

DESCRIPTION

The MDX-PFD board (MK77979) and voltage transformer module provide for power-up/power-down sequencing for use in conjunction with the battery backed MDX-BCLK and MDX-BRAM boards. A block diagram is shown in Figure 2. Figure 3 shows the MDX-PFD timing.

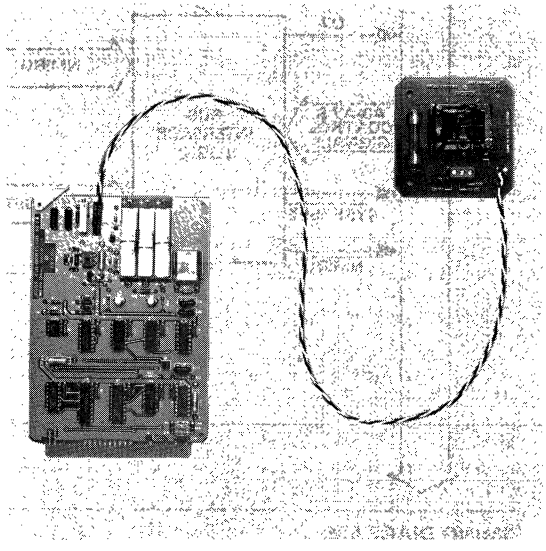
The Voltage Transformer Module is mounted separately from the card cage containing the MDX-PFD board. Its purpose is to provide a low voltage AC signal which is derived from the 115/230 volt line supplying the main system power. It contains a terminal strip for 115/230 VAC power, a fuse, and a transformer. A cable and connector are provided for connection to the MDX-PFD board.

Rectified AC voltage from the voltage transformer module is divided through a resistive network and used as an input to a comparator (U2) with an internal reference. The comparator "peak detects" the adjustable AC input which is factory set to approximately 95 VAC as a brown-out detection level. The comparator output triggers a retriggerable CMOS one shot (½ of U3) with a period of 13 mSec. This output generates the NMIRQ signal, and it also triggers a second one shot (½ of U3) which inhibits the first one shot for a period of 5 mSec. This second delay is necessary to allow a software power-down subroutine to complete before SYSRESET is generated.

POWER DOWN SEQUENCE

Detection of power failure immediately sets the NMIRQ flip-flop (½ of U5) causing non-maskable interrupt (NMIRQ) to go low, which in turn vectors the processor to location 66 H, the entry point of a user supplied power-down subroutine. Table 1 shows an example of a power-down subroutine.

MDX-PFD
Figure 1



ADDRESS DECODE AND CONTROL

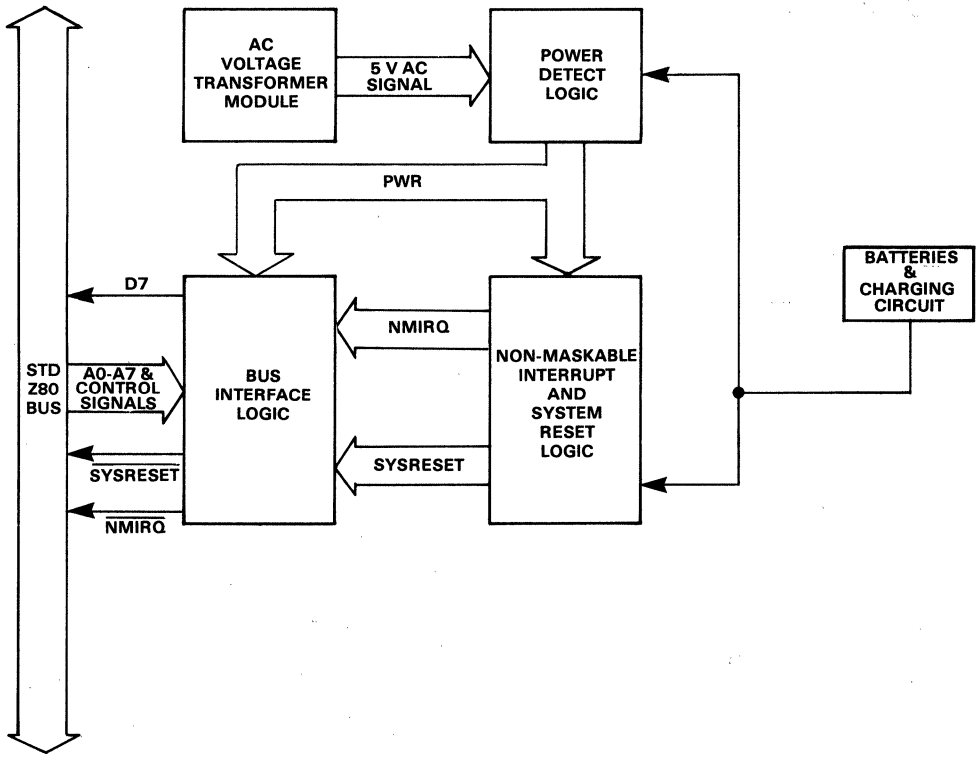
When the interrupt port 0F7H (PFD board address) is read by the power-down subroutine, a 0 in data bit 7 (D7) indicates power fail condition which a 1 indicates no power failure. The last instruction of the power-down subroutine should be a write to port address 0F7H. This will set the SYSRESET flip-flop (½ of U5) and cause SYSRESET to go low. The above conditions will be maintained by battery backed up CMOS logic until power is restored.

POWER UP SEQUENCE

When the power is detected by the MDX-PFD voltage comparator circuit, a reset signal is released from a counter (U6), allowing it to count. The counter then releases NMIRQ, nonmaskable interrupt request, causing it to go high after approximately 130 mSec. Next the counter releases SYSRESET, causing it to go high after approximately 260 mSec after AC power is detected, thus allowing normal system operation to begin the power up subroutine starting at address 00H or E000H. These delays are necessary in order to allow DC power to stabilize after AC power has been restored. Loss of power at any time before system reset goes high will cause the counter to be reset and the 130/260 mSec timer sequence to be repeated after AC power is again restored.

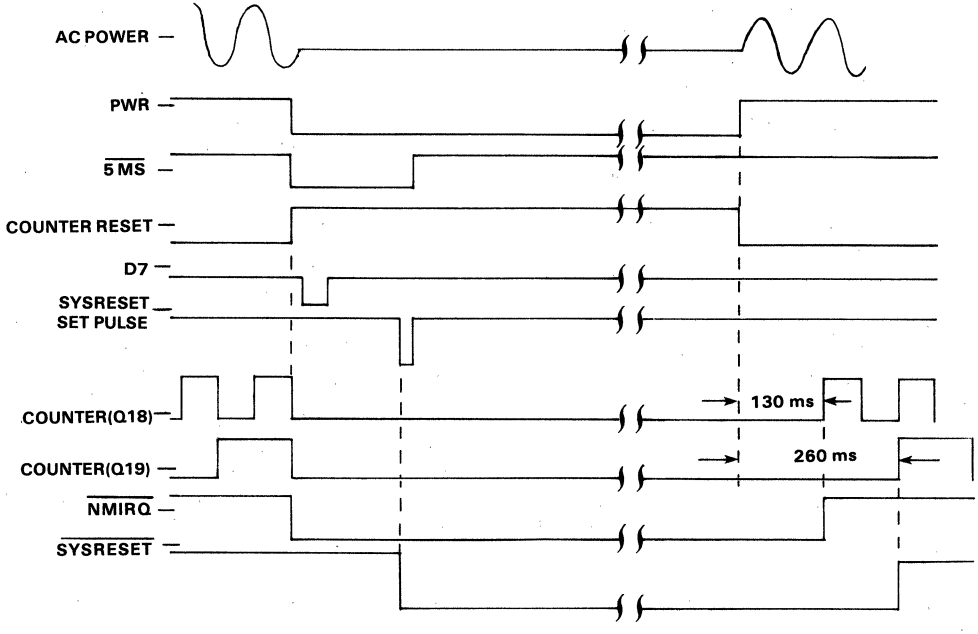
MDX-PFD BLOCK DIAGRAM

Figure 2



TIMING DIAGRAM

Figure 3



EXAMPLE OF POWER-DOWN SUBROUTINE

Table 1

```
ORG     0066H                   ;POWER FAIL TRAP
        •
        •
        •
        IN      A, (0F7H)       ;TEST FOR POWER-DOWN CONDITION FROM MDX-PFD
        AND     080H            ;IS BIT 7 SET?
        JP      NZ, NOFAIL      ;JUMP IF SO
        •
        •
USER POWER FAIL ROUTINE         (EG:SAVE REGISTERS VARIABLES ETC.)
        •
        OUT     (0F7H), A       ;INSTRUCT MDX-PFD TO ASSERT SYSRESET LOW
NOFAIL  •                       ;OTHER NMI INTERRUPT SERVICE ROUTINES
        •
        •
        •
```

BATTERY BACKUP

Three AAA size nickel-cadmium rechargeable cells are provided to supply standby power during primary AC power outages. These batteries will supply power for the logic for a minimum of five days when operated at 25 C. The batteries are charged from both +12 V DC (J1 pin 55) via CR5 and R6 and +5 V DC (J1 pin 1 and 2) via CR4 and R4. Zener diode CR1 serves to keep VBATT from going above 5.6 V DC when J3 pins 1 and 2 are not connected. If +12 V DC is not available, the batteries may be trickle charged from +5V DC alone by installing the jumper between J4 pin 1 and pin 2. Note, however, because of the reduced charging potential in this configuration, battery supply may not last the full five days.

Depending on the initial condition of the batteries, the initial charging current is 18 mA to 32 mA, the trickle charging current is 9 mA to 13 mA. When batteries are being charged with 5 volts only, the charge rate is approximately 4 mA.

STRAPPING OPTIONS

The CPU jumpers are used to activate the power up and pushbutton reset logic provided on the MDX-PFD board if CPU1 board is used as the microprocessor. Figure 4 shows the jumper configuration for use with CPU 1 and CPU 2 processors. The board is shipped with a jumper between J5 pins 1 and 2.

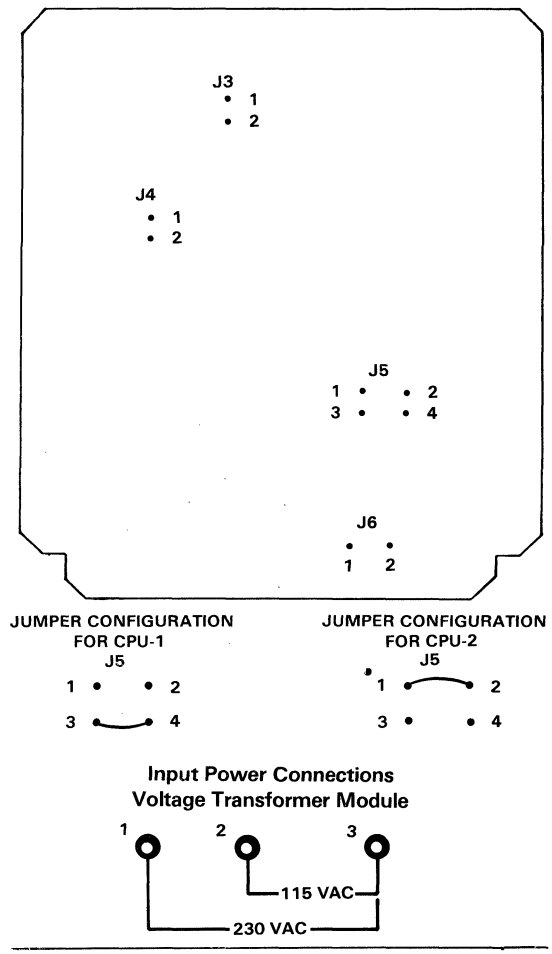
BATTERY CIRCUIT JUMPERS

The MDX-PFD board is shipped with the batteries disconnected from the logic and charging circuit. In order to connect the batteries, place a jumper between J3 pins 1 and 2.

The board is also shipped with no jumper between J4 pins 1 and 2. If +12 volts are not available for battery charging, a jumper should be placed between J4 pins 1 and 2.

JUMPER CONFIGURATIONS

Figure 4



SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

STD BUS Compatible

A0-A7 Inputs

I_{IL} = -.2 mA max at .4 V
I_{IH} = 20 μA max at 2.7 V

$\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$ Inputs

I_{IL} = -.2 mA max at .4 V
I_{IH} = 20 μA max at 2.7 V

$\overline{NMIRQ}$, $\overline{SYSRESET}$ Open Collector Output

I_{OL} 24 mA min at .5 V

D7 Tristate Output

I_{OL} 24 mA at .5 V

AC (Input to MDX-PFD)

5 VAC RMS

Power Supply Requirement

5 V ± 5% at 130 mA max.
12 V ± 5% at 45 mA max.

Operating Temperature

0° to 60°C
0° to 25°C for 5 day battery operation

MECHANICAL SPECIFICATIONS

Card Dimensions (MDX Card)

4.5 in. (11.43 cm) high by 6.50 in. (16.51 cm) long
0.675 in. (1.71 cm) maximum profile thickness
0.062 in. (0.16cm)printed circuit board thickness

Card Dimensions (Voltage Transformer Module)

3.00 in. (7.62 cm) wide by 3.00 in. (7.62 cm) long
0.062 (0.16 cm) printed circuit board thickness

Connectors

Function	Configuration	Mating Connector
STD Bus	56 pin dual read out 0.125 in. centers	Printed Circuit Viking 2VH28/1CE5
		Wire Wrap Viking 3VH28/1CND5
MDX-PFD Card to Voltage Transformer Module	AMP87551-2 2 pin rt. angle header strip on MDX-PFD Board	AMP87499-3 cable connector on Transformer Module

ORDERING INFORMATION

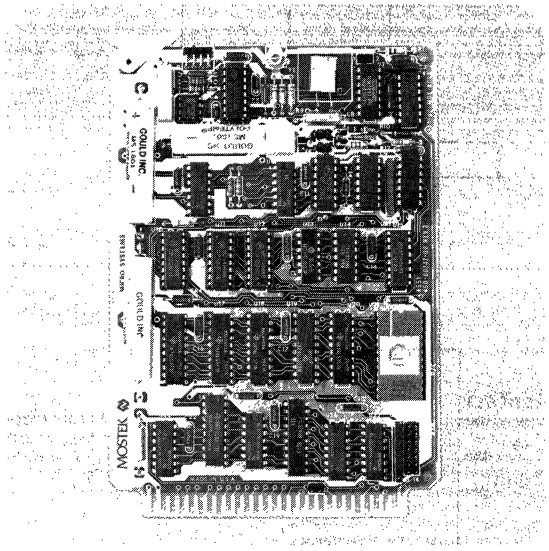
Designator	Description	Part Number
MDX-PFD	MDX-PFD Power Fail Detect Module XFMRS Cable with Technical Manual	MK77979
MDX-PFD Technical Manual	MDX-PFD Technical Manual only	4420046

MDX-BCLK

FEATURES

- ☐ STD Bus Compatible
- ☐ 24 hour clock
- ☐ Provides seconds, minutes, hours, day, and month in BCD format
- ☐ Contains Leap and non-Leap year Julian calendars
- ☐ Retains clock/calendar functional capability without system power for five days on fully-charged batteries
- ☐ Provides Interrupts at 62.5 ms (16 Hz), one sec, one min, and one hour intervals to CTC on MDX-CPU2 via user-supplied cable
- ☐ Accuracy of ten seconds per month at 25°C
- ☐ Power backup is provided via rechargeable batteries
- ☐ 2.5 MHz and 4.0 MHz operation
- ☐ 2 Port addresses

MDX-BCLK
Figure 1



DESCRIPTION

The MDX-BCLK module provides seconds, minutes, hours, days, and month data in BCD format (24 hour). Real-time interrupt capability is provided via the CTC on the MDX-CPU2 or MDX-INT module. The module is accurate to 10 seconds per month at 25°C. The battery-backup feature retains clock/calendar functional capability without system power for five days on fully charged batteries.

The board consists of nine main elements: address buffers, address/bus control decode logic, bi-directional data buffers, power detect circuitry, backup batteries, clock control register, clock data latches, CMOS clock circuit, and clock set logic. The address/bus control decode logic controls the direction of the bi-directional data buffers and the enabling of the clock control register, data clock latches, and the clock set logic. The power detect circuitry detects system power failure and prevents the TTL from interacting with the battery-backed-up CMOS. The clock control register selects the desired operation of the CMOS clock circuit (i.e., read seconds, set seconds, read minutes, and so on). The clock data latches, in conjunction with the clock control register, enable and select the desired clock data (seconds, minutes, hours, day of the month, and month). The CMOS clock circuit is a battery-backed-up clock which retains data for five days on fully charged batteries. The clock set logic allows clock setting through the STD BUS interface.

STRAPPING OPTIONS

Port Address Configuration Strapping

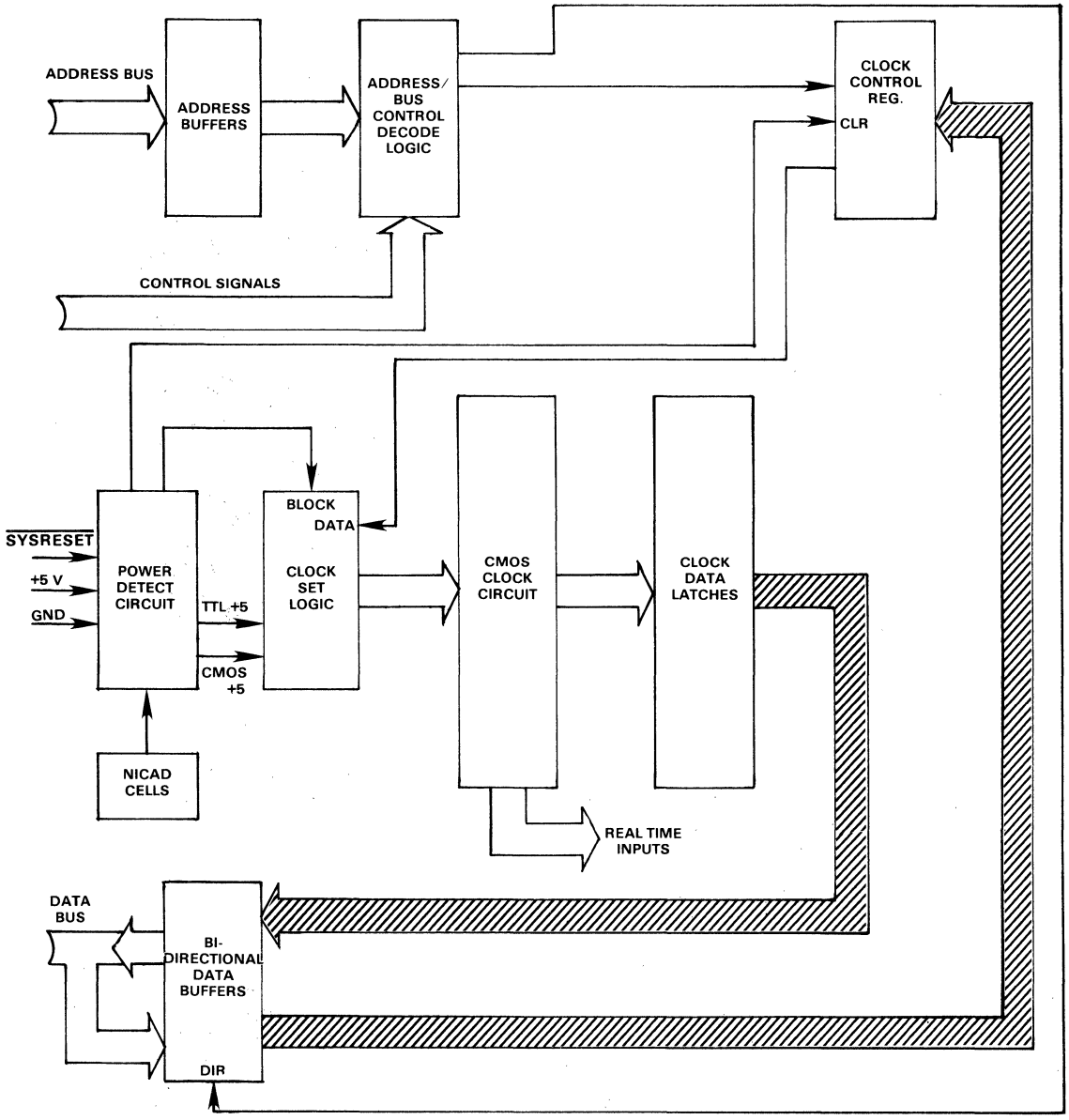
The MDX-BCLK module port address block permits port selection and system flexibility. Address selection is accomplished by installing the proper straps on Header J5. Installing a strap is equivalent to selecting the particular address bit to zero. In addition, the board can only be port addressed on even bit increments (i.e., 00H, 02H, 04H...). Figure 3 is an example of a port addressed at 80 H.

External Clock Input

Header J3 is provided to input a clock frequency other than the on-board 1 Hz frequency and is primarily intended for testing purposes. Header J3 must be strapped for module functional capability, and is strapped before shipment.

MDX-BCLK FUNCTIONAL BLOCK DIAGRAM

Figure 2



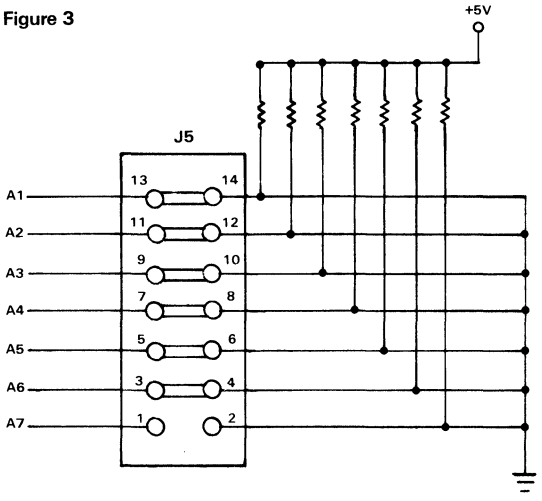
J5 PORT ADDRESS SELECTION

Table 1

PINS	ADDRESS BITS
13-14	A1
11-12	A2
9-10	A3
7- 8	A4
5- 6	A5
3- 4	A6
1- 2	A7

ADDRESS STRAPPING EXAMPLE FOR PORT ADDRESS 80H

Figure 3



Connector J2 Pinout for External Clock Frequencies

External clock frequencies are provided to enable the CTC on the MDX-CPU2 or MDX-INT to provide accurate real-time interrupts at 62.5 msec, one sec, one min, and one hour time intervals. The desired time interval or intervals are selected by connecting the appropriate pins of the 26 pin header on the MDX-CPU2 to the 8 pin header on the MDX-BCLK module. A twisted pair connection should be used where one conductor is ground (See Table 2 and Table 3).

J2 PINOUT

Table 2

FUNCTION	PIN	PIN	FUNCTION
GND	1	2	62.5 msec (16 Hz)
GND	3	4	1 sec
GND	5	6	1 min
GND	7	8	1 hour

MDX-CPU2 CTC HEADER PINOUT

Table 3

FUNCTION	PIN	PIN	FUNCTION
C/T 0	1	2	ZC 0
C/T 1	3	4	ZC 1
C/T 2	5	6	ZC 2
C/T 3	7	8	NC
$\overline{\text{NMI}}$	9	10	NC
NC	11	12	NC
NC	13	14	GND
GND	15	16	GND
GND	17	18	GND
GND	19	20	GND
GND	21	22	GND
GND	23	24	GND
GND	25	26	GND

Battery Disconnect

The MDX-BCLK module has on-board rechargeable batteries. Pins 3-4 on header J4 allow disconnection of these batteries when the system is to be powered down and the clock function is not needed. Removing the jumper disconnects the batteries, thus preventing discharge.

The MDX-BCLK module can function with a 5 volt supply because the 12 volt supply is only used to decrease battery charge time. In order to select 5 volt only operation, pins 1 and 2 must be strapped on Header J4. Note: this mode increases the charge time to 36 hours for a full charge at 25°C.

Power Fail Ciruitry

The power fail detection circuit senses when the 5 volt supply to the BCLK falls below 4.7 volts. If the 5 volt line remains below this threshold for more than 9 microseconds, access to the board will be disabled. The 9 microsecond delay is a result of the RC time constant used in the SPF, system power fail circuitry. This circuitry is composed of the ICL 8211, U1 (voltage reference); an MC14538B, U2 (dual multi-vibrator); and an MC14013B, U7 (D-type flip flop). The battery-backed CMOS clock circuitry remains active during SPU; access only to read or write is inhibited. The system power up, (SPU), signal is used to re-enable board access and may be active from 4.7 volts typical to 4.85 volts maximum. The SPU one shot U2, has a time-out of 5 ms to allow for stable power supply voltage before enabling board access. Because of the level at which the BCLK module becomes re-enabled, the user must set the power supply voltage at the board bus interface, connector J1, to a minimum of 4.9 volts (5 volts recommended).

Adjustment of R2 establishes the voltage level at which the MDX-BCLK module recognizes power fail. This level is factory set at 4.7 volts and should not be changed. If R2 requires adjustment, the following procedure should be used:

a) Adjust a power supply such that 4.7 volts is present on the 5 volt input (Pins 1 and 2 on J1).
b) Connect an oscilloscope or a voltmeter to the output of the ICL8211 (Pin 4 of U1).
c) Adjust R2 until the voltage on Pin 4 of the ICL8211 goes to a high level (greater than 2.4 V).
d) Slowly adjust R2 in the opposite direction until the voltage goes to a low level (less than .7 V).
e) The ICL8211, U1 provides 50 mV hysteresis typically between system power up signals which may be altered by varying the value of R4.

WARNING: Mostek does not assume any responsibility for module failure if this adjustment is made.

FUNCTIONAL SOFTWARE DESCRIPTION

The MDX-BCLK interface consists of two ports. When a write (OUT) is performed to the low order port (XXXXXXX 0) the control register is accessed. When a read (IN) is performed from the low order port, the desired clock data is accessed. Two successive writes (OUT) to the high order port (XXXXXXX 1) increment a particular counter depending on the state of the control register. Reading the high order port has no function and irrelevant data will be obtained.

Control Data Register

The control register on the MDX-BCLK module consists of eight bits whose functions are described in Table 4. In order to read and set clock data, the appropriate bits in the control register must be set. Writing FFH would set all bits and writing 00H would clear all bits of the control register.

D0-Clock Reset and Disable

When the D0 bit of the control register makes a transition from low to high (positive edge), the clock resets to zero (00:00:00). As long as the bit remains in the high condition, the 1 Hz input to the clock counter chain is disabled.

The disable function is level triggered. For instance, if D0 is a high level and a reset function is desired, the bit must be "dropped" to a low level and then "raised" to a high level.

D1-Calendar Reset

When the D1-bit of the control register makes a transition from low to high (positive edge), the calendar resets to January 1 (01,01).

D2-Second Read/Second Set

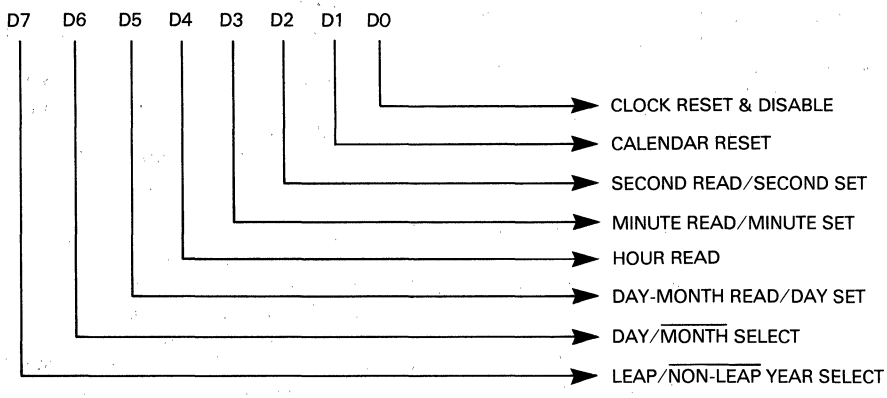
When the D2 bit of the control register is a high level, the second read/second set function is enabled. With the D2 bit set, and a read performed on the low order port, "second" data appears in BCD format. The bit also serves as the second set. When two successive writes (OUT) are performed on the high order port, the "seconds" counter advances by one second.

D3-Minute Read/Minute Set

When the D3 bit of the control register is a high level, the minute read/minute set function is enabled. When D3 bit is set and a read performed on the low order port, "minutes" appears in BCD format. The bit also serves as the minute set. When two successive writes (OUT) are performed on the high order port, the "minute" counter advances by one minute. After the "minute" counter reaches fifty-nine and is incremented one more time, the "hour" counter advances one hour. Note: The hour counter must be set through the minute counter.

CONTROL REGISTER FUNCTIONS

Table 4



CONTROL DATA REGISTER FUNCTIONS

Figure 4

WRITE (XXXX XXX0)								READ (XXXX XXX0)	OUT (XXXX XXX1)	COMMENTS
D7		D5		D3		D1	D0			
X	X	X	X	X	X	X	↓			Rising Edge Resets Clock to 00:00:00
X	X	X	X	X	X	X	1			High Level Disables 1 Hz Clock Pulse
X	X	X	X	X	X	↓	X			Rising Edge Resets Calendar To 01-01
1	X	X	X	X	X	X	X			High Level Selects Leap Year Calendar
0	X	X	X	X	X	X	X			Low Level Selects Non-Leap Year Calendar
X	X	0	0	0	1	X	X	SECOND DATA	INCREMENT SECONDS	Ripple Not Disabled To Minute Counter
X	X	0	0	1	0	X	X	MINUTE DATA	INCREMENT MINUTES & HOUR WITH RIPPLE	Ripple Not Disabled To Hour Counter
X	X	0	1	0	0	X	X	HOUR DATA		
X	0	1	0	0	0	X	X	MONTH DATA	INCREMENT DAY OF YEAR	
X	1	1	0	0	0	X	X	DAY DATA	INCREMENT DAY OF YEAR	

D4-Hour Read

When the D4 bit of the control register is a high level, the hour read function is enabled. When the D4 bit is set and a read performed on the low order port, "hour" data appears in BCD format.

D5-Day-Month Read/Day Set

When the D5 bit of the control register is a high level, the day-month read/day set function is enabled. With the D5 bit set, and a read is performed on the low order port, either "day" or "month" data appears in BCD format depending on the condition of the day/month select bit of the control register (D6). The D5 bit also serves as the day set. When two successive writes (OUT) are performed on the high order port, the day or month counter advances by one "day" or "month" depending on the condition of the day/month select bit.

D6-Day/Month Select

When the D6 bit of the control register is a low level, the "month" portion of the calendar is addressed and read operations can be performed on "month" data. When the D6 bit is a high level, the "day" portion of the calendar is addressed and read and set operations on "day" data can be performed.

D7-Leap/Non-Leap Year Select

The MDX-BCLK module contains leap and non-leap year calendars. With the D7 bit in a low state, the calendar is a 365 day non-leap calendar. With the D7 bit in a high state, the calendar is a 366 day leap year calendar. During a leap year, the D7 bit only has to be set when reading or setting operations are performed on the clock. It is not necessary to keep the bit set all the time during a leap year.

Power Up Condition

All bits of the control register power up in a low level state.

Clock Read/Set Software

The section provides a general flow chart for reading the clock and software examples in Z80 Assembly Language. The Z80 programs are sample implementations while the

flow charts provide detailed program outlines. Figure 5 is a general program for reading the clock calendar with leap year provisions. Figure 6 is a complete clock calendar with leap year provisions. Figure 7 and 8 are flow charts of the same information.

Explanation of Clock Read Flow Chart

The clock calendar read flow chart is shown in Figure 7 and consists of the following four parts:

1. Leap/Non-Leap Year Determination
2. Clock Read
3. Clock Check
4. End of Year

Clock Read and Check

In order to interpret the clock calendar correctly, one must determine if the year is a leap or non-leap year. Because the leap year is cleared when system power is lost, it should be set, if necessary, prior to each read. The clock calendar should be read next by setting the leap year bit accordingly and reading the clock in the following order:

1. Second Data
2. Month Data
3. Day Data
4. Hour Data
5. Minute Data
6. Second Data

After the above data has been obtained, the two second readings must be compared. This is necessary due to the possibility of reading the clock during a counter chain ripple. For example, if the time is (23:59:59) and the clock changes, one might obtain (23:00:00). By reading the seconds twice, the beginning and end one would always know the validity of the read. If the two second readings are different, one needs to re-read the entire clock.

End-Of-Year Function

Software is responsible for resetting the day/month counter. A status bit (D7) will be set on the 366th or 367th day depending on which calendar is used (leap or non-leap) to inform that the end of the year has arrived. The end-of-year data contained in the month portion of the calendar starts at 81H so that the user can test the high order bit to determine the end of the year. From then it counts in binary for up to 127 days past the end of the year (i.e., 82, 83, 84, 85, 86, 87, 88, 89, 8A, 8B,...) allowing the calendar correction.

Clock Set Advance

This section provides a general flow chart for reading the clock and a software example in Z80 Assembly Language. Figure 6 is a general program for setting the time.

Explanation of Clock/Calendar Set Flow Chart

The clock/calendar set flow chart is illustrated in Figure 8, and consists of the following three parts:

1. Leap/Non-Leap Year Determination
2. Clock Set
3. Calendar Set

Clock Set

To set the time on the MDX-BCLK module, set in sequence, the hours first, minutes next, and then seconds. Use the control register to select the desired counter for setting; write to the high order port to increment the counter. Set the second and minute counters individually; the hour counter is incremented automatically by the minute counter (i.e., after 60 increments of the minute counter, the hour counter advances.). Two algorithims can be used to set the clock. First, increment and then check each counter until the data matches that of the flow chart and sample programs. To set the clock, either increment each counter until it matches the flow chart and sample programs or reset the counters and increment from zero (i.e., 30 second desired set time requires 60 OUTs). The clock reset disable bit (D0) of the control register should be set and left set during the entire clock/calendar set time.

Calendar Set

To set the calendar on the MDX-BCLK module, the calendar reset should be raised and then lowered at the beginning of the calendar set program. The Leap Year/Non-Leap Year bit, D7, must be set accordingly before month and day data is set.

Mandatory setting order of the calendar is month and then day. Select the desired date to be set (day or month) with the control register and then write to the high order port to increment the counter.

CLOCK CALENDAR READ SOFTWARE

Figure 5

```
                                                MOSTEK MACRO-80 ASSEMBLER V2.2      PAGE 1
LOC     OBJ.CODE        STMT-NR   SOURCE-STMT   PASS2   OPSRD   OPSRD   OPSRD   REL

                                ;
                                ;
                                ; COMPLETE CLOCK AND CALENDAR READ
                                ;
                                ; PASS             HL      : POINTER TO DATE/TIME BUFFER
                                ;
                                ; RETURN           DATA IN BCD FORMAT
                                ;                   HL      :UNCHANGED
                                ;                  (HL)     :YEAR
                                ;                  (HL + 1) :MONTH
                                ;                  (HL + 2) :DAY
                                ;                  (HL + 3) :HOUR
                                ;                  (HL + 4) :MINUTE
                                ;                  (HL + 5) :SECOND
                                ;
                                ;                  DATE CORRECTED FOR END OF YEAR
                                ;
                                ; USES             AF  BC  DE  HL
                                ;
                                ; PRESERVES        AF  BC  DE  HL
                                ;
                                ;


                                ;
                                ;
                                ; CONTROL REGISTER AND MDX-BCLK DEFINITIONS
                                ;
                                        ;
                                ;
=0070                     28 BCLK   EQU   70H             ; BCLK BASE PORT ADDRESS
=0070                     29 DATA   EQU   BCLK            ; BCLK DATA PORT
=0071                     30 PULS   EQU   BCLK+1          ; BCLK PULSE PORT
                                ;
                                ;
=0080                     33 LEP    EQU   80H             ; LEAP YEAR BIT
=0060                     34 DAY    EQU   60H             ; DAY BIT
=0020                     35 MON    EQU   20H             ; MONTH BIT
=0010                     36 HRS    EQU   10H             ; HOUR BIT
=0008                     37 MIN    EQU   08H             ; MINUTE BIT
=0004                     38 SEC    EQU   04H             ; SECOND BIT
=0002                     39 CALR   EQU   02H             ; CALENDAR RESET BIT
=0001                     40 CLKD   EQU   01H             ; CLOCK RESET AND DISABLE
                                ;
                                ;
=0007                     43 LFLAG  EQU   7               ; LEAP YEAR TEST FLAG
=0007                     44 EYEAR  EQU   7               ; END OF YEAR TEST FLAG
                                ;
                                ;
                          47        GLOBAL READBACK
                                ;
                                ;
=0000'                    50 READCK:
```

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CLOCK CALENDAR READ SOFTWARE (CONT.)

Figure 5

```
                                                    MOSTEK MACRO-80 ASSEMBLER V2.2          PAGE 2
LOC     OBJ.CODE        STMT-NR   SOURCE-STMT       PASS2    OPSRD    OPSRD    OPSRD    REL

0000    F5                  51            PUSH      AF
0001    C5                  52            PUSH      BC
0002    D5                  53            PUSH      CE
                                ;
                                ;
                =0003'      56 LEPCK:
0003    7E                  57            LC        A,(HL)              ; GET CURRENT YEAR OUT OF BUFFER
0004    23                  58            INC       HL                  ; POINT TO MONTH DATA
0005    B7                  59            DR        A
0006    28 0C               60            JR        Z,NLEAP-$           ; NON-LEAP FOR YEAR 2000
0008    ES13                61            AND       13H
000A    2804                62            JR        Z,ISLEAP-$          ; LEAP FOR EVEN DECADES
000C    FE12                63            CP        12H
000E    2004                64            JR        NZ,NLEAP-$
                =0010'      65 ISLEAP:
0010    CBF9                66            SET       LFLAG,C             ; SET LEAP YEAR FLAG
0012    1802                67            JR        SETFLG-$
                =0014'      68 NLEAP:
0014    CBB9                69            RES       LFLAG,C             ; CLEAR LEAP FLAG
                =0016'      70 SETFLG:
0016    3E04                71            LD        A,SEC               ; SET CONTROL REG. FOR SEC READ
0018    D370                72            OUT       (DATA),A
001A    DB70                73            IN        A,(DATA)            ; GET SECOND DATA
001C    47                  74            LD        B,A
0010    C5                  75            PUSH      BC                  ; SAVE ON STACK
001E    E5                  76            PUSH      HL
001F    EB                  77            EX        DE,HL               ; BUFFER ADDRESS IN DE
0020    21 6400'            78            LD        HL,LTABLE           ; LEAP YEAR TABLE IN HL
0023    CB79                79            BIT       LFLAG,C             ; CHECK FOR LEAP YEAR
0025    2003                80            JR        NZ,OVER-$
0027    21 5F00'            81            LD        HL,TABLE            ; NON-LEAP TABLE IN HL
                =002A'      82 OVER:
002A    060A                83            LD        B,5*2               ; 5 BYTES TO WRITE, 5 TO READ
002C    0E70                84            LD        C,DATA
                =002E'      85 LOOP:
002E    EDA3                86            CUTI                          ; OUTPUT CONTROL BYTE,
                                                                        ; INCREMENT TABLE ADDRESS (HL)
                                                                        ; DECREMENT COUNTER (B)
0030    0B70                89            IN        A,(DATA)            ; INPUT DATA
0032    12                  90            LD        (DE),A              ; STORE IN BUFFER
0033    13                  91            INC       DE                  ; INCREMENT BUFFER POINTER
0034    10F8                92            DJNZ      LOOP-$              ; DECREMENT COUNTER (B)
                                ;
                                ;
0036    18                  95            DEC       DE                  ; POINT TO SECONDS IN BUFFER
0037    1A                  96            LC        A,(DE)
0038    E1                  97            POP       HL
0039    C1                  98            POP       BC                  ; GET FIRST SECOND READING
                                                                        ; OFF STACK
003A    BB                 100            CP        8                   ; CHECK FOR CLOCK ROLL OVER
```

CLOCK CALENDAR READ SOFTWARE (CONT.)

Figure 5

```
                                                MOSTEK MACRO-80 ASSEMBLER V2.2        PAGE 3
LOC     OBJ.CODE        STMT-NR  SOURCE-STMT    PASS2    OPSRD    OPSRD    OPSRD    REL

003B    20C6              101            JR      NZ,LEPCK-S          ; RE-READ CLOCK IF ROLL OVER OCCURED
                                ;
                                ;
003D    CB7E              104            BIT     EYEAR,(HL)          ; CHECK FOR END OF YEAR
003F    2008              105            JR      NZ,ENDYR-$          ; GO FIX IT
        =0041'            106 DONE:
0041    AF                107            XOR     A
0042    D370              108            CUT     (DATA),A            ; CLEAR CONTROL REGISTER
0044    23                109            DEC     HL                  ; RESTORE HL
0045    D1                110            POP     DE
0046    D1                111            POP     BC                  ; RESTORE REGISTERS
0047    F1                112            POP     AF
0048    C9                113            RET
        =0049'            114 ENDYR:
0049    46                115            LD      B,(HL)              ; GET MONTH DATA
                                                                     ; IT'S REALLY COUNT OF DAYS PAST
                                                                     ; END OF YEAR
004A    CBB8              118            RES     EYEAR,B             ; MASK FLAG
004C    3E62              119            LD      A,DAY+CALR          ; SETUP FOR DAY BUMP AND CAL RESET
004E    D370              120            OUT     (DATA),A
0050    1804              121            JR      UPDATE-$
        =0052'            122 ADVN:
0052    D371              123            OUT     (PULS),A
0054    D371              124            OUT     (PULS),A            ; INCREMENT DAYS
        =0056'            125 UPDATE:
0056    10FA              126            DJNZ    ADVN-$
                                ;
                                ;
0058    2B                129            DEC     HL                  ; POINT TO YEAR DATA
0059    7E                130            LD      A,(HL)
005A    3C                131            INC     A                   ; INCREMENT YEAR (IN BCD)
005B    27                132            DAA
005C    77                133            LD      (HL),A
005D    18A4              134            JR      LEPCK-$             ; RE-READ CLOCK
                                ;
                                ;
        =005F'            137 TABLE:
005F    20                138            DEFB    MON
0060    60                139            DEFB    DAY
0061    10                140            DEFB    HRS
0062    08                141            DEFB    MIN
0063    04                142            DEFB    SEC
                                ;
                                ;
        =0064'            145 LTABLE:
0064    A0                146            DEFB    MON + LEP
0065    E0                147            DEFB    DAY + LEP
0066    10                148            DEFB    HRS
0067    08                149            DEFB    MIN
0068    04                150            DEFB    SEC
```

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CLOCK CALENDAR READ SOFTWARE

Figure 6

```
                                                    MOSTEK MACRO-80 ASSEMBLER V2.2          PAGE 1
LOC      OBJ.CODE   STMT-NR    SOURCE-STMT          PASS2    OPSWR    OPSWR    OPSWR    REL

                                ;
                                ;
                                ; COMPLETE CLOCK AND CALENDAR SET
                                ;
                                ; PASS                DATA IN BCD FORMAT
                                ;                     HL        :POINTER TO CLOCK SET BUFFER
                                ;                     (HL)      :DESIRED YEAR SET
                                ;                     (HL + 1)  :DESIRED MONTH SET
                                ;                     (HL + 2)  :DESIRED DAY SET
                                ;                     (HL + 3)  :DESIRED HOUR SET
                                ;                     (HL + 4)  :DESIRED MINUTE SET
                                ;                     (HL + 5)  :DESIRED SECOND SET
                                ;
                                ;                     DATE CORRECTED FOR END OF YEAR
                                ;
                                ; USES                AF  BC  DE  HL
                                ;
                                ; PRESERVES           AF  BC  DE  HL
                                ;
                                ;


                                ;
                                ;
                                ; CONTROL REGISTER AND MDX-BCLK DEFINITIONS
                                ;
                                ;
=0070                     24 BCLK     EQU   70H          ; BCLK BASE PORT ADDRESS
=0070                     25 DATA     EQU   BCLK         ; BCLK DATA PORT
=0071                     26 PULS     EQU   BCLK+1       ; BCLK PULSE PORT
                                ;
                                ;
=0080                     29 LEP      EQU   80H          ; LEAP YEAR BIT
=0060                     30 DAY      EQU   60H          ; DAY BIT
=0020                     31 MON      EQU   20H          ; MONTH BIT
=0010                     32 HRS      EQU   10H          ; DAY BIT
=0008                     33 MIN      EQU   08H          ; MINUTE BIT
=0004                     34 SEC      EQU   04H          ; SECOND BIT
=0002                     35 CALR     EQU   02H          ; CALENDAR RESET BIT
=0001                     36 CLKD     EQU   01H          ; CLOCK RESET AND DISABLE
                                ;
                                ;
=0007                     39 LFLAG    EQU   7            ; LEAP YEAR TEST FLAG
=0007                     40 EYEAR    EQU   7            ; END OF YEAR TEST FLAG
=0004                     41 EOT      EQU   04H          ; FLAG FOR END OF TABLE
                                ;
                                ;
                          44        GLOBAL SCLOCK
                                ;
                                ;
=0000'                    47 SCLOCK:
0000   F5                48        PUSH  AF
0001   C5                49        PUSH  BC             ; PRESERVE REGISTERS
```

CLOCK CALENDAR READ SOFTWARE (CONT.)

Figure 6

```
                                                MOSTEK MACRO-80 ASSEMBLER V2.2          PAGE 2
LOC      OBJ.CODE  STMT-NR    SOURCE-STMT        PASS2    OPSWR    OPSWR    OPSWR    REL
0002     D5          50               PUSH    DE
0003     E5          51               PUSH    HL
                     52               ;
                     53               ;
         =0004'      54  LPCK:
0004     7E          55               LD      H,(HL)              ; GET YEAR DATA
0005     23          56               INC     HL                  ; POINT TO MONTH DATA
0006     B7          57               OR      A                   ; NON-LEAP YEAR 2000
0007     28 0C       58               JR      Z,NLEP-$
0009     E6 13       59               AND     13H                 ; ALL OTHER CASES
000B     28 04       60               JR      Z,ISLEP-$
000D     FE 12       61               CP      12H
000F     20 04       62               JR      NZ,NLEP-$
         =0011'      63  ISLEP:
0011     CBF9        64               SET     LFLAG,C             ; SET LEAP FLAG
0013     18 02       65               JR      SETF-$
         =0015'      66  NLEP:
0015     CBB9        67               RES     LFLAG,C
         =0017'      68  SETF:
                     69               ;
                     70               ;
0017     EB          71               EX      DE,HL               ; BUFFER POINTER IN DE
0018     21 5000'    72               LD      HL,TABL+2           ; GET TABLE POINTER
001B     CB79        73               BIT     LFLAG,C             ; TEST FOR LEAP YEAR
001D     20 03       74               JR      NZ,JUMP-$
001F     21 4E00'    75               LD      HL,TABL             ; GET NON-LEAP YEAR
                     76                                           ; TABLE POINTER
                     77  JUMP:
                     78               LD      A,CLKD
                     79               OUT     (DATA),A
0022     3E03        80               LD      A,CALR+CLKD         ; RESET CLOCK AND CALENDAR
0024     D370        81               OUT     (DATA),A            ;
         =0026'      82  SLOOP:
0026     1A          83               LD      A,(DE)              ; GET DESIRED SET DATA
0027     47          84               LD      B,A
0028     7E          85               LD      A,(HL)              ; GET CONTROL REGISTER DATA
                     86                                           ; OUT OF TABLE
0029     FE04        87               CP      EDT                 ; CHECK FOR END OF TABLE
0028     28 19       88               JR      Z,STOP-$
002D     D370        89               OUT     (DATA),A            ; SET UP CONTROL REGISTER
002F     DB70        90               IN      A,(DATA)            ; GET CLOCK DATA
0031     68          91               CP      B                   ; IS CLOCK SET?
0032     28 08       92               JR      Z,NEXT-$            ; IF SO SET NEXT PORTION
                     93               ;
                     94               ;
0034     23          95               INC     HL                  ; ADVANCE POINTER TO
0035     7E          96               LD      A,(HL)              ; TO SET DATA TABLE
0036     D370        97               OUT     (DATA),A            ; SET UP CONTROL REGISTER
003A     D371        98               OUT     (PULS),A            ; WRITE TWICE TO
003A     D371        99               OUT     (PULS),A            ; BUMP ONCE
003C     2B         100               DEC     HL                  ; RESTORE TABLE POINTER
                    101                                           ; FOR NEXT READ
003D     18E7       102               JR      SLOOP-$
```

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CLOCK CALENDAR READ SOFTWARE (CONT.)

Figure 6

```
                                                    MOSTEK MACRO-80 ASSEMBLER V2.2          PAGE 3
LOC      OBJ.CODE   STMT-NR    SOURCE-STMT          PASS2   OPSWR   OPSWR   OPSWR   REL

         =003F'       101  NEXT:
003F     23           102          INC     HL
0040     23           103          INC     HL              ;  ADVANCE TABLE POINTER
0041     23           104          INC     HL              ;  FOR NEXT OPERTION
0042     23           105          INC     HL
0043     13           106          INC     DE              ;  ADVANCE BUFFER POINTER
0044     18 E0        107          JR      SLOOP-$
         =0046'       108  STOP:
0046     AF           109          KOR     A
0047     D370         110          CUT     (DATA),A        ;  CLEAR CONTROL REGISTER
0049     E1           111          POP     HL
004A     D1           112          POP     DE              ;  RESTORE REGISTERS
004B     C1           113          POP     BC
004C     F1           114          POP     AF
004D     C9           115          RET
                      ;
                      ;
                      ;  TABLE ORGANIZATION COMMENTS:
                      ;
                      ;  THE TABLE BELOW CONTAINS FOUR TABLETS USED TO SET UP THE MDX-BCLK CONTROL
                      ;  REGISTER FOR CLOCK AND CALENDAR READ AND SET OPERATIONS. THE FOUR TABLES
                      ;  ARE NON-LEAP READ, NON-LEAP SET, LEAP READ, AND LEAP SET. THE FOUR TABLES
                      ;  ARE INTERLEAVED ON FOUR BYTE INCREMENTS.
                      ;
                      ;
                      ;
         =004E'       129  TABL:
                      ;
                      ;
004E     21           132          DEFB    MON+CLKD        ;  SELECT MONTH READ
                                                           ;  RESET CLOCK
                                                           ;  KEEP CLOCK DISABLED
                                                           ;  RESET CALENDAR
004F     21           136          DEFB    MON+CLKD        ;  SELECT MONTH SET
                                                           ;  KEEP CLOCK DISABLED
0050     A1           138          DEFB    MON+CLKD+LEP    ;  SELECT MONTH READ
                                                           ;  RESET CLOCK
                                                           ;  KEEP CLOCK DISABLED
                                                           ;  SELECT LEAP YEAR CALENDAR
0051     21           142          DEFB    MON+CLKD        ;  SELECT MONTH SET
                                                           ;  KEEP CLOCK DISABLED
0052     61           144          DEFB    DAY+CLKD        ;  SELECT DAY READ
                                                           ;  KEEP CLOCK DISABLED
0053     61           146          DEFB    DAY+CLKD        ;  SELECT DAY SET
                                                           ;  KEEP CLOCK DISABLED
0054     E1           148          DEFB    DAY+CLKD+LEP    ;  SELECT DAY READ
                                                           ;  KEEP CLOCK DISABLED
                                                           ;  SELECT LEAP YEAR CALENDAR
0055     61           151          DEFB    DAY+CLKD        ;  SELECT DAY SET
                                                           ;  KEEP CLOCK DISABLED
0056     11           153          DEFB    HRS+CLKD        ;  SELECT HOUR READ
                                                           ;  KEEP CLOCK DISABLED
```

CLOCK CALENDAR READ SOFTWARE (CONT.)

Figure 6

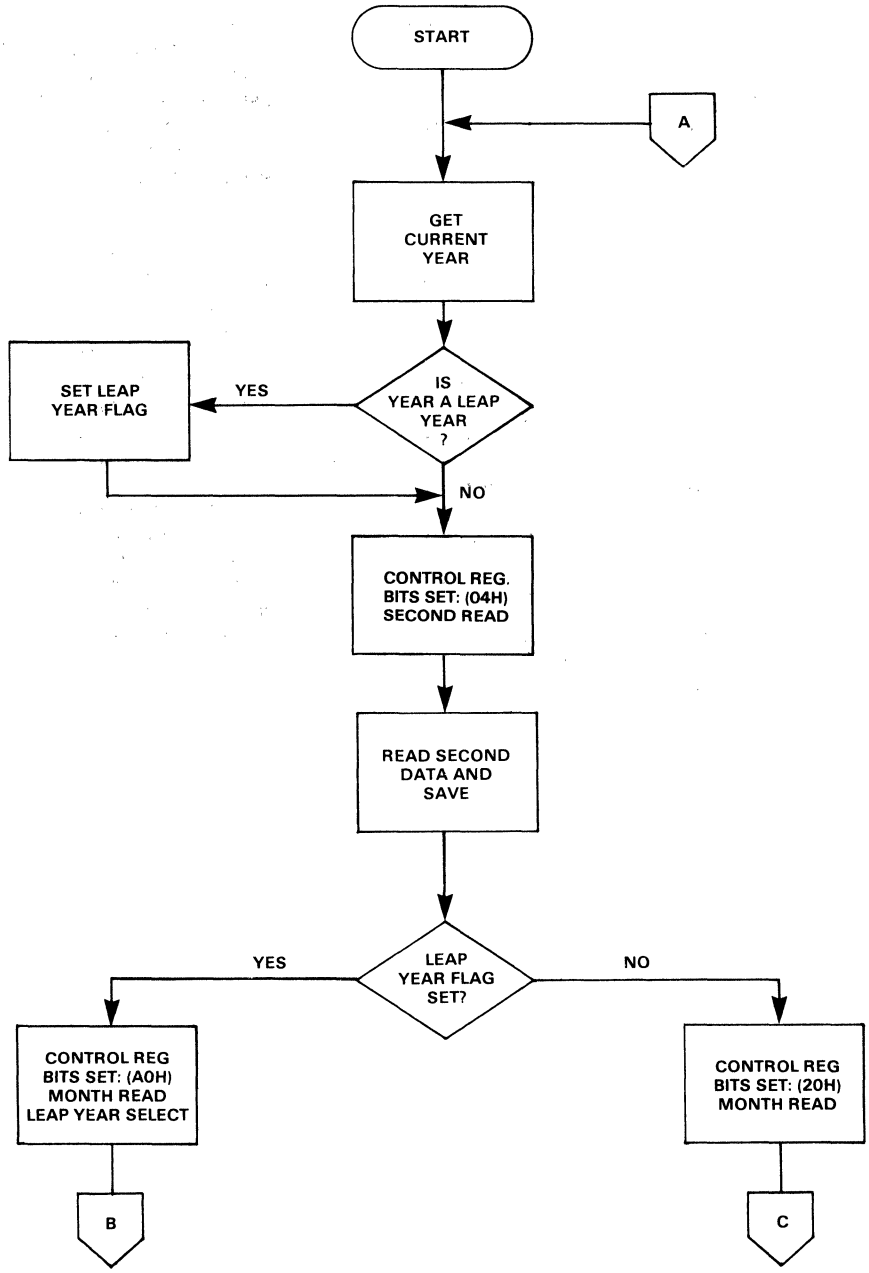
```
                                                MOSTEK MACRO-80 ASSEMBLER V2.2          PAGE 4
LOC      OBJ.CODE  STMT-NR    SOURCE-STMT        PASS2    OPSWR    OPSWR    OPSWR    REL

0057     09          159          DEFB    MIN+CLKD          ; SELECT HOUR SET
                                                           ; (NOTE: THAT THE HOUR COUNTER IS SET
                                                           ; THROUGH THE MINUTE COUNTER)
                                                           ; KEEP THE CLOCK DISABLED
0058     11          160          DEFB    HRS+CLKD          ; SELECT HOUR READ
                                                           ; KEEP CLOCK DISABLED
0059     09          162          DEFB    MIN+CLKD          ; SELECT HOUR SET
                                                           ; KEEP CLOCK DISABLED
005A     09          164          DEFB    MIN+CLKD          ; SELECT MINUTE READ
                                                           ; KEEP CLOCK DISABLE
005B     09          166          DEFB    MIN+CLKD          ; SELECT MINUTE SET
                                                           ; KEEP CLOCK DISABLED
005C     09          168          DEFB    MIN+CLKD          ; SELECT MINUTE READ
                                                           ; KEEP CLOCK DISABLED
005D     09          170          DEFB    MIN+CLKD          ; SELECT MINUTE SET
                                                           ; KEEP CLOCK DISABLED
005E     05          172          DEFB    SEC+CLKD          ; SELECT SECOND READ
                                                           ; KEEP CLOCK DISABLED
005F     05          174          DEFB    SEC+CLKD          ; SELECT SECOND SET
                                                           ; KEEP CLOCK DISABLED
0060     05          176          DEFB    SEC+CLKD          ; SELECT SECOND READ
                                                           ; KEEP CLOCK DISABLED
0061     05          178          DEFB    SEC+CLKD          ; SELECT SECOND SET
                                                           ; KEEP CLOCK DISABLED
0062     04          180          DEFB    EOT               ; END OF NON-LEAP TABLE
0063     04          181          DEFB    EOT               ; END OF LEAP TABLE
0064     04          182          DEFB    EOT
                                 ;
                                 ;
```

IVE

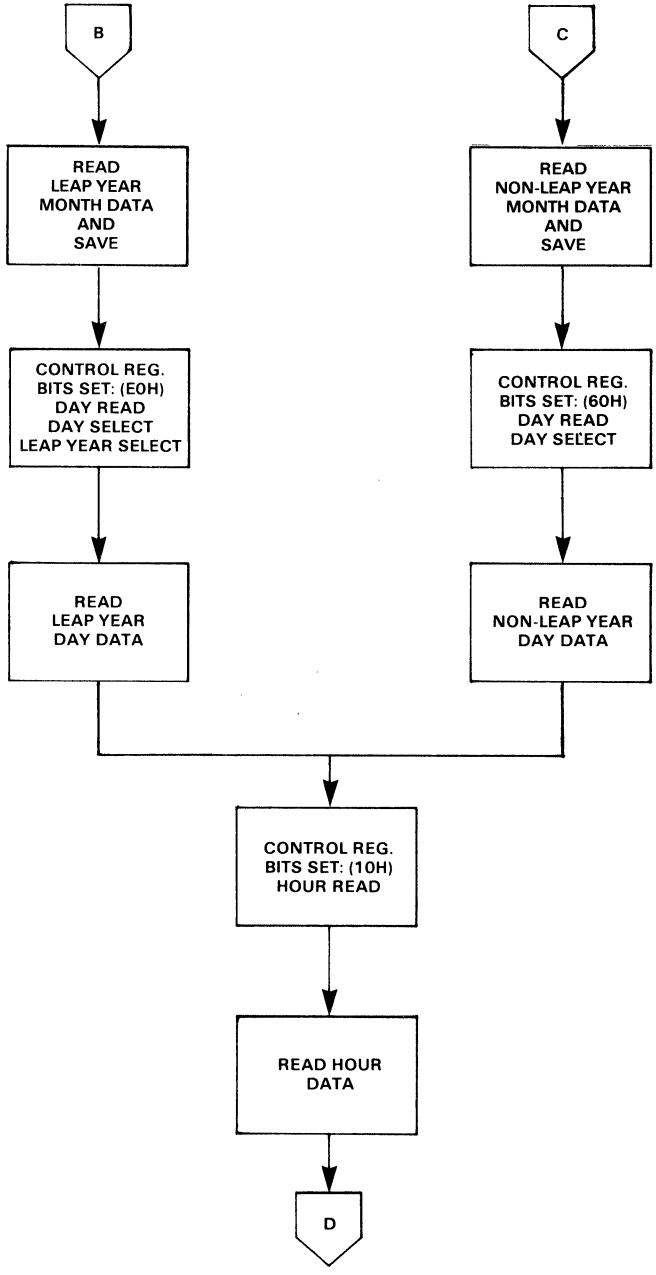
CLOCK CALENDAR READ FLOW CHART

Figure 7

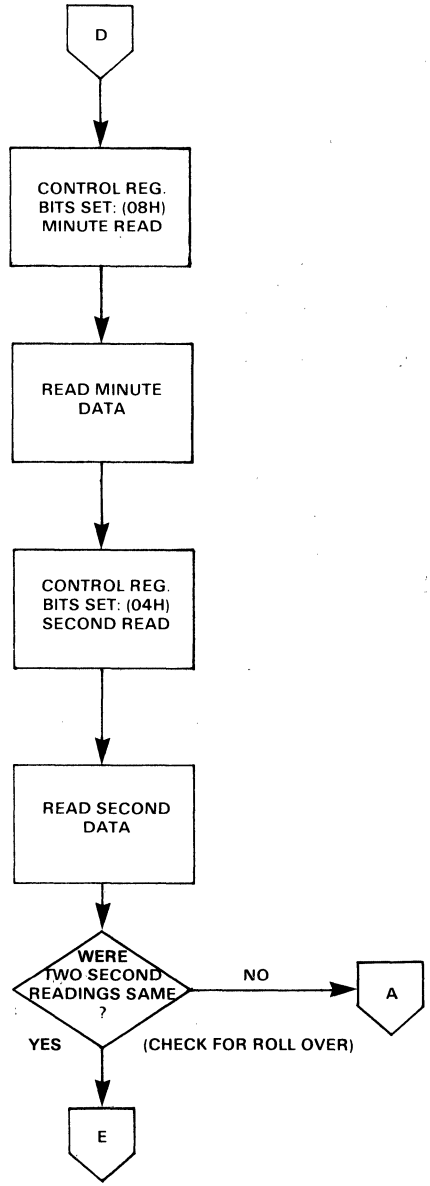


CLOCK CALENDAR READ FLOW CHART (Cont'd.)

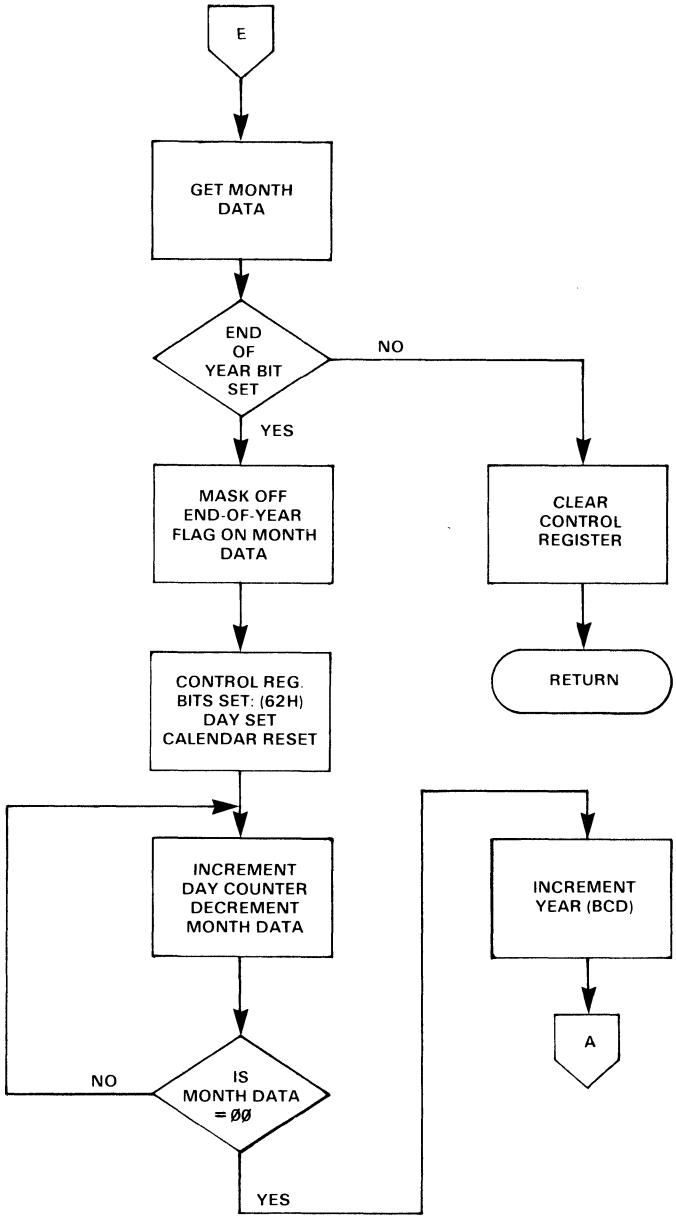
Figure 7



CLOCK CALENDAR READ FLOW CHART (Cont'd.)
Figure 7

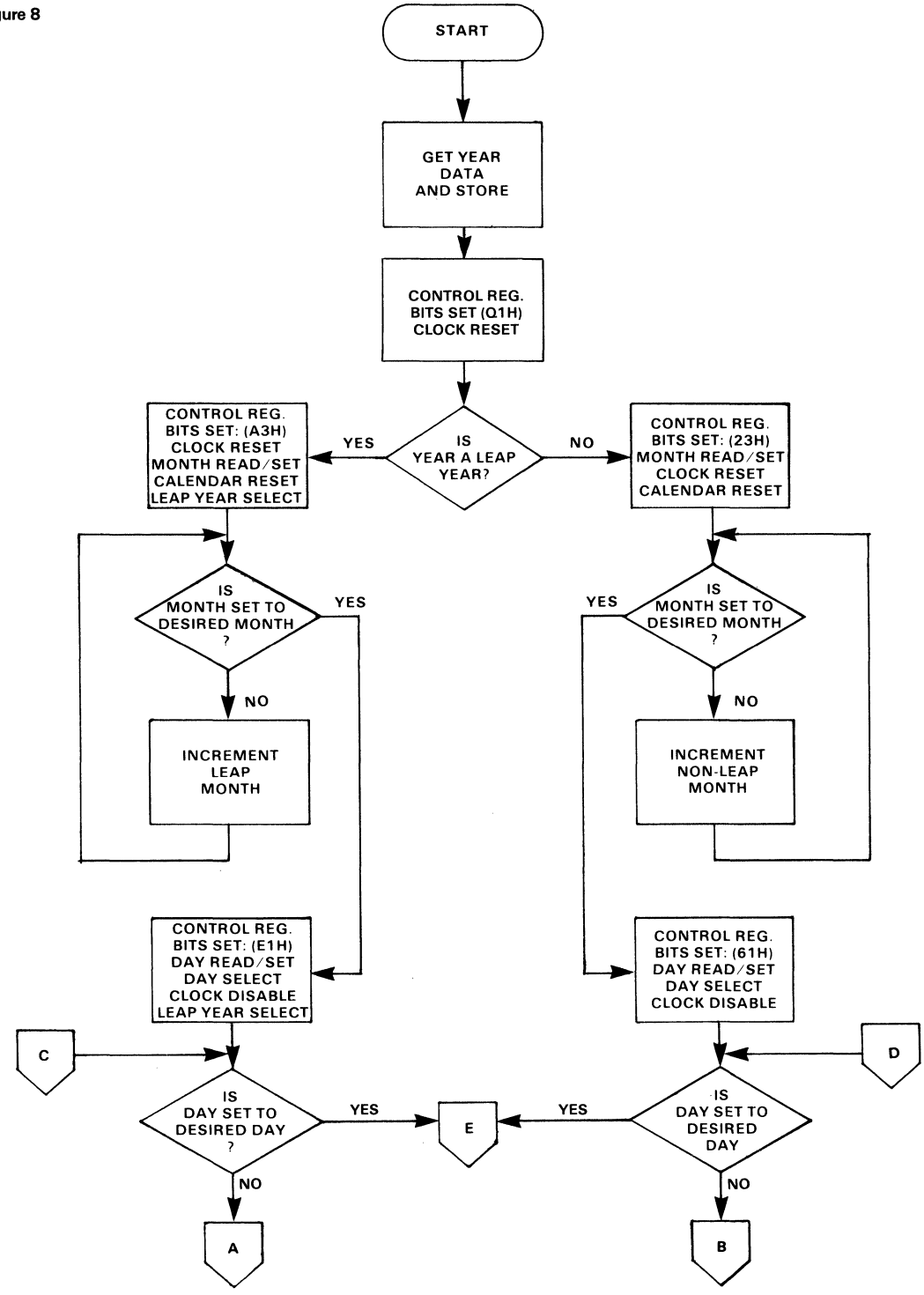


CLOCK CALENDAR READ FLOW CHART (Cont'd.)
Figure 7



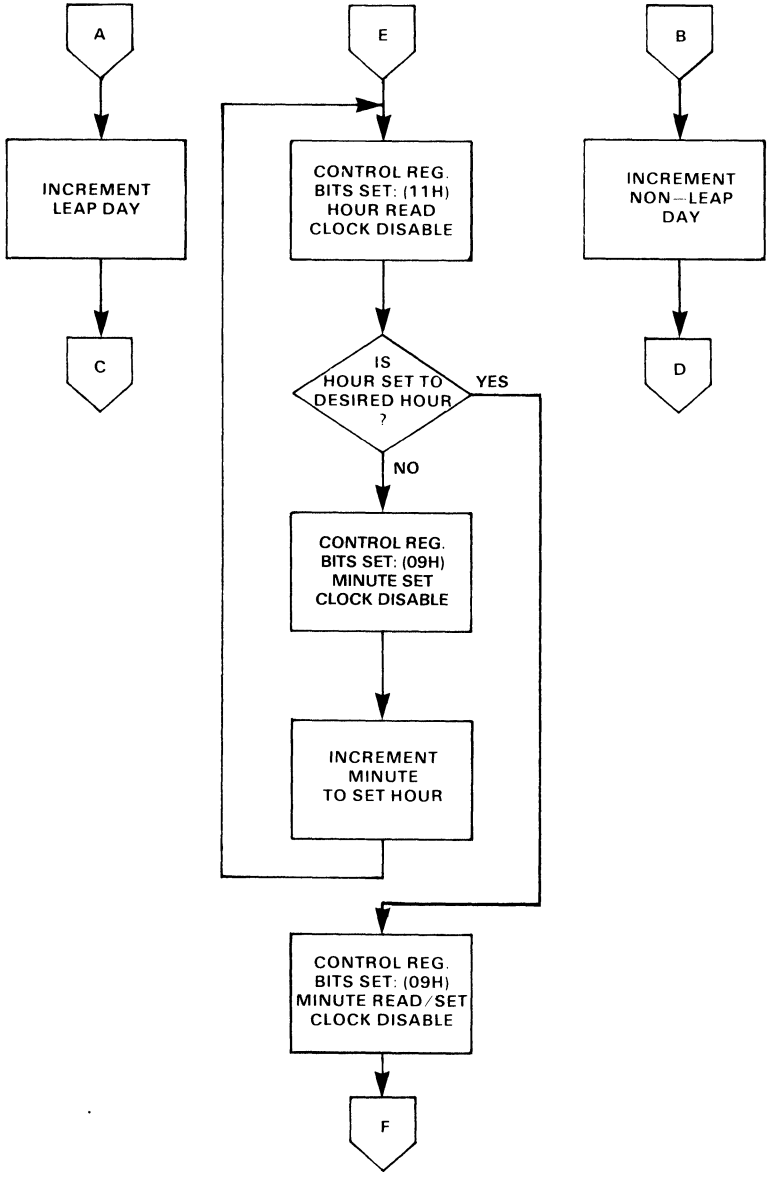
CLOCK CALENDAR SET FLOW CHART

Figure 8



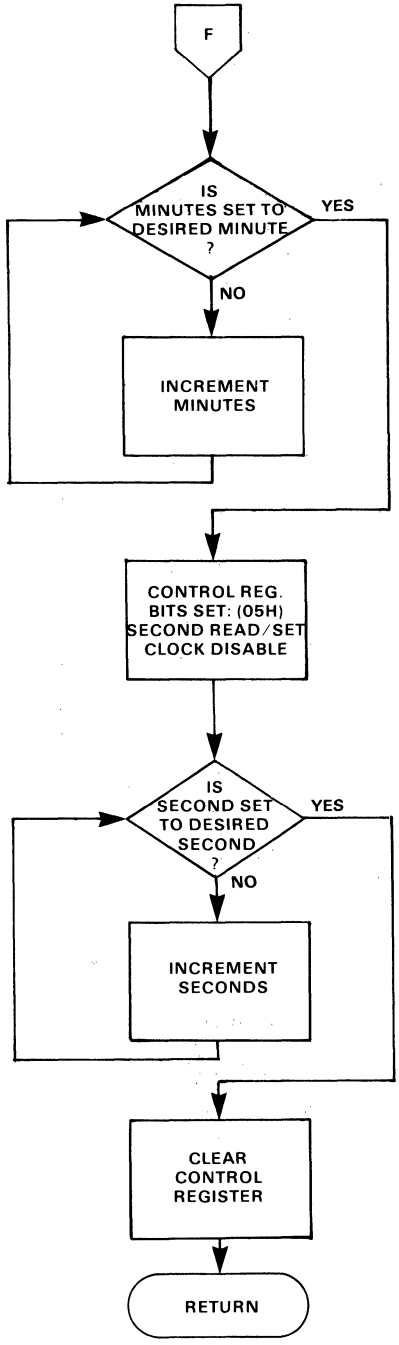
CLOCK CALENDAR SET FLOW CHART (Cont'd.)

Figure 8



CLOCK CALENDAR SET FLOW CHART (Cont'd.)

Figure 8



CONNECTORS

Function	Description	Mating Connector
STD BUS	56-pin, dual	Viking 3VH28/1CE5 (Printed circuit Viking 3VH28/1CND5 (Wire-wrap) Viking 3VH28/1CN5 (Solder Lug)
CTC Interface	2-position Housing Contact	AMP 87499-3 AMP 87046-1

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-BCLK	Battery Clock Module with Technical Manual	MK77976
MDX-BCLK Technical Manual	MDX-BCLK Technical Manual only	4420065

ACCESSORIES (MD-ACC)

INTRODUCTION

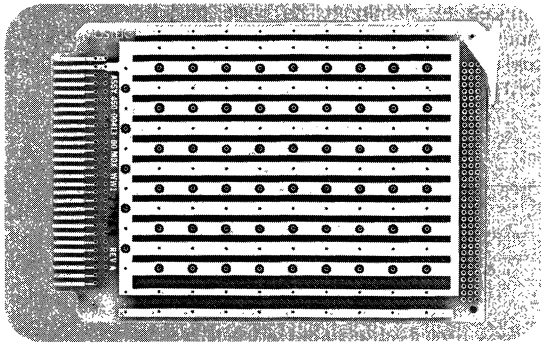
The following accessories are available to aid in the design, development, and production of products designed around the Mostek MD Series Z80* microcomputer modules:

MDX-WW1	Wire-wrap card with bussed power and ground
MDX-WW2	Wire-wrap card without bussed power and ground
MD-EXT	Extender card
MD-232DCE-C	25-pin "D" female MD DCE cable
MD-232DTE-C	25-pin "D" male MD DTE cable
MD-TTY-C	15-pin Molex-TTY cable
MD-PPG-C	25-pin "D" female PROM Programmer (PPG-8/16) interface cable
MD-CC6	6-slot card cage
MD-CC6WM	6-slot wall mount card cage
MD-CC10	10-slot card cage
MD-CC12A	12-slot card cage
MD-C16	16-slot card cage

WIRE WRAP CARDS

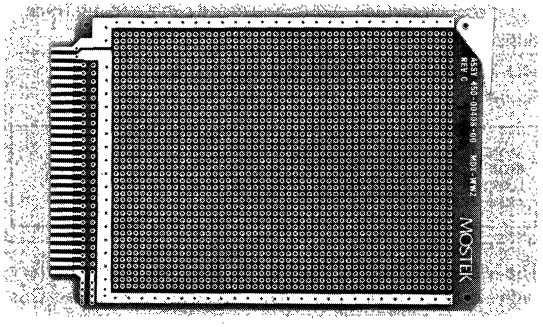
The MDX-WW1 (MK77959) is a wire-wrap card with bussed power and ground lines on the board to facilitate fabrication of circuits using wire-wrap sockets. A series of plated-through holes are available on the top of the card for mounting connectors. A photo of the board is shown in Figure 1.

MDX-WW1 (MK77959) PHOTO
Figure 1



The MDX-WW2 (MK77952) is a wire-wrap card with all plated-through holes on a 0.100-inch grid. This allows mounting of both DIP sockets and discrete components for circuit fabrication. The plated-through holes accept 0.025-inch square posts. A photo of the WW2 board is shown in Figure 2.

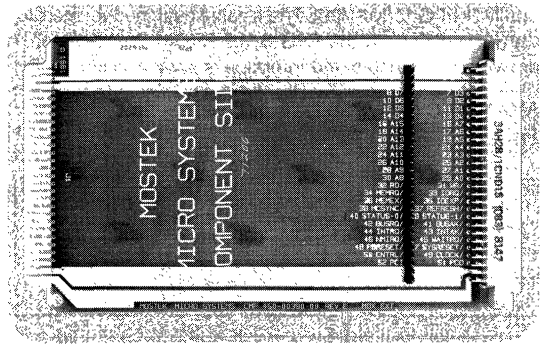
MDX-WW2 (MK77952) PHOTO
Figure 2



EXTENDER CARD

The MD-EXT (MK77953) is an extender card that allows the cards in the card cage to be extended outside the cage for easy access. A photo of the extender card is shown in Figure 3.

MD-EXT (MK77953) PHOTO
Figure 3



IVF

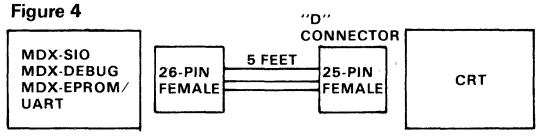
*Z80 is a registered Trademark of ZILOG

CABLES

The MD-232DCE-C (MK77955) is a cable designed to interface with either the MDX-SIO or MDX-EPROM/UART card. One end has a 26-pin socket to connect to the board. The other end has a 25-pin female "D" type connector. This cable allows the MD board to provide a Data Communication Equipment interface. A drawing of the cable and interface is shown in Figure 4.

MD-232DCE-C (MK77955)

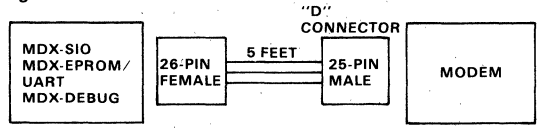
Figure 4



The MD-232DTE-C (MK77970) is a cable designed to interface with either the MDX-SIO or MDX-EPROM/UART card. One end has a 26-pin socket to connect to the board. The other end has a 25-pin male "D" type connector. This cable allows the MD board to provide a Data Terminal Equipment interface. A drawing of the cable and interface is shown in Figure 5.

MD-232DTE-C (MK77970)

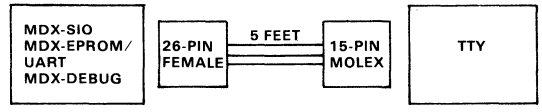
Figure 5



The MD-TTY-C (MK77956) is a cable designed to interface with either the MDX-SIO or MDX-EPROM/UART card. One end has a 26-pin socket to connect to the board. The other end has a Molex connector that allows connection to the terminal block in a teletype. A drawing of the cable and interface is shown in Figure 6.

MD-TTY-C (MK77956)

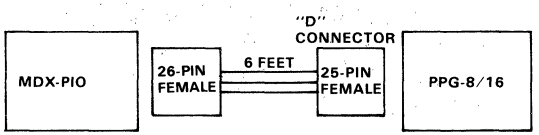
Figure 6



The MD-PPG-C (MK79957) is a cable designed to interface the MDX-PIO with the PPG-8/16 PROM Programmer. A drawing of the cable and interface is shown in Figure 7.

MD-PPG-C (MK77957)

Figure 7



CARD CAGES

There are five versions of card cages available from Mostek, they are:

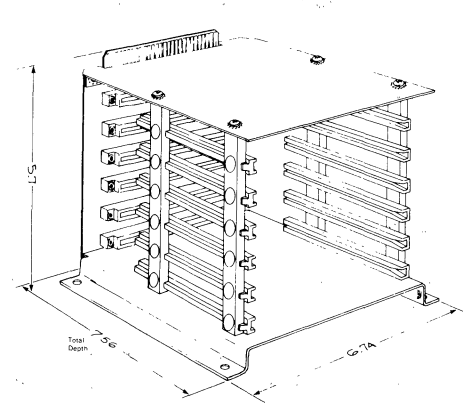
MD-CC6 (MK77973)
MD-CC6-WM (MK77978)
MD-CC10 (MK77989)
MD-CC12A (MK77970)
MD-CC16 (MK77977)

All models have connectors on 0.75-inch centers. MD-CC6 and MD-CC12A have the cards inserted horizontally while the MD-CC6-WM, MD-CC10, and MD-CC16 have the cards inserted vertically.

The MD-CC6 is a six-slot card cage fabricated out of aluminum. Its basic purpose is to be mounted to a baseplate, allowing the cards to be inserted horizontally. The card edge extending from the top of the cage is not intended to be used as a bus extension mechanism. The thickness of the motherboard prohibits standard connectors to fit on it. Figure 8 illustrates the six-slot card cage dimensions.

MD-CC6 DRAWING WITH DIMENSIONS

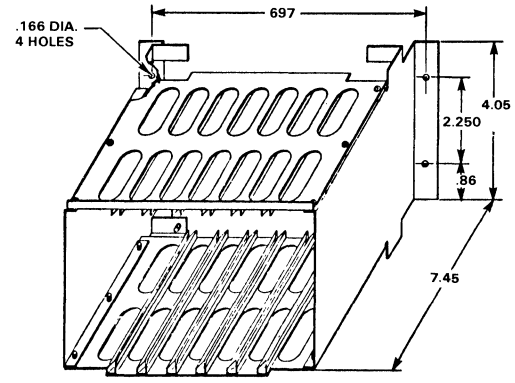
Figure 8



The MD-CC6-WM is a card cage fabricated from steel as opposed to aluminum. Its basic purpose is for wall mounting; for example in a NEMA enclosure for industrial applications. Figure 9 illustrates the six-slot wall-mount card dimensions.

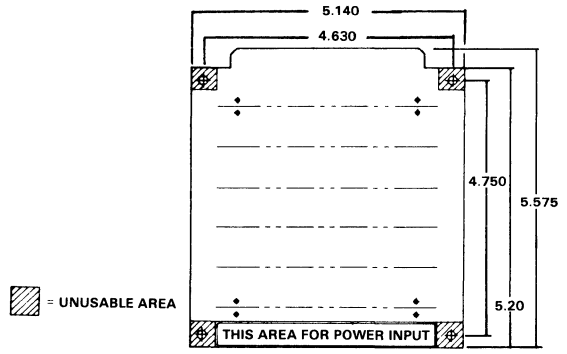
MD-CC6-WM DRAWING WITH DIMENSIONS

Figure 9



MD-CC6 AND MD-CC6 WM MOTHERBOARD WITH DIMENSIONS

Figure 10



The six-slot motherboard (for both CC6 and CC6-WM) has eight plated-through holes in which to insert 16-guage wire (maximum) for power and ground connections. The holes are denoted from left to right on the fab side of the motherboard (see Figure 10 for a drawing of the motherboard). In addition, there are five pins located on the lower right edge of the board for connecting a remote +12 V lamp. The /PBRESET line is also connected to these pins if the user desires a remote reset switch. The hole and pin assignments are shown in Table 1 and Table 2.

INTERCONNECTION OF POWER PLANE TO STD BUS-CC6, CC6-WM

Table 1

CONNECTION PINS (Left to Right)	DESIGNATOR	STD BUS PIN NO.
1, 2	GND	3, 4
3	-12 V	56
4, 5	+5 V	1, 2
6	+12 V	55
7	-5 V	5, 6
8	AUX. GND	53, 54

CONNECTION FOR REMOTE LAMP AND RESET SWITCH — CC6, and CC6-WM

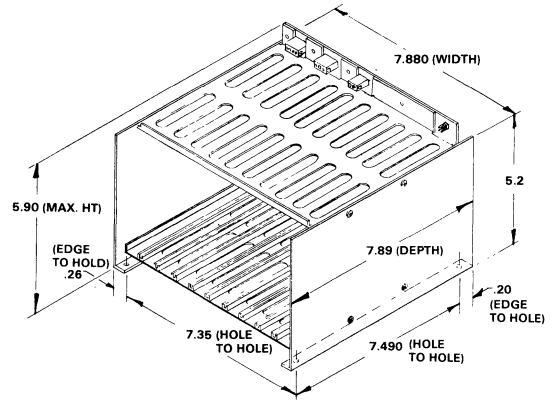
Table 2

CONNECTION	DESIGNATOR
5	+12 V
4	GND
3	/PBRESET
2	GND
1	KEY

The MD-CC10 (MK77989) is a ten-slot card cage fabricated from steel. Figure 11 slows the dimensions of the MD-CC10 card cage. Power connections to the MD-CC10 are provided by a 2-pin and 4-pin AMP Universal MATE-N-LOK connector. There is also a 3-pin Universal MATE-N-LOK connector for connecting a remote power lamp and reset button. The pins assignments for these connectors are shown in Table 3.

MD-CC10 DRAWING WITH DIMENSIONS

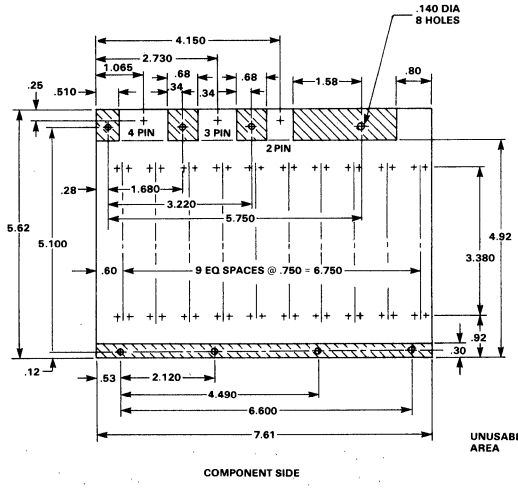
Figure 11



The MD-CC10 card cage motherboard is terminated at both ends of the bus with a special RC network designed to reduce signal ringing. The CC10 motherboard is shown in Figure 12.

MD-CC10 MOTHERBOARD WITH DIMENSIONS

Figure 12



The MD-CC12A (MK77970) is a twelve-slot card cage faricated from aluminum. Figure 13 shows the dimensions of the MD-CC12A card cage. Power connections to the MD-CC12A are accomplished via a 4-pin and 2-pin AMP Universal MATE-N-LOK connector. In addition, there is a 3-pin Universal MATE-N-LOK connector for connecting a remote power lamp and a remote reset button. The pin assignments for these connectors are shown in Table 3, with holes denoted from the component side left to right.

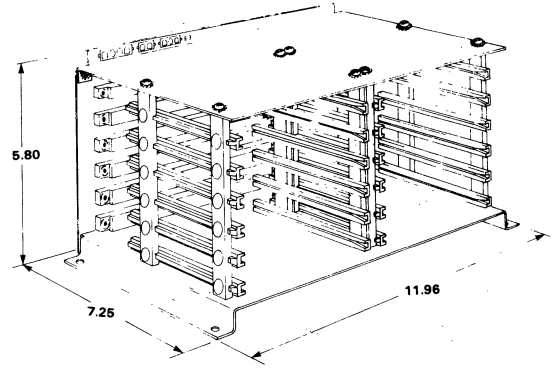
INTERCONNECTION OF POWER PLANE TO STD BUS — CC10, CC12A

Table 3

CONNECTION PINS (Left to Right)	DESIGNATOR	STD BUS PIN DESIGNATOR
4-Pin		
1	+5 V	1, 2
2	GND	3, 4
3	-12 V	56
4	+12 V	55
2-Pin		
1	AUX GND	53, 54
2	+5 V	5, 6
3-Pin		
1	GND	3, 4
2	+12 V	55
3	/PBRESET	48

MD-CC12A DRAWING WITH DIMENSIONS

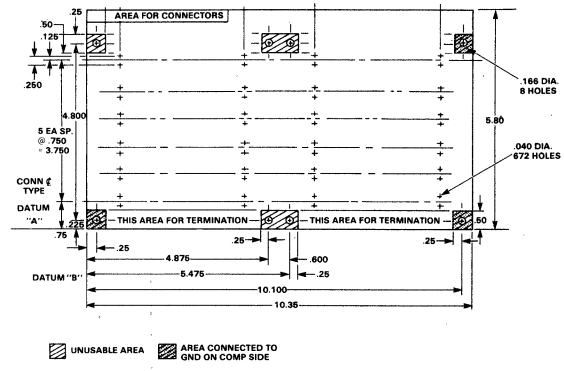
Figure 13



The MD-CC12A card cage motherboard is terminated at both ends of the bus with a special RC network designed to reduce signal ringing. The CC12A motherboard is shown in Figure 14.

MD-CC12A MOTHERBOARD

Figure 14

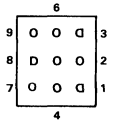


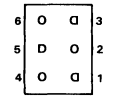
The MD-CC16 is a 16-slot card cage which can be wall mounted or rack mounted. It is constructed from steel giving it greater strength for industrial environments. (See Figure 15 for a drawing of the 16-slot card cage dimensions). There are two AMP MATE-N-LOK connectors (a 9-pin and 6-pin) which connect power to the card cage. Note that the connectors can be placed in one to two orientations, either on the left side or the top of the card cage (see Figure 15). In addition, the right side of the cage has a rectangular hole through which cables can be passed for connection to the MD cards. Table 4 gives the two connector pinouts for CC16.

INTERCONNECTOR OF POWER PLANE TO STD BUS — MD-CC16

Table 4

CONNECTION PINS	DESIGNATOR	STD BUS PIN DESIGNATOR
9-Pin		
1, 2,	+5 V	1, 2
3	+5 V SENSE	
4, 5, 7, 8	GND	3, 4
6	GND SENSE	
9	No connect	
6-Pin		
1	/PBRESET	48
2	AUX GND	53,54
3, 4	GND	3, 4
5	+12 V	55
6	-12 V	56

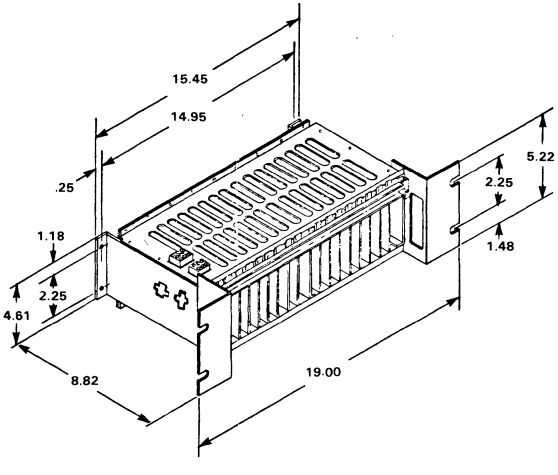




The mating connectors for the above pins are listed in the CONNECTORS section.

MD-CC16 DRAWING WITH DIMENSIONS

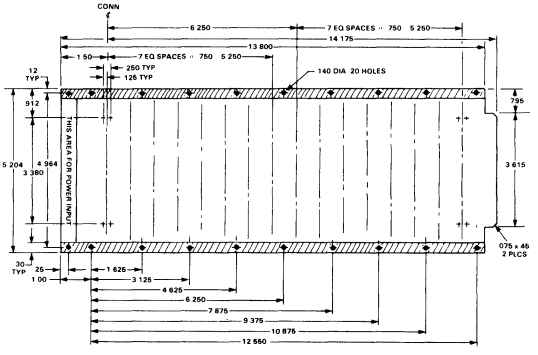
Figure 15



The MD-CC16 card cage motherboard is terminated at both ends of the bus with a special RC network designed to reduce signal ringing. The CC16 motherboard is shown in Figure 16.

MD-CC16 MOTHERBOARD WITH DIMENSIONS

Figure 16



I/O Expand/Memory Expansion

Each card cage motherboard has two stake pins (IOEXP and MEMEX) which are connected to bus pins 35 (IOEXP) and 36 (MEMEX). If the IOEXP (I/O Expand) pin is not used to must be strapped to the logic ground stake pin opposite pin IOEXP. If the MEMEX (Memory Expansion) pin is not used it must be strapped to the logic ground stake pin opposite pin MEMEX.

Card Priority

If a card slot is not used, the user can maintain the priority interrupt chain by strapping across the unused connector to terminal points provided on the assembly side of the motherboard of each card cage (opposite pins 51 and 52).

The interrupt priority for the MD-CC6 is highest at the bottom of the cage. The priority for the MD-CC6-WM, MD-CC10, and MD-CC16, is from right to left as viewed from the front, with the highest priority board at the right side.

The interrupt priority for the MD-CC12A card cage is from bottom to top on the right, then from bottom to top on the left side when viewed from the front with components facing upward. Therefore, the bottom-most board on the right side is the highest priority board, and the top-most board on the left side is the lowest priority board.

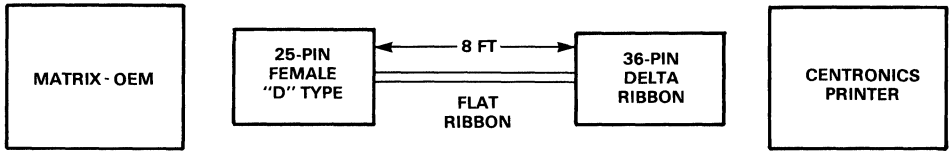
CONNECTORS

FUNCTION	CONFIGURATION	MATING CONNECTOR
STD BUS	56-Pin 0.125 in. centers	PRINTED CIRCUIT Viking 3VH28/ICE5 WIRE WRAP Viking 3V38/ICND5 SOLDER LUG Viking 3VH28/ICN5
Card Cage Mating Connectors	CC10 2-Pin SIP 3-Pin SIP 4-Pin SIP Contacts	PLUG HOUSING AMP 350777-1 PLUG HOUSING AMP 350766-1 PLUG HOUSING 350779-1 Socket AMP 350551-1
	CC12 2-Pin SIP 3-Pin SIP 4-Pin SIP Contacts	PLUG HOUSING AMP 350777-1 PLUG HOUSING AMP 350766-1 PLUG HOUSING AMP 350779-1 Socket AMP 350551-1
	CC16 6-Pin 9-Pin Contacts	PLUG HOUSING AMP 350715-1 PLUG HOUSING AMP 350720-1 Pin AMP 350552-1

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MDX-WW1	Wire-wrap card with bussed power and ground.	MK77959
MDX-WW2	Wire-wrap card without bussed power and ground.	MK77952
MD-EXT	Extender Card	MK77953
MD-232DCE-C	25-pin "D" female MD cable	MK77955
MD-232DTE-C	25-pin "D" male MD cable	MK77970
MK-TTY-C	15-pin Molex-TTY cable	MK77956
MD-PPG-C	25-pin "D" female PROM Programmer (PPG-8/16) interface cable	MK77957
MD-CC6	6-slot card cage with STD BUS motherboard	MK77973
MD-CC6-WM	6-slot wall mount card cage with STD BUS motherboard	MK77978
MD-CC10	10-slot card cage with STD BUS motherboard	MK77989
MD-CC12A	12-slot card cage with STD BUS motherboard	MK77990
MD-CC16	16-slot card cage with STD BUS motherboard	MK77977

MATRIX-80/OEM TO (MD-PTR2-C) CENTRONICS PRINTER CABLE (MK79099)



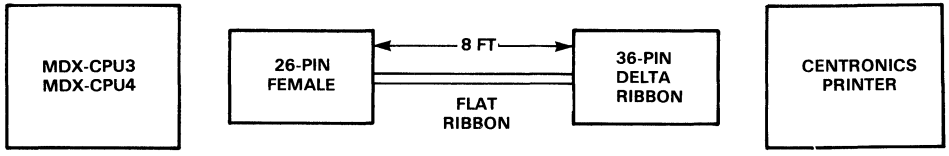
MD-PTR2-C DESCRIPTION

The MD-PTR2-C (MK79099) is an 8-foot long cable designed to interface the MATRIX-80/OEM enclosure to a parallel Centronics printer. One end of the cable has a 25-pin male "D" type connector to connect the MATRIX-80/OEM (I/O panel J1.) The other end has a 36-pin delta ribbon plug connector that will mate with the standard Centronics parallel interface connector on the printer.

ORDERING INFORMATION

Designator	Description	Part Number
MD-PTR2-C	MATRIX-80/OEM to Centronics	MK79099
	Printer Cable	
	Data Sheet Only	

MDX-CPU3/4 TO CENTRONICS (MD-PTR1-C) PRINTER CABLE MK79098



MD-PTR1-C DESCRIPTION

The MD-PTR1-C (MK79098) is an 8-foot long cable designed to interface the MDX-CPU3 or MDX-CPU4 STD modules to a parallel Centronics printer. One end of the cable has a 26-pin socket to connect to the STD Printer bus board. The other end has a 36-pin delta ribbon plug connector that will mate with the standard Centronics parallel interface connector.

ORDERING INFORMATION

Designator	Description	Part Number
MD-PTR1-C	MDX-CPU3/4 to Centronics	MK79098
	Printer Cable	
	Data Sheet Only	

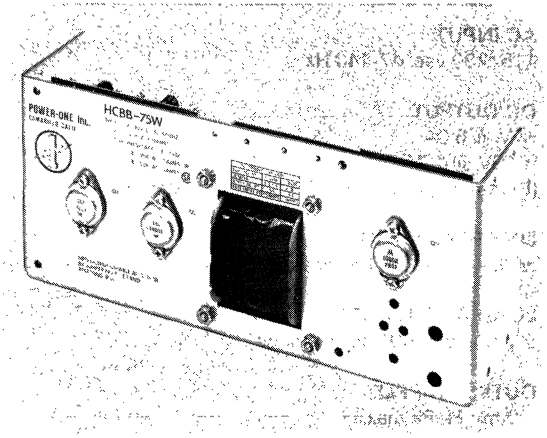
MD-PWRI
MK77964

FEATURES

- ☐ Triple output supply: +5 volts and ± 12 volts
- ☐ 115/230 vac ± 10%, 47-440 Hz
- ☐ Remote sensing on 5V output
- ☐ Overvoltage protection on 5V output
- ☐ ± 0.05% regulation
- ☐ Foldback current limit
- ☐ I.C. regulated design
- ☐ UL recognized
- ☐ CSA certified
- ☐ STD or STD-Z80 BUS compatible

MD-PWR1 PHOTO

Figure 1



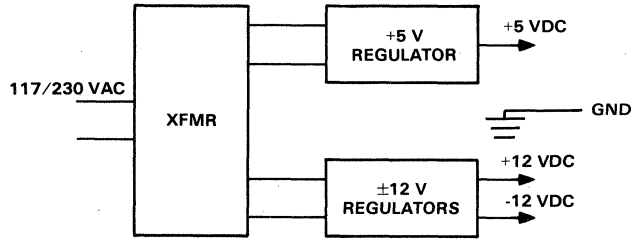
DESCRIPTION

The MD-PWR1 is an open-frame power supply. Designed to furnish power for the MDX-PROTO kit, the MD-PWR1 operates from 115/230 vac ± 10% at a frequency range of 47 to 440 Hz. This input power is then transformed and regulated into the three output voltages, +5 VDC and ± 12 VDC. The open-frame design allows for adequate cooling.

IVF

MD-PWR1 BLOCK DIAGRAM

Figure 2



AC INPUT
115/230 vac, 47-440 Hz

DC OUTPUT
+5V @ 6.0A
± 12V @ 1.7A
(Derate output current 10% for 50 Hz operation)

LINE REGULATION
±.05% for a 10% line change

LOAD REGULATION
± .05% for a 50% load change

OUTPUT RIPPLE
3.0 mV Pk-Pk max.

TRANSIENT RESPONSE
30 microseconds for 50% load change

SHORT CIRCUIT AND OVERVOLTAGE PROTECTION
Automatic current limit/foldback

REVERSE VOLTAGE PROTECTION
Provided on output and pass element

OVERVOLTAGE PROTECTION
Optional on ± 12V outputs

REMOTE SENSING
Provided on 5V output, open-sense-lead protection built-in

STABILITY
± 0.3% for 24 hours after warm up

TEMPERATURE RATING
0°C to 50°C full rated
(derate linearly to 40% at 70°C)

TEMPERATURE COEFFICIENT
± .03%/°C max.

EFFICIENCY
5V output: 45%, ± 12V output: 55%

VIBRATION AND SHOCK
Per MIL-STD-810B

SIZE
4.75 in (120.7 mm) wide x 11.0 in (279.4 mm) long x 2.75 in (69.9 mm) high

WEIGHT
8 lbs (3.6 kg)

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MD-PWR1	Power Supply Module with prestripped and tinned wires	MK77964

MD-RMC12

FEATURES

- ☐ Standard 19-inch rack-mountable chassis
- ☐ Removable structural-foam front panel for internal access
- ☐ Front panel RESET switch and POWER indicator
- ☐ 12-slot card cage
- ☐ Cards mounted horizontally for ease of cooling and cable routing
- ☐ Self-contained power supply and 115 CFM fan
- ☐ 100/115/230 Volt 50/60 Hz operation

GENERAL DESCRIPTION

The Mostek MD Series Rack Mounted System (MD-RMC12) provides rack mounting for the MD series Microcomputer modules. The system features a self-contained power supply designed to work on voltages and frequencies available worldwide. A structural foam front panel is provided with a system RESET switch and POWER indicator. The front panel is designed with quick-release ball studs so that it can be removed quickly for access to internal components. The card cage and power supply may be removed individually from the front or top for improved access. The cards are mounted in a horizontal plane with provisions for cabling over the card cage to the rear I/O panel. The back panel has an I/O panel prepunched for fifteen 25-pin D type connectors, one 50-pin D connector, and one BNC connector. AC components on the back panel include: On/Off switch, voltage selection switch, fuse holder (3 AG or 5 x 20 mm), and AC input receptacle/line filter.

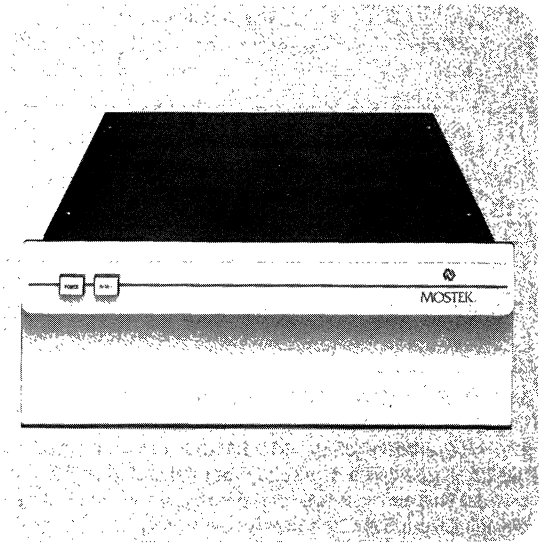
MOTHERBOARD CONNECTORS

The twelve connectors (J1-J12) mounted on the motherboard are dual readout, 56 pin .125" centers, card edge style. Power is connected to the motherboard by three connectors, J13, J14, and J15. The pinout for J13 and J14 is shown in Table 1.

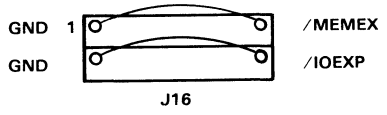
The motherboard is also the attachment point for the RESET button and POWER indicator on the front panel. This attachment is by the 3 pin connector J15. The front panel RESET switch is connected to pin 48 (/PBRESET) or the system bus, which initializes the system upon depression. The pinout for connector J15 is shown in Table 2.

One other connector is provided to the signals /MEMEX (pin 36) and /IOEXP (pin 35) to ground. These signals are not used by the Mostek STD-Z80 BUS, but may be tied low for compatibility with other boards by inserting mini-jumpers or wire. Wrap wires on J16 are shown in Figure 2.

MD-RMC12
Figure 1



J16 WIRE WRAPS
Figure 2



IVF

J13 AND J14 PINOUT

Table 1

J13	Pin	Wire Color	Connector
+5	1	Red	
GND	2	Black	AMP Universal Mate-n-lok
-12	3	White	PCB Pin Housing #350792-1 (supplied)
+12	4	Blue	Plug Housing #350779-1 (Using four Socket Contacts)

J14	Pin	Wire Color	Connector
AUX GND	1	Not supplied	AMP Universal Mate-n-lok
-5	2	Not supplied	PCB Pin Housing #350786-1
			Plug Housing #305777-1 (Using two Socket Contacts)

J15 PINOUT

Table 2

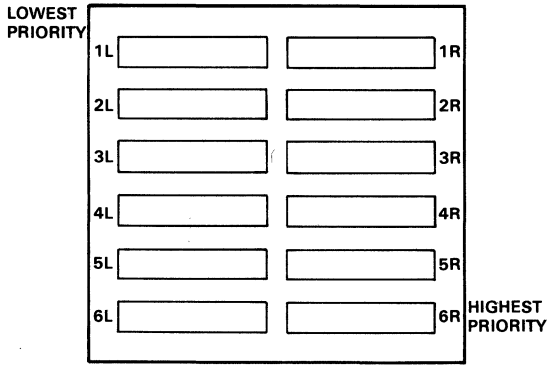
J15	Pin	Wire Color	Connector
GND	1	Black	AMP Universal Mate-n-lok
+12	2	Orange	PCB Pin Housing #350789-1 (supplied)
/PBRESET	3	Yellow	Plug Housing #350-766-1
			(Using 3 Socket Contacts)

MOTHERBOARD INTERRUPT PRIORITY CHAIN

The motherboard of the MD-RMC12 CPU subsystem is designed to allow a daisy chain of interrupt logic between boards. This wiring is accomplished by connecting PCO (pin 51) to PCI (pin 52) of the next lower priority board from slot 6R to slot 1R, to 6L to 1L. The twelve-slot daisy chain priority of the motherboard is shown in Figure 3. Provision has been made for jumper wires in case the user wishes to leave a slot open while still preserving the daisy chain. This is provided by wires E1-E11, with proper connection shown in Table 3.

TWELVE-SLOT PRIORITY CHAIN

Figure 3



JUMPER WIRE CONNECTIONS WITH DAISY CHAIN PRIORITY

Table 3

If no card is in:		Connect	To
J1	6R	—	—
J2	5R	E1	E2
J3	4R	E2	E3
J4	3R	E3	E4
J5	2R	E4	E5
J6	1R	E5	E6A
J7	6L	E6B	E7
J8	5L	E7	E8
J9	4L	E8	E9
J10	3L	E9	E10
J11	2L	E10	E11
J12	1L	—	—

I/O CONNECTORS

The rear panel is shipped with no internal I/O cabling connectors installed. This prepunched panel has provisions for 15 25-pin "D" subminiature connectors, one 50-pin "D" type connector, and one BNC bulkhead connector. The typical connectors used are shown in Table 4. Should the user desire to fabricate his own I/O panel, the panel is simply held in place by four screws.

I/O CONNECTORS

Table 4

25-Pin "D"	ANSLEY	609-25S (Insulation Displacement)
	WINCHESTER	49-1125S (Insulation Displacement)
	AMPHENOL	17-10250 (Discrete Wire)
50-Pin "D"	ANSLEY	609-50F

SWITCH AND INDICATOR FUNCTIONS

The MD-RMC12 SUBSYSTEM has three switches and one indicator light as follows:

Power ON/OFF switch	Right Rear Panel (S1)
Power selection switch	Right Rear Panel (S2)
POWER ON indicator light	Left Hand Indicator on Front Panel
RESET push button	Right Hand Button on Front Panel

The RESET button connects the /PBRESET signal of the STD BUS to LOGIC GROUND when pressed. This generates a RESET signal to the CPU.

POWER SELECTION

The system has a power selection switch (S2) on the upper right-hand rear panel to select between 115 V ± 10% operation or 230 V ± 10% operation. Set the switch so the primary voltage available shows through the hole in the rear panel. The MD-RMC12 will operate at either 50 or 60 Hz.

100 V AC OPERATION

The MD-RMC12 CPU subsystem can be operated at 100 V ± 10%; however, the following internal wiring changes must be made.

1. Remove the top from the subsystem.
2. Unsolder the blue/white wire from pin 1 on the power transformer.
3. Solder the solid blue wire on pin 2 of the power transformer.
4. Place the power selection switch (S2) in the 115 volt position.
5. Replace the top lid. System is now configured for 100 volt ± 10% operation.

FUSE SELECTION

If the voltage selector switch is changed from the factory setting indicated on the rear panel label, the fuse size may need to be changed. Refer to the following table for the correct fuse size for a given voltage selector setting.

United States systems (60 Hz) are shipped with a 3 AG (3 Amp) fuse in a grey fuse insert. European systems (50 Hz) are shipped with a 5 x 20 mm (3 Amp) fuse in a black fuse insert.

SPECIFICATIONS

Electrical Specifications

Input Power: 110/115/230 volts ac ± 10% 50/60 Hz

DC Power Available: +5 Vdc at 12 A max.
+12 Vdc at 1.7 A max.
- 12 Vdc at 1.7 A max.

Load Regulation: ± .05% for a 50% load change

Ouput Ripple: 3.0 mV PK-PK-max

Transient Response: 30 microseconds for a 50% load change

Short Circuit and Overload Protection: Automatic current limit/foldback

Overvoltage Protection: +5 volt output, set to 6.2 ± 0.4 volts

Stability: ±0.3% for 24 hours after warm-up

Thermal Protection: Bi-metal thermostat in primary ac line set to open at 180°F (82°C); close at 130°F (55°C)

Card Cage: 12-slot for MD series module 11.4 cm x 16.5 cm (4.5 x 6.5 in.). Connectors are the 56-pin edge card specified for the STD BUS

Fusing:

Line Voltage	MK77966 (MD-RMC12)	MK77975 (MD-RMC12-50)
100/115 V	3 Amp 3 AG*	3 Amp 5 x 20 mm
230 V	1.5 Amp 3 AG	1.5 Amp 5 x 20 mm*

*Configuration as shipped

Line Cord Supplied:

MK77966	MK77975
Similar to Beldon 17250B	Similar to Fell Model 1100

Front Panel Controls: RESET Switch
POWER-ON Indicator

Rear Panel Controls: ac Power ON/OFF
ac Fuse Holder
ac Line Receptacle/Filter
ac Line Voltage Selector

Mechanical Specifications

Weight: 25 lbs (11.3 kg)

Chassis: (a) 19" rack mountable. Using the two rails supplied
(b) Slide mounting available with optional slide mounting kit. Requires two inches of panel space below the unit.

Order Mostek part number MK78193 SLD Kit.

Operating Temperature Range: 0°C to 60°C

Dimensions:

Height - 7.0 in. (17.8 cm) panel space
7.3 in. (18.5 cm) overall, includes feet

Width - 19.0 in. (48.3 cm) at front panel
17.5 in. (44.5 cm) behind front panel

Depth - 21.6 in. (54.9 cm) with all protrusions
20.0 in. (50.8 cm) without foam front

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MD-RMC12	Rack-mounted CPU subsystem with MD series 12-slot card cage with U.S. line cord and fuse. 100/115/230 Volts 50/60 Hz AC operation, front panel, support bracket for rack mounting, and Technical Manual included.	MK77966
MD-RMC12-50	Same as above except with 5 x 20 mm fuse and European line cord.	MK77975
MD-RMC12 Technical Manual	MD-RMC12 Technical Manual Only	4420086

RACK-MOUNTABLE, DUAL-FLOPPY-DISK ENCLOSURE RMDFSS, RMDFSS-50

FEATURES

- ☐ Standard 19-inch rack-mountable chassis; 7-inch panel height
- ☐ Removable structural-foam front disk bezel for internal access
- ☐ Front panel power-on indicator
- ☐ Mounts two standard 8-inch floppy disk drives
- ☐ Disk Drives mounted horizontally for low profile
- ☐ Self-contained power supply and 115 CFM fan
- ☐ 100/115/230 volt, 50/60 Hz operation

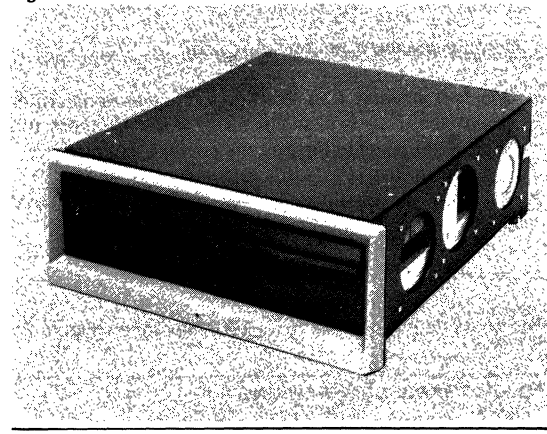
DESCRIPTION

The RMDFSS is a rack-mountable enclosure for two standard 8-inch floppy-disk drives. The enclosure is fully self-contained with disk drives, power supply, and fan. The RMDFSS is compatible with Mostek's Z80 based microcomputer systems, but can be used with any system which has a suitable disk interface.

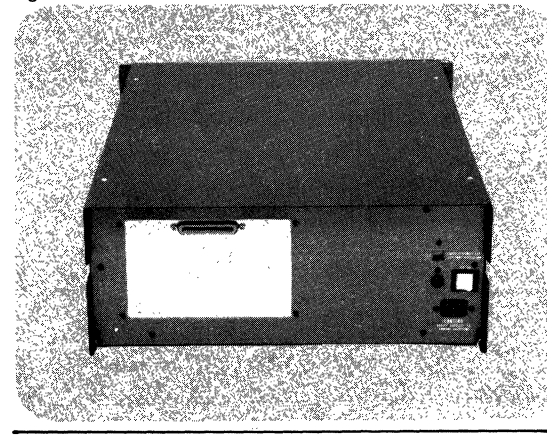
The power supply works on voltages and frequencies available world wide, and provides cooling with a 115 CFM fan. The two single-sided floppy-disk drives are mounted in a horizontal plane for a low-profile appearance and to conserve panel height in the rack. The enclosure has an attractive structural-foam front bezel where the power-on indicator light is located. Both the front bezel and metal top have quick release ball studs for easy access to the drives and power supply for maintenance. The back panel has an I/O panel pre-punched for one 50-pin "D" type connector for interface to the disk controller. AC components on the back panel include: ON/OFF switch, voltage selection switch (S2), fuse holder, and AC input receptacle/line filter.

The RMDFSS has a standard 19-inch wide chassis and requires a 7-inch panel clearance. Included are two stainless steel angle brackets which mount in the user supplied enclosure to provide support along the sides of the disk unit. An optional slide kit is available from Mostek by ordering MK78193 SLD KIT.

RMDFSS-FRONT VIEW
Figure 1



RMDFSS-REAR VIEW
Figure 2



UNPACKING AND INSPECTION

Remove the RMDFSS from the shipping container carefully. Remove the soft foam inserts located in the diskette openings.

Inspect the subsystem for shipping damage. Check for loose connectors or wires which may have been unseated during shipment. In case of damage, place a claim against the shipping agent.

INSTALLATION

POWER SELECTION

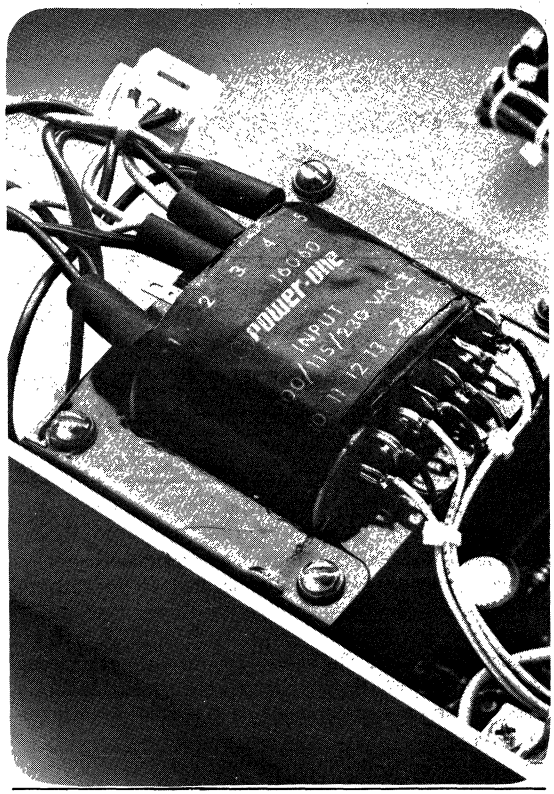
The RMDFSS has a power selection switch (S2) (see Figure 2) to select either 115 V ±10% or 230 V ±10% operation. Set the switch so the primary voltage available shows through the hole in the rear panel. The disk module is factory configured for either 50 Hz or 60 Hz (verify correct frequency for your installation on the rear panel label).

The RMDFSS can be operated at 100 V ± 10% by making the following internal wires changes:

1. Remove the top from the subsystem.
2. Unsolder all wires from Pin 1 on the power transformer except the blue-with-white stripe wire. Connect the unsoldered wires to Pin 2 of the power transformer.
3. Place the power selection switch (S2) in the 115 V position.
4. Replace top lid.

The subsystem is now wired for 100 V operation (Figure 3).

POWER TRANSFORMER WIRING
Figure 3



FUSE SELECTION

If the voltage selector switch is changed from the factory setting (as indicated on the rear panel label), the fuse size may need to be changed. The following table lists the correct fuse size for a given voltage selection:

100 Volt	115 Volt	230 Volt
3 Amp	3 Amp	1.5 Amp

Systems shipped in the United States (60 Hz) have a 3 AG (3-Amp) fuse in a grey fuse insert. European systems (50 Hz) are shipped with a 5 x 20mm (3-Amp) fuse in a black fuse insert.

SWITCH AND INDICATOR FUNCTIONS

The RMDFSS has two switches and one indicator with the following functions:

Power-on Switch (S1) - power-on subsystem

Power Selection Switch (S2) - selects AC line voltage

Power-on Indicator - illuminates when power is on

DISK CONFIGURATION AND INTERFACE CONNECTOR

The floppy-disk drives shipped in the RMDFSS are the following (or equivalent):

Shugart 800-2 single-sided 50 Hz, PN 853104
Shugart 800-2 single-sided 60 Hz, PN 850104

The drives are standard models and include write protect. Jumpers installed on the disk drives are as follows:

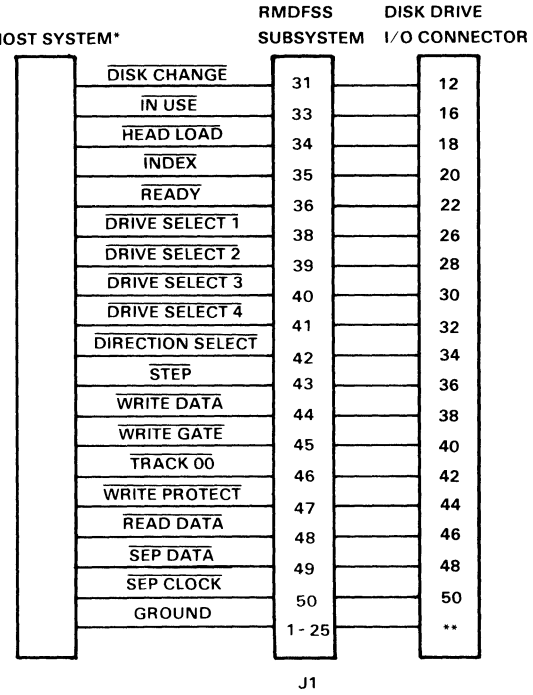
Logical Unit (DK1) (left drive viewed from front)	Logical Unit (DK0) (right drive viewed from front)
A	A
B	B
C	C
HL	T2
Y	HL
800	Y
T1	800
T2	DS1
T3	
T4	
T5	
T6	
DS2	

All other jumpers are open.

The interface connector supplied with the RMDFSS subsystem is a 50-pin, ribbon-contact type, Ansley 609-50F (or equivalent). The mating connector, which is user supplied, is either an

Ansley 609-50M insulation displacement type or the Amphenol 157 series for discrete wire cables. The Shugart equivalent pinout for the interface connector is shown in Table 1.

INTERFACE CONNECTOR PINOUT
Table 1



*USER DEFINED CONNECTOR
**ALL ODD NUMBERED PINS ARE GROUNDED

RMDFSS THERMAL PROTECTION

The RMDFSS contains an integral thermal breaker which will remove AC power should the interior temperature reach 82° C (180° F). AC power will be restored automatically when temperature lowers to approximately 55° C (130° F). Should this occur, check to see that the fan is operating and the enclosure venting is not obstructed.

DISK DRIVE MAINTENANCE

The disk drives require preventive maintenance every 12 months under normal usage. See Table 2 for preventive maintenance procedures. Cleanliness is very important to successful operation of the RMDFSS. The fan should be kept clean and free from dirt and lint. Do not lubricate the disk drive units; oil will allow dust and dirt to accumulate. The read/write heads on the disk drive units should be cleaned only when signs of oxide build-up are present. Oxide build-up will cause premature failure of diskette material. Occasional inspection of read/write heads and diskettes will monitor this condition.

DISK DRIVE REMOVAL

The disk drive units must be removed from the subsystem in order to inspect them or do preventive maintenance. The following procedure describes disk drive removal:

1. Disconnect all power from the RMDFSS.

****CAUTION****
High AC voltages are present within the RMDFSS even with AC switch OFF. Remove line cord from the wall outlet before servicing.

2. Remove lid (top) of RMDFSS by pulling upward to release fasteners.

3. Remove P1 (signal), P4 (AC), and P5 (DC) connectors from back of each drive. The P5 connectors are removed by depressing the tabs extending from the sides of the connectors.

4. Carefully remove the front bezel surrounding the disk drives. A pull from the front will remove the bezel from the chassis.

5. Remove the front and rear screws (3) that hold the bracket below the drive. This connects the baseplate to the disk drive. Note that two screws are visible from the front, and the third screw is visible from the top of the unit between disk drive and power supply.

6. Remove the disk drive unit(s) out the front of the enclosure.

7. Lay the drive upside down (on its top) and remove the four screws that hold the mounting bracket to the drive frame.

8. Replace the drive(s) in reverse order of the above steps.

ELECTRICAL SPECIFICATIONS

Input power: 100/115/230 Volts AC ± 10% 50/60 Hz

DC POWER AVAILABLE: (for disk drives)

+5 VDC at 3.0 A maximum
-5 VDC at 0.5 A maximum
+24 VDC at 3.4 A maximum

LOAD REGULATION: ± .05% for a 50% load change

OUTPUT RIPPLE: 3.0 mV PK-PK maximum

TRANSIENT RESPONSE:
30 microseconds for a 50% load change

SHORT CIRCUIT AND OVERLOAD PROTECTION:

Automatic current limit/foldback

DISK DRIVE PREVENTIVE MAINTENANCE PROCEDURES
Table 2

UNIT	FREQ. MONTHS	OBSERVE	ACTION
Read/Write head	12	Oxide Build-up	Clean Read/Write Head ONLY IF NECESSARY
		Check for proper alignment	Align
Read/Write Head Button	12	Excessive wear	Replace
Stepper Motor and Lead Screw	12	Inspect for nicks and burrs	Clean off oil, dust, and dirt
Belt	12	Frayed or weakened areas	Replace
Base	12	Inspect for loose screws, connectors, and switches	Tighten screws, connectors, and switches

ELECTRICAL SPECIFICATIONS (Cont'd)

OVERVOLTAGE PROTECTION:

+5 volt output, set to 6.2 ± 0.4 volts

STABILITY: ± 0.3% for 24 hours after warmup

THERMAL PROTECTION:

Bi-metal thermostat on primary AC line set to cut out at 82° C (180° F)

FUSING:

Line Voltage:	60 Hz	50 Hz
110/115 V	3 Amp* 3AG	3 Amp 5 x 20mm
230 V	1.5 Amp 3AG	1.5 Amp 5 x 20mm

LINE CORD SUPPLIED:

60 Hz (Beldon No. 17250B)
50 Hz (Feller Model 1100)

FRONT PANEL INDICATOR:

Power-on

REAR PANEL CONTROLS:

AC Power ON/OFF
AC Fuse holder
AC Line receptacle/filter
AC Line voltage selector

MECHANICAL SPECIFICATIONS

WEIGHT: 50lbs. (22.7kg)

OPERATING TEMPERATURE RANGE:

4.4°C to 46.1°C (Disk Drive limitation) or disk media specification, whichever is more stringent.

DIMENSIONS:

Height: 7.0 in. (17.8 cm) panel space
7.3 in. (18.5 cm) overall, (includes rubber feet on bottom)

Width: 19.0 in.(48.3 cm) with front bezel
17.5 in. (44.5 cm) without front bezel

Depth: 21.6 in. (54.9 cm) with all protrusions
20.0 in. (50.8 cm) without front bezel

Humidity: Up to 90% relative, noncondensing

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
RMDFSS	Rack-mountable, dual floppy-disk drive enclosure with 8-inch single-sided disk drives for 100/115/230 volt operation. Includes interface cable to SDE-RMC6 or MD-RMC12, front bezel, and support brackets for rack mounting. 60 Hz model	MK78183
RMDFSS-50	Same as above, 50 Hz model.	MK78185
SLD KIT	Slide mounting for above	MK78193

WARNING: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his measures may be required to correct the interference.

ENCLOSURE
MK77980, MK77981, MK77987, MK77988

FEATURES

- NEMA or 19 inch rack mountable
- CC16 STD BUS card cage, 0.75 inch centers
- 150 or 300 watt triple output switching power supply
- Strain relief for I/O cables
- Barrier strip for DC power
- Fan and buffered air flow for proper cooling
- STD BUS Industrial Enclosure

DESCRIPTION

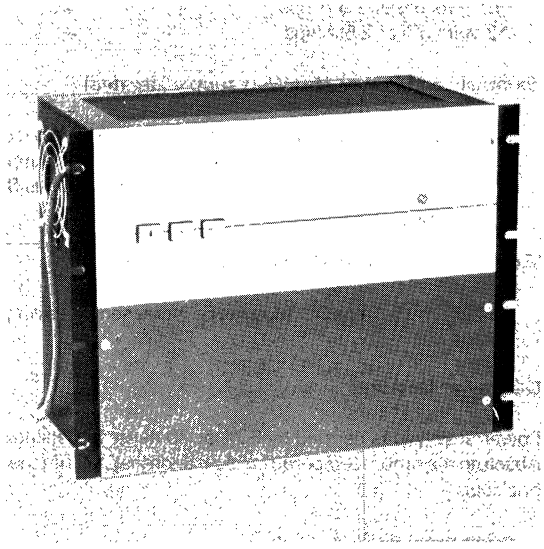
The ICS1 Enclosure provides packaging for STD Bus-based industrial control systems. Provisions have been made for adequate power for all sixteen card-cage slots. The optional 300 watt power supply contains sufficient drive to allow an additional 15 Amp external load (5 volts). In addition, the card cage may be quickly disconnected and removed from the enclosure.

Separate front panels for the card cage and power supply sections are provided. This allows the user to work on the cage and board assembly with power applied to the system with no shock hazard. A disconnect 'switch' in the power supply section removes AC power if the power supply section has its cover and cable removed. The AC power is fused where it enters the system, and the DC power is internally fused in the power supply. Complete overcurrent, overtemperature, and overvoltage protection is built in the power supply.

A special strain relieved port is provided for user I/O cabling to the STD BUS card cage. A terminal strip is provided on the power supply mounting bracket of sufficient size to connect up to 16 loads (300 watt supply, 8 loads with 150 watt supply). Internal mounting provisions are included for a power-fail-detect circuit and transformer assembly. The enclosure may be side or top mounted to a wall or in a rack.

SYSTEM PHOTO

Figure 1



IVF

ELECTRICAL SPECIFICATIONS

AC Power Requirements

Nominally 115/230 volts AC. Operating range 90-132 VAC, 47-63 Hz, single phase, internally changeable to 180-264 VAC.

AC Fuse Requirements

Slow blow fuse only.

150 Watt supply - 115 volt = MDL 5 Amp 250 volt (3AG)
230 volt = MDL 5 Amp 250 volt (3AG)
300 Watt supply - 115 volt = MDL 10 Amp 250 volt (3AG)
230 volt = MDL 10 Amp 250 volt (3AG)

DC Power Available

Adequate power is provided for a full card cage of STD BUS compatible boards plus an external load. The user is cautioned to check total power supply loading and derating data.

Card Cage Power 150 Watt supply (derated)
+5 volts 5% at 14 Amps
+12 volts 5% at 2.5 Amps
-12 volts 5% at 1 Amps

Card Cage Power 300 Watt supply (derated)
+5 volts 5% at 15 Amps
+12 volts 5% at 2.5 Amps
-12 volts 5% at 2.5 Amps

External Load Power 150 Watt supply (derated)

Nominally 1 Amp DC. May be increased by using fewer than 16 boards in the card cage. Approximately one Amp gained for each slot left empty. Absolute maximum is 8 Amps.

External Load Power 300 Watt supply (derated)

Maximum 15 Amps DC. May not be increased by leaving boards out.

DC Power Derating

Power supply was derated by 50% at 70 degrees Celsius. Absolute maximum temperature is 75 degrees C within the enclosure.

Overtemperature Protection

Power supply shuts down when internal temperature exceeds maximum safe rating. Unit automatically reverts back to normal operation when internal temperature is within safe limits.

Overload Protection

Current foldback overload protects against momentary overload. Short circuit protection is continuous without damage; current is limited to approximately 50% of rated load current. Outputs are dynamically protected from foldback lock-up. Recovery from overload is automatic. Outputs 2 and 3 (+12 and -12 volt) are set to 20% of rated current.

Overvoltage Protection

Output power is removed when the output voltage exceeds an internally set trip point. The trip point is factory set at 6 to 6.5 volts on the main +5 volt output. This protection is reset by cycling the input power. Outputs 2 and 3 also have this feature. Their trip point is set at 110% to 120% of their nominal output voltage.

Power Supply Minimum Loading

To obtain full current from the +12 and -12 volt outputs of the 150 Watt supply, the +5 volt output must have a minimum load of 3.6 Amps. The 300 Watt supply requires a minimum load of 7.2 Amps.

Operating Temperature Range

0°C to 60°C Ambient

MECHANICAL SPECIFICATIONS

Height	13.97 inches	354.8 mm
Width	19.0 inches	482.6 mm
Depth	9.53 inches	242.1 mm
Top Clearance	NONE	
Bottom Clearance	1.75 inches	44.4 mm
Front Clearance	0.5 inch	12.7 mm
Rear Clearance	N/A	
Right Side Clearance	0.5 inch	12.7 mm
Left Side Clearance	1.5 inch	38.1 mm
Weight		
ENCL, ENCL2	32 lb	14.5 kg
ENCL1, ENCL3	28 lb	12.7 kg

Connectors

Function	Description	Mating Connector
STD BUS	56-pin, dual	Viking 3VH28/1CE5 (printed circuit) Viking 3VH28/1CND5 (wire-wrap) Viking 3VH28/1CN5 (solder lug)

SYSTEM INSTALLATION

This system may be mounted in a 19-inch RETMA rack, or mounted to a wall or other vertical surface. AC input power is brought into the enclosure from the left. Input and output connectors for signals and dc power leave the box from the right side panel. These may then be routed to the external loads. The input ac power may be derived from the power cord assembly, or the cord may be removed and ¾ inch conduit cable may be used to install the power connections permanently.

Wall Mounting

Two mounting support brackets are bolted to the rear sides of the enclosure with ten (10) #8-32 bolts and lock washers as shown in Figure 2. The top and bottom of the enclosure may be used as mounting points if desired (see Figure 3). The complete assembly of enclosure and brackets may then

be mounted using bolts or screws to a flat surface. This enclosure requires at least a 14-inch by 19-inch flat surface for proper mounting.

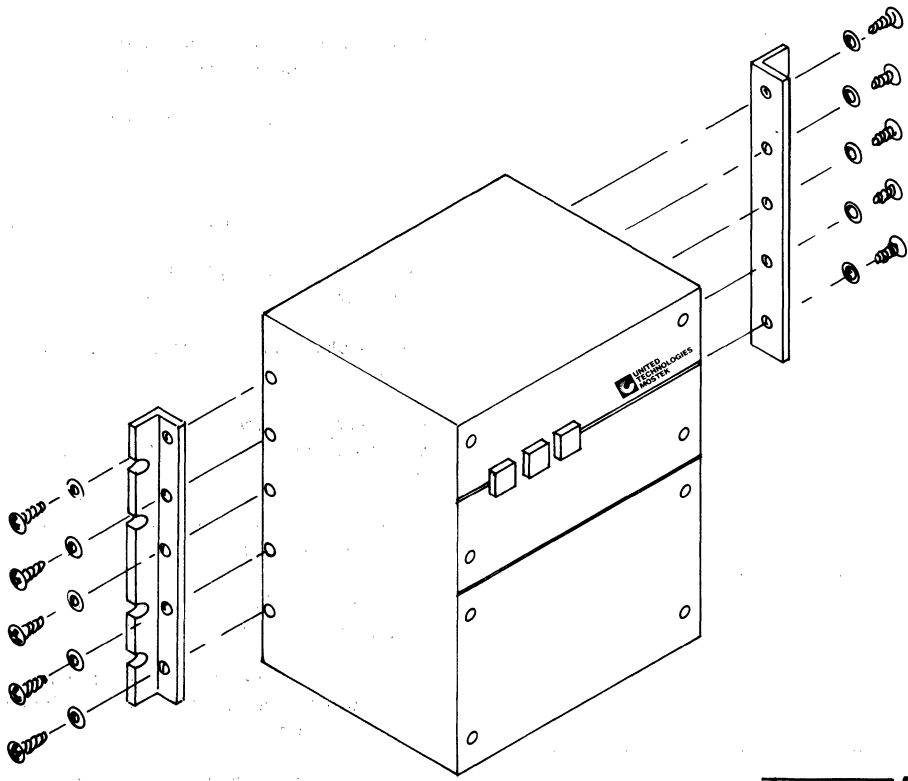
Rack Mounting

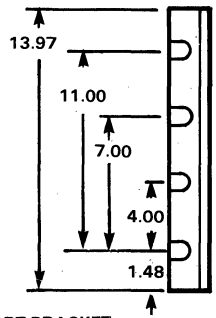
The ENCL is shipped ready for rack mounting. The two mounting support brackets are attached to the front sides of the enclosure. Ten (10) #8-32 bolts are used to hold the brackets in place. The enclosure may be installed in a 19-inch RETMA rack using mounting bolts or other appropriate hardware. The enclosure requires a 14-inch high rack space, plus a 1¾ inch gap on bottom for cooling purposes.

Clearance

When installing the enclosure, it is important to allow at least 1¾ inch clearance on the bottom to ensure adequate ventilation.

ASSEMBLY OF MOUNTING BRACKETS FOR WALL MOUNTING (SIDE)
Figure 2



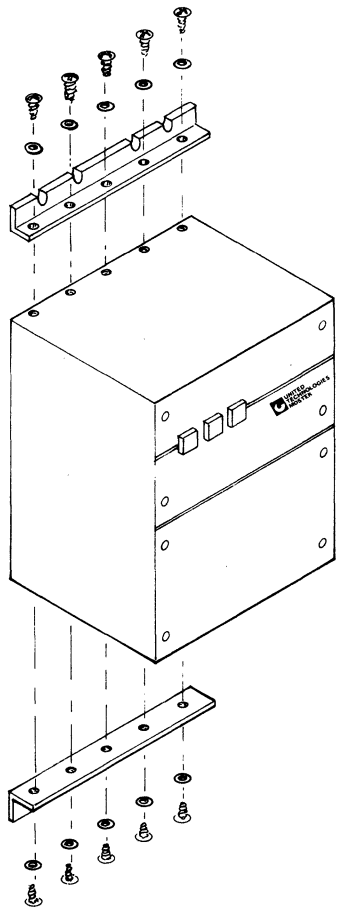


DETAIL, MOUNTING SUPPORT BRACKET.

IVF

ASSEMBLY OF MOUNTING BRACKETS FOR WALL MOUNTING (TOP)

Figure 3



LINE WIRING

The ENCL may be used with input voltages from 90 to 132 V ac or 180 to 264 V ac depending on the model. If necessary, the user may reconfigure the system from 90-132 V ac to 180-264 V ac or vice-versa by changing an internal jumper in the power supply. The user should ensure that the fan is operating with the appropriate voltage power supply.

115-230 Volt Operation

To reconfigure the system for 115 or 230 volt operation, it is necessary to remove the power supply from the system if the system uses an AC/DC power supply. The power supply will have the AC/DC label readily in view. See the end of this description should your power supply be a Deltron power supply. Disconnect external ac from the system before removing the power supply. Failure to do so could create a serious shock hazard to the user. Fan operation speed will be affected by a difference in input voltage.

a. Remove upper front panel of unit and disconnect the cable from inside.

b. Disconnect three connectors from power supply and dc wiring from terminal strip on power supply.

c. Remove card cage and associated connectors from the ENCL.

d. Remove the three screws from the heat shield and power supply underneath the power supply.

e. Remove the three nuts and washers holding the power supply mounting brackets on the rear wall of the enclosure.

f. Carefully remove the power supply from the Enclosure.

g. Remove the mounting brackets from the power supply (four [4] screws on the bottom).

h. Remove all wiring from the front panel area of the power supply.

i. Loosen only the nine (9) screws (ten if 300 watt model) securing the power supply cooling fins but do not remove the fins.

j. Remove the five (5) to eight (8) screws (depending on case size) from the front panel area of the supply.

k. Remove the six (6) screws on the sides of the power supply which hold the cover to the chassis.

l. Slide the cover forward until the terminals and barrier strips have cleared their cutouts on the front panel and then lift it to remove.

m. Remove the two screws on the heat radiator which hold the ac converter board to the heat radiator. The converter board is the assembly which includes the ac input barrier strip (see Figure 4 and 5).

n. For the 300 W power supply, bend the bottom of the power supply cover down until the input converter can be unplugged from its mating connector to the motherboard assembly. Unplug the input converter from the motherboard.

o. Connect JPR1 as shown in Figure 4 or 5 for 110 volt operation. Disconnect JPR1 as shown in Figure 4 or 5 for 230 volt operation.

p. Some models may also have Jumpers 2 and 3. For 110 volt operation on these models, remove JPR3 and install JPR1 and JPR2. For 230 volt operation, remove JPR1 and JPR2 and install JPR3.

q. Assembly is the reverse of disassembly. The screws are hardened thread rolling screws and special care must be taken to prevent thread stripping. All mechanical connections should be tight in order to minimize EMI requirements.

NOTE: The ENCL product series is configured at the factory for 110 V or 230 V operation and it is suggested that you consult the factory before making any alterations in the voltage configuration.

Some systems may be shipped with a Deltron Power Supply. If so, a voltage select option is provided via a terminal block located on the power supply. This terminal is clearly marked 115 V/230 V.

CARD-CAGE REMOVAL

The ENCL is designed to allow quick removal and replacement of the card cage. Cable disconnect is accomplished by two snap connectors mounted on the card cage. The card cage is attached to the rear of the enclosure with four (4) quarter-turn fasteners.

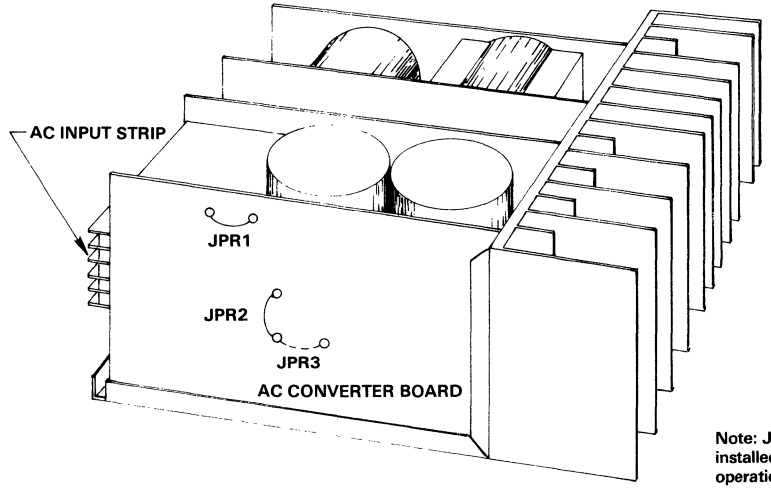
DC Wiring

A terminal block (TB2) is provided for distribution of logic ground and +5-volt power to external devices. The user is cautioned to check total loading on the power supply when powering external devices. Do not locate external devices more than 50 ft. from ENCL. The terminal block (TB2) will accept wire sizes AWG #22 to #14. It is recommended that AWG #14 (wire) be used to minimize IR drop in cabling to the external loads. An access hole, one and one-half (1½) inch in diameter, is provided for routing wire to the external devices. Separate VCC (+5 volt) and ground wires should be used to power each load device to minimize load crosstalk and IR drop. The terminal block will accept spade lugs, ring lugs, or bare wire terminations.

Power-Fail Detect (MDX-PFD)

The Power-Fail Detect modules (MK77979) may be installed in this enclosure and has to be ordered separately and installed by the user. The ac voltage transformer board and cover mounts on the four (4) #6-32 female studs on the rear surface of the enclosure. The MDX-PFD board plugs into the card cage and is connected to the transformer via a 2-wire cable. The 115/230 volt ac is routed to the transformer via the ac input terminal strip TB1 located on the left side wall of the enclosure. See PFD Technical Manual for connection of the ac input to the ac transformer board. The connection is dependent on the line voltage.

300 WATT AC CONVERTER ASSEMBLY
Figure 4



Note: Jumpers shown installed for 110 volt operation.

Card-Cage I/O Cable Routing

The I/O cables which connect to MDX cards installed in the card cage should be routed to the right in front of the card cage through the cable port on the right. The strain relief bracket on the right is used to secure the flat cables for distribution to external devices. Secure cables against the bracket and tighten the two (2) thumbscrews.

MDX Circuit Board Installation

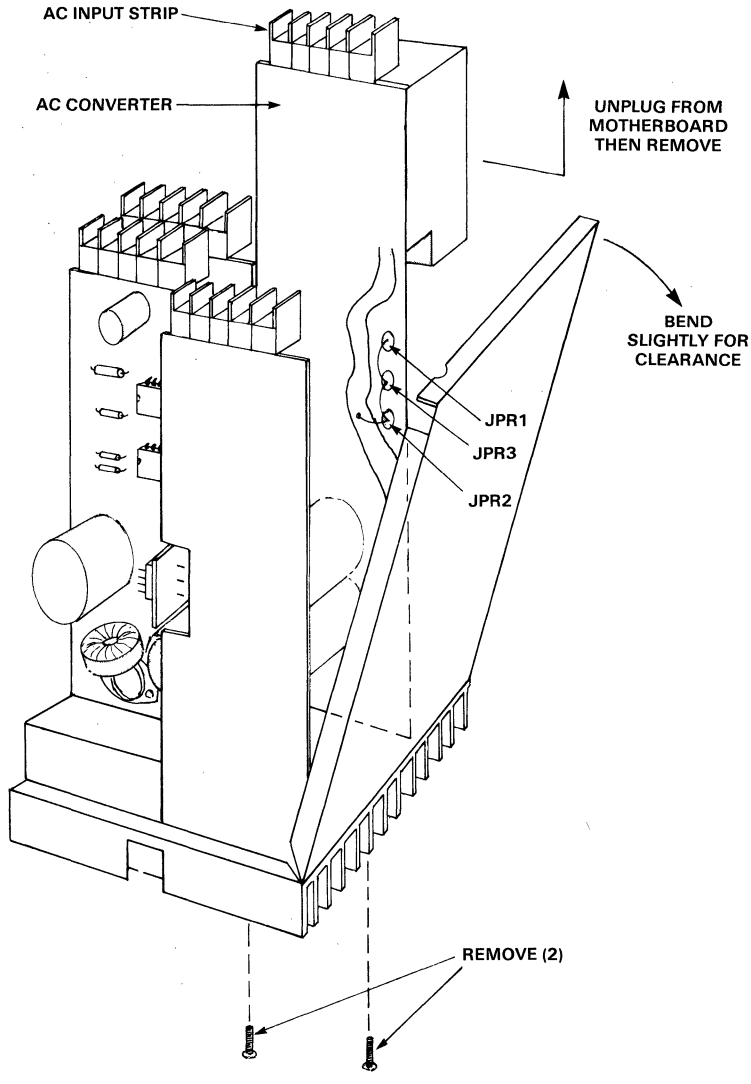
The MDX circuit boards are installed in the card cage with components facing to the left (user looking at card cage from front). The retaining bracket must be removed to install the cards. Quarter-turn thumb screws are used to install the retaining bracket. The boards must be installed with the card ejector up. The MD CC-16 is designed to prevent backwards installation of the STD BUS boards.

Priority Chain

The card cage is prioritized for interrupts from right to left. This means the highest priority interrupting device may be placed in the right-most slot. The lowest priority slot is far left. For a particular installation requiring both a complete interrupt priority daisy chain and an empty slot, wire-wrappable posts are provided on the motherboard for jumpering the priority chain.

150 WATT AC CONVERTER ASSEMBLY

Figure 5



ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
ENCL	Industrial Control System Enclosure - 300 Watt/60 Hz with Installation Manual	MK77980
ENCL1	Industrial Control System Enclosure - 150 Watt/60 Hz with Installation Manual	MK77987
ENCL2	Industrial Control System Enclosure - 300 Watt/50 Hz with Installation Manual	MK77981
ENCL3	Industrial Control System Enclosure - 150 Watt/50 Hz with Installation Manual	MK77988
Enclosure Technical Manual	Enclosure Technical Manual only	4420180

1983 COMPUTER PRODUCTS DATA BOOK

PRELIMINARY

SD/E-COMBO

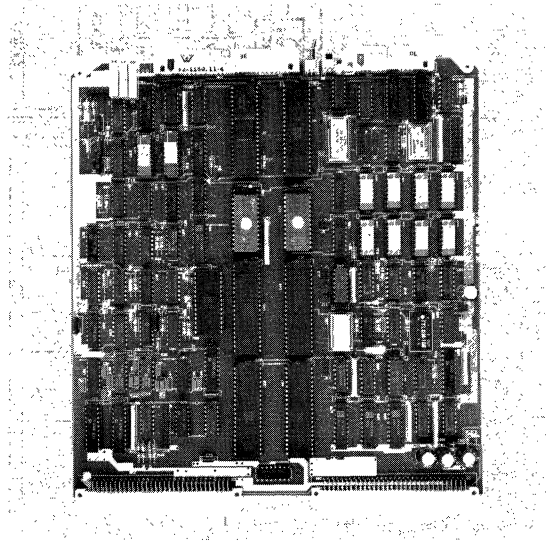
FEATURES

- One 4 MHz Z80 based CPU
- Two 28-pin sockets which may be strapped (using Mostek's BYTEWYDE concept) to accept either 2K x 8 or 8K x 8 ROMs or EPROMs
- Four cascadable Counter/Timer Channels
- Restart to 0000H or a 4K boundary from 0000H to F000H
- Two on-board RS-232-C subset D Serial I/O Channels with programmable Baud rate selection from 50 to 19.2K Baud. SIO channel A is used as a DCE (Data Communications Equipment) port and SIO channel B is used as a DTE (Data Terminal Equipment) port
- One software sense port and two programmable Baud rate generators
- Four eight bit Parallel I/O ports with handshake logic and selectable bit positions as Input, Output, or Bi-directional
- One Floppy Disk Controller for 1 to 4 floppy disk drives; Drives can be single (FM) or double (M2FM) density and can be either 5 or 8 inch media, single, or double sided
- Eight 65K x 1 bit MK4564 dynamic RAM memories
- One Direct Memory Access (DMA) chip which may be programmed to search and/or transfer blocks of data to and from any combination of memory or I/O device
- Eight memory maps in PROM which can handle any combination of ROMs/EPROMs and dynamic RAM, with jump-on-reset and shadow RAM capability
- Double Euro-card (extended) format

DESCRIPTION

The SD/E-COMBO board is a 4 MHz Z80-based expandable single board computer system with extensive on-board memory and Input/Output capabilities. The SD/E-Combo board can be used as a stand-alone application (such as a single board computer) or it can interface with other SD/E bus compatible boards.

SD/E-COMBO
Figure 1



CPU

The Z80 CPU (MK3880-4) features a 158 unit instruction set, single phase clock input, automatic dynamic memory refresh and an advanced set of addressing modes. This CPU generates all of the required addresses and control signals required for communication and control of data to and from memories and peripherals. It fetches and executes instructions and provides most of the timing signals required for proper operation of the board.

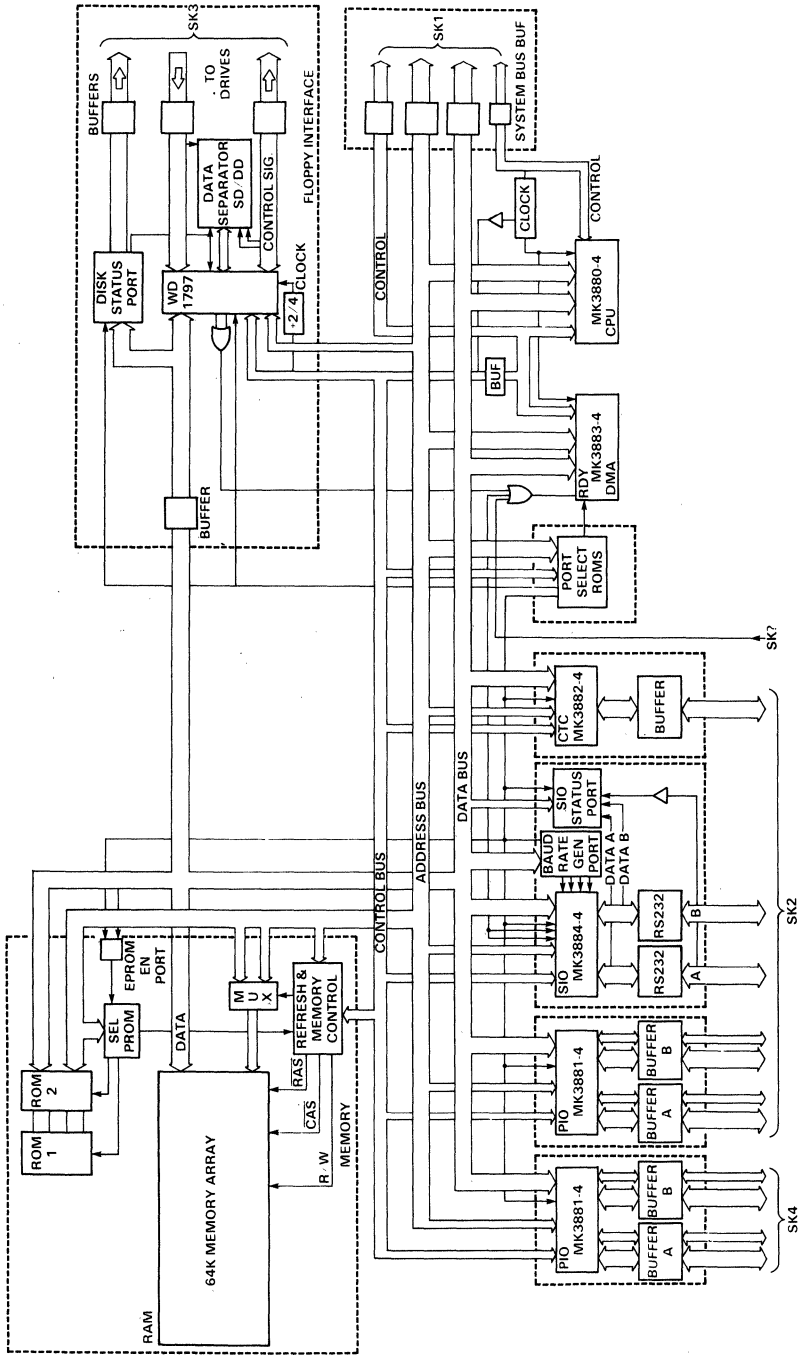
EPROM

The SD/E-COMBO board makes use of Mostek's BYTEWYDE memory concept by providing two 28-pin sockets that accept either 2K by 8 or 8K by 8 ROMs or EPROMs. When using 2K by 8 memories, each memory chip is inserted offset into the socket such that pins 1, 2, 27, and 28 are exposed and therefore not used. The memory control and addressing circuitry has a feature which allows the entire 65K bytes of memory to be addressed directly by the user. This is referred to as "Shadow Memory". In the SD/E-COMBO board, the term applies to the two EPROM sockets which may replace a portion of the main 65K of DRAM after a reset and can be enabled and disabled at will

V

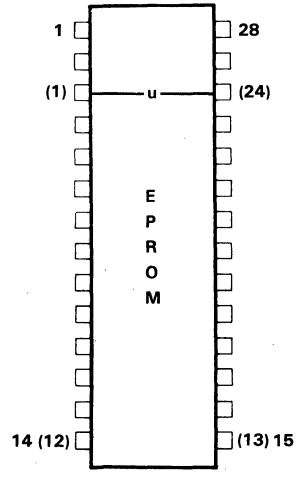
BLOCK DIAGRAM

Figure 2



24 PIN EPROM IN 28 PIN SOCKET

Figure 3



(XX) are 24 pin device

by any program. This ability of the COMBO to eliminate the EPROM/ROM socket from the addressing range of the Z80 is possible thru software control. Bit D4 of Port E2 controls this function. Any 2716 or 2764 type EPROM may be used as long as the access time from /OE is less than 335 nano-seconds.

DRAM

Eight 16 pin sockets provide DRAM (Dynamic Random Access Memory) storage capabilities for 65536 bytes of user memory using the MK4564 dynamic RAM. Each MK4564 is organized as 65536 by 1 bit. Refresh circuitry handles the DRAM refresh function automatically with no responsibility required of the system user. Refresh occurs during each operation code fetch and, therefore, is transparent to system throughput. The entire 65K bytes of memory is addressable directly using the sixteen position Address Bus. Normal shipping configuration after a reset is with the DRAM from 0000H through DFFFH, and from F000H to FFFFH, and EPROM from E000H through EFFFH.

PIO

The SD/E-COMBO boards Parallel Input/Output is designed around two MK3881-4 Z80-PIO controller chips. Each chip has two independent eight-bit Input/Output ports with two handshake (data transfer) control lines per port. This gives the user a total of 4 ports and 8 handshake lines. One PIO exits the board from SK1 and the other exits via SK4.

SIO

Serial Input/Output for the SD/E-COMBO board is designed around the MK3884-4 Z80-SIO chip. It provides two fully independent, serial data channels and is designed to be used in asynchronous applications. An independent software programmable Baud-rate clock generator is included to increase communication flexibility. Baud rates of the terminal may be measured via software by measuring the width of the start bit of the serial data stream. Channel A (SIOA) is shipped set up as Data Communication Equipment (DCE) and SIO channel B (SIOB) is shipped set up as Data Terminal Equipment (DTE). Both channels exit the board via edge connector SK2.

CTC

A four-channel Counter Timer Circuit consisting of an MK3882-4 Z80-CTC is included on-board for software controlled event counting and timer functions. The CTC Trigger inputs and zero-count outputs are buffered and brought out to connector SK2 for off-board control. Connecting the zero-count output of one CTC channel to the trigger input of another CTC channel makes it possible to cascade the four CTC channels for longer counting sequences.

DMA

The Z80 Direct Memory Access circuit, an MK3883-4 Z80-DMA, is a programmable single channel device which provides all address, control, and timing signals required to effect the transfer of blocks of data between two "ports" within a Z80-CPU-based system. These "ports" may be either system main memory, or any system peripheral input/output port. Additional benefits are gained with a feature of the DMA that can search a block of data for a particular byte (bit maskable) with or without a simultaneous data transfer. Primary use of the DMA function on the SD/E-COMBO is to provide floppy disk transfers.

FDC

The FD1797 is a MOS LSI device which performs the functions of a floppy disk formatter/controller in a single

2716/2764 EPROM DATA

Figure 4

Type	# of Pins	# of Bytes	Total # of Bits
2716	24	2K x 8	16,384
2764	28	8K x 8	65,536

chip implementation. The 1797 is IBM 3740 compatible in single density or Frequency Modulation (FM) mode of operation and IBM System 34 compatible in double density or Modified, Modified Frequency Modulation (M2FM) mode of operation. This chip contains all of the features necessary to read, write and format both single density and double density diskettes. This includes address mark detection, FM and M2FM data encoding and decoding logic, window extension and write precompensation. All control and data transfer lines exit the SD/E-COMBO board via edge connector SK3.

MECHANICAL SPECIFICATIONS

Card Dimensions

250 mm (9.84") high by 233.4 (9.19") mm wide
1.8 cm (.7") maximum profile thickness
1.6 mm (0.062") printed circuit board thickness

Mating Connectors

SK1 and SK2:	64 pin DIN type 41612 indirect Mating connector 96S-6033-05-22-1 (WW) 96S-6033-05-22-3 (Solder tail)
SK3:	Ansley 609-5000 W/O Strain Relief Ansley 609-5001 with Strain Relief Winchester 51-1150-01
SK4:	Ansley 609-2600 W/O Strain Relief Ansley 609-2601 with Strain Relief Winchester 51-0026-05

ELECTRICAL SPECIFICATIONS

Data Bus:	8 bits, bi-directional
Address Bus:	16 bits, bi-directional
Control Bus:	21 bits, both tri-state and bi-directional
System Bus:	SD/E compatible
Inputs:	One 74LS load maximum
Outputs:	I_{OH} = -3 mA min at 2.4 V I_{OL} = 24 mA min at 0.5 V
System Clock:	4.0 MHz ± .05%
I/O Addressing:	24 ports on-board expandable to 256 via SK1
Memory Addressing:	On-board CPU and DMA capable of addressing any memory address
Interrupts:	18 on-board, expandable to 128 thru SK1
Power Requirements:	+12 V @ 200 mA -12 V @ 25 mA +5 V @ 4.5 A
Operating Temperature:	0 °C to 50°C

CALIBRATION

Adjustment of the Floppy disk controller requires an oscilloscope. All connections are made at the test points located near R1, R2, and R3, the adjustment potentiometers.

Connect the oscilloscope ground to test point 6.

VCO VOLTAGE

Remove the floppy cable from SK3. Connect the oscilloscope to test point 3. Set the vertical range of the oscilloscope to 0.5 volts per division. Adjust the horizontal range control to a steady, bright line. Adjust R1 for 1.4 volts.

VCO FREQUENCY

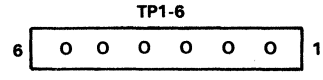
Do the VCO voltage adjustment first. Leave the floppy cable off SK3. Set the oscilloscope vertical range to 2 volts per division. Connect the oscilloscope to test point 2. Press the RESET button S2. Adjust R3 until the waveform has a rising-edge to rising-edge period of 2.0 micro-seconds.

WRITE PRE-COMPENSATION

Connect the oscilloscope to test point 4. Make the CPU write to the disk continuously in DOUBLE DENSITY. An easy way to do this is to format a disk. While the disk is being written, adjust R2 for a pulse width of 150 to 200 nanoseconds. The exact value is determined by your particular disk drive manufacturer. Check the manual of your particular disk drive for the recommended value.

TEST POINTS 1 THROUGH 6

Figure 5



CONNECTORS AND OPTION HEADERS

The SD/E-COMBO supports a wide variety of peripheral devices. The following tables are included to show the pinout of the various connectors used. The view is from the user looking INTO the I/O connector. Please note that each connector has a unique pinout specifically designed for its own application.

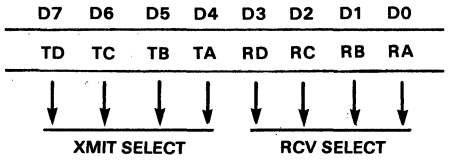
PORT ADDRESS CODES

Table 1

Port Address	Device Selected	Read Operation	Write Operation	Port Classification
D0	PIO1A	Data	Data	PIO
D1			Control	
D2	PIO1B	Data	Data	
D3			Control	
D4	PIO2A	Data	Data	
D5			Control	
D6	PIO2B	Data	Data	
D7			Control	
D8	CTC0	Dwn Counter	Control	CTC
D9	CTC1	Dwn Counter	Control	
DA	CTC2	Dwn Counter	Control	
DB	CTC3	Dwn Counter	Control	
DC	SIOA	Data	Data	SIO
DD		Status	Control	
DE	SIOB	Data	Data	
DF		Status	Control	
E0	DMA	Status	Control	DMA
E1	SIO Baud Rate		Selection	COMBO
E2	COMBO	E2 Status	E2 Control	
E3		E3 Status	E3 Control	
E4	FPY	Status	Control	FLOPPY
E5		Tk Reg	Track	
E6		Sect Reg	Sector	
E7		Data	Data	

PORT E1 COMMAND - SIO BAUD RATE

Figure 6

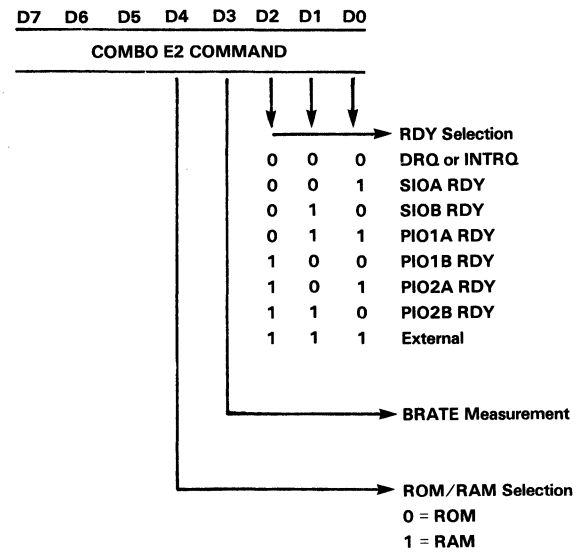


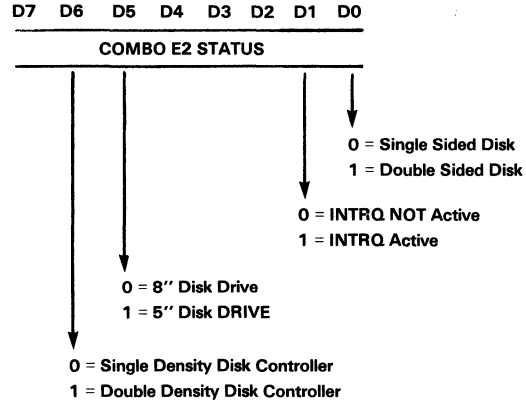
D	C	B	A	BAUD RATE	
0	0	0	0	50	
0	0	0	1	75	
0	0	1	0	110	
0	0	1	1	134.5	
0	1	0	0	150	
0	1	0	1	300	*
0	1	1	0	600	*
0	1	1	1	1200	*
1	0	0	0	1800	
1	0	0	1	2000	
1	0	1	0	2400	*
1	0	1	1	3600	
1	1	0	0	4800	*
1	1	0	1	7200	
1	1	1	0	9600	*
1	1	1	1	19200	*

* = Mostek firmware supports these Baud rates

PORT E2 COMMAND AND STATUS - FLP CONTROL

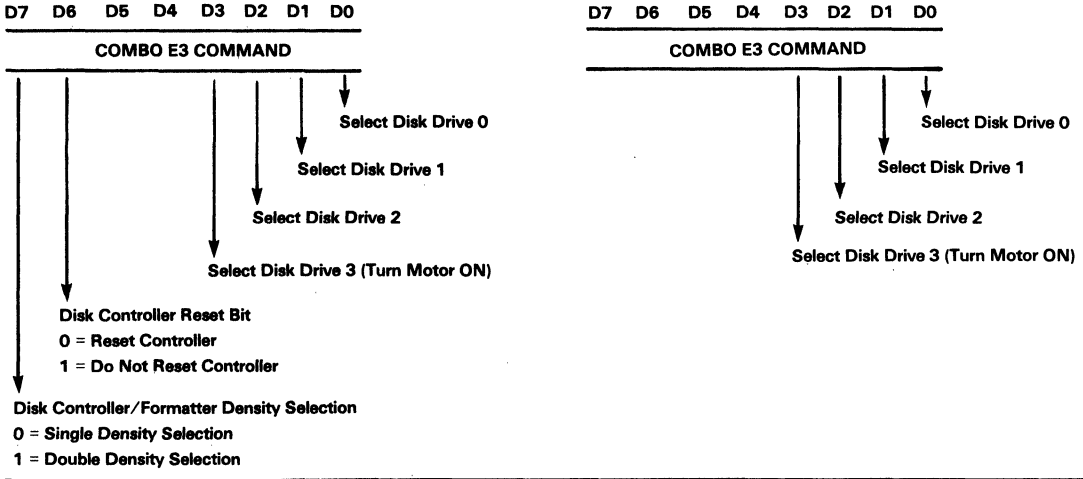
Figure 7





PORT E3 COMMAND AND STATUS - FLP CONTROL

Figure 8



SKI CONNECTOR - BUS EXPANSION

Figure 9

SK1

	c	a	
GND	1c	1a	GND
GND	2c	2a	GND
-12 V	3c	3a	-12 V
+5 V	4c	4a	+5 V
+5 V	5c	5a	+5 V
+12 V	6c	6a	+12 V
Reserved for -5 V	7c	7a	Reserved for -5 V
IEIB	8c	8a	IEOB
BAI	9c	9a	/BUSAKB
/MEMDISA	10c	10a	/DEBUGB
/MEMDISB	11c	11a	/RESETB
M1B	12c	12a	/RESTARTB
/NMIB	13c	13a	/MREQB
/BUSRQB	14c	14a	N/C
N/C	15c	15a	/INTB
/RDB	16c	16a	/WAITB
A0B	17c	17a	CLOCKB
A1B	18c	18a	/IORQB
A2B	19c	19a	/WRB
A3B	20c	20a	/RFSHB
A4B	21c	21a	N/C
A5B	22c	22a	/DINB
A6B	23c	23a	N/C
A7B	24c	24a	N/C
A8B	25c	25a	D0B
A9B	26c	26a	D1B
A10B	27c	27a	D2B
A11B	28c	28a	D3B
A12B	29c	29a	D4B
A13B	30c	30a	D5B
A14B	31c	31a	D6B
A15B	32c	32a	D7B

V

SK2 CONNECTOR - SIO/PIO EXPANSION

Figure 10

		c	a	
CTC Cable	ZC0B	1c	1a	C/T0B
	ZC1B	2c	2a	C/T1B
	ZC2B	3c	3a	C/T2B
	GND	4c	4a	C/T3B
SIOA Terminal Cable	(GND)AA	5c	5a	N/C
	(TXA)BA	6c	6a	N/C
	(RXA)BB	7c	7a	N/C
	(RTSA)CA	8c	8a	N/C
	(CTSA)CB	9c	9a	N/C
	(DSRA)CC	10c	10a	N/C
	(GND)AB	11c	11a	(DTRA)CD
	(RLSDA)CF	12c	12a	N/C
SIOB MODEM Cable	(GND)AA	13c	13a	N/C
	(TXB)BA	14c	14a	N/C
	(RXB)BB	15c	15a	N/C
	(RTSB)CA	16c	16a	N/C
	(CTSB)CB	17c	17a	N/C
	(DSRB)CC	18c	18a	N/C
	(GND)AB	19c	19a	(DTRB)CD
	(RLSDB)CF	20c	20a	N/C
PIO1 Line Printer Cable	GND	21c	21a	GND
	BTSB1	22c	22a	BRDY1
	P(D2)3	23c	23a	P(D2)4
	P(D2)2	24c	24a	P(D2)5
	P(D2)1	25c	25a	P(D2)6
	P(D2)0	26c	26a	P(D2)7
	ASTB1	27c	27a	ARDY1
	P(D2)3	28c	28a	P(D2)4
	P(D2)2	29c	29a	P(D2)5
	P(D2)1	30c	30a	P(D2)6
	P(D2)0	31c	31a	P(D2)7
	GND	32c	32a	GND

SK3 CONNECTOR - FLOPPY DISK

Figure 11

SK3

	1	2	
GND	3	4	/TG43
GND	5	6	N/C
GND	7	8	N/C
GND	9	10	/SSI
GND	11	12	N/C
GND	13	14	/SS (8")
GND	15	16	N/C
GND	17	18	/HLD
GND	19	20	/INDEX (8")
GND	21	22	/RDY (8")
GND	23	24	/INDEX (5")
GND	25	26	/DS1
GND	27	28	/DS2
GND	29	30	/DS3
GND	31	32	/DS4 (MOTOR ON 5")
GND	33	34	N/C
GND	35	36	/STEP
GND	37	38	/WD
GND	39	40	/WG
GND	41	42	/TRACK0
GND	43	44	/WTPT
GND	45	46	N/C
GND	47	48	/SS (5")
GND	49	50	N/C

SK4 CONNECTOR - PIO

Figure 12

SK4

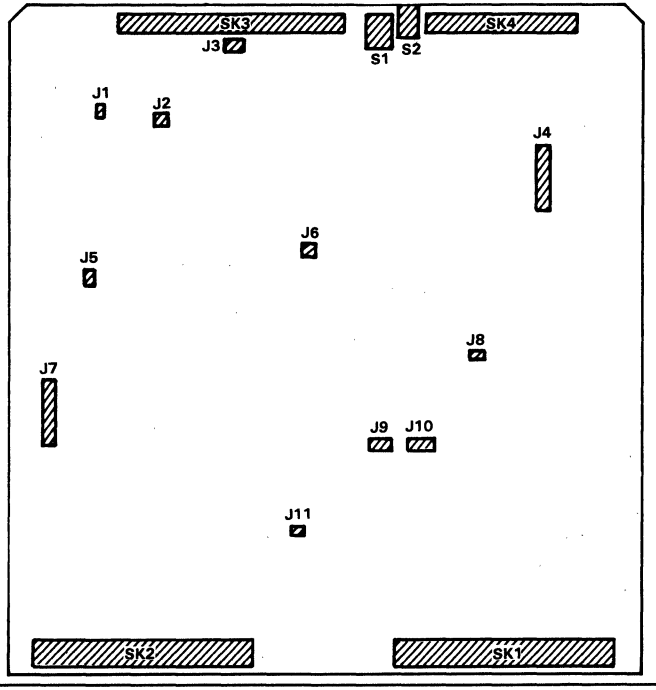
ARDY2	1	14	GND
ASTB2	2	15	GND
P(D4)7	3	16	P(D4)6
P(D4)5	4	17	P(D4)4
P(D4)3	5	18	P(D4)2
P(D4)1	6	19	P(D4)0
P(D6)0	7	20	P(D6)1
P(D6)2	8	21	P(D6)3
P(D6)4	9	22	P(D6)5
P(D6)6	10	23	P(D6)7
BSTB2	11	24	P(D6)GND
BRDY2	12	25	P(D6)GND
		26	N/C

STRAPPING OPTIONS

The following section describes the jumper straps on SD/E-COMBO in detail. Each functional section of the COMBO board has its own set of straps for changing functions. These areas are the disk interface, SIO interface, PIO interface, memory interface, and POWER-ON-RESET interface.

LOCATION OF JUMPERS AND SWITCHES

Figure 13

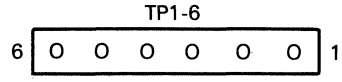


V

TP1-6 TEST POINTS

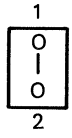
These six test points are for floppy disk controller calibration. Normally, no adjustment should ever be required. If calibration is necessary, see the section on calibration for instructions.

UNDER NO CIRCUMSTANCES SHOULD JUMPERS BE INSTALLED ON TEST POINTS 1 THROUGH 6.



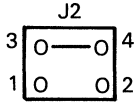
FLOPPY CONTROLLER JUMPERS

J1: AUTO PRECOMP - When open, double density write pre-compensation is always in effect. This strap has no effect in single density mode. When strapped, write data will be pre-compensated for all tracks greater than 43 automatically. Some 5¼ inch drives require write pre-compensation on all tracks. For use with these drives, jumper J1 should be removed. Normal shipping installation is J1 installed.



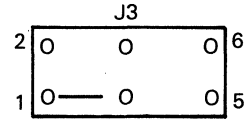
J1 Header

J2: VCO CLOCK - This clock is either a 4 MHz clock (pins 3 and 4 strapped) for use with 8 inch drives, or a 2 MHz clock (pins 1 and 2 strapped) for use with 5¼ inch drives. Normal shipping installation is J2 pins 3 to 4.



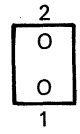
J2 Header

J3: FDC CLOCK and READY - This clock is either a 2 MHz clock (pins 1 and 3 strapped) for use with 8 inch drives, or a 1 MHz clock (pins 2 and 4 strapped) for use with 5¼ inch drives. Most 5¼ inch drives do not support a READY output signal. For use with these drives, J3 pins 5 and 6 should be strapped to supply a continuous RDY to the FDC chip. Normal shipping installation is J3 pins 1 to 3.



J3 Header

J5: 5¼ INCH DRIVE - This strap is used by Mostek software to determine whether 5¼ or 8 inch drives are used. Do not insert J5 unless you use 5¼ inch drives. This bit may be sensed by software as bit 5 of port E2. Normal shipping for J5 is NOT connected.



J5 Header

PIO JUMPERING

J4 AND J7: PIO OPTIONS - Low power Schottky TTL devices are provided to buffer the parallel I/O ports and handshake interface lines. The buffer devices are in sockets so the user may invert the data bits by substitution of devices. PIO1 is shipped with data bits D4-D7 for channel B inverted. The normal shipping configuration for PIO2 is non-inverting on all data bits. The A side of either PIO may be strapped for bi-directional, input, or output mode of operation. The B side of either PIO may be strapped for input or output only, as the B handshake lines are used when the A side is in bi-directional mode. Normal shipping installation is J4: pins 1-2, 3-4, 5-6, 7-8, 17-18, 19-20. Normal shipping for J7 is: 7-8, 15-16.

STRAPPING HEADER FOR J4 AND J7

Figure 14

	J4		J7	
PORT A BIDIRECTIONAL	1 — 2		1	2
PORT A BIDIRECTIONAL	3 — 4		3	4
PORT B D4-D7 OUTPUT	5 — 6		5	6
PORT B D0-D3 OUTPUT	7 — 8		7 —	8
PORT B RDY NON-INVERTED	9	10	9	10
PORT A RDY NON-INVERTED	11	12	11	12
PORT A D0-D7 INPUT	13	14	13	14
PORT A D0-D7 OUTPUT	15	16	15 —	16
PORT B STB NON-INVERTED	17 — 18		17	18
PORT A STB NON-INVERTED	19 — 20		19	20

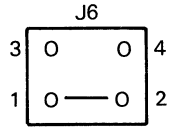
DRIVER SUBSTITUTION

Figure 15

	INVERTING	NON-INVERTING
Port A	74LS242	74LS243
Port B	74LS240	75LS244

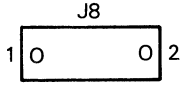
MEMORY JUMPERS

J6: EPROM SELECT - This strap selects either 2716 (2K x 8) or 2764 (8K x 8) type memories. If 2K by 8 EPROMs are to be used, strap pins 1 to 2 on this header. This is the chip signal VPP. If 8K by 8 EPROMs are to be used, strap pins 3 to 4. This allows signal A11 to the device. Normal shipping installation for J6 is 1 to 2.



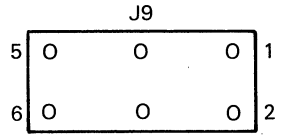
J6 Header

J8: PHANTOM EPROM - This jumper, when installed, allows a peripheral device or controller to disable the onboard EPROM. Normal shipping configuration is to NOT install J8.



J8 Header

J9: BANK SELECT - This header allows the user to store up to 8 different memory maps in ROM. This ROM is pre-programmed with a memory map. Normal shipping configuration is with all jumpers on J9 removed.



J9 Header

J9 STRAPPING

Figure 16

MAP	1-2	5-6	4-3
0	I	I	I
1	O	I	I
2	I	O	I
3	O	O	I
4	I	I	O
5	O	I	O
6	I	O	O
7	O	O	O

I = Installed jumper, O = open jumper

V

ROM MEMORY MAPS

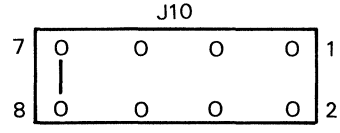
Figure 17

MAP	0	1	2	3	4	5	6	7	RAM ADDRESS
									F800-FFFF
		U43							F000-F7FF
		U43						U44	E800-EFFF
		U43						U43	E000-E7FF
									D800-DFFF
									D000-D7FF
									C800-CFFF
									C000-C7FF
									B800-BFFF
									B000-B7FF
									A800-AFFF
									A000-A7FF
									9800-9FFF
									9000-97FF
									8800-8FFF
									8000-87FF
									7800-7FFF
									7000-77FF
									6800-6FFF
									6000-67FF
									5800-5FFF
									5000-57FF
									4800-4FFF
									4000-47FF
						U44			3800-3FFF
						U44			3000-37FF
						U44			2800-2FFF
						U44			2000-27FF
					U43	U43			1800-1FFF
					U43	U43			1000-17FF
			U44		U43	U43			0800-0FFF
			U43	U43	U43	U43			0000-07FF

All unused locations in all maps are RAM

POWER-ON JUMP

J10: POWER-ON-RESET - This header allows the user to jump selectively to any 4K byte memory boundary upon a system reset. This feature may be defeated by switch S1 located between SK3 and SK4. If S1 is OFF, the Z80 CPU will reset to address 0000 if power is applied or switch S2 is pressed momentarily. If S1 is ON, the Z80 starting address will be determined by the jumper positions of J10.



J10 Header

POWER-ON-RESET JUMP ADDRESS

Figure 18

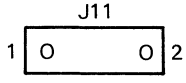
	Address	7-8	3-4	1-2	5-6
	0000	I	I	I	I
	1000	O	I	I	I
	2000	I	O	I	I
	3000	O	O	I	I
	4000	I	I	O	I
	5000	O	I	O	I
	6000	I	O	O	I
	7000	O	O	O	I
	8000	I	I	I	O
	9000	O	I	I	O
	A000	I	O	I	O
	B000	O	O	I	O
	C000	I	I	O	O
	D000	O	I	O	O
*	E000	I	O	O	O
	F000	O	O	O	O

*** = Normal shipping configuration**

I = Installed jumper, O = open jumper

SIO JUMPERING

J11: DTR ASSERTED - If the user's terminal attached to the SIO channel A does not support the Data Terminal Ready function, then J11 should be inserted. Normal shipping configuration is with J11 removed.



J11 Header

V

ORDERING INFORMATION

Designator	Description	Part Number
SD/E Combo	SD/E Combo single board computer system with Technical Manual	MK78202
SD/E Combo Technical Manual	SD/E Combo Technical Manual only	4420312

OEM-80E
MK78122, MK78124-3

FEATURES

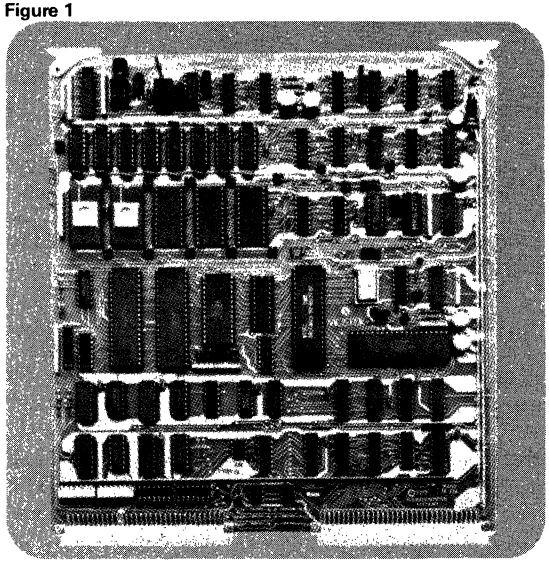
- Z80 CPU
- 20K x 8 EPROM
- Accepts 2708, 2716, or 2532 EPROM's
- 256 x 8 static scratchpad RAM on-board
- 16K (4K) x 8 dynamic RAM
- Z80 CTC - four counter/timer channels
- Restart to 0000H or E000H (switch option)
- On-board serial I/O port
- Software-programmable baud rate
- Current loop or RS-232-C (V.24) interface
- Four 8-bit parallel ports with handshake
- Ports buffered with TTL, socket-programmed
- Port direction in 4-bit blocks
- Programmable polarity on strobe lines
- Halt lamp
- Power-on-reset logic
- SDE BUS compatible

DESCRIPTION

The OEM-80E is a Z80 CPU-based computer board. The card has sufficient on-board I/O and memory to be used in a stand-alone mode in many applications, yet it is fully expandable to support more memory and I/O in applications requiring it. The five EPROM sockets on-board can be strapped to use a number of standard 24-pin ROM/EPROM products including PROMs and ROMs with capacities of up to 4K bytes each. The eight RAM sockets can be strapped for 4K or 16K RAMs, giving a maximum

OEM-80E BOARD PHOTO

Figure 1



16K bytes on-board. The Z80 built-in refresh logic reduces the area taken by the dynamic RAMs to that required by other manufacturers' 1K byte static RAM, the cost per bit being significantly reduced. Also on-board are two memory-decoding bipolar PROMs. These allow a wide range of RAM/PROM/ROM combinations to be selected by the user; if the exact combination required is not already supported, new PROMs can be easily programmed.

The user switch-selectable restart address allows the DDT-80 debug program to reside in the system without conflict with the user's own PROM-based software. If a problem develops, the user can switch from address 0 reset to address E000 (where DDT-80 resides) and use the powerful commands of the 2K byte DDT-80 to localize the problem.

The "E" format and DIN connectors allow quick integration into the user's system hardware. Putting all connectors on one card edge is a unique feature in microcomputer modules, although it is standard design practice for many large system builders. The simplified maintenance and clean cabling made possible by this technique should be appreciated by all experienced users.

MEMORY ADDRESSING AND CAPACITY

The recommended memory map is shown below:

0000-3FFF PROM (1 TO 16K)
4000-7FFF RAM (4 TO 16K)
8000-DFFF EXTERNAL MEMORY
E000-E7FF DDT-80 (2K)
E800-FEFF EXTERNAL MEMORY
FF00-FFFF SCRATCHPAD RAM (256 bytes, needed only if DDT-80 is used)

Memory cycle time required for the PROMs is 450 ns.

SERIAL I/O PORTS

A UART with 20mA current loop and RS-232-C (V.24) buffers/drivers provides a serial communication channel for interfacing to TTY or CRT terminals or serial printers. The baud rate is software-programmable over the range of 110 to 9600 baud.

PARALLEL I/O PORTS

The four parallel ports are designed to allow maximum flexibility in matching the MOS I/O ports to the real world of long lines or high voltages. Two ports support bidirectional TTL I/O with hystersis inputs. The ports can also be programmed for input or output only. The other ports are supplied with sockets which support a number of standard TTL devices for buffering. A list of pin-compatible devices is given below:

TYPE	USE
7400	16mA TTL inverting output
7402	TTL inverting input
7408	16mA TTL non-inverting output
7426	16mA high-voltage inverting open-collector output
7437	48mA TTL inverting output
7438	48mA TTL inverting open-collector output

COUNTER/TIMER CHANNELS

Four counter/timer channels are provided on the card in a Z80-CTC chip. One channel is used as the baud rate generator of the serial I/O port. The other three channels are available to the user. The channels may be programmed as delay generators, event counters or simply discrete interrupt inputs with a programmable edge trigger. The device can generate four interrupts.

INTERRUPTS

The OEM-80E has nine on-board interrupts. They are:

One Z80 CPU NMI (non-maskable interrupt)
Four Z80 PIO(2) Mod 2 Interrupts
Four Z80 CTC Mod 2 Interrupts

More interrupt devices (up to 128 total) can be added to the SDE bus.

BUS INTERFACE

All Z80 signals are buffered before leaving the OEM-80E. The buffering protects the MOS components from static charge during handling and from bus transients which could otherwise destroy these devices. The bus supports DMA transfers and the daisy-chained, multi-level interrupt structure of the Z80. The bus uses hystersis-input receivers and current-limited bus drivers to improve the noise margin of the bus. Switching the bus drivers on only when data is needed and stable further reduces the noise on the bus.

POWER REQUIREMENTS

+5V ±5% at 1.5 A
+12V ±5% at 0.175 A
-12V ±5% at 0.1 A

OPERATING TEMPERATURE RANGE

0°C to 50°C

BOARD SIZE

233.4mm (9.19 in) X 250 mm (9.84 in.)

CONNECTORS

Two 64-pin DIN 41612 (a-c) indirect, male

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
OEM-80E/4	OEM-80E/4 with 4K bytes of RAM (MK4027), 5 sockets for EPROM or ROM, 2 PIOs with sockets for TTL buffering logic, CTC, UART, socket for 256-byte scratch-pad RAM and sockets for memory mapping PROMs.	MK78122
OEM-80E/16	Same as OEM-80E/4 except with 16K bytes of RAM (MK4116)	MK78124
	OEM-80E Operations Manual only	MK78548

DCC-80E
MK78192

FEATURES

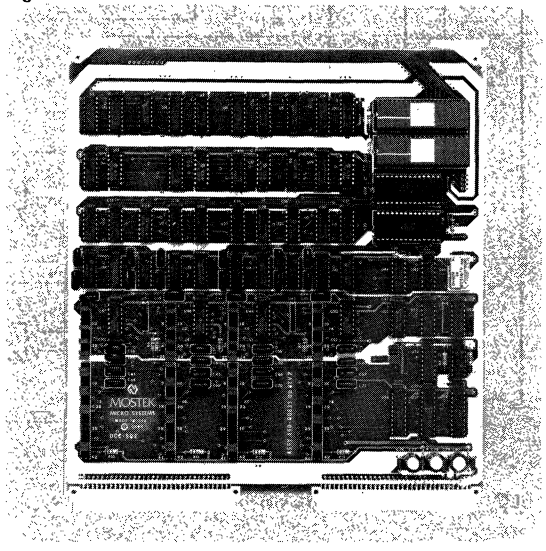
- 4 independent full-duplex channels
- Independent programmable Baud-rate clocks
- Data rates - 75 to 38.4K bits per second
- Receiver data registers quadruply-buffered
- Transmitter data registers double-buffered
- Asynchronous operation
- Binary synchronous operation
- HDLC or IBM SDLC operation
- Both CRC-16 and CRC-CCITT (-0 and-1) hardware implemented
- Modem control
- Operates as DTE or DCE
- Serial input and output as RS-232-C
- Address programmable
- SDE BUS compatible
- Each individual channel with NRZI encoder/decoder
- Scrambler cable included

DESCRIPTION

The Multichannel Serial Input/Output Module, DCC-80E, is designed to be a multiprotocol asynchronous or synchronous I/O module for the SDE BUS. The module is designed around the Mostek MK3887™ (Z80-SIO) which provides two full-duplex serial data channels. Each channel has an independent programmable Baud rate clock generator to increase module flexibility. Each channel is capable of handling asynchronous, synchronous, and synchronous bit-oriented protocols such as IBM BiSync, SDLC, and HDLC. It can generate CRC codes in any synchronous mode and can be programmed by the CPU for any traditional asynchronous format. The serial input and output data is fully buffered and is provided at the connector as RS-232-C levels. A modem control section is also provided for handshaking and status. The module can be jumper-configured as a data terminal or as a modem in order to facilitate a variety of interface configurations.

DCC-80E BOARD

Figure 1

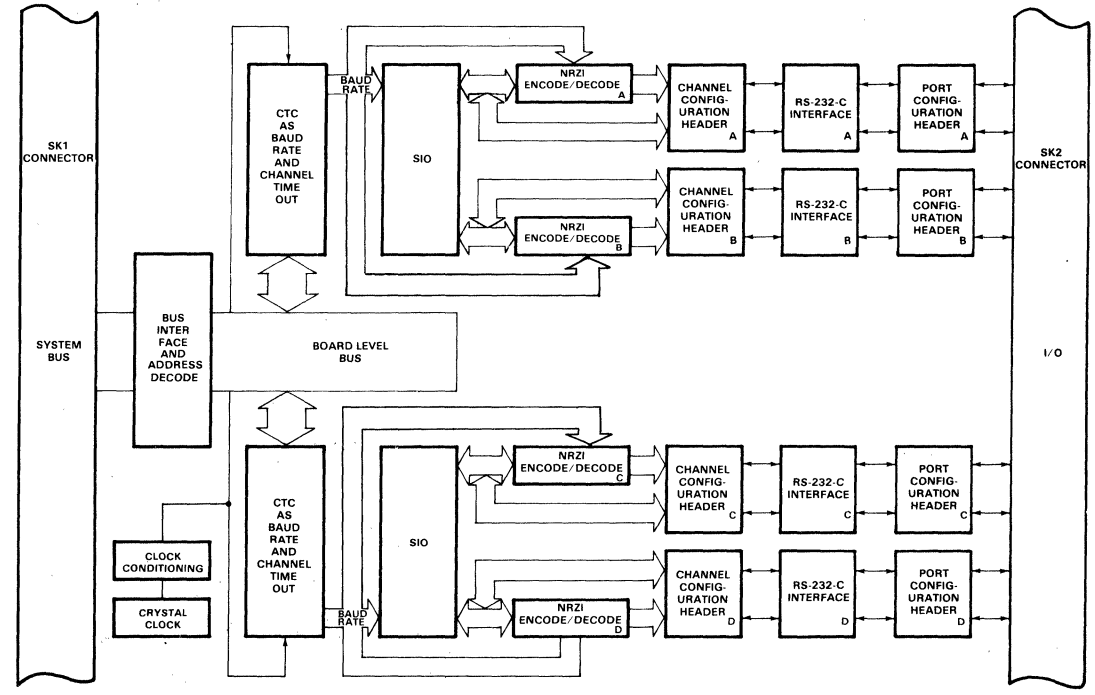


V

™SDE SERIES is a trademark of Mostek Corporation

DCC-80E BLOCK DIAGRAM

Figure 2



BLOCK DIAGRAM DISCUSSION

Figure 2 is a block diagram of the DCC-80E module which consists of eight main elements: The bus interface and address decode circuitry, the crystal clock and its associated conditioning circuitry, the counter timer circuitry (CTC), the serial input/output circuitry (SIO), the non-return-zero-inverted (NRZI) encode/decode circuitry, the channel configuration headers, the RS 232-C interface circuitry, and the port configuration headers.

The bus interface consists of both uni/bi-directional buffers which reduces the DCC-80E load on the bus to one LS-TTL load. The address decoders, in addition to being buffered, are jumper selectable to any one of the available 16 port boundaries in the Z80 I/O map. The DCC-80E contains command registers that are programmed to select the desired operational mode. The addressing scheme is as follows: (The X indicates the binary code necessary to represent which one of the 16 port addresses is selected.)

PORT ADDRESS	PORT FUNCTION
X0H ...	CTC as baud-rate generator for Channel A
X1H ...	CTC as programmable timer
X2H ...	SIO Data Input/Output of Channel A
X3H ...	SIO Status/Control for Channel A
X4H ...	CTC as baud-rate generator for Channel B
X5H ...	CTC as programmable timer
X6H ...	SIO Data Input/Output of Channel B
X7H ...	SIO Status/Control for Channel B
X8H ...	CTC as baud-rate generator for Channel C
X9H ...	CTC as programmable timer
XAH ...	SIO Data Input/Output of Channel C
XBH ...	SIO Status/Control for Channel C
XCH ...	CTC as baud-rate generator for Channel D
XDH ...	CTC as programmable timer
XEH ...	SIO Data Input/Output of Channel D
XFH ...	SIO Status/Control for Channel D

The crystal and associated conditioning circuitry provides an on-board stable clock capability for the counter timer circuits.

The CTC's are used as programmable baud-rate generators (Ports X0H, X8H, and XCH) as well as programmable time-out counters (Ports X1H, X5H, X9H, and XCH). Each DCC-80E channel has an individual programmable baud-rate generator. The x1 multiplier on the Z80-SIO must be used in the synchronous mode. The x16, x32, or x64 Z80-SIO clock rate may be specified for the asynchronous mode. Table 1 indicates the standard baud rates available for both operation modes.

STANDARD BAUD RATE

Table 1

Standard Baud Rates	
Asynchronous	**Synchronous**
75	
110	
150	
300	
600	600
1200	1200
2400	2400
4800	4800
9600	9600
19,200	19,200
38,400	38,400

The Mostek MK3887 (Z80-SIO) is the central element of the DCC-80E module. This device is a multifunction component designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic role is that of a parallel-to-serial, serial-to-parallel converter/controller, but within that role it is configured by software programming so that its function can be optimized for a given serial data communications application. It has the ability to compute circular redundancy checks making it compatible with such protocols as SDLC. This device provides two independent, full-duplex channels: A and B. Each channel features the following:

ASYNCHRONOUS OPERATION

- 5, 6, 7, or 8 bits/character
- 1, 1 1/2, or 2 stop bits
- Even, odd, or no parity
- x1, x16, x32, and x64 clock modes
- Break generation and detection
- Parity, Overrun, and Framing Error Detection

BINARY SYNCHRONOUS OPERATION

- One or two sync characters in separate registers
- Automatic sync character insertion
- CRC generation and checking

HDLC OR IBM SDLC OPERATION

- Automatic Zero Insertion and Detection
- Automatic Flag Insertion
- Address Field Recognition
- I-Field Residue Handling
- Overrun protection for valid receive messages
- CRC generation and checking

The MK3887 also provides modem control inputs and outputs as well as daisy-chain priority interrupt logic. Eight different interrupt vectors can be generated by the SIO in response to various conditions affecting the data communications channel transmission and reception. Ports X6H, XAH, and XEH are data channels of Z80-SIO devices. The CPU loads them with data to be sent and conversely reads back data assembled in the receiver buffer. The Write Registers (0-7) of the SIO are preset by a write operation on ports X3H, X7H, XBH, and XFH to control proper operation.

The NRZI circuitry interfaces the SIO to the channel headers and allows the user to connect the NRZI data to the RS 232-C interface. The RS 232-C line drivers and receivers not only provide the correct electrical signal levels, slew rates, and impedances, but also allow the NRZI encoded data to be configured as Data Terminal Equipment (DTE) or Data Communications Equipment (DCE). The port configuration headers are then used to select the orientation of the data communication interface. This allows the user to connect a DCC-80E module to a non-encoded modem.

Input and output to the board is provided via the SK2 connector. The configuration and pin out headers of each channel are identical, and are diverted to the correct DB25 connector in the Matrix-80/SDS via a ribbon cable and scrambler board which is sold as a separate product (see ordering information). The scrambler card installation and pin outs are shown in Figures 3 and 5.

OPERATIONAL FEATURES

The channel interface connects DCC-80E to data terminal/communications equipment. It consists of four basic parts:

1. Drivers and Receivers for RS-232-C
2. NRZI encoder
3. NRZI clock-recovery circuit
4. NRZI data-recovery circuit

Operation of DCC-80E can be tailored to any functional environment by means of prewiring two jumper fields, per channel, to any desired configuration.

WORD SIZE

Data: 5,6,7,8 bits
I/O addressing: 8-bits

I/O ADDRESSING

On-board fully programmable for 1 of 16 beginning port addresses. Board may be addressed to any one of sixteen on-board port addresses.

I/O CAPACITY

Serial: Four full-duplex serial ports, either synchronous or asynchronous. Special control registers and circuitry to permit implementation of SDLC, BiSync, Monosync, HDLC, and other formats can be programmed. All synchronous formats can be NRZI encoded.

INTERRUPTS

Generates vectored interrupts to 32 different locations corresponding to conditions within four SIO channels and four CTC channels. Interrupt vector location programmable. Daisy-chained priority interrupt maintained.

SYSTEM CLOCK

DCC-80E 2.5MHz ± .05%

OPERATING TEMPERATURE

0°C to 50°C

POWER SUPPLY REQUIREMENTS

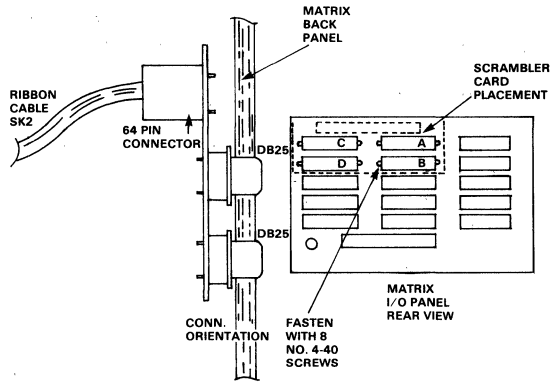
+12 volts ± 5% at 120 mA max.
-12 volts ± 5% at 80 mA max.
+5 volts ± 5% at 1.2 A max.

CARD DIMENSIONS

233.4 mm (9.19 in.) x 250 mm (9.84 in.) x 1.6 mm (0.062 in.)
See Figure 4

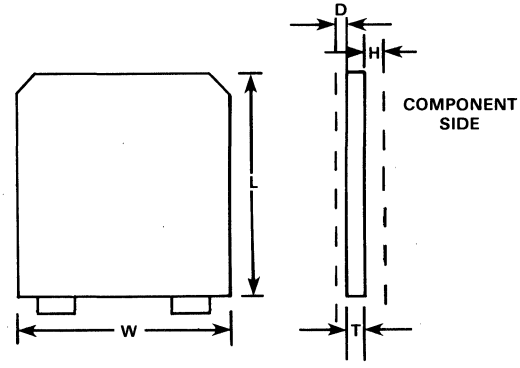
SCRAMBLER CARD ORIENTATION

Figure 3



CARD DIMENSIONS

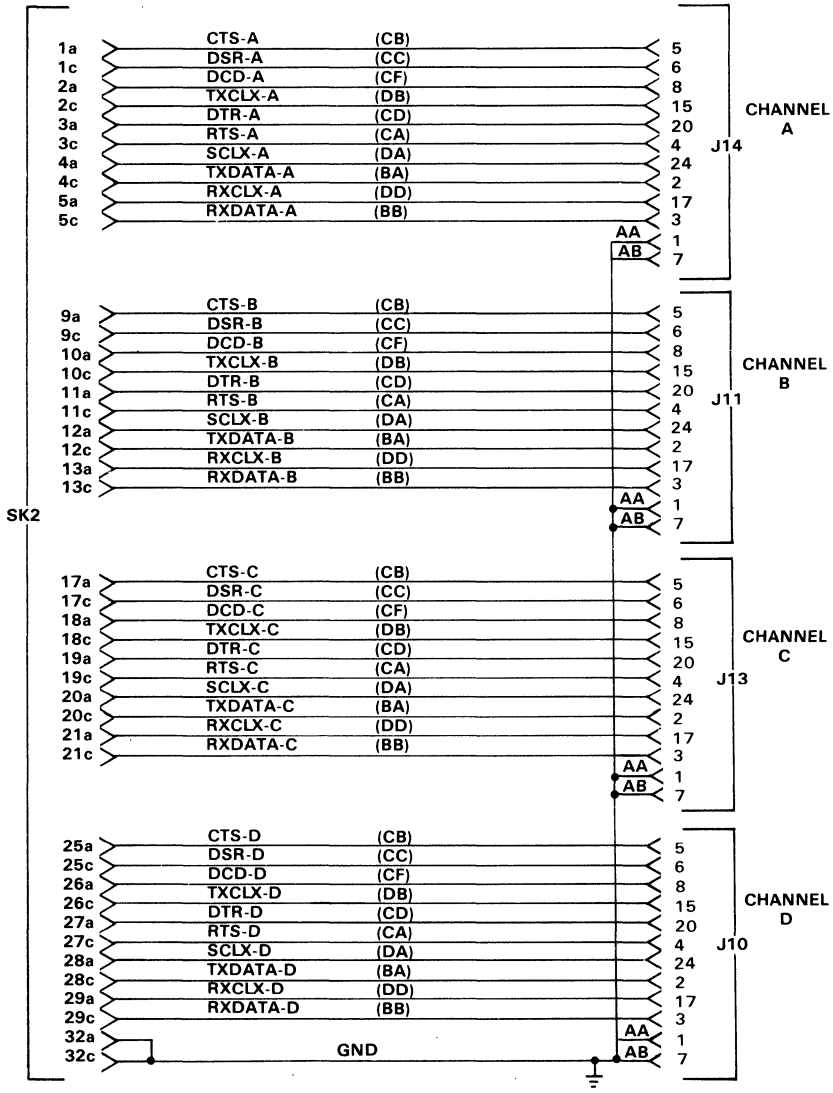
Figure 4



	DIMENSION	TYPICAL	MAXIMUM
L	Board Length	250.0 mm (9.84 in.)	250.2 mm (9.850 in.)
W	Board Width	233.4 mm (9.19 in.)	233.7 mm (9.200 in.)
H	Component Height	—	13.0 mm (0.510 in.)
T	Board Thickness	1.6 mm (0.062 in.)	1.7 mm (0.065 in.)
D	Lead Length	2.3 mm (0.090 in.)	2.5 mm (0.100 in.)

DCC-80E SCRAMBLER DIAGRAM

Figure 5



V

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NUMBER
DCC-80E	Four-channel data communication controller module with operations manual and scrambler cable	MK78192
Scrambler	Converts SK2 Pin out to four DB-25 connectors mounted on I/O panel of SDE-RMC6 or SDE-RMC6-50 or MATRIX-80/SDS	MK78200
DCC-80E-OM	DCC-80E Operations Manual Only	MK79812

FLP-80E
MK78146

FEATURES

- ☐ Soft-sector format compatible with IBM 3740 data entry system format
- ☐ Capable of controlling up to four flexible disk drives per subsystem
- ☐ Full disk initialization (Formatting)
- ☐ Full-sector (128 bytes) FIFO buffering for data
- ☐ Double buffering for control and status
- ☐ Automatic track-seek with verification
- ☐ Completely interruptable for real-time systems
- ☐ SDE BUS compatible

APPLICATIONS

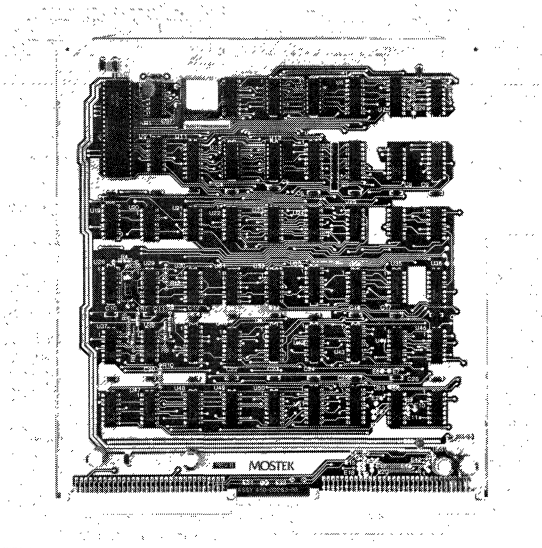
- ☐ Flexible disk-drive interface for use with Mostek's Software Development Board (OEM-80E) in a disk-based Z80 Development System (MATRIX).
- ☐ Single or multiple flexible disk-drive controller/formatter for disk-based OEM systems using the OEM-80E Single Board Computer.

DESCRIPTION

The FLP-80E is an add-on flexible disk controller module used to interface up to four flexible disk drives to the Mostek Software Development Board (OEM-80E).

FLP-80E BOARD PHOTO

Figure 1

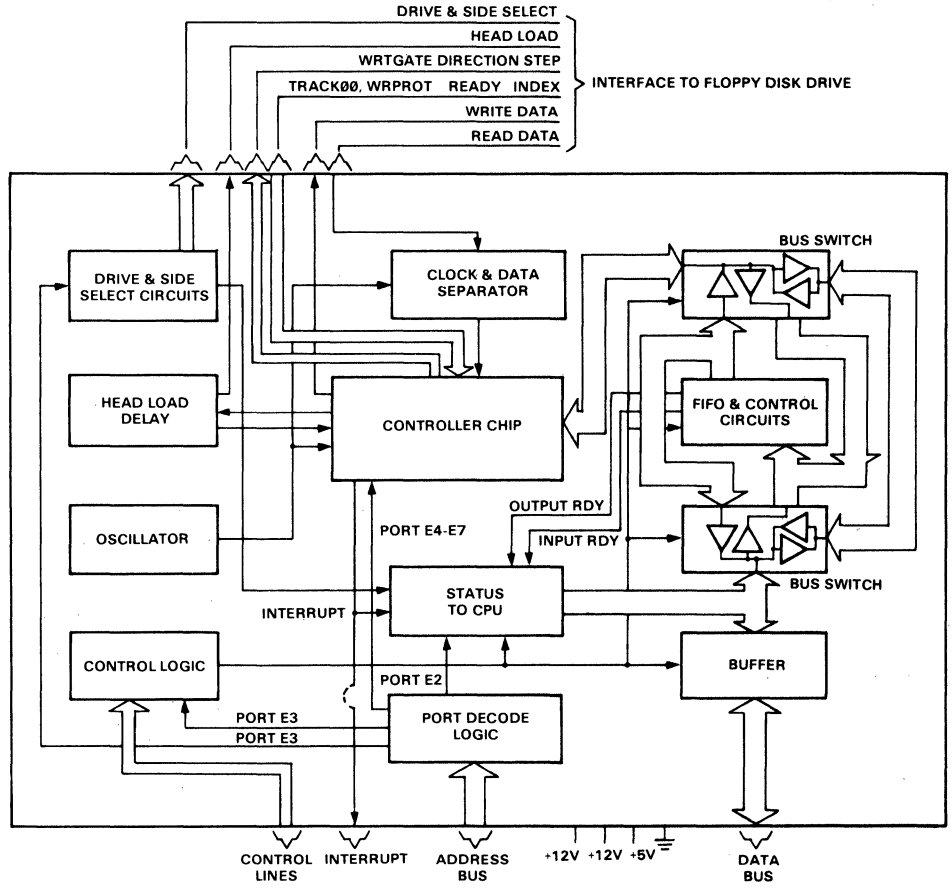


The FLP-80E provides the necessary electronics to accomplish track selection, head loading, data transfer, error detection, flexible drive interface, status reporting and format generation/recognition. The FLP-80E is designed to operate with either Shugart SA-800 Single-Sided or SA-850 Double-Sided Flexible Disk Drives. In addition to functioning as an add-on card to the OEM-80E system, the FLP-80E may be utilized directly in OEM applications to control/format up to four flexible disk drives of either single- or dual-sided type in Z80 systems.

V

FLP-80E BLOCK DIAGRAM

Figure 2



AVAILABLE SOFTWARE

Software for the FLP-80E disk controller is the Mostek Disk Operating System (FLP-80DOS). A user can easily design his own OEM software package around 20 powerful disk operating system commands permitting complex record insertion, deletion, and position manipulation. Other software includes application packages such as an advanced monitor and debugger, disk-based Text Editor, Z80 Assembler, Relocating Linking Loader, Peripheral Interchange Program, and a channelized I/O system for each peripheral interface. These programs provide state-of-the-art software for developing Z80 programs as well as establishing a firm basis for OEM products. Further information is provided in the FLP-80DOS Data Sheet, MK78556.

OPERATING TEMPERATURE RANGE

-0°C to 50°C

POWER SUPPLY REQUIREMENTS (Typical)

+12V ± 5% at 0.006A
+5V ± 5% at 1.1A
-12V ± 5% at 0.03A

INTERFACE LEVELS

TTL Compatible

BOARD SIZE

250mm x 233.4mm x 18mm

BOTTOM CONNECTOR

Dual 64-pin Eurocard Connector, DIN 41612 form D; A and C pinned.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
FLP-80E	FLP-80E Disk Controller Board with Operations Manual, FLP-80DOS bootstrap PROMs and diskette with FLP-80DOS Operations Manual.	MK78112
FLP-80DOS	FLP-80DOS bootstrap PROMs and diskette	MK78142
FLP-80E	FLP-80E Disk Controller Board with Operations Manual. (No Software)	MK78146
	FLP-80E Operations Manual. Detailed description of use and operation of FLP-80E.	MK78561
FLP-80DOS Data Sheet	Disk Operating System data sheet.	MK78556
	FLP-80DOS Operations Manual. Detailed description of the use and operation of FLP-80DOS.	MK78557

RAM-80E
MK78109, MK78110, MK78212

FEATURES

- ☐ Memory Capacity
  - RAM-80AE — 16,384 (16K) bytes using MK4027 RAM
  - RAM-80BE — 16,384 (16K) bytes expandable to 65,536 (65K) bytes using MK4116 RAM
  - RAM-80BE under page-mode operation — up to one megabyte of memory
- ☐ I/O Capacity (RAM-80BE only)
  Four 8-bit ports with handshake lines

DESCRIPTION

The RAM-80E is designed to provide RAM expansion capability for the Z80-based OEM-80E microcomputer. For user flexibility, it is offered in two basic configurations designated RAM-80AE and RAM-80BE.

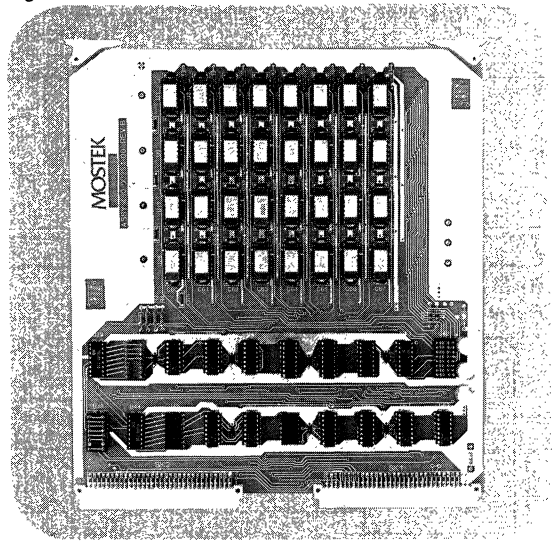
The RAM-80AE is the basic 16K-byte RAM board for users requiring the most economical means for adding RAM to an OEM-80E microcomputer. It is designed using the high-performance MK4027-4, 4096 x 1-bit dynamic RAM, and includes address strapping options for positioning the decoded memory space to start on any 4K incremental address boundary.

The RAM-80BE is a combination memory and I/O expansion board. The memory may be configured to have a memory capacity of 16K, 32K, 48K, or 65K bytes of RAM. This on-board memory expandability is made possible by population options of either 8, 16, 24, or 32 MK4116-4 (16,384 x 1 MOS dynamic RAM) memories. The RAM-80BE provides strapping options for positioning the decoded memory space to start on any 16K address boundary. In addition to the add-on memory, the RAM-80BE provides four 8-bit I/O ports from the two on-board MK3881 Z80 PIO circuits. Each I/O port is fully TTL-buffered and has two handshake lines per I/O port. The RAM-80BE also includes logic for "Page-Mode Operation" which permits up to 1 megabyte of memory (sixteen 65K x 8 RAM-80BEs) to be used in a single OEM-80E system.

A complete set of documentation for each RAM-80E board is available to ensure easy utilization.

RAM-80E BOARD PHOTO

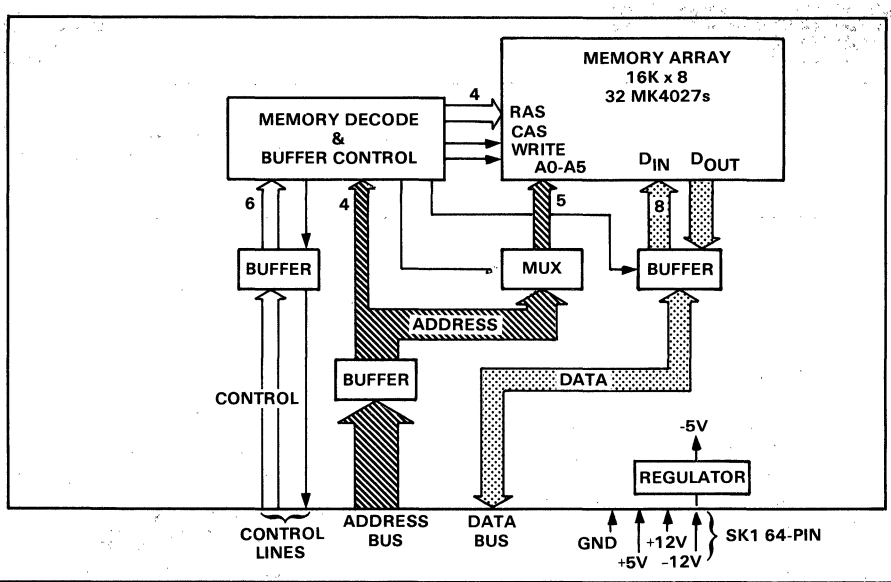
Figure 1



V

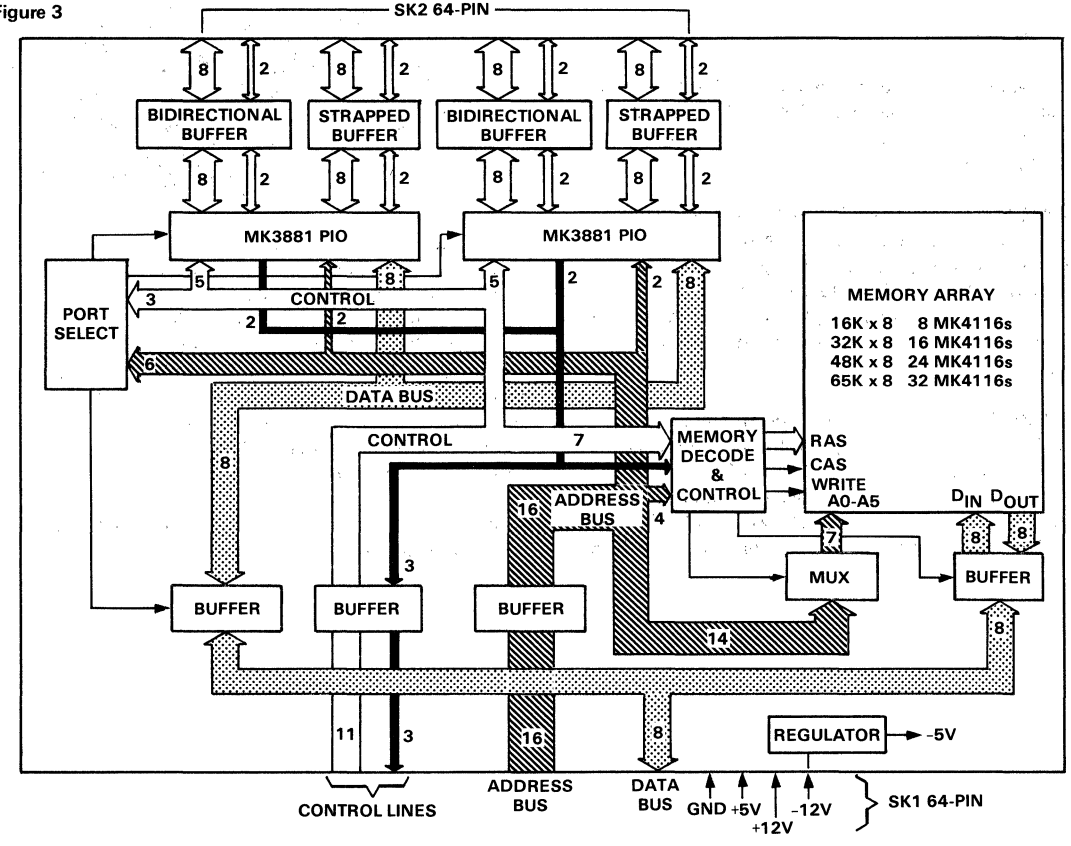
RAM-80AE BLOCK DIAGRAM

Figure 2



RAM-80BE BLOCK DIAGRAM

Figure 3



MEMORY ACCESS TIME

345ns (maximum)

MEMORY CYCLE TIME

450ns (minimum)

OPERATING TEMPERATURE

0°C to 50°C

POWER SUPPLY REQUIREMENTS

Voltage	RAM-80AE	RAM-80BE
+12V±5%	200mA typ. 575mA max.	200mA typ. 575mA max.
-12V±5%	25mA typ. 30mA max.	25mA typ. 30mA max.
+5V±5%	370mA typ. 550mA max.	1.1A typ. 1.5A max.

BOARD SIZE

250 mm x 233.4 mm x 18 mm

CONNECTOR

Dual 64-pin Eurocard Connector

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
RAM-80AE	16,384-byte RAM board with 32-MK4027s	MK78109
RAM-80BE	Expandable 16,384-byte RAM board with 8-MK4116s, sockets for additional MK4116s, 2—MK3881 Z80 PIOs, plus page-mode capability.	MK78110
	RAM-80BE Operations Manual. Complete description of the electrical specifications, timing, and circuit operation of the RAM-80BE. Also includes a detailed schematic diagram, assembly drawing and parts list.	MK78555
	RAM-80AE Operations Manual. Complete description of the electrical specifications, timing, and circuit operation of the RAM-80AE. Also includes a detailed schematic diagram, assembly drawing, and parts list.	MK78574

V

VDI-80E
MK78198, MK78033, MK78199, MK78035

FEATURES

- ☐ 24-line x 80-character display
- ☐ 5 x 8 dot matrix
- ☐ Upper and lower case display
- ☐ 96-character ASCII plus 32 special characters
- ☐ Programmable TABs
- ☐ Programmable Inverse Video
- ☐ Bidirectional Scrolling
- ☐ 48-character FIFO
- ☐ Auto repeat on keyboard interface
- ☐ Direct and relative cursor addressing and cursor address readback
- ☐ Direct speaker drive for bell tone
- ☐ Ability to read character, line, or screen information stored in screen RAM
- ☐ Two versions
  Serial: 110-9600 BAUD
  Parallel: 3200 Character/Sec
- ☐ 50/60 Hz versions

DESCRIPTION

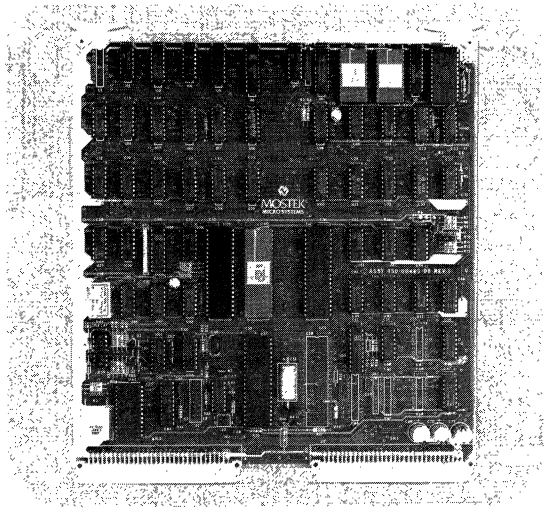
The Video Display Interface (VDI) board is a microprocessor-based video terminal controller system on a Double Eurocard format printed circuit board. The VDI serves as the interface between an ASCII encoded keyboard and an EIA standard video monitor to a microcomputer development system.

The display format is 24 lines of 80 characters. Each character is formed by a 5 x 8 dot matrix in a 6 x 9 cell (60 Hz version or a 6 x 11 cell (50 Hz version). See Figure 4.

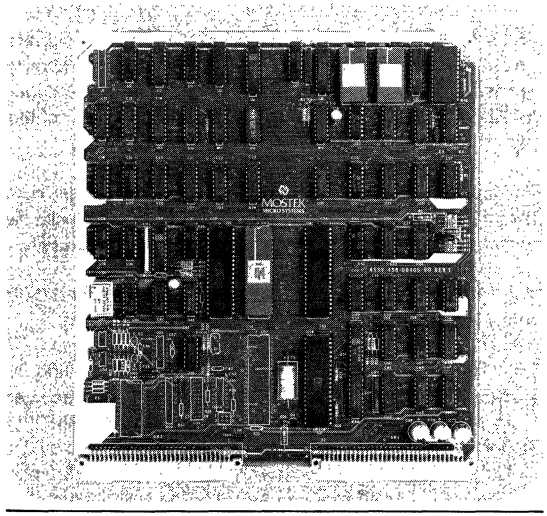
Character generation is accomplished by the provided MK34073 character generator. If other special characters are desired, the user may generate a custom character set in either a 2758 or 2716 EPROM and use it in place of the MK34073.

The VDI board will allow lower case characters to be generated from an upper case keyboard.

SERIAL VERSION PHOTO
Figure 1



PARALLEL VERSION PHOTO
Figure 2



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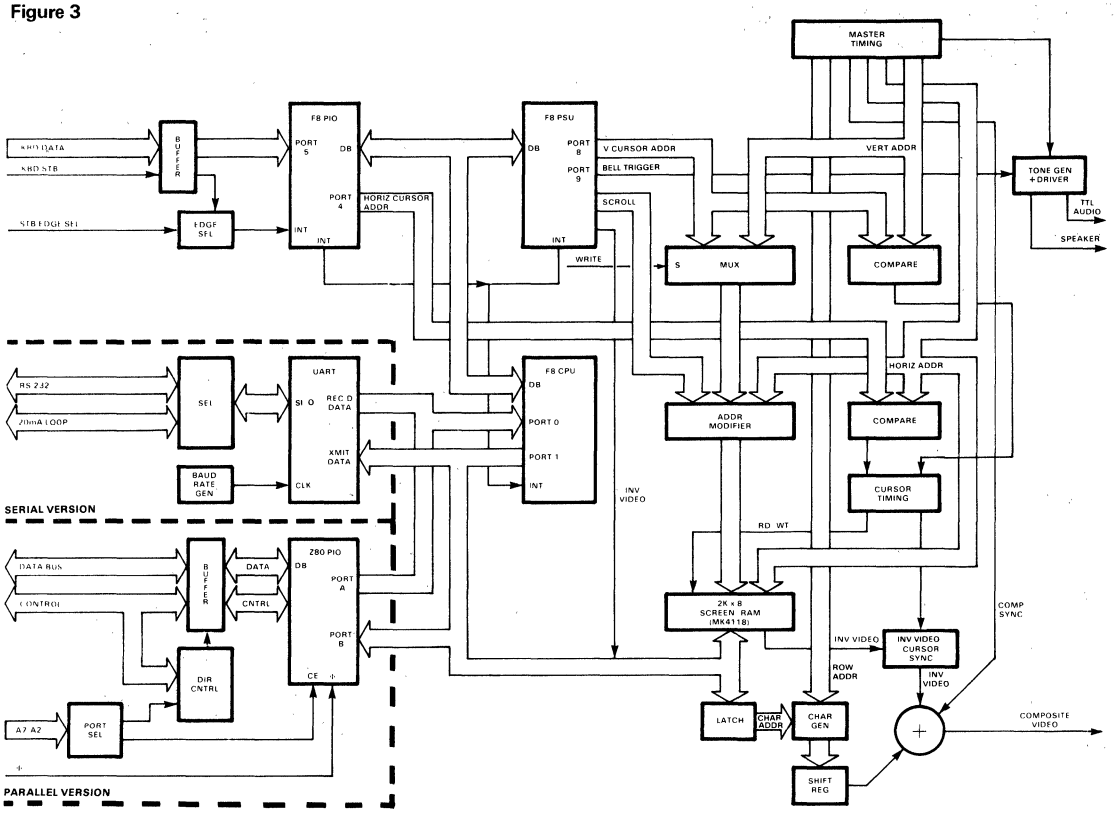
BLOCK DIAGRAM

Figure 3



BLOCK DIAGRAM DISCUSSION

The serial version VDI allows RS232-C or 20 mA Current Loop operation via a Universal Asynchronous Receiver Transmitter (UART) device. User strapping options include BAUD rate (110-9600), number of stop bits, number of bits per character, and even/odd parity.

The parallel version VDI uses the Z80-PIO for fast data transfer with a Z 80-CPU. The VDI port addressing scheme permits the use of up to 16 VDI's for use with one CPU.

The F8-PIO interrupts the F8-CPU when keyboard data is ready for transfer over the data bus.

The F8-CPU controls the flow of data according to instructions stored in the F8-PSU. Keyboard data received from the F8-PIO is sent to the system via the UART or Z80-PIO. Data received by the system is processed by the CPU and characters are written to screen memory via port 1. Likewise, screen memory data can be sent back to the system via port 1. The CPU also updates horizontal and vertical cursor addresses. The 48-character FIFO is implemented using 48 bytes of the 64-byte scratchpad RAM within the CPU.

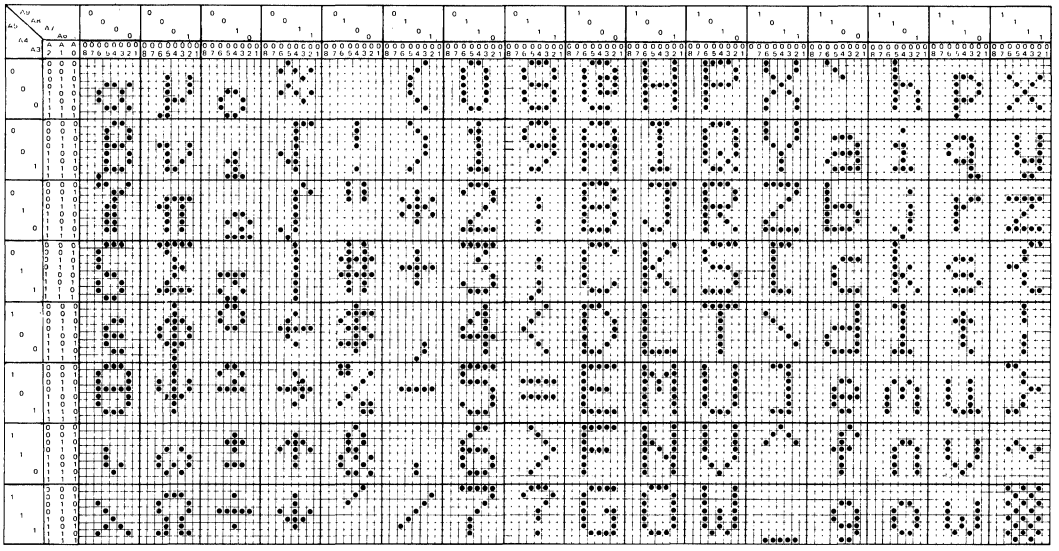
The F8-PSU not only provides 1K bytes of ROM storage for the VDI driver program, but has two I/O ports for vertical cursor and scroll addressing.

The Master timing block consists of a hybrid crystal oscillator module and a series of counters which generate all necessary horizontal and vertical sync and blanking pulses, plus a 12-bit screen address. Since only 11 addresses are required for the 2K-byte memory, the 12-bit address must be compacted to 11 bits by the Address Modifier. The horizontal and vertical screen memory address are constantly being compared to the current cursor address to generate proper read/write timing.

The video monitor is refreshed with the contents of the screen memory at a rate of 50/60 Hz. On power-up, screen memory is first cleared (loaded with spaces), then loaded with character data from the system. The 7-bit ASCII character from memory is latched and applied to the character generator as a character address. The row address is supplied by the master timer. The character dots are then loaded into the shift register and output serially to the composite video driver along with sync, blanking, and inverse video control signals.

MK34073 CHARACTER GENERATOR SYMBOLS

Figure 4



SPECIFICATIONS

SDE BUS INTERFACE

Inputs: One 74LS Load Max.
Outputs:

BAUD RATE: VOL = 0.4 V max @ IOL = 12 mA
VOH = 2.4 V min @ IOH = -3 mA

DATA BUS: VOL = 0.5 V max @ IOL = 24 mA
VOH = 2.0 V min @ IOH = -15 mA

INTB & DINB: (Open collector outputs)
VOL = 0.4 V max @ IOL = 16 mA
VOL = 0.7 V max @ IOL = 40 mA
IOH = 250 μA max @ VOH = 30 V

KBD ACK: VOL = 0.5 V max @ IOL = 8 mA
VOH = 2.7 V min @ IOH = -0.4 mA

TTL AUDIO: VOL = 0.5 V max @ IOL = 20 mA
VOH = 2.7 V min @ IOH = -1.0 mA

SPEAKER OUTPUT: A high level output is provided for driving a 50 ohm speaker directly.

VIDEO OUTPUT: EIA RS-170 Compatible (75 Ohm, 1 V p-p)

OPERATING TEMPERATURE

0 to 50° C

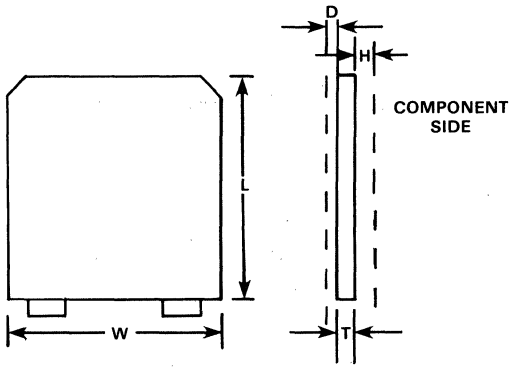
POWER SUPPLY REQUIREMENTS

Serial Version: +5 V ± 5% @ 1.8 A max
+12 V ± 5% @ 80 mA max
-12 V ± 5% @ 25 mA max

Parallel Version: +5 V ± 5% @ 1.9 A max
+12 V ± 5% @ 50 mA max

V

BOARD DIMENSIONS



Dimension		Typical	Maximum
L	Board Length	250.0 mm (9.84 in)	250.2 mm (9.850 in)
W	Board Width	233.4 mm (9.19 in)	233.7 mm (9.200 in)
H	Component Height	———	13.0 mm (0.510 in)
T	Board Thickness	1.6 mm (0.062 in)	1.7 mm (0.065 in)
D	Lead Length	2.3 mm (0.090 in)	2.5 mm (0.100 in)

CONNECTORS

FUNCTION	DESCRIPTION	MATING CONNECTOR
SDE BUS	Dual 64-pin Eurocard Connector, DIN 41612 form D; A and C pinned	Wire Wrap Tail: Winchester #96s-6033-0522-1 ELCO #8257-096-648-124 Solder Tail: Winchester #96s-6033-0522-3 ELCO #8257-096-649-124

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
SVDI-80E-60	Serial version Video Display Interface board (60 Hz operation) with Operations Manual.	MK78198
SVDI-80E-50	Serial version Video Display Inteface board (50 Hz operation) with Operations Manual.	MK78033
PVDI-80E-60	Parallel version Video Display Interface board (60 Hz operation) with Operations Manual.	MK78199
PVDI-80E-50	Parallel version Video Display Interface board (50 Hz operation) with Operations Manual.	MK78035
VDI-80E	Operations Manual Only (for all versions of VDI-80E boards).	MK79876

VI SDE Series Accessories

SDE SERIES ACCESSORIES
SDE-ACC
MK78152, MK79062, MK79063, MK79090, MK79088, MK79089, MK78187, MK78193

INTRODUCTION

The following items are available as accessories to support design, development, and production of products designed around the Mostek SDE Series Z80* microcomputer modules:

SDE-WW1	Wire-wrap board with bussed power and ground
SDE-EXT	Extender board
SDE-CRT-C	Matrix to CRT Cable
SDE-CPTR-C	Matrix to Centronics Printer
SDE-PPG-C	Matrix to PROM Programmer
SDE-DFE-C	Matrix to RMDFSS Cable
SDE-2DFE-C	Matrix to two RMDFSSs
SLD-KIT	Rack Mount Slide-Kit
RMDC	Rack Mount Dust Cover
TTCP	Table Top Conversion Package

WIRE WRAP BOARD

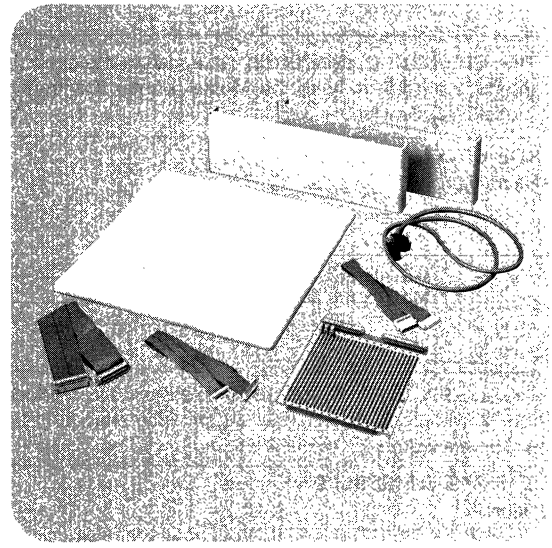
The SDE-WW1 (MK79063) is a wire wrap board with power and ground lines on the board to facilitate fabrication of circuits using wire-wrap sockets. Three rows of plated-through holes (spaces on 0.100 inch centers) are provided on the top edge of the board for mounting standard connectors. The spacing of the holes throughout the board are also on 0.100 inch centers to accommodate all IC Dual in-line Packages, discrete components, and 0.025 inch square posts.

EXTENDER BOARD

The SDE-EXT (MK79062) is a board that extends the bus signals out from the enclosure to suspected malfunctioning system board. This allows a technician the space required to use test probes or monitor signals at the component level on the board. The board is of a multi-layer design (an insulated ground plane sandwiched between the upper and lower signal trace etches of the board). This design decreases the amount of cross-talk between signal-runs. Additionally three light emitting diodes (LEDs) are mounted on the SDE-EXT board and are wired to the power signal etch lines. A technician can tell at a glance that all three power sources (+5 V, +12 V, and -12 V) are present.

SDE-ACC

Figure 1



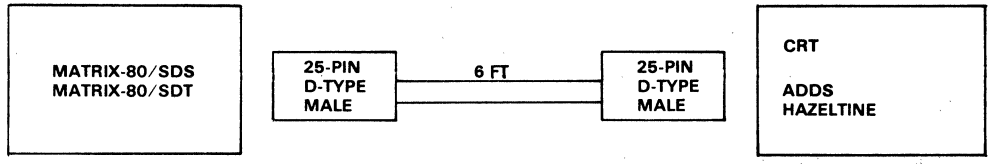
VI

CABLES

The SDE-CRT-C (MK78152) is a cable designed to interface the Matrix with a Video terminal (CRT). Both ends are a 25-pin D-type male connector. See Figure 2.

SDE-CRT-C MK78152

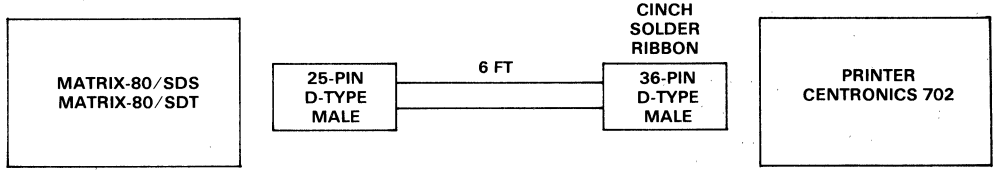
Figure 2



The SDE-CPTR-C (MK79089) is a cable designed to interface the Matrix with the Mostek printer (Centronics model 702). See Figure 3.

SDE-CPTR-C MK79089

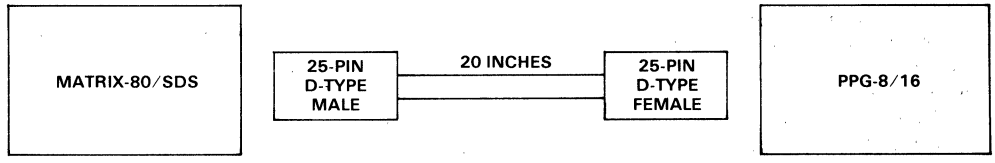
Figure 3



The SDE-PPG-C (MK79090) is a cable designed to interface the Matrix-80/SDS with the PROM Programmer PPG-8/16. See Figure 4.

SDE-PPG-C MK79090

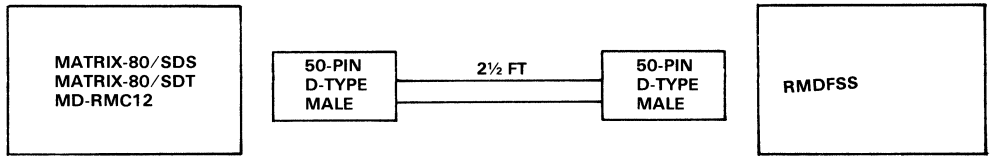
Figure 4



The SDE-DFE-C (MK79088) cable is designed to interface the Matrix-80/SDS CPU enclosure to the Floppy-disk drive enclosure. Both ends of the cable are 50-pin, D-type, Male connectors. See Figure 5.

SDE-DFE-C MK79088

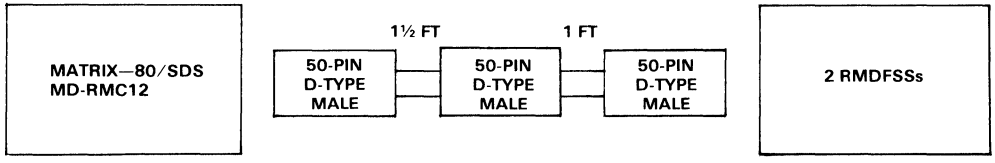
Figure 5



The SDE-2DFE-C cable is designed to interface the Matrix-80/SDS CPU enclosure to two floppy-disk drive enclosures. Both ends of the cable are 50-pin, D-type, male connectors with an additional connector (50-pin, D-type, male) in between the ends spaced as shown in Figure 6.

SDE-2DFE-C

Figure 6



SLIDE KIT

The SLD-KIT (MK78192) is designed specifically for mounting Mostek's rack-mountable enclosures in a standard E.I.A. 19-inch rack. The kit contains two slides with mounting hardware. The slides are installed underneath the enclosure. The SLD-KIT will mount the following enclosures:

* Matrix-80/SDS (MK78188, MK78189)
  Matrix-80/SDT (MK78197)
  SDE-RMC6 (MK78182-1, MK78182-2)
  RMDFSS (MK78183)
  RMDFSS-50 (MK78185)
  MD-RMC12 (MK77966)
  MD-RMC12-50 (MK77975)

*Note: Two slide kits are required.

RACK MOUNT TOP

The Top is a black, solid metal plate which serves as a top. This metal lid is required for all table top configured systems which are being converted to a rack-mounted configuration. The cover snaps-on in the same manner as does the structural-foam lid, and is dimensioned to fit as a lid while in the 19-inch rack, whereas the structural foam lid is not. The top is not used for rack mounted enclosures when they are stacked (butted up) one on top of each other. However, when there is no enclosure above to prevent dust from entering the unit, a top is recommended.

TABLE TOP CONVERSION PACKAGE

The TTCP (MK78187) is a kit containing two structural-foam side skins, lid, and mounting hardware. The purpose of this kit is to be able to configure a rack mounted system to a table top configuration. One TTCP kit is required for each rack mounted enclosure. This kit is designed for the following enclosures:

SDE-RMC6	MK78182-1, MK78182-2
RMDFSS	MK78183, MK78185
MD-RMC12	MK77966
MD-RMC12-50	MK77975

ORDERING INFORMATION

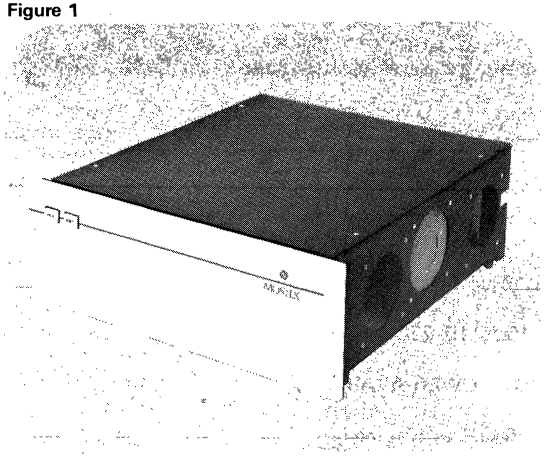
DESIGNATOR	DESCRIPTION	PART NO.
SDE-WW1	Wire Wrap Board	MK79063
SDE-EXT	Extender Board	MK79062
SDE-CRT-C	Matrix to CRT Cable (Male)	MK78152
SDE-CPTR-C	Matrix to Centronics Printer	MK79089
SDE-PPG-C	Matrix to PROM Programmer	MK79090
SDE-DFE-C	Matrix to RMDFSS	MK79088
SDE-2DFE-C	Matrix to two RMDFSSs	
SLD-KIT	Slide Kit	MK78193
RMDC	Rack Mount Top	
TTCP	Table Top Conversion Package	MK78187

SDE-RMC6
MK78182-1, MK78182-2

FEATURES

- ☐ Standard 19-inch rack-mountable chassis; 7-inch panel height
- ☐ Removable structural foam front panel for internal access
- ☐ Front panel RESET switch and POWER-ON indicator
- ☐ Six-slot card cage
- ☐ Cards mounted horizontally for ease of cooling and cable routing
- ☐ Self-contained power supply and 115 CFM fan
- ☐ 100/115/230 Volt 50/60 Hz operation

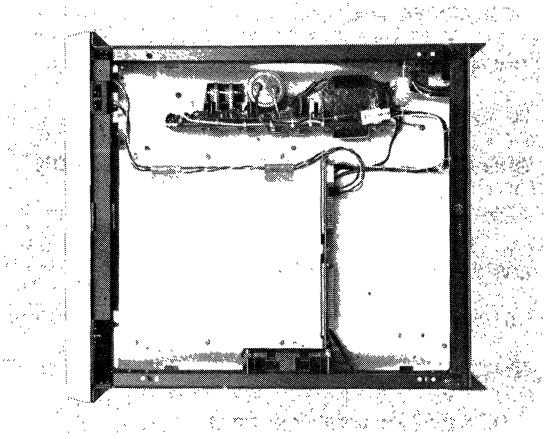
SD-RMC6 PHOTO
Figure 1



DESCRIPTION

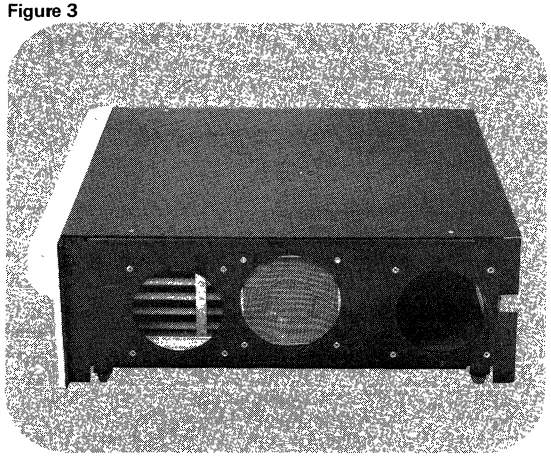
The Mostek SD Series rack-mount system (SDE-RMC6) offers a solution to rack mounting the line of SDE Series Microcomputer modules. The system features a self-contained power supply designed to work on voltages and frequencies available world-wide. All components are easily removed from front or top for improved maintenance. An attractive structural foam front panel is provided with system RESET switch and POWER-ON indicator. The front panel is designed with quick-release ball studs so that it can be quickly removed for access to internal components. The cards are mounted in a horizontal plane with I/O cabling at the rear of the card cage. The back panel has an I/O panel pre-punched for twelve 25-pin "D" type connectors, one 50-pin "D" connector, and one BNC connector for versatility. AC components on the back panel were selected to meet UL and VDE requirements and include: On/Off switch, voltage selection switch, fuse holder (3AG or 5 x 20 mm), and AC input receptacle/line filter.

SD-RMC6 Interior View
Figure 2

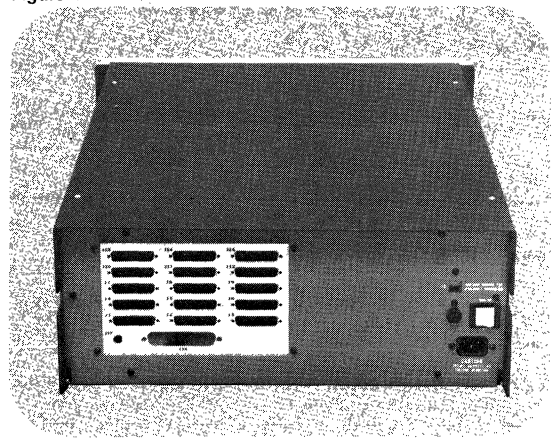


VI

SD-RMC6 Side View
Figure 3



SD-RMC6 Rear View
Figure 4



INPUT POWER

100/115/230 volts AC ± 10% 50/60Hz

DC POWER AVAILABLE

+5 VDC at 12A max.
+12 VDC at 1.7A max.
-12 VDC at 1.7A max.

LOAD REGULATION

± .05% for a 50% load change

OUTPUT RIPPLE

3.0 mV PK-PK max.

TRANSIENT RESPONSE

30 microseconds for a 50% load change

SHORT CIRCUIT AND OVERLOAD PROTECTION

Automatic current limit/foldback

OVERVOLTAGE PROTECTION

+5 Volt output, set to 6.2 ± 0.4 volts

STABILITY

± 0.3% for 24 hours after warmup

THERMAL PROTECTION

Bi-metal thermostat or primary AC line set to cut out at 180°F (82°C)

CARD CAGE

Six slot for SD/E series module (250mm x 233.4mm) (9.19 x 9.84 in). Wire-wrap tail connector provided for SK2 I/O connectors. All SK1 connectors wired one-to-one. No PC modules supplied.

FUSING

Line Voltage	MK78182-1	MK78182-2
110/115V	3 Amp 3AG*	3 Amp 5 x 20 mm
230 V	1.5 Amp 3AG	1.5 Amp 5 x 20mm*

*Configuration as shipped

LINE CORD SUPPLIED

MK78182-1	MK78182-2
Similar to Belden model 17205B	Similar to Feller model 1100

FRONT PANEL CONTROLS

RESET switch
POWER ON Indicator

REAR PANEL CONTROLS

AC Power On/Off
AC fuse holder
AC line receptacle/filter
AC line voltage selector

WEIGHT

25 lbs (11.3 kg)

CHASSIS

a) 19" rack-mountable using the two rails supplied.
b) Slide mounting available with optional slide mounting bit and requires two inches of panel space below the unit.

OPERATING TEMPERATURE RANGE

0°C to 60°C

HUMIDITY

Up to 90% relative, non-condensing

DIMENSIONS

Height: 7.0 in. (17.8 cm) panel space
7.3 in. (18.5 cm) overall, including feet

Width: 19.0 in. (48.3 cm) at front panel
17.5 in. (44.5 cm) behind front panel

Depth: 21.1 in. (53.6 cm) with all protrusions
20.0 in. (50.8 cm) without foam front

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
SDE-RMC6	Rack-mounted CPU subsystem with SD/E series six-slot card cage with U.S. line cord and fuse. 100/115/230 Volts 50/60 Hz AC operation front panel, rails for rack mounting and operation manual included.	MK78182-1
SDE-RMC6-50	Same as above except with 5 x 20 mm fuse and European line cord.	MK78182-2
SDE-RMC6 to CRT	CRT Interface Cable Only	MK78152
	SDE-RMC6 Operations Manual Only	MK79783
SLD Kit	Slide Kit	MK78193
TTCP	Table Top Conversion Package	MK78187

The following Mostek modules are compatible with the above CPU subsystem

OEM-80E	CPU Module Data Sheet	MK78550
RAM-80E	RAM Expander Data Sheet	MK78590
FLP-80E	Floppy Disk Interface Data Sheet	MK78572
VDI	Video Display Interface Data Sheet	MK78591
A/D-80E	A/D-D/A Interface Data Sheet	MK79709

1983 COMPUTER PRODUCTS DATA BOOK

VII Development Systems

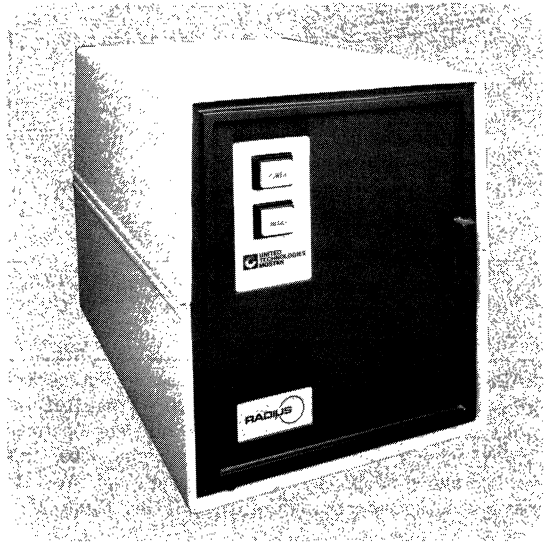
VII

RADIUS™ REMOTE DEVELOPMENT STATION

FEATURES

- ☐ Microcomputer development with host computer
  - Software development on the host
  - Download to RADIUS
  - Hardware debug and software integration on RADIUS
- ☐ Utilizes standard Mostek SDE series AIM modules
- ☐ Host software available
  - Preconfigured for selected hosts
  - Reconfigurable for other hosts
- ☐ Upload/download performed with error tolerant protocol
- ☐ Emulation possible while disconnected from the host
- ☐ Serial I/O Baud rate up to 9600
- ☐ Supports optional local line printer and PROM programmer
- ☐ Self-diagnostic test

RADIUS
Figure 1



INTRODUCTION

Mostek RADIUS - Remote Access Development and Integration μcomputer System - is a state-of-the-art microcomputer development system, designed specifically to be used in a host computer environment. RADIUS provides software development capability via the host computer and hardware development and software integration using the advanced in-circuit-emulation capability of Mostek AIM modules.

RADIUS is installed between the user's CRT terminal and the host computer via an ASCII RS-232 serial interface. See Figure 2. It can be operated in any of three modes: Transparent, Local or Utility.

In Transparent Mode, the user can:

- Perform any function that can be performed on the host computer. RADIUS becomes completely transparent to the user.

In Local Mode, the user can:

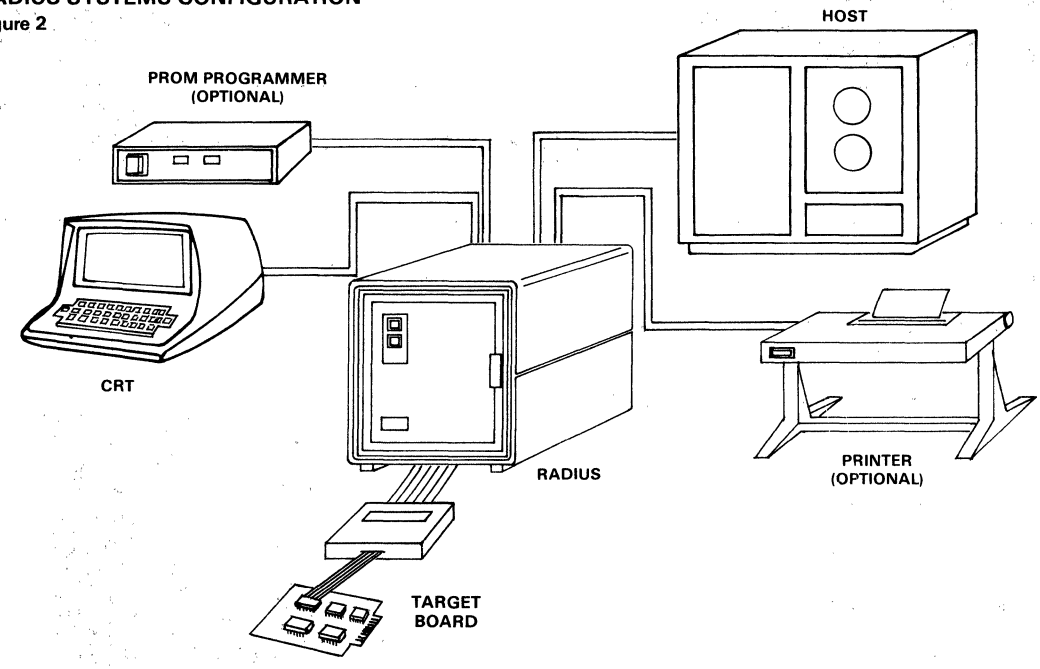
- Set optional Baud rates and special RADIUS control characters
- Perform self diagnostics on RADIUS

In Utility Mode, the user can:

- Run the host components of the RADIUS Utility Packages (i.e. AIM-Z80BE, AIM-7XE, Line Printer Utility, PROM Programmer Utility, etc.).
- Perform hardware debug and software integration.

RADIUS has no mass storage. Instead it uses the mass storage capabilities of the host. Once the user's target program is downloaded, the user has the option of disconnecting the RADIUS from the host. This allows the user to save connect time and long distance charges.

RADIUS SYSTEMS CONFIGURATION
Figure 2



RADIUS can be configured in a single-user environment or in a multi-user environment, in which several RADIUS units are connected to an appropriate host and operated simultaneously, performing entirely separate jobs. This configuration supports the development of multiple microprocessor/microcomputer systems. See Figure 3.

DEVELOPMENT SYSTEM

RADIUS is a cost effective microcomputer development tool. It consists of an integrated cabinet, power supply, I/O panel, and a Z80 based processor module with four serial I/O ports.

RADIUS is supplied with a host communications software package configured for several popular mini/micro-computer systems. (See ordering information.) A user rehostable version is available for other host computers. Additional preconfigured versions of the RADIUS host software will be provided in the future.

RADIUS HARDWARE FEATURES

RADIUS consists of a structural foam cabinet, a Z80 based RADIUS processor board, and a power supply board. The user can add AIM-68000, AIM-Z80BE, or AIM-7XE modules to RADIUS to perform the full range of real time in-circuit emulation needed for hardware development and software integration. Future AIM products will be completely supported on RADIUS.

The cabinet is divided into two compartments: the power supply compartment on the left and the processing compartment on the right. The processing compartment can house up to five boards: a RADIUS processor board, two-card AIM module set, and two slots for future expansion.

The RADIUS processor board contains:

- Z80 CPU
- 64 Kbyte internal systems memory
- Four SIO ports;
  - one dedicated to user terminal, one to the host computer, and two for optional printer and PROM programmer
  - RADIUS supports 11 standard Baud rates from 50 to 9600 Baud

RADIUS SOFTWARE FEATURES

- Local mode to set options on RADIUS and to perform local diagnostics
- Most link parameters set at host configuration time
- Full AIM command set available
- AIM packages can run command files from the host
- AIM packages can log all terminal output to the host
- Progress of download/upload indicated on CRT
- Protocol re-transmits messages upon line error
- Self-explanatory error messages
- Translators to convert INTELHEX, TEKHEX, Motorola S-Record, and F8HEX object formats to Mostek HEX
- Local PROM programming (optional)
- Local printing (optional)
- Self diagnostic test

RADIUS local mode provides the following commands:

- HELP
- PORT
- MEMORY
- OPTIONS
- DIAGNOSE
- QUIT

SPECIFICATIONS

The power supply board has single phase AC input at 47 Hz to 63 Hz for the following voltage ranges:

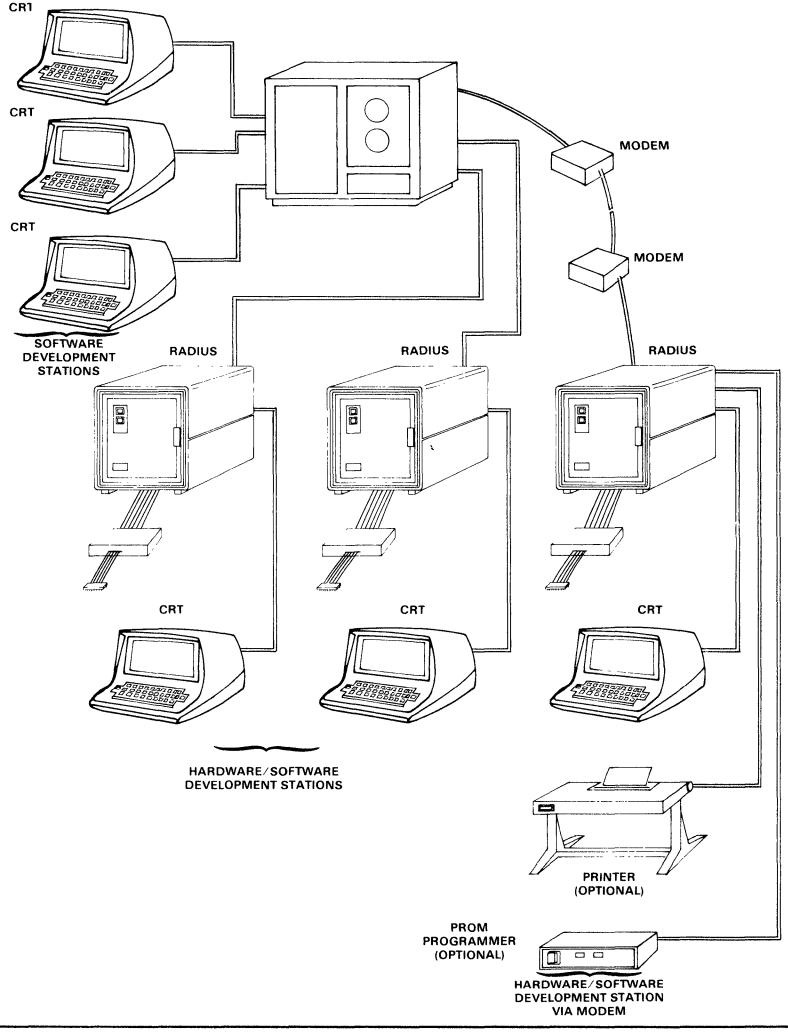
- 95 V to 132 V
- 190 V to 264 V

The approximate dimensions are:

- Width: 9.2"
- Height: 10.8"
- Depth: 12.6"

RADIUS INSTALLATION IN A MULTI-USER ENVIRONMENT

Figure 3



ORDERING INFORMATION

For detailed ordering information refer to the Development System Products Ordering Guide.

FEATURES

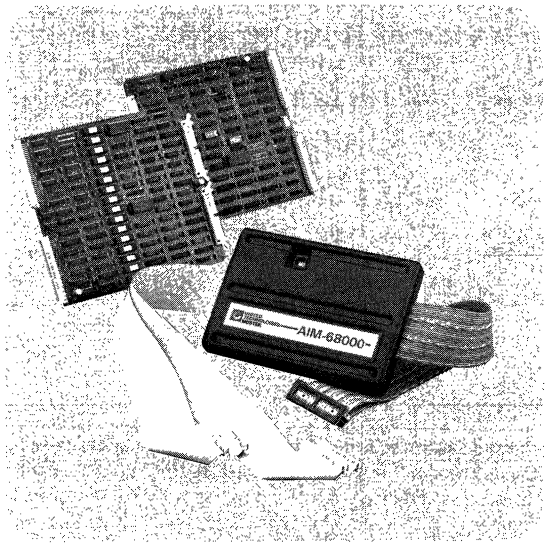
- In-circuit emulation for the MK68000 processor
- Real-time execution to 10 MHz with no wait states
- Direct interface to Mostek's RADIUS Station and MATRIX Development System
- 16K words of Emulation Memory mappable in 2K word blocks on 2K address boundaries; Illegal "Write-to-Memory" Detection provided
- "Stand-alone" Mode allows Software Debug with no Target System
- Flexible breakpoints: Hardware, Software, and Timer
- Single Step execution with Break on Register Contents
- Instruction trace memory for tracing Instruction Execution History ("Soft Trace")
- Exception Handler Routines provided
- Symbolic Addressing Capabilities
- Batch Mode and User Activity Logging provided
- Extensive HELP facility
- Disassembly of Instructions in memory
- English oriented Command Structure

GENERAL DESCRIPTION

AIM-68000 is an advanced development tool which provides debug assistance for both hardware and software via in-circuit emulation of the MK68000 microprocessor. All CPU signals are active during user program execution. No memory wait states are required.

The user friendly command structure consists of English-like commands. A structured HELP facility and the ability to enter keywords allow easy system familiarization. As the user becomes more familiar with the system, commands may be abbreviated. A BATCH facility with PAUSE allows a list of commands on the host to be executed. This feature is useful for test environments and lengthy program setups.

AIM-68000
Figure 1



Single Step capability allows the user to execute instructions one at a time and examine registers to see the exact effect of each instruction. The Single Step function operates in either ROM or RAM.

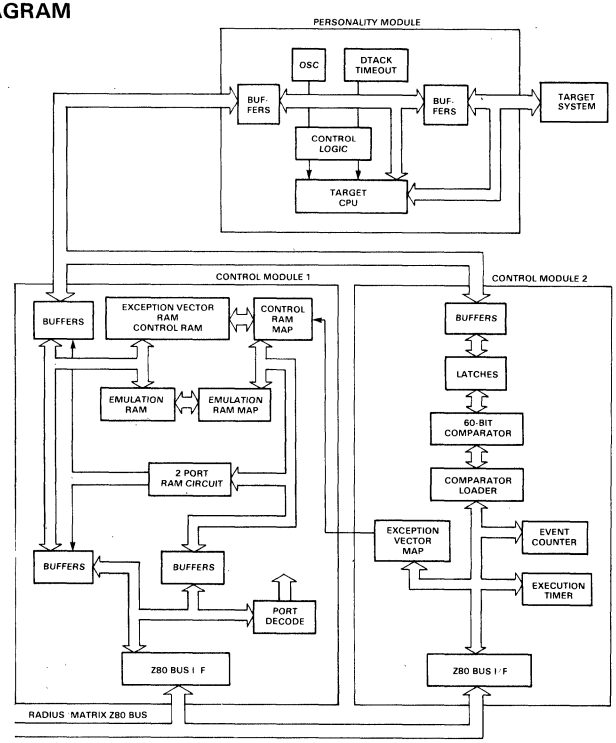
Up to 16K words of Emulation RAM can be used to emulate user Target ROM or RAM. This memory may also be used while the emulator operates in Stand-alone mode, allowing software development prior to hardware availability.

AIM-68000 breakpoint conditions allow 8 software breakpoints, one hardware breakpoint, and one timer breakpoint to be set.

The Hardware Breakpoint detect circuitry allows user program execution to proceed until a specified bus condition occurs. The Breakpoint consists of address, data, function codes, and an external "ARM" bit which allows the Hardware Breakpoint to be slaved to an external TTL input. Any of the Breakpoint condition bits may be designated as a "don't care" bit by setting the "match bits" option. An Event Count and Timer Breakpoint further enhance the Hardware Breakpoint facility.

A software Trace Buffer allows the storage of register

AIM68000 BLOCK DIAGRAM
Figure 2



contents and processor status during single step or Invisible Trace. Invisible Trace allows single stepping to proceed with no information displayed at the user's console. A powerful additional feature of the software trace is the Register Content Breakpoint Function which forces stepping to stop upon the occurrence of a specified set of register conditions. The Trace Buffer may be Reviewed after stepping terminates.

BLOCK DIAGRAM DESCRIPTION

The AIM-68000 emulator consists of two boards, Control 1, Control 2, and a Personality Module. The two control boards are attached to the personality module which contains the MK68000 CPU and plugs into the Target system CPU socket directly. Switch options in the personality module allow the user to operate AIM-68000 in a Stand-alone mode.

Control Board 1 contains the Emulation Memory, the Emulation Memory Map, Control RAM, the Control RAM Map, and the two port memory access circuitry. In addition, the Write Violation Detect circuitry is located on Control Board 1.

Control Board 2 contains circuitry for the Hardware Breakpoint, Timer Breakpoint, the Exception Vector Map, and Keyboard Escape.

The Personality Module contains an on board 10 MHz clock generator, the DTACK timeout hardware, and a number of buffers and associated steering logic.

USING AIM-68000

When AIM-68000 is attached to the user Target System, it effectively becomes part of the user's system. It is important to understand the implications of this addition. The considerations may be grouped into four areas. They are:

1. System (i.e., Emulation) Memory
2. Control Memory
3. Exception Vector Memory
4. MK68000 CPU Control Signals

SYSTEM MEMORY

System Memory may be mapped into or out of the user's memory space via the MAP command. If a block of memory is mapped as System resident, the memory will appear in the user's memory map. AIM-68000 provides a DTACK signal to the MK68000 CPU for those areas which are mapped as System and the memory cycles terminate with no wait states.

CONTROL MEMORY

Control Memory: AIM-68000 requires 1K words of the user's memory space. The default location for this memory is 24000H; however, it may be relocated via the INIT

command to reside anywhere in the MK68000 memory space. Control Memory is a two-port memory which may be accessed both by the MK68000 and the development system's Z80 CPU. The user software must not access the 1K word area of Control Memory.

The MK68000 executes in control memory whenever user software is not being executed. Execution in control memory may include the insertion of several wait states in a memory cycle; however, all user software is executed in real time with no wait states up to 10 MHz.

EXCEPTION VECTOR MEMORY

Exception Vector Memory is located at addresses 0-0FFH. Each exception Vector may be mapped as System or Target resident. If a vector is mapped as System Resident, AIM-68000 will provide the DTACK signal for the MK68000 CPU.

The RESET, NMI, and ILLEGAL INSTRUCTION vectors are special cases and are used to perform emulator functions. They operate as follows:

RESET: Is mapped as System Resident upon Initialization (INIT Command). Immediately after initialization, this vector is mapped as Target resident. It may not be remapped as system resident.

NMI: NMI is a shared Level 7 Autovector interrupt used by both AIM-68000 and the user. It may be mapped as either System or Target resident. If it is mapped as System resident, the response to a Level 7 Autovector Interrupt will be a message displayed on the user console. The user NMI vector is read from the Target system prior to execution. The user must not alter the Level 7 Autovector during program execution.

ILLEGAL INSTRUCTION: Illegal Instruction is the vector used by AIM-68000 to generate the Software Breakpoint. It may be mapped as either System or Target resident. The user Illegal Instruction vector is read from the target system prior to the start of execution. The user must not alter the vector during program execution.

Since the actual exception vectors fetched by the MK68000 are not always the vectors in Target memory, the user should not attempt to run memory verification programs on the Exception Vector Table.

MK68000 CPU CONTROL SIGNALS

All address lines, address strobe, and data strobes are presented to the Target System at the CPU socket for all memory accesses, whether they are for Target or AIM-68000 system resident memory. Data is presented on the data lines only during memory write cycles. MK68000 signal delay information is provided in the Specifications section.

AIM-68000 SOFTWARE

AIM68K is the software which operates the AIM-68000 emulator in either the RADIUS or MATRIX development system. In the RADIUS environment, Target software programs are generated and assembled on the host computer. The hex object module is downloaded into AIM-68000 and/or Target memory via the GET command.

The AIM68K software for use with the RADIUS station is available on several different formats for a variety of host computers. The software will be supplied on a flexible diskette for use in the MATRIX Development System.

COMMAND SUMMARY

The user commands for AIM68K are summarized in Table 1. Each command may also be entered in an abbreviated form. Keywords are allowed in the command syntax to promote rapid user familiarization.

AIM-68000 USER COMMANDS

Table 1

COMMAND	DESCRIPTION
ACCESS	Define memory accesses as word or byte
BASE	Set or Display Memory Offset
BATCH	Submit a Batch File
BREAK	Set or Display a Breakpoint
	Hardware Breakpoint
	Event Count for Hardware Breakpoint
	Trigger for Hardware Breakpoint
	Mask for Hardware Breakpoint
	Software Breakpoint (RAM only)
	Timer Breakpoint
	Register Contents Breakpoint (for use with STEP or GO command)
CLEAR	Clear one or more Breakpoints
COPY	Copy a block of memory to another area
DELETE	Delete a symbol
DISASSEMBLE	Disassemble instructions in memory
DUMP	Dump memory to a file
EXECUTE	Begin user program execution
FILL	Fill memory with a data pattern
GET	Load user program or mapping configuration
GO	Invisible Single Step with Trace
HELP	Display command syntax and description
	Structured to provide two levels of information for commands
HEXADECIMAL	Evaluate a hexadecimal expression
INITIALIZE	Initialize AIM-68000; Relocate Control Memory
LOCATE	Locate a pattern of data in memory
LOG	Log user activity to a host file
MAP	Map emulation memory into target memory space
MEMORY	Display and/or update memory
QUIT	Terminate AIM-68000 operation
RAMTEST	Test RAM memory; continuous test option
REGISTER	Examine or modify register contents
REVIEW	Examine the Software Trace buffer
SELECT	Choose registers or symbols for Step and Trace Display
SET	Set Exception Vector Map
SYMBOL	Enter or display symbols in table
STEP	Single Step with Software Trace
TRANSPARENT	Communicate with the host transparently
VERIFY	Verify memory against other memory

Note that the ACCESS command limits emulator accesses to word wide or byte wide operations only. A write only option for the MEMORY command allows the user to set up programmable peripheral devices manually.

SPECIFICATIONS

Target Operating Frequency	1.0 to 10 MHz
Standalone Operating Frequency	10 MHz
Operating Temperature Range	0° - 40°C
Target Power Requirement	None

Signals from the MK68000 have the following maximum delays:

Signal	Delay
A1-23	0 ns
/AS	0 ns
/BERR	40 ns
/BR	22 ns
/BG	0 ns
/BGACK	0 ns
CLK*	8 ns
D0-D15 t_{CLDO}**	145 ns @ 10 MHz 135 ns @ 8 MHz 100 ns @ 6 MHz
/LDS,/UDS	0 ns
/DTACK	14 ns
E	0 ns
FC2-0	0 ns
/HALT	0 ns
IPL2-0	40 ns
R/W	0 ns
/RESET	0 ns
/VMA	0 ns
/VPA	20 ns

* Skew from the Target CLK to the MK68000 CLK input.

** On a write cycle, DATA valid at the Target after the falling edge of S2, t_{CLDO} max.

ORDERING INFORMATION

For information on ordering AIM-68000 hardware and the appropriate AIM68K software, refer to the Development Products Ordering Guide.

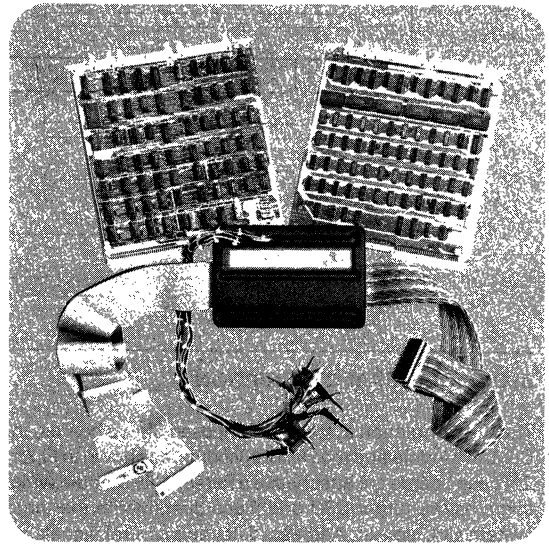
AIM-Z80BE APPLICATION INTERFACE MODULE

FEATURES

- Direct interface to Mostek's RADIUS Development Station and MATRIX-80/SDS Development System
- In-circuit emulation of the Z80 microprocessor
- Real-time execution (to 6 MHz with no wait states)
- Flexible breakpoints (one hardware, eight software, and one timer)
- Single-step execution
- 16 K bytes of emulation RAM
- Memory mappable into target or AIM system memory in 256 byte blocks
- Illegal write-to-memory detection
- Non-existent memory mapping and access detection
- Forty-eight-channel-by-1024-words history memory for tracing bus events
- T-state timer to measure execution time
- English-oriented command structure
- Disassembly of instructions
- System configuration parameters can be saved for future use

AIM-Z80BE PRODUCTS

Figure 1



GENERAL DESCRIPTION

AIM-Z80BE is an advanced development tool which provides debug assistance for both software and hardware via in-circuit-emulation of the Z80 microprocessor. Use of the AIM-Z80BE is transparent to the user's final system configuration (referred to as the "target"). No memory space or user ports are used, and all signals, including $\overline{\text{RESET}}$ $\overline{\text{INT}}$, and NMI are functional during emulation. No memory wait states are required.

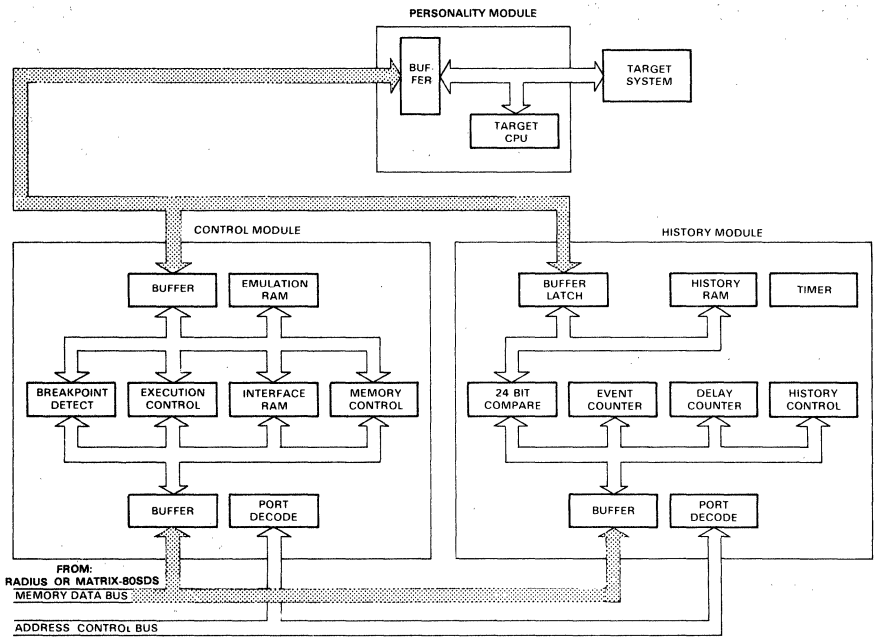
Single-step circuitry allows the user to execute target instructions one at a time to see the exact effect of each instruction. Single step is functional in both ROM and RAM. Up to 16K bytes of contiguous emulation RAM can be used to emulate the target microprocessor RAM or ROM. Thus, debugging can begin before the user system is completely configured with memory.

Breakpoint-detect circuitry allows real-time execution to proceed to any desired point in the user's program and then terminate execution. All CPU status information and register contents can be displayed for the user and saved for later continuation of execution or single-stepping. Real-time execution may be terminated by the user at any time. EVENT and DELAY counters associated with the hardware breakpoint give added flexibility for viewing the exact point of interest in the user's program.

A forty-eight channel history memory records up to 1024 bus transactions. The address bus, data bus, control signals, and 18 external probes may be logged into the history memory and later displayed by the user.

AIM-Z80BE BLOCK DIAGRAM

Figure 2



BLOCK DIAGRAM DESCRIPTION

The Z80 emulation system is composed of two boards, the Control Module and the History Module, as shown in Figure 2. These boards are attached to a Personality Module which contains the target CPU and plugs directly into the target system CPU socket. Address, data, and control signals are buffered by the Personality Module and cabled to the Control and History Module installed in the development system.

The Control Module has the circuitry for detecting the breakpoint condition(s) and forces program execution to begin in a separate System Interface RAM. The System Interface RAM is loaded with an interface program and is shadowed into the target memory space. This control program makes the target CPU a slave to the development system. When the user desires to resume execution of his program, the control program activates the execution control circuit and execution resumes at the desired address. The Control Module contains 16 K bytes of emulation RAM, which may be mapped into any address space required by the target system. Alternatively, if the user's system has memory available, he may use that as his target memory instead of the memory on the Control Module.

The History Module has a 24-bit comparator circuit, an EVENT counter, and a DELAY counter to detect a hardware breakpoint condition. The 48-channel-by-1024-word history RAM is controlled by the History Control Circuit.

The Timer Circuit is used to count target processor clocks for logging elapsed time and generating the timer breakpoint.

USING THE AIM-Z80BE

The Control and History Modules of AIM-Z80BE are installed directly into the development system. To complete the emulation system the Personality Module is used as a buffer interface between the first two boards and the target system's Z80 CPU socket.

The program which controls the AIM-Z80BE emulator system is AIMZ80. After execution of AIMZ80 is started, the program takes control of the AIM-Z80BE emulation system. The user can then initialize the target system and use the AIMZ80 commands to load, test, and debug the target program.

AIMZ80 SOFTWARE

AIMZ80 is the software which operates the AIM-Z80BE emulation system in the RADIUS Development Station or MATRIX Development System. Target system programs may be developed on a Mostek disk system by use of the appropriate assembler. Programs may be developed for RADIUS cross products supplied by Mostek or other vendors. The AIM software is supplied on a variety of media for use with Mostek disk-based development systems and with different host systems for RADIUS. The commands available in AIMZ80 are summarized below. Each command also has a "short form" which allows abbreviated input with fewer keystrokes.

BATCH	Read AIM commands from a file
BREAK	Display and set breakpoints (8 software, 1 hardware, and 1 timer breakpoint)
CLEAR	Clear one breakpoint or all breakpoints
COPY	Copy one block of memory to another block
DISABLE	Disable target CPU interrupts
DISASSEMBLE	Display and/or update instructions
DUMP	Dump a block of memory to a file
	Dump the memory map to a file
ENABLE	Enable target CPU interrupts
EXECUTE	Start or continue execution of the target program
FILL	Fill memory with a data byte
GET	Load a target program into memory
	Load the target memory map from a file
HEXADECIMAL	Perform hexadecimal arithmetic
HELP	Display a menu of commands for the user
HISTORY	Set history logging options
INIT	Reinitialize target handshake
LOCATE	Locate a pattern in a memory block
LOG	Log all console output to a file
MAP	Map the block of memory as target supplied, AIM system supplied, or non-existent, and write protected or not write protected
MEMORY	Display and/or update memory
OFFSET	Set an offset value for relative module debugging
PORT	Display and update a port on the target CPU
	Output a value to a port without reading it
QUIT	Return to the resident operating system
RAMTEST	Perform a test on the target RAM
REGISTER	Display and/or update the target CPU registers
STATUS	Display the current status of the AIM system
STEP	Perform a single or multi-step execution
TRACE	Display the contents of the history RAM
TRANSPARENT	Allows the RADIUS user to temporarily access the host
VERIFY	Verify the contents of a block of memory with another block or with a file.

SPECIFICATIONS

Target operating frequency: 500 kHz to 6 MHz (MK78204)

Target interface: all signals meet the specifications for the Z80 with the following exceptions:

1. The output low voltage is 0.5 V max at 1.8 mA for the ADDRESS, DATA, IORQ, RFSH, HALT, and BUSAK signals.
2. The input low current is 400 microamps max for the PHI clock, RESET, INT, NMI, and DATA signals.
3. The input high current is 20 microamps for the PHI clock, RESET, INT, NMI, and DATA signals.
4. The signals M1, MREQ, RD, and WR have a maximum of 25 nanoseconds added propagation delay.
5. The input signals RESET, INT, and NMI have a maximum of 45 nanoseconds propagation delay.

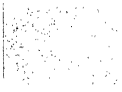
Target system power requirements: +5 V ± 5% @ 600 milliamps (maximum)

System compatibility: RADIUS, MATRIX-80/SDS,

Operating temperature range; 0 to +50 degrees C

ORDERING INFORMATION

For detailed ordering information refer to the Development System Products Ordering Guide.



AIM-7XE
APPLICATION INTERFACE MODULE

FEATURES

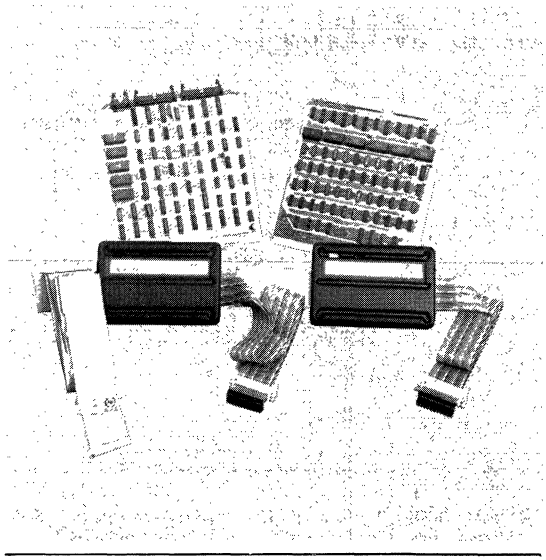
- Direct interface to Mostek's RADIUS Development Station and MATRIX-80/SDS Development System
- In-circuit emulation of all MK3870 and MK3873 family microprocessors (does not include piggy-back parts)
- Real-time execution (to 4 MHz with no wait states)
- Flexible breakpoints (one hardware, eight software, and one timer breakpoint) and any number of manually-inserted breakpoints
- Single-step execution
- 4 K bytes of emulation RAM
- Option of on-board oscillator or user clock
- Illegal write-to-memory detection
- Forty-eight-channel-by-1024-words history memory for tracing bus events
- Event counter and delay counter for monitoring bus events
- T-state timer to measure execution time
- English-oriented command structure
- Disassembly of instructions

GENERAL DESCRIPTION

AIM-7XE is an advanced development tool which provides debug assistance for both software and hardware via in-circuit-emulation of the MK3870 and MK3873 family of microprocessors. Use of the AIM-7XE is completely transparent to the user's final system configuration (referred to as the "target"). No memory space or user ports are used, and all signals, including /RESET and /EXT INT, are functional during emulation. No memory wait states are required.

Single-step circuitry allows the user to execute target instructions one at a time to see the exact effect of each instruction. 4 K bytes of emulation RAM are used to emulate the target microprocessor ROM.

AIM-7XE
Figure 1



Breakpoint-detect circuitry allows real-time execution to proceed to any desired point in the user's program and then terminate execution.

All CPU status information and registers can be displayed for the user and saved for later continuation of execution or single-stepping. Real-time execution may be terminated by the user at any time. EVENT and DELAY counters associated with the hardware breakpoint give added flexibility for viewing the exact point of interest in the user's program.

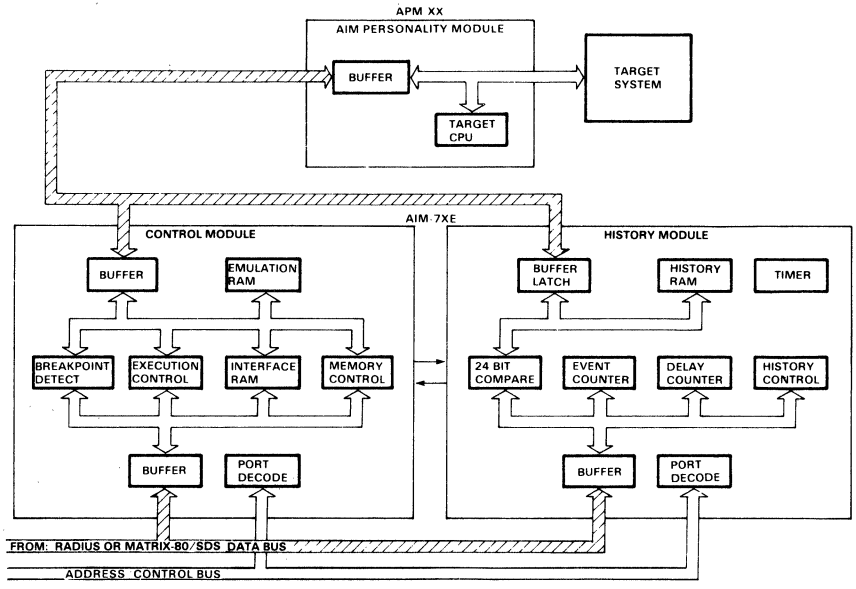
A forty-eight channel history memory records up to 1024 bus transactions. The address bus, data bus, ports 0, 1, and either port 4, 5, or 8 external probes may be logged into the history memory and later displayed by the user.

BLOCK DIAGRAM DESCRIPTION

The MK3870 Family emulation system is composed of both the AIM-7XE system and personality modules. AIM-7XE consists of two boards, the Control Module and the History Module, as shown in Figure 2. These boards are attached by cables to the Personality Module which contains the target

AIM-7XE BLOCK DIAGRAM

Figure 2



CPU and plugs directly into the target system CPU socket. Address, data, and control signals are buffered by the Personality Module.

The Control Module has the circuitry for detecting the breakpoint condition(s) and forces program execution to begin in the System Interface RAM. The System Interface RAM is loaded with an interface program and is shadowed into the target memory space. This control program makes the target CPU a slave to the development system. When the user desires to resume execution of his program, the control program activates the execution control circuit and execution resumes at the desired address.

The History Board has a 24-bit comparator circuit, an EVENT counter, and a DELAY counter to detect a hardware breakpoint condition. The 48-channel-by-1024-word history RAM is controlled by the History control circuit. The Timer circuit is used to count target processor clocks for logging elapsed time and generating the timer breakpoint.

USING THE AIM-7XE

The Control and History Modules of the AIM-7XE are installed directly into the Mostek development system. To complete the emulation system a Personality Module is required. This module is a buffer interface between the first two boards and the target system's CPU socket. Note that a complete user target system is not required to do software debugging. Only the AIM-7XE boards and a Personality Module are needed.

The program which controls the AIM-7XE emulator system is named AIM7X. After execution of AIM7X is started, the program takes control of the AIM-7XE emulation system. The user can then initialize the target system and use the AIM7X commands to load, test, and debug the target program.

AIM7X SOFTWARE

AIM7X is the software which operates the AIM-7XE emulation system in the Mostek RADIUS Development Station or MATRIX Development System. Target system programs may be developed on a Mostek disk system for RADIUS™ using cross products supplied by Mostek or other vendors. The AIM7X software is available on a diskette for Mostek disk-based systems and on a variety of media for different host systems for use with RADIUS™. The commands available in AIM7X are summarized below. Each command also has a "short form" which allows abbreviated input with fewer keystrokes.

BATCH	Read AIM commands from a file
BREAK	Display and set breakpoints (8 software, 1 hardware, and 1 timer breakpoint)
CLEAR	Clear one breakpoint or all breakpoints
COPY	Copy one block of memory to another block
DISABLE	Disable target CPU interrupts
DISASSEMBLE	Display and/or update instructions
DUMP	Dump a block of memory to a file
ENABLE	Enable target CPU interrupts
EXECUTE	Start or continue execution of the target program
FILL	Fill memory with a data byte
GET	Load a target program file into memory
HEXADECIMAL	Perform hexadecimal arithmetic
HELP	Display a menu of commands for the user
HISTORY	Set history logging options
INIT	Reinitialize target handshake
LOCATE	Locate a pattern in a memory block
LOG	Log all console output to a file
MEMORY	Display and/or update memory
OFFSET	Set an offset value for relative module debugging
PORT	Display and update a port on the target CPU
QUIT	Return to the resident operating system
RAMTEST	Perform a test on the target RAM
REGISTER	Display and/or update the target CPU registers
STATUS	Display the current status of the AIM system
STEP	Perform a single or multi-step execution
TRACE	Display the contents of the history RAM
TRANSPARENT	Allows the RADIUS user to temporarily access the host
VERIFY	Verify the contents of a block of memory with another block or a file

SPECIFICATIONS

Target operating frequency: 1 to 4 MHz

Target interface: All signals meet the specifications of the MK3870 family except that the XLT2 input will not accept a user crystal. It requires a TTL clock input.

System compatibility: RADIUS, MATRIX-80/SDS

Operating temperature range: 0 to +50°C

ORDERING INFORMATION

For detailed ordering information refer to the Development System Products Ordering Guide.

PRELIMINARY

EPP-1 MK78229 EPROM PROGRAMMER

FEATURES

- ☐ Provides EPROM programming capability for RADIUS
- ☐ May be adapted for use with other computers
- ☐ Communicates with host via half-duplex RS232 or TTL serial link
- ☐ Programs, reads, and verifies most +5 V EPROMs available today
- ☐ 4 Selectable Baud rates: 300, 1200, 2400, 9600
- ☐ Emulates a subset of DATA I/O's System 19 command set
- ☐ Includes wall mount transformer power supply
- ☐ 8K x 8 bits of on-board RAM
- ☐ 28 pin zero-insertion-force socket for 24 and 28 pin EPROMs
- ☐ LED indicators for "programming" and "power on".
- ☐ High level commands for ease of use with RADIUS

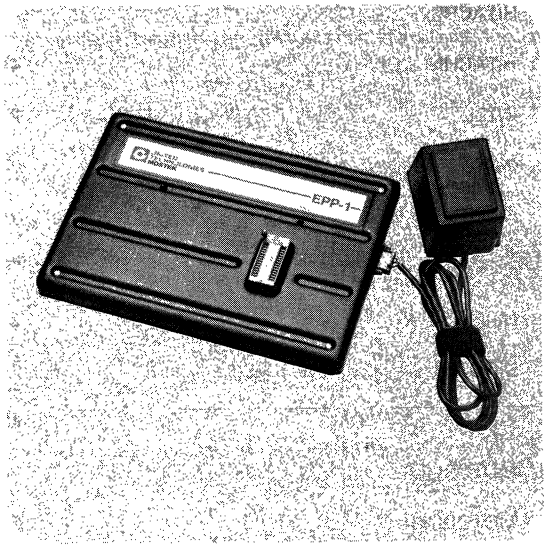
GENERAL DESCRIPTION

The EPP-1 is a microcomputer controlled MOS EPROM programmer capable of programming most MOS EPROMs currently available. It can be upgraded by adding a bipolar PROM to allow programming of new EPROMs when they become available.

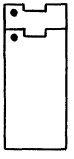
The EPP-1 is designed to be used with the RADIUS remote development station. The software for the RADIUS allows use of all the commands supported by EPP-1 and additional higher level commands for ease of use by the operator.

Communication with the host computer is via a serial link which can be RS232 or TTL compatible. Baud rates are selectable to 300, 1200, 2400 or 9600 Baud. The unit is powered by a wall mount transformer which provides unregulated DC voltages to the programmer.

EPP-1
Figure 1



LED indicators are provided to show when the power is on and when an EPROM is being programmed. A 28 pin zero-insertion-force socket is supplied for use with 24 and 28 pin EPROMs. 24 pin EPROMs are inserted with pin 1 of the EPROM in pin 3 of the 28 pin socket as shown below.



VII

EPROMs SUPPORTED

The following EPROMs may be programmed by the EPP-1.

MANUFACTURER	PART #	SIZE	FAMILY/PINOUT CONFIGURATION #
ADVANCED MICRO DEVICES	4716	2K x 8	1923
ELECTRONIC ARRAYS	2716	2K x 8	1923
FUJITSU	8516 (2716)	2K x 8	1923
HITACHI	46532	4K x 8	1925
HITACHI	46732	4K x 8	1924
INTEL	2758	1K x 8	1922
INTEL	2716	2K x 8	1923
INTEL	2732	4K x 8	1924
INTEL	2764	8K x 8	3533
MITSUBISHI	2716	2K x 8	1923
MOSTEK	2716	2K x 8	1923
MOTOROLA	MCM2716	2K x 8	1923
MOTOROLA	2532	4K x 8	1925
MOTOROLA	68764	8K x 8	6424
NATIONAL SEMICONDUCTOR	2716	2K x 8	1923
NATIONAL SEMICONDUCTOR	2532	4K x 8	1925
NATIONAL SEMICONDUCTOR	2732	4K x 8	1924
NIPPON ELECTRIC	2716	2K x 8	1923
OKI	2716	2K x 8	1923
TEXAS INSTRUMENTS	2508	1K x 8	1922
TEXAS INSTRUMENTS	2516	2K x 8	1923
TEXAS INSTRUMENTS	2532	4K x 8	1925
TEXAS INSTRUMENTS	2564	8K x 8	3130
TOSHIBA	323	2K x 8	1923

SOFTWARE

The high level commands supported by the RADIUS software for EPP-1 are:

COMMAND	DESCRIPTION
BATCH 'filename'	Accept command input from a Host file
BIT	Illegal bit test on EPROM
BLANK	Check if EPROM is blank
COMPARE 'filename'	Compare data from Host to EPROM Programmer
DEVICE xxxx	Select the device address to be used for programming, verifying, or loading device data
DIRECT	Allows direct entry of commands to the EPROM programmer via the console. May be terminated with control-C.
FAMILY [xxxx]	Select/display the family/pinout
HELP [Command name]	Display a HELP description of all commands or of a specific command
INPUT 'filename'	Input data from Host to EPROM programmer
LOAD	Load EPROM data from the EPROM into RAM
LOG 'filename'	Log console activity to a Host file
MEMORY xxxx [xxxx]	Display or update EPROM programmer RAM
MOVE xxxx xxxx xxxx	Move a block of data in RAM
OFFSET xxxx	Select an offset to be added to input addresses and subtracted from output addresses
OUTPUT xxxx xxxx 'filename'	Output data from EPROM programmer to Host
*(pause [msg])	Pause while in batch mode; message can be displayed.
PROGRAM	Program EPROM device with data in RAM
QUIT	Exit the utility; return EPROM programmer to keyboard control
RAM xxxx	Select RAM address to be used for data transfer
SHUFFLE xxxx	Merge 2 blocks of RAM; complement of SPLIT
SIZE xxxx	Select the hex number of bytes to be transferred; must be selected after RAM command
SPLIT xxxx	Split even/odd numbered bytes into 2 blocks; complement of SHUFFLE
SUM	Calculate check-sum of programmer RAM
SWAP	Swap nibbles in every byte in RAM
TRANSPARENT	Allows RADIUS development system transparent communication to Host
VERIFY	Verify EPROM device with data in RAM

EPP-1 DIRECT COMMAND SUMMARY

CONTROL COMMANDS

RETURN		Execute a command
ESC		Abort a command

UTILITY COMMANDS

G	Software Configuration number	This command returns a 4-digit hex number representing the software configuration of the programmer.
(HHHH)<	Set Begin RAM	BLOCK LIMIT L1. Defines first RAM address (in HEX) to be used for data transfers. Also functions as the RAM source address in the RAM-RAM Block Move command.
(HHHH);	Set Block Size	BLOCK LIMIT L2. Sets number of bytes (in HEX) to be transferred. Must be set after the Set Begin RAM command is used.
(HHHH):	Set Begin Device	BLOCK LIMIT L3. Sets the first device address (in HEX) to be used in data transfers. Also functions as the destination address in the RAM-RAM Block Move Command.
S	Sum-Check	Causes programmer to calculate the check-sum of RAM data and output it to the computer.
F	Error-Status Inquiry	EPROM programmer returns a 32 bit error code.
X	Error-Code	EPROM programmer outputs Error Codes stored in scratchpad RAM and then clears them from memory.
H	No operation	This is a null command and always returns a prompt character (>).

DEVICE COMMANDS

T	Illegal Bit Test	Test for illegal bit in a device.
B	Blank Check	Check that no bits are programmed in a device.
[	Family and Pinout	EPROM programmer sends a 4-digit number (FFPP) where FF is the family code and PP is the pinout in effect.
(FFPP)@	Select Family and Pinout	A 2-digit family code (FF) and pinout code (PP) specifies programming of a particular device.
R	Respond	Programmer indicates status and outputs device word limit, byte size, and programming pulse polarity.
L	Load	Load device data into RAM.
P	Program	Program RAM data into device.
V	Verify	Verify device against RAM.

I/O COMMANDS

W	Set Address Offset	Sets the specified offset to be subtracted from all incoming addresses and added to all outgoing addresses.
I	Input	Input data from computer to RAM.
O	Output	Output data from RAM to computer.
C	Compare	Compare RAM data with data from computer.

EDITING COMMANDS

\	RAM-RAM Block Move	Initiates transfer of data from one block RAM to another. Block limits must first be set.

PROGRAMMER RESPONSES

>+RETURN + LINE FEED	Prompt character. Informs the computer that the EPROM programmer has successfully executed a command.
F+RETURN + LINE FEED	Fail character. Informs the computer that the EPROM programmer has failed to execute the last-entered command.
?+RETURN + LINE FEED	Question mark. Informs the computer that the EPROM programmer does not understand a command.

TECHNICAL SPECIFICATIONS

Dimensions

7.8 in (19.8 cm) x 10.8 in. (27.4 cm)
2.0 in. (5.1 cm) maximum thickness

ELECTRICAL SPECIFICATIONS

Serial Communication Link

RS232 or TTL compatible

Operating Temperature

20°C to 40°C

Power Supply Requirements

115 V AC @ 200 ma

ORDERING INFORMATION

Designator	Description	Part No.
EPP-1	EPROM PROGRAMMER w/wall mount transformer (US)	MK78229-0
EPP-1	EPROM PROGRAMMER w/in line transformer (international)	MK78299-1
	EPP-1 Technical Manual	4420379

MATRIX™-80/SDS MICROCOMPUTER DEVELOPMENT SYSTEM

INTRODUCTION

The Mostek MATRIX™ is a complete state-of-the-art, floppy disk-based computer. Not only does it provide all the necessary tools for software development, but it provides complete hardware/software debug through Mostek's AIM™ series of in-circuit emulation cards for the 68000, Z80, and the 3870 family of single-chip microcomputers. The MATRIX has at its heart the powerful OEM-80E (Single Board Computer), the RAM-80BE (RAM I/O add-on board), and the FLP-80E (floppy disk controller board). Because these boards and software are available separately to OEM users, the MATRIX serves as an excellent test bed for developing systems applications.

The disk-based system eliminates the need for other mass storage media and provides ease of interface to any peripheral normally used with computers. The file-based structure for storage and retrieval consolidates the data base and provides a reliable portable media to speed and facilitate software development.

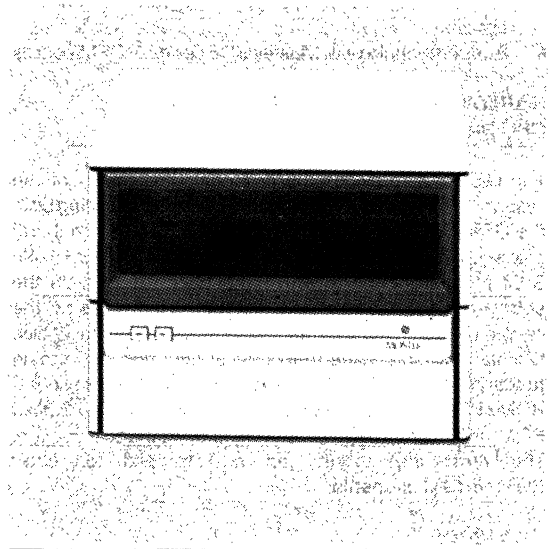
Development System Features

The MATRIX is an excellent integration of both hardware and software development tools for use throughout the complete system design and development phase. Debug can then proceed inside the MATRIX domain using its resources as if they were in the final system. Using combinations of the Monitor, Designer's Debugging Tool, execution time breakpoints, and single step/multistep operation along with a formatted memory dump, provides control for attacking those tough problems. The use of the Mostek AIM™ options provides extended debug with versatile hardware breakpoints on memory or port locations, a buffered in-circuit emulation cable for extending the software debug into its own natural hardware environment.

Package System Features

From a system standpoint, the MATRIX has been designed to be the basis of an end-product, such as a small business/industrial computer. Other hardware options are available, with even more to be added. Expansion of the disk drive units to a total of four single-sided or double-sided units provides up to two megabytes of storage. This computer uses the third-generation Z80 processor supported with the power of a complete family of peripheral chips. Through the use of its 158 instructions, including 16-bit arithmetic, bit manipulation, advanced block moves and interrupt handling, almost any application from communication concentrators to general purpose accounting systems is made easy.

MATRIX™-80/SDS
Figure 1



OEM Features

The hardware and software basis for the MATRIX is also available separately to the OEM purchaser. Through a software licensing agreement, all Mostek software can be utilized on these OEM series of cards.

MATRIX RESIDENT FIRMWARE (DDT-80)

The Designer's Debugging Tool consists of commands for facilitating an otherwise difficult debugging process. The MATRIX allows rapid source changes through the editor and assembler. This is followed by DDT operations which close the loop on the debug cycle. The DDT commands include:

Memory	- display, update, or tabulate memory
Port	- display, update or tabulate I/O ports
Execute	- execute user's program
Hexadecimal	- performs 16 bit add/sub
Copy	- copy one block to another

VII

MATRIX SYSTEM SPECIFICATIONS

- Z80 CPU
- 4K-byte PROM bootstrap and Z80 debugger
- 60K bytes user RAM (56K contiguous)
- 8 x 8 bit I/O ports (4 x PIO) with user-definable drivers/receivers
- Serial port, RS 232 and 20 mA current loop
- 4 channel counter/timer (CTC)
- 2 single-density, single-sided disk drives; 250K bytes per floppy disk
- 3 positions for AIM modules, Serial Interface, etc.
- PROM programmer I/O port. Programmer itself is optional.
- Bus compatible with Mostek SDE series of OEM boards

HARDWARE DESCRIPTION OEM-80E
CPU Module

The OEM-80E provides the essential CPU power of the system. While using the Z80 as the central processing unit, the OEM-80E is provided with other Z80 family peripheral chip support. Two Z80 PIO's give 4 completely programmable 8 bit parallel I/O ports with handshake from which the standard system peripherals are interfaced. Also on the card is the Z80-CTC counter timer circuit which has 3 free flexible channels to perform critical counting and timing functions. Along with 16K of RAM, the OEM-80E provides 5 ROM/PROM sockets which can be utilized for 10/20K of ROM or 5/10K PROM. Four sockets contain the firmware. The remaining socket can be strapped for other ROM/PROM elements.

RAM-80BE

The RAM-80BE adds additional memory with Mostek's MK4116 16K dynamic memory along with more I/O. These two fully programmable 8-bit I/O ports with handshake provide additional I/O expansion as system RAM memory needs to grow. Standard system configuration is 48K bytes for a system total of 60K bytes user RAM (56K contiguous).

FLP-80E

Integral to the MATRIX system is the floppy disk controller. The FLP-80E is a complete IBM 3740 single-density/double-sided controller for up to 4 drives. The controller has 128 bytes of FIFO buffer resulting in a completely interruptable disk system.

OPTIONAL MODULES COMPATIBLE WITH MATRIX

AIM-68000 (10 MHz max. clock rate)

The AIM-68000 is an advanced development tool which provides project debug capabilities for both hardware and software via in-circuit emulation of the MK68000 Microprocessor. Real-time emulation is provided up to 10 MHz operation. Flexible breakpoints and Single-Step emulation with Invisible Break on Register Contents are provided. Symbolic addressing and an extensive HELP Facility ease the use of AIM-68000.

AIM-Z80BE (6.0 MHz max. clock rate)

The AIM-Z80BE is an improved Z80 In-Circuit-Emulation module usable at Z80-CPU clock rates of up to 6MHz. The AIM-Z80BE is a two processor solution to In-Circuit Emulation which utilizes a Z80-CPU in the buffer box for accurate emulation at high clock rates with minimum restrictions on the target system. The AIM-Z80BE provides real time emulation (no WAIT states) while providing full access to RESET, NMI and INT control lines. Eight single byte software breakpoints (in RAM) are provided as well as one hardware trap (RAM or ROM). The emulation RAM on the AIM-Z80BE is mappable into the target system in 256 byte increments. A 1024 word x 48 bit history memory is triggerable by the hardware intercept and can be read back to the terminal to provide a formated display of the Z80-CPU address, data, and control busses during the execution of the program under test. Several trigger options are available to condition the loading of the history memory.

AIM-7XE

The AIM-7XE module provides debug and in-circuit emulation capabilities for the 3870 series microcomputers on the MATRIX. Multiple-breakpoint capability and single-step operation allow the designer complete control over the execution of the 3870 Series microcomputer.

Register, Port display, and modification capability provide information needed to find system "bugs." All I/O is in the user's system and is connected to AIM-7X by a 40-pin interface cable.

The debugging operation is controlled by a mnemonic debugger which controls the interaction between the Z80 host computer and the 3870 slave. It includes a history module for the last 1024 CPU cycles and also supports all 3870 family circuits.

DCC-80E

The DCC-80E multi-channel serial controller board was developed as a general purpose four port serial I/O card. DCC-80E can be user configured to interconnect computer systems and will support SDLC and BYSINC protocols.

Assembly and linking are done using cross products supplied by Mostek or other vendors.

MECHANICAL SPECIFICATIONS

Overall Dimensions:

CPU subsystem	- 8" High x 21" wide x 22" deep (20.3 cm x 53.3 cm x 55.8 cm)
Disk Subsystem	- 8" High x 21" wide x 22" deep (20.3 cm x 53.3 cm x 55.8 cm)

Humidity: up to 90% relative, noncondensing.

Material: Structural Foam (Noryl)

Weight: CPU Subsystem 25 lbs (11.3 Kg)
Disk Subsystem 50 lbs (22.7 Kg)

Fan Capacity: 115 CFM

Card Cage: Six slots DIN 41612 type connectors

Operating Temperature: +10°C to +35°C

ELECTRICAL SPECIFICATIONS

INPUT 100/115/230 volts AC ± 10%
50 Hz (MK78189) or 60 Hz (MK78188)

OUTPUT

CPU subsystem	+5 VDC at 12A max.
	+12 VDC at 1.7A max.
	-12 VDC at 1.7A max.
Disk subsystem	+5 VDC at 3.0A max.
	-5 VDC at 0.5A max.
	+24 VDC at 3.4A max.

ORDERING INFORMATION

See Development System Products ordering guide.

PERIPHERALS AND CABLES

NAME	DESCRIPTION	PART NO.
PPG-8/16	Programmer for 2708, 2758 and 2716 PROM Includes interfacing cables to MATRIX.	MK79081-1
SD-WW	Wire wrap card compatible with MATRIX.	MK79063
SD-EXT	Extender card compatible with MATRIX.	MK79062
LP-CABLE	Interface cable from MATRIX Microcomputer to Centronics 306 or 702 printer	MK79089
PPG-CABLE	Interface cables from MATRIX to PPG-8/16 PROM programmer (MK79081).	MK79090

EVAL-70
3870 EVALUATION SYSTEM

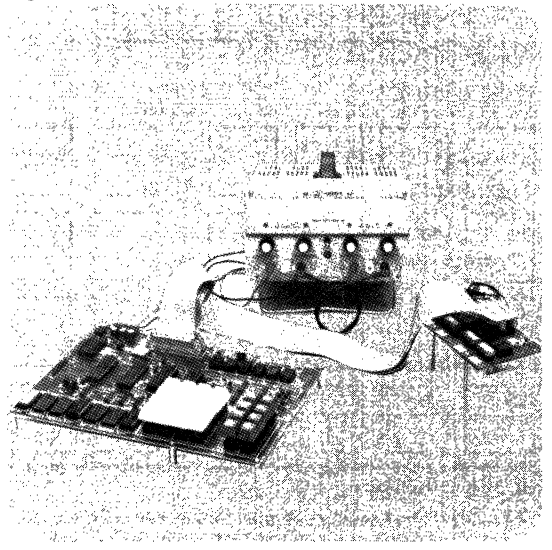
FEATURES

- An ideal hardware and/or software design aid for the MK38P70 and MK3870 family of Single-Chip Microcomputers
- Includes a 2K byte firmware monitor
- Keypad for command and data entry
- 7-segment address and data display
- Programming socket for MK2716/2758's
- Crystal controlled system clock
- 2K bytes of MK4118 static RAM (up to 4K optional)
- Sockets for up to 4K bytes of MK2716 PROM's
- Flexible memory map strapping options
- Current loop or RS-232 serial loader optional (110-300-1200 baud)
- 3 general purpose timer/counters
- 3 general purpose external interrupts
- Easy to use - requires only two supplies for normal operation (+5, +12)
- Ideal for evaluation of MK3870 family single-chip microcomputers
- Full in-circuit emulation of MK3870 single-chip microcomputer family.

DESCRIPTION

EVAL-70 is a single board computer with on-board keypad, address and data displays, and 2716 PROM programmer. EVAL-70 is designed to be an easy-to-use introduction to the industry standard MK3870 family of single-chip computers. Programs can be written and debugged in RAM using the powerful DDT-70 operating system. The 40 pin AIM cable can be used to perform real-time emulation of the MK3870 family of devices. After debugging, programs can be loaded into MK2716's for final circuit checkout (and emulation).

EVAL-70
Figure 1



USING EVAL-70

The photograph above shows how EVAL-70 is used as a program development tool. Only an external power supply is required for operation of EVAL-70; the built-in keyboard and display offer all the functions needed to design, develop, and debug programs for the MK3870 family of single-chip microcomputers at the machine code level.

COMMAND SUMMARY

DM:	Display memory: allows memory to be displayed and (RAM) updated.
DR:	Display registers: allows the user's register values to be displayed and updated.
DP:	Display ports: allows the contents of ports 0 thru F to be displayed and updated
HX:	Hex calculator: allows hexadecimal arithmetic calculations to be performed (add and subtract)
GO:	causes execution of a user program at a specified address

BK: Breakpoint: allows a breakpoint to be set or reset

ST: Step: causes single-step execution of a user program at a specified address

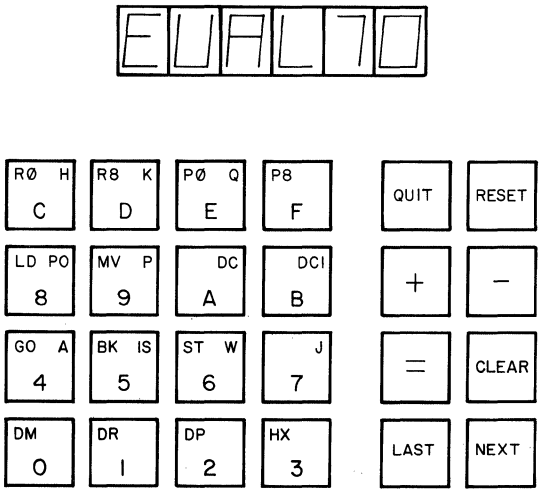
LD: Load: initiates the serial loader (optional)

MV: Move: allows a block of memory to be moved or copied from one space to another

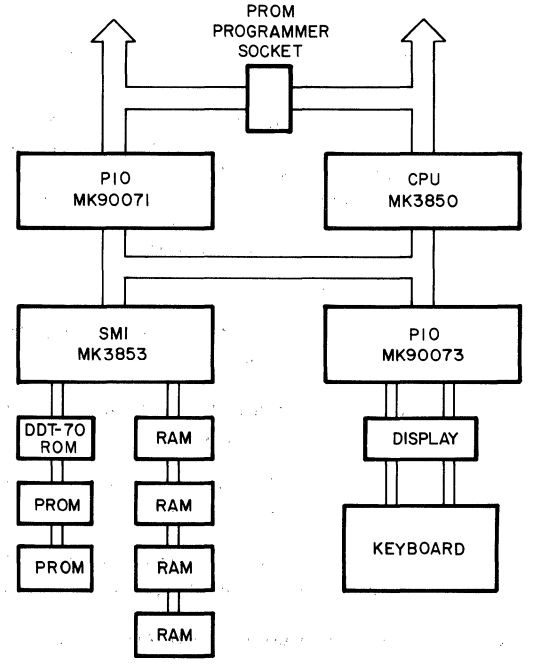
RO, R8: Read PROM: causes the PROM programmer socket to be read into address space 00-7FF or 800-F7F

PO, P8: Program PROM: causes the contents of address space 000-7FF or 800-F7F to be programmed into the PROM programmer socket

EVAL-70 KEYBOARD DRAWING



BLOCK DIAGRAM



BLOCK DIAGRAM

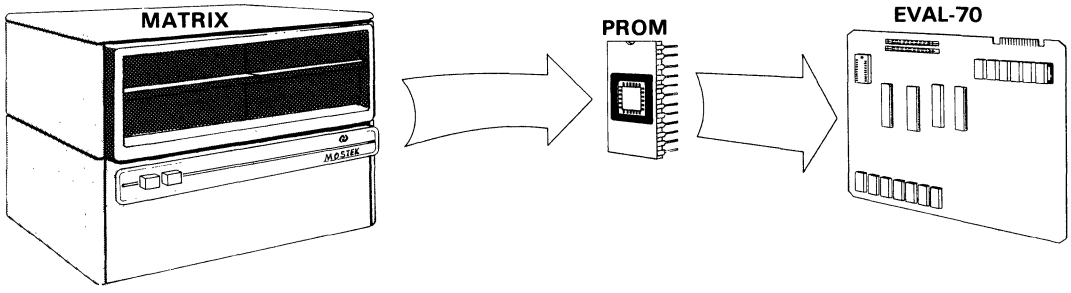
EVAL-70 uses several members of the F8 multichip family. A MK3850 Central Processing Unit (CPU) provides the ALU, registers, system control and two 8-bit ports. A MK90071 Peripheral Input Output chip (PIO) provides two more 8-bit ports plus a flexible timer/interrupt control block. These four ports are connected to the AIM cable connector for in-circuit emulation of the MK3870 family devices, and also to the PROM programmer socket. An additional PIO (MK90073) interfaces the LED display and keyboard. A MK3853 Static Memory Interface chip (SMI) interfaces the operating system ROM, up to two 2K PROMs and up to four 1K RAMs. A switch option allows either the 4K of PROM or the 4K of RAM to appear at address 0000H, with the other 4K appearing at 1000H. The operating system ROM may be up to 8K (currently 2K) starting at 8000H. A switch option allows reset to either 0000H or to the 8000H ROM.

USING EVAL-70 WITH LARGER SYSTEMS

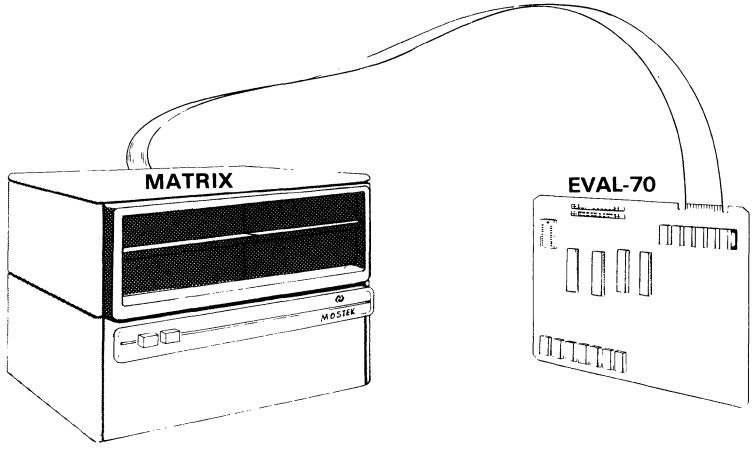
Although the EVAL-70 operating system (DDT-70) was designed to make program machine code entry simple and quick, many users will find it more efficient to assemble their programs on a larger computer and then download to EVAL-70.

The download to EVAL-70 may be accomplished in either of two ways:

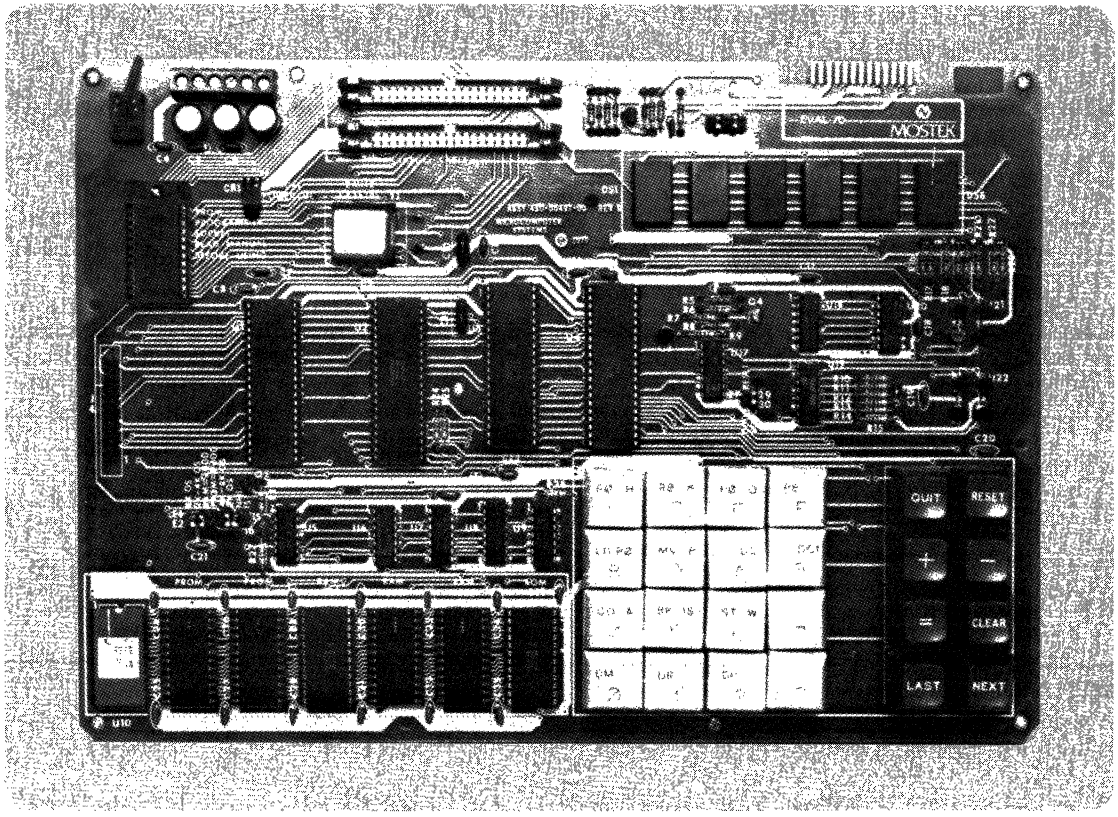
1) A PROM may be programmed on the Development System, and then read into RAM by the EVAL-70 for debugging.
2) A direct connection may be made between a serial port on the Development System and the serial loader port on EVAL-70. An optional serial loader program is provided in the EVAL-70 Operations Manual.



DEVELOPMENT SYSTEM



EVAL-70 BOARD



SPECIFICATIONS

Operating Temperature: 0°C - 50°C

Power Supplies Required: +5VDC ±5% 1.0A max
+12VDC ±5% 0.1A max
+25VDC ±5% 0.1A max

Board Size: 8.5 in. (21.6 cm) x 12 in. (30.5cm) x 2 in. (5cm)

Connectors and Cables: 40 pin in-circuit-emulation cable is provided.

ORDERING INFORMATION

See Development System Products ordering guide.

PPG8/16C PROM PROGRAMMER

FEATURES

- ☐ Programs, reads, and verifies 2708-, 2758-, and 2716-type PROMs (2758 and 2716 PROMS must be 5-Volt only type)
- ☐ Interfaces to MATRIX and MDX-PIO
- ☐ Driver software included on system diskette for M/OS-80
- ☐ Zero-insertion-force socket
- ☐ Power and programming indicators

DESCRIPTION

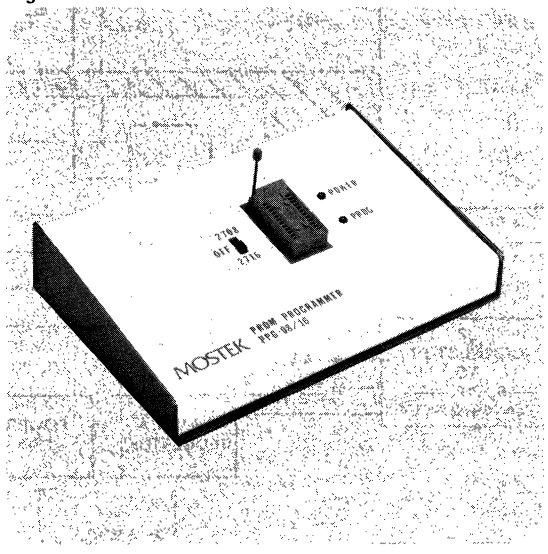
The PPG-8/16C PROM Programmer is a peripheral which provides a low-cost means of programming 2708, 2758, or 2716 PROMs. It is compatible with Mostek's MATRIX Microcomputer Development System and the MDX-PIO. The PPG-8/16C has a generalized computer interface (two 8-bit I/O ports) allowing it to be controlled by other types of host computers with user-generated driver software. A complete set of documentation is provided with the PPG-8/16C which describes the internal operation and details user's operating procedures

The PPG-8/16C is available in a metal enclosure for use with the MATRIX™ and the MDX-PIO. Interface cables for either the MATRIX or MDX-PIO must be purchased separately.

SOFTWARE DESCRIPTION

The driver software accomplishes five basic operations.

PPG 8/16C
Figure 1

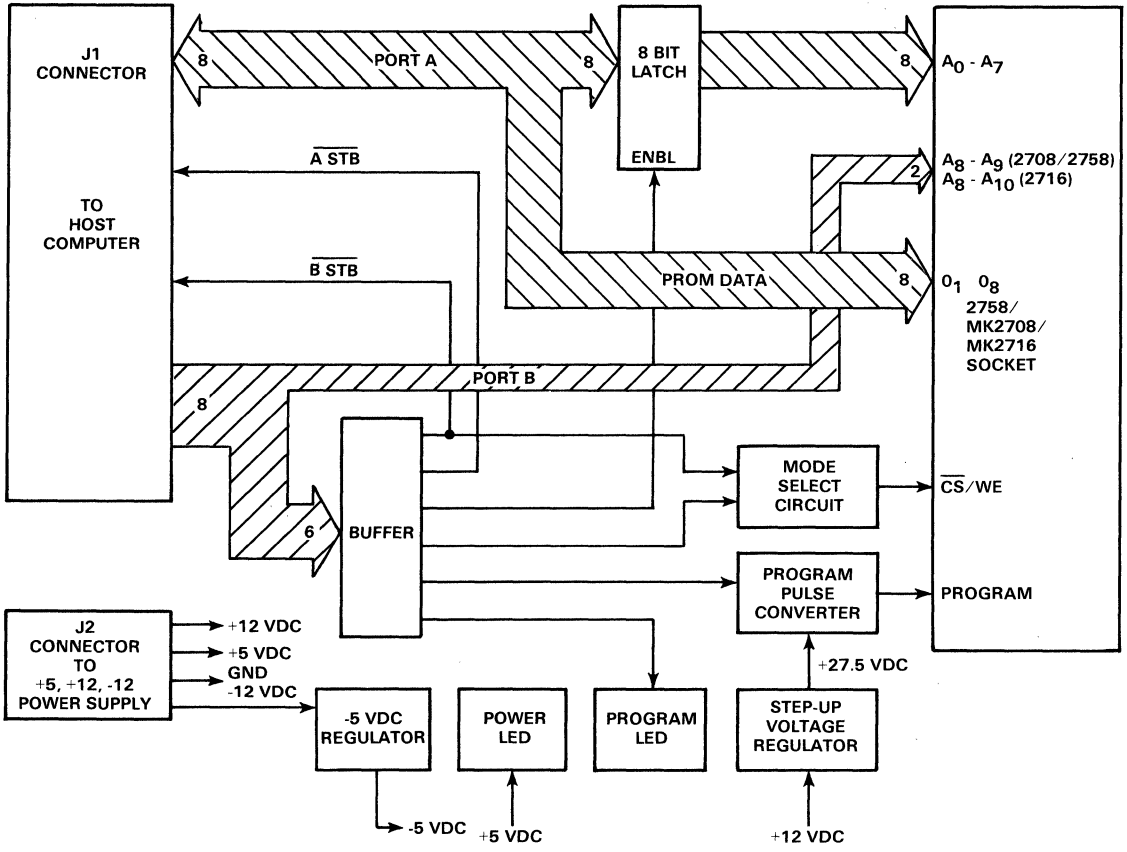


These are (1) loading data into host computer memory, (2) reading the contents of a PROM into host computer memory, (3) programming a PROM from the contents of the host computer memory, (4) verifying the contents of a PROM with the contents of the host computer memory, and (5) display and update of the host computer memory.

The driver software is provided on the M/OS-80 system diskette. The user documentation provided with the PPG-8/16C fully explains programming procedures to enable a user to develop a software driver on a different host computer.

VII

PPG 8/16C BLOCK DIAGRAM
Figure 2



INTERFACE

25-pin control connector (D type)
40-pin control connector (0.1-in. centers card edge)
for AID-80F, SDB-80, SDB-50/70, or MATRIX™
12-pin power connector (0.156-in. centers card edge)
All control signals are TTL-compatible

POWER REQUIREMENTS

+12 VDC at 250mA typical
+5 VDC at 100mA typical
–12 VDC at 50mA typical

ORDERING INFORMATION

See Development System Products ordering guide.

OPERATING TEMPERATURE

0°C –60°C

PROGRAMMING TIME

2708 - 2.5 minutes
2758 - 0.9 minutes
2716 - 1.8 minutes

RADIUS - Remote Development Station

RADIUS is a hardware/software development station that connects to a host computer. When you order a RADIUS, you must specify the operating voltage characteristics. The host software must be ordered separately (as described in the next section).

DESCRIPTION	ORDER
RADIUS for 60 Hz, 115 VAC Operation	MK78213
RADIUS for 50 Hz, 230 VAC Operation	MK78214

RADIUS HOST SOFTWARE

RADIUS host software is provided on a variety of media depending on host environment. When you order please specify one of the following.

DESCRIPTION	ORDER
M/OS Version - implemented for M/OS-80 and CP/M supplied on single-sided, single-density, 8-inch floppy diskette.	MK78224-11
RSX Version - implemented for RSX-11M V3.2 supplied on DEC DOS-11 format 9-track magnetic tape, 800 BPI. Host must have a FORTRAN IV (ANSI-66) compiler.	MK78224-33
VMS Version - implemeted for VMS V2.3 supplied on DEC DOS-11 format 9-track magnetic tape, 800 BPI. Host must have a FORTRAN IV (ANSI-66) compiler.	MK78224-34
Rehostable Version - supplied in source form. Host must have a FORTRAN IV (ANSI-66) compiler. Supplied on ASCII 9-track magnetic tape, 800 BPI, blocked in 80-character records.	MK78224-45

MATRIX - Microcomputer Development System

MATRIX is a stand-alone, floppy disk-based development system. It is supplied with FLP-80DOS, an editor, an assembler, and a linker. When you order a MATRIX, you must specify the operating voltage characteristics.

DESCRIPTION	ORDER
MATRIX for 60 Hz, 115 VAC operation	MK78188
MATRIX for 50 Hz, 230 VAC operation	MK78189

AIM-7XE (Application Interface Module for 387X)

AIM-7XE is the in-circuit-emulator for the 387X family. It will function in both RADIUS and MATRIX. When AIM-7XE is ordered, a personality module must also be ordered. This personality module provides emulation for the 3870 or 3873 family.

In addition, the AIM-7X software must be ordered separately (as described in next section).

DESCRIPTION	ORDER
AIM-7XE - control board and history board for 387X families.	MK79094
APM-70 - personality module for 3870 family	MK79093
APM-73 - personality module for 3873 family	MK79092

AIM-7X (Software for AIM 7XE)

The following software configurations are available for use with AIM 7XE. Please specify one of the following when ordering.

DESCRIPTION	ORDER
FLP-80DOS Version - configured for use with MATRIX. Supplied on single-sided, single-density, 8-inch floppy diskette.	MK78225-22
M/OS-80 Version - configured for use with M/OS-80 and CP/M host and RADIUS. Supplied on single-sided, single-density, 8-inch floppy diskette.	MK78225-10
RSX and VMS Version - configured for use with RSX-11M V3.2 and VMS V2.3 host and RADIUS. Supplied on DEC DOS-11 format 9-track magnetic tape, 800 BPI.	MK78225-30
ASCII Version - configured for use with general host and RADIUS. Supplied on ASCII 9-track magnetic tape, 800 BPI.	MK78225-40
M/OS-80 Version - configured for use with MATRIX. Supplied on single-sided, single-density, 8-inch floppy diskette.	MK78225-11

AIM-Z80AE/AIM-Z80BE (Application Interface Modules for Z80)

AIM-Z80AE and AIM-Z80BE are the in-circuit-emulators for the Z80. They will function in both RADIUS and MATRIX. When either of the two is ordered, the AIM-Z80 software must be ordered separately (as described in the next section).

DESCRIPTION	ORDER
AIM-Z80AE - In-circuit-emulator for 2.5 and 4 MHz Z80. Provides 32K emulation RAM	MK78181-4
AIM-Z80BE - In-circuit-emulator for 2.5, 4, and 6 MHz Z80. Provides 16K emulation RAM	MK78204

AIM-Z80 (Software for AIM-Z80AE/AIM-Z80BE)

The following software configurations are available for use with AIM-Z80AE or AIM-Z80BE. Please specify one of the following when ordering.

DESCRIPTION	ORDER
FLP-80DOS Version - configured for use with MATRIX. Supplied on single-sided, single-density, 8-inch floppy diskette.	MK78226-22
M/OS-80 Version - configured for use with M/OS-80 and CP/M host and RADIUS. Supplied on single-sided, single-density, 8-inch floppy diskette.	MK78226-10
RSX and VMS Version - configured for use with RSX-11M V3.2 and VMS V2.3 host and RADIUS. Supplied on DEC DOS-11 format 9-track Magnetic tape, 800 BPI.	MK78226-30
ASCII Version - configured for use with general host and RADIUS. Supplied on ASCII 9-track magnetic tape, 800 BPI.	MK78226-40
M/OS-80 Version - configured for use with MATRIX. Supplied on single-sided, single-density, 8-inch floppy diskette.	MK78226-11

AIM-68000 (Application Interface Module for 68000)

AIM-68000 is the in-circuit-emulator for the 68000. It will function in both RADIUS and MATRIX. When AIM-68000 is ordered, the AIM-68000 software must be ordered separately (as described in the next section).

DESCRIPTION	ORDER
AIM-68000 - In-ciruit-emulator for up to 10 MHz 68000. Includes two (2) control boards and a buffer box/cable assembly.	MK78228

AIM-68000 (Software for AIM-68000)

The following software configurations are available for use with AIM-68000. Please specify one of the following when ordering.

DESCRIPTION	ORDER
RSX and VMS Version - configured for use with RSX-11M V3.2 and VMS V2.3 host and RADIUS. Supplied on DEC DOS-11 format 9-track magnetic tape, 800 BPI.	MK78232-30
ASCII Version - configured for use with general host and RADIUS. Supplied on ASCII 9-track magnetic tape, 800 BPI.	MK78232-40

PPG-8/16C (EPROM Programmer)

PPG-8/16C is a programmer for use with MATRIX. It includes interface cable to MATRIX and FLP-80DOS compatible driver (on floppy diskette).

DESCRIPTION	ORDER
PPG-8/16C EPROM programmer	MK79081-1

EVAL-70

EVAL-70 is a 3870 family evaluation system. It includes an in-circuit-emulation cable.

DESCRIPTION	ORDER
EVAL-70	MK79086

SD/SDE ADAPTER

This board adapts SDE form factor boards to previous systems using SD form factor boards. This allows current AIM's to be used with the AID-80F system.

DESCRIPTION	ORDER
SD/SDE ADAPTER	MK79095

1983 COMPUTER PRODUCTS DATA BOOK

VIII Application Notes VIII

APPLICATION NOTE #1 INTERFACING MOSTEK'S MDX-PIO TO OPTO-22'S PB24

INTRODUCTION

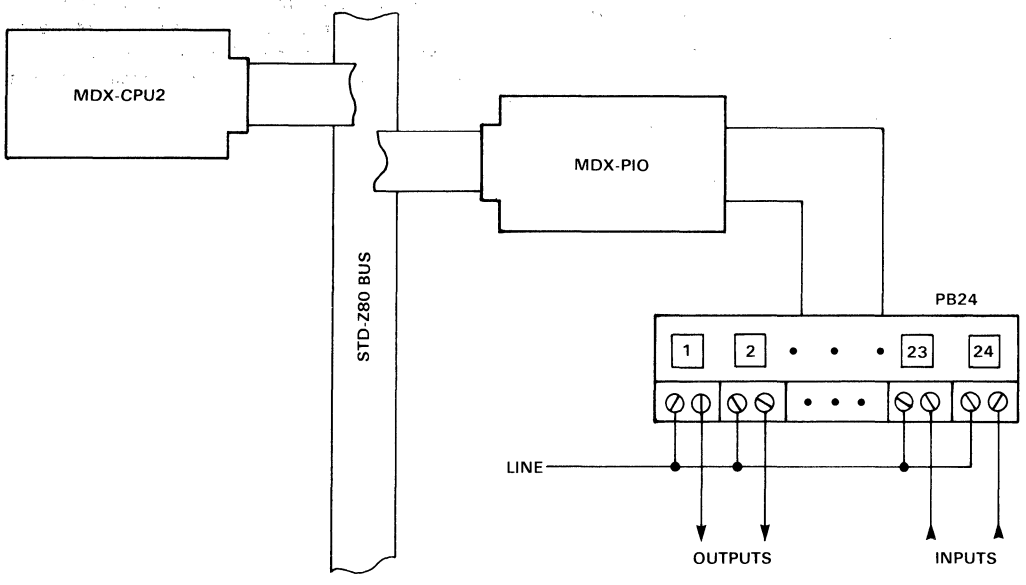
The impact of the microprocessor has, at least, been overwhelming. As consumers, most of us would be hard pressed to find any appliance that doesn't have some type of microprocessor contained within. In the area of instrumentation the microprocessor has brought about the development of a new generation of "smart" instruments.

Even though the areas of instrumentation and consumer products have provided great in-roads for the microprocessor, its utilization is still limited by the "real-world" interfaces through which the microprocessor must communicate. These interfaces must handle such things as current and voltage levels which would be destructive to the MOS circuitry contained within the IC package. The advent of the solid-state optically-isolated relay has lessened the impact of these "real-world" interface problems. It is with this in mind that this application note will show how to interface a microcomputer system (based upon Mostek's MD-SERIES) to an OPTO-22 PB24 which is a 24-channel I/O panel utilizing Opto 22's family of solid-state relays.

SYSTEM CONSIDERATIONS

In general, when controlling voltages in excess of 5 volts and currents in excess of 50 milliamps, devices other than ICs must be used. The solid state relay has provided the system designer with the perfect interface between the low current, low voltage world of the microprocessor and that of the real world. These relays come in many different sizes and specifications with regards to voltage and current. For this application note, we will be dealing with the plug-in modules offered by such manufacturers as Opto-22, Gordos, and Guardian. These modules come in both AC and DC versions with inputs and outputs available in each type. In general, these modules are capable of controlling up to 3 amps at their respective voltage ratings. This fact serves to limit the applications of these devices to low power direct control or high power indirect control through the use of higher power relays. Figure 1 shows a block diagram of this system.

Figure 1



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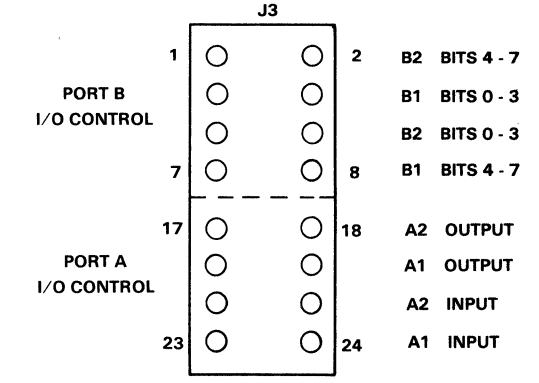
HARDWARE CONSIDERATIONS

As mentioned above, this particular application will make use of the MDX-PIO for the parallel interface between the microcomputer and the opto panel. In order to utilize this board the user must be aware of the many options available. This particular board is based upon the Z80-PIO peripheral chip. It is beyond the scope of this application note to go into great detail about this chip. For those readers wishing to gain more knowledge about this chip, please refer to the 1981 Z80 Microcomputer Data Book.

For the type of operation that the opto panel is generally used, the data is handled as discrete bits. With this in mind, we will use the MDX-PIO in the bit-control mode. For more detail on this board, consult the MDX-PIO Operations Manual. When operating in this mode, the board can be configured such that I/O bits are assigned in four bit groups; all bits within a given group must be either inputs or outputs. This comes about owing to the type of interface chips used on the MDX-PIO. The user must be aware of this when it comes time to configure the opto panel. Port bits are assigned as either input or output by strapping the PIO accordingly. Figure 2 summarizes the various I/O straps for the PIO. The installation of a strap selects the corresponding bits as outputs unless otherwise noted. Note that port B can be strapped as two four bit quantities while port A must be strapped as an eight bit quantity. To improve flexibility, the cable assignments in Tables 1 and 2 provide for the first 16 channels to be assigned to Port B1 and B2. Channels 17-24 are split between Port A1 and A2. In order for the software to use positive logic to activate the opto modules, the buffer chips on the PIO should be the inverting type. For channel A, 74LS240 devices should be used and for channel B, 74LS242 devices should be used.

Figure 2



The address assignment of the PIO is not critical owing to its having "ported" I/O as opposed to "memory-mapped" I/O. For this application note, the sample software routine expects the PIO to reside at I/O location 80 hex. To accomplish this assignment, simply strap the following pins on J4: 3-4, 5-6, 7-8, and 9-10.

SOFTWARE CONSIDERATIONS

There are two basic operations which are accomplished in software: programming the PIO and controlling the opto panel. Figure 3 is a source listing for the demonstration program. For details concerning the programming of the PIO, consult the Z80-PIO section of the Z80 Microcomputer Data Book. The software routine provided with this application note runs the PIO as a polled device rather than interrupt-driven. The assignment of I/O bits is dependent upon the application. In this case, four bits are assigned as inputs and four as outputs.

All that is necessary to program the PIO is the selection of bit control mode and assignment of I/O bits. Once programmed, the interraction between the application software and the physical devices which are being controlled is simply a matter of doing I/O instructions to I/O port 80H. A "1" in one of the input bits indicates that the device has been turned on. One nice feature of the PIO is that the software can read back the state of the output bits. This feature provides for storage of the state of the output bits.

A PARTIAL BASIC ROUTINE TO CONTROL THE OPTO PANEL

Figure 3

```
•
•
•
COMMENT: MASK CONTAINS THE 3 I/O MASKS; PORT = 80H
        FOR I = 1 TO 3
        OUT (2I + 127), 255
        OUT (2I + 127), MASK (I)
        NEXT I
•
•
•
        OUT PORT, DATA
        A = INP (PORT)
•
•
```

PINOUT ASSIGNMENTS FROM PIO-J1 TO PB24

Table 1

PIO PINOUT		PB24 PINOUT	
J1-1	ARDY		
J1-2	ASTB		
J1-3	A7		
J1-4	A5		
J1-5	A3	9	CHANNEL 19
J1-6	A1	13	CHANNEL 17
J1-7	B0	47	CHANNEL 0
J1-8	B2	43	CHANNEL 2
J1-9	B4	39	CHANNEL 4
J1-10	B6	35	CHANNEL 6
J1-11	BSTB		
J1-12	BRDY		
J1-13	N/C		
J1-14	GND		
J1-15	GND		
J1-16	A6		
J1-17	A4		
J1-18	A2	11	CHANNEL 18
J1-19	A0	15	CHANNEL 16
J1-20	B1	45	CHANNEL 1
J1-21	B3	41	CHANNEL 3
J1-22	B5	37	CHANNEL 5
J1-23	B7	33	CHANNEL 7
J1-24	GND		
J1-25	GND		
J1-26	N/C		

PINOUT ASSIGNMENTS
FROM PIO-J2 TO PB24
Table 2

PIO PINOUT		PB24 PINOUT	
J2-1	ARDY		
J2-2	ASTB		
J2-3	A7		
J2-4	A5		
J2-5	A3	1	CHANNEL 23
J2-6	A1	5	CHANNEL 21
J2-7	B0	31	CHANNEL 8
J2-8	B2	27	CHANNEL 10
J2-9	B4	23	CHANNEL 12
J2-10	B6	19	CHANNEL 14
J2-11	BSTB		
J2-12	BRDY		
J2-13	N/C		
J2-14	GND		
J2-15	GND		
J2-16	A6		
J2-17	A4		
J2-18	A2	1	CHANNEL 22
J2-19	A0	7	CHANNEL 20
J2-20	B1	29	CHANNEL 9
J2-21	B3	25	CHANNEL 11
J2-22	B5	21	CHANNEL 13
J2-23	B7	17	CHANNEL 15
J2-24	GND		
J2-25	GND		
J2-26	N/C		

MDX-RMC12/MD-RMC12-50 APPLICATION NOTE #2

INTRODUCTION

The MD-RMC12 is a subsystem enclosure for the successful STD BUS line offered by Mostek and several other vendors. The subsystem has a power supply, a fan, a 12-slot card cage, and is packaged in a 19-inch rack-mountable frame.

This application brief will detail the components for the cables that might be used and gives suggestions that might help improve the product's value to the user.

CABLES

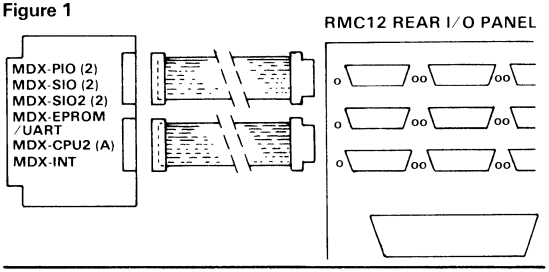
The rear I/O panel was provided for the convenience of the user. No cables are provided with the MD-RMC12 because of the diverse needs of the end user, but here are some recommended components and suggested cables to help configure a system.

MDX-PIO, MDX-SIO2, MDX-CPU2, and MDX-EPROM/UART (DEBUG)

A typical interface cable from a Mostek module to the back of the I/O connector panel is described in the following text. See Figure 1. The cable will be the interface for Mostek's MDX-EPROM/UART module, MDX-PIO, MDX-CPU2 or serial modules MDX-SIO, and MDX-SIO2; however, the cable will accommodate all of Mostek's modules that have a 26-pin header for the I/O connector.

CABLE INTERFACE

Figure 1

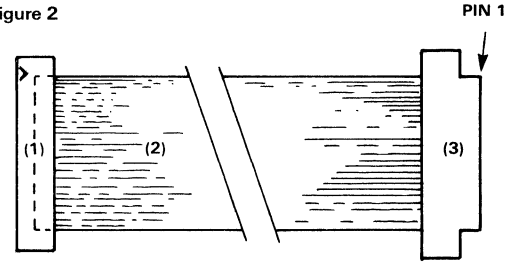


Note: This method provides direct one-to-one pinout of MDX module signal wiring. Any scrambling which may be required to suit a particular application should be done with multi-conductor discrete wire; i.e. Beldon 8459 (25-conductor; 22 AWG.)

1. The mating connector for the 26-pin header, on the I/O modules, is a mass-terminated type connector, like T&B Ansley 609-2601-01, Winchester Electronic's #51-1126-01 or 3M's #3399-6026. The header is then pressed on the cable. Pressing the header on the cable can be accomplished with the manufacturer's suggested presses. A bench vise, if used with care, can also be used. Note that pin 1 of the header connector is the pin marked by the arrow on the housing. See Figure 2.

CABLE ASSEMBLY

Figure 2



2. 24 inches of 26-conductor flat-ribbon cable: T&B Ansley's #171-26, Winchester Electronic's #55-2628-10/11 or 3M's #3365/26.

3. A 25-pin D-type socket connector, (T&B Ansley part #609-25S, or Winchester Electronic's #49-1125S), should be attached to the I/O panel with the socket-jack assembly with #4 lock washer and #4-40 hex nut, (T&B Ansley 609-003 or Winchester Electronic's 49-603-S) or #4 screws and nuts. The suggested method is the socket-jack assembly.

The D connector has 25 pins, and the flat ribbon cable has 26 conductors; therefore, the cable needs to have the last conductor (header pin 26) trimmed back approximately a half-inch to allow for pressing. This conductor isn't used by Mostek's I/O modules. The D-type connector is then pressed on the corrected end of the cable, making sure pin 1 of the D-type connector end matches pin 1 of the header end. The I/O panel position selected is up to the user, but to make it compatible with other Mostek MATRIX-80 systems, J3 is the suggested slot for the RS-232C (MDX-EPROM/UART, SIO, and SIO2 modules) interconnect. The printer position defined by Mostek is J1 and J2 is the PROM programmer position.

PRINTER, PROM PROGRAMMING

When a printer is going to be used with the RMC12 subsystem the interface cable will depend on what type of

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interface the printer has: parallel Centronics type or RS-232 serial type.

The parallel interface uses the MDX-PIO and an internal cable described in the preceding text (Figure 2). The external cable is detailed in Table 2.

When a serial interface is going to be used, a MDX-SIO or MDX-SIO2, the same internal cable as described in Figure 2 of the previous text is used. The external cable is the same as the CRT cable discussed later in the text and is detailed in Table 4.

The PPG 8/16 uses the MDX-PIO as the interface module and as such will also use the same internal cables as the previous paragraphs described. (Figure 2). The external cable is detailed in Table 3. The software for the PPG 8/16 is provided with M/OS-80 and FLP-80DOS operating systems.

The Mostek PROM programmer, PPG-8/16, will need a power harness brought from an external source, like a lab supply, or from the RMC12 itself. The PPG-8/16 requires 5 Vdc, and plus and minus 12 Vdc. The power can be taken directly from the RMC12 power supply by soldering 24-guage wire from the solder lugs on the power supply to the connector. The power connector attaches to J2 on the back of the PPG-8/16 with a 12-pin card-edge connector. There are many sources for the connector but here is a list of a few: AMP #583970-1 housing; #66067-5 contacts, and Winchester Electonic #HCA6S. (See Figure 3)

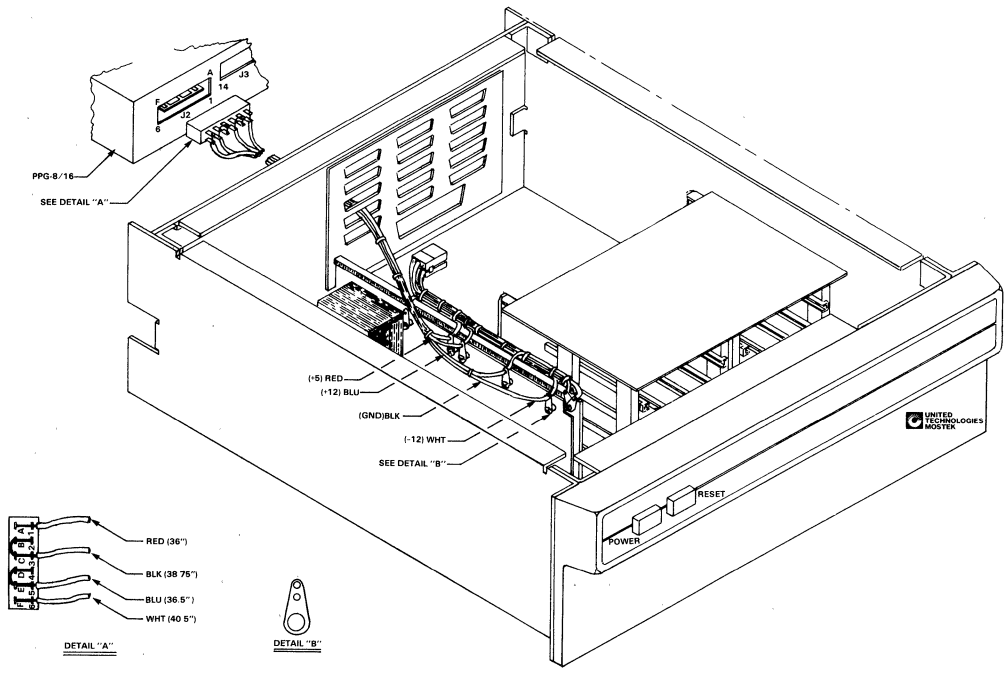
THE WIRING LIST FOR THE POWER CONNECTOR
Table 1

Power Supply Vdc	Connector Pin # (J2)	Color of Wire (24 AWG)
+12	4, D, 5, E	Blue
+5	1, A	Red
GND	2, B, 3, C	Black
-12	6, F	White

MDX-FLP, MDX-FLP2

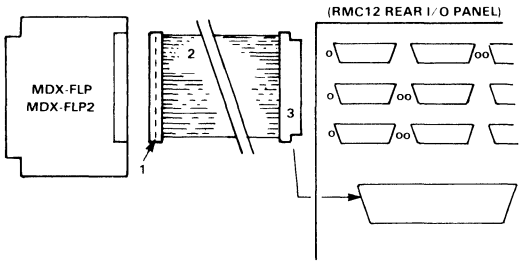
When the user needs Floppy Disk capabilities, another cable must be made. It interfaces Mostek's MDX-FLP module to the I/O panel. Mostek has a disk drive subsystem that contains two single-sided, single-density/double-density drives in a 19" rack-mount system called the RMDFSS. The cable suggested below is designed to interface the Mostek MDX-FLP Module to the rear I/O panel.

PPG/RMC 12 POWER CABLE
Figure 3



MDX-FLP MODULE TO THE REAR I/O PANEL

Figure 4



Materials for constructing the cable are listed below.

1. The MDX-FLP has a 50-pin header for I/O. The connector, like the previous cable discussed, is a mass-terminated crimp-on type of connector. (T&B Ansley part #609-5001M, Winchester Electronics #51-1150-01, or 3M' #3425-6050.)

2. The cable is 50-conductor flat cable, 24 inches long. (T&B Ansley #171-50, Winchester Electronic #55-5028-101-11 or 3M's #3320/50.)

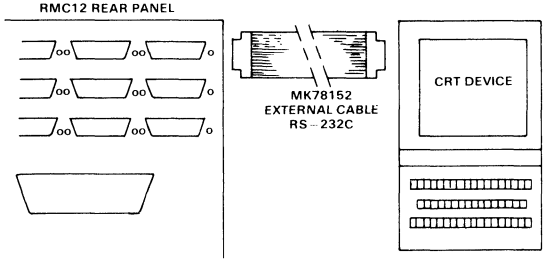
3. The connector that is attached to the rear I/O panel is also a mass-terminated connector. (T&B Ansley #609-50F or 3M #3489-1001.)

EXTERNAL CABLES

The external cables needed to interface the RMC12 and its complement boards will vary according to the user needs as do the internal cables. Detailed here are a few common cables.

EXTERNAL CABLING

Figure 5



RS-232C DEVICE TO REAR PANEL

The cable used to connect to a terminal device is a one-to-one 25-pin D connector (male). The Mostek cable can be purchased from Mostek or it can be constructed from the following components: Two 25-pin D-type pin connectors and five or six feet of twenty-five conductor flat ribbon cable.

The twenty-six conductor cable could be used if the last conductor is removed or trimmed back on both ends. The D connectors are like the T&B Ansley 609-25P. The cable is like T&B Ansley #609-25S, 26 conductor flat ribbon cable. The connectors are crimped on both ends to complete the cable.

RMC12 TO RMDFSS CABLE

When floppy disk-drive units are to be utilized with the RMC12, Mostek can provide a complete disk-drive subsystem, the RMDFSS. The RMDFSS is a rack-mountable, dual-floppy subsystem with two single-sided, single-density or double density drives with the power supply and muffin fan also provided in the enclosure. The disk drives are Shugart model number 800-2 drives and can be connected via a mass-terminated fifty-conductor cable from the rear of the I/O panel of the RMC12 and the rear of the RMDFSS subsystem via an external fifty-pin male connector (T&B Ansley 609-50M) on both ends of 50-conductor cable (T&B Ansley #609-50F). See Figure 6.

RMDFSS SUBSYSTEM

Figure 6

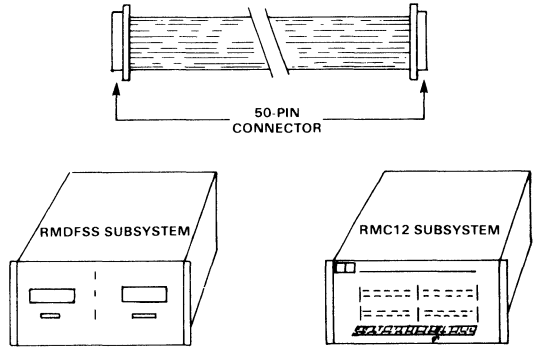


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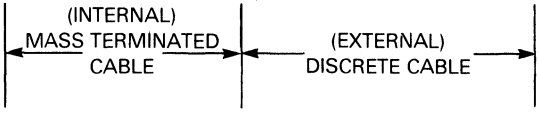
Table 2

Wire list for a cable from the Mostek Parallel Interface Module (1/2 MDX-PIO) to the rear I/O panel, and from the I/O panel to a parallel printer (Centronics-compatible). See MDX-PIO manual for board strapping instructions and component changes.

PIO Signal	26-Pin Header Conn.	Female Socket	Male Pin	Centronics Connector Socket	Centronics Parallel Signals
	*	**	***	****	
ARDY	J1-1	J1-1	J1-1		
$\overline{\text{ASTB}}$	J1-2	J1-2	J1-2		
A0	J1-19	J1-19	J1-19	2	DATA 1
A1	J1-6	J1-6	J1-6	3	DATA 2
A2	J1-18	J1-18	J1-18	4	DATA 3
A3	J1-5	J1-5	J1-5	5	DATA 4
A4	J1-17	J1-17	J1-17	6	DATA 5
A5	J1-4	J1-4	J1-4	7	DATA 6
A6	J1-16	J1-16	J1-16	8	DATA 7
A7	J1-3	J1-3	J1-3	9	DATA 8
BRDY	J1-12	J1-12	J1-12		
$\overline{\text{BSTB}}$	J1-11	J1-11	J1-11	10	$\overline{\text{ACKNLG}}$
B0	J1-7	J1-7	J1-7	1	$\overline{\text{STROBE}}$
B1	J1-20	J1-20	J1-20		
B2	J1-8	J1-8	J1-8		
B3	J1-21	J1-21	J1-21		
B4	J1-9	J1-9	J1-9	12	PE
B5	J1-22	J1-22	J1-22	11	BUSY
B6	J1-10	J1-10	J1-10		
B7	J1-23	J1-23	J1-23		
GND	J1-14	J1-14	J1-14		
GND	J1-15	J1-15	J1-15		
GND	J1-25	J1-25	J1-25	19	GND
GND	J1-24	J1-24	J1-24	20	GND

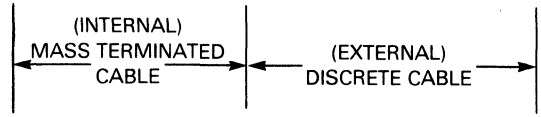


*26-pin header connector: T&B Ansley #609-2601-01
25-pin D-type ribbon socket connector: T&B Ansley 609-25S****
***25-pin D-type discrete pin plug connector: Cinch (TRW) #DBM-25P
****36-contact female connector: Cinch (TRW) #57-403060*****
*****Housing for the above 25-pin connector: Cinch (TRW) #DB-51226-1
******Pin 26 of the ribbon cable must be trimmed ½" before crimping

Table 3

Wire list for a cable from a Mostek parallel interface module (1/2 MDX-PIO) and a PROM programmer (PPG-8/16) to the rear I/O cable. See the MDX-PIO manual for board strapping instructions and component changes.

PIO Signal	26 Pin I/O	Female Male 25 D-Panel Connectors Socket	Pin	PPG-8/16 25-Pin D Connector	PPG-8/16 Signal Socket
	*	**	***	****	
ARDY	J2-1	J2-1	J2-1		
$\overline{\text{ASTB}}$	J2-2	J2-2	J2-2	J3-10	$\overline{\text{ASTB}}$
A0	J2-19	J2-19	J2-19	J3-1	PA0
A1	J2-6	J2-6	J2-6	J3-2	PA1
A2	J2-18	J2-18	J2-18	J3-3	PA2
A3	J2-5	J2-5	J2-5	J3-4	PA3
A4	J2-17	J2-17	J2-17	J3-5	PA4
A5	J2-4	J2-4	J2-4	J3-6	PA5
A6	J2-16	J2-16	J2-16	J3-7	PA6
A7	J2-3	J2-3	J2-3	J3-8	PA7
BRDY	J2-12	J2-12	J2-12		
$\overline{\text{BSTB}}$	J2-11	J2-11	J2-11	J3-17	$\overline{\text{BSTB}}$
B0	J2-7	J2-7	J2-7	J3-20	PB0
B1	J2-20	J2-20	J2-20	J3-21	PB1
B2	J2-8	J2-8	J2-8	J3-11	PB2
B3	J2-21	J2-21	J2-21	J3-12	PB3
B4	J2-9	J2-9	J2-9	J3-13	PB4
B5	J2-22	J2-22	J2-22	J3-14	PB5
B6	J2-10	J2-10	J2-10	J3-15	PB6
B7	J2-23	J2-23	J2-23	J3-16	PB7
GND	J2-14	J2-14	J2-14	J3-22	GND
GND	J2-15	J2-15	J2-15	J3-24	GND
GND	J2-25	J2-25	J2-25	J3-25	GND
GND	J2-24	J2-24	J2-24	J3-23	GND



*26-pin header connector: T&B Ansley #609-2601-01
25-pin D-type ribbon socket connector: T&B Ansley #609-25S****
***25-pin D-type discrete pin plug connector: Cinch (TRW) #DBM-25P
****25-pin D-type discrete socket connector: Cinch (TRW) #DBM-25S*****
*****Housing for the above 25-pin connectors; Cinch (TRW) #DB-51226-1
******Pin 26 of the ribbon cable must be trimmed ½" before crimping

Table 4

Wire list defining the cable from the communications modules, MDX-EPROM/UART, MDX-SIO, and MDX-SIO2, to the I/O panel and a communications device (i.e. Printer, CRT Terminal, etc.). The strapping information for the modules is detailed in the module operations manual.

SIO/ SIO2 (J1 or J2) EPROM/ UART Signal	26-Pin Header Conn.	Female Socket	Male Pin	25-Pin D Con- nector Socket	Printer or RS-232C Device
	*	**	***	***	
CHASSIS GND	J3-1	J3-1	J3-1	J3-1	CHASSIS GND
XMIT DATA	J3-2	J3-2	J3-2	J3-2	XMIT DATA
RECV DATA	J3-3	J3-3	J3-3	J3-3	RECV DATA
REQ TO SEND	J3-4	J3-4	J3-4	J3-4	REQ TO SEND
CLR TO SEND	J3-5	J3-5	J3-5	J3-5	CLR TO SEND
DATA SET RDY	J3-6	J3-6	J3-6	J3-6	DA SET RDY
GND	J3-7	J3-7	J3-7	J3-7	GND
CARRIER DETECT	J3-8	J3-8	J3-8	J3-8	CARRIER DETECT
	J3-9	J3-9	J3-9	J3-9	
	J3-10	J3-10	J3-10	J3-10	
	J3-11	J3-11	J3-11	J3-11	
20 mA- RECV RET	J3-12	J3-12	J3-12	J3-12	20 mA- SEND RET
20 mA+ SEND	J3-13	J3-13	J3-13	J3-13	20 mA+ RECV
	J3-14	J3-14	J3-14	J3-14	
	J3-15	J3-15	J3-15	J3-15	
READER STEP(+)	J3-16	J3-16	J3-16	J3-16	READER STEP(+)
	J3-17	J3-17	J3-17	J3-17	
	J3-18	J3-18	J3-18	J3-18	
	J3-19	J3-19	J3-19	J3-19	
DATA TERM RDY	J3-20	J3-20	J3-20	J3-20	DATA TERM RDY
READER STEP (-)	J3-21	J3-21	J3-21	J3-21	READER STEP (-)
	J3-22	J3-22	J3-22	J3-22	
	J3-23	J3-23	J3-23	J3-23	
20 mA+ RECV	J3-24	J3-24	J3-24	J3-24	20 mA+ SEND
20 mA- SEND	J3-25	J3-25	J3-25	J3-25	20 mA- RECV

(INTERNAL) ← MASS TERMINATED → CABLE | (EXTERNAL) ← MASS TERMINATED → CABLE

Notes for Table 4

*26-pin header connector: T&B Ansley #609-2601-01
25-pin D-type ribbon socket connector: T&B Ansley 609-25S**
***25-Pin D-type ribbon pin plug connector: T&B Ansley 609-25P
****Pin 26 of the ribbon cable must be trimmed ½" before crimping

MOSTEK PRODUCTS ORDERING INFORMATION

DESCRIPTION	MOSTEK #	NOTES
PROM Programmer PPG-8/16	MK79081-1	Cable included
PPG-8/16 cable only	MK79090	Power not provided
PIO to PPG Cable	MK77957	Power not provided
Centronics cable only	MK79089	used with scrambler
CRT cable only	MK78152	
MDX-PIO-parallel I/O MDX-PIO-4 4 MHz	MK77650 MK77650-4	STD-Z80 Module
MDX-SIO MDX-SIO-4	MK77651 MK77651-4	STD-Z80 Module
MDX-SIO2 MDX-SIO2-4	MK77670 MK77670-4	STD-Z80 Module
MDX-FLP	MK77654	STD-80 Module
MDX-EPROM/UART MDX-EPROM/UART	MK77753 MK77753-4	STD-Z80 Module
RMDFSS 115/220 V 50/60 Hz	MK78183 MK78185	Cable provided
RMDFSS cable only	MK79088	

VIII

APPLICATION BRIEF #3

RESET CIRCUIT FOR MDX-CPU2A

This application brief will detail the differences and the reason for the differences between the MDX-CPU2 and the MDX-CPU2A CPU cards.

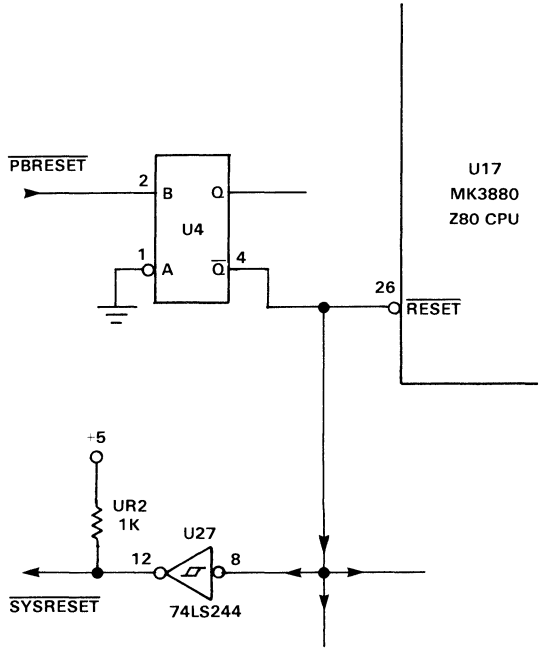
The difference between the two cards is in the way /SYSRESET is handled. The actual change is limited to a simple Printed Circuit Board change on the CPU card.

The change allows the /SYSRESET to be sourced by another card other than the CPU card (i.e. MDX-PFD). See Figures 1 and 2 for changes. Refer to the MDX-PFD manual for specifics on the power-fail detect usage.

The changes do not affect the parts count or the option strapping headers.

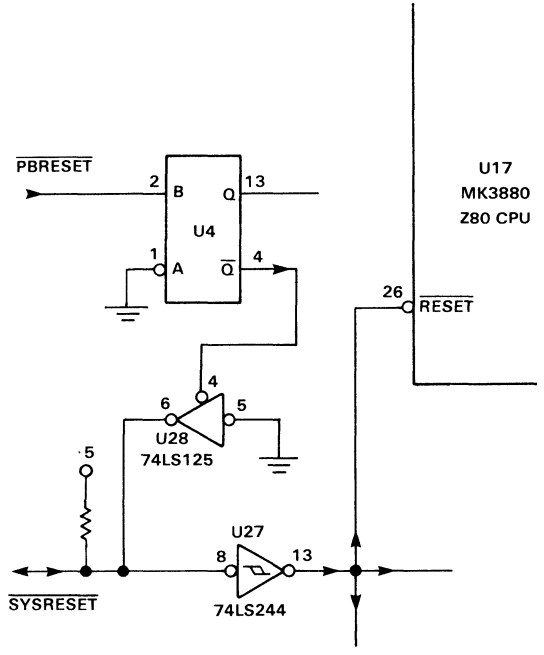
RESET CIRCUIT FOR CPU2

Figure 1



RESET CIRCUIT FOR CPU2A

Figure 2



VIII

APPLICATION NOTE #4
RESET CIRCUIT FOR MDX-CPU1A

This application note will detail the difference and the reason for the difference between the MDX-CPU1 and the MDX-CPU1A CPU cards. The difference between the two cards is in the way /SYSRESET is handled. The actual change required the addition of an IC and a change to the Printed Circuit Board.

These changes allow the /SYSRESET to be sourced by a card other than the CPU card (i.e. MDX-PFD). See Figures 1 and 2 for the affected circuitry.

For specifics on how to use the power-fail detect card, refer to the MDX-PFD Operations Manual.

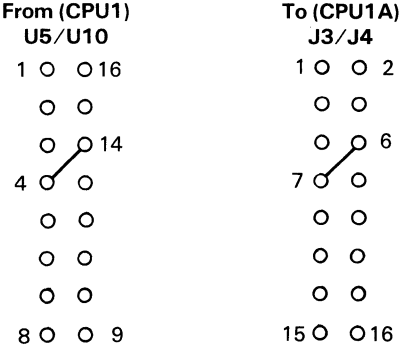
The addition of the IC provided the opportunity to bring the nomenclature screen up to date with the present practices in labeling headers and parts. These changes affect the parts count, nomenclature screen, and the option-strapping headers. Tables 1 and 2 will point out the changes in the option-headers and the parts designators.

OPTION HEADERS

Table 1

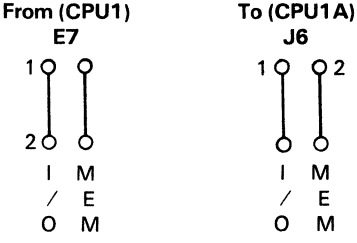
Old Designator	New Designator	Comments
U5	J3	number scheme changed
U10	J4	number scheme changed
E3, E4	J2	Pins 1 and 3 of J2
E5, E6	J2	Pins 4 and 2 of J2
E1, E2	J5	No functional change
E7	J6	No functional change

Option-header Jumpers



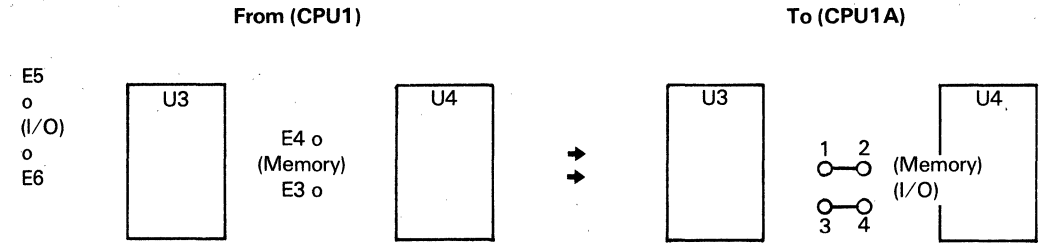
Example:
U5 4 to 14 = J3 7 to 6

Memory and I/O Expand jumper options



VIII

Wait State Jumper Options (I/O and Memory)



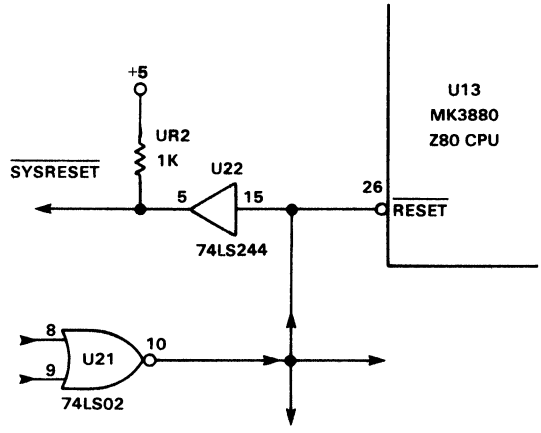
PARTS DESIGNATORS

Table 2

CPU1 Designator	PART	CPU1A Designator
U1	74S04	U1
U11	74LS14	U9
U12	74LS138	U10
U13	74LS04	U11
U14	MK3882	U12
U15	MK3880	U13
U17	74LS165	U17
U18	74LS393	U15
U2, 16	74LS74	U2, 14
U20	74LS32	U19
U21	74LS02	U20
U22, 25, 27	74LS244	U21, 24, 26
U23	35392	U22
U24	74LS245	U23
U26	74LS373	U25
U28	74LS08	U27
U29	OSC. 5/8MHz	Y1
U3	74LS00	U3
U4	74LS10	U4
U8	74S74	U7
U9, 19	74LS30	U8, 18
UR1, UR2	1K RES,SIP 6 PIN	UR1, UR2
UR3	22K RES,SIP 6 PIN	UR3
UR4	1K RES,SIP 8 PIN	UR4
X14	28 PIN SOCKET	X12
X15	40 PIN SOCKET	X13
X23	22 PIN SOCKET	X22
X6, X7	24 PIN SOCKET	X5, X6
C2	CAP. 33PF	C1
C3-5, 7-13, 15	CAP. .1UF	C2-3, C5-19
C6, 14	CAP. 15UF	C4, C20
CR1	DIODE IN914	CR1
Q1	TRANSISTOR 2N3906	Q1
R12, 13	RES. 4.7K OHMS	R2, 5
R3, 5, 8, 11	RES. 1.1K OHMS	R3, 4, 6, 9
R4, 10	RES. 270 OHMS	R1
R6	RES. 10K OHMS	R7
R7	RES. 22 OHMS	R8
R9	RES. 510 OHMS	R10

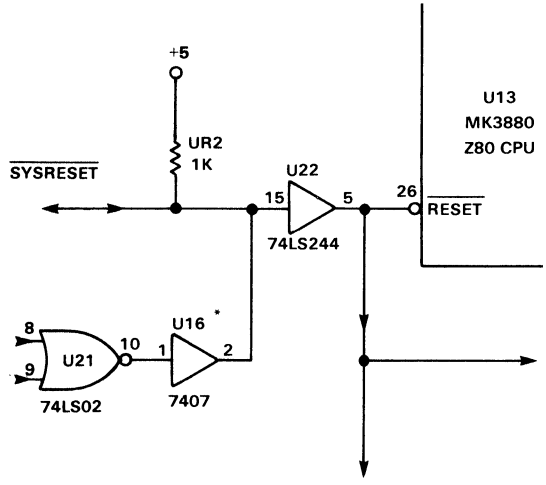
RESET CIRCUIT FOR CPU1

Figure 1



RESET CIRCUIT FOR CPU1A

Figure 2



* IC ADDED TO BOARD

VIII

APPLICATION NOTE #5
CUSTOMIZING THE MDX-CPU3 PROM

SCOPE:

This application note will detail how to customize the two PROM's (U23 and U24) on the MDX-CPU3.

CUSTOMIZING U23 (MK6360):

This bipolar PROM performs several functions. First, it provides the address decoding for the chip select signal to the Serial Timer Interrupt device (MK3801); Second, it provides the clocking pulse for the parallel output latch; Third, it provides the clocking signal pulse for the memory configuration latch; And fourth, it provides the input to the Programmable Array Logic (PAL) device indicating that an onboard port is being addressed.

The data contained in the bipolar PROM provided on the MDX-CPU3 is listed at the end of this application note. If a change is required (such as using a different address other than B0-BF for the serial port or D0 for the printer output port), a new bipolar PROM must be programmed. See Table 1 for the information needed to compute the correct data for your PROM.

BIPOLAR PROM OUTPUT-PIN AND DATA BIT DEFINITION
Table 1

OUTPUT PIN #	PROM DATA BIT 3	2	1	0	SIGNAL DESCRIPTION	ACTIVE STATE
12	—	—	—	X	STI Chip Select (MK3801)	HI
11	—	—	X	—	Output Latch Select (PTR)	HI
10	—	X	—	—	Memory Config Select	HI
9	X	—	—	—	Any Port Select (PAL input)	LO

For example, if a user wishes to have the STI port at 10-1F instead of B0-BF, the data in the remaining location 10-1F would be 1H (0001). The data in the remaining locations of the PROM must also be computed and programmed.

NOTE: Depending on the bits being changed and the type of unprogrammed bit (unprogrammed bit = 1 or 0) of the PROM, it may be possible to use the existing PROM.

CUSTOMIZING U24 (MK6359):

U24 is a bipolar PROM programmed at the factory (part number MK6359) to provide several functions for the MDX-CPU3. First, it provides the chip select signal to the EPROM/ROM socket; Second, it provides the A15 address line to select upper or lower 32K memory for on-board dynamic memory; Third, it provides the RAM select (RSEL) signal (on-board vs off-board) for an input to the PAL; And fourth, it provides the memory expand (MEMEX) signal for use in bank selecting of additional off-board memory.

The data contained in the bipolar function PROM provided on the MDX-CPU3 is listed at the end of this application note. If a change is required (such as using memory maps other than those provided), a new bipolar PROM must be programmed. See Table 2 for the information needed to compute the correct data for your PROM.

BIPOLAR PROM OUTPUT-PIN AND DATA BIT DEFINITION
Table 2

OUTPUT PIN #	PROM DATA BIT 3	2	1	0	SIGNAL DESCRIPTION	ACTIVE STATE
12	-	-	-	X	EPROM/ROM Select	LO
11	-	-	X	-	A15 Address Line	**
10	-	X	-	-	Select On-board RAM	LO
9	X	-	-	-	Memory Expand Output	LO

** = Tracks A15 input line, on shipped PROM. Potential use of this feature could be to have two separate 32K RAM memory banks on-board when using a MK38000 ROM (32K x 8.)

The 64K memory map is shown in Figure 1. Note that each PROM location represents a 2K block of CPU addressable memory. The PROM location for the MAP 0 is depicted in Figure 1.

MEMORY MAP SHOWING PROM ADDRESS LOCATIONS

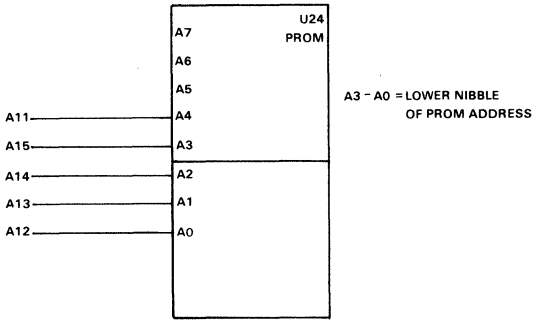
Figure 1

CPU Address Change	PROM Address
F800 - FFFF	1F
F000 - F7FF	0F
E800 - EFFF	1E
E000 - E7FF	0E
D800 - DFFF	1D
D000 - D7FF	0D
C800 - CFFF	1C
C000 - C7FF	0C
B800 - BFFF	1B
B000 - B7FF	0B
A800 - AFFF	1A
A000 - A7FF	0A
9800 - 9FFF	19
9000 - 97FF	09
8800 - 8FFF	18
8000 - 87FF	08
7800 - 7FFF	17
7000 - 77FF	07
6800 - 6FFF	16
6000 - 67FF	06
5800 - 5FFF	15
5000 - 57FF	05
4800 - 4FFF	14
4000 - 47FF	04
3800 - 3FFF	13
3000 - 37FF	03
2800 - 2FFF	12
2000 - 27FF	02
1800 - 1FFF	11
1000 - 17FF	01
0800 - 0FFF	10
0000 - 07FF	00

CROSS REFERENCE

CPU Address Bus to Prom Address Bus

Figure 3



PROM LOCATIONS AND PROM DATA BIT INFORMATION

Figure 2

MEMORY MAP	PROM LOC	BIT # 3210	DATA
0000H	00H	1100	CH
1000H	01H	1001	9H
2000H	02H	1001	9H
3000H	03H	1001	9H
4000H	04H	1001	9H
5000H	05H	1001	9H
6000H	06H	1001	9H
7000H	07H	1001	9H
8000H	08H	1011	BH
9000H	09H	1011	BH
A000H	0AH	1011	BH
B000H	0BH	1011	BH
C000H	0CH	1011	BH
D000H	0DH	1011	BH
E000H	0EH	1011	BH
F000H	0FH	1011	BH
0800H	10H	1001	9H
1800H	11H	1001	9H
2800H	12H	1001	9H
3800H	13H	1001	9H
4800H	14H	1001	9H
5800H	15H	1001	9H
6800H	16H	1001	9H
7800H	17H	1001	9H
8800H	18H	1011	BH
9800H	19H	1011	BH
A800H	1AH	1011	BH
B800H	1BH	1011	BH
C800H	1CH	1011	BH
D800H	1DH	1011	BH
E800H	1EH	1011	BH
F800H	1FH	1011	BH

NOTE: A contiguous addressing of memory does not enable sequential PROM address locations.

EXAMPLE

To truely understand the memory mapping PROM (U24), the following examples are given.

Eample #1 - You have a 2K EPROM (2716) that you would like to place in the memory map (Map 0) at location 0000H. Refer to Table 2. Bit 0 must be enabled (0 = active low) and the remaining three Bits selected accordingly. The PROM location to be programmed would be 00H. See Figure 2.

Example #2 - You have a 2K EPROM (2716) that you would like to place in the memory map (Map 0) at location E800H. Refer to Table 2. Bit 0 must be enabled (0 = active low) and the remaining three Bits selected accordingly. The PROM location to be programmed would be 1EH. See Figure 3.

Example #3 - You have a 4K EPROM (2732) that you would like to place in the memory map (Map 0) at location 0000H. Refer to Table 2. Bit 0 must be enabled (0 = active low) and the remaining three Bits selected accordingly. The PROM locations to be programmed would be 00H and 10H.

Example #4 - You have a 4K EPROM (2732) that you would like to place in the memory map (Map 0) at location 2800H. Refer to Table 2. Bit 0 must be enabled (0 = active low) and the remaining three Bits selected accordingly. The PROM locations to be programmed would be 12H and 03H.

Example #5 - You have a 8K EPROM (2764) that you would like to place in the memory map (Map 0) at location 0000H. Refer to Table 2. Bit 0 must be enabled (0 = active low) and the remaining three Bits selected accordingly. The PROM locations to be programmed would be 00H, 10H, and 11H.

Example #6 - You have a 32K ROM (MK38000) that you would like to place in the memory map (Map 0) at location 0000H. You would also like to take full advantage of having 64K Dynamic memory on the MDX-CPU3 board. i.e., you would like to have one memory map use one half of memory with the same 32K ROM. Thus, you essentially would have a 32K ROM system with 64K of Dynamic RAM on the same board. By installing jumper J5, the D2 input to U13 is no longer tied high and will follow the logic level represented by the D2 bit. Also, since the A15 address line is selected by the bipolar PROM, the A15 line is enabled to select the lower half of RAM for Map 0 and upper half of RAM for Map 1 as shown in Figures 4 and 5.

MAP 0 FOR EXAMPLE 6

Figure 4

MEMORY MAP	PROM LOC	BIT # 3210 (BINARY)	PROGRAMMED DATA (HEX)
0000H	00H	1100	CH
1000H	01H	1100	CH
2000H	02H	1100	CH
3000H	03H	1100	CH
4000H	04H	1100	CH
5000H	05H	1100	CH
6000H	06H	1100	CH
7000H	07H	1100	CH
8000H	08H	1011	BH
9000H	09H	1011	BH
A000H	0AH	1011	BH
B000H	0BH	1011	BH
C000H	0CH	1011	BH
D000H	0DH	1011	BH
E000H	0EH	1011	BH
F000H	0FH	1011	BH

Figure 4 (cont.)

0800H	10H	1100	CH
1800H	11H	1100	CH
2800H	12H	1100	CH
3800H	13H	1100	CH
4800H	14H	1100	CH
5800H	15H	1100	CH
6800H	16H	1100	CH
7800H	17H	1100	CH
8800H	18H	1011	BH
9800H	19H	1011	BH
A800H	1AH	1011	BH
B800H	1BH	1011	BH
C800H	1CH	1011	BH
D800H	1DH	1011	BH
E800H	1EH	1011	BH
F800H	1FH	1011	BH

Programmed data is a HEX value arrived at by using information from Table 2.

MAP 1 FOR EXAMPLE 6

Figure 5

MEMORY MAP	PROM LOC	BIT # 3210 (BINARY)	PROGRAMMED DATA (HEX)
0000H	20H	1100	CH
1000H	21H	1100	CH
2000H	22H	1100	CH
3000H	23H	1100	CH
4000H	24H	1100	CH
5000H	25H	1100	CH
6000H	26H	1100	CH
7000H	27H	1100	CH
8000H	28H	1001	9H
9000H	29H	1001	9H
A000H	2AH	1001	9H
B000H	2BH	1001	9H
C000H	2CH	1001	9H
D000H	2DH	1001	9H
E000H	2EH	1001	9H
F000H	2FH	1001	9H
0800H	30H	1100	CH
1800H	31H	1100	CH
2800H	32H	1100	CH
3800H	33H	1100	CH
4800H	34H	1100	CH
5800H	35H	1100	CH
6800H	36H	1100	CH
7800H	37H	1100	CH
8800H	38H	1001	9H
9800H	39H	1001	9H
A800H	3AH	1001	9H
B800H	3BH	1001	9H
C800H	3CH	1001	9H
D800H	3DH	1001	9H
E800H	3EH	1001	9H
F800H	3FH	1001	9H

BANK SWITCHING

An application may require more than one bank of memory. The MDX-CPU3 board supports bank switching by addressing the control port FF and sending it the bank number the user wishes to select. However, bank numbers and memory map numbers are not one and the same. See Tables 3A and 3B.

BANK SWITCHING WITH JUMPER J5 INSTALLED

Table 3A

DATA WRITTEN TO PORT FF	TO SELECT BANK #	AND SELECT MAP #	ADDRESS BIT 15	14	13	12	11	PROM BIT D2	D1	D0
RESET (00)	0	0	0	0	0	0	0	0	0	0
00	0	0	0	0	0	0	0	0	0	0
01	1	1	0	0	0	0	0	0	0	1
02	2	2	0	0	0	0	0	0	1	0
04	3	4	0	0	0	0	0	1	0	0
08	4	0	0	0	0	0	1	0	0	0
10	5	0	0	0	0	1	0	0	0	0
20	6	0	0	0	1	0	0	0	0	0
40	7	0	0	1	0	0	0	0	0	0
80	8	0	1	0	0	0	0	0	0	0

BANK SWITCHING WITH JUMPER J5 NOT INSTALLED (BIT D2 REMAINS HIGH FOR PROM)

Table 3B

DATA WRITTEN TO PORT FF	TO SELECT BANK #	AND SELECT MAP #	ADDRESS BIT 15	14	13	12	11	PROM BIT D2	D1	D0
RESET (00)	0	0	0	0	0	0	0	0	0	0
00	0	4	0	0	0	0	0	*	0	0
01	1	5	0	0	0	0	0	*	0	1
02	2	6	0	0	0	0	0	*	1	0
04	3	4	0	0	0	0	0	1	0	0
08	4	4	0	0	0	0	1	*	0	0
10	5	4	0	0	0	1	0	*	0	0
20	6	4	0	0	1	0	0	*	0	0
40	7	4	0	1	0	0	0	*	0	0
80	8	4	1	0	0	0	0	*	0	0

*** = 1 for Memory Decode PROM**
0 for Data off-board

EXPANDING THE NUMBER OF MEMORY MAPS

The devices shipped and discussed above will allow a maximum of 8 maps. However, should a user require more maps and not need to follow Mostek's bank selecting scheme, 16 maps are possible. The user can place a MMI-6306 (512 x 4) bipolar PROM (with users' programmed data) in socket U24; Lift pin U24-14 and connect a wire wrap wire from it to U13-10 and insert jumper J5. Now the user will have access to a total of 16 memory maps available.

PAL PIN DEFINITIONS:

Listed in Table 4 are the Boolean expressions for the PAL logic. These are listed to help the user know which signals are affected when changes are made to either of the two PROMs mentioned earlier.

PAL OUTPUT-PIN SIGNAL DESCRIPTION

Table 4

OUTPUT PIN #	SIGNAL		DESCRIPTION
16	CASSOFF	=	RFSH + IORQ + EPSEL*RD +/RSEL*/EPSEL
17	ENROM	=	RD*MREQ
19	INTAK	=	M1*IORQ
12	/WRTLTH	=	/IORQ + /WR +/PORTSEL
15	/MCYCLE	=	/MREQ +/RFSH*/WR*/RD
18	/DATAIN	=	RD*MREQ*RSEL + RD*MREQ*EPSEL + RD*IORQ*PORTSEL + M1*IORQ*/IEI*IEO + /BUSAK*/RD*MREQ + /BUSAK*/M1*/IORQ*/MREQ + /BUSAK*/RD*IORQ*/M1

PROM PATTERN (MMI 6301-1J 256 x 4)
U23 MK6360

LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA
00	8	20	8	40	8	60	8	80	8	A0	8	C0	8	E0	8
01	8	21	8	41	8	61	8	81	8	A1	8	C1	8	E1	8
02	8	22	8	42	8	62	8	82	8	A2	8	C2	8	E2	8
03	8	23	8	43	8	63	8	83	8	A3	8	C3	8	E3	8
04	8	24	8	44	8	64	8	84	8	A4	8	C4	8	E4	8
05	8	25	8	45	8	65	8	85	8	A5	8	C5	8	E5	8
06	8	26	8	46	8	66	8	86	8	A6	8	C6	8	E6	8
07	8	27	8	47	8	67	8	87	8	A7	8	C7	8	E7	8
08	8	28	8	48	8	68	8	88	8	A8	8	C8	8	E8	8
09	8	29	8	49	8	69	8	89	8	A9	8	C9	8	E9	8
0A	8	2A	8	4A	8	6A	8	8A	8	AA	8	CA	8	EA	8
0B	8	2B	8	4B	8	6B	8	8B	8	AB	8	CB	8	EB	8
0C	8	2C	8	4C	8	6C	8	8C	8	AC	8	CC	8	EC	8
0D	8	2D	8	4D	8	6D	8	8D	8	AD	8	CD	8	ED	8
0E	8	2E	8	4E	8	6E	8	8E	8	AE	8	CE	8	EE	8
0F	8	2F	8	4F	8	6F	8	8F	8	AF	8	CF	8	EF	8
10	8	30	8	50	8	70	8	90	8	B0	1	D0	2	F0	B
11	8	31	8	51	8	71	8	91	8	B1	1	D1	8	F1	8
12	8	32	8	52	8	72	8	92	8	B2	1	D2	8	F2	8
13	8	33	8	53	8	73	8	93	8	B3	1	D3	8	F3	8
14	8	34	8	54	8	74	8	94	8	B4	1	D4	8	F4	8
15	8	35	8	55	8	75	8	95	8	B5	1	D5	8	F5	8
16	8	36	8	56	8	76	8	96	8	B6	1	D6	8	F6	8
17	8	37	8	57	8	77	8	97	8	B7	1	D7	8	F7	8
18	8	38	8	58	8	78	8	98	8	B8	1	D8	8	F8	8
19	8	39	8	59	8	79	8	99	8	B9	1	D9	8	F9	8
1A	8	3A	8	5A	8	7A	8	9A	8	BA	1	DA	8	FA	8
1B	8	3B	8	5B	8	7B	8	9B	8	BB	1	DB	8	FB	8
1C	8	3C	8	5C	8	7C	8	9C	8	BC	1	DC	8	FC	8
1D	8	3D	8	5D	8	7D	8	9D	8	BD	1	DD	8	FD	8
1E	8	3E	8	5E	8	7E	8	9E	8	BE	1	DE	8	FE	8
1F	8	3F	8	5F	8	7F	8	9F	8	BF	1	DF	8	FF	4

NOTE: Data is in HEX

PROM PATTERN (MMI 6301-1J 256 x 4)
U24 MK6359

LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA	LOC	DATA
00	C	20	F	40	F	60	F	80	D	A0	9	C0	D	E0	F
01	9	21	F	41	F	61	F	81	D	A1	9	C1	D	E1	F
02	9	22	F	42	F	62	F	82	D	A2	9	C2	D	E2	F
03	9	23	F	43	F	63	F	83	D	A3	9	C3	D	E3	F
04	9	24	F	44	F	64	F	84	D	A4	9	C4	D	E4	F
05	9	25	F	45	F	65	F	85	D	A5	9	C5	D	E5	F
06	9	26	F	46	F	66	F	86	D	A6	9	C6	D	E6	F
07	9	27	F	47	F	67	F	87	D	A7	9	C7	D	E7	F
08	B	28	F	48	F	68	F	88	F	A8	B	C8	F	E8	F
09	B	29	F	49	F	69	F	89	F	A9	B	C9	F	E9	F
0A	B	2A	F	4A	F	6A	F	8A	F	AA	B	CA	F	EA	F
0B	B	2B	F	4B	F	6B	F	8B	F	AB	B	CB	F	EB	F
0C	B	2C	F	4C	F	6C	F	8C	F	AC	B	CC	F	EC	F
0D	B	2D	F	4D	F	6D	F	8D	F	AD	B	CD	F	ED	F
0E	A	2E	F	4E	F	6E	F	8E	B	AE	B	CE	B	EE	F
0F	B	2F	F	4F	F	6F	F	8F	B	AF	B	CF	B	EF	F
10	C	30	F	50	F	70	F	90	D	B0	9	D0	D	F0	F
11	9	31	F	51	F	71	F	91	D	B1	9	D1	D	F1	F
12	9	32	F	52	F	72	F	92	D	B2	9	D2	D	F2	F
13	9	33	F	53	F	73	F	93	D	B3	9	D3	D	F3	F
14	9	34	F	54	F	74	F	94	D	B4	9	D4	D	F4	F
15	9	35	F	55	F	75	F	95	D	B5	9	D5	D	F5	F
16	9	36	F	56	F	76	F	96	D	B6	9	D6	D	F6	F
17	9	37	F	57	F	77	F	97	D	B7	9	D7	D	F7	F
18	B	38	F	58	F	78	F	98	F	B8	B	D8	F	F8	F
19	B	39	F	59	F	79	F	99	F	B9	B	D9	F	F9	F
1A	B	3A	F	5A	F	7A	F	9A	F	BA	B	DA	F	FA	F
1B	B	3B	F	5B	F	7B	F	9B	F	BB	B	DB	F	FB	F
1C	B	3C	F	5C	F	7C	F	9C	F	BC	B	DC	F	FC	F
1D	B	3D	F	5D	F	7D	F	9D	F	BD	B	DD	F	FD	F
1E	A	3E	F	5E	F	7E	F	9E	B	BE	B	DE	B	FE	F
1F	B	3F	F	5F	F	7F	F	9F	B	BF	B	DF	B	FF	F

NOTE: Data is in HEX

UPGRADING FROM MDX-FLP1 TO MDX-FLP2 APPLICATION NOTE #6

INTRODUCTION

With the advent of the MDX-FLP2, Mostek STD-Z80 BUS systems have the capability of maintaining up to 4 MB of floppy storage on-line. In order for this benefit to be realized, the appropriate hardware and software products need to be brought together. This application note will detail the required software (M/OS-80) and hardware configurations necessary in order to make use of the above-mentioned benefit. The information contained herein is sufficient to make the transition from a FLP1-based system to a FLP2-based system. It is assumed that the system contains a CPU card (CPU1, 2, 3, etc.), sufficient memory to meet the operating system's needs, and at least a console interface (SIO, SIO2, EPROM/UART, etc.). Additional information may be gained from the M/OS-80 operations manual, the MDX-FLP2 data sheet/technical manual, and the MOSGEN operations manual. (See references.)

SOFTWARE

A system which is currently running M/OS-80 in conjunction with an MDX-FLP1 should have FLP1-DCF EPROM# MK6286 and one of several DDT EPROMs for the console and printer interfaces. There is no need to change the DDT EPROM when upgrading to an MDX-FLP2. The correct EPROM for an MDX-FLP2 system is FLP2-DCF EPROM #MK6340. Of course these EPROMs only apply to those M/OS-80 versions which are designed to run as non-phantom systems. Any version of M/OS-80 which is less than 5.0 is non-phantom.

Mostek uses the term "phantom" to indicate those systems in which the boot firmware is non-resident. In addition, the disk drivers are brought in as part of the operating system rather than being EPROM-resident. This gives greater flexibility to the system due to the increased space for software on a disk versus permanent EPROM storage in the system memory space. Through the use of a phantom system, only a bare bones disk driver need be resident during the boot phase. This driver determines the appropriate software routines which need to be loaded for a given hardware configuration. After this decision has been made, the boot firmware is phantomed out of the system memory space, thus freeing up additional memory.

Versions 5.0 or greater are designed to run as phantom systems and require a special "boot" EPROM. These systems are, in general, designed to utilize the MDX-CPU3 and MDX-CPU4 due to their ability to phantom certain memory sockets. As shipped from the factory, the default floppy controller in a phantom system is the MDX-FLP2. So, in most cases there will not need to be a migration path for MDX-FLP1 to MDX-FLP2 in phantom systems. There are, however, driver routines provided in the MOSGEN package which will allow the use of an MDX-FLP1 in a phantom system. Table 1 summarizes the various combinations of software and hardware which Mostek offers.

When utilizing the double-density capabilities of the MDX-FLP2 in a non-phantom system, the user must be aware of the requirement for tracks one and two to be formatted as single density. This is a requirement of the DCF EPROMs. The technique for generating a double-density operating system diskette in a non-phantom system is as follows:

1. Format the whole diskette as single density.
2. WRTSYS the diskette from a single-density source.
3. Go back into the format program and reformat the diskette beginning at track 2 as double-density.

After having completed the above procedure, the diskette can now be filled with data from other sources. The file area will have data stored in a double-density format while the system area will have data stored in a single-density format. The above procedure isn't necessary for a phantom system due to its ability to determine which floppy controller device is in the system and in what format the data is stored on the diskette.

HARDWARE

As shipped from the factory, the MDX-FLP2 is strapped correctly for operation with either M/OS-80 or FLP-80DOS and 8 inch drives. It is still a good idea to verify that the appropriate straps are in place. Figure 1 shows a board outline of the MDX-FLP2 and the placement of the jumper headers. Figure 1 also shows the correct strapping for the MDX-FLP2 as it is shipped from the factory. The following discussion details the operation of each strap on the MDX-FLP2.

J4: Auto Precomp — When open, double density write precompensation is always in effect (provided DDEN* is low). This is primarily for 5¼ inch drives that require write precompensation of every track. When strapped, write data is precompensated only for tracks greater than 43; (factory setting)

M/OS 80 CONFIGURATIONS

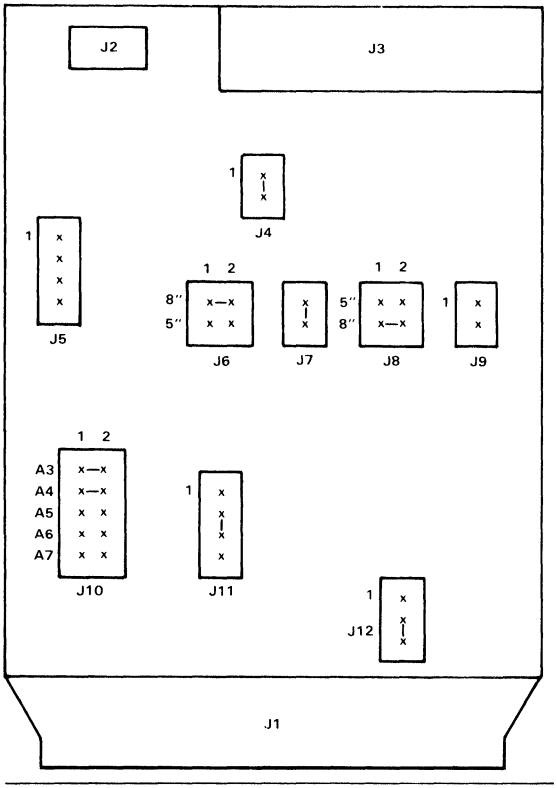
Table 1

Configuration	CPU			Memory (K)		Peripheral Devices			
File Name	**CPU**	**MHz**	**O/S**	**PROMs**	**Size**	**Console**	**Printer**	**Floppy**	**Hard Disk**
M/OS-80 -4									
Customer Update									
(MOS-AP32)	1,2	2&4	9	DDT/DCF	32	ALLCON1	PIOLST	FLP1[E0,8BO,5O,4D,A:,SDB,SDO]	NONE
MOS-AP48	1,2	2&4	9	DDT/DCF	48	ALLCON1	PIOLST	FLP1[E0,8BO,5O,4D,A:,SDB,SDO]	NONE
MOS-AP56	1,2	2&4	9	DDT/DCF	56	ALLCON1	PIOLST	FLP1[E0,8BO,5O,4D,A:,SDB,SDO]	NONE
MOS-AP64	1,2	2&4	13	DDT/DCF	64	ALLCON1	PIOLST	FLP1[E0,8BO,5O,4D,A:,SDB,SDO]	NONE
MOS-AS32	1,2	2&4	9	DDT/DCF	32	ALLCON1	SIOLST	FLP1[E0,8BO,5O,4D,A:,SDB,SDO]	NONE
MOS-AS48	1,2	2&4	9	DDT/DCF	48	ALLCON1	SIOLST	FLP1[E0,8BO,5O,4D,A:,SDB,SDO]	NONE
MOS-AS56	1,2	2&4	9	DDT/DCF	56	ALLCON1	SIOLST	FLP1[E0,8BO,5O,4D,A:,SDB,SDO]	NONE
MOS-AS64	1,2	2&4	13	DDT/DCF	64	ALLCON1	SIOLST	FLP1[E0,8BO,5O,4D,A:,SDB,SDO]	NONE
System Release									
(MOS-AP64)	1,2	2&4	13	DDT/DCF	64	ALLCON1	PIOLST	FLP1[E0,8BO,5O,4D,A:,SDB,SDO]	NONE
MOS-AS64	1,2	2&4	13	DDT/DCF	64	ALLCON1	SIOLST	FLP1[E0,8BO,5O,4D,A:,SDB,SDO]	NONE
MOS-DAP6	1,2	2&4	14	DDT/DCF PHANTOM	64	ALLCON1	PIOLST	FLP2[E0,8BO,5O,4D,A:,SDB,DDO] FLP2[E0,8BO,5BO,4D,A:,DDB,DDO]	NONE
MOS-DAS6	1,2	2&4	14	DDT/DCF PHANTOM	64	ALLCON1	SIOLST	FLP2[E0,8BO,5O,4D,A:,SDB,DDO] FLP2[E0,8B0,580,4D,A:,DDB,DDO]	NONE
M/OS-80 -5									
System Release									
(MOS-PHM)	3,4	4.0	9	PHANTOM	64	ALLCON2	ALLST	FLP2[E0,8BO,5BO,4D,A:,DDB,DDO]	NONE
MOS-TS	3,4	4.0	9	PHANTOM	64	ALLCON2	SIOLST	FLP2[E0,8BO,5BO,4D,A:,DDB,DDO]	NONE
MOS-8K	3,4	4.0	8	PHANTOM	64	ALLCON2	ALLLST	FLP2[E0,8BO,5BO,2D,A:,DDB,DDO]	NONE
MOS-TS8K	3,4	4.0	8	PHANTOM	64	ALLCON2	SIOLST	FLP2[E0,8BO,5BO,2D,A:,DDB,DDO]	NONE
MOS-F85	3,4	4.0	9	PHANTOM	64	ALLCON2	ALLLST	FLP2[E0,8BO,3BO,4D,A:,DDB,DDO] +FLP2[C0,80,50,3D,E:,DD0]	NONE
M/OS-80 -6									
System Release									
(MOS-HTTF)	3,4	4.0	12	PHANTOM	64	ALLCON2	ALLLST	FLP2[E0,8BO,5BO,4D,A:,DDB,DDO]	SASI1[A0,5BO,2D,E:,DDB,DDO]
MOS-HTSF	3,4	4.0	12	PHANTOM	64	ALLCON2	SIOLST	FLP2[E0,8BO,5BO,4D,A:,DDB,DDO]	SASI1[A0,3BO,2D,E:,DDB,DDO]
MOS-HTTH	3,4	4.0	12	PHANTOM	64	ALLCON2	ALLLST	FLP2[E0,8BO,5BO,4D,C:,DDB,DDO]	SASI1[A0,5BO,2D,A:,DDB,DDO]
MOS-HTSH	3,4	4.0	12	PHANTOM	64	ALLCON2	SIOLST	FLP2[E0,8BO,5BO,4D,C:,DDB,DDO]	SASI1[A0,5BO,2D,A:,DDB,DDO]
MOS-HF85	3,4	4.0	12	PHANTOM	64	ALLCON2	ALLLST	FLP2[E0,8B0,5B0,4D,A:,DDB,DDO] +FLP2[C0,8O,5O,3D,E:,DDO]	SASI1[A0,5BO,2D,H:,DDB,DDO]

( ) : FILE NAMED SYSTEM.COM ON RELEASE DISK
CPU MHz 2&4 : CALCULATED BAUD RATE AT BOOT-UP 2.5 TO 4.0
CPU 1,2 : MDX-CPU1 OR MDX-CPU2
ALLCON1 : UART OR SIO AT PORT 0DCH
ALLCON2 : STI AT PORT 0B0H OR UART/SIO AT PORT 0DCH
ALLLST : STI OR PIO AT PORT 0D0H
PIOLST: MDX-PIO AT PORT 0D0H
SIOLST : MDX-SIO AT PORT 0DEH
PHANTOM : PHANTOM BOOTM PROM
PHANTOMX : MODIFIED PHANTOM PROM TO OPERATE NON-PHANTOM
FLOPPY : FLP2[E0,8BO,5BO,4D,A:,SDB,SDO] = MDX-FLP2, PORT 0EOH, 8" BOOT/OPERATION, 5" BOOT/OPER, 4 LOGICAL DRIVES, START DRIVE A:, SINGLE DENSITY BOOT-UP, SINGLE DENSITY OPERATION
HARD DISK : SASI1[A0,5BO,2D,E:,DDB,DDO] = MDX-SASI1, PORT 0A0H, 2 LOGICAL DRIVES, START DRIVE E:, DOUBLE DENSITY BOOT, OPERATION

FLP2 STRAPPING LOCATIONS

Figure 1



J5: Test Points — Test points shown on the schematic are located on this jumper.

J6: VCO Clock — This clock is either a 4 MHz (8 inch drive) or 2 MHz (5¼ inch drive) clock.

J7: 8 Inch Ready — When using an 8 inch drive, this strap connects the READY signal to FLP2. When using a 5¼ inch drive, this strap is not connected. Thus, 5¼ drives will always appear ready.

J8: 8 or 5¼ inch Clock — Strap for either a 4 MHz (8 inch) or 2 MHz (5¼ inch) clock.

J9: 5¼ inch drive — This strap is used by Mostek software to determine whether 5¼ or 8 inch drives are used. Only strap J9 for 5¼ inch drives.

J10: Port Address Select — This header block is used to place the FLP2 on any of 32 possible 8-port boundaries. A jumper installed selects the given address bit to be a "zero".

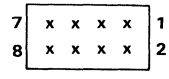
J11: I/O Expand — IOEXP* is normally not used on Mostek boards. Thus, the factory straps pins 2 and 3. If the user desires to use IOEXP*, strap pins 1 and 2 plus pins 3 and 4.

J12: EXT Request Level — This jumper determines whether the EXTREQ input to the FLP2 DMA is active low or active high. For an active low EXTREQ, strap pins 2 and 3 (factory setting); for an active high EXTREQ, strap pins 1 and 2.

One of the major additions to the MDX-FLP2 is the ability to support multiple DMA devices. This capability is accomplished through the implementation of a DMA daisy-chain which adheres to the STD BUS Practice for multiple DMA devices. Connections to the daisy chain are made on connector J2. The MDX-FLP1 does not support this feature, there is generally no need to be concerned with it. It is, however, a feature that one should be aware of especially if one plans to have other mass storage interfaces such as an MDX-SASI2 hard disk interface. Additional information on this topic can be gained from the 1981 STD BUS Specification and Practice which is available from the STD Manufacturing Group. Figure 2 details the pin-out of connector J2.

DAISY CHAIN CONNECTOR

Figure 2



J2 - TOP VIEW

PIN NO.	FUNCTION
1,3,5,7	Ground
2	BAI (Bus ACK In)
4	BAO (Bus ACK Out)
6	No connection
8	External DMA Request Input

The pin-out of J3 is unchanged therefore the cable used between the MDX-FLP1 and the disk devices can also be used with the MDX-FLP2.

SUMMARY

The upgrade from an MDX-FLP1 to an MDX-FLP2 should pose few, if any, problems. The major stumbling blocks are in the various software options the user has at his disposal. Table 1 provides a comprehensive cross-correlation between CPU boards, FLP boards, and software. As indicated above, the hardware should pose no problems. Keep in mind, however, that Mostek software usually expects the system disk drive to be of the 8 inch variety. If it is desired to have a 5¼ inch drive as the system drive, Version 5.0 or greater should be used. Again, this is possible due to the phantom capabilities of these versions.

REFERENCES

MDX-FLP2 Ops Manual #4420262

M/OS-80 Ops Manual #4420064

MOSGEN Ops Manual #4420270

MDX-SASI1: THE HARD DISK INTERFACE APPLICATION NOTE #7

INTRODUCTION

As microcomputer systems have increased in their complexity, so have their mass storage needs also increased. It isn't uncommon to see as much as 10 MB of mass storage attached to an 8-bit microcomputer. Mostek has responded to this need with the introduction of the MDX-SASI-1: a Shugart Associates System Interface (SASI™) bus adapter for the STD-Z80 BUS.

This application note will highlight the features of the SASI bus as well as provide a fairly comprehensive list of the controllers and disk drives which are compatible with the MDX-SASI-1. There will also be a brief discussion of the versions of M/OS-80 which are designed to utilize the capabilities of a hard disk. For more in-depth coverage, the reader should refer to the references listed at the end of this Application Note.

SASI

The Shugart Associates System Interface is an asynchronous, parallel bus designed to allow efficient transfer of data between computers and input/output devices. Due to its asynchronous nature, SASI allows speed independent communications. In general, SASI is oriented towards intelligent I/O devices.

Bus Ports are the lowest level of interface for a SASI system. There may be a maximum of 8 bus ports for a given SASI bus. Attached to the bus ports are bus devices which are in turn attached to the peripheral devices. A 50-pin flat ribbon cable connects the bus devices. There are 9 data lines and 9 control lines. Each of the 18 lines has a ground trace between it and adjacent traces to reduce noise sensitivity. The other traces are reserved for future use. During a communication session one bus device must be the initiator and the other must be the target. Initiators are those bus devices which start an operation on the bus while targets are those bus devices which perform the operation. A bus device may have a fixed role as an initiator or target, or the bus device may be able to assume either role.

SIMPLE SYSTEM
Figure 1

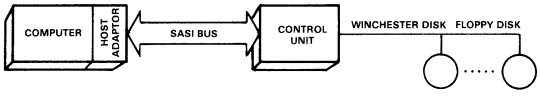


Figure 1 shows a simple SASI system composed of two bus devices; one, the computer, is the initiator and the other, the control unit, is the target. In this figure the MDX-SASI-1 serves as the host adaptor. This is the most common use for the MDX-SASI-1 in STD-Z80 BUS systems.

BASIC TWO CONTROL UNIT SYSTEM
Figure 2

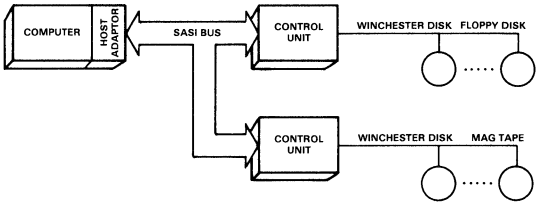


Figure 2 shows a more complex system in which there are two control units. With the MDX-SASI-1, there can be up to 7 control units. SASI also provides for multiple initiators; however, MDX-SASI-1 does not support this feature.

HARDWARE

A hard disk system must be composed of 4 hardware blocks. These blocks are the microcomputer, the bus adaptor, the hard disk controller, and the hard disk. Table 1 is a list of some of the manufacturers of hard disk controllers and drives which Mostek has evaluated and found to be compatible with MDX-SASI-1. This list is not "all inclusive" and the reader is urged to survey the trade journals for other possible vendors. One trend that is beginning to emerge is that of combining the controller with the drive with a SASI Bus Interface. Shugart has introduced a series of 8" drives (floppy and winchester) which support this feature.

Of course, MDX-SASI-1 serves as the bus adaptor. In this capacity it accepts parallel data from the microcomputer and sends it down the 50-pin ribbon cable. The pinout of MDX-SASI-1 allows for the use of a "mass terminated" ribbon cable. Several manufacturers provide the associated hardware to build these cables i.e. Ansley, Winchester, etc.

SASI™ is a trademark of Shugart Associates.

MANUFACTURERS OF HARD DISK CONTROLLERS AND DRIVES
Table 1

DRIVE MFG.	CONTROLLER MFG.		
	5¼"	DTC-510A/520A	XEBEC 1410
	CMS	CM5206, 5412, 5619	SAME
	IMI	5006, 5007, 5012	SAME
	RMS	RMS504, 509, 513	SAME
	SEAGATE	ST506, 412	SAME
	SHUGART	SA602, 604, 606	SAME
	TANDON	TM602S, 603S	SAME
	TI	525/62, /61, /122	SAME
	8"	DTC-101D	DTC-1401
	MEMOREX	101 OEM	
	SHUGART		SA-1000

SOFTWARE

Mostek's M/OS-80 operating system has provisions for adding hard disk storage to a Mostek microcomputer system. Release version MK71012C-81 is designed to support operation with MDX-SASI-1 and the XEBEC 1410 disk controller board. This particular version is generated to utilize the Seagate ST-506 drive or its equivalent.

The hardware set that this version of M/OS-80 is designed around is composed of: MDX-CPU3 or MDX-CPU4, MDX-FLP2, MDX-SASI-1, and the phantom boot ROM. Boot up can take place from either the floppy disk or the hard disk. The system contained on the diskette will support up to four 8" floppy disk drives and two 5¼" floppy disk drives or three 5¼" hard disk drives. There are four other versions supplied on the release diskette which provide for various mixes of floppy (8" and 5¼") and hard disk drives.

For those users wishing to use MDX-SASI-1 in systems which do not contain an operating system, Appendix A shows examples of software routines which can be used to do reads and writes from the hard disk as well as program the MDX-SASI-1 and select the controller. For detailed information about the different modes of data transfer on SASI, consult Shugart's product specification on the SASI bus.

MANUFACTURERS

Computer Memories Corp.
9233 Eaton Ave.
Chatsworth, CA 91311
213-709-6445

Data Technology Corp.
2775 Northwestern Parkway
Santa Clara, CA 95051
408-496-0434

Irwin International
2000 Green Road
Ann Arbor, MI 48105
313-663-3600

Memorex Corp.
San Tomas at Central Expressway
Santa Clara, CA 95052
408-987-1000

Rotating Memory Systems
1701 McCarthy Blvd.
Milpitas, CA 95035
408-946-6692

Seagate Technology
360 El Pueblo Road
Scotts Valley, CA 95066
408-438-6550

Shugart Associates
475 Oakmead Parkway
Sunnyvale, CA 94086
408-733-0100

Tandon Corp.
20320 Prairie
Chatsworth, CA 91311
714-675-2928

Texas Instruments
P.O. Box 202145
Dallas, TX 75220
1-800-231-4717
In TX - 1-800-392-2860

REFERENCES

MDX-SASI-1 Ops Manual #4420263

M/OS-80 Ops Manual #4420064

MOSGEN Ops Manual #4420270

Shugart SASI Product
Specification #30134-0 Rev. A

APPENDIX A

```
;*  MODULE Hardware Interface Routines
;*
;*  Description: This module contains the hardware interface routines required to communicate with MDX-SASI-1. All
;*               routines assume that the AUTO ACK logic (J4) is enabled.
;*
;*  Ver 0.1      10 Nov 81
;*
;*  The following are Port definitions as they exist on the MDX-SASI-1 board:
;*
;*  A7  A6  A5  A4  A3  A2  A1  A0     Function
;*   x   x   x   x   x   x   0   0   PIO Port A Data (Bidirectional)
;*   x   x   x   x   x   x   0   1   PIO Port B Data (Bit Control Mode)
;*   x   x   x   x   x   x   1   0   PIO Port A Control
;*   x   x   x   x   x   x   1   1   PIO Port B Control
;*
;*  Where x = Port Strapping options on the MDX-SASI Board.
;*
;*  Status Control Port Definitions (Port B on PIO):
;*
;*  b7   b6   b5   b4   b3   b2   b1   b0
;*  RES  SEL  ACK  BSY  MSG  C/D  REQ  I/O
;*                                      |-- Input/Output (input)
;*                                 |----- Request (input)
;*                            |---------- Control/Data (input)
;*                       |--------------- Message (input)
;*                  |-------------------- Busy (input)
;*             |------------------------- Acknowledge (input)
;*        |------------------------------ Select (output)
;*   |----------------------------------- Reset (output)
;*
;*  Note that Port B is programmed for BIT CONTROL MODE.
;*  Bits b0-b5 are configured for inputs while b7 and b6 are outputs.
```

VIII

```
;*    Port B Bit Control Constants
RES     EQU     80H     ;Reset
SEL     EQU     40H     ;Select
ACK     EQU     20H     ;Acknowledge
BSY     EQU     10H     ;Busy
MSG     EQU     08H     ;Message
CD      EQU     04H     ;Control/Data
REQ     EQU     02H     ;Request
IO      EQU     01H     ;Input/Output

;*
;*  ┌──────────────────────────────────────────────────────────────────────┐
;*  │                  MDX-SASI-1 Hardware Interface Routine               │
;*  │                                                                      │
;*  │ These routines handle reset, selection, status, command, and data to/from the MDX-SASI-1 board. These are the only
;*  │ routines that directly "toggle bits" on MDX-SASI-1. All routines use polled operation (no interrupts or DMA).
;*  │                                                                      │
;*  └──────────────────────────────────────────────────────────────────────┘


;*    PROCEDURE initialize PIO
;*
;*    Description: Initializes the Z80-PIO for polled operation
;*                 with the MDX-SASI-1 board.
;*
;*    Ver 0.1      26 Sep 81
;*
;*    Entry:       C - Base address of MDX-SASI-1 board.
;*
;*    Exit:        AF is changed.

INITPIO     EQU $

;   Set Port A of the PIO for bidirectional (Mode 2) operation.
            INC  C              ;Point to Port A control register
            INC  C
            LD   A, 8FH         ;Program Port A for
            OUT  (C), A         ;       mode 2 operation

;   Set Port B of the PIO for bit control (Mode 3) operation:
            INC  C              ;Point to Port B control register
            LD   A,OCFH         ;Program Port B for
            OUT  (C), A         ;       mode 3 operation

;   For Mode 3, the next byte must set the I/O regsiter bits.
;   Bits 7 and 6 are outputs. Bits 5, 4, 3, 2, 1, and 0 are inputs.
            LD   A, 00111111B
            OUT  (C), A

;*  Initialize MDX-SASI-1 board...
            DEC  C              ;Point to Data Port B
            DEC  C
            XOR  A              ;Deassert all control lines
            OUT  (C), A

            DEC  C              ;Point to Data Port A
            IN   A, (C)         ;Dummy read to enable MDX-SASI-1

;*  That's all for now...
            RET
```

```
;*    END procedure initialize PIO

;*    PROCEDURE Reset
;*
;*    Description: Resets the controller connected to the MDX-SASI-1.
;*
;*    Ver 0.1       26 Sep 81
;*
;*    Entry:        C - Base address of MDX-SASI-1 board.
;*
;*    Exit:         If A is 0, Then no errors.
;*                  If A is non 0, Then A contains the error code.

RESET   EQU $
        INC  C          ;Point to Port B

        LD   A,RES      ;Assert Reset Signal
        OUT (C), A

        XOR A           ;Remove Reset signal
        OUT (C), A

;   Check if all status lines are deasserted
        IN   A, (C)
        CP   0          ;If status lines deasserted
        JR   Z, OUT     ;       THEN get out
        LD   A, 40H     ;ELSE get error code

OUT:    DEC  C          ;Restore original value of C

        RET             ;Enough for now...

END PROCEDURE Reset

;*    PROCEDURE select

;*    Description: Selects the controller connected to the MDX-SASI-1.
;*
;*    Ver 0.1       26 Sep 81
;*
;*    Entry:        A - ID of controller (normally bit 0 set to 1)
;*                  C - Base address of MDX-SASI-1 board
;*
;*    Exit:         AF is changed.

SELECT  EQU $

        OUT (C), A      ;Assert ID bit (normally bit 0)

        INC  C          ;Point to Port B

        LD   A, SEL     ;Assert Select
        OUT (C), A

WAIT4:  IN   A,(C)      ;While
        AND BSY         ;       busy not asserted
        JR   Z,WAIT4    ;           wait

        XOR A           ;Deassert Select
        OUT (C), A
```

```
        DEC  C          ;Restore original value of C
        RET             ;       and exit

;*  END PROCEDURE select

;*  PROCEDURE block read

;*  Description: Reads a block of up to 256 bytes from the MDX-SASI-1 board.
;*
;*  Ver 0.1       26 Sep 81
;*
;*  Entry:        B - Byte count (Note that a value of 0 is 256).
;*                C - Base address of MDX-SASI-1 board.
;*                HL - Points to first byte of buffer area.
;*
;*  Exit:         A is changed.
;*                B is zero.
;*                HL points one past the last byte read.
;*

BLKRD   EQU $

LOOPO:  INC  C          ;Point to Port B

WAITO:  IN   A,(C)      ;WHILE
        AND ACK         ;       acknowledge asserted
        JR   NZ,WAITO   ;         wait

WAIT1:  IN   A, (C)     ;WHILE
        AND REQ         ;       request not asserted
        JR   Z,WAIT1    ;         wait

        DEC  C          ;Point to Port A

        INI             ;Read a byte

        JR   NZ,LOOPO   ;   and keep-on till done

        RET             ;That's all for now

;*  END PROCEDURE block read
```

```
;*    PROCEDURE block write
;*
;*    Description: Sends a block of up to 256 bytes to the MDX-SASI-1 board (Polled).
;*
;*    Ver 0.1        26 Sep 81
;*
;*    Entry:         B - Byte count (Note that a 0 implies 256 bytes).
;*                   C - Base address of MDX-SASI-1 board.
;*                   HL - First byte of block.
;*
;*    Exit:          A is changed.
;*                   B is zero.
;*                   HL points one past the last byte sent.
;*
BLKWR   EQU $

LOOP1:  INC  C          ;Point to Port B Data

WAIT2:  IN   A, (C)     ;WHILE
        AND ACK         ;     acknowledge asserted
        JR   NZ,WAIT2 ;       wait

WAIT3   IN   A, (C)     ;WHILE
        AND REQ         ;     request not asserted
        JR   Z,WAIT3  ;       wait

        DEC C           ;Point to Port A data

        OTI             ;Send a byte

        JR   NZ,LOOP1 ;   and keep-on till done

        RET             ;Let's get out of here

;*    END PROCEDURE block write
```

MDX-FLP2 VS. MDX-FLP1:HARDWARE AND SOFTWARE ISSUES APPLICATION NOTE #8

INTRODUCTION

With the introduction of the MDX-FLP2, the MDX-FLP1 will become increasingly less cost effective due to the performance increases of the MDX-FLP2. With this in mind, this application note will detail the differences between these two products so that present users of MDX-FLP1 can make the move to MDX-FLP2 with a minimum of effort .

HARDWARE

The major differences between the MDX-FLP1 and MDX-FLP2 are in the areas of the floppy controller chip, jumper options, I/O port definitions, and miscellaneous board differences.

Floppy Chip

Probably the biggest single difference between these two products is the presence of a Western Digital 1771 on MDX-FLP1 and a Western Digital 1797 on MDX-FLP2. The 1771 is a single-sided, single-density floppy controller/formatter while the 1797 supports both double-density and double-sided operation. This is not to imply that the 1797 doesn't support single-density and single-sided operation as well.

The command formats for both the 1771 and 1797 are virtually identical. Tables 1 and 2 provide a summary of the command formats for the 1771 and 1797, respectively. The only differences are as follows:

1 The 1797 allows the selection of a particular side with bit 1 of Type II and Type III commands. The 1771 doesn't support side select.

2. On the Write Sector command the 1771 allows the selection of 4 different data address marks where as the 1797 allows only 2.

3. The Read Track command of the 1771 may be conditionally synchronized with each address mark through the use of bit 0 of this command. The 1797 always synchronizes with the address marks.

4. Type III commands of the 1797 can have the head settling delay conditionally enabled. The 1771 always enables the delay except for the read address command on which it is an option.

5. On the Type 1 commands the step rate select bits are assigned differently. Table 3 shows the differences.

1771 COMMAND SUMMARY
Table 1

		BITS							
TYPE	**COMMAND**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	1	0	s
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

1797 COMMAND SUMMARY
Table 2

		BITS							
TYPE	**COMMAND**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	b	E	U	0
II	Write Sector	1	0	1	m	b	E	U	a_0
III	Read Address	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0

STEP RATES

Table 3

STEP RATE R_1 R_0	8"		5¼"	
	1797	1771	1797	1771
00	3 ms	6 ms	6 ms	12 ms
01	6 ms	6 ms	12 ms	12 ms
10	10 ms	10 ms	20 ms	20 ms
11	15 ms	20 ms	30 ms	40 ms

Jumper Options

There is a great deal of similarity between the jumper options of the MDX-FLP1 and the MDX-FLP2. Table 4 summarizes the correlation between MDX-FLP1 and MDX-FLP2. The Timing Resistor (R2) on FLP2 is socketed allowing easy replacement when adjusting the timing of U2 (74LS221) for the optimum Head Load Timing delay required by the drive being used.

If R2 equals
6.2 K Ω $\overline{HLT}$ = 43 ms
9.1 K Ω $\overline{HLT}$ = 64 ms
12 K Ω $\overline{HLT}$ = 84 ms

The notable differences are lack of Automatic Precompensation on FLP1, no support of IOEXP* on FLP1, and no forced single/double selection on FLP2.

I/O Ports

Ports 0, 1, 4, 5, 6, and 7 are the same for FLP1 and FLP2. The only difference being in a few of the status bits on some commands. Ports 2 and 3 have several differences. The drive select bits of Port 3 are the same for both FLP1 and FLP2. FLP2 doesn't have the side select bit but it does have both a density control bit and a 1797 reset bit in Port 3. The density control bit is in location b7 and the reset is in location b6.

FLP1, on the other hand, has bit b4 assigned as the side select. Port 2, bits 0, 1, and 5 are identical for both FLP1 and FLP2. FLP2 has Port 2, bit b6 assigned as a "zero" where as FLP1 has this bit assigned as a "one". This feature can be used by software to determine whether a FLP1 or FLP2 is present.

ADDITIONAL INFORMATION

One of the major additions to the MDX-FLP2 is the ability to support multiple DMA devices. This capability is accomplished through the implementation of a DMA daisy-chain which adheres to the STD BUS Practice for multiple DMA devices. Connections to the daisy chain are made on connector J2. Since the MDX-FLP1 is unable to support this feature, there is generally no need to concern oneself with it. It is, however, a feature that one should be aware of especially if one plans to have other mass storage interfaces such as an MDX-SASI2 hard disk interface. Additional information on this topic can be gained from the 1981 STD BUS Specification and Practice which is available from the STD Users Group.

J2, on the FLP2, is also used to provide for an external DMA request. This feature allows the DMA chip on the FLP2 to be shared with another peripheral controller such as the MDX-SASI1 hard disk interface. Figure 1 details the pin-out of connector J2.

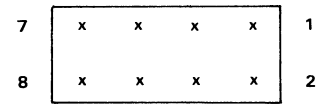
JUMPER CORRELATION

Table 4

	FLP1	FLP2
ADDRESS:		
BIT 7	E9	J10 (10,9)
6	E10	J10 (8,7)
5	E11	J10 (6,5)
4	E12	J10 (4,3)
3	E13	J10 (2,1)
FLOPPY CONTRL. CLOCK		
5¼"	E1	J8 (2,1)
8"	E2	J8 (4,3)
HEAD LOAD DELAY		
5¼"	E8 (OUT)	R_2 is
8"	E8 (IN)	socketed
DRIVE ID		
5¼"	E3 (IN)	J9 (IN)
8"	E3 (OUT)	J9 (OUT)
# SIDES		
SINGLE	E4 (IN)	N/A (bit 0 of Port 2,
DOUBLE	E4 (OUT)	"0" = single sided
		"1" = double sided)
DATA SEP.		
5¼"	E5 (OUT)	J6 (4,3)
8"	E5 (IN)	J6 (2,1)
AUTO PRECOMP		
5¼"	N/A	J4 (OUT)
8"	N/A	J4 (IN)
IOEXP		
If using	N/A	J11 (1,2 + 3,4)
If not using	N/A	J11 (2,3)
EXTREQ LEVEL		
HIGH	N/A	J12 (2,1)
LOW	N/A	J12 (2,3)

DMA DAISY CHAIN CONNECTOR

Figure 1



J_2 - Top View

PIN NUMBER	FUNCTION
1, 3, 5, 7	Ground
2	BAI (Bus ACK In)
4	BAO (Bus ACK Out)
6	No connection
8	External DMA Request Input

An additional feature of FLP2 is the ability to run at system speeds of 4 MHz. This speed improvement does not speed up the transfer rate from the drive but it does allow a mass storage device to be interfaced to a 4 MHz system.

The pin-out of J3 (J2-FLP1) is unchanged except for pin 48, side select; therefore, the cable used between the MDX-FLP1 and the disk devices can also be used with the MDX-FLP2. On FLP1, pins 14 and 16 are tied together and assigned as the side select control line. FLP2, on the other hand, has pins 14 and 48 tied together for this same function. In general, this will not cause a problem unless 8" drives which provide an internal data separator are used. (Shugart model #851.) These drives assign pin 48 as the data separator output to the controller. If one of these drives is used, the etch run going to pin 48 should be cut to prevent damage to either the FLP2 or the drive. Figure 2 shows the pin-out of J3 (J2-FLP1) with differences noted between FLP1 and FLP2.

The final hardware difference is in the area of the reset circuitry. FLP1 gets its reset from the SYSRESET* line directly. FLP2 gets its reset directly from SYSRESET* for everthing except the floppy controller chip. The chip gets its reset from one of the I/O port bits which is initialized to a "zero" by SYSRESET*. Therefore, the FLP2 comes up in the reset state and must be taken out of reset by outputing a "one" to bit b6 of Port 3. FLP1 comes up in the initialized state.

DRIVE INTERFACE

Figure 2

Signal	Description	Pin Number
Drive Select 1,2,3,4	Output	26,28,30,32
Side Select	Output	14,48 (see note), 16*
Step	Output	36
Write Data	Output	38
Write Gate	Output	40
Direction	Output	34
Head Load	Output	18
Read Data	Input	46
Index	Input	24 (5 in.) or 20 (8 in.)***
Track 00	Input	42
Write Protect	Input	44
Drive Ready	Input	22
2 Sided	Input	10**

NOTE: Some 8" drives have an optional DATA SEPARATOR output on pin 48. If this is true on your drive, cut the etch on the FLP2 board going to pin 48 on J3.

* Pin 14 & 16 (FLP1) Pin 14 & 48 (FLP2)
** only on FLP2
*** Pins 20 and 24 are common (tied together) on FLP1 and FLP2

SOFTWARE

Software differences between FLP2 and FLP1 are relatively minor. Most of the differences have been detailed in the hardware section. In summary those differences are the side select, step rate assignment, data address marks, reset control, and head settling delay. The lack of 4 data address marks on FLP2 shouldn't be a problem because most software only uses the Data Mark (FB) and the Deleted Data Mark (F8) both of which are supported by FLP2. The other two supported by FLP1 are user defined and may vary from routine to routine.

DUAL-DENSITY FORMAT

Table 5

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6
1	FC (Index Mark)
50*	4E
12	00
3	F5
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01
1	F7 (2 CRCs written)
22	4E
12	00
3	F5
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

* Write bracketed field 26 times
** Continue writing until FD179X interrupts out. Approx. 598 Bytes.

VIII

Even though the software differences between FLP2 and FLP1 are not very large, the implications of double-density operation versus single-density operation should not be underestimated. First of all, the data comes off the disk twice as fast as it does for single-density operation. This increased speed means that for programmed tranfers the software must be more efficient if there is to be no lost data. Secondly, the buffers must be twice the size they are for single-density operation because the sectors are twice as big.

Another area that the programmer must be aware of is that of the different format information required for single- and double-density operation. The single-density formats for FLP1 and FLP2 are identical. Table 5 shows the format information for IBM System 34 double-density operation. A few notable points are the sector length field (field after sector #), increased length of all gaps, and the different values placed into the gaps. Table 6 shows the values placed into the sector length field and what they mean. Note that this table is only valid when bit b3 of Type II commands is a "one". If this bit is a "zero", then the sector length field is treated as non-IBM format and it is beyond the scope of this application note to discuss all the possibilities of non-standard formats.

SUMMARY

It is hoped that this application note has provided the user with sufficient information to make the switch from MDX-FLP1 to MDX-FLP2. The majority of the changes are in hardware and should have minimum effect on the software for those users who are just using FLP2 as a replacement for FLP1. Again, to recap the areas of importance:

1. Remember that side selection takes place in the chip for FLP2 and on the board for FLP1.

2. 5¼" drives will always appear ready to FLP2.

3. Be aware of the slight differences between command and status information.

4. There is a fixed head settling delay for FLP2 which may require an additional software delay for 5¼" drives unless the value of R2 is changed to increase the setting delay.

SECTOR LENGTH FIELD DEFINITION
Table 6

SECTOR LENGTH TABLE	
Sector Length Field (Hex)	**Number of Bytes in Sector (Decimal)**
00	128*
01	256**
02	512
03	1024

* Single density value
** Double density value

REFERENCES

FD1771-01 Data Sheet
Western Digital Corp.

FD179X-02 Data Sheet
Western Digital Corp.

MDX-FLP1 Ops Manual #4420032

MDX-FLP2 Ops Manual #4420262

Western Digital Corp.
2445 McCabe Way
Irvine, California 92714
(714) 557-3550

STD Users Group
Bill-Shields - Chairman
8697 Frobisher St.
San Diego, California 92126
(714) 297-1353

STD Manufacturers Group
Matt Biewer - Chairman
Pro-Log Corp.
2411 Garden Rd.
Monterey, California 93940

MDX-CPU3/4 I/O DRIVERS APPLICATION NOTE #10

SCOPE:

This application note will detail how to control the serial port, parallel port, and the timer channels available on the MDX-CPU3 and MDX-CPU4.

INTRODUCTION:

The purpose of this application note is to help the first time user of the MDX-CPU3/4 interface the serial and parallel ports quickly. Sample drivers are provided and can be modified to suit the user's particular needs.

INTERFACING THE SERIAL PORT (J3)

The serial communication signals to perform an RS-232-C type interface have been buffered and pinned out to a 26-pin connector in such a manner that a flat ribbon mass terminated type connector could be used. Hardware and software considerations follow below.

HARDWARE:

Table 1 lists the connections required for the serial port.

SERIAL PORT (J3) PINOUT
Table 1

MDX-CPU3/4 (J3) Pin #	Signal	Z80-STI (MK3801) Pin #		SIGNAL DIRECTION Relative to CPU3/4
1	GND	NC		—
2	RX (BB)	38	SI &	Input
		11	I3	Input
3	TX (BA)	37	50	Output
4	RTS (CA)	9	I1	Input
5	CTS (CB)	10	I2	Output
6	DSR (CC)	13	I5	Output
7	GND	NC		—
8	RLSD (CF)	14	I6	Output
20	DTR (CD)	12	I4	Input

MATING CONNECTORS (P3) FOR J3

Flat Ribbon Type:
1) T & B Ansley # 609-2600M
2) Winchester Electronics #51-1126-00
3) 3M #3399-6000

Discrete Wire Type:
1) Winchester Electronics
Housing = #PGB-13-A
Contacts = #100-72020S (20-24AWG)
(Crimp) #100-72026S (26-30AWG)

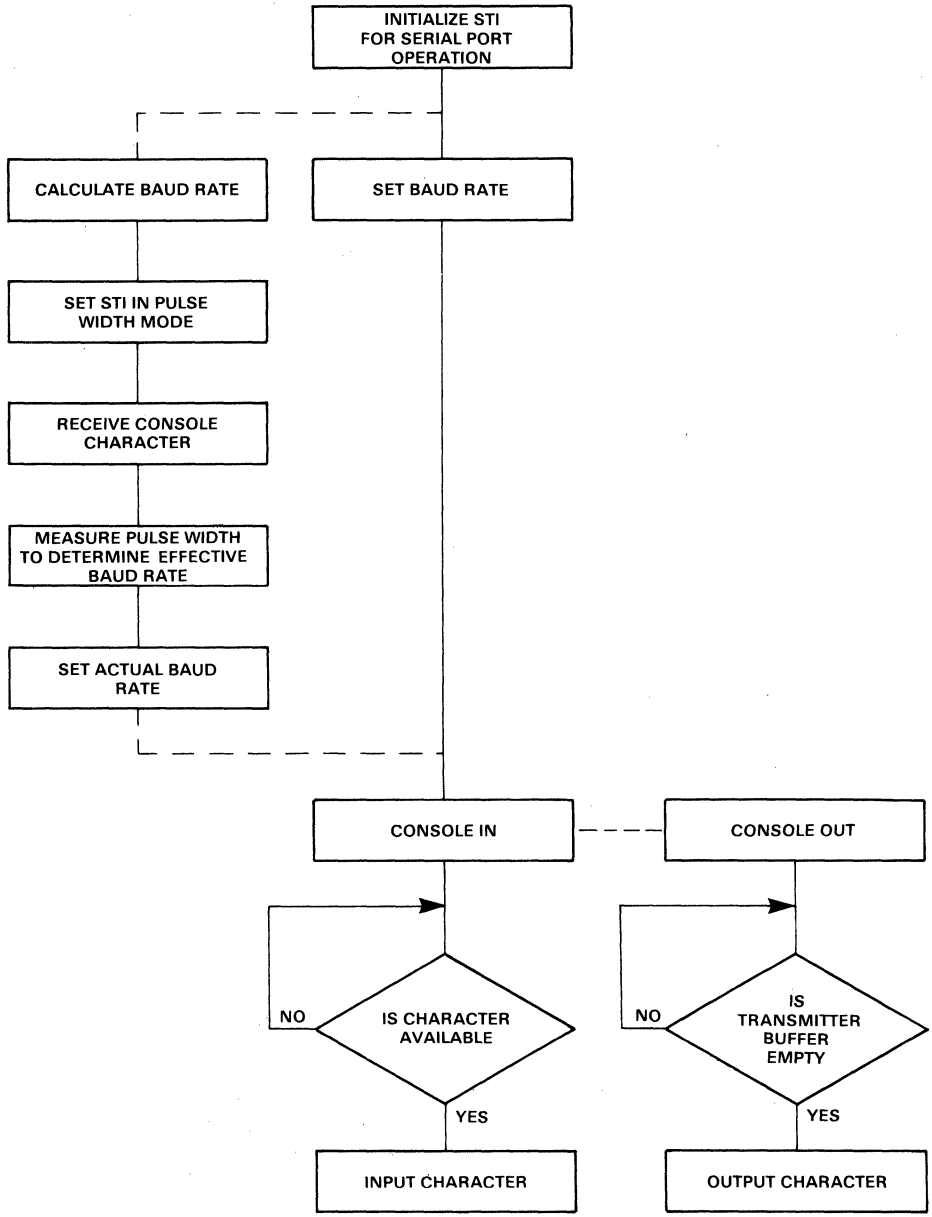
INTERFACING THE PARALLEL PORT (J2)

The parallel output port has been designed to support a parallel Centronics type printer interface directly. The port has been pinned out to a 26-pin connector in such a manner that a flat ribbon mass terminated type connector could be used on both ends. Hardware and software considerations follow below.

HARDWARE:

Table 2 lists the connections required for the parallel port.

Figure 1


INITIALIZE STI FOR SERIAL PORT OPERATION
CALCULATE BAUD RATE
SET BAUD RATE
SET STI IN PULSE WIDTH MODE
RECEIVE CONSOLE CHARACTER
MEASURE PULSE WIDTH TO DETERMINE EFFECTIVE BAUD RATE
SET ACTUAL BAUD RATE
CONSOLE IN
CONSOLE OUT
NO
IS CHARACTER AVAILABLE
YES
INPUT CHARACTER
NO
IS TRANSMITTER BUFFER EMPTY
YES
OUTPUT CHARACTER

PARALLEL PRINTER PORT (J2) PINOUT

Table 2

MDX-CPU3/4 (J2) Pin #	Signal	Z80-STI (MK3801) Pin #		SIGNAL DIRECTION Relative to CPU3/4
1	/STB	2	TBO	Output
2	PD0	21	D0	Output
3	PD1	22	D1	Output
4	PD2	23	D2	Output
5	PD3	24	D3	Output
6	PD4	25	D4	Output
7	PD5	26	D5	Output
8	PD6	27	D6	Output
9	PD7	28	D7	Output
10	NC	—		—
11	BUSY	8	I0	Input
12	PE	15	I7	Input
13	NC	—		—
14	GND	—		—
15	GND	—		—
16-26	NC	—		—

MATING CONNECTORS (P2) FOR J2

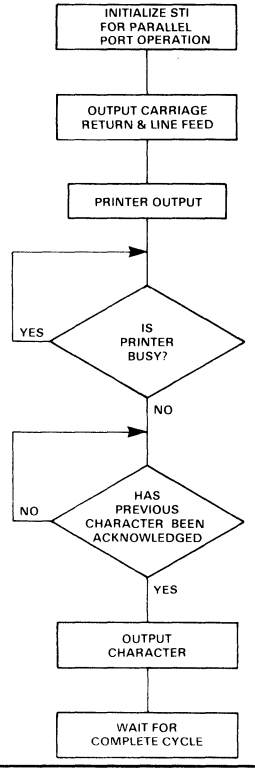
Same as those for J3

MATING CONNECTOR FOR PRINTER (36-PIN CENTRONICS TYPE)

Flat Ribbon Type: 1) 3M #3366-1001 (Bail Mount)

PARALLEL PRINTER PORT

Figure 2



INTERFACING THE TIMERS

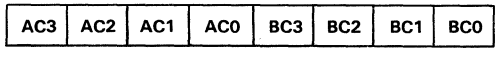
There are four timers associated with the STI chip onboard the MDX-CPU3/4. Timers A & B are full function timers that can perform basic delay function, event counting, or pulse measurement. Timers C & D on the other hand are delay timers only. The timer outputs have been dedicated as indicated below.

Z80-STI (MK3801) Pin #		CONNECTOR Pin #
1	TAO	J3-Pin 18 (/TAO) Available for user
2	TBO	J2-Pin 1 (/TBO) Printer Strobe
3	TCO	J3-Pin 11 (/TCO) Available for user
4	TDO	No external conn. Baud Rate Measurement

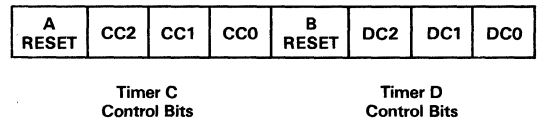
TIMER GENERAL COMMENTS

- ☐ All timer outputs are forced low by device (board) RESET.
- ☐ Only timer A & B outputs can be forced low by setting the A or B register RESET bit respectively. If this method is used, the other bits must be maintained in the correct state as well.
- ☐ Timer Data Registers and the main counters will maintain their contents during a RESET.
- ☐ No counting can occur while timer is stopped.
- ☐ Timer contents remain unaltered while stopped.
- ☐ Residual count in timer is lost when reloaded with a new value.
- ☐ In the Delay Mode, the prescaler is always active.
- ☐ In the Event Count Mode, the prescaler is disabled.
- ☐ Timer count will decrement to 01---then reload value from data register and toggle output state, during what normally would be count 00.
- ☐ Two time-out pulses are required for one complete output cycle.
- ☐ If the timer is stopped, the value loaded into the data register will also be loaded into the counter.
- ☐ If the timer is running, data must be written while the timer is not counting through 01H.
- ☐ If timer is running, and the prescaler is changed, the first output pulse will be incorrect ($0 \geq TO \leq 200$ clock cycles).

TIMER A & B CONTROL REGISTER (TABCR) PORT 9.



TIMER C & D CONTROL REGISTER (TCDCR) PORT 7.



CONTROL BIT DEFINITION

C3	C2	C1	C0	COMMENT
0	0	0	0	Timer Stopped
0	0	0	1	Delay Mode, ÷ 4 Prescale
0	0	1	0	Delay Mode, ÷ 10 Prescale
0	0	1	1	Delay Mode, ÷ 16 Prescale
0	1	0	0	Delay Mode, ÷ 50 Prescale
0	1	0	1	Delay Mode, ÷ 64 Prescale
0	1	1	0	Delay Mode, ÷ 100 Prescale
0	1	1	1	Delay Mode, ÷ 200 Prescale
1	0	0	0	Event Count Mode
1	0	0	1	Pulse Width Mode, ÷ 4 Prescale
1	0	1	0	Pulse Width Mode, ÷ 10 Prescale
1	0	1	1	Pulse Width Mode, ÷ 16 Prescale
1	1	0	0	Pulse Width Mode, ÷ 50 Prescale
1	1	0	1	Pulse Width Mode, ÷ 64 Prescale
1	1	1	0	Pulse Width Mode, ÷ 100 Prescale
1	1	1	1	Pulse Width Mode, ÷ 200 Prescale

SOFTWARE:

General Comments

The following assumptions are made:

1. MDX-CPU3 clock frequency is 3.6864 MHz. (standard)
2. Timer D is used for Baud rate generation.
3. Timer B is used for Printer Strobe.

Direct Registers are addressed as:

```
IN    A, (STI+register-name)
OUT   (STI+register-name),A
```

Indirect Registers are addressed as:

```
LD    A,(Interrupt-vector.AND.11100000B)+register
                                          -name
OUT   (STI+PVR),A
IN    A,(STI+IDR)
or
LD    A,(Interrupt-vector.AND.11100000B)+register
                                          -name
OUT   (STI+PVR),A
LD    A,register-value
OUT   (STI+IDR),A
```

STI CHIP REGISTER DEFINITIONS

```
STI         EQU     0B0H        ; STI BASE PORT ADDRESS
;
;           DIRECT REGISTERS
;
IDR         EQU     0           ; Indirect Data Register
GPIP        EQU     1           ; General purpose I/O Interrupt
IPRB        EQU     2           ; Interrupt Pending Register B
IPRA        EQU     3           ; Interrupt Pending Register A
ISRB        EQU     4           ; Interrupt In-Service Register B
ISRA        EQU     5           ; Interrupt In-Service Register A
IMRB        EQU     6           ; Interrupt Mask Register B
IMRA        EQU     7           ; Interrupt Mask Register A
PVR         EQU     8           ; Pointer/Vector Register
TABCR       EQU     9           ; Timers A and B Control Register
TBDR        EQU     10          ; Timer B Data Register
TADR        EQU     11          ; Timer A Data Register
UCR         EQU     12          ; USART Control Register
RSR         EQU     13          ; Receiver Status Register
TSR         EQU     14          ; Transmitter Status Register
UDR         EQU     15          ; USART Data Register
;
;
;           INDIRECT REGISTERS
;
SCR         EQU     0           ; Sync Character Register
TDDR        EQU     1           ; Timer D Data Register
TCDR        EQU     2           ; Timer C Data Register
AER         EQU     3           ; Active Edge Register
IERB        EQU     4           ; Interrupt Enable Register B
IERA        EQU     5           ; Interrupt Enable Register A
DDR         EQU     6           ; Data Direction Register
TCDCR       EQU     7           ; Timers C and D Control Register
;
;           BIT DEFINITIONS
;
PTRACK      EQU     0           ; Input Printer Acknowledge
PTRBSY      EQU     7           ; Input Printer Empty
;
RTS         EQU     1           ; Input Request To Send
CTS         EQU     2           ; Output Clear To Send
;
RX          EQU     3           ; Input Receive serial data
;                                 (for Baud rate measurement)
DTR         EQU     4           ; Input Data Terminal Ready
DSR         EQU     5           ; Output Data Set Ready
;
RSLD        EQU     6           ; Output Received Line Signal Detect
;
DDRVAL      EQU     01100100B   ; Value for DDR Register
GPIVAL      EQU     00000000B   ; Idle values for General Purpose Port
;
PTR         EQU     0D0H        ; Output Printer Data Port Address
;
BIT0        EQU     1
BIT1        EQU     2
BIT2        EQU     4
BIT3        EQU     8
BIT4        EQU     16
```

```
BIT5        EQU         32
BIT6        EQU         64
BIT7        EQU        128
;
;           ASCII SPECIAL CHARACTERS
;
NUL         DEFL        00H
ETX         DEFL        03H
EOT         DEFL        04H
BEL         DEFL        07H
BS          DEFL        08H
HT          DEFL        09H
LF          DEFL        0AH
FF          DEFL        0CH
CR          DEFL        0DH
NAK         DEFL        15H
CAN         DEFL        18H
ESC         DEFL        1BH
DEL         DEFL        7FH
;
;
;           INITIALIZE THE STI CHIP
;
;
STINIT:
            DI                          ;  just in case
            LD          A,DDR
            OUT         (STI+PVR),A
            LD          A,DDRVAL        ;  set up the general purpose port
            OUT         (STI+IDR),A
;
            LD          A,GPIVAL        ;  and set up idle values
            OUT         (STI+GPIP),A
;
;
;
;           FIXED BAUD RATE DRIVER
;
;
;
            LD          A,TCDCR
            OUT         (STI+PVR),A
            LD          A,00000001B     ;  timer D divide by 4 prescale
            OUT         (STI+IDR),A
;
            LD          A,TDDR
            OUT         (STI+PVR),A
            LD          A,3             ;  then divide by 3
            OUT         (STI+IDR),A     ;  the output toggles for each output
;                                       ;  giving an effective divide by 2
;
;                                       ;  the USART will divide by 16
;                                       ;
;                                       ;  thus 3.6864/4/3/2/16 = 9600
;                                       ;
            LD          A,10001000B     ;  USART control: divide by 16
;                                       ;                 8-bit word
;                                       ;                 async 1 stop
;                                       ;                 no parity
```

```
        OUT     (STI+UCR),A
;
        LD      A,00000001B  ; enable receiver
        OUT     (STI+RSR),A
        IN      A,(STI+RSR)  ; and clear any flags
;
        LD      A,00000101B  ; enable transmitter
        OUT     (STI+TSR),A
        IN      A,(STI+TSR)  ; and clear any flags
;
        LD      A,00000000B  ; disable all interrupts
        OUT     (STI+IERA),A
        OUT     (STI+IERB),A
;
        LD      A,CR
;
        CALL    TTYOUT
        LD      A,LF
        CALL    TTYOUT
;
;
;
;
;  AUTOMATIC BAUD RATE DETERMINATION
;
;
;
        LD      A,AER        ; Set active register for pulse
        OUT     (STI+PVR),A  ; width measurement of serial in
        XOR     A
        OUT     (STI+IDR),A
;
        OUT     (STI+TABCR),A ; Stop timer (just in case)
;
        OUT     (STI+TBDR),A ; Initialize counter value
;
        LD      A,00001101B  ; set up pulse width mode
        OUT     (STI+TABCR),A ;
;
        LD      A,IERA       ; set up interrupts in STI
        OUT     (STI+PVR),A
        XOR     A            ; clear previous interrupt
        OUT     (STI+IDR),A
        OUT     (STI+IMRA),A
        LD      A,00000001B
        OUT     (STI+IDR),A
;
        LD      A,IERB
        OUT     (STI+PVR),A
        XOR     A            ; clear previous interrupt
        OUT     (STI+IDR),A
        OUT     (STI+IMRB),A
        LD      A,00001000B
        OUT     (STI+IDR),A
;
LOOP1:  IN      A,(STI+IPRB) ; look for end of pulse
        AND     BIT3
        JR      NZ,DONE1     ; if end of pulse, exit
;
```

```
;
;               PRINTER INITIALIZATION DRIVER
;
;
;
PTRINT:
                LD      A,00000000B  ;  Stop the timer (just in case)
                OUT     (STI+TABCR),A
                LD      A,00001000B  ;  Force the timer low
                OUT     (STI+TCDCR),A
                LD      A,16         ;  16 x 10 x 271 nanosec = 43 msec
                OUT     (STI+TBDR),A
                LD      A,00000010B
                OUT     (STI+TABCR),A ;  intent is that approx 43 msec
;                                     ;  the printer strobe (timer
                                      ;  will go high
;
WAIT1:
                IN      A,(STI+TBDR)
                CP      15
                JR      NZ,WAIT1     ;  Wait for first cycle to stop
;
WAIT2:
                IN      A,(STI+TBDR)
                CP      16
                JR      NZ,WAIT2     ;  Wait for second cycle
;
                LD      A,00000000B  ;  Then turn off the timer
                OUT     (STI+TABCR),A
;
                LD      A,CR
                CALL    PTROUT
                LD      A,LF
                CALL    PTROUT
;
                RET
;
;
```

```
;
;
;               PRINTER OUTPUT DRIVER
;
;
;
;
PTROUT:
                PUSH    AF           ;  Save Character
;
BUSY:
                IN      A,(STI+GPIP)
                BIT     PTRBSY,A     ;  see if printer is busy
                JR      Z,BUSY       ;  make this paper empty
;
ACK:
                IN      A,(STI+GPIP)
                BIT     PTRACK,A     ;  see of previous ack is finished
                JR      NZ,ACK
;
```

```
                POP     AF
                OUT     (PTR),A         ;  now output the character
;
                PUSH    AF              ;  save it again
;
                LD      A,0             ;  stop the timer (just in case)
                OUT     (STI+TABCR),A
                LD      A,16            ;  16 x 10 x 271 nanosec = 43 msec
                OUT     (STI+TBDR),A
                LD      A,00000010B
                OUT     (STI+TABCR),A   ;  intent is that in approx 43 msec
;                                       ;  the printer strobe (timer b output)
                                        ;  will go low for approximately
;                                       ;  and then go high again
WAITT1:
                IN      A,(STI+TBDR)
                CP      14
                JR      NZ,WAIT1        ;  wait for first cycle to start
WAITT2:
                IN      A,(STI+TBDR)
                CP      15
                JR      NZ,WAITT2       ;  wait for second cycle to start
;
                LD      A,0
                OUT     (STI+TABCR),A   ;  then turn off timer
;
                POP     AF
                RET
```

SAMPLE PROGRAM

The example program below is a simple one. It inputs a character from the CRT console, echos the character back out to the CRT console and outputs the character to the printer.

```
                .Z80                    ;  Use Z80 Code
0000'           ASEG
00B0            STI             EQU     0B0H        ;  STI BASE PORT ADDRESS
                ;
                DIRECT REGISTERS
                ;
0000            IDR             EQU      0
0001            GPIP            EQU      1
0002            IPRB            EQU      2
0003            IPRA            EQU      3
0004            ISRB            EQU      4
0005            ISRA            EQU      5
0006            IMRB            EQU      6
0007            IMRA            EQU      7
0008            PVR             EQU      8
0009            TABCR           EQU      9
000A            TBDR            EQU     10
000B            TADR            EQU     11
000C            UCR             EQU     12
```

```
                IN      A,(STI+IPRA)
                AND     BIT0
                JP      Z,LOOP1
;
B110:           LD      B,105           ;  if overflow, then 110 Baud
                JR      DONE2
;
;
DONE1:          IN      A,(STI+TBDR)    ;  get pulse count counted down
                NEG                     ;  from 0
                SRL     A               ;  divide by 2 due to timer output
;
;
                LD      B,11000000B     ;  prepare to correct value
;
LOOP2:          RLCA
                JR      C,DONE2
                SRL     B
                JR      LOOP2
;
DONE2:          LD      A,TDDR          ;  output corrected value to
                OUT     (STI+PVR),A     ;  Baud rate generator
                LD      A,B
                OUT     (STI+IDR),A
;
                LD      A,TCDCR         ;  output prescaler
                OUT     (STI+PVR),A
                LD      A,B
                CP      105             ;  110 Baud?
                LD      A,00000010B     ;  divide by 10
                JR      Z,DONE3
                LD      A,00000001B     ;  else divide by 4
;
DONE3:          OUT     (STI+IDR),A
;
                LD      A,B
                CP      105             ;  110 or higher?
;
                LD      A,10011000B     ;  USART control: divide by 16
                                        ;                 8 bit word
;                                       ;                 async 2 stop bit
;                                       ;                 no parity
;
                JR      Z,DONE4         ;  skip around if 110 baud
;
;
                LD      A,10001000B     ;  USART control: divide by 16
;                                       ;                 8 bit word
;                                       ;                 async 2 stop bit
;                                       ;                 no parity
;
;
;
DONE4:          OUT     (STI+UCR),A
;
                LD      A,00000001B     ;  enable receiver
                OUT     (STI+RSR),A
                IN      A,(STI+RSR)     ;  and clear any flags
;
```

```
                LD      A,00000101B  ; enable transmitter
                OUT     (STI+TSR),A
                IN      A,(STI+TSR)  ; and clear any flags
;
                LD      A,IERA
                OUT     (STI+PCR),A
                XOR     A            ; disable interrupts
                OUT     (STI+IDR),A
                OUT     (STI+IMRA),A
                LD      A,IERB
                OUT     (STI+PVR),A
                XOR     A            ; disable interrupts
                OUT     (STI+IDR),A
                OUT     (STI+IMRB),A
;
                CALL    TTYIN        ; flush out that first input
;                                    ; character
                RET
;
;
;
;
;               CONSOLE-IN DRIVER
;
;
;
TTYIN:
                IN      A,(STI+RSR)  ; Input from receive status
                BIT     7,A          ; Bit 7 is "receive char available
                JR      Z,TTYIN      ; Wait for character to be received
;
                IN      A,(STI+UDR)  ; Input the character
                RES     7,A          ; Strip parity bit
                RET
;
;
;
;
;               CONSOLE-OUT DRIVER
;
;
;
TTYOUT:
                PUSH    AF           ; Save the character
WAIT:
                IN      A,(STI+TSR)  ; Input the transmitter status
                BIT     7,A          ; Bit 7 is the "buffer empty bit"
                JR      Z,WAIT       ; Wait for buffer to be empty
;
                POP     AF           ; Restore character
                OUT     (STI+UDR),A
                RET
;
TTYCHK:
                IN      A,(STI+RSR)  ; Input the receive status register
                BIT     7,A          ; Bit 7 is the buffer full bit
                RET                  ; which is set if a character
;                                    ; is received
;
;
;
```

```
                        ;
0060                    TTYOUT:
0060    F5                          PUSH    AF
0061                    WAIT:
0061    DB  BE                      IN      A,(STI+TSR)
0063    CB  7F                      BIT     7,A
0065    28  FA                      JR      Z,WAIT
                        ;
0067    F1                          POP     AF
0068    D3  BF                      OUT     (STI+UDR),A
006A    C9                          RET
                        ;
006B                    TTYCHK;
006B    DB  BD                      IN      A,(STI+RSR)
006D    CB  7F                      BIT     7,A
006F    C9                          RET
                        ;
0070                    TTYIN:
0070    DB  BD                      IN      A,(STI+RSR)
0072    CB  7F                      BIT     7,A
0074    28  FA                      JR      Z,TTYIN
                        ;
0076    DB  BF                      IN      A,(STI+UDR)
0078    CB  BF                      RES     7,A
007A    C9                          RET
                        ;
                        ;   INITIALIZE THE PRINTER
                        ;
007B                    PTRINT:
007B    3E  00                      LD      A,00000000B
007D    D3  B9                      OUT     (STI+TABCR),A
007F    3E  08                      LD      A,00001000B
0081    D3  B7                      OUT     (STI+TCDCR),A
0083    3E  10                      LD      A,16
0085    D3  BA                      OUT     (STI+TBDR),A
0087    3E  02                      LD      A,00000010B
0089    D3  B9                      OUT     (STI+TABCR),A
                        ;
008B                    WAIT1:
008B    DB  BA                      IN      A,(STI+TBDR)
008D    FE  0F                      CP      15
008F    20  FA                      JR      NZ,WAIT1
                        ;
0091                    WAIT2:
0091    DB  BA                      IN      A,(STI+TBDR)
0093    FE  10                      CP      16
0095    20  FA                      JR      NZ,WAIT2
                        ;
0097    3E  00                      LD      A,0000000B
0099    D3  B9                      OUT     (STI+TABCR),A
                        ;
009B    3E  0D                      LD      A,CR
009D    CD  00A6                    CALL    PTROUT
00A0    3E  0A                      LD      A,LF
00A2    CD  00A6                    CALL    PTROUT
                        ;
00A5    C9                          RET
                        ;
                        ;
00A6                    PTROUT:
00A6    F5              PUSH        AF
```

```
                        ;
00A7                    BUSY:
00A7    DB  B1                  IN      A,(STI+GPIP)
00A9    CB  7F                  BIT     PTRBSY,A
00AB    28  FA                  JR      Z,BUSY
                        ;
00AD                    ACK:
00AD    DB  B1                  IN      A,(STI+GPIP)
00AF    CB  47                  BIT     PTRACK,A
00B1    20  FA                  JR      NZ,ACK
                        ;
00B3    F1                      POP     AF
00B4    D3  D0                  OUT     (PTR),A
                        ;
00B6    F5                      PUSH    AF
                        ;
00B7    3E  00                  LD      A,0
00B9    D3  B9                  OUT     (STI+TABCR),A
00BB    3E  10                  LD      A,16
00BD    D3  BA                  OUT     (STI+TBDR),A
00BF    3E  02                  LD      A,00000010B
00C1    D3  B9                  OUT     (STI+TABCR),A
                        ;
                        ;
00C3                    WAITT1:
00C3    DB  BA                  IN      A,(STI+TBDR)
00C5    FE  0E                  CP      14
00C7    20  FA                  JR      NZ,WAITT1
00C9                    WAITT2:
00C9    DB  BA                  IN      A,(STI+TBDR)
00CB    FE  0F                  CP      15
00CD    20  FA                  JR      NZ,WAITT2
                        ;
00CF    3E  00                  LD      A,0
00D1    D3  B9                  OUT     (STI+TABCR),A
                        ;
00D3    F1                      POP     AF
00D4    C9                      RET
00D5                    ENCODE: END
```

Macros:

Symbols:

```
00AD    ACK         0003    AER         0007    BEL
0008    BS          00A7    BUSY        0018    CAN
000D    CR          0002    CTS         0006    DDR
0064    DDRVAL      007F    DEL         0005    DSR
0004    DTR         00D5    ENCODE      000B    ENTRY
0004    EOT         001B    ESC         0003    ETX
000C    FF          0001    GPIP        0000    GPIVAL
0009    HT          0000    IDR         0005    IERA
0004    IERB        0007    IMRA        0006    IMRB
0003    IPRA        0002    IPRB        0005    ISRA
0004    ISRB        000A    LF          0018    LOOP
00FF    MAPAD       0005    MAPN        0015    NAK
0000    NUL         00D0    PTR         0000    PTRACK
0007    PTRBSY      007B    PTRINT      00A6    PTROUT
0008    PVR         0006    RSLD        000D    RSR
0001    RST         0003    RX          0000    SCR
00B0    STI         0023    STINIT      0009    TABCR
```

```
000D                    RSR         EQU         13
000E                    TSR         EQU         14
000F                    UDR         EQU         15
                        ;
                        ;   INDIRECT REGISTERS
                        ;
0000                    SCR         EQU         0
0001                    TDDR        EQU         1
0002                    TCDR        EQU         2
0003                    AER         EQU         3
0004                    IERB        EQU         4
0005                    IERA        EQU         5
0006                    DDR         EQU         6
0007                    TCDCR       EQU         7
                        ;
                        ;
                        ;   MEMORY MAP CONTROL
                        ;
0005                    MAPN        EQU         5           ;   Memory Map #5
                        ;                                   ;   Configuration
00FF                    MAPAD       EQU         0FFH        ;   Memory Map Control
                        ;                                   ;   Port Address
                        ;
                        ;
                        BIT DEFINITIONS
                        ;
0000                    PTRACK      EQU         0
0007                    PTRBSY      EQU         7
                        ;
0001                    RTS         EQU         1
0002                    CTS         EQU         2
                        ;
0003                    RX          EQU         3
                        ;
0004                    DTR         EQU         4
0005                    DSR         EQU         5
                        ;
0006                    RSLD        EQU         6
                        ;
0064                    DDRVAL      EQU         01100100B
0000                    GPIVAL      EQU         00000000B
                        ;
00D0                    PTR         EQU         0D0H
                        ;
                        ;   ASCII SPECIAL CHARACTERISTICS
                        ;
0000                    NUL         DEFL        00H
0003                    ETX         DEFL        03H
0004                    EDT         DEFL        04H
0007                    BEL         DEFL        07H
0008                    BS          DEFL        08H
0009                    HT          DEFL        09H
000A                    LF          DEFL        0AH
000C                    FF          DEFL        0CH
000D                    CR          DEFL        0DH
0015                    NAK         DEFL        15H
0018                    CAN         DEFL        18H
001B                    ESC         DEFL        1BH
007F                    DEL         DEFL        7FH
                        ;
```

```
                                    ORG     00
0000    21  000B                    LD      HL,ENTRY        ;  Block Source Address
0003    11  000B                    LD      DE,ENTRY        ;  Block Destination
                    ;                                       ;  Address
                    ;
0006    01  00CA                    LD      BC,ENCODE-ENTRY ;  Block Length
0009    ED  B0                      LDIR
000B    3E  05      ENRTY:          LD      A,AMPN          ;  Load Map Number
000D    D3  FF                      OUT     (MAPAD),A       ;  Set Memory Map
000F    CD  0023                    CALL    STINIT
0012    CD  007B                    CALL    PTRINT
0015    CD  006B                    CALL    TTYCHK
0018    CD  0070    LOOP:           CALL    TTYIN
001B    CD  0060                    CALL    TTYOUT
001E    CD  00A6                    CALL    PTROUT
0021    18  F5                      JR      LOOP
                    ;
                    ;  STINIT
                    ;
0023                STINIT:
0023    F3                          DI
0024    3E  06                      LD      A,DDR
0026    D3  B8                      OUT     (STI+PVR),A
0028    3E  64                      LD      A,DDRVAL
002A    D3  B0                      OUT     (STI+IDR),A
                    ;
002C    3E  00                      LD      A,GPIVAL
002E    D3  B1                      OUT     (STI+GPIP),A
                    ;
0030    3E  07                      LD      A,TCDCR
0032    D3  B8                      OUT     (STI+PVR),A
0034    3E  01                      LD      A,00000001B
0036    D3  B0                      OUT     (STI+IDR),A
                    ;
0038    3E  01                      LD      A,TDDR
003A    D3  B8                      OUT     (STI+PVR),A
003C    3E  03                      LD      A,3
003E    D3  B0                      OUT     (STI+IDR),A
                    ;
0040    3E  88                      LD      A,10001000B
                    ;
0042    D3  BC                      OUT     (STI+UCR),A
                    ;
0044    3E  01                      LD      A,00000001B
0046    D3  BD                      OUT     (STI+RSR),A
0048    DB  BD                      IN      A,(STI+RSR)
                    ;
004A    3E  05                      LD      A,00000101B
004C    D3  BE                      OUT     (STI+TSR),A
004E    DB  BE                      IN      A,(STI+TSR)
                    ;
0050    3E  00                      LD      A,00000000B
0052    D3  B5                      OUT     (STI+IERA),A
0054    D3  B4                      OUT     (STI+IERB),A
                    ;
0056    3E  0D                      LD      A,CR
                    ;
0058    CD  0060                    CALL    TTYOUT
005B    3E  0A                      LD      A,LF
005D    CD  0060                    CALL    TTYOUT
```

000B	TADR	000A	TBDR	0007	TCDCR
0002	TCDR	0001	TDDR	000E	TSR
006B	TTYCHK	0070	TTYIN	0060	TTYOUT
000C	UCR	000F	UDR	0061	WAIT
008B	WAIT1	0091	WAIT2	00C3	WAITT1
00C9	WAITT2				

No fatal error(s)

PRO-LOG M900 UNIVERSAL PROM PROGRAMMER WITH THE STD-Z80 APPLICATION NOTE #11

INTRODUCTION

This application note describes the hardware and software required for programming MOS EPROMs using Mostek STD-Z80 Bus computer boards with a PROLOG M900 Universal PROM Programmer. A thrirty-two bit I/O module, the MDX-PIO, is the interface between the PROLOG M900 and the STD-Z80 Bus computer. With the system as described most MOS EPROMs can be programmed, read, contents verified against the RAM buffer and contents modified and then programmed into another PROM using the memory modify command. Files can be loaded from disk in binary or in HEX format and then the files can be programmed into the device that is selected. All operations are assisted with prompts from a menu driven screen driver.

The driver isn't limited to STD-Z80 computer products as it is port I/O mapped and can be used on most other computer systems.

FUNCTIONAL DESCRIPTION

The driver writes data from the computer to the PROLOG M900 unit, controls the address and data outputs, and then initiates the program cycle or read cycle. Basically, the driver manipulates the data and the address/control inputs from the computer so the PROLOG M900 receives the proper data to transfer to the target PROM from its internal buffer. The PROLOG M900 has an internal buffer to load data into. The buffer size is optional and should be the size of the largest PROM that is going to be used.

The driver supports 2708, 2516, 2716, 2532, 2732, 2564, and 2764 EPROMs. It will prompt the user on what configuration and personality modules for the M900 are needed with the selected PROM type. Some of the things the driver and the M900 will do:

(L)oad a file from disk to buffer area.
(M)odify the buffer contents.
(P)rogram PROM.
(R)ead the contents of a PROM into buffer area.
(V)erify the contents of a PROM to the buffer area.
(Q)uit driver and return to operating system.

The driver allows files that are stored on disk to be retrieved, the data is then loaded into memory and transferred to the PROM via the M900. The Memory command allows data to be altered or tabulated in the data buffer, then transferred to the PROM with the program command. The program command directs the data to be loaded in the PROM buffer within the M900; also, the program command controls the addressing and control signals needed to setup the M900 to program the PROM. As a support task, the driver can read PROMs and transfer the contents to the data buffer where the data can be modified or programmed into another PROM. The verify command compares the data in the data buffer and the PROM. If any locations do not match, an error message will be printed on the console device. After all tasks are complete or a new pattern is needed from the disk file, a QUIT command returns the control of the system to the operating system.

MDX-Z80 Bus Computer

Whereas this software driver can be configured to almost any computer system via the I/O port map, the Mostek MDX-Z80 Bus computer products are used as the host computer system. The system is a 64K disk based system with Mostek's M/OS-80* operating system. The I/O interface to the PROLOG M900 is provided by the MDX-PIO board. The MDX-PIO is a 32-bit parallel I/O board with TTL compatible outputs/inputs. The MDX-PIO communicates with the M900 through the parallel port provided as a factory installed option by PROLOG. The system needs to be at least a 32K operating system. The boards used with the driver are detailed below.

MDX-CPU1A (MK77855)

The MDX-CPU1A is a Z80 computer with 4K bytes of PROM sockets. The disk control firmware and the boot monitor are located on the board in the two 24-pin PROM sockets. The actual strapping is described in the appendix section.

MDX-DRAM32A (MK77761)

The MDX-DRAM32A is a memory board with 32K x 8 bytes of dynamic RAM that can be located on any 4K boundary. The system consists of two DRAM32As strapped at 0000 and 8000H. In addition, the upper RAM board has the 4K notch option enabled to stop any memory contentions between the CPU and the RAM boards. Strapping details are described in the appendix.

MDX-FLP2 (MK77677)

The MDX-FLP2 is a controller for interfacing the STD-Z80 Bus to floppy disk. The MDX-FLP2 allows double- or single-sided and single- or double-density 8-inch or 5¼-inch floppy drives.

MDX-SIO2 (MK77670)

The MDX-SIO2 is a serial communications board that provides the console interface and the printer port. The MDX-SIO2 has two independent asynchronous or synchronous serial I/O channels. Strapping information is described in the appendix.

MDX-PIO (MK77650)

The MDX-PIO is a 32 bit parallel Input/Output board that provides the total interface between the host computer and the PROLOG M900 Universal PROM Programmer. The MDX-PIO has four eight-bit I/O ports with handshake lines. The detailed strapping information is described in the appendix.

M/OS-80 Operating System (MK71010C81)

M/OS-80 is a C/PM* compatible operating system.

*C/PM is a trademark of Digital Research Corp.

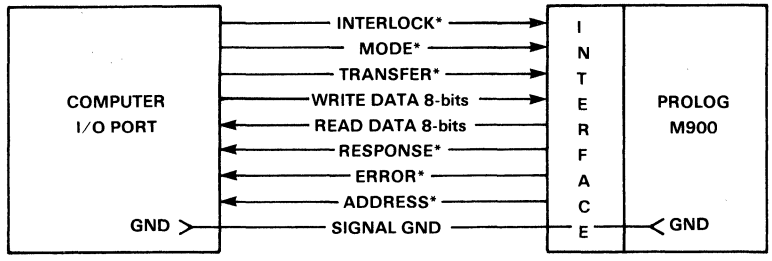
PROLOG M900 Universal PROM Programmer

The PROLOG Universal PROM Programmer can program many different types of bipolar PROMs and MOS EPROMs. This application note and driver will deal with MOS EPROMs. The EPROM type selected has a personality module and configuration module. The driver will prompt the user on which module it expects. If the wrong module is in place, an error will be printed and the BELL will sound.

The M900 interfaces to the host computer through a parallel port that is a factory installed option. The port provides a handshake routine for transferring data either to or from the COPY socket of the M900 PROM programmer. Connection is made via a 25-pin D-type connector. The interface has eight parallel bits for input data, eight bits for output data, and six bits for handshake and control lines.

PARALLEL INTERFACE DEFINITION

Figure 1



*** LOW ACTIVE SIGNALS**

PARALLEL INTERFACE PINOUT

Table 1

PIN	INPUTS	PIN	OUTPUTS	PIN	SIGNAL
8	WRITE DATA 8*	22	READ DATA 8*	1	+5 VOLTS**
6	WRITE DATA 7*	21	READ DATA 7*	25	LOGIC GND**
13	WRITE DATA 6*	24	READ DATA 6*	4	-12 VOTS**
10	WRITE DATA 5*	23	READ DATA 5*		
9	WRITE DATA 4*	18	READ DATA 4*		
7	WRITE DATA 3*	17	READ DATA 3*		
12	WRITE DATA 2*	20	READ DATA 2*		
11	WRITE DATA 1*	19	READ DATA 1*		
2	TRANSFER*	15	ADDRESS*		
3	MODE*	14	ERROR*		
5	INTERLOCK*	16	RESPONSE*		

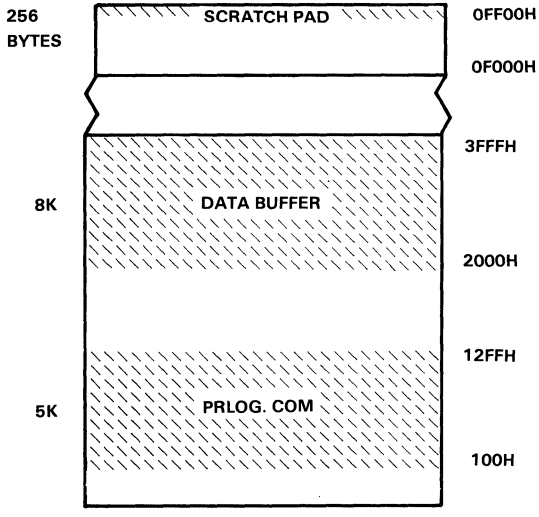
**** The signals are not used in this application.**

PRLOG Driver Considerations

The driver is a M/OS-80 compatible program. It is invoked by typing the programs file name "PRLOG" and then a carriage return (CR). The driver is approximately 5K and reserves RAM from 2000H to 3FFFH for the data buffer area to store data read from a PROM or loaded from a disk drive, a 2764 EPROM requires 8K for its data area. The operating system expects the area from 0FF00H to 0FFFFH to be reserved for the system scratch-pad area. The minimum system requires a 32K system with the previous areas reserved for the driver. In addition, the driver uses the I/O port addresses 0A8H to 0AFH as the MDX-PIO ports.

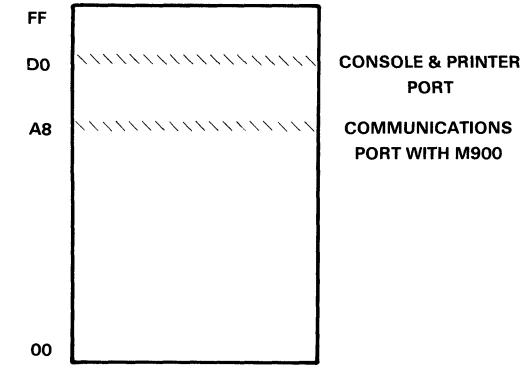
PRLOG DRIVERS MEMORY MAP

Figure 2



PRLOG PORT MAP

Figure 3



DESCRIPTION OF OPERATION

After the driver is loaded, the driver will prompt for the type of device, 2708, 2516, 2716, 2532, 2732, 2564, or 2764. After the device is selected, the driver will prompt the user with the personality and configuration modules as a reminder. Also at this time, the driver is establishing handshaking with the M900. If the handshake routine does not take place, and error message wil be displayed at the console and the console bell will sound until the RESET on the PROLOG M900 is pressed. The error condition should be removed with the reset; if not, check the setup and configuration modules to make sure the correct ones for the device are in place.

L-Load a specfied file
P-Program a PROM
M-Modify or tabulate memory
R-Read data from a PROM
V-Verifiy a PROM against memory
Q-Exit from program

Enter type of action required (L,R,P,V,M,Q)?

After the operation needed is selected, the driver will prompt the user for additional information it may require to complete the task selected. The information needed is detailed below.

LOAD Command

The load command is used to bring a file from the disk. The file has to be specified when the PRLOG driver is invoked.

A. PRLOG filename.ext (CR)

PRLOG . . . . . Drivers name.

filename.ext . . . . . file to be loaded form disk and the extension of .COM or .HEX.

(CR) . . . . . carriage return

The file name is stored until additional information is provided to load the data into the data buffer. The user must specify whether the file is in a binary or hexadecimal format. The driver has a hex loader for the hex files.

If the prompt for the type of action is an "L" and the file is specified, a prompt for the PROM loading address will be issued to the console. If a file is not loaded, then the following error message will be displayed at the console:

"**File name was not entered before load**"

The driver will have to be reinvoked and the file name loaded with it.

The buffer area is limited to the size of the EPROM being programmed. For example, a 2716 has a max buffer size of 2K, so the relative load address is anywhere from 0000 to 7FFH. Typically, the response is zero (0) in almost all cases.

The next prompt asks for the File load address and is asking for the starting location of the file to be loaded. The file will load only the amount of the data buffer. Again, using the 2716 as an example, only 2K of the file will be loaded into the data buffer. So if the file to be loaded is over 2K in length, it will require repeated loads to get all the file into the EPROMs. After the prompts are answered, the driver will access the disk and load the data according to the parameters entered from the prompts. The driver will re-issue the command prompt. A P-Program command or a V-Verify command typically follows the load.

PROGRAM Command

The PROGRAM command will transfer any data in the data buffer to the EPROM in the COPY socket of the M900 unit. The user will be prompted for PROM start location, where the data goes in the EPROM itself, again relative to zero (0). There is an optional PROM stop location. With multiple loads and the PROM start/end information many programs can be loaded into one PROM. This is very important when trying to use the larger format EPROMs.

READ Command

The READ command reads the data out off a PROM in the COPY socket of the M900 PROM programmer and transfers the data to the data buffer. The data can then be transferred to a PROM with the PROGRAM command or looked at and modified with the Memory command, using the "Save" command of M/OS-80 or C/PM* to save the data on the disk media.

VERIFY Command

The VERIFY command reads the data in a PROM in the COPY socket of the M900 and compares the contents against the data buffer. If any differences are noted, the address of the bad data with the read and expected data are displayed to the console device. A period will stop the display from advancing if many locations are noted. The period is used as a terminator for most of the other commands as well.

MEMORY Command

The MEMORY command is a valuable aid in correcting or tabulating PROMs. After getting the data from a PROM or disk file into the data buffer with a READ command or a LOAD command, the data can be tabulated to the console device by entering and "M" (CR) and answering the memory start/stop prompt. To modify a memory location, the single location to be modified is entered with no stop address and then the carriage return after the "M" command is entered. The MEMORY command shows the address and the contents along with the ASCII characters displayed beside the data line. A period will terminate the printing to the console device.

QUIT Command

The QUIT command returns the system to the operating system.

OPERATIONAL HINTS

Saving the Data Read from a PROM

This is a suggested routine to save the data onto a disk unit. After reading the data from a PROM with the READ command, the data is stored in the data buffer from 2000H to the end of the buffer which is determined by the PROM type selected. A 2732 would end its buffer at 2FFFH, so the complete PROM data would be from 2000H to 2FFFH. After the READ command has finished, use the QUIT command to return the system to the operating system. With the EXEC command of M/OS-80 execute the DDT monitor by typing:

A. EXEC E11D (CR)

The "." (period) prompt will be displayed. This is the prompt for the DDT monitor. The data is still in memory and needs to be transferred to memory location 100H to save disk space. Using the copy command of DDT type:

. C 2000,XXXX,100 (CR)

C-COPY. . . . memory contents from start-stop location.

2000. . . . The starting location of the data buffer.

XXXX. . . . The ending location of the data in the data buffer.

100. . . . The target load address.

After the prompt returns type: .E 0 (CR)

This will return the system to the operating system. After the operating system prompt appears, use the SAVE command to save the data on to the disk. The format of the command under M/OS-80 is as follows:

A. SAVE nn [B:]filename.com (CR)

nn. . . . Is the number of 256 byte blocks to be saved.

[B:]. . . . The unit of the drive the data is to be saved on.

PROGRAMMING MANY PROGRAMS ON A PROM

The best way to program several programs into one PROM is to use the XFER command of M/OS-80 to append the files to be programmed into one file. The format is:

A.XFER [options] [B:]newfile.ext=[B:]file1.ext,file2.ext,.... filen.ext (CR)

Then with the "newfile", follow the LOAD instructions and PROGRAM the PROM as needed.

EXAMPLES

PRLOG TEST.COM

Enter PROM type nnnn [2708, 2516, 2716, 2532, 2732, 2564, or 2764]:2716

SETUP THE PROLOG PROGRAMMER WITH THE

PM9064 and PA24-1 PERSONALITY MODULES.

AND THE 2048 CONFIGURATION PLUG.

L - LOAD a specified file
P - Program data to PROM
M - Display or update memory
R - Read data from a PROM
V - Verify a PROM against memory
Q - Exit from the program

Enter type of action required (L,R,P,V,M,Q):L

Enter file type - "B" for Binary or "H" for Hex:B

Enter PROM load address (PROM offset):0

Enter starting file address, [,file ending address]:0

File load completed '1st 2K of file was loaded from disk'

L - LOAD a specified file
P - Program data to PROM
M - Display or update memory
R - Read data from a PROM
V - Verify a PROM against memory
Q - Exit from the program

Enter type of action required (L,R,P,V,M,Q):L

Enter file type - "B" for Binary or "H" for Hex:B

Enter PROM load address (PROM offset):0

Enter starting file address, [,file ending address]:800

File load completed '2nd 2K of file was loaded from disk'

L - LOAD a specified file
P - Program data to PROM
M - Display or update memory
R - Read data from a PROM
V - Verify a PROM against memory
Q - Exit from the program

Enter type of action required (L,R,P,V,M,Q):M

Enter starting address [,ending address]:0.1F
0000 19 22 8A 12 CD E0 0A DA 76 0A CD 7F 0A CD A2 0A
."".....v.....

'Looked at first 16 bytes of the 2nd 2K loaded'

L - LOAD a specified file
P - Program data to PROM
M - Display or update memory
R - Read data from a PROM
V - Verify a PROM against memory
Q - Exit from the program

Enter type of action required (L,R,P,V,M,Q):R

Read complete 'The contents of a PROM in the copy socket read'

L - LOAD a specified file
P - Program data to PROM
M - Display or update memory
R - Read data from a PROM
V - Verify a PROM against memory
Q - Exit from the program

Enter type of action required (L,R,P,V,M,Q):P

Enter PROM starting, [ending address]:0,7FF 'Program new data in PROM'

Program complete 'PROM data transferred to new PROM'

L - LOAD a specified file
P - Program data to PROM
M - Display or update memory
R - Read data from a PROM
V - Verify a PROM against memory
Q - Exit from the program

Enter type of action required (L,R,P,V,M,Q):V

Verify complete 'contents of PROM compared with data buffer'

L - LOAD a specified file
P - Program data to PROM
M - Display or update memory
R - Read data from a PROM
V - Verify a PROM against memory
Q - Exit from the program

Enter type of action required (L,R,P,V,M,Q):Q

A. 'Return to the operating system'

APPENDIX A
STRAPPING OF PIO

J2	J3
1- 2	3-4 (0A8H)
17-18	7-8
23-24	

Change U6 from 74LS243 (as shipped from the factory) to a 74LS242.

STRAPPING OF FLP2

J2	J4	J6	J7	J8	J9
N/C	1-2	1-2	1-2	3-4	N/C

J10	J11	J12
1-2	2-3	2-3
3-4		

The above strapping is for a single-sided eight-inch disk drive.

STRAPPING OF THE CPU1A

J2/U5	J3	J4/U10
3-5	N/C	11-14
6-7		10-12
8-9		

EPROMs MK6235 and MK6340 should be in the PROM sockets U6 and U7.

STRAPPING OF THE CPU2A

J3	J4	J5	J6	J7-J8	J9-J12
3-4	N/C	3-4	N/C	1-8	1-8
				2-3	3-9
				4-5	4-5
				7-9	6-7

PROMs MK6235 and MK6340 should be in the PROM sockets U7 and U8 and 1K static RAMs in the other four sockets.

DRAM32/32A

1st DRAM (0000H)

	U28	
A-B		
D-E	closed	1
H-J	closed	2
	closed	3
	closed	4

2nd DRAM (8000H)

	U28	
A-B		
D-E	open	1
H-J	closed	2
	closed	3
	closed	4

SIO2 STRAPPING

RS232 (DCE)

Channel A:	J3	J7	J8	J9
	1- 2	1-2	7-8 (9600 Baud)	5-6 (0DCH)
	11-18	3-4	open (19200 Baud)	
	12-17			
	13-20			
	14-21			
	15-22			
	16-19			

Channel B:	J4	J7	J8
	1- 2	5-6	15-16 (9600 Baud) or
	11-18	17-8	9-10 (1200 Baud)
	12-21		
	13-20		
	15-22		
	16-19		

APPENDIX B
CABLE INFORMATION

	PROLOG M900		MDX-PIO		
25 D-type Plug	**PIN**	**SIGNAL**	**PIN**	**SIGNAL**	**26-Pin discrete header**
	1	+5 VDC	N/C		
	2	TRANSFER*	J2-22	B5	
	3	MODE*	J2-10	B6	
	4	-12 VDC	N/C		
	5	INTERLOCK*	J2-23	B7	
	6	WR DATA 7*	J2-16	A6	
	7	WR DATA 3*	J2-18	A2	
	8	WR DATA 8*	J2-3	A7	
	9	WR DATA 4*	J2-5	A3	
	10	WR DATA 5*	J2-17	A4	
	11	WR DATA 1*	J2-19	A0	
	12	WR DATA 2*	J2-6	A1	
	13	WR DATA 6*	J2-4	A5	
	14	ERROR*	J2-8	B2	
	15	ADDRESS*	J2-20	B1	
	16	RESPONSE*	J2-7	B0	
	17	RD DATA 3*	J1-18	A2	
	18	RD DATA 4*	J1-5	A3	
	19	RD DATA 1*	J1-19	A0	
	20	RD DATA 2*	J1-6	A1	
	21	RD DATA 7*	J1-16	A6	
	22	RD DATA 8*	J1-3	A7	
	23	RD DATA 5*	J1-17	A4	
	24	RD DATA 6*	J1-4	A5	
	25	GROUND	J1-14	GND	

*Low Active Signal

PORT MAP OF DRIVER

PIO#1		**J2**	
	PORT A	DATA	A8
	PORT A	CONTROL	A9
	PORT B	DATA	AA
	PORT B	CONTROL	AB
PIO#2		**J1**	
	PORT A	DATA	AC
	PORT A	CONTROL	AD
	PORT B	DATA	AE
	PORT B	CONTROL	AF

1983 COMPUTER PRODUCTS DATA BOOK

FLEXIBLE DISK OPERATING SYSTEM - **M/OS-80**

USER FEATURES

- ☐ Virtual CP/M™ compatibility gives the user many available programs to choose from.
- ☐ Additional utilities and systems commands provide increased capability and functionality to the user.
- ☐ Provided on standard media for use with Mostek standard systems and MD Series boards for short system integration time.

INTRODUCTION

M/OS-80 is a CP/M™ compatible, floppy disk operating system for the MD or SD series of microcomputer board systems. It offers a comprehensive solution to a wide variety of system design problems. The software is provided on an 8-inch single-sided, single-density floppy diskette which can be booted on Mostek disk-development systems or user-configured systems (see "Hardware Required" paragraph). M/OS-80 can be altered for different input/output hardware configurations by using the MOSGEN Utility (sold separately).

Several powerful utilities are provided with M/OS-80. These programs give the user a broad base of support and will improve design efficiency. These include:

Editior (Edit)
Designer's Development Tool (Debugger)
Transfer Utility (XFER)
File/Disk Dumps (DSKDUMP)
Print Utility (PRINT)
Print Spooler (SPOOL)
Several System Utilities

Because of M/OS-80's CP/M compatibility, a large number of pre-written programs are available. M/OS-80 is designed to run programs written for other CP/M-compatible operating systems, such as CDOS™, I/OS™, and SDOS™, provided these programs conform to the standards described by Digital Research in versions 1.4 through 2.2. Virtually all compilers and interpreters now sold for use on CP/M (versions 1.4 -2.2) will work. For those Mostek customers who are currently running FLP-80DOS, M/OS-80 provides a direct migration path to CP/M compatibility without any changes to the system hardware.

SYSTEM FEATURES

M/OS-80 is a more sophisticated and powerful floppy disk operating system than any other micro-operating system available. It provides the user with a unique, but invisible, library structure. By assigning one system disk as a Master Library disk, the system can free the user to place all application-related files on another disk while still having the utility of the various system programs on-line.

Unlike other operating systems, M/OS-80 provides the user with comprehensive error messages. In most cases, methods of recovery are displayed and the operator is given several options from which to choose.

HARDWARE REQUIRED

M/OS-80 is currently supplied in three versions. V3 is designed to run on Mostek's MATRIX systems and on systems built with MD Series boards. An MD Series system must contain the following boards:

Item	Hardware Required
Processor	MDX-CPU1 or MDX-CPU2
Console Interface	MDX-EPROM/UART or MDX-SIO
Printer Interface	MDX-PIO or MDX-SIO
Floppy Interface	MDX-FLP1 or MDX FLP2
Memory	(2) MDX-DRAM with 64K of RAM

The V5 system is for use with a Mostek Phantom PROM system configuration. The following boards are required:

Item	Hardware Required
Processor	MDX-CPU3 or MDX-CPU4
Floppy Interface	MDX-FLP2
Memory	(2) MDX-DRAM with 64K of RAM (required only for MDX-CPU4)

The V6 system is for use with a Mostek Phantom hard-disk system. The following boards are required:

IX

CP/M is a Trademark of Digital Research, Inc.
CDOS is a Trademark of Cromemco, Inc.
SDOS is a Trademark of SD Systems, Inc.
I/OS is a Trademark of Infosoft Systems, Inc.

Item	Hardware Required
Processor	MDX-CPU3 or MDX-CPU4
Floppy Interface	MDX-FLP2
Memory	(2) MDX-DRAM with 64K of RAM (required only for MDX-CPU4)
Hard Disk Interface	MDX-SASI1 & MDX-SASI2

With either the V3, V5 or V6, M/OS-80 requires 64K bytes of RAM for operation. Four bootstrap PROMs are supplied with V3, and one bootstrap PROM is supplied with V5 or V6. The system initially must have at least one 8-inch, single-sided, single-density floppy disk drive in order to boot-up M/OS-80. Up-to-four disk drives are supported. The V6 configuration can also boot-up from hard disk.

Table 1 details the peripheral and CPU configurations required for the M/OS-80 versions.

M/OS-80 CONFIGURATION SUMMARY
Table 1

PERIPHERALS	CPU1	CPU2	CPU3	CPU4*
UART Console	V3	V3	N/A	N/A
SIO Console	V3	V3	N/A	N/A
STI Console	N/A	N/A	V5/6	V5/6
SIO Line Printer	V3**	V3**	V5**/6	V5**/6
PIO Line Printer	V3	V3	N/A	N/A
STI Line Printer	N/A	N/A	V5/6	V5/6
FLP1	V3	V3	N/A	N/A
FLP2	V3***	V3***	V5/6	V5/6
SASI	*	*	V6	V6

N/A Not Applicable.
* Future Design.
** SIO line printer configuration is supplied as alternate on systems disk.
*** Single-density only.

NOTE:
1. MOSGEN Utility may be purchased to configure systems for different peripherals and smaller sizes of RAM. See the MOSGEN Data Sheet for more information.

EDIT - Text Editor

The ASCII EDITor file provided with M/OS-80 provides a text editor for users who do not have access to a screen-editor. The editor allows creation and modification of the text files by several easy-to-use commands. EDIT features include:

Find a text string
Change a text string
Find a line
Insert new text
Delete a line(s) or character(s)
Put a block of text into another file
Get a block of text from another file
View text on the console screen
Print text on the line printer
Create a set of commands which can be executed as a macro

XFER — Transfer Utility

The XFER program is a general-file transfer utility. It allows for the moving of files from disks or devices to other (or the same) disks or devices. The XFER features include:

Transfer an ASCII file
Compare two files without moving
Filter out illegal ASCII characters
Conditionally transfer a file (user prompted)
Transfer a Read-Only file
Expand tabs
Verify files after moving
Print HEX address of comparison failure
Transfer only old files
Transfer only new files

DSKDUMP - Disk Dump

The DSKDUMP program allows reading or modifying of a file, the disk data area, or the disk directory. Each block requested is read into a 128-byte buffer, then displayed. The blocks are numbered sequentially. Any block can be selected, displayed, modified, and written back to the disk.

PRINT - Print Utility

The PRINT utility formats ASCII files to the CRT or printer with automatic headings, tabbing and pagination. User-specified options include page width and length, page headings, date printed of the top of each page, and page formatting.

SPOOL - Print Spooler

The SPOOL file system feature is used to output a file from the printer to a system list device while the system continues with other functions. Any ASCII file may be spool-printed, and direct printer activity is prevented while a spool-print is active.

Other System Utilities

M/OS-80 provides several other system utilities to permit a user the highest degree of flexibility in the manipulation of the files and programs created and used with the system. Some of these utilities include: programs to format disks, change disk labels, examine directories, and to diagnose disk problems. A PROM programming utility is also included that interfaces with Mostek's PPG 8/16.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
M/OS-80 V3	One diskette containing all M/OS-80 programs in binary, four bootstrap PROMs, and one Operations Manual. (See Table 1 for hardware configuration requirements.) Requires the signed Software License Agreeement (enclosed) with purchase order.	MK71010C-81
M/OS-80 V5	One diskette containing all M/OS-80 programs in binary, one bootstrap PROM, and one Operations Manual. (See Table 1 for hardware configuration requirements.) Requires the signed Software License Agreement (enclosed) with purchase order.	MK71011C-81
M/OS-80 V6	One diskette containing all M/OS-80 programs in binary, one PROM for booting from floppy or hard disk, and an Operations Manual. (See Table 1 for hardware configuration requirements.) Requires the signed Software License Agreement (enclosed) with purchase order.	MK71012C-81
M/OS-80 Operations Manual	Detailed description of the operation and use of the M/OS-80 software package.	4420064
MOSGEN	System generation utilities and device drivers, data sheet	4420268
M80/L80 BASIC-80 BASCOM FORTRAN-80	Microsoft language packages, data sheet	4420309
AIM-Z80	In-circuit-emulation for Z80, data sheet	4420245

MOSGEN UTILITY MK71001

USER FEATURES

- ☐ Adapts M/OS-80 to customized MDX and SD systems.
- ☐ Allows tailoring M/OS-80 for different I/O devices and RAM sizes.
- ☐ Works on systems configured around the DDT/DCF PROMs or Phantom PROM.
- ☐ Menu driven format to speed the configuration process.

DESCRIPTION

Mostek's MOSGEN Utility is a system generation package used to generate unique configurations of the M/OS-80 Operating System. MOSGEN allows the user to modify the M/OS-80 by rewriting existing I/O drivers or creating new drivers for specialized I/O operation, and configuring different system RAM sizes.

MOSGEN allows creation of a command file which will link a newly customized system. The MOSGEN package also includes a set of object and source files to provide the user with a valid set of device drivers. These drivers are provided to help the user create new drivers based on known-working examples. Users are permitted to modify or select drivers for the following logical-unit devices:

- System Console (output)
- Keyboard (input)
- List
- Punch
- Reader
- Disk
- Clock

MOSGEN is supplied on two single-sided, single-density 8-inch diskettes. They are the System Generation diskette and the Device Drivers/Library diskette.

MOSGEN OPERATION

The MOSGEN package creates a batch submit (.CMD) file which, when executed, walks the system through the complex re-assembly, trial linkage, and final linkage process automatically and without operator intervention. The last steps of the MOSGEN-created batch file test the newly-created system for errors in linkage, size, and conformity to system restrictions. The user-supplied drivers are linked into the main core of the system during this linkage process. A special linkage editor is provided for the sole purpose of this system generation link. MOSGEN proves itself useful, if not essential, when system restrictions limit the amount of available RAM in the target system, or require the use of non-standard peripherals or special-intelligent I/O drivers.

MOSGEN may be used to configure M/OS-80 for different sizes of RAM in the user system down to a minimum of 24K bytes.

MOSGEN SYSTEM REQUIREMENTS

MOSGEN and all related software require the user to have a running 64K M/OS-80 system in place. Depending on the requirements of the users development languages, the system memory requirements may be in excess of the 32K bytes of RAM required for a minimum M/OS-80 system.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MOSGEN Utility	Two diskettes containing MOSGEN system generation utilities and device drivers, both source and object files, and one Operations Manual. A signed Software License Agreement is required with purchase order.	MK71001C-80
MOSGEN Operations Manual	Detailed description of the operation and use of the MOSGEN Utility.	4420270

ASM-68000 STRUCTURED MACRO CROSS ASSEMBLER LINK-68000 RELOCATING LINKAGE EDITOR

FEATURES

- ☐ Absolute or relocatable code generation
- ☐ Uses Motorola mnemonics and addressing
- ☐ Enhanced macro and conditional assembly capability
- ☐ Structural statements:

IF-THEN-ELSE	REPEAT-UNTIL
FOR-DO	WHILE-DO
LOOP-ENDL	EXIT

- ☐ Complex expression evaluation
- ☐ Source code, symbol table and cross-reference listing
- ☐ Includes Relocating Linkage Editor

GENERAL DESCRIPTION

Mostek's ASM-68000 Structured Macro Assembler is a powerful software package which enables the user to develop application programs for MK68000-based microcomputer systems. ASM-68000 translates assembly language source statements into relocatable object code for the LINK-68000 Relocating Linkage Editor, which in turn combines them into an absolute load module suitable for loading into the AIM-68000.

ASM-68000

The basic goals of ASM-68000 are: (1) to provide the programmer with the means to translate assembly language source statements into relocatable object code (for the Linkage Editor); and (2) to provide a printed listing containing the source language input, assembler object code, and additional information (such as error codes, if any) useful to the programmer. 68000 assembly language is a collection of mnemonics and symbols representing 68000 machine instructions, assembler directives, macros, symbolic names (labels), operators, and special symbols.

ASM-68000 uses Motorola-compatible mnemonics, addressing modes, and expression syntax. Numerous enhancements have been made in the ASM-68000 macro and conditional assembly capability, as compared to the Motorola assembler.

ASM-68000 produces a relocatable object module which contains information enabling LINK-68000 to combine modules and assign new sets of memory locations.

LINK-68000

LINK-68000 accepts object modules generated by ASM-68000 and combines them into an absolute load module. The user may specify up to four "segments" of memory. For example, ROM code could be contained in a segment separate from RAM data. Up to 16 relocatable sections, plus absolute and named common sections (limited only by available memory space), may be allocated among the segments. Comprehensive listing output options are provided, including a load map, externally defined symbols, undefined symbols, multiply defined symbols, segment lengths, and error counts. Extensive control of LINK-68000 is provided interactively at link time, including module order, address assignment, resolution of undefined references, and generation of listings.

OPERATING ENVIRONMENT

ASM-68000 and LINK-68000 are supplied on DOS-11 formatted magnetic tape (800 bpi) in compiled object form, ready to link and run on DEC PDP-11 under RSX-11M, or VAX under VMS in compatibility mode. A minimum user partition of 64K is required. Command files for automated installation are provided.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NUMBER
ASM-68000	68000 Structured Macro Cross Assembler, with manuals, includes LINK-68000, for RSX-11M (or VAX/VMS in compatibility mode	MK71020C-33
ASM-68000	Documentation package for above	MK71020D
RADIUS	Remote Development Station data sheet	4420194
AIM-68000	Application Interface Module data sheet	4420316

MICROSOFT M80/L80 - MK71002
MICROSOFT BASIC-80 - MK71003
MICROSOFT BASCOM - MK71004
MICROSOFT FORTRAN-80 - MK71005

FEATURES

- ☐ M/OS-80 development aids for Z80 microcomputer
- ☐ CP/M™ compatible
- ☐ Macro assembler
- ☐ Relocating linking loader
- ☐ BASIC interpreter and compiler
- ☐ FORTRAN compiler
- ☐ Common relocatable object format-link modules in different languages

INTRODUCTION

A series of Microsoft program development tools are now available from Mostek. They offer a comprehensive solution to a wide variety of system and application design problems. The software is provided on 8-inch single-sided single-density floppy diskettes and operates under M/OS-80.

M80/L80

M80 is a relocatable macro assembler for Z80 microcomputer systems, incorporating almost all "big computer" assembler features without sacrificing speed or memory space. The M80/L80 package is comprised of the M80 assembler, L80 linking loader, and a cross reference utility.

BASIC-80

BASIC-80 is the most extensive implementation of BASIC available for the Z80 microprocessor. In three years of use, it has become the world standard for microcomputer BASICs, meeting the requirements for the ANSI subset standard for BASIC, and supporting many unique features rarely found in other BASICs.

BASCOM

Microsoft's BASIC compiler (BASCOM) is a powerful new tool for programming BASIC applications or microcomputer system software. The single-pass compiler produces extremely efficient, optimized machine code that is in standard Microsoft relocatable binary format. Execution speed is typically 3-10 times faster than interpreter BASICs. The M80/L80 assembler/linker package is included with BASCOM.

FORTRAN-80

Microsoft's FORTRAN-80 package provides new capabilities for users of Z80 microcomputer systems. FORTRAN-80 is comparable to FORTRAN compilers on large mainframes and minicomputers. All of ANSI standard FORTRAN X3.9-1966 is included except the COMPLEX data type. Therefore, users may take advantage of the many application programs already written in FORTRAN. The M80/L80 assembler/linker package is included with FORTRAN-80.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NUMBER
M80/L80	Relocating macro assembler/linker on diskette, with operations manual	MK71002C-80
BASIC-80	BASIC interpreter on diskette, with operations manual	MK71003C-80
BASCOM	BASIC compiler on diskette with operations manual (includes M80/L80)	MK71004C-80
FORTRAN-80	FORTRAN compiler on diskette, with operations manual (includes M80/L80)	MK71005C-80
M/OS-80	CP/M™ compatible disk operating system data sheet	4420271

CRASM-70
3870 CROSS-ASSEMBLER

FEATURES

- ☐ Assembles standard 3870 and F8 source
- ☐ Produces absolute load module in F8HEX format
- ☐ Runs under M/OS-80 on any Mostek disk system
- ☐ Produces complete assembly listing to disk or printer
- ☐ Produces symbol reference table

DESCRIPTION

The Mostek 3870 Cross Assembler (CRASM-70) runs under the M/OS-80 operating system, and assembles standard 3870/F8 assembly language. The output is an absolute object file (load module) in F8HEX format. A conversion utility is provided to convert F8HEX files to Mostek Hex for use with the AIM-7X in-circuit-emulator system. The Mostek MATRIX-80/SDS disk development system can be used for stand-alone assembly and debug capability, with the AIM-7X plugged directly into the system. The assembler object module may also be downloaded from a M/OS-80-based system to a Mostek RADIUS development system containing an AIM-7X.

CRASM-70 produces an assembly listing which can be directed to a disk file or directly to the M/OS-80 LST: list device (printer). The listing shows program address, machine code, and line number for each statement, along with each source program statement. Any errors which are found in the source program are indicated in the listing. A symbol reference table is printed at the end of the listing. Up to 500 symbols may be used in the source program.

CRASM-70 is supplied on a standard 8-inch single-sided single-density CP/M-compatible diskette, precompiled, ready to run under M/OS-80.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NUMBER
CRASM-70	3870/F8 Cross Assembler, runs under M/OS-80, on 8" SSSD diskette, with manual	MK71007C-80
CRASM-70	Documentation package for above	MK71007D
RADIUS	Remote Development Station data sheet	4420194
AIM-7XE	Application Interface Module data sheet	4420246

SOFTWARE MODULAR LIBRARY

FEATURES

- ☐ Software subroutines/modules supplied in source form
- ☐ Software modules supplied for STD-Z80 MDX-Modular Board Series
  - MDX-CPU1/2/3/4
  - MDX-PIO
  - MDX-UART
  - MDX-SIO1/2/422
  - MDX-FLP1/2
  - MDX-SASI1/2
- ☐ Software modules supplied for Z80 chip set
  - MK3881 PIO
  - MK3882 CTC
  - MK3883 DMA
  - MK3884/5/7 SIO
  - MK3801 STI
- ☐ General Software Modules
  - PROM Programmer software for PROLOG M900 Programmer
- ☐ Assembly language source supplied on M/OS-80™ diskette
- ☐ M/OS-80 and CP/M™ Z80 compatible
- ☐ Designed for ease of modification by user
- ☐ Clear documentation provided in source

DESCRIPTION

The Mostek Software Modular Library is a set of software subroutines/modules which provide example programs for users of STD MDX boards. Each module is supplied in source form in Z80 assembly language. Complete documentation is included as comments in the source program which describes the interface, operation, and use of the module. Adaptation of the example program to the user's specific hardware configuration is the user's responsibility. All general/standard MDX I/O interfaces are included in the software modules.

The Modular Library is supplied on M/OS-80 single-sided, single-density 8-inch diskette. A file named "READ.ME" is supplied with the product which gives a general description of each module. This file can be listed to the console or printer. A complete printed listing is also supplied with the product. M/OS-80 and a Z80 assembler such as Microsoft's M80/L80™ package is required.

The printed listing may be ordered separately for those users who do not have access to an operational disk system.

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CP/M is a trademark of Digital Research Corporation.
M/OS-80 is a trademark of Mostek Corporation.
M80/L80 is a trademark of Microsoft Corporation.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
MODLIB	One M/OS-80 diskette containing the Software Modular Library source. Printed source listing is included.	MK71009C-80
MODLIB Listing	Printed source listing only.	MK71009D

1983 COMPUTER PRODUCTS DATA BOOK

UNITED TECHNOLOGIES MOSTEK

COMPUTER PRODUCTS DIVISION

ADVANCE INFORMATION

MK8200 GENERAL PURPOSE MEMORY

FEATURES

- 64 MB capacity with ECC
  72 MB capacity without ECC
- 64 bit word width
- 100 ns/word sequential data rate
  400 ns random access cycle time
- Four dynamically switchable refresh modes
- Unidirectional or bidirectional data bus
- Single bit correct, double bit detect capability
- Front panel access to internal error log
- Read and write capability to internal check bits
- Automatic check bit validation
- Rugged steel chassis
  Two piece connector system for enhanced reliability
  Integral fan pack and power supply
- High capacity power distribution to support burst refresh requirements

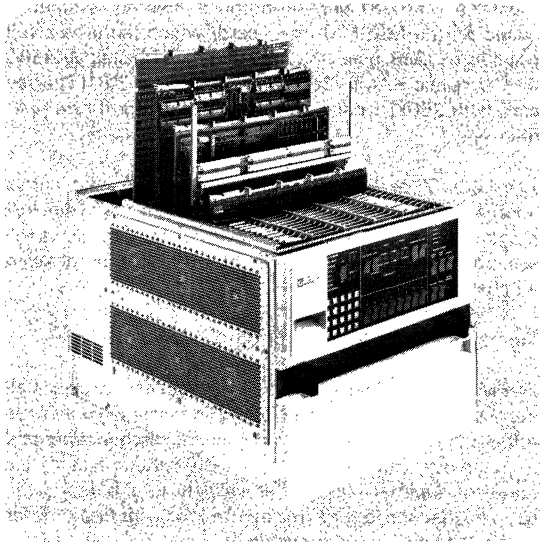
INTRODUCTION

Mostek's MK8200 memory system family is based on an architecture that permits maximum flexibility, with a capacity of 4 to 72 megabytes and word widths from 16 to 72 bits. Common piece parts can be easily reconfigured to fulfill a wide variety of applications, including such field-proven applications as fixed-head disk replacement, main memory, video buffers, digital telephone switching, and data acquisition and processing. The result is custom system performance without the problems normally encountered with "one-of-a-kind" approaches.

Designed around Mostek's MK4564 64K dynamic RAM, the MK8200 family gives you up to 72 megabytes of memory in a single, 15.75-inch rack-mountable chassis. Plus, all the logic necessary to support 256K RAMs is already in place, allowing for future "x4" densities without costly redesign. Performance features include 400 ns random cycle and access times, plus the ability to mix reads and writes at a 100 ns sequential data rate.

MK8200

Figure 1



The MK8200 memory system family, designed with the user in mind, is highlighted by a microprocessor-controlled front panel which allows centralized system interrogation via hardware or software control. Four dynamically selectable refresh modes include asynchronous (cycle hold off), external (external timing/internal address), synchronous (external timing/external address) and hidden (with refresh overhead hidden in an eight-way sequential addressing requirement).

Additional user-friendly features include card slot(s) inside the chassis for user control logic, multiple voltage power distribution available to support multiple logic families, and check bit validation which automatically writes memory to establish good ECC check bits. Convenient signal probe points and probe grounds are available throughout the system.

The Mostek MK8200 family, housed in a rugged steel chassis, is specifically designed for reliability and ease of maintenance. All cards feature a two-piece connector system which provides enhanced mechanical and electrical integrity over card-edge types. A high-capacity power distribution supports the peak power demands of full-speed operation and burst refresh modes. Ball bearing fans

feature fan rotation sensors with warning circuitry, and the system has a two-level ambient overtemperature warning and shutdown feature.

Maintainability is assured by power supply "in-tolerance" monitoring, built-in ECC, a built-in error log with isolation to the physical RAM location, and an optional diagnostic card to perform a full system check.

HARDWARE

Array Card

Mostek's MK8200 general-purpose memory system is based on the MK8100 array card, which features a full capacity of 3 MB, using industry-standard Mostek MK4564 64K dynamic RAMs. Compatibility of the MK8100 array card with 256K dynamic RAMs will allow for future "x4" offerings.

The MK8100 array card has no user options; each card's address is determined by the motherboard slot into which it plugs. In addition, the card's flexible architecture allows full system population at 24-, 48- and 72-bit internal word widths.

Timing and Address Control Card

The MK8110 timing and address control card provides all system timing, including four dynamically switchable refresh modes, a high-speed pipeline architecture and multiple-user interface protocols. The MK8110 card also features automatic check bit validation, a port for the optional diagnostic card, and an error log with locations for every RAM device in the system.

Data and Error Correction Control Card

The MK8111 data and ECC card completes the control card set. With error correction enabled, this card provides single-bit correction and double-bit detection of all memory device errors. Other important features include a fully independent read-and-write path architecture that supports unidirectional or bidirectional operation, high-speed pipeline data paths, serial-byte write and partial word-merge capabilities, real-time error status with the error syndrome and flags provided at read access time, and a port for the optional diagnostic card.

System Extender Card

The MK8170 extender card features closely controlled circuit impedance plus a provision to move the motherboard termination to the end of the extender, allowing the card to be used at full system throughput speeds. Additional features include integral card guides to support extended cards, plus convenient probe signal and grounding points.

Universal Wrapped-Wire I/O Card

The MK8171, a universal wrapped-wire card, features a multi-layer design that provides user access to auxiliary power distribution as well as standard system voltages. The card's top edge can handle up to 10 ribbon cable connectors for interfacing the card to the user or to other cards in the MK8200 system. In addition, the socket array area holds up to 250 16-pin packages; to allow user-inserted sockets, the MK8171 card is available unpinned, or fully pinned with hollow pin socket contacts.

SPECIFICATIONS

Storage Capacity (with ECC)

Standard Capacity: †
Up to 32 MB (four-way interleave)
Up to 48 MB (two-way or no interleave)
Extended Capacity: †
Up to 64 MB (four-way interleave)

Word Width

Up to 64 bits plus ECC (always 8 ECC bits)

Modes of Operation

Read
Write
Read/merge/write
Refresh (four modes)

Sequential Data Rate

100 ns per word (read or write)*

Random Read or Write Cycle Time

400 ns maximum*

Read Access Time

400 ns maximum* at chassis interface

Refresh Cycle Time

400 ns maximum* (refresh may be hidden)

Input Receivers

High-impedance TTL

Output Drivers

Tri-state and open collector

Data Input

Two sets of up to 72 single-ended lines

Data Output

Two sets of up to 72 single-ended lines

Address Inputs

27 lines and three controller addresses

Physical Size

Height: 15.75 inches
Depth: 23.60 inches
Width: 17.62 inches (flanges meet dimensional requirements for standard 19-inch RETMA rack)

Temperature

Storage: –40°C to +80°C
Operating: 0°C to 50°C inlet ambient (unrestricted)

Thermal Shock

30°C/hour maximum

Humidity

10% to 90% without condensation

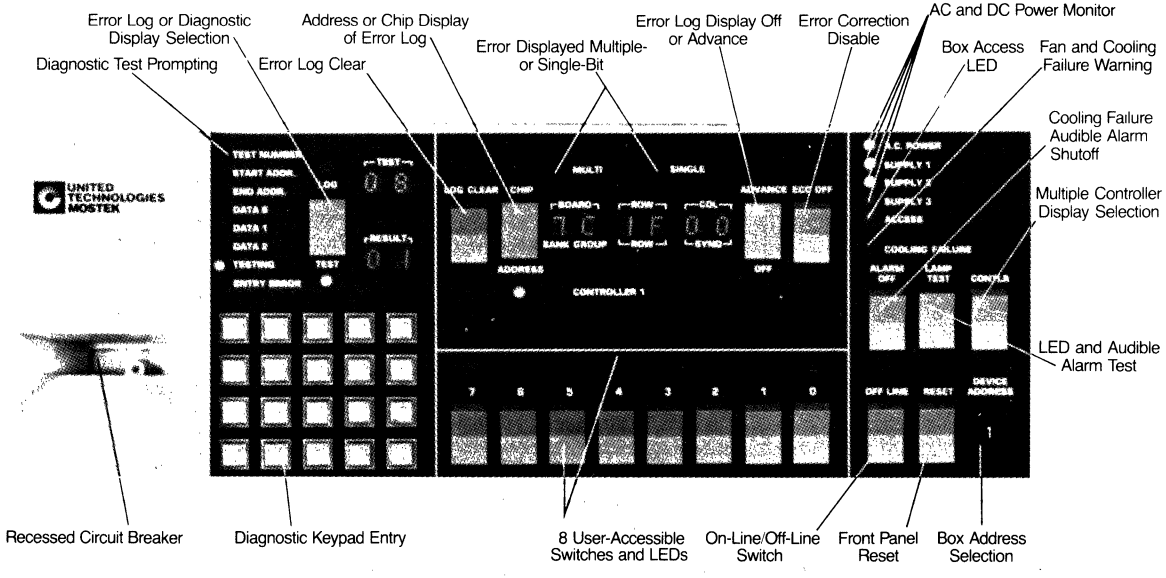
AC Power Requirements

115 ± 10% 47 Hz - 63 Hz, 30 A Max.
or
220 ± 10% 47 Hz - 63 Hz, 15 A Max.
(power consumption depends on configuration and application)

†Extended capacities are achieved by reducing the number of card slots available for user-option control boards and increasing the number of memory array card slots. Chassis size is unaffected.

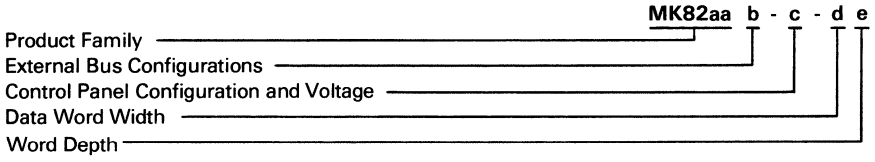
DISPLAY PANEL

Figure 2



ORDERING INFORMATION

The Mostek MK8200 is a family of high density, high performance memory subsystems. Many system configurations are available; these are detailed in the individual product descriptions. This section provides an overall numbering scheme for the MK8200 family. The available configurations are described by a three-part number, as defined below:



X

MK8200 PRODUCT FAMILY DESCRIPTION

Field aa is a two - digit field which comprehends the following variables:

1. Chassis Size
2. Internal Bus Structure (Maximum Word Width and Capacity)
3. Performance Thresholds which affect RAM type and/or Array Card Quantities
4. Custom Configurations

These numbers will be assigned sequentially as systems are configured, using the following as a starting point:

-10 Series = 72 Bit Internal
-30 Series = 48 Bit Internal
-50 Series = 24 Bit Internal

Existing Product Families are defined in the chart below:

MK8200 PRODUCT FAMILY CHART

Product Family	Chassis Size	Internal Bus		Inter-Leaving	RAM Type
		Width	Depth		
MK8210	15.75"	72 Bits	18 Arrays = 6 M Word (Standard Capacity)	4-Way	150 ns
MK8211	15.75"	72 Bits	24 Arrays = 8 M Word (Extended Capacity)	4-Way	150 ns
MK8220	15.75"	72 Bits	18 Arrays = 6 M Word (Standard Capacity)	None*	200 ns
MK8221	15.75"	72 Bits	24 Arrays = 8 M Word (Extended Capacity)	None*	200 ns
MK8230	15.75"	48 Bits	16 Arrays = 8 M Word (Split System)	4-Way	150 ns
MK8231	15.75"	48 Bits	24 Arrays = 12 M Word (Extended Capacity)	4-Way	150 ns
MK8232	15.75"	48 Bits	24 Arrays = 12 M Word (Extended Capacity)	None *	150 ns

All MK8200 Systems will support 4-Way interleaving if a sufficient population of memory exists. Systems denoted by a "" may not support interleaved operation at minimum populations.

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PRINTED IN USA March 1983