AN-595
Application Note

25-WATT AND 10-WATT VHF MARINE BAND TRANSMITTERS

Prepared by
John Hatchett
Applications Engineering

Design, performance and construction information are provided in this report for two power amplifiers suitable for VHF marine band (156-162 MHz) applications. Rated power output levels are 25 watts and 10 watts. Methods of meeting the FCC low power output (one watt or less) requirement are discussed in detail. Both amplifiers can be tuned to cover 144-175 MHz and performance data is provided for this frequency range.

MOTOROLA Semiconductor Products Inc.

25-WATT AND 10-WATT VHF MARINE BAND TRANSMITTERS

INTRODUCTION

This report gives design, performance and construction information for two 12.5 volt, FM transmitter power amplifiers designed for VHF marine band (156-162 MHz) applications. One of the amplifiers provides 25 watts of output power and the other 10 watts. Both have provisions for meeting the FCC requirement of being switchable to give one watt or less power output. Both designs have been subjected to open and short circuit load conditions at high line voltage and all load phase angles without damage to any transistor.

Components and construction techniques consistent with low cost, high volume production have been employed. The use of circuit designs and a printed circuit board layout which are common to both amplifiers minimizes the number of different components required and also makes it possible to extend the 10 watt amplifier to 25 watt capability by the addition of one more stage.

The amplifiers are tunable from 144 to 175 MHz and therefore are also useful for other VHF applications such as amateur two meter and land-mobile radio.

Performance information is given in Table 1 and also in the Transmitter Performance Section. A photograph of the amplifiers appears in Figure 1 and schematic diagrams in Figure 2.

DEVICE CONSIDERATIONS

The three RF transistor types employed in the amplifier designs are part of the Motorola VHF series optimized for 12.5 volt FM operation. They are of balanced emitter construction and the 25 watt device is manufactured using the Motorola *Isothermal technology process. The Isothermal design provides an additional measure of ruggedness to resist damage at high power levels over a wide range of thermal and VSWR excursions.

The power levels that each RF transistor must supply when the amplifiers are operating at rated output power at 158 MHz and 12.5 volts are given on the block diagrams of Figure 3. Both expected worst case power levels, as determined from the minimum specified device gains, and the power levels actually measured for constructed amplifiers have been included. A slight increase in these levels will be necessary to off-set any output harmonic filter loss. The expected effect of this additional loss (typically 0.3 to 0.5 dB) on the input power requirements can be obtained from Figure 13. The 10 watt amplifier shows the flexibility of achieving an optional, more economical, low power system from the 25 watt design simply by eliminating the 25 watt output stage and matching the 2N5590 driver into 50 ohms. If a lower input power is required, higher gain devices are available for use in the 10 watt design. Two additional line-ups are shown below with expected worst case power levels for 158 MHz, 12.5 volt operation.

135mw – 2N6255 – 2N6081 – 10w

80 mw – MRF607 – 2N6081 – 10w

The 2N6081 transistor is also of *Isothermal design and provides increased ruggedness as well as higher gain for the 10 watt system. For the 25 watt amplifier, the power required from the input stage will typically be less than one watt for 158 MHz operation. This makes the more economical 2N4427 device also a suitable candidate for this stage in 25 watt marine band applications. The design methods given in the following sections can also be applied to determine matching network component values for these alternate device line-ups.

An MJE2020 transistor is used in conjunction with a 1N5229 zener diode to provide a regulated dc supply voltage suitable for powering the transmitters during the low power output operating mode. The MJE2020 is a medium power transistor designed for use in general purpose audio amplifier and switching applications. The device is in the economical Motorola Case 199 plastic package. It is rated for a maximum continuous collector current of 5.0 A_{DC} and a maximum power dissipation of 80 watts at 25°C case temperature.

CIRCUIT DESCRIPTION

As indicated by the schematic diagrams of Figure 2, all the amplifier stages are of the common-emitter configuration and all are operated Class C. Except for a minor variation in the 2N5590 output network, all component values and transistor types used for the 10 watt amplifier are also common to the first two stages of the 25 watt amplifier.

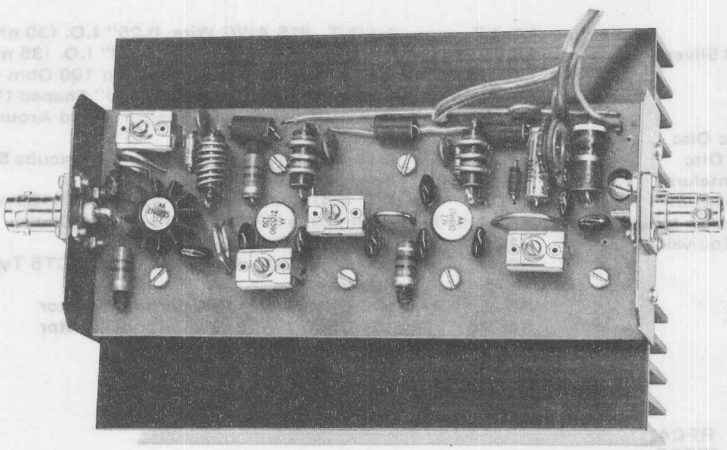
TRANSMITTER RF DESIGN

The transmitter gain stages have been designed for 158 MHz operation using large-signal transistor impedance data. These impedances for the 2N6082 and 2N5590 transistors appear in Figures 4 through 9. Large signal data for the 2N6255 transistor can be obtained from its data sheet. The resistive (R_{in}) and reactive (C_{in}, C_{out}) parallel impedance components are given by the curves. The

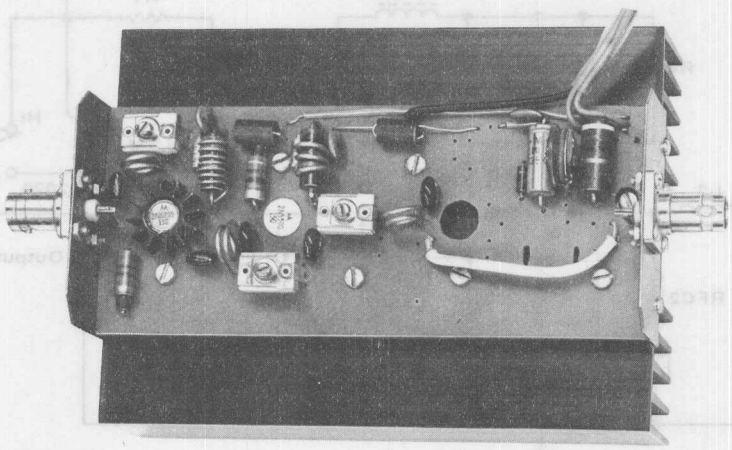
*Trademark of Motorola Inc.

TABLE 1 – Measured Performance at 158 MHz

	25 Watt Amplifier	10 Watt Amplifier
Vdc (Volts)	12.5	12.5
Power Input (mW)	75	180
Power Gain (dB)	25.2	17.4
Power Output Flatness (156.275-157.425 MHz) (dB)	±0.1	±0.1
2nd Harmonic Attenuation (dB)	40	40
Overall Efficiency of RF Stages (Percent)	56.8	44.5
DC Current (Amps):		
Total	3.61	1.89
Output Stage	2.70	1.60
Driver Stage	0.75	–
Input Stage	0.07	0.20
Power Switch Bias	0.09	0.09
Low Power Output ($\leq$1.0 Watt) Capability	Yes	Yes
Total DC Current for Low Power Output = 0.8 Watts (Amps)	0.95	1.08
Variation in Low Power Output for Cumulative Changes of ±2.0 dB in Power Input and 11.0 to 15.5 Volts in dc Supply Voltage (Watts)	<±0.2	<±0.2
Degradation in Input VSWR Between HI/LO Power Output (Percent)	<10	<10
Stability	Amplifiers are Stable for Input Drive Levels From Zero to Over 30 Percent Overdrive for V_{DC} Values from 8.0 to 15.5 Volts	
Ruggedness	No Transistor Damage for Open and Short Circuit Load Conditions for All Load Phase Angles and High Line of 15.5 Volts	



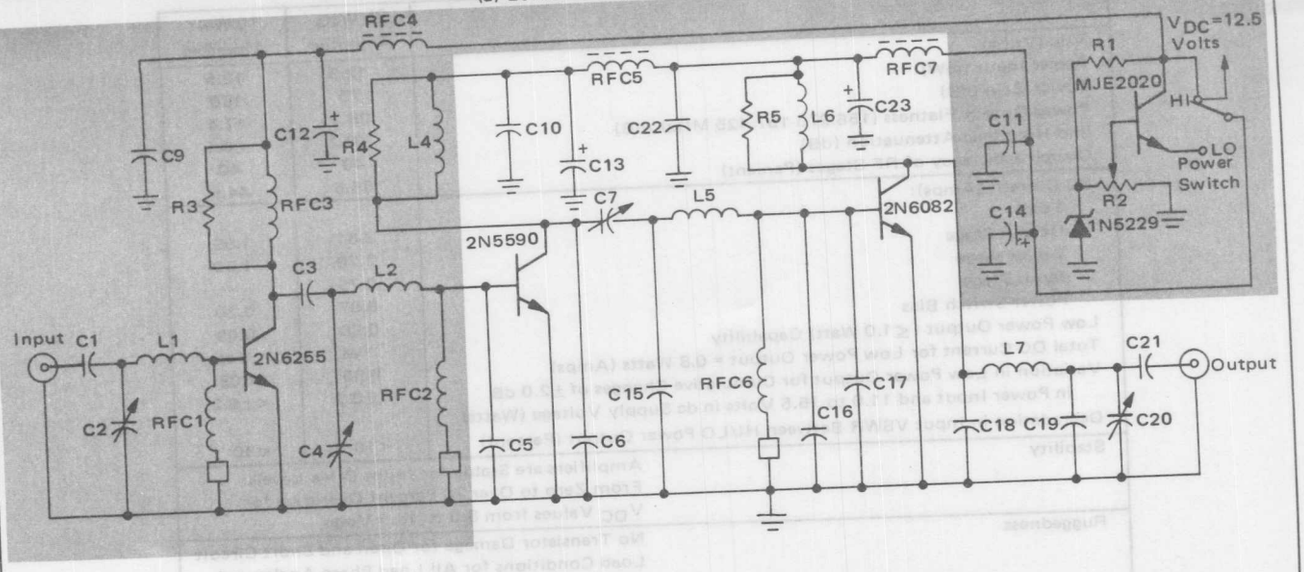
(a) 25 Watt Amplifier



(b) 10 Watt Amplifier

FIGURE 1 – Photograph of VHF Marine Transmitter Power Amplifiers

(a) 25 Watt Amplifier Schematic



NOTES:

1. Shaded components are common to both 25 Watt and 10 Watt systems.
2. Component designations C8 and L3 are not used in 25 Watt system.
3. Amplifiers constructed on 0.62", single sided, G10, printed circuit board.

C1, C3	– 10 pF	Dipped Silvered Mica	
C5, C6, C16, C17, C18	– 56 pF		
C8	– 36 pF		
C15, C21	– 22 pF		
C19	– 33 pF		
C9, C10, C22	– 0.001 μF Ceramic Disc		
C11	– 0.01 μF Ceramic Disc		
C12, C13, C23	– 1.0 μF, 35 V, Tantalum		
C14	– 10 μF, 25 V, Tantalum		
C2, C4, C7, C20	– 8-60 pF Compression Mica Trimmer ARCO #404 or Equivalent		

L1, L2	– 1-1/2 T, #16 AWG Wire, 0.25" I.D. (30 nH)
L3	– 1-1/2 T, #16 AWG Wire, 0.30" I.D. (35 nH)
L4, L6	– 3 T, #16 AWG Wire, Wound on 100 Ohm Resistor (45 nH)
L5	– #16 AWG Wire, 0.8" Long, "U" Shaped (12 nH)
L7	– #16 AWG Wire, 1.1" Long, Formed Around 0.6" Dia. Cyl. (15 nH)
RFC1, 2, 6	– 0.15 μH Molded Choke with Ferroxcube 5659065/3B Ferrite Bead on Ground Lead
RFC3	– 7 T, #20 AWG Wire, Wound on R3 (100 nH)
RFC4, 5, 7	– Ferroxcube VK200 19/4B Ferrite Choke
R1	– 91 Ohm, 2 W, ±5% Carbon Resistor
R2	– 100 Ohm, 0.25 W, Potentiometer, CTS Type R101B or Equivalent
R3	– 560 Ohm, 1 W, ±10% Carbon Resistor
R4, R5	– 100 Ohm, 1 W, ±10% Carbon Resistor

(b) 10 Watt Amplifier Schematic

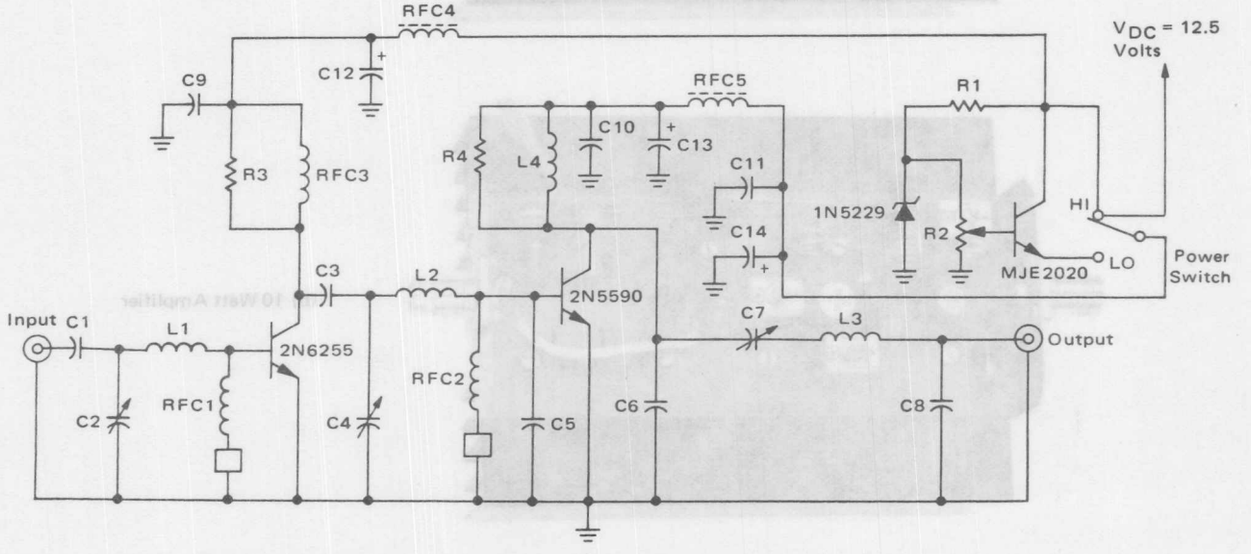
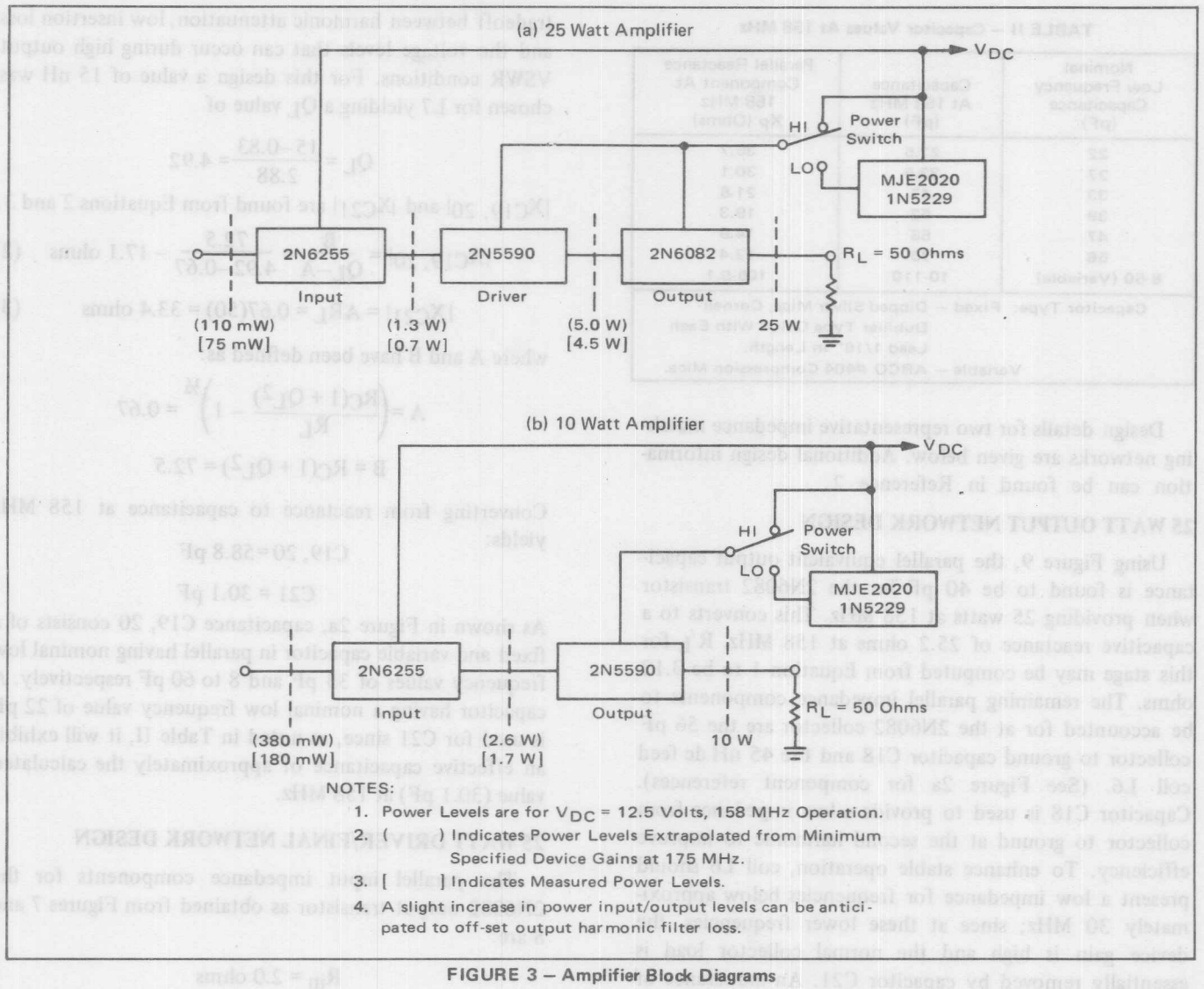


FIGURE 2 – Schematic Diagrams for 25 Watt and 10 Watt Amplifiers



NOTES:

1. Power Levels are for V_{DC} = 12.5 Volts, 158 MHz Operation.
2. ( ) Indicates Power Levels Extrapolated from Minimum Specified Device Gains at 175 MHz.
3. [ ] Indicates Measured Power Levels.
4. A slight increase in power input/output levels can be anticipated to off-set output harmonic filter loss.

FIGURE 3 – Amplifier Block Diagrams

approximate resistive portion of the load (R'_L), that must be presented to the collector by the associated matching network, has been calculated for an output power level, P, and a collector supply voltage, V_{CC}, from Equation 1.

$$R'_L = \frac{(V_{CC})^2}{2P} \qquad (1)$$

A detailed discussion related to the characterization of RF power transistors for large signal input and output impedances and the derivation and limitations of Equation 1 can be found in Reference 1. It is anticipated that several of the RF Power transistors applicable to VHF marine band transmitters will have their large signal impedance characterizations published in series equivalent form (R±jX) in the future. This data will provide R'_L directly; thus minimizing the need for the approximate solution provided by Equation 1. The designer is cautioned to pay particular attention to all large signal impedance data to determine whether it is in series or parallel equivalent form and to use it accordingly.

In all cases the transistor matching networks have been designed for the lowest Q that is still consistent with practical component values, reasonable harmonic suppression and smooth tuning. This permits the transmitters to be adjusted for an approximately flat response over the 156.275 to 157.425 MHz frequency band allocated to ship to ship and ship to shore communications.

For the 10 watt transmitter, the network following the 2N5590 transistor must step impedance up to match the 50 ohm load. For the 25 watt transmitter, this network must step the impedance down to match the combined base to ground impedance of the 2N6082 transistor. To best achieve these two varying requirements and still facilitate using a common printed circuit layout, two matching network configurations have been used (See Figure 2).

All fixed value capacitors from 12 to 56 pF used in the amplifiers are dipped silvered mica units. The effective capacitance of these components at 158 MHz will deviate from their low frequency value for nominal capacitance values above approximately 15 pF. These larger valued capacitors have been characterized at 158 MHz and the results tabulated in Table II. The table also provides the capacitance range at 158 MHz for the 8-60 pF variable capacitors.

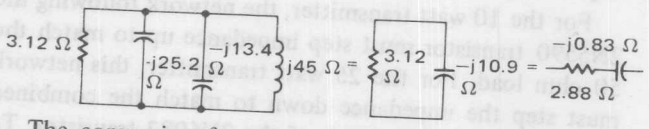
TABLE II – Capacitor Values At 158 MHz

Nominal Low Frequency Capacitance (pF)	Capacitance At 158 MHz (pF)	Parallel Reactance Component At 158 MHz Xp (Ohms)
22	27.5	36.7
27	33.5	30.1
33	47	21.8
39	52	19.3
47	68	14.9
56	75	13.4
8-60 (Variable)	10-110	108-9.1
Capacitor Type: Fixed – Dipped Silver Mica, Cornell-Dubilier Type CM04 With Each Lead 1/16" in Length. Variable – ARCO #404 Compression Mica.		

Design details for two representative impedance matching networks are given below. Additional design information can be found in Reference 2.

25 WATT OUTPUT NETWORK DESIGN

Using Figure 9, the parallel equivalent output capacitance is found to be 40 pF for the 2N6082 transistor when providing 25 watts at 158 MHz. This converts to a capacitive reactance of 25.2 ohms at 158 MHz. R'_L for this stage may be computed from Equation 1 to be 3.12 ohms. The remaining parallel impedance components to be accounted for at the 2N6082 collector are the 56 pF collector to ground capacitor C18 and the 45 nH dc feed coil L6. (See Figure 2a for component references). Capacitor C18 is used to provide a low impedance from collector to ground at the second harmonic to improve efficiency. To enhance stable operation, coil L6 should present a low impedance for frequencies below approximately 30 MHz; since at these lower frequencies, the device gain is high and the normal collector load is essentially removed by capacitor C21. An inductance of 45 nH meets this condition and also permits adequate decoupling from the dc line at 158 MHz. Accounting for L6 and using the 158 MHz value from Table II of 75 pF for C18 gives the total impedance at the 2N6082 collector to be:



The conversion from parallel to series form has been made using Equation 1 of the Appendix. The output network must therefore be designed to transform the 50 ohm external load to the conjugate of 2.88 ohms resistance in series with 0.83 ohms negative reactance. The required load impedance that must be present to the collector is therefore 2.88 + j 0.83 ohms as noted in Figure 10.

For the purpose of network design, an operator (Q_L) for the network in Figure 10 will be defined as $\frac{X_{L7} + X_C}{R_C}$ It should be noted that this Q_L is not intended to represent the loaded Q as defined by the 3 dB bandwidth points of the network. Values of Q_L, when defined as $\frac{X_{L7} + X_C}{R_C}$ of approximately 5 to 8 will provide a good tradeoff between harmonic attenuation, low insertion loss and the voltage levels that can occur during high output VSWR conditions. For this design a value of 15 nH was chosen for L7 yielding a Q_L value of

$$Q_L = \frac{15-0.83}{2.88} = 4.92$$

$|X_{C19, 20}|$ and $|X_{C21}|$ are found from Equations 2 and 3.

$$|X_{C19, 20}| = \frac{B}{Q_L - A} = \frac{72.5}{4.92-0.67} = 17.1 \text{ ohms} \quad (2)$$

$$|X_{C21}| = AR_L = 0.67(50) = 33.4 \text{ ohms} \quad (3)$$

where A and B have been defined as:

$$A = \left(\frac{R_C(1 + Q_L^2)}{R_L} - 1\right)^{1/2} = 0.67$$

$$B = R_C(1 + Q_L^2) = 72.5$$

Converting from reactance to capacitance at 158 MHz yields:

$$C19, 20 = 58.8 \text{ pF}$$

$$C21 = 30.1 \text{ pF}$$

As shown in Figure 2a, capacitance C19, 20 consists of a fixed and variable capacitor in parallel having nominal low frequency values of 33 pF and 8 to 60 pF respectively. A capacitor having a nominal low frequency value of 22 pF is used for C21 since, as noted in Table II, it will exhibit an effective capacitance of approximately the calculated value (30.1 pF) at 158 MHz.

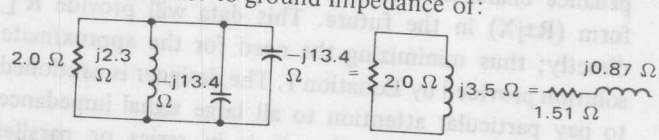
25 WATT DRIVER/FINAL NETWORK DESIGN

The parallel input impedance components for the 2N6082 output transistor as obtained from Figures 7 and 8 are:

$$R_{in} = 2.0 \text{ ohms}$$

$$C_{in} = -440 \text{ pF}$$

The negative sign associated with C_{in} indicates the actual parallel reactance component is an inductance. At 158 MHz this inductive reactance will have a value of 2.3 ohms. The two external base to ground capacitors, C16 and C17 (see Figure 2a for component references) provide a course impedance match at 158 MHz and a low impedance to ground at the second harmonic. Two capacitors in parallel have been used to minimize lead inductance and to provide an electrically symmetrical arrangement. Neglecting the effect of RFC6 but including measured values from Table II for C16 and C17 yields a combination base to ground impedance of:



Again Equation 1 of the Appendix has been used to convert from parallel to series form.

As noted in Figure 3a the required output power from the 2N5590 transistor is approximately 5 watts. For this condition, the parallel output impedance components are

PARALLEL EQUIVALENT INPUT RESISTANCE versus FREQUENCY

FIGURE 4 – 2N5590

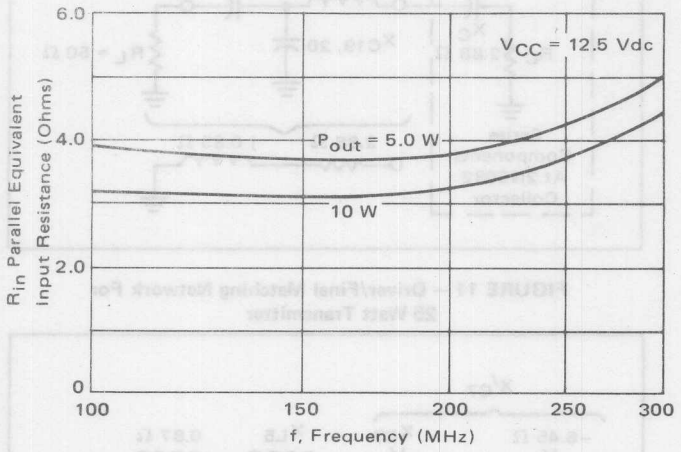
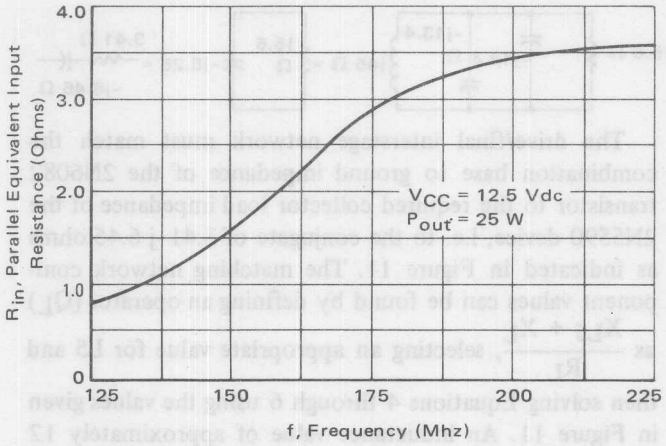


FIGURE 7 – 2N6082



PARALLEL EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

FIGURE 5 – 2N5590

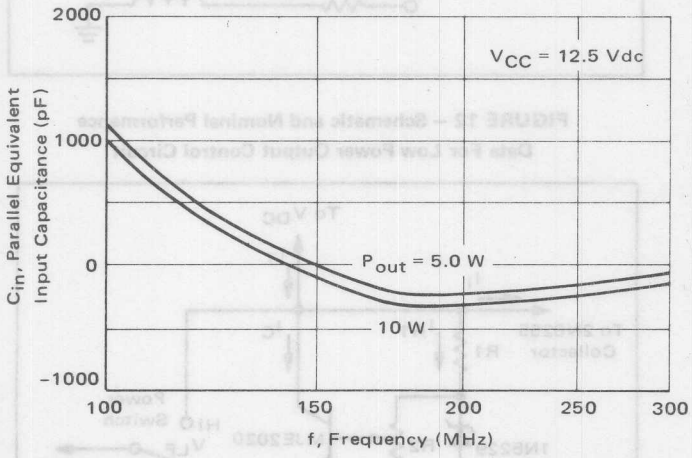
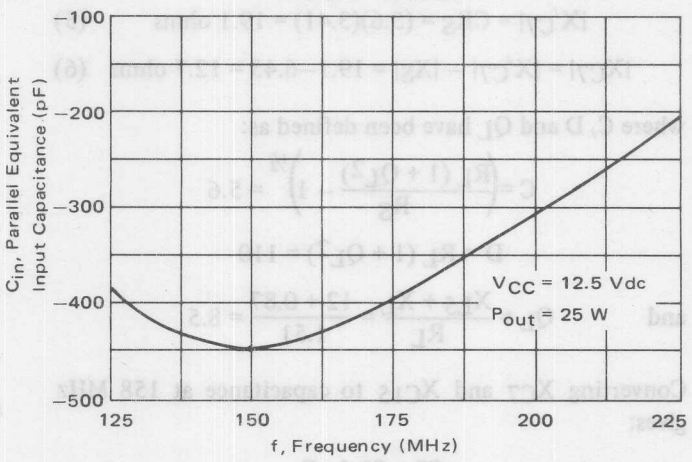


FIGURE 8 – 2N6082



PARALLEL EQUIVALENT OUTPUT CAPACITANCE versus FREQUENCY

FIGURE 6 – 2N5590

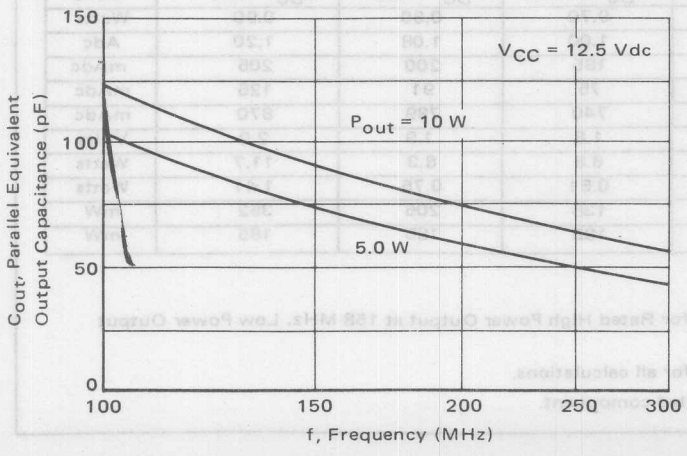
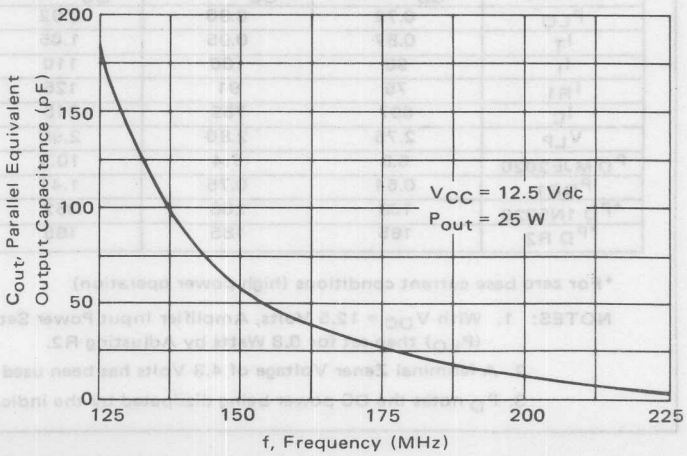
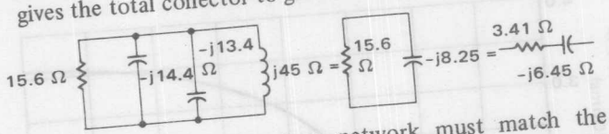


FIGURE 9 – 2N6082



15.6 ohms and 70 pF as obtained from Equation 1 and Figure 6. An external capacitor, C6 from collector to ground and a low inductance dc feed coil, L4, have again been used. Accounting for these two external components gives the total collector to ground impedance as:



The drive/final interstage network must match the combination base to ground impedance of the 2N6082 transistor to the required collector load impedance of the 2N5590 device, i.e. to the conjugate of 3.41 -j 6.45 ohms as indicated in Figure 11. The matching network component values can be found by defining an operator (Q_L) as $\frac{X_{L5} + X_L}{R_L}$, selecting an appropriate value for L5 and then solving Equations 4 through 6 using the values given in Figure 11. An inductance value of approximately 12 nH for L5 meets the requirements of providing a low Q network and component values which are practical to achieve.

$$|X_{C15}| = \frac{D}{Q_L - C} = \frac{110}{8.5\text{-}5.6} = 38 \text{ ohms} \quad (4)$$

$$|X'_{C7}| = CR_S = (5.6)(3.41) = 19.1 \text{ ohms} \quad (5)$$

$$|X_{C7}| = |X'_{C7}| - |X_S| = 19.1 - 6.45 = 12.7 \text{ ohms} \quad (6)$$

where C, D and Q_L have been defined as:

$$C = \left(\frac{R_L(1 + Q_L^2)}{R_S} - 1\right)^{1/2} = 5.6$$

$$D = R_L(1 + Q_L^2) = 110$$

and $$Q_L = \frac{X_{L5} + X_L}{R_L} = \frac{12 + 0.87}{1.51} = 8.5$$

Converting X_{C7} and X_{C15} to capacitance at 158 MHz gives:

C7 = 79.5 pF

C15 = 26.5 pF

FIGURE 10 – Output Network Configuration For 25 Watt Transmitter

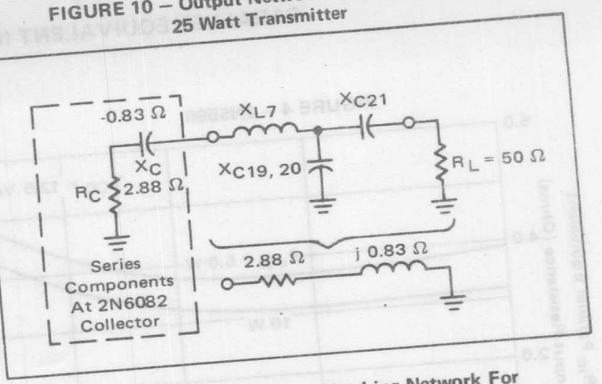


FIGURE 11 – Driver/Final Matching Network For 25 Watt Transmitter

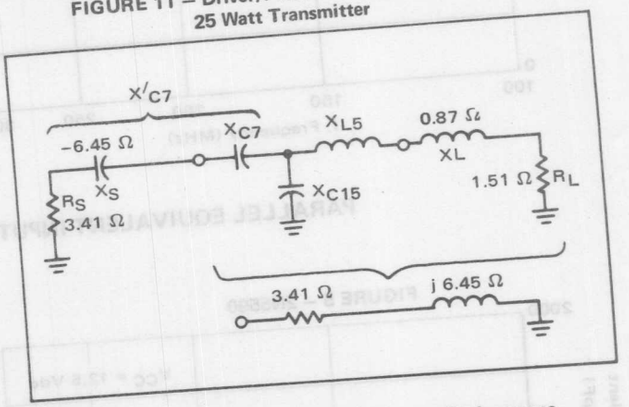
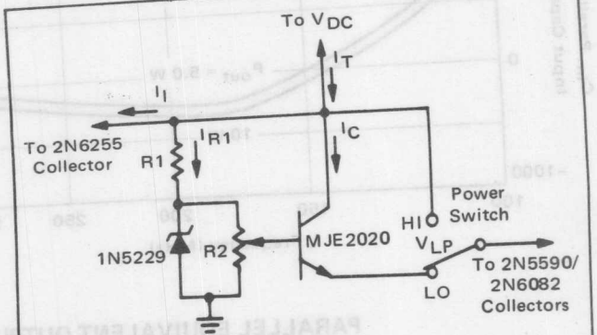


FIGURE 12 – Schematic and Nominal Performance Data For Low Power Output Control Circuit



R1 – 91 Ohm, 2 W, ± 5%
R2 – 100 Ohm, 1/4 W, Potentiometer

Quantity	25 Watt Transmitter			10 Watt Transmitter			Units
	V_{DC} = 11.0 V	V_{DC} = 12.5 V	V_{DC} = 15.5 V	V_{DC} = 11.0 V	V_{DC} = 12.5 V	V_{DC} = 15.5 V	
P_{LO}	0.72	0.80	0.92	0.70	0.80	0.90	Watts
I_T	0.87	0.95	1.05	1.00	1.08	1.20	Adc
I_I	98	100	110	185	200	205	mAdc
I_{R1}	75	91	125	75	91	125	mAdc
I_C	697	759	815	740	789	870	mAdc
V_{LP}	2.75	2.80	2.90	1.8	1.9	2.0	Volts
$P_{D\ MJE2020}$	5.8	7.4	10.3	6.8	8.3	11.7	Watts
P_{DR1}	0.51	0.75	1.41	0.51	0.75	1.41	Watts
*$P_{D\ 1N5229}$	138	206	352	138	206	352	mW
*$P_{D\ R2}$	185	185	185	185	185	185	mW

*For zero base current conditions (high power operation)

NOTES: 1. With V_{DC} = 12.5 Volts, Amplifier Input Power Set for Rated High Power Output at 158 MHz. Low Power Output (P_{LO}) then set for 0.8 Watts by Adjusting R2.

2. A Nominal Zener Voltage of 4.3 Volts has been used for all calculations.

3. P_D notes the DC power being dissipated by the indicated component.

Again, Table II indicates a fixed capacitor having a nominal low frequency value of 22 pF should be used for C15 and that the 8 to 60 pF trimmer capacitor is suitable for C7.

This completes the matching network discussion. Similar procedures can be followed for the remaining input and interstage networks. The printed circuit board layout has been configured to minimize interconnecting lead inductance in the RF signal path, however, in some cases it will be necessary to account for a small amount of additional interconnect inductance (on the order of 5 to 10 nH) in order to accurately determine the component values.

DESIGN CONSIDERATIONS FOR LOW POWER (≤ 1.0 WATT) OPERATION

The FCC regulations require that all VHF ship station transmitters operating in the 156-162 MHz band be equipped with a control for switching from rated power output to one watt or less power output. A variety of design problems can be encountered in meeting this requirement. The transmitter must be designed to remain stable under the different conditions imposed upon it during this radical variation from normal operation. In addition, tradeoffs in the low power circuitry between complexity, cost, and sensitivity of the low power output level with system variations must be considered.

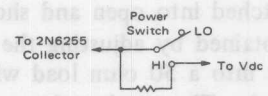
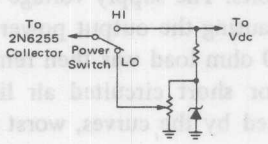
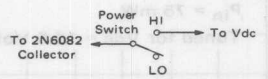
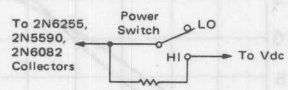
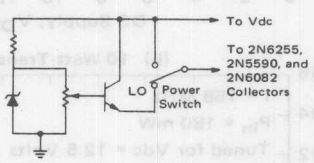
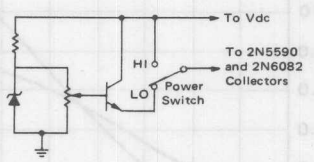
In general, the possible approaches available for reducing the output power to less than one watt can be divided into two categories:

a. The dc supply supply voltage can be altered to reduce the amount of RF gain available.

b. The RF signal level itself can be reduced.

Consideration has been given to both categories.

TABLE III – Performance of Low Power Control Circuits for 25 Watt Transmitter

Method	Description	Schematic Diagram	Advantages	Disadvantages	Comments
1	Decreasing DC Supply Voltage to Input Stage.				
	a. Using Dropping Resistor or Potentiometer.		a. Low Power Components are Adequate (Collector Current is Approximately 60 mAdc). b. Low Power Output Level can be Adjusted. c. Low Cost.	a. Very Low DC Collector Voltage Required (Approximately 1.0 Volt). b. Method 1a is Critical to Both Input Power and Vdc Variations. Method 1b is Critical to Input Power Variations. c. Degrades Input VSWR Significantly when Switching from High to Low Power.	Unsatisfactory—With 1a the Low Power Output will Nominally Vary from 0.15 to 1.0 Watt as Vdc Changes from 11.0 to 16.0 Volts. Both 1a and 1b Require Less Than ± 1.0 dB Variation in Input Power to Prevent Power Output from Exceeding 1.0 Watt or Being Cut-Off.
	b. Using Dropping Resistor and Zener Diode.				
2	Decreasing DC Supply Voltage to Driver Stage	Similar to Above	a. Relatively Low Power Components are Suitable but now must Control Approximately 250 mAdc. b. Doesn't Degrade Input VSWR as Badly as Method 1.	a. Required DC Collector Voltage is Still Low (Approximately 2.0 Volts). b. Critical to Input Power and/or Vdc Variations. c. Input Stage is Operating at Full Power Level with Mismatched Load.	Unsatisfactory—Similar to Above.
3	Removing DC Supply Voltage to Output Stage.		a. Lowest in Cost. b. Low Effect on Input VSWR. c. Relatively Insensitive to Both Input Power and VDC Variations.	a. Relatively Low Power Output is Achieved (Approximately 0.25 Watts). b. No Means of Adjusting Low Power Output Level. c. Driver Stage is Operating at Full Power Level with Mismatched Load.	Unsatisfactory—Low Power Output Varies only ± 0.2 Watt for *Standard Test Condition, but because of Extremely Low Initial Level (0.25 Watts) Absolute Value of Output can become too Low.
4	Decreasing DC Supply Voltage to all Three Stages.				
	a. Using High Power Dropping Resistor or Potentiometer.		a. Relatively Insensitive to Both Input Power and Vdc Variations. b. All Stages are Operating at Low Gain. c. Low Power Output Level can be Adjusted. d. Collector Voltage Values are Higher (Approximately 3.5 Volts).	a. High DC Current Level Involved. b. Bulky-High Power Resistor Required. c. Degrades Input VSWR.	Satisfactory—Low Power Output Varies ± 0.3 Watts for *Standard Test Condition. Most of Power Output Change is due to Vdc Variation.
	b. Using Zener Regulated DC Source.		a. Not Sensitive to Input Power or Vdc Variations. b. Suitable Low Cost Plastic Encapsulated Semiconductors are Available. c. Components are Relatively Compact and Light in Weight. d. Economical, Low Power, Potentiometer can be used to Set Low Power Output Level. e. Also b and d of Method 4a.	a. Must Provide Adequate Heat Sink for Control Transistor. b. Degrades Input VSWR.	Satisfactory—Low Power Output Varies Less Than ± 0.2 Watts for *Standard Test Condition.
5	Decreasing DC Supply Voltage to Driver and Output Stages Using Zener Regulated DC Source.		a. All the Advantages of Method 4b Except that Input Stage is now Operating at High Gain. b. Low Effect on Input VSWR.	a. Same as Method 4b but does not Significantly Effect Input VSWR. b. Input Stage is Operating at Full Power Level with Mismatched Load.	Recommended Choice—Low Power Output Varies Less Than ±0.2 Watts for Standard Test Condition. Input VSWR is Degraded Less Than 10% in Going from High to Low Power Output Operation.

*Standard Test Condition – Combined Changes of ± 2 dB in Power Input and 11.0 to 16.0 Volts in Vdc. Reference is Low Power Output of 0.8 Watts with Vdc = 12.5 Volts and Power Input Corresponding to that Required for 25 Watts High Power Output.

Attenuating the RF signal level appears to be the least desirable approach from the standpoint of circuit complexity, ease of achieving front panel control, and the effect on RF gain during normal power output operation. Many possible approaches of reducing power by altering the DC supply voltage have been investigated in detail for the 25 watt transmitter and the results summarized in Table III. These methods are of primary importance when a regulated dc supply is not being employed. If a dc regulator is being used then the decrease in dc supply voltage can best be accomplished in the dc regulator circuitry. Each method of Table III has been evaluated on the basis of:

a. Variation of power amplifier input VSWR when switched from normal to low power operation.

b. Sensitivity of low power output level to changes in battery voltage and input drive power.

c. Cost.

d. Adjustability of output power level.

e. Physical size of components.

Method 5 of Table III appears to offer the best overall choice and this approach has been incorporated in both the 25 watt and 10 watt transmitter designs. If, however, cost is of primary concern, an appropriate power resistor can be used to drop the dc supply voltage to the driver and output stage (similar to Method 4a).

Nominal current, voltage and component power dissipation values for Method 5 are given in Figure 12 for both the 25 and 10 watt transmitters. Heat sink considerations for the MJE2020 transistor are considered in the Thermal Design Section.

TRANSMITTER PERFORMANCE

In addition to the data given in Table I, the curves in Figures 13 and 14 provide additional performance information for a 25 watt and a 10 watt transmitter operating at 158 MHz. Figure 15 shows the amount of input power and dc current required for the 25 watt amplifier for various values of dc supply voltage. This information will be of use if it is intended to use a regulated dc supply to drive the transmitter since the regulated dc voltage will, of necessity, be reduced below the nominal battery voltage.

Figures 16 and 17 provide performance information for the transmitters when tuned for other frequencies in the 144 to 175 MHz band.

High load VSWR testing has been done on both amplifiers at high line voltage and for all load phase angles without damage to any transistor. Figure 18 indicates current and power dissipation levels that can be experienced when the 25 watt amplifier output is mismatched into open and short circuit loads. This data was obtained by adjusting the amplifier for rated power output into a 50 ohm load with a dc supply voltage of 13.6 volts. The supply voltage was then increased to 15.5 volts causing the output power to increase to 32.5 watts. The 50 ohm load was then removed and replaced with an open or short circuited air line of variable length. As indicated by the curves, worst case power dissipation for

FIGURE 13 – Power Output And DC Current Versus Power Input

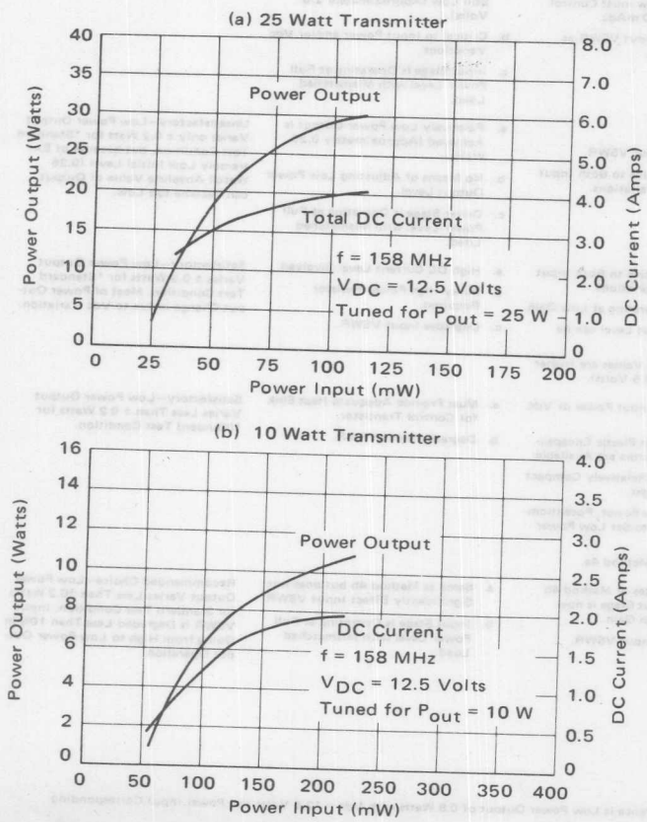


FIGURE 14 – Power Output And DC Current Versus DC Supply Voltage

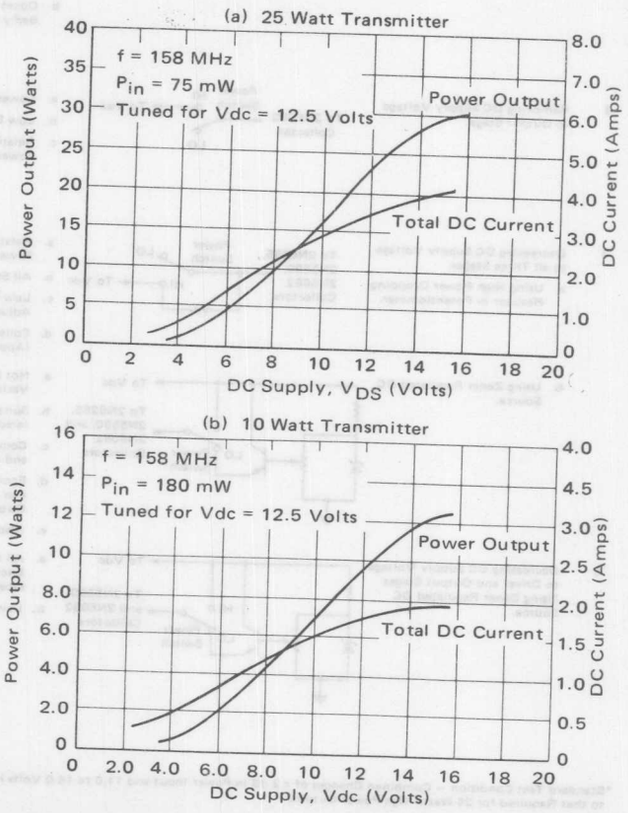
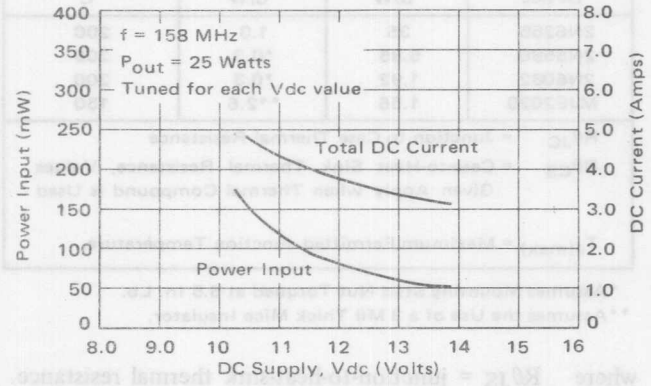


FIGURE 15 – Power Input and DC Current versus DC Supply Voltage for Rated Power Output



the output stage can increase from a normal 50 ohm load value of 13.3 watts to approximately 75 watts. Prolonged operation in this worst case condition with an ambient temperature of only 25°C will require a heat sink specification for the 2N6082 transistor of 0.12°C/W in order to keep the device junction temperature from exceeding 200°C. Designing the heat sink to be adequate for this infrequent mode of operation would normally be uneconomical and impractical. Therefore, if it is required to operate with this worst case load condition, the need for a protection circuit which will reduce either the RF drive power, the dc supply voltage, or the dc supply

FIGURE 16 – Power Output and DC Current versus Power Input at 175 MHz

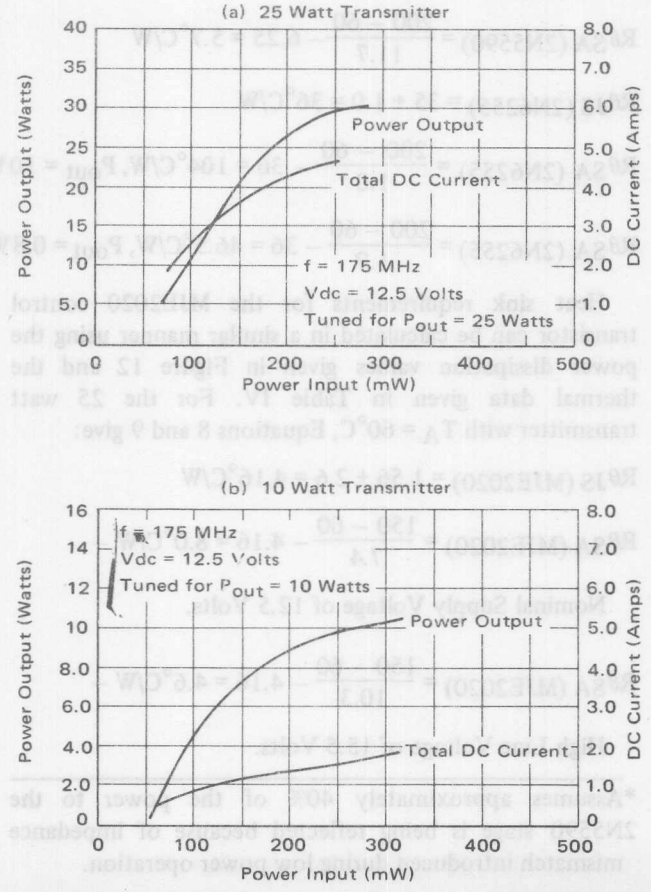
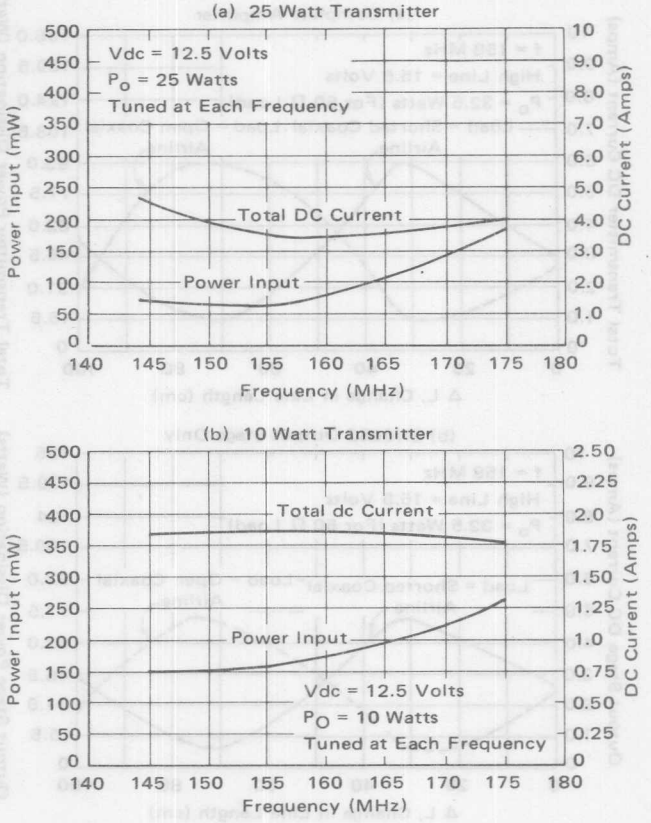


FIGURE 17 – Power Input and DC Current for VHF Band Operation



current during high VSWR load conditions should be considered even though transistors capable of withstanding infinite VSWR conditions are used. It is, however, important to use transistors capable of withstanding momentary worst case short and open load conditions so as to prevent device failure during the reaction time of the protection circuitry. The 2N5590 and 2N6082 output devices exhibit this degree of ruggedness.

THERMAL DESIGN

Proper thermal analysis and good thermal construction techniques are very important in RF power transmitter design and fabrication. Transmitter construction should include the use of:

a. A smooth heat sink surface to maximize heat sink to transistor case contact area.

b. A proper amount of thermal joint compound between heat sink and transistor case interface.

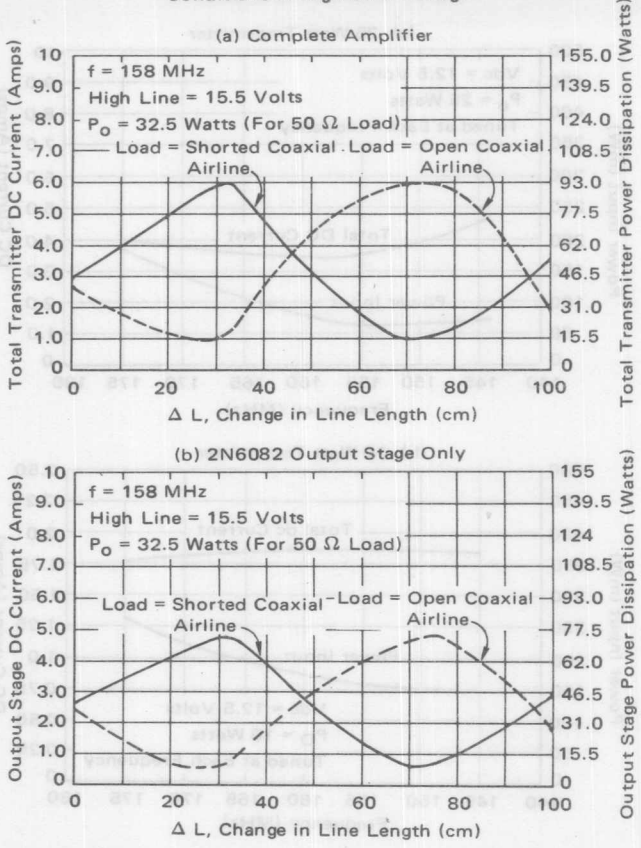
c. Torque as specified for the transistor when fastening the transistor to the heat sink.

d. A heat sink configuration that will permit locating the higher power level stages near the maximum heat transfer position on the heat sink.

Using the measured dc current values given in Table I and the measured RF power levels given in Figure 3, the approximate power dissipated in each transmitter RF stage, P_D, can be calculated from Equation 7.

$$P_D = P_{in(rf)} + P_{in(dc)} - P_{out(rf)} \quad (7)$$

FIGURE 18 – 25 Watt Amplifier Power Dissipation and DC Current for Open and Short Circuit Load Conditions at High Line Voltage



Power Input Set for Power Output = 25 Watts With V_{DC} = 13.6 Volts

Power dissipation for the 2N6255 and 2N5590 devices will be greater for the 10 watt transmitter and, in the case of the 2N6255 device, the worst dissipation will occur during the low power mode of operation. This happens, since at this time, the 2N6255 stage is receiving normal dc voltage and RF drive power but is working into a mismatched load.

Solving Equation 7 for a dc supply voltage of 12.5 volts yields:

2N6082 stage, P_D = 13.3 W – 25 Watt Amplifier

2N5590 stage, P_D = 11.7 W – 10 Watt Amplifier

2N6255 stage, P_D = { 1.0 W – 10 Watt Amplifier Operating at Rated Power; *1.7 W – 10 Watt Amplifier Operating in Low Power Mode

Thermal data for the transistors being used appears in Table IV.

For any single transistor stage, the heat sink to ambient thermal resistance ($R\theta_{SA}$) requirement may be computed from Equations 8 and 9.

$$R\theta_{JS} = R\theta_{JC} + R\theta_{CS} \quad (8)$$

$$R\theta_{SA} = \frac{T_{j(max)} - T_A}{P_D} - R\theta_{JS} \quad (9)$$

TABLE IV – Thermal Data

Device	$R\theta_{JC}$ °C/W	$R\theta_{CS}$ °C/W	$T_{J(max)}$ °C
2N6255	35	1.0	200
2N5590	5.85	*0.3	200
2N6082	1.92	*0.3	200
MJE2020	1.56	**2.6	150

$R\theta_{JC}$ = Junction to Case Thermal Resistance

$R\theta_{CS}$ = Case-to-Heat Sink Thermal Resistance, Values Given Apply when Thermal Compound is Used

$T_{J(max)}$ = Maximum Permitted Junction Temperature

*Assumes Mounting Stud Nut Torqued at 6.5 In. Lb.

**Assumes the Use of a 3 Mil Thick Mica Insulator.

where $R\theta_{JS}$ = junction-to-heat-sink thermal resistance.

T_A = ambient temperature.

Heat sink requirements for the 25 watt transmitter output stage can be obtained by using the appropriate P_D value and data from Table IV in Equations 8 and 9. If the maximum ambient temperature requirement is assumed to be 60°C this gives:

$$R\theta_{JS}\ (2N6082) = 1.92 + 0.3 = 2.22°C/W$$

$$R\theta_{SA}\ (2N6082) = \frac{200 - 60}{13.3} - 2.22 = 8.3°C/W$$

Calculating heat sink requirements for the 10 watt transmitter in a like manner yields:

$$R\theta_{JS}\ (2N5590) = 5.85 + 0.3 = 6.25°C/W$$

$$R\theta_{SA}\ (2N5590) = \frac{200 - 60}{11.7} - 6.25 = 5.7°C/W$$

$$R\theta_{JS}\ (2N6255) = 35 + 1.0 = 36°C/W$$

$$R\theta_{SA}\ (2N6255) = \frac{200 - 60}{1.0} - 36 = 104°C/W, P_{out} = 10\,W$$

$$R\theta_{SA}\ (2N6255) = \frac{200 - 60}{1.7} - 36 = 46.5°C/W, P_{out} = 0.8\,W$$

Heat sink requirements for the MJE2020 control transistor can be calculated in a similar manner using the power dissipation values given in Figure 12 and the thermal data given in Table IV. For the 25 watt transmitter with T_A = 60°C, Equations 8 and 9 give:

$$R\theta_{JS}\ (MJE2020) = 1.56 + 2.6 = 4.16°C/W$$

$$R\theta_{SA}\ (MJE2020) = \frac{150 - 60}{7.4} - 4.16 = 8.0°C/W -$$

Nominal Supply Voltage of 12.5 Volts.

$$R\theta_{SA}\ (MJE2020) = \frac{150 - 60}{10.3} - 4.16 = 4.6°C/W -$$

High Line Voltage of 15.5 Volts.

*Assumes approximately 40% of the power to the 2N5590 stage is being reflected because of impedance mismatch introduced during low power operation.

The MJE2020 device only dissipates significant power during transmission in the low power mode. During this time the power being dissipated by the output stage RF transistor is negligible. Therefore, if the MJE2020 is properly located near the RF output device, a common heat sink will serve both transistors.

The following points apply:

a. The $R\theta_{SA}$ values have been computed for continuous transmitter operation. The heat sink requirements will be reduced for duty cycle conditions.

b. If operation into mismatched loads is anticipated, the $R\theta_{SA}$ values must be modified to take into account the increased dissipation that can occur for these operating conditions.

c. It is not necessary for the heat sink to extend the entire amplifier length as shown in Figure 1. The only requirement is that the sink meet the $R\theta_{SA}$ requirements of the driver, final and control transistors.

CONSTRUCTION

The amplifiers have been constructed to minimize the amount of modifications required prior to reproducing the units economically in large quantities:

a. Low cost components have been used.

b. The number of tuning adjustments have been minimized.

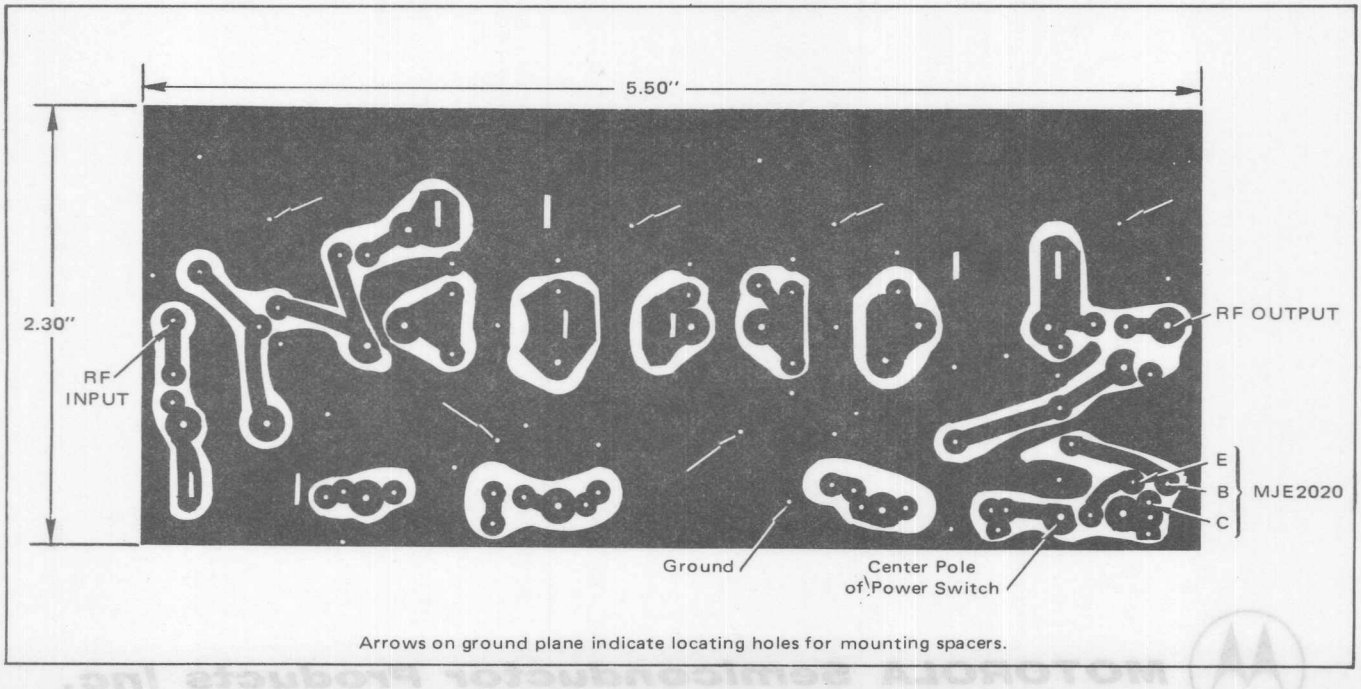
c. A commonality of components exists between the 25 watt and 10 watt transmitters.

d. Single sided printed circuit board construction adaptable to high volume assembly techniques such as wave soldering and automatic component insertion has been employed. A full scale layout for the board artwork appears in Figure 19.

The printed circuit board of Figure 19 has been laid out to minimize component lead length and interconnection inductance in the RF signal path and to maximize the amount of area available for the ground plane. It is imperative that the high level ground currents for the 25 watt output stage be confined as much as possible to this stage and not permitted to circulate in the vicinity of the low level input stage. If this conduction does occur, a degradation in transmitter gain and also an unnecessary increase in input VSWR when switching from normal to low power operation can result. Controlling the ground current flow becomes more difficult if a conducting plate, such as a heat sink, is grounded only near the amplifier output and input. This grounding condition will permit a significant portion of the load ground current to return to the output stage ground via the heat sink and low level input stage ground path. To alleviate this problem, additional RF ground returns must be provided between the heat sink and the circuit ground. Ground returns between the heat sink and the vicinity of each emitter lead for the 2N6082 and 2N5590 stages are especially important. These ground connections can be accomplished by using properly located spacers capable of providing a good RF connection between the printed circuit board ground and the heat sink. Suitable spacer locations are indicated in Figure 19.

Mounting and thermal information pertaining to the 2N5590 and 2N6082 device packages can be found in Reference 5. Ideally, these packages should be secured to the heat sink prior to being soldered into the circuit. This, however, is not easily achievable with the construction method being employed. Therefore, adequate precautions must be taken when soldering the device packages to the circuit board in order to assure proper alignment with the heat sink mounting holes and to eliminate tension

FIGURE 19 – Foil Side of Printed Circuit Board Artwork for 25/10 Watt VHF Power Amplifiers



between the ceramic to metal joints. Two alternate construction approaches are:

a. Put the amplifier circuit pattern on the component side of the board. This, however, will not permit the use of wave soldering techniques.

b. Use a double sided board layout which will require the use of plated through holes, eyelets or wrap-around grounds.

Regardless of the construction method used, it is essential to proper electrical performance that the RF transistors have their emitters grounded near the device package and that all component and interconnection lead lengths in the RF signal path be held to an absolute minimum.

The MJE2020 control transistor has been located on the back side of the printed circuit board to permit mounting directly on the heat sink. An alternate approach would be to locate the transistor on the component side over a cut out in the board and then use a spacer of low thermal resistance material between the heat sink and transistor. This second method would simplify assembly procedures at the expense of a slight increase in thermal resistance between the transistor case and heat sink. In either case, a mica washer must be used to electrically isolate the transistor from the sink. The MJE2020 device is available in several standard lead form configurations. The board layout of Figure 19 will accommodate configuration A. A description of the various lead configurations, mounting, and heat sinking techniques for the MJE2020 package (Case 199) are discussed in detail in Reference 6.

APPENDIX
SERIES AND PARALLEL EQUIVALENTS

To convert a parallel resistance and reactance combination to series:

$$R_S = \frac{R_P}{1 + \left(\frac{R_P}{X_P}\right)^2}, \quad X_S = \frac{X_P}{1 + \left(\frac{X_P}{R_P}\right)^2} \qquad (1)$$

To convert a series resistance and reactance combination to parallel:

$$R_P = R_S + \frac{(X_S)^2}{R_S}, \quad X_P = X_S + \frac{(R_S)^2}{X_S} \qquad (2)$$

REFERENCES

1. "Systemizing RF Power Amplifier Design," by Roy Hejhall, Application Note AN-282A.
2. "Matching Network Designs with Computer Solutions," by Frank Davis, Application Note AN-267.
3. "Design Techniques For an 80 Watt, 175 MHz Transmitter For 12.5 Volt Operation," by John Hatchett. Application Note AN-577.
4. "VHF Power Amplifiers Using Paralleled Output Transistors," by John Hatchett. Application Note AN-585.
5. "Mounting Stripline-Opposed-Emitter (SOE) Transistors," by Lou Danley. Application Note AN-555.
6. "Mounting Procedure For, And Thermal Aspects Of, Thermopad Plastic Devices," by Larry Wing. Application Note AN-290B.