DL138

MOTOROLA

FACT DATA

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Q2/88
DL138

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FACT DATA

Prepared by
Technical Information Center

This data book presents advanced information on Motorola's very high-speed, low-power advanced CMOS logic family.

FACT utilizes a sub 2 micron silicon gate CMOS process to attain speeds similar to that of Advanced Low Power Schottky while retaining the advantages of CMOS logic, namely, ultra low power and high noise immunity. As an added benefit, FACT offers the system designer superior line driving characteristics and excellent ESD and latchup immunity.

The FACT family consists of devices in two categories:

1. **AC,** standard logic functions with CMOS compatible inputs and TTL and MOS compatible outputs;

2. **ACT,** standard logic functions with TTL compatible inputs and TTL and MOS compatible outputs.

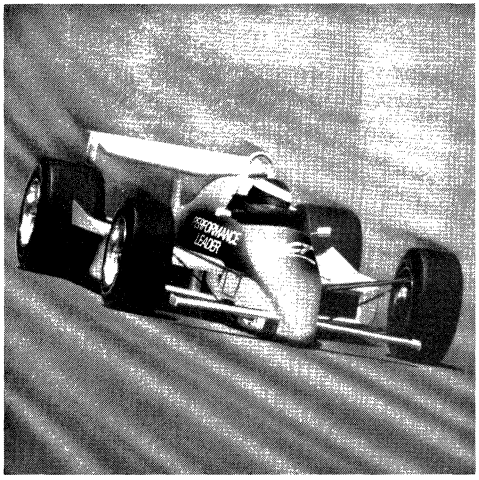
Series A

CONTENTS

Alphanumeric Index of Devices

MC74ACXX Devices — CMOS Input Levels

MC74ACTXX Devices — TTL Input Levels



Selection Information

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Functional Selection

Abbreviations

S = Synchronous
A = Asynchronous
B = Both Synchronous and Asynchronous

2S = 2-State Output
3S = 3-State Output

P = Planned (See FACT Selector Guide, SG-122 for latest availability status)

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Inverters

Description	Type of Output	No.	AC	ACT
Hex	2S	04	P	P

AND Gates

Description	Type of Output	No.	AC	ACT
Quad 2-Input	2S	08	P	P
Triple 3-Input	2S	11	P	P

NAND Gates

Description	Type of Output	No.	AC	ACT
Quad 2-Input	2S	00	P	P
Triple 3-Input	2S	10	P	P
Dual 4-Input	2S	20	P	

OR Gates

Description	Type of Output	No.	AC	ACT
Quad 2-Input	2S	32	P	P

NOR Gates

Description	Type of Output	No.	AC	ACT
Quad 2-Input	2S	02	P	P

Exclusive OR Gates

Description	Type of Output	No.	AC	ACT
Quad 2-Input	2S	86	P	

Schmitt Triggers

Description	Type of Output	No.	AC	ACT
Hex, Inverting	2S	14	P	P

Flip-Flops

Description	Clock Edge	No.	AC	ACT
Dual D w/Set & Clear	Pos	74	P	P
Dual $J\overline{K}$ w/Set & Clear	Pos	109	P	P
8-Bit D, Non-Inverting	Pos	825	P	P
8-Bit D, Inverting	Pos	826	P	P

Multiplexers

Description	Type of Output	No.	AC	ACT
Quad 2-to-1, Non-Inverting	2S	157	P	P
	3S	257	P	P
Quad 2-to-1, Inverting	2S	158	P	P
	3S	258	P	P
Dual 4-to-1, Non-Inverting	2S	153	P	P
	3S	253	P	P
Dual 4-to-1, Inverting	2S	352	P	P
	3S	353	P	P
8-to-1	2S	151	P	P
	3S	251	P	P
Quad 2-to-1 with Output Register				
398 — Positive edge triggered, $Q/\overline{Q}$ Outputs	2S	398	P	P
399 — Positive edge triggered, Q Output Only	2S	399	P	P

Decoders/Demultiplexers

Description	Type of Output	No.	AC	ACT
Dual 1-of-4	2S	139	P	P
1-of-8	2S	138	P	P

Latches

Description	No. of Bits	Type of Output	No.	AC	ACT
Transparent, Non-Inverting	8	3S	373	P	P
	9	3S	843	P	P
	9	3S	845	P	P
Octal, Non-Inverting	8	3S	573	P	P
Transparent, Inverting	8	3S	533	P	P
	8	3S	563	P	P
	9	3S	844	P	P
	9	3S	846	P	P

Shift Registers

Description	No. of Bits	Type of Output	Mode*				No.	AC	ACT
			SR	SL	Hold	Reset			
Parallel In-Parallel Out, Bidirectional	8	3S	X	X	X	A	299	P	P
	8	3S	X	X	X	S	323	P	P

* SR = Shift Right
SL = Shift Left

Asynchronous Counters — Negative Edge-Triggered

Description	Load	Set	Reset	No.	AC	ACT
14-Stage Binary			X	4020	P	
12-Stage Binary			X	4040	P	

Buffers/Line Drivers

Description	Type of Output	No.	AC	ACT
Octal, Non-Inverting	3S	241	P	P
	3S	244	P	P
Bus Pinout	3S	541	P	P
Octal, Inverting	3S	240	P	P
Bus Pinout	3S	540	P	P

Transceivers

Description	Type of Output	No.	AC	ACT
Octal, Non-Inverting	3S	245	P	P
	3S	640	P	P
	3S	643	P	P
Octal, Non-Inverting with	3S	646	P	
Register Mux Latch	OC	647		P
Octal, Inverting with Register Mux Latch	3S	648	P	

Cascadable Synchronous Counters — Positive Edge-Triggered

Description	Type of Output	Load	Reset	No.	AC	ACT
Decade	2S	S	A	160	P	P
	2S	S	S	162	P	P
Decade, Up/Down	2S	S		168	P	
	2S	A		190	P	
	2S	A	A	192*	P	
	3S	S	B	568	P	
4-Bit Binary	2S	S	A	161	P	P
	2S	S	S	163	P	P
4-Bit Binary,	2S	S		169	P	
Up/Down	2S	A		191	P	
	2S	A	A	193*	P	
	3S	S	B	569	P	

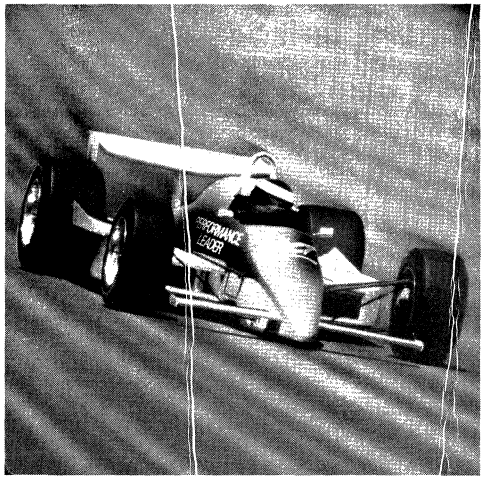
*The 192 and 193 do not provide a clock enable for synchronous cascading.

Comparators

Description	Type of Output	P=Q	P>Q	P<Q	No.	AC	ACT
4-Bit Identity	2S	X			520	P	P
	2S	X			521	P	P

MSI Flip-Flops/Registers

Description	No. of Bits	Type of Output	Set or Reset	Clock Enable	No.	AC	ACT
D-Type, Non-Inverting	4	2S		X	377	P	P
	6	2S	A		174	P	P
	6	2S		X	378	P	P
	8	2S	A		273	P	P
	8	3S			374	P	P
	8	3S			574	P	P
D-Type, Inverting	8	3S			534	P	P
	8	3S			564	P	P
D-Type, Q and $\overline{Q}$ Outputs	4	2S	A		175	P	P
	4	2S		X	379	P	P



Fact Description and Family Characteristics

2

FACT Descriptions and Family Characteristics

FACT — Logic

Motorola FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fan-out capability, extended power supply range and high reliability.

This data book describes the product line with device specifications as well as material discussing design considerations and comparing the FACT family to predecessor technologies.

The sub two-micron silicon gate CMOS process utilized in this family has been proven in the field. It has been further enhanced to meet and exceed the JEDEC standards for 74ACXX logic.

For direct replacement of LS, ALS and other TTL devices, the 'ACT circuits with TTL-type input thresholds are included in the FACT family. These include the more popular bus drivers/transceivers as well as many other 74ACTXXX devices.

2

Characteristics

- Full Logic Product Line
- Industry Standard Functions and Pinouts for SSI, MSI and LSI
- Meets or Exceeds JEDEC Standards for 74ACXX Family
- TTL Inputs on Selected Circuits
- High Performance Outputs
  - Common Output Structure for Standard and Buffer Drivers
  - Output Sink/Source Current of 24 mA
  - Transmission Line Driving 50 ohm (Commercial) Guaranteed
- Operation from 2–6 Volts Guaranteed
- Temperature Range −40°C to +85°C (Commercial)
- Improved ESD Protection Network
- High Current Latch-Up Immunity

Interfacing

FACT devices have a wide operating voltage range (V_{CC} = 2 to 6 Vdc) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:

'AC — This is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs that can drive ±24 mA of I_{OH} and I_{OL} current. Industry standard 'AC nomenclature and pinouts are used.

'ACT — This is a high-speed CMOS device with a TTL-to-CMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a V_{CC} = 5 V ± 0.5 V with V_{OH} = 2.4 V and V_{OL} = 0.4 V, but are functional over the entire FACT operating voltage range of 2 to 5.5 Vdc. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. 'ACT devices have the same output structures as 'AC devices.

Low Power CMOS Operation

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws three orders of magnitude less power than the equivalent LS or ALS TTL device. This enhances system reliability; because costly regulated high current power supplies, heat sinks and fans are eliminated, FACT logic devices are ideal for portable systems such as laptop computers and backpack communications systems. Operating power is also very low for FACT logic. Power consumption of various technologies with a clock frequency of 1 MHz is shown below.

FACT	=	0.1 mW/Gate
ALS	=	1.2 mW/Gate
LS	=	2.0 mW/Gate
HC	=	0.1 mW/Gate

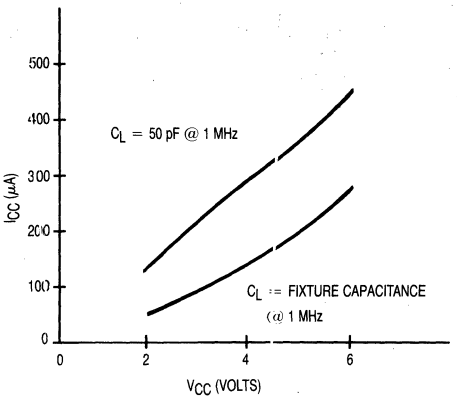


Figure 2-1. I_{CC} versus V_{CC}

Figure 2-1 illustrates the effects of I_{CC} versus power supply voltage (V_{CC}) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

AC Performance

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high-speed systems.

The example below describes typical values for a 74XX138, 3-to-8 line decoder.

FACT	=	6.0 ns @ C_L = 50 pF
ALS	=	12.0 ns @ C_L = 50 pF
LS	=	22.0 ns @ C_L = 15 pF
HC	=	17.5 ns @ C_L = 50 pF

AC performance specifications are guaranteed at 5 V ± 0.5 V and 3.3 V ± 0.3 V. For worst case design at 2 V V_{CC} on all device types, the formula below can be used to determine AC performance.

AC performance at 2 V V_{CC} = 1.9 x AC specification at 3.3 V.

Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the databook specification by 250 ps. This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and 5 V ± 10% V_{CC}.

Noise Immunity

The noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The comparisons shown describe the difference between the input threshold of a device and the output voltage, $|V_{IL} - V_{OL}|$ / $|V_{IH} - V_{OH}|$ at 4.5 V V_{CC}.

FACT	=	1.25/1.25 V
ALS	=	0.4/0.7 V
LS	=	0.3/0.7 V @ 4.75 V V_{CC}
HC	=	0.8/1.25 V

Output Characteristics

All FACT outputs are buffered to ensure consistent output voltage and current specifications across the family. Both 'AC and 'ACT device types have the same output structures. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system applications which can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times.

All devices ('AC or 'ACT) are guaranteed to source and sink 24 mA. Commercial devices, 74AC/ACTXXX, are capable of driving 50 ohm transmission lines.

I_{OL}/I_{OH} Characteristics

FACT	=	24/−24 mA
ALS	=	24/−15 mA
LS	=	8/−0.4 mA @ 4.75 V V_{CC}
HC	=	4/−4 mA

Dynamic Output Drive

Traditionally, in order to predict what incident wave voltages would occur in a system, the designer was required to do an output analysis using a Bergeron diagram. Not only is this a long and time consuming operation, but the designer needed to depend upon the accuracy and reliability of the manufacturer-supplied 'typical' output I/V curve. Additionally, there was no way to guarantee that any supplied device would meet these 'typical' performance values across the operating voltage and temperature limits. Fortunately for the system designers, Motorola has taken the necessary steps to guarantee incident wave switching on transmission lines with impedances as low as 50 ohms for the commercial temperature range.

Figure 2-2 shows a Bergeron diagram for switching both HIGH-to-LOW and LOW-to-HIGH. On the right side of the graph ($I_{out} > 0$), are the V_{OH} and I_{IH} curves for FACT logic while on the left side ($I_{out} < 0$), are the curves for V_{OL} and I_{IL}. Although we will only discuss here the LOW-to-HIGH transition, the information presented may be applied to a HIGH-to-LOW transition.

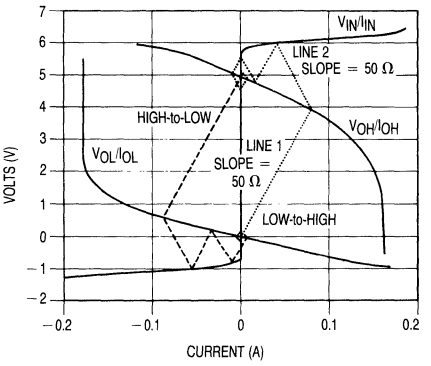


Figure 2-2. Gate Driving 50 Ohm Line Reflection Diagram

Begin analysis at the V_{OL} (quiescent) point. This is the intersection of the V_{OL}/I_{OL} curve for the output and the V_{IN}/I_{IN} curve for the input. For CMOS inputs and outputs, this point will be approximately 100 mV. Then draw a 50 ohm load line from this intersection to the V_{OH}/I_{OH} curve as shown by Line 1. This intersection is the voltage that the incident wave will have. Here it occurs at approximately 3.95 V. Then draw a line with a slope of −50 ohms from this first intersection point to the V_{IN}/I_{IN} curve as shown by Line 2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load lines from each intersection to the next. Lines terminating on the V_{OH}/I_{OH} curve should have positive slopes while lines terminating on the V_{IN}/I_{IN} curve should have negative slopes.

Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the V_{OH}/I_{OH} curve will be waves travelling from the driver to the receiver while intersection points on the V_{IN}/I_{IN} curve will be waves travelling from the receiver to the driver.

Figures 2-3a, 2-3b, 2-3c and 2-3d show the resultant waveforms. Each division on the time scale represents the propagation delay of the transmission line.

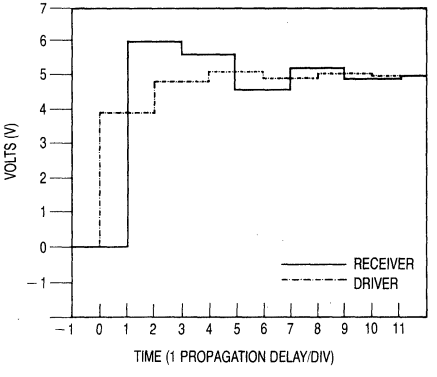


Figure 2-3a. Resultant Waveforms Driving 50 Ohm Line — Theoretical

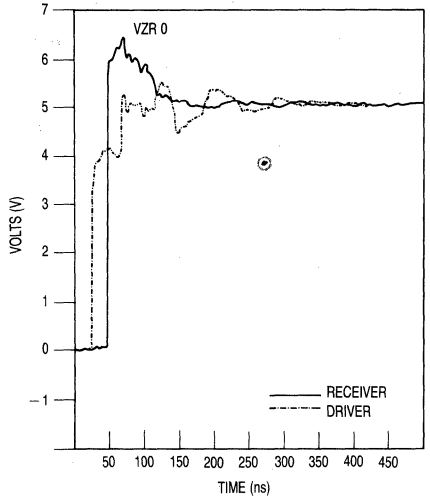


Figure 2-3b. Resultant Waveforms Driving 50 Ohm Line — Actual

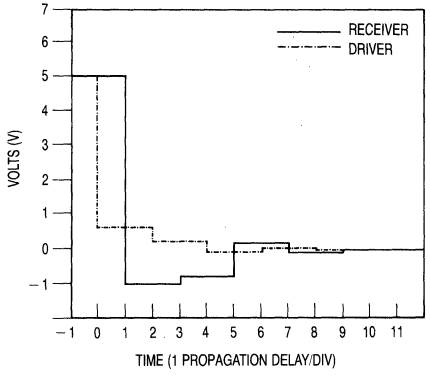


Figure 2-3c. Resultant Waveforms Driving 50 Ohm Line — Theoretical

While this exercise can be done for FACT, it is no longer necessary. FACT is guaranteed to drive an incident wave of enough voltage to switch another FACT input.

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either 70% or 30% of V_{CC}. The formula for calculating the current and voltage required is $|(V_{OQ} - V_I)/Z_o|$ at V_I. For V_{OQ} = 100 mV, V_{IH} = 3.85 V, V_{CC} = 5.5 V and Z_o = 50 ohms, the required I_{OH} at 3.85 V is 75 mA. For the HIGH-to-LOW transition, V_{OQ} = 5.4 V, V_{IL} = 1.35 V and Z_o = 50 ohms,

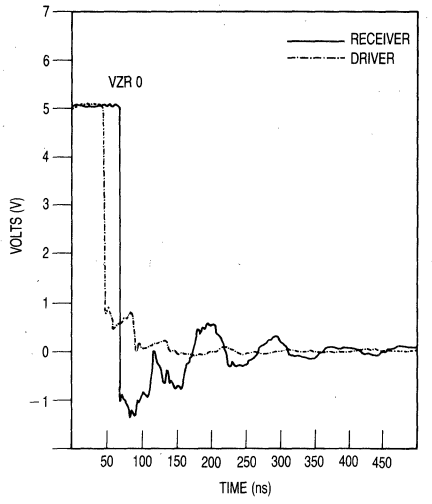


Figure 2-3d. Resultant Waveforms Driving 50 Ohm Line — Actual

I_{OL} is 75 mA at 1.65 V. FACT's I/O specifications include these limits. For transmission lines with impedances greater than 50 ohms, the current requirements are less and switching is still guaranteed.

It is important to note that the typical 24 mA drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid V_{IN} level.

The following performance charts are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltages.

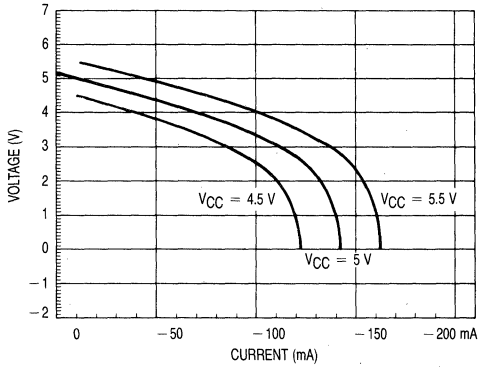


Figure 2-4. Output Characteristics V_{OH}/I_{OH}, 'AC00

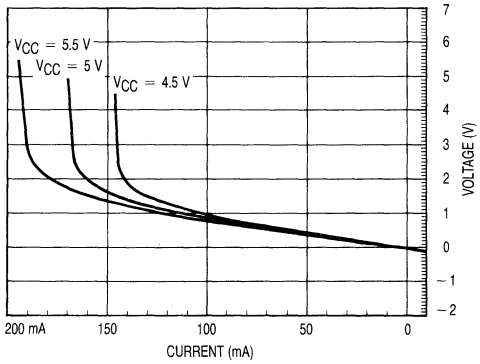


Figure 2-5. Output Characteristics V_{OL}/I_{OL}, 'AC00

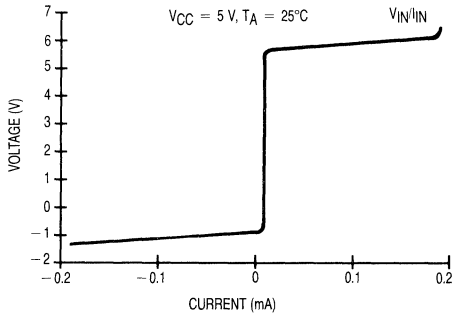


Figure 2-6. Input Characteristics V_{IN}/I_{IN}

Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low voltage operation in memory cards, it was decided by the JEDEC committee to establish interface standards for devices operating at 3.3 V ± 0.3 V. To this end, Motorola guarantees all of its devices operational at 3.3 V ± 0.3 V. Note also that AC and DC specifications are guaranteed between 3 and 5.5 V. Operation of FACT logic is also guaranteed from 2 to 6 V on V_{CC}.

Operating Voltage Ranges

FACT	=	2 to 6 V
ALS	=	5 V ± 10%
LS	=	5 V ± 5%
HC	=	2 to 6 V

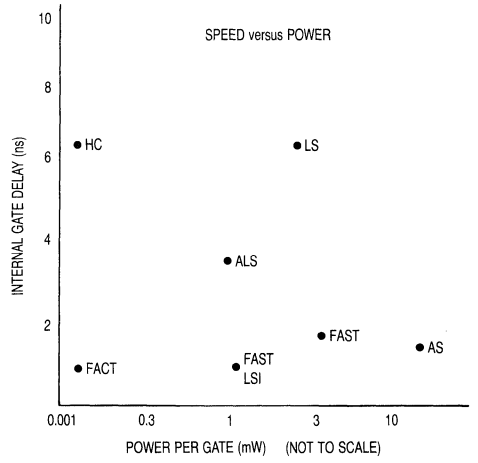


Figure 2-7. Internal Gate Delays

Figure 2-8. Logic Family Comparisons

GENERAL CHARACTERISTICS (All Max Ratings)

Symbol	Parameter	LS	ALS	HCMOS	FACT		Unit
					'AC	'ACT	
$V_{CC/EE/DD}$	Operating Voltage Range	5±5%	5±10%	2 to 6	2 to 6	2 to 6	V
T_A 74 Series	Operating Temperature Range	0 to +70	0 to +70	−40 to +85	−40 to +85	−40 to +85	°C
V_{IH} (min)	Input Voltage (limits)	2	2	3.15	3.15	2	V
V_{IL} (max)		0.8	0.8	0.9	1.35	0.8	V
V_{OH} (min)	Output Voltage (limits)	2.7	2.7	$V_{CC}-0.1$	$V_{CC}-0.1$	$V_{CC}-0.1$	V
V_{OL} (max)		0.5	0.5	0.1	0.1	0.1	V
I_{IH}	Input Current	20	20	+1	+1	+1	μA
I_{IL}		−400	−200	−1	−1	−1	μA
I_{OH}	Output Current at V_O (limit)	−0.4	−0.4	−4 @ $V_{CC}-0.8$	−24 @ $V_{CC}-0.8$	−24 @ $V_{CC}-0.8$	mA
I_{OL}		8	8	4 @ 0.4 V	24 @ 0.4 V	24 @ 0.4 V	mA
DCM	DC Noise Margin LOW/HIGH	0.3/0.7	0.4/0.7	0.8/1.25	1.25/1.25	0.7/2.4	V

Note: All DC parameters are specified over the commercial temperature range.

FACT Replaces LS, ALS, HCMOS

Motorola's Advanced CMOS family is specifically designed to outperform the LS, ALS and HCMOS families. Figure 2-7 shows the relative position of various logic families in speed/power performance. FACT exhibits 1 ns internal propagation delays while consuming 1 μW of power.

The Logic Family Comparisons table below summarizes the key performance specifications for various competitive technology logic families.

Figure 2-8. Logic Family Comparisons, cont'd.

SPEED/POWER CHARACTERISTICS (All Typical Ratings)

Symbol	Parameter	LS	ALS	HCMOS	FACT	Unit
I_G	Quiescent Supply Current/Gate	0.4	0.2	0.0005	0.0005	mA
P_G	Power/Gate (Quiescent)	2	1.2	0.0025	0.0025	mW
t_P	Propagation Delay	7	5	8	5	ns
—	Speed Power Product	14	6	0.02	0.01	pJ
f_{max}	Clock Frequency D/FF	33	50	50	160	MHz

PROPAGATION DELAY (Commercial Temperature Range)

	Product		LS	ALS	HCMOS	FACT	Unit
t_{PLH}/t_{PHL}	74XX00	Typ	10	5	8	5	ns
		Max	15	11	23	8.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX74	Typ	25	12	23	8	ns
		Max	40	18	44	10.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX163	Typ	18	10	20	5	ns
		Max	27	17	52	10	ns

Conditions: (LS) V_{CC} = 5 V, C_L = 15 pF, 25°C;
(ALS/HC/FACT) V_{CC} = 5 V, ± 10%, C_L = 50 pF, Typ values at 25°C, Max values at 0 to 70°C for ALS, −40 to +85°C for HC/FACT.

Circuit Characteristics

Power Dissipation

One advantage to using CMOS logic is its extremely low power consumption. During quiescent conditions, FACT will consume several orders of magnitude less current than its bipolar counterparts. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Power consumption of a circuit can be calculated using the formula:

$$P_D = [(C_L + C_{PD}) \cdot V_{CC} \cdot V_S \cdot f] + [I_Q \cdot V_{CC}]$$

where

P_D = power dissipation
C_L = load capacitance
C_{PD} = device power capacitance
V_{CC} = power supply
V_S = output voltage swing
f = frequency of operation
I_Q = quiescent current

Power consumption for FACT is dependent on the supply voltage, frequency of operation, internal capacitance and load. V_S will be V_{CC} and I_Q can be considered negligible for CMOS. Therefore, the simplified formula for CMOS is:

$$P_D = (C_L + C_{PD})\ V_{CC}^2\ f$$

C_{PD} values for CMOS devices are calculated by measuring the power consumption of a device at two different frequencies. C_{PD} is calculated in the following manner:

1. The power supply voltage is set to V_{CC} = 5 Vdc.
2. Signal inputs are set up so that as many outputs as possible are switching, giving a worst-case situation per JEDEC C_{PD} conditions (see Section 3).
3. The power supply current is measured and recorded at input frequencies of 200 kHz and 1 MHz.
4. The power dissipation capacitance is calculated by solving the two simultaneous equations

$$P_1 = (C_{PD} \cdot V_{CC}^2 \cdot f_1) + (I_{CC} \cdot V_{CC})$$
$$P_2 = (C_{PD} \cdot V_{CC}^2 \cdot f_2) + (I_{CC} \cdot V_{CC})$$

giving

$$C_{PD} = (P_1 - P_2)/V_{CC}^2(f_1 - f_2)$$

or

$$C_{PD} = (I_1 - I_2)/V_{CC}(f_1 - f_2)$$

where

I_1 = supply current at f_1 = 200 kHz.
I_2 = supply current at f_2 = 1 MHz.

On FACT device data sheets, C_{PD} is a typical value and is given either for the package or for the individual device (i.e., gates, flip-flops, etc.) within the package.

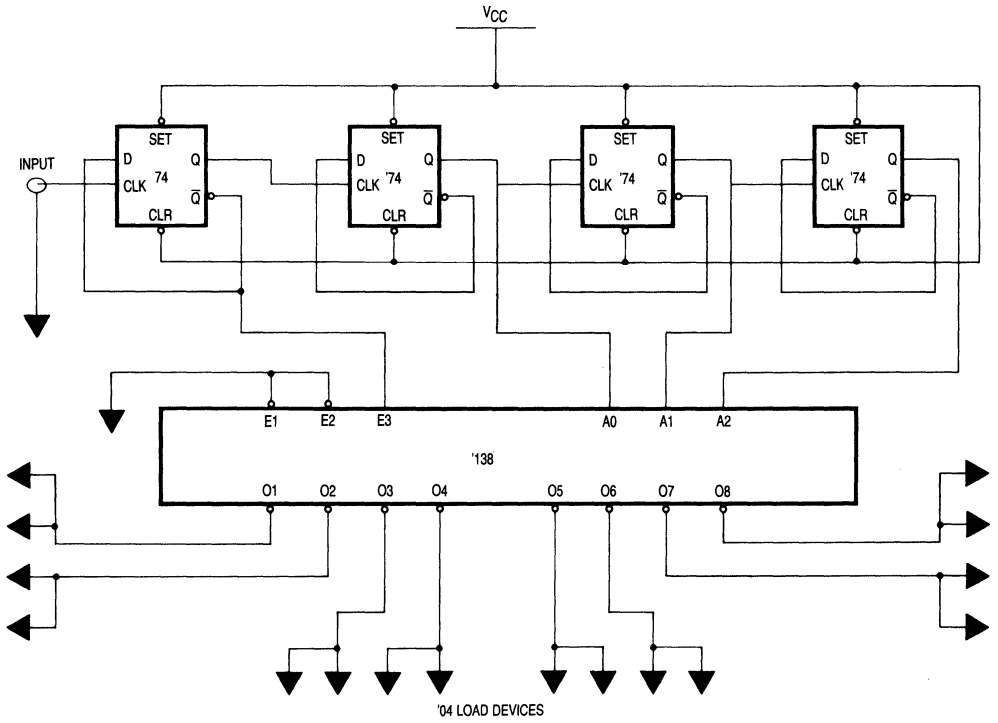


Figure 2-9. Power Demonstration Circuit Schematic

The circuit shown in Figure 2-9 was used to compare the power consumption of FACT versus ALS devices.

Two identical circuits were built on the same board and driven from the same input. In the circuit, the input signal was driven into four D-type flip-flops which act as divide-by-2 frequency dividers. The outputs from the flip-flops were connected to the inputs of a '138 decoder. This generated eight non-overlapping clock pulses on the outputs of the '138, which were then connected to an '04 inverter. The input frequency was then varied and the power consumption was measured. Figure 2-10 illustrates the results of these measurements.

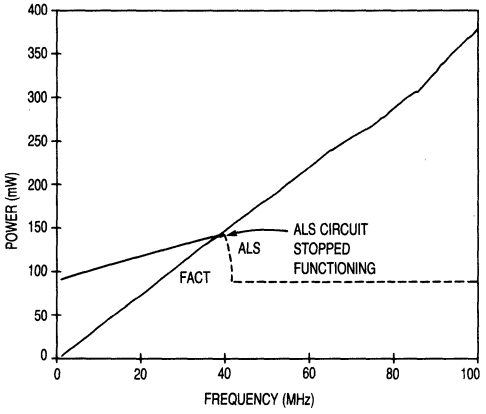


Figure 2-10. FACT versus ALS Circuit Power

Below 40 MHz, the FACT circuit dissipates much less power than the ALS version. It is interesting to note that when the frequency went to zero, the FACT circuit's power consumption also went to near zero; the ALS circuit continued to dissipate almost 100 mW. Another advantage of FACT is its capabilities above 40 MHz. At this frequency, the first 74ALS74 D-type flip-flop ceased to operate. Once this occurred, the entire circuit stopped working and the power consumption fell to its quiescent value. The FACT device, however, continued functioning beyond the limit of the frequency generator, which was 100 MHz.

This graph shows two advantages of FACT circuits (power and speed). FACT logic delivers increased performance in addition to offering the power savings of CMOS.

Refer to Section 3 for test philosophies regarding power dissipation.

Specification Derivation

At first glance, the specifications for FACT logic might appear to be widely spread, possibly indicating wide design margins are required. However, several effects are reflected in each specification.

Figures 2-11a through 2-11e illustrate how the data from

the characterization of actual devices is transformed into the specifications that appear on the data sheet. This data is taken from the 'AC245.

Figure 2-11a shows the data taken (from one part) on a typical, single path, t_{PHL} from An to Bn, over temperature at 5 V; there is negligible variation in the value of t_{PHL}. The next graph, Figure 2-11b, depicts data taken on the same device; this set of curves represents the data on all paths A to B and B to A. The data on this plot indicates only a small variation for t_{PHL}.

The graphs in Figures 2-11a and 2-11b include data at 5 V; Figure 2-11c shows the variation of delay times over the standard 5 ± 0.5 V voltage range. Note there is only a ± 6% variation in delay time due to voltage effects.

Now refer to Figure 2-11d which illustrates the process effects on delay time. This graph indicates that the process effects contribute to the spread in specifications more than any other factor in that the effects of the theoretical process spread can increase or decrease specification times by 30%. Because this 30% spread represents considerably more than ±3 standard deviations, this guarantees an increase in the manufacturability and the quality level of FACT product. To further ensure parts within specification will pass on testers at the limits of calibration, tester guardbands are incorporated.

With voltage and process effects added (Figure 2-11e), the full range of the specification can be seen. For reference, the data sheet values are shown on the graph.

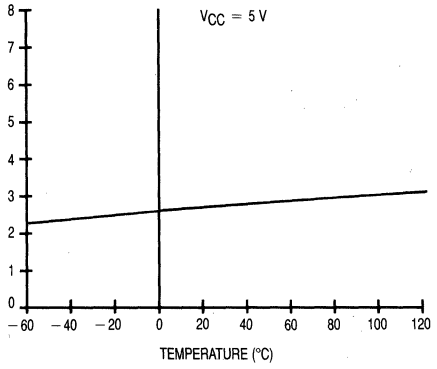


Figure 2-11a. t_{PHL}, An to Bn, Single Path

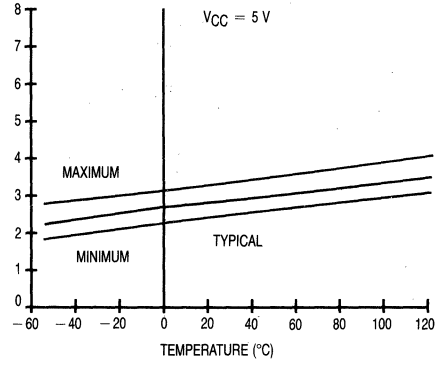


Figure 2-11b. t_{PHL}, A to B, All Paths

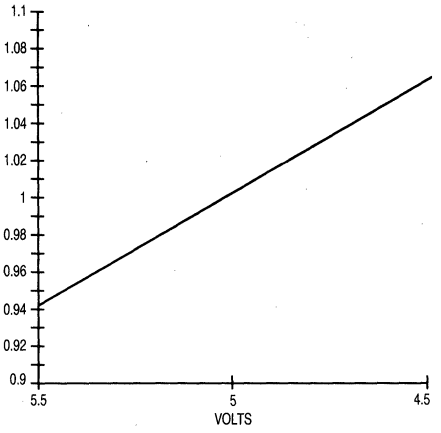


Figure 2-11c. Voltage Effects on Delay Times

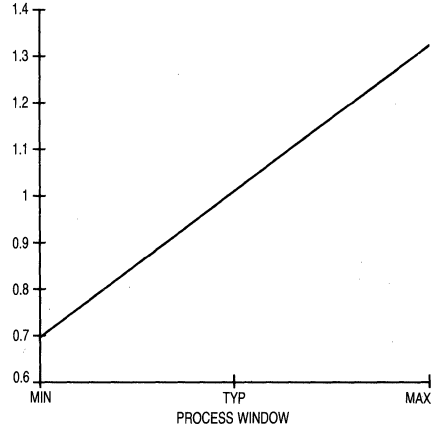


Figure 2-11d. FACT Process Effects on Delay Times

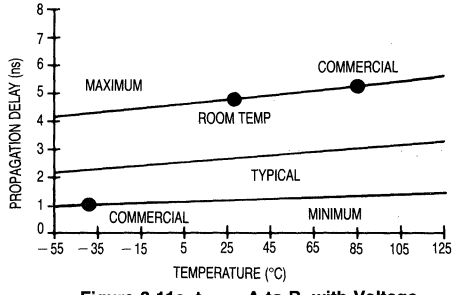


Figure 2-11e. t_{PHL}, A to B, with Voltage and Process Variation

This linear behavior with temperature and voltage is typical of CMOS. Although the graphs are drawn for a specific device, other part types have very similar graphical representations. Therefore, for performance-critical applications, where not all variables need to be taken into account at once, the user can narrow the specifications. For example, all parts in a critically timed subcircuit are together on a board, so it may be assumed the devices are at the same supply and temperature.

The same reasoning can be applied to setup and hold times. Consider the 'AC74. The setup time is 3 ns while the hold time is 0 ns. Theoretically, if these numbers were violated, the device would malfunction; however, in actuality, the device probably will not malfunction. Looking at the typical setup and hold times gives a better understanding of the device operation.

At 25°C and 5 V, the setup time is 1.5 ns while the hold time is −1.5 ns. They are the same; a positive setup time means the control signal to be valid before the clock edge, a positive hold time indicates the control signal will be held valid after the clock edge for the specified time, and a negative hold time means the control signal can transition before the clock edge. FACT devices were designed to be as immune to metastability as possible. This is reflected in the typical specifications. The true 'critical' time where the input is actually sampled is extremely short: less than 50 ps.

By applying the same reasoning as we did to the propagation delays to the setup and hold times, it becomes obvious that the spread from setup to hold time (3 ns worst-case) really covers devices across the entire process/temperature/voltage spread. The real difference between the setup and hold times for any single device, at a specified temperature and voltage, is negligible.

Capacitive Loading Effects

In addition to temperature and power supply effects, capacitive loading effects for loads greater than 50 pF should be taken into account for propagation delays of FACT devices. Minimum delay numbers may be determined from the table below. Propagation delays are measured to the 50% point of the output waveform.

Parameter	Voltage (V)			Units
	3	4.5	5.5	
t_{rise}	31	22	19	ps/pF
t_{fall}	18	13	12.5	ps/pF

T_A = 25°C

The two graphs following, Figures 2-12 and 2-13, describe propagation delays on FACT devices as affected by variations in power supply voltage (V_{CC}) and lumped load capacitance (C_L). Figures 2-14 and 2-15 show the effects of lumped load capacitance on rise and fall times for FACT devices.

Latch-up

A major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance. FACT logic is guaranteed not to latch-up with dynamic currents of 100 mA forced into or out of the inputs or the outputs under worst case conditions (T_A = 125°C and V_{CC} = 5.5 Vdc). At room temperature the parts can typically withstand dynamic currents of over 450 mA. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

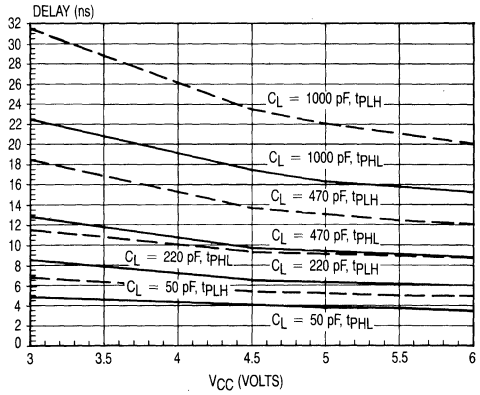


Figure 2-12. Propagation Delay versus V_{CC} ('AC00)

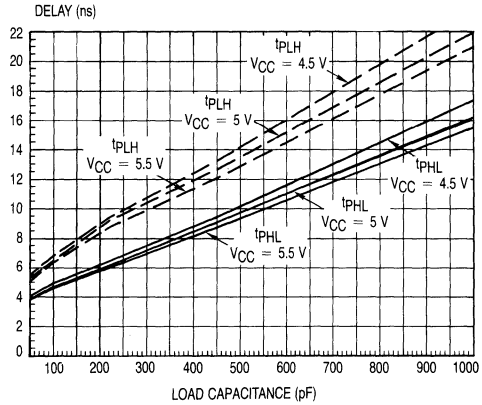


Figure 2-13. Propagation Delay versus C_L ('AC00)

FACT devices have been specifically designed to reduce the possibility of latch-up occurring; Motorola accomplished this by lowering the gain of the parasitic transistors, reducing substrate and p-well resistivity to increase external drive current required to cause a parasitic to turn ON, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

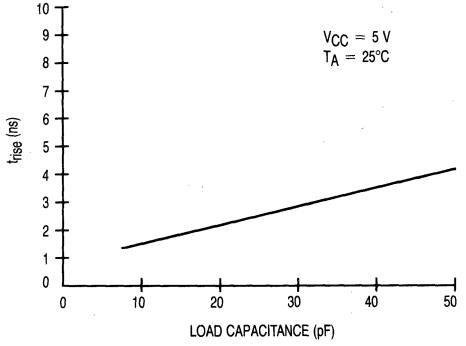


Figure 2.14. t_{rise} versus Capacitance

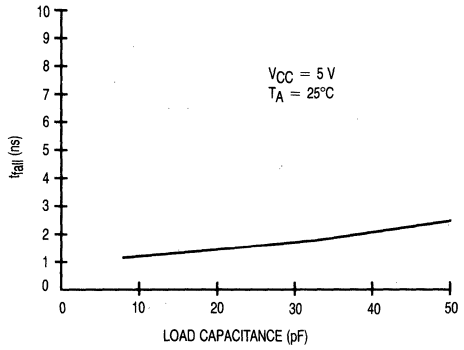


Figure 2-15. t_{fall} versus Capacitance

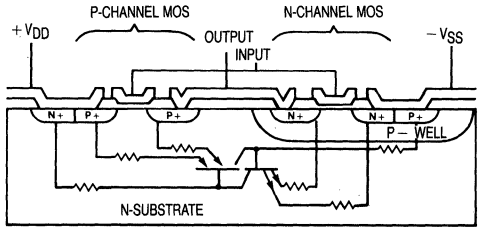


Figure 2-16. CMOS Inverter Cross Section with Latch-up Circuit Schematic

Electrostatic Discharge (ESD) Sensitivity

FACT circuits show excellent resistance to ESD-type damage. FACT logic is guaranteed to have 2000 V ESD immunity on all inputs and outputs using Human Body Model (1500 ohms, 100 pF). FACT parts do not require any special handling procedures. However, normal handling precautions should be observed as in the case of any semiconductor device.

Figure 2-17 shows the ESD test circuit used in the sensitivity analysis for this specification. Figure 2-18 is the pulse waveform required to perform the sensitivity test.

The test procedure is as follows: five pulses, each of 2000 V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. The voltage is increased and the testing procedure is again performed; this entire process is repeated until failure is detected. This is done to thoroughly evaluate all pins.

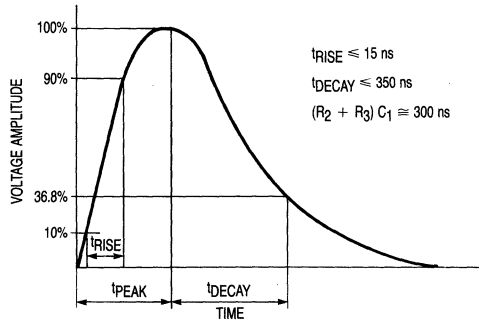


Figure 2-18. ESD Pulse Waveform

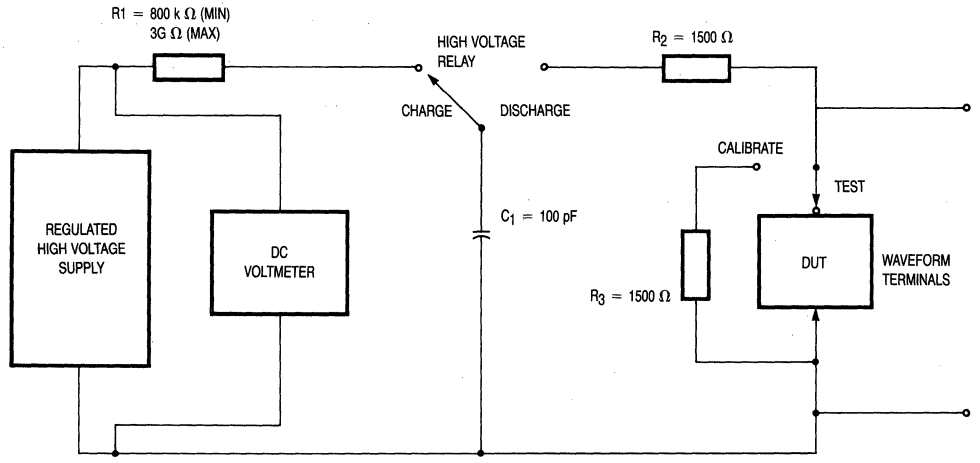
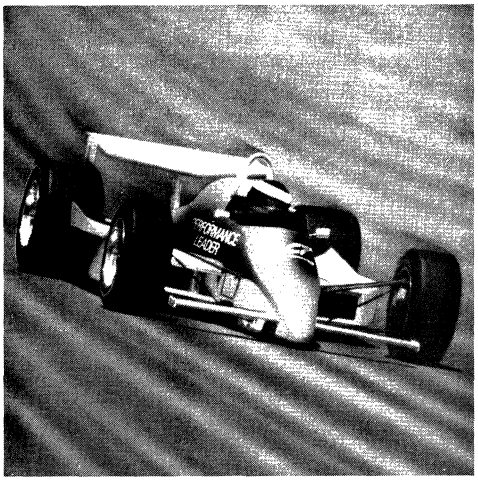


Figure 2-17. ESD Test Circuit



Ratings, Specifications and Waveforms

3

Ratings, Specifications and Waveforms

Specifying FACT Devices

Traditionally, when a semiconductor manufacturer completed a new device for introduction, specifications were based on the characterization of just a few parts. While these specifications were appealing to the designer, they were often too tight and, over time, the IC manufacturers had difficulty producing devices to the original specs. This forced the manufacturer to relax circuit specifications to reflect the actual performance of the device.

As a result, designers were required to review system designs to ensure the system would remain reliable with the new specifications. Motorola realized and understood the problems associated with characterizing devices too aggressively.

To provide more realistic and manufacturable specs, Motorola devised a systematic and thorough process to generate specifications. Devices are selected from multiple wafer lots to ensure process variations are taken into account. In addition, the process parameters are measured and compared to the known process limits.

This method of characterizing parts more accurately represents the product across time, voltage, temperature and process rather than portraying the fastest possible device. FACT circuits are therefore guaranteed to be manufacturable over time without the need to respecify timing.

These specification guidelines allow designers to design systems more efficiently since the devices used will behave as documented. Unspecified guardbands no longer need to be added by the designer to ensure system reliability.

Power Dissipation — Test Philosophy

In an effort to reduce confusion about measuring C_{PD}, a JEDEC standard test procedure (Appendix E) has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison. All device measurements are made with V_{CC} = 5 V at 25°C, with 3-state outputs both enabled and disabled.

Gates — Switch one input. Bias the remaining inputs such that the output switches.

Latches — Switch the Enable and D inputs such that the latch toggles.

Flip-Flops — Switch the clock pin while changing D (or bias J and K) such that the output(s) change each clock cycle. For parts with a common clock, exercise only one flip-flop.

Decoders — Switch one address pin which changes two outputs.

Multiplexers — Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.

Counters — Switch the clock pin with other inputs biased such that the device counts.

Shift Registers — Switch the clock pin with other inputs biased such that the device counts.

Transceivers — Switch one data input. For bidirectional devices enable only one direction.

Parity Generator — Switch one input.

Priority Encoders — Switch the lowest priority input.

Load Capacitance — Each output which is switching should be loaded with the standard 50 pF.

If the device is tested at a high enough frequency, the static supply current can be ignored. Thus at 1 MHz, the following formula can be used to calculate C_{PD}:

$C_{PD} = I_{CC}/(V_{CC})\,(1 \times 10^6)$ − Equivalent Load Capacitance

Ratings and Specifications

Figure 3-1. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Limits	Units
Supply Voltage	V_{CC}		−0.5 to 7	V
DC Input Diode Current or DC Input Voltage	I_{IK} V_I	$V_I = -0.5$ $V_I = V_{CC} + 0.5$	−20 20 −0.5 to V_{CC} + 0.5	mA mA V
DC Output Diode Current or DC Output Voltage	I_{OK} V_O	$V_O = -0.5$ $V_O = V_{CC} + 0.5$	−20 20 −0.5 to V_{CC} + 0.5	mA mA V
DC Output Source or Sink Current	I_O		±50	mA
DC V_{CC} or Ground Current Per Output Pin	I_{CC} or I_{GND}		±50	mA
Storage Temperature	T_{stg}		−65 to 150	°C

[1]Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. Motorola does not recommend operation of FACT circuits outside databook specifications.

Figure 3-2. Recommended Operating Conditions

Parameter		Symbol	Conditions	Limits	Units
Supply Voltage (unless otherwise specified)		V_{CC}		2.0 to 6.0	V
Input Voltage		V_I		0 to V_{CC}	V
Output Voltage		V_O		0 to V_{CC}	V
Operating Temperature	74AC/ACT	T_A		−40 to +85	°C
Junction Temperature	PDIP	T_J		140	°C
Input Rise and Fall Time[2] (typical) (except Schmitt inputs) V_{IN} from 30% to 70% of V_{CC}	'AC devices	t_r, t_f	V_{CC} @ 3 V V_{CC} @ 4.5 V V_{CC} @ 5.5 V	150 40 25	ns/V ns/V ns/V
Input Rise and Fall Time[2] (typical) (except Schmitt inputs) V_{IN} from 0.8 to 2 V, V_{meas} from 0.8 to 2 V	'ACT devices	t_r, t_f	V_{CC} @ 4.5 V V_{CC} @ 5.5 V	10 8	ns/V ns/V

[2]See individual data sheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	Conditions	V_{CC} (V)	74AC			Units
				T_A = 25°C		T_A = −40° to +85°C	
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} − 0.1 V	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} − 0.1 V	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V
V_{OH}	Minimum High Level Output Voltage	I_{OUT} = −50 μA	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V
		*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA I_{OH} −24 mA I_{OH} −24 mA	 3.0 4.5 5.5	 	 2.56 3.86 4.86	 2.46 3.76 4.76	 V
V_{OL}	Maximum Low Level Output Voltage	I_{OUT} = 50 μA	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V
		*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA I_{OL} 24 mA I_{OL} 24 mA	 3.0 4.5 5.5	 	 0.32 0.32 0.32	 0.37 0.37 0.37	 V
I_{IN}	Maximum Input Leakage Current	V_I = V_{CC}, GND	5.5		±0.1	±1.0	μA
I_{OZ}	Maximum 3-State Current	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND	5.5		±0.5	±5.0	μA
I_{OLD}	†Minimum Dynamic Output Current	V_{OLD} = 1.1 V	5.5			86	mA
I_{OHD}		V_{OHD} = 3.85 V	5.5			−75	mA

*All outputs loaded; threshold on input associated with output under test.
†Maximum test duration 20 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	Conditions	V_{CC} (V)	74AC		74ACT	Units
				T_A = 25°C		T_A = −40° to +85°C	
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} − 0.1 V	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1 V or V_{CC} − 0.1 V	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High Level	I_{OUT} = −50 μA	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V
		*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA	4.5 5.5	0.0001	3.86 4.86	3.76 4.76	V
V_{OL}	Maximum Low Level Output Voltage	I_{OUT} = 50 μA	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V
		*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA	4.5 5.5		0.32 0.32	0.37 0.37	V
I_{IN}	Maximum Input	V_I = V_{CC}, GND	5.5		±0.1	±1.0	μA
I_{OZ}	Maximum 3-State Current	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND	5.5		±0.5	±5.0	μA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} − 2.1 V	5.5	0.6		1.5	mA
I_{OLD}	†Minimum Dynamic Output Current	V_{OLD} = 1.1 V	5.5			86	mA
I_{OHD}		V_{OHD} = 3.85 V	5.5			−75	mA

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2 ms, one output loaded at a time.

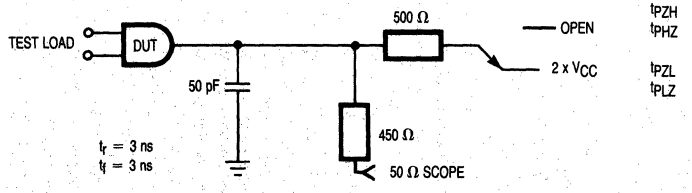


Figure 3-3. AC Tri-State Loading Circuit

AC Loading and Waveforms

Loading Circuit

Figure 3-3 shows the AC loading circuit used in characterizing and specifying propagation delays of all FACT devices ('AC and 'ACT) unless otherwise specified in the data sheet of a specific device.

The use of this load, differs somewhat from previous (HCMOS) practice, provides more meaningful information and minimizes problems of instrumentation and customer correlation. In the past, +25°C propagation delays for TTL devices were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance and implied the use of high impedance, high frequency scope probes. FAST circuits changed to 50 pF of capacitance allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions. This more closely resembles the inloading to be expected in average applications and thus gives the designer more useful delay figures. We have incorporated this scheme into the FACT product line. The net effect of the change in AC load is to increase the average observed propagation delay by about 1 ns.

The 500 ohm resistor to ground can be a high frequency passive probe for a sampling oscilloscope, which costs much less than the equivalent high impedance probe. Alternately, the 500 ohm resistor to ground can simply be a 450 ohm resistor feeding into a 50 ohm coaxial cable leading to a sampling scope input connector, with the internal 50 ohm termination of the scope completing the path to ground. This is the preferred scheme for correlation. (See Figure 3-3.) With this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50 ohm termination for the pulse generator that supplies the input signal.

Shown in Figure 3-3 is a second 500 ohm resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a 3-state output. With the switch closed, the pair of 500 ohm resistors and the 2 x V_{CC} supply voltage establish a quiescent HIGH level.

'ACxx Devices

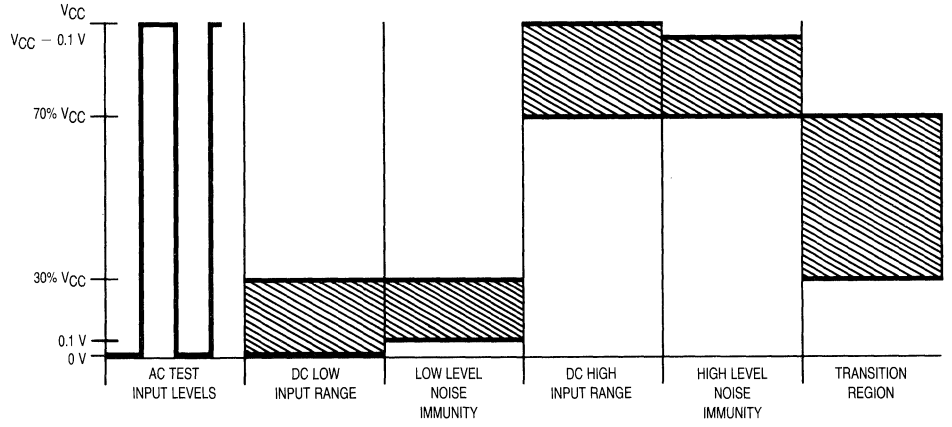


Figure 3-4a. Test Input Signal Levels

'ACTxx Devices

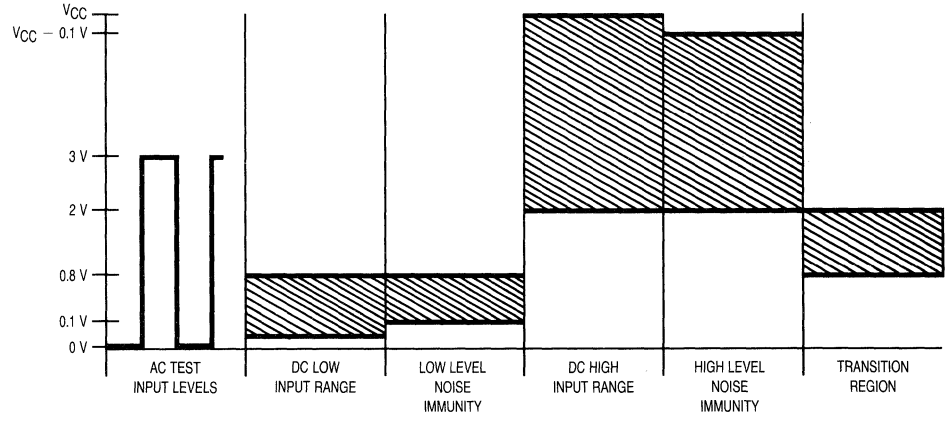


Figure 3-4b. Test Input Signal Levels

Test Conditions

Figures 3-4a and 3-4b describe the input signal voltage levels to be used when testing FACT circuits. The AC test conditions follow industry convention requiring V_{IN} to range from 0 V for a logic LOW to 3 V for a logic HIGH for 'ACT devices and 0 V to V_{CC} for 'AC devices. The DC parameters are normally tested with V_{IN} at guaranteed input levels, that is V_{IH} to V_{IL} (see data tables for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handler not specifically designed for high speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be seen in a system.

Noise immunity testing is performed by raising V_{IN} to the nominal supply voltage of 5 V then dropping to a level corresponding to V_{IH} characteristics, and then raising again to the 5 V level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0 V to V_{IL}, then returning to 0 V. Both V_{IH} and V_{IL} noise immunity tests should not induce a switch condition on the appropriate outputs of the FACT device.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

Rise and Fall Times

Input signals should have rise and fall times of 3 ns and signal swing of 0 V to 3.0 V V_{CC} for 'ACT devices or 0 V to V_{CC} for 'AC devices. Rise and fall times less than or equal to 1 ns should be used for testing f_{max} or pulse widths.

CMOS devices, including 4000 Series CMOS, HC, HCT and FACT families, tend to oscillate when the input rise and fall times become lengthy. As a direct result of its increased performance, FACT devices can be more sensitive to slow input rise and fall times than other lower performance technologies.

It is important to understand why this oscillation occurs. Consider the outputs, where the problem is initiated. Usually, CMOS outputs drive capacitive loads with low DC leakage. When the output changes from a HIGH level to a LOW level, or from a LOW level to a HIGH level, this capacitance has to be charged or discharged. With the present high performance technologies, this charging or discharging takes place in a very short time, typically 2–3 ns. The requirement to charge or discharge the capacitive loads quickly creates a condition where the instantaneous current change through the output structure is quite high. A voltage is generated across the V_{CC} or ground leads inside the package due to the inductance of these leads. The internal ground of the chip will change in reference to the outside world because of this induced voltage.

Consider the input. If the internal ground changes, the input voltage level appears to change to the DUT. If the input rise time is slow enough, its level might still be in the device threshold region, or very close to it, when the output switches. If the internally-induced voltage is large enough, it is possible to shift the threshold region enough so that it re-crosses the input level. If the gain of the device is sufficient and the input rise or fall time is slow enough, then the device may go into oscillation. As device propagation delays become shorter, the inputs will have less time to rise or fall through the threshold region. As device gains increase, the outputs will swing more, creating more induced voltage. Instantaneous current change will be greater as outputs become quicker, generating more induced voltage.

Package-related causes of output oscillation are not entirely to blame for problems with input rise and fall time measurements. All testers have V_{CC} and ground leads with a finite inductance. This inductance needs to be added to the inductance in the package to determine the overall voltage which will be induced when the outputs change. As the reference for the input signals moves further away from the pin under test, the test will be more susceptible to problems caused by the inductance of the leads and stray noise. Any noise on the input signal will also cause problems. With FACT logic having gains as high as 100, it merely takes a 50 mV change in the input to generate a full 5 V swing on the output.

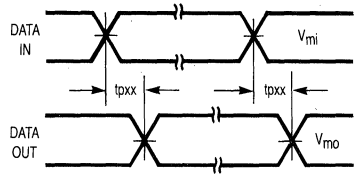


Figure 3-5. Waveform for Inverting and Non-Inverting Functions

*V_{mi} = 50% V_{CC} for 'AC devices; 1.5 V for 'ACT devices
V_{mo} = 50% for 'AC/'ACT devices

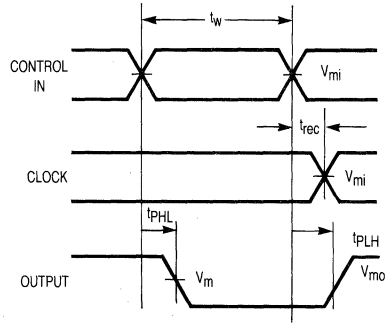


Figure 3-6. Propagation Delay, Pulse Width and t_{rec} Waveforms

Propagation Delay, f_{max}, Set and Hold Times

A 1 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. A 50% duty cycle should always be used when testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc.

Enable and Disable Times

Figures 3-7 and 3-8 show that the disable times are measured at the point where the output voltage has risen or fallen by 10% from the voltage rail level (i.e., ground for t_{PLZ} or V_{CC} for t_{PHZ}). This change enhances the repeatability of measurements, reduces test times, and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the high impedance state rising or falling waveform is RC-controlled, the first 10% of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 10% is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent Disable time and thus penalizes system performance since the designer must use the Enable and Disable times to devise worst case timing signals to ensure that the output of one device is disabled before that of another device is enabled.

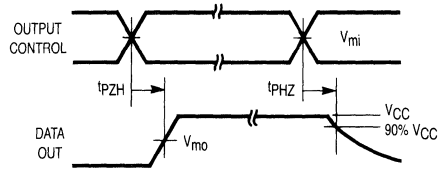


Figure 3-7. 3-State Output High Enable and Disable Times

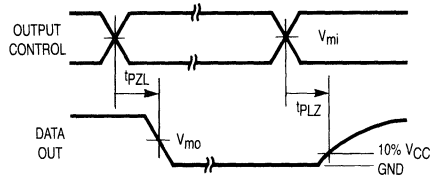


Figure 3-8. 3-State Output Low Enable and Disable Times

3

Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to FACT devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all plastic parts of the tester, which are near the device, are conductive and connected to ground.

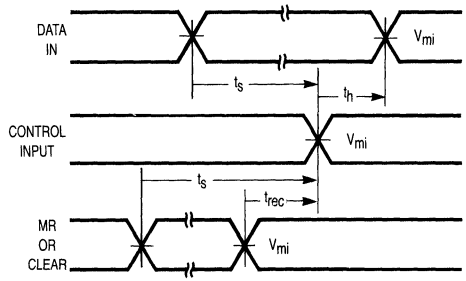


Figure 3-9. Setup Time, Hold Time and Recovery Time

*V_{mi} = 50% V_{CC} for 'AC devices; 1.5 V for 'ACT devices
V_{mo} = 50% V_{CC} for 'AC/'ACT devices

Design Considerations 4

Design Considerations

Today's system designer is faced with the problem of keeping ahead when addressing system performance and reliability. Motorola's Advanced CMOS helps designers achieve these goals.

FACT logic was designed to alleviate many of the drawbacks that are common to current technology logic circuits. FACT logic combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading and a 50 ohm transmission line drive capability (comparable to Motorola's FAST bipolar technology family) to offer a complete family of sub 2-micron SSI and MSI devices.

Performance features such as advanced Schottky speeds at CMOS power levels, advanced Schottky drive, excellent noise, ESD and latch-up immunity are characteristics that designers of state-of-the-art systems require. FACT logic answers all of these concerns in one family of products. To fully utilize the advantages provided by FACT, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of FACT.

4

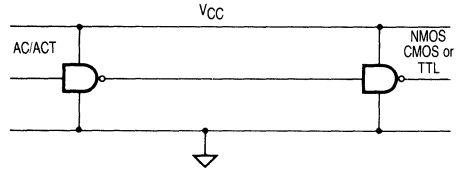
There are five items of interest which need to be evaluated when implementing FACT devices in new designs:

- Interfacing — interboard and technology interfaces, battery backup and power down or live insert/extract systems require some special thought.
- Transmission Line Driving — FACT has line driving capabilities superior to all CMOS families and most TTL families.
- Noise effects — As edge rates increase, the probability of crosstalk and ground bounce problems increases. The enhanced noise immunity and high threshold levels improve FACT's resistance to crosstalk problems.
- Board Layout — Prudent board layout will ensure that most noise effects are minimized.
- Power Supplies and Decoupling — Maximize ground and Vcc traces to keep Vcc/ground impedance as low as possible; full ground/Vcc planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package.

Interfacing

FACT devices have outputs which combine balanced CMOS outputs with high current line driving capability. Each standard output is guaranteed to source or sink 24 mA of current at worst case conditions. This allows FACT circuits to drive more loads than standard advanced Schottky parts; FACT can directly drive ALS, AS, LS, HC and HCT devices.

Figure 4-1. Interfacing FACT to NMOS, CMOS and TTL

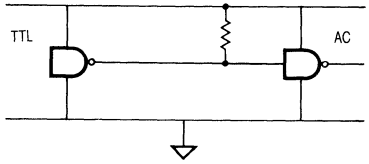


FACT devices can be directly driven by both NMOS and CMOS families, as shown in Figure 4-1, operating at the same rail potential without special considerations. This is possible due to the low input loading of FACT product, guaranteed to be less than 1 μA per input.

Some older technologies, including all existing TTL families, will not be able to drive FACT circuits directly; this is due to inadequate high level capability, which is guaranteed to 2.4 V. There are two simple approaches to the TTL-to-FACT interface problem. A TTL-to-CMOS converter can be

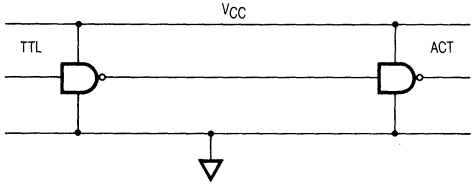
constructed employing a resistor pull-up to Vcc of approximately 4.7k ohms, which is depicted in Figure 4-2. The correct HIGH level is seen by the CMOS device while not loading down the TTL driver.

Figure 4-2. V_{IH} Pull-Up on TTL Outputs



Unfortunately, there will be designs where including a pull-up resistor will not be acceptable. In these cases, such as a terminated TTL bus, Motorola has designed devices which offer thresholds that are TTL-compatible (Figure 4-3). These interfaces tend to be slightly slower than their CMOS-level counterparts due to an extra buffer stage required for level conversion.

Figure 4-3. TTL Interfacing to 'ACT



ECL devices cannot directly drive FACT devices. Interfacing FACT-to-ECL can be accomplished by using TTL-to-ECL translators and 10125 ECL-to-TTL translators in addition to following the same rules on the TTL outputs to CMOS inputs (i.e., a resistor pull-up to Vcc of approximately 4.7k ohms). The translation can also be accomplished by a resistive network. A three-resistor interface between FACT and ECL logic is illustrated in Figure 4-4a. Figures 4-4b and 4-4c show the translation from ECL-to-FACT, which is somewhat more complicated. These two examples offer some possible interfaces between ECL and FACT logic.

Figure 4-4a. Resistive FACT-to-ECL Translation

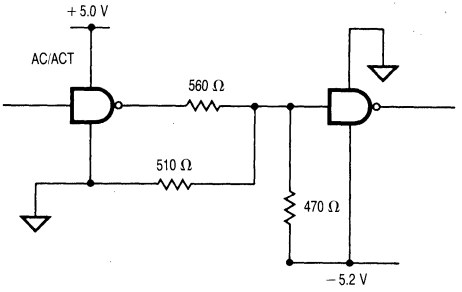


Figure 4-4b. Single-Ended ECL-to-'AC Circuit

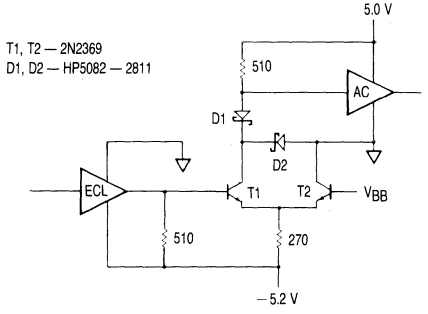
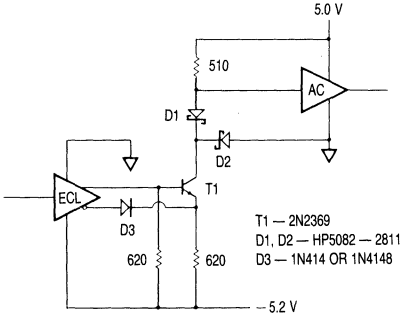


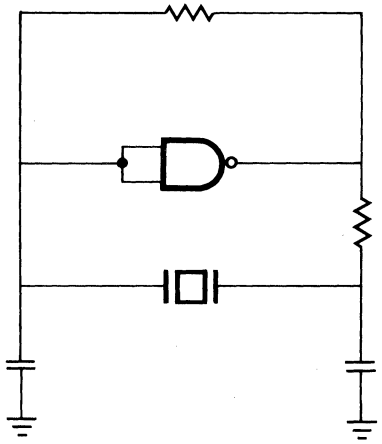
Figure 4-4c. Differential Output ECL-to-'AC Circuit



4

It should be understood that for FACT, as with other CMOS technologies, input levels that are between specified input values will cause both transistors in the CMOS structure to be conducting. This will cause a low resistive path from the supply rail to ground, increasing the power consumption by several orders of magnitude. It is important that CMOS inputs are always driven as close as possible to the rail.

Figure 4-5. Crystal Oscillator Circuit Implemented with FACT 'AC00



4

Line Driving

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer: Z_{oe}, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_o and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z_{oe} and t_{pde} can be calculated with:

$$Z_{oe} = \frac{Z_o}{\sqrt{1+C_t/C_l}}$$

$$t_{pde} = t_{pd}\sqrt{1+C_t/C_l}$$

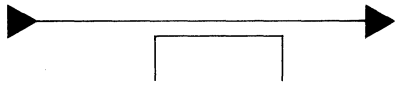
where C_l = intrinsic line capacitance and C_t = additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

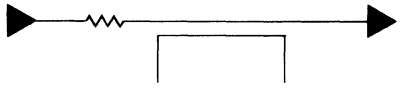
There are several termination schemes which may be used. Included are series, parallel, AC parallel and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

Termination Schemes

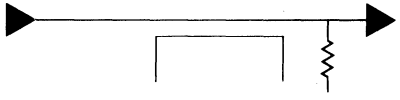
Figure 4-6. Termination Schemes



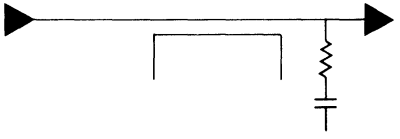
a: No Termination



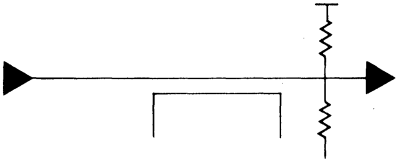
b: Series Termination



c: Parallel Termination



d: AC Parallel Termination



e: Thevenin Termination

Series Terminations
Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line. Loads that are between the driver and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor and the impedance of the line according to the formula

$$V_W = V_{CC} \bullet Z_{oe}/(Z_{oe} + R_S + Z_S)$$

The amplitude will be one-half the voltage swing if Rs (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

Parallel Termination
Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

AC Parallel Termination
AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

Thevenin Termination
Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be a function of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between V_{CC} or ground, increasing power consumption.

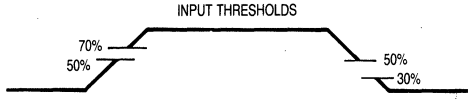
FACT circuits have been designed to drive 50 ohm transmission lines over the full commercial temperature range. This is guaranteed by the FACT family's specified dynamic drive capability of 86 mA sink and 75 mA source current. This ensures incident wave switching on

50 ohm transmission lines and is consistent with the 3 ns rated edge transition time.

FACT devices also feature balanced output totem pole structures to allow equal source and sink current capability. This gives rise to balanced edge rates and equal rise and fall times. Balanced drive capability and transition times eliminate both the need to calculate two different delay times for each signal path and the requirement to correct signal polarity for the shortest delay time.

FACT product inputs have been created to take full advantage of high output levels to deliver the maximum noise immunity to the system designer. V_{IH} and V_{IL} are specified at 70% and 30% of V_{CC} respectively. The corresponding output levels, V_{OH} and V_{OL}, are specified to be within 0.1 V of the rails, of which the output is sourcing or sinking 20 μA or less. These noise margins are outlined in Figure 4-7.

Figure 4-7. Input Threshold



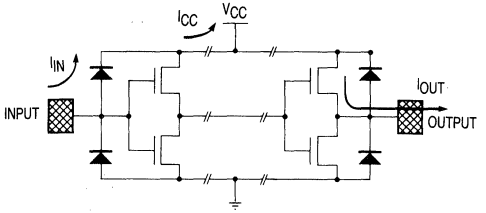
4

CMOS Bus Loading

CMOS logic devices have clamp diodes from all inputs and outputs to V_{CC} and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 4-8 exemplifies the situation when power is removed. Any input driven above the V_{CC} pin will forward-bias the clamp diode. Current can then flow into the device, and out V_{CC} or any output that is HIGH. Depending upon the system, this current, I_{IN}, can be quite high, and may not allow the bus voltage to reach a valid HIGH state. One possible solution to eliminate this problem is to place a series resistor in the line.

Figure 4-8. Noise Effects



Noise Effects

FACT offers the best noise immunity of any competing technology available today. With input thresholds specified at 30% and 70% of V_{CC} and outputs that drive to within 100 mV of the rails, FACT devices offer noise margins approaching 30% of V_{CC}. At 5 V V_{CC}, FACT's specified input and output levels give almost 1.5 V of noise margin for both ground- and V_{CC}-born noise. With realistic input thresholds closer to 50% of V_{CC}, the actual margins approach 2.5 V.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the superior performance of FACT circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Crosstalk is the capacitive coupling of signals from one line to

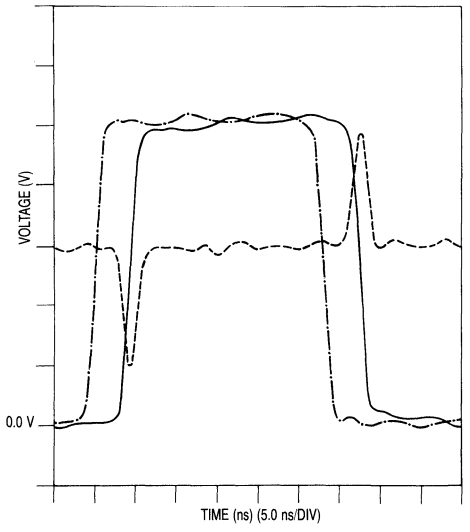
another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent.

Crosstalk has two basic causes. Forward crosstalk, Figure 4-9a, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air ($\epsilon_r = 1.0$) and epoxy glass ($\epsilon_r = 4.7$). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, Figure 4-9b, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. FACT's industry-leading noise margins make systems immune to crosstalk-related problems easier to design. FACT's AC noise margins, shown in Figures 4-10a and 4-10b, exemplify the outstanding immunity to everyday noise which can effect system reliability.

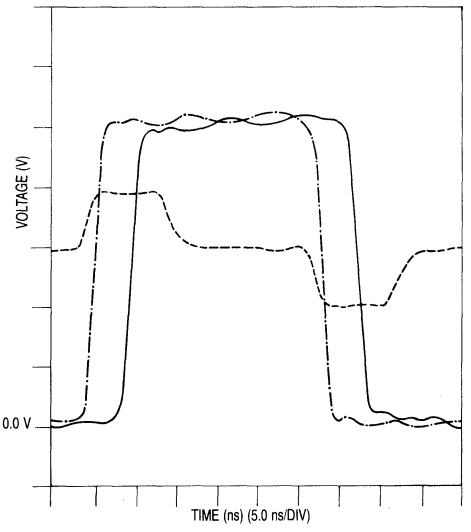
Figure 4-9a. Forward Crosstalk on PCB Traces



Key	Vertical Scale	Horizontal Scale
-·-·-· Active Driver	1.0 V/Div	50 ns/Div
– – – Forward Crosstalk	0.2 V/Div	5.0 ns/Div
—— Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

Figure 4-9b. Reverse Crosstalk on PCB Traces



Key	Vertical Scale	Horizontal Scale
-·-·-· Active Driver	1.0 V/Div	50 ns/Div
– – – Reverse Crosstalk	0.2 V/Div	5.0 ns/Div
—— Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

Figure 4-10a. High Noise Margin

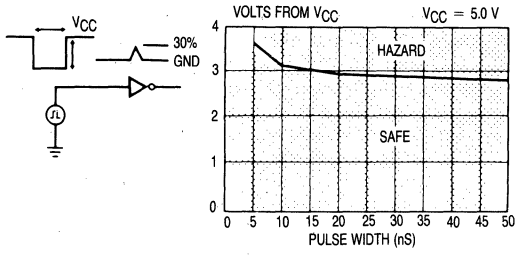
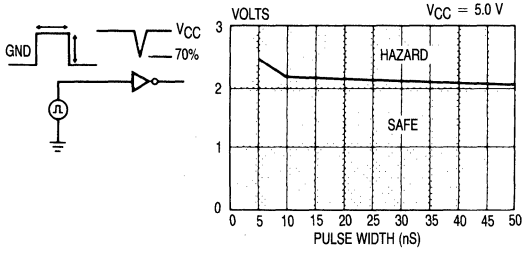


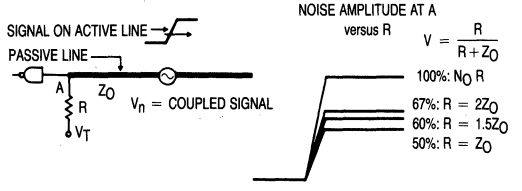
Figure 4-10b. Low Noise Margin



With over 2.0 V of noise margins, the FACT family offers better noise rejection than any other comparable technology.

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

Figure 4-11. Effects of Termination on Crosstalk



Ground Bounce

Ground bounce occurs as a result of the intrinsic characteristics of the leadframes and bondwires of the packages used to house CMOS devices. As edge rates and drive capability increase in advanced logic families, the effects of these intrinsic electrical characteristics become more pronounced.

Figure 4-12a shows a simple circuit model for a device in a leadframe driving a standard test load. The inductor L1 represents the parasitic inductance in the ground lead of the package; inductor L2 represents the parasitic inductance in the power lead of the package; inductor L3 represents the parasitic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the output of the device.

Figure 4-12a. Output Model

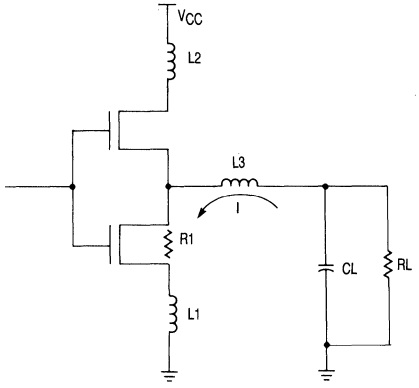


Figure 4-12b. Output Voltage

Figure 4-12c. Output Current

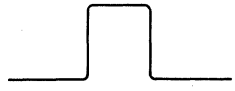
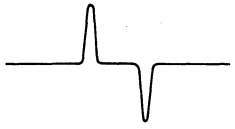


Figure 4-12d. Inductor Voltage



The three waveforms shown in Figures 4-12b, c and d, depict how ground bounce is generated. The first waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, the inductors L1 and L3, and C_L, the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = C_L \cdot dV/dt$]. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$V_{gb} = -L \cdot (dI/dt)$].

There are many factors which affect the amplitude of the ground bounce. Included are:

- Number of outputs switching simultaneously: more outputs results in more ground bounce.
- Type of output load: capacitive loads generate two to three times more ground bounce than typical system traces. Increasing the capacitive load to approximately 60-70 pF increases ground bounce. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load. Moving the load away from the output reduces the ground bounce.
- Location of the output pin: outputs closer to the ground pin exhibit less ground bounce than those further away.
- Voltage: lowering Vcc reduces ground bounce.
- Test fixtures: standard test fixtures generate 30 to 50% more ground bounce than a typical system since they use capacitive loads which both increase the AC load and form LCR tank circuits that oscillate.

Ground bounce produces several symptoms:

- Altered device states. FACT logic does not exhibit this symptom.
- Propagation delay degradation. FACT devices are characterized not to degrade more than 250 ps per additional output switching.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.
- Quiet output noise. FACT logic's worst-case quiet output noise has been measured to be approximately 500-1100 mV in actual system applications.

Observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce:

First, use caution when driving asynchronous TTL-level inputs from CMOS octal outputs, or

Second, use caution when running control lines (set, reset, load, clock, chip select) which are glitch-sensitive through the same devices that drive data or address lines.

When it is not possible to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

- Locate these outputs as close to the ground pin as possible.
- Use the lowest Vcc possible or separate the power supplies.
- Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

Design Rules

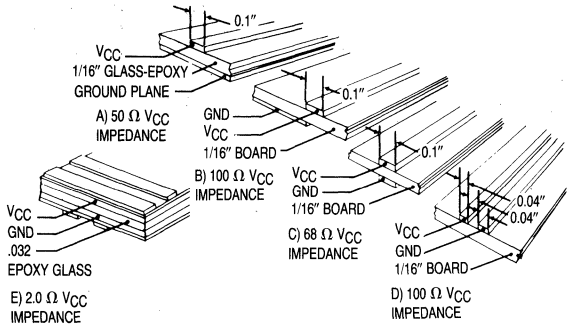
The set of design rules listed below are recommended to ensure reliable system operation by providing the optimum power supply connection to the devices. Most designers will recognize these guidelines as those they have employed with advanced bipolar logic families.

- Use multi-layer boards with Vcc and ground planes, with the device power pins soldered directly to the planes to insure the lowest power line impedances possible.
- Use decoupling capacitors for every device, usually 0.10 μF should be adequate. These capacitors should be located as close to the ground pin as possible.
- Do not use sockets or wirewrap boards whenever possible.
- Do not connect capacitors from the outputs directly to ground.

Decoupling Requirements

Motorola Advanced CMOS, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with FACT products.

Figure 4-13. Power Distribution Impedances

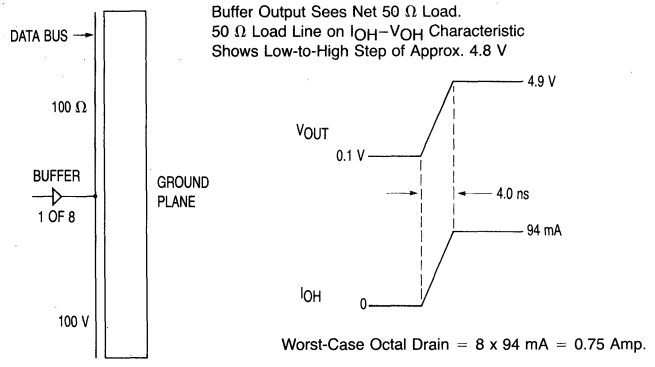


Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to a HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. Figure 4-13 displays various Vcc and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 50 and 100 ohms. This impedance appears in series with the load impedance and will cause a droop in the Vcc at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in Figure 4-14 to calculate the amount of decoupling necessary. This circuit utilizes an 'AC240 driving a 100 ohm bus from a point somewhere in the middle.

4

Figure 4-14. Octal Buffer Driving a 100 Ohm Bus



Being in the middle of the bus, the driver will see two 100 ohm loads in parallel, or an effective impedance of 50 ohms. To switch the line from rail to rail, a drive of 94 mA is needed; more than 750 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in Figure 4-15.

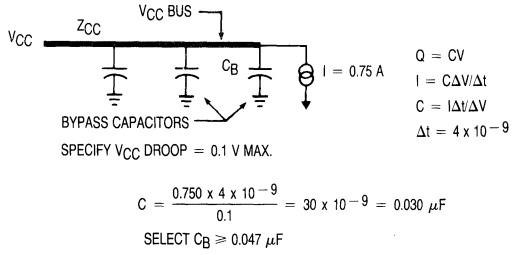
In this example, if the V_{CC} droop is to be kept below 0.1 V and the edge rate equals 4 ns, a 0.030 μf capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.

Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.

Figure 4-15. Formula for Calculating Decoupling Capacitors



Place one decoupling capacitor adjacent to each package driving any transmission line and distribute others evenly throughout the logic. One capacitor per three packages.

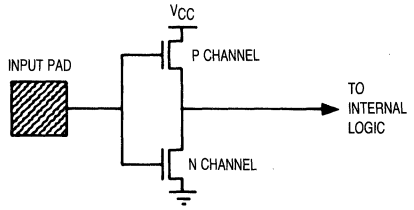
4

TTL-Compatible CMOS Designs Require Delta Icc Consideration

The FACT product line is comprised of two types of advanced CMOS circuits: 'AC and 'ACT devices. 'ACT indicates an advanced CMOS device with TTL-type input thresholds for direct replacement of LS and ALS circuits. As this 'ACT series is used to replace TTL, the Delta I_{CCT} specification must be considered; this spec may be confusing and misleading to the engineer unfamiliar with CMOS.

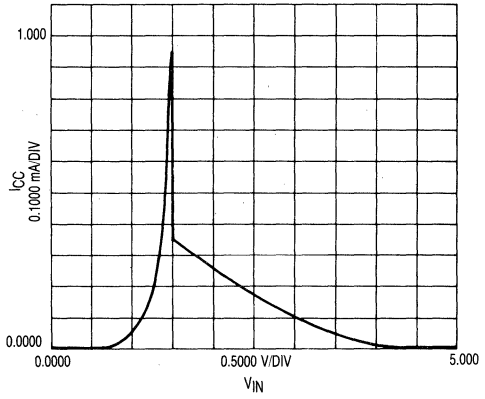
It is important to understand the concept of Delta I_{CCT} and how to use it within a design. First, consider where Delta I_{CCT} initiates. Most CMOS input structures are of the totem pole type with an n-channel transistor in a series with a p-channel transistor as illustrated below.

Figure 4-16. CMOS Input Structure



These two transistors can be modeled as variable resistors with resistances varying according to the input voltage. The resistance of an ON transistor is approximately 50 ohms while the resistance of an OFF transistor is generally greater than 5 Mohm. When the input to this structure is at either ground or Vcc, one transistor will be ON and one will be OFF. The total series resistance of this pair will be the combination of the two individual resistances, greater than 5 Mohm. The leakage current will then be less than 1 μA. When the input is between ground and Vcc, the resistance of the ON transistor will increase while the resistance of the OFF transistor will decrease. The net resistance will drop due to the much larger value of the OFF resistance. The total series resistance can be as low as 600 ohms. This reduction in series resistance of the input structure will cause a corresponding increase in Icc as current flows through the input structure. The following graph depicts typical Icc variance with input voltage for an 'ACT device.

Figure 4-17. I_{CC} versus Input Voltage for 'ACT Devices



The Delta Icc specification is the increase in Icc. For each input at Vcc-2.1 V, the Delta Icc value should be added to the quiescent supply current to arrive at the circuit's worst-case static Icc value.

Fortunately, there are several factors which tend to reduce the increase in Icc per input. Most TTL devices will be able to drive FACT inputs well beyond the TTL output specification due to FACT's low input loading in a typical system. FAST logic outputs can drive 'ACT-type inputs down to 200 mV and up to 3.5 V. Additionally, the typical Icc increase per input will be less than the specified limit. As shown in the graph above, the Icc increase at Vcc-2.1 V is less than 200 μA in the typical system. Experiments have shown that the Icc of an 'ACT240 series device typically increases only 200 μA when all of the inputs are connected to a FAST device instead of ground or Vcc.

It is important when designing with FACT, as with any TTL-compatible CMOS technology, that the Delta Icc specification be considered. Designers should be aware of the spec's significance and that the data book specification is a worst-case value; most systems will see values that are much less.

Testing Advanced CMOS Devices with I/O Pins

There are more and more CMOS families becoming available which can replace TTL circuits. Although testing these new CMOS units with programs and fixtures which were developed for bipolar devices will yield acceptable results most of the time, there are some cases where this approach will cause the test engineer problems.

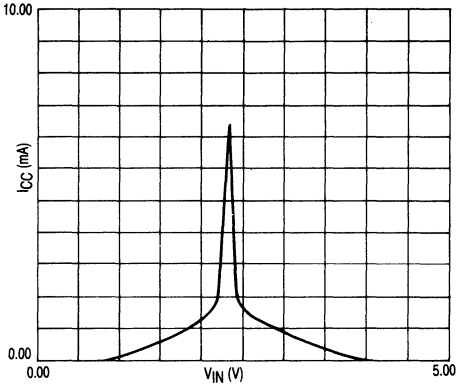
Such is the case with parts that have a bidirectional pin, exemplified by the '245 Octal Transceiver. If the proper testing methods are not followed, these types of parts may not pass those tests for Icc and input leakage currents, even when there is no fault with the devices.

CMOS circuits, unlike their bipolar counterparts, have static Icc specification orders of magnitude less than standard load currents. Most CMOS Icc specifications are usually less than 100 μA. When conducting an Icc test, greater care must be taken so that other currents will not mask the actual Icc of the device. These currents are usually sourced from the inputs and outputs.

Since the static Icc requirements of CMOS devices are so low, output load currents must be prevented from masking the current load of the device during an Icc test. Even a standard 500 ohm load resistor will sink 10 mA at 5 V, which is more than twice the Icc level being tested. Thus, most manufacturers will specify that all outputs must be unloaded during Icc tests.

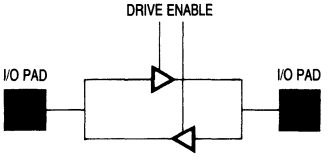
Another area of concern is identified when considering the inputs of the device. When the input is in the transition region, Icc can be several orders of magnitude greater than the specification. When the input voltage is in the transition region, both the n-channel and the p-channel transistors in the input totem-pole structure will be slightly ON, and a conduction is created from Vcc to ground. This conduction path leads to the increased Icc current seen in the Icc vs. V_{IN} curve. When the input is at either rail, the input structure no longer conducts. Most Icc testing is done with all of the inputs tied to either Vcc or ground. If the inputs are allowed to float, they will typically float to the middle of the transition region, and the input structure will conduct an order of magnitude more current than the actual Icc of the device under test which is being measured by the tester.

Figure 4-18. I_{CC} versus I_{IN}



When testing the Icc of a CMOS '245, problems can arise depending upon how the test is conducted. Note the structure of the '245's I/O pins illustrated below.

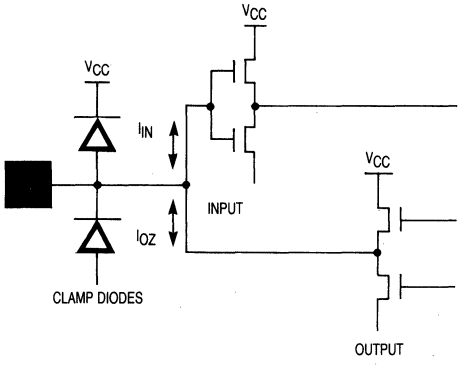
Figure 4-19. '245 I/O Structure



Each I/O pin is connected to both an input device and an output device. The pin can be viewed as having three states: input, output and output disabled. However, only two states actually exist.

The pin is either an input or an output. When testing the Icc of the device, the pins selected as outputs by the T/R signal must either be enabled and left open or be disabled and tied to either rail. If the output device is disabled and allowed to float, the input device will also float, and an excessive amount of current will flow from Vcc to ground. A simple rule to follow is to treat any output which is disabled as an input. This will help insure the integrity of an Icc test.

Figure 4-20. I/O Pin Internal Structure



Another area which might precipitate problems is the measurement of the leakages on I/O pins. The I/O pin internal structure is depicted below.

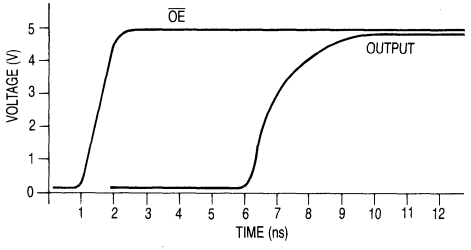
The pin is internally connected to both an input device and an output device; the limit for a leakage test must be the combined IIN specification of the input and the Ioz specification of the output. For FACT devices, IIN is specified at ± 1 μA while Ioz is specified at ± 5 μA. Combining these gives a limit of ±6 μA for I/O pins. Usually, I/O pins will show leakages that are less than the Ioz specification of the output alone.

Testing CMOS circuits is no more difficult than testing their bipolar counterparts. However, there are some areas of concern that will be new to many test engineers beginning to work with CMOS. Becoming familiar with and understanding these areas of concern prior to creating a test philosophy will avert many problems that might otherwise arise later.

Testing Disable Times of 3-State Outputs in a Transmission Line Environment

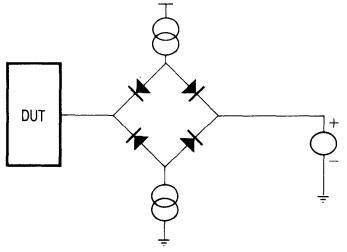
Traditionally, the disable time of a 3-state buffer has been measured from the 50% point on the disable input, to the 10% or 90% point on the output. On a bench test site, the output waveform is generated by a load capacitor and a pull-up/pull-down resistor. This circuit gives an RC charge/discharge curve as shown below.

Figure 4-21. Typical Bench 3-State Waveform



ATE test sites generally are unable to duplicate the bench test structure. ATE test loads differ because they are usually programmable and are situated away from the actual device. A commonly used test load is a Wheatstone bridge. The following figure illustrates the Wheatstone bridge test structure when used on the MCT 2000 test-system to duplicate the bench load.

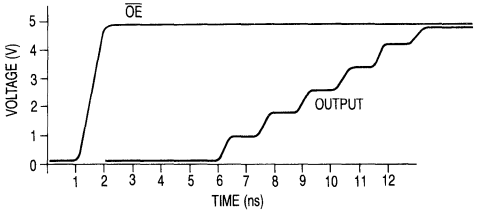
Figure 4-22. MCT Wheatstone Bridge Test Load



The voltage source provides a pull-up/pull-down voltage while the current sources provide I_{OH} and I_{OL}. When devices with slow output slew rates are tested with the ATE load, the resultant waveforms closely approximate the bench waveform, and a high degree of correlation can be achieved. However, when devices with high output slew rates are tested, different results are observed that make correlating tester results with bench results more difficult. This difference is due to the transmission line properties of the test equipment. Most disable tests are preceded by establishing a current flow through the output structure. Typically, these currents will be between 5 mA and 20 mA. The device is then disabled, and a comparator detects when the output has risen to the 10% or 90% level.

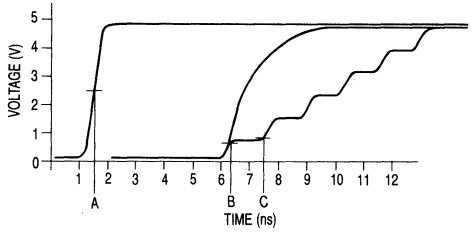
Consider the situation where the connection between the device under test (DUT) and the comparator is a transmission line. Visualize the device output as a switch; the effect is easier to see. There is current flowing through the line, and then the switch is opened. At the device end, the reflection coefficient changes from 0 to 1. This generates a current edge flowing back down the line equal to the current flowing in the line prior to the opening of the switch. This current wave will propagate down the line where it will encounter the high impedance tester load. This will cause the wave to be reflected back down the line toward the DUT. The current wave will continue to reflect in the transmission line until it reaches the voltage applied to the tester load. At this point, the current source impedance decreases and it will dissipate the current. A typical waveshape on a modern ATE is depicted in Figure 4-23.

Figure 4-23. Typical ATE 3-State Waveform



Transmission line theory states the voltage level of this current wave is equal to the current in the line times the impedance of the line. With typical currents as low as 5 mA and impedances of 50 to 60 ohms, this voltage step can be as minimal as 250 mV. If the comparator was programmed to the 10% point, it would be looking for a step of 550 mV at 5.5 V Vcc. Three reflections of the current pulse would be required before the comparator would detect the level. It is this added delay time caused by the transmission line environment of the ATE that may cause parts to fail customers' incoming tests, even though the device meets specifications. The figure below graphically shows this stepout.

Figure 4-24. Measurement Stepout



Point A represents the typical 50% measurement point on tester driven waveforms. Point B represents the point at which the delay time would be measured on a bench test fixture. Point C represents where the delay time could be measured on ATE fixtures. The delay time measured on the ATE fixture can vary from the bench measured delay time to some greater value, depending upon the voltage level that the tester is set. If the voltage level of the tester is close to voltage levels of the plateaus, the results may become non-repeatable.

Data Sheets 5

MOTOROLA

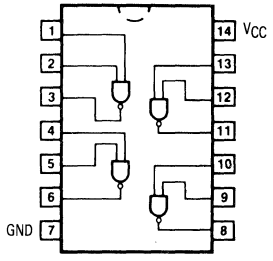
MC74AC00
MC74ACT00

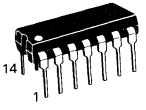
Product Preview

Quad 2-Input NAND Gate

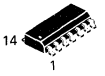
QUAD 2-INPUT
NAND GATE

- Outputs Source/Sink 24 mA
- 'ACT00 Has TTL Compatible Inputs





N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT00)	1.5	mA	V_{IN} = V_{CC} − 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3 5.0	1.0 1.0	7.0 6.0	9.5 8.0	1.0 1.0	10 8.5	ns	3-5
t_{PHL}	Propagation Delay	3.3 5.0	1.0 1.0	5.5 4.5	8.0 6.5	1.0 1.0	8.5 7.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0	1.0	5.5	9.0	1.0	9.5	ns	3-5
t_{PHL}	Propagation Delay	5.0	1.0	4.0	7.0	1.0	8.0	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	30	pF	V_{CC} = 5.0 V

5

MOTOROLA

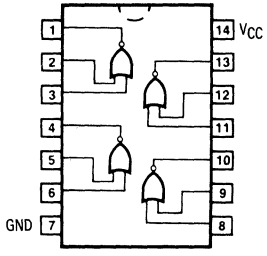
MC74AC02
MC74ACT02

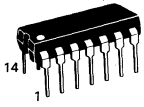
Product Preview

Quad 2-Input NOR Gate

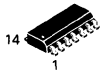
- Outputs Source/Sink 24 mA
- 'ACT02 Has TTL Compatible Inputs

QUAD 2-INPUT
NOR GATE





N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3 5.0	1.0 1.0	5.0 4.0	7.5 6.0	1.0 1.0	8.0 6.5	ns	3-5
t_{PHL}	Propagation Delay	3.3 5.0	1.0 1.0	5.0 4.5	7.5 6.5	1.0 1.0	8.0 7.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS — MC74ACT02
(Contact Local Motorola Sales Office)

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	30	pF	V_{CC} = 5.0 V

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

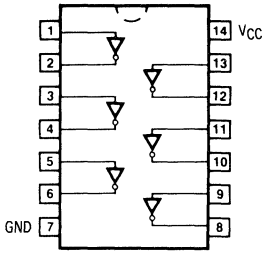
MC74AC04
MC74ACT04

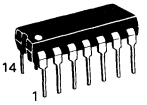
Product Preview

Hex Inverter

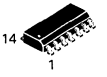
HEX INVERTER

- Outputs Source/Sink 24 mA
- 'ACT04 Has TTL Compatible Inputs





N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT04)	1.5	mA	V_{IN} = V_{CC} − 2.1 V, V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3 5.0	1.0 1.0	4.5 4.0	9.0 7.0	1.0 1.0	10 7.5	ns	3-5
t_{PHL}	Propagation Delay	3.3 5.0	1.0 1.0	4.5 3.5	8.5 6.5	1.0 1.0	9.5 7.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0		4.5				ns	3-6
t_{PHL}	Propagation Delay	5.0		3.9				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	30	pF	V_{CC} = 5.0 V

5

MOTOROLA

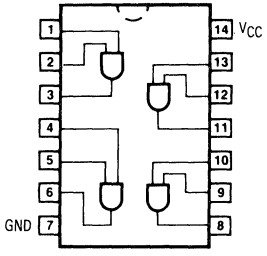
MC74AC08
MC74ACT08

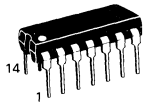
Product Preview

Quad 2-Input AND Gate

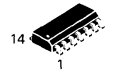
- Outputs Source/Sink 24 mA
- 'ACT08 Has TTL Compatible Inputs

QUAD 2-INPUT
AND GATE





N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT08)	1.5	mA	V_{IN} = V_{CC} − 2.1 V, V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.0	7.5	9.5	1.0	10	ns	3-5
		5.0	1.0	5.5	7.5	1.0	8.5		
t_{PHL}	Propagation Delay	3.3	1.0	7.0	8.5	1.0	9.0	ns	3-5
		5.0	1.0	5.5	7.0	1.0	7.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0		6.5				ns	3-5
t_{PHL}	Propagation Delay	5.0		6.7				ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	20	pF	V_{CC} = 5.0 V

5

MOTOROLA

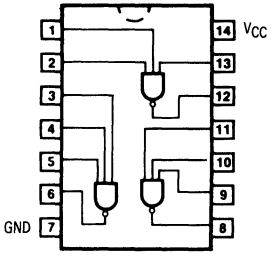
MC74AC10
MC74ACT10

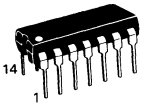
Product Preview

Triple 3-Input NAND Gate

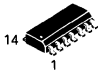
TRIPLE 3-INPUT NAND GATE

- Outputs Source/Sink 24 mA
- 'ACT10 Has TTL Compatible Inputs





N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3 5.0	1.0 1.0	6.0 4.5	9.5 7.0	1.0 1.0	10.5 8.0	ns	3-5
t_{PHL}	Propagation Delay	3.3 5.0	1.0 1.0	5.5 4.0	8.5 6.0	1.0 1.0	10 6.5	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS — MC74ACT10
(Contact Local Motorola Sales Office)

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	25	pF	V_{CC} = 5.0 V

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

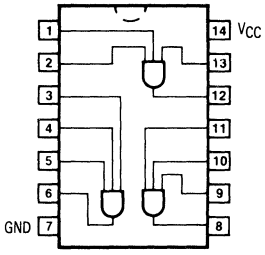
MC74AC11
MC74ACT11

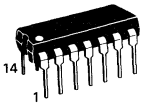
Product Preview

Triple 3-Input AND Gate

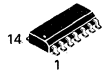
TRIPLE 3-INPUT AND GATE

- Outputs Source/Sink 24 mA
- 'ACT11 Has TTL Compatible Inputs





N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3 5.0	1.0 1.0	5.5 4.0	9.5 8.0	1.0 1.0	10 8.5	ns	3-5
t_{PHL}	Propagation Delay	3.3 5.0	1.0 1.0	5.5 4.0	8.5 7.0	1.0 1.0	9.5 7.5	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS — MC74ACT11
(Contact Local Motorola Sales Office)

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	20	pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC14
MC74ACT14

Product Preview

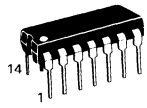
Hex Inverter Schmitt Trigger

HEX INVERTER SCHMITT TRIGGER

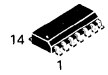
The MC74AC14/74ACT14 contains six logic inverters which accept standard CMOS input signals (TTL levels for MC74ACT14) and provide standard CMOS output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The MC74AC14/74ACT14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0 V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

- Outputs Source/Sink 24 mA
- 'ACT14 Has TTL Compatible Inputs



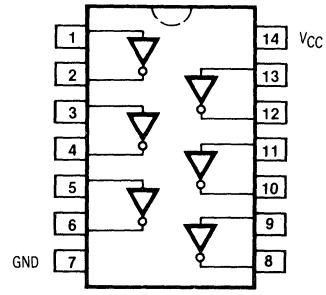
N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

FUNCTION TABLE

Input	Output
A	O
L	H
H	L



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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	74AC	74ACT	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current		40	40	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current		4.0	4.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT14)			1.5	mA	V_{IN} = V_{CC} − 2.1 V, V_{CC} = 5.5 V, T_A = Worst Case
V_{t+}	Maximum Positive Threshold	3.0 4.5 5.5	2.2 3.2 3.9	2.0	V	T_A = Worst Case
V_{t-}	Minimum Negative Threshold	3.0 4.5 5.5	0.5 0.9 1.1	0.8	V	T_A = Worst Case
$V_{h(max)}$	Maximum Hysteresis	3.0 4.5 5.5	1.2 1.4 1.6	1.2	V	T_A = Worst Case
$V_{h(min)}$	Minimum Hysteresis	3.0 4.5 5.5	0.3 0.4 0.5	0.4	V	T_A = Worst Case

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3 5.0	1.0 1.0	9.5 7.0	13.5 10	1.0 1.0	15 11	ns	3-5
t_{PHL}	Propagation Delay	3.3 5.0	1.0 1.0	7.5 6.0	11.5 8.5	1.0 1.0	13 9.5	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0		7.4				ns	3-5
t_{PHL}	Propagation Delay	5.0		8.6				ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	25	pF	V_{CC} = 5.0 V

MOTOROLA

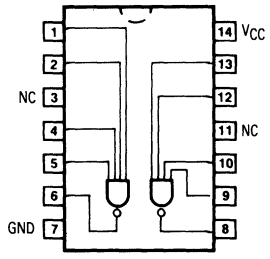
MC74AC20
MC74ACT20

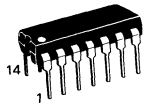
Product Preview

Dual 4-Input NAND Gate

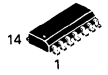
- Outputs Source/Sink 24 mA
- 'ACT20 Has TTL Compatible Inputs

DUAL 4-INPUT NAND GATE





N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3 5.0	1.0 1.0	6.0 5.0	8.5 7.0	1.0 1.0	10 8.0	ns	3-5
t_{PHL}	Propagation Delay	3.3 5.0	1.0 1.0	5.0 4.0	7.0 6.0	1.0 1.0	9.0 7.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS — MC74ACT20
(Contact Local Motorola Sales Office)

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

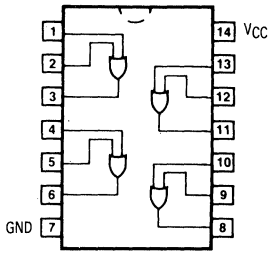
MC74AC32
MC74ACT32

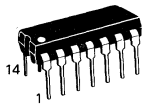
Product Preview

Quad 2-Input OR Gate

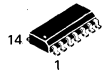
- Outputs Source/Sink 24 mA
- 'ACT32 Has TTL Compatible Inputs

QUAD 2-INPUT
OR GATE





N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT32)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.0	7.0	9.0	1.0	10	ns	3-5
		5.0	1.0	5.5	7.5	1.0	8.5		
t_{PHL}	Propagation Delay	3.3	1.0	7.0	8.5	1.0	9.0	ns	3-5
		5.0	1.0	5.0	7.0	1.0	7.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0		7.2				ns	3-5
t_{PHL}	Propagation Delay	5.0		6.6				ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	20	pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC74
MC74ACT74

Product Preview

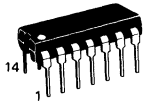
Dual D-Type Positive Edge-Triggered Flip-Flop

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

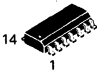
The MC74AC74/74ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:
- LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

- Outputs Source/Sink 24 mA
- 'ACT74 Has TTL Compatible Inputs

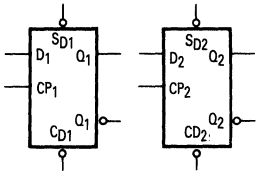


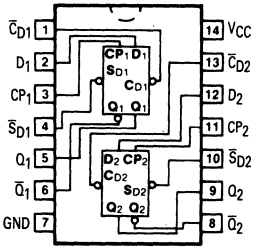
N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

TRUTH TABLE (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
$Q_0(\overline{Q}_0)$ = Previous Q($\overline{Q}$) before LOW-to-HIGH Transition of Clock

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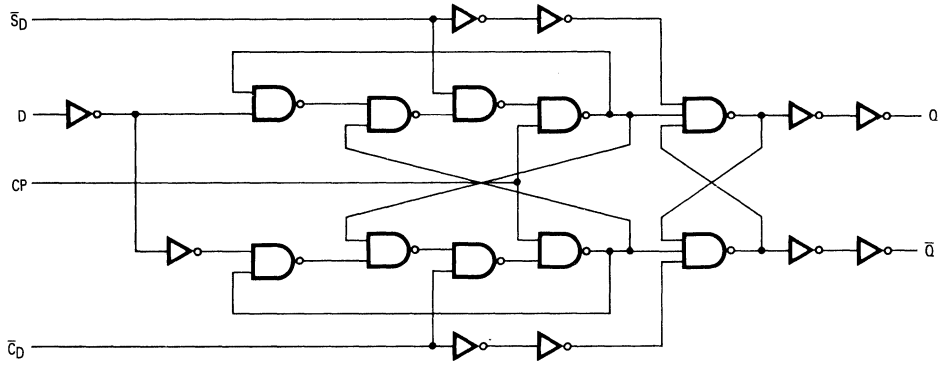
LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT74)	1.5	mA	V_{IN} = V_{CC} − 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	100 140	125 160		95 125		MHz	3-3
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	12 9.0	1.0 1.0	13 10	ns	3-6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	10.5 8.0	12 9.5	1.0 1.0	13.5 10.5	ns	3-6
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	13.5 10	1.0 1.0	16 10.5	ns	3-6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	14 10	1.0 1.0	14.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set-up Time, HIGH or LOW D_n to CP_n	3.3 5.0	1.5 1.0	4.0 3.0	4.5 3.0	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP_n	3.3 5.0	−2.0 −1.5	0 0	0 0	ns	3-9
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.3 5.0	3.0 2.5	5.5 4.5	7.0 5.0	ns	3-6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3 5.0	−2.5 −2.0	0 0	0 0	ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	210		125		MHz	3-3
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10	1.0	11.5	ns	3-6
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	7.5	11	1.0	13	ns	3-6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10	1.0	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set-up Time, HIGH or LOW D_n to CP_n	5.0	1.0	3.0	3.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP_n	5.0	−0.5	1.0	1.0	ns	3-9
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	5.0	3.0	5.0	6.0	ns	3-6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	−2.5	0	0	ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	35	pF	V_{CC} = 5.0 V

MOTOROLA

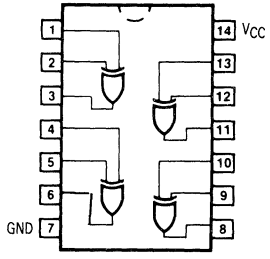
MC74AC86

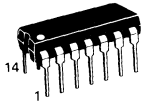
Product Preview

Quad 2-Input Exclusive-OR Gate

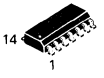
QUAD 2-INPUT EXCLUSIVE-OR GATE

- Outputs Source/Sink 24 mA





N SUFFIX
CASE 646-06
PLASTIC



D SUFFIX
CASE 751A-02
PLASTIC

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Inputs to Outputs	3.3 5.0		6.0 4.5				ns	3-5
t_{PHL}	Propagation Delay Inputs to Outputs	3.3 5.0		6.5 4.5				ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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MOTOROLA

MC74AC109
MC74ACT109

Product Preview

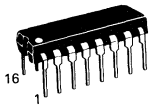
Dual $J\overline{K}$ Positive Edge-Triggered Flip-Flop

DUAL $J\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP

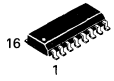
The MC74AC109/74ACT109 consists of two high-speed completely independent transition clocked $J\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The $J\overline{K}$ design allows operation as a D flip-flop (refer to MC74AC74/74ACT74 data sheet) by connecting the J and $\overline{K}$ inputs together.

Asynchronous Inputs:
- LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

- Outputs Source/Sink 24 mA
- 'ACT109 Has TTL Compatible Inputs

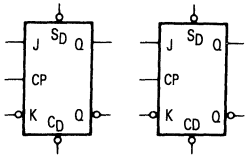


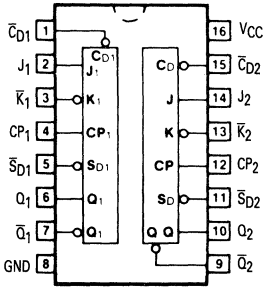
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

$J_1, J_2, \overline{K}_1, \overline{K}_2$	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}, \overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}, \overline{S}_{D2}$	Direct Set Inputs
$Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$	Outputs

TRUTH TABLE

Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐	L	L	L	H
H	H	⌐	H	L	Toggle	
H	H	⌐	L	H	Q_0	$\overline{Q}_0$
H	H	⌐	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
⌐ = LOW-to-HIGH Clock Transition
X = Immaterial
$Q_0(\overline{Q}_0)$ = Previous $Q_0(\overline{Q}_0)$ before LOW-to-HIGH Transition of Clock

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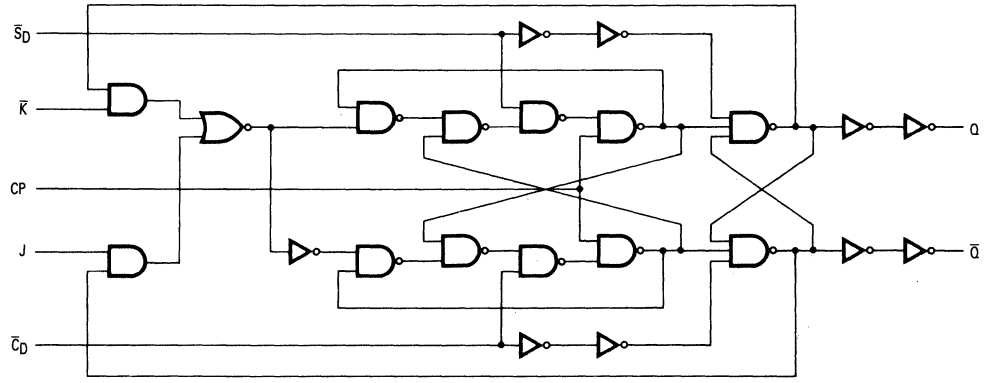
LOGIC DIAGRAM (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT109)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	125 150	150 175		100 125		MHz	3-3
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	13.5 10	1.0 1.0	16 10.5	ns	3-6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	14 10	1.0 1.0	14.5 10.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	12 9.0	1.0 1.0	13 10	ns	3-6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	10 7.5	12 9.5	1.0 1.0	13.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set-up Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3 5.0	3.5 2.0	6.5 4.5	7.5 5.0	ns	3-9
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3 5.0	−1.5 −0.5	0 0.5	0 0.5	ns	3-9
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	3.3 5.0	2.0 2.0	4.0 3.5	4.5 3.5	ns	3-6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3 5.0	−2.5 −1.5	0 0	0 0	ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	210		125		MHz	3-3
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	7.0	11	1.0	13	ns	3-6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10	1.0	11.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10	1.0	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Set-up Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0.5	2.0	2.5	ns	3-9
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0	2.0	2.0	ns	3-9
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	3.0	5.0	6.0	ns	3-6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	−2.5	0	0	ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	35	pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC138
MC74ACT138

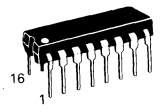
Product Preview

1-of-8 Decoder/Demultiplexer

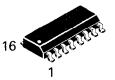
1-OF-8 DECODER/ DEMULTIPLEXER

The MC74AC138/74ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three MC74AC138/74ACT138 devices or a 1-of-32 decoder using four MC74AC138/74ACT138 devices and one inverter.

- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Active LOW Mutually Exclusive Outputs
- Outputs Source/Sink 24 mA
- 'ACT138 Has TTL Compatible Inputs

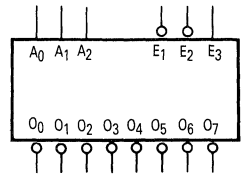


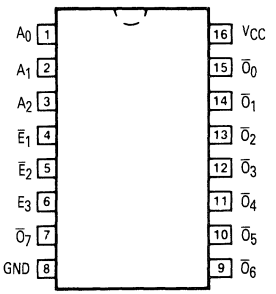
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

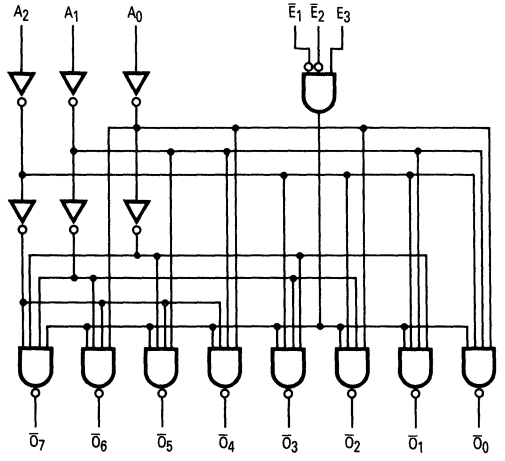
The MC74AC138/74ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_7$). The MC74AC138/74ACT138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enabled function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four MC74AC138/74ACT138 devices and one inverter (See Figure a). The MC74AC138/74ACT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

TRUTH TABLE

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

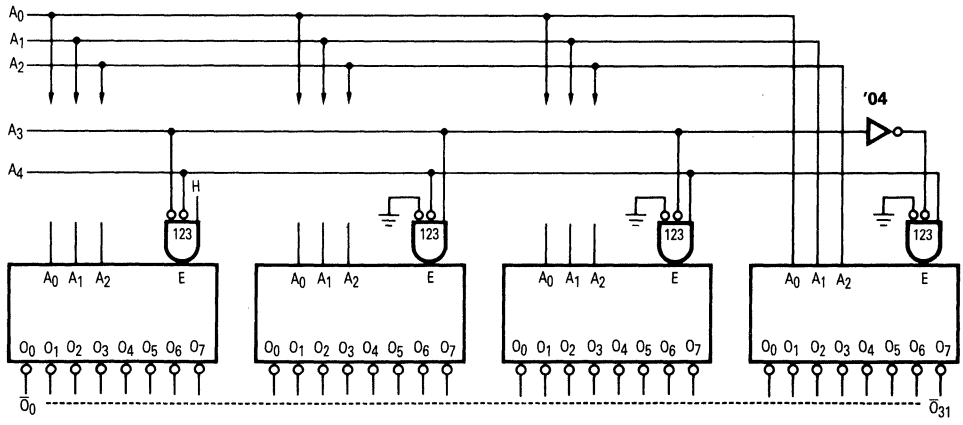
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure a: Expansion to 1-of-32 Decoding



DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT138)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, V_{CC} = 5.5 V, T_A = Worst Case

5

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.3 5.0	1.0 1.0	8.5 6.5	13 9.5	1.0 1.0	15 10.5	ns	3-6
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.3 5.0	1.0 1.0	8.0 6.0	12.5 9.0	1.0 1.0	14 10.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.3 5.0	1.0 1.0	11 8.0	15 11	1.0 1.0	16 12	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.3 5.0	1.0 1.0	9.5 7.0	13.5 9.5	1.0 1.0	15 10.5	ns	3-6
t_{PLH}	Propagation Delay E_3 to $\overline{O}_n$	3.3 5.0	1.0 1.0	11 8.0	15.5 11	1.0 1.0	16.5 12.5	ns	3-6
t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$	3.3 5.0	1.0 1.0	8.5 6.0	13 8.0	1.0 1.0	14 9.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.0	7.0	10.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.0	6.5	10.5	1.0	11.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.0	8.0	11.5	1.0	12.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.0	7.5	11.5	1.0	12.5	ns	3-6
t_{PLH}	Propagation Delay E_3 to $\overline{O}_n$	5.0	1.0	8.0	12	1.0	13	ns	3-6
t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$	5.0	1.0	6.5	10.5	1.0	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	60	pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC139
MC74ACT139

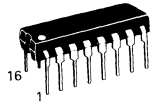
Product Preview

Dual 1-of-4 Decoder/Demultiplexer

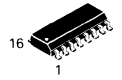
DUAL 1-OF-4 DECODER/DEMULTIPLEXER

The MC74AC139/74ACT139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually-exclusive active-LOW outputs. Each decoder has an active-LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the MC74AC139/74ACT139 can be used as a function generator providing all four minterms of two variables.

- Multifunction Capability
- Two Completely Independent 1-of-4 Decoders
- Active LOW Mutually Exclusive Outputs
- Outputs Source/Sink 24 mA
- 'ACT139 Has TTL Compatible Inputs

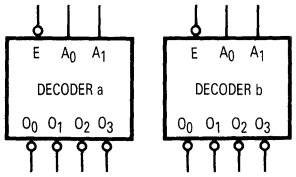


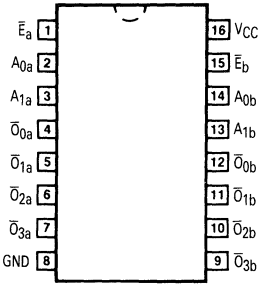
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

A_0, A_1	Address Inputs
$\overline{E}$	Enable Inputs
$\overline{O}_0$–$\overline{O}_3$	Outputs

TRUTH TABLE

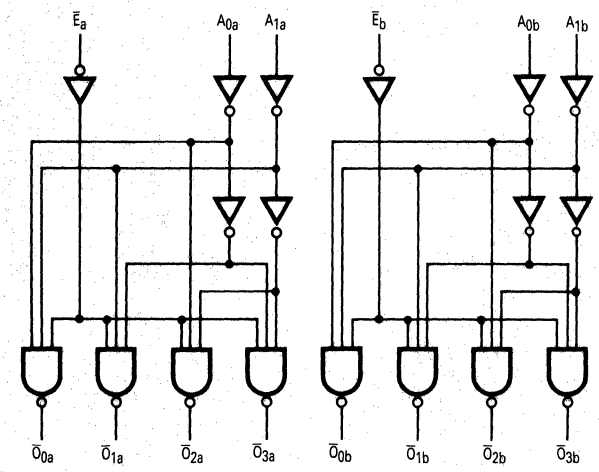
Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

5

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

LOGIC DIAGRAM

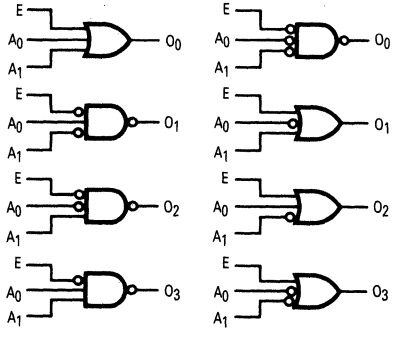


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The MC74AC139/74ACT139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0–A_1) and provides four mutually exclusive active-LOW outputs ($\overline{O}_0$–$\overline{O}_3$). Each decoder has an active-LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the MC74AC139/74ACT139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Figure a, and thereby reducing the number of packages required in a logic network.

Figure a: Gate Functions (each half)



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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.3 5.0	1.0 1.0	8.0 6.5	11.5 8.5	1.0 1.0	13 9.5	ns	3-6
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.3 5.0	1.0 1.0	7.0 5.5	10 7.5	1.0 1.0	11 8.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	3.3 5.0	1.0 1.0	9.5 7.0	12 8.5	1.0 1.0	13 10	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	3.3 5.0	1.0 1.0	8.0 6.0	10 7.5	1.0 1.0	11 8.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.0	6.0	8.5	1.0	9.5	ns	3-6
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.0	6.0	9.5	1.0	10.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	5.0	1.0	7.0	10	1.0	11	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	5.0	1.0	7.0	9.5	1.0	10.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC151
MC74ACT151

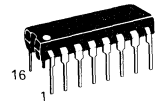
Product Preview

1-of-8 Decoder/Demultiplexer

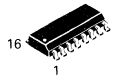
1-OF-8
DECODER/DEMULTIPLEXER

The MC74AC151/74ACT151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The MC74AC151/74ACT151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

- Outputs Source/Sink 24 mA
- 'ACT151 Has TTL Compatible Inputs

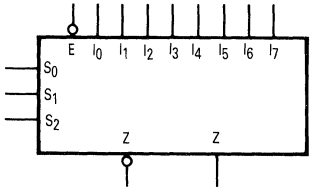


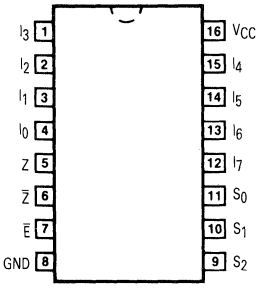
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

I_0–I_7	Data Inputs
S_0–S_2	Select Inputs
$\overline{E}$	Enable Input
Z	Data Output
$\overline{Z}$	Inverted Data Output

TRUTH TABLE

Inputs				Outputs	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

5

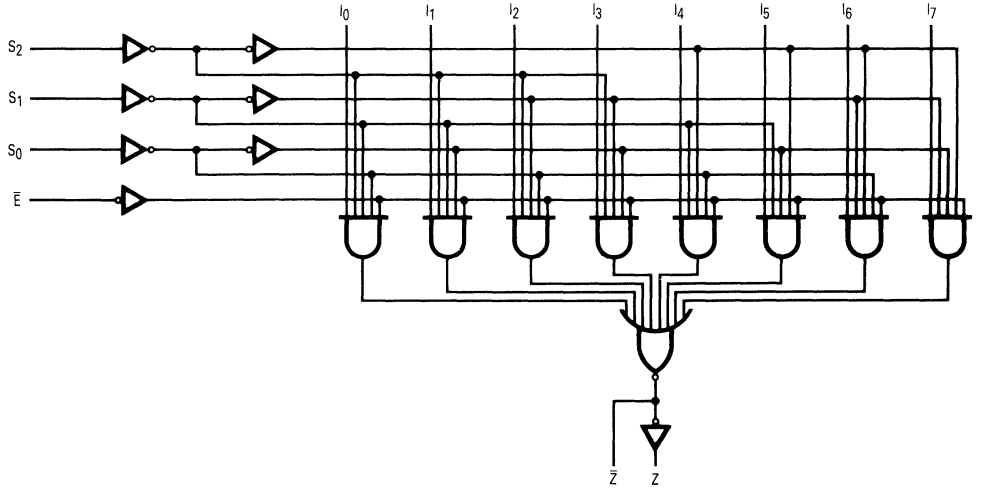
FUNCTIONAL DESCRIPTION

The MC74AC151/74ACT151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

The MC74AC151/74ACT151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the MC74AC151/74ACT151 can provide any logic function of four variables and its complement.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT151)	1.5	mA	V_{IN} = V_{CC} − 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	3.3 5.0	1.0 1.0	11.5 8.5	18 13	1.0 1.0	20 15	ns	3-6
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	3.3 5.0	1.0 1.0	12 8.5	18 13	1.0 1.0	20 15	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	3.3 5.0	1.0 1.0	8.0 6.0	13 10	1.0 1.0	14 11	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	3.3 5.0	1.0 1.0	8.5 6.5	13 10	10 1.0	14 11	ns	3-6
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	3.3 5.0	1.0 1.0	9.5 7.0	14 10.5	1.0 1.0	15.5 11	ns	3-5
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	3.3 5.0	1.0 1.0	9.5 7.0	15 11	1.0 1.0	16 12	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z	5.0	1.0	12.5	15.5	1.0	17	ns	3-6
t_{PHL}	Propagation Delay S_n to Z	5.0	1.0	12.5	15.5	1.0	16.5	ns	3-6
t_{PLH}	Propagation Delay S_n to $\overline{Z}$	5.0	1.0	12.5	15	1.0	16.5	ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}$	5.0	1.0	12.5	16.5	1.0	18.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}$ to Z	5.0	1.0	10	9.5	1.0	10	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}$ to Z	5.0	1.0	10.5	9.0	1.0	10	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}$ to $\overline{Z}$	5.0	1.0	10	8.5	1.0	9.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$	5.0	1.0	10.5	10	1.0	10.5	ns	3-6
t_{PLH}	Propagation Delay I_n to Z	5.0	1.0	11	11.5	1.0	12.5	ns	3-6
t_{PHL}	Propagation Delay I_n to Z	5.0	1.0	11	12	1.0	13.5	ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}$	5.0	1.0	11	12	1.0	13	ns	3-6
t_{PHL}	Propagation Delay I_n to $\overline{Z}$	5.0	1.0	11	12.5	1.0	14	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	70	pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC153
MC74ACT153

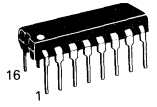
Product Preview

Dual 4-Input Multiplexer

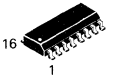
DUAL 4-INPUT MULTIPLEXER

The MC74AC153/74ACT153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the MC74AC153/74ACT153 can act as a function generator and generate any two functions of three variables.

- Outputs Source/Sink 24 mA
- 'ACT153 Has TTL Compatible Inputs

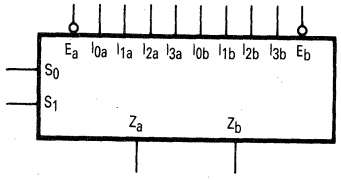


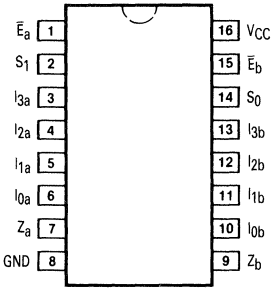
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\bar{E}_a$	Side A Enable Input
$\bar{E}_b$	Side B Enable Input
Z_a	Side A Output
Z_b	Side B Output

TRUTH TABLE

Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\bar{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

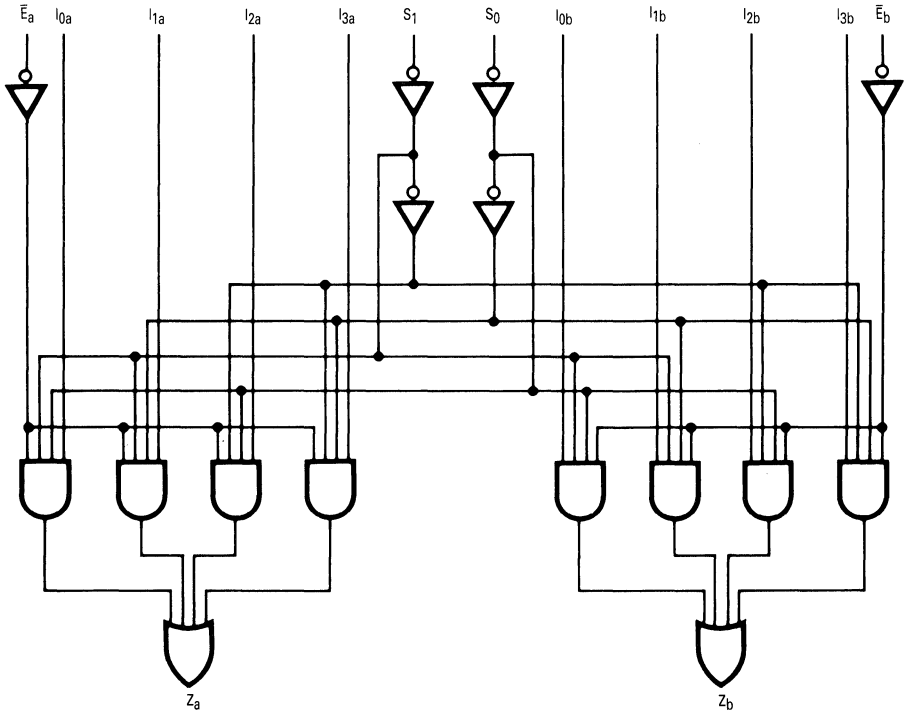
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

The MC74AC153/74ACT153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The MC74AC153/74ACT153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$
$$Z_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	3.3 5.0	1.0 1.0	9.5 6.5	15 11	1.0 1.0	17.5 12.5	ns	3-6
t_{PHL}	Propagation Delay S_n to Z_n	3.3 5.0	1.0 1.0	8.5 6.5	14.5 11	1.0 1.0	16.5 12	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to Z_n	3.3 5.0	1.0 1.0	8.0 5.5	13.5 9.5	1.0 1.0	16 11	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	3.3 5.0	1.0 1.0	7.0 5.0	11 8.0	1.0 1.0	12.5 9.0	ns	3-6
t_{PLH}	Propagation Delay I_n to Z_n	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0	1.0 1.0	14.5 10.5	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	3.3 5.0	1.0 1.0	7.0 5.0	11.5 8.5	1.0 1.0	13 10	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	5.0	1.0	7.0	11.5	1.0	13.5	ns	3-6
t_{PHL}	Propagation Delay S_n to Z_n	5.0	1.0	7.0	11.5	1.0	13.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	1.0	6.5	10.5	1.0	12.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	1.0	6.0	9.5	1.0	11	ns	3-6
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.0	5.5	9.5	1.0	11	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.0	5.5	9.5	1.0	11	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	65	pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC157
MC74ACT157

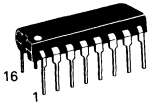
Product Preview

Quad 2-Input Multiplexer

QUAD 2-INPUT MULTIPLEXER

The MC74AC157/74ACT157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The MC74AC157/74ACT157 can also be used as a function generator.

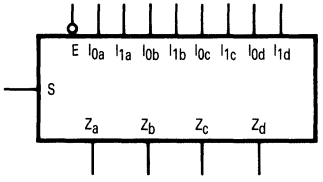
- Outputs Source/Sink 24 mA
- 'ACT157 Has TTL Compatible Inputs

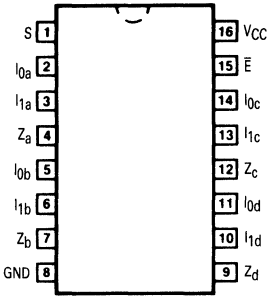


N SUFFIX
CASE 648-08
PLASTIC

D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Z_a–Z_d	Outputs

TRUTH TABLE

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

5

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

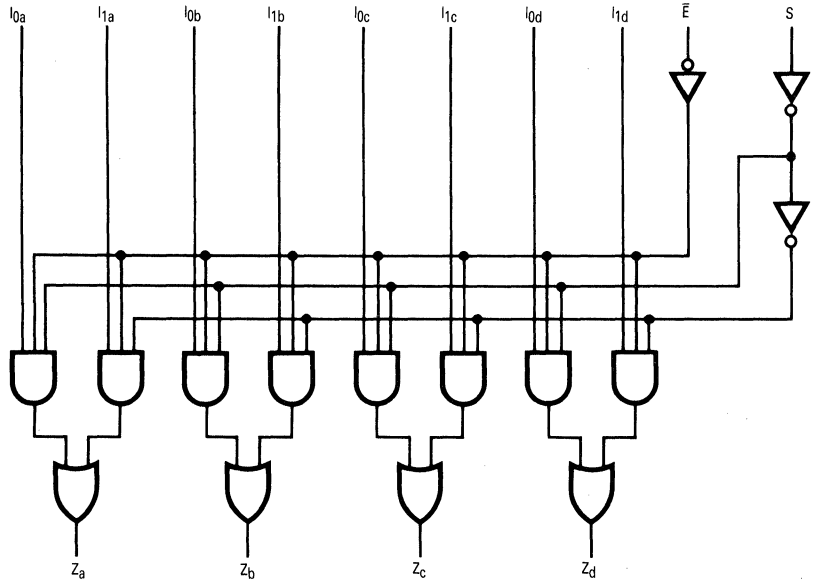
FUNCTIONAL DESCRIPTION

The MC74AC157/74ACT157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The MC74AC157/74ACT157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$Z_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$
$Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$
$Z_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$
$Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$

A common use of the MC74AC157/74ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The MC74AC157/74ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S to Z_n	3.3 5.0	1.0 1.0	7.0 5.5	11.5 9.0	1.0 1.0	13 10	ns	3-6
t_{PHL}	Propagation Delay S to Z_n	3.3 5.0	1.0 1.0	6.5 5.0	11 8.5	1.0 1.0	12 9.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	3.3 5.0	1.0 1.0	7.0 5.5	11.5 9.0	1.0 1.0	13 10	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	3.3 5.0	1.0 1.0	6.5 5.5	11 9.0	1.0 1.0	12 9.5	ns	3-6
t_{PLH}	Propagation Delay I_n to Z_n	3.3 5.0	1.0 1.0	5.0 4.0	8.5 6.5	1.0 1.0	9.0 7.0	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	3.3 5.0	1.0 1.0	5.0 4.0	8.0 6.5	1.0 1.0	9.0 7.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S to Z_n	5.0	1.0	5.5	9.0	1.0	10	ns	3-6
t_{PHL}	Propagation Delay S to Z_n	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	1.0	6.0	10	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	1.0	5.0	8.5	1.0	9.0	n	3-6
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.0	4.0	7.0	1.0	8.5	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.0	4.5	7.5	1.0	8.5	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC158
MC74ACT158

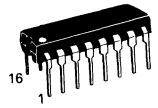
Product Preview

Quad 2-Input Multiplexer

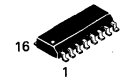
QUAD 2-INPUT MULTIPLEXER

The MC74AC158/74ACT158 is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The MC74AC158/74ACT158 can also be used as a function generator.

- Outputs Source/Sink 24 mA
- 'ACT158 Has TTL Compatible Inputs

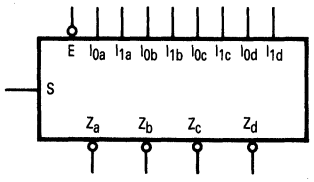


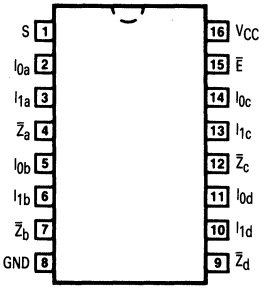
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

I_{0a}–I_{0d}	Source 0 Data Inputs
I_{1a}–I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
$\overline{Z}_a$–$\overline{Z}_d$	Inverted Outputs

TRUTH TABLE

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

5

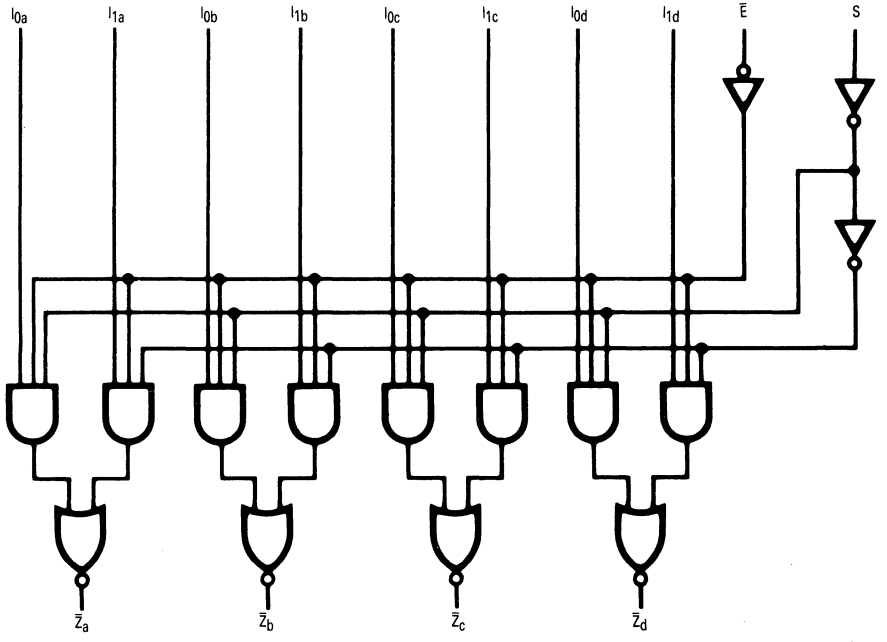
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

The MC74AC158/74ACT158 quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs. The MC74AC158/74ACT158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the MC74AC158/74ACT158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The MC74AC158/74ACT158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additiona I_{CC}/Input ('ACT158)	1.5	mA	V_{IN} = V_{CC} − 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	3.3 5.0	1.0 1.0	7.0 5.5	11.5 9.0	1.0 1.0	12.5 9.5	ns	3-6
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	3.3 5.0	1.0 1.0	7.0 5.5	11.5 9.0	1.0 1.0	12.5 10	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	3.3 5.0	1.0 1.0	7.5 6.0	12 9.5	1.0 1.0	13 10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	3.3 5.0	1.0 1.0	7.0 5.5	11 8.5	1.0 1.0	12 9.5	ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0	1.0 1.0	5.5 4.0	9.0 7.0	1.0 1.0	10 7.5	ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0	1.0 1.0	5.0 4.0	8.0 6.5	1.0 1.0	8.5 6.5	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	5.0	1.0	6.0	9.5	1.0	11	ns	3-6
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	5.0	1.0	5.5	9.0	1.0	10	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.0	4.5	8.0	1.0	8.5	ns	3-6
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.0	4.0	6.5	1.0	7.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC160
MC74ACT160
MC74AC162
MC74ACT162

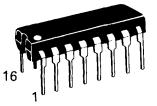
Product Preview

Synchronous Presettable BCD Decade Counter

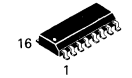
SYNCHRONOUS PRESETTABLE BCD DECADE COUNTER

The MC74AC160/74ACT160 and MC74AC162/74ACT162 are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC74AC160/74ACT160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74AC162/74ACT162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 120 MHz
- Outputs Source/Sink 24 mA
- 'ACT160 and 'ACT162 Have TTL Compatible Inputs

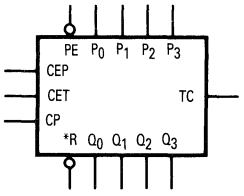


N SUFFIX
CASE 648-08
PLASTIC

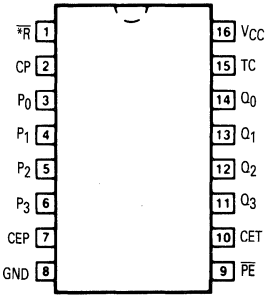


D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL



* $\overline{MR}$ for '160
* $\overline{SR}$ for '162



PIN NAMES

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$ ('160)	Asynchronous Master Reset Input
$\overline{SR}$ ('162)	Synchronous Reset Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

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FUNCTIONAL DESCRIPTION

The MC74AC160/74ACT160 and MC74AC162/74ACT162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '160) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('160), synchronous reset ('162), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{MR}$, '160), Synchronous Reset ($\overline{SR}$, '162), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('160) or $\overline{SR}$ ('162) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74AC160/74ACT160 and MC74AC162/74ACT162 use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC74AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the MC74AC160/74ACT160 and MC74AC162/74ACT162 decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations: Count Enable = $CEP \cdot CET \cdot \overline{PE}$

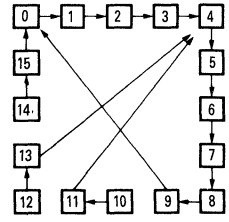
$TC = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot CET$

MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For '162 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM



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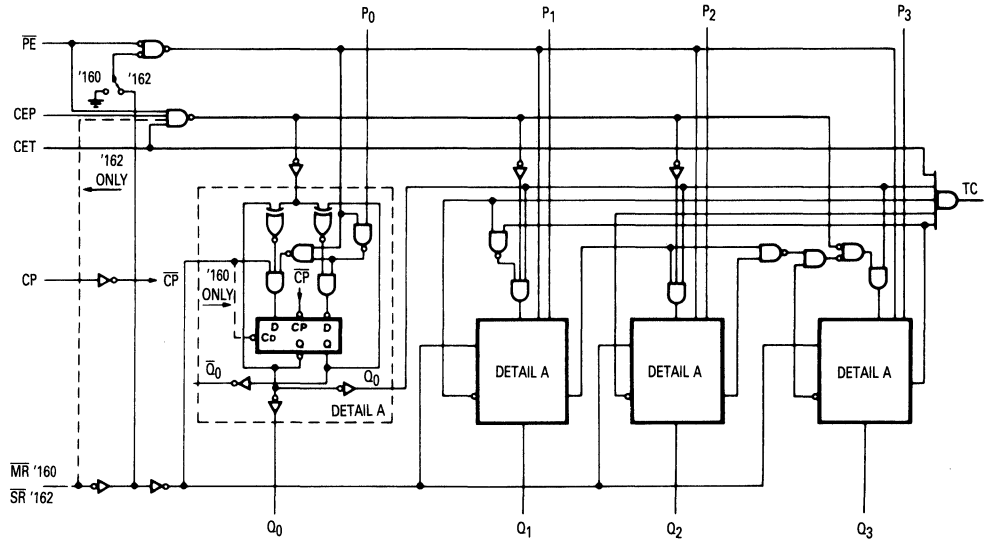
LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT160/162)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, V_{CC} = 5.5 V, T_A = Worst Case

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		87 118				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	3.3 5.0		7.5 5.5				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	3.3 5.0		8.5 6.0				ns	3-6
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	3.3 5.0		9.5 7.0				ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0		11 8.0				ns	3-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0		7.5 5.5				ns	3-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0		8.5 6.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n ('AC160)	3.3 5.0		8.5 6.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('AC160)	3.3 5.0		8.5 6.0				ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0			ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	3.3 3.3	5.5 4.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5			ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5			ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0			ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0			ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0			ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW ('AC160)	3.3 5.0	4.5 3.0			ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP ('AC160)	3.3 5.0	0 0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0		118				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	5.0		5.5				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	5.0		6.0				ns	3-6
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	5.0		7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	5.0		7.0				ns	3-6
t_{PLH}	Propagation Delay CP to TC	5.0		7.0				ns	3-6
t_{PHL}	Propagation Delay CP to TC	5.0		8.0				ns	3-6
t_{PLH}	Propagation Delay CET to TC	5.0		5.5				ns	3-6
t_{PHL}	Propagation Delay CET to TC	5.0		6.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n ('ACT160)	5.0		6.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('ACT160)	5.0		6.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0			ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP ('ACT162)	5.0	4.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP ('ACT162)	5.0	−5.5			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{MR}$ to CP ('ACT160)	5.0	4.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{MR}$ to CP ('ACT160)	5.0	−5.5			ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5			ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0			ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0			ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0			ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW ('ACT160)	5.0	3.0			ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP ('ACT160)	5.0	0			ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC161
MC74ACT161
MC74AC163
MC74ACT163

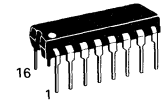
Product Preview

Synchronous Presettable Binary Counter

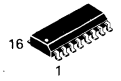
SYNCHRONOUS PRESETTABLE BINARY COUNTER

The MC74AC161/74ACT161 and MC74AC163/74ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The MC74AC161/74ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The MC74AC163/74ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 125 MHz
- Outputs Source/Sink 24 mA
- 'ACT161 and 'ACT163 Have TTL Compatible Inputs

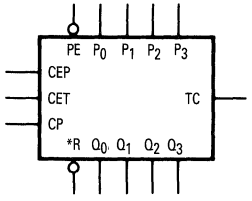


N SUFFIX
CASE 648-08
PLASTIC

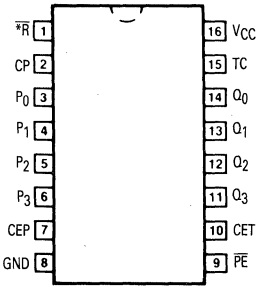


D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL



* $\overline{MR}$ for '161
* $\overline{SR}$ for '163



PIN NAMES

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$ ('161)	Asynchronous Master Reset Input
$\overline{SR}$ ('163)	Synchronous Reset Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

5

FUNCTIONAL DESCRIPTION

The MC74AC161/74ACT161 and MC74AC163/74ACT163 count modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('161), synchronous reset ('163), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{MR}$, '161), Synchronous Reset ($\overline{SR}$, '163), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('161) or $\overline{SR}$ ('163) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The MC74AC161/74ACT161 and MC74AC163/74ACT163 use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the MC74AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = CEP•CET•$\overline{PE}$

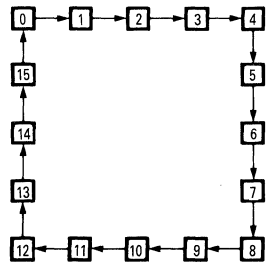
$$TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$$

MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge ( )
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For '163 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM



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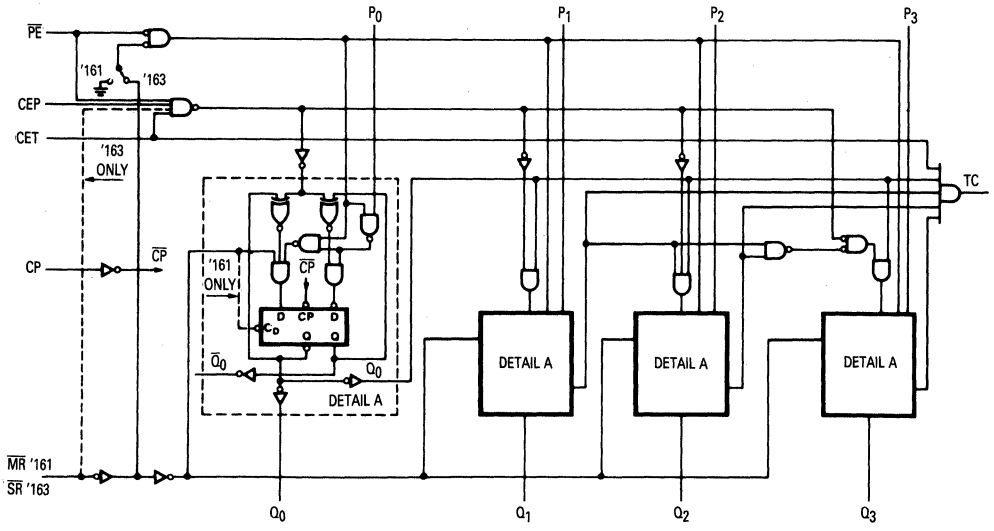
BLOCK DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT161/163)	1.5	mA	V_{IN} = V_{CC} − 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC161 T_A = +25°C, C_L = 50 pF			74AC161 T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		87 118				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0		7.5 5.5				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0		8.5 6.0				ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0		11 8.0				ns	3-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0		7.5 5.5				ns	3-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0		8.5 6.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0		8.5 6.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	3.3 5.0		11 8.0				ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC161 T_A = +25°C, C_L = 50 pF		74AC161 T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0			ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 3.3	5.5 4.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	5.5 4.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−7.5 −5.5			ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5			ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0			ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0			ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0			ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	4.5 3.0			ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT161 T_A = +25°C, C_L = 50 pF			74ACT161 T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	115	125		100		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	6.0	10.5	1.0	11.5	ns	3-6
t_{PLH}	Propagation Delay CP to TC	5.0	1.0	7.0	11	1.0	12.5	ns	3-6
t_{PHL}	Propagation Delay CP to TC	5.0	1.0	8.0	12.5	1.0	13.5	ns	3-6
t_{PLH}	Propagation Delay CET to TC	5.0	1.0	5.5	8.5	1.0	10	ns	3-6
t_{PHL}	Propagation Delay CET to TC	5.0	1.0	6.0	9.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.0	6.0	10	1.0	11	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	5.0	1.0	8.0	13.5	1.0	14.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT161 T_A = +25°C, C_L = 50 pF		74ACT161 T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	9.5	11.5	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0	0	0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{MR}$ to CP	5.0	4.0	8.5	9.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{MR}$ to CP	5.0	−5.5	−0.5	−0.5	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5	9.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5	−0.5	ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5	6.5	ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0	0	ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.0	3.5	ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.0	3.5	ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	3.0	3.0	7.5	ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	0	0.5	ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC163 $T_A = +25°C$, $C_L = 50$ pF			74AC163 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 110	87 118		60 95		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0	1.0 1.0	13.5 9.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.0 1.0	8.5 6.0	12 9.5	1.0 1.0	13 10	ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	1.0 1.0	9.5 7.0	15 10.5	1.0 1.0	16.5 11.5	ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	1.0 1.0	11 8.0	14 11	1.0 1.0	15.5 11.5	ns	3-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	1.0 1.0	7.5 5.5	9.5 6.5	1.0 1.0	11 7.5	ns	3-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	1.0 1.0	8.5 6.0	11 8.5	1.0 1.0	12.5 9.5	ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC163 $T_A = +25°C$, $C_L = 50$ pF		74AC163 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0	13.5 8.5	16 10.5	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0	−1.0 0	−0.5 0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	5.5 4.0	14 9.5	16.5 11	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5	−1.0 −0.5	−0.5 0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	5.5 4.0	11.5 7.5	14 8.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−7.5 −5.0	−1.0 −0.5	−0.5 0	ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5	6.0 4.5	7.0 5.0	ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0	0 0	0 0.5	ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0	3.5 2.5	4.0 3.0	ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0	4.0 3.0	4.5 3.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT163 T_A = +25°C, C_L = 50 pF			74ACT163 T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	120	128		105		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	5.5	10	1.0	11	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	6.0	11	1.0	12	ns	3-6
t_{PLH}	Propagation Delay CP to TC	5.0	1.0	7.0	11.5	1.0	13.5	ns	3-6
t_{PHL}	Propagation Delay CP to TC	5.0	1.0	8.0	13.5	1.0	15	ns	3-6
t_{PLH}	Propagation Delay CET to TC	5.0	1.0	5.5	9.0	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay CET to TC	5.0	1.0	6.0	10	1.0	11	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT163 T_A = +25°C, C_L = 50 pF		74ACT163 T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	10	12	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0	0.5	0.5	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	4.0	10	11.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	−5.5	−0.5	−0.5	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5	10.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5	0	ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5	6.5	ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0	0.5	ns	3-9
t_w	Clock Pulse Width HIGH or LOW	5.0	2.0	3.5	3.5	ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5	3.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Type	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC168
MC74AC169

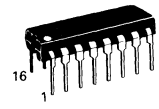
Product Preview

4-Stage Synchronous Bidirectional Counters

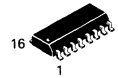
4-STAGE SYNCHRONOUS BIDIRECTIONAL COUNTERS

The MC74AC168 and MC74AC169 are fully synchronous 4-stage up/down counters. The MC74AC168 is a BCD decade counter; the MC74AC169 is a modulo-16 binary counter. Both feature a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

- Synchronous Counting and Loading
- Built-in Lookahead Carry Capability
- Presettable for Programmable Operation
- Outputs Source/Sink 24 mA

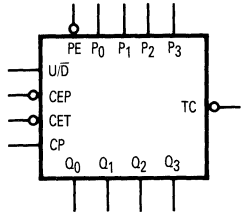


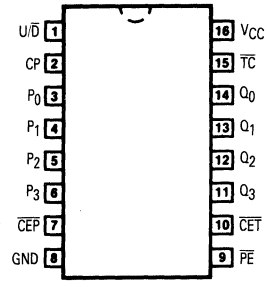
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





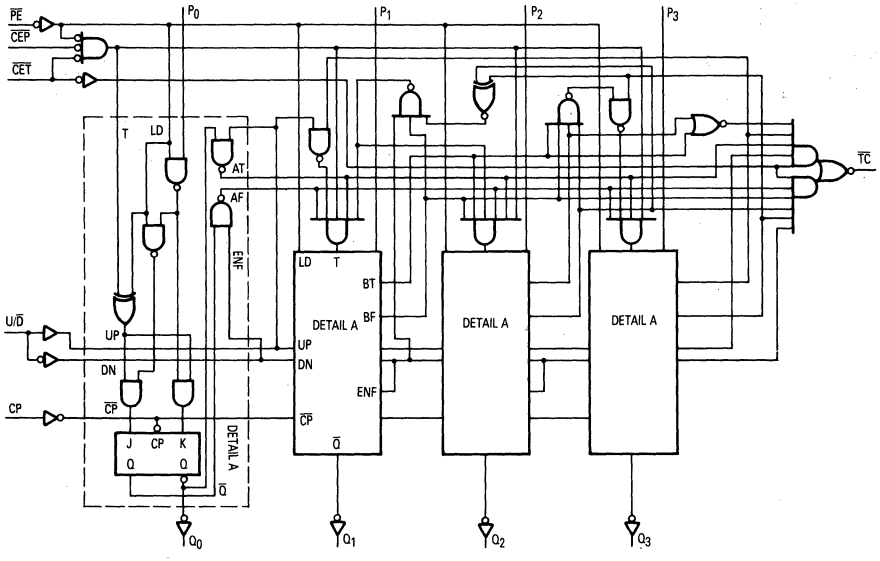
PIN NAMES

$\overline{CEP}$	Count Enable Parallel Input
$\overline{CET}$	Count Enable Trickle Input
CP	Clock Pulse Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
U/$\overline{D}$	Up-Down Count Control Input
Q_0–Q_3	Flip-Flop Outputs
$\overline{TC}$	Terminal Count Output

5

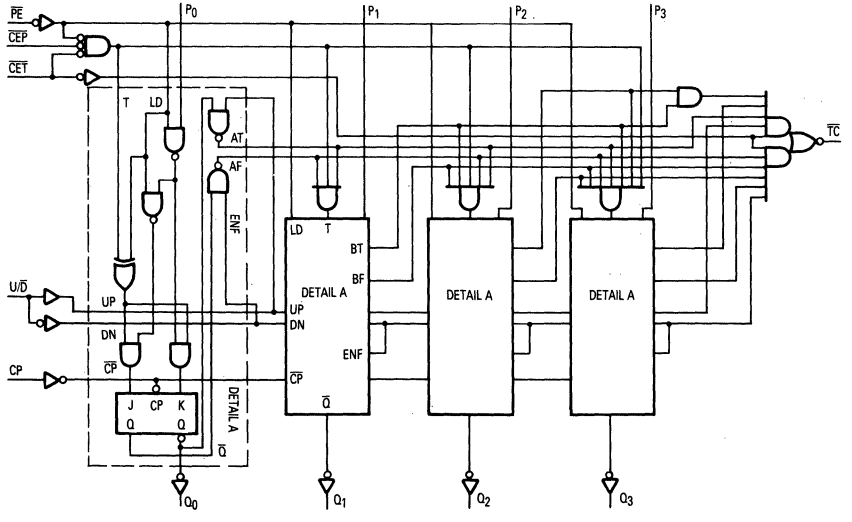
LOGIC DIAGRAMS

MC74AC168



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MC74AC169



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

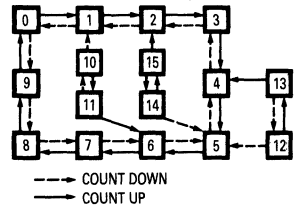
FUNCTIONAL DESCRIPTION

The MC74AC168 and MC74AC169 use edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0–P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the MC74AC169) in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the MC74AC168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the MC74AC169 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

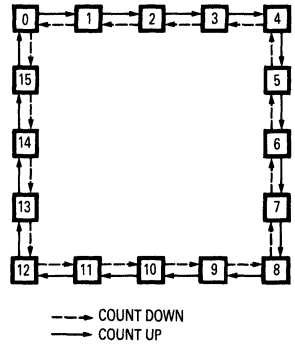
1) Count Enable = $\overline{CEP}$•$\overline{CET}$•$\overline{PE}$
2) Up: ('AC168): $\overline{TC} = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (\text{Up}) \cdot \overline{CET}$
   ('AC169): $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (\text{Up}) \cdot \overline{CET}$
3) Down (both): $\overline{TC} = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (\text{Down}) \cdot \overline{CET}$

STATE DIAGRAM

MC74AC168



MC74AC169



MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (P_n to Q_n)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC168 T_A = +25°C, C_L = 50 pF			74AC168 T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		118 154				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0		10.5 7.5				ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{TC}$	3.3 5.0		13.5 9.5				ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0		13.5 9.5				ns	3-6
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0		11 8.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0		9.5 7.0				ns	3-6
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0		10.5 7.5				ns	3-6
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0		9.0 6.5				ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC168 T_A = +25°C, C_L = 50 pF		74AC168 T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	3.0 1.5			ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	1.5 0.5			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 3.3	7.5 4.5			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	4.5 2.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	7.0 4.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	6.0 4.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 2.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 1.5			ns	3-9
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	3.3 5.0	12.5 9.0			ns	3-9
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to $\overline{CP}$	3.3 5.0	7.0 4.0			ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC169 T_A = +25°C, C_L = 50 pF			74AC169 T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	75 100	118 154		65 90		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0	1.0 1.0	9.5 7.0	13 10	1.0 1.0	14.5 11	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0	1.0 1.0	10.5 7.5	14.5 11	1.0 1.0	16 12	ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	1.0 1.0	13.5 9.5	18 13	1.0 1.0	22 14	ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	1.0 1.0	13.5 9.5	18 13	1.0 1.0	20.5 14.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	11 8.0	15 10.5	1.0 1.0	16.5 12	ns	3-6
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	9.5 7.0	12.5 9.0	1.0 1.0	14.5 10	ns	3-6
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	11 8.0	15 10.5	1.0 1.0	17 12	ns	3-6
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	10 7.0	13.5 9.5	1.0 1.0	15.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC169 T_A = +25°C, C_L = 50 pF		74AC169 T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	3.0 1.5	4.5 2.5	5.0 2.5	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	1.5 0.5	0.5 1.5	0.5 1.5	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	7.5 4.5	10.5 7.0	12.5 8.0	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	4.5 2.0	0 0.5	0 1.0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	7.0 4.0	10 6.5	12 8.0	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	6.0 4.0	0 0.5	0 1.0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 2.0	5.5 3.5	6.5 4.0	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 1.5	0 0.5	0 0.5	ns	3-9
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	3.3 5.0	7.0 4.5	10 6.5	11.5 7.5	ns	3-9
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to $\overline{CP}$	3.3 5.0	7.0 4.0	0 0.5	0 0.5	ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0	3.0 3.0	4.0 3.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	60	pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC174
MC74ACT174

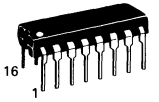
Product Preview

Hex D Flip-Flop with Master Reset

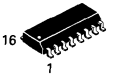
HEX D FLIP-FLOP WITH MASTER RESET

The MC74AC174/74ACT174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

- Outputs Source/Sink 24 mA
- 'ACT174 Has TTL Compatible Inputs

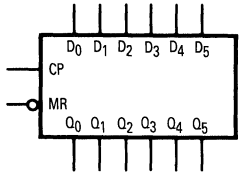


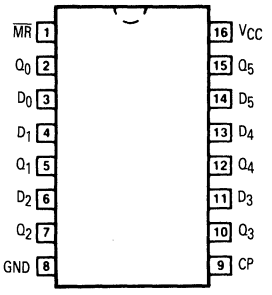
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_5	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_5	Outputs

TRUTH TABLE

Inputs			Output
$\overline{MR}$	CP	D	Q
L	X	X	L
H	⎍	H	H
H	⎍	L	L
H	L	X	Q

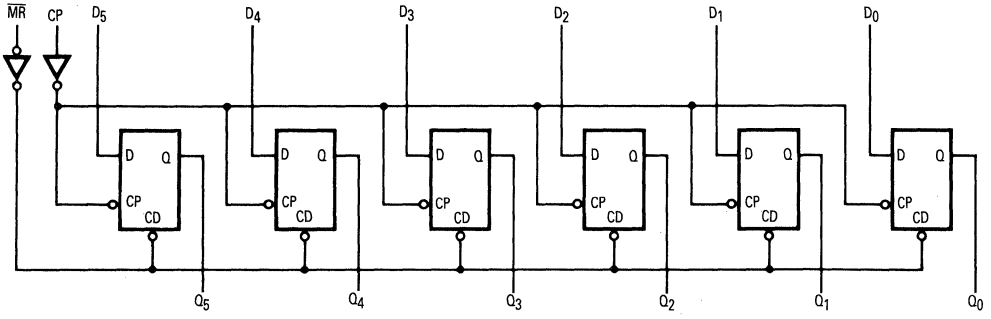
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⎍ = LOW-to-HIGH Transition of Clock

5

FUNCTIONAL DESCRIPTION

The MC74AC174/74ACT174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The MC74AC174/74ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT174)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	90 100	100 125		70 100		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	1.0 1.0	9.0 6.0	11.5 8.5	1.0 1.0	12.5 9.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	1.0 1.0	8.5 6.0	11 8.0	1.0 1.0	12 9.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0	1.0 1.0	9.0 7.0	11.5 9.0	1.0 1.0	12.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.5 2.0	6.5 5.0	7.0 5.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	1.0 0.5	3.0 3.0	3.0 3.0	ns	3-9
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0	ns	3-6
t_w	CP Pulse Width	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0	ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0	2.5 2.0	2.5 2.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	165	200		140		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	5.0	1.0	7.0	10.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	5.0	1.0	7.0	10.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.0	6.5	9.5	1.0	11	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	0.5	1.5	1.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0	2.0	2.0	ns	3-9
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	1.5	3.0	3.5	ns	3-6
t_w	CP Pulse Width HIGH or LOW	5.0	1.5	3.0	3.5	ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	−1.0	0.5	0.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	85	pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC175
MC74ACT175

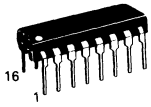
Product Preview

Quad D Flip-Flop

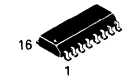
QUAD D FLIP-FLOP

The MC74AC175/74ACT175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Asynchronous Common Reset
- True and Complement Output
- Outputs Source/Sink 24 mA
- 'ACT175 Has TTL Compatible Inputs

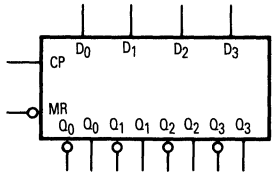


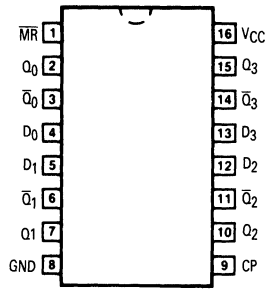
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_3	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0–Q_3	True Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complement Outputs

TRUTH TABLE

Inputs	Outputs	
@ t_n, $\overline{MR}$ = H	@ t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

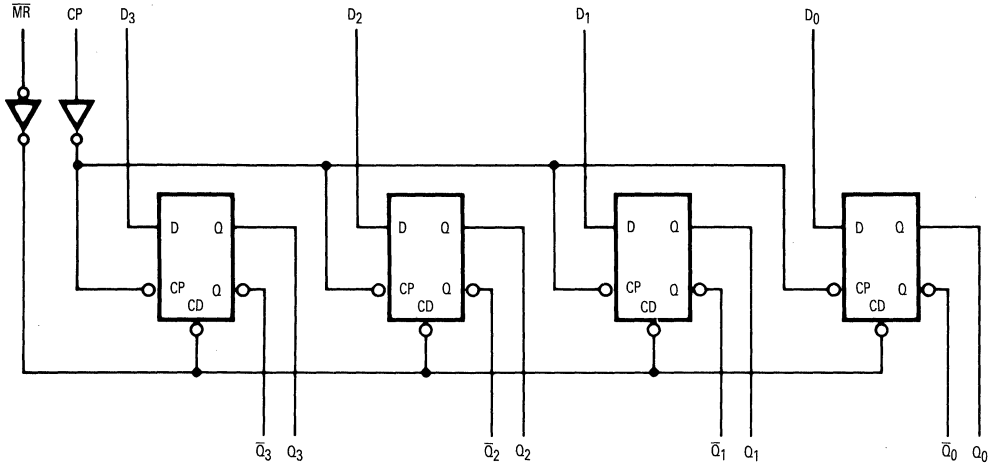
H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

5

FUNCTIONAL DESCRIPTION

The MC74AC175/74ACT175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The MC74AC175/74ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT175)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		118 160				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3 5.0		8.5 6.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0		7.5 5.5				ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	3.3 5.0		8.5 6.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	5.5 4.0			ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	5.5 4.0			ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	175	160		145		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10	1.0	11	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	5.0	1.0	7.0	11	1.0	12	ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.0	6.0	9.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s (H) t_s (L)	Setup Time D_n to CP	5.0	3.0 3.0	2.0 2.5	2.0 2.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.0	1.0	ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	4.0	3.0	3.5	ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	4.0	3.5	4.0	ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	0	0	ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC190
MC74AC191

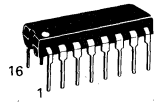
Product Preview

Up/Down Counters with Preset and Ripple Clock

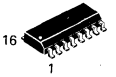
UP/DOWN COUNTERS WITH PRESET AND RIPPLE CLOCK

The MC74AC190 is a reversible BCD (8421) decade counter. The MC74AC191 is a reversible modulo 16 binary counter. Both feature synchronous counting and asynchronous presetting. The preset feature allows the MC74AC190 and MC74AC191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- High-Speed — 120 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Parallel Load
- Cascadable
- Outputs Source/Sink 24 mA

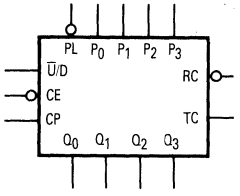


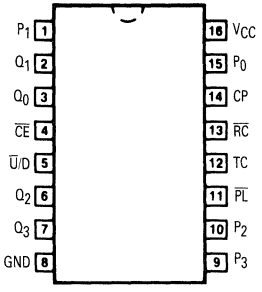
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

$\overline{CE}$	Count Enable Input
CP	Clock Pulse Input
P_0–P_3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input
$\overline{U}$/D	Up/Down Count Control Input
Q_0–Q_3	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output
TC	Terminal Count Output

5

FUNCTIONAL DESCRIPTION

The MC74AC190/74C191 are synchronous up/down counters. The MC74AC190 is a BCD decade counter while the MC74AC191 is organized as a 4-bit binary counter. Both contain four edge-triggered flip-flops with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Load inputs (P_0–P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The terminal count (TC) output is normally LOW. It goes HIGH when the circuits reach zero in the count down mode or 9 (MC74AC190) or 15 (MC74AC191) in the count up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures a and b. In Figure a, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

MODE SELECT TABLE

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

$\overline{RC}$ TRUTH TABLE

Inputs			Outputs
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⌐¬	⌐¬
H	X	X	H
X	L	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

STATE DIAGRAM

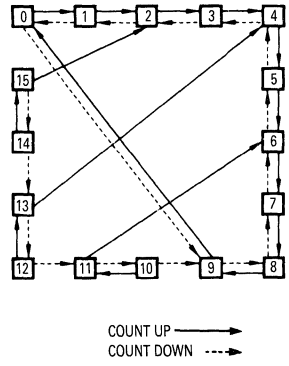


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Figure a: N-Stage Counter Using Ripple Clock

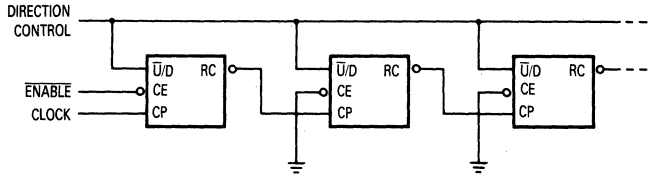


Figure b: Synchronous N-Stage Counter Using Ripple Carry/Borrow

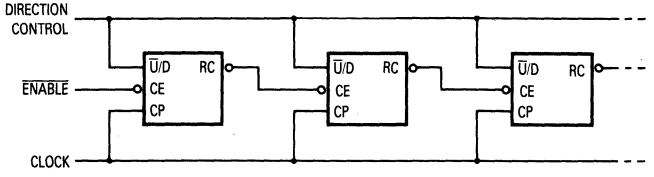
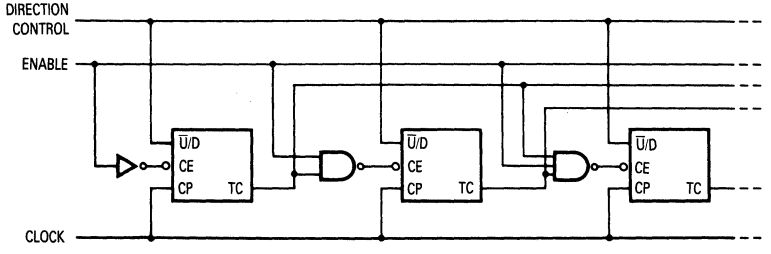


Figure c: Synchronous N-Stage Counter With Parallel Gated Carry/Borrow



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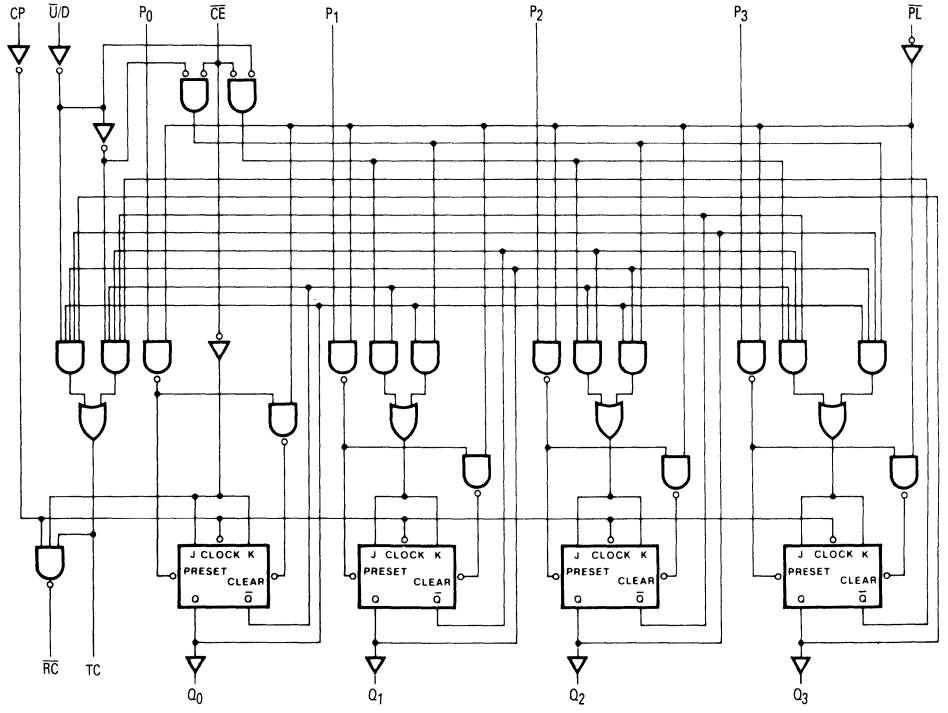
LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of the logic operations and should not be used to estimate propagation delays.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC190 T_A = +25°C, C_L = 50 pF			74AC190 T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		88 120				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0		10.5 7.5				ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0		15 11				ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0		13 9.5				ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{RC}$	3.3 5.0		9.0 6.5				ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{RC}$	3.3 5.0		9.5 7.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0		8.5 6.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	3.3 5.0		11 8.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	3.3 5.0		10.5 7.5				ns	3-6
t_{PLH}	Propagation Delay $\overline{U}$/D to TC	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{U}$/D to TC	3.3 5.0		9.5 7.0				ns	3-6
t_{PLH}	Propagation Delay P_n to Q_n	3.3 5.5		10.5 7.5				ns	3-6
t_{PHL}	Propagation Delay P_n to Q_n	3.3 5.0		9.5 7.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0		11.5 8.5				ns	3-6
t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0		11.5 8.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC190 T_A = +25°C, C_L = 50 pF		74AC190 T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	−0.5 −0.5			ns	3-9
t_s	Setup Time, LOW $\overline{CE}$ to CP	3.3 5.0	7.0 5.0			ns	3-9
t_h	Hold Time, LOW $\overline{CE}$ to CP	3.3 5.0	−1.5 −1.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{U}$/D to CP	3.3 5.0	7.0 5.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{U}$/D to CP	3.3 5.0	−1.5 −1.0			ns	3-9
t_w	$\overline{PL}$ Pulse Width, LOW	3.3 5.0	5.5 6.0			ns	3-6
t_w	CP Pulse Width, LOW	3.3 5.0	5.5 6.0			ns	3-6
t_{rec}	Recovery Time $\overline{PL}$ to CP	3.3 5.0	4.5 3.0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC191 T_A = +25°C, C_L = 50 pF			74AC191 T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 90	105 133		65 85		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	3.0 2.0	8.5 6.0	15 11	1.0 1.0	16 12	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	3.0 2.0	8.5 6.0	14.5 10.5	1.0 1.0	16 11.5	ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	4.0 3.0	10.5 7.5	18 12	1.0 1.0	20 14	ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	4.5 3.0	10.5 7.5	17.5 12.5	1.0 1.0	19 13.5	ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{RC}$	3.3 5.0	3.0 2.5	7.5 5.5	12 9.5	1.0 1.0	13.5 10.5	ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{RC}$	3.3 5.0	2.5 2.0	7.0 5.0	11.5 8.5	1.0 1.0	12.5 9.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0	2.5 1.5	7.0 5.0	12 8.5	1.0 1.0	13.5 9.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0	2.5 1.5	6.5 5.0	11 8.0	1.0 1.0	12.5 9.0	ns	3-6
t_{PLH}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	3.3 5.0	2.5 1.5	6.5 5.0	12.5 9.0	1.0 1.0	14.5 10	ns	3-6
t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	3.3 5.0	2.5 1.5	7.0 5.0	12 8.5	1.0 1.0	13.5 10	ns	3-6
t_{PLH}	Propagation Delay $\overline{U}$/D to TC	3.3 5.0	2.5 2.0	7.0 5.0	11.5 8.5	1.0 1.0	13.5 9.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{U}$/D to TC	3.3 5.0	2.5 1.5	6.5 5.0	11 8.5	1.0 1.0	12.5 9.5	ns	3-6
t_{PLH}	Propagation Delay P_n to Q_n	3.3 5.0	3.0 2.0	8.0 5.5	13.5 9.5	1.0 1.0	15.5 10.5	ns	3-6
t_{PHL}	Propagation Delay P_n to Q_n	3.3 5.0	3.0 2.0	7.5 5.5	13 9.5	1.0 1.0	14.5 10.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0	3.5 2.0	9.5 5.5	14.5 9.5	1.0 1.0	17.5 10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0	3.0 2.0	8.0 6.0	13.5 10	10 1.0	15.5 11	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC191 T_A = +25°C, C_L = 50 pF		74AC191 T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	1.0 0.5	3.0 2.0	3.0 2.5	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	−1.5 −0.5	0.5 1.0	1.0 1.0	ns	3-9
t_s	Setup Time, LOW $\overline{CE}$ to CP	3.3 5.0	3.0 1.5	6.0 4.0	7.0 4.5	ns	3-9
t_h	Hold Time, LOW $\overline{CE}$ to CP	3.3 5.0	−4.0 −2.5	−0.5 0	−0.5 0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{U}$/D to CP	3.3 5.0	4.0 2.5	8.0 5.5	9.0 6.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{U}$/D to CP	3.3 5.0	−5.0 −3.0	0 0.5	0 0.5	ns	3-9
t_w	$\overline{PL}$ Pulse Width, LOW	3.3 5.0	2.0 1.0	3.5 1.0	4.0 1.0	ns	3-6
t_w	CP Pulse Width, LOW	3.3 5.0	2.0 2.0	3.5 3.0	4.0 4.0	ns	3-6
t_{rec}	Recovery Time $\overline{PL}$ to CP	3.3 5.0	−0.5 −1.0	0 0	0 0	ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	75	pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC192
MC74AC193

Product Preview

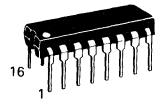
Up/Down Counters with Separate Up/Down Clocks

UP/DOWN COUNTERS WITH SEPARATE UP/DOWN CLOCKS

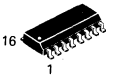
The MC74AC192 is an up/down BCD decade (8421) counter. The MC74AC193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided that are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

- High-Speed — 120 MHz Typical Count Frequency
- Synchronous Counting
- Asynchronous Parallel Load and Master Reset
- Outputs Source/Sink 24 mA

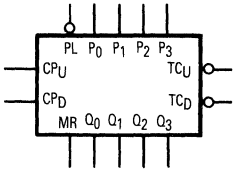


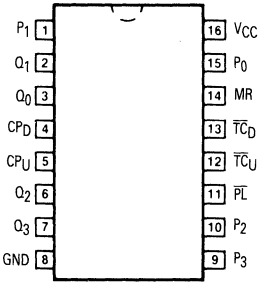
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





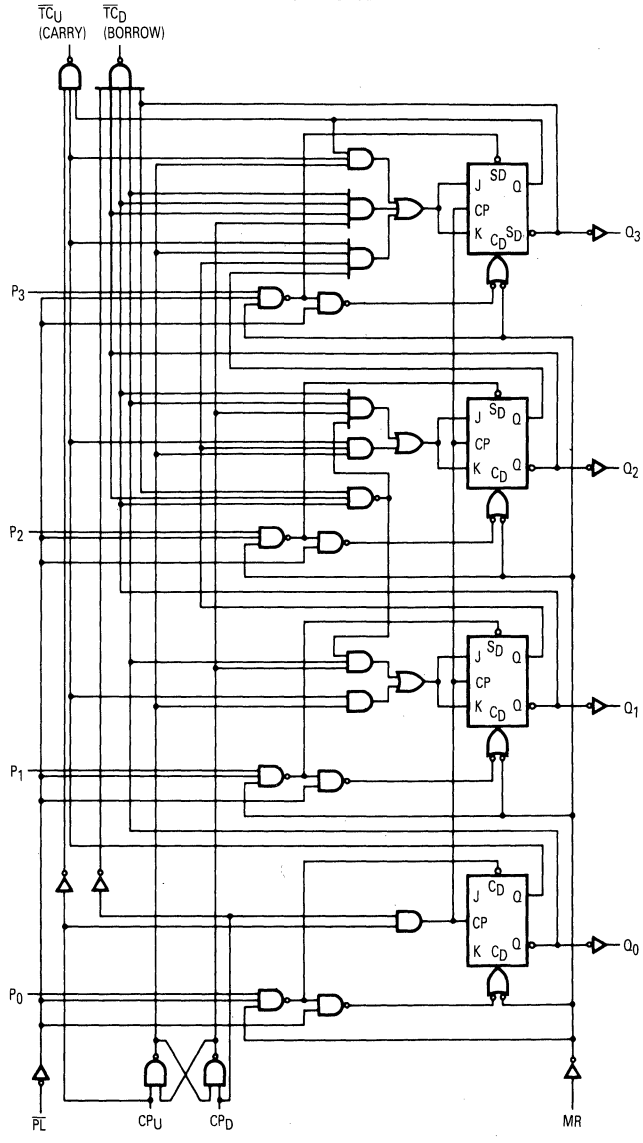
PIN NAMES

CP_U	Count Up Clock Input
CP_D	Count Down Clock Input
MR	Asynchronous Master Reset Input
$\overline{PL}$	Asynchronous Parallel Load Input
P_0–P_3	Parallel Data Inputs
Q_0–Q_3	Flip-Flop Outputs
$\overline{TC_D}$	Terminal Count Down (Borrow) Output
$\overline{TC_U}$	Terminal Count Up (Carry) Output

5

LOGIC DIAGRAM

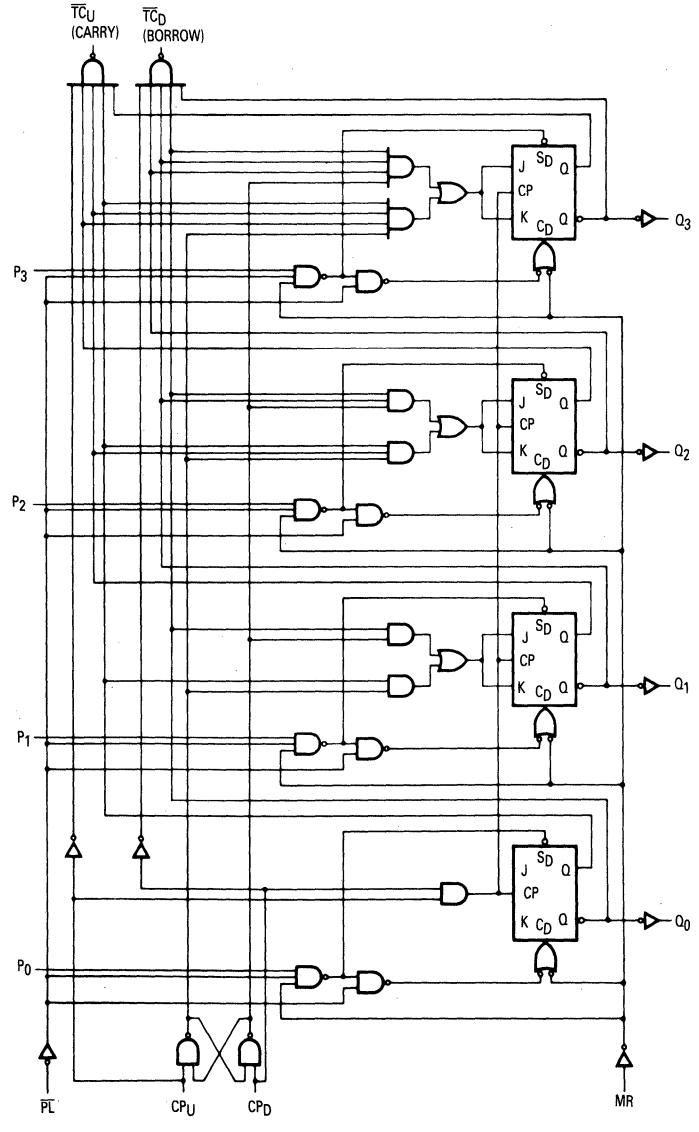
MC74AC192



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

LOGIC DIAGRAM

MC74AC193



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The MC74AC192/74AC193 are asynchronously presettable counters. The MC74AC192 is a decade counter while the MC74AC193 is organized for 4-bit binary operation. They both contain four edge-triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state, 9 (MC74AC192) or 15 (MC74AC193), the reset HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot \overline{CP}_U \text{ ('AC192)}$$
$$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U \text{ ('AC193)}$$
$$\overline{TC}_U = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

Both the MC74AC192 and the MC74AC193 have an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input (P_0–P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

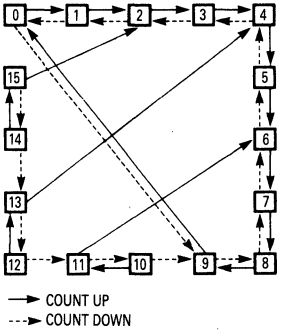
FUNCTION TABLE

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H		H	Count Up
L	H	H		Count Down

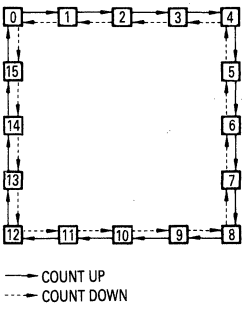
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
= LOW-to-HIGH Transition

STATE DIAGRAMS

MC74AC192



MC74AC193



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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		88 120				MHz	3-3
t_{PLH}	Propagation Delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		15 11				ns	3-6
t_{PHL}	Propagation Delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		13 9.5				ns	3-6
t_{PLH}	Propagation Delay CP_U or CP_D to Q_n	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP_U or CP_D to Q_n	3.3 5.0		10.5 7.5				ns	3-6
t_{PLH}	Propagation Delay P_n to Q_n	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay P_n to Q_n	3.3 5.0		9.5 7.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0		12.5 9.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0		11 8.0				ns	3-6
t_{PLH}	Propagation Delay MR to Q_n	3.3 5.0		12.5 9.0				ns	3-6
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$	3.3 5.0		12.5 9.0				ns	3-6
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$	3.3 5.0		11 8.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		11.5 8.5				ns	3-6
t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		9.5 7.0				ns	3-6
t_{PLH}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		11.5 8.5				ns	3-6
t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		11.5 8.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	−0.5 −0.5			ns	3-9
t_w	$\overline{PL}$ Pulse Width, LOW	3.3 5.0	8.5 6.0			ns	3-6
t_w	CP_U or CP_D Pulse Width, LOW	3.3 5.0	5.5 4.0			ns	3-6
t_w	CP_U or CP_D Pulse Width, LOW (Change of Direction)	3.3 5.0	9.0 6.5			ns	3-6
t_w	MR Pulse Width, HIGH	3.3 5.0	7.0 5.0			ns	3-6
t_{rec}	Recovery Time $\overline{PL}$ to CP_U or CP_D	3.3 5.0	4.5 3.0			ns	3-9
t_{rec}	Recovery Time MR to CP_U or CP_D	3.3 5.0	8.5 6.0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC240
MC74ACT240

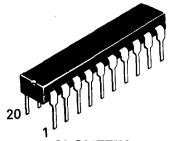
Product Preview

Octal Buffer/Line Driver with 3-State Outputs

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

The MC74AC240/74ACT240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- 'ACT240 Has TTL Compatible Inputs



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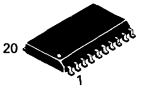


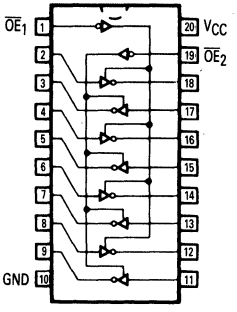
DW SUFFIX
CASE 751D-03
PLASTIC

TRUTH TABLES

Inputs		Outputs
$\overline{OE}_1$	D	(Pins 12, 14, 16, 18)
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	D	(Pins 3, 5, 7, 9)
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance



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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT240)	1.5	mA	V_{IN} = V_{CC} − 2.1 V, V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.0 4.5	8.0 6.5	1.0 1.0	9.0 7.0	ns	3-5
t_{PHL}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	5.5 4.5	8.0 6.0	1.0 1.0	8.5 6.5	ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	6.0 5.0	10.5 7.0	1.0 1.0	11 8.0	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	7.0 5.5	10 8.0	1.0 1.0	11 8.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.0 6.5	10 9.0	1.0 1.0	10.5 9.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.5 6.5	10.5 9.0	1.0 1.0	11.5 9.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	1.0	6.0	8.5	1.0	9.5	ns	3-5
t_{PHL}	Propagation Delay Data to Output	5.0	1.0	5.5	7.5	1.0	8.5	ns	3-5
t_{PZH}	Output Enable Time	5.0	1.0	7.0	8.5	1.0	9.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	7.0	9.5	1.0	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	8.0	9.5	1.0	10.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	6.5	10	1.0	10.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC241
MC74ACT241

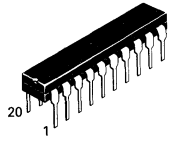
Product Preview

Octal Buffer/Line Driver with 3-State Outputs

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

The MC74AC241/74ACT241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- 'ACT241 Has TTL Compatible Inputs



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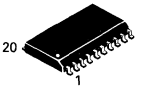


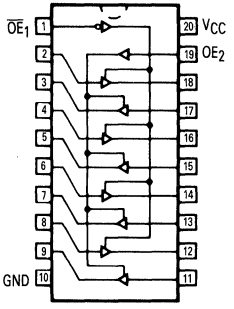
DW SUFFIX
CASE 751D-03
PLASTIC

TRUTH TABLES

Inputs		Outputs
$\overline{OE}_1$	D	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
OE_2	D	(Pins 3, 5, 7, 9)
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance



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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT241)	1.5	mA	V_{IN} = V_{CC} – 2.1 V, V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.0 5.0	9.0 7.0	1.0 1.0	10 7.5	ns	3-5
t_{PHL}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.0 4.5	9.0 7.0	1.0 1.0	10.5 7.5	ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	6.5 5.5	12.5 9.0	1.0 1.0	13 9.5	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	7.0 5.5	12 9.0	1.0 1.0	13 9.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	8.0 6.5	12 10	1.0 1.0	12.5 10.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.0 6.0	12.5 10	1.0 1.0	13.5 10.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	1.0	6.5	9.0	1.0	10	ns	3-5
t_{PHL}	Propagation Delay Data to Output	5.0	1.0	7.0	9.0	1.0	10	ns	3-5
t_{PZH}	Output Enable Time	5.0	1.0	6.0	9.0	1.0	10	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	7.0	10	1.0	11	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	8.0	10.5	1.0	11.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	7.0	10.5	1.0	11.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC244
MC74ACT244

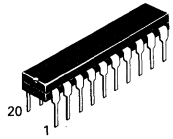
Product Preview

Octal Buffer/Line Driver with 3-State Outputs

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

The MC74AC244/74ACT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- 'ACT244 Has TTL Compatible Inputs



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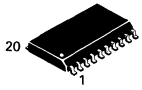


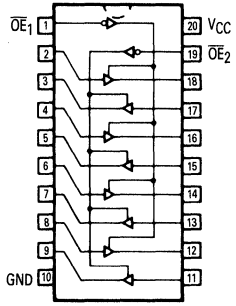
DW SUFFIX
CASE 751D-03
PLASTIC

TRUTH TABLES

Inputs		Outputs
$\overline{OE}_1$	D	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	D	(Pins 3, 5, 7, 9)
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance



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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT244)	1.5	mA	V_{IN} = V_{CC} − 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.5 5.0	9.0 7.0	1.0 1.0	10 7.5	ns	3-5
t_{PHL}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.5 5.0	9.0 7.0	1.0 1.0	10 7.5	ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	6.0 5.0	10.5 7.0	1.0 1.0	11 8.0	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	7.5 5.5	10 8.0	1.0 1.0	11 8.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.0 6.5	10 9	1.0 1.0	10.5 9.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.5 6.5	10.5 9.0	1.0 1.0	11.5 9.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	1.0	6.5	9.0	1.0	10	ns	3-5
t_{PHL}	Propagation Delay Data to Output	5.0	1.0	7.0	9.0	1.0	10	ns	3-5
t_{PZH}	Output Enable Time	5.0	1.0	6.0	8.5	1.0	9.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	7.0	9.5	1.0	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	9.5	1.0	10.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	7.5	10	1.0	10.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC245
MC74ACT245

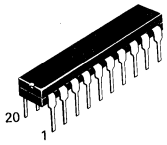
Product Preview

Octal Bidirectional Transceiver with 3-State Inputs/Outputs

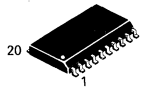
OCTAL BIDIRECTIONAL TRANSCEIVER WITH 3-STATE INPUTS/OUTPUTS

The MC74AC245/74ACT245 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a High Z condition.

- Noninverting Buffers
- Bidirectional Data Path
- A and B Outputs Source/Sink 24 mA
- 'ACT245 Has TTL Compatible Inputs



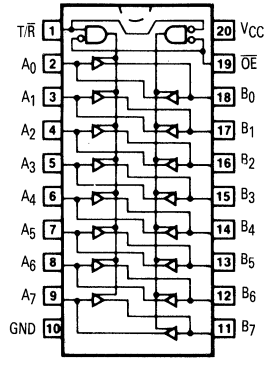
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

PIN NAMES

$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0–A_7	Side A 3-State Inputs or 3-State Outputs
B_0–B_7	Side B 3-State Inputs or 3-State Outputs



TRUTH TABLES

Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT245)	1.5	mA	V_{IN} = V_{CC} − 2.1 V, V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	3.3 5.0	1.0 1.0	5.0 3.5	8.5 6.5	1.0 1.0	9.0 7.0	ns	3-5
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	3.3 5.0	1.0 1.0	5.0 3.5	8.5 6.0	1.0 1.0	9.0 7.0	ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	7.0 5.0	11.5 8.5	1.0 1.0	12.5 9.0	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	7.5 5.5	12 9.0	1.0 1.0	13.5 9.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	6.5 5.5	12 9.0	1.0 1.0	12.5 10	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.0 5.5	11.5 9.0	1.0 1.0	13 10	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	5.0	1.0	4.0	7.5	1.0	8.0	ns	3-5
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	5.0	1.0	4.0	8.0	1.0	9.0	ns	3-5
t_{PZH}	Output Enable Time	5.0	1.0	5.0	10	1.0	11	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.5	10	1.0	12	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	5.5	10	1.0	11	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	5.0	10	1.0	11	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
$C_{I/O}$	Input/Output Capacitance	15	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	45	pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC251
MC74ACT251

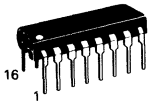
Product Preview

8-Input Multiplexer with 3-State Outputs

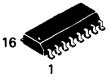
8-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The MC74AC251/74ACT251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

- Multifunctional Capability
- On-Chip Select Logic Decoding
- Inverting and Noninverting 3-State Outputs
- Outputs Source/Sink 24 mA
- 'ACT251 Has TTL Compatible Inputs

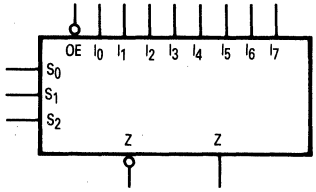


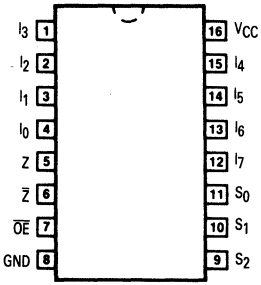
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

S_0–S_2	Select Inputs
$\overline{OE}$	3-State Output Enable Input
I_0–I_7	Multiplexer Inputs
Z	3-State Multiplexer Output
$\overline{Z}$	Complementary 3-State Multiplexer Output

TRUTH TABLE

Inputs				Outputs	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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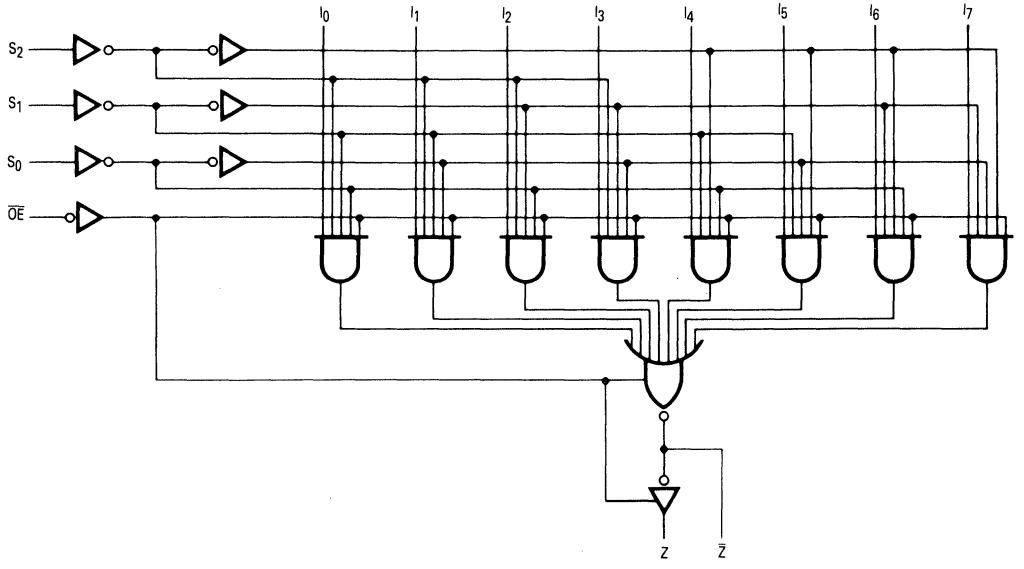
FUNCTIONAL DESCRIPTION

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active-LOW portion of the enable voltages.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT251)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	3.3 5.0	1.0 1.0	11.5 8.5	17.5 12.5	1.0 1.0	19 13.5	ns	3-6
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	3.3 5.0	1.0 1.0	11 8.0	17.5 12.5	1.0 1.0	19 13.5	ns	3-6
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	3.3 5.0	1.0 1.0	10 7.0	14 10	1.0 1.0	15.5 11	ns	3-5
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	3.3 5.0	1.0 1.0	9.0 6.5	14 10	1.0 1.0	15.5 11	ns	3-5
t_{PZH}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3 5.0	1.0 1.0	7.5 5.5	11 8.0	1.0 1.0	12 9.0	ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3 5.0	1.0 1.0	7.5 5.5	11 8.0	1.0 1.0	12 9.0	ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3 5.0	3.5 2.5	8.5 7.0	11.5 9.5	3.5 2.5	13 10	ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3 5.0	4.0 3.0	7.0 5.5	11 8.0	4.0 3.0	12 8.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	5.0	1.0	7.0	13.5	1.0	13	ns	3-6
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	5.0	1.0	7.5	13	1.0	14.5	ns	3-6
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	5.0	1.0	5.5	10	1.0	10.5	ns	3-5
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	5.0	1.0	6.5	10.5	1.0	12	ns	3-5
t_{PZH}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.0	5.0	9.0	1.0	9.0	ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.0	4.5	9.0	1.0	8.5	ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.0	6.0	10.5	1.0	10	ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.0	4.5	9.0	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	70	pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC253
MC74ACT253

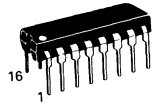
Product Preview

Dual 4-Input Multiplexer with 3-State Outputs

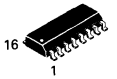
DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The MC74AC253/74ACT253 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

- Multifunctional Capability
- Noninverting 3-State Outputs
- Outputs Source/Sink 24 mA
- 'ACT253 Has TTL Compatible Inputs

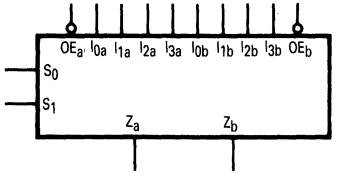


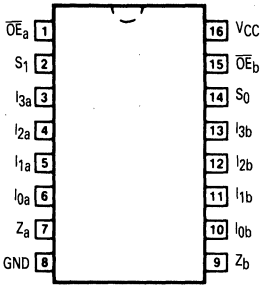
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
Z_a, Z_b	3-State Outputs

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TRUTH TABLE

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S_0 and S_1 are common to both sections.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

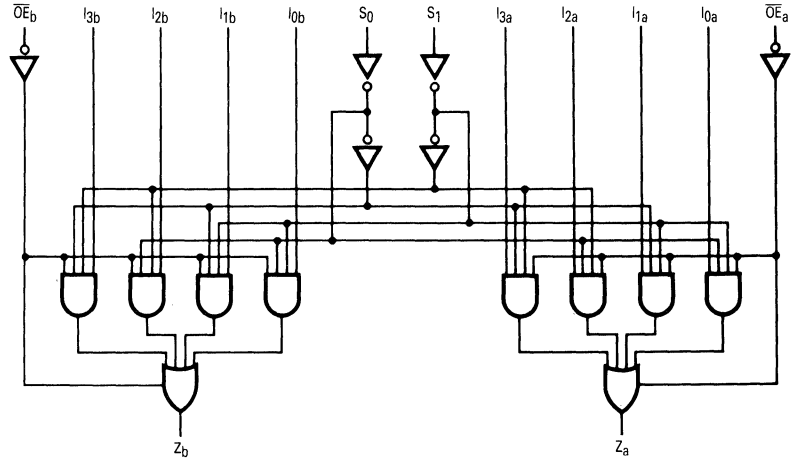
The MC74AC253/74ACT253 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT253)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	3.3 5.0	1.0 1.0	8.5 6.5	15.5 11	1.0 1.0	17.5 12.5	ns	3-6
t_{PHL}	Propagation Delay S_n to Z_n	3.3 5.0	1.0 1.0	9.5 7.0	16 11.5	1.0 1.0	18 13	ns	3-6
t_{PLH}	Propagation Delay I_n to Z_n	3.3 5.0	1.0 1.0	7.0 5.5	14.5 10	1.0 1.0	17 11.5	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	3.3 5.0	1.0 1.0	7.5 5.5	13 9.5	1.0 1.0	15 11	ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	4.5 3.5	8.0 6.0	1.0 1.0	8.5 6.5	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	5.0 3.5	8.0 6.0	1.0 1.0	9.0 7.0	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	5.5 5.0	9.5 8.0	1.0 1.0	10 8.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	5.0 4.0	8.0 7.0	1.0 1.0	9.0 7.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	5.0	1.0	7.0	11.5	1.0	13	ns	3-6
t_{PHL}	Propagation Delay S_n to Z_n	5.0	1.0	7.5	13	1.0	14.5	ns	3-6
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.0	5.5	10	1.0	11	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.0	6.5	11	1.0	12.5	ns	3-5
t_{PZH}	Output Enable Time	5.0	1.0	4.5	7.5	1.0	8.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.0	8.0	1.0	9.0	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	6.0	9.5	1.0	10	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	4.5	7.5	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC257
MC74ACT257

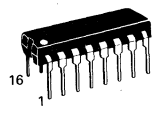
Product Preview

Quad 2-Input Multiplexer with 3-State Outputs

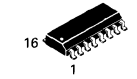
QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The MC74AC257/74ACT257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

- Multiplexer Expansion by Tying Outputs Together
- Noninverting 3-State Outputs
- Outputs Source/Sink 24 mA
- 'ACT257 Has TTL Compatible Inputs

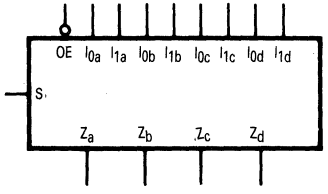


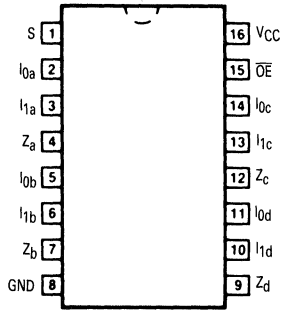
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

S	Common Data Select Input
$\overline{OE}$	3-State Output Enable Input
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
Z_a–Z_d	3-State Multiplexer Outputs

TRUTH TABLE

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

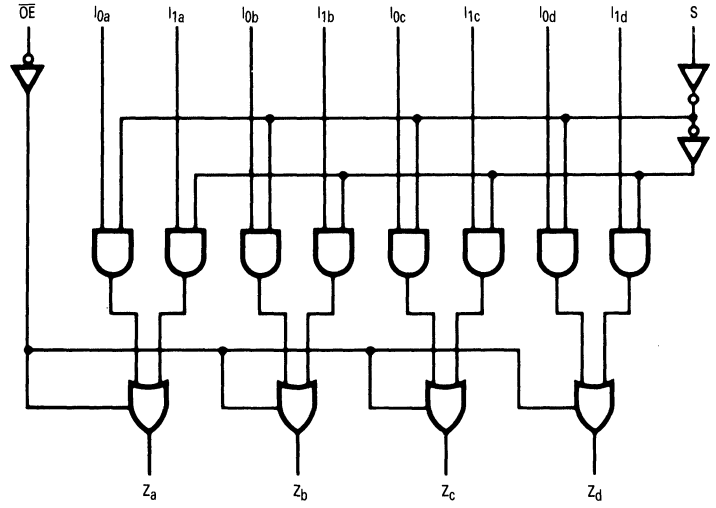
FUNCTIONAL DESCRIPTION

The MC74AC257/74ACT257 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$Z_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$
$Z_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$
$Z_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$
$Z_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT257)	1.5	mA	V_{IN} = V_{CC} − 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to Z_n	3.3 5.0		5.0 4.0				ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	3.3 5.0		6.0 4.5				ns	3-5
t_{PLH}	Propagation Delay S to Z_n	3.3 5.0		7.0 5.0				ns	3-6
t_{PHL}	Propagation Delay S to Z_n	3.3 5.0		7.5 5.5				ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		6.5 5.0				ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		5.5 5.0				ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		5.5 5.0				ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.5 5.0				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.0	5.0	7.0	1.0	7.5	ns	3-6
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.0	6.0	7.5	1.0	8.5	ns	3-6
t_{PLH}	Propagation Delay S to Z_n	5.0	1.0	7.0	9.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay S to Z_n	5.0	1.0	7.0	10.5	1.0	11.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	6.0	8.0	1.0	9.0	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	6.0	8.0	1.0	9.0	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	6.5	9.0	1.0	10	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	6.0	7.5	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC258
MC74ACT258

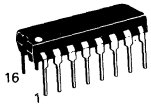
Product Preview

Quad 2-Input Multiplexer with 3-State Outputs

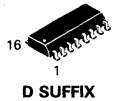
QUAD 2-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The MC74AC258/74ACT258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

- Multiplexer Expansion by Tying Outputs Together
- Inverting 3-State Outputs
- Outputs Source/Sink 24 mA
- 'ACT258 Has TTL Compatible Inputs

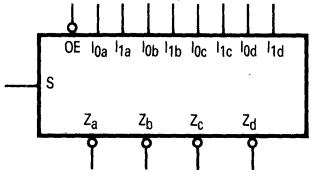


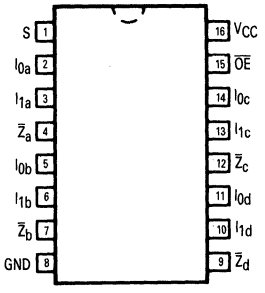
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

$\overline{S}$	Common Data Select Input
$\overline{OE}$	3-State Output Enable Input
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
$\overline{Z}_a$–$\overline{Z}_d$	3-State Multiplexer Outputs

TRUTH TABLE

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

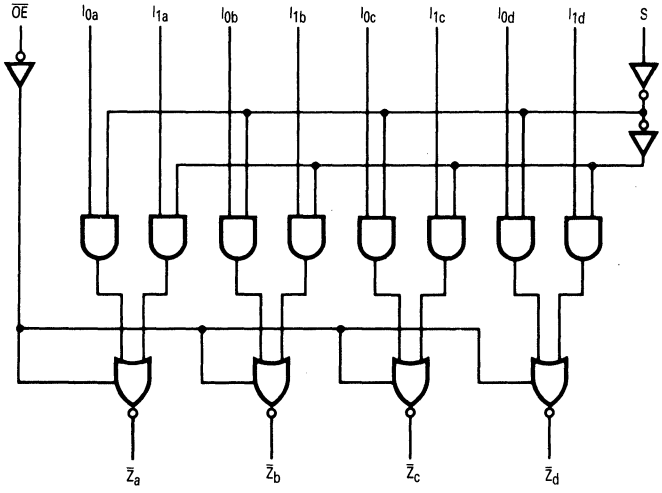
FUNCTIONAL DESCRIPTION

The MC74AC258/74ACT258 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The MC74AC258/74ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$\overline{Z}_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$
$\overline{Z}_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$
$\overline{Z}_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$
$\overline{Z}_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$

When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT258)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0	1.0 1.0	6.0 4.5	9.5 7.5	1.0 1.0	11 8.5	ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0	1.0 1.0	5.0 4.0	8.5 6.5	1.0 1.0	9.5 7.0	ns	3-5
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	3.3 5.0	1.0 1.0	7.5 6.0	12 9.5	1.0 1.0	14 10.5	ns	3-6
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	3.3 5.0	1.0 1.0	7.5 5.5	11.5 9.0	1.0 1.0	13 10	ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	6.0 4.5	9.5 7.5	1.0 1.0	10.5 8.5	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	5.5 5.5	9.0 7.0	1.0 1.0	10 8.0	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	5.5 5.5	10 8.5	1.0 1.0	11.5 9.0	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	5.5 5.0	9.0 7.0	1.0 1.0	10 8.0	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.0	6.5	8.5	1.0	9.5	ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.0	5.5	7.5	1.0	8.0	ns	3-5
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	5.0	1.0	7.5	10.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	5.0	1.0	7.0	9.5	1.0	11	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	6.5	8.5	1.0	9.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	6.5	8.5	1.0	9.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	9.0	1.0	10	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	6.0	8.0	1.0	9.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	55	pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC273
MC74ACT273

Product Preview

Octal D Flip-Flop

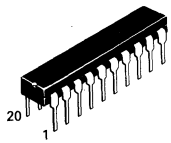
OCTAL D FLIP-FLOP

The MC74AC273/74ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

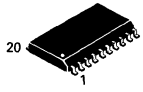
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

- Ideal Buffer for MOS Microprocessor or Memory
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Buffered, Asynchronous Master Reset
- See MC74AC377 for Clock Enable Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC374 for 3-State Version
- Outputs Source/Sink 24 mA
- 'ACT273 Has TTL Compatible Inputs

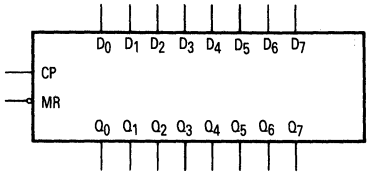


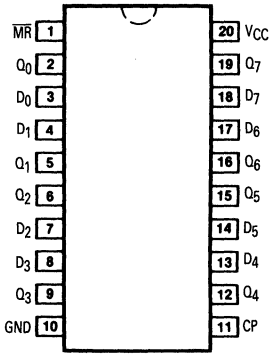
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

$\overline{D_0}$–D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0–Q_7	Data Outputs

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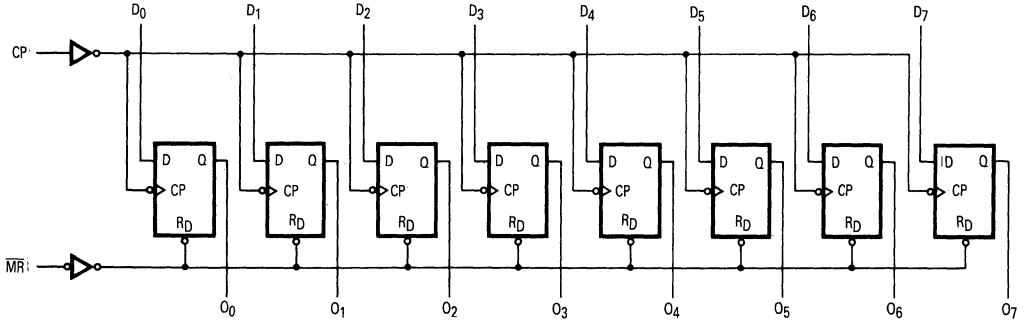
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	D_n	Q_n
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT273)	1.5	mA	V_{IN} = V_{CC} − 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	90 140	125 175		75 125		MHz	3-3
t_{PLH}	Propagation Delay Clock to Output	3.3 5.0	1.0 1.0	7.0 5.5	12.5 9.0	1.0 1.0	14 10	ns	3-6
t_{PHL}	Propagation Delay Clock to Output	3.3 5.0	1.0 1.0	7.0 5.0	13 10	1.0 1.0	14.5 11	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Output	3.3 5.0	1.0 1.0	7.0 5.0	13 10	1.0 1.0	14 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW Data to CP	3.3 5.0	3.5 2.5	5.5 4.0	6.0 4.5	ns	3-9
t_h	Hold Time, HIGH or LOW Data to CP	3.3 5.0	−2.0 −1.0	0 1.0	0 1.0	ns	3-9
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.5 4.0	6.0 4.5	ns	3-6
t_w	$\overline{MR}$ Pulse Width HIGH or LOW	3.3 5.0	2.0 1.5	5.5 4.0	6.0 4.5	ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	1.5 1.0	3.5 2.0	4.5 3.0	ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		200				MHz	3-3
t_{PLH}	Propagation Delay Clock to Output	5.0		6.0				ns	3-6
t_{PHL}	Propagation Delay Clock to Output	5.0		6.5				ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Output	5.0		7.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW Data to CP	5.0	3.0			ns	3-9
t_h	Hold Time, HIGH or LOW Data to CP	5.0	−2.5			ns	3-9
t_w	Clock Pulse Width HIGH or LOW	5.0	2.5			ns	3-6
t_w	$\overline{MR}$ Pulse Width HIGH or LOW	5.0	2.5			ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	−1.0			ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC299
MC74ACT299

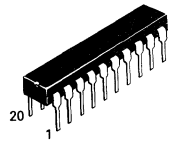
Product Preview

8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

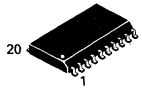
8-INPUT UNIVERSAL SHIFT/STORAGE REGISTER WITH COMMON PARALLEL I/O PINS

The MC74AC299/74ACT299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0, Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

- Common Parallel I/O for Reduced Pin Count
- Additional Serial Inputs and Outputs for Expansion
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- 'ACT299 Has TTL Compatible Inputs

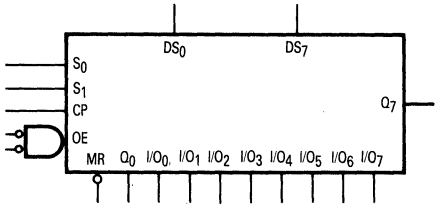


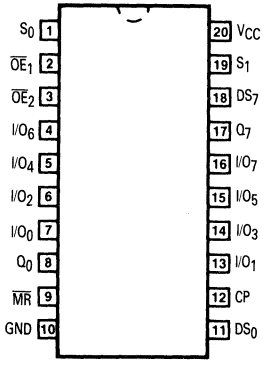
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs
I/O_0–I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
Q_0, Q_7	Serial Outputs

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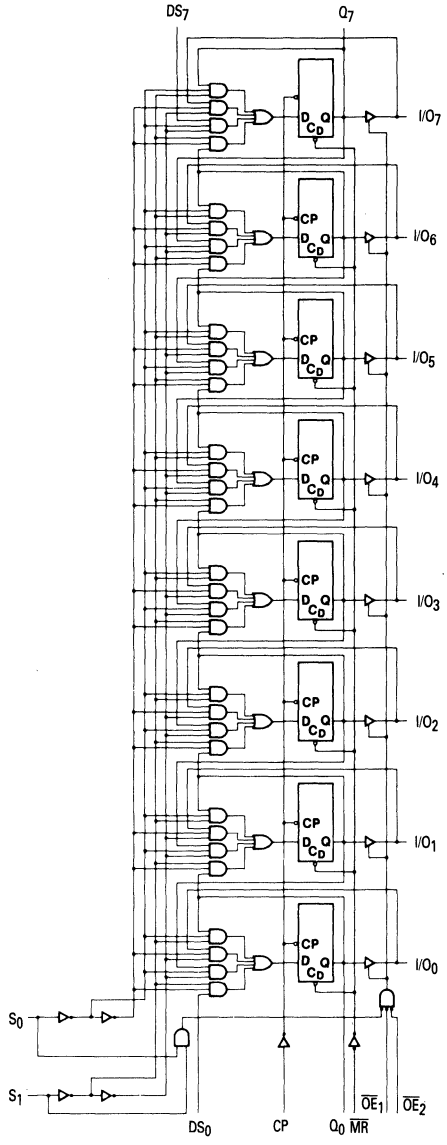
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The MC74AC299/74ACT299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Truth Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

TRUTH TABLE

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	⎍	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⎍	Shift Rights; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⎍	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⎍ = LOW-to-HIGH Transition

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT299)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, V_{CC} = 5.5 V, T_A = Worst Case

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Input Frequency	3.3 5.0		55 130				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	3.3 5.0		31 12				ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	3.3 5.0		30 13				ns	3-6
t_{PLH}	Propagation Delay CP to I/O_n	3.3 5.0		28 11				ns	3-6
t_{PHL}	Propagation Delay CP to I/O_n	3.3 5.0		28 12				ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to I/O_n	3.3 5.0		33 14				ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	3.3 5.0		31 13				ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	3.3 5.0		24 10				ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	3.3 5.0		24 10				ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	3.3 5.0		25 13				ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	3.3 5.0		24 12				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF		74AC T_A = −40°C to +85°C C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	12 5.0			ns	3-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	0 0			ns	3-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	3.3 5.0	6.0 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	3.3 5.0	0 0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	9.0 4.0			ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	7.0 4.0			ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Input Frequency	5.0		125				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	5.0		11				ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	5.0		12				ns	3-6
t_{PLH}	Propagation Delay CP to I/O_n	5.0		10				ns	3-6
t_{PHL}	Propagation Delay CP to I/O_n	5.0		12				ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.0		14				ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.0		13				ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	5.0		10				ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	5.0		10				ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	5.0		12				ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	5.0		11				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	5.0			ns	3-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	0			ns	3-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	5.0	3.0			ns	3-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	5.0	0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	4.0			ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	4.0			ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0			ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC323
MC74ACT323

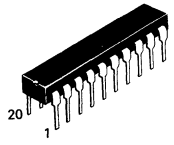
Product Preview

8-Input Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

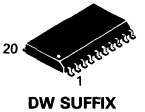
8-INPUT UNIVERSAL SHIFT/STORAGE REGISTER WITH SYNCHRONOUS RESET AND COMMON I/O PINS

The MC74AC323/74ACT323 is an 8-bit universal shift/storage register with 3-state outputs. Its function is similar to the MC74AC299/74ACT299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

- Common Parallel I/O for Reduced Pin Count
- Additional Serial Inputs and Outputs for Expansion
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- 'ACT323 Has TTL Compatible Inputs

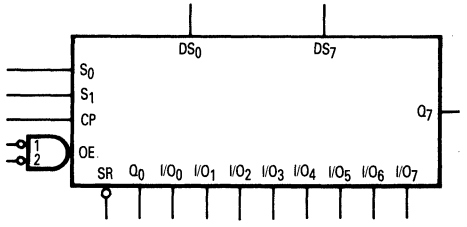


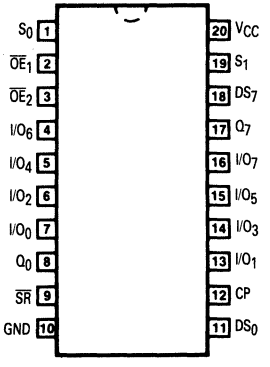
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL



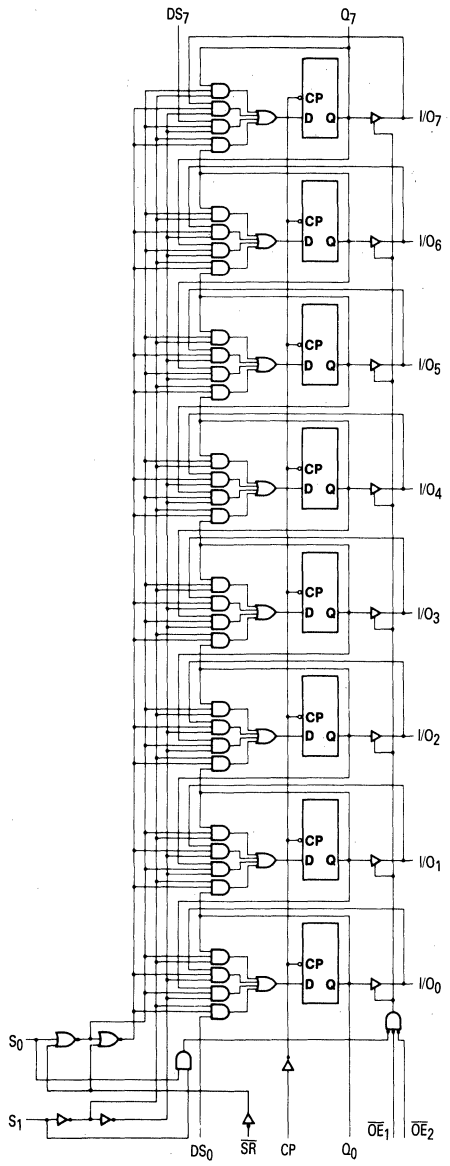


PIN NAMES

CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{SR}$	Synchronous Master Reset
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs
I/O_0–I/O_7	Multipled Parallel Data Inputs or 3-State Parallel Data Outputs
Q_0, Q_7	Serial Outputs

5

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The MC74AC323/74ACT323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

TRUTH TABLE

Inputs				Response
$\overline{SR}$	S_1	S_0	CP	
L	X	X	⎍	Synchronous Reset; Q_0–Q_7 = LOW
H	H	H	⎍	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⎍	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⎍	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⎍ = LOW-to-HIGH Clock Transition

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT323)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, V_{CC} = 5.5 V, T_A = Worst Case

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Input Frequency	3.3 5.0		55 130				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	3.3 5.0		31 12				ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	3.3 5.0		30 13				ns	3-6
t_{PLH}	Propagation Delay CP to I/O_n	3.3 5.0		28 11				ns	3-6
t_{PHL}	Propagation Delay CP to I/O_n	3.3 5.0		28 12				ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		24 10				ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		24 10				ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		25 13				ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		24 12				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	12 5.0			ns	3-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	0 0			ns	3-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	3.3 5.0	5.0 5.0			ns	3-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	3.3 5.0	0 0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	4.0 2.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	0 0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	9.0 4.0			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Input Frequency	5.0		125				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	5.0		12				ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	5.0		13				ns	3-6
t_{PLH}	Propagation Delay CP to I/O_n	5.0		10				ns	3-6
t_{PHL}	Propagation Delay CP to I/O_n	5.0		12				ns	3-6
t_{PZH}	Output Enable Time	5.0		10				ns	3-7
t_{PZL}	Output Enable Time	5.0		10				ns	3-8
t_{PHZ}	Output Disable Time	5.0		12				ns	3-7
t_{PLZ}	Output Disable Time	5.0		11				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF	74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum		
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	5.0		ns	3-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	0		ns	3-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	3.0		ns	3-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	0		ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	2.0		ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	0		ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	4.0		ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC352
MC74ACT352

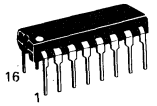
Product Preview

Dual 4-Input Multiplexer

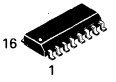
DUAL 4-INPUT MULTIPLEXER

The MC74AC352/74ACT352 is a very high-speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The MC74AC352/74ACT352 is the functional equivalent of the MC74AC353/74ACT353 except with inverted outputs.

- Inverted Version of the MC74AC353/74ACT353
- Separate Enables for Each Multiplexer
- Outputs Source/Sink 24 mA
- 'ACT352 Has TTL Compatible Inputs

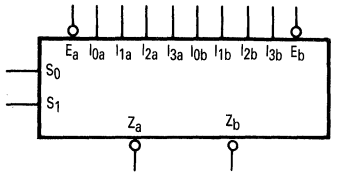


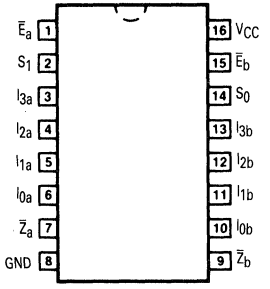
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\bar{E}_a$	Side A Enable Input
$\bar{E}_b$	Side B Enable Input
$\bar{Z}_a$, $\bar{Z}_b$	Multiplexer Outputs

5

TRUTH TABLE

Select Inputs		Inputs (a or b)					Outputs
S_0	S_1	$\bar{E}$	I_0	I_1	I_2	I_3	$\bar{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

FUNCTIONAL DESCRIPTION

The MC74AC352/74ACT352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs ($\overline{Z}_a$, $\overline{Z}_b$) are forced HIGH.

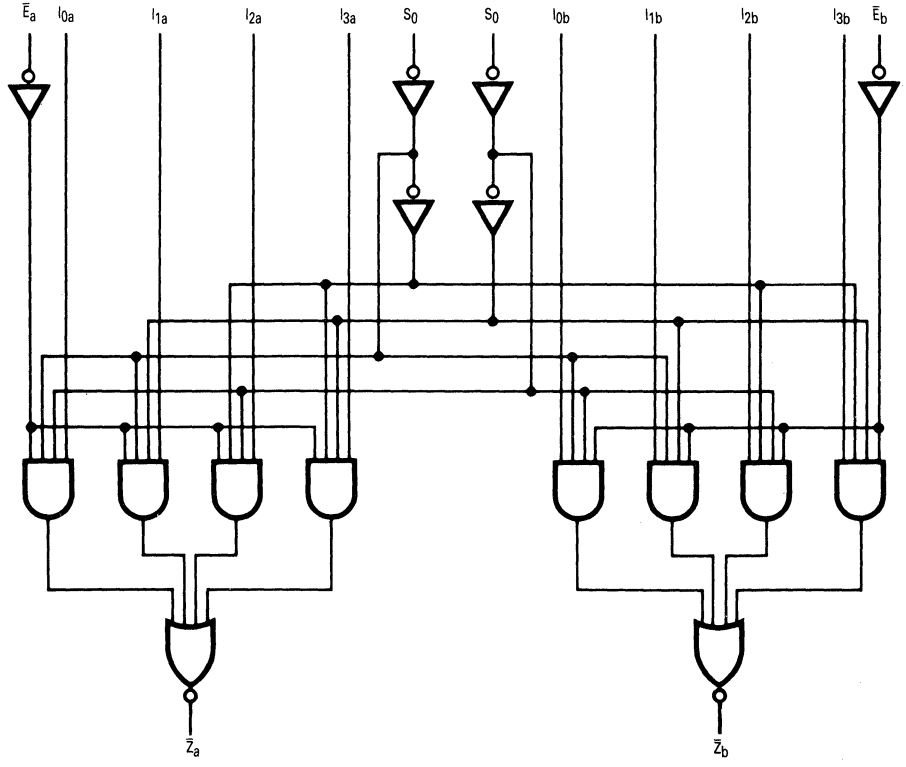
The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\overline{Z}_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The MC74AC352/74ACT352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The MC74AC352/74ACT352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT352)	1.5	mA	V_{IN} = V_{CC} − 2.1 V, V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to $\overline{Z}_n$	3.3 5.0		9.0 6.5				ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	3.3 5.0		9.0 6.5				ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	3.3 5.0		6.5 5.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	3.3 5.0		6.5 5.0				ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0		8.5 6.0				ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0		8.5 6.0				ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to $\overline{Z}_n$	5.0		7.0				ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	5.0		7.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	5.0		5.5				ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	5.0		5.5				ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0		6.5				ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0		6.5				ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC353
MC74ACT353

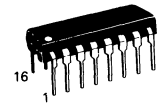
Product Preview

Dual 4-Input Multiplexer with 3-State Outputs

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The MC74AC353/74ACT353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus-oriented systems.

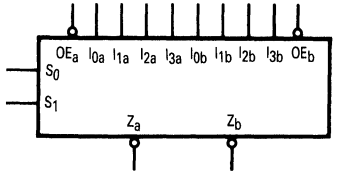
- Inverted Version of the MC74AC253/74ACT253
- Multifunction Capability
- Separate Enables for Each Multiplexer
- Outputs Source/Sink 24 mA
- 'ACT353 Has TTL Compatible Inputs

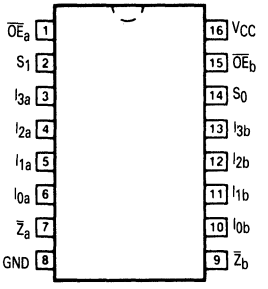


N SUFFIX
CASE 648-08
PLASTIC

D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Enable Input
$\overline{OE}_b$	Side B Enable Input
$\overline{Z}_a$, $\overline{Z}_b$	Multiplexer Outputs

TRUTH TABLE

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs S_0 and S_1 are common to both sections.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

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FUNCTIONAL DESCRIPTION

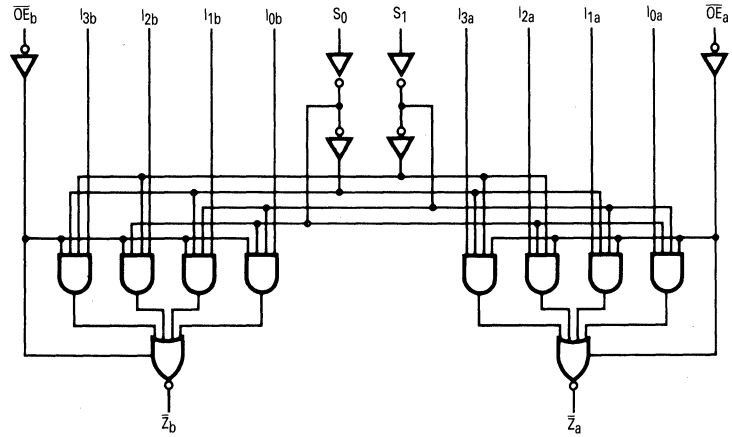
The MC74AC353/74ACT353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\overline{Z}_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT353)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to $\overline{Z}_n$	3.3 5.0		9.0 6.5				ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	3.3 5.0		9.0 6.5				ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0		6.5 5.0				ns	3-6
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0		6.5 5.0				ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		5.5 4.0				ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		6.0 4.5				ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 5.5				ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.5 4.0				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to $\overline{Z}_n$	5.0		7.0				ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	5.0		7.0				ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0		5.5				ns	3-6
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0		5.5				ns	3-6
t_{PZH}	Output Enable Time	5.0		4.5				ns	3-7
t_{PZL}	Output Enable Time	5.0		5.0				ns	3-8
t_{PHZ}	Output Disable Time	5.0		6.0				ns	3-7
t_{PLZ}	Output Disable Time	5.0		4.5				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC373
MC74ACT373

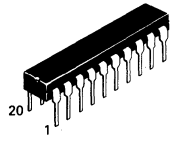
Product Preview

Octal Transparent Latch with 3-State Outputs

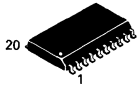
OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

The MC74AC373/74ACT373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- 'ACT373 Has TTL Compatible Inputs

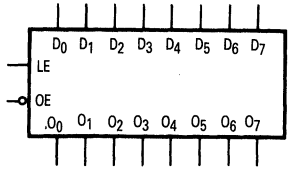


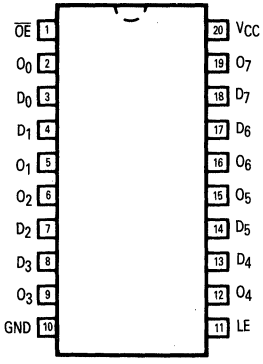
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	3-State Latch Outputs

TRUTH TABLE

Inputs			Outputs
$\overline{OE}$	LE	D_n	O_n
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before LOW-to-HIGH Transition of Clock

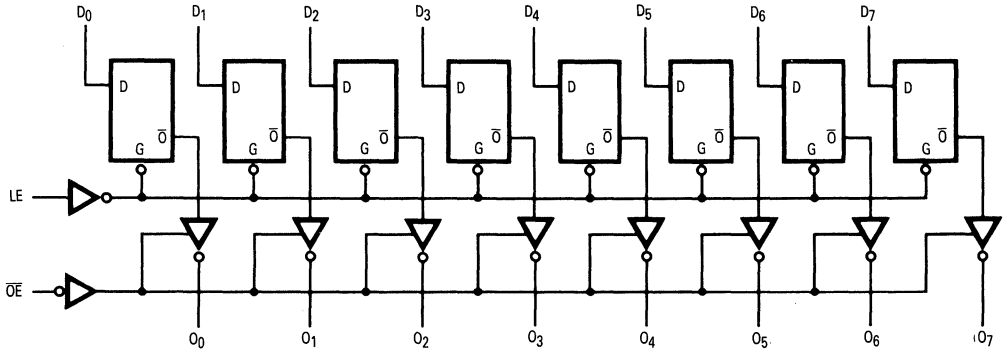
5

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

The MC74AC373/74ACT373 contains eight D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT373)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3 5.0	1.0 1.0	10 7.0	13.5 9.5	1.0 1.0	15 10.5	ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	3.3 5.0	1.0 1.0	9.5 7.0	13 9.5	1.0 1.0	14.5 10.5	ns	3-5
t_{PLH}	Propagation Delay LE to O_n	3.3 5.0	1.0 1.0	10 7.5	13.5 9.5	1.0 1.0	15 10.5	ns	3-6
t_{PHL}	Propagation Delay LE to O_n	3.3 5.0	1.0 1.0	9.5 7.0	12.5 9.5	1.0 1.0	14 10.5	ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	9.0 7.0	11.5 8.5	1.0 1.0	13 9.5	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	8.5 6.5	11.5 8.5	1.0 1.0	13 9.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	10 8.0	12.5 11	1.0 1.0	14.5 12.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	8.0 6.5	11.5 8.5	1.0 1.0	12.5 10	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	3.5 2.0	5.5 4.0	6.0 4.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	−3.0 −1.5	0 0	0 0	ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.0	5.5 4.0	6.0 4.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0	1.0	8.5	10	1.0	11.5	ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	5.0	1.0	8.0	10	1.0	11.5	ns	3-5
t_{PLH}	Propagation Delay LE to O_n	5.0	1.0	8.5	11	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay LE to O_n	5.0	1.0	8.0	10	1.0	11.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	8.0	9.5	1.0	10.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	7.5	9.0	1.0	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	9.0	11	1.0	12.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	7.5	8.5	1.0	10	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	3.0	7.0	8.0	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0	0	1.0	ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.0	7.0	8.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC374
MC74ACT374

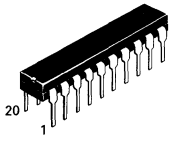
Product Preview

Octal D-Type Flip-Flop with 3-State Outputs

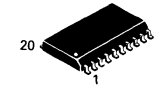
OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

The MC74AC374/74ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- See MC74AC273 for Reset Version
- See MC74AC377 for Clock Enable Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC574 for Broadside Pinout Version
- See MC74AC564 for Broadside Pinout Version with Inverted Outputs
- 'ACT374 Has TTL Compatible Inputs

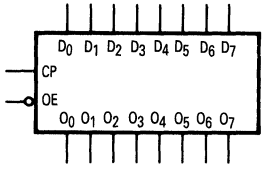


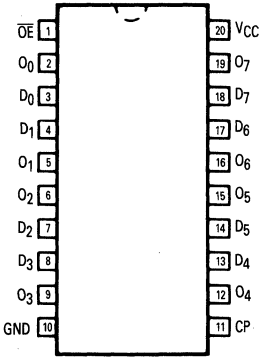
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_7	Data Inputs
$\overline{CP}$	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
O_0–O_7	3-State Outputs

TRUTH TABLE

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

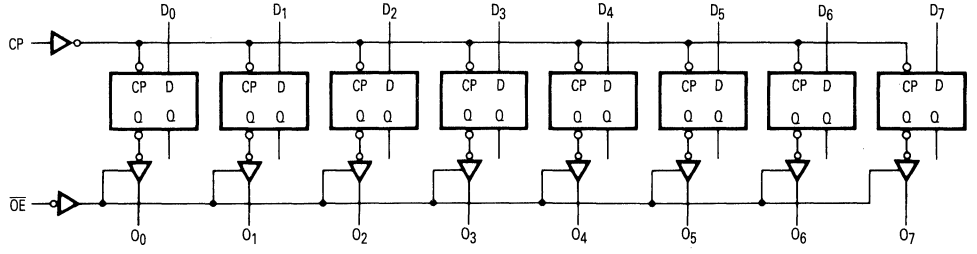
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

The MC74AC374/74ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT374)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	60 100	110 155		60 100		MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0	1.0 1.0	11 8.0	13.5 9.5	1.0 1.0	15.5 10.5	ns	3-6
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0	1.0 1.0	10 7.0	12.5 9.0	1.0 1.0	14 10	ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	9.5 7.0	11.5 8.5	1.0 1.0	13 9.5	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	9.0 6.5	11.5 8.5	1.0 1.0	13 9.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	10.5 8.0	12.5 11	1.0 1.0	14.5 12.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	8.0 6.5	11.5 8.5	1.0 1.0	12.5 10	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0	5.5 4.0	6.0 4.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 0	1.0 1.5	1.0 1.5	ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	4.0 2.5	5.5 4.0	6.0 4.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	100	160		90		MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	5.0	1.0	8.5	10	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay CP to O_n	5.0	1.0	8.0	9.5	1.0	11	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	8.0	9.5	1.0	10.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	8.0	9.0	1.0	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	8.5	11.5	1.0	12.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	7.0	8.5	1.0	10	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0	7.0	8.0	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.5	1.5	ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	7.0	8.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	80	pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC377
MC74ACT377

Product Preview

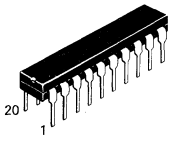
Octal D Flip-Flop with Clock Enable

OCTAL D FLIP-FLOP WITH CLOCK ENABLE

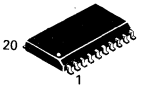
The MC74AC377/74ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

- Ideal for Addressable Register Applications
- Clock Enable for Address and Data Synchronization Applications
- Eight Edge-Triggered D Flip-Flops
- Buffered Common Clock
- Outputs Source/Sink 24 mA
- See MC74AC273 for Master Reset Version
- See MC74AC373 for Transparent Latch Version
- See MC74AC374 for 3-State Version
- 'ACT377 Has TTL Compatible Inputs

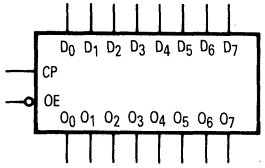


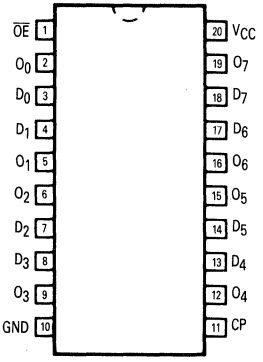
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





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PIN NAMES

D_0–D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0–Q_7	Data Outputs
CP	Clock Pulse Input

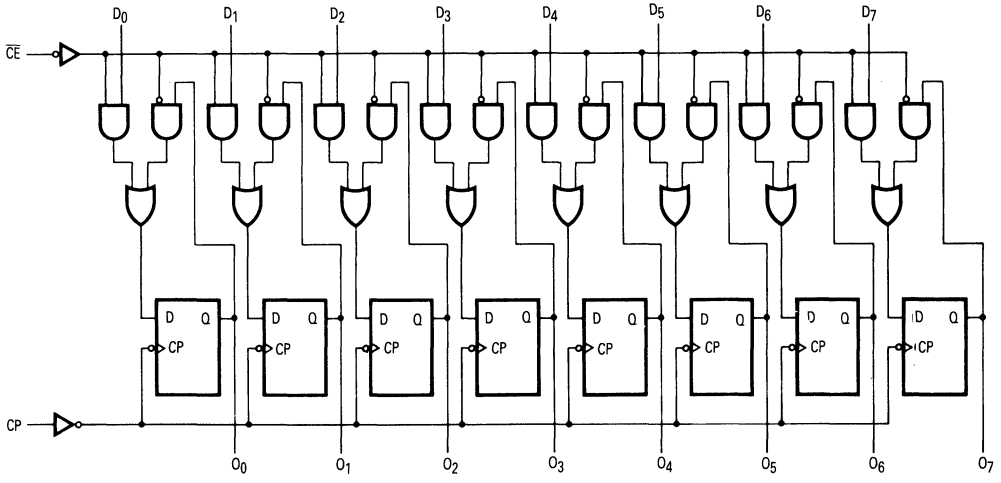
MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D_n	Q_n
Load '1'	⌐	L	H	H
Load '0'	⌐	L	L	L
Hold (Do Nothing)	⌐	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT377)	1.5	mA	V_{IN} = V_{CC} − 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	90 140	125 175		75 125		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	1.0 1.0	8.0 6.0	13 9.0	1.0 1.0	14 10	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	1.0 1.0	8.5 6.5	13 10	1.0 1.0	14.5 11	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	3.5 2.5	5.5 4.0	6.0 4.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−2.0 −1.0	0 1.0	0 1.0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	3.3 5.0	4.0 2.5	6.0 4.0	7.5 4.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	3.3 5.0	−3.5 −2.0	0 1.0	0 1.0	ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.5 4.0	6.0 4.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	140	175		125		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	5.0	1.0	6.5	9.0	1.0	10	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	5.0	1.0	7.0	10	1.0	11	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	2.5	4.5	5.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−1.0	1.0	1.0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	5.0	2.5	4.5	5.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	5.0	−1.0	1.0	1.0	ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	90	pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC378
MC74ACT378

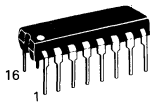
Product Preview

Parallel D Register with Enable

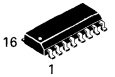
PARALLEL D REGISTER WITH ENABLE

The MC74AC378/74ACT378 is a 6-bit register with a buffered common Enable. This device is similar to the MC74AC174/74ACT174, but with common Enable rather than common Master Reset.

- 6-Bit High-Speed Parallel Register
- Positive Edge-Triggered D-Type Inputs
- Fully Buffered Common Clock and Enable Inputs
- Outputs Source/Sink 24 mA
- 'ACT378 Has TTL Compatible Inputs

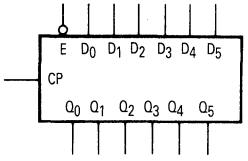


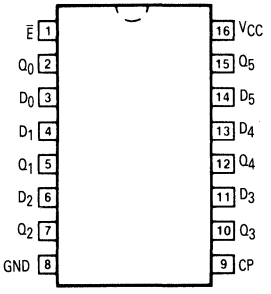
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

$\overline{E}$	Enable Input
D_0–D_5	Data Inputs
CP	Clock Pulse Input
Q_0–Q_5	Outputs

TRUTH TABLE

Inputs			Outputs
$\overline{E}$	CP	D_n	Q_n
H	⎍	X	No Change
L	⎍	H	H
L	⎍	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⎍ = LOW-to-HIGH Transition

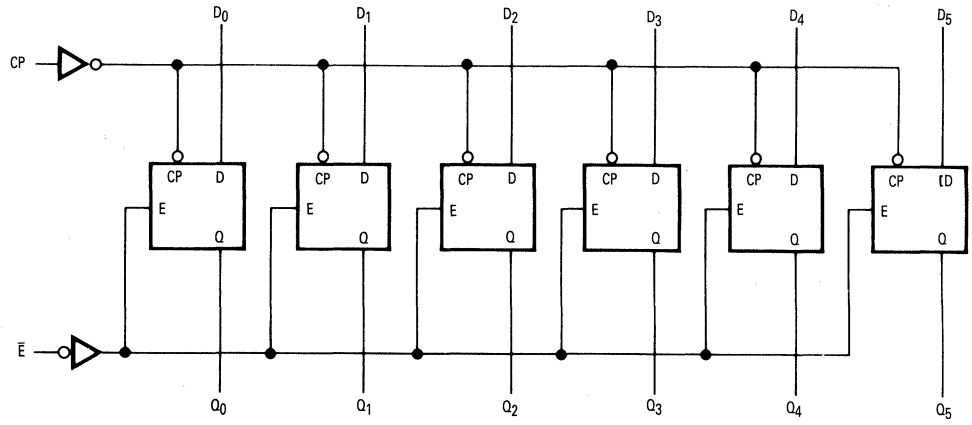
5

FUNCTIONAL DESCRIPTION

The MC74AC378/74ACT378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT378)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		74 100				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0		8.5 6.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0		7.5 5.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	1.5 1.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{E}$ to CP	3.3 5.0	−1.5 −1.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{E}$ to CP	3.3 5.0	0 0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	8.5 6.0			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		100				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	5.0		6.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	5.0		5.5				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	3.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{E}$ to CP	5.0	−1.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{E}$ to CP	5.0	0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	6.0			ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC379
MC74ACT379

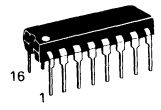
Product Preview

Quad Parallel Register with Enable

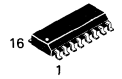
QUAD PARALLEL REGISTER WITH ENABLE

The MC74AC379/74ACT379 is a 4-bit register with a buffered common Enable. This device is similar to the MC74AC175/74ACT175 but features the common Enable rather than common Master Reset.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Buffered Common Enable Input
- True and Complement Outputs
- Outputs Source/Sink 24 mA
- 'ACT379 Has TTL Compatible Inputs

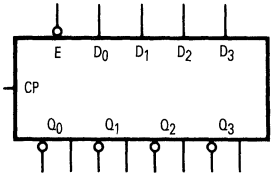


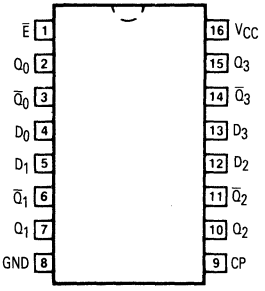
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

$\overline{E}$	Enable Input
D_0–D_3	Data Inputs
CP	Clock Pulse Input
Q_0–Q_3	Flip-Flop Outputs
$\overline{Q}_0$–$\overline{Q}_3$	Complement Outputs

TRUTH TABLE

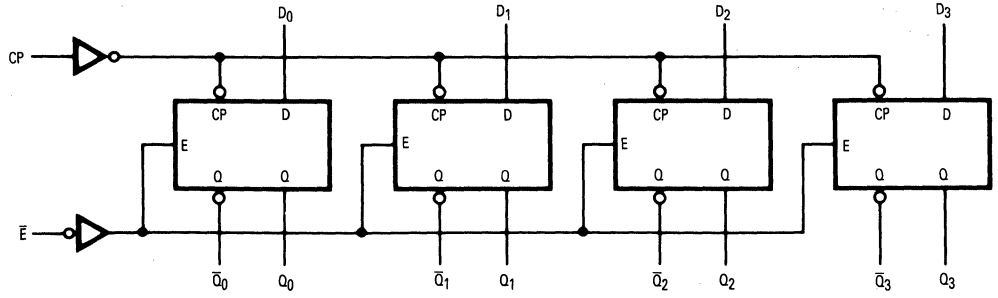
Inputs			Outputs	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	⌐	X	NC	NC
L	⌐	H	H	L
L	⌐	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition
NC = No Change

FUNCTIONAL DESCRIPTION

The MC74AC379/74ACT379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT379)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		118 160				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n, $\overline{Q}_n$	3.3 5.0		8.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	3.3 5.0		8.5 6.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{E}$ to CP	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{E}$ to CP	3.3 5.0	3.0 2.0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	5.5 4.0			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		160				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n, $\overline{Q}_n$	5.0		7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	5.0		6.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF		74ACT T_A = −40°C to +85°C C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	3.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{E}$ to CP	5.0	3.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{E}$ to CP	5.0	2.0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	4.0			ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC398
MC74ACT398
MC74AC399
MC74ACT399

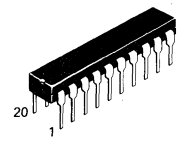
Product Preview

Quad 2-Port Register

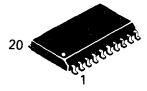
QUAD 2-PORT REGISTER

The MC74AC398/74ACT398 and MC74AC399/74ACT399 are the logical equivalents of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flop on the rising edge of the clock. The MC74AC399/74ACT399 is the 16-pin version of the MC74AC398/74ACT398, with only the Q outputs of the flip-flops available.

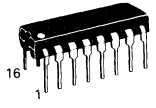
- Select Inputs from Two Data Sources
- Fully Positive Edge-Triggered Operation
- Both True and Complement Outputs — MC74AC398/74ACT398
- Outputs Source/Sink 24 mA
- 'ACT398 and 'ACT399 Have TTL Compatible Inputs



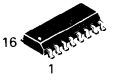
N SUFFIX
CASE 738-03
PLASTIC



N SUFFIX
CASE 648-08
PLASTIC



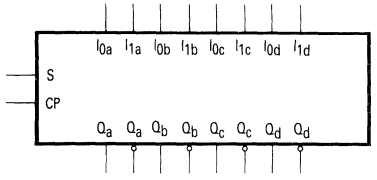
N SUFFIX
CASE 648-06
PLASTIC



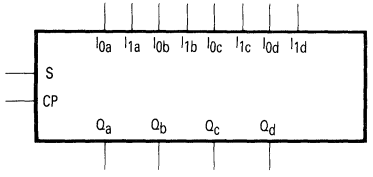
D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL

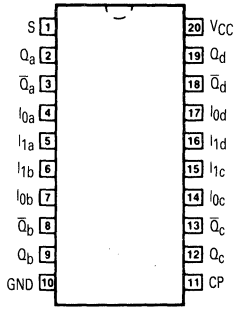
MC74AC398/74ACT398



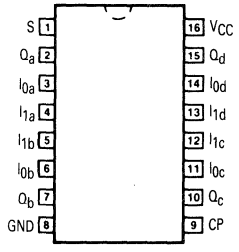
MC74AC399/74ACT399



MC74AC398/74ACT398



MC74AC399/74ACT399



PIN NAMES

S	Common Select Input
CP	Clock Pulse
I_{0a}–I_{0d}	Data Inputs from Source 0
I_{1a}–I_{1d}	Data Inputs from Source 1
Q_a–Q_d	Register True Outputs
$\overline{Q}_a$–$\overline{Q}_d$	Register Complementary Outputs (MC74AC398/74ACT398)

5

FUNCTIONAL DESCRIPTION

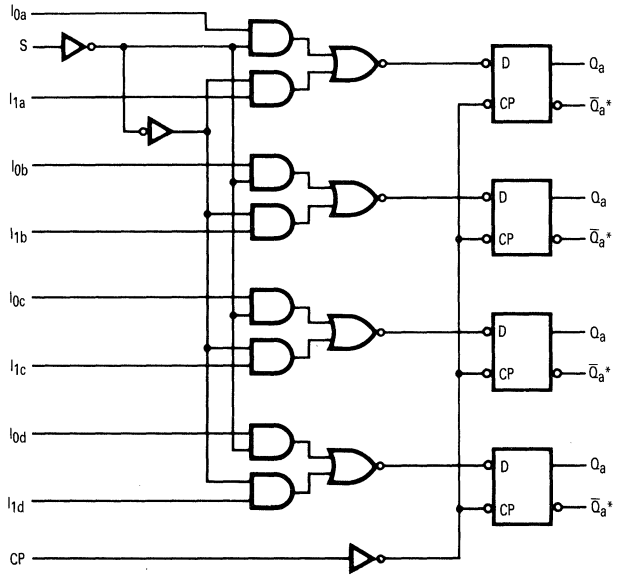
The MC74AC398/74ACT398 and MC74AC399/74ACT399 are high-speed quad 2-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The MC74AC398/74ACT398 has both Q and $\overline{Q}$ outputs.

FUNCTION TABLE

Inputs				Outputs	
S	I_0	I_1	CP	Q	$\overline{Q}$*
L	L	X	⎍	L	H
L	H	X	⎍	H	L
H	X	L	⎍	L	H
H	X	H	⎍	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⎍ = LOW-to-HIGH Clock Transition
* = MC74AC398/74ACT398 only

LOGIC DIAGRAM



*MC74AC398/74ACT398

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT398/399)	1.5	mA	V_{IN} = V_{CC} − 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		180 160				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or $\overline{Q}$	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or $\overline{Q}$	3.3 5.0		8.5 6.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF		74AC T_A = −40°C to +85°C C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW I_n to CP	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW I_n to CP	3.3 5.0	0 0			ns	3-9
t_s	Setup Time, HIGH or LOW S to CP ('398)	3.3 5.0	4.5 3.0			ns	3-9
t_s	Setup Time, HIGH or LOW S to CP ('399)	3.3 5.0	4.5 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW S to CP	3.3 5.0	−1.5 −1.0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	5.5 4.0			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Input Clock Frequency	5.0		160				MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}$	5.0		7.0				ns	3-6
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}$	5.0		6.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW I_n to CP	5.0	3.0			ns	3-9
t_h	Hold Time, HIGH or LOW I_n to CP	5.0	0			ns	3-9
t_s	Setup Time, HIGH or LOW S to CP ('398)	5.0	3.0			ns	3-9
t_s	Setup Time, HIGH or LOW S to CP ('399)	5.0	3.0			ns	3-9
t_h	Hold Time, HIGH or LOW S to CP	5.0	−1.0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	5.5			ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC520
MC74ACT520
MC74AC521
MC74ACT521

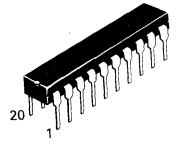
Product Preview

8-Bit Identity Comparator

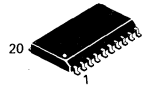
8-BIT IDENTITY COMPARATOR

The MC74AC534/74ACT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The MC74AC534/74ACT534 is the same as the MC74AC374/74ACT374 except that the outputs are inverted.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- 'ACT534 Has TTL Compatible Inputs
- Inverted Output Version of MC74AC374/74ACT374

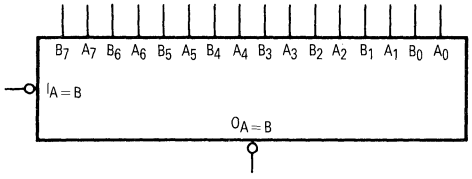


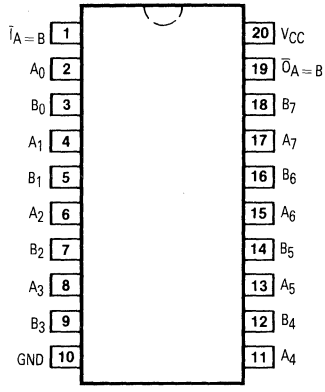
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

A_0–A_7	Word A Inputs
B_0–B_7	Word B Inputs
$\overline{I}_{A=B}$	Expansion or Enable Input
$\overline{O}_{A=B}$	Identity Output

TRUTH TABLE

Inputs		Outputs
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = HIGH Voltage Level
L = LOW Voltage Level
*$A_0=B_0$, $A_1=B_1$, $A_2=B_2$, etc.

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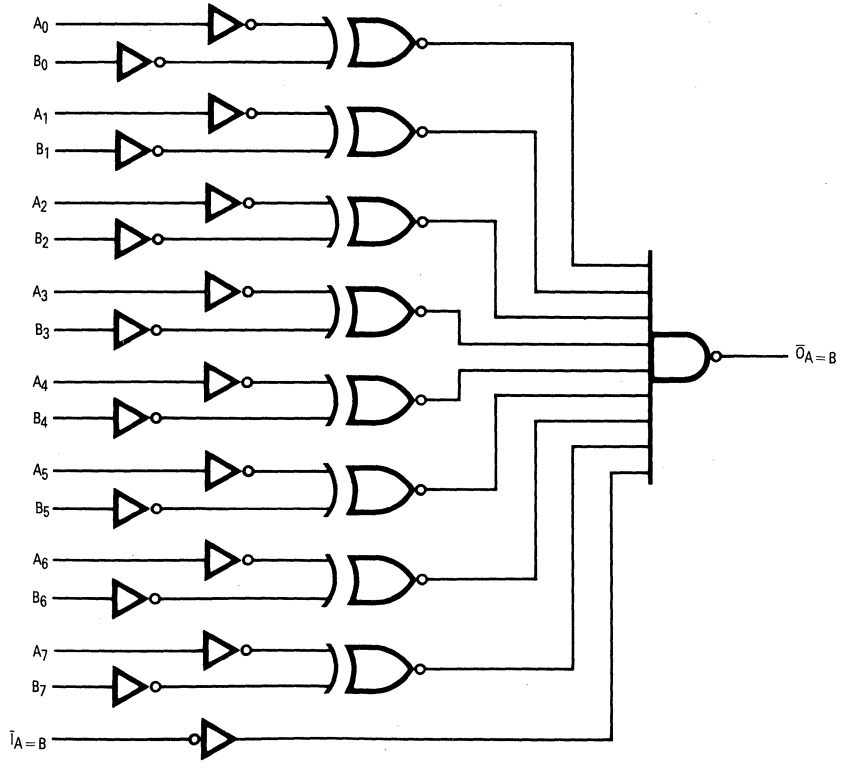
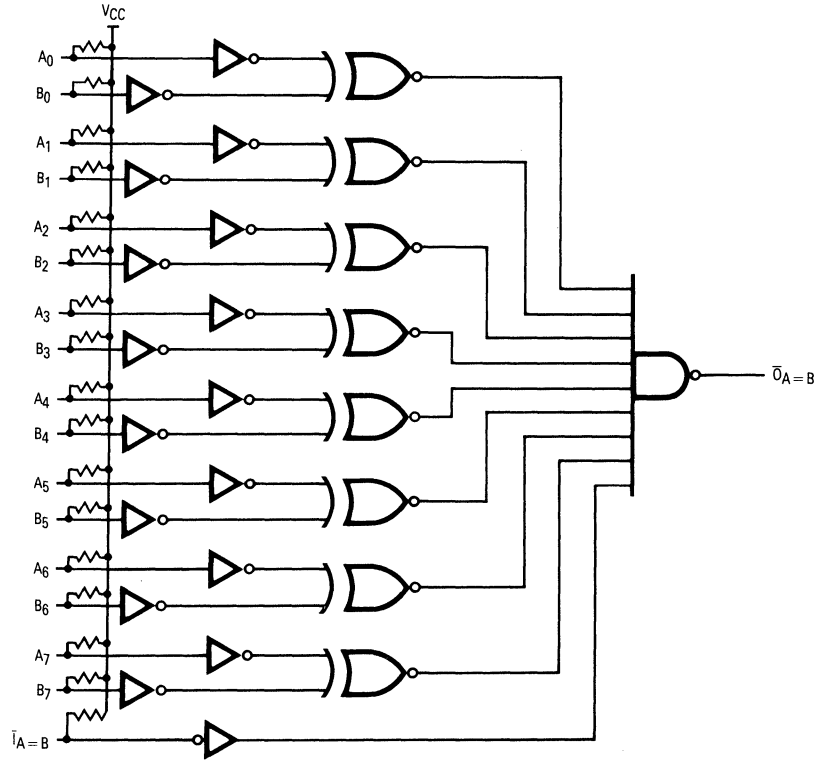
LOGIC DIAGRAM (MC74AC521/74ACT521)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

LOGIC DIAGRAM (MC74AC520/74ACT520)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT520/521)	1.5	mA	V_{IN} = V_{CC} – 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.3 5.0		13 9.5				ns	3-6
t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.3 5.0		13 9.5				ns	3-6
t_{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3 5.0		9.0 6.5				ns	3-6
t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3 5.0		9.5 7.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	5.0		9.5				ns	3-6
t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	5.0		9.5				ns	3-6
t_{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0		6.5				ns	3-6
t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0		7.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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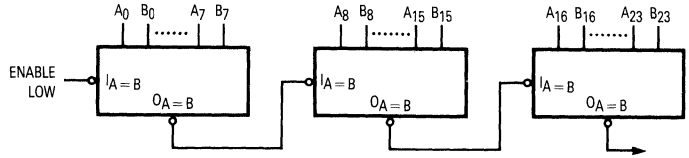
CAPACITANCE

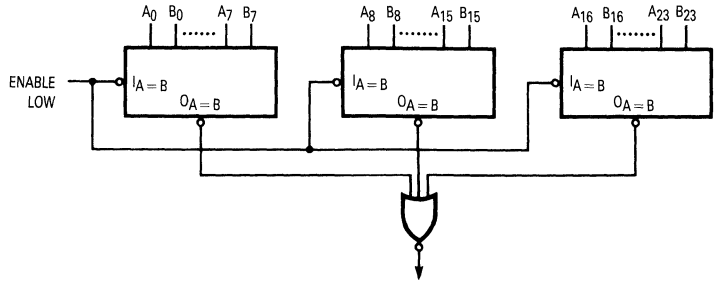
Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

APPLICATIONS

RIPPLE EXPANSION



PARALLEL EXPANSION



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MOTOROLA

MC74AC533
MC74ACT533

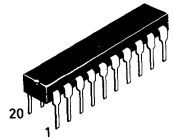
Product Preview

Octal Transparent Latch with 3-State Outputs

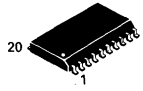
OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

The MC74AC533/74ACT533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. The MC74AC533/74ACT533 is the same as the MC74AC373/74ACT373, except that the outputs are inverted on the MC74AC533/74ACT533. For functional description please refer to the MC74AC373/74ACT373 data sheet.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- 'ACT533 Has TTL Compatible Inputs
- Inverted Output Version of MC74ACT373

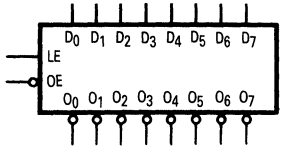


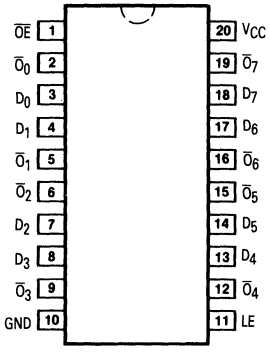
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_7	Data Inputs
$\overline{LE}$	Latch Enable Input
$\overline{OE}$	Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	Complementary 3-State Outputs

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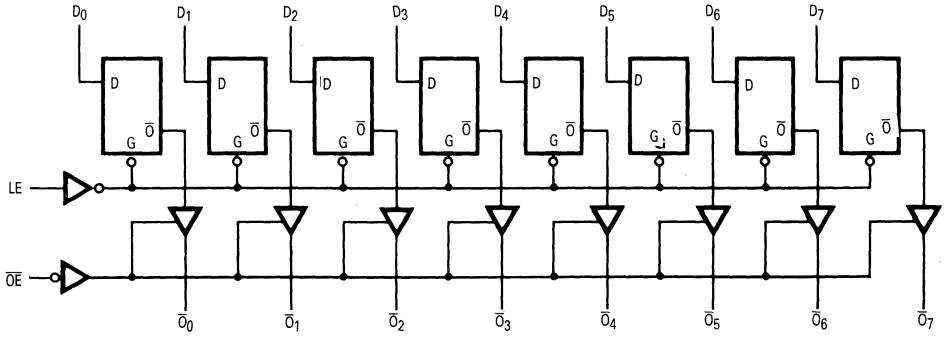
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT533)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	3.3 5.0		8.0 5.0				ns	3-5
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	3.3 5.0		7.0 5.0				ns	3-5
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	3.3 5.0		8.0 5.0				ns	3-6
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	3.3 5.0		7.0 5.0				ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		6.5 4.5				ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		6.0 4.5				ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 5.0				ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.0 3.5				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	3.5 2.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	−2.5 −1.5			ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	3.0 2.5			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	5.0		7.0				ns	3-5
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	5.0		6.5				ns	3-5
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	5.0		6.5				ns	3-6
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0		6.0				ns	3-6
t_{PZH}	Output Enable Time	5.0		6.0				ns	3-7
t_{PZL}	Output Enable Time	5.0		5.5				ns	3-8
t_{PHZ}	Output Disable Time	5.0		7.5				ns	3-7
t_{PLZ}	Output Disable Time	5.0		5.0				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	2.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−1.5			ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.0			ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC534
MC74ACT534

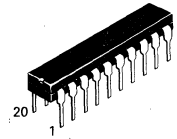
Product Preview

Octal D-Type Flip-Flop with 3-State Outputs

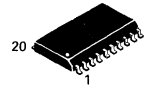
OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

The MC74AC534/74ACT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The MC74AC534/74ACT534 is the same as the MC74AC374/74ACT374 except that the outputs are inverted.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- 'ACT534 Has TTL Compatible Inputs
- Inverted Output Version of MC74AC374/74ACT374

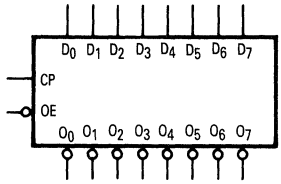


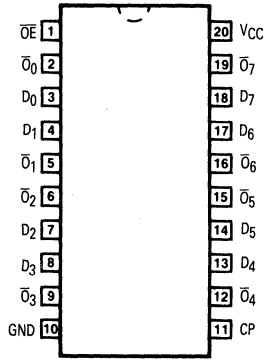
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	Complementary 3-State Outputs

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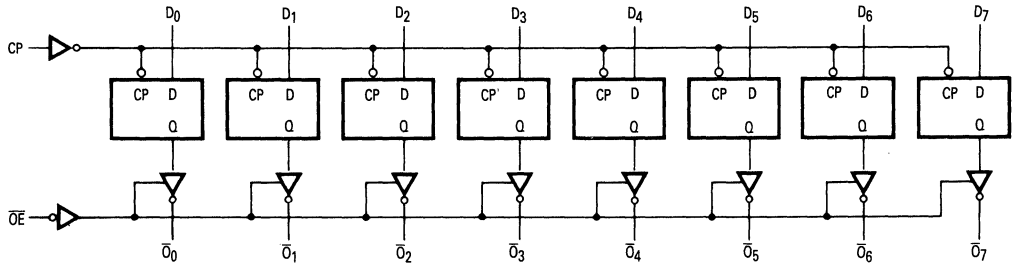
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

The MC74AC534/74ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT534)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		125 150				MHz	3-3
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0		10 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0		9.5 6.5				ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		8.5 6.5				ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		8.5 6.0				ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		9.0 7.0				ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		7.5 6.0				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 −0.5			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		100				MHz	3-3
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	5.0		6.5				ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{O}_n$	5.0		6.0				ns	3-6
t_{PZH}	Output Enable Time	5.0		5.5				ns	3-7
t_{PZL}	Output Enable Time	5.0		5.5				ns	3-8
t_{PHZ}	Output Disable Time	5.0		7.0				ns	3-7
t_{PLZ}	Output Disable Time	5.0		5.0				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5			ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.5			ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

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MOTOROLA

MC74AC540
MC74ACT540
MC74AC541
MC74ACT541

Product Preview

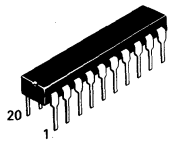
Octal Buffer/Line Driver with 3-State Outputs

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

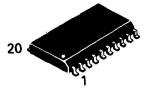
The MC74AC540/74ACT540 and MC74AC541/74ACT541 are octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers. The MC74AC541/74ACT541 is a noninverting option of the MC74AC540/74ACT540.

These devices are similar in function to the MC74AC240/74ACT240 and MC74AC244/74ACT244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

- 3-State Outputs
- Inputs and Outputs Opposite Side of Package, Allowing Easier Interface to Microprocessors
- Outputs Source/Sink 24 mA
- MC74AC540/74ACT540 Provides Inverted Outputs
- MC74AC541/74ACT541 Provides Noninverted Outputs
- 'ACT540 and 'ACT541 Have TTL Compatible Inputs

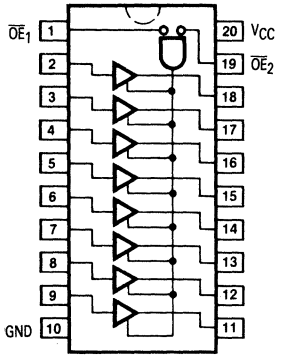


N SUFFIX
CASE 738-03
PLASTIC

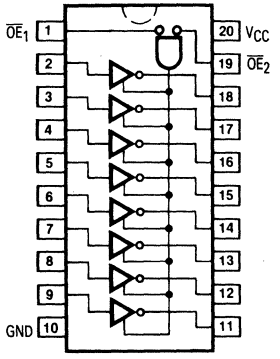


DW SUFFIX
CASE 751D-03
PLASTIC

MC74AC540/74ACT540



MC74AC541/74ACT541



TRUTH TABLE

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D	'540	'541
L	L	H	L	L
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT540/541)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output ('AC540)	3.3 5.0	1.0 1.0	5.5 4.0	7.5 6.0	1.0 1.0	8.0 6.5	ns	3-5
t_{PHL}	Propagation Delay Data to Output ('AC540)	3.3 5.0	1.0 1.0	5.0 4.0	7.0 5.5	1.0 1.0	7.5 6.0	ns	3-5
t_{PZH}	Output Enable Time ('AC540)	3.3 5.0	1.0 1.0	8.5 6.5	11 8.5	1.0 1.0	12 9.5	ns	3-7
t_{PZL}	Output Enable Time ('AC540)	3.3 5.0	1.0 1.0	7.5 6.0	10 7.5	1.0 1.0	11 8.5	ns	3-8
t_{PHZ}	Output Disable Time ('AC540)	3.3 5.0	1.0 1.0	8.5 7.5	13 10.5	1.0 1.0	14 11	ns	3-7
t_{PLZ}	Output Disable Time ('AC540)	3.3 5.0	1.0 1.0	7.0 6.0	10 8.0	1.0 1.0	11 9.0	ns	3-8
t_{PLH}	Propagation Delay Data to Output ('AC541)	3.3 5.0	1.0 1.0	5.5 4.0	8.0 6.0	1.0 1.0	9.0 6.5	ns	3-5
t_{PHL}	Propagation Delay Data to Output ('AC541)	3.3 5.0	1.0 1.0	5.5 4.0	8.0 6.0	1.0 1.0	8.5 6.5	ns	3-5
t_{PZH}	Output Enable Time ('AC541)	3.3 5.0	1.0 1.0	8.0 6.0	11.5 8.5	1.0 1.0	12.5 9.5	ns	3-7
t_{PZL}	Output Enable Time ('AC541)	3.3 5.0	1.0 1.0	7.0 5.5	10 7.5	1.0 1.0	11.5 8.5	ns	3-8
t_{PHZ}	Output Disable Time ('AC541)	3.3 5.0	1.0 1.0	9.0 7.0	12.5 9.5	1.0 1.0	14 10.5	ns	3-7
t_{PLZ}	Output Disable Time ('AC541)	3.3 5.0	1.0 1.0	6.5 5.5	9.5 7.5	1.0 1.0	10.5 8.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output ('ACT540)	5.0		6.0				ns	3-5
t_{PHL}	Propagation Delay Data to Output ('ACT540)	5.0		5.5				ns	3-5
t_{PZH}	Output Enable Time ('ACT540)	5.0		8.0				ns	3-7
t_{PZL}	Output Enable Time ('ACT540)	5.0		6.5				ns	3-8
t_{PHZ}	Output Disable Time ('ACT540)	5.0		10				ns	3-7
t_{PLZ}	Output Disable Time ('ACT540)	5.0		7.0				ns	3-8
t_{PLH}	Propagation Delay Data to Output ('ACT541)	5.0		6.0				ns	3-5
t_{PHL}	Propagation Delay Data to Output ('ACT541)	5.0		6.0				ns	3-5
t_{PZH}	Output Enable Time ('ACT541)	5.0		8.0				ns	3-7
t_{PZL}	Output Enable Time ('ACT541)	5.0		6.5				ns	3-8
t_{PHZ}	Output Disable Time ('ACT541)	5.0		10				ns	3-7
t_{PLZ}	Output Disable Time ('ACT541)	5.0		7.0				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	30	pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC563
MC74ACT563

Product Preview

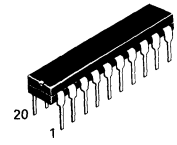
Octal D-Type Latch with 3-State Outputs

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUTS

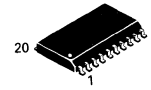
The MC74AC563/74ACT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

The MC74AC563/74ACT563 device is functionally identical to the MC74AC573/74ACT573, but with inverted outputs.

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to MC74AC573/74ACT573 but with Inverted Outputs
- Outputs Source/Sink 24 mA
- 'ACT563 Has TTL Compatible Inputs

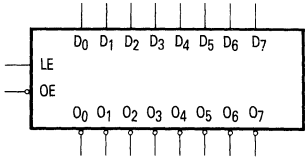


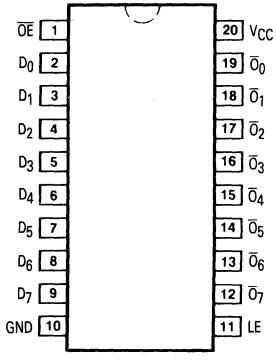
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	3-State Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	3-State Latch Outputs

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

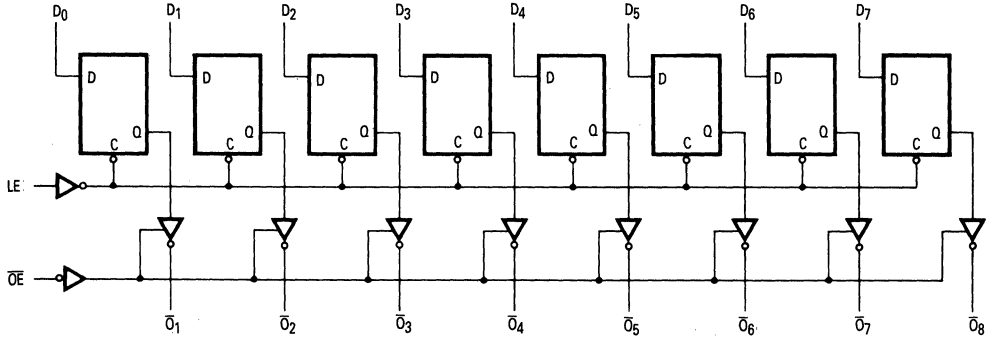
The MC74AC563/74ACT563 contains eight D-type latches with 3-state complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

FUNCTION TABLE

Inputs			Internal	Outputs	Function
$\overline{OE}$	LE	D	Q	O	
H	X	X	X	Z	High Z
H	H	L	H	Z	High Z
H	H	H	L	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT563)	1.5	mA	V_{IN} = V_{CC} – 2.1 V V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	3.3 5.0		7.5 5.0				ns	3-5
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	3.3 5.0		7.0 4.5				ns	3-5
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	3.3 5.0		7.5 5.0				ns	3-6
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	3.3 5.0		8.0 5.5				ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		6.0 4.0				ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		6.0 4.0				ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 5.0				ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.0 3.5				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	2.0 1.5			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	−2.5 −1.5			ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	3.0 2.5			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	5.0	1.0	7.0	11.5	1.0	12.5	ns	3-5
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	5.0	1.0	6.0	10	1.0	11	ns	3-5
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	5.0	1.0	6.5	10.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	5.5	9.0	1.0	10	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.5	8.5	1.0	9.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	6.5	10.5	1.0	11.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	4.5	8.0	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	1.5	4.0	4.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−2.0	0	0	ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.0	3.0	3.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC564
MC74ACT564

Product Preview

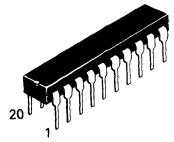
Octal D-Type Latch with 3-State Outputs

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUTS

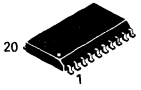
The MC74AC564/74ACT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The MC74AC564/74ACT564 device is functionally identical to the MC74AC574/74ACT574, but with inverted outputs.

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to MC74AC574/74ACT574 but with Inverted Outputs
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- 'ACT564 Has TTL Compatible Inputs

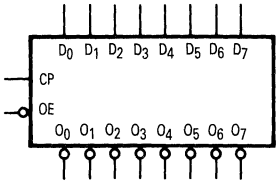


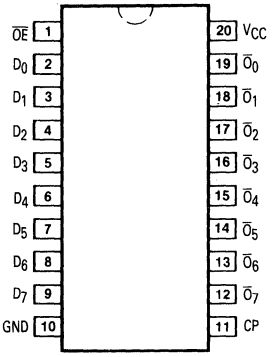
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_7	Data Inputs
$\overline{CP}$	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	3-State Outputs

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

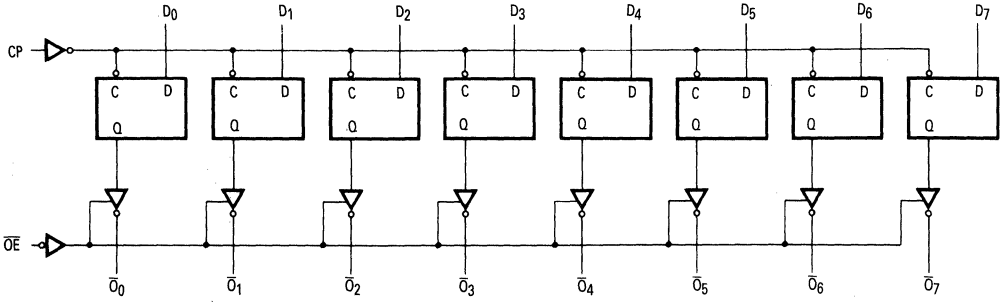
The MC74AC564/74ACT564 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

FUNCTION TABLE

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⌠	L	H	Z	Load
H	⌠	H	L	Z	Load
L	⌠	L	H	H	Data Available
L	⌠	H	L	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌠ = LOW-to-HIGH Transition
NC = No Change

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT564)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		110 150				MHz	3-3
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0		10.5 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0		9.5 6.0				ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		8.5 6.5				ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		8.0 5.5				ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		9.5 7.0				ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		7.5 5.5				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 −0.5			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	85	90		75		MHz	3-3
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	5.0	1.0	6.5	10.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{O}_n$	5.0	1.0	6.0	9.5	1.0	10.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	5.5	9.0	1.0	9.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.5	8.5	1.0	9.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	10.5	1.0	11.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	5.0	8.0	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0	2.5	3.0	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	1.0	1.0	ns	3-9
t_w	LE Pulse Width HIGH or LOW	5.0	2.5	3.0	3.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

5

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC568
MC74AC569

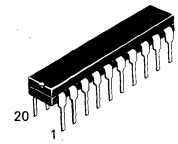
Product Preview

4-Bit Bidirectional Counters with 3-State Outputs

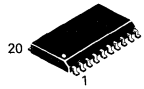
4-BIT BIDIRECTIONAL COUNTERS WITH 3-STATE OUTPUTS

The MC74AC568 and MC74AC569 are fully synchronous, bidirectional counters with 3-state outputs. The MC74AC568 is a BCD decade counter; the MC74AC569 is a modulo 16 binary counter. They feature preset capability for programmable operation, carry lookahead for easy cascading, and a U/$\overline{D}$ input to control the direction of counting. For maximum flexibility there are both synchronous and master asynchronous reset inputs as well as both Clocked Carry ($\overline{CC}$) and Terminal Count ($\overline{TC}$) outputs. All state changes except Master Reset are initiated by the rising edge of the clock. A HIGH signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high-impedance state but does not prevent counting, resetting or parallel loading.

- Synchronous Counting and Loading
- Lookahead Carry Capability for Easy Cascading
- Preset Capability for Programmable Operation
- 3-State Outputs for Bus Organized Systems
- Outputs Source/Sink 24 mA
- Synchronous and Asynchronous Resets

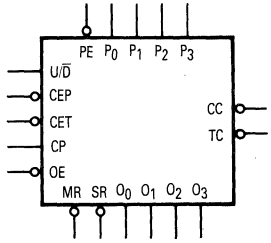


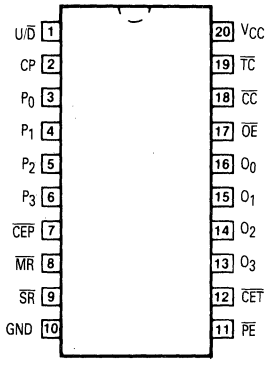
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL



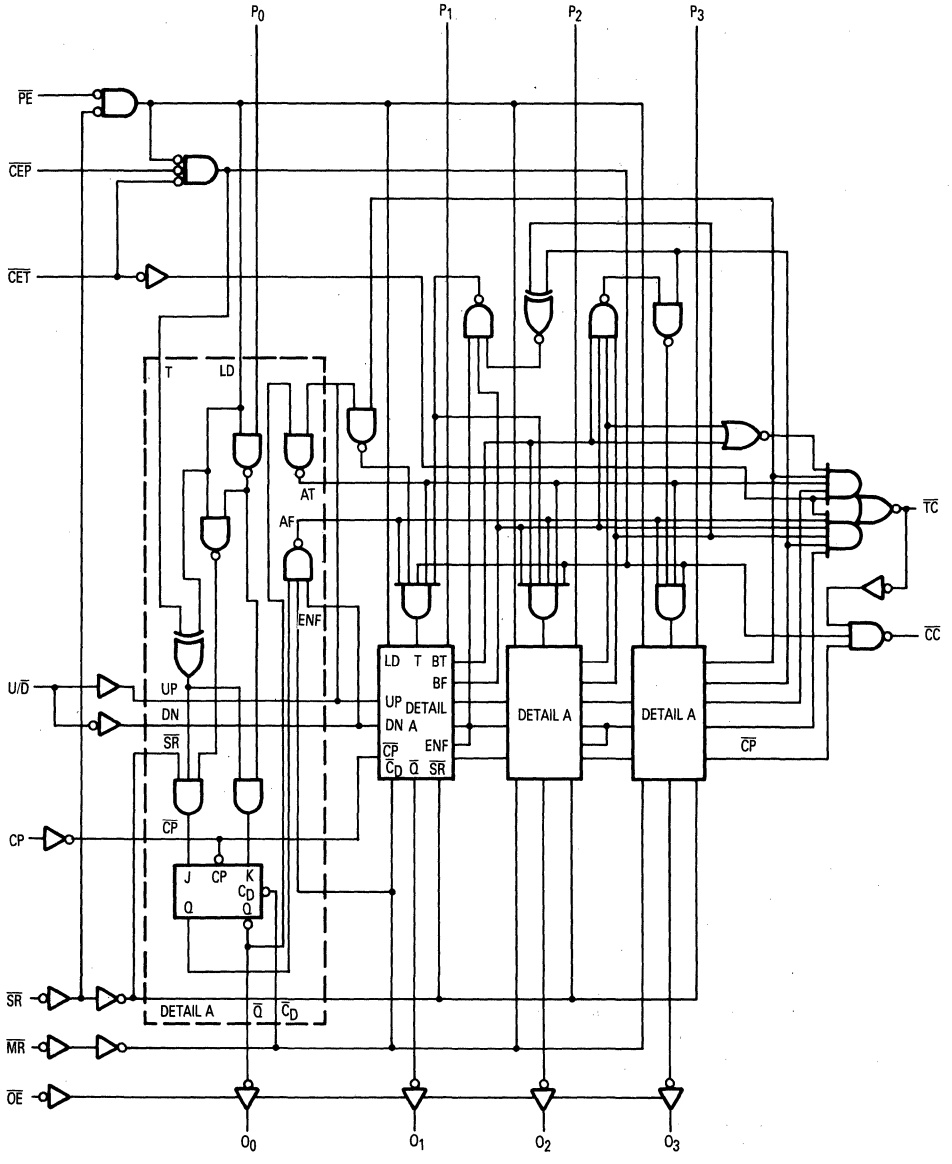


PIN NAMES

P_0–P_3	Parallel Data Inputs
$\overline{CEP}$	Count Enable Parallel Input
$\overline{CET}$	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{PE}$	Parallel Enable Input
U/$\overline{D}$	Up/Down Count Control Input
$\overline{OE}$	Output Enable Input
$\overline{MR}$	Master Reset Input
$\overline{SR}$	Synchronous Reset Input
O_0–O_3	3-State Parallel Data Outputs
$\overline{TC}$	Terminal Count Output
$\overline{CC}$	Clocked Carry Output

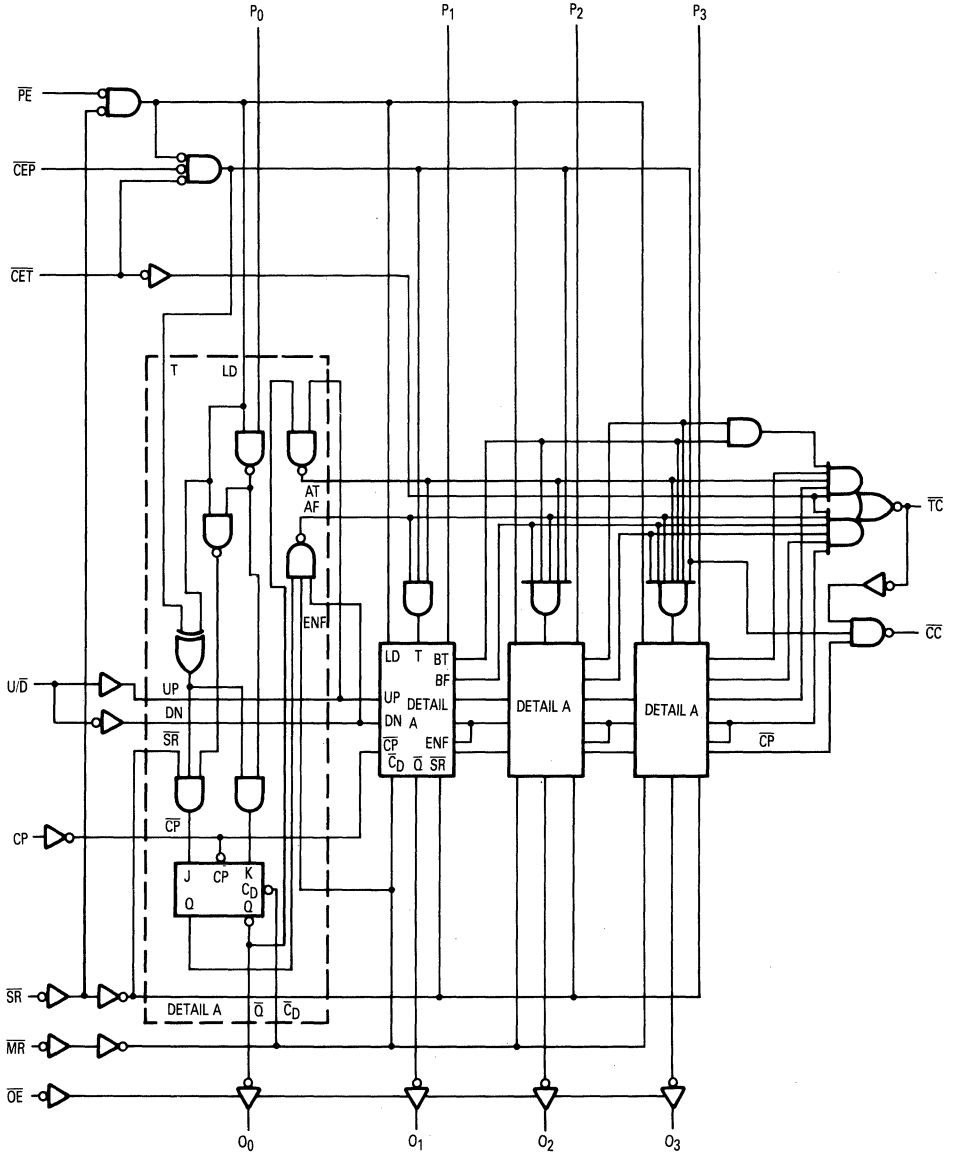
5

LOGIC DIAGRAM (MC74AC568)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

LOGIC DIAGRAM (MC74AC569)

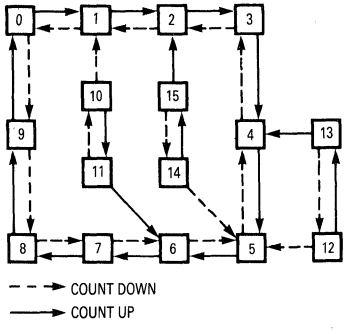


Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

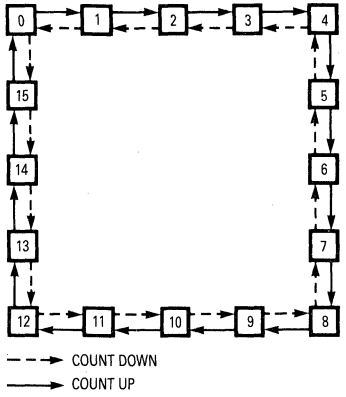
5

STATE DIAGRAMS

MC74AC568



MC74AC569



LOGIC EQUATIONS:

Count Enable $= \overline{CEP} \cdot \overline{CET} \cdot PE$

Up ('AC568): $\overline{TC} = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$

('AC569): $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$

Down (Both): $\overline{TC} = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot (Down) \cdot \overline{CET}$

FUNCTIONAL DESCRIPTION

The MC74AC568 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it will increment to 0 (LLLL) in the Up mode; in Down mode it will decrement from 0 to 9. The MC74AC569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the LOW-to-HIGH transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs — Master Reset ($\overline{MR}$), Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$) and Count Enable Trickle ($\overline{CET}$) — plus the Up/Down ($U/\overline{D}$) input determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$ and $\overline{PE}$ HIGH, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are LOW. Conversely, a HIGH signal on either $\overline{CEP}$ or $\overline{CET}$ inhibits counting.

the MC74AC568 and MC74AC569 use edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or $U/\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW providing $\overline{CET}$ is LOW, when the counter reaches zero in the Down mode, or reaches maximum (9 for the MC74AC568, 15 for the MC74AC569) in the Up mode. $\overline{TC}$ will then remain LOW until a state change occurs, whether by counting or presetting, or until $U/\overline{D}$ or $\overline{CET}$ is changed. To implement synchronous multistage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation. Figure a shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure b are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 10 (MC74AC568) or 16

(MC74AC569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally HIGH. When $\overline{SR}$ and $\overline{PE}$ are HIGH, and $\overline{CEP}$, $\overline{CET}$ and $\overline{TC}$ are LOW, the $\overline{CC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the $\overline{CC}$ Truth Table. When the Output Enable ($\overline{OE}$) is LOW, the parallel data outputs O_0–O_3 are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{OE}$ forces O_0–O_3 to the high-Z state but does not prevent counting, loading or resetting.

MODE SELECT TABLE

Inputs						Operating Mode
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	
L	X	X	X	X	X	Asynchronous Reset
H	L	X	X	X	X	Synchronous Reset
H	H	L	X	X	X	Parallel Load
H	H	H	H	X	X	Hold
H	H	H	X	H	X	Hold
H	H	H	L	L	H	Count Up
H	H	H	L	L	L	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

$\overline{CC}$ TRUTH TABLE

Inputs						Output
$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	$\overline{CC}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⊓	⊓

* = $\overline{TC}$ is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Figure a. Multistage Counter with Ripple Carry

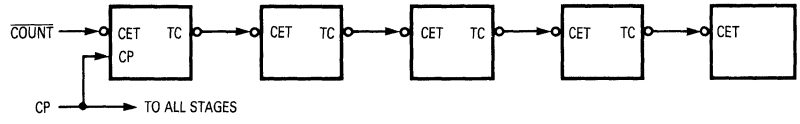
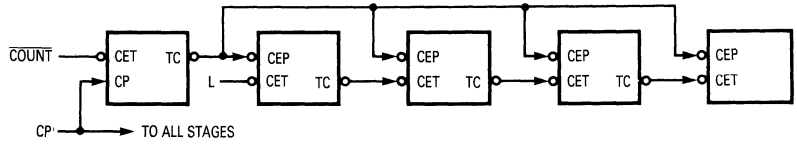


Figure b. Multistage Counter with Lookahead Carry



5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		87 117				MHz	3-3
t_{PLH}	Propagation Delay CP to O_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0		10 7.5				ns	3-6
t_{PHL}	Propagation Delay CP to O_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0		11 8.0				ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{TC}$	3.3 5.0		16.5 12				ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0		16.5 12				ns	3-6
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0		10.5 7.5				ns	3-6
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0		10 7.0				ns	3-6
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('568)	3.3 5.0		10.5 7.5				ns	3-6
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('568)	3.3 5.0		9.0 6.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS — continued (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('569)	3.3 5.0		10.5 7.5				ns	3-6
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('569)	3.3 5.0		9.0 6.5				ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{CC}$	3.3 5.0		11 8.0				ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{CC}$	3.3 5.0		9.5 7.0				ns	3-6
t_{PLH}	Propagation Delay $\overline{CEP}$ or $\overline{CET}$ to $\overline{CC}$	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{CEP}$ or $\overline{CET}$ to $\overline{CC}$	3.3 5.0		9.5 7.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to O_n	3.3 5.0		12.5 9.0				ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		7.5 5.5				ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		7.5 5.5				ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		9.5 7.0				ns	3-7
t_{PZL}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		11 8.0				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	8.0 6.0			ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	0 0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	3.3 5.0	8.0 12.5			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	3.3 5.0	0 0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	12.5 9.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	0 0			ns	3-9
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP ('568)	3.3 5.0	12.5 9.0			ns	3-9
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP ('569)	3.3 5.0	12.5 9.0			ns	3-9
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to CP	3.3 5.0	0 0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	4.0 3.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−1.5 −1.0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS — continued

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	4.0 3.0			ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	4.0 3.0			ns	3-6
t_{rec}	$\overline{MR}$ Recovery Time	3.3 5.0	4.0 3.0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC573
MC74ACT573

Product Preview

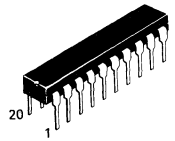
Octal D-Type Latch with 3-State Outputs

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUTS

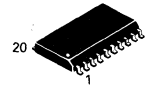
The MC74AC573/74ACT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

The MC74AC573/74ACT573 is functionally identical to the MC74AC373/74ACT373 but has inputs and outputs on opposite sides.

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to MC74AC373/74ACT373
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- 'ACT573 Has TTL Compatible Inputs

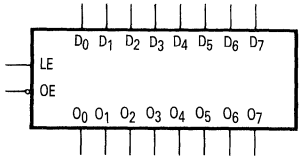


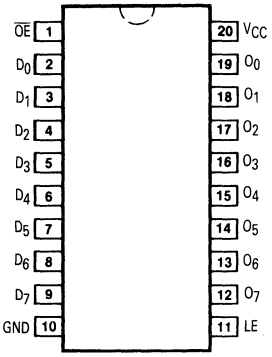
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	3-State Output Enable Input
O_0–O_7	3-State Latch Outputs

TRUTH TABLE

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	H
L	L	X	O_0
H	X	X	Z

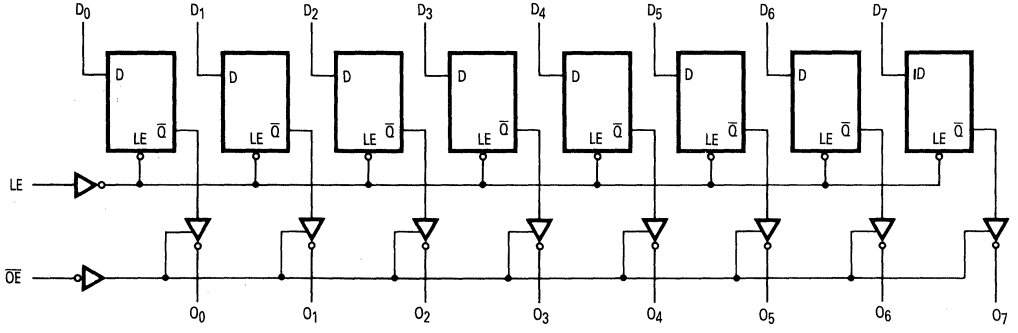
H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before LOW-to-HIGH Transition of Clock

5

FUNCTIONAL DESCRIPTION

The MC74AC573/74ACT573 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT573)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3 5.0		9.0 6.0				ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	3.3 5.0		9.0 6.0				ns	3-5
t_{PLH}	Propagation Delay LE to O_n	3.3 5.0		9.0 6.0				ns	3-6
t_{PHL}	Propagation Delay LE to O_n	3.3 5.0		8.0 5.5				ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		7.0 5.5				ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		7.5 5.5				ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		8.5 6.5				ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		6.5 5.0				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	2.0 1.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	0 0			ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.5			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0	1.0	6.0	10.5	1.0	12	ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	5.0	1.0	6.0	10.5	1.0	12	ns	3-5
t_{PLH}	Propagation Delay LE to O_n	5.0	1.0	6.0	10.5	1.0	12	ns	3-6
t_{PHL}	Propagation Delay LE to O_n	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	5.5	10	1.0	11	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.5	9.5	1.0	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	6.5	11	1.0	12.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	5.0	8.5	1.0	9.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	1.5	3.0	3.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−1.5	0	0	ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.0	3.5	4.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	25	pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC574
MC74ACT574

Product Preview

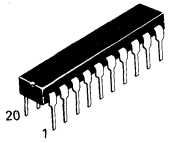
Octal D-Type Flip-Flop with 3-State Outputs

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

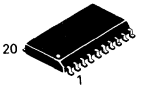
The MC74AC574/74ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The MC74AC574/74ACT574 is functionally identical to the MC74AC374/74ACT374 except for the pinouts.

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to MC74AC374/74ACT374
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- 'ACT574 Has TTL Compatible Inputs

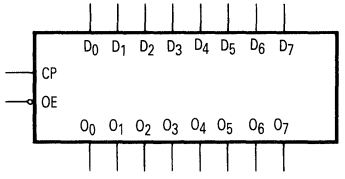


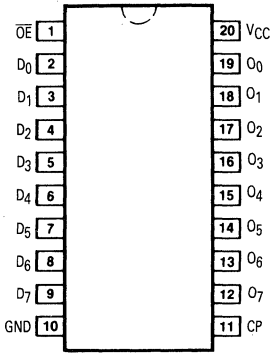
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
O_0–O_7	3-State Outputs

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

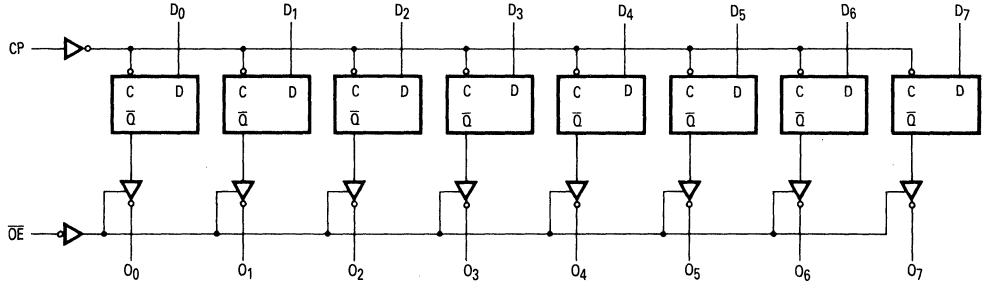
The MC74AC574/74ACT574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

FUNCTION TABLE

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O_n	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⎍	L	L	Z	Load
H	⎍	H	H	Z	Load
L	⎍	L	L	L	Data Available
L	⎍	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⎍ = LOW-to-HIGH Clock Transition
NC = No Change

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT574)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		110 160				MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0		10 7.0				ns	3-6
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0		10 6.5				ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		6.5 5.0				ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		6.0 4.0				ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 5.0				ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.0 3.5				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	4.0 2.5			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	100	110		85		ns	3-3
t_{PLH}	Propagation Delay CP to O_n	5.0	1.0	7.0	11	1.0	12	ns	3-6
t_{PHL}	Propagation Delay CP to O_n	5.0	1.0	6.5	10	1.0	11	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	6.4	9.5	1.0	10	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	6.0	9.0	1.0	10	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	10.5	1.0	11.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	5.5	8.5	1.0	9.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.5	2.5	2.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	1.0	1.0	ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	3.0	4.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V

MOTOROLA

MC74AC640
MC74ACT640

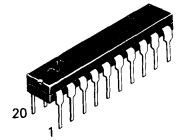
Product Preview

Octal Bidirectional Transceiver with 3-State Outputs

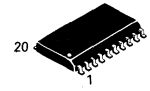
OCTAL BIDIRECTIONAL TRANSCEIVER WITH 3-STATE OUTPUTS

The MC74AC640/74ACT640 octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from bus A to bus B when T/$\overline{R}$ = HIGH, or from bus B to bus A when T/$\overline{R}$ = LOW. The enable input can be used to disable the device so the buses are effectively isolated.

- Bidirectional Data Path
- A and B Outputs Sink 24 mA/Source −24 mA
- 'ACT640 Has TTL Compatible Inputs



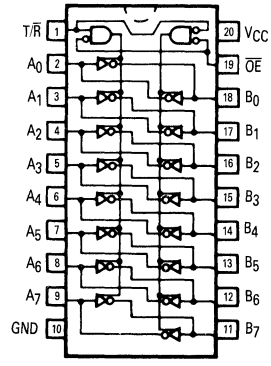
N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

PIN NAMES

A_0–A_7	Side A Inputs or 3-State Outputs
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
B_0–B_7	Side B Inputs or 3-State Outputs



TRUTH TABLE

$\overline{OE}$	T/$\overline{R}$	Applied Inputs	Valid Direction I/P→O/P	Output
H	X	X	X	X
L	H	H	A to B	L
L	H	L	A to B	H
L	L	H	B to A	L
L	L	L	B to A	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT640)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	3.3 5.0		5.5 4.0				ns	3-5
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	3.3 5.0		5.5 4.0				ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0		8.0 6.0				ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		7.5 5.5				ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 6.0				ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		7.5 6.0				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	5.0		5.0				ns	3-5
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	5.0		5.0				ns	3-5
t_{PZH}	Output Enable Time	5.0		7.0				ns	3-7
t_{PZL}	Output Enable Time	5.0		6.0				ns	3-8
t_{PHZ}	Output Disable Time	5.0		6.5				ns	3-7
t_{PLZ}	Output Disable Time	5.0		6.0				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0$ V
$C_{I/O}$	Input/Output Capacitance	15	pF	$V_{CC} = 5.0$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.0$ V

MOTOROLA

MC74AC643
MC74ACT643

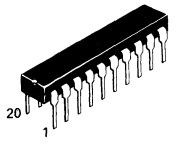
Product Preview

Octal Bidirectional Transceiver with 3-State Outputs

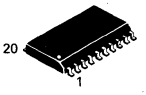
OCTAL BIDIRECTIONAL TRANSCEIVER WITH 3-STATE OUTPUTS

The MC74AC643/74ACT643 octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from bus A to bus B when T/$\overline{R}$ = HIGH, or from bus B to bus A when T/$\overline{R}$ = LOW. The enable input can be used to disable the device so the buses are effectively isolated.

- Noninverting Buffers
- Bidirectional Data Path
- A and B Outputs Sink 24 mA/Source −24 mA
- 'ACT643 Has TTL Compatible Inputs



N SUFFIX
CASE 738-03
PLASTIC



DW SUFFIX
CASE 751D-03
PLASTIC

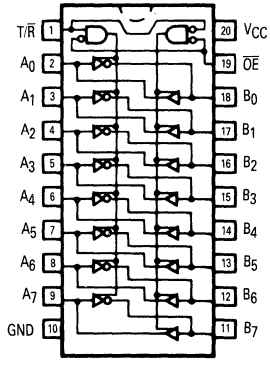
PIN NAMES

A_0–A_7	Side A Inputs or 3-State Outputs
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
B_0–B_7	Side B Inputs or 3-State Outputs

TRUTH TABLE

$\overline{OE}$	T/$\overline{R}$	Applied Inputs	Valid Direction I/P→O/P	Output
H	X	X	X	X
L	H	H	A to B	L
L	H	L	A to B	H
L	L	H	B to A	H
L	L	L	B to A	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT643)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	3.3 5.0		5.5 4.0				ns	3-5
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	3.3 5.0		5.5 4.0				ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0		8.0 6.0				ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		7.5 5.5				ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 6.0				ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		7.5 6.0				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	5.0		5.0				ns	3-5
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	5.0		5.0				ns	3-5
t_{PZH}	Output Enable Time	5.0		7.0				ns	3-7
t_{PZL}	Output Enable Time	5.0		6.0				ns	3-8
t_{PHZ}	Output Disable Time	5.0		6.5				ns	3-7
t_{PLZ}	Output Disable Time	5.0		6.0				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.0$ V
$C_{I/O}$	Input/Output Capacitance	15	pF	$V_{CC} = 5.0$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.0$ V

MOTOROLA

MC74AC646

Product Preview

Octal Transceiver/Register with 3-State Outputs (Non-Inverting)

OCTAL TRANSCEIVER/REGISTER WITH 3-STATE OUTPUTS (NON-INVERTING)

The MC74AC646 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated in the following figures.

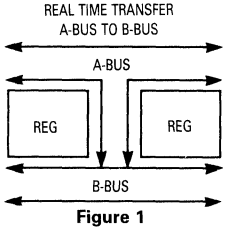


Figure 1

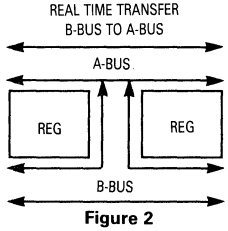


Figure 2

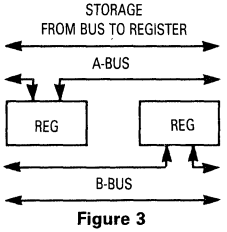


Figure 3

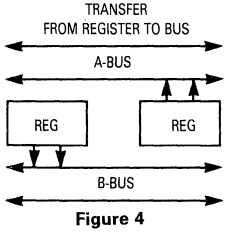
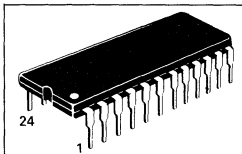
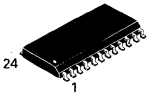


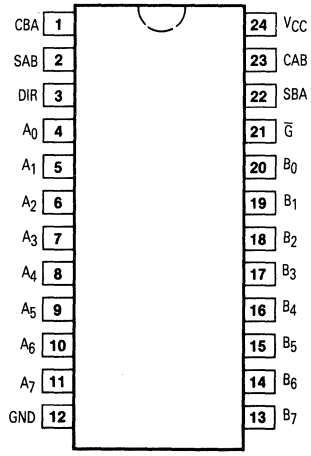
Figure 4



N SUFFIX
CASE 649-03
PLASTIC

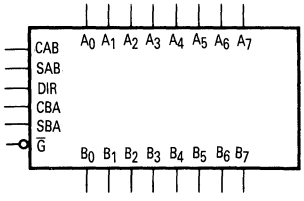


DW SUFFIX
CASE 751E-02
PLASTIC



- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data Transfers
- Choice of True and Inverting Data Paths
- 3-State Outputs
- 300 mil Slim Dual In-Line Package
- Outputs Source/Sink 24 mA

LOGIC SYMBOL



PIN NAMES

A_0–A_7	Data Register Inputs Data Register A Outputs
B_0–B_7	Data Register B Inputs Data Register B Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\overline{G}$	Output Enable Inputs

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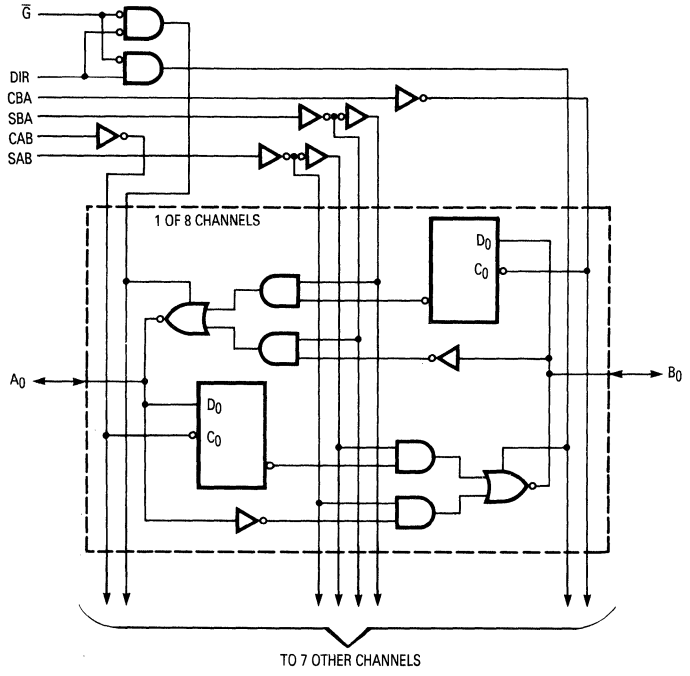
FUNCTION TABLE

Inputs						Data I/O*		Operation or Function
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	⌐	⌐	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0	10.5 7.5	16.5 12	1.0 1.0	18.5 13	ns	3-6
t_{PHL}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0	9.5 6.5	14.5 10.5	1.0 1.0	16 11.5	ns	3-6
t_{PLH}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0	7.5 5.0	12 8.0	1.0 1.0	13.5 9.0	ns	3-5
t_{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0	7.5 5.0	12.5 9.0	1.0 1.0	13.5 9.5	ns	3-5
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	3.3 5.0	1.0 1.0	8.5 6.0	13.5 10	1.0 1.0	15.5 11	ns	3-6
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	3.3 5.0	1.0 1.0	8.5 6.0	13.5 10	1.0 1.0	15 11	ns	3-6
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	7.0 5.0	11.5 8.5	1.0 1.0	12.5 9.0	ns	3-7
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0	1.0 1.0	14 10	ns	3-8
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	8.0 6.5	12.5 10	1.0 1.0	13.5 11	ns	3-7
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	7.5 6.0	12 9.5	1.0 1.0	13.5 10.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS — continued (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PZH}	Enable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	6.5 5.0	11 7.5	1.0 1.0	12 8.5	ns	3-7
t_{PZL}	Enable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	7.0 5.0	11.5 8.0	1.0 1.0	13 9.0	ns	3-8
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	7.5 5.5	11.5 9.5	1.0 1.0	12.5 10	ns	3-7
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	7.5 5.5	12 9.5	1.0 1.0	13.5 10.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup time, HIGH or LOW Bus to Clock	3.3 5.0	2.0 1.5	5.0 4.0	5.5 4.5	ns	3-9
t_h	Hold Time, HIGH or LOW Bus to Clock	3.3 5.0	−1.5 −0.5	0 0.5	0 1.0	ns	3-9
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	2.0 2.0	3.5 3.5	4.5 3.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
$C_{I/O}$	Input/Output Capacitance	15	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	60	pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC648

Product Preview

Octal Transceiver/Register with 3-State Outputs (Inverting)

OCTAL TRANSCEIVER/REGISTER WITH 3-STATE OUTPUTS (INVERTING)

The MC74AC648 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated in the following figures.

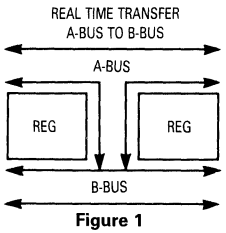


Figure 1

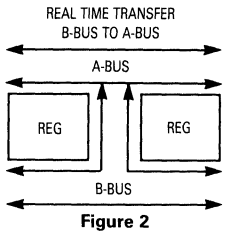


Figure 2

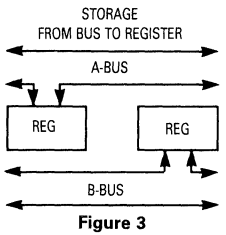


Figure 3

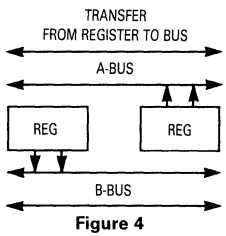
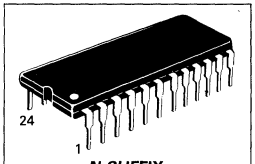
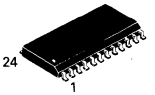


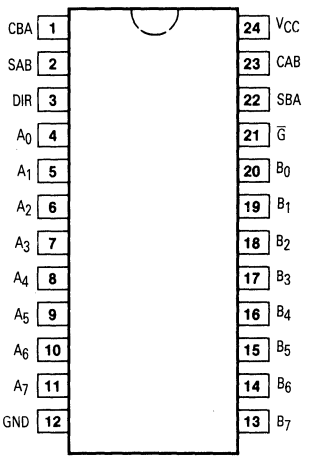
Figure 4



N SUFFIX
CASE 649-03
PLASTIC

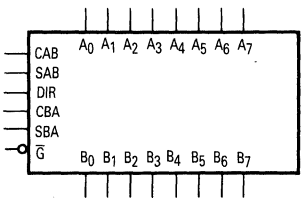


DW SUFFIX
CASE 751E-02
PLASTIC



- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data Transfers
- Choice of True and Inverting Data Paths
- 3-State Outputs
- 300 mil Slim Dual In-Line Package
- Outputs Source/Sink 24 mA

LOGIC SYMBOL



PIN NAMES

A_0–A_7	Data Register Inputs Data Register A Outputs
B_0–B_7	Data Register B Inputs Data Register B Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\overline{G}$	Output Enable Inputs

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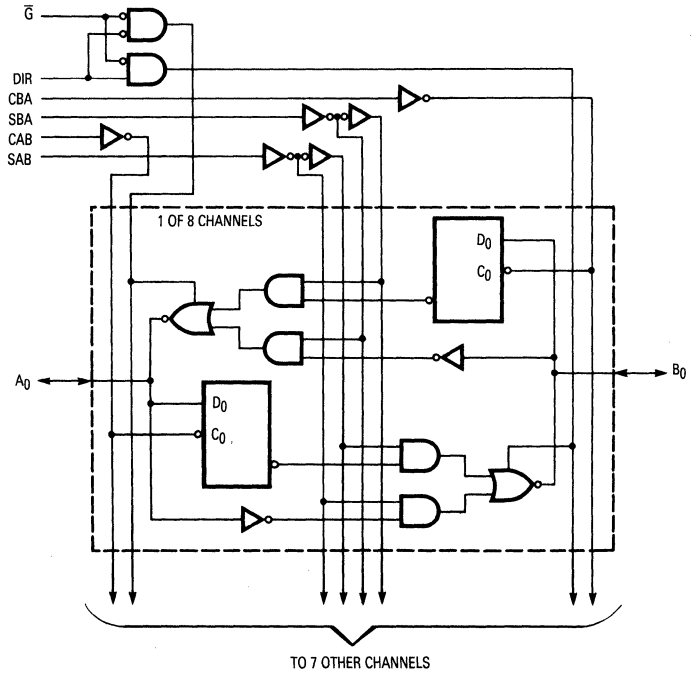
FUNCTION TABLE

Inputs						Data I/O*		Operation or Function
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	⌐	⌐	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus

*The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0	10 7.0	15.5 11	1.0 1.0	17 12	ns	3-6
t_{PHL}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0	8.5 6.0	13.5 10.5	1.0 1.0	14.5 11.5	ns	3-6
t_{PLH}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0	6.0 4.0	10 7.0	1.0 1.0	11 7.5	ns	3-5
t_{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0	5.5 3.5	9.0 7.5	1.0 1.0	10 8.0	ns	3-5
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0	1.0 1.0	14 10	ns	3-6
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/A_n or B_n HIGH or LOW)	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.5	1.0 1.0	14 10.5	ns	3-6
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	6.5 5.0	11 8.0	1.0 1.0	11.5 9.0	ns	3-7
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	7.0 5.0	11 8.0	1.0 1.0	12.5 9.0	ns	3-8
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	7.5 6.0	12 10	1.0 1.0	13 11	ns	3-7
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	7.0 5.5	11.5 9.0	1.0 1.0	12.5 10	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS — continued (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PZH}	Enable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	6.0 4.5	12.5 9.5	1.0 1.0	14 10.5	ns	3-7
t_{PZL}	Enable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	6.5 4.5	13 9.0	1.0 1.0	14.5 10.5	ns	3-8
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	7.0 5.5	11.5 9.0	1.0 1.0	13.5 10	ns	3-7
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	7.0 50	13.5 9.5	1.0 1.0	15 10	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup time, HIGH or LOW Bus to Clock	3.3 5.0	2.0 1.5	3.0 2.0	3.5 2.0	ns	3-9
t_h	Hold Time, HIGH or LOW Bus to Clock	3.3 5.0	−1.5 −0.5	0 1.0	0 1.0	ns	3-9
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	2.0 2.0	3.5 3.0	4.0 3.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
$C_{I/O}$	Input/Output Capacitance	15	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	65	pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC825
MC74ACT825
MC74AC826
MC74ACT826

Product Preview

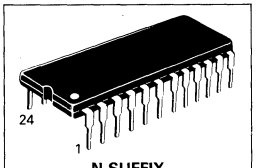
8-Bit D-Type Flip-Flop

8-BIT D-TYPE FLIP-FLOP

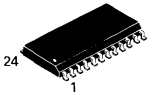
The MC74AC825/74ACT825 and MC74AC826/74ACT826 are 8-bit buffered registers. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface. The MC74AC825/74ACT825 has noninverting outputs; the MC74AC826/74ACT826 has inverting outputs.

The MC74AC825/74ACT825 is fully compatible with AMD's AM29825.

- Outputs Source/Sink 24 mA
- Inputs and Outputs are on Opposite Sides
- 'ACT825 and 'ACT826 Have TTL Compatible Inputs

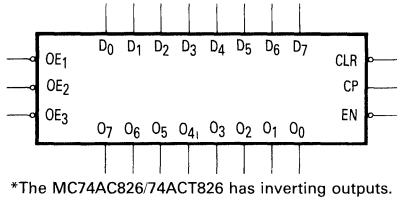


N SUFFIX
CASE 649-03
PLASTIC

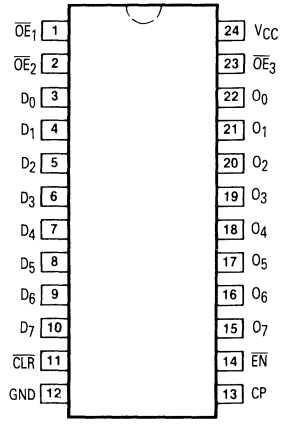


DW SUFFIX
CASE 751E-02
PLASTIC

LOGIC SYMBOL (MC74AC825/74ACT825)*



*The MC74AC826/74ACT826 has inverting outputs.



PIN NAMES

D_0–D_7	Data Inputs
O_0–O_7	Data Outputs (MC74AC825/74ACT825)
$\overline{O}_0$–$\overline{O}_7$	Data Outputs (MC74AC826/74ACT826)
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Output Enables
$\overline{EN}$	Clock Enable
$\overline{CLR}$	Clear
CP	Clock Input

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FUNCTIONAL DESCRIPTION

The MC74AC825/74ACT825 and MC74AC826/74ACT826 consist of eight D-type edge-triggered flip-flops. These devices have 3-state outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}_1$, $\overline{OE}_2$ and $\overline{OE}_3$ LOW, the contents of the flip-flops are available at the outputs. When one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the outputs go to the high impedance state.

Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The MC74AC825/74ACT825 and MC74AC826/74ACT826 have Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These pins are ideal for parity bus interfacing in high performance systems.

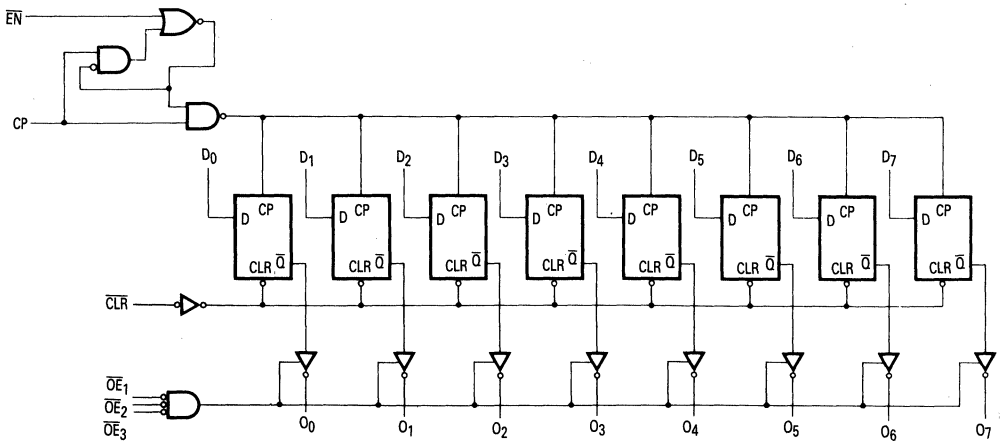
When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

FUNCTION TABLE

Inputs					Internal	Outputs		Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	Dn	Q	O ('825)	$\overline{O}$ ('826)	
H	X	L	⎍	L	L	Z	Z	High Z
H	X	L	⎍	H	H	Z	Z	High Z
H	L	X	X	X	L	Z	Z	Clear
L	L	X	X	X	L	L	L	Clear
H	H	H	X	X	NC	Z	Z	Hold
L	H	H	X	X	NC	NC	NC	Hold
H	H	L	⎍	L	L	Z	Z	Load
H	H	L	⎍	H	H	Z	Z	Load
L	H	L	⎍	L	L	L	H	Load
L	H	L	⎍	H	H	H	L	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⎍ = LOW-to-HIGH Transition
NC = No Change

LOGIC DIAGRAM (MC74AC825/74ACT825)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The MC74AC826/74ACT826 also has the same logic diagram with inverting outputs.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT825/826)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		100 125				MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0		9.0 6.5				ns	3-6
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0		9.0 6.5				ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	3.3 5.0		14.5 10.5				ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		9.0 6.0				ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		9.5 6.5				ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		12.5 8.5				ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		12 7.5				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	3.0 2.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.5			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	3.3 5.0	3.0 2.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	3.3 5.0	2.0 1.5			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5			ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	3.3 5.0	5.0 3.5			ns	3-6
t_{rec}	$\overline{CLR}$ to CP Recovery Time	3.3 5.0	2.0 1.5			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		110				MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	5.0		8.0				ns	3-6
t_{PHL}	Propagation Delay CP to O_n	5.0		8.0				ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0		12				ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0		7.5				ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0		8.0				ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		11				ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.5				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	2.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	5.0	2.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	5.0	1.5			ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	3.0			ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	3.5			ns	3-6
t_{rec}	$\overline{CLR}$ to CP Recovery Time	5.0	1.5			ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

MOTOROLA

Product Preview

9-Bit Transparent Latch

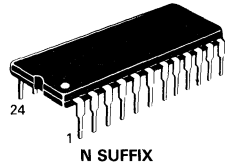
MC74AC843
MC74ACT843
MC74AC844
MC74ACT844

9-BIT TRANSPARENT LATCH

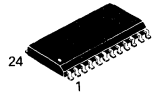
The MC74AC843/74ACT843 and MC74AC844/74ACT844 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity.

The MC74AC843/74ACT843 is functionally and pin compatible with AMD's AM29843.

- 'ACT843 and 'ACT844 Have TTL Compatible Inputs

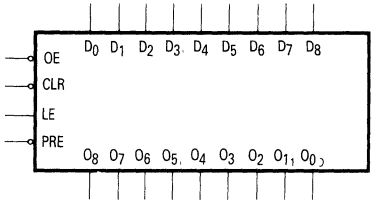


N SUFFIX
CASE 649-03
PLASTIC

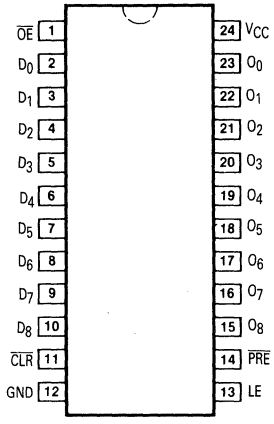


DW SUFFIX
CASE 751E-02
PLASTIC

LOGIC SYMBOL (MC74AC843/74ACT843)*



*The MC74AC844/74ACT844 has inverting outputs.



PIN NAMES

D_0–D_8	Data Inputs
O_0–O_8	Data Outputs (MC74AC843/74ACT843)
$\overline{O}_0$–$\overline{O}_8$	Data Outputs (MC74AC844/74ACT844)
$\overline{OE}$	Output Enable
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset

5

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

The MC74AC843/74ACT843 and MC74AC844/74ACT844 consist of nine D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

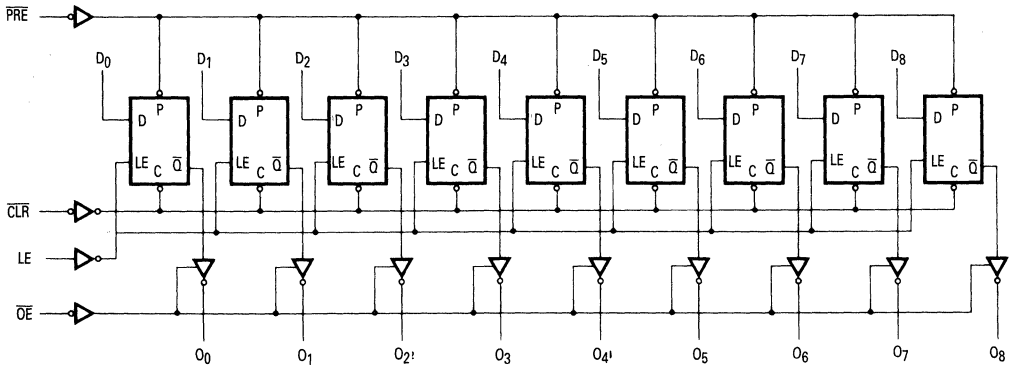
In addition to the LE and $\overline{OE}$ pins, the MC74AC843/74ACT843 and MC74AC844/74ACT844 have a Clear ($\overline{CLR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overides $\overline{CLR}$.

FUNCTION TABLE

Inputs					Internal	Outputs		Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D	Q	O ('843)	$\overline{O}$ ('844)	
H	H	H	H	L	L	Z	Z	High Z
H	H	H	H	H	H	Z	Z	High Z
H	H	H	L	X	NC	Z	Z	Latched
H	H	L	H	L	L	L	H	Transparent
H	H	L	H	H	H	H	L	Transparent
H	H	L	L	X	NC	NC	NC	Latched
H	L	L	X	X	H	H	L	Preset
L	H	L	X	X	L	L	H	Clear
L	L	L	X	X	H	H	L	Preset
L	H	H	L	X	L	Z	Z	Clear/High Z
H	L	H	L	X	H	Z	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

LOGIC DIAGRAM (MC74AC843/74ACT843)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The MC74AC844/74ACT844 also has the same logic diagram with inverting outputs.

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT843/844)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3 5.0		17 12				ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	3.3 5.0		16.5 11				ns	3-5
t_{PLH}	Propagation Delay LE to O_n	3.3 5.0		18.5 13				ns	3-6
t_{PHL}	Propagation Delay LE to O_n	3.3 5.0		17 12				ns	3-6
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	3.3 5.0		17 12				ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	3.3 5.0		17 12				ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		14.5 10				ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		11.5 8.0				ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		13 9.0				ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		13 9.0				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	4.0 2.5			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	0 0			ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.5			ns	3-6
t_w	$\overline{PRE}$ Pulse Width, LOW	3.3 5.0	4.0 2.5			ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	3.3 5.0	4.0 2.5			ns	3-6
t_{rec}	$\overline{PRE}$ Recovery Time	3.3 5.0	5.0 4.0			ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	3.3 5.0	5.0 4.0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0		12				ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	5.0		11				ns	3-5
t_{PLH}	Propagation Delay LE to O_n	5.0		13				ns	3-6
t_{PHL}	Propagation Delay LE to O_n	5.0		12				ns	3-6
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	5.0		12				ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0		12				ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0		10				ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0		8.0				ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0				ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	2.5			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0			ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.5			ns	3-6
t_w	$\overline{PRE}$ Pulse Width, LOW	5.0	2.5			ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	2.5			ns	3-6
t_{rec}	$\overline{PRE}$ Recovery Time	5.0	5.0			ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	5.0	5.0			ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC845
MC74ACT845
MC74AC846
MC74ACT846

Product Preview

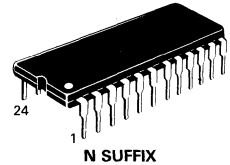
8-Bit Transparent Latch

8-BIT TRANSPARENT LATCH

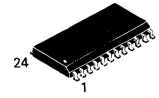
The MC74AC845/74ACT845 and MC74AC846/74ACT846 bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple $\overline{OE}$ controls.

The MC74AC845/74ACT845 is functionally and pin compatible with AMD's AM29845.

- 'ACT845 and 'ACT846 Have TTL Compatible Inputs

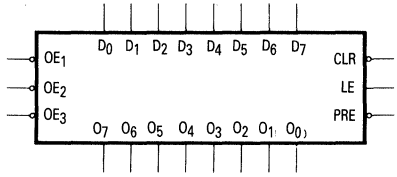


N SUFFIX
CASE 649-03
PLASTIC

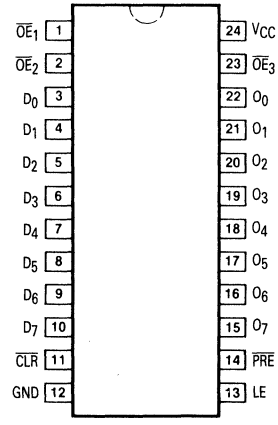


DW SUFFIX
CASE 751E-02
PLASTIC

LOGIC SYMBOL (MC74AC845/74ACT845)*



*The MC74AC846/74ACT846 has inverting outputs.



PIN NAMES

D_0–D_7	Data Inputs
O_0–O_7	Data Outputs (MC74AC845/74ACT845)
$\overline{O}_0$–$\overline{O}_7$	Data Outputs (MC74AC846/74ACT846)
$\overline{OE}_1$–$\overline{OE}_3$	Output Enables
$\overline{LE}$	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset

5

FUNCTIONAL DESCRIPTION

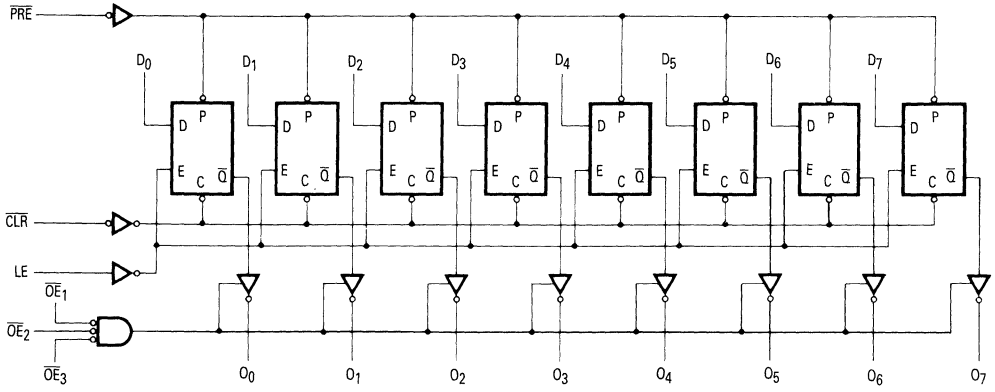
The MC74AC845/74ACT845 and MC74AC846/74ACT846 consist of eight D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) are LOW. When any one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the bus output is in the high impedance state.

FUNCTION TABLE

Inputs					Internal	Outputs		Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}_1$–$\overline{OE}_3$	LE	D	Q	O ('845)	$\overline{O}$ ('846)	
H	H	H	H	L	L	Z	Z	High Z
H	H	H	H	H	H	Z	Z	High Z
H	H	H	L	X	NC	Z	Z	Latched
H	H	L	H	L	L	L	H	Transparent
H	H	L	H	H	H	H	L	Transparent
H	H	L	L	X	NC	NC	NC	Latched
H	L	L	X	X	H	H	L	Preset
L	H	L	X	X	L	L	H	Clear
L	L	L	X	X	H	H	L	Preset
L	H	H	L	X	L	Z	Z	Clear/High Z
H	L	H	L	X	H	Z	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

LOGIC DIAGRAM (MC74AC845/74ACT845)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The MC74AC846/74ACT846 also has the same logic diagram with inverting outputs.

5

DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT845/846)	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3 5.0		17 12				ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	3.3 5.0		16.5 11				ns	3-5
t_{PLH}	Propagation Delay LE to O_n	3.3 5.0		18.5 13				ns	3-6
t_{PHL}	Propagation Delay LE to O_n	3.3 5.0		17 12				ns	3-6
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	3.3 5.0		17 12				ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	3.3 5.0		17 12				ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		14.5 10				ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		11.5 8.0				ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		13 9.0				ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		13 9.0				ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF		74AC T_A = −40°C to +85°C C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	4.0 2.5			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	0 0			ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.5			ns	3-6
t_w	$\overline{PRE}$ Pulse Width, LOW	3.3 5.0	4.0 2.5			ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	3.3 5.0	4.0 2.5			ns	3-6
t_{rec}	$\overline{PRE}$ Recovery Time	3.3 5.0	5.0 4.0			ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	3.3 5.0	5.0 4.0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF			74ACT T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0		12				ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	5.0		11				ns	3-5
t_{PLH}	Propagation Delay LE to O_n	5.0		13.5				ns	3-6
t_{PHL}	Propagation Delay LE to O_n	5.0		12				ns	3-6
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	5.0		12				ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0		12				ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0		10				ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0		18				ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0				ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0				ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF		74ACT T_A = −40°C to +85°C, C_L = 50 pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	2.5			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0			ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.5			ns	3-6
t_w	$\overline{PRE}$ Pulse Width, LOW	5.0	2.5			ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	2.5			ns	3-6
t_{rec}	$\overline{PRE}$ Recovery Time	5.0	5.0			ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	5.0	5.0			ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance		pF	V_{CC} = 5.0 V

5

MOTOROLA

MC74AC4020

Product Preview

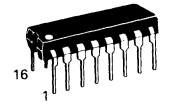
14-Stage Binary Ripple Counter

14-STAGE BINARY RIPPLE COUNTER

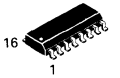
The MC74AC4020 consists of 14 master-slave flip-flops with 12 stages brought out to pins. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the MC74AC4020 for some designs.

- Outputs Source/Sink 24 mA
- Operating Voltage Range: 2.0 to 6.0 V
- High Noise Immunity

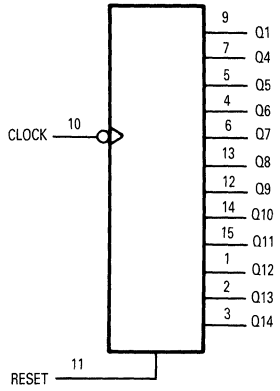


N SUFFIX
CASE 648-08
PLASTIC

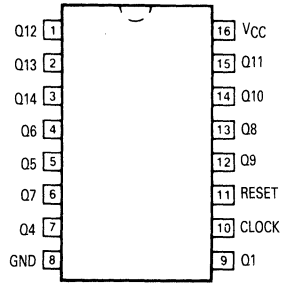


D SUFFIX
CASE 751B-03
PLASTIC

LOGIC DIAGRAM



PIN 16 = V_{CC}
PIN 8 = GND



FUNCTION TABLE

Clock	Reset	Output State
⌐	L	No Change
¬	L	Advance to next state
X	H	All Outputs are low

5

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOTOROLA

MC74AC4040

Product Preview

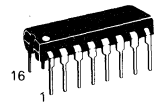
12-Stage Binary Ripple Counter

12-STAGE BINARY RIPPLE COUNTER

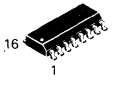
The MC74AC4040 consists of 12 master-slave flip-flops. The output of each flip-flop feeds the next and the frequency at each output is half that of the preceding one. The state of the counter advances on the negative-going edge of the Clock input. Reset is asynchronous and active-high.

State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and may have to be gated with the Clock of the MC74AC4040 for some designs.

- Outputs Source/Sink 24 mA
- Operating Voltage Range: 2.0 to 6.0 V
- High Noise Immunity

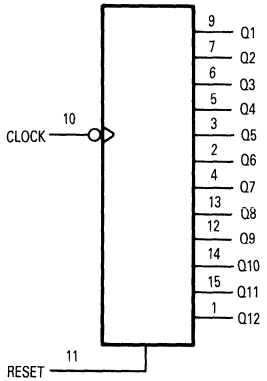


N SUFFIX
CASE 648-08
PLASTIC

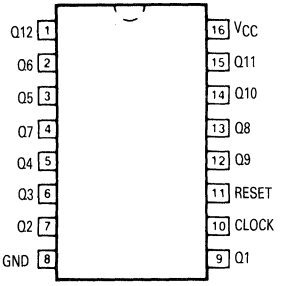


D SUFFIX
CASE 751B-03
PLASTIC

LOGIC DIAGRAM



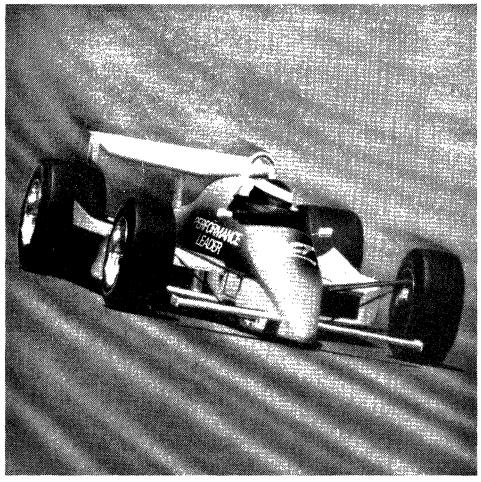
PIN 16 = V_{CC}
PIN 8 = GND



FUNCTION TABLE

Clock	Reset	Output State
⌐‾	L	No Change
‾⌐	L	Advance to next state
X	H	All Outputs are low

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.



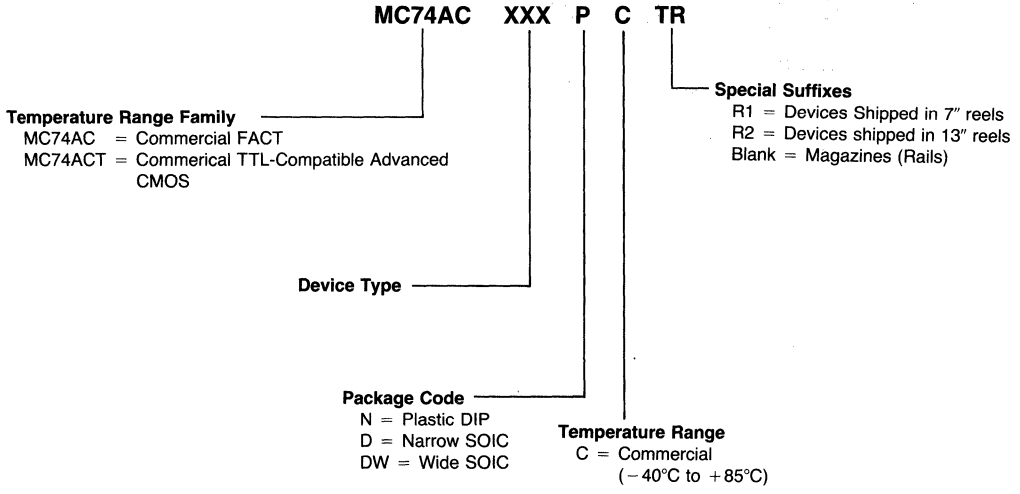
Package Outlines and Ordering Information

6

Package Outlines and Ordering Information

Ordering Information

The Product Index and Selection Guide in Section 1 lists only the basic device numbers. This basic number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Package Outlines

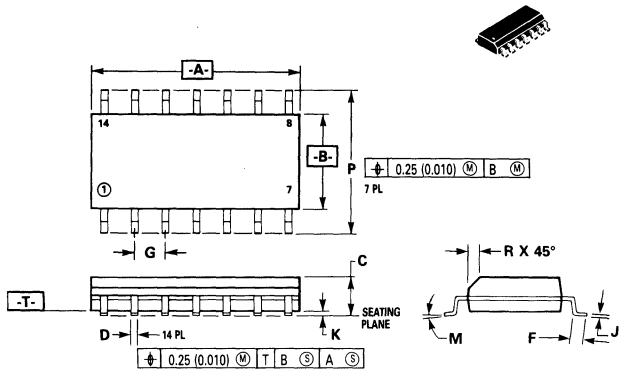
The package outlines indicated above are shown in the detailed outline drawings in this section.

6

PACKAGE OUTLINES

SOIC

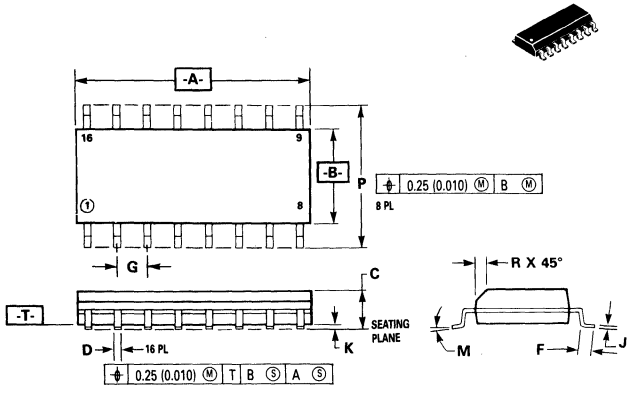
Case 751A-02 D Suffix
14-Pin Plastic
SO-14



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

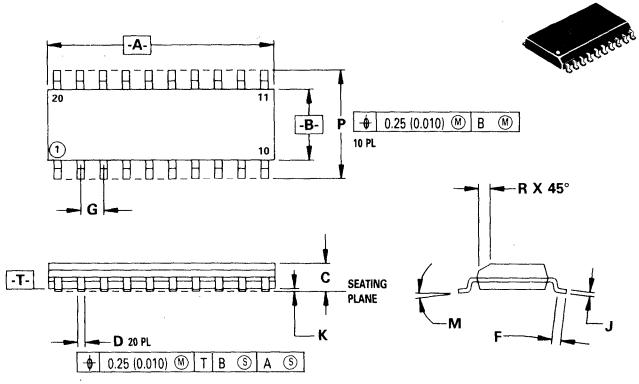
Case 751B-03 D Suffix
16-Pin Plastic
SO-16



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

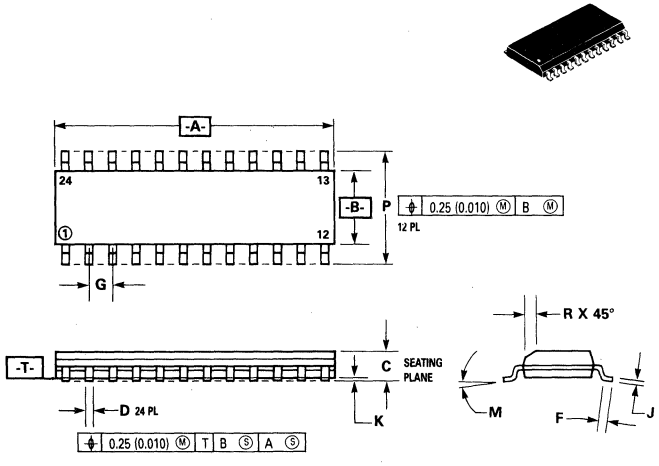
Case 751D-03 DW Suffix
20-Pin Plastic
SO-20



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Case 751E-02 DW Suffix
24-Pin Plastic
SO-24

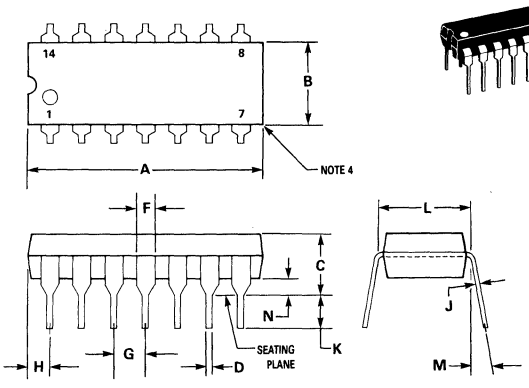


NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.50	0.601	0.610
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

PLASTIC DUAL-IN-LINE

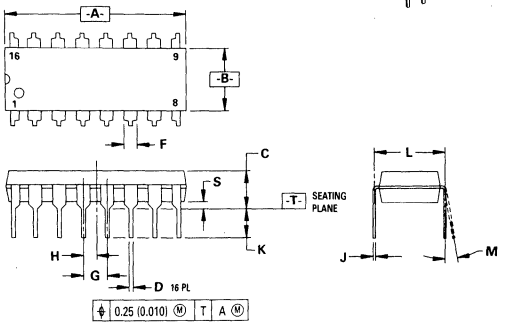
Case 646-06 N Suffix
14-Pin Plastic

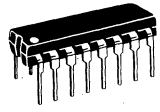


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

Case 648-08 N Suffix
16-Pin Plastic



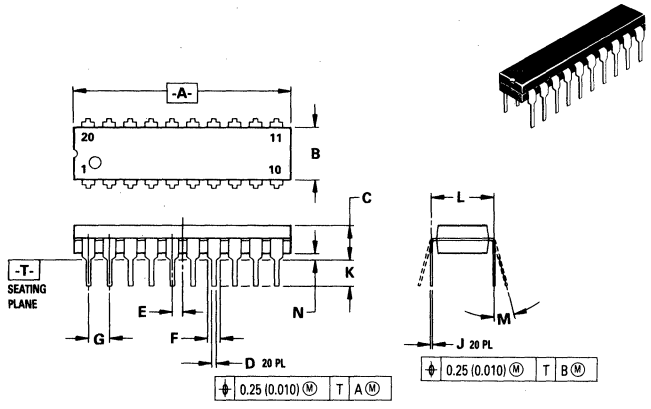


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

PLASTIC DUAL-IN-LINE (continued)

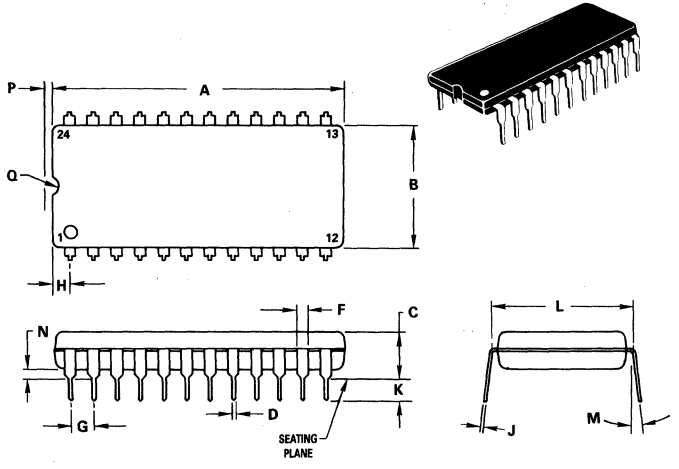
Case 738-03 N Suffix
20-Pin Plastic



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

Case 649-03 N Suffix
24-Pin Plastic



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

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