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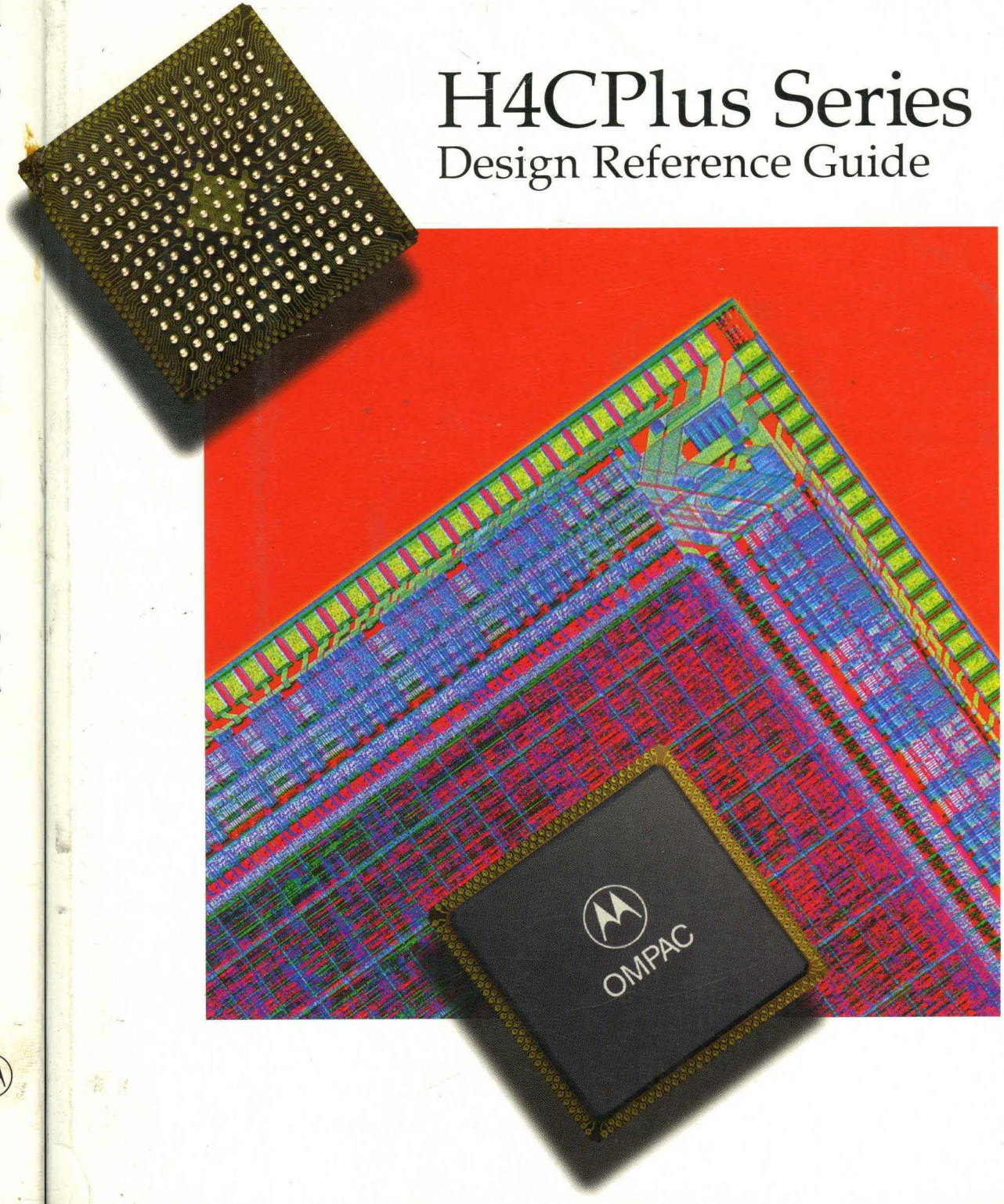
REV. 1

MOTOROLA

H4CPlus Series
Design Reference Guide



H4CPlus Series
Design Reference Guide

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MOTOROLA

H4CPlus™ Series CMOS Gate Arrays Design Reference Guide

Advanced Information

Written and Prepared by

Loren Kinsey
ASIC High-Performance Application Engineer

Clarence Nakata
ASIC CMOS Applications Engineer

James Grothe
ASIC CAD Application Engineer

Jon Houghten
ASIC High-Performance Application Engineer

JoEllen Brock
ASIC CMOS Application Technical Writer

This Reference Guide may be used alone or in conjunction with H4CPlus application notes. The appendix at the back of this manual contains application notes AN1500, AN1514 and AN1522. For additional copies of these or other H4CPlus application notes please contact your Motorola representative.

Revision Status:
This July, 1994 revision is released in conjunction with OACS 2.3 and OACS 3.15M.

New Macros in this release include:

Special I/O's, Special JTAG I/O's, and all JTAG macros. Also added were two new RAM macros and two D Flip-Flop macros.

Changes or Updates:

Chapters 1-3 were updated or rewritten to correspond with OACS 2.3 and OACS 3.15M offerings.
Added three new Arrays and two new packages in Section 4.
$Theta_{JA}$ numbers in Packaging Section were added and updated.
Updated all tables in Section 7 with latest technology file.
Updated Electrical Section.
Corrected and updated Index.
Added Appendix (Application notes).
General cosmetic alterations have been completed throughout this revision.

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Other major contributors include Frank Reid, New Product Manager, Dave Pivin, CMOS Applications Manager, Fred Devine, Graphic Illustrator, Peter Economopoulos, David Crohn and the rest of the ASIC CMOS design team, and the H4CPlus Product Engineering group.

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PRODUCT DESCRIPTION

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1 PRODUCT DESCRIPTION

SECTION 1. H4CPlus™ SERIES PRODUCT PROFILE

1.1 DESCRIPTION

The H4CPlus Series arrays feature 3.3V, 5V and mixed-voltage capability, high-speed interfaces, and an analog PLL for chip-to-chip clock skew management. The gate length has been reduced to 0.65 µm Leff to provide optimum performance in a mixed-voltage environment.

The low- and mixed-voltage capability lets designers customize the H4CPlus arrays to fit power and performance needs. All H4CPlus arrays have dual V_{DD} rails with custom power/ground bus tying to power input and output buffers for all 3.3V, all 5V or a mix of system voltage levels. Additionally, the core of the arrays may be powered by either 3.3V or 5V.

New, high-speed CMTL™, GTL™, and PECL macros offer enhanced chip-to-chip communication. Motorola's CMTL (Current Mode Transceiver Logic™) interface enables differential operation up to 400 MHz and up to 200MHz for single-ended configurations with active terminations. GTL inputs and outputs, and a PECL input is also available for additional interfacing options.

Also, new PCI (Peripheral Component Interface) compliant I/O buffers are available in 5V and 3.3V versions.

Each array may have two Analog PLLs, one embedded into each of two corners of the die, for on-chip clock signals up to 125 MHz with only 250ps jitter and includes on-chip clock synthesis.

Other design features include metal RAMs, ESSD/LSSD scan macros and JTAG boundary scan macros.

H4CPlus Series Features

- 0.65 µm Leff, channelless, 3-metal gate arrays
- Typical gate delay of 280 ps at 5V and 420 ps at 3.3V (NAN2, FO=2)
- Low power, 1µW/gate/MHz (3.3V), 3µW/gate/MHz (5V)
- 3.3V, 5V or mixed system and core voltage levels
- Custom power bus tying and ground bus isolation for special power needs
- Configurable I/O cell supports 2 to 24 mA, up to 48mA using dual I/O cells
- PCI compliant 5V and 3.3V I/O buffers
- High-speed CMTL interface
- GTL I/O and PECL input macros
- Analog PLL for clocks up to 125MHz
- JTAG 1149.1 boundary scan
- ESSD/LSSD scan macros
- Single-, dual-, and quad-port metal SRAMs
- Powerful design environment using Mentor Graphics' Falcon, Cadence's point tools, and Motorola design tools
- OMPAC™ ball-grid array, MicroCool™, and PQFP packaging

Table 1-1 H4CPlus Series Arrays

Array Name	Available Gates	Die Size (mils/side)	Die Pads	I/O Cells	Package Pins
H4CP028	28,400	239	176	160	128-169
H4CP048	48,100	287	216	208	128-225
H4CP075	74,520	337	256	256	128-225
H4CP109	109,368	391	304	312	160-313
H4CP146	145,544	438	344	360	160-313
H4CP178	178,000	476	376	400	160-313

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1.2 HIGH-PERFORMANCE TECHNOLOGY

The H4CPlus Series uses a self-aligned twin tub process in which n-type and p-type well implants are driven together to form deep, balanced wells to improve short n-channel transistor performance, see Figure1-1. A lightly doped drain (LDD) diffusion is used to reduce hot carrier injection effects caused by a high electric field in the short channel transistors. A highly-reliable multilayer metal structure is achieved by a planarization technique using tapered contacts and vias.

The combination of a small feature size and a thin gate oxide coating provides both high gate density and low power dissipation. The typical power dissipation for internal gates is only 1µW/gate/MHz at 3.3V and 3µW/gate/MHz at 5.0V with a load of 0.05 pF (fanout = 1).

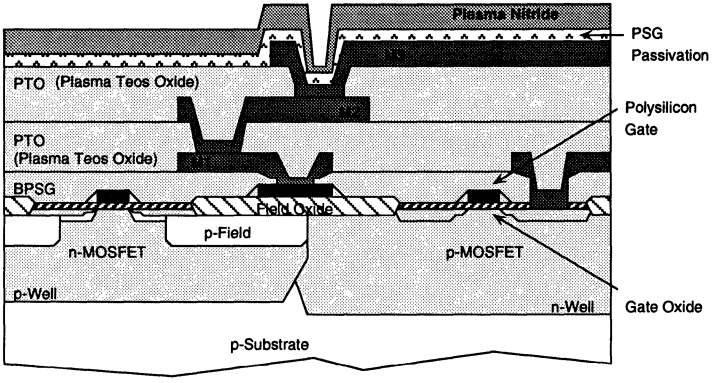

Figure 1-1 H4CPlus Series CMOS Device Cross-Section

1.2.1 The H4CPlus Primary Cell

The primary cell consists of four pairs of n- and p-type transistors. The transistors are the same size to optimize both gate density and routability. The primary cell is used to configure all H4CPlus Series macrocells.

Figure1-2 shows half of a primary cell (two p-type and two n-type transistors) configured in a 2-input NAND gate (NAN2). The typical gate delay for a 2-input NAND with a fanout of 2 is 280 ps at 5V and 420 ps at 3.3V.

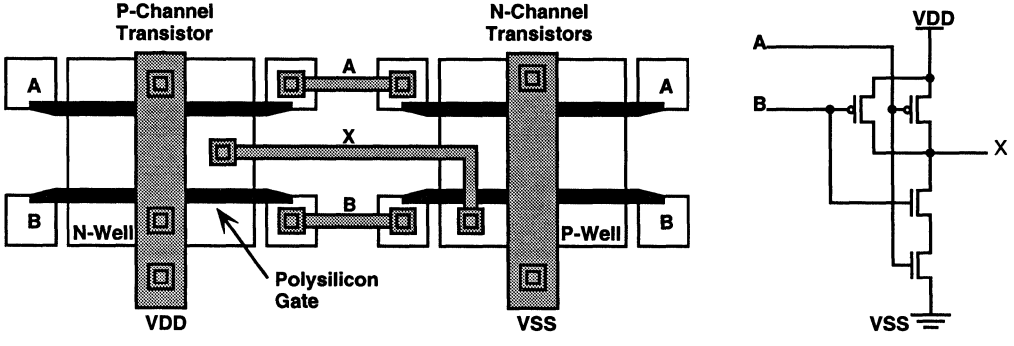

Figure 1-2 2-Input NAND Gate Implemented Within Half of a Primary Cell

1.2.2 Triple-Layer Metal Routing

A triple-layer metal (TLM) structure provides superior routing access to configure and connect macrocells and distribute power and ground, see Figure1-3.

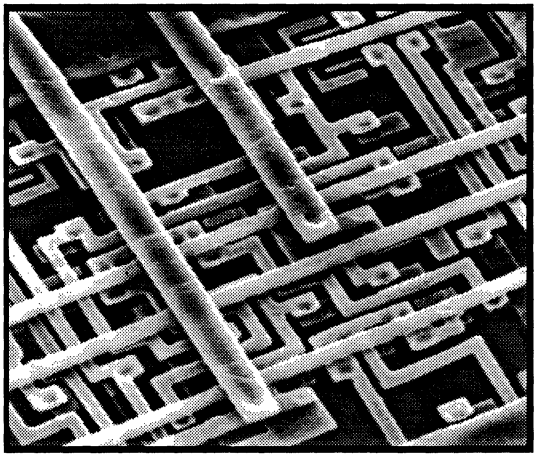

Figure 1-3 Triple-Layer Metallization

One important benefit of TLM routing is improved routability for higher gate utilization. TLM also provides improved clock distribution by moving the clock signals to the top metal layer where the capacitance per unit length is 30% less than the lower metal layers due to a thicker dielectric layer. In addition, TLM reduces interconnect delays typically by 10% with shorter interconnect lengths and improves power distribution.

- **Gate Ensemble™ Place and Route**

The design of the routing layers is accomplished with Cadence's Gate Ensemble place and route system. Some of Gate Ensemble's capabilities include timing driven layout (net and path constrained), soft/firm grouping of macros, clock-tree synthesis, incremental layout changes, and highly accurate distributed RC calculations. In addition, the power-bus router automatically uses single-, double-, or quadruple-width power tracks to optimize performance while minimizing spent routing channels where needed.

- **PrediX™ Floorplanning**

PrediX is Motorola's patented floorplanning and routability analysis tool that enables designers to predict and improve routing congestion especially in complex circuits. PrediX is easy to use and interfaces with Gate Ensemble to assure the desired results in layout and timing.

1.3 THE H4CPlus SERIES LIBRARY

The H4CPlus Series library is an optimized set of macros containing a complete suite of I/O functions, combinatorial and sequential functions. Many basic logic functions come in several versions including standard/high-drive capacity and scan/non-scan to provide you with the widest choice of functions.

1.3.1 I/O Functions

The H4CPlus Series I/O cells, see Figure1-4, are configurable into inputs, outputs, bidirectionals, oscillators, JTAG I/O, CMTL, GTL, and PECL interfaces. The standard CMOS, TTL, slew control, 3-state, open-drain and Schmitt-trigger I/O functions are available as well. The I/O cell also provides pull-up and pull-down resistors, active terminations for CMTL, voltage translation between 3.3V and 5V levels, and power and ground connections.

- **3.3V, 5V and Mixed-Voltage I/O**

The I/O cell can support any combination of 3.3V and 5V in system and core voltage requirements. This is accomplished with a voltage translator to translate between logic levels based on the system and core voltages, see Figure1-4.

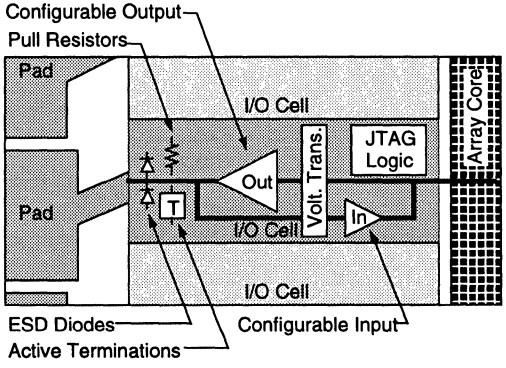

Figure 1-4 H4CPlus Series I/O Cell

Low-voltage interfaces are important in systems requiring low-power since most of the power dissipated in ICs occurs in the outputs. However, performance is usually sacrificed for lower power. The H4CPlus Series I/O offers all combinations of system

and core voltage levels to meet power and performance goals. For example, the ONL8 is a 12mA output for a 3.3V/3.3V (3.3V core with 3.3V Input/Output. It's power dissipation is about 56% less than the 5V/5V ON8 output, but it is 41% slower at 100pF, see Figure1-5. The ONLX8 (3.3V/5V) and the ONX8 (5V/3.3V) is moderately slower than the ON8.

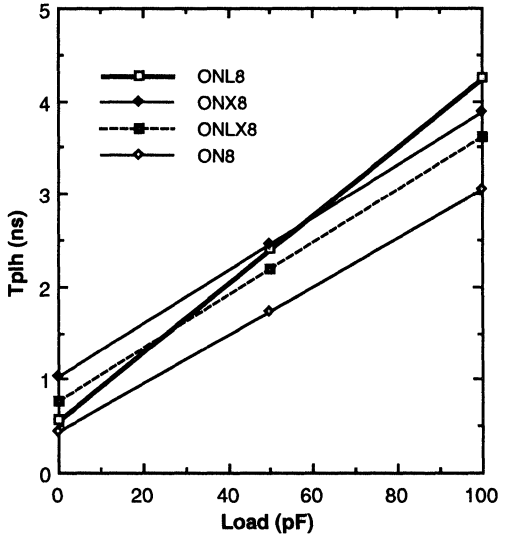

Figure 1-5 Performance Comparison of 12mA Output Buffers

- **PCI I/O Buffers**

PCI (Peripheral Component Interface) is emerging as a new high performance local bus architecture. It is a highly flexible, processor independent architecture that has applications in low- to high-end desktop, server and low-power, mobile systems. Motorola offers PCI compliant 3.3V and 5V I/O buffers to allow connection of H4CPlus arrays to any PCI local bus "speedway".

- **CMTL Interface**

Motorola's new Current Mode Transceiver Logic (CMTL) buffers provide a low-power alternative to high-speed interfaces. On-chip active termination allows for the lowest possible power dissipation while enhancing the performance. They may also be configured with external 50Ω terminations in bi-directional or PECL applications. The flexibility of this design allows simple, direct interfaces to ECLinPS or other ECL-level chips operating in a PECL environment with standard terminations.

Applications for CMTL range from video to telecommunications to tightly-coupled processor/cache interfaces. I/O pair delay is less than 2ns worst-case. Systems are no longer limited by slow buffers for critical chip-to-chip paths.

- **GTL Interface**

GTL is able to drive system backplanes while still occupying only a single I/O site for 50Ω and two sites for 25Ω. This licensed implementation provides a high-performance bus interface driver for use in RISC/CISC processor applications at system bus speeds well in excess of 50MHz.

- **PECL Input Buffer**

Standard Pseudo ECL voltage inputs created by ECL logic functions or special clock control and distribution chips can be brought directly into the chip in either differential or single-ended configurations.

- **JTAG Boundary Scan I/O**

The H4CPlus Series I/O cell has JTAG logic built-in to minimize the impact on performance and gate overhead. Also, the JTAG control and scan data signals between I/Os are connected automatically by design.

- **Selectable Output Drive**

Up to 24 mA is available from a single I/O cell, two cells may be paralleled for up to 48 mA drive from a single output pin. (All JTAG outputs and bidirectionals are not parallelable, but have higher current capacity versions available.) Unused output drivers may also be used to drive highly loaded internal signals such as clock networks.

- **Slew Rate Control**

Slew rate control outputs are available to reduce system SSO noise as well as over-shoot and undershoot of output signals caused by fast rise and fall times. All 4 and 8 mA output buffers have a moderate (10%) and slow (30%) slew control version.

- **Oscillators**

Three different oscillator I/O macros are available on the H4CPlus Series arrays: non-inverting buffer, clock buffer, and Schmitt trigger versions. These macros can be configured for ceramic resonators from 32 KHz to above 60 MHz with quartz crystals. Please see Section 3.3.5 for details on using these oscillator I/O macros.

1.3.2 Macrocells

The mature H4C Series library has been optimized to a set of the most popular and efficient functions, including several new scan macros, for the H4CPlus library. All H4CPlus macrocells have been characterized at typical operating conditions for 3.3V and 5.0V operation for the highest modelling accuracy. A summary of available macrocell types is shown in Table 1-2.

Table 1-2 Summary of Macrocells

Library Functions	Macros
AND	7
NAND	11
OR	7
NOR	11
EXOR	3
EXNOR	2
A/N, A/O, O/N, O/A	22
Inverting Buffer	9
Non-Inverting Buffer	8
3-State Buffer	8
D Flip-Flop	21
Latch	11
Multiplexer	13
Decoder	4
Arithmetic	9
Misc.	5

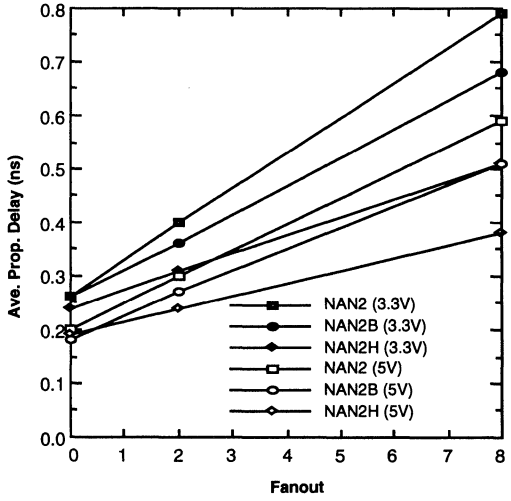

Figure 1-6 Performance of NAN2 Macros

Several types of macrocells come in high-drive, balanced slew-rate, or complementary output versions. High-drive versions provide improved performance on nets with high fanouts. Balanced slew rate versions of macrocells provide more symmetrical rise and fall slew rates with slightly better performance than standard macros. For example, Figure1-6 shows the NAN2H at 3.3V and 5V to have better performance than the balanced and standard-drive NAN2.

Table 1-3 Summary of Special Functions

Special Function	Macros
Metallized SRAMs	24
Analog PLL	1
Internal JTAG	6

- **Metallized SRAMs**

The metal SRAMs are a family of asynchronous single, dual, and quad-port blocks up to 2304 bits. These RAMs are gate array based (not diffused), and are an excellent choice for small memory block applications such as "scratch-pads" or FIFOs.

Table 1-4 Sizes of Metallized SRAMs

H4CPlus Series Metallized SRAM Sizes		
Single-Port	Dual-Port	Quad-Port
8x8	8x9	16x18
8x18	8x18	16x36
16x8	8x36	32x18
16x18	8x72	32x36
16x36	16x9	
32x8	16x18	
32x18	16x36	
32x36	16x72	
64x18	32x9	
64x36	32x18	
	32x36	
	32x72	

1.4 SPECIAL DESIGN FEATURES

The H4CPlus Series offers solutions to many of today's design problems. Increasing application complexities place higher demands on performance, clock skew management, testability, I/O capability and workstation based design environments. This section describes some of the special features of the H4CPlus Series that provide solutions to these problems.

1.4.1 Design for Testability

The time and cost to test an ASIC increases exponentially as the complexity and size of the ASIC grows. Using a design for test (DFT) methodology allows large, complex ASICs to be efficiently and economically tested.

Motorola supports several DFT methodologies, including ESSD/LSSD scan and JTAG boundary scan

- **ESSD/LSSD Scan**

Motorola offers Edge Sensitive Scan Design and Level Sensitive Scan Design (ESSD/LSSD) versions of flip-flops, latches and other functions in the H4CPlus Series library.

- **JTAG Boundary Scan**

Motorola's JTAG I/O and JTAG control macrocells are designed to conform to the IEEE 1149.1 JTAG boundary scan specification. The JTAG I/O macrocells are designed to optimize performance and minimize silicon overhead by embedding all sequential and multiplexing logic within the I/O sites of the array.

1.4.2 Clock Distribution and Management

ASICs are becoming an integral part of system design and are regularly found interfacing with multiple chips including other ASICs, microprocessors and memories. Optimizing performance of such systems rests on maximizing communication between chips using synchronous interfaces. Clock skew control and distribution, both on-chip and between chips, is of critical importance.The Motorola solution to clock management is to use the clock tree to control skew on-chip and an analog PLL to control clock skew between ASICs.

- **Clock Distribution**

Motorola offers clock tree synthesis during layout to build balanced clock distribution networks or clock trees. Clock trees are load-balanced networks that synchronizes clock signals for all on-chip sequential elements. Clock trees have a minimal effect on design routability, critical data paths, timing driven layout and floorplanning.

- **Analog Phase Locked Loop**

Motorola's analog PLL (APLL) may be used to synchronize multiple ASICs up to 125MHz (VCO/2). The APLL is an embedded function and requires 6 (CMOS) or 7 (PECL) pins for VCO control, reference frequency, test, and power signals (see Section 3.8). No external filters are needed.

An APLL is diffused into two opposite corners of all H4CPlus arrays. No area within the core of the array is used so the APLL does not reduce the total gate count.

THE OPEN ARCHITECTURE CAD SYSTEM

2

2 THE OPEN ARCHITECTURE CAD SYSTEM

SECTION 2. THE OPEN ARCHITECTURE CAD SYSTEM

2.1 INTRODUCTION

Motorola is in partnership with several leading CAD/CAE vendors to integrate the best design tools in the industry into one system. In many cases, Motorola has been instrumental in the definition and refining of key third-party design tools.

To satisfy specific CAD requirements, Motorola has developed several design tools to perform netlisting and translation, rule checking, delay and timing calculation, fault grading and automatic test pattern generation, floorplanning, test vector analysis and processing.

This section briefly describes Motorola's OACS ASIC design system and design options.

2.2 THE OPEN ARCHITECHTURE CAD SYSTEM

The Open Architecture CAD System (OACS) offers a highly versatile and powerful design environment for the design of Motorola's H4CPlus, H4C Series, and HDC Series CMOS arrays. The system integrates several of the industry's most powerful design tools with Motorola's high-performance tools into a standard EDIF based CAD environment. The release of this Design Reference Guide corresponds to the release of two major versions of OACS: OACS 2.3 and OACS 3.15M.

OACS 2.3 is Motorola's point tool CAE solution based on Cadence's Concept™ schematic editor, Synopsys' synthesis tools, and Cadence's Verilog™ logic simulator.

OACS 3.15M is Motorola's framework based CAE solution using Mentor Graphics' Falcon™ Framework. This solution provides support of Mentor Graphics' design entry tools and QuickSim II logic simulation.

The following sections will discuss the OACS design flow and how each solution fits into the flow.

OACS 2.3 and 3.15M Features

- EDIF 2.0.0 backplane to provide an open design environment
- Supports the following third-party design tools:
  - Synopsys' Design Compiler™, DesignWare™, HDL Compiler™ and Test Compiler™ (optional)
  - Cadence's Concept™ schematic capture (2.3)
  - Cadence's Verilog XL™ simulator and Veritime™ static timing analysis (2.3)
  - Quad Design's MOTIVE® static timing analysis (optional) (2.3)
  - Mentor Graphics' schematic capture Design Architect
  - Mentor Graphics' FALCON™ FRAMEWORK (3.15M)
  - Mentor Graphics' QUICKSIM II™ simulator and QUICKPATH™ static timing analysis (3.15M)
  - Mentor Graphics' AutoLogic™ design synthesis tool (3.15M)
- Motorola design tools:
  - DECAL™ delay calculator
  - FeliX™ diffused SRAM compiler (optional)
  - Mustang™ automatic test pattern generation (optional)
  - TestPAS™ test vector validation and extraction
  - ERC and MARV comprehensive electrical and manufacturing rules checking
  - PrediX™ floorplanning, routability prediction, and placement tool (optional)
- Testability support: ESSD/LSSD scan, JTAG boundary scan, BIST, and scan synthesis
- Sophisticated delay and timing limits calculations for accurate simulation and timing analysis
  - Estimated and actual (back-annotated) wire capacitances
  - Includes intrinsic, rise/fall time, output pin loading and distributed RC delays
  - Continuous process, temperature, and voltage variation
- Clock skew management: clock-tree synthesis, PLL, timing driven layout
- Supports multiple technologies: HDCMOS, H4C, H4C-CDA-1C, H4CPlus
- Supported on HP9000/7XX and SUN 4 Sparc® workstations

2.3 THE OACS DESIGN FLOW

From the conception of a design to its fabrication, the OACS design flow is accurate, efficient, and flexible. The design flow has three basic phases (see Figure 2-1): design capture and verification, physical design, and post-layout design verification.

2.3.1 Design Capture and Verification

- Building the Design Directory

The first step is to build the OACS design directory structure using CREATE_BLOCK. The directory structure is created automatically in seconds, specific company and design related information is entered for DESIGN_INFO.

- Design Capture and Synthesis

Next, there is a choice of either schematic capture or logic synthesis to enter the design into the OACS environment. The design can be entered in schematic form using either Mentor Graphics' DESIGN ARCHITECT design entry tool or Cadence's Concept schematic editor. If synthesis is used, the design can be described in Verilog hardware description language, industry standard VHDL, or truth tables for input to Synopsys' synthesis tools. Based on the OACS version being used, Synopsys either transfers the design to Mentor Graphics' EDDM database via Synopsys' Falcon Integrator™ or creates a basic EDIF netlist which specifies the Motorola macrocells and describes their connectivity in the design. In the latter case, EDIFMERGE processes this basic EDIF netlist to include additional information such as cell properties and package pin assignments. The design VHDL description can also be input to Mentor Graphics' AutoLogic for design compilation and EDDM database creation.

If the design requires memories they can be selected from several single-, dual-, and quad-port SRAMs in the H4CPlus Series library.

- Netlist Generation

NETLIST accepts schematic data or an EDIF netlist from EDIFMERGE to translate designs into an EDIF netlist, Verilog netlist, control files, and templates of other necessary files as needed by each of the OACS versions.

- Netlist Verification

After the EDIF netlist is ready, ERC scans the netlist and checks for violations in connection, I/O, and package pin rules.

Table 2-1 OACS DESIGN TOOLS

OACS Tools	Function
CREATE_BLOCK	Creates OACS design directory and invokes DESIGN_INFO
DESIGN_INFO	Collects design-specific information
DESIGN ARCHITECT	Invokes Mentor's DESIGN ARCHITECT design entry tool
ASIC_CONCEPT	Invokes Cadence's Concept schematic capture tool
SYNOPSYS	Invokes Synopsys logic compiler
EDIFMERGE	Appends Motorola specific properties to Synopsys connected EDIF netlist
NETLIST	Creates netlists and control files from schematic or EDIF descriptions
ERC	Checks netlist for violations
DECAL	Calculates delay and timing data
QUICKSIM II	Invokes Mentor Graphics' QuickSim II simulator
ASIC_VERILOG	Invokes Cadence's Verilog simulator
QUICKPATH	Invokes Mentor Graphics' QuickPath Static timing analysis tool
ASIC VERITIME	Invokes Cadence's Veritime static timing analysis tool
MUSTANG	Fault detection and automatic test pattern generation
MOTIVE	Quad Design timing analysis tool
TestPAS	Test vector merging and verification
ASIC_ORV	Checks data file and tool run sequence
ASIC_RELEASE	Automatically writes design data to tape
PrediX	Motorola's floorplanning and routability prediction tool

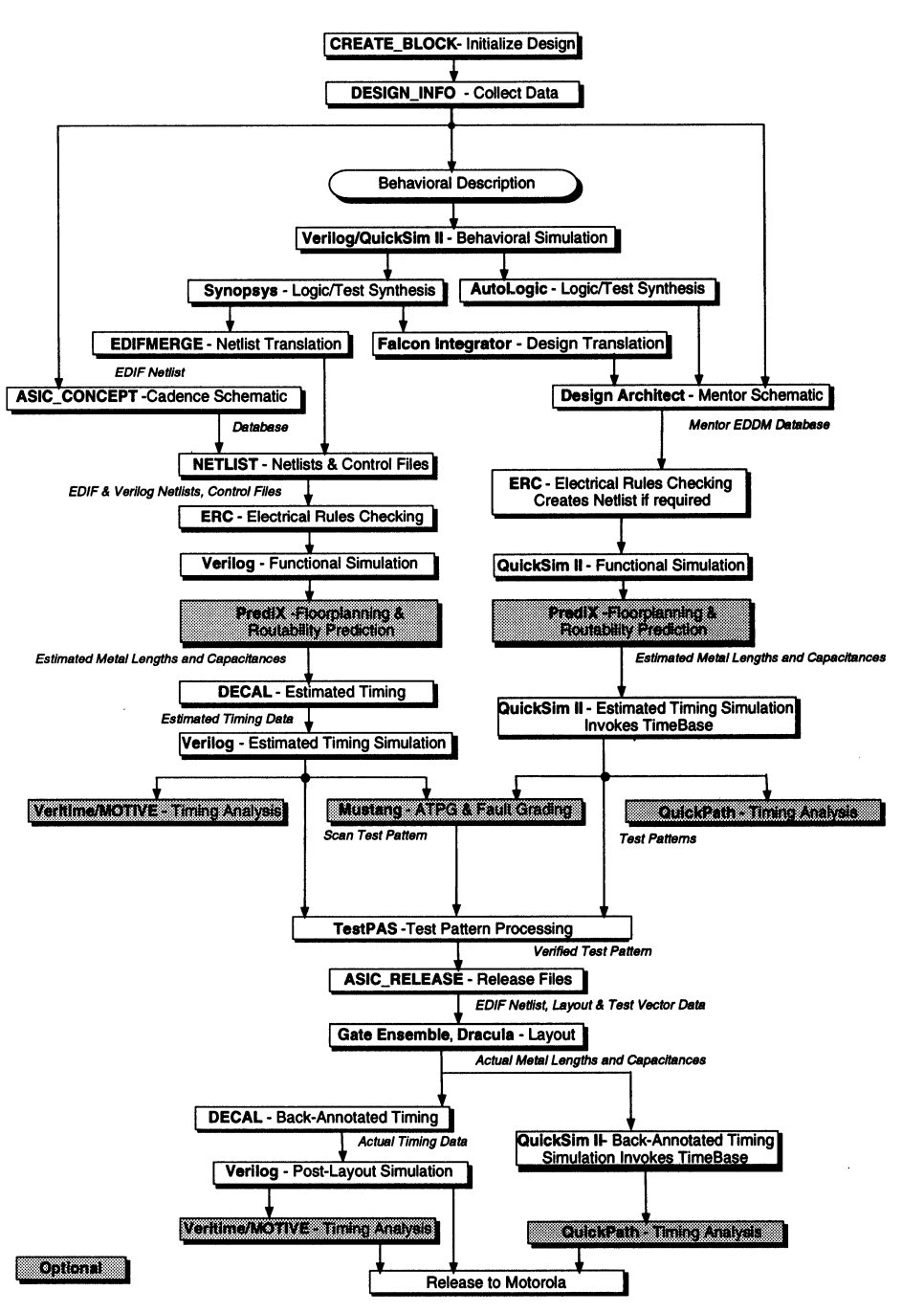

Figure 2-1 OACS Design Flow

- Pre-Layout Simulation and Timing Analysis

Before releasing designs for layout best and worst-case simulations must be performed using Verilog or QuickSim II. For OACS 2.3, DECAL calculates delay and timing data based on intrinsic delays, net and gate loading, slew rate effects, and net RC delays. For OACS 3.15M, TimeBase™ (Mentor Graphics' Central Delay Calculator) is invoked by QuickSim II to calculate the delay and timing data based on the same information as DECAL.

- Static Timing Analysis

Static timing analysis is optional and is supported on Mentor Graphics' QuickPath, Cadence's Veritime, and Quad Design's MOTIVE. Also, automatic test pattern generation and fault grading is available on Motorola's Mustang tool.

- Test Vector Processing

TestPAS is a system of tools that process your simulation and scan test vectors into vectors that are compatible with automatic IC test equipment.

2.3.2 Physical Design

- Floorplanning and Placement

Prior to release, designer's may elect to floorplan their design to optimize for density or performance. PrediX, Motorola's floorplanning tool, allows experimentation with various floorplans to achieve gate density and performance goals. In addition, the designer may elect to use PrediX to place design components onto the base array to improve the accuracy of the pre-route delay estimation.

- Routability Prediction

A Unique feature in PrediX is it's patented routability prediction capabilities. PrediX, void of floorplan and/or placement information, will give the designer immediate insight into the designs routability

- Place and Route

Physical design is performed by Motorola's Option Development Engineers (ODE). An ODE is dedicated to each option and works directly with designers to satisfy layout requirements. Options such as timing driven layout and clock tree synthesis are available to optimize silicon performance. Upon completion of the physical design, back-annotation data of actual wire routing lengths and RC parasitics are provided for post-layout verification and simulation.

2.3.3 Post-Layout Design Verification

The post-layout design verification is performed by the customer to assure that the physical layout of the design satisfies all performance and timing requirements. Post-layout simulations use the actual wire lengths and RC parasitics obtained from the physical layout to provide simulations that represent the circuit's behavior in silicon. Following a successful post-layout design verification and customer sign-off, Motorola begins manufacturing of the ASIC design.

2.4 OACS TECHNICAL SUPPORT

Motorola produces a complete set of manuals and provides direct access to technical assistance to support the OACS tools.

Accompanying the OACS software are five manuals which provide all the information needed to complete a successful ASIC design.

Motorola also offers on-line technical assistance from several regional design centers (RDCs) and CAD applications engineers to handle any problems. The RDC engineers are fully trained in the OACS software and third-party tools as well as in ASIC design.

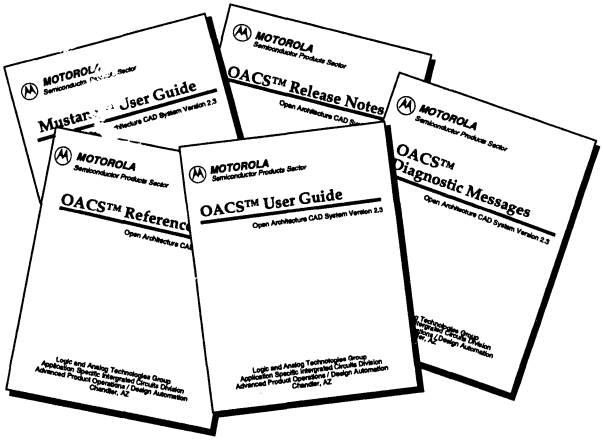

Figure 2-2 OACS 2.3 and 3.15M Documentation

DESIGN CONSIDERATIONS

3

3 DESIGN CONSIDERATIONS

SECTION 3. DESIGN CONSIDERATIONS

3.1 INTRODUCTION

This chapter describes the special features and design considerations of the H4CPlus Series arrays including I/O macros, power and ground requirements, power estimation, delay calculations, metallized SRAMs, and operation and use of the analog PLL. Where applicable, supporting documents such as application notes are cited for additional information.

3.2 GENERAL DESIGN INFORMATION

Core macro cells may be powered by either of the two basic supply voltages 3.3 V or 5.0 V. There is no core power segmentation. All core macro cells are fully characterized at both voltages. Core macros use the same name for both voltages, for example, a two-input "AND" gate would use the macro name, AND2, regardless of the selected supply voltage. I/O macros all have unique names. Not all I/O macros can be used with a single core voltage. When a core voltage is selected, a library containing the appropriate set of core macro switching characteristics is selected and the appropriate subset of I/O macros is then available for use. For a 5.0 V core (4.0-5.5 V), the library is H4CP5; for a 3.3 V core (2.7-4.0 V), the library is H4CP3.

For mixed voltage designs, the recommended powering sequence is to always activate or deactivate the highest voltage supply first for turning on or off the ASIC respectively.

3.3 H4CPlus SERIES I/O MACROS

This section describes the I/O cell and its various configurations as input, output, bidirectional, system interconnect, and oscillator macrocells. Included are design rules for I/O macros and oscillator pin placement.

The I/O cells provide all possible signal translation between mixed 3.3 V and 5.0 V systems. Input cells are powered from the core supply (VDD) independent of the input signal swing. Each output cell may be powered with either 3.3 V or 5.0 V independent of the core power supply.

The I/O cells that encircle the gate array core are designed to be highly-flexible and configurable into numerous I/O macro combinations. Each I/O cell contains input and output drivers, pull-resistors, ESD protection diodes and JTAG circuitry (see Figure 3-1).

I/O Cell Configurations:

- Inputs: Standard CMOS and TTL, Schmitt trigger, and high-drive macros
- Outputs: Standard CMOS and TTL, 3-state, and open-drain in 3 to 48 mA drive capacities
- Bidirectionals: all standard I/O types
- System Interconnect: CMTL I/O's, GTL I/O's, PCI I/O's and PECL inputs (see Section 3.3.4)
- JTAG boundary scan I/O macros
- Oscillator macrocells
- Power and ground sites
- ENID (enable IDD) test pin (see Section 3.4.7)

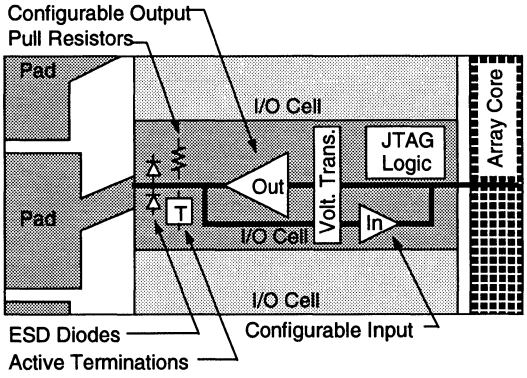

Figure 3-1 Simplified Diagram of the H4CPlus Series I/O Cell

3.3.1 Input Macros

The various input macro configurations include CMOS, TTL, inverting/non-inverting, Schmitt trigger, and high-drive clock input macros. Table 3-1 lists the various types of input macros available. All input macros are available in a JTAG version. See Section 5 Macro Naming Conventions.

Each input macro symbol, see Figure 3-2, has place holders for the input signal name (customer defined) and package pin number (also customer defined). Three connection ports (PAD, IC and DI) are also available.

Table 3-1 H4CPlus Series Input Macros (Non JTAG)

Input Macro	System Logic		Core Logic		Inverting	Non-Inverting	Non-Inverting High Drive	Schmitt Trigger
	3.3V	5.0V	3.3V	5.0V				
CMOS Input Logic								
ICI		•		•	•			
ICN		•		•		•		
ICNH		•		•			•	
ICXN		•	•			•		
ICXNH		•	•				•	
ILCI	•		•		•			
ILCN	•		•			•		
ILCNH	•		•				•	
ILSN	•		•			•		•
ILSNH	•		•				•	•
ISN		•		•		•		•
ISNH		•		•			•	•
ISXN		•	•			•		•
ISXNH		•	•				•	•
TTL Input Logic								
ILTXN	•			•		•		
ILTXNH	•			•			•	
ITN		•		•		•		
ITNH		•		•			•	
ITSN		•		•		•		•
ITSNH		•		•			•	•

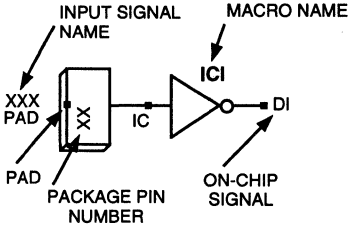

Figure 3-2 Example Input Symbol

The internal pull-resistors can be used to prevent the input macros from floating to an unknown state when they are not being driven by an external source. When selected, a pull-up resistor (about 75K ohms), always tied to the core power bus (VDD), is connected to the IC port of the input symbol as shown in Figure 3-3, to provide a high logic state. A pull-down resistor (about 35K ohms), always tied to the output ground rail (OVSS), may be connected to provide a low logic state.

Differential input or differential bidirectional pins may use pull-resistors. If pull-resistors are used on differential inputs, two pull-resistors must be used, one pull-up on IC and one pull-down on IC2 or the reverse, but not one input with a pull-resistor and the other input with no pull-resistor.

Pull-resistors are not meant to replace external pull-up or pull-down resistors which are attached to 3-state open-drain buses.

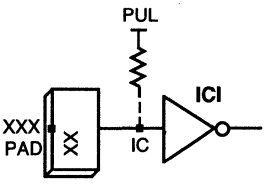

Figure 3-3 Example of an Input with a Pull-Up Resistor

All input macros are tied to the core power bus (VDD). For a 3.3 V core power bus chip with 3.3 V outputs and 5.0 V inputs, input macros must have their ESD diode connected to 5.0 V. Therefore, OVDD5 must be connected to 5.0 V, even though all outputs may be 3.3 V macros.

3.3.2 Output Macros

The various output macro configurations include standard CMOS, TTL, 3-state, slew-rate control, and open-drain output macros. Note that the number in the standard output macro name is not the output drive strength in mA (see Table 3-2). Most output macros are available in a JTAG version with the exception of 3 and 48 mA drive outputs. See Section 5 Macro Naming Conventions.

Each output symbol has place holders for the output signal name and package pin number. Each output also has a threshold-level (CMOS or TTL) property (not displayed) and two or three signal ports (DO, EN, and PAD), see Figure 3-4. The 3-state output macros have an additional port "EN" for the output enable signal.

The threshold-level property defines the CMOS or TTL switching level for timing purposes. The default value is "CMOS".

The 48 mA drive outputs (ON32x) require two I/O cells. The location of the output pad within the two cells is selected through the MASTER_OFFSET property in OACS. The default for this property is a zero. This places the output pad in the numerically lower location. When this property is set to one, the numerically higher pad is selected.

Table 3-2 H4CPlus Series Output Macros (Non JTAG)

Output Macro	System Logic		Core Logic		Drive(mA)[1]	3-State	Open-Drain	Slew-Rate Control
	3.3V	5.0V	3.3V	5.0V				
CMOS/TTL Output Logic								
ON2x		•		•	3	•	•	
ON4x		•		•	6	•	•	•
ON8x		•		•	12	•	•	•
ON16x		•		•	24	•	•	•
ON32x		•		•	48	•	•	•
ONL2x	•		•		2	•		
ONL4x	•		•		3	•	•	
ONL8x	•		•		6	•	•	
ONL16x	•		•		12	•	•	
ONLX2x	•			•	2	•		
ONLX4x	•			•	3	•		
ONLX8x	•			•	6	•		
ONLX16x	•			•	12	•		
ONX2x		•	•		3	•		
ONX4x		•	•		6	•		
ONX8x		•	•		12	•		

1. See electrical specifications for additional information.

x = Suffix such as S2, T, and OD.

3.3.2.1 Slew Rate Control Output Macros

Fast signal transitions and simultaneously switching outputs can cause crosstalk on adjacent signal pins and power bus noise. Output macros with the slew rate control can be used to slow the transition times of the output signal and reduce both types of noise. The slew rate control option is available for all ON4 through ON32 type output macros. Outputs with the "S2" suffix (ON4S2, ON8S2, etc.) provide a slew rate reduction of about 10% for ON4S2, ON8S2, ON16S2, and ON32S2 with 25, 50, 100, and 200 pF loads respectively.

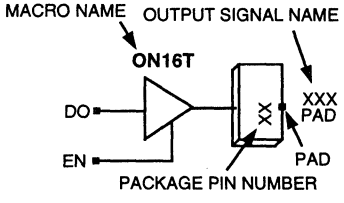

Figure 3-4 Example Output Symbol (3-State)

3.3.2.2 3-State Output Macros

3-state output macros are commonly used in bus applications when a high-impedance state is desired when the output is not used. For bidirectional 3-State macros, pull-resistors can be used to force the output to a "weak" low or high state while the output is disabled. However, the pull-resistors are not meant to replace external pull-up or pull-down resistors that are attached to a 3-state bus. The CAD system does not model pull-resistors on outputs because these resistors are parametrically checked on the tester but functionally will be over driven by test circuitry. Table 3-3 contains the states for bidirectional output macros with and without pull-resistors. All 3-state outputs use the "T" suffix (ON2T, ON16T, etc.).

Table 3-3 Function Table for 3-State Bidirectional Output Macro

DO	EN	PAD		
		No Resistor	Pull-Down	Pull-Up
L	H	L	L	L
H	H	H	H	H
X	L	Z	L (weak)	H (weak)

3.3.2.3 Open-Drain Output Macros

Open-drain output macros are often used to "wire-AND" multiple control signals on a common bus. The common bus will maintain a "low-state" as long as one or more signals is low. This avoids signal contention causing invalid logic states on the bus. For bidirectional open-drain macros, an external pull-up resistor is used to hold the output of the open-drain macro to a weak "high-state" until a low input forces its output to a "low-state", see Table 3-4. Open-drain outputs use the "OD" suffix (ON2OD, ON16OD, etc.). Internal pull-resistors are not meant to replace external pull-up or pull-down resistors which are attached to an open-drain bus.

Table 3-4 Open-Drain Output Macro Function Table

DO	PAD	
	No Resistor	Pull-Up
L	L	L
H	Z	H (weak)

3.3.3 Bidirectional Macros

Bidirectional macros are configured using a 3-state output macro and an input macro, see Figure 3-5. Only output and input macros with a "B" prefix can be used to configure bidirectional macros.

Internal pull-up and pull-down resistors may also be used in bidirectional macros by connecting the resistors to the "BIC" or "BC" ports or on the connecting net.

The available outputs and inputs used to configure bi-directional macros are listed in Table 3-5.

Table 3-5 Bidirectional Input and Output Macros (Non JTAG)

Input Macro	System Logic		Core Logic		Inverting	Non-Inverting	Schmitt Trigger
	3.3V	5.0V	3.3V	5.0V			
CMOS Input Logic							
BICI		•		•	•		
BICN		•		•		•	
BICXN		•	•			•	
BILCI	•		•		•		
BILCN	•		•			•	
BILSN	•		•			•	•
BISN		•		•			•
BISXN		•	•			•	•
TTL Input Logic							
BILTXN	•			•		•	
BITN		•		•		•	
BITSN		•		•		•	•

Output Macro	System Logic		Core Logic		Drive(mA)[1]	Open-Drain	3-State	Slew-Rate Control
	3.3V	5.0V	3.3V	5.0V				
CMOS/TTL Output Logic								
BON2x		•		•	3		•	
BON4x		•		•	6		•	•
BON8x		•		•	12	•	•	•
BON16x		•		•	24	•	•	•
BON32x		•		•	48	•	•	•
BONL2x	•		•		2		•	
BONL4x	•		•		3		•	
BONL8x	•		•		6	•	•	
BONL16x	•		•		12	•	•	
BONLX2x	•			•	2		•	
BONLX4x	•			•	3		•	
BONLX8x	•			•	6		•	
BONLX16x	•			•	12		•	
BONX2x		•	•		3		•	
BONX4x		•	•		6		•	
BONX8x		•	•		12		•	

1. See electrical specifications for additional information.

x = Suffix such as S2, T, and OD.

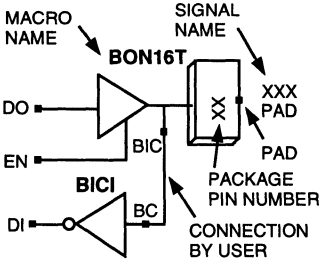

Figure 3-5 Example Bidirectional Macro

3.3.4 System Interconnect Macros

For high-speed chip-to-chip communications, the H4CPlus Series arrays support four types of data interface circuitry; Current Mode Transceiver Logic (CMTL), Gunning Transceiver Logic (GTL), Peripheral Component Interconnect (PCI) and Pseudo ECL (PECL). The available output and input macros used to configure each data transmission system are listed in Table 3-7. Logic level information about each of the four systems is displayed in Table 3-8. See Table 3-9 for worst case operating frequencies. Each of the data transmission systems has advantages and disadvantages as described in Table 3-6. The designer should select the appropriate system or systems for each design. For detailed application and performance information, refer to application note AN1521/D, *High-Performance CMOS Interfaces for H4CPlus ™Series Gate Arrays.*

Table 3-6 Comparison of System Interface Types

Type	3.3 V	5.0 V	Power	Noise Immunity	Differential	Single-Ended	Bidirectional	Active Termination
CMTL	yes	yes	med/high	600 mV	yes	yes	yes	yes
GTL	yes	yes	low	350 mV	no	yes	yes	no
PCI	yes	yes	med/high	250 mV	no	yes	yes	no
PECL	yes	yes	medium	140 mV	yes	no	no	no

Table 3-7 H4CPlus Series System Interface Macros

Input Macro	System Logic		Core Logic		Inverting	Non-Inverting	Differential
	3.3V	5.0V	3.3V	5.0V			
CMTL Input Logic							
BICMD		•		•			•
ICMD		•		•			•
ILCMD	•		•				•
GTL Input Logic							
BIGN		•		•		•	
IGI		•		•	•		
IGN		•		•		•	
BILGN	•		•			•	
ILGI	•		•		•		
ILGN	•		•			•	
PCI Input Logic							
IPCH		•		•		•	
BILPC	•		•			•	
ILPC	•		•			•	
ILPCH	•		•			•	
PECL Input Logic							
IPD		•		•			•
IPXD		•	•				•
ILPD	•		•				•

Output Macro	System Logic		Core Logic		Differential
	3.3V	5.0V	3.3V	5.0V	
CMTL Output Logic					
BOD32TCMT		•		•	•
O32CM		•		•	
OD32CMT		•		•	•
OD32TCMT		•		•	•
ODX32CMT		•	•		•
ODLX32CMT	•			•	•
ODL32CMT	•		•		•
GTL Output Logic					
BON40G		•		•	
ON20G		•		•	
BONL40G	•		•		
ONL20G	•		•		
PCI Output Logic					
BONTPC		•		•	
ONPC		•		•	
ONTPC		•		•	
BONLTPC	•		•		
ONLPC	•		•		
ONLTPC	•		•		

Table 3-8 Logic Levels for System Interface Macros

Parameter	VDD = 3.3 Volts				VDD = 5.0 Volts			
	CMTL	GTL	PCI	PECL	CMTL	GTL	PCI	PECL
Signal swing min	0.600 V	0.800 V	0.800	0.595 V	1.400 V	0.800 V	1.850	0.595 V
Noise margin High	0.200 V	0.350 V	1.402	0.140 V	0.600 V	0.350 V	0.400	0.140 V
Noise margin Low	0.200 V	0.350 V	0.743	0.145 V	0.600 V	0.350 V	0.250	0.145 V
V_{OH} min	1.950 V	1.200 V	2.970	2.275 V	3.200 V	1.200 V	2.400	3.975 V
V_{OL} max	1.350 V	0.400 V	0.330	1.680 V	1.800 V	0.400 V	0.550	3.380 V
V_{IH} min	1.750 V	0.850 V	1.568	2.135 V	2.600 V	0.850 V	2.000	3.835 V
V_{IL} max	1.550 V	0.750 V	1.073	1.825 V	2.400 V	0.750 V	0.800	3.525 V

Table 3-9 Worst Case Operating Frequencies (Preliminary)

Signal Type		Maximum Operation T_j = -40 to +85°C[3]					
		2.97 - 3.63 Volts			4.5 - 5.5 Volts		
		Clock MHz	Data Mb/s	V_{in} mV	Clock MHz	Data Mb/s	V_{in} mV
CMTL[2]	input	250	375	± 250	400	600	± 400
	output	105	160	-	210	250	-
GTL[1]	input	175	260	350	275	410	650
	output	100	150	-	200	250	-
PCI[1]	input	125	175	1200	125	175	1200
	output	50	100	-	50	100	-
PECL[2]	input	250	375	± 350	400	600	± 500

1. GTL and PCI operate in the single-ended mode.
2. CMTL and PECL operate in differential mode.
3. Output frequencies are dependent on PC board layout techniques, transmission line and crosstalk.

3.3.4.1 Current Mode Transceiver Logic

Current Mode Transceiver Logic (CMTL) was designed by Motorola to provide a high-speed interface with the following characteristics:

- Reduced voltage swings
- Low standby power
- High noise margins
- No external components for point to point
- Matched resistor termination for multi-tap
- Single or differential drive
- Differential bidirectional bus driving
- Internal active termination

The CMTL driver output stage is a complimentary push-pull CMOS output circuit with a reduced output voltage swing centered at the mid-point of the VDD power supply (VDD/2). The output stage eliminates the Miller capacitance and uses smaller devices than GTL in order to provide a higher bandwidth. Figure 3-6 shows an example of the OD32TCMT macro, a 32 mA CMTL differential output driver with an active termination across the outputs (denoted with the symbol "T"). The active termination is a pair of FETs connected like back to back diodes in order to further limit the swing at the output. The active termination sets the quiescent current of the driver at about 3.7 mA for VDD = 5.0 V.

The OD32TCMT is used to drive twisted pair line (Z_0 = 100 to 150 ohms) or two controlled impedance printed circuit board (PCB) lines (Z_0 = 50 to 100 ohms). The latter may have a CMTL receiver connected at the end of the lines without using termination resistors. The resistors are not needed for point to point connections due to the effective output impedance of the driver (32 ohms for VDD = 5.0 V and 50 ohms for VDD = 3.3 V)

which provides a series termination for twisted pair lines having a Z_0 of 100 ohms or controlled impedance PCB lines having a Z_0 of 50 ohms. For multi-taps on the lines, a resistor can be placed across the twisted pair at the end of the line with a value equal to the characteristic impedance of the pair of lines. Figure 3-7 shows an example of the ICMD macro which is a CMTL differential receiver. For VDD = 5.0 V, the receiver has an input sensitivity of ±200 mV differential for frequencies less than 200 MHz. The OD32TCMT can also be connected to an ECL receiver such as the ECLinPS MC10EL16/ 100EL16 for ECL receiver communications between CMOS arrays and to ECL operating on a positive supply voltage. Figure 3-8 shows an example of differential CMTL driving two transmission lines with no termination for point to point communications.

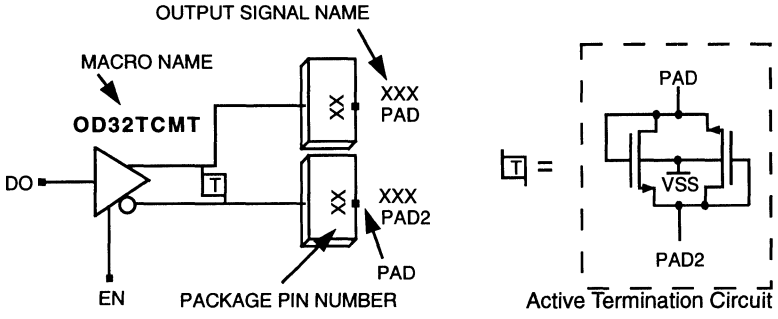

Figure 3-6 Example CMTL Driver Symbol

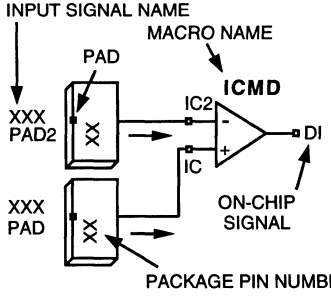

Figure 3-7 Example CMTL Receiver Symbol

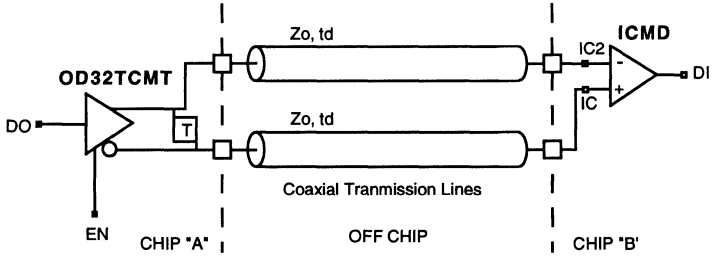

Figure 3-8 Differential CMTL with Active Termination

3.3.4.1.1 Differential I/O Rules

Differential I/O require two adjacent pads and attached package pins and two I/O cell sites. When using differential macros it is helpful to refer to the array floorplans or pad-to-pin cross-reference tables to locate suitable I/O cells for differential macros. Not all I/O cells have connecting die pads and depending on the package, not all die pads are connected to a package pin.

Design Rules for Differential I/O Macros:

1. Differential pads (PAD and PAD2) must be on the same side of the chip and occupy adjacent I/O cells connected to bond pads and package pins. See Figure 3-16 for the general layout of I/O cells and pads.
2. PAD must always be associated with an I/O cell.
3. PAD2 (IO_PIN1) must always be associated with a lower I/O site number than PAD (IO_PIN2).

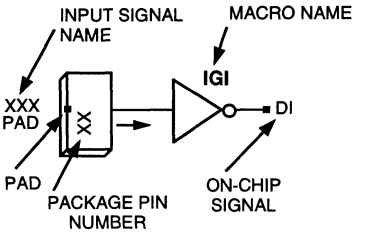

Figure 3-9 Example Gunning Receiver Symbol

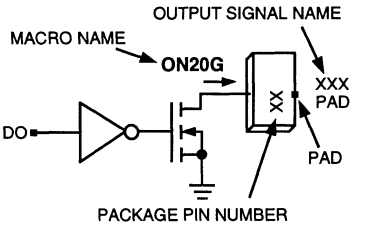

Figure 3-10 Example Gunning Driver Symbol

3.3.4.2 Gunning Transceiver Logic

Gunning Transceiver Logic (GTL), is a single-ended transmission line system with receivers, drivers and bidirectional macros (see Figure 3-9 and Figure 3-10).

The GTL drivers are open drain N-channel devices and the receivers are high gain differential comparators. The inverting input of all the GTL receivers is connected to the reference voltage pin, INPVR08 (see Section 3.4.6.1). This pin is required if a GTL macro is used in the design and should be connected to 0.8 V to maximize the noise margin. The GTL receivers have an uncertainty band of ± 50 mV around the reference voltage, INPVR08. The output sink current of the GTL driver ON20G macro is 24 mA while the BON40G macro is 48 mA. The ON20G macro is used to drive 50 ohm single-ended transmission lines with a 50 ohm resistor connected at the end of the line between the V_t supply (V_t = 1.2 V) and the signal line.

The BON40G macro is used to drive a bidirectional 50 ohm transmission line with a 50 ohm resistor connected at each end of the transmission line between the V_t supply and the signal line. BON40G is a single pad, dual site macro. OVSSP is a single pad, dual site macro which co-exists on the same sites as the BON40G. OVSSP is a special macro that provides the hi-drive capability (currents above 24 mA) to the adjacent macro. It must be placed in the numerically lower I/O cell site adjacent to the BON40G macro. By driving terminated transmission lines, high performance buses can be designed which minimize signal reflections that cause overshoot and undershoot.

3.3.4.3 PCI (Peripheral Component Interconnect)

The PCI bus was developed to provide a high-speed standard expansion bus for interfacing peripheral I/O to the processor and memory subsystems. It is processor independent and the bus is guaranteed to operate at 33 MHz. It was also designed for future expansion with 3.3 and 5.0 volt component combinations and 32 and 64 bit data interface. The benefits are lower costs through larger volumes, auto-configuration eliminates setup, upgradeable to higher performance, and plug and play. PCI is being used with the PowerPC™, Alpha™, 486, Pentium™ processors, and other chip sets, graphics, bridges and controllers, SCSI, IDE, communication, video, and multimedia.

The PCI interface is basically a CMOS bus that has virtually no power during steady state conditions. The PCI output drivers (see Figure 3-11 and Figure 3-12) are designed to switch only half the bus voltage required in order to reduce switching currents, reduce device sizes and improve circuit propagation delays. As the waveform reaches the end of the unterminated bus, the voltage doubles and returns back to the driver where the signal is terminated by the source impedance of the driver. This technique is called reflected wave switching in which, after the driver switches, it takes two times the line delay of the bus for all receivers to see a valid voltage. The fully loaded bus is assumed to be as low as 32 ohms while the unloaded trace impedance is 65 ohms. See Table 3-7 for a listing of the PCI macros that are available.

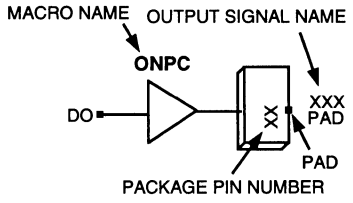

Figure 3-11 Example PCI Driver Symbol

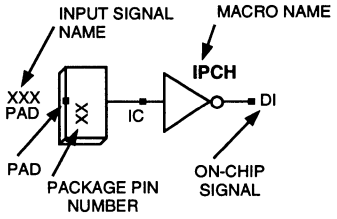

Figure 3-12 Example PCI Receiver Symbol

The DC specifications are very similar to TTL for the 5.0 volt PCI as shown in Table 3-10. For 3.3 volt operation, PCI uses a new, proportional input specification centered at 0.4 x (VDD). Proportional specifications provide better performance and larger noise margins. For input buffers, V_{IH} and V_{IL} are the logic threshold parameters.

What separates the specification of PCI from standard CMOS is the new AC voltage and current drive specifications for the outputs. Table 3-10 shows the minimum and maximum V_{OH} and V_{OL} to guarantee successful reflected wave switching. V_{OH}(AC) min and V_{OL}(AC) max are the main parameters that set the maximum value for the output impedance.

For instance at VDD = 4.75 V, when the output is switching from a low to a high, the output must reach at least to V_{OH}(AC) min of 1.4 V (for a Z_o = 32 ohms requiring at least 44 mA for 1.4V) so that with reflected wave switching the voltage will be twice this value, or 2.8 V. Since V_{IH} min of the receiver is 2.0 V, this achieves a noise margin of 800 mV which provides adequate margin for transient voltage ringing.

Table 3-10 PCI DC and AC Voltage Specifications

Symbol	VDD		Unit
	3.0 to 3.6 V	4.75 to 5.25 V	
V_{IH}min	0.475(VDD)	2.0	Volts
V_{IL}max	0.325(VDD)	0.8	Volts
V_{OH}min	0.9(VDD) @ -0.5 mA	2.4 @ -2.0 mA	Volts
V_{OL}max	0.1(VDD) @ 1.5 mA	0.55 @ 6.0 mA	Volts
V_{OH}(AC)min	0.3(VDD) @ -12 mA	1.4 @ -44 mA	Volts
V_{OH}(AC)max	0.7(VDD) @ -32 mA	3.1 @ -142 mA	Volts
V_{OL}(AC)max	0.6(VDD) @ 16 mA	2.2 @ 95 mA	Volts
V_{OL}(AC)min	0.18(VDD) @ 38 mA	0.71 @ 206 mA	Volts

When the output is switching from a high to a low, the output must reach at least to V_{OL}(AC) max of 2.2 V which results in a voltage change of 3.05 V for VDD = 5.25 V and 2.55 V for VDD = 4.75 V. This results in a minimum current of 95 mA for VDD = 5.25 V for a Z_o of 32 ohms. With reflected wave switching the voltage will be twice the voltage change reaching a V_{OL} of -0.85 V for VDD = 5.25 V or -0.35 V for VDD = 4.75 V which provides a noise margin of greater than the required 800 mV.

3.3.4.4 Pseudo ECL

Pseudo ECL (PECL), is ECL operating at VCC = 5.0 V and VEE = 0.0 V. PECL can be used in a differential system to gain the advantages of higher performance, high common mode noise immunity and signal ground noise immunity to minimize thermal voltage level problems. However, two package pins are used by the differential system. Transmission lines normally used with PECL are twisted pair, coaxial cables, and controlled impedance printed circuit board interconnects that are terminated with a resistor matching the characteristic impedance of the transmission line. Normally an external supply, V_t = 3.0 V, is required to connect to the termination resistor. PECL is also capable of driving low impedance (25 ohms) lines. Differential inputs require special rules, (see Section 3.3.4.1.1).

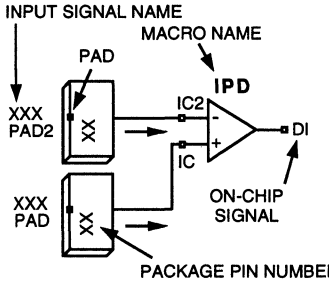

Figure 3-13 Example PECL Receiver Symbol

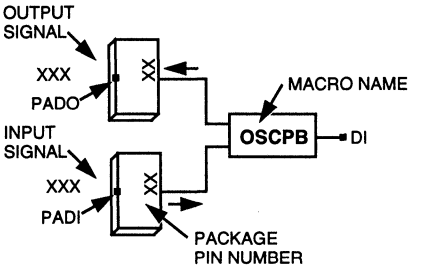

Figure 3-14 Example Oscillator Symbol

3.3.5 Oscillator Macros

Oscillator macros are used to generate clock signals from an external crystal and other discrete components. There are six oscillator I/O macros available for configuring crystal oscillator circuits (see Table 3-11). The OSCPB and the OSCPBL are the standard oscillator macros for 5.0 V and 3.3 V respectively. The OSCPHB and OSCPHBL macros are high-drive versions for driving high fanout clock networks. The OSCPSB and OSCPSBL use a Schmitt trigger input to insure CMOS edge speeds from very low crystal frequencies.

The oscillator macros have two pad ports, PADI and PADO, and one internal port DI (see Figure 3-14). The output pad, PADO, provides the inverted signal feedback to the crystal that is necessary for oscillation and DI provides the internal clock signal to the array core.

Table 3-11 Oscillator Macrocells

Oscillator Macro	System Logic		Core Logic		High Drive	Schmitt Trigger
	3.3V	5.0V	3.3V	5.0V		
OSCPB		•		•		
OSCPHB		•		•	•	
OSCPSB		•		•		•
OSCPBL	•		•			
OSCPHBL	•		•		•	
OSCPSBL	•		•			•

When using oscillator macros it is helpful to refer to the array floorplans or Pad-to-Pin Cross-Reference Tables to locate suitable I/O cells for oscillator macros. Not all I/O cells have die pads and depending on the package not all die pads are connected to a package pin (see Figure 3-16). The following rules must be used for the oscillator to function properly.

Design Rules for H4CPlus Series Oscillator Macros:

1. Oscillator pads (PADI and PADO) must be on the same side of the chip and occupy adjacent I/O cells connected to bond pads and package pins, see Figure 3-16.
2. PADO must always be associated with an I/O cell with a lower location number than PADI.

Note: Use the Array Floorplans or Pad-to-Pin Cross-Reference Tables in Section 4 to determine correct oscillator macro locations.

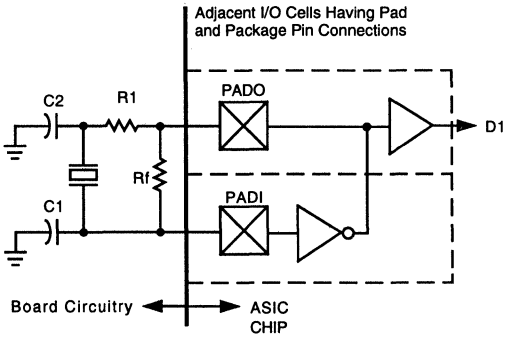

Figure 3-15 Example Oscillator Application

The oscillator macrocells contain an inverting amplifier and a driver to the internal array. The customer must supply the necessary external components to build a working oscillator. A typical implementation is shown in Figure 3-15. Please refer to the crystal manufacturers' specifications for crystal characteristics and oscillator design.

Oscillator Design Hints:

- Follow crystal manufacturers' recommendations for circuit components.
- Keep PCB traces and component leads short as possible to avoid parasitic capacitances and inductances.
- Select I/O cells with the shortest bond wire lengths (usually near the center of the die) to minimize parasitic inductances.
- Use high quality components.
- For fast start-up, use crystals with low series resistance (high Q).

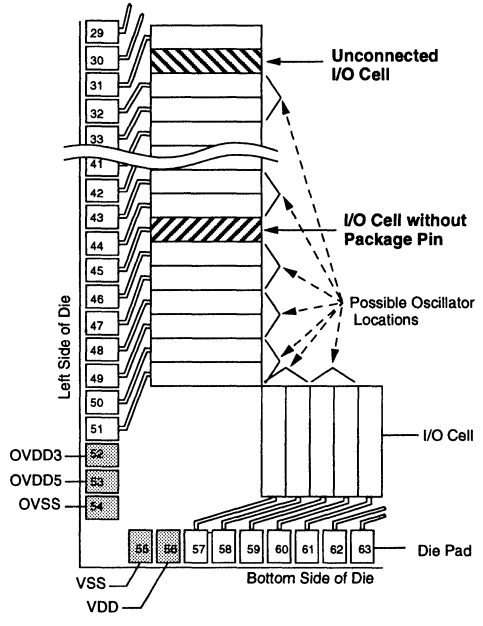

Figure 3-16 Die Section Showing Valid Oscillator Macro Placement

3.4 POWER AND GROUND CONSIDERATIONS

This section describes the H4CPlus array power and ground buses, required power and ground rules, precautions for Simultaneously Switching Outputs (SSO), and rules for location of SSO pins. Additionally, special power and ground requirements for system interconnect macros and the use of the required test pin are addressed. A description of voltage selection and implementation is available in application note AN1514, *H4CPlus™ Series 3.3V/5V Design Considerations.*

3.4.1 Power and Ground Buses

All H4CPlus Series arrays have three power and two ground buses, plus four reference voltage buses for system interconnect use (see Section 3.4.6.1). The buses VDD and VSS supply power and ground to the core and input macros. OVDD3 and OVDD5 are the 3.3 V and 5.0 V power buses for most output and oscillator macros and OVSS is the ground bus for most output and oscillator macros.

Table 3-12 Power and Ground Macros

Power Macro	Normal Voltage	Use
OVDD3	3.3V	Output and oscillator macro power
OVDD5	5.0V	Output and oscillator macro power
OVSS	0.0V	Output and oscillator macro ground
VDD	3.3V or 5.0V	Core and input macro power
VSS	0.0V	Core and input macro ground
OVSSP[1]	0.0V	Output and oscillator macro ground

1.To be used with dual-cell GTL macros, see Section 3.4.6.2

The OVDD3 and OVDD5 buses may be combined when all outputs are operating at a single voltage level. The core and output VDD buses may optionally be combined to form common power buses by using macros. This is often desirable in reducing power bus noise since the bus capacitance is increased and the inductance decreased. Other advantages include better utilization of OVDD/VDD and OVSS/VSS pins and decreased SSO noise. Table 3-13 illustrates the customer selectable power configuration options and the legal power and bus tying macros. Note that VSS and OVSS are unaffected by the power selection options.

3.4.2 Required Core Power and Ground Pins

A fixed set of five power and ground pads exists at each corner of the array to allow easy access for functional probe testing (see Figure 3-17). Depending on the array and package type, additional core power and ground pins may be required (see Pin-to-Pad Cross-Reference Tables). Note: Some array/package combinations have no fixed power or ground pads connected to package pins.

Table 3-13 Legal Combinations of Power and Bus Tying Macros

Customer Selection			Power Bus Voltage			Legal Power and Bus Tying Macro Selection							Fixed Power Connections
Core	I/O	Tie Core to I/O	VDD	OVDD3	OVDD5	VDD	OVDD3	OVDD5	ALLVDD	BOTHOVDD	BOTHVDD3	BOTHVDD5	
3.3V	3.3V	No	3.3V	3.3V	3.3V	Yes				Yes			OVDD3 is tied to OVDD5 at each OVDD3 and OVDD5 site
3.3V	3.3V	Yes	3.3V	3.3V	3.3V				Yes				Combines all VDD buses at each VDD, OVDD3 and OVDD5 site
3.3V	Mixed	No	3.3V	3.3V	5.0V	Yes	Yes	Yes					No power buses tied.
3.3V	Mixed	Yes	3.3V	3.3V	5.0V			Yes			Yes		VDD is tied to OVDD3 at each VDD and OVDD3 site
3.3V	5.0V	N/A	3.3V	5.0V	5.0V	Yes				Yes			OVDD3 is tied to OVDD5 at each OVDD3 and OVDD5 site
5.0V	5.0V	No	5.0V	5.0V	5.0V	Yes				Yes			OVDD3 is tied to OVDD5 at each OVDD3 and OVDD5 site
5.0V	5.0V	Yes	5.0V	5.0V	5.0V				Yes				Combines all VDD buses at each VDD, OVDD3 and OVDD5 site
5.0V	Mixed	No	5.0V	3.3V	5.0V	Yes	Yes	Yes					No power buses tied
5.0V	Mixed	Yes	5.0V	3.3V	5.0V		Yes					Yes	VDD is tied to OVDD5 at each VDD and OVDD5 site
5.0V	3.3V	N/A	5.0V	3.3V	3.3V	Yes	Yes	Yes					OVDD5 is tied to OVDD3 at each OVDD3 and OVDD5 site

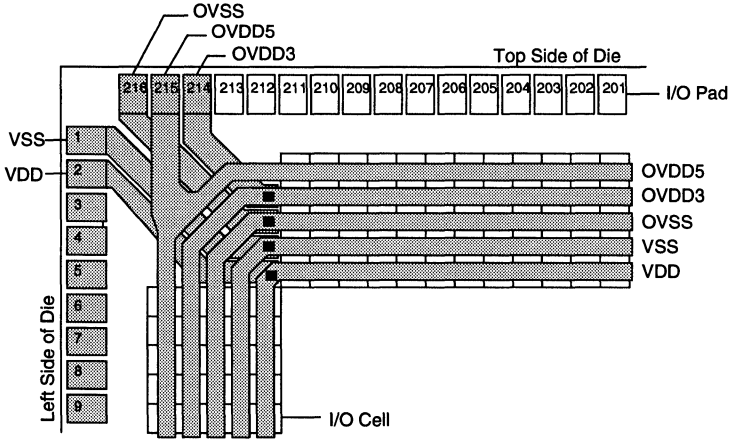

Figure 3-17 Power and Ground Bus

The VDD and VSS requirements can be checked by using Eq. (3-1). The equation will determine if additional VDD pins are required. If the value of P_A is negative, no additional VDD pins are required. A positive value for P_A requires additional VDD/VSS pins to be added to the design and the number should be equal to the numeric value of P_A rounded up to the next integer. More pins may be added to improve any design. **An equal number of VSS pins must also be added to the design.**

$$P_A = \frac{E}{N} - P_{pk} \qquad (3\text{-}1)$$

where:

P_A = Total additional VDD pins required

E = Number of equivalent gates used in the design

N = Number of gates that can be powered from a power/ground pair, see Table 3-14

P_{pk} = Fixed VDD pins for the selected package (see Pin-to-Pad Cross-Reference Tables in Section 4)

Table 3-14 Core Power Specification

Core Power VDD	Gates/Pin Pair
3.3V	12,000
5.0V	8,000

Rules and Recommendations for VDD and VSS Pins:

1. The fixed power and ground pins on each array are required and cannot be altered.
2. All power bus macros require assignment to an I/O cell that is connected to a package pin.
3. Additional VDD/VSS pads should be evenly spaced with fixed VDD/VSS pads.
4. Place VDD and VSS pads near or within groups of high-current output macros.
5. Use power macros to connect internal and output power buses. (This reduces the number of package pins required for VDD/VSS.)

Note:

Depending on the design, rules 4 and 5 should be used only after consideration of SSO noise since this may cause increased noise in the core.

3.4.3 Required I/O Macro Power and Ground Pins

Depending on the array and package type, additional pins may be required for I/O macro power (OVDD3 and OVDD5) and ground (OVSS). The following DC requirement must be met. No I/O macro may be located more than 25 I/O cell sites from the power macro or pin supplying it with power or ground.

Note: Some array/package combinations have no fixed power or ground pads preassigned to package pins.

Rules for Additional OVDD and OVSS Pins:

1. The fixed power and ground pins on each array are required and cannot be altered.
2. All power macros require assignment to an I/O cell that is connected to a package pin.
3. Additional OVDD/OVSS pads should be evenly spaced with fixed OVDD/OVSS pads.

3.4.4 Optional Peripheral Power Pins for Simultaneously Switching Outputs (SSO)

Simultaneously switching outputs are output macros which change state within four nanoseconds of each other. As an output macro switches state, it must charge or discharge an external capacitive load in a short period of time, but the required current sourced or sunk by the output is inhibited by the cumulative inductances of the package leads and the gate array. The total effect of the inductance and rapid current change (plus crosstalk) can be observed as voltages induced on the power and ground buses and also on adjacent signal pins, see Figure 3-18.

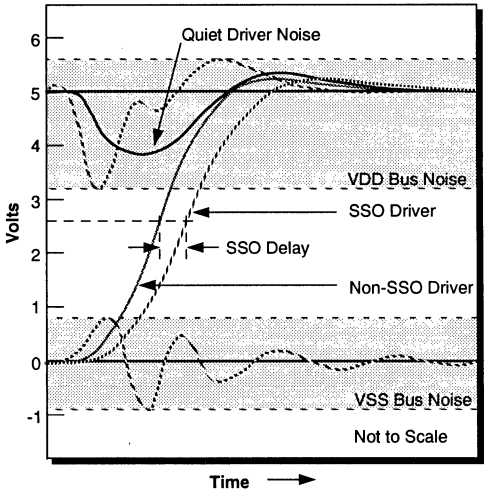

Figure 3-18 SSO Derived Noise

As the number of SSO's increase so does the severity of the power bus noise and other SSO related prob-

lems such as quiet-driver noise and SSO delay. Quiet-driver noise is the induced voltage swing of an output macro caused by power bus noise, while SSO delay is the additional time needed by the output macro to charge or discharge a capacitive load due to reduced power caused by SSO.

There are several ways to minimize SSO problems.

Controlling SSO Noise:

1. Provide sufficient OVDD3, OVDD5 and OVSS pins and distribute them as required. (see Eq. (3-2))
2. Place SSO pins as close as possible to OVDD3, OVDD5 and OVSS pins.
3. Place noise sensitive input signal pins such as clocks, enables, and resets near VSS pins and away from SSO's.

Table 3-15 SSO Multiplier for Macro and Logic Type

CMOS/TTL Macros	Output Logic Type			
	TTL		CMOS	
	VSS	VDD	VSS	VDD
ON2	90	144	144	144
ON2OD	90	288	144	288
ON2T/BON2T	90	144	144	144
ONX2	90	108	90	108
ONX2T/BONX2T	90	108	90	108
ONLX2	180	288	288	288
ONLX2T/BONLX2T	180	288	288	288
ONL2	180	216	180	216
ONL2T/BONL2T	180	216	180	216
ON4	60	96	96	96
ON4OD	60	288	96	288
ON4S2	72	115	115	115
ON4T/BON4T	60	96	96	96
ON4TS2/BON4TS2	72	115	115	115
ONX4	60	72	60	72
ONX4T/BONX4T	60	72	60	72
ONLX4	120	192	192	192
ONLX4T/BONLX4T	120	192	192	192
ONL4	120	144	120	144
ONL4OD	120	288	120	288
ONL4T/BONL4T	120	144	120	144
ON8	40	64	64	64
ON8OD/BON8OD	40	288	64	288
ON8S2	48	77	77	77
ON8T/BON8T	40	64	64	64
ON8TS2/BON8TS2	48	77	77	77
ONX8	40	48	40	48
ONX8T/BONX8T	40	48	40	48
ONLX8	80	128	128	128
ONLX8T/BONLX8T	80	128	128	128
ONL8	80	96	80	96
ONL8OD/BONL8OD	80	288	80	288
ONL8T/BONL8T	80	96	80	96

CMOS/TTL Macros	Output Logic Type			
	TTL		CMOS	
	VSS	VDD	VSS	VDD
ON16	20	32	32	32
ON16OD/BON16OD	20	288	32	288
ON16S2	24	39	39	39
ON16T/BON16T	20	32	32	32
ON16TS2/BON16TS2	24	39	39	39
ONLX16	40	64	64	64
ONLX16T/BONLX16T	40	64	64	64
ONX16	20	24	20	24
ONX16T/BONX16T	20	24	20	24
ONL16	40	48	40	48
ONL16OD/BONL16OD	40	288	40	288
ONL16T/BONL16T	40	48	40	48
ON32	10	16	16	16
ON32OD/BON32OD	10	288	16	288
ON32S2	12	19	19	19
ON32T/BON32T	10	16	16	16
ON32TS2/BON32TS2	12	19	19	19
PCI Macros	**VSS**		**VDD**	
ONPC	20		64	
ONTPC/BONTPC	20		64	
ONLPC	40		128	
ONLTPC/BONLTPC	40		128	
CMTL Macros	**VSS**		**VDD**	
O32CM	20		32	
OD32CMT	20		32	
OD32TCMT/BOD32TCMT	20		32	
ODX32CM	40		48	
ODLX32CMT	40		64	
ODL32CMT	40		48	
GTL Macros	**VSS**		**VDD**	
ON20G	32		288	
BON40G	16		288	
ONL20G	32		288	
BONL40G	16		288	

The following is an equation to determine if the maximum number of SSO's between OVSS or OVDD pins has been violated. If the relationship is not true, SSO must be redistributed such that fewer SSO's exist between OVSS or OVDD pins. If this cannot be achieved, additional OVSS and/or OVDD pins must be added.

$$A_N \Sigma \left(\frac{1}{M_N} \right) \leq 1 \qquad (3\text{-}2)$$

where:
A_N = Array scaling factor see Table 3-16
M_N = Macro scaling factor see Table 3-15

Table 3-16 SSO Multiplier for Array Type and Package (A_N)

Array	Package								
	QFP				Micro-Cool		OMPAC		
	128	160	208	240*	160	208	169	225	313*
H4CP028	8	8	n/a	n/a	n/a	n/a	n/a	n/a	n/a
H4CP048	8	8	8	n/a	n/a	n/a	6	6	n/a
H4CP075	8	8	8	n/a	n/a	n/a	6	6	n/a
H4CP109	n/a	8	8	8	8	8	n/a	6	6
H4CP146	n/a	n/a	n/a	n/a	8	8	n/a	n/a	6
H4CP178	n/a	n/a	n/a	n/a	8	8	n/a	n/a	6

* Estimated

For example, assume an H4CP075 array in a 208 QFP with CMOS outputs. ON8 outputs are to be used in a bus application. A_N, the SSO multiplier for array and package type is 8, and M_N for an ON8 output is 64. From Eq. (3-2) it can be calculated that no more than 8 ON8 SSO's can be placed between OVDD or OVSS pins; $8(8/64) \leq 1$. Therefore, if 64 SSO ON8 outputs are required, at least 8 OVDD and 8 OVSS pins are required. Note: As stated in Section 3.4.3, a DC check must also be made to determine the minimum number of OVDD and OVSS pins.

3.4.5 Rules for Optional Peripheral SSO OVDD and OVSS Pins:

1. The fixed power and ground pins on each array are required and cannot be altered.
2. All power macros require assignment to an I/O cell that is connected to a package pin.
3. Place additional SSO OVDD and OVSS pads near or within groups of high-current output macros.

3.4.6 Special Requirements for System Interconnect Macros

System interconnect macros have several unique requirements such as a reference voltage and ground bus segmentation.

3.4.6.1 Reference Voltages

System interconnect macros require a reference voltage if they are used single-ended. Each reference voltage macro is only used once in the design. All reference macros require assignment to an I/O cell that is connected to a package pin.

The following reference voltage pin names and buses are supported:

INPVR08	0.8 V reference for single-ended GTL inputs
INPVR25	2.5 V reference for single-ended CMTL inputs in 5.0 V systems
INPVR16	1.6 V reference for single-ended CMTL inputs in 3.3 V systems
INPVR38	3.8 V reference for single-ended PECL inputs

For example, if a GTL input macro is used in the design, a INPVR08 macro is required.

3.4.6.2 GTL Ground Segmentation

Segmentation of the output ground bus (OVSS) will only be supported for GTL output macros. Power bus segmentation macros isolate sections of the OVSS bus for isolation of GTL outputs. The isolated OVSS bus segments must contain dedicated pins and as many additional OVSS pins as required by the number of GTL output macros used in the design. GTL generated noise on OVSS could cause false triggering in the I/O or core section if OVSS bus segmentation is not used to isolate the GTL output.

Rules for OVSS Bus Segmentation:

1. I/O cells designated for fixed VDD/VSS cannot be used.
2. All bus segmentation macros requiring a package pin must be assigned to an I/O cell that is connected to a package pin.
3. A fixed OVSS pin is required in every segment so that the segment will be powered when unpackaged chips are probed.
4. An OVSS pin is required for every two GTL output macros that have a 48 mA sink current (such as BON40G or BONL40G). An OVSS pin is required for every four GTL output macros that have a 24 mA sink current (such as ON20G or ONL20G).

The bus segmentation macros cut the OVSS buses. The OVSSL and OVSSR macros are used to cut the bus to the left or right respectively and supply the power to the right or left respectively. These macros are also connected to an I/O pad such that they can be connected to a package pin. The OSVSSL and OSVSSR macros are not connected to an I/O pad. They may be used when a design is pin limited. Table 3-17 lists the available power bus segmentation macros and describes their use.

Table 3-17 OVSS Bus Segmentation Macros

OVSS Bus Segmentation Macros	Pin Req'd	OVSS Bus Cut	Use
OVSSL	YES	LEFT	Cut to the Left and Supply OVSS to the Right
OVSSR	YES	RIGHT	Cut to the Right and Supply OVSS to the Left
OSVSSL	NO	LEFT	Bus Cut
OSVSSR	NO	RIGHT	Bus Cut

The term left (L) and right (R) is used to denote the direction as viewed from the edge of the chip looking toward the center. Since the die pads and I/O sites are numbered counterclockwise, left refers to a lower number and right refers to a higher number. For example, refer to the die pad and I/O site numbering in Section 4, Figure 4-1.

The OVSSP macro may be used with dual-cell GTL macros (BON40G and BONL40G) to provide an output ground connection. The OVSSP macro may be placed on the adjacent pad to the GTL output thus utilizing this pad for ground.

Table 3-18 contains an example of how a 9 bit GTL bus could be implemented on an H4CP048 array in a 128 QFP. Since the design is pin limited, an attempt was made to use as few package pins as possible. Nine BON40G, (48ma bidirectional GTL outputs) were used. In addition to the nine signal pins, five pins (one for every pair of BON40G outputs) are required to be connected to the isolated OVSS bus. In this example, a total of 14 package pins were used.

Table 3-18 GTL Macro Placement for 9Bit Bus on Left Side of H4CP048 128 QFP

LEFT SIDE			
DIE PAD #	I/O CELL #	PACKAGE PINS #	MACRO TYPE
9	7	-	OSVSSL
10	8	7	<------- OVSSP
11	9	8	BON40G (Bit 0)
12	10	-	BON40G (Bit 1)
13	11	9	
14	12	10	<------- OVSSP
15	13	11	BON40G (Bit 2)
16	14	-	-
17	OVSS(15)	-	-
18	16	12	<------- OVSSP
19	17	13	BON40G (Bit 3)
20	18	-	-
21	19	-	-
22	20	-	BON40G (Bit 4)
23	21	14	
24	22	15	<------- OVSSP
25	23	16	BON40G (Bit 5)
26	24	-	-
27	OVDD5(25)	-	-
-	26	-	-
28	27	-	BON40G (Bit 6)
29	28	17	
30	29	18	<------- OVSSP
31	30	19	BON40G (Bit 7)
-	31	-	-
32	32	-	-
33	33	-	-
34	34	-	BON40G (Bit 8)
35	35	20	
-	36	-	OSVSSR

Notes:

1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise
2. OVSS, and OVDD5 indicate fixed power and ground pads on the die for probe test and are array dependent.

3.4.7 Test Pin

The ENID pin is required on all designs.

A test pin, ENID (enable IDD), must be added to each array in order to test for IDD device leakage. The customer must place the ENID pin in the schematic like any other input pin and assign it a pin number. For synthesis, the ENID pin must be added to the attributes files, similar to the power and ground pins (i.e. OVDD3, OVDD5, VDD, OVSS and VSS). Other than selecting the pin number, the customer should do nothing with this pin; it will not be modeled and will not be simulated.

This pin will be used at test to disable termination and pull-up current flow as well as disable the current sources in comparator inputs. The ENID pin is active high and has a pull-down resistor (the pull-down resistor current will be sourced by the tester and will not affect the IDD test measurement). In normal usage the ENID pin must be grounded.

3.5 POWER ESTIMATION

This section describes a manual power estimation method to assist in determining package requirements and chip junction temperature. The accuracy of this method is dependent upon understanding the design and its application. A definition of data rate and frequency will help clarify the power equations. Data rate is one bit of data per unit of time (b/s) or a maximum of one transition per unit of time. Frequency is, two bits of data per unit of time (Hz) or a maximum of two transitions. For example, a data rate of 1.0 Mb/s equals a frequency of 0.5 MHz. Therefore, if a flip-flop has an input clock frequency of 30 MHz, the maximum bit rate is 30 Mb/s and the maximum output frequency is 15 MHz.

Information needed to estimate power:

- H4CPlus array supply voltage & switching frequency
- Estimate of utilized and simultaneously switching gates
- Number of RAMs
- Number and types of inputs, outputs, and bidirectional macros
- Loads on the outputs

The estimated total power dissipated by an H4CPlus Series array is the sum of the core, RAM, and I/O power.

$$P_D = P_{core} + P_{ramt} + P_{io} \quad (3\text{-}3)$$

3.5.1 Core Power

The bulk of the power dissipated by the internal array (P_{core}) is based upon dynamic power of internal capacitive components including the input capacitance of each gate (NAN2 equivalent), the capacitive load of metal routing between macros and the output capacitance of 3-state macros (if applicable). The contribution of leakage currents, and therefore static power, is negligible. The internal power (excluding RAMs) is:

$$P_{core} = V_{DD}^2 \sum_{n=1}^{n} f_n (N_{g_n} C_g + N_{m_n} C_m + N_{t_n} C_t) \quad \{\mu W\} \quad (3\text{-}4)$$

where:

C_g = 0.05 pF (typical gate input capacitance)
C_m = typical metal capacitance (see Table 3-27)
C_t = 0.06 pF (typical 3-state macro output capacitance)
N_{g_n} = number of gates switching at f_n
N_{m_n} = number of macros switching at f_n
N_{t_n} = number of 3-state macros switching at f_n
V_{DD} = supply voltage {V}
f_n = output frequency of macros switching at f_n {MHz}

Table 3-19 RAM Power Estimates

RAM	C_{ram} {pF}	Power {µW/MHz} 3.3 V	5.0 V
Single-Port RAM's			
RSB8X8	8.5	46	106
RSB8X18	14.0	76	175
RSB16X8	13.1	71	164
RSB16X18	18.2	99	228
RSB16X36	29.5	161	369
RSB32X8	12.6	69	158
RSB32X18	24.1	131	301
RSB32X36	35.4	193	443
RSB64X18	28.6	156	358
RSB64X36	39.9	217	499
Dual-Port RAM's			
RDB8X9	15.5	84	194
RDB8X18	18.9	103	236
RDB8X36	27.8	151	348
RDB8X72	39.5	215	494
RDB16X9	27.9	152	349
RDB16X18	31.4	171	393
RDB16X36	38.2	208	478
RDB16X72	52.0	283	650
RDB32X9	51.8	282	648
RDB32X18	55.2	301	690
RDB32X36	62.1	338	776
RDB32X72	75.9	413	949
Quad-Port RAM's			
RQB16X18	71.7	390	896
RQB16X36	91.9	500	1149
RQB32X18	125.3	682	1566
RQB32X36	145.5	792	1819

1. Power = $1/2C_{ram}VDD^2f$ (µW/MHz)
2. Assumes all RAM outputs are switching.

3.5.2 RAM Power

A design may have several sizes of RAMs. The power consumed by the RAMs must be calculated separately from the rest of the core circuitry since RAMs generally have higher gate density and greater numbers of simultaneously switching gates. The combined power dissipated by all RAMs is

$$P_{ramt} = \sum P_{ram} \quad \{\mu W\} \qquad (3\text{-}5)$$

An estimate of the worst-case power dissipated by a RAM is based on its total equivalent capacitance.

$$P_{ram} = 1/2C_{ram}V_{DD}^2 f \quad \{\mu W\} \qquad (3\text{-}6)$$

where:

C_{ram} = total equivalent capacitance of RAMs (see Table 3-19)

V_{DD} = supply voltage {V}

f = 1 / (total address cycle time in µs) {MHz}

3.5.3 I/O Power

I/O power (P_{io}) is composed of three components, static (P_{iostat}), dynamic (P_{iodyn}), and system interconnect (P_{sysint}) power (see Section 3.5.5).

$$P_{io} = P_{iostat} + P_{iodyn} + P_{sysint} \qquad (3\text{-}7)$$

3.5.3.1 Static I/O Power (CMOS, TTL and PCI)

Static I/O power, P_{iostat}, is caused by the leakage currents (I_{in}) of input macros and pull-resistors. I_{in} can be significant if many inputs with pull-resistors and TTL input macros are used.

The leakage current of an input is dependent on the configuration and logic state of the input, see Table 3-20. For example, if an input has a pull-down resistor it will only draw significant current during the times the input is in a high state. Therefore, it is necessary to estimate the active time an input is drawing current versus the total operation time. The total static I/O power is:

$$P_{iostat} = \sum (I_{in}t_{active})V_{DD} \quad \{\mu W\} \qquad (3\text{-}8)$$

where:

I_{in} = input leakage current {µA} (see Table 3-20)

t_{active} = estimate of percentage of time when an input draws current (e.g.: use 0.5 for 50%)

Table 3-20 Typical Leakage Currents for Inputs

Resistor Type	Active State	VDD=3.3V I_{in} {µA}	VDD=5.0V I_{in} {µA}
none	either	1	1
PUL	low	15	41
PDL	high	25	69

Table 3-21 Estimated Short Circuit Power for I/O Macros

Macro Type 5V	$P_{ioshort}$* {µW/MHz}	Macro Type 3.3V	$P_{ioshort}$* {µW/MHz}
Inputs (all)	90	Inputs (all)	90
Outputs		Outputs	
ON2/BON2	83	ONL2/BONL2	33
ON4/BON4	112	ONL4/BONL4	43
ON8/BON8	166	ONL8/BONL8	59
ON16/BON16	233	ONL16/BONL16	80
ON32/BON32	395		
ONPC	173	ONLPC	80

* Input edge rate = 0.5ns, Typical 25°C

3.5.3.2 Dynamic I/O Power (CMOS, TTL and PCI)

Dynamic I/O power, P_{iodyn}, is the largest contributor to power dissipation by the array and is mostly the result of capacitive loads (C_L) on the outputs. The short circuit I/O power, $P_{ioshort}$, also contributes to the dynamic power and is estimated in Table 3-21. (The loads on input macros are usually small and are not considered.) The dynamic I/O power is:

$$P_{iodyn} = \sum C_L V_{DD} V_O f + \sum (P_{ioshort}) f \ \{\mu W\} \quad (3\text{-}9)$$

where:

C_L = capacitive load on outputs {pF}
f = output switching frequency {MHz}
$P_{ioshort}$ = estimated short circuit power for I/O macros (see Table 3-21)
V_{DD} = supply voltage {V}
V_O = maximum output voltage swing at the operating frequency {V}

3.5.4 Power Estimation Example

The following example estimates the total power dissipation of a hypothetical design and determines an appropriate package and junction temperature for simulation.

The assumptions are:

- Array: H4CP109
- Utilized Gates: 70,000 gates (logic only), 25% worst-case switching activity; 2,000 gates (clock distribution), 100% worst case switching activity
- I/O Types and loads: 70 CMOS inputs at 5.0 V swing, 30 with PUL resistors, 28 ONX2 outputs with 50 pF loads at 5.0 V swing and 24 BON8T with 50 pF loads at 5.0 V swing
- Conditions: Core bus VDD is 3.3 V, Output bus OVDD5 is 5.0 V, Output bus OVDD3 is tied to bus OVDD5, input clock frequency = 66 MHz, logic and output signals switching at 16.5 and 8.25 MHz
- An average fanout for macros of 2
- No system interconnect macros are used
- No RAM Macros are used

The input clock is immediately divided by two and by four. Of the 2,000 gates in the clock path, one-half are at 33 MHz (N_{g_1} = 1,000) and one-half are at 16.5 MHz (N_{g_2} = 1,000). The number of macros, N_{m_1}, is 133 (assuming 7.5 gates/macro) and $N_{m_1} = N_{m_2}$. Of the 70,000 utilized gates about 25% (17,500) of the gates are determined to be switching during a clock cycle. One-half of the gates have outputs switching at 16.5 MHz (N_{g_3} = 8,750) and one-half have outputs switching at 8.25 MHz (N_{g_4} = 8,750). The number of macros, N_{m_3} is 875 (assuming 10 gates/macro) and $N_{m_3} = N_{m_4}$. The metal capacitance is obtained from Table 3-27, C_m = 0.36 pF for the H4CP109 with an average fanout of two. No 3-state macros are used, therefore $N_{t_n}C_t$ = zero. The power consumed by the internal array provided by Eq. (3-4) is:

$$P_{core} = 3.3^2 [33(1000(0.05) + 133(0.36))$$
$$+ 16.5(1000(0.05) + 133(0.36))$$
$$+ 16.5(8750(0.05) + 875(0.36))$$
$$+ 8.25(8750(0.05) + 875(0.36))]$$

$$\mathbf{P_{core} = 255,582\ \mu W \text{ or } 0.26W}$$

The power consumed by the I/O is the sum of static and dynamic power, (see Eq. (3-7)).

The static I/O power is the sum of the leakage currents of all inputs during their active time. In this example 40 inputs have no pull-resistors and draw 1µA (see Table 3-20) all the time and 30 inputs have a PUL resistor which are active low about 20% of the time. The pull-up resistor is tied to VDD. The static I/O power using Eq. (3-8) is:

$$P_{iostat} = (40(1)1.0 + 30(15)0.20)3.3$$

$$\mathbf{P_{iostat} = 429\ \mu W \text{ or } 0.00429W}$$

The dynamic I/O power is the sum of the powers consumed by the 28 ONX2 outputs driving 50 pF, the 24 BON8T driving 50 pF, and the short circuit power of all the I/O. The dynamic I/O power using Eq. (3-9) is:

$$P_{iodyn} = [28(50)(5)^2 + 28(150)]8.25 + [24(50)(5)^2 + 24(490)]16.5$$

$$P_{iodyn} = 1,012,440\ \mu W \text{ or } 1.01W$$

The I/O power is:

$$\mathbf{P_{io} = 0.00 + 1.01 = 1.01\ W}$$

The total estimated power dissipated is:

$$P_D = P_{core} + P_{io} = 0.26 + 1.01$$

$$\mathbf{P_D = 1.27\ W}$$

This design uses 122 signal pins which fits into either a 208 QFP or a 208 MicroCool™. For this design, the maximum allowed junction temperature, T_j, is 85°C (assuming an ambient temperature of 25°C). To determine the required air flow, the thermal resistance (junction-to-ambient), $R_{\Theta JA}$, must first be calculated:

$$T_j = T_a + R_{\Theta JA}P_D$$

$$R_{\Theta JA} = (T_j - T_a)/P_D$$

$$R_{\Theta JA} = (85 - 25)/1.27 = 47.2°C/W$$

An $R_{\Theta JA}$ of 47.2 °C/W can be supported by the 208 QFP or the 208 MicroCool with no air flow (see Table 4-2 of Packaging Section).

3.5.5 System Interconnect I/O Power

The power consumed by the system interconnect output macros must be calculated separately from the rest of the I/O macros because of the special equations that are required. The system interconnect power is:

$$P_{sysint} = P_{REC} + P_{GTL} + P_{CMTL} \quad (3\text{-}10)$$

The DC receiver power, P_{REC}, is listed in Table 3-22.

3.5.5.1 GTL Output Power

The power dissipation of the GTL output, P_{GTL}, can be expressed using the following equation:

$$P_{GTL} = P_{GTL\_DC} + P_{GTL\_AC} \quad (3\text{-}11)$$

Table 3-22 DC Receiver Macro Power (typ.)

Receiver Macros	DC Power (mW)	Receiver Macros	DC Power (mW)
BICMD	10.50	ILCMD	1.98
BIGN	8.50	ILGI	1.16
BILGN	1.98	ILGN	1.98
ICMD	10.50	ILPD	2.64
IGI	11.00	IPD	2.50
IGN	8.50	IPXD	1.65

where:

$$P_{GTL\_DC} = V_{OL}\frac{(V_t - V_{OL})}{R_L}t_{LOW}X10^6\ \{\mu W\} \quad (3\text{-}12)$$

$$P_{GTL\_AC} = C_L V_t V_O f\ \{\mu W\} \quad (3\text{-}13)$$

where:

C_L = Total capacitance due to the input fan-in and package. {pF}

f = Maximum frequency that the output is switching. {MHz}

R_L = Termination load resistance for matching the characteristic impedance, Z_o, of the transmission line. Note: if 50 ohm load resistors are used at both ends of the line for bidirectional lines, R_L = 25 ohms. {Ω}

t_{LOW} = Fractional percentage of the cycle time the output is in the LOW state. For worst case, use 1.0.(e.g. use 0.5 for 50%)

V_O = Output voltage swing at the operating frequency with the equivalent R_L and C_L load. Normally equal to V_t - V_{OL}. {V}

V_{OL} = Output low voltage, 0.25 V typ., 0.4 V max. {V}

V_t = External GTL power supply voltage, normally 1.2 V, for connecting to the termination resistor. {V}

The power dissipated in the external resistor load is:

$$P_{EXT\_RL} = (V_t - V_{OL})^2\frac{t_{LOW}}{R_L}X10^6\ \{\mu W\} \quad (3\text{-}14)$$

Where each term is as previously described.

As an example assume that a GTL driver is driving a single-ended line (1.0 ft.) terminated with a 50 ohm resistor to V_t = 1.2 V, assume C_L = 10 pF at a frequency of f = 66 MHz.

The DC power using Eq. (3-12)is:

$$P_{GTL\_DC} = 0.25\frac{(1.2-0.25)}{50}0.5X10^6 = 2375\ \mu W$$

The AC power using Eq. (3-13)is:

$$P_{GTL\_AC} = (10)\ (1.2)\ (1.2-0.25)\ (66)$$
$$= 752.4\ \mu W$$

The total GTL power is:

$$P_{GTL} = 2375 + 752.4 = 3127.4\ \mu W \text{ or } 3.1\ mW$$

Using Eq. (3-14) the external resistor power is:

$$P_{EXT\_RL} = (1.2-0.25)^2\left(\frac{0.5}{50}\right)X10^6$$
$$= 9{,}025\ \mu W \text{ or } 9.03\ mW$$

Note that the length of the transmission line is not a factor in the power dissipation.

3.5.5.2 CMTL Output Power

Power consumption for CMTL outputs (P_{CMTL}), is dependent on the power-supply voltage, frequency of operation, macro through current, termination method, transmission line, and load. The power dissipation for a CMTL output can be calculated from the following equation:

$$P_{CMTL} = P_{CL} + P_{RL} + P_{act} + P_{LINE} \qquad (3\text{-}15)$$

where:

P_{CL} = power due to through-current and load capacitance.

$$P_{CL} = (C_L + C_{pd})\,V_O V_{DD} f \qquad \{\mu W\} \quad (3\text{-}16)$$

P_{RL} = driver power due to external resistor load for terminated lines. Note: For differential drive, multiply P_{RL} times four.

$$P_{RL} = \left(\frac{V_O}{4R_L}\right)(V_{DD} - V_O)\,X10^6 \qquad \{\mu W\} \quad (3\text{-}17)$$

P_{act} = power due to active termination. Note: If K = 1 in Eq. (3-21) below, then $P_{act} = 0$.

$$P_{act} = fV_{DD}I_{act}(T - 2T_{ave}) \qquad \{\mu W\} \quad (3\text{-}18)$$

P_{LINE} = power due to unterminated transmission line. Note: $P_{LINE} = 0$, if the line is terminated at the receiving end with a matching impedance. Also, for differential drive, P_{LINE} must be doubled.

$$P_{LINE} = fC_{TL\_MOD}V_{DD}V_O\frac{(1-\rho_S^K)}{(1+\rho_S^K)} \quad \{\mu W\} \quad (3\text{-}19)$$

where:

C_L = total capacitive load due to input fan-in and package. For differential drive, C_L must be doubled since there are two lines. {pF}

C_{pd} = power dissipation capacitance of output device due to through-current {pF} (see Table 3-23)

C_{TL_MOD} = modified transmission line capacitance for power dissipation.

$$C_{TL\_MOD} = \frac{T_{L\_MOD}}{Z_O}X10^3 \quad \{pF\} \qquad (3\text{-}20)$$

f = the maximum switching frequency {MHz}

I_{act} = static current due to active termination (see Table 3-23)
Note: if K =1 in Eq. (3-21), then $I_{act} = 0$.

K = positive integer (when ρ_S is a negative number see Eq. (3-24)) ≥ 1. Note: When K = 1, voltage at the receiver is a maximum when the voltage at the driver is constant at V_{DD} / 2.

$$K = \frac{T}{4T_{L\_MOD}} \qquad (3\text{-}21)$$

R_L = termination resistor connected to V_{DD} / 2 for single-ended drive. For differential drive R_L is the total resistance between the differential lines. {Ω}

R_O = the output impedance of the CMTL driver {ohms} (see Table 3-23)

T = switching period (1/f) $X10^3$ {ns}

T_L = total transmission line delay {ns}

T_{L_MOD} = modified transmission line delay for calculating K and C_{TL_MOD} {ns}; to calculate T_{L_MOD} use only one of the appropriate equations, either Eq. (3-22) or Eq. (3-23).

$$\text{if } \quad n\frac{T}{2} \le T_L \le n\frac{T}{2} + \frac{T}{4} \quad \text{for n = integer from}$$

0 to N. Then use Eq. (3-22)

$$T_{L\_MOD} = T_L - N\frac{T}{2} \qquad (3\text{-}22)$$

or

if $n\frac{T}{2} + \frac{T}{4} < T_L < (n+1)\frac{T}{2}$ for n = integer

from 0 to N. Then use Eq. (3-23)

$$T_{L\_MOD} = (N+1)\frac{T}{2} - T_L \qquad (3\text{-}23)$$

Note: The value for T_{L_MOD} must be adjusted, if ρ_S is a negative number, so that K is an integer in Eq. (3-21). However, if K > 5, the P_{LINE} term $(1-\rho_S{}^K/(1+\rho_S{}^K) \approx 1$, for $|\rho_S| < 0.5$. The adjusted value of T_{L_MOD} that is used in Eq. (3-21) must be used in Eq. (3-20). For twisted pair differential drive, C_{TL_MOD} should be doubled.

T_{ave} = average rise and fall times for power dissipation calculations (see Table 3-23)

V_{DD} = Supply voltage {V}

V_O = The output voltage swing in volts (see Table 3-23) at the operating frequency and the equivalent load condition. For unterminated lines, the total load capacitance should include the capacitance for the specific line length of C_{TL_MOD}. For terminated lines, the load should include the termination resistor.

Z_o = is the characteristic impedance of the transmission line to AC ground for controlled impedance printed circuit board line. For twisted pair differential drive, Z_O is the characteristic impedance between the two lines. {Ω}

ρ_S = The source coefficient of reflection

$$\rho_S = \frac{R_O - Z_O}{R_O + Z_O} \qquad (3\text{-}24)$$

For terminated lines, the external load resistor, R_L, will dissipate power as shown in Eq. (3-25). For single-ended lines with R_L connected to VDD/2, then P_{EXT_RL} is 1/4 the value calculated in Eq. (3-25).

$$P_{EXT\_RL} = \frac{V_O^2}{R_L} X10^6 \quad \{\mu W\} \qquad (3\text{-}25)$$

The P_{CL} term lumps the total load capacitance, including capacitance due to the package, with the typical power dissipation capacitance, C_{pd}. C_{pd} is a measure of internal capacitances given specifically for power consumption calculations. It provides a simplified and accurate method for calculating an output power dissipation caused by the switching through current.

The P_{RL} term is the power dissipated in the output device due to a termination or load resistor. It does not include the power dissipated in the load resistor itself (see Eq. (3-25)).

The P_{act} term calculates the power due to active self-termination. A static current is present when a CMTL output is terminated with the active network which results in a DC power at low frequencies that can be calculated using Eq. (3-18). The P_{LINE} term in the equation is the power dissipated due to driving an unterminated transmission line.

The P_{LINE} reaches a maximum power whenever the line delay is equal to a quarter wavelength (also 3/4T, 5/4T, etc.) at which time the receiver voltage reaches a maximum along with the power. The P_{LINE} reaches a minimum power whenever the line delay is equal to a half wavelength (also T, 3/2T, etc.) at which time the driver appears to have zero line capacitance with the voltage at the driver and receiver being the same with no overshoot or undershoot.

Table 3-23 CMTL (OD32TCMT) Output Characteristics Versus VDD

VDD	C_{pd}	I_{act}	T_{ave}	V_O {Volts} @ C_L = 50 pF			R_O
Voltage	pF	mA	ns	1 MHz	100 MHz	150 MHz	Ohms
2.97	16.6	0	2.0	0.94	0.32	0.25	55
3.30	16.7	0.10	1.9	1.05	0.59	0.43	50
3.63	16.8	0.19	1.8	1.17	0.80	0.60	45
4.00	16.3	0.90	1.7	1.38	1.09	0.92	40
4.50	15.5	1.80	1.5	1.58	1.56	1.25	36
4.75	15.0	2.79	1.45	1.72	1.63	1.45	34
5.00	14.7	3.70	1.35	1.83	1.83	1.65	32
5.25	14.1	4.60	1.3	1.95	1.95	1.81	30
5.50	13.8	5.60	1.2	2.10	2.10	2.00	28

Note: I_{act} is the current for the value of V_o at 1.0 MHz. If V_o changes due to resistor or capacitive loading, the value of I_{act} also changes.

3.5.5.2.1 CMTL Power Example

As an example of calculating P_{CMTL} assume that a differential CMTL driver (OD32TCMT) with active termination (see Figure 3-8) is used for point to point communications driving an unterminated controlled impedance PCB lines having a Z_O of 50 ohms. Assume V_{DD} = 5.0 V, f = 100 MHz, and T_L = 4.0 ns. From Table 3-23, R_O = 32 ohms, I_{act} = 3.7 mA, C_{pd} = 14.7 pF, T_{ave} = 1.35 ns, and V_O = 1.83 V. Assume the package and fan-in capacitance is such that C_L = 5.0 pF/line. For f = 100 MHz, T = 10.0 ns.

From Eq. (3-16):

$$P_{CL} = (10 + 14.7)(1.83)(5)(100)$$
$$= 22{,}600\ \mu W \text{ or } 22.6\ mW$$

From Eq. (3-17) P_{RL} = 0 since R_L is not used.

From Eq. (3-18):

$$P_{act} = (100)(5)(3.7)(10 - 2(1.35))$$
$$= 13{,}505\ \mu W \text{ or } 13.5\ mW$$

From Eq. (3-23):

Since solving for n gives N = 0; then $\frac{T}{4} < T_L < \frac{T}{2}$

or $2.5 < T_L < 5$

Then $T_{L\_MOD} = (0+1)\frac{10}{2} - 4 = 1.0$ ns

From Eq. (3-24):

$$\rho_S = \frac{32 - 50}{32 + 50} \approx -0.22$$

From Eq. (3-21):

$$K = \frac{10}{4(1)} = 2.5$$

Therefore P_{LINE} must be calculated for K = 2 ($T_{L\_MOD_2}$ = 1.25 ns) and K = 3 ($T_{L\_MOD_3}$ = 0.833 ns) and then interpolate for K = 2.5.

From Eq. (3-20):

$$C_{TL\_MOD_2} = \frac{1.25}{0.05} = 25\ pF \text{ and}$$

$$C_{TL\_MOD_3} = \frac{0.833}{0.05} = 16.67\ pF$$

From Eq. (3-19):

$$P_{LINE_2} = (100)(25)(5)(1.83)\frac{(1 - (-0.22)^2)}{(1 + (-0.22)^2)}$$
$$= 20{,}763\ \mu W$$

$$P_{LINE_3} = (100)(16.67)(5)(1.83)\frac{(1 - (-0.22)^3)}{(1 + (-0.22)^3)}$$
$$= 15{,}581\ \mu W$$

Interpolating for K = 2.5, P_{LINE} = 18,172 µW or 18.2 mW, but for differential drive, P_{LINE} must be doubled since there are two lines. Use the value of 36.4 mW for line power.

Therefore, the total CMTL power is:

$$P_{CMTL} = (22.6) + (0) + (13.5) + (36.4)$$
$$\mathbf{= 72.5\ mW}$$

As another example, assume that the previous exercise used a termination resistor of R_L = 100 ohms in order to match the two 50 ohm transmission lines. The loaded V_o can be calculated using the following equation.

$$V_{O\,(loaded)} = V_O\frac{Z_O}{R_O + Z_O} = 1.83\left(\frac{50}{32 + 50}\right) \quad (3\text{-}26)$$
$$= 1.12 \text{ Volts}$$

$I_{act} \approx 0.19$ mA due to the reduced V_O amplitude which is approximately the same as V_{DD} = 3.6 V (@ 1.0 MHz) with no output load (see Table 3-23).

From Eq. (3-16):

$$P_{CL} = (10 + 14.7)(1.12)(5)(100)$$
$$= 13{,}832\ \mu W = 13.83\ mW$$

From Eq. (3-17):

$$P_{RL} = 4\left(\frac{1.12}{4(100)}\right)(5 - 1.12)X10^6 = 43{,}456\ \mu W$$
$$= 43.46\ mW$$

From Eq. (3-18):

$$P_{act} = (100)(5)(0.19)(10 - 2(1.35))$$
$$= 694\ \mu W \text{ or } 0.69\ mW$$

Since the differential lines are terminated, P_{LINE} = 0, therefore the total power is:

$$P_{CMTL} = 13.83 + 43.46 + 0.69 \mathbf{= 57.98\ mW}$$

The external power dissipated by R_L from Eq. (3-25):

$$P_{EXT\_RL} = \frac{(1.12)^2}{100}X10^6$$
$$\mathbf{= 12{,}544\ \mu W \text{ or } 12.5\ mW}$$

The CMTL on-chip power for the unterminated line (72.5 mW) is higher than the terminated line (57.98 mW) at 100 MHz for V_{DD} = 5 volts.

3.6 DELAY ESTIMATION

The switching characteristics (SC) data which is included on each macro data sheet (see example in Figure 3-19) shows the nominal performance of the macro under typical conditions, but the SC tables can also be used in calculating delay paths under various conditions. The delay calculations described in this section are useful in estimating critical paths under any operating condition. The following equations are the same as those used by the CAD system, except for certain simplifications and assumptions. A complete description of the delay and timing equations is available in application note AN1093/D, *Delay and Timing Methods for CMOS ASICs.*

3.6.1 Delay Equations

The macro delay is dependent on the no-load delay, input rise/fall time delay, load delay and operating conditions. (Note that the RC delay is neglected in these equations.) The rising and falling delay equations are:

$$t_{PLH} = \left(t_{PLH0} + t_{INP_r} + K1C_{Lout}\right)PTV \quad (3\text{-}27)$$

$$t_{PHL} = \left(t_{PHL0} + t_{INP_f} + K2C_{Lout}\right)PTV \quad (3\text{-}28)$$

where:

t_{PLH0}, t_{PHL0} = rising and falling macro no-load delays (see Figure 3-19)

t_{INPr}, t_{INPf} = estimated input rise/fall time delay (Table 3-24)

K1, K2 = rising and falling load sensitivity K-factors (see Figure 3-19)

C_{Lout} = total capacitive load on the output net {pF} (Table 3-27)

PTV = process, temperature, and voltage scaling factors for 3.3V and 5.0V. (Table 3-25, Table 3-26)

The input rise/fall time delay, t_{INP}, of a macro is dependent on the output rise and fall time of the driving macro. The output rise and fall time of the driving macro can be determined by the following equations.

$$t_r = t_{r0} + K3C_{Lin} \quad (3\text{-}29)$$

$$t_f = t_{f0} + K4C_{Lin} \quad (3\text{-}30)$$

where:

t_{r0}, t_{f0} = no-load output rise/fall times from driving macro (see Figure 3-19)

K3, K4 = output rise/fall time K-factors from driving macro (see Figure 3-19)

C_{Lin} = total capacitive load on the input net {pF} (Table 3-27)

Table 3-24 Estimated Input Rise/Fall Time Delays

Rise/Fall Time, t_r, t_f {ns}	VDD = 3.3 Volts		VDD = 5.0 Volts	
	Est. Rise Delay, t_{INP_r} {ns}	Est. Fall Delay, t_{INP_f} {ns}	Est. Rise Delay, t_{INP_r} {ns}	Est. Fall Delay, t_{INP_f} {ns}
0.25	-0.04	-0.03	-0.03	-0.03
0.50	0	0	0	0
1.0	0.08	0.06	0.05	0.05
2.0	0.24	0.18	0.16	0.15
3.0	0.40	0.30	0.27	0.25
4.0	0.49	0.37	0.32	0.30
6.0	0.67	0.51	0.42	0.40
8.0	0.85	0.65	0.52	0.50

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate t_r,t_f = 1.00ns) T_J = 25.0°C (Nominal) all units are in ns.

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFRP								
t_{PLH}	Propagation Delay,	0.90	0.98	1.23		1.23	1.3		1.17
t_{PHL}	CK to Q	0.91	0.99	1.22		1.32	1.4		0.92
t_{PLH}	Propagation Delay,	1.05	1.13	1.38		1.51	1.62		1.16
t_{PHL}	CK to QB	1.11	1.19	1.41	0.76	1.56	1.66	1.93	0.92
t_{PHL}	Propagation Delay, RB to Q	0.40	0.47	0.70	0.76	0.57	0.67	0.94	0.93
t_{PLH}	Propagation Delay, RB to QB	0.55	0.63	0.88		0.77	0.8		1.16
t_r	Output Rise Time, Q	0.18	0.42	1.15		0.23	0.5		3.42
t_f	Output Fall Time, Q	0.17	0.29	0.64		0.21	0.7		1.41
t_r	Output Rise Time, QB	0.13	0.37	1.11		0.18	0.52		3.45
t_f	Output Fall Time, QB	0.14	0.26	0.61	1.17	0.21	0.35	0.77	1.40

t_{PLH0} → K1; t_{PHL0} → K2; t_{r0} → K3; t_{f0} → K4

Capacitance per fanout = 0.05 pF (metal capacitance is not included)

Figure 3-19 Example Switching Characteristics Table

Table 3-25 3.3 V Process, Voltage, Temperature Scaling Factors (Normalized to Typical)

Scaling Factors for 3.3 Volts								
Process	Voltage	Temperature °C						
		-55 (0.79)	-40 (0.83)	0 (0.93)	25 (1.00)	70 (1.12)	85 (1.16)	125 (1.26)
Best (0.76)	2.70 (1.30)	0.78	0.82	0.92	0.99	1.10	1.14	1.25
	3.00 (1.12)	0.67	0.71	0.80	0.85	0.95	0.98	1.07
	3.30 (1.00)	0.60	0.63	0.71	0.76	0.85	0.88	0.96
	3.60 (0.91)	0.55	0.57	0.65	0.69	0.77	0.80	0.87
	4.00 (0.79)	0.48	0.50	0.56	0.60	0.67	0.69	0.76
Typical (1.00)	2.70 (1.30)	1.03	1.08	1.22	1.30	1.45	1.50	1.64
	3.00 (1.12)	0.89	0.93	1.05	1.12	1.25	1.30	1.41
	3.30 (1.00)	0.79	0.83	0.93	1.00	1.12	1.16	1.26
	3.60 (0.91)	0.72	0.76	0.85	0.91	1.02	1.05	1.15
	4.00 (0.79)	0.63	0.66	0.74	0.79	0.88	0.91	1.00
Worst (1.33)	2.70 (1.30)	1.37	1.44	1.62	1.73	1.93	2.00	2.18
	3.00 (1.12)	1.18	1.24	1.39	1.49	1.66	1.72	1.88
	3.30 (1.00)	1.05	1.10	1.24	1.33	1.49	1.54	1.68
	3.60 (0.91)	0.96	1.00	1.13	1.21	1.35	1.40	1.53
	4.00 (0.79)	0.83	0.87	0.98	1.05	1.17	1.22	1.32

Table 3-26 5.0 V Process, Voltage, Temperature Scaling Factors (Normalized to Typical)

Scaling Factors for 5.0 Volts								
Process	Voltage	Temperature °C						
		-55 (0.79)	-40 (0.83)	0 (0.93)	25 (1.00)	70 (1.12)	85 (1.16)	125 (1.26)
Best (0.76)	4.00 (1.23)	0.74	0.78	0.87	0.93	1.04	1.08	1.18
	4.50 (1.08)	0.65	0.68	0.77	0.82	0.92	0.95	1.04
	4.75 (1.04)	0.63	0.66	0.74	0.79	0.88	0.92	0.99
	5.00 (1.00)	0.60	0.63	0.71	0.76	0.85	0.88	0.96
	5.25 (0.97)	0.58	0.61	0.69	0.74	0.82	0.86	0.92
	5.50 (0.95)	0.57	0.60	0.67	0.72	0.81	0.84	0.91
Typical (1.00)	4.00 (1.23)	0.97	1.02	1.15	1.23	1.37	1.42	1.55
	4.50 (1.08)	0.85	0.90	1.01	1.08	1.21	1.25	1.36
	4.75 (1.04)	0.83	0.86	0.97	1.04	1.16	1.20	1.30
	5.00 (1.00)	0.79	0.83	0.93	1.00	1.12	1.16	1.26
	5.25 (0.97)	0.77	0.81	0.90	0.97	1.08	1.12	1.22
	5.50 (0.95)	0.75	0.79	0.89	0.95	1.06	1.10	1.20
Worst (1.33)	4.00 (1.23)	1.29	1.36	1.53	1.64	1.83	1.89	2.06
	4.50 (1.08)	1.14	1.19	1.34	1.44	1.61	1.66	1.81
	4.75 (1.04)	1.10	1.15	1.29	1.38	1.54	1.60	1.73
	5.00 (1.00)	1.05	1.10	1.24	1.33	1.49	1.54	1.68
	5.25 (0.97)	1.02	1.07	1.20	1.29	1.44	1.50	1.62
	5.50 (0.95)	1.00	1.05	1.18	1.26	1.41	1.46	1.59

Table 3-27 Metal and Total Load Capacitance Based on Array and Fanout

Array	Metal & Load Cap. (pF)	Fanout						
		1	2	4	6	10	15	25
H4CP028	C_m	0.16	0.24	0.41	0.59	0.95	1.28	2.02
	C_{Lin}, C_{Lout}	0.21	0.34	0.61	0.89	1.45	2.03	3.27
H4CP048	C_m	0.18	0.27	0.50	0.68	1.06	1.46	2.32
	C_{Lin}, C_{Lout}	0.23	0.37	0.70	0.98	1.56	2.21	3.57
H4CP075	C_m	0.22	0.34	0.62	0.85	1.30	1.80	2.85
	C_{Lin}, C_{Lout}	0.27	0.44	0.82	1.15	1.80	2.55	4.10
H4CP109	C_m	0.24	0.36	0.67	0.97	1.41	1.99	3.08
	C_{Lin}, C_{Lout}	0.29	0.46	0.87	1.27	1.91	2.74	4.33
H4CP146	C_m	0.25	0.38	0.70	1.02	1.48	2.08	3.22
	C_{Lin}, C_{Lout}	0.30	0.48	0.90	1.32	1.98	2.83	4.47
H4CP178	C_m	0.27	0.42	0.77	1.11	1.61	2.27	3.52
	C_{Lin}, C_{Lout}	0.32	0.52	0.97	1.41	2.11	3.02	4.77

Note: C_m = typical metal capacitance per array; C_{Lin}, C_{Lout} = C_m + (fanout)• 0.05.

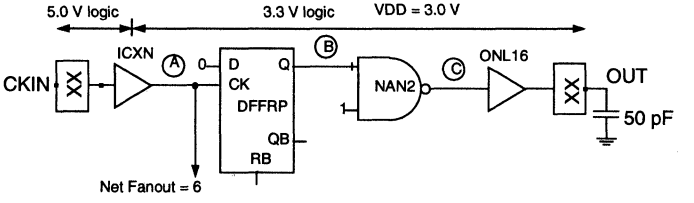

Figure 3-20 Example Delay Path

3.6.2 Example Delay Calculation

The delay calculation for path CKIN to OUT in Figure 3-20 is demonstrated below. The assumptions are: P = worst-case, T = 70° C, VDD = 3.0 V, t_r = 1.0 ns at CKIN, and the array is an H4CP109. The values for the no-load delays (t_{PLH0}, t_{PHL0}) and K-factors can be found in the Switching Characteristics (SC) tables in Section 7 for macros ICXN, DFFRP, NAN2, and ONL16.

The input signal swing to macro ICXN is 5.0 V and the core logic is 3.3 V, with a 3.3 V output macro. Each delay calculation must take into account the logic signal swing and the associated VDD voltage. For I/O macros there are four possible logic signal swings to consider and associated VDD voltages and for the core macros only two logic swings and associated VDD voltages are possible.

Only the rising edge will trigger the clock input of DFFRP and the path is CKIN to the CK input of DFFRP. The DFFRP CK input is non-inverting, therefore only the rising edge will be calculated for the input path to DFFRP input CK. The path from DFFRP Q output to the OUT pin will have both rising and falling edges calculated.

3.6.2.1 Delay from CKIN to Node A

The signal at CKIN is a 5.0 V logic swing with a rise time of 1.0 ns and the signal at point A is a 3.3 V logic swing. The macro type is ICXN with VDD = 3.0 V since all input macros are tied to the core power bus. The input ESD diode is connected to 5.0 V because it is interfacing to a 5.0 V logic level. The correct SC table for this macro has a heading of 5.0/3.3 V. The rising edge delay time is calculated by using Eq. (3-27).

$$t_{PLH} = (0.39 + 0.05 + 0.15\,(1.27))\,1.66 = 1.05\text{ns}$$

where:

The first term t_{PLH0} is the rising macro no-load delay. This number is from the ICXN SC table. t_{PLH0} = 0.39

The term t_{INP_r} is the input rise time delay. This number is from Table 3-24, for a 1.0 ns rise time. t_{INP_r} = 0.05

The third term K1(C_{Lout}) is composed of two parts. The first K1 is the rising load sensitivity K-factor and is from the ICXN SC table. The other part C_{Lout} is the

capacitive load on Node A and is determined from Table 3-27, for array type H4CP109 with a fanout of 6.
K1 =0.15, C_{Lout} = 1.27 pF

The last term, PTV, is from Table 3-25. PTV = 1.66

3.6.2.2 Delay from Node A to Node B

From this point on two cases must be considered. Case1 is when DFFRP output Q is a rising edge and case 2, when DFFRP output Q is a falling edge. Each case will retain the phase information through out this example, so that case 1 and 2 may be summed at the end, for a total input output delay for each output edge.

Case 1:

The signal at A is a 3.3 V logic swing with an unknown rise time and a fanout of 6. The signal at point B is a 3.3 V logic swing. The macro type is DFFRP, and the SC table heading is 3.3 V. The rising edge delay time will be calculated, but first the input rise time of the driving signal at point A needs to be calculated.

Node A rise time is calculated by using Eq. (3-1).

$$t_r = 0.15 + 0.35\,(1.27) = 0.59\text{ns}$$

where:

The first term t_{r0} is the no-load output rise time from the driving macro, ICXN. This number is determined from the ICXN SC table. t_{r0} = 0.15

The next term K3(C_{Lin}) is composed of two parts, the first, K3, is the output rising time K-factor and is determined from the ICXN SC table. The other part, C_{Lin}, is the capacitive load on Node A, is determined from Table 3-27, for array type H4CP109 with a fanout of 6.
K3 = 0.35, C_{Lin} = 1.27 pF

Now that the rise time of node A is known. The rising edge delay time is calculated by using Eq. (3-27).

$$t_{PLH} = (1.23 + 0.01 + 1.17\,(0.29))\,1.66 = 2.62\text{ns}$$

where:

The first term t_{PLH0} is the rising macro no-load delay. This number is determined from the DFFRP SC table. t_{PLH0} = 1.23

The term t_{INP_r} is the input rise time delay. This number is determined from Table 3-24, using the 0.59 ns rise time that was calculated above. $t_{INP_r} \approx 0.01$

The third term, K1(C_{Lout}), is composed of two parts, the first, K1, is the rising load sensitivity K-factor and is determined from the DFFRP SC table. The other part, C_{Lout}, is the capacitive load on Node B and is determined from Table 3-27, for array type H4CP109 with a fanout of one. K1 = 1.17, C_{LOUT} = 0.29 pF

The last term PTV is from Table 3-25. PTV = 1.66

Case 2:

The signal at A is a 3.3 V logic swing with a 0.59 ns rise time as calculated above in Case 1. The signal at point B is a 3.3 V logic swing. The macro type is DFFRP, and the SC table heading is 3.3 V. The falling edge delay time will be calculated, by using Eq. (3-28) with a small change. The second term t_{INP_f} is changed to the rising edge t_{INP_r} because only the rising edge will trigger the clock input of macro DFFRP.

$$t_{PHL} = (1.32 + 0.01 + 0.92\,(0.29))\,1.66 = 2.65\text{ns}$$

Where each term is determined similarly as in case 1.

3.6.2.3 Node B to Node C

Two cases need to be considered. Case 1 is when the NAN2 output is a falling edge and case 2, when the NAN2 output is a rising edge.

Case 1:

The signal at B is a 3.3 V logic swing with an unknown rise time and a fanout of one. The signal at point C is a 3.3 V logic swing. The macro type is NAN2, and the SC table heading is 3.3 V.

First, the input rise time of the driving signal at point B must be calculated. The input signal is inverted propagating through macro NAN2, so the falling output delay calculation requires that the input rise time be used. Node B rise time is calculated by using Eq. (3-1).

$$t_r = 0.23 + 3.42\,(0.29) = 1.22\text{ns}$$

Where each term is determined similarly as previously described.

Now that the rise time of node B is known, the falling edge delay time will be calculated by using Eq. (3-28) with a small change. The second term, t_{INP_f}, is changed to the rising edge t_{INP_r} because of the input edge being inverted as it passes through macro NAN2.

$$t_{PHL} = (0.34 + 0.12 + 1.50\,(1.14))\,1.66 = 3.61\text{ns}$$

Where each term is determined similarly as previously described.

C_{Lout} is the capacitive load on Node C. The load on Node C is equivalent to one ONL16 plus the metal for a fanout of one.

Use the equation below to find the capacitive load on Node C.

$$C_{Lout} = IPC + C_m$$

$$C_{Lout} = 0.90 + 0.24 = 1.14\text{pF}$$

where:

The first term is IPC of the output macro. This number is determined from the ONL16 input capacitance table. IPC = 0.90

The last term is from Table 3-27. Cm = 0.24

Case 2:

The signal at B is a 3.3 V logic swing with an unknown fall time and a fanout of one. The signal at point C is a 3.3 V logic swing. The macro type is NAN2, and the SC table heading is 3.3 V.

First, the input fall time of the driving signal at point B must be calculated. Node B fall time is calculated by using Eq. (3-30).

$$t_f = 0.21 + 1.41\,(0.29) = 0.62\text{ns}$$

Where each term is determined similarly as previously described.

Now that the fall time of node B is known, the rising edge delay time will be calculated by using Eq. (3-27) with a small change. The second term, t_{INP_f}, is changed to the falling edge t_{INP_f} because of the input edge being inverted as it passes through macro NAN2.

$$t_{PLH} = (0.17 + 0.01 + 1.15\,(1.14))\,1.66 = 2.48\text{ns}$$

Where each term is determined similarly as previously described.

3.6.2.4 Node C to Pad OUT

Two cases need to be considered. Case 1 is when the ONL16 output is a falling edge and case 2, when the ONL16 output is a rising edge.

Case 1:

The signal at C is a 3.3 V logic swing with an unknown fall time and a fanout of two. The signal at point OUT is a 3.3 V logic swing. The macro type is ONL16, and the SC table heading is 3.3 V.

First, the input fall time of the driving signal at point C must be calculated. Node C fall time is calculated by using Eq. (3-30).

$$t_f = 0.22 + 2.54\,(1.14) = 3.12\text{ns}$$

Where each term is determined similarly as previously described.

Now that the fall time of node C is known, the falling edge delay time will be calculated by using Eq. (3-28).

$$t_{PHL} = (0.82 + 0.31 + 0.02\,(50))\,1.66 = 3.53\text{ns}$$

C_{LOUT} is the capacitive load on Node OUT. The load on Node OUT is 50 pF. C_{LOUT} = 50 pF

All other terms are determined similarly as previously described.

Case 2:

The signal at C is a 3.3 V logic swing with an unknown rise time and a fanout of two. The signal at point OUT is a 3.3 V logic swing. The macro type is ONL16, and the SC table heading is 3.3 V.

First the input rise time of the driving signal at point C must be calculated. Node C rise time is calculated by using Eq. (3-1).

$$t_r = 0.29 + 3.44\,(1.14) = 4.21\text{ns}$$

Where each term is determined similarly as previously described.

Now that the rise time of node C is known, the rising edge delay time will be calculated by using Eq. (3-27).

$$t_{PLH} = (0.71 + 0.53 + 0.02\,(50))\,1.66 = 3.71\text{ns}$$

C_{Lout} is the capacitive load on Node OUT. The load on Node OUT is 50 pF. C_{Lout} = 50 pF

All other terms are determined similarly as previously described.

3.6.2.5 The Total Path Delay

The total delay from CKIN to OUT is the sum of the delays across each macro. The two cases are not identical because the rising and falling delays are not the same. The general equation is:

$$\Sigma t_P = t_{P(CKINtoA)} + t_{P(AtoB)} + t_{P(BtoC)} + t_{P(CtoOUT)}$$

For Case 1 the delay total is:

$$\Sigma t_P = 1.05 + 2.62 + 3.61 + 3.53 = 10.81\text{ns}$$

For Case 2 the delay total is:

$$\Sigma t_P = 1.05 + 2.65 + 2.48 + 3.71 = 9.89\text{ns}$$

3.7 METALLIZED SRAMs

The H4CPlus Series library includes a family of asynchronous single-, dual-, and quad-port metallized SRAM blocks up to 2304 bits. Single-port SRAMs are designed for low-power and dual-port SRAMs are optimized for high-speed. A comprehensive guide to using these blocks and their performance is shown in the SRAM macro data sheets in Section 7.5.

Table 3-28 Features of Metallized SRAMs

Feature	Metal Rams
Strobe	Asynchronous
Ports	Single, Dual, Quad
Construction	Gate-array Based
Max. Words	64 (SP)
Bits/Word	9-72 (DP)
Max. Block Size	2304 bits
Min. Gate Density	~3 gates/bit
Availability	fixed sizes
Routing Impact	M2 partial, M3 open

Table 3-29 Sizes of Metallized SRAMs

Metallized SRAM Sizes		
Single-Port, Low-Power	Dual-Port, High-Speed	Quad-Port
8x8	8x9	16x18
8x18	8x18	16x36
16x8	8x36	32x18
16x18	8x72	32x36
16x36	16x9	
32x8	16x18	
32x18	16x36	
32x36	16x72	
64x18	32x9	
64x36	32x18	
	32x36	
	32x72	

3.7.1 Multiple Memory Blocks

It is possible to combine two or more memory blocks to create larger memory blocks. When multiple memory blocks are used, the customer is responsible for creating the external decoder logic needed. The maximum number of SRAM blocks on an array is restricted to 16, depending on array/SRAM sizes.

3.7.2 Array Sizing

To choose an array into which a design with SRAM(s) will fit, two considerations must be evaluated: the physical size/layout of the SRAM(s) and the gate utilization. This information is given in the SRAM macro data sheets in Section 7.5.

3.8 ANALOG PHASE LOCKED LOOP

Motorola's analog phase locked loop (APLL) optimizes ASIC and system-level clock skew by reducing insertion delay and providing frequency multiplication. Clock skew is caused by the difference in insertion delay required for the system clock to propagate into each IC. Further, insertion delay into an IC is dependent on the load of the internal clock tree and the input edge rate. The APLL controls IC-to-IC clock skew by synchronizing their internal clocks with the system clock. For further description regarding the use of the APLL for maximizing operating frequencies see application note, *AN1522/D, Analog Phase-Locked-Loop for H4CPlus and M5C Arrays.*

Motorola's Analog PLL Features:

- Supported output clock rates (FVCO):
  60 to 160 MHz @ 3.3 V
  70 to 250 MHz @ 5.0 V
- Lock Time < 25 µs
- Input reference frequency:
  FREF = FVCO/N where N ≤16
- ± 200 ps jitter
- Phase Error ± 50 ps single-ended input
- Phase Error ± 200 ps differential input
- No external components required
- Insertion delay reduction
- Frequency multiplication
- Application note available

Table 3-30 APLL Macro Selection Guide

Macro	VDD	Clock Input	N = FVCO/FREF
APL1	3.3 V	Single-ended (CMOS)	1 ≤ N ≤ 4
APDL1	3.3 V	Differential (PECL)	1 ≤ N ≤ 4
APL2	3.3 V	Single-ended (CMOS)	5 ≤ N ≤ 16
APDL2	3.3 V	Differential (PECL)	5 ≤ N ≤ 16
AP1	5.0 V	Single-ended (CMOS)	1 ≤ N ≤ 4
APD1	5.0 V	Differential (PECL)	1 ≤ N ≤ 4
AP2	5.0 V	Single-ended (CMOS)	5 ≤ N ≤ 16
APD2	5.0 V	Differential (PECL)	5 ≤ N ≤ 16

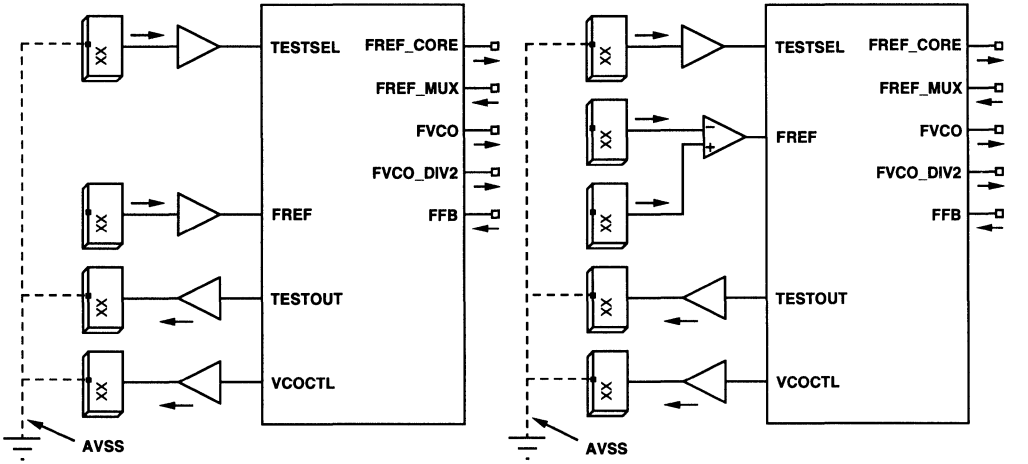

Figure 3-21 Analog PLL Macro Symbols

3.8.1 General Description

Two basic versions of the APLL are offered. A normal CMOS single-ended clock input version (FREF), and a PECL differential clock input version (FREF and FREFB). In addition, different versions exist for 3.3 V and 5.0 V cores as well as for the integer multiple (N) between output and input reference frequencies. All together, eight combinations of the APLL exist and are summarized in Table 3-30. As an example, if an APLL is desired to operate with a 3.3 V core, single-ended (S.E.) clock input and with an integer multiple of 10 (FREF = FVCO/ 10), the APL2 macro would be selected.

On arrays which use 3.3 V and 5.0 V power simultaneously, the APLL I/O's are powered by the same supply as the array core.

3.8.2 APLL Macrocell Descriptions

The APLL macro symbol is shown in Figure 3-21 and is supported in Motorola's H4CPlus Series library. Three test pins are utilized to bypass the APLL to test the core logic and to test the APLL. The three test pins are tied to AVSS in the application. Table 3-31 contains a description of the six (seven for differential PECL) fixed I/O pins for the APLL. Table 3-32 describes the five APLL signals which interface to the array core. Up to two APLL's may be used on an array. If one APLL is used, P1 must be appended to the array name in design_info and the APLL is located in the lower left corner of the die. If two APLL's are used, P2 is appended to the array name and the second APLL is located in the upper right corner of the die.

Table 3-31 Analog PLL Pin Description

Pin Name	Description
AVDD	Analog VDD Supply (for low noise)
AVSS	Analog VSS Supply (for low noise)
FREF	Reference Frequency Input (CMOS and PECL)
FREFB	Reference Frequency Input (PECL)

Pin Name	Description
TESTSEL	Test Select (for test only)
TESTOUT	Output Frequency (for test only)
VCOCTL	VCO control voltage (for test only)

Table 3-32 Analog PLL Core Signal Descriptions

Signal Name	Description
FFB	Input to the phase det. from clock tree
FREF_CORE	Output to the Core from the Input Buffer
FREF_MUX	Input to the phase det. from ref. freq.

Signal Name	Description
FVCO	VCO output
FVCO_DIV2	VCO output ÷ 2

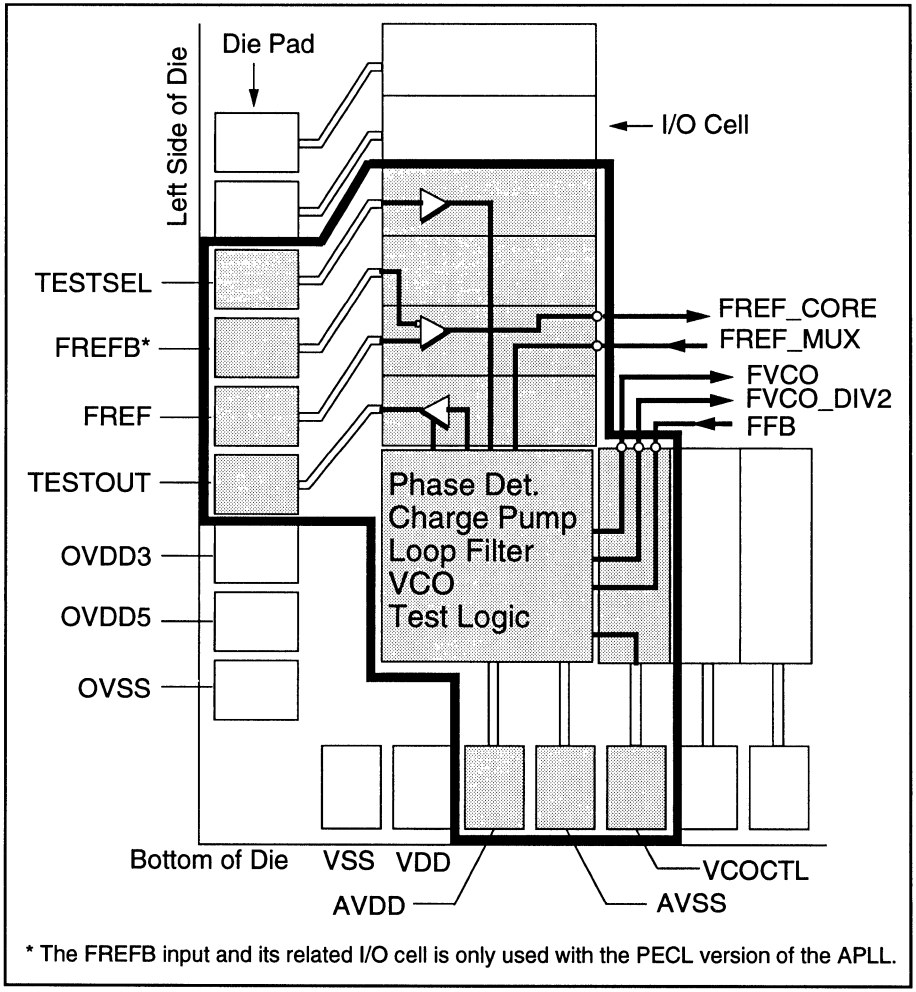

Figure 3-22 Typical Analog PLL Layout

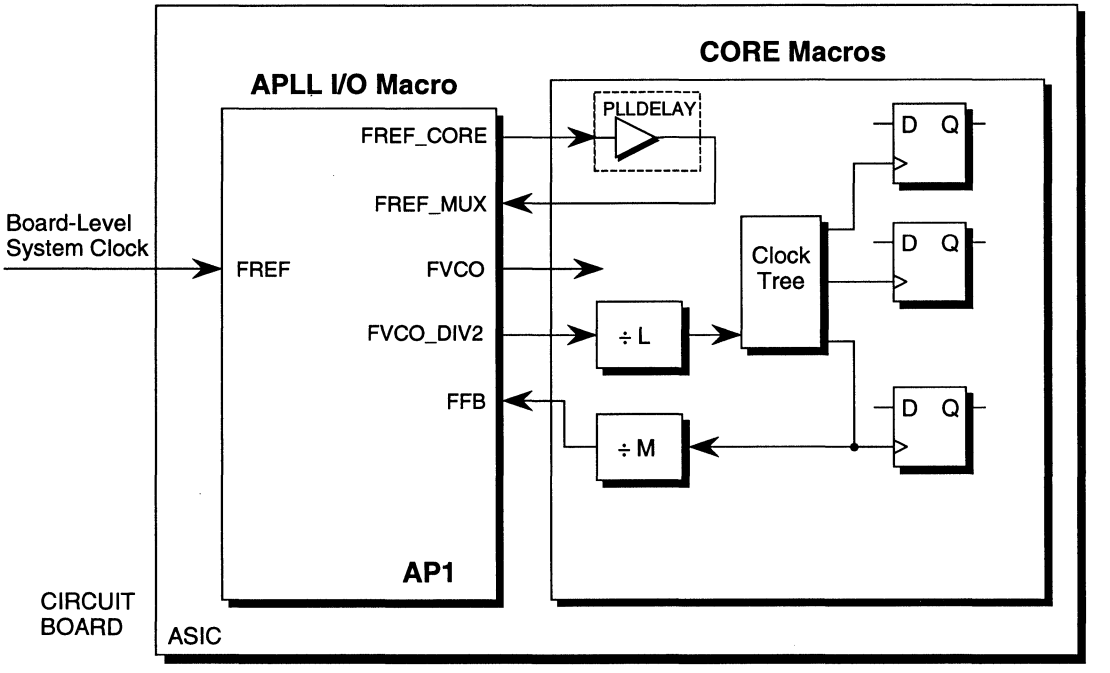

Figure 3-23 Clock Distribution with APLL

Figure 3-22 shows the lower left corner of an H4CPlus array with a PECL Differential APLL. All of the circuitry is located inside the thick black line and uses four (five with PECL input) I/O cell sites. For single-ended APLL macros, signal FREFB is not used and TESTSEL is placed in that location. Only the first three die pads and I/O cells are used on the left side of the die with a single-ended clock input (FREF).

Figure 3-23 contains a typical application of the APLL. The divider blocks (÷ L and ÷ M) are used to adjust for desired clock frequencies and to center the APLL FVCO and FVCO_DIV2 outputs. The PLLDELAY macro is a delay element for matching the delay of the M divider block when M > 1. As an example, assume a 5.0 Volt core, and a 40 MHz clock tree is desired. With an input reference frequency of 20 MHz, L = 2 and M = 2. By selecting N = 8, (2 x 2 x 2), the FVCO_DIV2 is forced to 80 MHz. This is approximately the middle of the operation frequency range, since the FVCO_DIV2 range is between 35 and 125 MHz. (In this example macro PLLDELAY is used to adjust delay times.)

3.8.3 APLL Operation

Figure 3-24 contains a block diagram of the APLL macro. Basically, the APLL is a classical second order system that compares the phase of the input reference clock (FREF) with the phase of the feedback signal (FFB), and adjusts the phase of the FFB signal to be locked in phase and frequency with the FREF signal. It uses a type IV phase/frequency detector that sends correction pulses to a charge pump. The charge pump, based on the correction pulses, either adds or subtracts charge from the on-chip passive loop filter, thereby altering the control voltage of the VCO. The VCO, in turn, produces a different phase and frequency which is fedback to the phase detector. Correction pulses are generated until the APLL is locked. Frequency multiplication is easily implemented by putting a digital divider in the feedback path.

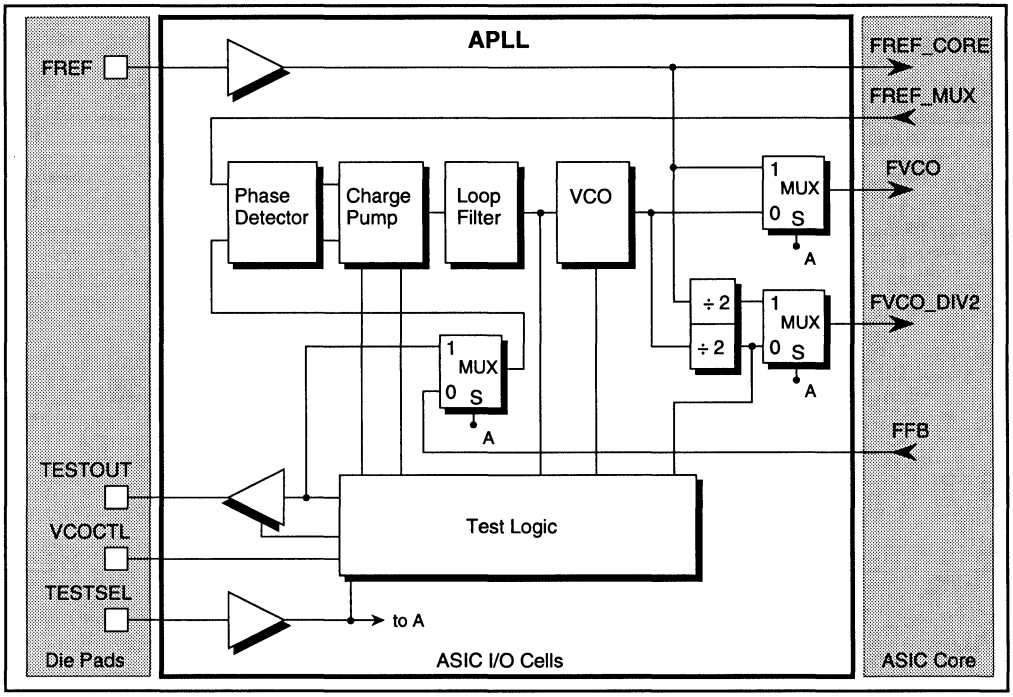

Figure 3-24 APLL Block Diagram

3.9 JTAG BOUNDARY SCAN

JTAG is a standardized boundary scan methodology used for board-level testing to detect faults in package and board connections, as well as internal circuitry. In 1985, a group of European companies (Joint Test Action Group) developed a method of system test which was later standardized. This standard, IEEE 1149.1, defines testing of interconnections between ICs, internal IC circuitry, and observing and modifying normal circuit operation.

Motorola fully supports the IEEE 1149.1 standard with a complete family of JTAG I/O buffers and JTAG control functions.

A complete guide to the use of Motorola's JTAG is available in an application note, *AN1500/D, IEEE Std. 1149.1 Boundary Scan for H4C™ Arrays With H4CPlus™ Supplement.*

3.9.1 General Description

The minimum IEEE 1149.1 JTAG architecture, see Figure 3-25, consists of a Test Access Port, TAP controller, scannable instruction register, bypass register, and boundary scan register. Device ID and design test registers are optional.

3.9.1.1 TAP and I/O Periphery Signals

The Test Access Port (TAP) provides access to on-chip test structures and consists of five externally accessible signals which are used to control and observe boundary scan test data. (An additional pin is required if Mustang ATPG is used.)

TCK is the test clock used to synchronize all JTAG functions and allow test data flow independent of the system clock. The Test Mode Select signal, TMS, controls the operation of the JTAG circuitry by controlling the TAP controller. TRSTB is an optional reset input for the TAP controller. TDI and TDO are the Test Data Input and Output ports for test instructions and data.

Six internal JTAG signal lines encircle the periphery of the array to provide efficient interconnection for the JTAG I/O macrocells. These signal lines include CKDR, SHDR, UDDR, IMC, OMC, and TDI/TDO (TDI and TDO share the same signal network). Except for TDI/TDO, these signals require special buffers to interface the I/O periphery with the JTAG logic within the core.

Motorola JTAG Features:

- IEEE 1149.1 standard
- Minimum impact on silicon area and performance
- Mustang and FastScan ATPG compatible
- Only four pins are required for JTAG signals

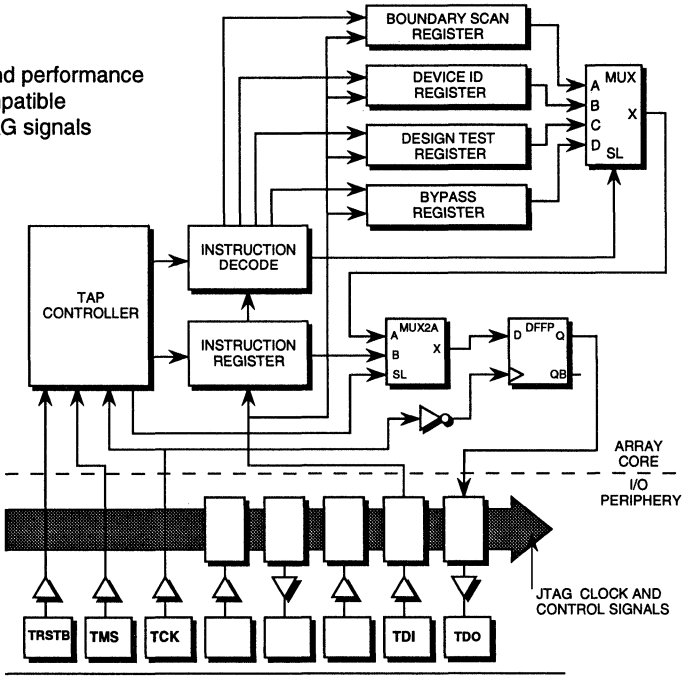

Figure 3-25 Simplified JTAG Functional Diagram

3.9.1.2 JTAG Control and Test Registers

The **TAP Controller** (FMC_TAPC) is a synchronous, 16-state machine which controls and manages the mode of operation for the test circuitry, see Figure 3-26. An example of the operation of the tap controller is shown in Figure 3-27 where the TAP controller is sequenced through most of its test states. The TAP controller (FMC_TAPC) is a soft macro that is placed as a unit.

The **Instruction Register** encodes various public and private instructions defining which test registers are used and the serial test data register path between TDI and TDO. Public instructions are defined by the 1149.1 specification to perform several basic tasks, see Table 3-33. *Extest* checks the board interconnections between components, *Intest* is used to perform tests on the internal logic of the ASIC, *Sample* allows the normal operation of the ASIC while sampling external I/O signals, *IDcode* selects the Device ID register to extract the identification code, and *Bypass* selects the Bypass register to redirect the test data from TDI directly to TDO, effectively removing the IC from the boundary scan chain. Private instructions are defined by the user to perform additional tasks as needed. The Instruction Register is configured from MC_IREG or MC_IREG4 macros to provide the necessary number of instruction bits.

The **Instruction Decoder** is user-defined and translates the instructions into separate signals for controlling the test registers and register multiplexer.

The **Boundary Scan Register** is the chain of JTAG I/O macrocells that are linked together to form a shift register around the periphery of the array. This register enables non-intrusive monitoring of I/O signals and the scanning of predetermined patterns into the register to produce a known condition in the I/O buffers. Test data enters the boundary scan register through the TDI port, then is shifted around the array through each JTAG I/O cell in a counterclockwise direction, and finally exits through the TDO port. Non-JTAG I/O macrocells and unused I/O sites are not part of the boundary scan register, and therefore are transparent to the test data movement.

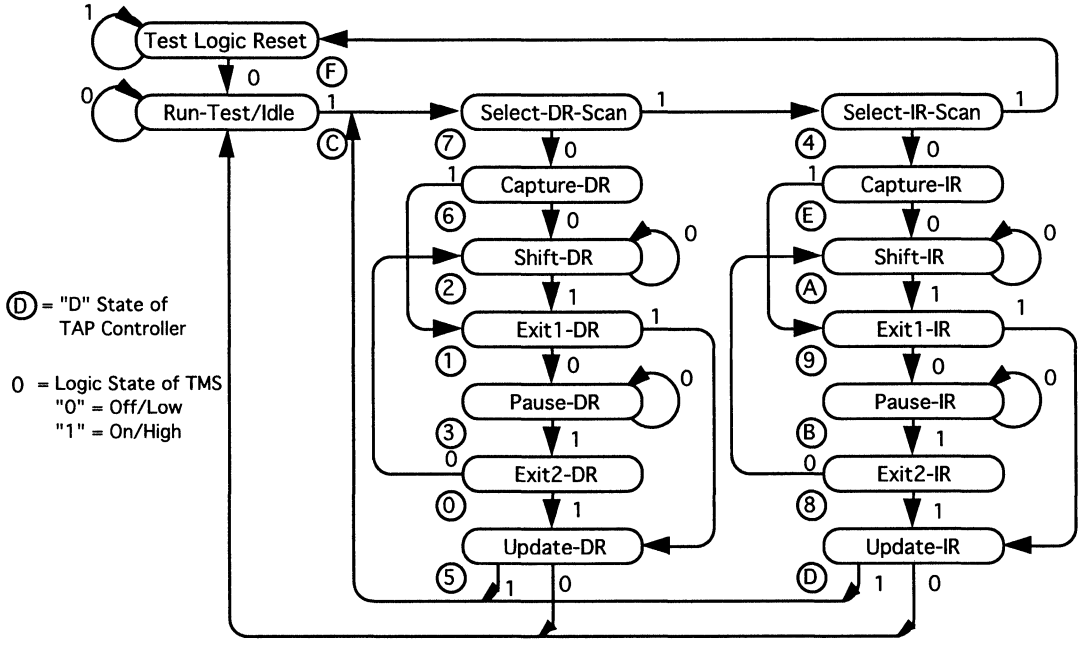

Figure 3-26 TAP Controller 16-State Diagram

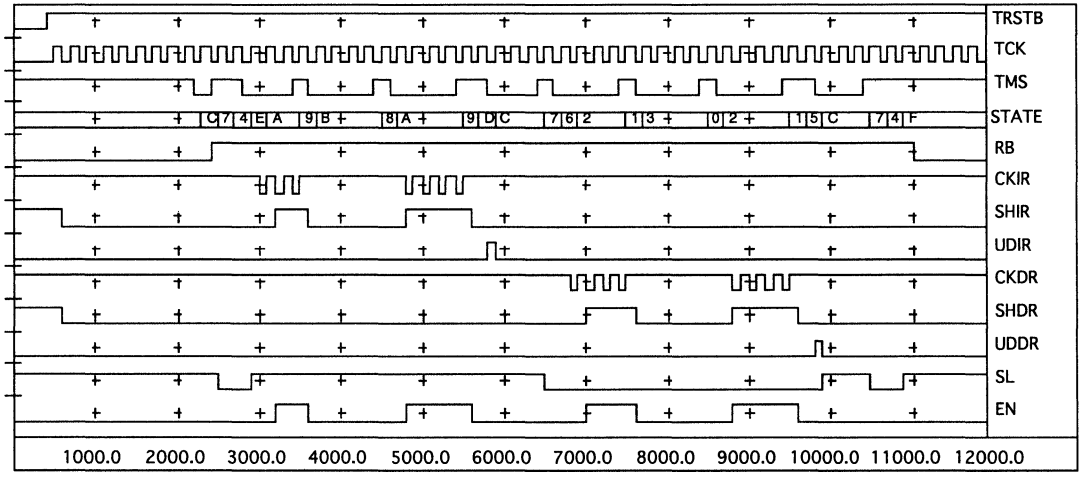

Figure 3-27 Example Timing Diagram for JTAG Test Cycle

Table 3-33 Public Instructions

Instruction Register Bits			Instruction	Register	Mode
I2	I1	I0			
0	0	0	Extest*	Boundary Scan	Test
0	0	1	Intest	Boundary Scan	Test
0	1	0	Sample*	Boundary Scan	Normal
0	1	1	Optional		
1	0	0	IDcode	Device ID	Normal
1	0	1	Optional		
1	1	0	Optional		
1	1	1	Bypass*	Bypass	Normal

* Required

The **Bypass Register** is a single-bit shift register used to provide the shortest path between TDI and TDO. This enables the scan chain of one ASIC to be minimized so that another component may be more easily tested. The Bypass register is implemented using a BPREG macro.

The **Device Identification Register** is a 32-bit register which holds a manufacturer's identity code, part number and version code. The bit assignment for the ID code is given in Table 3-34. **Customers must use a Motorola assigned JTAG identification numbers.** Please contact a Motorola sales representative for information.

Table 3-34 IDREG ID Codes

Bit #	Code Use
0-11	Motorola Inc. Identification
12-21	Sequence Number
22-27	Motorola ASIC Identification
28-31	Version Number

Design Test Registers are design-dependent and are optionally used to provide additional design-specific testability. Various forms of scan methodologies, including Edge/Level Sensitive Scan Design (ESSD/LSSD) and Built-In Self Test (BIST), can be used.

3.9.2 General Design Guidelines

The following guidelines are presented here to provide a general view of JTAG design requirements.

Guidelines for Designing with JTAG:

- Special design rules apply depending on array size, speed requirements, and Mustang ATPG compatibility for ESSD/LSSD scan.
- When using the ISS2000™ tester, TDI, TDOUT, TMS and TCK I/O macros must each be assigned to a "scannable" package pin identified by an asterisk (*) in the pad-to-pin cross-reference tables.
- All JTAG output buffers have high-drive versions available for greater current capacity.
- All JTAG I/O macros must comply with standard ERC (electrical rule checks) for non-JTAG I/O.
- Some JTAG macros require either an I/O site without a bonding pad or an I/O site whose pad is not assigned to a package pin.

3.10 H4CPlus Versus H4C Performance

Major performance improvements have been achieved in the design of H4CPlus in comparison to H4C. The performance improvements are in the output drive strength (IDS) of the devices. However, because device sizes are the same, major intrinsic delay improvements are not expected. There are four factors which contribute to the internal macro improvements.

1. The drive factor for H4CPlus is better.
2. Input gate loading capacitance is lower (0.05 v.s. 0.06 pF).
3. Routed metal capacitance is lower.
4. Typical rise time will be faster than H4C.

The combination of these factors result in better rise/fall times and therefore better performance. This performance improvement has been verified in test cases using Verilog and Decal. Improvement can also be verified by running a timing simulation on critical nets using the Motorola OACS system.

Data published in the reference guides may not always seem to support the performance improvements. The reason for this is in data presentation. The H4CPlus library data uses a more accurate measurement for voltage input threshold (0.4 X VDD), where in H4C VDD/2 was used for the AC measurement. The major difference in the generation of the data within the reference guides is in the balanced "B" macros (i.e. NAN2B). The "B" type macros were not characterized at their actual threshold of 2.5 V for H4CPlus, and therefore the two edges will appear unbalanced.

PACKAGES AND ARRAY FLOORPLANS

4

4 PACKAGES AND ARRAY FLOORPLANS

SECTION 4. PACKAGES AND ARRAY FLOORPLANS

4.1 PACKAGE SELECTION

Table 4-1 Package Selection

ARRAY NAME		H4CP028	H4CP048	H4CP075	H4CP109	H4CP146	H4CP178
CDA Array (Die Size)		239	287	337	391	438	476
# of I/O Cells		160	208	256	312	360	400
# of Programmable Signal or Power and Ground Pads*		156	184	212	252	280	304
# of Dedicated Power and Ground Pads*		20	32	44	52	64	72
PACKAGE TYPE							
128 QFP (CU)	Q	A,F	A,F	A,F			
160 QFP (CU)	Q	A	A,F	A,F	A,F		
208 QFP (CU)	Q		A	A,F	A,F		
240 QFP (CU)					A,F		
160 MicroCool (CD)	Q				A,F	A,F	A,F
208 MicroCool (CD)	Q				A,F	A,F	A,F
169 OMPAC (CU)	Q	A	A	A			
225 OMPAC (CU)	Q		A	A	A	P	P
313 OMPAC (CU)					A	A	A

*Numbers indicate Wirebond pads availability
QFP: Plastic Quad Flat Pack (CU) denotes Cavity Up (CD) denotes Cavity Down
MicroCool: QFP-type package with heat slug
All QFPs and MicroCools are manufactured with Molded Carrier Ring (MCR)
OMPAC: Over-Molded Pad Array Carrier, a PGA type package with solder balls instead of pins,
Prototypes for the 169 and 225 OMPAC are supplied in a GTPAC package (see Page 4-70 and Page 4-75 for mechanical drawings)
A- Available
F- Flexible power pin assignment.
P- Planned.
Q- Qualified. (Consult factory for qualification status)
Note: The 225 OMPAC package is limited to the following three combinations of mixed (System/Core) power combinations:
5 V / 5 V, 3 V & 5 V / 5 V, and 3 V / 3 V.

4.2 PACKAGE THERMAL AND POWER INFORMATION

Table 4-2 Estimated Theta Junction to Ambient for Packages

Package	H4CP Array	Die Size	Cavity/ Flag Size	Thermal Resistance - Junction to Ambient ($R_{\Theta JA}$)				
				Free Air	100 LFM	200 LFM	300 LFM	500 LFM
128 QFP (CU) ♦	H4CP028	239 X 239	300 X 300	31.6	29.4	28.0	27.2	26.2
160 QFP(CU) ♦	H4CP028	239 X 239	380 X 380	31.8	29.6	28.0	27.2	26.4
128 QFP (CU) ♦	H4CP048	287 X 287	300 X 300	30.7	28.3	26.9	26.2	25.2
160 QFP(CU) ♦	H4CP048	287 X 287	350 X 350	30.9	28.5	27.1	26.4	25.4
208 QFP (CU) ♦	H4CP048	287 X 287	380 X 380	28.6	26.0	25.2	24.7	24.2
128 QFP (CU) ♦	H4CP075	337 X 337	350 X 350	27.9	25.5	24.0	23.2	22.3
160 QFP (CU) ♦	H4CP075	337 X 337	400 X 400	28.0	25.7	24.2	23.4	22.5
208 QFP (CU) ♦	H4CP075	337 X 337	380 X 380	27.6	25.0	24.2	23.7	23.2
160 QFP (CU) ♦	H4CP109	391 X 391	450 X 450	25.2	23.0	21.4	20.7	19.8
208 QFP(CU) ♦	H4CP109	391 X 391	450 X 450	24.9	22.3	21.5	21.0	20.5
240 QFP(CU) Δ	H4CP109	391 X 391	453 X 453	21.0	17.7	16.5	15.7	13.2
160 MicroCool (CD) ♦	H4CP109	391 X 391	452 X 452	16.1	14.8	13.7	13	11.5
208 MicroCool (CD) ♦	H4CP109	391 X 391	452 X 452	16.2	14.9	13.8	13.0	11.6
160 MicroCool (CD) ♦	H4CP146	438 X 438	535 X 535	16.0	14.7	13.6	12.8	11.4
208 MicroCool (CD) ♦	H4CP146	438 X 438	535 X 535	16.1	14.8	13.6	12.9	11.5
160 MicroCool (CD) ♦	H4CP178	476 X 476	535 X 535	15.8	14.6	13.4	12.7	11.3
208 MicroCool (CD) ♦	H4CP178	476 X 476	535 X 535	15.9	14.6	13.5	12.8	11.3
169 OMPAC (CU) ♦	H4CP028	239 X 239	278 X 278	28.2	24.1	22.8	21.9	21.0
169 OMPAC (CU) ♦	H4CP048	287 X 287	296 X 296	27.0	23.1	21.8	21.0	20.0
225 OMPAC (CU) ♦	H4CP048	287 X 287	296 X 296	24.0	20.4	18.9	18.1	16.8
169 OMPAC (CU) ♦	H4CP075	337 X 337	347 X 352	23.9	20.5	19.3	18.6	17.8
225 OMPAC (CU) ♦	H4CP075	337 X 337	347 X 352	23.1	19.6	18.2	17.4	16.1
225 OMPAC (CU) ♦	H4CP109	391 X 391	431 X 431	22.2	18.8	17.5	16.7	15.5
313 OMPAC (CU) Δ	H4CP109	391 X 391	431 X 431	22.2	18.8	17.5	16.7	15.5
313 OMPAC (CU) Δ	H4CP146	438 X 438	478 X 478	21.1	17.9	16.6	15.9	14.7
313 OMPAC (CU) Δ	H4CP178	476 X 476	515 X 515	20.1	17.0	15.8	15.1	14.0

Note: See conditional information regarding power dissipation in section 4.3

QFP: Plastic Quad Flat Pack MCR: Molded Carrier Ring (CD)
MicroCool: QFP-Type Package with heat slug
OMPAC™: Over-Molded Pad Array Carrier, a PGA type package with solder balls instead of pins

n/a = not available at this time
(CD) Denotes Cavity Down
(CU) Denotes Cavity Up

♦: Actual, thermal test die used and characterized using a thermally enhanced test board.

Δ: Preliminary information.

Note: Die and Cavity/Flag size are in mils x mils. Die Sizes listed are not actual, but are a close approximation.

4.3 CHOOSING A PACKAGE

Package cooling decisions will differ depending on which power level target the customer wants to meet. Hence, the thermal resistance data is interpreted to provide recommendations for package cooling. The following examples describe probable environmental conditions anticipated when utilizing "low power" CMOS technology in various system markets.

1. In the **Mainframe Computer Market**, forced air cooling with 500 LFM airflow is standard in the industry. Designers generally expect to use a heatsink with any package. Currently the most prevalent T_J(max) in this specific market is 105°C, with the highest ambient temperature of the system specified at 60°C.
2. In the **Small Mainframe, Workstation, and PC Markets** the most desirable cooling is passive, meaning free air cooling (possibly aided by utilizing a heatsink). If any airflow in these systems is to be tolerated, it will be minimal (less than 300 LFM at the location of the package). In this market T_J(max) is between 70 - 85°C, with the highest system ambient temperature typically at 40°C.
3. The **Telecommunications Market** generally uses no forced air or other special cooling capabilities but these systems allow for higher T_J(max), typically up to 115°C with system ambient temperatures of 70°C.

This wide variation, in both anticipated cooling environments and temperature differentials between package and ambient, clearly dictates the implementation of differently designed packages.

The following is one example of a package and its associated estimated power dissipation which illustrates the considerations required to make a proper choice in packaging.

208 QFP:

This package can dissipate up to 1.5 W of power in a telecom environment with the 45°C temperature differential and 1.3 W in the PC environment without forced air. But in the 500 LFM airflow, mainframe environment, the power dissipation could be raised to nearly 2.0 W.

4.4 CALCULATING JUNCTION TEMPERATURE:

A calculation of the average junction temperature is based on the concept of thermal resistance between the junction and a temperature reference point on the case. A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_A + (R\Theta_{JA} \times P_D)$$

where: T_J = Junction Temperature (°C)

T_A= Ambient Temperature (°C)

$R\Theta_{JA}$ =Thermal Resistance Junction to Ambient as specified (°C/W).

P_D = power dissipated in the device (W).

4.5 FIXED POWER AND GROUND

Each array has fixed power and ground as noted in the array footprints and in the pin to pad tables. In the pin to pad tables, fixed power and ground pads, VSS, VDD, OVSS, OVDD3 and OVDD5 on the die are for probe test and are array dependent. These are identified by () around the I/O cell number. Package dependent power and ground, OVSS and OVDD5 are for final test and are noted in the pin to pad tables by () around the word, OVSS, OVDD5.

Note:

In the 225 OMPAC package the power planes tie VDD and OVDD5 together which limits it to the following three combinations of mixed (Core/System) power combinations:

5 V / 5 V, 5 V / 3 V & 5 V, and 3 V / 3 V.

4.6 ANALOG PHASE LOCK LOOP

Each of the H4CPlus Arrays has the option of adding an Analog Phase Lock Loop (APLL). There are two APLL options available, APLL option 1 - located in the bottom left corner of the array or APLL option 2 -located in the bottom left **and** top right corners of the array. I/O to pad interconnect will change for the top and or the bottom side of the array and pad to pin tables will change accordingly. I/O to pad interconnect tables for each APLL option have been added to the end of each array portion of Section 4. Naming convention for the APLL options are as follows:

H4CPXXX	Base Array -No APLL
H4CPXXXP1	Base Array -with 1 APLL
H4CPXXXP2	Base Array -with 2 APLL

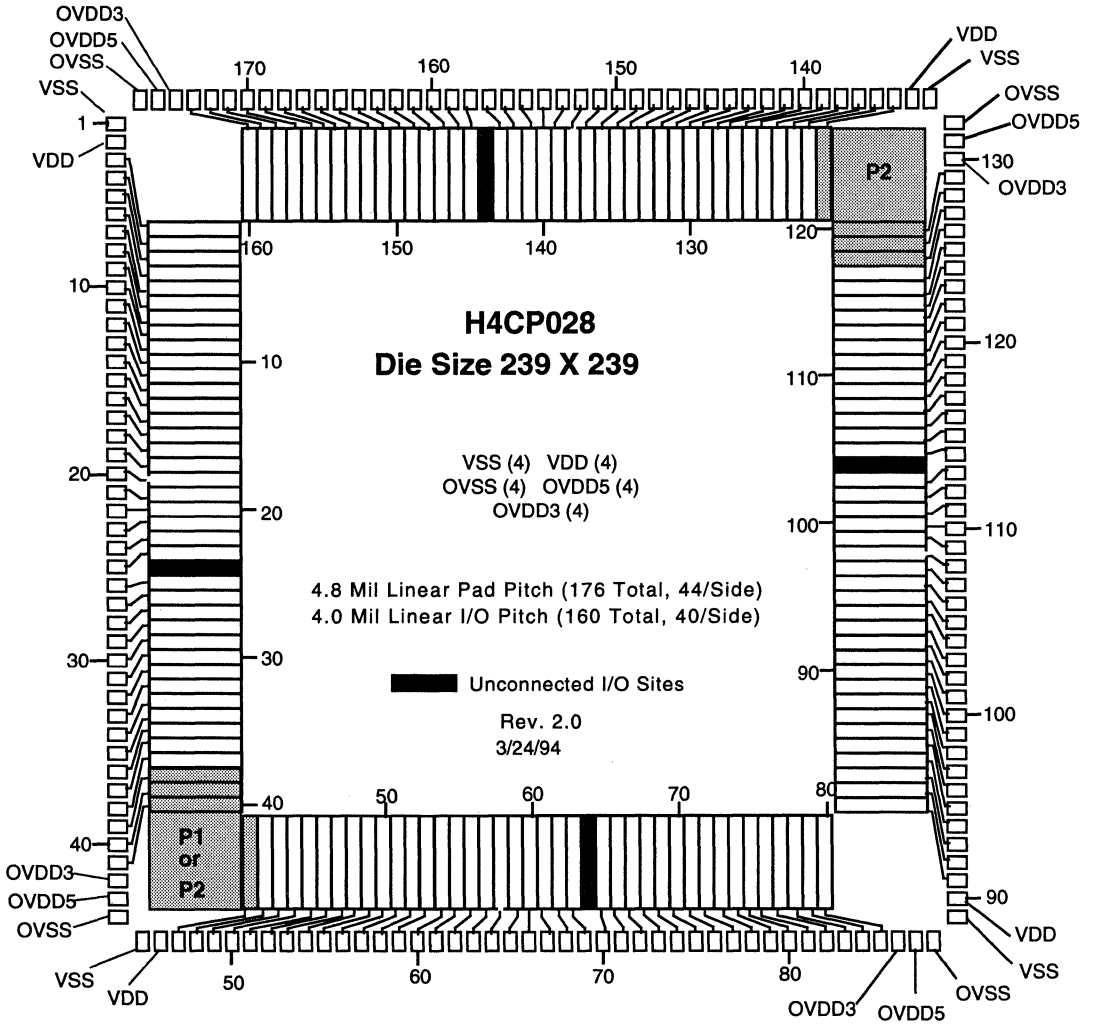

Figure 4-1 H4CP028 Footprint

Note:
P1 = Analog PLL option 1 (H4CP028P1) bottom left corner only,
see Table 4-6 for I/O to pad configuration.
P2 = Analog PLL option 2 (H4CP028P2) bottom left and top right corners,
see Table 4-7 for I/O to pad configuration.

Table 4-3 H4CP028 128 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	45	VSS	-	89	VSS	-	133	VSS	-
2	VDD	-	46	VDD	-	90	VDD	-	134	VDD	-
3	1	1	47	41	33	91	81	65	135	121	97
4	2	2	48	42	34	92	82	66	136	122	98
5	3	3	49	43	35	93	83	67	137	123	99
6	4	4	50	44	36	94	84	68	138	124	100
7	5	-	51	45	-	95	85	-	139	125	-
8	6	5	52	46	37	96	86	69	140	126	101
9	7	6	53	47	38	97	87	70	141	127	102
10	8	7	54	48	39	98	88	71	142	128	103
11	9	8	55	49	40	99	89	72	143	129	104
12	10	-	56	50	-	100	90	-	144	130	-
13	11	9	57	51	41	101	91	73	145	131	105
14	12	10	58	52	42	102	92	74	146	132	106
15	13	11	59	53	43	103	93	75	147	133	107
16	14	12	60	54	44	104	94	76	148	134	108
17	15	-	61	55	-	105	95	-	149	135	-
18	16	13	62	56	45	106	96	77	150	136	109
19	17	14	63	57	46	107	97	78	151	137	110
20	18	15	64	58	47	108	98	79	152	138	111
21	19	16	65	59	48	109	99	80	153	139	112
22	20	-	66	60	-	110	100	-	154	140	-
23	21	17	67	61	49	111	101	81	155	141	113
24	22	18	68	62	50	112	102	82	156	142	114
25	23	19	69	63	51	113	103	83	157	143	115
26	25	20	70	65	52	114	105	84	158	145	116
27	26	-	71	66	-	115	106	-	159	146	-
28	27	21	72	67	53	116	107	85	160	147	117
29	28	22	73	68	54	117	108	86	161	148	118
30	29	23	74	69	55	118	109	87	162	149	119
31	30	24	75	70	56	119	110	88	163	150	120
32	31	-	76	71	-	120	111	-	164	151	-
33	32	25	77	72	57	121	112	89	165	152	121
34	33	26	78	73	58	122	113	90	166	153	122
35	34	27	79	74	59	123	114	91	167	154	123
36	35	28	80	75	60	124	115	92	168	155	124
37	36	-	81	76	-	125	116	-	169	156	-
38	37	29	82	77	61	126	117	93	170	157	125
39	38	30	83	78	62	127	118	94	171	158	126
40	39	31	84	79	63	128	119	95	172	159	127
41	40	32	85	80	64	129	120	96	173	160	128
42	OVDD3	-	86	OVDD3	-	130	OVDD3	-	174	OVDD3	-
43	OVDD5	-	87	OVDD5	-	131	OVDD5	-	175	OVDD5	-
44	OVSS	-	88	OVSS	-	132	OVSS	-	176	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die(Array) for probe test.
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Table 4-4 H4CP028 160 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	45	VSS	-	89	VSS	-	133	VSS	-
2	VDD	-	46	VDD	-	90	VDD	-	134	VDD	-
3	1	1	47	41	41	91	81	81	135	121	121
4	2	2	48	42	42	92	82	82	136	122	122
5	3	3	49	43	43	93	83	83	137	123	123
6	4	4	50	44	44	94	84	84	138	124	124
7	5	5	51	45	45	95	85	85	139	125	125
8	6	6	52	46	46	96	86	86	140	126	126
9	7	7	53	47	47	97	87	87	141	127	127
10	8	8	54	48	48	98	88	88	142	128	128
11	9	9	55	49	49	99	89	89	143	129	129
12	10	10	56	50	50	100	90	90	144	130	130
13	11	11	57	51	51	101	91	91	145	131	131
14	12	12	58	52	52	102	92	92	146	132	132
15	13	13	59	53	53	103	93	93	147	133	133
16	14	14	60	54	54	104	94	94	148	134	134
17	15	15	61	55	55	105	95	95	149	135	135
18	16	16	62	56	56	106	96	96	150	136	136
19	17	17	63	57	57	107	97	97	151	137	137
20	18	18	64	58	58	108	98	98	152	138	138
21	19	19	65	59	59	109	99	99	153	139	139
22	20	20	66	60	60	110	100	100	154	140	140
23	21	21	67	61	61	111	101	101	155	141	141
24	22	22	68	62	62	112	102	102	156	142	142
25	23	23	69	63	63	113	103	103	157	143	143
26	25	24	70	65	64	114	105	104	158	145	144
27	26	25	71	66	65	115	106	105	159	146	145
28	27	26	72	67	66	116	107	106	160	147	146
29	28	27	73	68	67	117	108	107	161	148	147
30	29	28	74	69	68	118	109	108	162	149	148
31	30	29	75	70	69	119	110	109	163	150	149
32	31	30	76	71	70	120	111	110	164	151	150
33	32	31	77	72	71	121	112	111	165	152	151
34	33	32	78	73	72	122	113	112	166	153	152
35	34	33	79	74	73	123	114	113	167	154	153
36	35	34	80	75	74	124	115	114	168	155	154
37	36	35	81	76	75	125	116	115	169	156	155
38	37	36	82	77	76	126	117	116	170	157	156
39	38	37	83	78	77	127	118	117	171	158	157
40	39	38	84	79	78	128	119	118	172	159	158
41	40	39	85	80	79	129	120	119	173	160	159
42	OVDD3	-	86	OVDD3	-	130	OVDD3	-	174	OVDD3	-
43	OVDD5	-	87	OVDD5	-	131	OVDD5	-	175	OVDD5	-
44	OVSS	40	88	OVSS	80	132	OVSS	120	176	OVSS	160

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die(Array) for probe test.

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Table 4-5 H4CP028 169 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
1	VSS	1	a	45	VSS	44	a	89	VSS	87	a	133	VSS	130	a
2	VDD	2	A1	46	VDD	45	N1	90	VDD	88	N13	134	VDD	131	A13
3	1	3	E5	47	41	46	J5	91	81	89	J9	135	121	132	E9
4	2	4	D3	48	42	47	L4	92	82	90	K11	136	122	133	C10
5	3	5	B1	49	43	48	N2	93	83	91	M13	137	123	134	A12
6	4	6	C2	50	44	49	M3	94	84	92	L12	138	124	135	B11
7	5	7	F6	51	45	50	H6	95	85	93	H8	139	125	136	F8
8	6	8	E4	52	46	51	K5	96	86	94	J10	140	126	137	D9
9	7	9	C1	53	47	52	N3	97	87	95	L13	141	127	138	A11
10	8	10	D2	54	48	53	M4	98	88	96	K12	142	128	139	B10
11	9	11	E3	55	49	54	L5	99	89	97	J11	143	129	140	C9
12	10	12	D1	56	50	55	N4	100	90	98	K13	144	130	141	A10
13	11	13	F5	57	51	56	J6	101	91	99	H9	145	131	142	E8
14	12	14	E2	58	52	57	M5	102	92	100	J12	146	132	143	B9
15	13	15	E1	59	53	58	N5	103	93	101	J13	147	133	144	A9
16	14	16	F3	60	54	59	L6	104	94	102	H11	148	134	145	C8
17	15	17	F2	61	55	60	M6	105	95	103	H12	149	135	146	B8
18	16	18	F4	62	56	61	K6	106	96	104	H10	150	136	147	D8
19	17	19	F1	63	57	62	N6	107	97	105	H13	151	137	148	A8
20	18	20	G5	64	58	63	J7	108	98	106	G9	152	138	149	E7
21	19	21	G2	65	59	64	M7	109	99	107	G12	153	139	150	B7
22	20	22	G1	66	60	65	N7	110	100	108	G13	154	140	151	A7
23	21	23	G3	67	61	66	L7	111	101	109	G11	155	141	152	C7
24	22	24	G4	68	62	67	K7	112	102	110	G10	156	142	153	D7
25	23	25	H1	69	63	68	N8	113	103	111	F13	157	143	154	A6
26	25	26	H2	70	65	69	M8	114	105	112	F12	158	145	155	B6
27	26	27	H5	71	66	70	J8	115	106	113	F9	159	146	156	E6
28	27	28	H3	72	67	71	L8	116	107	114	F11	160	147	157	C6
29	28	29	J1	73	68	72	N9	117	108	115	E13	161	148	158	A5
30	29	30	J2	74	69	73	M9	118	109	116	E12	162	149	159	B5
31	30	31	H4	75	70	74	K8	119	110	117	F10	163	150	160	D6
32	31	32	K1	76	71	75	N10	120	111	118	D13	164	151	161	A4
33	32	33	J3	77	72	76	L9	121	112	119	E11	165	152	162	C5
34	33	34	K2	78	73	77	M10	122	113	120	D12	166	153	163	B4
35	34	35	J4	79	74	78	K9	123	114	121	E10	167	154	164	D5
36	35	36	L1	80	75	79	N11	124	115	122	C13	168	155	165	A3
37	36	37	K3	81	76	80	L10	125	116	123	D11	169	156	166	C4
38	37	38	L2	82	77	81	M11	126	117	124	C12	170	157	167	B3
39	38	39	M1	83	78	82	N12	127	118	125	B13	171	158	168	A2
40	39	40	K4	84	79	83	K10	128	119	126	D10	172	159	169	D4
41	40	41	L3	85	80	84	L11	129	120	127	C11	173	160	170	C3
42	OVDD3	-	-	86	OVDD3	-	-	130	OVDD3	-	-	174	OVDD3	-	-
43	OVDD5	42	M2	87	OVDD5	85	M12	131	OVDD5	128	B12	175	OVDD5	171	B2
44	OVSS	43	a	88	OVSS	86	a	132	OVSS	129	a	176	OVSS	172	a

NOTES:

1. Die Pad/IO-Cell numbers start at top of LEFT side and increment counter-clockwise.
2. Pkg Pin and Bond FInger numbers start at top of LEFT side and increment counter-clockwise.
3. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die (Array) for probe test.
4. OVSS & OVDD5 in () are power and ground for Final Test and are fixed on the Package.
5. The following is a cross reference of package dependent Power and Ground Pkg Pin numbers:
GND: a=F7, G6, G7, G8, H7

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Table 4-6 H4CP028P1
Analog PLL Option 1

BOTTOM	
DIE PAD	I/O CELL
45	VSS
46	VDD
47	AVSS
48	AVDD
49	41
50	42
51	43
52	44
53	45
54	46
55	47
56	48
57	49
58	50
59	52
60	53
61	54
62	55
63	57
64	58
65	59
66	60
67	61
68	62
69	63
70	65
71	66
72	67
73	68
74	69
75	70
76	71
77	72
78	73
79	74
80	75
81	76
82	77
83	78
84	79
85	80
86	OVDD3
87	OVDD5
88	OVSS

Note: This table replaces the BOTTOM side of each pad to pin table for each array/package combination when Analog PLL option 1 is used in the H4CP028 array.

Table 4-7 H4CP028P2
Analog PLL Option 2

BOTTOM		TOP	
DIE PAD	I/O CELL	DIE PAD	I/O CELL
45	VSS	133	VSS
46	VDD	134	VDD
47	AVSS	135	AVSS
48	AVDD	136	AVDD
49	41	137	121
50	42	138	122
51	43	139	123
52	44	140	124
53	45	141	125
54	46	142	126
55	47	143	127
56	48	144	128
57	49	145	129
58	50	146	130
59	52	147	132
60	53	148	133
61	54	149	134
62	55	150	135
63	57	151	137
64	58	152	138
65	59	153	139
66	60	154	140
67	61	155	141
68	62	156	142
69	63	157	143
70	65	158	145
71	66	159	146
72	67	160	147
73	68	161	148
74	69	162	149
75	70	163	150
76	71	164	151
77	72	165	152
78	73	166	153
79	74	167	154
80	75	168	155
81	76	169	156
82	77	170	157
83	78	171	158
84	79	172	159
85	80	173	160
86	OVDD3	174	OVDD3
87	OVDD5	175	OVDD5
88	OVSS	176	OVSS

Note: This table replaces the BOTTOM and the TOP side of each pad to pin table for each array/package combination when Analog PLL option 2 is used in the H4CP028 array.

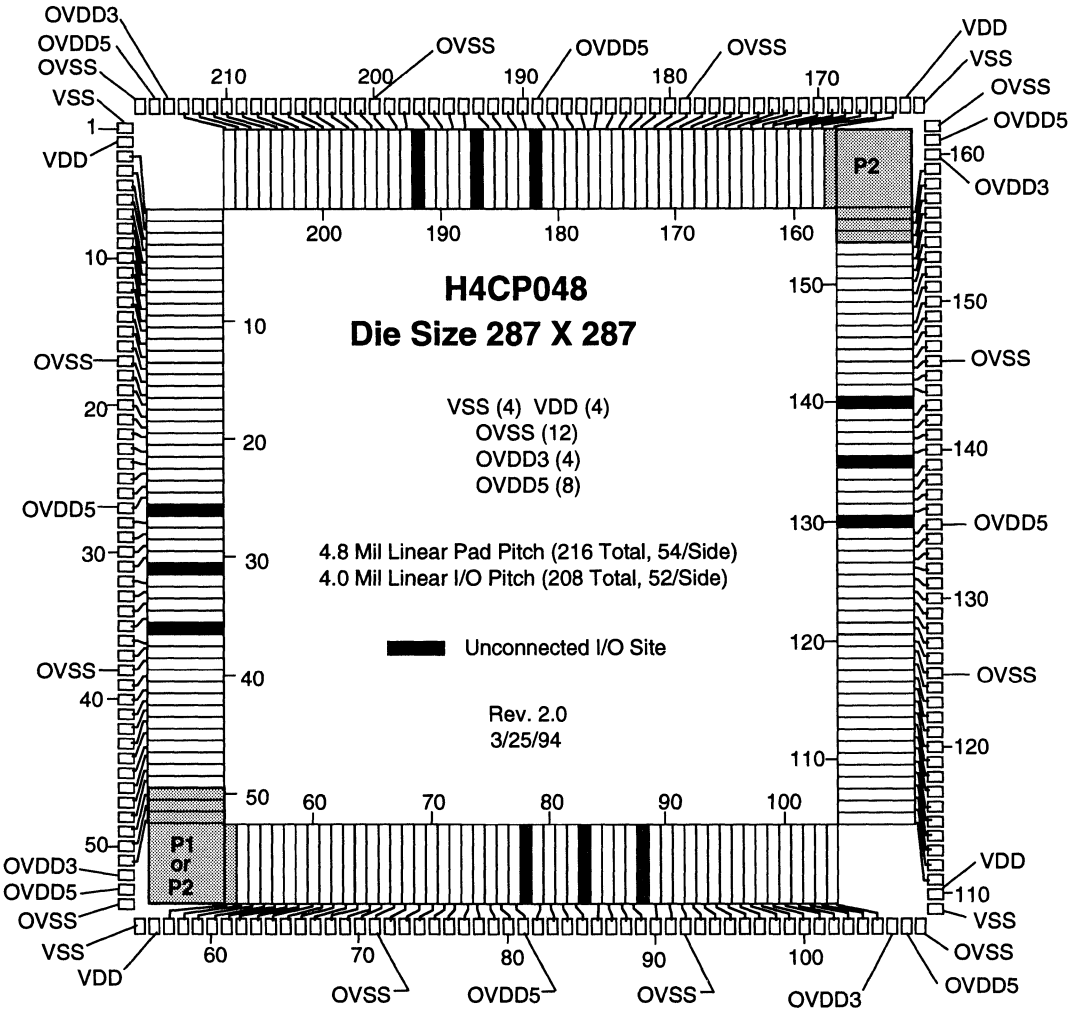

Figure 4-2 H4CP048 Footprint

Note:
P1 = Analog PLL option 1 (H4CP048P1) bottom left corner only,
see Table 4-13 for I/O to pad configuration.
P2 = Analog PLL option 2 (H4CP048P2) bottom left and top right corners,
see Table 4-14 for I/O to pad configuration.

Table 4-8 H4CP048 128 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	55	VSS	-	109	VSS	-	163	VSS	-
2	VDD	-	56	VDD	-	110	VDD	-	164	VDD	-
3	1	1	57	53	33	111	105	65	165	157	97
4	2	2	58	54	34	112	106	66	166	158	98
5	3	3	59	55	35	113	107	67	167	159	99
6	4	4	60	56	36	114	108	68	168	160	100
7	5	5	61	57	37	115	109	69	169	161	101
8	6	6	62	58	38	116	110	70	170	162	102
9	7	-	63	59	-	117	111	-	171	163	-
10	8	7	64	60	39	118	112	71	172	164	103
11	9	8	65	61	40	119	113	72	173	165	104
12	10	-	66	62	-	120	114	-	174	166	-
13	11	9	67	63	41	121	115	73	175	167	105
14	12	10	68	64	42	122	116	74	176	168	106
15	13	11	69	65	43	123	117	75	177	169	107
16	14	-	70	66	-	124	118	-	178	170	-
17	OVSS(15)	-	71	OVSS(67)	-	125	OVSS(119)	-	179	OVSS(171)	-
18	16	12	72	68	44	126	120	76	180	172	108
19	17	13	73	69	45	127	121	77	181	173	109
20	18	-	74	70	-	128	122	-	182	174	-
21	19	-	75	71	-	129	123	-	183	175	-
22	20	-	76	72	-	130	124	-	184	176	-
23	21	14	77	73	46	131	125	78	185	177	110
24	22	15	78	74	47	132	126	79	186	178	111
25	23	16	79	75	48	133	127	80	187	179	112
26	24	-	80	76	-	134	128	-	188	180	-
27	OVDD5(25)	-	81	OVDD5(77)	-	135	OVDD5(129)	-	189	OVDD5(181)	-
28	27	-	82	79	-	136	131	-	190	183	-
29	28	17	83	80	49	137	132	81	191	184	113
30	29	18	84	81	50	138	133	82	192	185	114
31	30	19	85	82	51	139	134	83	193	186	115
32	32	-	86	84	-	140	136	-	194	188	-
33	33	-	87	85	-	141	137	-	195	189	-
34	34	-	88	86	-	142	138	-	196	190	-
35	35	20	89	87	52	143	139	84	197	191	116
36	37	21	90	89	53	144	141	85	198	193	117
37	38	-	91	90	-	145	142	-	199	194	-
38	OVSS(39)	-	92	OVSS(91)	-	146	OVSS(143)	-	200	OVSS(195)	-
39	40	22	93	92	54	147	144	86	201	196	118
40	41	23	94	93	55	148	145	87	202	197	119
41	42	24	95	94	56	149	146	88	203	198	120
42	43	-	96	95	-	150	147	-	204	199	-
43	44	25	97	96	57	151	148	89	205	200	121
44	45	26	98	97	58	152	149	90	206	201	122
45	46	-	99	98	-	153	150	-	207	202	-
46	47	27	100	99	59	154	151	91	208	203	123
47	48	28	101	100	60	155	152	92	209	204	124
48	49	29	102	101	61	156	153	93	210	205	125
49	50	30	103	102	62	157	154	94	211	206	126
50	51	31	104	103	63	158	155	95	212	207	127
51	52	32	105	104	64	159	156	96	213	208	128
52	OVDD3	-	106	OVDD3	-	160	OVDD3	-	214	OVDD3	-
53	OVDD5	-	107	OVDD5	-	161	OVDD5	-	215	OVDD5	-
54	OVSS	-	108	OVSS	-	162	OVSS	-	216	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die(Array) for probe test.

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Table 4-9 H4CP048 160 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	55	VSS	-	109	VSS	-	163	VSS	-
2	VDD	-	56	VDD	-	110	VDD	-	164	VDD	-
3	1	1	57	53	41	111	105	81	165	157	121
4	2	2	58	54	42	112	106	82	166	158	122
5	3	3	59	55	43	113	107	83	167	159	123
6	4	4	60	56	44	114	108	84	168	160	124
7	5	5	61	57	45	115	109	85	169	161	125
8	6	6	62	58	46	116	110	86	170	162	126
9	7	7	63	59	47	117	111	87	171	163	127
10	8	8	64	60	48	118	112	88	172	164	128
11	9	9	65	61	49	119	113	89	173	165	129
12	10	-	66	62	-	120	114	-	174	166	-
13	11	10	67	63	50	121	115	90	175	167	130
14	12	11	68	64	51	122	116	91	176	168	131
15	13	12	69	65	52	123	117	92	177	169	132
16	14	13	70	66	53	124	118	93	178	170	133
17	OVSS(15)	-	71	OVSS(67)	-	125	OVSS(119)	-	179	OVSS(171)	-
18	16	14	72	68	54	126	120	94	180	172	134
19	17	15	73	69	55	127	121	95	181	173	135
20	18	-	74	70	-	128	122	-	182	174	-
21	19	16	75	71	56	129	123	96	183	175	136
22	20	17	76	72	57	130	124	97	184	176	137
23	21	-	77	73	-	131	125	-	185	177	-
24	22	18	78	74	58	132	126	98	186	178	138
25	23	19	79	75	59	133	127	99	187	179	139
26	24	20	80	76	60	134	128	100	188	180	140
27	OVDD5(25)	-	81	OVDD5(77)	-	135	OVDD5(129)	-	189	OVDD5(181)	-
28	27	21	82	79	61	136	131	101	190	183	141
29	28	22	83	80	62	137	132	102	191	184	142
30	29	-	84	81	-	138	133	-	192	185	-
31	30	23	85	82	63	139	134	103	193	186	143
32	32	24	86	84	64	140	136	104	194	188	144
33	33	-	87	85	-	141	137	-	195	189	-
34	34	25	88	86	65	142	138	105	196	190	145
35	35	26	89	87	66	143	139	106	197	191	146
36	37	27	90	89	67	144	141	107	198	193	147
37	38	28	91	90	68	145	142	108	199	194	148
38	OVSS(39)	-	92	OVSS(91)	-	146	OVSS(143)	-	200	OVSS(195)	-
39	40	29	93	92	69	147	144	109	201	196	149
40	41	30	94	93	70	148	145	110	202	197	150
41	42	31	95	94	71	149	146	111	203	198	151
42	43	-	96	95	-	150	147	-	204	199	-
43	44	32	97	96	72	151	148	112	205	200	152
44	45	33	98	97	73	152	149	113	206	201	153
45	46	34	99	98	74	153	150	114	207	202	154
46	47	35	100	99	75	154	151	115	208	203	155
47	48	36	101	100	76	155	152	116	209	204	156
48	49	37	102	101	77	156	153	117	210	205	157
49	50	38	103	102	78	157	154	118	211	206	158
50	51	39	104	103	79	158	155	119	212	207	159
51	52	40	105	104	80	159	156	120	213	208	160
52	OVDD3	-	106	OVDD3	-	160	OVDD3	-	214	OVDD3	-
53	OVDD5	-	107	OVDD5	-	161	OVDD5	-	215	OVDD5	-
54	OVSS	-	108	OVSS	-	162	OVSS	-	216	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die(Array) for probe test.

Rev 1.0 6/18/93 JEB

Table 4-10 H4CP048 169 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
1	VSS	1	a	55	VSS	48	a	109	VSS	96	a	163	VSS	143	a
2	VDD	-	-	56	VDD	-	-	110	VDD	-	-	164	VDD	-	-
3	1	2	A1	57	53	49	N1	111	105	97	N13	165	157	144	A13
4	2	3	B1	58	54	50	K4	112	106	98	M13	166	158	145	D10
5	3	4	C2	59	55	51	N2	113	107	99	L12	167	159	146	A12
6	4	5	C1	60	56	52	M3	114	108	100	L13	168	160	147	B11
7	5	6	D3	61	57	53	N3	115	109	101	K11	169	161	148	A11
8	(OVDD5)6	7	c	62	(OVDD5)58	54	d	116	(OVDD5)110	102	e	170	(OVDD5)162	149	b
9	7	8	D2	63	59	55	L4	117	111	103	K12	171	163	150	C10
10	8	9	D1	64	60	56	M4	118	112	104	K13	172	164	151	B10
11	9	10	E4	65	61	57	N4	119	113	105	J10	173	165	152	A10
12	10	-	-	66	62	-	-	120	114	-	-	174	166	-	-
13	11	11	E3	67	63	58	K5	121	115	106	J11	175	167	153	D9
14	12	12	E2	68	64	59	L5	122	116	107	J12	176	168	154	C9
15	13	13	E1	69	65	60	M5	123	117	108	J13	177	169	155	B9
16	(OVDD5)14	14	c	70	(OVDD5)66	61	d	124	(OVDD5)118	109	e	178	(OVDD5)170	156	b
17	OVSS(15)	15	a	71	OVSS(67)	62	a	125	OVSS(119)	110	a	179	OVSS(171)	157	a
18	16	16	F4	72	68	63	N5	126	120	111	H10	180	172	158	A9
19	17	17	F3	73	69	64	K6	127	121	112	H11	181	173	159	D8
20	18	18	F2	74	70	65	L6	128	122	113	H12	182	174	160	C8
21	19	19	F1	75	71	66	M6	129	123	114	H13	183	175	161	B8
22	20	20	F5	76	72	67	N6	130	124	115	H9	184	176	162	A8
23	21	21	G4	77	73	68	J6	131	125	116	G10	185	177	163	E8
24	22	-	-	78	74	69	K7	132	126	-	-	186	178	164	D7
25	23	22	G2	79	75	70	M7	133	127	117	G12	187	179	165	B7
26	24	23	G1	80	76	71	N7	134	128	118	G13	188	180	166	A7
27	OVDD5(25)	-	-	81	OVDD5(77)	-	-	135	OVDD5(129)	-	-	189	OVDD5(181)	-	-
28	27	24	G3	82	79	72	L7	136	131	119	G11	190	183	167	C7
29	(OVSS)28	25	a	83	(OVSS)80	73	a	137	(OVSS)132	120	a	191	(OVSS)184	168	a
30	29	26	G5	84	81	74	J7	138	133	121	G9	192	185	169	E7
31	30	27	H5	85	82	75	J8	139	134	122	F9	193	186	170	E6
32	32	28	H1	86	84	76	N8	140	136	123	F13	194	188	171	A6
33	33	29	H2	87	85	77	M8	141	137	124	F12	195	189	172	B6
34	34	30	H3	88	86	78	L8	142	138	125	F11	196	190	173	C6
35	35	-	-	89	87	-	-	143	139	-	-	197	191	-	-
36	37	31	H4	90	89	79	K8	144	141	126	F10	198	193	174	D6
37	38	32	J1	91	90	80	N9	145	142	127	E13	199	194	175	A5
38	OVSS(39)	33	a	92	OVSS(91)	81	a	146	OVSS(143)	128	a	200	OVSS(195)	176	a
39	(OVDD5)40	34	d	93	(OVDD5)92	82	e	147	(OVDD5)144	129	b	201	(OVDD5)196	177	c
40	41	35	J2	94	93	83	M9	148	145	130	E12	202	197	178	B5
41	42	36	J3	95	94	84	L9	149	146	131	E11	203	198	179	C5
42	43	37	J4	96	95	85	K9	150	147	132	E10	204	199	180	D5
43	44	38	K1	97	96	86	N10	151	148	133	D13	205	200	181	A4
44	45	39	K2	98	97	87	M10	152	149	134	D12	206	201	182	B4
45	46	40	K3	99	98	88	L10	153	150	135	D11	207	202	183	C4
46	(OVDD5)47	41	d	100	(OVDD5)99	89	e	154	(OVDD5)151	136	b	208	(OVDD5)203	184	c
47	48	42	L1	101	100	90	N11	155	152	137	C13	209	204	185	A3
48	49	43	L2	102	101	91	M11	156	153	138	C12	210	205	186	B3
49	50	44	L3	103	102	92	L11	157	154	139	C11	211	206	187	C3
50	51	45	M1	104	103	93	N12	158	155	140	B13	212	207	188	A2
51	52	46	M2	105	104	94	M12	159	156	141	B12	213	208	189	B2

Table 4-10 H4CP048 169 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
52	OVDD3	-	-	106	OVDD3	-	-	160	OVDD3	-	-	214	OVDD3	-	-
53	OVDD5	-	-	107	OVDD5	-	-	161	OVDD5	-	-	215	OVDD5	-	-
54	OVSS	47	a	108	OVSS	95	a	162	OVSS	142	a	216	OVSS	190	a

NOTES:

1. Die Pad/IO-Cell numbers start at top of LEFT side and increment counter-clockwise.
2. Pkg Pin and Bond FInger numbers start at top of LEFT side and increment counter-clockwise.
3. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die(Array) for probe test.
4. OVSS & OVDD5 in () are power and ground for Final Test and are Package dependent
5. The following is a cross reference of package dependent Power and Ground Pin numbers:

GND: a = H6, H7, H8, G6, G7, G8, F6, F7, F8

PWR: b = E9, c = E5, D4, d =J5, e = J9, K10

6. Only OVDD5 is connected to package PWR pins.
7. VDD must be supplied separately through I/O package pins for all applications.
8. OVDD3 must be supplied separately through I/O package pins for mixed voltage (5V / 3.3V applications).

Rev. 1.0 6/18/93 JEB

Rev. 1.1 5/11/94 JEB added note 6.

Table 4-11 H4CP048 208 QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	1	55	VSS	53	109	VSS	105	163	VSS	157
2	VDD	2	56	VDD	54	110	VDD	106	164	VDD	158
3	1	3	57	53	55	111	105	107	165	157	159
4	2	4	58	54	56	112	106	108	166	158	160
5	3	5	59	55	57	113	107	109	167	159	161
6	4	6	60	56	58	114	108	110	168	160	162
7	5	7	61	57	59	115	109	111	169	161	163
8	6	8	62	58	60	116	110	112	170	162	164
9	7	9	63	59	61	117	111	113	171	163	165
10	8	10	64	60	62	118	112	114	172	164	166
11	9	11	65	61	63	119	113	115	173	165	167
12	10	-	66	62	-	120	114	-	174	166	-
13	11	12	67	63	64	121	115	116	175	167	168
14	12	13	68	64	65	122	116	117	176	168	169
15	13	14	69	65	66	123	117	118	177	169	170
16	14	15	70	66	67	124	118	119	178	170	171
17	OVSS(15)	16	71	OVSS(67)	68	125	OVSS(119)	120	179	OVSS(171)	172
18	16	17	72	68	69	126	120	121	180	172	173
19	17	18	73	69	70	127	121	122	181	173	174
20	18	19	74	70	71	128	122	123	182	174	175
21	19	20	75	71	72	129	123	124	183	175	176
22	20	21	76	72	73	130	124	125	184	176	177
23	21	22	77	73	74	131	125	126	185	177	178
24	22	23	78	74	75	132	126	127	186	178	179
25	23	24	79	75	76	133	127	128	187	179	180
26	24	25	80	76	77	134	128	129	188	180	181
27	OVDD5(25)	26	81	OVDD5(77)	78	135	OVDD5(129)	130	189	OVDD5(181)	182
28	27	27	82	79	79	136	131	131	190	183	183
29	28	28	83	80	80	137	132	132	191	184	184
30	29	29	84	81	81	138	133	133	192	185	185
31	30	30	85	82	82	139	134	134	193	186	186
32	32	31	86	84	83	140	136	135	194	188	187
33	33	32	87	85	84	141	137	136	195	189	188
34	34	33	88	86	85	142	138	137	196	190	189
35	35	34	89	87	86	143	139	138	197	191	190
36	37	35	90	89	87	144	141	139	198	193	191
37	38	36	91	90	88	145	142	140	199	194	192
38	OVSS(39)	37	92	OVSS(91)	89	146	OVSS(143)	141	200	OVSS(195)	193
39	40	38	93	92	90	147	144	142	201	196	194
40	41	39	94	93	91	148	145	143	202	197	195
41	42	40	95	94	92	149	146	144	203	198	196
42	43	-	96	95	-	150	147	-	204	199	-
43	44	41	97	96	93	151	148	145	205	200	197
44	45	42	98	97	94	152	149	146	206	201	198
45	46	43	99	98	95	153	150	147	207	202	199
46	47	44	100	99	96	154	151	148	208	203	200
47	48	45	101	100	97	155	152	149	209	204	201
48	49	46	102	101	98	156	153	150	210	205	202
49	50	47	103	102	99	157	154	151	211	206	203
50	51	48	104	103	100	158	155	152	212	207	204
51	52	49	105	104	101	159	156	153	213	208	205
52	OVDD3	50	106	OVDD3	102	160	OVDD3	154	214	OVDD3	206
53	OVDD5	51	107	OVDD5	103	161	OVDD5	155	215	OVDD5	207
54	OVSS	52	108	OVSS	104	162	OVSS	156	216	OVSS	208

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die(Array) for probe test.

Rev 1.0 6/18/93 JEB

Table 4-12 H4CP048 225 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
1	VSS	1	a	55	VSS	55	a	109	VSS	109	a	163	VSS	163	a
2	VDD	2	c	56	VDD	56	e	110	VDD	110	d	164	VDD	164	b
3	1	3	A1	57	53	57	R1	111	105	111	R15	165	157	165	A15
4	2	4	B1	58	54	58	R2	112	106	112	P15	166	158	166	A14
5	3	5	C3	59	55	59	N3	113	107	113	N13	167	159	167	C13
6	4	6	C2	60	56	60	P3	114	108	114	N14	168	160	168	B13
7	5	7	C1	61	57	61	R3	115	109	115	N15	169	161	169	A13
8	6	8	D3	62	58	62	N4	116	110	116	M13	170	162	170	C12
9	7	9	D2	63	59	63	P4	117	111	117	M14	171	163	171	B12
10	8	10	D1	64	60	64	R4	118	112	118	M15	172	164	172	A12
11	9	11	E4	65	61	65	M5	119	113	119	L12	173	165	173	D11
12	10	12	E3	66	62	66	N5	120	114	120	L13	174	166	174	C11
13	11	13	E2	67	63	67	P5	121	115	121	L14	175	167	175	B11
14	12	14	E1	68	64	68	R5	122	116	122	L15	176	168	176	A11
15	13	15	F4	69	65	69	M6	123	117	123	K12	177	169	177	D10
16	14	16	F3	70	66	70	N6	124	118	124	K13	178	170	178	C10
17	OVSS(15)	17	a	71	OVSS(67)	71	a	125	OVSS(119)	125	a	179	OVSS(171)	179	a
18	16	18	F2	72	68	72	P6	126	120	126	K14	180	172	180	B10
19	17	19	F1	73	69	73	R6	127	121	127	K15	181	173	181	A10
20	18	20	F5	74	70	74	L6	128	122	128	K11	182	174	182	E10
21	19	21	G4	75	71	75	M7	129	123	129	J12	183	175	183	D9
22	20	22	G2	76	72	76	P7	130	124	130	J14	184	176	184	B9
23	21	23	G1	77	73	77	R7	131	125	131	J15	185	177	185	A9
24	22	24	G3	78	74	78	N7	132	126	132	J13	186	178	186	C9
25	23	25	H4	79	75	79	M8	133	127	133	H12	187	179	187	D8
26	24	26	H3	80	76	80	N8	134	128	134	H13	188	180	188	C8
27	OVDD5(25)	27	c	81	OVDD5(77)	81	e	135	OVDD5(129)	135	d	189	OVDD5(181)	189	b
28	27	28	H1	82	79	82	R8	136	131	136	H15	190	183	190	A8
29	28	29	H2	83	80	83	P8	137	132	137	H14	191	184	191	B8
30	29	30	H5	84	81	84	L8	138	133	138	H11	192	185	192	E8
31	30	31	J3	85	82	85	N9	139	134	139	G13	193	186	193	C7
32	32	32	J1	86	84	86	R9	140	136	140	G15	194	188	194	A7
33	33	33	J2	87	85	87	P9	141	137	141	G14	195	189	195	B7
34	34	34	J4	88	86	88	M9	142	138	142	G12	196	190	196	D7
35	35	35	K5	89	87	89	L10	143	139	143	F11	197	191	197	E6
36	37	36	K1	90	89	90	R10	144	141	144	F15	198	193	198	A6
37	38	37	K2	91	90	91	P10	145	142	145	F14	199	194	199	B6
38	OVSS(39)	38	a	92	OVSS(91)	92	a	146	OVSS(143)	146	a	200	OVSS(195)	200	a
39	40	39	K3	93	92	93	N10	147	144	147	F13	201	196	201	C6
40	41	40	K4	94	93	94	M10	148	145	148	F12	202	197	202	D6
41	42	41	L1	95	94	95	R11	149	146	149	E15	203	198	203	A5
42	43	42	L2	96	95	96	P11	150	147	150	E14	204	199	204	B5
43	44	43	L3	97	96	97	N11	151	148	151	E13	205	200	205	C5
44	45	44	L4	98	97	98	M11	152	149	152	E12	206	201	206	D5
45	46	45	M1	99	98	99	R12	153	150	153	D15	207	202	207	A4
46	47	46	M2	100	99	100	P12	154	151	154	D14	208	203	208	B4
47	48	47	M3	101	100	101	N12	155	152	155	D13	209	204	209	C4
48	49	48	N1	102	101	102	R13	156	153	156	C15	210	205	210	A3
49	50	49	N2	103	102	103	P13	157	154	157	C14	211	206	211	B3
50	51	50	M4	104	103	104	M12	158	155	158	D12	212	207	212	D4
51	52	51	P1	105	104	105	R14	159	156	159	B15	213	208	213	A2

Table 4-12 H4CP048 225 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
52	OVDD3	52	P2	106	OVDD3	106	P14	160	OVDD3	160	B14	214	OVDD3	214	B2
53	OVDD5	53	e	107	OVDD5	107	d	161	OVDD5	161	b	215	OVDD5	215	c
54	OVSS	54	a	108	OVSS	108	a	162	OVSS	162	a	216	OVSS	216	a

Notes:

1. Die Pad/IO-Cell numbers start at top of LEFT side and increment counter-clockwise.
2. Pkg Pin and Bond Finger numbers start at top of left side and increment counter-clockwise.
3. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die(Array) for probe test.
4. OVSS & OVDD5 in () are power and ground for Final Test and are Package dependent.
5. The following is a cross reference of package dependent Power and Ground Pkg Pin numbers:
GND: a =K7, K8, K9, J6, J7, J8, J9, J10, H6, H7, H8, H9, H10, G6, G7, G8, G9, G10, F7, F8, F9
PWR: b = G11, F10, E9, E11, c = G5, F6, E5, E7, d = L5, L7, K6, J5, e = L9, L11, K10, J11
6. Both OVDD5 and VDD are connected together through the package PWR pins.
7. The 225 OMPAC package is limited to the following three combinations of mixed (Core/System) power combinations:
5 V / 5 V, 5 V / 3 V & 5 V, and 3 V / 3 V.

Rev. 1.0 6/18/93 JEB
Rev. 1.1 5/11/94 added note 6.

Table 4-13 H4CP048P1
Analog PLL Option 1

BOTTOM SIDE	
DIE PAD	I/O CELL
55	VSS
56	VDD
57	AVSS
58	AVDD
59	53
60	54
61	55
62	56
63	57
64	58
65	59
66	60
67	61
68	62
69	64
70	65
71	OVSS(66)
72	67
73	68
74	70
75	71
76	72
77	73
78	74
79	75
80	76
81	OVDD5(77)
82	79
83	80
84	81
85	82
86	84
87	85
88	86
89	87
90	89
91	90
92	OVSS(91)
93	92
94	93
95	94
96	95
97	96
98	97
99	98
100	99
101	100
102	101
103	102
104	103
105	104
106	OVDD3
107	OVDD5
108	OVSS

Note: This table replaces the BOTTOM side of each pad to pin table for each array/package combination when Analog PLL option 1 is used in the H4CP048 array.

Table 4-14 H4CP048P2
Analog PLL Option 2

BOTTOM SIDE		TOP SIDE	
Die Pad	I/O Cell	Die Pad	I/O Cell
55	VSS	163	VSS
56	VDD	164	VDD
57	AVSS	165	AVSS
58	AVDD	166	AVDD
59	53	167	157
60	54	168	158
61	55	169	159
62	56	170	160
63	57	171	161
64	58	172	162
65	59	173	163
66	60	174	164
67	61	175	165
68	62	176	166
69	64	177	168
70	65	178	169
71	OVSS(66)	179	OVSS(170)
72	67	180	171
73	68	181	172
74	70	182	174
75	71	183	175
76	72	184	176
77	73	185	177
78	74	186	178
79	75	187	179
80	76	188	180
81	OVDD5(77)	189	OVDD5(181)
82	79	190	183
83	80	191	184
84	81	192	185
85	82	193	186
86	84	194	188
87	85	195	189
88	86	196	190
89	87	197	191
90	89	198	193
91	90	199	194
92	OVSS(91)	200	OVSS(195)
93	92	201	196
94	93	202	197
95	94	203	198
96	95	204	199
97	96	205	200
98	97	206	201
99	98	207	202
100	99	208	203
101	100	209	204
102	101	210	205
103	102	211	206
104	103	212	207
105	104	213	208
106	OVDD3	214	OVDD3
107	OVDD5	215	OVDD5
108	OVSS	216	OVSS

Note: This table replaces the BOTTOM and the TOP side of each pad to pin table for each array/package combination when Analog PLL option 2 is used in the H4CP048 array.

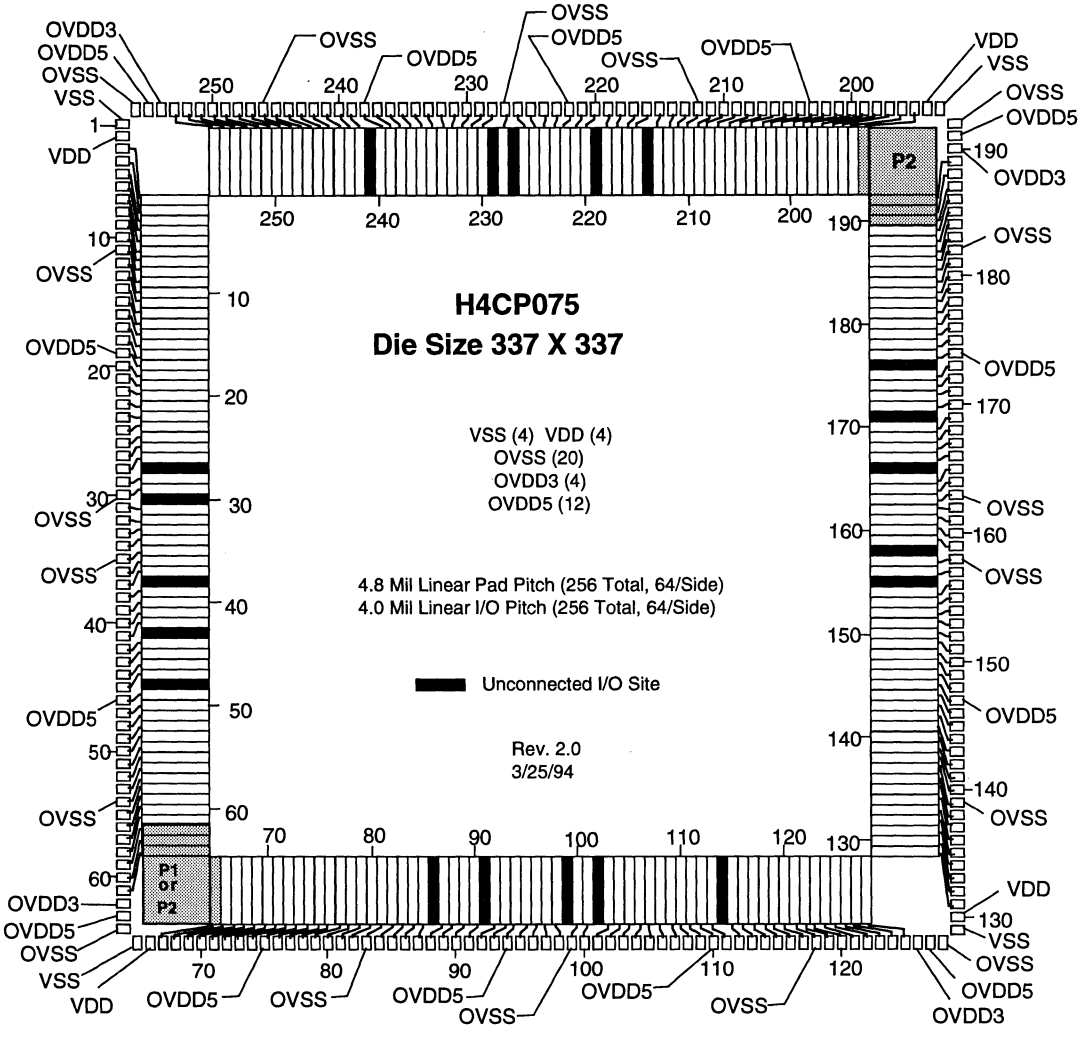

Figure 4-3 H4CP075 Footprint

Note:
P1 = Analog PLL option 1 (H4CP075P1) bottom left corner only,
see Table 4-20 for I/O to pad configuration.
P2 = Analog PLL option 2 (H4CP075P2) bottom left and top right corners,
see Table 4-21 for I/O to pad configuration.

Table 4-15 H4CP075 128 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	65	VSS	-	129	VSS	-	193	VSS	-
2	VDD	-	66	VDD	-	130	VDD	-	194	VDD	-
3	1	1	67	65	33	131	129	65	195	193	97
4	2	2	68	66	34	132	130	66	196	194	98
5	3	3	69	67	35	133	131	67	197	195	99
6	4	4	70	68	36	134	132	68	198	196	100
7	5	5	71	69	37	135	133	69	199	197	101
8	6	6	72	70	38	136	134	70	200	198	102
9	7	7	73	71	39	137	135	71	201	199	103
10	8	-	74	72	-	138	136	-	202	200	-
11	OVSS(9)	-	75	OVDD5(73)	-	139	OVSS(137)	-	203	OVDD5(201)	-
12	10	-	76	74	-	140	138	-	204	202	-
13	11	-	77	75	-	141	139	-	205	203	-
14	12	8	78	76	40	142	140	72	206	204	104
15	13	9	79	77	41	143	141	73	207	205	105
16	14	10	80	78	42	144	142	74	208	206	106
17	15	-	81	79	-	145	143	-	209	207	-
18	16	-	82	80	-	146	144	-	210	208	-
19	OVDD5(17)	-	83	OVSS(81)	-	147	OVDD5(145)	-	211	OVSS(209)	-
20	18	11	84	82	43	148	146	75	212	210	107
21	19	12	85	83	44	149	147	76	213	211	108
22	20	-	86	84	-	150	148	-	214	212	-
23	21	-	87	85	-	151	149	-	215	213	-
24	22	-	88	87	-	152	150	-	216	215	-
25	23	13	89	88	45	153	151	77	217	216	109
26	24	14	90	89	46	154	152	78	218	217	110
27	25	15	91	90	47	155	153	79	219	218	111
28	26	-	92	92	-	156	154	-	220	220	-
29	28	-	93	93	-	157	156	-	221	221	-
30	OVSS(29)	-	94	OVDD5(94)	-	158	OVSS(157)	-	222	OVDD5(222)	-
31	31	-	95	95	-	159	159	-	223	223	-
32	32	16	96	96	48	160	160	80	224	224	112
33	33	17	97	97	49	161	161	81	225	225	113
34	34	-	98	98	-	162	162	-	226	226	-
35	OVSS(35)	-	99	OVSS(100)	-	163	OVSS(163)	-	227	OVSS(228)	-
36	36	-	100	101	-	164	164	-	228	229	-
37	37	-	101	103	-	165	165	-	229	231	-
38	39	18	102	104	50	166	167	82	230	232	114
39	40	19	103	105	51	167	168	83	231	233	115
40	41	20	104	106	52	168	169	84	232	234	116
41	42	-	105	107	-	169	170	-	233	235	-
42	44	-	106	108	-	170	172	-	234	236	-
43	45	-	107	109	-	171	173	-	235	237	-
44	46	21	108	110	53	172	174	85	236	238	117
45	47	22	109	111	54	173	175	86	237	239	118
46	OVDD5(49)	-	110	OVDD5(112)	-	174	OVDD5(177)	-	238	OVDD5(240)	-
47	50	-	111	113	-	175	178	-	239	241	-
48	51	-	112	115	-	176	179	-	240	243	-
49	52	23	113	116	55	177	180	87	241	244	119
50	53	24	114	117	56	178	181	88	242	245	120
51	54	25	115	118	57	179	182	89	243	246	121
52	55	-	116	119	-	180	183	-	244	247	-
53	56	-	117	120	-	181	184	-	245	248	-
54	OVSS(57)	-	118	OVSS(121)	-	182	OVSS(185)	-	246	OVSS(249)	-
55	58	26	119	122	58	183	186	90	247	250	122
56	59	27	120	123	59	184	187	91	248	251	123

Table 4-15 H4CP075 128 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
57	60	28	121	124	60	185	188	92	249	252	124
58	61	29	122	125	61	186	189	93	250	253	125
59	62	30	123	126	62	187	190	94	251	254	126
60	63	31	124	127	63	188	191	95	252	255	127
61	64	32	125	128	64	189	192	96	253	256	128
62	OVDD3	-	126	OVDD3	-	190	OVDD3	-	254	OVDD3	-
63	OVDD5	-	127	OVDD5	-	191	OVDD5	-	255	OVDD5	-
64	OVSS	-	128	OVSS	-	192	OVSS	-	256	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die(Array) for probe test.
Rev 1.0 11/29/93 JEB

Table 4-16 H4CP075 160 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	65	VSS	-	129	VSS	-	193	VSS	-
2	VDD	-	66	VDD	-	130	VDD	-	194	VDD	-
3	1	1	67	65	41	131	129	81	195	193	121
4	2	2	68	66	42	132	130	82	196	194	122
5	3	3	69	67	43	133	131	83	197	195	123
6	4	4	70	68	44	134	132	84	198	196	124
7	5	5	71	69	45	135	133	85	199	197	125
8	6	6	72	70	46	136	134	86	200	198	126
9	7	-	73	71	-	137	135	-	201	199	-
10	8	-	74	72	-	138	136	-	202	200	-
11	OVSS(9)	-	75	OVDD5(73)	-	139	OVSS(137)	-	203	OVDD5(201)	-
12	10	7	76	74	47	140	138	87	204	202	127
13	11	8	77	75	48	141	139	88	205	203	128
14	12	9	78	76	49	142	140	89	206	204	129
15	13	-	79	77	-	143	141	-	207	205	-
16	14	10	80	78	50	144	142	90	208	206	130
17	15	11	81	79	51	145	143	91	209	207	131
18	16	-	82	80	-	146	144	-	210	208	-
19	OVDD5(17)	-	83	OVSS(81)	-	147	OVDD5(145)	-	211	OVSS(209)	-
20	18	12	84	82	52	148	146	92	212	210	132
21	19	13	85	83	53	149	147	93	213	211	133
22	20	14	86	84	54	150	148	94	214	212	134
23	21	-	87	85	-	151	149	-	215	213	-
24	22	15	88	87	55	152	150	95	216	215	135
25	23	16	89	88	56	153	151	96	217	216	136
26	24	-	90	89	-	154	152	-	218	217	-
27	25	17	91	90	57	155	153	97	219	218	137
28	26	18	92	92	58	156	154	98	220	220	138
29	28	19	93	93	59	157	156	99	221	221	139
30	OVSS(29)	-	94	OVDD5(94)	-	158	OVSS(157)	-	222	OVDD5(222)	-
31	31	-	95	95	-	159	159	-	223	223	-
32	32	20	96	96	60	160	160	100	224	224	140
33	33	21	97	97	61	161	161	101	225	225	141
34	34	-	98	98	-	162	162	-	226	226	-
35	OVSS(35)	-	99	OVSS(100)	-	163	OVSS(163)	-	227	OVSS(228)	-
36	36	22	100	101	62	164	164	102	228	229	142
37	37	23	101	103	63	165	165	103	229	231	143
38	39	24	102	104	64	166	167	104	230	232	144
39	40	-	103	105	-	167	168	-	231	233	-
40	41	25	104	106	65	168	169	105	232	234	145
41	42	26	105	107	66	169	170	106	233	235	146
42	44	-	106	108	-	170	172	-	234	236	-
43	45	27	107	109	67	171	173	107	235	237	147
44	46	28	108	110	68	172	174	108	236	238	148
45	47	29	109	111	69	173	175	109	237	239	149
46	OVDD5(49)	-	110	OVDD5(112)	-	174	OVDD5(177)	-	238	OVDD5(240)	-
47	50	30	111	113	70	175	178	110	239	241	150
48	51	31	112	115	71	176	179	111	240	243	151
49	52	32	113	116	72	177	180	112	241	244	152
50	53	-	114	117	-	178	181	-	242	245	-
51	54	33	115	118	73	179	182	113	243	246	153
52	55	34	116	119	74	180	183	114	244	247	154
53	56	35	117	120	75	181	184	115	245	248	155
54	OVSS(57)	-	118	OVSS(121)	-	182	OVSS(185)	-	246	OVSS(249)	-
55	58	-	119	122	-	183	186	-	247	250	-
56	59	-	120	123	-	184	187	-	248	251	-

Table 4-16 H4CP075 160 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
57	60	36	121	124	76	185	188	116	249	252	156
58	61	37	122	125	77	186	189	117	250	253	157
59	62	38	123	126	78	187	190	118	251	254	158
60	63	39	124	127	79	188	191	119	252	255	159
61	64	40	125	128	80	189	192	120	253	256	160
62	OVDD3	-	126	OVDD3	-	190	OVDD3	-	254	OVDD3	-
63	OVDD5	-	127	OVDD5	-	191	OVDD5	-	255	OVDD5	-
64	OVSS	-	128	OVSS	-	192	OVSS	-	256	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die(Array) for probe test.

Rev 1.0 6/18/93 JEB

Table 4-17 H4CP075 169 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
1	VSS	1	a	65	VSS	48	a	129	VSS	96	a	193	VSS	143	a
2	VDD	-	-	66	VDD	-	-	130	VDD	-	-	194	VDD	-	-
3	1	2	A1	67	65	49	N2	131	129	97	N13	195	193	144	A12
4	2	3	B1	68	66	50	K3	132	130	98	M13	196	194	145	D11
5	3	4	B2	69	67	51	L3	133	131	99	M12	197	195	146	C11
6	4	5	C2	70	68	52	M3	134	132	100	L12	198	196	147	B11
7	5	6	C1	71	69	53	N3	135	133	101	L13	199	197	148	A11
8	(OVDD5)6	7	b	72	(OVDD5)70	54	c	136	(OVDD5)134	102	d	200	(OVDD5)198	149	e
9	7	8	E4	73	71	55	L4	137	135	103	J10	201	199	150	C10
10	8	9	D3	74	72	56	L5	138	136	104	K11	202	200	151	C9
11	OVSS(9)	-	-	75	OVDD5(73)	-	-	139	OVSS(137)	-	-	203	OVDD5(201)	-	-
12	10	10	D2	76	74	57	M4	140	138	105	K12	204	202	152	B10
13	11	-	-	77	75	-	-	141	139	-	-	205	203	-	-
14	12	11	D1	78	76	58	N4	142	140	106	K13	206	204	153	A10
15	13	12	E3	79	77	59	K5	143	141	107	J11	207	205	154	D9
16	14	-	-	80	78	-	-	144	142	-	-	208	206	-	-
17	15	13	E2	81	79	60	M5	145	143	108	J12	209	207	155	B9
18	16	14	E1	82	80	61	N5	146	144	109	J13	210	208	156	A9
19	OVDD5(17)	-	-	83	OVSS(81)	-	-	147	OVDD5(145)	-	-	211	OVSS(209)	-	-
20	(OVDD5)18	15	b	84	(OVDD5)82	62	c	148	(OVDD5)146	110	d	212	(OVDD5)210	157	e
21	(OVSS)19	16	a	85	(OVSS)83	63	a	149	(OVSS)147	111	a	213	(OVSS)211	158	a
22	20	17	F3	86	84	64	L6	150	148	112	H11	214	212	159	C8
23	21	18	F4	87	85	65	K6	151	149	113	H10	215	213	160	D8
24	22	-	-	88	87	-	-	152	150	-	-	216	215	-	-
25	23	19	F2	89	88	66	M6	153	151	114	H12	217	216	161	B8
26	24	20	F1	90	89	67	N6	154	152	115	H13	218	217	162	A8
27	25	-	-	91	90	-	-	155	153	-	-	219	218	-	-
28	26	21	F5	92	92	68	J6	156	154	116	H9	220	220	163	E8
29	28	22	G4	93	93	69	K7	157	156	117	G10	221	221	164	D7
30	OVSS(29)	-	-	94	OVDD5(94)	-	-	158	OVSS(157)	-	-	222	OVDD5(222)	-	-
31	31	23	G3	95	95	70	L7	159	159	118	G11	223	223	165	C7
32	32	24	G1	96	96	71	N7	160	160	119	G13	224	224	166	A7
33	33	-	-	97	97	72	M7	161	161	-	-	225	225	167	B7
34	34	25	G2	98	98	73	J7	162	162	120	G12	226	226	168	E7
35	OVSS(35)	26	a	99	OVSS(100)	74	a	163	OVSS(163)	121	a	227	OVSS(228)	169	a
36	36	27	G5	100	101	75	J8	164	164	122	G9	228	229	170	E6
37	37	-	-	101	103	-	-	165	165	-	-	229	231	-	-
38	39	28	H1	102	104	76	N8	166	167	123	F13	230	232	171	A6
39	40	29	H5	103	105	77	K8	167	168	124	F9	231	233	172	D6
40	41	-	-	104	106	-	-	168	169	-	-	232	234	-	-
41	42	30	H4	105	107	78	M8	169	170	125	F10	233	235	173	B6
42	44	31	H2	106	108	79	L8	170	172	126	F12	234	236	174	C6
43	45	-	-	107	109	-	-	171	173	-	-	235	237	-	-
44	46	32	J1	108	110	80	N9	172	174	127	E13	236	238	175	A5
45	(OVSS)47	33	a	109	(OVSS)111	81	a	173	(OVSS)175	128	a	237	(OVSS)239	176	a
46	OVDD5(49)	34	c	110	OVDD5(112)	82	d	174	OVDD5(177)	129	e	238	OVDD5(240)	177	b
47	50	35	H3	111	113	83	M9	175	178	130	F11	239	241	178	B5
48	51	-	-	112	115	-	-	176	179	-	-	240	243	-	-
49	52	36	J2	113	116	84	K9	177	180	131	E12	241	244	179	D5
50	53	37	K1	114	117	85	N10	178	181	132	D13	242	245	180	A4
51	54	38	J3	115	118	86	M10	179	182	133	E11	243	246	181	B4
52	55	-	-	116	119	-	-	180	183	-	-	244	247	-	-

Table 4-17 H4CP075 169 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
53	56	39	K2	117	120	87	L9	181	184	134	D12	245	248	182	C5
54	OVSS(57)	-	-	118	OVSS(121)	-	-	182	OVSS(185)	-	-	246	OVSS(249)	-	-
55	58	40	J4	119	122	88	L10	183	186	135	E10	247	250	183	C4
56	(OVDD5)59	41	c	120	(OVDD5)123	89	d	184	(OVDD5)187	136	e	248	(OVDD5)251	184	b
57	60	42	L1	121	124	90	N11	185	188	137	C13	249	252	185	A3
58	61	43	L2	122	125	91	M11	186	189	138	C12	250	253	186	B3
59	62	44	M2	123	126	92	K10	187	190	139	B12	251	254	187	D4
60	63	45	M1	124	127	93	L11	188	191	140	B13	252	255	188	C3
61	64	46	N1	125	128	94	N12	189	192	141	A13	253	256	189	A2
62	OVDD3	-	-	126	OVDD3	-	-	190	OVDD3	-	-	254	OVDD3	-	-
63	OVDD5	-	-	127	OVDD5	-	-	191	OVDD5	-	-	255	OVDD5	-	-
64	OVSS	47	a	128	OVSS	95	a	192	OVSS	142	a	256	OVSS	190	a

Notes:
1. Die Pad/IO-Cell numbers start at top of LEFT side and increment counter-clockwise.
2. Pkg Pin and Bond FInger numbers start at top of LEFT side and increment counter-clockwise.
3. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die (Array) for probe test.
4. OVSS & OVDD5 in () are power and ground for Final Test and are Package dependent
5. The following is a cross reference of package dependent Power and Ground Pkg Pin numbers:
GND: a =F6, F7, F8, G6, G7, G8, H6, H7, H8
PWR: b = E5, c = J5, K4, d = J9, e =D10, E9
6. Only OVDD5 is connected to package PWR pins.
7.VDD must be supplied separately through I/O package pins for all applications.

Rev. 1.0 6/18/93 JEB
Rev. 1.1 5/11/94 JEB added note 6.

Table 4-18 H4CP075 208 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	65	VSS	-	129	VSS	-	193	VSS	-
2	VDD	-	66	VDD	-	130	VDD	-	194	VDD	-
3	1	1	67	65	53	131	129	105	195	193	157
4	2	2	68	66	54	132	130	106	196	194	158
5	3	3	69	67	55	133	131	107	197	195	159
6	4	4	70	68	56	134	132	108	198	196	160
7	5	5	71	69	57	135	133	109	199	197	161
8	6	6	72	70	58	136	134	110	200	198	162
9	7	7	73	71	59	137	135	111	201	199	163
10	8	8	74	72	60	138	136	112	202	200	164
11	OVSS(9)	-	75	OVDD5(73)	-	139	OVSS(137)	-	203	OVDD5(201)	-
12	10	9	76	74	61	140	138	113	204	202	165
13	11	10	77	75	62	141	139	114	205	203	166
14	12	11	78	76	63	142	140	115	206	204	167
15	13	12	79	77	64	143	141	116	207	205	168
16	14	13	80	78	65	144	142	117	208	206	169
17	15	14	81	79	66	145	143	118	209	207	170
18	16	15	82	80	67	146	144	119	210	208	171
19	OVDD5(17)	-	83	OVSS(81)	-	147	OVDD5(145)	-	211	OVSS(209)	-
20	18	16	84	82	68	148	146	120	212	210	172
21	19	17	85	83	69	149	147	121	213	211	173
22	20	18	86	84	70	150	148	122	214	212	174
23	21	19	87	85	71	151	149	123	215	213	175
24	22	20	88	87	72	152	150	124	216	215	176
25	23	21	89	88	73	153	151	125	217	216	177
26	24	22	90	89	74	154	152	126	218	217	178
27	25	23	91	90	75	155	153	127	219	218	179
28	26	24	92	92	76	156	154	128	220	220	180
29	28	25	93	93	77	157	156	129	221	221	181
30	OVSS(29)	-	94	OVDD5(94)	-	158	OVSS(157)	-	222	OVDD5(222)	-
31	31	-	95	95	-	159	159	-	223	223	-
32	32	26	96	96	78	160	160	130	224	224	182
33	33	27	97	97	79	161	161	131	225	225	183
34	34	28	98	98	80	162	162	132	226	226	184
35	OVSS(35)	-	99	OVSS(100)	-	163	OVSS(163)	-	227	OVSS(228)	-
36	36	29	100	101	81	164	164	133	228	229	185
37	37	30	101	103	82	165	165	134	229	231	186
38	39	31	102	104	83	166	167	135	230	232	187
39	40	32	103	105	84	167	168	136	231	233	188
40	41	33	104	106	85	168	169	137	232	234	189
41	42	34	105	107	86	169	170	138	233	235	190
42	44	35	106	108	87	170	172	139	234	236	191
43	45	36	107	109	88	171	173	140	235	237	192
44	46	37	108	110	89	172	174	141	236	238	193
45	47	38	109	111	90	173	175	142	237	239	194
46	OVDD5(49)	-	110	OVDD5(112)	-	174	OVDD5(177)	-	238	OVDD5(240)	-
47	50	39	111	113	91	175	178	143	239	241	195
48	51	40	112	115	92	176	179	144	240	243	196
49	52	41	113	116	93	177	180	145	241	244	197
50	53	42	114	117	94	178	181	146	242	245	198
51	54	43	115	118	95	179	182	147	243	246	199
52	55	44	116	119	96	180	183	148	244	247	200
53	56	45	117	120	97	181	184	149	245	248	201
54	OVSS(57)	-	118	OVSS(121)	-	182	OVSS(185)	-	246	OVSS(249)	-
55	58	46	119	122	98	183	186	150	247	250	202
56	59	47	120	123	99	184	187	151	248	251	203
57	60	48	121	124	100	185	188	152	249	252	204
58	61	49	122	125	101	186	189	153	250	253	205
59	62	50	123	126	102	187	190	154	251	254	206
60	63	51	124	127	103	188	191	155	252	255	207
61	64	52	125	128	104	189	192	156	253	256	208

Table 4-18 H4CP075 208 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
62	OVDD3	-	126	OVDD3	-	190	OVDD3	-	254	OVDD3	-
63	OVDD5	-	127	OVDD5	-	191	OVDD5	-	255	OVDD5	-
64	OVSS	-	128	OVSS	-	192	OVSS	-	256	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die (Array) for probe test.

Rev 1.0 6/18/93 JEB

Table 4-19 H4CP075 225 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
1	VSS	1	b	65	VSS	65	b	129	VSS	129	b	193	VSS	193	b
2	VDD	2	c	66	VDD	66	d	130	VDD	130	e	194	VDD	194	a
3	1	3	D4	67	65	67	M4	131	129	131	M12	195	193	195	D12
4	2	4	B1	68	66	68	R2	132	130	132	P15	196	194	196	B13
5	3	5	C2	69	67	69	P3	133	131	133	N14	197	195	197	A14
6	4	6	E5	70	68	70	L5	134	132	134	L11	198	196	198	E11
7	5	7	D3	71	69	71	N4	135	133	135	M13	199	197	199	C12
8	6	8	C1	72	70	72	R3	136	134	136	N15	200	198	200	A13
9	7	9	D2	73	71	73	P4	137	135	137	M14	201	199	201	B12
10	8	10	E4	74	72	74	M5	138	136	138	L12	202	200	202	D11
11	OVSS(9)	11	b	75	OVDD5(73)	75	d	139	OVSS(137)	139	b	203	OVDD5(201)	203	a
12	10	12	D1	76	74	76	R4	140	138	140	M15	204	202	204	A12
13	11	13	E3	77	75	77	N5	141	139	141	L13	205	203	205	C11
14	12	14	E2	78	76	78	P5	142	140	142	L14	206	204	206	B11
15	13	15	F5	79	77	79	L6	143	141	143	K11	207	205	207	E10
16	14	16	E1	80	78	80	R5	144	142	144	L15	208	206	208	A11
17	15	17	F4	81	79	81	M6	145	143	145	K12	209	207	209	D10
18	16	18	F3	82	80	82	N6	146	144	146	K13	210	208	210	C10
19	OVDD5(17)	19	c	83	OVSS(81)	83	d	147	OVDD5(145)	147	e	211	OVSS(209)	211	b
20	(OVSS)18	20	b	84	(OVDD5)82	84	a	148	(OVSS)146	148	b	212	(OVDD5)210	212	a
21	19	21	F2	85	83	85	P6	149	147	149	K14	213	211	213	B10
22	20	22	F1	86	84	86	R6	150	148	150	K15	214	212	214	A10
23	21	23	G4	87	85	87	M7	151	149	151	J12	215	213	215	D9
24	22	24	G3	88	87	88	N7	152	150	152	J13	216	215	216	C9
25	23	25	G2	89	88	89	P7	153	151	153	J14	217	216	217	B9
26	24	26	G1	90	89	90	R7	154	152	154	J15	218	217	218	A9
27	25	27	G5	91	90	91	L7	155	153	155	J11	219	218	219	E9
28	26	28	H3	92	92	92	N8	156	154	156	H13	220	220	220	C8
29	28	29	H2	93	(VDD)93	93	d	157	156	157	H14	221	(VDD)221	221	a
30	OVSS(29)	30	b	94	OVDD5(94)	94	d	158	OVSS(157)	158	b	222	OVDD5(222)	222	a
31	31	31	H1	95	95	95	P8	159	159	159	H15	223	223	223	B8
32	(OVDD5)32	32	c	96	(OVSS)96	96	b	160	(OVDD5)160	160	e	224	(OVSS)224	224	b
33	(VDD)33	33	c	97	97	97	R8	161	(VDD)161	161	e	225	225	225	A8
34	34	34	H4	98	98	98	M8	162	162	162	H12	226	226	226	D8
35	OVSS(35)	35	b	99	OVSS(100)	99	b	163	OVSS(163)	163	b	227	OVSS(228)	227	b
36	36	36	H5	100	101	100	L8	164	164	164	H11	228	229	228	E8
37	37	37	J2	101	103	101	P9	165	165	165	G14	229	231	229	B7
38	39	38	J1	102	104	102	R9	166	167	166	G15	230	232	230	A7
39	40	39	J3	103	105	103	N9	167	168	167	G13	231	233	231	C7
40	41	40	J4	104	106	104	M9	168	169	168	G12	232	234	232	D7
41	42	41	J5	105	107	105	L9	169	170	169	G11	233	235	233	E7
42	44	42	K1	106	108	106	R10	170	172	170	F15	234	236	234	A6
43	45	43	K2	107	109	107	P10	171	173	171	F14	235	237	235	B6
44	46	44	K3	108	110	108	N10	172	174	172	F13	236	238	236	C6
45	(VSS)47	45	b	109	(VSS)111	109	b	173	(VSS)175	173	b	237	(VSS)239	237	b
46	OVDD5(49)	46	d	110	OVDD5(112)	110	e	174	OVDD5(177)	174	a	238	OVDD5(240)	238	c
47	50	47	L1	111	113	111	R11	175	178	175	E15	239	241	239	A5
48	51	48	L2	112	115	112	P11	176	179	176	E14	240	243	240	B5
49	52	49	K4	113	116	113	M10	177	180	177	F12	241	244	241	D6
50	53	50	L3	114	117	114	N11	178	181	178	E13	242	245	242	C5
51	54	51	M1	115	118	115	R12	179	182	179	D15	243	246	243	A4
52	55	52	K5	116	119	116	L10	180	183	180	F11	244	247	244	E6

Table 4-19 H4CP075 225 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
53	56	53	M2	117	120	117	P12	181	184	181	D14	245	248	245	B4
54	OVSS(57)	54	b	118	OVSS(121)	118	b	182	OVSS(185)	182	b	246	OVSS(249)	246	b
55	58	55	L4	119	122	119	M11	183	186	183	E12	247	250	247	D5
56	59	56	N1	120	123	120	R13	184	187	184	C15	248	251	248	A3
57	60	57	M3	121	124	121	N12	185	188	185	D13	249	252	249	C4
58	61	58	N2	122	125	122	P13	186	189	186	C14	250	253	250	B3
59	62	59	P1	123	126	123	R14	187	190	187	B15	251	254	251	A2
60	63	60	N3	124	127	124	N13	188	191	188	C13	252	255	252	C3
61	64	61	P2	125	128	125	P14	189	192	189	B14	253	256	253	B2
62	OVDD3	62	R1	126	OVDD3	126	R15	190	OVDD3	190	A15	254	OVDD3	254	A1
63	OVDD5	63	d	127	OVDD5	127	e	191	OVDD5	191	a	255	OVDD5	255	c
64	OVSS	64	b	128	OVSS	128	b	192	OVSS	192	b	256	OVSS	256	b

Notes:

1. Die Pad/IO-Cell numbers start at top of LEFT side and increment counter-clockwise.
2. Pkg Pin and Bond Finger numbers start at top of LEFT side and increment counter-clockwise.
3. VSS, VDD, OVSS, OVDD3, & OVDD5 indicates fixed power and ground pads on the die (Array) for probe test.
4. OVSS & OVDD5 in () are power and ground for Final Test and are Package dependent,
5. The following is a cross reference of package dependent Power and Ground Pkg Pin numbers:
   PWR: a = F9,F10,G10 c=F6, F7, G6 d=J6, K6, K7 e=K9, K10, J10
   GND: b =F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8
6. Both OVDD5 and VDD are connected together through the package PWR pins.
7. OVDD3 must be supplied separately through I/O package pins for mixed voltage (5V / 3.3V) I/O applications.
8. The 225 OMPAC package is limited to the following three combinations of mixed (Core/System) power combinations:
   5 V / 5 V, 5 V / 3 V & 5 V, and 3 V / 3 V.

REV. 1.0 6/18/93 JEB
REV. 1.1 7/12/93 JEB Updated PWR, defined power planes a, c,d and e.
REV. 1.2 5/11/94 JEB Added notes 6 and 7.

Table 4-20 H4CP075P1 Analog PLL Option 1

BOTTOM	
DIE PAD	I/O CELL
65	VSS
66	VDD
67	AVSS
68	AVDD
69	65
70	66
71	67
72	68
73	69
74	70
75	OVDD5(71)
76	72
77	73
78	74
79	76
80	77
81	78
82	79
83	OVSS(81)
84	82
85	83
86	84
87	85
88	87
89	88
90	89
91	90
92	92
93	93
94	OVDD5(94)
95	95
96	96
97	97
98	98
99	OVSS(100)
100	101
101	103
102	104
103	105
104	106
105	107
106	108
107	109
108	110
109	111
110	OVDD5(112)
111	113
112	115
113	116
114	117
115	118
116	119
117	120

Table 4-20 H4CP075P1 Analog PLL Option 1

BOTTOM	
DIE PAD	I/O CELL
118	OVSS(121)
119	122
120	123
121	124
122	125
123	126
124	127
125	128
126	OVDD3
127	OVDD5
128	OVSS

Note: This table replaces the BOTTOM side of each pad to pin table for each array/package combination when Analog PLL option 1 is used in the H4CP075 array.

Table 4-21 H4CP075P2
Analog PLL Option 2

BOTTOM		TOP	
DIE PAD	I/O CELL	DIE PAD	I/O CELL
65	VSS	193	VSS
66	VDD	194	VDD
67	AVSS	195	AVSS
68	AVDD	196	AVDD
69	65	197	193
70	66	198	194
71	67	199	195
72	68	200	196
73	69	201	197
74	70	202	198
75	OVDD5(71)	203	OVDD5(199)
76	72	204	200
77	73	205	201
78	74	206	202
79	76	207	204
80	77	208	205
81	78	209	206
82	79	210	207
83	OVSS(81)	211	OVSS(209)
84	82	212	210
85	83	213	211
86	84	214	212
87	85	215	213
88	87	216	215
89	88	217	216
90	89	218	217
91	90	219	218
92	92	220	220
93	93	221	221
94	OVDD5(94)	222	OVDD5(222)
95	95	223	223
96	96	224	224
97	97	225	225
98	98	226	226
99	OVSS(100)	227	OVSS(228)
100	101	228	229
101	103	229	231
102	104	230	232
103	105	231	233
104	106	232	234
105	107	233	235
106	108	234	236
107	109	235	237
108	110	236	238
109	111	237	239
110	OVDD5(112)	238	OVDD5(240)
111	113	239	241
112	115	240	243
113	116	241	244
114	117	242	245
115	118	243	246
116	119	244	247
117	120	245	248

Table 4-21 H4CP075P2
Analog PLL Option 2

BOTTOM		TOP	
DIE PAD	I/O CELL	DIE PAD	I/O CELL
118	OVSS(121)	246	OVSS(249)
119	122	247	250
120	123	248	251
121	124	249	252
122	125	250	253
123	126	251	254
124	127	252	255
125	128	253	256
126	OVDD3	254	OVDD3
127	OVDD5	255	OVDD5
128	OVSS	256	OVSS

Note: This table replaces the BOTTOM and the TOP side of each pad to pin table for each array/package combination when Analog PLL option 2 is used in the H4CP075 array.

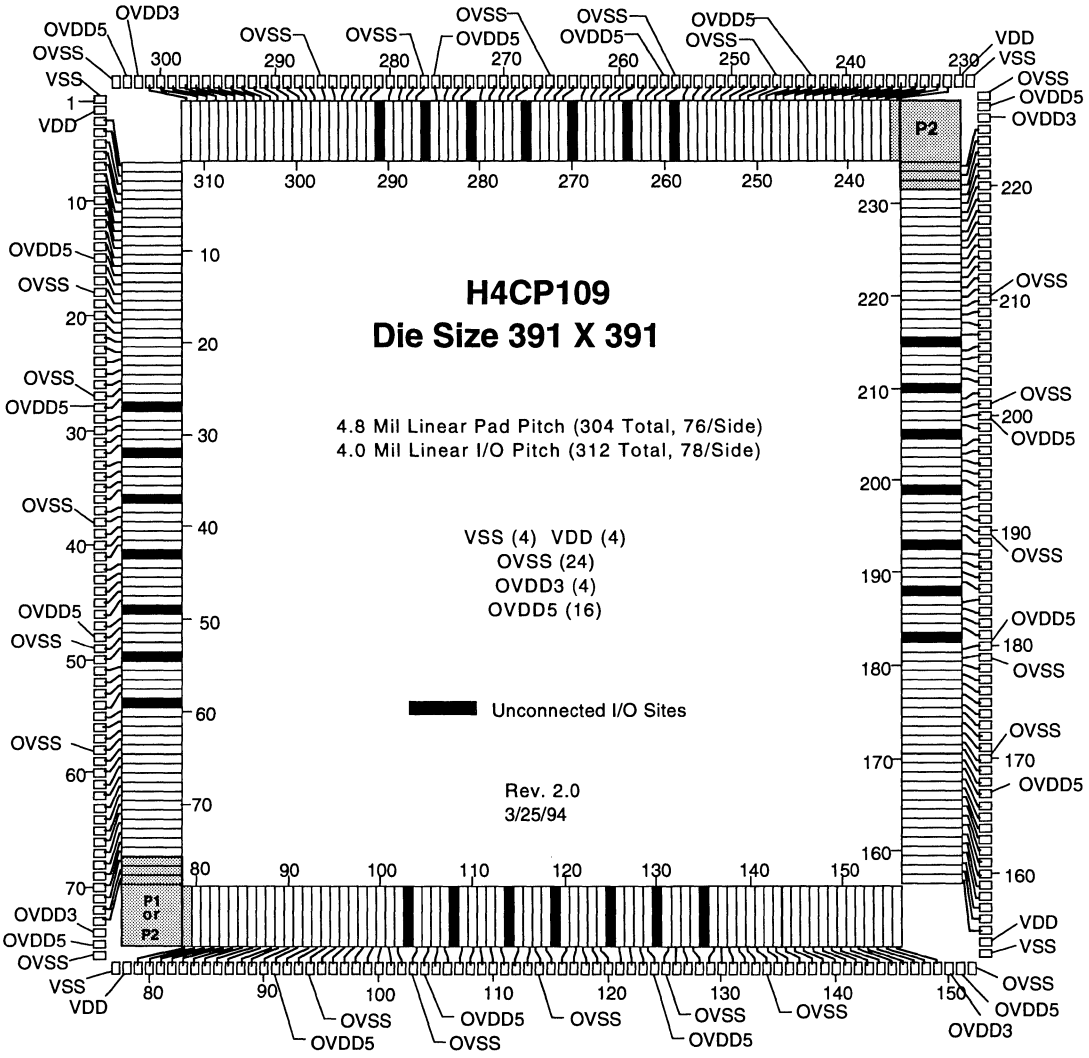

Figure 4-4 H4CP109 Footprint

Note:
P1 = Analog PLL option 1 (H4CP109P1) bottom left corner only,
see Table 4-29 for I/O to pad configuration.
P2 = Analog PLL option 2 (H4CP109P2) bottom left and top right corners,
see Table 4-30 for I/O to pad configuration.

Table 4-22 H4CP109 160 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	77	VSS	-	153	VSS	-	229	VSS	-
2	VDD	-	78	VDD	-	154	VDD	-	230	VDD	-
3	1	1	79	79	41	155	157	81	231	235	121
4	2	2	80	80	42	156	158	82	232	236	122
5	3	3	81	81	43	157	159	83	233	237	123
6	4	4	82	82	44	158	160	84	234	238	124
7	5	5	83	83	45	159	161	85	235	239	125
8	6	6	84	84	46	160	162	86	236	240	126
9	7	-	85	85	-	161	163	-	237	241	-
10	8		86	86		162	164		238	242	
11	9	7	87	87	47	163	165	87	239	243	127
12	10	8	88	88	48	164	166	88	240	244	128
13	11	-	89	89	-	165	167	-	241	245	-
14	12	-	90	90	-	166	168	-	242	246	-
15	OVDD5(13)	-	91	OVDD5(91)	-	167	OVDD5(169)	-	243	OVDD5(247)	-
16	14	9	92	92	49	168	170	89	244	248	129
17	15	10	93	93	50	169	171	90	245	249	130
18	OVSS(16)	-	94	OVSS(94)	-	170	OVSS(172)	-	246	OVSS(250)	-
19	17	-	95	95	-	171	173	-	247	251	-
20	18	11	96	96	51	172	174	91	248	252	131
21	19	12	97	97	52	173	175	92	249	253	132
22	20	-	98	98	-	174	176	-	250	254	-
23	21	-	99	99	-	175	177	-	251	255	-
24	22	13	100	100	53	176	178	93	252	256	133
25	23	14	101	101	54	177	179	94	253	257	134
26	24	15	102	102	55	178	180	95	254	258	135
27	OVSS(25)	-	103	OVSS(104)	-	179	OVSS(181)	-	255	OVSS(260)	-
28	OVDD5(26)	-	104	OVDD5(105)	-	180	OVDD5(182)	-	256	OVDD5(261)	-
29	28	16	105	106	56	181	184	96	257	262	136
30	29	17	106	107	57	182	185	97	258	263	137
31	30	-	107	109	-	183	186	-	259	265	-
32	31	-	108	110	-	184	187	-	260	266	-
33	33	-	109	111	-	185	189	-	261	267	-
34	34	18	110	112	58	186	190	98	262	268	138
35	35	19	111	113	59	187	191	99	263	269	139
36	36	20	112	115	60	188	192	100	264	271	140
37	38	-	113	116	-	189	194	-	265	272	-
38	OVSS(39)	-	114	OVSS(117)	-	190	OVSS(195)	-	266	OVSS(273)	-
39	40	21	115	118	61	191	196	101	267	274	141
40	41	22	116	120	62	192	197	102	268	276	142
41	42	23	117	121	63	193	198	103	269	277	143
42	44	-	118	122	-	194	200	-	270	278	-
43	45	-	119	123	-	195	201	-	271	279	-
44	46	-	120	124	-	196	202	-	272	280	-
45	47	24	121	126	64	197	203	104	273	282	144
46	48	25	122	127	65	198	204	105	274	283	145
47	50	-	123	128	-	199	206	-	275	284	-
48	OVDD5(51)	-	124	OVDD5(129)	-	200	OVDD5(207)	-	276	OVDD5(285)	-
49	OVSS(52)	-	125	OVSS(131)	-	201	OVSS(208)	-	277	OVSS(287)	-
50	53	26	126	132	66	202	209	106	278	288	146
51	55	27	127	133	67	203	211	107	279	289	147
52	56	28	128	134	68	204	212	108	280	290	148
53	57	-	129	136	-	205	213	-	281	292	-
54	58	-	130	137	-	206	214	-	282	293	-
55	60	-	131	138	-	207	216	-	283	294	-

Table 4-22 H4CP109 160 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
56	61	29	132	139	69	208	217	109	284	295	149
57	62	30	133	140	70	209	218	110	285	296	150
58	OVSS(63)	-	134	OVSS(141)	-	210	OVSS(219)	-	286	OVSS(297)	-
59	64	-	135	142	-	211	220	-	287	298	-
60	65	31	136	143	71	212	221	111	288	299	151
61	66	32	137	144	72	213	222	112	289	300	152
62	67	-	138	145	-	214	223	-	290	301	-
63	68		139	146		215	224		291	302	
64	69	33	140	147	73	216	225	113	292	303	153
65	70	34	141	148	74	217	226	114	293	304	154
66	71	-	142	149	-	218	227	-	294	305	-
67	72	-	143	150	-	219	228	-	295	306	-
68	73	35	144	151	75	220	229	115	296	307	155
69	74	36	145	152	76	221	230	116	297	308	156
70	75	37	146	153	77	222	231	117	298	309	157
71	76	38	147	154	78	223	232	118	299	310	158
72	77	39	148	155	79	224	233	119	300	311	159
73	78	40	149	156	80	225	234	120	301	312	160
74	OVDD3	-	150	OVDD3	-	226	OVDD3	-	302	OVDD3	-
75	OVDD5	-	151	OVDD5	-	227	OVDD5	-	303	OVDD5	-
76	OVSS	-	152	OVSS	-	228	OVSS	-	304	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die (Array) for probe test.

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Table 4-23 H4CP109 160 MicroCool Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	77	VSS	-	153	VSS	-	229	VSS	-
2	VDD	-	78	VDD	-	154	VDD	-	230	VDD	-
3	1	40	79	79	160	155	157	120	231	235	80
4	2	39	80	80	159	156	158	119	232	236	79
5	3	38	81	81	158	157	159	118	233	237	78
6	4	37	82	82	157	158	160	117	234	238	77
7	5	36	83	83	156	159	161	116	235	239	76
8	6	35	84	84	155	160	162	115	236	240	75
9	7	-	85	85	-	161	163	-	237	241	-
10	8		86	86		162	164		238	242	
11	9	34	87	87	154	163	165	114	239	243	74
12	10	33	88	88	153	164	166	113	240	244	73
13	11	-	89	89	-	165	167	-	241	245	-
14	12		90	90		166	168		242	246	
15	OVDD5(13)	-	91	OVDD5(91)	-	167	OVDD5(169)	-	243	OVDD5(247)	-
16	14	32	92	92	152	168	170	112	244	248	72
17	15	31	93	93	151	169	171	111	245	249	71
18	OVSS(16)	-	94	OVSS(94)	-	170	OVSS(172)	-	246	OVSS(250)	-
19	17		95	95		171	173		247	251	
20	18	30	96	96	150	172	174	110	248	252	70
21	19	29	97	97	149	173	175	109	249	253	69
22	20		98	98		174	176		250	254	
23	21		99	99		175	177		251	255	
24	22	28	100	100	148	176	178	108	252	256	68
25	23	27	101	101	147	177	179	107	253	257	67
26	24	26	102	102	146	178	180	106	254	258	66
27	OVSS(25)	-	103	OVSS(104)	-	179	OVSS(181)	-	255	OVSS(260)	-
28	OVDD5(26)	-	104	OVDD5(105)	-	180	OVDD5(182)	-	256	OVDD5(261)	-
29	28	25	105	106	145	181	184	105	257	262	65
30	29	24	106	107	144	182	185	104	258	263	64
31	30		107	109		183	186		259	265	
32	31	-	108	110	-	184	187	-	260	266	-
33	33		109	111		185	189		261	267	
34	34	23	110	112	143	186	190	103	262	268	63
35	35	22	111	113	142	187	191	102	263	269	62
36	36	21	112	115	141	188	192	101	264	271	61
37	38		113	116		189	194		265	272	
38	OVSS(39)	-	114	OVSS(117)	-	190	OVSS(195)	-	266	OVSS(273)	-
39	40	20	115	118	140	191	196	100	267	274	60
40	41	19	116	120	139	192	197	99	268	276	59
41	42	18	117	121	138	193	198	98	269	277	58
42	44	-	118	122	-	194	200	-	270	278	-
43	45		119	123		195	201		271	279	
44	46	-	120	124	-	196	202	-	272	280	-
45	47	17	121	126	137	197	203	97	273	282	57
46	48	16	122	127	136	198	204	96	274	283	56
47	50		123	128		199	206		275	284	
48	OVDD5(51)	-	124	OVDD5(129)	-	200	OVDD5(207)	-	276	OVDD5(285)	-
49	OVSS(52)	-	125	OVSS(131)	-	201	OVSS(208)	-	277	OVSS(287)	-
50	53	15	126	132	135	202	209	95	278	288	55
51	55	14	127	133	134	203	211	94	279	289	54
52	56	13	128	134	133	204	212	93	280	290	53
53	57	-	129	136	-	205	213	-	281	292	-
54	58		130	137		206	214		282	293	
55	60	-	131	138	-	207	216	-	283	294	-
56	61	12	132	139	132	208	217	92	284	295	52

Table 4-23 H4CP109 160 MicroCool Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
57	62	11	133	140	131	209	218	91	285	296	51
58	OVSS(63)	-	134	OVSS(141)	-	210	OVSS(219)	-	286	OVSS(297)	-
59	64		135	142		211	220		287	298	
60	65	10	136	143	130	212	221	90	288	299	50
61	66	9	137	144	129	213	222	89	289	300	49
62	67		138	145		214	223		290	301	
63	68		139	146		215	224		291	302	
64	69	8	140	147	128	216	225	88	292	303	48
65	70	7	141	148	127	217	226	87	293	304	47
66	71	-	142	149	-	218	227		294	305	
67	72	-	143	150	-	219	228	-	295	306	-
68	73	6	144	151	126	220	229	86	296	307	46
69	74	5	145	152	125	221	230	85	297	308	45
70	75	4	146	153	124	222	231	84	298	309	44
71	76	3	147	154	123	223	232	83	299	310	43
72	77	2	148	155	122	224	233	82	300	311	42
73	78	1	149	156	121	225	234	81	301	312	41
74	OVDD3	-	150	OVDD3	-	226	OVDD3	-	302	OVDD3	-
75	OVDD5	-	151	OVDD5	-	227	OVDD5	-	303	OVDD5	-
76	OVSS	-	152	OVSS	-	228	OVSS	-	304	OVSS	-

Notes:
1. Die pad/cell numbers start at top of LEFT side and increment counter-clockwise.
2. Package numbers start at bottom of the LEFT side and increment clockwise
3.VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die (Array) for probe test..

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Table 4-24 H4CP109 208 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	77	VSS	-	153	VSS	-	229	VSS	-
2	VDD	-	78	VDD	-	154	VDD	-	230	VDD	-
3	1	1	79	79	53	155	157	105	231	235	157
4	2	2	80	80	54	156	158	106	232	236	158
5	3	3	81	81	55	157	159	107	233	237	159
6	4	4	82	82	56	158	160	108	234	238	160
7	5	5	83	83	57	159	161	109	235	239	161
8	6	6	84	84	58	160	162	110	236	240	162
9	7	7	85	85	59	161	163	111	237	241	163
10	8	8	86	86	60	162	164	112	238	242	164
11	9	9	87	87	61	163	165	113	239	243	165
12	10	10	88	88	62	164	166	114	240	244	166
13	11	11	89	89	63	165	167	115	241	245	167
14	12	12	90	90	64	166	168	116	242	246	168
15	OVDD5(13)	-	91	OVDD5(91)	-	167	OVDD5(169)	-	243	OVDD5(247)	-
16	14	13	92	92	65	168	170	117	244	248	169
17	15	14	93	93	66	169	171	118	245	249	170
18	OVSS(16)	-	94	OVSS(94)	-	170	OVSS(172)	-	246	OVSS(250)	-
19	17	15	95	95	67	171	173	119	247	251	171
20	18	16	96	96	68	172	174	120	248	252	172
21	19	17	97	97	69	173	175	121	249	253	173
22	20	-	98	98	-	174	176	-	250	254	-
23	21	-	99	99	-	175	177	-	251	255	-
24	22	18	100	100	70	176	178	122	252	256	174
25	23	19	101	101	71	177	179	123	253	257	175
26	24	20	102	102	72	178	180	124	254	258	176
27	OVSS(25)	-	103	OVSS(104)	-	179	OVSS(181)	-	255	OVSS(260)	-
28	OVDD5(26)	-	104	OVDD5(105)	-	180	OVDD5(182)	-	256	OVDD5(261)	-
29	28	21	105	106	73	181	184	125	257	262	177
30	29	22	106	107	74	182	185	126	258	263	178
31	30	23	107	109	75	183	186	127	259	265	179
32	31	-	108	110	-	184	187	-	260	266	-
33	33	-	109	111	-	185	189	-	261	267	-
34	34	-	110	112	-	186	190	-	262	268	-
35	35	24	111	113	76	187	191	128	263	269	180
36	36	25	112	115	77	188	192	129	264	271	181
37	38	26	113	116	78	189	194	130	265	272	182
38	OVSS(39)	-	114	OVSS(117)	-	190	OVSS(195)	-	266	OVSS(273)	-
39	40	27	115	118	79	191	196	131	267	274	183
40	41	28	116	120	80	192	197	132	268	276	184
41	42	29	117	121	81	193	198	133	269	277	185
42	44	-	118	122	-	194	200	-	270	278	-
43	45	-	119	123	-	195	201	-	271	279	-
44	46	-	120	124	-	196	202	-	272	280	-
45	47	30	121	126	82	197	203	134	273	282	186
46	48	31	122	127	83	198	204	135	274	283	187
47	50	32	123	128	84	199	206	136	275	284	188
48	OVDD5(51)	-	124	OVDD5(129)	-	200	OVDD5(207)	-	276	OVDD5(285)	-
49	OVSS(52)	-	125	OVSS(131)	-	201	OVSS(208)	-	277	OVSS(287)	-
50	53	33	126	132	85	202	209	137	278	288	189
51	55	34	127	133	86	203	211	138	279	289	190
52	56	35	128	134	87	204	212	139	280	290	191
53	57	-	129	136	-	205	213	-	281	292	-
54	58	-	130	137	-	206	214	-	282	293	-
55	60	36	131	138	88	207	216	140	283	294	192
56	61	37	132	139	89	208	217	141	284	295	193
57	62	38	133	140	90	209	218	142	285	296	194
58	OVSS(63)	-	134	OVSS(141)	-	210	OVSS(219)	-	286	OVSS(297)	-
59	64	39	135	142	91	211	220	143	287	298	195
60	65	40	136	143	92	212	221	144	288	299	196
61	66	-	137	144	-	213	222	-	289	300	-
62	67	41	138	145	93	214	223	145	290	301	197

Table 4-24 H4CP109 208 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
63	68	42	139	146	94	215	224	146	291	302	198
64	69	43	140	147	95	216	225	147	292	303	199
65	70	44	141	148	96	217	226	148	293	304	200
66	71	45	142	149	97	218	227	149	294	305	201
67	72	46	143	150	98	219	228	150	295	306	202
68	73	47	144	151	99	220	229	151	296	307	203
69	74	48	145	152	100	221	230	152	297	308	204
70	75	49	146	153	101	222	231	153	298	309	205
71	76	50	147	154	102	223	232	154	299	310	206
72	77	51	148	155	103	224	233	155	300	311	207
73	78	52	149	156	104	225	234	156	301	312	208
74	OVDD3	-	150	OVDD3	-	226	OVDD3	-	302	OVDD3	-
75	OVDD5	-	151	OVDD5	-	227	OVDD5	-	303	OVDD5	-
76	OVSS	-	152	OVSS	-	228	OVSS	-	304	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die (Array) for probe test.

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Table 4-25 H4CP109 208 MicroCool Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	77	VSS	-	153	VSS	-	229	VSS	-
2	VDD	-	78	VDD	-	154	VDD	-	230	VDD	-
3	1	52	79	79	208	155	157	156	231	235	104
4	2	51	80	80	207	156	158	155	232	236	103
5	3	50	81	81	206	157	159	154	233	237	102
6	4	49	82	82	205	158	160	153	234	238	101
7	5	48	83	83	204	159	161	152	235	239	100
8	6	47	84	84	203	160	162	151	236	240	99
9	7	46	85	85	202	161	163	150	237	241	98
10	8	45	86	86	201	162	164	149	238	242	97
11	9	44	87	87	200	163	165	148	239	243	96
12	10	43	88	88	199	164	166	147	240	244	95
13	11	42	89	89	198	165	167	146	241	245	94
14	12	41	90	90	197	166	168	145	242	246	93
15	OVDD5(13)	-	91	OVDD5(91)	-	167	OVDD5(169)	-	243	OVDD5(247)	-
16	14	40	92	92	196	168	170	144	244	248	92
17	15	39	93	93	195	169	171	143	245	249	91
18	OVSS(16)	-	94	OVSS(94)	-	170	OVSS(172)	-	246	OVSS(250)	-
19	17	38	95	95	194	171	173	142	247	251	90
20	18	37	96	96	193	172	174	141	248	252	89
21	19	36	97	97	192	173	175	140	249	253	88
22	20	-	98	98	-	174	176	-	250	254	-
23	21	-	99	99	-	175	177	-	251	255	-
24	22	35	100	100	191	176	178	139	252	256	87
25	23	34	101	101	190	177	179	138	253	257	86
26	24	33	102	102	189	178	180	137	254	258	85
27	OVSS(25)	-	103	OVSS(104)	-	179	OVSS(181)	-	255	OVSS(260)	-
28	OVDD5(26)	-	104	OVDD5(105)	-	180	OVDD5(182)	-	256	OVDD5(261)	-
29	28	32	105	106	188	181	184	136	257	262	84
30	29	31	106	107	187	182	185	135	258	263	83
31	30	30	107	109	186	183	186	134	259	265	82
32	31	-	108	110	-	184	187	-	260	266	-
33	33	-	109	111	-	185	189	-	261	267	-
34	34	-	110	112	-	186	190	-	262	268	-
35	35	29	111	113	185	187	191	133	263	269	81
36	36	28	112	115	184	188	192	132	264	271	80
37	38	27	113	116	183	189	194	131	265	272	79
38	OVSS(39)	-	114	OVSS(117)	-	190	OVSS(195)	-	266	OVSS(273)	-
39	40	26	115	118	182	191	196	130	267	274	78
40	41	25	116	120	181	192	197	129	268	276	77
41	42	24	117	121	180	193	198	128	269	277	76
42	44	-	118	122	-	194	200	-	270	278	-
43	45	-	119	123	-	195	201	-	271	279	-
44	46	-	120	124	-	196	202	-	272	280	-
45	47	23	121	126	179	197	203	127	273	282	75
46	48	22	122	127	178	198	204	126	274	283	74
47	50	21	123	128	177	199	206	125	275	284	73
48	OVDD5(51)	-	124	OVDD5(129)	-	200	OVDD5(207)	-	276	OVDD5(285)	-
49	OVSS(52)	-	125	OVSS(131)	-	201	OVSS(208)	-	277	OVSS(287)	-
50	53	20	126	132	176	202	209	124	278	288	72
51	55	19	127	133	175	203	211	123	279	289	71
52	56	18	128	134	174	204	212	122	280	290	70
53	57	-	129	136	-	205	213	-	281	292	-
54	58	-	130	137	-	206	214	-	282	293	-
55	60	17	131	138	173	207	216	121	283	294	69
56	61	16	132	139	172	208	217	120	284	295	68
57	62	15	133	140	171	209	218	119	285	296	67
58	OVSS(63)	-	134	OVSS(141)	-	210	OVSS(219)	-	286	OVSS(297)	-
59	64	14	135	142	170	211	220	118	287	298	66
60	65	13	136	143	169	212	221	117	288	299	65
61	66	-	137	144	-	213	222	-	289	300	-
62	67	12	138	145	168	214	223	116	290	301	64

Table 4-25 H4CP109 208 MicroCool Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
63	68	11	139	146	167	215	224	115	291	302	63
64	69	10	140	147	166	216	225	114	292	303	62
65	70	9	141	148	165	217	226	113	293	304	61
66	71	8	142	149	164	218	227	112	294	305	60
67	72	7	143	150	163	219	228	111	295	306	59
68	73	6	144	151	162	220	229	110	296	307	58
69	74	5	145	152	161	221	230	109	297	308	57
70	75	4	146	153	160	222	231	108	298	309	56
71	76	3	147	154	159	223	232	107	299	310	55
72	77	2	148	155	158	224	233	106	300	311	54
73	78	1	149	156	157	225	234	105	301	312	53
74	OVDD3	-	150	OVDD3	-	226	OVDD3	-	302	OVDD3	-
75	OVDD5	-	151	OVDD5	-	227	OVDD5	-	303	OVDD5	-
76	OVSS	-	152	OVSS	-	228	OVSS	-	304	OVSS	-

Notes:
1. Die pad/cell numbers start at top of LEFT side and increment counter-clockwise.
2. Package numbers start at bottom of the LEFT side and increment clockwise.
3.VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die(Array) for probe test.

Rev 1.0 6/18/93 JEB

Table 4-26 H4CP109 225 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
1	VSS	1	b	77	VSS	71	b	153	VSS	141	b	229	VSS	211	b
2	VDD	2	a	78	VDD	72	a	154	VDD	142	a	230	VDD	212	a
3	1	3	A1	79	79	73	R1	155	157	143	R15	231	235	213	A15
4	2	4	C3	80	80	74	N3	156	158	144	N13	232	236	214	C13
5	3	5	D4	81	81	75	M4	157	159	145	M12	233	237	215	D12
6	4	-	-	82	82	-	-	158	160	-	-	234	238	-	-
7	5	6	B1	83	83	76	R2	159	161	146	P15	235	239	216	A14
8	(OVDD5)6	7	a	84	(OVDD5)84	77	a	160	(OVDD5)162	147	a	236	(OVDD5)240	217	a
9	7	8	C2	85	85	78	P3	161	163	148	N14	237	241	218	B13
10	(OVSS)8	9	b	86	(OVSS)86	79	b	162	(OVSS)164	149	b	238	(OVSS)242	219	b
11	9	10	D3	87	87	80	N4	163	165	150	M13	239	243	220	C12
12	10	11	C1	88	88	81	R3	164	166	151	N15	240	244	221	A13
13	11	12	D2	89	89	82	P4	165	167	152	M14	241	245	222	B12
14	12	13	E4	90	90	83	M5	166	168	153	L12	242	246	223	D11
15	OVDD5(13)	14	a	91	OVDD5(91)	84	a	167	OVDD5(169)	154	a	243	OVDD5(247)	224	a
16	14	15	E3	92	92	85	N5	168	170	155	L13	244	248	225	C11
17	15	16	D1	93	93	86	R4	169	171	156	M15	245	249	226	A12
18	OVSS(16)	17	b	94	OVSS(94)	87	b	170	OVSS(172)	157	b	246	OVSS(250)	227	b
19	17	18	F5	95	95	88	L6	171	173	158	K11	247	251	228	E10
20	18	19	E2	96	96	89	P5	172	174	159	L14	248	252	229	B11
21	19	20	F4	97	97	90	M6	173	175	160	K12	249	253	230	D10
22	(VSS)20	21	b	98	(VSS)98	91	b	174	(VSS)176	161	b	250	(VSS)254	231	b
23	21	22	E1	99	99	92	R5	175	177	162	L15	251	255	232	A11
24	22	-	-	100	100	-	-	176	178	-	-	252	256	-	-
25	23	23	F3	101	101	93	N6	177	179	163	K13	253	257	233	C10
26	24	24	G5	102	102	94	L7	178	180	164	J11	254	258	234	E9
27	OVSS(25)	25	b	103	OVSS(104)	95	b	179	OVSS(181)	165	b	255	OVSS(260)	235	b
28	OVDD5(26)	26	a	104	OVDD5(105)	96	a	180	OVDD5(182)	166	a	256	OVDD5(261)	236	a
29	28	27	F2	105	106	97	P6	181	184	167	K14	257	262	237	B10
30	29	28	F1	106	107	98	R6	182	185	168	K15	258	263	238	A10
31	30	29	G3	107	109	99	N7	183	186	169	J13	259	265	239	C9
32	31	30	G4	108	110	100	M7	184	187	170	J12	260	266	240	D9
33	(OVSS)33	31	b	109	(OVSS)111	101	b	185	(OVSS)189	171	b	261	(OVSS)267	241	b
34	34	32	G2	110	112	102	P7	186	190	172	J14	262	268	242	B9
35	35	33	G1	111	113	103	R7	187	191	173	J15	263	269	243	A9
36	36	34	H3	112	115	104	N8	188	192	174	H13	264	271	244	C8
37	38	35	H2	113	116	105	P8	189	194	175	H14	265	272	245	B8
38	OVSS(39)	36	b	114	OVSS(117)	106	b	190	OVSS(195)	176	b	266	OVSS(273)	246	b
39	40	37	H1	115	118	107	R8	191	196	177	H15	267	274	247	A8
40	(OVDD5)41	38	a	116	(OVDD5)120	108	a	192	(OVDD5)197	178	a	268	(OVDD5)276	248	a
41	42	39	H4	117	121	109	M8	193	198	179	H12	269	277	249	D8
42	44	40	H5	118	122	110	L8	194	200	180	H11	270	278	250	E8
43	45	41	J2	119	123	111	P9	195	201	181	G14	271	279	251	B7
44	46	-	-	120	124	-	-	196	202	-	-	272	280	-	-
45	47	42	J1	121	126	112	R9	197	203	182	G15	273	282	252	A7
46	48	43	J3	122	127	113	N9	198	204	183	G13	274	283	253	C7
47	50	44	J4	123	128	114	M9	199	206	184	G12	275	284	254	D7
48	OVDD5(51)	45	a	124	OVDD5(129)	115	a	200	OVDD5(207)	185	a	276	OVDD5(285)	255	a
49	OVSS(52)	46	b	125	OVSS(131)	116	b	201	OVSS(208)	186	b	277	OVSS(287)	256	b
50	53	47	J5	126	132	117	L9	202	209	187	G11	278	288	257	E7
51	55	48	K1	127	133	118	R10	203	211	188	F15	279	289	258	A6
52	56	-	-	128	134	-	-	204	212	-	-	280	290	-	-

Table 4-26 H4CP109 225 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
53	57	49	K2	129	136	119	P10	205	213	189	F14	281	292	259	B6
54	(VDD)58	50	a	130	(VDD)137	120	a	206	(VDD)214	190	a	282	(VDD)293	260	a
55	60	51	K3	131	138	121	N10	207	216	191	F13	283	294	261	C6
56	61	52	K4	132	139	122	M10	208	217	192	F12	284	295	262	D6
57	62	53	L1	133	140	123	R11	209	218	193	E15	285	296	263	A5
58	OVSS(63)	54	b	134	OVSS(141)	124	b	210	OVSS(219)	194	b	286	OVSS(297)	264	b
59	64	55	L2	135	142	125	P11	211	220	195	E14	287	298	265	B5
60	65	56	L3	136	143	126	N11	212	221	196	E13	288	299	266	C5
61	66	57	M1	137	144	127	R12	213	222	197	D15	289	300	267	A4
62	67	58	M2	138	145	128	P12	214	223	198	D14	290	301	268	B4
63	(OVDD5)68	59	a	139	(OVDD5)146	129	a	215	(OVDD5)224	199	a	291	(OVDD5)302	269	a
64	69	60	K5	140	147	130	L10	216	225	200	F11	292	303	270	E6
65	70	61	L4	141	148	131	M11	217	226	201	E12	293	304	271	D5
66	71	62	N1	142	149	132	R13	218	227	202	C15	294	305	272	A3
67	(OVSS)72	63	b	143	(OVSS)150	133	b	219	(OVSS)228	203	b	295	(OVSS)306	273	b
68	73	64	M3	144	151	134	N12	220	229	204	D13	296	307	274	C4
69	74	-	-	145	152	-	-	221	230	-	-	297	308	-	-
70	75	65	N2	146	153	135	P13	222	231	205	C14	298	309	275	B3
71	76	66	P1	147	154	136	R14	223	232	206	B15	299	310	276	A2
72	77	67	P2	148	155	137	P14	224	233	207	B14	300	311	277	B2
73	78	68	L5	149	156	138	L11	225	234	208	E11	301	312	278	E5
74	OVDD3	-	-	150	OVDD3	-	-	226	OVDD3	-	-	302	OVDD3	-	-
75	OVDD5	69	a	151	OVDD5	139	a	227	OVDD5	209	a	303	OVDD5	279	a
76	OVSS	70	b	152	OVSS	140	b	228	OVSS	210	b	304	OVSS	280	b

NOTES:

1. Die Pad/IO-Cell numbers start at top of LEFT side and increment counter-clockwise.
2. Pkg Pin and Bond FInger numbers start at top of left side and increment counter-clockwise.
3. VSS, VDD, OVSS, OVDD3, & OVDD5 indicates fixed power and ground pads on the die(Array) for probe test.
4. OVSS & OVDD5 in () are power and ground for Final Test and are Package dependent
5. The following is a cross reference of package dependent Power and Ground Pkg Pin numbers:
PWR; a = F9,F10,G10, F6, F7, G6, J6, K6, K7, K9, K10, J10.
GND: b =F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8
6. Both OVDD5 and VDD are connected together through the package PWR pins.
7. OVDD3 must be supplied seperately through I/O package pins for mixed voltage (5V / 3.3V) I/O applications.
8. The 225 OMPAC package is limited to the following three combinations of mixed (Core/System) power combinations:
   5 V / 5 V, 5 V / 3 V & 5 V, and 3 V / 3 V.

Rev. 1.0 1/4/94 JEB
Rev. 1.1 5/11/94 JEB added notes 6 and 7.

Table 4-27 H4CP109 240 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	77	VSS	-	153	VSS	-	229	VSS	-
2	VDD	-	78	VDD	-	154	VDD	-	230	VDD	-
3	1	1	79	79	61	155	157	121	231	235	181
4	2	2	80	80	62	156	158	122	232	236	182
5	3	3	81	81	63	157	159	123	233	237	183
6	4	4	82	82	64	158	160	124	234	238	184
7	5	5	83	83	65	159	161	125	235	239	185
8	6	6	84	84	66	160	162	126	236	240	186
9	7	7	85	85	67	161	163	127	237	241	187
10	8	8	86	86	68	162	164	128	238	242	188
11	9	9	87	87	69	163	165	129	239	243	189
12	10	10	88	88	70	164	166	130	240	244	190
13	11	11	89	89	71	165	167	131	241	245	191
14	12	12	90	90	72	166	168	132	242	246	192
15	OVDD5(13)	-	91	OVDD5(91)	-	167	OVDD5(169)	-	243	OVDD5(247)	-
16	14	13	92	92	73	168	170	133	244	248	193
17	15	14	93	93	74	169	171	134	245	249	194
18	OVSS(16)	-	94	OVSS(94)	-	170	OVSS(172)	-	246	OVSS(250)	-
19	17	15	95	95	75	171	173	135	247	251	195
20	18	16	96	96	76	172	174	136	248	252	196
21	19	17	97	97	77	173	175	137	249	253	197
22	20	18	98	98	78	174	176	138	250	254	198
23	21	19	99	99	79	175	177	139	251	255	199
24	22	20	100	100	80	176	178	140	252	256	200
25	23	21	101	101	81	177	179	141	253	257	201
26	24	22	102	102	82	178	180	142	254	258	202
27	OVSS(25)	-	103	OVSS(104)	-	179	OVSS(181)	-	255	OVSS(260)	-
28	OVDD5(26)	-	104	OVDD5(105)	-	180	OVDD5(182)	-	256	OVDD5(261)	-
29	28	23	105	106	83	181	184	143	257	262	203
30	29	24	106	107	84	182	185	144	258	263	204
31	30	25	107	109	85	183	186	145	259	265	205
32	31	26	108	110	86	184	187	146	260	266	206
33	33	-	109	111	-	185	189	-	261	267	-
34	34	27	110	112	87	186	190	147	262	268	207
35	35	28	111	113	88	187	191	148	263	269	208
36	36	29	112	115	89	188	192	149	264	271	209
37	38	30	113	116	90	189	194	150	265	272	210
38	OVSS(39)	-	114	OVSS(117)	-	190	OVSS(195)	-	266	OVSS(273)	-
39	40	31	115	118	91	191	196	151	267	274	211
40	41	32	116	120	92	192	197	152	268	276	212
41	42	33	117	121	93	193	198	153	269	277	213
42	44	34	118	122	94	194	200	154	270	278	214
43	45	-	119	123	-	195	201	-	271	279	-
44	46	35	120	124	95	196	202	155	272	280	215
45	47	36	121	126	96	197	203	156	273	282	216
46	48	37	122	127	97	198	204	157	274	283	217
47	50	38	123	128	98	199	206	158	275	284	218
48	OVDD5(51)	-	124	OVDD5(129)	-	200	OVDD5(207)	-	276	OVDD5(285)	-
49	OVSS(52)	-	125	OVSS(131)	-	201	OVSS(208)	-	277	OVSS(287)	-
50	53	39	126	132	99	202	209	159	278	288	219
51	55	40	127	133	100	203	211	160	279	289	220
52	56	41	128	134	101	204	212	161	280	290	221
53	57	42	129	136	102	205	213	162	281	292	222
54	58	43	130	137	103	206	214	163	282	293	223
55	60	44	131	138	104	207	216	164	283	294	224
56	61	45	132	139	105	208	217	165	284	295	225
57	62	46	133	140	106	209	218	166	285	296	226
58	OVSS(63)	-	134	OVSS(141)	-	210	OVSS(219)	-	286	OVSS(297)	-
59	64	47	135	142	107	211	220	167	287	298	227
60	65	48	136	143	108	212	221	168	288	299	228
61	66	-	137	144	-	213	222	-	289	300	-
62	67	49	138	145	109	214	223	169	290	301	229

Table 4-27 H4CP109 240 (CU) QFP Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
63	68	50	139	146	110	215	224	170	291	302	230
64	69	51	140	147	111	216	225	171	292	303	231
65	70	52	141	148	112	217	226	172	293	304	232
66	71	53	142	149	113	218	227	173	294	305	233
67	72	54	143	150	114	219	228	174	295	306	234
68	73	55	144	151	115	220	229	175	296	307	235
69	74	56	145	152	116	221	230	176	297	308	236
70	75	57	146	153	117	222	231	177	298	309	237
71	76	58	147	154	118	223	232	178	299	310	238
72	77	59	148	155	119	224	233	179	300	311	239
73	78	60	149	156	120	225	234	180	301	312	240
74	OVDD3	-	150	OVDD3	-	226	OVDD3	-	302	OVDD3	-
75	OVDD5	-	151	OVDD5	-	227	OVDD5	-	303	OVDD5	-
76	OVSS	-	152	OVSS	-	228	OVSS	-	304	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die (Array) for probe test.

Rev 1.0 6/18/93 JEB

Table 4-28 H4CP109 313 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
1	VSS	GND	a	77	VSS	GND	a	153	VSS	GND	a	229	VSS	GND	a
2	VDD	1	D4	78	VDD	70	Z3	154	VDD	139	Z23	230	VDD	208	D22
3	1	2	E3	79	79	71	BB1	155	157	140	BB25	231	235	209	C23
4	2	3	C1	80	80	72	Z5	156	158	141	X23	232	236	210	C21
5	3	4	B2	81	81	73	BB3	157	159	142	Z25	233	237	211	A23
6	4	5	G5	82	82	74	X7	158	160	143	V21	234	238	212	E19
7	5	7	F4	83	83	76	Y6	159	161	145	W22	235	239	214	D20
8	6	8	D2	84	84	77	AA4	160	162	146	Y24	236	240	215	B22
9	7	9	F2	85	85	78	AA6	161	163	147	W24	237	241	216	B20
10	8	10	G3	86	86	79	Z7	162	164	148	V23	238	242	217	C19
11	9	11	H4	87	87	80	Y8	163	165	149	U22	239	243	218	D18
12	10	12	H6	88	88	81	W8	164	166	150	U20	240	244	219	F18
13	11	13	E1	89	89	82	BB5	165	167	151	X25	241	245	220	A21
14	12	14	J5	90	90	83	X9	166	168	152	T21	242	246	221	E17
15	OVDD5(13)	PWR	b	91	OVDD5(91)	PWR	b	167	OVDD5(169)	PWR	b	243	OVDD5(247)	PWR	b
16	14	15	K6	92	92	84	W10	168	170	153	S20	244	248	222	F16
17	15	16	H2	93	93	85	AA8	169	171	154	U24	245	249	223	B18
18	OVSS(16)	GND	a	94	OVSS(94)	GND	a	170	OVSS(172)	GND	a	246	OVSS(250)	GND	a
19	17	17	G1	95	95	86	BB7	171	173	155	V25	247	251	224	A19
20	18	18	L5	96	96	87	X11	172	174	156	R21	248	252	225	E15
21	19	19	K4	97	97	88	Y10	173	175	157	S22	249	253	226	D16
22	20	20	J3	98	98	89	Z9	174	176	158	T23	250	254	227	C17
23	21	21	K2	99	99	90	AA10	175	177	159	S24	251	255	228	B16
24	22	22	K8	100	100	91	U10	176	178	160	S18	252	256	229	H16
25	23	23	J7	101	101	92	V9	177	179	161	T19	253	257	230	G17
26	24	24	J1	102	102	93	BB9	178	180	162	T25	254	258	231	A17
27	OVSS(25)	GND	a	103	OVSS(104)	GND	a	179	OVSS(181)	GND	a	255	OVSS(260)	GND	a
28	OVDD5(26)	PWR	b	104	OVDD5(105)	PWR	b	180	OVDD5(182)	PWR	b	256	OVDD5(261)	PWR	b
29	28	25	L7	105	106	94	V11	181	184	163	R19	257	262	232	G15
30	29	26	L3	106	107	95	Z11	182	185	164	R23	258	263	233	C15
31	30	27	M4	107	109	96	Y12	183	186	165	P22	259	265	234	D14
32	31	28	L9	108	110	97	T11	184	187	166	R17	260	266	235	J15
33	33	29	M6	109	111	98	W12	185	189	167	P20	261	267	236	F14
34	34	30	L1	110	112	99	BB11	186	190	168	R25	262	268	237	A15
35	35	31	M8	111	113	100	U12	187	191	169	P18	263	269	238	H14
36	36	32	M2	112	115	101	AA12	188	192	170	P24	264	271	239	B14
37	38	33	M10	113	116	102	S12	189	194	171	P16	265	272	240	K14
38	OVSS(39)	GND	a	114	OVSS(117)	GND	a	190	OVSS(195)	GND	a	266	OVSS(273)	GND	a
39	40	34	N7	115	118	103	V13	191	196	172	N19	267	274	241	G13
40	41	35	N3	116	120	104	Z13	192	197	173	N23	268	276	242	C13
41	42	36	N1	117	121	105	BB13	193	198	174	N25	269	277	243	A13
42	44	37	P10	118	122	106	S14	194	200	175	M16	270	278	244	K12
43	45	39	P2	119	123	108	AA14	195	201	177	M24	271	279	246	B12
44	46	40	P8	120	124	109	U14	196	202	178	M18	272	280	247	H12
45	47	41	R1	121	126	110	BB15	197	203	179	L25	273	282	248	A11
46	48	42	P6	122	127	111	W14	198	204	180	M20	274	283	249	F12
47	50	43	R9	123	128	112	T15	199	206	181	L17	275	284	250	J11
48	OVDD5(51)	PWR	b	124	OVDD5(129)	PWR	b	200	OVDD5(207)	PWR	b	276	OVDD5(285)	PWR	b
49	OVSS(52)	GND	a	125	OVSS(131)	GND	a	201	OVSS(208)	GND	a	277	OVSS(287)	GND	a
50	53	44	P4	126	132	113	Y14	202	209	182	M22	278	288	251	D12
51	55	45	R3	127	133	114	Z15	203	211	183	L23	279	289	252	C11
52	56	46	R7	128	134	115	V15	204	212	184	L19	280	290	253	G11

Table 4-28 H4CP109 313 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
53	57	47	T1	129	136	116	BB17	205	213	185	J25	281	292	254	A9
54	58	48	S8	130	137	117	U16	206	214	186	K18	282	293	255	H10
55	60	49	S2	131	138	118	AA16	207	216	187	K24	283	294	256	B10
56	61	50	T7	132	139	119	V17	208	217	188	J19	284	295	257	G9
57	62	51	T3	133	140	120	Z17	209	218	189	J23	285	296	258	C9
58	OVSS(63)	GND	a	134	OVSS(141)	GND	a	210	OVSS(219)	GND	a	286	OVSS(297)	GND	a
59	64	52	S4	135	142	121	Y16	211	220	190	K22	287	298	259	D10
60	65	53	R5	136	143	122	X15	212	221	191	L21	288	299	260	E11
61	66	54	V1	137	144	123	BB19	213	222	192	G25	289	300	261	A7
62	67	55	U2	138	145	124	AA18	214	223	193	H24	290	301	262	B8
63	68	56	S6	139	146	125	W16	215	224	194	K20	291	302	263	F10
64	69	57	T5	140	147	126	X17	216	225	195	J21	292	303	264	E9
65	70	58	X1	141	148	127	BB21	217	226	196	E25	293	304	265	A5
66	71	59	U6	142	149	128	W18	218	227	197	H20	294	305	266	F8
67	72	60	U4	143	150	129	Y18	219	228	198	H22	295	306	267	D8
68	73	61	V3	144	151	130	Z19	220	229	199	G23	296	307	268	C7
69	74	62	W2	145	152	131	AA20	221	230	200	F24	297	308	269	B6
70	75	64	W4	146	153	133	Y20	222	231	202	F22	298	309	271	D6
71	76	65	X5	147	154	134	X21	223	232	203	E21	299	310	272	C5
72	77	66	W6	148	155	135	W20	224	233	204	G21	300	311	273	E7
73	78	67	Z1	149	156	136	BB23	225	234	205	C25	301	312	274	A3
74	OVDD3	69	c	150	OVDD3	138	d	226	OVDD3	207	e	302	OVDD3	276	f
75	OVDD5	PWR	b	151	OVDD5	PWR	b	227	OVDD5	PWR	b	303	OVDD5	PWR	b
76	OVSS	GND	a	152	OVSS	GND	a	228	OVSS	GND	a	304	OVSS	GND	a

NOTES:

1. Die Pad/IO-Cell numbers start at top of LEFT side and increment counter-clockwise.
2. Pkg Pin and Bond FInger numbers start at top of LEFT side and increment counter-clockwise.
3. VSS, VDD, OVSS, OVDD3, & OVDD5 indicates fixed power and ground pads on the die (Array) for probe test.
4. OVSS & OVDD5 in () are power and ground for Final Test and are Package dependent.
5. The following is a cross reference of package dependent Power and Ground Pkg Pin numbers:
PWR: a = J13, K10, K16, L11, L13, L15, M12, M14, N9, N11, N13, N15, N17, P12, P14, R11, R13, R15, S16, T13
ODD3: c = Y2, AA2 d =AA22, AA24 e = A25, B24 f = C3, E5
GND: b =G7, G19, H8, H18, J9, J17, S10, T9, T17, U8, U18, V7, V19.
6. Only OVDD5 is connected to package PWR pins. VDDis be supplied seperately through I/O package pins.

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Table 4-29 H4CP109P1 Analog PLL Option 1

BOTTOM	
DIE PAD	I/O CELL
77	VSS
78	VDD
79	AVSS
80	AVDD
81	79
82	80
83	81
84	82
85	83
86	84
87	85
88	86
89	87
90	88
91	OVDD5(90)
92	91
93	92
94	OVSS(93)
95	94
96	96
97	97
98	98
99	99
100	100
101	101
102	102
103	OVSS(104)
104	OVDD5(105)
105	106
106	107
107	109
108	110
109	111
110	112
111	113
112	115
113	116
114	OVSS(117)
115	118
116	120
117	121
118	122
119	123
120	124
121	126
122	127
123	128
124	OVDD5(129)
125	OVSS(131)
126	132
127	133
128	134
129	136

Table 4-29 H4CP109P1 Analog PLL Option 1

BOTTOM	
DIE PAD	I/O CELL
130	137
131	138
132	139
133	140
134	OVSS(141)
135	142
136	143
137	144
138	145
139	146
140	147
141	148
142	149
143	150
144	151
145	152
146	153
147	154
148	155
149	156
150	OVDD3
151	OVDD5
152	OVSS

Note: This table replaces the BOTTOM side of each pad to pin table for each array/package combination when Analog PLL option 1 is used in the H4CP109 array.

Table 4-30 H4CP109P2
Analog PLL Option 2

BOTTOM		TOP	
DIE PAD	I/O CELL	DIE PAD	I/O CELL
77	VSS	229	VSS
78	VDD	230	VDD
79	AVSS	231	AVSS
80	AVDD	232	AVDD
81	79	233	235
82	80	234	236
83	81	235	237
84	(OVDD5)82	236	(OVDD5)238
85	83	237	239
86	(OVSS)84	238	(OVSS)240
87	85	239	241
88	86	240	242
89	87	241	243
90	88	242	244
91	OVDD5(90)	243	OVDD5(246)
92	91	244	247
93	92	245	248
94	OVSS(93)	246	OVSS(249)
95	94	247	250
96	96	248	252
97	97	249	253
98	(VSS)98	250	(VSS)254
99	99	251	255
100	100	252	256
101	101	253	257
102	102	254	258
103	OVSS(104)	255	OVSS(260)
104	OVDD5(105)	256	OVDD5(261)
105	106	257	262
106	107	258	263
107	109	259	265
108	110	260	266
109	(OVSS)111	261	(OVSS)267
110	112	262	268
111	113	263	269
112	115	264	271
113	116	265	272
114	OVSS(117)	266	OVSS(273)
115	118	267	274
116	(OVDD5)120	268	(OVDD5)276
117	121	269	277
118	122	270	278
119	123	271	279
120	124	272	280
121	126	273	282
122	127	274	283
123	128	275	284
124	OVDD5(129)	276	OVDD5(285)
125	OVSS(131)	277	OVSS(287)
126	132	278	288
127	133	279	289
128	134	280	290
129	136	281	292

Table 4-30 H4CP109P2
Analog PLL Option 2

BOTTOM		TOP	
DIE PAD	I/O CELL	DIE PAD	I/O CELL
130	(VDD)137	282	(VDD)293
131	138	283	294
132	139	284	295
133	140	285	296
134	OVSS(141)	286	OVSS(297)
135	142	287	298
136	143	288	299
137	144	289	300
138	145	290	301
139	(OVDD5)146	291	(OVDD5)302
140	147	292	303
141	148	293	304
142	149	294	305
143	(OVSS)150	295	(OVSS)306
144	151	296	307
145	152	297	308
146	153	298	309
147	154	299	310
148	155	300	311
149	156	301	312
150	OVDD3	302	OVDD3
151	OVDD5	303	OVDD5
152	OVSS	304	OVSS

Note: This table replaces the BOTTOM and the TOP side of each pad to pin table for each array/package combination when Analog PLL option 2 is used in the H4CP109 array.

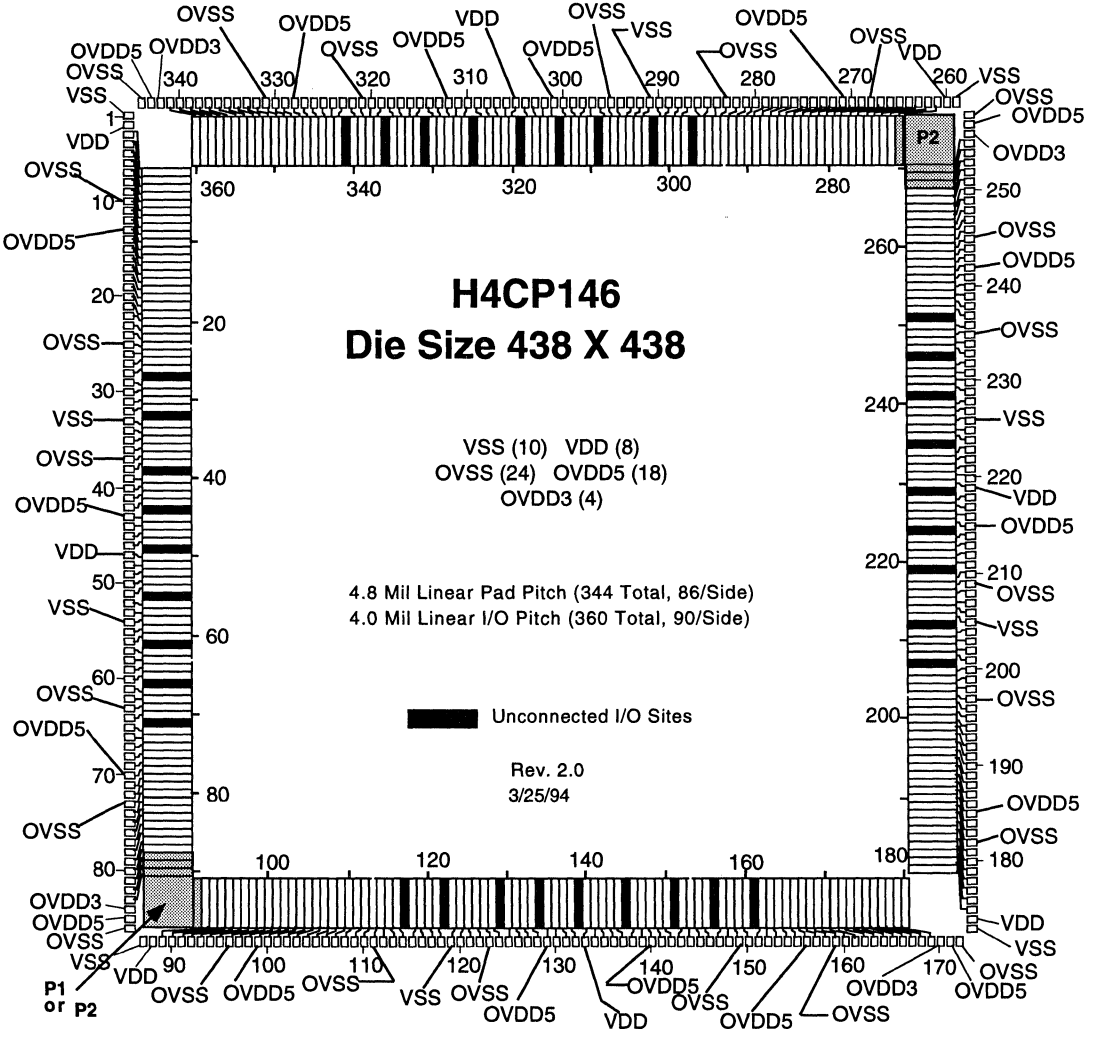

Figure 4-5 H4CP146 Footprint

Note:
P1 = Analog PLL option 1 (H4CP146P1) bottom left corner only,
see Table 4-34 for I/O to pad configuration
P2 = Analog PLL option 2 (H4CP146P2) bottom left and top right corners,
see Table 4-35 for I/O to pad configuration.

Table 4-31 H4CP146 160 MicroCool Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	87	VSS	-	173	VSS	-	259	VSS	-
2	VDD	-	88	VDD	-	174	VDD	-	260	VDD	-
3	1	40	89	91	160	175	181	120	261	271	80
4	2	39	90	92	159	176	182	119	262	272	79
5	3	38	91	93	158	177	183	118	263	273	78
6	4	37	92	94	157	178	184	117	264	274	77
7	5	-	93	95	-	179	185	-	265	275	-
8	6	36	94	96	156	180	186	116	266	276	76
9	7	35	95	97	155	181	187	115	267	277	75
10	OVSS(8)	-	96	OVSS(98)	-	182	OVSS(188)	-	268	OVSS(278)	-
11	9	34	97	99	154	183	189	114	269	279	74
12	10	33	98	100	153	184	190	113	270	280	73
13	OVDD5(11)	-	99	OVDD5(101)	-	185	OVDD5(191)	-	271	OVDD5(281)	-
14	12	-	100	102	-	186	192	-	272	282	-
15	13	-	101	103	-	187	193	-	273	283	-
16	14	32	102	104	152	188	194	112	274	284	72
17	15	31	103	105	151	189	195	111	275	285	71
18	16	-	104	106	-	190	196	-	276	286	-
19	17	-	105	107	-	191	197	-	277	287	-
20	18	-	106	108	-	192	198	-	278	288	-
21	19	30	107	109	150	193	199	110	279	289	70
22	20	29	108	110	149	194	200	109	280	290	69
23	21	-	109	111	-	195	201	-	281	291	-
24	22	-	110	112	-	196	202	-	282	292	-
25	OVSS(23)	-	111	OVSS(113)	-	197	OVSS(203)	-	283	OVSS(293)	-
26	24	28	112	114	148	198	204	108	284	294	68
27	25	27	113	115	147	199	205	107	285	295	67
28	26	-	114	116	-	200	206	-	286	296	-
29	28	-	115	118	-	201	208	-	287	298	-
30	29	-	116	119	-	202	209	-	288	299	-
31	30	26	117	120	146	203	210	106	289	300	66
32	31	25	118	121	145	204	211	105	290	301	65
33	VSS(33)	-	119	VSS(123)	-	205	VSS(213)	-	291	VSS(303)	-
34	34	-	120	124	-	206	214	-	292	304	-
35	35	24	121	125	144	207	215	104	293	305	64
36	36	23	122	126	143	208	216	103	294	306	63
37	OVSS(37)	-	123	OVSS(127)	-	209	OVSS(217)	-	295	OVSS(307)	-
38	38	-	124	128	-	210	218	-	296	308	-
39	40	-	125	130	-	211	220	-	297	310	-
40	41	22	126	131	142	212	221	102	298	311	62
41	42	21	127	132	141	213	222	101	299	312	61
42	43	-	128	133	-	214	223	-	300	313	-
43	OVDD5(45)	-	129	OVDD5(135)	-	215	OVDD5(225)	-	301	OVDD5(315)	-
44	46	20	130	136	140	216	226	100	302	316	60
45	47	19	131	137	139	217	227	99	303	317	59
46	48	18	132	138	138	218	228	98	304	318	58
47	VDD(50)	-	133	VDD(140)	-	219	VDD(230)	-	305	VDD(320)	-
48	51	-	134	141	-	220	231	-	306	321	-
49	52	-	135	142	-	221	232	-	307	322	-
50	53	17	136	143	137	222	233	97	308	323	57
51	54	16	137	144	136	223	234	96	309	324	56
52	56	-	138	146	-	224	236	-	310	326	-
53	57	-	139	147	-	225	237	-	311	327	-
54	VSS(58)	-	140	OVDD5(148)	-	226	VSS(238)	-	312	OVDD5(328)	-
55	59	15	141	149	135	227	239	95	313	329	55
56	60	14	142	150	134	228	240	94	314	330	54
57	62	-	143	152	-	229	242	-	315	332	-
58	63	-	144	153	-	230	243	-	316	333	-
59	64	-	145	154	-	231	244	-	317	334	-
60	65	-	146	155	-	232	245	-	318	335	-
61	67	13	147	157	133	233	247	93	319	337	53
62	68	12	148	158	132	234	248	92	320	338	52

Table 4-31 H4CP146 160 MicroCool Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
63	OVSS(69)	-	149	OVSS(159)	-	235	OVSS(249)	-	321	OVSS(339)	-
64	70	-	150	160	-	236	250	-	322	340	-
65	72	-	151	162	-	237	252	-	323	342	-
66	73	11	152	163	131	238	253	91	324	343	51
67	74	10	153	164	130	239	254	90	325	344	50
68	75	-	154	165	-	240	255	-	326	345	-
69	76	-	155	166	-	241	256	-	327	346	-
70	OVDD5(77)	-	156	OVDD5(167)	-	242	OVDD5(257)	-	328	OVDD5(347)	-
71	78	9	157	168	129	243	258	89	329	348	49
72	79	8	158	169	128	244	259	88	330	349	48
73	OVSS(80)	-	159	OVSS(170)	-	245	OVSS(260)	-	331	OVSS(350)	-
74	81	-	160	171	-	246	261	-	332	351	-
75	82	7	161	172	127	247	262	87	333	352	47
76	83	6	162	173	126	248	263	86	334	353	46
77	84	-	163	174	-	249	264	-	335	354	-
78	85	-	164	175	-	250	265	-	336	355	-
79	86	5	165	176	125	251	266	85	337	356	45
80	87	4	166	177	124	252	267	84	338	357	44
81	88	3	167	178	123	253	268	83	339	358	43
82	89	2	168	179	122	254	269	82	340	359	42
83	90	1	169	180	121	255	270	81	341	360	41
84	OVDD3	-	170	OVDD3	-	256	OVDD3	-	342	OVDD3	-
85	OVDD5	-	171	OVDD5	-	257	OVDD5	-	343	OVDD5	-
86	OVSS	-	172	OVSS	-	258	OVSS	-	344	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die for probe test and are array dependent.

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Table 4-32 H4CP146 208 MicroCool Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	87	VSS	-	173	VSS	-	259	VSS	-
2	VDD	-	88	VDD	-	174	VDD	-	260	VDD	-
3	1	52	89	91	208	175	181	156	261	271	104
4	2	51	90	92	207	176	182	155	262	272	103
5	3	50	91	93	206	177	183	154	263	273	102
6	4	49	92	94	205	178	184	153	264	274	101
7	5	-	93	95	-	179	185	-	265	275	-
8	6	48	94	96	204	180	186	152	266	276	100
9	7	47	95	97	203	181	187	151	267	277	99
10	OVSS(8)	-	96	OVSS(98)	-	182	OVSS(188)	-	268	OVSS(278)	-
11	9	46	97	99	202	183	189	150	269	279	98
12	10	45	98	100	201	184	190	149	270	280	97
13	OVDD5(11)	-	99	OVDD5(101)	-	185	OVDD5(191)	-	271	OVDD5(281)	-
14	12	-	100	102	-	186	192	-	272	282	-
15	13	44	101	103	200	187	193	148	273	283	96
16	14	43	102	104	199	188	194	147	274	284	95
17	15	-	103	105	-	189	195	-	275	285	-
18	16	-	104	106	-	190	196	-	276	286	-
19	17	42	105	107	198	191	197	146	277	287	94
20	18	41	106	108	197	192	198	145	278	288	93
21	19	-	107	109	-	193	199	-	279	289	-
22	20	-	108	110	-	194	200	-	280	290	-
23	21	40	109	111	196	195	201	144	281	291	92
24	22	39	110	112	195	196	202	143	282	292	91
25	OVSS(23)	-	111	OVSS(113)	-	197	OVSS(203)	-	283	OVSS(293)	-
26	24	38	112	114	194	198	204	142	284	294	90
27	25	37	113	115	193	199	205	141	285	295	89
28	26	36	114	116	192	200	206	140	286	296	88
29	28	-	115	118	-	201	208	-	287	298	-
30	29	35	116	119	191	202	209	139	288	299	87
31	30	34	117	120	190	203	210	138	289	300	86
32	31	-	118	121	-	204	211	-	290	301	-
33	VSS(33)	-	119	VSS(123)	-	205	VSS(213)	-	291	VSS(303)	-
34	34	33	120	124	189	206	214	137	292	304	85
35	35	32	121	125	188	207	215	136	293	305	84
36	36	-	122	126	-	208	216	-	294	306	-
37	OVSS(37)	-	123	OVSS(127)	-	209	OVSS(217)	-	295	OVSS(307)	-
38	38	31	124	128	187	210	218	135	296	308	83
39	40	30	125	130	186	211	220	134	297	310	82
40	41	-	126	131	-	212	221	-	298	311	-
41	42	29	127	132	185	213	222	133	299	312	81
42	43	28	128	133	184	214	223	132	300	313	80
43	OVDD5(45)	-	129	OVDD5(135)	-	215	OVDD5(225)	-	301	OVDD5(315)	-
44	46	27	130	136	183	216	226	131	302	316	79
45	47	26	131	137	182	217	227	130	303	317	78
46	48	25	132	138	181	218	228	129	304	318	77
47	VDD(50)	-	133	VDD(140)	-	219	VDD(230)	-	305	VDD(320)	-
48	51	24	134	141	180	220	231	128	306	321	76
49	52	23	135	142	179	221	232	127	307	322	75
50	53	-	136	143	-	222	233	-	308	323	-
51	54	22	137	144	178	223	234	126	309	324	74
52	56	21	138	146	177	224	236	125	310	326	73
53	57	20	139	147	176	225	237	124	311	327	72
54	VSS(58)	-	140	OVDD5(148)	-	226	VSS(238)	-	312	OVDD5(328)	-
55	59	19	141	149	175	227	239	123	313	329	71
56	60	18	142	150	174	228	240	122	314	330	70
57	62	-	143	152	-	229	242	-	315	332	-
58	63	17	144	153	173	230	243	121	316	333	69
59	64	16	145	154	172	231	244	120	317	334	68
60	65	-	146	155	-	232	245	-	318	335	-
61	67	15	147	157	171	233	247	119	319	337	67
62	68	14	148	158	170	234	248	118	320	338	66

Table 4-32 H4CP146 208 MicroCool Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
63	OVSS(69)	-	149	OVSS(159)	-	235	OVSS(249)	-	321	OVSS(339)	-
64	70	-	150	160	-	236	250	-	322	340	-
65	72	13	151	162	169	237	252	117	323	342	65
66	73	12	152	163	168	238	253	116	324	343	64
67	74	-	153	164	-	239	254	-	325	344	-
68	75	11	154	165	167	240	255	115	326	345	63
69	76	10	155	166	166	241	256	114	327	346	62
70	OVDD5(77)	-	156	OVDD5(167)	-	242	OVDD5(257)	-	328	OVDD5(347)	-
71	78	9	157	168	165	243	258	113	329	348	61
72	79	8	158	169	164	244	259	112	330	349	60
73	OVSS(80)	-	159	OVSS(170)	-	245	OVSS(260)	-	331	OVSS(350)	-
74	81	-	160	171	-	246	261	-	332	351	-
75	82	7	161	172	163	247	262	111	333	352	59
76	83	6	162	173	162	248	263	110	334	353	58
77	84	-	163	174	-	249	264	-	335	354	-
78	85	-	164	175	-	250	265	-	336	355	-
79	86	5	165	176	161	251	266	109	337	356	57
80	87	4	166	177	160	252	267	108	338	357	56
81	88	3	167	178	159	253	268	107	339	358	55
82	89	2	168	179	158	254	269	106	340	359	54
83	90	1	169	180	157	255	270	105	341	360	53
84	OVDD3	-	170	OVDD3	-	256	OVDD3	-	342	OVDD3	-
85	OVDD5	-	171	OVDD5	-	257	OVDD5	-	343	OVDD5	-
86	OVSS	-	172	OVSS	-	258	OVSS	-	344	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die for probe test and are array dependent.

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Table 4-33 H4CP146 313 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
1	VSS	GND	a	87	VSS	GND	a	173	VSS	GND	a	259	VSS	GND	a
2	VDD	1	D4	88	VDD	70	Z3	174	VDD	139	Z23	260	VDD	208	D22
3	1	2	E3	89	91	71	BB1	175	181	140	BB25	261	271	209	C23
4	2	3	C1	90	92	72	Z5	176	182	141	X23	262	272	210	C21
5	3	4	B2	91	93	73	BB3	177	183	142	Z25	263	273	211	A23
6	4	5	G5	92	94	74	X7	178	184	143	V21	264	274	212	E19
7	(OVDD3)5	6	F6	93	(OVDD3)95	75	Y4	179	(OVDD3)185	144	Y22	265	(OVDD3)275	213	F20
8	6	7	F4	94	96	76	Y6	180	186	145	W22	266	276	214	D20
9	7	8	D2	95	97	77	AA4	181	187	146	Y24	267	277	215	B22
10	OVSS(8)	GND	a	96	OVSS(98)	GND	a	182	OVSS(188)	GND	a	268	OVSS(278)	GND	a
11	9	9	F2	97	99	78	AA6	183	189	147	W24	269	279	216	B20
12	10	10	G3	98	100	79	Z7	184	190	148	V23	270	280	217	C19
13	OVDD5(11)	PWR	b	99	OVDD5(101)	PWR	b	185	OVDD5(191)	PWR	b	271	OVDD5(281)	PWR	b
14	12	11	H4	100	102	80	Y8	186	192	149	U22	272	282	218	D18
15	13	12	H6	101	103	81	W8	187	193	150	U20	273	283	219	F18
16	14	13	E1	102	104	82	BB5	188	194	151	X25	274	284	220	A21
17	15	14	J5	103	105	83	X9	189	195	152	T21	275	285	221	E17
18	(OVSS)16	GND	a	104	(OVSS)106	GND	a	190	(OVSS)196	GND	a	276	(OVSS)286	GND	a
19	17	15	K6	105	107	84	W10	191	197	153	S20	277	287	222	F16
20	18	16	H2	106	108	85	AA8	192	198	154	U24	278	288	223	B18
21	19	17	G1	107	109	86	BB7	193	199	155	V25	279	289	224	A19
22	20	18	L5	108	110	87	X11	194	200	156	R21	280	290	225	E15
23	21	19	K4	109	111	88	Y10	195	201	157	S22	281	291	226	D16
24	22	20	J3	110	112	89	Z9	196	202	158	T23	282	292	227	C17
25	OVSS(23)	GND	a	111	OVSS(113)	GND	a	197	OVSS(203)	GND	a	283	OVSS(293)	GND	a
26	24	21	K2	112	114	90	AA10	198	204	159	S24	284	294	228	B16
27	25	22	K8	113	115	91	U10	199	205	160	S18	285	295	229	H16
28	26	23	J7	114	116	92	V9	200	206	161	T19	286	296	230	G17
29	(OVDD5)28	PWR	b	115	(OVDD5)118	PWR	b	201	(OVDD5)208	PWR	b	287	(OVDD5)298	PWR	b
30	29	24	J1	116	119	93	BB9	202	209	162	T25	288	299	231	A17
31	30	25	L7	117	120	94	V11	203	210	163	R19	289	300	232	G15
32	31	26	L3	118	121	95	Z11	204	211	164	R23	290	301	233	C15
33	VSS(33)	GND	a	119	VSS(123)	GND	a	205	VSS(213)	GND	a	291	VSS(303)	GND	a
34	34	27	M4	120	124	96	Y12	206	214	165	P22	292	304	234	D14
35	35	28	L9	121	125	97	T11	207	215	166	R17	293	305	235	J15
36	36	29	M6	122	126	98	W12	208	216	167	P20	294	306	236	F14
37	OVSS(37)	GND	a	123	OVSS(127)	GND	a	209	OVSS(217)	GND	a	295	OVSS(307)	GND	a
38	38	30	L1	124	128	99	BB11	210	218	168	R25	296	308	237	A15
39	40	31	M8	125	130	100	U12	211	220	169	P18	297	310	238	H14
40	41	32	M2	126	131	101	AA12	212	221	170	P24	298	311	239	B14
41	42	33	M10	127	132	102	S12	213	222	171	P16	299	312	240	K14
42	43	34	N7	128	133	103	V13	214	223	172	N19	300	313	241	G13
43	OVDD5(45)	PWR	b	129	OVDD5(135)	PWR	b	215	OVDD5(225)	PWR	b	301	OVDD5(315)	PWR	b
44	46	35	N3	130	136	104	Z13	216	226	173	N23	302	316	242	C13
45	47	36	N1	131	137	105	BB13	217	227	174	N25	303	317	243	A13
46	48	37	P10	132	138	106	S14	218	228	175	M16	304	318	244	K12
47	VDD(50)	38	N5	133	VDD(140)	107	X13	219	VDD(230)	176	N21	305	VDD(320)	245	E13
48	51	39	P2	134	141	108	AA14	220	231	177	M24	306	321	246	B12
49	52	40	P8	135	142	109	U14	221	232	178	M18	307	322	247	H12
50	53	41	R1	136	143	110	BB15	222	233	179	L25	308	323	248	A11
51	54	42	P6	137	144	111	W14	223	234	180	M20	309	324	249	F12
52	56	43	R9	138	146	112	T15	224	236	181	L17	310	326	250	J11

Table 4-33 H4CP146 313 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
53	57	44	P4	139	147	113	Y14	225	237	182	M22	311	327	251	D12
54	VSS(58)	GND	a	140	OVDD5(148)	PWR	b	226	VSS(238)	GND	a	312	OVDD5(328)	PWR	b
55	59	45	R3	141	149	114	Z15	227	239	183	L23	313	329	252	C11
56	60	46	R7	142	150	115	V15	228	240	184	L19	314	330	253	G11
57	(OVSS)62	GND	a	143	(OVSS)152	GND	a	229	(OVSS)242	GND	a	315	(OVSS)332	GND	a
58	63	47	T1	144	153	116	BB17	230	243	185	J25	316	333	254	A9
59	64	48	S8	145	154	117	U16	231	244	186	K18	317	334	255	H10
60	(OVDD5)65	PWR	b	146	(OVDD5)155	PWR	b	232	(OVDD5)245	PWR	b	318	(OVDD5)335	PWR	b
61	67	49	S2	147	157	118	AA16	233	247	187	K24	319	337	256	B10
62	68	50	T7	148	158	119	V17	234	248	188	J19	320	338	257	G9
63	OVSS(69)	GND	a	149	OVSS(159)	GND	a	235	OVSS(249)	GND	a	321	OVSS(339)	GND	a
64	70	51	T3	150	160	120	Z17	236	250	189	J23	322	340	258	C9
65	72	52	S4	151	162	121	Y16	237	252	190	K22	323	342	259	D10
66	73	53	R5	152	163	122	X15	238	253	191	L21	324	343	260	E11
67	74	54	V1	153	164	123	BB19	239	254	192	G25	325	344	261	A7
68	75	55	U2	154	165	124	AA18	240	255	193	H24	326	345	262	B8
69	76	56	S6	155	166	125	W16	241	256	194	K20	327	346	263	F10
70	OVDD5(77)	PWR	b	156	OVDD5(167)	PWR	b	242	OVDD5(257)	PWR	b	328	OVDD5(347)	PWR	b
71	78	57	T5	157	168	126	X17	243	258	195	J21	329	348	264	E9
72	79	58	X1	158	169	127	BB21	244	259	196	E25	330	349	265	A5
73	OVSS(80)	GND	a	159	OVSS(170)	GND	a	245	OVSS(260)	GND	a	331	OVSS(350)	GND	a
74	81	59	U6	160	171	128	W18	246	261	197	H20	332	351	266	F8
75	82	60	U4	161	172	129	Y18	247	262	198	H22	333	352	267	D8
76	83	61	V3	162	173	130	Z19	248	263	199	G23	334	353	268	C7
77	84	62	W2	163	174	131	AA20	249	264	200	F24	335	354	269	B6
78	(VDD)85	63	V5	164	(VDD)175	132	X19	250	(VDD)265	201	D24	336	(VDD)355	270	B4
79	86	64	W4	165	176	133	Y20	251	266	202	F22	337	356	271	D6
80	87	65	X5	166	177	134	X21	252	267	203	E21	338	357	272	C5
81	88	66	W6	167	178	135	W20	253	268	204	G21	339	358	273	E7
82	89	67	Z1	168	179	136	BB23	254	269	205	C25	340	359	274	A3
83	90	68	X3	169	180	137	Z21	255	270	206	E23	341	360	275	A1
84	OVDD3	69	c	170	OVDD3	138	d	256	OVDD3	207	e	342	OVDD3	276	f
85	OVDD5	PWR	b	171	OVDD5	PWR	b	257	OVDD5	PWR	b	343	OVDD5	PWR	b
86	OVSS	GND	a	172	OVSS	GND	a	258	OVSS	GND	a	344	OVSS	GND	a

NOTES:

1. Die Pad/IO-Cell numbers start at top of LEFT side and increment counter-clockwise.
2. Pkg Pin and Bond FInger numbers start at top of left side and increment counter-clockwise.
3. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die (Array) for probe test.
4. OVSS & OVDD5 in () are power and ground for Final Test and are Package dependent
5. The following is a cross reference of package dependent Power and Ground Pkg Pin numbers:
GND: a = J13, K10, K16, L11, L13, L15, M12, M14, N9, N11, N13, N15, N17, P12, P14, R11, R13, R15, S16, T13
OVDD3: c = Y2, AA2 d = AA22, AA24 e = A25, B24 f = C3, E5
PWR: b = G7, G19, H8, H18, J9, J17, S10, T9, T17, U8, U18, V7, V19
6. Only OVDD5 is connected to package PWR pins.

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Table 4-34 H4CP146P1 Analog PLL Option 1

BOTTOM SIDE	
DIE	
Die Pad	I/O Cell
87	VSS
88	VDD
89	AVSS
90	AVDD
91	91
92	92
93	93
94	94
95	95
96	OVSS(96)
97	97
98	99
99	OVDD5(100)
100	101
101	102
102	104
103	105
104	106
105	107
106	108
107	109
108	110
109	111
110	112
111	OVSS(113)
112	114
113	115
114	116
115	118
116	119
117	120
118	121
119	VSS(123)
120	124
121	125
122	126
123	OVSS(127)
124	128
125	130
126	131
127	132
128	133
129	OVDD5(135)
130	136
131	137
132	138
133	VDD(140)
134	141
135	142
136	143
137	144
138	146

Table 4-34 H4CP146P1 Analog PLL Option 1

BOTTOM SIDE	
DIE	
Die Pad	I/O Cell
139	147
140	OVDD5(148)
141	149
142	150
143	152
144	153
145	154
146	155
147	157
148	158
149	OVSS(159)
150	160
151	162
152	163
153	164
154	165
155	166
156	OVDD5(167)
157	168
158	169
159	OVSS(170)
160	171
161	172
162	173
163	174
164	175
165	176
166	177
167	178
168	179
169	180
170	OVDD3
171	OVDD5
172	OVSS

Note: This table replaces the BOTTOM side of each pad to pin table for each array/package combination when Analog PLL option 1 is used in the H4CP146 array.

Table 4-35 H4CP146P2 Analog PLL Option 2

BOTTOM SIDE		TOP	
DIE		DIE	
Die Pad	I/O Cell	Die Pad	I/O Cell
87	VSS	259	VSS
88	VDD	260	VDD
89	AVSS	261	AVSS
90	AVDD	262	AVDD
91	91	263	271
92	92	264	272
93	93	265	273
94	94	266	274
95	95	267	275
96	OVSS(96)	268	OVSS(276)
97	97	269	277
98	99	270	279
99	OVDD5(100)	271	OVDD5(280)
100	101	272	281
101	102	273	282
102	104	274	284
103	105	275	285
104	106	276	286
105	107	277	287
106	108	278	288
107	109	279	289
108	110	280	290
109	111	281	291
110	112	282	292
111	OVSS(113)	283	OVSS(293)
112	114	284	294
113	115	285	295
114	116	286	296
115	118	287	298
116	119	288	299
117	120	289	300
118	121	290	301
119	VSS(123)	291	VSS(303)
120	124	292	304
121	125	293	305
122	126	294	306
123	OVSS(127)	295	OVSS(307)
124	128	296	308
125	130	297	310
126	131	298	311
127	132	299	312
128	133	300	313
129	OVDD5(135)	301	OVDD5(315)
130	136	302	316
131	137	303	317
132	138	304	318
133	VDD(140)	305	VDD(320)
134	141	306	321
135	142	307	322
136	143	308	323
137	144	309	324

Table 4-35 H4CP146P2 Analog PLL Option 2

BOTTOM SIDE		TOP	
DIE		DIE	
Die Pad	I/O Cell	Die Pad	I/O Cell
138	146	310	326
139	147	311	327
140	OVDD5(148)	312	OVDD5(328)
141	149	313	329
142	150	314	330
143	152	315	332
144	153	316	333
145	154	317	334
146	155	318	335
147	157	319	337
148	158	320	338
149	OVSS(159)	321	OVSS(339)
150	160	322	340
151	162	323	342
152	163	324	343
153	164	325	344
154	165	326	345
155	166	327	346
156	OVDD5(167)	328	OVDD5(347)
157	168	329	348
158	169	330	349
159	OVSS(170)	331	OVSS(350)
160	171	332	351
161	172	333	352
162	173	334	353
163	174	335	354
164	175	336	355
165	176	337	356
166	177	338	357
167	178	339	358
168	179	340	359
169	180	341	360
170	OVDD3	342	OVDD3
171	OVDD5	343	OVDD5
172	OVSS	344	OVSS

Note: This table replaces the BOTTOM and the TOP side of each pad to pin table for each array/package combination when Analog PLL option 2 is used in the H4CP146 array.

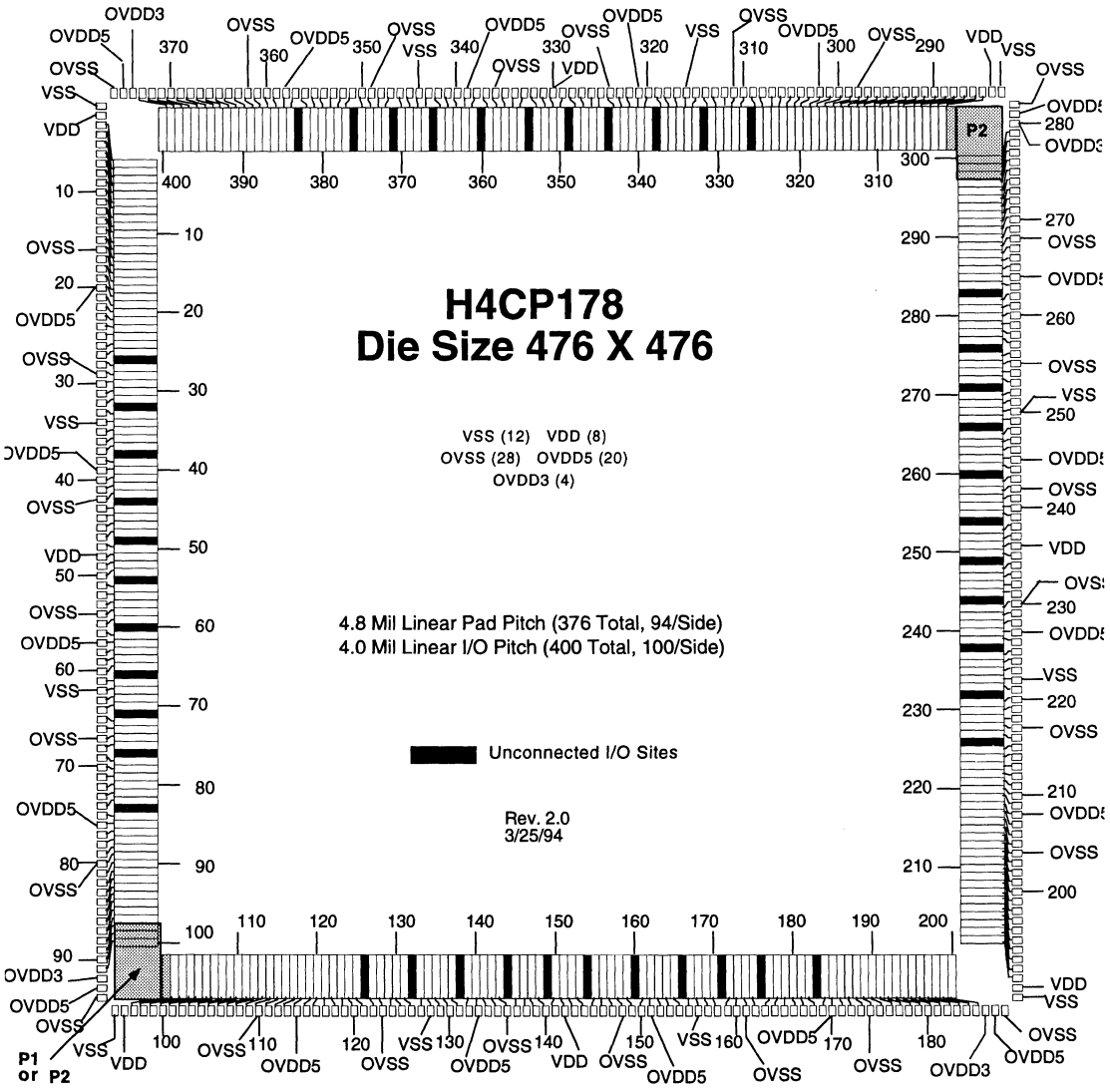

Figure 4-6 H4CP178 Footprint

Note:
P1 = Analog PLL option 1 (H4CP178P1) bottom left corner only,
see Table 4-39 for I/O to pad configuration.
P2 = Analog PLL option 2 (H4CP178P2) bottom left and top right corners,
see Table 4-40 for I/O to pad configuration.

Table 4-36 H4CP178 160 MicroCool Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	95	VSS	-	189	VSS	-	283	VSS	-
2	VDD	-	96	VDD	-	190	VDD	-	284	VDD	-
3	1	40	97	101	160	191	201	120	285	301	80
4	2	39	98	102	159	192	202	119	286	302	79
5	3	38	99	103	158	193	203	118	287	303	78
6	4	37	100	104	157	194	204	117	288	304	77
7	5	36	101	105	156	195	205	116	289	305	76
8	6	-	102	106	-	196	206	-	290	306	-
9	7	-	103	107	-	197	207	-	291	307	-
10	8	-	104	108	-	198	208	-	292	308	-
11	9	35	105	109	155	199	209	115	293	309	75
12	10	34	106	110	154	200	210	114	294	310	74
13	11	-	107	111	-	201	211	-	295	311	-
14	12	-	108	112	-	202	212	-	296	312	-
15	13	-	109	113	-	203	213	-	297	313	-
16	OVSS(14)	-	110	OVSS(114)	-	204	OVSS(214)	-	298	OVSS(314)	-
17	15	33	111	115	153	205	215	113	299	315	73
18	16	32	112	116	152	206	216	112	300	316	72
19	17	-	113	117	-	207	217	-	301	317	-
20	OVDD5(18)	-	114	OVDD5(118)	-	208	OVDD5(218)	-	302	OVDD5(318)	-
21	19	31	115	119	151	209	219	111	303	319	71
22	20	30	116	120	150	210	220	110	304	320	70
23	21	-	117	121	-	211	221	-	305	321	-
24	22	-	118	122	-	212	222	-	306	322	-
25	23	-	119	123	-	213	223	-	307	323	-
26	24	29	120	124	149	214	224	109	308	324	69
27	25	28	121	125	148	215	225	108	309	325	68
28	27	-	122	127	-	216	227	-	310	327	-
29	OVSS(28)	-	123	OVSS(128)	-	217	OVSS(228)	-	311	OVSS(328)	-
30	29	-	124	129	-	218	229	-	312	329	-
31	30	27	125	130	147	219	230	107	313	330	67
32	31	26	126	131	146	220	231	106	314	331	66
33	33	-	127	133	-	221	233	-	315	333	-
34	VSS(34)	-	128	VSS(134)	-	222	VSS(234)	-	316	VSS(334)	-
35	35	-	129	135	-	223	235	-	317	335	-
36	36	25	130	136	145	224	236	105	318	336	65
37	37	24	131	137	144	225	237	104	319	337	64
38	39	-	132	139	-	226	239	-	320	339	-
39	OVDD5(40)	-	133	OVDD5(140)	-	227	OVDD5(240)	-	321	OVDD5(340)	-
40	41	23	134	141	143	228	241	103	322	341	63
41	42	22	135	142	142	229	242	102	323	342	62
42	OVSS(43)	-	136	OVSS(143)	-	230	OVSS(243)	-	324	OVSS(343)	-
43	45	-	137	145	-	231	245	-	325	345	-
44	46	-	138	146	-	232	246	-	326	346	-
45	47	21	139	147	141	233	247	101	327	347	61
46	48	20	140	148	140	234	248	100	328	348	60
47	50	-	141	150	-	235	250	-	329	350	-
48	VDD(51)	-	142	VDD(151)	-	236	VDD(251)	-	330	VDD(351)	-
49	52	-	143	152	-	237	252	-	331	352	-
50	53	-	144	153	-	238	253	-	332	353	-
51	55	19	145	155	139	239	255	99	333	355	59
52	56	18	146	156	138	240	256	98	334	356	58
53	57	17	147	157	137	241	257	97	335	357	57
54	OVSS(58)	-	148	OVSS(158)	-	242	OVSS(258)	-	336	OVSS(358)	-
55	59	-	149	159	-	243	259	-	337	359	-
56	61	-	150	161	-	244	261	-	338	361	-
57	OVDD5(62)	-	151	OVDD5(162)	-	245	OVDD5(262)	-	339	OVDD5(362)	-
58	63	16	152	163	136	246	263	96	340	363	56
59	64	15	153	164	135	247	264	95	341	364	55
60	65	-	154	165	-	248	265	-	342	365	-
61	67	-	155	167	-	249	267	-	343	367	-
62	VSS(68)	-	156	VSS(168)	-	250	VSS(268)	-	344	VSS(368)	-

Table 4-36 H4CP178 160 MicroCool Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
63	69	14	157	169	134	251	269	94	345	369	54
64	70	13	158	170	133	252	270	93	346	370	53
65	72	-	159	172	-	253	272	-	347	372	-
66	73	-	160	173	-	254	273	-	348	373	-
67	OVSS(74)	-	161	OVSS(174)	-	255	OVSS(274)	-	349	OVSS(374)	-
68	75	-	162	175	-	256	275	-	350	375	-
69	77	12	163	177	132	257	277	92	351	377	52
70	78	11	164	178	131	258	278	91	352	378	51
71	79	-	165	179	-	259	279	-	353	379	-
72	80	-	166	180	-	260	280	-	354	380	-
73	81	10	167	181	130	261	281	90	355	381	50
74	82	9	168	182	129	262	282	89	356	382	49
75	84	-	169	184	-	263	284	-	357	384	-
76	OVDD5(85)	-	170	OVDD5(185)	-	264	OVDD5(285)	-	358	OVDD5(385)	-
77	86	-	171	186	-	265	286	-	359	386	-
78	87	8	172	187	128	266	287	88	360	387	48
79	88	7	173	188	127	267	288	87	361	388	47
80	OVSS(89)	-	174	OVSS(189)	-	268	OVSS(289)	-	362	OVSS(389)	-
81	90	-	175	190	-	269	290	-	363	390	-
82	91	-	176	191	-	270	291	-	364	391	-
83	92	6	177	192	126	271	292	86	365	392	46
84	93	5	178	193	125	272	293	85	366	393	45
85	94	-	179	194	-	273	294	-	367	394	-
86	95	-	180	195	-	274	295	-	368	395	-
87	96	-	181	196	-	275	296	-	369	396	-
88	97	4	182	197	124	276	297	84	370	397	44
89	98	3	183	198	123	277	298	83	371	398	43
90	99	2	184	199	122	278	299	82	372	399	42
91	100	1	185	200	121	279	300	81	373	400	41
92	OVDD3	-	186	OVDD3	-	280	OVDD3	-	374	OVDD3	-
93	OVDD5	-	187	OVDD5	-	281	OVDD5	-	375	OVDD5	-
94	OVSS	-	188	OVSS	-	282	OVSS	-	376	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die for probe test and are array dependent.

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Table 4-37 H4CP178 208 MicroCool Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
1	VSS	-	95	VSS	-	189	VSS	-	283	VSS	-
2	VDD	-	96	VDD	-	190	VDD	-	284	VDD	-
3	1	52	97	101	208	191	201	156	285	301	104
4	2	51	98	102	207	192	202	155	286	302	103
5	3	50	99	103	206	193	203	154	287	303	102
6	4	49	100	104	205	194	204	153	288	304	101
7	5	-	101	105	-	195	205	-	289	305	-
8	6	-	102	106	-	196	206	-	290	306	-
9	7	48	103	107	204	197	207	152	291	307	100
10	8	47	104	108	203	198	208	151	292	308	99
11	9	-	105	109	-	199	209	-	293	309	-
12	10	-	106	110	-	200	210	-	294	310	-
13	11	-	107	111	-	201	211	-	295	311	-
14	12	46	108	112	202	202	212	150	296	312	98
15	13	45	109	113	201	203	213	149	297	313	97
16	OVSS(14)	-	110	OVSS(114)	-	204	OVSS(214)	-	298	OVSS(314)	-
17	15	-	111	115	-	205	215	-	299	315	-
18	16	44	112	116	200	206	216	148	300	316	96
19	17	43	113	117	199	207	217	147	301	317	95
20	OVDD5(18)	-	114	OVDD5(118)	-	208	OVDD5(218)	-	302	OVDD5(318)	-
21	19	42	115	119	198	209	219	146	303	319	94
22	20	41	116	120	197	210	220	145	304	320	93
23	21	-	117	121	-	211	221	-	305	321	-
24	22	40	118	122	196	212	222	144	306	322	92
25	23	39	119	123	195	213	223	143	307	323	91
26	24	-	120	124	-	214	224	-	308	324	-
27	25	38	121	125	194	215	225	142	309	325	90
28	27	37	122	127	193	216	227	141	310	327	89
29	OVSS(28)	-	123	OVSS(128)	-	217	OVSS(228)	-	311	OVSS(328)	-
30	29	-	124	129	-	218	229	-	312	329	-
31	30	36	125	130	192	219	230	140	313	330	88
32	31	35	126	131	191	220	231	139	314	331	87
33	33	-	127	133	-	221	233	-	315	333	-
34	VSS(34)	-	128	VSS(134)	-	222	VSS(234)	-	316	VSS(334)	-
35	35	-	129	135	-	223	235	-	317	335	-
36	36	34	130	136	190	224	236	138	318	336	86
37	37	33	131	137	189	225	237	137	319	337	85
38	39	-	132	139	-	226	239	-	320	339	-
39	OVDD5(40)	-	133	OVDD5(140)	-	227	OVDD5(240)	-	321	OVDD5(340)	-
40	41	32	134	141	188	228	241	136	322	341	84
41	42	31	135	142	187	229	242	135	323	342	83
42	OVSS(43)	-	136	OVSS(143)	-	230	OVSS(243)	-	324	OVSS(343)	-
43	45	30	137	145	186	231	245	134	325	345	82
44	46	29	138	146	185	232	246	133	326	346	81
45	47	28	139	147	184	233	247	132	327	347	80
46	48	27	140	148	183	234	248	131	328	348	79
47	50	-	141	150	-	235	250	-	329	350	-
48	VDD(51)	-	142	VDD(151)	-	236	VDD(251)	-	330	VDD(351)	-
49	52	26	143	152	182	237	252	130	331	352	78
50	53	25	144	153	181	238	253	129	332	353	77
51	55	-	145	155	-	239	255	-	333	355	-
52	56	24	146	156	180	240	256	128	334	356	76
53	57	23	147	157	179	241	257	127	335	357	75
54	OVSS(58)	-	148	OVSS(158)	-	242	OVSS(258)	-	336	OVSS(358)	-
55	59	22	149	159	178	243	259	126	337	359	74
56	61	21	150	161	177	244	261	125	338	361	73
57	OVDD5(62)	-	151	OVDD5(162)	-	245	OVDD5(262)	-	339	OVDD5(362)	-
58	63	-	152	163	-	246	263	-	340	363	-
59	64	20	153	164	176	247	264	124	341	364	72
60	65	19	154	165	175	248	265	123	342	365	71
61	67	-	155	167	-	249	267	-	343	367	-
62	VSS(68)	-	156	VSS(168)	-	250	VSS(268)	-	344	VSS(368)	-

Table 4-37 H4CP178 208 MicroCool Pad to Pin Cross Reference

LEFT			BOTTOM			RIGHT			TOP		
DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE	DIE PAD	I/O CELL	PACKAGE
63	69	18	157	169	174	251	269	122	345	369	70
64	70	17	158	170	173	252	270	121	346	370	69
65	72	16	159	172	172	253	272	120	347	372	68
66	73	15	160	173	171	254	273	119	348	373	67
67	OVSS(74)	-	161	OVSS(174)	-	255	OVSS(274)	-	349	OVSS(374)	-
68	75	-	162	175	-	256	275	-	350	375	-
69	77	14	163	177	170	257	277	118	351	377	66
70	78	13	164	178	169	258	278	117	352	378	65
71	79	-	165	179	-	259	279	-	353	379	-
72	80	-	166	180	-	260	280	-	354	380	-
73	81	12	167	181	168	261	281	116	355	381	64
74	82	11	168	182	167	262	282	115	356	382	63
75	84	-	169	184	-	263	284	-	357	384	-
76	OVDD5(85)	-	170	OVDD5(185)	-	264	OVDD5(285)	-	358	OVDD5(385)	-
77	86	10	171	186	166	265	286	114	359	386	62
78	87	9	172	187	165	266	287	113	360	387	61
79	88	-	173	188	-	267	288	-	361	388	-
80	OVSS(89)	-	174	OVSS(189)	-	268	OVSS(289)	-	362	OVSS(389)	-
81	90	8	175	190	164	269	290	112	363	390	60
82	91	7	176	191	163	270	291	111	364	391	59
83	92	-	177	192	-	271	292	-	365	392	-
84	93	6	178	193	162	272	293	110	366	393	58
85	94	5	179	194	161	273	294	109	367	394	57
86	95	-	180	195	-	274	295	-	368	395	-
87	96	-	181	196	-	275	296	-	369	396	-
88	97	4	182	197	160	276	297	108	370	397	56
89	98	3	183	198	159	277	298	107	371	398	55
90	99	2	184	199	158	278	299	106	372	399	54
91	100	1	185	200	157	279	300	105	373	400	53
92	OVDD3	-	186	OVDD3	-	280	OVDD3	-	374	OVDD3	-
93	OVDD5	-	187	OVDD5	-	281	OVDD5	-	375	OVDD5	-
94	OVSS	-	188	OVSS	-	282	OVSS	-	376	OVSS	-

Notes:
1. Die pad/cell and Package numbers start at top of LEFT side and increment counter-clockwise.
2. VSS, VDD, OVSS, OVDD3 and OVDD5 indicate fixed power and ground pads on the die for probe test and are array dependent.

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Table 4-38 H4CP178 313 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
1	VSS	GND	a	95	VSS	GND	a	189	VSS	GND	a	283	VSS	GND	a
2	VDD	1	D4	96	VDD	71	Z3	190	VDD	141	Z23	284	VDD	211	D22
3	1	2	E3	97	101	72	BB1	191	201	142	BB25	285	301	212	C23
4	2	3	C1	98	102	73	Z5	192	202	143	X23	286	302	213	C21
5	3	4	B2	99	103	74	BB3	193	203	144	Z25	287	303	214	A23
6	4	5	G5	100	104	75	X7	194	204	145	V21	288	304	215	E19
7	5	6	F6	101	105	76	Y4	195	205	146	Y22	289	305	216	F20
8	(OVSS)6	GND	a	102	(OVSS)106	GND	a	196	(OVSS)206	GND	a	290	(OVSS)306	GND	a
9	7	7	F4	103	107	77	Y6	197	207	147	W22	291	307	217	D20
10	8	8	D2	104	108	78	AA4	198	208	148	Y24	292	308	218	B22
11	9	9	F2	105	109	79	AA6	199	209	149	W24	293	309	219	B20
12	10	10	G3	106	110	80	Z7	200	210	150	V23	294	310	220	C19
13	11	-	-	107	111	-	-	201	211	-	-	295	311	-	-
14	12	11	H4	108	112	81	Y8	202	212	151	U22	296	312	221	D18
15	13	12	H6	109	113	82	W8	203	213	152	U20	297	313	222	F18
16	OVSS(14)	GND	a	110	OVSS(114)	GND	a	204	OVSS(214)	GND	a	298	OVSS(314)	GND	a
17	15	13	E1	111	115	83	BB5	205	215	153	X25	299	315	223	A21
18	16	14	J5	112	116	84	X9	206	216	154	T21	300	316	224	E17
19	17	15	K6	113	117	85	W10	207	217	155	S20	301	317	225	F16
20	OVDD5(18)	PWR	b	114	OVDD5(118)	PWR	b	208	OVDD5(218)	PWR	b	302	OVDD5(318)	PWR	b
21	19	16	H2	115	119	86	AA8	209	219	156	U24	303	319	226	B18
22	20	17	G1	116	120	87	BB7	210	220	157	V25	304	320	227	A19
23	(VDD)21	18	L5	117	(VDD)121	88	X11	211	(VDD)221	158	R21	305	(VDD)321	228	E15
24	22	19	K4	118	122	89	Y10	212	222	159	S22	306	322	229	D16
25	23	20	J3	119	123	90	Z9	213	223	160	T23	307	323	230	C17
26	24	21	K2	120	124	91	AA10	214	224	161	S24	308	324	231	B16
27	25	22	K8	121	125	92	U10	215	225	162	S18	309	325	232	H16
28	27	23	J7	122	127	93	V9	216	227	163	T19	310	327	233	G17
29	OVSS(28)	GND	a	123	OVSS(128)	GND	a	217	OVSS(228)	GND	a	311	OVSS(328)	GND	a
30	(OVDD3)29	24	J1	124	(OVDD3)129	94	BB9	218	(OVDD3)229	164	T25	312	(OVDD3)329	234	A17
31	30	25	L7	125	130	95	V11	219	230	165	R19	313	330	235	G15
32	31	26	L3	126	131	96	Z11	220	231	166	R23	314	331	236	C15
33	33	27	M4	127	133	97	Y12	221	233	167	P22	315	333	237	D14
34	VSS(34)	GND	a	128	VSS(134)	GND	a	222	VSS(234)	GND	a	316	VSS(334)	GND	a
35	35	-	-	129	135	-	-	223	235	-	-	317	335	-	-
36	36	28	L9	130	136	98	T11	224	236	168	R17	318	336	238	J15
37	37	29	M6	131	137	99	W12	225	237	169	P20	319	337	239	F14
38	39	-	-	132	139	-	-	226	239	-	-	320	339	-	-
39	OVDD5(40)	PWR	b	133	OVDD5(140)	PWR	b	227	OVDD5(240)	PWR	b	321	OVDD5(340)	PWR	b
40	41	30	L1	134	141	100	BB11	228	241	170	R25	322	341	240	A15
41	42	31	M8	135	142	101	U12	229	242	171	P18	323	342	241	H14
42	OVSS(43)	GND	a	136	OVSS(143)	GND	a	230	OVSS(243)	GND	a	324	OVSS(343)	GND	a
43	45	32	M2	137	145	102	AA12	231	245	172	P24	325	345	242	B14
44	46	33	M10	138	146	103	S12	232	246	173	P16	326	346	243	K14
45	47	34	N7	139	147	104	V13	233	247	174	N19	327	347	244	G13
46	48	35	N3	140	148	105	Z13	234	248	175	N23	328	348	245	C13
47	(OVDD5)50	PWR	b	141	(OVDD5)150	PWR	b	235	(OVDD5)250	PWR	b	329	(OVDD5)350	PWR	b
48	VDD(51)	-	-	142	VDD(151)	-	-	236	VDD(251)	-	-	330	VDD(351)	-	-
49	52	36	N1	143	152	106	BB13	237	252	176	N25	331	352	246	A13
50	53	37	P10	144	153	107	S14	238	253	177	M16	332	353	247	K12
51	55	38	M5	145	155	108	X13	239	255	178	N21	333	355	248	E13
52	56	39	P2	146	156	109	AA14	240	256	179	M24	334	356	249	B12
53	57	40	P8	147	157	110	U14	241	257	180	M18	335	357	250	H12

Table 4-38 H4CP178 313 OMPAC Pad to Pin Cross Reference

LEFT SIDE				BOTTOM SIDE				RIGHT SIDE				TOP SIDE			
DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE		DIE		PACKAGE	
Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball	Die Pad	I/O Cell	Bond Finger	Solder Ball
54	OVSS(58)	GND	a	148	OVSS(158)	GND	a	242	OVSS(258)	GND	a	336	OVSS(358)	GND	a
55	59	41	R1	149	159	111	BB15	243	259	181	L25	337	359	251	A11
56	61	42	P6	150	161	112	W14	244	261	182	M20	338	361	252	F12
57	OVDD5(62)	PWR	b	151	OVDD5(162)	PWR	b	245	OVDD5(262)	PWR	b	339	OVDD5(362)	PWR	b
58	63	43	R9	152	163	113	T15	246	263	183	L17	340	363	253	J11
59	64	44	P4	153	164	114	Y14	247	264	184	M22	341	364	254	D12
60	65	45	R3	154	165	115	Z15	248	265	185	L23	342	365	255	C11
61	(VDD)67	46	R7	155	(VDD)167	116	V15	249	(VDD)267	186	L19	343	(VDD)367	256	G11
62	VSS(68)	GND	a	156	VSS(168)	GND	a	250	VSS(268)	GND	a	344	VSS(368)	GND	a
63	69	47	T1	157	169	117	BB17	251	269	187	J25	345	369	257	A9
64	70	48	S8	158	170	118	U16	252	270	188	K18	346	370	258	H10
65	72	49	S2	159	172	119	AA16	253	272	189	K24	347	372	259	B10
66	73	50	T7	160	173	120	V17	254	273	190	J19	348	373	260	G9
67	OVSS(74)	GND	a	161	OVSS(174)	GND	a	255	OVSS(274)	GND	a	349	OVSS(374)	GND	a
68	(OVDD3)75	51	T3	162	(OVDD3)175	121	Z17	256	(OVDD3)275	191	J23	350	(OVDD3)375	261	C9
69	77	52	S4	163	177	122	Y16	257	277	192	K22	351	377	262	D10
70	78	53	R5	164	178	123	X15	258	278	193	L21	352	378	263	E11
71	79	54	V1	165	179	124	BB19	259	279	194	G25	353	379	264	A7
72	80	55	U2	166	180	125	AA18	260	280	195	H24	354	380	265	B8
73	81	56	S6	167	181	126	W16	261	281	196	K20	355	381	266	F10
74	82	57	T5	168	182	127	X17	262	282	197	J21	356	382	267	E9
75	84	-	-	169	184	-	-	263	284	-	-	357	384	-	-
76	OVDD5(85)	PWR	b	170	OVDD5(185)	PWR	b	264	OVDD5(285)	PWR	b	358	OVDD5(385)	PWR	b
77	86	58	X1	171	186	128	BB21	265	286	198	E25	359	386	268	A5
78	87	59	U6	172	187	129	W18	266	287	199	H20	360	387	269	F8
79	88	60	U4	173	188	130	Y18	267	288	200	H22	361	388	270	D8
80	OVSS(89)	GND	a	174	OVSS(189)	GND	a	268	OVSS(289)	GND	a	362	OVSS(389)	GND	a
81	90	61	V3	175	190	131	Z19	269	290	201	G23	363	390	271	C7
82	91	62	W2	176	191	132	AA20	270	291	202	F24	364	391	272	B6
83	92	63	V5	177	192	133	X19	271	292	203	D24	365	392	273	B4
84	93	64	W4	178	193	134	Y20	272	293	204	F22	366	393	274	D6
85	94	65	X5	179	194	135	X21	273	294	205	E21	367	394	275	C5
86	(OVSS)95	GND	a	180	(OVSS)195	GND	a	274	(OVSS)295	GND	a	368	(OVSS)395	GND	a
87	96	-	-	181	196	-	-	275	296	-	-	369	396	-	-
88	97	66	W6	182	197	136	W20	276	297	206	G21	370	397	276	E7
89	98	67	Z1	183	198	137	BB23	277	298	207	C25	371	398	277	A3
90	99	68	X3	184	199	138	Z21	278	299	208	E23	372	399	278	A1
91	100	69	Y2	185	200	139	AA22	279	300	209	A25	373	400	279	C3
92	OVDD3	70	AA2	186	OVDD3	140	AA24	280	OVDD3	210	B24	374	OVDD3	280	E5
93	OVDD5	PWR	b	187	OVDD5	PWR	b	281	OVDD5	PWR	b	375	OVDD5	PWR	b
94	OVSS	GND	a	188	OVSS	GND	a	282	OVSS	GND	a	376	OVSS	GND	a

NOTES:

1. Die Pad/IO-Cell numbers start at top of LEFT side and increment counter-clockwise.
2. Pkg Pin and Bond FIngers numbers start at top of LEFT side and increment counter-clockwise.
3. VSS, VDD, OVSS, OVDD3, & OVDD5 indicates fixed power and ground pads on the die (Array) for probe test.
4. OVSS & OVDD5 in () are power and ground for Final Test and are Package dependent.
5. The following is a cross reference of package dependent Power and Ground Pkg Pin numbers:
PWR, a = J13, K10, K16, L11, L13, L15, M12, M14, N9, N11, N13, N15, N17, P12, P14, R11, R13, R15, S16, T13
GND, b = G7, G19, H8, H18, J9, J17, S10, T9, T17, U8, U18, V7, V19
6. Only OVDD5 is connected to package PWR pins. VDD must be supplied seperately through I/O package pins.

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REV. 1.0 5/11/94 JEB

Table 4-39 H4CP178P1 Analog PLL Option 1

BOTTOM SIDE	
DIE	
Die Pad	I/O Cell
95	VSS
96	VDD
97	AVSS
98	AVDD
99	101
100	102
101	103
102	104
103	105
104	106
105	107
106	109
107	110
108	111
109	113
110	OVSS(114)
111	115
112	116
113	117
114	OVDD5(118)
115	119
116	120
117	121
118	122
119	123
120	124
121	125
122	127
123	OVSS(128)
124	129
125	130
126	131
127	133
128	VSS(134)
129	135
130	136
131	137
132	139
133	OVDD5(140)
134	141
135	142
136	OVSS(143)
137	145
138	146
139	147
140	148
141	150
142	VDD(151)
143	152
144	153
145	155

Table 4-39 H4CP178P1 Analog PLL Option 1

BOTTOM SIDE	
DIE	
Die Pad	I/O Cell
146	156
147	157
148	OVSS(158)
149	159
150	161
151	OVDD5(162)
152	163
153	164
154	165
155	167
156	VSS(168)
157	169
158	170
159	172
160	173
161	OVSS(174)
162	175
163	177
164	178
165	179
166	180
167	181
168	182
169	184
170	OVDD5(185)
171	186
172	187
173	188
174	OVSS(189)
175	190
176	191
177	192
178	193
179	194
180	195
181	196
182	197
183	198
184	199
185	200
186	OVDD3
187	OVDD5
188	OVSS

Note: This table replaces the BOTTOM side of each pad to pin table for each array/package combination when Analog PLL option 1 is used in the H4CP178 array.

Table 4-40 H4CP178P2 Analog PLL Option 2

BOTTOM SIDE		TOP SIDE	
DIE		DIE	
Die Pad	I/O Cell	Die Pad	I/O Cell
95	VSS	283	VSS
96	VDD	284	VDD
97	AVSS	285	AVSS
98	AVDD	286	AVDD
99	101	287	301
100	102	288	302
101	103	289	303
102	104	290	304
103	105	291	305
104	106	292	306
105	107	293	307
106	109	294	309
107	110	295	310
108	111	296	311
109	113	297	313
110	OVSS(114)	298	OVSS(314)
111	115	299	315
112	116	300	316
113	117	301	317
114	OVDD5(118)	302	OVDD5(318)
115	119	303	319
116	120	304	320
117	121	305	321
118	122	306	322
119	123	307	323
120	124	308	324
121	125	309	325
122	127	310	327
123	OVSS(128)	311	OVSS(328)
124	129	312	329
125	130	313	330
126	131	314	331
127	133	315	333
128	VSS(134)	316	VSS(334)
129	135	317	335
130	136	318	336
131	137	319	337
132	139	320	339
133	OVDD5(140)	321	OVDD5(340)
134	141	322	341
135	142	323	342
136	OVSS(143)	324	OVSS(343)
137	145	325	345
138	146	326	346
139	147	327	347
140	148	328	348
141	150	329	350
142	VDD(151)	330	VDD(351)
143	152	331	352
144	153	332	353
145	155	333	355

Table 4-40 H4CP178P2 Analog PLL Option 2

BOTTOM SIDE		TOP SIDE	
DIE		DIE	
Die Pad	I/O Cell	Die Pad	I/O Cell
146	156	334	356
147	157	335	357
148	OVSS(158)	336	OVSS(358)
149	159	337	359
150	161	338	361
151	OVDD5(162)	339	OVDD5(362)
152	163	340	363
153	164	341	364
154	165	342	365
155	167	343	367
156	VSS(168)	344	VSS(368)
157	169	345	369
158	170	346	370
159	172	347	372
160	173	348	373
161	OVSS(174)	349	OVSS(374)
162	175	350	375
163	177	351	377
164	178	352	378
165	179	353	379
166	180	354	380
167	181	355	381
168	182	356	382
169	184	357	384
170	OVDD5(185)	358	OVDD5(385)
171	186	359	386
172	187	360	387
173	188	361	388
174	OVSS(189)	362	OVSS(389)
175	190	363	390
176	191	364	391
177	192	365	392
178	193	366	393
179	194	367	394
180	195	368	395
181	196	369	396
182	197	370	397
183	198	371	398
184	199	372	399
185	200	373	400
186	OVDD3	374	OVDD3
187	OVDD5	375	OVDD5
188	OVSS	376	OVSS

Note: This table replaces the BOTTOM and the TOP side of each pad to pin table for each array/package combination when Analog PLL option 2 is used in the H4CP178 array.

4.7 MECHANICAL DATA

Note: Where formal case outlines are not available, preliminary drawings are shown.

4.8 Geometric Characteristics and Symbols

The following is a list of common characters, text, and symbols used in Motorola Case Outlines:

MECHANICAL DRAWINGS INCLUDED

- **QFP**-Excised from MCR
  128, 160, 208, 240 Pin
- **MicroCool** QFP -Excised from MCR
  160, 208 Pin
- **OMPAC**
  169, 225, 313 Pin
- **MCR**
  AB Ring


Flatness

Straightness


Circularity (Roundness)


Cylindricity


Perpendicularity (Squareness)


Angularity


Parallelism


Profile of a Surface


Profile of a Line


Total Runout


Circular Runout


Position


Concentricity


Symmetry

BSC BASIC -Untoleranced dimensions locating true position

Ref. A dimension which is obtained from other dimensions and their tolerances.


Maximum Material Condition MMC


Regardless of Feature Size RFS

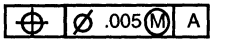

Least Material Condition LMC


Projected Tolerance Zone


Diametrical (Cylindrical) Tol. Zone or Feature

Basic, or Exact, Dimension

Datum Feature Symbol

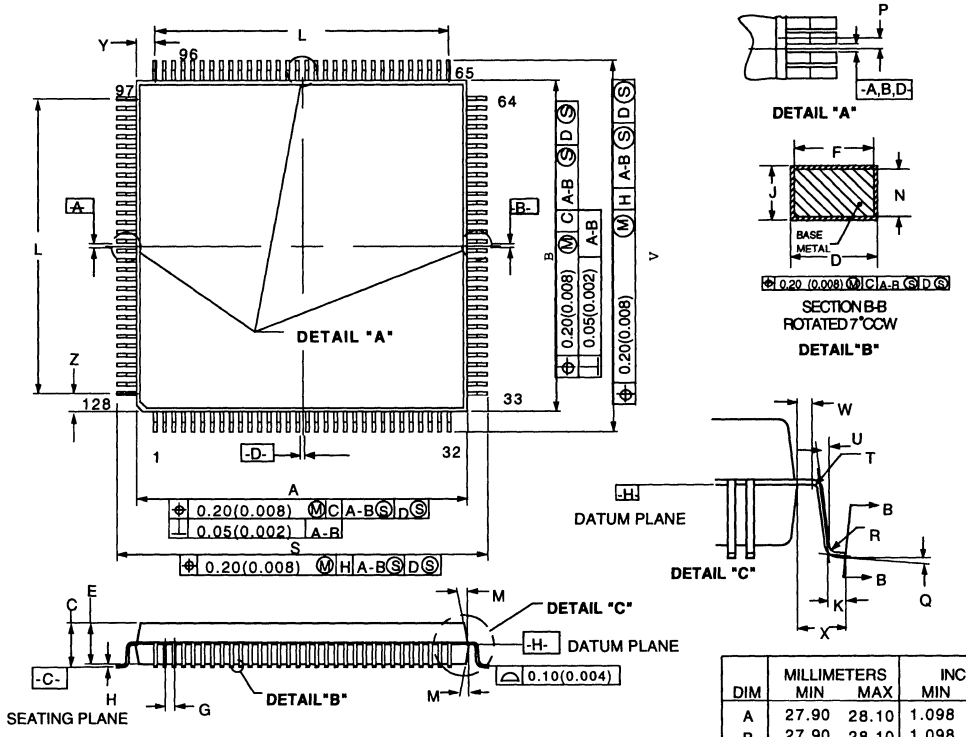


Feature Control Frame

Datum Target

128-PIN PACKAGES

PLASTIC QUAD FLAT PACK
CASE 862A-01
(Excised from the AB MCR, see page 4-37)



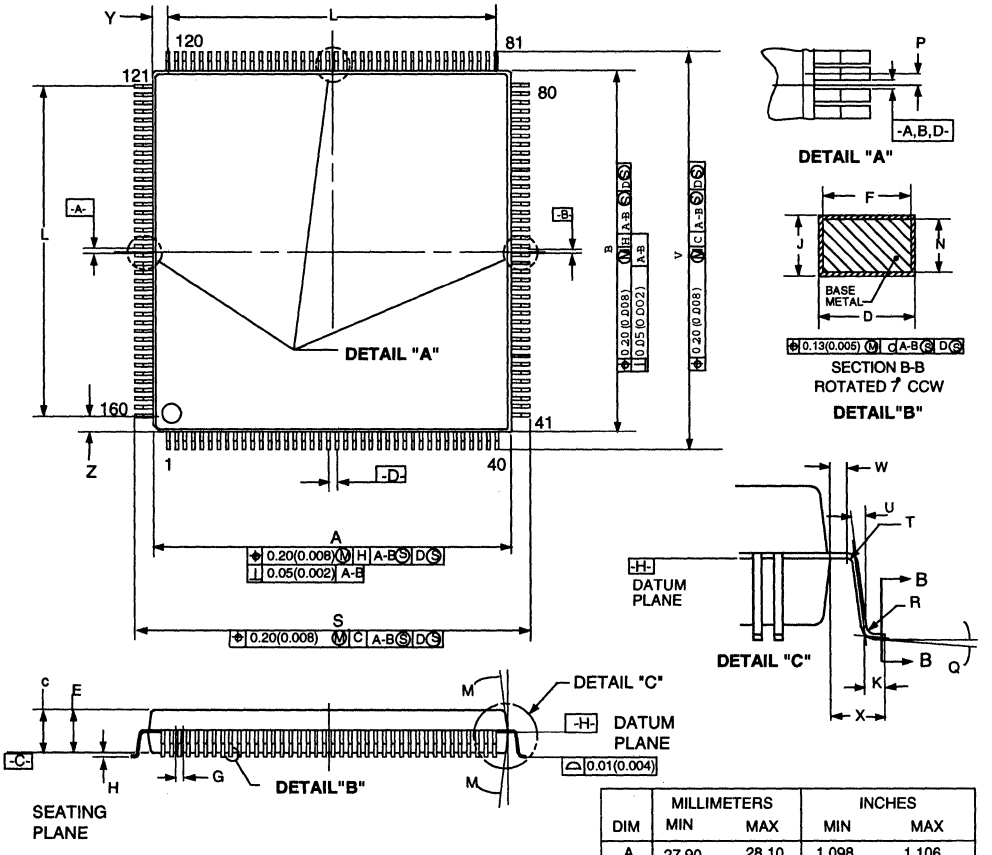
DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.45	3.85	0.136	0.152
D	0.30	0.45	0.012	0.018
E	3.17	3.67	0.125	0.144
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.032 BSC	
H	0.25	0.35	0.010	0.014
J	0.13	0.23	0.005	0.009
K	0.75	0.92	0.030	0.036
L	24.80 REF		0.976 REF	
M	5°	16°	5°	16°
N	0.13	0.17	0.005	0.007
P	0.40 BSC		0.016 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.10	31.37	1.224	1.235
T	0.13	---	0.005	---
U	0°	---	0°	---
V	31.10	31.37	1.224	1.235
W	0.40	---	0.016	---
X	1.60 REF		0.063 REF	
Y	1.60 REF		0.063 REF	
Z	1.60 REF		0.063 REF	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25(.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08(.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

160-PIN PACKAGES

PLASTIC QUAD FLAT PACK
CASE 864A-01
(Excised from the AB MCR, see page 4-37)



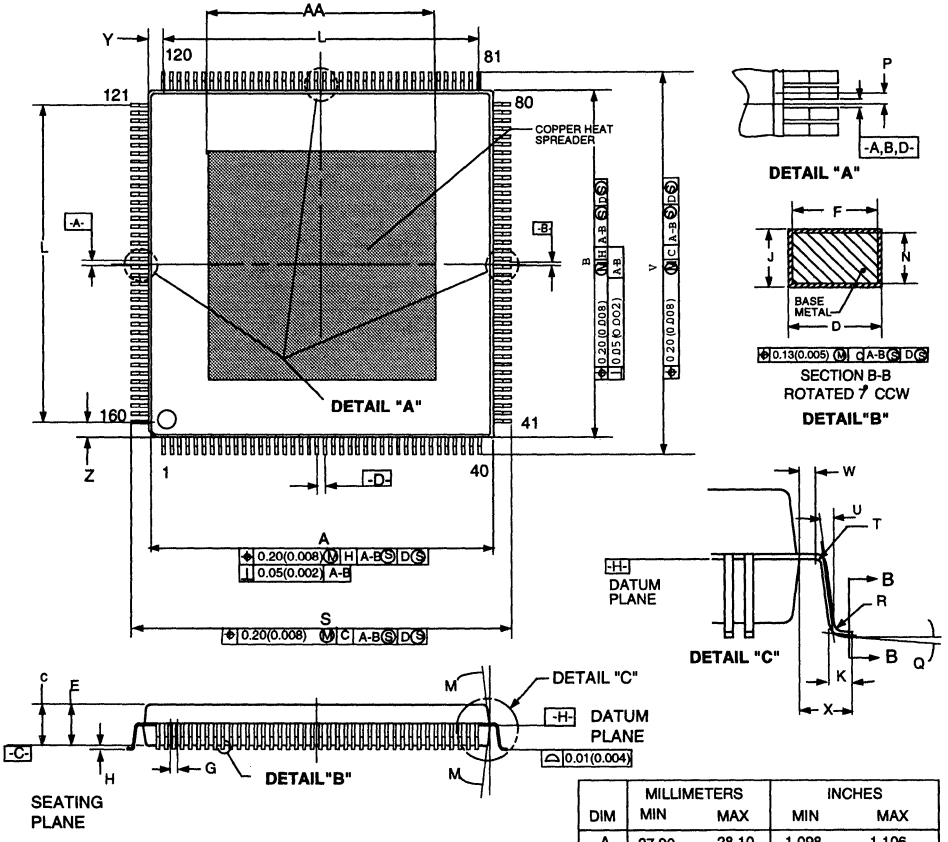
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.35	3.85	0.132	0.152
D	0.22	0.33	0.009	0.013
E	3.20	3.50	0.126	0.138
F	0.22	0.38	0.009	0.015
G	0.650 BSC		0.0256 BSC	
H	0.25	0.35	0.010	0.012
J	0.11	0.23	0.004	0.009
K	0.70	0.90	0.028	0.035
L	25.35 REF		0.998 REF	
M	5°	16°	5°	16°
N	0.11	0.19	0.004	0.007
P	0.325 BSC		0.0130 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.00	31.40	1.220	1.236
T	0.13	---	0.005	---
U	0°	---	0°	---
V	31.00	31.40	1.220	1.236
W	0.40	---	0.016	---
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINSIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-. PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBARPROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

160-PIN PACKAGES

MicroCool QUAD FLAT PACK
CASE 864D-02
(Excised from the AB MCR, see page 4-37)



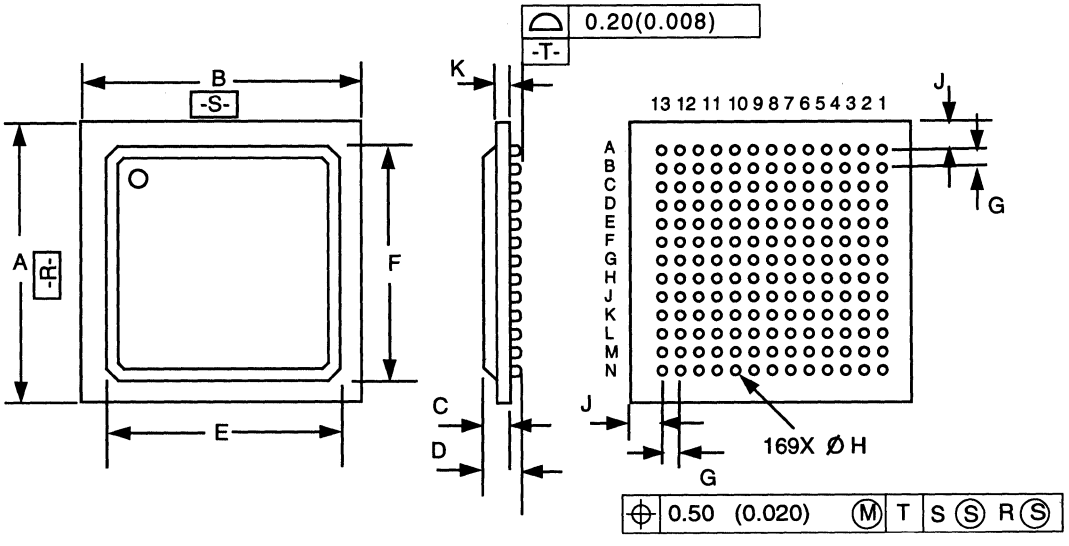
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.45	3.85	0.136	0.152
D	0.22	0.38	0.009	0.015
E	3.20	3.50	0.126	0.138
F	0.22	0.33	0.009	0.013
G	0.650 BSC		0.0256 BSC	
H	0.25	0.35	0.010	0.012
J	0.13	0.23	0.005	0.009
K	0.75	0.95	0.030	0.037
L	25.35 REF		0.998 REF	
M	5°	16°	5°	16°
N	0.13	0.197	0.005	0.007
P	0.325 BSC		0.0130 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	31.10	31.37	1.224	1.235
T	0.13	---	0.005	---
U	0°	---	0°	---
V	31.10	31.37	1.224	1.235
W	0.40	---	0.016	---
X	1.60 REF		0.063 REF	
Y	1.33 REF		0.052 REF	
Z	1.33 REF		0.052 REF	
AA	16.30	18.30	0.642	0.720

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINSIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-. PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBARPROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

169-PIN PACKAGES

OMPAC
CASE 938
GTPAC (used for prototypes only)
CASE 971-01



DIMENSIONS for OMPAC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.90	23.10	0 .902	0.909
B	22.90	23.10	0 .902	0.909
C	1.33	1.73	0.0523	0.0681
D	1.83	2.43	0.0720	0.0956
E	19.30	19.70	0.7598	0.7755
F	19.30	19.70	0.7598	0.7755
G	1.50 BSC		0.0590 BSC	
H	0.690	0.810	0.0271	0.0318
J	2.400	2.600	0.094	0.102
K	0.310	0.410	0.012	0.016

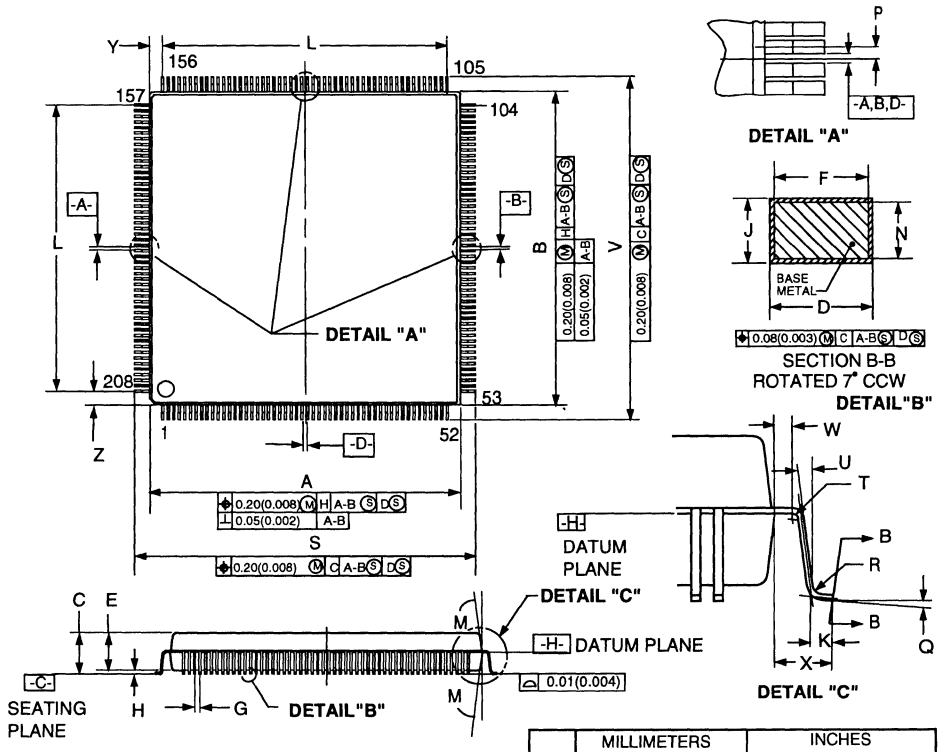
DIMENSIONS for GTPAC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.90	23.10	0 .902	0.909
B	22.90	23.10	0 .902	0.909
C	1.526	2.134	0.060	0.084
D	2.026	2.834	0.080	0.112
E	15.300	19.300	0.602	0.760
F	15.300	19.300	0.602	0.760
G	1.50 BSC		0.0590 BSC	
H	0.690	0.810	0.0271	0.0318
J	2.400	2.600	0.094	0.102
K	0.510	0.610	0.020	0.024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: MILLIMETER

208-PIN PACKAGES

PLASTIC QUAD FLAT PACK
CASE 872A-01
1.6 FOOT LENGTH
(Excised from the AB MCR see page 4-37)



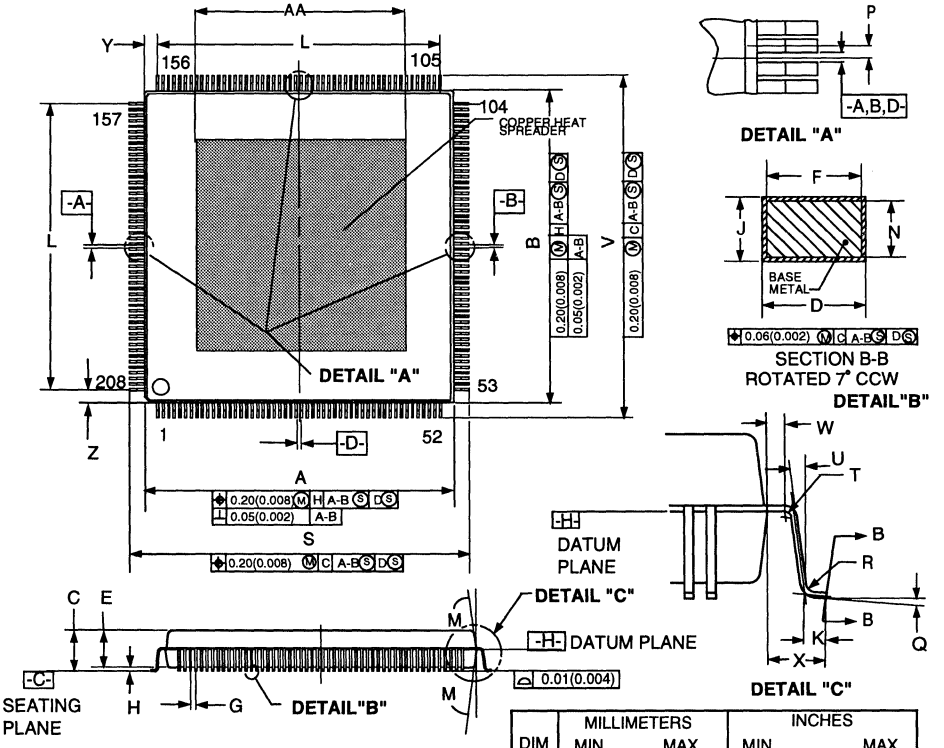
DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.45	4.10	0.136	0.161
D	0.17	0.27	0.007	0.011
E	3.20	3.60	0.126	0.142
F	0.17	0.23	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.25	—	0.010	—
J	0.09	0.20	0.003	0.008
K	0.75	0.95	0.030	0.037
L	25.5 REF		1.004 REF	
M	5°	16°	5°	16°
N	0.09	0.16	0.003	0.006
P	0.250 BSC		0.010 BSC	
Q	0°	7°	0°	7°
R	0.13	0.25	0.005	0.010
S	31.00	31.40	1.220	1.236
T	0.13	---	0.005	---
U	0°	---	0°	---
V	31.00	31.40	1.220	1.236
W	0.20	---	0.008	---
X	1.60 REF		0.063 REF	
Y	1.25 REF		0.049 REF	
Z	1.25 REF		0.049 REF	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINSIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.38 (0.015).

208-PIN PACKAGES

PLASTIC QUAD FLAT PACK MicroCool™
CASE 872G-01
1.6 FOOT LENGTH
(Excised from the AB MCR see page 4-37)



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.90	28.10	1.098	1.106
B	27.90	28.10	1.098	1.106
C	3.45	4.10	0.136	0.161
D	0.17	0.27	0.007	0.011
E	3.20	3.60	0.126	0.142
F	0.17	0.23	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.25	----	0.010	----
J	0.09	0.20	0.003	0.008
K	0.75	0.95	0.030	0.037
L	25.5 REF		1.004 REF	
M	5°	16°	5°	16°
N	0.09	0.18	0.003	0.007
P	0.250 BSC		0.010 BSC	
Q	0°	7°	0°	7°
R	0.13	0.25	0.005	0.010
S	31.00	31.40	1.220	1.236
T	0.13	---	0.005	---
U	0°	---	0°	---
V	31.00	31.40	1.220	1.236
W	0.20	---	0.008	---
X	1.60 REF		0.063 REF	
Y	1.25 REF		0.049 REF	
Z	1.25 REF		0.049 REF	
AA	16.80	18.80	0.661	0.740

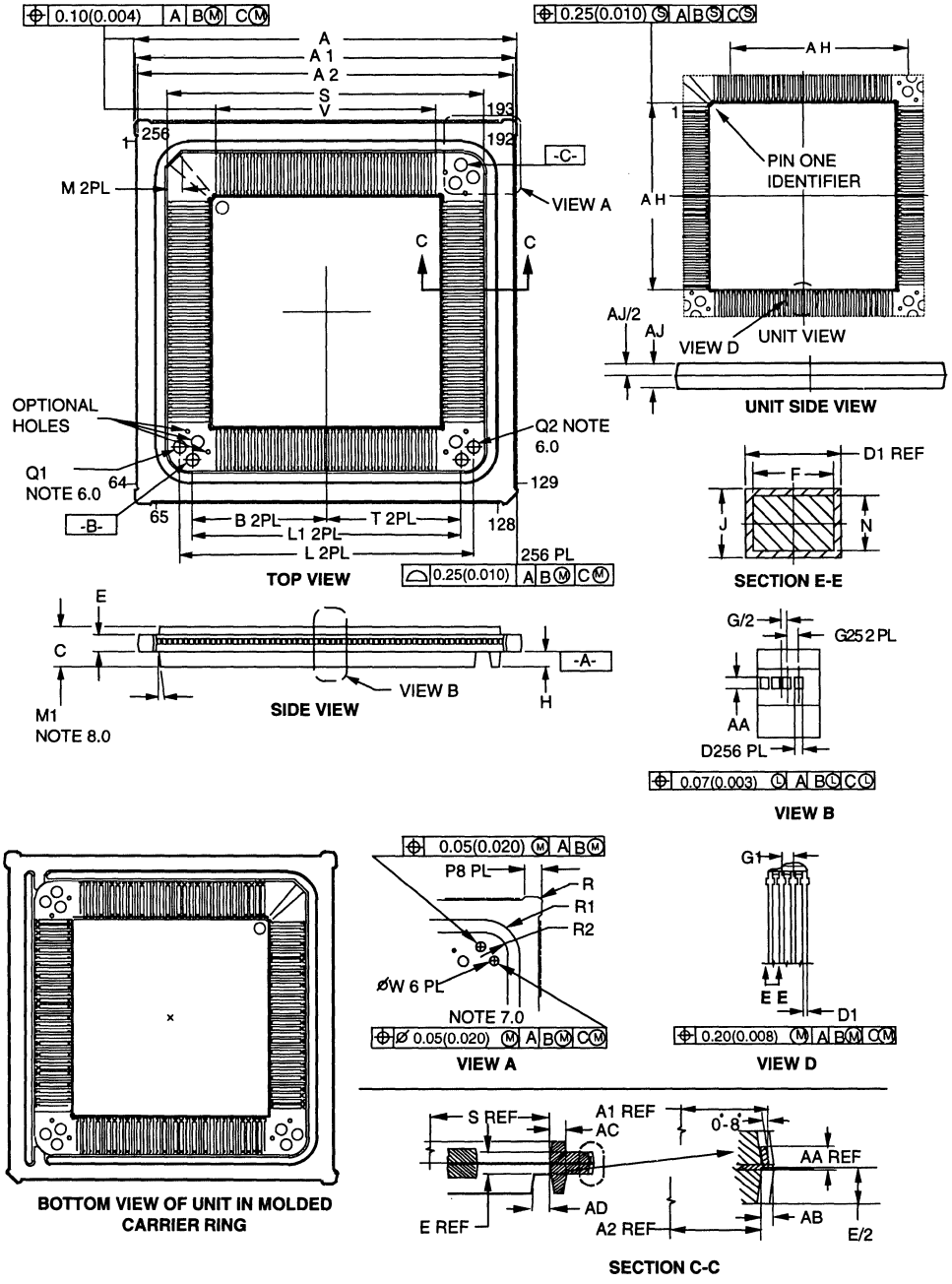
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINSIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35 (0.014).

MOLDED CARRIER RING

SIZE AB: FOUR UNITS PER STRIP

CASE OUTLINES 884(120 pin), 885(128 pin), 887(160 pin),888-01(208 pin)



MOLDED CARRIER RING

SIZE AB: (Continued)

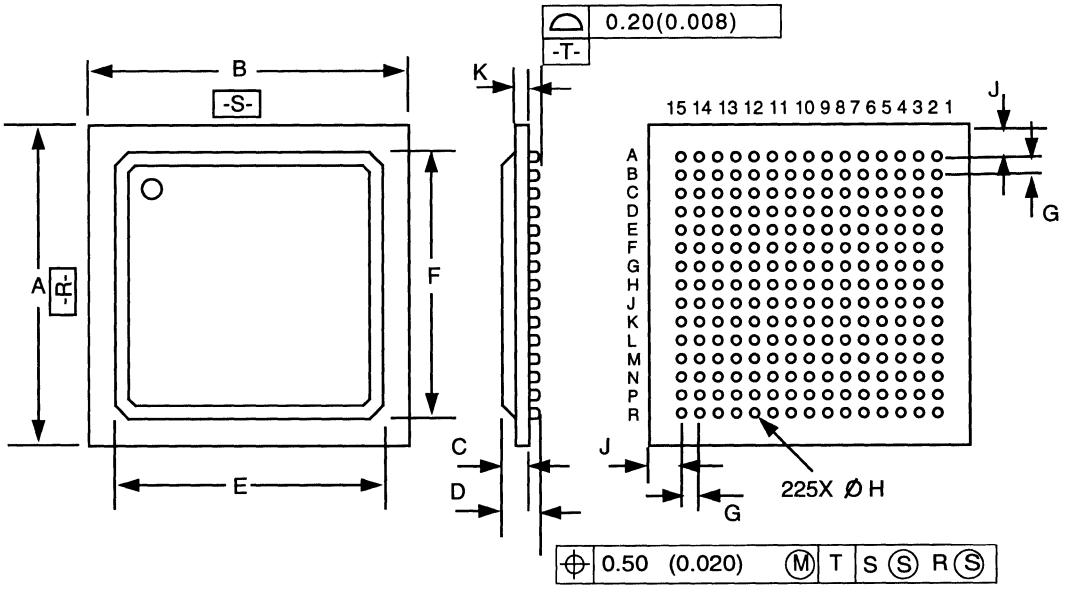
NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. A, DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.20(0.008) PER SIDE.
4. A AND S DIMENSIONS INCLUDE MOLD MISMATCH, AND ARE MEASURED AT THE PARTING LINE.
5. UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTERLINES.
6. B AND C DATUM HOLES ARE TO BE USED FOR TRIM, FORM AND EXCISE OF THE MOLDED PACKAGE ONLY. HOLES Q1 AND Q2 ARE TO BE USED FOR ELECTRICAL TESTING ONLY.
7. NON-DATUM HOLES ONLY.
8. APPLIES TO RING AND PACKAGE FEATURES.

	MILLIMETERS		INCHES			MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	45.87	46.13	1.806	1.816	M	1.30	2.30	0.051	0.091
A1	45.70 BSC		1.799 BSC		M1	8°MAX		8°MAX	
A2	45.17	45.43	1.778	1.789	N	0.13	0.17	0.005	0.007
B	16.10 BSC		0.634 BSC		P	1.77	2.03	0.070	0.080
C	4.70	4.90	0.185	0.193	R	0.40	0.60	0.016	0.024
D	0.40	0.50	0.016	0.020	R1	3.50	4.50	0.138	0.177
D1	0.22	0.38	0.009	0.015	R2	2.00	3.00	0.079	0.118
E	1.90	2.10	0.075	0.083	S	37.87	38.13	1.491	1.501
F	0.22	0.33	0.009	0.013	T	16.10 BSC		0.634 BSC	
G	0.65 BSC		0.026 BSC		V	26.30	26.40	1.035	1.039
G1	0.65 BSC		0.026 BSC		W	1.45	1.55	0.057	0.061
H	1.70	1.90	0.067	0.075	AA	0.45	0.85	0.018	0.033
J	0.13	0.23	0.005	0.009	AB	0.30	0.60	0.012	0.024
L	32.20 BSC		1.268 BSC		AC	1.37	1.63	0.054	0.064
L1	35.20 BSC		1.386 BSC		AD	1.37	1.63	0.054	0.064
					AH	27.90	28.10	1.098	1.106
					AJ	3.20	3.40	0.126	0.134

225-PIN PACKAGES

OMPAC
CASE 938A
GTPAC (used for prototypes only)
CASE 970-01



DIMENSIONS for OMPAC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26.90	27.10	1.0590	1.0669
B	26.90	27.10	1.0590	1.0669
C	1.330	1.730	0.0523	0.0681
D	1.830	2.430	0.072	0.956
E	23.80	24.20	0.9370	0.9527
F	23.80	24.20	0.9370	0.9527
G	1.500 BSC		0.590 BSC	
H	0.690	0.810	0.0271	0.0318
J	2.900	3.100	0.114	0.122
K	0.310	0.410	0.012	0.016

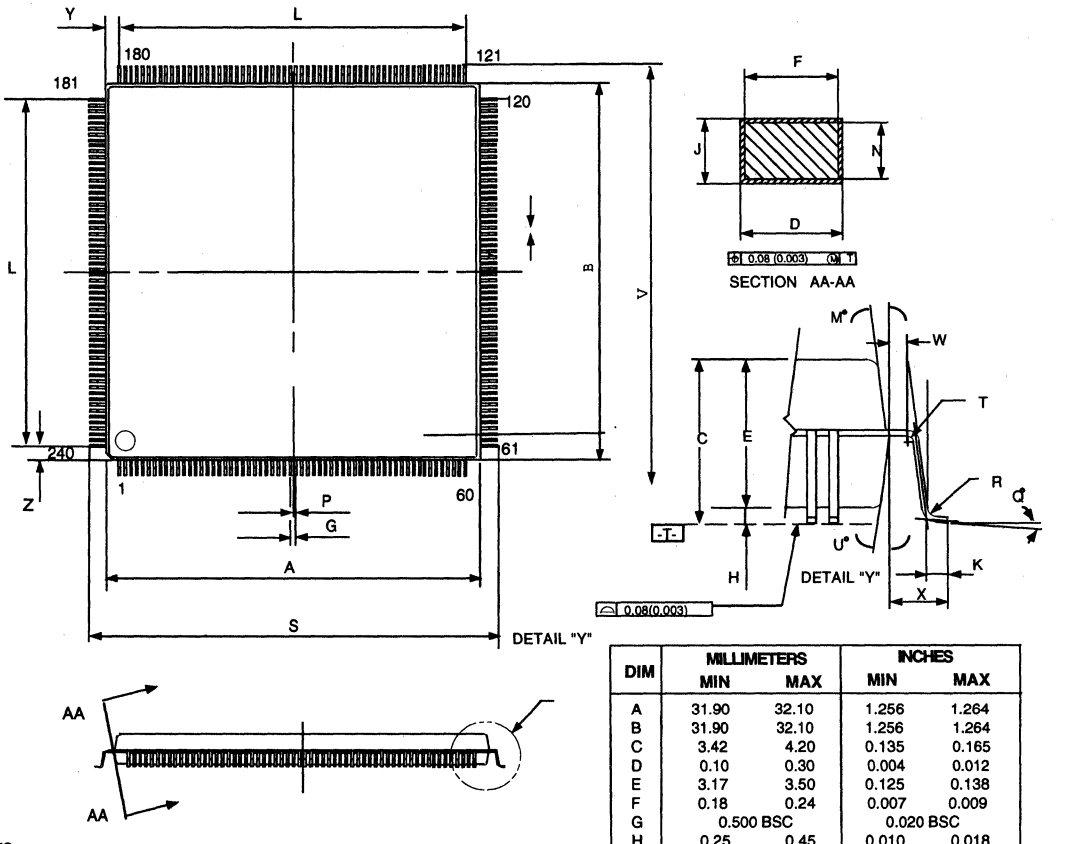
DIMENSIONS for GTPAC

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	26.90	27.10	1.0590	1.0669
B	26.90	27.10	1.0590	1.0669
C	1.526	2.134	0.060	0.084
D	2.026	2.834	0.080	0.112
E	17.780	22.860	0.700	0.900
F	17.780	22.860	0.700	0.900
G	1.500 BSC		0.590 BSC	
H	0.690	0.810	0.0271	0.0318
J	2.900	3.100	0.114	0.122
K	0.510	0.610	0.020	0.024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: MILLIMETER

240-PIN PACKAGES

PLASTIC QUAD FLAT PACK
CASE 961-01
Free Leaded (not build in MCR)



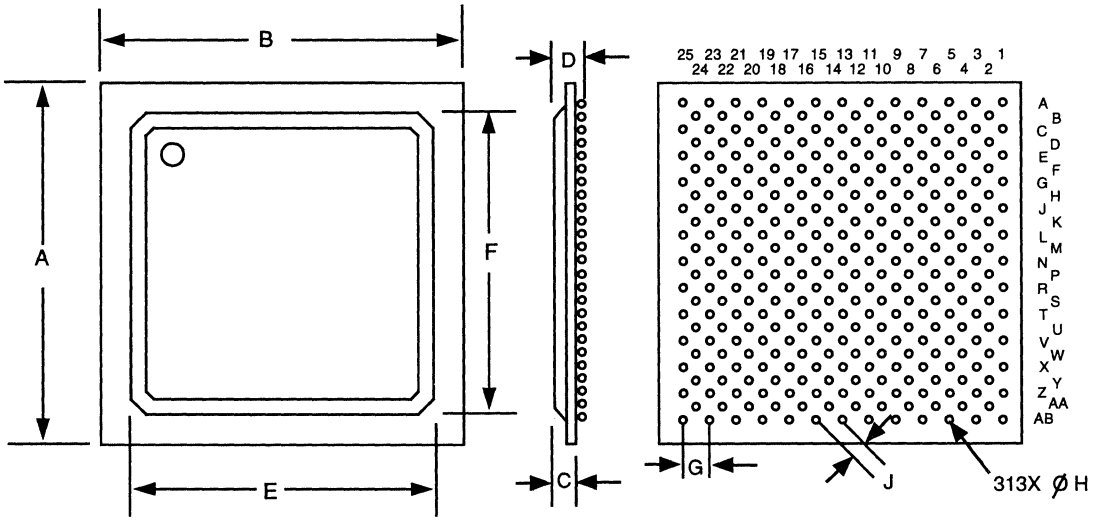
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.38 (O.015).
6. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.00030).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.90	32.10	1.256	1.264
B	31.90	32.10	1.256	1.264
C	3.42	4.20	0.135	0.165
D	0.10	0.30	0.004	0.012
E	3.17	3.50	0.125	0.138
F	0.18	0.24	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.25	0.45	0.010	0.018
J	0.09	0.20	0.003	0.008
K	0.35	0.65	0.014	0.026
L	25.5 REF		1.004 REF	
M	5°	16°	5°	16°
N	0.11	0.14	0.004	0.006
P	0.250 BSC		0.010 BSC	
Q	0°	10°	0°	10°
R	0.13	0.30	0.005	0.012
S	34.35	34.85	1.352	1.372
T	0.13	---	0.05	---
U	0°	---	0°	---
V	34.35	34.85	1.352	1.372
W	0.40	---	0.016	---
X	1.30 REF		0.051 REF	
Y	1.25 REF		0.049 REF	

313-PIN PACKAGES

OMPAC
(Preliminary Drawing)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	34.90	35.10	1.3740	1.3819
B	34.90	35.10	1.3740	1.3819
C	1.53	1.93	0.0602	0.076
D	2.03	2.63	0.0799	0.1035
E	29.80	30.20	1.1732	1.1890
F	29.80	30.20	1.1732	1.1890
G	2.54 BSC		0.100 BSC	
H	0.690	0.810	0.0271	0.0318
J	1.8 BSC		0.707 BSC	

MACRO NAMING CONVENTIONS 5

5 MACRO NAMING CONVENTIONS

SECTION 5. MACRO NAMING CONVENTIONS

The naming convention for the Motorola H4CPlus Macrocell Array Series is the same as that used for Motorola's H4C and 62A Series Macrocell Arrays.

Basic Gates:

Begin with a descriptive prefix usually followed by the number of inputs of the gates. A list of the prefixes is shown below:

NAN - NAND gate
NOR - NOR gate
AND - AND gate
OR - OR gate
EXOR - Exclusive OR gate
EXNOR - Exclusive NOR gate
AOI - AND/OR/Invert gate
OAI - OR/AND/Invert gate
ANDOI - AND + NOR into a NOR
ONDAI - OR + NAND into a NAND
MAJ - Majority
TBUF - "3-state" buffer
INVT - Inverting 3-state buffer
DS - Schmitt trigger

Suffix Options:

 # - Refers to the number of inputs
H - High drive (usually 2X drive Output)
B - Balanced drive
C - Complementary outputs

Buffers/Inverters:

Use the same convention as for Basic Gates with the exception that the (#) number refers to the number of devices in parallel on the output or X# Drive. A list of the prefixes is shown below:

INV - Inverter
BUF - Non-inverting buffer

Suffix Options:

 # - X# drive
B - Balanced drive
C - Complementary outputs
X - Uses an Output buffer from an I/O site
P - Uses an Output buffer from a Power/GND site

Flip-Flops:

Begin with the type followed by a number of different options which explain the functionality of the flip flop.

DFF - D type flip-flop
D - Used as an abbreviation of DFF if the macro name becomes too long.
JKFF - JK type flip-flop
JK - Used as an abbreviation of JKFF if the macro name becomes too long.
TFF - Toggle type flip-flop

Suffix Options:

R - Reset
S - Set
L - LSSD or scan type Input
P - Positive-edge clocked
T - 3-state Output
H - High drive (usually 2X drive Output)
A or B - These are used when different versions of the same function (such as the DFFRTPA or the JKFFRSPB) already exist in other technologies but have different states when both Set and Reset are taken low at the same time.

Latches:

Names have many of the same suffixes as flip-flops with the following differences:

LAT - Latch
CCND - Cross-coupled NAND latch
L1LSSD - L1 type LSSD latch
SRLSSD1 - SR type LSSD1 latch

Suffix Options:

N - Negative gate latched
P - Positive gate latched
R - Reset
S - Set
G - Common gated input
H - High drive (usually 2X drive Output)

Inputs:

Begin with an I which is followed by a C (CMOS), T (TTL), S (CMOS level Schmitt Trigger), or TS (TTL level Schmitt Trigger) which indicates switching voltage levels. An I or N is placed in the name which indicates whether the input is Inverting (I)or Non-Inverting (N).

Prefix Options:

B - Bidirectional version (same as above without pad)

Suffix Options:

H - Clock buffer (High drive)

Example:

ICN - Input/CMOS/Non-Inverting
BICN - Bidirectional version of ICN (without the pad)
ICNH - ICN with High drive (uses output buffer transistors)

5

Outputs:

The base begins with an O which is followed by an I (Inverting) or a N (Non-Inverting). The third alphanumeric indicates the approximate source & sink current drive in mA.

NOTE:
The number following ON is approximately the number of mA that buffer can source and sink and still maintain the proper threshold voltages across commercial worst case temperature, voltage and process. The actual current in mA is generally significantly higher. For an exact breakdown of typical currents at different temperatures and voltages please refer to the DC Electrical Specifications in Section 8.

Prefix Options:

B - Bidirectional version (same as above without pad)

Suffix Options:

T - 3-state output
OD - Open-Drain output

Example:

ON4 - Output/Non-inverting/4 mA drive
ON4T - Output/Non-inverting/4 mA drive/ 3-state Output
BON4T - Bidirectional version of ON4T (with BIC port)
ON4OD - Output/Non-inverting/4 mA drive /Open-Drain Output

SPECIAL Input and Outputs:

CMTL, GTL, PCI and PECL I/O's have the same naming convention's as standard inputs and outputs. An M (CMTL), G (GTL), PC (PCI), or a P (PECL) is added to the name to identify its special function.

JTAG macros end with a J and follow all of the standard naming conventions.

Analog Phase Look Loop:

All APLL macros begin with AP.

Suffix Options:

1 - CMOS PLL Type 1
2 - CMOS PLL Type 2
D1 - PECL PLL Differential Type 1
D2 - PECL PLL Differential Type 2

System/Core I/O Voltage definition and naming convention:

5/5 V = 5 Volt System and 5 Volt Core (standard naming convention)
e.g.: ICN, ON2

5/3.3 V = 5 Volt System and 3.3 Volt Core (standard name with an **X**)
e.g.: IC**X**N, ON**X**2

3.3/5 V = 3.3 Volt System and 5 Volt Core (standard name with **LX**)
e.g.: I**LX**N, ON**LX**2T

3.3/3.3 V = 3.3 Volt System and 3.3 Volt Core (standard name with an **L**)
e.g.: I**L**CN, ON**L**2

Resistors:

Begin with a PD (Pull-Down) or PU (Pull-Up)

Suffix Options:

H - Higher current pull
L - Lower current pull

QUICK REFERENCE GUIDE

6

6 QUICK REFERENCE GUIDE

SECTION 6. MACRO DESCRIPTIONS AND QUICK REFERENCE GUIDE

The following tables detail the elements which make up the H4CPlus Series library. The elements are organized into the following categories: Internal Macrocells, Memory Blocks (RAM Macrocells), Peripheral Macros (Input/Output Macrocells) and JTAG Macros.

S = Sections Used (#of Input/Output drivers used for function).

Gates = equivalent gate count (Internal Macrocells)
System/Core I/O Voltage definition:
5/5 V = 5 Volt System and 5 Volt Core
5/3.3 V = 5 Volt System and 3.3 Volt Core
3.3/5 V = 3.3 Volt System and 5 Volt Core
3.3/3.3 V = 3.3 Volt System and 3.3 Volt Core

INTERNAL MACROS

#	INTERNAL MACROS		Gates	Page #
		AND GATES		
1	AND2	2-Input AND Gate	2	7-195
2	AND2H	2-Input AND Gate, 2X Drive	2	7-195
3	AND3	3-Input AND Gate	2	7-196
4	AND3H	3-Input AND Gate, 2X Drive	3	7-196
5	AND4	4-Input AND Gate	3	7-197
6	AND4H	4-Input AND Gate, 2X Drive	3	7-197
7	AND8H	8-Input AND Gate, 2X Drive	6	7-198
		NAND GATES		
1	NAN2	2-Input NAND Gate	1	7-305
2	NAN2H	2-Input NAND Gate, 2X Drive	2	7-305
3	NAN2B	2-Input NAND Gate, Balanced	2	7-305
4	NAN3	3-Input NAND Gate	2	7-307
5	NAN3H	3-Input NAND Gate, 2X Drive	3	7-307
6	NAN4	4-Input NAND Gate	2	7-308
7	NAN4H	4-Input NAND Gate, 2X Drive	4	7-308
8	NAN5	5-Input NAND Gate	4	7-310
9	NAN5H	5-Input NAND Gate, 2X Drive	5	7-310
10	NAN6CH	6-Input NAND Gate, 2X Drive, 1X Complementary Output	6	7-312
11	NAN8H	8-Input NAND Gate, 2X Drive	7	7-313
		OR GATES		
1	OR2	2-Input OR Gate	2	7-330
2	OR2H	2-Input OR Gate, 2X Drive	2	7-330
3	OR3	3-Input OR Gate	2	7-331
4	OR3H	3-Input OR Gate, 2X Drive	3	7-331
5	OR4	4-Input OR Gate	3	7-332
6	OR4H	4-Input OR Gate, 2X Drive	3	7-332
7	OR8H	8-Input OR Gate, 2X Drive	8	7-333
		NOR GATES		
1	NOR2	2-Input NOR Gate	1	7-314
2	NOR2H	2-Input NOR Gate, 2X Drive	2	7-314
3	NOR2B	2-Input NOR Gate, Balanced	2	7-314
4	NOR3	3-Input NOR Gate	2	7-316
5	NOR3H	3-Input NOR Gate, 2X Drive	4	7-316
6	NOR4	4-Input NOR Gate	4	7-317
7	NOR4H	4-Input NOR Gate, 2X Drive	4	7-317
8	NOR5	5-Input NOR Gate	4	7-319
9	NOR5H	5-Input NOR Gate, 2X Drive	5	7-319
10	NOR6CH	6-Input NOR Gate, 2X Drive, 1X Complementary Output	6	7-321
11	NOR8H	8-Input NOR Gate, 2X Drive	7	7-323

INTERNAL MACROS

#	INTERNAL MACROS		Gates	Page #
		EXCLUSIVE OR & EXCLUSIVE NOR GATES		
1	EXNORA	2-Input Ex NOR, Unbuffered Inputs	3	7-259
2	EXNOR3H	3-Input Exclusive NOR, 2X Drive	8	7-260
3	EXORA	2-Input Exclusive OR, Unbuffered Inputs	3	7-261
4	EXOR3H	3-Input Exclusive OR, 2X Drive	8	7-262
5	EXOR4H	4-Input Exclusive OR, 2X Drive	10	7-263
		AND/NOR, AND/OR, OR/NAND, & OR/AND GATES		
1	ANDOI22	2-Input AND + 2-Input NOR, into 2-Input NOR	3	7-199
2	ANDOI22H	2-Input AND+2-Input NOR,→2-Input NOR 2X Drive	4	7-199
3	AO21H	2-Input AND, 1-Wide,→2-Input OR, 2X	3	7-201
4	AO22H	2-Input AND, 2-Wide, into 2-Input OR, 2X	3	7-202
5	AO321H	3,2,1-input AND-OR Gate, 2X Drive	5	7-203
6	AO4321H	4,3,2,1-input AND-OR Gate, 2X Drive	8	7-204
7	AOI21	2-Input AND, 1-Wide, into 2-input NOR	2	7-206
8	AOI21H	2-Input AND, 1-Wide, into 2-input NOR, 2X	3	7-206
9	AOI211	2-Input AND, 1-Wide, into 3-input NOR	2	7-207
10	AOI211H	2-Input AND, 1-Wide, into 3-input NOR, 2X	4	7-207
11	AOI22	2-Input AND, 2-Wide, into 2-input NOR	2	7-208
12	AOI22H	2-Input AND, 2-Wide, into 2-input NOR,2X	4	7-208
13	OA21H	2-Input OR, 1-Wide, into 2-input AND, 2X	3	7-325
14	OA22H	2-Input OR, 2-Wide, into 2-input AND, 2X	3	7-326
15	OAI21	2-Input OR, 1-Wide, into 2-input NAND	2	7-327
16	OAI21H	2-Input OR, 1-Wide, into 2-input NAND,2X	3	7-327
17	OAI211	2-Input OR, 1-Wide, into 3-input NAND	2	7-328
18	OAI211H	2-Input OR, 1-Wide, into 3-input NAND,2X	4	7-328
19	OAI22	2-Input OR, 2-Wide, into 2-input NAND	2	7-330
20	OAI22H	2-Input OR, 2-Wide, into 2-input NAND, 2X	4	7-330
21	ONDAI22	2-Input OR + 2-Input NAND, into 2-Input NAND	3	7-332
22	ONDAI22H	2-Input OR + 2-Input NAND, into 2-Input NAND, 2X Drive	4	7-332
		INVERTING BUFFERS		
1	INV	Inverter	1	7-266
2	INVB	Inverter, Balanced(Symmetrical Rise & Fall)	1	7-266
3	INV2	2-Inverters in parallel	1	7-267
4	INV2B	2-Inverters in parallel, Balanced (Symmetrical Rise & Fall)	2	7-267
5	INV4	4-Inverters in parallel	2	7-268
6	INV4B	4-Inverters in parallel, Balanced (Symmetrical Rise & Fall)	4	7-268
7	INV8	8-Inverters in parallel	4	7-269
8	INV8B	8-Inverters in parallel, Balanced (Symmetrical Rise & Fall)	8	7-269
9	INVX	Inverted Buffer (used to drive internal logic from an I/O Site)	--	7-272
		NON-INVERTING BUFFERS		
1	BUF	1X drive Buffer	1	7-210
2	BUF2	2X drive Buffer	2	7-211
3	BUF2B	2X drive Buffer, Balanced (Symmetrical Rise & Fall)	3	7-211
4	BUF4	4X drive Buffer	3	7-212
5	BUF4B	4X drive Buffer, Balanced (Symmetrical Rise & Fall)	5	7-212
6	BUF8	8X drive Buffer	5	7-213
7	BUF8B	8X drive Buffer, Balanced (Symmetrical Rise & Fall)	9	7-213
8	BUFX	Non-Inverting Buffer (used to drive internal logic from an I/O Site)	--	7-214

INTERNAL MACROS

#	INTERNAL MACROS		Gates	Page #
		3-STATE BUFFERS		
1	TBUF	3-state Buffer, Active Low Enable	4	7-343
2	TBUFH	3-state Buffer, Active Low Enable, 2X Drive	5	7-343
3	TBUFP	3-state Buffer, Active High Enable	4	7-344
4	TBUFPH	3-state Buffer, Active High Enable, 2X Drive	5	7-344
5	INVT	Inverting 3-state Buffer, Active Low Enable	2	7-270
6	INVTH	Inverting 3-state Buffer, Active Low Enable, 2X Drive	3	7-270
7	INVTP	Inverting 3-state Buffer, Active High Enable	3	7-271
8	INVTPH	Inverting 3-state Buffer, Active High Enable, 2x Drive	4	7-271
		D TYPE FLIP-FLOPS		
1	DFF1A	Scan D Flip-Flop	15	7-222
2	DFF4A	4-Bit Scan D Flip-Flop	48	7-224
3	DFFGLP	D Flip-Flop, Multiplexed (or Scan) Input with HOLD function	13	7-226
4	DFFP	D Flip-Flop	8	7-230
5	DFFPH	DFFP, 2X Drive	8	7-230
6	DFFLPA	D Flip-Flop, Multiplexed (or Scan) W/Unbuffered Input/ Clock	8	7-228
7	DFFLPAH	DFFLP, 2X Drive	9	7-228
8	DFFRP	D Flip-Flop with Reset	8	7-232
9	DFFRPH	DFFRP, 2X Drive	10	7-232
10	DFFRLP	D Flip-Flop W/Reset, Multiplexed (or Scan) Input	11	7-234
11	DFFRLPH	DFFRLP, 2X Drive	11	7-234
12	DFFRSLPB	D Flip-Flop w/Set and Reset	14	7-238
13	DFFRSPHB	D Flip-Flop w/Set and Reset, 2X Drive	10	7-236
14	DFFSCH	DFFSC, 2X Drive	18	7-240
15	DFFSCAH	DFFSCA, 2X Drive	20	7-242
16	DFFSP	D Flip-Flop with Set	8	7-245
17	DFFSPH	DFFSP, 2X Drive	10	7-245
18	DFFSLP	D Flip-Flop w/Set, Multiplexed (or Scan) Input	12	7-247
19	DFFSLPH	DFFSLP, 2X Drive	12	7-247
20	DFFSRPA	D Flip-Flop with Synchronous Reset	9	7-249
21	DFFSRLPA	D Flip-Flop, Multiplexed (or Scan) Input with Synchronous Reset	12	7-251
22	DFFSSP	D Flip-Flop with Synchronous Set	9	7-253
23	DFFSSLP	D Flip-Flop, Multiplexed (or Scan) Input with Synchronous Set	12	7-255
		LATCHES		
1	LATN	D-Type Latch, Neg Gate Latched	5	7-276
2	LATNH	LATN, 2X Drive	6	7-276
3	LATP	D-Type Latch, Pos Gate Latched	5	7-278
4	LATPH	LATP, 2X Drive	6	7-278
5	LATRN	D-Type Latch W/Reset, Neg Gate Latched	6	7-280
6	LATRNH	LATRN, 2X Drive	7	7-280
7	LATRP	D-Type Latch W/Reset, Pos Gate Latched	6	7-282
8	LATRPH	LATRP, 2X Drive	7	7-282
9	LAT4TH	LAT4TH, 2X Drive	23	7-284
10	LSSD1AH	LSSD1A, 2X Drive	14	7-286
11	SRLSSD1H	SRLSSD1, 2X Drive	13	7-341

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		MULTIPLEXERS		
1	MUX2A	2-1 Multiplexer, 1X Drive	3	7-291
2	MUX2H	2-Input Multiplexer, 2X Drive	3	7-292
3	MUX2IH	MUX2I, 2X Drive	3	7-293
4	MUX4H	4-Input Multiplexer, 2X Drive	7	7-294
5	MUX41A	Four 2-1 MUX with Common Select	12	7-295
6	MUX41AH	MUX41A, 2X Drive	14	7-295
7	MUX8AH	7-Input Multiplexer, 2X Drive	18	7-296
8	MX41	4-Input Multiplexer with individual Selects, 2X Drive	5	7-298
9	MX41H	MX41, 2X Drive	6	7-298
10	MX61	6-Input MultiplexerW/ Individual Selects	8	7-300
11	MX61H	MX61, 2X Drive	9	7-300
12	MX81	8-Input Multiplexer W/Individual Selects	10	7-302
13	MX81H	MX81, 2X Drive	12	7-302
		DECODERS		
1	DEC4H	DEC4, 2X Drive	9	7-217
2	DEC4AH	1 of 4 Decoder, Active High Outputs, 2X Drive	14	7-218
3	DEC1OF8	1 of 8 Decoder with Enable, Active Low Outputs	16	7-219
4	DEC8AH	1 of 8 Decoder with Enable, Active High Outputs, 2X Drive	30	7-220
		ARITHMETIC CIRCUITS		
1	AD4FULA	4-Bit Full Adder, 2X Drive	40	7-185
2	AD4PG	4-Bit Full Adder with Propagate & Generate, 2X Drive	94	7-187
3	ADFULH	ADFUL, 2X Drive	10	7-192
4	ADFULHA	Full Adder, 2X Drive	10	7-193
5	ADHALFH	ADHALF, 2X Drive	6	7-194
6	ECOMP4	4-Bit Equality Comparator	16	7-258
7	LACG4	4-bit Look-Ahead-Carry Generator	32	7-273
8	MCOMP4	4-bit Magnitude Comparator	35	7-289
		MISCELLANEOUS		
1	DCR4H	4-Bit Decrementer, 2X Drive	28	7-215
2	DLY8	7-Stage Inverter Delay5/5 Volt	4	7-257
3	INC4H	4-Bit Incrementer, 2X Drive	28	7-264
4	ROT8A	8-Bit Rotate, 1X Drive	54	7-338
5	SHIFT8	8-Bit Shift Register	45	7-340

MEMORY BLOCKS

MEMORY BLOCKS				
#	Name	Ram Size	Gate Count	Page Number
		Single-Port RAM's (LOW Power)		
1	RSB8X8	8 word X 8bit	198	7-346
2	RSB8X18	8 word X 18bit	440	7-346
3	RSB16X8	16 word X 8bit	342	7-346
4	RSB16X18	16 word X 18bit	760	7-346
5	RSB16X36	16 word X 36 bit	1440	7-346
6	RSB32X8	32 word X 8bit	630	7-346
7	RSB32X18	32 word X 18 bit	1400	7-346
8	RSB32X36	32 word X 36 bit	2660	7-346
9	RSB64X18	64 word X 18 bit	2680	7-346
10	RSB64X36	64 word X 36 bit	5092	7-346
		Dual-Port RAM's (HIGH Speed)		
1	RDB8X9	8 word X 9 bit	356	7-352
2	RDB8X18	8 word X 18 bit	608	7-352
3	RDB8X36	8 word X 36 bit	1112	7-352
4	RDB8X72	8 word X 72 bit	2156	7-352
5	RDB16X9	16 word X 9 bit	725	7-352
6	RDB16X18	16 word X 18 bit	1193	7-352
7	RDB16X36	16 word X 36 bit	2129	7-352
8	RDB16X72	16 word X 72 bit	4050	7-352
9	RDB32X9	32 word X 9 bit	1400	7-352
10	RDB32X18	32 word X 18 bit	2300	7-352
11	RDB32X36	32 word X 36 bit	4100	7-352
12	RDB32X72	32 word X 72 bit	7798	7-352
		QUAD Port RAM's		
1	RQB16X18	16 word X 18 bit	2200	7-358
2	RQB16X36	16 word X 36 bit	3766	7-358
3	RQB32X18	32 word X 18 bit	4762	7-358
4	RQB32X36	32 word X 36 bit	7738	7-358

#	PERIPHERAL MACROS		S	Page #
		5/5 Volt INPUTS		
1	ICI	CMOS, Inverting Input	1/0	7-1
2	BICI	CMOS, Inverting Input (Input part of Bidirectional)	1/0	7-1
3	ICN	CMOS, Non-inverting Input	1/0	7-2
4	BICN	CMOS, Non-inverting Bidirectional Input	1/0	7-2
5	ICNH	CMOS, Non-inverting Clock Driver Input	1/1	7-2
6	ISN	CMOS Schmitt, Non-inverting Input	1/0	7-3
7	BISN	CMOS Schmitt, Non-inverting Bidirectional Input	1/0	7-3
8	ISNH	CMOS, Schmitt, Non-inverting Clock Driver Input	1/1	7-3
9	ITN	TTL, Non-inverting Input	1/0	7-4
10	BITN	TTL, Non-inverting Bidirectional Input	1/0	7-4
11	ITNH	TTL, Non-inverting Clock Driver Input	1/1	7-4
12	ITSN	TTL Schmitt, Non-inverting Input	1/0	7-5
13	BITSN	TTL, Schmitt, Non-inverting Bidirectional Input	1/0	7-5
14	ITSNH	TTL, Schmitt, Non-inverting Clock Driver Input	1/1	7-5
		5/3.3 Volt INPUTS		
15	ICXN	CMOS, Non-inverting Input	1/0	7-2
16	BICXN	CMOS, Non-inverting Bidirectional Input	1/0	7-2
17	ICXNH	CMOS, Non-inverting Clock Driver Input	1/1	7-2
18	ISXN	CMOS Schmitt, Non-inverting Input	1/0	7-3
19	BISXN	CMOS Schmitt, Non-inverting Bidirectional Input	1/0	7-3
20	ISXNH	CMOS, Schmitt, Non-inverting Clock Driver Input	1/1	7-3
		3.3/5 Volt INPUTS		
21	ILTXN	TTL, Non-inverting Input	1/0	7-4
22	BILTXN	TTL, Non-inverting Bidirectional Input	1/0	7-4
23	ILTXNH	TTL, Non-inverting Clock Driver Input	1/1	7-4
		3.3/3.3 Volt INPUTS		
1	ILCI	CMOS, Inverting Input	1/0	7-1
2	BILCI	CMOS, Inverting Bidirectional Input	1/0	7-1
3	ILCN	CMOS, Non-inverting Input	1/0	7-2
4	BILCN	CMOS, Non-inverting Bidirectional Input	1/0	7-2
5	ILCNH	CMOS, Non-inverting Clock Driver Input	1/1	7-2
6	ILSN	CMOS Schmitt, Non-inverting Input	1/0	7-3
7	BILSN	CMOS Schmitt, Non-inverting Bidirectional Input	1/0	7-3
8	ILSNH	CMOS, Schmitt, Non-inverting Clock Driver Input	1/1	7-3
		5/5 Volt OUTPUTS		
1	ON2	3mA Standard Output	0/1	7-6
2	ON4	6mA Standard Output	0/1	7-6
3	ON8	12mA Standard Output	0/1	7-6
4	ON16	24mA Standard Output	0/1	7-6
5	ON32	32mA Standard Output	0/1	7-6
6	ON4S2	6mA Standard Output with Slew Control	0/1	7-9
7	ON8S2	12mA Standard Output with Slew Control	0/1	7-9
8	ON16S2	24mA Standard Output with Slew Control	0/1	7-9
9	ON32S2	32mA Standard Output with Slew Control	0/1	7-9
10	ON2T	3mA 3-State Output	0/1	7-11
11	BON2T	3mA 3-State Bidirectional Output	0/1	7-11
12	ON4T	6mA 3-State Output	0/1	7-11
13	BON4T	6mA 3-State Bidirectional Output	0/1	7-11
14	ON8T	12mA 3-State Output	0/1	7-11

#	PERIPHERAL MACROS		S	Page #
		5/5 Volt OUTPUTS (Continued)		
15	BON8T	12mA 3-State Bidirectional Output	0/1	7-11
16	ON16T	24mA 3-State Output	0/1	7-11
17	BON16T	24mA 3-State Bi-directional Output	0/1	7-11
18	ON32T	48mA 3-State Output	0/1	7-11
19	BON32T	48mA 3-State Bi-directional Output	0/1	7-11
20	ON4TS2	6mA 3-State Output with Slew Control	0/1	7-16
21	BON4TS2	6mA 3-State Output with Slew Control	0/1	7-16
22	ON8TS2	12mA 3-State Output with Slew Control	0/1	7-16
23	BON8TS2	12mA 3-State Output with Slew Control (Output part of Bidirectional)	0/1	7-16
24	ON16TS2	24mA 3-State Output with Slew Control	0/1	7-16
25	BON16TS2	24mA 3-State Output with Slew Control (Output part of Bidirectional)	0/1	7-16
26	ON32TS2	48mA 3-State Output with Slew Control	0/1	7-16
27	BON32TS2	48mA 3-State Output with Slew Control (Output part of Bidirectional)	0/1	7-16
28	ON2OD	3mA (Sink) Open-Drain Output	0/1	7-19
29	ON4OD	6mA (Sink) Open-Drain Output	0/1	7-19
30	ON8OD	12mA (Sink) Open-Drain Output	0/1	7-19
31	BON8OD	12mA (Sink) Open-Drain Bidirectional Output	0/1	7-19
32	ON16OD	24mA (Sink) Open-Drain Output	0/1	7-19
33	BON16OD	24mA (Sink) Open-Drain Bidirectional Output	0/1	7-19
34	ON32OD	48mA (Sink) Open-Drain Output	0/1	7-19
35	BON32OD	48mA (Sink) Open-Drain Bidirectional Output	0/1	7-19
		5/3.3 Volt OUTPUTS		
1	ONX2	3mA Standard Output	0/1	7-6
2	ONX4	6mA Standard Output	0/1	7-6
3	ONX8	12mA Standard Output	0/1	7-6
4	ONX2T	3mA 3-State Output	0/1	7-11
5	BONX2T	3mA 3-State Bidirectional Output	0/1	7-11
6	ONX4T	6mA 3-State Output	0/1	7-11
7	BONX4T	6mA 3-State Bidirectional Output	0/1	7-11
8	ONX8T	12mA 3-State Output	0/1	7-11
9	BONX8T	12mA 3-State Bidirectional Output	0/1	7-11
		3.3/5 Volt OUTPUTS		
1	ONLX2	2mA Standard Output	0/1	7-6
2	ONLX4	3mA Standard Output	0/1	7-6
3	ONLX8	6mA Standard Output	0/1	7-6
4	ONLX16	12mA Standard Output	0/1	7-6
5	ONLX2T	2mA 3-State Output	0/1	7-11
6	BONLX2T	2mA 3-State Bidirectional Output	0/1	7-11
7	ONLX4T	3mA 3-State Output	0/1	7-11
8	BONLX4T	3mA 3-State Bidirectional Output	0/1	7-11
9	ONLX8T	6mA 3-State Output	0/1	7-11
10	BONLX8T	6mA 3-State Bidirectional Output	0/1	7-11
11	ONLX16T	12mA 3-State Output	0/1	7-11
12	BONLX16T	12mA 3-State Bidirectional Output	0/1	7-11

#	PERIPHERAL MACROS		S	Page #
		3.3/3.3 Volt OUTPUTS		
1	ONL2	2mA Standard Output	0/1	7-6
2	ONL4	3mA Standard Output	0/1	7-6
3	ONL8	6mA Standard Output	0/1	7-6
4	ONL16	12mA Standard Output	0/1	7-6
5	ONL2T	2mA 3-State Output	0/1	7-11
6	BONL2T	2mA 3-State Bidirectional Output	0/1	7-11
7	ONL4T	3mA 3-State Output	0/1	7-11
8	BONL4T	3mA 3-State Bidirectional Output	0/1	7-11
9	ONL8T	6mA 3-State Output	0/1	7-11
10	BONL8T	6mA 3-State Bidirectional Output	0/1	7-11
11	ONL16T	12mA 3-State Output	0/1	7-11
12	BONL16T	12mA 3-State Bidirectional Output	0/1	7-11
13	ONL4OD	3mA (Sink) Open-Drain Output	0/1	7-19
14	ONL8OD	6mA (Sink) Open-Drain Output	0/1	7-19
15	BONL8OD	6mA (Sink) Open-Drain Bidirectional Output	0/1	7-19
16	ONL16OD	12mA (Sink) Open-Drain Output	0/1	7-19
17	BONL16OD	12mA (Sink) Open-Drain Bidirectional Output	0/1	7-19

Note: Any of the "B" prefix Outputs may be used with any of the "B" prefix Inputs (above) to form a unique Bidirectional combination (with or without any of the two "pull" resistors).

		5/5 Volt OSCILLATORS		
1	OSCPB	Standard Oscillator	2/2	7-21
2	OSCPHB	Oscillator with Clock Driver Buffer	2/2	7-21
3	OSCPSB	Oscillator with Schmitt Trigger Buffer	2/2	7-21
		3.3/3.3 Volt OSCILLATORS		
1	OSCPBL	Standard Oscillator	2/2	7-21
2	OSCPHBL	Oscillator with Clock Driver Buffer	2/2	7-21
3	OSCPSBL	Oscillator with Schmitt Trigger Buffer	2/2	7-21
		RESISTORS		
1	PUL	Pull-Up, Low current/speed Resistor	N/A	7-23
2	PDL	Pull-Down, Low current/speed Resistor	N/A	7-23

Note: Any one of these two resistors may be used with any Input or Bidirectional.

		5/5 Volt ANALOG PLL MACROS		
1	AP1	Analog CMOS PLL Type 1	0	7-362
2	AP2	Analog CMOS PLL Type 2	0	7-362
3	APD1	Analog PECL PLL Differential Type 1	0	7-365
4	APD2	Analog PECL PLL Differential Type 2	0	7-365
5	PLLDelay	Non-Inverting Analog PLL Buffer	1	7-368
		3.3/3.3 Volt ANALOG PLL MACROS		
1	APL1	Analog CMOS PLL Type 1	0	7-362
2	APL2	Analog CMOS PLL Type 2	0	7-362
3	APDL1	Analog PECL PLL Differential Type 1	0	7-365
4	APDL2	Analog PECL PLL Differential Type 2	0	7-365
5	PLLDelay	Non-Inverting Analog PLL Buffer	1	7-368

#	PERIPHERAL MACROS		S	Page #
		5/5 Volt CMTL INPUT/OUTPUT		
1	ICMD	CMTL Differential Input	1/0	7-24
2	BICMD	CMTL Differential Bidirectional Input	1/0	7-24
3	OD32TCMT	CMTL 3-State Differential Output with Active Termination	0/1	7-25
4	BOD32TCMT	CMTL Bidirectional 3-State Differential Output with Active Termination	0/1	7-25
5	O32CM	CMTL Output Single Ended	0/1	7-29
6	OD32CMT	CMTL 3-State Differential Output	0/1	7-27
		5/3.3 Volt CMTL INPUT/OUTPUT		
1	ODLX32CMT	CMTL 3-State Differential Output	0/1	7-27
		3.3/5 Volt CMTL INPUT/OUTPUT		
1	ODX32CM	CMTL Differential Output	0/1	7-26
		3.3/3.3 Volt CMTL INPUT/OUTPUT		
1	ILCMD	CMTL Differential Input	1/0	7-24
2	ODL32CMT	CMTL 3-State Differential Output	0/1	7-27
		5/5 Volt GTL INPUT/OUTPUT		
1	IGI	Inverting GTL Input	1/0	7-30
2	IGN	Non-Inverting GTL Input	1/0	7-31
3	BIGN	Non-Inverting GTL Bidirectional Input	1/0	7-31
4	ON20G	GTL Output	0/1	7-32
5	BON40G	GTL Bidirectional Output	0/1	7-32
		3.3/3.3 Volt GTL INPUT/OUTPUT		
1	ILGI	Inverting GTL Input	1/0	7-30
2	ILGN	Non-Inverting GTL Input	1/0	7-31
3	BILGN	Non-Inverting GTL Bidirectional Input	1/0	7-31
4	ONL20G	GTL Output	0/1	7-32
5	BONL40G	GTL Bidirectional Output	0/1	7-32
		5/5 Volt PECL INPUT/OUTPUT		
1	IPD	PECL Differential Input	1/0	7-33
		5/3.3 Volt PECL INPUT/OUTPUT		
1	IPXD	PECL Differential Input	1/0	7-33
		3.3/3.3 Volt PECL INPUT/OUTPUT		
1	ILPD	PECL Differential Input	1/0	7-33
		5/5 Volt PCI INPUT/OUTPUT		
1	IPCH	PCI Non-Inverting Clock Input	1/0	7-34
2	ONPC	PCI Standard Output	1/0	7-35
3	ONTPC	PCI 3-State Standard Output	1/0	7-36
4	BONTPC	PCI 3-State Bidirectional Output	1/0	7-36
		3.3/3.3 Volt PCI INPUT/OUTPUT		
1	ILPC	PCI Non-Inverting Input	1/0	7-34
1	BILPC	PCI Non-Inverting Bidirectional Input	1/0	7-34
2	ILPCH	PCI Non-Inverting Clock Input	1/0	7-34
3	ONLPC	PCI Standard Output	1/0	7-35
4	ONLTPC	PCI 3-State Standard Output	1/0	7-36
5	BONLTPC	PCI 3-State Bidirectional Output	1/0	7-36

JTAG INPUT and OUTPUT MACROS

#	JTAG MACROS		S or Gates	Page #
		JTAG Control Macro Functions		
1	BPREG	1-Bit Bypass Register	10	7-172
2	ENSCANI	Enable Boundary scan Macro	20	7-173
3	IDREG	32-Bit device Identification Code Register	256	7-175
4	MC_IREG	1-Bit pf Instruction Register (Soft Macro)	25	7-177
5	MC_IREG4	1-Bit pf Instruction Register (Soft Macro)	124	7-178
6	FMC_TAPCA	TAP Controller (FIRM Macro) Fixed Placement which effects Routing	276	7-179
		5/5 Volt INPUTS		
1	ICNJ	CMOS, Non-inverting Input	1/0	7-105
2	BICNJ	CMOS, Non-inverting Bidirectional Input	1/0	7-73
3	ICNCKHJ	CMOS, Non-inverting Clock Driver Input	1/0	7-114
4	ISNJ	CMOS Schmitt, Non-inverting Input	1/0	7-108
5	BISNJ	CMOS Schmitt, Non-inverting Bidirectional Input	1/0	7-74
6	ISNCKHJ	CMOS Schmitt, Non-inverting Clock Driver Input	1/0	7-117
7	ITNJ	TTL, Non-inverting Input	1/0	7-110
8	BITNJ	TTL, Non-inverting Bidirectional Input	1/0	7-75
9	ITNCKHJ	TTL, Non-inverting Clock Driver Input	1/0	7-119
10	ITSNJ	TTL Schmitt, Non-inverting Input	1/0	7-112
11	BITSNJ	TTL Schmitt, Non-inverting Bidirectional Input	1/0	7-76
12	ITSNCKHJ	TTL, Schmitt, Non-inverting Clock Driver Input	1/1	7-120
		5/3.3 Volt INPUTS		
1	ICXNJ	CMOS, Non-inverting Input	1/0	7-105
2	BICXNJ	CMOS, Non-inverting Bidirectional Input	1/0	7-73
3	ICXNCKHJ	CMOS, Non-inverting Clock Driver Input	1/0	7-114
4	ISXNJ	CMOS Schmitt, Non-inverting Input	1/0	7-108
5	BISXNJ	CMOS Schmitt, Non-inverting Bidirectional Input	1/0	7-74
6	ISXNCKHJ	CMOS Schmitt, Non-inverting Clock Driver Input	1/0	7-117
		3.3/5 Volt INPUTS		
1	ILTXNJ	TTL, Non-inverting Input	1/0	7-110
2	BILTXNJ	TTL, Non-inverting Bidirectional Input	1/0	7-75
3	ILTXNCKHJ	TTL, Non-inverting Clock Driver Input	1/0	7-119
		3.3/3.3 Volt INPUTS		
1	ILCNJ	CMOS, Non-inverting Input	1/0	7-105
2	BILCNJ	CMOS, Non-inverting Bidirectional Input	1/0	7-73
3	ILCNCKHJ	CMOS, Non-inverting Clock Driver Input	1/0	7-114
4	ILSNJ	CMOS Schmitt, Non-inverting Input	1/0	7-108
5	BILSNJ	CMOS Schmitt, Non-inverting Bidirectional Input	1/0	7-74
6	ILSNCKHJ	CMOS Schmitt, Non-inverting Clock Driver Input	1/0	7-117
		5/5 Volt OUTPUTS		
1	ON4J	6mA Standard Output	0/1	7-121
2	ON8J	12mA Standard Output	0/1	7-125
3	ON16J	24mA Standard Output	0/1	7-128
4	ON4S2J	6mA Standard Output with Slew Control	0/1	7-131
5	ON8S2J	12mA Standard Output with Slew Control	0/1	7-131
6	ON16S2J	24mA Standard Output with Slew Control	0/1	7-131
7	ON4TJ	6mA 3-State Output	0/1	7-142
8	BN4TJ	6mA 3-State Bidirectional Output	0/1	7-83
9	ON8TJ	12mA 3-State Output	0/1	7-146
10	BN8TJ	12mA 3-State Bidirectional Output	0/1	7-89
11	ON16TJ	24mA 3-State Output	0/1	7-150

#	JTAG MACROS		S or Gates	Page #
		5/5 Volt OUTPUTS (Continued)		
12	BN16TJ	24mA 3-State Bi-directional Output	0/1	7-94
13	ON4TS2J	6mA 3-State Output with Slew Control	0/1	7-154
14	BN4TS2J	6mA 3-State Output with Slew Control	0/1	7-99
15	ON8TS2J	12mA 3-State Output with Slew Control	0/1	7-154
16	BN8TS2J	12mA 3-State Output with Slew Control (Output part of Bidirectional)	0/1	7-89
17	ON16TS2J	24mA 3-State Output with Slew Control	0/1	7-154
18	BN16TS2J	24mA 3-State Output with Slew Control (Output part of Bidirectional)	0/1	7-99
19	ON4ODJ	6mA (Sink) Open-Drain Output	0/1	7-135
20	ON8ODJ	12mA (Sink) Open-Drain Output	0/1	7-138
21	BN8ODJ	12mA (Sink) Open-Drain Bidirectional Output	0/1	7-77
22	ON16ODJ	24mA (Sink) Open-Drain Output	0/1	7-140
23	BN16ODJ	24mA (Sink) Open-Drain Bidirectional Output	0/1	7-80
		5/3.3 Volt OUTPUTS		
1	ONX4J	6mA Standard Output	0/1	7-121
2	ONX8J	12mA Standard Output	0/1	7-121
3	ONX4TJ	6mA 3-State Output	0/1	7-121
4	BNX4TJ	6mA 3-State Bidirectional Output	0/1	7-83
5	ONX8TJ	12mA 3-State Output	0/1	7-146
6	B NX8TJ	12mA 3-State Bidirectional Output	0/1	7-89
		3.3/5 Volt OUTPUTS		
1	ONLX4J	3mA Standard Output	0/1	7-121
2	ONLX8J	6mA Standard Output	0/1	7-125
3	ONLX16J	12mA Standard Output	0/1	7-128
4	ONLX4TJ	3mA 3-State Output	0/1	7-142
5	BNLX4TJ	3mA 3-State Bidirectional Output	0/1	7-83
6	ONLX8TJ	6mA 3-State Output	0/1	7-146
7	BNLX8TJ	6mA 3-State Bidirectional Output	0/1	7-89
8	ONLX16TJ	12mA 3-State Output	0/1	7-150
9	BNLX16TJ	12mA 3-State Bidirectional Output	0/1	7-94
		3.3/3.3 Volt OUTPUTS		
1	ONL4J	3mA Standard Output	0/1	7-121
2	ONL8J	6mA Standard Output	0/1	7-125
3	ONL16J	12mA Standard Output	0/1	7-128
4	ONL4TJ	3mA 3-State Output	0/1	7-142
5	BNL4TJ	3mA 3-State Bidirectional Output	0/1	7-83
6	ONL8TJ	6mA 3-State Output	0/1	7-146
7	BNL8TJ	6mA 3-State Bidirectional Output	0/1	7-89
8	ONL16TJ	12mA 3-State Output	0/1	7-150
9	BNL16TJ	12mA 3-State Bidirectional Output	0/1	7-94
10	ONL4ODJ	3mA (Sink) Open-Drain Output	0/1	7-135
11	ONL8ODJ	6mA (Sink) Open-Drain Output	0/1	7-138
12	BNL8ODJ	6mA (Sink) Open-Drain Bidirectional Output	0/1	7-77
13	ONL16ODJ	12mA (Sink) Open-Drain Output	0/1	7-140
14	BNL16ODJ	12mA (Sink) Open-Drain Bidirectional Output	0/1	7-80

Note: Any of the "B" prefix Outputs may be used with any of the "B" prefix Inputs (above) to form a unique Bidirectional combination (with or without any of the two "pull" resistors).

JTAG, OSCILLATOR, CMTL, GTL, PECL and PCI MACROS

#	JTAG MACROS		S or Gates	Page #
		5/5 Volt OSCILLATORS		
1	OSCPBJ	B-S Register Oscillator W/Non-Inverting	2/2	7-158
2	OSCPHBJ	Input/Oscillator W/Clock Buffer Input	2/2	7-158
3	OSCPSB	Oscillator W/Schmitt Trigger Input -JTAG	2/2	7-158
		3.3/3.3 Volt OSCILLATORS		
1	OSCPBLJ	B-S Register Oscillator W/Non-Inverting	2/2	7-158
2	OSCPHBLJ	Input/Oscillator W/Clock Buffer Input	2/2	7-158
3	OSCPSBLJ	Oscillator W/Schmitt Trigger Input -JTAG	2/2	7-158
		5/5 Volt CMTL INPUT/OUTPUT		
1	ICMDJ	CMTL Differential Input	1/0	7-37
2	OD32TCMTJ	CMTL 3-State Differential Output with Active Termination	0/1	7-38
3	OD32CMTJ	CMTL 3-State Differential Output	0/1	7-40
		3.3/3.3 Volt CMTL INPUT/OUTPUT		
4	ODL32CMTJ	CMTL 3-State Differential Output	0/1	7-40
		5/5 Volt GTL INPUT/OUTPUT		
1	IGNJ	Non-Inverting GTL Input	1/0	7-42
2	BIGNJ	Non-Inverting GTL Bidirectional Input	1/0	7-44
3	ON20GJ	GTL Output	0/1	7-45
4	BN40GJ	GTL Bidirectional Output	0/1	7-45
		3.3/3.3 Volt GTL INPUT/OUTPUT		
1	ILGNJ	Non-Inverting GTL Input	1/0	7-42
2	BILGNJ	Non-Inverting GTL Bidirectional Input	1/0	7-44
3	ONL20GJ	GTL Output	0/1	7-45
4	BNL40GJ	GTL Bidirectional Output	0/1	7-45
		5/5 Volt PECL INPUT/OUTPUT		
1	IPDJ	PECL Differential Input	1/0	7-49
		5/5 Volt PCI INPUT/OUTPUT		
1	IPCHJ	PCI Non-Inverting Input	1/0	7-51
2	ONPCJ	PCI Standard Output	1/0	7-54
3	ONTPCJ	PCI 3-State Standard Output	1/0	7-56
4	BNTPCJ	PCI 3-State Bidirectional Output	1/0	7-59
		3.3/3.3 Volt PCI INPUT/OUTPUT		
1	ILPCJ	PCI Non-Inverting Input	1/0	7-50
1	BILPCJ	PCI Non-Inverting Bidirectional Input	1/0	7-53
2	ILPCHJ	PCI Non-Inverting Input	1/0	7-51
3	ONLPCJ	PCI Standard Output	1/0	7-54
4	ONLTPCJ	PCI 3-State Standard Output	1/0	7-56
5	BNLTPCJ	PCI 3-State Bidirectional Output	1/0	7-59

#	JTAG TAP I/O MACROS		S or Gates	Page #
		5/5 Volt TAP Inputs/Outputs Functions		
1	TCK	Test Clock	1/0	7-63
2	TCKH	Test Clock, High Drive	1/1	7-63
3	TCKT	Test Clock, TTL Levels	1/0	7-64
4	TCKHT	Test Clock, TTL Levels, High Drive	1/1	7-64
5	TDI	Test Data Input	1/0	7-65
6	TDIT	Test Data Input,TTL Levels	1/0	7-66
7	TDOUT	Test Data Output	1/1	7-66

JTAG TAP MACROS and BOUNDARY SCAN MACROS

#	JTAG TAP I/O MACROS		S or Gates	Page #
8	TMS	Test Mode Select	1/0	7-67
9	TMST	Test Mode Select, TTL Levels	1/0	7-68
10	TRSTB	Test Reset (Bar)	1/0	7-69
11	TRSTBT	Test Reset (Bar),TTL Levels	1/0	7-70
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3	TCKTX	Test Clock, TTL Levels	1/0	7-64
4	TCKHTX	Test Clock, TTL Levels, High Drive	1/1	7-64
5	TDIX	Test Data Input	1/0	7-65
6	TDITX	Test Data Input,TTL Levels	1/0	7-65
7	TDOUTX	Test Data Output	1/1	7-71
8	TMSX	Test Mode Select	1/0	7-67
9	TMSTX	Test Mode Select, TTL Levels	1/0	7-68
10	TRSTBX	Test Reset (Bar)	1/0	7-69
11	TRSTBTX	Test Reset (Bar),TTL Levels	1/0	7-70
		3.3/5 Volt TAP Inputs/Outputs Functions		
1	TCKLTX	Test Clock, TTL Levels	1/0	7-64
2	TCKHLTX	Test Clock, TTL Levels, High Drive	1/1	7-64
3	TDILTX	Test Data Input,TTL Levels	1/0	7-66
4	TDOUTLX	Test Data Output	1/1	7-71
5	TMSLTX	Test Mode Select, TTL Levels	1/0	7-68
6	TRSTBTX	Test Reset (Bar),TTL Levels	1/0	7-70
		3.3/3.3 Volt TAP Inputs/Outputs Functions		
1	TCKL	Test Clock	1/0	7-63
2	TCKHL	Test Clock, High Drive	1/1	7-63
3	TDIL	Test Data Input	1/0	7-65
4	TDOUTL	Test Data Output	1/1	7-71
5	TMSL	Test Mode Select	1/0	7-67
6	TRSTBL	Test Reset (Bar)	1/0	7-69
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3	CKDRCC2	B-S Register Clock Driver -JTAG	0	7-163
4	ENSCANJ	B-S Register Enable Scan Macro -JTAG	0	7-170
5	IMCDR	B-S Register Input Mode Control Driver -JTAG	0	7-164
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9	TDBUF	B-S Register Test Data Buffer -JTAG	1/0	7-168
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MACRO LIBRARY COMPOSITES

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7 MACRO LIBRARY COMPOSITES

SECTION 7. H4CP SERIES MACRO COMPOSITES

Section 7.1 Periphery Cells (Inputs/Outputs/Bidirectionals)

Inverting CMOS Inputs and Bidirectional Input (3.3 V and 5 V System/Core Voltage)

5/5 V **ICI/BICI**
3.3/3.3 V **ILCI/BILCI**

MACRO	SECTIONS USED
ICI/ILCI	1/0
BICI/BILCI	1/0

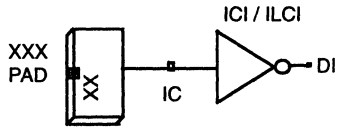
Rev. 1.07

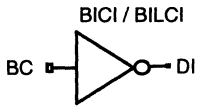
MACRO	OUTPUTS/INPUTS
ICI/ILCI	DI / PAD,IC
BICI/BILCI	DI / BC

MACRO	INPUT CAP.
ICI/ILCI	PAD: 5.29pF
BICI/BILCI	BC: 0.39pF

Function Table

PAD	DI
L	H
H	L





CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		ICI/BICI				ILCI/BILCI			
t_{PLH}	Propagation Delay, PAD to DI	0.18	0.19	0.23	0.12	0.23	0.24	0.29	0.15
t_{PHL}		0.16	0.18	0.22	0.15	0.20	0.22	0.27	0.18
t_r	Output Rise Time, DI	0.18	0.20	0.27	0.24	0.20	0.23	0.33	0.33
t_f	Output Fall Time, DI	0.17	0.19	0.25	0.18	0.15	0.18	0.25	0.24

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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Non-Inverting CMOS Inputs, Bidirectional Inputs and Clock Inputs (3.3 V and 5 V System/Core Voltage)

5/5 V **ICN/BICN/ICNH**
5/3.3 V **ICXN/BICXN/ICXNH**
3.3/3.3 V **ILCN/BILCN/ILCNH**

MACRO	SECTIONS USED
ICN/ICXN/ILCN	1/0
BICN/BICXN/ BILCN	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
ICN/ICXN/ILCN	DI / PAD,IC
BICN/BICXN/ BILCN	DI / BC

MACRO	INPUT CAP.
ICN/ICXN/ILCN	PAD: 5.06pF
BICN/BICXN/ BILCN	BC: 0.10pF

MACRO	SECTIONS USED
ICNH/ICXNH/ ILCNH	1/1

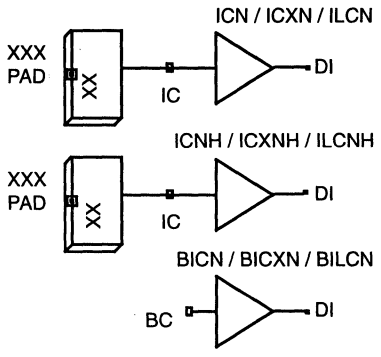
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ICNH/ILCNH	DI / PAD,IC

MACRO	INPUT CAP.
ICNH/ILCNH	PAD: 5.16pF

Function Table

PAD	DI
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=25	FO=50	K (ns/pF)
		ICN/BICN				ICNH			
t_{PLH}	Propagation Delay, PAD to DI	0.35	0.36	0.39	0.11	0.38	0.47	0.55	0.07
t_{PHL}		0.36	0.37	0.42	0.15	0.41	0.50	0.58	0.07
t_r	Output Rise Time, DI	0.13	0.15	0.23	0.25	0.16	0.28	0.39	0.09
t_f	Output Fall Time, DI	0.12	0.14	0.20	0.20	0.21	0.30	0.39	0.07

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		ICXN/BICXN				ILCN/BILCN			
t_{PLH}	Propagation Delay, PAD to DI	0.39	0.41	0.45	0.15	0.45	0.46	0.51	0.15
t_{PHL}		0.44	0.46	0.52	0.19	0.48	0.50	0.56	0.19
t_r	Output Rise Time, DI	0.15	0.19	0.29	0.35	0.17	0.21	0.31	0.34
t_f	Output Fall Time, DI	0.13	0.16	0.23	0.25	0.17	0.20	0.27	0.24

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		FO=0	FO=25	FO=50	K (ns/pF)	FO=0	FO=25	FO=50	K (ns/pF)
		ICXNH				ILCNH			
t_{PLH}	Propagation Delay, PAD to DI	0.31	0.38	0.45	0.05	0.50	0.61	0.72	0.09
t_{PHL}		0.26	0.36	0.47	0.09	0.51	0.61	0.72	0.09
t_r	Output Rise Time, DI	0.18	0.36	0.54	0.14	0.20	0.36	0.53	0.13
t_f	Output Fall Time, DI	0.20	0.37	0.54	0.14	0.22	0.35	0.48	0.10

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

Non-Inverting CMOS Schmitt Trigger Inputs and Bidirectional Input (3.3 V and 5 V System/Core Voltage)

5/5 V — **ISN/BISN/ISNH**
5/3.3 V — **ISXN/BISXN/ISXNH**
3.3/3.3 V — **ILSN/BILSN/ILSNH**

MACRO	SECTIONS USED
ISN/ISXN/ILSN	1/0
BISN/BISXN/ BILSN	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
ICN/ICXN/ILCN	DI / PAD,IC
BISN/BISXN/ BILSN	DI / BC

MACRO	INPUT CAP.
ISN/ISXN/ILSN	PAD: 5.08pF
BISN/BISXN/ BILSN	BC: 0.12pF

MACRO	SECTIONS USED
ISNH/ISXNH/ ILSNH	1/1

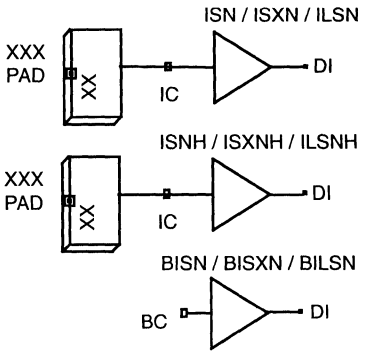
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ISNH/ILSNH	DI / PAD,IC

MACRO	INPUT CAP.
ISNH/ILSNH	PAD: 5.20pF

Function Table

PAD	DI
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=25	FO=50	K (ns/pF)
		ISN/BISN				ISNH			
t_{PLH}	Propagation Delay, PAD to DI	0.55	0.56	0.59	0.11	0.49	0.54	0.59	0.04
t_{PHL}		0.80	0.82	0.87	0.18	0.90	0.99	1.08	0.07
t_r	Output Rise Time, DI	0.16	0.18	0.26	0.25	0.20	0.34	0.48	0.11
t_f	Output Fall Time, DI	0.27	0.29	0.35	0.20	0.35	0.49	0.64	0.12

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		ISXN/BISXN				ILSN/BILSN			
t_{PLH}	Propagation Delay, PAD to DI	0.48	0.50	0.55	0.16	0.65	0.66	0.71	0.17
t_{PHL}		0.98	1.01	1.08	0.24	1.07	1.09	1.16	0.24
t_r	Output Rise Time, DI	0.16	0.20	0.32	0.39	0.20	0.24	0.34	0.34
t_f	Output Fall Time, DI	0.39	0.41	0.49	0.25	0.31	0.34	0.41	0.26

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		FO=0	FO=25	FO=50	K (ns/pF)	FO=0	FO=25	FO=50	K (ns/pF)
		ISXNH				ILSNH			
t_{PLH}	Propagation Delay, PAD to DI	0.46	0.52	0.59	0.05	0.59	0.66	0.73	0.06
t_{PHL}		0.93	1.04	1.16	0.09	1.26	1.37	1.49	0.09
t_r	Output Rise Time, DI	0.21	0.38	0.56	0.14	0.25	0.42	0.59	0.14
t_f	Output Fall Time, DI	0.44	0.60	0.76	0.13	0.52	0.69	0.86	0.14

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

Non-Inverting TTL Inputs and Bidirectional Input and Clock Inputs (3.3 V and 5 V System/Core Voltage)

5/5 V ITN/BITN/ITNH
3.3/5 V ILTXN/BILTXN/ILTXNH

MACRO	SECTIONS USED
ITN/ILTXN	1/0
BITN/BILTXN	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
ITN/ILTXN	DI / PAD,IC
BITN/BILTXN	DI / BC

MACRO	INPUT CAP.
ITN/ILTXN	PAD: 5.05pF
BITN/BILTXN	BC: 0.09pF

MACRO	SECTIONS USED
ITNH	1/1

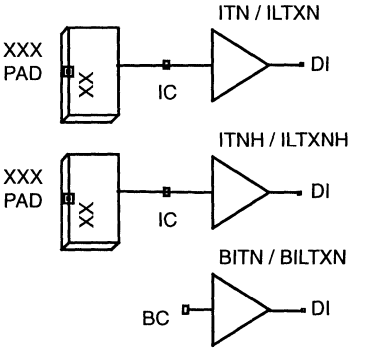
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ITNH	DI / PAD,IC

MACRO	INPUT CAP.
ITNH	PAD: 5.06pF

Function Table

PAD	DI
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		ITN/BITN				ILTXN/BILTXN			
t_{PLH}	Propagation Delay, PAD to DI	0.29	0.31	0.34	0.11	0.29	0.31	0.34	0.11
t_{PHL}		0.64	0.65	0.71	0.18	0.64	0.65	0.71	0.18
t_r	Output Rise Time, DI	0.12	0.15	0.22	0.24	0.12	0.15	0.22	0.24
t_f	Output Fall Time, DI	0.28	0.30	0.36	0.20	0.28	0.30	0.36	0.20

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=25	FO=50	K (ns/pF)	FO=0	FO=25	FO=50	K (ns/pF)
		ITNH				ILTXNH			
t_{PLH}	Propagation Delay, PAD to DI	0.49	0.55	0.62	0.05	0.48	0.48	0.49	0.04
t_{PHL}		0.80	0.89	0.98	0.07	0.76	0.77	0.79	0.07
t_r	Output Rise Time, DI	0.11	0.23	0.35	0.09	0.11	0.13	0.16	0.11
t_f	Output Fall Time, DI	0.19	0.29	0.39	0.08	0.20	0.21	0.25	0.12

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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Non-Inverting TTL Schmitt Trigger Input (5 V System/Core Voltage) 5/5 V ITSN/BITSN

MACRO	SECTIONS USED
ITSN	1/0
BITSN	1/0

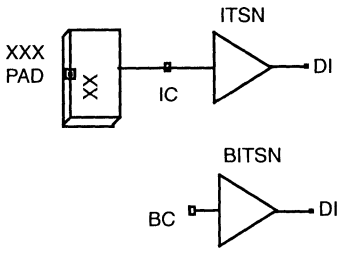
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ITSN	DI / PAD,IC
BITSN	DI / BC

MACRO	INPUT CAP.
ITSN	PAD: 5.17pF
BITSN	BC: 0.21pF

Function Table

PAD	DI
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		ITSN/BITSN			
t_{PLH}	Propagation Delay, PAD to DI	0.47	0.48	0.51	0.11
t_{PHL}		1.03	1.05	1.10	0.19
t_r	Output Rise Time, DI	0.13	0.16	0.23	0.25
t_f	Output Fall Time, DI	0.33	0.35	0.41	0.20

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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Output Buffers (3.3 V and 5 V System/Core Voltage)

5/5 V **ONn**
5/3.3 V **ONXn**
3.3/5 V **ONLXn**
3.3/3.3 V **ONLn**
n=2, 4, 8, 16 or 32

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

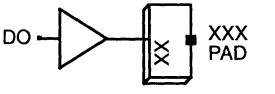
MACRO	OUTPUTS/INPUTS
All	PAD / DO

MACRO	INPUT CAP.
ON2,ONL2	DO: 0.28pF
ONLX2	DO: 0.30pF
ON4,ONL4	DO: 0.39pF
ONLX4	DO: 0.54pF
ON8,ONL8	DO: 0.56pF
ON16,ONLX16,ONL16	DO: 0.90pF
ON32	DO: 1.66pF
ONX2,ONX4	DO: 0.40pF
ONX8	DO: 0.47pF
ONLX8	DO: 0.75pF

Function Table

DO	PAD
L	L
H	H

ONn / ONXn / ONLXn / ONLn



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON2				ONLX2			
t_{PLH}	Propagation Delay, DO to PAD	0.41	4.92	9.43	0.09	0.89	4.85	8.80	0.08
t_{PHL}		0.38	6.27	12.15	0.12	0.35	4.47	8.59	0.08
t_r	Output Rise Time, PAD	0.22	10.61	21.00	0.21	0.36	9.34	18.33	0.18
t_f	Output Fall Time, PAD	0.23	11.80	23.37	0.23	0.18	9.55	18.92	0.19
		ON4				ONLX4			
t_{PLH}	Propagation Delay, DO to PAD	0.59	2.86	5.12	0.05	0.55	2.79	5.03	0.04
t_{PHL}		0.58	2.56	4.55	0.04	0.41	2.48	4.54	0.04
t_r	Output Rise Time, PAD	0.28	5.41	10.55	0.10	0.26	5.31	10.37	0.10
t_f	Output Fall Time, PAD	0.30	4.08	7.87	0.08	0.18	4.84	9.50	0.09
		ON8				ONLX8			
t_{PLH}	Propagation Delay, DO to PAD	0.43	1.74	3.05	0.03	0.77	2.19	3.61	0.03
t_{PHL}		0.75	2.03	3.32	0.03	0.68	1.87	3.07	0.02
t_r	Output Rise Time, PAD	0.21	3.13	6.06	0.06	0.53	3.46	6.40	0.06
t_f	Output Fall Time, PAD	0.46	3.29	6.11	0.06	0.48	2.79	5.10	0.05
		ON16				ONLX16			
t_{PLH}	Propagation Delay, DO to PAD	0.52	1.39	2.27	0.02	0.76	2.18	3.60	0.03
t_{PHL}		0.64	1.53	2.42	0.02	0.50	1.20	1.90	0.01
t_r	Output Rise Time, PAD	0.36	2.09	3.81	0.03	0.50	3.44	6.38	0.06
t_f	Output Fall Time, PAD	0.42	1.87	3.32	0.03	0.39	1.59	2.79	0.02
		ON32				N/A			
t_{PLH}	Propagation Delay, DO to PAD	0.34	0.84	1.34	0.01				
t_{PHL}		0.54	1.08	1.61	0.01				
t_r	Output Rise Time, PAD	0.38	1.33	2.29	0.02				
t_f	Output Fall Time, PAD	0.72	1.33	1.93	0.01				

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX2				ONL2			
t_{PLH}	Propagation Delay, DO to PAD	0.70	5.19	9.69	0.09	0.55	6.95	13.35	0.13
t_{PHL}		0.86	6.56	12.27	0.11	0.53	7.58	14.63	0.14
t_r	Output Rise Time, PAD	0.49	10.87	21.26	0.21	0.32	14.63	28.93	0.29
t_f	Output Fall Time, PAD	0.54	12.10	23.66	0.23	0.31	14.40	28.49	0.28
		ONX4				ONL4			
t_{PLH}	Propagation Delay, DO to PAD	1.02	3.28	5.55	0.05	0.75	3.95	7.16	0.06
t_{PHL}		0.86	3.79	6.73	0.06	0.73	3.12	5.50	0.05
t_r	Output Rise Time, PAD	0.47	5.58	10.68	0.10	0.32	7.43	14.53	0.14
t_f	Output Fall Time, PAD	0.36	6.11	11.87	0.12	0.35	4.96	9.58	0.09
		ONX8				ONL8			
t_{PLH}	Propagation Delay, DO to PAD	1.06	2.49	3.92	0.03	0.57	2.41	4.25	0.04
t_{PHL}		1.15	2.72	4.29	0.03	0.95	2.49	4.03	0.03
t_r	Output Rise Time, PAD	0.70	3.57	6.43	0.06	0.25	4.28	8.32	0.08
t_f	Output Fall Time, PAD	0.58	3.40	6.23	0.06	0.56	3.98	7.41	0.07
		N/A				ONL16			
t_{PLH}	Propagation Delay, DO to PAD					0.71	1.89	3.08	0.02
t_{PHL}						0.82	1.88	2.95	0.02
t_r	Output Rise Time, PAD					0.46	2.80	5.15	0.05
t_f	Output Fall Time, PAD					0.52	2.26	4.01	0.03

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON2				ONLX2			
t_{PLH}	Propagation Delay, DO to PAD	0.36	2.63	4.90	0.05	0.87	3.90	6.94	0.06
t_{PHL}		0.45	9.58	18.71	0.18	0.37	5.54	10.72	0.10
t_r	Output Rise Time, PAD	0.22	10.61	21.00	0.21	0.36	9.34	18.33	0.18
t_f	Output Fall Time, PAD	0.23	11.80	23.37	0.23	0.18	9.55	18.92	0.19
		ON4				ONLX4			
t_{PLH}	Propagation Delay, DO to PAD	0.53	1.69	2.85	0.02	0.53	2.25	3.98	0.03
t_{PHL}		0.63	3.70	6.76	0.06	0.43	3.02	5.62	0.05
t_r	Output Rise Time, PAD	0.28	5.41	10.55	0.10	0.26	5.31	10.37	0.10
t_f	Output Fall Time, PAD	0.30	4.08	7.87	0.08	0.18	4.84	9.50	0.09
		ON8				ONLX8			
t_{PLH}	Propagation Delay, DO to PAD	0.37	1.06	1.75	0.01	0.71	1.84	2.98	0.02
t_{PHL}		0.84	2.76	4.68	0.04	0.73	2.18	3.63	0.03
t_r	Output Rise Time, PAD	0.21	3.13	6.06	0.06	0.53	3.46	6.40	0.06
t_f	Output Fall Time, PAD	0.46	3.29	6.11	0.06	0.48	2.79	5.10	0.05

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON16				ONLX16			
t_{PLH}	Propagation Delay, DO to PAD	0.40	0.91	1.42	0.01	0.70	1.83	2.96	0.02
t_{PHL}		0.73	2.02	3.30	0.03	0.54	1.37	2.19	0.02
t_r	Output Rise Time, PAD	0.36	2.09	3.81	0.03	0.50	3.44	6.38	0.06
t_f	Output Fall Time, PAD	0.42	1.87	3.32	0.03	0.39	1.59	2.79	0.02
		ON32							
t_{PLH}	Propagation Delay, DO to PAD	0.14	0.44	0.74	0.01	N/A			
t_{PHL}		0.67	1.41	2.15	0.01				
t_r	Output Rise Time, PAD	0.38	1.33	2.29	0.02				
t_f	Output Fall Time, PAD	0.72	1.33	1.93	0.01				

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX2				ONL2			
t_{PLH}	Propagation Delay, DO to PAD	0.59	2.85	5.11	0.05	0.52	5.48	10.43	0.10
t_{PHL}		1.01	9.96	18.91	0.18	0.57	9.23	17.90	0.17
t_r	Output Rise Time, PAD	0.49	10.87	21.26	0.21	0.32	14.63	28.93	0.29
t_f	Output Fall Time, PAD	0.54	12.10	23.66	0.23	0.31	14.40	28.49	0.28
		ONX4				ONL4			
t_{PLH}	Propagation Delay, DO to PAD	0.92	2.08	3.25	0.02	0.72	3.21	5.69	0.05
t_{PHL}		0.95	5.51	10.07	0.09	0.76	3.68	6.60	0.06
t_r	Output Rise Time, PAD	0.47	5.58	10.68	0.10	0.32	7.43	14.53	0.14
t_f	Output Fall Time, PAD	0.36	6.11	11.87	0.12	0.35	4.96	9.58	0.09
		ONX8				ONL8			
t_{PLH}	Propagation Delay, DO to PAD	0.85	1.70	2.54	0.02	0.55	1.99	3.42	0.03
t_{PHL}		1.27	3.64	6.01	0.05	1.00	2.85	4.70	0.04
t_r	Output Rise Time, PAD	0.70	3.57	6.43	0.06	0.25	4.28	8.32	0.08
t_f	Output Fall Time, PAD	0.58	3.40	6.23	0.06	0.56	3.98	7.41	0.07
		N/A				ONL16			
t_{PLH}	Propagation Delay, DO to PAD					0.65	1.61	2.57	0.02
t_{PHL}						0.87	2.13	3.38	0.03
t_r	Output Rise Time, PAD					0.46	2.80	5.15	0.05
t_f	Output Fall Time, PAD					0.52	2.26	4.01	0.03

Output Buffers with Slew Rate Control (S2) (5 V System/Core Voltage)

5/5 V
n=4, 8, 16 or 32

ONnS2

MACRO	SECTIONS USED
All	0/1

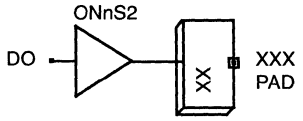
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD / DO

MACRO	INPUT CAP.
ON4S2	DO: 0.39pF
ON8S2	DO: 0.60pF
ON16S2	DO: 0.90pF
ON32S2	DO: 1.66pF

Function Table

DO	PAD
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ON4S2			
t_{PLH}	Propagation Delay, DO to PAD	1.30	3.66	6.01	0.05
t_{PHL}		1.04	3.08	5.13	0.04
t_r	Output Rise Time, PAD	0.61	5.69	10.77	0.10
t_f	Output Fall Time, PAD	0.48	4.24	7.99	0.08
		ON8S2			
t_{PLH}	Propagation Delay, DO to PAD	1.11	2.62	4.12	0.03
t_{PHL}		1.22	2.61	4.01	0.03
t_r	Output Rise Time, PAD	0.70	3.60	6.49	0.06
t_f	Output Fall Time, PAD	0.66	3.50	6.33	0.06
		ON16S2			
t_{PLH}	Propagation Delay, DO to PAD	1.25	2.31	3.36	0.02
t_{PHL}		1.02	2.01	3.00	0.02
t_r	Output Rise Time, PAD	0.69	2.48	4.26	0.04
t_f	Output Fall Time, PAD	0.56	2.04	3.53	0.03
		ON32S2			
t_{PLH}	Propagation Delay, DO to PAD	1.15	1.80	2.46	0.01
t_{PHL}		0.92	1.50	2.07	0.01
t_r	Output Rise Time, PAD	0.98	1.80	2.62	0.02
t_f	Output Fall Time, PAD	0.76	1.49	2.22	0.01

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ON4S2			
t_{PLH}	Propagation Delay, DO to PAD	1.13	2.42	3.70	0.03
t_{PHL}		1.13	4.25	7.37	0.06
t_r	Output Rise Time, PAD	0.61	5.69	10.77	0.10
t_f	Output Fall Time, PAD	0.48	4.24	7.99	0.08
		ON8S2			
t_{PLH}	Propagation Delay, DO to PAD	0.89	1.79	2.70	0.02
t_{PHL}		1.35	3.38	5.40	0.04
t_r	Output Rise Time, PAD	0.70	3.60	6.49	0.06
t_f	Output Fall Time, PAD	0.66	3.50	6.33	0.06
		ON16S2			
t_{PLH}	Propagation Delay, DO to PAD	1.04	1.71	2.39	0.01
t_{PHL}		1.14	2.54	3.93	0.03
t_r	Output Rise Time, PAD	0.69	2.48	4.26	0.04
t_f	Output Fall Time, PAD	0.56	2.04	3.53	0.03
		ON32S2			
t_{PLH}	Propagation Delay, DO to PAD	0.93	1.35	1.76	0.01
t_{PHL}		1.18	1.91	2.65	0.01
t_r	Output Rise Time, PAD	0.98	1.80	2.62	0.02
t_f	Output Fall Time, PAD	0.76	1.49	2.22	0.01

NOTE:
The H4CPlus Series user has the option to configure outputs with slew rate control to slow down the output edge rates of signals going off-chip. This feature helps to decrease system noise and overshoot/undershoot of the output signals caused by fast rise or fall times. The S2 option has up to 10% reduction in slew rate.

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3-State Outputs and Bidirectional Outputs (3.3 V and 5 V System/Core Voltage)

5/5 V ONnT/BONnT
5/3.3 V ONXnT/BONXnT
3.3/5 V ONLXnT/BONLXnT
3.3/3.3 V ONLnT/BONLnT
n=2, 4, 8, 16 or 32

MACRO	SECTIONS USED
ONnT/ONXnT/ONLXnT/ONLnT	0/1
BONnT/BONXnT/BONLXnT/BONLnT	0/1

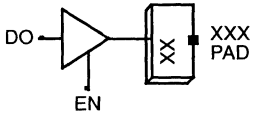
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ONnT/ONXnT/ONLXnT/ONLnT	PAD / DO,EN
BONnT/BONXnT/BONLXnT/BONLnT	BIC / DO,EN

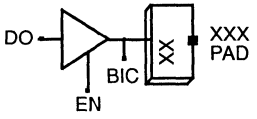
MACRO	INPUT CAP.
ON2T,BON2T,ON4T,BON4T,ON8T,BON8T, ONX2T,BONX2T,ONX4T,BONX4T,ONX8T,BONX8T, ONLX2T,BONLX2T,ONLX4T,BONLX4T,ONLX8T, BONLX8T,ONL2T,BONL2T,ONL4T,BONL4T, ONL8T,BONL8T	DO: 0.24pF EN: 0.19pF
ON16T,BON16T,ONLX16T,BONLX16T, ONL16T,BONL16T	DO,EN: 0.24pF

MACRO	OUTPUT CAP.
ON2T,BON2T,ON4T,BON4T,ONX2T,BONX2T, ONX4T,BONX4T,ONLX2T,BONLX2T,ONLX4T, BONLX4T,ONL2T,BONL2T,ONL4T,BONL4T	PAD: 4.96pF
ON8T,BON8T,ONX8T,BONX8T,ONL8T,BONL8T	PAD: 5.10pF
ON16T,BON16T,ONLX8T,BONLX8T,ONLX16T, BONLX16T,ONL16T,BONL16T	PAD: 5.76pF
ON32T,BON32T	PAD: 9.52pF

ONnT / ONXnT / ONLXnT / ONLnT



BONnT / BONXnT / BONLXnT / BONLnT



Function Table

DO	EN	PAD
L	L	Z
L	H	L
H	L	Z
H	H	H

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON2T/BON2T				ONLX2T/BONLX2T			
t_{PLH}	Propagation Delay, DO to PAD	0.64	5.15	9.66	0.09	1.10	5.05	9.00	0.08
t_{PHL}		0.66	6.54	12.43	0.12	0.64	4.76	8.88	0.08
t_{PLZ}	Propagation Delay, EN to PAD	0.34	0.34	0.35	0.00	0.62	0.63	0.63	0.00
t_{PZL}		0.47	6.35	12.24	0.12	0.52	4.64	8.76	0.08
t_{PZH}	Propagation Delay, EN to PAD	0.56	5.07	9.58	0.09	1.03	4.98	8.93	0.08
t_{PHZ}		0.64	0.64	0.65	0.00	1.03	1.03	1.04	0.00
t_r	Output Rise Time, PAD	0.23	10.60	20.98	0.21	0.42	9.27	18.12	0.18
t_f	Output Fall Time, PAD	0.24	11.79	23.35	0.23	0.19	9.54	18.89	0.19
		ON4T/BON4T				ONLX4T/BONLX4T			
t_{PLH}	Propagation Delay, DO to PAD	0.84	3.11	5.37	0.05	0.91	3.15	5.39	0.04
t_{PHL}		0.85	2.84	4.82	0.04	0.80	2.87	4.93	0.04
t_{PLZ}	Propagation Delay, EN to PAD	0.78	0.79	0.79	0.00	0.84	0.85	0.85	0.00
t_{PZL}		0.69	2.68	4.66	0.04	0.75	2.81	4.88	0.04
t_{PZH}	Propagation Delay, EN to PAD	0.77	3.03	5.30	0.05	0.83	3.07	5.31	0.04
t_{PHZ}		0.77	0.77	0.78	0.00	0.83	0.83	0.84	0.00
t_r	Output Rise Time, PAD	0.31	5.38	10.44	0.10	0.31	5.34	10.37	0.10
t_f	Output Fall Time, PAD	0.32	4.07	7.83	0.08	0.30	3.38	6.47	0.06

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON8T/BON8T				ONLX8T/BONLX8T			
t_{PLH}	Propagation Delay, DO to PAD	0.78	2.09	3.40	0.03	1.08	2.50	3.92	0.03
t_{PHL}		0.87	2.15	3.44	0.03	0.80	1.99	3.19	0.02
t_{PLZ}	Propagation Delay, EN to PAD	0.62	0.62	0.63	0.00	0.84	0.85	0.85	0.00
t_{PZL}		0.66	1.95	3.23	0.03	0.74	1.94	3.13	0.02
t_{PZH}	Propagation Delay, EN to PAD	0.69	2.00	3.31	0.03	0.99	2.41	3.83	0.03
t_{PHZ}		0.96	0.96	0.97	0.00	0.99	0.99	1.00	0.00
t_r	Output Rise Time, PAD	0.22	3.15	6.08	0.06	0.48	3.52	6.56	0.06
t_f	Output Fall Time, PAD	0.34	2.77	5.20	0.05	0.30	2.36	4.42	0.04
		ON16T/BON16T				ONLX16T/BONLX16T			
t_{PLH}	Propagation Delay, DO to PAD	0.82	1.70	2.57	0.02	0.99	2.41	3.83	0.03
t_{PHL}		0.97	1.86	2.75	0.02	0.79	1.49	2.19	0.01
t_{PLZ}	Propagation Delay, EN to PAD	0.68	0.68	0.69	0.00	0.80	0.80	0.81	0.00
t_{PZL}		0.67	1.56	2.45	0.02	0.71	1.41	2.11	0.01
t_{PZH}	Propagation Delay, EN to PAD	0.72	1.59	2.47	0.02	0.89	2.31	3.73	0.03
t_{PHZ}		1.14	1.14	1.15	0.00	0.89	0.89	0.90	0.00
t_r	Output Rise Time, PAD	0.29	2.17	4.04	0.04	0.44	3.49	6.54	0.06
t_f	Output Fall Time, PAD	0.33	1.95	3.56	0.03	0.30	1.67	3.05	0.03
		ON32T/BON32T				N/A			
t_{PLH}	Propagation Delay, DO to PAD	1.04	1.55	2.06	0.01				
t_{PHL}		1.07	1.60	2.13	0.01				
t_{PLZ}	Propagation Delay, EN to PAD	0.97	0.97	0.98	0.00				
t_{PZL}		0.87	1.40	1.93	0.01				
t_{PZH}	Propagation Delay, EN to PAD	0.93	1.44	1.95	0.01				
t_{PHZ}		0.95	0.95	0.96	0.00				
t_r	Output Rise Time, PAD	0.37	1.36	2.35	0.02				
t_f	Output Fall Time, PAD	0.73	1.33	1.92	0.01				

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX2T/BONX2T				ONL2T/BONL2T			
t_{PLH}	Propagation Delay, DO to PAD	1.33	5.84	10.34	0.09	0.92	7.32	13.72	0.13
t_{PHL}		1.81	7.70	13.59	0.12	0.89	7.94	14.99	0.14
t_{PLZ}	Propagation Delay, EN to PAD	0.83	0.84	0.84	0.00	0.75	0.75	0.76	0.00
t_{PZL}		1.59	7.48	13.37	0.12	0.67	7.72	14.77	0.14
t_{PZH}	Propagation Delay, EN to PAD	1.22	5.72	10.23	0.09	0.81	7.21	13.61	0.13
t_{PHZ}		1.20	1.21	1.21	0.00	0.79	0.80	0.80	0.00
t_r	Output Rise Time, PAD	0.49	10.88	21.27	0.21	0.33	14.62	28.92	0.29
t_f	Output Fall Time, PAD	0.54	12.11	23.68	0.23	0.31	14.39	28.46	0.28

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX4T/BONX4T				ONL4T/BONL4T			
t_{PLH}	Propagation Delay, DO to PAD	1.65	3.92	6.19	0.05	1.18	4.39	7.59	0.06
t_{PHL}		1.97	4.92	7.88	0.06	1.16	3.55	5.93	0.05
t_{PLZ}	Propagation Delay, EN to PAD	0.98	0.99	0.99	0.00	1.01	1.02	1.02	0.00
t_{PZL}		1.73	4.69	7.64	0.06	0.93	3.32	5.70	0.05
t_{PZH}	Propagation Delay, EN to PAD	1.54	3.81	6.08	0.05	1.06	4.27	7.47	0.06
t_{PHZ}		1.48	1.48	1.49	0.00	1.04	1.04	1.05	0.00
t_r	Output Rise Time, PAD	0.47	5.58	10.69	0.10	0.38	7.37	14.36	0.14
t_f	Output Fall Time, PAD	0.37	6.13	11.88	0.12	0.38	4.94	9.50	0.09
		ONX8T/BONX8T				ONL8T/BONL8T			
t_{PLH}	Propagation Delay, DO to PAD	1.96	3.40	4.85	0.03	1.15	2.99	4.83	0.04
t_{PHL}		1.99	3.58	5.17	0.03	1.17	2.71	4.25	0.03
t_{PLZ}	Propagation Delay, EN to PAD	1.17	1.18	1.18	0.00	1.00	1.01	1.01	0.00
t_{PZL}		1.76	3.35	4.94	0.03	0.92	2.46	4.00	0.03
t_{PZH}	Propagation Delay, EN to PAD	1.85	3.29	4.74	0.03	1.03	2.87	4.71	0.04
t_{PHZ}		1.67	1.67	1.68	0.00	1.01	1.01	1.02	0.00
t_r	Output Rise Time, PAD	0.84	3.63	6.43	0.06	0.28	4.29	8.30	0.08
t_f	Output Fall Time, PAD	0.58	3.40	6.22	0.06	0.42	3.36	6.30	0.06
		N/A				ONL16T/BONL16T			
t_{PLH}	Propagation Delay, DO to PAD					1.21	2.40	3.58	0.02
t_{PHL}						1.29	2.35	3.42	0.02
t_{PLZ}	Propagation Delay, EN to PAD					1.01	1.02	1.02	0.00
t_{PZL}						0.94	2.00	3.07	0.02
t_{PZH}	Propagation Delay, EN to PAD					1.08	2.26	3.45	0.02
t_{PHZ}						1.06	1.06	1.07	0.00
t_r	Output Rise Time, PAD					0.38	2.88	5.39	0.05
t_f	Output Fall Time, PAD					0.42	2.35	4.27	0.04

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TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON2T/BON2T				ONLX2T/BONLX2T			
t_{PLH}	Propagation Delay, DO to PAD	0.59	2.86	5.13	0.05	1.06	4.09	7.13	0.06
t_{PHL}		0.72	9.85	18.98	0.18	0.66	5.83	11.01	0.10
t_{PLZ}	Propagation Delay, EN to PAD	0.65	0.65	0.66	0.00	0.65	0.65	0.66	0.00
t_{PZL}		0.55	9.68	18.81	0.18	0.55	5.72	10.90	0.10
t_{PZH}	Propagation Delay, EN to PAD	0.51	2.78	5.05	0.05	0.98	4.02	7.05	0.06
t_{PHZ}		0.51	0.52	0.52	0.00	0.98	0.99	0.99	0.00
t_r	Output Rise Time, PAD	0.23	10.60	20.98	0.21	0.42	9.27	18.12	0.18
t_f	Output Fall Time, PAD	0.24	11.79	23.35	0.23	0.19	9.54	18.89	0.19

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON4T/BON4T				ONLX4T/BONLX4T			
t_{PLH}	Propagation Delay, DO to PAD	0.76	1.92	3.08	0.02	0.88	2.60	4.33	0.03
t_{PHL}		0.92	3.99	7.05	0.06	0.83	3.43	6.02	0.05
t_{PLZ}	Propagation Delay, EN to PAD	0.86	0.86	0.87	0.00	0.86	0.87	0.87	0.00
t_{PZL}		0.77	3.83	6.90	0.06	0.77	3.37	5.96	0.05
t_{PZH}	Propagation Delay, EN to PAD	0.67	1.83	2.99	0.02	0.79	2.52	4.24	0.03
t_{PHZ}		0.67	0.68	0.68	0.00	0.79	0.80	0.80	0.00
t_r	Output Rise Time, PAD	0.31	5.38	10.44	0.10	0.31	5.34	10.37	0.10
t_f	Output Fall Time, PAD	0.32	4.07	7.83	0.08	0.30	3.38	6.47	0.06
		ON8T/BON8T				ONLX8T/BONLX8T			
t_{PLH}	Propagation Delay, DO to PAD	0.76	1.92	3.08	0.02	1.02	2.15	3.29	0.02
t_{PHL}		0.92	3.99	7.05	0.06	0.83	2.28	3.73	0.03
t_{PLZ}	Propagation Delay, EN to PAD	0.86	0.86	0.87	0.00	0.87	0.88	0.88	0.00
t_{PZL}		0.77	3.83	6.90	0.06	0.77	2.22	3.67	0.03
t_{PZH}	Propagation Delay, EN to PAD	0.67	1.83	2.99	0.02	0.93	2.06	3.20	0.02
t_{PHZ}		0.67	0.68	0.68	0.00	0.93	0.93	0.94	0.00
t_r	Output Rise Time, PAD	0.31	5.38	10.44	0.10	0.48	3.52	6.56	0.06
t_f	Output Fall Time, PAD	0.32	4.07	7.83	0.08	1.02	2.15	3.29	0.02
		ON16T/BON16T				ONLX16T/BONLX16T			
t_{PLH}	Propagation Delay, DO to PAD	0.74	1.25	1.76	0.01	0.93	2.06	3.19	0.02
t_{PHL}		1.04	2.33	3.61	0.03	0.82	1.65	2.47	0.02
t_{PLZ}	Propagation Delay, EN to PAD	0.68	0.68	0.69	0.00	0.82	0.83	0.83	0.00
t_{PZL}		0.76	2.05	3.33	0.03	0.73	1.56	2.38	0.02
t_{PZH}	Propagation Delay, EN to PAD	0.63	1.14	1.65	0.01	0.83	1.96	3.09	0.02
t_{PHZ}		1.14	1.14	1.15	0.00	0.83	0.84	0.84	0.00
t_r	Output Rise Time, PAD	0.29	2.17	4.04	0.04	0.44	3.49	6.54	0.06
t_f	Output Fall Time, PAD	0.33	1.95	3.56	0.03	0.30	1.67	3.05	0.03
		ON32T/BON32T				N/A			
t_{PLH}	Propagation Delay, DO to PAD	0.93	1.24	1.56	0.01				
t_{PHL}		1.29	1.95	2.62	0.01				
t_{PLZ}	Propagation Delay, EN to PAD	1.11	1.12	1.12	0.00				
t_{PZL}		1.02	1.69	2.35	0.01				
t_{PZH}	Propagation Delay, EN to PAD	0.82	1.13	1.45	0.01				
t_{PHZ}		0.83	0.83	0.84	0.00				
t_r	Output Rise Time, PAD	0.37	1.36	2.35	0.02				
t_f	Output Fall Time, PAD	0.73	1.33	1.92	0.01				

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TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX2T/BONX2T				ONL2T/BONL2T			
t_{PLH}	Propagation Delay, DO to PAD	1.23	3.49	5.76	0.05	0.89	5.84	10.80	0.10
t_{PHL}		1.97	11.10	20.24	0.18	0.93	9.60	18.26	0.17
t_{PLZ}	Propagation Delay, EN to PAD	0.83	0.84	0.84	0.00	0.79	0.80	0.80	0.00
t_{PZL}		1.78	10.92	20.05	0.18	0.71	9.37	18.04	0.17
t_{PZH}	Propagation Delay, EN to PAD	1.10	3.37	5.63	0.05	0.78	5.73	10.69	0.10
t_{PHZ}		1.20	1.21	1.21	0.00	0.76	0.76	0.77	0.00
t_r	Output Rise Time, PAD	0.49	10.88	21.27	0.21	0.33	14.62	28.92	0.29
t_f	Output Fall Time, PAD	0.54	12.11	23.68	0.23	0.31	14.39	28.46	0.28
		ONX4T/BONX4T				ONL4T/BONL4T			
t_{PLH}	Propagation Delay, DO to PAD	1.55	2.72	3.88	0.02	1.15	3.63	6.12	0.05
t_{PHL}		2.07	6.65	11.23	0.09	1.20	4.12	7.04	0.06
t_{PLZ}	Propagation Delay, EN to PAD	0.98	0.99	0.99	0.00	1.05	1.05	1.06	0.00
t_{PZL}		1.84	6.42	11.00	0.09	0.97	3.89	6.81	0.06
t_{PZH}	Propagation Delay, EN to PAD	1.43	2.60	3.76	0.02	1.02	3.51	5.99	0.05
t_{PHZ}		1.48	1.48	1.49	0.00	1.00	1.01	1.01	0.00
t_r	Output Rise Time, PAD	0.47	5.58	10.69	0.10	0.38	7.37	14.36	0.14
t_f	Output Fall Time, PAD	0.37	6.13	11.88	0.12	0.38	4.94	9.50	0.09
		ONX8T/BONX8T				ONL8T/BONL8T			
t_{PLH}	Propagation Delay, DO to PAD	1.96	3.40	4.85	0.03	1.11	2.55	3.98	0.03
t_{PHL}		1.99	3.58	5.17	0.03	1.22	3.07	4.92	0.04
t_{PLZ}	Propagation Delay, EN to PAD	1.17	1.18	1.18	0.00	1.06	1.06	1.07	0.00
t_{PZL}		1.76	3.35	4.94	0.03	0.97	2.82	4.67	0.04
t_{PZH}	Propagation Delay, EN to PAD	1.85	3.29	4.74	0.03	0.99	2.42	3.86	0.03
t_{PHZ}		1.67	1.67	1.68	0.00	0.97	0.98	0.98	0.00
t_r	Output Rise Time, PAD	0.84	3.63	6.43	0.06	0.28	4.29	8.30	0.08
t_f	Output Fall Time, PAD	0.58	3.40	6.22	0.06	0.42	3.36	6.30	0.06
		N/A				ONL16T/BONL16T			
t_{PLH}	Propagation Delay, DO to PAD					1.17	2.13	3.09	0.02
t_{PHL}						1.33	2.59	3.84	0.03
t_{PLZ}	Propagation Delay, EN to PAD					1.06	1.07	1.07	0.00
t_{PZL}						0.99	2.24	3.50	0.03
t_{PZH}	Propagation Delay, EN to PAD					1.03	1.99	2.95	0.02
t_{PHZ}						1.01	1.02	1.02	0.00
t_r	Output Rise Time, PAD					0.38	2.88	5.39	0.05
t_f	Output Fall Time, PAD					0.42	2.35	4.27	0.04

3-State Outputs and Bidirectional Outputs with Slew Rate Control (S2) (5 V System/Core Voltage)

5/5 V
n=4, 8, or 16

ONnTS2
BONnTS2

MACRO	SECTIONS USED
ON4TS2,ON8TS2,ON16TS2	0/1
BON4TS2,BON8TS2,BON16TS2	0/1

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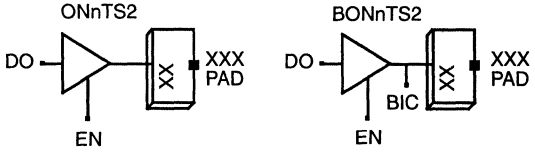
MACRO	OUTPUTS/INPUTS
ON4TS2,ON8TS2,ON16TS2	PAD / DO,EN
BON4TS2,BON8TS2,BON16TS2	BIC / DO,EN

MACRO	INPUT CAP.
ON4TS2,BON4TS2,ON8TS2, BON8TS2	DO: 0.24pF EN: 0.19pF
ON16TS2,BON16TS2	DO,EN: 0.24pF

MACRO	OUTPUT CAP.
ON4TS2,BON4TS2	PAD: 4.96pF
ON8TS2,BON8TS2	PAD: 5.10pF
ON16TS2,BON16TS2	PAD: 5.76pF
ON32TS2,BON32TS2	PAD: 9.52pF



Function Table

DO	EN	PAD
L	L	Z
L	H	L
H	L	Z
H	H	H

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ON4TS2/BON4TS2			
t_{PLH}	Propagation Delay, DO to PAD	1.32	4.07	6.81	0.05
t_{PHL}		1.16	3.54	5.93	0.05
t_{PLZ}	Propagation Delay, EN to PAD	1.10	1.11	1.11	0.00
t_{PZL}		1.01	3.44	5.87	0.05
t_{PZH}	Propagation Delay, EN to PAD	1.25	4.04	6.83	0.06
t_{PHZ}		1.25	1.26	1.26	0.00
t_r	Output Rise Time, PAD	0.57	5.72	10.87	0.10
t_f	Output Fall Time, PAD	0.45	4.28	8.11	0.08
		ON8TS2/BON8TS2			
t_{PLH}	Propagation Delay, DO to PAD	1.18	2.69	4.19	0.03
t_{PHL}		1.29	2.68	4.08	0.03
t_{PLZ}	Propagation Delay, EN to PAD	1.21	1.21	1.22	0.00
t_{PZL}		1.12	2.51	3.91	0.03
t_{PZH}	Propagation Delay, EN to PAD	1.11	2.61	4.12	0.03
t_{PHZ}		1.10	1.11	1.11	0.00
t_r	Output Rise Time, PAD	0.62	3.71	6.80	0.06
t_f	Output Fall Time, PAD	0.54	3.62	6.71	0.06

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ON16TS2/BON16TS2			
t_{PLH}	Propagation Delay, DO to PAD	1.35	2.40	3.46	0.02
t_{PHL}		1.20	2.19	3.18	0.02
t_{PLZ}	Propagation Delay, EN to PAD	1.06	1.06	1.07	0.00
t_{PZL}		0.97	1.96	2.95	0.02
t_{PZH}	Propagation Delay, EN to PAD	1.25	2.31	3.36	0.02
t_{PHZ}		1.26	1.26	1.27	0.00
t_r	Output Rise Time, PAD	0.55	2.62	4.70	0.04
t_f	Output Fall Time, PAD	0.42	2.19	3.95	0.04
		ON32TS2/BON32TS2			
t_{PLH}	Propagation Delay, DO to PAD	1.66	2.30	2.94	0.01
t_{PHL}		1.39	1.97	2.55	0.01
t_{PLZ}	Propagation Delay, EN to PAD	1.26	1.27	1.27	0.00
t_{PZL}		1.17	1.75	2.33	0.01
t_{PZH}	Propagation Delay, EN to PAD	1.57	2.21	2.85	0.01
t_{PHZ}		1.59	1.59	1.60	0.00
t_r	Output Rise Time, PAD	0.76	1.70	2.63	0.02
t_f	Output Fall Time, PAD	0.75	1.46	2.17	0.01

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ON4TS2/BON4TS2			
t_{PLH}	Propagation Delay, DO to PAD	1.15	2.83	4.50	0.03
t_{PHL}		1.26	4.70	8.15	0.07
t_{PLZ}	Propagation Delay, EN to PAD	1.21	1.22	1.22	0.00
t_{PZL}		1.12	4.66	8.21	0.07
t_{PZH}	Propagation Delay, EN to PAD	1.07	2.76	4.45	0.03
t_{PHZ}		1.07	1.07	1.08	0.00
t_r	Output Rise Time, PAD	0.57	5.72	10.87	0.10
t_f	Output Fall Time, PAD	0.45	4.28	8.11	0.08
		ON8TS2/BON8TS2			
t_{PLH}	Propagation Delay, DO to PAD	1.00	1.90	2.81	0.02
t_{PHL}		1.41	3.43	5.46	0.04
t_{PLZ}	Propagation Delay, EN to PAD	1.35	1.35	1.36	0.00
t_{PZL}		1.26	3.28	5.31	0.04
t_{PZH}	Propagation Delay, EN to PAD	0.91	1.81	2.72	0.02
t_{PHZ}		0.91	0.91	0.92	0.00
t_r	Output Rise Time, PAD	0.62	3.71	6.80	0.06
t_f	Output Fall Time, PAD	0.54	3.62	6.71	0.06

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ON16TS2/BON16TS2			
t_{PLH}	Propagation Delay, DO to PAD	1.19	1.86	2.54	0.01
t_{PHL}		1.30	2.70	4.09	0.03
t_{PLZ}	Propagation Delay, EN to PAD	1.17	1.18	1.18	0.00
t_{PZL}		1.09	2.48	3.88	0.03
t_{PZH}	Propagation Delay, EN to PAD	1.08	1.76	2.43	0.01
t_{PHZ}		1.09	1.09	1.10	0.00
t_r	Output Rise Time, PAD	0.55	2.62	4.70	0.04
t_f	Output Fall Time, PAD	0.42	2.19	3.95	0.04
		ON32TS2/BON32TS2			
t_{PLH}	Propagation Delay, DO to PAD	1.46	1.87	2.29	0.01
t_{PHL}		1.62	2.37	3.12	0.01
t_{PLZ}	Propagation Delay, EN to PAD	1.56	1.56	1.57	0.00
t_{PZL}		1.48	2.23	2.98	0.01
t_{PZH}	Propagation Delay, EN to PAD	1.33	1.75	2.16	0.01
t_{PHZ}		1.34	1.34	1.35	0.00
t_r	Output Rise Time, PAD	0.76	1.70	2.63	0.02
t_f	Output Fall Time, PAD	0.75	1.46	2.17	0.01

NOTE:
The H4CPlus Series user has the option to configure outputs with slew rate control to slow down the output edge rates of signals going off-chip. This feature helps to decrease system noise and overshoot/undershoot of the output signals caused by fast rise or fall times. The S2 option has up to 10% reduction in slew rate.

Open-drain Outputs and Bidirectional Outputs (3.3 V and 5 V System/core Voltage)

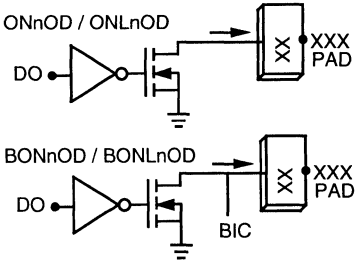
5/5 V **ONnOD/BONnOD**
3.3/3.3 V **ONLnOD/BONLnOD**
n=4, 8, 16 or 32

MACRO	SECTIONS USED
ON2OD/ON4OD/ONL4OD/ON8OD/ ONL8OD/ON16OD/ONL16OD/ ON32OD	0/1
BON4OD/BONL4OD/BON8OD/ BONL8OD/BON16OD/BONL16OD/ BON32OD	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
ON2OD/ON4OD/ONL4OD/ON8OD/ ONL8OD/ON16OD/ONL16OD/ ON32OD	PAD / DO
BON4OD/BONL4OD/BON8OD/ BONL8OD/BON16OD/BONL16OD/ BON32OD	BIC / DO

MACRO	INPUT CAP.
ON2OD	DO: 0.19pF
ON4OD/ONL4OD,	DO: 0.24pF
ON8OD/BON8OD/ONL8OD/ BNL8OD	DO: 0.30pF
ON16OD/BON16OD/ONL16OD/ BONL16OD	DO: 0.45pF
ON32OD/BON32OD	DO: 0.76pF



MACRO	OUTPUT CAP.
ON2OD/ON4OD/ONL4OD/ON8OD/ ONL8OD/ON16OD/ONL16OD/ BON4OD/BONL4OD/BON8OD/ BONL8OD/BON16OD/BONL16OD	PAD: 4.96pF
ON32OD,BON32OD	PAD: 7.92pF

Function Table

DO	PAD
L	L
H	Z

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON2OD				N/A			
t_{PLZ}	Propagation Delay, DO to PAD	0.35	0.35	0.36	0.00				
t_{PZL}		0.34	6.61	12.88	0.13				
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00				
t_f	Output Fall Time, PAD	0.29	15.45	30.62	0.30				
		ON4OD				ONL4OD			
t_{PLZ}	Propagation Delay, DO to PAD	0.47	0.47	0.48	0.00	0.59	0.59	0.60	0.00
t_{PZL}		0.46	2.66	4.86	0.04	0.75	3.14	5.52	0.05
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.36	4.37	8.37	0.08	0.77	6.01	11.25	0.10
		ON8OD/BON8OD				ONL8OD/BONL8OD			
t_{PLZ}	Propagation Delay, DO to PAD	0.40	0.40	0.41	0.00	0.57	0.57	0.58	0.00
t_{PZL}		0.40	2.05	3.70	0.03	0.67	2.26	3.85	0.03
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.37	2.91	5.45	0.05	1.10	3.80	6.50	0.05

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON16OD/BON16OD				ONL16OD/BONL16OD			
t_{PLZ}	Propagation Delay, DO to PAD	0.39	0.40	0.40	0.00	0.62	0.63	0.63	0.00
t_{PZL}		0.39	1.28	2.17	0.02	0.66	1.80	2.94	0.02
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.38	2.04	3.70	0.03	1.35	2.73	4.11	0.03
		ON32OD/BON32OD				N/A			
t_{PLZ}	Propagation Delay, DO to PAD	0.39	0.39	0.40	0.00				
t_{PZL}		0.39	0.96	1.54	0.01				
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00				
t_f	Output Fall Time, PAD	0.78	1.41	2.03	0.01				

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON2OD				N/A			
t_{PLZ}	Propagation Delay, DO to PAD	0.42	0.43	0.43	0.00				
t_{PZL}		0.42	10.62	20.81	0.20				
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00				
t_f	Output Fall Time, PAD	0.29	15.45	30.62	0.30				
		ON4OD				ONL4OD			
t_{PLZ}	Propagation Delay, DO to PAD	0.54	0.55	0.55	0.00	0.82	0.83	0.83	0.00
t_{PZL}		0.54	3.86	7.18	0.07	0.92	3.79	6.66	0.06
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.36	4.37	8.37	0.08	0.77	6.01	11.25	0.10
		ON8OD/BON8OD				ONL8OD/BONL8OD			
t_{PLZ}	Propagation Delay, DO to PAD	0.49	0.50	0.50	0.00	0.56	0.57	0.57	0.00
t_{PZL}		0.49	2.80	5.11	0.05	0.76	2.66	4.56	0.04
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.37	2.91	5.45	0.05	1.10	3.80	6.50	0.05
		ON16OD/BON16OD				ONL16OD/BONL16OD			
t_{PLZ}	Propagation Delay, DO to PAD	0.49	0.49	0.50	0.00	0.59	0.60	0.60	0.00
t_{PZL}		0.49	1.77	3.06	0.03	0.74	2.09	3.44	0.03
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.38	2.04	3.70	0.03	1.35	2.73	4.11	0.03
		ON32OD/BON32OD				N/A			
t_{PLZ}	Propagation Delay, DO to PAD	0.43	0.43	0.44	0.00				
t_{PZL}		0.52	1.31	2.11	0.02				
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00				
t_f	Output Fall Time, PAD	0.78	1.41	2.03	0.01				

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Oscillator W/ Non-Inverting Input
Oscillator W/ Clock Buffer Input
Oscillator W/ Schmitt Trigger Input
(3 V and 5 V System/Core Voltage)

5/5 V
3.3V/3.3V

OSCPB/OSCPBL
OSCPHB/OSCPHBL
OSCPSB/OSCPSBL

MACRO	SECTIONS USED
All	1/0

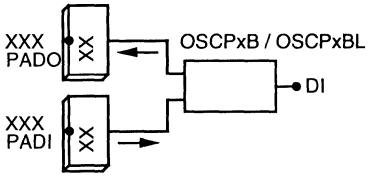
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	DI,PADO / PADI

MACRO	INPUT CAP.
All	PADI: 5.76pF

Function Table

PADI	PADO	DI
L	H	H
H	L	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		OSCPB				OSCPBL			
t_{PLH}	Propagation Delay, PADO to DI	0.33	0.34	0.37	0.09	0.46	0.47	0.51	0.13
t_{PHL}		0.36	0.37	0.41	0.14	0.52	0.54	0.59	0.17
t_r	Output Rise Time, DI	0.05	0.08	0.16	0.27	0.08	0.11	0.23	0.38
t_f	Output Fall Time, DI	0.04	0.06	0.13	0.22	0.05	0.08	0.16	0.27
		OSCPHB				OSCPHBL			
t_{PLH}	Propagation Delay, PADO to DI	0.29	0.29	0.30	0.03	0.41	0.41	0.43	0.05
t_{PHL}		0.40	0.41	0.43	0.06	0.53	0.54	0.56	0.08
t_r	Output Rise Time, DI	0.07	0.08	0.11	0.10	0.10	0.11	0.16	0.14
t_f	Output Fall Time, DI	0.07	0.08	0.11	0.10	0.09	0.10	0.14	0.12
		OSCPSB				OSCPSBL			
t_{PLH}	Propagation Delay, PADO to DI	0.73	0.73	0.75	0.03	1.00	1.01	1.02	0.05
t_{PHL}		0.99	1.00	1.02	0.06	1.38	1.39	1.41	0.08
t_r	Output Rise Time, DI	0.07	0.08	0.11	0.10	0.10	0.11	0.15	0.14
t_f	Output Fall Time, DI	0.07	0.08	0.11	0.10	0.09	0.10	0.14	0.12

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		OSCPB				OSCPBL			
t_{PLH}	Propagation Delay, PADI to PADO	0.41	3.33	6.24	0.06	0.48	3.99	7.51	0.07
t_{PHL}		0.38	2.60	4.82	0.04	0.46	3.62	6.78	0.06
t_r	Output Rise Time, PADO	0.16	5.17	10.18	0.10	0.21	7.18	14.15	0.14
t_f	Output Fall Time, PADO	0.41	3.33	6.24	0.06	0.18	6.99	13.81	0.14

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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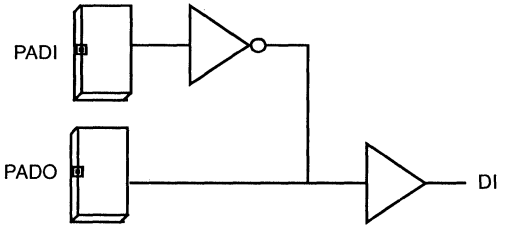
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		OSCPHB				OSCPHBL			
t_{PLH}	Propagation Delay, PADI to PADO	0.42	3.05	5.69	0.05	0.48	3.66	6.84	0.06
t_{PHL}		0.40	2.62	4.84	0.04	0.47	3.63	6.79	0.06
t_r	Output Rise Time, PADO	0.18	5.19	10.20	0.10	0.23	7.20	14.17	0.14
t_f	Output Fall Time, PADO	0.15	5.18	10.21	0.10	0.19	6.34	12.49	0.12
		OSCPSB				OSCPSBL			
t_{PLH}	Propagation Delay, PADI to PADO	0.41	3.05	5.68	0.05	0.48	3.66	6.84	0.06
t_{PHL}		0.39	2.61	4.83	0.04	0.47	3.63	6.79	0.06
t_r	Output Rise Time, PADO	0.17	5.18	10.19	0.10	0.22	7.19	14.16	0.14
t_f	Output Fall Time, PADO	0.14	5.17	10.21	0.10	0.17	6.33	12.49	0.12

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

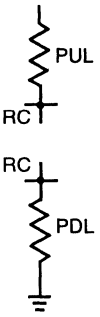
FUNCTIONAL DIAGRAM: OSCPB



7

Pull-Up Resistors / Pull-Down Resistors

PUL
PDL



The Pull-up and Pull-down resistors are used to attach to any of the input macros. Their main purpose is to keep the inputs from floating to an illegal state when they are not being driven. These resistors are not meant to replace external pull-up and pull-down resistors which are attached to a 3-state bus, or open-drain 3-state bus.
The low current option offered is used when a slower pull is desired, or when power dissipation and I_{DD} (standby current) need to be kept to a minimum. For exact breakdown of typical currents at different temperatures please see Section 8 "H4CPlus DC ELECTRICAL CHARACTERISTICS" on page 1 of that section.

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Section 7.2 Special Input/Output/Bidirectionals Macros

7.2.1 CMTL

CMTL Differential Input and Bidirectional Input (3.3 V and 5 V System/Core Voltage)

5/5 V ICMD
3/3 V BICMD
ILCMD

MACRO	SECTIONS USED
ICMD/ILCMD	1/0
BICMD	1/0

Rev. 1.07

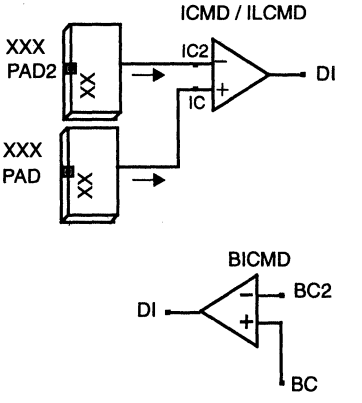
MACRO	OUTPUTS/INPUTS
ICMD/ILCMD	DI / PAD,PAD2,IC,IC2
BICMD	DI / BC,BC2

MACRO	INPUT CAP.
	PAD,PAD2: 5.06pF
BICMD	BC,BC2: 0.130F

Function Table

PAD/BC	PAD2/BC2	DI
L	H	L
H	L	H
L	L	ND
H	H	ND

ND = Not Defined



CMTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
ICMD/BICMD					
t_{PLH}	Propagation Delay, PAD,PAD2 to DI	0.88	0.89	0.93	0.11
t_{PHL}		0.83	0.85	0.89	0.15
t_r	Output Rise Time, DI	0.08	0.08	0.10	0.04
t_f	Output Fall Time, DI	0.05	0.06	0.10	0.12

CMTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)
ILCMD					
t_{PLH}	Propagation Delay, PAD,PAD2 to DI	1.22	1.24	1.29	0.17
t_{PHL}		1.27	1.29	1.34	0.19
t_r	Output Rise Time, DI	0.09	0.10	0.14	0.13
t_f	Output Fall Time, DI	0.09	0.11	0.16	0.16

CMTL Differential Output and Bidirectional Output with Active Termination (5 V System/Core Voltage)

5/5 V

OD32TCMT
BOD32TCMT

MACRO	SECTIONS USED
OD32TCMT	0/1
BOD32TCMT	0/1

Rev. 1.07

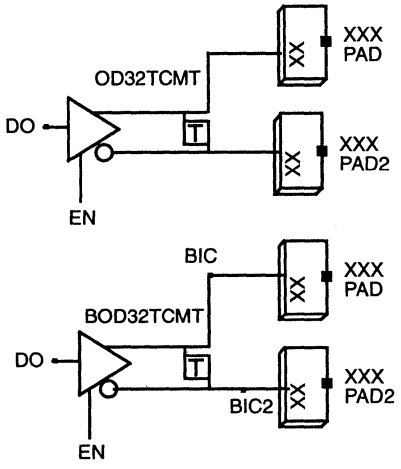
MACRO	OUTPUTS/INPUTS
OD32TCMT	PAD,PAD2 / DO,EN
BOD32TCMT	BIC,BIC2 / DO,EN

MACRO	INPUT CAP.
All	DO: 0.44pF EN: 0.24pF

MACRO	OUTPUT CAP.
All	PAD,PAD2: 4.96pF

Function Table

DO	EN	PAD	PAD2
L	L	Z	Z
L	H	L	H
H	L	Z	Z
H	H	H	L



CMTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
OD32TCMT/BOD32TCMT					
t_{PLH}	Propagation Delay, DO to PAD	0.51	2.54	4.58	0.04
t_{PHL}		0.61	1.86	3.12	0.03
t_{PLH}	Propagation Delay, DO to PAD2	0.63	1.89	3.14	0.03
t_{PHL}		0.48	2.51	4.55	0.04
t_{PLZ}	Propagation Delay, EN to PAD	0.53	0.54	0.54	0.00
t_{PZL}		1.00	2.25	3.51	0.03
t_{PZH}	Propagation Delay, EN to PAD,PAD2	1.40	3.43	5.47	0.04
t_{PHZ}		0.54	0.55	0.55	0.00
t_{PLZ}	Propagation Delay, EN to PAD2	0.56	0.57	0.57	0.00
t_{PZL}		1.00	2.25	3.51	0.03
t_r	Output Rise Time, PAD	0.91	2.96	5.00	0.04
t_f	Output Fall Time, PAD	0.54	4.73	8.92	0.08
t_r	Output Rise Time, PAD2	0.89	2.97	5.04	0.04
t_f	Output Fall Time, PAD2	0.65	5.01	9.38	0.09

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CMTL Differential Output (5 V System/ 3.3 V Core Voltage)

5/3.3 V **ODX32CM**

MACRO	SECTIONS USED
ODX32CM	0/1

Rev. 1.07

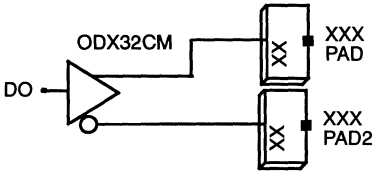
MACRO	OUTPUTS/INPUTS
ODX32CM	PAD,PAD2 / DO

MACRO	INPUT CAP.
ODX32CM	DO: 0.65pF

MACRO	OUTPUT CAP.
ODX32CM	PAD,PAD2: 4.96pF

Function Table

DO	PAD	PAD2
L	L	H
H	H	L



CMTL SWITCHING CHARACTERISTICS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)
ODX32CM					
t_{PLH}	Propagation Delay, DO to PAD	1.30	2.08	2.87	0.02
t_{PHL}		1.28	2.05	2.82	0.02
t_{PLH}	Propagation Delay, DO to PAD2	1.14	1.90	2.66	0.02
t_{PHL}		1.19	1.94	2.69	0.01
t_r	Output Rise Time, PAD	0.39	3.14	5.90	0.06
t_f	Output Fall Time, PAD	0.58	2.53	4.49	0.04
t_r	Output Rise Time, PAD2	0.23	2.96	5.68	0.05
t_f	Output Fall Time, PAD2	0.47	2.40	4.32	0.04

7

CMTL 3-State Differential Output (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/5 V
3.3/3.3 V

OD32CMT
ODLX32CMT
ODL32CMT

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

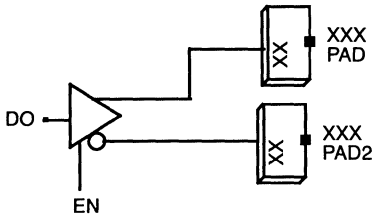
MACRO	OUTPUTS/INPUTS
All	PAD,PAD2 / DO,EN

MACRO	INPUT CAP.
All	DO: 0.44pF EN: 0.24pF

MACRO	OUTPUT CAP.
All	PAD,PAD2: 4.96pF

Function Table

DO	PAD	PAD2
L	L	H
H	H	L



OD32CMT / ODLX32CMT / ODL32CMT

CMTL SWITCHING CHARACTERISTICS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		OD32CMT				ODLX32CMT			
t_{PLH}	Propagation Delay, DO to PAD	0.63	1.34	2.05	0.01	0.72	1.69	2.66	0.02
t_{PHL}		0.56	1.24	1.93	0.01	0.74	1.64	2.53	0.02
t_{PLH}	Propagation Delay, DO to PAD2	0.59	1.27	1.96	0.01	0.98	1.92	2.87	0.02
t_{PHL}		0.59	1.30	2.01	0.01	1.08	2.01	2.94	0.02
t_{PLZ}	Propagation Delay, EN to PAD	0.46	0.47	0.47	0.00	0.52	0.53	0.53	0.00
t_{PZL}		1.13	1.81	2.50	0.01	1.45	2.66	3.87	0.02
t_{PZH}	Propagation Delay, EN to PAD,PAD2	1.67	2.38	3.09	0.01	2.30	3.48	4.65	0.02
t_{PHZ}		0.46	0.46	0.47	0.00	0.64	0.64	0.65	0.00
t_{PLZ}	Propagation Delay, EN to PAD2	0.48	0.49	0.49	0.00	0.60	0.60	0.61	0.00
t_{PZL}		1.13	1.81	2.50	0.01	1.45	2.66	3.87	0.02
t_r	Output Rise Time, PAD	1.18	2.45	3.72	0.03	1.75	3.80	5.84	0.04
t_f	Output Fall Time, PAD	0.62	2.35	4.09	0.03	0.91	2.84	4.78	0.04
t_r	Output Rise Time, PAD2	1.35	2.56	3.76	0.02	1.97	3.93	5.88	0.04
t_f	Output Fall Time, PAD2	0.76	2.45	4.15	0.03	0.87	3.36	5.84	0.05

CMTL SWITCHING CHARACTERISTICS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)
ODL32CMT					
t_{PLH}	Propagation Delay, DO to PAD	0.83	1.77	2.71	0.02
t_{PHL}		0.81	1.68	2.55	0.02
t_{PLH}	Propagation Delay, DO to PAD2	1.11	2.04	2.97	0.02
t_{PHL}		1.23	2.16	3.09	0.02
t_{PLZ}	Propagation Delay, EN to PAD	0.60	0.60	0.61	0.00
t_{PZL}		1.72	2.90	4.07	0.02
t_{PZH}	Propagation Delay, EN to PAD,PAD2	2.34	3.52	4.71	0.02
t_{PHZ}		1.78	1.79	1.79	0.00
t_{PLZ}	Propagation Delay, EN to PAD2	0.68	0.69	0.69	0.00
t_{PZL}		1.72	2.90	4.07	0.02
t_r	Output Rise Time, PAD	1.76	3.39	5.02	0.03
t_f	Output Fall Time, PAD	0.87	3.26	5.65	0.05
t_r	Output Rise Time, PAD2	1.92	3.76	5.59	0.04
t_f	Output Fall Time, PAD2	1.27	3.57	5.88	0.05

7

CMTL Output (5 V System/Core Voltage) 5/5 V O32CM

MACRO	SECTIONS USED
O32CM	0/1

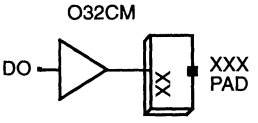
Rev. 1.07

MACRO	OUTPUTS/INPUTS
O32CM	PAD / DO

MACRO	INPUT CAP.
O32CM	DO: 0.90pF

Function Table

DO	PAD
L	L
H	H



CMTL SWITCHING CHARACTERISTICS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)
O32CM					
t_{PLH}	Propagation Delay, DO to PAD	0.51	1.17	1.82	0.01
t_{PHL}		0.45	1.24	2.04	0.02
t_r	Output Rise Time, PAD	1.36	2.78	4.21	0.03
t_f	Output Fall Time, PAD	0.75	2.30	3.85	0.03

7

7.2.2 GTL

Inverting GTL Input (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

IGI
ILGI

MACRO	SECTIONS USED
All	1/0

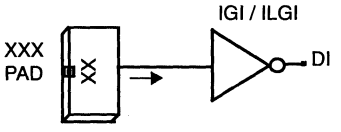
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	DI / PAD

MACRO	INPUT CAP.
All	PAD: 5.06pF

Function Table

PAD	DI
L	H
H	L



GTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		IGI				ILGI			
t_{PLH}	Propagation Delay, PAD to DI	1.00	1.01	1.04	0.10	1.34	1.35	1.40	0.15
t_{PHL}		0.90	0.92	0.97	0.16	1.34	1.36	1.42	0.20
t_r	Output Rise Time, DI	0.14	0.16	0.23	0.24	0.15	0.18	0.29	0.35
t_f	Output Fall Time, DI	0.15	0.17	0.23	0.19	0.17	0.19	0.27	0.25

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

Non-Inverting GTL Input and Bidirectional Input (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

IGN/BIGN
ILGN/BILGN

MACRO	SECTIONS USED
IGN/ILGN	1/0
BIGN/BILGN	1/0

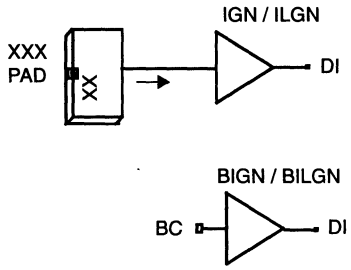
Rev. 1.07

MACRO	OUTPUTS/INPUTS
IGN/ILGN	DI / PAD
BIGN/BILGN	DI / BC

MACRO	INPUT CAP.
IGN/ILGN	PAD: 5.06pF
BIGN/BILGN	BC: 0.10pF

Function Table

PAD	DI
L	L
H	H



GTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		IGN/BIGN				ILGN/BILGN			
t_{PLH}	Propagation Delay, PAD to DI	0.95	0.96	0.99	0.11	1.32	1.33	1.37	0.15
t_{PHL}		0.90	0.92	0.97	0.15	1.26	1.28	1.34	0.20
t_r	Output Rise Time, DI	0.13	0.15	0.23	0.24	0.15	0.18	0.29	0.35
t_f	Output Fall Time, DI	0.15	0.17	0.23	0.19	0.18	0.21	0.28	0.24

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

GTL Output and Bidirectional Output (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

ON20G
BON40G
ONL20G
BONL40G

MACRO	SECTIONS USED
ON20G/ONL20G	0/1
BON40G/BONL40G	0/1

Rev. 1.07

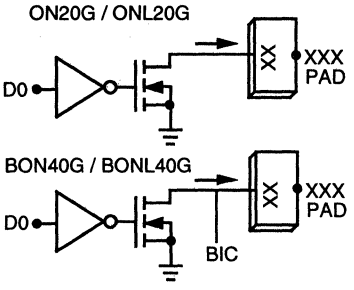
MACRO	OUTPUTS/INPUTS
ON20G/ONL20G	PAD / DO
BON40G/BONL40G	BIC / DO

MACRO	INPUT CAP.
ON20G/ONL20G	DO: 0.62pF
BON40G/BONL40G	DO: 1.09pF

MACRO	OUTPUT CAP.
ON20G/ONL20G	PAD: 4.96pF
BON40G/BONL40G	PAD: 4.96pF

Function Table

PAD	DO
L	L
H	H



GTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON20G				ONL20G			
t_{PLH}	Propagation Delay, DO to PAD	0.30	2.61	4.93	0.05	0.36	2.59	4.82	0.04
t_{PHL}		0.25	0.80	1.35	0.01	0.44	1.19	1.95	0.02
t_r	Output Rise Time, PAD	0.11	5.44	10.76	0.11	0.13	5.44	10.75	0.11
t_f	Output Fall Time, PAD	0.35	1.13	1.92	0.02	0.55	1.60	2.65	0.02
		BON40G				BONL40G			
t_{PLH}	Propagation Delay, DO to PAD	0.32	1.44	2.55	0.02	0.45	1.53	2.60	0.02
t_{PHL}		0.20	0.57	0.95	0.01	0.43	0.91	1.40	0.01
t_r	Output Rise Time, PAD	0.13	2.75	5.37	0.05	0.29	2.92	5.56	0.05
t_f	Output Fall Time, PAD	0.33	0.75	1.18	0.01	0.58	1.12	1.65	0.01

Note:
The GTL Output Switching Characteristics are specified with a pull-up resistor to 1.2 V.
ON20G and ONL20G use 50 Ohms
BON40G and BONL40G use 25 Ohms

7.2.3 PECL

PECL Differential Input (3.3 V and 5 V System/Core Voltage)

5/5 V **IPD**
5/3.3 V **IPXD**
3.3/3.3 V **ILPD**

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

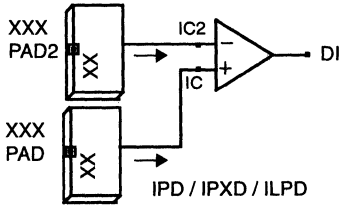
MACRO	OUTPUTS/INPUTS
All	DI / PAD,PAD2,IC,IC2

MACRO	INPUT CAP.
All	PAD,PAD2: 4.98pF

Function Table

PAD	PAD2	DI
L	L	ND
L	H	L
H	L	H
H	H	ND

ND = Not Defined



PECL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
IPD					
t_{PLH}	Propagation Delay, PAD,PAD2 to DI	0.74	0.75	0.78	0.11
t_{PHL}		0.75	0.76	0.81	0.15
t_r	Output Rise Time, DI	0.13	0.16	0.23	0.24
t_f	Output Fall Time, DI	0.12	0.14	0.20	0.20

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

PECL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		IPXD				ILPD			
t_{PLH}	Propagation Delay, PAD,PAD2 to DI	0.92	0.93	0.97	0.14	0.93	0.94	0.99	0.14
t_{PHL}		0.93	0.95	1.01	0.19	1.01	1.03	1.09	0.18
t_r	Output Rise Time, DI	0.14	0.17	0.28	0.35	0.16	0.20	0.31	0.37
t_f	Output Fall Time, DI	0.14	0.17	0.24	0.25	0.18	0.20	0.28	0.26

7.2.4 PCI

PCI Input and Bidirectional Input (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

IPCH
ILPC/ILPCH/BILPC

MACRO	SECTIONS USED
ILPC	1/0
BILPC	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
ILPC	DI / PAD,IC
BILPC	DI / BC

MACRO	INPUT CAP.
ILPC	PAD: 5.02pF
BILPC	BC: 0.06pF

MACRO	SECTIONS USED
IPCH	1/1
ILPCH	1/1

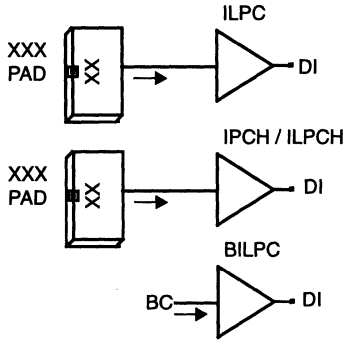
Rev. 1.07

MACRO	OUTPUTS/INPUTS
IPCH	DI / PAD,IC
ILPCH	DI / PAD,IC

MACRO	INPUT CAP.
IPCH	PAD: 5.40pF
ILPCH	PAD: 5.37pF

Function Table

PAD	DI
L	L
H	H



PCI SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=25	FO=50	K (ns/pF)	FO=0	FO=25	FO=50	K (ns/pF)
		IPCH				ILPCH			
t_{PLH}	Propagation Delay, PAD to DI	0.29	0.33	0.38	0.04	0.37	0.45	0.53	0.06
t_{PHL}		0.51	0.60	0.69	0.07	0.51	0.64	0.77	0.10
t_r	Output Rise Time, DI	0.11	0.24	0.36	0.10	0.11	0.28	0.45	0.14
t_f	Output Fall Time, DI	0.18	0.31	0.45	0.11	0.17	0.31	0.46	0.12

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

PCI SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		ILPC/BILPC			
t_{PLH}	Propagation Delay, PAD to DI	0.45	0.46	0.51	0.15
t_{PHL}		0.74	0.76	0.83	0.22
t_r	Output Rise Time, DI	0.15	0.19	0.29	0.35
t_f	Output Fall Time, DI	0.26	0.28	0.36	0.24

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

PCI Output (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3

ONPC
ONLPC

MACRO	SECTIONS USED
ONPC	0/1
ONLPC	0/1

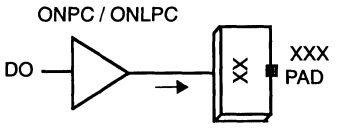
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ONPC	PAD / DO
ONLPC	PAD / DO

MACRO	INPUT CAP.
ONPC	DO: 0.68pF
ONLPC	DO: 0.90pF

Function Table

DO	PAD
L	L
H	H



PCI SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONPC				ONLPC			
t_{PLH}	Propagation Delay, DO to PAD	0.46	1.25	2.04	0.02	0.69	1.64	2.59	0.02
t_{PHL}		0.74	2.03	3.31	0.03	0.92	2.17	3.42	0.02
t_r	Output Rise Time, PAD	0.33	3.74	7.15	0.07	0.53	2.87	5.21	0.05
t_f	Output Fall Time, PAD	0.48	1.91	3.35	0.03	0.57	2.31	4.04	0.03

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

PCI 3-State Output and Bidirectional Output (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

ONTPC/BONTPC
ONLTPC/BONLTPC

MACRO	SECTIONS USED
ALL	0/1

Rev. 1.07

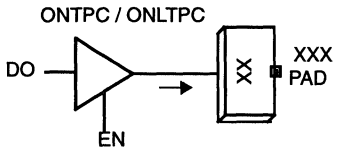
MACRO	OUTPUTS/INPUTS
ONTPC/ONLTPC	PAD / DO,EN
BONTPC/BONLTPC	BIC / DO,EN

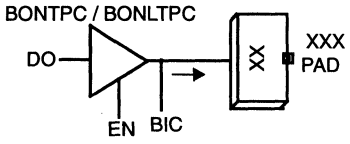
MACRO	INPUT CAP.
ALL	DO,EN: 0.24pF

MACRO	OUTPUT CAP.
ONTPC,BONTPC	PAD: 5.10pF
ONLTPC,BONLTPC	PAD: 5.76pF

Function Table

DO	EN	PAD
L	H	L
H	H	H
X	L	Z





PCI SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONTPC/BONTPC				ONLTPC/BONLTPC			
t_{PLH}	Propagation Delay, DO to PAD	0.74	1.66	2.58	0.02	1.34	2.29	3.24	0.02
t_{PHL}		1.03	2.62	4.20	0.03	1.55	2.80	4.05	0.02
t_{PLZ}	Propagation Delay, EN to PAD	0.90	0.91	0.91	0.00	1.13	1.14	1.14	0.00
t_{PZL}		0.81	2.39	3.98	0.03	1.06	2.31	3.56	0.02
t_{PZH}	Propagation Delay, EN to PAD	0.62	1.54	2.46	0.02	1.08	2.03	2.98	0.02
t_{PHZ}		0.61	0.62	0.62	0.00	1.06	1.06	1.07	0.00
t_r	Output Rise Time, PAD	0.33	3.74	7.15	0.07	0.53	2.87	5.21	0.05
t_f	Output Fall Time, PAD	0.40	1.99	3.59	0.03	0.58	2.32	4.06	0.03

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

7.2.5 CMTL -JTAG

CMTL Differential Input and Bidirectional Input -JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V ICMDJ

MACRO	SECTIONS USED
ICMDJ	1/0

Rev. 1.07

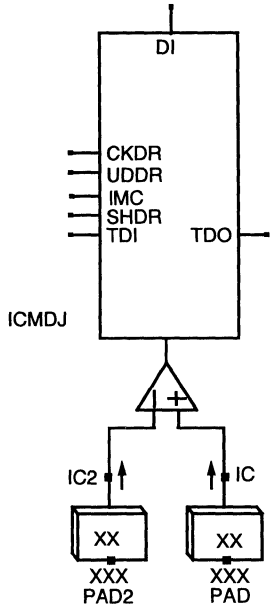
MACRO	OUTPUTS/INPUTS
ICMDJ	DI,TDO / PAD,PAD2,IC,IC2,CKDR,UDDR, IMC,SHDR,TDI

MACRO	INPUT CAP.
ICMDJ	CKDR,TDI: 0.04pF IMC,SHDR,UDDR: 0.10pF PAD,PAD2: 5.06pF

Function Table

PAD/BC	PAD2/BC2	DI
L	H	L
H	L	H
L	L	ND
H	H	ND

ND = Not Defined



CMTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
ICMDJ					
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, IMC to D	0.76	0.78	0.85	0.21
t_{PHL}		0.51	0.52	0.56	0.14
t_{PLH}	Propagation Delay, PAD,PAD2 to DI	0.97	0.99	1.02	0.12
t_{PHL}		0.93	0.95	1.00	0.18
t_{PLH}	Propagation Delay, TDO to DI	0.76	0.78	0.82	0.13
t_{PHL}		0.85	0.87	0.93	0.21
t_{PLH}	Propagation Delay, UDDR to DI	0.88	0.89	0.93	0.13
t_{PHL}		1.02	1.04	1.11	0.21
t_r	Output Rise Time, DI	0.19	0.22	0.29	0.23
t_f	Output Fall Time, DI	0.21	0.23	0.30	0.22
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

CMTL Differential Output with Active Termination -JTAG (5 V System/Core Voltage)

5/5 V

OD32TCMTJ

MACRO	SECTIONS USED
OD32TCMTJ	0/1

Rev. 1.07

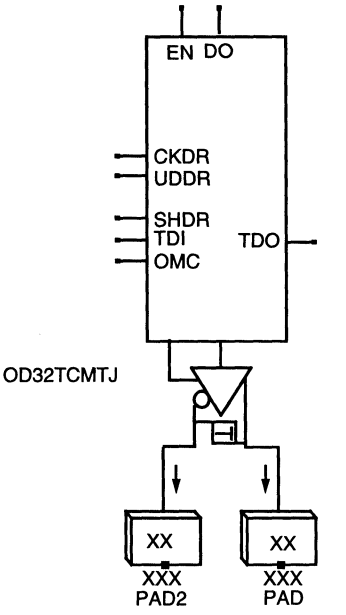
MACRO	OUTPUTS/INPUTS
OD32TCMTJ	PAD,PAD2,TDO / DO,EN,CKDR,UDDR,SHDR, TDI,OMC

MACRO	INPUT CAP.
OD32TCMTJ	CKDR,TDI: 0.04pF DO: 0.35pF EN: 0.24pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
OD32TCMTJ	PAD,PAD2: 4.96pF

Function Table

DO	EN	PAD	PAD2
L	L	Z	Z
L	H	L	H
H	L	Z	Z
H	H	H	L



CMTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
OD32TCMTJ					
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD,PAD2	1.29	2.14	2.99	0.02
t_{PHL}		1.25	2.10	2.95	0.02
t_{PLZ}	Propagation Delay, EN to PAD	1.45	1.45	1.46	0.00
t_{PZL}		1.53	2.38	3.23	0.02
t_{PZH}	Propagation Delay, EN to PAD	1.53	2.38	3.23	0.02
t_{PHZ}		1.43	1.43	1.44	0.00
t_{PLZ}	Propagation Delay, EN to PAD2	1.26	1.27	1.27	0.00
t_{PZL}		1.35	2.25	3.15	0.02
t_{PZH}	Propagation Delay, EN to PAD2	1.66	2.46	3.26	0.02
t_{PHZ}		1.56	1.57	1.57	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.55	2.40	3.25	0.02
t_{PHL}		1.46	2.31	3.16	0.02
t_{PLH}	Propagation Delay, OMC to PAD2	1.46	2.31	3.16	0.02
t_{PHL}		1.55	2.40	3.25	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.79	2.64	3.49	0.02
t_{PHL}		1.68	2.53	3.38	0.02

CMTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
t_{PLH}	Propagation Delay, TDO to PAD2	1.68	2.53	3.38	0.02
t_{PHL}		1.79	2.64	3.49	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	1.92	2.77	3.62	0.02
t_{PHL}		1.85	2.70	3.55	0.02
t_{PLH}	Propagation Delay, UDDR to PAD2	1.85	2.70	3.55	0.02
t_{PHL}		1.92	2.77	3.62	0.02
t_r	Output Rise Time, PAD	0.39	1.54	2.69	0.02
t_f	Output Fall Time, PAD	0.34	1.74	3.14	0.03
t_r	Output Rise Time, PAD2	0.37	1.57	2.77	0.02
t_f	Output Fall Time, PAD2	0.33	1.73	3.13	0.03
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

CMTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V
		Minimum Requirement
	OD32TCMTJ	
t_{su}	Set Up Time, DO,SHDR to CKDR	0.23
t_{su}	Set Up Time, TDI to CKDR	0.14
t_h	Hold Time, CKDR to DO	0.27
t_h	Hold Time, CKDR to SHDR	0.19
t_h	Hold Time, CKDR to TDI	0.32
t_w	Pulse Width, CKDR(L)	0.40
t_w	Pulse Width, CKDR(H)	0.78
t_w	Pulse Width, UDDR(H)	0.47

CMTL 3-State Differential Output -JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

OD32CMTJ
ODL32CMTJ

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

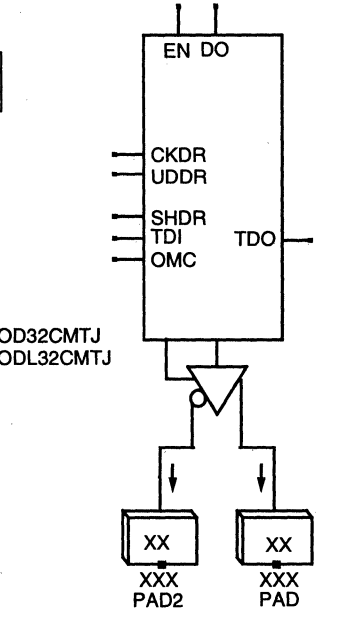
MACRO	OUTPUTS/INPUTS
All	PAD,PAD2,TDO / DO,EN,CKDR,UDDR,SHDR,TDI,OMC

MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF DO: 0.35pF EN: 0.24pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
All	PAD,PAD2: 4.96pF

Function Table

DO	PAD	PAD2
L	L	H
H	H	L



CMTL SWITCHING CHARACTERISTICS (Input Edge Rate t_r,t_f=1.00ns)

Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		OD32CMTJ				ODL32CMTJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	1.04	1.04	1.04	0.00
t_{PHL}		0.72	0.72	0.72	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.26	2.51	3.76	0.03	1.74	3.99	6.24	0.04
t_{PHL}		1.31	2.26	3.21	0.02	2.00	3.45	4.90	0.03
t_{PLH}	Propagation Delay, DO to PAD2	1.31	2.26	3.21	0.02	2.00	3.45	4.90	0.03
t_{PHL}		1.26	2.51	3.76	0.03	1.74	3.99	6.24	0.04
t_{PLZ}	Propagation Delay, EN to PAD	1.44	1.44	1.45	0.00	1.90	1.90	1.91	0.00
t_{PZL}		1.52	2.47	3.42	0.02	1.98	2.98	3.98	0.02
t_{PZH}	Propagation Delay, EN to PAD	1.52	2.47	3.42	0.02	2.02	3.02	4.02	0.02
t_{PHZ}		1.41	1.42	1.42	0.00	1.93	1.93	1.94	0.00
t_{PLZ}	Propagation Delay, EN to PAD2	1.26	1.27	1.27	0.00	1.67	1.68	1.68	0.00
t_{PZL}		1.35	2.40	3.45	0.02	1.75	2.80	3.85	0.02
t_{PZH}	Propagation Delay, EN to PAD2	1.64	2.54	3.44	0.02	2.21	3.16	4.11	0.02
t_{PHZ}		1.54	1.55	1.55	0.00	2.11	2.12	2.12	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.52	2.77	4.02	0.03	2.11	4.36	6.61	0.04
t_{PHL}		1.52	2.47	3.42	0.02	2.27	3.72	5.17	0.03

CMTL SWITCHING CHARACTERISTICS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
t_{PLH}	Propagation Delay, OMC to PAD2	1.52	2.47	3.42	0.02	2.27	3.72	5.17	0.03
t_{PHL}		1.52	2.77	4.02	0.03	2.11	4.36	6.61	0.04
t_{PLH}	Propagation Delay, TDO to PAD	1.85	2.80	3.75	0.02	2.86	4.31	5.76	0.03
t_{PHL}		1.74	2.69	3.64	0.02	2.63	4.03	5.43	0.03
t_{PLH}	Propagation Delay, TDO to PAD2	1.75	2.70	3.65	0.02	2.64	4.04	5.44	0.03
t_{PHL}		1.85	2.80	3.75	0.02	2.86	4.31	5.76	0.03
t_{PLH}	Propagation Delay, UDDR to PAD	1.89	3.14	4.39	0.03	2.65	4.90	7.15	0.04
t_{PHL}		1.92	2.87	3.82	0.02	2.85	4.25	5.65	0.03
t_{PLH}	Propagation Delay, UDDR to PAD2	1.92	2.87	3.82	0.02	2.85	4.25	5.65	0.03
t_{PHL}		1.89	3.14	4.39	0.03	2.65	4.90	7.15	0.04
t_r	Output Rise Time, PAD	0.10	1.25	2.40	0.02	0.00	1.75	3.50	0.03
t_f	Output Fall Time, PAD	0.21	1.61	3.01	0.03	0.13	2.08	4.03	0.04
t_r	Output Rise Time, PAD2	0.20	1.40	2.60	0.02	0.02	1.72	3.42	0.03
t_f	Output Fall Time, PAD2	0.14	1.55	2.95	0.03	0.00	1.95	3.90	0.04
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

CMOS TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		OD32CMTJ	ODL32CMTJ
t_{su}	Set Up Time, DO to CKDR	0.24	0.38
t_{su}	Set Up Time, SHDR to CKDR	0.24	0.43
t_{su}	Set Up Time, TDI to CKDR	0.14	0.28
t_h	Hold Time, CKDR to DO	0.27	0.38
t_h	Hold Time, CKDR to SHDR	0.19	0.25
t_h	Hold Time, CKDR to TDI	0.32	0.42
t_w	Pulse Width, CKDR(L)	0.40	0.67
t_w	Pulse Width, CKDR(H)	0.78	1.18
t_w	Pulse Width, UDDR(H)	0.47	0.64

7

7.2.6 GTL

Non-Inverting GTL Input (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

IGNJ
ILGNJ

MACRO	SECTIONS USED
IGNJ/ILGNJ	1/0

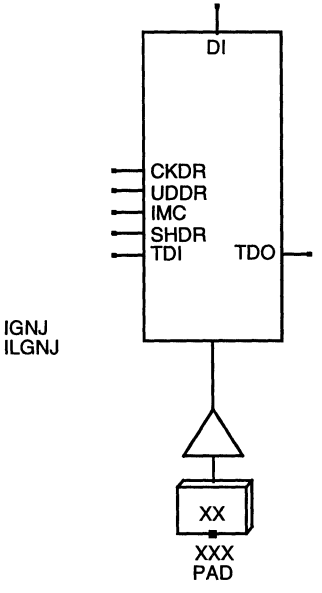
Rev. 1.07

MACRO	OUTPUTS/INPUTS
IGNJ/ILGNJ	DI,TDO / PAD,CKDR,UDDR,IMC,SHDR,TDI

MACRO	INPUT CAP.
IGNJ/ILGNJ	CKDR,TDI: 0.04pF IMC,SHDR,UDDR: 0.10pF PAD: 5.06pF

Function Table

PAD	DI
L	L
H	H



GTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

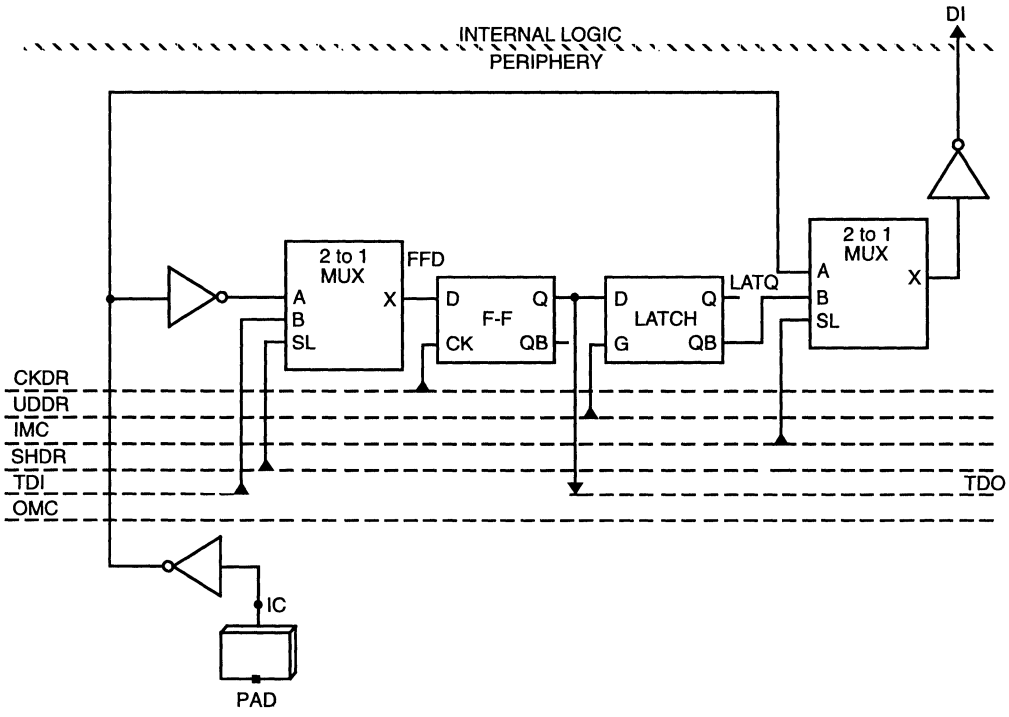
Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		IGNJ				ILGNJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00	1.04	1.04	1.04	0.00
t_{PHL}		0.72	0.72	0.72	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, IMC to DI	0.76	0.79	0.85	0.21	1.07	1.10	1.20	0.31
t_{PHL}		0.51	0.52	0.56	0.14	0.70	0.72	0.78	0.19
t_{PLH}	Propagation Delay, PAD to DI	0.75	0.76	0.80	0.12	1.24	1.25	1.30	0.17
t_{PHL}		0.88	0.89	0.95	0.19	1.22	1.25	1.33	0.26
t_{PLH}	Propagation Delay, TDO to DI	0.76	0.78	0.82	0.13	1.14	1.16	1.21	0.19
t_{PHL}		0.85	0.87	0.93	0.21	1.27	1.30	1.39	0.31
t_{PLH}	Propagation Delay, UDDR to DI	0.88	0.89	0.93	0.13	1.21	1.23	1.28	0.20
t_{PHL}		1.02	1.04	1.11	0.21	1.48	1.51	1.60	0.31
t_r	Output Rise Time, DI	0.17	0.19	0.27	0.25	0.22	0.26	0.36	0.34
t_f	Output Fall Time, DI	0.23	0.25	0.32	0.22	0.34	0.37	0.45	0.27
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

GTL TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		IGNJ	ILGNJ
t_{su}	Set Up Time, PAD to CKDR	0.97	1.52
t_{su}	Set Up Time, SHDR to CKDR	0.31	0.49
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26
t_h	Hold Time, CKDR to PAD	-0.41	-0.78
t_h	Hold Time, CKDR to SHDR	0.16	0.23
t_h	Hold Time, CKDR to TDI	0.31	0.41
t_w	Pulse Width, CKDR(L)	0.45	0.71
t_w	Pulse Width, CKDR(H)	0.80	1.20
t_w	Pulse Width, UDDR(H)	0.71	1.01

FUNCTIONAL DIAGRAM: IGNJ



7

Non-Inverting GTL Bidirectional Input (3.3 V and 5 V System/Core Voltage)

BIGNJ
BILGNJ

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

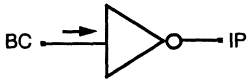
MACRO	OUTPUTS/INPUTS
All	IP / BC

MACRO	INPUT CAP.
All	BC: 0.09pF

MACRO	OUTPUT CAP.
All	IP: 0.23pF

Function Table

PAD	IP
L	H
H	L



BIGNJ / BILGNJ

GTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BIGNJ				BILGNJ			
t_{PLH}	Propagation Delay, BC to IP	0.80	0.80	0.80	0.00	1.10	1.10	1.10	0.00
t_{PHL}		0.93	0.93	0.93	0.00	1.26	1.26	1.26	0.00
t_r	Output Rise Time, IP	0.57	0.57	0.57	0.00	0.75	0.75	0.75	0.00
t_f	Output Fall Time, IP	0.32	0.32	0.32	0.00	0.41	0.41	0.41	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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NOTE:
Path delay from PAD to DI in the bidirectional buffer will be non-inverted when used together with JTAG bidirectional output buffers.

GTL Output and Bidirectional Output (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

ON20GJ
BN40GJ
ONL20GJ
BNL40GJ

MACRO	SECTIONS USED
ON20GJ/ONL20GJ	0/1
BN40GJ/BNL40GJ	0/1

Rev. 1.07

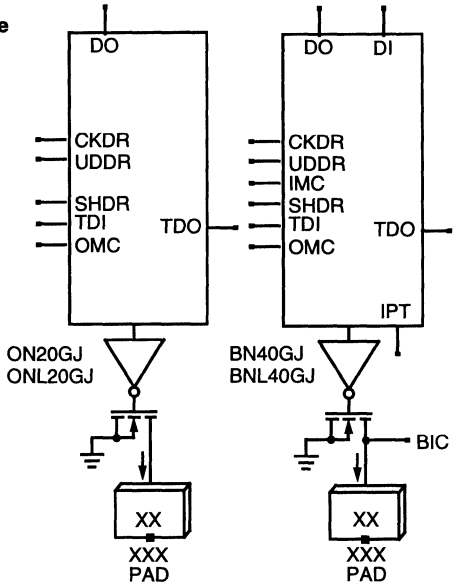
MACRO	OUTPUTS/INPUTS
ON20GJ/ONL20GJ	PAD,TDO / DO,CKDR,UDDR,SHDR,TDI,OMC
BN40GJ/BNL40GJ	BIC,DI,TDO / DO,CKDR,UDDR,IMC,SHDR,TDI, OMC,IPT

MACRO	INPUT CAP.
ON20GJ/ONL20GJ	CKDR,TDI: 0.04pF DO: 0.26pF OMC,SHDR: 0.10pF UDDR: 0.08pF
BN40GJ/BNL40GJ	CKDR,TDI: 0.04pF DO: 0.31pF IMC,OMC,SHDR,UDDR: 0.10pF IPT: 0.22pF

MACRO	OUTPUT CAP.
All	PAD: 4.96pF

Function Table

PAD	DO
L	L
H	Z



GTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON20GJ				ONL20GJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00	1.04	1.04	1.04	0.00
t_{PHL}		0.72	0.72	0.72	0.00	1.01	1.01	1.01	0.00
t_{PLZ}	Propagation Delay, DO to PAD	0.71	3.06	5.41	0.05	0.90	3.15	5.40	0.04
t_{PZL}		0.78	1.08	1.38	0.01	1.12	1.57	2.02	0.01
t_{PLZ}	Propagation Delay, OMC to PAD	0.72	3.07	5.42	0.05	0.96	3.26	5.56	0.05
t_{PZL}		0.98	1.23	1.48	0.00	1.42	1.77	2.12	0.01
t_{PLZ}	Propagation Delay, TDO to PAD	1.04	1.54	2.04	0.01	1.51	1.91	2.31	0.01
t_{PZL}		1.12	1.42	1.72	0.01	1.68	2.13	2.58	0.01
t_{PLZ}	Propagation Delay, UDDR to PAD	1.25	3.60	5.95	0.05	1.68	3.93	6.18	0.04
t_{PZL}		1.29	1.59	1.89	0.01	1.90	2.35	2.80	0.01
t_r	Output Rise Time, PAD	0.23	5.59	10.94	0.11	0.24	5.59	10.94	0.11
t_f	Output Fall Time, PAD	0.45	1.10	1.75	0.01	0.65	1.55	2.45	0.02
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

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GTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BN40GJ				BNL40GJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00	1.04	1.04	1.04	0.00
t_{PHL}		0.72	0.72	0.72	0.00	1.01	1.01	1.01	0.00
t_{PLZ}	Propagation Delay, DO to PAD	0.66	1.86	3.06	0.02	0.97	2.12	3.27	0.02
t_{PZL}		0.83	1.03	1.23	0.00	0.92	1.12	1.32	0.00
t_{PLZ}	Propagation Delay, OMC to PAD	0.70	1.90	3.10	0.02	1.05	2.20	3.35	0.02
t_{PZL}		1.46	1.61	1.76	0.00	1.73	1.88	2.03	0.00
t_{PLZ}	Propagation Delay, TDO to PAD	1.70	2.85	4.00	0.02	2.52	3.67	4.82	0.02
t_{PZL}		1.83	2.03	2.23	0.00	2.35	2.55	2.75	0.00
t_{PLZ}	Propagation Delay, UDDR to PAD	1.81	2.96	4.11	0.02	2.59	3.74	4.89	0.02
t_{PZL}		2.00	2.20	2.40	0.00	2.56	2.76	2.96	0.00
t_r	Output Rise Time, PAD	0.24	2.89	5.54	0.05	0.24	2.89	5.54	0.05
t_f	Output Fall Time, PAD	0.40	0.75	1.10	0.01	0.40	0.75	1.10	0.01
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

GTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BN40GJ				BNL40GJ			
t_{PLH}	Propagation Delay, IMC to DI	0.51	0.52	0.56	0.13	0.68	0.70	0.76	0.19
t_{PHL}		0.76	0.78	0.85	0.22	1.07	1.10	1.20	0.31
t_{PLH}	Propagation Delay, IPT to DI	0.16	0.17	0.20	0.12	0.28	0.29	0.34	0.16
t_{PHL}		0.32	0.34	0.40	0.18	0.48	0.50	0.57	0.23
t_{PLH}	Propagation Delay, TDO to DI	0.79	0.80	0.84	0.13	1.17	1.19	1.25	0.19
t_{PHL}		0.88	0.90	0.97	0.21	1.32	1.35	1.44	0.31
t_{PLH}	Propagation Delay, UDDR to DI	0.89	0.91	0.95	0.13	1.25	1.27	1.33	0.19
t_{PHL}		1.05	1.08	1.14	0.22	1.52	1.55	1.65	0.31
t_r	Output Rise Time, DI	0.20	0.23	0.29	0.22	0.18	0.21	0.32	0.35
t_f	Output Fall Time, DI	0.24	0.25	0.31	0.19	0.24	0.27	0.35	0.26

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

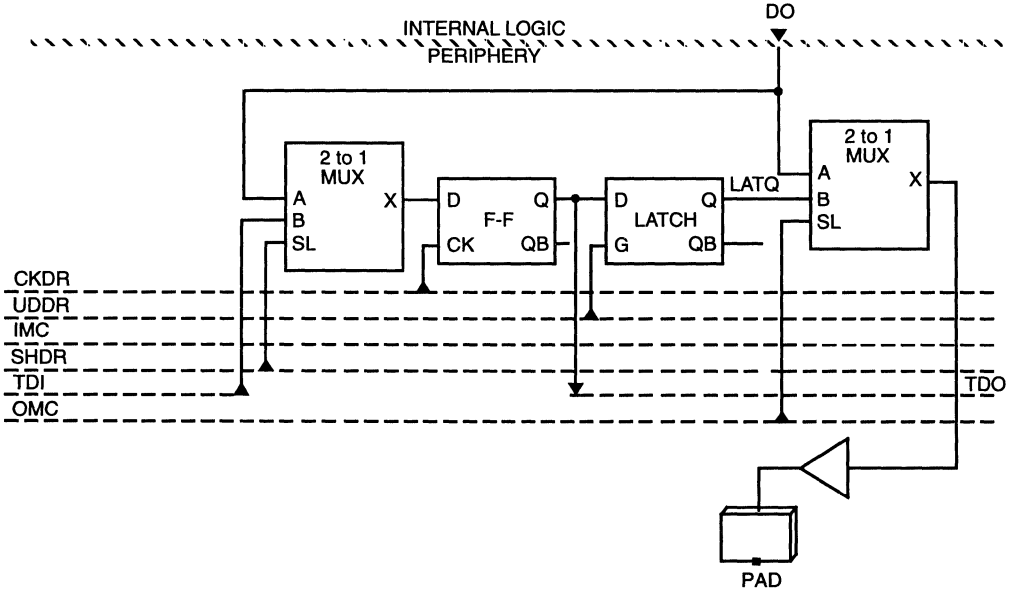
CMOS TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		ON20GJ	ONL20GJ
t_{su}	Set Up Time, DO to CKDR	0.18	0.36
t_{su}	Set Up Time, SHDR to CKDR	0.24	0.43
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26
t_h	Hold Time, CKDR to DO	0.29	0.39
t_h	Hold Time, CKDR to SHDR	0.19	0.26
t_h	Hold Time, CKDR to TDI	0.31	0.39

CMOS TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
t_w	Pulse Width, CKDR(L)	0.41	0.67
t_w	Pulse Width, CKDR(H)	0.65	1.00
t_w	Pulse Width, UDDR(H)	0.46	0.66
		BN40GJ	**BNL40GJ**
t_{su}	Set Up Time, DO to CKDR	0.75	1.03
t_{su}	Set Up Time, IPT to CKDR	0.67	0.53
t_{su}	Set Up Time, SHDR to CKDR	0.31	0.26
t_{su}	Set Up Time, TDI to CKDR	0.13	0.16
t_h	Hold Time, CKDR to DO	0.14	-0.08
t_h	Hold Time, CKDR to IPT	0.00	0.23
t_h	Hold Time, CKDR to SHDR	0.16	0.41
t_h	Hold Time, CKDR to TDI	0.31	0.68
t_w	Pulse Width, CKDR(L)	0.41	1.18
t_w	Pulse Width, CKDR(H)	0.77	0.08
t_w	Pulse Width, UDDR(H)	0.74	0.36

FUNCTIONAL DIAGRAM: ON20GJ



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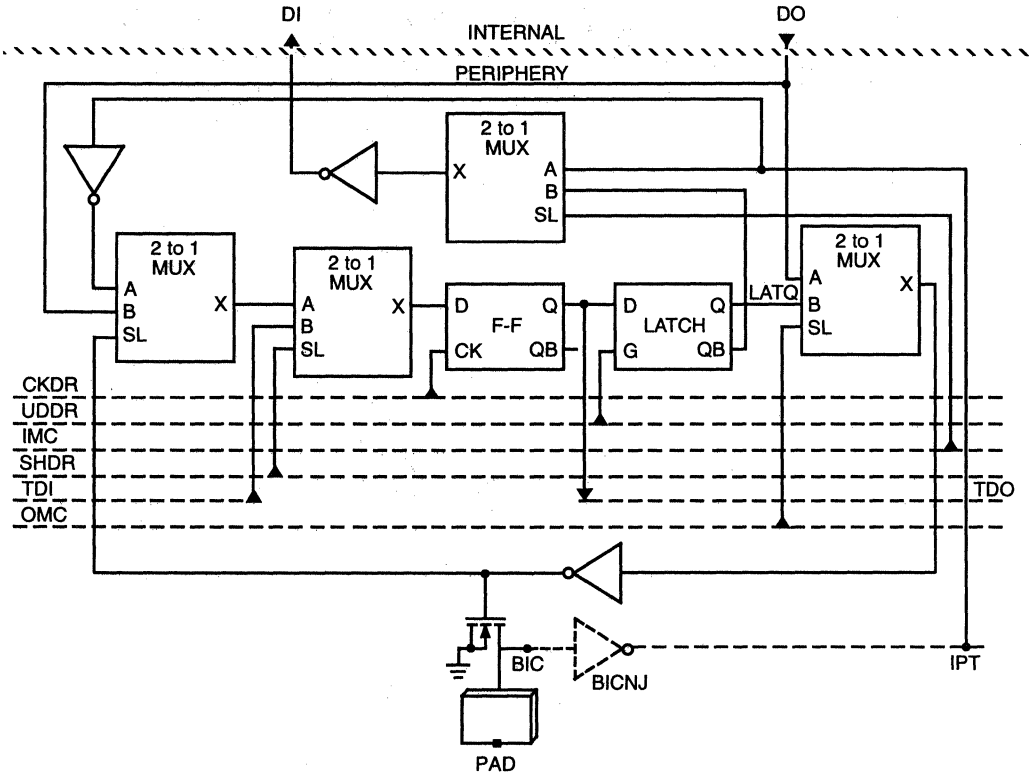
FUNCTIONAL DIAGRAM: BN40GJ



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7.2.7 PECL

PECL Differential Input (3.3 V and 5 V System/Core Voltage)

5/5 V **IPDJ**

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

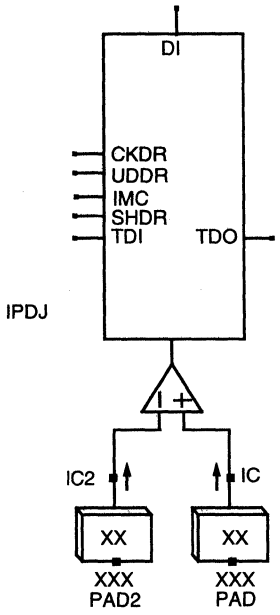
MACRO	OUTPUTS/INPUTS
All	DI / PAD,PAD2,IC,IC2

MACRO	INPUT CAP.
All	PAD,PAD2: 4.98pF

Function Table

PAD	PAD2	DI
L	L	ND
L	H	L
H	L	H
H	H	ND

ND = Not Defined



PECL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
	IPDJ				
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, IMC to DI	0.76	0.78	0.85	0.21
t_{PHL}		0.51	0.52	0.56	0.14
t_{PLH}	Propagation Delay, PAD,PAD2 to DI	0.84	0.85	0.88	0.11
t_{PHL}		0.83	0.85	0.91	0.18
t_{PLH}	Propagation Delay, TDO to DI	0.76	0.78	0.82	0.13
t_{PHL}		0.85	0.87	0.93	0.21
t_{PLH}	Propagation Delay, UDDR to DI	0.88	0.89	0.93	0.13
t_{PHL}		1.02	1.04	1.11	0.21
t_r	Output Rise Time, DI	0.16	0.18	0.26	0.25
t_f	Output Fall Time, DI	0.21	0.23	0.30	0.22
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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7.2.8 PCI

PCI Input -JTAG (3.3 V and 5 V System/Core Voltage)

3.3/3.3 V **ILPCJ**

MACRO	SECTIONS USED
ILPCJ	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
ILPCJ	DI,TDO / PAD,IC,CKDR,UDDR,IMC,SHDR,TDI

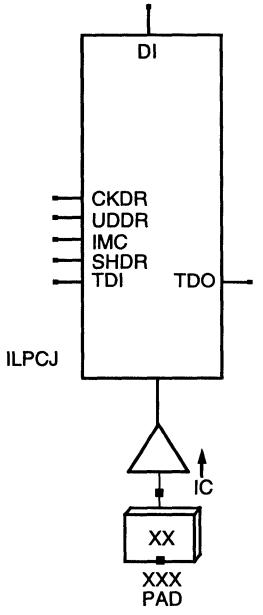
MACRO	INPUT CAP.
ILPCJ	CKDR,TDI: 0.04pF IMC,SHDR,UDDR: 0.10pF PAD: 5.02pF

FUNCTION TABLE

JTAG	
PAD	DI
L	L
H	H

JTAG

For JTAG Truth Table Information, See Table 3, "JTAG Logic Truth Tables - Inputs," on page 181 in this Manual.



PCI SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)
	ILPCJ				
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, IMC to DI	1.07	1.10	1.19	0.31
t_{PHL}		0.70	0.72	0.78	0.19
t_{PLH}	Propagation Delay, PAD to DI	0.68	0.70	0.75	0.17
t_{PHL}		1.01	1.04	1.13	0.29
t_{PLH}	Propagation Delay, TDO to DI	1.14	1.16	1.21	0.19
t_{PHL}		1.27	1.30	1.39	0.31
t_{PLH}	Propagation Delay, UDDR to DI	1.21	1.23	1.28	0.20
t_{PHL}		1.48	1.51	1.60	0.31
t_r	Output Rise Time, DI	0.27	0.31	0.41	0.33
t_f	Output Fall Time, DI	0.42	0.45	0.54	0.29
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

NOTE
For Functional Diagram see page 7-43

PCI Input -JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

IPCHJ
ILPCHJ

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

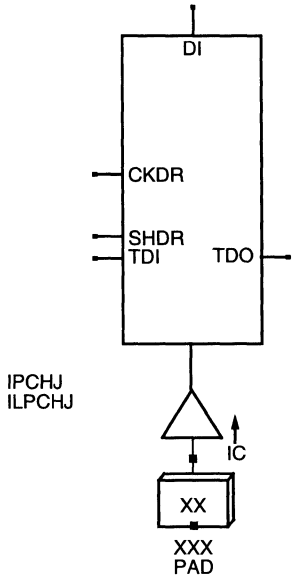
MACRO	OUTPUTS/INPUTS
All	DI,TDO / PAD,IC,CKDR,SHDR,TDI

MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF PAD: 5.40pF SHDR: 0.09pF

FUNCTION TABLE

JTAG	
PAD	DI
L	L
H	H

JTAG
For JTAG Truth Table Information, See Table 3, "JTAG Logic Truth Tables - Inputs," on page 181 in this Manual).



PCI SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		IPCHJ				ILPCHJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.68	0.68	0.68	0.00	1.01	1.01	1.01	0.00
t_{PHL}		0.71	0.71	0.71	0.00	0.98	0.98	0.98	0.00
t_{PLH}	Propagation Delay, PAD to DI	0.37	0.37	0.38	0.04	0.40	0.41	0.43	0.05
t_{PHL}		0.47	0.47	0.50	0.07	0.53	0.54	0.57	0.08
t_r	Output Rise Time, DI	0.05	0.06	0.09	0.10	0.08	0.09	0.13	0.14
t_f	Output Fall Time, DI	0.07	0.08	0.11	0.11	0.08	0.09	0.13	0.14
t_r	Output Rise Time, TDO	0.58	0.58	0.58	0.00	0.79	0.79	0.79	0.00
t_f	Output Fall Time, TDO	0.39	0.39	0.39	0.00	0.49	0.49	0.49	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

PCI TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns)

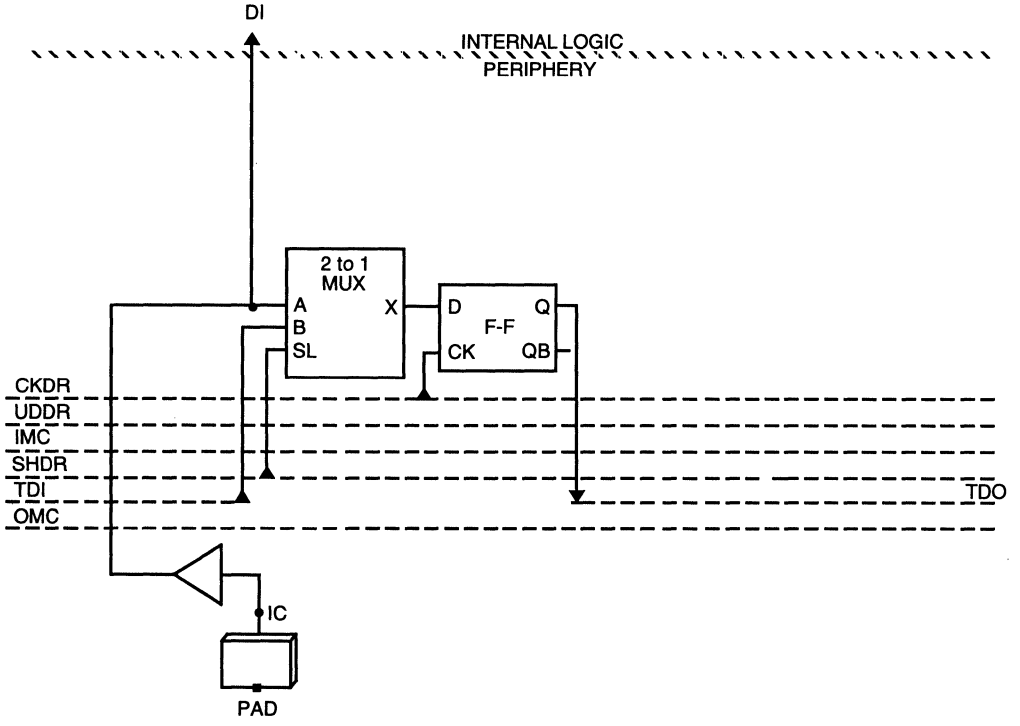
Rev. 1.07

Sym	Parameter	Nom. V_{DD}= 5.0 V, T_J= 25.0°C	
		Minimum Requirement	Minimum Requirement
		IPCHJ	ILPCHJ
t_{su}	Set Up Time, DI to CKDR	0.47	0.67
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.43
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26

PCI TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	Nom. V_{DD}= 5.0 V, T_J= 25.0°C	
		Minimum Requirement	Minimum Requirement
t_h	Hold Time, CKDR to DI	0.10	0.07
t_h	Hold Time, CKDR to SHDR	0.19	0.25
t_h	Hold Time, CKDR to TDI	0.31	0.41
t_w	Pulse Width, CKDR(L)	0.45	0.71
t_w	Pulse Width, CKDR(H)	0.65	0.98

FUNCTIONAL DIAGRAM: IPCHJ



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Inverting PCI Bidirectional Input Buffer-JTAG (3.3 V System/Core Voltage)

3.3/3.3 V **BILPCJ**

MACRO	SECTIONS USED
BILPCJ	0/1

Rev. 1.07

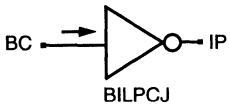
MACRO	OUTPUTS/INPUTS
BILPCJ	IP / BC

MACRO	INPUT CAP.
BILPCJ	BC: 0.06pF

MACRO	OUTPUT CAP.
BILPCJ	IP: 0.16pF

FUNCTION TABLE

JTAG	
BC	IP
L	H
H	L



PCI SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		BILPCJ			
t_{PLH}	Propagation Delay, BC to IP	0.62	0.62	0.62	0.00
t_{PHL}		0.55	0.55	0.55	0.00
t_r	Output Rise Time, IP	1.32	1.32	1.32	0.00
t_f	Output Fall Time, IP	0.52	0.52	0.52	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

NOTE:
Path delay from PAD to DI in the bidirectional buffer will be non-inverted when used together with JTAG bidirectional output buffers.

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PCI Output -JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

ONPCJ
ONLPCJ

MACRO	SECTIONS USED
ONPCJ	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
ONPCJ	PAD,TDO / DO,CKDR,UDDR,SHDR,TDI,OMC

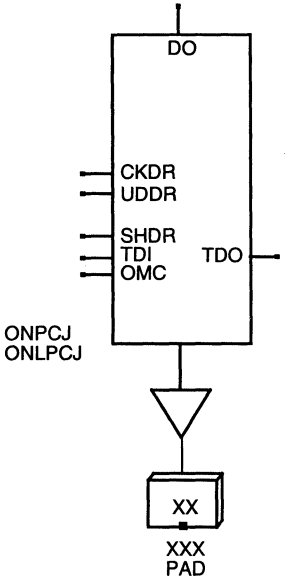
MACRO	INPUT CAP.
ONPCJ	CKDR,TDI: 0.04pF DO: 0.24pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
ONPCJ	PAD: 5.10pF

FUNCTION TABLE

JTAG	
DO	PAD
L	L
H	H

JTAG
For JTAG Truth Table Information, See Table 4, "JTAG Logic Truth Tables - Outputs," on page 181 in this Manual.



PCI SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONPCJ				ONLPCJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	1.04	1.04	1.04	0.00
t_{PHL}		0.72	0.72	0.72	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.81	2.31	3.81	0.03	1.21	2.36	3.51	0.02
t_{PHL}		1.04	1.89	2.74	0.02	1.52	2.52	3.52	0.02
t_{PLH}	Propagation Delay, OMC to PAD	1.00	2.50	4.00	0.03	1.52	2.67	3.82	0.02
t_{PHL}		1.24	2.09	2.94	0.02	1.79	2.79	3.79	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.25	2.75	4.25	0.03	1.96	3.11	4.26	0.02
t_{PHL}		1.40	2.25	3.10	0.02	2.08	3.08	4.08	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	1.38	2.88	4.38	0.03	2.04	3.19	4.34	0.02
t_{PHL}		1.58	2.43	3.28	0.02	2.30	3.30	4.30	0.02
t_r	Output Rise Time, PAD	0.31	3.76	7.21	0.07	0.52	2.87	5.22	0.05
t_f	Output Fall Time, PAD	0.50	1.90	3.30	0.03	0.58	2.28	3.98	0.03
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONPCJ				ONLPCJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	1.04	1.04	1.04	0.00
t_{PHL}		0.72	0.72	0.72	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.74	1.49	2.24	0.01	1.15	2.05	2.95	0.02
t_{PHL}		1.15	2.35	3.55	0.02	1.58	2.78	3.98	0.02
t_{PLH}	Propagation Delay, OMC to PAD	0.93	1.68	2.43	0.01	1.46	2.36	3.26	0.02
t_{PHL}		1.34	2.59	3.84	0.03	1.85	3.05	4.25	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.18	1.93	2.68	0.01	1.90	2.80	3.70	0.02
t_{PHL}		1.51	2.76	4.01	0.03	2.13	3.33	4.53	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	1.31	2.06	2.81	0.01	1.98	2.88	3.78	0.02
t_{PHL}		1.69	2.89	4.09	0.02	2.36	3.56	4.76	0.02
t_r	Output Rise Time, PAD	0.31	3.76	7.21	0.07	0.52	2.87	5.22	0.05
t_f	Output Fall Time, PAD	0.50	1.90	3.30	0.03	0.58	2.28	3.98	0.03
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		ONPCJ	ONLPCJ
t_{su}	Set Up Time, DO to CKDR	0.18	0.37
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.43
t_{su}	Set Up Time, TDI to CKDR	0.14	0.28
t_h	Hold Time, CKDR to DO	0.26	0.35
t_h	Hold Time, CKDR to SHDR	0.19	0.25
t_h	Hold Time, CKDR to TDI	0.32	0.42
t_w	Pulse Width, CKDR(L)	0.40	0.67
t_w	Pulse Width, CKDR(H)	0.78	1.18
t_w	Pulse Width, UDDR(H)	0.47	0.64

NOTE
For Functional Diagram see page 7-47

PCI Non-Inverting 3-State Output -JTAG (3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

ONTPCJ
ONLTPCJ

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD,TDO / DO,EN,CKDR,UDDR,SHDR,TDI,OMC

MACRO	INPUT CAP.
ONTPCJ	CKDR,TDI: 0.04pF DO,EN: 0.24pF OMC,SHDR: 0.10pF UDDR: 0.08pF
ONLTPCJ	CKDR,TDI: 0.04pF DO,EN: 0.23pF OMC,SHDR: 0.10pF UDDR: 0.08pF

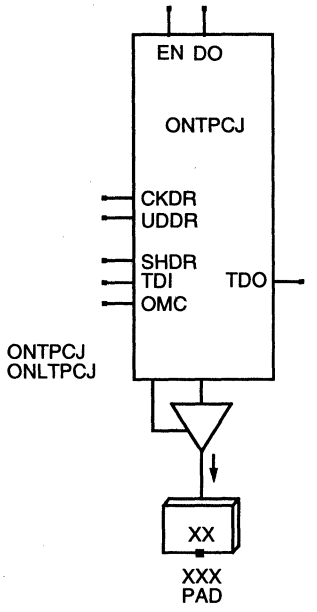
MACRO	OUTPUT CAP.
ONTPCJ	PAD: 5.10pF
ONLTPCJ	PAD: 4.96pF

FUNCTION TABLE

JTAG		
DO	EN	PAD
L	H	L
H	H	H
X	L	Z

JTAG

For JTAG Truth Table Information, See Table 6, "JTAG Logic Truth Tables - Outputs," on page 182 in this Manual.



PCI SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONTPCJ				ONLTPCJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	1.04	1.04	1.04	0.00
t_{PHL}		0.72	0.72	0.72	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.92	2.42	3.92	0.03	1.49	2.64	3.79	0.02
t_{PHL}		1.15	2.00	2.85	0.02	1.58	2.58	3.58	0.02
t_{PLZ}	Propagation Delay, EN to PAD	0.89	0.90	0.90	0.00	1.19	1.20	1.20	0.00
t_{PZL}		0.98	1.83	2.68	0.02	1.27	2.27	3.27	0.02
t_{PZH}	Propagation Delay, EN to PAD	0.77	2.32	3.87	0.03	1.23	2.38	3.53	0.02
t_{PHZ}		0.76	0.76	0.77	0.00	1.20	1.20	1.21	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.10	2.60	4.10	0.03	1.77	2.92	4.07	0.02
t_{PHL}		1.33	2.18	3.03	0.02	1.85	2.85	3.85	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.34	2.84	4.34	0.03	2.20	3.35	4.50	0.02
t_{PHL}		1.50	2.35	3.20	0.02	2.14	3.14	4.14	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	1.48	2.98	4.48	0.03	2.29	3.44	4.59	0.02
t_{PHL}		1.67	2.52	3.37	0.02	2.35	3.35	4.35	0.02
t_r	Output Rise Time, PAD	0.31	3.76	7.21	0.07	0.52	2.87	5.22	0.05
t_f	Output Fall Time, PAD	0.50	1.90	3.30	0.03	0.59	2.29	3.99	0.03
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

TTL SWITCHING CHARACTERISTICS

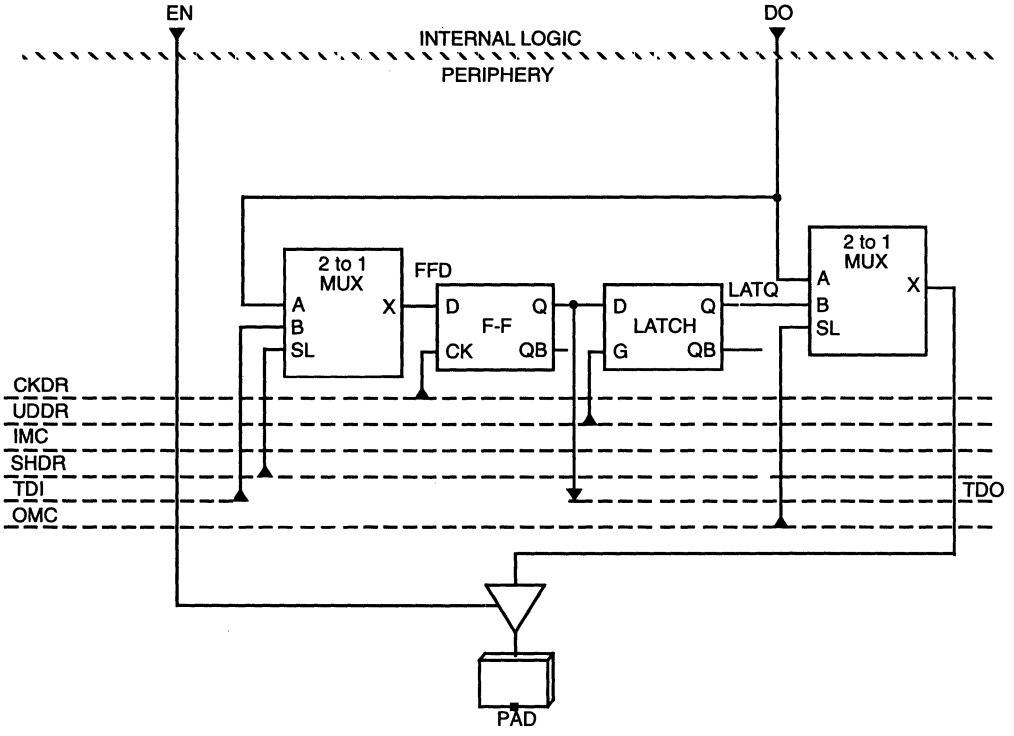
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONTPCJ				ONLTPCJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	1.04	1.04	1.04	0.00
t_{PHL}		0.72	0.72	0.72	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.84	1.59	2.35	0.01	1.43	2.33	3.23	0.02
t_{PHL}		1.26	2.46	3.66	0.02	1.64	2.84	4.04	0.02
t_{PLZ}	Propagation Delay, EN to PAD	1.00	1.01	1.01	0.00	1.25	1.26	1.26	0.00
t_{PZL}		1.10	2.35	3.60	0.03	1.33	2.53	3.73	0.02
t_{PZH}	Propagation Delay, EN to PAD	0.69	1.49	2.29	0.02	1.17	2.07	2.97	0.02
t_{PHZ}		0.69	0.69	0.70	0.00	1.14	1.14	1.15	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.02	1.77	2.52	0.01	1.71	2.61	3.51	0.02
t_{PHL}		1.42	2.67	3.92	0.03	1.91	3.11	4.31	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.27	2.02	2.77	0.01	2.14	3.04	3.94	0.02
t_{PHL}		1.61	2.81	4.01	0.02	2.20	3.40	4.60	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	1.41	2.16	2.91	0.01	2.23	3.13	4.03	0.02
t_{PHL}		1.78	2.98	4.18	0.02	2.41	3.61	4.81	0.02
t_r	Output Rise Time, PAD	0.31	3.76	7.21	0.07	0.52	2.87	5.22	0.05
t_f	Output Fall Time, PAD	0.50	1.90	3.30	0.03	0.59	2.29	3.99	0.03
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

PCI/TTL TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		ONTPCJ	ONLTPCJ
t_{su}	Set Up Time, DO to CKDR	0.19	0.40
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.43
t_{su}	Set Up Time, TDI to CKDR	0.14	0.28
t_h	Hold Time, CKDR to DO	0.25	0.35
t_h	Hold Time, CKDR to SHDR	0.19	0.25
t_h	Hold Time, CKDR to TDI	0.32	0.42
t_w	Pulse Width, CKDR(L)	0.40	0.67
t_w	Pulse Width, CKDR(H)	0.78	1.18
t_w	Pulse Width, UDDR(L)	0.05	0.08
t_w	Pulse Width, UDDR(H)	0.46	0.64

FUNCTIONAL DIAGRAM: ONTPCJ



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PCI Non-Inverting 3-State Bidirectional Output -JTAG (3 V and 5 V System/Core Voltage)

5/5 V **BNTPCJ**
3.3/3.3 V **BNLTPCJ**

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	BIC,DI,TDO / DO,EN,CKDR,UDDR,IMC,SHDR, TDI,OMC,IPT

MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF DO,IPT: 0.24pF EN: 0.21pF IMC,OMC,SHDR,UDDR: 0.10pF

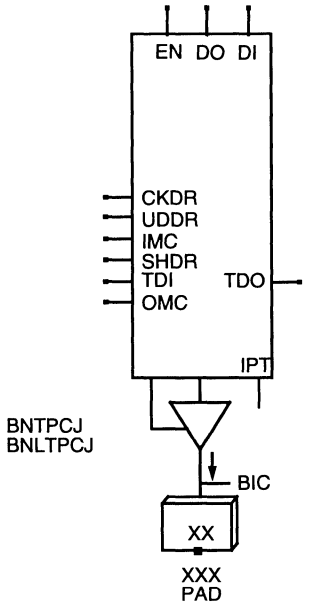
MACRO	OUTPUT CAP.
All	PAD: 5.10pF

FUNCTION TABLE

JTAG		
DO	EN	PAD
L	H	L
H	H	H
X	L	Z

JTAG

For JTAG Truth Table Information, See Table 6, "JTAG Logic Truth Tables - Outputs," on page 182 in this Manual.



PCI SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BNTPCJ				BNLTPCJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00	1.04	1.04	1.04	0.00
t_{PHL}		0.72	0.72	0.72	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.92	2.42	3.92	0.03	1.56	2.71	3.86	0.02
t_{PHL}		1.15	2.00	2.85	0.02	1.59	2.59	3.59	0.02
t_{PLZ}	Propagation Delay, EN to PAD	0.90	0.91	0.91	0.00	1.30	1.30	1.31	0.00
t_{PZL}		0.99	1.84	2.69	0.02	1.38	2.38	3.38	0.02
t_{PZH}	Propagation Delay, EN to PAD	0.75	2.30	3.85	0.03	1.36	2.51	3.66	0.02
t_{PHZ}		0.74	0.75	0.75	0.00	1.34	1.34	1.35	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.38	2.88	4.38	0.03	2.18	3.33	4.48	0.02
t_{PHL}		1.70	2.50	3.30	0.02	2.28	3.08	3.88	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.91	3.41	4.91	0.03	3.03	4.13	5.23	0.02
t_{PHL}		2.13	2.93	3.73	0.02	3.00	3.95	4.90	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	2.01	3.51	5.01	0.03	3.10	4.20	5.30	0.02
t_{PHL}		2.31	3.11	3.91	0.02	3.20	4.15	5.10	0.02
t_r	Output Rise Time, PAD	0.31	3.76	7.21	0.07	0.52	2.87	5.22	0.05
t_f	Output Fall Time, PAD	0.50	1.90	3.30	0.03	0.59	2.29	3.99	0.03
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

PCI SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BNTPCJ				BNLTPCJ			
t_{PLH}	Propagation Delay, IMC to DI	0.75	0.77	0.84	0.22	1.07	1.10	1.19	0.31
t_{PHL}		0.51	0.52	0.56	0.13	0.68	0.70	0.76	0.19
t_{PLH}	Propagation Delay, IPT to DI	0.16	0.17	0.20	0.12	0.28	0.29	0.34	0.16
t_{PHL}		0.32	0.34	0.40	0.18	0.48	0.50	0.57	0.23
t_{PLH}	Propagation Delay, TDO to DI	0.79	0.80	0.84	0.13	1.17	1.19	1.25	0.19
t_{PHL}		0.88	0.90	0.97	0.21	1.32	1.35	1.44	0.31
t_{PLH}	Propagation Delay, UDDR to DI	0.89	0.91	0.95	0.13	1.25	1.27	1.33	0.19
t_{PHL}		1.05	1.08	1.14	0.22	1.52	1.55	1.65	0.31
t_r	Output Rise Time, DI	0.20	0.23	0.29	0.22	0.18	0.21	0.32	0.35
t_f	Output Fall Time, DI	0.24	0.25	0.31	0.19	0.24	0.27	0.35	0.26

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BNTPCJ				BNLTPCJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00	1.04	1.04	1.04	0.00
t_{PHL}		0.72	0.72	0.72	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.85	1.60	2.35	0.01	1.50	2.40	3.30	0.02
t_{PHL}		1.26	2.51	3.76	0.03	1.65	2.85	4.05	0.02
t_{PLZ}	Propagation Delay, EN to PAD	1.02	1.02	1.03	0.00	1.36	1.36	1.37	0.00
t_{PZL}		1.10	2.35	3.60	0.03	1.44	2.64	3.84	0.02
t_{PZH}	Propagation Delay, EN to PAD	0.68	1.48	2.28	0.02	1.30	2.20	3.10	0.02
t_{PHZ}		0.67	0.68	0.68	0.00	1.28	1.28	1.29	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.31	2.07	2.81	0.01	2.13	3.03	3.93	0.02
t_{PHL}		1.82	2.82	3.82	0.02	2.34	3.34	4.34	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.84	2.59	3.34	0.01	2.97	3.87	4.77	0.02
t_{PHL}		2.24	3.44	4.64	0.02	3.06	4.21	5.36	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	1.94	2.69	3.44	0.01	3.04	3.94	4.84	0.02
t_{PHL}		2.42	3.62	4.82	0.02	3.26	4.41	5.56	0.02
t_r	Output Rise Time, PAD	0.31	3.76	7.21	0.07	0.52	2.87	5.22	0.05
t_f	Output Fall Time, PAD	0.50	1.90	3.30	0.03	0.59	2.29	3.99	0.03
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

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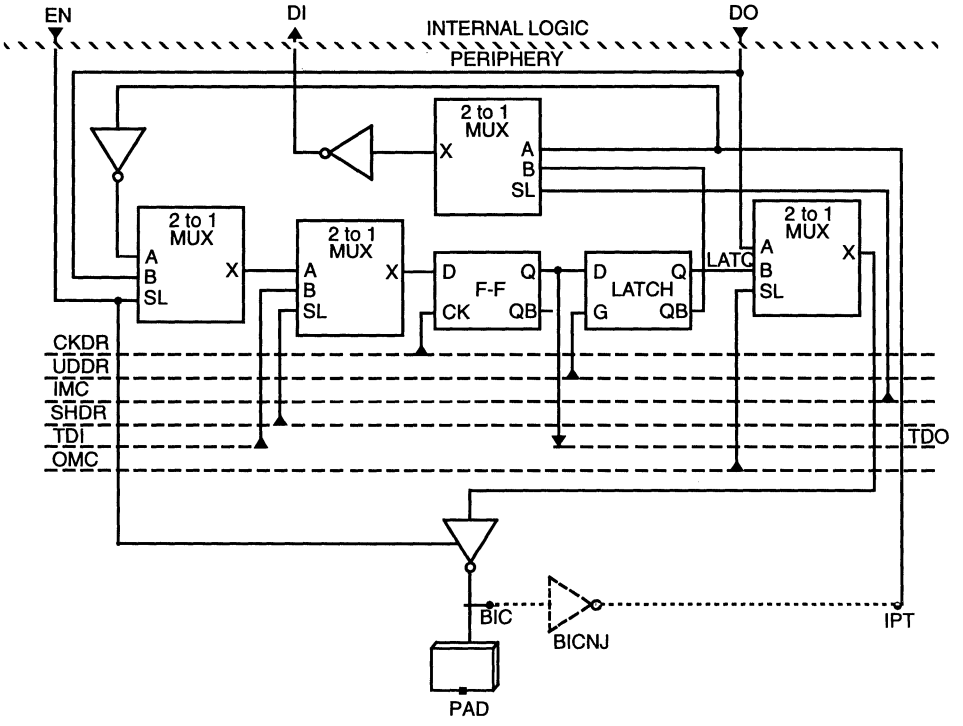
PCI/TTL TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		BNTPCJ	BNLTPCJ
t_{su}	Set Up Time, DO to CKDR	0.33	0.63
t_{su}	Set Up Time, EN,IPT to CKDR	0.65	1.03
t_{su}	Set Up Time, SHDR to CKDR	0.31	0.53
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26
t_h	Hold Time, CKDR to DO,SHDR	0.15	0.20
t_h	Hold Time, CKDR to EN	0.08	0.04
t_h	Hold Time, CKDR to IPT	0.00	-0.08
t_h	Hold Time, CKDR to TDI	0.31	0.23
t_w	Pulse Width, CKDR(L)	0.42	0.41
t_w	Pulse Width, CKDR(H)	0.78	0.72
t_w	Pulse Width, UDDR(H)	0.75	0.08

FUNCTIONAL DIAGRAM: BNTPCJ



7

Section 7.3 JTAG Boundary Scan Functions

Section 7.3.1Test Macros -JTAG

Test Clock Buffer - JTAG
1X & 2X Drive, CMOS Levels
(3.3 V and 5 V System/Core Voltage)

5/5 V
5/3.3 V
3.3/3.3 V

TCK/TCKH
TCKX/TCKHX
TCKL/TCKHL

MACRO	SECTIONS USED
TCK/TCKX/TCKL	1/0
TCKH/TCKHX/TCKHL	1/1

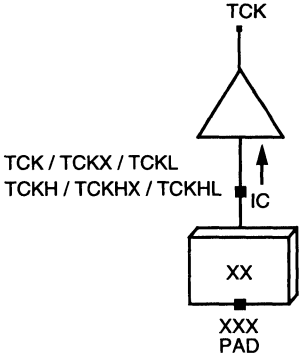
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	TCK / PAD,IC

MACRO	INPUT CAP.
TCK/TCKX/TCKL	PAD: 5.06pF
TCKH/TCKHX/TCKHL	PAD: 5.16pF

FUNCTION TABLE

JTAG	
PAD	TCK
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		TCK			
t_{PLH}	Propagation Delay, PAD to TCK	0.33	0.34	0.38	0.11
t_{PHL}		0.37	0.39	0.43	0.15
t_r	Output Rise Time, TCK	0.13	0.15	0.23	0.25
t_f	Output Fall Time, TCK	0.12	0.14	0.20	0.20
		TCKH			
t_{PLH}	Propagation Delay, PAD to TCK	0.36	0.36	0.37	0.04
t_{PHL}		0.44	0.45	0.47	0.07
t_r	Output Rise Time, TCK	0.16	0.17	0.20	0.10
t_f	Output Fall Time, TCK	0.21	0.22	0.25	0.11

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		TCKX				TCKL			
t_{PLH}	Propagation Delay, PAD to TCK	0.21	0.23	0.27	0.15	0.43	0.44	0.49	0.15
t_{PHL}		0.62	0.64	0.70	0.19	0.50	0.52	0.58	0.19
t_r	Output Rise Time, TCK	0.15	0.19	0.29	0.35	0.17	0.21	0.31	0.34
t_f	Output Fall Time, TCK	0.13	0.16	0.23	0.25	0.17	0.20	0.27	0.24
		TCKHX				TCKHL			
t_{PLH}	Propagation Delay, PAD to TCK	0.25	0.26	0.27	0.05	0.48	0.48	0.50	0.05
t_{PHL}		0.64	0.65	0.68	0.08	0.53	0.54	0.57	0.08
t_r	Output Rise Time, TCK	0.17	0.18	0.22	0.14	0.20	0.21	0.25	0.14
t_f	Output Fall Time, TCK	0.22	0.23	0.27	0.13	0.22	0.23	0.27	0.13

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

Test Clock Buffer - JTAG
1X and 2X Drive, TTL Levels
(3.3 V and 5 V System/Core Voltage)

5/5 V
5/3.3 V
3.3/5 V

TCKT/TCKHT
TCKTX/TCKHTX
TCKLTX/TCKHLTX

MACRO	SECTIONS USED
TCKT/TCKTX/TCKLTX	1/0
TCKHT/TCKHTX/ TCKHLTX	1/1

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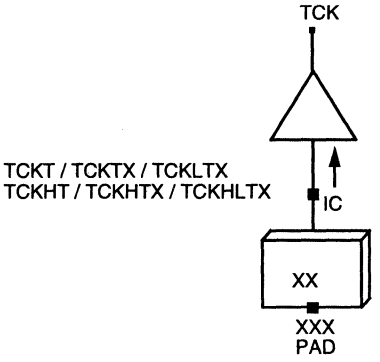
MACRO	OUTPUTS/INPUTS
All	TCK / PAD,IC

MACRO	INPUT CAP.
TCKT/TCKTX/TCKLTX	PAD: 5.05pF
TCKHT/TCKHTX/ TCKHLTX	PAD: 5.40pF

FUNCTION TABLE

JTAG	
PAD	TCK
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		TCKT				TCKLTX			
t_{PLH}	Propagation Delay,	0.29	0.31	0.34	0.11	0.29	0.31	0.34	0.11
t_{PHL}	PAD to TCK	0.64	0.65	0.71	0.18	0.64	0.65	0.71	0.18
t_r	Output Rise Time, TCK	0.12	0.15	0.22	0.24	0.12	0.15	0.22	0.24
t_f	Output Fall Time, TCK	0.28	0.30	0.36	0.20	0.28	0.30	0.36	0.20

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				5/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		TCKTX				TCKHTX			
t_{PLH}	Propagation Delay,	0.45	0.47	0.51	0.15	0.49	0.50	0.51	0.05
t_{PHL}	PAD to TCK	0.38	0.40	0.46	0.19	0.40	0.41	0.44	0.08
t_r	Output Rise Time, TCK	0.15	0.19	0.29	0.35	0.17	0.18	0.22	0.14
t_f	Output Fall Time, TCK	0.13	0.16	0.23	0.25	0.22	0.23	0.27	0.13

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		TCKHT				TCKHLTX			
t_{PLH}	Propagation Delay,	0.33	0.33	0.34	0.04	0.33	0.33	0.34	0.04
t_{PHL}	PAD to TCK	0.47	0.47	0.50	0.07	0.47	0.47	0.50	0.07
t_r	Output Rise Time, TCK	0.11	0.12	0.15	0.10	0.11	0.12	0.15	0.10
t_f	Output Fall Time, TCK	0.18	0.19	0.22	0.11	0.18	0.19	0.22	0.11

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

Test Data Input Buffer - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V **TDI**
5/3.3 V **TDIX**
3.3/3.3 V **TDIL**

MACRO	SECTIONS USED
ALL	1/0

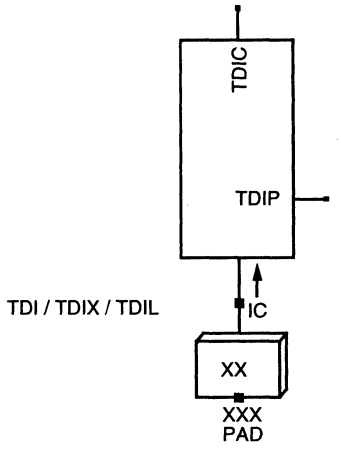
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ALL	TDIC,TDIP / PAD,IC

MACRO	INPUT CAP.
ALL	PAD: 5.06pF

FUNCTION TABLE

JTAG		
PAD	TDIC	TDIP
L	L	L
H	H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		TDI			
t_{PLH}	Propagation Delay, PAD to TDIC	0.38	0.39	0.42	0.12
t_{PHL}		0.42	0.43	0.48	0.16
t_{PLH}	Propagation Delay, PAD to TDIP	0.44	0.48	0.59	0.39
t_{PHL}		0.40	0.43	0.54	0.34
t_r	Output Rise Time, TDIC	0.14	0.17	0.24	0.25
t_f	Output Fall Time, TDIC	0.13	0.15	0.21	0.21
t_r	Output Rise Time, TDIP	0.17	0.27	0.58	1.04
t_f	Output Fall Time, TDIP	0.13	0.18	0.32	0.47

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		TDIX				TDIL			
t_{PLH}	Propagation Delay, PAD to TDIC	0.25	0.26	0.31	0.15	0.48	0.49	0.54	0.16
t_{PHL}		0.68	0.70	0.76	0.20	0.56	0.58	0.64	0.20
t_{PLH}	Propagation Delay, PAD to TDIP	0.29	0.35	0.51	0.56	0.54	0.59	0.76	0.56
t_{PHL}		0.67	0.71	0.84	0.41	0.55	0.60	0.72	0.41
t_r	Output Rise Time, TDIC	0.15	0.19	0.29	0.36	0.20	0.23	0.33	0.34
t_f	Output Fall Time, TDIC	0.16	0.18	0.26	0.25	0.16	0.19	0.26	0.25
t_r	Output Rise Time, TDIP	0.16	0.31	0.76	1.48	0.20	0.34	0.78	1.47
t_f	Output Fall Time, TDIP	0.17	0.23	0.40	0.57	0.17	0.23	0.40	0.57

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

Test Data Input Buffer - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
5/3.3 V
3.3/5 V

TDIT
TDITX
TDILTX

MACRO	SECTIONS USED
ALL	1/0

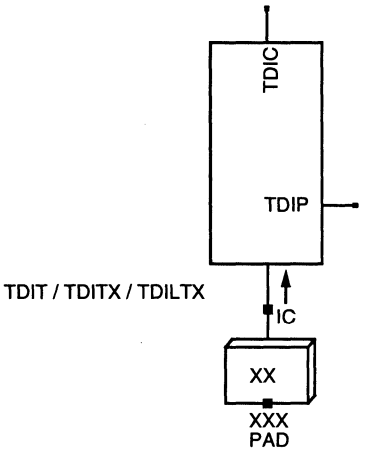
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ALL	TDIC,TDIP / PAD,IC

MACRO	INPUT CAP.
ALL	PAD: 5.05pF

FUNCTION TABLE

JTAG		
PAD	TDIC	TDIP
L	L	L
H	H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		TDIT				TDILTX			
t_{PLH}	Propagation Delay,	0.33	0.34	0.37	0.11	0.33	0.34	0.37	0.11
t_{PHL}	PAD to TDIC	0.76	0.78	0.84	0.20	0.76	0.78	0.84	0.20
t_{PLH}	Propagation Delay,	0.36	0.40	0.51	0.38	0.36	0.40	0.51	0.38
t_{PHL}	PAD to TDIP	0.71	0.75	0.88	0.42	0.71	0.75	0.88	0.42
t_r	Output Rise Time, TDIC	0.14	0.16	0.23	0.24	0.14	0.16	0.23	0.24
t_f	Output Fall Time, TDIC	0.34	0.36	0.42	0.20	0.34	0.36	0.42	0.20
t_r	Output Rise Time, TDIP	0.14	0.24	0.56	1.05	0.14	0.24	0.56	1.05
t_f	Output Fall Time, TDIP	0.33	0.38	0.52	0.46	0.33	0.38	0.52	0.46

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3V			
		FO=0	FO=2	FO=8	K (ns/pF)
		TDITX			
t_{PLH}	Propagation Delay,	0.49	0.50	0.55	0.15
t_{PHL}	PAD to TDIC	0.44	0.46	0.52	0.20
t_{PLH}	Propagation Delay,	0.53	0.59	0.75	0.56
t_{PHL}	PAD to TDIP	0.43	0.47	0.60	0.41
t_r	Output Rise Time, TDIC	0.15	0.19	0.29	0.36
t_f	Output Fall Time, TDIC	0.16	0.18	0.26	0.25
t_r	Output Rise Time, TDIP	0.16	0.31	0.76	1.48
t_f	Output Fall Time, TDIP	0.17	0.23	0.40	0.57

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

Test Mode Select Buffer - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V **TMS**
5/3.3 V **TMSX**
3.3/3.3 V **TMSL**

MACRO	SECTIONS USED
ALL	1/0

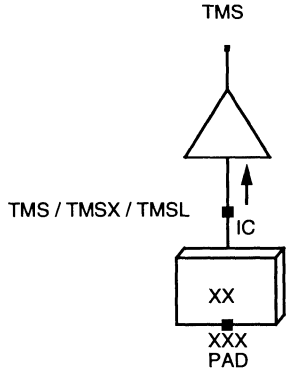
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ALL	TMS / PAD,IC

MACRO	INPUT CAP.
ALL	PAD: 5.06pF

FUNCTION TABLE

JTAG	
PAD	TMS
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		TMS			
t_{PLH}	Propagation Delay,	0.33	0.34	0.38	0.11
t_{PHL}	PAD to TMS	0.37	0.39	0.43	0.15
t_r	Output Rise Time, TMS	0.13	0.15	0.23	0.25
t_f	Output Fall Time, TMS	0.12	0.14	0.20	0.20

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		TMSX				TMSL			
t_{PLH}	Propagation Delay,	0.21	0.23	0.27	0.15	0.43	0.44	0.49	0.15
t_{PHL}	PAD to TMS	0.62	0.64	0.70	0.19	0.50	0.52	0.58	0.19
t_r	Output Rise Time, TMS	0.15	0.19	0.29	0.35	0.17	0.21	0.31	0.34
t_f	Output Fall Time, TMS	0.13	0.16	0.23	0.25	0.17	0.20	0.27	0.24

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

Test Mode Select Buffer - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V TMST
5/3.3 V TMSTX
3.3/5 V TMSLTX

MACRO	SECTIONS USED
ALL	1/0

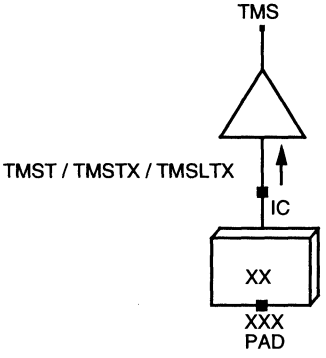
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ALL	TMS / PAD,IC

MACRO	INPUT CAP.
ALL	PAD: 5.05pF

FUNCTION TABLE

JTAG	
PAD	TMS
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		TMST				TMSLTX			
t_{PLH}	Propagation Delay,	0.29	0.31	0.34	0.11	0.29	0.31	0.34	0.11
t_{PHL}	PAD to TMS	0.64	0.65	0.71	0.18	0.64	0.65	0.71	0.18
t_r	Output Rise Time,TMS	0.12	0.15	0.22	0.24	0.12	0.15	0.22	0.24
t_f	Output Fall Time, TMS	0.28	0.30	0.36	0.20	0.28	0.30	0.36	0.20

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		TMSTX			
t_{PLH}	Propagation Delay,	0.45	0.47	0.51	0.15
t_{PHL}	PAD to TMS	0.38	0.40	0.46	0.19
t_r	Output Rise Time, TMS	0.15	0.19	0.29	0.35
t_f	Output Fall Time, TMS	0.13	0.16	0.23	0.25

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

Test Reset (Bar) Buffer - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V TRSTB
5/3.3 V TRSTBX
3.3/3.3 V TRSTBL

MACRO	SECTIONS USED
ALL	1/0

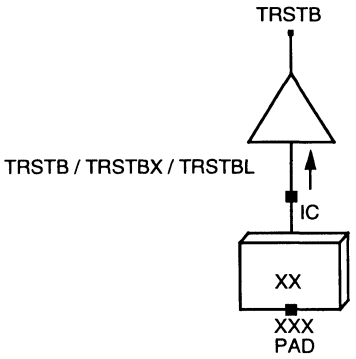
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ALL	TRSTB / PAD,IC

MACRO	INPUT CAP.
ALL	PAD: 5.06pF

FUNCTION TABLE

JTAG	
PAD	TRSTB
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		TRSTB				TRSTBL			
t_{PLH}	Propagation Delay,	0.33	0.34	0.38	0.11	0.43	0.44	0.49	0.15
t_{PHL}	PAD to TRSTB	0.37	0.39	0.43	0.15	0.50	0.52	0.58	0.19
t_r	Output Rise Time, TRSTB	0.13	0.15	0.23	0.25	0.17	0.21	0.31	0.34
t_f	Output Fall Time, TRSTB	0.12	0.14	0.20	0.20	0.17	0.20	0.27	0.24

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		TRSTBX			
t_{PLH}	Propagation Delay,	0.21	0.23	0.27	0.15
t_{PHL}	PAD to TRSTB	0.62	0.64	0.70	0.19
t_r	Output Rise Time, TRSTB	0.15	0.19	0.29	0.35
t_f	Output Fall Time, TRSTB	0.13	0.16	0.23	0.25

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

Test Reset (Bar) Buffer - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V **TRSTBT**
5/3.3 V **TRSTBTX**
3.3/5 V **TRSTBLTX**

MACRO	SECTIONS USED
ALL	1/0

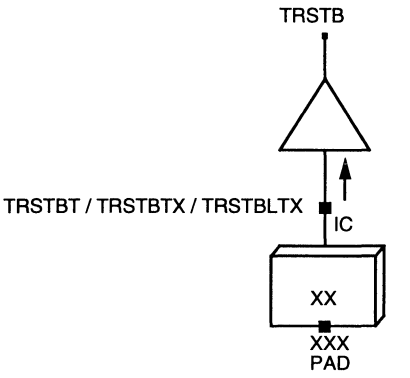
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ALL	TRSTB / PAD,IC

MACRO	INPUT CAP.
ALL	PAD: 5.05pF

FUNCTION TABLE

JTAG	
PAD	TRSTB
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		TRSTBT				TRSTBLTX			
t_{PLH}	Propagation Delay, PAD to TRSTB	0.29	0.31	0.34	0.11	0.29	0.31	0.34	0.11
t_{PHL}		0.64	0.65	0.71	0.18	0.64	0.65	0.71	0.18
t_r	Output Rise Time, TRSTB	0.12	0.15	0.22	0.24	0.12	0.15	0.22	0.24
t_f	Output Fall Time, TRSTB	0.28	0.30	0.36	0.20	0.28	0.30	0.36	0.20

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		TRSTBTX			
t_{PLH}	Propagation Delay, PAD to TRSTB	0.45	0.47	0.51	0.15
t_{PHL}		0.38	0.40	0.46	0.19
t_r	Output Rise Time, TRSTB	0.15	0.19	0.29	0.35
t_f	Output Fall Time, TRSTB	0.13	0.16	0.23	0.25

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

Test Data Output Buffer - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
5/3.3 V
3.3/5 V
3.3/3.3 V

TDOUT
TDOUTX
TDOUTLX
TDOUTL

MACRO	SECTIONS USED
ALL	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
ALL	TDOC,PAD / DO,EN,TDI

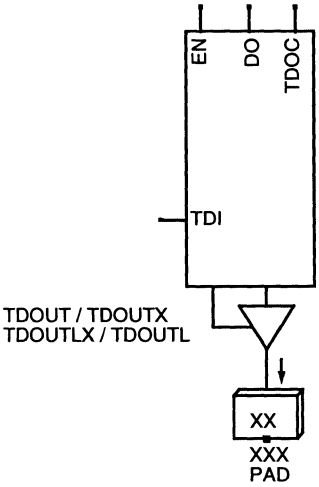
MACRO	INPUT CAP.
ALL	DO: 0.24pF EN: 0.19pF TDI: 0.11pF

MACRO	OUTPUT CAP.
ALL	PAD: 5.10pF

FUNCTION TABLE

EN	DO	PAD
L	X	Z
H	L	L
H	H	H

TDI	TDOC
L	L
H	H
JTAG	
For JTAG Truth Table Information, See Table 7-6:JTAG Logic Truth Tables - Outputs on page 7-184 in this Manual).	



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		TDOUT				TDOUTLX			
t_{PLH}	Propagation Delay, DO to PAD	0.82	2.25	3.67	0.03	1.14	2.84	4.55	0.03
t_{PHL}		0.92	2.46	4.00	0.03	0.95	2.41	3.88	0.03
t_{PLZ}	Propagation Delay, EN to PAD	0.78	0.78	0.79	0.00	0.62	0.62	0.63	0.00
t_{PZL}		0.72	2.34	3.95	0.03	0.97	3.45	5.93	0.05
t_{PZH}	Propagation Delay, EN to PAD	0.74	2.18	3.61	0.03	1.06	2.78	4.50	0.03
t_{PHZ}		1.06	1.07	1.07	0.00	1.24	1.24	1.25	0.00
t_{PLH}	Propagation Delay, TDI to TDOC	0.32	5.65	10.97	0.11	0.32	5.65	10.97	0.11
t_{PHL}		0.33	7.93	15.54	0.15	0.33	7.93	15.54	0.15
t_r	Output Rise Time, PAD	0.31	3.23	6.15	0.06	0.57	3.59	6.61	0.06
t_f	Output Fall Time, PAD	0.41	2.82	5.22	0.05	0.47	2.93	5.39	0.05
t_r	Output Rise Time, TDOC	0.13	12.57	25.02	0.25	0.13	12.57	25.02	0.25
t_f	Output Fall Time, TDOC	0.13	10.11	20.09	0.20	0.13	10.11	20.09	0.20

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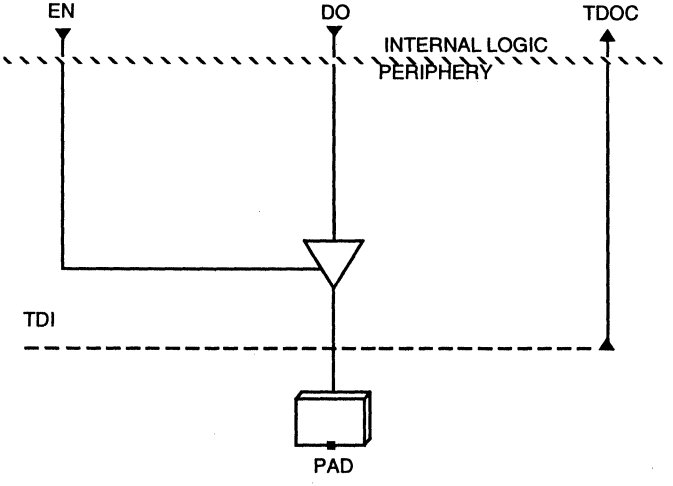
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		TDOUTX				TDOUTL			
t_{PLH}	Propagation Delay,	1.54	2.81	4.09	0.03	1.21	3.16	5.10	0.04
t_{PHL}	DO to PAD	1.90	3.83	5.76	0.04	1.24	3.11	4.99	0.04
t_{PLZ}	Propagation Delay,	1.18	1.19	1.19	0.00	0.88	0.89	0.89	0.00
t_{PZL}	EN to PAD	2.23	4.18	6.13	0.04	0.99	2.93	4.86	0.04
t_{PZH}	Propagation Delay,	1.42	2.71	3.99	0.03	1.09	3.07	5.04	0.04
t_{PHZ}	EN to PAD	1.59	1.60	1.60	0.00	1.25	1.25	1.26	0.00
t_{PLH}	Propagation Delay,	0.41	8.09	15.76	0.15	0.41	8.09	15.76	0.15
t_{PHL}	TDI to TDOC	0.45	9.76	19.06	0.19	0.45	9.76	19.06	0.19
t_r	Output Rise Time, PAD	0.30	2.97	5.64	0.05	0.40	4.40	8.40	0.08
t_f	Output Fall Time, PAD	0.52	3.46	6.39	0.06	0.52	3.43	6.34	0.06
t_r	Output Rise Time, TDOC	0.17	17.56	34.95	0.35	0.17	17.56	34.95	0.35
t_f	Output Fall Time, TDOC	0.15	12.45	24.75	0.25	0.15	12.45	24.75	0.25

FUNCTIONAL DIAGRAM: TDOUT



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Section 7.3.2 Bidirectional Macros -JTAG

Non-Inverting CMOS Bidirectional Input Buffer - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V **BICNJ**
5/3.3 V **BICXNJ**
3.3/3.3 V **BILCNJ**

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

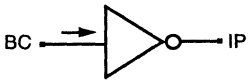
MACRO	OUTPUTS/INPUTS
All	IP / BC

MACRO	INPUT CAP.
All	BC: 0.10pF

MACRO	OUTPUT CAP.
All	IP: 0.24pF

FUNCTION TABLE

JTAG	
BC	IP
L	H
H	L



BICNJ / BICXNJ / BILCNJ

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		BICNJ			
t_{PLH}	Propagation Delay, BC to IP	0.30	0.30	0.30	0.00
t_{PHL}		0.39	0.39	0.39	0.00
t_r	Output Rise Time, IP	0.49	0.49	0.49	0.00
t_f	Output Fall Time, IP	0.47	0.47	0.47	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BICXNJ				BILCNJ			
t_{PLH}	Propagation Delay, BC to IP	0.52	0.52	0.52	0.00	0.40	0.40	0.40	0.00
t_{PHL}		0.24	0.24	0.24	0.00	0.48	0.48	0.48	0.00
t_r	Output Rise Time, IP	0.60	0.60	0.60	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, IP	0.43	0.43	0.43	0.00	0.55	0.55	0.55	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

NOTE:
Path delay from PAD to DI in the bidirectional buffer will be non-inverted when used together with JTAG bidirectional output buffers.

Non-Inverting CMOS Schmitt Trigger Bidirectional Input Buffer - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V **BISNJ**
5/3.3 V **BISXNJ**
3.3/3.3 V **BILSNJ**

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

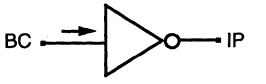
MACRO	OUTPUTS/INPUTS
All	IP / BC

MACRO	INPUT CAP.
All	BC: 0.12pF

MACRO	OUTPUT CAP.
All	IP: 0.27pF

FUNCTION TABLE

JTAG	
BC	IP
L	H
H	L



BISNJ / BISXNJ / BILSNJ

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		BISNJ			
t_{PLH}	Propagation Delay, BC to IP	0.70	0.70	0.70	0.00
t_{PHL}		0.66	0.66	0.66	0.00
t_r	Output Rise Time, IP	1.27	1.27	1.27	0.00
t_f	Output Fall Time, IP	0.59	0.59	0.59	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BISXNJ				BILSNJ			
t_{PLH}	Propagation Delay, BC to IP	1.04	1.04	1.04	0.00	0.93	0.93	0.93	0.00
t_{PHL}		0.42	0.42	0.42	0.00	0.80	0.80	0.80	0.00
t_r	Output Rise Time, IP	1.78	1.78	1.78	0.00	1.77	1.77	1.77	0.00
t_f	Output Fall Time, IP	0.53	0.53	0.53	0.00	0.68	0.68	0.68	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

NOTE:
Path delay from PAD to DI in the bidirectional buffer will be non-inverted when used together with JTAG bidirectional output buffers.

Non-Inverting TTL Bidirectional Input Buffer-JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/5 V

BITNJ
BILTXNJ

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

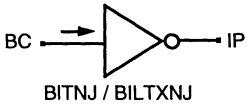
MACRO	OUTPUTS/INPUTS
All	IP / BC

MACRO	INPUT CAP.
All	BC: 0.09pF

MACRO	OUTPUT CAP.
All	IP: 0.23pF

FUNCTION TABLE

JTAG	
BC	IP
L	H
H	L



BITNJ / BILTXNJ

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BITNJ				BILTXNJ			
t_{PLH}	Propagation Delay, BC to IP	0.49	0.49	0.49	0.00	0.51	0.51	0.51	0.00
t_{PHL}		0.38	0.38	0.38	0.00	0.47	0.47	0.47	0.00
t_r	Output Rise Time, IP	1.28	1.28	1.28	0.00	1.30	1.30	1.30	0.00
t_f	Output Fall Time, IP	0.31	0.31	0.31	0.00	0.41	0.41	0.41	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

NOTE:
Path delay from PAD to DI in the bidirectional buffer will be non-inverted when used together with JTAG bidirectional output buffers.

Non-Inverting TTL Schmitt Trigger Bidirectional Input Buffer-JTAG (5 V System/Core Voltage)

5/5 V **BITSNJ**

MACRO	SECTIONS USED
BITSNJ	0/1

Rev. 1.07

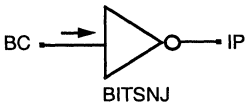
MACRO	OUTPUTS/INPUTS
BITSNJ	IP / BC

MACRO	INPUT CAP.
BITSNJ	BC: 0.18pF

MACRO	OUTPUT CAP.
BITSNJ	IP: 0.35pF

FUNCTION TABLE

JTAG	
BC	IP
L	H
H	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		BITSNJ			
t_{PLH}	Propagation Delay, BC to IP	0.84	0.84	0.84	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_r	Output Rise Time, IP	1.53	1.53	1.53	0.00
t_f	Output Fall Time, IP	0.55	0.55	0.55	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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NOTE:
Path delay from PAD to DI in the bidirectional buffer will be non-inverted when used together with JTAG bidirectional output buffers.

Non-Inverting Open-Drain Bidirectional Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

BN8ODJ
BNL8ODJ

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	BIC,DI,TDO / DO,CKDR,UDDR,IMC,SHDR, TDI,OMC,IPT

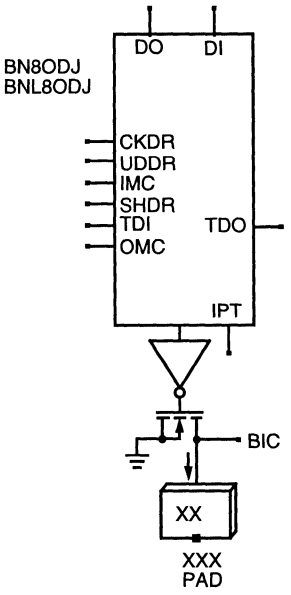
MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF DO: 0.19pF IMC,OMC,SHDR,UDDR: 0.10pF IPT: 0.22pF

MACRO	OUTPUT CAP.
All	PAD: 4.96pF

FUNCTION TABLE

JTAG	
DO	PAD
L	L
H	Z

IPT	DI
L	H
H	L
JTAG	
For JTAG TruthTable Information, See Table 7-1:JTAG Logic Truth Tables - Bidirectionals on page 7-181 in this Manual.	



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BN8ODJ				BNL8ODJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.76	0.76	0.76	0.00	1.13	1.13	1.13	0.00
t_{PHL}		0.68	0.68	0.68	0.00	0.95	0.95	0.95	0.00
t_{PLZ}	Propagation Delay, DO to PAD	0.98	0.98	0.99	0.00	1.33	1.33	1.34	0.00
t_{PZL}		0.97	2.22	3.47	0.03	1.30	2.80	4.30	0.03
t_{PLZ}	Propagation Delay, OMC to PAD	1.82	1.83	1.83	0.00	2.36	2.36	2.37	0.00
t_{PZL}		1.82	2.87	3.92	0.02	2.36	3.61	4.86	0.02
t_{PLZ}	Propagation Delay, TDO to PAD	1.90	1.90	1.91	0.00	2.63	2.64	2.64	0.00
t_{PZL}		1.90	3.15	4.40	0.03	2.63	4.13	5.63	0.03
t_{PLZ}	Propagation Delay, UDDR to PAD	2.08	2.08	2.09	0.00	2.82	2.83	2.83	0.00
t_{PZL}		2.08	3.33	4.58	0.03	2.82	4.32	5.82	0.03
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.53	2.88	5.23	0.05	0.64	3.54	6.44	0.06
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BN8ODJ				BNL8ODJ			
t_{PLH}	Propagation Delay, IMC to DI	0.52	0.54	0.59	0.16	0.71	0.73	0.80	0.22
t_{PHL}		0.74	0.76	0.81	0.19	1.03	1.06	1.14	0.28
t_{PLH}	Propagation Delay, IPT to DI	0.18	0.20	0.24	0.14	0.30	0.32	0.38	0.19
t_{PHL}		0.29	0.31	0.36	0.17	0.45	0.47	0.53	0.21
t_{PLH}	Propagation Delay, TDO to DI	0.81	0.82	0.87	0.16	1.20	1.22	1.29	0.22
t_{PHL}		0.85	0.87	0.93	0.19	1.28	1.31	1.39	0.28
t_{PLH}	Propagation Delay, UDDR to DI	0.89	0.91	0.95	0.13	1.25	1.27	1.33	0.19
t_{PHL}		1.05	1.07	1.14	0.22	1.52	1.55	1.65	0.31
t_r	Output Rise Time, DI	0.20	0.23	0.29	0.22	0.18	0.21	0.32	0.35
t_f	Output Fall Time, DI	0.24	0.25	0.31	0.19	0.24	0.27	0.35	0.26

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

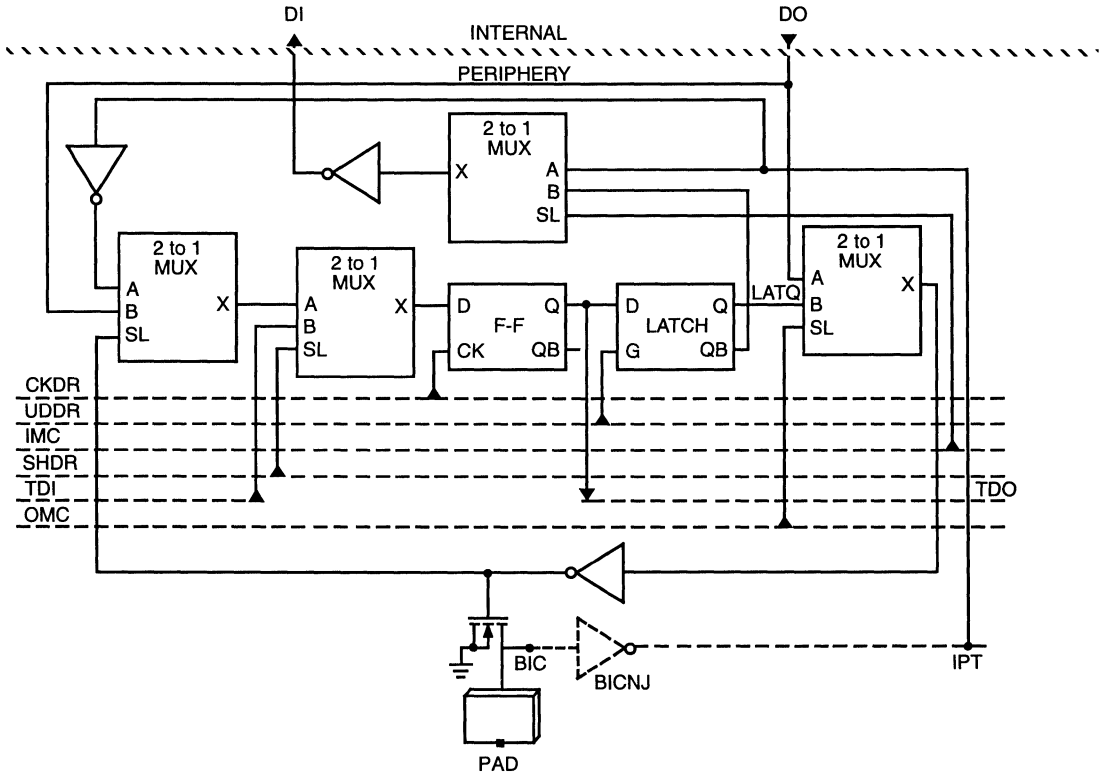
Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BN8ODJ				BNL8ODJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.76	0.76	0.76	0.00	1.13	1.13	1.13	0.00
t_{PHL}		0.68	0.68	0.68	0.00	0.95	0.95	0.95	0.00
t_{PLZ}	Propagation Delay, DO to PAD	1.09	1.09	1.10	0.00	1.39	1.39	1.40	0.00
t_{PZL}		1.08	2.98	4.88	0.04	1.35	3.20	5.05	0.04
t_{PLZ}	Propagation Delay, OMC to PAD	2.17	2.17	2.18	0.00	2.53	2.53	2.54	0.00
t_{PZL}		2.17	3.77	5.37	0.03	2.53	4.08	5.63	0.03
t_{PLZ}	Propagation Delay, TDO to PAD	2.01	2.01	2.02	0.00	2.69	2.69	2.70	0.00
t_{PZL}		2.01	3.91	5.81	0.04	2.69	4.49	6.29	0.04
t_{PLZ}	Propagation Delay, UDDR to PAD	2.19	2.19	2.20	0.00	2.88	2.89	2.89	0.00
t_{PZL}		2.19	4.09	5.99	0.04	2.88	4.73	6.58	0.04
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.53	2.88	5.23	0.05	0.64	3.54	6.44	0.06
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	
		Minimum Requirement	Minimum Requirement
		BN8ODJ	BNL8ODJ
t_{su}	Set Up Time, DO to CKDR	0.65	0.97
t_{su}	Set Up Time, IPT to CKDR	0.65	1.02
t_{su}	Set Up Time, SHDR to CKDR	0.31	0.53
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26
t_h	Hold Time, CKDR to DO	0.15	0.17
t_h	Hold Time, CKDR to IPT	-0.01	-0.09
t_h	Hold Time, CKDR to SHDR	0.15	0.23
t_h	Hold Time, CKDR to TDI	0.31	0.41
t_w	Pulse Width, CKDR(L)	0.41	0.68
t_w	Pulse Width, CKDR(H)	0.77	1.18
t_w	Pulse Width, UDDR(H)	0.74	1.04

FUNCTIONAL DIAGRAM: BNxODJ



Non-Inverting Open-Drain Bidirectional Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V **BN16ODJ**
3.3/3.3 V **BNL16ODJ**

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	BIC,DI,TDO / DO,CKDR,UDDR,IMC,SHDR, TDI,OMC,IPT

MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF DO: 0.19pF IMC,OMC,SHDR,UDDR: 0.10pF IPT: 0.22pF

MACRO	OUTPUT CAP.
All	PAD: 4.96pF

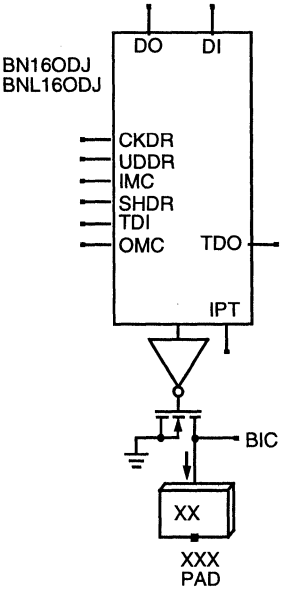
FUNCTION TABLE

JTAG	
DO	PAD
L	L
H	Z

IPT	DI
L	H
H	L

JTAG

For JTAG TruthTable Information, See Table 7-2:JTAG Logic Truth Tables - Bidirectionals on page 7-182 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BN16ODJ				BNL16ODJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.76	0.76	0.76	0.00	1.13	1.13	1.13	0.00
t_{PHL}		0.68	0.68	0.68	0.00	0.95	0.95	0.95	0.00
t_{PLZ}	Propagation Delay, DO to PAD	1.01	1.02	1.02	0.00	1.39	1.39	1.40	0.00
t_{PZL}		1.01	1.86	2.71	0.02	1.35	2.35	3.35	0.02
t_{PLZ}	Propagation Delay, OMC to PAD	1.72	1.73	1.73	0.00	2.23	2.24	2.24	0.00
t_{PZL}		1.72	2.42	3.12	0.01	2.23	3.08	3.93	0.02
t_{PLZ}	Propagation Delay, TDO to PAD	1.94	1.94	1.95	0.00	2.68	2.69	2.69	0.00
t_{PZL}		1.94	2.79	3.64	0.02	2.68	3.68	4.68	0.02
t_{PLZ}	Propagation Delay, UDDR to PAD	2.12	2.12	2.13	0.00	2.89	2.89	2.90	0.00
t_{PZL}		2.12	2.97	3.82	0.02	2.89	3.89	4.89	0.02
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.53	1.98	3.43	0.03	0.64	2.39	4.14	0.03
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BN16ODJ				BNL16ODJ			
t_{PLH}	Propagation Delay, IMC to DI	0.51	0.52	0.56	0.13	0.71	0.73	0.80	0.22
t_{PHL}		0.76	0.78	0.85	0.22	1.03	1.06	1.14	0.28
t_{PLH}	Propagation Delay, IPT to DI	0.16	0.17	0.20	0.12	0.30	0.32	0.38	0.19
t_{PHL}		0.32	0.34	0.40	0.18	0.45	0.47	0.53	0.21
t_{PLH}	Propagation Delay, TDO to DI	0.79	0.80	0.84	0.13	1.20	1.22	1.29	0.22
t_{PHL}		0.88	0.90	0.97	0.21	1.28	1.31	1.39	0.27
t_{PLH}	Propagation Delay, UDDR to DI	0.89	0.91	0.95	0.13	1.25	1.27	1.33	0.19
t_{PHL}		1.05	1.08	1.14	0.22	1.52	1.55	1.65	0.31
t_r	Output Rise Time, DI	0.20	0.23	0.29	0.22	0.18	0.21	0.32	0.35
t_f	Output Fall Time, DI	0.24	0.25	0.31	0.19	0.24	0.27	0.35	0.26

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BN16ODJ				BNL16ODJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.76	0.76	0.76	0.00	1.13	1.13	1.13	0.00
t_{PHL}		0.68	0.68	0.68	0.00	0.95	0.95	0.95	0.00
t_{PLZ}	Propagation Delay, DO to PAD	1.13	1.13	1.14	0.00	1.45	1.45	1.46	0.00
t_{PZL}		1.12	2.37	3.62	0.03	1.41	2.61	3.81	0.02
t_{PLZ}	Propagation Delay, OMC to PAD	1.97	1.98	1.98	0.00	2.36	2.36	2.37	0.00
t_{PZL}		1.97	3.02	4.07	0.02	2.36	3.36	4.36	0.02
t_{PLZ}	Propagation Delay, TDO to PAD	2.05	2.06	2.06	0.00	2.74	2.75	2.75	0.00
t_{PZL}		2.05	3.30	4.55	0.03	2.74	3.94	5.14	0.02
t_{PLZ}	Propagation Delay, UDDR to PAD	2.23	2.24	2.24	0.00	2.95	2.95	2.96	0.00
t_{PZL}		2.23	3.48	4.73	0.03	2.95	4.15	5.35	0.02
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.53	1.98	3.43	0.03	0.64	2.39	4.14	0.03
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		BN16ODJ	BNL16ODJ
t_{su}	Set Up Time, DO to CKDR	0.66	0.99
t_{su}	Set Up Time, IPT to CKDR	0.66	1.02
t_{su}	Set Up Time, SHDR to CKDR	0.31	0.53
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26
t_h	Hold Time, CKDR to DO	0.15	0.17
t_h	Hold Time, CKDR to IPT	-0.01	-0.09
t_h	Hold Time, CKDR to SHDR	0.15	0.23
t_h	Hold Time, CKDR to TDI	0.31	0.41
t_w	Pulse Width, CKDR(L)	0.41	0.68
t_w	Pulse Width, CKDR(H)	0.77	1.18
t_w	Pulse Width, UDDR(H)	0.74	1.04

NOTE: For Functional Diagram see page 7- 79

Non - Inverting 3-State Bidirectional Output Buffers (3.3 V and 5 V System/Core Voltage)

5/5 V **BN4TJ**
5/3.3 V **BNX4TJ**
3.3/5 V **BNLX4TJ**
3.3/3.3 V **BNL4TJ**

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	BIC,DI,TDO / DO,EN,CKDR,UDDR,IMC,SHDR, TDI,OMC,IPT

MACRO	INPUT CAP.
ALL	CKDR,TDI: 0.04pF DO,IPT: 0.24pF EN: 0.21pF IMC,OMC,SHDR,UDDR: 0.10pF

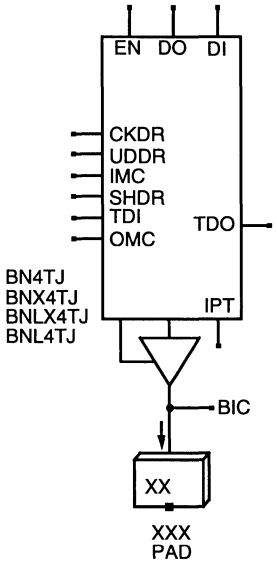
MACRO	OUTPUT CAP.
ALL	PAD: 4.96pF

FUNCTION TABLE

JTAG		
DO	EN	PAD
L	H	L
H	H	H
X	L	Z

IPT	DI
L	H
H	L

JTAG
For JTAG Truth Table Information, See Table 7-2, "JTAG Logic Truth Tables - Bidirectionals," on page 7-182 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BN4TJ				BNLX4TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLZ}	Propagation Delay, DO to PAD	0.99	3.24	5.49	0.05	1.04	3.29	5.54	0.05
t_{PZL}		1.02	2.97	4.92	0.04	0.83	2.88	4.93	0.04
t_{PLZ}	Propagation Delay, EN to PAD	0.83	0.83	0.84	0.00	1.06	1.07	1.07	0.00
t_{PZL}		0.92	2.92	4.92	0.04	1.16	3.51	5.86	0.05
t_{PZH}	Propagation Delay, EN to PAD	0.84	3.14	5.44	0.05	0.89	3.19	5.49	0.05
t_{PHZ}		0.83	0.84	0.84	0.00	0.88	0.89	0.89	0.00
t_{PLZ}	Propagation Delay, OMC to PAD	1.44	3.69	5.94	0.05	1.49	3.74	5.99	0.05
t_{PZL}		1.59	3.54	5.49	0.04	1.40	3.45	5.50	0.04
t_{PLZ}	Propagation Delay, TDO to PAD	1.98	4.23	6.48	0.05	2.04	4.29	6.54	0.05
t_{PZL}		2.01	3.96	5.91	0.04	1.83	3.88	5.93	0.04
t_{PLZ}	Propagation Delay, UDDR to PAD	2.08	4.33	6.58	0.05	2.13	4.38	6.63	0.05
t_{PZL}		2.20	4.15	6.10	0.04	2.01	4.06	6.11	0.04
t_r	Output Rise Time, PAD	0.38	5.53	10.68	0.10	0.38	5.53	10.68	0.10
t_f	Output Fall Time, PAD	0.37	4.17	7.97	0.08	0.28	4.93	9.58	0.09
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BN4TJ				BNLX4TJ			
t_{PLH}	Propagation Delay, IMC to DI	0.75	0.77	0.84	0.22	0.75	0.77	0.84	0.22
t_{PHL}		0.51	0.52	0.56	0.13	0.51	0.52	0.56	0.13
t_{PLH}	Propagation Delay, IPT to DI	0.16	0.17	0.20	0.12	0.16	0.17	0.20	0.12
t_{PHL}		0.32	0.34	0.40	0.18	0.32	0.34	0.40	0.18
t_{PLH}	Propagation Delay, TDO to DI	0.79	0.80	0.84	0.13	0.79	0.80	0.84	0.13
t_{PHL}		0.88	0.90	0.97	0.21	0.88	0.90	0.97	0.21
t_{PLH}	Propagation Delay, UDDR to DI	0.89	0.91	0.95	0.13	0.89	0.91	0.95	0.13
t_{PHL}		1.05	1.08	1.14	0.22	1.05	1.08	1.14	0.22
t_r	Output Rise Time, DI	0.63	0.63	0.63	0.00	0.20	0.23	0.29	0.22
t_f	Output Fall Time, DI	0.41	0.41	0.41	0.00	0.24	0.25	0.31	0.19

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BNX4TJ				BNL4TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLZ}	Propagation Delay, DO to PAD	1.68	3.93	6.18	0.04	1.36	4.56	7.76	0.06
t_{PZL}		1.93	4.88	7.83	0.06	1.37	3.72	6.07	0.05
t_{PLZ}	Propagation Delay, EN to PAD	1.23	1.24	1.24	0.00	1.07	1.07	1.08	0.00
t_{PZL}		1.34	4.14	6.94	0.06	1.15	3.60	6.05	0.05
t_{PZH}	Propagation Delay, EN to PAD	1.47	3.77	6.07	0.05	1.16	4.46	7.76	0.07
t_{PHZ}		1.44	1.45	1.45	0.00	1.13	1.14	1.14	0.00
t_{PLZ}	Propagation Delay, OMC to PAD	2.30	4.55	6.80	0.04	1.98	5.18	8.38	0.06
t_{PZL}		2.62	5.52	8.42	0.06	2.13	4.38	6.63	0.04
t_{PLZ}	Propagation Delay, TDO to PAD	3.15	5.40	7.65	0.04	2.82	6.02	9.22	0.06
t_{PZL}		3.38	6.28	9.18	0.06	2.86	5.11	7.36	0.04
t_{PLZ}	Propagation Delay, UDDR to PAD	3.22	5.47	7.72	0.04	2.90	6.10	9.30	0.06
t_{PZL}		3.55	6.45	9.35	0.06	3.05	5.30	7.55	0.04
t_r	Output Rise Time, PAD	0.43	5.58	10.73	0.10	0.48	7.63	14.78	0.14
t_f	Output Fall Time, PAD	0.34	6.09	11.84	0.11	0.44	5.09	9.74	0.09
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BNX4TJ				BNL4TJ			
t_{PLH}	Propagation Delay, IMC to DI	1.07	1.10	1.19	0.31	1.07	1.10	1.19	0.31
t_{PHL}		0.68	0.70	0.76	0.19	0.68	0.70	0.76	0.19
t_{PLH}	Propagation Delay, IPT to DI	0.28	0.29	0.34	0.16	0.28	0.29	0.34	0.16
t_{PHL}		0.48	0.50	0.57	0.23	0.48	0.50	0.57	0.23
t_{PLH}	Propagation Delay, TDO to DI	1.17	1.19	1.25	0.19	1.17	1.19	1.25	0.19
t_{PHL}		1.32	1.35	1.44	0.31	1.32	1.35	1.44	0.31
t_{PLH}	Propagation Delay, UDDR to DI	1.25	1.27	1.33	0.19	1.25	1.27	1.33	0.19
t_{PHL}		1.52	1.55	1.65	0.31	1.52	1.55	1.65	0.31
t_r	Output Rise Time, DI	0.18	0.21	0.32	0.35	0.18	0.21	0.32	0.35
t_f	Output Fall Time, DI	0.24	0.27	0.35	0.26	0.24	0.27	0.35	0.26

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BN4TJ				BNLX4TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLZ}	Propagation Delay, DO to PAD	0.91	2.06	3.21	0.02	1.01	2.76	4.51	0.04
t_{PZL}		1.10	4.16	7.20	0.06	0.86	3.46	6.06	0.05
t_{PLZ}	Propagation Delay, EN to PAD	0.91	0.92	0.92	0.00	1.10	1.10	1.11	0.00
t_{PZL}		1.01	4.16	7.31	0.06	1.19	4.14	7.09	0.06
t_{PZH}	Propagation Delay, EN to PAD	0.75	1.90	3.05	0.02	0.86	2.61	4.36	0.04
t_{PHZ}		0.75	0.75	0.76	0.00	0.85	0.85	0.86	0.00
t_{PLZ}	Propagation Delay, OMC to PAD	1.36	2.51	3.66	0.02	1.46	3.21	4.96	0.04
t_{PZL}		1.67	4.72	7.77	0.06	1.43	3.98	6.53	0.05
t_{PLZ}	Propagation Delay, TDO to PAD	1.90	3.05	4.20	0.02	2.00	3.70	5.40	0.03
t_{PZL}		2.09	5.14	8.19	0.06	1.86	4.41	6.96	0.05
t_{PLZ}	Propagation Delay, UDDR to PAD	2.00	3.15	4.30	0.02	2.10	3.85	5.60	0.04
t_{PZL}		2.29	5.34	8.39	0.06	2.04	4.59	7.14	0.05
t_r	Output Rise Time, PAD	0.38	5.53	10.68	0.10	0.38	5.53	10.68	0.10
t_f	Output Fall Time, PAD	0.37	4.17	7.97	0.08	0.28	4.93	9.58	0.09
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BNX4TJ				BNL4TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLZ}	Propagation Delay, DO to PAD	1.59	2.74	3.89	0.02	1.31	3.81	6.31	0.05
t_{PZL}		2.02	6.57	11.12	0.09	1.41	4.31	7.21	0.06
t_{PLZ}	Propagation Delay, EN to PAD	1.33	1.34	1.34	0.00	1.10	1.10	1.11	0.00
t_{PZL}		1.44	5.94	10.44	0.09	1.11	1.11	1.12	0.00
t_{PZH}	Propagation Delay, EN to PAD	1.37	2.52	3.67	0.02	1.19	4.19	7.19	0.06
t_{PHZ}		1.35	1.35	1.36	0.00	1.11	3.66	6.21	0.05
t_{PLZ}	Propagation Delay, OMC to PAD	2.21	3.36	4.51	0.02	1.93	4.43	6.93	0.05
t_{PZL}		2.72	7.27	11.82	0.09	2.17	4.97	7.77	0.06
t_{PLZ}	Propagation Delay, TDO to PAD	3.06	4.16	5.26	0.02	2.78	5.23	7.68	0.05
t_{PZL}		3.47	8.02	12.57	0.09	2.90	5.65	8.40	0.05
t_{PLZ}	Propagation Delay, UDDR to PAD	3.13	4.28	5.43	0.02	2.85	5.30	7.75	0.05
t_{PZL}		3.64	8.19	12.74	0.09	3.09	5.89	8.69	0.06
t_r	Output Rise Time, PAD	0.43	5.58	10.73	0.10	0.48	7.63	14.78	0.14
t_f	Output Fall Time, PAD	0.34	6.09	11.84	0.11	0.44	5.09	9.74	0.09
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

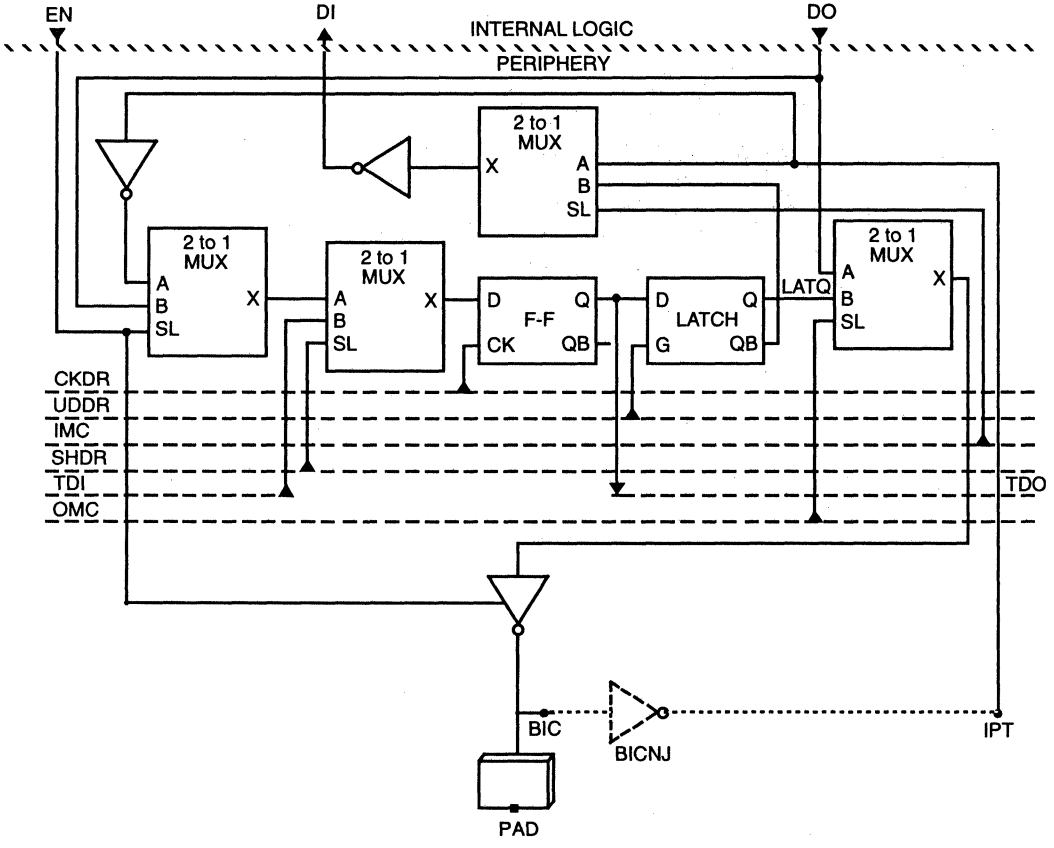
Sym	Parameter	5/5 V	3.3/5 V
		Minimum Requirement	Minimum Requirement
		BN4TJ	BNLX4TJ
t_{su}	Set Up Time, DO,SHDR to CKDR	0.33	0.33
t_{su}	Set Up Time, EN to CKDR	0.63	0.62
t_{su}	Set Up Time, IPT to CKDR	0.67	0.67
t_{su}	Set Up Time, TDI to CKDR	0.13	0.13
t_h	Hold Time, CKDR to DO,SHDR	0.15	0.15
t_h	Hold Time, CKDR to EN	0.11	0.12
t_h	Hold Time, CKDR to IPT	0.00	0.00
t_h	Hold Time, CKDR to TDI	0.31	0.31
t_w	Pulse Width, CKDR(L)	0.42	0.42
t_w	Pulse Width, CKDR(H)	0.78	0.78
t_w	Pulse Width, UDDR(H)	0.75	0.75

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		BNX4TJ	BNL4TJ
t_{su}	Set Up Time, DO to CKDR	0.62	0.62
t_{su}	Set Up Time, EN to CKDR	1.16	0.99
t_{su}	Set Up Time, IPT to CKDR	1.03	1.03
t_{su}	Set Up Time, SHDR to CKDR	0.53	0.53
t_{su}	Set Up Time, TDI to CKDR	0.26	0.26
t_h	Hold Time, CKDR to DO	0.19	0.20
t_h	Hold Time, CKDR to EN	0.01	0.07
t_h	Hold Time, CKDR to IPT	-0.08	-0.08
t_h	Hold Time, CKDR to SHDR	0.23	0.23
t_h	Hold Time, CKDR to TDI	0.41	0.41
t_w	Pulse Width, CKDR(L)	0.72	0.72
t_w	Pulse Width, CKDR(H)	1.18	1.18
t_w	Pulse Width, UDDR(H)	1.05	1.05

FUNCTIONAL DIAGRAM: BNXTJ



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Non-Inverting 3-State Bidirectional Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V **BN8TJ**
5/3.3 V **BNX8TJ**
3.3/5 V **BNLX8TJ**
3.3/3.3 V **BNL8TJ**

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	BIC,DI,TDO / DO,EN,CKDR,UDDR,IMC,SHDR, TDI,OMC,IPT

MACRO	INPUT CAP.
ALL	CKDR,TDI: 0.04pF DO,IPT: 0.24pF EN: 0.21pF IMC,OMC,SHDR,UDDR: 0.10pF

MACRO	OUTPUT CAP.
ALL	PAD: 5.10pF

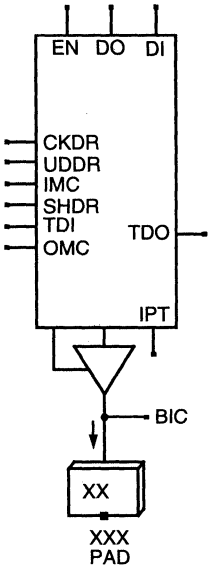
FUNCTION TABLE

JTAG		
DO	EN	PAD
L	H	L
H	H	H
X	L	Z

IPT	DI
L	H
H	L

JTAG
For JTAG Truth Table Information, See Table 7-2, "JTAG Logic Truth Tables - Bidirectionals," on page 7-182 in this Manual.

BN8TJ
BNX8TJ
BNLX8TJ
BNL8TJ



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BN8TJ				BNLX8TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLZ}	Propagation Delay, DO to PAD	0.92	2.22	3.52	0.03	1.34	2.69	4.04	0.03
t_{PZL}		1.10	2.35	3.60	0.03	1.16	2.26	3.36	0.02
t_{PLZ}	Propagation Delay, EN to PAD	0.91	0.91	0.92	0.00	1.26	1.26	1.27	0.00
t_{PZL}		1.00	2.25	3.50	0.03	1.35	2.55	3.75	0.02
t_{PZH}	Propagation Delay, EN to PAD	0.75	2.05	3.35	0.03	1.19	2.59	3.99	0.03
t_{PHZ}		0.73	0.74	0.74	0.00	1.18	1.18	1.19	0.00
t_{PLZ}	Propagation Delay, OMC to PAD	1.37	2.67	3.97	0.03	1.79	3.14	4.49	0.03
t_{PZL}		1.65	2.90	4.15	0.03	1.71	2.66	3.61	0.02
t_{PLZ}	Propagation Delay, TDO to PAD	1.91	3.21	4.51	0.03	2.33	3.68	5.03	0.03
t_{PZL}		2.09	3.34	4.59	0.03	2.15	3.25	4.35	0.02
t_{PLZ}	Propagation Delay, UDDR to PAD	2.00	3.30	4.60	0.03	2.43	3.78	5.13	0.03
t_{PZL}		2.27	3.52	4.77	0.03	2.33	3.43	4.53	0.02
t_r	Output Rise Time, PAD	0.29	3.24	6.19	0.06	0.59	3.54	6.49	0.06
t_f	Output Fall Time, PAD	0.49	2.74	4.99	0.05	0.54	2.84	5.14	0.05
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BN8TJ				BNLX8TJ			
t_{PLH}	Propagation Delay, IMC to DI	0.75	0.77	0.84	0.22	0.75	0.77	0.84	0.22
t_{PHL}		0.51	0.52	0.56	0.13	0.51	0.52	0.56	0.13
t_{PLH}	Propagation Delay, IPT to DI	0.16	0.17	0.20	0.12	0.16	0.17	0.20	0.12
t_{PHL}		0.32	0.34	0.40	0.18	0.32	0.34	0.40	0.18
t_{PLH}	Propagation Delay, TDO to DI	0.79	0.80	0.84	0.13	0.79	0.80	0.84	0.13
t_{PHL}		0.88	0.90	0.97	0.21	0.88	0.90	0.97	0.21
t_{PLH}	Propagation Delay, UDDR to DI	0.89	0.91	0.95	0.13	0.89	0.91	0.95	0.13
t_{PHL}		1.05	1.08	1.14	0.22	1.05	1.08	1.14	0.22
t_r	Output Rise Time, DI	0.20	0.23	0.29	0.22	0.20	0.23	0.29	0.22
t_f	Output Fall Time, DI	0.24	0.25	0.31	0.19	0.24	0.25	0.31	0.19

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BNX8TJ				BNL8TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLZ}	Propagation Delay, DO to PAD	2.03	3.38	4.73	0.03	1.30	3.15	5.00	0.04
t_{PZL}		2.04	3.59	5.14	0.03	1.49	2.99	4.49	0.03
t_{PLZ}	Propagation Delay, EN to PAD	1.47	1.48	1.48	0.00	1.19	1.20	1.20	0.00
t_{PZL}		1.57	3.07	4.57	0.03	1.27	2.77	4.27	0.03
t_{PZH}	Propagation Delay, EN to PAD	1.85	3.25	4.65	0.03	1.10	2.95	4.80	0.04
t_{PHZ}		1.84	1.85	1.85	0.00	1.07	1.08	1.08	0.00
t_{PLZ}	Propagation Delay, OMC to PAD	2.65	4.00	5.35	0.03	1.92	3.77	5.62	0.04
t_{PZL}		2.72	4.27	5.82	0.03	2.18	3.68	5.18	0.03
t_{PLZ}	Propagation Delay, TDO to PAD	3.50	4.85	6.20	0.03	2.77	4.57	6.37	0.04
t_{PZL}		3.45	5.00	6.55	0.03	2.89	4.34	5.79	0.03
t_{PLZ}	Propagation Delay, UDDR to PAD	3.57	4.92	6.27	0.03	2.84	4.64	6.44	0.04
t_{PZL}		3.64	5.14	6.64	0.03	3.09	4.54	5.99	0.03
t_r	Output Rise Time, PAD	0.78	3.63	6.48	0.06	0.35	4.40	8.45	0.08
t_f	Output Fall Time, PAD	0.56	3.41	6.26	0.06	0.59	3.34	6.09	0.05
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BNX8TJ				BNL8TJ			
t_{PLH}	Propagation Delay, IMC to DI	1.07	1.10	1.19	0.31	1.07	1.10	1.19	0.31
t_{PHL}		0.68	0.70	0.76	0.19	0.68	0.70	0.76	0.19
t_{PLH}	Propagation Delay, IPT to DI	0.28	0.29	0.34	0.16	0.28	0.29	0.34	0.16
t_{PHL}		0.48	0.50	0.57	0.23	0.48	0.50	0.57	0.23
t_{PLH}	Propagation Delay, TDO to DI	1.17	1.19	1.25	0.19	1.17	1.19	1.25	0.19
t_{PHL}		1.32	1.35	1.44	0.31	1.32	1.35	1.44	0.31
t_{PLH}	Propagation Delay, UDDR to DI	1.25	1.27	1.33	0.19	1.25	1.27	1.33	0.19
t_{PHL}		1.52	1.55	1.65	0.31	1.52	1.55	1.65	0.31
t_r	Output Rise Time, DI	0.18	0.21	0.32	0.35	0.18	0.21	0.32	0.35
t_f	Output Fall Time, DI	0.24	0.27	0.35	0.26	0.24	0.27	0.35	0.26

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BN8TJ				BNLX8TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLZ}	Propagation Delay, DO to PAD	0.85	1.50	2.15	0.01	1.28	2.33	3.38	0.02
t_{PZL}		1.20	3.10	5.00	0.04	1.22	2.62	4.02	0.03
t_{PLZ}	Propagation Delay, EN to PAD	1.01	1.02	1.02	0.00	1.30	1.31	1.31	0.00
t_{PZL}		1.11	3.01	4.91	0.04	1.40	2.85	4.30	0.03
t_{PZH}	Propagation Delay, EN to PAD	0.67	1.32	1.97	0.01	1.12	2.22	3.32	0.02
t_{PHZ}		0.66	0.67	0.67	0.00	1.11	1.11	1.12	0.00
t_{PLZ}	Propagation Delay, OMC to PAD	1.30	1.95	2.60	0.01	1.72	2.77	3.82	0.02
t_{PZL}		1.76	3.61	5.46	0.04	1.77	3.12	4.47	0.03
t_{PLZ}	Propagation Delay, TDO to PAD	1.84	2.49	3.14	0.01	2.26	3.31	4.36	0.02
t_{PZL}		2.19	4.04	5.89	0.04	2.20	3.55	4.90	0.03
t_{PLZ}	Propagation Delay, UDDR to PAD	1.93	2.58	3.23	0.01	2.36	3.41	4.46	0.02
t_{PZL}		2.38	4.23	6.08	0.04	2.38	3.73	5.08	0.03
t_r	Output Rise Time, PAD	0.29	3.24	6.19	0.06	0.59	3.54	6.49	0.06
t_f	Output Fall Time, PAD	0.49	2.74	4.99	0.05	0.54	2.84	5.14	0.05
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

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TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BNX8TJ				BNL8TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLZ}	Propagation Delay, DO to PAD	1.80	2.60	3.40	0.02	1.27	2.67	4.07	0.03
t_{PZL}		2.15	4.50	6.85	0.05	1.54	3.34	5.14	0.04
t_{PLZ}	Propagation Delay, EN to PAD	1.62	1.62	1.63	0.00	1.25	1.25	1.26	0.00
t_{PZL}		1.72	4.02	6.32	0.05	1.33	3.18	5.03	0.04
t_{PZH}	Propagation Delay, EN to PAD	1.61	2.41	3.21	0.02	1.06	2.51	3.96	0.03
t_{PHZ}		1.60	1.60	1.61	0.00	1.04	1.04	1.05	0.00
t_{PLZ}	Propagation Delay, OMC to PAD	2.42	3.22	4.02	0.02	1.89	3.29	4.69	0.03
t_{PZL}		2.83	5.18	7.53	0.05	2.23	4.03	5.83	0.04
t_{PLZ}	Propagation Delay, TDO to PAD	3.28	4.03	4.78	0.01	2.74	4.14	5.54	0.03
t_{PZL}		3.56	5.91	8.26	0.05	2.95	4.75	6.55	0.04
t_{PLZ}	Propagation Delay, UDDR to PAD	3.35	4.10	4.85	0.01	2.81	4.21	5.61	0.03
t_{PZL}		3.75	6.10	8.45	0.05	3.14	4.94	6.74	0.04
t_r	Output Rise Time, PAD	0.78	3.63	6.48	0.06	0.35	4.40	8.45	0.08
t_f	Output Fall Time, PAD	0.56	3.41	6.26	0.06	0.59	3.34	6.09	0.05
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/5 V
		Minimum Requirement	Minimum Requirement
		BN8TJ	BNLX8TJ
t_{su}	Set Up Time, DO,SHDR to CKDR	0.33	0.32
t_{su}	Set Up Time, EN to CKDR	0.64	0.63
t_{su}	Set Up Time, IPT to CKDR	0.67	0.67
t_{su}	Set Up Time, TDI to CKDR	0.13	0.13
t_h	Hold Time, CKDR to DO,SHDR	0.15	0.15
t_h	Hold Time, CKDR to EN	0.10	0.11
t_h	Hold Time, CKDR to IPT	0.00	0.00
t_h	Hold Time, CKDR to TDI	0.31	0.31
t_w	Pulse Width, CKDR(L)	0.42	0.42
t_w	Pulse Width, CKDR(H)	0.78	0.78
t_w	Pulse Width, UDDR(H)	0.75	0.75

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		BNX8TJ	BNL8TJ
t_{su}	Set Up Time, DO to CKDR	0.63	0.61
t_{su}	Set Up Time, EN to CKDR	1.13	1.00
t_{su}	Set Up Time, IPT to CKDR	1.03	1.03
t_{su}	Set Up Time, SHDR to CKDR	0.53	0.53
t_{su}	Set Up Time, TDI to CKDR	0.26	0.26
t_h	Hold Time, CKDR to DO	0.20	0.20
t_h	Hold Time, CKDR to EN	0.01	0.05
t_h	Hold Time, CKDR to IPT	-0.08	-0.08
t_h	Hold Time, CKDR to SHDR	0.23	0.23
t_h	Hold Time, CKDR to TDI	0.41	0.41
t_w	Pulse Width, CKDR(L)	0.72	0.72
t_w	Pulse Width, CKDR(H)	1.18	1.18
t_w	Pulse Width, UDDR(H)	1.05	1.05

NOTE:
For Functional Diagram see page 7-88

Non-Inverting 3-State Bidirectional Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/5 V
3.3/3.3 V

BN16TJ
BNLX16TJ
BNL16TJ

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	BIC,DI,TDO / DO,EN,CKDR,UDDR,IMC,SHDR, TDI,OMC,IPT

MACRO	INPUT CAP.
ALL	CKDR,TDI: 0.04pF DO,EN,IPT: 0.24pF IMC,OMC,SHDR,UDDR: 0.10pF

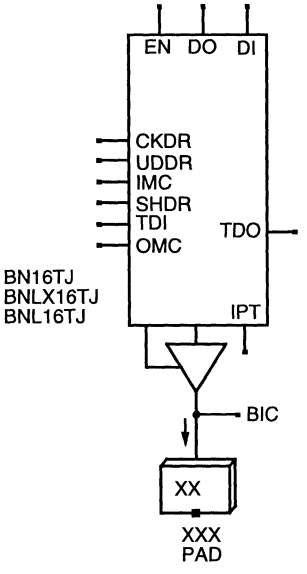
MACRO	OUTPUT CAP.
ALL	PAD: 5.76pF

FUNCTION TABLE

JTAG		
DO	EN	PAD
L	H	L
H	H	H
X	L	Z

IPT	DI
L	H
H	L

JTAG
For JTAG Truth Table Information, See Table 7-2, "JTAG Logic Truth Tables - Bidirectionals," on page 7-182 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BN16TJ				BNLX16TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLZ}	Propagation Delay, DO to PAD	1.05	1.85	2.65	0.02	1.30	2.65	4.00	0.03
t_{PZL}		1.18	1.98	2.78	0.02	1.07	1.72	2.37	0.01
t_{PLZ}	Propagation Delay, EN to PAD	0.92	0.92	0.93	0.00	1.01	1.01	1.02	0.00
t_{PZL}		1.00	1.85	2.70	0.02	1.10	1.75	2.40	0.01
t_{PZH}	Propagation Delay, EN to PAD	0.89	1.74	2.59	0.02	1.13	2.53	3.93	0.03
t_{PHZ}		0.88	0.88	0.89	0.00	1.12	1.13	1.13	0.00
t_{PLZ}	Propagation Delay, OMC to PAD	1.50	2.30	3.10	0.02	1.75	3.10	4.45	0.03
t_{PZL}		1.73	2.53	3.33	0.02	1.61	2.16	2.71	0.01
t_{PLZ}	Propagation Delay, TDO to PAD	2.04	2.84	3.64	0.02	2.29	3.64	4.99	0.03
t_{PZL}		2.17	2.97	3.77	0.02	2.05	2.65	3.25	0.01
t_{PLZ}	Propagation Delay, UDDR to PAD	2.14	2.94	3.74	0.02	2.39	3.74	5.09	0.03
t_{PZL}		2.35	3.15	3.95	0.02	2.23	2.83	3.43	0.01
t_r	Output Rise Time, PAD	0.43	2.13	3.83	0.03	0.58	3.53	6.48	0.06
t_f	Output Fall Time, PAD	0.50	1.90	3.30	0.03	0.46	1.61	2.76	0.02
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		BN16TJ				BNLX16TJ			
t_{PLH}	Propagation Delay, IMC to DI	0.75	0.77	0.84	0.22	0.75	0.77	0.84	0.22
t_{PHL}		0.51	0.52	0.56	0.13	0.51	0.52	0.56	0.13
t_{PLH}	Propagation Delay, IPT to DI	0.16	0.17	0.20	0.12	0.16	0.17	0.20	0.12
t_{PHL}		0.32	0.34	0.40	0.18	0.32	0.34	0.40	0.18
t_{PLH}	Propagation Delay, TDO to DI	0.79	0.80	0.84	0.13	0.79	0.80	0.84	0.13
t_{PHL}		0.88	0.90	0.97	0.21	0.88	0.90	0.97	0.21
t_{PLH}	Propagation Delay, UDDR to DI	0.89	0.91	0.95	0.13	0.89	0.91	0.95	0.13
t_{PHL}		1.05	1.08	1.14	0.22	1.05	1.08	1.14	0.22
t_r	Output Rise Time, DI	0.20	0.23	0.29	0.22	0.20	0.23	0.29	0.22
t_f	Output Fall Time, DI	0.24	0.25	0.31	0.19	0.24	0.25	0.31	0.19

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		BNL16TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00
t_{PLZ}	Propagation Delay, DO to PAD	1.49	2.64	3.79	0.02
t_{PZL}		1.59	2.59	3.59	0.02
t_{PLZ}	Propagation Delay, ENto PAD	1.20	1.21	1.21	0.00
t_{PZL}		1.28	2.28	3.28	0.02
t_{PZH}	Propagation Delay, ENto PAD	1.26	2.41	3.56	0.02
t_{PHZ}		1.24	1.25	1.25	0.00
t_{PLZ}	Propagation Delay, OMC to PAD	2.11	3.26	4.41	0.02
t_{PZL}		2.27	3.07	3.87	0.02
t_{PLZ}	Propagation Delay, TDO to PAD	2.97	4.07	5.17	0.02
t_{PZL}		2.99	3.94	4.89	0.02
t_{PLZ}	Propagation Delay, UDDR to PAD	3.05	4.15	5.25	0.02
t_{PZL}		3.20	4.15	5.10	0.02
t_r	Output Rise Time, PAD	0.53	2.88	5.23	0.05
t_f	Output Fall Time, PAD	0.59	2.29	3.99	0.03
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		BNL16TJ			
t_{PLH}	Propagation Delay, IMC to DI	1.07	1.10	1.19	0.31
t_{PHL}		0.68	0.70	0.76	0.19
t_{PLH}	Propagation Delay, IPT to DI	0.28	0.29	0.34	0.16
t_{PHL}		0.48	0.50	0.57	0.23
t_{PLH}	Propagation Delay, TDO to DI	1.17	1.19	1.25	0.19
t_{PHL}		1.32	1.35	1.44	0.31
t_{PLH}	Propagation Delay, UDDR to DI	1.25	1.27	1.33	0.19
t_{PHL}		1.52	1.55	1.65	0.31
t_r	Output Rise Time, DI	0.18	0.21	0.32	0.35
t_f	Output Fall Time, DI	0.24	0.27	0.35	0.26

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		BN16TJ				BNLX16TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLZ}	Propagation Delay, DO to PAD	0.92	1.37	1.82	0.01	1.23	2.28	3.33	0.02
t_{PZL}		0.70	0.70	0.70	0.00	1.11	1.86	2.61	0.01
t_{PLZ}	Propagation Delay, EN to PAD	1.03	1.03	1.04	0.00	1.05	1.06	1.06	0.00
t_{PZL}		1.12	2.37	3.62	0.03	1.14	1.94	2.74	0.02
t_{PZH}	Propagation Delay, EN to PAD	0.75	1.20	1.65	0.01	1.06	2.16	3.26	0.02
t_{PHZ}		0.75	0.75	0.76	0.00	1.05	1.06	1.06	0.00
t_{PLZ}	Propagation Delay, OMC to PAD	1.37	1.82	2.27	0.01	1.69	2.74	3.79	0.02
t_{PZL}		1.84	2.84	3.84	0.02	1.67	2.32	2.97	0.01
t_{PLZ}	Propagation Delay, TDO to PAD	1.91	2.36	2.81	0.01	2.23	3.28	4.33	0.02
t_{PZL}		2.27	3.47	4.67	0.02	2.10	2.85	3.60	0.01
t_{PLZ}	Propagation Delay, UDDR to PAD	2.01	2.46	2.91	0.01	2.32	3.37	4.42	0.02
t_{PZL}		2.45	3.65	4.85	0.02	2.28	3.03	3.78	0.01
t_r	Output Rise Time, PAD	0.43	2.13	3.83	0.03	0.58	3.53	6.48	0.06
t_f	Output Fall Time, PAD	0.50	1.90	3.30	0.03	0.46	1.61	2.76	0.02
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		BNL16TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00
t_{PLZ}	Propagation Delay, DO to PAD	1.43	2.33	3.23	0.02
t_{PZL}		1.64	2.84	4.04	0.02
t_{PLZ}	Propagation Delay, ENto PAD	1.26	1.27	1.27	0.00
t_{PZL}		1.34	2.54	3.74	0.02
t_{PZH}	Propagation Delay, ENto PAD	1.20	2.10	3.00	0.02
t_{PHZ}		1.18	1.19	1.19	0.00
t_{PLZ}	Propagation Delay, OMC to PAD	2.05	2.95	3.85	0.02
t_{PZL}		2.33	3.33	4.33	0.02
t_{PLZ}	Propagation Delay, TDO to PAD	2.91	3.81	4.71	0.02
t_{PZL}		3.05	4.20	5.35	0.02
t_{PLZ}	Propagation Delay, UDDR to PAD	2.99	3.89	4.79	0.02
t_{PZL}		3.26	4.41	5.56	0.02
t_r	Output Rise Time, PAD	0.53	2.88	5.23	0.05
t_f	Output Fall Time, PAD	0.59	2.29	3.99	0.03
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/5 V
		Minimum Requirement	Minimum Requirement
		BN16TJ	BNLX16TJ
t_{su}	Set Up Time, DO,SHDR to CKDR	0.33	0.33
t_{su}	Set Up Time, EN to CKDR	0.65	0.65
t_{su}	Set Up Time, IPT to CKDR	0.65	0.67
t_{su}	Set Up Time, TDI to CKDR	0.13	0.13
t_h	Hold Time, CKDR to DO,SHDR	0.14	0.15
t_h	Hold Time, CKDR to EN	0.08	0.08
t_h	Hold Time, CKDR to IPT	0.00	0.00
t_h	Hold Time, CKDR to TDI	0.31	0.31
t_w	Pulse Width, CKDR(L)	0.42	0.42
t_w	Pulse Width, CKDR(H)	0.78	0.78
t_w	Pulse Width, UDDR(H)	0.75	0.75

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V
		Minimum Requirement
	BNL16TJ	
t_{su}	Set Up Time, DO to CKDR	0.63
t_{su}	Set Up Time, EN,IPT to CKDR	1.04
t_{su}	Set Up Time, SHDR to CKDR	0.53
t_{su}	Set Up Time, TDI to CKDR	0.26
t_h	Hold Time, CKDR to DO	0.19
t_h	Hold Time, CKDR to EN	0.03
t_h	Hold Time, CKDR to IPT	-0.08
t_h	Hold Time, CKDR to SHDR	0.23
t_h	Hold Time, CKDR to TDI	0.41
t_w	Pulse Width, CKDR(L)	0.72
t_w	Pulse Width, CKDR(H)	1.18
t_w	Pulse Width, UDDR(H)	1.05

NOTE:
For Functional Diagram see page 7-88

Non-Inverting 3-State Bidirectional Output Buffers - JTAG With Slew Rate Control (S2) (5 V System/Core Voltage)

5/5 V

BN4TS2J
BN8TS2J
BN16TS2J

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	BIC,DI,TDO / DO,EN,CKDR,UDDR,IMC,SHDR, TDI,OMC,IPT

MACRO	INPUT CAP.
BN4TS2J,BN8TS2J	CKDR,TDI: 0.04pF DO,IPT: 0.24pF EN: 0.21pF IMC,OMC,SHDR,UDDR: 0.10pF
BN16TS2J	CKDR,TDI: 0.04pF DO,EN,IPT: 0.24pF IMC,OMC,SHDR,UDDR: 0.10pF

MACRO	OUTPUT CAP.
BN4TS2J	PAD: 4.96pF
BN8TS2J	PAD: 5.10pF
BN16TS2J	PAD: 5.76pF

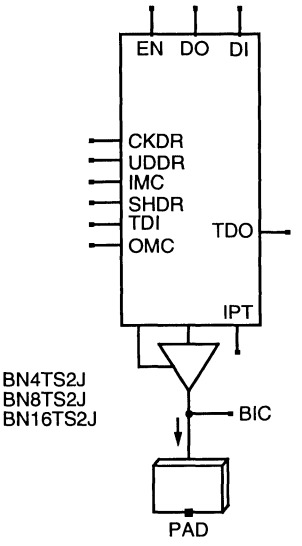
FUNCTION TABLE

JTAG		
DO	EN	PAD
L	H	L
H	H	H
X	L	Z

IPT	DI
L	H
H	L

JTAG

For JTAG Truth Table Information, See Table 7-2, "JTAG Logic Truth Tables - Bidirectionals," on page 7-182 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
BN4TS2J					
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.64	3.94	6.24	0.05
t_{PHL}		1.43	3.43	5.43	0.04
t_{PLZ}	Propagation Delay, EN to PAD	1.24	1.25	1.25	0.00
t_{PZL}		1.33	3.38	5.43	0.04
t_{PZH}	Propagation Delay, EN to PAD	1.49	3.84	6.19	0.05
t_{PHZ}		1.49	1.49	1.50	0.00
t_{PLH}	Propagation Delay, OMC to PAD	2.09	4.39	6.69	0.05
t_{PHL}		1.99	3.94	5.89	0.04
t_{PLH}	Propagation Delay, TDO to PAD	2.63	4.93	7.23	0.05
t_{PHL}		2.42	4.37	6.32	0.04
t_{PLH}	Propagation Delay, UDDR to PAD	2.72	5.02	7.32	0.05
t_{PHL}		2.61	4.56	6.51	0.04
t_r	Output Rise Time, PAD	0.70	5.80	10.90	0.10
t_f	Output Fall Time, PAD	0.55	4.35	8.15	0.08
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
BN8TS2J					
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.58	2.98	4.38	0.03
t_{PHL}		1.37	2.67	3.97	0.03
t_{PLZ}	Propagation Delay, EN to PAD	1.19	1.20	1.20	0.00
t_{PZL}		1.28	2.58	3.88	0.03
t_{PZH}	Propagation Delay, EN to PAD	1.43	2.83	4.23	0.03
t_{PHZ}		1.43	1.43	1.44	0.00
t_{PLH}	Propagation Delay, OMC to PAD	2.03	3.43	4.83	0.03
t_{PHL}		1.93	3.23	4.53	0.03
t_{PLH}	Propagation Delay, TDO to PAD	2.57	3.97	5.37	0.03
t_{PHL}		2.36	3.66	4.96	0.03
t_{PLH}	Propagation Delay, UDDR to PAD	2.67	4.07	5.47	0.03
t_{PHL}		2.54	3.84	5.14	0.03
t_r	Output Rise Time, PAD	0.79	3.69	6.59	0.06
t_f	Output Fall Time, PAD	0.70	2.95	5.20	0.05
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00
BN16TS2J					
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.72	2.67	3.62	0.02
t_{PHL}		1.52	2.42	3.32	0.02
t_{PLZ}	Propagation Delay, EN to PAD	1.27	1.27	1.28	0.00
t_{PZL}		1.36	2.26	3.16	0.02
t_{PZH}	Propagation Delay, EN to PAD	1.57	2.52	3.47	0.02
t_{PHZ}		1.56	1.56	1.57	0.00
t_{PLH}	Propagation Delay, OMC to PAD	2.18	3.13	4.08	0.02
t_{PHL}		2.07	2.97	3.87	0.02
t_{PLH}	Propagation Delay, TDO to PAD	2.72	3.67	4.62	0.02
t_{PHL}		2.50	3.40	4.30	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	2.81	3.76	4.71	0.02
t_{PHL}		2.68	3.58	4.48	0.02
t_r	Output Rise Time, PAD	0.78	2.53	4.28	0.04
t_f	Output Fall Time, PAD	0.64	2.09	3.54	0.03
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
BN4TS2J					
t_{PLH}	Propagation Delay, IMC to DI	0.75	0.77	0.84	0.22
t_{PHL}		0.51	0.52	0.56	0.13
t_{PLH}	Propagation Delay, IPT to DI	0.16	0.17	0.20	0.12
t_{PHL}		0.32	0.34	0.40	0.18
t_{PLH}	Propagation Delay, TDO to DI	0.79	0.80	0.84	0.13
t_{PHL}		0.88	0.90	0.97	0.21
t_{PLH}	Propagation Delay, UDDR to DI	0.89	0.91	0.95	0.13
t_{PHL}		1.05	1.08	1.14	0.22
t_r	Output Rise Time, DI	0.20	0.23	0.29	0.22
t_f	Output Fall Time, DI	0.24	0.25	0.31	0.19
BN8TS2J					
t_{PLH}	Propagation Delay, IMC to DI	0.75	0.77	0.84	0.22
t_{PHL}		0.51	0.52	0.56	0.13
t_{PLH}	Propagation Delay, IPT to DI	0.16	0.17	0.20	0.12
t_{PHL}		0.32	0.34	0.40	0.18
t_{PLH}	Propagation Delay, TDO to DI	0.79	0.80	0.84	0.13
t_{PHL}		0.88	0.90	0.97	0.21
t_{PLH}	Propagation Delay, UDDR to DI	0.89	0.91	0.95	0.13
t_{PHL}		1.05	1.08	1.14	0.22
t_r	Output Rise Time, DI	0.20	0.23	0.29	0.22
t_f	Output Fall Time, DI	0.24	0.25	0.31	0.19
BN16TS2J					
t_{PLH}	Propagation Delay, IMC to DI	0.75	0.77	0.84	0.22
t_{PHL}		0.51	0.52	0.56	0.13
t_{PLH}	Propagation Delay, IPT to DI	0.16	0.17	0.20	0.12
t_{PHL}		0.32	0.34	0.40	0.18
t_{PLH}	Propagation Delay, TDO to DI	0.79	0.80	0.84	0.13
t_{PHL}		0.88	0.90	0.97	0.21
t_{PLH}	Propagation Delay, UDDR to DI	0.89	0.91	0.95	0.13
t_{PHL}		1.05	1.08	1.14	0.22
t_r	Output Rise Time, DI	0.20	0.23	0.29	0.22
t_f	Output Fall Time, DI	0.24	0.25	0.31	0.19

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
BN4TS2J					
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.46	2.66	3.86	0.02
t_{PHL}		1.54	4.64	7.74	0.06
t_{PLZ}	Propagation Delay, EN to PAD	1.36	1.37	1.37	0.00
t_{PZL}		1.45	4.65	7.85	0.06
t_{PZH}	Propagation Delay, EN to PAD	1.31	2.51	3.71	0.02
t_{PHZ}		1.30	1.31	1.31	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.91	3.11	4.31	0.02
t_{PHL}		2.10	5.15	8.20	0.06
t_{PLH}	Propagation Delay, TDO to PAD	2.45	3.65	4.85	0.02
t_{PHL}		2.53	5.58	8.63	0.06
t_{PLH}	Propagation Delay, UDDR to PAD	2.55	3.75	4.95	0.02
t_{PHL}		2.73	5.78	8.83	0.06
t_r	Output Rise Time, PAD	0.70	5.80	10.90	0.10
t_f	Output Fall Time, PAD	0.55	4.35	8.15	0.08
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00
BN8TS2J					
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.35	2.15	2.95	0.02
t_{PHL}		1.52	3.47	5.42	0.04
t_{PLZ}	Propagation Delay, EN to PAD	1.34	1.35	1.35	0.00
t_{PZL}		1.44	3.44	5.44	0.04
t_{PZH}	Propagation Delay, EN to PAD	1.19	1.99	2.79	0.02
t_{PHZ}		1.18	1.19	1.19	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.80	2.60	3.40	0.02
t_{PHL}		2.07	4.02	5.97	0.04
t_{PLH}	Propagation Delay, TDO to PAD	2.34	3.14	3.94	0.02
t_{PHL}		2.51	4.41	6.31	0.04
t_{PLH}	Propagation Delay, UDDR to PAD	2.44	3.24	4.04	0.02
t_{PHL}		2.69	4.64	6.59	0.04
t_r	Output Rise Time, PAD	0.79	3.69	6.59	0.06
t_f	Output Fall Time, PAD	0.70	2.95	5.20	0.05
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
BN16TS2J					
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.49	2.09	2.69	0.01
t_{PHL}		1.66	2.96	4.26	0.03
t_{PLZ}	Propagation Delay, EN to PAD	1.42	1.42	1.43	0.00
t_{PZL}		1.50	2.80	4.10	0.03
t_{PZH}	Propagation Delay, EN to PAD	1.32	1.92	2.52	0.01
t_{PHZ}		1.31	1.32	1.32	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.94	2.54	3.14	0.01
t_{PHL}		2.21	3.51	4.81	0.03
t_{PLH}	Propagation Delay, TDO to PAD	2.48	3.03	3.58	0.01
t_{PHL}		2.64	3.94	5.24	0.03
t_{PLH}	Propagation Delay, UDDR to PAD	2.58	3.13	3.68	0.01
t_{PHL}		2.82	4.12	5.42	0.03
t_r	Output Rise Time, PAD	0.78	2.53	4.28	0.04
t_f	Output Fall Time, PAD	0.64	2.09	3.54	0.03
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V
		Minimum Requirement
BN4TS2J		
t_{su}	Set Up Time, DO,SHDR to CKDR	0.32
t_{su}	Set Up Time, EN to CKDR	0.63
t_{su}	Set Up Time, IPT to CKDR	0.67
t_{su}	Set Up Time, TDI to CKDR	0.13
t_h	Hold Time, CKDR to DO,SHDR	0.15
t_h	Hold Time, CKDR to EN	0.11
t_h	Hold Time, CKDR to IPT	0.00
t_h	Hold Time, CKDR to TDI	0.31
t_w	Pulse Width, CKDR(L)	0.42
t_w	Pulse Width, CKDR(H)	0.78
t_w	Pulse Width, UDDR(H)	0.75

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V
		Minimum Requirement
	BN8TS2J	
t_{su}	Set Up Time, DO,SHDR to CKDR	0.32
t_{su}	Set Up Time, EN,IPT to CKDR	0.65
t_{su}	Set Up Time, TDI to CKDR	0.13
t_h	Hold Time, CKDR to DO,SHDR	0.15
t_h	Hold Time, CKDR to EN	0.10
t_h	Hold Time, CKDR to IPT	0.00
t_h	Hold Time, CKDR to TDI	0.31
t_w	Pulse Width, CKDR(L)	0.42
t_w	Pulse Width, CKDR(H)	0.78
t_w	Pulse Width, UDDR(H)	0.75
	BN16TS2J	
t_{su}	Set Up Time, DO to CKDR	0.33
t_{su}	Set Up Time, EN,IPT to CKDR	0.65
t_{su}	Set Up Time, SHDR to CKDR	0.31
t_{su}	Set Up Time, TDI to CKDR	0.13
t_h	Hold Time, CKDR to DO,SHDR	0.15
t_h	Hold Time, CKDR to EN	0.08
t_h	Hold Time, CKDR to IPT	0.00
t_h	Hold Time, CKDR to TDI	0.31
t_w	Pulse Width, CKDR(L)	0.42
t_w	Pulse Width, CKDR(H)	0.78
t_w	Pulse Width, UDDR(H)	0.75

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NOTE:
For Functional Diagram see page 7-88

Section 7.3.3 Input Macros -JTAG

Non - Inverting CMOS Input - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V **ICNJ**
5/3.3 V **ICXNJ**
3.3/3.3 V **ILCNJ**

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

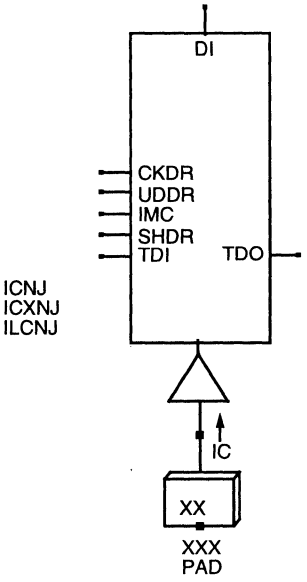
MACRO	OUTPUTS/INPUTS
All	DI,TDO / PAD,IC,CKDR,UDDR,IMC, SHDR,TDI

MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF IMC,SHDR,UDDR: 0.10pF PAD: 5.06pF

FUNCTION TABLE

JTAG	
PAD	DI
L	L
H	H

JTAG
For JTAG Truth Table Information, See Table 7-3 "JTAG Logic Truth Tables - Inputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
ICNJ					
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, IMC to DI	0.76	0.78	0.84	0.21
t_{PHL}		0.51	0.52	0.56	0.14
t_{PLH}	Propagation Delay, PAD to DI	0.47	0.48	0.52	0.12
t_{PHL}		0.53	0.55	0.60	0.18
t_{PLH}	Propagation Delay, TDO to DI	0.76	0.78	0.82	0.13
t_{PHL}		0.85	0.87	0.93	0.21
t_{PLH}	Propagation Delay, UDDR to DI	0.88	0.89	0.93	0.13
t_{PHL}		1.02	1.04	1.11	0.21
t_r	Output Rise Time, DI	0.20	0.23	0.30	0.25
t_f	Output Fall Time, DI	0.22	0.24	0.31	0.23
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		ICXNJ				ILCNJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, IMC to DI	1.07	1.10	1.19	0.31	1.07	1.10	1.19	0.31
t_{PHL}		0.70	0.72	0.78	0.19	0.70	0.72	0.78	0.19
t_{PLH}	Propagation Delay, PAD to DI	0.41	0.42	0.48	0.17	0.63	0.65	0.70	0.17
t_{PHL}		0.86	0.88	0.96	0.25	0.75	0.77	0.85	0.26
t_{PLH}	Propagation Delay, TDO to DI	1.14	1.16	1.21	0.19	1.14	1.16	1.21	0.19
t_{PHL}		1.27	1.30	1.39	0.31	1.27	1.30	1.39	0.31
t_{PLH}	Propagation Delay, UDDR to DI	1.21	1.23	1.28	0.20	1.21	1.23	1.28	0.20
t_{PHL}		1.48	1.51	1.60	0.31	1.48	1.51	1.60	0.31
t_r	Output Rise Time, DI	0.23	0.27	0.38	0.36	0.25	0.29	0.39	0.34
t_f	Output Fall Time, DI	0.29	0.32	0.40	0.28	0.29	0.32	0.40	0.28
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	1.04	1.04	1.04	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

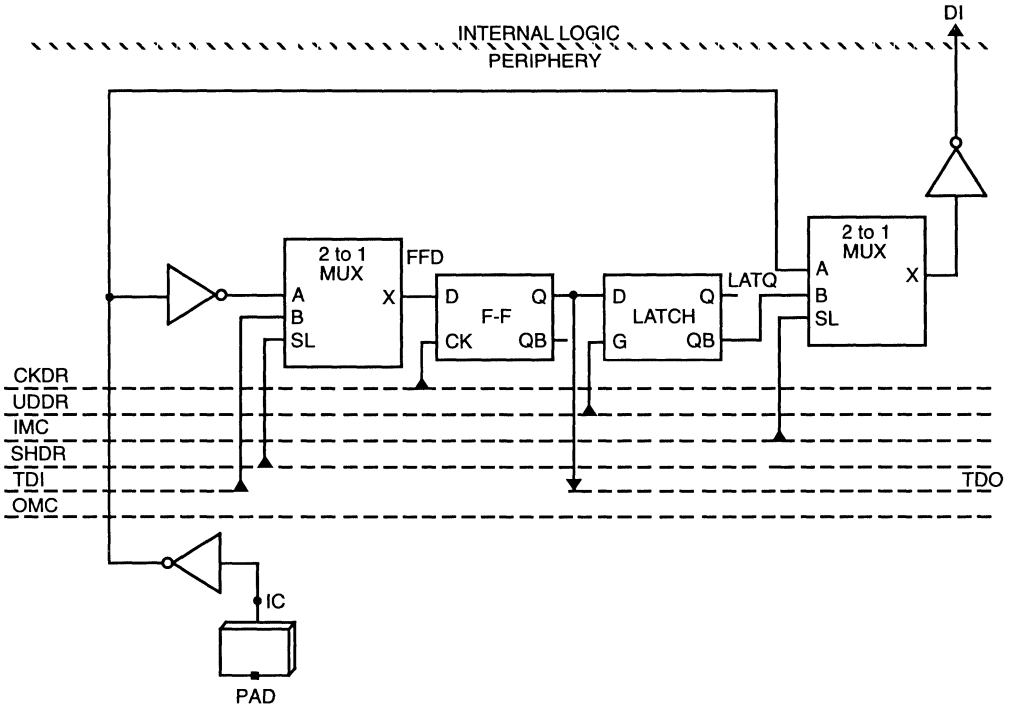
Sym	Parameter	5/5 V
		Minimum Requirement
	ICNJ	
t_{su}	Set Up Time, PAD to CKDR	0.75
t_{su}	Set Up Time, SHDR to CKDR	0.31
t_{su}	Set Up Time, TDI to CKDR	0.13
t_h	Hold Time, CKDR to PAD	-0.10
t_h	Hold Time, CKDR to SHDR	0.16
t_h	Hold Time, CKDR to TDI	0.31
t_w	Pulse Width, CKDR(L)	0.45
t_w	Pulse Width, CKDR(H)	0.80
t_w	Pulse Width, UDDR(H)	0.71

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/3.3 V	3.3/3.3V
		Minimum Requirement	Minimum Requirement
		ICXNJ	ILCNJ
t_{su}	Set Up Time, PAD to CKDR	1.13	1.09
t_{su}	Set Up Time, SHDR to CKDR	0.49	0.49
t_{su}	Set Up Time, TDI to CKDR	0.26	0.26
t_h	Hold Time, CKDR to PAD	0.05	-0.14
t_h	Hold Time, CKDR to SHDR	0.23	0.23
t_h	Hold Time, CKDR to TDI	0.41	0.41
t_w	Pulse Width, CKDR(L)	0.71	0.71
t_w	Pulse Width, CKDR(H)	1.20	1.20
t_w	Pulse Width, UDDR(H)	0.08	0.08

FUNCTIONAL DIAGRAM: IxNJ



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Non - Inverting CMOS Schmitt Trigger Input - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
5/3.3 V
3.3/3.3 V

ISNJ
ISXNJ
ILSNJ

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

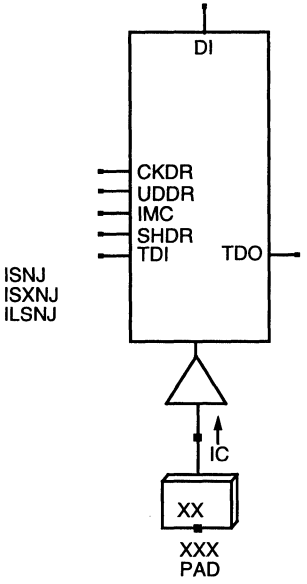
MACRO	OUTPUTS/INPUTS
All	DI,TDO / PAD,IC,CKDR,UDDR,IMC, SHDR,TDI

MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF IMC,SHDR,UDDR: 0.10pF PAD: 5.08pF

FUNCTION TABLE

JTAG	
PAD	DI
L	L
H	H

JTAG
For JTAG Truth Table Information, See Table 7-3 "JTAG Logic Truth Tables - Inputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
ISNJ					
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, IMC to DI	0.68	0.70	0.77	0.22
t_{PHL}		0.51	0.53	0.57	0.14
t_{PLH}	Propagation Delay, PAD to DI	0.66	0.68	0.72	0.13
t_{PHL}		0.99	1.01	1.08	0.22
t_{PLH}	Propagation Delay, TDO to DI	0.76	0.78	0.82	0.13
t_{PHL}		0.85	0.87	0.93	0.21
t_{PLH}	Propagation Delay, UDDR to DI	0.88	0.89	0.93	0.13
t_{PHL}		1.02	1.04	1.11	0.21
t_r	Output Rise Time, DI	0.23	0.25	0.33	0.25
t_f	Output Fall Time, DI	0.40	0.42	0.49	0.22
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		ISXNJ				ILSNJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, IMC to DI	1.02	1.05	1.14	0.31	1.02	1.05	1.14	0.31
t_{PHL}		0.66	0.68	0.74	0.19	0.66	0.68	0.74	0.19
t_{PLH}	Propagation Delay, PAD to DI	0.59	0.60	0.66	0.18	0.86	0.88	0.94	0.19
t_{PHL}		1.48	1.51	1.60	0.31	1.37	1.40	1.50	0.31
t_{PLH}	Propagation Delay, TDO to DI	1.14	1.16	1.21	0.19	1.14	1.16	1.21	0.19
t_{PHL}		1.27	1.30	1.39	0.31	1.27	1.30	1.39	0.31
t_{PLH}	Propagation Delay, UDDR to DI	1.23	1.25	1.31	0.19	1.23	1.25	1.31	0.19
t_{PHL}		1.48	1.51	1.60	0.31	1.48	1.51	1.60	0.31
t_r	Output Rise Time, DI	0.24	0.28	0.39	0.36	0.24	0.27	0.38	0.36
t_f	Output Fall Time, DI	0.46	0.49	0.59	0.31	0.46	0.49	0.59	0.31
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V
		Minimum Requirement
	ISNJ	
t_{su}	Set Up Time, PAD to CKDR	0.75
t_{su}	Set Up Time, SHDR to CKDR	0.31
t_{su}	Set Up Time, TDI to CKDR	0.13
t_h	Hold Time, CKDR to PAD	-0.10
t_h	Hold Time, CKDR to SHDR	0.16
t_h	Hold Time, CKDR to TDI	0.31
t_w	Pulse Width, CKDR(L)	0.45
t_w	Pulse Width, CKDR(H)	0.80
t_w	Pulse Width, UDDR(H)	0.71

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/3.3 V	3.3/3.3V
		Minimum Requirement	Minimum Requirement
		ISXNJ	ILSNJ
t_{su}	Set Up Time, PAD to CKDR	1.70	1.72
t_{su}	Set Up Time, SHDR to CKDR	0.49	0.49
t_{su}	Set Up Time, TDI to CKDR	0.26	0.26
t_h	Hold Time, CKDR to PAD	-0.34	-0.63
t_h	Hold Time, CKDR to SHDR	0.23	0.23
t_h	Hold Time, CKDR to TDI	0.41	0.41
t_w	Pulse Width, CKDR(L)	0.71	0.71
t_w	Pulse Width, CKDR(H)	1.20	1.20
t_w	Pulse Width, UDDR(H)	0.08	0.08

NOTE:

For Functional Diagram see page 7-107

Non-Inverting TTL Input Input - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V **ITNJ**
3.3/5 V **ILTXNJ**

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

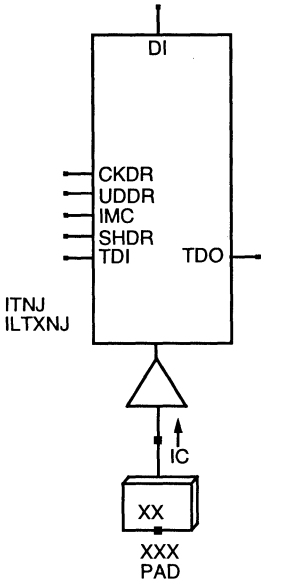
MACRO	OUTPUTS/INPUTS
All	DI,TDO / PAD,IC,CKDR,UDDR,IMC, SHDR,TDI

MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF IMC,SHDR,UDDR: 0.10pF PAD: 5.05pF

FUNCTION TABLE

JTAG	
PAD	DI
L	L
H	H

JTAG
For JTAG Truth Table Information, See Table 7-3 "JTAG Logic Truth Tables - Inputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		ITNJ				ILTXNJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, IMC to DI	0.68	0.70	0.77	0.22	0.68	0.70	0.77	0.22
t_{PHL}		0.51	0.53	0.57	0.14	0.51	0.53	0.57	0.14
t_{PLH}	Propagation Delay, PAD to DI	0.48	0.49	0.52	0.12	0.48	0.49	0.52	0.12
t_{PHL}		0.79	0.81	0.87	0.22	0.79	0.81	0.87	0.22
t_{PLH}	Propagation Delay, TDO to DI	0.76	0.78	0.82	0.13	0.76	0.78	0.82	0.13
t_{PHL}		0.85	0.87	0.93	0.21	0.85	0.87	0.93	0.21
t_{PLH}	Propagation Delay, UDDR to DI	0.88	0.89	0.93	0.13	0.88	0.89	0.93	0.13
t_{PHL}		1.02	1.04	1.11	0.21	1.02	1.04	1.11	0.21
t_r	Output Rise Time, DI	0.15	0.18	0.25	0.25	0.15	0.18	0.25	0.25
t_f	Output Fall Time, DI	0.39	0.41	0.48	0.23	0.39	0.41	0.48	0.23
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V	3.3/5 V
		Minimum Requirement	Minimum Requirement
		ITNJ	ILTXNJ
t_{su}	Set Up Time, PAD to CKDR	1.27	1.24
t_{su}	Set Up Time, SHDR to CKDR	0.31	0.31
t_{su}	Set Up Time, TDI to CKDR	0.13	0.13
t_h	Hold Time, CKDR to PAD	0.14	-0.02
t_h	Hold Time, CKDR to SHDR	0.14	0.16
t_h	Hold Time, CKDR to TDI	0.31	0.31
t_w	Pulse Width, CKDR(L)	0.45	0.45
t_w	Pulse Width, CKDR(H)	0.80	0.80
t_w	Pulse Width, UDDR(H)	0.71	0.71

NOTE:
For Functional Diagram see page 7-107

Non-Inverting TTL Schmitt Trigger Input - JTAG (5 V System/Core Voltage)

5/5 V

ITSNJ

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

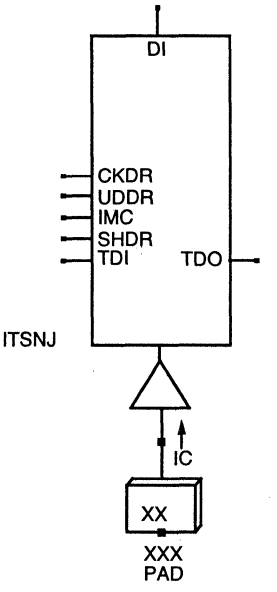
MACRO	OUTPUTS/INPUTS
All	DI,TDO / PAD,IC,CKDR,UDDR,IMC, SHDR,TDI

MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF IMC,SHDR,UDDR: 0.10pF PAD: 5.05pF

FUNCTION TABLE

JTAG	
PAD	DI
L	L
H	H

JTAG
For JTAG Truth Table Information, See Table 7-3 "JTAG Logic Truth Tables - Inputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		ITSNJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.70	0.70	0.70	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, IMC to DI	0.63	0.65	0.72	0.22
t_{PHL}		0.48	0.50	0.54	0.14
t_{PLH}	Propagation Delay, PAD to DI	0.76	0.77	0.81	0.13
t_{PHL}		1.11	1.14	1.20	0.22
t_{PLH}	Propagation Delay, TDO to DI	0.76	0.78	0.82	0.13
t_{PHL}		0.85	0.87	0.93	0.21
t_{PLH}	Propagation Delay, UDDR to DI	0.88	0.89	0.93	0.13
t_{PHL}		1.02	1.04	1.11	0.21
t_r	Output Rise Time, DI	0.22	0.24	0.32	0.25
t_f	Output Fall Time, DI	0.43	0.45	0.52	0.23
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V Minimum Requirement
	ITSNJ	
t_{su}	Set Up Time, PAD to CKDR	1.57
t_{su}	Set Up Time, SHDR to CKDR	0.31
t_{su}	Set Up Time, TDI to CKDR	0.13
t_h	Hold Time, CKDR to PAD	-0.38
t_h	Hold Time, CKDR to SHDR	0.16
t_h	Hold Time, CKDR to TDI	0.31
t_w	Pulse Width, CKDR(L)	0.45
t_w	Pulse Width, CKDR(H)	0.80
t_w	Pulse Width, UDDR(H)	0.71

NOTE:
For Functional Diagram see page 7-107

Non - Inverting CMOS Clock Buffer Input- JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
5/3.3 V
3.3/3.3 V

ICNCKHJ
ICXNCKHJ
ILCNCKHJ

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

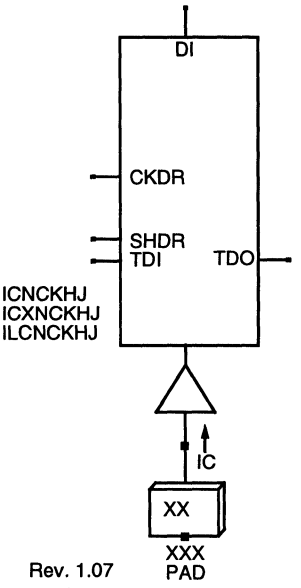
MACRO	OUTPUTS/INPUTS
All	DI,TDO / PAD,IC,CKDR,SHDR,TDI

MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF PAD: 5.16pF SHDR: 0.09pF

FUNCTION TABLE

JTAG	
PAD	DI
L	L
H	H

JTAG
For JTAG Truth Table Information, See Table 7-5 "JTAG Logic Truth Table - Clock/ "Sample Only" Inputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
ICNCKHJ					
t_{PLH}	Propagation Delay, CKDR to TDO	0.68	0.68	0.68	0.00
t_{PHL}		0.71	0.71	0.71	0.00
t_{PLH}	Propagation Delay, PAD to DI	0.44	0.45	0.46	0.04
t_{PHL}		0.38	0.39	0.41	0.07
t_r	Output Rise Time, DI	0.08	0.09	0.12	0.10
t_f	Output Fall Time, DI	0.06	0.07	0.11	0.11
t_r	Output Rise Time, TDO	0.58	0.58	0.58	0.00
t_f	Output Fall Time, TDO	0.39	0.39	0.39	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		ICXNCKHJ				ILCNCKHJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PHL}		0.98	0.98	0.98	0.00	0.98	0.98	0.98	0.00
t_{PLH}	Propagation Delay, PAD to DI	0.32	0.33	0.34	0.05	0.57	0.58	0.59	0.05
t_{PHL}		0.62	0.63	0.65	0.08	0.50	0.51	0.54	0.08
t_r	Output Rise Time, DI	0.10	0.11	0.16	0.14	0.11	0.12	0.17	0.14
t_f	Output Fall Time, DI	0.08	0.10	0.14	0.14	0.08	0.10	0.14	0.14
t_r	Output Rise Time, TDO	0.79	0.79	0.79	0.00	0.79	0.79	0.79	0.00
t_f	Output Fall Time, TDO	0.49	0.49	0.49	0.00	0.49	0.49	0.49	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

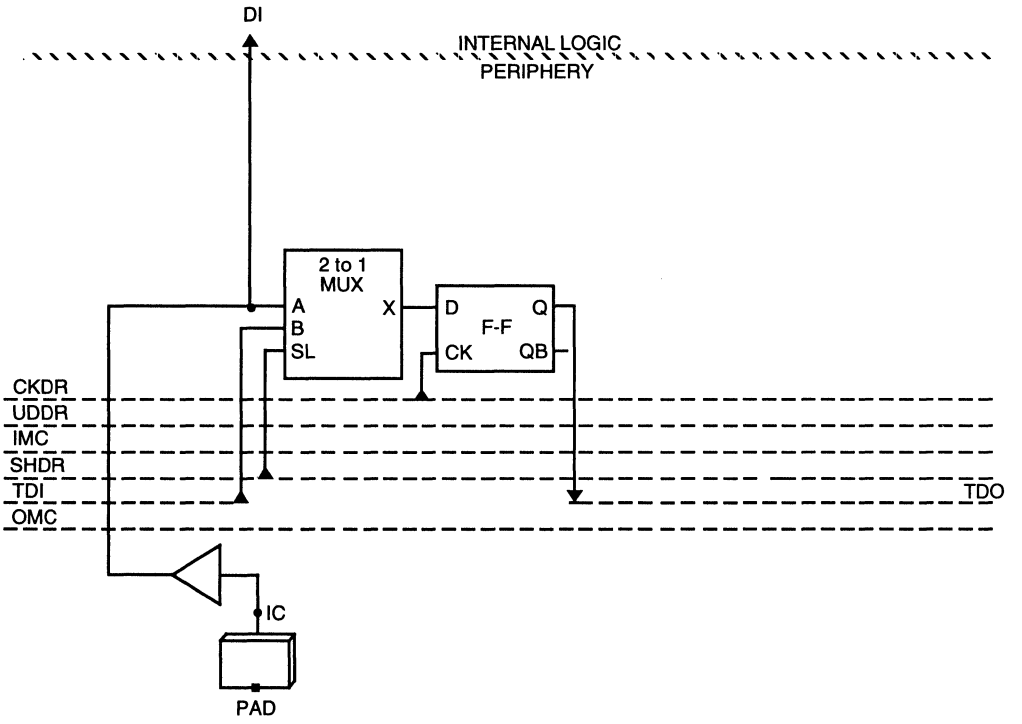
Sym	Parameter	5/5 V
		Minimum Requirement
	ICNCKHJ	
t_{su}	Set Up Time, DI to CKDR	0.56
t_{su}	Set Up Time, SHDR to CKDR	0.25
t_{su}	Set Up Time, TDI to CKDR	0.13
t_h	Hold Time, CKDR to DI	-0.05
t_h	Hold Time, CKDR to SHDR	0.19
t_h	Hold Time, CKDR to TDI	0.31
t_w	Pulse Width, CKDR(L)	0.45
t_w	Pulse Width, CKDR(H)	0.65

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/3.3 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		ICXNCKHJ	ILCNCKHJ
t_{su}	Set Up Time, DI to CKDR	0.56	0.82
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.43
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26
t_h	Hold Time, CKDR to DI	-0.05	-0.04
t_h	Hold Time, CKDR to SHDR	0.19	0.25
t_h	Hold Time, CKDR to TDI	0.31	0.41
t_w	Pulse Width, CKDR(L)	0.45	0.71
t_w	Pulse Width, CKDR(H)	0.65	0.98

FUNCTIONAL DIAGRAM: IxNCKHJ



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Non - Inverting CMOS Schmitt Trigger Clock Buffer Input - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
5/3.3 V
3.3/3.3 V

ISNCKHJ
ISXNCKHJ
ILSNCKHJ

MACRO	SECTIONS USED
All	1/0

Rev. 1.07

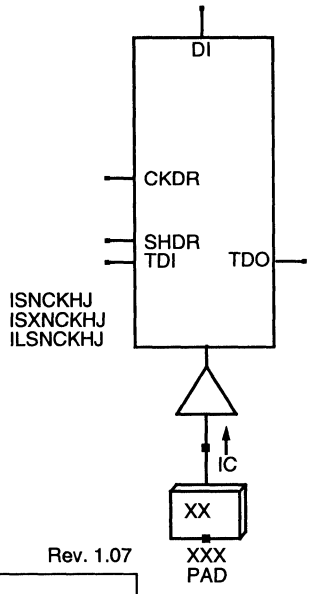
MACRO	OUTPUTS/INPUTS
All	DI,TDO / PAD,IC,CKDR,SHDR,TDI

MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF PAD: 5.20pF SHDR: 0.09pF

FUNCTION TABLE

JTAG	
PAD	DI
L	L
H	H

JTAG
For JTAG Truth Table Information, See Table 7-5 "JTAG Logic Truth Table - Clock/"Sample Only" Inputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)
ISNCKHJ					
t_{PLH}	Propagation Delay, CKDR to TDO	0.68	0.68	0.68	0.00
t_{PHL}		0.71	0.71	0.71	0.00
t_{PLH}	Propagation Delay, PAD to DI	0.61	0.61	0.62	0.04
t_{PHL}		1.01	1.02	1.04	0.07
t_r	Output Rise Time, DI	0.08	0.09	0.12	0.10
t_f	Output Fall Time, DI	0.14	0.15	0.18	0.11
t_r	Output Rise Time, TDO	0.58	0.58	0.58	0.00
t_f	Output Fall Time, TDO	0.39	0.39	0.39	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		ISXNCKHJ				ILSNCKHJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PHL}		0.98	0.98	0.98	0.00	0.98	0.98	0.98	0.00
t_{PLH}	Propagation Delay, PAD to DI	0.46	0.47	0.48	0.05	0.80	0.80	0.82	0.05
t_{PHL}		1.53	1.53	1.56	0.08	1.43	1.44	1.46	0.08
t_r	Output Rise Time, DI	0.09	0.11	0.15	0.14	0.10	0.12	0.16	0.14
t_f	Output Fall Time, DI	0.19	0.20	0.24	0.14	0.19	0.20	0.24	0.14
t_r	Output Rise Time, TDO	0.79	0.79	0.79	0.00	0.79	0.79	0.79	0.00
t_f	Output Fall Time, TDO	0.49	0.49	0.49	0.00	0.49	0.49	0.49	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V
		Minimum Requirement
	ISNCKHJ	
t_{su}	Set Up Time, DI to CKDR	1.09
t_{su}	Set Up Time, SHDR to CKDR	0.25
t_{su}	Set Up Time, TDI to CKDR	0.13
t_h	Hold Time, CKDR to DI	-0.27
t_h	Hold Time, CKDR to SHDR	0.19
t_h	Hold Time, CKDR to TDI	0.31
t_w	Pulse Width, CKDR(L)	0.45
t_w	Pulse Width, CKDR(H)	0.65

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		ISXNCKHJ	ILSNCKHJ
t_{su}	Set Up Time, DI to CKDR	1.70	1.47
t_{su}	Set Up Time, SHDR to CKDR	0.43	0.43
t_{su}	Set Up Time, TDI to CKDR	0.26	0.26
t_h	Hold Time, CKDR to DI	-0.10	-0.33
t_h	Hold Time, CKDR to SHDR	0.25	0.25
t_h	Hold Time, CKDR to TDI	0.41	0.41
t_w	Pulse Width, CKDR(L)	0.71	0.71
t_w	Pulse Width, CKDR(H)	0.98	0.98

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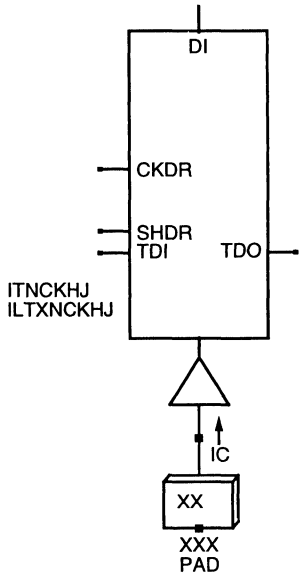
NOTE:
For Functional Diagram see page 7-116

Non - Inverting TTL Clock Buffer Input Clock Buffer Input - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/5 V

ITNCKHJ
ILTXNCKHJ



MACRO	SECTIONS USED
All	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	DI,TDO / PAD,IC,CKDR,SHDR,TDI

MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF PAD: 5.40pF SHDR: 0.09pF

FUNCTION TABLE

JTAG	
PAD	DI
L	L
H	H

JTAG
For JTAG Truth Table Information, SeeTable 7-5 "JTAG Logic Truth Table - Clock/"Sample Only" Inputs" on page 7-183 in this Manual.

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	55 V				3.3/5 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		ITNCKHJ				ILTXNCKHJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.68	0.68	0.68	0.00	0.68	0.68	0.68	0.00
t_{PHL}		0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PLH}	Propagation Delay, PAD to DI	0.37	0.37	0.38	0.04	0.40	0.40	0.41	0.04
t_{PHL}		0.47	0.47	0.50	0.07	0.49	0.50	0.52	0.07
t_r	Output Rise Time, DI	0.05	0.06	0.09	0.10	0.05	0.06	0.10	0.10
t_f	Output Fall Time, DI	0.07	0.08	0.11	0.11	0.07	0.08	0.11	0.11
t_r	Output Rise Time, TDO	0.58	0.58	0.58	0.00	0.58	0.58	0.58	0.00
t_f	Output Fall Time, TDO	0.39	0.39	0.39	0.00	0.39	0.39	0.39	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/5 V
		Minimum Requirement	Minimum Requirement
		ITNCKHJ	ILTXNCKHJ
t_{su}	Set Up Time, DI to CKDR	0.47	0.51
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.25
t_{su}	Set Up Time, TDI to CKDR	0.13	0.13
t_h	Hold Time, CKDR to DI	0.10	0.06
t_h	Hold Time, CKDR to SHDR	0.19	0.19
t_h	Hold Time, CKDR to TDI	0.31	0.31
t_w	Pulse Width, CKDR(L)	0.45	0.45
t_w	Pulse Width, CKDR(H)	0.65	0.65

NOTE:
For Functional Diagram see page 7-116

Non - Inverting TTL Schmitt Trigger Clock Buffer Input - JTAG (5 V System/Core Voltage)

5/5 V

ITSNCKHJ

MACRO	SECTIONS USED
ITSNCKHJ	1/0

Rev. 1.07

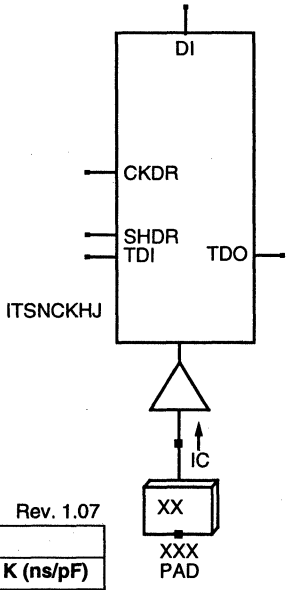
MACRO	OUTPUTS/INPUTS
ITSNCKHJ	DI,TDO / PAD,IC,CKDR,SHDR,TDI

MACRO	INPUT CAP.
ITSNCKHJ	CKDR,TDI: 0.04pF PAD: 5.27pF SHDR: 0.09pF

FUNCTION TABLE

JTAG	
PAD	DI
L	L
H	H

JTAG
For JTAG Truth Table Information, SeeTable 7-5 "JTAG Logic Truth Table - Clock/"Sample Only" Inputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	55 V			
		FO=0	FO=2	FO=8	K (ns/pF)
		ITSNCKHJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.68	0.68	0.68	0.00
t_{PHL}		0.71	0.71	0.71	0.00
t_{PLH}	Propagation Delay, PAD to DI	0.74	0.74	0.75	0.04
t_{PHL}		1.22	1.23	1.25	0.07
t_r	Output Rise Time, DI	0.07	0.08	0.12	0.10
t_f	Output Fall Time, DI	0.17	0.18	0.22	0.11
t_r	Output Rise Time, TDO	0.58	0.58	0.58	0.00
t_f	Output Fall Time, TDO	0.39	0.39	0.39	0.00

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V
		Minimum Requirement
		ITSNCKHJ
t_{su}	Set Up Time, DI to CKDR	1.15
t_{su}	Set Up Time, SHDR to CKDR	0.25
t_{su}	Set Up Time, TDI to CKDR	0.13
t_h	Hold Time, CKDR to DI	-0.24
t_h	Hold Time, CKDR to SHDR	0.19
t_h	Hold Time, CKDR to TDI	0.31
t_w	Pulse Width, CKDR(L)	0.45
t_w	Pulse Width, CKDR(H)	0.65

NOTE:
For Functional Diagram see page 7-116

Section 7.3.4 Output Buffers -JTAG

Non - Inverting Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
5/3.3 V
3.3/5 V
3.3/3.3 V

ON4J
ONX4J
ONLX4J
ONL4J

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD,TDO / DO,CKDR,UDDR,SHDR,TDI,OMC

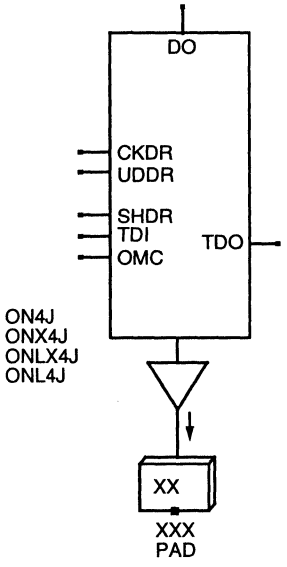
MACRO	INPUT CAP.
ON4J ONL4J	CKDR,TDI: 0.04pF DO: 0.40pF OMC,SHDR: 0.10pF UDDR: 0.08pF
ONX4J ONLX4J	CKDR,TDI: 0.04pF DO: 0.26pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
All	PAD: 4.96pF

FUNCTION TABLE

JTAG	
DO	PAD
L	L
H	H

JTAG
For JTAG Truth Table Information, See Table 7-4 "JTAG Logic Truth Tables - Outputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON4J				ONLX4J			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.78	3.03	5.28	0.05	0.97	3.22	5.47	0.05
t_{PHL}		0.75	2.70	4.65	0.04	0.80	2.85	4.90	0.04
t_{PLH}	Propagation Delay, OMC to PAD	1.02	3.27	5.52	0.05	1.12	3.37	5.62	0.05
t_{PHL}		0.98	2.93	4.88	0.04	0.98	3.03	5.08	0.04
t_{PLH}	Propagation Delay, TDO to PAD	1.25	3.50	5.75	0.05	1.37	3.62	5.87	0.05
t_{PHL}		1.16	3.11	5.06	0.04	1.16	3.21	5.26	0.04
t_{PLH}	Propagation Delay, UDDR to PAD	1.38	3.63	5.88	0.05	1.50	3.75	6.00	0.05
t_{PHL}		1.34	3.29	5.24	0.04	1.33	3.38	5.43	0.04
t_r	Output Rise Time, PAD	0.39	5.54	10.69	0.10	0.38	5.53	10.68	0.10
t_f	Output Fall Time, PAD	0.37	4.17	7.97	0.08	0.28	4.93	9.58	0.09
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX4J				ONL4J			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.26	3.46	5.66	0.04	1.04	4.24	7.44	0.06
t_{PHL}		1.36	4.31	7.26	0.06	0.98	3.33	5.68	0.05
t_{PLH}	Propagation Delay, OMC to PAD	1.52	3.72	5.92	0.04	1.40	4.60	7.80	0.06
t_{PHL}		1.59	4.54	7.49	0.06	1.28	3.63	5.98	0.05
t_{PLH}	Propagation Delay, TDO to PAD	1.96	4.16	6.36	0.04	1.82	5.02	8.22	0.06
t_{PHL}		1.90	4.85	7.80	0.06	1.60	3.95	6.30	0.05
t_{PLH}	Propagation Delay, UDDR to PAD	2.04	4.24	6.44	0.04	1.91	5.11	8.31	0.06
t_{PHL}		2.13	5.08	8.03	0.06	1.82	4.17	6.52	0.05
t_r	Output Rise Time, PAD	0.24	5.24	10.24	0.10	0.48	7.63	14.78	0.14
t_f	Output Fall Time, PAD	0.33	6.08	11.83	0.11	0.44	5.09	9.74	0.09
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON4J				ONLX4J			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.70	1.85	3.00	0.02	0.94	2.69	4.44	0.04
t_{PHL}		0.84	3.89	6.94	0.06	0.83	3.43	6.03	0.05
t_{PLH}	Propagation Delay, OMC to PAD	0.94	2.09	3.24	0.02	1.08	2.83	4.58	0.04
t_{PHL}		1.06	4.11	7.16	0.06	1.01	3.61	6.21	0.05
t_{PLH}	Propagation Delay, TDO to PAD	1.17	2.32	3.47	0.02	1.34	3.09	4.84	0.04
t_{PHL}		1.24	4.29	7.34	0.06	1.19	3.79	6.39	0.05
t_{PLH}	Propagation Delay, UDDR to PAD	1.30	2.45	3.60	0.02	1.47	3.22	4.97	0.04
t_{PHL}		1.42	4.47	7.52	0.06	1.36	3.96	6.56	0.05
t_r	Output Rise Time, PAD	0.39	5.54	10.69	0.10	0.38	5.53	10.68	0.10
t_f	Output Fall Time, PAD	0.37	4.17	7.97	0.08	0.28	4.93	9.58	0.09
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX4J				ONL4J			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.21	2.31	3.41	0.02	1.00	3.50	6.00	0.05
t_{PHL}		1.45	6.00	10.55	0.09	1.02	3.92	6.82	0.06
t_{PLH}	Propagation Delay, OMC to PAD	1.46	2.56	3.66	0.02	1.35	3.85	6.35	0.05
t_{PHL}		1.69	6.24	10.79	0.09	1.32	4.22	7.12	0.06
t_{PLH}	Propagation Delay, TDO to PAD	1.90	3.00	4.10	0.02	1.78	4.28	6.78	0.05
t_{PHL}		1.99	6.54	11.09	0.09	1.64	4.54	7.44	0.06
t_{PLH}	Propagation Delay, UDDR to PAD	1.99	3.09	4.19	0.02	1.87	4.37	6.87	0.05
t_{PHL}		2.22	6.77	11.32	0.09	1.86	4.76	7.66	0.06
t_r	Output Rise Time, PAD	0.24	5.24	10.24	0.10	0.48	7.63	14.78	0.14
t_f	Output Fall Time, PAD	0.33	6.08	11.83	0.11	0.44	5.09	9.74	0.09
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

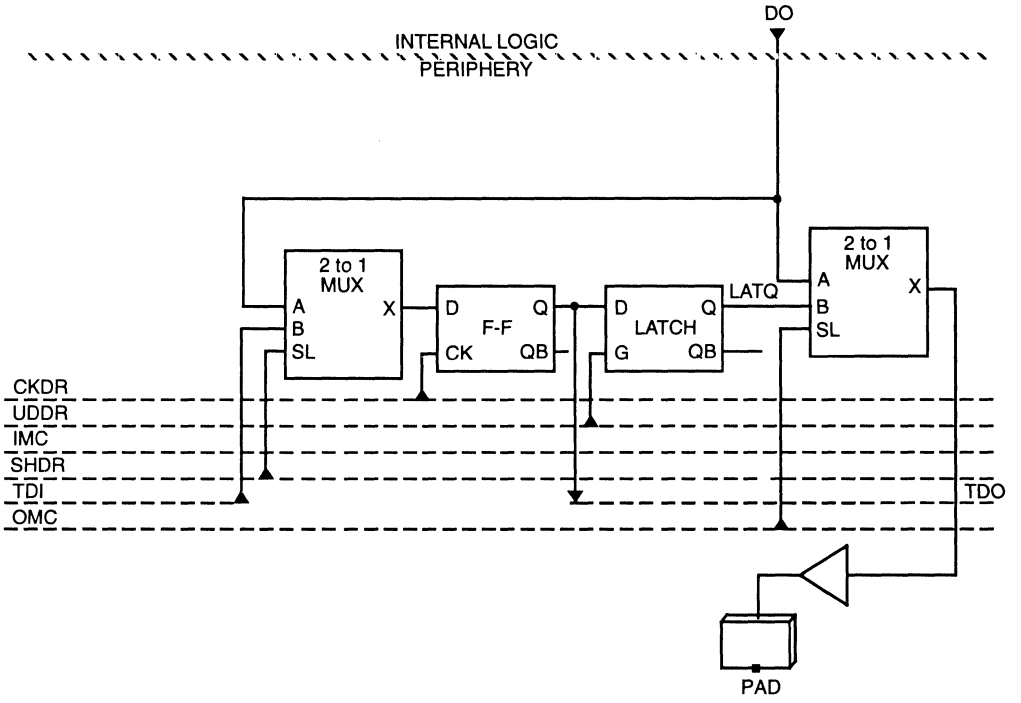
Sym	Parameter	5/5 V	3.3/5 V
		Minimum Requirement	Minimum Requirement
		ON4J	ONLX4J
t_{su}	Set Up Time, DO to CKDR	0.22	0.18
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.25
t_{su}	Set Up Time, TDI to CKDR	0.14	0.14
t_h	Hold Time, CKDR to DO	0.25	0.26
t_h	Hold Time, CKDR to SHDR	0.19	0.19
t_h	Hold Time, CKDR to TDI	0.32	0.32
t_w	Pulse Width, CKDR(L)	0.40	0.40
t_w	Pulse Width, CKDR(H)	0.78	0.78
t_w	Pulse Width, UDDR(H)	0.47	0.47

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		ONX4J	ONL4J
t_{su}	Set Up Time, DO to CKDR	0.36	0.38
t_{su}	Set Up Time, SHDR to CKDR	0.43	0.43
t_{su}	Set Up Time, TDI to CKDR	0.28	0.28
t_h	Hold Time, CKDR to DO	0.36	0.38
t_h	Hold Time, CKDR to SHDR	0.25	0.25
t_h	Hold Time, CKDR to TDI	0.42	0.42
t_w	Pulse Width, CKDR(L)	0.67	0.67
t_w	Pulse Width, CKDR(H)	1.18	1.18
t_w	Pulse Width, UDDR(H)	0.64	0.64

FUNCTIONAL DIAGRAM: ONXJ



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Non - Inverting Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
5/3.3 V
3.3/5 V
3.3/3.3 V

ON8J
ONX8J
ONLX8J
ONL8J

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD,TDO / DO,CKDR,UDDR,SHDR,TDI,OMC

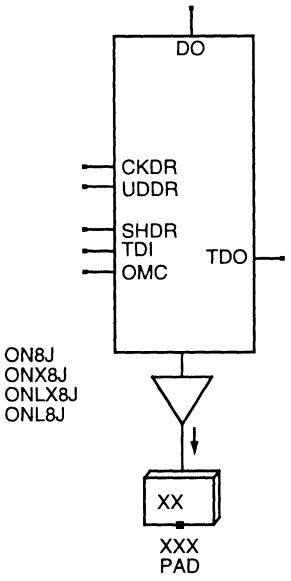
MACRO	INPUT CAP.
ON8J ONX8J ONL8J	CKDR,TDI: 0.04pF DO: 0.26pF OMC,SHDR: 0.10pF UDDR: 0.08pF
ONLX8J	CKDR,TDI: 0.04pF DO: 0.31pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
All	PAD: 5.10pF

FUNCTION TABLE

JTAG	
DO	PAD
L	L
H	H

JTAG
For JTAG Truth Table Information, See Table 7-4 "JTAG Logic Truth Tables - Outputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON8J				ONLX8J			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.90	2.20	3.50	0.03	1.10	2.45	3.80	0.03
t_{PHL}		1.04	2.29	3.54	0.03	1.14	2.24	3.34	0.02
t_{PLH}	Propagation Delay, OMC to PAD	1.04	2.34	3.64	0.03	1.29	2.64	3.99	0.03
t_{PHL}		1.22	2.47	3.72	0.03	1.33	2.43	3.53	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.30	2.60	3.90	0.03	1.55	2.90	4.25	0.03
t_{PHL}		1.40	2.65	3.90	0.03	1.50	2.60	3.70	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	1.43	2.73	4.03	0.03	1.68	3.03	4.38	0.03
t_{PHL}		1.57	2.82	4.07	0.03	1.68	2.78	3.88	0.02
t_r	Output Rise Time, PAD	0.29	3.24	6.19	0.06	0.58	3.54	6.49	0.06
t_f	Output Fall Time, PAD	0.49	2.74	4.99	0.05	0.55	2.85	5.15	0.05
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX8J				ONL8J			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.77	3.12	4.47	0.03	1.23	3.08	4.93	0.04
t_{PHL}		1.76	3.26	4.76	0.03	1.38	2.88	4.38	0.03
t_{PLH}	Propagation Delay, OMC to PAD	2.00	3.35	4.70	0.03	1.48	3.33	5.18	0.04
t_{PHL}		2.02	3.52	5.02	0.03	1.63	3.13	4.63	0.03
t_{PLH}	Propagation Delay, TDO to PAD	2.46	3.81	5.16	0.03	1.92	3.77	5.62	0.04
t_{PHL}		2.31	3.81	5.31	0.03	1.94	3.44	4.94	0.03
t_{PLH}	Propagation Delay, UDDR to PAD	2.53	3.88	5.23	0.03	2.00	3.85	5.70	0.04
t_{PHL}		2.52	4.02	5.52	0.03	2.15	3.65	5.15	0.03
t_r	Output Rise Time, PAD	0.66	3.56	6.46	0.06	0.35	4.40	8.45	0.08
t_f	Output Fall Time, PAD	0.57	3.37	6.17	0.06	0.59	3.34	6.09	0.05
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON8J				ONLX8J			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.83	1.48	2.13	0.01	1.04	2.09	3.14	0.02
t_{PHL}		1.15	3.05	4.95	0.04	1.19	2.59	3.99	0.03
t_{PLH}	Propagation Delay, OMC to PAD	0.97	1.62	2.27	0.01	1.23	2.28	3.33	0.02
t_{PHL}		1.32	3.22	5.12	0.04	1.38	2.78	4.18	0.03
t_{PLH}	Propagation Delay, TDO to PAD	1.23	1.88	2.53	0.01	1.48	2.53	3.58	0.02
t_{PHL}		1.50	3.40	5.30	0.04	1.55	2.95	4.35	0.03
t_{PLH}	Propagation Delay, UDDR to PAD	1.36	2.01	2.66	0.01	1.62	2.67	3.72	0.02
t_{PHL}		1.67	3.57	5.47	0.04	1.73	3.13	4.53	0.03
t_r	Output Rise Time, PAD	0.29	3.24	6.19	0.06	0.58	3.54	6.49	0.06
t_f	Output Fall Time, PAD	0.49	2.74	4.99	0.05	0.55	2.85	5.15	0.05
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX8J				ONL8J			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.57	2.32	3.07	0.01	1.20	2.60	4.00	0.03
t_{PHL}		1.87	4.17	6.47	0.05	1.44	3.24	5.04	0.04
t_{PLH}	Propagation Delay, OMC to PAD	1.81	2.56	3.31	0.01	1.45	2.85	4.25	0.03
t_{PHL}		2.13	4.43	6.73	0.05	1.68	3.48	5.28	0.04
t_{PLH}	Propagation Delay, TDO to PAD	2.27	3.02	3.77	0.01	1.88	3.28	4.68	0.03
t_{PHL}		2.42	4.72	7.02	0.05	1.99	3.79	5.59	0.04
t_{PLH}	Propagation Delay, UDDR to PAD	2.34	3.09	3.84	0.01	1.97	3.37	4.77	0.03
t_{PHL}		2.64	4.94	7.24	0.05	2.21	4.01	5.81	0.04
t_r	Output Rise Time, PAD	0.66	3.56	6.46	0.06	0.35	4.40	8.45	0.08
t_f	Output Fall Time, PAD	0.57	3.37	6.17	0.06	0.59	3.34	6.09	0.05
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V	3.3/5 V
		Minimum Requirement	Minimum Requirement
		ON8J	ONLX8J
t_{su}	Set Up Time, DO to CKDR	0.18	0.18
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.25
t_{su}	Set Up Time, TDI to CKDR	0.14	0.14
t_h	Hold Time, CKDR to DO	0.26	0.26
t_h	Hold Time, CKDR to SHDR	0.19	0.19
t_h	Hold Time, CKDR to TDI	0.32	0.32
t_w	Pulse Width, CKDR(L)	0.40	0.40
t_w	Pulse Width, CKDR(H)	0.78	0.78
t_w	Pulse Width, UDDR(H)	0.47	0.47

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/3.3 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		ONX8J	ONL8J
t_{su}	Set Up Time, DO to CKDR	0.36	0.36
t_{su}	Set Up Time, SHDR to CKDR	0.43	0.43
t_{su}	Set Up Time, TDI to CKDR	0.28	0.28
t_h	Hold Time, CKDR to DO	0.36	0.37
t_h	Hold Time, CKDR to SHDR	0.25	0.25
t_h	Hold Time, CKDR to TDI	0.42	0.42
t_w	Pulse Width, CKDR(L)	0.67	0.67
t_w	Pulse Width, CKDR(H)	1.18	1.18
t_w	Pulse Width, UDDR(H)	0.64	0.64

NOTE:
For Functional Diagram see page 7-124

Non - Inverting Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/5 V
3.3/3.3 V

ON16J
ONXL16J
ONL16J

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD,TDO / DO,CKDR,UDDR,SHDR,TDI,OMC

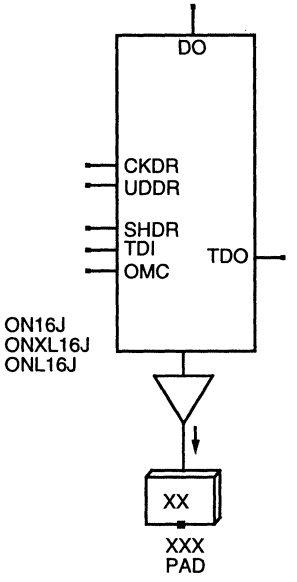
MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF DO: 0.31pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
All	PAD: 5.76pF

FUNCTION TABLE

JTAG	
DO	PAD
L	L
H	H

JTAG
For JTAG Truth Table Information, See Table 7-4 "JTAG Logic Truth Tables - Outputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON16J				ONLX16J			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.87	1.67	2.47	0.02	1.13	2.49	3.84	0.03
t_{PHL}		1.14	1.99	2.84	0.02	0.99	1.64	2.29	0.01
t_{PLH}	Propagation Delay, OMC to PAD	1.07	1.87	2.67	0.02	1.33	2.68	4.03	0.03
t_{PHL}		1.32	2.17	3.02	0.02	1.18	1.83	2.48	0.01
t_{PLH}	Propagation Delay, TDO to PAD	1.32	2.12	2.92	0.02	1.58	2.93	4.28	0.03
t_{PHL}		1.49	2.34	3.19	0.02	1.35	2.00	2.65	0.01
t_{PLH}	Propagation Delay, UDDR to PAD	1.45	2.25	3.05	0.02	1.71	3.06	4.41	0.03
t_{PHL}		1.67	2.52	3.37	0.02	1.53	2.18	2.83	0.01
t_r	Output Rise Time, PAD	0.43	2.13	3.83	0.03	0.58	3.53	6.48	0.06
t_f	Output Fall Time, PAD	0.49	1.89	3.29	0.03	0.46	1.61	2.76	0.02
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ONL16J			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.21	2.36	3.51	0.02
t_{PHL}		1.52	2.52	3.52	0.02
t_{PLH}	Propagation Delay, OMC to PAD	1.52	2.67	3.82	0.02
t_{PHL}		1.79	2.79	3.79	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.96	3.11	4.26	0.02
t_{PHL}		2.08	3.08	4.08	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	2.04	3.19	4.34	0.02
t_{PHL}		2.30	3.30	4.30	0.02
t_r	Output Rise Time, PAD	0.52	2.87	5.22	0.05
t_f	Output Fall Time, PAD	0.58	2.28	3.98	0.03
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON16J				ONLX16J			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.74	1.19	1.64	0.01	1.07	2.12	3.17	0.02
t_{PHL}		1.25	2.45	3.65	0.02	1.03	1.78	2.53	0.01
t_{PLH}	Propagation Delay, OMC to PAD	0.95	1.40	1.85	0.01	1.26	2.31	3.36	0.02
t_{PHL}		1.43	2.63	3.83	0.02	1.23	1.98	2.73	0.01
t_{PLH}	Propagation Delay, TDO to PAD	1.19	1.64	2.09	0.01	1.51	2.56	3.61	0.02
t_{PHL}		1.61	2.81	4.01	0.02	1.40	2.15	2.90	0.01
t_{PLH}	Propagation Delay, UDDR to PAD	1.33	1.78	2.23	0.01	1.65	2.70	3.75	0.02
t_{PHL}		1.78	2.98	4.18	0.02	1.57	2.32	3.07	0.01
t_r	Output Rise Time, PAD	0.43	2.13	3.83	0.03	0.58	3.53	6.48	0.06
t_f	Output Fall Time, PAD	0.49	1.89	3.29	0.03	0.46	1.61	2.76	0.02
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ONL16J			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.15	2.05	2.95	0.02
t_{PHL}		1.58	2.78	3.98	0.02
t_{PLH}	Propagation Delay, OMC to PAD	1.46	2.36	3.26	0.02
t_{PHL}		1.85	3.05	4.25	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.90	2.80	3.70	0.02
t_{PHL}		2.13	3.33	4.53	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	1.98	2.88	3.78	0.02
t_{PHL}		2.36	3.56	4.76	0.02
t_r	Output Rise Time, PAD	0.52	2.87	5.22	0.05
t_f	Output Fall Time, PAD	0.58	2.28	3.98	0.03
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/5 V
		Minimum Requirement	Minimum Requirement
		ON16J	ONLX16J
t_{su}	Set Up Time, DO to CKDR	0.19	0.18
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.25
t_{su}	Set Up Time, TDI to CKDR	0.14	0.14
t_h	Hold Time, CKDR to DO	0.25	0.26
t_h	Hold Time, CKDR to SHDR	0.19	0.19
t_h	Hold Time, CKDR to TDI	0.32	0.32
t_w	Pulse Width, CKDR(L)	0.40	0.40
t_w	Pulse Width, CKDR(H)	0.78	0.78
t_w	Pulse Width, UDDR(H)	0.47	0.47

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V
		Minimum Requirement
	ONL16J	
t_{su}	Set Up Time, DO to CKDR	0.37
t_{su}	Set Up Time, SHDR to CKDR	0.43
t_{su}	Set Up Time, TDI to CKDR	0.28
t_h	Hold Time, CKDR to DO	0.35
t_h	Hold Time, CKDR to SHDR	0.25
t_h	Hold Time, CKDR to TDI	0.42
t_w	Pulse Width, CKDR(L)	0.67
t_w	Pulse Width, CKDR(H)	1.18
t_w	Pulse Width, UDDR(H)	0.64

NOTE:
For Functional Diagram see page 7-124

Non - Inverting Output Buffers - JTAG With Slew Rate Control (S2) (5 V System/Core Voltage)

5/5 V

ON4S2J
ON8S2J
ON16S2J

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD,TDO / DO,CKDR,UDDR,SHDR,TDI,OMC

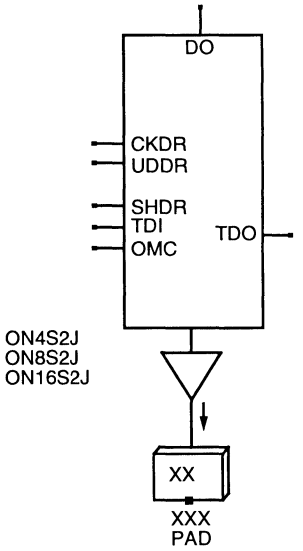
MACRO	INPUT CAP.
ON4S2J	CKDR,TDI: 0.04pF DO: 0.40pF OMC,SHDR: 0.10pF UDDR: 0.08pF
ON8S2J	CKDR,TDI: 0.04pF DO: 0.26pF OMC,SHDR: 0.10pF UDDR: 0.08pF
ON16S2J	CKDR,TDI: 0.04pF DO: 0.31pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
ON4S2J	PAD: 4.96pF
ON8S2J	PAD: 5.10pF
ON16S2J	PAD: 5.76pF

FUNCTION TABLE

JTAG	
DO	PAD
L	L
H	H

JTAG
For JTAG Truth Table Information, See Table 7-4 "JTAG Logic Truth Tables - Outputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5//5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ON4S2J			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.56	3.86	6.16	0.05
t_{PHL}		1.20	3.20	5.20	0.04
t_{PLH}	Propagation Delay, OMC to PAD	1.76	4.06	6.36	0.05
t_{PHL}		1.39	3.39	5.39	0.04
t_{PLH}	Propagation Delay, TDO to PAD	1.98	4.28	6.58	0.05
t_{PHL}		1.58	3.58	5.58	0.04
t_{PLH}	Propagation Delay, UDDR to PAD	2.11	4.41	6.71	0.05
t_{PHL}		1.75	3.75	5.75	0.04
t_r	Output Rise Time, PAD	0.71	5.81	10.91	0.10
t_f	Output Fall Time, PAD	0.55	4.35	8.15	0.08
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5//5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ON8S2J			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.57	2.97	4.37	0.03
t_{PHL}		1.32	2.62	3.92	0.03
t_{PLH}	Propagation Delay, OMC to PAD	1.70	3.10	4.50	0.03
t_{PHL}		1.49	2.79	4.09	0.03
t_{PLH}	Propagation Delay, TDO to PAD	1.97	3.37	4.77	0.03
t_{PHL}		1.67	2.97	4.27	0.03
t_{PLH}	Propagation Delay, UDDR to PAD	2.10	3.50	4.90	0.03
t_{PHL}		1.85	3.15	4.45	0.03
t_r	Output Rise Time, PAD	0.78	3.68	6.58	0.06
t_f	Output Fall Time, PAD	0.70	2.95	5.20	0.05
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00
		ON16S2J			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.53	2.48	3.43	0.02
t_{PHL}		1.49	2.39	3.29	0.02
t_{PLH}	Propagation Delay, OMC to PAD	1.72	2.67	3.62	0.02
t_{PHL}		1.67	2.57	3.47	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.98	2.93	3.88	0.02
t_{PHL}		1.85	2.75	3.65	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	2.12	3.07	4.02	0.02
t_{PHL}		2.02	2.92	3.82	0.02
t_r	Output Rise Time, PAD	0.78	2.53	4.28	0.04
t_f	Output Fall Time, PAD	0.64	2.09	3.54	0.03
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

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TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5//5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ON4S2J			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.38	2.58	3.78	0.02
t_{PHL}		1.31	4.41	7.51	0.06
t_{PLH}	Propagation Delay, OMC to PAD	1.58	2.78	3.98	0.02
t_{PHL}		1.51	4.61	7.71	0.06
t_{PLH}	Propagation Delay, TDO to PAD	1.80	3.00	4.20	0.02
t_{PHL}		1.69	4.79	7.89	0.06
t_{PLH}	Propagation Delay, UDDR to PAD	1.93	3.13	4.33	0.02
t_{PHL}		1.87	4.97	8.07	0.06
t_r	Output Rise Time, PAD	0.71	5.81	10.91	0.10
t_f	Output Fall Time, PAD	0.55	4.35	8.15	0.08
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5//5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ON8S2J			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.34	2.14	2.94	0.02
t_{PHL}		1.47	3.42	5.37	0.04
t_{PLH}	Propagation Delay, OMC to PAD	1.47	2.27	3.07	0.02
t_{PHL}		1.64	3.59	5.54	0.04
t_{PLH}	Propagation Delay, TDO to PAD	1.74	2.54	3.34	0.02
t_{PHL}		1.82	3.77	5.72	0.04
t_{PLH}	Propagation Delay, UDDR to PAD	1.87	2.67	3.47	0.02
t_{PHL}		1.99	3.94	5.89	0.04
t_r	Output Rise Time, PAD	0.78	3.68	6.58	0.06
t_f	Output Fall Time, PAD	0.70	2.95	5.20	0.05
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00
		ON16S2J			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.30	1.90	2.50	0.01
t_{PHL}		1.63	2.93	4.23	0.03
t_{PLH}	Propagation Delay, OMC to PAD	1.49	2.09	2.69	0.01
t_{PHL}		1.81	3.11	4.41	0.03
t_{PLH}	Propagation Delay, TDO to PAD	1.75	2.35	2.95	0.01
t_{PHL}		1.99	3.29	4.59	0.03
t_{PLH}	Propagation Delay, UDDR to PAD	1.88	2.48	3.08	0.01
t_{PHL}		2.16	3.46	4.76	0.03
t_r	Output Rise Time, PAD	0.78	2.53	4.28	0.04
t_f	Output Fall Time, PAD	0.64	2.09	3.54	0.03
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V
		Minimum Requirement
	ON4S2J	
t_{su}	Set Up Time, DO to CKDR	0.39
t_{su}	Set Up Time, SHDR to CKDR	0.25
t_{su}	Set Up Time, TDI to CKDR	0.14
t_h	Hold Time, CKDR to DO,SHDR	0.18
t_h	Hold Time, CKDR to TDI	0.32
t_w	Pulse Width, CKDR(L)	0.40
t_w	Pulse Width, CKDR(H)	0.78
t_w	Pulse Width, UDDR(H)	0.47

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V
		Minimum Requirement
	ON8S2J	
t_{su}	Set Up Time, DO to CKDR	0.18
t_{su}	Set Up Time, SHDR to CKDR	0.25
t_{su}	Set Up Time, TDI to CKDR	0.14
t_h	Hold Time, CKDR to DO	0.26
t_h	Hold Time, CKDR to SHDR	0.19
t_h	Hold Time, CKDR to TDI	0.32
t_w	Pulse Width, CKDR(L)	0.40
t_w	Pulse Width, CKDR(H)	0.78
t_w	Pulse Width, UDDR(H)	0.46
	ON16S2J	
t_{su}	Set Up Time, DO to CKDR	0.19
t_{su}	Set Up Time, SHDR to CKDR	0.25
t_{su}	Set Up Time, TDI to CKDR	0.14
t_h	Hold Time, CKDR to DO	0.25
t_h	Hold Time, CKDR to SHDR	0.19
t_h	Hold Time, CKDR to TDI	0.32
t_w	Pulse Width, CKDR(L)	0.40
t_w	Pulse Width, CKDR(H)	0.78
t_w	Pulse Width, UDDR(H)	0.46

NOTE:
For Functional Diagram see page 7-124

Non-Inverting Open-Drain Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

ON4ODJ
ONL4ODJ

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD,TDO / DO,CKDR,UDDR,SHDR,TDI,OMC

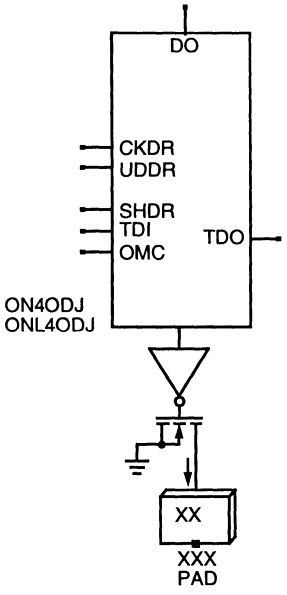
MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF DO: 0.32pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
All	PAD: 4.96pF

FUNCTION TABLE

JTAG	
DO	PAD
L	L
H	Z

JTAG
For JTAG Truth Table Information, See Table 7-5 "JTAG Logic Truth Table - Clock/"Sample Only" Inputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON4ODJ				ONL4ODJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.76	0.76	0.76	0.00	1.13	1.13	1.13	0.00
t_{PHL}		0.68	0.68	0.68	0.00	0.95	0.95	0.95	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.70	0.70	0.71	0.00	0.93	0.93	0.94	0.00
t_{PHL}		0.69	2.69	4.69	0.04	0.88	3.33	5.78	0.05
t_{PLH}	Propagation Delay, OMC to PAD	1.54	1.55	1.55	0.00	1.92	1.93	1.93	0.00
t_{PHL}		1.54	3.24	4.94	0.03	1.92	3.97	6.02	0.04
t_{PLH}	Propagation Delay, TDO to PAD	1.05	1.05	1.06	0.00	1.46	1.47	1.47	0.00
t_{PHL}		1.06	3.06	5.06	0.04	1.46	3.91	6.36	0.05
t_{PLH}	Propagation Delay, UDDR to PAD	1.23	1.24	1.24	0.00	1.68	1.68	1.69	0.00
t_{PHL}		1.23	3.23	5.23	0.04	1.68	4.13	6.58	0.05
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.41	4.51	8.61	0.08	0.48	5.58	10.68	0.10
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

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TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON4ODJ				ONL4ODJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.76	0.76	0.76	0.00	1.13	1.13	1.13	0.00
t_{PHL}		0.68	0.68	0.68	0.00	0.95	0.95	0.95	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.79	0.79	0.80	0.00	0.97	0.97	0.98	0.00
t_{PHL}		0.78	3.93	7.08	0.06	0.93	3.93	6.93	0.06
t_{PLH}	Propagation Delay, OMC to PAD	2.03	2.04	2.04	0.00	2.17	2.17	2.18	0.00
t_{PHL}		2.03	4.68	7.33	0.05	2.17	4.67	7.17	0.05
t_{PLH}	Propagation Delay, TDO to PAD	1.14	1.14	1.15	0.00	1.51	1.51	1.52	0.00
t_{PHL}		1.15	4.30	7.45	0.06	1.50	4.50	7.50	0.06
t_{PLH}	Propagation Delay, UDDR to PAD	1.32	1.32	1.33	0.00	1.72	1.72	1.73	0.00
t_{PHL}		1.32	4.47	7.62	0.06	1.72	4.72	7.72	0.06
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.41	4.51	8.61	0.08	0.48	5.58	10.68	0.10
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		ON4ODJ	ONL4ODJ
t_{su}	Set Up Time, DO to CKDR	0.18	0.34
t_{su}	Set Up Time, SHDR to CKDR	0.24	0.43
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26
t_h	Hold Time, CKDR to DO,TDI	0.30	0.41
t_h	Hold Time, CKDR to SHDR	0.19	0.25
t_w	Pulse Width, CKDR(L)	0.41	0.67
t_w	Pulse Width, CKDR(H)	0.65	1.00
t_w	Pulse Width, UDDR(H)	0.46	0.66

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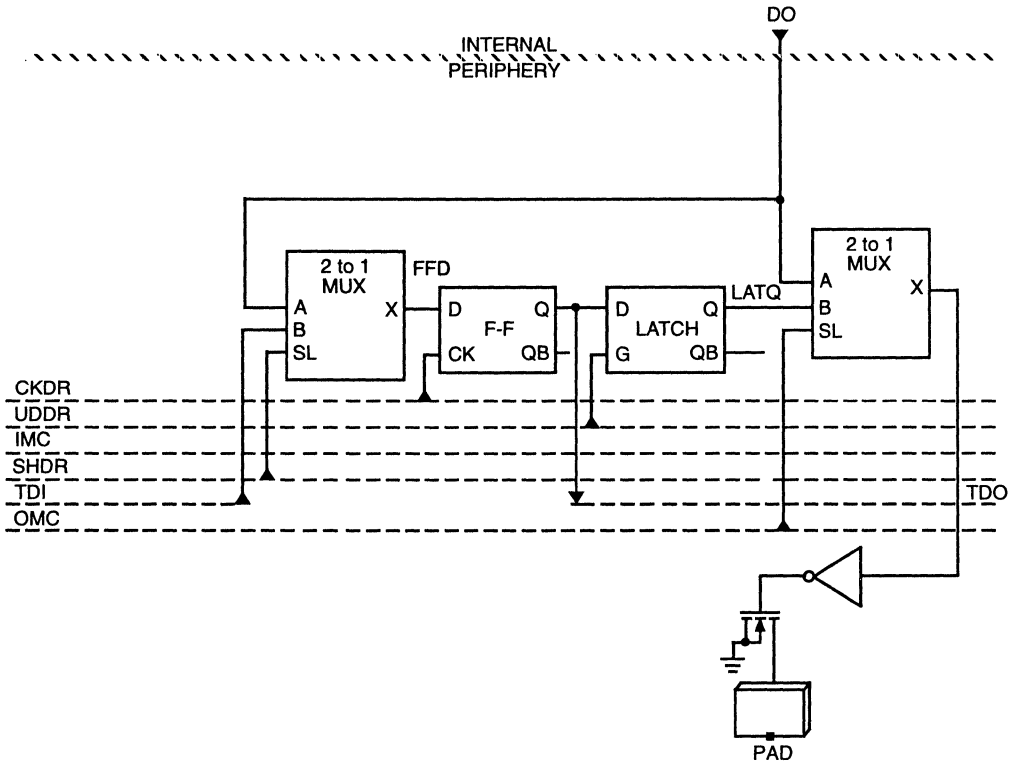
FUNCTIONAL DIAGRAM: ONxODJ



7

Non-Inverting Open-Drain Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

ON8ODJ
ONL8ODJ

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD,TDO / DO,CKDR,UDDR,SHDR,TDI,OMC

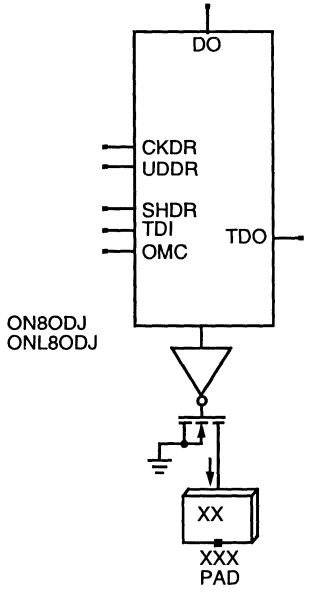
MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF DO: 0.35pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
All	PAD: 4.96pF

FUNCTION TABLE

JTAG	
DO	PAD
L	L
H	Z

JTAG
For JTAG Truth Table Information, See Table 7-5 "JTAG Logic Truth Table - Clock/"Sample Only" Inputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON8ODJ				ONL8ODJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.76	0.76	0.76	0.00	1.13	1.13	1.13	0.00
t_{PHL}		0.68	0.68	0.68	0.00	0.95	0.95	0.95	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.74	0.75	0.75	0.00	1.03	1.03	1.04	0.00
t_{PHL}		0.75	2.00	3.25	0.03	0.99	2.49	3.99	0.03
t_{PLH}	Propagation Delay, OMC to PAD	1.35	1.36	1.36	0.00	1.72	1.73	1.73	0.00
t_{PHL}		1.35	2.40	3.45	0.02	1.72	2.97	4.22	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.13	1.13	1.14	0.00	1.58	1.59	1.59	0.00
t_{PHL}		1.13	2.38	3.63	0.03	1.58	3.08	4.58	0.03
t_{PLH}	Propagation Delay, UDDR to PAD	1.31	1.31	1.32	0.00	1.80	1.80	1.81	0.00
t_{PHL}		1.31	2.56	3.81	0.03	1.80	3.30	4.80	0.03
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.53	2.88	5.23	0.05	0.63	3.53	6.43	0.06
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON8ODJ				ONL8ODJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.76	0.76	0.76	0.00	1.13	1.13	1.13	0.00
t_{PHL}		0.68	0.68	0.68	0.00	0.95	0.95	0.95	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.85	0.86	0.86	0.00	1.09	1.09	1.10	0.00
t_{PHL}		0.86	2.76	4.66	0.04	1.05	2.90	4.75	0.04
t_{PLH}	Propagation Delay, OMC to PAD	1.70	1.70	1.71	0.00	1.89	1.90	1.90	0.00
t_{PHL}		1.70	3.30	4.90	0.03	1.89	3.44	4.99	0.03
t_{PLH}	Propagation Delay, TDO to PAD	1.24	1.24	1.25	0.00	1.64	1.65	1.65	0.00
t_{PHL}		1.24	3.14	5.04	0.04	1.64	3.49	5.34	0.04
t_{PLH}	Propagation Delay, UDDR to PAD	1.42	1.42	1.43	0.00	1.85	1.86	1.86	0.00
t_{PHL}		1.42	3.32	5.22	0.04	1.85	3.70	5.55	0.04
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.53	2.88	5.23	0.05	0.63	3.53	6.43	0.06
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		ON8ODJ	ONL8ODJ
t_{su}	Set Up Time, DO to CKDR	0.18	0.36
t_{su}	Set Up Time, SHDR to CKDR	0.24	0.43
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26
t_h	Hold Time, CKDR to DO,TDI	0.30	0.40
t_h	Hold Time, CKDR to SHDR	0.19	0.25
t_w	Pulse Width, CKDR(L)	0.41	0.67
t_w	Pulse Width, CKDR(H)	0.65	1.00
t_w	Pulse Width, UDDR(H)	0.46	0.66

NOTE:
For Functional Diagram see page 7-137

Non-Inverting Open-Drain Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/3.3 V

ON16ODJ
ONL16ODJ

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD,TDO / DO,CKDR,UDDR,SHDR,TDI,OMC

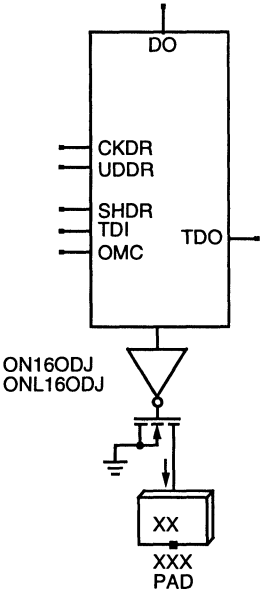
MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF DO: 0.40pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
All	PAD: 4.96pF

FUNCTION TABLE

JTAG	
DO	PAD
L	L
H	Z

JTAG
For JTAG Truth Table Information, See Table 7-5 "JTAG Logic Truth Table - Clock/"Sample Only" Inputs" on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON16ODJ				ONL16ODJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.76	0.76	0.76	0.00	1.13	1.13	1.13	0.00
t_{PHL}		0.68	0.68	0.68	0.00	0.95	0.95	0.95	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.79	0.79	0.80	0.00	1.09	1.10	1.10	0.00
t_{PHL}		0.79	1.64	2.49	0.02	1.06	2.06	3.06	0.02
t_{PLH}	Propagation Delay, OMC to PAD	1.28	1.28	1.29	0.00	1.63	1.64	1.64	0.00
t_{PHL}		1.28	1.98	2.68	0.01	1.63	2.48	3.33	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.19	1.19	1.20	0.00	1.68	1.68	1.69	0.00
t_{PHL}		1.19	2.04	2.89	0.02	1.67	2.67	3.67	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	1.37	1.37	1.38	0.00	1.89	1.89	1.90	0.00
t_{PHL}		1.37	2.22	3.07	0.02	1.89	2.89	3.89	0.02
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.54	1.99	3.44	0.03	0.63	2.38	4.13	0.03
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON16ODJ				ONL16ODJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.76	0.76	0.76	0.00	1.13	1.13	1.13	0.00
t_{PHL}		0.68	0.68	0.68	0.00	0.95	0.95	0.95	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.90	0.91	0.91	0.00	1.15	1.16	1.16	0.00
t_{PHL}		0.91	2.16	3.41	0.03	1.12	2.32	3.52	0.02
t_{PLH}	Propagation Delay, OMC to PAD	1.53	1.53	1.54	0.00	1.76	1.77	1.77	0.00
t_{PHL}		1.53	2.58	3.63	0.02	1.76	2.76	3.76	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.30	1.30	1.31	0.00	1.74	1.74	1.75	0.00
t_{PHL}		1.30	2.55	3.80	0.03	1.73	2.93	4.13	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	1.48	1.49	1.49	0.00	1.94	1.95	1.95	0.00
t_{PHL}		1.48	2.73	3.98	0.03	1.94	3.14	4.34	0.02
t_r	Output Rise Time, PAD	0.00	0.01	0.01	0.00	0.00	0.01	0.01	0.00
t_f	Output Fall Time, PAD	0.54	1.99	3.44	0.03	0.63	2.38	4.13	0.03
t_r	Output Rise Time, TDO	0.63	0.63	0.63	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		ON16ODJ	ONL16ODJ
t_{su}	Set Up Time, DO to CKDR	0.18	0.34
t_{su}	Set Up Time, SHDR to CKDR	0.24	0.43
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26
t_h	Hold Time, CKDR to DO,TDI	0.31	0.40
t_h	Hold Time, CKDR to SHDR	0.19	0.25
t_w	Pulse Width, CKDR(L)	0.41	0.67
t_w	Pulse Width, CKDR(H)	0.65	1.00
t_w	Pulse Width, UDDR(H)	0.46	0.66

NOTE:
For Functional Diagram see page 7-137

Non-Inverting 3-State Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
5/3.3 V
3.3/5 V
3.3/3.3 V

ON4TJ
ONX4TJ
ONLX4TJ
ONL4TJ

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD,TDO / DO,EN,CKDR,UDDR,SHDR,TDI,OMC

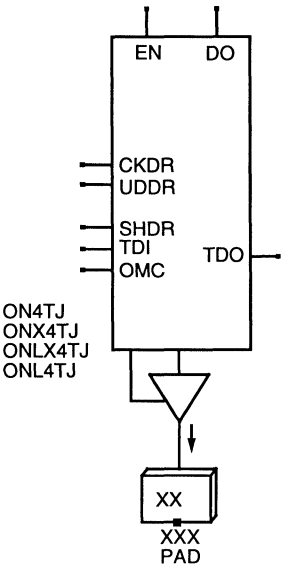
MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF DO: 0.24pF EN: 0.19pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
All	PAD: 4.96pF

FUNCTION TABLE

JTAG		
DO	EN	PAD
L	H	L
H	H	H
X	L	Z

JTAG
For JTAG Truth Table Information, See Table 7-6 "JTAG Logic Truth Tables - Outputs" on page 7-184 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON4TJ				ONLX4TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.00	3.25	5.50	0.05	1.04	3.29	5.54	0.05
t_{PHL}		1.02	2.97	4.92	0.04	0.83	2.88	4.93	0.04
t_{PLZ}	Propagation Delay, EN to PAD	0.82	0.82	0.83	0.00	0.82	0.83	0.83	0.00
t_{PZL}		0.91	2.91	4.91	0.04	0.92	3.77	6.62	0.06
t_{PZH}	Propagation Delay, EN to PAD	0.86	3.16	5.46	0.05	0.91	3.21	5.51	0.05
t_{PHZ}		0.85	0.86	0.86	0.00	0.90	0.91	0.91	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.16	3.41	5.66	0.05	1.21	3.46	5.71	0.05
t_{PHL}		1.21	3.16	5.11	0.04	1.02	3.07	5.12	0.04
t_{PLH}	Propagation Delay, TDO to PAD	1.42	3.67	5.92	0.05	1.47	3.72	5.97	0.05
t_{PHL}		1.38	3.33	5.28	0.04	1.19	3.24	5.29	0.04
t_{PLH}	Propagation Delay, UDDR to PAD	1.55	3.80	6.05	0.05	1.60	3.85	6.10	0.05
t_{PHL}		1.56	3.51	5.46	0.04	1.37	3.42	5.47	0.04
t_r	Output Rise Time, PAD	0.38	5.53	10.69	0.10	0.38	5.53	10.68	0.10
t_f	Output Fall Time, PAD	0.37	4.17	7.97	0.08	0.28	4.93	9.58	0.09
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX4TJ				ONL4TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.39	3.59	5.79	0.04	1.35	4.55	7.75	0.06
t_{PHL}		1.91	4.86	7.81	0.06	1.37	3.72	6.07	0.05
t_{PLZ}	Propagation Delay, EN to PAD	0.84	0.85	0.85	0.00	1.07	1.07	1.08	0.00
t_{PZL}		0.95	3.50	6.05	0.05	1.15	3.60	6.05	0.05
t_{PZH}	Propagation Delay, EN to PAD	1.19	3.44	5.69	0.04	1.14	4.44	7.74	0.07
t_{PHZ}		1.17	1.18	1.18	0.00	1.11	1.12	1.12	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.68	3.88	6.08	0.04	1.65	4.85	8.05	0.06
t_{PHL}		2.19	5.14	8.09	0.06	1.63	3.98	6.33	0.05
t_{PLH}	Propagation Delay, TDO to PAD	2.09	4.29	6.49	0.04	2.07	5.27	8.47	0.06
t_{PHL}		2.49	5.44	8.39	0.06	1.94	4.29	6.64	0.05
t_{PLH}	Propagation Delay, UDDR to PAD	2.19	4.39	6.59	0.04	2.15	5.35	8.55	0.06
t_{PHL}		2.72	5.67	8.62	0.06	2.16	4.51	6.86	0.05
t_r	Output Rise Time, PAD	0.24	5.24	10.24	0.10	0.48	7.63	14.78	0.14
t_f	Output Fall Time, PAD	0.33	6.08	11.83	0.11	0.44	5.09	9.74	0.09
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON4TJ				ONLX4TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.92	2.07	3.22	0.02	1.01	2.76	4.51	0.04
t_{PHL}		1.10	4.15	7.20	0.06	0.86	3.46	6.06	0.05
t_{PLZ}	Propagation Delay, EN to PAD	0.91	0.91	0.92	0.00	0.86	0.86	0.87	0.00
t_{PZL}		1.00	4.15	7.30	0.06	0.96	4.41	7.86	0.07
t_{PZH}	Propagation Delay, EN to PAD	0.77	1.92	3.07	0.02	0.87	2.62	4.37	0.04
t_{PHZ}		0.77	0.78	0.78	0.00	0.87	0.87	0.88	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.08	2.23	3.38	0.02	1.18	2.93	4.68	0.04
t_{PHL}		1.30	4.35	7.40	0.06	1.05	3.65	6.25	0.05
t_{PLH}	Propagation Delay, TDO to PAD	1.34	2.49	3.64	0.02	1.44	3.19	4.94	0.04
t_{PHL}		1.46	4.51	7.56	0.06	1.22	3.82	6.42	0.05
t_{PLH}	Propagation Delay, UDDR to PAD	1.47	2.62	3.77	0.02	1.57	3.32	5.07	0.04
t_{PHL}		1.64	4.69	7.74	0.06	1.40	4.00	6.60	0.05
t_r	Output Rise Time, PAD	0.38	5.53	10.69	0.10	0.38	5.53	10.68	0.10
t_f	Output Fall Time, PAD	0.37	4.17	7.97	0.08	0.28	4.93	9.58	0.09
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX4TJ				ONL4TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.34	2.44	3.54	0.02	1.31	3.81	6.31	0.05
t_{PHL}		2.01	6.56	11.11	0.09	1.40	4.30	7.20	0.06
t_{PLZ}	Propagation Delay, EN to PAD	0.95	0.95	0.96	0.00	1.11	1.11	1.12	0.00
t_{PZL}		1.05	5.30	9.55	0.08	1.19	4.19	7.19	0.06
t_{PZH}	Propagation Delay, EN to PAD	1.13	2.28	3.43	0.02	1.09	3.64	6.19	0.05
t_{PHZ}		1.12	1.12	1.13	0.00	1.07	1.07	1.08	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.63	2.73	3.83	0.02	1.60	4.10	6.60	0.05
t_{PHL}		2.28	6.83	11.38	0.09	1.67	4.57	7.47	0.06
t_{PLH}	Propagation Delay, TDO to PAD	2.04	3.14	4.24	0.02	2.02	4.52	7.02	0.05
t_{PHL}		2.58	7.13	11.68	0.09	1.97	4.87	7.77	0.06
t_{PLH}	Propagation Delay, UDDR to PAD	2.14	3.24	4.34	0.02	2.10	4.60	7.10	0.05
t_{PHL}		2.81	7.36	11.91	0.09	2.19	5.09	7.99	0.06
t_r	Output Rise Time, PAD	0.24	5.24	10.24	0.10	0.48	7.63	14.78	0.14
t_f	Output Fall Time, PAD	0.33	6.08	11.83	0.11	0.44	5.09	9.74	0.09
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

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CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

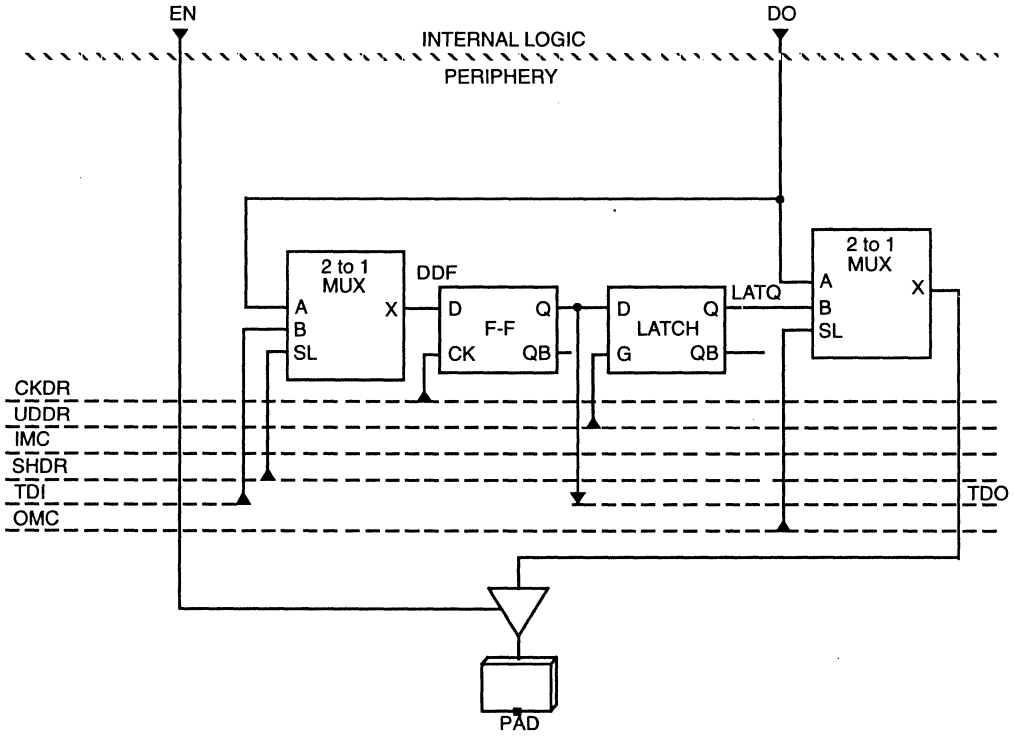
Sym	Parameter	5/5 V	3.3/5 V
		Minimum Requirement	Minimum Requirement
		ON4TJ	ONL4TJ
t_{su}	Set Up Time, DO to CKDR	0.19	0.19
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.25
t_{su}	Set Up Time, TDI to CKDR	0.14	0.14
t_h	Hold Time, CKDR to DO	0.26	0.26
t_h	Hold Time, CKDR to SHDR	0.19	0.19
t_h	Hold Time, CKDR to TDI	0.32	0.32
t_w	Pulse Width, CKDR(L)	0.40	0.40
t_w	Pulse Width, CKDR(H)	0.78	0.78
t_w	Pulse Width, UDDR(H)	0.47	0.46

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		ONX4TJ	ONL4TJ
t_{su}	Set Up Time, DO to CKDR	0.36	0.35
t_{su}	Set Up Time, SHDR to CKDR	0.43	0.43
t_{su}	Set Up Time, TDI to CKDR	0.28	0.28
t_h	Hold Time, CKDR to DO	0.36	0.36
t_h	Hold Time, CKDR to SHDR	0.25	0.25
t_h	Hold Time, CKDR to TDI	0.42	0.42
t_w	Pulse Width, CKDR(L)	0.67	0.67
t_w	Pulse Width, CKDR(H)	1.18	1.18
t_w	Pulse Width, UDDR(H)	0.64	0.64

FUNCTIONAL DIAGRAM: ONxTJ



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Non-Inverting 3-State Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
5/3.3 V
3.3/5 V
3.3/3.3 V

ON8TJ
ONX8TJ
ONLX8TJ
ONL8TJ

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD,TDO / DO,EN,CKDR,UDDR,SHDR,TDI,OMC

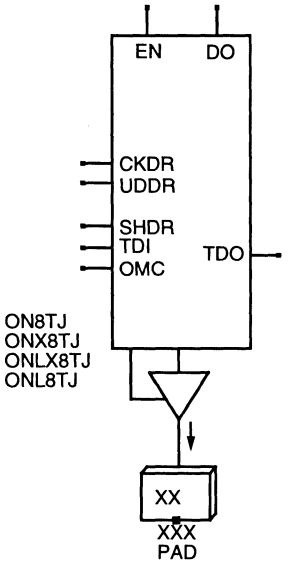
MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF DO: 0.24pF EN: 0.19pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
All	PAD: 5.10pF

FUNCTION TABLE

JTAG		
DO	EN	PAD
L	H	L
H	H	H
X	L	Z

JTAG
For JTAG Truth Table Information, See Table 7-6 "JTAG Logic Truth Tables - Outputs" on page 7-184 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON8TJ				ONLX8TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.92	2.22	3.52	0.03	1.34	2.69	4.04	0.03
t_{PHL}		1.10	2.35	3.60	0.03	1.16	2.26	3.36	0.02
t_{PLZ}	Propagation Delay, EN to PAD	0.90	0.90	0.91	0.00	1.14	1.15	1.15	0.00
t_{PZL}		0.99	2.24	3.49	0.03	1.24	2.69	4.14	0.03
t_{PZH}	Propagation Delay, EN to PAD	0.78	2.08	3.38	0.03	1.21	2.61	4.01	0.03
t_{PHZ}		0.77	0.78	0.78	0.00	1.20	1.21	1.21	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.08	2.38	3.68	0.03	1.50	2.86	4.20	0.03
t_{PHL}		1.29	2.54	3.79	0.03	1.36	2.45	3.56	0.02
t_{PLH}	Propagation Delay, TDO to PAD	1.35	2.65	3.95	0.03	1.77	3.12	4.47	0.03
t_{PHL}		1.46	2.71	3.96	0.03	1.53	2.63	3.73	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	1.48	2.78	4.08	0.03	1.90	3.25	4.60	0.03
t_{PHL}		1.64	2.89	4.14	0.03	1.70	2.80	3.90	0.02
t_r	Output Rise Time, PAD	0.29	3.24	6.19	0.06	0.59	3.54	6.49	0.06
t_f	Output Fall Time, PAD	0.48	2.73	4.98	0.05	0.55	2.85	5.15	0.05
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX8TJ				ONL8TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.55	2.80	4.05	0.02	1.31	3.16	5.01	0.04
t_{PHL}		2.03	3.58	5.13	0.03	1.49	2.99	4.49	0.03
t_{PLZ}	Propagation Delay, EN to PAD	1.18	1.19	1.19	0.00	1.18	1.19	1.19	0.00
t_{PZL}		1.27	2.67	4.07	0.03	1.27	2.77	4.27	0.03
t_{PZH}	Propagation Delay, EN to PAD	1.35	2.65	3.95	0.03	1.10	2.95	4.80	0.04
t_{PHZ}		1.34	1.34	1.35	0.00	1.08	1.08	1.09	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.84	3.09	4.34	0.02	1.60	3.45	5.30	0.04
t_{PHL}		2.30	3.85	5.40	0.03	1.76	3.26	4.76	0.03
t_{PLH}	Propagation Delay, TDO to PAD	2.26	3.51	4.76	0.02	2.01	3.86	5.71	0.04
t_{PHL}		2.60	4.15	5.70	0.03	2.04	3.54	5.04	0.03
t_{PLH}	Propagation Delay, UDDR to PAD	2.35	3.60	4.85	0.02	2.09	3.94	5.79	0.04
t_{PHL}		2.83	4.38	5.93	0.03	2.26	3.76	5.26	0.03
t_r	Output Rise Time, PAD	0.19	3.04	5.89	0.06	0.35	4.40	8.45	0.08
t_f	Output Fall Time, PAD	0.57	3.37	6.17	0.06	0.59	3.34	6.09	0.05
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON8TJ				ONLX8TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.85	1.50	2.15	0.01	1.28	2.33	3.38	0.02
t_{PHL}		1.20	3.10	5.00	0.04	1.21	2.61	4.01	0.03
t_{PLZ}	Propagation Delay, EN to PAD	1.01	1.01	1.02	0.00	1.19	1.19	1.20	0.00
t_{PZL}		1.11	3.01	4.91	0.04	1.28	3.03	4.78	0.04
t_{PZH}	Propagation Delay, EN to PAD	0.71	1.36	2.01	0.01	1.14	2.24	3.34	0.02
t_{PHZ}		0.70	0.70	0.71	0.00	1.13	1.14	1.14	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.01	1.66	2.31	0.01	1.44	2.49	3.54	0.02
t_{PHL}		1.40	3.30	5.20	0.04	1.41	2.81	4.21	0.03
t_{PLH}	Propagation Delay, TDO to PAD	1.28	1.93	2.58	0.01	1.71	2.76	3.81	0.02
t_{PHL}		1.57	3.47	5.37	0.04	1.58	2.98	4.38	0.03
t_{PLH}	Propagation Delay, UDDR to PAD	1.41	2.06	2.71	0.01	1.84	2.89	3.94	0.02
t_{PHL}		1.75	3.65	5.55	0.04	1.75	3.15	4.55	0.03
t_r	Output Rise Time, PAD	0.29	3.24	6.19	0.06	0.59	3.54	6.49	0.06
t_f	Output Fall Time, PAD	0.48	2.73	4.98	0.05	0.55	2.85	5.15	0.05
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

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TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ONX8TJ				ONL8TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00	1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.51	2.16	2.81	0.01	1.28	2.68	4.08	0.03
t_{PHL}		2.15	4.50	6.85	0.05	1.54	3.34	5.14	0.04
t_{PLZ}	Propagation Delay, EN to PAD	1.38	1.39	1.39	0.00	1.24	1.25	1.25	0.00
t_{PZL}		1.47	3.67	5.87	0.04	1.32	3.17	5.02	0.04
t_{PZH}	Propagation Delay, EN to PAD	1.31	1.96	2.61	0.01	1.07	2.52	3.97	0.03
t_{PHZ}		1.30	1.30	1.31	0.00	1.05	1.05	1.06	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.81	2.46	3.11	0.01	1.57	2.97	4.37	0.03
t_{PHL}		2.41	4.76	7.11	0.05	1.81	3.61	5.41	0.04
t_{PLH}	Propagation Delay, TDO to PAD	2.22	2.87	3.52	0.01	1.98	3.38	4.78	0.03
t_{PHL}		2.72	5.07	7.42	0.05	2.10	3.90	5.70	0.04
t_{PLH}	Propagation Delay, UDDR to PAD	2.31	2.96	3.61	0.01	2.06	3.46	4.86	0.03
t_{PHL}		2.94	5.29	7.64	0.05	2.31	4.11	5.91	0.04
t_r	Output Rise Time, PAD	0.19	3.04	5.89	0.06	0.35	4.40	8.45	0.08
t_f	Output Fall Time, PAD	0.57	3.37	6.17	0.06	0.59	3.34	6.09	0.05
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/5 V
		Minimum Requirement	Minimum Requirement
		ON8TJ	ONLX8TJ
t_{su}	Set Up Time, DO to CKDR	0.19	0.19
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.25
t_{su}	Set Up Time, TDI to CKDR	0.14	0.14
t_h	Hold Time, CKDR to DO	0.26	0.26
t_h	Hold Time, CKDR to SHDR	0.19	0.19
t_h	Hold Time, CKDR to TDI	0.32	0.32
t_w	Pulse Width, CKDR(L)	0.40	0.40
t_w	Pulse Width, CKDR(H)	0.78	0.78
t_w	Pulse Width, UDDR(H)	0.47	0.46

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/3.3 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		ONX8TJ	ONL8TJ
t_{su}	Set Up Time, DO to CKDR	0.36	0.35
t_{su}	Set Up Time, SHDR to CKDR	0.43	0.43
t_{su}	Set Up Time, TDI to CKDR	0.28	0.28
t_h	Hold Time, CKDR to DO	0.36	0.37
t_h	Hold Time, CKDR to SHDR	0.25	0.25
t_h	Hold Time, CKDR to TDI	0.42	0.42
t_w	Pulse Width, CKDR(L)	0.67	0.67
t_w	Pulse Width, CKDR(H)	1.18	1.18
t_w	Pulse Width, UDDR(H)	0.64	0.64

NOTE:
For Functional Diagram see page 7-145

Non-Inverting 3-State Output Buffers - JTAG (3.3 V and 5 V System/Core Voltage)

5/5 V
3.3/5 V
3.3/3.3 V

ON16TJ
ONLX16TJ
ONL16TJ

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD,TDO / DO,EN,CKDR,UDDR,SHDR,TDI,OMC

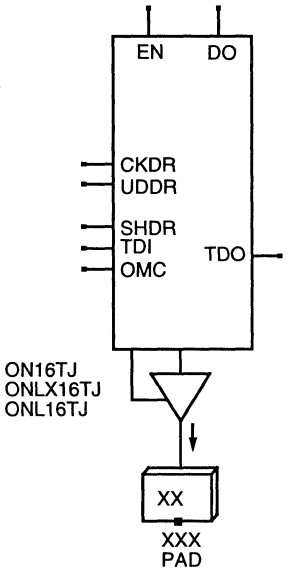
MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF DO,EN: 0.24pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
All	PAD: 5.76pF

FUNCTION TABLE

JTAG		
DO	EN	PAD
L	H	L
H	H	H
X	L	Z

JTAG
For JTAG Truth Table Information, See Table 7-6 "JTAG Logic Truth Tables - Outputs" on page 7-184 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON16TJ				ONLX16TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.04	1.84	2.64	0.02	1.29	2.64	3.99	0.03
t_{PHL}		1.18	1.98	2.78	0.02	1.07	1.72	2.37	0.01
t_{PLZ}	Propagation Delay, EN to PAD	0.90	0.91	0.91	0.00	0.95	0.96	0.96	0.00
t_{PZL}		0.99	1.84	2.69	0.02	1.04	1.84	2.64	0.02
t_{PZH}	Propagation Delay, EN to PAD	0.90	1.75	2.60	0.02	1.14	2.54	3.94	0.03
t_{PHZ}		0.89	0.90	0.90	0.00	1.13	1.14	1.14	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.22	2.02	2.82	0.02	1.47	2.82	4.17	0.03
t_{PHL}		1.36	2.16	2.96	0.02	1.25	1.90	2.55	0.01
t_{PLH}	Propagation Delay, TDO to PAD	1.47	2.27	3.07	0.02	1.72	3.07	4.42	0.03
t_{PHL}		1.53	2.33	3.13	0.02	1.42	2.07	2.72	0.01
t_{PLH}	Propagation Delay, UDDR to PAD	1.60	2.40	3.20	0.02	1.86	3.21	4.56	0.03
t_{PHL}		1.71	2.51	3.31	0.02	1.59	2.24	2.89	0.01
t_r	Output Rise Time, PAD	0.43	2.13	3.83	0.03	0.58	3.53	6.48	0.06
t_f	Output Fall Time, PAD	0.48	1.88	3.28	0.03	0.47	1.62	2.77	0.02
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ONL16TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.49	2.64	3.79	0.02
t_{PHL}		1.58	2.58	3.58	0.02
t_{PLZ}	Propagation Delay, EN to PAD	1.19	1.20	1.20	0.00
t_{PZL}		1.27	2.27	3.27	0.02
t_{PZH}	Propagation Delay, EN to PAD	1.23	2.38	3.53	0.02
t_{PHZ}		1.20	1.20	1.21	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.77	2.92	4.07	0.02
t_{PHL}		1.85	2.85	3.85	0.02
t_{PLH}	Propagation Delay, TDO to PAD	2.20	3.35	4.50	0.02
t_{PHL}		2.14	3.14	4.14	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	2.29	3.44	4.59	0.02
t_{PHL}		2.35	3.35	4.35	0.02
t_r	Output Rise Time, PAD	0.52	2.87	5.22	0.05
t_f	Output Fall Time, PAD	0.59	2.29	3.99	0.03
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		ON16TJ				ONLX16TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00	0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	0.92	1.37	1.81	0.01	1.23	2.28	3.33	0.02
t_{PHL}		1.29	2.49	3.69	0.02	1.11	1.86	2.61	0.01
t_{PLZ}	Propagation Delay, EN to PAD	1.01	1.02	1.02	0.00	0.99	0.99	1.00	0.00
t_{PZL}		1.10	2.35	3.60	0.03	1.08	1.98	2.88	0.02
t_{PZH}	Propagation Delay, EN to PAD	0.77	1.22	1.67	0.01	1.07	2.17	3.27	0.02
t_{PHZ}		0.76	0.76	0.77	0.00	1.06	1.07	1.07	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.09	1.54	1.99	0.01	1.40	2.45	3.50	0.02
t_{PHL}		1.47	2.67	3.87	0.02	1.29	2.04	2.79	0.01
t_{PLH}	Propagation Delay, TDO to PAD	1.35	1.80	2.25	0.01	1.66	2.71	3.76	0.02
t_{PHL}		1.64	2.84	4.04	0.02	1.47	2.22	2.97	0.01
t_{PLH}	Propagation Delay, UDDR to PAD	1.48	1.93	2.38	0.01	1.79	2.84	3.89	0.02
t_{PHL}		1.81	3.01	4.21	0.02	1.64	2.39	3.14	0.01
t_r	Output Rise Time, PAD	0.43	2.13	3.83	0.03	0.58	3.53	6.48	0.06
t_f	Output Fall Time, PAD	0.48	1.88	3.28	0.03	0.47	1.62	2.77	0.02
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00	0.41	0.41	0.41	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)
		ONL16TJ			
t_{PLH}	Propagation Delay, CKDR to TDO	1.04	1.04	1.04	0.00
t_{PHL}		1.01	1.01	1.01	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.43	2.33	3.23	0.02
t_{PHL}		1.64	2.84	4.04	0.02
t_{PLZ}	Propagation Delay, EN to PAD	1.25	1.26	1.26	0.00
t_{PZL}		1.33	2.53	3.73	0.02
t_{PZH}	Propagation Delay, EN to PAD	1.17	2.07	2.97	0.02
t_{PHZ}		1.14	1.14	1.15	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.71	2.61	3.51	0.02
t_{PHL}		1.91	3.11	4.31	0.02
t_{PLH}	Propagation Delay, TDO to PAD	2.14	3.04	3.94	0.02
t_{PHL}		2.20	3.40	4.60	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	2.23	3.13	4.03	0.02
t_{PHL}		2.41	3.61	4.81	0.02
t_r	Output Rise Time, PAD	0.52	2.87	5.22	0.05
t_f	Output Fall Time, PAD	0.59	2.29	3.99	0.03
t_r	Output Rise Time, TDO	0.87	0.87	0.87	0.00
t_f	Output Fall Time, TDO	0.52	0.52	0.52	0.00

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/5 V
		Minimum Requirement	Minimum Requirement
		ON16TJ	ONLX16TJ
t_{su}	Set Up Time, DO to CKDR	0.19	0.19
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.25
t_{su}	Set Up Time, TDI to CKDR	0.14	0.14
t_h	Hold Time, CKDR to DO	0.25	0.25
t_h	Hold Time, CKDR to SHDR	0.19	0.19
t_h	Hold Time, CKDR to TDI	0.32	0.32
t_w	Pulse Width, CKDR(L)	0.40	0.40
t_w	Pulse Width, CKDR(H)	0.78	0.78
t_w	Pulse Width, UDDR(H)	0.47	0.47

CMOS/TTL TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	3.3/3.3 V
		Minimum Requirement
		ONL16TJ
t_{su}	Set Up Time, DO to CKDR	0.40
t_{su}	Set Up Time, SHDR to CKDR	0.43
t_{su}	Set Up Time, TDI to CKDR	0.28
t_h	Hold Time, CKDR to DO	0.35
t_h	Hold Time, CKDR to SHDR	0.25
t_h	Hold Time, CKDR to TDI	0.42
t_w	Pulse Width, CKDR(L)	0.67
t_w	Pulse Width, CKDR(H)	1.18
t_w	Pulse Width, UDDR(H)	0.64

NOTE:
For Functional Diagram see page 7-145

Non-Inverting 3-State Output Buffers - JTAG With Slew Rate Control (S2) (5 V System/Core Voltage)

5/5 V

ON4TS2J
ON8TS2J
ON16TS2J

MACRO	SECTIONS USED
All	0/1

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PAD,TDO / DO,EN,CKDR,UDDR,SHDR,TDI,OMC

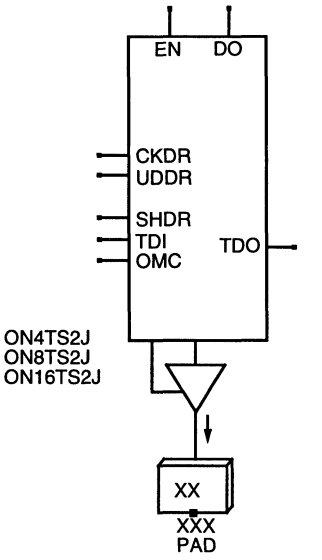
MACRO	INPUT CAP.
ON4TS2J, ON8TS2J	CKDR,TDI: 0.04pF DO: 0.24pF EN: 0.19pF OMC,SHDR: 0.10pF UDDR: 0.08pF
ON16TS2J	CKDR,TDI: 0.04pF DO,EN: 0.24pF OMC,SHDR: 0.10pF UDDR: 0.08pF

MACRO	OUTPUT CAP.
ON4TS2J	PAD: 4.96pF
ON8TS2J	PAD: 5.10pF
ON16TS2J	PAD: 5.76pF

FUNCTION TABLE

JTAG		
DO	EN	PAD
L	H	L
H	H	H
X	L	Z

JTAG
For JTAG Truth Table Information, See Table 7-6 "JTAG Logic Truth Tables - Outputs" on page 7-184 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
	ON4TS2J				
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.64	3.94	6.24	0.05
t_{PHL}		1.43	3.43	5.43	0.04
t_{PLZ}	Propagation Delay, EN to PAD	1.23	1.24	1.24	0.00
t_{PZL}		1.33	3.38	5.43	0.04
t_{PZH}	Propagation Delay, EN to PAD	1.52	3.87	6.22	0.05
t_{PHZ}		1.51	1.52	1.52	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.80	4.10	6.40	0.05
t_{PHL}		1.62	3.62	5.62	0.04
t_{PLH}	Propagation Delay, TDO to PAD	2.06	4.36	6.66	0.05
t_{PHL}		1.79	3.79	5.79	0.04
t_{PLH}	Propagation Delay, UDDR to PAD	2.19	4.49	6.79	0.05
t_{PHL}		1.96	3.96	5.96	0.04
t_r	Output Rise Time, PAD	0.70	5.80	10.90	0.10
t_f	Output Fall Time, PAD	0.55	4.35	8.15	0.08
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
ON8TS2J					
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.58	2.98	4.38	0.03
t_{PHL}		1.37	2.67	3.97	0.03
t_{PLZ}	Propagation Delay, EN to PAD	1.18	1.18	1.19	0.00
t_{PZL}		1.28	2.58	3.88	0.03
t_{PZH}	Propagation Delay, EN to PAD	1.46	2.86	4.26	0.03
t_{PHZ}		1.45	1.45	1.46	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.75	3.15	4.55	0.03
t_{PHL}		1.57	2.87	4.17	0.03
t_{PLH}	Propagation Delay, TDO to PAD	2.01	3.41	4.81	0.03
t_{PHL}		1.73	3.03	4.33	0.03
t_{PLH}	Propagation Delay, UDDR to PAD	2.14	3.54	4.94	0.03
t_{PHL}		1.91	3.21	4.51	0.03
t_r	Output Rise Time, PAD	0.79	3.69	6.59	0.06
t_f	Output Fall Time, PAD	0.71	2.96	5.21	0.05
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00
ON16TS2J					
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.72	2.67	3.62	0.02
t_{PHL}		1.52	2.42	3.32	0.02
t_{PLZ}	Propagation Delay, EN to PAD	1.26	1.27	1.27	0.00
t_{PZL}		1.35	2.25	3.15	0.02
t_{PZH}	Propagation Delay, EN to PAD	1.58	2.53	3.48	0.02
t_{PHZ}		1.57	1.58	1.58	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.89	2.84	3.79	0.02
t_{PHL}		1.70	2.60	3.50	0.02
t_{PLH}	Propagation Delay, TDO to PAD	2.15	3.10	4.05	0.02
t_{PHL}		1.88	2.78	3.68	0.02
t_{PLH}	Propagation Delay, UDDR to PAD	2.28	3.23	4.18	0.02
t_{PHL}		2.04	2.94	3.84	0.02
t_r	Output Rise Time, PAD	0.78	2.53	4.28	0.04
t_f	Output Fall Time, PAD	0.64	2.09	3.54	0.03
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
	ON4TS2J				
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.46	2.66	3.86	0.02
t_{PHL}		1.54	4.64	7.74	0.06
t_{PLZ}	Propagation Delay, EN to PAD	1.35	1.36	1.36	0.00
t_{PZL}		1.45	4.65	7.85	0.06
t_{PZH}	Propagation Delay, EN to PAD	1.33	2.53	3.73	0.02
t_{PHZ}		1.33	1.33	1.34	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.63	2.83	4.03	0.02
t_{PHL}		1.73	4.83	7.93	0.06
t_{PLH}	Propagation Delay, TDO to PAD	1.89	3.09	4.29	0.02
t_{PHL}		1.90	5.00	8.10	0.06
t_{PLH}	Propagation Delay, UDDR to PAD	2.02	3.22	4.42	0.02
t_{PHL}		2.08	5.18	8.28	0.06
t_r	Output Rise Time, PAD	0.70	5.80	10.90	0.10
t_f	Output Fall Time, PAD	0.55	4.35	8.15	0.08
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00
	ON8TS2J				
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.35	2.15	2.95	0.02
t_{PHL}		1.52	3.47	5.42	0.04
t_{PLZ}	Propagation Delay, EN to PAD	1.33	1.34	1.34	0.00
t_{PZL}		1.43	3.43	5.43	0.04
t_{PZH}	Propagation Delay, EN to PAD	1.22	2.02	2.82	0.02
t_{PHZ}		1.21	1.22	1.22	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.52	2.32	3.12	0.02
t_{PHL}		1.71	3.66	5.61	0.04
t_{PLH}	Propagation Delay, TDO to PAD	1.78	2.58	3.38	0.02
t_{PHL}		1.88	3.83	5.78	0.04
t_{PLH}	Propagation Delay, UDDR to PAD	1.91	2.71	3.51	0.02
t_{PHL}		2.06	4.01	5.96	0.04
t_r	Output Rise Time, PAD	0.79	3.69	6.59	0.06
t_f	Output Fall Time, PAD	0.71	2.96	5.21	0.05
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00
	ON16TS2J				
t_{PLH}	Propagation Delay, CKDR to TDO	0.71	0.71	0.71	0.00
t_{PHL}		0.72	0.72	0.72	0.00
t_{PLH}	Propagation Delay, DO to PAD	1.48	2.08	2.68	0.01
t_{PHL}		1.66	2.96	4.26	0.03
t_{PLZ}	Propagation Delay, EN to PAD	1.41	1.42	1.42	0.00
t_{PZL}		1.50	2.80	4.10	0.03
t_{PZH}	Propagation Delay, EN to PAD	1.34	1.94	2.54	0.01
t_{PHZ}		1.33	1.34	1.34	0.00
t_{PLH}	Propagation Delay, OMC to PAD	1.66	2.26	2.86	0.01
t_{PHL}		1.84	3.14	4.44	0.03

TTL SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V			
		pF=0	pF=50	pF=100	K (ns/pF)
t_{PLH}	Propagation Delay, TDO to PAD	1.91	2.51	3.11	0.01
t_{PHL}		2.02	3.32	4.62	0.03
t_{PLH}	Propagation Delay, UDDR to PAD	2.05	2.65	3.25	0.01
t_{PHL}		2.19	3.49	4.79	0.03
t_r	Output Rise Time, PAD	0.78	2.53	4.28	0.04
t_f	Output Fall Time, PAD	0.64	2.09	3.54	0.03
t_r	Output Rise Time, TDO	0.62	0.62	0.62	0.00
t_f	Output Fall Time, TDO	0.41	0.41	0.41	0.00

CMOS/TTL TIMING REQUIREMENTS

Rev.1.07

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Sym	Parameter	5/5 V
		Minimum Requirement
	ON4TS2J	
t_{su}	Set Up Time, DO to CKDR	0.19
t_{su}	Set Up Time, SHDR to CKDR	0.25
t_{su}	Set Up Time, TDI to CKDR	0.14
t_h	Hold Time, CKDR to DO	0.26
t_h	Hold Time, CKDR to SHDR	0.19
t_h	Hold Time, CKDR to TDI	0.32
t_w	Pulse Width, CKDR(L)	0.40
t_w	Pulse Width, CKDR(H)	0.78
t_w	Pulse Width, UDDR(H)	0.46
	ON8TS2J	
t_{su}	Set Up Time, DO to CKDR	0.19
t_{su}	Set Up Time, SHDR to CKDR	0.25
t_{su}	Set Up Time, TDI to CKDR	0.14
t_h	Hold Time, CKDR to DO	0.26
t_h	Hold Time, CKDR to SHDR	0.19
t_h	Hold Time, CKDR to TDI	0.32
t_w	Pulse Width, CKDR(L)	0.40
t_w	Pulse Width, CKDR(H)	0.78
t_w	Pulse Width, UDDR(H)	0.47
	ON16TS2J	
t_{su}	Set Up Time, DO to CKDR	0.19
t_{su}	Set Up Time, SHDR to CKDR	0.25
t_{su}	Set Up Time, TDI to CKDR	0.14
t_h	Hold Time, CKDR to DO	0.25
t_h	Hold Time, CKDR to SHDR	0.19
t_h	Hold Time, CKDR to TDI	0.32
t_w	Pulse Width, CKDR(L)	0.40
t_w	Pulse Width, CKDR(H)	0.78
t_w	Pulse Width, UDDR(H)	0.47

NOTE
For Funtional Diagram see page 7-145

Oscillator w/ Non-Inverting Input / 5/5 V / 3.3/3.3 V OSCPBJ/OSCPBLJ
Oscillator w/ Clock Buffer Input / 5/5 V / 3.3/3.3 V OSCPHBJ/OSCPHBLJ
Oscillator w/ Schmitt Trigger Input 5/5 V / 3.3/3.3 V OSCPSBJ/OSCPSBLJ
- JTAG
(3.3 V and 5 V System/Core Voltage)

MACRO	SECTIONS USED
All	1/0

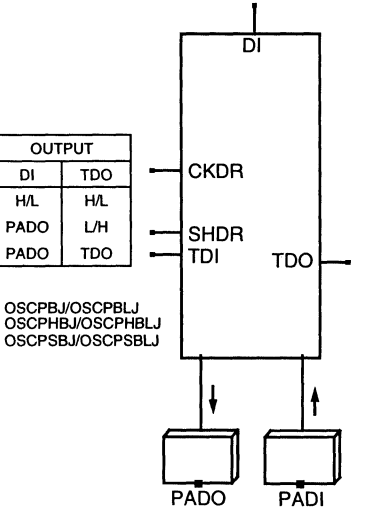
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	PADO,DI,TDO / CKDR,SHDR,TDI,PADI

MACRO	INPUT CAP.
All	CKDR,TDI: 0.04pF PADI: 5.76pF SHDR: 0.09pF

FUNCTION TABLE

INPUT					OUTPUT	
PADI	PADO	CKDR	SHDR	TDI	DI	TDO
L/H	H/L	⌐	L	X	H/L	H/L
X	X	⌐	H	L/H	PADO	L/H
X	X	⌙	X	X	PADO	TDO



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		OSCPBJ				**OSCPBLJ**			
t_{PLH}	Propagation Delay, CKDR to TDO	0.68	0.68	0.68	0.00	1.01	1.01	1.01	0.00
t_{PHL}		0.71	0.71	0.71	0.00	0.98	0.98	0.98	0.00
t_{PLH}	Propagation Delay, PADI to DI	2.53	2.65	3.03	1.25	3.37	3.54	4.07	1.76
t_{PHL}		3.03	3.17	3.61	1.44	3.84	3.97	4.36	1.28
t_r	Output Rise Time, DI	0.29	0.32	0.40	0.29	0.34	0.38	0.49	0.37
t_f	Output Fall Time, DI	0.32	0.35	0.42	0.26	0.30	0.33	0.42	0.30
t_r	Output Rise Time, TDO	0.58	0.58	0.58	0.00	0.79	0.79	0.79	0.00
t_f	Output Fall Time, TDO	0.39	0.39	0.39	0.00	0.49	0.49	0.49	0.00
		OSCPHBJ				**OSCPHBLJ**			
t_{PLH}	Propagation Delay, CKDR to TDO	0.68	0.68	0.68	0.00	1.01	1.01	1.01	0.00
t_{PHL}		0.71	0.71	0.71	0.00	0.98	0.98	0.98	0.00
t_{PLH}	Propagation Delay, PADI to DI	2.65	2.66	2.67	0.04	3.64	3.65	3.66	0.05
t_{PHL}		4.14	4.15	4.17	0.06	5.63	5.64	5.65	0.05
t_r	Output Rise Time, DI	2.05	2.06	2.07	0.05	0.34	0.38	0.49	0.37
t_f	Output Fall Time, DI	2.22	2.23	2.24	0.05	0.30	0.33	0.42	0.30
t_r	Output Rise Time, TDO	0.58	0.58	0.58	0.00	0.79	0.79	0.79	0.00
t_f	Output Fall Time, TDO	0.39	0.39	0.39	0.00	0.49	0.49	0.49	0.00
		OSCPSBJ				**OSCPSBLJ**			
t_{PLH}	Propagation Delay, CKDR to TDO	0.68	0.68	0.68	0.00	1.01	1.01	1.01	0.00
t_{PHL}		0.71	0.71	0.71	0.00	0.98	0.98	0.98	0.00
t_{PLH}	Propagation Delay, PADI to DI	3.42	3.43	3.44	0.05	4.72	4.73	4.75	0.07
t_{PHL}		4.90	4.90	4.92	0.06	7.17	7.17	7.18	0.04
t_r	Output Rise Time, DI	2.05	2.06	2.07	0.05	0.34	0.38	0.49	0.37
t_f	Output Fall Time, DI	2.30	2.30	2.32	0.05	0.30	0.33	0.42	0.30
t_r	Output Rise Time, TDO	0.58	0.58	0.58	0.00	0.79	0.79	0.79	0.00
t_f	Output Fall Time, TDO	0.39	0.39	0.39	0.00	0.49	0.49	0.49	0.00

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		pF=0	pF=50	pF=100	K (ns/pF)	pF=0	pF=50	pF=100	K (ns/pF)
		OSCPBJ				OSCPBLJ			
t_{PLH}	Propagation Delay,	1.61	2.66	3.71	0.02	2.10	3.60	5.10	0.03
t_{PHL}	PADI to PADO	1.91	3.01	4.11	0.02	2.55	3.35	4.15	0.02
t_r	Output Rise Time, PADO	2.32	4.72	7.12	0.05	0.00	36.35	72.70	0.73
t_f	Output Fall Time, PADO	2.59	5.24	7.89	0.05	13.65	19.33	25.00	0.11
		OSCPHBJ				OSCPHBLJ			
t_{PLH}	Propagation Delay,	1.61	2.66	3.71	0.02	2.10	3.60	5.10	0.03
t_{PHL}	PADI to PADO	1.92	3.02	4.12	0.02	2.56	3.36	4.16	0.02
t_r	Output Rise Time, PADO	2.34	4.74	7.14	0.05	0.00	36.35	72.70	0.73
t_f	Output Fall Time, PADO	2.60	5.25	7.90	0.05	13.69	19.34	25.00	0.11
		OSCPSBJ				OSCPSBLJ			
t_{PLH}	Propagation Delay,	1.61	2.66	3.71	0.02	2.10	3.60	5.10	0.03
t_{PHL}	PADI to PADO	1.92	3.02	4.12	0.02	2.56	3.36	4.16	0.02
t_r	Output Rise Time, PADO	2.34	4.74	7.14	0.05	0.00	36.35	72.70	0.73
t_f	Output Fall Time, PADO	2.59	5.24	7.89	0.05	13.67	19.34	25.00	0.11

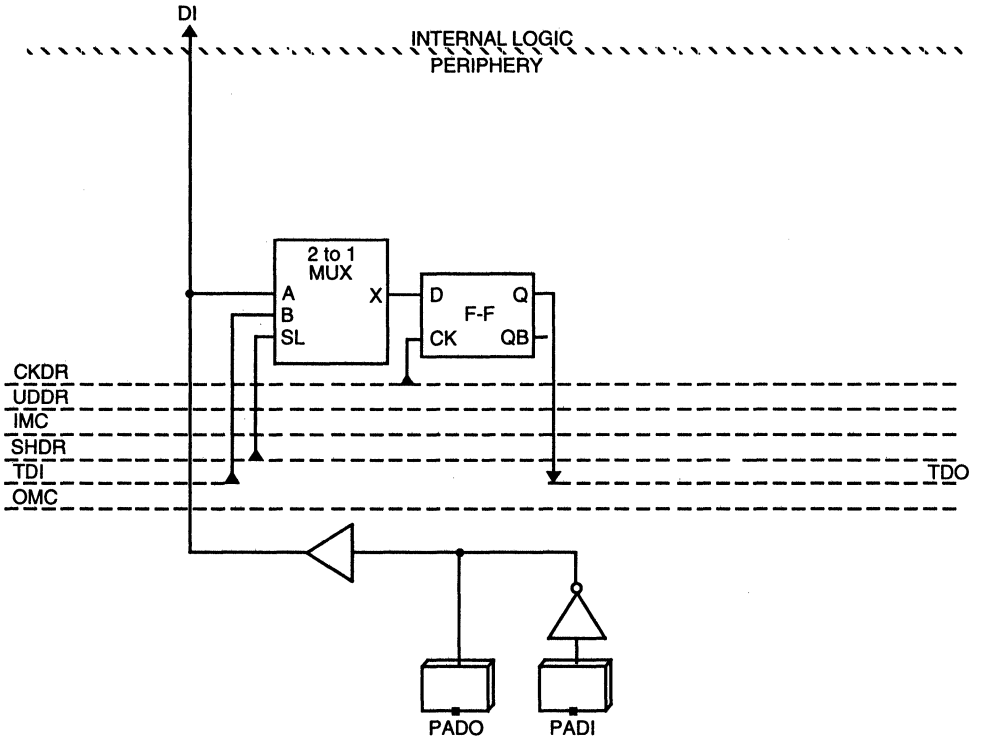
Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
		OSCPBJ	OSCPBLJ
t_{su}	Set Up Time, DI to CKDR	2.89	3.67
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.44
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26
t_h	Hold Time, CKDR to DI	-2.08	-2.75
t_h	Hold Time, CKDR to SHDR	0.19	0.25
t_h	Hold Time, CKDR to TDI	0.31	0.41
t_w	Pulse Width, CKDR(L)	0.45	0.71
t_w	Pulse Width, CKDR(H)	0.65	0.98
		OSCPHBJ	OSCPHBLJ
t_{su}	Set Up Time, DI to CKDR	3.19	3.89
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.43
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26
t_h	Hold Time, CKDR to DI	-1.77	-2.49
t_h	Hold Time, CKDR to SHDR	0.19	0.25
t_h	Hold Time, CKDR to TDI	0.31	0.41
t_w	Pulse Width, CKDR(L)	0.45	0.71
t_w	Pulse Width, CKDR(H)	0.65	0.98
		OSCPSBJ	OSCPSBLJ
t_{su}	Set Up Time, DI to CKDR	3.80	4.80
t_{su}	Set Up Time, SHDR to CKDR	0.25	0.42
t_{su}	Set Up Time, TDI to CKDR	0.13	0.26
t_h	Hold Time, CKDR to DI	-2.73	-3.76
t_h	Hold Time, CKDR to SHDR	0.19	0.25
t_h	Hold Time, CKDR to TDI	0.31	0.41
t_w	Pulse Width, CKDR(L)	0.45	0.71
t_w	Pulse Width, CKDR(H)	0.65	0.98

FUNCTIONAL DIAGRAM: OSCPBJ



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Section 7.3.5 Miscellaneous Boundary-Scan Macros -JTAG

Boundry Scan Cell Clock Driver - JTAG (Unused I/O or Pwr/Gnd Site) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V **CKDRMID**

MACRO	EQUIV. GATES
CKDRMID	0

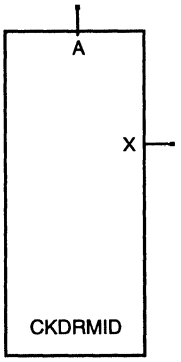
Rev. 1.07

MACRO	OUTPUTS/INPUTS
CKDRMID	X / A

MACRO	INPUT CAP.
CKDRMID	A: 0.20pF

FUNCTION TABLE

JTAG	
A	X
L	L
H	H



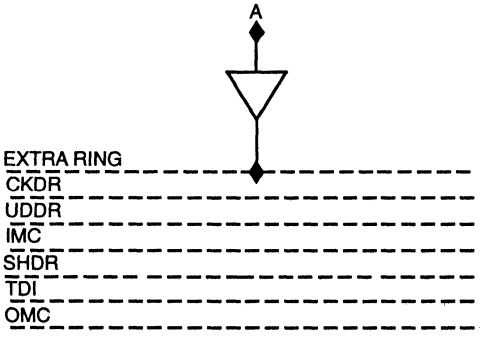
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
CKDRMID									
t_{PLH}	Propagation Delay, A to X	0.48	0.48	0.50	0.07	0.65	0.66	0.69	0.10
t_{PHL}		0.44	0.45	0.47	0.07	0.55	0.55	0.58	0.09
t_r	Output Rise Time, X	0.43	0.44	0.48	0.13	0.61	0.62	0.67	0.17
t_f	Output Fall Time, X	0.26	0.27	0.31	0.11	0.26	0.27	0.31	0.13

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: CKDRMID



Boundry Scan Cell Clock Driver - JTAG (Unused I/O or Pwr/Gnd Site) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V **CKDRCC1**

MACRO	EQUIV. GATES
CKDRCC1	0

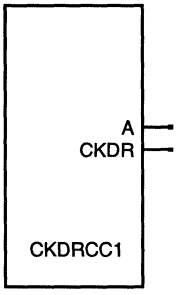
Rev. 1.07

MACRO	OUTPUTS/INPUTS
CKDRCC1	CKDR / A

MACRO	INPUT CAP.
CKDRCC1	A: 0.21pF

FUNCTION TABLE

JTAG	
A	CKDR
L	L
H	H



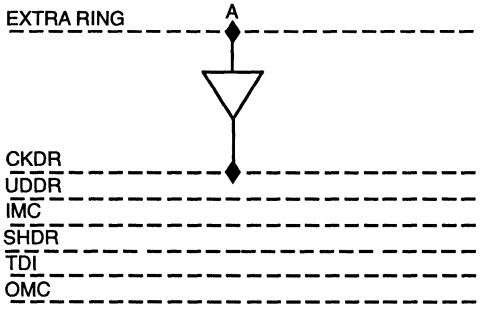
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
CKDRCC1									
t_{PLH}	Propagation Delay, A to CKDR	0.48	0.48	0.50	0.07	0.65	0.66	0.69	0.10
t_{PHL}		0.44	0.45	0.47	0.07	0.55	0.55	0.58	0.09
t_r	Output Rise Time, CKDR	0.43	0.44	0.48	0.13	0.61	0.62	0.67	0.17
t_f	Output Fall Time, CKDR	0.26	0.27	0.31	0.11	0.26	0.27	0.31	0.13

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: CKDRCC1



Boundry Scan Cell Clock Driver - JTAG (Unused I/O or Pwr/Gnd Site) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V **CKDRCC2**

MACRO	EQUIV. GATES
CKDRCC2	0

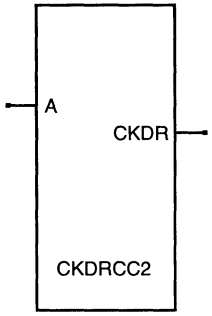
Rev. 1.07

MACRO	OUTPUTS/INPUTS
CKDRCC2	CKDR / A

MACRO	INPUT CAP.
CKDRCC2	A: 0.21pF

FUNCTION TABLE

JTAG	
A	CKDR
L	L
H	H



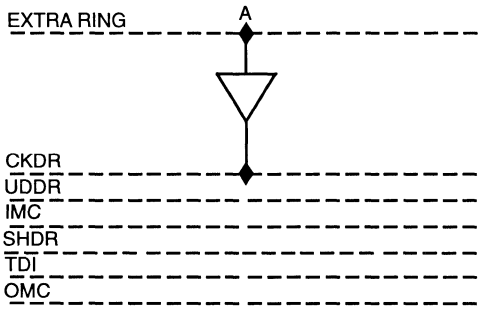
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
CKDRCC2									
t_{PLH}	Propagation Delay, A to CKDR	0.48	0.48	0.50	0.07	0.65	0.66	0.69	0.10
t_{PHL}		0.44	0.45	0.47	0.07	0.55	0.55	0.58	0.09
t_r	Output Rise Time, CKDR	0.43	0.44	0.48	0.13	0.61	0.62	0.67	0.17
t_f	Output Fall Time, CKDR	0.26	0.27	0.31	0.11	0.26	0.27	0.31	0.13

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: CKFRCC2



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Boundry Scan Cell Input Mode Control Driver - JTAG (Unused I/O or Pwr/Gnd Site) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V **IMCDR**

MACRO	EQUIV. GATES
IMCDR	0

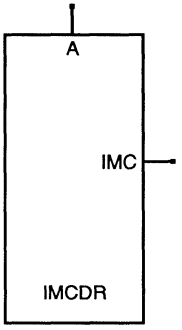
Rev. 1.07

MACRO	OUTPUTS/INPUTS
IMCDR	IMC / A

MACRO	INPUT CAP.
IMCDR	A: 0.20pF

FUNCTION TABLE

JTAG	
A	IMC
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	IMCDR								
t_{PLH}	Propagation Delay, A to IMC	0.48	0.48	0.50	0.07	0.65	0.66	0.69	0.10
t_{PHL}		0.44	0.45	0.47	0.07	0.55	0.55	0.58	0.09
t_r	Output Rise Time, IMC	0.43	0.44	0.48	0.13	0.61	0.62	0.67	0.17
t_f	Output Fall Time, IMC	0.26	0.27	0.31	0.11	0.26	0.27	0.31	0.13

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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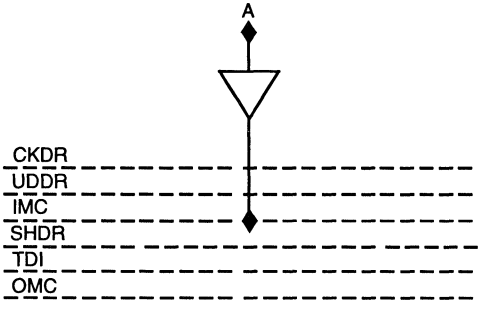
FUNCTIONAL DIAGRAM: IMCDR



Boundry Scan Cell Output Mode Control Driver - JTAG (Unused I/O or Pwr/Gnd Site) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V

OMCDR

MACRO	EQUIV. GATES
OMCDR	0

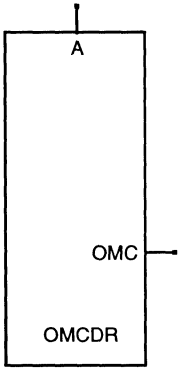
Rev. 1.07

MACRO	OUTPUTS/INPUTS
OMCDR	OMC / A

MACRO	INPUT CAP.
OMCDR	A: 0.20pF

FUNCTION TABLE

JTAG	
A	OMC
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
OMCDR									
t_{PLH}	Propagation Delay, A to OMC	0.48	0.48	0.50	0.07	0.65	0.66	0.69	0.10
t_{PHL}		0.44	0.45	0.47	0.07	0.55	0.55	0.58	0.09
t_r	Output Rise Time, OMC	0.43	0.44	0.48	0.13	0.61	0.62	0.67	0.17
t_f	Output Fall Time, OMC	0.26	0.27	0.31	0.11	0.26	0.27	0.31	0.13

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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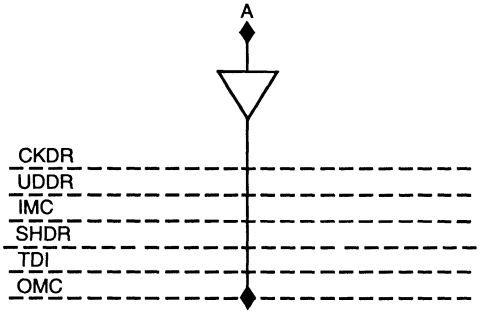
FUNCTIONAL DIAGRAM: OMCDR



Clock Net ISO and Test Data Resync- JTAG (Unused I/O or Output Pwr/Gnd Site) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V

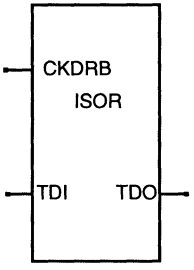
ISOR

MACRO	SECTIONS USED
ISOR	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
ISOR	TDO / CKDRB,TDI

MACRO	INPUT CAP.
ISOR	CKDR,TDI: 0.04pF



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
ISOR									
t_{PLH}	Propagation Delay, CKDRB to TDO	0.60	0.60	0.60	0.00	0.88	0.88	0.88	0.00
t_{PHL}		0.71	0.71	0.71	0.00	1.01	1.01	1.01	0.00
t_r	Output Rise Time, TDO	0.58	0.58	0.58	0.00	0.79	0.79	0.79	0.00
t_f	Output Fall Time, TDO	0.38	0.38	0.38	0.00	0.50	0.50	0.50	0.00

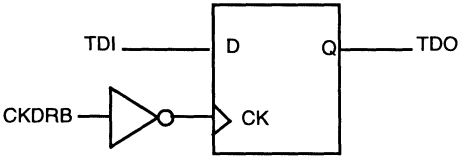
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns)

Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
ISOR			
t_{su}	Set Up Time, TDI to CKDRB	0.11	0.20
t_h	Hold Time, CKDRB to TDI	0.36	0.49
t_w	Pulse Width, CKDRB(L)	0.40	0.64
t_w	Pulse Width, CKDRB(H)	0.62	0.92

FUNCTIONAL DIAGRAM: ISOR



Boundry Scan Cell Shift Driver - JTAG (Unused I/O or Pwr/Gnd Site) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V **SHDR**

MACRO	EQUIV. GATES
SHDR	0

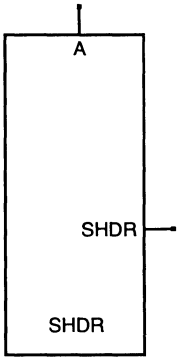
Rev. 1.07

MACRO	OUTPUTS/INPUTS
SHDR	SHDR / A

MACRO	INPUT CAP.
SHDR	A: 0.20pF

FUNCTION TABLE

JTAG	
A	SHDR
L	L
H	H



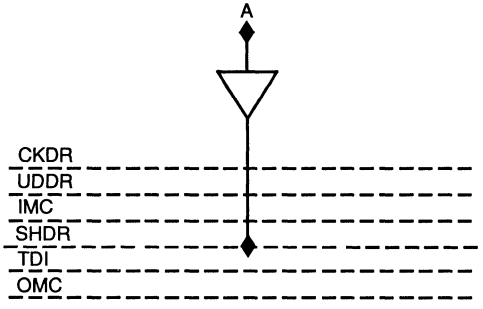
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	SHDR								
t_{PLH}	Propagation Delay, A to SHDR	0.48	0.48	0.50	0.07	0.65	0.66	0.69	0.10
t_{PHL}		0.44	0.45	0.47	0.07	0.55	0.55	0.58	0.09
t_r	Output Rise Time, SHDR	0.43	0.44	0.48	0.13	0.61	0.62	0.67	0.17
t_f	Output Fall Time, SHDR	0.26	0.27	0.31	0.11	0.26	0.27	0.31	0.13

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: SHDR



7

B - S Register Test Data Buffer (Unused I/O or Output Pwr/Gnd Site) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V

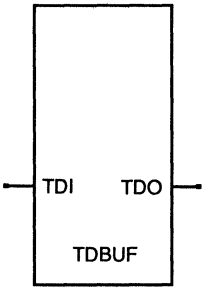
TDBUF

MACRO	EQUIV. GATES
TDBUF	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
TDBUF	TDO / TDI

MACRO	INPUT CAP.
TDBUF	TDI: 0.11pF



CMOS SWITCHING CHARACTERISTICS

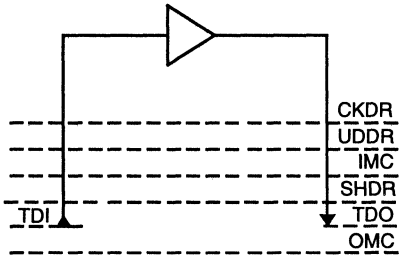
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	TDBUF								
t_{PLH}	Propagation Delay,	0.32	0.33	0.37	0.11	0.41	0.43	0.47	0.15
t_{PHL}	TDI to TDO	0.33	0.34	0.39	0.15	0.45	0.47	0.53	0.19
t_r	Output Rise Time, TDO	0.13	0.15	0.23	0.25	0.17	0.21	0.31	0.35
t_f	Output Fall Time, TDO	0.13	0.15	0.21	0.20	0.15	0.17	0.25	0.25

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: TDBUF



Boundry Scan Cell Update Driver - JTAG (Unused I/O or Pwr/Gnd Site) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V

UDDR

MACRO	EQUIV. GATES
UDDR	0

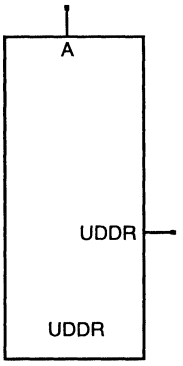
Rev. 1.07

MACRO	OUTPUTS/INPUTS
UDDR	UDDR / A

MACRO	INPUT CAP.
UDDR	A: 0.20pF

FUNCTION TABLE

JTAG	
A	UDDR
L	L
H	H



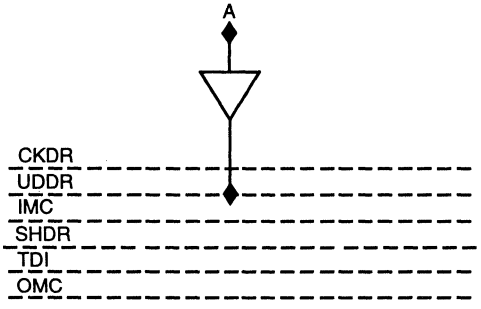
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	UDDR								
t_{PLH}	Propagation Delay, A to UDDR	0.48	0.48	0.50	0.07	0.65	0.66	0.69	0.10
t_{PHL}		0.44	0.45	0.47	0.07	0.55	0.55	0.58	0.09
t_r	Output Rise Time, UDDR	0.43	0.44	0.48	0.13	0.61	0.62	0.67	0.17
t_f	Output Fall Time, UDDR	0.26	0.27	0.31	0.11	0.26	0.27	0.31	0.13

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: UDDR



7

Enable Scan Macro - JTAG (Unused I/O or Output Pwr/Gnd Site) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V **ENSCANJ**

MACRO	EQUIV. GATES
ENSCANJ	0

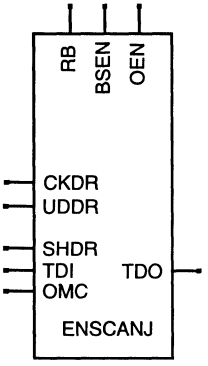
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ENSCANJ	OEN,TDO / BSEN,RB,CKDR,UDDR, SHDR,TDI,OMC

MACRO	INPUT CAP.
ENSCANJ	BSEN: 0.12pF CKDR,TDI: 0.04pF OMC,SHDR: 0.10pF RB: 0.02pF UDDR: 0.08pF

FUNCTION TABLE

JTAG
For JTAG Truth Table Information, See Table 7-7 "JTAG Logic Truth Tables - Enable Scan" on page 7-184 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	ENSCANJ								
t_{PLH}	Propagation Delay, BSEN to OEN	0.46	0.47	0.51	0.10	0.59	0.61	0.66	0.16
t_{PHL}		0.30	0.31	0.36	0.14	0.46	0.47	0.53	0.19
t_{PLH}	Propagation Delay, CKDR to TDO	0.58	0.58	0.58	0.00	0.85	0.85	0.85	0.00
t_{PHL}		0.60	0.60	0.60	0.00	0.87	0.87	0.87	0.00
t_{PLH}	Propagation Delay, OMC to OEN	0.77	0.79	0.82	0.12	1.08	1.10	1.15	0.17
t_{PHL}		0.58	0.60	0.64	0.15	0.75	0.77	0.83	0.19
t_{PHL}	Propagation Delay, RB to OEN	0.79	0.81	0.85	0.15	1.11	1.13	1.19	0.19
t_{PLH}	Propagation Delay, TDO to OEN	1.13	1.14	1.17	0.11	1.69	1.71	1.76	0.16
t_{PHL}		0.88	0.90	0.94	0.15	1.32	1.33	1.39	0.18
t_{PLH}	Propagation Delay, UDDR to OEN	1.22	1.23	1.27	0.13	1.78	1.79	1.84	0.16
t_{PHL}		1.04	1.05	1.10	0.15	1.49	1.51	1.56	0.18
t_r	Output Rise Time, OEN	0.21	0.24	0.31	0.25	0.24	0.28	0.38	0.34
t_f	Output Fall Time, OEN	0.15	0.17	0.23	0.21	0.23	0.26	0.33	0.25
t_r	Output Rise Time, TDO	0.22	0.22	0.22	0.00	0.31	0.31	0.31	0.00
t_f	Output Fall Time, TDO	0.20	0.20	0.20	0.00	0.25	0.25	0.25	0.00

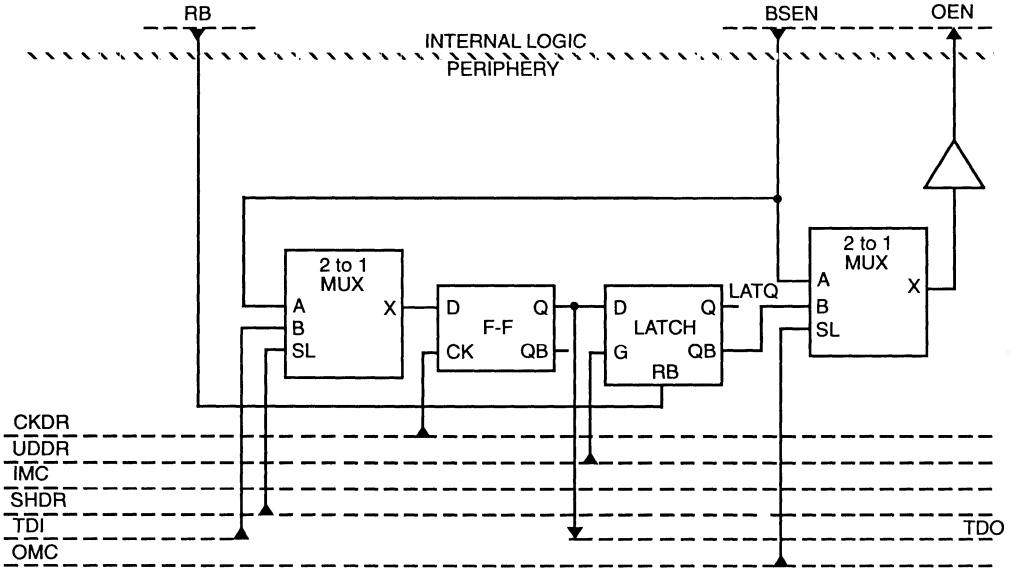
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
	ENSCANJ		
t_{su}	Set Up Time, BSEN to CKDR	0.23	0.37
t_{su}	Set Up Time, SHDR to CKDR	0.23	0.43
t_{su}	Set Up Time, TDI to CKDR	0.14	0.26
t_h	Hold Time, CKDR to BSEN	0.37	0.47
t_h	Hold Time, CKDR to SHDR	0.12	0.20
t_h	Hold Time, CKDR to TDI	0.30	0.41
t_{rec}	Recovery Time, RB to UDDR	0.31	0.34
t_w	Pulse Width, CKDR(L)	0.42	0.69
t_w	Pulse Width, CKDR(H)	0.74	1.12
t_w	Pulse Width, RB(L)	0.27	0.42
t_w	Pulse Width, UDDR(H)	0.47	0.66

FUNCTIONAL DIAGRAM: ENSCANJ



7

Section 7.3.6 Control Macros-JTAG

Bypass Register - JTAG (Internal) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V **BPREG**

MACRO	EQUIV. GATES
BPREG	10

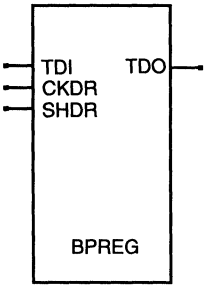
Rev. 1.07

MACRO	OUTPUTS/INPUTS
BPREG	TDO / TDI,CKDR,SHDR

MACRO	INPUT CAP.
BPREG	CKDR,SHDR,TDI: 0.05pF

FUNCTION TABLE

INPUT			OUTPUT
TDI	CKDR	SHDR	TDO
X	↓	L	L
X	↓	L	L
L	↓	H	L
H	↓	H	H
X	↑	X	TDO



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	BPREG								
t_{PLH}	Propagation Delay,	0.88	0.96	1.21	0.82	1.24	1.35	1.70	1.16
t_{PHL}	CKDR to TDO	0.98	1.06	1.29	0.77	1.42	1.51	1.79	0.93
t_r	Output Rise Time, TDO	0.15	0.40	1.13	2.43	0.21	0.55	1.59	3.44
t_f	Output Fall Time, TDO	0.14	0.26	0.61	1.18	0.21	0.36	0.78	1.41

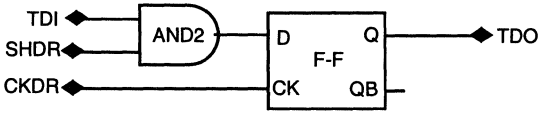
Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
	BPREG		
t_{su}	Set Up Time, SHDR to CKDR	0.59	0.89
t_{su}	Set Up Time, ,TDI to CKDR	0.59	0.86
t_h	Hold Time, CKDR to SHDR	-0.04	-0.07
t_h	Hold Time, CKDR to TDI	0.06	0.03
t_w	Pulse Width, CKDR(L)	0.61	0.96
t_w	Pulse Width, CKDR(H)	0.80	1.17

FUNCTIONAL DIAGRAM: BPREG



Enable Boundry Scan Macro - JTAG (Internal) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V **ENSCANI**

MACRO	EQUIV. GATES
ENSCANI	20

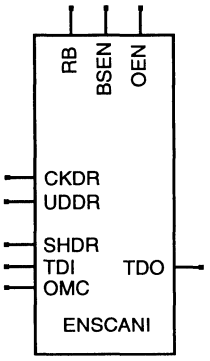
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ENSCANI	OEN,TDO / BSEN,RB,CKDR,UDDR,SHDR, TDI,OMC

MACRO	INPUT CAP.
ENSCANI	BSEN,OMC: 0.12pF CKDR,TDI,UDDR: 0.05pF RB: 0.07pF SHDR: 0.10pF

FUNCTION TABLE

JTAG
For JTAG Truth Table Information, See Table 7-7 JTAG Logic Truth Tables - Enable Scan on page 7-183 in this Manual.



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
ENSCANI									
t_{PLH}	Propagation Delay, BSEN to OEN	0.37	0.41	0.53	0.41	0.52	0.58	0.75	0.59
t_{PHL}		0.37	0.41	0.51	0.35	0.52	0.57	0.70	0.45
t_{PLH}	Propagation Delay, CKDR to TDO	0.89	0.97	1.22	0.83	1.26	1.38	1.73	1.17
t_{PHL}		0.98	1.05	1.26	0.70	1.40	1.49	1.75	0.87
t_{PLH}	Propagation Delay, OMC to OEN	0.46	0.50	0.63	0.42	0.64	0.70	0.87	0.58
t_{PHL}		0.57	0.61	0.72	0.36	0.81	0.85	0.98	0.45
t_{PHL}	Propagation Delay, RB to OEN	0.74	0.78	0.89	0.37	1.13	1.17	1.31	0.45
t_{PLH}	Propagation Delay, TDO to OEN	1.14	1.18	1.31	0.42	1.70	1.76	1.93	0.59
t_{PHL}		1.02	1.05	1.16	0.36	1.54	1.58	1.72	0.44
t_{PLH}	Propagation Delay, UDDR to OEN	1.27	1.31	1.44	0.42	1.85	1.91	2.08	0.59
t_{PHL}		1.21	1.24	1.35	0.35	1.76	1.81	1.94	0.45
t_r	Output Rise Time, OEN	0.13	0.25	0.61	1.22	0.18	0.35	0.86	1.72
t_f	Output Fall Time, OEN	0.15	0.20	0.36	0.54	0.20	0.26	0.46	0.66
t_r	Output Rise Time, TDO	0.31	0.56	1.30	2.46	0.42	0.76	1.81	3.47
t_f	Output Fall Time, TDO	0.21	0.32	0.65	1.11	0.27	0.40	0.81	1.36

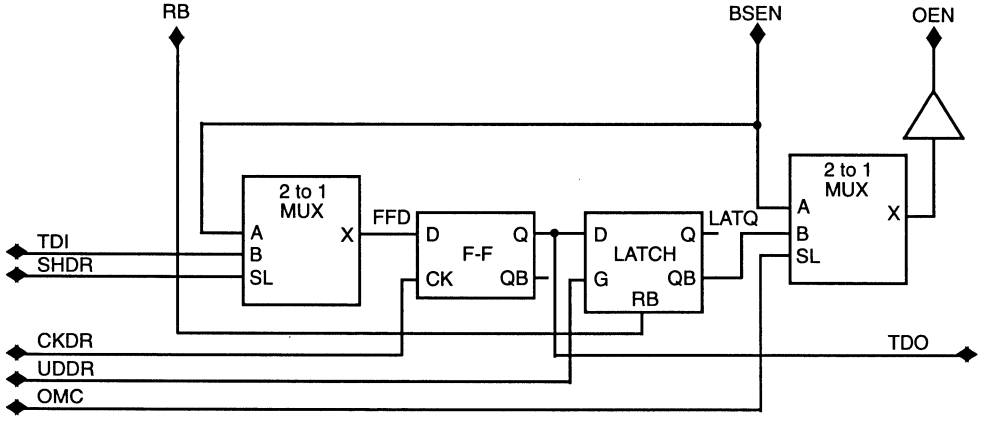
Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
	ENSCANI		
t_{su}	Set Up Time, BSEN to CKDR	0.57	0.88
t_{su}	Set Up Time, SHDR to CKDR	0.77	1.18
t_{su}	Set Up Time, TDI to CKDR	0.61	0.94
t_h	Hold Time, CKDR to BSEN	0.01	0.03
t_h	Hold Time, CKDR to SHDR	-0.17	-0.26
t_h	Hold Time, CKDR to TDI	-0.04	-0.06
t_{rec}	Recovery Time, RB to UDDR	0.66	0.96
t_w	Pulse Width, CKDR(L)	0.55	0.89
t_w	Pulse Width, CKDR(H)	0.73	1.10
t_w	Pulse Width, RB(L)	0.43	0.68
t_w	Pulse Width, UDDR(H)	0.76	1.13

FUNCTIONAL DIAGRAM: ENSCANI



Device Identification Register (32 bit) - JTAG (Internal) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V

IDREG

MACRO	EQUIV. GATES
IDREG	256

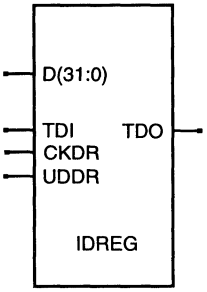
Rev. 1.07

MACRO	OUTPUTS/INPUTS
IDREG	TDO / D0-D9,D10-D19,D20-D29,D30,D31,TDI,CKDR,SHDR

MACRO	INPUT CAP.
IDREG	CKDR: 2.20pF D0,D1,D10-D19,D2,D20-D29,D3,D30,D31,D4-D9,TDI: 0.06pF SHDR: 4.03pF

FUNCTION TABLE

INPUT				OUTPUT
DX	CKDR	SHDR	TDI	TDO
-D0	↓	L	X	L
-D0	↓	L	X	H
X	↓	H	L	SHIFTED
X	↓	H	H	DATA
X	↑	X	X	TDO



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
IDREG									
t_{PLH}	Propagation Delay,	0.77	0.86	1.11	0.83	1.11	1.23	1.58	1.17
t_{PHL}	CKDR to TDO	0.77	0.84	1.06	0.72	1.10	1.19	1.47	0.91
t_r	Output Rise Time, TDO	0.30	0.54	1.27	2.44	0.42	0.76	1.79	3.44
t_f	Output Fall Time, TDO	0.28	0.39	0.72	1.09	0.38	0.51	0.91	1.33

Fanout (FO) capacitance does not include estimated metal lengths (each FO = 0.05pF).

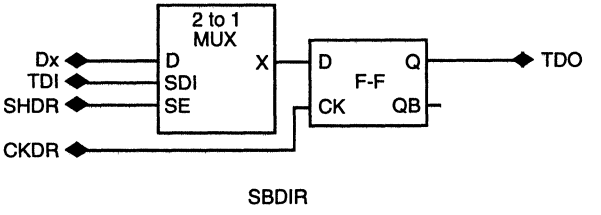
CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

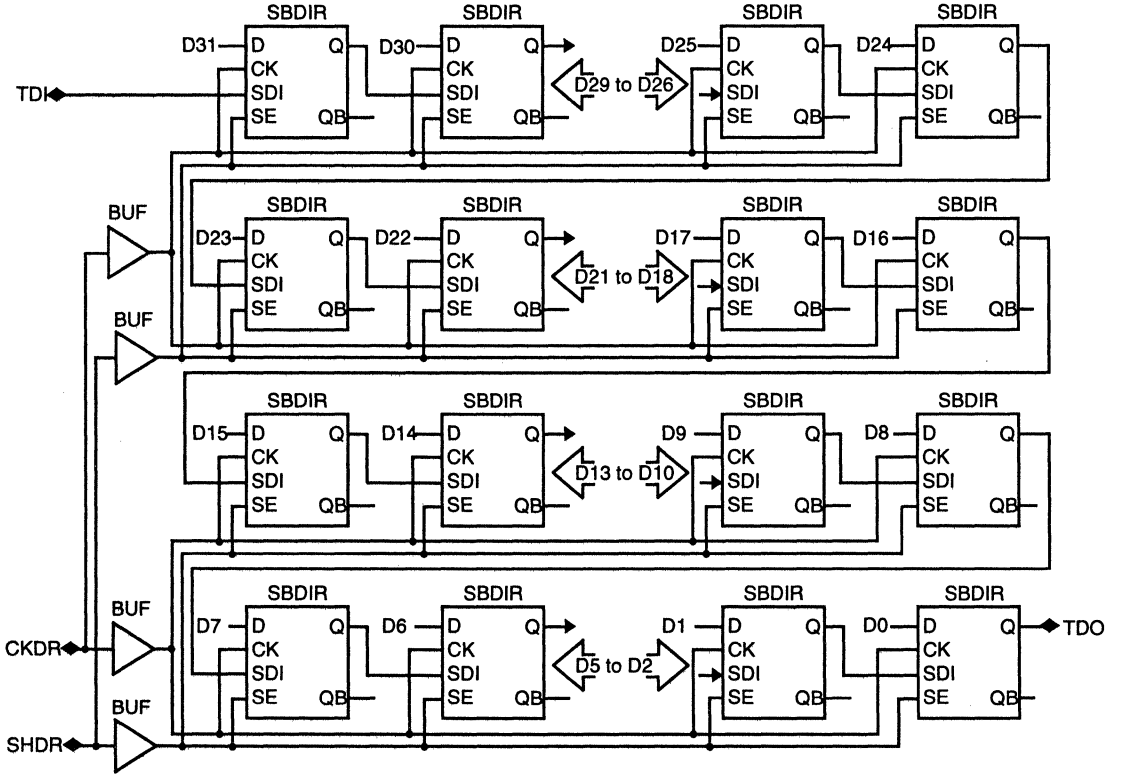
Sym	Parameter	5/5 V	3.3/3.3 V
		Minimum Requirement	Minimum Requirement
IDREG			
t_{su}	Set Up Time, SHDR to CKDR	0.38	0.62
t_{su}	Set Up Time, TDI to CKDR	0.19	0.41
t_h	Hold Time, CKDR to SHDR	0.21	0.30
t_h	Hold Time, CKDR to TDI	0.36	0.48
t_w	Pulse Width, CKDR(L)	0.54	0.86
t_w	Pulse Width, CKDR(H)	0.66	1.01

7

IDREG Building Block



FUNCTIONAL DIAGRAM: IDREG



32 STAGES

Instruction Register (1 Bit) - JTAG (Soft Macro) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V

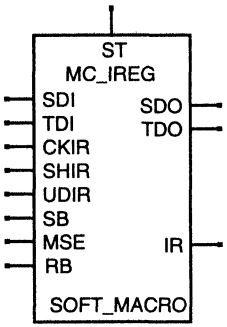
MC_IREG

MACRO	EQUIV. GATES
MC_IREG	25

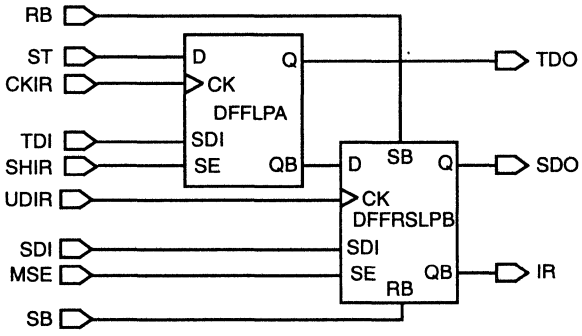
Rev. 1.07

MACRO	OUTPUTS/INPUTS
MC_IREG	SDO,TDO,IR/ SDI,TDI,CKIR,SHIR,UDIR,SB, MSE,RB,ST

MACRO	INPUT CAP.
MC_IREG	SDI,TDI,UDIR,ST: 0.05 pF SHIR,SB,MSE,RB: 0.09 pF CKIR: 0.14 pF



FUNCTIONAL DIAGRAM: MC_IREG



7

Instruction Register (4 Bit) - JTAG (Soft Macro) (3.3 V and 5 V System/Core Voltage)

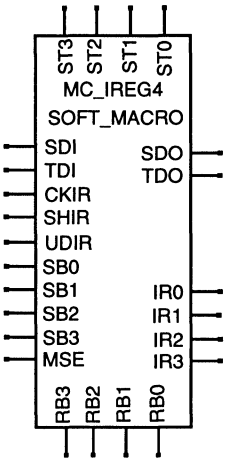
5/5 V / 3.3/3.3 V **MC_IREG4**

MACRO	EQUIV. GATES
MC_IREG4	124

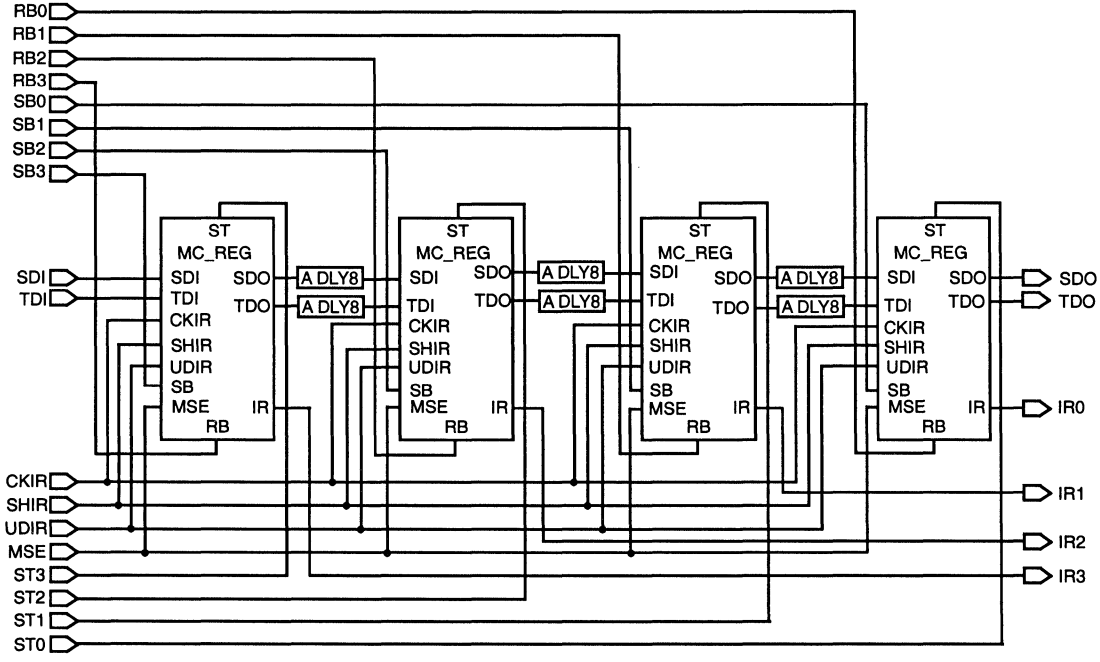
Rev. 1.07

MACRO	OUTPUTS/INPUTS
MC_IREG4	SDO,TDO,IR0-IR3/ SDI,TDI,CKIR,SHIR,UDIR, SB0-SB3,MSE,RBO-RB3,ST0-ST3

MACRO	INPUT CAP.
MC_IREG4	SDI,TDI,,ST0-ST3: 0.05 pF SB0-SB3,RB0-RB3: 0.09 pF CKIR: 0.56 pF SHIR,MSE: 0.36 pF UDIR 0.2 pF

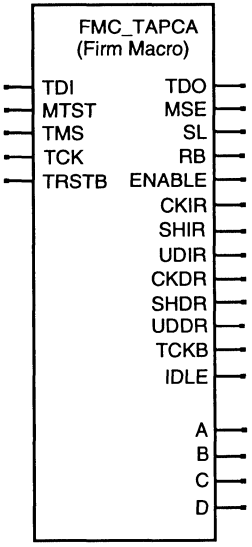


FUNCTIONAL DIAGRAM: MC_IREG4



TAP Controller - JTAG (Firm Macro) (3.3 V and 5 V System/Core Voltage)

5/5 V / 3.3/3.3 V FMC_TAPCA



MACRO	EQUIV. GATES
FMC_TAPC	276

Rev. 1.07

MACRO	OUTPUTS/INPUTS
FMC_TAPC	CKDR,CKIR,ENABLE,IDLE,MSE,RB,SHDR, SHIR,SL,TCKB,TDO,UDDR,UDIR,A-D / MTST,TCK,TDI,TMS,TRSTB

MACRO	INPUT CAP.
FMC_TAPC	MTST: 0.29pF TCK: 0.27pF TDI: 0.10pF TMS: 0.14pF TRSTB: 1.02pF

Note:
Placement is fixed and will have a direct effect on routing outcome.

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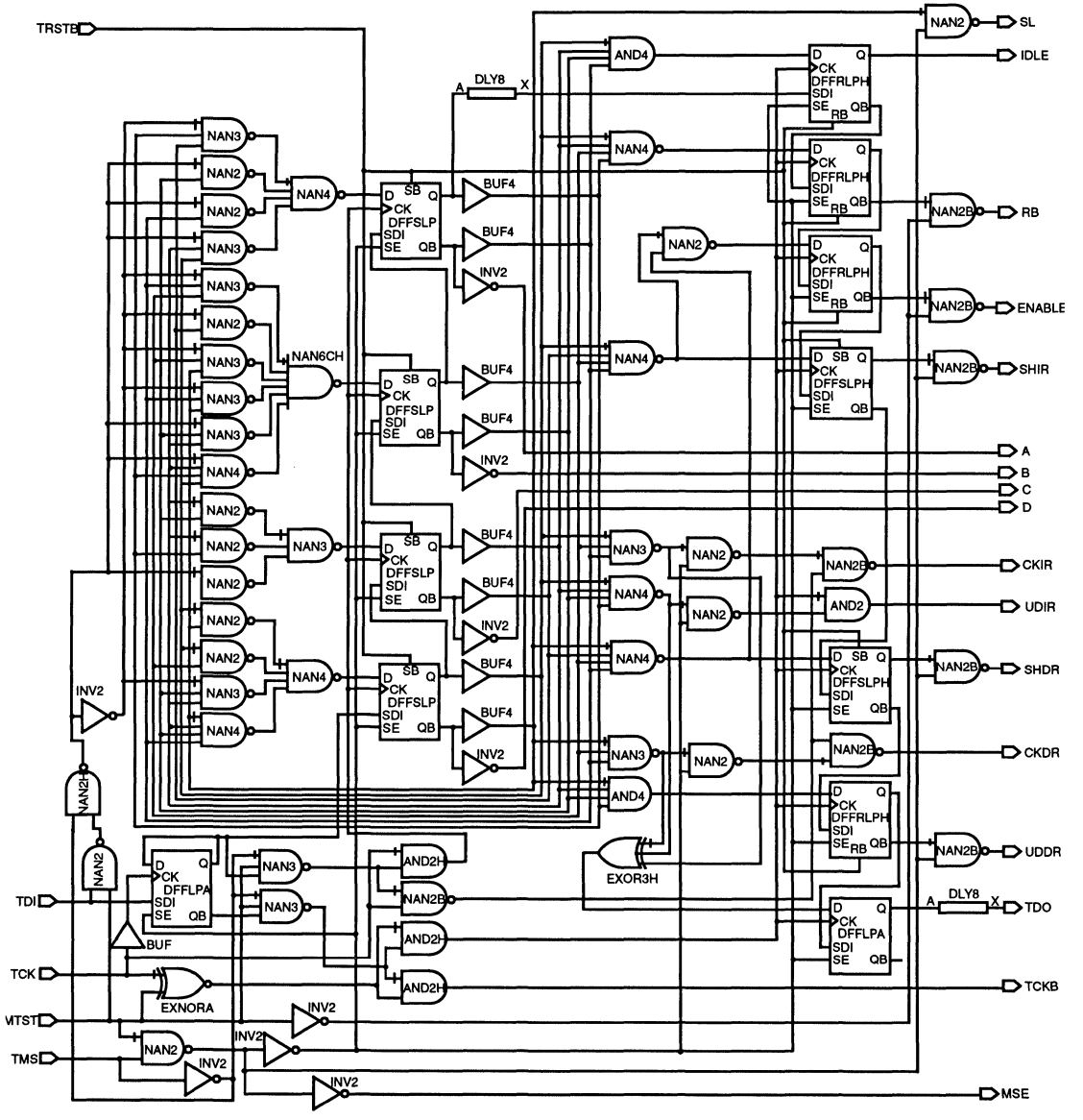
FUNCTIONAL DIAGRAM: FMC_TAPC



JTAG TRUTH TABLES

Table 7-1: JTAG Logic Truth Tables - Bidirectionals

JTAG BIDIRECTIONAL OPEN DRAIN BUFFERS												
TAPCTLR STATE	DO	LATQ	CKDR	UDDR	IMC	OMC	SHDR	ACTIVE PATHS			CLOCKED PATHS	TEST MODE *see Notes
IDLE	L	X	H	L	L	L	L	DO→ PAD	DO→FFD	PAD→DI		S1
CAPTURE	L	X	↓	L	L	L	L	DO→ PAD	DO→FFD	PAD→DI	DO→TDO	S1
SHIFT	L	X	↓	L	L	L	H	DO→ PAD	TDI→FFD	PAD→DI	TDI→TDO	S1
UPDATE	L	X	↑	H	L	L	L	DO→PAD	DO→FFD	PAD→DI	TDO→LATQ	S1
IDLE	X	L	H	L	H	H	L	LATQ→ PAD	DO→FFD	LATQ→DI		E,I,1
CAPTURE	X	L	↓	L	H	H	L	LATQ→ PAD	DO→FFD	LATQ→DI	PAD→TDO	E,I,1
SHIFT	X	L	↓	L	H	H	H	LATQ→ PAD	TDI→FFD	LATQ→DI	TDI→TDO	E,I,1
UPDATE	X	L	↑	H	H	H	L	LATQ→PAD	DO→FFD	LATQ→DI	TDO→PAD,DI	E,I,1
IDLE	H	X	H	L	L	L	L	PAD→DI	PAD→FFD			S,2
CAPTURE	H	X	↓	L	L	L	L	PAD→DI	PAD→FFD		PAD→TDO	S,2
SHIFT	H	X	↓	L	L	L	H	PAD→DI	TDI→FFD		TDI→TDO	S,2
UPDATE	H	X	↑	H	L	L	L	PAD→ DI	PAD→FFD		TDO→LATQ	S,2
IDLE	X	H	H	L	H	H	L	LATQ→DI	PAD→FFD			E,I,2
CAPTURE	X	H	↓	L	H	H	L	LATQ→DI	PAD→FFD		PAD→TDO	E,I,2
SHIFT	X	H	↓	L	H	H	H	LATQ→DI	TDI→FFD		TDI→TDO	E,I,2
UPDATE	X	H	↑	H	H	H	L	LATQ→DI	PAD→FFD		TDO→DI	E,I,2

Table 7-2: JTAG Logic Truth Tables - Bidirectionals

JTAG BIDIRECTIONAL TRI-STATE BUFFERS											
TAPCTLR STATE	EN	CKDR	UDDR	IMC	OMC	SHDR	ACTIVE PATHS			CLOCKED PATHS	TEST MODE *see Notes
IDLE	H	H	L	L	L	L	DO→PAD	DO→FFD	PAD→DI		S1
CAPTURE	H	↓	L	L	L	L	DO→PAD	DO→FFD	PAD→DI	DO→TDO	S1
SHIFT	H	↓	L	L	L	H	DO→PAD	TDI→FFD	PAD→DI	TDI→TDO	S1
UPDATE	H	↑	H	L	L	L	DO→PAD	DO→FFD	PAD→DI		S1
IDLE	H	H	L	H	H	L	LATQ→PAD	DO→FFD	LATQ→DI		E,I,1
CAPTURE	H	↓	L	H	H	L	LATQ→PAD	DO→FFD	LATQ→DI	DO→TDO	E,I,1
SHIFT	H	↓	L	H	H	H	LATQ→PAD	TDI→FFD	LATQ→DI	TDI→TDO	E,I,1
UPDATE	H	↑	H	H	H	L	LATQ→PAD	DO→FFD	LATQ→DI	TDO→PAD,DI	E,I,1
IDLE	L	H	L	L	L	L	PAD→DI	PAD→FFD			S,2
CAPTURE	L	↓	L	L	L	L	PAD→DI	PAD→FFD		PAD→TDO	S,2
SHIFT	L	↓	L	L	L	H	PAD→DI	TDI→FFD		TDI→TDO	S,2
UPDATE	L	↑	H	L	L	L	PAD→DI	PAD→FFD			S,2
IDLE	L	H	L	H	H	L	LATQ→DI	PAD→FFD			E,I,2
CAPTURE	L	↓	L	H	H	L	LATQ→DI	PAD→FFD		PAD→TDO	E,I,2
SHIFT	L	↓	L	H	H	H	LATQ→DI	TDI→FFD		TDI→TDO	E,I,2
UPDATE	L	↑	H	H	H	L	LATQ→DI	PAD→FFD		TDO→DI	E,I,2

NOTES FOR ALL JTAG LOGIC TRUTH TABLES:

E = EXTEST; **S** = SAMPLE; **I** = INTEST

1. = Output is enabled and the JTAG boundary scan cell is monitoring the output signal. (DO)
2. = Output is disabled and the JTAG boundary scan cell is monitoring the input signal. (PAD)

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Table 7-3: JTAG Logic Truth Tables - Inputs

NON-INVERTING CMOS and TTL INPUTS								
TAPCTLR STATE	CKDR	UDDR	IMC	SHDR	ACTIVE PATHS		CLOCKED PATHS	TEST MODE *see Notes
IDLE	H	L	L	L	PAD→DI	PAD→FFD		S
CAPTURE	↗	L	L	L	PAD→DI	PAD→FFD	DO→TDO	S
SHIFT	↗	L	L	H	PAD→DI	TDI→FFD	TDI→TDO	S
UPDATE	↘	H	L	L	PAD→DI	PAD→FFD		S
IDLE	H	L	H	L	LATQ→DI	PAD→FFD		E,I
CAPTURE	↗	L	H	L	LATQ→DI	PAD→FFD	PAD→TDO	E,I
SHIFT	↗	L	H	H	LATQ→DI	TDI→FFD	TDI→TDO	E,I
UPDATE	↘	H	H	L	LATQ→DI	PAD→FFD	TDO→DI	E,I
* FOR MACRO ICNJA ONLY								

Table 7-4: JTAG Logic Truth Tables - Outputs

STANDARD/OPEN DRAIN OUTPUTS								
TAPCTLR STATE	CKDR	UDDR	OMC	SHDR	ACTIVE PATHS		CLOCKED PATHS	TEST MODE *see Notes
IDLE	H	L	L	L	DO→PAD	DO→FFD		S
CAPTURE	↗	L	L	L	DO→PAD	DO→FFD	DO→TDO	S
SHIFT	↗	L	L	H	DO→PAD	TDI→FFD	TDI→TDO	S
UPDATE	↘	H	L	L	DO→PAD	DO→FFD		S
IDLE	H	L	H	L	LATQ→PAD	DO→FFD		E,I
CAPTURE	↗	L	H	L	LATQ→PAD	DO→FFD	DO→TDO	E,I
SHIFT	↗	L	H	H	LATQ→PAD	TDI→FFD	TDI→TDO	E,I
UPDATE	↘	H	H	L	LATQ→PAD	DO→FFD	TDO→PAD	E,I

Table 7-5: JTAG Logic Truth Table - Clock/"Sample Only" Inputs

STANDARD/OPEN DRAIN OUTPUTS						
TAPCTLR STATE	CKDR	SHDR	ACTIVE PATHS		CLOCKED PATHS	TEST MODE *see Notes
IDLE	H	L	PAD→DI	PAD→FFD		S,E,I
CAPTURE	↗	L	PAD→DI	PAD→FFD	PAD→TDO	S,E,I
SHIFT	↗	H	PAD→DI	TDI→FFD	TDI→TDO	S,E,I

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NOTES FOR ALL JTAG LOGIC TRUTH TABLES:

E = EXTEST; **S** = SAMPLE; **I** = INTEST

1. = Output is enabled and the JTAG boundary scan cell is monitoring the output signal. (DO)
2. = Output is disabled and the JTAG boundary scan cell is monitoring the input signal. (PAD)

Table 7-6: JTAG Logic Truth Tables - Outputs

TRI-STATE OUTPUTS									
TAPCTLR STATE	EN	CKDR	UDDR	OMC	SHDR	ACTIVE PATHS		CLOCKED PATHS	TEST MODE *See Notes
IDLE	H	H	L	L	L	DO→PAD	DO→FFD		S
CAPTURE	H	↓	L	L	L	DO→PAD	DO→FFD	DO→ TDO	S
SHIFT	H	↓	L	L	H	DO→PAD	TDI→FFD	TDI→ TDO	S
UPDATE	H	↑	H	L	L	DO→PAD	DO→FFD		S
IDLE	L	H	L	L	L		DO→FFD		S
CAPTURE	L	↓	L	L	L		DO→FFD	DO→ TDO	S
SHIFT	L	↓	L	L	H		TDI→FFD	TDI→ TDO	S
UPDATE	L	↑	H	L	L		DO→FFD		S
IDLE	H	H	L	H	L	LATQ→PAD	DO→FFD		E,I
CAPTURE	H	↓	L	H	L	LATQ→PAD	DO→FFD	DO →TDO	E,I
SHIFT	H	↓	L	H	H	LATQ→PAD	TDI→FFD	TDI→ TDO	E,I
UPDATE	H	↑	H	H	L	LATQ→PAD	DO→FFD	TDO→ PAD	E,I
IDLE	L	H	L	H	L		DO→FFD		E,I
CAPTURE	L	↓	L	H	L		DO→FFD	DO→ TDO	E,I
SHIFT	L	↓	L	H	H		TDI→FFD	TDI→ TDO	E,I
UPDATE	L	↑	H	H	L		DO→FFD		E,I

Table 7-7: JTAG Logic Truth Tables - Enable Scan

ENABLE SCAN MACROS									
TAPCTLR STATE	RB	CKDR	UDDR	OMC	SHDR	ACTIVE PATHS		CLOCKED PATHS	TEST MODE *see Notes
IDLE	H	H	L	L	L	BSE→ OEN	BSEN→ FFD		S
CAPTURE	H	↓	L	L	L	BSEN→ OEN	BSEN→ FFD	BSEN→ TDO	S
SHIFT	H	↓	L	L	H	BSEN→ OEN	TDI→ FFD	TDI→ TDO	S
UPDATE	H	↑	H	L	L	BSEN→ OEN	BSEN→ FFD		S
IDLE	H	H	L	H	L	LATQ→ OEN	BSEN→ FFD		E,I
CAPTURE	H	↓	L	H	L	LATQ→ OEN	BSEN→ FFD	BSEN→ TDO	E,I
SHIFT	H	↓	L	H	H	LATQ→ OEN	TDI→ FFD	TDI→ TDO	E,I
UPDATE	H	↑	H	H	L	LATQ→ OEN	BSEN→ FFD	TDO→ OEN	E,I
RESET	L	H	L	H	L	LATQ→ OEN			E,I

NOTES FOR ALL JTAG LOGIC TRUTH TABLES:

E = EXTEST; **S** = SAMPLE; **I** = INTEST

1. = Output is enabled and the JTAG boundary scan cell is monitoring the output signal. (DO)
2. = Output is disabled and the JTAG boundary scan cell is monitoring the input signal. (PAD)

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Table 7-8: Tap Controller Truth Table

Current State		TAP Controller Outputs													Instruction RegisterState		TDO Output	
Name	Code-HEX	D	C	B	A	RB	SL	ENABLE	SHIR	CKIR	UDIR	SHDR	CKDR	UDDR	IDLE	Shift Register	Parallel Out	Register Selection	Buffer State
Exit2-DR	0	0	0	0	0	1	0	0	0	1	0	0	1	0	0	DC	IDCODE/ BYPASS	DC	Off
Exit1-DR	1	0	0	0	1	1	0	0	0	1	0	0	1	0	0	Parallel load	NC	Instruction	Off or On
Shift-DR	2	0	0	1	0	1	0	1	0	1	0	1	C	0	0	NC	Load from Shift Register	DC	Off
Pause-DR	3	0	0	1	1	1	0	0	0	1	0	0	1	0	0	DC	NC	DC	Off
Select-IR-Scan	4	0	1	0	0	1	0	0	0	1	0	0	1	0	0	NC	NC	Instruction	On
Update-DR	5	0	1	0	1	1	0	0	0	1	0	0	1	$\overline{C}$	0	Serial Shift	NC	Instruction	On
Capture-DR	6	0	1	1	0	1	0	0	0	1	0	0	C	0	0	NC	NC	Instruction	On
Select-DR-Scan	7	0	1	1	1	1	0	0	0	1	0	0	1	0	0	NC	NC	Instruction	On
Exit2-IR	8	1	0	0	0	1	1	0	0	1	0	0	1	0	0	DC	NC	DC	Off
Exit1-IR	9	1	0	0	1	1	1	0	0	1	0	0	1	0	0	DC	NC	Test Data	Off or On
Shift-IR	A	1	0	1	0	1	1	1	1	C	0	0	1	0	0	DC	NC	DC	Off
Pause-IR	B	1	0	1	1	1	1	0	0	1	0	0	1	0	0	DC	NC	DC	Off
Run-Test/Idle	C	1	1	0	0	1	1	0	0	1	0	0	1	0	1	DC	NC	Test Data	On
Update-IR	D	1	1	0	1	1	1	0	0	1	$\overline{C}$	0	1	0	0	DC	NC	Test Data	On
Capture-IR	E	1	1	1	0	1	1	0	0	C	0	0	1	0	0	DC	NC	Test Data	On
Test-Logic-Reset	F	1	1	1	1	1	1	0	0	1	0	0	1	0	1	DC	NC	Test Data	On
	F	1	1	1	1	0	1	0	1	1	0	1	1	0	0				

NOTES:

R, ENB, SHIR and SHDR change on the falling edge of TCK.

DC= Don't Care

NC = No Change (Retain Previous State)

For TAP Controller Outputs only, C = TCK Signal

For TAP Controller Outputs only, $\overline{C}$ = $\overline{TCK}$ Signal

State changes occur on rising edge of TCK

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7.4 Internal Cells (Gates)

4-Bit Full Adder
2X Drive
(3.3 V and 5 V Core Voltage)

AD4FULA

MACRO	EQUIV. GATES
AD4FULA	40

Rev.1.07

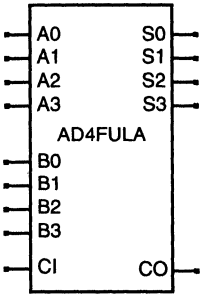
MACRO	OUTPUTS/INPUTS
AD4FULA	S0-S3,CO / A0-A3,B0-B3,CI

MACRO	INPUT CAP.
AD4FULA	A0-A3,CI: 0.11pF B0-B3: 0.05pF

FUNCTION TABLE

ADD WORD (A) TO WORD (B) +CARRY IN
(S0-S3) = (A0-A3)+(B0-B3)+CI
NOTE: A0,B0,S0 = LSB, A3,B3,S3= MSB

Faster CI to CO
Lower input Cap



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AD4FULA								
t_{PLH}	Propagation Delay, A0 to CO	2.95	2.99	3.12	0.42	4.00	4.06	4.24	0.60
t_{PHL}		2.30	2.34	2.48	0.46	3.47	3.53	3.70	0.58
t_{PLH}	Propagation Delay, A0 to S0 & A1 to S1 & A2 to S2 & A3 to S3	0.99	1.04	1.17	0.43	1.40	1.46	1.64	0.59
t_{PHL}		1.09	1.13	1.27	0.46	1.60	1.66	1.83	0.58
t_{PLH}	Propagation Delay, A0 to S1 & A1 to S2 & A2 to S3	1.45	1.49	1.62	0.43	2.04	2.10	2.28	0.60
t_{PHL}		1.03	1.07	1.20	0.44	1.52	1.58	1.74	0.56
t_{PLH}	Propagation Delay, A0 to S2 & A1 to S3	2.05	2.10	2.22	0.43	2.87	2.93	3.11	0.60
t_{PHL}		1.61	1.65	1.78	0.44	2.39	2.45	2.61	0.55
t_{PLH}	Propagation Delay, A0 to S3	2.24	2.28	2.41	0.43	3.03	3.09	3.27	0.60
t_{PHL}		2.73	2.78	2.91	0.44	4.11	4.17	4.33	0.55
t_{PLH}	Propagation Delay, A1 to CO	2.31	2.35	2.48	0.42	3.16	3.22	3.40	0.60
t_{PHL}		1.74	1.79	1.93	0.46	2.62	2.68	2.85	0.58
t_{PLH}	Propagation Delay, A2 to CO	1.69	1.73	1.86	0.42	2.32	2.38	2.56	0.60
t_{PHL}		1.17	1.22	1.35	0.45	1.75	1.80	1.98	0.58
t_{PLH}	Propagation Delay, A3 to CO	1.07	1.11	1.24	0.42	1.48	1.54	1.72	0.60
t_{PHL}		0.59	0.63	0.75	0.41	0.86	0.92	1.07	0.52
t_{PLH}	Propagation Delay, B0 to CO	3.07	3.12	3.24	0.42	4.19	4.25	4.43	0.60
t_{PHL}		2.97	3.02	3.15	0.45	4.44	4.50	4.67	0.58
t_{PLH}	Propagation Delay, B0 to S0 & B1 to S1 & B2 to S2 & B3 to S3	1.17	1.22	1.34	0.42	1.60	1.66	1.84	0.60
t_{PHL}		1.21	1.26	1.39	0.45	1.80	1.86	2.04	0.58
t_{PLH}	Propagation Delay, B0 to S1 & B1 to S2 & B2 to S3	1.77	1.82	1.94	0.42	2.54	2.60	2.78	0.60
t_{PHL}		1.71	1.76	1.89	0.44	2.51	2.57	2.73	0.56
t_{PLH}	Propagation Delay, B0 to S2 & B1 to S3	2.39	2.44	2.56	0.43	3.38	3.44	3.62	0.60
t_{PHL}		2.30	2.34	2.47	0.43	3.40	3.45	3.62	0.55
t_{PLH}	Propagation Delay, B0 to S3	3.03	3.07	3.20	0.43	4.23	4.29	4.47	0.60
t_{PHL}		2.85	2.90	3.03	0.44	4.27	4.32	4.49	0.55
t_{PLH}	Propagation Delay, B1 to CO	2.47	2.52	2.64	0.42	3.37	3.43	3.61	0.60
t_{PHL}		2.41	2.45	2.59	0.46	3.58	3.64	3.81	0.58

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

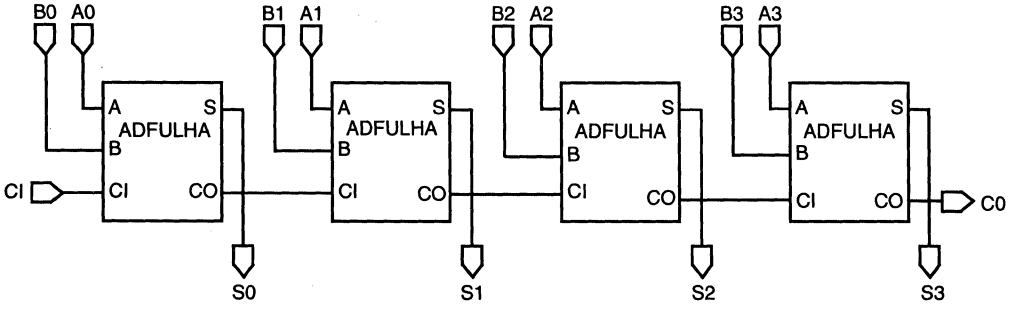
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay, B2 to CO	1.83	1.87	2.00	0.42	2.51	2.57	2.75	0.60
t_{PHL}		1.84	1.88	2.02	0.45	2.70	2.75	2.93	0.58
t_{PLH}	Propagation Delay, B3 to CO	1.21	1.26	1.38	0.42	1.66	1.72	1.90	0.60
t_{PHL}		1.26	1.30	1.43	0.43	1.83	1.88	2.05	0.55
t_{PLH}	Propagation Delay, CI to CO	2.52	2.56	2.69	0.42	3.36	3.42	3.61	0.60
t_{PHL}		2.30	2.35	2.48	0.46	3.53	3.59	3.76	0.58
t_{PLH}	Propagation Delay, CI to S0	0.42	0.46	0.59	0.43	0.57	0.63	0.81	0.60
t_{PHL}		0.48	0.53	0.66	0.43	0.68	0.74	0.91	0.55
t_{PLH}	Propagation Delay, CI to S1	1.05	1.09	1.22	0.43	1.42	1.48	1.66	0.60
t_{PHL}		1.04	1.09	1.22	0.44	1.58	1.64	1.80	0.55
t_{PLH}	Propagation Delay, CI to S2	1.68	1.72	1.85	0.43	2.26	2.32	2.50	0.60
t_{PHL}		1.61	1.65	1.78	0.44	2.45	2.50	2.67	0.55
t_{PLH}	Propagation Delay, CI to S3	2.30	2.35	2.47	0.43	3.11	3.17	3.35	0.60
t_{PHL}		2.17	2.22	2.35	0.44	3.32	3.37	3.54	0.56
t_r	Output Rise Time, CO,S0-S3	0.19	0.31	0.67	1.20				
t_f	Output Fall Time, CO,S0-S3	0.29	0.35	0.52	0.58				
t_r	Output Rise Time, CO					0.23	0.40	0.91	1.69
t_f	Output Fall Time, CO					0.39	0.47	0.68	0.71
t_r	Output Rise Time, S0-S3					0.26	0.43	0.94	1.69
t_f	Output Fall Time, S0-S3					0.37	0.44	0.66	0.71

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: AD4FULA



NOTE: See page 7-193 for the Functional Diagram for ADFULHA.

4-Bit Full Adder with Propagate & Generate 2X Drive (3.3 V and 5 V Core Voltage)

AD4PG

MACRO	EQUIV. GATES
AD4PG	94

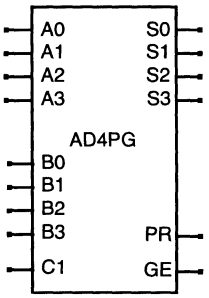
Rev. 1.07

MACRO	OUTPUTS/INPUTS
AD4PG	S0-S3,PR,GE / A0-A3,B0-B3,CI

MACRO	INPUT CAP.
AD4PG	A0-A3,B0-B3,CI: 0.10pF

FUNCTION TABLE

PROPAGATE (PROPAGATE THE CARRY BIT) PR= (A0+B0)(A1+B1)(A2+B2)(A3+B3)
GENERATE (GENERATE A CARRY BIT) GE= (A3*B3) + (A2*B2)(A3+B3) + (A1*B1)(A2+B2)(A3+B3) + (A0*B0)(A1+B1)(A2+B2)(A3+B3)
ADD WORD (A) TO WORD (B) +CARRY IN (S0-S3) = (A0-A3)+(B0-B3)+CI
NOTE: A0,B0,S0 = LSB, A3,B3,S3= MSB



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AD4PG								
t_{PLH}	Propagation Delay, A0 to GE	1.11	1.15	1.29	0.45	1.55	1.62	1.81	0.64
t_{PHL}		0.77	0.85	1.08	0.77	1.05	1.16	1.47	1.06
t_{PLH}	Propagation Delay, A0 to PR	1.12	1.16	1.30	0.45	1.53	1.59	1.78	0.64
t_{PHL}		0.88	0.92	1.04	0.40	1.25	1.30	1.44	0.49
t_{PLH}	Propagation Delay, A0,B0 to S0(INV=0),S0(INV=1)	1.32	1.36	1.50	0.45				
t_{PHL}		1.36	1.40	1.54	0.46				
t_{PLH}	Propagation Delay, A0 to S1(INV=0),S1(INV=1)	1.26	1.31	1.45	0.47				
t_{PHL}		1.21	1.26	1.41	0.50				
t_{PLH}	Propagation Delay, A0 to S2(INV=0),S2(INV=1)	1.82	1.87	2.02	0.48				
t_{PHL}		1.46	1.51	1.66	0.51				
t_{PLH}	Propagation Delay, A0 to S3(INV=0),S3(INV=1)	1.60	1.65	1.80	0.48				
t_{PHL}		1.63	1.68	1.83	0.50				
t_{PLH}	Propagation Delay, A0 to S0(INV=0)					1.83	1.89	2.08	0.64
t_{PHL}						1.96	2.02	2.20	0.58
t_{PLH}	Propagation Delay, A0 to S0(INV=1)					1.79	1.85	2.05	0.64
t_{PHL}						2.00	2.06	2.23	0.58
t_{PLH}	Propagation Delay, A0 to S1(INV=0)					1.78	1.84	2.05	0.68
t_{PHL}						1.80	1.87	2.06	0.66
t_{PLH}	Propagation Delay, A0 to S1(INV=1)					1.74	1.81	2.01	0.68
t_{PHL}						1.84	1.90	2.10	0.66
t_{PLH}	Propagation Delay, A0 to S2(INV=0) & B0 to S2(INV=1)					2.64	2.71	2.92	0.69
t_{PHL}						2.18	2.25	2.45	0.68
t_{PLH}	Propagation Delay, A0 to S2(INV=1)					2.60	2.67	2.88	0.69
t_{PHL}						2.22	2.29	2.49	0.68
t_{PLH}	Propagation Delay, A0 to S3(INV=0)					2.29	2.36	2.57	0.69
t_{PHL}						2.43	2.50	2.69	0.67
t_{PLH}	Propagation Delay, A0 to S3(INV=1)					2.25	2.32	2.53	0.69
t_{PHL}						2.47	2.54	2.73	0.67
t_{PLH}	Propagation Delay, A1 to GE	1.32	1.37	1.50	0.43	1.88	1.94	2.12	0.61
t_{PHL}		0.94	1.01	1.25	0.78	1.30	1.41	1.73	1.06
t_{PLH}	Propagation Delay, A1 to PR	1.02	1.06	1.20	0.44	1.40	1.47	1.66	0.64
t_{PHL}		0.82	0.86	0.98	0.40	1.17	1.21	1.36	0.49

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay,	1.63	1.68	1.82	0.47				
t_{PHL}	A1 to S1(INV=0),S1(INV=1)	1.75	1.80	1.96	0.52				
t_{PLH}	Propagation Delay,					2.26	2.33	2.53	0.68
t_{PHL}	A1 to S1(INV=0)					2.60	2.67	2.89	0.71
t_{PLH}	Propagation Delay,					2.23	2.30	2.50	0.68
t_{PHL}	A1 to S1(INV=1))					2.64	2.71	2.92	0.71
t_{PLH}	Propagation Delay,	2.02	2.07	2.21	0.48				
t_{PHL}	A1 to S2(INV=0)-S3(INV=1)	1.88	1.93	2.08	0.50				
t_{PLH}	Propagation Delay, A1 to S3(INV=0)	2.05	2.10	2.24	0.47				
t_{PHL}	& B1 to S2(INV=0),S2(INV=1)	1.85	1.90	2.05	0.51				
t_{PLH}	Propagation Delay, A1 to S2(INV=0),					2.90	2.97	3.17	0.68
t_{PHL}	S3(INV=1) & B1 to S2(INV=1					2.79	2.85	3.06	0.67
t_{PLH}	Propagation Delay,					2.86	2.93	3.14	0.68
t_{PHL}	A1 to S2(INV=1					2.83	2.89	3.10	0.67
t_{PLH}	Propagation Delay,					2.94	3.01	3.21	0.67
t_{PHL}	A1 to S3(INV=0)					2.77	2.83	3.04	0.69
t_{PLH}	Propagation Delay,	1.06	1.10	1.23	0.43	1.51	1.57	1.75	0.60
t_{PHL}	A2 to GE	1.09	1.17	1.40	0.77	1.57	1.68	2.00	1.07
t_{PLH}	Propagation Delay,	1.09	1.13	1.27	0.45	1.53	1.59	1.79	0.64
t_{PHL}	A2 to PR	0.91	0.95	1.08	0.41	1.30	1.35	1.50	0.50
t_{PLH}	Propagation Delay,	2.03	2.07	2.20	0.44				
t_{PHL}	A2 to S2(INV=0),S2(INV=1)	2.18	2.23	2.39	0.52				
t_{PLH}	Propagation Delay,	2.49	2.53	2.68	0.48				
t_{PHL}	A2 to S3(INV=0),S3(INV=1)	2.17	2.22	2.38	0.52				
t_{PLH}	Propagation Delay,					2.82	2.89	3.08	0.64
t_{PHL}	A2 to S2(INV=0					3.21	3.28	3.50	0.72
t_{PLH}	Propagation Delay,					2.78	2.85	3.04	0.64
t_{PHL}	A2 to S2(INV=1)					3.25	3.32	3.54	0.72
t_{PLH}	Propagation Delay,					3.55	3.62	3.83	0.69
t_{PHL}	A2 to S3(INV=0)					3.21	3.28	3.49	0.70
t_{PLH}	Propagation Delay,					3.51	3.58	3.79	0.69
t_{PHL}	A2 to S3(INV=1)					3.24	3.31	3.52	0.70
t_{PLH}	Propagation Delay,					1.35	1.41	1.59	0.59
t_{PHL}	A3 to GE					1.63	1.74	2.06	1.07
t_{PLH}	Propagation Delay,	0.96	1.01	1.13	0.42				
t_{PHL}	A3,B3 to GE	1.12	1.20	1.43	0.77				
t_{PLH}	Propagation Delay,	1.13	1.17	1.31	0.45	1.59	1.65	1.85	0.64
t_{PHL}	A3 to PR	0.97	1.02	1.14	0.41	1.39	1.44	1.59	0.51
t_{PLH}	Propagation Delay,	1.60	1.65	1.80	0.48				
t_{PHL}	A3,B3 to S3(INV=0),S3(INV=1)	1.61	1.66	1.82	0.54				
t_{PLH}	Propagation Delay,					2.24	2.31	2.52	0.69
t_{PHL}	A3 to S3(INV=0)					2.37	2.44	2.66	0.73
t_{PLH}	Propagation Delay,					2.20	2.27	2.48	0.69
t_{PHL}	A3 to S3(INV=1)					2.41	2.48	2.70	0.73
t_{PLH}	Propagation Delay,	1.13	1.17	1.31	0.45	1.60	1.67	1.86	0.64
t_{PHL}	B0 to GE	0.77	0.84	1.08	0.78	1.07	1.18	1.49	1.06
t_{PLH}	Propagation Delay,	1.06	1.11	1.24	0.45	1.46	1.52	1.72	0.64
t_{PHL}	B0 to PR	0.90	0.94	1.06	0.40	1.28	1.33	1.47	0.49
t_{PLH}	Propagation Delay,					1.84	1.91	2.10	0.64
t_{PHL}	B0 to S0(INV=0)					2.01	2.06	2.24	0.58

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay,					1.81	1.87	2.06	0.64
t_{PHL}	B0 to S0(INV=1)					2.04	2.10	2.27	0.58
t_{PLH}	Propagation Delay,	1.31	1.36	1.50	0.46				
t_{PHL}	B0 to S1(INV=0),S1(INV=1)	1.49	1.54	1.69	0.50				
t_{PLH}	Propagation Delay,					1.84	1.90	2.10	0.66
t_{PHL}	B0 to S1(INV=0)					2.18	2.24	2.44	0.66
t_{PLH}	Propagation Delay,					1.80	1.87	2.07	0.66
t_{PHL}	B0 to S1(INV=1)					2.21	2.28	2.47	0.66
t_{PLH}	Propagation Delay,	1.85	1.89	2.04	0.47				
t_{PHL}	B0 to S2(INV=0),S2(INV=1)	1.43	1.48	1.63	0.50				
t_{PLH}	Propagation Delay,					2.67	2.74	2.94	0.69
t_{PHL}	B0 to S2(INV=0)					2.14	2.20	2.41	0.68
t_{PLH}	Propagation Delay,	2.20	2.25	2.39	0.47				
t_{PHL}	B0 to S3(INV=0),S3(INV=1)	2.32	2.37	2.52	0.51				
t_{PLH}	Propagation Delay,					3.13	3.20	3.40	0.67
t_{PHL}	B0 to S3(INV=0)					3.44	3.51	3.71	0.68
t_{PLH}	Propagation Delay,					3.10	3.17	3.37	0.67
t_{PHL}	B0 to S3(INV=1)					3.47	3.54	3.74	0.68
t_{PLH}	Propagation Delay,	1.34	1.39	1.52	0.43	1.93	1.99	2.18	0.61
t_{PHL}	B1 to GE	0.94	1.01	1.25	0.78	1.31	1.42	1.74	1.06
t_{PLH}	Propagation Delay,	0.97	1.02	1.15	0.45	1.32	1.39	1.58	0.64
t_{PHL}	B1 to PR	0.85	0.89	1.01	0.40	1.19	1.24	1.39	0.49
t_{PLH}	Propagation Delay,	1.98	2.02	2.15	0.44				
t_{PHL}	B1 to S1(INV=0),S1(INV=1)	2.10	2.15	2.30	0.49				
t_{PLH}	Propagation Delay,					2.81	2.87	3.06	0.62
t_{PHL}	B1 to S1(INV=0)					3.04	3.11	3.31	0.66
t_{PLH}	Propagation Delay,					2.77	2.83	3.02	0.62
t_{PHL}	B1 to S1(INV=1)					3.08	3.15	3.35	0.66
t_{PLH}	Propagation Delay,					2.93	3.00	3.20	0.69
t_{PHL}	B1 to S2(INV=0)					2.73	2.80	3.00	0.67
t_{PLH}	Propagation Delay,	2.05	2.09	2.24	0.48				
t_{PHL}	B1 to S3(INV=0),S3(INV=1)	2.01	2.06	2.21	0.50				
t_{PLH}	Propagation Delay,					2.88	2.95	3.15	0.68
t_{PHL}	B1 to S3(INV=0)					2.93	3.00	3.20	0.67
t_{PLH}	Propagation Delay,					2.84	2.91	3.11	0.68
t_{PHL}	B1 to S3(INV=1)					2.97	3.04	3.24	0.67
t_{PLH}	Propagation Delay,	1.08	1.12	1.25	0.42	1.57	1.63	1.81	0.60
t_{PHL}	B2 to GE	1.10	1.18	1.41	0.77	1.58	1.69	2.01	1.07
t_{PLH}	Propagation Delay,	1.05	1.10	1.23	0.45	1.47	1.53	1.72	0.64
t_{PHL}	B2 to PR	0.93	0.97	1.09	0.41	1.33	1.38	1.53	0.50
t_{PLH}	Propagation Delay,	1.46	1.51	1.65	0.47				
t_{PHL}	B2 to S2(INV=0),S2(INV=1)	1.53	1.59	1.74	0.52				
t_{PLH}	Propagation Delay,					2.05	2.12	2.32	0.68
t_{PHL}	B2 to S2(INV=0)					2.30	2.37	2.58	0.70
t_{PLH}	Propagation Delay,					2.02	2.09	2.30	0.68
t_{PHL}	B2 to S2(INV=1)					2.33	2.40	2.61	0.70
t_{PLH}	Propagation Delay,	2.04	2.09	2.23	0.47				
t_{PHL}	B2 to S3(INV=0),S3(INV=1)	1.74	1.79	1.94	0.51				
t_{PLH}	Propagation Delay,					2.95	3.01	3.21	0.67
t_{PHL}	B2 to S3(INV=0)					2.57	2.64	2.85	0.69

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay, B2 to S3(INV=1)					2.92	2.99	3.19	0.67
t_{PHL}						2.60	2.67	2.87	0.69
t_{PLH}	Propagation Delay, B3 to GE					1.41	1.47	1.64	0.60
t_{PHL}						1.66	1.77	2.09	1.07
t_{PLH}	Propagation Delay, B3 to PR	1.11	1.15	1.28	0.45	1.55	1.61	1.80	0.64
t_{PHL}		1.00	1.05	1.17	0.41	1.44	1.49	1.64	0.51
t_{PLH}	Propagation Delay, CI to S0(INV=0),S0(INV=1)	0.69	0.73	0.87	0.44				
t_{PHL}		0.72	0.76	0.89	0.43				
t_{PLH}	Propagation Delay, CI to S0(INV=0)					0.97	1.03	1.22	0.63
t_{PHL}						1.02	1.07	1.23	0.54
t_{PLH}	Propagation Delay, CI to S0(INV=1)					0.93	0.99	1.18	0.63
t_{PHL}						1.06	1.11	1.28	0.54
t_{PLH}	Propagation Delay, CI to S1(INV=0), S1(INV=1),S2(INV=0)	0.73	0.78	0.92	0.46				
t_{PHL}		0.75	0.80	0.94	0.48				
t_{PLH}	Propagation Delay, CI to S1(INV=0),S2(INV=0)					1.02	1.09	1.29	0.66
t_{PHL}						1.09	1.16	1.34	0.62
t_{PLH}	Propagation Delay, CI to S1(INV=1),S2(INV=1)					0.98	1.05	1.24	0.66
t_{PHL}						1.14	1.20	1.39	0.62
t_{PLH}	Propagation Delay, CI to S2(INV=1),S3(INV=1)	0.71	0.76	0.90	0.47				
t_{PHL}		0.76	0.81	0.96	0.49				
t_{PLH}	Propagation Delay, CI to S3(INV=0)					1.01	1.07	1.27	0.66
t_{PHL}						1.05	1.12	1.30	0.62
t_{PLH}	Propagation Delay, CI to S3(INV=1)					0.96	1.03	1.23	0.66
t_{PHL}						1.09	1.16	1.34	0.62
t_{PLH}	Propagation Delay, CI to S3(INV=0)	0.72	0.76	0.90	0.47				
t_{PHL}		0.73	0.78	0.92	0.48				
t_{PLH}	Propagation Delay, B2 to S3(INV=0)								
t_{PHL}									
t_{PLH}	Propagation Delay, B2 to S3(INV=1)								
t_{PHL}									
t_r	Output Rise Time, GE	0.39	0.51	0.87	1.19	0.51	0.67	1.18	1.68
t_f	Output Fall Time, GE	0.38	0.52	0.93	1.39	0.46	0.64	1.19	1.82
t_r	Output Rise Time, PR	0.25	0.37	0.73	1.19	0.32	0.49	0.99	1.68
t_f	Output Fall Time, PR	0.26	0.32	0.49	0.57	0.31	0.38	0.58	0.68
t_r	Output Rise Time, S0	0.25	0.37	0.73	1.20	0.32	0.49	0.99	1.68
t_f	Output Fall Time, S0	0.29	0.35	0.52	0.58	0.40	0.47	0.68	0.70
t_r	Output Rise Time, S1,S2	0.35	0.47	0.83	1.20	0.41	0.58	1.09	1.71
t_f	Output Fall Time, S1,S2	0.44	0.50	0.69	0.63	0.62	0.70	0.93	0.76
t_r	Output Rise Time, S3	0.39	0.51	0.87	1.21	0.45	0.62	1.13	1.71
t_f	Output Fall Time, S3	0.47	0.53	0.73	0.64	0.65	0.73	0.96	0.79

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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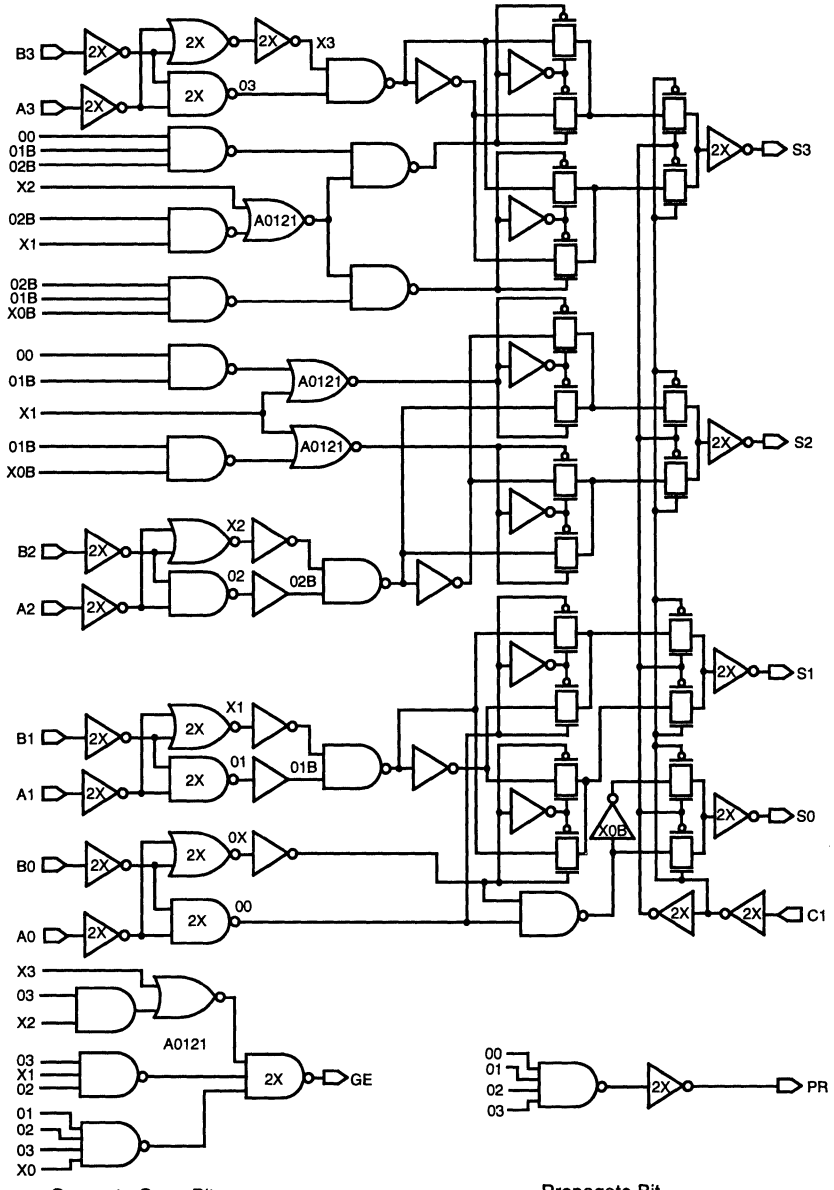
FUNCTIONAL DIAGRAM: AD4PG



Generate Carry Bit Section

Propagate Bit Section

Full Adder
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

ADFULH

MACRO	EQUIV. GATES
ADFULH	10

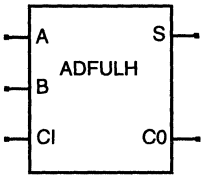
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ADFULH	CO,S / A,B,CI

MACRO	INPUT CAP.
ADFULH	A: 0.15pF B: 0.20pF CI: 0.22pF

FUNCTION TABLE

A	B	CI	S	CO
L	L	L	L	L
L	H	L	H	L
H	L	L	H	L
H	H	L	L	H
L	L	H	H	L
L	H	H	L	H
H	L	H	L	H
H	H	H	H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

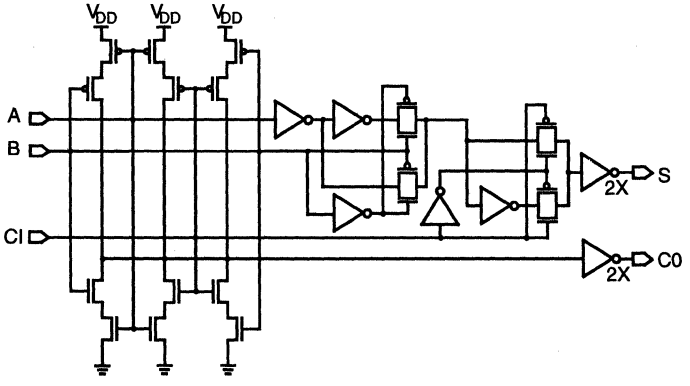
Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	ADFULH								
t_{PLH}	Propagation Delay, A to CO	0.61	0.65	0.78	0.42	0.82	0.88	1.07	0.61
t_{PHL}		0.77	0.82	0.96	0.48	1.18	1.24	1.43	0.63
t_{PLH}	Propagation Delay, A to S	1.09	1.14	1.26	0.42	1.57	1.63	1.81	0.60
t_{PHL}		1.06	1.11	1.24	0.44	1.58	1.63	1.80	0.55
t_{PLH}	Propagation Delay, B to CO	0.66	0.71	0.83	0.43	0.87	0.93	1.12	0.60
t_{PHL}		0.67	0.72	0.87	0.49	1.00	1.06	1.26	0.64
t_{PLH}	Propagation Delay, B to S	0.88	0.92	1.05	0.42	1.25	1.31	1.49	0.60
t_{PHL}		0.89	0.94	1.07	0.43	1.35	1.41	1.57	0.55
t_{PLH}	Propagation Delay, CI to CO	0.64	0.69	0.82	0.43	0.85	0.91	1.10	0.61
t_{PHL}		0.75	0.80	0.94	0.48	1.07	1.13	1.32	0.64
t_{PLH}	Propagation Delay, CI to S	0.43	0.47	0.60	0.42	0.56	0.62	0.80	0.60
t_{PHL}		0.49	0.53	0.68	0.49	0.75	0.81	1.00	0.64
t_r	Output Rise Time, CO	0.23	0.35	0.71	1.18	0.30	0.47	0.97	1.67
t_f	Output Fall Time, CO	0.39	0.45	0.62	0.58	0.50	0.57	0.80	0.75
t_r	Output Rise Time, S	0.24	0.35	0.71	1.19	0.29	0.46	0.96	1.69
t_f	Output Fall Time, S	0.27	0.33	0.52	0.64	0.82	0.88	1.07	0.61

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: ADFULH



Full Adder
2X Drive
(3.3 V and 5 V Core Voltage)

ADFULHA

MACRO	EQUIV. GATES
ADFULHA	10

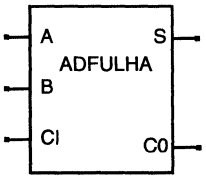
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ADFULHA	CO,S / A,B,CI

MACRO	INPUT CAP.
ADFULHA	A,CI: 0.11pF B: 0.05pF

FUNCTION TABLE

A	B	CI	S	CO
L	L	L	L	L
L	H	L	H	L
H	L	L	H	L
H	H	L	L	H
L	L	H	H	L
L	H	H	L	H
H	L	H	L	H
H	H	H	H	H



CMOS SWITCHING CHARACTERISTICS

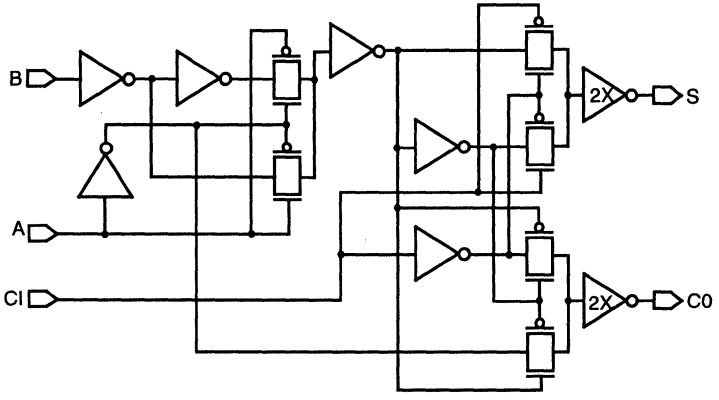
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	ADFULHA								
t_{PLH}	Propagation Delay, A to CO	1.07	1.11	1.24	0.42	1.49	1.55	1.73	0.60
t_{PHL}		0.59	0.63	0.75	0.42	0.86	0.91	1.07	0.52
t_{PLH}	Propagation Delay, A to S	1.00	1.04	1.17	0.43	1.39	1.45	1.63	0.60
t_{PHL}		1.09	1.14	1.28	0.46	1.62	1.68	1.86	0.59
t_{PLH}	Propagation Delay, B to CO	1.23	1.27	1.40	0.42	1.69	1.75	1.93	0.60
t_{PHL}		1.25	1.29	1.42	0.44	1.81	1.87	2.03	0.56
t_{PLH}	Propagation Delay, B to S	1.16	1.20	1.33	0.43	1.58	1.64	1.82	0.61
t_{PHL}		1.23	1.28	1.41	0.45	1.84	1.89	2.07	0.58
t_{PLH}	Propagation Delay, CI to CO	0.64	0.68	0.81	0.42	0.87	0.93	1.11	0.60
t_{PHL}		0.61	0.65	0.79	0.46	0.92	0.98	1.15	0.58
t_{PLH}	Propagation Delay, CI to S	0.41	0.46	0.59	0.43	0.55	0.61	0.79	0.60
t_{PHL}		0.50	0.54	0.67	0.43	0.71	0.77	0.94	0.56
t_r	Output Rise Time, CO	0.17	0.29	0.64	1.19	0.25	0.41	0.91	1.67
t_f	Output Fall Time, CO	0.27	0.33	0.51	0.58	0.39	0.47	0.68	0.72
t_r	Output Rise Time, S	0.19	0.31	0.67	1.19	0.25	0.41	0.91	1.67
t_f	Output Fall Time, S	0.28	0.34	0.51	0.59	0.39	0.47	0.68	0.72

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: ADFULHA



Half Adder
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

ADHALFH

MACRO	EQUIV. GATES
ADHALFH	6

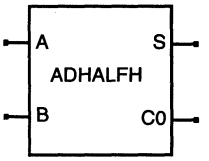
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ADHALFH	CO,S / A,B

MACRO	INPUT CAP.
ADHALFH	A: 0.09pF B: 0.17pF

FUNCTION TABLE

A	B	S	CO
L	L	L	L
L	H	H	L
H	L	H	L
H	H	L	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

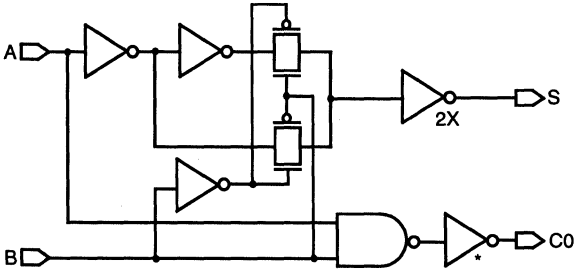
Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	ADHALFH								
t_{PLH}	Propagation Delay, A to CO	0.43	0.47	0.60	0.42	0.57	0.63	0.80	0.59
t_{PHL}		0.38	0.42	0.54	0.39	0.54	0.58	0.73	0.48
t_{PLH}	Propagation Delay, A to S	0.64	0.68	0.81	0.43	0.88	0.94	1.12	0.60
t_{PHL}		0.72	0.77	0.90	0.44	1.05	1.11	1.27	0.55
t_{PLH}	Propagation Delay, B to CO	0.44	0.48	0.61	0.42	0.57	0.63	0.81	0.59
t_{PHL}		0.30	0.34	0.46	0.39	0.47	0.52	0.66	0.47
t_{PLH}	Propagation Delay, B to S	0.41	0.45	0.58	0.43	0.54	0.60	0.78	0.60
t_{PHL}		0.45	0.49	0.62	0.44	0.67	0.73	0.90	0.56
t_r	Output Rise Time, CO	0.17	0.29	0.65	1.20	0.21	0.37	0.88	1.69
t_f	Output Fall Time, CO	0.16	0.22	0.39	0.58	0.20	0.27	0.47	0.68
t_r	Output Rise Time, S	0.18	0.30	0.66	1.19	0.20	0.37	0.88	1.69
t_f	Output Fall Time, S	0.24	0.30	0.47	0.59	0.34	0.41	0.63	0.72

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: ADHALF



2-Input AND Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

AND2
AND2H

MACRO	EQUIV. GATES
All	2

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A,B

MACRO	INPUT CAP.
All	A,B: 0.05pF

FUNCTION TABLE

A	B	X
L	L	L
L	H	L
H	L	L
H	H	H

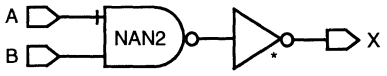
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AND2								
t_{PLH}	Propagation Delay, A to X	0.38	0.47	0.71	0.82	0.50	0.62	0.96	1.16
t_{PHL}		0.25	0.33	0.56	0.76	0.38	0.47	0.74	0.91
t_{PLH}	Propagation Delay, B to X	0.37	0.46	0.70	0.83	0.49	0.61	0.96	1.16
t_{PHL}		0.34	0.41	0.64	0.76	0.47	0.56	0.84	0.91
t_r	Output Rise Time, X	0.15	0.39	1.12	2.43	0.19	0.53	1.57	3.44
t_f	Output Fall Time, X	0.14	0.25	0.61	1.18	0.18	0.32	0.75	1.43
	AND2H								
t_{PLH}	Propagation Delay, A to X	0.44	0.49	0.61	0.42	0.58	0.64	0.82	0.59
t_{PHL}		0.33	0.37	0.49	0.38	0.48	0.53	0.67	0.47
t_{PLH}	Propagation Delay, B to X	0.44	0.48	0.61	0.42	0.59	0.64	0.82	0.58
t_{PHL}		0.40	0.44	0.55	0.38	0.56	0.61	0.75	0.48
t_r	Output Rise Time, X	0.17	0.29	0.65	1.20	0.25	0.42	0.92	1.69
t_f	Output Fall Time, X	0.19	0.25	0.42	0.57	0.24	0.31	0.51	0.68

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: AND2



*1X for AND 2
2X for AND2H

3-Input AND Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

AND3
AND3H

MACRO	EQUIV. GATES
AND3	2
AND3H	3

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-C

MACRO	INPUT CAP.
All	A-C: 0.05pF

FUNCTION TABLE

A	B	C	X
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

CMOS SWITCHING CHARACTERISTICS

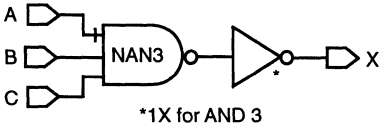
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AND3								
t_{PLH}	Propagation Delay, A to X	0.50	0.58	0.83	0.83	0.63	0.75	1.10	1.17
t_{PHL}		0.26	0.34	0.57	0.76	0.41	0.51	0.78	0.92
t_{PLH}	Propagation Delay, B to X	0.52	0.60	0.85	0.82	0.67	0.78	1.13	1.16
t_{PHL}		0.34	0.41	0.64	0.76	0.51	0.60	0.87	0.91
t_{PLH}	Propagation Delay, C to X	0.50	0.58	0.83	0.83	0.69	0.80	1.15	1.17
t_{PHL}		0.41	0.48	0.71	0.76	0.59	0.68	0.96	0.93
t_r	Output Rise Time, X	0.19	0.43	1.16	2.42	0.25	0.59	1.62	3.42
t_f	Output Fall Time, X	0.18	0.30	0.65	1.18	0.21	0.35	0.78	1.42
	AND3H								
t_{PLH}	Propagation Delay, A to X	0.58	0.62	0.75	0.43	0.74	0.80	0.98	0.60
t_{PHL}		0.34	0.38	0.50	0.39	0.50	0.55	0.70	0.48
t_{PLH}	Propagation Delay, B to X	0.58	0.63	0.75	0.43	0.76	0.82	1.00	0.62
t_{PHL}		0.40	0.44	0.55	0.39	0.59	0.63	0.78	0.48
t_{PLH}	Propagation Delay, C to X	0.57	0.61	0.74	0.43	0.79	0.85	1.03	0.61
t_{PHL}		0.47	0.51	0.62	0.39	0.67	0.72	0.87	0.49
t_r	Output Rise Time, X	0.24	0.36	0.72	1.18	0.32	0.49	0.99	1.68
t_f	Output Fall Time, X	0.25	0.30	0.47	0.56	0.28	0.35	0.56	0.68

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: AND3



*1X for AND 3
2X for AND3H

4-Input AND Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

AND4
AND4H

MACRO	EQUIV. GATES
All	3

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-D

MACRO	INPUT CAP.
All	A-D: 0.05pF

FUNCTION TABLE

A	B	C	D	X
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

CMOS SWITCHING CHARACTERISTICS

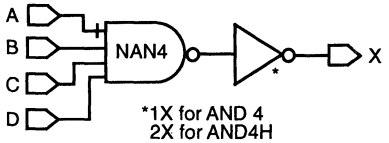
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AND4								
t_{PLH}	Propagation Delay, A to X	0.58	0.67	0.92	0.84	0.74	0.86	1.21	1.18
t_{PHL}		0.26	0.34	0.57	0.76	0.42	0.52	0.79	0.92
t_{PLH}	Propagation Delay, B to X	0.61	0.70	0.95	0.84	0.79	0.91	1.26	1.19
t_{PHL}		0.33	0.41	0.64	0.76	0.51	0.60	0.88	0.92
t_{PLH}	Propagation Delay, C to X	0.63	0.72	0.97	0.84	0.86	0.98	1.33	1.19
t_{PHL}		0.40	0.48	0.71	0.76	0.61	0.70	0.98	0.93
t_{PLH}	Propagation Delay, D to X	0.62	0.70	0.95	0.84	0.87	0.99	1.35	1.19
t_{PHL}		0.44	0.52	0.75	0.77	0.65	0.75	1.03	0.94
t_r	Output Rise Time, X	0.23	0.47	1.19	2.41	0.30	0.64	1.65	3.40
t_f	Output Fall Time, X	0.21	0.33	0.68	1.18	0.25	0.39	0.82	1.42
	AND4H								
t_{PLH}	Propagation Delay, A to X	0.67	0.71	0.85	0.45	0.85	0.92	1.11	0.64
t_{PHL}		0.34	0.38	0.49	0.39	0.52	0.56	0.71	0.48
t_{PLH}	Propagation Delay, B to X	0.70	0.74	0.88	0.45	0.91	0.98	1.17	0.64
t_{PHL}		0.40	0.43	0.55	0.39	0.59	0.64	0.79	0.48
t_{PLH}	Propagation Delay, C to X	0.71	0.76	0.89	0.45	0.98	1.04	1.23	0.63
t_{PHL}		0.46	0.50	0.62	0.40	0.68	0.73	0.88	0.49
t_{PLH}	Propagation Delay, D to X	0.70	0.75	0.88	0.45	0.97	1.04	1.23	0.64
t_{PHL}		0.49	0.53	0.65	0.41	0.72	0.77	0.92	0.51
t_r	Output Rise Time, X	0.29	0.41	0.76	1.18	0.38	0.54	1.05	1.68
t_f	Output Fall Time, X	0.27	0.32	0.49	0.57	0.30	0.36	0.57	0.68

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: AND4



8-Input AND Gate
2X Drive
(3.3 V and 5 V Core Voltage)

AND8H

MACRO	EQUIV. GATES
AND8H	6

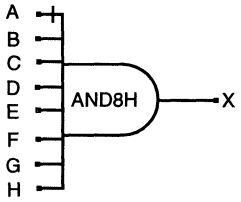
Rev. 1.07

MACRO	OUTPUTS/INPUTS
AND8H	X / A-H

MACRO	INPUT CAP.
AND8H	A-H: 0.05pF

FUNCTION TABLE

A	B	C	D	E	F	G	H	X
L	X	X	X	X	X	X	X	L
X	L	X	X	X	X	X	X	L
X	X	L	X	X	X	X	X	L
X	X	X	L	X	X	X	X	L
X	X	X	X	L	X	X	X	L
X	X	X	X	X	L	X	X	L
X	X	X	X	X	X	L	X	L
X	X	X	X	X	X	X	L	L
H	H	H	H	H	H	H	H	H



CMOS SWITCHING CHARACTERISTICS

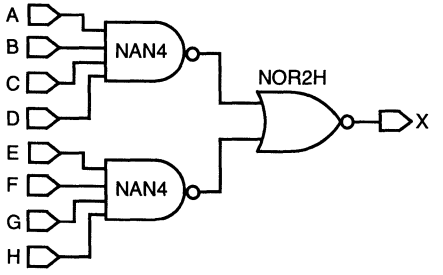
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AND8H								
t_{PLH}	Propagation Delay, A to X	0.72	0.80	1.04	0.81	0.91	1.03	1.39	1.20
t_{PHL}		0.33	0.37	0.49	0.39	0.52	0.56	0.71	0.48
t_{PLH}	Propagation Delay, B to X	0.76	0.84	1.08	0.80	0.97	1.09	1.45	1.21
t_{PHL}		0.39	0.43	0.55	0.39	0.59	0.64	0.79	0.49
t_{PLH}	Propagation Delay, C to X	0.77	0.85	1.09	0.81	1.04	1.16	1.52	1.20
t_{PHL}		0.46	0.50	0.61	0.40	0.68	0.73	0.88	0.49
t_{PLH}	Propagation Delay, D to X	0.76	0.84	1.09	0.81	1.04	1.16	1.52	1.21
t_{PHL}		0.48	0.52	0.65	0.41	0.72	0.77	0.92	0.51
t_{PLH}	Propagation Delay, E to X	0.72	0.80	1.04	0.81	0.93	1.05	1.41	1.20
t_{PHL}		0.33	0.37	0.49	0.39	0.54	0.59	0.73	0.48
t_{PLH}	Propagation Delay, F to X	0.76	0.84	1.08	0.80	0.99	1.11	1.47	1.20
t_{PHL}		0.39	0.43	0.55	0.39	0.62	0.67	0.81	0.49
t_{PLH}	Propagation Delay, G to X	0.77	0.85	1.09	0.81	1.06	1.18	1.54	1.21
t_{PHL}		0.46	0.50	0.61	0.40	0.76	0.81	0.96	0.50
t_{PLH}	Propagation Delay, H to X	0.76	0.84	1.09	0.81	0.49	0.84	1.88	3.47
t_{PHL}		0.48	0.52	0.65	0.41	0.35	0.42	0.63	0.68
t_r	Output Rise Time, X	0.36	0.60	1.32	2.39	0.91	1.03	1.39	1.20
t_f	Output Fall Time, X	0.30	0.36	0.53	0.56	0.52	0.56	0.71	0.48

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: AND8H



2-Input AND + 2-Input NOR into a 2-Input NOR 1X & 2X Drive (3.3 V and 5 V Core Voltage)

ANDOI22 ANDOI22H

MACRO	EQUIV. GATES
ANDOI22	3
ANDOI22H	4

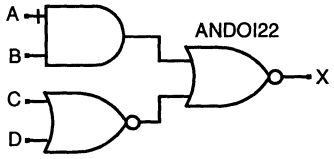
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-D

MACRO	INPUT CAP.
ANDOI22	A-D: 0.05pF
ANDOI22H	A,B: 0.09pF C,D: 0.05pF

FUNCTION TABLE

A	B	C	D	X
H	H	X	X	L
X	X	L	L	L
L	X	H	X	H
L	X	X	H	H
X	L	H	X	H
X	L	X	H	H



CMOS SWITCHING CHARACTERISTICS

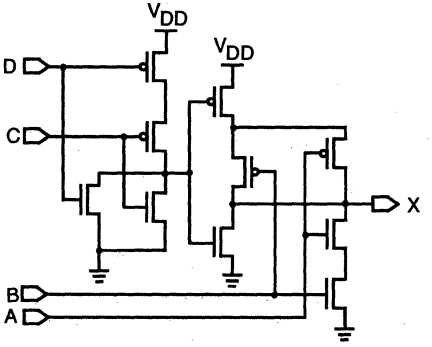
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

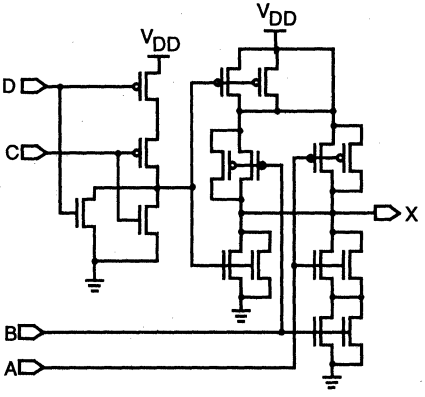
Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
ANDOI22									
t_{PLH}	Propagation Delay, A to X	0.21	0.37	0.85	1.61	0.21	0.37	0.85	1.61
t_{PHL}		0.29	0.40	0.74	1.14	0.29	0.40	0.74	1.14
t_{PLH}	Propagation Delay, B to X	0.27	0.43	0.92	1.60	0.27	0.43	0.92	1.60
t_{PHL}		0.25	0.37	0.71	1.13	0.25	0.37	0.71	1.13
t_{PLH}	Propagation Delay, C to X	0.47	0.63	1.12	1.61	0.47	0.63	1.12	1.61
t_{PHL}		0.49	0.57	0.80	0.77	0.49	0.57	0.80	0.77
t_{PLH}	Propagation Delay, D to X	0.50	0.66	1.14	1.61	0.50	0.66	1.14	1.61
t_{PHL}		0.50	0.58	0.81	0.77	0.50	0.58	0.81	0.77
t_r	Output Rise Time, X	0.51	1.00	2.46	4.87	0.51	1.00	2.46	4.87
t_f	Output Fall Time, X	0.31	0.51	1.10	1.96	0.31	0.51	1.10	1.96
ANDOI22H									
t_{PLH}	Propagation Delay, A to X	0.18	0.26	0.50	0.80	0.18	0.26	0.50	0.80
t_{PHL}		0.25	0.31	0.48	0.57	0.25	0.31	0.48	0.57
t_{PLH}	Propagation Delay, B to X	0.27	0.35	0.59	0.80	0.27	0.35	0.59	0.80
t_{PHL}		0.24	0.30	0.47	0.56	0.24	0.30	0.47	0.56
t_{PLH}	Propagation Delay, C to X	0.50	0.58	0.82	0.81	0.50	0.58	0.82	0.81
t_{PHL}		0.59	0.63	0.75	0.41	0.59	0.63	0.75	0.41
t_{PLH}	Propagation Delay, D to X	0.53	0.61	0.85	0.81	0.53	0.61	0.85	0.81
t_{PHL}		0.59	0.63	0.75	0.41	0.59	0.63	0.75	0.41
t_r	Output Rise Time, X	0.48	0.73	1.45	2.42	0.48	0.73	1.45	2.42
t_f	Output Fall Time, X	0.38	0.47	0.75	0.94	0.38	0.47	0.75	0.94

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: ANDOI22



FUNCTIONAL DIAGRAM: ANDOI22H



7

2, 1-Input AND-OR
2X Drive
(3.3 V and 5 V Core Voltage)

AO21H

MACRO	EQUIV. GATES
AO21H	3

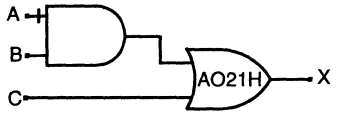
Rev. 1.07

MACRO	OUTPUTS/INPUTS
AO21H	X / A-C

MACRO	INPUT CAP.
AO21H	A-C: 0.05pF

FUNCTION TABLE

A	B	C	X
X	X	H	H
H	H	X	H
X	L	L	L
L	X	L	L



CMOS SWITCHING CHARACTERISTICS

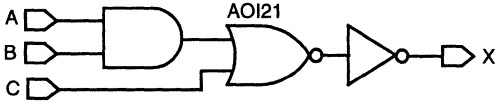
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AO21H								
t_{PLH}	Propagation Delay, A to X	0.44	0.48	0.61	0.43	0.59	0.65	0.83	0.60
t_{PHL}		0.55	0.59	0.72	0.43	0.80	0.86	1.02	0.55
t_{PLH}	Propagation Delay, B to X	0.43	0.48	0.60	0.42	0.60	0.66	0.83	0.59
t_{PHL}		0.64	0.68	0.81	0.44	0.94	1.00	1.17	0.56
t_{PLH}	Propagation Delay, C to X	0.40	0.44	0.57	0.42	0.53	0.59	0.76	0.59
t_{PHL}		0.51	0.55	0.67	0.42	0.73	0.78	0.94	0.54
t_r	Output Rise Time, X	0.16	0.28	0.64	1.20	0.21	0.38	0.88	1.69
t_f	Output Fall Time, X	0.31	0.37	0.53	0.55	0.38	0.45	0.66	0.70

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: AO21H



2-Wide, 2-Input AND-OR 2X Drive (3.3 V and 5 V Core Voltage)

AO22H

MACRO	EQUIV. GATES
AO22H	3

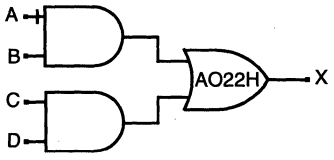
Rev. 1.07

MACRO	OUTPUTS/INPUTS
AO22H	X / A-D

MACRO	INPUT CAP.
AO22H	A-D: 0.05pF

FUNCTION TABLE

A	B	C	D	X
H	H	X	X	H
X	X	H	H	H
X	L	L	X	L
L	X	X	L	L
H	L	H	L	L
L	H	L	H	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

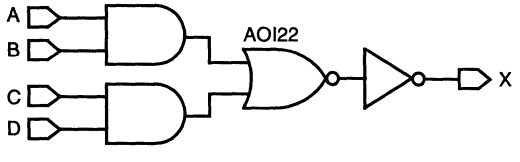
Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AO22H								
t_{PLH}	Propagation Delay, A to X	0.57	0.61	0.74	0.43	0.76	0.82	1.00	0.60
t_{PHL}		0.67	0.72	0.85	0.45	1.03	1.09	1.26	0.57
t_{PLH}	Propagation Delay, B to X	0.55	0.59	0.72	0.43	0.73	0.79	0.98	0.61
t_{PHL}		0.77	0.81	0.95	0.45	1.17	1.23	1.40	0.58
t_{PLH}	Propagation Delay, C to X	0.45	0.49	0.62	0.43	0.61	0.67	0.85	0.60
t_{PHL}		0.56	0.60	0.73	0.43	0.82	0.87	1.04	0.56
t_{PLH}	Propagation Delay, D to X	0.44	0.49	0.61	0.42	0.61	0.67	0.85	0.59
t_{PHL}		0.65	0.70	0.83	0.45	0.98	1.03	1.20	0.56
t_r	Output Rise Time, X	0.21	0.33	0.68	1.18	0.26	0.43	0.93	1.68
t_f	Output Fall Time, X	0.37	0.42	0.59	0.56	0.42	0.49	0.70	0.69

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: AO22H



3,2, 1-Input AND-OR Gate 2X Drive (3.3 V and 5 V Core Voltage)

AO321H

MACRO	EQUIV. GATES
AO321H	5

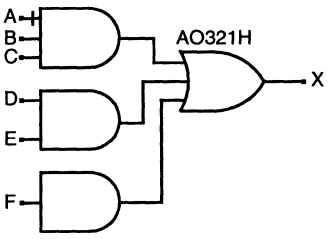
Rev. 1.07

MACRO	OUTPUTS/INPUTS
AO321H	X / A-F

MACRO	INPUT CAP.
AO321H	A-F: 0.05pF

FUNCTION TABLE

A	B	C	D	E	F	X
L	X	X	L	X	L	L
X	L	X	L	X	L	L
X	X	L	L	X	L	L
L	X	X	X	L	L	L
X	L	X	X	L	L	L
X	X	L	X	L	L	L
H	H	H	X	X	X	H
X	X	X	H	H	X	H
X	X	X	X	X	H	H



CMOS SWITCHING CHARACTERISTICS

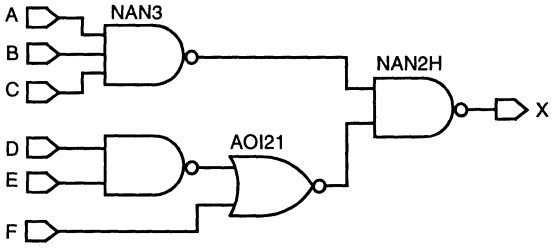
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AO321H								
t_{PLH}	Propagation Delay, A to X	0.57	0.62	0.75	0.44	0.76	0.82	1.00	0.61
t_{PHL}		0.37	0.43	0.60	0.57	0.55	0.62	0.85	0.76
t_{PLH}	Propagation Delay, B to X	0.58	0.62	0.75	0.43	0.77	0.83	1.01	0.62
t_{PHL}		0.43	0.49	0.66	0.58	0.62	0.70	0.93	0.77
t_{PLH}	Propagation Delay, C to X	0.57	0.61	0.74	0.43	0.79	0.85	1.04	0.62
t_{PHL}		0.50	0.55	0.73	0.58	0.71	0.79	1.02	0.77
t_{PLH}	Propagation Delay, D to X	0.49	0.53	0.66	0.41	0.68	0.74	0.91	0.59
t_{PHL}		0.69	0.74	0.92	0.58	0.99	1.07	1.31	0.78
t_{PLH}	Propagation Delay, E to X	0.49	0.53	0.66	0.42	0.68	0.74	0.92	0.59
t_{PHL}		0.60	0.65	0.83	0.57	0.85	0.93	1.16	0.78
t_{PLH}	Propagation Delay, F to X	0.45	0.49	0.62	0.42	0.61	0.67	0.85	0.59
t_{PHL}		0.55	0.61	0.78	0.57	0.78	0.86	1.09	0.77
t_r	Output Rise Time, X	0.27	0.39	0.75	1.20	0.35	0.52	1.03	1.69
t_f	Output Fall Time, X	0.33	0.42	0.71	0.97	0.38	0.50	0.88	1.24

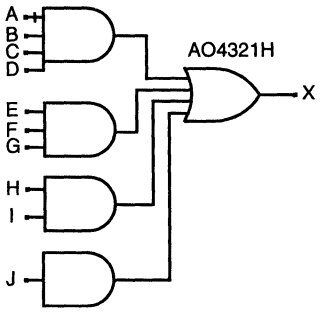
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: AO321H



4,3,2, 1-Input AND-OR Gate
2X Drive
(3.3 V and 5 V Core Voltage)

AO4321H



MACRO	EQUIV. GATES
AO4321H	8

Rev. 1.07

MACRO	OUTPUTS/INPUTS
AO4321H	X / A-J

MACRO	INPUT CAP.
AO4321H	A-J: 0.05pF

FUNCTION TABLE

(A*B*C*D)	(E*F*G)	(H*I)	J	X
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H
L	L	L	L	L

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

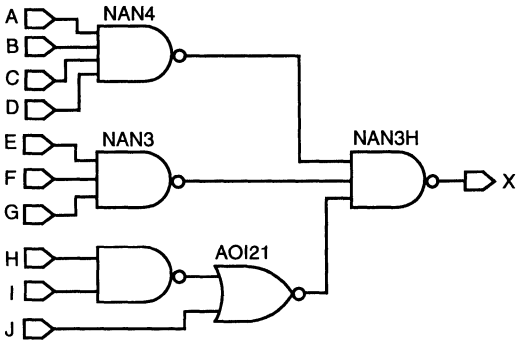
Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AO4321H								
t_{PLH}	Propagation Delay, A to X	0.66	0.70	0.84	0.45	0.86	0.93	1.12	0.64
t_{PHL}		0.39	0.47	0.70	0.77	0.59	0.69	1.01	1.05
t_{PLH}	Propagation Delay, B to X	0.68	0.73	0.86	0.46	0.92	0.99	1.18	0.64
t_{PHL}		0.46	0.53	0.76	0.77	0.66	0.77	1.08	1.06
t_{PLH}	Propagation Delay, C to X	0.70	0.75	0.89	0.46	0.99	1.05	1.25	0.64
t_{PHL}		0.52	0.60	0.83	0.77	0.76	0.87	1.19	1.06
t_{PLH}	Propagation Delay, D to X	0.70	0.74	0.88	0.46	0.99	1.05	1.25	0.65
t_{PHL}		0.57	0.65	0.88	0.78	0.81	0.92	1.24	1.07
t_{PLH}	Propagation Delay, E to X	0.64	0.68	0.81	0.43	0.85	0.91	1.09	0.60
t_{PHL}		0.43	0.50	0.74	0.77	0.64	0.74	1.06	1.05
t_{PLH}	Propagation Delay, F to X	0.64	0.68	0.81	0.43	0.88	0.94	1.12	0.60
t_{PHL}		0.49	0.57	0.80	0.77	0.71	0.82	1.13	1.05
t_{PLH}	Propagation Delay, G to X	0.63	0.67	0.80	0.43	0.89	0.95	1.13	0.61
t_{PHL}		0.55	0.63	0.86	0.77	0.78	0.89	1.21	1.06
t_{PLH}	Propagation Delay, H to X	0.53	0.57	0.70	0.42	0.74	0.80	0.98	0.59
t_{PHL}		0.75	0.83	1.06	0.77	1.08	1.19	1.51	1.06
t_{PLH}	Propagation Delay, I to X	0.54	0.58	0.71	0.42	0.75	0.81	0.99	0.60
t_{PHL}		0.65	0.73	0.96	0.77	0.94	1.05	1.37	1.07
t_{PLH}	Propagation Delay, J to X	0.49	0.53	0.66	0.42	0.68	0.74	0.91	0.59
t_{PHL}		0.61	0.69	0.92	0.77	0.87	0.98	1.30	1.07
t_r	Output Rise Time, X	0.40	0.52	0.88	1.20	0.50	0.66	1.17	1.69
t_f	Output Fall Time, X	0.37	0.51	0.92	1.38	0.43	0.61	1.16	1.80

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: AO4321H



2, 1-Input AND-OR-Invert 1X & 2X Drive (3.3 V and 5 V Core Voltage)

AOI21 AOI21H

MACRO	EQUIV. GATES
AOI21	2
AOI21H	3

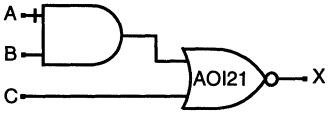
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-C

MACRO	INPUT CAP.
AOI21	A-C: 0.05pF
AOI21H	A-C: 0.09pF

FUNCTION TABLE

A	B	C	X
X	X	H	L
H	H	X	L
X	L	L	H
L	X	L	H



CMOS SWITCHING CHARACTERISTICS

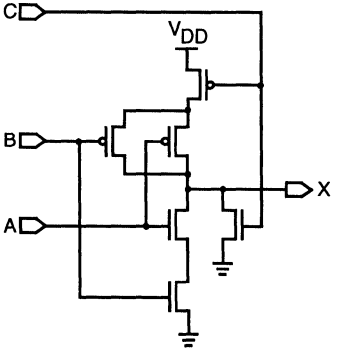
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

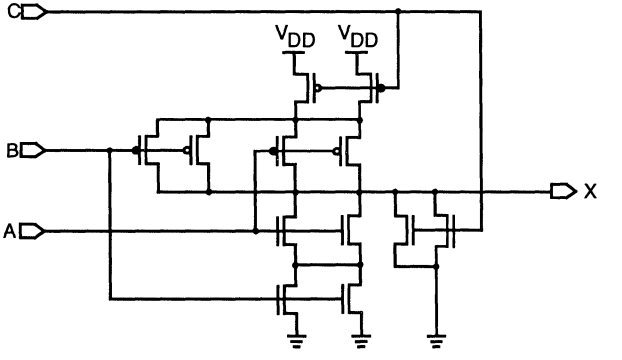
Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AOI21								
t_{PLH}	Propagation Delay, A to X	0.20	0.36	0.85	1.61	0.28	0.52	1.22	2.36
t_{PHL}		0.28	0.40	0.74	1.14	0.37	0.52	0.97	1.50
t_{PLH}	Propagation Delay, B to X	0.27	0.43	0.91	1.60	0.38	0.62	1.32	2.35
t_{PHL}		0.25	0.37	0.71	1.13	0.34	0.49	0.94	1.50
t_{PLH}	Propagation Delay, C to X	0.30	0.46	0.94	1.61	0.44	0.67	1.38	2.36
t_{PHL}		0.29	0.36	0.59	0.76	0.38	0.47	0.74	0.91
t_r	Output Rise Time, X	0.50	0.99	2.45	4.87	0.70	1.40	3.50	7.01
t_f	Output Fall Time, X	0.28	0.48	1.07	1.96	0.31	0.57	1.33	2.54
	AOI21H								
t_{PLH}	Propagation Delay, A to X	0.18	0.26	0.50	0.80	0.24	0.36	0.71	1.18
t_{PHL}		0.25	0.30	0.47	0.57	0.33	0.40	0.63	0.75
t_{PLH}	Propagation Delay, B to X	0.27	0.35	0.59	0.80	0.37	0.48	0.84	1.18
t_{PHL}		0.24	0.30	0.46	0.56	0.32	0.40	0.62	0.75
t_{PLH}	Propagation Delay, C to X	0.29	0.37	0.61	0.80	0.41	0.53	0.89	1.18
t_{PHL}		0.26	0.29	0.41	0.38	0.34	0.39	0.52	0.46
t_r	Output Rise Time, X	0.49	0.73	1.46	2.42	0.66	1.00	2.05	3.50
t_f	Output Fall Time, X	0.31	0.40	0.69	0.94	0.33	0.46	0.83	1.25

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: AOI21



FUNCTIONAL DIAGRAM: AOI21H



2,1, 1-Input AND-OR-Invert 1X & 2X Drive (3.3 V and 5 V Core Voltage)

AOI211
AOI211H

MACRO	EQUIV. GATES
AOI211	2
AOI211H	4

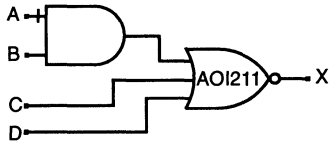
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-D

MACRO	INPUT CAP.
All	A-D: 0.05pF

FUNCTION TABLE

A	B	C	D	X
H	H	X	X	L
L	H	L	L	H
H	L	L	L	H
X	X	H	X	L
X	X	X	H	L



CMOS SWITCHING CHARACTERISTICS

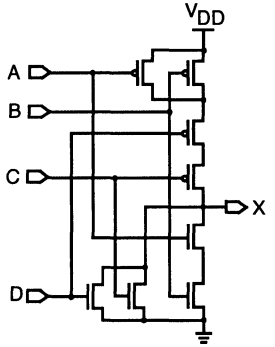
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

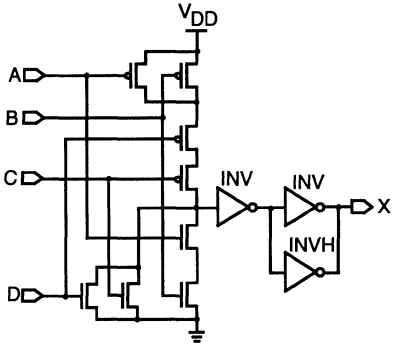
Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AOI211								
t_{PLH}	Propagation Delay, A to X	0.31	0.55	1.29	2.44	0.49	0.86	1.94	3.62
t_{PHL}		0.35	0.46	0.81	1.15	0.46	0.61	1.06	1.52
t_{PLH}	Propagation Delay, B to X	0.42	0.66	1.39	2.43	0.65	1.02	2.10	3.61
t_{PHL}		0.31	0.42	0.77	1.15	0.43	0.58	1.03	1.52
t_{PLH}	Propagation Delay, C to X	0.25	0.49	1.22	2.42	0.32	0.68	1.77	3.61
t_{PHL}		0.22	0.30	0.52	0.76	0.31	0.40	0.67	0.91
t_{PLH}	Propagation Delay, D to X	0.29	0.54	1.26	2.42	0.42	0.78	1.87	3.62
t_{PHL}		0.25	0.32	0.55	0.76	0.35	0.44	0.71	0.91
t_r	Output Rise Time, X	0.77	1.50	3.70	7.34	1.09	2.15	5.34	10.63
t_f	Output Fall Time, X	0.34	0.54	1.13	1.96	0.38	0.63	1.39	2.54
	AOI211H								
t_{PLH}	Propagation Delay, A to X	0.83	0.86	0.95	0.29	1.25	1.29	1.41	0.40
t_{PHL}		0.70	0.73	0.81	0.28	1.01	1.04	1.14	0.34
t_{PLH}	Propagation Delay, B to X	0.99	1.02	1.11	0.29	1.48	1.52	1.64	0.40
t_{PHL}		0.69	0.72	0.80	0.28	1.00	1.04	1.14	0.34
t_{PLH}	Propagation Delay, C to X	0.79	0.81	0.90	0.28	1.10	1.14	1.26	0.40
t_{PHL}		0.53	0.56	0.64	0.27	0.78	0.81	0.91	0.34
t_{PLH}	Propagation Delay, D to X	0.83	0.86	0.94	0.28	1.19	1.23	1.35	0.40
t_{PHL}		0.58	0.60	0.68	0.26	0.81	0.85	0.95	0.34
t_r	Output Rise Time, X	0.21	0.28	0.51	0.76	0.25	0.36	0.69	1.10
t_f	Output Fall Time, X	0.21	0.25	0.36	0.37	0.25	0.30	0.44	0.46

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: AOI211



FUNCTIONAL DIAGRAM: AOI211H



7

2-Wide, 2-Input AND-OR-Invert 1X & 2X Drive (3.3 V and 5 V Core Voltage)

AOI22 AOI22H

MACRO	EQUIV. GATES
AOI22	2
AOI22H	4

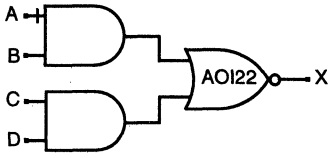
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-D

MACRO	INPUT CAP.
All	A-D: 0.05pF

FUNCTION TABLE

A	B	C	D	X
H	H	X	X	L
X	X	H	H	L
X	L	L	X	H
L	X	X	L	H
H	L	H	L	H
L	H	L	H	H



CMOS SWITCHING CHARACTERISTICS

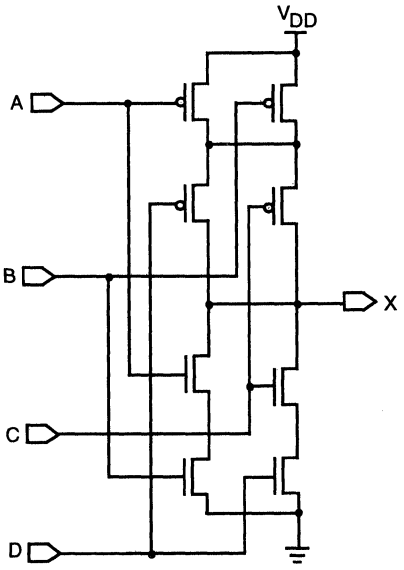
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

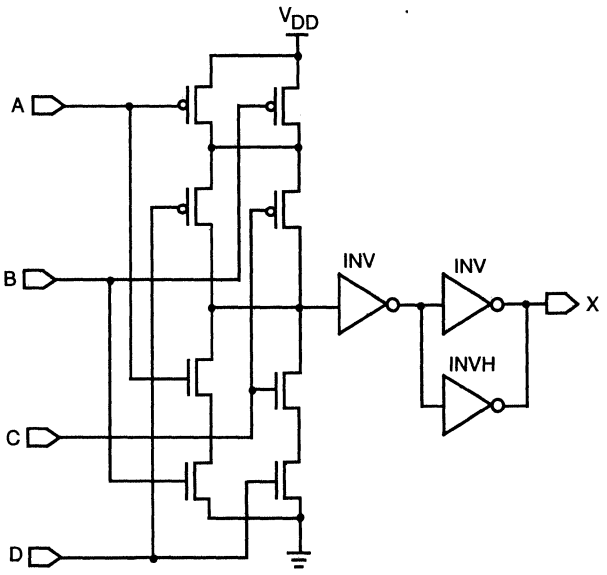
Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	AOI22								
t_{PLH}	Propagation Delay, A to X	0.21	0.33	0.69	1.22	0.31	0.49	1.03	1.79
t_{PHL}		0.38	0.49	0.84	1.14	0.48	0.64	1.09	1.51
t_{PLH}	Propagation Delay, B to X	0.26	0.38	0.74	1.21	0.39	0.57	1.11	1.79
t_{PHL}		0.34	0.46	0.80	1.14	0.46	0.61	1.06	1.51
t_{PLH}	Propagation Delay, C to X	0.26	0.43	0.91	1.61	0.38	0.61	1.32	2.36
t_{PHL}		0.31	0.42	0.76	1.14	0.39	0.54	0.99	1.50
t_{PLH}	Propagation Delay, D to X	0.33	0.49	0.98	1.60	0.47	0.71	1.42	2.35
t_{PHL}		0.27	0.38	0.73	1.14	0.36	0.51	0.96	1.50
t_r	Output Rise Time, X	0.61	1.10	2.56	4.87	0.84	1.55	3.65	7.01
t_f	Output Fall Time, X	0.33	0.53	1.12	1.97	0.36	0.61	1.38	2.55
	AOI22H								
t_{PLH}	Propagation Delay, A to X	0.62	0.65	0.73	0.28	0.91	0.95	1.07	0.39
t_{PHL}		0.76	0.79	0.87	0.28	1.07	1.10	1.21	0.34
t_{PLH}	Propagation Delay, B to X	0.71	0.74	0.82	0.28	1.02	1.06	1.18	0.40
t_{PHL}		0.76	0.78	0.87	0.28	1.05	1.09	1.19	0.34
t_{PLH}	Propagation Delay, C to X	0.76	0.79	0.88	0.28	1.09	1.13	1.25	0.40
t_{PHL}		0.69	0.72	0.80	0.28	0.98	1.02	1.12	0.34
t_{PLH}	Propagation Delay, D to X	0.86	0.88	0.97	0.29	1.26	1.30	1.42	0.40
t_{PHL}		0.70	0.73	0.81	0.27	0.98	1.01	1.11	0.34
t_r	Output Rise Time, X	0.20	0.28	0.51	0.77	0.23	0.34	0.67	1.10
t_f	Output Fall Time, X	0.22	0.26	0.37	0.37	0.25	0.30	0.43	0.45

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: AOI22



FUNCTIONAL DIAGRAM: AOI22H



7

Non-Inverting Buffer
1X Drive
(3.3 V and 5 V Voltage)

BUF

MACRO	EQUIV. GATES
BUF	1

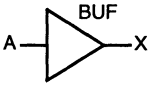
Rev. 1.07

MACRO	OUTPUTS/INPUTS
BUF	X / A

MACRO	INPUT CAP.
BUF	A: 0.05pF

FUNCTION TABLE

A	X
L	L
H	H



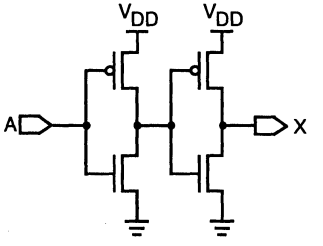
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	BUF								
t_{PLH}	Propagation Delay,	0.29	0.37	0.62	0.82	0.39	0.50	0.85	1.15
t_{PHL}	A to X	0.28	0.35	0.58	0.75	0.37	0.46	0.74	0.91
t_r	Output Rise Time, X	0.17	0.41	1.14	2.42	0.16	0.51	1.54	3.46
t_f	Output Fall Time, X	0.15	0.26	0.61	1.17	0.15	0.29	0.72	1.43

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: BUF



7

Non-Inverting Buffer
2X Drive
(3.3 V and 5 V Voltage)

BUF2
BUF2B

MACRO	EQUIV. GATES
BUF2	2
BUF2B	3

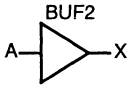
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A

MACRO	INPUT CAP.
BUF2	A: 0.05pF
BUF2B	A: 0.07pF

FUNCTION TABLE

A	X
L	L
H	H



CMOS SWITCHING CHARACTERISTICS

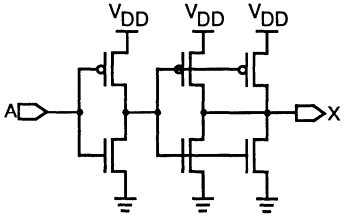
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	BUF2								
t_{PLH}	Propagation Delay,	0.34	0.38	0.50	0.41	0.44	0.50	0.67	0.58
t_{PHL}	A to X	0.34	0.38	0.50	0.38	0.47	0.52	0.66	0.47
t_r	Output Rise Time, X	0.15	0.27	0.63	1.20	0.17	0.34	0.86	1.72
t_f	Output Fall Time, X	0.16	0.22	0.39	0.56	0.22	0.29	0.49	0.68
	BUF2B								
t_{PLH}	Propagation Delay,	0.40	0.42	0.48	0.21	0.48	0.51	0.60	0.30
t_{PHL}	A to X	0.25	0.28	0.40	0.38	0.38	0.43	0.56	0.45
t_r	Output Rise Time, X	0.14	0.19	0.37	0.58	0.16	0.25	0.50	0.83
t_f	Output Fall Time, X	0.13	0.18	0.36	0.58	0.16	0.23	0.43	0.69

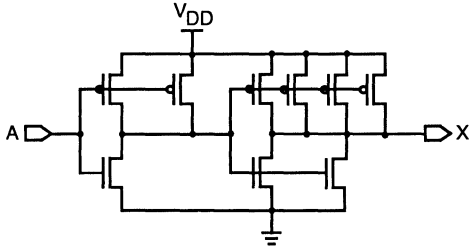
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: BUF2



FUNCTIONAL DIAGRAM: BUF2B



Non-Inverting Buffer
4X Drive
(3.3 V and 5 V Voltage)

BUF4
BUF4B

MACRO	EQUIV. GATES
BUF4	3
BUF4B	5

Rev. 1.07

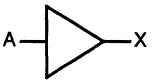
MACRO	OUTPUTS/INPUTS
All	X / A

MACRO	INPUT CAP.
BUF4	A: 0.05pF
BUF4B	A: 0.07pF

FUNCTION TABLE

A	X
L	L
H	H

BUF4



CMOS SWITCHING CHARACTERISTICS

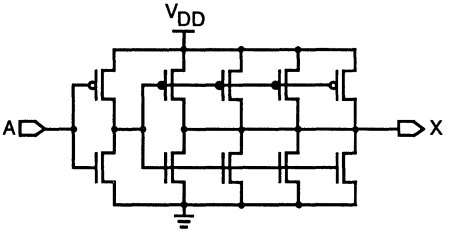
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
BUF4									
t_{PLH}	Propagation Delay,	0.42	0.44	0.51	0.22	0.54	0.57	0.67	0.31
t_{PHL}	A to X	0.45	0.47	0.54	0.21	0.63	0.66	0.74	0.27
t_r	Output Rise Time, X	0.15	0.21	0.39	0.59	0.23	0.31	0.56	0.82
t_f	Output Fall Time, X	0.22	0.25	0.33	0.28	0.29	0.32	0.42	0.33
BUF4B									
t_{PLH}	Propagation Delay,	0.49	0.51	0.55	0.13	0.62	0.64	0.69	0.18
t_{PHL}	A to X	0.38	0.40	0.46	0.20	0.53	0.55	0.63	0.25
t_r	Output Rise Time, X	0.20	0.23	0.31	0.27	0.23	0.27	0.39	0.40
t_f	Output Fall Time, X	0.17	0.20	0.28	0.28	0.24	0.27	0.37	0.32

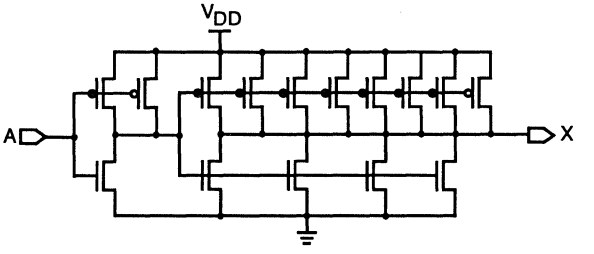
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: BUF4



FUNCTIONAL DIAGRAM: BUF4B



Non-Inverting Buffer 8X Drive (3.3 V and 5 V Voltage)

BUF8
BUF8B

MACRO	EQUIV. GATES
BUF8	5
BUF8B	10

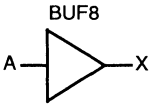
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A

MACRO	INPUT CAP.
BUF8	A: 0.09pF
BUF8B	A: 0.14pF

FUNCTION TABLE

A	X
L	L
H	H



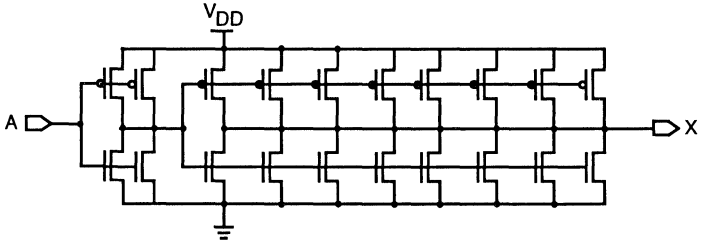
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

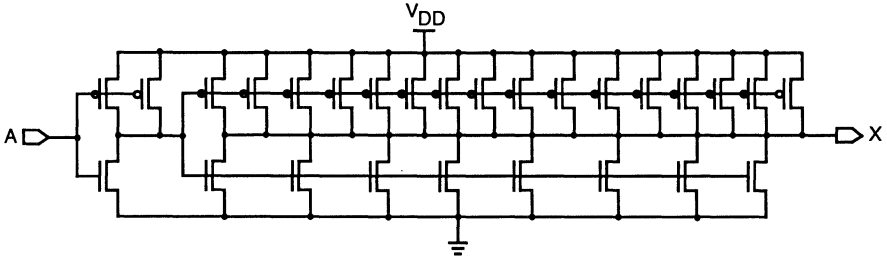
Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
BUF8									
t_{PLH}	Propagation Delay, A to X	0.40	0.41	0.44	0.11	0.51	0.52	0.57	0.17
t_{PHL}		0.41	0.42	0.46	0.12	0.56	0.58	0.62	0.16
t_r	Output Rise Time, X	0.14	0.17	0.26	0.29	0.21	0.25	0.37	0.40
t_f	Output Fall Time, X	0.19	0.20	0.24	0.14	0.25	0.27	0.32	0.17
BUF8B									
t_{PLH}	Propagation Delay, A to X	0.49	0.50	0.52	0.08	0.61	0.62	0.65	0.10
t_{PHL}		0.38	0.39	0.42	0.10	0.51	0.53	0.57	0.14
t_r	Output Rise Time, X	0.20	0.21	0.25	0.14	0.23	0.25	0.31	0.21
t_f	Output Fall Time, X	0.19	0.20	0.24	0.13	0.22	0.24	0.29	0.17

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: BUF8



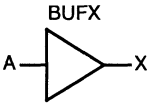
FUNCTIONAL DIAGRAM: BUF8B



7

Non-Inverting Buffer, High Drive (Use Output Buffer From I/O Site) (3.3 V and 5 V Voltage)

BUFX



MACRO	EQUIV. GATES
BUFX	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
BUFX	X / A

MACRO	INPUT CAP.
BUFX	A: 0.18pF

FUNCTION TABLE

A	X
L	L
H	H

CMOS SWITCHING CHARACTERISTICS

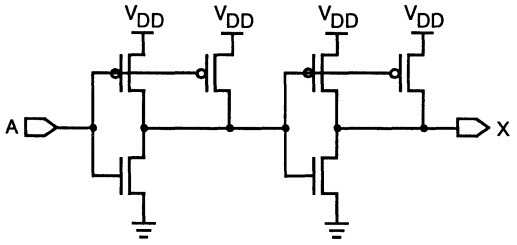
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
BUFX									
t_{PLH}	Propagation Delay,	0.25	0.26	0.27	0.05	0.37	0.38	0.40	0.07
t_{PHL}	A to X	0.32	0.32	0.34	0.07	0.39	0.40	0.43	0.09
t_r	Output Rise Time, X	0.12	0.13	0.16	0.09	0.13	0.15	0.18	0.13
t_f	Output Fall Time, X	0.20	0.21	0.23	0.07	0.20	0.21	0.24	0.11

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: BUFX



4-Bit Decrementer
2X Drive
(3.3 V and 5 V Voltage)

DCR4H

MACRO	EQUIV. GATES
DCR4H	28

Rev. 1.07

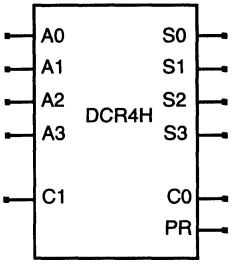
MACRO	OUTPUTS/INPUTS
DCR4H	S0-S3,CO,PR / A0-A3,CI

MACRO	INPUT CAP.
DCR4H	A0-A2: 0.17pF A3: 0.10pF CI: 0.21pF

FUNCTION TABLE

A0-A3	CI	S0-S3	CO	PR
≠ 0	H	A0-A3	H	H
≠ 0	L	(A0-A3)-1	H	H
=0	H	L(All)	H	L
=0	L	H(All)	L	L

NOTE: A0,S0 = LSB, A3,S3 = MSB



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
DCR4H									
t_{PLH}	Propagation Delay, A0 to CO	0.59	0.63	0.76	0.41	0.82	0.88	1.06	0.59
t_{PHL}		1.37	1.41	1.54	0.42	2.00	2.06	2.22	0.53
t_{PLH}	Propagation Delay, A0 to PR	0.36	0.40	0.53	0.41	0.51	0.57	0.74	0.58
t_{PHL}		0.98	1.04	1.19	0.51	1.42	1.49	1.70	0.68
t_{PLH}	Propagation Delay, A0 to S0 & A1 to S1 & A2 to S2 & A3 to S3	0.62	0.66	0.79	0.43	0.89	0.95	1.13	0.60
t_{PHL}		0.71	0.76	0.89	0.44	1.03	1.08	1.25	0.56
t_{PLH}	Propagation Delay, A0 to S1 & A1 to S2	1.00	1.04	1.17	0.42	1.44	1.50	1.68	0.60
t_{PHL}		0.85	0.89	1.02	0.44	1.21	1.26	1.43	0.56
t_{PLH}	Propagation Delay, A0 to S2	1.51	1.55	1.68	0.42	2.20	2.26	2.44	0.60
t_{PHL}		1.18	1.23	1.36	0.44	1.69	1.75	1.92	0.56
t_{PLH}	Propagation Delay, A0 to S3	2.00	2.04	2.17	0.42	2.92	2.98	3.16	0.60
t_{PHL}		1.47	1.51	1.65	0.44	2.09	2.14	2.31	0.57
t_{PLH}	Propagation Delay, A1 to CO	0.61	0.65	0.77	0.42	0.85	0.91	1.09	0.58
t_{PHL}		1.43	1.47	1.59	0.42	2.14	2.20	2.35	0.53
t_{PLH}	Propagation Delay, A1 to PR	0.38	0.43	0.55	0.41	0.54	0.59	0.77	0.59
t_{PHL}		1.05	1.10	1.25	0.51	1.57	1.64	1.84	0.68
t_{PLH}	Propagation Delay, A1 to S3	1.49	1.53	1.66	0.42	1.45	1.51	1.69	0.60
t_{PHL}		1.15	1.19	1.32	0.44	1.24	1.29	1.46	0.56
t_{PLH}	Propagation Delay, A2,A3 to CO	0.62	0.67	0.79	0.41	2.17	2.23	2.41	0.60
t_{PHL}		1.52	1.56	1.68	0.42	1.63	1.68	1.85	0.56
t_{PLH}	Propagation Delay, A2 to PR	0.40	0.44	0.57	0.42	0.87	0.93	1.11	0.58
t_{PHL}		1.10	1.15	1.31	0.51	2.29	2.35	2.51	0.53
t_{PLH}	Propagation Delay, A2 to S3	0.95	0.99	1.12	0.43	0.55	0.61	0.79	0.59
t_{PHL}		0.79	0.83	0.96	0.44	1.71	1.78	1.98	0.68
t_{PLH}	Propagation Delay, A3 to PR	0.40	0.45	0.57	0.42	1.40	1.46	1.64	0.60
t_{PHL}		1.16	1.21	1.36	0.50	1.13	1.19	1.36	0.56
t_{PLH}	Propagation Delay, CI to CO	0.31	0.35	0.47	0.41	0.88	0.94	1.11	0.58
t_{PHL}		0.50	0.54	0.67	0.42	2.34	2.39	2.55	0.53

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

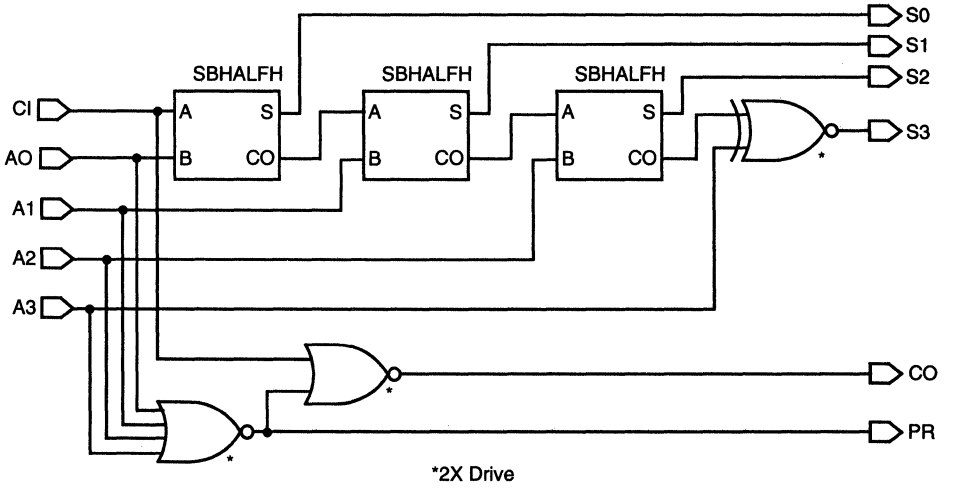
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0ºC (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay, CI to S0	0.46	0.51	0.63	0.42	0.56	0.62	0.80	0.60
t_{PHL}		0.50	0.54	0.67	0.44	1.76	1.83	2.03	0.68
t_{PLH}	Propagation Delay, CI to S1	0.73	0.77	0.90	0.43	0.42	0.48	0.65	0.58
t_{PHL}		0.94	0.99	1.12	0.44	0.71	0.77	0.92	0.53
t_{PLH}	Propagation Delay, CI to S2	1.06	1.10	1.23	0.42	0.68	0.74	0.92	0.59
t_{PHL}		1.47	1.51	1.64	0.44	0.72	0.78	0.95	0.56
t_{PLH}	Propagation Delay, CI to S3	1.35	1.39	1.52	0.43	1.00	1.06	1.24	0.60
t_{PHL}		1.95	1.99	2.13	0.44	1.44	1.49	1.66	0.55
t_r	Output Rise Time, CO	0.13	0.25	0.61	1.21	1.48	1.54	1.72	0.60
t_f	Output Fall Time, CO	0.24	0.30	0.47	0.57	0.31	0.38	0.59	0.70
t_r	Output Rise Time, PR	0.19	0.31	0.67	1.21	0.26	0.43	0.95	1.71
t_f	Output Fall Time, PR	0.54	0.60	0.78	0.58	0.64	0.72	0.94	0.75
t_r	Output Rise Time, S0-S3	0.18	0.30	0.66	1.19				
t_f	Output Fall Time, S0-S3	0.21	0.27	0.45	0.60				
t_r	Output Rise Time, S0,S1,S3					0.21	0.38	0.89	1.70
t_f	Output Fall Time, S0,S1,S3					0.30	0.38	0.59	0.71
t_r	Output Rise Time, S2					0.24	0.41	0.91	1.70
t_f	Output Fall Time, S2					0.31	0.38	0.60	0.73

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: DCR4H



*2X Drive

1 of 4 Decoder
2X Drive
(3.3 V and 5 V Voltage)

DEC4H

MACRO	EQUIV. GATES
DEC4H	9

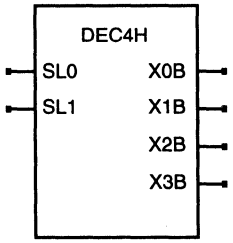
Rev. 1.07

MACRO	OUTPUTS/INPUTS
DEC4H	X0B-X3B / SL0,SL1

MACRO	INPUT CAP.
DEC4H	SL0,SL1: 0.24pF

FUNCTION TABLE

SL1	SL0	X0B	X1B	X2B	X3B
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L



CMOS SWITCHING CHARACTERISTICS

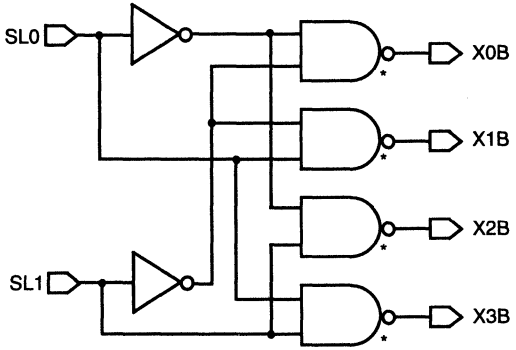
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DEC4H								
t_{PLH}	Propagation Delay,	0.41	0.46	0.58	0.42	0.56	0.62	0.79	0.58
t_{PHL}	SL0 to X0B,X2B	0.48	0.54	0.71	0.58	0.67	0.75	0.98	0.77
t_{PLH}	Propagation Delay,	0.10	0.14	0.27	0.41	0.15	0.21	0.38	0.58
t_{PHL}	SL0 to X1B,X3B	0.25	0.31	0.48	0.57	0.31	0.39	0.61	0.75
t_{PLH}	Propagation Delay,	0.48	0.52	0.65	0.42	0.63	0.69	0.87	0.59
t_{PHL}	SL1 to X0B,X1B	0.50	0.56	0.73	0.57	0.69	0.77	1.00	0.77
t_{PLH}	Propagation Delay,	0.16	0.20	0.32	0.41	0.21	0.27	0.44	0.58
t_{PHL}	SL1 to X2B,X3B	0.24	0.30	0.46	0.55	0.30	0.38	0.60	0.74
t_r	Output Rise Time, X0B-X2B	0.24	0.36	0.72	1.20	0.32	0.49	1.00	1.70
t_f	Output Fall Time, X0B-X2B	0.23	0.33	0.61	0.95	0.30	0.43	0.80	1.23
t_r	Output Rise Time, X3B	0.26	0.37	0.73	1.18	0.32	0.49	0.99	1.69
t_f	Output Fall Time, X3B	0.22	0.31	0.59	0.94	0.26	0.38	0.75	1.23

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: DEC4H



*2X Drive

1 of 4 Decoder, Active High Outputs 2X Drive (3.3 V and 5 V Voltage)

DEC4AH

MACRO	EQUIV. GATES
DEC4AH	14

Rev. 1.07

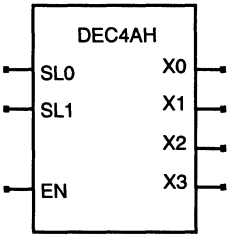
MACRO	OUTPUTS/INPUTS
DEC4AH	X0-X3 / SL0,SL1,EN

MACRO	INPUT CAP.
DEC4AH	EN: 0.20pF SL0,SL1: 0.15pF

FUNCTION TABLE

SL1	SL0	EN	X0	X1	X2	X3
L	L	H	H	L	L	L
L	H	H	L	H	L	L
H	L	H	L	L	H	L
H	H	H	L	L	L	H
X	X	L	L	L	L	L

NOTE:
This macro has common enable on decoder.



CMOS SWITCHING CHARACTERISTICS

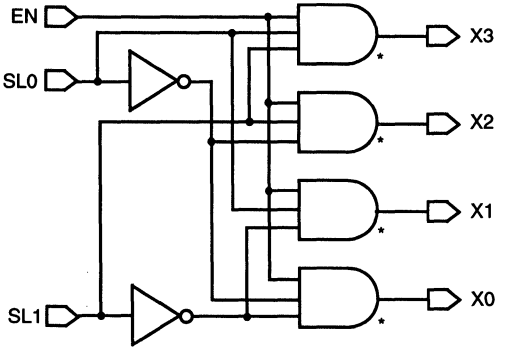
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DEC4AH								
t_{PLH}	Propagation Delay, EN to X0-X3	0.56	0.61	0.74	0.43	0.78	0.84	1.02	0.62
t_{PHL}		0.46	0.50	0.62	0.40	0.66	0.71	0.86	0.50
t_{PLH}	Propagation Delay, SL0 to X0,X2	0.71	0.75	0.88	0.43	0.96	1.02	1.21	0.62
t_{PHL}		0.65	0.68	0.80	0.40	0.89	0.94	1.08	0.49
t_{PLH}	Propagation Delay, SL0 to X1,X3	0.56	0.60	0.73	0.43	0.74	0.80	0.99	0.62
t_{PHL}		0.38	0.42	0.54	0.40	0.57	0.62	0.77	0.48
t_{PLH}	Propagation Delay, SL1 to X0,X1	0.65	0.69	0.82	0.43	0.88	0.94	1.12	0.62
t_{PHL}		0.55	0.59	0.71	0.39	0.78	0.83	0.97	0.48
t_{PLH}	Propagation Delay, SL1 to X2,X3	0.56	0.61	0.74	0.43	0.72	0.78	0.96	0.62
t_{PHL}		0.33	0.37	0.48	0.39	0.49	0.54	0.69	0.48
t_r	Output Rise Time, X0-X3	0.21	0.33	0.68	1.18	0.26	0.43	0.94	1.68
t_f	Output Fall Time, X0-X3	0.23	0.29	0.46	0.57	0.28	0.35	0.56	0.69

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: DEC4AH



*2X Drive for DEC4AH

1 of 8 Decoder, with Enable Active Low Outputs (3.3 V and 5 V Voltage)

DEC1OF8

MACRO	EQUIV. GATES
DEC1OF8	16

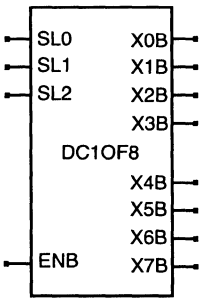
Rev. 1.07

MACRO	OUTPUTS/INPUTS
DEC1OF8	X0B-X7B / SL0-SL2,ENB

MACRO	INPUT CAP.
DEC1OF8	ENB: 0.19pF SL0: 0.16pF SL1: 0.14pF SL2: 0.05pF

FUNCTION TABLE

SL2	SL1	SL0	ENB	X0B	X1B	X2B	X3B	X4B	X5B	X6B	X7B
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L
X	X	X	H	H	H	H	H	H	H	H	H



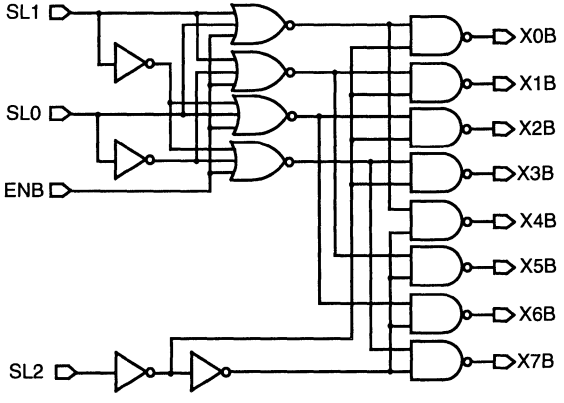
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DEC1OF8								
t_{PLH}	Propagation Delay, ENB to X0B-X7B	0.34	0.42	0.67	0.82	0.49	0.60	0.95	1.16
t_{PHL}		0.83	0.95	1.31	1.20	1.21	1.37	1.85	1.60
t_{PLH}	Propagation Delay, SL0 to X0B,X2B,X4B,X6B	0.37	0.46	0.70	0.83	0.53	0.64	0.99	1.16
t_{PHL}		0.89	1.01	1.37	1.19	1.31	1.47	1.95	1.60
t_{PLH}	Propagation Delay, SL0 to X1B,X3B,X5B,X7B	0.53	0.61	0.86	0.82	0.73	0.85	1.20	1.16
t_{PHL}		1.10	1.22	1.58	1.20	1.61	1.77	2.25	1.61
t_{PLH}	Propagation Delay, SL1 to X0B,X1B,X4B,X5B	0.39	0.47	0.72	0.83	0.55	0.66	1.01	1.17
t_{PHL}		0.91	1.03	1.38	1.19	1.35	1.51	1.99	1.60
t_{PLH}	Propagation Delay, SL1 to X2B,X3B,X6B,X7B	0.57	0.65	0.90	0.83	0.77	0.89	1.24	1.16
t_{PHL}		1.15	1.27	1.63	1.19	1.71	1.87	2.35	1.60
t_{PLH}	Propagation Delay, SL2 to X0B-X3B	0.58	0.66	0.90	0.82	0.75	0.86	1.21	1.16
t_{PHL}		0.59	0.71	1.05	1.15	0.83	0.98	1.44	1.53
t_{PLH}	Propagation Delay, SL2 to X4B-X7B	0.85	0.94	1.18	0.82	1.19	1.30	1.65	1.16
t_{PHL}		0.91	1.02	1.37	1.14	1.22	1.37	1.83	1.52
t_r	Output Rise Time, X0B-X7B	0.26	0.51	1.24	2.45	0.33	0.67	1.71	3.45
t_f	Output Fall Time, X0B-X7B	0.41	0.61	1.19	1.94	0.51	0.76	1.51	2.51

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: DEC1OF8



7

1 of 8 Decoder with Enable Active High Outputs 2X Drive (3.3 V and 5 V Voltage)

DEC8AH

MACRO	EQUIV. GATES
DEC8AH	30

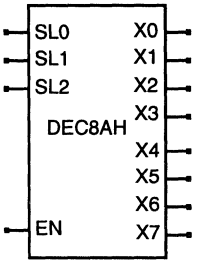
Rev. 1.07

MACRO	OUTPUTS/INPUTS
DEC8AH	X0-X7 / SL0-SL2,EN

MACRO	INPUT CAP.
DEC8AH	EN: 0.39pF SL0-SL2: 0.10pF

FUNCTION TABLE

SL2	SL1	SL0	EN	X0	X1	X2	X3	X4	X5	X6	X7
L	L	L	H	H	L	L	L	L	L	L	L
L	L	H	H	L	H	L	L	L	L	L	L
L	H	L	H	L	L	H	L	L	L	L	L
L	H	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	H	L	L	L
H	L	H	H	L	L	L	L	L	H	L	L
H	H	L	H	L	L	L	L	L	L	H	L
H	H	H	H	L	L	L	L	L	L	L	H
X	X	X	L	L	L	L	L	L	L	L	L



CMOS SWITCHING CHARACTERISTICS

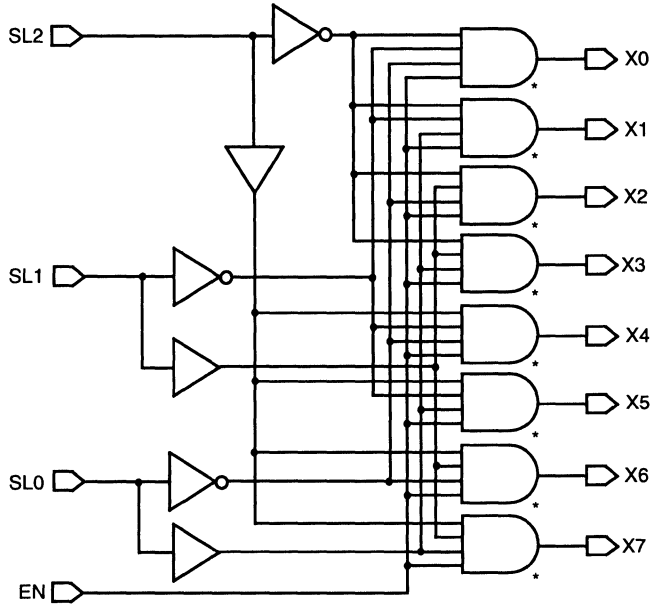
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DEC8AH								
t_{PLH}	Propagation Delay, EN to X0-X7	0.69	0.74	0.87	0.45	0.97	1.04	1.23	0.64
t_{PHL}		0.48	0.52	0.64	0.41	0.70	0.75	0.91	0.51
t_{PLH}	Propagation Delay, SL0 to X0,X2,X4,X6	1.02	1.06	1.20	0.45	1.42	1.48	1.67	0.64
t_{PHL}		0.84	0.88	1.00	0.41	1.16	1.21	1.36	0.50
t_{PLH}	Propagation Delay, SL0 to X1,X3,X5,X7	1.15	1.19	1.33	0.45	1.61	1.68	1.87	0.65
t_{PHL}		0.90	0.94	1.06	0.41	1.23	1.28	1.43	0.50
t_{PLH}	Propagation Delay, SL1 to X0,X1,X4,X5	0.94	0.99	1.12	0.45	1.31	1.37	1.56	0.64
t_{PHL}		0.75	0.79	0.91	0.39	1.05	1.09	1.24	0.49
t_{PLH}	Propagation Delay, SL1 to X2,X3,X6,X7	1.06	1.10	1.24	0.45	1.48	1.55	1.74	0.65
t_{PHL}		0.80	0.84	0.96	0.40	1.10	1.15	1.29	0.50
t_{PLH}	Propagation Delay, SL2 to X0-X3	0.84	0.88	1.02	0.45	1.15	1.21	1.41	0.64
t_{PHL}		0.63	0.67	0.79	0.39	0.88	0.93	1.07	0.49
t_{PLH}	Propagation Delay, SL2 to X4-X7	1.01	1.05	1.19	0.46	1.40	1.47	1.66	0.65
t_{PHL}		0.73	0.77	0.89	0.40	1.01	1.06	1.21	0.48
t_r	Output Rise Time, X0-X7	0.26	0.37	0.73	1.18				
t_f	Output Fall Time, X0-X7	0.28	0.33	0.50	0.56				
t_r	Output Rise Time, X0,X2,X4,X6					0.32	0.49	0.99	1.68
t_f	Output Fall Time, X0,X2,X4,X6					0.30	0.37	0.57	0.68
t_r	Output Rise Time, X1,X3,X5,X7					0.35	0.52	1.03	1.68
t_f	Output Fall Time, X1,X3,X5,X7					0.30	0.37	0.57	0.68

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: DEC8AH



*2X Drive

7

Scan D Flip Flop (3.3 V and 5 V Core Voltage)

DFF1A

MACRO	EQUIV. GATES
DFF1A	15

Rev. 1.07

MACRO	OUTPUTS/INPUTS
DFF1A	Q,SQ / D,CK,SD,SE,E1,E2

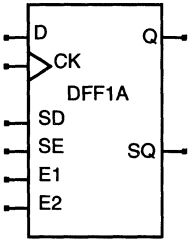
MACRO	INPUT CAP.
DFF1A	CK,E1,E2: 0.05pF D: 0.15pF SD: 0.21pF SE: 0.10pF

FUNCTIONAL DESCRIPTION:

DFF1A is a redesign of the DFF1 to enhance routability.

FUNCTION TABLE

D	CK	SD	SE	E1	E2	Q	SQ	MODE
L	↗	X	L	H	H	L	L	NORMAL
H	↗	X	L	H	H	H	H	
X	↗	L	H	X	X	L	L	SCAN
X	↗	H	H	X	X	H	H	
X	↗	X	L	L	X	Q	SQ	HOLD OR
X	↗	X	L	X	L	Q	SQ	DISABLE



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFF1A								
t_{PLH}	Propagation Delay, CK to Q	0.79	0.83	0.96	0.43	1.10	1.17	1.35	0.61
t_{PHL}		0.77	0.82	0.96	0.46	1.13	1.19	1.36	0.60
t_{PLH}	Propagation Delay, CK to SQ	1.34	1.42	1.67	0.82	1.91	2.02	2.37	1.16
t_{PHL}		1.35	1.42	1.65	0.76	1.95	2.05	2.32	0.92
t_r	Output Rise Time, Q	0.18	0.30	0.65	1.19	0.22	0.39	0.90	1.69
t_f	Output Fall Time, Q	0.25	0.31	0.48	0.60	0.35	0.42	0.64	0.73
t_r	Output Rise Time, SQ	0.15	0.40	1.12	2.43	0.19	0.53	1.57	3.44
t_f	Output Fall Time, SQ	0.15	0.26	0.61	1.17	0.21	0.35	0.77	1.40

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

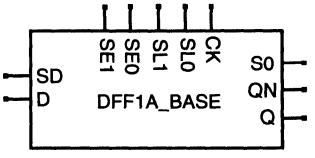
7

CMOS TIMING REQUIREMENTS

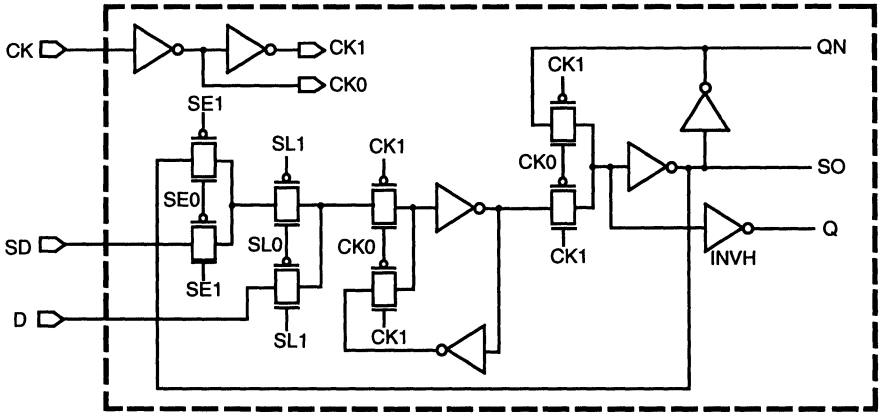
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V Minimum Requirement	3.3 V Minimum Requirement
	DFF1A		
t_{su}	Set Up Time, D to CK	0.32	0.57
t_{su}	Set Up Time, E1 to CK	1.03	1.51
t_{su}	Set Up Time, E2 to CK	1.01	1.47
t_{su}	Set Up Time, SD to CK	0.55	0.98
t_{su}	Set Up Time, SE to CK	0.94	1.38
t_h	Hold Time, CK to D	0.36	0.48
t_h	Hold Time, CK to E1	-0.29	-0.44
t_h	Hold Time, CK to E2	-0.25	-0.39
t_h	Hold Time, CK to SD	0.19	0.21
t_h	Hold Time, CK to SE	-0.04	-0.09
t_w	Pulse Width, CK(L)	0.68	1.06
t_w	Pulse Width, CK(H)	1.00	1.46
t_{per}	Min Period, CK	1.62	2.41

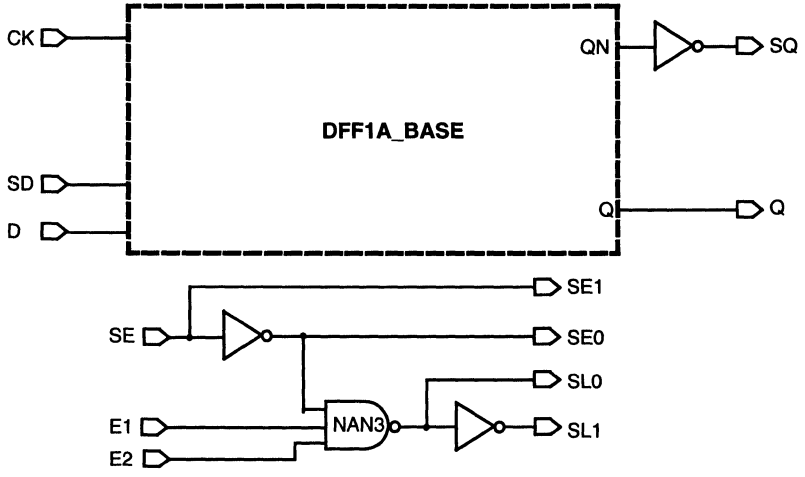
SYMBOL: DFF1A_BASE



FUNCTIONAL DIAGRAM: DFF1A_BASE



FUNCTIONAL DIAGRAM: DFF1A



7

4-Bit Scan D Flip Flop (3.3 V and 5 V Core Voltage)

DFF4A

MACRO	EQUIV. GATES
DFF4A	48

Rev. 1.07

MACRO	OUTPUTS/INPUTS
DFF4A	Q0-Q3,SQ3 / D0-D3,CK,SD0,SE,E1,E2

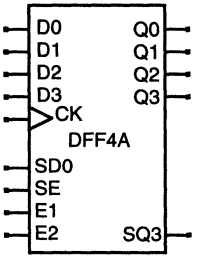
MACRO	INPUT CAP.
DFF4A	CK: 0.21pF D0-D3,SD0: 0.15pF E1,E2: 0.05pF SE: 0.27pF

FUNCTIONAL DESCRIPTION:

DFF4A is a redesign of the DFF4 to enhance routability.

FUNCTION TABLE

D0-D3	CK	SD0	SE	E1	E2	Q0-Q3	SQ3	MODE
L	↗	X	L	H	H	L	L	NORMAL
H	↗	X	L	H	H	H	H	
X	↗	L	H	X	X	L,Qn-1	Q2	SCAN
X	↗	H	H	X	X	H,Qn-1	Q2	
X	↗	X	L	L	X	Qn	SQ3	HOLD OR
X	↗	X	L	X	L	Qn	SQ3	DISABLE



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFF4A								
t_{PLH}	Propagation Delay, CK to Q0-Q3	0.79	0.83	0.96	0.43	1.11	1.17	1.35	0.61
t_{PHL}		0.78	0.82	0.96	0.46	1.13	1.19	1.37	0.60
t_{PLH}	Propagation Delay, CK to SQ3	1.34	1.43	1.67	0.82	1.92	2.03	2.38	1.16
t_{PHL}		1.35	1.43	1.65	0.76	1.94	2.03	2.30	0.91
t_r	Output Rise Time, Q0-Q3	0.18	0.30	0.66	1.19	0.22	0.39	0.90	1.69
t_f	Output Fall Time, Q0-Q3	0.26	0.32	0.50	0.59	0.36	0.43	0.65	0.73
t_r	Output Rise Time, SQ3	0.15	0.40	1.13	2.43	0.19	0.53	1.56	3.44
t_f	Output Fall Time, SQ3	0.13	0.25	0.60	1.18	0.19	0.33	0.76	1.41

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

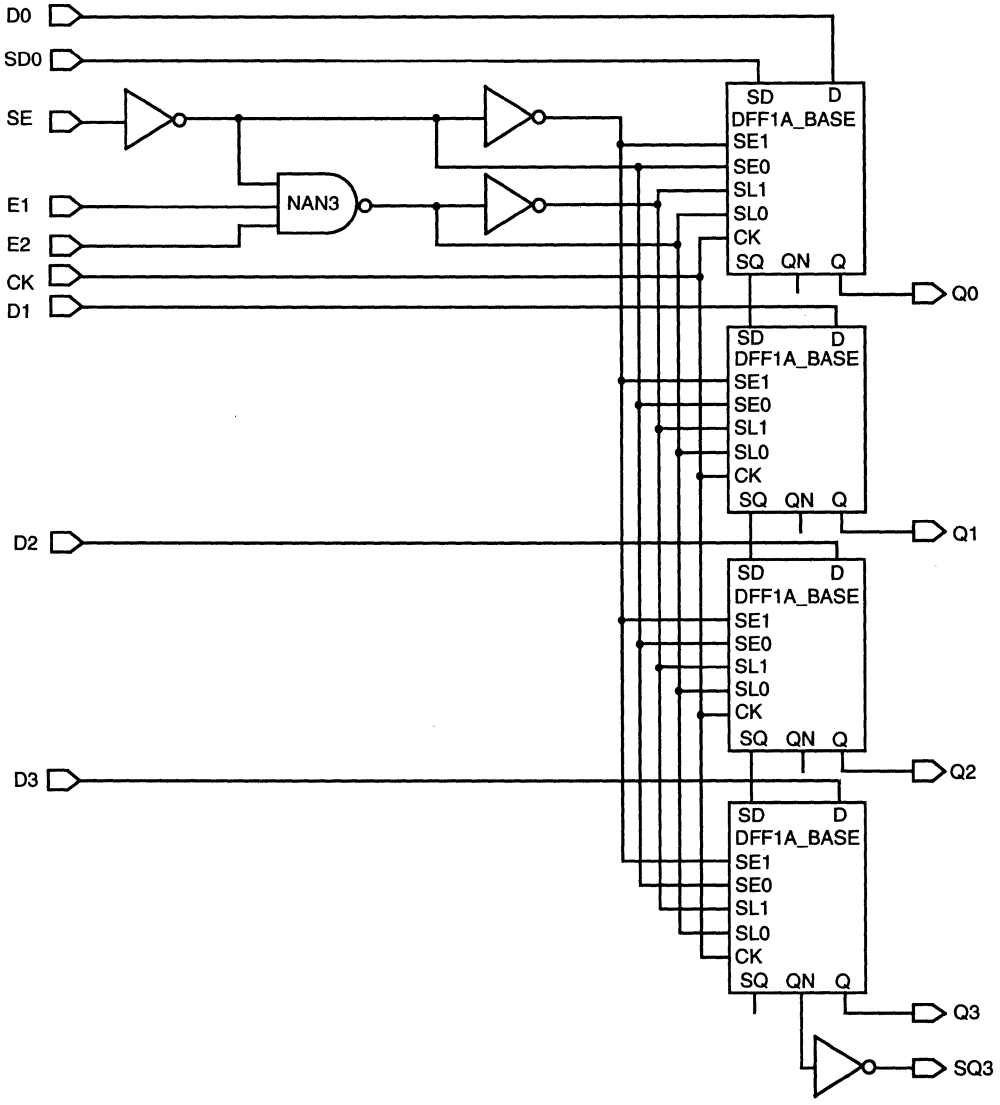
7

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V	3.3 V
		Minimum Requirement	Minimum Requirement
	DFF4A		
t_{su}	Set Up Time, D0-D3 to CK	0.32	0.57
t_{su}	Set Up Time, E1,E2 to CK	1.57	2.27
t_{su}	Set Up Time, SD0 to CK	0.55	0.98
t_{su}	Set Up Time, SE to CK	1.11	1.62
t_h	Hold Time, CK to D0-D3	0.36	0.47
t_h	Hold Time, CK to E1	-0.77	-1.12
t_h	Hold Time, CK to E2	-0.82	-1.20
t_h	Hold Time, CK to SD0	0.19	0.21
t_h	Hold Time, CK to SE	-0.15	-0.22
t_w	Pulse Width, CK(L)	0.68	1.05
t_w	Pulse Width, CK(H)	0.97	1.44
t_{per}	Min Period, CK	1.59	2.39

FUNCTIONAL DIAGRAM: DFF4A



D Flip Flop, Multiplexed (or Scan) Input with HOLD Function (3.3 V and 5 V Core Voltage)

DFFGLP

MACRO	EQUIV. GATES
DFFGLP	13

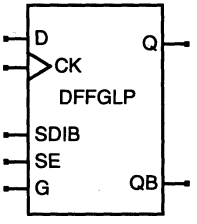
Rev. 1.07

MACRO	OUTPUTS/INPUTS
DFFGLP	Q,QB / D,CK,SDIB,SE,G

MACRO	INPUT CAP.
DFFGLP	CK,D,SDIB: 0.05pF G,SE: 0.10pF

FUNCTION TABLE

D	SDIB	SE	CK	G	Qn+1	QBn+1
X	L	H	↑	X	H	L
X	H	H	↑	X	L	H
L	X	L	↑	H	L	H
H	X	L	↑	H	H	L
X	X	L	↑	L	Qn	QBn



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFGLP								
t_{PLH}	Propagation Delay, CK to Q	0.81	0.86	0.99	0.44	1.10	1.17	1.35	0.62
t_{PHL}		0.90	0.98	1.22	0.80	1.23	1.33	1.64	1.01
t_{PLH}	Propagation Delay, CK to QB	1.26	1.34	1.59	0.82	1.73	1.84	2.19	1.15
t_{PHL}		1.37	1.44	1.67	0.76	1.92	2.01	2.28	0.90
t_r	Output Rise Time, Q	0.23	0.34	0.69	1.15	0.32	0.49	1.00	1.71
t_f	Output Fall Time, Q	0.31	0.43	0.77	1.14	0.36	0.52	1.00	1.58
t_r	Output Rise Time, QB	0.13	0.38	1.12	2.47	0.20	0.54	1.58	3.46
t_f	Output Fall Time, QB	0.09	0.22	0.62	1.31	0.16	0.31	0.77	1.51

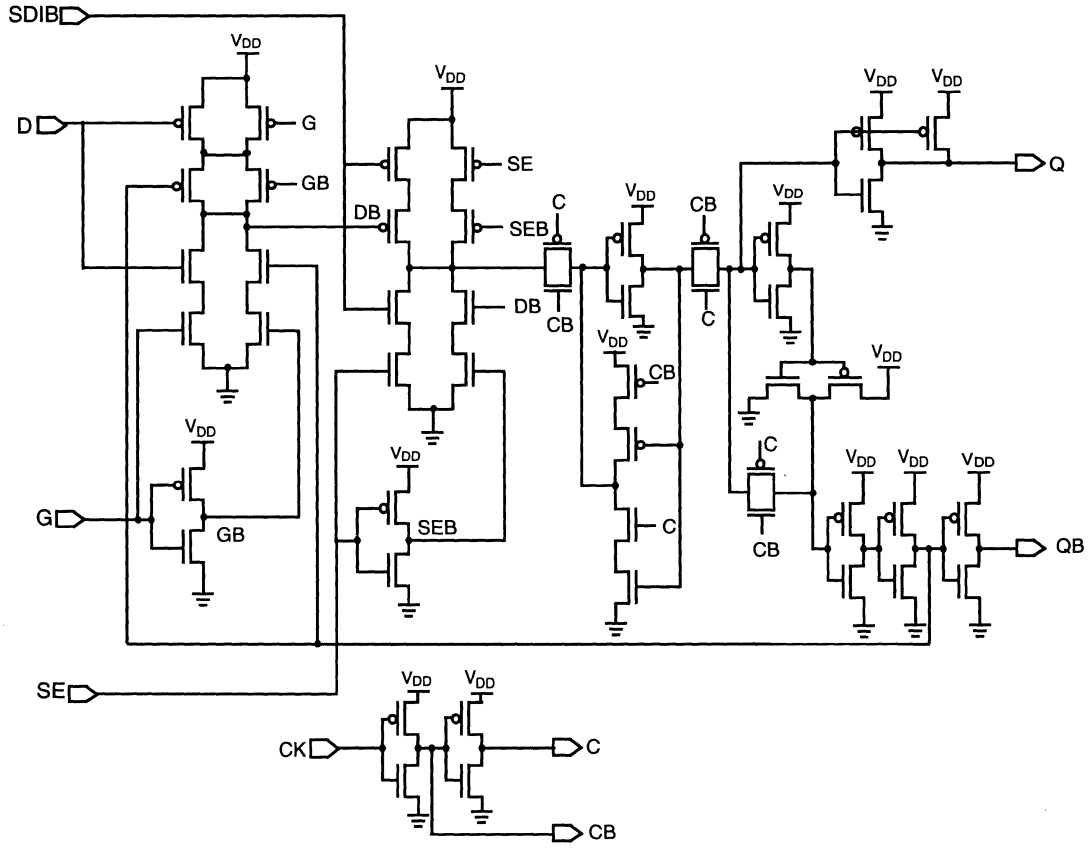
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V Minimum Requirement	3.3 V Minimum Requirement
	DFFGLP		
t_{su}	Set Up Time, D to CK	1.01	1.59
t_{su}	Set Up Time, G to CK	0.96	1.53
t_{su}	Set Up Time, SDIB to CK	0.53	0.82
t_{su}	Set Up Time, SE to CK	0.61	1.09
t_h	Hold Time, CK to D	-0.20	-0.34
t_h	Hold Time, CK to G	-0.32	-0.51
t_h	Hold Time, CK to SDIB	0.15	0.11
t_h	Hold Time, CK to SE	0.01	0.02
t_w	Pulse Width, CK(L)	0.35	0.65
t_w	Pulse Width, CK(H)	0.58	0.90

FUNCTIONAL DIAGRAM: DFFGLP



D Flip Flop, Multiplexed (or Scan) Input 1X & 2X Drive (3.3 V and 5 V Core Voltage)

DFFLPA
DFFLPAH

MACRO	EQUIV. GATES
DFFLPA	8
DFFLPAH	9

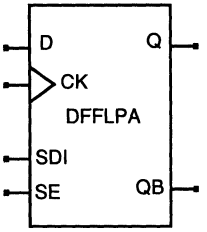
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	Q,QB / D,CK,SDI,SE

MACRO	INPUT CAP.
All	CK: 0.14pF D,SDI: 0.05pF SE: 0.09pF

FUNCTIONAL DECRIPTION:

This macro matches the functionality of the DFFLP & DFFLPH (respectively). The layout has been modified to reduce gate count and increase performance. All inputs including CK are unbuffered.



FUNCTION TABLE

D	SDI	SE	CK	Q	QB
L	X	L	↑	L	H
H	X	L	↑	H	L
X	L	H	↑	L	H
X	H	H	↑	H	L

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFLPA								
t_{PLH}	Propagation Delay, CK to Q	0.64	0.72	0.97	0.83	0.90	1.02	1.37	1.16
t_{PHL}		0.56	0.64	0.87	0.77	0.80	0.89	1.17	0.93
t_{PLH}	Propagation Delay, CK to QB	0.70	0.78	1.03	0.83	0.99	1.10	1.45	1.16
t_{PHL}		0.84	0.92	1.15	0.76	1.23	1.32	1.59	0.92
t_r	Output Rise Time, Q	0.13	0.37	1.10	2.44	0.18	0.53	1.56	3.44
t_f	Output Fall Time, Q	0.14	0.25	0.61	1.18	0.20	0.34	0.77	1.41
t_r	Output Rise Time, QB	0.13	0.37	1.10	2.44	0.16	0.51	1.55	3.46
t_f	Output Fall Time, QB	0.14	0.25	0.61	1.18	0.21	0.35	0.77	1.40
	DFFLPAH								
t_{PLH}	Propagation Delay, CK to Q	0.67	0.71	0.84	0.43	0.94	1.00	1.18	0.59
t_{PHL}		0.60	0.64	0.76	0.41	0.85	0.90	1.05	0.50
t_{PLH}	Propagation Delay, CK to QB	0.82	0.86	0.98	0.41	1.13	1.19	1.37	0.58
t_{PHL}		0.94	0.98	1.10	0.40	1.35	1.40	1.55	0.49
t_r	Output Rise Time, Q	0.16	0.28	0.64	1.19	0.21	0.38	0.88	1.68
t_f	Output Fall Time, Q	0.16	0.22	0.39	0.57	0.24	0.31	0.51	0.68
t_r	Output Rise Time, QB	0.11	0.23	0.59	1.21	0.17	0.34	0.85	1.70
t_f	Output Fall Time, QB	0.16	0.21	0.38	0.56	0.21	0.28	0.49	0.69

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

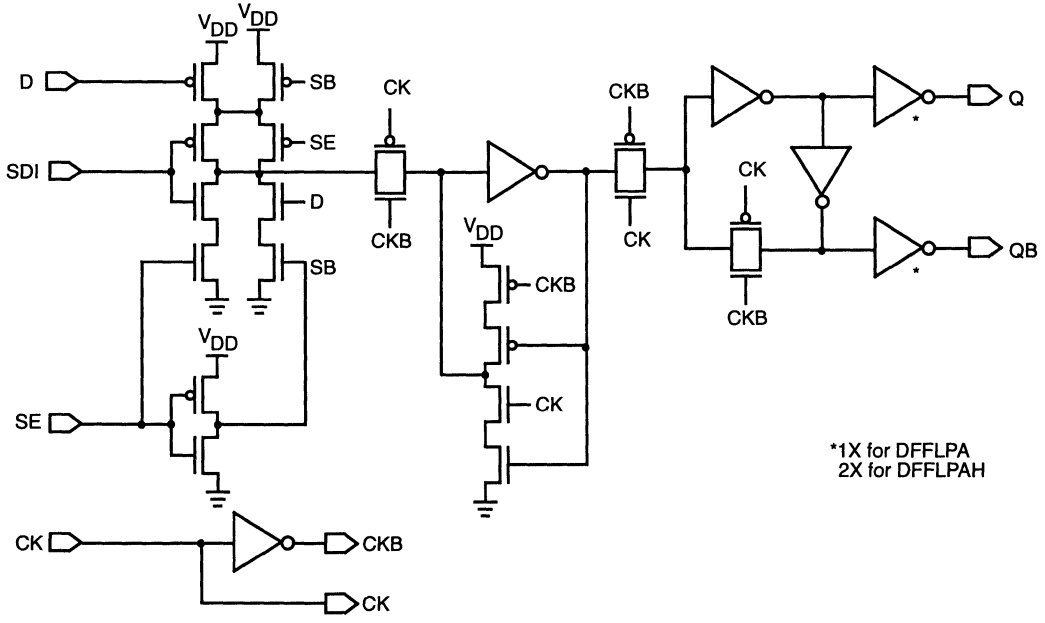
Sym	Parameter	5 V	3.3 V
		Minimum Requirement	Minimum Requirement
	DFFLPA		
t_{su}	Set Up Time, D to CK	0.66	1.03
t_{su}	Set Up Time, SDI to CK	0.71	1.09
t_{su}	Set Up Time, SE to CK	0.79	1.23
t_h	Hold Time, CK to D	-0.23	-0.22
t_h	Hold Time, CK to SDI	-0.23	-0.26

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V Minimum Requirement	3.3 V Minimum Requirement
t_h	Hold Time, CK to SE	-0.27	-0.29
t_w	Pulse Width, CK(L)	0.44	0.67
t_w	Pulse Width, CK(H)	0.52	0.76
	DFFLPAH		
t_{su}	Set Up Time, D to CK	0.66	1.03
t_{su}	Set Up Time, SDI to CK	0.71	1.09
t_{su}	Set Up Time, SE to CK	0.79	1.23
t_h	Hold Time, CK to D	-0.23	-0.22
t_h	Hold Time, CK to SDI	-0.23	-0.26
t_h	Hold Time, CK to SE	-0.27	-0.29
t_w	Pulse Width, CK(L)	0.44	0.67
t_w	Pulse Width, CK(H)	0.63	0.89

FUNCTIONAL DIAGRAM: DFFLPA



7

D Flip Flop
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

DFFP
DFFPH

MACRO	EQUIV. GATES
All	8

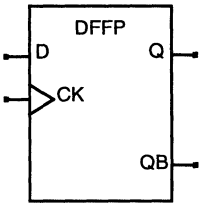
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	Q,QB / D,CK

MACRO	INPUT CAP.
All	CK,D: 0.05pF

FUNCTION TABLE

D	CK	Q	QB
L	↑	L	H
H	↑	H	L
X	↓	Q	QB



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFP								
t_{PLH}	Propagation Delay, CK to Q	0.85	0.94	1.18	0.82	1.19	1.30	1.65	1.16
t_{PHL}		0.95	1.03	1.26	0.76	1.37	1.47	1.74	0.92
t_{PLH}	Propagation Delay, CK to QB	1.08	1.16	1.41	0.83	1.54	1.66	2.00	1.16
t_{PHL}		1.05	1.12	1.35	0.76	1.49	1.58	1.85	0.91
t_r	Output Rise Time, Q	0.14	0.38	1.11	2.44	0.18	0.53	1.56	3.45
t_f	Output Fall Time, Q	0.14	0.26	0.61	1.18	0.21	0.35	0.78	1.41
t_r	Output Rise Time, QB	0.13	0.37	1.10	2.44	0.16	0.51	1.55	3.45
t_f	Output Fall Time, QB	0.12	0.24	0.59	1.18	0.18	0.32	0.75	1.42
	DFFPH								
t_{PLH}	Propagation Delay, CK to Q	0.90	0.94	1.07	0.42	1.24	1.30	1.48	0.59
t_{PHL}		1.00	1.04	1.16	0.40	1.45	1.50	1.64	0.49
t_{PLH}	Propagation Delay, CK to QB	1.20	1.24	1.37	0.41	1.71	1.77	1.95	0.58
t_{PHL}		1.15	1.19	1.31	0.40	1.63	1.68	1.82	0.48
t_r	Output Rise Time, Q	0.19	0.31	0.66	1.19	0.25	0.41	0.92	1.68
t_f	Output Fall Time, Q	0.19	0.24	0.41	0.57	0.27	0.34	0.54	0.67
t_r	Output Rise Time, QB	0.16	0.28	0.64	1.20	0.22	0.39	0.90	1.69
t_f	Output Fall Time, QB	0.16	0.22	0.39	0.57	0.22	0.29	0.49	0.69

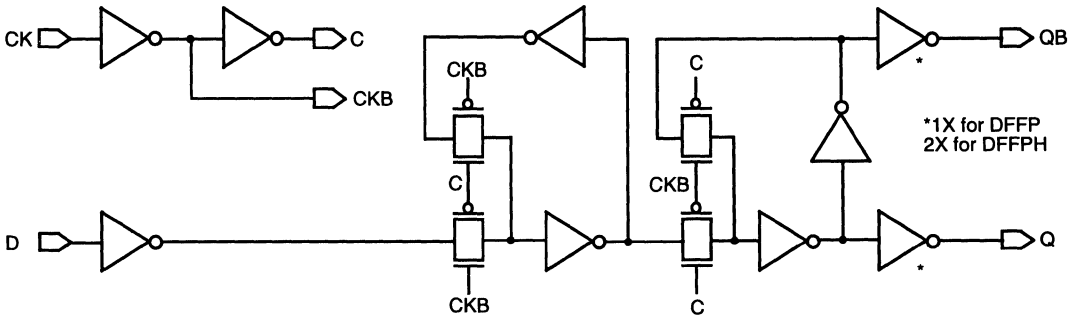
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V Minimum Requirement	3.3 V Minimum Requirement
	DFFP		
t_{su}	Set Up Time, D to CK	0.27	0.45
t_h	Hold Time, CK to D	0.25	0.35
t_w	Pulse Width, CK(L)	0.57	0.88
t_w	Pulse Width, CK(H)	0.76	1.13
	DFFPH		
t_{su}	Set Up Time, D to CK	0.27	0.45
t_h	Hold Time, CK to D	0.25	0.35
t_w	Pulse Width, CK(L)	0.57	0.89
t_w	Pulse Width, CK(H)	0.88	1.28

FUNCTIONAL DIAGRAM: DFFP



7

D Flip Flop with Reset
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

DFFRP
DFFRPH

MACRO	EQUIV. GATES
DFFRP	8
DFFRPH	10

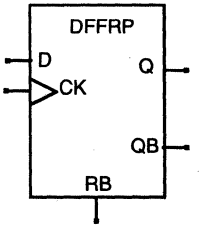
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	Q,QB / RB,D,CK

MACRO	INPUT CAP.
All	CK,D: 0.05pF RB: 0.10pF

FUNCTION TABLE

D	CK	RB	Q	QB
L	↗	H	L	H
H	↗	H	H	L
X	↘	H	Q	QB
X	X	L	L	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFRP								
t_{PLH}	Propagation Delay, CK to Q	0.90	0.98	1.23	0.83	1.23	1.35	1.70	1.17
t_{PHL}		0.91	0.99	1.22	0.77	1.32	1.41	1.69	0.92
t_{PLH}	Propagation Delay, CK to QB	1.05	1.13	1.38	0.83	1.51	1.62	1.97	1.16
t_{PHL}		1.11	1.19	1.41	0.76	1.56	1.66	1.93	0.92
t_{PHL}	Propagation Delay, RB to Q	0.40	0.47	0.70	0.76	0.57	0.67	0.94	0.93
t_{PLH}	Propagation Delay, RB to QB	0.55	0.63	0.88	0.82	0.77	0.88	1.23	1.16
t_r	Output Rise Time, Q	0.18	0.42	1.15	2.42	0.23	0.58	1.60	3.42
t_f	Output Fall Time, Q	0.17	0.29	0.64	1.17	0.21	0.36	0.78	1.41
t_r	Output Rise Time, QB	0.13	0.37	1.11	2.44	0.18	0.52	1.56	3.45
t_f	Output Fall Time, QB	0.14	0.26	0.61	1.17	0.21	0.35	0.77	1.40
	DFFRPH								
t_{PLH}	Propagation Delay, CK to Q	0.95	1.00	1.12	0.43	1.30	1.36	1.54	0.61
t_{PHL}		0.96	1.00	1.12	0.40	1.39	1.44	1.59	0.49
t_{PLH}	Propagation Delay, CK to QB	1.18	1.22	1.34	0.41	1.67	1.72	1.90	0.58
t_{PHL}		1.24	1.28	1.40	0.40	1.73	1.78	1.93	0.49
t_{PHL}	Propagation Delay, RB to Q	0.45	0.49	0.61	0.40	0.63	0.68	0.83	0.50
t_{PLH}	Propagation Delay, RB to QB	0.66	0.71	0.83	0.41	0.93	0.99	1.16	0.59
t_r	Output Rise Time, Q	0.20	0.32	0.68	1.19	0.29	0.45	0.96	1.68
t_f	Output Fall Time, Q	0.21	0.27	0.44	0.56	0.27	0.34	0.54	0.68
t_r	Output Rise Time, QB	0.16	0.28	0.64	1.20	0.24	0.41	0.93	1.70
t_f	Output Fall Time, QB	0.18	0.24	0.41	0.57	0.26	0.32	0.53	0.68

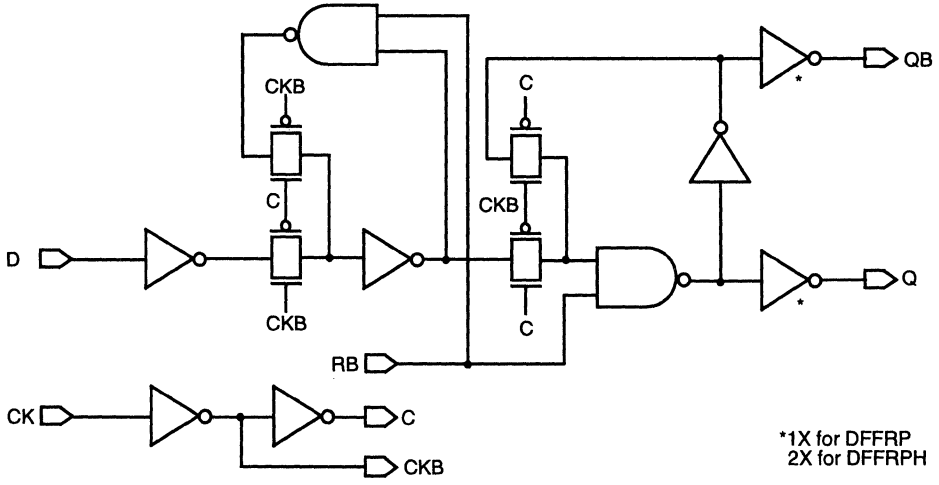
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V Minimum Requirement	3.3 V Minimum Requirement
	DFFRP		
t_{su}	Set Up Time, D to CK	0.42	0.63
t_h	Hold Time, CK to D	0.22	0.31
t_{rec}	Recovery Time, RB to CK	-0.08	-0.11
t_w	Pulse Width, CK (L)	0.65	1.00
t_w	Pulse Width, CK(H)	0.73	1.09
t_w	Pulse Width, RB(L)	0.65	0.88
t_w	Pulse Width, RB(H)	0.03	0.04
	DFFRPH		
t_{su}	Set Up Time, D to CK	0.42	0.63
t_h	Hold Time, CK to D	0.22	0.31
t_{rec}	Recovery Time, RB to CK	-0.09	-0.11
t_w	Pulse Width, CK(L)	0.65	1.00
t_w	Pulse Width, CK(H)	0.85	1.24
t_w	Pulse Width, RB(L)	0.73	1.00
t_w	Pulse Width, RB(H)	0.04	0.05

FUNCTIONAL DIAGRAM: DFFRP



7

D Flip Flop with Reset Multiplexed (or Scan) Input 1X & 2X Drive (3.3 V and 5 V Core Voltage)

DFFRLP
DFFRLPH

MACRO	EQUIV. GATES
All	11

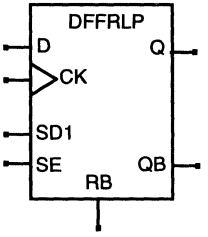
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	Q,QB / D,CK,SDI,SE,RB

MACRO	INPUT CAP.
All	CK,D,SDI: 0.05pF RB,SE: 0.10pF

FUNCTION TABLE

D	SDI	SE	CK	RB	Q	QB
L	X	L	↑	H	L	H
H	X	L	↑	H	H	L
X	L	H	↑	H	L	H
X	H	H	↑	H	H	L
X	X	X	↓	H	Q	QB
X	X	X	X	L	L	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFRLP								
t_{PLH}	Propagation Delay, CK to Q	0.94	1.02	1.27	0.83	1.31	1.43	1.78	1.17
t_{PHL}		1.05	1.12	1.35	0.77	1.50	1.60	1.87	0.93
t_{PLH}	Propagation Delay, CK to QB	1.14	1.23	1.47	0.83	1.63	1.75	2.09	1.16
t_{PHL}		1.09	1.17	1.40	0.76	1.54	1.64	1.91	0.91
t_{PHL}	Propagation Delay, RB to Q	0.33	0.41	0.64	0.76	0.50	0.59	0.87	0.92
t_{PLH}	Propagation Delay, RB to QB	0.44	0.52	0.77	0.83	0.63	0.74	1.09	1.16
t_r	Output Rise Time, Q	0.18	0.42	1.15	2.42	0.23	0.57	1.60	3.42
t_f	Output Fall Time, Q	0.16	0.28	0.63	1.17	0.20	0.34	0.77	1.42
t_r	Output Rise Time, QB	0.12	0.37	1.10	2.45	0.17	0.52	1.55	3.45
t_f	Output Fall Time, QB	0.12	0.24	0.59	1.18	0.17	0.31	0.74	1.42
	DFFRLPH								
t_{PLH}	Propagation Delay, CK to Q	0.99	1.04	1.16	0.43	1.37	1.43	1.62	0.60
t_{PHL}		1.11	1.15	1.26	0.40	1.57	1.62	1.77	0.50
t_{PLH}	Propagation Delay, CK to QB	1.26	1.30	1.43	0.41	1.80	1.86	2.03	0.58
t_{PHL}		1.23	1.27	1.39	0.39	1.74	1.79	1.93	0.47
t_{PHL}	Propagation Delay, RB to Q	0.39	0.43	0.55	0.40	0.57	0.62	0.77	0.49
t_{PLH}	Propagation Delay, RB to QB	0.57	0.62	0.74	0.41	0.79	0.85	1.03	0.58
t_r	Output Rise Time, Q	0.19	0.31	0.67	1.20	0.27	0.44	0.94	1.69
t_f	Output Fall Time, Q	0.24	0.29	0.46	0.56	0.27	0.34	0.54	0.68
t_r	Output Rise Time, QB	0.17	0.29	0.66	1.21	0.19	0.36	0.88	1.71
t_f	Output Fall Time, QB	0.15	0.21	0.38	0.57	0.23	0.30	0.50	0.68

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

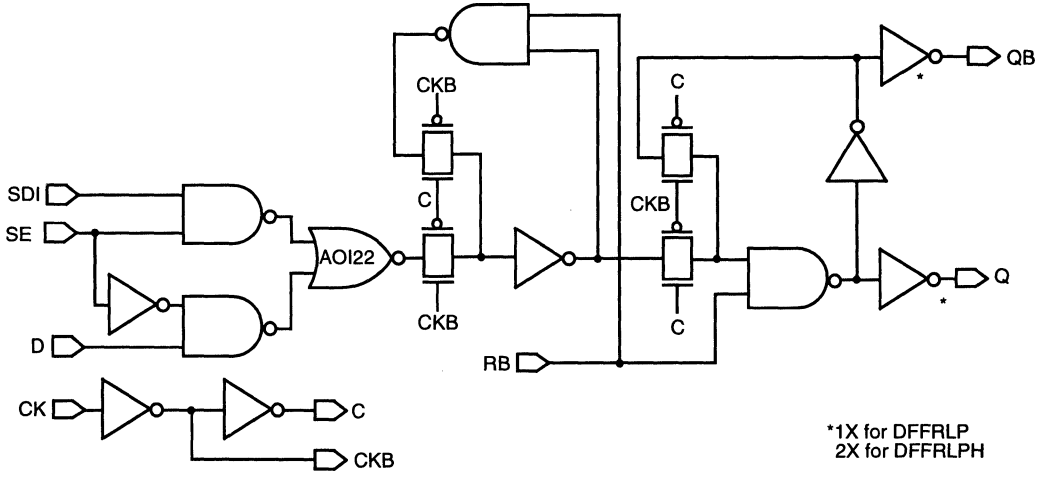
CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V Minimum Requirement	3.3 V Minimum Requirement
	DFFRLP		
t_{su}	Set Up Time, D to CK	0.67	1.10
t_{su}	Set Up Time, SDI to CK	0.70	1.15
t_{su}	Set Up Time, SE to CK	0.73	1.15
t_h	Hold Time, CK to D	0.11	0.16
t_h	Hold Time, CK to SDI	0.05	0.11
t_h	Hold Time, CK to SE	0.08	0.16
t_{rec}	Recovery Time, RB to CK	-0.13	-0.16
t_w	Pulse Width, CK(L)	0.67	1.07
t_w	Pulse Width, CK(H)	0.81	1.18
t_w	Pulse Width, RB(L)	0.62	0.88
t_w	Pulse Width, RB(H)	0.03	0.04
	DFFRLPH		
t_{su}	Set Up Time, D to CK	0.67	1.11
t_{su}	Set Up Time, SDI to CK	0.70	1.15
t_{su}	Set Up Time, SE to CK	0.73	1.15
t_h	Hold Time, CK to D	0.11	0.16
t_h	Hold Time, CK to SDI	0.05	0.10
t_h	Hold Time, CK to SE	0.08	0.16
t_{rec}	Recovery Time, RB to CK	-0.13	-0.16
t_w	Pulse Width, CK (L)	0.66	1.07
t_w	Pulse Width, CK(H)	0.93	1.34
t_w	Pulse Width, RB(L)	0.66	0.93
t_w	Pulse Width, RB(H)	0.03	0.04

7

FUNCTIONAL DIAGRAM: DFFRLP



*1X for DFFRLP
2X for DFFRLPH

D Flip Flop with Set and Reset 2X Drive (3.3 V and 5 V Core Voltage)

DFFRSPHB

MACRO	EQUIV. GATES
DFFRSPHB	10.0

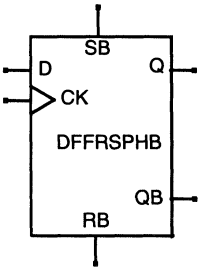
Rev. 1.07

MACRO	OUTPUTS/INPUTS
DFFRSPHB	Q,QB / SB,D,CK,RB

MACRO	INPUT CAP.
DFFRSPHB	CK,D: 0.05pF RB,SB: 0.09pF

FUNCTION TABLE

D	CK	RB	SB	Q	QB
L	↑	H	H	L	H
H	↑	H	H	H	L
X	↓	H	H	Q	QB
X	X	L	H	L	H
X	X	H	L	H	L
X	X	L	L	L	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFRSPHB								
t_{PLH}	Propagation Delay, CK to Q	0.91	0.96	1.08	0.43	1.27	1.33	1.51	0.60
t_{PHL}		1.03	1.07	1.19	0.38	1.52	1.57	1.71	0.47
t_{PLH}	Propagation Delay, CK to QB	1.33	1.37	1.50	0.42	1.92	1.98	2.16	0.59
t_{PHL}		1.24	1.28	1.39	0.37	1.78	1.82	1.96	0.46
t_{PLH}	Propagation Delay, RB to Q	0.50	0.54	0.67	0.43	0.67	0.73	0.90	0.60
t_{PHL}		0.38	0.42	0.53	0.37	0.56	0.60	0.74	0.46
t_{PLH}	Propagation Delay, RB to QB	0.67	0.71	0.84	0.43	0.96	1.02	1.20	0.59
t_{PLH}	Propagation Delay, SB to Q	0.88	0.93	1.05	0.43	1.29	1.35	1.53	0.60
t_{PLH}	Propagation Delay, SB to QB	0.66	0.70	0.83	0.44	0.85	0.92	1.10	0.62
t_{PHL}		0.38	0.41	0.52	0.36	0.55	0.59	0.73	0.46
t_r	Output Rise Time, Q	0.23	0.35	0.71	1.20	0.28	0.45	0.96	1.69
t_f	Output Fall Time, Q	0.22	0.27	0.43	0.53	0.29	0.35	0.55	0.66
t_r	Output Rise Time, QB	0.27	0.38	0.74	1.19	0.38	0.55	1.05	1.69
t_f	Output Fall Time, QB	0.21	0.26	0.42	0.52	0.25	0.32	0.51	0.65

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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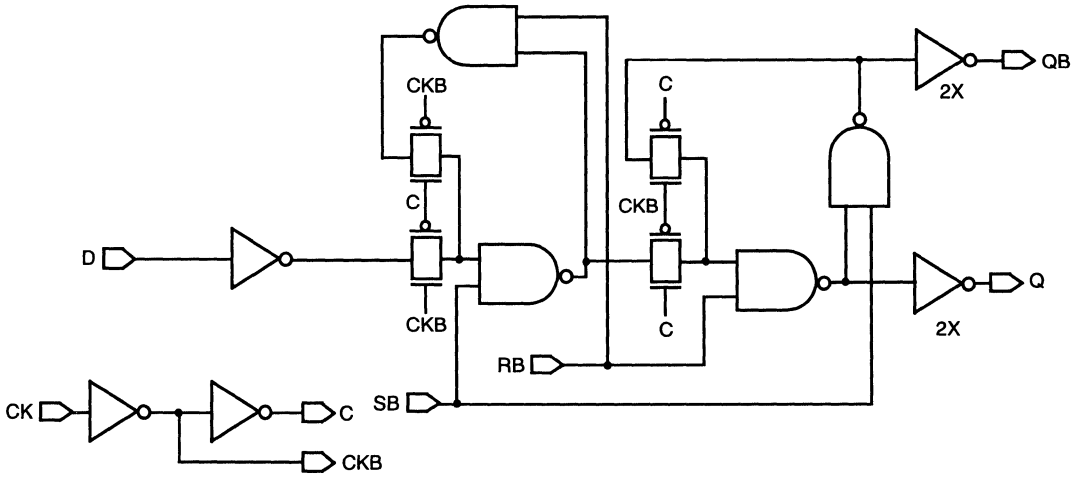
CMOS TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5 V	3.3 V
		Minimum Requirement	Minimum Requirement
	DFFRSPHB		
t_{su}	Set Up Time, D to CK	0.48	0.76
t_h	Hold Time, CK to D	0.20	0.29
t_h	Hold Time, RB to SB	2.20	0.61
t_h	Hold Time, SB to RB	0.60	0.78
t_{rec}	Recovery Time, RB to CK	0.00	0.00
t_{rec}	Recovery Time, SB to CK	-0.03	-0.03
t_w	Pulse Width, CK(L)	0.73	1.15
t_w	Pulse Width, CK(H)	0.98	1.46
t_w	Pulse Width, RB(L)	0.03	1.08
t_w	Pulse Width, RB(H)	0.75	0.04
t_w	Pulse Width, SB(L)	0.78	1.15
t_w	Pulse Width, SB(H)	0.04	0.04

FUNCTIONAL DIAGRAM: DFFRSPHB



7

D Flip Flop with Set and Reset Multiplexed (or Scan) Input 1X Drive (3.3 V and 5 V Core Voltage)

DFFRSLPB

MACRO	EQUIV. GATES
DFFRSLPB	14

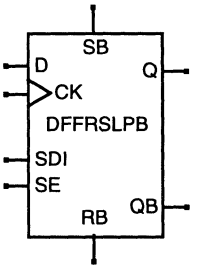
Rev. 1.07

MACRO	OUTPUTS/INPUTS
DFFRSLPB	Q,QB / SB,D,CK,SDI,SE,RB

MACRO	INPUT CAP.
DFFRSLPB	CK,D,SDI: 0.05pF RB,SB,SE: 0.09pF

FUNCTION TABLE

D	SDI	SE	CK	RB	SB	Q	QB
L	X	L	↗	H	H	L	H
H	X	L	↗	H	H	H	L
X	L	H	↗	H	H	L	H
X	H	H	↗	H	H	H	L
X	X	X	↘	H	H	Q	QB
X	X	X	X	L	H	L	H
X	X	X	X	H	L	H	L
X	X	X	X	L	L	L	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFRSLPB								
t_{PLH}	Propagation Delay, CK to Q	0.77	0.88	1.20	1.07	1.13	1.29	1.74	1.51
t_{PHL}		0.88	0.94	1.12	0.59	1.33	1.41	1.62	0.72
t_{PLH}	Propagation Delay, CK to QB	1.13	1.23	1.55	1.06	1.67	1.82	2.27	1.51
t_{PHL}		1.01	1.07	1.24	0.59	1.51	1.58	1.79	0.71
t_{PLH}	Propagation Delay, RB to Q	0.37	0.47	0.79	1.07	0.51	0.66	1.11	1.51
t_{PHL}		0.41	0.47	0.65	0.59	0.58	0.66	0.87	0.71
t_{PLH}	Propagation Delay, RB to QB	0.67	0.78	1.10	1.06	0.92	1.07	1.52	1.51
t_{PLH}	Propagation Delay, SB to Q	0.88	0.98	1.30	1.07	1.25	1.40	1.86	1.50
t_{PLH}	Propagation Delay, SB to QB	0.54	0.65	0.97	1.07	0.73	0.88	1.34	1.52
t_{PHL}		0.41	0.47	0.64	0.58	0.56	0.64	0.85	0.72
t_r	Output Rise Time, Q	0.18	0.43	1.16	2.45	0.25	0.59	1.63	3.45
t_f	Output Fall Time, Q	0.18	0.29	0.62	1.10	0.24	0.37	0.78	1.35
t_r	Output Rise Time, QB	0.24	0.49	1.23	2.46	0.31	0.66	1.70	3.46
t_f	Output Fall Time, QB	0.16	0.27	0.60	1.10	0.23	0.36	0.77	1.35

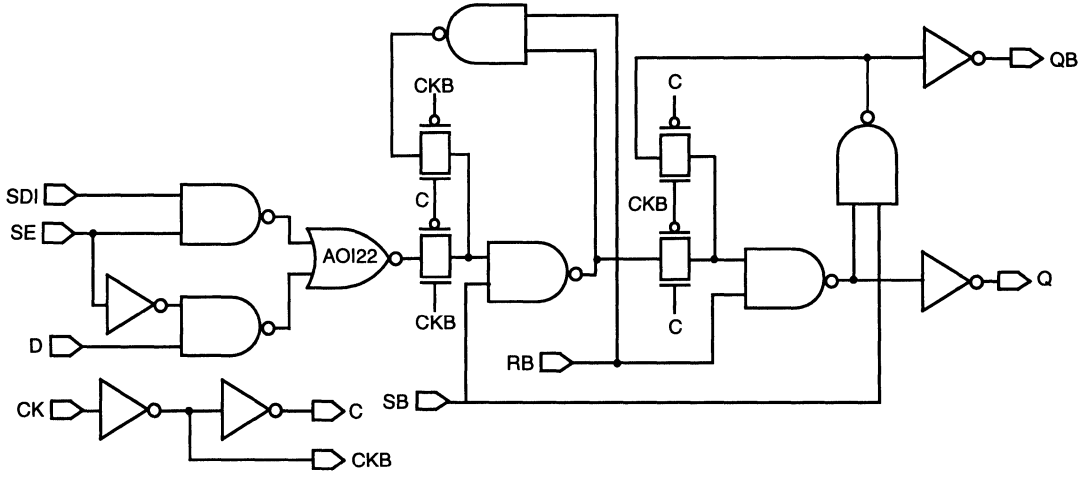
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

CMOS TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5 V	3.3 V
		Minimum Requirement	Minimum Requirement
	DFFRSLPB		
t_{su}	Set Up Time, D to CK	1.21	1.77
t_{su}	Set Up Time, SDI to CK	1.21	1.84
t_{su}	Set Up Time, SE to CK	1.16	1.77
t_h	Hold Time, CK to D	0.04	0.12
t_h	Hold Time, CK to SDI	-0.01	0.06
t_h	Hold Time, CK to SE	-0.11	-0.11
t_h	Hold Time, RB to SB	0.47	0.61
t_h	Hold Time, SB to RB	0.55	0.72
t_{rec}	Recovery Time, RB,SB to CK	0.01	0.00
t_w	Pulse Width, CK(L)	1.02	1.44
t_w	Pulse Width, CK(H)	0.78	1.13
t_w	Pulse Width, RB(L)	0.78	1.08
t_w	Pulse Width, RB,SB(H)	0.08	0.10
t_w	Pulse Width, SB(L)	0.83	1.14

FUNCTIONAL DIAGRAM: DFFRSLPB



7

D Flip Flop with Scan Latch 2X Drive (3.3 V and 5 V Core Voltage)

DFFSCH

MACRO	EQUIV. GATES
DFFSCH	18

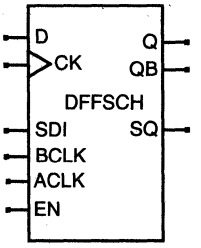
Rev. 1.07

MACRO	OUTPUTS/INPUTS
DFFSCH	Q,QB,SQ / D,CK,SDI,BCLK,ACLK,EN

MACRO	INPUT CAP.
DFFSCH	ACLK,BCLK,EN: 0.10pF CK: 0.05pF D: 0.16pF SDI: 0.20pF

FUNCTIONAL DESCRIPTION:

This macro consists of a D type Flip Flop with Q feedback (hold) capability. It allows scan data to be muxed into the slave stage and contains a separate scan latch for storing scan data independent of Q. CK clocks the Flip Flop, BCLK controls latching scan data into the slave stage and ACLK controls the final scan data latch.



FUNCTION TABLE

D	EN	CK	SDI	BCLK	ACLK	Q	QB	SQ	Notes
X	X	L	X	L	L	Q	QB	SQ	1
X	L	⌐	X	L	L	Q	QB	SQ	2
L	H	⌐	X	L	L	L	H	SQ	3
H	H	⌐	X	L	L	H	L	SQ	3
X	X	L	X	L	H	Q	QB	QB	4
X	X	L	L	H	L	H	L	SQ	5
X	X	L	H	H	L	L	H	SQ	5
X	X	L	L	H	H	H	L	L	6
X	X	L	H	H	H	L	H	H	6

1. No Clock 2. Active Clock, disabled 3. Active Clock, enabled
4. Scan-out Clock applied 5. Scan-in Clock applied 6. Flush or Ring-oscillate

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFSCH								
t_{PLH}	Propagation Delay, ACLK to SQ	0.67	0.75	1.00	0.83	0.98	1.09	1.44	1.16
t_{PHL}		0.66	0.73	0.96	0.76	0.90	0.99	1.27	0.92
t_{PLH}	Propagation Delay, BCLK to Q	0.66	0.69	0.77	0.26	0.95	0.99	1.10	0.36
t_{PHL}		0.88	0.93	1.08	0.48	1.32	1.39	1.58	0.65
t_{PLH}	Propagation Delay, BCLK to QB	1.13	1.16	1.23	0.23	1.74	1.77	1.87	0.33
t_{PHL}		1.29	1.33	1.45	0.41	1.80	1.85	2.01	0.52
t_{PLH}	Propagation Delay, BCLK to SQ	1.83	1.91	2.16	0.83	2.77	2.89	3.23	1.16
t_{PHL}		1.85	1.93	2.16	0.76	2.62	2.72	2.99	0.92
t_{PLH}	Propagation Delay, CK to Q	0.96	0.98	1.06	0.27	1.38	1.42	1.53	0.37
t_{PHL}		1.09	1.14	1.28	0.48	1.62	1.68	1.88	0.64
t_{PLH}	Propagation Delay, CK to QB	1.34	1.37	1.44	0.23	2.03	2.06	2.16	0.33
t_{PHL}		1.60	1.64	1.76	0.41	2.26	2.31	2.46	0.52
t_{PLH}	Propagation Delay, CK to SQ	2.18	2.26	2.51	0.83	3.28	3.39	3.74	1.16
t_{PHL}		2.28	2.35	2.58	0.76	3.25	3.34	3.61	0.92
t_{PLH}	Propagation Delay, SDI to Q	0.56	0.58	0.66	0.25	0.81	0.85	0.96	0.36
t_{PHL}		0.75	0.80	0.94	0.48	1.13	1.20	1.39	0.65
t_{PLH}	Propagation Delay, SDI to QB	0.96	0.98	1.05	0.24	1.54	1.58	1.67	0.32
t_{PHL}		1.12	1.16	1.28	0.40	1.58	1.63	1.78	0.52
t_{PLH}	Propagation Delay, SDI to SQ	1.68	1.75	1.98	0.76	2.40	2.49	2.77	0.92
t_{PHL}		1.68	1.76	2.01	0.82	2.57	2.69	3.03	1.16
t_r	Output Rise Time, Q	0.29	0.35	0.52	0.57	0.38	0.46	0.71	0.82
t_f	Output Fall Time, Q	0.44	0.49	0.67	0.59	0.59	0.66	0.89	0.75
t_r	Output Rise Time, QB	0.26	0.32	0.49	0.56	0.32	0.40	0.64	0.79
t_f	Output Fall Time, QB	0.31	0.36	0.53	0.55	0.36	0.43	0.63	0.68
t_r	Output Rise Time, SQ	0.20	0.44	1.17	2.44	0.25	0.60	1.63	3.44
t_f	Output Fall Time, SQ	0.18	0.30	0.65	1.17	0.24	0.39	0.81	1.40

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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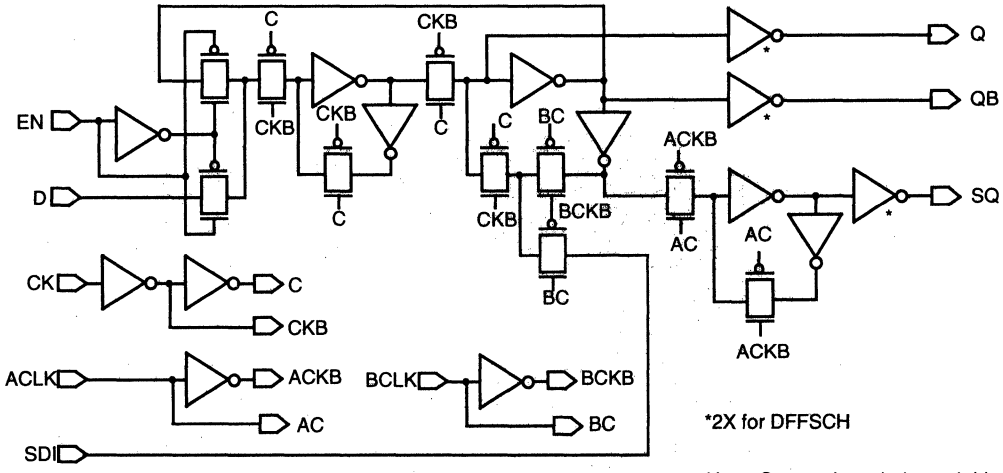
FUNCTIONAL DIAGRAM: DFFSCH



Note: Outputs have balanced drive.

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V Minimum Requirement	3.3 V Minimum Requirement
	DFFSCH		
t_{su}	Set Up Time, BCLK to ACLK	1.70	2.59
t_{su}	Set Up Time, CK to ACLK	1.84	2.74
t_{su}	Set Up Time, SDI to ACLK	1.67	2.50
t_{su}	Set Up Time, SDI to BCLK	1.33	1.93
t_{su}	Set Up Time, D to CK	0.15	0.34
t_{su}	Set Up Time, EN to CK	0.43	0.66
t_h	Hold Time, ACLK to BCLK	-1.21	-1.71
t_h	Hold Time, ACLK to CK	-1.21	-1.87
t_h	Hold Time, ACLK to SDI	-1.08	-1.58
t_h	Hold Time, BCLK to CK	-1.07	-1.65
t_h	Hold Time, BCLK to SDI	0.00	-0.01
t_h	Hold Time, CK to BCLK	-1.05	-1.51
t_h	Hold Time, CK to D	0.43	0.57
t_h	Hold Time, CK to EN	0.23	0.31
t_{rec}	Recovery Time, CK to ACLK	1.97	2.93
t_{rec}	Recovery Time, ACLK to CK	-1.49	-2.20
t_w	Pulse Width, ACLK(H)	0.43	0.65
t_w	Pulse Width, BCLK(H)	1.28	1.89
t_w	Pulse Width, CK(L)	0.59	0.94
t_w	Pulse Width, CK(H)	1.52	2.20

D Flip Flop Scan Latch with Set 2X Drive (3.3 V and 5 V Core Voltage)

DFFSCAH

MACRO	EQUIV. GATES
DFFSCAH	20

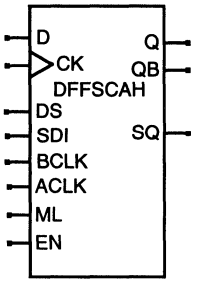
Rev. 1.07

MACRO	OUTPUTS/INPUTS
DFFSCAH	Q,QB,SQ / D,CK,DS,SDI,BCLK, ACLK,ML,EN

MACRO	INPUT CAP.
DFFSCAH	ACLK,BCLK,CK,EN, ML: 0.10pF D: 0.15pF DS: 0.05pF SDI: 0.41pF

FUNCTIONAL DESCRIPTION:

This macro consists of a D type Flip Flop with Q feedback (hold) capability. It allows scan data to be muxed into the Master slave or the slave stage and contains a separate scan latch for storing scan data independent of Q. CK clocks the Flip Flop, BCLK controls latching scan data into the slave stage, ML controls latching Scan data into the Master slave and ACLK controls the final scan data latch. DS is used when latching SDI into the master stage to ignore the D or feedback data. ML HIGH while DS is LOW is illegal.



FUNCTION TABLE

D	EN	CK	SDI	BCLK	ACLK	DS	ML	Q	QB	SQ	Notes
X	X	L	X	L	L	L	L	Q	QB	SQ	1
X	L	⌐	X	L	L	L	L	Q	QB	SQ	2
L	H	⌐	X	L	L	L	L	L	H	SQ	3
H	H	⌐	X	L	L	L	L	H	L	SQ	3
X	X	L	X	L	H	L	L	Q	QB	QB	4
X	X	L	L	H	L	L	L	H	L	SQ	5
X	X	L	H	H	L	L	L	L	H	SQ	5
X	X	L	L	H	H	L	L	H	L	L	6
X	X	L	H	H	H	L	L	L	H	H	6

1. No Clock 2. Active Clock, disabled 3. Active Clock,enabled
4. Scan-out Clock applied 5. Scan-in Clock applied 6. Flush or Ring-oscillate

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFSCAH								
t_{PLH}	Propagation Delay,	0.63	0.71	0.96	0.83	0.93	1.04	1.39	1.16
t_{PHL}	ACLK to SQ	0.62	0.69	0.92	0.77	0.86	0.96	1.24	0.93
t_{PLH}	Propagation Delay,	0.59	0.62	0.69	0.24	0.81	0.84	0.95	0.34
t_{PHL}	BCLK to Q	0.77	0.81	0.95	0.45	1.15	1.21	1.39	0.60
t_{PLH}	Propagation Delay,	1.06	1.08	1.15	0.23	1.60	1.63	1.73	0.32
t_{PHL}	BCLK to QB	1.20	1.24	1.37	0.41	1.66	1.71	1.87	0.53
t_{PLH}	Propagation Delay,	1.73	1.82	2.06	0.82	2.61	2.73	3.08	1.16
t_{PHL}	BCLK to SQ	1.75	1.83	2.06	0.77	2.48	2.57	2.85	0.93
t_{PLH}	Propagation Delay,	0.70	0.73	0.80	0.24	0.99	1.03	1.13	0.34
t_{PHL}	CK to Q	0.86	0.91	1.04	0.46	1.25	1.31	1.49	0.60
t_{PLH}	Propagation Delay,	1.15	1.17	1.24	0.23	1.70	1.74	1.83	0.33
t_{PHL}	CK to QB	1.32	1.36	1.48	0.41	1.84	1.89	2.05	0.53
t_{PLH}	Propagation Delay,	1.96	2.05	2.29	0.83	2.93	3.05	3.39	1.16
t_{PHL}	CK to SQ	2.00	2.08	2.31	0.77	2.85	2.94	3.22	0.93
t_{PLH}	Propagation Delay,	0.99	1.01	1.09	0.25	1.46	1.50	1.60	0.34
t_{PHL}	ML to Q	1.21	1.25	1.39	0.46	1.73	1.79	1.97	0.61
t_{PLH}	Propagation Delay,	1.48	1.50	1.57	0.23	2.19	2.22	2.31	0.32
t_{PHL}	ML to QB	1.63	1.67	1.79	0.41	2.33	2.38	2.54	0.52
t_{PLH}	Propagation Delay,	2.32	2.40	2.65	0.82	3.40	3.52	3.87	1.16
t_{PHL}	ML to SQ	2.32	2.39	2.62	0.76	3.33	3.42	3.70	0.93
t_{PLH}	Propagation Delay,	0.46	0.48	0.56	0.24	0.68	0.71	0.81	0.34
t_{PHL}	SDI to Q	0.65	0.70	0.83	0.45	0.96	1.02	1.20	0.60
t_{PLH}	Propagation Delay,	1.33	1.35	1.42	0.23	1.98	2.01	2.11	0.32
t_{PHL}	SDI to QB	1.51	1.55	1.68	0.41	2.17	2.22	2.38	0.52

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay,	1.59	1.67	1.92	0.83	2.41	2.52	2.87	1.16
t_{PHL}	SDI to SQ	1.59	1.66	1.89	0.76	2.27	2.36	2.64	0.93
t_r	Output Rise Time, Q	0.28	0.34	0.52	0.58	0.32	0.40	0.64	0.82
t_f	Output Fall Time, Q	0.40	0.46	0.64	0.59	0.53	0.60	0.82	0.73
t_r	Output Rise Time, QB	0.28	0.34	0.51	0.56	0.33	0.41	0.65	0.80
t_f	Output Fall Time, QB	0.31	0.37	0.53	0.55	0.37	0.44	0.65	0.69
t_r	Output Rise Time, SQ	0.21	0.45	1.18	2.44	0.26	0.60	1.63	3.44
t_f	Output Fall Time, SQ	0.17	0.29	0.64	1.18	0.24	0.38	0.80	1.41

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

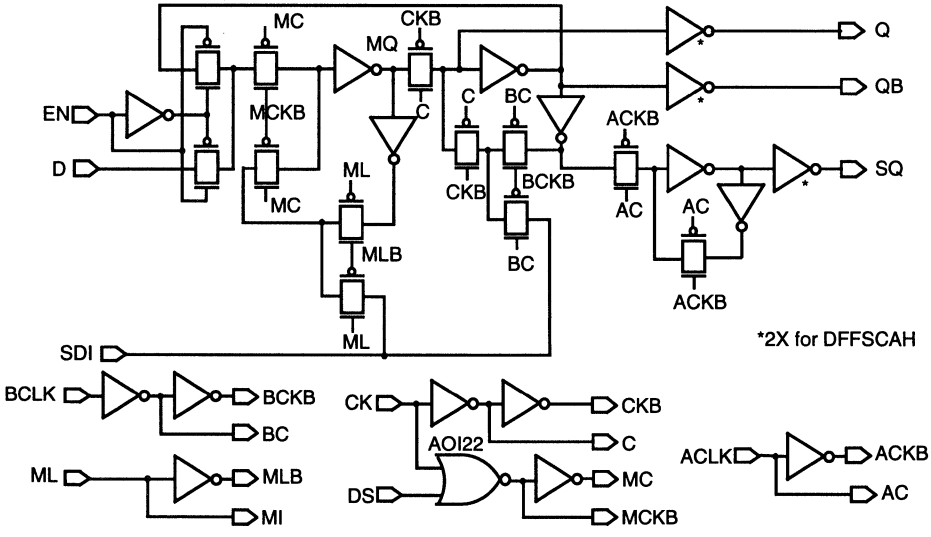
Sym	Parameter	5 V	3.3 V
		Minimum Requirement	Minimum Requirement
	DFFSCAH		
t_{su}	Set Up Time, BCLK to ACLK	1.74	2.61
t_{su}	Set Up Time, CK to ACLK	1.74	2.64
t_{su}	Set Up Time, ML to ACLK	2.31	3.38
t_{su}	Set Up Time, SDI to ACLK	1.72	2.53
t_{su}	Set Up Time, SDI to BCLK	0.91	1.28
t_{su}	Set Up Time, D to CK	0.44	0.72
t_{su}	Set Up Time, DS to CK	0.85	1.36
t_{su}	Set Up Time, EN to CK	0.71	1.08
t_{su}	Set Up Time, ML to CK	0.94	1.34
t_{su}	Set Up Time, SDI to CK	1.24	1.76
t_{su}	Set Up Time, CK to DS	0.68	-0.08
t_{su}	Set Up Time, D to DS	0.51	0.82
t_{su}	Set Up Time, EN to DS	0.79	1.18
t_{su}	Set Up Time, SDI to ML	1.28	1.83
t_h	Hold Time, ACLK to BCLK	-1.12	-1.60
t_h	Hold Time, ACLK to CK	-1.12	-1.69
t_h	Hold Time, ACLK to ML	-1.64	-2.38
t_h	Hold Time, ACLK to SDI	-1.02	-1.47
t_h	Hold Time, BCLK to CK	-0.98	-1.48
t_h	Hold Time, BCLK,CK to SDI	0.06	0.08
t_h	Hold Time, CK to BCLK	-0.95	-1.40
t_h	Hold Time, CK to D	0.34	0.42
t_h	Hold Time, CK to EN	0.13	0.17
t_h	Hold Time, CK to ML	-0.08	-0.10
t_h	Hold Time, DS to D	0.23	0.28
t_h	Hold Time, DS to EN	0.03	0.02
t_h	Hold Time, DS to ML	-0.40	-0.70
t_h	Hold Time, ML to CK	0.23	0.30
t_h	Hold Time, ML to DS	0.32	0.45

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V Minimum Requirement	3.3 V Minimum Requirement
t_h	Hold Time, ML to SDI	0.16	0.20
t_{rec}	Recovery Time, CK to ACLK	1.80	2.72
t_{rec}	Recovery Time, ACLK to CK	-1.26	-1.76
t_{rec}	Recovery Time, ML to CK	-0.24	-0.33
t_w	Pulse Width, ACLK(H)	0.52	0.79
t_w	Pulse Width, BCLK(H)	1.20	1.75
t_w	Pulse Width, CK (L)	0.89	1.41
t_w	Pulse Width, CK(H)	1.32	1.90
t_w	Pulse Width, DS(L)	0.89	1.34
t_w	Pulse Width, ML(H)	0.94	1.37

FUNCTIONAL DIAGRAM: DFFSCAH



D Flip Flop Latch with Set
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

DFFSP
DFFSPH

MACRO	EQUIV. GATES
DFFSP	8
DFFSPH	10

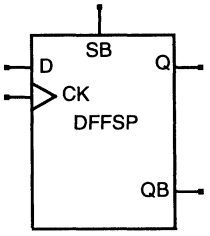
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	Q,QB / SB,D,CK

MACRO	INPUT CAP.
All	CK,D: 0.05pF SB: 0.09pF

FUNCTION TABLE

D	CK	SB	Q	QB
L	↗	H	L	H
H	↗	H	H	L
X	↘	H	Q	QB
X	X	L	H	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
DFFSP									
t_{PLH}	Propagation Delay, CK to Q	0.82	0.90	1.15	0.83	1.13	1.25	1.60	1.16
t_{PHL}		1.00	1.08	1.31	0.76	1.43	1.53	1.80	0.93
t_{PLH}	Propagation Delay, CK to QB	1.22	1.30	1.55	0.83	1.73	1.84	2.19	1.16
t_{PHL}		1.07	1.15	1.38	0.76	1.52	1.61	1.88	0.92
t_{PHL}	Propagation Delay, SB to Q	0.69	0.77	1.02	0.82	1.01	1.13	1.48	1.16
t_{PLH}	Propagation Delay, SB to QB	0.32	0.39	0.62	0.76	0.47	0.56	0.84	0.92
t_r	Output Rise Time, Q	0.14	0.39	1.12	2.44	0.20	0.55	1.58	3.45
t_f	Output Fall Time, Q	0.16	0.27	0.62	1.17	0.22	0.36	0.78	1.41
t_r	Output Rise Time, QB	0.16	0.40	1.13	2.43	0.20	0.55	1.58	3.45
t_f	Output Fall Time, QB	0.15	0.27	0.62	1.17	0.22	0.36	0.78	1.41
DFFSPH									
t_{PLH}	Propagation Delay, CK to Q	0.86	0.90	1.03	0.42	1.18	1.24	1.42	0.59
t_{PHL}		1.06	1.10	1.22	0.40	1.51	1.56	1.71	0.50
t_{PLH}	Propagation Delay, CK to QB	1.34	1.38	1.51	0.43	1.90	1.96	2.14	0.60
t_{PHL}		1.18	1.22	1.34	0.40	1.66	1.71	1.85	0.49
t_{PHL}	Propagation Delay, RB to Q	0.82	0.86	0.98	0.41	1.17	1.23	1.40	0.59
t_{PLH}	Propagation Delay, RB to QB	0.38	0.42	0.54	0.39	0.55	0.60	0.75	0.49
t_r	Output Rise Time, Q	0.19	0.30	0.66	1.19	0.27	0.44	0.95	1.70
t_f	Output Fall Time, Q	0.19	0.25	0.42	0.56	0.26	0.32	0.53	0.68
t_r	Output Rise Time, QB	0.82	0.90	1.15	0.83	0.27	0.44	0.94	1.68
t_f	Output Fall Time, QB	1.00	1.08	1.31	0.76	0.24	0.31	0.51	0.68

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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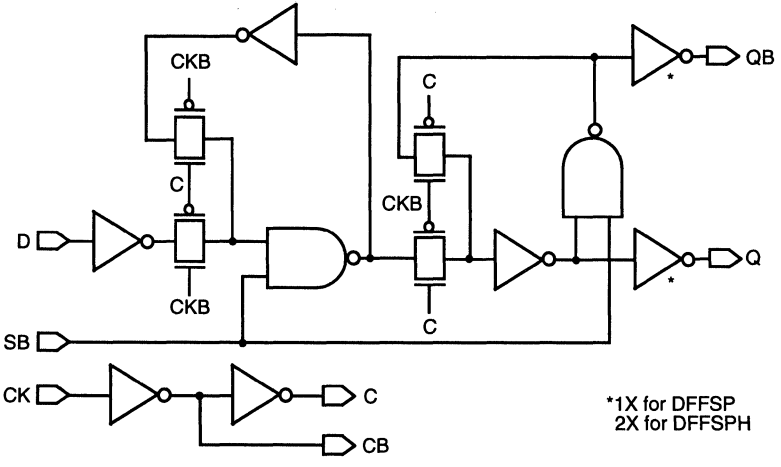
CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V Minimum Requirement	3.3 V Minimum Requirement
	DFFSP		
t_{su}	Set Up Time, D to CK	0.34	0.58
t_h	Hold Time, CK to D	0.28	0.40
t_{rec}	Recovery Time, SB to CK	-0.06	-0.06
t_w	Pulse Width, CK(L)	0.73	1.13
t_w	Pulse Width, CK(H)	0.86	1.27
t_w	Pulse Width, SB(L)	0.73	0.98
t_w	Pulse Width, SB(H)	0.04	0.05
	DFFSPH		
t_{su}	Set Up Time, D to CK	0.34	0.58
t_h	Hold Time, CK to D	0.28	0.40
t_{rec}	Recovery Time, SB to CK	-0.06	-0.06
t_w	Pulse Width, CK(L)	0.72	1.12
t_w	Pulse Width, CK(H)	0.99	1.44
t_w	Pulse Width, SB(L)	0.72	1.04
t_w	Pulse Width, SB(H)	0.04	0.05

FUNCTIONAL DIAGRAM: DFFSP



D Flip Flop with Set, Multiplexed (or Scan) Input 1X & 2X Drive (3.3 V and 5 V Core Voltage)

DFFSLP
DFFSLPH

MACRO	EQUIV. GATES
All	12

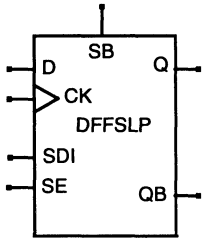
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	Q,QB / SB,D,CK,SDI,SE

MACRO	INPUT CAP.
All	CK,D,SDI: 0.05pF SB,SE: 0.11pF

FUNCTION TABLE

D	SDI	SE	CK	SB	Q	QB
L	X	L	↑	H	L	H
H	X	L	↑	H	H	L
X	L	H	↑	H	L	H
X	H	H	↑	H	H	L
X	X	X	↓	H	Q	QB
X	X	X	X	L	H	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
DFFSLP									
t_{PLH}	Propagation Delay, CK to Q	0.81	0.90	1.14	0.83	1.12	1.23	1.58	1.16
t_{PHL}		0.96	1.04	1.27	0.77	1.40	1.49	1.77	0.93
t_{PLH}	Propagation Delay, CK to QB	1.17	1.26	1.51	0.83	1.70	1.82	2.16	1.16
t_{PHL}		1.08	1.15	1.38	0.76	1.51	1.60	1.88	0.92
t_{PHL}	Propagation Delay, SB to Q	0.69	0.77	1.02	0.83	1.00	1.12	1.47	1.16
t_{PLH}	Propagation Delay, SB to QB	0.32	0.40	0.63	0.76	0.48	0.57	0.84	0.92
t_r	Output Rise Time, Q	0.15	0.39	1.12	2.43	0.19	0.54	1.57	3.44
t_f	Output Fall Time, Q	0.16	0.28	0.63	1.17	0.21	0.35	0.78	1.41
t_r	Output Rise Time, QB	0.15	0.39	1.12	2.43	0.19	0.54	1.57	3.44
t_f	Output Fall Time, QB	0.16	0.28	0.63	1.17	0.21	0.35	0.78	1.41
DFFSLPH									
t_{PLH}	Propagation Delay, CK to Q	0.88	0.92	1.05	0.42	1.23	1.29	1.46	0.58
t_{PHL}		1.07	1.11	1.23	0.40	1.53	1.58	1.73	0.50
t_{PLH}	Propagation Delay, CK to QB	1.37	1.42	1.54	0.43	1.97	2.03	2.21	0.60
t_{PHL}		1.23	1.27	1.39	0.40	1.74	1.79	1.94	0.49
t_{PHL}	Propagation Delay, RB to Q	0.77	0.81	0.93	0.42	1.12	1.18	1.36	0.58
t_{PLH}	Propagation Delay, RB to QB	0.40	0.44	0.56	0.39	0.59	0.63	0.78	0.48
t_r	Output Rise Time, Q	0.20	0.31	0.67	1.19	0.25	0.42	0.93	1.70
t_f	Output Fall Time, Q	0.20	0.26	0.43	0.56	0.27	0.33	0.54	0.69
t_r	Output Rise Time, QB	0.22	0.34	0.69	1.18	0.28	0.45	0.95	1.68
t_f	Output Fall Time, QB	0.21	0.27	0.43	0.56	0.28	0.35	0.55	0.68

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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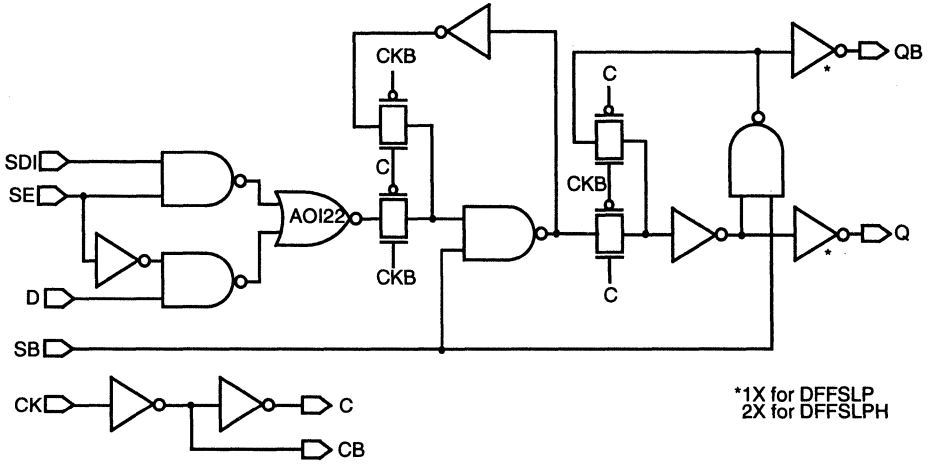
CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V Minimum Requirement	3.3 V Minimum Requirement
	DFFSLP		
t_{su}	Set Up Time, D to CK	0.74	1.23
t_{su}	Set Up Time, SDI to CK	0.72	1.15
t_{su}	Set Up Time, SE to CK	0.85	1.35
t_h	Hold Time, CK to D	0.05	0.08
t_h	Hold Time, CK to SDI	0.10	0.15
t_h	Hold Time, CK to SE	-0.01	0.01
t_{rec}	Recovery Time, SB to CK	-0.03	-0.05
t_w	Pulse Width, CK(L)	0.71	1.11
t_w	Pulse Width, CK(H)	0.83	1.23
t_w	Pulse Width, SB(L)	0.63	0.90
t_w	Pulse Width, SB(H)	0.03	0.05
	DFFSLPH		
t_{su}	Set Up Time, D to CK	0.85	1.39
t_{su}	Set Up Time, SDI to CK	0.81	1.31
t_{su}	Set Up Time, SE to CK	0.95	1.50
t_h	Hold Time, CK to D	0.01	0.04
t_h	Hold Time, CK to SDI	0.08	0.12
t_h	Hold Time, CK to SE	-0.04	-0.03
t_{rec}	Recovery Time, SB to CK	-0.02	-0.04
t_w	Pulse Width, CK(L)	0.74	1.16
t_w	Pulse Width, CK(H)	1.01	1.47
t_w	Pulse Width, SB(L)	0.67	0.95
t_w	Pulse Width, SB(H)	0.03	0.05

7

FUNCTIONAL DIAGRAM: DFFSLP



D Flip Flop with Synchronous Reset (3.3 V and 5 V Core Voltage)

DFFSRPA

MACRO	EQUIV. GATES
DFFSRPA	9

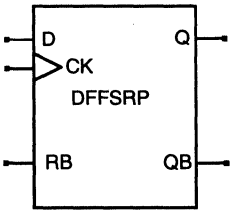
Rev. 1.07

MACRO	OUTPUTS/INPUTS
DFFSRPA	Q,QB / D,CK,RB

MACRO	INPUT CAP.
DFFSRPA	CK,D,RB: 0.05pF

FUNCTION TABLE

D	CK	RB	Qn+1	QBn+1
L	↗	H	L	H
H	↗	H	H	L
X	↗	L	L	H
X	↗	X	X	X



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFSRP								
t_{PLH}	Propagation Delay,	0.81	0.85	0.98	0.42	1.08	1.14	1.31	0.59
t_{PHL}	CK to Q	1.07	1.14	1.37	0.76	1.45	1.55	1.83	0.94
t_{PLH}	Propagation Delay,	1.17	1.21	1.33	0.41	1.61	1.66	1.84	0.58
t_{PHL}	CK to QB	1.11	1.19	1.42	0.76	1.55	1.64	1.91	0.91
t_r	Output Rise Time, Q	0.15	0.27	0.63	1.21	0.30	0.47	0.97	1.66
t_f	Output Fall Time, Q	0.17	0.29	0.67	1.26	0.26	0.40	0.83	1.44
t_r	Output Rise Time, QB	0.14	0.27	0.65	1.27	0.14	0.31	0.84	1.75
t_f	Output Fall Time, QB	0.16	0.29	0.67	1.29	0.28	0.43	0.85	1.41

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

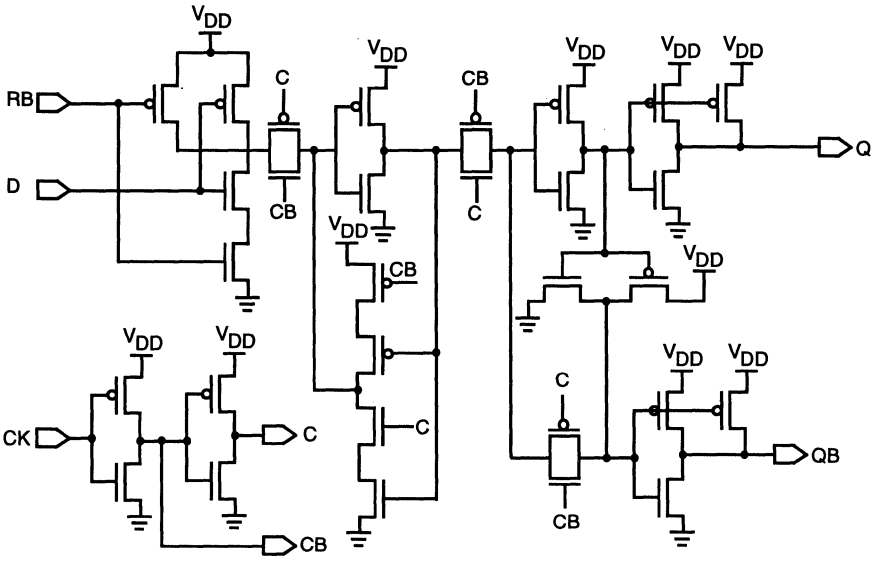
CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V	3.3 V
		Minimum Requirement	Minimum Requirement
	DFFSRPA		
t_{su}	Set Up Time, D to CK	0.42	0.62
t_{su}	Set Up Time, RB to CK	0.38	0.60
t_h	Hold Time, CK to D	0.27	0.30
t_h	Hold Time, CK to RB	0.22	0.24
t_w	Pulse Width, CK(L)	0.34	0.62
t_w	Pulse Width, CK(H)	0.61	0.91

7

FUNCTIONAL DIAGRAM: DFFSRPA



7

D Flip Flop, Multiplexed (or Scan) Input with Synchronous Reset (3.3 V and 5 V Core Voltage)

DFFSRLPA

MACRO	EQUIV. GATES
DFFSRLPA	12

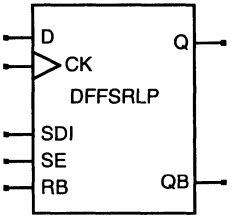
Rev. 1.07

MACRO	OUTPUTS/INPUTS
DFFSRLPA	Q,QB / D,CK,SDI,SE,RB

MACRO	INPUT CAP.
DFFSRLPA	CK,D,RB,SDI: 0.05pF SE: 0.09pF

FUNCTION TABLE

D	SDI	SE	CK	RB	Qn+1	QBn+1
X	L	H	↑	X	L	H
X	H	H	↑	X	H	L
L	X	L	↑	H	L	H
H	X	L	↑	H	H	L
X	X	L	↑	L	L	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
DFFSRLP									
t_{PLH}	Propagation Delay, CK to Q	0.80	0.85	0.98	0.43	1.10	1.16	1.35	0.62
t_{PHL}		0.89	0.97	1.21	0.80	1.23	1.33	1.62	0.99
t_{PLH}	Propagation Delay, CK to QB	0.97	1.01	1.13	0.41	1.32	1.38	1.56	0.59
t_{PHL}		1.15	1.23	1.46	0.76	1.60	1.69	1.97	0.94
t_r	Output Rise Time, Q	0.20	0.31	0.67	1.18	0.33	0.50	1.00	1.67
t_f	Output Fall Time, Q	0.33	0.44	0.78	1.13	0.43	0.57	1.02	1.47
t_r	Output Rise Time, QB	0.19	0.30	0.65	1.16	0.38	0.54	1.02	1.60
t_f	Output Fall Time, QB	0.14	0.26	0.65	1.27	0.23	0.38	0.83	1.49

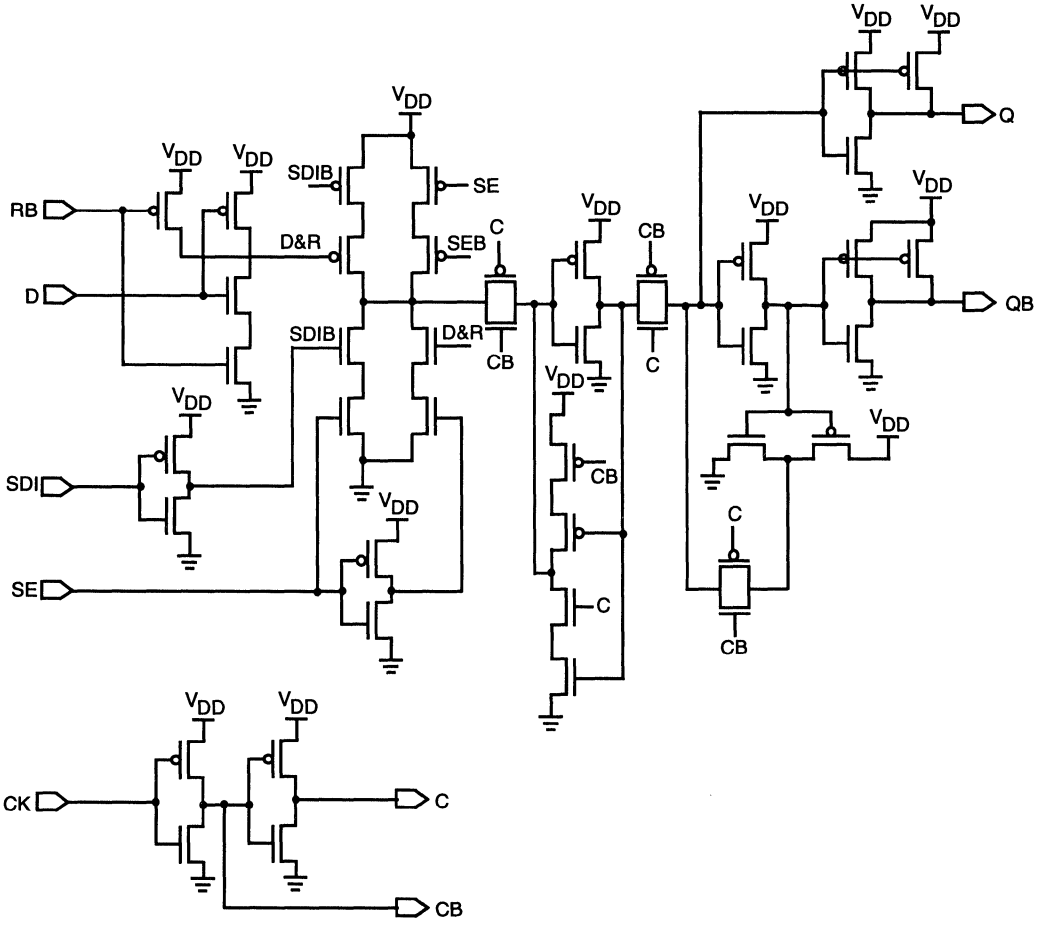
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V	3.3 V
		Minimum Requirement	Minimum Requirement
DFFSRLP			
t_{su}	Set Up Time, D,RB,SDI to CK	0.63	1.01
t_{su}	Set Up Time, SE to CK	0.61	1.10
t_h	Hold Time, CK to D	-0.02	-0.04
t_h	Hold Time, CK to RB	0.06	0.05
t_h	Hold Time, CK to SDI	0.01	-0.07
t_h	Hold Time, CK to SE	0.37	0.01
t_w	Pulse Width, CK(L)	0.60	0.69
t_w	Pulse Width, CK(H)	0.63	0.93

FUNCTIONAL DIAGRAM: DFFSRLP



D Flip Flop with Synchronous Set (3.3 V and 5 V Core Voltage)

DFFSSP

MACRO	EQUIV. GATES
DFFSSP	9

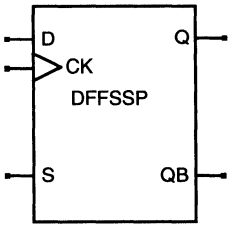
Rev. 1.07

MACRO	OUTPUTS/INPUTS
DFFSSP	Q,QB / D,CK,S

MACRO	INPUT CAP.
DFFSSP	CK,D,S: 0.05pF

FUNCTION TABLE

D	CK	S	Qn+1	QBn+1
L	↗	L	L	H
H	↗	L	H	L
X	↗	H	H	L
X	↗	X	X	X



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFSSP								
t_{PLH}	Propagation Delay, CK to Q	0.80	0.84	0.97	0.42	1.08	1.14	1.31	0.59
t_{PHL}		1.06	1.14	1.37	0.76	1.46	1.55	1.83	0.93
t_{PLH}	Propagation Delay, CK to QB	1.16	1.20	1.32	0.42	1.60	1.66	1.84	0.58
t_{PHL}		1.10	1.18	1.41	0.76	1.55	1.64	1.91	0.91
t_r	Output Rise Time, Q	0.15	0.27	0.63	1.21	0.30	0.46	0.97	1.69
t_f	Output Fall Time, Q	0.16	0.29	0.66	1.23	0.19	0.35	0.81	1.53
t_r	Output Rise Time, QB	0.13	0.26	0.63	1.26	0.19	0.36	0.87	1.71
t_f	Output Fall Time, QB	0.16	0.29	0.67	1.29	0.27	0.42	0.85	1.44

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

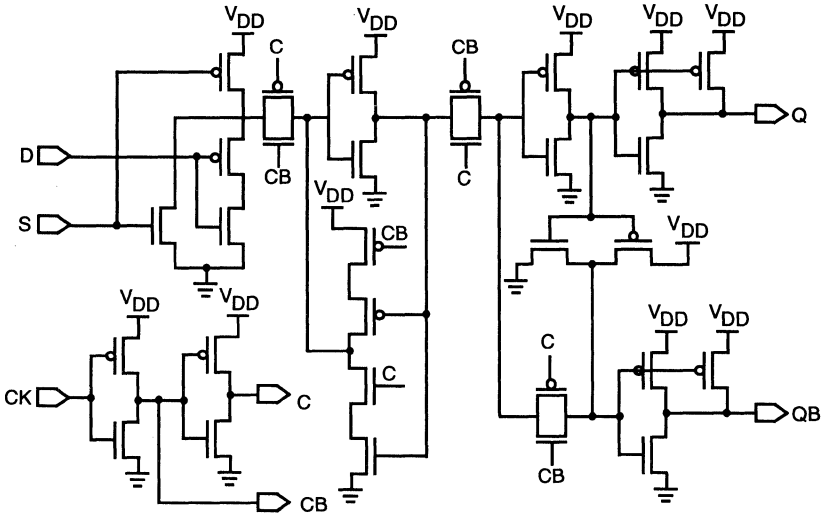
CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V	3.3 V
		Minimum Requirement	Minimum Requirement
	DFFSSP		
t_{su}	Set Up Time, D,S to CK	0.44	0.79
t_h	Hold Time, CK to D	0.20	0.26
t_h	Hold Time, CK to S	0.17	0.24
t_w	Pulse Width, CK(L)	0.44	0.78
t_w	Pulse Width, CK(H)	0.62	0.92

7

FUNCTIONAL DIAGRAM: DFFSSP



7

D Flip Flop, Multiplexed (or Scan) Input with Synchronous Set (3.3 V and 5 V Core Voltage)

DFFSSLP

MACRO	EQUIV. GATES
DFFSSLP	12

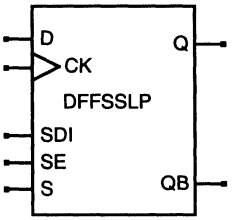
Rev. 1.07

MACRO	OUTPUTS/INPUTS
DFFSSLP	Q,QB / D,CK,SDI,SE,S

MACRO	INPUT CAP.
DFFSSLP	CK,D,S,SDI: 0.05pF SE: 0.09pF

FUNCTION TABLE

D	SDI	SE	CK	S	Qn+1	QBn+1
X	L	H	↑	X	L	H
X	H	H	↑	X	H	L
L	X	L	↑	L	L	H
H	X	L	↑	L	H	L
X	X	L	↑	H	H	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DFFSSLP								
t_{PLH}	Propagation Delay, CK to Q	0.81	0.85	0.98	0.43	1.10	1.16	1.35	0.62
t_{PHL}		0.89	0.97	1.21	0.80	1.23	1.33	1.62	0.99
t_{PLH}	Propagation Delay, CK to QB	0.97	1.01	1.13	0.41	1.32	1.38	1.56	0.59
t_{PHL}		1.16	1.24	1.47	0.76	1.60	1.69	1.97	0.94
t_r	Output Rise Time, Q	0.24	0.35	0.70	1.15	0.33	0.50	1.00	1.67
t_f	Output Fall Time, Q	0.33	0.44	0.78	1.13	0.43	0.57	1.02	1.47
t_r	Output Rise Time, QB	0.19	0.30	0.65	1.16	0.38	0.54	1.02	1.60
t_f	Output Fall Time, QB	0.14	0.27	0.66	1.30	0.23	0.38	0.83	1.49

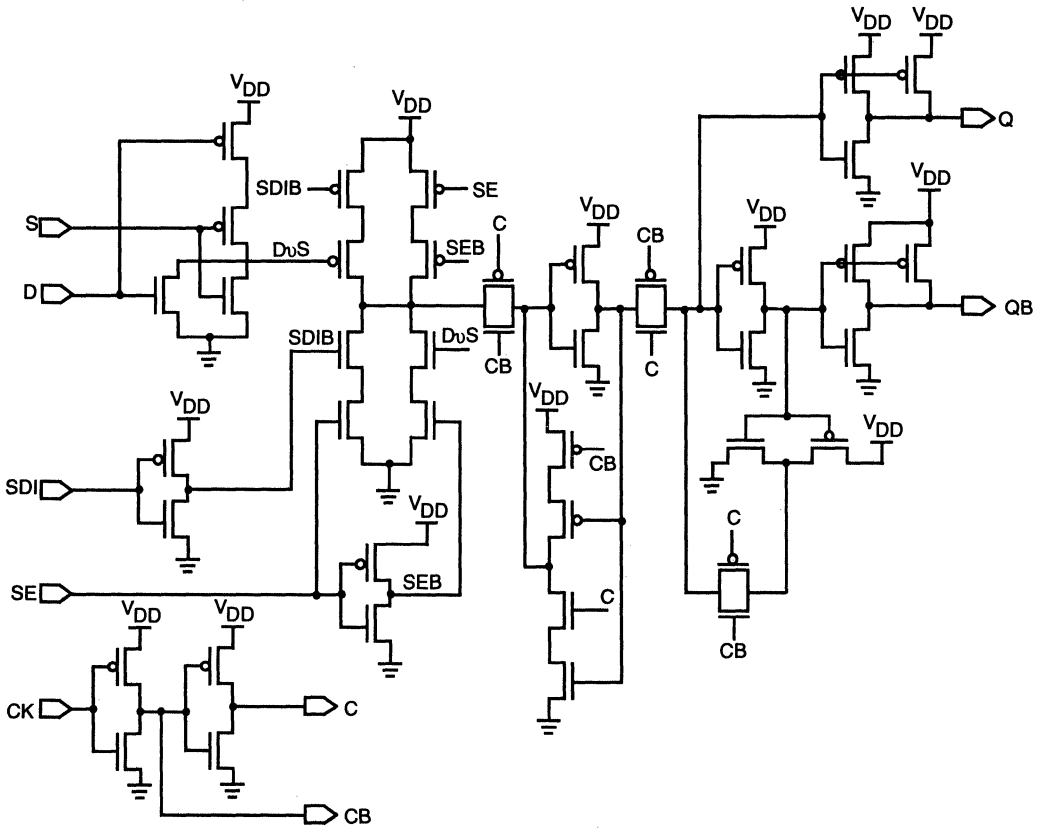
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V	3.3 V
		Minimum Requirement	Minimum Requirement
	DFFSSLP		
t_{su}	Set Up Time, D to CK	0.68	1.05
t_{su}	Set Up Time, S to CK	0.68	1.02
t_{su}	Set Up Time, SDI to CK	0.61	1.02
t_{su}	Set Up Time, SE to CK	0.61	1.09
t_h	Hold Time, CK to D	0.03	-0.03
t_h	Hold Time, CK to S	0.07	0.00
t_h	Hold Time, CK to SDI	-0.02	-0.07
t_h	Hold Time, CK to SE	0.01	0.00
t_w	Pulse Width, CK(L)	0.37	0.69
t_w	Pulse Width, CK(H)	0.61	0.93

FUNCTIONAL DIAGRAM: DFFSSLP



8 Stage Inverter Delay (3.3 V and 5 V Core Voltage)

DLY8

MACRO	EQUIV. GATES
DLY8	4

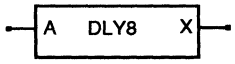
Rev. 1.07Rev. 1.07

MACRO	OUTPUTS/INPUTS
DLY8	X / A

MACRO	INPUT CAP.
DLY8	A: 0.05pF

FUNCTION TABLE

A	X
L	L
H	H



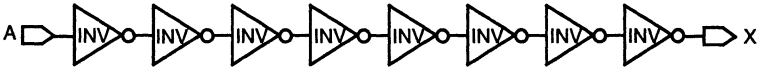
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	DLY8								
t_{PLH}	Propagation Delay,	1.00	1.08	1.33	0.83	1.40	1.52	1.86	1.16
t_{PHL}	A to X	1.02	1.10	1.32	0.76	1.42	1.51	1.78	0.91
t_r	Output Rise Time, X	0.12	0.37	1.10	2.44	0.17	0.51	1.55	3.45
t_f	Output Fall Time, X	0.10	0.22	0.57	1.19	0.16	0.30	0.73	1.42

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: DLY8



7

4-Bit Equality Comparator (3.3 V and 5 V Core Voltage)

ECOMP4

MACRO	EQUIV. GATES
ECOMP4	16

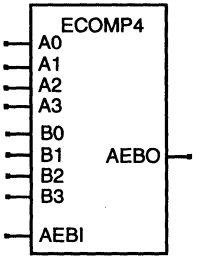
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ECOMP4	AEBO / A0-A3,B0-B3,AEBI

MACRO	INPUT CAP.
ECOMP4	A0-A3,B0-B3: 0.11pF AEBI: 0.05pF

FUNCTION TABLE

Data Words	AEBI	AEBO
A = B	L	L
A Not Equal to B	L	H
X	H	H



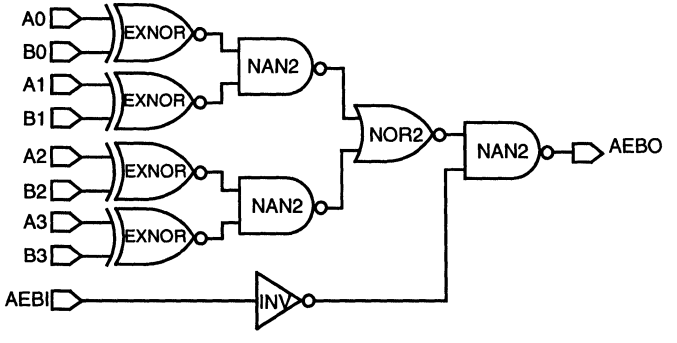
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
ECOMP4									
t_{PLH}	Propagation Delay, A0 to AEBO	0.66	0.74	0.99	0.83	0.96	1.07	1.42	1.16
t_{PHL}		0.84	0.95	1.29	1.15	1.24	1.39	1.84	1.52
t_{PLH}	Propagation Delay, A1 to AEBO	0.64	0.72	0.97	0.83	0.90	1.02	1.36	1.16
t_{PHL}		0.85	0.96	1.31	1.15	1.26	1.41	1.87	1.52
t_{PLH}	Propagation Delay, A2 to AEBO	0.63	0.71	0.96	0.83	0.91	1.02	1.37	1.16
t_{PHL}		0.80	0.91	1.26	1.15	1.17	1.33	1.78	1.52
t_{PLH}	Propagation Delay, A3 to AEBO	0.60	0.69	0.93	0.83	0.87	0.98	1.33	1.16
t_{PHL}		0.80	0.92	1.26	1.15	1.19	1.34	1.79	1.52
t_{PLH}	Propagation Delay, AEBI to AEBO	0.32	0.41	0.65	0.82	0.43	0.54	0.89	1.16
t_{PHL}		0.32	0.43	0.77	1.14	0.44	0.59	1.04	1.51
t_{PLH}	Propagation Delay, B0 to AEBO	0.87	0.95	1.20	0.83	1.29	1.40	1.75	1.15
t_{PHL}		1.03	1.14	1.49	1.15	1.49	1.64	2.10	1.52
t_{PLH}	Propagation Delay, B1 to AEBO	0.85	0.93	1.18	0.83	1.24	1.36	1.71	1.16
t_{PHL}		1.03	1.15	1.49	1.15	1.51	1.66	2.12	1.51
t_{PLH}	Propagation Delay, B2 to AEBO	0.87	0.95	1.20	0.83	1.27	1.39	1.73	1.16
t_{PHL}		1.03	1.14	1.49	1.15	1.47	1.62	2.07	1.52
t_{PLH}	Propagation Delay, B3 to AEBO	0.82	0.90	1.15	0.83	1.22	1.33	1.68	1.16
t_{PHL}		1.01	1.13	1.47	1.14	1.47	1.62	2.07	1.52
t_r	Output Rise Time, AEBO	0.22	0.47	1.20	2.45	0.26	0.61	1.65	3.46
t_f	Output Fall Time, AEBO	0.21	0.41	1.01	1.99	0.29	0.55	1.32	2.56

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: ECOMP4



7

2-Input Exclusive NOR Gate 1X Drive With Unbuffered Input (3.3 V and 5 V Core Voltage)

EXNORA

MACRO	EQUIV. GATES
EXNORA	3

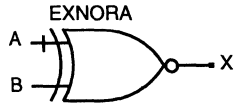
Rev. 1.07

MACRO	OUTPUTS/INPUTS
EXNORA	X / A,B

MACRO	INPUT CAP.
EXNORA	A,B: 0.10pF

FUNCTION TABLE

A	B	X
L	L	H
L	H	L
H	L	L
H	H	H



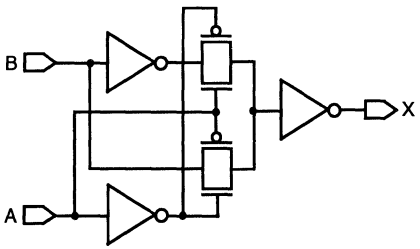
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	EXNORA								
t_{PLH}	Propagation Delay,	0.38	0.46	0.71	0.83	0.49	0.61	0.96	1.16
t_{PHL}	A to X	0.49	0.56	0.80	0.78	0.71	0.81	1.10	0.95
t_{PLH}	Propagation Delay,	0.39	0.48	0.73	0.83	0.53	0.64	0.99	1.16
t_{PHL}	B to X	0.45	0.53	0.77	0.78	0.68	0.78	1.06	0.95
t_r	Output Rise Time, X	0.16	0.41	1.14	2.44	0.19	0.53	1.57	3.44
t_f	Output Fall Time, X	0.21	0.33	0.67	1.16	0.29	0.43	0.85	1.40

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: EXNORA



7

3-Input Exclusive NOR Gate, 2X Drive (3.3 V and 5 V Core Voltage)

EXNOR3H

MACRO	EQUIV. GATES
EXNOR3H	8

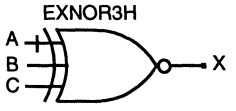
Rev. 1.07

MACRO	OUTPUTS/INPUTS
EXNOR3H	X / A-C

MACRO	INPUT CAP.
EXNOR3H	A,B: 0.12pF C: 0.05pF

FUNCTION TABLE

A	B	C	X
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	H
H	H	H	L



CMOS SWITCHING CHARACTERISTICS

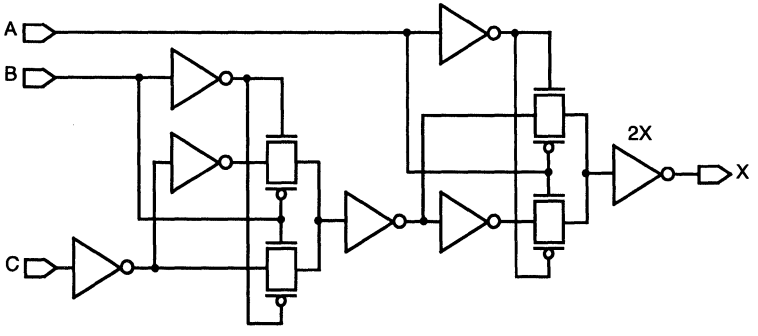
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	EXNOR3H								
t_{PLH}	Propagation Delay, A to X	0.40	0.45	0.57	0.43	0.54	0.60	0.78	0.60
t_{PHL}		0.47	0.52	0.67	0.49	0.73	0.79	0.99	0.65
t_{PLH}	Propagation Delay, B to X	0.82	0.86	0.99	0.42	1.19	1.25	1.43	0.60
t_{PHL}		0.86	0.90	1.03	0.44	1.30	1.36	1.52	0.56
t_{PLH}	Propagation Delay, C to X	1.02	1.06	1.19	0.43	1.46	1.52	1.70	0.60
t_{PHL}		1.02	1.07	1.20	0.44	1.52	1.58	1.74	0.56
t_r	Output Rise Time, X	0.18	0.30	0.66	1.20	0.22	0.39	0.89	1.68
t_f	Output Fall Time, X	0.25	0.31	0.50	0.63	0.35	0.43	0.67	0.80

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: EXNOR3H



2-Input Exclusive OR Gate 1X Drive With Unbuffered Input (3.3 V and 5 V Core Voltage)

EXORA

MACRO	EQUIV. GATES
EXORA	3

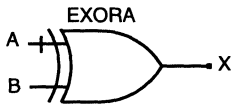
Rev. 1.07

MACRO	OUTPUTS/INPUTS
EXORA	X / A,B

MACRO	INPUT CAP.
EXORA	A,B: 0.10pF

FUNCTION TABLE

A	B	X
L	L	L
L	H	H
H	L	H
H	H	L



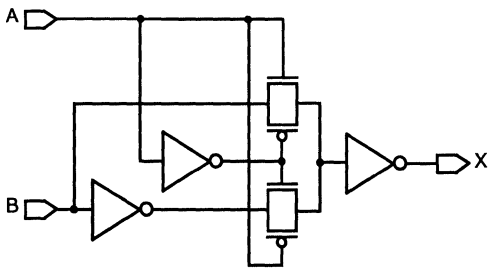
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
EXORA									
t_{PLH}	Propagation Delay, A to X	0.40	0.48	0.73	0.83	0.57	0.69	1.04	1.16
t_{PHL}		0.37	0.45	0.68	0.78	0.57	0.67	0.95	0.94
t_{PLH}	Propagation Delay, B to X	0.40	0.48	0.73	0.83	0.54	0.66	1.01	1.16
t_{PHL}		0.45	0.53	0.77	0.78	0.68	0.77	1.06	0.95
t_r	Output Rise Time, X	0.17	0.41	1.14	2.43	0.22	0.56	1.60	3.46
t_f	Output Fall Time, X	0.22	0.34	0.69	1.16	0.30	0.44	0.86	1.41

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: EXORA



7

3-Input Exclusive OR Gate, 2X Drive (3.3 V and 5 V Core Voltage)

EXOR3H

MACRO	EQUIV. GATES
EXOR3H	8

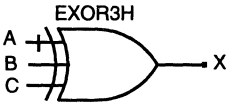
Rev. 1.07

MACRO	OUTPUTS/INPUTS
EXOR3H	X / A-C

MACRO	INPUT CAP.
EXOR3H	A,B: 0.11pF C: 0.05pF

FUNCTION TABLE

A	B	C	X
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	H



CMOS SWITCHING CHARACTERISTICS

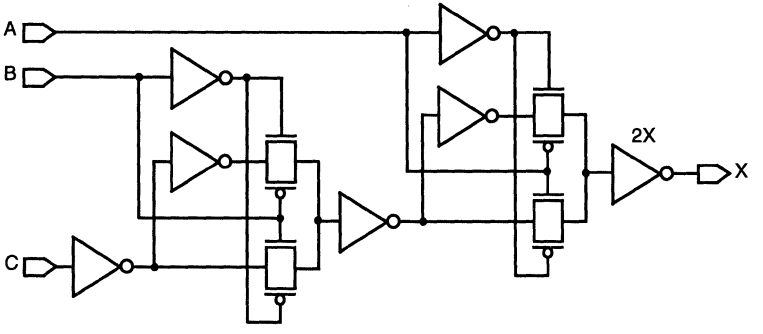
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	EXOR3H								
t_{PLH}	Propagation Delay, A to X	0.45	0.50	0.63	0.45	0.60	0.67	0.86	0.63
t_{PHL}		0.45	0.49	0.62	0.43	0.68	0.74	0.90	0.55
t_{PLH}	Propagation Delay, B to X	0.83	0.87	1.00	0.43	1.20	1.26	1.44	0.60
t_{PHL}		0.86	0.91	1.04	0.44	1.30	1.36	1.53	0.56
t_{PLH}	Propagation Delay, C to X	1.01	1.06	1.19	0.43	1.47	1.53	1.71	0.59
t_{PHL}		1.02	1.06	1.19	0.44	1.51	1.56	1.73	0.56
t_r	Output Rise Time, X	0.19	0.31	0.67	1.20	0.27	0.44	0.94	1.68
t_f	Output Fall Time, X	0.23	0.29	0.47	0.58	0.35	0.42	0.63	0.71

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: EXOR3H



4-Input Exclusive OR Gate, 2X Drive (3.3 V and 5 V Core Voltage)

EXOR4H

MACRO	EQUIV. GATES
EXOR4H	10

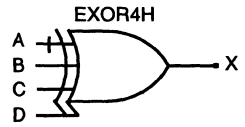
Rev. 1.07

MACRO	OUTPUTS/INPUTS
EXOR4H	X / A-D

MACRO	INPUT CAP.
EXOR4H	A,C: 0.11pF B,D: 0.05pF

FUNCTION TABLE

Number of Inputs A through D that are HIGH	X
0,2,4	L
1,3	H



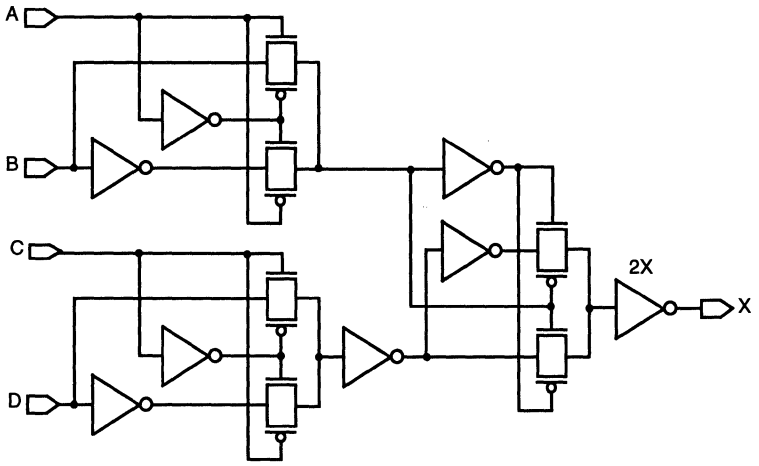
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
EXOR4H									
t_{PLH}	Propagation Delay, A to X	0.76	0.81	0.93	0.43	1.15	1.21	1.39	0.59
t_{PHL}		0.90	0.95	1.10	0.50	1.41	1.48	1.67	0.65
t_{PLH}	Propagation Delay, B to X	0.89	0.93	1.06	0.42	1.23	1.29	1.47	0.59
t_{PHL}		1.01	1.06	1.21	0.50	1.58	1.65	1.84	0.65
t_{PLH}	Propagation Delay, C to X	0.75	0.79	0.93	0.45	1.04	1.11	1.30	0.63
t_{PHL}		0.77	0.82	0.97	0.52	1.18	1.26	1.47	0.70
t_{PLH}	Propagation Delay, D to X	0.84	0.88	1.02	0.45	1.13	1.19	1.38	0.63
t_{PHL}		0.89	0.94	1.10	0.52	1.36	1.43	1.64	0.71
t_r	Output Rise Time, X	0.26	0.38	0.73	1.18	0.31	0.48	0.98	1.69
t_f	Output Fall Time, X	0.42	0.48	0.67	0.61	0.57	0.65	0.88	0.77

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: EXOR4H



4-Bit Incrementer, 2X Drive (3.3 V and 5 V Core Voltage)

INC4H

MACRO	EQUIV. GATES
INC4H	28

Rev. 1.07

MACRO	OUTPUTS/INPUTS
INC4H	S0-S3,CO,PR / A0-A3,CI

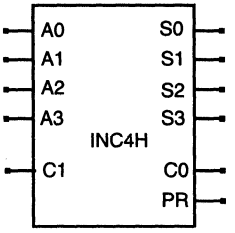
MACRO	INPUT CAP.
INC4H	A0-A2: 0.23pF A3: 0.10pF CI: 0.17pF

FUNCTION TABLE

A0-A3	CI	S0-S3	CO	PR
H(All)	L	H(All)	L	H
H(All)	H	L(All)	H	H
X(All)*	L	(A0-A3)	L	L
X(All)*	H	(A0-A3)+1	L	L

NOTE: A0,S0 = LSB, A3,S3 = MSB

* Indicates don't care for all states except H(All)



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	INC4H								
t_{PLH}	Propagation Delay, A0 to CO	0.98	1.02	1.15	0.42	1.27	1.33	1.51	0.59
t_{PHL}		0.56	0.60	0.72	0.39	0.88	0.93	1.07	0.48
t_{PLH}	Propagation Delay, A0 to PR	0.69	0.74	0.87	0.44	0.88	0.95	1.14	0.64
t_{PHL}		0.34	0.38	0.49	0.40	0.54	0.58	0.73	0.48
t_{PLH}	Propagation Delay, A0 to S0 & A1 to S1 & A2 to S2 & A3 to S3	0.40	0.44	0.57	0.42	0.53	0.59	0.77	0.60
t_{PHL}		0.43	0.48	0.61	0.44	0.65	0.70	0.87	0.55
t_{PLH}	Propagation Delay, A0 to S1 & A1 to S2	0.93	0.98	1.10	0.43	1.26	1.32	1.50	0.60
t_{PHL}		0.88	0.93	1.06	0.45	1.34	1.40	1.57	0.57
t_{PLH}	Propagation Delay, A0 to S2	1.32	1.37	1.49	0.43	1.83	1.89	2.07	0.60
t_{PHL}		1.27	1.32	1.45	0.45	1.89	1.95	2.12	0.57
t_{PLH}	Propagation Delay, A0 to S3	1.60	1.64	1.77	0.42	2.24	2.30	2.48	0.59
t_{PHL}		1.51	1.56	1.69	0.44	2.26	2.32	2.48	0.55
t_{PLH}	Propagation Delay, A1 to CO	1.00	1.05	1.17	0.42	1.33	1.39	1.56	0.59
t_{PHL}		0.62	0.66	0.78	0.39	0.96	1.01	1.15	0.47
t_{PLH}	Propagation Delay, A1 to PR	0.72	0.76	0.90	0.44	0.94	1.01	1.20	0.64
t_{PHL}		0.40	0.44	0.56	0.40	0.61	0.66	0.81	0.49
t_{PLH}	Propagation Delay, A1 to S3	1.22	1.27	1.39	0.42	1.29	1.35	1.53	0.60
t_{PHL}		1.14	1.18	1.32	0.44	1.36	1.42	1.59	0.57
t_{PLH}	Propagation Delay, A2 to CO	1.05	1.09	1.22	0.42	1.69	1.75	1.93	0.60
t_{PHL}		0.69	0.73	0.85	0.39	1.73	1.78	1.95	0.55
t_{PLH}	Propagation Delay, A2 to PR	0.76	0.80	0.93	0.44	1.42	1.48	1.65	0.59
t_{PHL}		0.47	0.51	0.63	0.40	1.04	1.09	1.23	0.48
t_{PLH}	Propagation Delay, A2 to S3	0.83	0.87	1.00	0.42	1.02	1.09	1.28	0.64
t_{PHL}		0.76	0.81	0.94	0.44	0.71	0.76	0.91	0.50
t_{PLH}	Propagation Delay, A3 to CO	1.02	1.06	1.18	0.42	1.14	1.20	1.37	0.60
t_{PHL}		0.73	0.77	0.89	0.39	1.18	1.24	1.40	0.55
t_{PLH}	Propagation Delay, A3 to PR	0.73	0.77	0.90	0.44	1.41	1.46	1.64	0.59
t_{PHL}		0.52	0.56	0.68	0.41	1.09	1.14	1.28	0.48

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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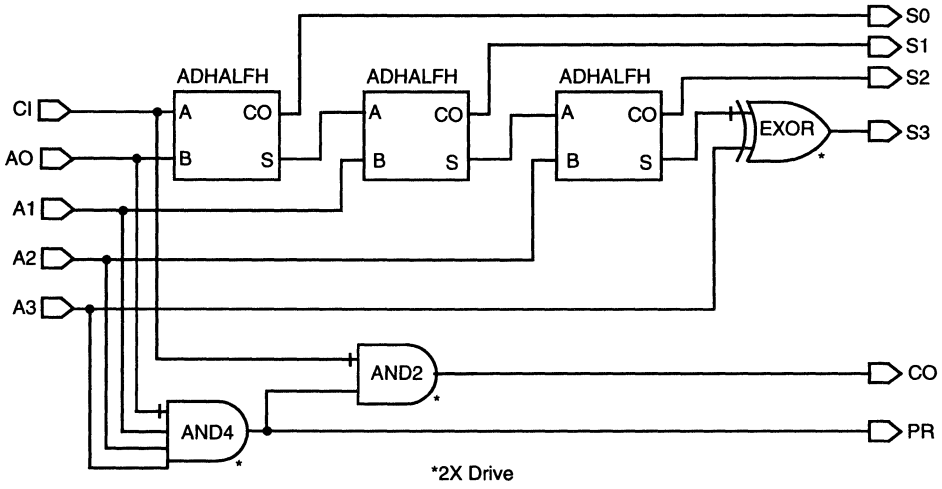
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay, CI to CO	0.42	0.46	0.59	0.42	1.02	1.08	1.27	0.64
t_{PHL}		0.37	0.41	0.53	0.39	0.75	0.80	0.95	0.50
t_{PLH}	Propagation Delay, CI to S0	0.58	0.62	0.74	0.42	0.54	0.60	0.78	0.59
t_{PHL}		0.61	0.65	0.79	0.45	0.53	0.58	0.72	0.48
t_{PLH}	Propagation Delay, CI to S1	0.91	0.95	1.08	0.43	0.75	0.81	0.99	0.60
t_{PHL}		0.96	1.00	1.14	0.45	0.91	0.97	1.14	0.57
t_{PLH}	Propagation Delay, CI to S2	1.31	1.36	1.48	0.42	1.25	1.31	1.49	0.60
t_{PHL}		1.34	1.38	1.52	0.45	1.41	1.46	1.64	0.57
t_{PLH}	Propagation Delay, CI to S3	1.59	1.63	1.76	0.42	1.80	1.86	2.05	0.61
t_{PHL}		1.59	1.63	1.76	0.44	1.96	2.01	2.18	0.57
t_r	Output Rise Time, CO	0.15	0.27	0.63	1.21	0.18	0.35	0.86	1.70
t_f	Output Fall Time, CO	0.16	0.22	0.39	0.58	0.20	0.27	0.48	0.70
t_r	Output Rise Time, PR	0.31	0.43	0.79	1.19	0.42	0.59	1.10	1.69
t_f	Output Fall Time, PR	0.26	0.32	0.49	0.58	0.32	0.39	0.60	0.70
t_r	Output Rise Time, S0	0.18	0.30	0.66	1.20	0.24	0.41	0.91	1.68
t_f	Output Fall Time, S0	0.28	0.34	0.52	0.60	0.39	0.46	0.68	0.71
t_r	Output Rise Time, S1,S2	0.21	0.33	0.69	1.20	0.24	0.41	0.91	1.68
t_f	Output Fall Time, S1,S2	0.29	0.35	0.53	0.60	0.39	0.46	0.68	0.71
t_r	Output Rise Time, S3	0.17	0.29	0.65	1.20	0.22	0.39	0.90	1.70
t_f	Output Fall Time, S3	0.22	0.28	0.46	0.60	0.31	0.38	0.59	0.72

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: INC4H



*2X Drive

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Inverter, 1X Drive (3.3 V and 5 V Core Voltage)

INV
INVB

MACRO	EQUIV. GATES
All	1

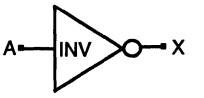
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A

MACRO	INPUT CAP.
INV	A: 0.05pF
INVB	A: 0.07pF

FUNCTION TABLE

A	X
L	H
H	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	INV								
t_{PLH}	Propagation Delay, A to X	0.14	0.22	0.46	0.82	0.17	0.28	0.63	1.15
t_{PHL}		0.22	0.30	0.52	0.76	0.29	0.38	0.66	0.91
t_r	Output Rise Time, X	0.16	0.40	1.13	2.42	0.19	0.53	1.56	3.44
t_f	Output Fall Time, X	0.16	0.27	0.62	1.15	0.17	0.31	0.73	1.41
	INVB								
t_{PLH}	Propagation Delay, A to X	0.06	0.10	0.22	0.42	0.10	0.16	0.34	0.58
t_{PHL}		0.27	0.34	0.57	0.75	0.32	0.41	0.68	0.91
t_r	Output Rise Time, X	0.17	0.29	0.64	1.16	0.17	0.33	0.84	1.68
t_f	Output Fall Time, X	0.16	0.28	0.62	1.15	0.17	0.32	0.74	1.41

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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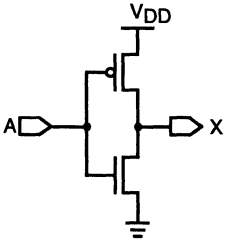
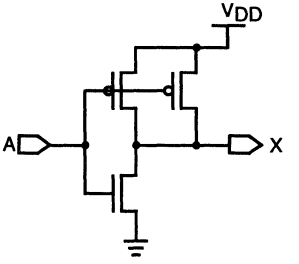
FUNCTIONAL DIAGRAM: INV



FUNCTIONAL DIAGRAM: INVB



Inverter, 2X Drive (3.3 V and 5 V Core Voltage)

INV2 INV2B

MACRO	EQUIV. GATES
INV2	1
INV2B	2

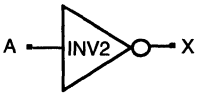
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A

MACRO	INPUT CAP.
INV2	A: 0.09pF
INV2B	A: 0.14pF

FUNCTION TABLE

A	X
L	H
H	L



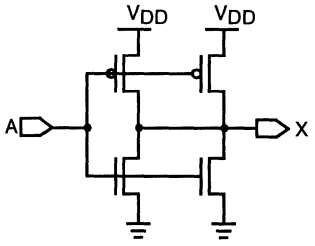
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

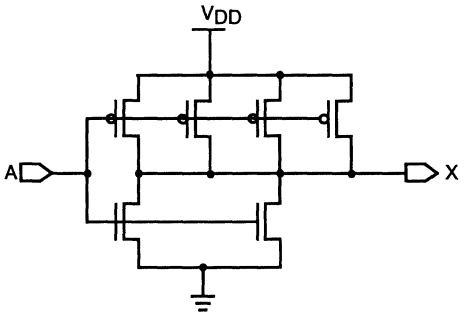
Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
INV2									
t_{PLH}	Propagation Delay, A to X	0.11	0.15	0.27	0.41	0.13	0.19	0.36	0.58
t_{PHL}		0.19	0.23	0.34	0.38	0.24	0.29	0.43	0.46
t_r	Output Rise Time, X	0.16	0.28	0.63	1.18	0.17	0.34	0.85	1.69
t_f	Output Fall Time, X	0.19	0.25	0.41	0.54	0.15	0.22	0.42	0.68
INV2B									
t_{PLH}	Propagation Delay, A to X	0.03	0.05	0.12	0.22	0.08	0.11	0.19	0.29
t_{PHL}		0.25	0.29	0.40	0.38	0.29	0.33	0.47	0.46
t_r	Output Rise Time, X	0.19	0.25	0.41	0.54	0.18	0.26	0.51	0.81
t_f	Output Fall Time, X	0.17	0.23	0.39	0.55	0.17	0.24	0.44	0.67

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: INV2



FUNCTIONAL DIAGRAM: INV2B



7

Inverter, 4X Drive (3.3 V and 5 V Core Voltage)

INV4 INV4B

MACRO	EQUIV. GATES
INV4	2
INV4B	4

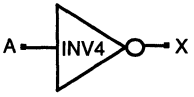
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A

MACRO	INPUT CAP.
INV4	A: 0.19pF
INV4B	A: 0.28pF

FUNCTION TABLE

A	X
L	H
H	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	INV4								
t_{PLH}	Propagation Delay,	0.10	0.12	0.18	0.21	0.11	0.14	0.23	0.29
t_{PHL}	A to X	0.15	0.17	0.23	0.20	0.22	0.24	0.31	0.24
t_r	Output Rise Time, X	0.20	0.26	0.42	0.55	0.20	0.28	0.53	0.82
t_f	Output Fall Time, X	0.17	0.19	0.27	0.26	0.16	0.20	0.29	0.32
	INV4B								
t_{PLH}	Propagation Delay,	0.01	0.02	0.06	0.13	0.06	0.08	0.12	0.15
t_{PHL}	A to X	0.24	0.26	0.32	0.19	0.27	0.30	0.37	0.23
t_r	Output Rise Time, X	0.22	0.24	0.32	0.24	0.21	0.25	0.37	0.38
t_f	Output Fall Time, X	0.19	0.22	0.30	0.26	0.20	0.23	0.32	0.32

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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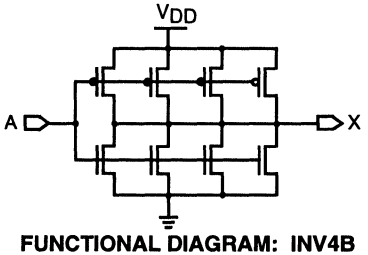
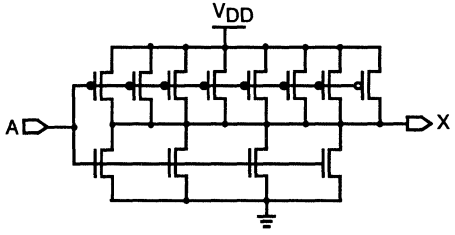
FUNCTIONAL DIAGRAM: INV4



FUNCTIONAL DIAGRAM: INV4B



Inverter, 8X Drive (3.3 V and 5 V Core Voltage)

INV8
INV8B

MACRO	EQUIV. GATES
INV8	4
INV8B	8

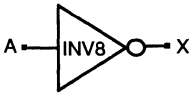
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A

MACRO	INPUT CAP.
INV8	A: 0.37pF
INV8B	A: 0.57pF

FUNCTION TABLE

A	X
L	H
H	L



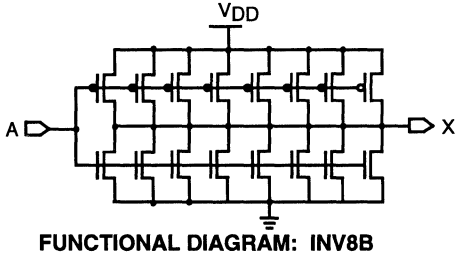
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

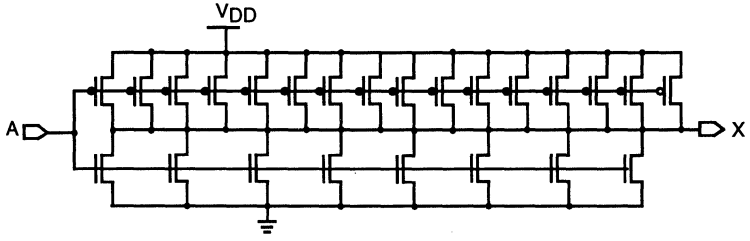
Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	INV8								
t_{PLH}	Propagation Delay, A to X	0.09	0.10	0.13	0.11	0.11	0.12	0.17	0.15
t_{PHL}		0.14	0.15	0.18	0.12	0.20	0.22	0.26	0.13
t_r	Output Rise Time, X	0.17	0.20	0.28	0.28	0.21	0.25	0.37	0.39
t_f	Output Fall Time, X	0.17	0.18	0.22	0.13	0.18	0.19	0.24	0.16
	INV8B								
t_{PLH}	Propagation Delay, A to X	-0.01	0.00	0.02	0.08	0.04	0.05	0.08	0.09
t_{PHL}		0.23	0.24	0.27	0.10	0.25	0.26	0.30	0.13
t_r	Output Rise Time, X	0.23	0.24	0.28	0.11	0.25	0.27	0.32	0.17
t_f	Output Fall Time, X	0.19	0.20	0.24	0.13	0.18	0.20	0.25	0.16

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: INV8



FUNCTIONAL DIAGRAM: INV8B



7

Invertering 3-state Buffer, Active Low Enable 1X & 2X Drive (3.3 V and 5 V Core Voltage)

INVT
INVTH

MACRO	EQUIV. GATES
INVT	2
INVTH	3

Rev. 1.07

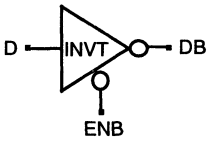
MACRO	OUTPUTS/INPUTS
All	DB / D,ENB

MACRO	INPUT CAP.
INVT	D: 0.05pF ENB: 0.07pF
INVTH	D,ENB: 0.09pF

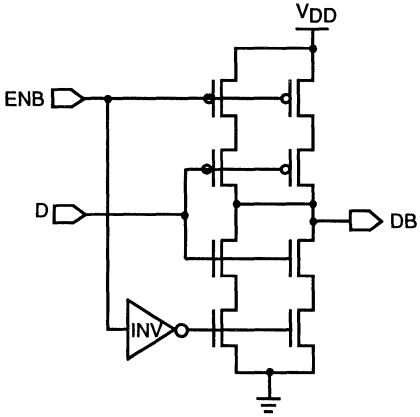
MACRO	OUTPUT CAP.
INVT	DB: 0.06pF
INVTH	DB: 0.11pF

FUNCTION TABLE

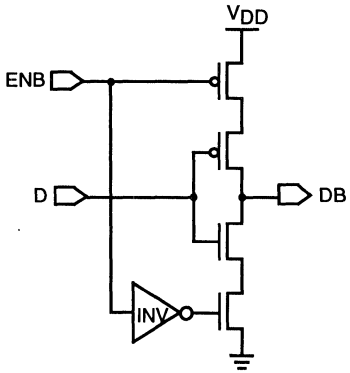
D	ENB	DB
L	L	H
H	L	L
X	H	Z



FUNCTIONAL DIAGRAM: INVTH



FUNCTIONAL DIAGRAM: INVT



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
INVT									
t_{PLH}	Propagation Delay, D to DB	0.15	0.31	0.79	1.60	0.20	0.44	1.14	2.36
t_{PHL}		0.24	0.35	0.69	1.14	0.31	0.46	0.91	1.50
t_{PLZ}	Propagation Delay, ENB to DB	0.26	0.26	0.26	0.00	0.34	0.34	0.34	0.00
t_{PZL}		0.68	0.79	1.13	1.14	0.80	0.95	1.40	1.50
t_{PZH}	Propagation Delay, ENB to DB	0.38	0.54	1.02	1.61	0.48	0.72	1.43	2.36
t_{PHZ}		0.44	0.44	0.44	0.00	0.50	0.50	0.50	0.00
t_r	Output Rise Time, DB	0.24	0.73	2.19	4.86	0.33	1.03	3.13	7.00
t_f	Output Fall Time, DB	0.19	0.38	0.97	1.95	0.21	0.46	1.21	2.52
INVTH									
t_{PLH}	Propagation Delay, D to DB	0.17	0.25	0.49	0.80	0.22	0.34	0.69	1.18
t_{PHL}		0.23	0.29	0.46	0.57	0.31	0.38	0.61	0.75
t_{PLZ}	Propagation Delay, ENB to DB	0.31	0.31	0.31	0.00	0.40	0.40	0.40	0.00
t_{PZL}		0.73	0.79	0.96	0.57	0.85	0.92	1.15	0.76
t_{PZH}	Propagation Delay, ENB to DB	0.41	0.49	0.73	0.81	0.52	0.64	1.00	1.18
t_{PHZ}		0.45	0.45	0.45	0.00	0.53	0.53	0.53	0.00
t_r	Output Rise Time, DB	0.29	0.53	1.25	2.41	0.37	0.72	1.77	3.49
t_f	Output Fall Time, DB	0.22	0.32	0.60	0.94	0.23	0.35	0.72	1.23

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

Invertering 3-state Buffer, Active HIGH Enable 1X & 2X Drive (3.3 V and 5 V Core Voltage)

INVTP
INVTPH

MACRO	EQUIV. GATES
INVTP	3
INVTPH	4

Rev. 1.07

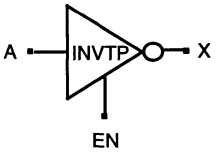
MACRO	OUTPUTS/INPUTS
All	X / A,EN

MACRO	INPUT CAP.
INVTP	A: 0.05pF EN: 0.07pF
INVTPH	A: 0.05pF EN: 0.09pF

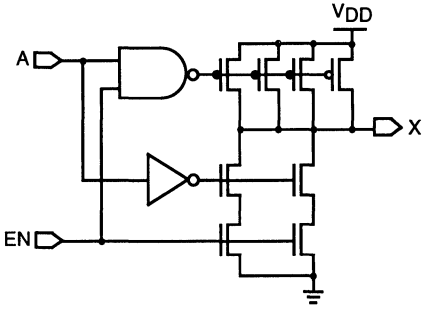
MACRO	OUTPUT CAP.
INVTP	X: 0.06pF
INVTPH	X: 0.12pF

FUNCTION TABLE

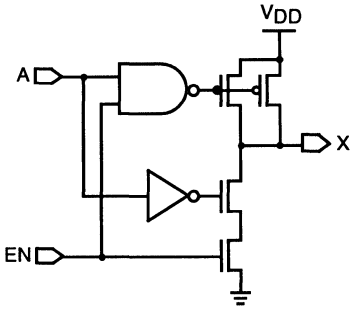
A	EN	X
L	H	H
H	H	L
X	L	Z



FUNCTIONAL DIAGRAM: INVTPH



FUNCTIONAL DIAGRAM: INVTP



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
INVTP									
t_{PLH}	Propagation Delay, A to X	0.48	0.52	0.65	0.43	0.65	0.71	0.89	0.59
t_{PHL}		0.51	0.62	0.96	1.14	0.68	0.83	1.28	1.49
t_{PLZ}	Propagation Delay, EN to X	0.32	0.31	0.31	0.00	0.36	0.36	0.36	0.00
t_{PZL}		0.42	0.53	0.86	1.10	0.49	0.64	1.07	1.46
t_{PZH}	Propagation Delay, EN to X	0.60	0.64	0.77	0.43	0.72	0.77	0.95	0.59
t_{PHZ}		0.45	0.45	0.45	0.00	0.59	0.59	0.59	0.00
t_r	Output Rise Time, X	0.12	0.24	0.60	1.20	0.16	0.33	0.84	1.70
t_f	Output Fall Time, X	0.14	0.34	0.93	1.99	0.20	0.45	1.21	2.54
INVTPH									
t_{PLH}	Propagation Delay, A to X	0.51	0.53	0.60	0.23	0.71	0.74	0.84	0.32
t_{PHL}		0.57	0.62	0.79	0.56	0.75	0.83	1.05	0.74
t_{PLZ}	Propagation Delay, EN to X	0.29	0.29	0.29	0.00	0.34	0.34	0.34	0.00
t_{PZL}		0.40	0.46	0.63	0.56	0.48	0.55	0.77	0.74
t_{PZH}	Propagation Delay, EN to X	0.63	0.65	0.72	0.23	0.75	0.78	0.88	0.32
t_{PHZ}		0.60	0.60	0.60	0.00	0.78	0.78	0.78	0.00
t_r	Output Rise Time, X	0.17	0.23	0.40	0.58	0.20	0.29	0.54	0.83
t_f	Output Fall Time, X	0.20	0.30	0.59	0.96	0.24	0.36	0.74	1.24

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

Inverted Buffer, High Drive (Use Output Buffer From I/O Site) (3.3 V and 5 V Core Voltage)

INVX

MACRO	EQUIV. GATES
INVX	1/0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
INVX	X / A

MACRO	INPUT CAP.
INVX	A: 0.16pF

FUNCTION TABLE

A	X
L	H
H	L

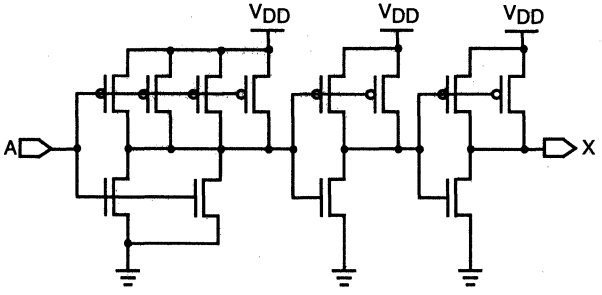
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	INVX								
t_{PLH}	Propagation Delay,	0.33	0.34	0.35	0.05	0.45	0.46	0.48	0.07
t_{PHL}	A to X	0.44	0.45	0.47	0.07	0.58	0.58	0.61	0.09
t_r	Output Rise Time, X	0.10	0.11	0.14	0.10	0.15	0.16	0.20	0.12
t_f	Output Fall Time, X	0.20	0.21	0.23	0.08	0.20	0.21	0.24	0.10

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: INVX



7

4-Bit Look Ahead Carry Generator (3.3V and 5V Core Voltage)

LACG4

MACRO	EQUIV. GATES
LACG4	32

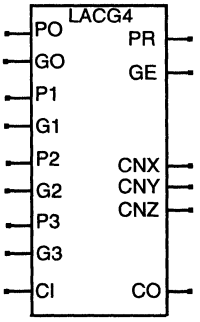
Rev. 1.07

MACRO	OUTPUTS/INPUTS
LACG4	CNX-CNZ,CO,PR,GE / CI,P0,G0,P1,G1,P2,G2,P3,G3

MACRO	INPUT CAP.
LACG4	CI,G0,P0,P2,P3: 0.23pF G1: 0.17pF G2: 0.10pF G3: 0.05pF P1: 0.19pF

FUNCTION TABLE

PROPAGATE (PROPAGATE THE CARRY BIT)
PR = (P0*P1*P2*P3)
GENERATE (GENERATE A CARRY BIT)
GE = (P1*P2*P3*G0) + (P2*P3*G1) + (P3*G2) + G3
CNX = CARRY FOR FIRST STAGE
CNX = (P0*CI) + G0
CNY = CARRY FOR SECOND STAGE
CNY = (P0*P1*CI) + (P1 *G0) + G1
CNZ = CARRY FOR THIRD STAGE
CNZ = (P0*P1*P2*CI) + (P1*P2*G0) + (P2*G1) + G2
CO = OVERALL CARRY OUT
CO = (PR*CI) + GE



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	LACG4								
t_{PLH}	Propagation Delay, CI to CNX	0.39	0.48	0.73	0.83	0.52	0.63	0.98	1.16
t_{PHL}		0.29	0.40	0.74	1.14	0.42	0.57	1.02	1.50
t_{PLH}	Propagation Delay, CI to CNY	0.52	0.60	0.85	0.83	0.68	0.80	1.15	1.17
t_{PHL}		0.34	0.49	0.96	1.54	0.51	0.72	1.35	2.11
t_{PLH}	Propagation Delay, CI to CNZ	0.62	0.71	0.96	0.85	0.82	0.94	1.30	1.19
t_{PHL}		0.38	0.57	1.16	1.95	0.57	0.84	1.66	2.71
t_{PLH}	Propagation Delay, CI to CO	0.47	0.51	0.63	0.42	0.60	0.66	0.83	0.59
t_{PHL}		0.35	0.41	0.58	0.58	0.51	0.58	0.81	0.76
t_{PLH}	Propagation Delay, G0 to CNX	0.33	0.41	0.66	0.83	0.46	0.58	0.92	1.16
t_{PHL}		0.30	0.41	0.75	1.14	0.43	0.58	1.03	1.50
t_{PLH}	Propagation Delay, G0 to CNY	0.42	0.50	0.75	0.83	0.59	0.70	1.05	1.16
t_{PHL}		0.41	0.57	1.03	1.54	0.60	0.81	1.44	2.11
t_{PLH}	Propagation Delay, G0 to CNZ	0.55	0.63	0.88	0.84	0.74	0.85	1.20	1.17
t_{PHL}		0.39	0.59	1.18	1.96	0.60	0.87	1.69	2.71
t_{PLH}	Propagation Delay, G0 to CO	1.01	1.05	1.18	0.42	1.38	1.44	1.62	0.59
t_{PHL}		0.93	0.99	1.16	0.58	1.38	1.46	1.69	0.77
t_{PLH}	Propagation Delay, G0 to GE	0.97	1.05	1.30	0.82	1.33	1.45	1.79	1.16
t_{PHL}		0.92	0.99	1.23	0.77	1.38	1.47	1.75	0.94
t_{PLH}	Propagation Delay, G1 to CNY	0.38	0.46	0.71	0.83	0.52	0.64	0.99	1.17
t_{PHL}		0.38	0.54	1.00	1.54	0.54	0.75	1.38	2.10
t_{PLH}	Propagation Delay, G1 to CNZ	0.50	0.58	0.83	0.83	0.68	0.79	1.14	1.17
t_{PHL}		0.45	0.65	1.23	1.96	0.67	0.94	1.76	2.71
t_{PLH}	Propagation Delay, G1 to CO	0.99	1.03	1.16	0.42	1.37	1.43	1.60	0.59
t_{PHL}		0.97	1.03	1.21	0.58	1.44	1.51	1.74	0.77
t_{PLH}	Propagation Delay, G1 to GE	0.98	1.06	1.31	0.82	1.32	1.44	1.79	1.16
t_{PHL}		0.95	1.03	1.26	0.77	1.44	1.53	1.81	0.93
t_{PLH}	Propagation Delay, G2 to CNZ	0.41	0.49	0.75	0.84	0.57	0.69	1.04	1.18
t_{PHL}		0.49	0.68	1.27	1.95	0.68	0.95	1.77	2.72
t_{PLH}	Propagation Delay, G2 to CO	0.94	0.98	1.10	0.42	1.31	1.37	1.55	0.59
t_{PHL}		1.01	1.07	1.24	0.58	1.49	1.56	1.79	0.76
t_{PLH}	Propagation Delay, G2 to GE	0.91	0.99	1.24	0.83	1.26	1.38	1.73	1.16
t_{PHL}		1.00	1.08	1.31	0.77	1.48	1.57	1.85	0.93

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

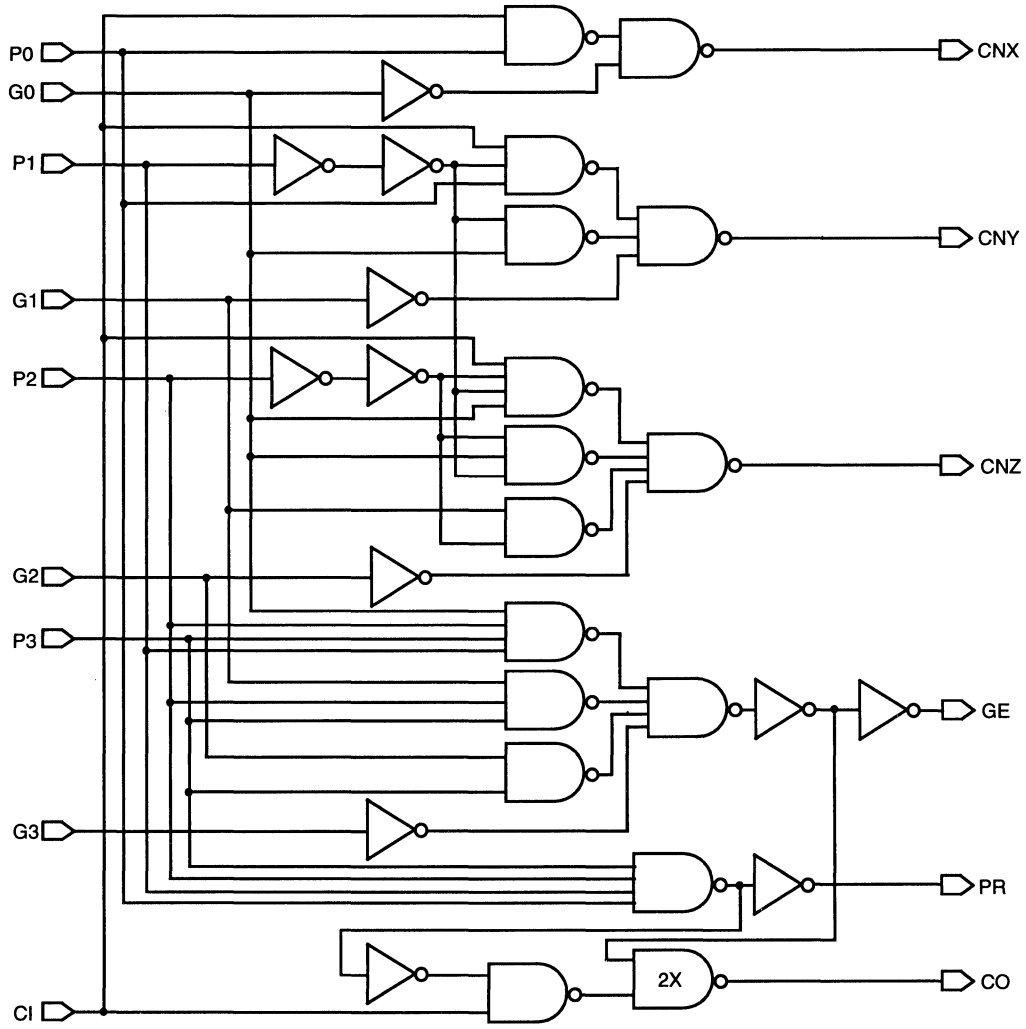
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay, G3 to CO	0.87	0.91	1.03	0.42	1.22	1.28	1.45	0.59
t_{PHL}		1.04	1.09	1.27	0.58	1.47	1.55	1.78	0.77
t_{PLH}	Propagation Delay, G3 to GE	0.85	0.93	1.18	0.82	1.17	1.29	1.64	1.16
t_{PHL}		1.03	1.10	1.33	0.77	1.47	1.56	1.84	0.94
t_{PLH}	Propagation Delay, P0 to CNX	0.37	0.45	0.70	0.83	0.51	0.62	0.97	1.16
t_{PHL}		0.37	0.48	0.82	1.13	0.52	0.67	1.11	1.50
t_{PLH}	Propagation Delay, P0 to CNY	0.52	0.60	0.85	0.83	0.74	0.85	1.20	1.17
t_{PHL}		0.48	0.64	1.10	1.54	0.69	0.90	1.54	2.11
t_{PLH}	Propagation Delay, P0 to CNZ	0.66	0.75	1.00	0.85	0.97	1.09	1.44	1.19
t_{PHL}		0.56	0.76	1.35	1.96	0.81	1.08	1.90	2.72
t_{PLH}	Propagation Delay, P0 to CO	1.13	1.17	1.30	0.42	1.56	1.62	1.80	0.59
t_{PHL}		0.85	0.91	1.08	0.58	1.26	1.34	1.57	0.76
t_{PLH}	Propagation Delay, P0 to PR	0.76	0.85	1.10	0.86	1.05	1.18	1.54	1.21
t_{PHL}		0.49	0.57	0.80	0.77	0.73	0.83	1.11	0.94
t_{PLH}	Propagation Delay, P1 to CNY	0.96	1.04	1.29	0.83	1.36	1.48	1.83	1.17
t_{PHL}		0.85	1.00	1.47	1.54	1.16	1.37	2.00	2.10
t_{PLH}	Propagation Delay, P1 to CNZ	1.09	1.18	1.43	0.85	1.59	1.71	2.06	1.19
t_{PHL}		0.95	1.15	1.73	1.96	1.31	1.58	2.39	2.71
t_{PLH}	Propagation Delay, P1 to CO	1.05	1.09	1.22	0.42	1.53	1.59	1.76	0.59
t_{PHL}		1.12	1.18	1.36	0.58	1.62	1.70	1.93	0.77
t_{PLH}	Propagation Delay, P1 to GE	1.02	1.10	1.35	0.83	1.48	1.59	1.94	1.16
t_{PHL}		1.12	1.20	1.43	0.77	1.62	1.72	2.00	0.94
t_{PLH}	Propagation Delay, P1 to PR	0.74	0.82	1.08	0.86	1.05	1.17	1.53	1.21
t_{PHL}		0.52	0.60	0.84	0.78	0.78	0.87	1.16	0.95
t_{PLH}	Propagation Delay, P2 to CNZ	0.99	1.07	1.32	0.85	1.40	1.52	1.88	1.19
t_{PHL}		0.85	1.04	1.63	1.95	1.15	1.43	2.24	2.71
t_{PLH}	Propagation Delay, P2 to CO	1.03	1.08	1.20	0.42	1.44	1.50	1.67	0.58
t_{PHL}		1.01	1.07	1.24	0.58	1.46	1.54	1.77	0.76
t_{PLH}	Propagation Delay, P2 to GE	1.00	1.08	1.33	0.83	1.38	1.50	1.84	1.16
t_{PHL}		1.00	1.08	1.31	0.77	1.45	1.55	1.83	0.94
t_{PLH}	Propagation Delay, P2 to PR	0.73	0.81	1.07	0.86	0.97	1.09	1.46	1.21
t_{PHL}		0.42	0.50	0.73	0.77	0.63	0.73	1.01	0.94
t_{PLH}	Propagation Delay, P3 to CO	1.06	1.10	1.23	0.42	1.51	1.57	1.74	0.59
t_{PHL}		1.08	1.14	1.31	0.58	1.56	1.64	1.87	0.76
t_{PLH}	Propagation Delay, P3 to GE	1.04	1.12	1.37	0.82	1.46	1.58	1.92	1.16
t_{PHL}		1.07	1.15	1.38	0.77	1.55	1.65	1.93	0.94
t_{PLH}	Propagation Delay, P3 to PR	0.71	0.79	1.05	0.85	0.91	1.03	1.40	1.21
t_{PHL}		0.36	0.44	0.67	0.77	0.55	0.65	0.93	0.93
t_r	Output Rise Time, CNX	0.20	0.45	1.18	2.44	0.26	0.61	1.64	3.45
t_f	Output Fall Time, CNX	0.17	0.36	0.96	1.99	0.21	0.47	1.23	2.55
t_r	Output Rise Time, CNY	0.34	0.58	1.32	2.44	0.45	0.80	1.83	3.45
t_f	Output Fall Time, CNY	0.29	0.57	1.41	2.80	0.37	0.73	1.83	3.66
t_r	Output Rise Time, CNZ	0.45	0.69	1.42	2.43	0.59	0.94	1.97	3.43
t_f	Output Fall Time, CNZ	0.43	0.80	1.89	3.63	0.54	1.02	2.46	4.79
t_r	Output Rise Time, CO	0.26	0.38	0.75	1.20	0.34	0.51	1.02	1.70
t_f	Output Fall Time, CO	0.22	0.31	0.60	0.97	0.28	0.41	0.78	1.24
t_r	Output Rise Time, GE	0.17	0.41	1.14	2.43	0.20	0.54	1.58	3.45
t_f	Output Fall Time, GE	0.21	0.32	0.67	1.16	0.28	0.42	0.83	1.39
t_r	Output Rise Time, PR	0.30	0.54	1.26	2.40	0.36	0.70	1.72	3.39
t_f	Output Fall Time, PR	0.23	0.34	0.69	1.16	0.28	0.42	0.85	1.42

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: LACG4



D-Type Latch, Negative Gate Latched 1x & 2x Drive (3.3V and 5V Core Voltage)

LATN
LATNH

MACRO	EQUIV. GATES
LATN	5
LATNH	6

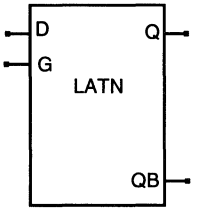
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	Q,QB / D,G

MACRO	INPUT CAP.
All	D,G: 0.05pF

FUNCTION TABLE

Dn	G	Q	QB
L	H	L	H
H	H	H	L
X	L	Q	QB



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
LATN									
t_{PLH}	Propagation Delay, D to Q	0.52	0.61	0.86	0.83	0.71	0.83	1.18	1.16
t_{PHL}		0.56	0.64	0.88	0.80	0.83	0.93	1.23	0.99
t_{PLH}	Propagation Delay, D to QB	0.70	0.78	1.03	0.83	1.01	1.13	1.48	1.16
t_{PHL}		0.76	0.83	1.06	0.77	1.04	1.14	1.41	0.93
t_{PLH}	Propagation Delay, G to Q	0.67	0.75	1.00	0.83	0.93	1.05	1.40	1.17
t_{PHL}		0.71	0.79	1.03	0.80	1.05	1.15	1.44	0.98
t_{PLH}	Propagation Delay, G to QB	0.86	0.94	1.19	0.83	1.23	1.34	1.69	1.16
t_{PHL}		0.89	0.97	1.20	0.76	1.27	1.37	1.64	0.92
t_r	Output Rise Time, Q	0.17	0.42	1.14	2.42	0.23	0.58	1.61	3.43
t_f	Output Fall Time, Q	0.24	0.36	0.71	1.17	0.34	0.48	0.90	1.40
t_r	Output Rise Time, QB	0.14	0.38	1.11	2.44	0.20	0.55	1.58	3.44
t_f	Output Fall Time, QB	0.15	0.26	0.62	1.17	0.22	0.36	0.78	1.40
LATNH									
t_{PLH}	Propagation Delay, D to Q	0.56	0.60	0.73	0.43	0.75	0.81	0.99	0.60
t_{PHL}		0.58	0.62	0.76	0.46	0.84	0.90	1.08	0.59
t_{PLH}	Propagation Delay, D to QB	0.83	0.87	1.00	0.42	1.20	1.26	1.43	0.59
t_{PHL}		0.87	0.91	1.03	0.40	1.19	1.24	1.39	0.50
t_{PLH}	Propagation Delay, G to Q	0.68	0.73	0.86	0.43	0.96	1.02	1.20	0.61
t_{PHL}		0.72	0.76	0.90	0.45	1.06	1.12	1.29	0.59
t_{PLH}	Propagation Delay, G to QB	0.97	1.01	1.13	0.42	1.42	1.47	1.65	0.59
t_{PHL}		1.00	1.04	1.16	0.39	1.41	1.46	1.60	0.50
t_r	Output Rise Time, Q	0.19	0.31	0.66	1.19	0.25	0.42	0.92	1.68
t_f	Output Fall Time, Q	0.26	0.32	0.50	0.59	0.37	0.45	0.66	0.73
t_r	Output Rise Time, QB	0.16	0.28	0.64	1.19	0.21	0.38	0.88	1.69
t_f	Output Fall Time, QB	0.21	0.27	0.44	0.56	0.24	0.31	0.52	0.68

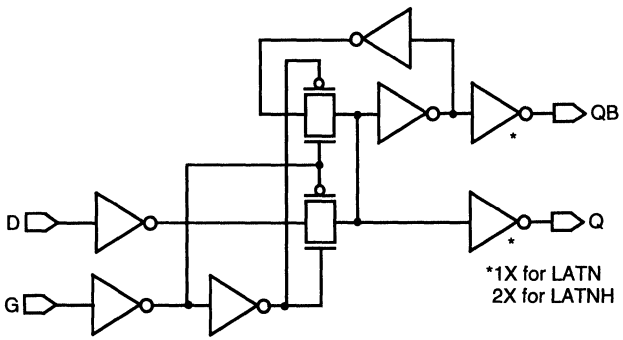
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V Minimum Requirement	3.3V Minimum Requirement
	LATN		
t_{su}	Set Up Time, D to G	0.58	0.86
t_h	Hold Time, G to D	0.09	0.17
t_w	Pulse Width, G(L)	0.01	0.01
t_w	Pulse Width, G(H)	0.63	0.92
	LATNH		
t_{su}	Set Up Time, D to G	0.73	1.08
t_h	Hold Time, G to D	0.06	0.14
t_w	Pulse Width, G(L)	0.01	0.01
t_w	Pulse Width, G(H)	0.76	1.11

FUNCTIONAL DIAGRAM: LATN



7

D-Type Latch, Positive Gate Latched 1x & 2x Drive (3.3V and 5V Core Voltage)

LATP
LATPH

MACRO	EQUIV. GATES
LATP	5
LATPH	6

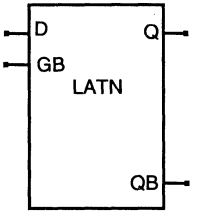
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	Q,QB / D,GB

MACRO	INPUT CAP.
All	D,GB: 0.05pF

FUNCTION TABLE

D	GB	Q	QB
L	L	L	H
H	L	H	L
X	H	Q	QB



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
LATP									
t_{PLH}	Propagation Delay, D to Q	0.53	0.62	0.87	0.83	0.73	0.84	1.19	1.16
t_{PHL}		0.57	0.65	0.89	0.80	0.85	0.95	1.25	0.99
t_{PLH}	Propagation Delay, D to QB	0.72	0.81	1.05	0.83	1.04	1.15	1.50	1.16
t_{PHL}		0.78	0.86	1.09	0.77	1.08	1.17	1.45	0.93
t_{PLH}	Propagation Delay, GB to Q	0.60	0.69	0.94	0.83	0.84	0.95	1.30	1.17
t_{PHL}		0.71	0.79	1.03	0.80	1.05	1.14	1.44	0.99
t_{PLH}	Propagation Delay, GB to QB	0.86	0.94	1.19	0.83	1.24	1.35	1.70	1.16
t_{PHL}		0.84	0.91	1.15	0.77	1.19	1.29	1.56	0.93
t_r	Output Rise Time, Q	0.17	0.41	1.14	2.43	0.24	0.58	1.61	3.43
t_f	Output Fall Time, Q	0.25	0.37	0.72	1.16	0.38	0.52	0.94	1.40
t_r	Output Rise Time, QB	0.14	0.39	1.12	2.44	0.20	0.54	1.58	3.44
t_f	Output Fall Time, QB	0.18	0.30	0.65	1.17	0.23	0.37	0.79	1.40
LATPH									
t_{PLH}	Propagation Delay, D to Q	0.57	0.62	0.75	0.43	0.76	0.82	1.00	0.60
t_{PHL}		0.59	0.63	0.77	0.46	0.86	0.92	1.10	0.59
t_{PLH}	Propagation Delay, D to QB	0.84	0.89	1.01	0.42	1.23	1.29	1.46	0.59
t_{PHL}		0.89	0.93	1.05	0.41	1.22	1.27	1.42	0.50
t_{PLH}	Propagation Delay, GB to Q	0.64	0.68	0.81	0.43	0.88	0.94	1.12	0.61
t_{PHL}		0.71	0.75	0.89	0.45	1.04	1.10	1.28	0.59
t_{PLH}	Propagation Delay, GB to QB	0.97	1.01	1.13	0.42	1.41	1.47	1.64	0.59
t_{PHL}		0.95	0.99	1.11	0.41	1.34	1.39	1.54	0.50
t_r	Output Rise Time, Q	0.19	0.31	0.67	1.20	0.24	0.41	0.91	1.68
t_f	Output Fall Time, Q	0.27	0.33	0.51	0.59	0.39	0.46	0.68	0.72
t_r	Output Rise Time, QB	0.17	0.28	0.64	1.18	0.22	0.39	0.90	1.69
t_f	Output Fall Time, QB	0.20	0.26	0.42	0.56	0.25	0.32	0.52	0.68

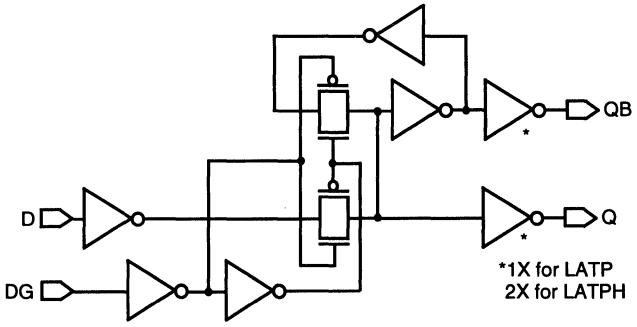
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V Minimum Requirement	3.3V Minimum Requirement
	LATP		
t_{su}	Set Up Time, D to GB	0.50	0.79
t_h	Hold Time, GB to D	-0.07	-0.08
t_w	Pulse Width, GB(L)	0.62	0.97
	LATPH		
t_{su}	Set Up Time, D to GB	0.66	0.99
t_h	Hold Time, GB to D	-0.10	-0.11
t_w	Pulse Width, GB(L)	0.75	1.16

FUNCTIONAL DIAGRAM: LATP



7

D-Type Latch with Reset
Negative Gate Latched 1x & 2x Drive
(3.3V and 5V Core Voltage)

LATRN
LATRNH

MACRO	EQUIV. GATES
LATRN	6
LATRNH	7

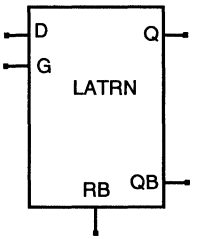
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	Q,QB / RB,D,G

MACRO	INPUT CAP.
All	D,G: 0.05pF RB: 0.07pF

FUNCTION TABLE

D	G	RB	Q	QB
L	H	H	L	H
H	H	H	H	L
X	L	H	Q	QB
X	X	L	L	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
LATRN									
t_{PLH}	Propagation Delay, D to Q	0.74	0.82	1.07	0.84	0.97	1.09	1.45	1.19
t_{PHL}		0.58	0.66	0.90	0.81	0.89	0.99	1.29	1.00
t_{PLH}	Propagation Delay, D to QB	0.71	0.79	1.04	0.83	1.05	1.17	1.52	1.16
t_{PHL}		0.96	1.03	1.26	0.76	1.30	1.40	1.67	0.93
t_{PLH}	Propagation Delay, G to Q	0.78	0.86	1.12	0.85	1.09	1.21	1.57	1.19
t_{PHL}		0.75	0.83	1.07	0.81	1.11	1.21	1.51	1.00
t_{PLH}	Propagation Delay, G to QB	0.88	0.96	1.21	0.83	1.28	1.39	1.74	1.16
t_{PHL}		1.00	1.08	1.31	0.76	1.42	1.51	1.79	0.93
t_{PLH}	Propagation Delay, RB to Q	0.72	0.81	1.06	0.85	0.96	1.08	1.44	1.20
t_{PHL}		0.28	0.36	0.59	0.77	0.47	0.56	0.84	0.93
t_{PLH}	Propagation Delay, RB to QB	0.43	0.51	0.76	0.83	0.65	0.77	1.11	1.16
t_{PHL}		0.94	1.02	1.25	0.76	1.29	1.39	1.66	0.93
t_r	Output Rise Time, Q	0.24	0.48	1.20	2.40	0.31	0.65	1.67	3.40
t_f	Output Fall Time, Q	0.26	0.38	0.73	1.17	0.40	0.54	0.96	1.41
t_r	Output Rise Time, QB	0.14	0.38	1.12	2.44	0.19	0.54	1.58	3.45
t_f	Output Fall Time, QB	0.16	0.27	0.62	1.17	0.21	0.36	0.78	1.41
LATRNH									
t_{PLH}	Propagation Delay, D to Q	0.77	0.82	0.95	0.45	1.02	1.08	1.28	0.64
t_{PHL}		0.60	0.64	0.78	0.47	0.90	0.96	1.14	0.61
t_{PLH}	Propagation Delay, D to QB	0.85	0.89	1.02	0.41	1.24	1.30	1.48	0.59
t_{PHL}		1.10	1.14	1.26	0.40	1.50	1.55	1.70	0.50
t_{PLH}	Propagation Delay, G to Q	0.82	0.86	1.00	0.45	1.13	1.20	1.39	0.64
t_{PHL}		0.75	0.79	0.93	0.47	1.12	1.18	1.36	0.60
t_{PLH}	Propagation Delay, G to QB	1.00	1.04	1.17	0.42	1.47	1.52	1.70	0.59
t_{PHL}		1.16	1.20	1.31	0.40	1.60	1.65	1.80	0.50
t_{PLH}	Propagation Delay, RB to Q	0.76	0.80	0.94	0.46	1.01	1.07	1.26	0.64
t_{PHL}		0.29	0.33	0.45	0.41	0.48	0.53	0.68	0.50
t_{PLH}	Propagation Delay, RB to QB	0.52	0.56	0.68	0.42	0.76	0.81	0.99	0.59
t_{PHL}		1.10	1.14	1.26	0.40	1.49	1.54	1.69	0.50
t_r	Output Rise Time, Q	0.27	0.39	0.74	1.18	0.31	0.48	0.98	1.68
t_f	Output Fall Time, Q	0.28	0.34	0.52	0.60	0.39	0.46	0.68	0.73
t_r	Output Rise Time, QB	0.17	0.29	0.65	1.20	0.22	0.39	0.90	1.70
t_f	Output Fall Time, QB	0.21	0.26	0.43	0.55	0.27	0.34	0.54	0.68

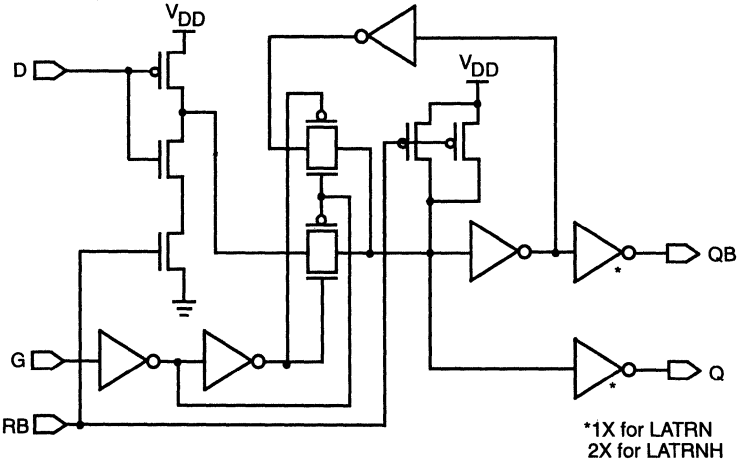
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V Minimum Requirement	3.3V Minimum Requirement
	LATRN		
t_{su}	Set Up Time, D to G	0.83	1.12
t_h	Hold Time, G to D	0.14	0.16
t_{rec}	Recovery Time, RB to G	0.67	0.95
t_w	Pulse Width, G(L)	0.02	0.05
t_w	Pulse Width, G(H)	0.76	1.12
t_w	Pulse Width, RB(L)	0.43	0.68
t_w	Pulse Width, RB(H)	0.05	0.10
	LATRNH		
t_{su}	Set Up Time, D to G	1.01	1.36
t_h	Hold Time, G to D	0.10	0.11
t_{rec}	Recovery Time, RB to G	0.84	1.20
t_w	Pulse Width, G(L)	0.02	0.05
t_w	Pulse Width, G(H)	0.94	1.35
t_w	Pulse Width, RB(L)	0.54	0.83
t_w	Pulse Width, RB(H)	0.05	0.10

FUNCTIONAL DIAGRAM: LATRN



D-Type Latch with Reset Positive Gate Latched 1x & 2x Drive (3.3V and 5V Core Voltage)

LATRP
LATRPH

MACRO	EQUIV. GATES
LATRP	6
LATRPH	7

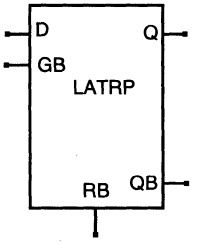
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	Q,QB / RB,D,GB

MACRO	INPUT CAP.
All	D,GB: 0.05pF RB: 0.07pF

FUNCTION TABLE

D	G	RB	Q	QB
L	H	H	L	H
H	H	H	H	L
X	L	H	Q	QB
X	X	L	L	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
LATRP									
t_{PLH}	Propagation Delay, D to Q	0.73	0.82	1.07	0.84	0.97	1.08	1.44	1.19
t_{PHL}		0.57	0.66	0.90	0.81	0.88	0.98	1.28	1.00
t_{PLH}	Propagation Delay, D to QB	0.71	0.79	1.04	0.83	1.05	1.16	1.51	1.16
t_{PHL}		0.95	1.03	1.26	0.76	1.29	1.39	1.67	0.93
t_{PLH}	Propagation Delay, GB to Q	0.73	0.82	1.07	0.85	1.01	1.13	1.49	1.19
t_{PHL}		0.73	0.81	1.06	0.81	1.09	1.19	1.49	1.00
t_{PLH}	Propagation Delay, GB to QB	0.86	0.95	1.20	0.83	1.26	1.37	1.72	1.16
t_{PHL}		0.96	1.03	1.26	0.77	1.34	1.43	1.71	0.93
t_{PLH}	Propagation Delay, RB to Q	0.72	0.80	1.06	0.85	0.95	1.07	1.43	1.19
t_{PHL}		0.28	0.36	0.59	0.77	0.47	0.56	0.84	0.93
t_{PLH}	Propagation Delay, RB to QB	0.43	0.51	0.76	0.83	0.65	0.76	1.11	1.16
t_{PHL}		0.94	1.02	1.24	0.76	1.30	1.39	1.67	0.93
t_r	Output Rise Time, Q	0.24	0.48	1.20	2.41	0.31	0.65	1.67	3.40
t_f	Output Fall Time, Q	0.26	0.38	0.73	1.16	0.39	0.53	0.95	1.40
t_r	Output Rise Time, QB	0.15	0.39	1.13	2.44	0.19	0.54	1.58	3.45
t_f	Output Fall Time, QB	0.15	0.27	0.62	1.17	0.23	0.37	0.79	1.41
LATRPH									
t_{PLH}	Propagation Delay, D to Q	0.77	0.81	0.95	0.45	0.97	1.08	1.44	1.19
t_{PHL}		0.59	0.64	0.78	0.46	0.88	0.98	1.28	1.00
t_{PLH}	Propagation Delay, D to QB	0.85	0.89	1.01	0.41	1.05	1.16	1.51	1.16
t_{PHL}		1.10	1.14	1.26	0.40	1.29	1.39	1.67	0.93
t_{PLH}	Propagation Delay, GB to Q	0.76	0.81	0.95	0.45	1.01	1.13	1.49	1.19
t_{PHL}		0.74	0.78	0.92	0.46	1.09	1.19	1.49	1.00
t_{PLH}	Propagation Delay, GB to QB	0.98	1.02	1.15	0.42	1.26	1.37	1.72	1.16
t_{PHL}		1.09	1.13	1.25	0.40	1.34	1.43	1.71	0.93
t_{PLH}	Propagation Delay, RB to Q	0.75	0.80	0.93	0.46	0.95	1.07	1.43	1.19
t_{PHL}		0.29	0.33	0.45	0.41	0.47	0.56	0.84	0.93
t_{PLH}	Propagation Delay, RB to QB	0.52	0.56	0.68	0.42	0.65	0.76	1.11	1.16
t_{PHL}		1.09	1.13	1.25	0.40	1.30	1.39	1.67	0.93
t_r	Output Rise Time, Q	0.27	0.39	0.74	1.18	0.31	0.65	1.67	3.40
t_f	Output Fall Time, Q	0.28	0.34	0.52	0.59	0.39	0.53	0.95	1.40
t_r	Output Rise Time, QB	0.18	0.30	0.66	1.20	0.19	0.54	1.58	3.45
t_f	Output Fall Time, QB	0.21	0.26	0.43	0.55	0.23	0.37	0.79	1.41

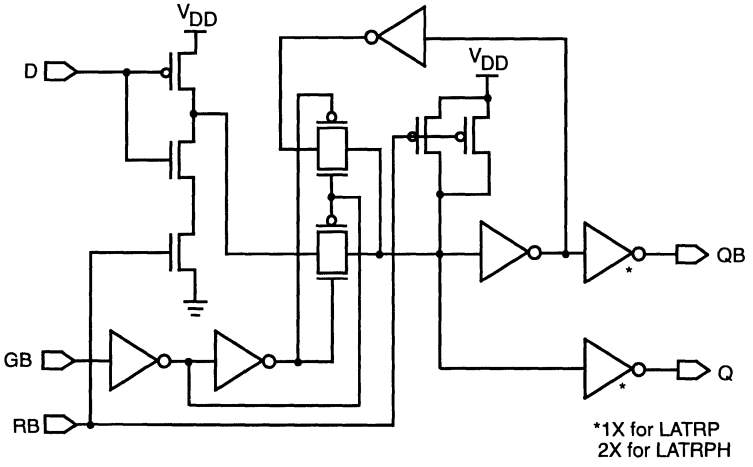
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V Minimum Requirement	3.3V Minimum Requirement
	LATRP		
t_{su}	Set Up Time, D to GB	0.71	0.96
t_h	Hold Time, GB to D	-0.02	-0.08
t_{rec}	Recovery Time, RB to GB	0.08	0.21
t_w	Pulse Width, GB(L)	0.72	1.04
t_w	Pulse Width, GB,RB(H)	0.04	0.03
t_w	Pulse Width, RB(L)	0.59	0.87
	LATRPH		
t_{su}	Set Up Time, D to GB	0.88	1.21
t_h	Hold Time, GB to D	-0.05	-0.13
t_{rec}	Recovery Time, RB to GB	0.19	0.34
t_w	Pulse Width, GB(L)	0.88	1.28
t_w	Pulse Width, GB,RB(H)	0.04	0.04
t_w	Pulse Width, RB(L)	0.75	1.10

FUNCTIONAL DIAGRAM: LATRP



4- Bit D-Type Latch, with 3-State Output 2x Drive (3.3V and 5V Core Voltage)

LAT4TH

MACRO	EQUIV. GATES
LAT4TH	23

Rev. 1.07

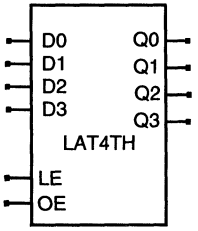
MACRO	OUTPUTS/INPUTS
LAT4TH	Q0-Q3 / D0-D3,LE,OE

MACRO	INPUT CAP.
LAT4TH	D0-D3,LE,OE: 0.05pF

MACRO	OUTPUT CAP.
LAT4TH	Q0-Q3: 0.06pF

FUNCTION TABLE

Dn	LE	OE	Q
L	H	H	L
H	H	H	H
X	L	H	Q
X	X	L	Z



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
LAT4TH									
t_{PLH}	Propagation Delay, D0 to Q0 & D1	0.80	0.84	0.97	0.43	1.18	1.24	1.41	0.59
t_{PHL}	to Q1 & D2 to Q2 & D3 to Q3	0.82	0.93	1.25	1.08	1.14	1.29	1.71	1.43
t_{PLH}	Propagation Delay,	1.34	1.38	1.51	0.43	1.89	1.95	2.12	0.59
t_{PHL}	LE to Q0-Q3	1.13	1.24	1.56	1.08	1.59	1.73	2.16	1.42
t_{PLZ}	Propagation Delay,	0.92	0.92	0.92	0.00	1.10	1.10	1.10	0.00
t_{PZL}	OE to Q0-Q3	0.85	0.97	1.32	1.18	1.17	1.32	1.79	1.55
t_{PZH}	Propagation Delay,	1.19	1.24	1.36	0.43	1.56	1.62	1.80	0.59
t_{PHZ}	OE to Q0-Q3	0.89	0.89	0.89	0.00	1.17	1.17	1.17	0.00
t_r	Output Rise Time, Q0-Q3	0.15	0.26	0.62	1.19	0.15	0.32	0.84	1.71
t_f	Output Fall Time, Q0-Q3	0.41	0.59	1.15	1.87	0.52	0.76	1.48	2.39

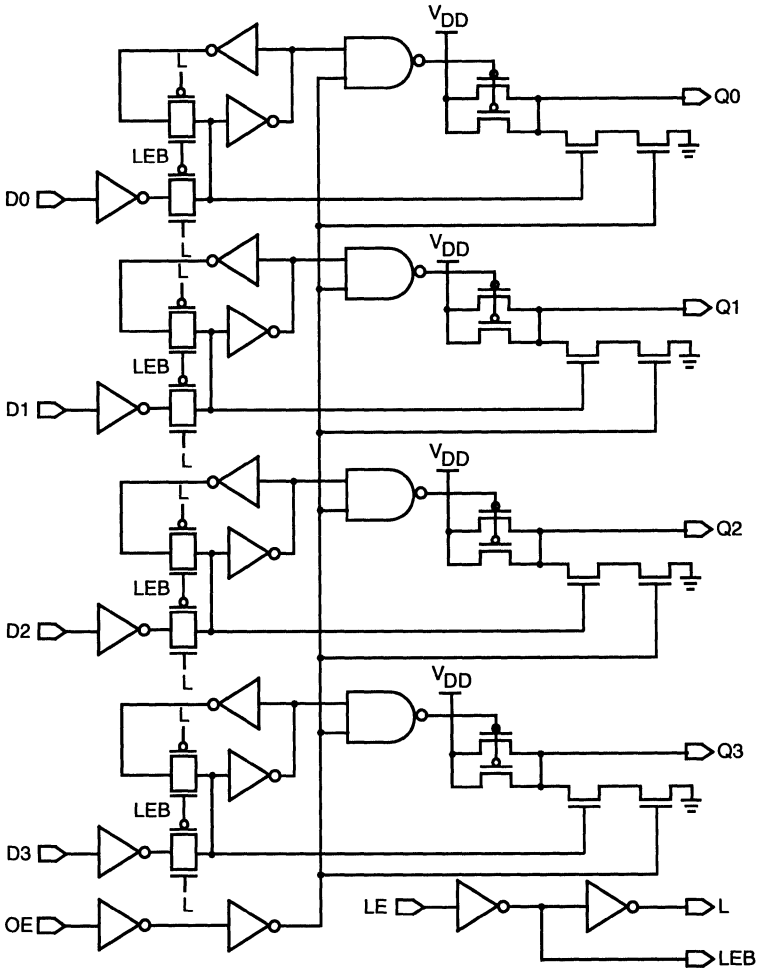
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V	3.3V
		Minimum Requirement	Minimum Requirement
LAT4TH			
t_{su}	Set Up Time, D0-D3 to LE	0.38	0.95
t_h	Hold Time, LE to D0-D3	0.54	1.04
t_w	Pulse Width, LE(L)	0.07	0.10
t_w	Pulse Width, LE(H)	0.86	1.26

FUNCTIONAL DIAGRAM: LAT4TH



7

D-Type Latch with Scan into a D-Type Latch 1x & 2x Drive

LSSD1AH

MACRO	EQUIV. GATES
LSSD1AH	14

Rev. 1.07

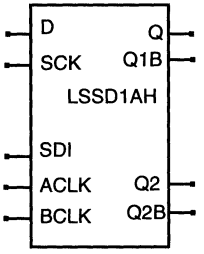
MACRO	OUTPUTS/INPUTS
LSSD1AH	Q1,Q1B,Q2,Q2B / D,SCLK,SDI,ACLK,BCLK

MACRO	INPUT CAP.
LSSD1AH	ACLK,BCLK,D,SCLK,SDI: 0.05pF

FUNCTION TABLE

D	SCLK	SDI	ACLK	Q1	Q1B	MODE
L	H	X	X	L	H	NORMAL
H	H	X	X	H	L	
X	L	L	H	L	H	SCAN
X	L	H	H	H	L	
X	L	X	L	Q1	Q1B	NOR/SCAN

BCK	Q1	Q2	Q2B
L	X	Q2	Q2B
H	L	L	H
H	H	H	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	LSSD1AH								
t_{PLH}	Propagation Delay, ACLK to Q1	1.05	1.10	1.23	0.46	1.36	1.42	1.62	0.66
t_{PHL}		1.25	1.31	1.47	0.54	1.82	1.89	2.11	0.73
t_{PLH}	Propagation Delay, ACLK to Q1B	1.59	1.63	1.75	0.42	2.27	2.33	2.51	0.60
t_{PHL}		1.41	1.46	1.58	0.40	1.88	1.93	2.09	0.51
t_{PLH}	Propagation Delay, ACLK to Q2	1.92	1.96	2.10	0.45	2.57	2.63	2.82	0.64
t_{PHL}		2.18	2.23	2.38	0.50	3.23	3.29	3.48	0.65
t_{PLH}	Propagation Delay, ACLK to Q2B	2.45	2.49	2.62	0.41	3.58	3.64	3.82	0.59
t_{PHL}		2.22	2.26	2.38	0.40	3.02	3.07	3.22	0.50
t_{PLH}	Propagation Delay, BCLK to Q2	0.77	0.81	0.95	0.44	1.07	1.13	1.32	0.62
t_{PHL}		0.79	0.84	0.99	0.49	1.19	1.25	1.44	0.63
t_{PLH}	Propagation Delay, BCLK to Q2B	1.05	1.09	1.22	0.42	1.54	1.60	1.78	0.58
t_{PHL}		1.08	1.12	1.24	0.40	1.51	1.56	1.71	0.50
t_{PLH}	Propagation Delay, D to Q1	0.53	0.57	0.70	0.43	0.71	0.77	0.95	0.61
t_{PHL}		0.66	0.71	0.84	0.46	0.99	1.05	1.22	0.59
t_{PLH}	Propagation Delay, D to Q1B	0.98	1.02	1.14	0.41	1.43	1.49	1.66	0.59
t_{PHL}		0.83	0.87	1.00	0.41	1.13	1.18	1.33	0.50
t_{PLH}	Propagation Delay, D to Q2	1.35	1.39	1.53	0.46	1.86	1.92	2.11	0.64
t_{PHL}		1.55	1.60	1.75	0.49	2.30	2.37	2.56	0.65
t_{PLH}	Propagation Delay, D to Q2B	1.82	1.87	1.99	0.42	2.72	2.77	2.95	0.59
t_{PHL}		1.64	1.68	1.80	0.40	2.25	2.30	2.45	0.50
t_{PLH}	Propagation Delay, SCLK to Q1	0.81	0.86	0.99	0.43	1.03	1.09	1.27	0.61
t_{PHL}		0.89	0.94	1.08	0.46	1.24	1.30	1.48	0.59
t_{PLH}	Propagation Delay, SCLK to Q1B	1.19	1.23	1.35	0.42	1.63	1.68	1.86	0.59
t_{PHL}		1.13	1.17	1.30	0.41	1.50	1.55	1.70	0.50
t_{PLH}	Propagation Delay, SCLK to Q2	1.75	1.80	1.94	0.46	2.33	2.39	2.59	0.65
t_{PHL}		1.94	2.00	2.15	0.52	2.80	2.87	3.07	0.69
t_{PLH}	Propagation Delay, SCLK to Q2B	2.22	2.26	2.39	0.42	3.18	3.24	3.41	0.59
t_{PHL}		2.07	2.11	2.23	0.40	2.79	2.84	2.99	0.50
t_{PLH}	Propagation Delay, SDI to Q1	0.80	0.85	0.99	0.46	1.06	1.13	1.33	0.67
t_{PHL}		1.02	1.08	1.24	0.55	1.58	1.65	1.87	0.73

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay, SDI to Q1B	1.40	1.44	1.56	0.42	2.11	2.17	2.34	0.59
t_{PHL}		1.13	1.17	1.30	0.41	1.53	1.58	1.74	0.51
t_{PLH}	Propagation Delay, SDI to Q2	1.66	1.71	1.84	0.46	2.28	2.34	2.53	0.64
t_{PHL}		1.97	2.02	2.17	0.49	2.99	3.05	3.25	0.65
t_{PLH}	Propagation Delay, SDI to Q2B	2.27	2.31	2.44	0.42	3.40	3.46	3.64	0.59
t_{PHL}		1.93	1.97	2.09	0.41	2.67	2.72	2.87	0.50
t_r	Output Rise Time, Q1	0.31	0.43	0.79	1.19	0.37	0.54	1.04	1.67
t_f	Output Fall Time, Q1	0.50	0.56	0.74	0.60	0.64	0.72	0.95	0.77
t_r	Output Rise Time, Q1B	0.20	0.32	0.68	1.19	0.26	0.43	0.94	1.68
t_f	Output Fall Time, Q1B	0.25	0.31	0.48	0.57	0.28	0.35	0.55	0.68
t_r	Output Rise Time, Q2	0.25	0.37	0.73	1.19	0.33	0.50	1.01	1.68
t_f	Output Fall Time, Q2	0.40	0.46	0.64	0.60	0.52	0.60	0.82	0.76
t_r	Output Rise Time, Q2B	0.18	0.30	0.66	1.20	0.22	0.39	0.90	1.68
t_f	Output Fall Time, Q2B	0.19	0.24	0.41	0.57	0.26	0.33	0.54	0.69

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

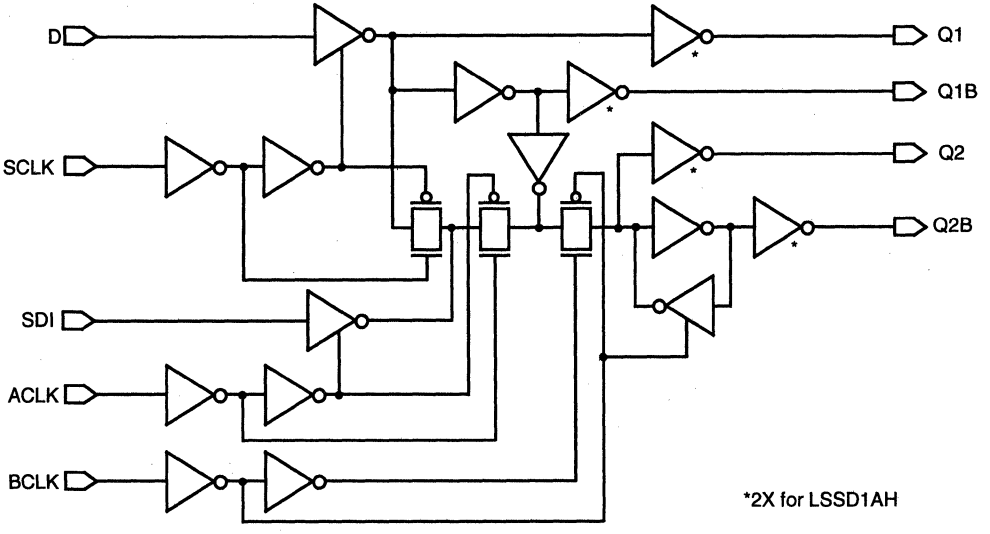
CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V	3.3V
		Minimum Requirement	Minimum Requirement
	LSSD1AH		
t_{su}	Set Up Time, SDI to ACLK	1.27	2.01
t_{su}	Set Up Time, ACLK to BCLK	2.26	3.33
t_{su}	Set Up Time, D to BCLK	1.57	2.36
t_{su}	Set Up Time, SCLK to BCLK	2.03	2.92
t_{su}	Set Up Time, SDI to BCLK	2.01	3.06
t_{su}	Set Up Time, D to SCLK	1.02	1.58
t_h	Hold Time, ACLK to SDI	-0.25	-0.34
t_h	Hold Time, BCLK to ACLK	-1.33	-1.71
t_h	Hold Time, BCLK to D	-0.07	0.01
t_h	Hold Time, BCLK to SCLK	-1.18	-1.44
t_h	Hold Time, BCLK to SDI	-0.32	-0.34
t_h	Hold Time, SCLK to D	0.00	0.01
t_w	Pulse Width, ACLK(H)	2.77	2.77
t_w	Pulse Width, BCLK(H)	1.50	1.50
t_w	Pulse Width, SCLK(H)	2.38	2.38

7

FUNCTIONAL DIAGRAM: LSSD1A



*2X for LSSD1AH

7

4-Bit Magnitude Comparator (3.3 V and 5 V Core Voltage)

MCOMP4

MACRO	EQUIV. GATES
MCOMP4	35

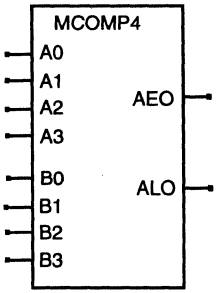
Rev. 1.07

MACRO	OUTPUTS/INPUTS
MCOMP4	AEO,ALO / A0-A3,B0-B3

MACRO	INPUT CAP.
MCOMP4	A0-A3: 0.16pF B0-B3: 0.10pF

FUNCTION TABLE

A0 B0	A1 B1	A2 B2	A3 B3	AEO	ALO
X	X	X	A3<B3	L	H
X	X	X	A2>B2	L	L
X	X	A2<B2	A3=B3	L	H
X	X	A2>B2	A3=B3	L	L
X	A1<B1	A2=B2	A3=B3	L	H
X	A1>B1	A2=B2	A3=B3	L	L
A0<B0	A1=B1	A2=B2	A3=B3	L	H
A1>B1	A1=B1	A2=B2	A3=B3	L	L
A1=B1	A1=B1	A2=B2	A3=B3	H	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	MCOMP4								
t_{PLH}	Propagation Delay, A0 to AEO	0.91	0.96	1.09	0.46	1.32	1.39	1.58	0.64
t_{PHL}		0.78	0.83	0.95	0.41	1.12	1.17	1.32	0.51
t_{PLH}	Propagation Delay, A0 to ALO	0.83	0.87	1.01	0.45	1.17	1.23	1.42	0.64
t_{PHL}		0.59	0.67	0.90	0.78	0.85	0.96	1.28	1.06
t_{PLH}	Propagation Delay, A1 to AEO	0.97	1.01	1.15	0.45	1.39	1.46	1.65	0.64
t_{PHL}		0.81	0.85	0.98	0.41	1.15	1.20	1.35	0.50
t_{PLH}	Propagation Delay, A1 to ALO	0.93	0.98	1.12	0.46	1.34	1.41	1.60	0.65
t_{PHL}		0.84	0.92	1.15	0.77	1.18	1.28	1.60	1.05
t_{PLH}	Propagation Delay, A2 to AEO	1.10	1.15	1.28	0.45	1.58	1.65	1.84	0.64
t_{PHL}		0.87	0.91	1.03	0.40	1.22	1.27	1.41	0.49
t_{PLH}	Propagation Delay, A2 to ALO	0.78	0.82	0.95	0.43	1.11	1.17	1.35	0.60
t_{PHL}		0.92	1.00	1.23	0.77	1.35	1.46	1.78	1.07
t_{PLH}	Propagation Delay, A3 to AEO	1.11	1.15	1.28	0.45	1.58	1.64	1.83	0.64
t_{PHL}		0.83	0.87	0.99	0.40	1.16	1.21	1.36	0.48
t_{PLH}	Propagation Delay, A3 to ALO	0.72	0.76	0.89	0.42	1.03	1.09	1.27	0.59
t_{PHL}		0.86	0.93	1.17	0.78	1.28	1.39	1.71	1.07
t_{PLH}	Propagation Delay, B0 to AEO	0.86	0.90	1.04	0.45	1.21	1.27	1.46	0.64
t_{PHL}		0.69	0.73	0.86	0.41	1.00	1.05	1.20	0.51
t_{PLH}	Propagation Delay, B0 to ALO	1.00	1.05	1.19	0.45	1.42	1.49	1.68	0.64
t_{PHL}		0.72	0.80	1.03	0.78	1.02	1.13	1.44	1.05
t_{PLH}	Propagation Delay, B1 to AEO	0.92	0.97	1.11	0.45	1.32	1.38	1.58	0.64
t_{PHL}		0.73	0.77	0.89	0.41	1.03	1.08	1.23	0.50
t_{PLH}	Propagation Delay, B1 to ALO	1.04	1.09	1.22	0.43	1.50	1.56	1.74	0.61
t_{PHL}		0.78	0.86	1.09	0.78	1.09	1.20	1.52	1.06
t_{PLH}	Propagation Delay, B2 to AEO	1.01	1.06	1.19	0.45	1.45	1.51	1.71	0.65
t_{PHL}		0.76	0.81	0.93	0.40	1.07	1.12	1.26	0.49
t_{PLH}	Propagation Delay, B2 to ALO	0.96	1.00	1.13	0.42	1.37	1.43	1.61	0.60
t_{PHL}		1.03	1.11	1.34	0.78	1.52	1.62	1.95	1.07
t_{PLH}	Propagation Delay, B3 to AEO	1.02	1.06	1.20	0.46	1.46	1.53	1.72	0.65
t_{PHL}		0.74	0.78	0.90	0.40	1.03	1.08	1.23	0.49

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

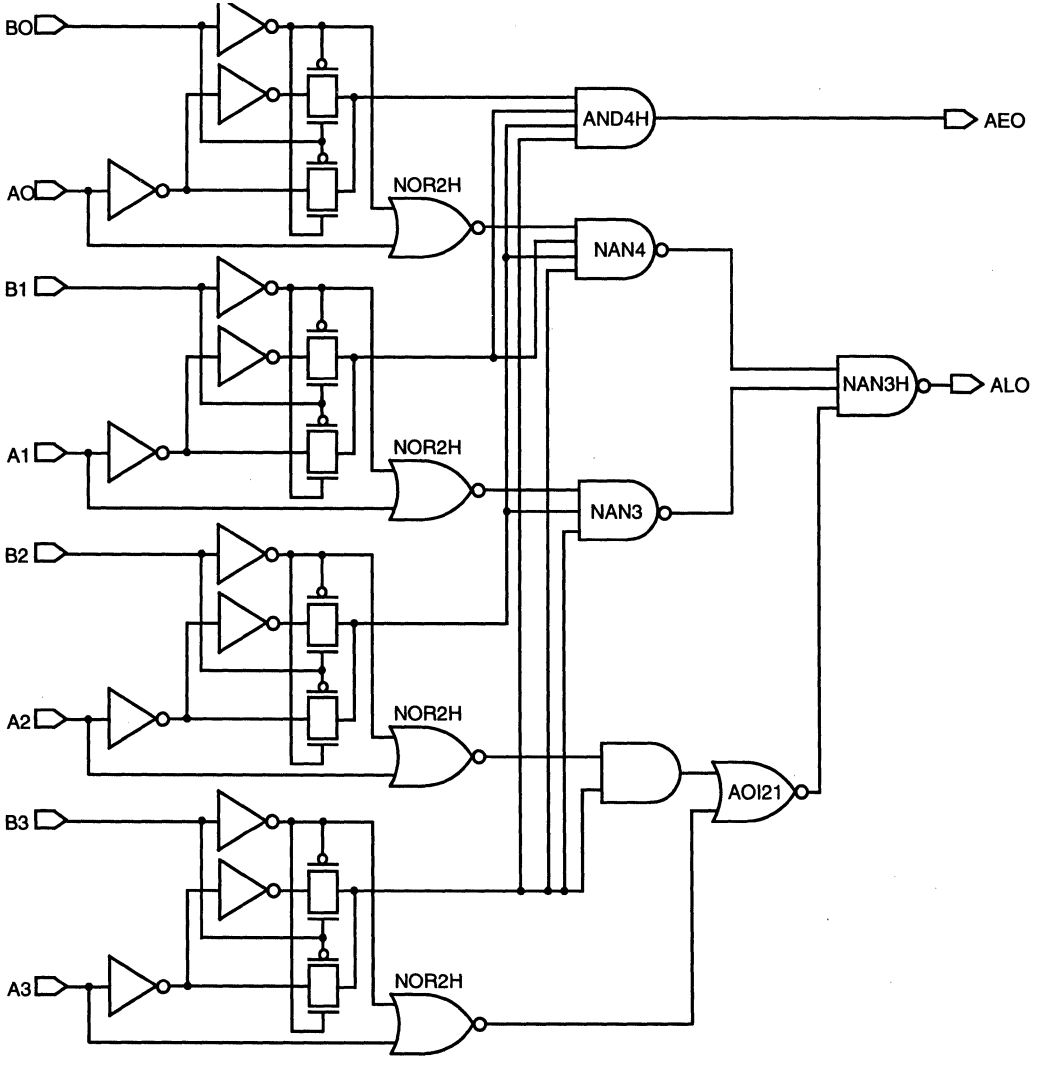
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay, B3 to ALO	1.06	1.11	1.24	0.43	1.54	1.61	1.79	0.61
t_{PHL}		1.03	1.11	1.34	0.77	1.47	1.58	1.90	1.06
t_r	Output Rise Time, AEO	0.28	0.40	0.75	1.18	0.35	0.51	1.02	1.68
t_f	Output Fall Time, AEO	0.25	0.31	0.48	0.57	0.30	0.37	0.58	0.69
t_r	Output Rise Time, ALO	0.39	0.51	0.87	1.19	0.50	0.67	1.18	1.69
t_f	Output Fall Time, ALO	0.37	0.51	0.93	1.39	0.45	0.63	1.17	1.82

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: MCOMP4



2-1 Multiplexer, 1X Drive (3.3 V and 5 V Core Voltage)

MUX2A

MACRO	EQUIV. GATES
MUX2A	3

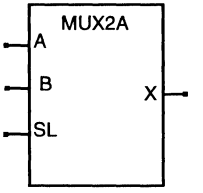
Rev. 1.07

MACRO	OUTPUTS/INPUTS
MUX2A	X / A,SL,B

MACRO	INPUT CAP.
MUX2A	A,B: 0.05pF SL: 0.11pF

FUNCTION TABLE

A	B	SL	X
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H



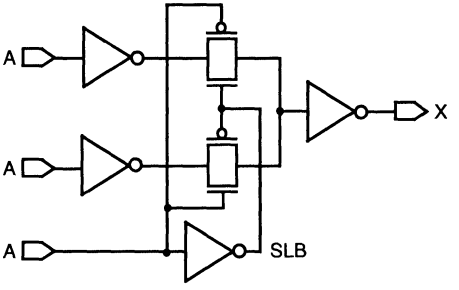
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	MUX2A								
t_{PLH}	Propagation Delay, A,B to X	0.45	0.54	0.78	0.83	0.61	0.73	1.08	1.16
t_{PHL}		0.48	0.56	0.79	0.78	0.71	0.81	1.09	0.95
t_{PLH}	Propagation Delay, SL to X	0.36	0.44	0.69	0.83	0.49	0.60	0.95	1.16
t_{PHL}		0.42	0.49	0.73	0.77	0.62	0.71	0.99	0.95
t_r	Output Rise Time, X	0.15	0.40	1.13	2.43	0.21	0.56	1.59	3.44
t_f	Output Fall Time, X	0.22	0.34	0.69	1.17	0.30	0.44	0.86	1.41

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: MUX2A



7

2- Input Multiplexer, 2X Drive (3.3 V and 5 V Core Voltage)

MUX2H

MACRO	EQUIV. GATES
MUX2H	3

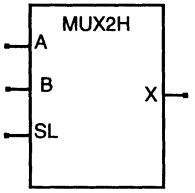
Rev. 1.07

MACRO	OUTPUTS/INPUTS
MUX2H	X / A,SL,B

MACRO	INPUT CAP.
MUX2H	A,B: 0.12pF SL: 0.10pF

FUNCTION TABLE

A	B	SL	X
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H



CMOS SWITCHING CHARACTERISTICS

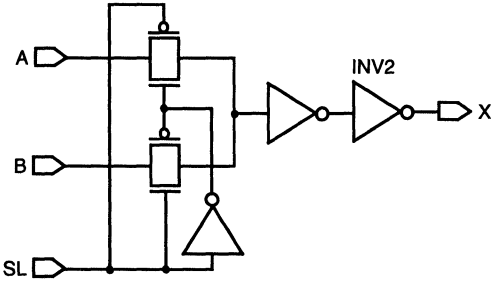
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	MUX2H								
t_{PLH}	Propagation Delay, A,B to X	0.38	0.42	0.55	0.41	0.52	0.58	0.76	0.59
t_{PHL}		0.37	0.41	0.53	0.39	0.53	0.58	0.72	0.47
t_{PLH}	Propagation Delay, SL to X	0.49	0.53	0.65	0.41	0.69	0.75	0.93	0.58
t_{PHL}		0.56	0.59	0.71	0.39	0.79	0.84	0.98	0.48
t_r	Output Rise Time, X	0.11	0.23	0.59	1.21	0.16	0.33	0.84	1.72
t_f	Output Fall Time, X	0.14	0.20	0.37	0.57	0.19	0.26	0.47	0.69

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: MUX2H



2- Input Multiplexer, Inverting Output, 2X Drive (3.3 V and 5 V Core Voltage)

MUX2IH

MACRO	EQUIV. GATES
MUX2IH	3

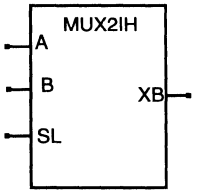
Rev. 1.07

MACRO	OUTPUTS/INPUTS
MUX2IH	XB / A,B,SL

MACRO	INPUT CAP.
MUX2IH	A,B: 0.16pF SL: 0.11pF

FUNCTION TABLE

A	B	SL	XB
L	X	L	H
H	X	L	L
X	L	H	H
X	H	H	L



CMOS SWITCHING CHARACTERISTICS

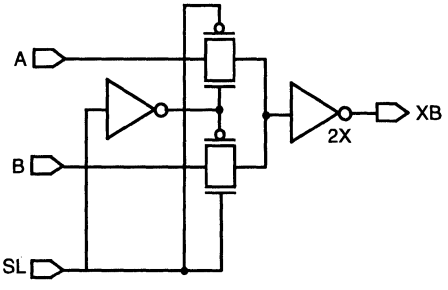
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	MUX2IH								
t_{PLH}	Propagation Delay, A,B to X	0.17	0.21	0.34	0.42	0.25	0.30	0.48	0.59
t_{PHL}		0.25	0.29	0.41	0.41	0.39	0.44	0.58	0.48
t_{PLH}	Propagation Delay, SL to X	0.32	0.36	0.49	0.41	0.51	0.57	0.74	0.58
t_{PHL}		0.38	0.42	0.54	0.40	0.53	0.57	0.72	0.48
t_r	Output Rise Time, X	0.17	0.29	0.65	1.21	0.19	0.36	0.87	1.70
t_f	Output Fall Time, X	0.21	0.27	0.44	0.58	0.26	0.33	0.54	0.69

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: MUX2IH



7

4-1 Multiplexer, 2X Drive (3.3 V and 5 V Core Voltage)

MUX4H

MACRO	EQUIV. GATES
MUX4H	7

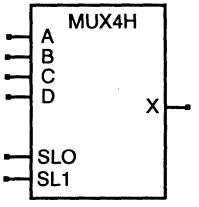
Rev. 1.07

MACRO	OUTPUTS/INPUTS
MUX4H	X / A-D,SL0,SL1

MACRO	INPUT CAP.
MUX4H	A-D,SL1: 0.12pF SL0: 0.16pF

FUNCTION TABLE

A	B	C	D	SL1	SL0	X
L	X	X	X	L	L	L
H	X	X	X	L	L	H
X	L	X	X	L	H	L
X	H	X	X	L	H	H
X	X	L	X	H	L	L
X	X	H	X	H	L	H
X	X	X	L	H	H	L
X	X	X	H	H	H	H



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

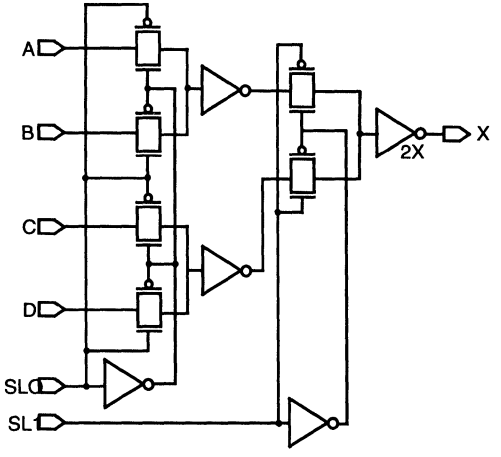
Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	MUX4H								
t_{PLH}	Propagation Delay, A-D to X	0.57	0.62	0.74	0.43	0.82	0.87	1.05	0.59
t_{PHL}		0.57	0.62	0.75	0.44	0.85	0.91	1.08	0.56
t_{PLH}	Propagation Delay, SL0 to X	0.70	0.74	0.87	0.43	0.99	1.05	1.23	0.60
t_{PHL}		0.80	0.84	0.97	0.44	1.18	1.23	1.40	0.56
t_{PLH}	Propagation Delay, SL1 to X	0.40	0.45	0.57	0.43	0.54	0.60	0.78	0.60
t_{PHL}		0.45	0.49	0.62	0.44	0.69	0.74	0.91	0.55
t_r	Output Rise Time, X	0.19	0.31	0.67	1.20	0.22	0.39	0.89	1.69
t_f	Output Fall Time, X	0.24	0.30	0.48	0.59	0.34	0.41	0.62	0.71

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: MUX4H



4-BIT, 2-Input Multiplexer, 1X & 2X Drive (3.3 V and 5 V Core Voltage)

MUX41A MUX41AH

MACRO	EQUIV. GATES
MUX41A	12
MUX41AH	14

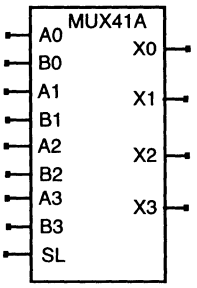
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X0-X3 / A0,B0,A1,B1,A2,B2,A3,B3,SL

MACRO	INPUT CAP.
All	A0-A3,B0-B3: 0.12pF SL: 0.05pF

FUNCTION TABLE

An	Bn	SL	Xn
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H



CMOS SWITCHING CHARACTERISTICS

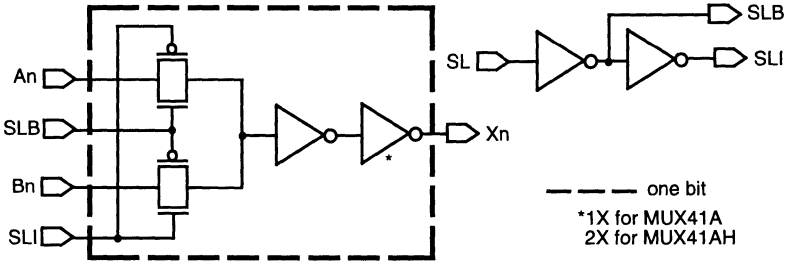
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	MUX41A								
t_{PLH}	Propagation Delay, A0,B0 to X0 & A1,	0.33	0.41	0.66	0.82	0.48	0.59	0.94	1.16
t_{PHL}	B1 to X1 & A2,B2 to X2 & A3,B3 to X3	0.32	0.39	0.62	0.75	0.46	0.55	0.82	0.90
t_{PLH}	Propagation Delay,	0.96	1.05	1.30	0.83	1.31	1.42	1.77	1.16
t_{PHL}	SL to X0	0.79	0.87	1.10	0.76	1.38	1.47	1.74	0.91
t_{PLH}	Propagation Delay,	0.91	1.00	1.25	0.83	1.30	1.41	1.76	1.16
t_{PHL}	SL to X1-X3	0.95	1.02	1.21	0.63	1.37	1.45	1.69	0.78
t_r	Output Rise Time, X0-X3	0.15	0.39	1.12	2.45	0.18	0.53	1.56	3.45
t_f	Output Fall Time, X0-X3	0.12	0.24	0.60	1.19	0.17	0.32	0.74	1.42
	MUX41AH								
t_{PLH}	Propagation Delay,	0.38	0.42	0.55	0.41	0.53	0.58	0.76	0.58
t_{PHL}	A0 to X0	0.37	0.41	0.53	0.39	0.53	0.58	0.72	0.47
t_{PLH}	Propagation Delay, A1,B1 to X1 & A2,	0.38	0.38	0.38	0.00	0.53	0.53	0.53	0.01
t_{PHL}	B2 to X2 & A3,B3 to X3 & B0 to X0	0.37	0.37	0.37	0.00	0.53	0.53	0.53	0.00
t_{PLH}	Propagation Delay,	0.93	0.93	0.93	0.00	1.31	1.31	1.31	0.01
t_{PHL}	SL to X0-X3	1.00	1.00	1.00	0.00	1.39	1.39	1.39	0.00
t_r	Output Rise Time, X0	0.11	0.24	0.60	1.21	0.16	0.33	0.84	1.70
t_f	Output Fall Time, X0	0.15	0.21	0.38	0.56	0.20	0.26	0.47	0.68
t_r	Output Rise Time, X1-X3	0.11	0.12	0.12	0.01	0.16	0.16	0.17	0.02
t_f	Output Fall Time, X1-X3	0.15	0.15	0.15	0.01	0.20	0.20	0.20	0.01

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: MUX41A



8-Input Multiplexer, 2X Drive (3.3 V and 5 V Core Voltage)

MUX8AH

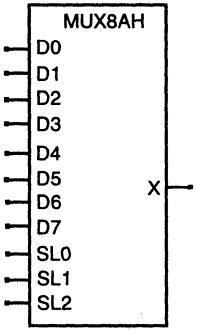
MACRO	EQUIV. GATES
MUX8AH	18

Rev. 1.07

MACRO	OUTPUTS/INPUTS
MUX8AH	X / D0-D7,SL0-SL2

MACRO	INPUT CAP.
MUX8AH	D0-D7,SL1: 0.12pF SL0,SL2: 0.05pF

SL2	SL1	SL0	X
L	L	L	D0
L	L	H	D1
L	H	L	D2
L	H	H	D3
H	L	L	D4
H	L	H	D5
H	H	L	D6
H	H	H	D7



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

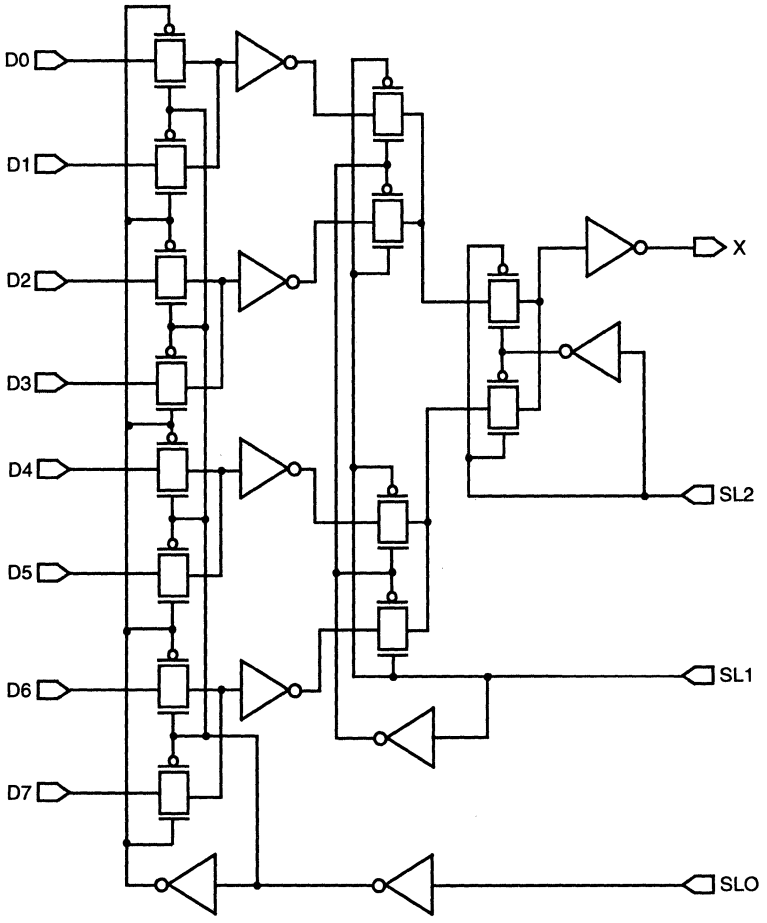
Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	MUX8AH								
t_{PLH}	Propagation Delay, D0-D3 to X	0.81	0.86	0.99	0.44	1.13	1.19	1.38	0.63
t_{PHL}		0.80	0.85	1.00	0.50	1.24	1.31	1.51	0.68
t_{PLH}	Propagation Delay, D4-D7 to X	0.78	0.82	0.95	0.43	1.08	1.15	1.33	0.62
t_{PHL}		0.76	0.81	0.96	0.50	1.18	1.25	1.45	0.66
t_{PLH}	Propagation Delay, SL0 to X	1.12	1.17	1.30	0.44	1.55	1.61	1.80	0.63
t_{PHL}		1.24	1.29	1.44	0.50	1.85	1.92	2.12	0.68
t_{PLH}	Propagation Delay, SL1 to X	0.83	0.87	1.01	0.44	1.16	1.22	1.41	0.63
t_{PHL}		0.85	0.90	1.05	0.51	1.32	1.39	1.59	0.68
t_{PLH}	Propagation Delay, SL2 to X	0.68	0.73	0.86	0.44	0.95	1.01	1.19	0.62
t_{PHL}		0.74	0.79	0.93	0.49	1.11	1.18	1.37	0.65
t_r	Output Rise Time, X	0.24	0.36	0.72	1.19	0.30	0.56	1.36	2.65
t_f	Output Fall Time, X	0.37	0.43	0.61	0.62	0.71	0.81	1.11	1.01

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: MUX8AH



4-Input Multiplexer with Individual Selects 1X & 2X Drive (3.3 V and 5 V Core Voltage)

MX41
MX41H

MACRO	EQUIV. GATES
MX41	5
MX41H	6

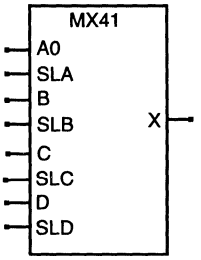
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A,SLA,B,SLB,C,SLC,D,SLD

MACRO	INPUT CAP.
All	A-D,SLA-SLD: 0.05pF

FUNCTION TABLE

A*SLA	B*SLB	C*SLC	D*SLD	X
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H
L	L	L	L	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	MX41								
t_{PLH}	Propagation Delay, A to X	0.50	0.58	0.83	0.83	0.68	0.79	1.14	1.17
t_{PHL}		0.58	0.70	1.04	1.15	0.85	1.00	1.46	1.52
t_{PLH}	Propagation Delay, B to X	0.40	0.48	0.73	0.83	0.55	0.66	1.01	1.16
t_{PHL}		0.43	0.54	0.88	1.14	0.61	0.76	1.21	1.51
t_{PLH}	Propagation Delay, C to X	0.53	0.61	0.86	0.83	0.72	0.84	1.19	1.16
t_{PHL}		0.54	0.66	1.00	1.14	0.81	0.96	1.41	1.51
t_{PLH}	Propagation Delay, D to X	0.42	0.50	0.75	0.83	0.58	0.70	1.04	1.16
t_{PHL}		0.40	0.51	0.85	1.14	0.57	0.72	1.17	1.51
t_{PLH}	Propagation Delay, SLA to X	0.52	0.60	0.85	0.83	0.70	0.81	1.16	1.16
t_{PHL}		0.49	0.60	0.95	1.15	0.73	0.88	1.34	1.52
t_{PLH}	Propagation Delay, SLB to X	0.39	0.47	0.72	0.83	0.54	0.65	1.00	1.16
t_{PHL}		0.52	0.63	0.97	1.14	0.73	0.88	1.33	1.51
t_{PLH}	Propagation Delay, SLC to X	0.55	0.63	0.88	0.83	0.74	0.86	1.21	1.16
t_{PHL}		0.45	0.57	0.91	1.15	0.69	0.84	1.29	1.51
t_{PLH}	Propagation Delay, SLD to X	0.40	0.48	0.73	0.83	0.57	0.69	1.03	1.16
t_{PHL}		0.49	0.60	0.94	1.14	0.69	0.84	1.29	1.51
t_r	Output Rise Time, X	0.26	0.51	1.24	2.44	0.34	0.68	1.71	3.44
t_f	Output Fall Time, X	0.26	0.46	1.05	1.98	0.33	0.58	1.34	2.52
	MX41H								
t_{PLH}	Propagation Delay, A to X	0.44	0.48	0.61	0.43	0.60	0.65	0.83	0.59
t_{PHL}		0.47	0.53	0.71	0.59	0.67	0.75	0.98	0.78
t_{PLH}	Propagation Delay, B to X	0.54	0.58	0.71	0.43	0.72	0.78	0.96	0.60
t_{PHL}		0.52	0.58	0.76	0.60	0.77	0.85	1.08	0.79
t_{PLH}	Propagation Delay, C to X	0.49	0.53	0.66	0.42	0.67	0.73	0.91	0.59
t_{PHL}		0.49	0.55	0.72	0.58	0.70	0.78	1.01	0.77
t_{PLH}	Propagation Delay, D to X	0.59	0.63	0.76	0.42	0.79	0.85	1.03	0.59
t_{PHL}		0.52	0.58	0.75	0.57	0.76	0.84	1.07	0.78
t_{PLH}	Propagation Delay, SLA to X	0.44	0.48	0.61	0.42	0.62	0.68	0.86	0.59
t_{PHL}		0.58	0.63	0.81	0.59	0.84	0.91	1.15	0.79
t_{PLH}	Propagation Delay, SLB to X	0.54	0.59	0.71	0.42	0.74	0.80	0.97	0.60
t_{PHL}		0.62	0.69	0.87	0.61	0.93	1.01	1.25	0.80

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

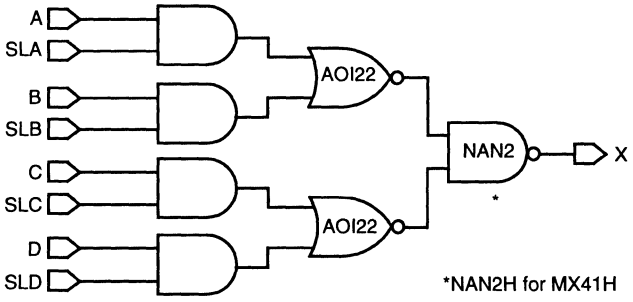
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay,	0.50	0.55	0.67	0.41	0.69	0.75	0.93	0.59
t_{PHL}	SLC to X	0.59	0.65	0.82	0.58	0.84	0.92	1.15	0.78
t_{PLH}	Propagation Delay,	0.59	0.63	0.76	0.42	0.81	0.86	1.04	0.59
t_{PHL}	SLD to X	0.62	0.68	0.85	0.58	0.92	0.99	1.23	0.78
t_r	Output Rise Time, X	0.29	0.41	0.77	1.19	0.37	0.54	1.05	1.68
t_f	Output Fall Time, X	0.29	0.39	0.67	0.95	0.37	0.50	0.87	1.23

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: MX41



*NAN2H for MX41H

7

6-Input Multiplexer with Individual Selects 1X & 2X Drive (3.3 V and 5 V Core Voltage)

MX61
MX61H

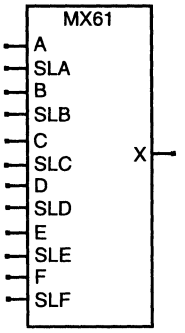
MACRO	EQUIV. GATES
MX61	8
MX61H	9

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X/A,SLA,B,SLB,C,SLC,D, SLD,E,SLE,F,SLF

MACRO	INPUT CAP.
All	A-F,SLA-SLF: 0.05pF

A*SLA	B*SLB	C*SLC	D*SLD	E*SLE	F*SLF	X
H	X	X	X	X	X	H
X	H	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
X	X	X	X	X	H	H
L	L	L	L	L	L	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	MX61								
t_{PLH}	Propagation Delay, A to X	0.51	0.59	0.84	0.83	0.70	0.82	1.17	1.16
t_{PHL}		0.62	0.78	1.24	1.55	0.90	1.12	1.75	2.12
t_{PLH}	Propagation Delay, B to X	0.41	0.49	0.74	0.83	0.57	0.69	1.03	1.16
t_{PHL}		0.47	0.62	1.08	1.54	0.66	0.87	1.50	2.11
t_{PLH}	Propagation Delay, C to X	0.55	0.63	0.88	0.83	0.76	0.87	1.22	1.16
t_{PHL}		0.61	0.77	1.23	1.55	0.90	1.11	1.75	2.11
t_{PLH}	Propagation Delay, D to X	0.44	0.52	0.77	0.83	0.61	0.73	1.08	1.16
t_{PHL}		0.47	0.62	1.08	1.54	0.67	0.88	1.51	2.11
t_{PLH}	Propagation Delay, E to X	0.59	0.67	0.92	0.83	0.82	0.93	1.28	1.17
t_{PHL}		0.63	0.78	1.24	1.55	0.93	1.14	1.77	2.11
t_{PLH}	Propagation Delay, F to X	0.48	0.56	0.81	0.83	0.68	0.79	1.14	1.17
t_{PHL}		0.49	0.64	1.10	1.54	0.71	0.92	1.55	2.11
t_{PLH}	Propagation Delay, SLA to X	0.52	0.61	0.86	0.83	0.72	0.83	1.18	1.16
t_{PHL}		0.54	0.69	1.16	1.54	0.78	0.99	1.62	2.12
t_{PLH}	Propagation Delay, SLB to X	0.40	0.49	0.74	0.83	0.56	0.67	1.02	1.16
t_{PHL}		0.55	0.71	1.17	1.54	0.77	0.99	1.62	2.11
t_{PLH}	Propagation Delay, SLC to X	0.57	0.65	0.90	0.83	0.77	0.89	1.24	1.16
t_{PHL}		0.53	0.68	1.15	1.55	0.78	1.00	1.63	2.11
t_{PLH}	Propagation Delay, SLD to X	0.40	0.49	0.74	0.83	0.60	0.72	1.07	1.16
t_{PHL}		0.55	0.71	1.17	1.54	0.78	0.99	1.62	2.11
t_{PLH}	Propagation Delay, SLE to X	0.61	0.69	0.94	0.83	0.83	0.95	1.30	1.17
t_{PHL}		0.54	0.70	1.16	1.55	0.82	1.03	1.67	2.11
t_{PLH}	Propagation Delay, SLF to X	0.48	0.56	0.81	0.83	0.67	0.78	1.13	1.16
t_{PHL}		0.57	0.72	1.18	1.54	0.81	1.02	1.65	2.11
t_r	Output Rise Time, X	0.40	0.64	1.37	2.44	0.51	0.85	1.89	3.44
t_f	Output Fall Time, X	0.34	0.62	1.46	2.80	0.42	0.78	1.88	3.66

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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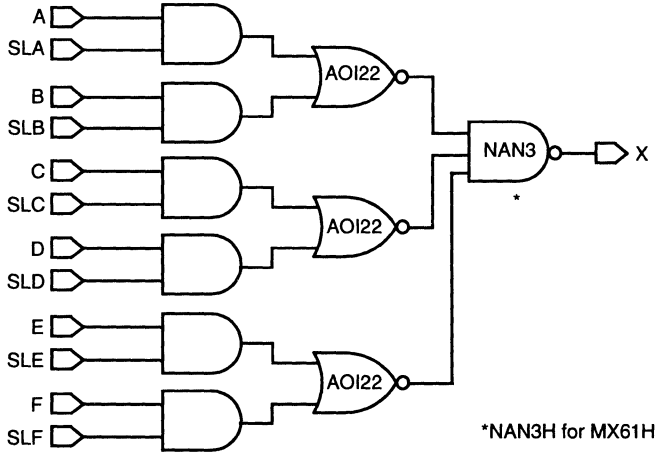
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	MX61H								
t_{PLH}	Propagation Delay, A to X	0.46	0.50	0.63	0.43	0.62	0.68	0.86	0.60
t_{PHL}		0.53	0.61	0.84	0.78	0.75	0.86	1.17	1.06
t_{PLH}	Propagation Delay, B to X	0.55	0.59	0.72	0.43	0.74	0.80	0.98	0.60
t_{PHL}		0.56	0.64	0.88	0.79	0.83	0.94	1.26	1.08
t_{PLH}	Propagation Delay, C to X	0.52	0.56	0.68	0.42	0.71	0.77	0.95	0.59
t_{PHL}		0.56	0.64	0.87	0.78	0.80	0.90	1.22	1.07
t_{PLH}	Propagation Delay, D to X	0.61	0.65	0.78	0.43	0.83	0.89	1.07	0.60
t_{PHL}		0.60	0.67	0.91	0.77	0.87	0.98	1.30	1.07
t_{PLH}	Propagation Delay, E to X	0.55	0.59	0.72	0.43	0.75	0.81	0.99	0.60
t_{PHL}		0.56	0.64	0.88	0.79	0.81	0.91	1.23	1.07
t_{PLH}	Propagation Delay, F to X	0.64	0.68	0.81	0.43	0.87	0.93	1.11	0.60
t_{PHL}		0.59	0.67	0.90	0.77	0.87	0.98	1.30	1.07
t_{PLH}	Propagation Delay, SLA to X	0.46	0.50	0.63	0.42	0.63	0.69	0.87	0.60
t_{PHL}		0.65	0.72	0.96	0.78	0.90	1.00	1.33	1.08
t_{PLH}	Propagation Delay, SLB to X	0.55	0.60	0.72	0.42	0.76	0.82	1.00	0.59
t_{PHL}		0.69	0.77	1.00	0.78	0.98	1.09	1.42	1.09
t_{PLH}	Propagation Delay, SLC to X	0.52	0.57	0.69	0.42	0.73	0.79	0.96	0.59
t_{PHL}		0.67	0.75	0.98	0.77	0.95	1.06	1.38	1.07
t_{PLH}	Propagation Delay, SLD to X	0.61	0.65	0.78	0.42	0.84	0.90	1.08	0.59
t_{PHL}		0.70	0.78	1.02	0.78	1.02	1.13	1.45	1.08
t_{PLH}	Propagation Delay, SLE to X	0.55	0.59	0.72	0.42	0.76	0.82	1.00	0.60
t_{PHL}		0.67	0.74	0.98	0.77	0.95	1.06	1.38	1.07
t_{PLH}	Propagation Delay, SLF to X	0.64	0.68	0.81	0.42	0.88	0.94	1.12	0.60
t_{PHL}		0.70	0.77	1.01	0.77	1.02	1.13	1.45	1.07
t_r	Output Rise Time, X	0.41	0.53	0.89	1.19	0.52	0.69	1.19	1.68
t_f	Output Fall Time, X	0.38	0.51	0.92	1.37	0.45	0.63	1.18	1.81

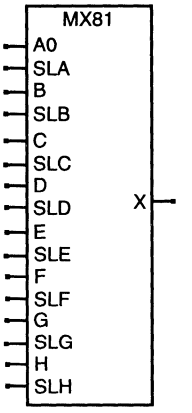
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: MX61



8-Input Multiplexer with Individual Selects 1X & 2X Drive (3.3 V and 5 V Core Voltage)

MX81
MX81H



MACRO	EQUIV. GATES
MX81	10
MX81H	12

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A,SLA,B,SLB,C,SLC, D,SLD,E,SLE,F,SLF,G,SLG, H,SLH

MACRO	INPUT CAP.
All	A-H,SLA-SLH: 0.05pF

FUNCTION TABLE

A*SLA	B*SLB	C*SLC	D*SLD	E*SLE	F*SLF	G*SLG	H*SLH	X
H	X	X	X	X	X	X	X	H
X	H	X	X	X	X	X	X	H
X	X	H	X	X	X	X	X	H
X	X	X	H	X	X	X	X	H
X	X	X	X	H	X	X	X	H
X	X	X	X	X	H	X	X	H
X	X	X	X	X	X	H	X	H
X	X	X	X	X	X	X	H	H
L	L	L	L	L	L	L	L	L

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	MX81								
t_{PLH}	Propagation Delay, A to X	0.52	0.60	0.85	0.83	0.71	0.83	1.18	1.16
t_{PHL}		0.65	0.85	1.43	1.96	0.94	1.21	2.03	2.72
t_{PLH}	Propagation Delay, B to X	0.42	0.50	0.75	0.83	0.58	0.70	1.05	1.16
t_{PHL}		0.49	0.69	1.27	1.95	0.69	0.96	1.77	2.71
t_{PLH}	Propagation Delay, C to X	0.56	0.65	0.89	0.83	0.78	0.90	1.25	1.16
t_{PHL}		0.68	0.87	1.46	1.95	0.99	1.26	2.08	2.72
t_{PLH}	Propagation Delay, D to X	0.47	0.55	0.80	0.83	0.66	0.77	1.12	1.16
t_{PHL}		0.53	0.73	1.32	1.96	0.77	1.04	1.85	2.72
t_{PLH}	Propagation Delay, E,G to X	0.60	0.68	0.93	0.83	0.83	0.95	1.30	1.17
t_{PHL}		0.70	0.90	1.49	1.96	1.05	1.32	2.13	2.72
t_{PLH}	Propagation Delay, F to X	0.50	0.58	0.83	0.83	0.71	0.83	1.18	1.17
t_{PHL}		0.57	0.77	1.36	1.96	0.83	1.10	1.92	2.72
t_{PLH}	Propagation Delay, H to X	0.50	0.58	0.83	0.83	0.70	0.82	1.17	1.18
t_{PHL}		0.57	0.77	1.36	1.96	0.80	1.07	1.89	2.71
t_{PLH}	Propagation Delay, SLA to X	0.53	0.62	0.87	0.83	0.71	0.83	1.18	1.17
t_{PHL}		0.56	0.76	1.34	1.95	0.83	1.10	1.92	2.72
t_{PLH}	Propagation Delay, SLB to X	0.41	0.50	0.74	0.83	0.57	0.69	1.04	1.16
t_{PHL}		0.58	0.78	1.36	1.95	0.81	1.08	1.90	2.71
t_{PLH}	Propagation Delay, SLC to X	0.58	0.66	0.91	0.83	0.80	0.91	1.26	1.16
t_{PHL}		0.59	0.79	1.37	1.96	0.87	1.14	1.96	2.72
t_{PLH}	Propagation Delay, SLD to X	0.46	0.54	0.79	0.83	0.65	0.76	1.11	1.16
t_{PHL}		0.62	0.82	1.40	1.95	0.87	1.15	1.96	2.72
t_{PLH}	Propagation Delay, SLE to X	0.61	0.70	0.95	0.83	0.84	0.96	1.31	1.17
t_{PHL}		0.62	0.82	1.40	1.95	0.93	1.20	2.02	2.72
t_{PLH}	Propagation Delay, SLF to X	0.50	0.58	0.83	0.83	0.71	0.83	1.18	1.16
t_{PHL}		0.65	0.85	1.44	1.96	0.94	1.21	2.03	2.72
t_{PLH}	Propagation Delay, SLG to X	0.61	0.70	0.95	0.83	0.86	0.98	1.33	1.18
t_{PHL}		0.62	0.82	1.40	1.95	0.92	1.19	2.01	2.72

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

CMOS SWITCHING CHARACTERISTICS

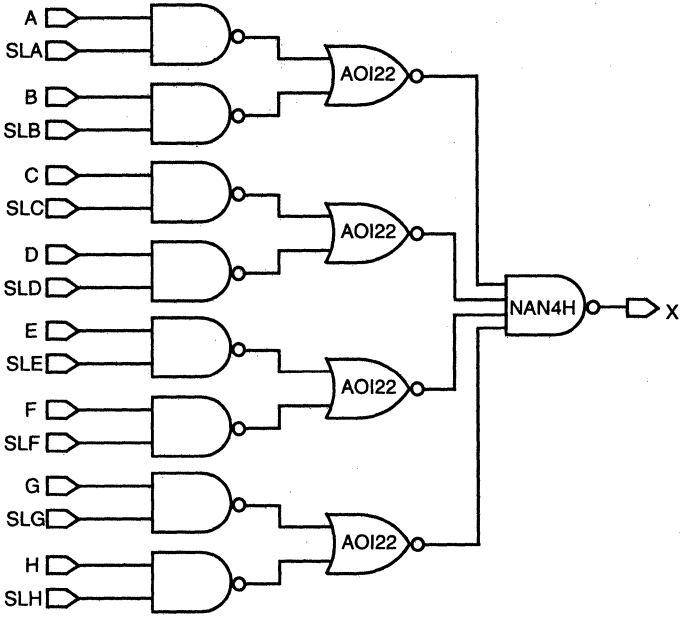
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay,	0.50	0.58	0.83	0.83	0.69	0.81	1.16	1.18
t_{PHL}	SLH to X	0.65	0.85	1.44	1.96	0.91	1.19	2.00	2.72
t_r	Output Rise Time, X	0.50	0.75	1.48	2.44	0.63	0.97	2.00	3.44
t_f	Output Fall Time, X	0.44	0.81	1.89	3.63	0.56	1.04	2.47	4.78
	MX81H								
t_{PLH}	Propagation Delay,	0.52	0.56	0.69	0.42	0.72	0.77	0.95	0.59
t_{PHL}	A to X	0.60	0.70	0.99	0.98	0.86	0.99	1.40	1.37
t_{PLH}	Propagation Delay,	0.61	0.65	0.78	0.43	0.83	0.89	1.07	0.59
t_{PHL}	B to X	0.65	0.75	1.04	0.98	0.93	1.07	1.48	1.37
t_{PLH}	Propagation Delay,	0.49	0.54	0.66	0.43	0.67	0.73	0.91	0.60
t_{PHL}	C to X	0.59	0.69	0.99	0.98	0.83	0.97	1.38	1.37
t_{PLH}	Propagation Delay,	0.58	0.62	0.75	0.43	0.79	0.85	1.03	0.60
t_{PHL}	D to X	0.64	0.74	1.03	0.98	0.92	1.06	1.47	1.38
t_{PLH}	Propagation Delay,	0.57	0.62	0.74	0.43	0.79	0.85	1.03	0.60
t_{PHL}	E to X	0.66	0.76	1.06	0.98	0.92	1.06	1.47	1.38
t_{PLH}	Propagation Delay,	0.67	0.71	0.84	0.43	0.92	0.97	1.15	0.60
t_{PHL}	F,H to X	0.69	0.79	1.08	0.99	1.02	1.15	1.57	1.37
t_{PLH}	Propagation Delay,	0.58	0.62	0.75	0.43	0.79	0.85	1.03	0.61
t_{PHL}	G to X	0.64	0.74	1.03	0.98	0.94	1.08	1.49	1.37
t_{PLH}	Propagation Delay,	0.53	0.57	0.69	0.41	0.73	0.79	0.97	0.59
t_{PHL}	SLA to X	0.72	0.82	1.11	0.98	1.01	1.15	1.56	1.37
t_{PLH}	Propagation Delay,	0.62	0.66	0.78	0.42	0.85	0.91	1.08	0.59
t_{PHL}	SLB to X	0.76	0.86	1.15	0.98	1.09	1.23	1.64	1.37
t_{PLH}	Propagation Delay,	0.50	0.54	0.67	0.42	0.69	0.75	0.93	0.59
t_{PHL}	SLC to X	0.72	0.81	1.11	0.98	1.00	1.14	1.55	1.37
t_{PLH}	Propagation Delay,	0.59	0.63	0.75	0.42	0.81	0.87	1.04	0.59
t_{PHL}	SLD,SLE,SLG to X	0.76	0.86	1.15	0.99	1.09	1.23	1.64	1.38
t_{PLH}	Propagation Delay,	0.66	0.71	0.83	0.43	0.92	0.98	1.16	0.60
t_{PHL}	SLF,SLH to X	0.80	0.90	1.19	0.98	1.17	1.31	1.72	1.37
t_r	Output Rise Time, X	0.55	0.67	1.03	1.19	0.68	0.84	1.35	1.69
t_f	Output Fall Time, X	0.50	0.68	1.22	1.79	0.63	0.87	1.58	2.37

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: MX81H



7

2-Input NAND Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

NAN2
NAN2H
NAN2B

MACRO	EQUIV. GATES
NAN2	1
NAN2H,NAN2B	2

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A,B

MACRO	INPUT CAP.
NAN2	A,B: 0.05pF
NAN2H	A,B: 0.09pF
NAN2B	A,B: 0.07pF

FUNCTION TABLE

A	B	X
L	L	H
L	H	H
H	L	H
H	H	L

CMOS SWITCHING CHARACTERISTICS

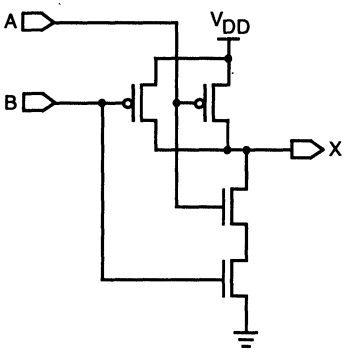
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
NAN2									
t_{PLH}	Propagation Delay, A to X	0.12	0.21	0.45	0.82	0.17	0.29	0.63	1.15
t_{PHL}		0.27	0.38	0.72	1.14	0.34	0.49	0.94	1.50
t_{PLH}	Propagation Delay, B to X	0.17	0.25	0.49	0.82	0.22	0.34	0.68	1.15
t_{PHL}		0.24	0.36	0.70	1.13	0.31	0.46	0.91	1.50
t_r	Output Rise Time, X	0.23	0.47	1.20	2.42	0.29	0.63	1.66	3.44
t_f	Output Fall Time, X	0.20	0.40	0.99	1.96	0.22	0.47	1.23	2.54
NAN2H									
t_{PLH}	Propagation Delay, A to X	0.10	0.14	0.27	0.41	0.14	0.20	0.38	0.58
t_{PHL}		0.25	0.31	0.48	0.57	0.31	0.38	0.61	0.75
t_{PLH}	Propagation Delay, B to X	0.16	0.20	0.32	0.41	0.21	0.27	0.45	0.58
t_{PHL}		0.24	0.30	0.46	0.56	0.30	0.37	0.60	0.75
t_r	Output Rise Time, X	0.25	0.37	0.73	1.18	0.29	0.46	0.97	1.70
t_f	Output Fall Time, X	0.22	0.32	0.60	0.94	0.22	0.34	0.71	1.23
NAN2B									
t_{PLH}	Propagation Delay, A to X	0.05	0.09	0.22	0.42	0.11	0.17	0.35	0.58
t_{PHL}		0.34	0.46	0.80	1.13	0.40	0.55	1.00	1.50
t_{PLH}	Propagation Delay, B to X	0.08	0.12	0.24	0.41	0.15	0.21	0.38	0.58
t_{PHL}		0.31	0.42	0.76	1.13	0.37	0.52	0.97	1.50
t_r	Output Rise Time, X	0.23	0.35	0.70	1.17	0.23	0.40	0.90	1.69
t_f	Output Fall Time, X	0.23	0.43	1.01	1.96	0.23	0.49	1.25	2.54

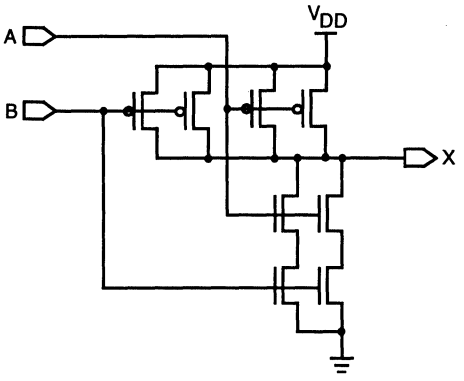
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

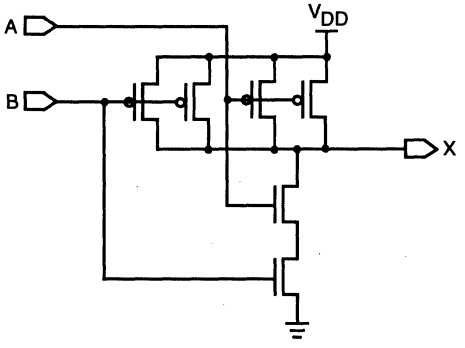
FUNCTIONAL DIAGRAM: NAN2



FUNCTIONAL DIAGRAM: NAN2H



FUNCTIONAL DIAGRAM: NAN2B



7

3-Input NAND Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

NAN3
NAN3H

MACRO	EQUIV. GATES
NAN3	2
NAN3H	3

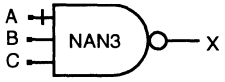
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-C

MACRO	INPUT CAP.
NAN3	A-C: 0.05pF
NAN3H	A-C: 0.09pF

FUNCTION TABLE

A	B	C	X
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L



CMOS SWITCHING CHARACTERISTICS

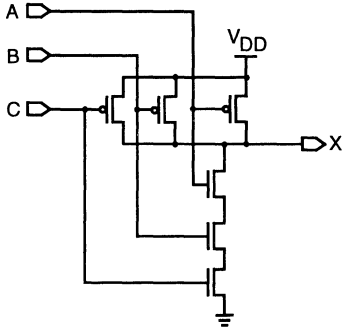
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

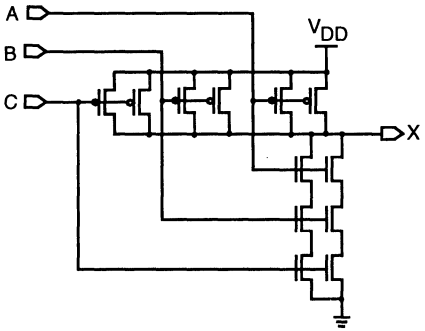
Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
NAN3									
t_{PLH}	Propagation Delay, A to X	0.13	0.21	0.46	0.82	0.19	0.30	0.65	1.15
t_{PHL}		0.33	0.48	0.94	1.53	0.39	0.60	1.24	2.10
t_{PLH}	Propagation Delay, B to X	0.17	0.25	0.50	0.82	0.24	0.36	0.70	1.15
t_{PHL}		0.32	0.48	0.94	1.54	0.41	0.62	1.25	2.10
t_{PLH}	Propagation Delay, C to X	0.21	0.29	0.54	0.83	0.30	0.41	0.76	1.16
t_{PHL}		0.32	0.47	0.93	1.54	0.42	0.63	1.26	2.10
t_r	Output Rise Time, X	0.37	0.61	1.34	2.42	0.46	0.81	1.84	3.44
t_f	Output Fall Time, X	0.28	0.56	1.39	2.78	0.32	0.69	1.79	3.67
NAN3H									
t_{PLH}	Propagation Delay, A to X	0.10	0.14	0.26	0.41	0.16	0.22	0.39	0.58
t_{PHL}		0.31	0.38	0.61	0.76	0.36	0.46	0.78	1.05
t_{PLH}	Propagation Delay, B to X	0.15	0.20	0.32	0.41	0.23	0.28	0.46	0.58
t_{PHL}		0.30	0.38	0.61	0.77	0.39	0.49	0.81	1.05
t_{PLH}	Propagation Delay, C to X	0.19	0.24	0.36	0.41	0.27	0.33	0.51	0.59
t_{PHL}		0.29	0.37	0.60	0.77	0.39	0.50	0.81	1.05
t_r	Output Rise Time, X	0.37	0.49	0.84	1.19	0.45	0.62	1.13	1.70
t_f	Output Fall Time, X	0.30	0.43	0.84	1.37	0.32	0.50	1.05	1.83

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: NAN3



FUNCTIONAL DIAGRAM: NAN3H



7

4-Input NAND Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

NAN4
NAN4H

MACRO	EQUIV. GATES
NAN4	2
NAN4H	4

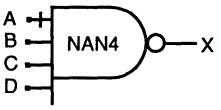
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-D

MACRO	INPUT CAP.
NAN4	A-D: 0.05pF
NAN4H	A-D: 0.09pF

FUNCTION TABLE

A	B	C	D	X
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L



CMOS SWITCHING CHARACTERISTICS

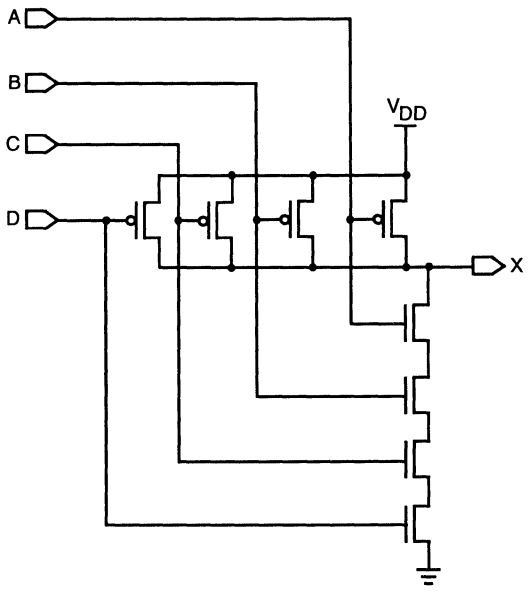
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

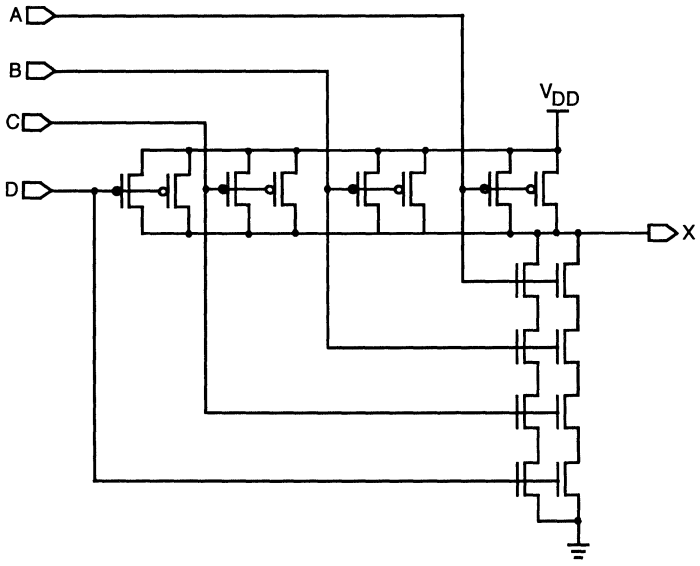
Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
NAN4									
t_{PLH}	Propagation Delay, A to X	0.13	0.21	0.46	0.82	0.19	0.31	0.66	1.15
t_{PHL}		0.36	0.56	1.14	1.94	0.42	0.69	1.51	2.71
t_{PLH}	Propagation Delay, B to X	0.17	0.25	0.49	0.82	0.25	0.37	0.71	1.15
t_{PHL}		0.38	0.57	1.16	1.95	0.47	0.74	1.56	2.71
t_{PLH}	Propagation Delay, C to X	0.21	0.29	0.54	0.83	0.31	0.42	0.77	1.16
t_{PHL}		0.40	0.59	1.18	1.95	0.53	0.80	1.61	2.71
t_{PLH}	Propagation Delay, D to X	0.23	0.31	0.56	0.84	0.34	0.45	0.81	1.17
t_{PHL}		0.37	0.57	1.15	1.95	0.53	0.80	1.61	2.71
t_r	Output Rise Time, X	0.45	0.70	1.42	2.42	0.58	0.92	1.95	3.44
t_f	Output Fall Time, X	0.40	0.76	1.84	3.62	0.47	0.95	2.39	4.79
NAN4H									
t_{PLH}	Propagation Delay, A to X	0.10	0.14	0.27	0.41	0.17	0.23	0.40	0.58
t_{PHL}		0.35	0.44	0.73	0.96	0.40	0.53	0.94	1.35
t_{PLH}	Propagation Delay, B to X	0.16	0.20	0.32	0.41	0.24	0.30	0.47	0.58
t_{PHL}		0.38	0.48	0.77	0.97	0.47	0.60	1.01	1.36
t_{PLH}	Propagation Delay, C to X	0.19	0.23	0.36	0.42	0.29	0.35	0.52	0.59
t_{PHL}		0.39	0.49	0.78	0.98	0.51	0.65	1.05	1.36
t_{PLH}	Propagation Delay, D to X	0.22	0.26	0.39	0.43	0.32	0.38	0.56	0.60
t_{PHL}		0.37	0.47	0.76	0.98	0.52	0.66	1.07	1.36
t_r	Output Rise Time, X	0.49	0.61	0.97	1.18	0.58	0.75	1.27	1.70
t_f	Output Fall Time, X	0.41	0.59	1.13	1.80	0.46	0.70	1.42	2.38

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: NAN4



FUNCTIONAL DIAGRAM: NAN4H



5-Input NAND Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

NAN5
NAN5H

MACRO	EQUIV. GATES
NAN5	4
NAN5H	5

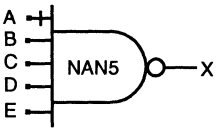
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-E

MACRO	INPUT CAP.
All	A-E: 0.05pF

FUNCTION TABLE

A	B	C	D	E	X
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

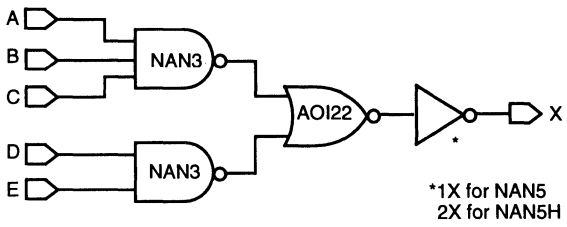
Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
NAN5									
t_{PLH}	Propagation Delay, A to X	0.34	0.42	0.67	0.82	0.55	0.67	1.01	1.16
t_{PHL}		0.78	0.86	1.09	0.77	1.05	1.15	1.43	0.94
t_{PLH}	Propagation Delay, B to X	0.43	0.51	0.76	0.83	0.63	0.75	1.10	1.16
t_{PHL}		0.79	0.87	1.10	0.77	1.09	1.18	1.46	0.94
t_{PLH}	Propagation Delay, C to X	0.49	0.58	0.82	0.83	0.71	0.83	1.17	1.16
t_{PHL}		0.77	0.85	1.08	0.77	1.10	1.19	1.47	0.94
t_{PLH}	Propagation Delay, D to X	0.36	0.45	0.69	0.82	0.55	0.67	1.02	1.16
t_{PHL}		0.69	0.77	1.00	0.76	0.98	1.07	1.35	0.94
t_{PLH}	Propagation Delay, E to X	0.46	0.54	0.79	0.83	0.63	0.75	1.10	1.16
t_{PHL}		0.68	0.76	0.99	0.77	0.98	1.07	1.35	0.94
t_r	Output Rise Time, X	0.15	0.40	1.13	2.44	0.17	0.52	1.55	3.45
t_f	Output Fall Time, X	0.21	0.32	0.67	1.16	0.27	0.41	0.83	1.39
NAN5H									
t_{PLH}	Propagation Delay, A to X	0.39	0.43	0.55	0.41	0.60	0.66	0.84	0.58
t_{PHL}		0.87	0.92	1.04	0.42	1.20	1.25	1.41	0.53
t_{PLH}	Propagation Delay, B to X	0.48	0.52	0.64	0.41	0.69	0.75	0.92	0.58
t_{PHL}		0.90	0.94	1.07	0.42	1.22	1.28	1.43	0.53
t_{PLH}	Propagation Delay, C to X	0.53	0.58	0.70	0.42	0.77	0.83	1.00	0.58
t_{PHL}		0.87	0.91	1.04	0.42	1.24	1.29	1.45	0.52
t_{PLH}	Propagation Delay, D to X	0.43	0.47	0.59	0.41	0.61	0.67	0.84	0.58
t_{PHL}		0.78	0.82	0.95	0.42	1.12	1.17	1.33	0.52
t_{PLH}	Propagation Delay, E to X	0.51	0.55	0.67	0.41	0.70	0.76	0.93	0.58
t_{PHL}		0.78	0.82	0.95	0.42	1.11	1.16	1.32	0.53
t_r	Output Rise Time, X	0.17	0.29	0.65	1.21	0.21	0.38	0.89	1.71
t_f	Output Fall Time, X	0.28	0.33	0.50	0.56	0.35	0.42	0.62	0.69

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: NAN5



7

6-Input NAND Gate 2X Drive with Complementary 1X Drive (3.3 V and 5 V Core Voltage)

NAN6CH

MACRO	EQUIV. GATES
NAN6CH	6

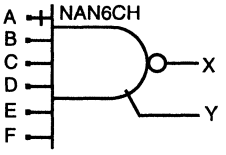
Rev. 1.07

MACRO	OUTPUTS/INPUTS
NAN6CH	X,Y / A-F

MACRO	INPUT CAP.
NAN6CH	A-F: 0.05pF

FUNCTION TABLE

A	B	C	D	E	F	X	Y
L	X	X	X	X	X	H	L
X	L	X	X	X	X	H	L
X	X	L	X	X	X	H	L
X	X	X	L	X	X	H	L
X	X	X	X	L	X	H	L
X	X	X	X	X	L	H	L
H	H	H	H	H	H	L	H



CMOS SWITCHING CHARACTERISTICS

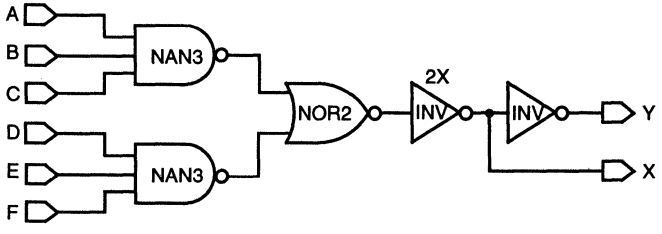
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		NAN6CH							
t_{PLH}	Propagation Delay, A to X	0.40	0.44	0.56	0.41	0.62	0.67	0.85	0.58
t_{PHL}		0.89	0.93	1.06	0.42	1.22	1.27	1.42	0.52
t_{PLH}	Propagation Delay, B to X	0.49	0.53	0.65	0.41	0.70	0.76	0.93	0.58
t_{PHL}		0.91	0.96	1.08	0.41	1.24	1.29	1.45	0.52
t_{PLH}	Propagation Delay, C to X	0.55	0.59	0.71	0.42	0.78	0.84	1.01	0.58
t_{PHL}		0.89	0.93	1.05	0.41	1.25	1.30	1.46	0.52
t_{PLH}	Propagation Delay, D to X	0.44	0.48	0.60	0.41	0.65	0.71	0.88	0.58
t_{PHL}		0.90	0.94	1.07	0.42	1.25	1.30	1.46	0.52
t_{PLH}	Propagation Delay, E to X	0.52	0.56	0.69	0.41	0.74	0.80	0.97	0.58
t_{PHL}		0.91	0.95	1.07	0.42	1.27	1.33	1.48	0.52
t_{PLH}	Propagation Delay, F to X	0.58	0.62	0.75	0.41	0.83	0.89	1.06	0.58
t_{PHL}		0.89	0.94	1.06	0.41	1.29	1.34	1.50	0.52
t_{PLH}	Propagation Delay, X to Y	0.09	0.17	0.42	0.82	0.12	0.24	0.58	1.16
t_{PHL}		0.12	0.20	0.43	0.76	0.19	0.28	0.56	0.91
t_r	Output Rise Time, X	0.21	0.33	0.69	1.21	0.26	0.43	0.94	1.71
t_f	Output Fall Time, X	0.29	0.35	0.52	0.56	0.35	0.42	0.63	0.69
t_r	Output Rise Time, Y	0.15	0.39	1.12	2.43	0.19	0.54	1.57	3.44
t_f	Output Fall Time, Y	0.11	0.23	0.58	1.18	0.16	0.30	0.73	1.42

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: NAN6CH



8-Input NAND Gate, 2X Drive (3.3 V and 5 V Core Voltage)

NAN8H

MACRO	EQUIV. GATES
NAN8H	7

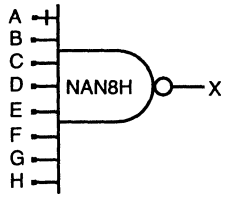
Rev. 1.07

MACRO	OUTPUTS/INPUTS
NAN8H	X / A-H

MACRO	INPUT CAP.
NAN8H	A-H: 0.05pF

FUNCTION TABLE

A	B	C	D	E	F	G	H	X
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L



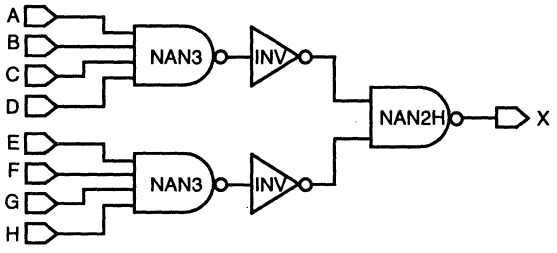
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	NAN8H								
t_{PLH}	Propagation Delay,	0.41	0.45	0.57	0.41	0.63	0.68	0.86	0.58
t_{PHL}	A to X	0.83	0.88	1.06	0.57	1.10	1.18	1.40	0.76
t_{PLH}	Propagation Delay,	0.49	0.53	0.65	0.41	0.71	0.77	0.94	0.58
t_{PHL}	B to X	0.86	0.92	1.09	0.57	1.15	1.22	1.45	0.76
t_{PLH}	Propagation Delay,	0.55	0.59	0.72	0.42	0.80	0.86	1.03	0.58
t_{PHL}	C to X	0.88	0.94	1.11	0.57	1.20	1.28	1.51	0.76
t_{PLH}	Propagation Delay,	0.58	0.62	0.75	0.42	0.84	0.90	1.08	0.58
t_{PHL}	D to X	0.86	0.91	1.09	0.57	1.21	1.28	1.51	0.76
t_{PLH}	Propagation Delay,	0.43	0.48	0.60	0.41	0.67	0.73	0.90	0.58
t_{PHL}	E to X	0.83	0.89	1.06	0.57	1.09	1.17	1.40	0.76
t_{PLH}	Propagation Delay,	0.52	0.56	0.68	0.41	0.76	0.82	0.99	0.58
t_{PHL}	F to X	0.87	0.93	1.10	0.57	1.14	1.22	1.45	0.76
t_{PLH}	Propagation Delay,	0.59	0.63	0.75	0.41	0.84	0.90	1.08	0.58
t_{PHL}	G to X	0.89	0.95	1.12	0.57	1.21	1.28	1.51	0.76
t_{PLH}	Propagation Delay,	0.62	0.66	0.78	0.42	0.89	0.95	1.12	0.58
t_{PHL}	H to X	0.87	0.92	1.09	0.57	1.21	1.28	1.51	0.76
t_r	Output Rise Time, X	0.27	0.39	0.76	1.21	0.30	0.47	0.98	1.71
t_f	Output Fall Time, X	0.23	0.32	0.61	0.96	0.28	0.41	0.78	1.23

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: NAN8H



2-Input NOR Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

NOR2
NOR2H
NOR2B

MACRO	EQUIV. GATES
NOR2	1
NOR2H, NOR2B	2

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A,B

MACRO	INPUT CAP.
NOR2	A,B: 0.05pF
NOR2H	A,B: 0.09pF
NOR2B	A,B: 0.07pF

FUNCTION TABLE

A	B	X
L	L	H
L	H	L
H	L	L
H	H	L

CMOS SWITCHING CHARACTERISTICS

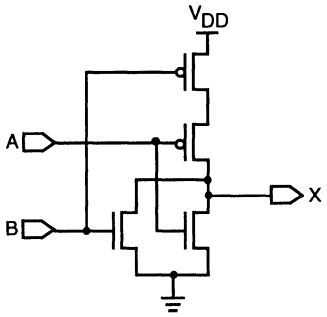
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
NOR2									
t_{PLH}	Propagation Delay, A to X	0.18	0.34	0.82	1.60	0.22	0.45	1.16	2.35
t_{PHL}		0.21	0.28	0.51	0.76	0.29	0.38	0.65	0.91
t_{PLH}	Propagation Delay, B to X	0.16	0.32	0.81	1.60	0.23	0.46	1.17	2.36
t_{PHL}		0.24	0.31	0.54	0.76	0.32	0.41	0.69	0.91
t_r	Output Rise Time, X	0.26	0.75	2.21	4.86	0.36	1.06	3.17	7.01
t_f	Output Fall Time, X	0.19	0.31	0.65	1.15	0.21	0.35	0.78	1.41
NOR2H									
t_{PLH}	Propagation Delay, A to X	0.18	0.26	0.50	0.80	0.22	0.34	0.69	1.18
t_{PHL}		0.18	0.22	0.33	0.38	0.26	0.30	0.44	0.46
t_{PLH}	Propagation Delay, B to X	0.17	0.25	0.49	0.80	0.23	0.35	0.70	1.18
t_{PHL}		0.21	0.25	0.36	0.38	0.29	0.34	0.48	0.46
t_r	Output Rise Time, X	0.29	0.53	1.26	2.42	0.36	0.71	1.76	3.50
t_f	Output Fall Time, X	0.22	0.27	0.44	0.55	0.23	0.30	0.50	0.68
NOR2B									
t_{PLH}	Propagation Delay, A to X	0.12	0.20	0.44	0.80	0.17	0.29	0.64	1.17
t_{PHL}		0.27	0.34	0.57	0.75	0.34	0.43	0.70	0.91
t_{PLH}	Propagation Delay, B to X	0.10	0.18	0.42	0.80	0.17	0.29	0.64	1.18
t_{PHL}		0.32	0.39	0.62	0.76	0.39	0.48	0.76	0.91
t_r	Output Rise Time, X	0.27	0.52	1.24	2.41	0.32	0.67	1.72	3.49
t_f	Output Fall Time, X	0.24	0.36	0.70	1.15	0.26	0.40	0.82	1.41

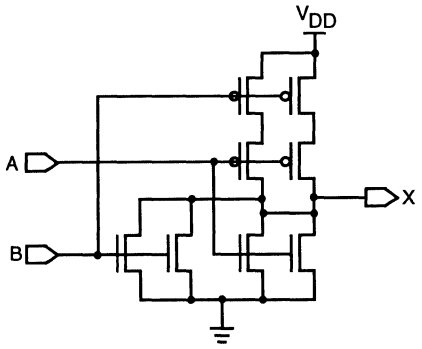
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

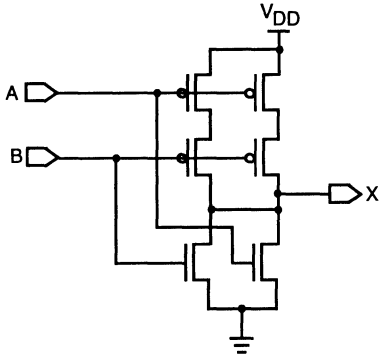
FUNCTIONAL DIAGRAM: NOR2



FUNCTIONAL DIAGRAM: NOR2H



FUNCTIONAL DIAGRAM: NOR2B



7

3-Input NOR3 Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

NOR3
NOR3H

MACRO	EQUIV. GATES
NOR3	2
NOR3H	4

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-C

MACRO	INPUT CAP.
All	A-C: 0.05pF

FUNCTION TABLE

A	B	C	X
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

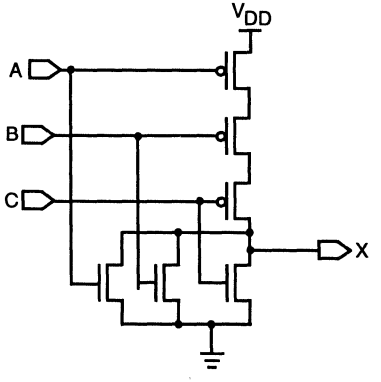
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

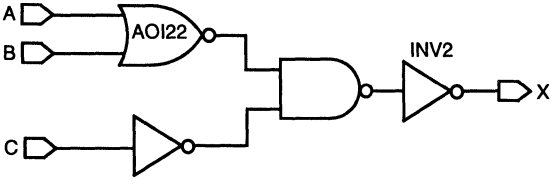
Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	NOR3								
t_{PLH}	Propagation Delay, A to X	0.25	0.49	1.22	2.42	0.32	0.68	1.77	3.61
t_{PHL}		0.22	0.30	0.52	0.76	0.31	0.40	0.67	0.91
t_{PLH}	Propagation Delay, B to X	0.30	0.54	1.27	2.42	0.42	0.79	1.87	3.62
t_{PHL}		0.25	0.32	0.55	0.76	0.35	0.44	0.71	0.91
t_{PLH}	Propagation Delay, C to X	0.30	0.54	1.27	2.42	0.47	0.83	1.91	3.62
t_{PHL}		0.25	0.32	0.55	0.76	0.36	0.45	0.73	0.92
t_r	Output Rise Time, X	0.57	1.30	3.50	7.34	0.83	1.89	5.08	10.63
t_f	Output Fall Time, X	0.25	0.37	0.71	1.15	0.28	0.42	0.84	1.41
	NOR3H								
t_{PLH}	Propagation Delay, A to X	0.64	0.68	0.81	0.43	0.89	0.95	1.13	0.59
t_{PHL}		0.47	0.51	0.62	0.39	0.70	0.74	0.89	0.47
t_{PLH}	Propagation Delay, B to X	0.65	0.69	0.82	0.43	0.90	0.96	1.14	0.59
t_{PHL}		0.51	0.55	0.66	0.39	0.74	0.79	0.93	0.47
t_{PLH}	Propagation Delay, C to X	0.51	0.55	0.68	0.42	0.69	0.75	0.93	0.59
t_{PHL}		0.55	0.59	0.71	0.39	0.78	0.83	0.97	0.47
t_r	Output Rise Time, X	0.22	0.34	0.70	1.20	0.24	0.41	0.92	1.69
t_f	Output Fall Time, X	0.20	0.26	0.43	0.57	0.25	0.32	0.53	0.68

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: NOR3



FUNCTIONAL DIAGRAM: NOR3H



4-Input NOR Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

NOR4
NOR4H

MACRO	EQUIV. GATES
All	4

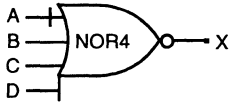
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-D

MACRO	INPUT CAP.
All	A-D: 0.05pF

FUNCTION TABLE

A	B	C	D	X
L	L	L	L	H
X	X	X	H	L
X	X	H	X	L
X	H	X	X	L
H	X	X	X	L



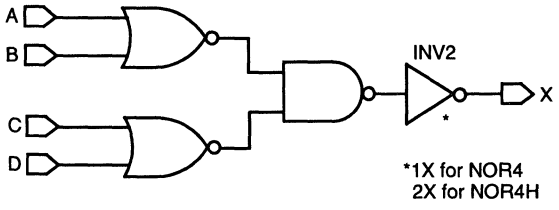
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	NOR4								
t_{PLH}	Propagation Delay, A to X	0.57	0.66	0.90	0.82	0.79	0.91	1.25	1.16
t_{PHL}		0.40	0.48	0.71	0.76	0.59	0.68	0.96	0.91
t_{PLH}	Propagation Delay, B to X	0.58	0.67	0.91	0.83	0.80	0.92	1.26	1.16
t_{PHL}		0.44	0.52	0.75	0.76	0.65	0.74	1.01	0.90
t_{PLH}	Propagation Delay, C to X	0.58	0.67	0.91	0.83	0.80	0.92	1.27	1.16
t_{PHL}		0.44	0.52	0.75	0.76	0.68	0.77	1.05	0.91
t_{PLH}	Propagation Delay, D to X	0.58	0.67	0.92	0.83	0.80	0.92	1.27	1.16
t_{PHL}		0.50	0.58	0.80	0.76	0.72	0.81	1.09	0.92
t_r	Output Rise Time, X	0.17	0.41	1.14	2.43	0.19	0.53	1.57	3.44
t_f	Output Fall Time, X	0.14	0.26	0.61	1.18	0.18	0.32	0.74	1.42
	NOR4H								
t_{PLH}	Propagation Delay, A to X	0.62	0.66	0.79	0.43	0.87	0.93	1.10	0.59
t_{PHL}		0.45	0.49	0.61	0.39	0.67	0.72	0.86	0.48
t_{PLH}	Propagation Delay, B to X	0.63	0.67	0.80	0.43	0.87	0.93	1.11	0.59
t_{PHL}		0.49	0.53	0.65	0.39	0.72	0.77	0.91	0.47
t_{PLH}	Propagation Delay, C to X	0.63	0.67	0.80	0.43	0.86	0.92	1.10	0.59
t_{PHL}		0.49	0.53	0.65	0.39	0.74	0.79	0.94	0.48
t_{PLH}	Propagation Delay, D to X	0.63	0.67	0.80	0.43	0.87	0.93	1.11	0.59
t_{PHL}		0.55	0.58	0.70	0.39	0.78	0.83	0.97	0.49
t_r	Output Rise Time, X	0.18	0.30	0.65	1.18	0.20	0.37	0.88	1.68
t_f	Output Fall Time, X	0.19	0.25	0.42	0.57	0.21	0.28	0.48	0.68

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: NOR4



*1X for NOR4
2X for NOR4H

7

5-Input NOR Gate, 1X & 2X Drive (3.3 V and 5 V Core Voltage)

NOR5
NOR5H

MACRO	EQUIV. GATES
NOR5	4
NOR5H	5

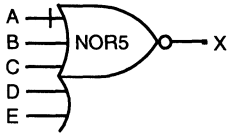
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-E

MACRO	INPUT CAP.
All	A-E: 0.05pF

FUNCTION TABLE

A	B	C	D	E	X
L	L	L	L	L	H
X	X	X	X	H	L
X	X	X	H	X	L
X	X	H	X	X	L
X	H	X	X	X	L
H	X	X	X	X	L



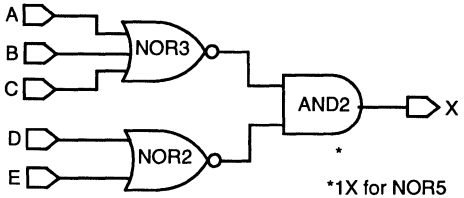
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	NOR5								
t_{PLH}	Propagation Delay, A to X	0.80	0.88	1.13	0.82	1.11	1.23	1.58	1.16
t_{PHL}		0.44	0.51	0.74	0.76	0.67	0.76	1.03	0.91
t_{PLH}	Propagation Delay, B to X	0.84	0.92	1.17	0.83	1.20	1.32	1.67	1.16
t_{PHL}		0.48	0.55	0.78	0.76	0.69	0.79	1.06	0.92
t_{PLH}	Propagation Delay, C to X	0.84	0.92	1.17	0.83	1.25	1.37	1.72	1.16
t_{PHL}		0.48	0.55	0.78	0.76	0.71	0.80	1.08	0.92
t_{PLH}	Propagation Delay, D to X	0.58	0.67	0.92	0.83	0.82	0.94	1.28	1.16
t_{PHL}		0.48	0.55	0.78	0.76	0.70	0.79	1.06	0.92
t_{PLH}	Propagation Delay, E to X	0.60	0.68	0.93	0.83	0.82	0.94	1.28	1.16
t_{PHL}		0.51	0.59	0.82	0.76	0.74	0.83	1.10	0.92
t_r	Output Rise Time, X	0.19	0.43	1.16	2.43	0.23	0.57	1.60	3.44
t_f	Output Fall Time, X	0.15	0.27	0.62	1.18	0.18	0.33	0.75	1.43
	NOR5H								
t_{PLH}	Propagation Delay, A to X	0.86	0.90	1.03	0.42	1.20	1.26	1.44	0.60
t_{PHL}		0.49	0.53	0.65	0.39	0.74	0.79	0.93	0.47
t_{PLH}	Propagation Delay, B to X	0.91	0.95	1.08	0.42	1.29	1.35	1.53	0.60
t_{PHL}		0.53	0.57	0.69	0.38	0.77	0.82	0.96	0.48
t_{PLH}	Propagation Delay, C to X	0.91	0.95	1.08	0.42	1.34	1.40	1.57	0.60
t_{PHL}		0.53	0.57	0.69	0.38	0.80	0.85	0.99	0.47
t_{PLH}	Propagation Delay, D to X	0.64	0.68	0.81	0.42	0.88	0.94	1.12	0.59
t_{PHL}		0.52	0.56	0.68	0.39	0.77	0.82	0.96	0.47
t_{PLH}	Propagation Delay, E to X	0.64	0.68	0.81	0.43	0.90	0.95	1.13	0.59
t_{PHL}		0.56	0.60	0.71	0.39	0.80	0.85	0.99	0.48
t_r	Output Rise Time, X	0.23	0.35	0.71	1.18	0.28	0.44	0.95	1.69
t_f	Output Fall Time, X	0.20	0.26	0.42	0.55	0.26	0.32	0.53	0.68

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

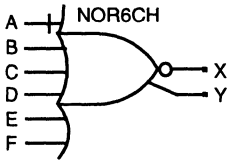
FUNCTIONAL DIAGRAM: NOR5



*1X for NOR5
2X for NOR5H

6-Input NOR Gate 2X Drive with Complementary Output 1X Drive (3.3 V and 5 V Core Voltage)

NOR6CH



MACRO	EQUIV. GATES
NOR6CH	6

Rev. 1.07

MACRO	OUTPUTS/INPUTS
NOR6CH	X,Y / A-F

MACRO	INPUT CAP.
NOR6CH	A-F: 0.05pF

FUNCTION TABLE

A	B	C	D	E	F	X	Y
L	L	L	L	L	L	H	L
X	X	X	X	X	H	L	H
X	X	X	X	H	X	L	H
X	X	X	H	X	X	L	H
X	X	H	X	X	X	L	H
X	H	X	X	X	X	L	H
H	X	X	X	X	X	L	H

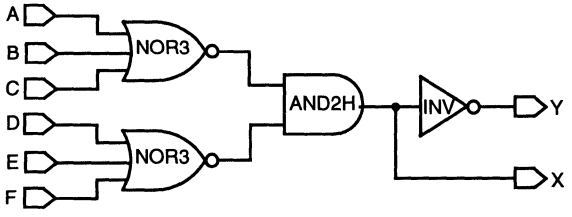
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	NOR6CH								
t_{PLH}	Propagation Delay, A to X	0.88	0.92	1.05	0.42	1.24	1.30	1.47	0.59
t_{PHL}		0.52	0.56	0.67	0.38	0.77	0.81	0.95	0.47
t_{PLH}	Propagation Delay, B to X	0.94	0.98	1.10	0.41	1.32	1.38	1.56	0.59
t_{PHL}		0.56	0.60	0.71	0.38	0.80	0.84	0.99	0.47
t_{PLH}	Propagation Delay, C to X	0.94	0.98	1.10	0.41	1.37	1.43	1.61	0.59
t_{PHL}		0.56	0.60	0.71	0.38	0.83	0.87	1.01	0.47
t_{PLH}	Propagation Delay, D to X	0.85	0.90	1.02	0.42	1.18	1.24	1.42	0.59
t_{PHL}		0.56	0.60	0.72	0.38	0.82	0.87	1.01	0.47
t_{PLH}	Propagation Delay, E to X	0.88	0.92	1.05	0.42	1.27	1.33	1.51	0.59
t_{PHL}		0.60	0.63	0.75	0.38	0.86	0.91	1.05	0.47
t_{PLH}	Propagation Delay, F to X	0.88	0.92	1.05	0.42	1.31	1.37	1.54	0.59
t_{PHL}		0.60	0.63	0.75	0.38	0.88	0.93	1.07	0.47
t_{PLH}	Propagation Delay, X to Y	0.08	0.16	0.41	0.83	0.12	0.24	0.58	1.15
t_{PHL}		0.14	0.21	0.44	0.76	0.22	0.31	0.59	0.91
t_r	Output Rise Time, X	0.29	0.41	0.77	1.18	0.37	0.54	1.05	1.70
t_f	Output Fall Time, X	0.23	0.29	0.46	0.57	0.28	0.35	0.56	0.69
t_r	Output Rise Time, Y	0.17	0.41	1.13	2.42	0.19	0.53	1.56	3.44
t_f	Output Fall Time, Y	0.15	0.26	0.61	1.17	0.20	0.34	0.77	1.40

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: NOR6CH



7

8-Input NOR Gate
2X Drive
(3.3 V and 5 V Core Voltage)

NOR8H

MACRO	EQUIV. GATES
NOR8H	7

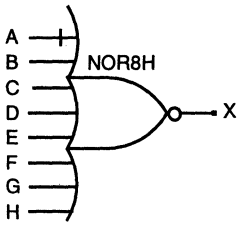
Rev. 1.07

MACRO	OUTPUTS/INPUTS
NOR8H	X / A-H

MACRO	INPUT CAP.
NOR8H	A-H: 0.05pF

FUNCTION TABLE

A	B	C	D	E	F	GF	H	X
L	L	L	L	L	L	L	L	H
X	X	X	X	X	X	X	H	L
X	X	X	X	X	X	H	X	L
X	X	X	X	X	H	X	X	L
X	X	X	X	H	X	X	X	L
X	X	X	H	X	X	X	X	L
X	X	H	X	X	X	X	X	L
X	H	X	X	X	X	X	X	L
H	X	X	X	X	X	X	X	L



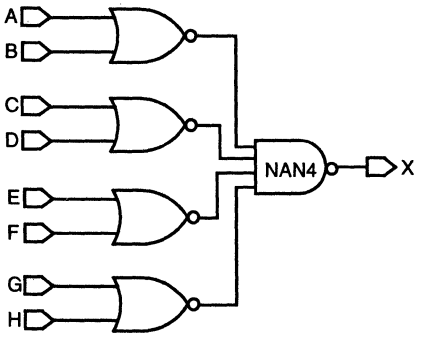
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	NOR8H								
t_{PLH}	Propagation Delay, A to X	0.80	0.85	0.99	0.45	1.11	1.17	1.37	0.64
t_{PHL}		0.48	0.52	0.64	0.40	0.73	0.77	0.92	0.48
t_{PLH}	Propagation Delay, B to X	0.82	0.86	1.00	0.45	1.12	1.19	1.38	0.64
t_{PHL}		0.52	0.56	0.68	0.39	0.76	0.81	0.95	0.49
t_{PLH}	Propagation Delay, C to X	0.86	0.90	1.04	0.45	1.18	1.25	1.44	0.64
t_{PHL}		0.55	0.59	0.71	0.39	0.80	0.85	1.00	0.49
t_{PLH}	Propagation Delay, D to X	0.86	0.91	1.04	0.45	1.18	1.25	1.44	0.65
t_{PHL}		0.58	0.62	0.74	0.40	0.83	0.88	1.03	0.49
t_{PLH}	Propagation Delay, E to X	0.89	0.94	1.08	0.45	1.25	1.32	1.51	0.65
t_{PHL}		0.60	0.64	0.76	0.40	0.89	0.94	1.09	0.50
t_{PLH}	Propagation Delay, F,G to X	0.90	0.95	1.08	0.45	1.25	1.32	1.51	0.65
t_{PHL}		0.64	0.68	0.80	0.40	0.93	0.98	1.12	0.49
t_{PLH}	Propagation Delay, H to X	0.90	0.94	1.08	0.45	1.28	1.34	1.53	0.64
t_{PHL}		0.66	0.71	0.83	0.41	0.96	1.01	1.16	0.51
t_r	Output Rise Time, X	0.26	0.38	0.74	1.18	0.35	0.52	1.02	1.68
t_f	Output Fall Time, X	0.24	0.30	0.47	0.56	0.30	0.37	0.58	0.69

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: NOR8H



2, 1-Input OR-AND Gate
2X Drive
(3.3 V and 5 V Core Voltage)

OA21H

MACRO	EQUIV. GATES
OA21H	3

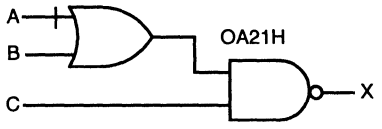
Rev. 1.07

MACRO	OUTPUTS/INPUTS
OA21H	X / A-C

MACRO	INPUT CAP.
OA21H	A-C: 0.05pF

FUNCTION TABLE

A	B	C	X
X	X	L	L
H	X	H	H
X	H	H	H
L	L	X	L



CMOS SWITCHING CHARACTERISTICS

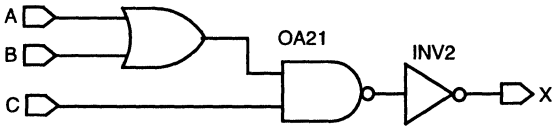
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	OA21H								
t_{PLH}	Propagation Delay, A to X	0.42	0.46	0.59	0.43	0.57	0.63	0.81	0.60
t_{PHL}		0.53	0.57	0.70	0.42	0.77	0.82	0.98	0.54
t_{PLH}	Propagation Delay, B to X	0.48	0.52	0.65	0.43	0.63	0.69	0.87	0.60
t_{PHL}		0.52	0.56	0.69	0.42	0.77	0.83	0.99	0.54
t_{PLH}	Propagation Delay, C to X	0.52	0.56	0.69	0.42	0.68	0.74	0.92	0.59
t_{PHL}		0.44	0.49	0.61	0.41	0.63	0.68	0.84	0.51
t_r	Output Rise Time, X	0.20	0.32	0.68	1.20	0.23	0.40	0.90	1.68
t_f	Output Fall Time, X	0.27	0.33	0.49	0.55	0.33	0.40	0.60	0.70

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: OA21H



2-Wide, 2-Input OR-AND Gate
2X Drive
(3.3 V and 5 V Core Voltage)

OA22H

MACRO	EQUIV. GATES
OA22H	3

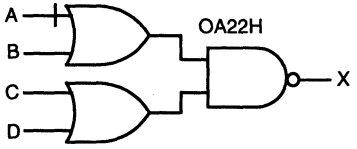
Rev. 1.07

MACRO	OUTPUTS/INPUTS
OA22H	X / A-D

MACRO	INPUT CAP.
OA22H	A-D: 0.05pF

FUNCTION TABLE

A	B	C	D	X
H	X	H	X	H
X	H	H	X	H
H	X	X	H	H
X	H	X	H	H
L	L	X	X	L
X	X	L	L	L



CMOS SWITCHING CHARACTERISTICS

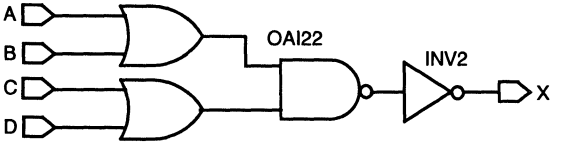
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	OA22H								
t_{PLH}	Propagation Delay, A to X	0.41	0.45	0.58	0.42	0.57	0.63	0.81	0.59
t_{PHL}		0.75	0.80	0.93	0.45	1.11	1.17	1.34	0.56
t_{PLH}	Propagation Delay, B to X	0.45	0.49	0.62	0.43	0.63	0.69	0.86	0.59
t_{PHL}		0.74	0.79	0.92	0.45	1.13	1.18	1.35	0.56
t_{PLH}	Propagation Delay, C to X	0.47	0.52	0.64	0.43	0.63	0.69	0.87	0.60
t_{PHL}		0.56	0.60	0.74	0.44	0.79	0.85	1.02	0.58
t_{PLH}	Propagation Delay, D to X	0.47	0.51	0.64	0.43	0.63	0.69	0.87	0.60
t_{PHL}		0.52	0.56	0.68	0.42	0.77	0.82	0.98	0.54
t_r	Output Rise Time, X	0.19	0.31	0.67	1.20	0.23	0.40	0.90	1.68
t_f	Output Fall Time, X	0.36	0.41	0.59	0.57	0.43	0.50	0.71	0.71

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: OA22H



2, 1-Input OR-AND-INVERT Gate, 1X and 2X Drive (3.3 V and 5 V Core Voltage)

OAI21
OAI21H

MACRO	EQUIV. GATES
OAI21	2
OAI21H	3

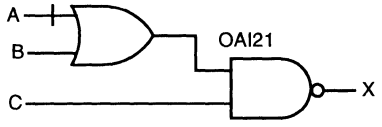
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-C

MACRO	INPUT CAP.
OAI21	A-C: 0.05pF
OAI21H	A-C: 0.09pF

FUNCTION TABLE

A	B	C	X
H	X	H	L
X	H	H	L
H	X	X	L
X	H	X	L
L	L	X	H
X	X	L	H



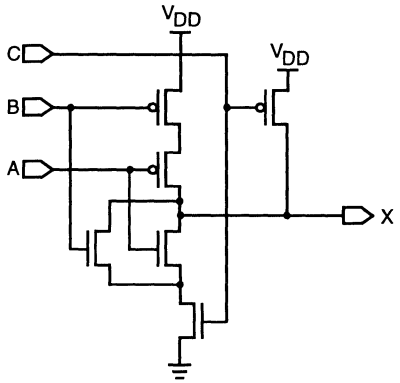
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

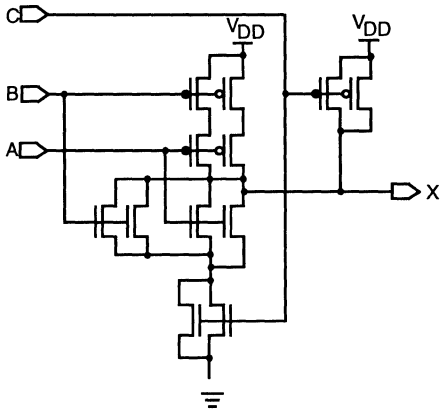
Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	OAI21								
t_{PLH}	Propagation Delay, A to X	0.19	0.35	0.83	1.61	0.25	0.49	1.20	2.36
t_{PHL}		0.26	0.38	0.72	1.14	0.35	0.50	0.95	1.50
t_{PLH}	Propagation Delay, B to X	0.17	0.33	0.82	1.61	0.27	0.50	1.21	2.36
t_{PHL}		0.31	0.43	0.77	1.14	0.40	0.55	1.00	1.50
t_{PLH}	Propagation Delay, C to X	0.21	0.29	0.54	0.82	0.28	0.40	0.74	1.16
t_{PHL}		0.32	0.44	0.78	1.14	0.42	0.57	1.02	1.50
t_r	Output Rise Time, X	0.40	0.88	2.34	4.86	0.51	1.21	3.32	7.01
t_f	Output Fall Time, X	0.28	0.48	1.07	1.97	0.30	0.55	1.32	2.55
	OAI21H								
t_{PLH}	Propagation Delay, A to X	0.18	0.26	0.50	0.80	0.25	0.36	0.72	1.18
t_{PHL}		0.25	0.30	0.47	0.57	0.33	0.40	0.63	0.75
t_{PLH}	Propagation Delay, B to X	0.17	0.25	0.50	0.80	0.26	0.38	0.73	1.18
t_{PHL}		0.29	0.35	0.52	0.57	0.38	0.46	0.68	0.75
t_{PLH}	Propagation Delay, C to X	0.20	0.24	0.36	0.41	0.26	0.31	0.49	0.58
t_{PHL}		0.31	0.37	0.54	0.57	0.40	0.48	0.70	0.75
t_r	Output Rise Time, X	0.41	0.65	1.37	2.42	0.51	0.85	1.90	3.50
t_f	Output Fall Time, X	0.29	0.39	0.68	0.96	0.33	0.45	0.82	1.23

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: OAI21



FUNCTIONAL DIAGRAM: OAI21H



7

2, 1, 1-Input OR-AND-INVERT Gate 1X & 2X Drive (3.3 V and 5 V Core Voltage)

OAI211
OAI211H

MACRO	EQUIV. GATES
OAI211	2
OAI211H	4

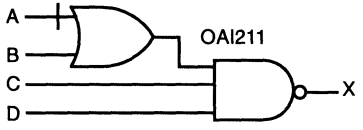
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-D

MACRO	INPUT CAP.
All	A-D: 0.05pF

FUNCTION TABLE

A	B	C	D	X
H	X	H	H	L
X	H	H	H	L
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H



CMOS SWITCHING CHARACTERISTICS

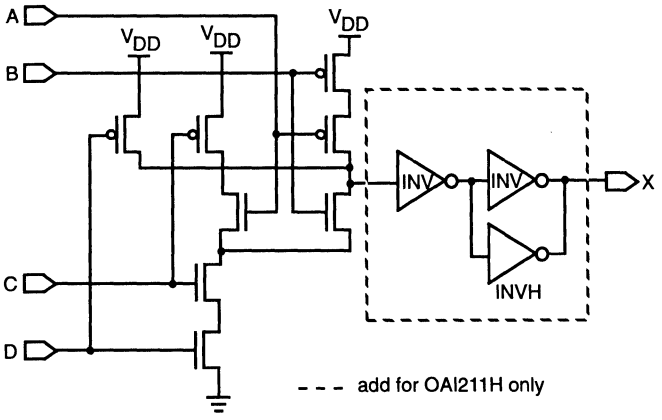
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	OAI211								
t_{PLH}	Propagation Delay, A to X	0.19	0.35	0.83	1.61	0.27	0.51	1.22	2.36
t_{PHL}		0.26	0.38	0.72	1.14	0.38	0.59	1.22	2.10
t_{PLH}	Propagation Delay, B to X	0.17	0.33	0.82	1.61	0.29	0.52	1.23	2.36
t_{PHL}		0.31	0.43	0.77	1.14	0.45	0.66	1.30	2.11
t_{PLH}	Propagation Delay, C to X	0.21	0.29	0.54	0.82	0.29	0.41	0.75	1.16
t_{PHL}		0.32	0.44	0.78	1.14	0.54	0.75	1.38	2.11
t_{PLH}	Propagation Delay, D to X	0.21	0.29	0.54	0.82	0.33	0.44	0.79	1.16
t_{PHL}		0.32	0.44	0.78	1.14	0.52	0.74	1.37	2.11
t_r	Output Rise Time, X	0.40	0.88	2.34	4.86	0.63	1.33	3.44	7.01
t_f	Output Fall Time, X	0.28	0.48	1.07	1.97	0.44	0.81	1.90	3.67
	OAI211H								
t_{PLH}	Propagation Delay, A to X	0.61	0.64	0.73	0.29	0.90	0.94	1.05	0.40
t_{PHL}		0.72	0.74	0.82	0.27	1.00	1.03	1.14	0.34
t_{PLH}	Propagation Delay, B to X	0.61	0.64	0.73	0.28	0.91	0.95	1.06	0.39
t_{PHL}		0.77	0.80	0.88	0.28	1.09	1.13	1.23	0.34
t_{PLH}	Propagation Delay, C to X	0.58	0.61	0.69	0.28	0.83	0.87	0.99	0.39
t_{PHL}		0.86	0.89	0.97	0.27	1.17	1.21	1.31	0.35
t_{PLH}	Propagation Delay, D to X	0.64	0.67	0.75	0.28	0.88	0.92	1.04	0.40
t_{PHL}		0.84	0.87	0.95	0.28	1.17	1.20	1.31	0.35
t_r	Output Rise Time, X	0.20	0.28	0.51	0.78	0.22	0.33	0.67	1.11
t_f	Output Fall Time, X	0.23	0.27	0.38	0.37	0.28	0.33	0.46	0.45

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: OAI211



7

2-Wide, 2-Input OR-AND-INVERT Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

OAI22
OAI22H

MACRO	EQUIV. GATES
OAI22	2
OAI22H	4

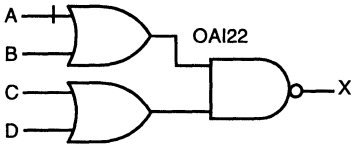
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-D

MACRO	INPUT CAP.
All	A-D: 0.05pF

FUNCTION TABLE

A	B	C	D	X
H	X	H	X	L
X	H	H	X	L
H	X	X	H	L
X	H	X	H	L
L	L	X	X	H
X	X	L	L	H



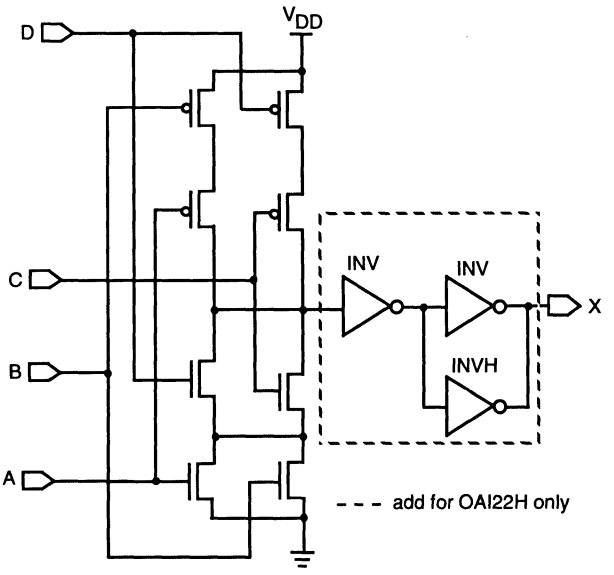
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	OAI22								
t_{PLH}	Propagation Delay, A to X	0.33	0.49	0.97	1.61	0.45	0.69	1.39	2.36
t_{PHL}		0.31	0.43	0.77	1.14	0.42	0.57	1.02	1.50
t_{PLH}	Propagation Delay, B to X	0.35	0.51	0.99	1.60	0.53	0.77	1.47	2.36
t_{PHL}		0.32	0.40	0.66	0.86	0.41	0.53	0.86	1.13
t_{PLH}	Propagation Delay, C to X	0.19	0.35	0.84	1.61	0.25	0.48	1.19	2.36
t_{PHL}		0.31	0.43	0.77	1.14	0.40	0.55	1.00	1.50
t_{PLH}	Propagation Delay, D to X	0.17	0.33	0.82	1.60	0.26	0.49	1.20	2.36
t_{PHL}		0.28	0.37	0.65	0.92	0.37	0.49	0.84	1.18
t_r	Output Rise Time, X	0.74	1.23	2.69	4.87	1.01	1.71	3.82	7.01
t_f	Output Fall Time, X	0.28	0.48	1.07	1.97	0.29	0.54	1.31	2.55
	OAI22H								
t_{PLH}	Propagation Delay, A to X	0.84	0.87	0.95	0.29	1.20	1.24	1.36	0.40
t_{PHL}		0.69	0.72	0.80	0.27	0.99	1.02	1.13	0.34
t_{PLH}	Propagation Delay, B to X	0.86	0.88	0.97	0.28	1.25	1.29	1.41	0.40
t_{PHL}		0.67	0.70	0.78	0.27	0.96	0.99	1.09	0.34
t_{PLH}	Propagation Delay, C to X	0.64	0.67	0.76	0.29	0.91	0.95	1.07	0.40
t_{PHL}		0.68	0.71	0.79	0.27	0.94	0.98	1.08	0.34
t_{PLH}	Propagation Delay, D to X	0.61	0.64	0.73	0.29	0.87	0.91	1.03	0.39
t_{PHL}		0.62	0.65	0.73	0.27	0.88	0.91	1.01	0.34
t_r	Output Rise Time, X	0.21	0.28	0.51	0.76	0.24	0.35	0.68	1.11
t_f	Output Fall Time, X	0.21	0.25	0.36	0.37	0.25	0.30	0.44	0.45

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: OAI22



7

2-Input OR + 2-Input NAND Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

ONDAI22
ONDAI22H

MACRO	EQUIV. GATES
ONDAI22	3
ONDAI22H	4

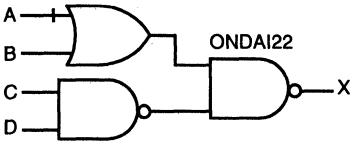
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-D

MACRO	INPUT CAP.
ONDAI22	A-D: 0.05pF
ONDAI22H	A,B: 0.09pF C,D: 0.05pF

FUNCTION TABLE

A	B	C	D	X
L	L	X	X	H
X	X	H	H	H
X	H	X	L	L
H	X	X	L	L
X	H	L	X	L
H	X	L	X	L



CMOS SWITCHING CHARACTERISTICS

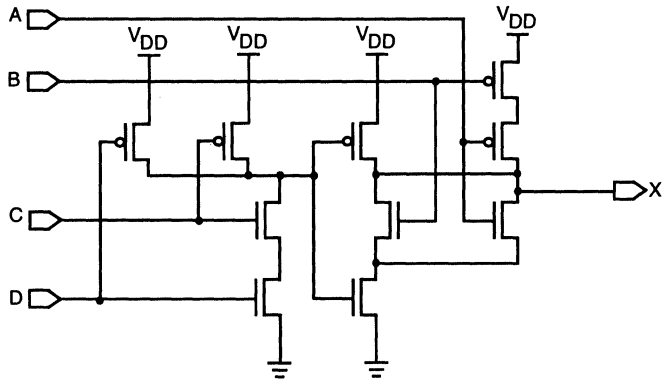
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	ONDAI22								
t_{PLH}	Propagation Delay, A to X	0.19	0.35	0.83	1.61	0.26	0.49	1.20	2.36
t_{PHL}		0.27	0.38	0.72	1.14	0.35	0.50	0.95	1.50
t_{PLH}	Propagation Delay, B to X	0.18	0.34	0.82	1.61	0.27	0.51	1.21	2.36
t_{PHL}		0.31	0.43	0.77	1.14	0.40	0.55	1.00	1.50
t_{PLH}	Propagation Delay, C to X	0.46	0.54	0.79	0.83	0.62	0.73	1.08	1.16
t_{PHL}		0.36	0.47	0.81	1.14	0.52	0.67	1.12	1.51
t_{PLH}	Propagation Delay, D to X	0.46	0.54	0.79	0.83	0.61	0.73	1.07	1.16
t_{PHL}		0.43	0.55	0.89	1.14	0.60	0.75	1.21	1.51
t_r	Output Rise Time, X	0.40	0.88	2.34	4.87	0.53	1.23	3.33	7.01
t_f	Output Fall Time, X	0.28	0.48	1.08	1.99	0.30	0.56	1.32	2.55
	ONDAI22H								
t_{PLH}	Propagation Delay, A to X	0.18	0.26	0.50	0.80	0.24	0.35	0.71	1.18
t_{PHL}		0.24	0.30	0.47	0.57	0.32	0.40	0.62	0.75
t_{PLH}	Propagation Delay, B to X	0.18	0.26	0.50	0.80	0.26	0.38	0.73	1.19
t_{PHL}		0.29	0.35	0.52	0.57	0.38	0.46	0.69	0.75
t_{PLH}	Propagation Delay, C to X	0.51	0.56	0.68	0.42	0.69	0.75	0.92	0.59
t_{PHL}		0.42	0.48	0.65	0.57	0.61	0.69	0.91	0.76
t_{PLH}	Propagation Delay, D to X	0.51	0.55	0.68	0.41	0.68	0.74	0.91	0.58
t_{PHL}		0.49	0.54	0.72	0.57	0.69	0.76	0.99	0.76
t_r	Output Rise Time, X	0.41	0.65	1.38	2.42	0.55	0.90	1.95	3.50
t_f	Output Fall Time, X	0.29	0.39	0.68	0.97	0.33	0.45	0.82	1.24

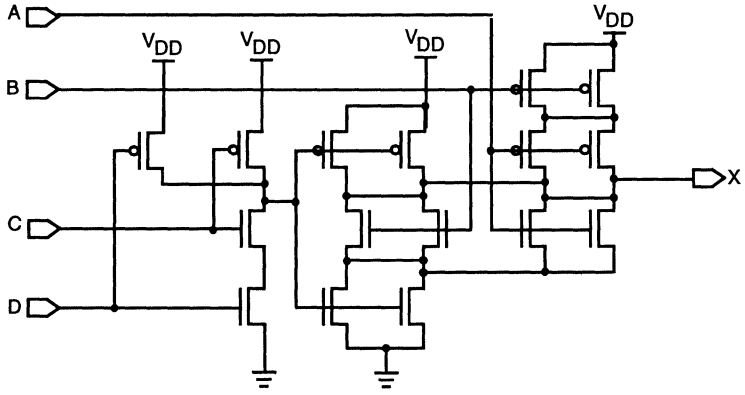
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: ONDAI22



FUNCTIONAL DIAGRAM: ONDAI22H



7

2-Input OR Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

OR2
OR2H

MACRO	EQUIV. GATES
All	2

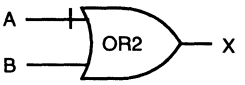
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A,B

MACRO	INPUT CAP.
All	A,B: 0.05pF

FUNCTION TABLE

A	B	X
L	L	L
L	H	H
H	L	H
H	H	H



CMOS SWITCHING CHARACTERISTICS

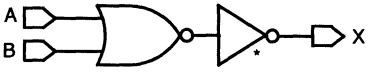
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	OR2								
t_{PLH}	Propagation Delay, A to X	0.26	0.35	0.60	0.83	0.38	0.50	0.84	1.15
t_{PHL}		0.42	0.50	0.73	0.77	0.60	0.70	0.98	0.94
t_{PLH}	Propagation Delay, B to X	0.30	0.39	0.63	0.82	0.42	0.53	0.88	1.15
t_{PHL}		0.44	0.51	0.74	0.76	0.61	0.70	0.98	0.94
t_r	Output Rise Time, X	0.17	0.41	1.14	2.42	0.17	0.52	1.55	3.45
t_f	Output Fall Time, X	0.20	0.31	0.66	1.15	0.26	0.40	0.82	1.41
	OR2H								
t_{PLH}	Propagation Delay, A to X	0.32	0.36	0.49	0.41	0.44	0.50	0.67	0.58
t_{PHL}		0.53	0.57	0.69	0.41	0.74	0.79	0.95	0.53
t_{PLH}	Propagation Delay, B to X	0.36	0.40	0.52	0.41	0.48	0.54	0.71	0.58
t_{PHL}		0.53	0.57	0.69	0.41	0.75	0.80	0.96	0.52
t_r	Output Rise Time, X	0.15	0.27	0.63	1.21	0.19	0.37	0.88	1.72
t_f	Output Fall Time, X	0.27	0.33	0.49	0.56	0.32	0.39	0.59	0.70

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

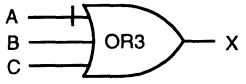
FUNCTIONAL DIAGRAM: OR2



*1X for OR2
2X for OR2H

3-Input OR Gate
1X & 2X Drive
(3.3 V and 5 V Core Voltage)

OR3
OR3H



MACRO	EQUIV. GATES
OR3	2
OR3H	3

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-C

MACRO	INPUT CAP.
All	A-C: 0.05pF

FUNCTION TABLE

A	B	C	X
L	L	L	L
L	X	H	H
X	H	X	H
H	X	X	H

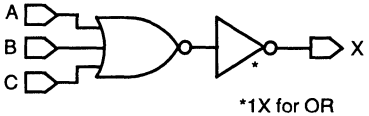
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
OR3									
t_{PLH}	Propagation Delay, A to X	0.28	0.36	0.61	0.82	0.41	0.52	0.87	1.15
t_{PHL}		0.62	0.70	0.94	0.81	0.89	0.99	1.29	1.01
t_{PLH}	Propagation Delay, B to X	0.32	0.40	0.65	0.82	0.45	0.56	0.91	1.16
t_{PHL}		0.67	0.75	0.99	0.81	0.98	1.08	1.39	1.01
t_{PLH}	Propagation Delay, C to X	0.32	0.40	0.65	0.82	0.47	0.58	0.93	1.16
t_{PHL}		0.67	0.75	0.99	0.81	1.03	1.13	1.43	1.00
t_r	Output Rise Time, X	0.16	0.40	1.13	2.44	0.19	0.53	1.57	3.45
t_f	Output Fall Time, X	0.29	0.41	0.75	1.14	0.38	0.52	0.94	1.40
OR3H									
t_{PLH}	Propagation Delay, A to X	0.34	0.38	0.50	0.41	0.47	0.52	0.70	0.58
t_{PHL}		0.74	0.79	0.93	0.46	1.07	1.13	1.31	0.61
t_{PLH}	Propagation Delay, B to X	0.36	0.40	0.53	0.41	0.50	0.56	0.74	0.59
t_{PHL}		0.79	0.83	0.97	0.46	1.17	1.23	1.41	0.60
t_{PLH}	Propagation Delay, C to X	0.36	0.40	0.53	0.41	0.52	0.58	0.76	0.59
t_{PHL}		0.79	0.83	0.97	0.46	1.20	1.26	1.45	0.61
t_r	Output Rise Time, X	0.15	0.28	0.64	1.21	0.23	0.40	0.91	1.70
t_f	Output Fall Time, X	0.39	0.45	0.62	0.57	0.49	0.56	0.78	0.72

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: OR3



*1X for OR
2X for OR3H

4-Input OR Gate, 1X & 2X Drive (3.3 V and 5 V Core Voltage)

OR4 OR4H

MACRO	EQUIV. GATES
All	3

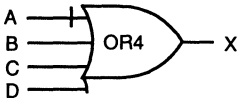
Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	X / A-D

MACRO	INPUT CAP.
All	A-D: 0.05pF

FUNCTION TABLE

A	B	C	D	X
L	L	L	L	L
X	X	X	H	H
X	X	H	X	H
X	H	X	X	H
H	X	X	X	H



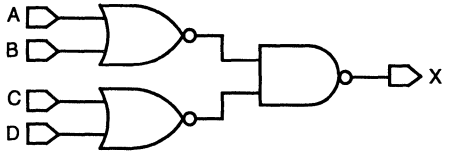
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

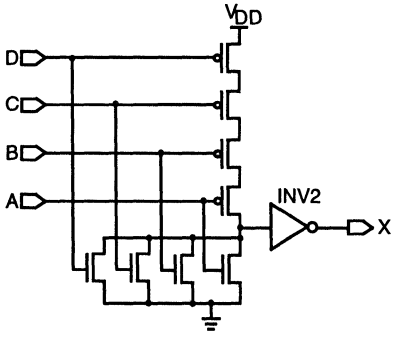
Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	OR4								
t_{PLH}	Propagation Delay, A to X	0.27	0.35	0.60	0.82	0.39	0.50	0.85	1.15
t_{PHL}		0.45	0.56	0.91	1.15	0.63	0.78	1.24	1.51
t_{PLH}	Propagation Delay, B to X	0.31	0.39	0.64	0.82	0.42	0.54	0.89	1.15
t_{PHL}		0.46	0.58	0.92	1.14	0.64	0.79	1.24	1.51
t_{PLH}	Propagation Delay, C to X	0.30	0.38	0.63	0.83	0.42	0.54	0.89	1.15
t_{PHL}		0.44	0.55	0.90	1.14	0.64	0.79	1.24	1.51
t_{PLH}	Propagation Delay, D to X	0.34	0.42	0.67	0.82	0.47	0.58	0.93	1.16
t_{PHL}		0.44	0.56	0.90	1.14	0.63	0.78	1.23	1.51
t_r	Output Rise Time, X	0.22	0.46	1.19	2.43	0.27	0.61	1.65	3.45
t_f	Output Fall Time, X	0.22	0.41	1.00	1.96	0.28	0.54	1.29	2.52
	OR4H								
t_{PLH}	Propagation Delay, A to X	0.34	0.38	0.50	0.41	0.47	0.53	0.70	0.58
t_{PHL}		0.90	0.95	1.10	0.51	1.32	1.38	1.59	0.68
t_{PLH}	Propagation Delay, B to X	0.36	0.40	0.53	0.41	0.51	0.57	0.74	0.59
t_{PHL}		1.00	1.05	1.20	0.51	1.49	1.56	1.76	0.68
t_{PLH}	Propagation Delay, C to X	0.38	0.42	0.54	0.42	0.53	0.59	0.76	0.59
t_{PHL}		1.07	1.12	1.27	0.51	1.61	1.67	1.88	0.68
t_{PLH}	Propagation Delay, D to X	0.38	0.42	0.54	0.42	0.53	0.59	0.77	0.60
t_{PHL}		1.07	1.12	1.27	0.51	1.66	1.72	1.93	0.68
t_r	Output Rise Time, X	0.16	0.28	0.64	1.21	0.23	0.40	0.91	1.70
t_f	Output Fall Time, X	0.51	0.57	0.74	0.58	0.61	0.68	0.91	0.76

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: OR4



FUNCTIONAL DIAGRAM: OR4H



7

8-Input OR Gate, 2X Drive (3.3 V and 5 V Core Voltage)

OR8H

MACRO	EQUIV. GATES
OR8H	8

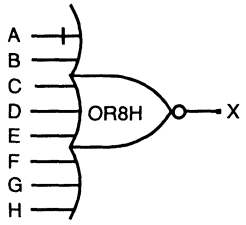
Rev. 1.07

MACRO	OUTPUTS/INPUTS
OR8H	X / A-H

MACRO	INPUT CAP.
OR8H	A-H: 0.05pF

FUNCTION TABLE

A	B	C	D	E	F	G	H	X
L	L	L	L	L	L	L	L	L
X	X	X	X	X	X	X	H	H
X	X	X	X	X	X	H	X	H
X	X	X	X	X	H	X	X	H
X	X	X	X	H	X	X	X	H
X	X	X	H	X	X	X	X	H
X	X	H	X	X	X	X	X	H
X	H	X	X	X	X	X	X	H
H	X	X	X	X	X	X	X	H



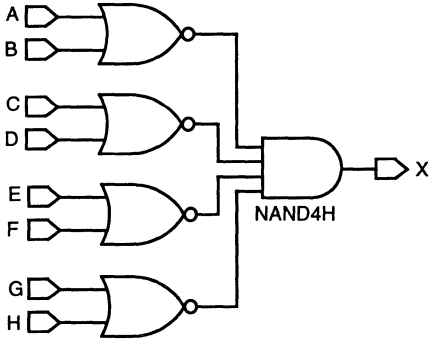
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	OR8								
t_{PLH}	Propagation Delay, A to X	0.34	0.38	0.50	0.41	0.47	0.53	0.70	0.58
t_{PHL}		0.63	0.73	1.02	0.98	0.87	1.01	1.42	1.37
t_{PLH}	Propagation Delay, B to X	0.37	0.41	0.53	0.41	0.51	0.57	0.74	0.58
t_{PHL}		0.64	0.73	1.03	0.98	0.88	1.02	1.43	1.37
t_{PLH}	Propagation Delay, C to X	0.38	0.42	0.54	0.41	0.53	0.59	0.77	0.58
t_{PHL}		0.68	0.78	1.07	0.97	0.94	1.08	1.49	1.37
t_{PLH}	Propagation Delay, D to X	0.41	0.45	0.58	0.41	0.57	0.63	0.81	0.58
t_{PHL}		0.68	0.78	1.07	0.98	0.95	1.09	1.50	1.37
t_{PLH}	Propagation Delay, E to X	0.40	0.45	0.57	0.42	0.58	0.64	0.81	0.59
t_{PHL}		0.70	0.80	1.09	0.98	0.99	1.12	1.54	1.38
t_{PLH}	Propagation Delay, F to X	0.44	0.48	0.61	0.42	0.62	0.68	0.85	0.59
t_{PHL}		0.70	0.79	1.09	0.99	1.00	1.14	1.55	1.38
t_{PLH}	Propagation Delay, G to X	0.40	0.45	0.57	0.42	0.62	0.68	0.85	0.59
t_{PHL}		0.70	0.80	1.09	0.98	1.00	1.14	1.55	1.38
t_{PLH}	Propagation Delay, H to X	0.44	0.48	0.61	0.42	0.64	0.70	0.88	0.60
t_{PHL}		0.70	0.79	1.09	0.99	1.03	1.17	1.58	1.38
t_r	Output Rise Time, X	0.49	0.61	0.97	1.21	0.62	0.79	1.31	1.71
t_f	Output Fall Time, X	0.46	0.64	1.17	1.78	0.58	0.81	1.52	2.37

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: OR8H



8-Bit Rotate, 1X Drive (3.3 V and 5 V Core Voltage)

ROT8A

MACRO	EQUIV. GATES
ROT8A	54

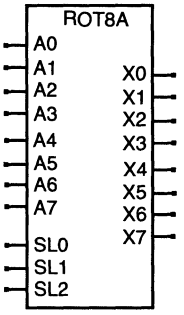
Rev. 1.07

MACRO	OUTPUTS/INPUTS
ROT8A	X0-X7 / A0-A7,SL0-SL2

MACRO	INPUT CAP.
ROT8A	A0-A7,SL0-SL2: 0.10pF

FUNCTION TABLE

SL2	SL1	SL0	X0	X1	X2	X3	X4	X5	X6	X7
L	L	L	A0	A1	A2	A3	A4	A5	A6	A7
L	L	H	A1	A2	A3	A4	A5	A6	A7	A0
L	H	L	A2	A3	A4	A5	A6	A7	A0	A1
L	H	H	A3	A4	A5	A6	A7	A0	A1	A2
H	L	L	A4	A5	A6	A7	A0	A1	A2	A3
H	L	H	A5	A6	A7	A0	A1	A2	A3	A4
H	H	L	A6	A7	A0	A1	A2	A3	A4	A5
H	H	H	A7	A0	A1	A2	A3	A4	A5	A6



CMOS SWITCHING CHARACTERISTICS

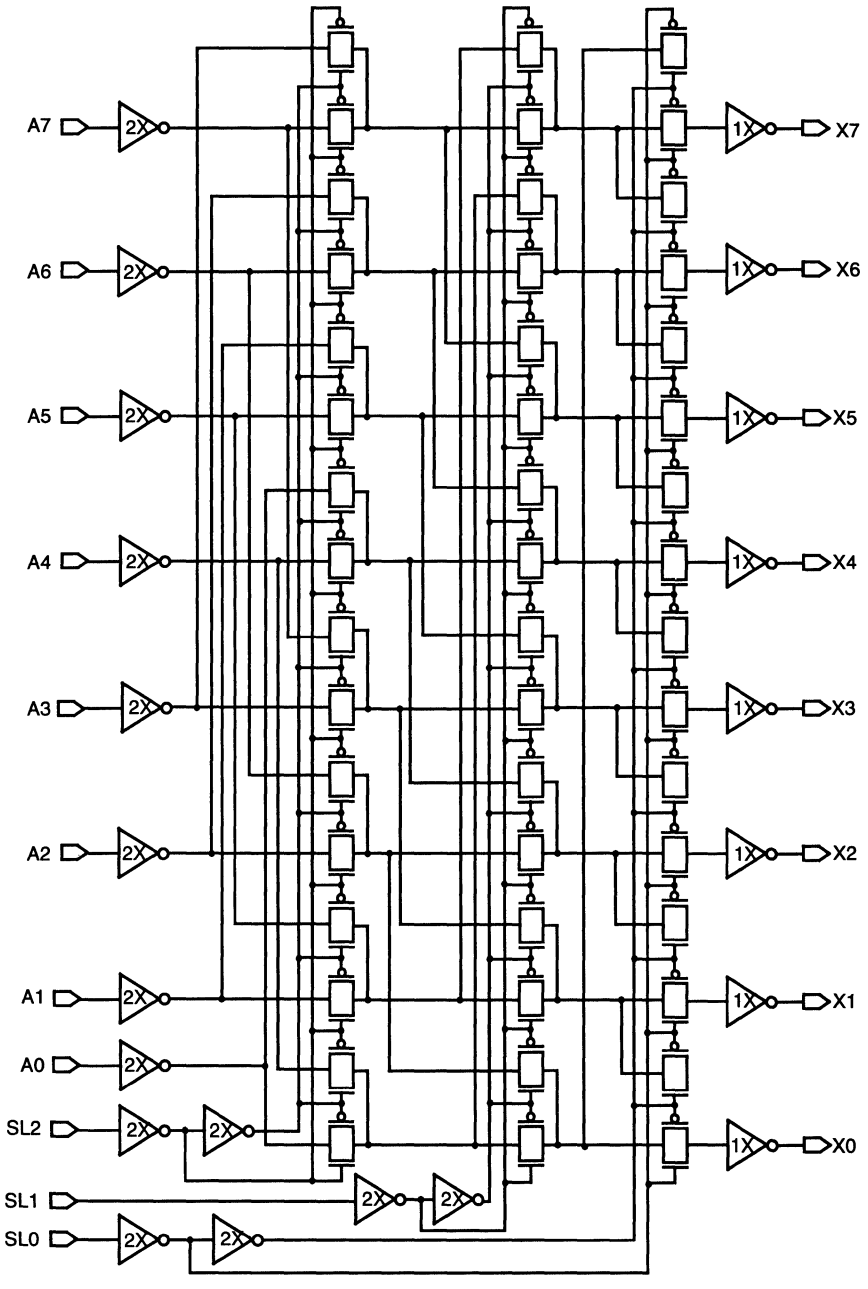
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	ROT8A								
t_{PLH}	Propagation Delay, A0-A7 to X0-X7	0.88	0.97	1.22	0.85	1.23	1.35	1.71	1.20
t_{PHL}		0.88	0.97	1.24	0.91	1.42	1.54	1.90	1.19
t_{PLH}	Propagation Delay, SL0 to X0-X7	0.92	1.01	1.26	0.85	1.29	1.41	1.77	1.20
t_{PHL}		0.91	1.00	1.26	0.86	1.38	1.49	1.81	1.09
t_{PLH}	Propagation Delay, SL1 to X0-X7	1.21	1.30	1.55	0.85	1.69	1.81	2.17	1.21
t_{PHL}		1.21	1.30	1.57	0.90	1.90	2.01	2.37	1.17
t_{PLH}	Propagation Delay, SL2 to X0-X7	1.32	1.40	1.66	0.85	1.88	2.00	2.36	1.20
t_{PHL}		1.38	1.47	1.75	0.91	2.16	2.27	2.63	1.18
t_r	Output Rise Time, X0-X7	0.28	0.52	1.24	2.40	0.35	0.70	1.72	3.41
t_f	Output Fall Time, X0-X7	0.45	0.57	0.93	1.20	0.69	0.83	1.28	1.49

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: ROT8A



8-Bit Shift Register with Positive Edge Triggered Clock (3.3 V and 5 V Core Voltage)

SHIFT8

MACRO	EQUIV. GATES
SHIFT8	45

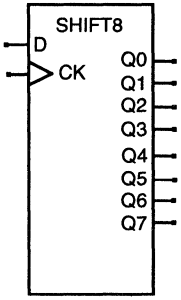
Rev. 1.07

MACRO	OUTPUTS/INPUTS
SHIFT8	Q0-Q7 / D,CK

MACRO	INPUT CAP.
SHIFT8	CK: 0.15pF D: 0.05pF

FUNCTION TABLE

D	CK	Q0	Q1	Q2....	...Q7
L	↓	L	Q0	Q1	Q6
H	↓	H	Q0	Q1	Q6



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
ROT8A									
t_{PLH}	Propagation Delay,	1.16	1.24	1.49	0.83	1.55	1.67	2.02	1.16
t_{PHL}	CK to Q0-Q7	1.37	1.44	1.67	0.77	1.94	2.03	2.31	0.93
t_r	Output Rise Time, Q0-Q7	0.14	0.38	1.12	2.44	0.21	0.55	1.58	3.44
t_f	Output Fall Time, Q0-Q7	0.17	0.29	0.64	1.16	0.23	0.37	0.79	1.40

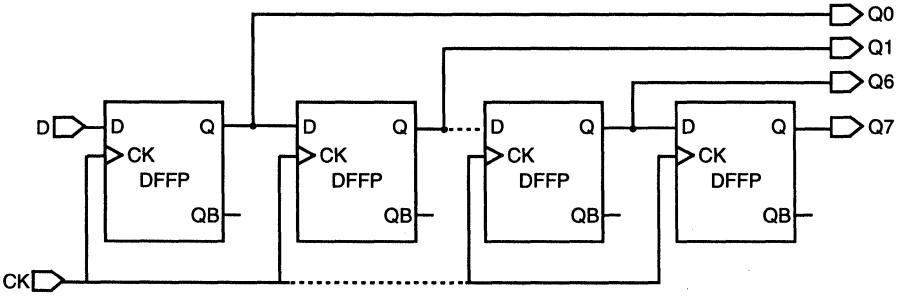
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V Minimum Requirement	3.3V Minimum Requirement
SHIFT8			
t_{su}	Set Up Time, D to CK	0.05	0.18
t_h	Hold Time, CK to D	0.70	0.96
t_w	Pulse Width, CK(L)	0.84	1.33
t_w	Pulse Width, CK(H)	0.93	1.35

FUNCTIONAL DIAGRAM: SHIFT8



D-Type Latch with Scan into a D-Type 2X Drive (3.3 V and 5 V Core Voltage)

SRLSSD1H

MACRO	EQUIV. GATES
SRLSSD1H	13

Rev. 1.07

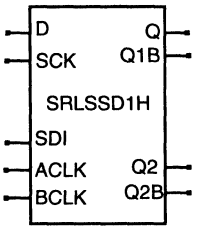
MACRO	OUTPUTS/INPUTS
SRLSSD1H	Q1,Q1B,Q2,Q2B / D,SCLK,SDI,ACLK,BCLK

MACRO	INPUT CAP.
SRLSSD1H	ACLK,SCLK: 0.09pF BCLK,D,SDI: 0.05pF

FUNCTION TABLE

D	SCLK	SDI	ACLK	Q1	Q1B	MODE
L	H	X	L	L	H	NORMAL
H	H	X	L	H	L	NORMAL
X	L	L	H	L	H	SCAN
X	L	H	H	H	L	SCAN
X	L	X	L	Q1	Q1B	NOR/SCAN
H	H	X	H	H	L	-
X	H	H	H	H	L	-
L	H	L	H	L	H	-

BCLK	Q1	Q2	Q2B
L	X	Q2	Q2B
H	L	L	H
H	H	H	L



CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	SRLSSD1H								
t_{PLH}	Propagation Delay, ACLK,D,SCLK,SDI to Q1	0.90	0.95	1.08	0.45	1.21	1.27	1.46	0.64
t_{PHL}		1.11	1.17	1.33	0.55	1.76	1.84	2.06	0.73
t_{PLH}	Propagation Delay, ACLK,SCLK to Q1B	1.63	1.68	1.81	0.43	2.44	2.50	2.69	0.62
t_{PHL}		1.31	1.35	1.49	0.44	1.83	1.89	2.06	0.57
t_{PLH}	Propagation Delay, ACLK,SCLK to Q2	1.76	1.80	1.92	0.41	2.46	2.52	2.70	0.59
t_{PHL}		2.04	2.08	2.20	0.40	3.08	3.13	3.28	0.50
t_{PLH}	Propagation Delay, ACLK,SCLK to Q2B	2.22	2.26	2.39	0.41	3.28	3.34	3.52	0.59
t_{PHL}		1.91	1.95	2.06	0.39	2.71	2.76	2.91	0.49
t_{PLH}	Propagation Delay, BCLK to Q2	0.82	0.86	0.99	0.42	0.69	0.73	0.84	0.38
t_{PHL}		0.89	0.93	1.05	0.41	1.49	1.54	1.69	0.50
t_{PLH}	Propagation Delay, BCLK to Q2B	1.10	1.15	1.27	0.42	1.57	1.63	1.81	0.58
t_{PHL}		1.10	1.14	1.26	0.39	1.56	1.60	1.75	0.49
t_{PLH}	Propagation Delay, D,SDI to Q1B	1.65	1.70	1.82	0.43	2.51	2.57	2.76	0.61
t_{PHL}		1.44	1.49	1.62	0.45	2.01	2.07	2.24	0.57
t_{PLH}	Propagation Delay, D,SDI to Q2	1.77	1.81	1.94	0.41	2.48	2.54	2.72	0.59
t_{PHL}		2.02	2.06	2.18	0.41	3.05	3.10	3.25	0.50
t_{PLH}	Propagation Delay, D,SDI to Q2B	2.24	2.28	2.40	0.41	3.35	3.40	3.58	0.58
t_{PHL}		2.06	2.10	2.21	0.39	2.89	2.94	3.09	0.49
t_r	Output Rise Time, Q1	0.31	0.43	0.78	1.17	0.35	0.52	1.02	1.68
t_f	Output Fall Time, Q1	0.52	0.58	0.76	0.60	0.67	0.74	0.97	0.77
t_r	Output Rise Time, Q1B	0.28	0.40	0.75	1.17	0.34	0.51	1.00	1.65
t_f	Output Fall Time, Q1B	0.31	0.36	0.53	0.56	0.37	0.44	0.65	0.70
t_r	Output Rise Time, Q2	0.15	0.27	0.63	1.19	0.23	0.40	0.90	1.68
t_f	Output Fall Time, Q2	0.19	0.25	0.42	0.56	0.26	0.32	0.53	0.68
t_r	Output Rise Time, Q2B	0.15	0.27	0.63	1.19	0.20	0.37	0.88	1.71
t_f	Output Fall Time, Q2B	0.19	0.25	0.42	0.56	0.24	0.31	0.52	0.69

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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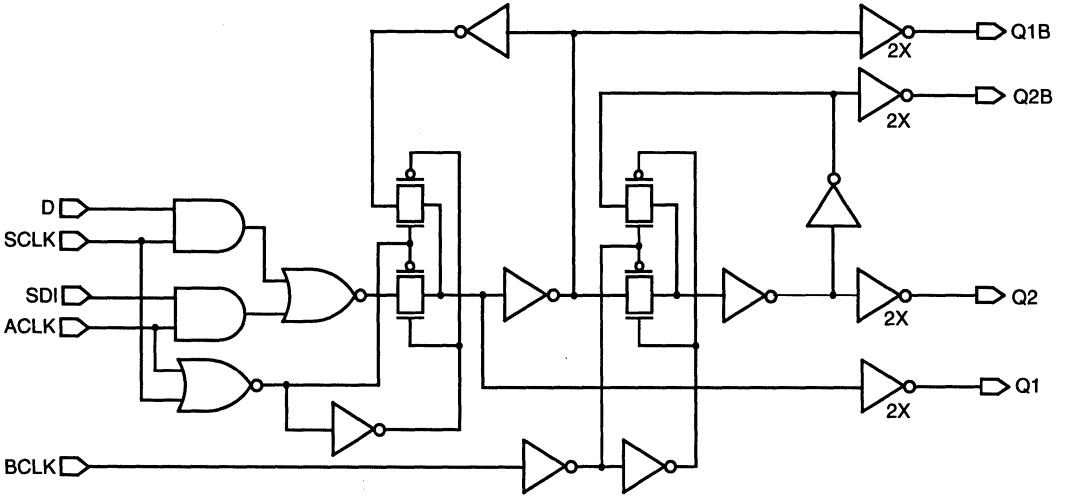
CMOS TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V Minimum Requirement	3.3V Minimum Requirement
	SRLSSD1H		
t_{su}	Set Up Time, SCLK to ACLK	1.54	2.29
t_{su}	Set Up Time, SDI to ACLK	1.58	2.34
t_{su}	Set Up Time, ACLK,SCLK to BCLK	1.99	2.82
t_{su}	Set Up Time, D,SDI to BCLK	2.01	3.01
t_{su}	Set Up Time, ACLK to SCLK	1.57	2.35
t_{su}	Set Up Time, D to SCLK	1.62	2.42
t_h	Hold Time, ACLK to SCLK	-0.19	-0.12
t_h	Hold Time, ACLK to SDI	-0.16	-0.12
t_h	Hold Time, BCLK to ACLK	-0.92	-1.20
t_h	Hold Time, BCLK to D,SDI	-0.79	-1.06
t_h	Hold Time, BCLK to SCLK	-0.89	-1.12
t_h	Hold Time, SCLK to ACLK	-0.24	-0.29
t_h	Hold Time, SCLK to D	-0.19	-0.22
t_w	Pulse Width, ACLK,SCLK(H)	1.32	2.06
t_w	Pulse Width, BCLK(L)	0.02	0.05
t_w	Pulse Width, BCLK(H)	0.80	1.11

FUNCTIONAL DIAGRAM: SRLSSD1H



Non-Inverting 3-State Buffer, Active Low Enable 1X & 2X Drive (3.3 V and 5 V Core Voltage)

TBUF
TBUFH

MACRO	EQUIV. GATES
TBUF	4
TBUFH	5

Rev. 1.07

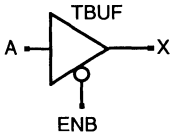
MACRO	OUTPUTS/INPUTS
All	X / A,ENB

MACRO	INPUT CAP.
All	A,ENB: 0.09pF

MACRO	OUTPUT CAP.
TBUF	X: 0.07pF
TBUFH	X: 0.11pF

FUNCTION TABLE

A	ENB	X
L	L	L
H	L	H
X	H	Z



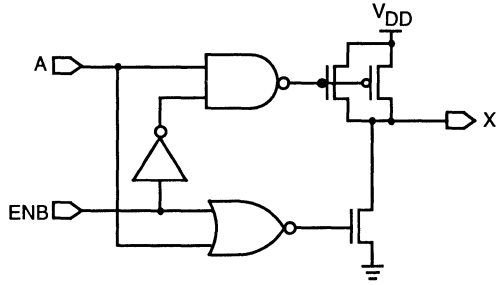
CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

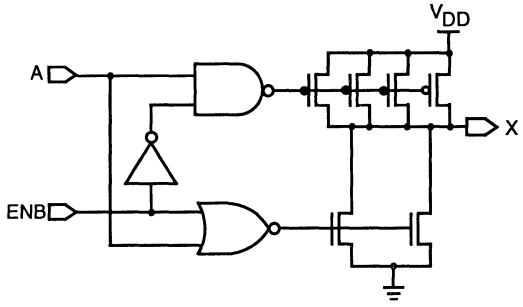
Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
TBUF									
t_{PLH}	Propagation Delay, A to X	0.32	0.36	0.49	0.42	0.44	0.50	0.67	0.59
t_{PHL}		0.36	0.44	0.67	0.77	0.52	0.61	0.89	0.93
t_{PLZ}	Propagation Delay, ENB to X	0.25	0.25	0.25	0.00	0.33	0.33	0.33	0.00
t_{PZL}		0.84	0.92	1.15	0.78	1.01	1.10	1.38	0.94
t_{PZH}	Propagation Delay, ENB to X	0.63	0.67	0.80	0.43	0.85	0.91	1.08	0.59
t_{PHZ}		0.85	0.85	0.85	0.00	1.03	1.03	1.03	0.00
t_r	Output Rise Time, X	0.18	0.29	0.65	1.17	0.17	0.34	0.85	1.70
t_f	Output Fall Time, X	0.17	0.29	0.64	1.16	0.22	0.37	0.79	1.41
TBUFH									
t_{PLH}	Propagation Delay, A to X	0.35	0.37	0.44	0.23	0.49	0.52	0.61	0.32
t_{PHL}		0.40	0.44	0.56	0.40	0.56	0.61	0.76	0.50
t_{PLZ}	Propagation Delay, ENB to X	0.30	0.30	0.30	0.00	0.40	0.40	0.40	0.00
t_{PZL}		0.85	0.89	1.02	0.42	1.04	1.09	1.24	0.51
t_{PZH}	Propagation Delay, ENB to X	0.64	0.66	0.73	0.24	0.89	0.92	1.01	0.32
t_{PHZ}		0.99	0.99	0.99	0.00	1.21	1.21	1.21	0.00
t_r	Output Rise Time, X	0.19	0.25	0.42	0.56	0.21	0.29	0.54	0.82
t_f	Output Fall Time, X	0.20	0.25	0.42	0.56	0.25	0.32	0.53	0.68

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

FUNCTIONAL DIAGRAM: TBUF



FUNCTIONAL DIAGRAM: TBUFH



Non-Inverting 3-State Buffer, Active High Enable 1X & 2X Drive (3.3 V and 5 V Core Voltage)

TBUFP TBUFPH

MACRO	EQUIV. GATES
TBUFP	4
TBUFPH	5

Rev. 1.07

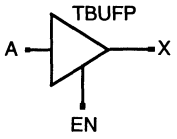
MACRO	OUTPUTS/INPUTS
All	X / A,EN

MACRO	INPUT CAP.
All	A,EN: 0.09pF

MACRO	OUTPUT CAP.
TBUFP	X: 0.09pF
TBUFPH	X: 0.17pF

FUNCTION TABLE

A	EN	X
L	H	L
H	H	H
X	L	Z



CMOS SWITCHING CHARACTERISTICS

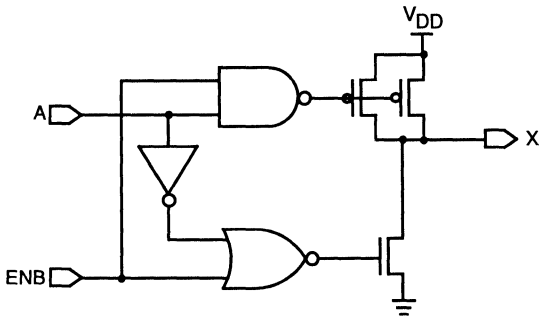
(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
TBUFP									
t_{PLH}	Propagation Delay, A to X	0.33	0.37	0.50	0.42	0.46	0.52	0.69	0.59
t_{PHL}		0.37	0.45	0.68	0.77	0.53	0.63	0.90	0.93
t_{PLZ}	Propagation Delay, EN to X	0.37	0.37	0.37	0.00	0.51	0.51	0.51	0.00
t_{PZL}		0.50	0.58	0.81	0.77	0.70	0.79	1.07	0.94
t_{PZH}	Propagation Delay, EN to X	0.32	0.36	0.49	0.42	0.45	0.51	0.69	0.59
t_{PHZ}		0.46	0.46	0.46	0.00	0.60	0.60	0.60	0.00
t_r	Output Rise Time, X	0.18	0.30	0.65	1.17	0.16	0.33	0.85	1.71
t_f	Output Fall Time, X	0.18	0.30	0.64	1.16	0.23	0.37	0.79	1.41
TBUFPH									
t_{PLH}	Propagation Delay, A to X	0.37	0.40	0.47	0.23	0.52	0.55	0.64	0.32
t_{PHL}		0.42	0.46	0.58	0.40	0.60	0.65	0.79	0.50
t_{PLZ}	Propagation Delay, EN to X	0.40	0.40	0.40	0.00	0.56	0.56	0.56	0.00
t_{PZL}		0.53	0.57	0.69	0.41	0.76	0.81	0.96	0.51
t_{PZH}	Propagation Delay, EN to X	0.35	0.37	0.44	0.23	0.51	0.54	0.64	0.32
t_{PHZ}		0.60	0.60	0.60	0.00	0.79	0.79	0.79	0.00
t_r	Output Rise Time, X	0.19	0.25	0.42	0.57	0.22	0.31	0.56	0.83
t_f	Output Fall Time, X	0.22	0.27	0.44	0.56	0.26	0.33	0.54	0.69

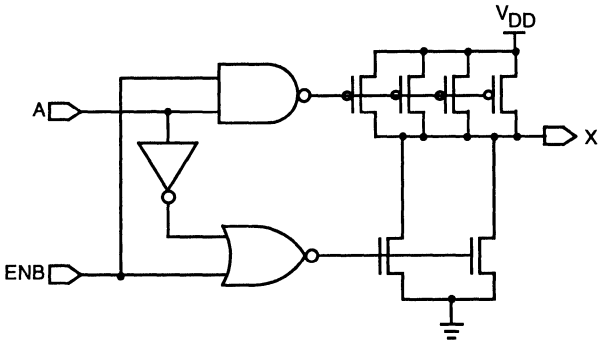
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

FUNCTIONAL DIAGRAM: TBUFP



FUNCTIONAL DIAGRAM: TBUFPH



7

Section 7.5 Metalized RAMs

Low Power Single Port RAM

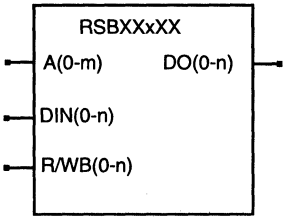
RSBXXxXX

MACRO	EQUIV. GATES
RSBXXxXX	see table below

Rev. 1.07

INPUTS	A(0-m),DIN(0-n),R/WB(0-n)
OUTPUTS	DO(0-n)

SIGNAL NAME	INPUT CAP.
A(0-m)	see table below
DIN(0-n)	0.1 pF
R/WB(0-n)	0.1 pF



Size, Address Line Input Capacitance, and Array Availability Information for Single Port RAM's

Size (Words X Bits)	Name	Size (Columns X Rows)	Total Gate Count	Input Capacitance Per Address Line
8-WORD BLOCK				
8X8	RSB8X8	20X11	198	0.1 pF
8X18	RSB8X18	20X11	440	
16-WORD BLOCK				
16X8	RSB16X8	20X19	342	0.1 pF
16X18	RSB16X18	20X19	760	
16X36	RSB16X36	38X19	1444	
32-WORD BLOCK				
32X8	RSB32X8	9X35	630	0.15pF
32X18	RSB32X18	20X35	1400	
32X36	RSB32X36	38X35	2660	
64-WORD BLOCK				
64X18	RSB64X18	20X67	2680	0.20 pF
64X36	RSB64X36	38X67	5092	

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
RSB8X8									
t_{PLH}	Propagation Delay, A0-A2 to DO0-DO7	2.44	2.50	2.69	0.62	3.39	3.50	3.83	1.09
t_{PHL}		2.35	2.41	2.57	0.54	3.73	3.84	4.18	1.13
t_{PLH}	Propagation Delay, DIN0-DIN7 to DO0-DO7	0.97	1.04	1.26	0.72	1.25	1.35	1.67	1.06
t_{PHL}		1.30	1.34	1.45	0.37	1.93	1.98	2.16	0.58
t_{PLH}	Propagation Delay, RWB0-RWB7 to DO0-DO7	1.09	1.17	1.38	0.72	1.33	1.42	1.68	0.88
t_{PHL}		1.30	1.34	1.44	0.35	1.87	1.94	2.16	0.71
t_r	Output Rise Time, DO0-DO7	0.73	0.84	1.15	1.04	1.09	1.26	1.76	1.67

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_f	Output Fall Time, DO0-DO7	0.78	0.85	1.05	0.67	0.91	1.06	1.49	1.44
	RSB8X18								
t_{PLH}	Propagation Delay,	2.59	2.65	2.82	0.58	3.79	3.88	4.17	0.96
t_{PHL}	A0-A2 to DO0-DO17	2.49	2.55	2.73	0.58	4.40	4.49	4.76	0.91
t_{PLH}	Propagation Delay,	0.97	1.04	1.26	0.72	1.25	1.36	1.67	1.06
t_{PHL}	DIN0-DIN17 to DO0-DO17	1.30	1.34	1.45	0.37	1.93	1.98	2.16	0.58
t_{PLH}	Propagation Delay,	1.10	1.17	1.38	0.72	1.33	1.42	1.68	0.88
t_{PHL}	RWB0-RWB17 to DO0-DO17	1.30	1.34	1.44	0.35	1.90	1.97	2.15	0.63
t_r	Output Rise Time, DO0-DO17	0.73	0.83	1.14	1.03	1.51	1.61	1.93	1.05
t_f	Output Fall Time, DO0-DO17	0.74	0.81	1.03	0.74	1.47	1.56	1.80	0.81

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	RSB16X8								
t_{PLH}	Propagation Delay,	2.99	3.05	3.24	0.62	4.28	4.37	4.63	0.89
t_{PHL}	A0-A3 to DO0-DO7	2.75	2.80	2.96	0.52	4.39	4.48	4.77	0.96
t_{PLH}	Propagation Delay,	1.09	1.17	1.40	0.76	1.42	1.53	1.84	1.05
t_{PHL}	DIN0-DIN17 to DO0-DO7	1.41	1.45	1.55	0.35	2.14	2.20	2.39	0.64
t_{PLH}	Propagation Delay,	1.27	1.33	1.51	0.61	1.41	1.51	1.82	1.02
t_{PHL}	RWB0-RWB7 to DO0-DO7	1.45	1.48	1.59	0.36	2.23	2.30	2.49	0.66
t_r	Output Rise Time, DO0-DO7	0.88	0.99	1.31	1.06	1.49	1.62	1.99	1.24
t_f	Output Fall Time, DO0-DO7	0.80	0.87	1.07	0.69	1.22	1.37	1.79	1.42
	RSB16X18								
t_{PLH}	Propagation Delay,	3.02	3.09	3.29	0.67	4.40	4.49	4.77	0.92
t_{PHL}	A0-A3 to DO0-DO17	2.83	2.88	3.06	0.57	4.71	4.80	5.08	0.94
t_{PLH}	Propagation Delay,	1.09	1.17	1.40	0.76	1.42	1.53	1.84	1.05
t_{PHL}	DIN0-DIN17 to DO0-DO17	1.41	1.45	1.55	0.35	2.14	2.20	2.39	0.64
t_{PLH}	Propagation Delay,	1.27	1.33	1.51	0.61	1.41	1.51	1.82	1.02
t_{PHL}	RWB0-RWB17 to DO0-DO17	1.47	1.50	1.59	0.30	2.23	2.30	2.50	0.65
t_r	Output Rise Time, DO0-DO17	0.81	0.93	1.29	1.20	1.37	1.50	1.90	1.34
t_f	Output Fall Time, DO0-DO17	0.83	0.90	1.11	0.69	1.27	1.41	1.83	1.42
	RSB16X36								
t_{PLH}	Propagation Delay,	3.31	3.37	3.56	0.64	4.73	4.82	5.10	0.92
t_{PHL}	A0-A3 to DO0-DO35	3.16	3.21	3.38	0.55	5.07	5.16	5.43	0.89
t_{PLH}	Propagation Delay,	1.09	1.17	1.40	0.76	1.42	1.53	1.84	1.05
t_{PHL}	DIN0-DIN35 to DO0-DO35	1.41	1.45	1.55	0.36	2.14	2.20	2.39	0.64
t_{PLH}	Propagation Delay,	1.27	1.33	1.51	0.61	1.39	1.49	1.80	1.02
t_{PHL}	RWB0-RWB35 to DO0-DO35	1.45	1.48	1.59	0.36	2.21	2.28	2.47	0.65
t_r	Output Rise Time, DO0-DO35	0.98	1.08	1.38	0.99	1.46	1.59	1.95	1.20
t_f	Output Fall Time, DO0-DO35	0.83	0.90	1.11	0.69	1.23	1.38	1.81	1.46

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
RSB32X8									
t_{PLH}	Propagation Delay, A0-A3 to DO0-DO7	3.72	3.79	3.99	0.68	5.18	5.31	5.68	1.24
t_{PHL}		3.30	3.36	3.54	0.59	5.42	5.52	5.82	0.99
t_{PLH}	Propagation Delay, DIN0-DIN17 to DO0-DO7	1.30	1.38	1.61	0.76	1.66	1.77	2.10	1.12
t_{PHL}		1.76	1.80	1.92	0.40	2.56	2.64	2.87	0.77
t_{PLH}	Propagation Delay, RWB0-RWB7 to DO0-DO17	1.44	1.51	1.74	0.76	1.73	1.84	2.18	1.11
t_{PHL}		1.84	1.86	1.92	0.22	2.59	2.66	2.87	0.69
t_r	Output Rise Time, DO0-DO7	0.69	0.84	1.28	1.47	1.92	2.08	2.57	1.62
t_f	Output Fall Time, DO0-DO7	0.94	1.02	1.25	0.76	1.44	1.55	1.89	1.14
RSB32X18									
t_{PLH}	Propagation Delay, A0-A3 to DO0-DO17	3.70	3.78	4.03	0.82	4.97	5.11	5.52	1.37
t_{PHL}		3.39	3.45	3.64	0.62	5.33	5.44	5.78	1.11
t_{PLH}	Propagation Delay, DIN0-DIN17 to DO0-DO17	1.31	1.38	1.61	0.76	1.66	1.77	2.10	1.12
t_{PHL}		1.76	1.80	1.92	0.40	2.56	2.64	2.87	0.78
t_{PLH}	Propagation Delay, RWB0-RWB17 to DO0-DO17	1.46	1.53	1.76	0.76	1.73	1.84	2.18	1.11
t_{PHL}		1.56	1.61	1.78	0.56	2.60	2.67	2.87	0.69
t_r	Output Rise Time, DO0-DO17	1.34	1.43	1.70	0.90	1.94	2.12	2.64	1.74
t_f	Output Fall Time, DO0-DO17	0.92	1.00	1.24	0.80	1.94	2.04	2.31	0.91
RSB32X36									
t_{PLH}	Propagation Delay, A0-A3 to DO0-DO35	4.01	4.08	4.29	0.69	5.44	5.55	5.89	1.12
t_{PHL}		3.37	3.44	3.65	0.70	5.58	5.69	6.03	1.13
t_{PLH}	Propagation Delay, DIN0-DIN35 to DO0-DO35	1.31	1.38	1.61	0.76	1.66	1.77	2.10	1.11
t_{PHL}		1.76	1.80	1.92	0.40	2.56	2.64	2.87	0.78
t_{PLH}	Propagation Delay, RWB0-RWB35 to DO0-DO35	1.42	1.50	1.72	0.76	1.73	1.84	2.18	1.12
t_{PHL}		1.76	1.80	1.92	0.39	2.59	2.66	2.87	0.69
t_r	Output Rise Time, DO0-DO35	1.51	1.60	1.86	0.87	1.92	2.07	2.52	1.50
t_f	Output Fall Time, DO0-DO35	1.24	1.29	1.46	0.56	1.41	1.53	1.90	1.20

Capacitance per fanout = 0.06 pF (metal capacitance is not included).

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CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
RSB64X18									
t_{PLH}	Propagation Delay, A0-A3 to DO0-DO17	5.46	5.59	5.95	1.22	8.51	8.62	8.93	1.04
t_{PHL}		5.30	5.38	5.60	0.75	9.00	9.11	9.43	1.07
t_{PLH}	Propagation Delay, DIN0-DIN17 to DO0-DO17	1.81	1.90	2.17	0.91	2.20	2.32	2.69	1.25
t_{PHL}		2.31	2.35	2.50	0.48	3.60	3.68	3.91	0.76
t_{PLH}	Propagation Delay, RWB0-RWB17 to DO0-DO17	1.89	1.99	2.27	0.94	2.19	2.31	2.67	1.20
t_{PHL}		2.38	2.42	2.55	0.44	3.62	3.70	3.93	0.76
t_r	Output Rise Time, DO0-DO17	2.92	3.00	3.26	0.85	3.42	3.59	4.09	1.67
t_f	Output Fall Time, DO0-DO17	1.65	1.77	2.14	1.24	2.98	3.08	3.37	0.97

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		RSB64X36							
t_{PLH}	Propagation Delay, A0-A3 to DO0-DO35	5.92	6.00	6.24	0.79	8.51	8.62	8.93	1.04
t_{PHL}		5.51	5.57	5.76	0.62	9.00	9.11	9.43	1.07
t_{PLH}	Propagation Delay, DIN0-DIN35 to DO0-DO35	1.83	1.91	2.17	0.86	2.20	2.32	2.69	1.25
t_{PHL}		2.31	2.35	2.50	0.48	3.60	3.68	3.91	0.76
t_{PLH}	Propagation Delay, RWB0-RWB35 to DO0-DO35	1.89	1.99	2.27	0.94	2.19	2.31	2.67	1.20
t_{PHL}		2.38	2.42	2.55	0.43	3.62	3.70	3.93	0.76
t_r	Output Rise Time, DO0-DO35	1.61	1.71	2.03	1.05	3.42	3.59	4.09	1.67
t_f	Output Fall Time, DO0-DO35	1.69	1.79	2.07	0.95	2.98	3.08	3.37	0.97

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Abbr.	Parameter		8-WORD BLOCK		16-WORD BLOCK		32-WORD BLOCK		64-WORD BLOCK	
			5 V	3.3 V	5 V	3.3 V	5 V	3.3 V	5 V	3.3 V
t_{DSU}	Set Up Time,	DIN(n) to R/WB (WL = 8)	1.54	2.15	1.73	2.47	2.04	2.99	-	-
		DIN(n) to R/WB (WL = 18)	1.54	1.84	1.73	2.71	2.04	2.91	2.96	4.16
		DIN(n) to R/WB (WL = 36)	-	-	1.51	2.71	2.04	2.91	3.00	4.16
t_{AWB}	Set Up Time,	A to R/WB (WL = 8)	0.38	0.50	0.57	0.69	0.72	0.93	-	-
		A to R/WB (WL = 18)	0.35	0.64	0.50	0.90	0.60	0.89	0.85	1.23
		A to R/WB (WL = 36)		-	1.51	1.83	1.62	1.89	2.26	1.23
t_{ASU}	Set Up Time,	A to R/WB (WL = 8)	3.80	5.82	5.15	7.11	4.81	7.70	-	-
		A to R/WB (WL = 18)	5.04	6.77	5.26	7.14	5.65	8.42	7.56	11.73
		A to R/WB (WL = 36)	-	-	5.22	7.09	4.76	6.93	9.35	11.73
t_{DH}	Hold Time,	R/WB to DIN(n)	0.18	0.28	0.22	0.20	0.22	0.16	0.19	-0.01
t_{WP}	Pulse Width	R/WB (L,H) (WL = 8)	1.88	2.63	2.10	2.97	2.76	3.58	-	-
		R/WB (L,H) (WL = 18)	1.97	2.66	2.18	3.01	2.59	3.28	3.49	-0.01
		R/WB (L,H) (WL = 36)	-	-	2.16	3.02	2.71	3.79	3.32	-0.01
t_{AH}	Hold Time,	R/WB to A (WL = 8)	0.09	0.02	0.08	0.07	0.06	0.05	-	-
		R/WB to A (WL = 18)	0.09	0.04	0.05	0.03	0.07	0.09	0.10	0.05
		R/WB to A (WL = 36)	-	-	0.07	0.05	0.07	0.06	0.14	0.05

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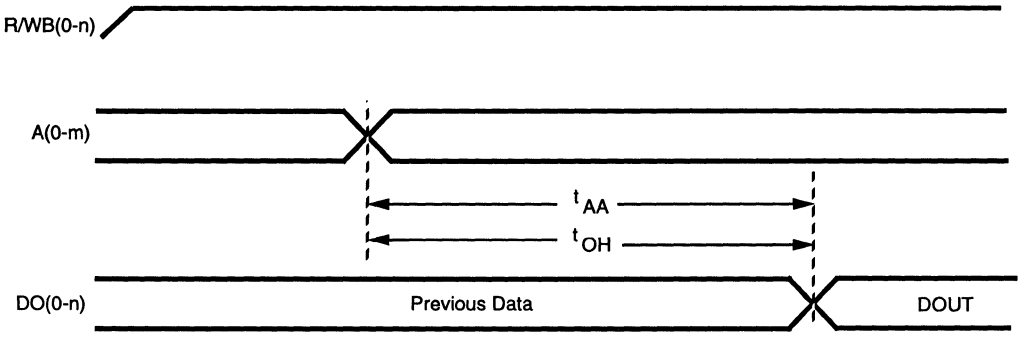
TIMING DIAGRAM: READ CYCLE Low Power Single Port RAM

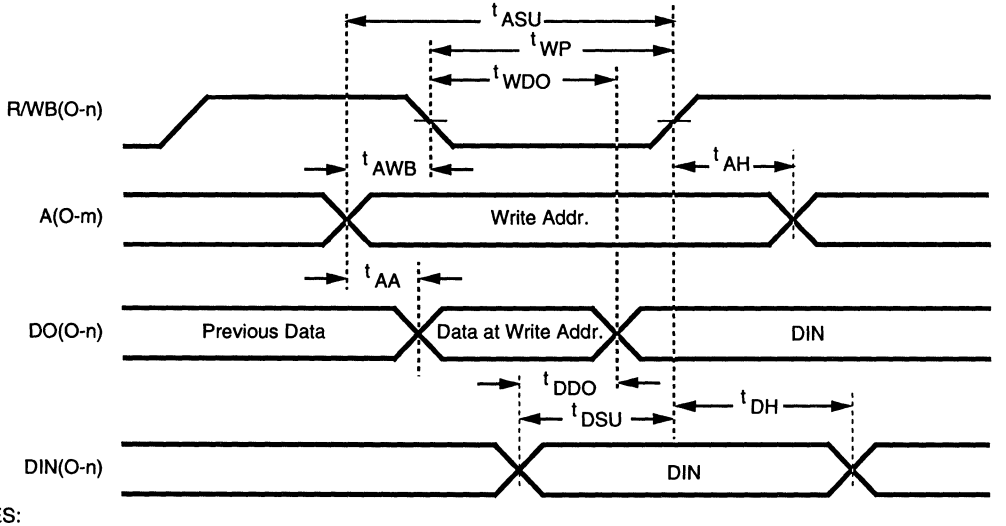


NOTES:
1. R/WB remains high throughout Read Cycles.

2. The OUTPUT HOLD TIME, t_{OH},will be the same as t_{AA} due to internal switching speed and internal loading.

3.Since Address, A(m), is not latched internally, the Data-Out Bus, DO(n), will always reflect the contents of memory selected by the current Address following time period t_{AA}

WRITE CYCLE Low Power Single Port RAM

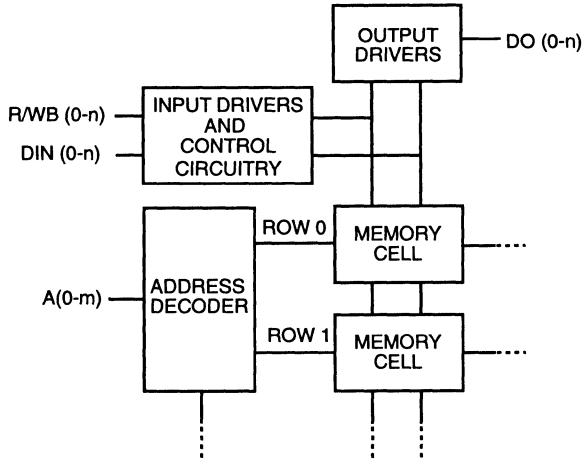


NOTES:
1. For a Write Operation, Address must remain stable for the contiguous period consisting of time periods t_{AWB}, t_{WP} and t_{AH}.
2. Since Address, A(m), is not latched internally, the Data-Out Bus, DO(n), will always reflect the contents of memory selected by the current Address following time period t_{AA}.

3. When in the Write Mode, defined by R/WB being low, DO(n) will reflect the Data value of DIN(n) following time periods t_{WDO} and t_{DDO}, whichever occurs later.

4. Write occurs on the rising edge of R/WB, at which time the Data, appearing on both DIN(n) and DO(n) is written to the Address location.

FUNCTIONAL DIAGRAM:
Low Power Single Port RAM



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High Speed Dual Port RAM

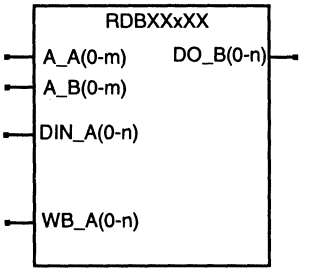
RDBXXxXX

MACRO	EQUIV. GATES
RDBXXxXX	see table below

Rev. 1.07

INPUTS	AA(0-m),AB(0-m), DINA(0-n),WBA
OUTPUTS	DOB(0-n)

SIGNAL NAME	INPUT CAP.
AA(0-m)	see table below
AB(0-m)	see table below
DINA(0-n)	0.05 pF
WBA	see table below



Size, Address Line Input Capacitance, and Array Availability Information for Dual Port RAM's

Size (Words X Bits)	Name	Size (Columns X Rows)	Total Gate Count	Port A Input Capacitance Per Address Line	Port A Input Capacitance WB_A Line	Port B Input Capacitance Per Address Line
8-WORD BLOCK						
8X9	RDB8X9	13X14	356	0.15 pF	0.15 pF	0.15 pF
8X18	RDB8X18	22X14	608			
8X36	RDB8X36	40X14	1112			
8X72	RDB8X72	77X14	2156			
16-WORD BLOCK						
16X9	RDB16X9	14X26	725	AA0-AA1= 0.20 pF AA2-AA3= 0.09pF	0.20 pF	0.20 pF
16X18	RDB16X18	23X26	1193			
16X36	RDB16X36	41X26	2129			
16X72	RDB16X72	78X26	4050			
32-WORD BLOCK						
32X9	RDB32X9	14X50	1400	AA0-AA1= 0.25 pF AA2-AA3=0.09pF AA4=0.20 pF	0.20 pF	AB0-AB1= 0.25 pF AB2-AB3=0.09pF AB4=0.20 pF
32X18	RDB32X18	23X50	2300			
32X36	RDB32X36	41X50	4100			
32X72	RDB32X72	78X50	7798			

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
RDB8X9									
t_{PLH}	Propagation Delay, A0-A2 to DO0-DO8	1.75	1.83	2.07	0.81	2.67	2.79	3.14	1.20
t_{PHL}		1.92	1.99	2.20	0.68	2.94	3.02	3.25	0.77
t_{PLH}	Propagation Delay, DIN0-DIN8 to DO0-DO8	1.47	1.55	1.80	0.81	2.51	2.63	2.98	1.17
t_{PHL}		2.11	2.18	2.39	0.70	3.03	3.12	3.38	0.87
t_{PLH}	Propagation Delay, RWB0-RWB8 to DO0-DO8	2.34	2.43	2.68	0.83	3.74	3.86	4.20	1.13
t_{PHL}		2.40	2.47	2.69	0.71	3.54	3.63	3.88	0.85
t_r	Output Rise Time, DO0-DO8	0.18	0.43	1.19	2.52	0.35	0.72	1.83	3.70
t_f	Output Fall Time, DO0-DO8	0.41	0.51	0.82	1.02	0.48	0.61	0.98	1.25

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
RDB8X18									
t_{PLH}	Propagation Delay, A0-A2 to DO0-DO17	1.84	1.93	2.17	0.82	2.92	3.04	3.39	1.18
t_{PHL}		2.07	2.14	2.35	0.70	2.99	3.08	3.34	0.88
t_{PLH}	Propagation Delay, DIN0-DIN17 to DO0-DO17	1.47	1.55	1.80	0.81	2.51	2.63	2.98	1.17
t_{PHL}		2.11	2.18	2.38	0.70	3.03	3.11	3.37	0.87
t_{PLH}	Propagation Delay, RWB0-RWB17 to DO0-DO17	2.48	2.56	2.81	0.82	3.99	4.11	4.46	1.16
t_{PHL}		2.64	2.70	2.89	0.63	3.77	3.85	4.09	0.80
t_r	Output Rise Time, DO0-DO17	0.18	0.43	1.19	2.52	0.40	0.75	1.82	3.56
t_f	Output Fall Time, DO0-DO17	0.66	0.75	1.00	0.84	0.42	0.56	0.99	1.43
RDB8X36									
t_{PLH}	Propagation Delay, A0-A2 to DO0-DO35	2.10	2.19	2.45	0.87	3.43	3.54	3.88	1.12
t_{PHL}		2.32	2.39	2.59	0.66	3.28	3.37	3.65	0.91
t_{PLH}	Propagation Delay, DIN0-DIN35 to DO0-DO35	1.47	1.56	1.80	0.81	2.51	2.63	2.98	1.17
t_{PHL}		2.11	2.18	2.39	0.70	3.03	3.11	3.37	0.87
t_{PLH}	Propagation Delay, RWB0-RWB35 to DO0-DO35	2.89	2.98	3.23	0.83	4.52	4.64	5.00	1.19
t_{PHL}		2.94	3.01	3.23	0.72	4.40	4.48	4.72	0.80
t_r	Output Rise Time, DO0-DO35	0.20	0.45	1.21	2.52	0.56	0.90	1.91	3.37
t_f	Output Fall Time, DO0-DO35	0.62	0.71	0.97	0.86	1.35	1.43	1.65	0.73
RDB8X72									
t_{PLH}	Propagation Delay, A0-A2 to DO0-DO71	2.28	2.36	2.61	0.84	3.82	3.93	4.26	1.11
t_{PHL}		2.62	2.69	2.88	0.65	3.72	3.80	4.04	0.80
t_{PLH}	Propagation Delay, DIN0-DIN71 to DO0-DO71	1.48	1.56	1.80	0.81	2.52	2.64	2.99	1.17
t_{PHL}		2.11	2.18	2.39	0.70	3.02	3.11	3.37	0.87
t_{PLH}	Propagation Delay, RWB0-RWB71 to DO0-DO71	3.44	3.52	3.76	0.81	5.38	5.49	5.83	1.12
t_{PHL}		3.47	3.53	3.73	0.66	4.79	4.87	5.11	0.80
t_r	Output Rise Time, DO0-DO71	0.37	0.61	1.31	2.33	0.67	0.97	1.87	3.00
t_f	Output Fall Time, DO0-DO71	0.65	0.73	1.00	0.89	0.82	0.93	1.25	1.07

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
RDB16X9									
t_{PLH}	Propagation Delay, A0-A3 to DO0-DO8	2.31	2.39	2.64	0.83	3.59	3.71	4.07	1.20
t_{PHL}		2.70	2.77	2.97	0.66	3.67	3.76	4.02	0.87
t_{PLH}	Propagation Delay, DIN0-DIN8 to DO0-DO8	1.89	1.98	2.23	0.83	3.33	3.45	3.81	1.20
t_{PHL}		2.91	2.98	3.19	0.69	4.06	4.16	4.43	0.91
t_{PLH}	Propagation Delay, RWB0-RWB8 to DO0-DO8	2.81	2.89	3.13	0.80	4.23	4.35	4.72	1.22
t_{PHL}		2.83	2.91	3.14	0.76	4.27	4.35	4.60	0.82
t_r	Output Rise Time, DO0-DO8	0.35	0.60	1.32	2.43	0.59	0.92	1.88	3.22
t_f	Output Fall Time, DO0-DO8	0.51	0.60	0.90	0.97	0.66	0.79	1.15	1.23
RDB16X18									
t_{PLH}	Propagation Delay, A0-A3 to DO0-DO18	2.42	2.50	2.75	0.83	3.82	3.93	4.27	1.14
t_{PHL}		2.74	2.81	3.03	0.73	3.78	3.88	4.17	0.98
t_{PLH}	Propagation Delay, DIN0-DIN18 to DO0-DO18	1.89	1.98	2.23	0.83	3.32	3.44	3.81	1.21
t_{PHL}		2.92	2.99	3.19	0.69	4.06	4.16	4.43	0.91
t_{PLH}	Propagation Delay, RWB0-RWB18 to DO0-DO18	2.87	2.95	3.19	0.81	4.60	4.72	5.07	1.18
t_{PHL}		3.03	3.10	3.30	0.66	4.39	4.48	4.74	0.87

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_r	Output Rise Time, DO0-DO17	0.42	0.66	1.39	2.43	0.48	0.83	1.89	3.53
t_f	Output Fall Time, DO0-DO17	0.58	0.69	0.99	1.01	0.93	1.04	1.37	1.10
	RDB16X36								
t_{PLH}	Propagation Delay, A0-A3 to DO0-DO35	2.65	2.74	2.99	0.85	4.18	4.30	4.64	1.16
t_{PHL}		3.06	3.12	3.32	0.66	4.24	4.33	4.58	0.84
t_{PLH}	Propagation Delay, DIN0-DIN35 to DO0-DO35	1.89	1.98	2.23	0.83	3.36	3.48	3.84	1.21
t_{PHL}		2.92	2.99	3.19	0.69	4.06	4.16	4.43	0.91
t_{PLH}	Propagation Delay, RWB0-RWB35 to DO0-DO35	3.30	3.38	3.62	0.80	5.22	5.33	5.67	1.14
t_{PHL}		3.36	3.43	3.64	0.70	4.94	5.03	5.30	0.88
t_r	Output Rise Time, DO0-DO35	0.19	0.44	1.22	2.57	0.53	0.85	1.84	3.28
t_f	Output Fall Time, DO0-DO35	0.35	0.46	0.81	1.14	1.33	1.42	1.67	0.83
	RDB16X72								
t_{PLH}	Propagation Delay, A0-A3 to DO0-DO71	3.04	3.12	3.37	0.81	4.63	4.75	5.11	1.18
t_{PHL}		3.06	3.15	3.43	0.91	4.78	4.86	5.11	0.81
t_{PLH}	Propagation Delay, DIN0-DIN71 to DO0-DO71	1.90	1.98	2.23	0.83	3.45	3.57	3.90	1.13
t_{PHL}		2.92	2.99	3.19	0.69	4.06	4.15	4.43	0.91
t_{PLH}	Propagation Delay, RWB0-RWB71 to DO0-DO71	3.59	3.68	3.93	0.85	5.70	5.82	6.19	1.20
t_{PHL}		3.68	3.75	3.97	0.74	5.20	5.28	5.54	0.85
t_r	Output Rise Time, DO0-DO71	0.35	0.59	1.34	2.47	1.00	1.29	2.17	2.93
t_f	Output Fall Time, DO0-DO71	1.22	1.27	1.42	0.52	1.36	1.43	1.64	0.69

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	RDB32X9								
t_{PLH}	Propagation Delay, A0-A4 to DO0-DO8	3.72	3.80	4.04	0.81	5.49	5.61	5.97	1.20
t_{PHL}		4.00	4.07	4.29	0.72	5.48	5.59	5.92	1.11
t_{PLH}	Propagation Delay, DIN0-DIN7 to DO0-DO8	3.00	3.08	3.32	0.81	5.02	5.14	5.50	1.21
t_{PHL}		4.05	4.14	4.44	0.98	5.82	5.91	6.18	0.88
t_{PLH}	Propagation Delay, RWB0-RWB8 to DO0-DO8	3.69	3.78	4.05	0.91	5.86	6.02	6.50	1.59
t_{PHL}		4.29	4.37	4.60	0.77	6.10	6.20	6.52	1.07
t_r	Output Rise Time, DO0-DO8	0.44	0.68	1.42	2.45	1.20	1.52	2.46	3.15
t_f	Output Fall Time, DO0-DO8	0.91	1.00	1.28	0.93	1.44	1.54	1.83	0.97
	RDB32X18								
t_{PLH}	Propagation Delay, A0-A4 to DO0-DO17	3.76	3.84	4.09	0.82	5.72	5.85	6.23	1.28
t_{PHL}		4.27	4.35	4.58	0.78	5.73	5.85	6.20	1.18
t_{PLH}	Propagation Delay, DIN0-DIN17 to DO0-DO17	3.00	3.08	3.32	0.81	5.02	5.14	5.50	1.21
t_{PHL}		4.05	4.14	4.44	0.98	5.82	5.91	6.18	0.88
t_{PLH}	Propagation Delay, RWB0-RWB17 to DO0-DO17	4.18	4.26	4.49	0.76	6.50	6.62	6.97	1.18
t_{PHL}		4.42	4.50	4.73	0.77	6.17	6.28	6.62	1.11
t_r	Output Rise Time, DO0-DO17	0.34	0.59	1.35	2.54	1.21	1.52	2.45	3.10
t_f	Output Fall Time, DO0-DO17	0.63	0.73	1.02	0.99	0.88	1.02	1.41	1.32
	RDB32X36								
t_{PLH}	Propagation Delay, A0-A4 to DO0-DO35	3.92	4.00	4.25	0.82	6.00	6.12	6.48	1.20
t_{PHL}		4.43	4.50	4.72	0.72	6.09	6.18	6.47	0.96
t_{PLH}	Propagation Delay, DIN0-DIN35 to DO0-DO35	3.00	3.08	3.32	0.81	5.02	5.14	5.50	1.21
t_{PHL}		4.05	4.14	4.44	0.98	5.82	5.91	6.18	0.88

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
t_{PLH}	Propagation Delay, RWB0-RWB35 to DO0-DO35	4.58	4.66	4.91	0.83	6.90	7.05	7.50	1.50
t_{PHL}		4.80	4.88	5.10	0.76	6.73	6.82	7.11	0.96
t_r	Output Rise Time, DO0-DO35	0.43	0.68	1.43	2.49	0.75	1.09	2.12	3.44
t_f	Output Fall Time, DO0-DO35	0.83	0.92	1.19	0.90	0.89	1.00	1.32	1.08
	RDB32X72								
t_{PLH}	Propagation Delay, A0-A4 to DO0-DO71	4.17	4.25	4.50	0.82	6.32	6.45	6.83	1.27
t_{PHL}		4.75	4.81	5.00	0.64	6.43	6.54	6.88	1.13
t_{PLH}	Propagation Delay, DIN0-DIN71 to DO0-DO71	3.00	3.08	3.33	0.81	5.03	5.15	5.51	1.20
t_{PHL}		4.04	4.14	4.44	0.99	5.82	5.91	6.18	0.88
t_{PLH}	Propagation Delay, RWB0-RWB71 to DO0-DO71	5.18	5.26	5.50	0.81	7.89	8.01	8.37	1.19
t_{PHL}		5.28	5.36	5.59	0.78	7.33	7.43	7.73	1.00
t_r	Output Rise Time, DO0-DO71	0.39	0.64	1.37	2.45	1.19	1.51	2.45	3.15
t_f	Output Fall Time, DO0-DO71	0.88	0.97	1.24	0.90	1.23	1.34	1.66	1.06

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

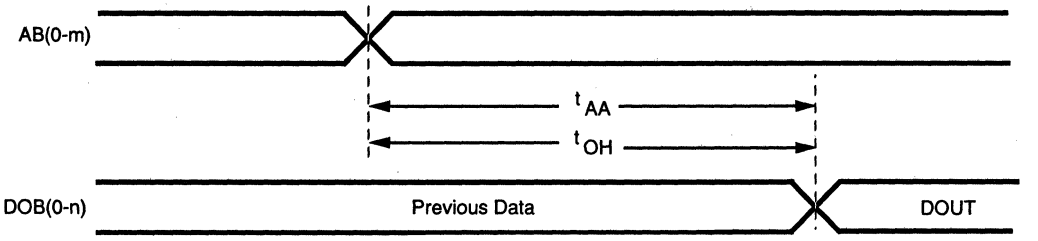
TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Abbr.	Parameter		8-WORD BLOCK		16-WORD BLOCK		32-WORD BLOCK	
			5 V	3.3 V	5 V	3.3 V	5 V	3.3 V
t_{DSU}	Set Up Time,	DINA(n) to WBA (WL = 9)	0.28	0.53	0.37	0.64	0.19	0.77
		DINA(n) to WBA (WL = 18)	0.12	0.27	0.21	0.40	0.08	0.50
		DINA(n) to WBA (WL = 36)	-0.05	-0.08	0.05	0.12	-0.08	0.35
		DINA(n) to WBA (WL = 72)	-0.47	-0.46	-0.36	-.012	-0.43	-0.37
t_{AWB}	Set Up Time,	AA(n) to WBA (WL = 9)	0.02	-0.16	0.12	0.15	-0.25	-0.22
		AA(n) to WBA (WL = 18)	0.01	-0.27	0.01	0.05	-0.25	-0.46
		AA(n) to WBA (WL = 36)	-0.23	-0.61	-0.08	-0.27	-0.48	-0.50
		AA(n) to WBA (WL = 72)	-0.52	-0.94	-0.25	-0.42	-0.73	-1.13
t_{ASU}	Set Up Time,	AA(n) to WBA (WL = 9)	4.00	5.01	3.98	4.90	3.23	5.42
		AA(n) to WBA (WL = 18)	4.22	5.28	4.20	5.23	3.53	5.86
		AA(n) to WBA (WL = 36)	4.65	5.90	4.55	5.81	3.97	5.54
		AA(n) to WBA (WL = 72)	5.06	6.56	4.87	6.35	4.42	7.02
t_{DH}	Hold Time,	WBA to DINA(n) (WL = 9)	0.87	1.28	0.72	1.11	1.33	1.73
		WBA to DINA(n) (WL = 18)	1.10	1.62	0.93	1.45	1.51	1.97
		WBA to DINA(n) (WL = 36)	1.41	2.14	1.28	1.92	1.97	2.52
		WBA to DINA(n) (WL = 72)	1.98	2.85	1.80	2.56	2.46	3.34
t_{DH}	Hold Time,	WBA to AA(n) (WL = 9)	0.66	1.10	0.33	0.75	1.19	1.51
		WBA to AA(n) (WL = 18)	0.82	1.35	0.46	0.99	1.29	1.66
		WBA to AA(n) (WL = 36)	1.14	1.87	0.82	1.48	1.76	2.21
		WBA to AA(n) (WL = 72)	1.61	2.44	1.22	1.96	2.18	2.90
t_{WP}	Pulse Width	WBA (L) (WL = 9)	1.97	3.00	1.95	2.95	2.40	3.54
		WBA (L) (WL = 18)	2.20	3.28	2.18	3.25	2.61	3.86
		WBA (L) (WL = 36)	2.62	3.93	2.53	3.83	3.06	4.58
		WBA (L) (WL = 72)	3.09	4.53	2.93	4.37	3.52	5.11

7

TIMING DIAGRAM: READ CYCLE High Speed Dual Port RAM



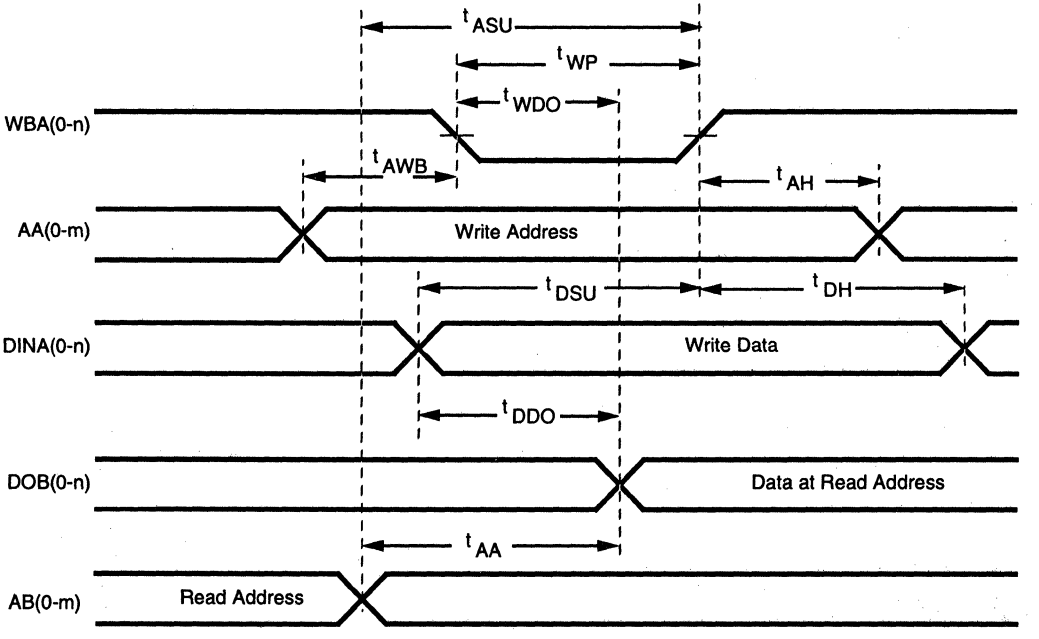
NOTES:
1. WB_A(n) has no affect on Read Operations.

2. Read is accomplished by placing the location of the desired Memory word on the A_B Address Bus.
No other action is necessary.

3. Since Addresses are not latched internally, the Data-Out Bus, DO_B(n), will always reflect the contents of the Memory location selected by Address Bus A_B(m), following time period t_{AA}.

4. The OUTPUT HOLD TIME, t_{OH}, will be the same as t_{AA} due to internal switching speed and internal loading.

TIMING DIAGRAM: WRITE CYCLE High Speed Dual Port RAM

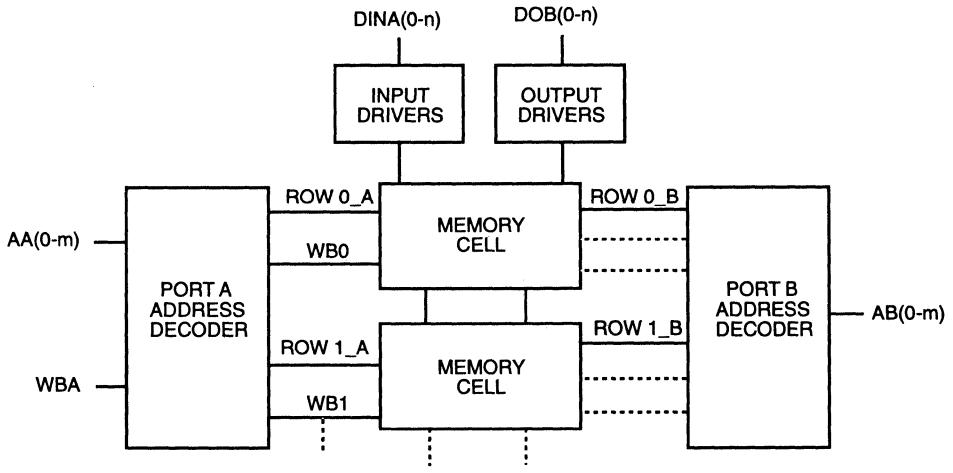


NOTES:
1. For a Write Operation, Address must remain stable for the contiguous period consisting of time periods t_{AWB}, t_{WP} and t_{AH}.

2. Since the Address is not latched internally, the Data-Out Bus, DOB(n), will always reflect the contents of the respective Memory location selected on Address Bus AB(m) following time period t_{AA}.

3. Parameter t_{DDO} will only apply if the Address value on the Write Address Bus, AA(m), is the same as the Address value on the Read Address Bus, AB(m). Configurations equating the Write Address Bus with Read Address Bus allows the Write Data to appear on the Data-Out Bus, DOB(n) concurrent with the Write Operation.

FUNCTIONAL DIAGRAM: High Speed Dual Port RAM



7

Four Port RAM

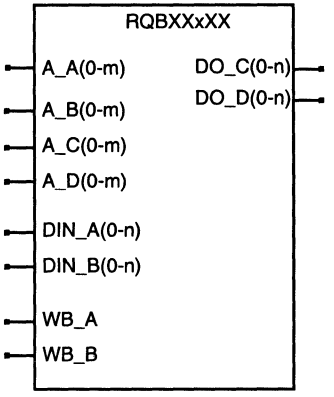
RQBXXxXX

MACRO	EQUIV. GATES
RQBXXxXX	see table below

Rev. 1.07

INPUTS	AA(0-m),AB(0-m),AC(0-m), AD(0-m), DINA(0-n),DINB(0-n), WBA(0-n), WBB(0-n)
OUTPUTS	DOC(0-n),DOD(0-n)

SIGNAL NAME	INPUT CAP.
AA(0-m)	see table below
AB(0-m)	see table below
AC(0-m)	see table below
AD(0-m)	see table below
DINA(0-n) DINB(0-n)	0.06 pF
WBA	see table below
WBB	see table below



Size, Address Line Input Capacitance, and Array Availability Information for Single Port RAM's

Size (Words X Bits)	Name	Size (Columns X Rows)	Total Gate Count	Input Capacitance Per Address Line	Input Capacitance WB_A & WB_B Lines
16-WORD BLOCK					
16X18	RQB16X18	33X37	2200	0.18 pF	0.12 pF
16X36	RQB16X36	55X37	3766		
32-WORD BLOCK					
32X18	RQB32X18	36X70	4762	0.36 pF	024 pF
32X36	RQB32X36	58X70	7738		

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns.

Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
RQB16X18									
t_{PLH}	Propagation Delay, AC0-AD3 to DOC0-DOD17	3.52	3.69	4.20	1.69	5.50	5.73	6.44	2.34
t_{PHL}		3.98	4.12	4.54	1.40	5.90	6.06	6.51	1.50
t_{PLH}	Propagation Delay, DINA0-DINB17 to DOC0-DOD17	3.84	4.01	4.51	1.67	6.08	6.29	6.95	2.18
t_{PHL}		5.06	5.24	5.76	1.75	7.22	7.39	7.91	1.72
t_{PLH}	Propagation Delay, WBA,WBB to DOC0-DOD17	5.03	5.20	5.71	1.70	8.43	8.66	9.35	2.31
t_{PHL}		5.57	5.72	6.15	1.43	8.08	8.24	8.74	1.66
t_r	Output Rise Time, DOC0-DOD17	0.34	0.84	2.36	5.04	0.67	1.35	3.39	6.80
t_f	Output Fall Time, DOC0-DOD17	0.69	0.90	1.52	2.06	1.29	1.51	2.18	2.23
RQB16X36									
t_{PLH}	Propagation Delay, AC0-AD3 to DOC0-DOD35	3.91	4.08	4.57	1.64	6.04	6.28	7.00	2.39
t_{PHL}		4.51	4.65	5.07	1.40	6.36	6.52	7.00	1.60
t_{PLH}	Propagation Delay, DINA0-DINB17 to DOC0-DOD35	3.84	4.01	4.51	1.67	6.07	6.30	7.01	2.36
t_{PHL}		5.06	5.23	5.76	1.75	7.23	7.41	7.92	1.72
t_{PLH}	Propagation Delay, WBA,WBB to DOC0-DOD35	5.42	5.59	6.10	1.70	9.09	9.32	10.01	2.30
t_{PHL}		6.10	6.24	6.67	1.43	7.37	7.55	8.08	1.77
t_r	Output Rise Time, DOC0-DOD35	0.25	0.77	2.32	5.18	0.89	1.54	3.50	6.52
t_f	Output Fall Time, DOC0-DOD35	0.70	0.92	1.58	2.18	1.11	1.34	2.03	2.31

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Sym	Parameter	5.0 V				3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
	RQB32X18								
t_{PLH}	Propagation Delay, AC0-AD4 to DOC0-DOD17	4.88	5.05	5.55	1.67	6.97	7.21	7.94	2.41
t_{PHL}		5.85	5.99	6.39	1.34	7.90	8.09	8.65	1.87
t_{PLH}	Propagation Delay, DINA0-DINB35 to DOC0-DOD17	5.82	6.01	6.58	1.91	8.69	8.99	9.90	3.03
t_{PHL}		9.02	9.19	9.68	1.64	11.45	11.62	12.14	1.74
t_{PLH}	Propagation Delay, WBA-WBB to DOC0-DOD17	7.08	7.26	7.81	1.82	11.19	11.46	12.26	2.68
t_{PHL}		8.55	8.72	9.20	1.62	11.38	11.59	12.20	2.03
t_r	Output Rise Time, DOC0-DOD17	0.70	1.18	2.63	4.81	2.08	2.66	4.40	5.80
t_f	Output Fall Time, DOC0-DOD17	1.13	1.31	1.85	1.81	2.44	2.65	3.28	2.10
	RQB32X36								
t_{PLH}	Propagation Delay, AC0-AD4 to DOC0-DOD35	4.97	5.15	5.67	1.75	7.85	8.09	8.81	2.40
t_{PHL}		6.16	6.29	6.70	1.35	8.52	8.71	9.26	1.86
t_{PLH}	Propagation Delay, DINA0-DINB35 to DOC0-DOD35	5.82	6.01	6.58	1.91	8.69	8.99	9.90	3.03
t_{PHL}		8.68	8.85	9.34	1.64	11.27	11.49	12.18	2.27
t_{PLH}	Propagation Delay, WBA-WBB to DOC0-DOD35	7.03	7.21	7.74	1.77	9.90	10.21	11.11	3.03
t_{PHL}		9.21	9.31	9.64	1.08	11.95	12.12	12.64	1.71
t_r	Output Rise Time, DOC0-DOD35	0.52	1.04	2.59	5.16	1.84	2.43	4.21	5.92
t_f	Output Fall Time, DOC0-DOD35	1.13	1.32	1.87	1.85	2.51	2.73	3.38	2.16

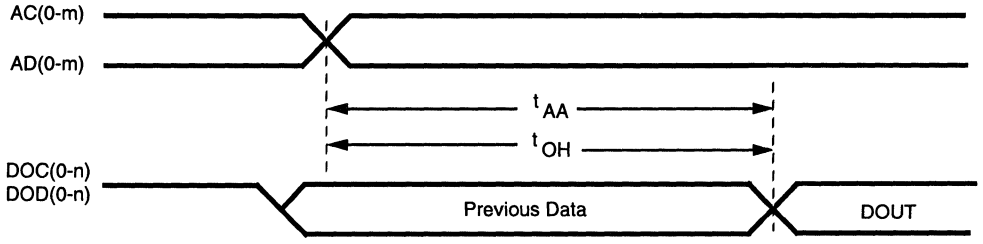
Capacitance per fanout = 0.05 pF (metal capacitance is not included).

TIMING REQUIREMENTS

(Input Edge Rate tr,tf=1.00ns) TJ= 25.0°C (Nominal) all units are in ns. Rev. 1.07

Abbr.	Parameter		16-WORD BLOCK		32-WORD BLOCK	
			5 V	3.3 V	5 V	3.3 V
t_{DSU}	Set Up Time,	DIN(n) to WB (WL =18)	-0.21	0.04	0.27	0.44
		DIN(n) to WB (WL =36)	-0.46	-0.34	-0.04	-0.27
t_{AWB}	Set Up Time,	AA to WB (WL =18)	-0.83	-1.27	-0.80	-1.32
		AA to WB (WL =36)	-1.09	-1.76	-1.07	-1.60
t_{ASU}	Set Up Time,	AA to WB (WL =18)	5.02	6.57	5.01	6.54
		AA to WB (WL =36)	5.33	6.39	5.36	6.54
t_{DH}	Hold Time,	WB to DIN(n) (WL =18)	2.42	3.26	2.42	3.23
		WB to DIN(n) (WL =36)	2.65	3.75	2.88	4.09
t_{WP}	Pulse Width	WB to DO (n) (WL =18)	3.00	4.57	3.03	4.38
		WB to DO (n) (WL =36)	3.31	4.95	3.34	4.87

TIMING DIAGRAM: READ CYCLE Four Port RAM



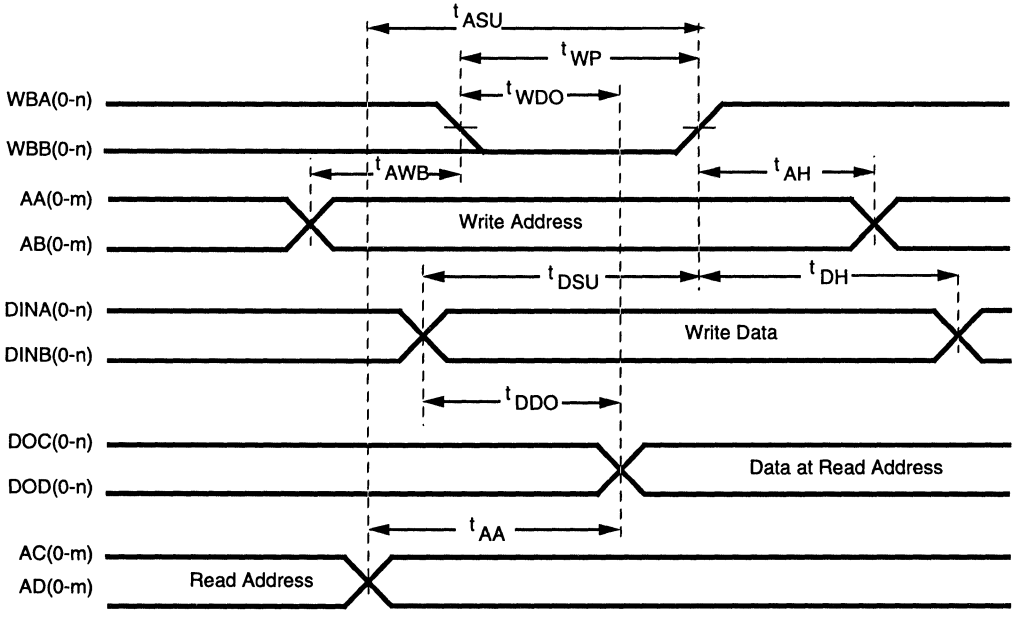
NOTES:
1. WBA(n) has no affect on Read Operations.

2. Read is accomplished by placing the location of the desired Memory word on Address Bus AC(n) and /or AD(m). No other action is necessary.

3. Since Addresses are not latched internally, the Data-Out Bus, DOC(n) **AND** DOD(n), will always reflect the contents of the Memory location selected by Address Bus AC(m) and AD(m), following time period t_{AA}.

4. The OUTPUT HOLD TIME, t_{OH}, will be the same as t_{AA} due to internal switching speed and internal loading.

TIMING DIAGRAM: WRITE CYCLE Four Port RAM

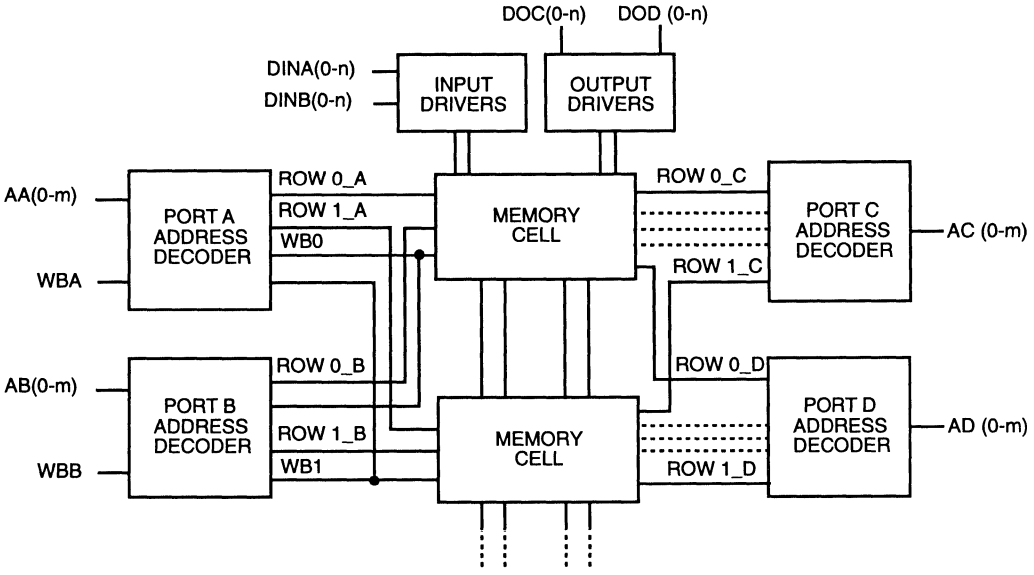


NOTES:
1. For a Write Operation, Address must remain stable for the contiguous period consisting of time periods t_{AWB}, t_{WP} and t_{AH}.

2. Since the Address is not latched internally, the Data-Out Bus, DOC(n) and DOD(n), will always reflect the contents of the respective Memory location selected on Address Bus AC(m) and AD(m)following time period t_{AA}.

3. Parameter t_{DDO} will only apply if the Address value on the Write Address Bus, AA(m) and AB(m), is the same as the Address value on the Read Address Bus, AC(m) and AD(m). Configurations equating the Write Address Bus with Read Address Bus allows the Write Data to appear on the Data-Out Bus, DOC(n) and DOD)n) concurrent with the Write Operation.

FUNCTIONAL DIAGRAM: of Four Port RAM



7

Section 7.6 Analog Phase Lock Loop Macros

CMOS Single-Ended Analog Phase Locked Loop (3.3 V and 5 V System/Core Voltage)

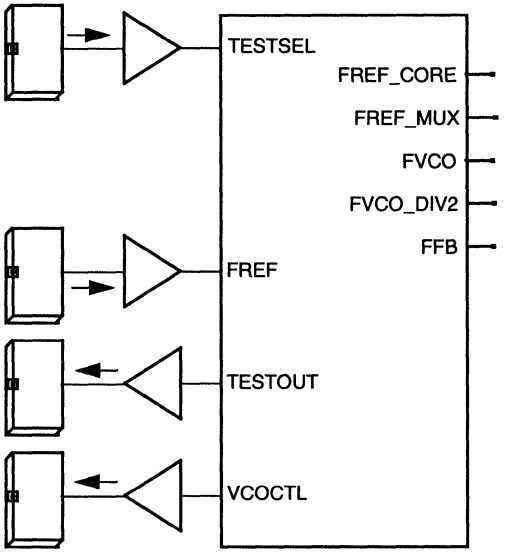
5/5 V AP1
5/5 V AP2
3.3/3.3 V APL1
3.3/3.3 V APL2

MACRO	EQUIV. GATES
All	0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	FREF_CORE,FVCO,FVCO_DIV2,TESTOUT, VCOCTL / FREF,FREF_MUX,FFB,TESTSEL

MACRO	INPUT CAP.
AP1,AP2	FFB: 0.13pF FREF: 5.06pF FREF_MUX: 0.04pF TESTSEL: 0.09pF
APL1,APL2	FFB: 0.13pF FREF: 5.06pF FREF_MUX: 0.04pF TESTSEL: 0.08pF



7

CMOS SWITCHING CHARACTERISTICS (Input Edge Rate t_r,t_f=1.0ns) Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		AP1				APL1			
t_{PLH}	Propagation Delay, FREF to FREF_CORE	0.30	0.31	0.35	0.13	0.42	0.45	0.53	0.27
t_{PHL}		0.32	0.34	0.40	0.18	0.41	0.42	0.47	0.17
t_{PHL}	Propagation Delay, TESTSEL to FVCO, FVCO_DIV2	2.67	2.67	2.67	0.00	3.94	3.94	3.94	0.00
t_r	Output Rise Time, FREF_CORE	0.13	0.16	0.26	0.34	0.19	0.22	0.31	0.29
t_f	Output Fall Time, FREF_CORE	0.12	0.14	0.21	0.20	0.18	0.20	0.25	0.18
t_r	Output Rise Time, FVCO,FVCO_DIV2	0.14	0.16	0.21	0.16	0.18	0.20	0.27	0.22
t_f	Output Fall Time, FVCO,FVCO_DIV2	0.15	0.17	0.22	0.19	0.17	0.20	0.27	0.24

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS (Input Edge Rate t_r,t_f=1.0ns) Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		AP2				APL2			
t_{PLH}	Propagation Delay, FREF to FREF_CORE	0.30	0.31	0.35	0.13	0.42	0.45	0.53	0.27
t_{PHL}		0.32	0.34	0.40	0.18	0.41	0.42	0.47	0.17
t_{PHL}	Propagation Delay, TESTSEL to FVCO, FVCO_DIV2	2.67	2.67	2.67	0.00	3.94	3.94	3.94	0.00
t_r	Output Rise Time, FREF_CORE	0.13	0.16	0.26	0.34	0.19	0.22	0.31	0.29
t_f	Output Fall Time, FREF_CORE	0.12	0.14	0.21	0.20	0.18	0.20	0.25	0.18
t_r	Output Rise Time, FVCO,FVCO_DIV2	0.14	0.16	0.21	0.16	0.18	0.20	0.27	0.22
t_f	Output Fall Time, FVCO,FVCO_DIV2	0.15	0.17	0.22	0.19	0.17	0.20	0.27	0.24

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/5 V	3.3/3/3 V
		Minimum Requirement	Minimum Requirement
		AP1, AP2	APL1, APL2
t_{rec}	Recovery Time, TESTSEL to FREF	-0.03	0.35
t_w	Pulse Width, FREF(L)	0.60	0.90
t_w	Pulse Width, FREF(H)	0.45	0.90
t_w	Pulse Width, TESTSEL(L)	0.91	0.99

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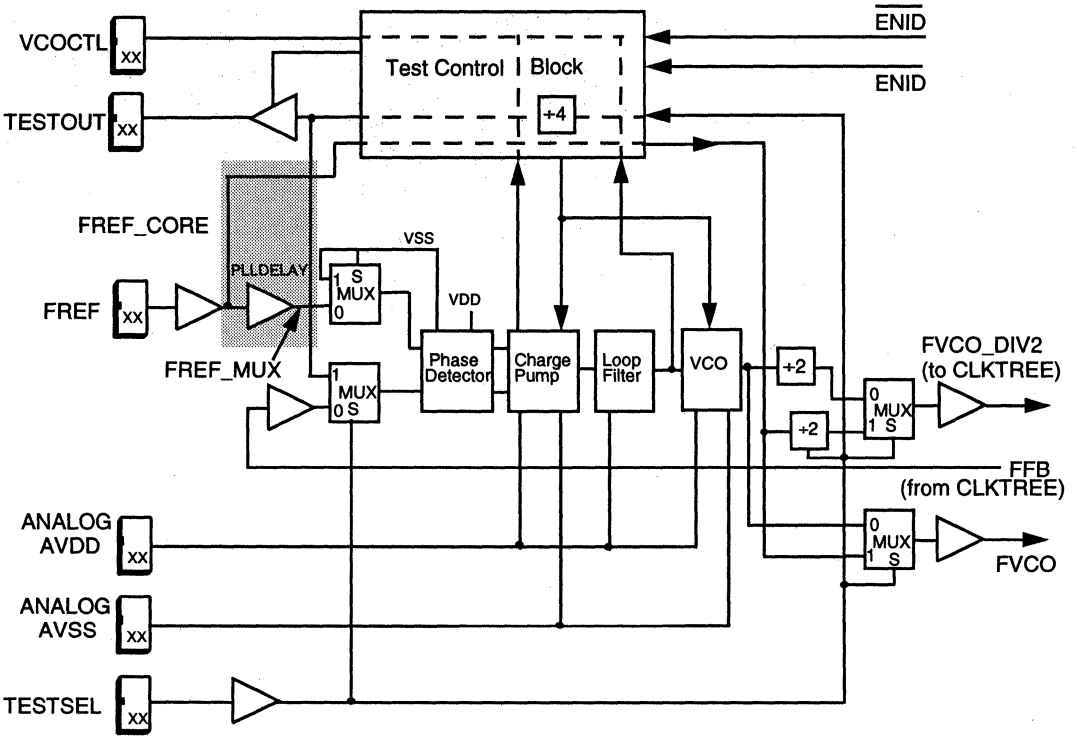
FUNCTIONAL DIAGRAM: Analog Phase Locked Loop -CMOS Input



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PECL Differential Analog Phase Locked Loop (3.3 V and 5 V System/Core Voltage)

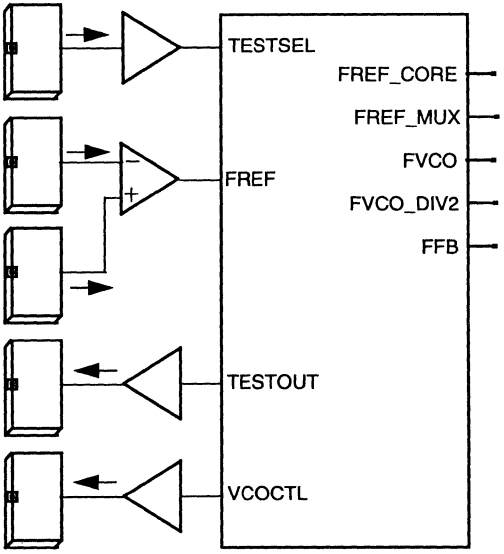
5/5 V	APD1
5/5 V	APD2
3.3/3.3 V	APDL1
3.3/3.3 V	APDL2

MACRO	EQUIV. GATES
All	0

Rev. 1.07

MACRO	OUTPUTS/INPUTS
All	FREF_CORE,FVCO,FVCO_DIV2,TESTOUT, VCOCTL / FREF,FREFB,FREF_MUX,FFB,TESTSEL

MACRO	INPUT CAP.
APD1,APD2	FFB,TESTSEL: 0.08pF FREF,FREFB: 4.98pF FREF_MUX: 0.04pF
APDL1,APDL2	FFB,TESTSEL: 0.07pF FREF,FREFB: 4.98pF FREF_MUX: 0.04pF



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CMOS SWITCHING CHARACTERISTICS (Input Edge Rate t_r,t_f=1.0ns) Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		APD1				APDL1			
t_{PLH}	Propagation Delay, FREF,FREFB to FREF_CORE	0.65	0.66	0.70	0.11	0.90	0.92	0.96	0.14
t_{PHL}		0.68	0.69	0.74	0.15	0.98	0.99	1.05	0.18
t_{PHL}	Propagation Delay, TESTSEL to FVCO,FVCO_DIV2	2.67	2.67	2.67	0.00	3.94	3.94	3.94	0.00
t_r	Output Rise Time, FREF_CORE	0.11	0.14	0.21	0.25	0.16	0.20	0.31	0.37
t_f	Output Fall Time, FREF_CORE	0.12	0.14	0.21	0.23	0.18	0.20	0.28	0.26
t_r	Output Rise Time, FVCO,FVCO_DIV2	0.14	0.16	0.21	0.16	0.18	0.20	0.27	0.22
t_f	Output Fall Time, FVCO,FVCO_DIV2	0.15	0.17	0.22	0.19	0.17	0.20	0.27	0.24

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS SWITCHING CHARACTERISTICS (Input Edge Rate t_r,t_f=1.0ns) Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
		APD2				APDL2			
t_{PLH}	Propagation Delay, FREF,FREFB to FREF_CORE	0.65	0.66	0.70	0.11	0.90	0.92	0.96	0.14
t_{PHL}		0.68	0.69	0.74	0.15	0.98	0.99	1.05	0.18
t_{PHL}	Propagation Delay, TESTSEL to FVCO, FVCO_DIV2	2.67	2.67	2.67	0.00	3.94	3.94	3.94	0.00
t_r	Output Rise Time, FREF_CORE	0.11	0.14	0.21	0.25	0.16	0.20	0.31	0.37
t_f	Output Fall Time, FREF_CORE	0.12	0.14	0.21	0.23	0.18	0.20	0.28	0.26
t_r	Output Rise Time, FVCO,FVCO_DIV2	0.14	0.16	0.21	0.16	0.18	0.20	0.27	0.22
t_f	Output Fall Time, FVCO,FVCO_DIV2	0.15	0.17	0.22	0.19	0.17	0.20	0.27	0.24

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

CMOS TIMING REQUIREMENTS (Input Edge Rate t_r,t_f=1.00ns) Rev. 1.07

Sym	Parameter	5/5 V	3.3/3/3 V
		Minimum Requirement	Minimum Requirement
		APD1, APD2	APDL1, APDL2
t_{rec}	Recovery Time, TESTSEL to FREF	-0.03	0.35
t_{rec}	Recovery Time, TESTSEL to FREFB	-0.03	0.35
t_w	Pulse Width, FREF,FREFB(L)	0.60	0.90
t_w	Pulse Width, FREF,FREFB(H)	0.45	0.90
t_w	Pulse Width, TESTSEL(L)	0.91	0.99

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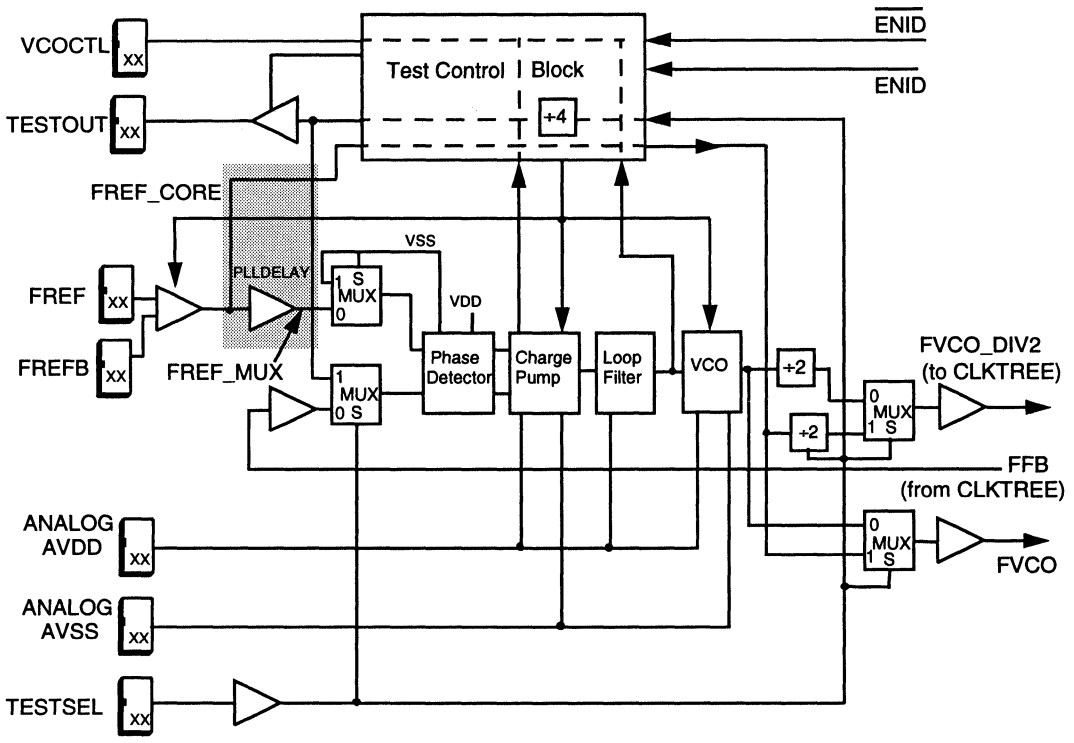
FUNCTIONAL DIAGRAM: Analog Phase Locked Loop -PECL Input



7

Non-Inverting Analog PLL Buffer 1X Drive (3.3 V and 5 V Voltage)

5/5 V / 3.3/3.3 V **PLLDELAY**

MACRO	EQUIV. GATES
PLLDELAY	1

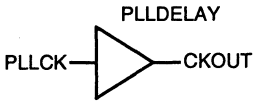
Rev. 1.07

MACRO	OUTPUTS/INPUTS
PLLDELAY	CKOUT / PLLCK

MACRO	INPUT CAP.
PLLDELAY	PLLCK: 0.05pF

FUNCTION TABLE

PLLCK	CKOUT
L	L
H	H



CMOS SWITCHING CHARACTERISTICS (Input Edge Rate t_r,t_f=1.0ns) Rev.1.07

Sym	Parameter	5/5 V				3.3/3.3 V			
		FO=0	FO=2	FO=8	K (ns/pF)	FO=0	FO=2	FO=8	K (ns/pF)
PLLDELAY									
t_{PLH}	Propagation Delay, PLLCK to CKOUT	0.29	0.37	0.62	0.82	0.29	0.37	0.62	0.82
t_{PHL}		0.28	0.35	0.58	0.75	0.28	0.35	0.58	0.75
t_r	Output Rise Time, CKOUT	0.17	0.41	1.14	2.42	0.17	0.41	1.14	2.42
t_f	Output Fall Time, CKOUT	0.15	0.26	0.61	1.17	0.15	0.26	0.61	1.17

Capacitance per fanout = 0.05 pF (metal capacitance is not included).

7

DC ELECTRICAL CHARACTERISTICS

8

8 DC ELECTRICAL CHARACTERISTICS

SECTION 8. H4CPlus DC ELECTRICAL CHARACTERISTICS

Table 8-1 Preliminary Electrical Considerations for H4CPlus Series Arrays

ABSOLUTE MAXIMUM RATINGS				
Symbol	Parameter	V_{DD}=3V/3.3V±0.3V	V_{DD}=5V±10%	Unit
V_{DD}	DC Supply Voltage	-0.5 to 4.6	-0.5 to 6.0	V
V_{in}	DC Input Voltage	-0.5 to V_{DD} + 0.5	-0.5 to V_{DD} + 0.5	V
Vout	DC Output Voltage	-0.5 to V_{DD} + 0.5	-0.5 to V_{DD} + 0.5	V
I	DC Current Drain per Pin, Any Single Input or Output	±50	±50	mA
I	DC Current Drain per Pin, Any Paralleled Outputs	±100	±100	mA
I	DC Current Drain VDD and VSS Pins	±100	±100	mA
T_{stg}	Storage Temperature	-65 to +150	-65 to +150	°C
T_L	Lead Temperature (10 second soldering)	300	300	°C

Note: Maximum ratings are those values beyond which damage to the device may occur.

RECOMMENDED OPERATING CONDITIONS (to guarantee functionality)				
Symbol	Parameter	Min	Max	Unit
V_{DD}*	DC Supply Voltage, V_{DD} = 5.0V (Nominal)	4.5	5.5	V
V_{DD}*	DC Supply Voltage, V_{DD} = 3.0/3.3V (Nominal)	2.7	3.6	V

* For testing, only. V_{DD} range is wider for simulation purposes.

Notes:
1. All parameters are characterized for DC conditions after thermal equilibrium has been established.
2. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{ss} or V_{DD}).
3. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

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Table 8-2 Preliminary DC Electrical Characteristics for H4CPlus Series Arrays (T_a = -40°C to 85°C)

Sym.	Parameter	Condition	V_{DD}=3V/3.3V±0.3V Guaranteed		V_{DD}=5V±10% Guaranteed		Unit
			Min.	Max.	Min.	Max.	
V_{IH}	Input High Voltage, CMOS Inputs (3.3V and 5V core)		2.0	V_{DD}+0.3	0.7 V_{DD}	V_{DD}+0.3	V
	TTL Inputs (5V core)		2.0	V_{DD}+0.3	2.2*	V_{DD}+0.3	
V_{IL}	Input Low Voltage, CMOS Inputs (3.3V and 5V core)		-0.3	0.8	-0.3	0.3 V_{DD}	V
	TTL Inputs (5V core)		-0.3	0.8	-0.3	0.8	
V_{T+}	Positive Threshold Voltage, CMOS Schmitt Trigger		-	0.75V_{DD}	-	0.7V_{DD}	V
	TTL Schmitt Trigger		N/A	N/A	-	2.4	
V_{T-}	Negative Threshold Voltage, CMOS Schmitt Trigger		0.25V_{DD}	-	0.25V_{DD}	-	V
	TTL Schmitt Trigger		N/A	N/A	0.8	-	
V_{Hy}	Hysteresis - CMOS Schmitt Trigger	V_{T+} to V_{T-}	0.1V_{DD}		0.12V_{DD}	-	V
	Hysteresis - TTL Schmitt Trigger		N/A	N/A	0.05V_{DD}	-	
I_{OH}†	Output High Current, ON16 Output Type	V_{DD} =Min, V_{OH} Min= 0.8V_{DD}	-12.0	-	-24.0	-	mA
	ON8 Output Type		-6.0	-	-12.0	-	
	ON4 Output Type		-3.0	-	-6.0	-	
	ON2 Output Type		-2.0	-	-3.0	-	
I_{OL}	Output Low Current, ON16 Output Type	V_{DD} =Min, V_{OL} Max= 0.4 Volts	12	-	24.0	-	mA
	ON8 Output Type		6	-	12.0	-	
	ON4 Output Type		3	-	6.0	-	
	ON2 Output Type		2	-	3.0	-	
V_{OH}	Output High Voltage, LVCMOS	V_{DD} = Min, I_{OH}= -100µA	V_{DD}-0.2	-	N/A	N/A	V
V_{OL}	Output Low Voltage, LVCMOS	V_{DD} = Min, I_{OH}= -100µA	-	0.2	N/A	N/A	V
I_{in}	Input Leakage Current, No Pull Resistor	V_{in} = V_{DD} or V_{SS}	-5	5	-5	5	µA
	with Pullup Resistor	PUL; V_{in} = V_{SS}	-5	-100	-10	-200	
	with Pulldown Resistor	PDL; V_{in} = V_{DD}	5	100	10	200	
I_{oz}**	Output Leakage Current, 3-State Output	Output = Hi Impedance V_{out} = V_{DD} or V_{SS}	-10	10	-10	10	µA
	Output Leakage Current, Open Drain Output (Device Off)	Output = Hi Impedance V_{out} = V_{DD}	-10	10	-10	10	
I_{DD}	Max Quiescent Supply Current	I_{out} = 0mA V_{in} = V_{DD} or V_{SS}	Design Dependent				mA

* V_{IH} = 2.0V at V_{DD} = 5V±5%
** Single-Drive Output
† For 3.3V ± 0.3 and 5V ± 10%, only. For 2.7 V consult factory.

Table 8-3 Preliminary DC Electrical Characteristics for H4CPlus GTL I/O (T_a = -40°C to 85°C)

Sym.	Parameter	Conditions	V_{DD}= 3.3V±0.3V Guaranteed		V_{DD}=5V±10% Guaranteed		Unit
			Min.	Max.	Min.	Max.	
DC Characteristics for GTL Receivers							
V_{IH}	Input High Voltage, GTL Inputs	N/A	V_{VR08}+0.10	V_{DD}+0.30	V_{VR08}+0.10	V_{DD}+0.30	V
V_{IL}	Input Low Voltage, GTL Inputs	N/A	-0.30	V_{VR08}-0.10	-0.30	V_{VR08}-0.10	V
I_{IH}	Input High Current, GTL Input	V_{in}=V_{TT}, V_{DD}= Max	-	5	-	5	µA
I_{IL}	Input Low Current, GTL Inputs	V_{in}=0.4V, V_{DD}= Max	-	-5	-	-5	µA
V_{VR08}	GTL Ref. Voltage	-	0.68	0.90	0.68	0.90	V
I_{DD}*	Typical Quiescent Supply Current	-	2.0				mA
DC Characteristics for GTL Drivers							
V_{OH}*	Output High Voltage, 20mA Output Macros	I_{OH}=-10µA, V_{DD}= Min	V_{TT} -0.05	V_{TT} +0.05	V_{TT} -0.05	V_{TT} +0.05	V
	40mA Output Macros	I_{OH}=-10µA, V_{DD}= Min	V_{TT} -0.05	V_{TT} +0.05	V_{TT} -0.05	V_{TT} +0.05	
V_{OL}	Output Low Voltage, 20mA Output Macros	I_{OL}=20mA, V_{DD}= 3 V	-	0.4	-	-	V
	40mA Output Macros	I_{OL}=40mA, V_{DD}= 3 V	-	0.4	-	-	
V_{OL}	Output Low Voltage, 24mA Output Macros	I_{OL}=24mA, V_{DD}= 4.5 V	-	-	-	0.4	V
	48mA Output Macros	I_{OL}=48mA, V_{DD}= 4.5 V	-	-	-	0.4	
I_{OZH}	GTL Output Off Current High	V_{out}=1.2V, V_{DD}= Max	-	10	-	10	µA
I_{OZL}	GTL Output Off Current Low	V_{out}=0.4V, V_{DD}= Max	-	-10	-	-10	µA

* Not tested.

Notes:
1. Recommended: V_{TT} = 1.2V ± 5%, V_{VR08} = (2/3) V_{TT}, RT = 25Ω/50Ω.

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Table 8-4 Preliminary DC Electrical Characteristics for H4CPlus CMTL Buffers (T_a = -40°C to 85°C)

Sym.	Parameter	Conditions	V_{DD}= 3.3V±0.3V Guaranteed		V_{DD}=5V±10% Guaranteed		Unit
			Min.	Max.	Min.	Max.	
DC Characteristics for CMTL Receivers							
V_{IDH}	Minimum Input High Voltage, CMTL Inputs (Differential)	See Definition in Section 9	-	100	-	100	mV
V_{IDL}	Maximum Input Low Voltage, CMTL Inputs (Differential)	See Definition in Section 9	-	100	-	100	mV
V_{ICM}	Input Common Mode Voltage Range, V_{ICM} Min	See Definition in Section 9, V_{DD}= Max	0.6	-	1.0	-	V
	V_{ICM} Max	See Definition in Section 9, V_{DD}= Min	-	2.2	-	3.5	V
I_{IH}	Input High Current, CMTL Inputs (No Termination)	V_{in}=V_{OH}max, V_{DD}= Max	-	5	-	5	µA
	CMTL Inputs (Active Termination)	V_{in}=V_{OH}max, V_{DD}=Max	-	-	-	-	µA
I_{IL}	Input Low Current, CMTL Inputs (No Termination)	V_{in}=V_{OL}min, V_{DD}=Max	-	5	-	5	µA
	CMTL Inputs (Active Termination)	V_{in}=V_{OL}min, V_{DD}=Max	-	-	-	-	µA
I_{DD}	Max Quiescent Supply Current	-	-	2	-	4.2	mA
DC Characteristics for CMTL Drivers							
V_{OH}	Minimum Output High Voltage, CMTL Outputs (no Load)**	V_{DD}= Min	N/A	N/A	2.5	3.7	V
	CMTL Outputs (50Ω)†		c	c	2.4	3.1	
	CMTL Outputs (100Ω)†		c	c	2.5	3.2	
V_{OL}	Maximum Output High Voltage, CMTL Outputs (no Load)**	V_{DD}= Min	N/A	N/A	1.0	2.0	V
	CMTL Outputs (50Ω)†		c	c	1.6	2.4	
	CMTL Outputs (100Ω)†		c	c	1.5	2.3	
$\|V_{OD}\|$	Differential Output Voltage, CMTL Outputs (no Load)**	See Definition in Section 9 V_{DD}= Max	N/A	N/A	1.0	2.5	V
	CMTL Outputs (50Ω)†		c	c	0.4	1.1	
	CMTL Outputs (100Ω)†		c	c	0.5	1.4	
V_{OS}	Output Offset Voltage, CMTL Outputs (no Load)**	See Definition in Section 9 V_{DD}= Min	N/A	N/A	2.1	2.6	V
	CMTL Outputs (50Ω)†		c	c	2.1	2.65	
	CMTL Outputs (100Ω)†		c	c	2.1	2.65	
I_{OZH}	CMTL Output Off Current High	V_{out}=V_{DD}, V_{DD}= Max	-10	10	-10	10	µA
I_{OZL}	CMTL Output Off Current Low	V_{out}=V_{SS}, V_{DD}= Max	-10	10	-10	10	µA
R_o	Output Impedance (Typical)	100Ω ≤ Load ≤ 200 Ω †	50		30		Ω

* Not tested.
** OD32TCMT and BON32TCMT macros, only.
† Loads across differential CMTL outputs.
c Consult factory.

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Table 8-5 Preliminary DC Electrical Characteristics for PECL Receivers (T_a = -40°C to 85°C)

Sym.	Parameter	Conditions	V_{DD}= 3.3V±0.3V Guaranteed		V_{DD}=5V±10% Guaranteed		Unit
			Min.	Max.	Min.	Max.	
DC Characteristics for PECL Receivers							
V_{IDH}	Minimum Input High Voltage, PECL Differential Input	See Definition in Section 9	-	100	-	100	mV
V_{IDL}	Input Low Voltage, PECL Differential Input	See Definition in Section 9	-	100	-	100	mV
V_{ICM}	Input Common Mode Voltage Range, V_{ICM} Min	See Definition in Section 9	V_{DD}-2.0	-	V_{DD}-2.0	-	V
	V_{ICM} Max		-	V_{DD}-0.8	-	V_{DD}-0.8	V
I_{IH}	Input High Current, PECL Input	V_{in}=V_{DD}, V_{DD}=Max	-	5	-	5	µA
I_{IL}	Input Low Current, PECL Input	V_{in}=V_{SS}, V_{DD}=Max	-	5	-	5	µA
I_{DD}*	Max Quiescent Supply Current	-	0.5				mA

* Not tested.

Table 8-6 Preliminary Electrical Characteristics for H4CPlus Series PCI Buffers (T_a = -40°C to 85°C)

Sym.	Parameter	Condition	V_{DD}= 3.3V±0.3V Guaranteed		V_{DD}=5V±10% Guaranteed		Unit
			Min.	Max.	Min.	Max.	
DC Characteristics for PCI Receivers							
V_{IH}	Input High Voltage		0.475V_{DD}	V_{DD}+0.5	2.0	V_{DD}+0.5	V
V_{IL}	Input Low Volage		-0.5	0.325V_{DD}	-0.5	0.8	V
I_{IH}	Input High Leakage Current	3.3 V: 0<V_{in}<V_{DD} 5.0 V: V_{in} = 2.7 V	-	10	-	70	µA
I_{IL}	Input Low Leakage Current	3.3 V: 0<V_{in}<V_{DD} 5.0 V: V_{in} = 0.5 V	-	-10	-	-70	µA
DC Characteristics for PCI Drivers							
V_{OH}	Output High Voltage	3.3 V: I_{out} = -500 µA 5.0 V: I_{out} = -2 mA	0.9V_{DD}	-	2.4	-	V
V_{OL}	Output Low Voltage	3.3 V: I_{out} =1500 µA 5.0 V: I_{out} = 6 mA	-	0.1V_{DD}	-	0.55	V
AC Characteristics for PCI Drivers (Not Tested)							
V_{OHmin}	Output High Voltage Minimum	3.3 V: I_{out} = -12 mA 5.0 V: I_{out} = -44 mA	0.3V_{DD}	-	1.4	-	V
V_{OHmax}	Output High Voltage Maximum	3.3 V: I_{out} = -32 mA 5.0 V: I_{out} = -142 mA	-	0.7V_{DD}	-	3.1	V
V_{OLmin}	Output Low Voltage Minimum	3.3 V: I_{out} = 16 mA 5.0 V: I_{out} = 95 mA	0.6V_{DD}	-	2.2	-	V
V_{OLmax}	Output Low Voltage Maximum	3.3 V: I_{out} = 38 mA 5.0 V: I_{out} = 206 mA	-	0.18 V_{DD}	-	0.71	V

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DEFINITIONS OF SPECIFICATIONS

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9 DEFINITIONS OF SPECIFICATIONS

SECTION 9. DEFINITIONS OF SPECIFICATIONS

CURRENT

For the purpose of describing the direction of current flow a positive current refers to current flow into a device while negative current refers to current flow out of a device.

I_{DD} Maximum Quiescent Supply Current

The power supply current required without any internal nodes in the process of switching, under the specified conditions.

I_{in} Input Leakage Current

The maximum input leakage current, flowing into or out of a buffer, under the specified conditions.

I_{OH} Minimum Current of Output Buffers

The guaranteed minimum current flowing from an output buffer at the specified voltage level for the indicated buffer type and the indicated conditions.

I_{OL} Maximum Current of Output Buffers

The guaranteed minimum current flowing into an output buffer at the specified voltage level for the indicated buffer type and the indicated conditions.

I_{OZ} Output Leakage Current

The maximum output leakage current of an output buffer in the high-impedance state, under the specified conditions.

CAPACITANCE

C_{in} Input Capacitance of Input Buffers

The maximum internal capacitance seen at the pad of an input buffer.

$C_{I/O}$ Input Capacitance of Bidirectional Buffers

The maximum internal capacitance seen at the pad of a bidirectional buffer in input mode.

C_L Load Capacitance

The total external capacitance seen by an output buffer.

C_{out} Output Capacitance of Output Buffers

The maximum internal capacitance seen at the pad of an output buffer or bidirectional buffer in output mode in a high-impedance state.

VOLTAGE

All voltages are referenced to ground (V_{SS}).

HYSTERESIS

The difference in response due to the direction of input change. Specifically, the difference between V_{t+} and V_{t-}.

V_{CMRR} Common Mode Rejection Range

The common mode voltage rejection range for a driver /receiver combination is dependent on the system operating conditions. V_{CMRR} is the voltage range in which the output driver ground can be different from the input receiver ground while the receiver operates normally with the specified V_{ID}. V_{ICM+} specifies the upper voltage limit and V_{ICM-} specifies the lower voltage limit. In a system, the common mode voltage rejection range can be calculated using the following equations at the appropriate frequency, input voltage, line attenuation, power supply voltage range, and V_{DD} differences between driver and receiver:

$V_{CMRR+} = V_{ICM+} - V_{OS}$
$V_{CMRR-} = V_{ICM-} - V_{OS}$

V_{DD} Positive Power Supply Voltage

V_{ICM} Input Common Mode Voltage

The midpoint differential input voltage range for normal operation of the differential receiver in which the V_{ICM+} specifies the upper voltage limit and V_{ICM-} specifies the lower voltage limit. When the inputs are switching, the crossing voltage must be between the V_{ICM-} and V_{ICM+} values of V_{ICM}. For input signals V_{IA} (true) and V_{IB} (complement), $V_{ICM} = (V_{IA} + V_{IB})/2$.

V_{ID} The Differential Input Voltage Signal

The signal is defined as the difference in the voltages between the true and complement inputs of the differential receiver. For input signals V_{IA} (true) and V_{IB} (complement), $V_{ID} = V_{IA} - V_{IB}$.

V_{IDH} Differential Input Voltage HIGH

The voltage level is defined as a positive value that results when taking the true input voltage in the "high" state and subtracting the complement input voltage in the "low" state. For input signals V_{IA} (true) and V_{IB} (complement), $V_{IDH} = V_{IHA} - V_{ILB}$.

V_{IDL} Differential Input Voltage LOW
The voltage level is defined as a positive value that results when taking the complement input voltage in the "high" state and subtracting the true input voltage in the "low" state. For input signals V_{IA} (true) and V_{IB} (complement), $V_{IDL} = V_{IHB} - V_{ILA}$.

V_{IH} Input HIGH Voltage
The guaranteed input high threshold for inputs to the device. Whenever the input voltage level exceeds this value, a logic high will be recognized by the device.

V_{IL} Input LOW Voltage
The guaranteed input low threshold for inputs to the device. Whenever the input voltage level is below this value, a logic low will be recognized by the device.

V_{OD} The Differential Output Voltage Signal
The signal is defined as the difference in the voltages between the true and complement outputs of the differential driver. For output signals V_{OA} (true output) and V_{OB} (complement output), $V_{OD} = V_{OA} - V_{OB}$.

V_{ODH} The Differential Output Voltage HIGH
The voltage level is defined as a positive value that results when taking the true output voltage in the "high" state and subtracting the complement output voltage in the "low" state. For output signals V_{OA} (true) and V_{OB} (complement), $V_{ODH} = V_{OHA} - V_{OLB}$.

V_{ODL} The Differential Output Voltage LOW
The voltage level is defined as a positive value that results when taking the complement output voltage in the "high" state and subtracting the true output voltage in the "low" state. For output signals V_{OA} (true) and V_{OB} (complement), $V_{ODL} = V_{OHB} - V_{OLA}$.

V_{OH} Output Voltage HIGH
The voltage level at the output terminal is specified with a resistor load or a load current. V_{OHA} or V_{OHB} refers to the V_{OH} level at the A or B output terminal.

V_{OL} Output Voltage LOW
The voltage level at the output terminal is specified with a resistor load or a load current. V_{OLA} or V_{OLB} refers to the V_{OL} level at the A or B output terminal.

V_{OS} The Output Offset Voltage or Output Common Mode Voltage
This signal is defined as the voltage midpoint of the output signal. For differential output signals V_{OA} (true) and V_{OB} (complement), $V_{OS} = (V_{OA} + V_{OB})/2$. For a single-ended output $V_{OS} = (V_{OH} + V_{OL})/2$.

V_{OSH} The Output Offset Voltage or Output Common Mode When The Differential Output is in the "HIGH" State
This voltage is defined as the voltage midpoint of the differential output in the "high" state. For output signals V_{OA} (true) and V_{OB} (complement),
$V_{OSH} = (V_{OHA} + V_{OLB})/2$.

V_{OSL} The Output Offset Voltage or Output Common Mode When The Differential Output is in the "LOW" State
This voltage is defined as the voltage midpoint of the differential output in the "low" state. For output signals V_{OA} (true) and V_{OB} (complement),
$V_{OSL} = (V_{OHB} + V_{OLA})/2$.

V_{SS} Negative Power Supply Voltage

V_{T+} Positive-Going Voltage Threshold
The voltage level at which an input will recognize a logic low-to-high transition when the voltage level has been increased from a value below V t-(min).

V_{T-} Negative-Going Voltage Threshold
The voltage level at which an input will recognize a logic high-to-high transition when the voltage level has been decreased from a value above V t+(max).

ΔV_{OD} The Change in Differential Voltage Between Complementary States
The voltage change is defined as the magnitude difference of V_{ODH} and V_{ODL}.

ΔV_{OS} The Change in Output Offset Voltage Between Complementary Outputs for Differential Signals
The voltage change is defined as the magnitude difference of V_{OSH} and V_{OSL}.

AC SWITCHING PARAMETERS and WAVEFORMS

t_{PHL} Propagation Delay HIGH-TO-LOW
The time delay from an input signal to the HIGH-TO-LOW transition of an output signal (see Figures 9-1 through 9-4).

t_{PLH} Propagation Delay LOW-TO-HIGH
The time delay from an input signal to the LOW-TO-HIGH transition of an output signal (see Figures 9-1 through 9-4).

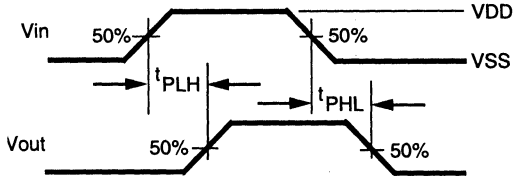

Figure 9-1 Non-Inverting CMOS Input Buffers, Output Buffers and Internal Macros

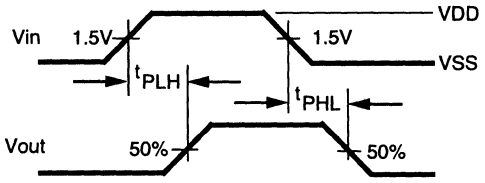

Figure 9-2 Non-Inverting TTL Input Buffers

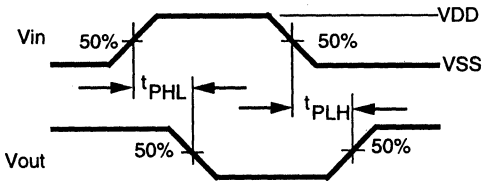

Figure 9-3 Inverting CMOS Input Buffers, Output Buffers and Internal Macros

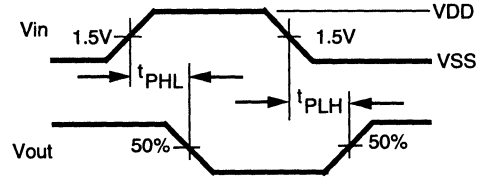

Figure 9-4 Inverting TTL Input Buffers

t_r Signal Rise Time
LOW-TO-HIGH logic transition time on a signal, measured from the 10% to the 90% points of the waveform (see Figure 9-5).

t_f Signal Fall Time
HIGH-TO-LOW logic transition time on a signal, measured from the 90% to the 10% points of the waveform (see Figure 9-5).

t_{PHZ} Output Disable Time HIGH-TO-Z
The time delay encountered for the output to switch from a "high" state or logical '1' to a high-impedance state after the output enable signal is disabled. For internal macros this measurement is independent of load capacitance (Figure 9-6). Output is guaranteed to be in high-impedance state as soon as signal at E1 and E2 reaches threshold. External outputs are dependent on load capacitance. (Figure 9-7).

t_{PLZ} Output Disable Time LOW-TO-Z
The time delay encountered for the output to switch from an active LOW to a high-impedance state after the enable signal is negated. For internal macros this measurement is independent of load capacitance (Figure 9-6). Output is guaranteed to be in 3-state as soon as signal at E1 and E2 reaches threshold. External outputs are dependent on load capacitance.(Figure 9-7).

t_{PZH} Output Enable Time Z-TO-HIGH
The time delay for an output buffer to switch from a high-impedance state to a "HIGH" state after the output enable signal is asserted (see Figures 9-6 and 9-7).

t_{PZL} Output Enable Time Z-TO-LOW
The time delay for an output buffer to switch from a high-impedance state to a "LOW" state after the output enable signal is asserted (see Figures 9-6 and 9-7).

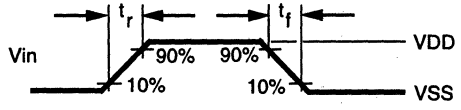

Figure 9-5 Signal Rise and Fall Time Measurements

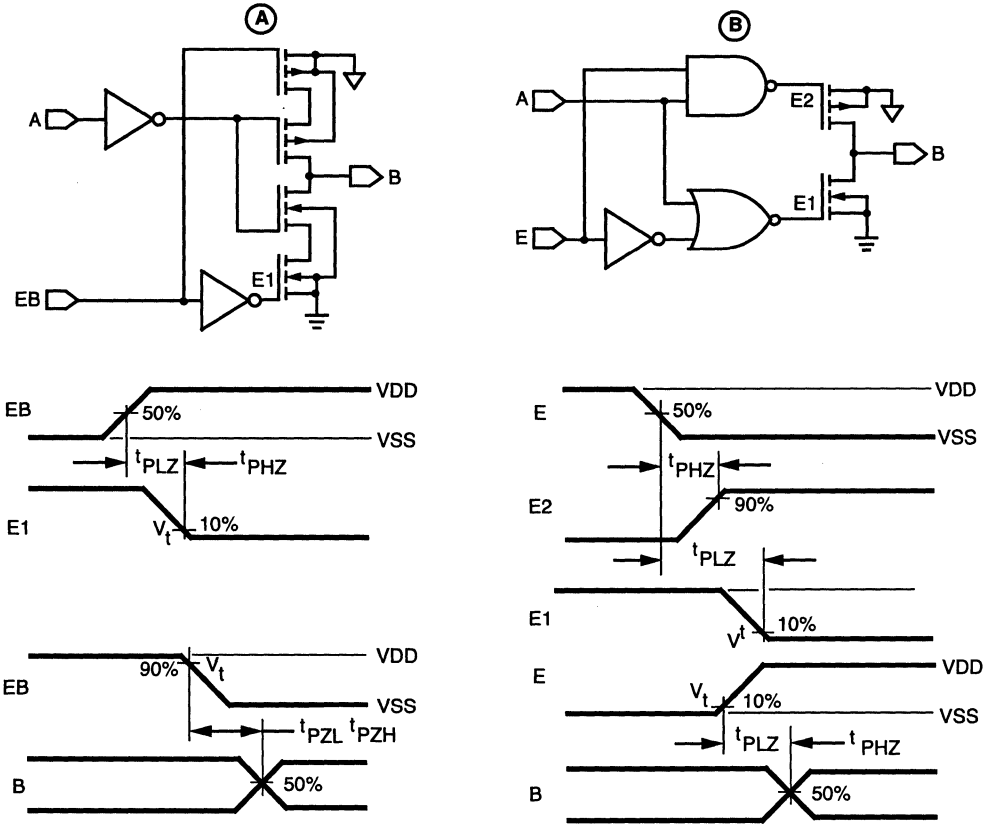

Figure 9-6 Internal Cell HIGH-Impedance State Measurements and Example Circuits for A) Active LOW Enable, and B) Active HIGH Enable Macros

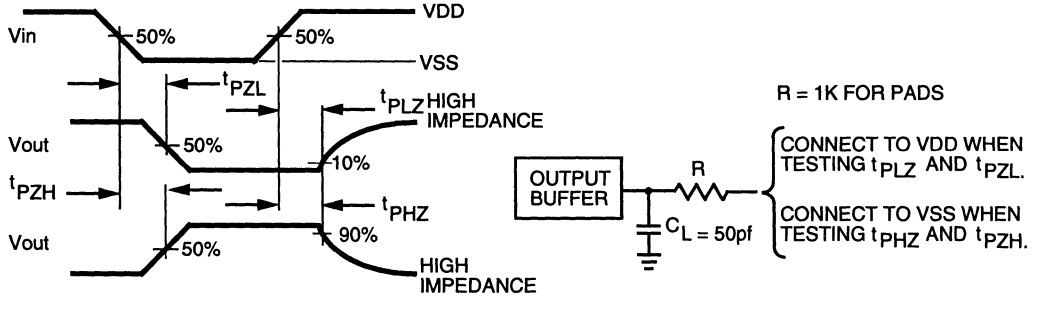

Figure 9-7 Output Buffer HIGH-Impedance State Measurement and Test Circuit

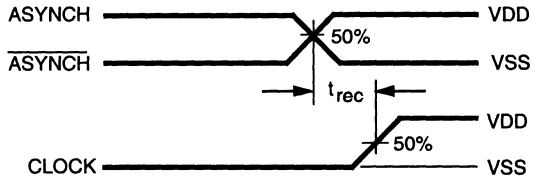

Figure 9-8 Recovery Time Measurement

t_{rec} Recovery Time
The minimum time required between the disabling edge of an asynchronous signal (set, reset, load) and the enabling edge of a synchronous signal (clock) (see Figure 9-8).

t_h Hold Time
The minimum time during which data to be recognized must remain constant after the specified edge of the control signal (usually the clock) to ensure proper data recognition (see Figure 9-9).

t_{su}Setup Time
The minimum time during which data to be recognized must remain valid prior to the specified edge of the control signal to ensure proper data recognition (see Figure 9-9).

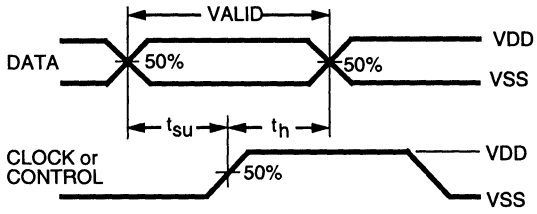

Figure 9-9 Setup and Hold Time Measurements Between Data and Clock/Control Signals (Active Rising Edge Example)

$t_{w(H)}$Pulse Width (HIGH)
The minimum time between the 50% point of the rising edge and the 50% point of the falling edge of a pulse (see Figure 9-10).

$t_{w(L)}$Pulse Width (LOW)
The minimum time between the 50% point of the falling edge and the 50% point of the rising edge of a pulse (see Figure 9-10).

f_{max}Maximum Operating Frequency
The maximum rate at which clock pulses meeting the clock requirements (i.e., t_w, t_f, 50% duty cycle) may be applied to a sequential circuit. Above this frequency the device is not guaranteed to function.

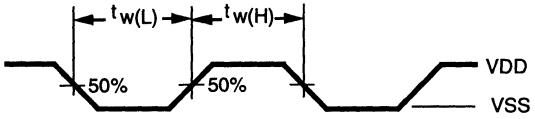

Figure 9-10 Switching Waveforms Showing tw(L) and tw(H) Measurements

RAM-MACROCELL SWITCHING CHARACTERISTICS DEFINITIONS

t_{AA}Address Access Time
The propagation delay time between a valid address and data accessed by that address being present and valid at the output. (see Figures 9-11 and 9-12).

t_{OH}Output Hold Time
The time in which output data will remain present and valid, following a change on the address inputs, which access the data. (Figure 9-11).

t_{AWB} Address to Write Enable Setup Time
The minimum time between changes on the address inputs and assertion of the Write Enable line. (see Figure 9-12).

t_{ASU} Address to Write Enable Setup Time
The minimum time between changes on the address inputs and deassertion of the Write Enable line. (see Figure 9-12).

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tWP Write Enable Pulse Width

The minimum time the Write Enable line must remain in either the Logic low or Logic high state. (see Figure 9-12).

t_{WDO} Write Enable Assertion to Data Out

The propagation delay between assertion of the Write Enable line and internal data reaching, and being valid, at the output. (see Figure 9-12).

t_{DDO} Data In to Data Out

The propagation delay between changes on the data inputs and that changed data reaching, and being valid, on the data output; write operation only (see Figure 9-12).

t_{DSU} Data In Setup Time

The minimum time between changes on the data inputs and the end of the write operation (negation of Write Enable line). (see Figure 9-12).

t_{AH}Address Hold Time

The minimum time the address inputs must continue to be held in their same Logic state following completion of the write operation (negation of Write Enable line). (see Figure 9-12).

t_{DH}Data In Hold Time

The minimum time the data inputs must continue to be held in their same Logic states following completion of the write operation (negation of Write Enable line). (see Figure 9-12).

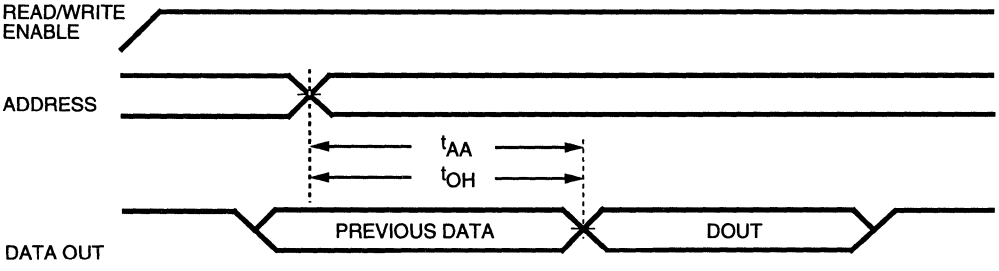

Figure 9-11 RAM Read Cycle

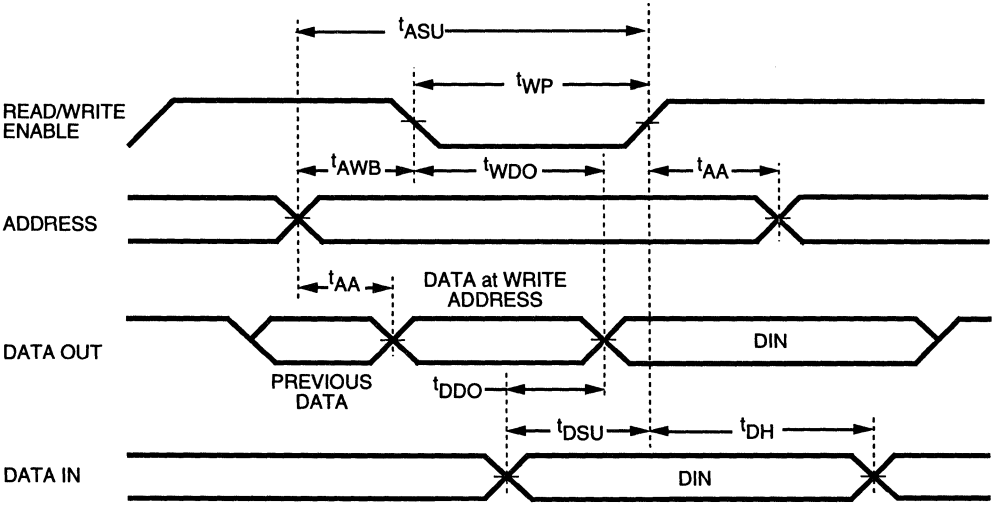

Figure 9-12 RAM Write Cycle

9

DIFFERENTIAL VOLTAGE CHARACTERISTICS AND DESCRIPTION

The difference (D = A - B) between two complementary signals is the differential voltage. (see Figure 9-13).

Waveform Definition for Differential Signals

The terminology used for describing differential signals can be described by observing the waveforms shown in Figure 9-13. The signals can be either outputs or inputs with the voltage levels separated by a "/" to distinguish between output/input. A single-ended signal consists of one output connected to one or more logic inputs such as signal V_{OA} or V_{OB} when used independent of each other. For the example shown in Figure 9-13, the voltage per pin of output V_{OA} or V_{OB} is 1 Vpp (volts peak-to-peak). If the V_{OA} and V_{OB} signals are the complement of each other at all times, including during switching, then the signals together make up a differential pair or differential signal. The differential voltage is defined as the difference in the voltages between the differential pair. Signal V_{OD}/V_{ID} is the resulting differential output/input signal when signal V_{OB}/V_{IB} is subtracted from signal V_{OA}/V_{IA}.

For the example shown in Figure 9-13, the differential output voltage, V_{OD}, is +1.0 volt in the "high" state (V_{ODH}) and -1.0 volt in the "low" state ($-V_{ODL}$) when the V_{OA} and V_{OB} signals have a V_{OH} = 3.1 V and V_{OL} = 2.1 V. The differential output voltage can also be described as a peak to peak voltage such as 2.0 Vpp. Thus, the differential output voltage can be described as ±1.0 volt or 2.0 Vpp. In the specifications, V_{ODH} and V_{ODL} are specified for the differential output voltage with a value equal to 1.0 volt for the example shown.

The differential input voltage is defined similarly. For the example shown in Figure 9-13, the differential input voltage, V_{ID}, is +0.2 volt in the "high" state (V_{IDH}) and -0.2 volt in the "low" state (V_{IDL}) when the signals have a V_{IH} = 2.7 V and V_{IL} = 2.5 V. Thus, the differential input voltage can be described as ±0.2 V or 0.4 Vpp. For differential inputs, the absolute values of V_{IH} and V_{IL} can vary as long as the difference is greater than the specified value for V_{IDH} and V_{IDL} (0.2 V for the example shown) and they are within the input voltage range (V_{IL}min to V_{IH}max) and the input common mode voltage range (V_{ICM-} to V_{ICM+}) of the receiver. In the specifications, V_{IDH} and V_{IDL} are specified for the differential input voltage with a value equal to 0.2 volts for the example shown.

Note:

See SECTION 9 for further definitions of letter symbols and specifications.

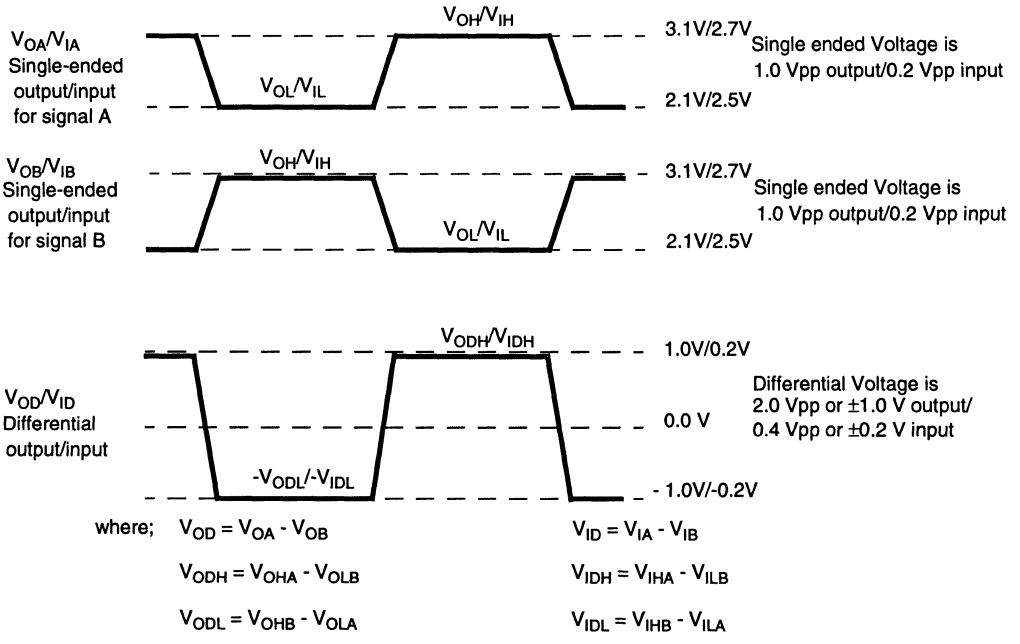

Figure 9-13 Differential Voltage

9

GLOSSARY OF TERMS 10

10 GLOSSARY OF TERMS

SECTION 10. GLOSSARY

ASIC (Application Specific Integrated Circuit)

An IC whose function is specified or designed by the customer including gate arrays, standard cell arrays, etc. Within the scope of this document ASIC refers to gate arrays and customer defined arrays.

Automatic Place and Route

Automated wiring of a gate array to form the components and interconnections which define the function of a specific circuit. The data from place and route is used to define the metallization masks used for the fabrication of an ASIC.

Back-Annotation

To use place and route data (metal interconnect lengths and capacitances) to enable accurate delay and timing simulation of an ASIC circuit.

BGA (Ball Grid Array package)

(see OMPAC)

BIST (Built-in Self Test)

Logic functions which automatically test memories such as RAMs using test-pattern generation, test application, and response evaluation.

Bond (die) Pad

One of many metal connection points that reside along the periphery of the die used to attach a connection between a unique internal I/O port and external package pin.

Burst Pin

Capability of an IC tester to repeat clock pulses to test BIST structures without using large quantities of tester memory.

CAD/CAE (Computer Aided Design and Engineering)

The use of computers to perform any development, design and analysis tasks.

Cavity Up/Cavity Down

Cavity Up (CU) is a package design where the backside of the chip is facing toward the board once the package is mounted, whereas in Cavity Down (CD) the backside of the chip is facing away from the board.

CDA (Customer Defined Array)

Gate array with embedded blocks.

Clock Frequency

The reciprocal of the clock period.

Clock Period

The time delay that exists between all clocked elements when a clock signal is distributed throughout a design.

Clock Skew

The time difference between the arrival of a common clock pulse at two or more devices.

CMTL™ (Current Mode Transceiver Logic)

Motorola developed I/O buffers designed for high-speed, low-power interfacing.

Data Rate

The number of bits of data transferred or processed per second. One bit of data is transferred between sequential elements (flip-flops, registers, etc.) during one clock period, therefore the maximum data rate is equivalent to the clock frequency. For example, a 30 MHz clock results in a maximum 30 Mb/s data rate.

Delay, Maximum

The value specified for the worst-case process, worst-case voltage, and worst-case temperature variations. It may or may not have a worst-case capacitance load associated with it.

Delay, Minimum

The value specified for the best-case process, best-case voltage, and best-case temperature variations. It may or may not have a best-case capacitance load associated with it.

Delay, Typical

The value specified for the typical process, the typical voltage, and the typical temperature variations. It may or may not have a typical capacitance load associated with it.

Design for Testability

A design methodology and discipline that considers test requirements throughout the design cycle and incorporates features that permit thorough testing with minimum effort and maximum fault detection.

Design Release

The transfer of design data (netlist, test vectors, etc.) to Motorola for prototype fabrication. The customer must have successfully completed all design, simulation, and verification phases prior to release.

Die

Silicon "chip" containing micro electronic devices.

Differential Inputs

These are inputs driven by the true and complement input signals.

Differential Outputs

These are outputs driven by the true and complement output of a single macrocell element.

DRC (Design Rules Check)

Automated analysis of technology specific design rules pertaining to the dimensions, spacing and ratios of the various device layers in fabrication.

EDIF (Electronic Design Interchange Format)

An industry standard textural format for describing all types of electronic design information including schematics and symbols.

EIAJ (Electronics Industry Association of Japan)

ERC (Electrical Rules Check)

Automated analysis of technology specific rules pertaining to the use of internal and I/O macrocells for circuit design.

ESD (Electrostatic Static Discharge)

The temporary charging effect of a high-voltage caused by static electricity. ESD is easily generated and often reaches over a thousand volts. ESD can cause damage to sensitive CMOS circuitry if proper handling precautions are not employed.

Fall Time

The time required for an output to transition from the 90% voltage level to 10% of its final output voltage level.

Gate

A unit consisting of 2 p-channel and 2 n-channel transistors used to define the size of individual macrocells and to quantify gate array density.

Gate Array

An arrangement of transistors on a die whose interconnections are defined by the customer to produce a specific logical function.

GTL™ (Gunning Transceiver Logic)

Xerox Co. developed CMOS low-voltage-swing transceiver.

H4C

Refers to the H4C Series of Motorola High Density CMOS macrocell arrays.

H4CP, H4CPlus

Refers to the H4CPlus Series of Motorola High Density CMOS macrocell arrays.

HD, HDC

Refers to the HDC Series of Motorola High Density CMOS macrocell arrays.

Hot Carrier Injection

The phenomena of highly energized carriers entering the gate oxide region and, because of their charge, causing reliability problems for rapid gate switching.

I_{DD}

A measurement of the current leakage of the die when everything is turned "off". If the current leakage is above a certain threshold, you probably have a short somewhere on the die; hardware test culls any die that are above the allowed threshold.

JTAG (Joint Test Action Group)

Developers of boundary scan methodology for testing IC's and boards.

JEDEC (Joint Electronic Device Engineering Council)

K-Factor

A multiplier used in propagation delay and timing calculations. Determines the sensitivity of delay and timing to external factors including capacitive loading, input rise/fall times, etc. See Section 7.

Latch-Up

An abnormal operating condition of CMOS devices where the device stops all function and damage may occur. This is caused by an input of a device momentarily being driven beyond the power supply voltage (VDD). This relative bias condition creates a silicon-controlled rectifier (SCR) through the die, thus causing latch-up.

Layout

See automatic place and route.

LDD (Lightly Doped Drain)

A diffusion process in CMOS device fabrication to minimize hot carrier injection by reducing the electric field across short channel gates.

L_{eff}

Effective gate channel length caused by post-drive lateral diffusion of the drain and source.

LSSD (Level-Sensitive Scan Design)

LSSD aims at reducing the sensitivity of the circuit to ac parameters (including rise/fall times, setup/hold time, and propagation delays) and variation in parameters due to processing variations, physical layout, and operating voltage. LSSD uses dual- and single-port latches for memory and multiphase clocking for synchronization.

MCR (Molded Carrier Ring)

Device used to protect and maintain package pin alignment during handling.

Metal Layer

Layers on aluminum deposited over a gate array in which interconnections between transistors and logic blocks are made.

MicroCool

QFP compatible plastic package with internal heat sink for higher heat dissipation capacity.

Micron

One-millionth (10^{-6}) of a meter.

Netlist

A textual (ASCII) description of an electronic circuit which includes circuit components, interconnections, and specific information related to the design and technology used.

NDA (Non-Disclosure Agreement)

A contract in which the customer agrees to not disclose Motorola proprietary information.

NRE (Non-Recurring Engineering)

A one-time fee charged to customers for materials and services in producing ASIC prototypes.

OACS (Open Architecture CAD System)

A system of workstation software used to design and verify Motorola ASIC designs.

OMPAC™ (Over-Molded Pad Array Carrier)

A package whose pins consist of an array of solder balls.

Operating Frequency, Maximum

Fmax is the maximum rate at which clock pulses meeting the clock requirement (t_w, t_r, and t_f) may be applied to a sequential circuit and have the circuit function properly.

Option

A unique customer ASIC design.

Option Cycle Time:

The time required for Motorola to complete the manufacture of an ASIC

Pad Pitch

The distance (in microns) between the midpoints of adjacent I/O bond pads.

PCI (Peripheral Component Interconnect)

A high-performance local-bus standard used to interface with high-speed peripherals.

Physical Database

Electronic files which describe all process layers in the fabrication of a gate array. May also be used in describing customer design specific data.

Poly (Polysilicon, Polycrystalline silicon)

Conductive material in CMOS device fabrication used for gates and transistor interconnection.

Propagation Delay

The amount of time a circuit takes to logically change its outputs due to a change in inputs. It also refers to the amount of time it takes a signal to travel over a length of metal interconnect.

Primary Cell

The basic architectural block of a CMOS array consisting of a group of four p-channel and four n-channel transistors.

PECL (Pseudo-ECL)

Refers to CMOS functions which comply with ECL voltage levels.

QFP (Quad Flat Package)

A surface mount, four sided gullwing leaded package which conforms to EIAJ/JEDEC. See Section 4.

Recovery Time (t_{rec})

The time between the disabling edge of an asynchronous signal (set, reset and load) and the enabling edge of a synchronous signal (clock).

Rise Time (t_r)

The time required for an output to transition from the 10% voltage level to 90% of its final output voltage.

Scan Design

A design-for-test methodology in which all sequential elements (flops, latches, etc.) are multiplexed such that in test mode data path chains are created and monitored.

Scan Pins

Connections on a tester capable of high speed scan testing.

Schematic Capture

a design-for-test methodology in which all sequential elements (flops, latches, etc.) are multiplexed such that in test mode data path chains are created and monitored.

Sea-of-Gates

A gate array architecture in which no channels for device interconnections exist. Interconnections are provided by multiple conductive layers above the gate array.

Setup Time

The minimum time during which data to be recognized must remain constant prior to the specified edge of the control signal to ensure proper data recognition.

Skew

The difference in delay between two parallel signal paths.

Test Vectors

Input stimulus specially prepared to test ASIC prototypes on production test equipment.

Test Verification

The process of proving the effectiveness of a set of test vectors toward correct operation of the circuit.

Turnkey

Engineering services an ASIC manufacturer provides (for a fee) to perform tasks normally required of the customer to design an ASIC application.

UTIC (Universal Test Interface Code)

Developed by Motorola.

UTIC Language

UTIC is a language for describing device stimulus, expected response, parametric test information and package information. This information is used as input to automatic test program generation software and the Verilog simulator.

Via

A vertical length of metal deposited through a small hole in oxide used to electrically connect two layers of metal.

Wirebond

A step in die packaging where thin wires are bonded between die I/O pads and package pads.

APPLICATION NOTES

APPENDIX A

A

APPENDIX

MOTOROLA
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APPLICATION NOTE

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IEEE Std. 1149.1 Boundary Scan for H4C™ Arrays

With H4CPlus™ Supplement

Prepared by: Roy Jones and Nick Spence

Edited by: Clarence Nakata

Application Specific Integrated Circuits Division, Chandler AZ

Table of Contents **Page**

1. Introduction

This application note describes how IEEE standard boundary scan, commonly referred to as "JTAG," has been implemented on Motorola's H4C family of sub-micron CMOS gate arrays. The user is assumed to have a working knowledge of JTAG boundary scan. For background information refer to the IEEE specification entitled "Standard Test Access Port and Boundary-Scan Architecture, IEEE Std. 1149.1-1990," and to the textbook entitled "The Test Access Port and Boundary-Scan Architecture" by Maunder and Tulloss, published by the IEEE Computer Society Press.

Section 2. describes the macros which have been added to the H4C library to facilitate designing boundary scan circuitry into an H4C gate array.

Section 3. describes how the JTAG clock and control signals are distributed around the chip periphery to each pin's boundary scan cell (BSC). The design constraints associated with the distribution of these signals are also described.

Section 4. describes how to add boundary scan to a chip whose system logic has been designed using conventional scan techniques. Mustang™, Motorola's scan ATPG (Automatic Test Pattern Generation) tool, is used to test the JTAG circuitry as well as the system scan circuitry.

Section 5. presents an example JTAG circuit and describes the process the designer must go through to establish the chip pin-out. The constraints described in Section 3.0 must be taken into consideration.

Section 6. describes the CAD design flows used when designing an H4C array which incorporates JTAG boundary scan.

Appendix A lists the ERC (Electrical Rule Checker) rules that are specific to JTAG circuitry. The majority of these rules are associated with the design constraints described in Section 3.

Appendix B provides background information relevant to the "Mustang-Compatible JTAG" discussed in Section 4.

Appendix C describes how to build the EDIFMERGE "Attribute file" for JTAG designs using Synopsys logic synthesis.

Appendix D provides H4CP specific procedures.

2. H4C JTAG Macro Descriptions

Technical data, including logic diagrams, for all JTAG macros in the H4C library can be found in the H4C Series Design Reference Guide. These macros have been placed in three categories in the descriptions that follow: I/O macros, core macros and special purpose macros.

2.1 I/O Macros

I/O macros include the input, output and bidirectional boundary scan cells. The JTAG boundary scan logic associated with these macros is diffused into the peripheral I/O sites. The JTAG logic in a given I/O site is used only if a JTAG BSC macro is instantiated at the package pin bonded to that I/O site.

Non-JTAG hi-drive output and bidirectional macros have always carried a "hi-drive" property to differentiate them from their normal-drive counterparts. However, hi-drive versions of the JTAG output and JTAG bidirectional macros have no such hi-drive property. Instead, there is a separate macro for each JTAG hi-drive so that the timing of these macros can be modeled correctly.

2.2 Core Macros

Macros residing in the core of the array include the Bypass Register (BPREG), Device Identification Register (IDREG), Instruction Register (MC_IREG4), and TAP Controller (FMC_TAPC).

The IDREG and BPREG are hard macros in the H4C library. Motorola will assign device identification codes according to the following format:

```
Bit #:   31-28 27---22  21----------1211----------0
Value:   VVVV 000111  DDDDDDDDDD000000011101
```

where
Bits 31-28: version number assigned by Motorola ASIC
Bits 27-22: unique number assigned to Motorola ASIC
Bits 21-12: sequence number assigned by Motorola ASIC
Bits 11-0: unique number assigned to Motorola Inc.

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The MC_IREG4 is a soft macro; it consists of a schematic capture symbol (or Verilog HDL module) which is comprised of individual gate and flip-flop hard macros, which are placed and routed individually by GateEnsemble™. There is no fixed layout for the MC_IREG4 as an entity. A functional diagram of the MC_IREG4 is shown in Section 4.3, Figure 4-2.

The FMC_TAPC is a firm macro; it is like a soft macro in that it is comprised of, and modeled as, individual gate and flip-flop hard macros. Unlike a soft macro, a firm macro such as the FMC_TAPC has been placed and routed as a single entity by Gate Ensemble. Consequently, both the internal metal interconnect and timing of a firm macro are fixed and do not change when the chip is laid out. A functional diagram of the FMC_TAPC is shown in Figure B-4 in Appendix B, which discusses this macro in detail.

2.3 Special Purpose Macros

2.3.1 TAP macros: TCK, TMS, TRSTB, TDI, TDO and TDOA.

TCK, TMS, TRSTB and TDI are simply input buffers with no BSC logic. Each must be used at the pin driven by the JTAG signal of the same name.

A functional diagram of the TDO macro is shown in Figure 2-1. The 'IR' port receives scan data from the TDO port of the Instruction Register. The 'DR' port receives scan data from whichever JTAG data register is activated by the current JTAG instruction. Therefore the multiplexer contained in the TDO macro selects either the Instruction Register or the currently active JTAG data register to be shifted out through the TDO pin.

The TDO macro is used with the "small array" scheme for distribution of the JTAG control signals. (See Section 3.3.)

The TDOA macro is functionally identical to TDO. TDOA is used with the "large array" scheme for distribution of the JTAG control signals. (See Section 3.2.)

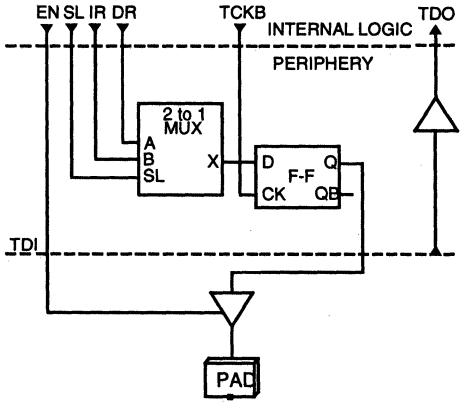

Figure 2-1 TDO Macro (TDO, TDOA)

2.3.2 ENSCANI/J/P

The ENSCAN BSC's are used to drive the enable port of 3-state bidirectional and output BSC's. The ENSCANI, ENSCANJ, and ENSCANP are functionally identical. The differences among the three are:

ENSCANJ must reside on a non-power I/O site.

ENSCANP must reside on a power I/O site.

ENSCANI must reside in the array core.

In the example of Figure 2-2 an ENSCANP supplies the 3-state enable to an output bus. The BSEN input is driven from the core by the system 3-state enable signal, and the OEN output feeds into the core where it can be buffered if necessary before driving the EN inputs of the 3-state output buffers.

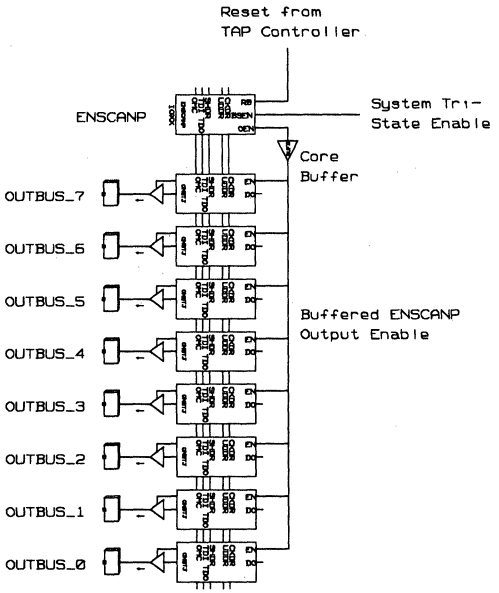

Figure 2-2 ENSCANP Driving 3-State Enable of 8-bit Output Bus

If an ENSCANI had been used instead, it would go at the end of the BSC scan chain closest to TDO as shown in Figure 2-3. The BSC scan data path enters the core through a port on the TDO/A macro, passes through all ENSCANI's, then gets multiplexed with the scan paths from all other JTAG data registers before passing to the DR port of the TDO macro on its way off chip. **(Note that test data must shift counterclockwise through the BSC's around the periphery of the chip.)** ENSCANI's in the core receive CKDR, SHDR, UDDR directly from the FMC_TAPC, and OMC directly from the MC_IREG4 decode logic, before these signals enter the I/O area for distribution to the peripheral BSC's.

It is recommended that ENSCANI's be used only if there are no power sites or unused I/O sites available on which to place ENSCANP's or ENSCANJ's.

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2.3.3 TDBUF(P)

If consecutive peripheral BSC's are separated by more than seven I/O sites, a TDBUF or TDBUFP buffer macro must be inserted between them since a BSC's TDO output has limited drive strength. The TDBUF(P) must not be more than seven I/O sites away from the BSC driving it.

2.3.4 I/O BSC Control Signal Buffers

These are the buffers that distribute CKDR, SHDR, UDDR, IMC and OMC to the peripheral BSC's. These buffers are described in detail in Section 3.0, "JTAG Clock & Control Signal Distribution."

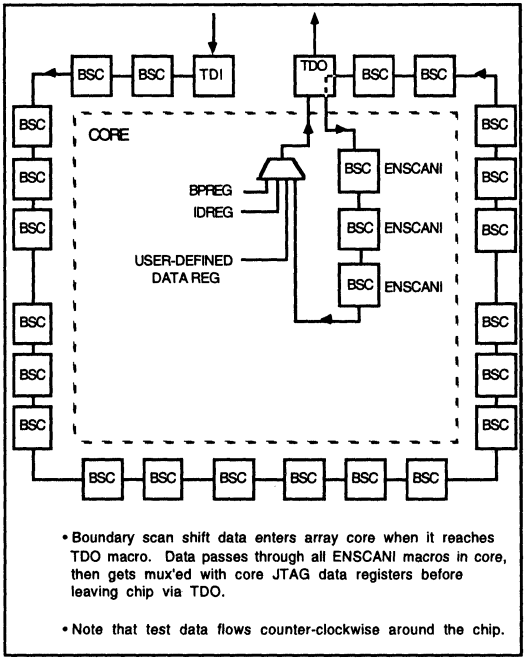

Figure 2-3 Position of ENSCANI 3-State Enable Macros within I/O Boundary Scan Register

3. JTAG Clock & Control Signal Distribution

3.1 Overview

On Motorola's sub-micron H4C arrays the JTAG boundary scan cells are diffused into the periphery, or I/O area, of the chip. The advantages realized, as compared to implementing the BSC's with core macros, are as follows:

1. Area savings
   i) 100% utilization in the periphery versus 60-70% in the core (i. e., no unused gates in the periphery).
   ii) transistor sizes can be optimized to their small, non-varying loads
   iii) interconnect between BSC's is done by abutment, minimizing wire length. For these reasons, diffusing the BSC's into the I/O area conserves a significant amount of chip area compared to implementing the BSC's in the array core, even though the chip I/O area is ~20% larger than it would be if it did not include built-in JTAG logic.
2. There is less additional data path delay due to the mux in the input BSC's since it has been optimized in terms of transistor size and minimum wire interconnect.
3. There are no distribution "trees" for the BSC control signals to increase routing congestion in the core.
4. RAM and MPU diffused blocks don't interfere with the peripheral distribution "rings" for these control signals, preventing increased signal skew.
5. Hold time violations cannot occur when shifting the boundary scan register since all BSC's share a common clock net.

The five JTAG clock and control signals are CKDR, SHDR, UDDR, IMC and OMC. Two methods are provided for distributing these signals to the boundary scan cells located in the periphery of H4C arrays. The "large or high speed array" scheme can be used to maximize performance on any array size, but it must be used on the larger arrays (H4C086 and above) to ensure that edge-rate limits are not violated on the peripheral clock and control lines, which have a large number of BSC loads. The "small or low speed array" scheme is more simply implemented and can be used on smaller arrays which have no such edge-rate problem (H4C057 and below), when maximum performance is not required. The "large or high speed array" scheme should enable the boundary scan circuitry to operate at > 25Mhz.

In Figures 3-1 to 3-6, a dotted line marks the boundary between the core and periphery of the array. All of the special buffers for the JTAG clock and control signals reside in power sites or unused I/O sites in the periphery in order to:

i) maximize the drive capability of these buffers by utilizing the large transistors that normally drive off-chip, and to
ii) facilitate optimum buffer placement to achieve:
   a) minimum insertion delay for each signal,
   b) minimum skew for each signal between a buffer's nearest and farthest BSC loads, and
   c) minimum SHDR-to-CKDR skew and CKDR-to-UDDR skew at any given BSC.

Use of the "P" versions of these buffers allows them to be placed on power sites, which conserves I/O sites for other uses such as hi-drive outputs.

For packages with highly inductive leads HSPICE simulations have shown large voltage spikes on OUTVDD and OUTVSS (the output driver power and ground buses) due to simultaneously switching outputs (SSO). These spikes can couple to the outputs of "quiet" (inactive) drivers. For this reason the JTAG buffers are powered from INPVDD/INPVSS

A

(the core power and ground buses), since they drive BSC's which are also powered from INPVDD/INPVSS. These buffers are also slew-rate controlled in order to inject as little switching noise as possible onto INPVDD and INPVSS. The JTAG buffers are all roughly equivalent to an ON4S4 output buffer.

3.2 Large or High Speed Arrays

3.2.1 CKDR Distribution

Because the CKDR ring must encircle the entire chip, the resistance of the metal can be several hundred ohms. The same is true of the control lines as well. As a result, one very large buffer cannot drive the ring without suffering severe performance loss in terms of long prop delays and edge-rates at the more distant BSC's. A much better approach is to use multiple, distributed buffers to drive the ring. As shown in Figure 3-2, the TAP controller drives a CKDRMID buffer, which in turn drives one CKDRCC1 and one CKDRCC2 buffer via an "extra" ring. The CKDRCC1 and CKDRCC2 each drive roughly half of the JTAG I/O cells on the chip via the CKDR ring. Because these two buffers are placed diametrically opposite to each other, only half of the extra ring is needed to distribute CKDR to them. By detaching the unneeded half of the extra ring, metal capacitance on this net is greatly reduced and substantial speed improvement is realized. In addition, the Gate Ensemble place and route software can correctly model metal interconnect resistance and capacitance (RC's) on this net only if it is not a closed loop. (Gate Ensemble must see only one path from a net's driver to any given load on that net.) There is a physical cut in the extra ring within the CKDRCC1 and CKDRCC2 macros such that detachment of the unneeded half of the extra ring is accomplished automatically when these macros are placed.

There is a physical cut in the CKDR ring within the TDOA macro. However, closing the CKDR ring on the opposite side of the chip from TDOA is important because it guarantees that, over any range of operating conditions, there will never be race conditions/hold time violations during shifting of the I/O boundary scan register. This is true due to the fact that all I/O BSC's share a common clock (CKDR) net. Nor is there a "bus contention" problem on the CKDR ring, due to the wide separation (roughly two sides of the chip) and minimal skew between the CKDRCC1 and CKDRCC2 buffers which drive this ring. However, Gate Ensemble cannot correctly model distributed RC's for nets driven by more than one source if these sources are active simultaneously. The solution is to capture the schematic, or write the HDL circuit description, such that, as in Figure 3-1, CKDRCC1 drives all BSC's on CKDRNET1 and CKDRCC2 drives all BSC's on CKDRNET2, so that the CAD system actually sees a gap in the ring. The performance of the CKDR ring is identical with or without the gap under the following conditions (refer to Figure 3-1):

i) branches (a) and (c) are perfectly balanced in terms of number of loads and length of metal interconnect

ii) branches (b) and (d) are perfectly balanced in terms of number of loads and length of metal interconnect

iii) CKDRMID is perfectly centered between CKDRCC1 and CKDRCC2.

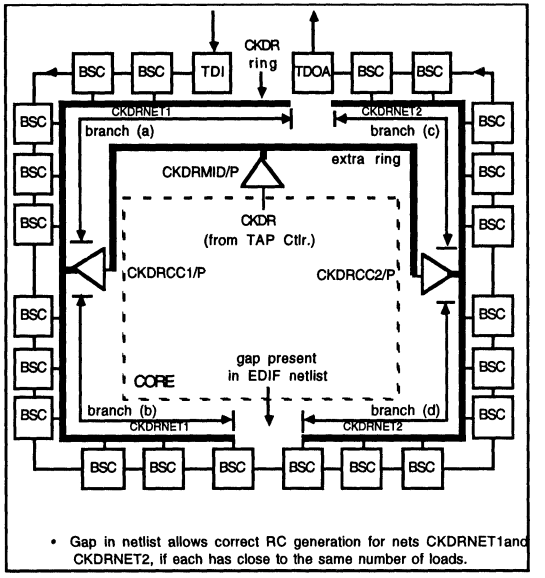

Figure 3-1 CKDR Distribution (Netlist Interconnect for Large or Fast Arrays)

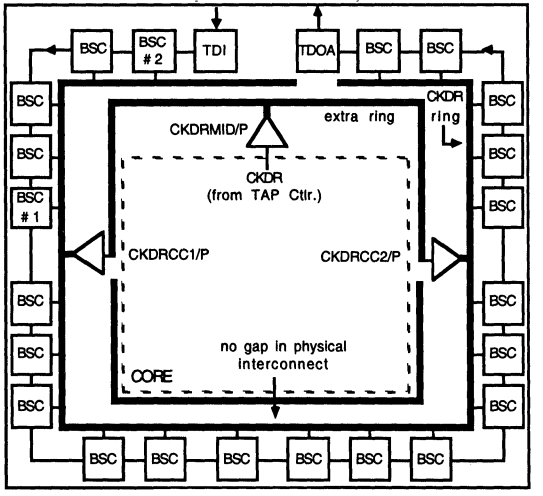

Figure 3-2 CKDR Physical Distribution (Physical Interconnect for Large/Fast Arrays)

In reality, the ASIC designer will not be able to achieve this perfect balance. However, RC's for loads on the CKDR ring, which has no gap in silicon, can be calculated within 5% error by Gate Ensemble if:

iv) the number of loads on branch (a) is within 15% of the number of loads on branch (c)

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v) the number of loads on branch (b) is within 15% of the number of loads on branch (d)

vi) the number of I/O sites between CKDRMID and CKDRCC1 is within 15% of the number of I/O sites between CKDRMID and CKDRCC2.

ERC errors are generated if the above conditions are not met. In addition, ERC warnings are generated if the following two conditions are not met:

vii) the number of loads on branch (a) is within 15% of the number of loads on branch (b)

viii) the number of loads on branch (c) is within 15% of the number of loads on branch (d)

Simulation accuracy does not suffer if (vii) and (viii) are violated, therefore the chip designer may choose to ignore these two ERC warnings. However best performance is achieved by adhering to these two conditions.

Note: Since the gap in Figure 3-1 is not a gap in silicon, it does not correspond to any particular I/O site and therefore its placement is not constrained by the availability of an unused I/O site. The designer has complete freedom as to where this gap is "placed," which is done by connecting some BSC's to CKDRCC1 and the others to CKDRCC2 as in Figure 3-1. Consequently, the imbalance between the number of loads on CKDRNET1 and the number of loads on CKDRNET2 should never be greater than one (which would occur if there are an odd number of peripheral JTAG macros driven by CKDR).

CKDR, SHDR, UDDR and OMC are routed within the core directly from the TAP Controller to ENSCANI bidirectional enable BSC's, which reside in the core.

3.2.2 SHDR, UDDR Distribution

SHDR and UDDR use a distribution scheme which is different from the CKDR scheme, which was able to make use of the extra ring. SHDR will be used for illustration (see Figure 3-3).

The TAP controller drives two SHDR buffers, each of which drives roughly half of the JTAG I/O cells on the chip via the SHDR ring. Gap 1 and gap 2 are both actual physical cuts in the SHDR ring, unlike the gap in the CKDR ring. As a result the ASIC designer does not need to balance the number of BSC loads on nets 1 and 2 in order for Gate Ensemble to correctly model the distributed RC's for these loads. Gap 1 is designed into the TDOA macro. To create gap 2 the ASIC designer must place a special "ISO" macro on a power or I/O site near the point diametrically opposite from the TDOA macro. This ISO macro cuts the SHDR and UDDR rings. A break in these lines does not cause timing problems as it would in the CKDR line, and it frees the designer from the need to balance loads on these lines as he has to do on CKDR. Even so, ERC warnings are generated if the following two conditions are not met:

i) the number of loads on branch (a) is within 15% of the number of loads on branch (b)

ii) the number of loads on branch (c) is within 15% of the number of loads on branch (d)

As stated above, simulation accuracy does not suffer if (i) and (ii) are violated, therefore the chip designer may choose to ignore these two ERC warnings. However best performance is achieved by adhering to these two conditions. The ERC warnings are simply to alert the designer that his buffer placement will not achieve minimum insertion delay and maximum shift speed. **Note: The ISO macro has nothing to do with the CKDR gap in Figure 3-1.**

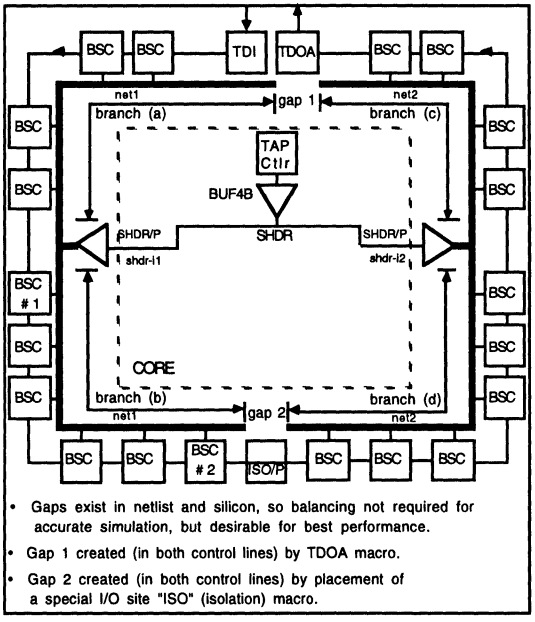

Figure 3-3 SHDR, UDDR Distribution (Large/Fast Arrays)

3.2.3 IMC, OMC Distribution

The distribution scheme for IMC and OMC is similar to the scheme for SHDR. The difference is that the SHDR line is cut by the TDOA and ISO macros, whereas the IMC and OMC lines are cut by the CKDRCC1 and CKDRCC2 macros. The IMCDR and OMCDR buffers can now be placed in a different area from the SHDR and UDDR buffers (see Figures 3-3 and 3-4), relieving buffer congestion so that as many JTAG buffers as possible can be placed on power sites, allowing more efficient use of the I/O sites.

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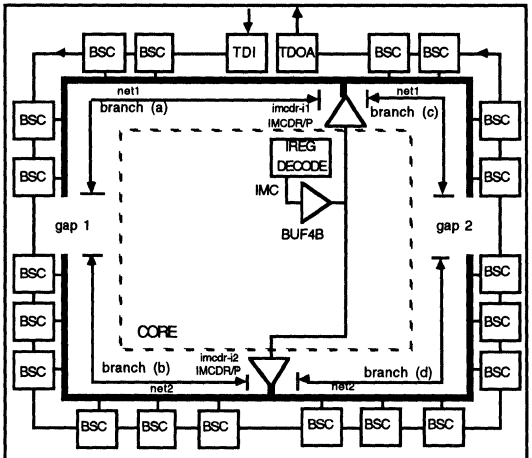

Figure 3-4 IMC, OMC Distribution (Large/Fast Arrays)

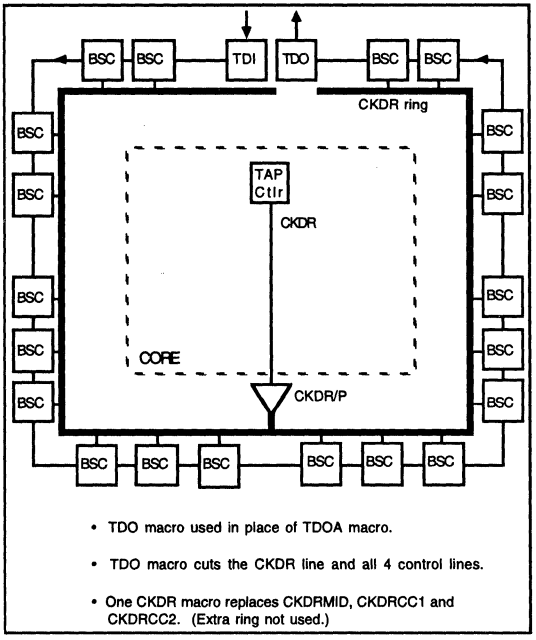

Figure 3-5 CKDR Distribution (Small/Slow Arrays)

3.3 Small or Low Speed Arrays

3.3.1 CKDR Distribution

As shown in Figure 3-5, the TAP controller drives one CKDR buffer, which drives the CKDR ports of all JTAG I/O cells on the chip via the CKDR ring. The CKDRCC1 and CKDRCC2 buffers, and therefore the extra ring, are not needed. Consequently there is no balancing of loads to be done, as for large or high speed arrays. There is a physical cut in the CKDR ring within the TDO macro so that Gate Ensemble can correctly model distributed RC's for BSC loads on this ring. The netlist interconnect matches the physical interconnect, unlike the large/high speed array scheme. The TDO macro replaces the TDOA macro used in the large/high speed array scheme.

3.3.2 SHDR, UDDR, IMC, OMC Distribution

SHDR, UDDR, IMC and OMC all use the same distribution scheme, which is also the same as the CKDR scheme since the extra ring is not being used. As shown in Figure 3-6, the TAP controller drives one SHDR buffer which drives the SHDR ports of all JTAG I/O cells on the chip via the SHDR ring. The ISO macro is not used so that gap 2 in the SHDR and UDDR lines (see Figure 3-3) does not exist. Likewise, gaps 1 and 2 in the IMC and OMC lines (see Figure 3-4) do not exist, since CKDRCC1 and CKDRCC2 are not used in the CKDR scheme. There is only one gap in each control line, and that gap occurs in the TDO macro.

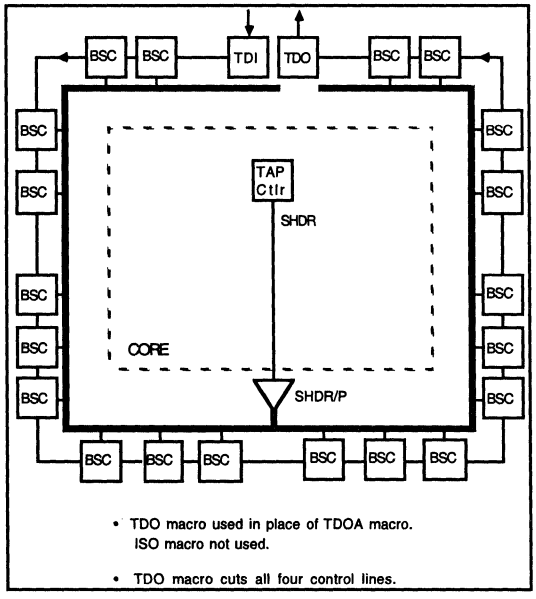

Figure 3-6 SHDR, UDDR, IMC, OMC (Small/Slow Arrays)

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4. Mustang-Compatible JTAG

4.1 Introduction

On the Motorola H4C family of CMOS arrays, JTAG boundary scan circuitry has been designed to be compatible with Motorola's Mustang ATPG product, which was designed to do automatic test pattern generation for conventional scan designs. However, as defined by the IEEE 1149.1 specification, JTAG boundary scan violates several conventional scan design rules. Section 4.0 and Appendix B describe how the JTAG boundary scan circuitry has been implemented on H4C arrays in order to allow it to be tested by Mustang.

The user is assumed to have a working knowledge of Mustang. For more information on Mustang itself refer to Tim Boland's Application Note, number AN1096, entitled "Guidelines for Using the Mustang ATPG System," and to the Mustang User's Guide portion of Motorola's Open Architecture CAD System™ (OACS) documentation.

4.2 Design Overview

Motorola has designed scan-compatibility into the JTAG circuitry in two respects:

1. Special Mustang modeling has been done for the boundary scan cell, which contains a non-scannable latch.
2. The TAP Controller has been modified to include scannable flip-flops, and to satisfy some Mustang timing requirements. For detailed explanations of items 1 and 2 see Appendix B. In addition, the user is responsible for:

- ensuring that no timing problems arise due to clock skews, and
- interconnecting all JTAG circuitry such that Mustang compatibility is maintained.

4.2.1 Handling of Clock Skew

Motorola's H4C arrays use the gated-clock JTAG implementation shown in IEEE 1149.1. That is, the original clock TCK is gated within the TAP Controller and the instruction decoding logic to provide the CKIR, CKDR, UDIR and UDDR signals to the JTAG cells. This can cause skew problems in Mustang test mode, particularly due to the large clock delays to the boundary scan cells. Section 4.3 addresses the prevention of timing problems due to clock skew.

4.2.2 JTAG Circuitry Interconnection

An extra pin, called "MTST" for "Mustang test mode" in this document, must be added to the chip to logically reconfigure the JTAG circuitry when Mustang testing is to be done. When this input is active all circuit elements including the TAP Controller will become scan-compatible, the JTAG TMS pin will be used as the scan/shift enable control signal, and the scan chain connected between the TDI and TDO pins will contain all the flip-flops which are part of the JTAG circuitry. The JTAG logic must also be correctly controlled in Mustang scan mode to ensure that the scan paths are completed (requires that IMC and OMC both be low). Section 4.4 describes in detail how to properly hook-up all JTAG circuitry for Mustang compatibility.

4.3 Handling of Clock Skew

The JTAG design can suffer from clock skew problems during Mustang test mode because the gated clocks (CKIR, UDIR, CKDR's for each data register) must be enabled at the same time. The problems occur when the clock arrives early to one flip-flop causing its output to change before the clock arrives at the next flip-flop. This can result in hold time violations and/or the wrong data being loaded.

The JTAG logic does not suffer from this problem during normal operation because some sections are clocked on the rising edge of TCK while others are clocked on the falling edge, such that input data to each JTAG register always changes on the inactive edge of the clock to that register. For example, a new instruction becomes active when the shadow latches in the instruction register are "clocked" by UDIR, which occurs on the falling edge of TCK. The new instruction drives decode logic which enables CKDR to the appropriate data register (e. g. the Identification Register, Bypass Register or peripheral boundary scan register). These CKDR enable signals change on the falling edge of TCK in order to be stable during the rising edge of TCK/CKDR. Likewise the SHDR and TDI signals, which feed each data register, change on the falling edge of TCK in order to be stable during the rising edge of TCK/CKDR. Also, the flip-flop within the TDO macro is clocked on the falling edge of TCK because its input data, which comes from either the "CKIR" flops in the Instruction Register or from one of the data registers, changes on the rising edge of TCK.

As described above, during normal JTAG operation input data to each JTAG register always changes on the inactive edge of the clock to that register, so that the data is stable during clocking of the state elements. However, when operating in Mustang test mode all flip-flops must clock on the same edge of the clock signal. This can cause problems both during scan operation (the shift in and shift out of scan data) and also during the pulsing of the system or TCK clocks. (A Mustang scan test consists of three parts: shift in of scan stimulus, pulsing of zero or one of the clocks -- referred to as "clock pulse mode," and shift out of the chip's response to the scan stimulus.)

As described in Section 4.4, all JTAG registers will be included in the same scan chain during Mustang testing. Each data register is clocked by its own gated version of CKDR, and the Instruction Register's CKIR and UDIR flops are clocked by CKIR and UDIR respectively. Consequently, the JTAG scan chain is operated by several different clocks which have different insertion delays, creating the potential for skew problems during the scan operation. Skew problems during scanning can be controlled by putting registers whose clocks have longer insertion delays at the beginning of the scan chain. Since the I/O boundary scan register has the slowest clock distribution it should be the first part of the scan chain. Also, if timing analysis shows it to be necessary, delays can be added between flip-flops driven by different clocks.

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In order to prevent skew problems when Mustang pulses the system or TCK clocks, the JTAG clock gating must be altered so that the clock pulse is applied either to the flip-flops that would normally change on the rising edge of TCK or to the flip-flops that would normally change on the falling edge of TCK. This is done by adding a flop to the TAP controller which controls the clock gating only during Mustang clock pulse mode. (This flop is labeled "TCK/TCKB Select Flop" in Figure B-4 of Appendix B.) Putting this flop inside the TAP Controller allows all of the JTAG logic within the TAP controller to remain in a single scan chain.

As shown in Figure 4-1 the Instruction Register UDIR latches have been changed to flops, for the following reasons:

1. to eliminate the undetectable stuck-at-one faults which are present on each latch gate input (for more details see Section B.1 of Appendix B),
2. to enable separate clocking of the UDIR flop, which must change on the falling edge of TCK. The UDIR signal can now be applied separately from the CKIR signal to remove the possibility of skew.

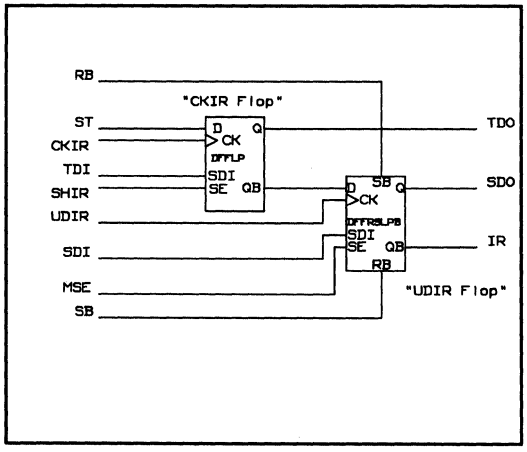

Figure 4-1 Single-Bit Instruction Register Cell (MC_IREG).

The "MC_IREG4" four-bit Instruction Register macro is shown in Figure 4-2. During scan mode CKIR and UDIR are active simultaneously, with CKIR leading UDIR by a few nanoseconds at the output of the TAP Controller. Consequently, to prevent hold-time violations during scan mode, the "UDIR flops" must precede the "CKIR flops" in the JTAG scan chain. For this purpose, SDI and SDO ports are provided on the MC_IREG and MC_IREG4 macros to serve as "Scan-Data-In" and "Scan-Data-Out" for the UDIR flops (see Figures 4-1, 4-2 and 4-3). As shown in Figure 4-3, during Mustang scan mode (MSE high) scan data from the TAP Controller's "TDO" port enters the UDIR flops in the MC_IREG4 via the SDI port. After exiting at SDO, the scan data is fed back to the MC_IREG4 "TDI" port to pass through the CKIR flops. During normal JTAG operation (MSE low), JTAG test data from the TAP TDI pin is passed to the CKIR flops in the MC_IREG4 as required.

Extra delays are included in the scan paths within the MC_IREG4 because it is currently a soft macro. As such, the metal interconnect between its four MC_IREG cells will differ somewhat from layout to layout, potentially causing a small amount of CKIR or UDIR skew between the four cells. The DLY8 macros within the MC_IREG4 add delay in the scan path to compensate for any such skew.

Referring to the Mustang-compatible TAP Controller in Appendix B, Figure B-4, note the inclusion of the following circuitry:

1. A "TCK/TCKB Select Flop" to control the clock gating in Mustang clock pulse mode.
2. An extra delay on TDO to prevent skew problems caused by the early clocking of the flip-flops in the TAP Controller. The TDO signal would normally be passed onto the Instruction Register as shown in Section 4.4. The Instruction Register clock CKIR will arrive later than the clock to the flip-flops in the TAP Controller because of the clock gating circuitry within the TAP Controller.
3. A delay macro in the scan path between the top left flip-flop and the top right flip-flop because these flops have separate clocks which pass through different gating logic. A buffer was also added to the clock for the "TCK/TCKB Select Flop" for similar reasons.

Since the FMC_TAPC Mustang-compatible TAP Controller is a firm macro, its fixed layout guarantees no timing problems will ever arise internal to the FMC_TAPC.

It is very difficult to control clock skew between core/system flip-flops and the boundary scan cells because of the long insertion delay of clock CKDR in the periphery. In order to prevent skew problems from occurring between the JTAG logic and the system logic during Mustang test mode, either:

i) the clock TCK should be different from the system clock, or

ii) circuitry similar to the "TCK/TCKB Select Flop" and "Clock Select" gates in the TAP Controller should be implemented to prevent Mustang from pulsing both TCK and the system clock in the same clock cycle.

It is important that timing analysis be done to verify that no setup or hold time violations occur due to the aforementioned sources of clock skew. Veritime is able to take into account the effects of variations in process/voltage/temperature across a chip.

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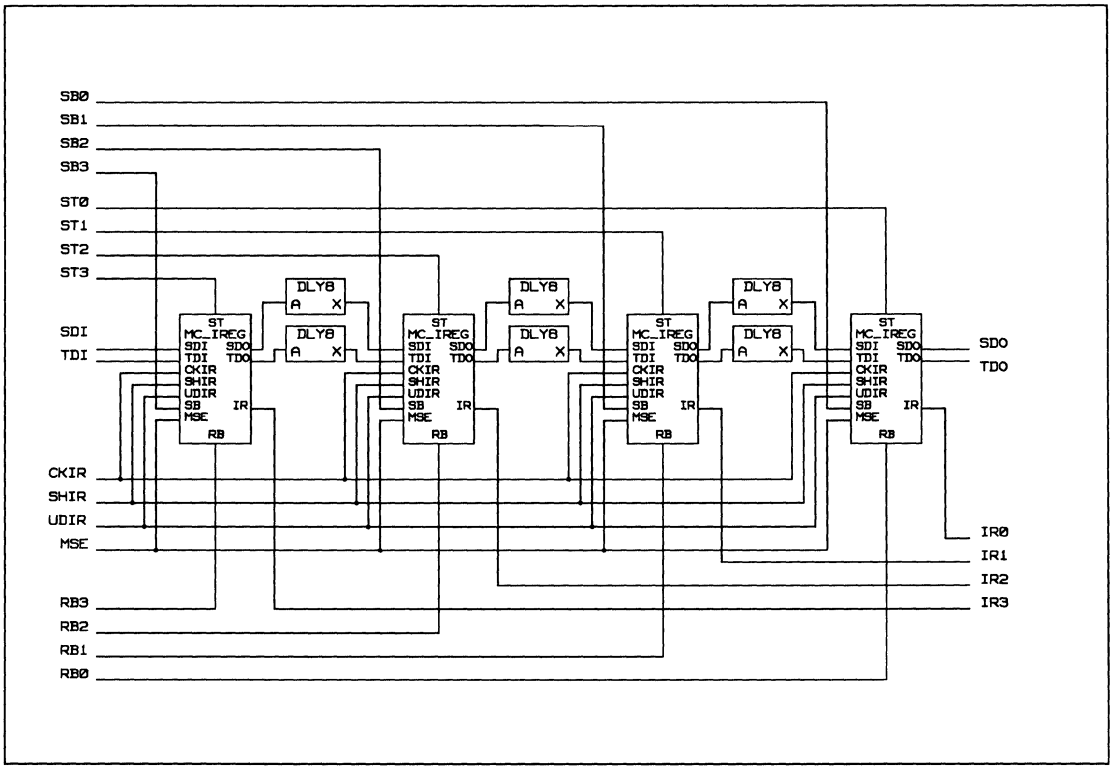

Figure 4-2 MC_IREG4 Functional Diagram

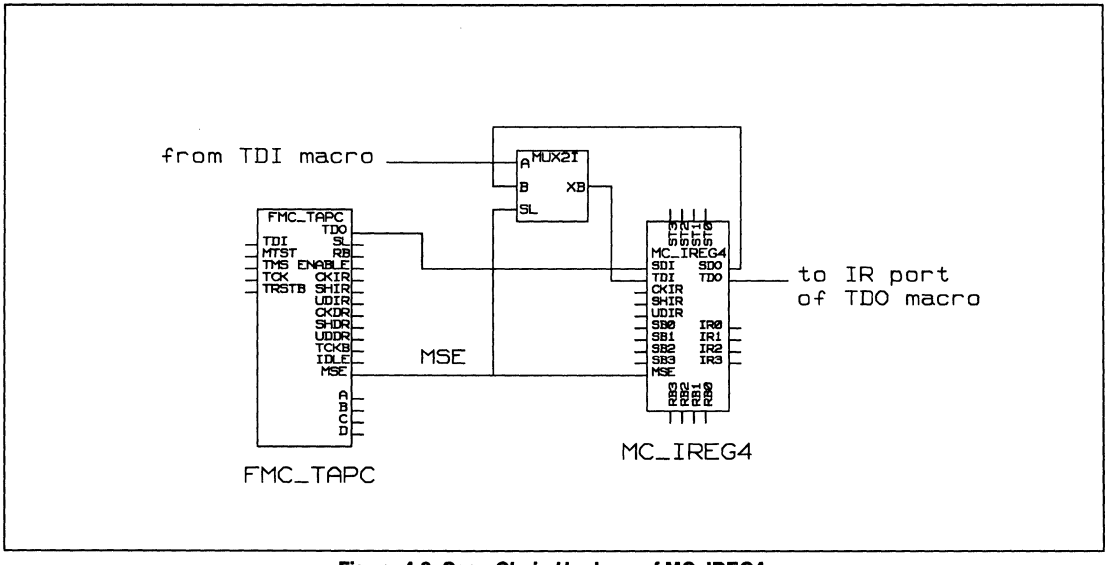

Figure 4-3 Scan Chain Hook-up of MC_IREG4

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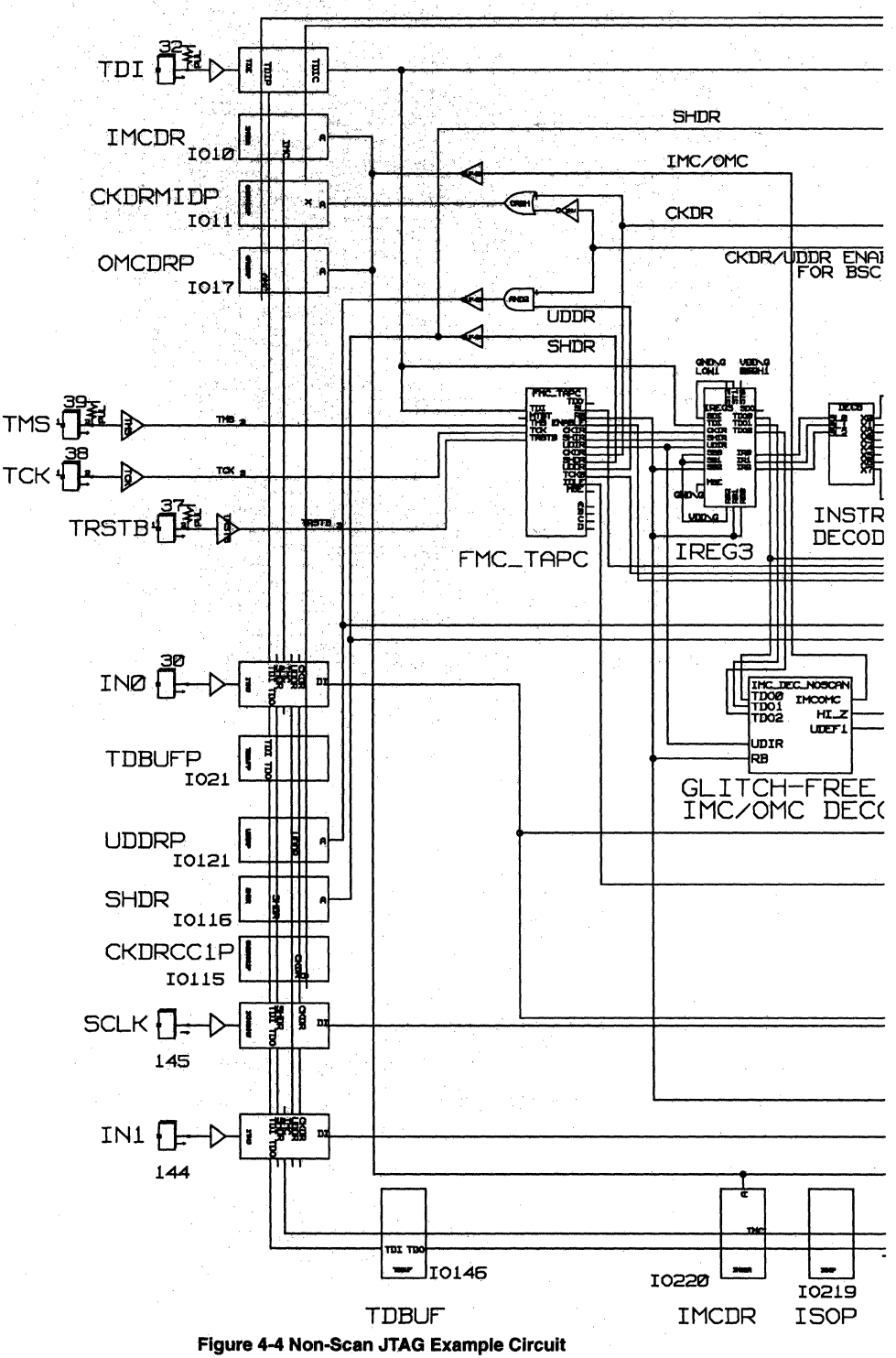

Figure 4-4 Non-Scan JTAG Example Circuit

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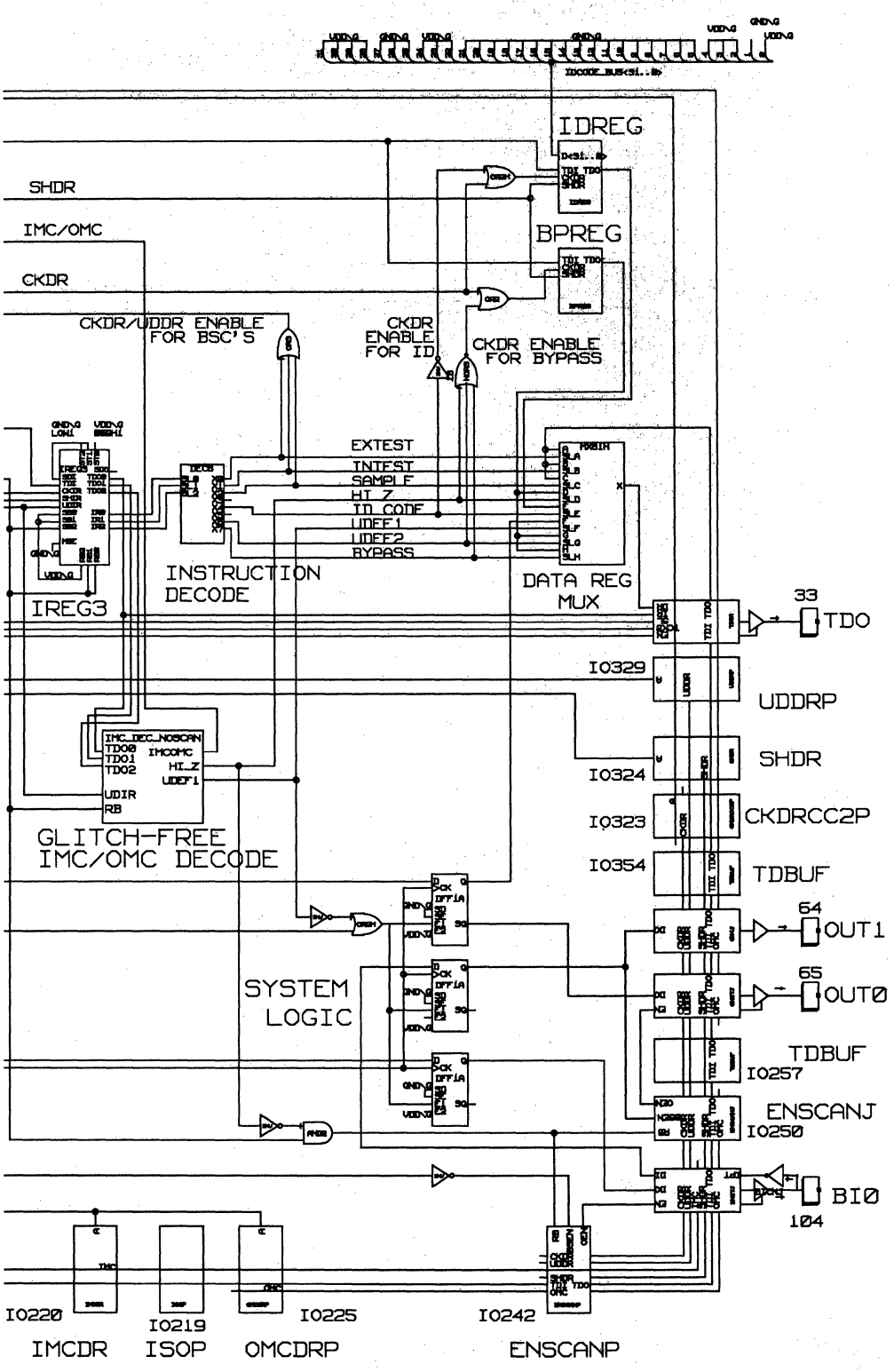

Figure 4-4 Non-Scan JTAG Example Circuit (continued)

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4.4 JTAG Circuitry Interconnection

First a non-scan, JTAG design will be discussed to show the essential circuitry required to implement JTAG on H4C arrays. Afterwards, the requirements for a Mustang/scan-compatible JTAG design will be discussed and illustrated.

4.4.1 Non-Scan JTAG Interconnection

If the system logic is not a scan design, Mustang cannot be used for ATPG. An example of a non-scan, JTAG design is shown in Figure 4-4. Note that:

- the MTST pin is not required
- the MSE and TDO TAP Controller outputs are not used
- the TAP Controller MTST input and Instruction Register MSE input should be tied low

Except for the three flip-flops labeled "System Logic," all of the circuitry in Figure 4-4 is part of the JTAG logic. The BSC's and peripheral JTAG buffers are located around the periphery of the schematic. **Note that test data must shift counter-clockwise through the BSC's around the periphery of the chip.**

On H4C arrays, JTAG boundary scan uses a gated CKDR signal as described in the IEEE 1149.1 specification. That is, CKDR is gated to the appropriate data register (peripheral boundary scan register, Bypass Register, Device Identification Register, etc.) under control of the Instruction Register decode logic. For example, if the Instruction Register holds the Sample, INTEST or EXTEST instruction, then CKDR and UDDR will be gated to the peripheral boundary scan register. In addition, the Instruction Register decode logic must generate the Input Mode Control (IMC) and Output Mode Control (OMC) signals. IMC and OMC control the select lines of the data path multiplexers within the input and output BSC's, respectively. Since users may define their own JTAG instruction sets, the Instruction Register decode logic is design specific; therefore it is not implemented as a special macro in the H4C library. However, in this example a DEC8 macro from the H4C library is sufficient to implement the Instruction Register decoder.

Because instruction decoding is done by combinatorial logic, the decoded control signals may glitch temporarily when UDIR activates a new instruction. Such glitches are harmless on some control signals, but not on others. Control signals which cannot afford to be glitched should be decoded from the instruction register CKIR flops instead of the UDIR flops. The decoded signals then drive flops which are clocked by UDIR. In Figure 4-4 the "Glitch-Free IMC/OMC Decode" block uses this method to decode the IMC/OMC, HI-Z and UDEF1 signals. The IREG3 is a 3-bit instruction register built from three 1-bit MC_IREG cells in order to bring out the CKIR flop outputs at the TDO0, TDO1 and TDO2 ports (see Figure 4-5). These signals are used to decode the IMC/OMC, HI-Z and UDEF1 signals as shown in Figure 4-6. Alternatively, all instruction decoding could be performed on the instruction register CKIR flops, with each decoded signal driving its own "UDIR" flop.

Note that even though IMC and OMC are independent lines in the chip periphery, driven by separate IMCDR and OMCDR drivers, both IMC and OMC are functionally equivalent to the "Mode" control signal defined in IEEE 1149.1. Therefore they would normally have a common source in the array core. In Figure 4-4 this common source is labeled "IMC/OMC."

The ENSCANP and ENSCANJ macros have been hooked-up such that they can be reset either by resetting the TAP Controller or by loading a "HI_Z" instruction, which puts all 3-state outputs in the hi-impedance state.

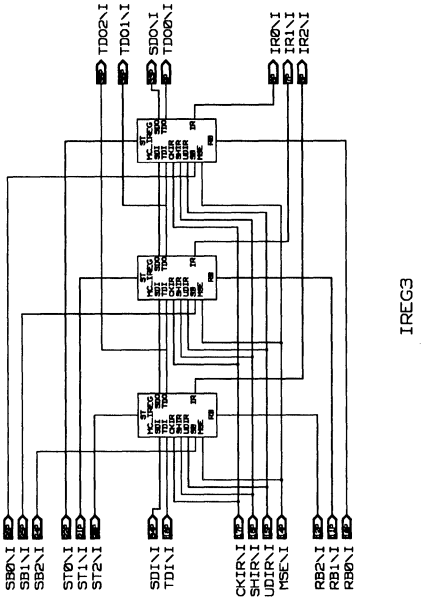

Figure 4-5 IREG3 3-Bit Instruction Register

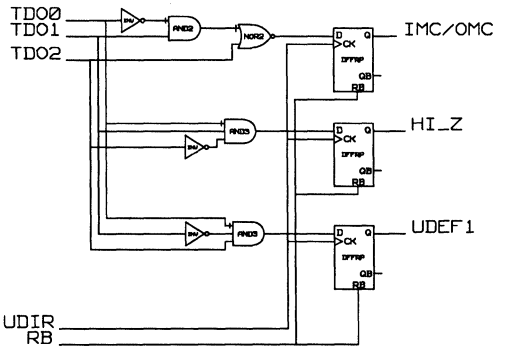

Figure 4-6 Glitch-Free IMC/OMC Decode Block

4.4.2 Mustang-Compatible JTAG Interconnection

In order to make a JTAG design Mustang-compatible the FMC_TAPC TAP Controller of Figure B-4 must be used, as well as an Instruction Register like the one in Figure 4-2. The designer must also add extra circuitry to link up all of the JTAG registers into one scan chain during Mustang test mode. The requirements, which are illustrated in Figure 4-7, are as follows:

1. An extra MTST input pin, which will only be active during Mustang testing, must be added to the design. A pull-up/pull-down resistor may be used to hold this pin inactive during normal operation. **Note: the input macro driven by MTST must be either a non-JTAG macro or a "sample-only" macro such as an ICNCKHJ.**
2. The Mustang test mode input pin must be connected to the MTST input of the TAP Controller and to OR gates which perform clock gating for JTAG data registers. This will cause all of the JTAG scan chains (i. e. the TAP Controller, Instruction Register, and data registers) to be clocked together in Mustang test mode, during which they are part of one scan chain between TDI and TDO.
3. The Mustang scan path through the JTAG logic must be connected starting with the boundary scan chain, then any internal data registers (e.g. Bypass register and ID code register), then the TAP Controller and finally the Instruction Register. This reduces the probability of clock skew problems occurring.
4. Two-input multiplexers must be placed on the connections between the TDI pin and each internal/core JTAG scan chain to enable all JTAG scan chains to be connected up as one long chain during Mustang test mode. The output of each multiplexer will feed the input to a JTAG scan chain. The select input on the multiplexer must be connected to the TAP Controller's Mustang Scan Enable (MSE) output (MSE is TMS logically AND'ed with MTST). The TDI signal should be connected to the A input of the multiplexers. The B input of the multiplexers should be connected to the end of the previous JTAG scan chain, where the order is that defined in item 3 above.
5. In order to use JTAG input and output BSC's as the input to or output from a scan chain they must be forced into transparent mode. If the output has an enable line then this too must be activated during scan. This is done by adding gating logic to the IMC and OMC control lines to force them low during scan mode.
6. If the TCK and system clocks are derived from the same source then they must be clocked on the same edge of the source clock. This may require placing an exclusive-or gate on the TCK input to the TAP Controller, as well as adding clock gating circuitry similar to that built into the TAP Controller, which is described in Appendix B. This circuitry would serve to prevent race conditions between the BSC's and the system/core logic.
7. Mustang requires all asynchronous control lines to be controlled only by an external input. An asynchronous reset line which enters the chip through a normal input BSC can be controlled by the jlatch (see Appendix B) within that BSC. Therefore the reset line must be gated with MTST in the array core so that the reset will be disabled during Mustang testing. Alternatively, the asynchronous reset can enter the chip through a "sample-only" cell. In this case gating the reset signal with MTST is not required, however the reset is no longer controllable from the JTAG BSC ring.

4.5 Mustang-Compatible JTAG Example Circuit

In Figure 4-7 the non-scan JTAG design in Figure 4-4 has been modified, according to the requirements of Section 4.4-2, to create a Mustang-compatible JTAG design. The system logic in this example consists solely of the "System Scan Reg," which is a conventional scan design consisting of one scan chain starting at the IN0 input and exiting at the OUT0 output. The remaining circuitry implements JTAG boundary scan which, during Mustang testing, is configured as one scan chain which enters the chip at pin TDI and exits at pin TDO, as described in Section 4.4-2. (Larger designs typically have multiple scan chains for the system logic because of the long time taken to load/scan them.) As in Figure 4-4, the BSC's and peripheral JTAG buffers are located around the periphery of the schematic. **Note that test data must shift counterclockwise through the BSC's around the periphery of the chip.** The "Glitch-Free IMC/OMC Decode" block functions as described in Section 4.4-1, except that the flops inside it are now scan flops.

Mustang test mode is established by forcing the MTST pin high. During Mustang test mode the TMS pin controls scan mode (MTST and TMS high), during which bidirectional pins must be disabled. Using TRSTB, instead of TMS, to disable the bidirectionals during scan mode improves the fault coverage of the bidirectionals. During scan mode all JTAG registers are configured into one scan chain via 2-input multiplexers at the TDI inputs of the Device Identification Register, Bypass Register, TAP Controller, and Instruction Register. Within the Instruction Register, UDIR flops as well as CKIR flops become part of this same chain as described previously in Section 4-3. The scan chain order is as follows:

TDI, BSC's, IDREG, BPREG, FMC_TAPC, MC_IREG4, TDO. Also, during Mustang scan mode IMC and OMC are forced low so that I/O BSC's will pass scan data into and out of the chip.

The Mustang control file used is as follows:

```
SCAN_OUTPUT TDO
SCAN_OUTPUT OUT0
SCAN_MODE TMS 1
```

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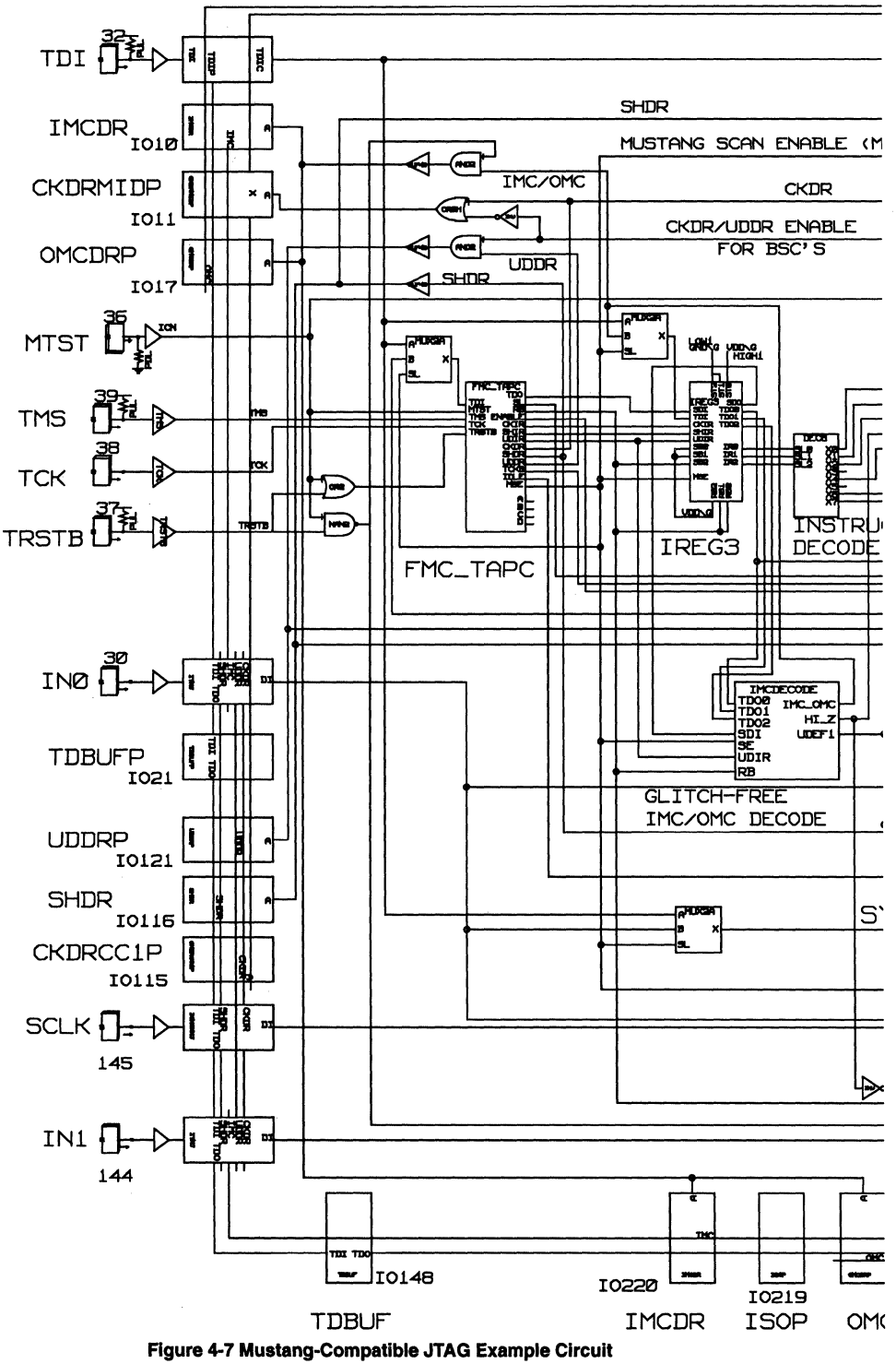

Figure 4-7 Mustang-Compatible JTAG Example Circuit

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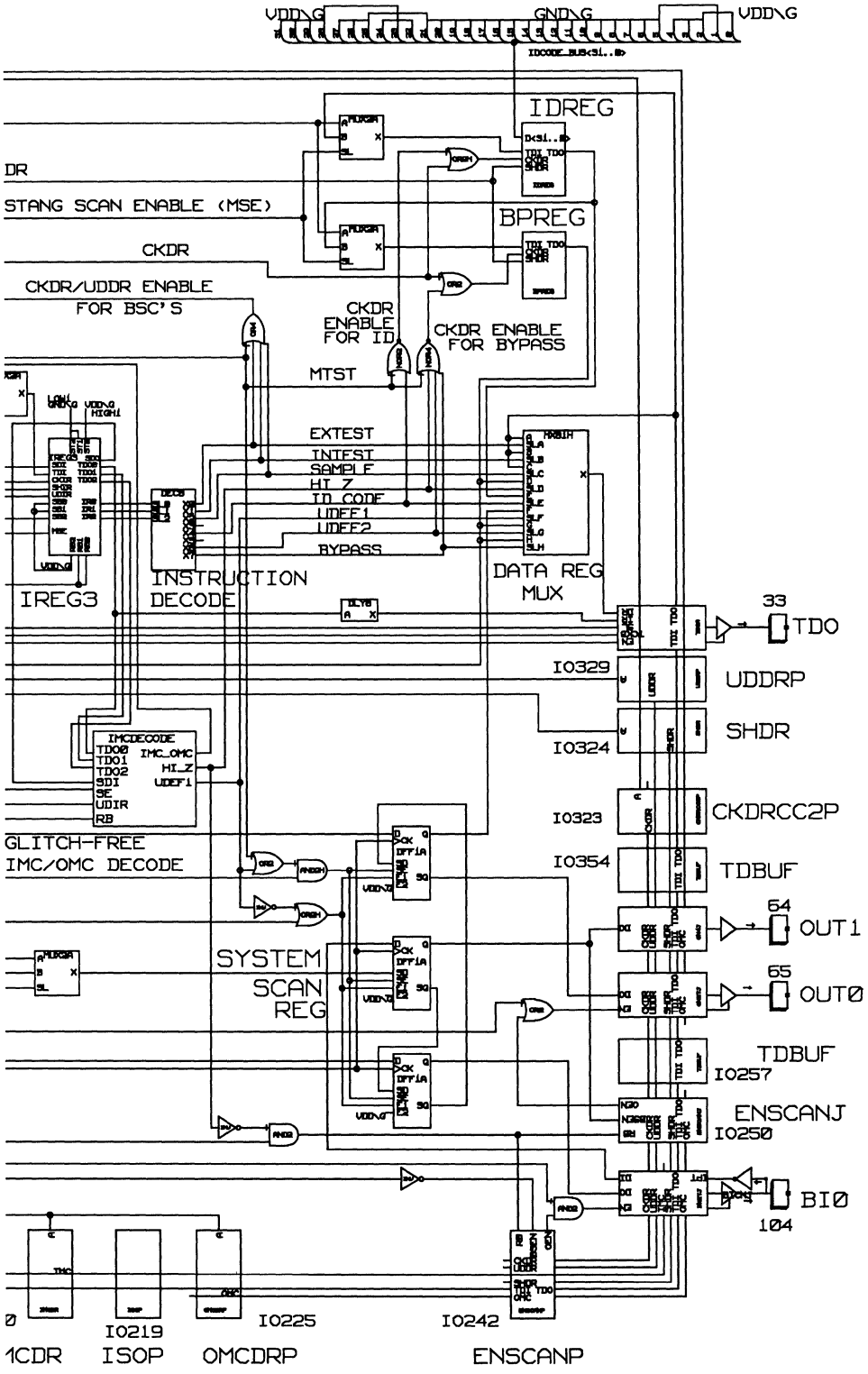

Figure 4-7 Mustang-Compatible JTAG Example Circuit (continued)

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```
SCAN_CLOCK  TCK  1 1
SCAN_CLOCK  SCLK 1 2
SYSTEM_CLOCK TCK  1 1
SYSTEM_CLOCK SCLK 1 2
ASSERT MTST 1
BIDIRECT_CONTROL TRSTB 1
SCAN_MODE      TRSTB 1
```

The fault coverage obtained for this example circuit was >95%. This fault coverage is essentially that of the JTAG circuitry alone since the system logic in this example consists solely of one 3-stage shift register. The fault coverage for a real-world chip design would be much higher, since the vast majority of the circuitry would be scannable system logic with close to 100% fault coverage.

The implementation of the "System Scan Reg" shown in Figure 4-7 is just an example of what could be done. When a user-defined JTAG instruction (code = binary 101) is active, the "E1" input to the System Scan Reg becomes the IDLE output from the Tap Controller so as to allow the System Scan Reg to be clocked while in the "Run-Test/Idle" state. When the user-defined test is completed the contents of the System Scan Reg can be shifted out through TDO under control of SHDR from the TAP Controller, just like any other JTAG test data register such as the Bypass register or peripheral boundary scan register. If the user has no interest in doing such a test, E1 could be tied high (always enabled) and SE could be wired directly to MSE, for example.

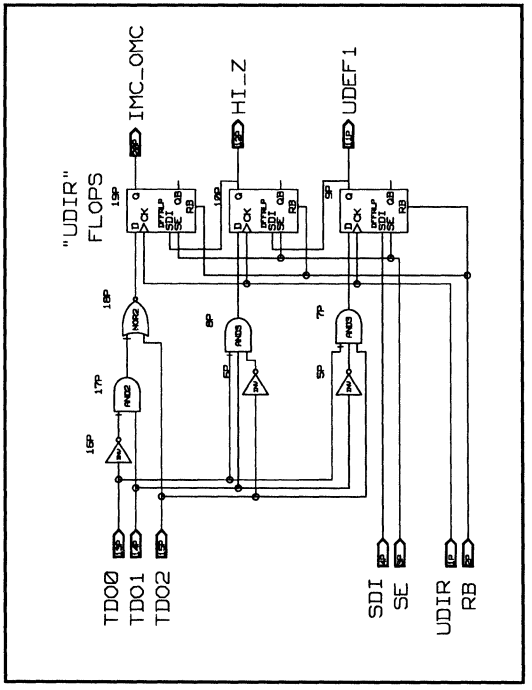

Figure 4-8 Glitch-Free IMC/OMC Decode Block

4.6 Conclusions

The methodology presented here allows Mustang to be used with JTAG by modifying the designs of the TAP Controller and the Instruction Register. The results show that it is possible to achieve high fault coverage using fully automated test pattern generation with Mustang. However, Mustang cannot test the gate (G) input to the BSC shadow latches. Nor can Mustang test all of the JTAG Instruction Register decoding logic. Testing of these areas should be achieved by supplementing the Mustang test patterns with some manually written vectors which test the JTAG circuitry in its normal functional mode of operation. Merging of these functional vectors with the Mustang vectors is accomplished by TESTPAS, which is one of the OACS CAD tools.

5. JTAG I/O Macro Placement and Pin-out Assignment

5.1 Pin & I/O Site Placement of JTAG I/O Macros

5.1.1 Placement of Test Access Port (TAP) Pins

For each array size there are 32 fixed pad pairs which can interface to 64 high-speed scan channels on the Typhoon tester. These pad pairs are marked with asterisks on each Pad-to-Pin cross reference table in the H4C Design Reference Guide. Test Access Port (TAP) pins TMS, TCK, TDI and TDO each must be assigned to a pin which is bonded to one of these "*" pads. It is recommended that TMS be adjacent to TCK, and that TDI be adjacent to TDO. TDI must be counterclockwise from TDO, and no BSC's should be placed between TDI and TDO (clockwise from TDI) because these BSC's would not be contained in the I/O boundary scan data register.

5.1.2 Placement of Non-bonded JTAG Macros

"Non-bonded" macros reside in I/O or power sites but have no off-chip connections. These macros include TDBUF/P, ENSCANJ/P, ISO/P, and the special buffers for CKDR, SHDR, UDDR, IMC and OMC:

CKDRMID, CKDRMIDP (large or high speed arrays only)
CKDRCC1, CKDRCC1P (large or high speed arrays only)
CKDRCC2, CKDRCC2P (large or high speed arrays only)
CKDR, CKDRP (small or low speed arrays only)
SHDR, SHDRP
UDDR, UDDRP
IMCDR, IMCDRP
OMCDR, OMCDRP
ISO, ISOP

Referring to the "H4C123 160 QFP PAD-to-Pin Cross Reference" in the H4C Series Design Reference Guide, each non-bonded macro must reside on a specific power or I/O site which:

- does not connect to a pad (e. g., I/O sites 58 & 59), or
- connects to a pad which is not bonded out to a package pin (e. g., I/O sites 47 and 48), or
- connects to a power/ground pad (e. g., I/O sites 50 and 51); the "P" version of the macro is used at power/ground sites.

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In addition, the JTAG buffers must reside within 25 sites of the nearest INPVSS and INPVDD (or BOTHVSS and BOTHVDD). The Pin-to-Pad Cross Reference for the pertinent array and package is used to select a site for each non-bonded macro.

5.1.3 Placement of JTAG I/O Macros within Schematic Capture

The user must assign a package pin number to the "IO_PIN1" property on each I/O macro, including input, output and bidirectional BSC's and the TAP macros. In addition, a FIX property whose initial value is "IOXX" is already attached to each non-bonded JTAG macro, which the user places by substituting the I/O site # for the "XX" portion of the FIX value. In Figure 4-7 the JTAG buffers have been placed according to the "large or fast array" scheme (see Section 3.2), using the "Pad to Pin" for an H4C123 array in a 160QFP package. Note the inclusion of TDBUF's to buffer BSC TDO output ports where the following BSC is >=7 I/O sites away. In determining the pin-out and I/O site placement, follow the guidelines in Section 5.2.

5.1.4 Placement of JTAG I/O Macros within Synopsys/Verilog HDL Flow

For Verilog HDL design entry followed by Synopsys logic synthesis, the designer creates a Verilog netlist for the JTAG I/O and the non-bonded macros. The designer also creates the EDIFMERGE "Attribute" file, which contains I/O site placement information in the form of FIX properties for all of the peripheral JTAG macros. The Verilog netlists for the JTAG I/O, the core JTAG logic, and the system logic are combined into one EDIF netlist using Synopsys. This "Synopsys EDIF" netlist, along with the Attribute file, are subsequently input to EDIFMERGE to create the "Motorola EDIF" netlist required by the OACS tools. (EDIFMERGE creates a Motorola EDIF netlist from the Synopsys EDIF netlist by adding properties which are specific to Motorola's H4C technology. For more information on EDIFMERGE see the Synopsys/EDIFMERGE Application Note for OACS.)

Had Verilog HDL been used instead of schematic capture to enter the circuit in Figure 4-7, the JTAG portion of the Attribute file would appear as shown in Fig. C-1 (Appendix C).

5.2 Guidelines for Finding an ERC-Compatible Chip Pin-out

In both procedures that follow, the JTAG clock and control signal buffers should be placed on power sites to the extent possible.

5.2.1 Full Boundary Scan Pin-Out Guidelines

In selecting the pin-out for a chip which uses full boundary scan (the vast majority of system signal pins use BSC's), it is recommended that the following steps be done in sequence:

1. Place TDI and TDOA on a pair of adjacent high-speed scan tester pins. TDI must be counterclockwise from TDO. In the same general area as TDI and TDOA, place TCK and TMS on high-speed tester pins and TRSTB on a normal pin.
2. Place remaining system pins, and any additional power/ground pins required, in conformance with the ERC rules governing the placement of output drivers relative to power pin locations. Also keep in mind the rules governing sharing of a single I/O site by two different macros.
3. Place ENSCANJ/P 3-state control BSC's on available I/O or power sites.
4. Between every pair of BSC's separated by >7 non-BSC I/O sites, a TDBUF/P must be inserted on an I/O site within 7 sites of the BSC whose TDO port drives the other's TDI port. (TDBUF/P is built from the input buffer portion of an I/O site, and can therefore share an I/O site with a non-JTAG output driver or with a "paralleled" output driver used to build a hi-drive.)
5. Place the CKDRCC1/P and CKDRCC2/P buffers such that, in Figure 3-1, nets CKDRNET1 and CKDRNET2 are balanced as described in Section 3.1.
6. Place the CKDRMID/P buffer equidistant between CKDRCC1/P and CKDRCC2/P as shown in Figure 3-1.
7. Place the ISO/P macro diametrically opposite from TDOA (approximately), as in Figure 3-3.
8. Place the SHDR/P buffers approximately in the center of nets 1 and 2 as shown in Figure 3-3. Do the same for the UDDR/P buffers.
9. Place the IMCDR/P buffers approximately halfway between the CKDRCC1/P and CKDRCC2/P buffers, which create gap 1 and gap 2 in Figure 3-4. Do the same for the OMCDR/P buffers.

5.2.2 Partial Boundary Scan Pin-Out Guidelines

"Partial boundary scan" refers to a chip on which many system signal pins use non-JTAG I/O macros. In selecting the pin-out for such a chip, it is recommended that the following steps be done in sequence:

1. Place system pins (i. e., all pins except TDI, TDOA, TMS, TCK, and TRSTB), and any additional power/ground pins required, in conformance with the ERC rules governing the placement of output drivers relative to power pin locations. Also keep in mind the rules governing sharing of a single I/O site by two different macros.
2. Place ENSCANJ/P 3-state control BSC's on available I/O or power sites.
3. Choose a pair of adjacent high-speed scan tester pins for TDI and TDOA (with TDI counterclockwise from TDO) such that a line drawn from TDOA through the center of the chip creates two halves which each contain an equal number of BSC's, and to the extent possible, an equal number of non-JTAG pins. In the same general area as TDI and TDOA, place TCK and TMS on high-speed tester pins and TRSTB on any pin.

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4. Between every pair of BSC's separated by >7 non-BSC I/O sites, a TDBUF/P must be inserted on an I/O site within 7 sites of the BSC whose TDO port drives the other's TDI port. (TDBUF/P is built from the input buffer portion of an I/O site, and can therefore share an I/O site with a non-JTAG output driver or with a "paralleled" output driver used to build a hi-drive.)
5. Place the CKDRCC1/P and CKDRCC2/P buffers such that between each buffer and TDOA there is an equal number of BSC's, and to the extent possible, an equal number of non-JTAG pins. Refer to Figure 3-1.
6. Place the CKDRMID/P buffer equidistant between CKDRCC1/P and CKDRCC2/P (typically near TDOA). Refer to Figure 3-1.
7. Place the ISO/P macro diametrically opposite from TDOA (approximately), as in Figure 3-3.
8. Place the SHDR/P buffers approximately halfway between the TDOA and ISO/P, in terms of BSC's (see Figure 3-3). Do the same for the UDDR/P buffers.
9. Place the IMCDR/P buffers approximately halfway between the CKDRCC1/P and CKDRCC2/P buffers, in terms of BSC's (see Figure 3-4). Do the same for the OMCDR/P buffers.

6. CAD Design Flows

For Mentor QSIM simulation on the HP/Apollo platform, entry of an H4C design would likely be done via schematic capture. The corresponding "Schematic Capture/QSIM Design Flow" in Section 6.1 follows a "bottom-up" design methodology.

For Verilog simulation on either the Sun or HP/Apollo platform, design entry can be done by either schematic capture or, for Synopsys users, by writing a Verilog HDL circuit description. The "Schematic Capture/Verilog Design Flow" in Section 6.2 and the "Synopsys/Verilog Design Flow" in Section 6.3 both follow a "top-down" design methodology where the chip is initially described behaviorally using Verilog HDL. In Section 6.2 the HDL is manually converted into gates using schematic capture, whereas in Section 6.3 the HDL is synthesized into gates using Synopsys.

For real world schematic capture designs, it may be more practical to capture the BSC's in rows rather than trying to capture the I/O in the shape of a chip footprint as in Figure 4-7.

During pre-layout simulations, estimated parasitic resistance and capacitance values are used for the metal interconnect between peripheral JTAG macros, as is done for interconnect between core macros. **As a result, it is possible to get pre-layout DECAL edge-rate warnings or errors for nets in the periphery. These warnings and errors are invalid, since the peripheral nets have been shown by SPICE to have no edge-rate problems.** After layout the actual resistance and capacitance values are used, at which time no edge-rate errors should occur on peripheral nets.

6.1 Schematic Capture/QSIM Design Flow

I. Determine Chip Pin-Out and Capture JTAG I/O

1. Use CAPTURE to capture a schematic of the JTAG I/O, following the "Guidelines for Finding an ERC-Compatible Chip Pin-Out" in Section 5.2.
2. Verify JTAG I/O conform to electrical design rules:
   a. Run FLATTEN to generate a QSIM database.
   b. Run NETLIST to generate an EDIF netlist (used by ERC).
   c. Run ERC for peripheral rule checks. Repeat steps 1 and 2 until ERC passes.

II. Design Chip's System (Non-JTAG) Logic

A. Design Individual Sub-Blocks

3. Use CAPTURE to capture a schematic for one system sub-block "Y".
4. Run FLATTEN to generate a QSIM database for Y.
5. (Optional) Verify Y via unit-delay QSIM simulation. Repeat steps 3-5 until Y's functionality is correct.
6. Run NETLIST to create the required Motorola netlists:
   a. an EDIF netlist (used by ERC and DECAL)
   b. a TEGAS/TDL netlist (used by MUSTANG) if the chip is a scan design.
7. Run ERC to verify Y conforms to electrical design rules. If violations occur return to step 3 to correct the schematic.
8. If the chip is a scan design, run the MUSTANG design rule checker to verify Y conforms to scan design rules. (Also generate test patterns if Y's fault coverage is desired.) If violations occur return to step 3 to correct the schematic.
9. Verify Y via real-time simulation:
   a. Run DECAL to calculate real-time delays. If edge-rate violations occur, return to step 3 to correct the schematic.
   b. Run INSERT_DELAYS to insert real-time delays into the QSIM database.
   c. Run QSIM. If Y's functionality or timing is incorrect, return to step 3 to correct the schematic.
10. Repeat steps 3-9 for each system sub-block on the chip.

B. Combine All of Chip's System Sub-Blocks

11. Use CAPTURE to combine the sub-blocks for all system logic on the chip.
12. Run FLATTEN to generate a QSIM database.
13. Run NETLIST to create an EDIF netlist. Also create a TEGAS/TDL netlist if the chip is a scan design.
14. Run ERC and, if the chip is a scan design, run MUSTANG; then run DECAL and INSERT_DELAYS followed by QSIM real-time simulation.

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If violations occur in any of these tools, make schematic corrections for all erroneous sub-blocks. Re-verify each corrected sub-block individually to the extent desired in section II, part A, then return to step 11.

III. Combine JTAG Circuitry with Chip's System Logic

15. Use CAPTURE to capture a schematic of the core JTAG logic (including the TAP Controller etc.).

Verify All JTAG Circuitry by Itself (Optional)

16. In CAPTURE, combine the core JTAG logic with the JTAG I/O from step 1.
17. Run FLATTEN to generate a QSIM database.
18. Do unit-delay QSIM simulation, if desired. If step 18 is done, repeat steps 16-18 until functionality is correct.
19. Run NETLIST to create an EDIF netlist. Also create a TEGAS/TDL netlist if the chip is a scan design.
20. Run ERC and, if the chip is a scan design, run the MUSTANG design rule checker; then run DECAL and INSERT_DELAYS followed by QSIM real-time simulation. If violations occur in any of these tools, return to step 16 to correct the schematic.

Verify Combined System and JTAG Circuitry

21. Use CAPTURE to combine the core JTAG logic, JTAG I/O, and system logic.
22. Create required netlists for the entire chip:
    a. Run FLATTEN to generate a QSIM database.
    b. Run NETLIST to create the following:
        i) an EDIF netlist (used by ERC and DECAL)
        ii) a TEGAS/TDL netlist (used by MUSTANG) if the chip is a scan design.
        iii) an "Actual.RC" file (used by DECAL) for each firm macro, such as the FMC_TAPC
23. Run ERC to verify the entire chip conforms to electrical design rules.
24. If the chip is a scan design, run the MUSTANG design rule checker to verify the entire chip conforms to scan design rules.
25. Verify entire chip via real-time simulation:
    a. Run DECAL to calculate real-time delays.
    b. Run INSERT_DELAYS to insert real-time delays into the QSIM database.
    c. Run QSIM.

If errors occur in any of steps 23-25, return to step 15 to fix the core JTAG logic, or return to step 3 to fix any erroneous system sub-blocks. Re-verify each corrected sub-block individually to the extent desired in section II, part A, then continue at step 11, 15 or 21 as desired.

26. If the chip is a scan design, run MUSTANG to generate scan test patterns.
27. Run TESTPAS to combine the functional and scan test patterns from steps 25 and 26, respectively.

6.2 Schematic Capture/Verilog Design Flow

Veritime timing analysis is recommended as a complement to real-time simulations (those using DECAL delays instead of unit-delays).

I. Behavioral-Level Design

1. As part of the behavioral verification of the entire system, create and verify a Verilog HDL behavioral description for all system logic on the H4C chip.

II. Determine Chip Pin-Out and Capture JTAG I/O

2. Use ASIC_GED to capture a schematic of the JTAG I/O, following the "Guidelines for Finding an ERC-Compatible Chip Pin-Out" in Section 5.2.
3. Verify JTAG I/O conform to electrical design rules:
    a. Run NETLIST to generate an EDIF netlist (used by ERC).
    b. Run ERC for peripheral rule checks. Repeat steps 2 and 3 until ERC passes.

III. Design Chip's System (Non-JTAG) Logic

A. Convert Behavioral Description to an RTL (Register-Transfer Level) Description

4. For one chip sub-block "X," convert the behavioral description to an RTL description. If X is to be converted into gates by logic synthesis as opposed to schematic capture, then the RTL description must use only those Verilog constructs supported by Synopsys.
5. Simulate X's RTL description, by itself. Modify and re-simulate X's RTL description until its functionality matches X's behavioral description.
6. Repeat step 1's simulation of the chip behavioral description, but use the RTL description for X in place of X's behavioral description. Modify X's RTL description as necessary until chip functionality matches that of the all-behavioral chip description in step 1. Repeat steps 4-6 for each of the chip's sub-blocks.
7. Simulate all system logic on the chip at the RTL level. Modify the sub-blocks' RTL descriptions as necessary until chip functionality matches that of the all-behavioral chip description in step 1.

B. Convert Sub-Block RTL Descriptions to Gate-Level Netlists

8. Use ASIC_GED to capture a schematic for one system sub-block "X".
9. Run NETLIST to create the required netlists for X:
    a. an EDIF netlist (used by ERC and DECAL) and a Verilog netlist
    b. a TEGAS/TDL netlist (used by MUSTANG) if the chip is a scan design.
10. (Optional) Do unit-delay simulation of X's gate-level netlist by itself, using the same vectors used to verify X's RTL description in step 5. If X's functionality is incorrect return to step 8 to correct the

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schematic, or correct X's RTL description and return to step 5, 6 or 7 to verify the correction.

11. (Optional) Repeat step 7's simulation of the chip RTL description, but use the gate-level netlist for sub-block X in place of X's RTL description. Handle bugs as prescribed in step 10.
12. Run ERC to verify X conforms to electrical design rules. If violations occur return to step 8 to correct the schematic.
13. If the chip is a scan design, run the MUSTANG design rule checker to verify X conforms to scan design rules. (Also generate test patterns if Y's fault coverage is desired.) If violations occur return to step 8 to correct the schematic.
14. Verify X via real-time simulation and timing analysis:
    a. Run DECAL to calculate real-time delays. If edge-rate violations occur, return to step 8 to correct the schematic.
    b. Repeat step 10, using DECAL delays instead of unit delays.
    c. Repeat step 11, using DECAL delays instead of unit delays.
15. Repeat steps 8-14 for each system sub-block on the chip.

C. Combine Netlists for All of Chip's System Sub-Blocks

16. Use ASIC_GED to combine the sub-blocks for all system logic on the chip.
17. Run NETLIST to create Verilog and EDIF netlists. Also create a TEGAS/TDL netlist if the chip is a scan design.
18. Run ERC and, if the chip is a scan design, run MUSTANG. Run DECAL; then simulate the gate-level netlist for the chip's system logic using the same vectors which were used in step 7 to verify the RTL description of the chip's system logic. If violations occur in any of these tools, do one of the following for each erroneous sub-block:
    i) return to step 8 to correct the sub-block's schematic, or
    ii) correct the sub-block's RTL description and return to step 5, 6 or 7 to verify the correction.
    iii) Re-verify each corrected sub-block individually to the extent desired in section III, part B, then return to step 16.

IV. Combine JTAG Circuitry with Chip's System Logic

19. Use ASIC_GED to capture a schematic of the core JTAG logic (including the TAP Controller etc.).

Verify All JTAG Circuitry by Itself (Optional)

20. In ASIC_GED, combine the core JTAG logic with the JTAG I/O from step 2.
21. Run NETLIST to create EDIF and Verilog netlists. Also create a TEGAS/TDL netlist if the chip is a scan design.
22. Run ERC and, if the chip is a scan design, run the MUSTANG design rule checker; then run DECAL followed by Verilog real-time simulation. If violations occur in any of these tools, return to step 20 to correct the schematic.

Verify Combined System and JTAG Circuitry

23. Use ASIC_GED to combine the core JTAG logic, JTAG I/O, and system logic.
24. Run NETLIST for the entire chip to create the following:
    a. an EDIF netlist (used by ERC and DECAL) and a Verilog netlist
    b. an "Actual.RC" file (used by DECAL) for each firm macro, such as the FMC_TAPC
    c. a TEGAS/TDL netlist (used by MUSTANG) if the chip is a scan design.
25. Run ERC to verify entire chip conforms to electrical design rules.
26. If the chip is a scan design, run the MUSTANG design rule checker to verify entire chip conforms to scan design rules.
27. Verify entire chip via real-time simulation and timing analysis:
    a. Run DECAL to calculate real-time delays.
    b. Simulate the gate-level netlist for the entire chip using the same vectors which were used in step 7 to verify the RTL description of the chip's system logic. Then exercise the JTAG logic in a separate simulation. If errors occur in any of steps 25-27, return to step 19 to correct the core JTAG logic, or do one of the following for each erroneous sub-block:
        i) return to step 8 to correct the sub-block's schematic, or
        ii) correct the sub-block's RTL description and return to step 5, 6 or 7 to verify the correction. Re-verify each corrected sub-block individually to the extent desired in section III, part B, then continue at step 16, 19 or 23 as desired.
28. If the chip is a scan design, run MUSTANG to generate scan test patterns.
29. Run TESTPAS to combine the functional and scan test patterns from steps 27 and 28, respectively.

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6.3 Synopsys/Verilog Design Flow

Tieoff's and buses require special handling when a Verilog netlist created by the OACS "NETLIST" tool is to be used in Synopsys (e. g. in steps16, 23 or 25 below). In an OACS netlist, the two statements which define VDD and VSS tieoff's are not recognized by Synopsys and must be modified as described in a preliminary application note entitled "High-Level Design Methodology for OACS 2.0." Also, in an OACS netlist buses are separated into individual bits, which need to be recombined into buses to properly connect to other Verilog HDL modules within Synopsys. An example of this is shown in the "High-Level Design" Application Note.

The "Synopsys delays" mentioned below are the macrocell prop delays calculated by Synopsys during the process of synthesizing a sub-block. These delays must be written out to a "Verilog.timing" file in order to be used during simulation of a synthesized sub-block. Synopsys delays are accurate to within approximately 5% of DECAL delays.

Veritime timing analysis is recommended as a complement to real-time simulations (those using either DECAL or Synopsys delays instead of unit-delays).

I. Behavioral-Level Design

1. As part of the behavioral verification of the entire system, create and verify a Verilog HDL behavioral description for all system logic on the H4C chip.

II. Determine Chip Pin-Out and Create JTAG I/O Netlist

2. Create both a Verilog netlist and a "Motorola EDIF" netlist for the JTAG I/O only (no core module instantiation).
3. Verify JTAG I/O conform to electrical design rules:
   a. Run ERC for peripheral rule checks. If violations occur (other than those due to the absence of a core module instantiation) return to step 2 to correct the JTAG I/O netlists.

III. Design Chip's System (Non-JTAG) Logic

A. Convert Behavioral Description to RTL (Register-Transfer Level) Description

4. For one chip sub-block "X," convert the behavioral description to an RTL description. If X is to be converted into gates by logic synthesis as opposed to schematic capture, then the RTL description must use only those Verilog constructs supported by Synopsys.
5. Simulate X's RTL description, by itself. Modify and re-simulate X's RTL description until its functionality matches X's behavioral description.
6. Repeat step 1's simulation of the chip behavioral description, but use the RTL description for sub-block X in place of X's behavioral description. Modify X's RTL description as necessary until chip functionality matches that of the all-behavioral chip description in step 1. Repeat steps 4-6 for each of the chip's sub-blocks.
7. Simulate all system logic on the chip at the RTL level. Modify the sub-blocks' RTL descriptions as necessary until chip functionality matches that of the all-behavioral chip description in step 1.

B. Synthesize Sub-Block RTL Descriptions Into Gate-Level Netlists

Synopsys/Verilog Debug Loop

8. For one sub-block "X," synthesize the RTL description into a gate-level Verilog netlist using Synopsys.
9. Simulate X's gate-level netlist by itself, using the same vectors used to verify X's RTL description in step 5. Use Synopsys delays. If X's functionality or timing is incorrect:
   a. return to step 8 to modify the synthesis constraints and re-run Synopsys, or
   b. correct X's RTL description and return to step 5, 6 or 7 to verify the correction.
10. Repeat step 7's simulation of the chip RTL description, but use the gate-level netlist for sub-block X in place of X's RTL description. Use Synopsys delays for X. Handle bugs as prescribed in step 9.

OACS Verification

11. Create the required netlists for X:
    a. Run Synopsys to generate a flat EDIF netlist.
    b. Run EDIFMERGE to generate a "Motorola EDIF" netlist (used by ERC and DECAL).
    c. Run NETLIST to create a Verilog netlist from the "Motorola EDIF" netlist. Also generate a TEGAS/TDL netlist for MUSTANG if the chip is a scan design.
12. Run ERC to verify X conforms to electrical design rules. If violations occur, correct X's RTL description and return to step 5, 6 or 7 to verify the correction.
13. If the chip is a scan design, run the MUSTANG design rule checker to verify X conforms to scan design rules. (Also generate test patterns if X's fault coverage is desired.) If violations occur, correct X's RTL description and return to step 5, 6 or 7 to verify the correction.
14. Verify X via real-time simulation and timing analysis:
    a. Run DECAL to calculate real-time delays. Handle edge-rate violations as prescribed in step 9.
    b. Repeat step 9, using DECAL delays instead of Synopsys delays.
    c. Repeat step 10, using DECAL delays instead of Synopsys delays.
15. Repeat steps 8-14 for each synthesized sub-block until each one has a correct gate-level Verilog netlist.

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C. Design "Not-To-Be-Synthesized"/Schematic Capture Sub-Blocks

OACS Verification

8a. Use ASIC_GED to capture a schematic for one system sub-block "Y".

9a. Run NETLIST to create the following netlists for Y:

a. an EDIF netlist (used by ERC and DECAL) and a Verilog netlist

b. a TEGAS/TDL netlist (used by MUSTANG) if the chip is a scan design

10a. (Optional) Do unit-delay simulation of Y's gate-level netlist by itself, using the same vectors used to verify Y's RTL description in step 5. If Y's functionality is incorrect:

a. return to step 8a to correct the schematic, or

b. correct Y's RTL description and return to step 5, 6 or 7 to verify the correction.

11a. (Optional) Repeat step 7's simulation of the chip RTL description, but use the gate-level netlist for sub-block Y in place of Y's RTL description. Handle bugs as prescribed in step 10a.

12a. Run ERC to verify Y conforms to electrical design rules. If violations occur return to step 8a to correct the schematic.

13a. If the chip is a scan design, run the MUSTANG design rule checker to verify Y conforms to scan design rules. (Also generate test patterns if Y's fault coverage is desired.) If violations occur return to step 8a to correct the schematic.

14a. Verify Y via real-time simulation and timing analysis:

a. Run DECAL to calculate real-time delays. If edge-rate violations occur, return to step 8a to correct the schematic.

b. Repeat step 10a, using DECAL delays instead of unit delays.

c. Repeat step 11a, using DECAL delays instead of unit delays.

15a. Repeat steps 8a-14a for each sub-block to be entered via schematic capture until each one has a correct gate-level Verilog netlist.

D. Combine All of Chip's System Sub-Blocks

Synopsys/Verilog Debug Loop

16. Read into Synopsys the gate-level Verilog netlists for all system sub-blocks on the chip. Run Synopsys with logic optimization turned off (i. e., no "compile") to write out one Verilog netlist and one EDIF netlist which contain all system logic on the chip.

17. Simulate the gate-level netlist for all system logic, using Synopsys delays. Use the same vectors which were used in step 7 to verify the RTL description of the chip's system logic. If violations occur, do one of the following for each erroneous sub-block:

a. return to step 8a to correct the sub-block's schematic, or

b. correct the sub-block's RTL description and return to step 5, 6 or 7 to verify the correction.

Re-verify each corrected sub-block individually to the extent desired in section III, part B or C, then return to step 16.

OACS Verification

18. Run EDIFMERGE to create a "Motorola EDIF" netlist, then run NETLIST to create a TEGAS/TDL netlist for MUSTANG (if the chip is a scan design) and a Verilog netlist.

19. Run ERC. Handle violations as prescribed in step 17.

20. If the chip is a scan design, run MUSTANG. Handle violations as prescribed in step 17.

21. Run DECAL and then repeat step 17, using DECAL delays instead of Synopsys delays.

IV. Combine JTAG Circuitry with Chip's System Logic

OACS Verification

22. Create a gate-level Verilog netlist for the core JTAG logic (including the TAP Controller etc.) by one of two methods:

a. capture a schematic and run NETLIST.

b. write a Verilog netlist manually.

Verify All JTAG Circuitry by Itself (Optional)

23. Merge the core JTAG logic and the JTAG I/O into one Verilog netlist using Synopsys. (The Verilog netlists for any "soft" macros used, such as the MC_IREG or MC_IREG4, must be read into Synopsys; likewise for the Verilog netlists for any "firm" macros used, such as the FMC_TAPC.)

24. Do a unit-delay simulation on all JTAG circuitry. (Synopsys delays are not usable for simulation because they only include the core<-->PAD data path through each BSC.) If violations occur return to step 22 to correct the schematic.

Verify Combined System and JTAG Circuitry

25. Create the required netlists for the entire chip:

a. Run Synopsys with logic optimization turned off (i. e., no "compile") to generate a flat EDIF netlist (except for firm macros) from the Verilog netlists for the system logic, core JTAG logic, and JTAG I/O. (As in step 23 above, the Verilog netlists for "soft" and "firm" macros must be read into Synopsys. However, firm macros must remain hierarchical until step 'c' below. For more detail see the preliminary application note "High-Level Design Methodology for OACS 2.0".)

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b. Run EDIFMERGE to generate an "edif.net" netlist. Rename it as "edif.hnet" since it contains hierarchical firm macros which have not yet been flattened.

c. Run NETLIST, with the "edif.hnet" as input, to create:

i) "complete" or "flat" EDIF and Verilog netlists which include each firm macro's internal circuitry

ii) an "Actual.RC" file (used be DECAL) for each firm macro, such as the FMC_TAPC

iii) a TEGAS/TDL netlist for MUSTANG, if the chip is a scan design.

26. Run ERC to verify entire chip conforms to electrical design rules.

27. If the chip is a scan design, run the MUSTANG design rule checker to verify entire chip conforms to scan design rules.

28. Verify entire chip via real-time simulation and timing analysis:

a. Run DECAL to calculate real-time delays (uses "complete" EDIF netlist).

b. Simulate the gate-level netlist for the entire chip using the same vectors which were used in step 7 to verify the RTL description of the chip's system logic. Then exercise the JTAG logic in a separate simulation.

If errors occur in any of steps 26-28, return to step 22 to correct the core JTAG logic, or do one of the following for each erroneous sub-block:

i) return to step 8a to correct the sub-block's schematic, or

ii) correct the sub-block's RTL description and return to step 5, 6 or 7 to verify the correction.

Re-verify each corrected sub-block individually to the extent desired in section III, part B or C, then continue at step 16, 22 or 25 as desired.

29. If the chip is a scan design, run MUSTANG to generate scan test patterns.

30. Run TESTPAS to combine the functional and scan test patterns from steps 28 and 29, respectively.

Appendix A: Electronic Rule Checker (ERC) Rules for JTAG

Each rule presented in this appendix has been classified as either a warning (W) or an error (E) based upon the severity of the violation. Warnings are used to indicate a possible violation of JTAG specification requirements which will not cause any failure in the design methodology or manufacture. As such, a warning may be ignored if the condition that it flags is truly what the designer intended to implement. On the other hand, errors must be corrected.

Appendix A.1: General Rules for H4C

1. (E) BUFXP and INVXP macros must be placed on power or ground sites.
2. (E) No macro may have both an IO_PIN1 and a FIX property.
3. (E) The IO_PIN1 property must be used on all IO macros which contain a pad port.
4. (E, W)All the ERC rules that apply to non-JTAG input macros apply to input BSC macros and to TCK, TMS, TDI, TRSTB macros.
5. (E, W)All the ERC rules that apply to non-JTAG output macros apply to output BSC macros and to TDO, TDOA macros.
6. (E, W)All the ERC rules that apply to non-JTAG bidirectional instances apply to bidirectional BSC instances. A bidirectional BSC instance is constructed from a bidirectional output BSC macro and a bidirectional input BSC macro.
7. (E, W)All the ERC rules that apply to non-JTAG bidirectional output macros apply to bidirectional output BSC macros.
8. (E, W)All the ERC rules that apply to non-JTAG bidirectional input macros apply to bidirectional input BSC macros.
9. (E, W)All the ERC rules that apply to non-JTAG oscillator macros apply to oscillator BSC macros.
10. (E) For peripheral JTAG macros, an I/O site can be shared only in the following ways.

a. Any normal drive input BSC macro, excluding ICNJA, and any normal drive non-JTAG input macro can share its I/O site with a parallel/slave buffer used in JTAG or non-JTAG high-drive output and high-drive bidirectional macros.

b. A TDBUF macro can share its I/O site with a parallel/slave buffer used in JTAG or non-JTAG high-drive output and high-drive bidirectional macros, but a TDBUFP cannot. (TDBUF(P) is built with the input buffer portion of an I/O site.)

c. A bidirectional BSC instance is constructed from a bidirectional output BSC macro and a bidirectional input BSC macro. An IO_PIN1 property is associated with a bidirectional output BSC macro. Neither an IO_PIN1 nor a FIX property is associated with a bidirectional input

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BSC macro. A bidirectional input BSC macro shares a site with the bidirectional output BSC macro to which it gets connected. Note that the ENSCANJ cannot share an I/O site, even though it does not use the input or output buffer portion of the I/O site. In addition, neither the ISO(P) macro nor any of the special buffers for CKDR, SHDR, UDDR, IMC and OMC can share an I/O site.

11. (E) When placing I/O macros and JTAG buffers in the periphery, the user must leave room for hi-drive parallel/slave buffers. (Paralleled buffers cannot be placed on power sites.) There also must be enough empty I/O sites for EDIF2TANGATE to place all BUFX and INVX macros used in the design.
12. (E) Only peripheral macros can be located in the periphery of a chip. Peripheral macros must be located in the periphery of a chip.

Appendix A.2: Test Access Port Connections

The rules in this section ensure that the Test Access Port is implemented correctly.

1. (W)There must be one and only one macro from the set {TCK, TCKT, TCKS, TCKH, TCKHT, TCKHS} in the design.
2. (E) There must be one and only one macro from the set {TMS, TMST, TMSS} in the design.
3. (E) There must be one and only one macro from the set {TDI, TDIT, TDIS} in the design.
4. (E) There must be one and only one TDO or TDOA macro in the design.
5. (E) There must not be more than one macro from the set {TRSTB, TRSTBT, TRSTBS, ICNJA} in the design.
6. (E) The PAD inputs of {TCK, TCKT, TCKS, TCKH, TCKHT, TCKHS, TMS, TMST, TMSS, TDI, TDIT, TDIS} macros must be connected to high speed scan pads. The PAD outputs of TDO and TDOA macros must be connected to high speed scan pads.
7. (E) There must be a pullup resistor connected to the IC ports of {TMS, TMST, TMSS, TDI, TDIT, TDIS, TRSTB, TRSTBT, TRSTBS, ICNJA} macros.

Appendix A.3: JTAG Conformance

The rules in this section ensure that the design conforms to the internal requirements of the JTAG specification. Since most of these are not required in order to have a fully functional device they are warnings.

1. (W)The number of BPREG macros in the design must be greater than zero.
2. (E) There must not be more than one BPREG macro in the design.
3. (E) There must not be more than one IDREG macro in the design.
4. (E) If the device I. D. code is specified in the design information then there must be one IDREG macro in the design.
5. (E) If there is one IDREG macro in the design then the value set on the D31 to D0 pins must match the I. D. code specified in the design information. D31 is the most significant bit. If a bit is 1(0), the corresponding D-port must be connected to VDD (VSS).
6. (W)If any 3-state BSC's are used in the design then there must be one or more instances of a macro from the set {ENSCANI, ENSCANP, ENSCANJ}.

Appendix A.4: JTAG I/O Scan Ring

The rules in this section ensure that the connection and placement of JTAG I/O macros in the periphery conform to the H4C array implementation of JTAG.

1. (E) No BSC JTAG macros may be placed between a macro from {TDI, TDIT, TDIS} and a macro from {TDO, TDOA} in the direction clockwise of a macro from {TDI, TDIT, TDIS}.
2. (E) Instances of peripheral JTAG buffer macros must have valid FIX property values that locate them in the periphery of the design.
3. (E) All 'xxxP' JTAG macros must be placed on power and ground IO sites.
4. (E) No 'non-xxxP' JTAG macro can be placed on a power or ground site.
5. (E) The fanout of the TDIP port of a macro from {TDI, TDIT, TDIS} must be one. The TDIP port of a macro from {TDI, TDIT, TDIS} must be connected to the TDI port of a peripheral BSC or the TDI port of a macro from {TDO, TDOA, TDBUF, TDBUFP}.
6. (E) The fanout of the TDO port of every peripheral BSC or TDBUF/P macro must be one. The TDO port of such a macro must be connected to the TDI port of another peripheral BSC or the TDI port of a macro from {TDBUF, TDBUFP, TDO, TDOA}.
7. (E) The fan-in of the TDI port of every peripheral BSC and TDBUF/P macro must be one. The TDI port of such a macro must be connected to the TDO port of another peripheral BSC, TDBUF/P, or the TDIP port of a macro from {TDI, TDIT, TDIS}.
8. (E) The fanin of the TDI port of the TDO/TDOA macro must be one, and must be connected to the TDO port of a peripheral BSC, TDBUF/P, or the TDIP port of a macro from {TDI, TDIT, TDIS}.
9. (E) Starting from the {TDI, TDIT, TDIS} macro, the order of the peripheral BSC's obtained by tracing fanouts of their TDO ports must be the same as the order obtained by traversing I/O sites in the counter-clockwise direction from the {TDI, TDIT, TDIS}.

10.(W)If there are any unused I/O sites then there should be zero ENSCANI macros.

11.(E) The number of I/O sites between a peripheral BSC and the fanout instance of its TDO port must be <= 7 (not including the I/O sites of the driver and the receiver).

Appendix A.5: Hi-Drive Outputs

1. (E) There must be no HIDRIVE property on any BSC output or bidirectional macro, or on the TDO/TDOA macro.

Appendix A.6: JTAG Clock & Control Signal Distribution

The rules in Sections A.6.1, A.6.2 and A.6.3 are split into two cases. Case I should be used for large and/or high speed arrays. Case II can be used for small and/or low speed arrays. The case type can be specified in the "design_info" file. A given design must follow either Case I or Case II rules for all six signals, namely CKDR, SHDR, UDDR, IMC and OMC. Case types cannot be mixed on the same chip. Also, an "E" or "W" in parenthesis classifies each rule as either an error or a warning.

The following rule applies to all six of these signals:

1. (E) All JTAG buffers must reside within 25 I/O sites of the nearest INPVSS or BOTHVSS macro, and within 25 I/O sites of the nearest INPVDD or BOTHVDD macro.

Appendix A.6.1: CKDR Distribution

The rules in this section verify proper distribution of the CKDR signal in the periphery. Case I uses a central CKDRMID/P macro driving a CKDRCC1/P and a CKDRCC2/P macro as shown in Figure 3-1. Case II only requires a single CKDR macro as shown in Figure 3-5.

CASE I - Large and/or High Speed Arrays (see Figure 3-1)

1. (E) There must be one and only one occurrence of each of the following macros: CKDRCC1/P, CKDRCC2/P, CKDRMID/P, and TDOA. There must be no occurrences of the CKDR/P macro.
2. (E) The CKDRMID/P must be driven by a core macro.
3. (E) CKDRMID/P can only drive CKDRCC1/P and CKDRCC2/P.
4. (E) CKDRCC1/P and CKDRCC2/P can only be driven by a CKDRMID/P.
5. (E) CKDRCC1/P and CKDRCC2/P cannot drive same net.
6. (E) CKDRCC1/P and CKDRCC2/P can only drive the CKDR port of peripheral BSC's. Conversely, the CKDR port of peripheral BSC's can only be driven by either CKDRCC1/P or CKDRCC2/P.
7. (E) CKDRCC1/P must drive only the CKDRNET1 net.
8. (E) CKDRCC2/P must drive only the CKDRNET2 net.
9. (E) The CKDRMID/P must reside in an I/O site between TDI and CKDRCC1/P, or between CKDRCC2/P and TDOA, or between TDOA and TDI.
10. (E) There must not be any common IO sites among IO sites covered by physical CKDRNET1 and physical CKDRNET2.
11. (E) CKDRCC1/P must reside at an IO/power/ground site covered by physical CKDRNET1. CKDRCC2/P must reside at an IO/power/ground site covered by physical CKDRNET2.

In Figure 3-1, branches (a) and (b) comprise CKDRNET1 and branches (c) and (d) comprise CKDRNET2.

12.(E) IMID2CC1 - MID2CC2I/[(MID2CC1 + MID2CC2)/2] <15%, where MID2CC1 = # I/O sites between CKDRMID/P and CKDRCC1/P. MID2CC2 = # I/O sites between CKDRMID/P and CKDRCC2/P.

13.(E) $\frac{|\text{\# loads on branch (a) - \# loads on branch (c)}|}{[\text{\# loads on branch (a) + \# loads on branch (c)}]1/2} < 15\%$

14.(E) $\frac{|\text{\# loads on branch (b) - \# loads on branch (d)}|}{[\text{\# loads on branch (b) + \# loads on branch (d)}]/2} < 15\%$

15.(E) $\frac{|(\text{\#loads onCKDRNET1})-(\text{\#loads onCKDRNET2})|}{(\text{\# loads on CKDRNET1 + \# loads on CKDRNET2})/2} < 15\%$

16.(W) $\frac{|\text{\# loads on branch (a) - \# loads on branch (b)}|}{[\text{\# loads on branch (a) + \# loads on branch (b)}]/2} < 15\%$

17.(W) $\frac{|\text{\# loads on branch (c) - \# loads on branch (d)}|}{[\text{\# loads on branch (c) + \# loads on branch (d)}]/2} < 15\%$

CASE II - Small and/or Low Speed Arrays (see Figure 3-5)

1. (E) There must be one and only one occurrence of the CKDR/P macro.
2. (E) There must be no occurrences of the CKDRCC1/P, CKDRCC2/P, or CKDRMID/P macros.
3. (E) The CKDR/P must be driven by a core macro.
4. (E) The CKDR/P can only drive the CKDR port of peripheral BSC's. Conversely, the CKDR port of peripheral BSC's can only be driven by the CKDR/P.
5. (E) The TDO macro must be used instead of the TDOA macro.

Appendix A.6.2: SHDR, UDDR Distribution

The rules in this section verify proper distribution of the SHDR and UDDR signals in the array periphery. The rules are given for SHDR explicitly. These need to be repeated for UDDR by substituting "UDDR" wherever "SHDR" appears.

CASE I - Large and/or High Speed Arrays (see Figure 3-3)

1. (E) There must be two and only two occurrences of the SHDR/P macro.
2. (E) Both SHDR/P's cannot drive the same net.

3. (E) Each SHDR/P must be driven by a core macro.
4. (E) There must be one and only one occurrence of ISO/P macro.
5. (E) Each SHDR/P can only drive the SHDR port of peripheral BSC's. Conversely, the SHDR port of peripheral BSC's can only be driven by a SHDR/P.

In Figure 3-3, the SHDR/P macro driving net1 is called 'shdr-i1' and the SHDR/P macro driving net2 is called 'shdr-i2', for the purpose of explanation.

6. (E) shdr-i1 must reside in an I/O site between TDOA and ISO/P, as IO sites are traversed counter-clockwise from TDOA. shdr-i2 must reside in an I/O site between TDOA and ISO/P, as IO sites are traversed clockwise from TDOA.
7. (E) All the peripheral BSC's on IO sites between TDOA and ISO/P, as IO sites are traversed counter-clockwise from TDOA, must have their SHDR ports driven by shdr-i1. All the peripheral BSC's on IO sites between TDOA and ISO/P, as IO sites are traversed clockwise from TDOA, must have their SHDR ports driven by buffer shdr-i2.

In Figure 3-3, branches (a) and (b) comprise net1 and branches (c) and (d) comprise net2.

8. (W) $\frac{|\#\text{ loads on branch(a)} - \#\text{ loads on branch(b)}|}{[\#\text{ loads on branch (a)} + \#\text{ loads on branch (b)}]/2} < 15\%$
9. (W) $\frac{|\#\text{ loads on branch(c)} - \#\text{ loads on branc (d)}|}{[\#\text{ loads on branch (c)} + \#\text{ loads on branch (d)}]/2} < 15\%$
10. (W) $\frac{|(\#\text{ loads on net 1}) - (\#\text{ loads on net 2})|}{(\#\text{ loads on net 1} + \#\text{ loads on net 2})/2} < 15\%$

CASE II - Small and/or Low Speed Arrays (see Figure 3-6)

1. (E) There must be one and only one occurrence of the SHDR/P macro.
2. (E) The SHDR/P must be driven by a core macro.
3. (E) The SHDR/P can only drive the SHDR port of peripheral BSC's. Conversely, the SHDR port of peripheral BSC's can only be driven by a SHDR/P.
4. (E) There must be no occurrences of the ISO/P macro.

Appendix A.6.3: IMC, OMC Distribution

The rules in this section verify the distribution of the IMC and OMC signals in the periphery. The rules are given for IMC explicitly. These need to be repeated for OMC by substituting OMC in place of IMC.

CASE I - Large and/or High Speed Arrays (see Figure 3-4)

1. (E) There must be two and only two occurrences of IMCDR/P.
2. (E) Both IMCDR/P's cannot drive the same net.
3. (E) An IMCDR/P must be driven by a core macro.
4. (E) Each IMCDR/P can only drive the IMC port of peripheral BSC's. Conversely, the IMC port of peripheral BSC's can only be driven by an IMCDR/P.

In Figure 3-4, the IMCDR/P driving net1 is called 'imcdr-i1' and the IMCDR/P driving net2 is called 'imcdr-i2', for the purpose of explanation.

5. (E) imcdr-i1 must reside in an IO/power/ground site between CKDRCC1/P and CKDRCC2/P, as I/O sites are traversed clockwise from CKDRCC1/P. imcdr-i2 must reside in an IO/power/ground site between CKDRCC1/P and CKDRCC2/P, as I/O sites are traversed counter-clockwise from CKDRCC1/P.
6. (E) All the peripheral BSC's on IO sites between CKDRCC1/P and CKDRCC2/P, as I/O sites are traversed clockwise from CKDRCC1/P, must have their IMC ports driven by imcdr-i1. All the peripheral BSC's on IO sites between CKDRCC1/P and CKDRCC2/P, as I/O sites are traversed counter-clockwise from CKDRCC1/P, must have their IMC ports driven by imcdr-i2.
7. (W) $\frac{|\#\text{ loads on branch(a)} - \#\text{ loads on branch(c)}|}{[\#\text{ loads on branch (a)} + \#\text{ loads on branch (c)}]/2} < 15\%$
8. (W) $\frac{|\#\text{ loads on branch(b)} - \#\text{ loads on branch(d)}|}{[\#\text{ loads on branch (b)} + \#\text{ loads on branch (d)}]/2} < 15\%$

CASE II - Small and/or Low Speed Arrays (see Figure 3-6)

1. (E) There must be one and only one occurrence of the IMCDR/P macro.
2. (E) The IMCDR/P must be driven by a core macro.
3. (E) The IMCDR/P can only drive the IMC port of peripheral BSC's. Conversely, the IMC port of peripheral BSC's can only be driven by the IMCDR/P.

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Appendix B: BSC Modeling & TAP Controller Design for Mustang Compatibility

Appendix B.1: BSC Mustang Model

The peripheral boundary scan cells use a shadow register structure similar to that shown in Figure B-1.

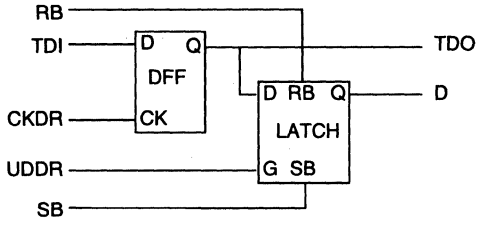

Figure B-1 General JTAG Shadow Register Structure.

Mustang cannot correctly model this functionality because the shadow latch is not on a scan chain, so a more limited Mustang-compatible model is used. The shadow latch is modeled as a combinatorial element instead of being static. This is done by creating a primitive with the truth table shown in Table B-1:

Table B-1 Truth Table for JTAG Combinatorial "jlatch"

D	G	RB	SB	Q
X	X	0	1	0
X	X	1	0	1
0	1	1	1	0
1	1	1	1	1
All Other States				X

The primitive operates with the constraint that either one of the reset / set pins (RB, SB) must be active or the gate (G) must be active with the data (D) input known. Any other combination will result in an X being generated at the output.

The JTAG boundary scan cell Mustang models have been constructed using this primitive. As a result, Mustang can detect all faults within the BSC except a stuck-at-one fault on the gate input of the latch.

Appendix B.2: TAP Controller

The TAP Controller implementation given in the IEEE 1149.1 JTAG specification is shown in Figure B-2. This TAP Controller design is not compatible with scan design rules because:

i) it contains static elements that are not scannable

ii) it contains signals which are gated by the TCK clock

iii) both the rising and falling edges of TCK are used as active edges.

In order to correct these problems the following steps were taken:

1. Two extra inputs and one extra output have been added to the TAP Controller. The MTST input is active high whenever the design is to be used in Mustang-compatible mode (such as during production test at Motorola).Scan data enters the TAP Controller via the TDI input and leaves via the TDO output. The TDI and TDO mentioned here are ports on the TAP Controller macro and should not be confused with the TDI and TDO pins.
2. All of the flip flops were changed to scannable devices.
3. The inverter in the path generating TCKB was replaced with an exclusive-or gate to ensure that all of the static elements will be clocked on the rising edge of the TCK clock. The paths to the CKIR and CKDR outputs are unaltered since these already clock on the correct edge.
4. NAND gates were added to the following outputs to put them into the specified state during Mustang scan mode:
   a. SL = 1: TDO used as scan output for Instruction Register scan chain.
   b. ENABLE = 1: Enables TDO 3-state output.
   c. RB = 1: Prevents reset of JTAG logic while shifting scan chains.
   d. SHIR = 1: Puts Instruction register into scan mode.
   e. SHDR = 1: Puts Data registers into scan mode.
   f. UDDR = 1: Holds data register shadow latches transparent.

In addition, the TMS input is AND'ed with the MTST input to form the Mustang Scan Enable (MSE) signal. MSE is passed to the scan enable of all flip-flops in the TAP Controller. When high, MSE places these flops in scan/shift mode.

Suppose a core/system flop gets its data from an input BSC having the shadow register structure shown in Figure B-1. The latch within this BSC is driven by UDDR, which is derived from clock TCK in Figure B-2. Since the latch in the BSC must be modeled as a combinatorial "JLATCH," Mustang sees a clock derivative (UDDR) propagating through the JLATCH to drive the data input of the system flop. This condition violates scan design rules; state element data inputs cannot be derived from a clock. The problem can be overcome in the TAP Controller by replacing the NAND which gates TCK to UDDR with a flip-flop which is clocked on the falling edge of TCK. This has the additional effect of extending the update pulse from half a cycle to a complete cycle, which satisfies the Mustang requirement that the data input to a flop be an NRZ (non-pulsed) waveform. (UDDR still drives the data input of the core/system flop via the combinatorial JLATCH.)

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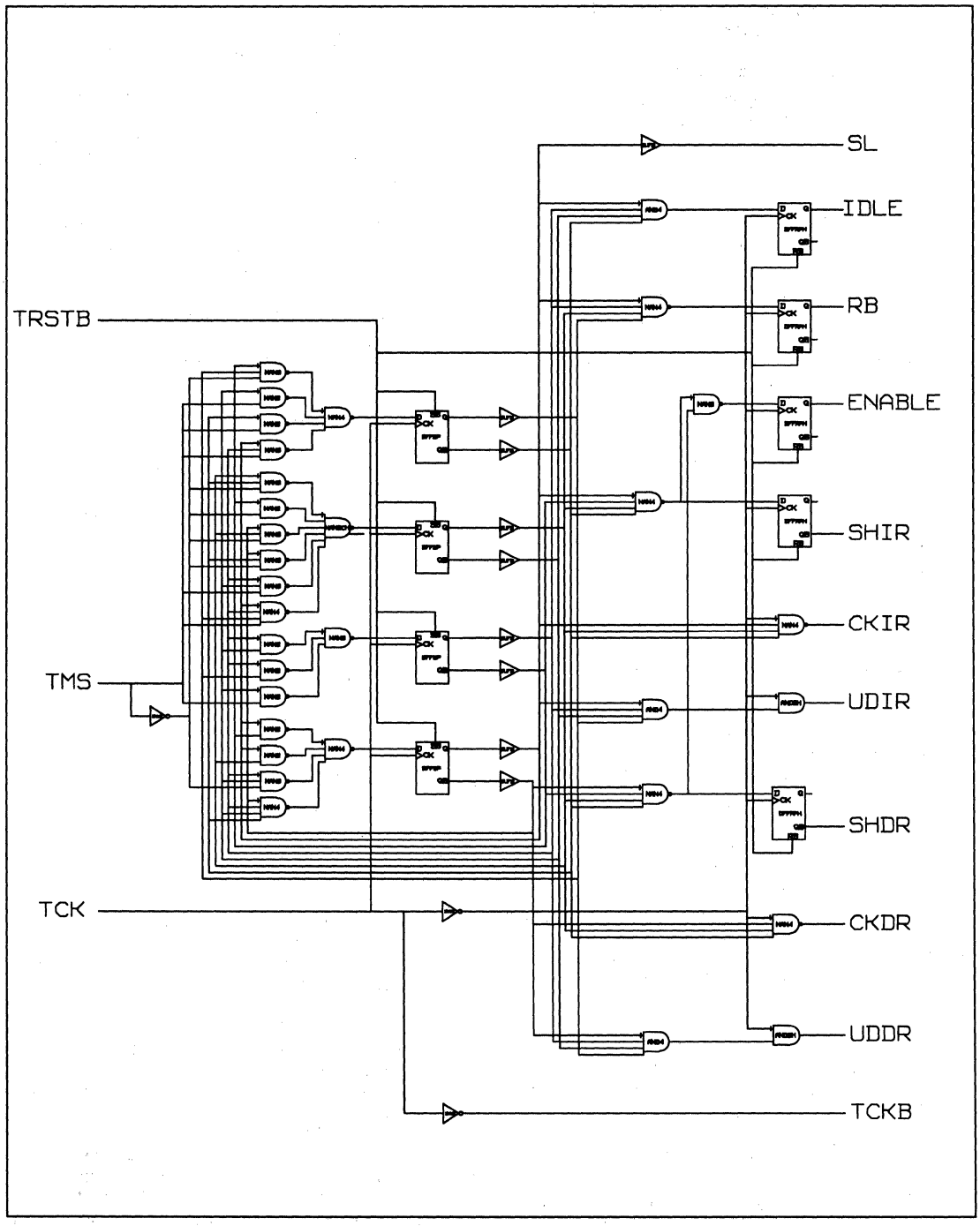

Figure B-2 TAP Controller Shown in IEEE 1149.1 JTAG Specification

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Since the latch portion of the Instruction Register has been changed to a flop (see Figure 4-1) this problem does not exist on UDIR, which therefore need not be generated by a flop. In fact, UDIR must not be generated by a flop now that it drives a flop clock port instead of the combinatorial JLATCH. The reason is that Mustang requires flops to have pulsed clocks.

The new functionality for UDDR is shown in the waveform diagram of Figure B-3, which demonstrates the loading of a data register.

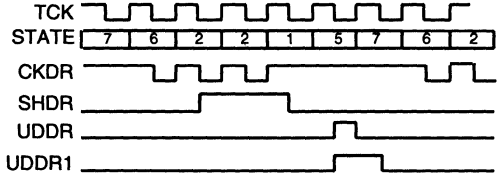

Figure B-3 JTAG Control Signals Waveform Diagram

The waveform diagram shows the operation of the TAP Controller while performing the fastest cycle of loading and updating the data register. This shows the shortest time possible, during JTAG operation, between UDDR going inactive and the next occurrence of a CKDR pulse. UDDR is the current update signal while UDDR1 is the signal that is generated by the new TAP Controller design in Figure B-4. This diagram shows that the addition of a flip-flop on the UDDR signal causes no functional change in the operation of the JTAG boundary scan circuitry.

Some additional circuitry has been added to the TAP Controller to improve its fault coverage:

1. A large number of faults on the NAND gates on the left are not detectable because the TMS line which feeds into them also puts the flip flops which observe them into scan mode. This is resolved by adding gating to allow the TDI input to control the NAND gates when the device is in Mustang test mode.
2. Faults on gates feeding the CKDR, CKIR, and UDIR outputs are undetected because they are unobservable. (MTST overrides the TAP Controller state for control of these signals during Mustang test mode because Mustang requires control of all clocks from a pin, in this case the TCK pin.) The fault coverage is improved by monitoring all three signals with an exclusive-or gate, which is observed by a flop that is added to the scan chain.

Appendix C: EDIFMERGE Attribute File Entries for Peripheral JTAG Macros

Figure C-1 shows the JTAG portion of the Attribute file for the circuit in Section 4.5, Figure 4-7 (if this circuit had been entered using Verilog HDL instead of schematic capture).

In Figure C-1, comment lines are denoted by an asterisk as the leading character. The keyword "-INSTANCE" is followed by a Fix entry for each non-bonded macro in the design. In each FIX entry the macro instance name is copied from the Synopsys EDIF netlist, and is the instance "name" with any leading non-alphabetic characters stripped off. (The instance "rename," which is not used, is enclosed in quotes and follows the instance "name" in the netlist.)

The ISOP macro requires two entries in the Attribute file. In the entry which follows the "-NONLOGICCELL" keyword, the instance name is arbitrarily chosen. This instance name is then used in the second ISOP entry, which follows the "-INSTANCE" keyword along with the entries for the other non-bonded macros.

Note that the TAP macros are fix-placed via the IO_PIN1 property, not the FIX property, since these are input macros which connect to package pins.

```
-NONLOGICCELL
*cell type          instance name
 ISOP               isop;

-PORT
*Signal Name        property        Pin #
 TMS                IO_PIN1         "39";
 TCK                IO_PIN1         "38";
 TDOA               IO_PIN1         "33";
 TDI                IO_PIN1         "32";

-INSTANCE
*instance name      property        I/O site #
 imcdr_1            FIX             "IO10";
 ckdrmid p          FIX             "IO11";
 omcdrp_1           FIX             "IO17";
 ckdrcc1p           FIX             "IO115";
 shdr_1             FIX             "IO116";
 uddrp_1            FIX             "IO121";
 isop               FIX             "IO219";
 imcdr_2            FIX             "IO220";
 omcdrp_2           FIX             "IO225";
 ckdrcc2p           FIX             "IO323";
 shdr_2             FIX             "IO324";
 uddrp_2            FIX             "IO329";
```

Figure C-1 JTAG-Macro Portion of Attribute File for H4C123 in 160 QFP(CD) or MicroCool

Non-JTAG hi-drive outputs and bidirectionals are designated by a HIDRIVE property. However each JTAG hi-drive is a separate macro, which has a COMPLEX_HIDRIVE property instead of a HIDRIVE property. COMPLEX_HIDRIVE properties are added to the EDIF netlist automatically by the NETLIST program, therefore a JTAG hi-drive has no entry in the Attribute file for either a HIDRIVE property or a COMPLEX_HIDRIVE property.

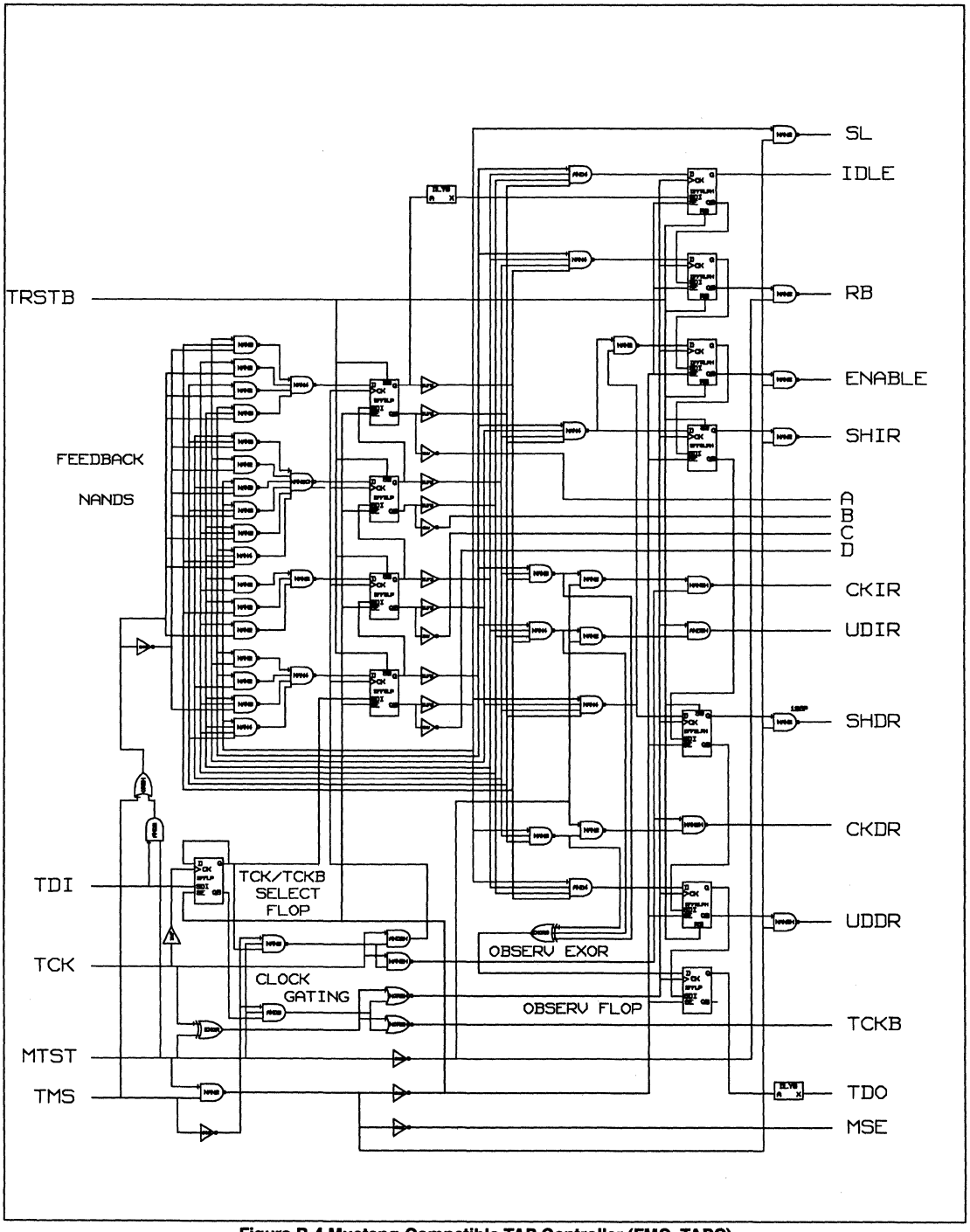

Figure B-4 Mustang-Compatible TAP Controller (FMC_TAPC).

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Appendix D: JTAG for H4CPlus

The H4CPlus JTAG implementation is identical to the H4C JTAG implementation with the exeption of the changes described below.

1. The TDO and CKDR macros do not exist because the "Small or Low-Speed Array" distribution scheme (see section 3.3) has not been implemented.
2. The H4C TDOA macro has been renamed "TDOUT" in H4CPlus, and the mux and flop (see Figure 2-1) have been removed from the TDOUT macro. This logic must now be implemented in the array core, where the customer can modify it if he wishes.
3. Only the "non-P" version exists for the following macros:
   - ISOR
   - CKDRCC1
   - CKDRCC2
   - CKDRMID
   - SHDR
   - UDDR
   - IMCDR
   - OMCDR
   - ENSCANJ
   - TDBUF

   The ISOR, CKDRCC1, CKDRCC2, ENSCANJ and TDBUF macros can now be placed on normal I/O sites as well as on output-power/gnd sites. However, they cannot be placed on input-power/gnd sites. All the rest of these macros can be placed by themselves on normal I/O sites, output-power/gnd sites, and input-power/gnd sites.
4. The ISOR macro now makes a physical cut in the CKDR ring, in addition to the SHDR and UDDR rings as in H4C. The ISOR also contains a flop and an inverter such that the flop is clocked on the falling edge of CKDR (see Figure 7-1). This flop is placed in the shift path of the boundary scan chain to prevent hold time violations due to clock skew between the two physically separate CKDR nets. Unlike H4C, all BSC's no longer share a common clock net, therefore hold time violations between BSC's are of concern. However, the falling-edge flop inside the ISOR macro allows CKDRNET2 in Figure 7-1 to be skewed from CKDRNET1 by up to half a cycle of CKDR without causing a hold time violation. The benefit realized is that there is no fake cut required in the netlist for accurate simulation (see section 3.2), therefore the need for tight balancing of the CKDR buffers is eliminated, along with the associated ERC rules. Simulation using PREDIX RC's now will show if enough skew exists between CKDRNET1 and CKDRNET2 to cause timing violations when shifting data through the boundary scan chain.
5. The customer must use PREDIX to compute the actual RC's for peripheral JTAG nets, in order to do accurate JTAG simulations. DECAL merges the PREDIX peripheral RC's with either DECAL-estimated RC's for the array core (for pre-layout simulations) or with Gate Ensemble-generated actual RC's for the array core (for pre-layout simulations).
6. The paralleled output buffer portion of a hi-drive, such as an ON32, can reside on an ouptut-gnd I/O site if that gnd is an OVSSP macro.

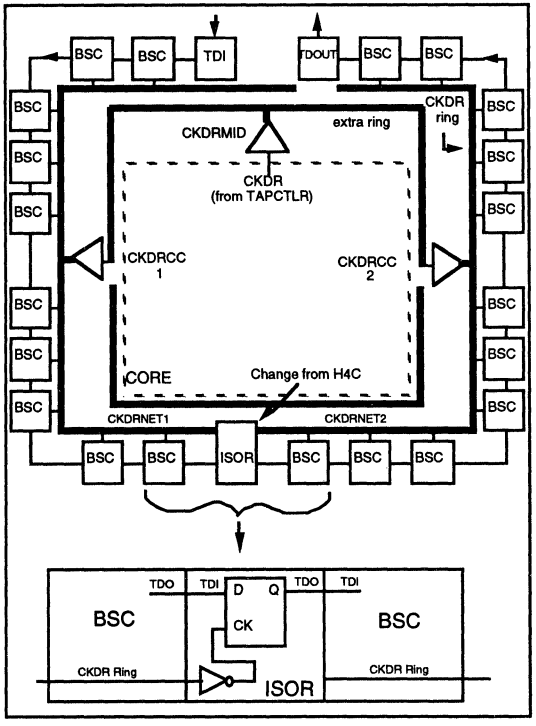

Figure D-1 CKDR Distribution to I/O Boundary Scan Cells on H4CPlus Arrays

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H4CPlus™ Series 3.3V/5V Design Considerations

Prepared by: David Crohn
and Peter Economopoulos
Motorola, Chandler AZ

INTRODUCTION

The H4CPlus Series technology offers the ability to implement designs with one of two possible core voltages, in combination with all 3V, all 5V, or mixed 3V/ 5V I/O designs. To achieve this end, it is helpful to understand how this technology is implemented, and how to incorporate these details into the design via Motorola's Open Architecture CAD System (OACS™) interface.

Throughout this application note, 3.3-volt I/Os will be loosely referred to as 3-volt I/Os, since the operating range is selectable from 3.0 ±.3 volts, to 3.3 ±.3 volts, and is not required to be 3.3 volts.

This application note is best understood if the reader has a working knowledge of the Motorola OACS[1] design tools.

OBJECTIVE

This application note provides the knowledge necessary to implement designs that are all 3V, all 5V, or mix both 3- and 5- volt I/Os and a single core voltage of either 3 or 5 volts in the H4CPlus Series CMOS array family.

1. DESIGN DETAILS

1.1 Power Rail Configuration

An H4CPlus array has five distinct power and ground rails, which are shown in Figure 1. An H4CPlus Series array contains an output power rail for powering 5-volt outputs named the OVDD5 rail, an output power rail for powering 3-volt outputs named the OVDD3 rail, an output ground bus named OVSS, and the core power and ground rails named VDD and VSS, respectively.

1.2 Technology Selection

There are two distinct technology libraries to choose from when implementing an H4CPlus design. They are the H4CP3 library, which contains all of the 3-volt core macros along with the 3-to-3 and 3-to-5 volt I/Os, and the H4CP5 library, which consists of all the 5-volt core macros with the corresponding 5-to-5 and 5-to-3 volt I/Os available for that technology. The selection process is the same as selecting between array families (e.g., HDC and H4C Series) in the OACS DESIGN_INFO tool today. Once a given technology has been selected, accessing macros in the other technology is neither possible, nor desirable.

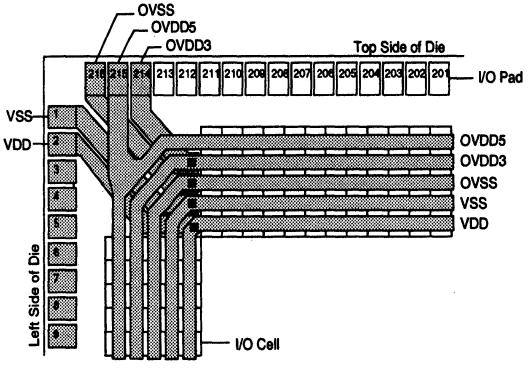

Figure 1 H4CPlus Power and Ground Busses

1.3 Macro Naming Conventions

The H4CPlus macro naming conventions have been selected to simplify the design process. There are two distinct conventions to describe: those for the core macrocells, and those used in the I/O portion of a design.

1.3.1 Core Macrocells

Core macros have the same name regardless of technology selected. The only difference between the technologies for core macros is the timing data, since H4CP3 has been characterized at 3.3 volts, and H4CP5 at 5.0 volts. Section 1.2 describes the H4CP3 or H4CP5 timing data selection process.

1.3.2 I/O Macrocells

A consistent naming convention has been put in place so that I/O selection can be done easily. The two key characters used are "L" and "X". Remembering the following two rules —

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that always apply— will simplify macro selection. An "L" in the I/O macro name always indicates that the macro has been designed for a 3-volt external interface. An "X" always indicates that there is a translation of voltage between the core and the external interface voltage.

Consequently, the H4CP3 technology will contain only I/O macros with either an "L" or an "X" in their names, but not both. The names of H4CP5 I/O macros will either contain both letters (L and X) together or neither letter- e.g. ONLX8 or ON8.

For example, an ONL8 is an 8mA output with a 3-volt core and a 3-volt interface. An ONX8, is a macro with a 3-volt core and a 5-volt interface. Both of these macros would be found only in the H4CP3 library. An ON8 is a 5-volt core, 5-volt interface macro. An ONLX8 is a 5-volt core, 3-volt interface macro. Both of these macros would be found only in the H4CP5 library.

1.3.3 Special 3-Volt I/O Considerations

The usage of 3-volt receivers in a technology that allows 3 and/or 5-volt supplies has three points that require explanation.

The first is with respect to the input threshold. Due to the small difference between 3-volt CMOS and TTL thresholds, no distinction is made. Consequently, an ILTN macro will not be found in the H4CP3 library. Instead an ILCN with a VDD/2 threshold is used, since the small difference in threshold was not considered justification enough to create a separate 3-volt TTL receiver at this time.

The next design impact to consider is steady state current draw consumed by 3-volt inputs with a 5-volt core voltage, such as an ILTXN. Receivers are powered by the core voltage, which in this case would be 5 volts. A high on the 3-volt input would result in the receiver never completely cutting off the P-channel transistor. For a 3.3-volt signal, and a 5-volt core with typical conditions this current would be 225µA, and with a TTL input high of 2.0 volts this current would be 850µA.

The steady state current is only a power issue and will cause no degradation in the performance or functionality of the receiver over time, but the designer needs to be aware that this condition exists. This current is included by ERC during its DC power consumption analysis.

The final point is in regards to the type of receiver a 3-volt output is driving. three-volt outputs should not drive CMOS inputs, since VOH requirements can not be guaranteed. ERC will flag any invalid bi-directional combinations in a design, such as a BICN used with a BONLX8T. This check cannot be done for external loads, since ERC does not know what type of receiver is being driven by the 3-volt output. Refer to the "H4CPlus Series Design Reference Guide" [2] DC Electrical Characteristics chapter for the 3- and 5- volt specifications when implementing the I/O portion of the design.

1.4 Power Bus Tying

Many legitimate power bus tying combinations are possible with H4CPlus. Both output rails (OVDD5 and OVDD3) can be tied, or the core power rail can be tied to either output power rail, or all three power rails can be tied together as well.

The mechanism for choosing which buses to tie is the OACS DESIGN_INFO tool. The first selection to make is whether to use the 3-volt or 5-volt technology. The next selection is whether the I/O is all 3-volt, all 5-volt, or a mix of the two. An important point to understand is that this question pertains to the interface voltage, and not necessarily the voltage at which the I/O operates.

Making this selection isn't always as easy as it would appear to be. At first glance, a design with a 3-volt core and all 3-volt outputs with a 5-volt input, such as an ICXN, may appear to only require 3-volt power since inputs are powered from the core. Even though this macro is powered from the core, it still requires the OVDD5 power to be provided with 5 volts to prevent forward-biasing the protection diode when 5 volt signals are received at the input. So even though the input macro and all of the outputs are powered by 3 volts, it is incorrect to select all 3-volt I/O, since 5 volts is required as well.

The basic rule of thumb is this: The only time "I/O Type 3.3v" can be selected in DESIGN_INFO is if all I/O macros used contain an "L" in their name. The only time "I/O Type 5.0v" can be selected in DESIGN_INFO is if all I/O macros do not contain an "L" in their name. Any other scenario would require that "I/O Type mixed" be selected in DESIGN_INFO.

The final selection to make is whether or not to tie the core power rail to either of the output rails, if outputs exist in the design that operate at the same voltage as the core.

For example, if H4CP5 is the technology selected, and all 3.3-volt I/O is indicated, then the question to answer regarding the tying of the core to the output rail would disappear, since all the I/O are at a different potential than the core.

There is one exception to designer-controlled bus tying selection. If all 3.3-volt or 5-volt I/O is selected, then by default the two output power buses OVDD3 and OVDD5 will be tied. There are several reasons for this. First, dedicated power pins to the unused power rail can now be used to provide power to the utilized power rail. Second, this prevents a floating metal ring around the array from building up excess charge. Finally, the added bus capacitance and reduced pin inductance are advantageous for improving the SSO environment.

Valid DESIGN_INFO selections are verified by ERC. Running ERC early on, and frequently as the I/O portion of the design is implemented, prevents time consuming corrections that may not otherwise be found until the final stages of ASIC development.

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1.4.1 Power Bus Macro Selection

A full set of design selectable power macros exist that enable designers to place powers and grounds where necessary, and either tie or provide the individual rails as needed by the design. Table 1 gives the macro name and the associated power or ground bus supplied by that macro. Table 2 shows which programmable power macros to use based on the design outlined by entries in DESIGN_INFO. Figures 2-11 illustrate the core, I/O, and bus tie connections for the various scenarios listed in Table 2.

Table 1. Macro Definition

MACRO NAME	BUS SUPPLIED
ALLVDD	VDD,OVDD3,OVDD5
BOTHOVDD	OVDD3, OVDD5
BOTHVDD3	VDD, OVDD3
BOTHVDD5	VDD, OVDD5
OVDD5	OVDD5
OVDD3	OVDD3
VDD	VDD
OVSS	OVSS
VSS	VSS

Table 2. Macro Selection

Customer Options in DESIGN_INFO			MACRO NAME							
Technology Selection	I/O Type	Tie Core Rail to I/O Rail	VDD	OVDD3	OVDD5	ALLVDD	BOTHOVDD	BOTHVDD3	BOTHVDD5	Figure
H4CP3	All 3 Volt	No	X				X			2
H4CP3	All 3 Volt	Yes				X				3
H4CP3	Mixed	No	X	X	X					4
H4CP3	Mixed	Yes			X			X		5
H4CP3	All 5 Volt	N/A	X				X			6
H4CP5	All 5 Volt	No	X				X			7
H4CP5	All 5 Volt	Yes				X				8
H4CP5	Mixed	No	X	X	X					9
H4CP5	Mixed	Yes		X					X	10
H4CP5	All 3 Volt	N/A	X				X			11

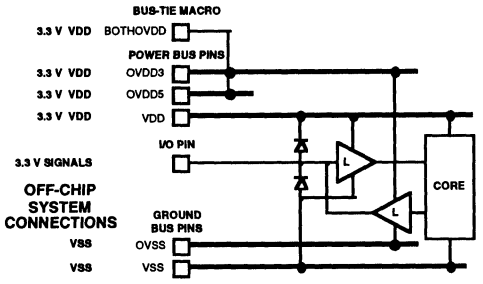

Figure 2 Example of a 3.3 V Core with 3.3 V I/O and OVDD3 & OVDD5 Tied

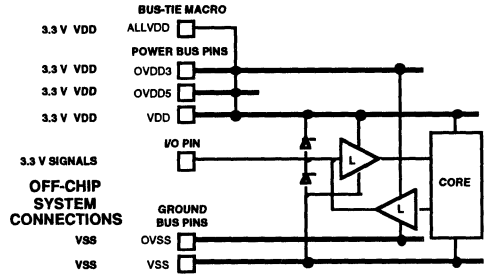

Figure 3 Example of a 3.3 V Core with 3.3 V I/O and All VDD Tied

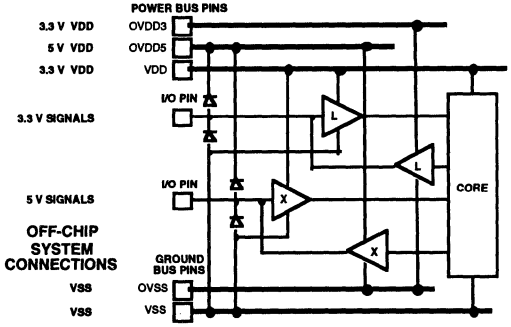

Figure 4 Example of a 3.3 V Core with Mixed 3.3V/5V I/O and No VDD Ties

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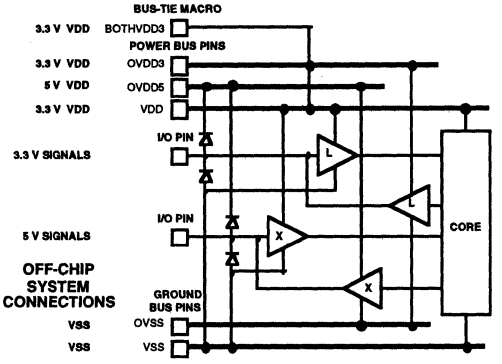

Figure 5 Example of a 3.3 V Core with Mixed 3.3V/5V I/O and OVDD3 & VDD Tied

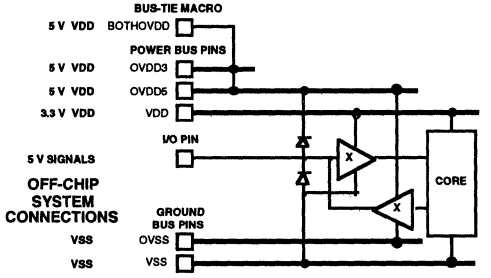

Figure 6 Example of a 3.3 V Core with 5 V I/O and OVDD3 & OVDD5 Tied

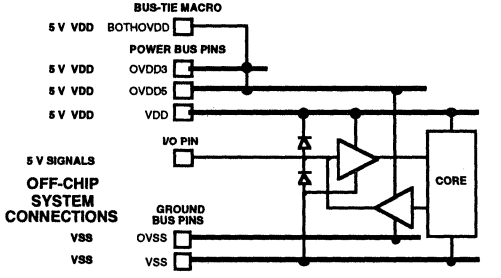

Figure 7 Example of a 5 V Core with 5V I/O and OVDD3 & OVDD5 Tied

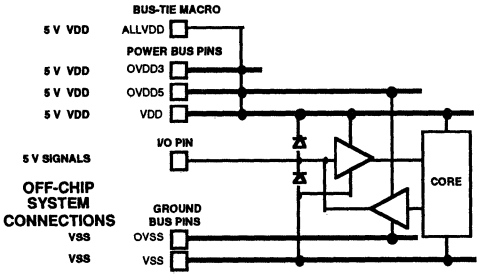

Figure 8 Example of a 5 V Core with 5V I/O and All VDD Tied

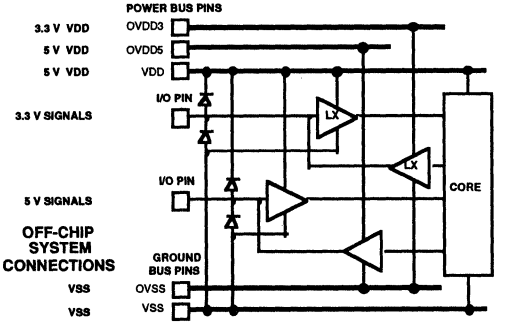

Figure 9 Example of a 5 V Core with Mixed 3.3V/5V I/O and No VDD Tied

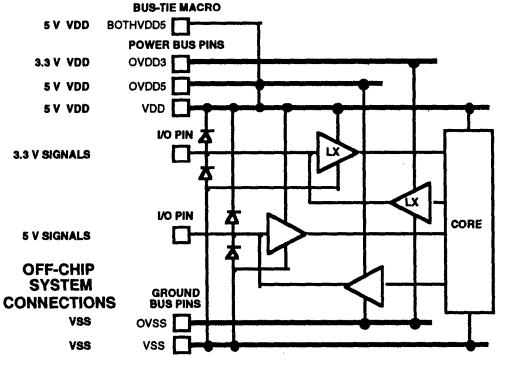

Figure 10 Example of a 5 V Core with Mixed 3.3V/5V I/O and OVDD5 & VDD Tied

A

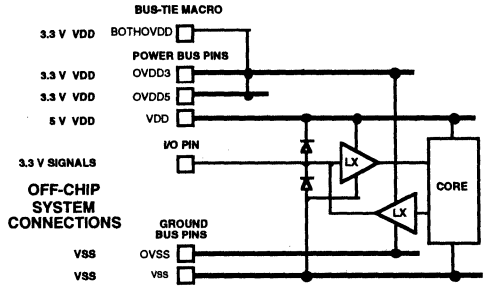

Figure 11 Example of a 5 V Core with 3.3 V I/O and OVDD3 & OVDD5 Tied

1.5 Propagation Delay Adjustments

When simulating with timing, propagation delay adjustments can be applied to macros powered by 3 volts independently of macros powered by 5 volts. The DESIGN_INFO tool has entries for a designer to select best-, typical-, and worst-case voltages for the 5-volt rail and for the 3-volt rail independently. The associated delay adjustments would then be applied to macros powered by the given rail.

For example, a design with a 5-volt core may have all 3-volt I/Os, but it is desired to run the I/Os at 3.0 rather than at 3.3 volts. Simply modify the values in DESIGN_INFO to be 3.0±.3 volts, and leave the 5-volt rail at 5 volts. The appropriate delay adjustments will then be applied to the 3-volt I/Os, independently from the adjustments made to the macros powered by the 5-volt supply.

There are limits to the range of voltage adjustments possible. If the H4CP3 technology is selected, and the designer requests the design's core power supply to be 4.5 volts, then an error will occur, since if this is the true operating voltage, then a switch to the H4CP5 technology should be considered. H4CP5 has been characterized at 5.0 volts, and provides more accurate timing being scaled to 4.5 volts, rather than scaling 3.3-volt data to 4.5 volts, which exceeds the range of the scaling equations.

Although ranges typically selected for the 3-volt supply will be from 2.7 volts (worst-case) to 3.6 volts (best-case), DESIGN_INFO will allow selections up to 4.0 volts to be made. Similarly for the 5-volt supply, typical selections will be from 4.5 volts (worst-case) to 5.5 volts (best-case), but selections down to 4.0 volts are allowed. Selections outside these ranges will cause fatal errors when DECAL [1] attempts to apply voltage adjustments that don't exist.

The designation for the two supplies in DESIGN_INFO is VDD for the core and output power rail(s), if supplied by the same voltage, and VDD2 for the alternate output power rail. So, if "Technology H4CP3" is selected, then the default range for VDD will be from 3.0 to 3.6 volts, and from 4.5 to 5.5 volts for VDD2. If "Technology H4CP5" is selected, then the default range for VDD will be from 4.5 to 5.5 volts, and from 3.0 to 3.6 volts for VDD2. If the "I/O Type" and "Technology" selections are for the same voltage, the VDD2 will be removed, and only the VDD entry will remain, since at that point it is known that the core and both output power rails will be operating at the same potential.

1.6 Pull-ups and Pull-downs

Pull-downs always tie to the output ground rail OVSS. The pull-ups, however, always tie to the core VDD rail. There are two scenarios which present potential design concerns.

The first scenario is for designs which have a 3-volt core and 5-volt inputs. The consequence is having the 5-volt input to 3-volt core potential difference across the pull-up resistor. This is not a serious problem, since the current through the pull-up will be small, with the difference of the 5-volt signal to the 3-volt core across a large resistance.

The second scenario is where bidirectional buses are employed that have 5-volt swings and have pull-ups to the 3-volt core. When the bus is tri-stated, the steady state would be 3 volts, and not 5 volts unless pulled to 5 volts through some external termination.

The suggested approach for these two scenarios is to use pull-downs if some type of pull resistor is absolutely necessary. Pull-ups can be used if the consequences mentioned above are understood, and can be tolerated by a given design. Simulation does not differentiate between pull-ups to 3 and 5 volts, and ERC will not flag these as errors or warnings, since neither scenario is destructive.

1.7 SSO and Power Requirement Rules

This section addresses the electrical restrictions to consider when implementing the I/O portion of a design. These considerations can be broken down into two distinct areas: AC analysis or Simultaneously Switching Outputs (SSO), and DC power requirements.

1.7.1 SSO Analysis

Every output, whether it be 3- or 5-volt, has a drive parameter for it. ERC uses the parameter in conjunction with the package chosen, to do a detailed SSO analysis of a design, and flag problem areas as errors. A more comprehensive explanation of this analysis is covered in Chapter 3 of the "H4CPlus Series Design Reference Guide" [2].

It is this analysis by ERC that offers designers tremendous flexibility when implementing mixed I/O designs. Although one needs to be cognizant of I/O partitioning and placement of power and ground based on the discussion of SSOs in the "H4CPlus Series Design Reference Guide" [2], there are no special restrictions regarding isolation of 3- and 5-volt I/Os, and no ground pad separation requirements. In the event an oversight is made, ERC will inform the designer where the

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violation has occurred so corrections can be made early on in the design cycle.

There is one consideration to keep in mind when implementing the I/O portion of a design. ERC will do either a CMOS or TTL SSO analysis for each of the SSO segments based on the macros found in the SSO segment. An SSO segment is defined as the group of I/Os found between two output power or ground macros. This means there are two distinct SSO segments for ERC to analyze for each output macro. One for the output power rail (OVDD5 or OVDD3) it uses, and one for the output ground rail OVSS. The individual analysis is necessary since the SSO noise sensitivity to the different technologies (e.g., CMOS and TTL for 3 and 5 volts) is different.

The first step in doing SSO analysis is determining whether a SSO segment is TTL or CMOS. If for a given SSO segment an `OUTPUT_THRESHOLD` of TTL is found on an output, any 3-volt outputs are found, or a TTL or 3-volt input are found within the segment, then TTL analysis will be done. Otherwise, CMOS analysis will be applied.

For example, say a design has an SSO segment with an OVDD5 and an OVSS pad on each end. If seven of them drive CMOS loads, and one drives a TTL load (determined by the value of the `OUTPUT_THRESHOLD` property), then TTL SSO analysis will be applied to that segment, even though seven of the loads drive CMOS levels. In this case the SSO noise seen at the TTL output would be the first to fail, and would be the weakest link in that SSO segment. The same argument can be applied if one of the macros in this predominantly CMOS segment were a 3-volt or TTL input.

The point of this discussion is to communicate the flexibility available for creating mixed-voltage I/O designs in the H4CPlus technology, but at the same time pointing out the consequences of design choices, so intended design objectives can be achieved.

1.7.2 DC Power Requirements

There are two basic DC power requirements to meet: IR loss and current density. The rule used for IR loss is the 25 I/O site rule, which states that a macro cannot be more than 25 I/O sites from the power site it is drawing its power from. This applies only to the output power rails, since the core-powered inputs always power CMOS loads, which don't require a steady state current source like an output may potentially need. The same rule is used for both 3- and 5-volt outputs, since the IR loss for the 25 I/O sites has enough margin to satisfy both and is not believed to be overly restrictive in either case.

The current density rule is 64mA per power/ground pin. ERC simply performs a current requirement calculation, divides out the number of powers and grounds available, and determines if there is enough or not. Once again, 3- and 5-volt outputs are given the same treatment. Whether an 8mA output is 3 or 5 volts, it is still designed to drive 8mA, therefore 8mA would be used by ERC during its analysis.

1.8 Testing

Option testing will be done at both 3.3 and 5.0 volts for designs which use both voltages. With two power rails, testing at the simulated voltages is necessary to make sure that the part functions properly at the voltages for which it was intended. Two other points to mention are power cycling of mixed-voltage designs and IDD testing.

1.8.1 Power Cycling

During test and in its application, the 5-volt power should be applied to the option before the 3-volt power, and similarly the 3-volt power should be removed before the 5-volt power. This will prevent parasitic devices from experiencing transients greater than their supply voltage.

1.8.2 Enable IDD (ENID) Pin

H4CPlus offers the ability to do IDD testing without having to put special test vector requirements on designers via the addition of the ENID pin. All H4CPlus designs are required to designate one pin for ENID by instantiating the symbol and defining the `IO_PIN1` property to the desired pin. When ENID is high all pull-up and pull-down resistors, and current sources in differential receivers are disabled, which enables accurate IDD testing independent of the state of the test vector. ENID has an internal pull-down to allow a design to function without tying it to ground. However tying ENID to ground in the system is still advised.

2. SUMMARY

This application note should give a designer having previous OACS experience the information necessary to expeditiously create 3- and/or 5-volt designs using the H4CPlus technology.

REFERENCES

(1) M. Vening, OACS User Guide, Order # 0384-OACS-U.0 from the Motorola ASIC Hotline (1-800-MDS-ASIC in the USA), October 1993.

(2) C. Nakata, J. Brock, H4CPlus Series Design Reference Guide, Order # H4CPDM/D from the Motorola Literature Distribution Center.

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APPLICATION NOTE

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Analog Phase Lock Loop for H4CPlus™ and M5C™ Series Arrays

Prepared by: Roy Jones
Edited by: Clarence Nakata
Application Specific Integrated Circuits Division, Chandler AZ

Table of Contents **Page**

1. Introduction

This application note describes the implementation and use of an analog phase-locked loop, or APLL, which is available on two families of CMOS gate arrays offered by Motorola: the H4CPlus Series arrays and the M5C Series arrays.

Section 2 describes the various versions of the APLL which are offered as different library macros. This section also contains APLL performance data and signal descriptions, and shows the physical placement of the APLL on H4CPlus and M5C arrays.

Section 3 describes how the APLL Verilog simulation model works and how it is used for "system-mode" simulations (as opposed to "option release" simulations).

Section 4 describes Motorola's strategy for testing H4CPlus and M5C arrays that contain an APLL. A Motorola-internal test program is used to test the APLL itself, while user-supplied option release test vectors are used to test the remainder of the chip.

The Appendix shows a schematic of the test circuitry built into the APLL as well as a table of the various operating modes of this circuitry, which is controlled by the Motorola-internal test program.

2. Feature Description

Appendix D and Appendix E contain a comprehensive discussion and analysis of the use of Motorola's digital PLL (DPLL) to speed-up chip-to-chip data transfer by cancelling out on-chip clock network insertion delay. This analysis also applies to an analog PLL (APLL), which can be used for the same purpose.

Compared to the DPLL, the APLL can run faster, and has less in-lock phase error. The APLL also provides on-chip frequency synthesis, which allows a slower/quieter backplane clock frequency to be multiplied up to the desired on-chip clock frequency. The DPLL is not offered in H4CPlus or M5C Series Arrays.

The following table lists the APLL macros available in H4CPlus and M5C arrays.

Table 1 APLL Macros

Macro	Technology	Analog Power	FREF Input Type	N, Loop Divider
AP1	H4CPlus	5 V	CMOS	1 - 4
APD1	H4CPlus	5 V	PECL	1 - 4
AP2	H4CPlus	5 V	CMOS	5 - 16
APD2	H4CPlus	5 V	PECL	5 - 16
APL1	H4CPlus	3.3 V	CMOS	1 - 4
APDL1	H4CPlus	3.3 V	PECL	1 - 4
APL2	H4CPlus	3.3 V	CMOS	5 - 16
APDL2	H4CPlus	3.3 V	PECL	5 - 16
APL1	M5C	3.3 V	CMOS	1 - 16
APDL1	M5C	3.3 V	PECL	1 - 16

PECL is defined as positive- or pseudo-ECL. Table 2 summarizes the performance of the H4CPlus and M5C APLL macros. The "Output Frequency Range" is the *linear* range of the VCO; its full range extends somewhat further. "Max clk tree delay" is the maximum delay that the APLL can handle in its feedback loop before going unstable.

Note 1: All of the performance numbers in Table 2 are preliminary! The guaranteed values for these parameters are in the respective H4CPlus and M5C Design Reference Manuals.

Note 2: On H4CPlus arrays which may use both 3.3V and 5V power, the APLL I/O must be powered by the same voltage level as the array core.

All H4CPlus and M5C Series APLL's require the following six pins (see Figure 1):

- AVDD: analog power
- AVSS: analog ground
- FREF: reference frequency input pin (also used by tester to clock the core logic)
- TESTSEL: configures the APLL for tester measurements
- TESTOUT: divided-down APLL output frequency for tester
- VCOCTL: for measuring VCO control voltage and charge pump current

TESTOUT, TESTSEL and VCOCTL are dedicated test pins which must be grounded during normal system operation. An additional input pin, FREFB, is required if the reference frequency is a PECL differential clock (see Figure 2).

Each APLL also has the following five signals which interface to the array core:

- FREF_CORE: output of FREF pin input buffer; drives FREF_MUX directly, or through a PLLDELAY macro to cancel phase error due to a core divider (see Section 3.1)
- FREF_MUX: phase detector reference frequency input
- FVCO: VCO output frequency
- FVCO_DIV2: FVCO frequency divided by 2
- FFB: phase detector feedback frequency input

Referring to Figure 1 and Figure 2, for each type of APLL (CMOS-input and PECL-input), a buffer (buffer B) comparable to the FREF input buffer is included at the FFB feedback input to the phase detector in order to prevent the FREF input buffer's prop delay from adding to the phase error between the FREF pin and the clock tree. In addition, the PLLDELAY macro can be placed in the array core between the APLL's FREF_CORE output and FREF_MUX input in order to prevent a core divider's prop delay from adding to the phase error between the FREF pin and the clock tree (see Section 3.1). No external components are required for filtering of the VCO control voltage.Up to two APLL's can be used on an H4CPlus array, in the lower left and upper right corners where they are isolated from digital pwr/gnd/signal interconnects to minimize coupling of digital noise into the APLL. If only one APLL is used on an array, the APLL must reside in the lower left corner.

On M5C Series arrays, up to three APLL's can be used. If only one APLL is used it must reside in the upper left corner. If two APLL's are used, they must reside in the upper left and upper right corners. If three APLL's are used, the only restriction is that there is no APLL in the lower left corner.

As shown in Figure 3, an APLL macro covers the corner and also four adjacent I/O sites (five I/O sites if FREF is a PECL input - see Figure 4). Accordingly, the pad locations are fixed for the APLL I/O signals. The Manufacturing Rules Verification (MARV) program contained in Motorola's OACS™ system checks that the designer has made correct pin assignments for the APLL I/O. ERC also checks compliance with the APLL placement restrictions described in the previous two paragraphs.

Table 2 APLL Performance*

	H4CPlus		M5C
	3.3 V	5 V	
Output Frequency Range			
FVCO (MHz)	60 - 160	70 - 250	100 - 300
FVCO_DIV2 (MHz)	30 - 80	35 - 125	50 - 150
Output Duty Cycle			
FVCO	25% - 75%	25% - 75%	25% - 75%
FVCO_DIV2	50%	50%	50%
Loop Divider Value, N			
APxx1 macros	1 - 4	1 - 4	1 - 16
APxx2 macros	5 - 16	5 - 16	
Reference Frequency Range (MHz)			
Normal use:			
APxx1 macros	15 - 160	17.5 - 250	6.25 - 300
APxx2 macros	3.8 - 32	4.4 - 50	
On tester (N=8) all macros	7.5 - 20	8.75 - 31.2	12.5 - 37.5
Phase Error			
CMOS Singe-Ended Inputs	50ps	50ps	50ps
PECL Differential Inputs	200ps	200ps	200ps
Jitter	200ps	200ps	200ps
Max. Clock Tree Delay (Worst-Case)	25ns	20ns	20ns
Max. Lock-Acquisition Time	10µs	10µs	10µs

* All specs are preliminary.

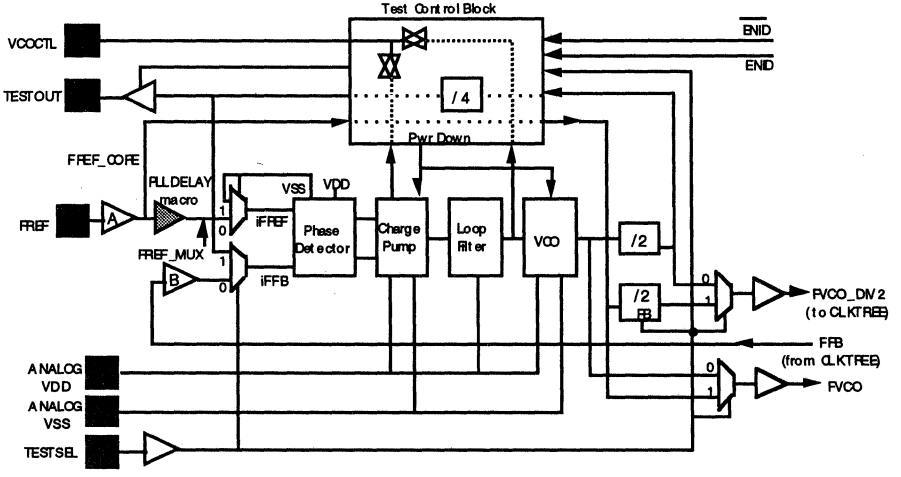

Figure 1 Analog PLL Block Diagram (CMOS Input)

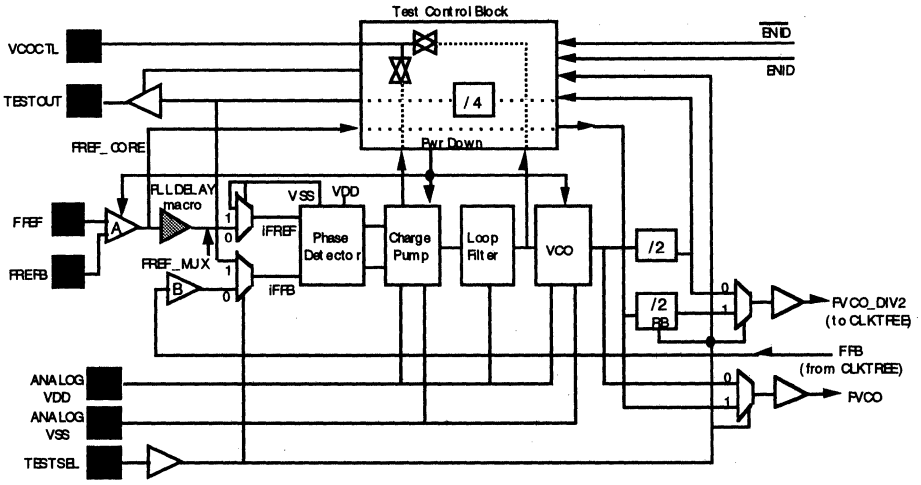

Figure 2 Analog PLL Block Diagram (PECL Input)

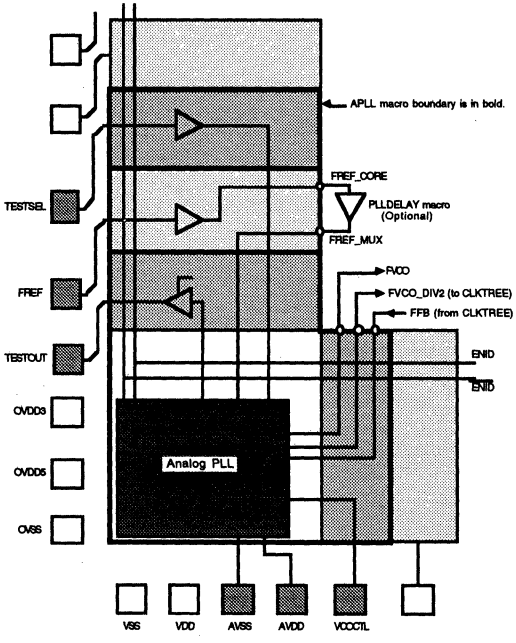

Figure 3 Analog PLL Layout (CMOS Input)

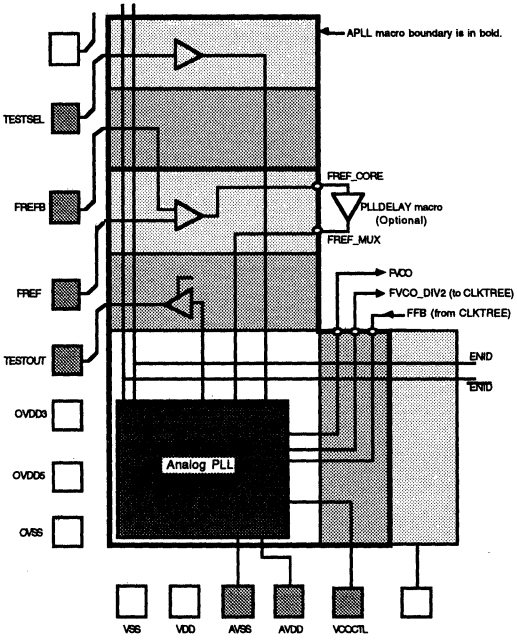

Figure 4 Analog PLL Layout (PECL Input)

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3. APLL Modelling for Simulation

3.1 Overview

Figure 5 is a generic block diagram showing clock distribution using an APLL. Either or both of the divide-by-L and divide-by-M may be used. If used, they reside in the array core. The phase detector reference frequency iFREF is actually an internal signal in the APLL. As shown in Figure 1 and Figure 2, iFREF drives directly into the phase detector and is delayed from the APLL's FREF_MUX input port by a mux prop delay. Similarly, iFFB is actually an APLL internal signal which connects directly to the phase detector and is delayed from the APLL's FFB input port by the prop delay through a buffer and a mux. These mux and buffer delays are such that when the APLL has phase-locked iFFB to iFREF, then the FREF pin will be phase-locked to the clock tree output, which is the ultimate objective. A special PLLDELAY macro can be used to cancel phase error between the clock tree and FREF which is caused by the divide-by-M. The PLLDELAY macro has the same delay as the CK->Q of a resettable flip-flop, therefore if a divide-by-M is used it should be designed using resettable flip-flops.

Note: Use of another divider in place of the PLLDELAY macro is not supported. The Motorola-internal vectors used to test the APLL in silicon require that the frequency at iFREF be the same as the frequency at the FREF pin. See Section 4 for details of the test strategy for APLL arrays.

The feedback loop between the VCO and phase detector resides in the array core, external to the APLL, and contains the clock tree and possibly a frequency divider, which will be referred to as the *core* divider. If a core divider exists it typically would follow the clock tree as does the divide-by-M. However the core divider could also precede the clock tree, as does the divide-by-L, if the clock tree is to be driven by a frequency lower than the minimum possible FVCO_DIV2 from the APLL. A third possibility is that the core divider is composed of both the divide-by-L and divide-by-M.

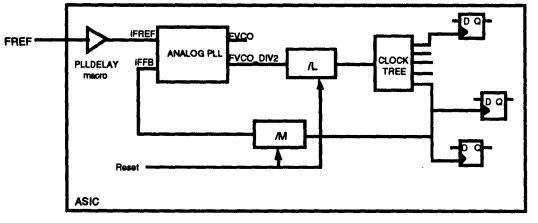

Figure 5 Clock Distribution Using an Analog PLL

In addition to generating the VCO frequency FVCO, the APLL contains a divide-by-2 to generate FVCO_DIV2, which has a 50% duty cycle. FVCO_DIV2 typically is the signal used to drive the clock tree, where FVCO is available for faster clocking of a small, localized block of logic. Therefore, throughout this document it is assumed that the clock tree is driven by FVCO_DIV2 rather than FVCO. In this case, FVCO gets divided by 2 (within the APLL itself) and then divided again by the core divider, if one exists, before arriving at the phase detector feedback input FFB. The product of these two divider values equals the *loop divider* value "N." The APLL model measures the reference frequency iFREF and the loop divider value N and generates VCO frequency required for phase-lock, FVCO = N x iFREF. The phase of FVCO_DIV2 compensates for the clock tree plus core divider delay in the core feedback loop such that the output of the clock tree is in phase with the board reference clock at the FREF pin.

In its default mode, the model acquires phase-lock approximately 20 cycles after the start of iFREF (or after reset of the core divider eliminates its 'X' state at simulation startup). However, if the user prefers, the model can also be set-up to emulate the actual time required by the APLL to achieve phase-lock in the real-world. During this "acquisition delay" the model puts out a constant (but not phase-locked) VCO frequency, which will change abruptly to the phase-locked frequency FVCO = N x iFREF after 10us has expired. Other than accurate acquisition delay, this behavior does not model the true transient response of the APLL. However, what is important is accurate modeling of the APLL's steady-state performance after phase-lock has been achieved.

The model generates FVCO and FVCO_DIV2 such that after phase-lock is achieved the clock signal fed back to the phase detector, iFFB, has the specified worst-case phase error relative to the phase detector reference clock, iFREF. The user can select this steady-state phase error to be leading, lagging, or randomly jittering between the two as described in Section 3.6. The model also does a variety of checks for such things as loss of phase-lock, the FVCO frequency required is out of range, etc.

The Verilog model emulates the APLL only during system simulations and not during option release simulations, which generate test vectors used for testing of parts. The reason is that the APLL is inactive during tester application of option release test vectors, which verify all circuitry except for the APLL. Consequently, during option release simulations the clock applied at the APLL's FREF pin will bypass the APLL and drive the core directly. For information on how to control the APLL during option release simulations, as well as information on how the APLL is verified on the tester, see Section 4, "Test Strategy for APLL Arrays."

3.2 Initialization/Reset of Dividers

When an APLL array is on a board in a system, it is unnecessary to reset the two dividers in Figure 5. However, during *system-mode simulation* these dividers must be initialized to a known state before the FREF and FVCO clocks can propagate to phase detector inputs iFREF and iFFB, respectively. Unfortunately, prior to phase-lock, FVCO and FVCO_DIV2 have no fixed timing relationship with respect to the chip's input pins. Consequently, trying to do a synchronous hardware initialization/reset of the core divider may be difficult to do without generating timing violations, such as a reset recovery time violation. A more practical approach during system-mode simulations *(but not option release simulations)* would be to use the Verilog "force" and "release" commands to initialize the states of the flip-flops in the core divider. This can be done by "forcing" the D inputs of the divider flops to known

A

states until FVCO starts, at which time these states will get clocked into the flops. When "release" occurs the flops are released to function normally. "Release" can occur at any time with respect to the arrival of clock edges at the core divider without causing the divider state to go unknown.

Alternatively, an asynchronous set/reset of the dividers can be done via chip logic or a pin at simulation start-up, *before the iFREF clock starts toggling*, since the model will not generate an FVCO clock until iFREF starts to toggle. In this way an asynchronous set or reset of all dividers can be done without generating timing violations.

Note: The reset signal for these dividers cannot be shared with any circuitry that must be reset after phase-lock is acquired, since resetting the APLL's dividers would cause the APLL to lose phase-lock.

Artificial initialization of the core dividers using "force" and "release" can be used for system-mode simulations *but not for option release simulations*, where simulation output states must match chip output states on the tester. By driving the clock tree, the divide-by-L in Figure 5 affects chip output states. Therefore *during option release simulations* the divide-by-L must be initialized/reset via chip logic or a pin, and not by using "force" and "release." The same is true of the divide-by-M if it is made observable at an output pin in order to test it. If the divide-by-M drives only FFB then it affects no output pin during option release simulations and is therefore not testable (since the APLL is inactive). In this case it need not be initialized. The divide-by-M still needs to be initialized/reset during system-mode simulations, however.

3.3 Acquisition Mode

The APLL model starts in acquisition mode at simulation start-up. It measures the frequency of the phase detector reference clock, iFREF, as well as the loop divide-by-N in order to calculate the required VCO lock frequency FVCO = iFREF x N. The model starts generating an FVCO clock which has an arbitrary phase relationship to iFREF. The resulting feedback clock at the phase detector, iFFB, has an initial phase error with respect to iFREF. The model measures this phase error and corrects the phase of FVCO such that iFFB will be in phase with iFREF, producing phase-lock.

At the start of simulation the model waits for a clock signal to appear at iFREF, and then measures the period of iFREF by keeping track of the time between successive iFREF rising edges. The model now starts generating FVCO and FVCO_DIV2, where FVCO is the center frequency of the VCO. While the VCO free-runs, the model waits until the state at iFFB is no longer 'X,' indicating that the core divider has been initialized to a known state as described previously. The model then waits until a 0->1 rising edge occurs at iFFB (as opposed to an X->1 rising edge), indicating that the core divider has been released to function normally after having been initialized/reset.

When the second iFFB rising edge occurs the model measures the frequency at iFFB and calculates the loop divider ratio 'N', where N = FVCO frequency/(iFFB frequency). If N is not within the specified range for the APLL macro used (see Section 2), the model stops the simulation after printing a message to the effect that the user must modify the loop divider circuitry such that N does lie within the specified range. If N is within the specified range but iFREF x N = FVCO is not within the specified frequency range for the VCO, the user must modify FREF and/or N such that FVCO does lie within the VCO's range. To modify N, circuitry in the array core must be changed; however, FREF can be modified interactively during Verilog simulation as described in Section 3.6. If iFREF x N = FVCO is, in fact, out of the VCO's range the model will now return to the start of the acquisition mode. Otherwise operation proceeds as follows.

Once a "legal" loop divider ratio N has been determined, the following information is printed to the screen:

- `Loop divider value, N`
- `Phase detector reference frequency, iFREF`
- `VCO frequency, FVCO`
- `VCO/2 frequency, FVCO_DIV2`
- `Duration of FVCO high and low pulses (FVCO duty cycle, effectively)`

Then a series of pulses is generated at FVCO for use in measuring the propagation delay through the feedback loop, which is equal to the sum of the clock tree propagation delay and loop divider propagation delay.

This is done in order to verify that the loop delay is not so large as to cause the APLL to go unstable and never acquire phase-lock. After generating an FVCO pulse the model waits long enough to see if the FVCO pulse causes a rising edge at iFFB. It will take anywhere from 1 to N FVCO pulses to generate a rising edge at iFFB, depending on the initial state of the loop divider. When a rising edge does occur at iFFB, the loop delay is measured as the time delay between the rising edge at iFFB and the last FVCO rising edge. If the loop delay is larger than the specified limit, the model prints a message to that effect and stops the simulation to allow the clock tree or loop divider to be re-designed. Otherwise the model will now begin its 10us acquisition delay, as described in Section 3.1. At the end of this delay, the VCO stops long enough for the clock tree to empty of all pulses generated by the free-running VCO during the acquisition delay. (If the APLL was not set-up to emulate the real-world acquisition delay, the model will skip down to this point if the feedback loop delay measured was within spec.) The APLL model now waits for the next rising edge of iFREF to start generating N cycles of the VCO lock frequency FVCO = iFREF x N. N cycles of FVCO span a complete cycle of iFREF, and the last of these N FVCO cycles should produce the next rising edge at iFFB (due to the state in which the loop divider was left after the loop delay was measured). The rising edge of the first of these N FVCO cycles is delayed from the iFREF rising edge by the "VCO_offset" such that the resultant iFFB rising edge is aligned with a subsequent iFREF rising edge (within the APLL's specified phase error), producing phase-lock. The model calculates the VCO_offset using the previously measured feedback loop delay.

If the N^{th} FVCO pulse does not produce a rising edge at iFFB, something's probably wrong with the core divider; for example, it may have been disabled or reset. In this case, the APLL will print an error message to that effect and then restart its acquisition routine to try again to acquire phase-lock. If, on the other hand, phase-lock has indeed been acquired, the fol-

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lowing information is printed to the screen:

```
- Time at which phase-lock was acquired.
- APLL steady state phase error at iFFB with
  respect to iFREF.
```

Now the APLL model goes into tracking mode.

3.4 Tracking Mode

Whenever a rising edge occurs on iFREF, the model measures the time difference between this edge and the associated rising edge on iFFB. If this "phase error" is less than the specified worst-case phase error of the APLL, then the APLL is still in lock. In this case the model will generate the next N FVCO cycles in the manner described previously in Section 3.3, in order to produce the next rising edge on iFFB. However if the phase error between iFREF and iFFB is greater than the specified worst-case phase error of the APLL, lock has been lost. In this case the model prints a "loss-of-lock" message which includes the simulation time at which lock was lost. The model waits long enough for the clock tree to empty of all 'pipelined' FVCO pulses, and then returns to acquisition mode to try to re-acquire phase-lock.

3.5 Initialization of APLL Simulation Parameters

For best accuracy, Verilog simulations involving APLL's in system mode should be done with the following timescale setting: `` `timescale 1ns/1ps ``

Therefore the timescale statement in the *asic_verilog* 'verilog.control' file should be changed to 1ps resolution, as shown above. For option-release simulations, the timescale can be left at the default value of 10ps.

In addition, there are four user-settable parameters whose range of values are hard-coded inside the APLL Verilog model because they cannot be specified in the Standard Delay Format (SDF) *verilog.timing* file output by DECAL. These parameters are:

- ***jitter*** -- determines whether iFFB will always lead, always lag, or randomly jitter between leading and lagging with respect to iFREF. The amount of lead or lag is always equal to the APLL's maximum steady-state phase error. Valid values for *jitter* are "lead", "lag" or "random". The default value is "random".
- ***use_silicon_delay*** -- determines whether the model will emulate the real-world APLL acquisition delay (described in Section 3.1). Valid values for *use_silicon_delay* are "yes" or "no". The default value is "no".
- ***vco_duty_cycle*** -- determines the duty-cycle of the FVCO output for this simulation. Valid values for *vco_duty_cycle* are "min", "typ" or "max". The default value is "min".
- ***ptv*** -- determines whether the best-, typical-, or worst-case process/temperature/voltage (PTV) value is to be used for the *maximum feedback loop delay*. Valid values for *ptv* are "bst", "typ" or "wst". The default value is "wst".

These four parameters are used only during system-mode simulations. They are not used during option release simulations, during which the FREF input clock bypasses the APLL and drives the clock tree directly. (See Section 4 for details regarding option release simulations.)

In a non-interactive simulation, the value used for *maximum feedback loop delay* is determined by one of the following Verilog command line "plus arguments": +mindelays, +typdelays or +maxdelays. Therefore if the OACS tool *asic_verilog* is used, the *maximum feedback loop delay* value will be chosen automatically according to the PTV conditions selected for the array; the *ptv* parameter is ignored. However in an interactive simulation, the *maximum feedback loop delay* value is determined by assigning the *ptv* parameter a value of "bst", "typ" or "wst". In this case the designer must set the *ptv* parameter value to match the PTV conditions chosen for the array. Otherwise the value for *maximum feedback loop delay* may be for a different PTV condition than that used for the rest of the array.

The FVCO_DIV2 output has a 50% duty cycle, but the FVCO duty cycle can vary over a wide range. Therefore in designs which make use of the APLL's FVCO output, system-mode simulations should be done at the following four sets of conditions:

i) PTV = best-case, `vco_duty_cycle = "min"`

ii) PTV = best-case, `vco_duty_cycle = "max"`

iii) PTV = worst-case, `vco_duty_cycle = "min"`

iv) PTV = worst-case, `vco_duty_cycle = "max"`

Because of the way that the APLL model generates "random" jitter, it is possible that the model will falsely swallow low-going FVCO pulses when *vco_duty_cycle* = "max", if the FVCO is operating at the upper end of its frequency range. These two conditions, coupled with random jitter, can combine to make the low-going FVCO pulses narrow enough that they get swallowed by the FVCO output buffer within the APLL model. In such cases, if FVCO is used in the design then the *jitter* parameter must be restricted to values of "lead" or "lag".

The user can assign a value to a particular parameter by putting a 'defparam' statement in the HDL stimulus file, such as:

```
defparam stim.cell1.\TC_TOP/APLL.448P_4
   .core_apll.ptv = "wst";
```

The pathname is taken from a real design named "TC_TOP." "stim" is the name of the module which applies stimulus to "TC_TOP", "cell1" is the name of the instantiation of "TC_TOP" within module "stim", "\TC_TOP/APLL.448P_4" is the instance name generated by the OACS NETLIST tool for the APLL macro used in "TC_TOP", and *core_apll* is the sub-module within the APLL Verilog model in which the *ptv, jitter, vco_duty_cycle,* and *use_silicon_delay* parameters are defined. Note that in this particular design a space is required after the APLL instance name because its first character is a backslash. Similar statements can be used to assign values to the *jitter, vco_duty_cycle* and *use_silicon_delay* parameters, for example:

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```
defparam stim.cell1.\TC_TOP/APLL.448P_4
   .core_apll.jitter = "lead";
defparam stim.cell1.\TC_TOP/APLL.448P_4
   .core apll.vco_duty_cycle="max";
defparam stim.cell1.\TC_TOP/APLL.448P_4
   .core apll.use_silicon_delay="yes";
```

Alternatively, these four parameters can be changed "on the fly" within an interactive Verilog run if the designer wishes to re-simulate without having to re-compile. If such a re-simulation is to be at a different PTV, the *ptv* parameter must be changed accordingly. The following interactive Verilog commands show how to change these parameters prior to a re-simulation (">" represents the Verilog prompt in interactive mode):

```
> $reset;
> $scope(stim.cell1.\TC_TOP/APLL.448P_4
   .core_apll);
> ptv = "wst";
> jitter = "lead";
> vco_duty_cycle = "max";
> use_silicon_delay = "yes";
> .
```

The designer may even want to change one of these three parameters prior to the first simulation after compilation. If so, a *$stop* command could be included at the start of the HDL stimulus to cause Verilog to stop at time zero and give a ">" prompt. At this time the designer can enter the same interactive Verilog commands shown above, although in this case the *$reset* command is unnecessary. Alternatively, 'defparam' statements can be put in the HDL stimulus file, as described previously.

This same method can be used to change FREF interactively if necessary. If the VCO frequency FVCO = iFREF x N is out of the APLL's range, the APLL model prints a message to the screen stating that iFREF and/or N must be changed. Referring to Figure 5, changing N

(N = L x M) requires a circuit change. However if the designer chooses to change only FREF, he can do so by scoping into his HDL stimulus module and updating the FREF period parameter.

3.6 Example Simulations of an APLL

Figure 6 shows the Verilog graphical waveforms for an interactive system mode simulation using an APLL. Also shown is a portion of the transcript window containing messages printed out by the APLL model. For this simulation, the APLL model has been set-up to not emulate the real-world acquisition delay of the APLL. Note that the TSTSEL waveform, which corresponds to the TESTSEL input on the APLL, is held low throughout the simulation. (For an option release simulation, TSTSEL = TESTSEL would be taken high after the first test cycle, and held high throughout the rest of the simulation. See Section 4.1, "Testing the Array Core".) Referring to Figure 5, at simulation start-up the APLL is configured with L = 1 and M = 2.

In this example, the divide-by-M is reset by a RESETB signal (top waveform in Figure 6) rather than by the "force" and "release" commands, which were previously described in Section 3.6. While the divide-by-M is held in reset iFFB remains low.

Initially, FVCO and FVCO_DIV2 are unknown, as is FFB prior to reset of the loop divider. The loop divider consists of a divide-by-2 flip-flop in the array core along with the flip-flop internal to the APLL which divides FVCO down to FVCO_DIV2. When RESETB goes active the loop divider state becomes known, at which time the APLL model outputs a low on both FVCO and FVCO_DIV2. Now the the loop divider's reset signal, RESETB, can return to its inactive state, since there is no longer an 'x' at the clock input to the loop divider. Since FVCO and FVCO_DIV2 will start toggling as soon as FREF starts toggling, FREF is not started until after RESETB goes inactive in order to prevent reset recovery time violations in the loop divider (discussed in Section 3.2).

The APLL model waits for the first two iFREF pulses in order to determine the frequency of iFREF and to start generating FVCO_mid and FVCO_mid/2, where FVCO_mid is the VCO center frequency. The model now waits for feedback pulses at iFFB. After the second iFFB rising edge, the model measures the iFFB frequency and calculates the loop divider value

N = FVCO_max/(iFFB frequency). N is then used to calculate the in-lock VCO frequency:

FVCO = iFREF x N. N, iFREF, FVCO, and FVCO_DIV2 are printed to the screen, as well as the high and low pulse widths of FVCO (FVCO duty cycle, effectively). At this point the model stops generating FVCO long enough for the clock tree to empty of all pulses. After this pause the model starts generating individual FVCO pulses and looking for a rising edge to result at iFFB. In this example it takes 3 FVCO pulses to cause the next rising edge on iFFB, due to the initial state of the loop divider. These three pulses are followed by N additional FVCO pulses (N happens to be four in this case) to verify that N more FVCO pulses will cause another iFFB rising edge at the expected time. At this point the model starts generating the in-lock frequency FVC0 = N x iFREF, with the proper phase such that the next rising edge of iFFB will be phase-locked to iFREF.

Figure 7 shows Verilog graphical waveforms and part of the transcript window for a non-interactive system mode simulation in which the APLL model has been set-up to emulate the real-world acquisition delay of the APLL. (Section 3.5 explains how to do this.) For this example simulation, the acquisition delay was shortened in order to fit the waveforms on the page. At the end of the acquisition delay the model stops generating the VCO center frequency at FVCO and waits long enough for the clock tree to empty of all pulses. After this pause the model starts generating the in-lock frequency FVC0 = N x iFREF, with the proper phase such that the next rising edge of iFFB will be phase-locked to iFREF.

Figure 8 shows Verilog graphical waveforms and part of the transcript window for the start of an option release simulation using an APLL. Note that the TSTSEL waveform, which corresponds to the TESTSEL input on the APLL, is taken high after the first test cycle and held high throughout the rest of the simulation. The FREF clock is low at simulation start-up, and stays low until after TESTSEL goes high. Similarly RESETB, which resets the loop divider, is inactive (high) until after TESTSEL goes high.

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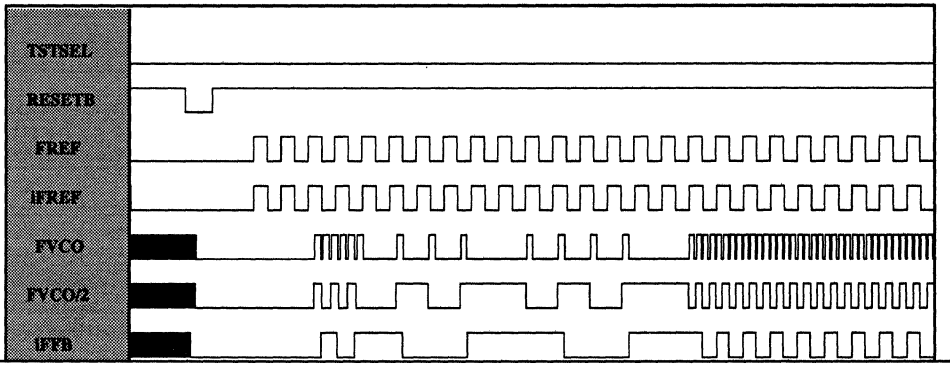


```
################################################################################
################################################################################
###                                                                          ###
###  Parameter 'ptv' has been given a value of "wst" for APLL instance       ###
###       stim.cell1.APLLOACS22/APLL.27P_1.core_apll                         ###
###  Worst-case timing must also be used for the rest of the design.         ###
###                                                                          ###
################################################################################
################################################################################

Assigned values for user-settable parameters for APLL instance
     (stim.cell1.APLLOACS22/APLL.27P_1.core_apll):
   vco_duty_cycle = "max"
   jitter = "lag"
   use_silicon_delay = "no"

################################################################################
################################################################################

   To backannotate timing before simulation -
   type one of the following :

    (If more than one is activated, last choice
    overrides the rest.)

    Type "ba_timing_wcs;" for worst case timing
    Type "ba_timing_typ;" for typical case timing
    Type "ba_timing_bcs;" for best case timing


   Else, type "." (period) to simulate with
   unit timing.
L84 "aplloacs22/design_data/verilog.control": $stop at simulation time 0.00 ns
Type ? for help
C1 > ba_timing_wcs;
C2 > .

    Back-annotating worst case timing ..................
                .
                .
                .
Operating environment for APLL instance
        (stim.cell1.APLLOACS22/APLL.27P_1.core_apll.acquire):
   N = 4 (Loop divider value)
   iFREF  = 50 MHz (Phase detector reference frequency)
   FVCO   = 200 MHz (VCO frequency)
   FVCO_DIV2 = 100 MHz (VCO/2 frequency)
   VCO_high = 3.75 ns (VCO high pulse width)
   VCO_low  = 1.25 ns (VCO low pulse width)

APLL instance (stim.cell1.APLLOACS22/APLL.27P_1.core_apll.track)
    ACQUIRED PHASE-LOCK at time 447.46 with phase error = 0.25 ns

L97 "/home/cdc1/aplltc/tc_top/sub_blocks/aplloacs22/vectors/stimulus/hdl.stim":
$stop at simulation time 590.00 ns
C2 >
```

Figure 6 Example Verilog System-Mode Simulation of an APLL (acquisition delay excluded)

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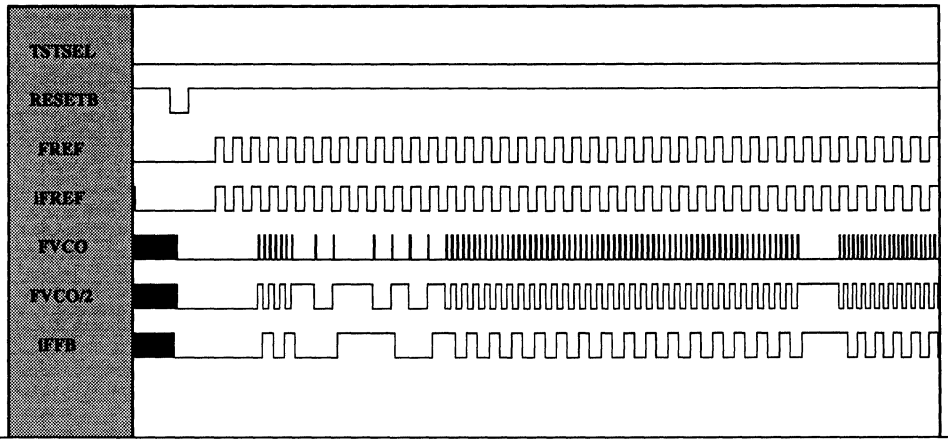
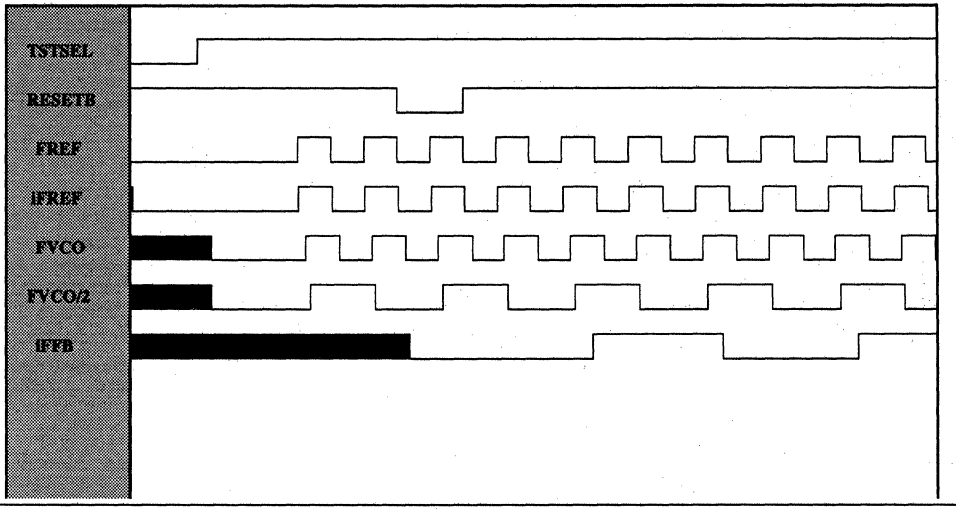



```
################################################################################
################################################################################

Assigned values for user-settable parameters for APLL instance
     (stim.cell1.APLLOACS22/APLL.27P_1.core_apll):
   vco_duty_cycle = "min"
   jitter = "lead"
   use_silicon_delay = "yes"

################################################################################
################################################################################

    Back-annotating worst case timing ..................


   *** SDF Annotator version 1.0.10
   ***     SDF file:  aplloacs22/timing/veritool.timing
   ***     Back-annotation scope:  stim
   ***     Configuration file:  /home/bass1/oacs2.x/oacs_apll_tools2.0/sdf.config
   ***     SDF Annotator log file:  aplloacs22/timing/reports/sdf.log
   ***     MTM selection parameter specified: MAXIMUM

   ***     SCALE FACTORS parameter specified: 1.000000:1.000000:1.000000

   ***     SCALE TYPE parameter specified: FROM_MTM

           Parsing configuration file...

           Configuring for back-annotation...

           Reading SDF file and back-annotating timing data...

   *** SDF back-annotation successfully completed

Operating environment for APLL instance
       (stim.cell1.APLLOACS22/APLL.27P_1.core_apll.acquire):
   N = 4 (Loop divider value)
   iFREF  = 50 MHz (Phase detector reference frequency)
   FVCO   = 200 MHz (VCO frequency)
   FVCO_DIV2 = 100 MHz (VCO/2 frequency)
   VCO_high = 1.25 ns (VCO high pulse width)
   VCO_low  = 3.75 ns (VCO low pulse width)

APLL instance (stim.cell1.APLLOACS22/APLL.27P_1.core_apll.track)
    ACQUIRED PHASE-LOCK at time 824.46 with phase error = -0.25 ns

L128 "/home/cdc1/aplltc/tc_top/sub_blocks/aplloacs22/vectors/stimulus/hdl.stim":
 $stop at simulation time 900.00 ns
Type ? for help
C1 >
```

Figure 7 Example Verilog System-Mode Simulation of an APLL (acquisition delay included)

A




```
################################################################################
################################################################################

Assigned values for user-settable parameters for APLL instance
     (stim.cell1.APLLOACS22/APLL.27P_1.core_apll):
   vco_duty_cycle = "min"
   jitter = "random"
   use_silicon_delay = "no"

################################################################################
################################################################################


    Back-annotating worst case timing ..................


   *** SDF Annotator version 1.0.10
   ***     SDF file:  aplloacs22/timing/veritool.timing
   ***     Back-annotation scope:  stim
   ***     Configuration file:  /home/bass1/oacs2.x/oacs_apll_tools2.0/sdf.config
   ***     SDF Annotator log file:  aplloacs22/timing/reports/sdf.log
   ***     MTM selection parameter specified: MAXIMUM

   ***     SCALE FACTORS parameter specified: 1.000000:1.000000:1.000000

   ***     SCALE TYPE parameter specified: FROM_MTM

           Parsing configuration file...

           Configuring for back-annotation...

           Reading SDF file and back-annotating timing data...


   *** SDF back-annotation successfully completed

TESTSEL pin went high at time              24.30 ns
     for APLL instance ( stim.cell1.APLLOACS22/APLL.27P_1.core_apll )
     FREF will now bypass the APLL and appear at the FVCO output.
     (If APLL output ports FVCO_DIV2 and FVCO stay 'x', then
     TESTSEL was not held low long enough, unless port FREF_CORE is also 'x').

L96 "/home/cdc1/aplltc/tc_top/sub_blocks/aplloacs22/vectors/stimulus/hdl.stim":
$stop at simulation time 250.00 ns
Type ? for help
C1 >
```

Figure 8 Example Verilog Option Release Simulation of an APLL

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4. Test Strategy for APLL Arrays

4.1 Testing the Array Core

On the tester, customer "option release" test vectors are used to test all of the array except the APLL, which is powered down during this time. Consequently the APLL is not used to clock the array core. The ASIC designer must use an external test clock to generate test vectors for option release, as is done for any non-APLL design. This external test clock is applied at the FREF pin.

At simulation start-up TESTSEL must be low, and must stay low for at least one test cycle, in order to initialize some flip-flops inside the APLL. During this time the model must output an 'x' on APLL outputs FVCO and FVCO_DIV2, since the VCO will be oscillating freely in silicon. To ensure that FVCO and FVCO_DIV2 remain 'x' while TESTSEL is low, the following two conditions must be met:

1. FREF should be low at simulation start-up, and should remain low at least until TESTSEL goes high.
2. If there is a reset signal for the loop divider, this reset must be inactive at simulation start-up, and must remain inactive at least until TESTSEL goes high. This condition is required because as soon as a known logic state appears at iFFB, the model outputs a known (low) state at FVCO and FVCO_DIV2 to facilitate reset of the loop divider during system simulations.

After TESTSEL goes high the APLL will be powered down, and the reference clock at the FREF pin will bypass the APLL and come out at the APLL's FVCO port (see Figure 1 and Figure 2). Similarly, FREF/2 comes out on the APLL's FVCO_DIV2 port. **Once TESTSEL goes high it must stay high throughout the rest of the option release simulation.**

4.2 Testing the APLL

The APLL is tested at Motorola by a canned test routine, during which the rest of the array does not toggle. This procedure is used to eliminate coupling of digital switching noise into the APLL through AVDD and AVSS, which are tied to the core VDD and VSS on the tester in order to eliminate the need for special test hardware for APLL arrays. In a customer's system, of course, AVDD and AVSS provide isolated power and ground for the APLL.

The APLL contains a divide-by-4 which is driven by VCO/2 in order to produce a frequency at the TESTOUT pin which is slow enough to be measured on a production tester. As shown in Table A.1 in the Appendix, the following tests are performed on the tester while in APLL test mode (TSTQ1 = 1):

i) Allow the APLL to lock at its center frequency and measure the VCO/8 frequency at the TESTOUT pin, with the VCOCTL pin turned off.

ii) Allow the APLL to lock at its center frequency and measure the VCO/8 frequency at the TESTOUT pin, and the VCO control voltage at the VCOCTL pin.

iii) Allow the APLL to lock at its center frequency and measure the VCO/8 frequency at the TESTOUT pin, and the charge pump current at the VCOCTL pin.

iv) Measure the dynamic IDD of the APLL. (A CMOS input APLL still will be in phase-lock from the previous step. For a PECL input APLL, the PECL input will be turned off by ENID ("Enable IDD" pin, see OACS User/Reference Guide); therefore the dynamic IDD measurement will be made while the APLL is not phase-locked but is free running at the minimum possible VCO frequency, since the phase detector reference frequency input, iFREF, will not be toggling).

On the tester, frequency measurement is effectively done by locating an edge on TESTOUT and then examining several more cycles to see that subsequent edges occur within the expected window. CMOS-input APLL's will remain phase-locked when moving from test (i) to test (ii), and from test (ii) to test (iii), etc. However PECL-input APLL's will lose lock when moving from one test to another. As shown in Table A.1, toggling the ENID pin is what causes the transition from one test to the next. However taking ENID high also powers-down the PECL input buffer, at which time a PECL-input APLL will lose phase-lock. Therefore after ENID is taken back low to begin the next test, a PECL-input APLL must be given time to re-acquire phase-lock before measurements are taken.

Tests i-iv are repeated at the APLL minimum and maximum *operating* frequencies, which are the most extreme frequencies achievable within the linear range of the VCO transfer function. These frequency limits are given in Section 2.

The VCOCTL pin is used to measure the VCO control voltage and charge pump current. These measurements can be related to the stability and bandwidth of the APLL. This pin should be tied to analog VSS in the customer's system to prevent noise from being injected onto the VCO control voltage during normal system operation.

During static IDD testing of the chip as a whole, which occurs during tester application of option release vectors, APLL bias currents are turned off under control of the ENID pin.

The canned APLL vector set, which performs tests (i)-(iv) above, toggles the ENID pin, which has no simulation model. Therefore, the customer cannot simulate these canned vectors.

Appendix A: APLL Internal Test Circuitry

Figure A.1 and Figure A.2 are more detailed versions of Figure 1 and Figure 2, respectively, showing the test control circuitry built into the APLL. Table A.1 shows how the TESTSEL and ENID signals are used to control this circuitry in order to move the APLL into each of its operating modes. The top portion of Table A.1 shows how the Motorola-internal APLL test program performs the tests described in Section 4.2.

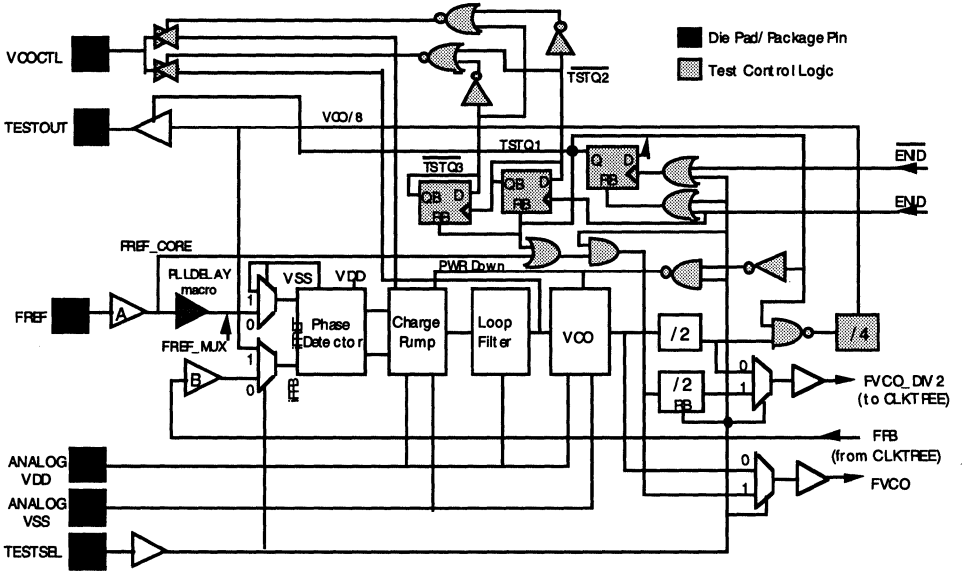

Figure A.1 Analog PLL Schematic and Test Logic (CMOS Input)

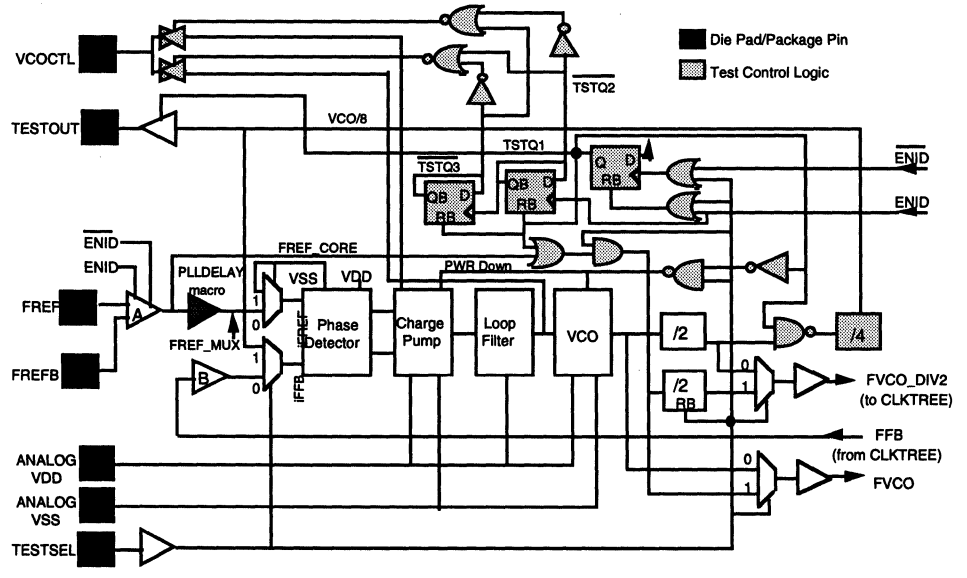

Figure A.2 Analog PLL Schematic and Test Logic (PECL Input)

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Table A.1 APLL Simulation and Test Mode Sequence

Test	Inputs		APLL Internal Nodes			Simulation and Test Modes
	TESTSEL	ENID	TSTQ1	TSTQ2	TSTQ3	
APLL Test Provided at Motorola (Not User Defined)	0	0	0	0	0	**Reset test flops.**
	0	**1**	0	0	0	(Set-up Test)
	1	1	**1**	0	0	(Set-up Test)
	1	**0**	1	0	0	**Measure frequency; VCOCTL pin 3-state.**
	1	0	1	0	0	(Running Test)
	1	**1**	1	**1**	0	(Set-up Next Test)
	1	**0**	1	1	0	**Measure frequency & VCO control voltage.**
	1	0	1	1	0	(Running Test)
	1	**1**	1	**0**	**1**	(Set-up Next Test)
	1	**0**	1	0	1	**Measure frequency & charge pump current.**
	1	0	1	0	1	(Running Test)
	1	**1**	1	**1**	1	**Measure dynamic IDD of APLL.**
	1	1	1	1	1	(Running Test)
Core Test (User Defined)	**0**	**0**	**0**	**0**	**0**	**Reset test flops.**
	1	0	0	0	0	**Start functional testing of array core with APLL inactive.**
	1	0	0	0	0	(Running Test)
	1	**1**	0	0	0	**IDD vector (at Motorola only)**
	1	**0**	0	0	0	(Running Test)
	1	0	0	0	0	(Running Test)
	0	0	0	0	0	**Customer board simulation with APLL active.**

* User can only simulate states in which ENID is low/inactive.

Appendix B: Transfer Functions

The APLL is a classical second order control system. Its transfer functions are:

Phase Detector Transfer Function:
$K_p = I_p/2\pi$
where I_p is the charge pump current.

Filter Transfer Function:
$K_f = R + 1/sC$
where R is the loop resistor and C is the loop capacitor.

VCO Transfer Function:
$K_o = K_v/s$
where K_v is the gain of the VCO in the linear region.

Open Loop Transfer Function:
$G(s) = K_p(K_f)(K_o)/N$
where N is the value of the divider in the feedback path.

Closed Loop Transfer Function:
$H(s) = G(s)/(1 + G(s))$
$H(s) = 2\zeta\omega_n s + \omega_n^2/(s^2 + 2\zeta\omega_n s + \omega_n^2)$
where $\omega_n = (K_v I_p/2\pi CN)^{1/2}$

Damping factor = $\zeta = RC\omega_n/2$

Typical values for the loop parameters are given in Table B.1.

Table B.1 Typical Loop Parameter Values

Parameter		3.3 V	5 V
I_p (µA)		70	100
K_o (MHz/V)		150	200
R (Ohm)	N = 1-4	2100	1400
	N = 5-16	4200	2500
C (pF)		50	50

From these typical values and the closed loop transfer function, the user can determine the characteristics of the loop and generate Bode Plots, if desired.

Appendix C: VCO Frequency vs. Voltage

Select a VCO frequency in the middle of the linear region of Figure C.1 to optimize damping.

Example: Using a 5V APLL, if the desired clock tree frequency (CLK) is 50 MHz (see Figure 5) and FREF is 25 MHz, select "/M" = 2 and "/L" = 2. This gives CLK = 50 MHz, VCO_DIV2 = 100 MHz and VCO = 200 MHz which is in linear region of Figure C.1.

Table C.1 Minimum Operating Frequency

Divide Factor, N	3.3 V			5 V		
	Filter Resister, R	Damping, ζ	F_{pdmin} (MHz)	Filter Resister, R	Damping, ζ	F_{pdmin} (MHz)
1	2100	0.76	66	1400	0.70	84
2	2100	0.54	33	1400	0.49	42
3	2100	0.44	22	1400	0.40	28
4	2100	0.38	17	1400	0.35	21
5	4200	0.68	26	2800	0.63	34
6	4200	0.62	22	2800	0.57	28
7	4200	0.58	19	2800	0.53	24
8	4200	0.54	17	2800	0.49	21
9	4200	0.51	15	2800	0.47	19
10	4200	0.48	13	2800	0.44	17
11	4200	0.46	12	2800	0.42	15
12	4200	0.44	11	2800	0.40	14
13	4200	0.42	10	2800	0.39	13
14	4200	0.41	9	2800	0.37	12
15	4200	0.39	9	2800	0.36	11
16	4200	0.38	8	2800	0.35	11
Notes:	Ip=0.07mA, C=50 pF, VCO gain =1.5x10^8 MHz/V			Ip=0.1mA, C=50 pF, VCO gain =2x10^8 MHz/V		

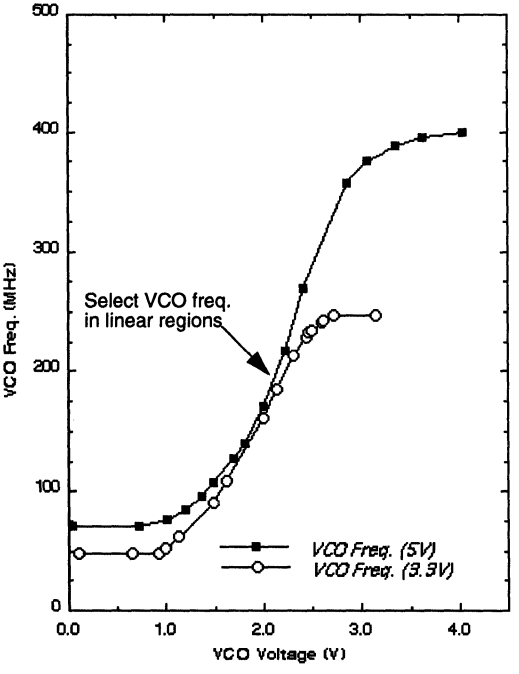

Figure C.1 VCO Frequency vs. Voltage

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Appendix D: PLL Basics

(From application note "ASIC Distribution Using a Phase-Locked-Loop (PLL)", AN1509)

D.1 INTRODUCTION

Transferring data between ASIC chips at frequencies above 40 MHz requires special on-chip circuitry in current sub-micron technologies. Phase locked loops can provide skew management in ASIC devices to help compensate for clock tree insertion delays and process, temperature and voltage variations allowing maximum multi-chip system performance.

This application note is written to help designers of multi-chip ASIC systems maximize system performance by managing clock distribution and optimizing clock skew and data path relationships. It contains equations relating measurable timing and skew parameters to maximum frequencies of operation. It explains techniques available to minimize critical parameters which contribute to clock skew.

D.2 BACKGROUND

D.2.1 REGISTER-TO-REGISTER DATA TRANSFER BETWEEN ASIC CHIPS

When determining the maximum frequency at which data can be transferred from one ASIC device to another, a designer must carefully consider both the delay of the data path and the skew of the clock. The data path is the delay from a register in the sending ASIC (including clock to Q) to the D input of a register in the receiving ASIC (including the setup and hold times), see Figure D.1. The clock skew or Tskew is the difference between a rising edge on ClkA in ASIC1 and ClkB in ASIC2.

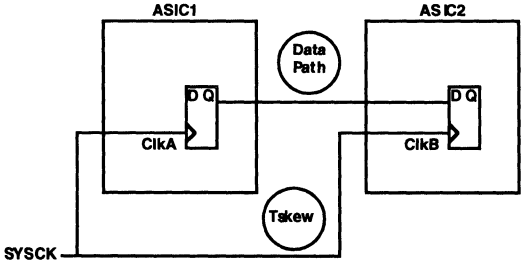

Figure D.1 Chip-to-Chip Timing Parameters

Tskew in this document refers to clock skew in both the positive and negative directions. Positive skew is when the rising edge of ClkB occurs later than a rising edge of ClkA. Positive skew affects data transfer from a hold time standpoint. Negative skew is when the rising edge of ClkB occurs earlier than a rising edge on ClkA. Negative skew affects data transfer from a setup time standpoint. A complete analysis of clock skew is performed in Appendix E.

D.2.2 SETUP AND HOLD TIME CONSIDERATIONS

To insure error-free data transitions between ASIC1 and ASIC2, the data path from the sending flip- flop in ASIC1 to the receiving flip flop in ASIC2 must not be so long that a set-up time violation is realized on the receiving flop- flop. The same data path must also be long enough to avoid a hold-time violation on the receiving flip-flop. This setup and hold time relationship must take into consideration clock skew between the rising edge of ClkA, which initiates the data transfer and the rising edge of ClkB which clocks in the transferred data.

D.2.3 INSERTION DELAY AND THE EFFECT OF THE CLOCK TREE

Insertion delay is defined as the delay from the rising edge of the external system clock to the rising edge of the clock on any given flip- flop on the ASIC. In Figure D.2, it's the delay from SYSCK to ClkA or ClkB. Insertion delay is made up of the clock input buffer and clock tree delays. The insertion delay in one ASIC can be very different from the insertion delay in another ASIC, depending on the size of the ASIC and the number of elements that must be clocked by the clock tree. Differences in insertion delays between ASIC devices directly contribute to clock skew (Tskew). In the example circuit (Figure D.2), if ASIC1 has an insertion delay of 5 ns and ASIC2 an insertion delay of 10 ns, then a rising edge in ASIC 1 will be skewed by at least 5 ns from a rising edge in ASIC 2.

D.2.4 PTV VARIATIONS

Process, Temperature and Voltage (PTV) variations can increase the difference in insertion delays. Most ASIC technologies use a multiplier to adjust delays due to PTV. In the H4C technology, a worst-case multiplier (WCM) and a best-case multiplier (BCM) are used. The WCM modifies a typical delay to represent worst-case conditions. The WCM is greater than one. The BCM is less than one and modifies a typical delay to represent a best-case condition. The "process spread" is the difference between a best-case delay and a worst-case delay for a given data path. The process spread can be found by dividing the WCM by the BCM (WCM/BCM). Choosing a technology with a minimum process spread will allow higher overall performance.

D.2.5 MAXIMUM FREQUENCY OF OPERATION

An equation can be derived that relates setup and hold times, insertion delay and process spread to determine the maximum frequency at which data can be safely transferred from chip-to-chip. A full derivation of this equation is provided in Appendix E. The equation in terms of the minimum period is,

$$MinPer = Tskew\ (WCM/BCM + 1) + WCM\ (Tsu + Th + TDm) \quad (D.1)$$

where,

MinPer Minimum clock period in ns (1/max frequency of operation).

Tskew Total skew (positive and/or negative) between

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rising edges of ClkA and ClkB (see Figure D.2).

WCM Worst Case Multiplier.

BCM Best Case Multiplier.

Tsu Setup delay of flip flop in receiving ASIC (ASIC2 in Figure D.2).

Th Hold delay of flip flop in receiving ASIC (ASIC2 in Figure D.2).

TDm Data path delay margin

Two things become apparent in looking at Equation (D.1). First, Tskew is the dominant parameter affecting the maximum frequency at which data can be transferred between ASIC devices. Secondly, the process spread for the chosen technology is also very important. Clearly, Tskew and the process spread must be minimized to allow maximum performance.

To address the problem of clock skew, a Phase Locked Loop (PLL) can be added to each ASIC device to reduce the effects of insertion delay differences and help manage the skew from chip-to-chip. The PLL will synchronize the rising edge on SYSCK such that it will be simultaneous with a rising edge on flop ck, see Figure D.3. If the PLL is used on each ASIC device, all flop ck signals on every ASIC will be simultaneous within the error of the PLL. The PLL will compensate for differences in insertion delays from ASIC-to-ASIC as well as PTV variations.

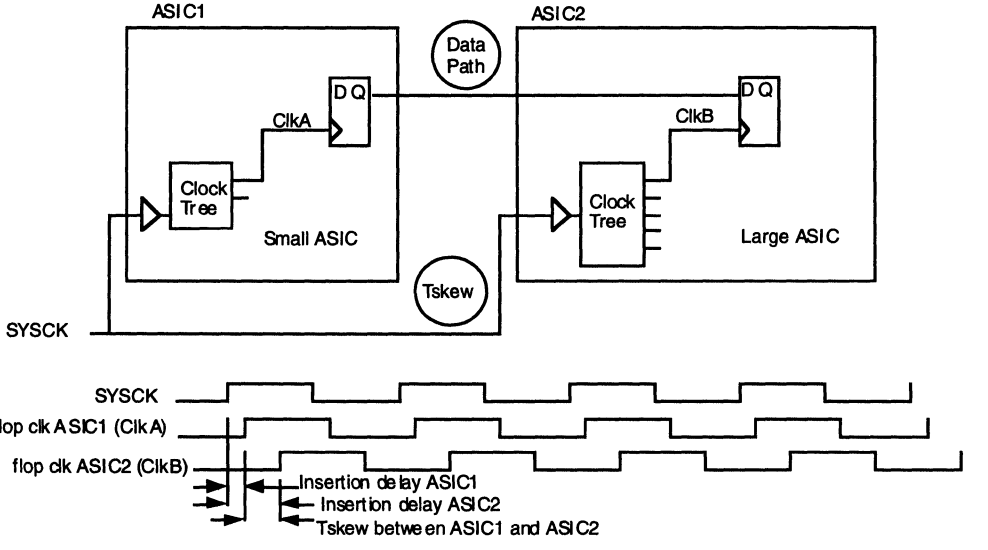

Figure D.2 Effect of Clock Tree on T_{skew}

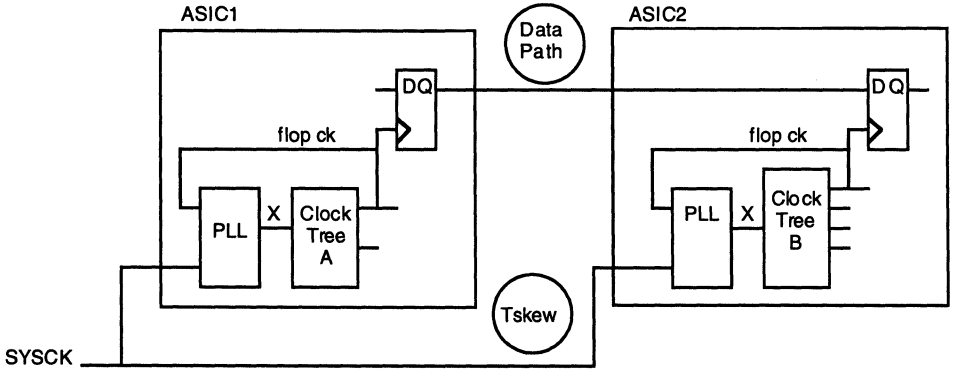

Figure D.3 PLL Solution

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Appendix E: Derivation of Minimum Period Equation

(From application note "ASIC Distribution Using a Phase-Locked-Loop (PLL)", AN1509)

This section contains a derivation of the equation that relates clock skew, process spread, and flip-flop specifications to determine the minimum period or maximum frequency at which data can be transferred between ASIC devices. Figure E.1 illustrates the data and clock paths between two ASIC's. If data is to be transferred reliably from ASIC1 to ASIC2, the set up and hold time requirements of the receiving flip flop in ASIC2 must be satisfied in the presence of clock skew and process spread. First, we will analyze the setup and hold time requirements of the receiving flip flop. This is similar to the classic shift register problem where clock skew can cause setup or hold problems on the receiving flip flop.

The data delay path from ASIC1 to ASIC2 includes 1) the delay from a rising edge of ClkA to the output of ASIC1 - TDout, 2) the delay of the PC board trace - TDbrd and 3) the delay of the input path of ASIC2 - TDin. The setup and hold time parameters of the receiving flip flop Tsu and Th must also be considered. The total data path delay is,

$$TD = TDout + TDbrd + TDin \qquad (E.1)$$

When considering the setup time requirements of ASIC2, the worst case path from ASIC1 to ASIC2 must be considered. The minimum period at which data can be safely transferred in the presence of clock skew without violating the setup requirements of the receiving flip flop is,

$$MinPer = WCM(TD + Tsu) + Tskew \qquad (E.2)$$

Note that typical delay values are used in these equations. These values are modified for best case and worst case by the multipliers BCM and WCM respectively. Additionally, the worst- case path assumes the edge direction, rising or falling that results in the longest delay.

Figure E.2 illustrates the setup time requirement. The dashed lines on ClkB represent clock skew.

When considering the hold- time requirements of ASIC2, the best-case path must be considered. The best-case path assumes the edge direction, rising or falling that results in the shortest delay. The equation relating the data path, hold time and Tskew is,

$$BCM(TD) \geq Tskew + BCM(Th) \qquad (E.3)$$

We now have two equations relating the data path. To find the minimum period, first consider the ideal case, then generalize it. Ideally, assume the data path delay TD is just long enough to prevent a hold-time violation, or the best-case datadelay is equal to the hold time plus the clock skew,

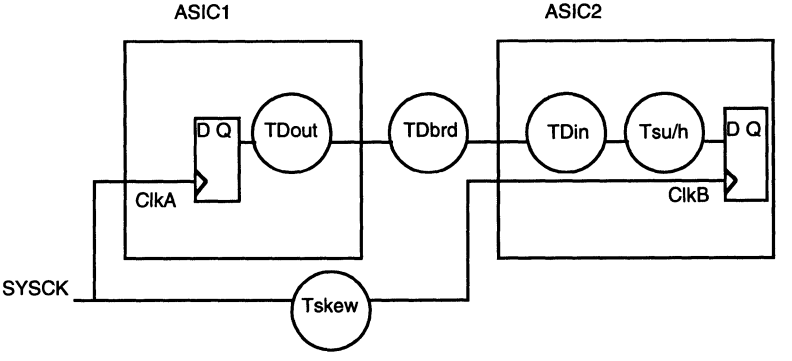

Figure E.1 Chip-to-Chip Data Transfers

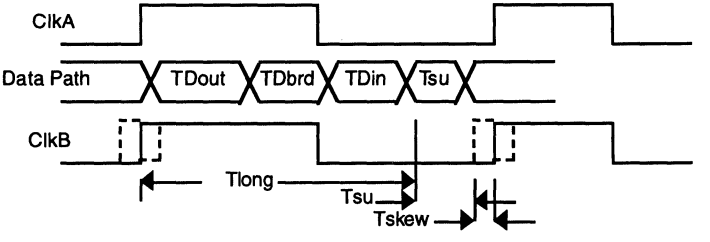

Figure E.2 Clock Skew and Setup Time Requirements

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$$BCM(TD) = Tskew + BCM(Th) \quad (E.4)$$

If true, we could solve this equation for TD and put that value into the setup time equation,

$$TD = (Tskew+BCM(Th))/BCM \quad (E.5)$$

$$MinPer = WCM(((Tskew+BCM(Th))/BCM) + Tsu) + Tskew \quad (E.6)$$

Notice that Tskew appears twice in this equation. Skew in the positive direction affects hold time and skew in the negative direction affects the setup time. Generally, we don't know if the clock skew is in the positive or negative direction so we consider it twice.

Figure E.4 illustrates this equation. The minimum period is found by taking the best-case data path delay that is just long enough to prevent a hold-time violation in the presence of clock skew, BCM(TD), multiply that delay by the worst-case multiplier WCM(TD), and add to that the worst-case set-up time and the clock skew.

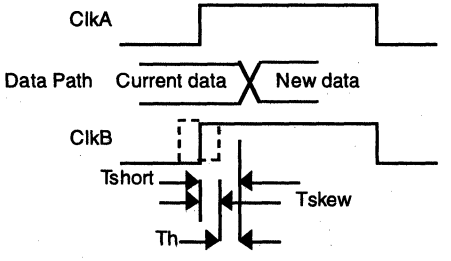

Figure E.3 Clock Skew and Hold Time Requirements

Equation (E.5) can be reduced to become very close to our final equation,

$$MinPer = WCM (Tskew/BCM + Th + Tsu) + Tskew$$

$$MinPer = WCM/BCM (Tskew) + WCM(Th + Tsu) + Tskew$$

combining the Tskew terms,

$$MinPer = Tskew (WCM/BCM+1) + WCM (Tsu+Th) \quad (E.7)$$

It is unrealistic to assume all data paths can be tuned to be just long enough to prevent a hold-time violation. We should therefore introduce some margin in the data path. Generally, this margin would be defined by the shortest chip-to-chip data path delay on one end of the spectrum and the longest chip-to-chip data path delay on the other end. This assumes, of course, that these paths are long enough or short enough to prevent hold time or setup time violations respectively. When designing shift registers from discrete components, it is common to add delay to the data path to insure there is not a hold time violation in the presence of clock skew. If the maximum frequency of a system is limited by the data path delay from chip-to-chip (see Equation (E.2)) it may be necessary to add delay to shorter data paths to prevent hold times. There should always be a 1-2 ns margin (typical delays) between the shortest data path and the longest data path to allow room for variation in delay as the paths are tuned to prevent violations. If this margin TDm is added, a new equation and timing diagram result. From Equation (E.5) we add the margin TDm to the typical data delay TD,

$$TD = ((Tskew+BCM(Th))/BCM) + TDm \quad (E.8)$$

The minimum period is,

$$MinPer=WCM((((Tskew+BCM(Th))/BCM)+TDm)+Tsu) +Tskew$$

$$MinPer = WCM(Tskew/BCM + Th +TDm + Tsu) + Tskew$$

$$MinPer=WCM/BCM(Tskew)+WCM(Th+TDm)+Tsu) +Tskew$$

$$MinPer=Tskew(WCM/BCM+1)+WCM(Tsu+Th+TDm) \quad (E.9)$$

Note that if the period of operation is larger than the minimum defined above, the data path margin TDm will be larger and there will be more room for data path tuning.

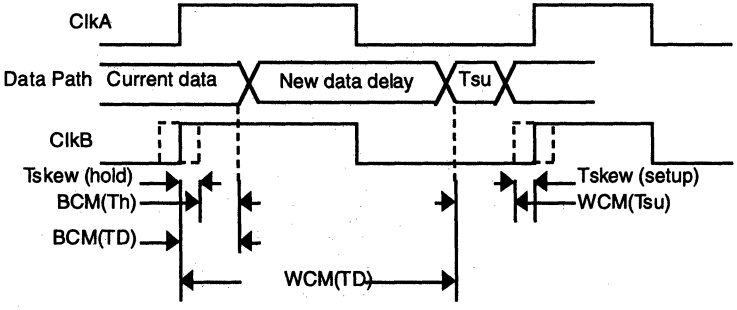

Figure E.4 Ideal Minimum Period Considering Setup and Hold Time

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