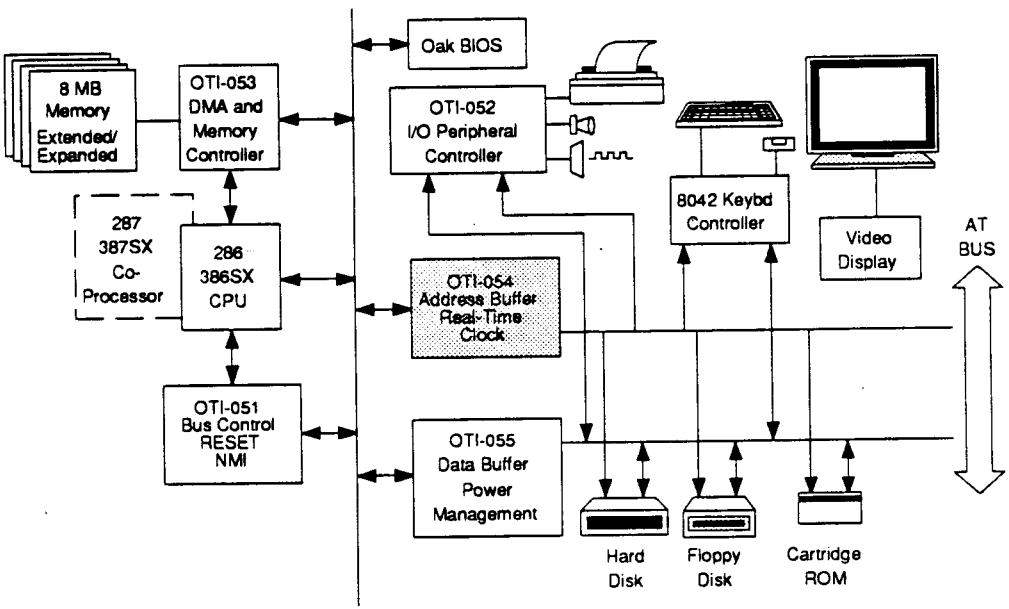
1.0 INTRODUCTION TO OTI-054 ADDRESS BUFFER and REAL TIME CLOCK

OTI-054 contains the address buffer drivers for IBM AT or Model 30 - 286 compatible systems and replaces all the TTL address and command drivers that are normally required on the system board. In addition to the Address drivers, OTI-054 also includes a Real Time Clock. The Real Time Clock is compatible to MC146818 with the following exceptions:

- 128 Bytes of CMOS RAM total
- no CKFS (clock select input)
- no SQW (square wave output)

System Block Diagram



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2.0 PIN-OUT ASSIGNMENT

Table 1. OTI-054 Pin Description

SYMBOL	PIN #	TYPE	NAME and FUNCTION
SA1-SA19 SA21-SA23	3-6,8-14,18-21, 23-26,28-30	I/O	ADDRESS LINE (1-19,21-23): are the CPU address lines (unlatched).
A0	2	I/O	ADDRESS LINE 0: address line 0 from OTI-051.
A20	27	I/O	ADDRESS LINE 20: address line 20 from OTI-051 gated by 8042 output and port 92(Hex) output.
BHE-	1	I/O	BYTE HIGH ENABLE: is an active low signal from OTI-051 and is used to enable data onto the most significant half of the data bus.
PCBHE-	100	I/O	I/O CHANNEL BYTE HIGH ENABLE: is an active low signal on the I/O channel. It is a latched version of BHE-. When MASTER- is low, it becomes an input to form BHE-.
ALE	16	I	ADDRESS LATCH ENABLE: is an active high pulse signal during the beginning of either the CPU or DMA cycle. A(1-23) will be latched internally using the ALE falling edge.
PCA(0-16)	99,98,96-92,90, 88,86-84,82-78	I/O	PC BUS ADDRESS (0-16): are the latched address version of SA(0-16). When ALE is high, PCA(0-16) are the transparent signals of A0 and SA(1- 16). PCA(0-16) are latched at the falling edge of ALE and stay latched until ALE is high again.
PCA(17-19)	77-75	O	PC BUS ADDRESS (17-19): are the latched address version of SA(17- 19). When ALE is high, PCA(17-19) are the transparent signals of (17-19). PCA(17-19) are latched at the falling edge of ALE and stay latched until ALE is high again.
LA(17-23)	38-36,34-31	I/O	UNLATCHED ADDRESS (17-23): are the unlatched address version of SA(17- 23) in the synchronous mode when BUSCLK = CPUCLK/2. When BUSCLK = CPUCLK/4 or when the asynchronous mode is selected, LA17-23 are latched at the falling edge of ALE.
XD7 - XD0	60,59,57-52	I/O	XDATA BUS: bi-directional data lines to/from the CPU or I/O channel bus.
IORD-	73	I/O	I/O READ COMMAND: active low command to instruct the I/O device to drive its data onto the data bus.
IOWR-	72	I/O	I/O WRITE COMMAND: active low command to instruct the I/O device to read the data present on the data bus.
MEMRD-	71	I/O	MEMORY READ COMMAND: active low signal to instruct the memory subsystem to drive its data onto the data bus.
MEMWR-	70	I/O	MEMORY WRITE COMMAND: active low signal to instruct the memory subsystem to store the data present on the data bus.

Table 1. OTI-054 Pin Description (Continued)

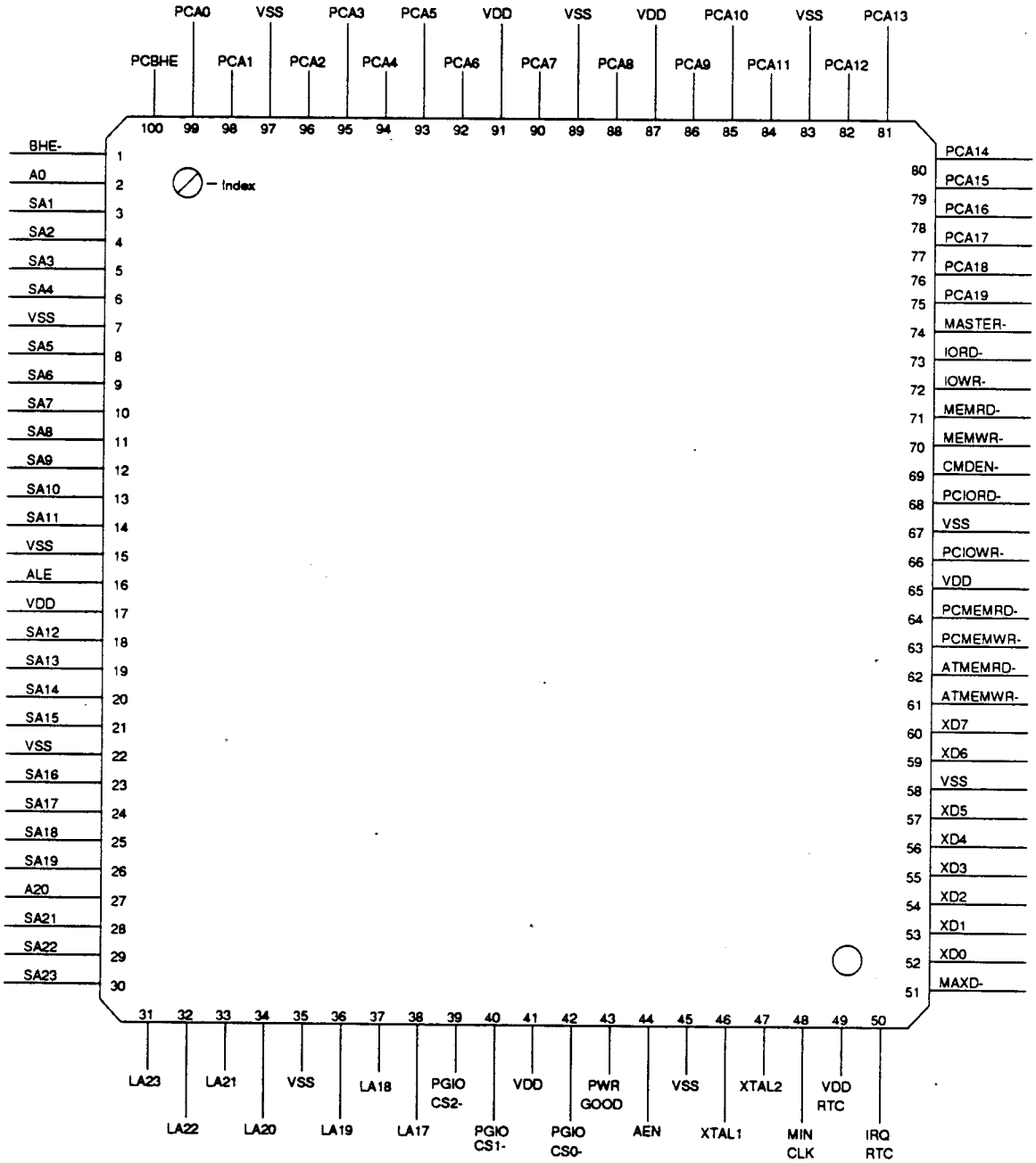
SYMBOL	PIN #	TYPE	NAME and FUNCTION
CMDEN-	69	I	COMMAND ENABLE: is an active low control signal to enable or disable the command buffer going to the I/O channel bus (PC bus). It is used to prevent bus contention between I/O devices that share the same address space resided in the X bus and in the I/O channel bus. CMDEN- is active low if: 1. Non DMA, all I/O cycles except: 1.1 Floppy I/O if an on-board floppy is enabled. 1.2 Hard Disk I/O if an on-board hard disk Controller is enabled. 1.3 Serial Com #1 if an on-board serial com. is enabled. 1.4 Parallel I/O if an on-board parallel port is enabled. 1.5 Video I/O if an on-board video is enabled. 1.6 Co-processor I/O. 2. During DMA cycle. 3. During memory refresh cycle. 4. Non DMA, PC memory cycle except: 4.1 On-board video is enabled and an on- board Video BIOS ROM has been specified through port 1A(Hex)bit 4 to 7. 4.2 On-board video is enabled and an on-board Video Memory has been specified through port 1B(Hex)bit 0 to 5.
PCIORD-	68	I/O	I/O READ COMMAND: active low command to instruct the I/O device on the I/O channel to drive its data onto the data bus.
PCIOWR-	66	I/O	I/O WRITE COMMAND: active low command to instruct the I/O device on the I/O channel to read the data present on the data bus.
PCMEMRD-	64	O	MEMORY READ COMMAND: active low signal to instruct the memory subsystem on the I/O channel to drive its data onto the data bus. The current cycle is within the 1M address space.
PCMEMWR-	63	O	MEMORY WRITE COMMAND: active low signal to instruct the memory subsystem on the I/O channel to store the data present on the data bus. The current cycle is within the 1M address space.
ATMEMRD-	62	I/O	MEMORY READ COMMAND: active low signal to instruct the memory subsystem to drive its data onto the data bus.
ATMEMWR-	61	I/O	MEMORY WRITE COMMAND: active low signal to instruct the memory subsystem to store the data present on the data bus.
AEN	44	I	ADDRESS ENABLE: is an active high signal during the DMA cycle to degate the I/O devices from the I/O channel to allow DMA transfers to take place.
MASTER-	74	I	MASTER: this signal is used together with a DRQ line to gain control of the system.
PWRGOOD	43	I	POWER GOOD: PWRGOOD comes from a power supply to indicate that power is stable. The signal is inactive if an under voltage condition occurs. The PWRGOOD signal has a turn on delay that is in between 100ms and 500ms. The OTI-051 provides a Schmitt trigger input for POWERGOOD.
PGIOCS0-	42	O	PROGRAMMABLE I/O CHIP SELECT 0: is an active low I/O chip select signal with a programmable I/O address space.
PGIOCS1-	40	O	PROGRAMMABLE I/O CHIP SELECT 1: is an active low I/O chip select signal with a programmable I/O address space.
PGIOCS2-	39	O	PROGRAMMABLE I/O CHIP SELECT 2: is an active low I/O chip select signal with a programmable I/O address space.

Table 1. OTI-054 Pin Description

SYMBOL	PIN #	TYPE	NAME and FUNCTION (Continued)
			***** REAL TIME CLOCK *****
XTAL1	46	I	XTAL INPUT FOR RTC: is the crystal input for the real time clock.
XTAL2	47	O	XTAL OUTPUT FOR RTC: is the crystal output for the real time clock.
MINCLK	48	O	MINUTE CLOCK: output signal from the minute count inside the Real Time Clock.
IRQRTC	50	O	INTERRUPT REQUEST FOR RTC: is an output from the real time clock requesting interrupt.
VDDRTC	49	I	POWER FOR RTC: battery power for the Real Time Clock.
			***** MISCELLANEOUS *****
MAXD-	51	O	ENABLE MA TO/FROM PCD: this is an active low signal used to enable the transceiver between MA1-8 and PCD0-7. This allows OTI-053 to be accessed through the PC-DATA bus.
VDD	17,41,65,87,91	I	5 V. SUPPLY: 5 pins
VSS	7,15,22,35,45, 58,67,83,89,97	I	GROUND: 10 pins.

NOTE: OTI-054 would enter into TEST mode under the following conditions:

MASTER-: '0'
PCIORD-: '0'
PCIOWR-: '0'


PCA0
VSS
PCA3
PCA5
VDD
VSS
VDD
PCA10
VSS
PCA13
PCBHE
PCA1
PCA2
PCA4
PCA6
PCA7
PCA8
PCA9
PCA11
PCA12
100 99 98 97 96 95 94 93 92 91 90 89 88 87 86 85 84 83 82 81
BHE-
A0
SA1
SA2
SA3
SA4
VSS
SA5
SA6
SA7
SA8
SA9
SA10
SA11
VSS
ALE
VDD
SA12
SA13
SA14
SA15
VSS
SA16
SA17
SA18
SA19
A20
SA21
SA22
SA23
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30
Index
80 79 78 77 76 75 74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54 53 52 51
PCA14
PCA15
PCA16
PCA17
PCA18
PCA19
MASTER-
IORD-
IOWR-
MEMRD-
MEMWR-
CMDEN-
PCIORD-
VSS
PCIOWR-
VDD
PCMEMRD-
PCMEMWR-
ATMEMRD-
ATMEMWR-
XD7
XD6
VSS
XD5
XD4
XD3
XD2
XD1
XD0
MAXD-
31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
LA23
LA22
LA21
LA20
VSS
LA19
LA18
LA17
PGIO CS2-
PGIO CS1-
VDD
PGIO CS0-
PWR GOOD
AEN
VSS
XTAL1
XTAL2
MIN CLK
VDD RTC
IRQ RTC

3.0 OTI-054 FUNCTIONAL DESCRIPTION

OTI-054 functions can be categorized as follows:

1. Address and Command Buffers
2. Real Time Clock
3. Programmable I/O Chip Selects

3.1 Address and Command Buffers

OTI-054 integrates all the address and command buffers that are specified in the AT bus. The propagation delay for all the buffers is 25ns. The output current on the AT bus side is 20 mA at a capacitive loading of 200 pF. On the CPU side, the capacitive loading is designed for 80 pF.

3.2 Real Time Clock

The Real Time Clock is compatible to MC146818 with the following exceptions:

- 128 Bytes of CMOS RAM total
- no CKFS (clock select input)
- no SQW (square wave output).

For a detailed description of the Real Time Clock, refer to the specification of MC146818.

Power to the Real Time Clock can be backed up by a 3V battery. When system power is down, battery power is routed to the Real Time Clock only, so that the Real Time Clock can still continue to run. Battery power is conserved, since it does not go to the other circuitry on the chip. The Real Time Clock has an extra output coming from the MINUTE counter. This signal is used by the power management circuitry as the MINUTE CLOCK in the other chips of the chipset. A total of 128 Bytes of CMOS RAM are implemented in the Real Time Clock. The extra 64 bytes can be accessed the same way as through the index register. The index range is 0 - 7F.

RT/CMOS and NMI Mask I/O Port 0070(Hex) W:

Bit	Function
7	Non-maskable Interrupt (NMI) 0 - NMI enabled 1 - NMI disabled
6-0	RTC/CMOS RAM address register to access the CMOS RAM

CMOS RAM Data Register I/O Port 0071(Hex) R/W:

To access the CMOS RAM, first write the index to port 70(Hex), then perform READ/WRITE to port 71.

4.3 Programmable I/O Chip Select

OTI-054 provides three programmable I/O chip select output pins. The I/O addresses for the 3 I/O chip selects can be programmed 8 bits at a time. Three indexed ports are provided for each I/O address to accomodate the 24-bit I/O address.

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4.0 ELECTRICAL CHARACTERISTICS

4.1 A.C. Characteristics

Table 2. A.C. Characteristics of OTI-054

A.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	LOADING CAPACITANCE
t1	ALE to PC Address Valid		25	ns	CL=100 pF
t2	SA Address to LA Address		25	ns	CL=100 pF
t3	PCA0 from A0 Delay		25	ns	CL=100 pF
t4	AT-BUS Command Delay		25	ns	CL=100 pF
t5	Master Mode Command Delay		25	ns	CL=80 pF
t6	Master Mode Address Delay		25	ns	CL=100 pF
t7	Address Valid Before ALE	40		ns	
t8	ALE Before IOWRN	35		ns	
t9	WRITE Data SETUP Time	100		ns	
t10	WRITE Data HOLD Time	20		ns	
t11	READ Data Valid from IORDN		100	ns	
t12	READ Data Float from IORDN	5		ns	
t13	Chip Selects from ALE		40	ns	

4.2 DC Characteristics

Table 3. DC Characteristics of OTI-054

D.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
VOH	Output HIGH Voltage	2.4		V	IOH=400 µA
VOL1	Output LOW Voltage		0.45	V	IOL=20 mA, Note 1
VOL2	Output LOW Voltage		0.45	V	IOL=16 mA, Note 1
VOL3	Output LOW Voltage		0.45	V	IOL=12 mA, Note 1
VOL4	Output LOW Voltage		0.45	V	IOL=10 mA, Note 1
VOL5	Output LOW Voltage		0.45	V	IOL= 8 mA, Note 1
VOL6	Output LOW Voltage		0.45	V	IOL= 4 mA, Note 1
VOL7	Output LOW Voltage		0.45	V	IOL= 2 mA, Note 1
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	TTL
VIL	Input LOW Voltage	- 0.5	0.8	V	TTL
VIS	Schmitt Input HIGH	2.4	VDD+0.5	V	Schmitt, Note 2
VIC	CMOS Input HIGH Voltage	3.8	VDD+0.5	V	CMOS, Note 2
ILI	Input Leakage Current	- 10	10	µA	
OLI	Output Leakage Current	- 10	10	µA	
ICC	Operating Supply Current		20	mA	Input=VDD or VSS No Output Load
IDDRTC	Real Time Clock Supply Current		16	µA	VDDRTC = 3 V
CI	Input Capacitance		8	pF	
CO	Output Capacitance		8	pF	
CIO	I/O Capacitance		16	pF	

1. Output Current (IOL) Capabilities:

20 mA :	ATMEMWRN,ATMEMRDN,PCMEMWRN,PCMEMRDN, PCIOWRN,PCIORDN,IOWRN,IORDN,PCA0-19
12 mA :	LA17-23
10 mA :	BHEN,SA0-23,PGIOCSN,MINCLK,IRQRTC,MAXDN,XD0-7,PBHEN
8 mA :	-
4 mA :	-
2 mA :	-

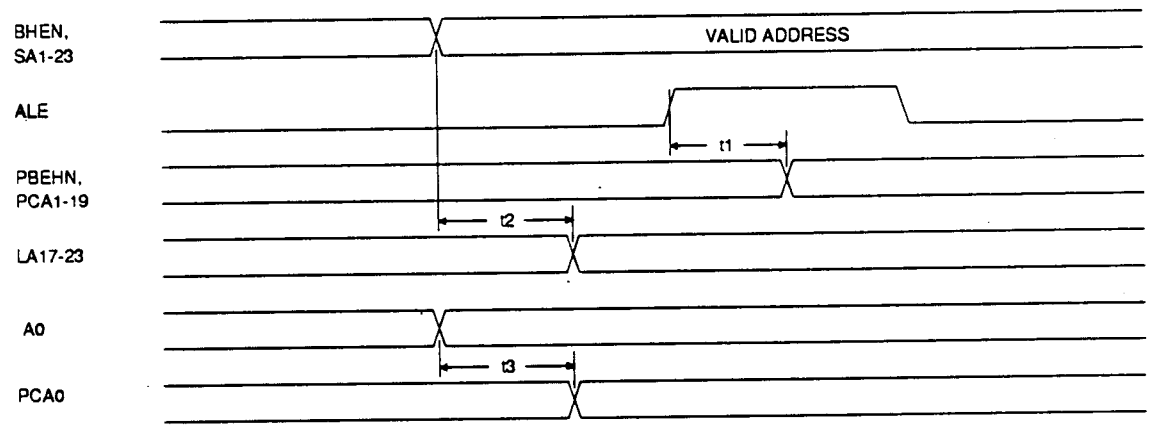
2. Input Structures:

Schmitt triggered:	-
CMOS :	-
TTL :	All Others
Input with Pullup:	-

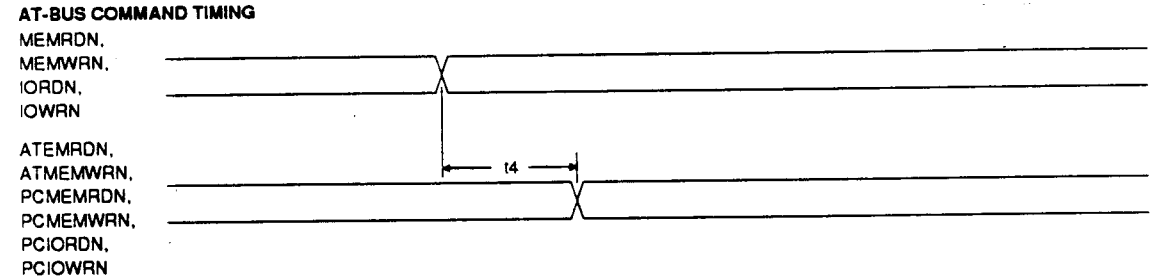
5.0 OTI-054 TIMING DIAGRAMS

FIGURE 4-1.

AT-BUS ADDRESS TIMING



AT-BUS COMMAND TIMING



MASTER MODE TIMING

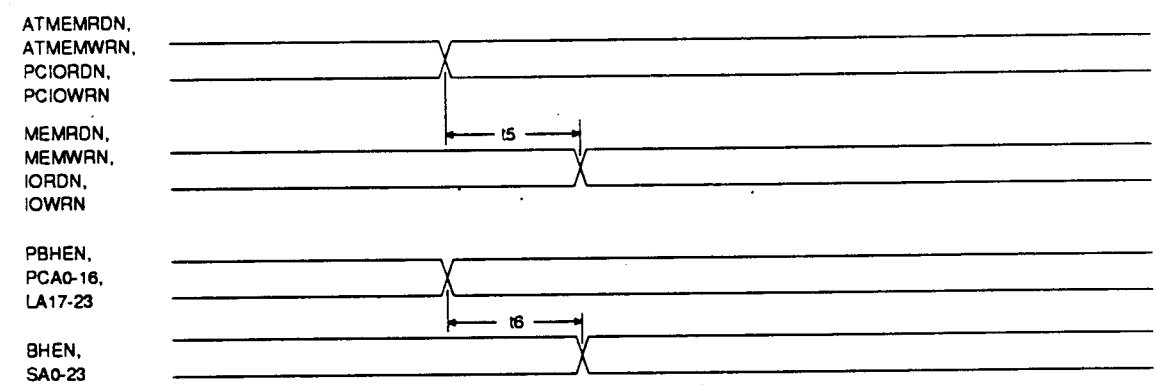
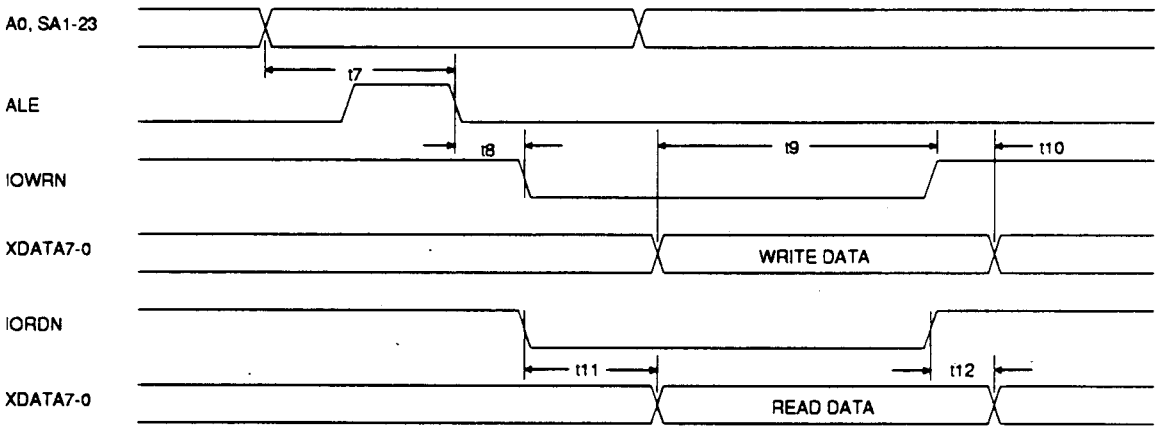


FIGURE 4-2.

I/O CYCLE TIMING



CHIP SELECT TIMING