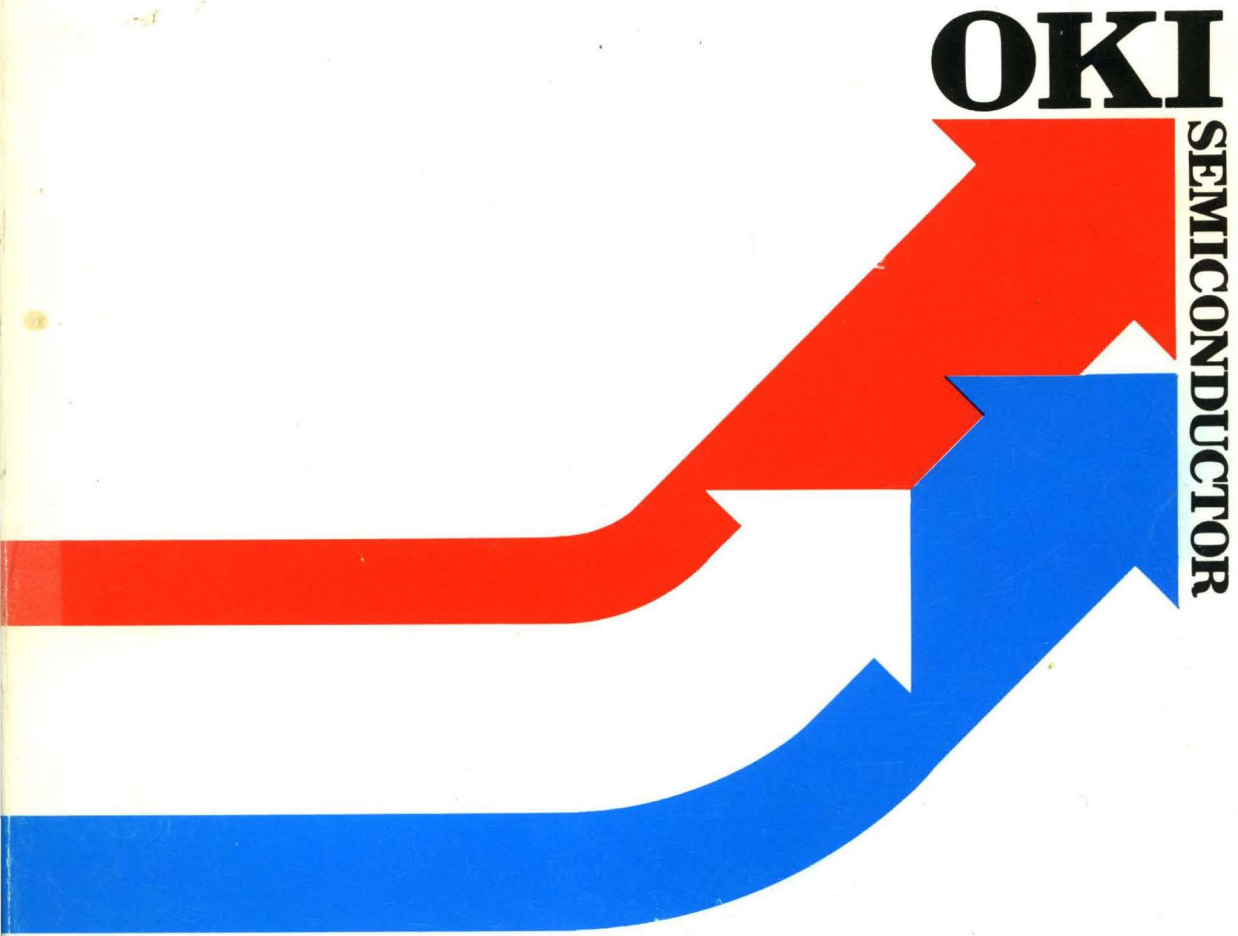
MEMORY DATABOOK 1983



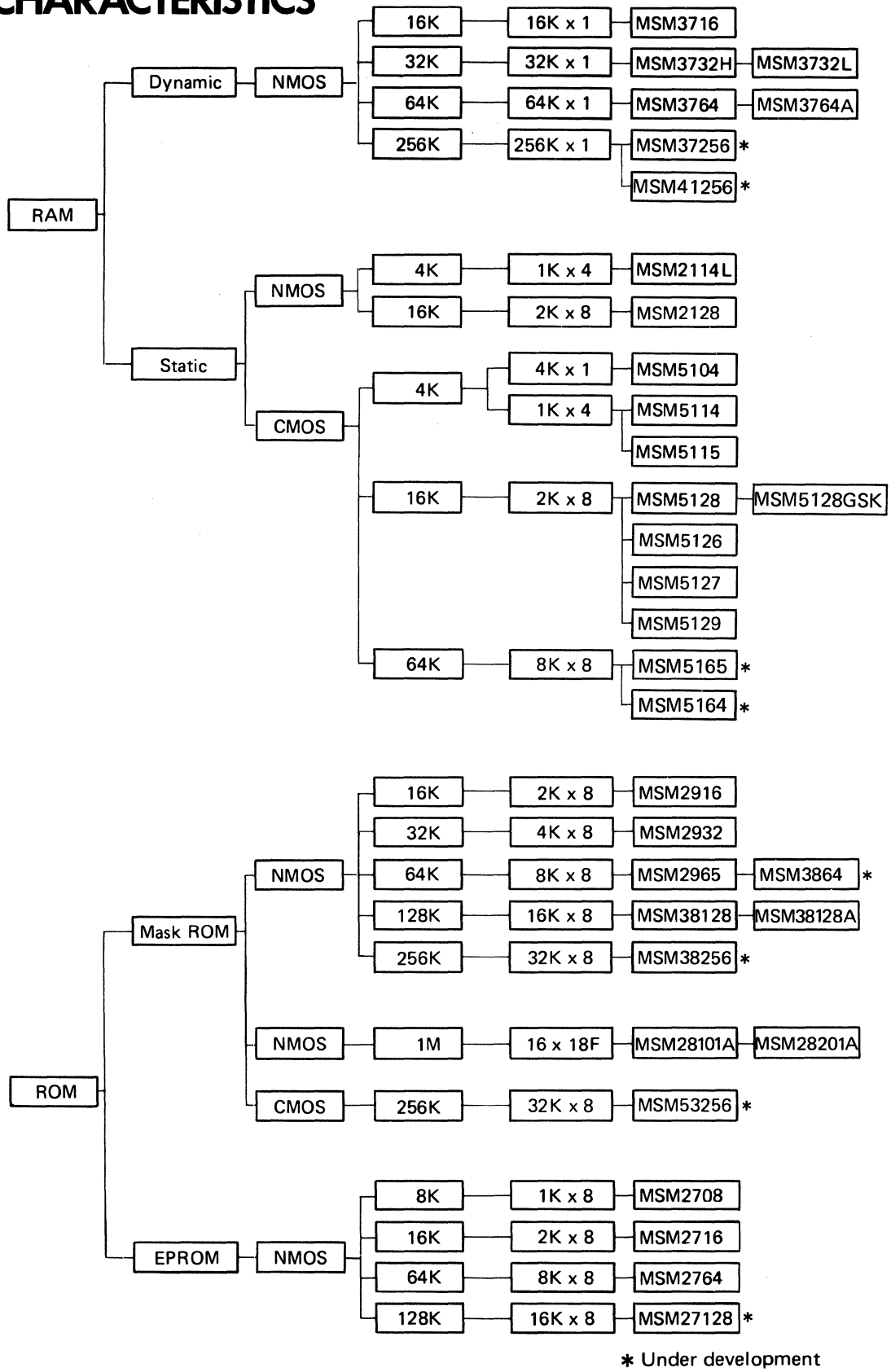
2nd Edition: May, 1983

CONTENTS

(All specifications and details published are subject to change without notice.)

IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS

1 IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS



* Under development

• DYNAMIC RAMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM3716-2	16k	16 Pin Dynamic	16,384 x 1	16	150	375	528/20	+12,+5	MK4116-2
MSM3716-3					200	375	528/20	-5	MK4116-3
MSM3732H-15	32k	16 Pin Dynamic A7 (Column)=H	32,768 x 1	16	150	270	248/28	+5	
MSM3732H-20					200	330	248/28		
MSM3732L-15	32k	16 Pin Dynamic A7 (Column)=L	32,768 x 1	16	150	270	248/28	+5	
MSM3732L-20					200	330	248/28		
MSM3764-15	64k	16 Pin Dynamic	65,536 x 1	16	150	270	248/28	+5	TMS4164-15
MSM3764-20					200	330	248/28		TMS4164-20
MSM3764A-12	64K	16 Pin Dynamic	65,536 x 1	16	120	230	330/28	+5	
MSM3764A-15					150	260	330/28		
MSM3764A-20					200	330	330/28		
MSM37256-15	256k	16 Pin Dynamic	262,144x1	16	150	270	440/28	+5	
MSM37256-20					200	330	440/28		
MSM41256-10	256k	16 Pin Dynamic	262,144x1	16	100	200	415/28	+5	
MSM41256-12					120	230	415/28		
MSM41256-15					150	280	415/28		

• NMOS STATIC RAMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM2114L-2	4K	Static, Common I/O	1024 x 4	18	200	200	396	+5	2114L2
MSM2114L-3					300	300	396		2114L3
MSM2114L					450	450	396		2114L
MSM2128-12	16K	Static, Common I/O with Power Down Mode	2048 x 8	24	120	120	660/110	+5	TMM2016 M58725
MSM2128-15					150	150	550/110		
MSM2128-20					200	200	550/110		

■ IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS ■

• CMOS STATIC RAMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM5114-2	4K	Fully Static, Common I/O	1024x4	18	200	200	192/0.04	+5	TC5514 μPD444
MSM5114-3					300	300	192/0.04		
MSM5114					450	450	192/0.04		
MSM5115-2	4K	Clocked Static, Common I/O	1024x4	18	200	300	33/0.04	+5	HM6514
MSM5115-3					300	420	33/0.04		
MSM5104-2	4K	Clocked Static, Common I/O	4096x1	18	200	300	33/0.04	+5	HM6504
MSM5104-3					300	420	33/0.04		
MSM5128-12	16K	Fully Static, Common I/O	2048x8	24	120	120	330/0.275	+5	HM6116 μPD446
MSM5128-15					150	150	300/0.275		
MSM5128-20					200	200	275/0.275		
MSM5127-15	16K	Fully Static Common I/O	2048x8	24	150	150	300/0.275	+5	
MSM5127-20	16K				200	200	275/0.275		
MSM5129-15	16K	Fully Static Common I/O	2048x8	24	150	150	300/0.275	+5	
MSM5129-20	16K				200	200	275/0.275		
MSM5126-20	16K	Fully Static Common I/O	2048x8	24	150	150	385/0.165	+5	
MSM5126-25	16K				200	200	385/0.165		
MSM5165	64K	Fully Static Common I/O	8192x8	28	100	100	495/5.5	+5	
					120	120			
					150	150			

• EPROMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mW) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM2708	8k	24 Pin EPROM	1024 x 8	24	450	450	800	+12,+5 -5	2708
MSM2716	16k	24 Pin EPROM	2048 x 8	24	450	450	525/132	+5	2716
MSM2764	64k	28 Pin EPROM	8192x8	28	200	200	790/185	+5	2764
MSM27128	128k	28 Pin EPROM	16,384x8	28	250	250	788/184	+5	27128

• MASK ROMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mW) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM2916	16K	24 Pin MASK ROM	2048x8	24	250	250	550	+5	2716 EPROM
MSM2932	32K	24 Pin MASK ROM	4096x8	24	300	300	687	+5	2532 EPROM
MSM2965	64K	24 Pin MASK ROM	8192x8	24	300	300	687	+5	
MSM3864	64K	28 Pin MASK ROM	8192x8	28	250	250	550	+5	
MSM38128	128K	28 Pin MASK ROM	16384x8	28	450	450	660/110	+5	
MSM38128A	128K	28 Pin MASK ROM	16384x8	28	250	250	550	+5	
MSM38256	256K	28 Pin MASK ROM	32768x8	28	250	250	660	+5	
MSM28101	1M	40 Pin MASK RAM 18x16 Chinese-character font output	3760x16 x18	40	10μS	22μS	893	+5	JIS-Chinese-character coding system 0~7, 16~47
MSM28201									JIS Chinese-character coding system 48~87
MSM53256	256K	28 Pin CMOS MASK ROM	32768x8	28	200	200		+5	

PACKAGING

2

PACKAGING

2

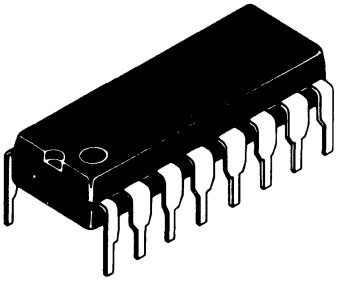
Name	No. of Pins	Packages		
		RS	AS	
		PLASTIC	CERDIP	SIDE-BRAZED
MSM3716	16	○		○
3732	16	○		○
3764	16	○		○
3764A	16	○		○
37256	16			○
2114L	18	○		○
2128	24	○		
5104	18	○		○
5114	18	○		○
5115	18	○		○
5126	24	○		
5127	24	○		
5128	24	○		
5129	24	○		
5165	28	○		○
2916	24	○	○	
2932	24	○	○	
2965	24	○		
3864	28	○		
38128	28	○		
38128A	28	○		
38256	28	○		
38256A	28	○		
53256	28	○		
28101A	40			○
28201A	40			○
2708	24		○	
2716	24		○	
2764	28		○	
27128	28		○	

Note: Model names suffixed by RS denote plastic mold devices, while AS denotes cerdip or side-brazed devices.

Ex. MSM2916RS . . . . . plastic mold device

MSM2916AS . . . . . cerdip or side-brazed device

• 16 PIN PLASTIC



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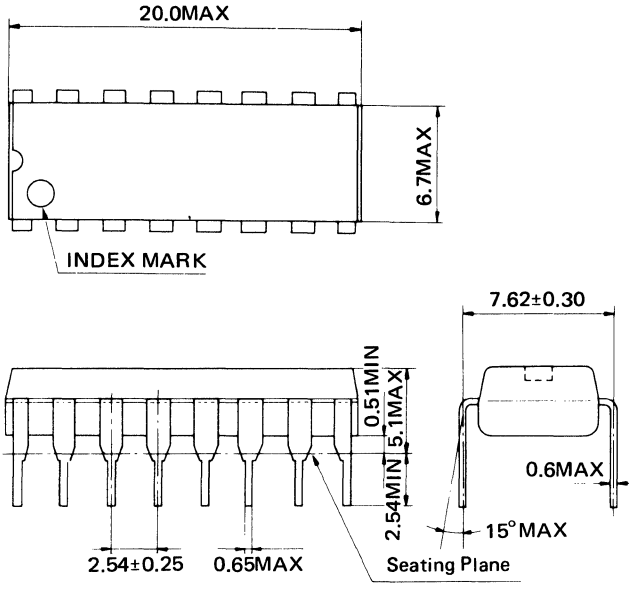
MSM3732
MSM3764



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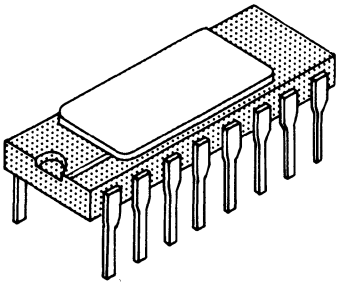
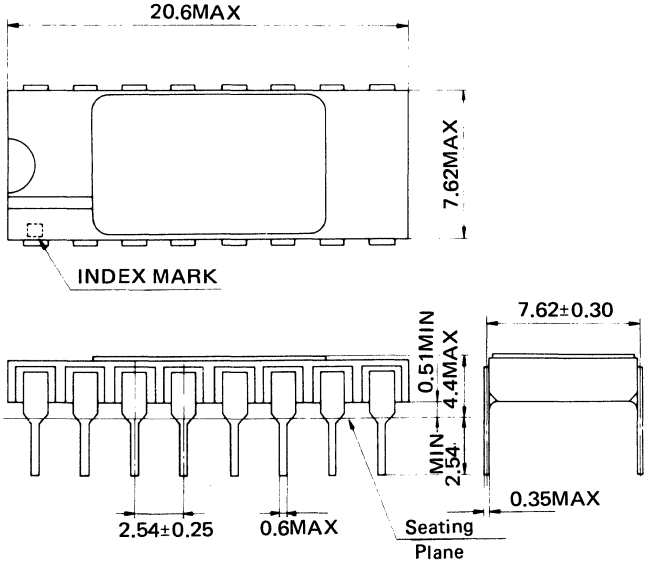


MSM3716



• 16 PIN SIDE-BRAZED

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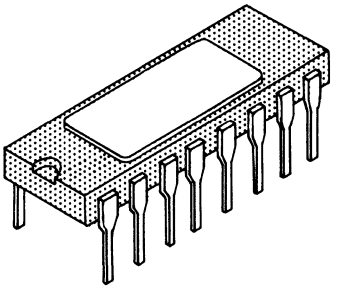

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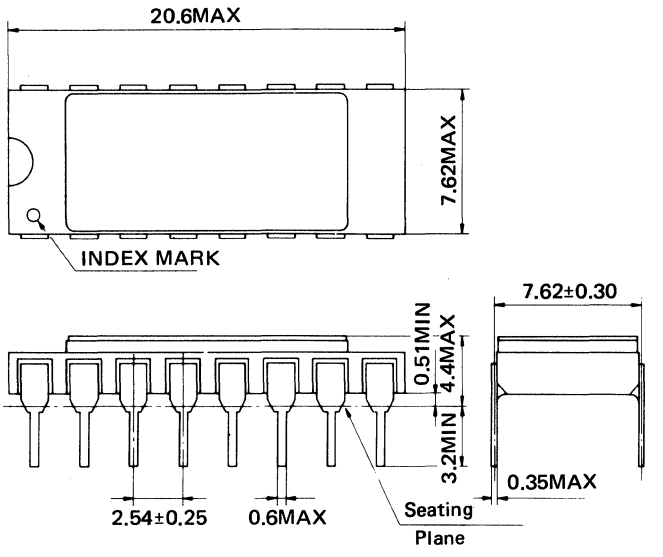
MSM3764A
MSM37256



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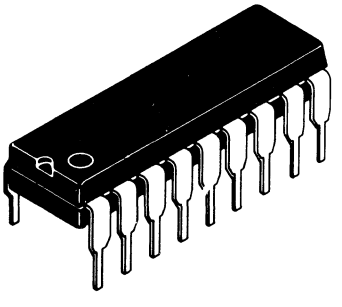

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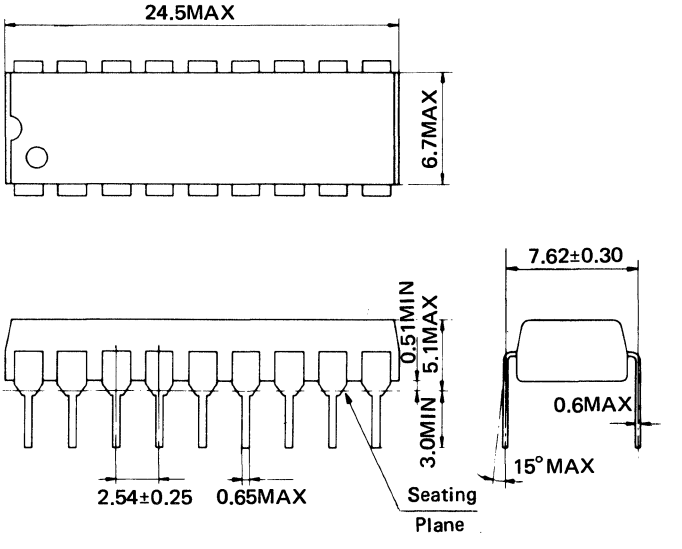
MSM5114
MSM5115



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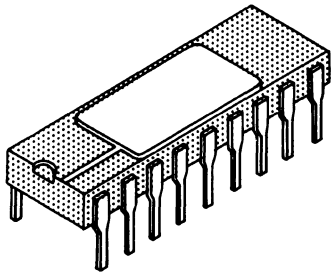

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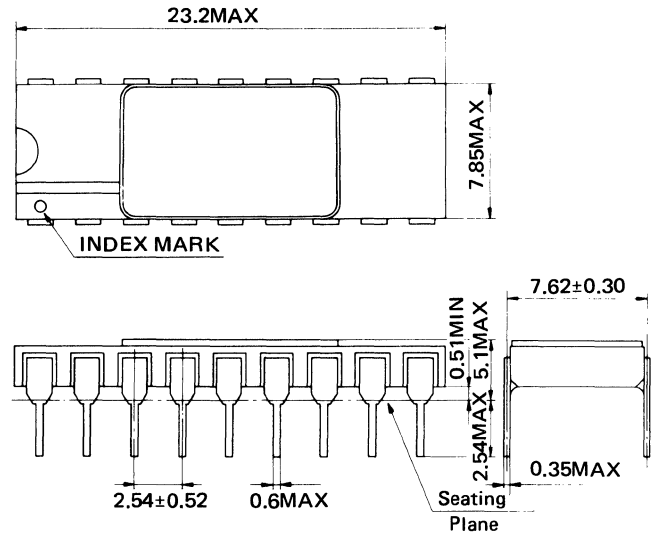
MSM5114
MSM5115



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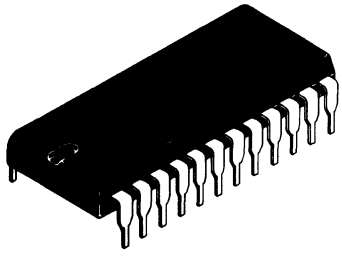

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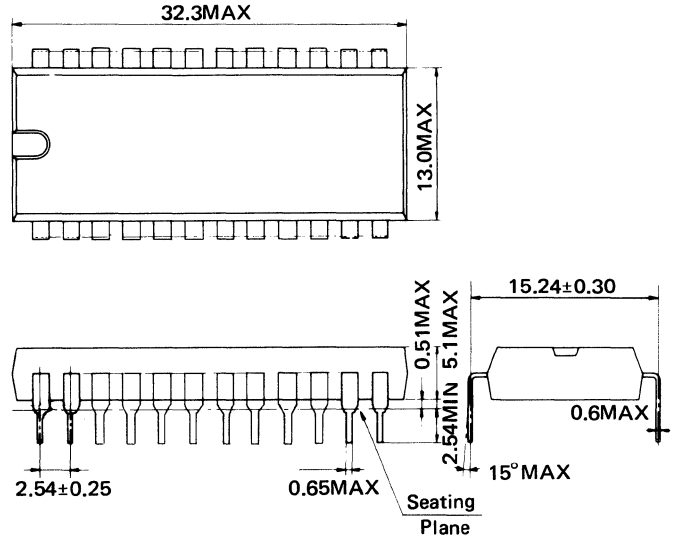
MSM2916
MSM2932
MSM5127
MSM5129
MSM5126
MSM2965



• 24 PIN CERDIP

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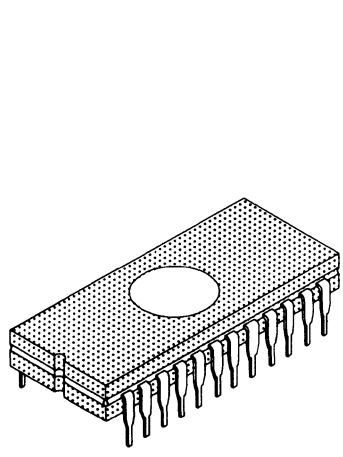

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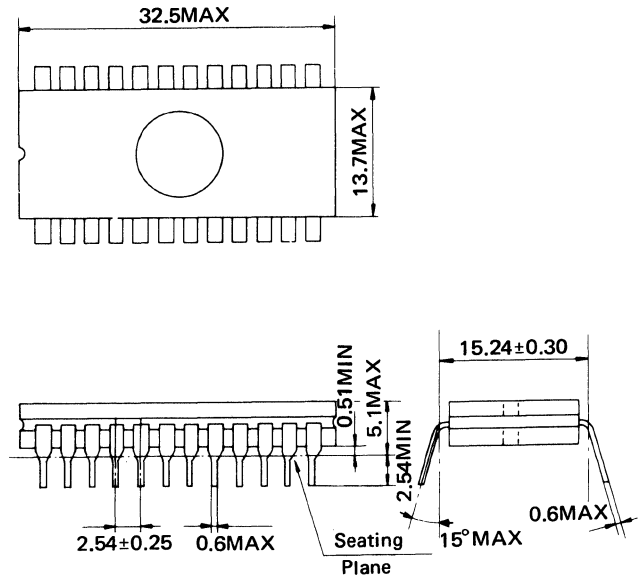
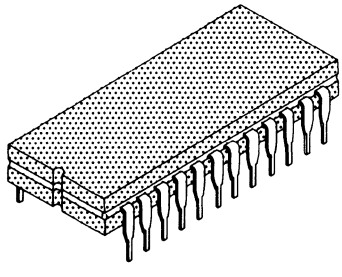
MSM2716



• 24 PIN CERDIP



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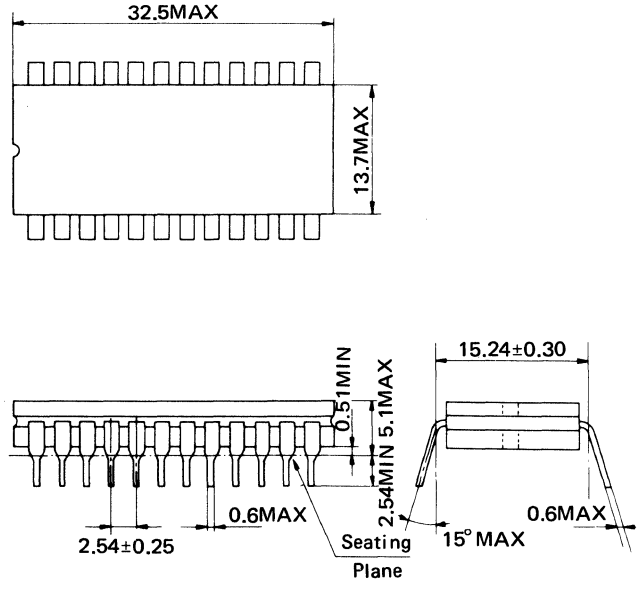

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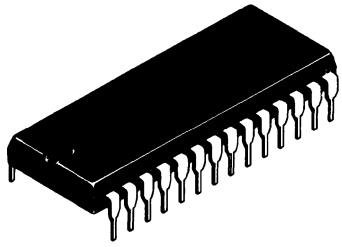

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MSM38256
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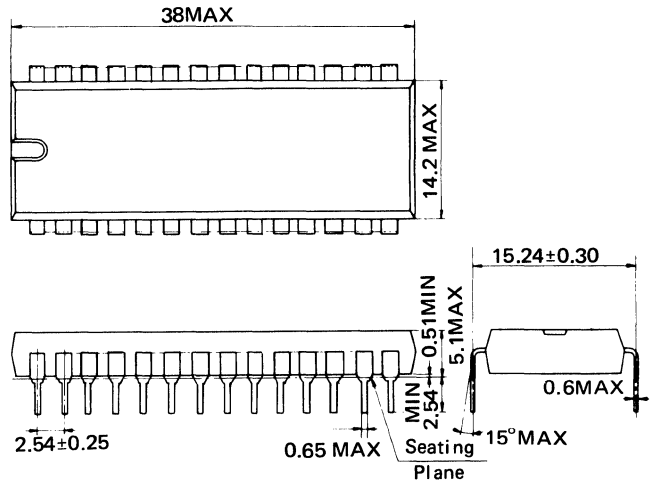
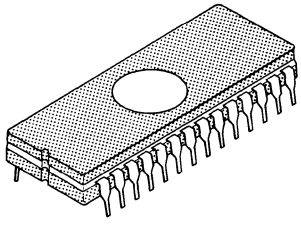


• 28 PIN CERDIP



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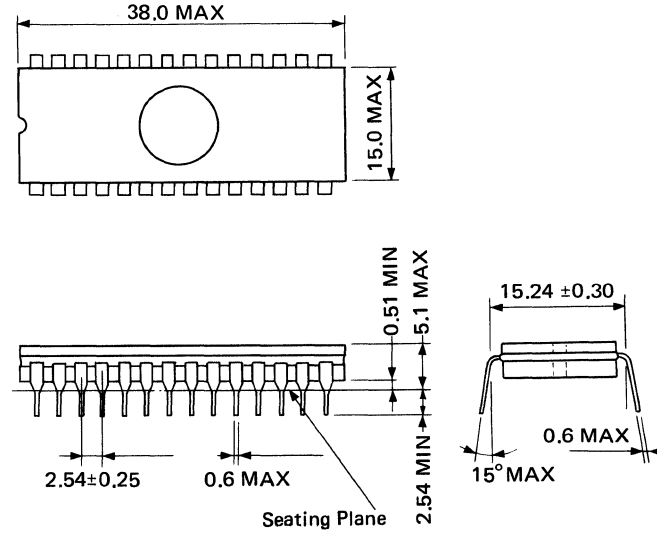
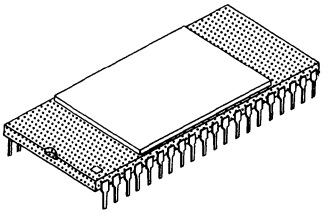
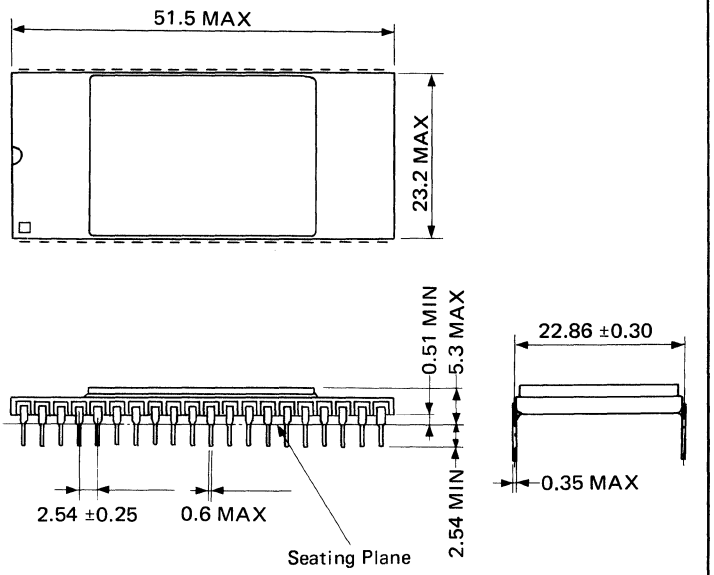
MSM27128



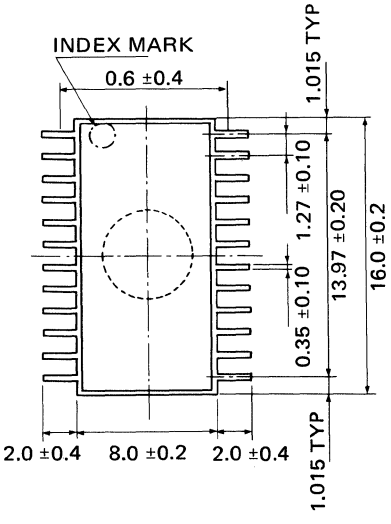
• 40 PIN SIDE-BRAZED

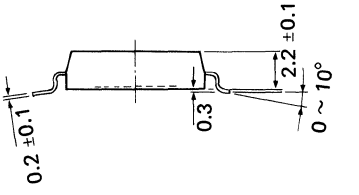


MSM28101A
MSM28201A



• 24 PIN PLASTIC FLAT





MSM5128GSK

RELIABILITY INFORMATION

RELIABILITY INFORMATION

1. INTRODUCTION

Semiconductor memories play a leading role in the explosive progress of semiconductor technology. They use some of the most advanced design and manufacturing technology developed to date. With greater integration, diversity and reliability, their applications have expanded enormously. Their use in large scale computers, control equipment, calculators, electronic games and in many other fields has increased at a fast rate.

A failure in electronic banking or telephone switching equipment, for example, could have far reaching effects and can cause incalculable losses. So, the demand, for stable high quality memory devices is strong.

We, at Oki Electric is fully aware of this demand. So we have adopted a comprehensive quality assurance system based on the concept of consistency in development, manufacturing and sales.

With the increasing demand for improvement in function, capability and reliability, we will expand our efforts in the future. Our quality assurance system and the underlying concepts are outlined briefy below.

2. QUALITY ASSURANCE SYSTEM AND UNDERLYING CONCEPTS

The quality assurance system employed by Oki Electric can be divided into 4 major stages: device planning, developmental prototype, production prototype, and mass production. This system is outlined in the following block diagram (Fig. 1-1).

1) Device planning stage

To manufacture devices that meet the market demands and satisfy customer needs, we carefully consider functional and failure rate requirements, utilization form, environment and other conditions. Once we determine the proper type, material and structure, we check the design and manufacturing techniques and the line processing capacity. Then we prepare the development planning and time schedule.

2) Developmental prototype stage

We determine circuits, pattern design, process settings, assembly techniques and structural requirements during this stage. At the same time, we carry out actual prototype reliability testing.

Since device quality is largely determined during the designing stage, Oki Electric pays careful attention to quality confirmation during this stage.

This is how we do it:

(1) After completion of circuit design (or pattern design), personnel from the design, process technology, production technology, installation technology and reliability departments get together for a thorough review to ensure design quality and to anticipate problems that may occur during mass production. Past experience and know-how guide these discussions.

(2) Since many semiconductor memories involve new concepts and employ high level manufacturing technology, the TEG evaluation test is often used during this stage.

Note: TEG (Test Element Group) refers to the device group designed for stability evaluation of MOS transistors, diodes, resistors, capacitors and other circuit component element used in LSI memories.

(3) Prototypes are subjected to repeated reliability and other special evaluation tests. In addition, the stability and capacity of the manufacturing process are checked.

3) Production prototype stage

During this stage, various tests check the reliability and other special features of the production prototype at the mass production factory level. After confirming the quality of device, we prepare the various standards required for mass production, and then start production. Although reliability and other special tests performed on the production prototype are much the same as those performed on the developmental prototype, the personnel, facilities and production site differ for the two prototypes, necessitating repeated confirmation tests.

4) Mass production

During the mass production stage, careful management of purchased materials, parts and facilities used during the manufacturing process, measuring equipment, manufacturing conditions and environment is necessary to ensure device quality first stipulated during the designing stages. The manufacturing process (including inspection of the completed device) is followed by a lot guarantee inspection to check that the specified quality is maintained under conditions identical to those under which a customer would actually use the device. This lot guarantee inspection is performed in 3 different forms as shown below.

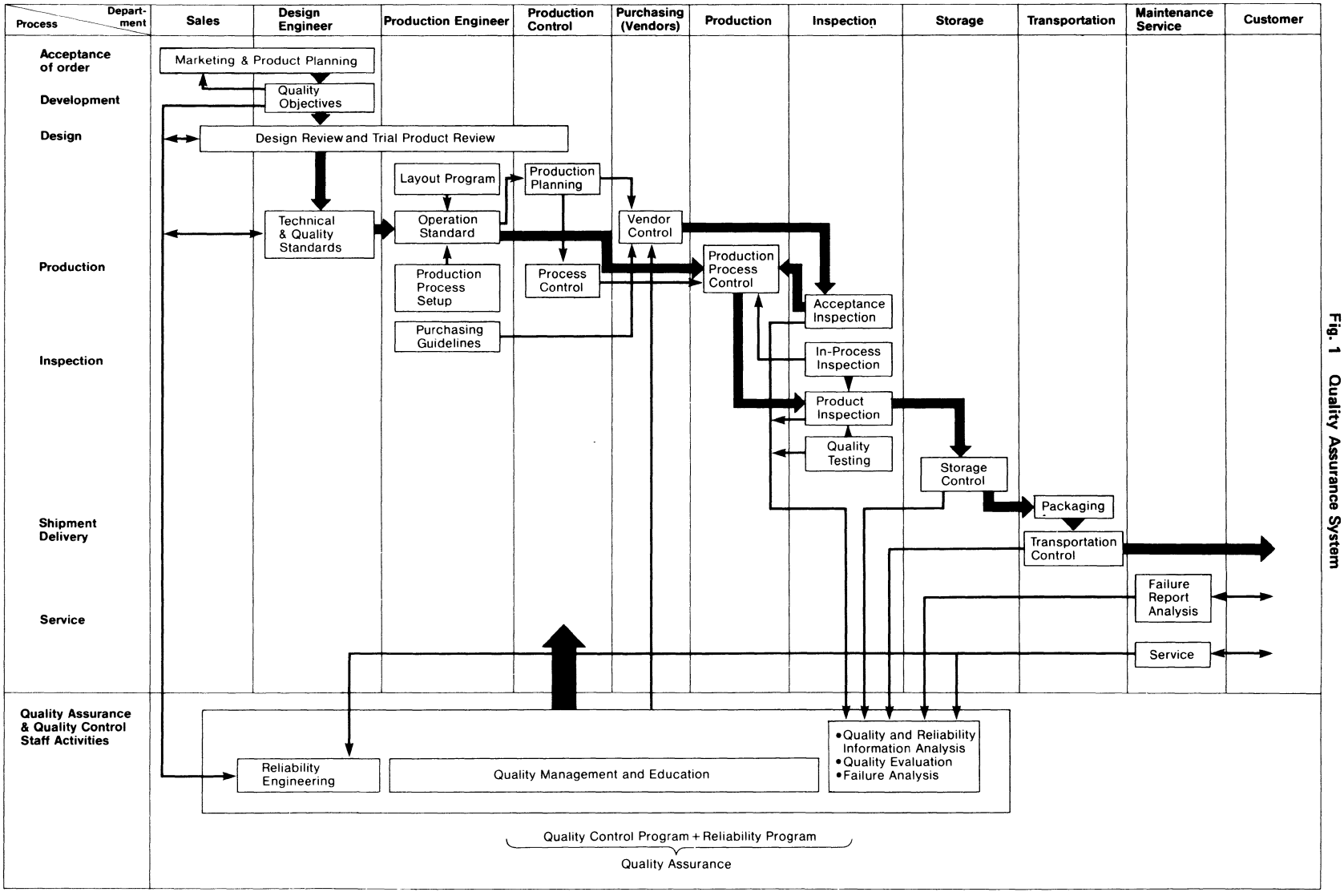
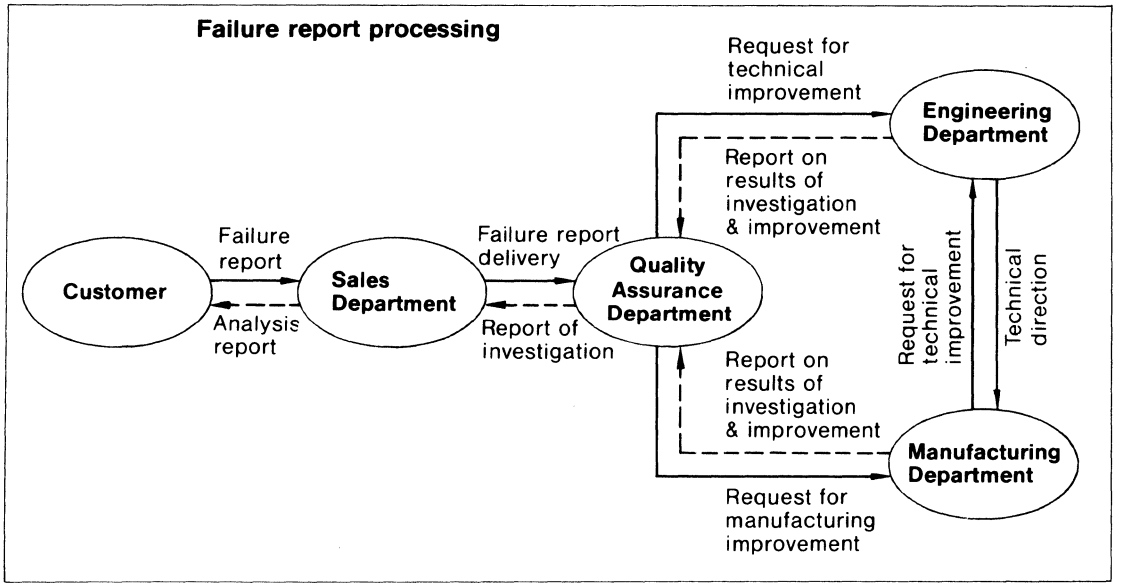


Fig. 1 Quality Assurance System

Fig. 2 Defect Processing Flowchart



(1) Group A tests: appearance, labels, dimensions and electrical characteristics inspection

(2) Group B tests: check of durability under thermal and mechanical environmental stresses, and operating life characteristics

(3) Group C tests: performed periodically to check operational life etc on long term basis.

Note: Like the reliability tests, the group B tests conform to the following standards.
MIL-STD-883B, JIS C 7022, EIAJ-IC-121

Devices which pass these lot guarantee inspections are stored in a warehouse awaiting shipment to customers. Standards are also set up for handling, storage and transportation during this period, thereby ensuring quality prior to delivery.

5) At Oki Electric, all devices are subjected to thorough quality checks. If, by chance, a failure does occur after delivery to the customer, defective devices are processed and the problem rectified immediately to minimize the inconvenience to the customer in accordance with the following flowchart.

3. EXAMPLE OF RELIABILITY TEST RESULTS

We have outlined the quality assurance system and the underlying concepts employed by Oki Electric. Now, we will give a few examples of the reliability tests performed during the developmental and production prototype stages. All reliability tests performed by Oki Electric conform with the following standards.

MIL-STD-883B, JIS C 7022, EIAJ-IC-121

OKI MEMORY LSI LIFE TEST RESULTS

Test item	Test condition	Device name	MSM3764-XXRS			MSM2128-XXRS			MSM5128-XXRS		
		Function	65536 x 1 bit DYNAMIC RAM			2048 x 8 bit STATIC RAM			2048 x 8 bit STATIC RAM		
		Structure	Si gate N-MOS 16P plastic package			Si gate N-MOS 24P plastic package			Si gate C-MOS 24P plastic package		
			Sample size	Test hours	Failures	Sample Size	Test hours	Failures	Sample size	Test hours	Failures
Operating life test	Ta = 125°C Vcc = 5.5V		175	3000	0	40	1000	0	100	1000	0
	Ta = 150°C Vcc = 5.5V		50	1000	0				50	2000	0
Temperature humidity test	140°C 85% Vcc = 5.5V		90	100	0				20	100	0
	85°C 85% Vcc = 5.5V		520	3000	0	40	1000	0	70	1000	0
Pressure cooker test	121°C 100% No bias		340	300	0	40	300	0	50	300	0

Test item	Test condition	Device name	MSM2764-AS			MSM38128-XXRS			MSM2965-XXRS		
		Function	8192 x 8 bit UV erasable EP ROM			16384 x 8 bit Mask ROM			8192 x 8 bit Mask ROM		
		Structure	Si gate N-MOS 28 P cerdip			Si gate N-MOS 28P plastic package			Si gate N-MOS 24P plastic package		
			Sample size	Test hours	Failures	Sample Size	Test hours	Failures	Sample size	Test hours	Failures
Operating life test	Ta = 125°C Vcc = 5.5V					40	2000	0	40	2000	0
	Ta = 150°C Vcc = 5.5V		40	1000	0						
Temperature humidity test	140°C 85% Vcc = 5.5V										
	85°C 85% Vcc = 5.5V		50	1000	0	20	2000	0	40	1500	0
Pressure cooker test	121°C 100% No bias					40	500	0	40	168	0

3

OKI MEMORY LSI ENVIRONMENTAL TEST RESULTS

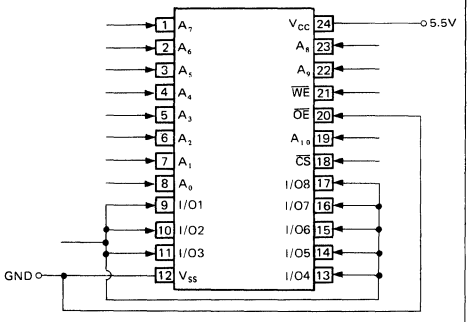
Test item		Device name / Test condition	MSM3764-XXRS Sample size	MSM3764-XXRS Failures	MSM2128-XXRS Sample size	MSM2128-XXRS Failures	MSM5128-XXRS Sample size	MSM5128-XXRS Failures
Thermal environmental test	Soldering heat	260°C 10 sec	20	0	20	0	25	0
	Thermal shock	0°C~100°C 5 min 5 min 10 cycles						
	Temperature cycling	−55°C~RT~150°C 30 min 30 min 100 cycles	320	0	100	0	65	0
Mechanical environmental test	Variable frequency vibration	100Hz~200Hz 4 min per cycle 4 times in X, Y, Z	20	0	20	0	18	0
	Shock	1500G, 0.5 ms, 5 times in each X, Y, Z						
	Constant acceleration	10000G or 20000G 1 min in each X, Y, Z						
Electrical Environmental test	ESD	200pF, 0Ω, 5 times	10	0	10	0	10	0

Test item		Device name / Test condition	MSM2764AS Sample size	MSM2764AS Failures	MSM38128-XXRS Sample size	MSM38128-XXRS Failures	MSM2965-XXRS Sample size	MSM2965-XXRS Failures
Thermal environmental test	Soldering heat	260°C 10 sec	50	0	10	0	50	0
	Thermal shock	0°C~100°C 5 min 5 min 10 cycles						
	Temperature cycling	−55°C~RT~150°C 30 min 30 min 100 cycles	50 (−65°~ RT~ 150°C 30′ 3′ 30′ 20∞)	0	126	0	80	0
Mechanical environmental test	Variable frequency vibration	100Hz~200Hz 4 min per cycle 4 times in X, Y, Z	50	0				
	Shock	1500G, 0.5 ms, 5 times in each X, Y, Z						
	Constant acceleration	10000G or 20000G 1 min in each X, Y, Z						
Electrical environmental test	ESD	200pF, 0Ω, 5 times	10	0	10	0	10	0

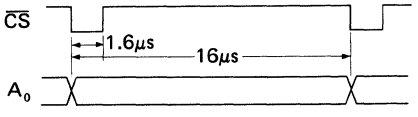
◆ **Data example 1**

Device: MSM2128-XXRS
Test: Continuous operation under high temperature
Test conditions: Ta = 125°C, Vcc = 5.5V, f = 63 kHz

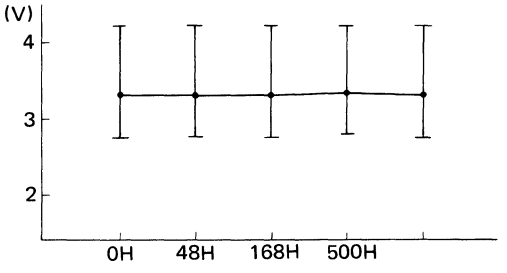
Test circuit



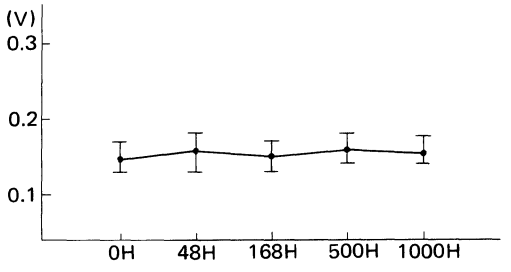
$\overline{CS}$ Timing



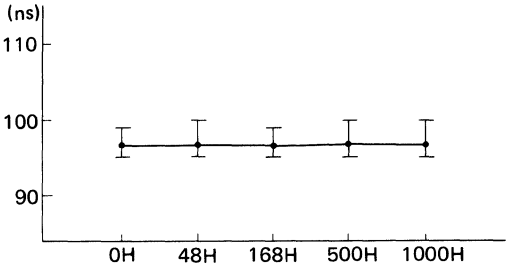
V_{OH} MAX



V_{OL} MAX



T_{AC}

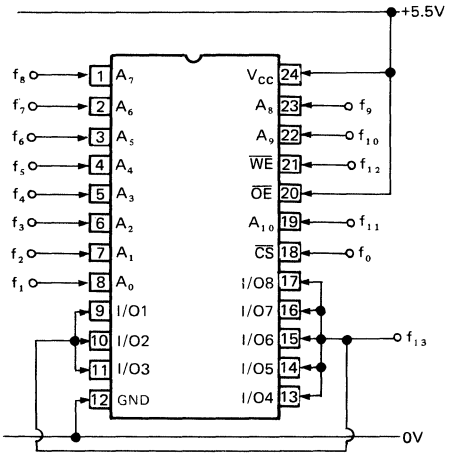


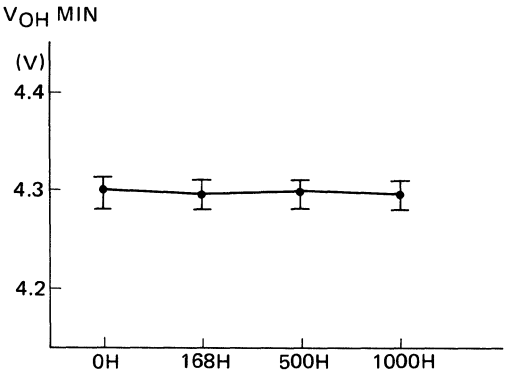
3

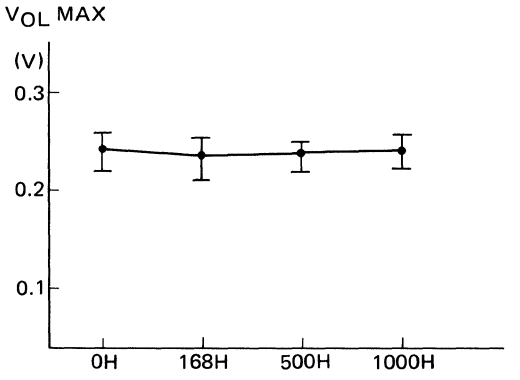
♦ **Data example 2**

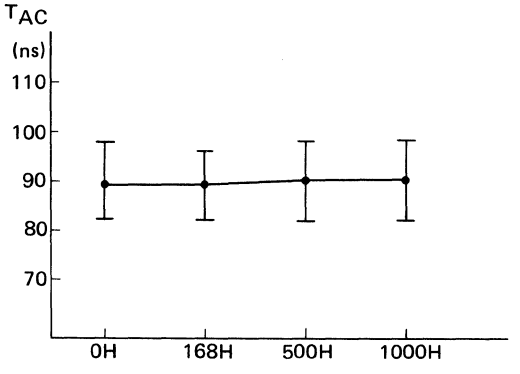
Device: MSM5128-XXRS
Test: Continuous operation under high temperature
Test conditions: Ta = 125°C, Vcc = 5.5V

Test circuit





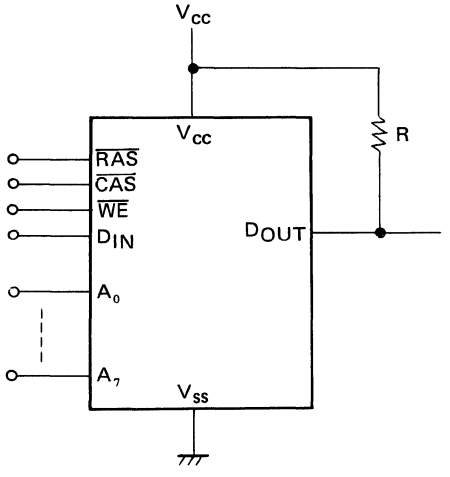


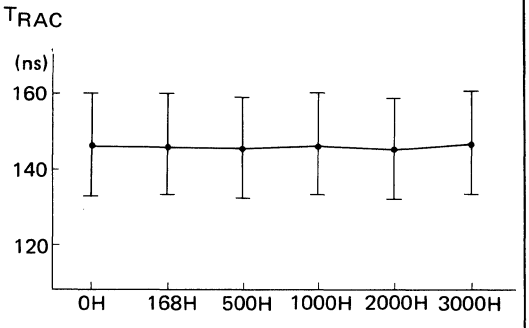


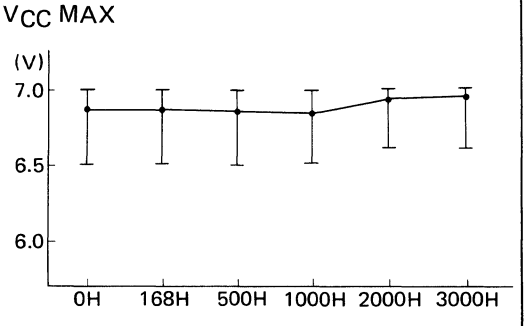
◆ Data example 3

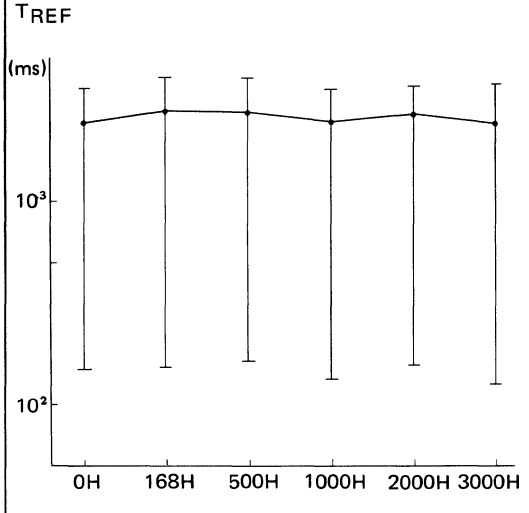
Device: MSM3764-XXRS
Test: Continuous operation under high temperature
Test conditions: Ta = 125°C, Vcc = 5.5V, f = 330 kHz

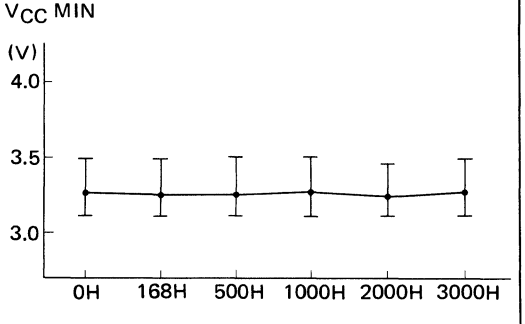
Test circuit











Since these reliability tests must determine performance under actual working conditions in a short period of time, they are performed under severe test conditions. For example, the 125°C high temperature continuous operation test performed for 1000 hours is equivalent to testing device life from 2 to 300 years of use at Ta = 40°C.

By repeating these accelerated reliability tests, device quality is checked and defects analyzed. The resulting information is extremely useful in improving the manufacturing processes. Some of the more common defects in memory LSI elements and their analysis are described below.

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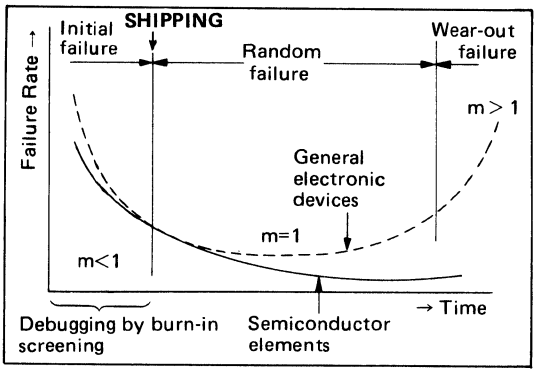
4. SEMICONDUCTOR MEMORY FAILURES

The life-span characteristics of semiconductor elements in general (not only semiconductor IC devices) is described by the curve shown in the diagram below. Although semiconductor memory failures are similar to those of ordinary integrated circuits, the degree of integration (miniaturization), manufacturing complexity and other circuit element factors influence their incidence.

< Semiconductor Element Failure Rate Curve >

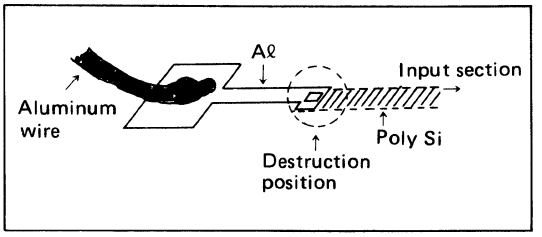


1) Surge Destruction

This is destruction of the input/output stage circuits by external surge currents or static electricity. The accompanying photograph shows a point of contact between aluminum and poly-silicon that has been dissolved by a surge current. A hole has formed in the substrate silicon, leading to a short circuit. This kind of failure is traceable in about 30% of defective devices returned to the manufacturer. Despite miniaturization of semiconductor memory component elements (which means the elements themselves are less resistant), these failures usually occur during assembly and other handling operations.

At Oki Electric, all devices are subjected to static electricity intensity tests (under simulated operational conditions) in the development stage to reduce this type of failure. In addition to checking endurance against surge currents, special protective circuits are incorporated in the input and output sections.

Example of surge destruction



2) Oxide Film Insulation Destruction (Pin Holes)

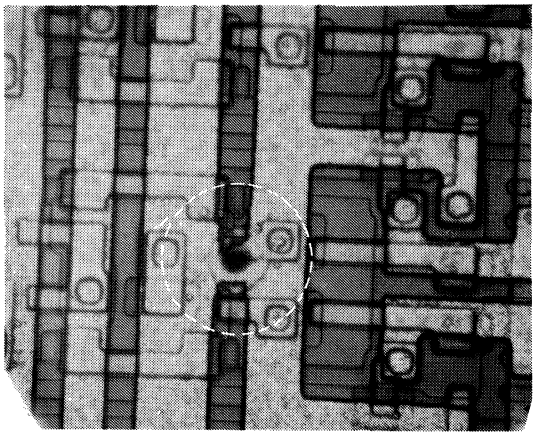
Unlike surge destruction, this kind of failure is caused by manufacturing defects. Local weakened sections are ruptured when subjected to external electrical stress. Although this problem is accentuated by the miniaturization of circuit elements, it can be resolved by maintaining an ultra-clean manufacturing environment and through 100% burn-in screening.

3) Surface Deterioration due to Ionic Impurities

Under some temperature and electric field conditions, charged ionic impurities moving within the oxide film previously resulted in occasional deterioration of silicon surfaces. This problem has been eliminated by new surface stabilization techniques.

4) Photolithographic Defects

Integrated circuits are formed by repeated photographic etching processes. Dust and scratches on the mask (which corresponds to a photographic negative) can cause catastrophic defects. At present, component elements have been reduced in size to the order of 10^{-4} cm through miniaturization. However, the size of dust and scratches stays the same. At Oki Electric, a high degree of automation, minimizing human intervention in the process, and unparalleled cleanliness solves this problem.



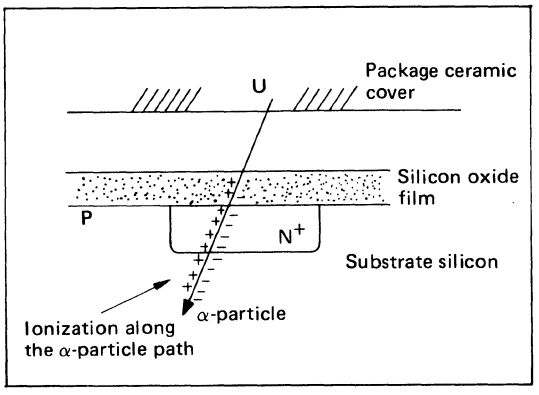
Photolithographic Defect
(Gate not formed in circled area)

5) Aluminum Corrosion

Aluminum corrosion is due to electrolytic reactions caused by the presence of water and minute impurities. When aluminum dissolves, lines break. This problem is unique to the plastic capsules now used widely to reduce costs. Oki Electric has carefully studied the possible cause and effect relationship between structure and manufacturing conditions on the one hand, and the generation of aluminum corrosion on the other. Refinements incorporated in Oki LSIs permit superior endurance to even the most severe high humidity conditions.

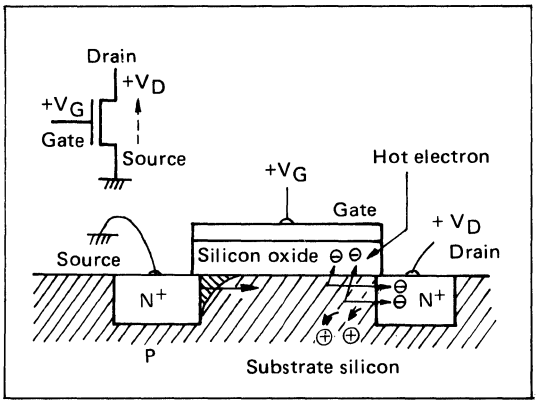
6) Alpha-Particle Soft Failure

This problem occurs when devices are highly miniaturized, such as in 64-kilobit RAMs. The inversion of memory cell data by alpha-particle generated by radioactive elements like uranium and thorium (present in minute quantities, measured in ppb) in the ceramic package material causes defects. Since failure is only temporary and normal operation restored quickly, this is referred to as a "soft" failure. At Oki Electric we have eliminated the problem by coating the chip surface of 64-kilobit RAMs with a resin which effectively screens out these alpha-particle.



7) Degradation in Performance Characteristics Due to Hot Electrons

With increased miniaturization of circuit elements, internal electric field strength in the channels increases since the applied voltage remains the same at 5 V. As a result, electrons flowing in the channels, as shown in the accompanying diagram, tend to enter into the oxide film near the drain, leading to degradation of performance. Although previous low-temperature operation tests have indicated an increase of this failure, we have confirmed by our low-temperature acceleration tests, including checks on test element groups, that no such problem exists in Oki LSIs.



Characteristic deterioration caused by hot electron

With further progress in the miniaturization of circuit components, failures related to pin hole oxide film destruction and photolithography have increased. To eliminate these defects during manufacturing, we at Oki Electric have been continually improving our production processes based on reliability tests and information gained from the field. And we subject all devices to high-temperature burn-in screening for 48 to 96 hours to ensure even greater reliability.

MOS MEMORY HANDLING PRECAUTIONS

MOS MEMORY HANDLING PRECAUTIONS

1. Static Electricity Countermeasures

Since voltage is generally controlled by means of the transistor gate oxide film in MOS memories, the input impedance is high and the insulation tends to be destroyed more readily by static electricity.

Although Oki MOS memories incorporate built-in protector circuits to protect all input terminals from such destruction, it is not considered possible to give complete protection against heat destruction due to overcurrents and insulation film destruction due to irregular high voltages. It is, therefore, necessary to observe the following precautionary measures.

1) Under no circumstances must voltages or currents in excess of the specified ratings be applied to any input terminal.
2) Always use an electrically conductive mat or shipping tubes for storage and transporting purposes.
3) Avoid wearing apparel made of synthetic fiber during operations. The wearing of cottons which do not readily generate static electricity is desirable. Also avoid handling devices with bare hands. If handling with bare hands cannot be avoided, make sure that the body is grounded, and that a 1MΩ resistor is always connected between the body and ground in order to prevent the generation of static electricity.
4) Maintaining the relative humidity in the operation room at 50% helps to prevent static electricity. This should be remembered especially during dry seasons.
5) When using a soldering iron, the iron should be grounded from the tip. And as far as possible, use low power soldering irons (12 V or 24 V irons).

2. Power Supply and Input Signal Noise

2.1 Power supply noise absorption

In dynamic memories, the flow of power supply current differs greatly between accessing and standby modes.

Although very little power is consumed by CMOS memories during standby mode, considerable current is drawn for charging and discharging (instantaneous current requirements) during access mode. In order to absorb the "spike noise" generated by these current requirements, the use of relatively large capacitance capacitors (about one 10μF capacitor for every 8 to 10 RAMs) is recommended along with good high frequency response capacitors of about 0.1μF for each memory element. Power line wiring with as little line impedance as possible is also desirable.

2.2 Input signal noise absorption

Overshooting and undershooting of the input signal should be kept to a bare minimum. Undershooting in particular can result in loss of cell data stability within the memory. For this reason,

(1) Avoid excessive undershooting when using an address common bus for memory board RAMs and ROMs.
(2) Since noise can be generated very easily when using direct drive for applying memory board RAM addresses from other driver boards, it is highly recommended that these addresses be first received by buffer.
(3) Methods available for eliminating undershooting generated in the address line include
   a) Clamping of the undershooting by including a diode.
   b) Connect 10~20Ω in series with driver outputs.
   c) Smooth the rising edge and falling edge waveforms.

3. CMOS Memory Operating Precautions

3.1 Latch-Up

If the CMOS memory input signal level exceeds the Vcc power line voltage by +0.3 V, or drops below the ground potential by −0.3 V, the latch-up mechanism may be activated. And once this latch-up mode has been activated, the memory power has to be switched off before normal operating mode can be restored. Destruction of the memory element is also possible if the power is not switched off.

Although Oki CMOS memories have been designed to counter these tendencies, it is still recommended that input signal overshooting and undershooting by avoided.

3.2 Battery Back-Up

Take special note of the following 4 points when designing battery back-up systems.

(1) Do not permit the input signal H level to exceed Vcc +0.3 V when the memory Vcc power is dropped. To achieve this, it is recommended that a CMOS driver using a Vcc power common with the CMOS memory, or an open collector buffer or open drain buffer pulled-up by a Vcc power common with the CMOS memory be used for driving purposes.
(2) Set the chip select input signal CE to the same H level as the CMOS memory Vcc power line. And in order to minimize memory power consumption, set the write enable input $\overline{WE}$ level, the address input and the data input to either ground level or to the same H level as the CMOS memory Vcc power line.
(3) Make sure that the CMOS memory Vcc power line is increased without "ringing" or temporary breaks when restoring the battery back-up mode.
(4) When using synchronous type CMOS memories (MSM5115, MSM5104), make sure that accessing occurs after elapse of the chip enable off time (t_{CC}) prescribed in the catalog after the Vcc power line has reached the guaranteed operating voltage range.

For further details, refer to "CMOS Memory Battery Back-up" at the end of this manual.

EPROM WRITING AND ERASURE

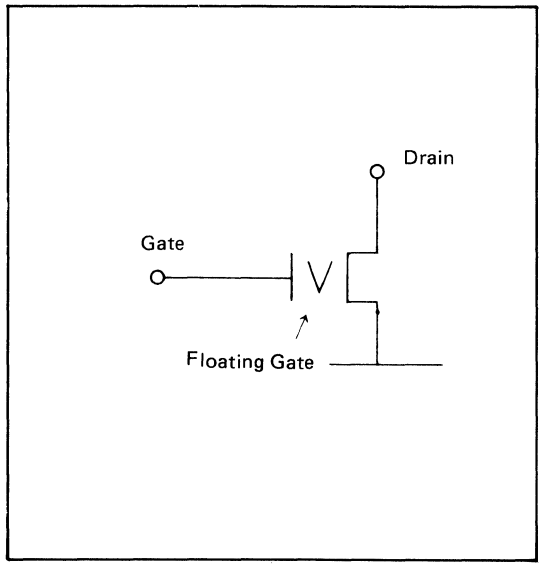
5

EPROM WRITING AND ERASURE

1. EPROM Writing Erasure

1.1 EPROM MSM2716/2764 writing

Writing in the MSM2716AS involves setting the drain and gate voltages of the floating gate stage to a high voltage. When the drain voltage exceeds 15 V and the gate voltage 20 V, the channel charge (electrons) becomes highly energized and flow over the oxide film barrier into the floating gate. And since the high gate voltage is positive polarity, electrons will flow into the floating gate very easily. When electrons build up in the floating gate, the memory element "threshold voltage" is changed, and subsequently stored as memory data. Once the charge has been built up, the surrounding oxide film (high insulation) prevents escape of electrons. The data is thus stored as "non-volatile" data.



When the MSM2716AS is shipped from the factory, the floating gate is left in discharged status (all bits "1"), i.e. "blank" status. During writing processes, +25 V is applied to the Vpp terminal and V_{IH} to the $\overline{OE}$ input. The data to be programmed is applied in parallel to the outputs ($O_0 - 7$). After the address and data have been set up, application of V_{IH} level for 50 ms to the $\overline{CE}$ input will enable writing of data. Since the +25 V applied to Vpp is fairly close to the element's withstanding voltage, make sure that the voltage setting is maintained strictly within the 25 V ±1 V range. Application of voltages in excess of the rated voltage, and overshooting, to the Vpp terminal can result in permanent damage to the element.

Although MSM2716AS rewriting should be checked about 100 times by sample testing, in actual practice 5 to 10 times is usually the limit. This will not likely result in any problem.

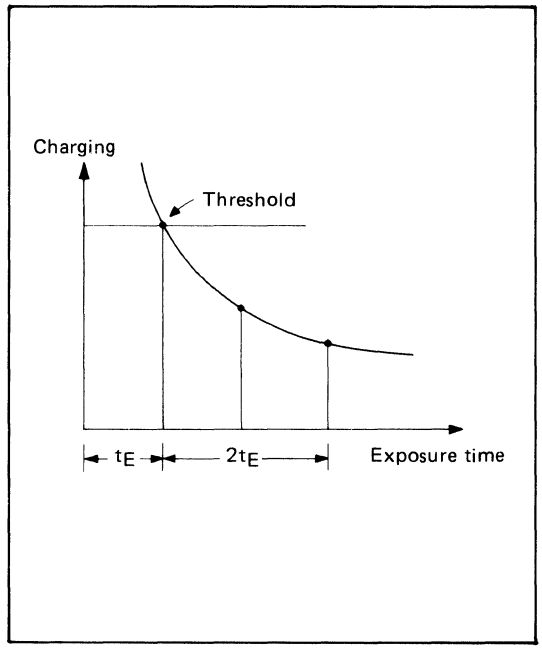
1.2 PROM programmer

Oki Electric employs a system whereby the various programmer available on the market are examined, and agreements reached with different programmer manufacturers. The purpose of this system is to check compatibility between programmer manufacturers and Oki Electric devices, and making modifications whenever required. Users are thus ensured trouble-free use.

In the event of EPROM trouble with Oki devices and approved programmer, problems will be handled by both Oki and driver manufacturer except where such problems have been caused purposely.

1.3 Erasure

Erasure of data written in the MSM2716AS can be effected by ultra-violet radiation of the memory element. In this case, the charge is discharged into the substrate or electrode by the ultra-violet energy, but note that the following erasure conditions must be met. If a memory which has not been properly erased is used, writing problems and operating failures are likely to arise. Also note that excessively long erasure times (of several hours duration) can also result in failure.



Lengthy exposure to direct sunlight can also result in loss of bits. Direct exposure of MSM2716 to the strong summer sun for a single day can result in bit changes. Although normal fluorescent lights have practically no effect, light rays beamed onto elements can cause special changes. It is therefore recommended that the glass face be covered with a screening label.

2. EPROM Handling

2.1 Defects caused by static electricity

The generation of static electricity on the EPROM glass face can result in changes in the memory contents. This, however, can be restored by brief exposure (several seconds) to ultra-violet radiation. But this exposure must be kept short. Exposure for 30 seconds or more can cause changes in the normal bits.

2.2 Handling precautions

(1) Avoid carpets and clothes etc where static electricity is generated.
(2) Make sure the programmer and mounting system are securely grounded.
(3) Also make sure that any soldering iron employed is properly grounded.
(4) Always carry in an electrically conductive plastic mat.
(5) Written ROMs are also to be kept in an electrically conductive plastic mat.
(6) Do not touch the glass seal by hand since this can result in deterioration of the ultra-violet permeability required for erasure, and subsequently lead to poor erasure.

2.3 System debugging precautions

During system debugging, check operations with a voltage of ±5% (oscillating).

MASK ROM CUSTOMER PROGRAM SPECIFICATIONS

MASK ROM CUSTOMER PROGRAM SPECIFICATIONS

The mask ROM custom program code programming method is outlined below.

1. Usable media

(1) Magnetic tape
(2) EPROM

Magnetic tape and EPROM are used as standard (with MSM2916 and MSM2932 employing only EPROM).

2. Magnetic tape specifications

2.1 Use the following types of magnetic tape in magnetic tape units compatible with IBM magnetic tape units.

(1) Length: 2400 feet, 1200 feet or 600 feet
(2) No label
(3) Width: 1/2 feet
(4) Channels: 9 channels
(5) Bit density: 800BPI standard, although 1600BPI can also be employed.
(6) Block size: Integer multiples of 256 bytes possible with 256 bytes as standard. 1 block, 1 record is standard.

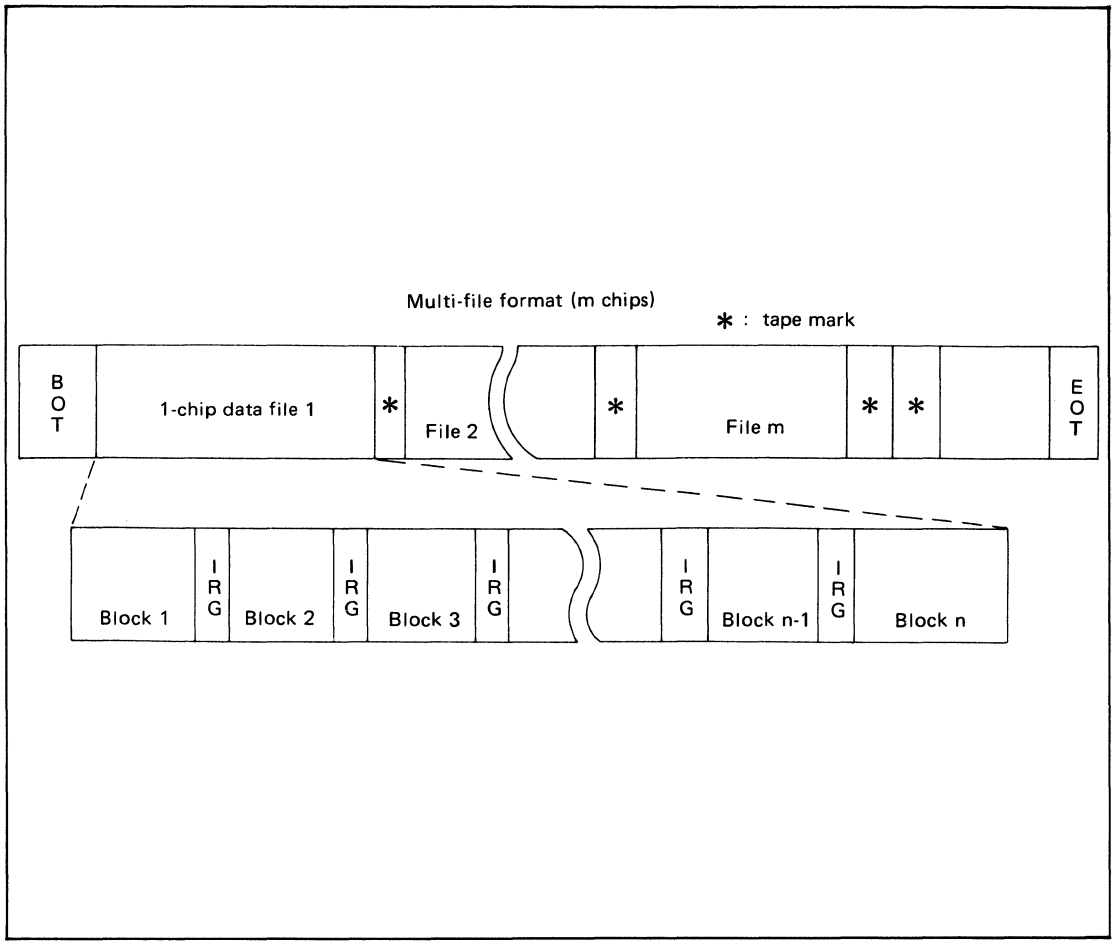
2.2 Magnetic tape format

(1) The data for a single chip should not extend into several tapes. Data for several chips are allowed to be included in a single magnetic tape, multiple file format being permitted. In this case, include the data of a single chip in one file.
(2) Use tape marks for file partitions when employing multiple file formats.
(3) Denote the completion of a magnetic tape file by two successive tape marks.

2.3 Magnetic tape data format

(1) The data contained in a single file on magnetic tape must be inserted from the head address $(0000)_{hex}$ of the device up to the final address in succession for a single chip.
(2) In this case, the LSB of the data should correspond to D_0, and the MSB to D_7.
(3) "1" bits in the data denote high device output, while "0" denotes low output.

2.4 Magnetic tape examples



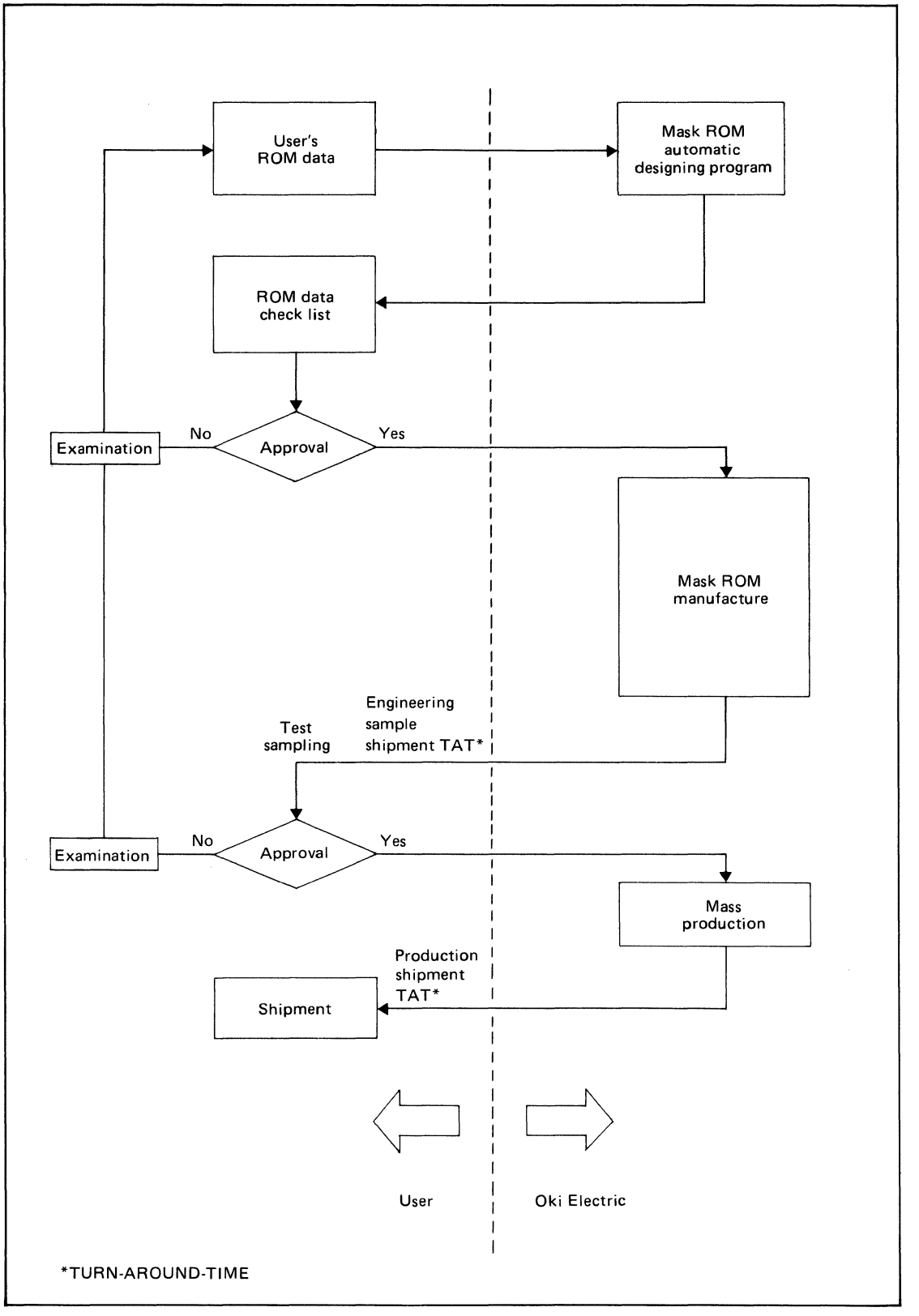
3. EPROM Specifications

(1) MSM2716, MSM2764, Intel 2716, 2732, 2764 or equivalent device may be used.

(2) Prepare 2 EPROMs containing identical data.

MASK ROM DEVELOPMENT FLOWCHART

MASK ROM DEVELOPMENT FLOWCHART



7

TERMINOLOGY AND SYMBOLS

TERMINOLOGY AND SYMBOLS

1. Pin Terminology

Term	EPROM	ROM	Static RAM	Dynamic RAM
Power supply voltage pin	V_{DD}, V_{CC} V_{GG}, V_{BB}	V_{CC}	V_{CC}	V_{DD}, V_{CC} V_{BB}
Address input pin	$A_0 \sim A_{12}$	$A_0 \sim A_{13}$	$A_0 \sim A_{11}$	$A_0 \sim A_7$
Data input pin			DI	D IN
Data output pin	$O_0 \sim O_7$	$D_0 \sim D_{15}$	DO	D OUT
Data input/output pin			$I/O_1 \sim I/O_8$	
Chip enable pin	CE	CE	CE	
Output enable pin	OE	OE	OE	
Address enable pin		AE		
Chip select pin	CS		CS	
Write enable pin	WE		WE	$\overline{WE}$
Row address strobe pin				$\overline{RAS}$
Column address strobe pin				$\overline{CAS}$
Program input pin	Program, V_{PP}			
Data valid pin		DV		
Clock input pin		ϕT		
Ground pin	V_{SS}	V_{SS}	V_{SS}	V_{SS}
Vacant terminal	NC	NC		

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2. Absolute Maximum Ratings

Term	EPROM	ROM	Static RAM	Dynamic RAM
Power supply voltage	V_{DD}, V_{CC} V_{GG}, V_{BB} V_{SS}	V_{CC} V_{SS}	V_{CC} V_{SS}	V_{DD}, V_{CC} V_{BB} V_{SS}
Terminal voltage	V_T		V_T	V_T
Input voltage	V_I	V_I	V_I	V_I
Output voltage	V_O	V_O	V_O	V_O
Input current				
Output current			I_O	
Output shorting current				I_{OS}
Load capacitance				
Permissible loss	P_D	P_D	P_D	P_D
Operating temperature	Topr	Topr	Topr	Topr
Storage temperature	Tstg	Tstg	Tstg	Tstg

3. Recommended Operation Conditions

Term	EPROM	ROM	Static RAM	Dynamic RAM
Power supply voltage	V_{DD}, V_{CC} V_{GG}, V_{BB} V_{SS}	V_{CC} V_{SS}	V_{CC} V_{SS}	V_{DD}, V_{CC} V_{BB} V_{SS}
"H" clock input voltage				V_{IHC}
"H" input voltage	V_{IH}	V_{IH}	V_{IH}	V_{IH}
"L" input voltage	V_{IL}	V_{IL}	V_{IL}	V_{IL}
Data storage voltage			V_{CCH}	
Load capacitance		C_L	C_L	
Fan-out	N	N	N	
Operating temperature	Topr	Topr	Topr	Topr

4. DC Characteristics

Term	EPROM	ROM	Static RAM	Dynamic RAM
"H" output voltage	V_{OH}	V_{OH}	V_{OH}	V_{OH}
"L" output voltage	V_{OL}	V_{OL}	V_{OL}	V_{OL}
"H" output current			I_{OH}	
"L" output current				
Input leak current	I_{LI}	I_{LI}	I_{LI}	I_{LI}
Output leak current	I_{LO}	I_{LO}	I_{LO}	I_{LO}
I/O leak current			I_{LO}	
Program terminal current	I_{PP1}, I_{PP2}			
Peak power on current		I_{PO}	I_{PO}, I_{SBP}	
Power supply current	I_{DD}, I_{CC} I_{BB}, I_{CC1} I_{CC2}	I_{CC}, I_{CCS} I_{CCA}	I_{CC}, I_{CCA} I_{CC1}, I_{CC2} I_{CCS}, I_{CCS1} I_{SB}	I_{DD1}, I_{CC1}, I_{BB1} I_{DD2}, I_{CC2}, I_{BB2} I_{DD3}, I_{CC3}, I_{BB3} I_{DD4}, I_{CC4}, I_{BB4}

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5. AC Characteristics

(1) Read cycle

Term	EPROM	ROM	Static RAM	Dynamic RAM
Read cycle time		t_C, t_{RC}, t_{CYC}	t_{RC}	t_{RC}
Address access time	t_{ACC}	t_{AA}, t_{ACC}	t_A, t_{AC}, t_{ACC}, t_{AA}	
Chip select access time	t_{CO}	t_{CS}	t_{CO}, t_{ACS1}, t_{ACS2}	
Chip enable access time	t_{CE}	t_{ACE}	t_{AC}	
Output enable access time	t_{OE}	t_{CO}	t_{OE}	
Output setting time		t_{LZ}	t_{CX}, t_{LZ}	
Output valid time	t_{OH}	t_{OH}	t_{OH}, t_{OHA}	
Output disable time	t_{DF}	t_{HZ}	t_{OTD}, t_{HZ}, t_{OFF}	t_{OFF}
Address set-up time		t_{AS}	t_{AS}	
Address hold time		t_{AH}	t_{AH}	
Chip enable off time			t_{CC}	
Chip enable pulse width			t_{CE}	
Power-up time		t_{PU}	t_{PU}	
Power-down time		t_{PD}	t_{PD}	
Address enable pulse width		t_{AE}		
Data valid access time		t_{VA}		
Data valid delay time		t_{VD}		
Clock delay time		t_{VH}		
Clock pule width		t_H		
Clock delay time		t_L		
Output delay time		t_{DD}		
Output access time		t_{DA}		
Output hold time		t_{DH}		
Address enable set-up time		t_{AES}		

(2) Write Cycle

Term	EPROM	ROM	Static RAM	Dynamic RAM
Write cycle time			t_{WC}	t_{WC}
Address set-up time	t_{AS}		t_{AS}, t_{AW}	
Write pulse width	t_{PW}		t_{W}, t_{WP}	t_{WP}
Write recovery time			t_{WR}	
Data set-up time	t_{DS}		t_{DS}, t_{DW}	t_{DS}
Data hold time	t_{DH}		t_{DH}	t_{DH}
Output off time	t_{DF}		t_{OTW}, t_{WZ}	t_{OFF}
Chip select set-up time	t_{CSS}		t_{CW}	
Address hold time	t_{AH}		t_{AH}, t_{WR}	
Chip enable off time			t_{CC}	
Chip enable pulse width			t_{CW}, t_{CE}	
Write enable set-up time			t_{WS}	
Write enable read time			t_{WCL}	
Write enable hold time			t_{WH}	
Address/write enable setting time			t_{AW}	
Write enable output activation			t_{OW}	
Output enable set-up time	t_{OES}			
Output enable hold time	t_{OEH}			
Program read delay time	t_{DPR}			
Output enable delay time	t_{OE}			
Chip enable data valid time	t_{DV}			
Program pulse rising edge time	t_{PRT}			
Program pulse falling edge time	t_{PFT}			
V_{PP} restoration time	t_{VR}			
Chip enable hold time	t_{CH}			

DATA SHEET

MOS DYNAMIC RAMS

MSM3716 AS/RS

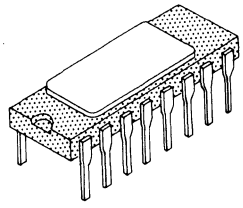
16384 WORD x 1 BIT DYNAMIC RAM (E3-S-001-32)

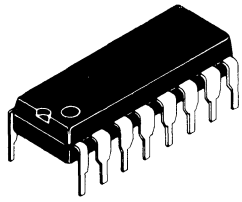
GENERAL DESCRIPTION

The Oki N-MOS integrated circuit MSM3716 AS/RS is an address multiplex type dynamic RAM with a 16,384 word x 1-bit configuration, featuring a wide operational margin and high-speed low power consumption while using a single transistor.

FEATURES

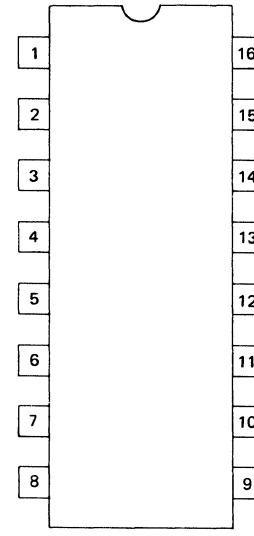
- 16,384 words x 1 bit
- 150ns access time and 375ns cycle time (MSM3716-2AS/RS)
  200ns access time and 375ns cycle time (MSM3716-3AS/RS)
- Standard 16-pin layout
- Low power consumption: 528mW (operation), 20mW (standby)
- Output data controlled by $\overline{CAS}$ only, while system design freedom is increased by not latch at cycle end.
- Read modify write, $\overline{RAS}$ only refresh and page mode operations possible.
- TTL compatible low capacitance for all inputs.
- 128 refresh cycle.





PIN CONFIGURATION

(Top View)



1	V_{BB}	9	V_{CC}
2	D_{IN}	10	A_5
3	$\overline{WRITE}$	11	A_4
4	$\overline{RAS}$	12	A_3
5	A_0	13	A_6
6	A_2	14	D_{OUT}
7	A_1	25	$\overline{CAS}$
8	V_{DD}	16	V_{SS}

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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Conditions	Value	Unit
Power supply voltage	V_{DD}	Respect to Vss	−1.0 ~ +15.0	V
	Vcc		−1.0 ~ +15.0	
	V_{BB}	Respect to Vss V_{DD} − Vss > 0 · 0	0 ~ −20.0	
	V_{DD}	Respect to V_{BB}	−0.5 ~ +20.0	
	Vcc		−0.5 ~ +20.0	
	Vss		−0.5 ~ +20.0	
Input voltage	V_I	Respect to V_{BB}	−0.5 ~ +20.0	
Output voltage	V_O		−0.5 ~ +20.0	
Storage temperature	Tstg		−55 ~ +150	°C
Permissible loss	P_D		1	W

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Conditions	Recommended Operating Conditions			Unit
			Min.	Typ.	Max.	
Power supply voltage	V_{DD}	Vss = 0	10.8	12.0	13.2	V
	V_{CC}		4.5	5.0	5.5	
	V_{BB}		−4.5	−5.0	−5.5	
"H" clock input voltage (note 1)	V_{IHC}		2.7		6.0	
"H" input voltage (note 2)	V_{IH}		2.4		6.0	
"L" input voltage (note 3)	V_{IL}		−1.0		0.8	
Operating temperature	Topr		0		70	°C

Notes: 1. $\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$ inputs
2. A_0 ~ A_6 and D_{IN} inputs
3. All inputs

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DC CHARACTERISTICS

(V_{DD} = 12.0V±10%, Vcc = 5.0V±10%, V_{BB} = −5.0V±10%, Vss = 0V, Ta = 0~70°C)

Parameter	Symbol	Conditions	Special Ratings		Unit	Note
			Min.	Max.		
Average power supply current during operation	I_{DD1}	t_{RC} = 375 ns		40	mA	4
	I_{CC1}					5
	I_{BB1}			200	μA	
Power supply current during standby mode	I_{DD2}	$\overline{RAS}$ = V_{IHC}		1.5	mA	
	I_{CC2}	D_{OUT} = High Impedance	−10	10	μA	
	I_{BB2}			100	μA	
Refresh power supply current	I_{DD3}	t_{RC} = 375 ns		27	mA	4
	I_{CC3}		−10	10	μA	
	I_{BB3}			200	μA	
Page mode power supply current	I_{DD4}	$\overline{RAS}$ = V_{IL}		29	mA	4
	I_{CC4}	t_{PC} = 225 ns				5
	I_{BB4}			200	μA	
Input leak current	I_{L1}	V_{BB} = −5V $0 \leq V_I < 6.0V$	−10	10	μA	
Output leak current	I_{LO}	D_{OUT} = Disable $0 \leq V_O \leq 5.5V$	−10	10	μA	
"H" output voltage	V_{OH}	I_O = −5 mA	2.4		V	
"L" output voltage	V_{OL}	I_O = 4.2 mA		0.4	V	

Notes: 4. I_{DD1}, I_{DD3} and I_{DD4} depend on cycle time.
5. I_{CC1} and I_{CC4} are changed by output load. Vcc is connected to D_{OUT} at low impedance during reading of "H" level data.

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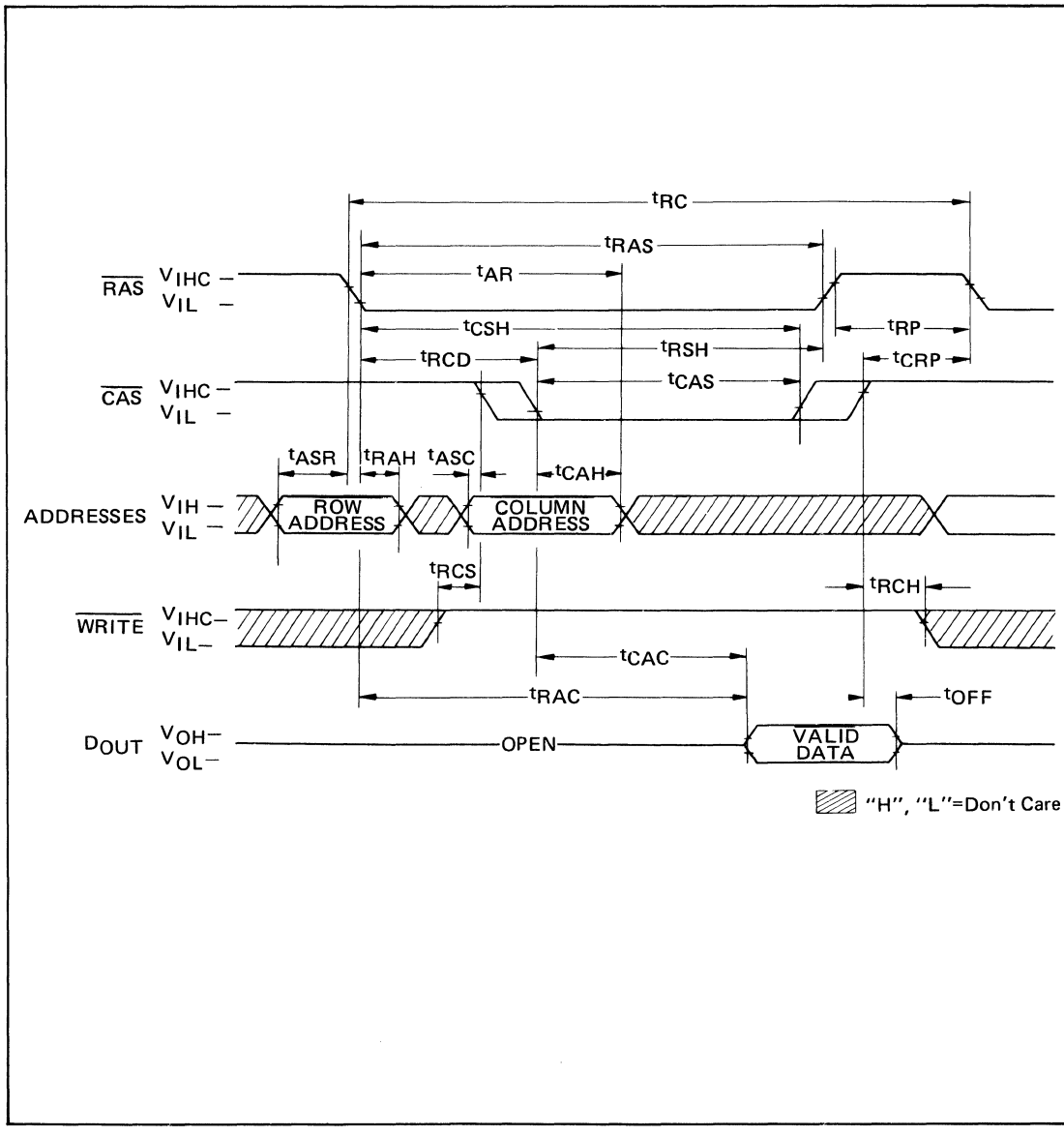
AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(V_{DD} = 12.0V±10%, Vcc = 5.0V±10%, V_{BB} = −5V±10%, Vss = 0V, Ta = 0~70°C) (Notes; 6, 7. 8)

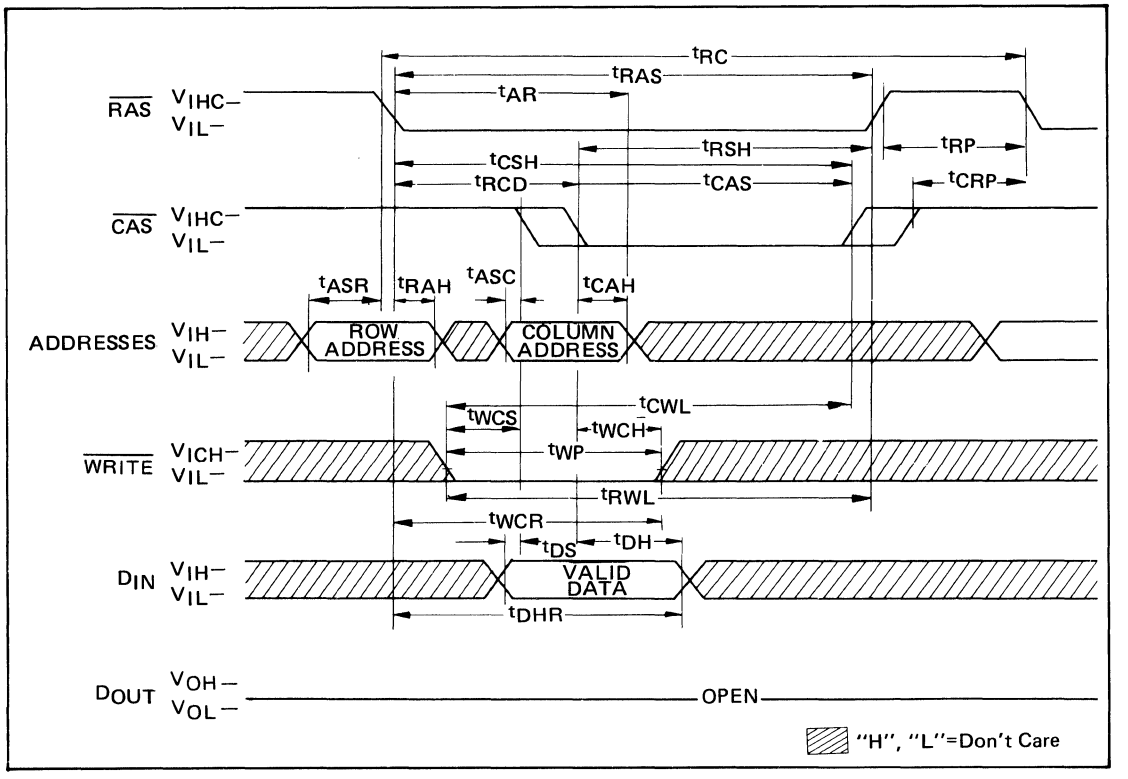
Parameter	Symbol	MSM3716-2AS/RS		MSM3716-3AS/RS		Units	Note
		Min.	Max.	Min.	Max.		
Random read/write cycle time	t_{RC}	375		375		ns	
Read and write cycle time	t_{RWC}	375		375		ns	
Page mode cycle time	t_{PC}	170		225			
Access time from $\overline{RAS}$	t_{RAC}		150		200		9, 11
Access time from $\overline{CAS}$	t_{CAC}		100		135	ns	10, 11
Output turn-off delay time	t_{OFF}	0	40	0	50	ns	
Rise and fall time	t_T	3	35	3	50	ns	
$\overline{RAS}$ precharge time	t_{RP}	100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	100		135		ns	
$\overline{CAS}$ pulse width	t_{CAS}	100	10,000	135	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	150		200		ns	
$\overline{RAS}$ and $\overline{CAS}$ delay time	t_{RCD}	25	50	30	65	ns	12
$\overline{RAS}$ and $\overline{CAS}$ precharge time	t_{CRP}	−20		−20		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	20		25		ns	
Column address set-up time	t_{ASC}	−5		−5		ns	
Column address hold time	t_{CAH}	45		55		ns	
Column address hold time from $\overline{RAS}$	t_{AR}	95		120		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time	t_{RCH}	0		0		ns	
Write command hold time	t_{WCH}	45		55		ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	95		120		ns	
Write command pulse width	t_{WP}	45		55		ns	
Write command and $\overline{RAS}$ read time	t_{RWL}	60		80		ns	
Write command and $\overline{CAS}$ read time	t_{CWL}	60		80		ns	
Data input set-up time	t_{DS}	0		0		ns	13
Data input hold time	t_{DH}	45		55		ns	13
Input hold time for data from $\overline{RAS}$	t_{DHR}	95		120		ns	
$\overline{CAS}$ precharge time	t_{CP}	60		80		ns	
Write command set-up time	t_{WCS}	−20		−20		ns	14
$\overline{CAS}$ and write command delay time	t_{CWD}	70		95		ns	14
$\overline{RAS}$ and write command delay time	t_{RWD}	120		160		ns	14
Refresh cycle	t_{REF}		2		2	ms	

NOTES: 6. Normal memory operation may not be possible unless at least 8 cycles of operation are performed after the power is switched on.
7. AC measurements when t_T = 5ns.
8. Prescribed timing input levels of V_{IHC} (MIN), V_{IH} (MIN) and V_{IL} (MAX).
9. In the case of $t_{RCD} \leq t_{RCD}$ (MAX); t_{RAC} is increased only for $t_{RCD}-t_{RCD}$ (MAX) for $t_{RCD} > t_{RCD}$ (MAX) case.
10. For $t_{RCD} \geq t_{RCD}$ (MAX) case.
11. For 2TTL + 100pF load case.
12. t_{RCD} (MAX) is the value guaranteed by t_{RAC} (MAX), and when $t_{RCD} > t_{RCD}$ (MAX) it is distributed by t_{CAC}.
13. t_{DS} and t_{DH} are specified by the $\overline{CAS}$ falling edge during the write cycle (early write), and by the $\overline{WRITE}$ falling edge during read modify write cycle.
14. t_{WCS}, t_{CWD} and t_{RWD} are not parameters specifying operational limits.
$t_{WCS} \geq t_{WCS}$ (MIN) results in write cycle (early write) with high impedance output.
$t_{CWD} \geq t_{WCS}$ (MIN) and $t_{RWD} \geq t_{RWD}$ (MIN) result in read modify write cycle.

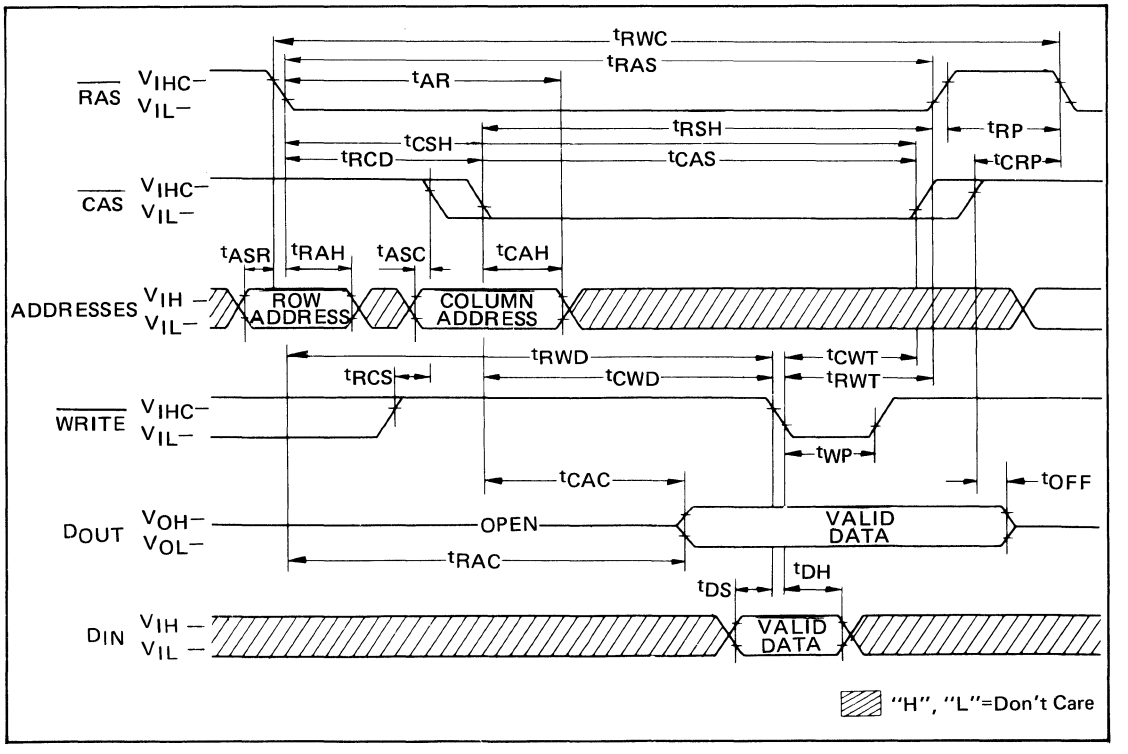
READ CYCLE



WRITE CYCLE (EARLY WRITE)



READ-WRITE/READ-MODIFY-WRITE CYCLE



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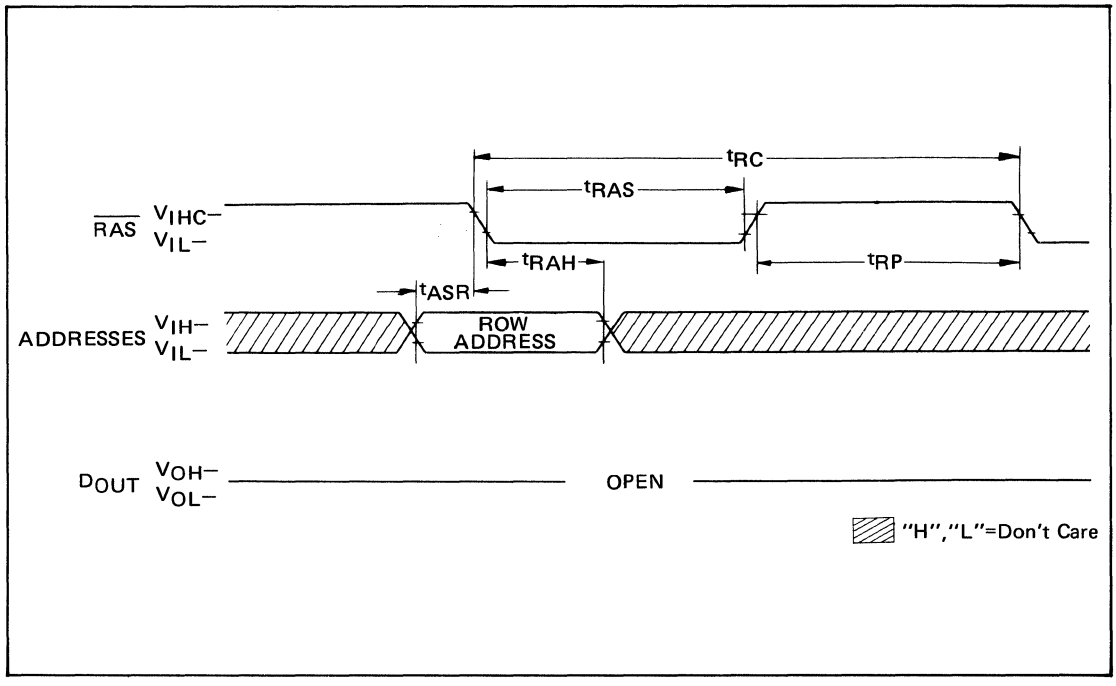
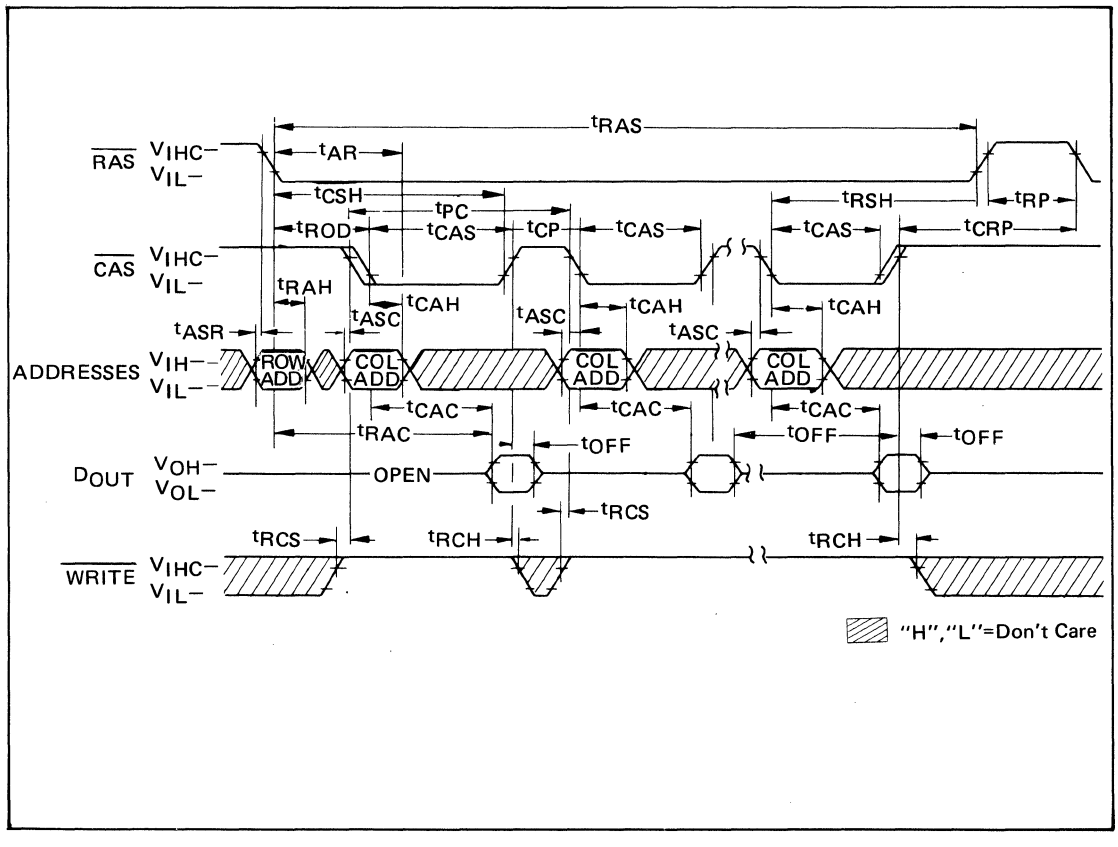
"$\overline{RAS}$-ONLY" REFRESH CYCLE $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care



PAGE MODE READ CYCLE



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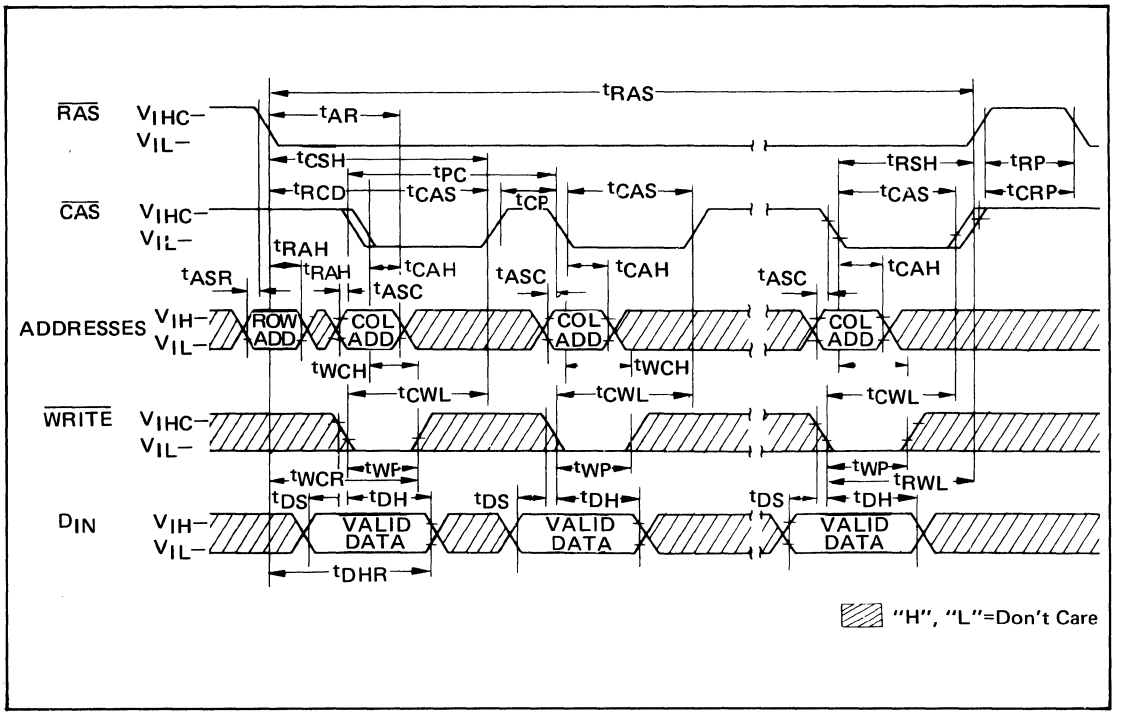
PAGE MODE WRITE CYCLE



TERMINAL CAPACITANCE CHARACTERISTICS

(V_{DD} = 12.0V ± 10%, V_{SS} = 0V, V_{BB} = 5.0V ± 10%, Ta = 0 ~ 70°C)

Parameter	Symbol	Standard	Maximum	Unit	Remarks
Input Capacitance (A_0~A_6, D_{IN})	C_I	4	5		
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{CRITE}$)	C_I	8	10	pF	
Output Capacitance (D_{OUT})	C_O	5	7		$\overline{CAS}$=V_{IHC}

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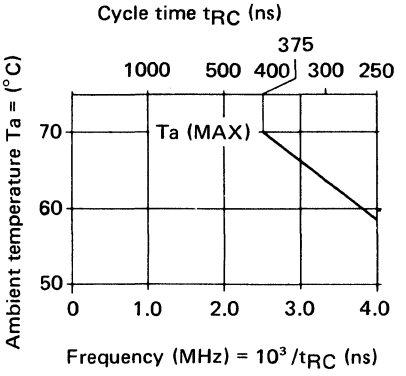
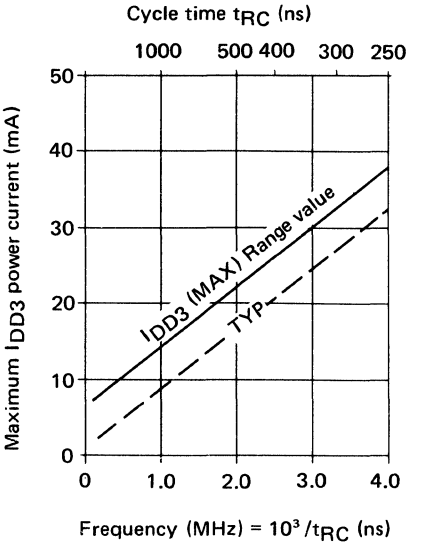
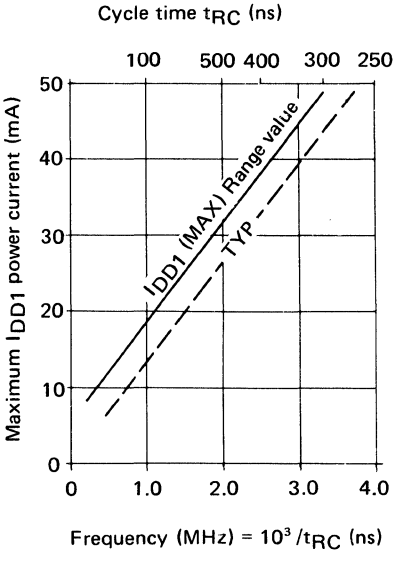
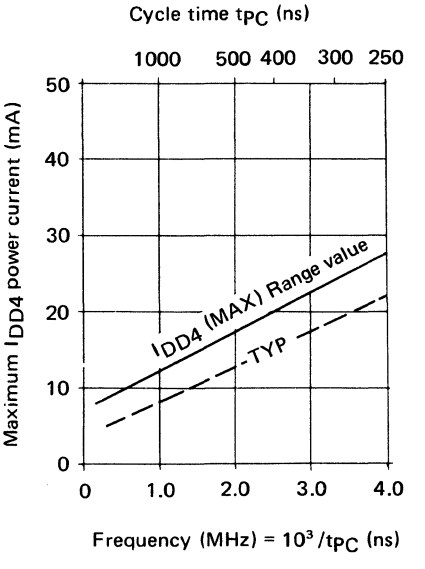
TYPICAL CHARACTERISTICS









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MSM3732 AS/RS

32,768-BIT DYNAMIC RANDOM ACCESS MEMORY (E3-S-002-32)

GENERAL DESCRIPTION

The Oki MSM3732H/L is a fully decoded, dynamic NMOS random access memory organized as 32,768 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

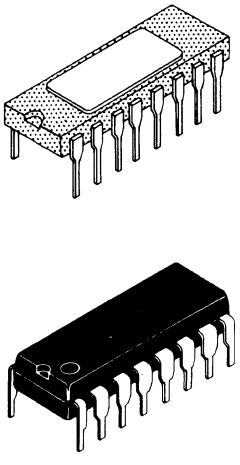
Multiplexed row and column address inputs permit the MSM3732 to be housed in a standard 16 pin DIP.

The MSM3732 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

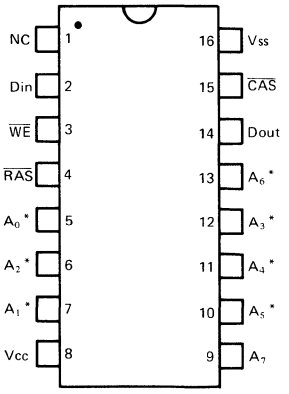
FEATURES

- 32,768 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  150 ns max (MSM3732H/L-15)
  200 ns max (MSM3732H/L-20)
- Cycle time,
  270 ns min (MSM3732H/L-15)
  330 ns min (MSM3732H/L-20)
- Low power: 248 mW active,
  28 mW max standby
- **Single +5V Supply, ±10% tolerance**
- **All inputs TTL compatible, low capacitive load**
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 128 refersh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance



PIN CONFIGURATION

(Top View)



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address

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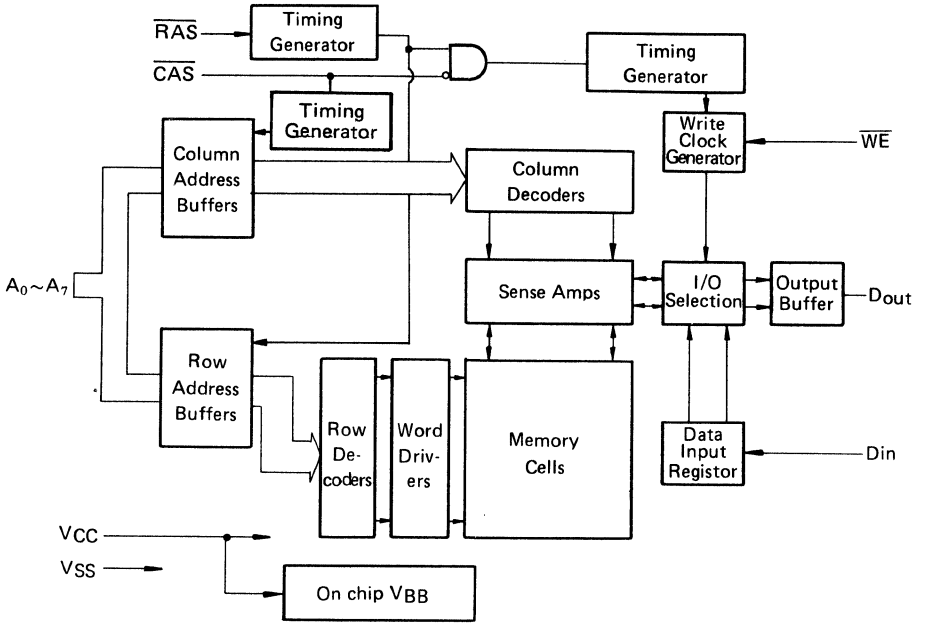
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		45	mA	
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
Refresh Current Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		35	mA	
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		42	mA	
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
Output Levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_7, D_{IN})	C_{IN1}	4.5	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	7	10	pF
Output Capacitance (D_{OUT})	C_{OUT}	5	7	pF

Capacitance measured with Boonton Meter.

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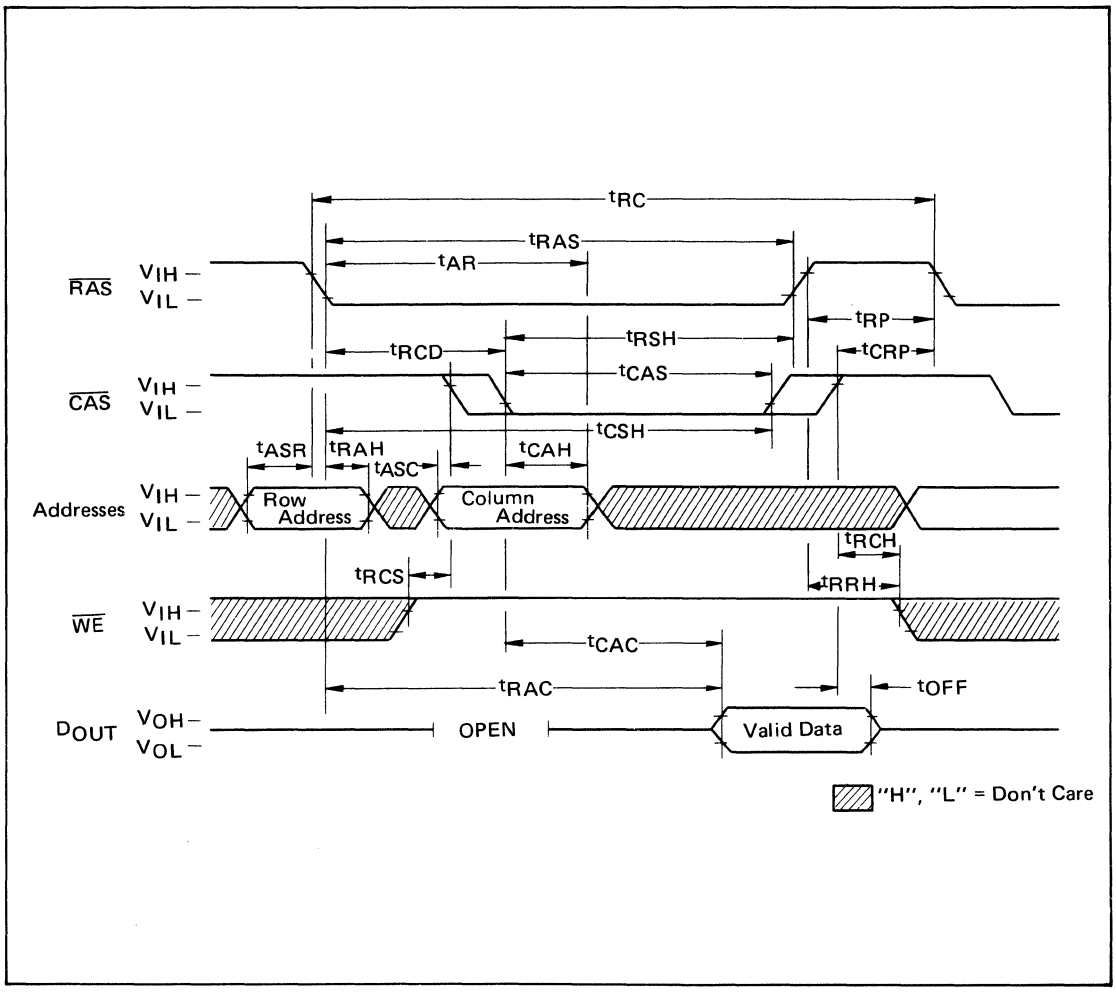
AC CHARACTERISTICS

Notes 1, 2, 3 Under Recommended Operating conditions

Parameter	Symbol	Units	MSM3732-15		MSM3732-20		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2	
Random read or write cycle time	t_{RC}	ns	270		330		
Read-write cycle time	t_{RWC}	ns	270		330		
Page mode cycle time	t_{PC}	ns	170		225		
Access time from $\overline{RAS}$	t_{RAC}	ns		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		100		135	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	50	
Transition time	t_T	ns	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	100		135		
$\overline{CAS}$ precharge time	t_{CP}	ns	60		80		
$\overline{CAS}$ pulse width	t_{CAS}	ns	100	10,000	135	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	20	50	25	65	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	20		25		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	45		55		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	95		120		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		8
Write command hold time	t_{WCH}	ns	45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	95		120		
Write command pulse width	t_{WP}	ns	45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	45		55		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	45		55		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	95		120		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	60		80		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	110		145		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		25		

NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
5) Assumes that $t_{RCD} < t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING



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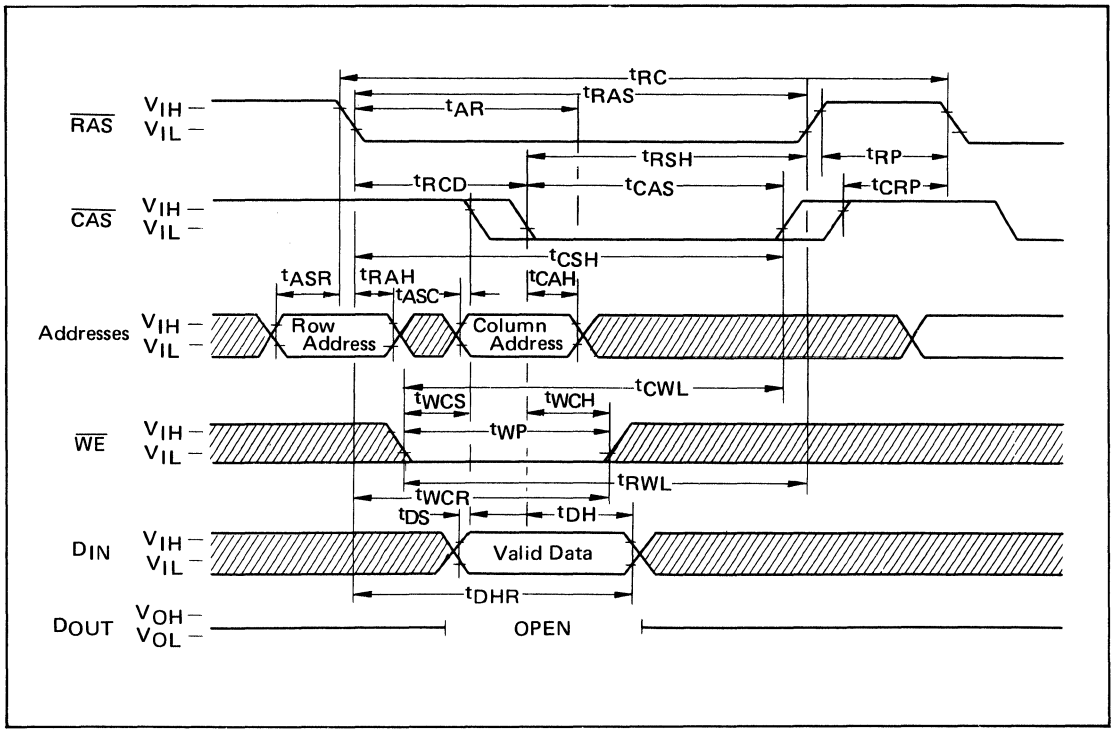
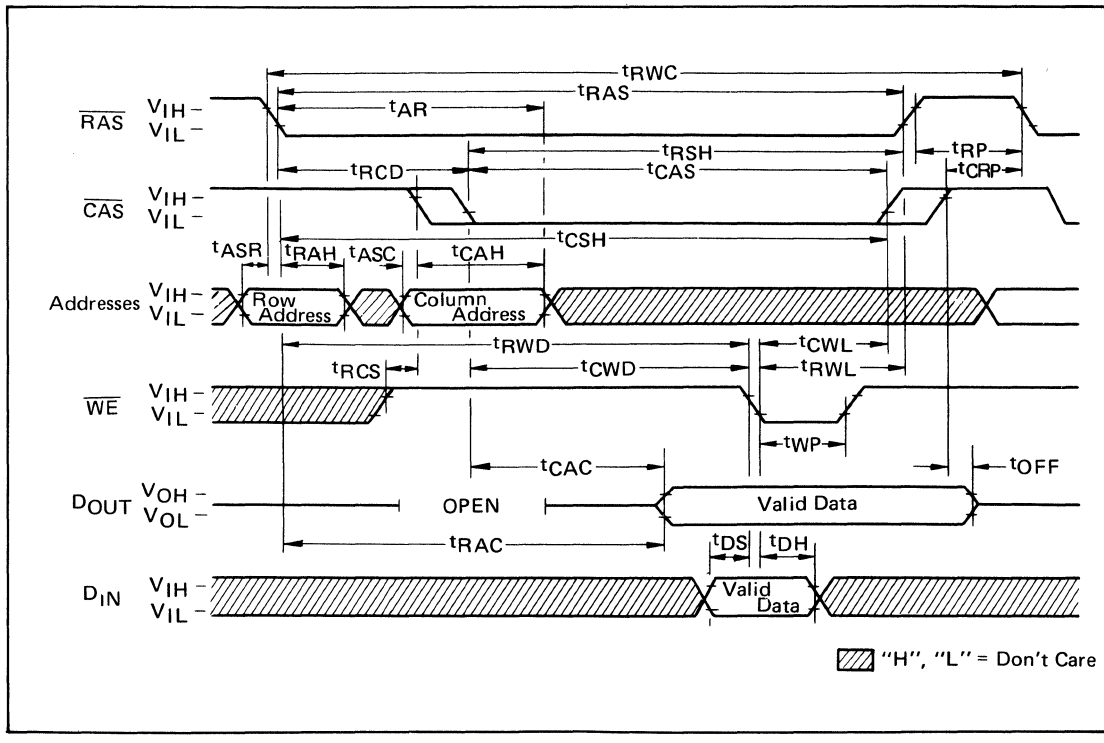
WRITE CYCLE TIMING
(EARLY WRITE)

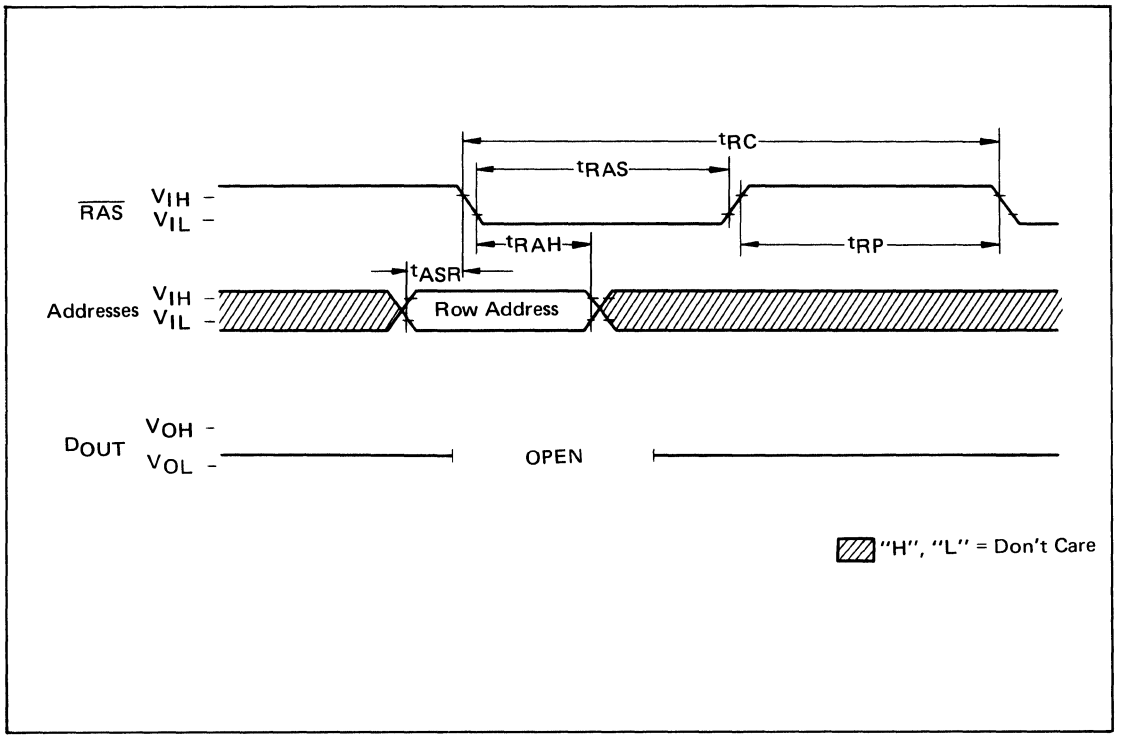


READ-WRITE/READ-MODIFY-WRITE CYCLE

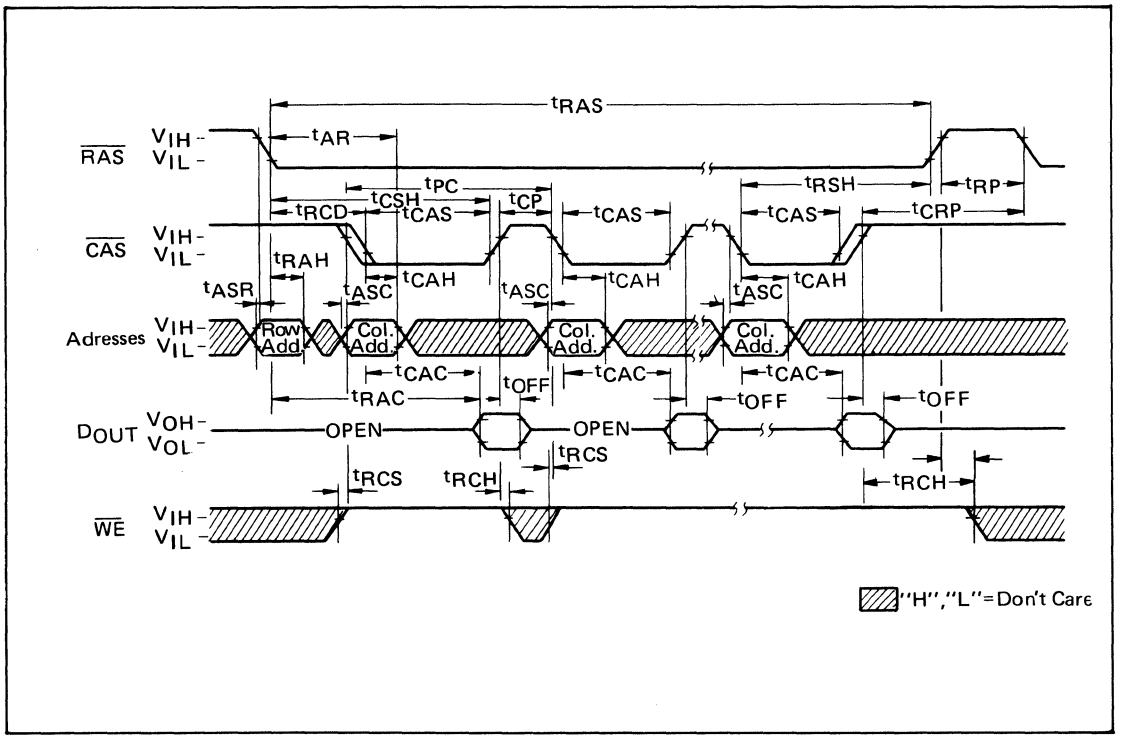


$\overline{RAS}$ ONLY REFRESH TIMING

($\overline{CAS}$: V_{IH}, $\overline{WE}$ & DIN: Don't care)



PAGE MODE READ CYCLE



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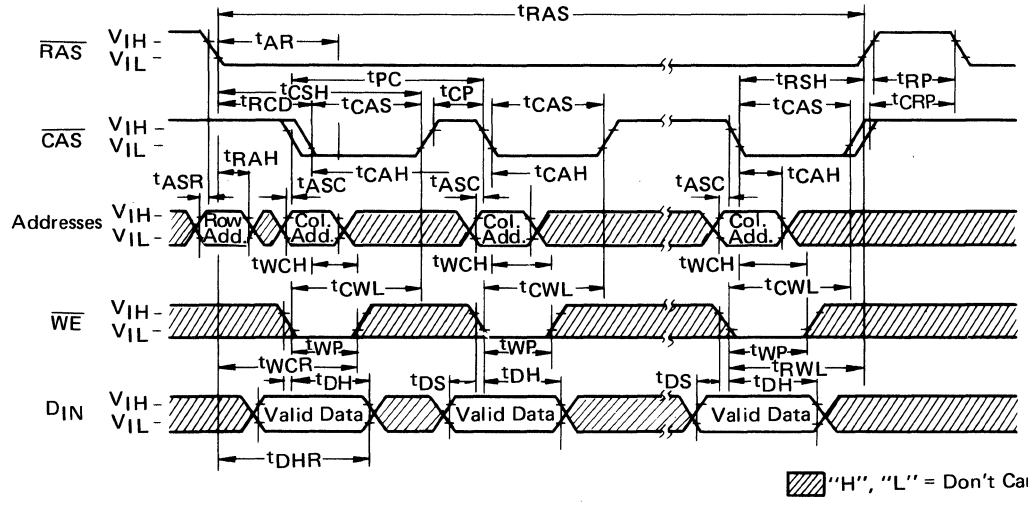
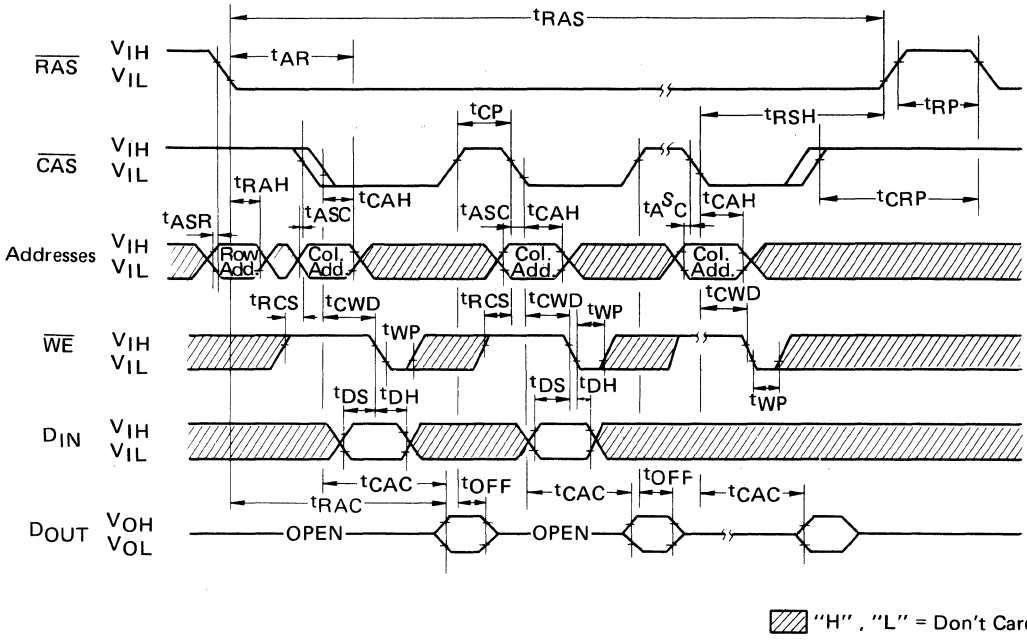
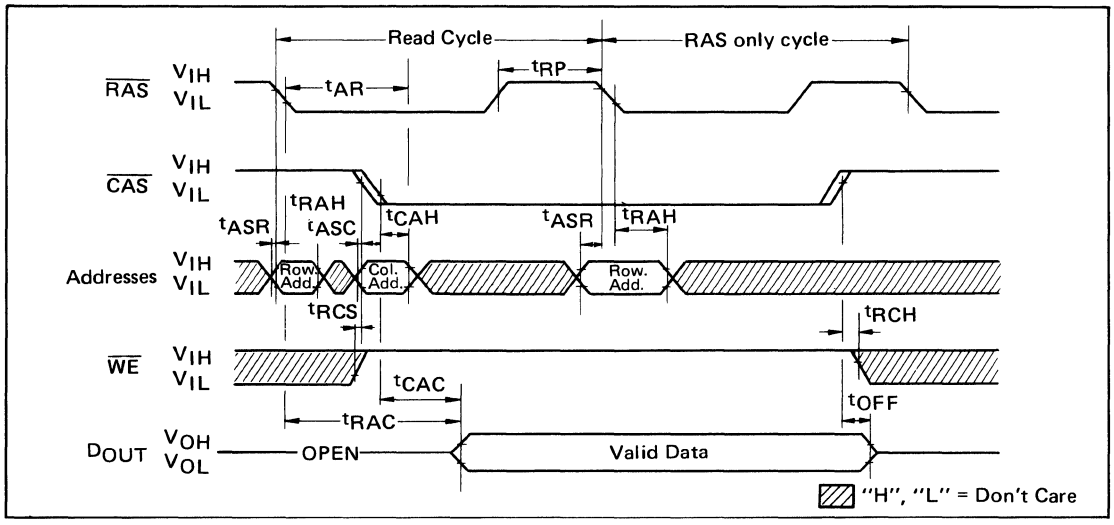
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



HIDDEN REFRFSH



DESCRIPTION

Address Inputs:

A total of fifteen binary input address bits are required to decode any 1 of 32,768 storage cell locations within the MSM3732. Eight row-address bits are established on the input pins (A_0~A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The seven column-address bits (A_0 through A_6) are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

One Column Address (A_7) has to be fixed at logic "0" (low level) for MSM3732L, and at logic "1" (high level) for MSM3732H.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM3732 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transistion. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM3732 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses (A_0~A_6) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each rwo to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

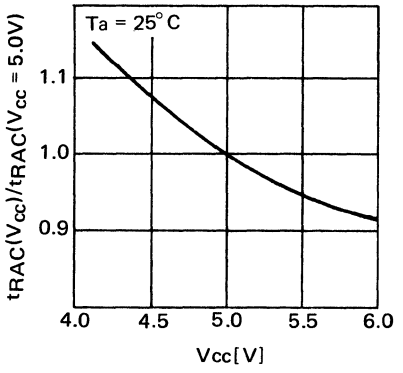
Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

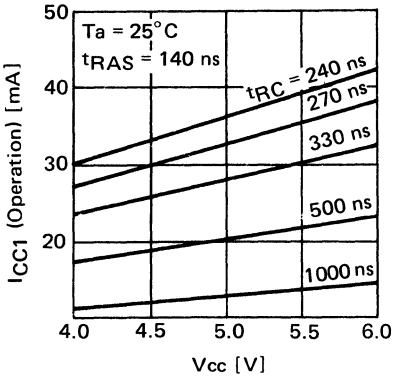
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

TYPICAL CHARACTERISTICS

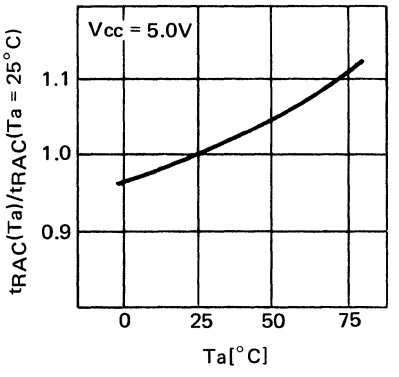
Access time from $\overline{RAS}$
(Relative value) v.s. Vcc



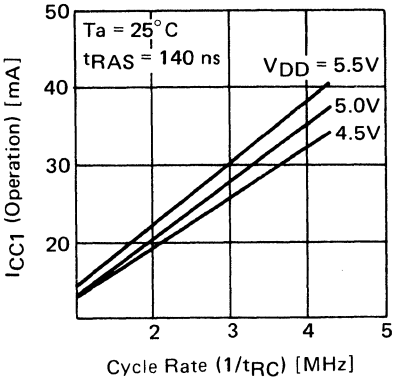
I_{CC1} (t_{RAS}: Constant)
v.s. Vcc



Access time from $\overline{RAS}$
(Relative value) v.s. Ta



I_{CC1} (t_{RAS}: Constant)
v.s. Cycle rate



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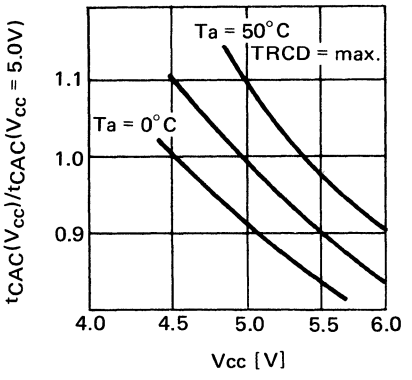
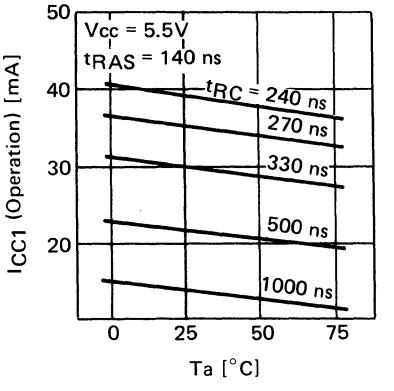
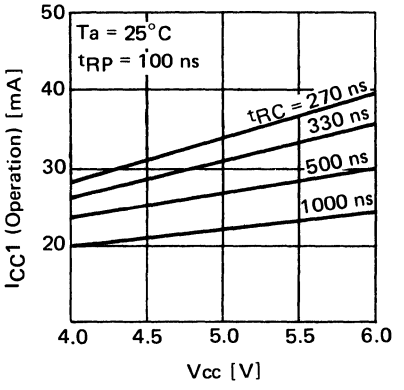
Access time from $\overline{CAS}$
(Relative value) v.s. Vcc



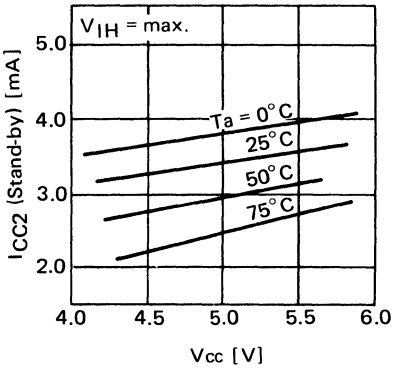
I_{CC1} (t_{RAS}: Constant)
v.s. Ta



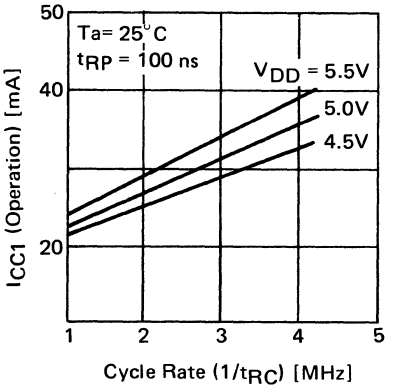
I_{CC1} (t_{RP}: Constant)
v.s. Vcc



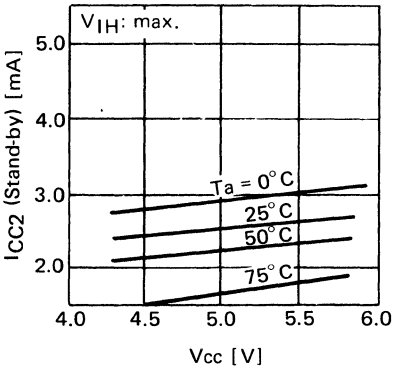
I_{CC2} (MSM3764-12)
v.s. Vcc



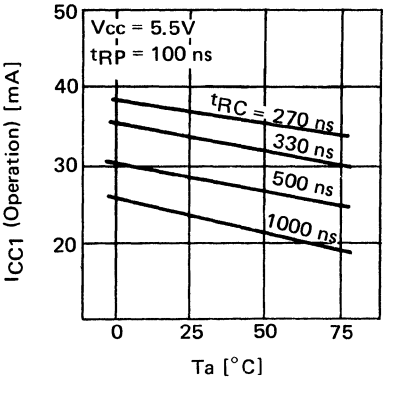
I_{CC1} (t_{RP}: Constant)
v.s. Cycle rate



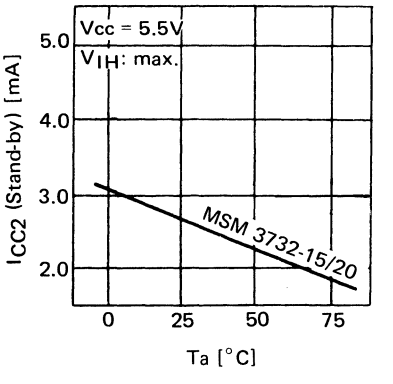
I_{CC2} (MSM3732-15/-20)
v.s. Vcc



I_{CC1} (t_{RP}: Constant)
v.s. Ta



I_{CC2} V.S. Ta



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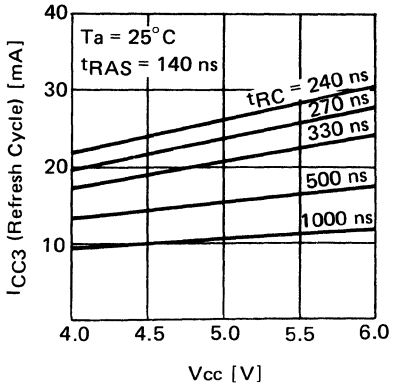
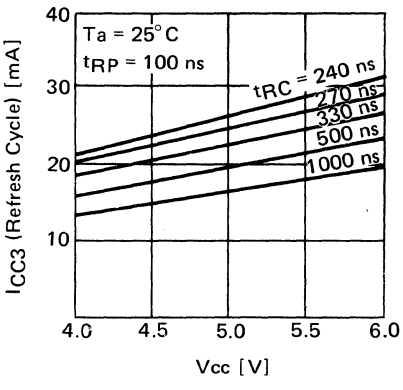
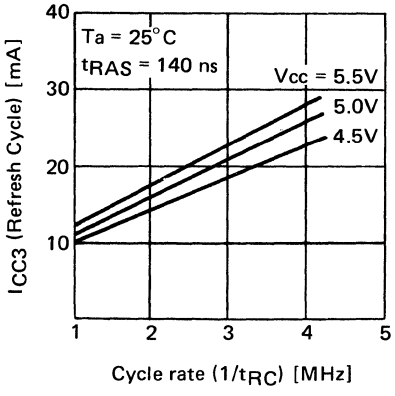
I_{CC3} (t_{RAS}: Constant)
v.s Vcc



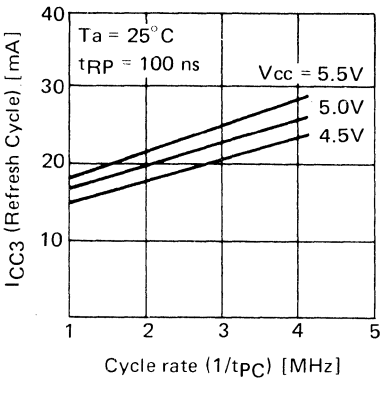
I_{CC3} (t_{RP}: Constant)
v.s. Vcc



I_{CC3} (t_{RAS}: Constant)
v.s. Cycle rate



I_{CC3} (t_{RP}: Constant)
v.s. Cycle rate



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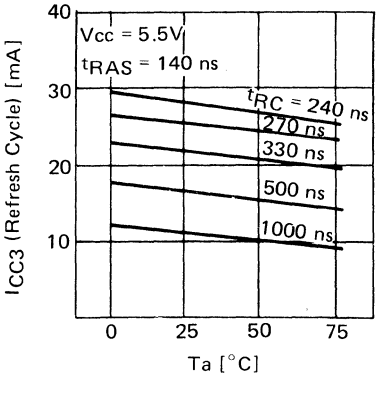
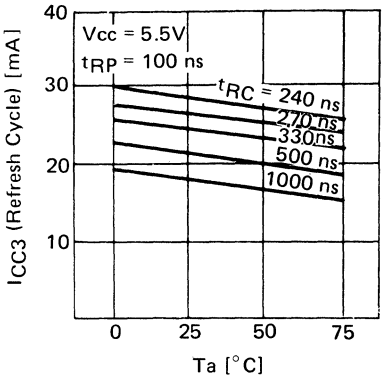
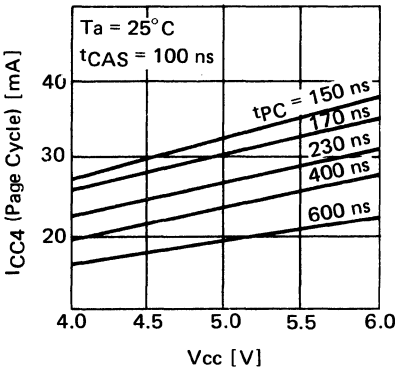
I_{CC3} (t_{RAS}: Constant)
v.s. Ta



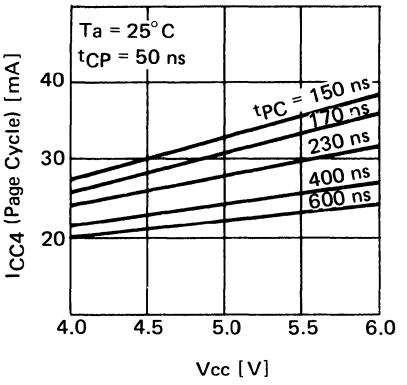
I_{CC3} (t_{RP}: Constant)
v.s. Ta



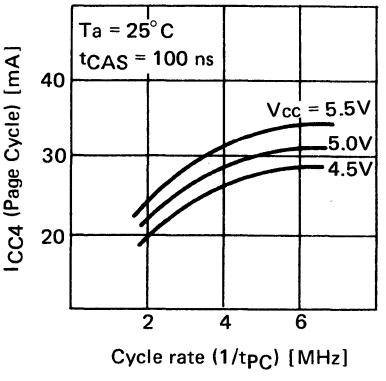
I_{CC4} (t_{CAS}: Constant)
v.s. Vcc



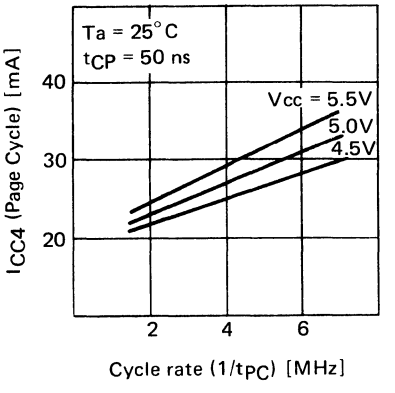
I_{CC4} (t_{CP}: Constant)
v.s. Vcc



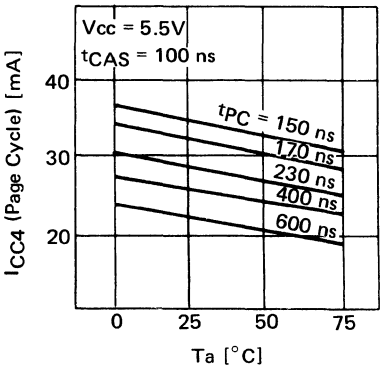
I_{CC4} (t_{CAS}: Constant)
v.s. Cycle rate



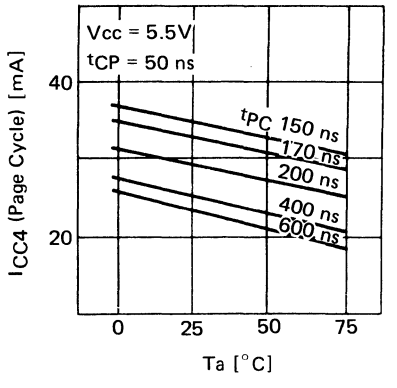
I_{CC4} (t_{CP}: Constant)
v.s. Cycle rate



I_{CC4} (t_{CAS}: Constant)
v.s. Ta

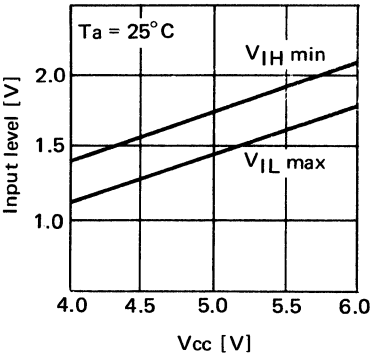


I_{CC4} (t_{CP}: Constant)
v.s. Ta

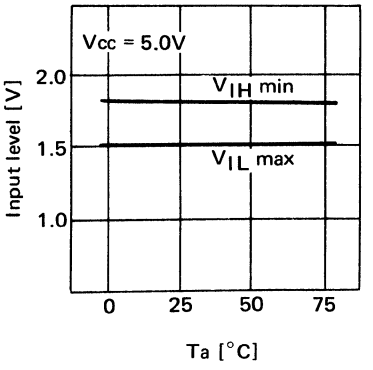


9

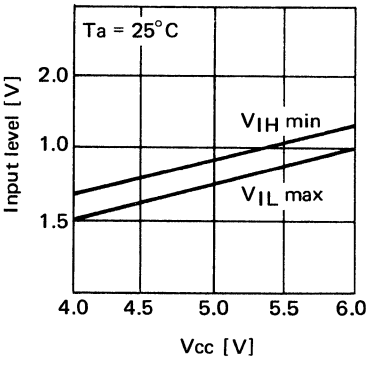
Address Input
v.s Vcc



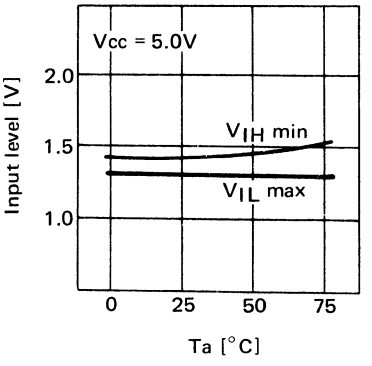
Address Input
v.s. Ta



Data Input
v.s. Vcc

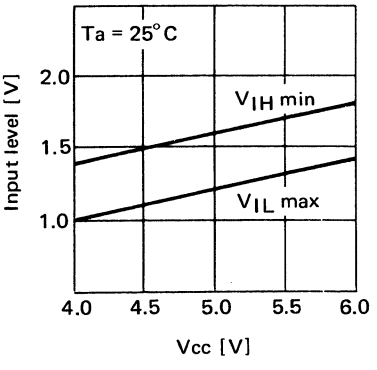


Data Input
v.s. Ta

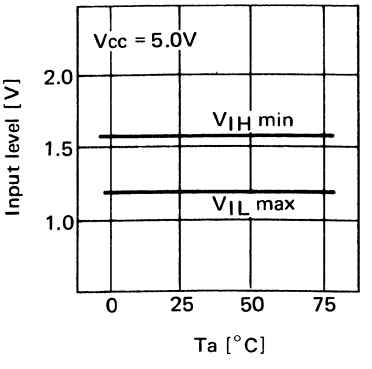


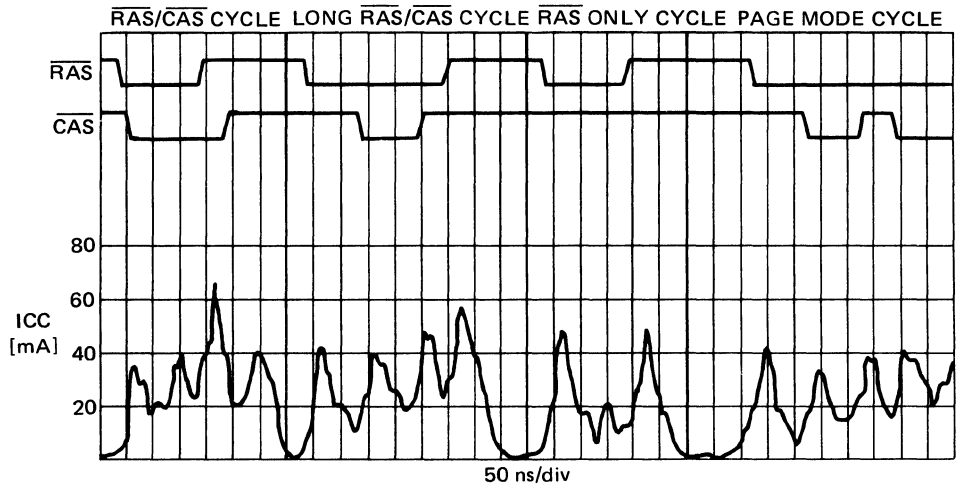
9

Clock Input
v.s. Vcc

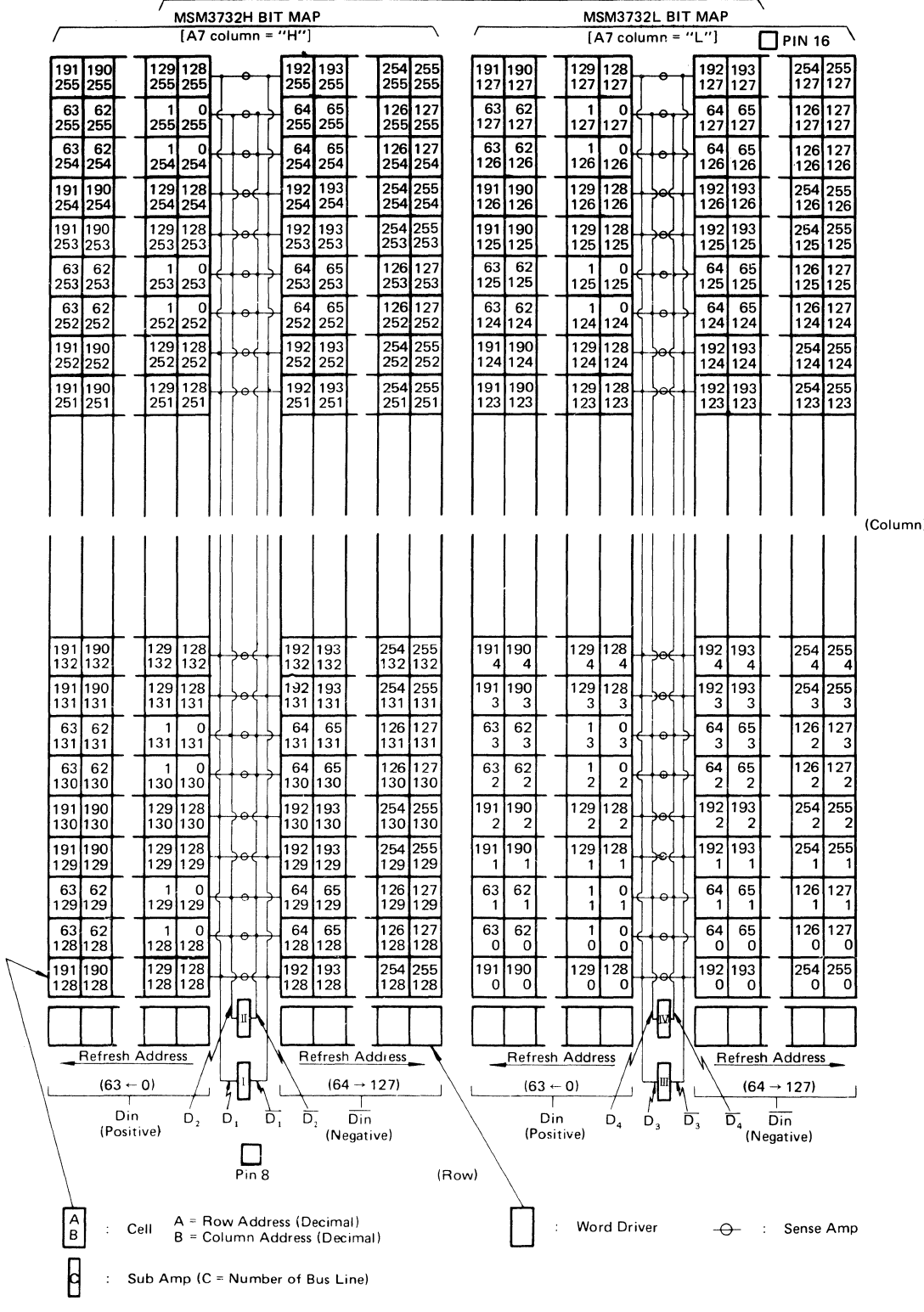


Clock Input
v.s. Ta




RAS/CAS CYCLE
LONG RAS/CAS CYCLE
RAS ONLY CYCLE
PAGE MODE CYCLE
RAS
CAS
80
60
ICC
[mA]
40
20
50 ns/div

MSM3732 Bit MAP (Physical-Decimal)



OKI semiconductor

MSM3764 AS/RS

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY (E3-S3-003-32)

GENERAL DESCRIPTION

The Oki MSM3764 is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

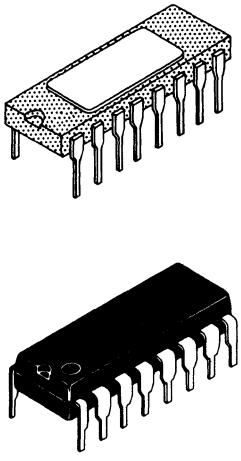
Multiplexed row and column address inputs permit the MSM3764 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MSM3764 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

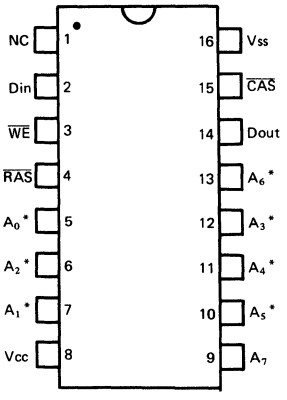
FEATURES

- 65,536 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  150 ns max (MSM3764-15)
  200 ns max (MSM3764-20)
- Cycle time,
  270 ns min (MSM3764-15)
  330 ns min (MSM3764-20)
- Low power: 248 mW active,
  28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 128 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance



PIN CONFIGURATION

(Top View)



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address

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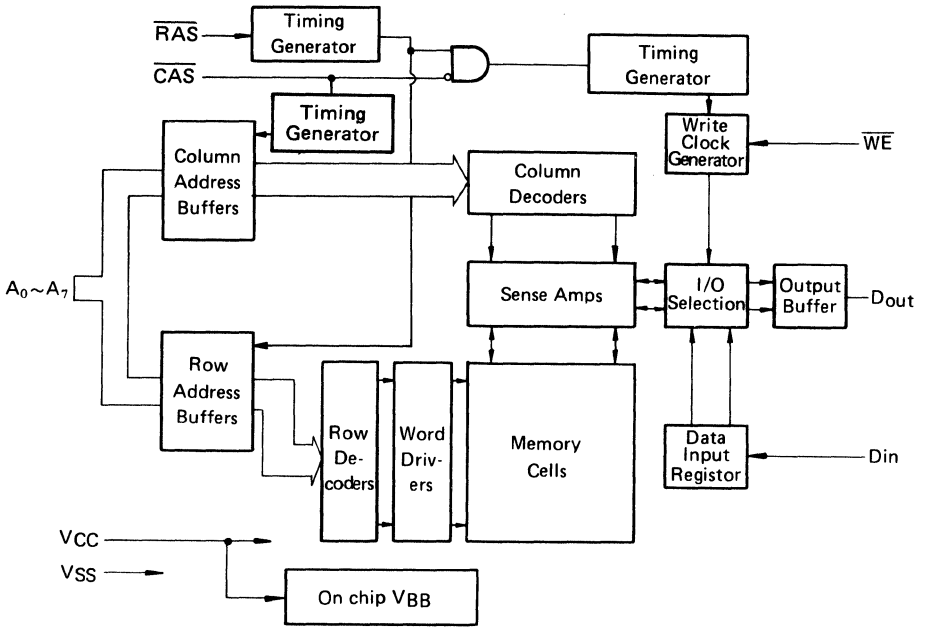
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		45	mA	
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
Refresh Current Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		35	mA	
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		42	mA	
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
Output Levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_7, D_{IN})	C_{IN1}	4.5	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	7	10	pF
Output Capacitance (D_{OUT})	C_{OUT}	5	7	pF

Capacitance measured with Boonton Meter.

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AC CHARACTERISTICS

Notes 1, 2, 3 Under Recommended Operating conditions

Parameter	Symbol	Units	MSM3764-15		MSM3764-20		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2	
Random read or write cycle time	t_{RC}	ns	270		330		
Read-write cycle time	t_{RWC}	ns	270		330		
Page mode cycle time	t_{PC}	ns	170		225		
Access time from $\overline{RAS}$	t_{RAC}	ns		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		100		135	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	50	
Transition time	t_T	ns	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	100		135		
$\overline{CAS}$ precharge time	t_{CP}	ns	60		80		
$\overline{CAS}$ pulse width	t_{CAS}	ns	100	10,000	135	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	20	50	25	65	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	20		25		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	45		55		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	95		120		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		8
Write command hold time	t_{WCH}	ns	45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	95		120		
Write command pulse width	t_{WP}	ns	45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	45		55		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	45		55		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	95		120		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	60		80		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	110		145		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		25		

NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.

2) AC measurements assume t_T = 5 ns.

3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4) Assumes that $t_{RCD} \leq t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

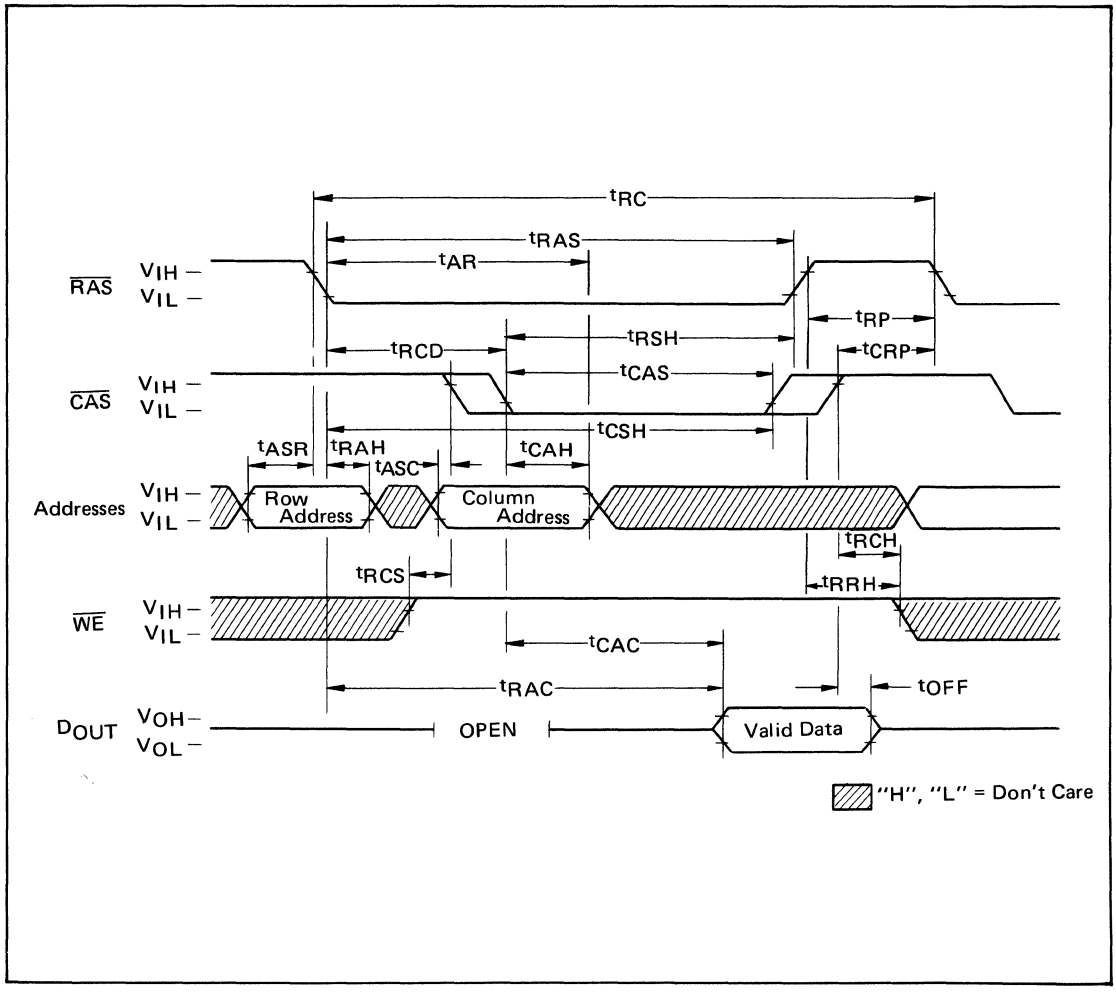
5) Assumes that $t_{RCD} \leq t_{RCD}$ (max.)

6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING



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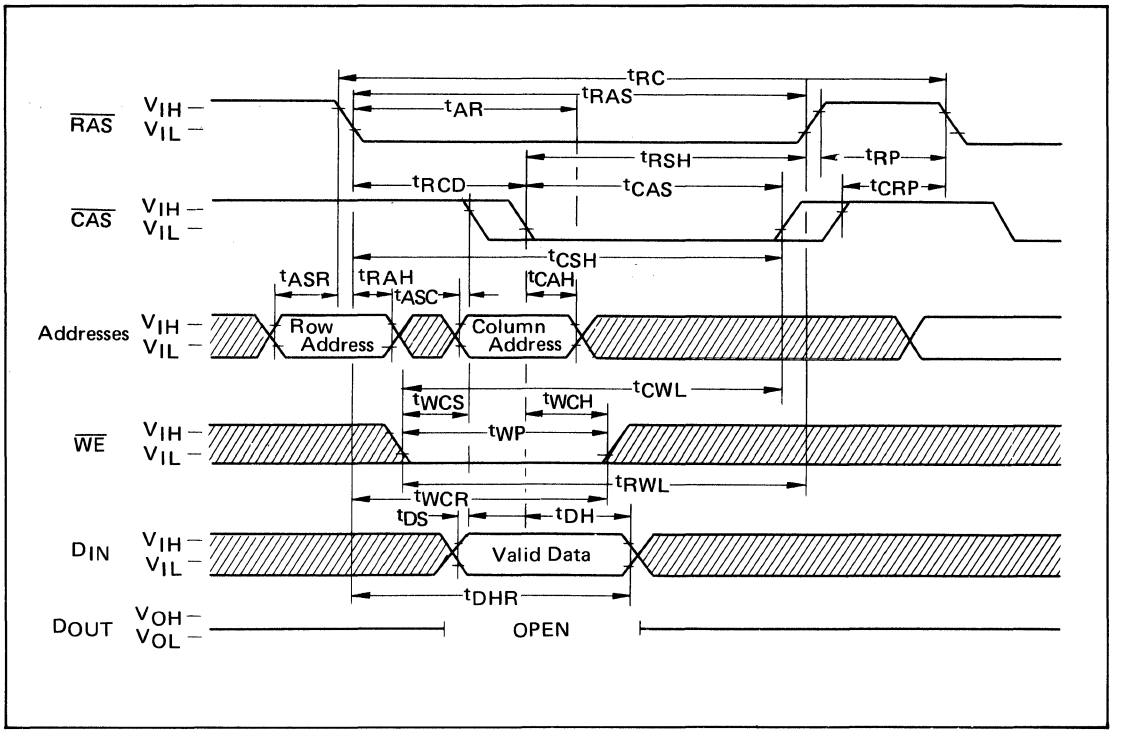
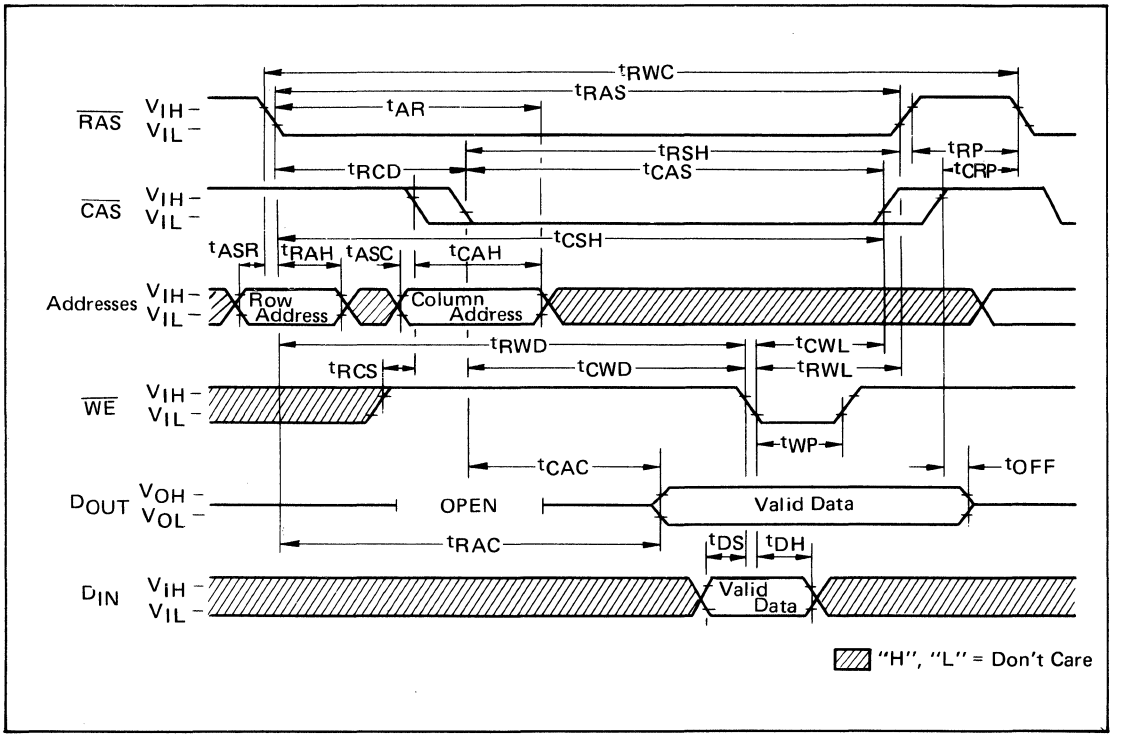
WRITE CYCLE TIMING

(EARLY WRITE)

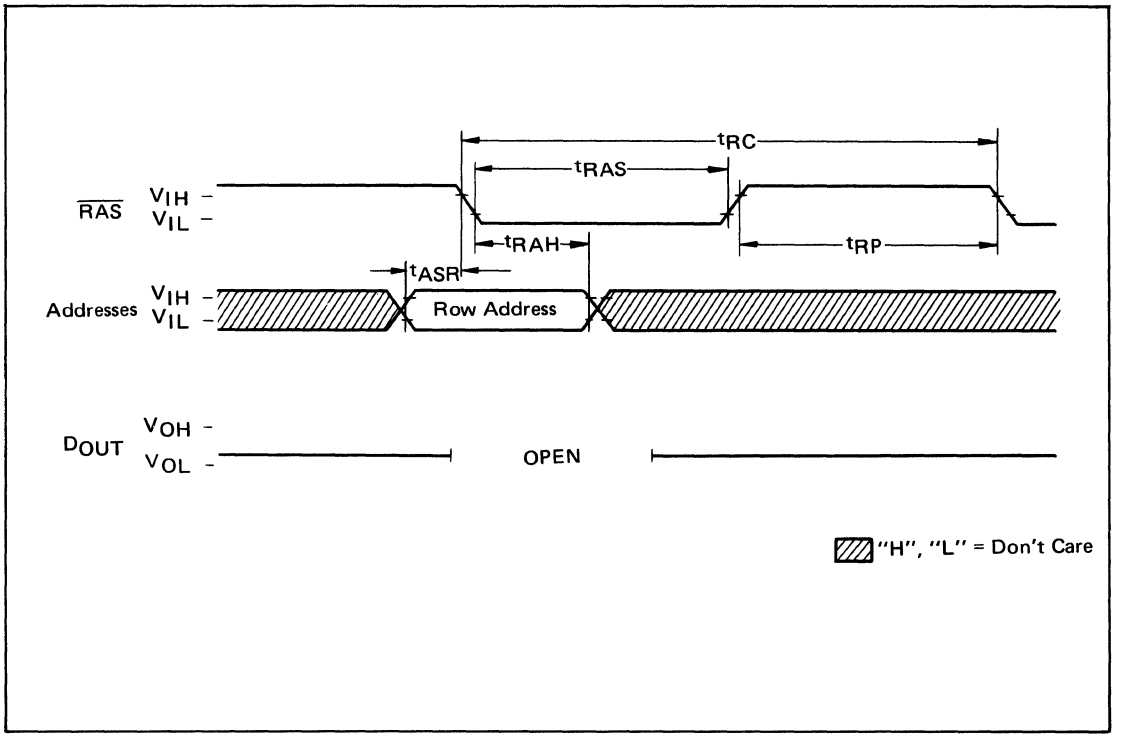


READ-WRITE/READ-MODIFY-WRITE CYCLE

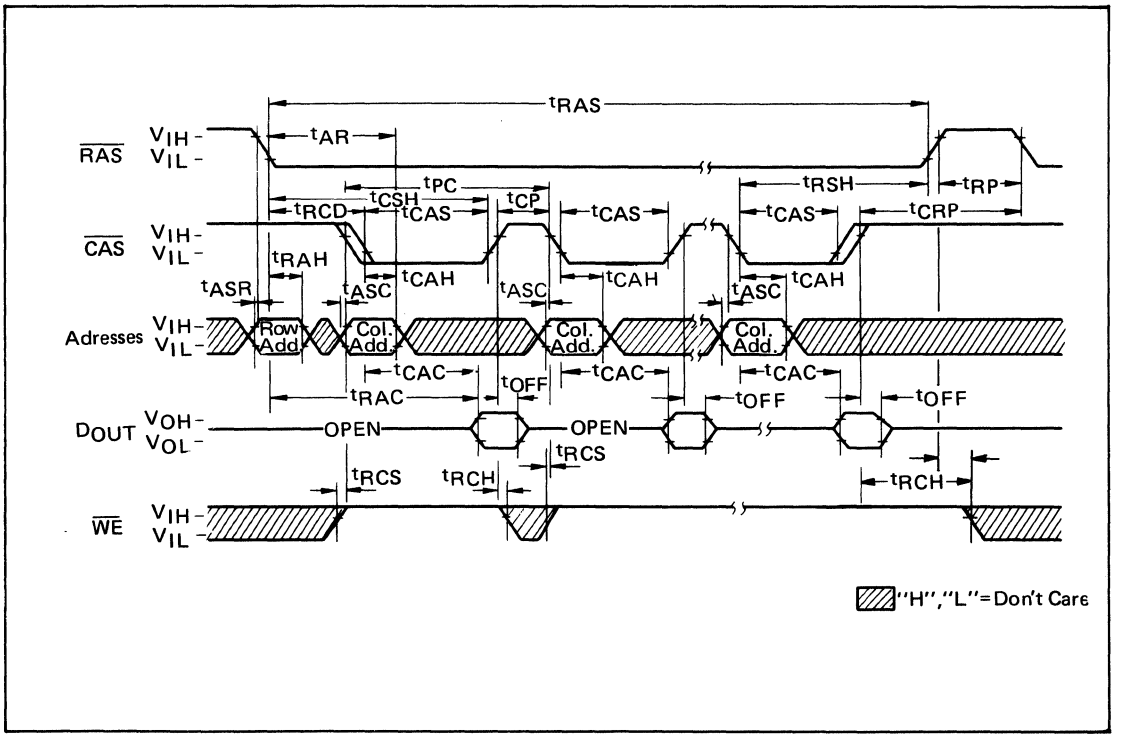


$\overline{RAS}$ ONLY REFRESH TIMING

($\overline{CAS}$: V_{IH}, $\overline{WE}$ & DIN: Don't care)



PAGE MODE READ CYCLE



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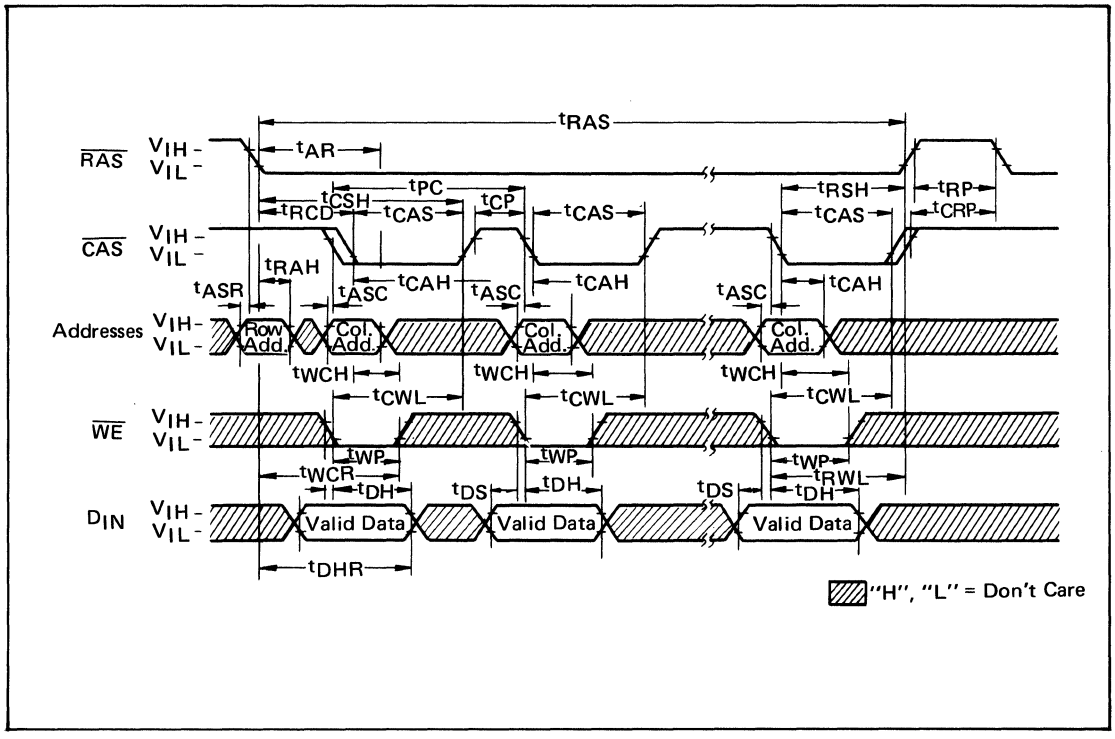
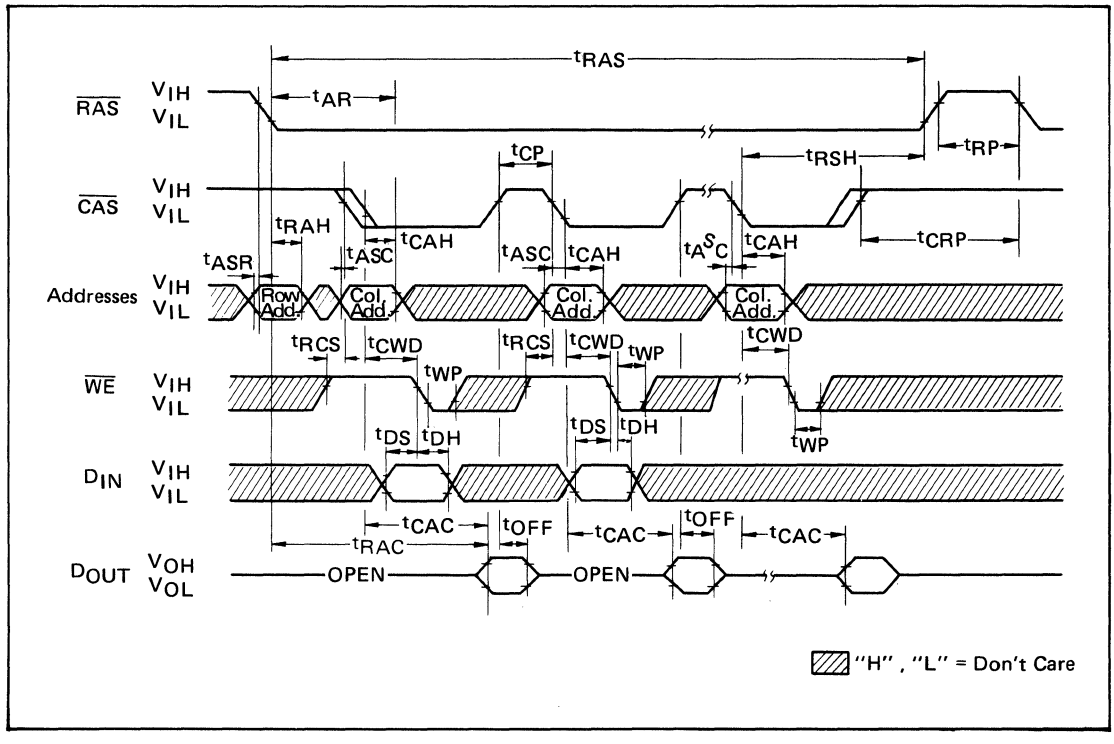
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



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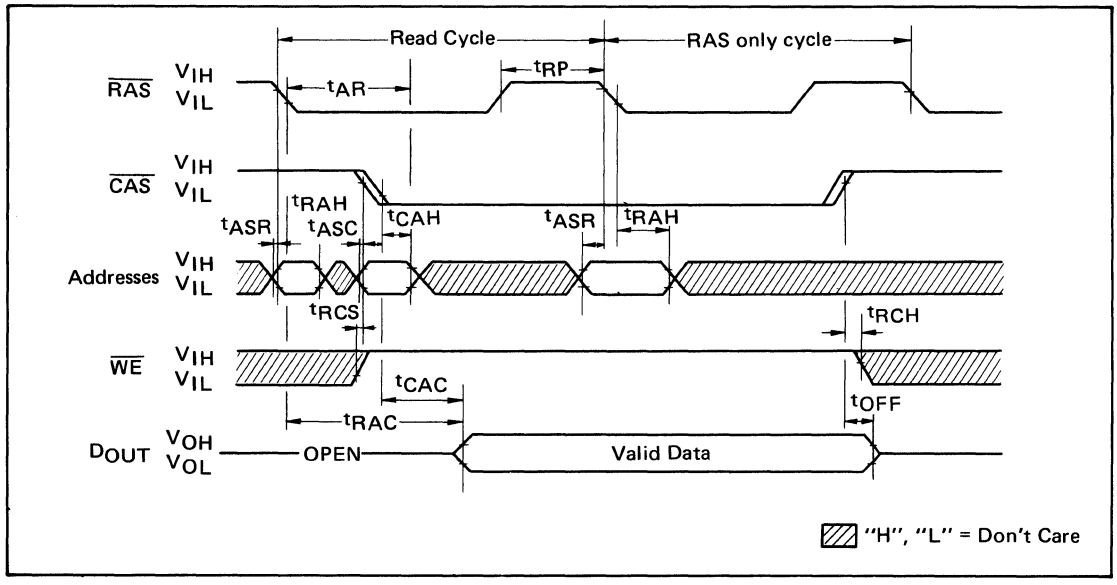
HIDDEN REFRFSH



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MSM3764. Eight row-address bits are established on the input pins (A_0~A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM3764 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transistion. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM3764 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses (A_0~A_6) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each rwo to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

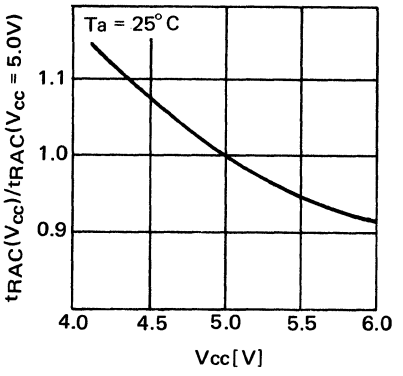
Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

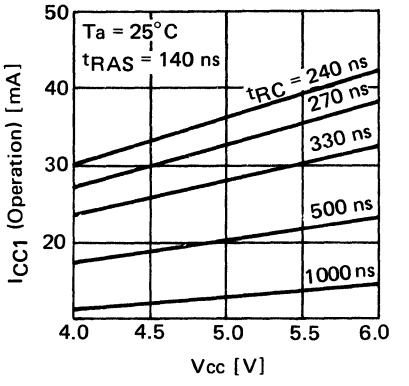
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

TYPICAL CHARACTERISTICS

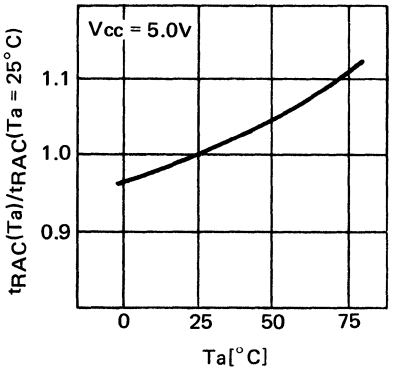
Access time from $\overline{RAS}$
(Relative value) v.s. Vcc



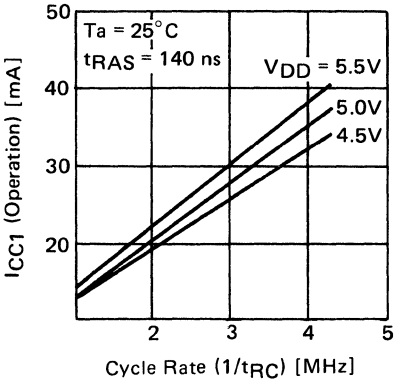
I_{CC1} (t_{RAS}: Constant)
v.s. Vcc



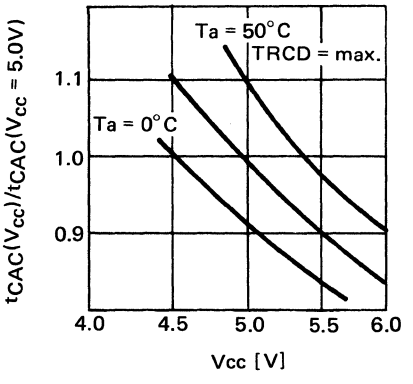
Access time from $\overline{RAS}$
(Relative value) v.s. Ta



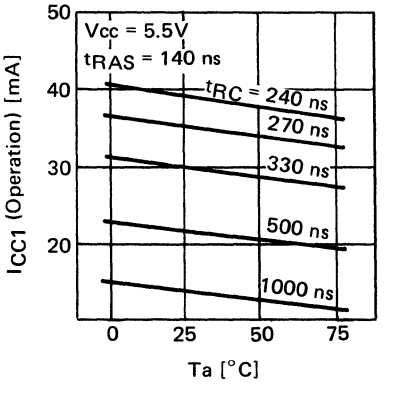
I_{CC1} (t_{RAS}: Constant)
v.s. Cycle rate



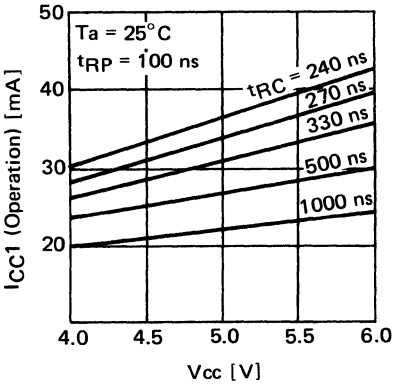
Access time from $\overline{CAS}$
(Relative value) v.s. Vcc



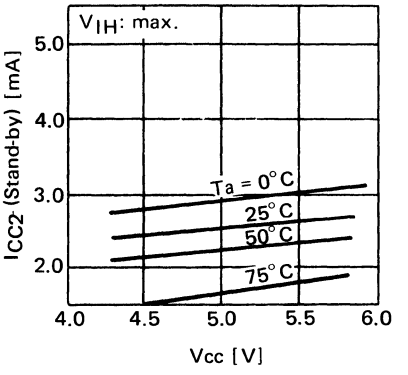
I_{CC1} (t_{RAS}: Constant)
v.s. Ta



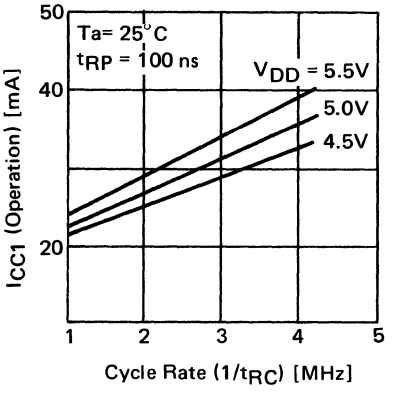
I_{CC1} (t_{RP}: Constant)
v.s. Vcc



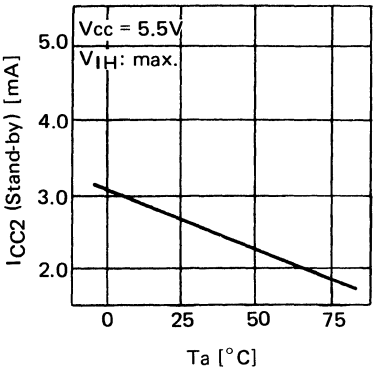
I_{CC2}
v.s. Vcc



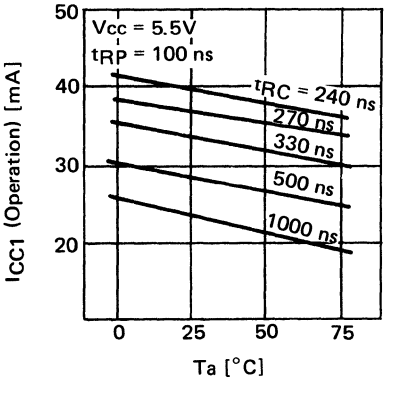
I_{CC1} (t_{RP}: Constant)
v.s. Cycle rate



I_{CC2} V.S. Ta



I_{CC1} (t_{RP}: Constant)
v.s. Ta



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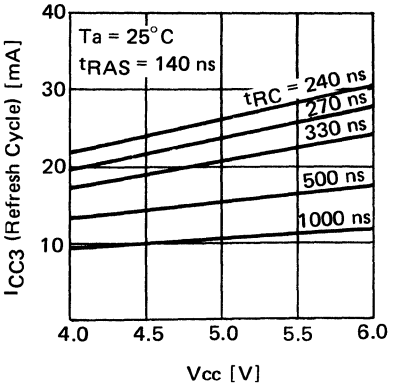
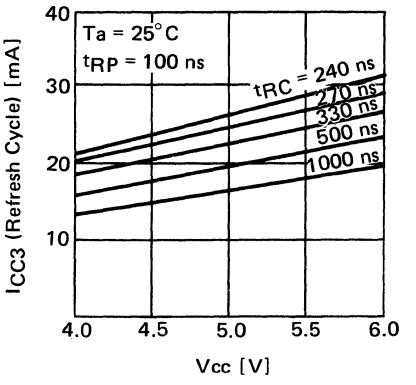
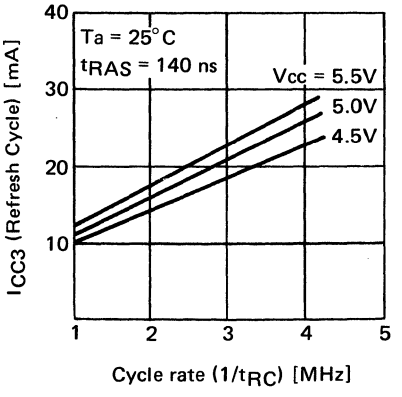
I_{CC3} (t_{RAS}: Constant)
v.s Vcc



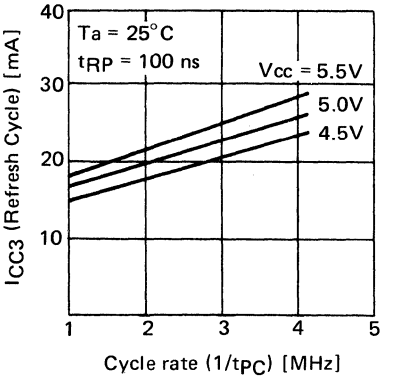
I_{CC3} (t_{RP}: Constant)
v.s. Vcc



I_{CC3} (t_{RAS}: Constant)
v.s. Cycle rate



I_{CC3} (t_{RP}: Constant)
v.s. Cycle rate



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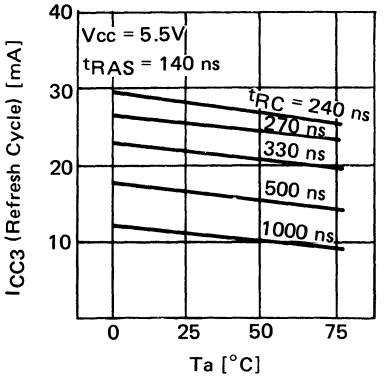
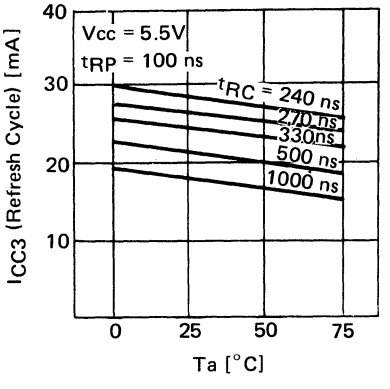
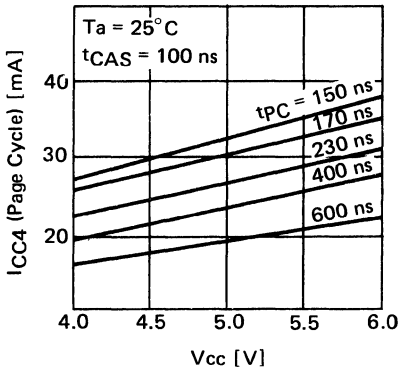
I_{CC3} (t_{RAS}: Constant)
v.s. Ta



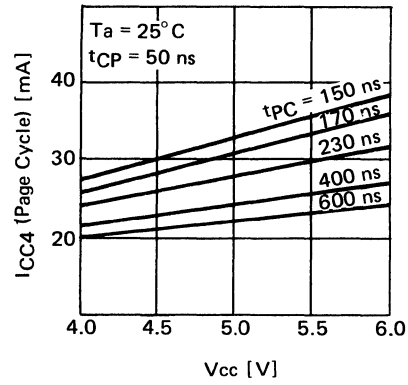
I_{CC3} (t_{RP}: Constant)
v.s. Ta



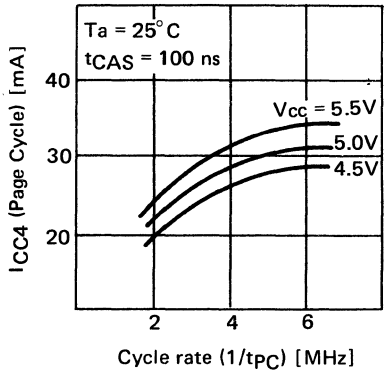
I_{CC4} (t_{CAS}: Constant)
v.s. Vcc



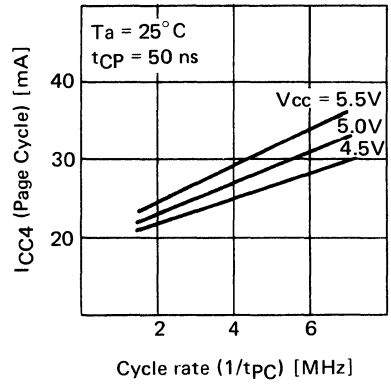
I_{CC4} (t_{CP}: Constant)
v.s. Vcc



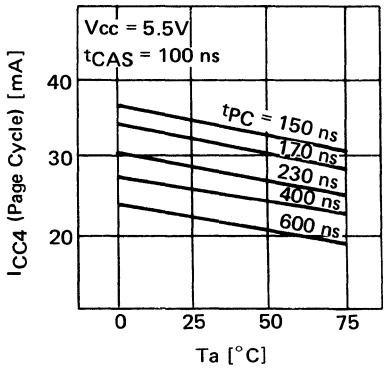
I_{CC4} (t_{CAS}: Constant)
v.s. Cycle rate



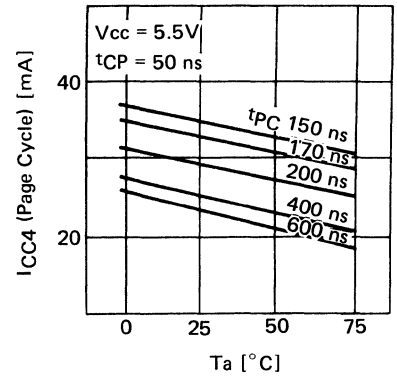
I_{CC4} (t_{CP}: Constant)
v.s. Cycle rate



I_{CC4} (t_{CAS}: Constant)
v.s. Ta

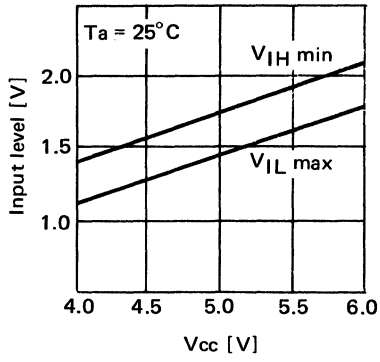


I_{CC4} (t_{CP}: Constant)
v.s. Ta

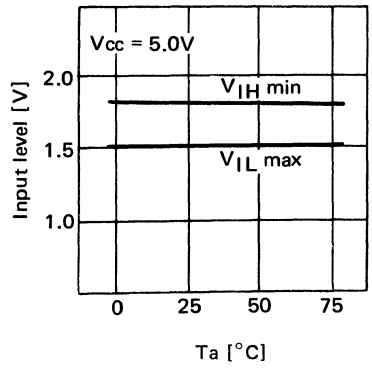


9

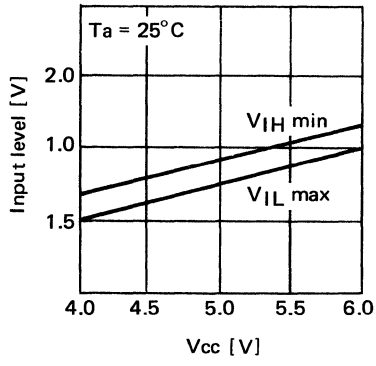
Address Input
v.s Vcc



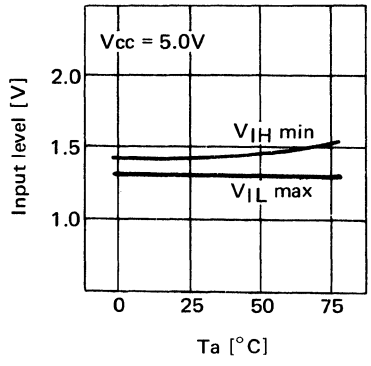
Address Input
v.s. Ta



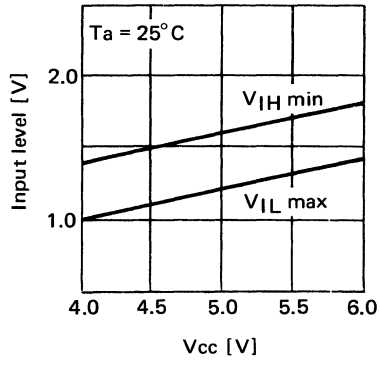
Data Input
v.s. Vcc



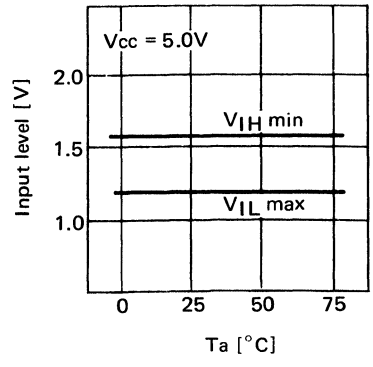
Data Input
v.s. Ta



Clock Input
v.s. Vcc



Clock Input
v.s. Ta



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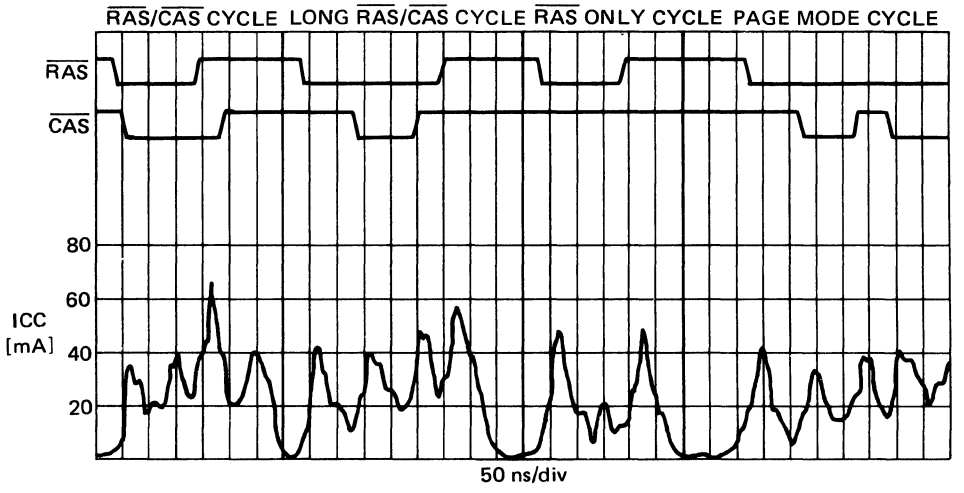
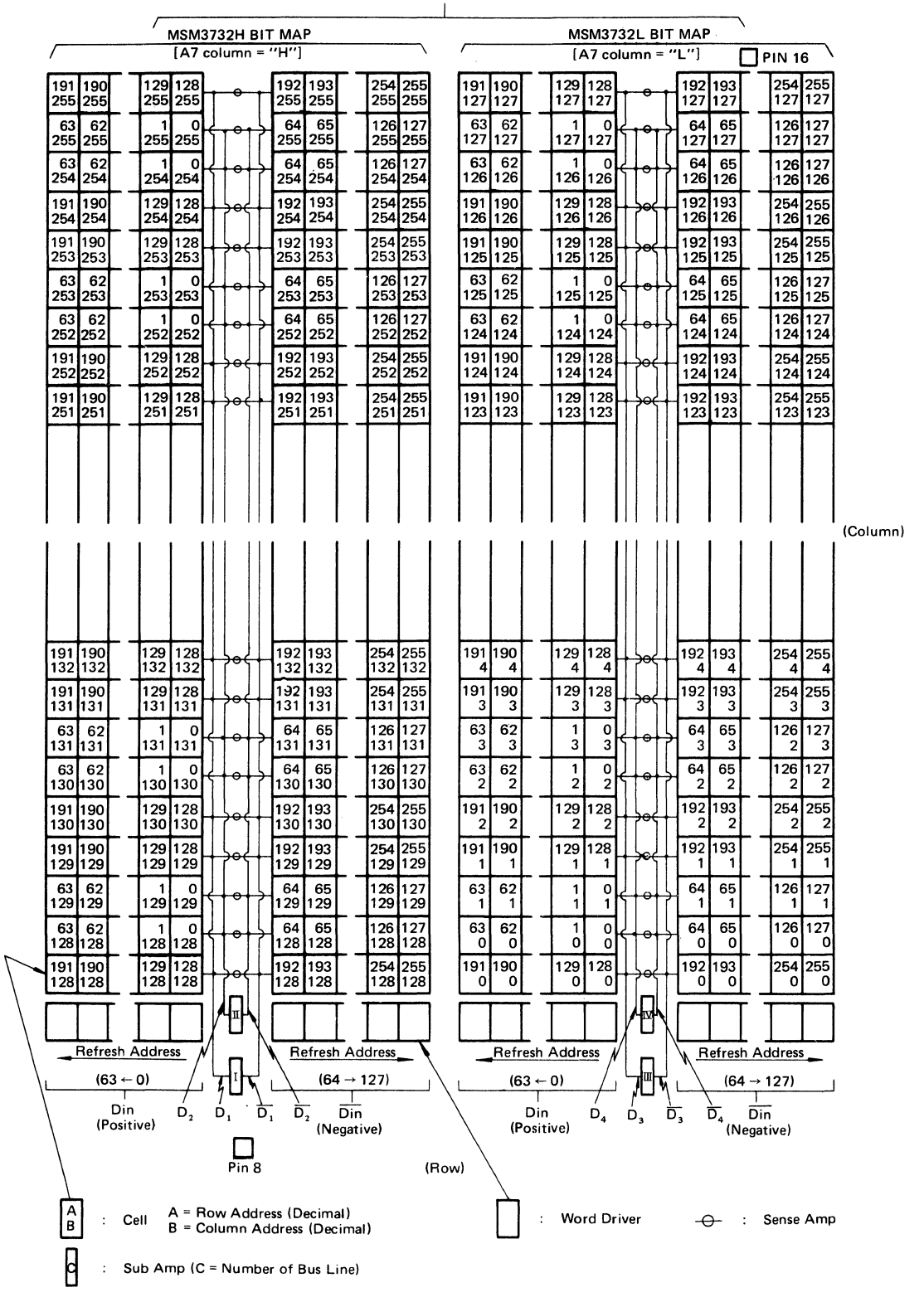

RAS/CAS CYCLE
LONG RAS/CAS CYCLE
RAS ONLY CYCLE
PAGE MODE CYCLE
RAS
CAS
80
60
ICC
[mA]
40
20
50 ns/div

MSM3764 Bit MAP (Physical-Decimal)



Preliminary

MSM3764 AAS/ARS

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY (E3-S-004-32)

GENERAL DESCRIPTION

The Oki MSM3764A is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

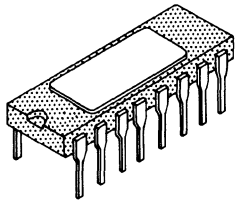
Multiplexed row and column address inputs permit the MSM3764A to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

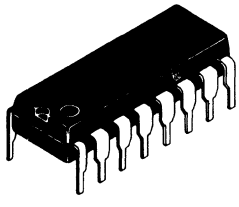
The MSM3764A is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

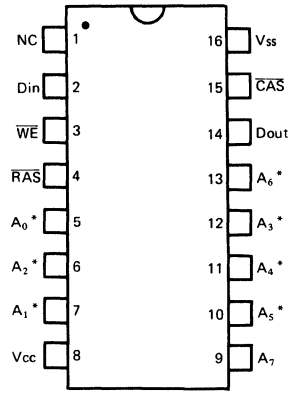
- 65,536 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  120 ns max (MSM3764A-12)
  150 ns max (MSM3764A-15)
  200 ns max (MSM3764A-20)
- Cycle time,
  230 ns min (MSM3764A-12)
  260 ns min (MSM3764A-15)
  330 ns min (MSM3764A-20)
- Low power: 330 mW active,
  28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 128 refersh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance





PIN CONFIGURATION

(Top View)



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address

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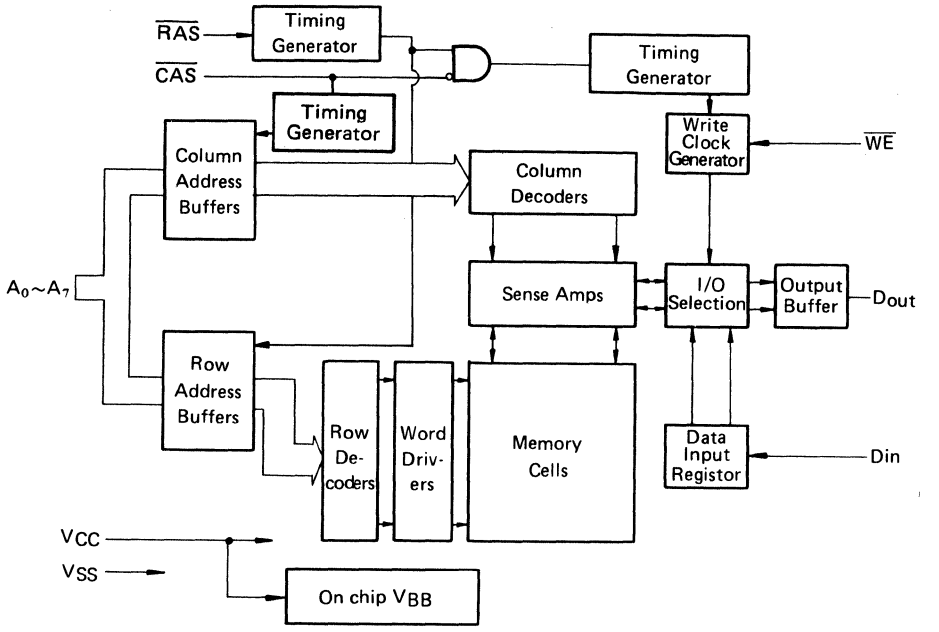
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		60	mA	
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
Refresh Current Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		40	mA	
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		60	mA	
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
Output Levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_7, D_{IN})	C_{IN1}	4.5	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	7	10	pF
Output Capacitance (D_{OUT})	C_{OUT}	5	7	pF

Capacitance measured with Boonton Meter.

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AC CHARACTERISTICS

Notes 1, 2, 3 Under Recommended Operating conditions

Parameter	Symbol	Units	MSM3764A-12		MSM3764A-15		MSM3764A-20		Note
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2		2	
Random read or write cycle time	t_{RC}	ns	230		260		330		
Read-write cycle time	t_{RWC}	ns	255		280		345		
Page mode cycle time	t_{PC}	ns	130		145		190		
Access time from $\overline{RAS}$	t_{RAC}	ns		120		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		60		75		100	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	35	0	40	0	50	
Transition time	t_T	ns	3	35	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	60		75		100		
$\overline{CAS}$ precharge time (Page cycle)	t_{CP}	ns	60		60		80		
$\overline{CAS}$ pulse width	t_{CAS}	ns	60	10,000	75	10,000	100	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	120		150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	60	25	75	30	100	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		0		
Row Address set-up time	t_{ASR}	ns	0		0		0		
Row Address hold time	t_{RAH}	ns	20		20		25		
Column Address set-up time	t_{ASC}	ns	0		0		0		
Column Address hold time	t_{CAH}	ns	20		20		25		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	80		95		125		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time	t_{RCH}	ns	0		0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		−10		8
Write command hold time	t_{WCH}	ns	40		45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	100		120		155		
Write command pulse width	t_{WP}	ns	40		45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		45		55		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		45		55		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	40		45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	100		120		155		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	40		45		55		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	100		120		155		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	0		0		0		
$\overline{CAS}$ precharge time	t_{CPN}	ns	30		35		45		

NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.

2) AC measurements assume t_T = 5 ns.

3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

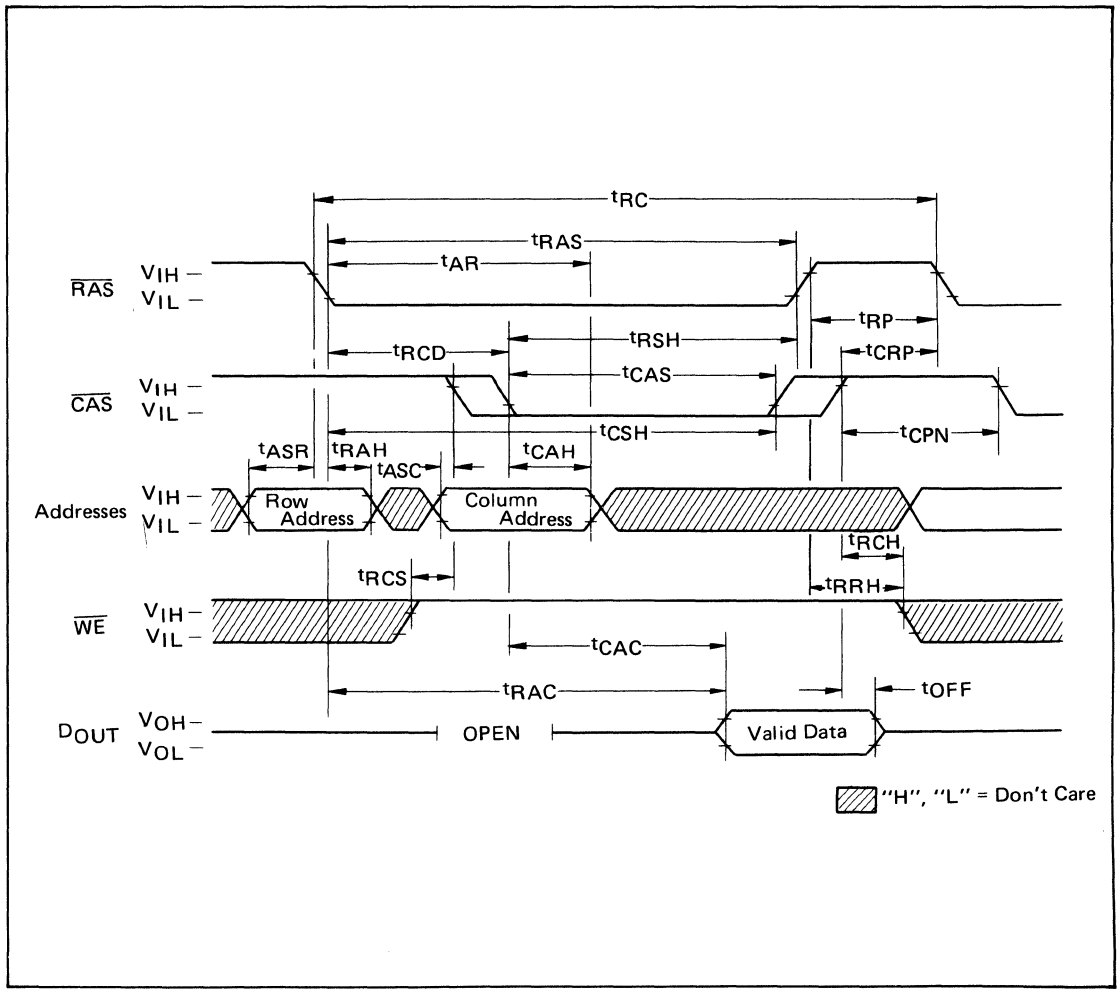
5) Assumes that $t_{RCD} < t_{RCD}$ (max.)

6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

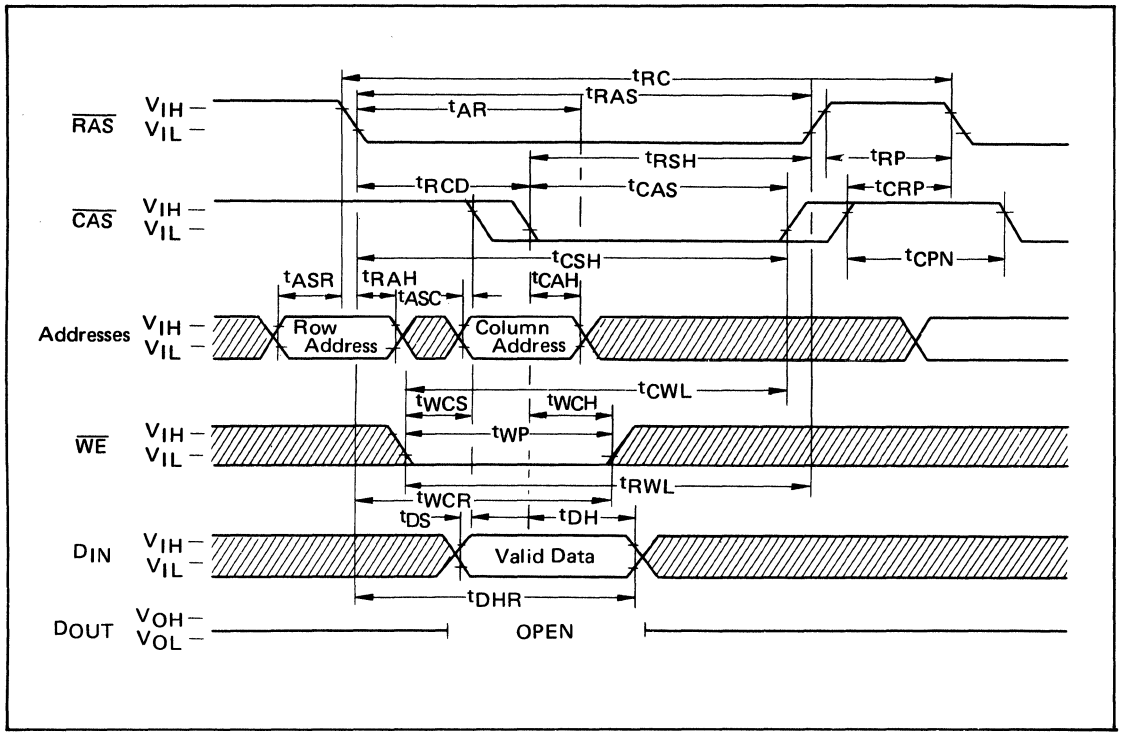
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

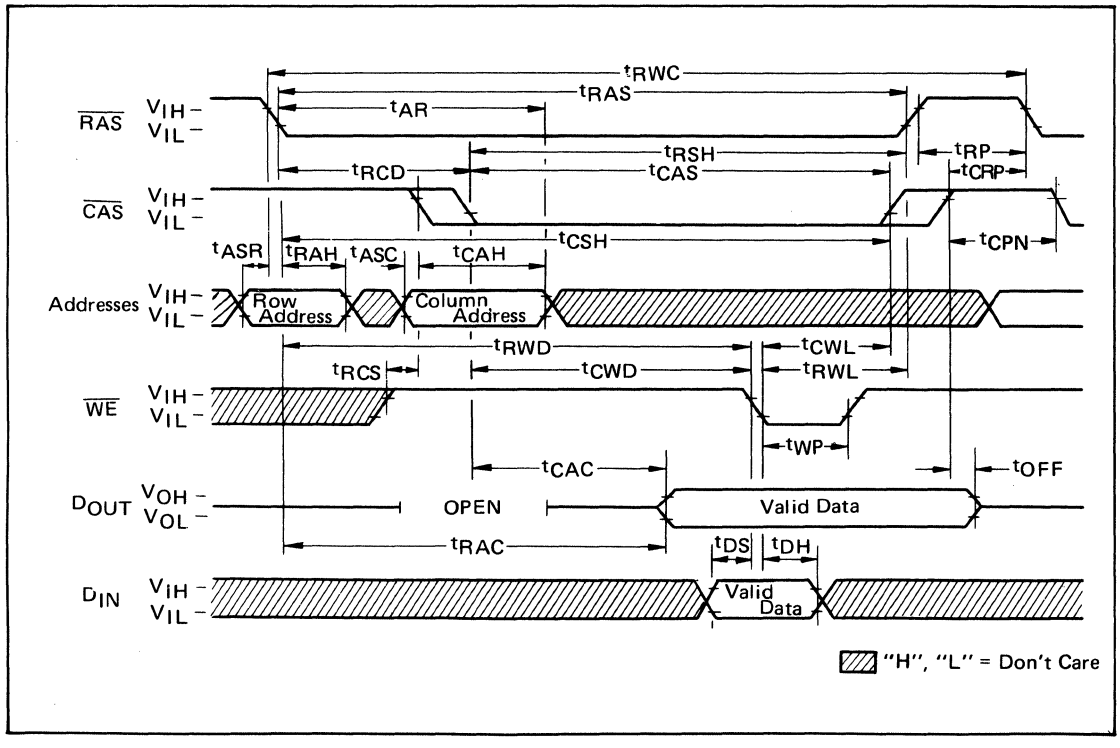


WRITE CYCLE TIMING

(EARLY WRITE)

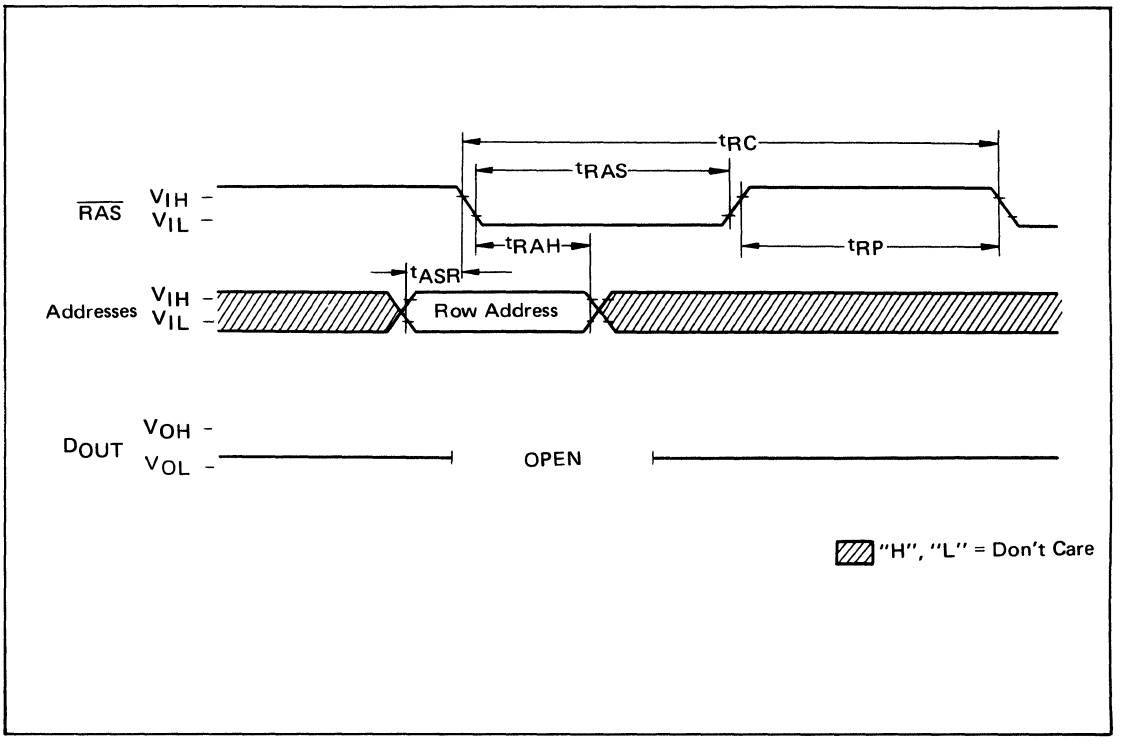


READ-WRITE/READ-MODIFY-WRITE CYCLE

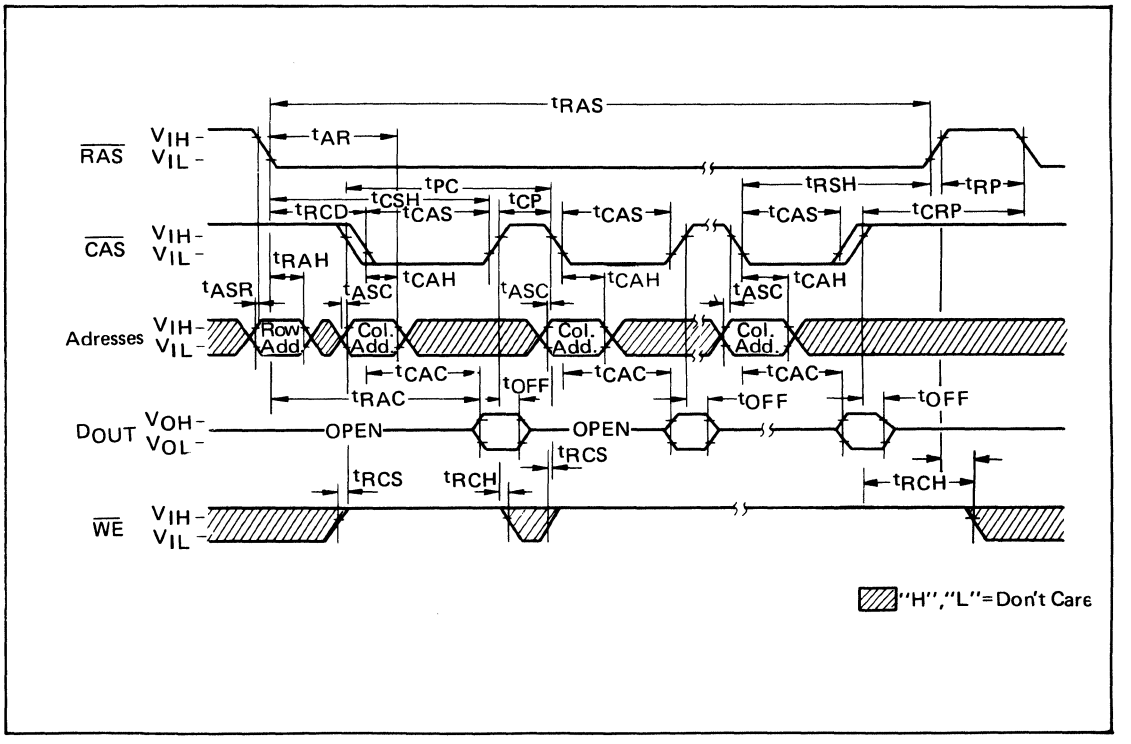


$\overline{RAS}$ ONLY REFRESH TIMING

($\overline{CAS}$: V_{IH}, $\overline{WE}$ & DIN: Don't care)



PAGE MODE READ CYCLE



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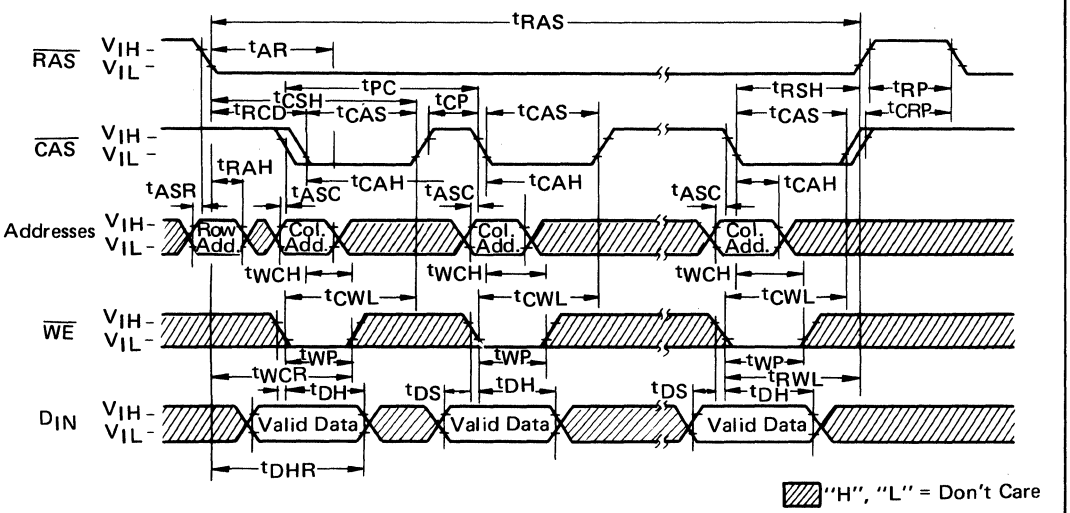
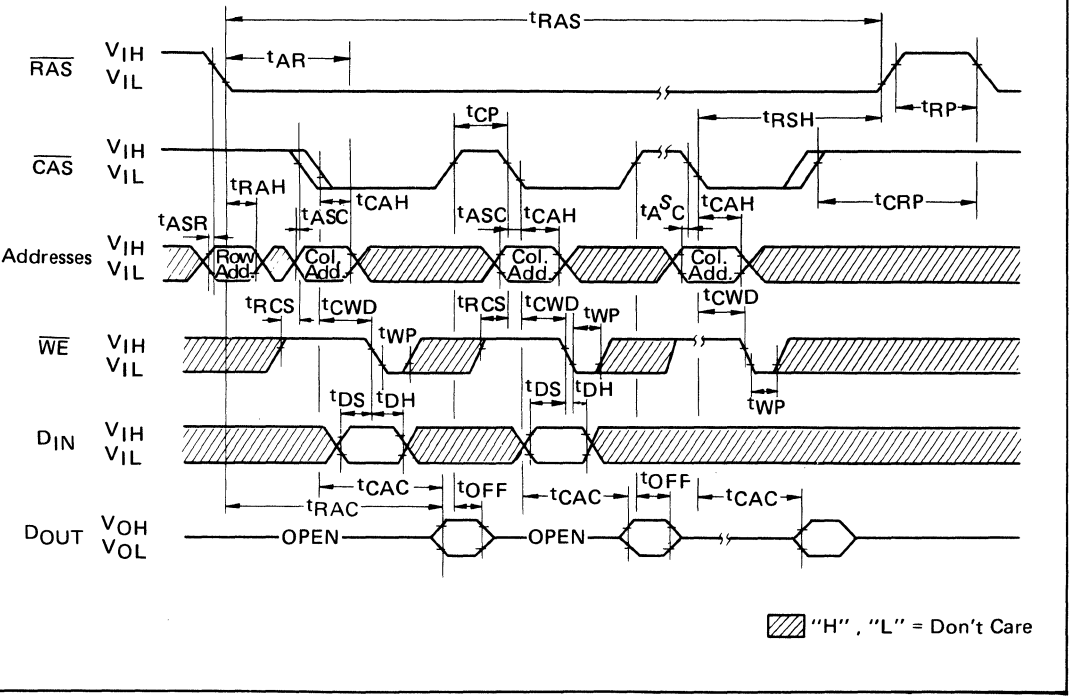
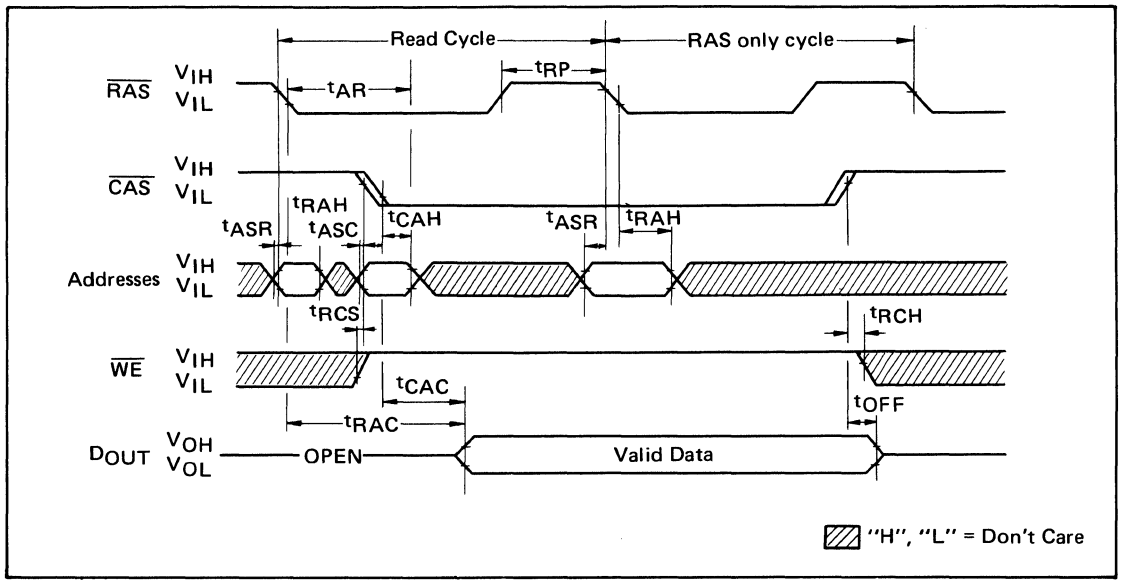
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



HIDDEN REFRFSH



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MSM3764A. Eight row-address bits are established on the input pins ($A_0 \sim A_7$) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM3764A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transistion. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM3764A while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each rwo to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

Preliminary

MSM37256AS

262144-BIT DYNAMIC RANDOM ACCESS MEMORY <Page Mode Type>

GENERAL DESCRIPTION

The Oki MSM37256 is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

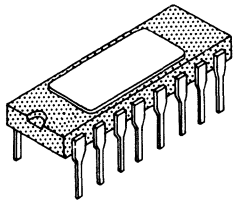
Multiplexed row and column address inputs permit the MSM37256 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out.

The MSM37256 is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

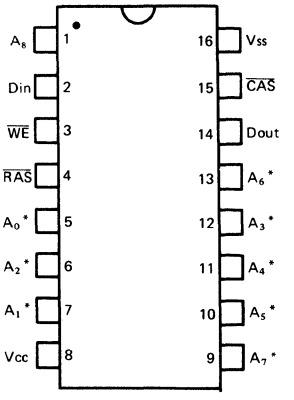
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 262144 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  150 ns max (MSM37256-15AS)
  200 ns max (MSM37256-20AS)
- Cycle time,
  270 ns min (MSM37256-15AS)
  330 ns min (MSM37256-20AS)
- Low power: 440 mW active,
  28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 256 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance



PIN CONFIGURATION



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)

* Refresh Address

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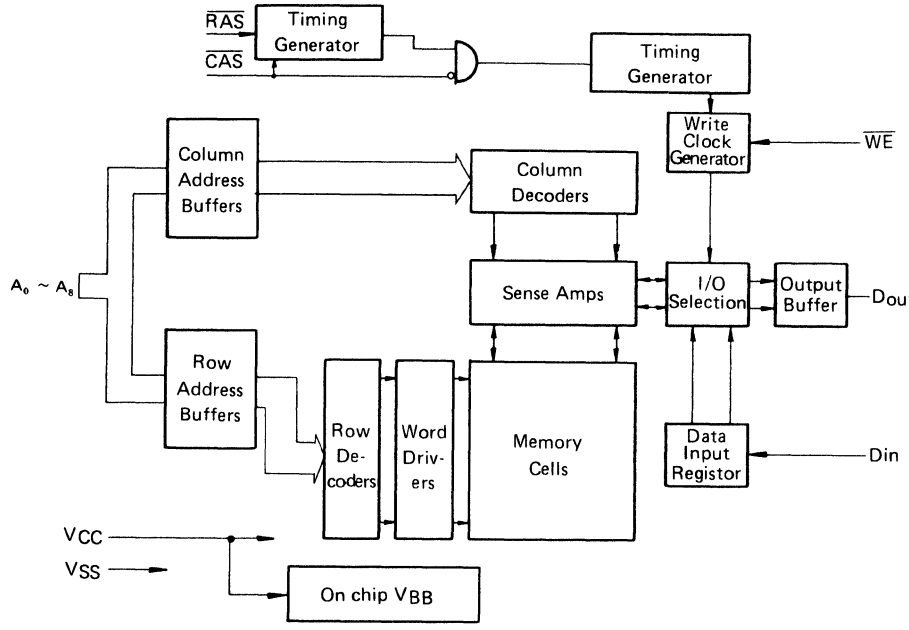
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		80	mA	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
REFRESH CURRENT Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		65	mA	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		60	mA	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = −5 mA)	V_{OH}	2.4		V	
Output low voltage (I_{OL} = 4.2 mA)	V_{OL}		0.4	V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_8, D_{IN})	C_{IN1}	5	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	7	10	pF
Output Capacitance (D_{OUT})	C_{OUT}	5	7	pF

Capacitance measured with Boonton Meter.

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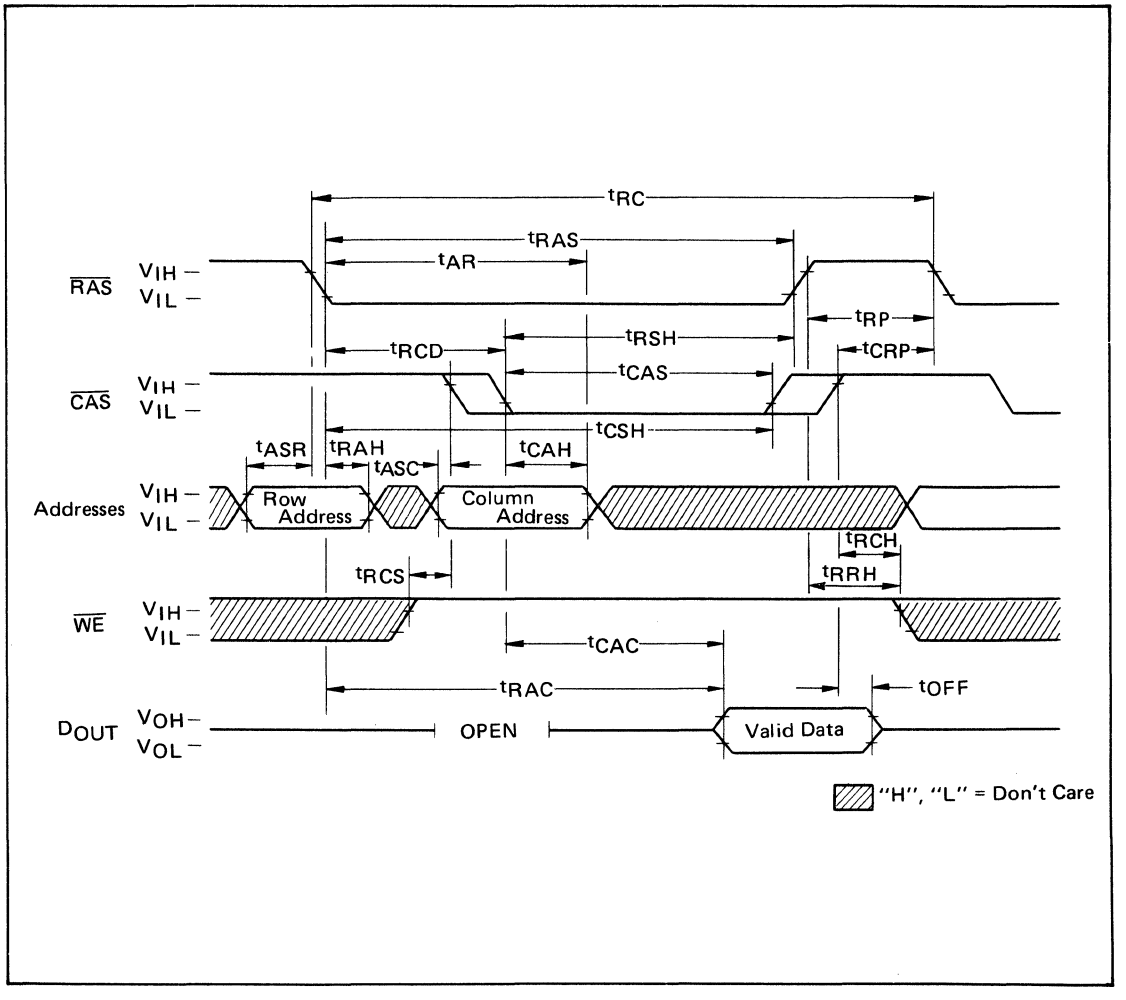
AC CHARACTERISTICS

Notes 1, 2, 3 Under Recommended Operating conditions

Parameter	Symbol	Units	MSM37256-15		MSM37256-20		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4	
Random read or write cycle time	t_{RC}	ns	270		330		
Read-write cycle time	t_{RWC}	ns	270		330		
Page mode cycle time	t_{PC}	ns	170		225		
Access time from $\overline{RAS}$	t_{RAC}	ns		150		200	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		100		135	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	40	0	50	
Transition time	t_T	ns	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	150	10,000	200	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	100		135		
$\overline{CAS}$ precharge time	t_{CP}	ns	60		80		
$\overline{CAS}$ pulse width	t_{CAS}	ns	100	10,000	135	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	150		200		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	20	50	25	65	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	20		25		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	45		55		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	95		120		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		8
Write command hold time	t_{WCH}	ns	45		55		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	95		120		
Write command pulse width	t_{WP}	ns	45		55		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	45		55		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	45		55		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	45		55		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	95		120		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	60		80		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	110		145		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		25		

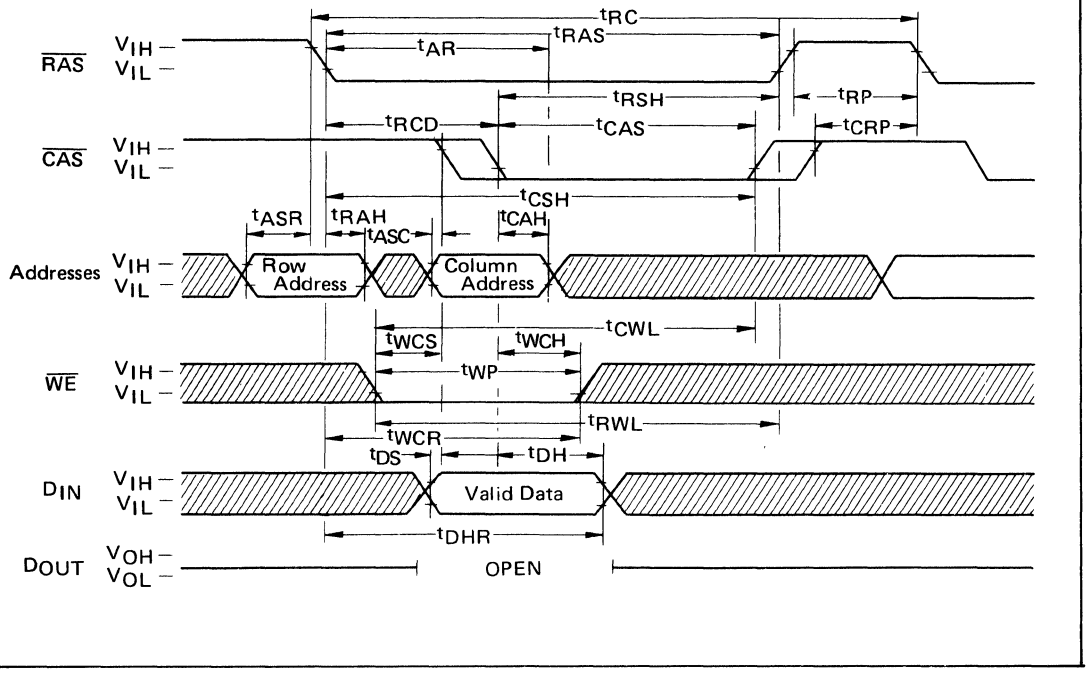
NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
5) Assumes that $t_{RCD} < t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING

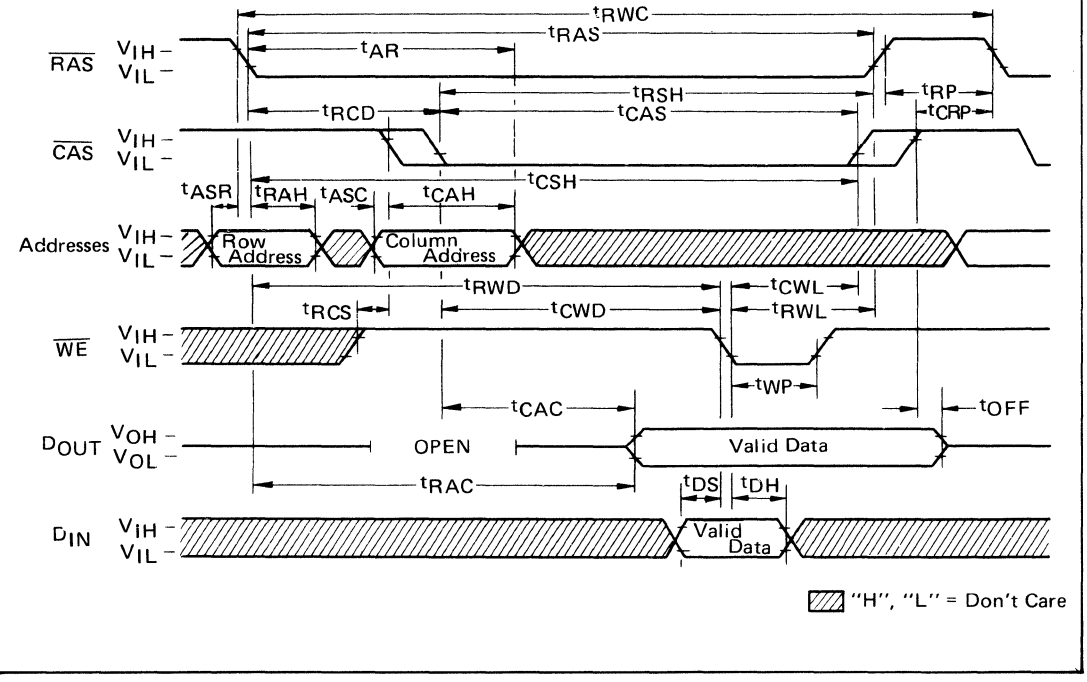


WRITE CYCLE TIMING

(EARLY WRITE)

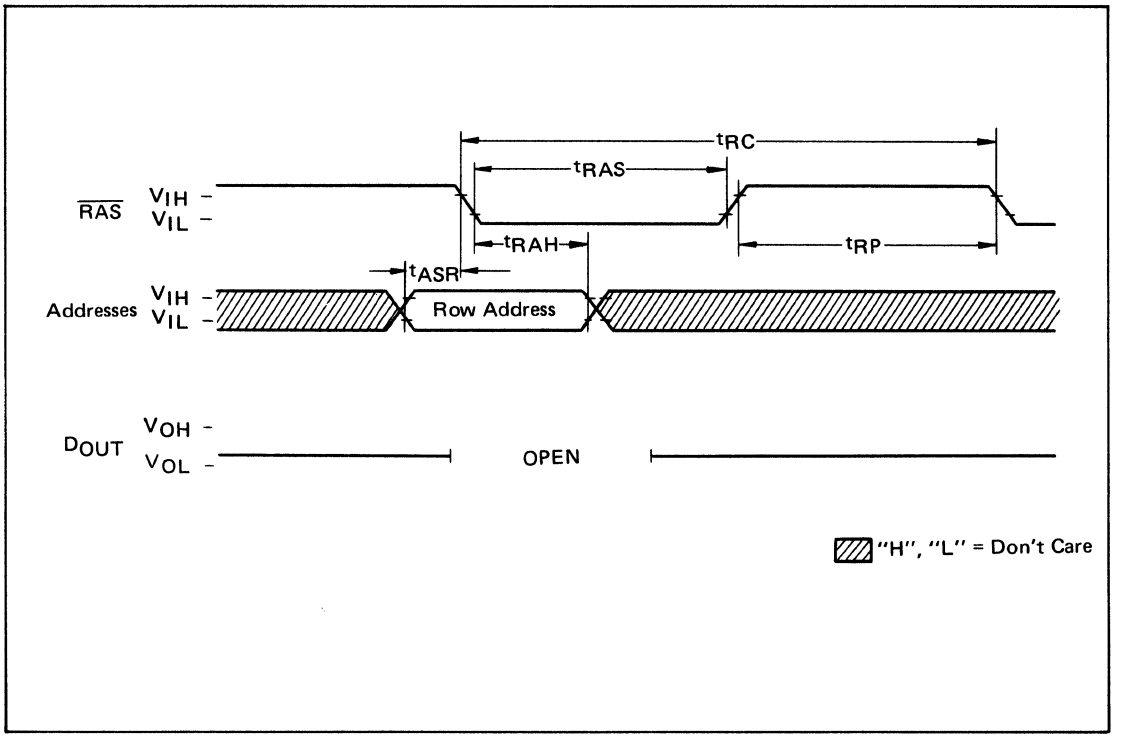


READ-WRITE/READ-MODIFY-WRITE CYCLE

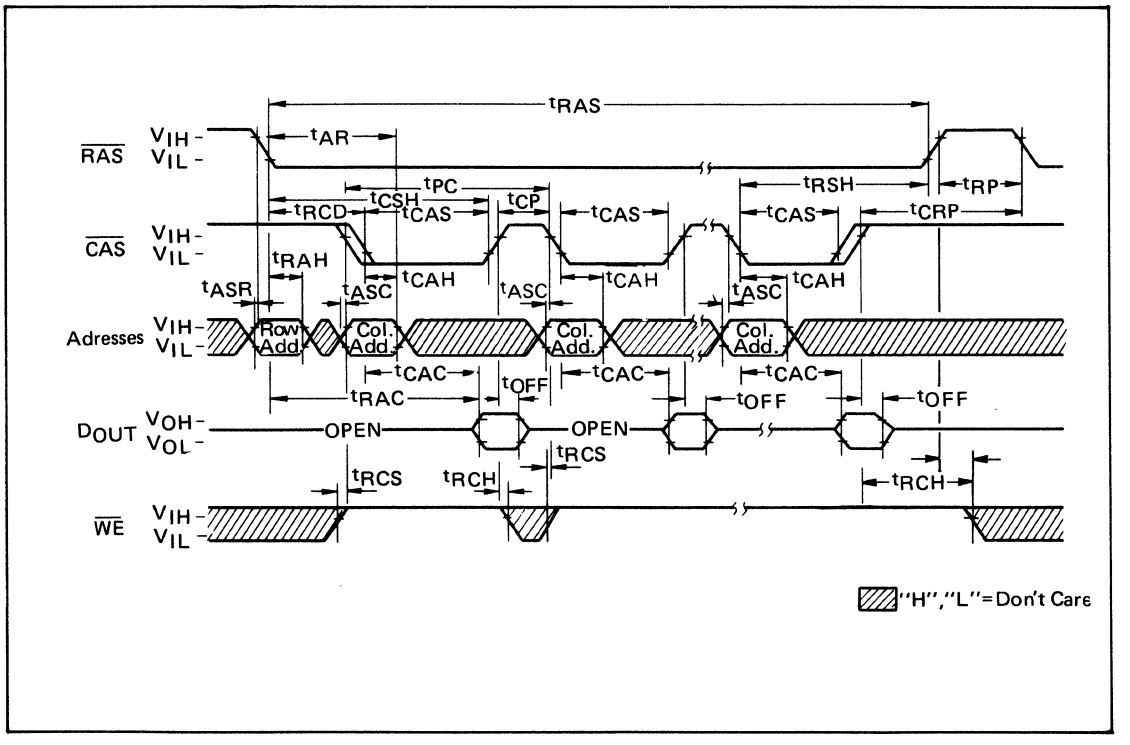


$\overline{RAS}$ ONLY REFRESH TIMING

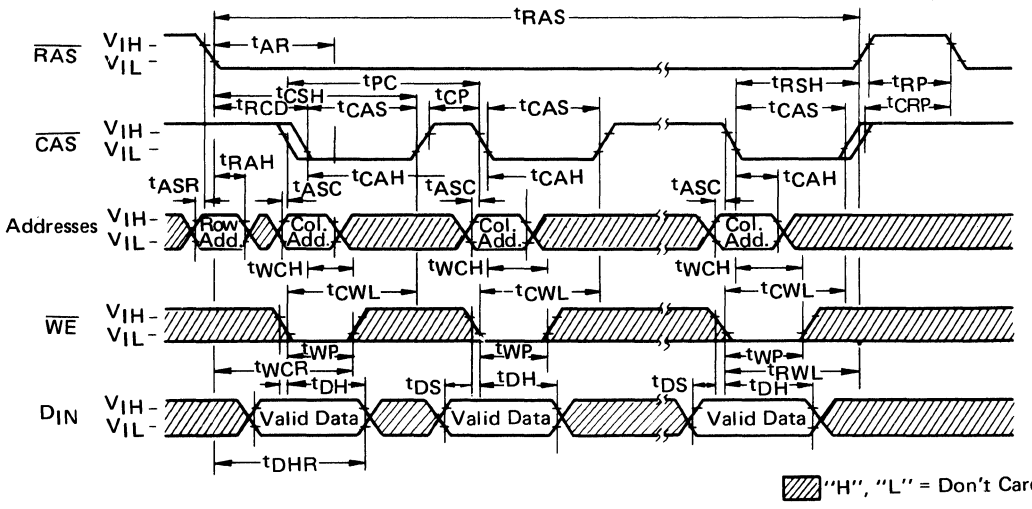
($\overline{CAS}$: V_{IH}, $\overline{WE}$ & D_{IN}: Don't care)



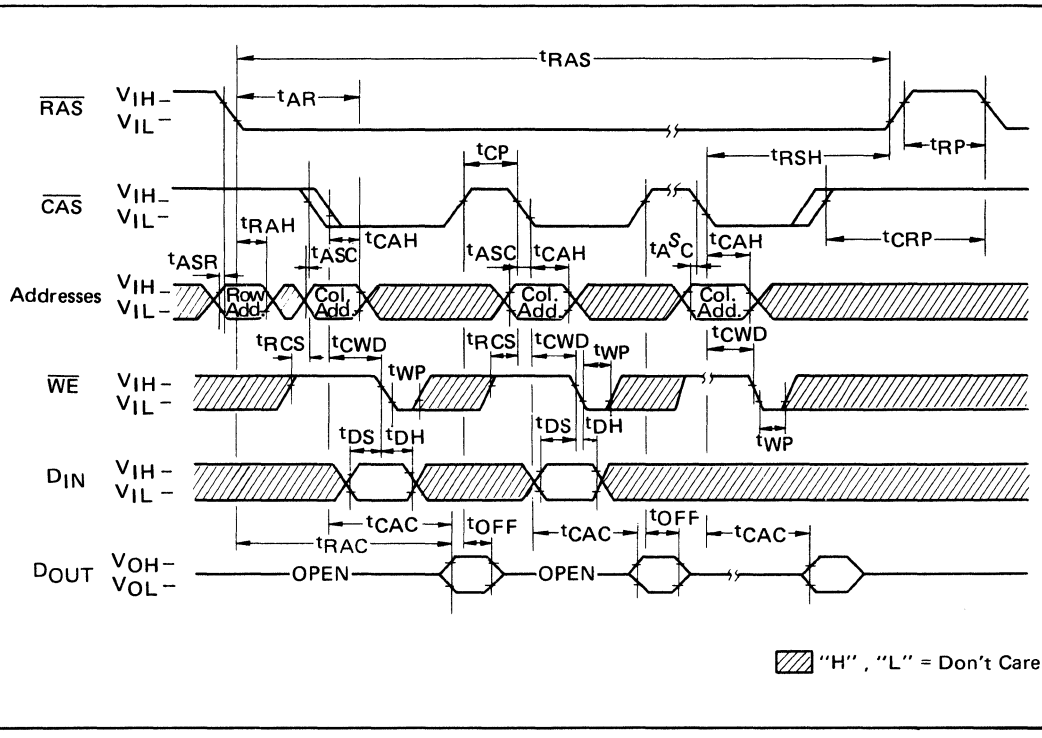
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



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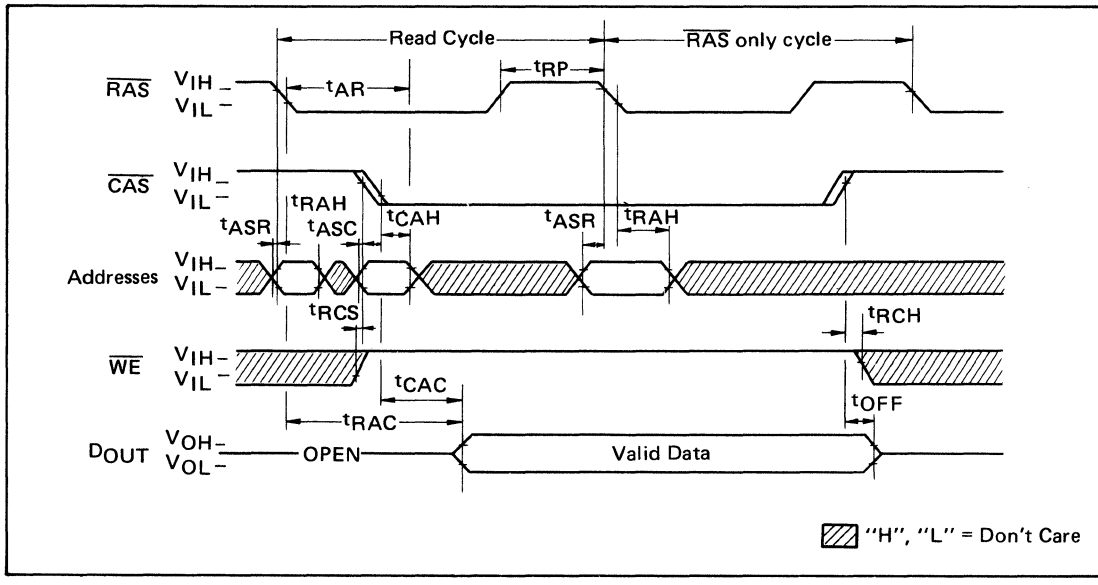
HIDDEN REFRFSH



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 262144 storage cell locations within the MSM37256. Eight row-address bits are established on the input pins ($A_0 \sim A_8$) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM37256 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transistion. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM37256 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ($A_0 \sim A_7$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_8. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row-addresses with $\overline{RAS}$ will cause all bits in each rwo to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:

$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

OKI semiconductor

Preliminary

MSM41256AS/RS

262144-BIT DYNAMIC RANDOM ACCESS EMMORY < Nibble Mode Type >

GENERAL DESCRIPTION

The Oki MSM41256 is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

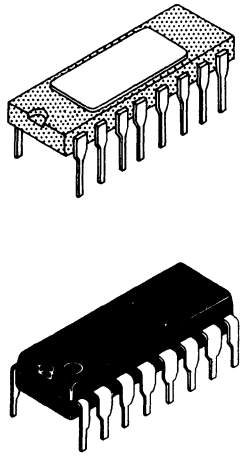
Multiplexed row and column address inputs permit the MSM41256 to be housed in a standard 16 pin DIP. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41256 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability, also features "nibble mode" which allows high speed serial access to up to 4 bits of data.

The MSM41256 is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

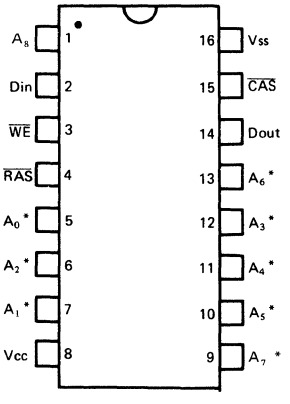
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

- 262,144 x 1 RAM, 16 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time
  - 100 ns max (MSM41256-10AS/RS)
  - 120 ns max (MSM41256-12AS/RS)
  - 150 ns max (MSM41256-15AS/RS)
- Cycle time,
  - 200 ns min (MSM41256-10AS/RS)
  - 230 ns min (MSM41256-12AS/RS)
  - 280 ns min (MSM41256-15AS/RS)
- Low power: 415 mW active, 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 4ms/256 refresh cycles
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle and allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Nibble Mode" capability



PIN CONFIGURATION



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)

* Refresh Address

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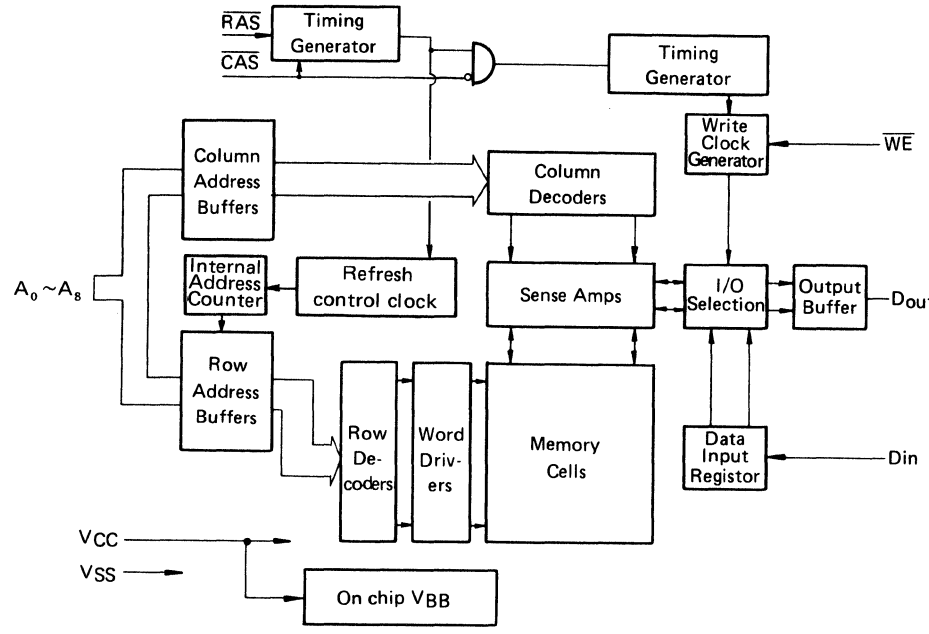
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		75	mA	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
REFRESH CURRENT Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		60	mA	
Nibble MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		25	mA	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = −5 mA)	V_{OH}	2.4		V	
Output low voltage (I_{OL} = 4.2 mA)	V_{OL}		0.4	V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_8, D_{IN})	C_{IN1}	5	7	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	7	10	pF
Output Capacitance (D_{OUT})	C_{OUT}	5	7	pF

Capacitance measured with Boonton Meter.

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AC CHARACTERISTICS

Notes 1, 2, 3 Under Recommended Operating conditions

Parameter	Symbol	Units	MSM41256-10		MSM41256-12		MSM41256-15		Note
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		230		280		
Read-write cycle time	t_{RWC}	ns	245		280		335		
Page mode cycle time	t_{PC}	ns	150		170		225		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	25	0	25	0	30	
Transition time	t_T	ns	3	35	3	35	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		100		120		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10,000	120	10,000	150	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10,000	60	10,000	75	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	20	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		0		
Row Address set-up time	t_{ASR}	ns	0		0		0		
Row Address hold time	t_{RAH}	ns	15		20		20		
Column Address set-up time	t_{ASC}	ns	0		0		0		
Column Address hold time	t_{CAH}	ns	15		20		20		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	65		85		95		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time	t_{RCH}	ns	0		0		0		
Write command set-up time	t_{WCS}	ns	0		0		0		8
Write command hold time	t_{WCH}	ns	40		45		50		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	80		95		120		
Write command pulse width	t_{WP}	ns	20		25		30		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		45		50		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		45		50		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		25		30		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	70		85		105		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	50		60		75		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	100		120		150		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		20		25		

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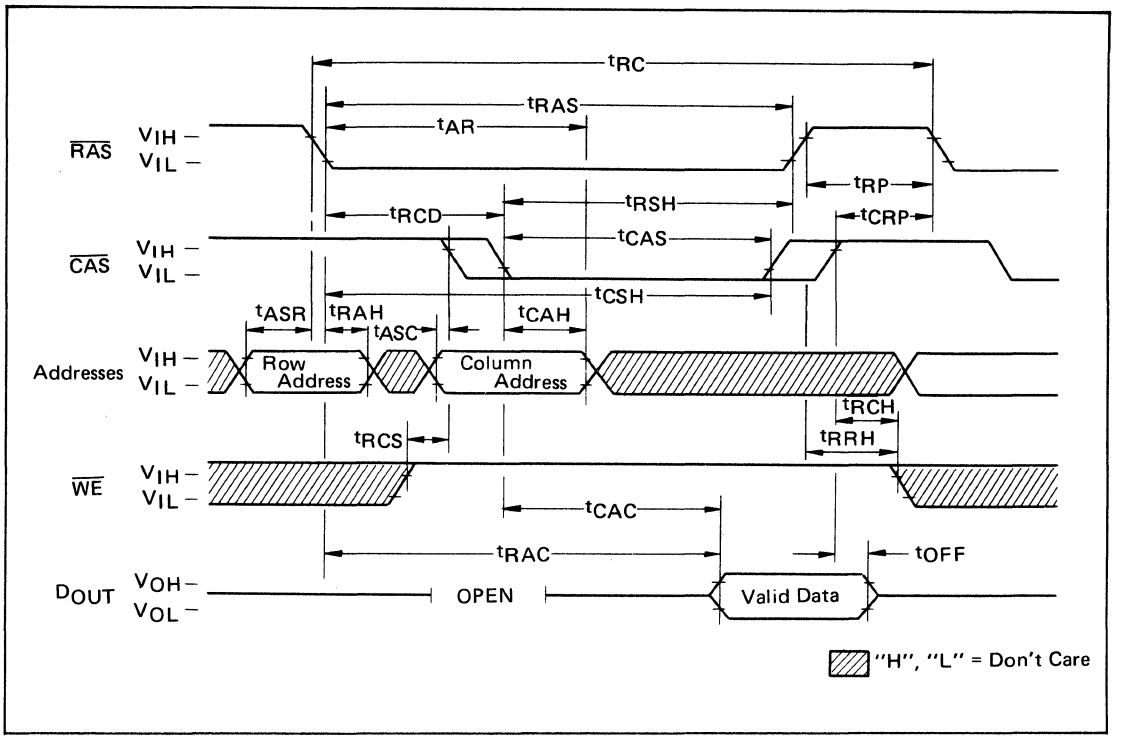
AC CARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Unit	MSM41256-10		MSM41256-12		MSM41256-15		Note
			Min.	Max.	Min.	Max.	Min	Max.	
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
Nibble Mode Read/Write Cycle Time	t_{NC}	ns	50		65		80		
Nibble Mode Read-Write Cycle Time	t_{NRWC}	ns	50		65		80		
Nibble Mode Access Time	t_{NCAC}	ns		20		30		40	
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCAS}	ns	20		30		40		
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	ns	20		25		30		
Nibble Mode $\overline{RAS}$ Hold Time	t_{NRSH}	ns	20		30		40		
Nibble Mode $\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$	t_{RNH}	ns	20		20		20		
Refresh Counter Test Cycle Time	t_{RTC}	ns	315		365		440		
Refresh Counter Test $\overline{CAS}$ Precharge Time	t_{CPT}	ns	50		60		70		
Refresh Counter Test $\overline{RAS}$ Pulse Width	t_{TRAS}	ns	215		255		310		

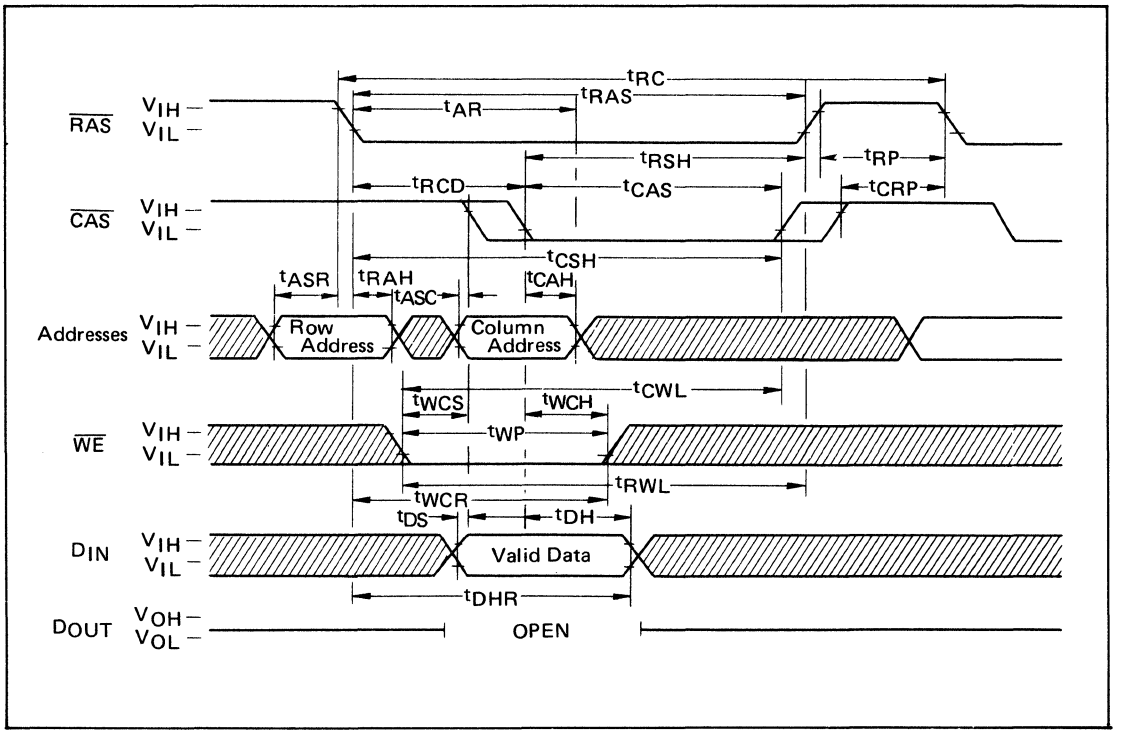
NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.
2) AC measurements assume t_T = 5 ns.
3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
5) Assumes that $t_{RCD} < t_{RCD}$ (max.)
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

READ CYCLE TIMING



WRITE CYCLE TIMING

(EARLY WRITE)



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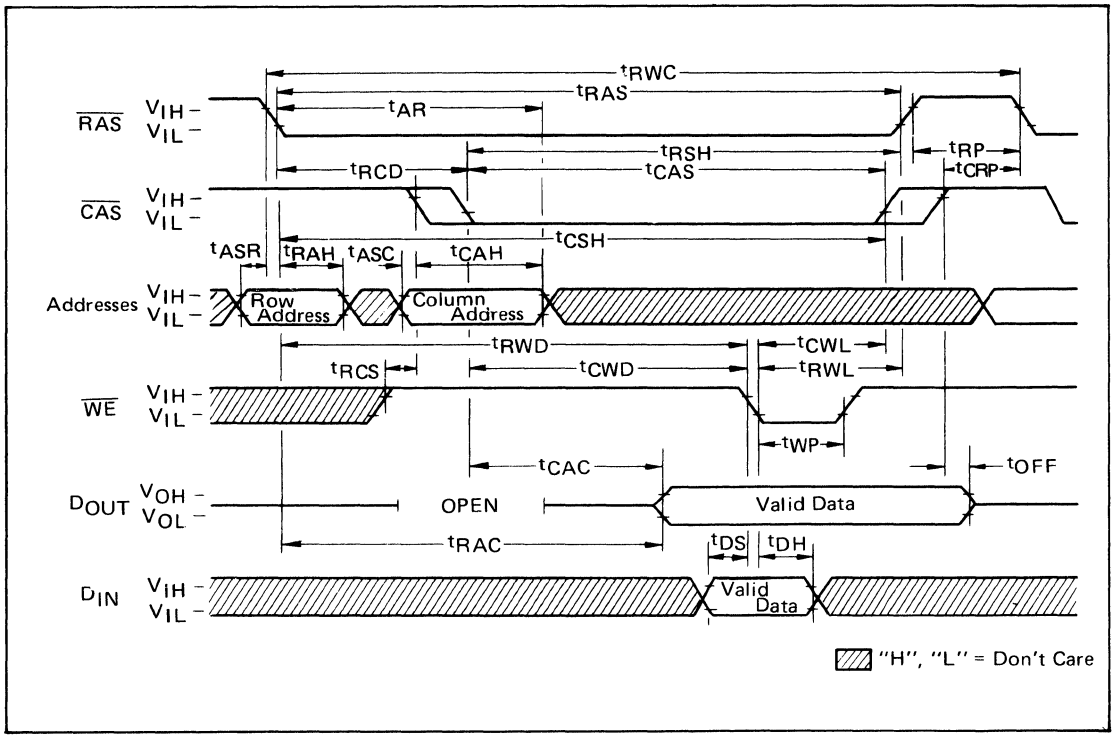
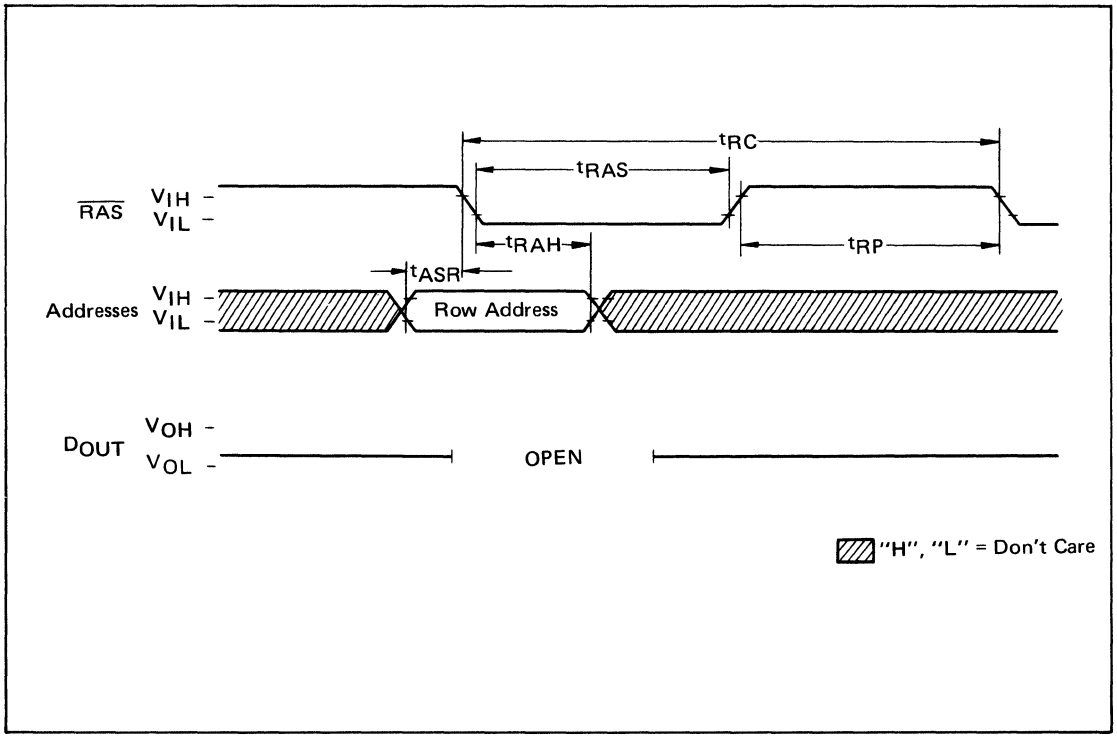
READ-WRITE/READ-MODIFY-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH TIMING

($\overline{CAS}$: VIH, $\overline{WE}$ & DIN: Don't care)



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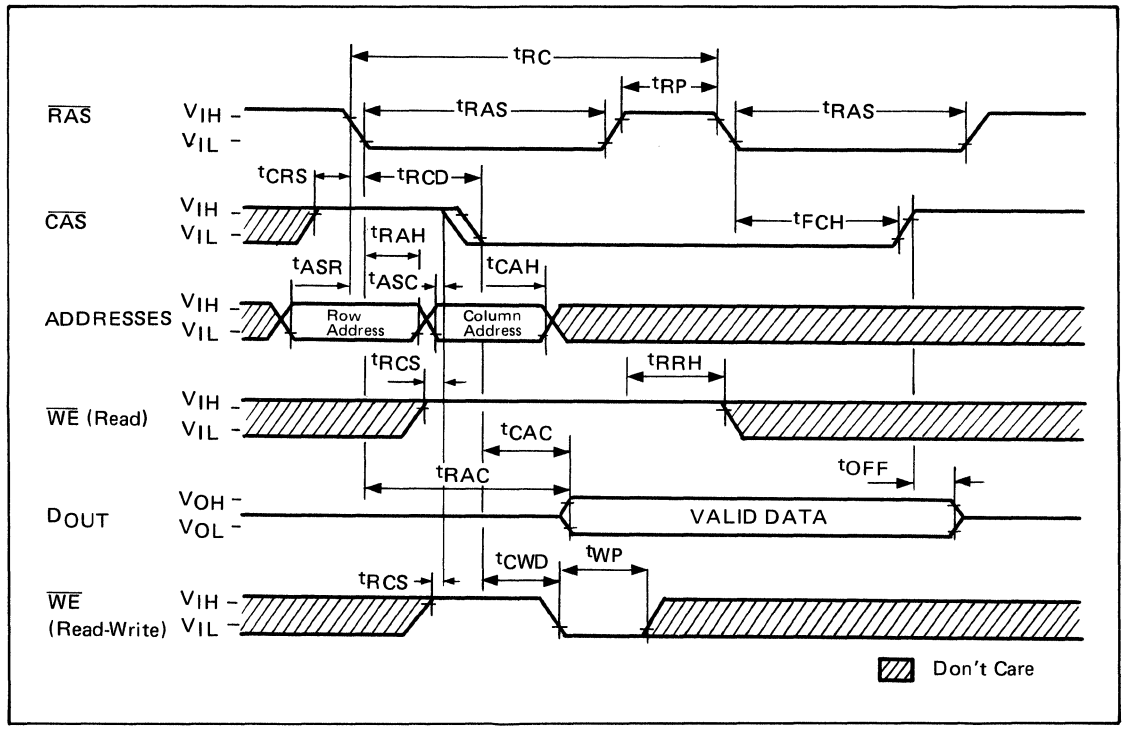
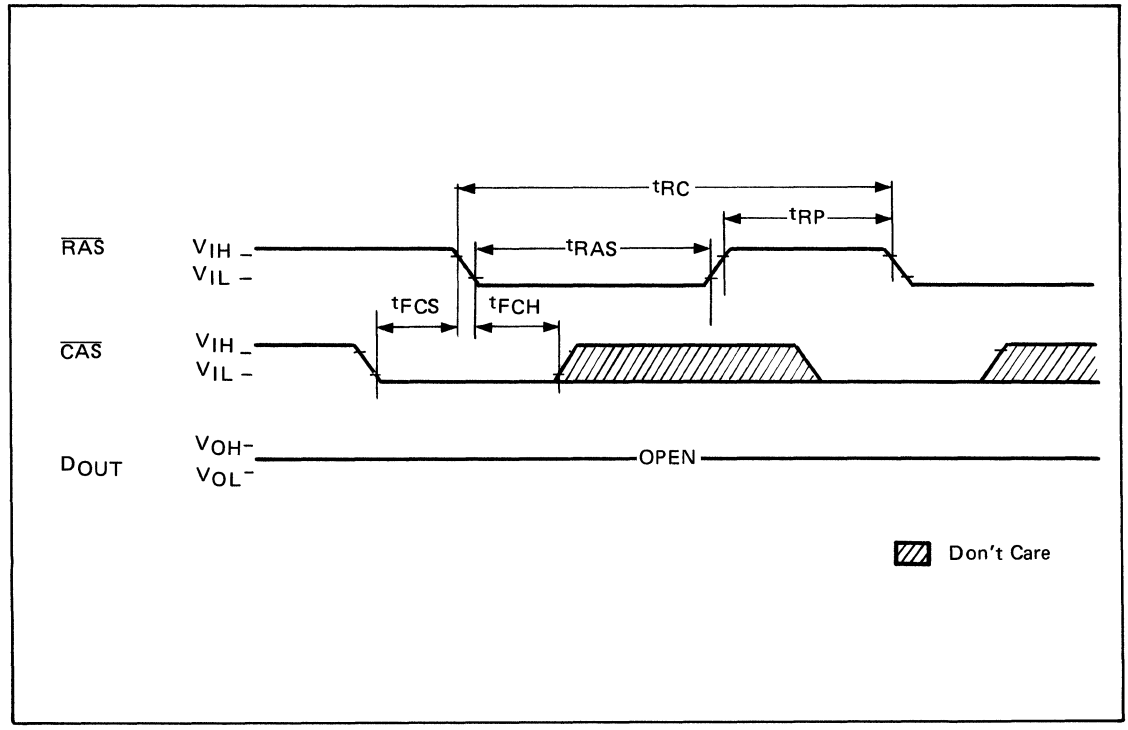
Hidden Refresh Cycle



"CAS-before-RAS" Refresh Cycle

NOTE: Address, WE, D_{IN} = Don't Care



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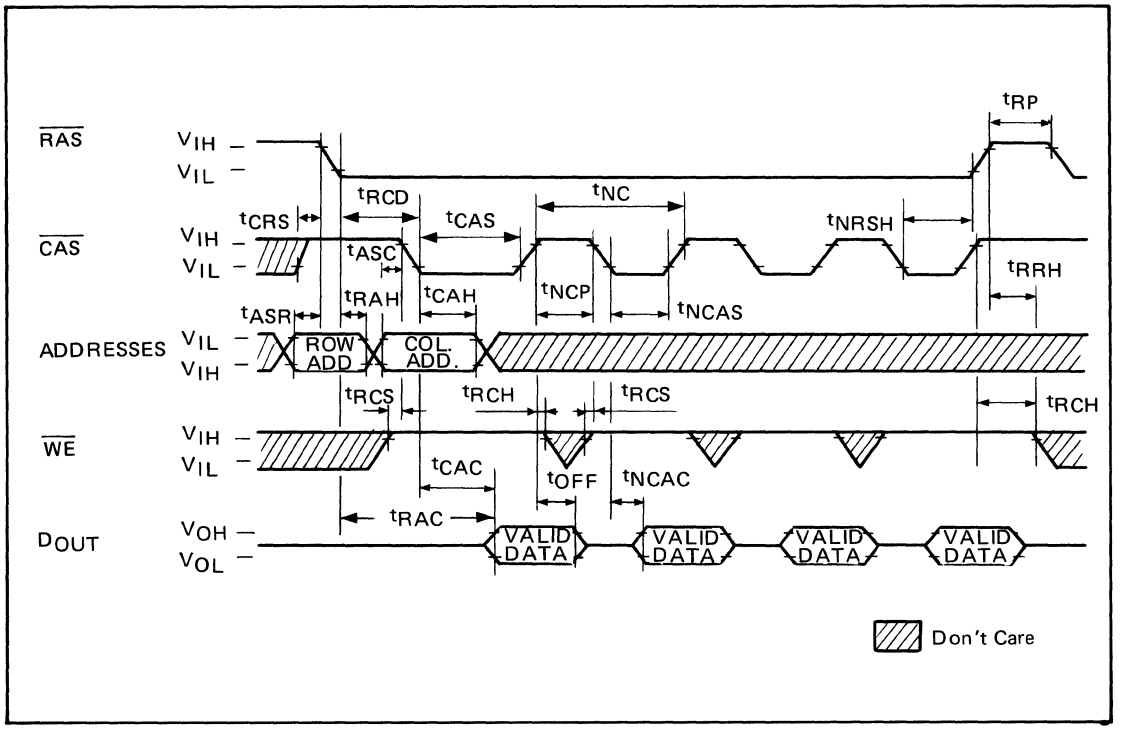
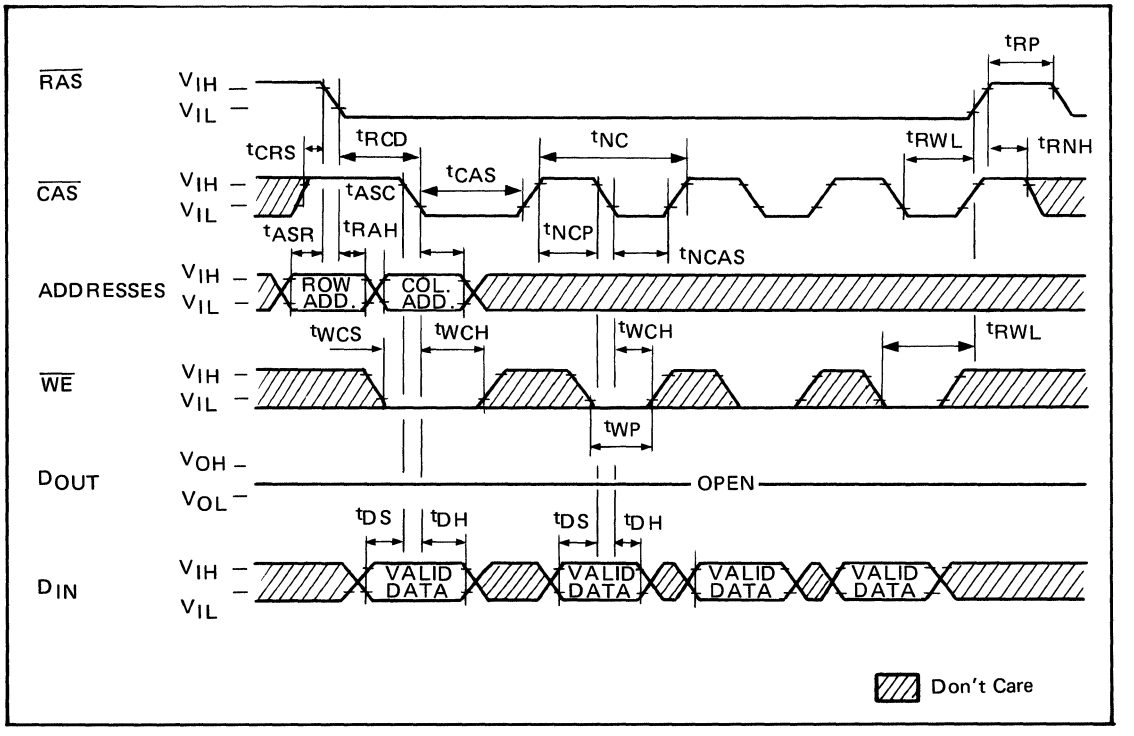
Nibble Mode Read Cycle



Nibble Mode Write Cycle



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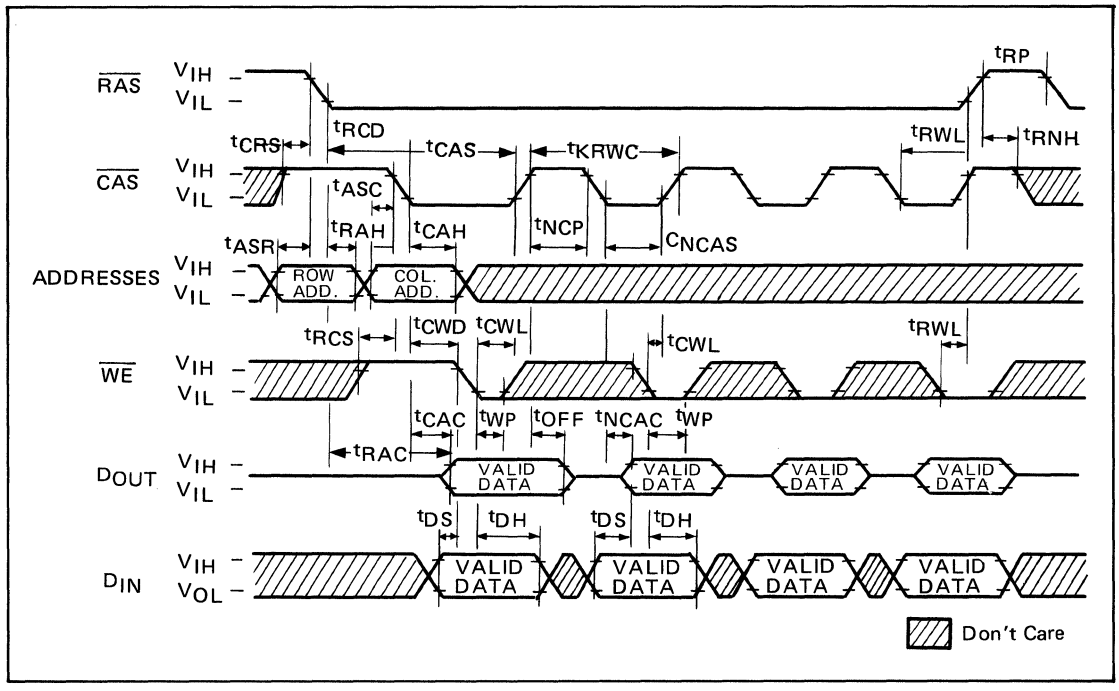
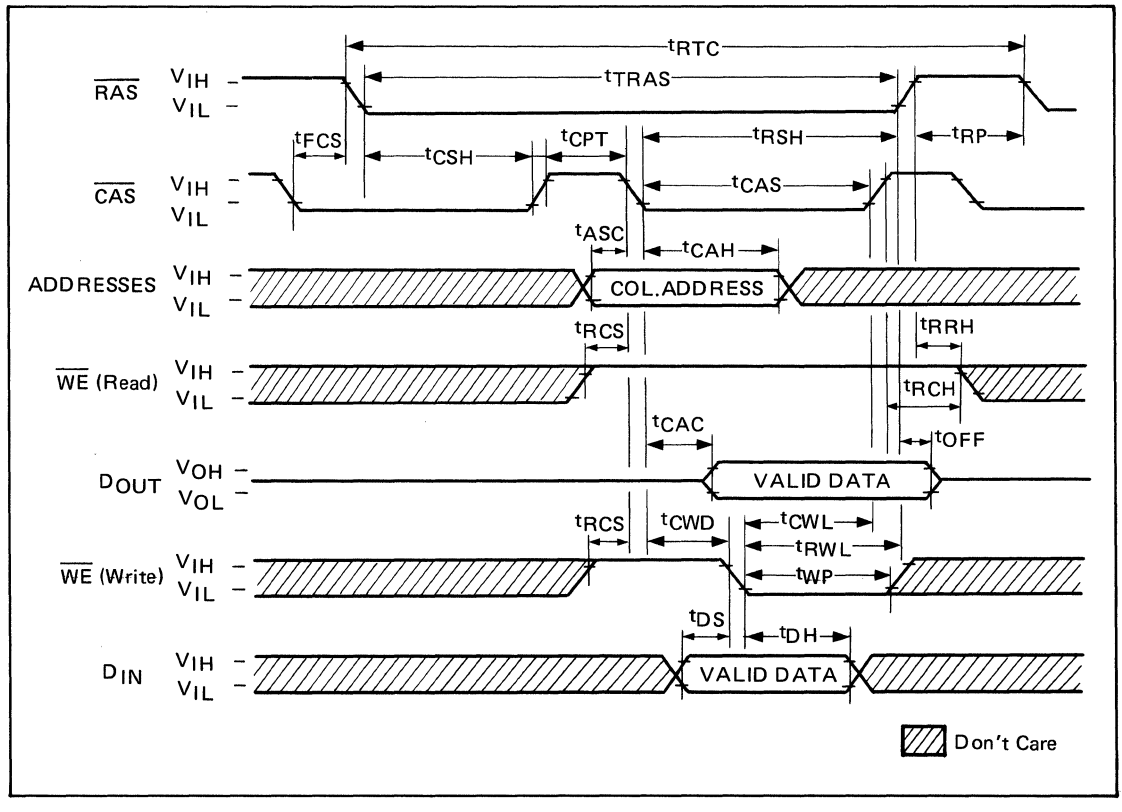
Nibble Mode Read-Write Cycle



"CAS-before-RAS" Refresh Counter Test Cycle



9

DESCRIPTION

Simple Timing Requirement

The MSM41256 has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSM41256 can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSM41256 has the minimal hold times of Address (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). And the MSM41256 can commit better memory system through-put during operations in an inter-leaved system. Furthermore, Oki has made timing requirements referenced to $\overline{RAS}$ non-restrictive and deleted from the data sheet, which includes t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. Therefore,the hold times of the Column Address, Din and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not ristricted by t_{RCD}.

Fast Read- While-Write cycle

The MSM41256 has the fast read while write cycle which is achieved by excellent control of the Tri-state output buffer in addition to the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MSM41256 goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MSM41256 goes to delayed write mode where the output contains the data from the cell selected and the data from Din is written into the cell selected. Therefore, very fast read write cycle becomes available.

Address Inputs

A total of eighteenbinary input address bits are required to decode any 1 of 262144 cell locations within MSM41256. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MSM41256 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ strobes the Data In (D_{IN}). In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is storbed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output byffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transistion of $\overline{RAS}$ when $t_{RCD(max)}$ is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max) Data remains valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8 RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1)

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation may be executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the tri-state control of D_{OUT} Pin is determined by the first normal access cycle.

The data output is controlled by only $\overline{WE}$ state referenced at $\overline{CAS}$ negative transition of the normal cycle (Nibble first bit). That is, when $t_{WCS} > t_{WCS}$ (min) is met, the data output will remain open circuit throughout the succeeding Nibble cycle regardless to $\overline{WE}$ state. Whereas, when $t_{CWD} > t_{CWD}$ (min) is met, the data output will contain data from the cell selected during regardless to $\overline{WE}$ state. The write operation is done during the period where $\overline{WE}$ and $\overline{CAS}$ clocks are low. Therefore, write operation can be done bit by bit during each nibble operation at any timing conditions of $\overline{WE}$ (t_{WCS} and t_{CWD}) at the normal cycle (nibble first bit).

Table 1

SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	
$\overline{RAS}/\overline{CAS}$ (normal mode)	1	0	10101010	0	101010 10	----- input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	101010 10	
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	101010 10	generated inter-
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	101010 10	nally
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	101010 10	sequence repeats

NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

$\overline{RAS}$ only Refresh

Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 through A_7) at least every 4 ms. $\overline{RAS}$ only refresh avoids any output during refresh because the buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 256 row-addresses (A_0 through A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on MSM41256 offers an alternate refresh method. If $\overline{CAS}$ is held on "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh opeation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ befoe $\overline{RAS}$ refresh operation.

Hidden Refresh

Hidden refresh cycle may takes place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. In MSM41256 hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always "low" when $\overline{RAS}$ goes to "low" in hidden refresh.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activted circuitry.

As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, after the $\overline{CAS}$ before $\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to "high" and goes to "low" again while $\overline{RAS}$ is held "low", the read and write operation are enabled. A memory cell address (consisting of a row address (9 bits) and a column address (9 bits)) to be accessed can be defined as follows:

* A ROW ADDRESS – Bits A_0 through A_7 are defined by the refresh counter.
  The other bit A_8 is set "high" internally.
* A COLUMN ADDRESS – All the bits A_0 through A_8 are defined by latching levels on A_0 throgh A_8 at the second falling edge of CAS.

SUGGESTED $\overline{CAS}$ before $\overline{RAS}$ COUNTER TEST PROCEDURE

The timing as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operation, 8 cycles are required.
(2) Write a test pattern of "low"s into memory cells at a single column address and 256 row addresses.
(3) By using read-modify-write cycle, read the "low" written at the last operation (Step (2)) and write a new "high" in the same cycle. This cycle is repeated 256 times, and "high"s are written into the 256 memory cells.
(4) Read the "high"s written at the last operation (Step (3)).
(5) Compliment the test pattern and repeat the steps (2), (3) and (4).

MOS STATIC RAMS

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MSM2114LRS

4096-BIT (1024 x 4) STATIC RAM (E3-S-006-32)

GENERAL DESCRIPTION

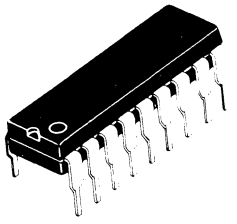
The Oki MSM2114L is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using Oki's reliable N-channel Silicon Gate MOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. Directly TTL compatible inputs, outputs and operation from a single +5V supply simplify system designs. Common data input/output pins using three-state outputs are provided.

The MSM2114L series is offered in an 18-pin dual-in-line plastic (RS Suffix) package. The series is guaranteed for operation from 0°C to 70°C.

FEATURES

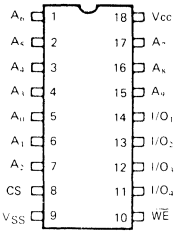
- Low Power Dissipation
- Single +5V Supply (±10% Tolerance)
- High Density 300-mil 18-Pin Package
- Fully Static Operation
- Common I/O Capability using Three-State Outputs
- Directly TTL Compatible
- N-channel Silicon Gate MOS Technology
- Interchangeable with Intel 2114L Devices

	2114L-2	2114L-3	2114L
Max. Access Time (NS)	200	300	450
Max. Power Dissipation (MW)	396	396	396



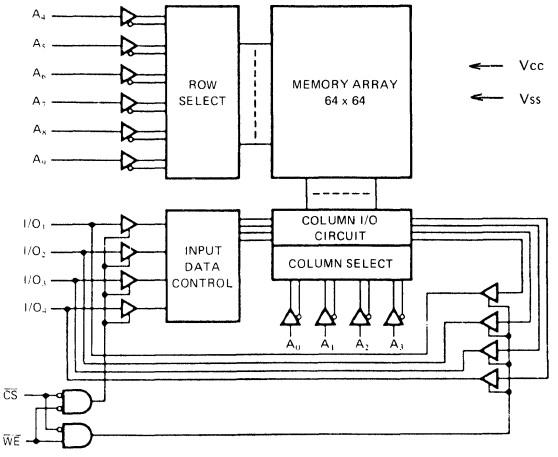
PIN CONFIGURATION

(Top View)



A_0 ~ A_9: Address Inputs
$\overline{WE}$: Write Enable
$\overline{CS}$: Chip Select
I/O_1-I/O_4: Data Input/Output
Vcc: +5V Supply
V_{SS} : Ground

FUNCTIONAL BLOCK DIAGRAM



$\overline{CS}$	$\overline{WE}$	I/O	Mode
H	X	Hi-Z	Not Selected
L	L	H	Write 1
L	L	L	Write 0
L	H	D-out	Read

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Temperature Under Bias	Topr	0 to +70	°C	
Storage Temperature	T_{stg}	−55 to +150	°C	
Supply Voltage	V_{CC}	−0.5 to +7	V	Respect to V_{SS}
Input Voltage	V_{IN}	−0.5 to +7	V	
Output Voltage	V_{OUT}	−0.5 to +7	V	
Power Dissipation	P_D	1.0	W	

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ±10%
Input Signal Level	V_{IH}	2.0	5	6.0	V	Respect to V_{SS}
	V_{IL}	−0.5	0	0.8	V	
Operating Temperature	T_{opr}	0		+70	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Load Current	I_{LI}			10	μA	V_{IN} = 0 to +5.5V
I/O Leakage Current	I_{LOL}			−10	μA	$\overline{CS}$ = 2.4V $V_{I/O}$ = 0.4V
I/O Leakage Current	I_{LOH}			10	μA	$\overline{CS}$ = 2.4V $V_{I/O}$ = 5.5V
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −0.2mA
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0mA
Power Supply Current	I_{CC}			72	mA	V_{CC} = 5.5V I/O = 0mA T_A = 0°C

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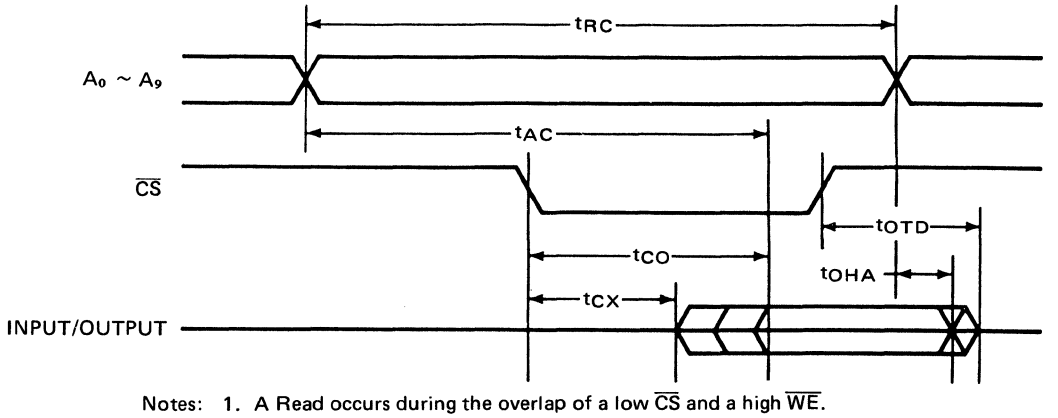
AC CHARACTERISTICS
READ CYCLE

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Parameter	Symbol	2114L-2RS		2114L-3RS		2114LRS		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	200		300		450		ns
Access Time	t_{AC}		200		300		450	ns
Chip Selection to Output Valid	t_{CO}		70		100		120	ns
Chip Selection to Output Active	t_{CX}	20		20		20		ns
Output 3-state from Deselection	t_{OTD}		60		80		100	ns
Output Hold from Address Change	t_{OHA}	10		10		10		ns



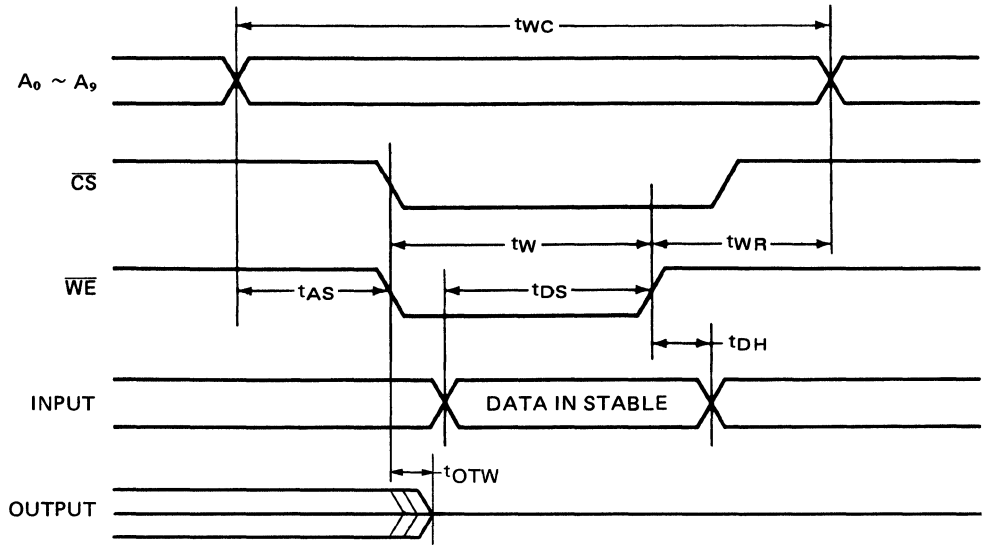
Notes:
1. A Read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.
3. Input Pulse Levels: 0.8V to +2.0V
4. Input Rise and Fall Time: 10ns
5. Timing Measurement Reference Levels: 1.5V
6. Output Load: 1 TTL Gate and C_L = 50pF

WRITE CYCLE

(V_{CC} = 5V ±10%, T_a = 0°C to 70°C)

Parameter	Symbol	2114L-2RS		2114L-3RS		2114LRS		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	200		300		450		ns
Write Time	t_W	120		150		200		ns
Write Release Time	t_{WR}	20		30		50		ns
Address Setup Time	t_{AS}	0		0		0		ns
Data Setup Time	t_{DS}	120		150		200		ns
Data Hold From Write Time	t_{DH}	0		0		0		ns
Write Enabled to Output in High Z	t_{OTW}		60		80		100	ns

WRITE CYCLE



Notes:
1. A Write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. Input Pulse Levels: 0.8V to +2.0V
3. Input Rise and Fall Time: 10ns
4. Timing Measurement Reference Levels: 1.5V
5. t_W: Overlap time of a low $\overline{CS}$ and low $\overline{WE}$
6. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
7. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
8. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
9. When I/O pins are Data output mode, don't force inverse signal to those pins.

CAPACITANCE

(T_a = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$		6	8	pF
Input Capacitance	C_{IN}		4	6	pF

Note: This parameter is periodically sampled and not 100% tested.

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MSM2128RS

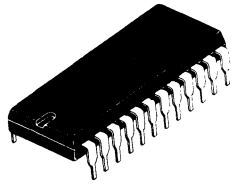
2 KW x 8 BIT STATIC RAM (E3-S-008-32)

GENERAL DESCRIPTION

OKI MSM2128 is a 16384 bits static Random Access Memory organized as 2048 words by 8 bits using Advanced N-channel Silicon Gate MOS technology. It uses fully static circuitry through out and no clocks or refresh required. The reduced standby power dissipation is automatically performed by CS control. Single +5 V Power supply. All inputs and outputs are directly TTL compatible. Common data I/O using three-state outputs. 24 pin package is pin compatible with 16 K UV Erasable Programmable ROM.

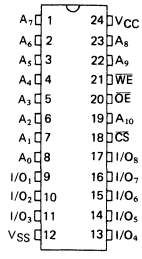
FEATURES

- Single power supply
- External clock and refresh operation not required
- Access time
  - MSM2128-12RS . . . 120ns (max)
  - MSM2128-15RS . . . 150ns (max)
  - MSM2128-20RS . . . 200ns (max)
- Low power dissipation
  - during operation . . . MSM2128-15RS/20RS
  - . . . 550 mW (max)
  - . . . MSM2128-12RS
  - . . . 660 mW (max)
  - during standby . . . 110 mW (max)
- TTL compatible I/O
- Three-state I/O
- Common data I/O capability
- Power down mode using chip select signal
- Convertibility of pins used in 16KEPROM MSM2716



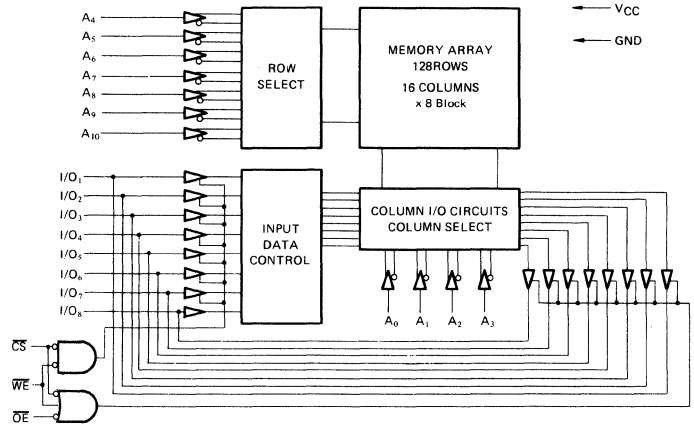
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{10}$: Address Inputs
$I/O_1 \sim I/O_8$: Data Input/Output
V_{CC}: Power (5V)
V_{SS}: Ground
$\overline{WE}$: Write Enable
$\overline{CS}$: Chip Select
$\overline{OE}$: Output Enable

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_{IN}	−0.5 to 7	V	
Operating Temperature	Topr	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	

DC AND OPERATING CHARACTERISTICS

(T_a = 0°C to + 70°C, V_{CC} = 5V ±10%, unless otherwise notes.)

Parameter	Symbol	2128-12RS			2128-15/20RS			Unit	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Input Load Current	I_{LI}	−10		10	−10		10	μA	V_{CC} = Max. V_{IN} = GND to V_{CC}
Output Leakage Current	I_{LO}	−10		10	−10		10	μA	$\overline{CS}$ = $\overline{OE}$ = V_{IH}, V_{CC} = Max. V_{out} = GND to V_{CC}
Operating Current	I_{CC}			120			100	mA	V_{CC} = Max. $\overline{CS}$ = V_{IL} I I/O = 0 mA t_{cyc} = Min.
Standby Current	I_{SB}			15			15	mA	V_{CC} = Min. to Max. $\overline{CS}$ = V_{IH}
Peak Power-on Current	I_{SBP}			20			20	mA	V_{CC} = GND to V_{CC} = Min. $\overline{CS}$ = Lower of V_{CC} or V_{IH}
Input Voltage	V_{IH}	2	5	6	2	5	6	V	Respect to V_{SS}
	V_{IL}	−0.5	0	0.8	−0.5	0	0.8	V	
Output Voltage	V_{OH}	2.4		V_{CC}	2.4		V_{CC}	V	I_{OH} = −1.0 mA
	V_{OL}			0.4			0.4	V	I_{OL} = 2.1 mA

Notes 1. Typical limits are at V_{CC} = 5V, T_a = 25°C, and specified loading.

AC CHARACTERISTICS

(T_a = 0°C to + 70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

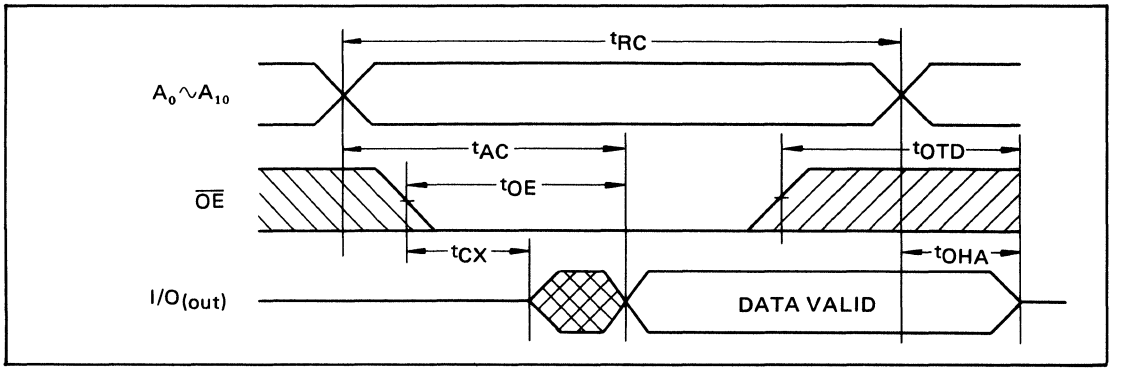
AC TEST CONDITIONS

Parameter	Conditions
Input High Level	2.0V
Input Low Level	0.8V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	C_L = 100 pF, 1TTL Gate

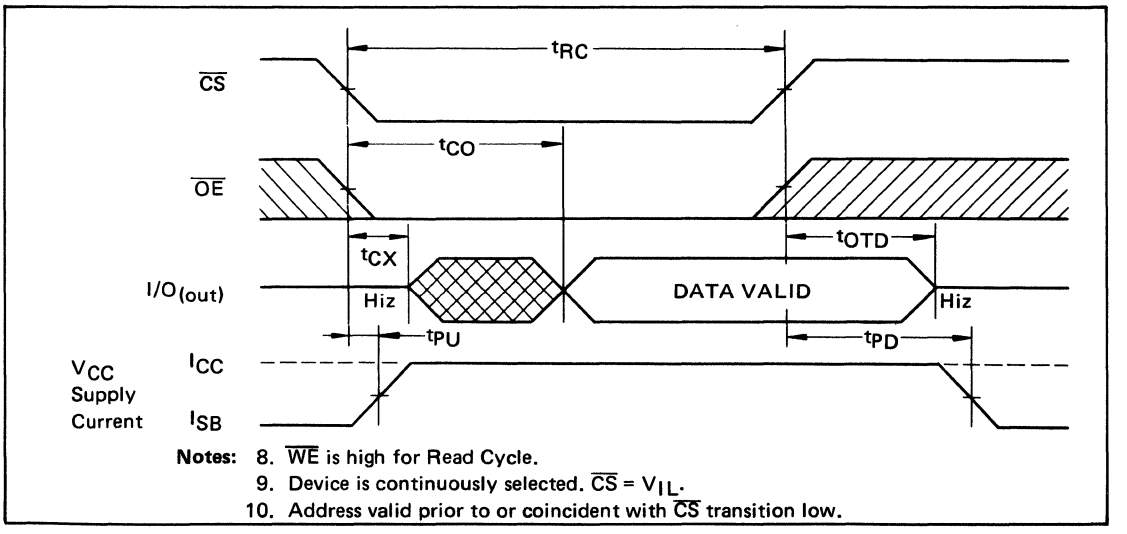
READ CYCLE [1]

Parameter	Symbol	2128-12RS		2128-15RS		2128-20RS		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	120		150		200		ns	
Address Access Time	t_{AC}		120		150		200	ns	
Output Enable to Output Delay	t_{OE}		50		60		70	ns	
Chip Select Access Time	t_{CO}		120		150		200	ns	
Chip Selection to Output in Low Z	t_{CX} [2]	10		10		10		ns	
Chip Selection to Output in High Z	t_{OTD} [3]	0	40	0	50	0	60	ns	
Output Hold from Address Time	t_{OHA}	10		10		10		ns	
Chip Select to Power Up Time	t_{PU}	0		0		0		ns	
Chip Select to Power Down Time	t_{PD}		50		60		80	ns	

READ CYCLE NO. 1 [8] [9]



READ CYCLE NO. 2 [8] [10]



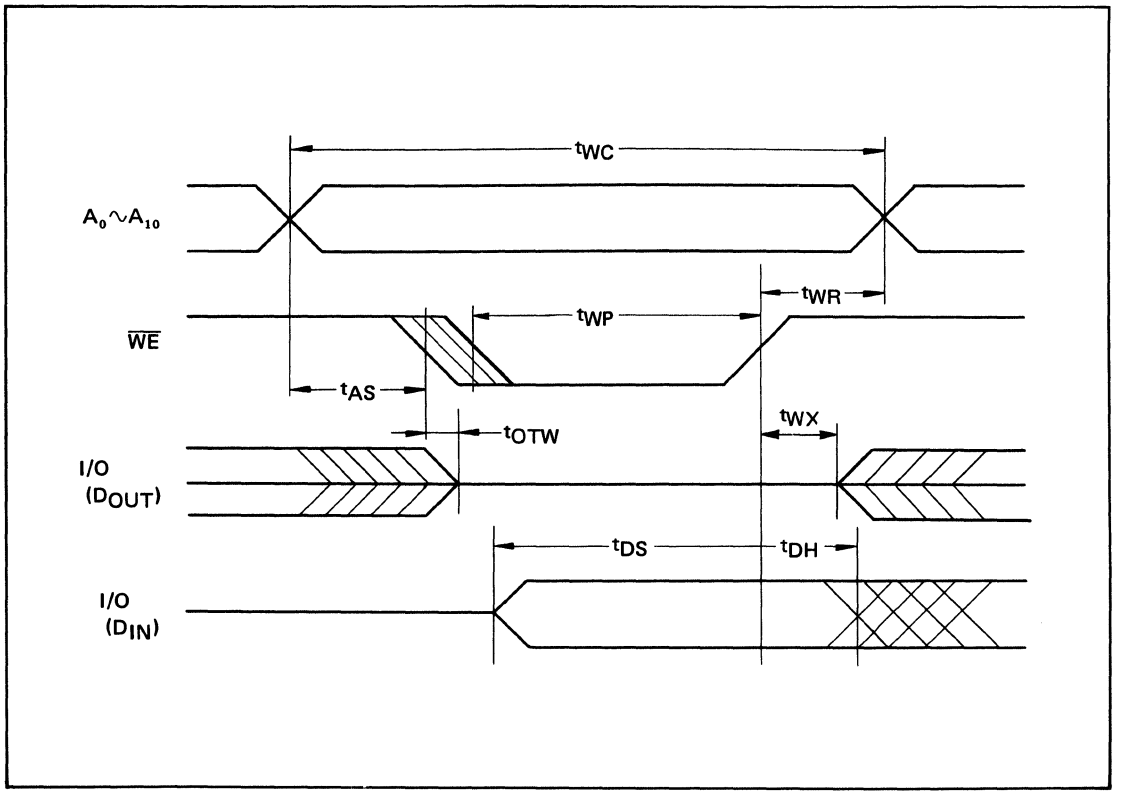
Notes: 8. $\overline{WE}$ is high for Read Cycle.
9. Device is continuously selected. $\overline{CS} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.

WRITE CYCLE (4)(5)

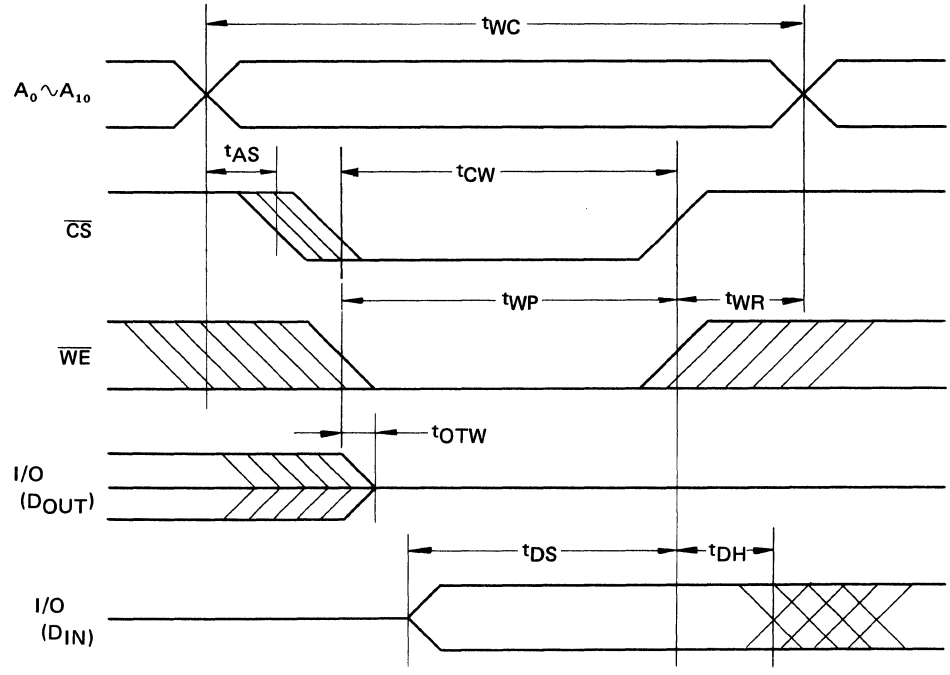
Parameter	Symbol	2128-12RS		2128-15RS		2128-20RS		Unit	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	120		150		200		ns	
Chip Selection to End of Write	t_{CW}	90		120		150		ns	
Address Setup Time	t_{AS}	20		20		20		ns	
Write Pulse Width	t_{WP}	60		80		100		ns	
Write Recovery Time	t_{WR}(6)	10		10		10		ns	
Data Valid to End of Write	t_{DS}(6)	50		70		90		ns	
Data Hold Time	t_{DH}(6)	10		15		15		ns	
Write Enabled to Output in High Z	t_{OTW}(7)	0	40	0	50	0	60	ns	
Output Active from End of White	t_{WX}	5		5		5		ns	

Notes
1. A read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
5. $\overline{OE}$ may be allowed in a Write Cycle both high and low.
6. t_{WR}, t_{DS}, and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
7. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.

WRITE CYCLE NO. 1(11)(13)



WRITE CYCLE NO. 2[12][13]



Notes 11. $\overline{WE}$ control mode
12. $\overline{CS}$ control mode
13. When I/O pins are Data output mode, don't force inverse signal to these pins.

FUNCTION TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	Output	Power
H	X	X	Not Selected	High Z	Standby
L	L	X	Write	High Z	Active
L	H	L	Read	D_{OUT}	Active
L	H	H	Not Selected	High Z	Active

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit	Conditions
Input/Output Capacitance	$C_{I/O}$		8	pF	$V_{I/O}$ = 0V
Input Capacitance	C_{IN}		6	pF	V_{IN} = 0V

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5114RS

4096-BIT (1024 x 4) CMOS STATIC RAM (E3-S-010-32)

GENERAL DESCRIPTION

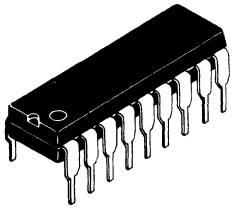
The Oki MSM5114 is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using Oki's reliable Silicon Gate CMOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. Microwatt power dissipation typical of all CMOS is exhibited in all static states. Directly TTL compatible inputs, outputs and operation from a single +5V supply simplify system designs. Common data input/output pins using three-state outputs are provided.

The MSM5114 series is offered in an 18-pin plastic (RS suffix) package. The series is guaranteed for operation from 0°C to 70°C and over a 4V to 6V power supply range.

FEATURES

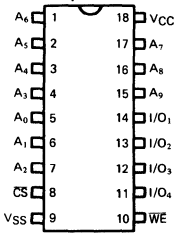
- Fully Static Operation
- Low Power Dissipation
  40μW Max. Standby Power
  192 mW/MHz Max. Operating Power
- Data Retention to V_{CC}=2V
- Single 4 ~ 6V Power Supply
- High Density 300-mil 18-Pin Package
- Common I/O Capability using Three-State Outputs
- Directly TTL/CMOS Compatible
- Silicon Gate CMOS Technology
- Interchangeable with Intel 2114L Devices

	5114-2	5114-3	5114
Max. Access Time (NS)	200	300	450
Max. Operating Power (MW/MHz)	192	192	192
Max. Standby Power (μW)	40	40	40



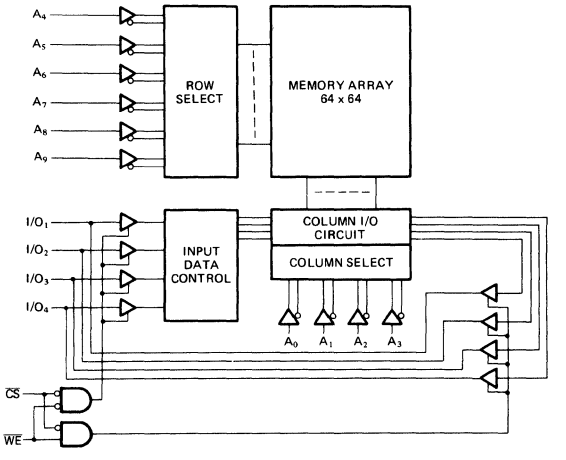
PIN CONFIGURATION

(Top View)



$\overline{A_0}$ To A_9: Address Inputs
$\overline{WE}$: Write Enable
$\overline{CS}$: Chip Select
$I/O_1 \sim I/O_4$: Data Input/Output
V_{CC}: +5V Supply
VSS : Ground

FUNCTIONAL BLOCK DIAGRAM



$\overline{CS}$	$\overline{WE}$	I/O	Mode
H	X	Hi-Z	Not Selected
L	L	H	Write 1
L	L	L	Write 0
L	H	D-out	Read

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to VSS
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Data I/O Voltage	V_D	−0.3 to V_{CC} + 0.3	V	
Storage Temperature	T_{stg}	−55 to 150	°C	

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operations of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4	5	6	V	5V ± 20%
Input Signal Level	V_{IH}	2.4	5	V_{CC}	V	Respect to V_{SS}
	V_{IL}	−0.3	0	0.8	V	
Operating Temperature	T_{opr}	0		70	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%; Ta = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Load Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Data I/O Leakage Current	I_{LO}	−1		1	μA	$V_{I/O}$ = 0 to V_{CC}
Output High Voltage	V_{OH}	4.2			V	I_{OUT} = −40 μA
Output Low Voltage	V_{OL}			0.4	V	I_{OUT} = 1.6 mA
Output High Current	I_{OH}	−1.0			mA	V_{OUT} = 2.4V
Standby Supply Current	I_{CCS}		0.2	50	μA	V_{IN} = 0 or V_{CC}, $V_{\overline{CS}}$ = V_{CC}
Operating Supply Current	I_{CC}		19	35	mA	V_{IN} = 0 or V_{CC}, t_{RC} = 1 μs

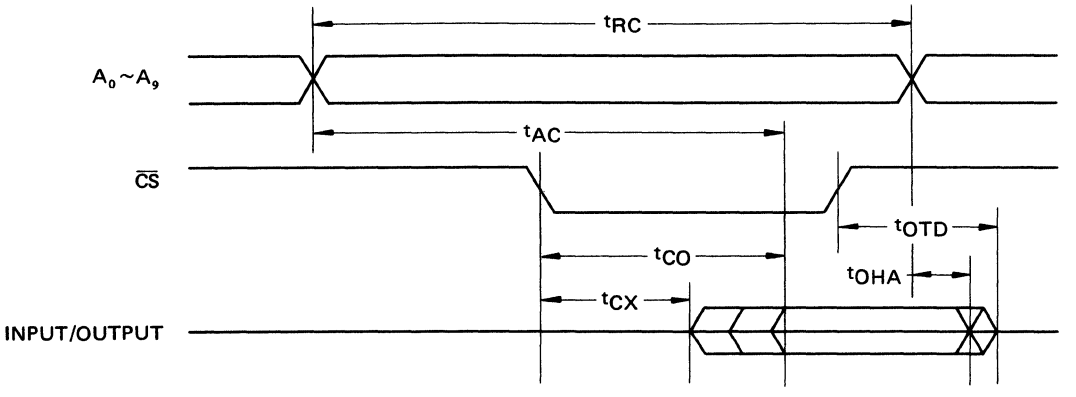
AC CHARACTERISTICS

READ CYCLE

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Parameter	Symbol	5114-2		5114-3		5114		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	200		300		450		ns
Access Time	t_{AC}		200		300		450	ns
Chip Selection to Output Valid	t_{CO}		200		300		450	ns
Chip Selection to Output Active	t_{CX}	20		20		20		ns
Output 3-state from Deselection	t_{OTD}		60		80		100	ns
Output Hold from Address Change	t_{OHA}	10		10		10		ns

READ CYCLE



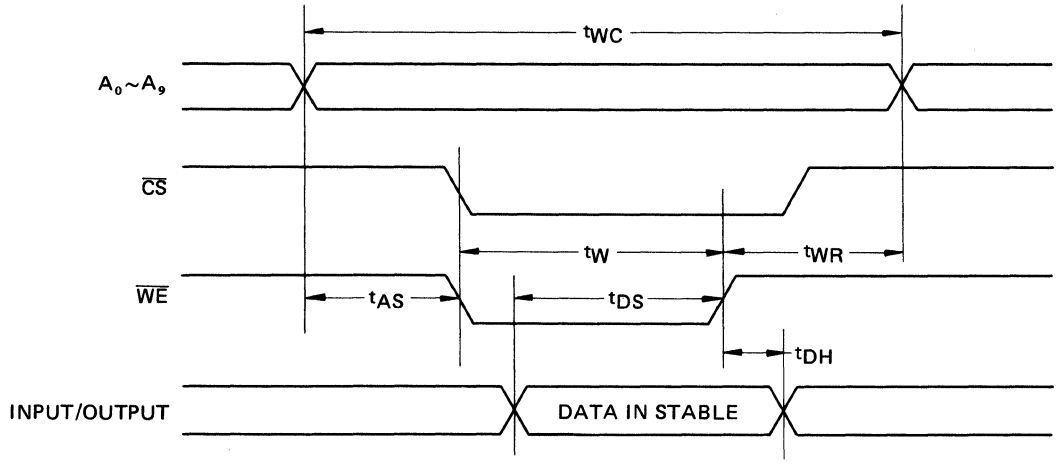
Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$ and high $\overline{WE}$.
2. Input Pulse levels: 0.8V to +2.4V
3. Input Rise and Fail Time: 10 ns
4. Timing Measurement Reference Levels: 1.5V
5. Output Load: 1 TTL Gate and C_L = 50 pF

WRITE CYCLE

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Parameter	Symbol	5114-2		5114-3		5114		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	200		300		450		ns
Write Time	t_W	150		190		250		ns
Write Release Time	t_{WR}	20		30		50		ns
Address Setup Time	t_{AS}	20		20		20		ns
Data Setup Time	t_{DS}	120		150		200		ns
Data Hold From Write Time	t_{DH}	10		10		10		ns

WRITE CYCLE



Notes:
1. A Write occurs during the overlap of a low $\overline{CS}$ and low $\overline{WE}$.
2. Input Pulse Levels: 0.8V to +2.4V
3. Input Rise and Fall Time: 10 ns
4. Timing Measurement Reference Levels: 1.5V
5. t_W: Overlap time of a low $\overline{CS}$ and low $\overline{WE}$.
6. t_{AS}: Low $\overline{WE}$ from address or low $\overline{CS}$ from address
7. t_{WR}, t_{DS} and t_{DH} are defined from High CS or High $\overline{WE}$, whichever occurs first.

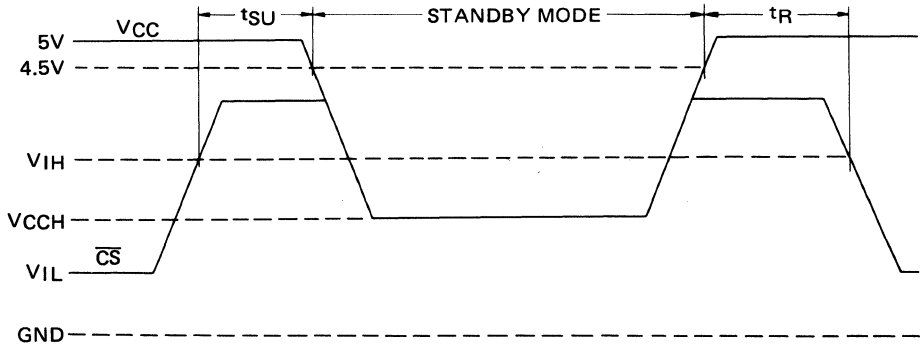
LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	V_{IN} = 0 or V_{CC}, $V_{\overline{CS}} = V_{CC}$
Data Retention Current	I_{CCH}		0.1	20	μA	V_{CC} = 2V $V_{CS} = V_{CC}$ V_{IN} = 0V or V_{CC}
$\overline{CS}$ to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

9

LOW V_{CC} DATA RETENTION WAVEFORM



CAPACITANCE

($T_a = 25°C$, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			10	pF
Input Capacitance	C_{IN}			8	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5104RS

4096-BIT (4096 x 1) CMOS STATIC RAM (E3-S-011-32)

GENERAL DESCRIPTION

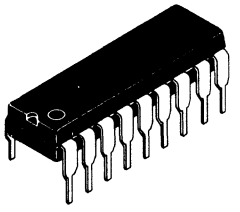
The Oki MSM5104 is a 4096-bit static Random Access Memory organized as 4096 words by 1 bit using Oki's reliable Silicon Gate CMOS technology. Microwatt power dissipation typical of all CMOS is exhibited in all static state. Directly TTL compatible inputs, output, operation from a single +5 V supply and on-chip address-data registers simplify system designs.

The MSM5104 series is offered in an 18-pin plastic (RS suffix) package. The series is guaranteed for operation from 0°C to 70°C and over a 4 V to 6 V power supply range.

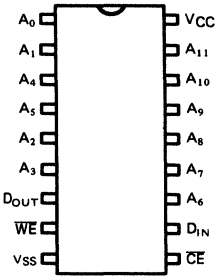
FEATURES

- Low Power Dissipation
  40μW Max. Standby Power
  33mW/MHz Max. Operating Power
- Data Retention to V_{CC}=2V
- Single 4 ~ 6V Power Supply
- High Density 300-mil 18-Pin Package
- On-Chip Address and Data Registers
- Separate Data Input and Output
- Three-State Ouput
- Directly TTL/CMOS Compatible
- Silicon Gate CMOS Technology
- Pin-compatible with Mostek 4104, Interchangeable with Harris 6504

	5104-2	5104-3
Max. Access Time (NS)	200	300
Max. Operating Power (MW/MHz)	33	33
Max. Standby Power (μ)	40	40

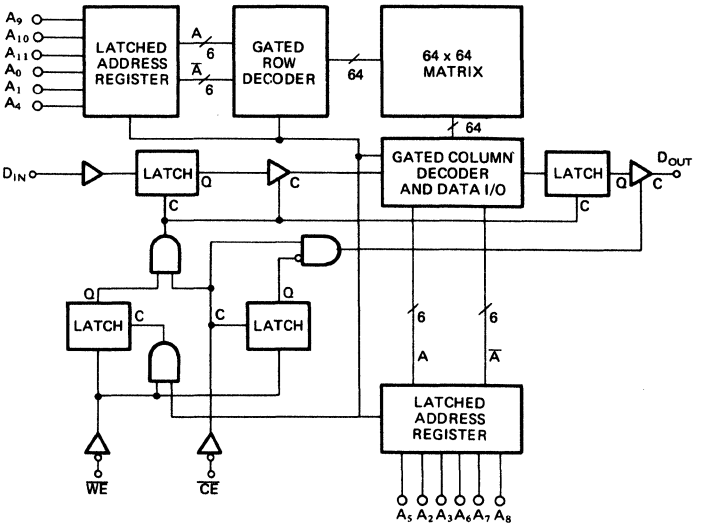


PIN CONFIGURATION



A_0 To A_{11}: Address Inputs
$\overline{WE}$: Write Enable
$\overline{CE}$: Chip Enable
D_{IN}: Data Input
D_{OUT}: Data Output
V_{CC}: +5V Supply
V_{SS}: Ground

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 7.0	V
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V
Output Voltage	V_{OUT}	0 to V_{CC}	V
Storage Temperature	T_{stg}	−55 to 150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4	5	6	V	5V ± 20%
Input Signal Level	V_{IH}	2.4	5	V_{CC}	V	Respect to V_{SS}
	V_{IL}	−0.3	0	0.8	V	
Operating Temperature	T_{opr}	0		70	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%; Ta = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Load Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−1		1	μA	$V_{I/O}$ = 0 to V_{CC}
Output High Voltage	V_{OH}	4.2			V	I_{OUT} = −40μA
Output Low Voltage	V_{OL}			0.4	V	I_{OUT} = 1.6mA
Output High Current	I_{OH}	−1.0			mA	V_{OUT} = 2.4V
Standby Supply Current	I_{CCS}		0.2	50	μA	V_{IN} = 0 or V_{CC}
Operating Supply Current	I_{CC}			6	mA	V_{IN} = 0 or V_{CC}, t_{RC} = 1 μs

AC CHARACTERISTICS

(V_{CC}=5V±10%, T_a = 0°C to +70°)

Parameter	Symbol	5104-2		5104-3		Unit
		Min.	Max.	Min.	Max.	
Read/Write Cycle Time	t_{RC}, t_{WC}	300		420		ns
Chip Enable Access Time	t_{AC}		200		300	ns
Chip Enable Pulse Width	t_{CE}	200		300		ns
Chip Enable Off Time	t_{CC}	100		120		ns
Address Hold Time	t_{AH}	40		50		ns
Address Setup Time	t_{AS}	0		0		ns
Output Disable Time	t_{OFF}	0	70	0	100	ns
Write Enable Pulse Width	t_{WP}	100		130		ns
Write Enable Setup Time	t_{WS}	0		0		ns

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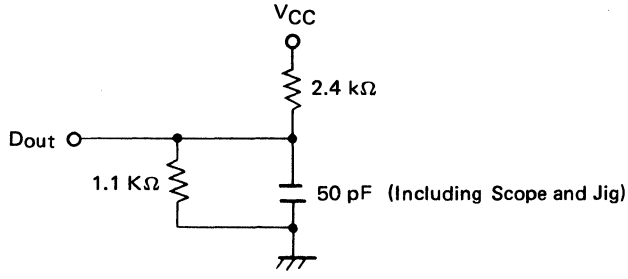
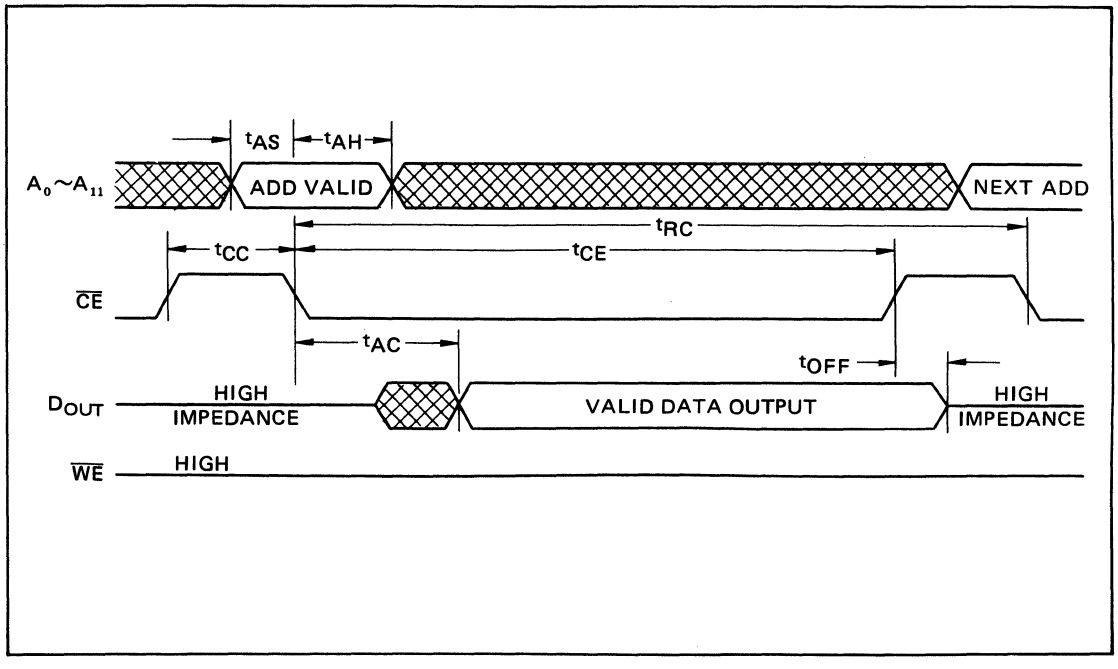
Parameter	Symbol	5104-2		5104-3		Unit
		Min.	Max.	Min.	Max.	
Write Enable Hold Time	t_{WH}	120		150		ns
Data Setup Time	t_{DS}	0		0		ns
Data Hold Time	t_{DH}	60		80		ns
Data Valid Time to Write Pulse	t_{DV}	0		0		ns
Write Enable Read Time	t_{WCL}	150		200		ns

AC TEST CONDITIONS

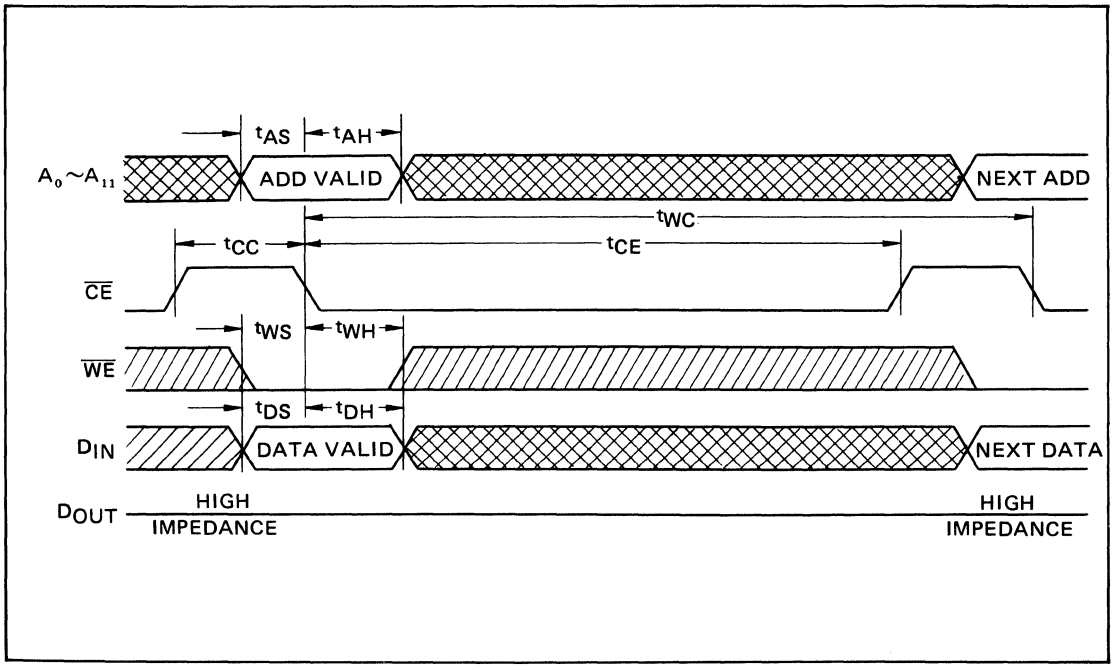
Input Pulse Levels: 0.8V to 2.4V
Timing Measurement Reference Levels: 1.5V
Input Rise and Fall Time: 10 ns



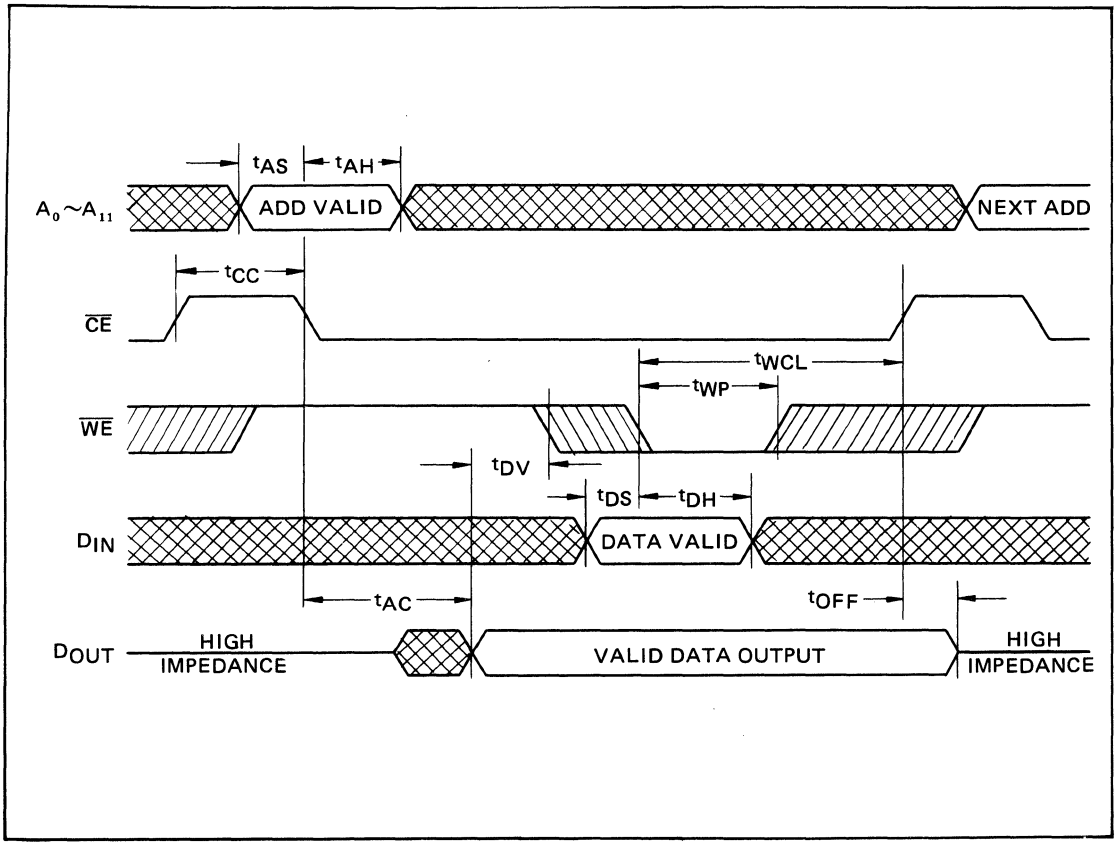
READ CYCLE



EARLY WRITE CYCLE



READ MODIFY WRITE CYCLE



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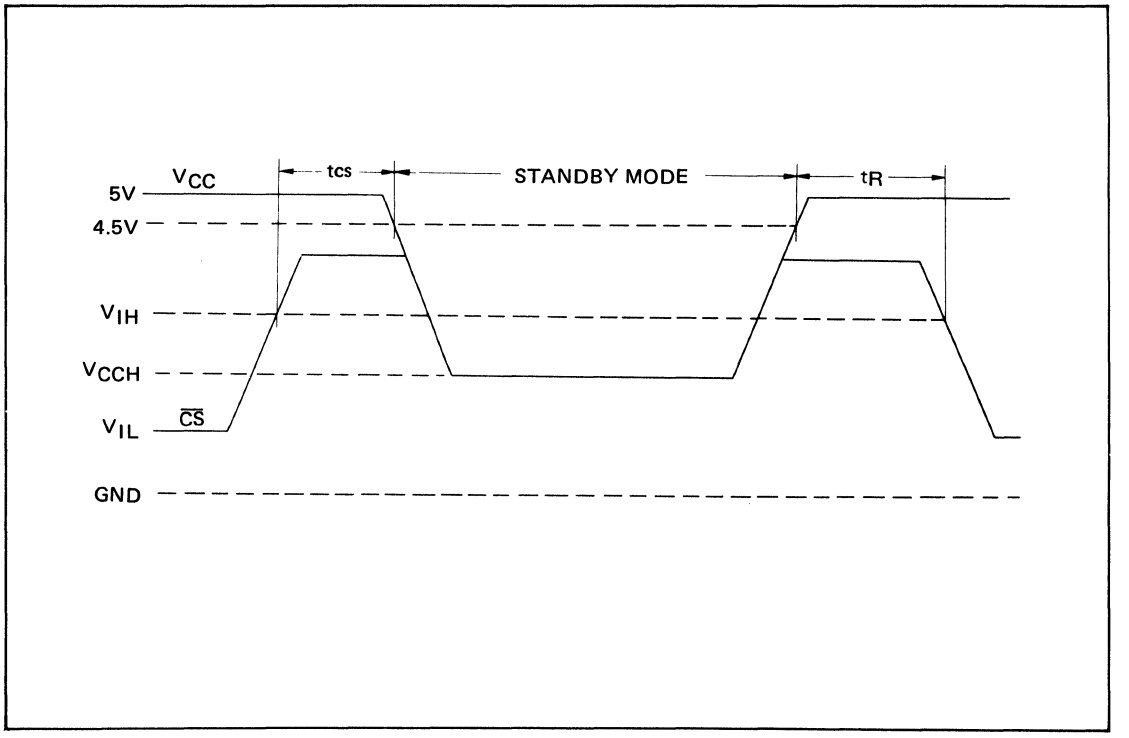
LOW V_{CC} DATA RETENTION CHARACTERISTICS

(Ta = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	V_{IN} = 0V or V_{CC}
Data Retention Current	I_{CCH}		0.1	20	μA	V_{CC} = 2V $V_{\overline{CE}}$ = V_{CC} V_{IN} = 0V or V_{CC}
$\overline{CE}$ to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

LOW V_{CC} DATA RETENTION WAVEFORM



9

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			10	pF
Input Capacitance	C_{IN}			8	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5115RS

4096-BIT (1024 x 4) CMOS STATIC RAM (E3-S-012-32)

GENERAL DESCRIPTION

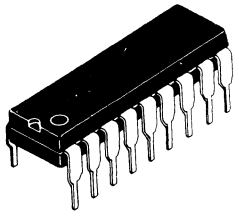
The Oki MSM5115 is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits using Oki's reliable Silicon Gate CMOS technology. Microwatt power dissipation typical of all CMOS is exhibited in all static states. Directly TTL compatible inputs, outputs, operation from a single +5 V supply and on-chip address registers simplify system designs. Common data input/output pins using three-state outputs are provided.

The MSM5115 series is offered in an 18-pin plastic (RS suffix) package. The series is guaranteed for operation from 0°C to 70°C and over a 4 V to 6 V power supply range.

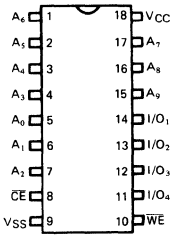
FEATURES

- Low Power Dissipation
  40μW Max. Standby Power
  33mW/MHz Max. Operating Power
- Data Retention to V_{CC} = 22V
- Single 4 ~ 6V Power Supply
- High Density 300-mil 18-Pin Package
- On-Chip Address Register
- Common I/O Capability using Three- State Outputs
- Directly TTL/CMOS Compatible
- Silicon Gate CMOS Technology
- Pin-compatible with Intel 2114, Interchangeable with Harris 6514

	5114-2	5115-3
Max. Access Time (NS)	200	300
Max. Operating Power (MW/MHz)	33	33
Max. Standby Power (μW)	40	40

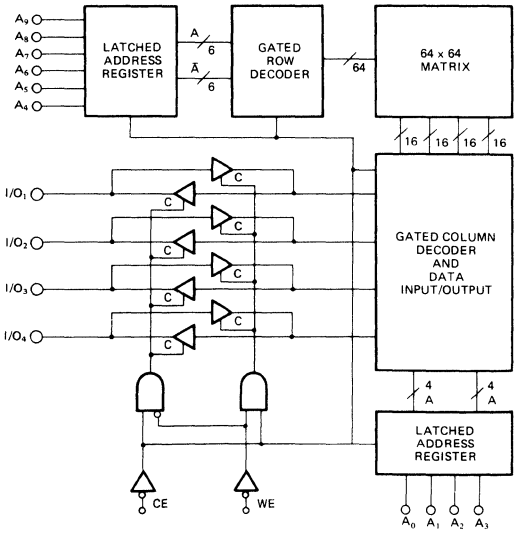


PIN CONFIGURATION



$\overline{A_0}$ To A_9 : Address Inputs
$\overline{WE}$: Write Enable
$\overline{CE}$: Chip Enable
$I/O_1 \sim I/O_4$: Data Input/Output
V_{CC}: +5V Supply
VSS : Ground

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 7.0	V
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V
Data I/O Voltage	V_D	−0.3 to V_{CC} + 0.3	V
Storage Temperature	T_{stg}	−55 to 150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4	5	6	V	5V ± 20%
Input Signal Level	V_{IH}	2.4	5	V_{CC}	V	Respect to V_{SS}
	V_{IL}	−0.3	0	0.8	V	
Operating Temperature	T_{opr}	0		70	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%; T_a = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Load Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Data I/O Leakage Current	I_{LO}	−1		1	μA	$V_{I/O}$ = 0 to V_{CC}
Output High Voltage	V_{OH}	4.2			V	I_{OUT} = −40μA
Output Low Voltage	V_{OL}			0.4	V	I_{OUT} = 1.6mA
Output High Current	I_{OH}	−1.0			mA	V_{OUT} = 2.4V
Standby Supply Current	I_{CCS}		0.2	50	μA	V_{IN} = 0 or V_{CC}
Operating Supply Current	I_{CC}			6	mA	V_{IN} = 0 or V_{CC}, t_{RC} = 1 μs

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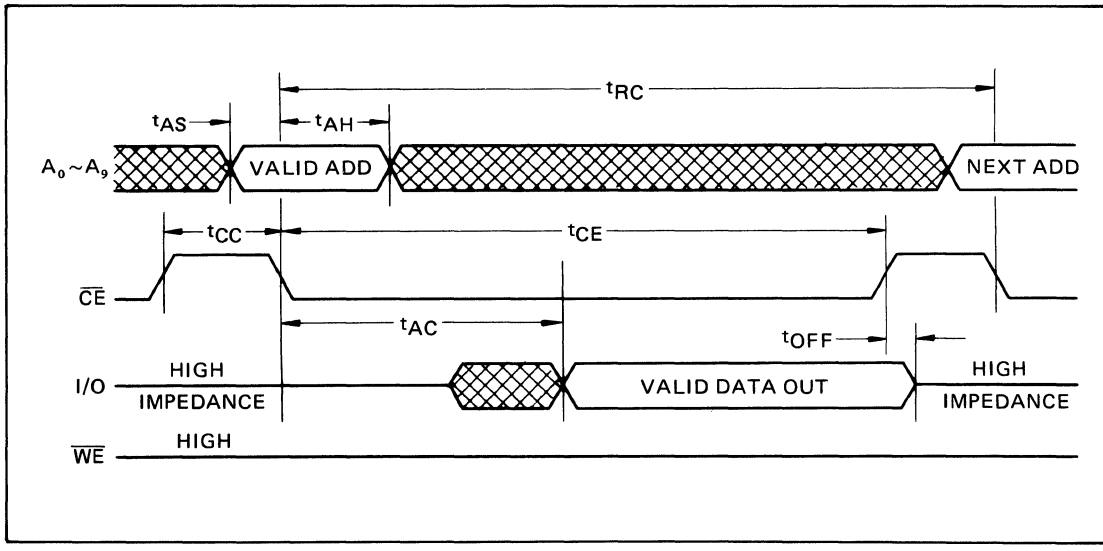
AC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

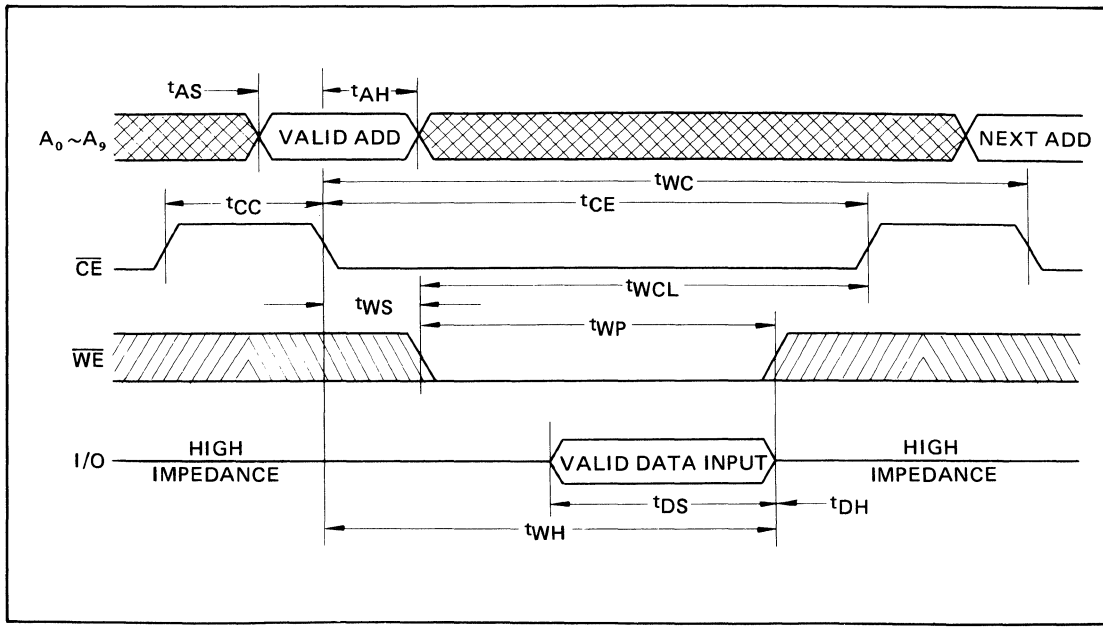
Parameter	Symbol	5115-2		5115-3		Unit
		Min.	Max.	Min.	Max.	
Read/Write Cycle Time	t_{RC}, t_{WC}	300		420		ns
Chip Enable Access Time	t_{AC}		200		300	ns
Chip Enable Pulse Width	t_{CE}	200		300		ns
Chip Enable Off Time	t_{CC}	100		120		ns
Address Hold Time	t_{AH}	40		50		ns
Address Setup Time	t_{AS}	0		0		ns
Output Disable Time	t_{OFF}	0	70	0	100	ns
Write Enable Pulse Width	t_{WP}	100		130		ns
Write Enable Setup Time	t_{WS}	0		0		ns

Parameter	Symbol	5115-2		5115-3		Unit
		Min.	Max.	Min.	Max.	
Write Enable Hold	t_{WH}	170		250		ns
Data Setup Time	t_{DS}	100		130		ns
Data Hold Time	t_{DH}	0		0		ns
Data Valid Time to Write Pulse	t_{DV}	0		0		ns
Write Enable Read Time	t_{WCL}	150		200		ns

READ CYCLE



WRITE CYCLE



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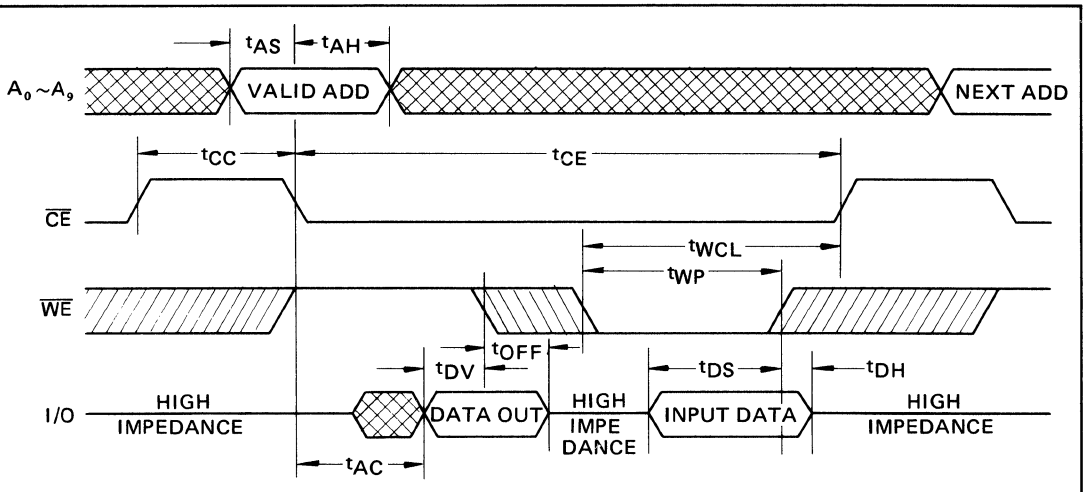
READ MODIFY WRITE CYCLE



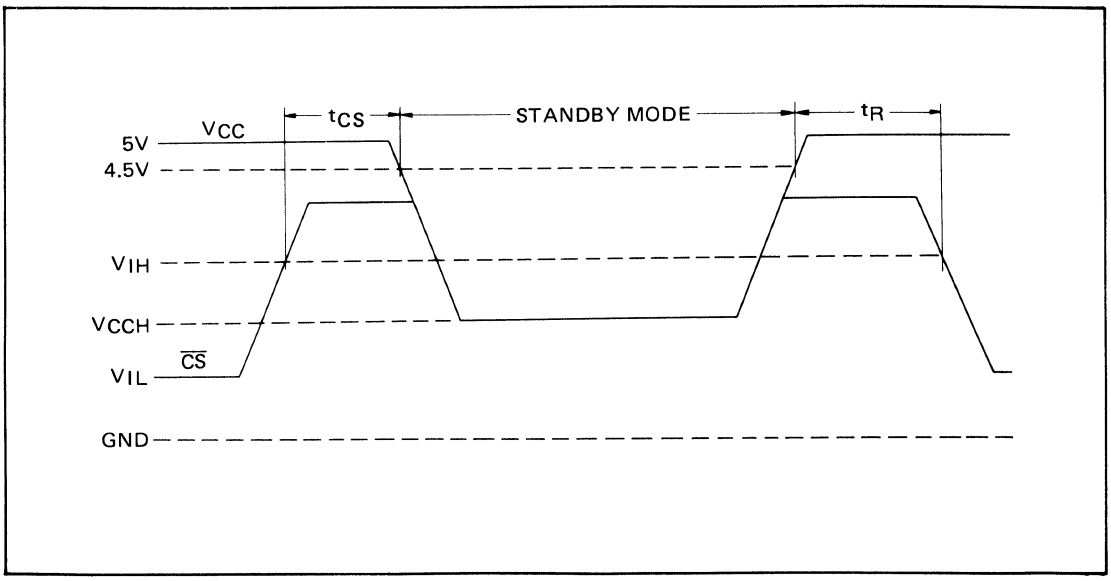
Notes: 1. Input Rise and Fall Time: 10 ns
2. Timing Measurement Reference Levels: 1.5V
3. Output Load: C_L = 50 pF
4. Input Pulse Levels: 0.8V to 2.4V

LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	V_{IN} = 0V or V_{CC}
Data Retention Current	I_{CCH}		0.1	20	μA	V_{CC} = 2V $\sqrt{\overline{CE}}$ = V_{CC} V_{IN} = 0V or V_{CC}
$\overline{CE}$ to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

LOW V_{CC} DATA RETENTION WAVEFORM



CAPACITANCE

($T_a = 25°C$, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			10	pF
Input Capacitance	C_{IN}			8	pF

Note: This parameter is periodically sampled and not 100% tested.

MSM5128RS

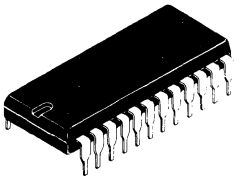
2048-WORD x 8-BIT C-MOS STATIC RAM (E3-S-013-32)

GENERAL DESCRIPTION

MSM5128RS is a 2048-word 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL coupling for inputs and outputs. And since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to employ. MSM5128RS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 50μA) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.
A byte system is adopted, and since there is pin compatibility with ultra-violet erasable type programmable ROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, $\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

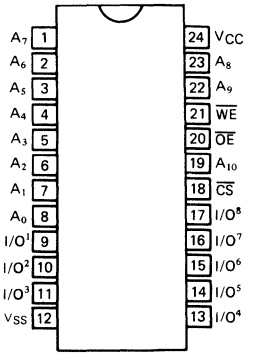
FEATURES

- Single 5V Supply
- Battery Back-up at 2V
- Operating temperature range Ta = −40°C to +85°C
- Low Power Dissipation
  - Standby; 1.0 μA MAX Ta = 25°C
    10 μA MAX Ta = 60°C
    50 μA MAX Ta = 85°C
  - Operation; 200 mW TYP
- High Speed (Equal Access and Cycle Time)
  MSM5128-12/15/20; 120 ns/150 ns/200 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with
  - 16K EPROM (MSM2716)
  - 16K NMOS SRAM (MSM2128)



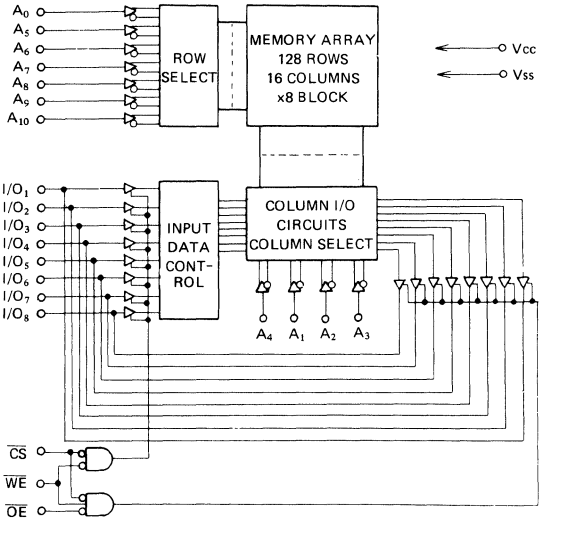
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{10}$: Address
$I/O^1 \sim I/O^8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS}: Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	−40 to 85	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Storage Supply Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

9

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = −40°C to +85°C)

Parameter	Symbol		MSM5128-12			MSM5128-15			MSM5128-20			Unit	Test Condition	
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
Input Leakage Current	I_{LI}		−1		1	−1		1	−1		1	μA	V_{IN} = 0 to V_{CC}	
Output Leakage Current	I_{LO}		−1		1	−1		1	−1		1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}	
Output Voltage	V_{OH}		2.4			2.4			2.4			V	I_{OH} = −1 mA	
	V_{OL}				0.4			0.4			0.4	V	I_{OL} = 4 mA (5128-12) I_{OL} = 2.1 mA (5128-15/20)	
Standby Supply Current	I_{CCS}	Ta 25°C		0.1	1.0		0.1	1.0		0.1	1.0	μA	$\overline{CS} \geq V_{CC}$ − 0.2V V_{IN} = 0 to V_{CC}	
		60°C			10			10			10			
		85°C			50			50			50			
	I_{CCS1}			0.3	1		0.3	1		0.3	1	mA	$\overline{CS}$ = V_{IH} t_{cyc} = Min. cycle	
Operating Supply Current	I_{CCA}			40	60		37	55		35	50	mA	Min. cycle	Ta = 0~85°C
				40	72		37	66		35	60	mA		Ta=−40~85°C

AC CHARACTERISTICS

Test Condition

Parameter	Conditions
Input Pulse Level	V_{IH}=2.2V, V_{IL}=0.8V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

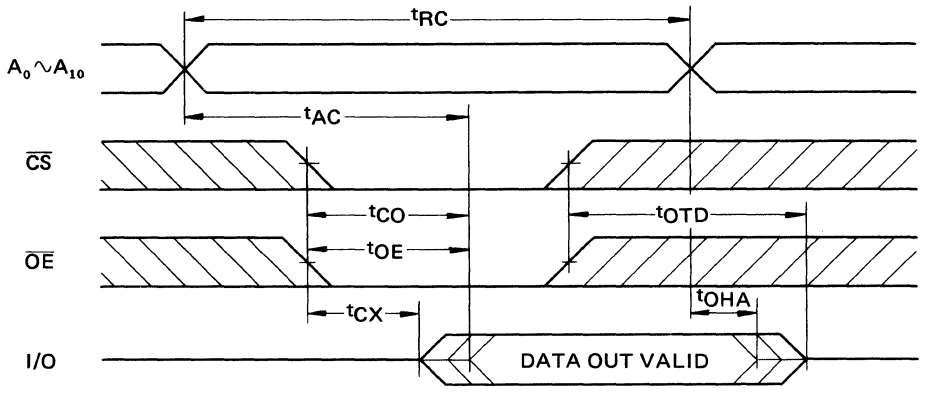
9

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = −40°C to +85°C)

Parameter	Symbol	MSM5128-12		MSM5128-15		MSM5128-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	120		150		200		ns
Address Access Time	t_{AC}		120		150		200	ns
Chip Select Access Time	t_{CO}		120		150		200	ns
Output Enable to Output Valid	t_{OE}		80		100		120	ns
Chip Selection to Output Active	t_{CX}	10		15		20		ns
Output Hold Time From Address Change	t_{OHA}	10		15		20		ns
Output 3-state from Deselection	t_{OTD}	0	50	0	50	0	60	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

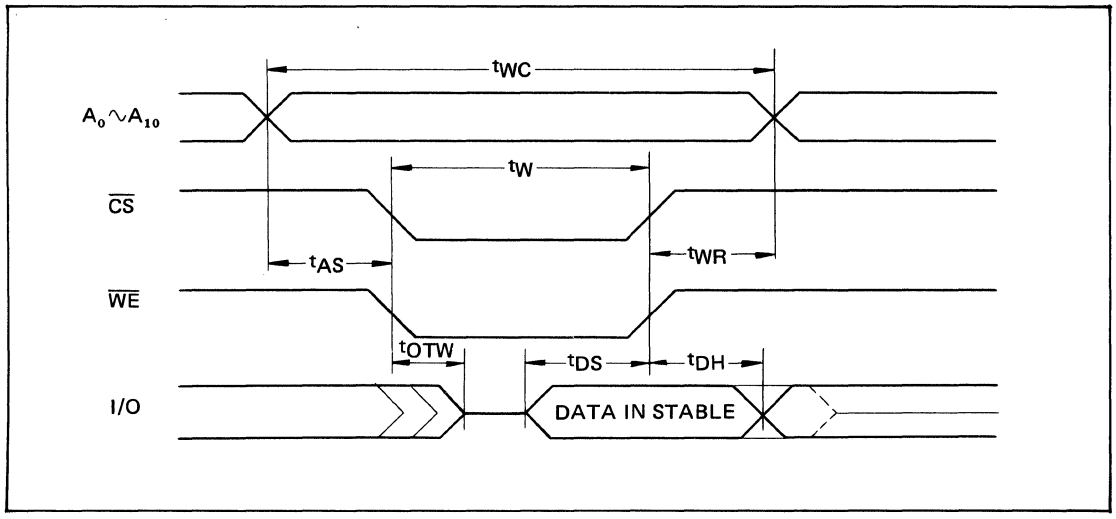
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = −40°C to +85°C)

Parameter	Symbol	MSM5128-12		MSM5128-15		MSM5128-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	120		150		200		ns
Address to Write Setup Time	t_{AS}	15		20		20		ns
Write Time	t_W	70		90		120		ns
Write Recovery Time	t_{WR}	15		20		20		ns
Data Setup Time	t_{DS}	50		60		80		ns
Data Hold from Write Time	t_{DH}	5		10		10		ns
Output 3-State from Write	t_{OTW}		50		50		60	ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

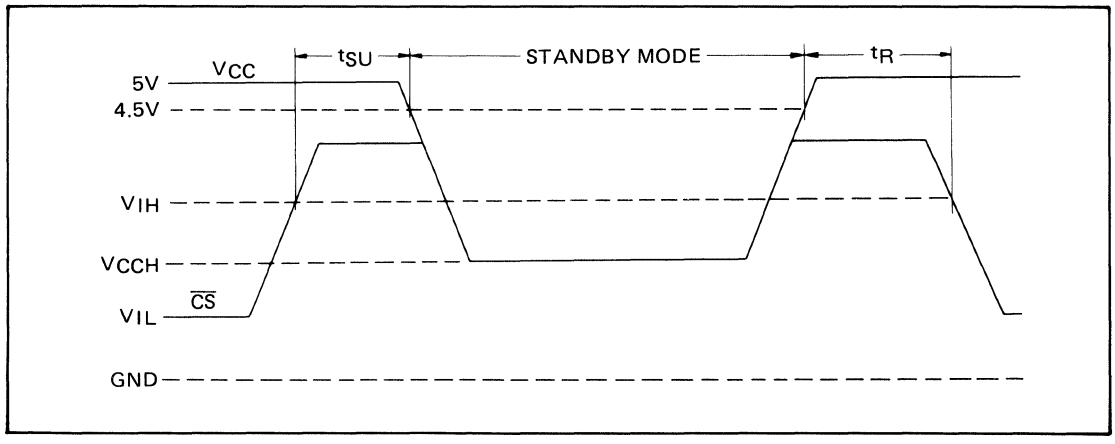
WRITE CYCLE



LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = −40°C to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	V_{IN} = 0V to V_{CC}, $\overline{CS}$ = V_{CC}
Data Retention Current	I_{CCH}		0.05	20	μA	V_{CC} = 2V $\overline{CS}$ = V_{CC} V_{IN} = 0V to V_{CC}
$\overline{CS}$ to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5128-20GSK

2048-WORD x 8-BIT C-MOS STATIC RAM (E3-S-013-32)

GENERAL DESCRIPTION

MSM5128GS is a 2048-word 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL coupling for inputs and outputs. And since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to employ. MSM5128GS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 50μA) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

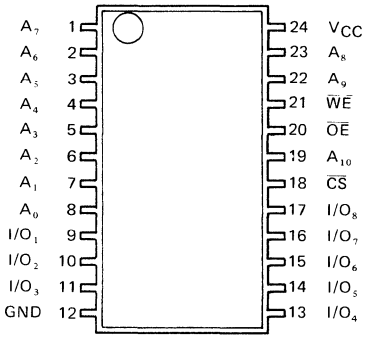
A byte system is adopted, and since there is pin compatibility with ultra-violet erasable type programmable ROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, $\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- Battery Back-up at 2V
- Operating temperature range Ta = −40°C to +85°C
- Low Power Dissipation
  - Standby; 1.0 μA MAX Ta = 25°C
    10 μA MAX Ta = 60°C
    50 μA MAX Ta = 85°C
  - Operation; 200 mW TYP
- High Speed (Equal Access and Cycle Time)
  MSM5128-20; 200 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 24 Pin Flat PKG

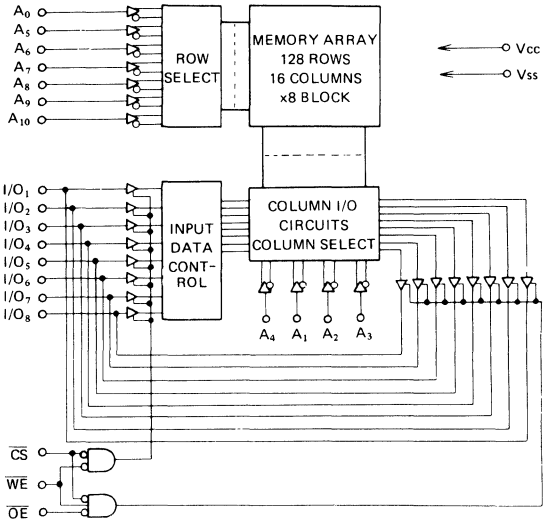
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{10}$: Address
$I/O^1 \sim I/O^8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS}: Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	−40 to 85	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Storage Supply Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

9

DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = -40°C to +85°C)

Parameter	Symbol		MSM5128-20 Min.	Typ.	Max.	Unit	Test Condition	
Input Leakage Current	I_{LI}		-1		1	μA	V_{IN} = 0 to V_{CC}	
Output Leakage Current	I_{LO}		-1		1	μA	CS = V_{IH} or OE = V_{IH} $V_{I/O}$ = 0 to V_{CC}	
Output Voltage	V_{OH}		2.4			V	I_{OH} = -1 mA	
	V_{OL}				0.4	V	I_{OL} = 4 mA (5128-12) I_{OL} = 2.1 mA (5128-15/20)	
Standby Supply Current	I_{CCS}	Ta 25°C		0.1	1.0	μA	CS ≧ V_{CC} - 0.2V V_{IN} = 0 to V_{CC}	
		60°C			10			
		85°C			50			
	I_{CCS1}			0.3	1	mA	CS = V_{IH} t_{cyc} = Min. cycle	
Operating Supply Current	I_{CCA}			35	50	mA	Min. cycle	Ta = 0 ~ 85°C
				35	60	mA		Ta = -40 ~ 85°C

AC CHARACTERISTICS

Test Condition

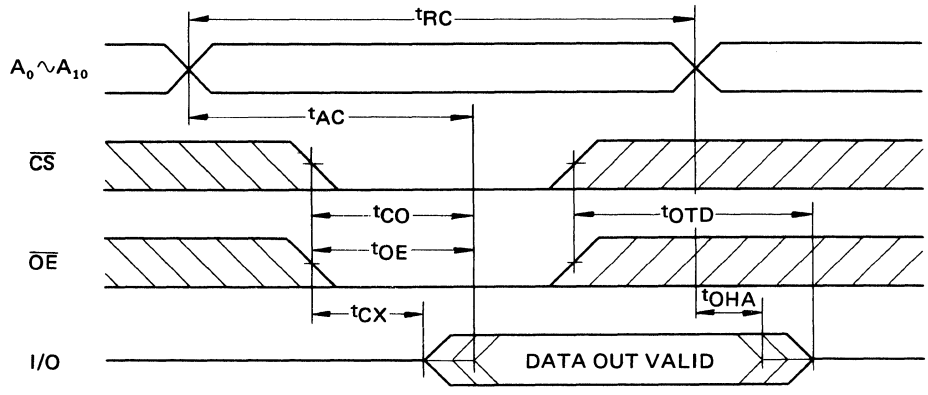
Parameter	Conditions
Input Pulse Level	V_{IH}=2.2V, V_{IL}=0.8V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = -40°C to +85°C)

Parameter	Symbol	MSM5128-20 Min.	Max.	Unit
Read Cycle Time	t_{RC}	200		ns
Address Access Time	t_{AC}		200	ns
Chip Select Access Time	t_{CO}		200	ns
Output Enable to Output Valid	t_{OE}		120	ns
Chip Selection to Output Active	t_{CX}	20		ns
Output Hold Time from Address Change	t_{OHA}	20		ns
Output 3-state from Deselection	t_{OTD}	0	60	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

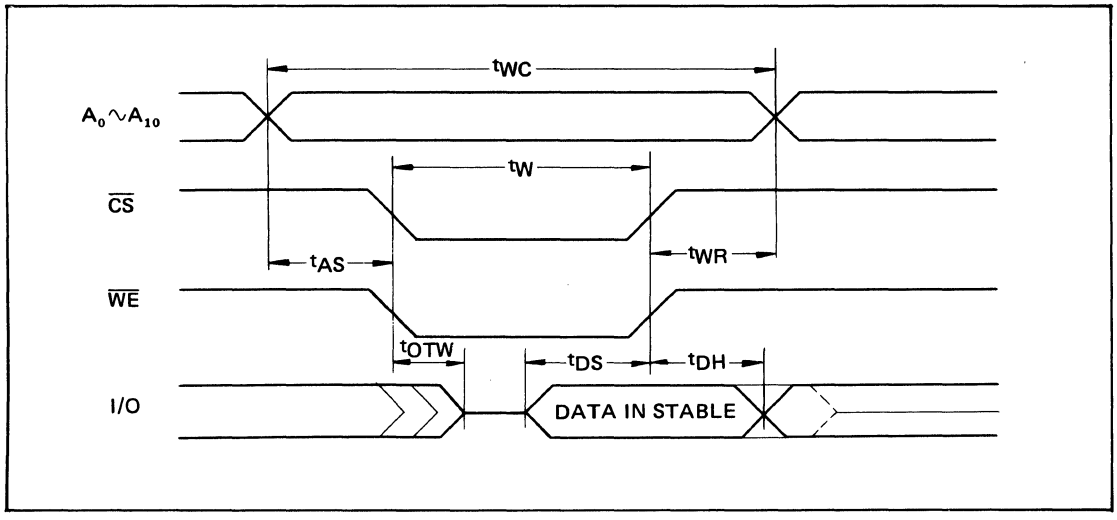
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = −40°C to +85°C)

Parameter	Symbol	MSM5128-20		Unit
		Min.	Max.	
Write Cycle Time	t_{WC}	200		ns
Address to Write Setup Time	t_{AS}	20		ns
Write Time	t_W	120		ns
Write Recovery Time	t_{WR}	20		ns
Data Setup Time	t_{DS}	80		ns
Data Hold from Write Time	t_{DH}	10		ns
Output 3-State from Write	t_{OTW}		60	ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

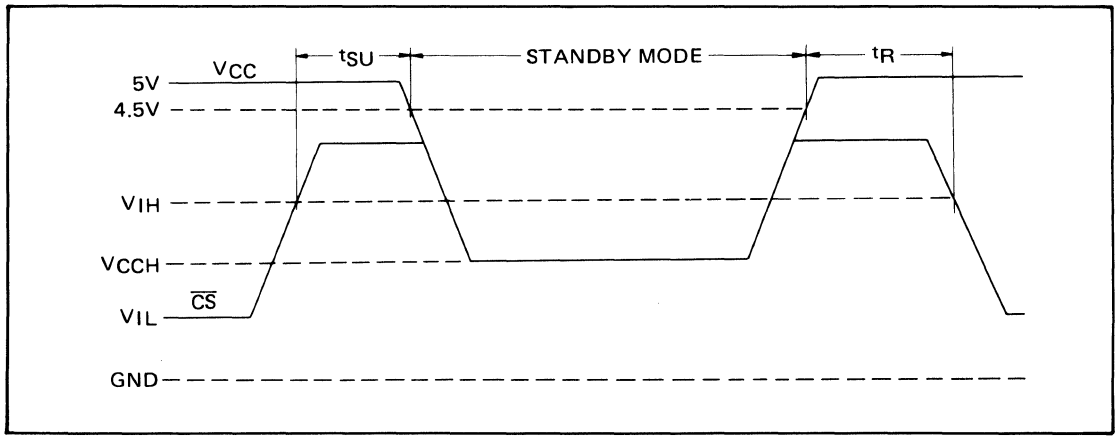
WRITE CYCLE



LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = −40°C to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	V_{IN} = 0V to V_{CC}, $\overline{CS}$ = V_{CC}
Data Retention Current	I_{CCH}		0.05	20	μA	V_{CC} = 2V $\overline{CS}$ = V_{CC} V_{IN} = 0V to V_{CC}
$\overline{CS}$ to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	



9

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

MSM5126RS

2048-WORD x 8-BIT C-MOS STATIC RAM (E3-S-014-32)

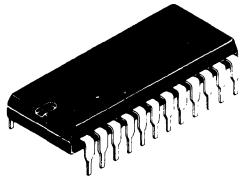
GENERAL DESCRIPTION

MSM5126RS is a 2048-word 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL coupling for inputs and outputs. And since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to employ. MSM5126RS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 30μA) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

A byte system is adopted, and since there is pin compatibility with ultra-violet erasable type programmable ROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, $\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

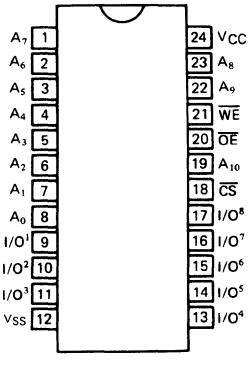
FEATURES

- Single 5V Supply
- Battery Back-up at 2V
- Operating temperature range Ta = −30°C to +85°C
- Low Power Dissipation
  - Standby; 1.0 μA MAX T_a = 25°C
    5.0 μA MAX T_a = 60°C
    30 μA MAX T_a = 85°C
  - Operation; 200 mW TYP
- High Speed (Equal Access and Cycle Time)
  MSM5126-20/25; 200 ns/250 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with
  - 16K EPROM (MSM2716)
  - 16K NMOS SRAM (MSM2128)



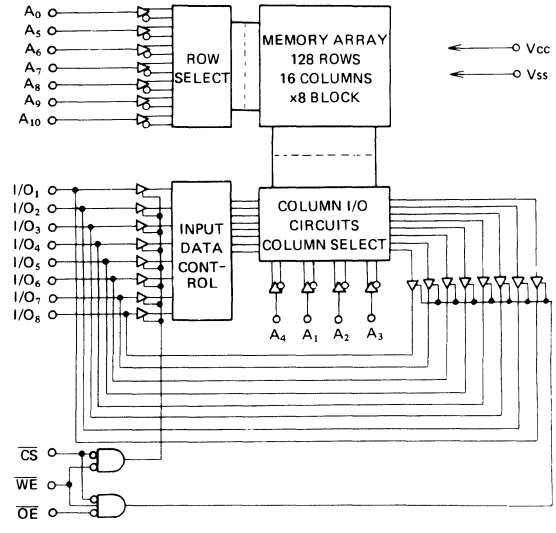
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{10}$: Address
$I/O^1 \sim I/O^8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS}: Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



9

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	−30 to 85	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Storage Supply Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

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DC CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = −30°C to +85°C)

Parameter	Symbol	Test Condition		MSM5126-20/25 Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}		−1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}		−5		5	μA
Output Voltage	V_{OH}	I_{OH} = −1 mA		2.4			V
	V_{OL}	I_{OL} = 2.0 mA				0.4	V
Standby Supply Current	I_{CCS}	$\overline{CS}$ = V_{CC} − 0.5V V_{CC} = 2V ~ 5.5V	Ta = 25°C		0.05	1.0	μA
			Ta = 60°C			5.0	
			Ta = 85°C			30	
	I_{CCS_1}	$\overline{CS}$ = V_{IH} t_{CYC} = Min. cycle			1	3	mA
Operating Supply Current	I_{CCA}	$\overline{CS}$ = 0V, V_{IN} = V_{IH}/V_{IL} I_{OUT} = 0 mA			40	70	mA
		$\overline{CS}$ = 0V, V_{IN} = V_{CC}/GND, I_{OUT} = 0 mA			30	55	mA

AC CHARACTERISTICS

Test Condition

Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	2.2V 0.8V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = −30°C to +85°C)

Parameter	Symbol	MSM5126-20 Min.	MSM5126-20 Max.	MSM5126-25 Min.	MSM5126-25 Max.	Unit
Read Cycle Time	t_{RC}	200		250		ns
Address Access Time	t_{AC}		200		250	ns
Chip Select Access Time	t_{CO}		200		250	ns
Output Enable to Output Valid	t_{OE}		100		100	ns
Chip Selection to Output Active	t_{CX}	10		10		ns
Output Hold Time From Address Change	t_{OHA}	10		10		ns
Output 3-state from Deselection	t_{OTD}	0	80	0	80	ns

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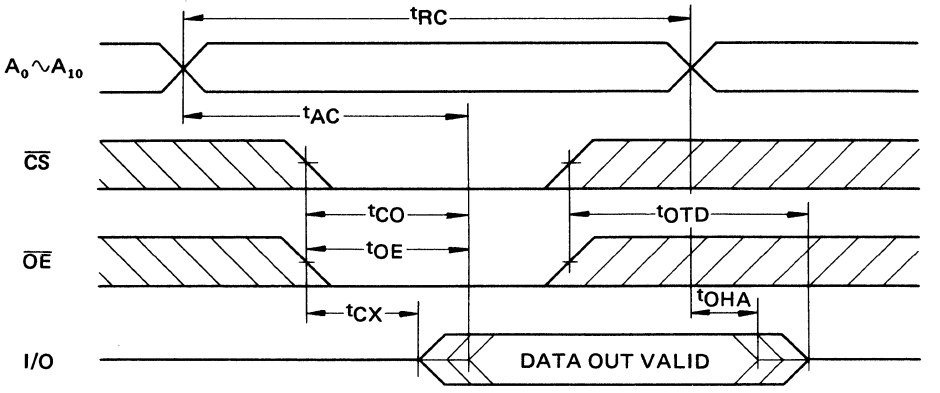
READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CS}$ or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

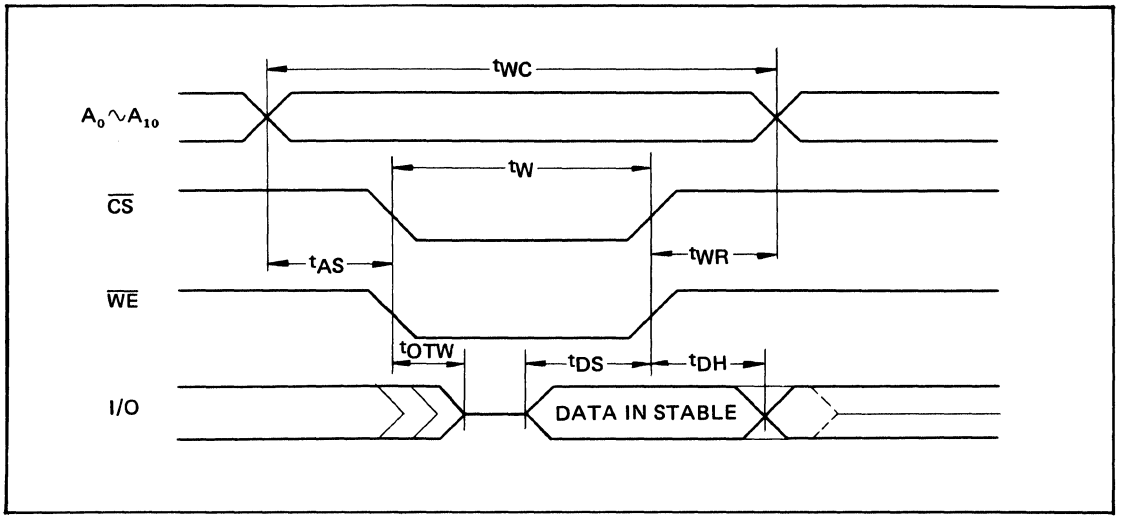
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = −30°C to +85°C)

Parameter	Symbol	MSM5126-20		MSM5126-25		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	200		250		ns
Address to Write Setup Time	t_{AS}	0		0		ns
Write Time	t_W	160		200		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	80		120		ns
Data Hold from Write Time	t_{DH}	0		0		ns
Output 3-State from Write	t_{OTW}		80		80	ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

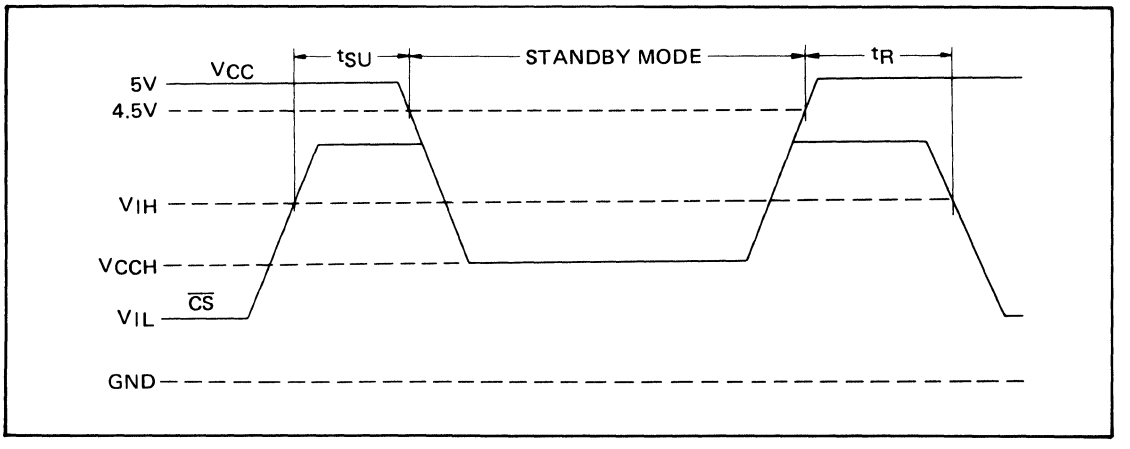
WRITE CYCLE



LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = −30°C to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	V_{IN} = 0V to V_{CC}
Data Retention Current	I_{CCH}		0.05	30	μA	V_{CC} = 2V ~ 5.5V $V_{\overline{CS}} = V_{CC} - 0.5V$
$\overline{CS}$ to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	



CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$		5	10	pF
Input Capacitance	C_{IN}		5	10	pF

Note: This parameter is periodically sampled and not 100% tested.

MSM5127RS

2,048-WORD x 8-BIT CMOS STATIC RAM (E3-S-015-32)

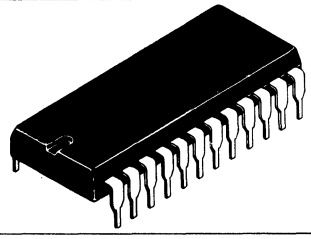
GENERAL DESCRIPTION

MSM5127RS is a 2048-word 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL coupling for inputs and outputs. And since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to employ. MSM5127RS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 50μA) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

A byte system is adopted, and since there is pin compatibility with ultra-violet erasable type programmable ROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, two CE signals enable simple memory expansion and easily battery back-up capability etc.

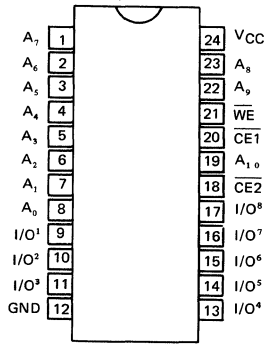
FEATURES

- Single 5V supply
- Battery back-up at 2V
- Low power dissipation
  - Standby; 1.0 μA MAX Ta = 25°C
    10 μA MAX Ta = 60°C
    50 μA MAX Ta = 85°C
  - Operation; 200 mW TYP
- High Speed (Equal access and cycle time)
  MSM5127-15/20: 150 ns/200 ns MAX
- Direct TTL compatible (Input and Output)
- 3-State output
- Pin compatible with
  16 K EPROM (MSM2716)
  16 K NMOS SRAM (MSM2128)



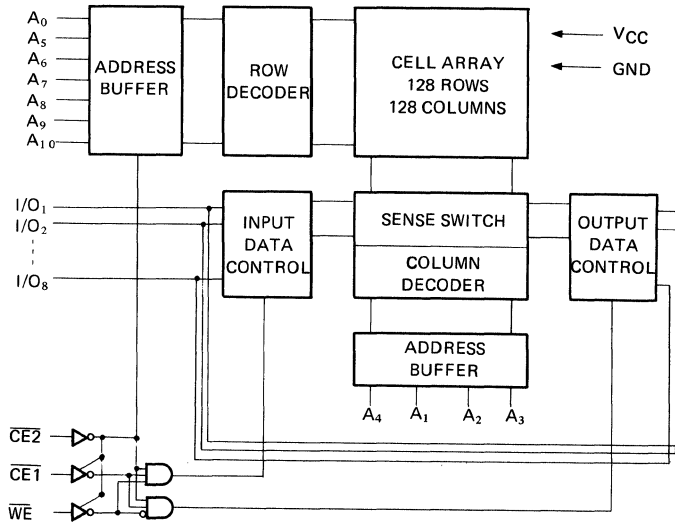
PIN CONFIGURATION

(Top View)



Pin Names	Function
A_0~A_{10}	Address
I/O^1~I/O^8	Data Input/Output
$\overline{CE1}$, $\overline{CE2}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

Mode	$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	I/O Operation
Standby	X	H	X	High Z
Read	H	L	X	High Z
	L	L	H	D_{OUT}
Wire	L	L	L	D_{IN}

X: H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 ~ 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 ~ V_{CC} + 0.3	V	
Operating Temperature	T_a	−40 ~ 85	°C	
Storage Temperature	T_{stg}	−55 ~ 150	°C	
Power Dissipation	P_d	1.0	W	

RECOMMENDED OPERTING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ±10%
	GND		0		V	
Data Storage Supply Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC}+0.3	V	5V ±10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

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DC CHARACTERISTICS

(V_{CC} = 5V ± 10% Ta = –40 ~ 85°C

Parameter	Symbol		MSM5127-15			MSM5127-20			Unit	Test Condition	
			Min.	Typ.	Max.	Min.	Typ.	Max.			
Input Leakage Current	I_{LI}		–1		1	–1		1	μA	V_{IN} = 0 to V_{CC}	
Output Leakage Current	I_{LO}		–1		1	–1		1	μA	$\overline{CE2}$ = V_{IH} or $\overline{CE1}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}	
Output Voltage	V_{OH}		2.4			2.4			V	I_{OH} = –1 mA	
	V_{OL}				0.4			0.4	V	I_{OL} = 2.1 mA	
Standby Supply Current	I_{CCS}	Ta 25°C		0.1	1.0		0.1	1.0	μA	$\overline{CE2} \geqq V_{CC}$ – 0.2V V_{IN} = 0 to V_{CC}	
		60°C			10			10			
		85°C			50			50			
	I_{CCS1}			0.3	1		0.3	1	mA	$\overline{CE2}$ = V_{IH} t_{cyc} = min cycle	
Operating Supply Current	I_{CCA}			37	55		35	50	mA	Min. cycle	Ta = 0 ~ 85°C
				37	66		35	60	mA		Ta = –40 ~ 85°C

AC CHARACTERISTICS

TEST CONDITION

Parameter	Conditions
Input Pulse Level	V_{IH} = 2.2V, V_{IL} = 0.8V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V±10%, Ta = –40~85°C)

Parameter	Symbol	MSM5127-15		MSM5127-20		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	150		200		ns
Address Access Time	t_{AC}		150		200	ns
$\overline{CE2}$ Access Time	t_{CO2}		150		200	ns
$\overline{CE1}$ Access Time	t_{CO1}		100		120	ns
Chip Selection to Output Active	t_{CX}	15		20		ns
Output Hold Time From Address Change	t_{OHA}	15		20		ns
Output 3-state from Deselection	t_{OTD}	0	50	0	60	ns

NOTES: 1. A read occurs during the overlap of a low $\overline{CE2}$, a low $\overline{CE1}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CE1}$ or $\overline{CE2}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CE1}$ or $\overline{CE2}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

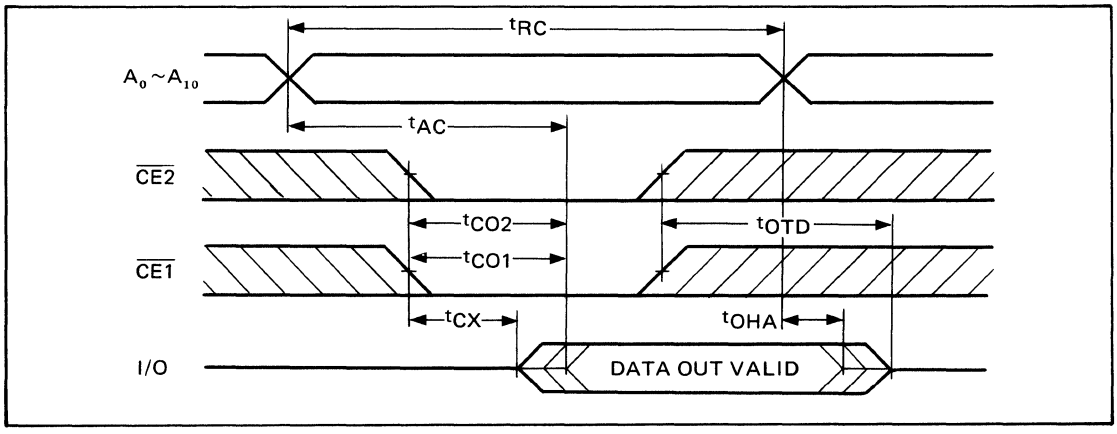
WRITE CYCLE

(V_{CC} = 5V±10%, Ta = −40~85°C)

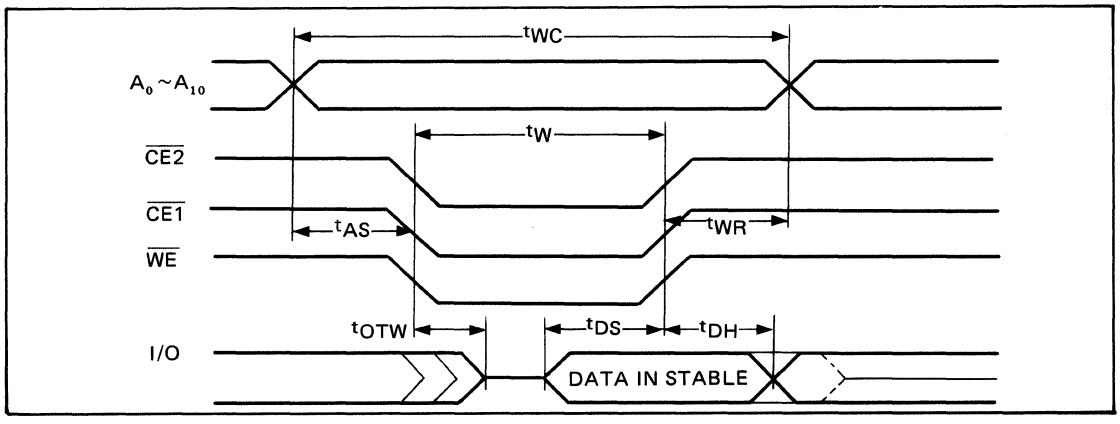
Parameter	Symbol	MSM5127-15		MSM5127-20		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	150		200		ns
Address to Write Setup Time	t_{AS}	20		20		ns
Write Time	t_W	90		120		ns
Write Recovery Time	t_{WR}	20		20		ns
Data Setup Time	t_{DS}	60		80		ns
Data Hold from Write Time	t_{DH}	10		10		ns
Output 3-State from Write	t_{OTW}		50		60	ns

NOTES: 1. A Write Cycle occurs during the overlap of a low $\overline{CE1}$, a low $\overline{CE2}$ and a low $\overline{WE}$.
2. t_{AS} is specified from $\overline{CE1}$ or $\overline{CE2}$ or $\overline{WE}$, whichever occurs last.
3. t_W is an overlap time of a low $\overline{CE1}$, a low $\overline{CE2}$ and a low $\overline{WE}$.
4. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CE1}$ or $\overline{CE2}$ or $\overline{WE}$, whichever occurs first.
5. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
6. When I/O pins are Data output mode, don't force inverse signal to those pins.

READ CYCLE



WRITE CYCLE



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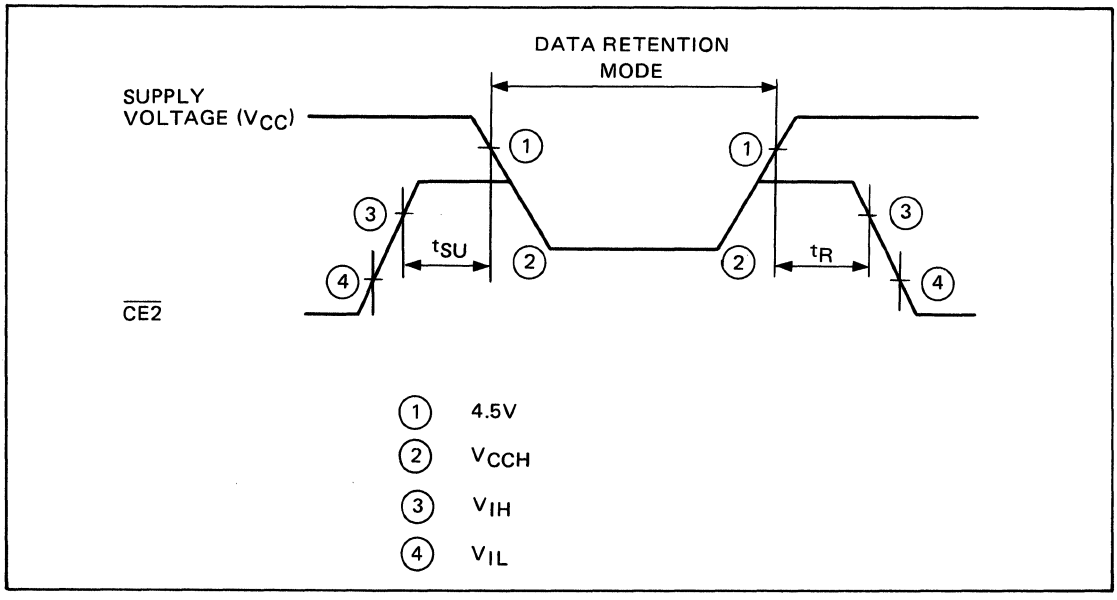
LOW V_{CC} DATA RETENTION CHARACTERISTICS

(Ta = –40 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	$\overline{V_{IN}}$ = 0V to V_{CC} $\overline{CE2}$ = Vcc
Data Retention Current	I_{CCH}		0.05	20	μA	Vcc = 2V, $\overline{CE2}$ = Vcc V_{IN} = 0V to Vcc
$\overline{CE}$ to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

LOW V_{CC} DATA RETENSION WAVEFORM



9

CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM5129RS

2,048-WORD x 8-BIT CMOS STATIC RAM (E3-S-016-32)

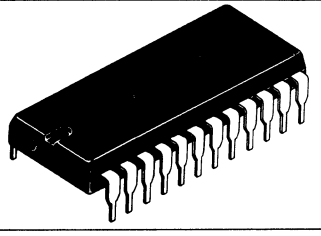
GENERAL DESCRIPTION

MSM5129RS is a 2048-word 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL coupling for inputs and outputs. And since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to employ. MSM5129RS is also a CMOS silicon gate device which requires very little power during standby (maximum standby current of 50μA) when there is no chip selection. Stored data is retained if the power voltage drops to 2V, thereby enabling battery back-up.

A byte system is adopted, and since there is pin compatibility with ultra-violet erasable type programmable ROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, two CE signals enable simple memory expansion and easily battery back-up capability etc.

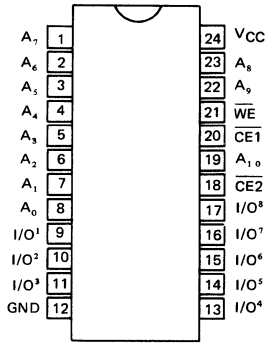
FEATURES

- Single 5V supply
- Battery back-up at 2V
- Low power dissipation
  - Standby; 1.0 μA MAX Ta = 25°C
    10 μA MAX Ta = 60°C
    50 μA MAX Ta = 85°C
  - Operation: 200 mW TYP
- High Speed (Equal access and cycle time)
  MSM5129-15/20: 150 ns/200 ns MAX
- Direct TTL compatible (Input and Output)
- 3-State output
- Pin compatible with
  16 K EPROM (MSM2716)
  16 K NMOS SRAM (MSM2128)



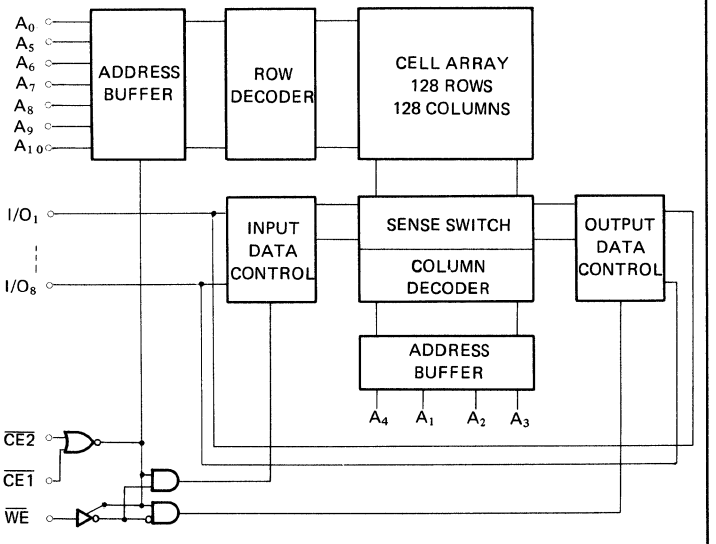
PIN CONFIGURATION

(Top View)



Pin Names	Function
$A_0 \sim A_{10}$	Address
$I/O^1 \sim I/O^8$	Data Input/Output
$\overline{CE1}$, $\overline{CE2}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	

FUNCTIONAL BLOCK DIAGRAM



9

TRUTH TABLE

Mode	$\overline{CE1}$	$\overline{CE2}$	$\overline{WE}$	I/O Operation
STANDBY	H	X	X	High Z
	L	H	X	
READ	L	L	H	D_{OUT}
WRITE	L	L	L	D_{IN}

X: H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Note
Supply Voltage	V_{CC}	−0.3 ~ 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 ~ V_{CC} + 0.3	V	
Operating Temperature	T_a	−40 ~ 85	°C	
Storage Temperature	T_{stg}	−55 ~ 150	°C	
Power Dissipation	P_d	1.0	W	

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ±10%
	GND		0		V	
Data Storage Supply Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC}+0.3	V	5V ±10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

9

DC CHARACTERISTICS

(V_{CC} = 5V ± 100% Ta = –40 ~ 85°C)

Parameter	Symbol	MSM5129-15			MSM5129-20			Unit	Test Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	–1		1	–1		1	μA	V_{IN}=0 to V_{CC}
Output Leakage Current	I_{LO}	–1		1	–1		1	μA	$\overline{CE2}$ =V_{IH} or $\overline{CE1}$=V_{IH} $V_{I/O}$=0 to V_{CC}
Output Voltage	V_{OH}	2.4			2.4			V	I_{OH}=–1 mA
	V_{OL}			0.4			0.4	V	I_{OL}=2.1 mA
Standby Supply Current	I_{CCS} Ta 25°C		0.1	1.0		0.1	1.0	μA	$\overline{CE2} \geqq$ Vcc–0.2V $\overline{CE1} \geqq$ Vcc–0.2V or $\leqq$0.2V V_{IN}=0 to Vcc
	I_{CCS} 60°C			10			10	μA	$\overline{CE1} \geqq$ Vcc–0.2V $\overline{CE2} \geqq$ Vcc–0.2V or $\leqq$0.2V V_{IN}=0 to Vcc
	I_{CCS} 85°C			50			50	μA	
	I_{CCS1}		0.6	2		0.6	2	mA	$\overline{CE}$= V_{IH} t_{cyc}=min cycle
Operating Supply Current	I_{CCA}		37	55		35	50	mA	Min. cycle Ta=0~85°C
			37	66		35	60	mA	Min. cycle Ta=–40~85°C

AC CHARACTERISTICS

TEST CONDITION

Parameter	Conditions
Input Pulse Level	V_{IH} = 2.2V, V_{IL} = 0.8V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V±10%, Ta = –40~85°C)

Parameter	Symbol	MSM5129-15		MSM5129-20		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	150		200		ns
Address Access Time	t_{AC}		150		200	ns
$\overline{CE1}$ Access Time	t_{CO1}		150		200	ns
$\overline{CE2}$ Access Time	t_{CO2}		150		200	ns
Chip Selection to Output Active	t_{CX}	15		20		ns
Output Hold Time from Address Change	t_{OHA}	15		20		ns
Output 3-state from Deselection	t_{OTD}	0	50	0	60	ns

NOTES: 1. A read occurs during the overlap of a low $\overline{CE2}$, a low $\overline{CE1}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CE1}$ or $\overline{CE2}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CE1}$ or $\overline{CE2}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

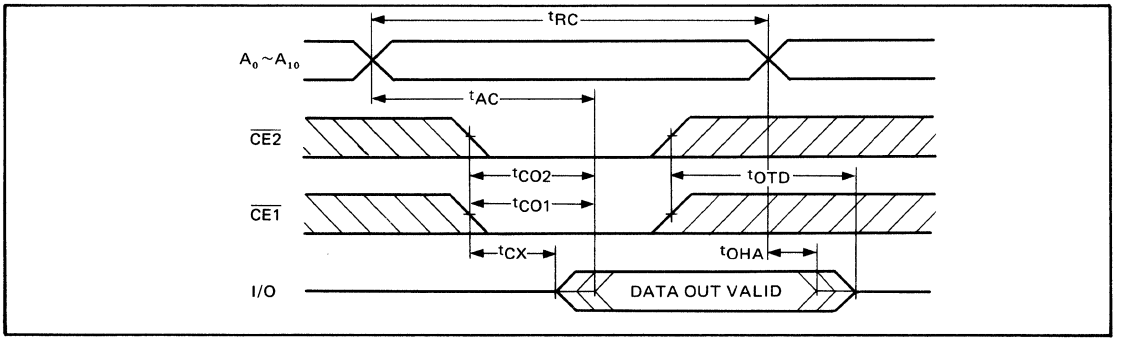
WRITE CYCLE

(V_{CC} = 5V±10%, Ta = –40~85°C)

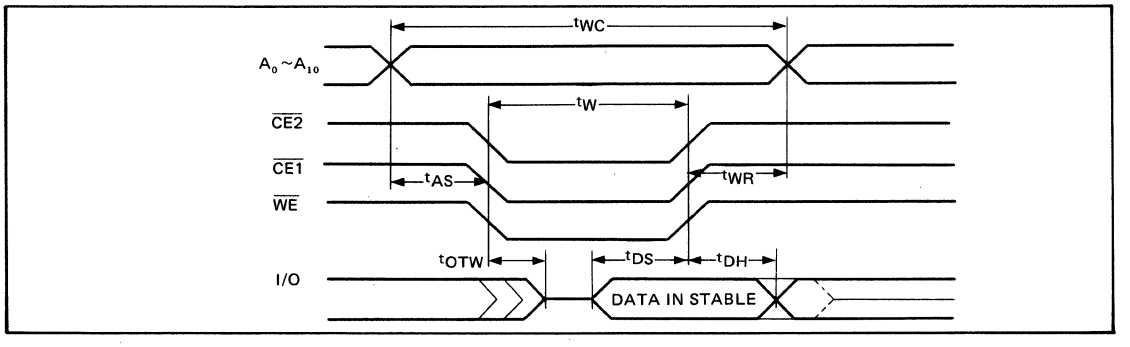
Parameter	Symbol	MSM5129-15		MSM5129-20		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	150		200		ns
Address to Write Setup Time	t_{AS}	20		20		ns
Write Time	t_{W}	90		120		ns
Write Recovery Time	t_{WR}	20		20		ns
Data Setup Time	t_{DS}	60		80		ns
Data Hold from Write Time	t_{DH}	10		10		ns
Output 3-State from Write	t_{OTW}		50		60	ns

NOTES: 1. A Write Cycle occurs during the overlap of a low $\overline{CE1}$, a low $\overline{CE2}$ and a low $\overline{WE}$.
2. t_{AS} is specified from $\overline{CE1}$ or $\overline{CE2}$ or $\overline{WE}$, whichever occurs last.
3. t_{W} is an overlap time of a low $\overline{CE1}$, a low $\overline{CE2}$ and a low $\overline{WE}$.
4. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CE1}$ or $\overline{CE2}$ or $\overline{WE}$, whichever occurs first.
5. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
6. When I/O pins are Data output mode, don't force inverse signal to those pins.

READ CYCLE



WRITE CYCLE

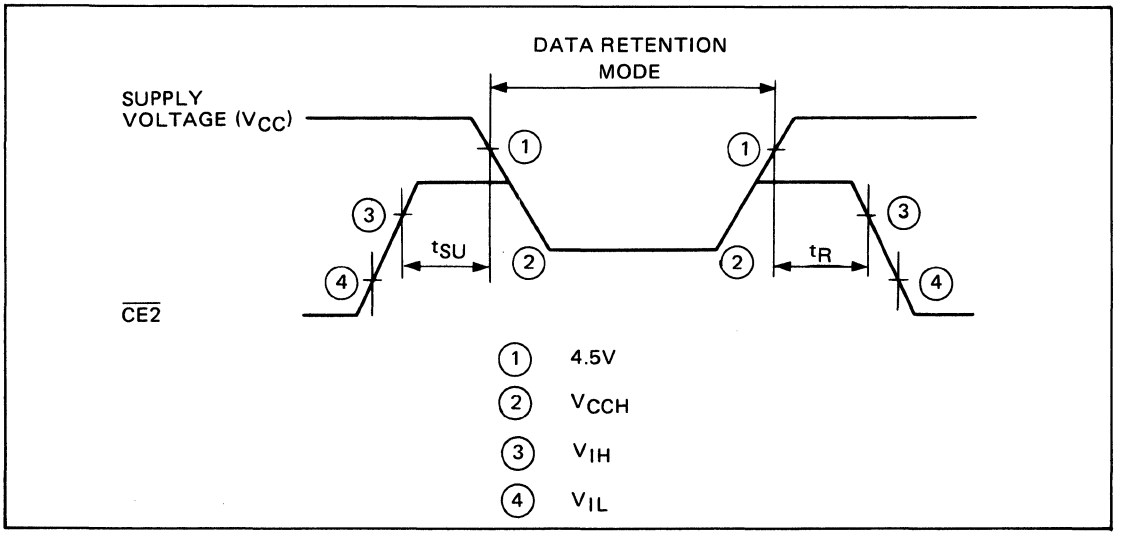


LOW V_{CC} DATA RETENTION CHARACTERISTICS

(Ta = –40 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	$\overline{CE2}$ = Vcc $\overline{CE1}$ = 0 or Vcc V_{IN} = 0 to Vcc
						$\overline{CE1}$ = Vcc $\overline{CE2}$ = 0 or Vcc V_{IN} = 0 to Vcc
Data Retention Current	I_{CCH}		0.05	20	μA	Vcc = 2V, $\overline{CE2}$ = Vcc $\overline{CE1}$ = 0 or Vcc V_{IN} = 0 to Vcc
						Vcc = 2V, $\overline{CE1}$ = Vcc $\overline{CE2}$ = 0 or Vcc V_{IN} = 0 to Vcc
$\overline{CE}$ to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

LOW V_{CC} DATA RETENSION WAVEFORM



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

9

Preliminary

MSM5165RS

8,192-WORD x 8-BIT CMOS STATIC RAM (E3-S-017-32)

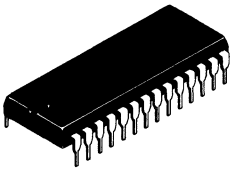
GENERAL DESCRIPTION

MSM5165 is a 8192 word 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL coupling for inputs and outputs. And since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to employ. MSM5165 is also a CMOS silicon gate device which requires very low power during standby (standby current of 1mA) when there is no chip selection.

A byte system is adopted, and since there is pin compatibility with ultra-violet erasable type programmable ROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, $\overline{CE}_1$ CE_2 and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

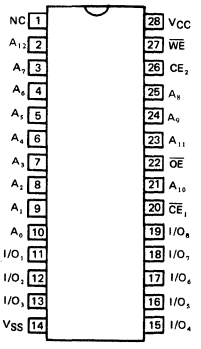
FEATURES

- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  - Standby; 5.5 mW MAX
  - Operation; 495 mW MAX
- High Speed (Equal Access and Cycle Time)
  - 100 – 150 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with
  - 64K EPROM (MSM2764)
  - 64K NMOS SRAM (MSM2188)
- 28-pin DIP PKG



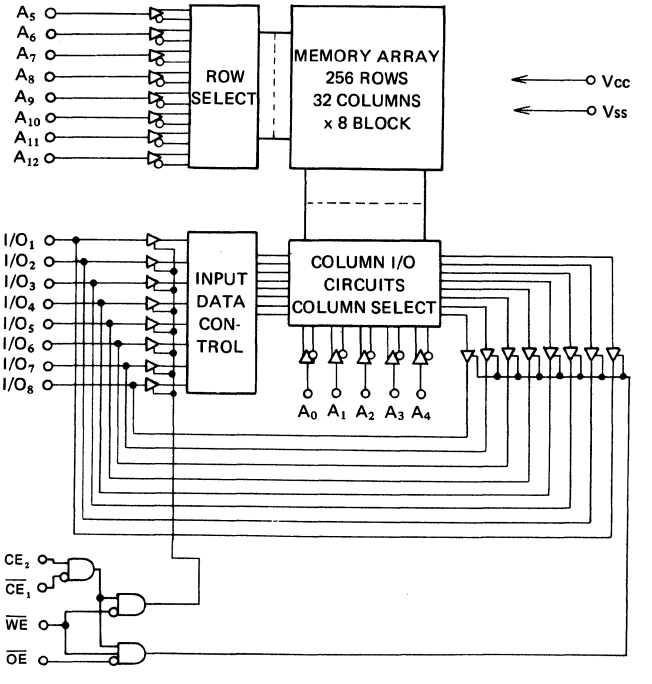
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{12}$	: Address
$I/O_1 \sim I/O_8$	: Data Input/Output
$\overline{CE}_1$, CE_2	: Chip Select
$\overline{WE}$	: Write Enable
$\overline{OE}$	: Output Enable
V_{CC}, V_{SS}	: Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



9

TRUTH TABLE

Mode	$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	X	High Z
	X	L	X	X	
Read	L	H	H	H	High Z
	L	H	H	L	D_{OUT}
Wreite	L	H	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Storage Supply Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.5	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

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DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM5165			Unit	Test Condition	
		Min.	Typ.	Max.			
Input Leakage Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}	
Output Leakage Current	I_{LO}	−1		1	μA	$\overline{CE}_1$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}	
Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA	
	V_{OL}			0.4	V	I_{OL} = 2.1 mA	
Standby Supply Current	I_{CCS}			1	mA	$\overline{CE}_1 \geqq V_{CC} - 0.2V$, $CE_2 \geqq V_{CC} - 0.2V$ or $CE_2 \leqq 0.2V$ V_{IN} = 0 to V_{CC}	
						$CE_2 \leqq 0.2V$ V_{IN} = 0 to V_{CC}	
	I_{CCS1}			3	mA	$\overline{CE}_1$ = V_{IH}, CE_2 = V_{IL} t_{cyc} = Min. cycle	
Operating Supply Current	I_{CCA}			90	mA mA	Min. cycle	T_a = 0 ~ 70°C

AC CHARACTERISTICS

Test Condition

Parameter	Conditions
Input Pulse Level	V_{IH}=2.2V, V_{IL}=0.8V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

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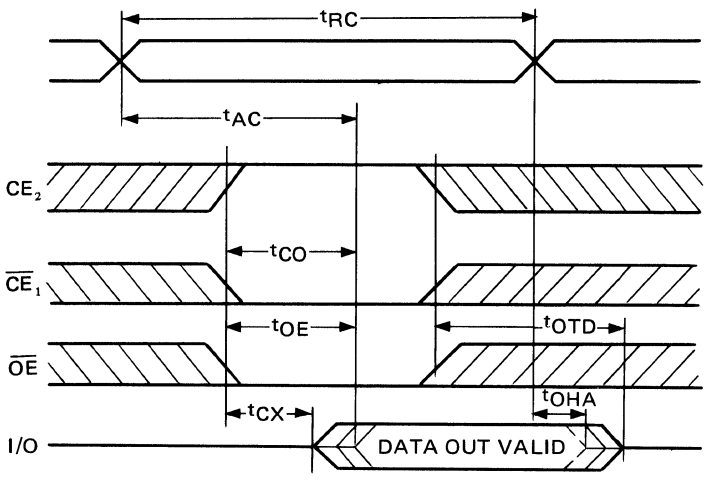
READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM5165-10		MSM5165-12		MSM5165-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AC}		100		120		150	ns
Chip Enable Access Time	t_{CO}		100		120		150	ns
Output Enable to Output Valid	t_{OE}		60		80		100	ns
Chip Selection to Output Active	t_{CX}	10		10		15		ns
Output Hold Time From Address Change	t_{OHA}	10		10		15		ns
Output 3-state from Deselection	t_{OTD}	0	40	0	50	0	50	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CE_1}$, a high CE_2, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CE_1}$, CE_2 or $\overline{OE}$, whichever occurs last.
3. t_{OTD} is specified from $\overline{CE_1}$, CE_2 or $\overline{OE}$, whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

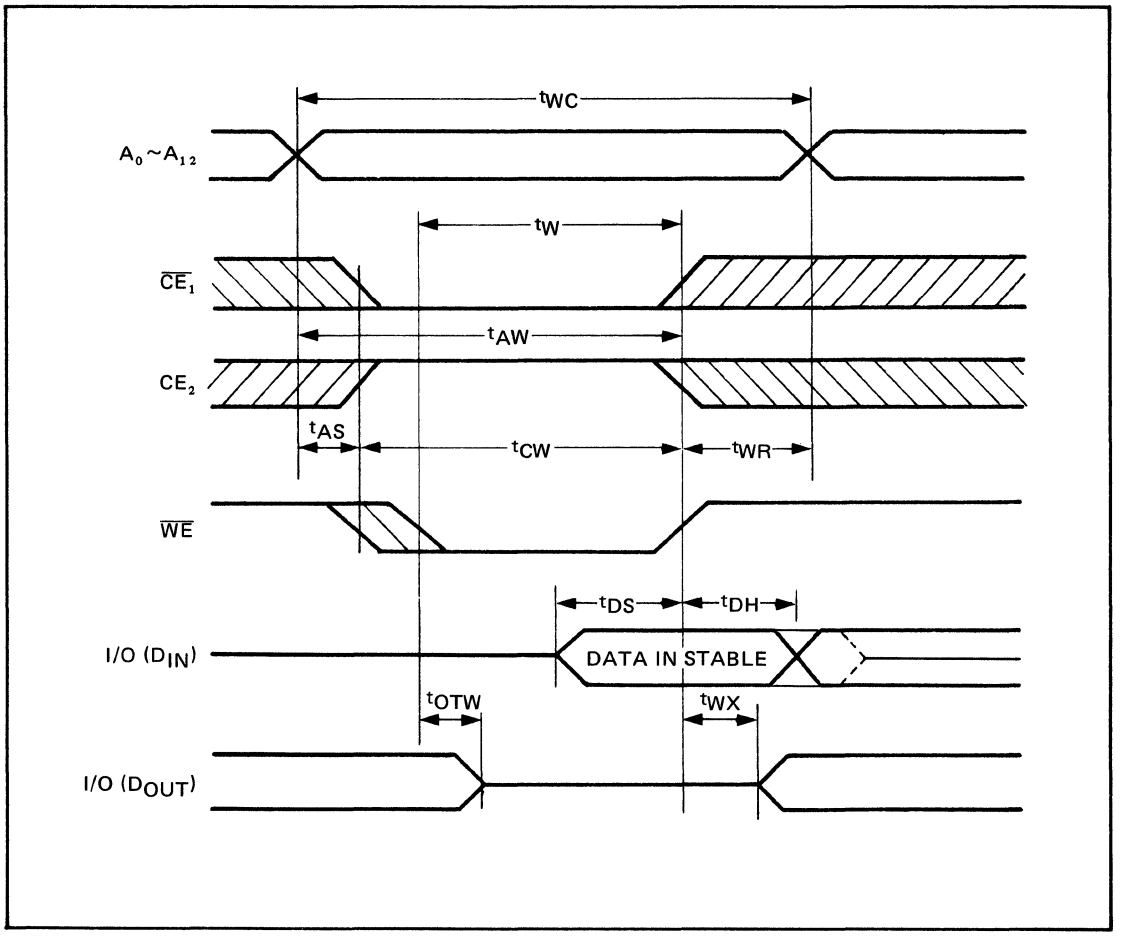
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM5165-10		MSM5165-12		MSM5165-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	100		120		150		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	60		70		90		ns
Write Recovery Time	t_{WR}	15		15		20		ns
Data Setup Time	t_{DS}	40		50		60		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	40	0	50	0	50	ns
Chip Selection to End of Write	t_{CW}	80		90		110		ns
Address Valid to End of Write	t_{AW}	80		90		110		ns
Output Active from End of Write	t_{WX}	5		5		10		ns

Note: 1. A Write Cycle occurs during the overlap of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
2. OE may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CE_1}$, CE_2 or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CE_1}$, CE_2 or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE

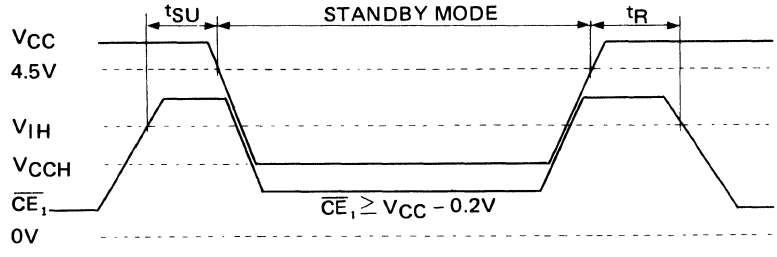


LOW V_{CC} DATA RETENTION CHARACTERISTICS

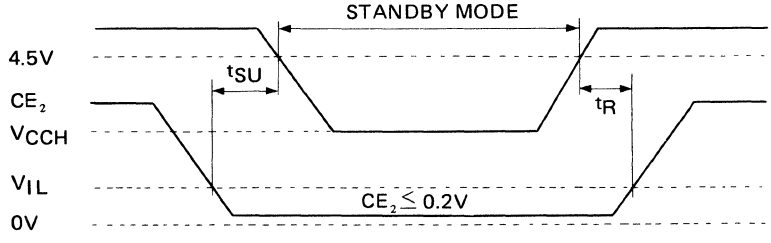
(T_a = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2			V	$\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$
						$CE_2 \leq 0.2V$
Data Retention Current	I_{CCH}			1	mA	V_{CC} = 3V, $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$
						V_{CC} = 3V, $CE_2 \leq 0.2V$
CS to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	t_{RC}			ns	

$\overline{CE}_1$ CONTROL



CE_2 CONTROL



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

MOS MASK ROMS

9

MSM2916RS

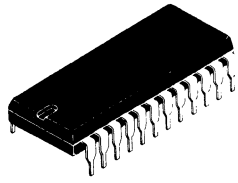
16,384-BITS STATIC 16 K MASK ROM (E3-S-023-32)

GENERAL DESCRIPTION

The MSM2916RS is a 16,384-bits static, N channel MOS Read only memory organized as 2,048 words by 8 bits.
The three-state outputs and TTL inputs/outputs level allow for direct interface with common system bus structures.
The MSM2916RS single +5 V power supply and 250 ns access time are both ideal for usage with high performance microcomputers.
The three chip selects CS_1, CS_2 and CS_3 may be defined by customer and fixed during the masking process.

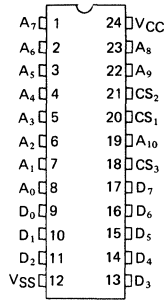
FEATURES

- Organization ..... 2048W x 8 bit
- Static Operation ..... No clocks required
- Supply Voltage ..... 5V ± 10%
- Access Time ..... 250 ns Max.
- Power Dissipation .... 550 mW Max.
- Input Voltage ..... V_{IH} = 2.0V Min., V_{IL} = 0.8V Max.
- Output Voltage ..... V_{OH} = 2.4V Min., V_{OL} = 0.4V Max.
- Package ..... 24 PIN DIP



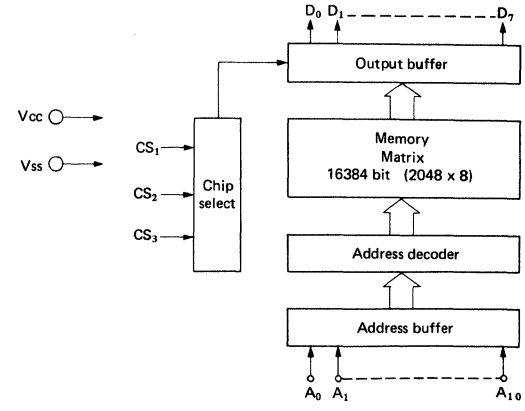
PIN CONFIGURATION

(Top View)



Note: CS_1, CS_2 and CS_3 are programmable CHIP SELECTS

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to +7.0	V
Output Voltage	V_O	−0.3 to +7.0	V
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
"H" Input Voltage	V_{IH}	2.0		Vcc	V
"L" Input Voltage	V_{IL}	−0.3		0.8	V

DC CHARACTERISTICS

(Vcc = 5 V ± 10%, Vss = 0 V, Ta = 0°C to +70°C)

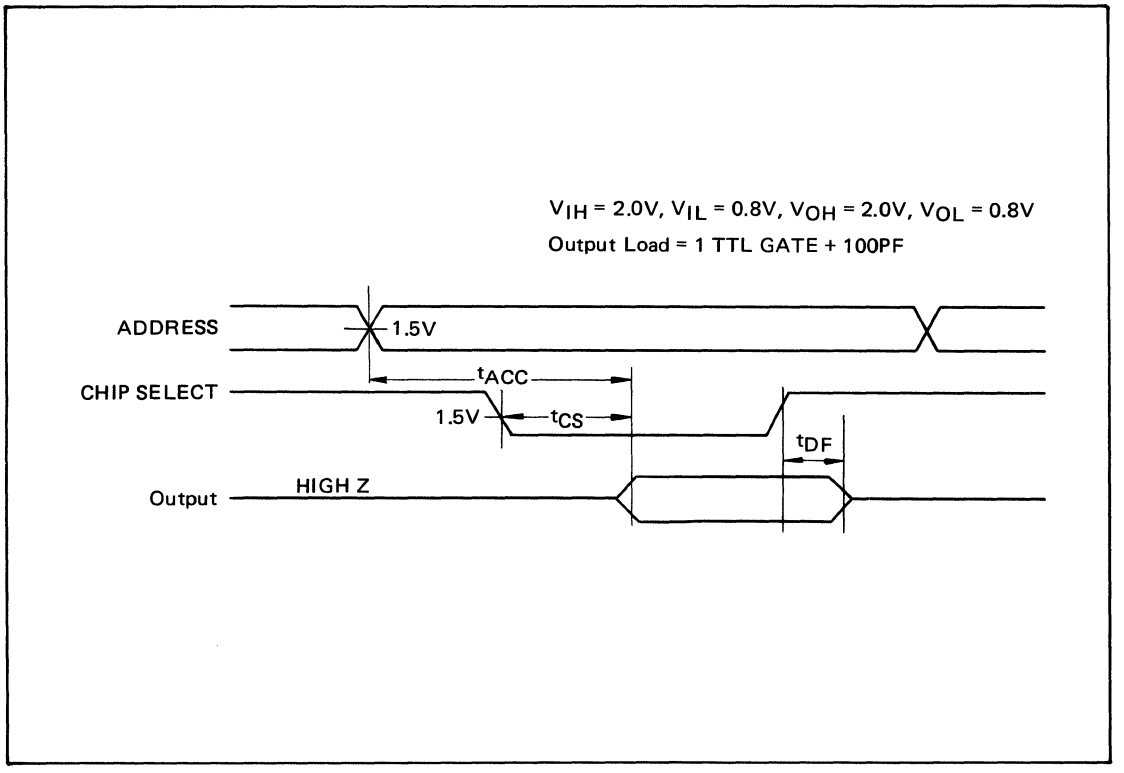
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}		2.0		Vcc	V
"L" Input Voltage	V_{IL}		−0.3		0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = −100μA	2.4			V
"L" Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input Leak Current	I_{LI}	V_I = 0 ~ Vcc	−10		10	μA
Output Leak Current	I_{LO}	V_O = 0 ~ Vcc	−10		10	μA
Power Supply Current	Icc	Vcc = 5.5V			100	mA
Input Capacitance	C_I	V_I = 0V, V_O = 0V f = 1 MHz Ta = 25°C			6	pF
Output Capacitance	C_O				12	pF

AC OPERATING CHARACTERISTICS

(Vcc = 5 V ± 10%, Vss = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
Read Cycle time	t_{CYC}	250		ns
Address Access time	t_{ACC}		250	ns
Chip Select Access time	t_{CS}		150	ns
Output Disable Delay time	t_{DF}		150	ns

9


V_{IH} = 2.0V, V_{IL} = 0.8V, V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load = 1 TTL GATE + 100PF
ADDRESS
1.5V
CHIP SELECT
t_{ACC}
1.5V
t_{CS}
t_{DF}
Output
HIGH Z

9

MSM2932RS

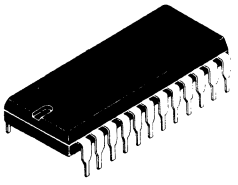
32,768-BITS STATIC-32K MASK ROM (E3-S-024-32)

GENERAL DESCRIPTION

The MSM2932RS is a 32,768-bits static, N channel MOS Read only memory organized as 4,096 words by 8 bits.
The three-state outputs and TTL inputs/outputs level allow for direct interface with common system bus structures.
The MSM2932RS single +5 V power supply and 300 ns access time are both ideal for usage with high performance microcomputers.
The two chip selects CS_1 and CS_2 may be defined by customer and fixed during the masking process.

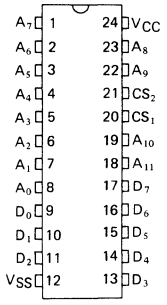
FEATURES

- Organization ..... 4096W x 8 bit
- Static Operation ..... No clocks required
- Supply Voltage ..... 5V ± 10%
- Access Time ..... 300 ns Max.
- Power Dissipation .... 687 mW Max.
- Input Voltage ..... V_{IH} = 2.0V Min., V_{IL} = 0.8V Max.
- Output Voltage ..... V_{OH} = 2.4V Min., V_{OL} = 0.4V Max.
- Package ..... 24 PIN DIP



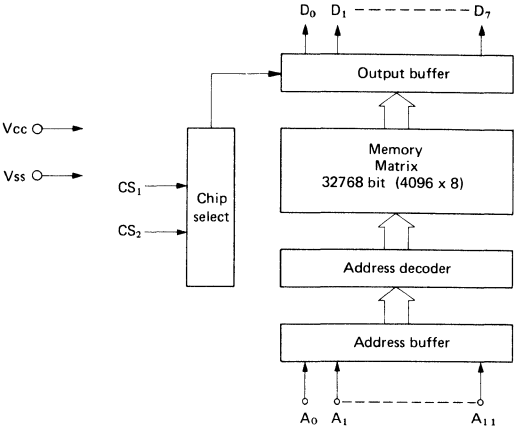
PIN CONFIGURATION

(Top View)



Note: CS_1, CS_2 are programmable CHIP SELECTS

FUNCTIONAL BLOCK DIAGRAM



9

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to +7.0	V
Output Voltage	V_O	−0.3 to +7.0	V
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
"H" Input Voltage	V_{IH}	2.0		Vcc	V
"L" Input Voltage	V_{IL}	−0.3		0.8	V

DC CHARACTERISTICS

(Vcc = 5 V ± 10%, Vss = 0 V, Ta = 0°C to +70°C)

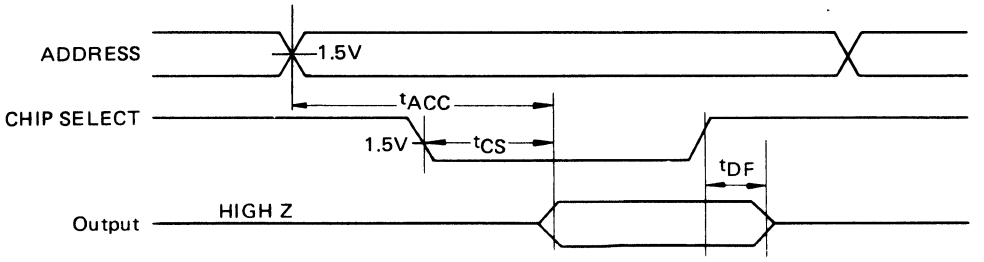
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}		2.0		Vcc	V
"L" Input Voltage	V_{IL}		−0.3		0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = −100μA	2.4			V
"L" Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input Leak Current	I_{LI}	V_I = 0 ~ Vcc	−10		10	μA
Output Leak Current	I_{LO}	V_O = 0 ~ Vcc	−10		10	μA
Power Supply Current	Icc	V_{cc} = 5.5V			125	mA
Input Capacitance	C_I	V_I = 0V, V_O = 0V f = 1 MHz Ta = 25°C			6	pF
Output Capacitance	C_O				12	pF

AC OPERATING CHARACTERISTICS

(Vcc = 5 V ± 10%, Vss = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
Read Cycle time	t_{CYC}	300		ns
Address Access time	t_{ACC}		300	ns
Chip Select Access time	t_{CS}		150	ns
Output Disable Delay time	t_{DF}		150	ns

V_{IH} = 2.0V, V_{IL} = 0.8V, V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load = 1 TTL GATE + 100PF



MSM2965RS

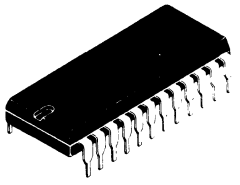
65,536 BITS STATIC-64K MASK ROM (E3-S-025-32)

GENERAL DESCRIPTION

The MSM2965RS is a 65,536-bits static, N channel MOS Read only memory organized as 8,192 words by 8 bits.
The three-state outputs and TTL inputs/outputs level allow for direct interface with common system bus structures.
The MSM2965RS single +5 V power supply and 300 ns access time are both ideal for usage with high performance microcomputers.
CS may be defined by customer and fixed during the masking process.

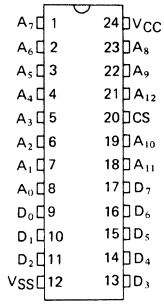
FEATURES

- Organization ..... 8192W x 8 bit
- Static Operation ..... No clocks required
- Supply Voltage ..... 5V ± 10%
- Access Time ..... 300 ns Max.
- Power Dissipation .... 687 mW Max.
- Input Voltage ..... V_{IH} = 2.0V Min., V_{IL} = 0.8V Max.
- Output Voltage ..... V_{OH} = 2.4V Min., V_{OL} = 0.4V Max.
- Package ..... 24 PIN DIP



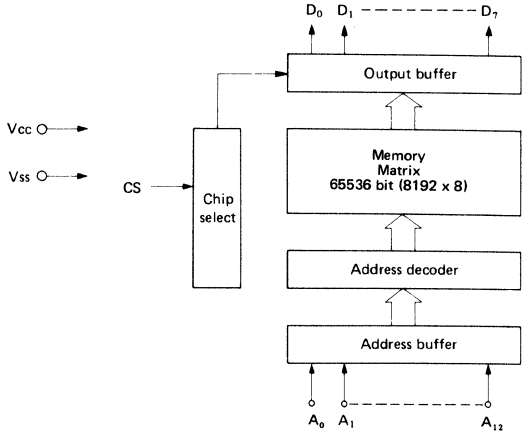
PIN CONFIGURATION

(Top View)



Note: CS is programmable CHIP SELECT

FUNCTIONAL BLOCK DIAGRAM



9

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	−0.3 to +7.0	V
Input Voltage	V_I	−0.3 to +7.0	V
Output Voltage	V_O	−0.3 to +7.0	V
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
"H" Input Voltage	V_{IH}	2.0		Vcc	V
"L" Input Voltage	V_{IL}	−0.3		0.8	V

DC CHARACTERISTICS

(Vcc = 5 V ± 10%, Vss = 0 V, Ta = 0°C to +70°C)

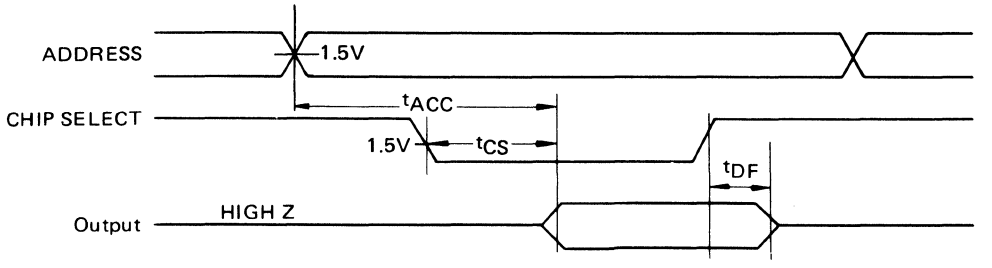
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}		2.0		Vcc	V
"L" Input Voltage	V_{IL}		−0.3		0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = −100μA	2.4			V
"L" Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input Leak Current	I_{LI}	V_I = 0 ~ Vcc	−10		10	μA
Output Leak Current	I_{LO}	V_O = 0 ~ Vcc	−10		10	μA
Power Supply Current	Icc	V_{cc} = 5.5V			125	mA
Input Capacitance	C_I	V_I = 0V, V_O = 0V f = 1 MHz Ta = 25°C			6	pF
Output Capacitance	C_O				12	pF

AC OPERATING CHARACTERISTICS

(Vcc = 5 V ± 10%, Vss = 0 V, Ta = 0°C to +70°C)

Parameter	Symbol	Min.	Max.	Unit
Read Cycle time	t_{CYC}	300		ns
Address Access time	t_{ACC}		300	ns
Chip Select Access time	t_{CS}		100	ns
Output Disable Delay time	t_{DF}		100	ns

V_{IH} = 2.0V, V_{IL} = 0.8V, V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load = 1 TTL GATE + 100PF



9

Preliminary

MSM3864RS

8,192 WORD x 8 BIT MASK ROM (E3-S-026-32)

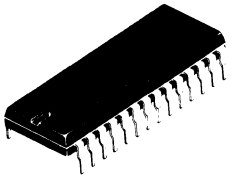
GENERAL DESCRIPTION

MSM3864RS is an N-channel silicon gate E/D MOS device MASK ROM with a 8,192 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs can be directly connected to the TTL. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30 mA (max) when the chip is not selected. The application of a byte system and the convertibility of the pins with a programmable ROM whose memory can be erased by ultraviolet ray radiation is most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

As it provides CE, OE, and CS as the control signal, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

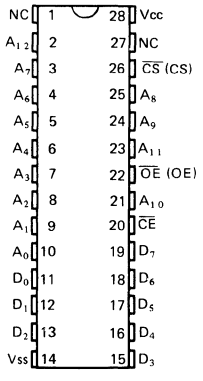
FEATURES

- 5V single power supply
- 8,192 words x 8 bits
- Access time: 200 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

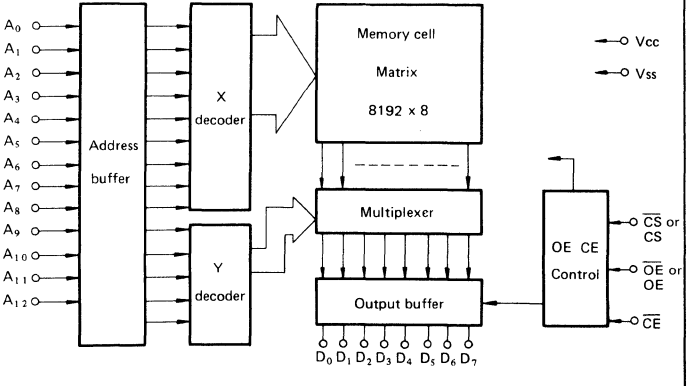
(Top View)



$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply
$A_0 \sim A_{12}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable
$\overline{CS}$	:	Chip select

Note: Please specify the OE active level and CS active level or open in ordering this IC.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	Respect to V_{SS}
Output Voltage	V_O	−0.5 to 7	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	–	4.5	5	5.5	V
	V_{SS}	–	0	0	0	V
Input Signal Level	V_{IH}	–	2	5	6	V
	V_{IL}	–	−0.5	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	–	Vcc	V
	V_{OL}	I_{OL} = 2.1 mA		–	0.4	V
Input Leak Current	I_{LI}	V_I = 0V or V_{CC}	−10	–	10	μA
Output Leak Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	–	10	μA
Power Supply Current	Icc	Vcc = Max. I_O = 0 mA	–	–	100	mA
	Iccs	Vcc = Max.	–	–	30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = V_{CC} or V_{IH}	–	–	60	mA
Operating Temperature	T_{opr}	–	0	–	70	°C

AC CHARACTERISTICS

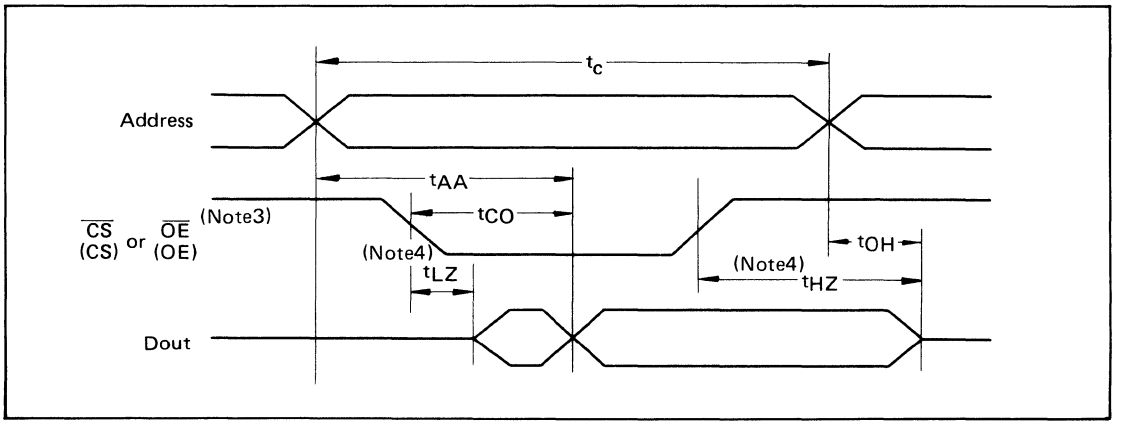
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH}=2.0V V_{IL}=0.8V
Input Rising, Falling Time	tr=ty=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

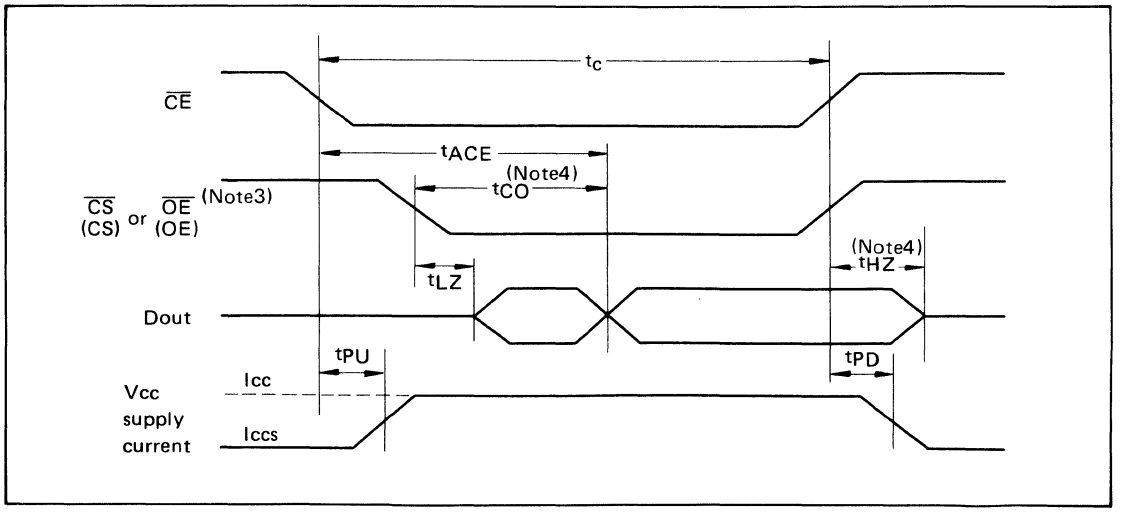
READ CYCLE

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_c	200	–		ns	
Address Access Time	t_{AA}	–	–	200	ns	
Chip Enable Access Time	t_{ACE}	–	–	200	ns	
Output Delay Time	t_{CO}	–	–	100	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	0	–	100	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	
Power Up Time	t_{PU}	0	–	100	ns	
Power Down Time	t_{PD}	–	–	100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Note: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) The $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{LZ} is determined by the later level, $\overline{CE}$ "L"/$\overline{CS}$ "L" or $\overline{OE}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H"/$\overline{CS}$ "H" or $\overline{OE}$ "H".
While, t_{HZ} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		10	pF	V_O=0V

MSM38128RS

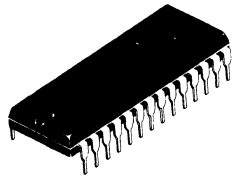
16384 WORD x 8 BIT MASK ROM (E3-S-027-32)

GENERAL DESCRIPTION

MSM38128RS is an N-channel silicon gate E/D MOS device ROM with a 16,384 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs can be directly connected to the TTL. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 20 mA (max) when the chip is not selected. The application of a byte system and the convertibility of the pins with a programmable ROM whose memory can be erased by ultraviolet ray radiation is most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
Since it provides both CE and OE signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

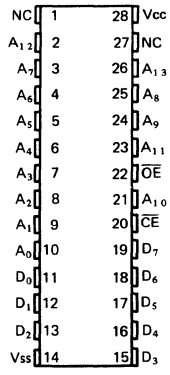
FEATURES

- 16384 words x 8 bits
- 5V single power supply
- Access time: 450 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

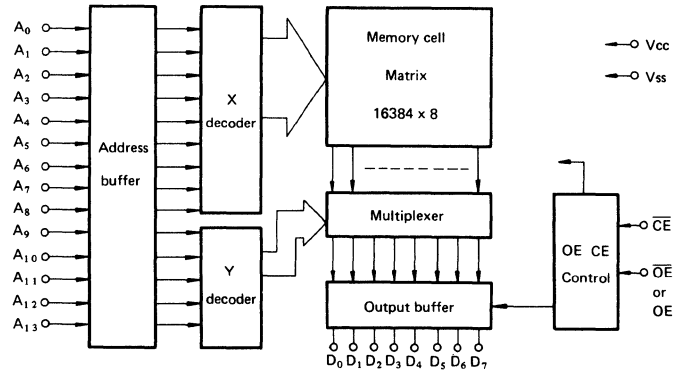
(Top View)



$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply voltage
$A_0 \sim A_{13}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable

Note: The $\overline{OE}$ active level is specified by customer.

FUNCTIONAL BLOCK DIAGRAM



9

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	
Output Voltage	V_O	−0.5 to 7	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{cc}		4.5	5	5.5	V
	V_{ss}		0	0	0	V
Input Signal Level	V_{IH}		2		6	V
	V_{IL}		−0.5		0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4		Vcc	V
	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input Leak Current	I_{LI}	V_I = 0V or V_{cc}	−10		10	μA
Output Leak Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10		10	μA
Power Supply Current	Icc	Vcc = Max. I_O = 0 mA			120	mA
	Iccs	Vcc = Max.			20	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = Vco or V_{IH}			20	mA
Operating Temperature	T_{opr}		0		70	°C

9

AC CHARACTERISTICS

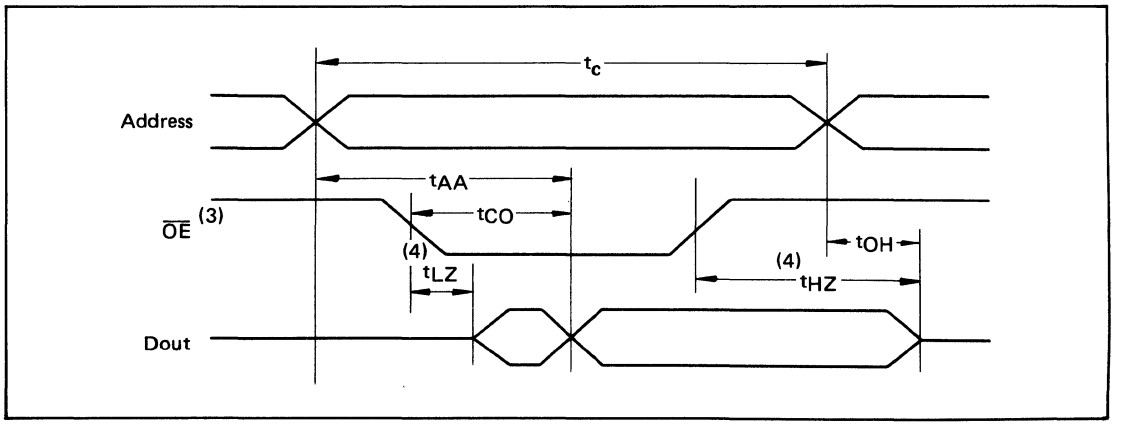
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH}=2.0V V_{IL}=0.8V
Input Rising, Falling Time	tr=ty=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8 & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

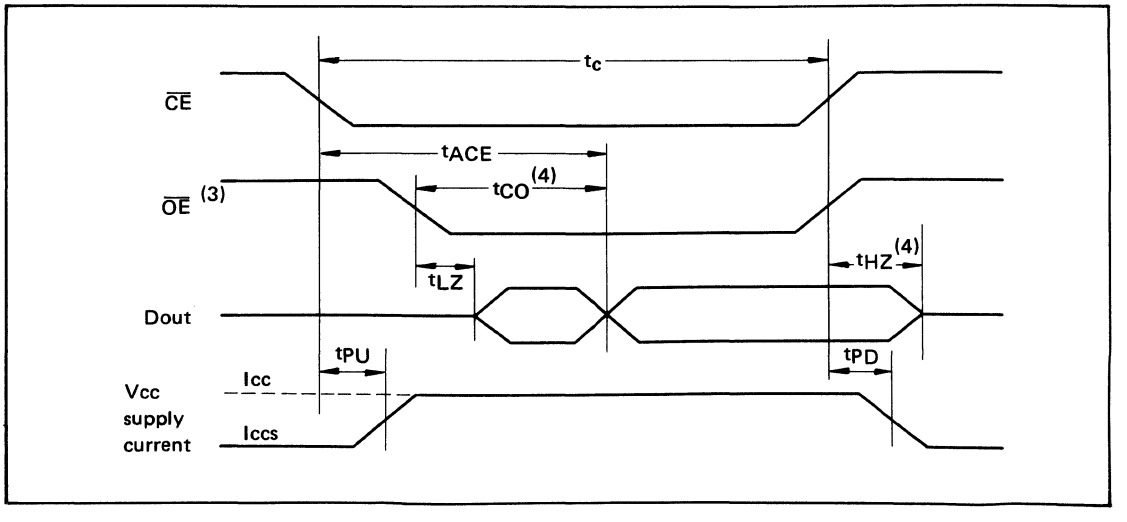
READ CYCLE

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_c	450			ns	
Address Access Time	t_{AA}			450	ns	
Chip Enable Access Time	t_{ACE}			450	ns	
Output Delay Time	t_{CO}			150	ns	
Output Setting Time	t_{LZ}	20			ns	
Output Disable Time	t_{HZ}	0		120	ns	
Output Retaining Time	t_{OH}	20			ns	
Power Up Time	t_{PU}	0		120	ns	
Power Down Time	t_{PD}			120	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Note: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) $\overline{OE}$ is shown in the negative logic here, however the active level is freely selected.
(4) t_{CO} and t_{LZ} are determined by the later $\overline{CE}$ "L" or $\overline{OE}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H" or $\overline{OE}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		10	pF	V_O=0V

9

OKI semiconductor

MSM38128ARS

16,384 WORD x 8 BIT MASK ROM (E3-S-028-32)

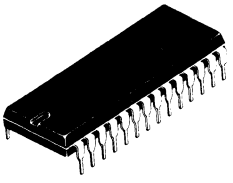
GENERAL DESCRIPTION

MSM38128ARS is an N-channel silicon gate E/D MOS device MASK ROM with a 16,384 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs can be directly connected to the TTL. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30mA (max) when the chip is not selected. The application of a byte system and the convertibility of the pins with a programmable ROM whose memory can be erased by ultraviolet ray radiation is most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

As it provides CE, OE, and CS as the control signal, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

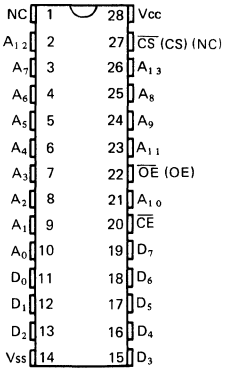
FEATURES

- 5V single power supply
- 16384 words x 8 bits
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

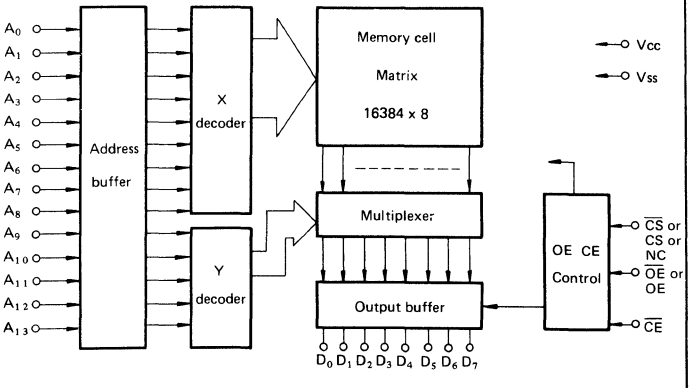
(Top View)



$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply
$A_0 \sim A_{12}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable
$\overline{CS}$	:	Chip select

Note: Please specify the OE active level and CS active level or open in ordering this IC.

FUNCTIONAL BLOCK DIAGRAM



9

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	Respect to V_{SS}
Output Voltage	V_O	−0.5 to 7	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	–	4.5	5	5.5	V
	V_{SS}	–	0	0	0	V
Input Signal Level	V_{IH}	–	2	–	6	V
	V_{IL}	–	−0.5	–	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	–	Vcc	V
	V_{OL}	I_{OL} = 2.1 mA		–	0.4	V
Input Leak Current	I_{LI}	V_I = 0V or V_{CC}	−10	–	10	μA
Output Leak Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	–	10	μA
Power Supply Current	Icc	Vcc = Max. I_O = 0 mA	–	–	100	mA
	Iccs	Vcc = Max.	–	–	30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = V_{CC} or V_{IH}	–	–	60	mA
Operating Temperature	T_{opr}	–	0	–	70	°C

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AC CHARACTERISTICS

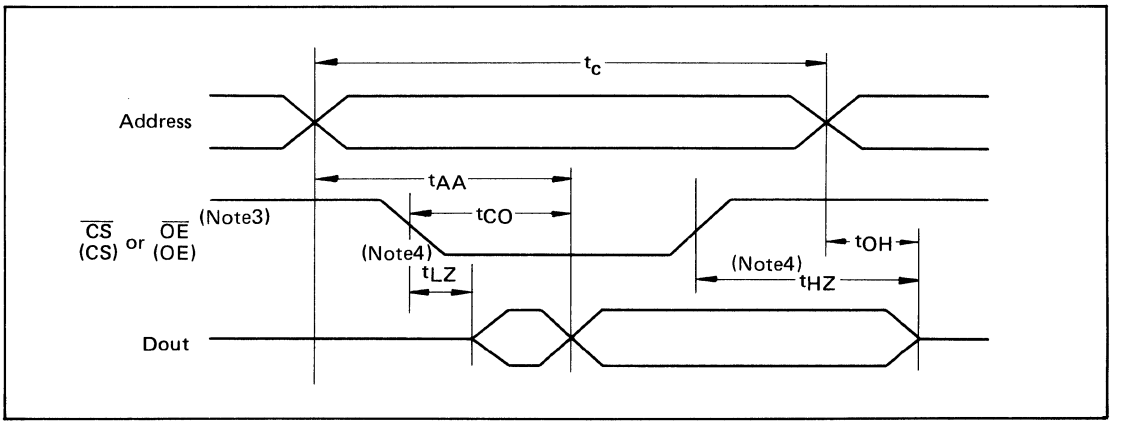
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH}=2.0V V_{IL}=0.8V
Input Rising, Falling Time	tr=ty=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

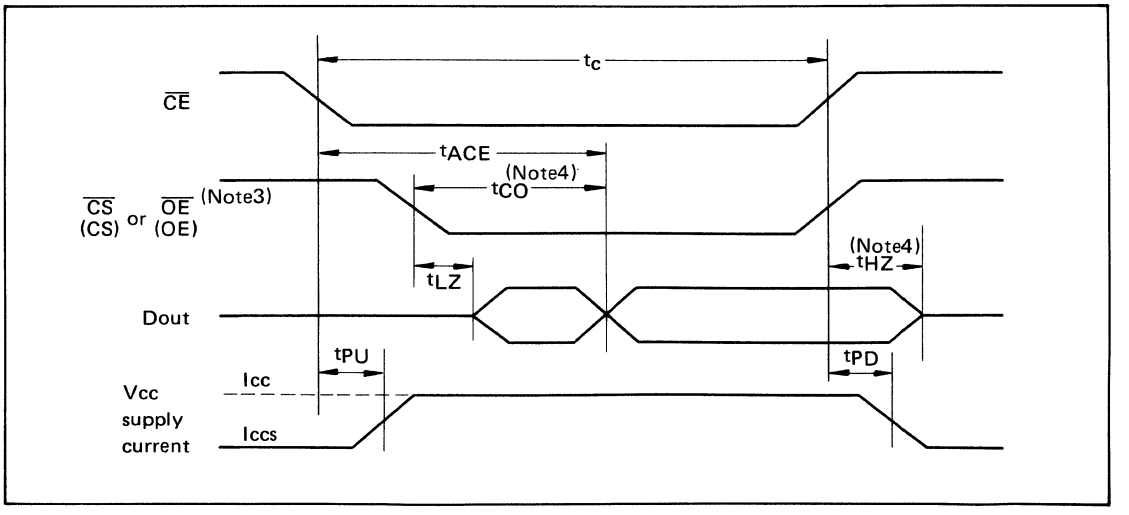
READ CYCLE

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	250	—		ns	
Address Access Time	t_{AA}	—	—	250	ns	
Chip Enable Access Time	t_{ACE}	—	—	250	ns	
Output Delay Time	t_{CO}	—	—	100	ns	
Output Setting Time	t_{LZ}	10	—	—	ns	
Output Disable Time	t_{HZ}	0	—	100	ns	
Output Retaining Time	t_{OH}	10	—	—	ns	
Power Up Time	t_{PU}	0	—	100	ns	
Power Down Time	t_{PD}	—	—	100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Note: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) The $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{LZ} is determined by the later level, $\overline{CE}$ "L"/$\overline{CS}$ "L" or $\overline{OE}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H"/$\overline{CS}$ "H" or $\overline{OE}$ "H".
While, t_{HZ} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		10	pF	V_O=0V

Preliminary

MSM38256RS

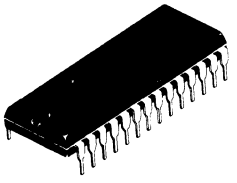
32768 WORD x 8 BIT MASK ROM (E3-S-029-32)

GENERAL DESCRIPTION

MSM38256RS is an N-channel silicon gate E/D MOS device ROM with a 32,768 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs can be directly connected to the TTL. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30 mA (max) when the chip is not selected. The application of a byte system and the convertibility of the pins with a programmable ROM whose memory can be erased by ultraviolet ray radiation is most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
Since it provides CE, CS and OE signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

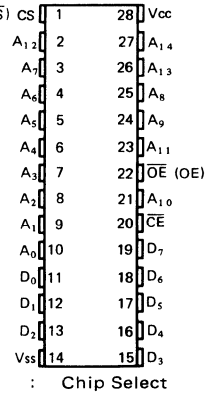
FEATURES

- 32768 words x 8 bits
- 5V single power supply
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

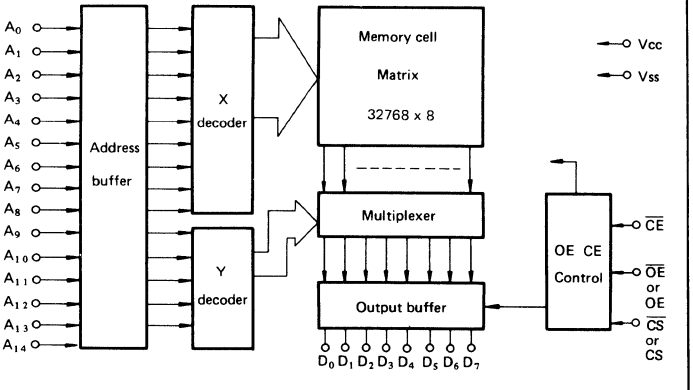
(Top View)



CS	:	Chip Select
$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply voltage
$A_0 \sim A_{13}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable

Note: The $\overline{OE}$ active level and CS active level are specified by customer.

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	
Output Voltage	V_O	−0.5 to 7	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{cc}		4.5	5	5.5	V
	V_{ss}		0	0	0	V
Input Signal Level	V_{IH}		2		6	V
	V_{IL}		−0.5		0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4		Vcc	V
	V_{OL}	I_{OL} = 2.1 mA			0.4	V
Input Leak Current	I_{LI}	V_I = 0V or V_{cc}	−10		10	μA
Output Leak Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10		10	μA
Power Supply Current	Icc	Vcc = Max. I_O = 0 mA			120	mA
	Iccs	Vcc = Max.			30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = Vco or V_{IH}			60	mA
Operating Temperature	T_{opr}		0		70	°C

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AC CHARACTERISTICS

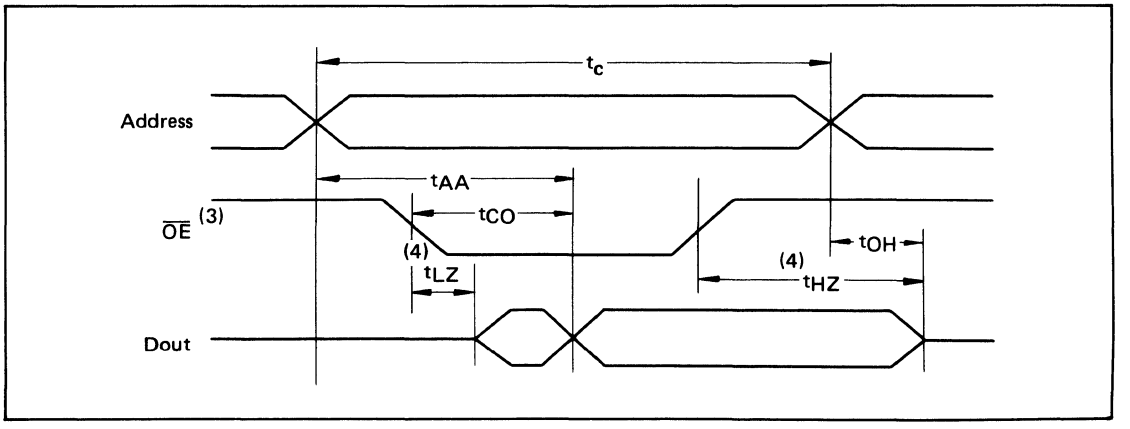
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH}=2.0V V_{IL}=0.8V
Input Rising, Falling Time	tr=ty=15 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8 & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

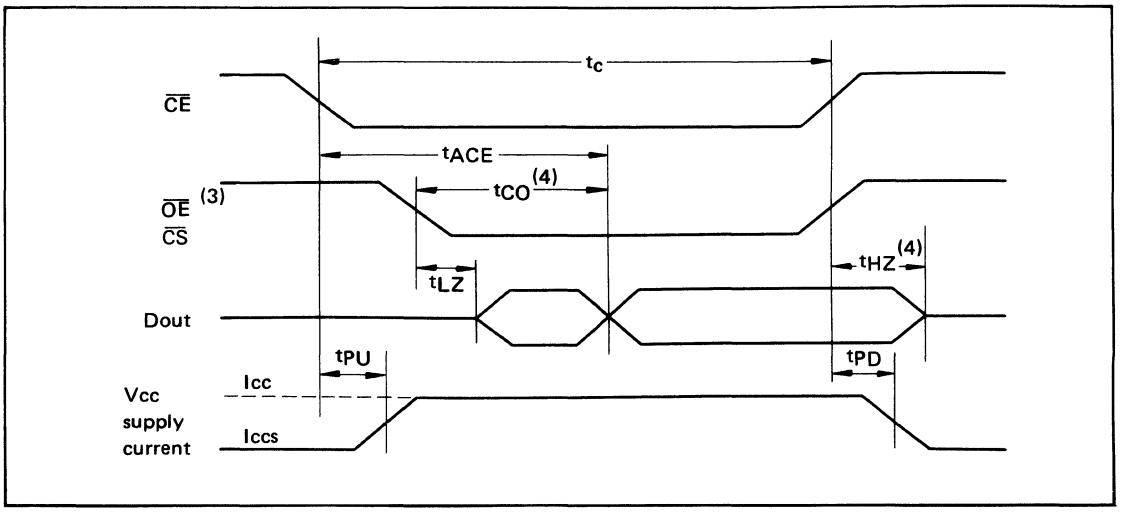
READ CYCLE

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	250			ns	
Address Access Time	t_{AA}			250	ns	
Chip Enable Access Time	t_{ACE}			250	ns	
Output Delay Time	t_{CO}			100	ns	
Output Setting Time	t_{LZ}	10			ns	
Output Disable Time	t_{HZ}	0		100	ns	
Output Retaining Time	t_{OH}	10			ns	
Power Up Time	t_{PU}	0			ns	
Power Down Time	t_{PD}			100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



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Note: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{CO} and t_{LZ} are determined by the later $\overline{CE}$ "L", $\overline{OE}$ "L" or $\overline{CS}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H", $\overline{OE}$ "H" or $\overline{CS}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I		8	pF	V_I=0V
Output Capacitance	C_O		10	pF	V_O=0V

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Preliminary

MSM38256ARS

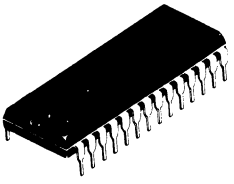
32768 WORD x 8 BIT MASK ROM (E3-S-030-32)

GENERAL DESCRIPTION

MSM38256RS is an N-channel silicon gate E/D MOS device ROM with a 32,768 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs can be directly connected to the TTL. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30 mA (max) when the chip is not selected. The application of a byte system and the convertibility of the pins with a programmable ROM whose memory can be erased by ultraviolet ray radiation is most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
Since it provides both CE and OE signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

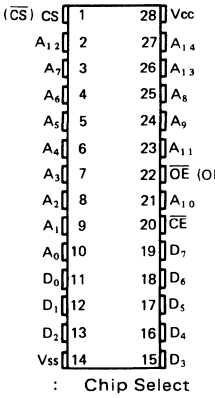
FEATURES

- 32768 words x 8 bits
- 5V single power supply
- Access time: 200 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

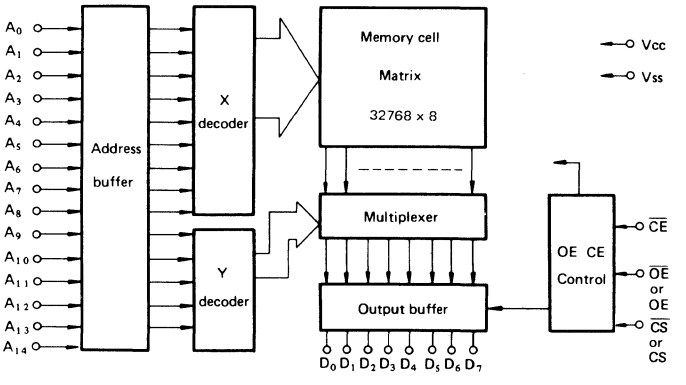
(Top View)



CS	:	Chip Select
$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply voltage
$A_0 \sim A_{13}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable

Note: The $\overline{OE}$ active level and CS active level are specified by customer.

FUNCTIONAL BLOCK DIAGRAM



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MSM28101AAS

JAPANESE-CHARACTER GENERATING 1M BIT MASK ROM (E3-S-032-32)

GENERAL DESCRIPTION

MSM28101AAS is a 1M Bit Mask ROM using the N channel silicon gate MOS process which stores 3,760 characters of numeric characters, Japanese cursive and square syllabarys, JIS 1st standard Japanese-characters, etc., in one chip.

Since it is of large capacity, Japanese-character pattern of 3,760 characters can be generated with only one chip. Furthermore, since the dot matrix character form of 18 lines x 16 strings is available from the data out pin by only inputting the JIS Japanese-character code into the address pin, it excels in functioning property and proves optimum for constituting the Japanese-character terminal.

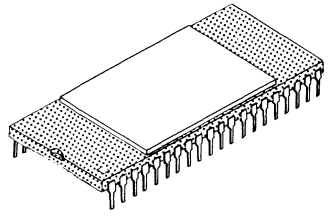
The power supply voltage is of 5 V single power supply, the input level is of TTL compatible, the data output is of 3-state output, the data valid is the output of the open collector and is packaged on the 40-pin DIP.

FEATURES

- Function: 18 x 16 chinese-character font output
- Configuration: Duplex configuration of cell-array using the defect permissible technique
- Storage capacity: 1082880 Bits
- Number of generating characters: 3,418 characters
- Storage character range: Partition 0 ~ 7 and partition 16 ~ 47 of Japanese-character code system for JIS information processing
- Address input: 14 Bits ($A_0 \sim A_{13}$)
- Data output: 16 Bits ($\overline{D_0} \sim \overline{D_{15}}$, 3-state)
- Output mode: 16 Bits x 18 times transfer
- Address enable: 1 each (AE)
- Data valid: 1 each ($\overline{DV}$, open collector output)
- Clock: 1 each (ϕT) DC ~ 1.5MHz
- Used temperature: Ta = 0 ~ 70°C
- Access time: 10 μs MAX
- Data transfer rate: 22 μs/character
- Interface: TTL level
- Power supply voltage: 5V single power supply (±5%)
- Power consumption: 700 mW TYP
- Package: Side-brazed 40-pin DIP
- Process: E/D MOS process
- Memory cell: Multi-gate ROM

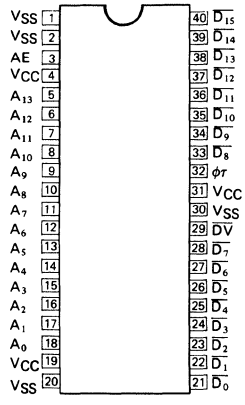
This specification is sometimes subject to change without notice

9



PIN CONFIGURATION

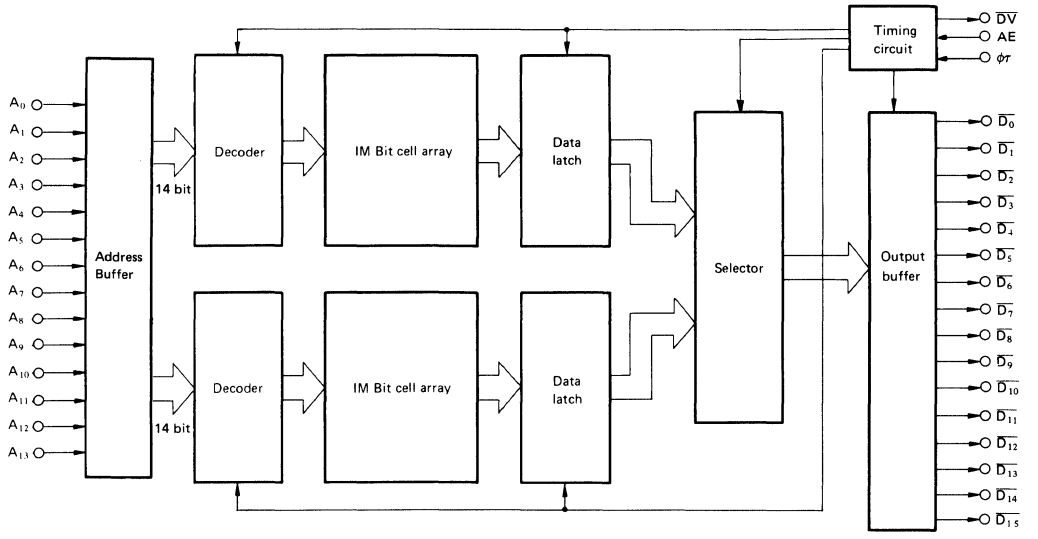
(Top View)



$A_0 \sim A_{13}$: Address input
$\overline{D_0} \sim \overline{D_{15}}$: Data output
AE: Address enable
$\overline{DV}$: Data valid output
ϕT: Clock input
V_{CC}: Power supply voltage (5V)
V_{SS}: GND (OV)

(Note) Connect all V_{CC} and V_{SS} terminals.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Conditions	Value	Unit
Power Supply Voltage	Vcc	Respect to Vss	−0.5 ~7	V
Input Terminal Voltage	V_{IN}	Respect to Vss	−0.5 ~7	V
Output Terminal Voltage	V_{OUT}	Respect to Vss	−0.5 ~7	V
Permissible Loss	P_D		2	W
Operating Temperature	T_{opr}		0 ~70	°C
Storage Temperature	T_{stg}		−35 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Specification value			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	Vcc	5V ± 5%	4.75	5	5.25	V
Power Supply Voltage	Vss		0	0	0	V
Input Signal Level	V_{IH}	Respect to Vss	2.0	5	6	V
	V_{IL}	Respect to Vss	−0.5	0	0.8	V
Operating Temperature	Topr		0		70	°C

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DC CHARACTERISTICS

(Vcc = 5V ±5%, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Specification value			Unit
			Min.	Typ.	Max.	
Output Signal Level	V_{OH}	I_{OH}=−0.2 mA	2.4		Vcc	V
	V_{OL}	I_{OL} =1.6 mA			0.4	V
Input Leak Current	I_{LI}	V_{IN}=0 ~Vcc	−10		10	μA
Output Leak Current	I_{LO}	V_{OUT}=0 ~Vcc V_{AE}=0.8V	−10		10	μA
Average Power Supply Current	I_{CCA}	t_{RC}=22μs t_C=650 ms t_{AR}=300 ns			170	mA
Steady State Power Supply Current	I_{CCS}	V_{AE}=0.8V			170	mA

AC CHARACTERISTICS

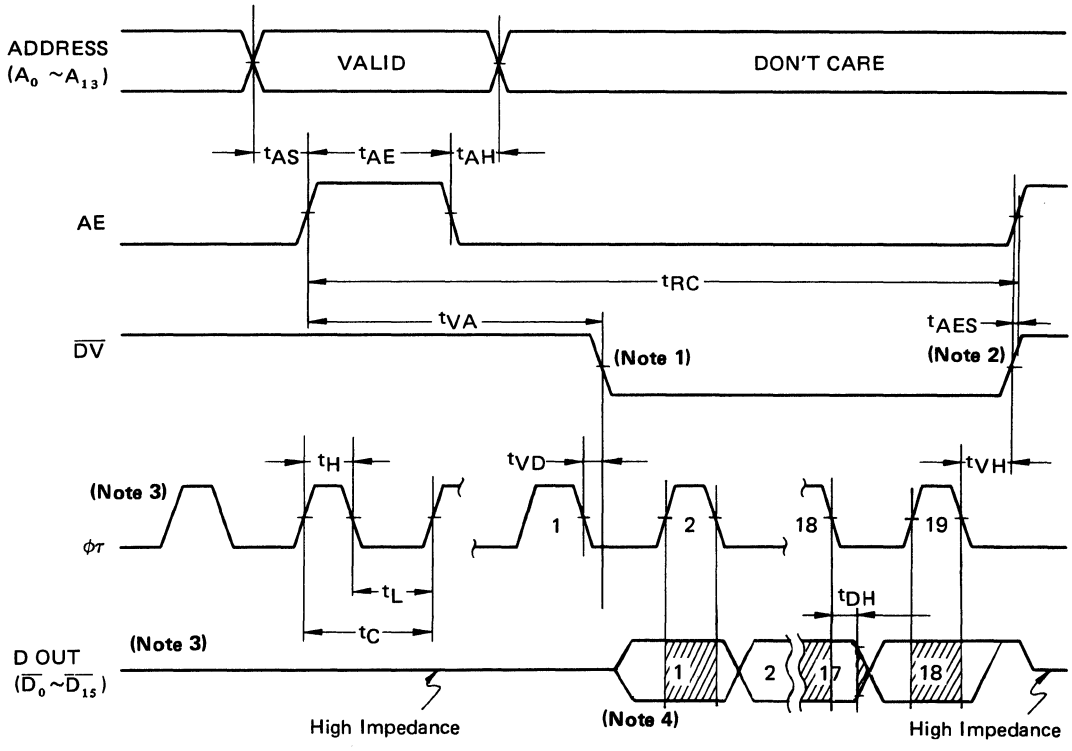
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH} = 2.0V, V_{IL} = 0.8V
Input Rising, Falling Time	t_r = t_f = 15 ns
Input Timing Level	1.5V
Loading Condition	C_L = 50 pF, 1TTL Gate

READ CYCLE

(Vcc = 5V ±5%, T_a = 0°C to +70°C)

Parameter	Symbol	Conditions	Specification Value			Unit
			Min.	Typ.	Max.	
Read Cycle Time	t_{RC}		22			μS
Address Setting Time	t_{AS}		0			ns
AE Pulse Width	t_{AE}		300			ns
Address Retaining Time	t_{AH}		100			ns
$\overline{DV}$ Access Time	t_{VA}				10	μS
$\overline{DV}$ Delay Time	t_{VD}				150	ns
$\overline{DV}$ Retaining Time	t_{VH}				100	ns
ϕ_T Pulse Width	t_H		200			ns
ϕ_T Delay Time	t_L		450			ns
Output Retaining Time	t_{DH}		50			ns
AE Setting Time	t_{AES}		0			ns



(Note 1) $\overline{DV}$ is determined by the falling of $\phi\tau$.
(Note 2) $\overline{DV}$ changes with the falling of $\phi\tau$.
(Note 3) $\phi\tau$ and Dn DATA are repeated 18 times during $\overline{DV}$ is Low.
(Note 4) The $\overline{Dn}$ timing levels are 2.0 V and 0.8 V.
(Note 5) Sometimes it will not normally operate unless input is made at least once with AE as the dummy after input of power supply.
(Note 6) $\overline{DV}$ is an open collector output and $\overline{Dn}$ is a 3-stage output.

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INPUT/OUTPUT CAPACITANCE

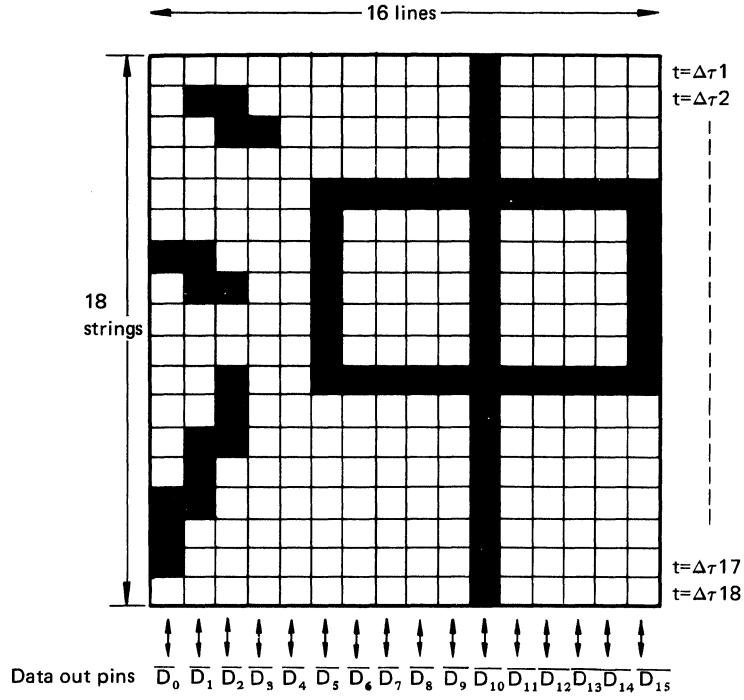
(Ta = 25°C, f = 1 MHz)

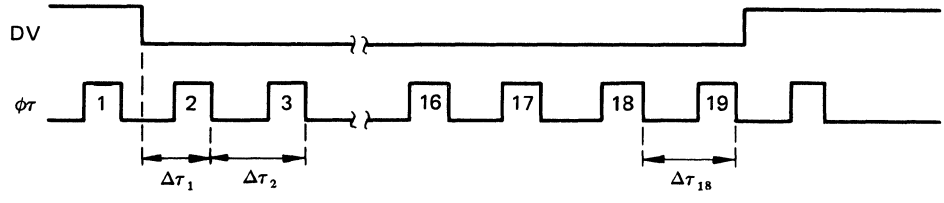
Parameter	Symbol	Conditions	Specification value			Unit
			Min.	Typ.	Max.	
Input Capacitance (excluding AE)	C_{IN}	V_{IN} = OV			8	pF
Input Capacitance (AE terminal)	C_{IN}	V_{IN} = OV			15	pF
Output Capacitance	C_{OUT}	V_{OUT} = OV			8	pF

FUNCTIONAL CHARACTERISTICS

Parameter	Specification	Unit	Remarks
Font Type	18 lines x 16 strings dot matrix		
Output Mode	16 bits x 18 times transfer		**(Note 1)**
Number of Generating characters	3418	Word	
Storage Character Range	0 ~ 7 (Non chinese-character area) 16 ~ 47 (JIS 1st standard)	Partition	**(Note 2)**

(Note 1) The correspondence of the 18 lines x 16 strings matrix and the data out pins are as shown in the diagram below.
Output for the character portion will be Low (V_{OL}) and the output for the background portion will be High (V_{OH}).





(Note 2) The correspondence of the 1st and 2nd bytes of JIS C 6226 and the address pins are as shown below.

JIS C 6226	Second byte							First byte						
	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_7	b_6	b_5	b_4	b_3	b_2	b_1
Address Pin	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

OKI semiconductor

MSM28201AAS

1M BIT MASK ROM FOR JAPANESE-CHARACTER PATTERN (E3-S-033-32)

GENERAL DESCRIPTION

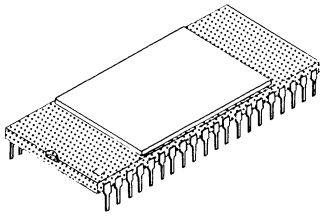
MSM28201AAS is a 1M-bit mask ROM employing an N-channel silicon gate MOS process, and with 3760 Japanese-characters (kanji conforming with JIS no. 2 standards) incorporated in single chip.

With this large capacity, 3760 Japanese-character patterns can be generated in a single chip. And by only a single input of JIS Japanese-character code via the address pin, 18-row x 16-column dot matrix character forms can be obtained from the data output pin, making this device ideal for construction of functionally versatile Japanese-character terminals.

The power supply voltage is 5V single, the input level TTL compatible, outputs are tri-state data out, and data valid is denoted by open collector. The device is mounted in a 40-pin DIP.

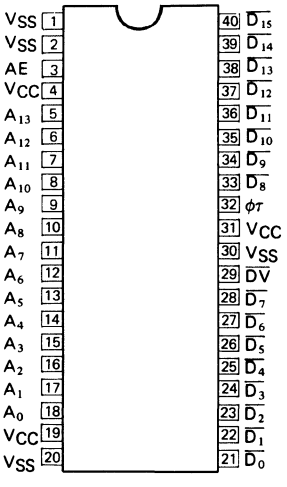
FEATURES

- Function . . . . . 18 x 16 chinese-character font output
- Configuration . . . . Duplex configuration employing defect permissible technique
- Storage capacity . . . 1082880 bits
- Number of generated characters . . . . . 3384 characters
- Accommodation character region . . . Japanese-character encoded partitions 48 to 87 for JIS data processing.
- Address input . . . . 14 bits (A_0 to A_{13})
- Data output . . . . . 16 bits ($\overline{D_0}$ to $\overline{D_{15}}$, tristate)
- Output mode . . . . 16 bit x 18 transfers
- Address enable . . . 1 (AE)
- Data valid . . . . . 1 ($\overline{DV}$, open collector output)
- Clock . . . . . 1 (ϕT) DC to 1.5MHz
- Operating temperature . . . . . Ta=0°C to 70°C
- Access time . . . . . 10 μs MAX.
- Data transfer rate . . 22 μs/character
- Interface . . . . . TTL level
- Power supply voltage 5V single (±5%)
- Power consumption . 700 mW TYP
- Package . . . . . Side-brazed 40-pin DIP
- Process . . . . . E/D MOS process
- Memory cell . . . . . Multi-gate ROM



PIN CONFIGURATION

(Top View)



$A_0 \sim A_{13}$: Address inputs
$\overline{D_0} \sim \overline{D_{15}}$: Data outputs
AE : Address enable
$\overline{DV}$: Data valid output
ϕT : Clock input
Vcc : Power supply voltage (5 V)
Vss : GND (0 V)

Note: All Vss pins are to be connected

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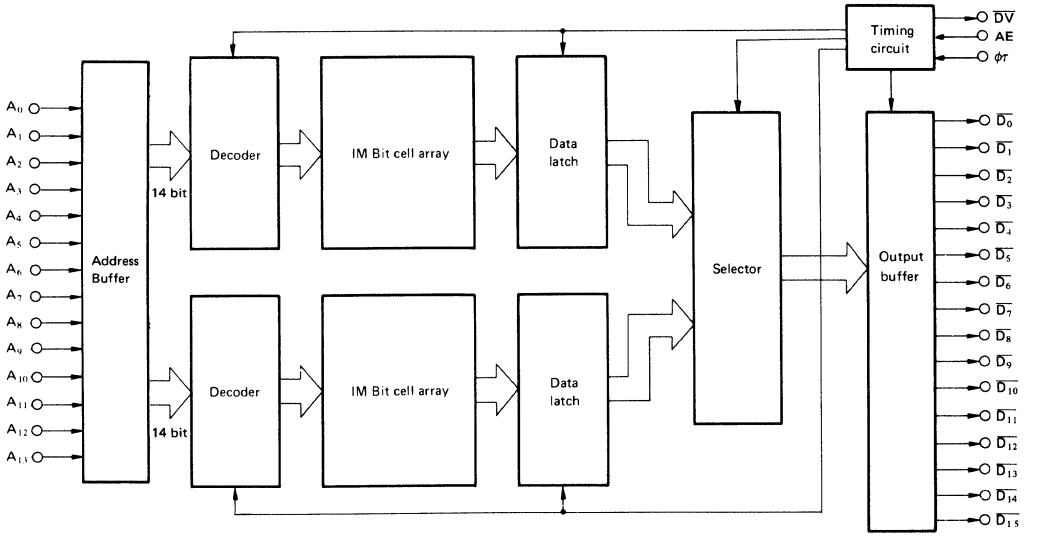
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Conditions	Value	Unit
Power Supply Voltage	Vcc	Respect to Vss	−0.5~7	V
Input Voltage	V_I	Respect to Vss	−0.5~7	V
Output Voltage	V_O	Respect to Vss	−0.5~7	V
Permissible Loss	P_D		2	W
Operating Temperature	Topr		0 ~ 70	°C
Storage Temperature	Tstg		−35~125	°C

9

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Range Value			Unit
			Min	Typ	Max	
Power Supply Voltage	Vcc	5 V ± 5%	4.75	5	5.25	V
Power Supply Voltage	Vss		0	0	0	V
"H" Input Voltage	V_{IH}	Respect to Vss	2.0	5	6	V
"L" Input Voltage	V_{IL}	Respect to Vss	−0.5	0	0.8	V
Operating Temperature	Topr		0		70	°C

DC CHARACTERISTICS

(V_{CC} = 5V ±5%, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Range Value			Unit
			Min.	Typ.	Max.	
"H" Output Voltage	V_{OH}	I_{OH} = −0.2 mA	2.4		V_{CC}	V
"L" Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input Leak Current	I_{LI}	V_I = 0 ~ V_{CC}	−10		10	μA
Output Leak Current	I_{LO}	V_O = 0 ~ V_{CC} V_{AE} = 0.8V	−10		10	μA
Average Power Supply Current	I_{CCA}	t_{RC} = 22μS, t_C = 650 ns t_{AE} = 300ns			170	mA
Rated Power Supply Current	I_{CCS}	V_{AE} = 0.8V			170	mA

AC CHARACTERISTICS

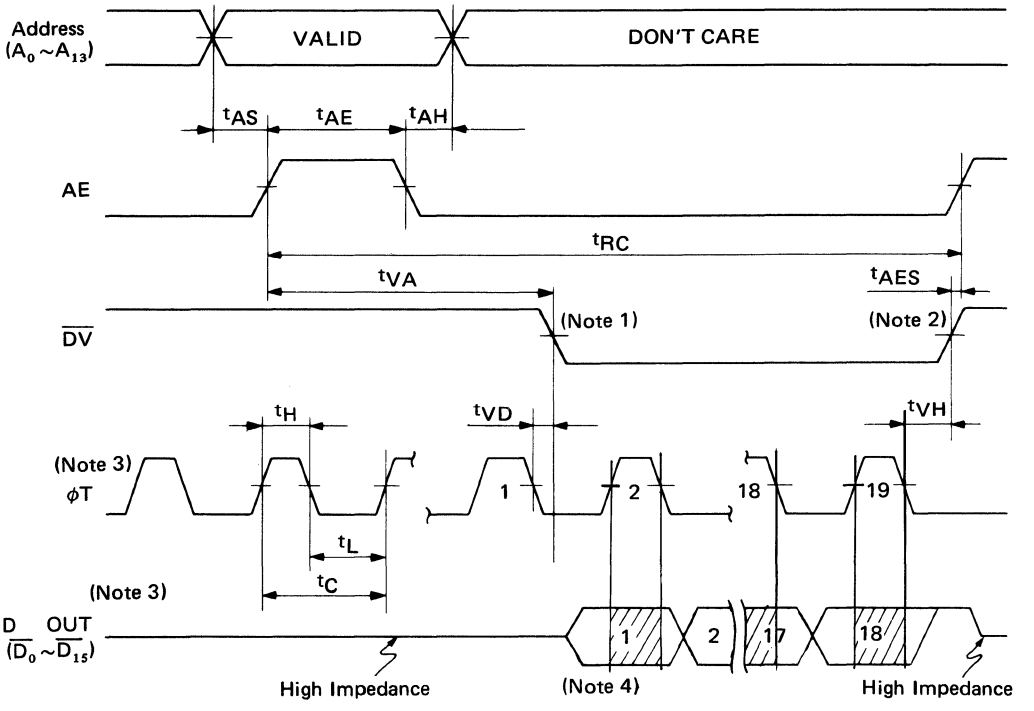
TIMING CONDITIONS

Parameter	Conditions
Input Signal Level	V_{IH}=2.0 V, V_{IL}=0.8 V
Input Rise/Fall Time	tr=tf=15ns
Input Timing Level	1.5V
Output Load	C_L=50pF, 1TTL Gate

READ CYCLE

(V_{CC} = 5V ±5%, Ta = 0°C to +70°C)

Parameter	Symbol	Conditions	Specification Value			Unit
			Min.	Typ.	Max.	
Read Cycle Time	t_{RC}		22			μS
Address Setting Time	t_{AS}		0			ns
AE Pulse Width	t_{AE}		300			ns
Address Retaining Time	t_{AH}		100			ns
$\overline{DV}$ Access Time	t_{VA}				10	μS
$\overline{DV}$ Delay Time	t_{VD}				150	ns
$\overline{DV}$ Retaining Time	t_{VH}				100	ns
ϕ_T Pulse Width	t_H		200			ns
ϕ_T Delay Time	t_L		450			ns
Output Retaining Time	t_{DH}		50			ns
AE Setting Time	t_{AES}		0			ns



NOTE:
1. $\overline{DV}$ is determined by the ϕT falling edge.
2. $\overline{DV}$ is changed by the ϕT falling edge.
3. ϕT and DnDATA are repeated 18 times when $\overline{DV}$ is low.
4. $\overline{Dn}$ timing levels of 2.0V and 0.8V.
5. Normal operation may not be possible unless there is at least one AE dummy input after the power is switched on.
6. $\overline{DV}$ denotes open collector output, and $\overline{Dn}$ the tristate output.

9

INPUT/OUTPUT CAPACITANCE

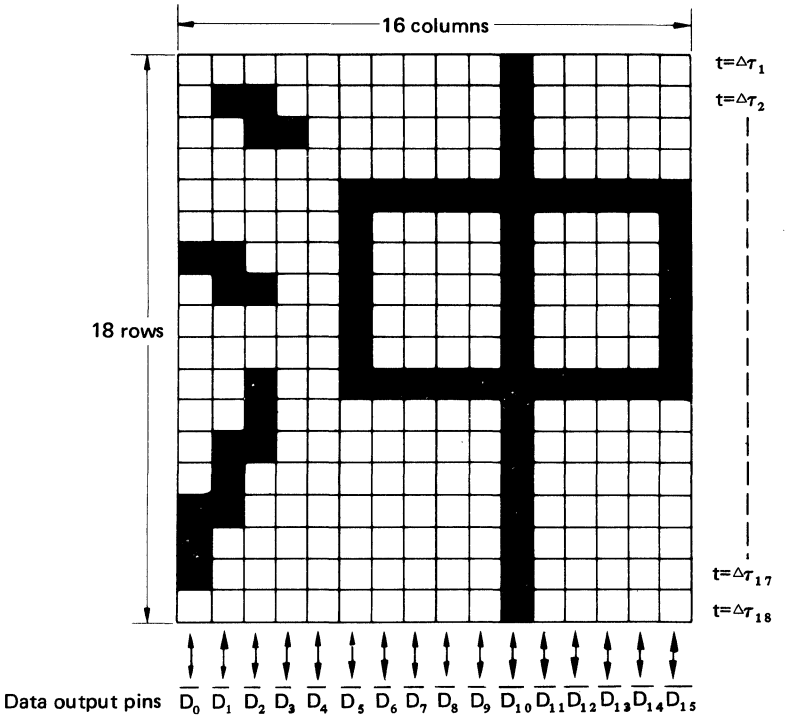
(Ta=25°C, f=1 MHz)

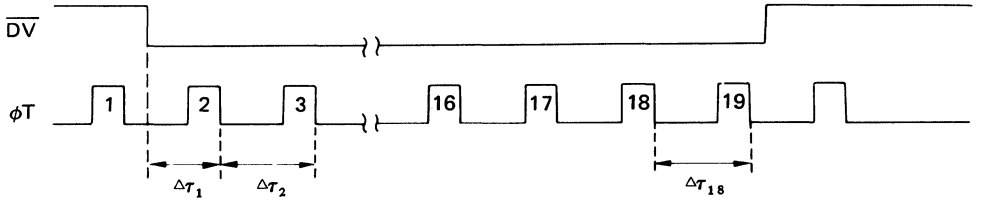
Parameter	Symbol	Conditions	Range Value			Unit
			Min.	Typ.	Max.	
Input Capacitance (excluding AE)	C_I	V_I=0 V			15	pF
Input Capacitance (AE pin)	C_I	V_I=0 V			35	pF
Output Capacitance	C_O	V_O=0 V			10	pF

FUNCTIONAL CHARACTERISTICS

Parameter	Range	Unit	Remarks
Font Format	18-row x 16-column dot matrix		
Output Mode	16 bit x 18 transfers		(Note 1)
Number of Characters Generated	3384	Word	
Character Accommodation Region	48~87 (JIS No.2 standard)	Partition	(Note 2)

Note 1. The relation between the 18-row x 16-column matrix and the data output pins is outlined below. The output is low (V_{OL}) for the character portion, and high (V_{OH}) for the background area.





Note 2. The address pins are related to the JIS C6226 no.1 and no.2 bytes in the following way.

JIS C 6226	No.2 byte							No.1 bytes						
	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_7	b_6	b_5	b_4	b_3	b_2	b_1
Address Pin	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

Preliminary

MSM53256RS

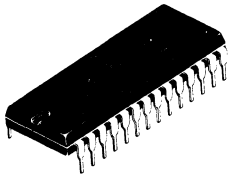
32,768 WORD x 8 BIT MASK ROM (E3-S-031-32)

GENERAL DESCRIPTION

MSM53256AS/RS is a silicon gate C-MOS device ROM with a 32,768 words x 8 bit capacity. It operates on a 5 V single power supply and all inputs and outputs can be directly connected to the TTL. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30μA (max) when the chip is not selected. The application of a byte system is most suitable for use as a large-capacity fixed memory for micro-computers and data terminals.
Since it provides $\overline{CE}$, CS and $\overline{OE}$ signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

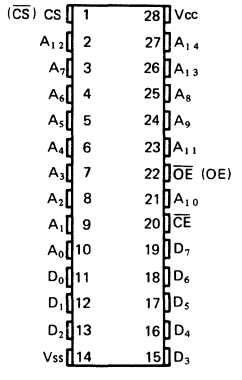
FEATURES

- 32,768 words x 8 bits
- 5V single power supply
- Access time: 200 ns MAX
- Input/output TTL compatible
- 3-state output
- Standby current 30 μA MAX
- 28-pin DIP



PIN CONFIGURATION

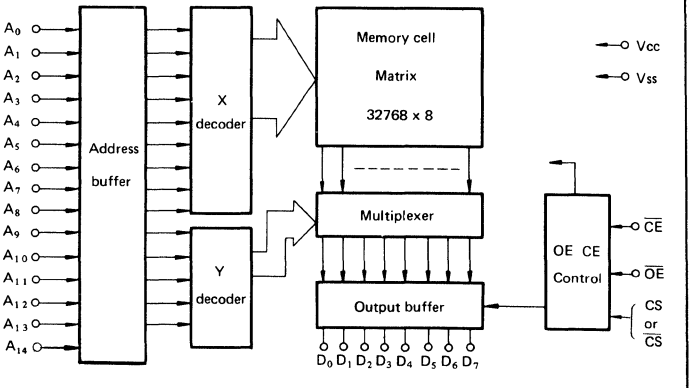
(Top View)



$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply voltage
$A_0 \sim A_{13}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable
CS	:	Chip select

Note: The $\overline{CS}$ active level and $\overline{OE}$ active level are specified by customer.

FUNCTIONAL BLOCK DIAGRAM



9

MOS EPROMS

MSM2708AS

8192-BIT UV ERASABLE ELECTRICALLY-PROGRAMMABLE READ-ONLY MEMORY (E3-S-019-32)

GENERAL DESCRIPTION

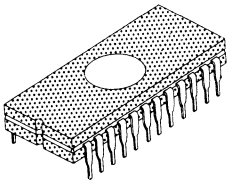
The Oki MSM2708 AS (Compatible to the Intel 2708) is a 8192-bit ultraviolet light erasable and electrically reprogrammable EPROM, ideally suited where fast turnaround and pattern experimentation are important requirements. All data inputs and outputs are TTL compatible during both the read and program modes. The outputs are three-state, allowing direct interface with common system bus structures.

The MSM2708 AS is fabricated with the N-channel silicon gate FAMOS technology and is available in a 24-pin dual in-line package.

FEATURES

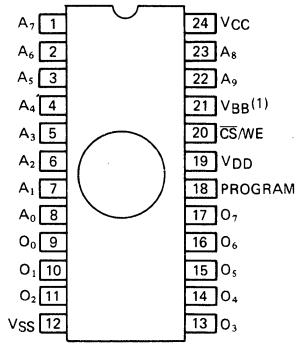
- Data Inputs and Outputs TTL Compatible during both Read and Program Modes
- Three-State Outputs — OR-Tie Capability
- Static — No Clocks Required

	Max. Power	Max. Access	Organization
MSM 2708 AS	800 mW	450 ns	1K x 8



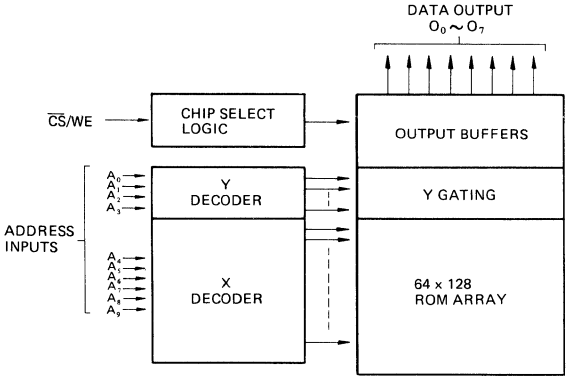
PIN CONFIGURATION

(Top View)



$A_0 \sim A_9$	Address Inputs
$O_1 \sim O_8$	Data Outputs/Inputs
$\overline{CS}$/WE	Chip Select/Write Enable Input

FUNCTIONAL BLOCK DIAGRAM



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PIN CONNECTION DURING READ OR PROGRAM

Mode	PIN Number							
	Data I/O 9 ~ 11, 13 ~ 17	Address Inputs 1 ~ 8, 22, 23	V_{SS} 12	Program 18	V_{DD} 19	$\overline{CS}$/WE 20	V_{BB} 21	V_{CC} 24
Read	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	−5	+5
Deselect	High Impedance	Don't Care	GND	GND	+12	V_{IH}	−5	+5
Program	D_{IN}	A_{IN}	GND	Pulsed 26V	+12	V_{IHW}	−5	+5

ABSOLUTE MAXIMUM RATINGS*

- Temperature Under Bias . . . . . −25°C to +85°C
- Storage Temperature . . . . . −65°C to +125°C
- V_{DD} with Respect to V_{BB} . . . . . +20V to −0.3V
- V_{CC} and V_{SS} with Respect to V_{BB} . . . . . +15V to −0.3V
- All Input or Output Voltages with Respect to V_{BB} during Read . . . . . +15V to −0.3V
- $\overline{CS}$/WE Input with Respect to V_{BB} during Programming . . . . . +20V to −0.3V
- Program Input with Respect to V_{BB} . . . . . +35V to −0.3V
- Power Dissipation 1.5W

*

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC AND AC OPERATING CONDITIONS DURING READ

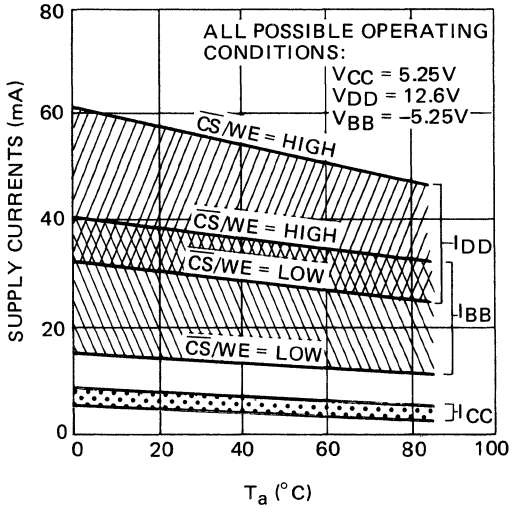
Temperature Range	0°C to 70°C
V_{CC} Power Supply	5V ± 5%
V_{DD} Power Supply	12V ± 5%
V_{BB} Power Supply	−5V ± 5%

READ OPERATION
DC AND OPERATING CHARACTERISTICS

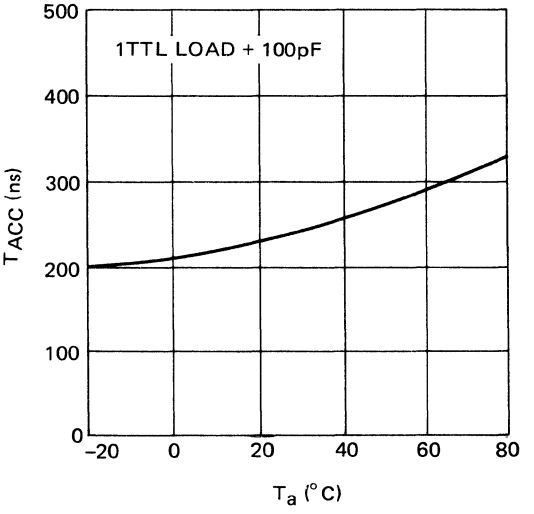
Parameter	Symbol	Min.	Typ.(2)	Max.	Units	Test Conditions
Address and Chip Select Input Leakage Current	I_{LI}		1	10	μA	V_{IN}=5.25V or V_{IN}=V_{IL}
Output Leakage Current	I_{LO}		1	10	μA	V_{OUT}=5.5V, $\overline{CS}$/WE=5V
V_{DD} Supply Current	I_{DD}(3)		50	65	mA	Worst Case Supply Currents All Inputs High: CS/WE=5V; T_a=0°C
V_{CC} Supply Current	I_{CC}(3)		6	10	mA	
V_{BB} Supply Current	I_{BB}(3)		30	45	mA	
Input Low Voltage	V_{IL}	V_{SS}		0.65	V	
Input High Voltage	V_{IH}	3.0		V_{CC}+1	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL}=1.6mA
Output High Voltage	V_{OH1}	3.7			V	I_{OH}=−100 A
Output High Voltage	V_{OH2}	2.4			V	I_{OH}=−1mA
Power Dissipation	P_D			800	mW	T_a=70°C

Note: 1. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.
2. Typical values are for T_a = 25°C and nominal supply voltages.
3. The total power dissipation is not calculated by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC} and I_{BB} currents should be used to determine power supply capacity only.

RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



ACCESS TIME VS. TEMPERATURE



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A.C. CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units
Address to Output Delay	t_{ACC}		350	450	ns
Chip Select to Output Delay	$t_{\overline{CO}}$		60	120	ns
Chip Deselect to Output Float	t_{DF}	0		120	ns
Address to Output Hold	t_{OH}	0			

CAPACITANCE(1)

($Ta = 25°C$, $f = 1$ MHz)

Parameter	Symbol	Typ.	Max.	Unit.	Conditions
Input Capacitance	C_{IN}	4	6	pF	$V_{IN} = 0V$
Output Capacitance	C_{OUT}	8	12	pF	$V_{OUT} = 0V$

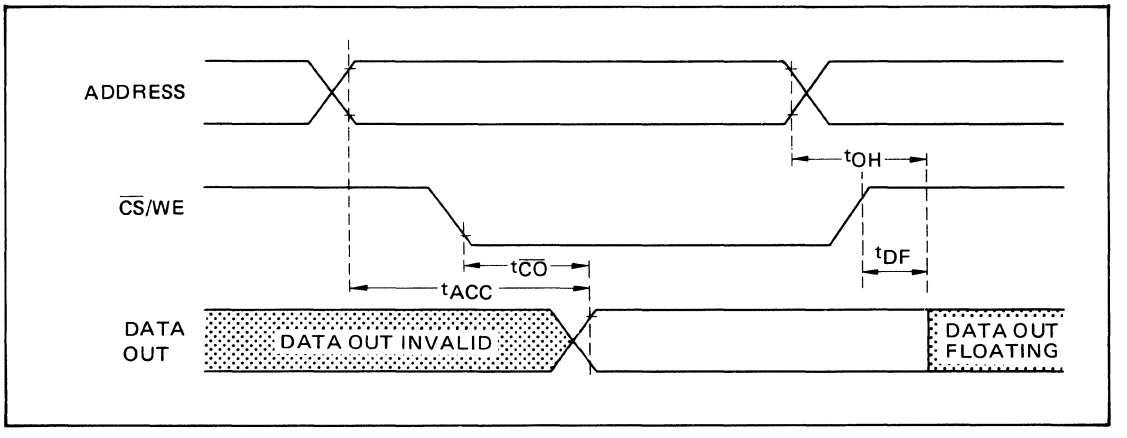
Note: 1. This parameter is periodically sampled and is not 100% tested.

AC TEST CONDITIONS:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: <20 ns

Timing Measurement
Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs.
Input Pulse Levels: 0.65V to 2.0V

WAVEFORMS



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ERASURE CHARACTERISTICS

The erasure characteristics of the MSM 2708 AS are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4,000 Angstrom (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3,000–4,000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical device in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the MSM 2708 AS is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Oki which should be placed over the MS 3578 AS window to prevent unitentional erasure.

The recommended erasure procedure for the MSM 2708 AS is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x Exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

OKI semiconductor

MSM2716AS

16384-BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

(E3-S-020-32)

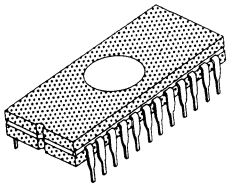
GENERAL DESCRIPTION

The MSM2716AS is a read only memory with the capacity of 2048 words x 8 bits whose contents can be erased by ultraviolet ray irradiation. Since the memory contents can be programmed as desired by the user and the alteration is easy, it is ideal for a processor program.

The MSM2716AS is processed as the N-channel silicon gate MOS with floating gates, and is encased in a standard 24-pin ceramic package.

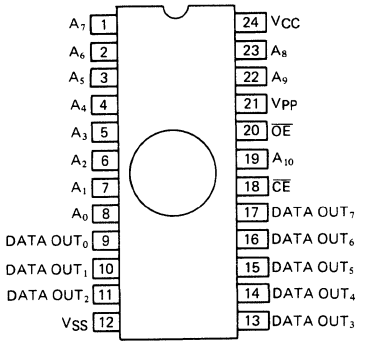
FEATURES

- Single power supply . . . . . +5V
- Low power Dissipation . . . . 525 mW in operation and 132 mW in standby state
- UV erasable and electrically programmable.
- Minimum programming time . . . . . 100 seconds for all 16,384 bits.
- Full decoding . . . . . 2048 words x 8 bits
- Static operation . . . . . No clock requirement
- TTL connection for inputs/outputs (tristate output)
- Easy expansion of memory capacity (wired-OR connection)
- Access time . . . . . 450 ns
- Pin compatible with INTEL's 2716

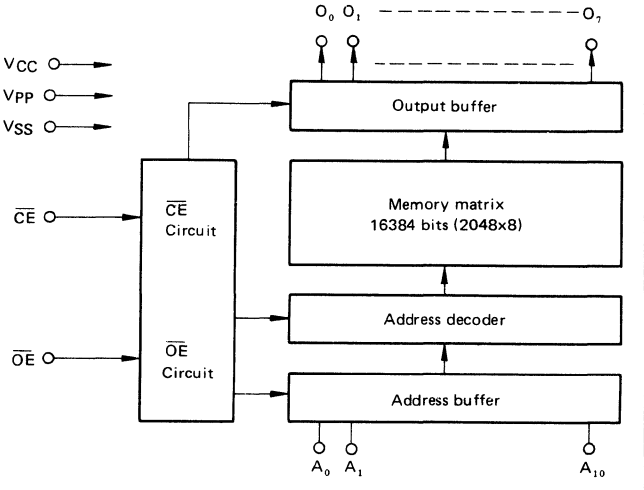


PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



The specifications are subject to change without notice.

9

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (18)	$\overline{OE}$ (20)	Vpp (21)	Vcc (24)	OUTPUTS (9~11, 13~17)
Read	V_{IL}	V_{IL}	+5V	+5V	D out
Stand by	V_{IH}	Don't care	+5V	+5V	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25V	+5V	D in
Program Verify	V_{IL}	V_{IL}	+25V	+5V	D out
Program Inhibit	V_{IL}	V_{IH}	+25V	+5V	High Z

High Z = High Impedance

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATING

Rating	Symbol	Conditions	Value	Unit
Storage Temperature	T_{stg}	–	−55 to +125	°C
Terminal Voltage			(to Vss)	
Address Input and Data Input			−0.3 to +6	
Program Input Vpp			−0.3 to +28	V
Vcc			−0.3 to +6	
Power Dissipation	P_D		525	mW

READ OPERATION

Operating range (for Vss = 0V)

Parameter	Symbol	Conditions	Guaranteed Range	Unit
Source Supply Voltage	Vcc		+5 to ±0.25	V
	Vpp		Vcc ± 0.6	V
Operating Temperature	Topr		0 to +70	°C
Number of Leads	N	TTL gate load	1	–

9

DC OPERATING CHARACTERISTICS

(Vcc = 5V ± 5%, Vpp = Vcc ± 0.6V, Ta = 0°C to +70°C unless specified otherwise)

Parameter	Symbol	Conditions	Guaranteed Range			Unit
			Min.	Typ.	Max.	
Input Leak Current	I_{LI}	V_{IN} = 5.25V			10	μA
Output Leak Current	I_{LO}	V_{OUT} = 5.25V			10	μA
Program Pin Current	Ipp	Vpp = 5.85V			5	mA
Collector Supply Current (Standby)	I_{CC1}	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}		10	25	mA
Collector Supply Current (Active)	I_{CC2}	$\overline{OE}$ = $\overline{CE}$ = V_{IL}		60	100	mA
"H" Input Voltage	V_{IH}		2.2		V_{CC+1}	V
"L" Input Voltage	V_{IL}		-0.1		0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = -400 μA	2.4			V
"L" Output Voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V

Note: V_{CC} must be supplied before or when Vpp is supplied, and must be cut off when or after Vpp is cut off.

AC OPERATING CHARACTERISTICS

(Vcc = 5V ± 5%, Vpp = Vcc ±0.6V, Ta = 0°C to +70°C unless specified otherwise)

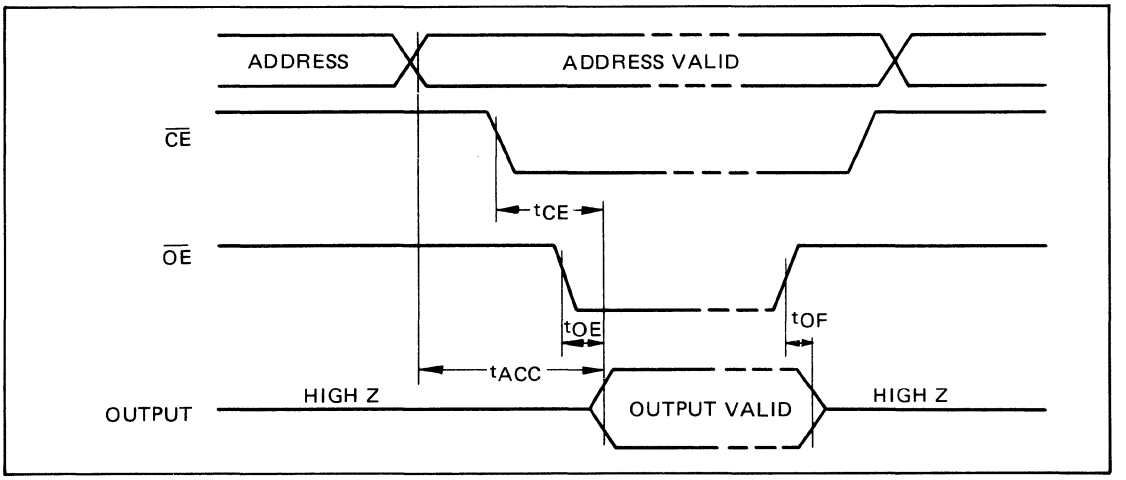
Parameter	Symbol	Conditions	Guaranteed range			Unit
			Min.	Typ.	Max.	
Address Output Delay Time	t_{ACC}	$\overline{OE}$ = CE = V_{IL}		250	450	ns
$\overline{CE}$ Output Delay Time	t_{CE}	$\overline{OE}$ = V_{IL}		280	450	ns
$\overline{OE}$ Output Delay Time	t_{OE}	$\overline{CE}$ = V_{IL}			120	ns
Output Disable Delay Time	t_{DF}	$\overline{CE}$ = V_{IL}	0		100	ns

*AC characteristics measuring conditions

Input pulse level . . . . . 0.8 ~ 2.2V
Input rise/fall time . . . . . Within 20 ns
Output load . . . . . 1TTL Gate + 100 pF
Timing measurement reference levels . . . . Input 1V and 2V, Output 0.8V and 2.4V

TIME CHART

Read Mode



PROGRAMMING OPERATION

(Vcc = 5V ± 5%, Vpp = 25V ± 1V, Ta = 25°C ± 5°C unless specified otherwise)

Parameter	Symbol	Conditions	Guaranteed Range			Unit
			Min.	Typ.	Max.	
Input Leak Current	I_{LI}	V_{IN} = 5.25V/0.45V			10	μA
Program Pin Current	I_{PP1}	$\overline{CE}$ = V_{IL}			6	mA
Programming Current	I_{PP2}	$\overline{CE}$ = V_{IH}			30	mA
Collector Supply Current	I_{CC}				100	mA
"H" Input Voltage	V_{IH}		2.2		V_{CC+1}	V
"L" Input Voltage	V_{IL}		−0.1		0.8	V

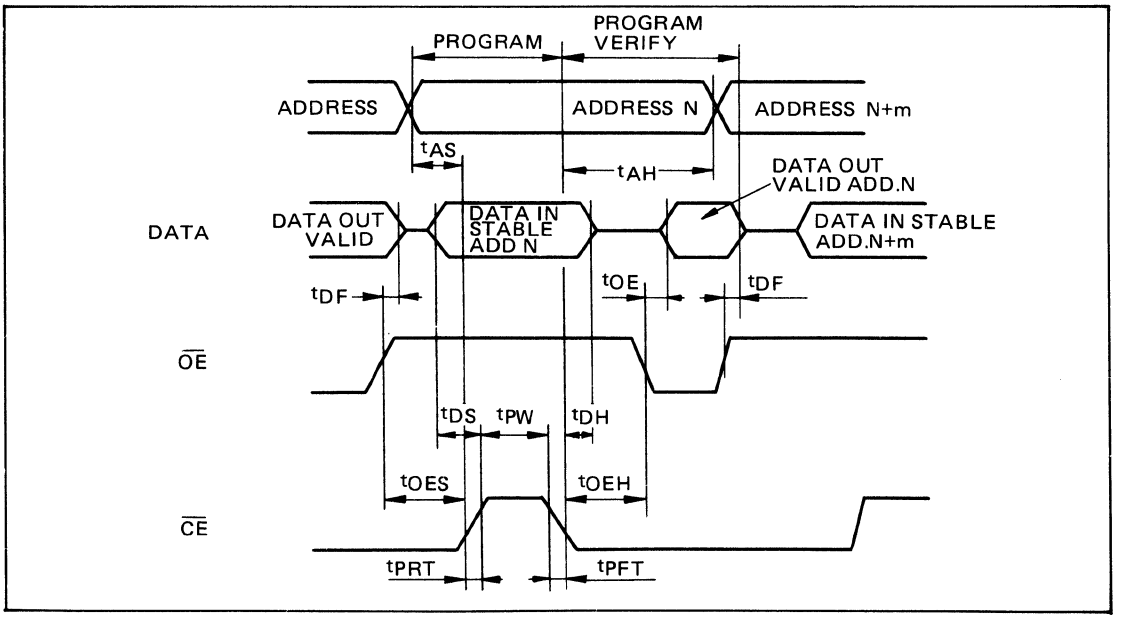
AC CHARACTERISTICS

(Vcc = 5V ± 5%, Vpp = 25V ± 1V, Ta = 25°C ± 5°C unless specified otherwise)

Parameter	Symbol	Guaranteed Range			Unit
		Min.	Typ.	Max.	
Address Setup Time	t_{AS}	2			μS
OE Setup Time	t_{OES}	2			μS
Data Setup Time	t_{DS}	2			μS
Address Hold Time	t_{AH}	2			μS
OE Hold Time	t_{OEH}	2			μS
Data Hold Time	t_{DH}	2			μS
Output Disable Delay Time	t_{DF}	0		120	ns
Output Enable Delay Time	t_{OE}			120	ns
Program Pulse Width	t_{PW}	45	50	55	ms
Program Pulse Fall Time	t_{PRT}	5			ns
Program Pulse Rise Time	t_{PFT}	5			ns

* AC characteristics measurement conditions are the same as those for read operation.

TIME CHART (PROGRAM MODE)



OPERATION

• Read mode

When $\overline{OE}$ is set to "L" level, reading of the memory contents starts 450 ns (T_{ACC}) after the address or 120 ns (t_{OE}) after $\overline{OE}$ if the address is already fixed.

• Output deselection

Multiple MSM2716AS chips may be combined by wired-OR connection. The data in one MSM2716AS is read when $\overline{OE}$ is at "L" level. Other MSM2716AS chips are set to the output deselection state by setting the $\overline{OE}$ to the "H" level.

• Standby mode

Setting $\overline{CE}$ to "H" level causes the power to be decreased to 1/4 of that in the read mode (525 mW → 132 mW).

• Programming

All bits of the MSM2716AS are set to "H" level at the time of delivery or after erasure. When 0 is written, the corresponding bit goes to "L" level. In the programming mode, $\overline{OE}$ input at Vpp=25V is used as "H" level.

The programming data must be supplied in parallel to output pins ($0_0 \sim 0_7$). The address and input are both TTL level. Supplying $\overline{CE}$ input (TTL "H" level) at 50 ms intervals after setting up the address and data enables programming. Avoid programming by supplying a DC signal to $\overline{CE}$ pin.

• Program verify

The MSM2716AS can be verified in the programming mode. Vpp for this operation is 25V.

• Program inhibit

Multiple MSM2716AS chips can be programmed in parallel and with different data in this mode. All pins other than $\overline{CE}$ can be used in common for all chips.

Supply TTL "H" level to $\overline{CE}$ pins of the chips to be programmed and TTL "L", level to $\overline{CE}$ pins of the chips not to be programmed.

HANDLING OF MSM2716AS

Since the MSM2716AS is an ERROM of N-channel silicon gate FAMOS type, pay special attention as follows in addition to general handling caution of MOS ICs so as to maintain high reliability.

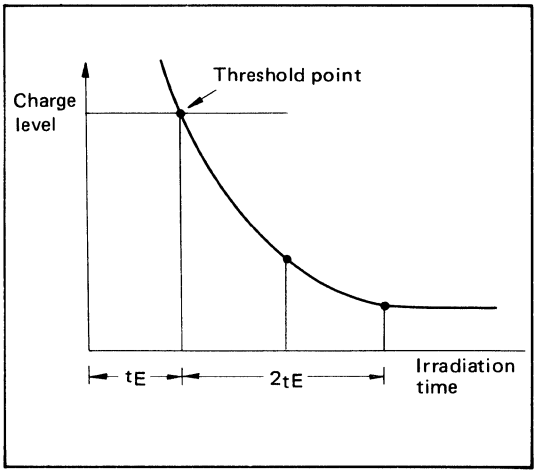
• Attention during writing

Since all bits of the MSM2716AS are erased before delivery, writing can be started as it is. Sufficient erasure is necessary before reprogramming.

For writing operation, avoid a location with strong light intensity. 100—200 lux is allowable.

• Attention during erasure

The contents of the MSM2716AS can be erased by irradiation of ultraviolet rays. The charge (electrons) in the floating gates decreases with the time lapse, but erasing time t_E till the threshold point (where all bits are judged as 1 by a writer) is insufficient. Irradiate for another 2 t_E for sufficient discharge of electrons.



The irradiation energy for erasure of the MSM2716AS contents is 15W·sec/cm^2.

• Caution for handling

(1) Keep away from carpet or cloth that generates static electricity.
(2) Perfectly ground the using writer and the system in which the MSM2716AS is used.
(3) If a soldering iron is used, be sure to ground it.
(4) Always carry in electrically conductive plastic mat.
(5) The programmed ROM must be encased in electrically conductive plastic mat.
(6) Do not touch the glass seal portion with a hand to prevent insufficient erasure caused by decreased UV ray transmission.

• Caution for system debugging

Check the functioning status by fluctuating the voltage by ±5%.

MSM2764AS

8192 x 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

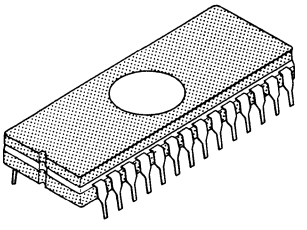
(E3-S-021-32)

GENERAL DESCRIPTION

The MSM2764AS is a 8192W x 8 bit ultraviolet erassable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM2764AS is ideal for microprocessor programs, etc.
The MSM2764AS is manufactured by the N channel double silicon gate MOS technology and is contained in the 28-pin CERDIP package.

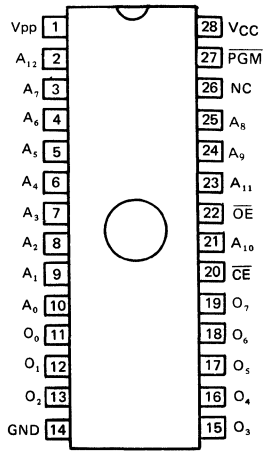
FEATURES

- +5V single power supply
- 8192 words x 8 bits configuration
- 50ms single pulse programming
- Access time:
  MAX 200 ns (MSM2764-20AS)
  MAX 250 ns (MSM2764-25AS)
  MAX 300 ns (MSM2764-30AS)
- Power consumption:
  MAX 788 mw (during operation)
  MAX 184 mw (during stand-by)
- Perfect static operation
- INPUT/OUTPUT TTL level (tristate output)
- Pin compatible to the INTEL 2764.

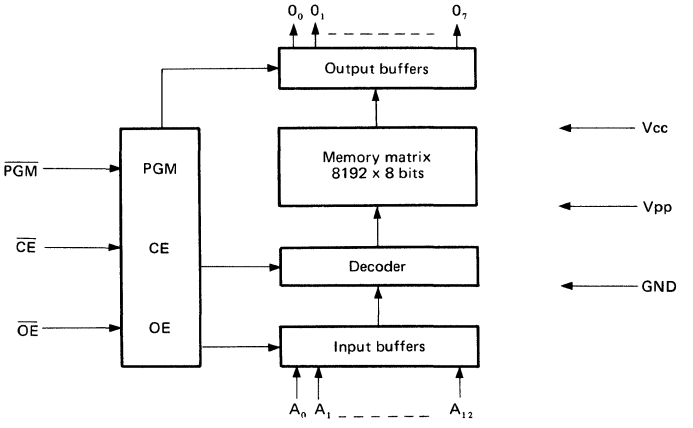


PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

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FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	Vcc (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+ 5V	+5V	Dout
Stand-by	V_{IH}	–	–	+ 5V	+5V	High impedance
Program	V_{IL}	–	V_{IL}	+21V	+5V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+21V	+5V	Dout
Program Inhibit	V_{IH}	–	–	+21V	+5V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATING

Temperature Under Bias	Ta	–10°C~80°C
Storage Temperature	Tstg	–55°C~125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	–0.6V~7V
Program Voltage	Vpp	–0.6V~23V
Power Assembly Voltage	P_D	1.5W

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

• Recommended operation condition

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min	Typ	Max			
Vcc Power Supply Voltage	Vcc	4.75	5.0	5.25	0°C~70°C	Vcc=5V±5% Vpp=Vcc±0.6V	V
Vpp Voltage	Vpp	4.15	5.0	5.85			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	–0.1	–	0.8			V

The voltage with respect to GND

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DC CHARACTERISTICS

(Vcc = 5V±5%, Vpp = Vcc±0.6V, Ta = 0°C~70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Stp.	Max.	
Input Leak Current	I_{LI}	V_{IN} = 5.25V	—	—	10	μA
Output Leak Current	I_{LO}	V_{OUT} = 5.25V	—	—	10	μA
Vcc Power Current (Stand-by)	Icc_1	$\overline{CE}$ = V_{IH}	—	—	35	mA
Vcc Power Current (Operation)	Icc_2	$\overline{CE}$ = V_{IL}	—	—	150	mA
Program Power Current	Ipp_1	Vpp = Vcc±0.6V	—	—	15	mA
Input Voltage "H" Level	V_{IH}	—	2.0	—	Vcc+1	V
Input Voltage "L" Level	V_{IL}	—	-0.1	—	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = 400μA	2.4	—	—	V
Output Voltage "L" level	V_{OL}	I_{OL} = 2.1mA	—	—	0.45	V

AC CHARACTERISTICS

(Vcc = 5V±5%, Vpp = Vcc±0.6V, Ta = 0°C~70°C)

Parameter	Symbol	Conditions	2764-20		2764-25		2764-30		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	—	200	—	250	—	300	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	—	200	—	250	—	300	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	10	70	10	100	10	150	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	60	0	90	0	130	ns

Measurement condition

- Input pulse level . . . . . 0.8V~2.2V
- Input rise/fall time . . . . . under 20 ns
- Output load . . . . . 1TTL GATE + 100pF
- Output timing reference level . . . . . Input 1V, 2V/Output 0.8V, 2V

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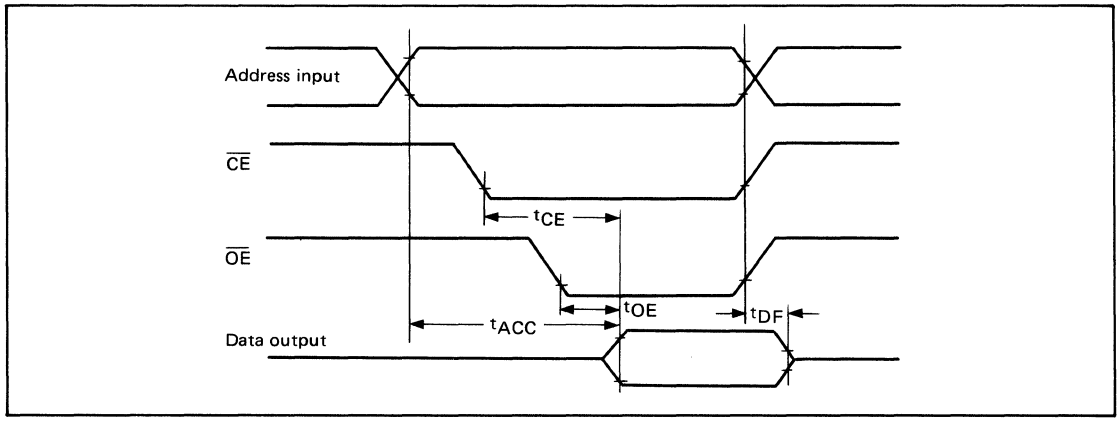
TIME CHART



<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(Vcc = 5V±5%, Vpp = 21V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	
Input Leak Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP}	$\overline{CE}$ = $\overline{PGM}$ = V_{IL}	–	–	30	mA
Vcc Power Current	I_{CC}	—	–	–	150	mA
Input Voltage "H" Level	V_{IH}	—	2.0	–	Vcc+1	V
Input Voltage "L" Level	V_{IL}	—	-0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	—	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	—	–	–	0.45	V

AC CHARACTERISTICS

(Vcc = 5V±5%, Vpp = 21V±0.5V, Ta=25°C~5°C)

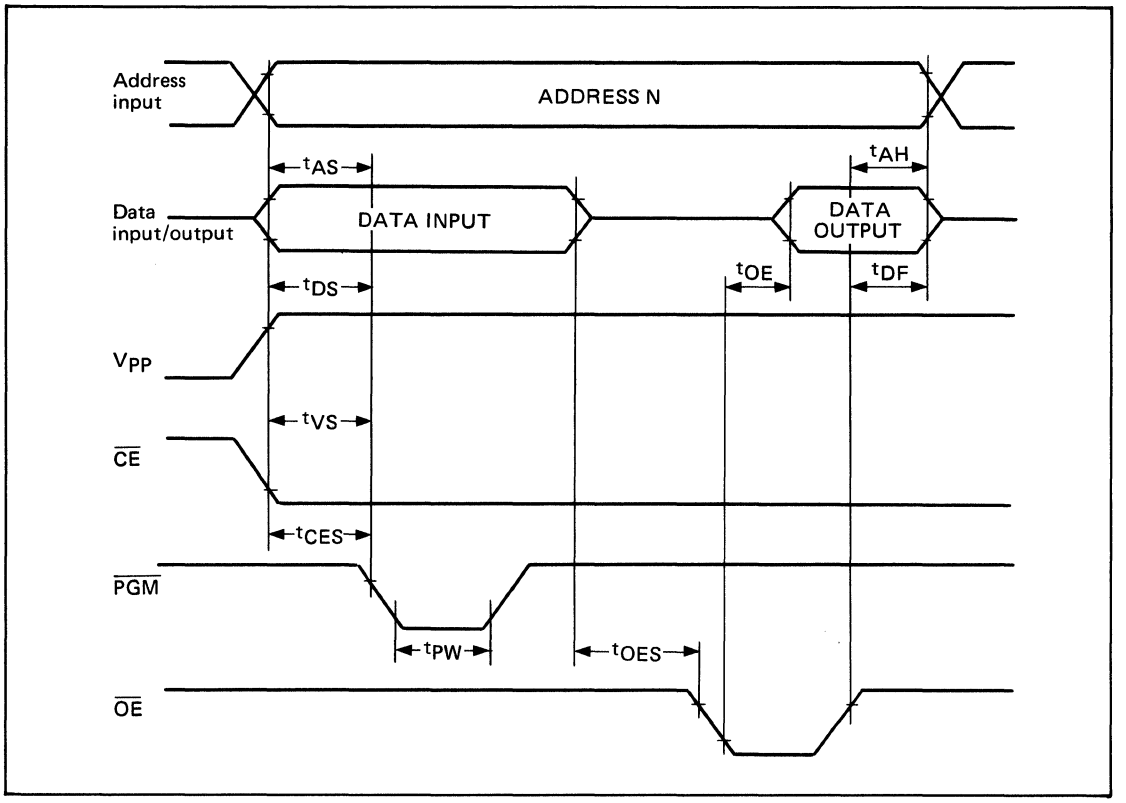
Parameter	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	
Address Set-up Time	t_{AS}	—	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	—	2	–	–	μs
Data Set-up Time	t_{DS}	—	2	–	–	μs
Address Hold Time	t_{AH}	—	0	–	–	μs
Data Hold Time	t_{DH}	—	2	–	–	μs
$\overline{OE}$ Output Valid Delay Time	t_{DF}	—	0	–	130	ns
V_{pp} Power Set-up Time	t_{VS}	—	2	–	–	μs
Program Pulse Width	t_{PW}	—	45	50	55	ms
$\overline{CE}$ Set-up Time	t_{CES}	—	2	–	–	μs
$\overline{OE}$ Output Valid Delay Time	t_{OE}	—	–	–	150	ns

Measurement condition

Input pulse level . . . . . 0.8V~2.2V
Input rise/fall time . . . . . Under 20 ns
Output timing reference level . . . . . Input 1V, 2V/output 0.8V, 2V

9

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

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Preliminary

MSM27128AS

131,072-BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

(E3-S-022-32)

INTRODUCTION

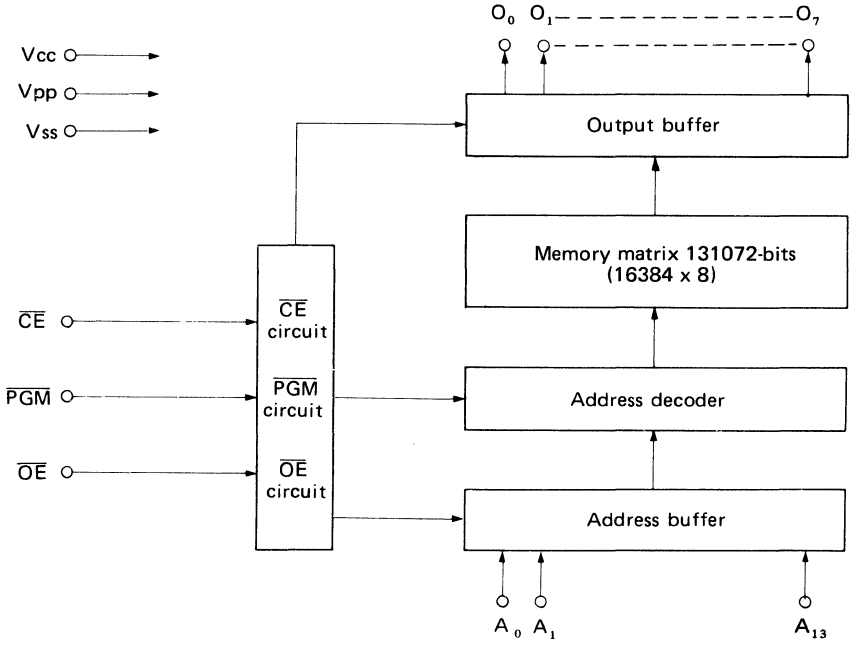
MSM27128AS is a 16384 word x 8-bit read-only memory capable of being erased by ultra violet light. The user may thus generate the desired memory contents, and subsequently alter the contents very simply, making this device ideal for processor programming etc.

MSM27128AS has been manufactured by N-channel silicon gate MOS techniques with a floating gate, and sealed in a standard 28-pin cerdip package.

FEATURES

- Single power supply . . . . . +5V
- Power consumption . . . . . 788 mW during operation, 184 mW during standby mode
- Ultra violet light erasable, and electrically rewritable
- Reduced programming time. 150 seconds for all 131,072 bits
- Full decoding . . . . . 16384 words x 8 bits
- Static operation . . . . . Clock unnecessary
- Input/output TTL connection possible (tristate output)
- Simple expansion of memory capacity (wired OR connections)
- Access time . . . . . 250 ns
- Pin-compatible with Intel 27128

FUNCTIONAL BLOCK DIAGRAM



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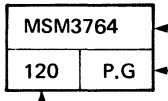
CROSS REFERENCE LIST

(Note)



- Type No.
- Package Material
- Access Time (ns) max.

P: PLASTIC
G: CERDIP
C: SIDE-BRAZED

1. DYNAMIC RAM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
						2117-5			MCM4116-30	μPD416			
						300 P.G			300 G.C	300 P.G			
					HM4716A-4	2117-4	TMS4116-25	MK4116-4	MCM4116-25	μPD416-1	TMM416-4	M5K4116-4	MB8116N
					250 P.G	250 P.G	250 P.G.C	250 P.G	250 G.C	250 P.G	250 G	250 P.G	250 C
				MSM3716-3	HM4716A-3	2117-3	TMS4116-20	MK4116-3	MCM4116-20	μPD416-2	TMM416-3	M5K4116-3	MB8116E
				200 C	200 P.G	200 P.G	200 P.G.C	200 P.G	200 G.C	200 P.G	200 G	200 P.G	200 C
	16k	16384 x 1	16	MSM3716-2	HM4716A-2	2117-2	TMS4116-15	MK4116-2	MCM4116-15	μPD416-3	TMM416-2	M5K4116-2	MB8116H
				150 C	150 P.G	150 P.G	150 P.G.C	150 P.G	150 G.C	150 P.G	150 G	150 P.G	150 C
					HM4716A-1								MB8216E
					120 P.G								120 C
					HM4816								
					100 C								
	64k	65536 x 1	16	MSM3764-15	HM4864-2	2164-15	TMS4164-15	MK4164-15	MCM6664-15	μPD4164-3	TMM4164C-3	M5K4164-15	MB8264-15
				150 C	150 C	150 C	150 C	150 C	150 C	150 C	150 C	150 C	150 C
				MSM3764-20	HM4864-3			MK4164-20	MCM6664-20	μPD4164-2	TMM4164C-4	M5K4164-20	MB8264-20
				200 C	200 C			200 C	200 C	200 C	150 C	200 C	200 C

Struc-ture	Total Bit	Or-gani-zation	Num-ber of Pin	Oki		Hitachi		Intel	Texas		Mostek	Motorola		NEC		Toshiba		Mitsubishi		Fujitsu	
																		M5K4164A-10		MB8264A-10	
																		100	P.C	100	P.G
				MSM3764A-12		HM4864A-1			TMS4164A-12			MSM6664A-12		μPD4164A-4		TMM4164A-2		M5K4164A-12		MB8264A-12	
				120	P.C	120	P.G		120	P.C		120	C	120	P.G.C	120	P	120	P.C	120	P.G
	64k	65536 x 1	16	MSM3764A-15		HM4864A-2			TMS4164A-15			MCM6664A-15		μPD4164A-3		TMM4164A-3					
				150	P.C	150	P.G		150	P.C		150	C	150	P.G.C	150	P				
				MSM3764A-29		HM4864A-3			TMS4164A-20			MCM6664A-20		μPD4164A-2							
				200	P.C	200	P.G		200	P.C		200	C	200	P.G.C						

2. STATIC RAM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	4k	1024 x 4	18		HM472114A-1		TMS4045-15			μPD2114L-5			MB8114H
					150 P.G		150 P.G.C			150 P.G			150 P.C
				MSM2114L-2	HM472114A-2	2114/L-2	TMS40/L45-20	MK4114-3	MCM21/L14-20	μPD2114L-3	TMM314A/L1	M5L2114L-2	MB8114EL
				200 P	200 P	200 P.G	200 P.G.C	200 P.C	200 P.C	200 P.G	200 P	200 P.G	200 P.C
							TMS40/L45-25	MK4114-4	MCM21/L14-25	μPD2114L-2			
							250 P.G.C	250 P.C	250 P.C	250 P.G			
				MSM2114L-3	HM472114-3	2114/L-3		MK4114-5	MCM21/L14-30	μPD2114L-1		M5L2114L-3	MB8114NL
				300 P	300 P.G	300 P.G		300 P.C	300 P.C	300 P.G		300 P.G	300 P.C
				MSM2114L	HM472114-4	2114/L	TMS40/L45-45		MCM21/L14-30	μPD2114	TMM314A/L	M5L2114L	
				450 P	450 P.G	450 P.G	450 P.G.C		450 P.C	450 P.G	450 P	450 P.G	
	16k	2048 x 8	24								TMM2016P-1		MB8168
											100 P		100
				MSM2128-12									
				120 P									

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
				MSM2128-15							TMM2016P	58725-15	MB8168
				150 P							150 P	150 P.C	150
				MSM2128-20								58725	
				200 P								200 P.C	
COMS	4K	4096 x 1	18	MSM5104-2									
				200 P									
													MB8404E
													250 P
				MSM5104-3									
				300 P									
					HM4315				MCM146504		TC5504		
					450 P				450 P.C		450 P		
											TC5504-1		
											550 P		
											TC5504-2		
											800 P		
		1024 x 4	18	MSM5115-2									
				200 P									
													MB8414E
													250 P
				MSM5115-3									
				300 P									

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
CMOS	4k	1024 x 4	18								TC5047-1 550 P		
											TC5047-2 800 P		
	4k	1024 x 4	18	MSM5114-2 200 P						μPD444-3 200 P			
										μPD444-2 250 P			
				MSM5114-3 300 P	HM4334-3 300 P					μPD444-1 300 P			
				MSM5114 450 P	HM4334-4 450 P					μPD444 450 P	TC5514 450 P	M58981-45 450 G	
											TC5514-1 650 P		
											TC5514-2 800 P		
	16k	2048 x 8	24	MSM5128-12 120 P	HM6116/L-2 120 P								
				MSM5128-15 150 P	HM6116/L-3 150 P					μPD446-3 150 P			
				MSM5128-20 200 P	HM6116/L-4 200 P					μPD446-2 200 P	TC5517-2 200 P		
										μPD446-1 250 P	TC5517 250 P		

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
CMOS	16k	2048 x 8	24	MSM5127-15 150 P						μPD447-3 150 P			
				MSM5127-20 200 P						μPD447-2 200 P	TC5516-2 200 P		
										μPD447-1 250 P	TC5516 250 P		
										μPD447 450 P			
				MSM5129-15 150 P	HM6117/L-3 150 P					μPD449-3 150 P		M5M5118-15 150 P	
				MSM5129-20 200 P	HM6117/L-4 200 P					μPD449-2 200 P		MSM5118 200 P	
										μPD449-1 250 P			
										μPD449 450 P			
				MSM5126-20 200 P	HM6116/L-4 200 P					μPD446-2 200 P	TC5517-2 200 P		
				MSM5126-25 250 P						μPD446-1 250 P	TC5517 250 P		
										μPD446 450 P			

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3. MASK ROM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	16k	2048 x 8	24	MSM2916	HN462316E	2316E		MK34000-3	MCM68A 316A		TMM334		MB8316
				250 P	450 P	450 P.G		350 P.C	350 P.C		450 P		450 P
								MK31000-3	MCM68A 316A	μPD2316	TMM331A	M58731	
								550 P.C	350 P.C	450 P.G	450 P	650 P.G	
	32k	4096 x 8	24	MSM2932		2332A				μPD2332	TMM333	M58333	MB8332
				300 P		450 P.G				450 P.G	450 P	650 P	200 P
					HN46332		TMS4732	MK32000-5	MCM68A 332				
					350 P		450 P.G	300 P.G	350 P.C				
	64k	8192 x 8	24	MSM2965				MK36000-5	MCM68A 364				
				300 P				300 P.G	250 P.C				
					HN48364				MCM68A 364			M58334	
					350 P				350 P.C			650 P	
			28	MSM3864		2364A				μPD2364	TMM2364		
				250 .P		450 P.G				450 P.G	250 P		
	128k		28	MSM38128						μPD23128			
				450 P.C						250 C			
				MSM38128A									
				250 P									

4. EPROM

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Mostek	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	16k	2048 x 8	24			2716-1		MK2716-6	MCM27A				
						350 C		350 C	350 C				
						2716-2		MK2716-7					
						390 C		400 C					
				MSM2716 cerdip	HN462716	2716		MK2716-8	MCM2716	μPD2716	TMM323	M5L2716	MB8516
				450 C	450 C	450 C		450 C	450 C	450 C	450 C	450 C	450 C
												M5L2716-65	
												650 C	
							TMS2516						
							450 G.C						
	64k	8192 x 8	28	MSM2764-20AS 200ns CERDIP	—	2764-2	—	—	—	—	TMM2764D-2	M5L2764K-2	MBM2764-20
											200 C	200 C	200 C
				MSM2764-25AS 250ns CERDIP	HN482764 250ns C	2764	—	—	—	μPD2764	TMM2764D	M5L2764K	MBM2764-25
											250 C	250 C	250 C
				MSM2764-30AS 300ns GERDIP	HN482764-3 300n C	2764-3						M5L2764K-3	MBM2764-30
												300 C	300 C

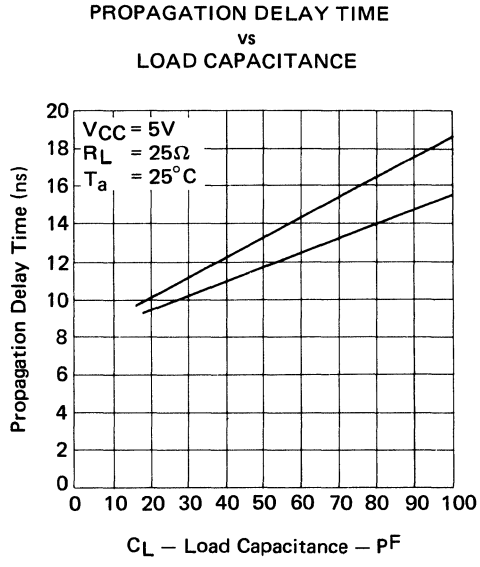
APPLICATIONS

64K BIT DYNAMIC RAM APPLICATION NOTES

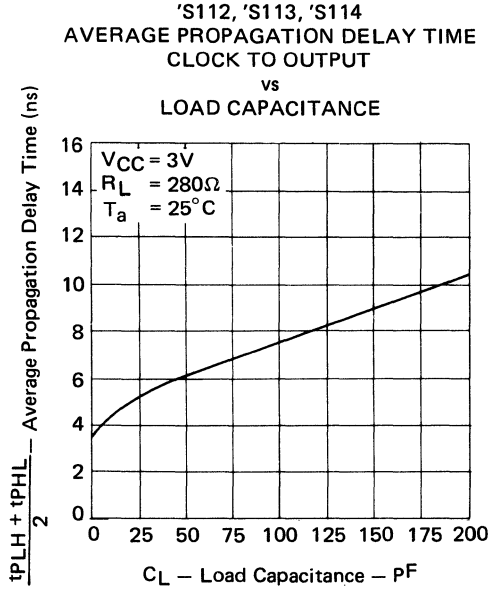
1. MEMORY DRIVER

There are problems in driving MOS ICs by a TTL driver: increase of driver delay time due to capacitive load and ringing waveform at the falling edge.
An example of the increase of delay time due to capacitive load is shown in the following figure.
The number of load memory elements must be taken into consideration when designing the timing.

In case of LS type



In case of L type



- If the number of load memory elements is 20 ~ 40 (150 ~ 300pF) on a two layer board, an undershoot of −2 to −3V (peak voltage) occurs. Therefore, measures against ringing must be taken as described in the following.

- Measures against ringing
  (1) No consideration is required for the rising edge since there is a margin.
  (2) Since a ringing may be considered as a reflection due to mismatching between the driver output impedance and signal line impedance, it can be prevented by taking the line matching (termination).
  For memory arrays, however, termination with pull up or bleeder resistance is not effective. Instead, series resistance (damping resistance) is suitable for memory arrays.
  (3) The optimul value of series resistance differs depending upon the speed, pattern status, and driver. Experiences will help much in determining the optimul series resistance.
  As a standard, a resistance of 10 ~ 100Ω is suitable.
  Note that the speed will be lowered if the resistance is so great. An example is shown in attached drawing 3.
  (4) Make the signal lines as short as possible. Multilayer board design is effective in reducing the undershoot (as the signal line impedance is lowered).

2. DECOUPLING CAPACITORS

The dynamic MOS RAM is featured by the great power current at the active time in comparison to that at the standby time.
For example, the rated value (Icc1) of the mean power current of the MSM3764 is 45mA, while the standby current (Icc2) of the MSM3764-15 (150ns version) is 5mA. The former is approximately 10 times greater than the latter. The peak current of the MSM3764 approaches 90mA in the worst case. It is approximately 20 times as great as the standby current Icc2.
Therefore, the power circuit must be designed so as to prevent the above current variation from causing an erroneous operation of the memory. A by-pass capacitor must be inserted for this purpose. There are two types of by-pass capacitors: high frequency capacitor and low frequency capacitor.

2.1 High Frequency Capacitor

In the Icc current waveform, the peak current rises at a high speed such as 10ns, and a high frequency noise represented by the following expression is caused to occur by the L component of the current applied to the capacitor:

$$\triangle V = L\frac{\triangle i}{\triangle t}$$

To reduce the fluctuation $\triangle V$, the value of L must be reduced.
For this purpose, the capacitor must be placed as close as possible to the power pin of the IC. Further, sufficient capacity for supplying the peak current is required. The standard capacity for a double sided circuit board (two layer circuit board) is $0.05 \sim 0.1\mu F$ or more. The capacity may be less than this value for a multi layer circuit board since the L component is less than the former.
When designing a board, mount one capacitor with excellent high frequency characteristics for every two or three MOS IC memory chips, near the power pins of these IC chips.

2.2 Low Frequency Capacitor

A low frequency capacitor is required for suppressing the power fluctuation due to a sudden current variation (for example, current variation caused by a status change from the standby status to the continuous access status or concurrent refreshment of the entire board) in a board unit. The power fluctuation in this case is a slow variation of several handred ns.
For this reason, the low frequency capacitor must have a capacity larger than the high frequency capacitor.
Though the capacity requirement depends upon the number of memories which operate simultaneously (bit width), $50\mu F$ is enough for a 16 ~ 32 bit system in a practical use.
As an example of capacitor which satisfies the requirements in both 2.1 and 2.2 above, a small-sized tantalum capacitor with excellent high frequency characteristics is shown in the following table. It is desirable to mount a low frequency capacitor near the power input pin in order to suppress the fluctuation of power supplied from outside, even if this capacitor is mounted.

Manufacturer	Model	Capacity (μF)
Oki Ceramic Co.	Model CA tantalum capacitor Model CB	0.1 ~ 20μF

The frequency characteristics of the above capacitor and the power bus bar are illustrated in attached figure 1.

3. PRINTED CIRCUIT BOARD

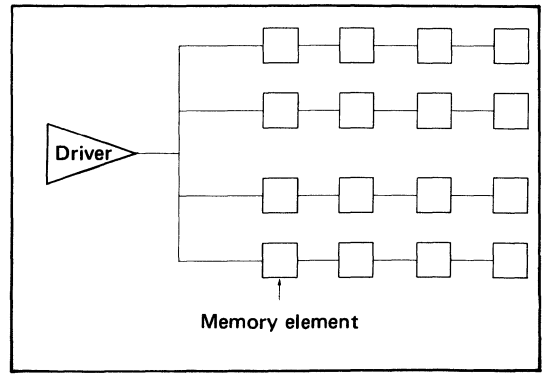
3.1 Number of Layers

Considering the measures against power noise which was described in 2. above and the routing to be described in 3.2, two layers are enough in principle.

3.2 Routing

An example of routing on a two-layer circuit board is shown in attached drawing 2. In designing the routing, note the following four points:

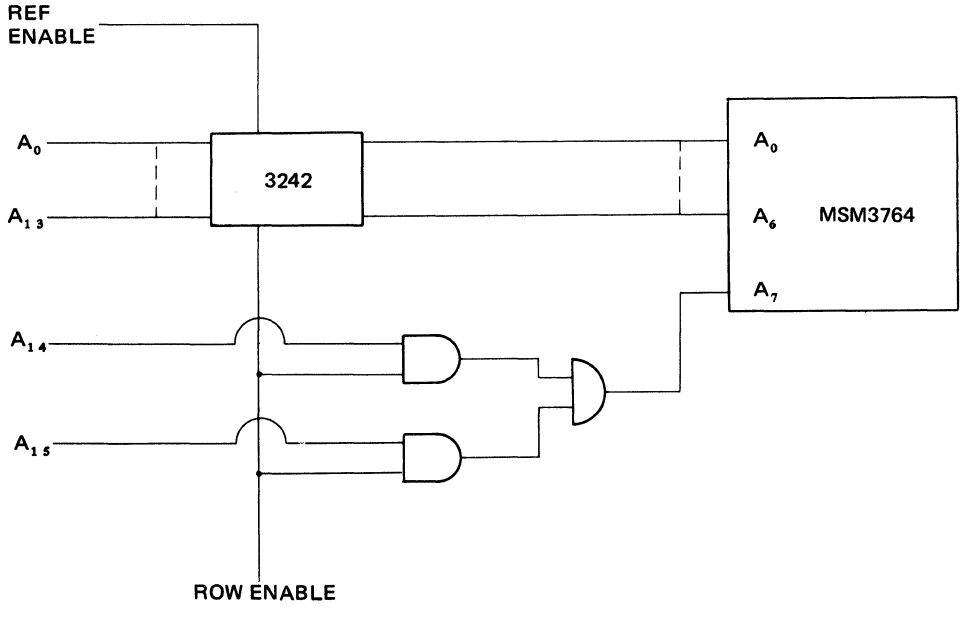
(I) The MOS drive line based on the TTL must be as short as possible to prevent ringing (reflection) and reduce crosstalk.
(II) Considerations are required to lower the impedance of the power line (including the ground). (For example, make a solid or grid-formed power line pattern. It is desirable that the power line pattern has width of at least 1.27mm.)
(III) If a signal line is to be branched for multi drive, the line must be branched at the driving end. (See the following figure.) And, the memory matrix must be designed in an integrated form, and peripheral drivers must be placed near the memory matrix.



4. PERIPHERAL CONTROL CIRCUIT

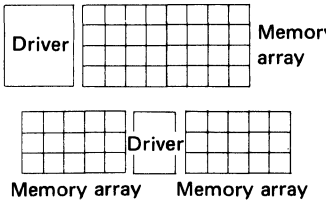
The three types of dynamic RAM control ICs shown in the following table are available at present.

Manufacturer	Model	Functions
Intel	i-3242	○ Seven-bit address multiplexer (for 16K bit dynamic RAM) ○ Seven-bit refresh address count function ○ Direct dirving capability of memory elements (for approx. 20 elements. 250 pF/25 ns 15 pF/9 ns) ○ Application to a 64K bit dynamic RAM, example (see the following figure)
Motorola	MC-3242	
Texas Instruments (T. I)	74LS601 603	○ Refresh timer using an RC multivibrator ○ Timing generation ○ Refresh address (7-bit address)
Advanced Micro Device (AMD)	Am2964A	○ Address latch/multiplex function (16-bit address) ○ Refresh address counter ○ $\overline{RAS}$ decoder (2 ~ 4)
Intel	i-8203	○ 8-bit address multiplexer (for 16K/64K DRAM) ○ Direct dring capability of memory element ○ Including timing control



5. NOTES ON MOUNTING 1 MB MEMORY ON A BOARD

The advent of a 64K bit dynamic RAM such as the MSM3764 has made it extremely easy to mount 1 MB memory on a board from the viewpoint of mounting space. In this case, however, note the following points since the number of memory elements mounted is so large as 128 ~ 176 (when redundant bits are provided).

<table>
<tr><th>Point to be noted</th><th>Consideration</th><th>Practical example</th></tr>
<tr><td>Mounting of memory elements</td><td>Memory elements may be integrated or divided.
(Design the memory array(s) to make the drive lines shortest.)</td><td> 
</td></tr>
<tr><td>Memory element driving method</td><td>Take care about the delay time and undershoot noise of the drive element.
(If the condition $V_{ILmin} = -1V$ recommended for the MOS dynamic RAM operation is satisfied, the memory elements will display the full reliability.)</td><td>Drive element
<table>
<tr><th>Parameter / Element</th><th>Delay time</th><th>(mA) IOL</th><th>Noise</th></tr>
<tr><td>7404</td><td>Medium speed</td><td>16</td><td>○</td></tr>
<tr><td>74S04</td><td>High speed</td><td>20</td><td>×</td></tr>
</table></td></tr>
<tr><td rowspan="3">Measures against noise</td><td>○ Two layers are enough for a board.
(Pay attention to the power line pattern.)</td><td></td></tr>
<tr><td>○ High frequency noise</td><td>Mount a 0.1 ~ 1 μF capacitor for every two memory elements.</td></tr>
<tr><td>○ Low frequency noise</td><td>Mount a tantalum capacitor etc. of 50 μF or more near the power input pin of the memory package.</td></tr>
<tr><td rowspan="2">Timing design</td><td>○ Prevent skew between each timing in order to enhance the system access speed.</td><td>Use ICs of the same tipe for racing timing (for example, $\overline{RAS}$ or $\overline{CAS}$).</td></tr>
<tr><td>○ Make a sufficient margin in timing design.</td><td>Skew and mounting delay</td></tr>
<tr><td>Thermal design</td><td>Thermal design under the worst condition is required.</td><td>Operation at a case temperature of 70°C must be guaranteed.</td></tr>
</table>

6. MEMORY SYSTEM RELIABILITY

6.1 Reliability Determination Factors

The memory system reliability depends upon the four factors shown in the left column of the following table. These factors are determined as shown in the right column of this table.

Memory system reliability factor	Factor determination
System-required reliability	Determined by the user-required specifications (MTBF).
Unit capacity	α [MB] = [word depth] x [bit count]
Parts reliability	Logic element ——— Hard error Memory element ——— Soft error
Cost	

6.2 Hard Error and Soft Error

(I) Hard error

A hard error is a permanent error which occurs each time a certain address is accessed.

(II) Soft error

A soft error is a transient error that does not repeat. The following are the three causes for soft errors:

(1) Insufficient power margin
(2) Insufficient system noise margin
(3) Particle failure
(4) Insufficient power margin
(5) Insufficient system noise margin
(6) particle failure

Items (1) through (5) are largely influenced by the system design. For item (6), it is required to consider whether a remedy such as ECC should be taken or not to satisfy the system-required reliability based on the parts reliability (pertaining to hard errors and soft errors). See 1.3 and 1.4 for details.

6.3 Measures for Reliability Enhancement

The following are the two typical means for the enhancement of system reliability.

(1) Parity..... Error detection only (makes no contribution to the MTBF enhancement)
(2) ECC..... The SEC-DED* is used in general

*Single Error Correct — Double Error Detect
(one bit error correction and two bit error detection)

6.4 Reliability Calculation Method

MTBF for a hard error and a soft error

(1) Memory element reliability

Hard error $r_H = e^{-\lambda H \cdot t}$ (λ_H: Hard error rate)
Soft error $r_S = e^{-\lambda S \cdot t}$ (λ_S: Soft error rate)

Reliability

$$R = \underbrace{(r_H)^n}_{①} + \underbrace{nC_1 \cdot (r_H \cdot r_S)^{n-1} \cdot (1 - r_H)}_{②}$$

① Probability of no hard error
② Probability of one bit hard error followed by no hard or soft error

Find a value for t when the value of R is e^{-1}.
The following calculations are based on the assumption that there is a low probability of two bit soft error occurrence.

(2) Memory unit reliability

Assume a memory unit whose size is n bits in bit width and k blocks in address capacity. The memory element reliability is expressed as follows:

$$r = e^{-\lambda t} \quad (\lambda: \text{ error rate})$$

① One bit correction

Find a value for t which satisfies the following expression:

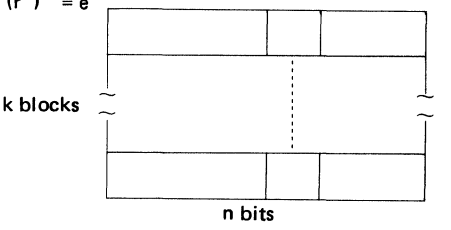
$$R = \left\{ \underbrace{(r)^n}_{①} + \underbrace{nC_1 \cdot r^{n-1}(1 - r)}_{②} \right\}^k = e^{-1}$$

① Probability of all bits being correct
② Probability of error occurrence for only one bit

② Only parity error detection without bit correction

Find a value for t which satisfies the following expression:

$$R = (r^n)^k = e^{-1}$$



6.5 Reliability Calculation Result Example

(1) Comparison of 64k byte, 128k byte, and 256k byte configurations (without ECC)

① 64kbyte

Element	λH (Fit)	λS (Fit)	MTBF (years)
64k	100	1000	11.5
16k	100	200	10.6
		100	15.9
		50	21.1
	50	200	12.7
		100	21.1
		50	31.7

② 128kbyte

Element	λH (Fit)	λS (Fit)	MTBF (years)
64k	100	1000	5.8
16k	100	200	5.3
		100	7.9
		50	10.6
	50	200	6.3
		100	10.6
		50	15.9

③ 256kbyte

Element	λH (Fit)	λS (Fit)	MTBF (years)
64k	100	1000	2.9
16k	100	200	2.6
		100	4.0
		50	5.3
	50	200	3.2
		100	5.3
		50	7.9

Notes: 1. The bit width is 9 bits for each case.
2. 1 bit is used for parity error detection.

(2) Comparison of 1M byte configurations (with ECC)

Element	λH (Fit)	λS (Fit)	Reliability (years)	
			Bit width: 22 bits	Bit width: 39 bits
64k	100 (100%)	1000	8.2 (0.76)	7.9 (0.79)
	100 (50% 50%)	1000	13.9 (0.76)	14.5 (0.79)
16k	100 (100%)	100	8.3 (1.05)	6.8 (1.08)
	100 (50% 50%)	100	13.0 (1.05)	10.7 (1.08)

Notes: 1. When the bit width is 22 bits, six bits are used for the ECC.
2. When the bit width is 39 bits, seven bits are used for the ECC.
3. Values in parentheses are the reliabilities in the case of parity error detection without ECC.
4. The (50%, 50%) in the λH column means that 50% of the hard error rate λH is handled as the total bit hard error rate and the remaining 50% is handled as the one bit hard error rate (which reflects the hard error mode analysis result confirmed so far).

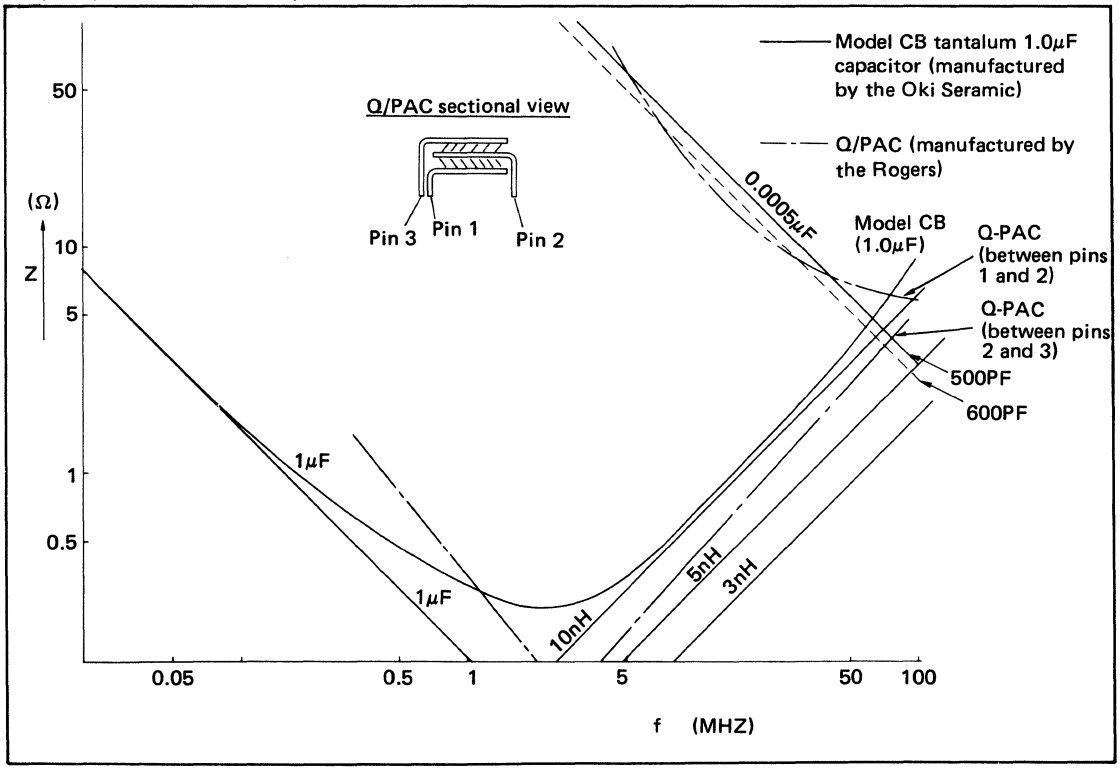
7. MEMORY COMPARISON STANDARD

In general, power, speed, and usability are required for memory elements. At present, 64K bit dynamic RAMs can be supplied by a lot of manufacturers, and these elements have almost unified specifications.

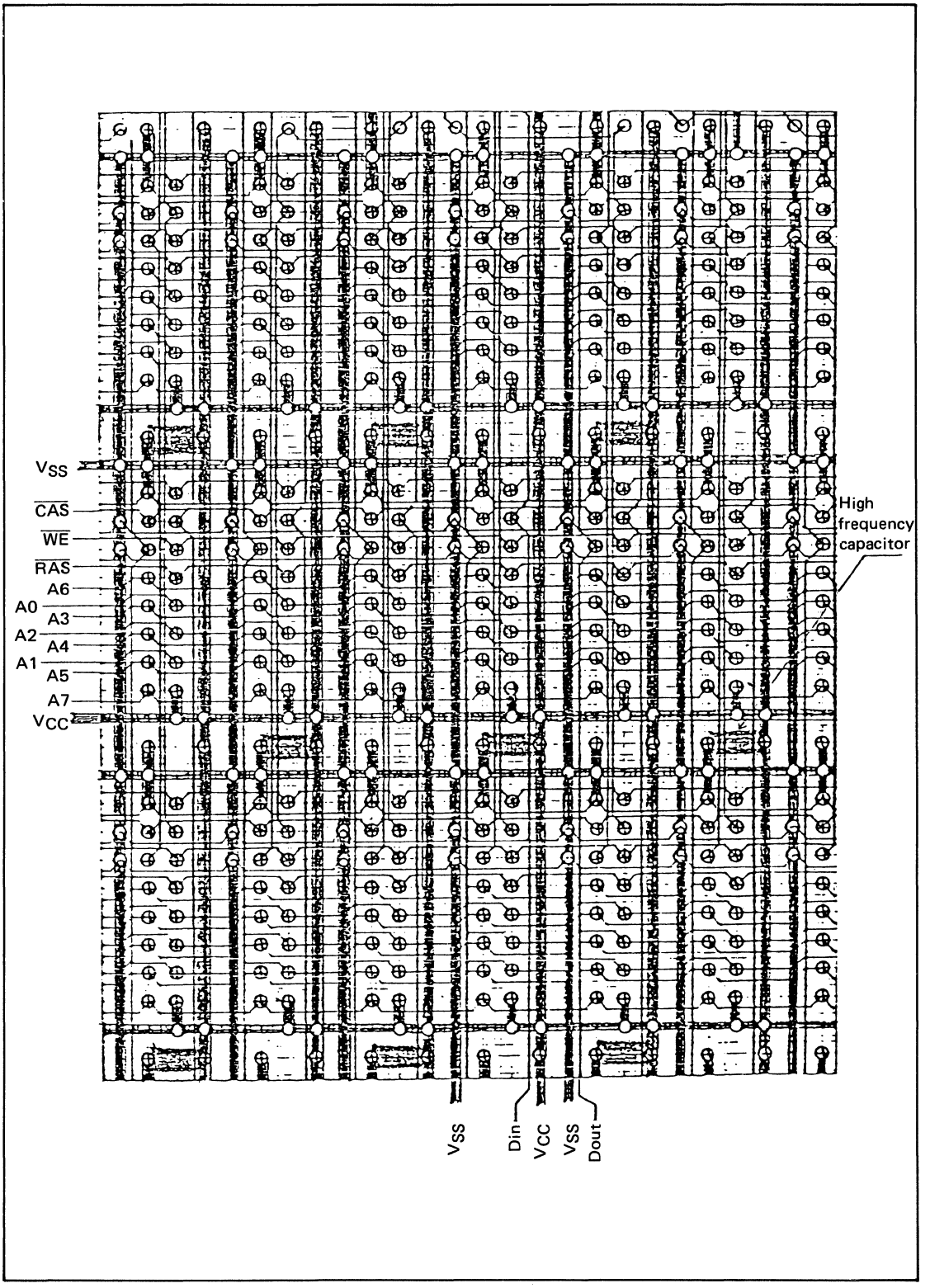
In designing a circuit board to achieve stable system operation, however, considerations must be given to the specification values and margins against the specification values, pertaining to the points shown in the following table. Factors that will affect the stable system operation are power, temperature, aging, clock skew, uneven operation of peripheral ICs, and so forth.

Point to be noted	Actual item to be considered	Reason
Power	○ Currents (Icc1, Icc3, and Icc4) at the operating time and current (Icc2) at the standby time	The power system must be noted. (example: with battery backup)
	○ Current waveform (especially the peak current value)	The noise margin must be strict for memories with large peak current.
Timing margin	○ Address setup (t_{ASR}, t_{ASC}) and hold (t_{RAH}, t_{CAH}) timing	In system designing, these timing pulses are directly related to the access time.
	○ Data setup (t_{DS}) timing and write pulse width (t_{WP})	These timing pulses are related to the cycle time in writing.
	Voltage, temperature, and dependability of each timing (especially the t_{REF} and t_{RAC})	The temperature inclination must be little for the timing pulses t_{REF} and t_{RAC}.
Voltage margin	It is impossible to achieve the ideal voltage status when used within a system.	A sufficient voltage margin must be provided under consideration of various factors which will affect the system operation stability.

Attached drawing 1
Frequency characteristics of capacitor and Q/PAC

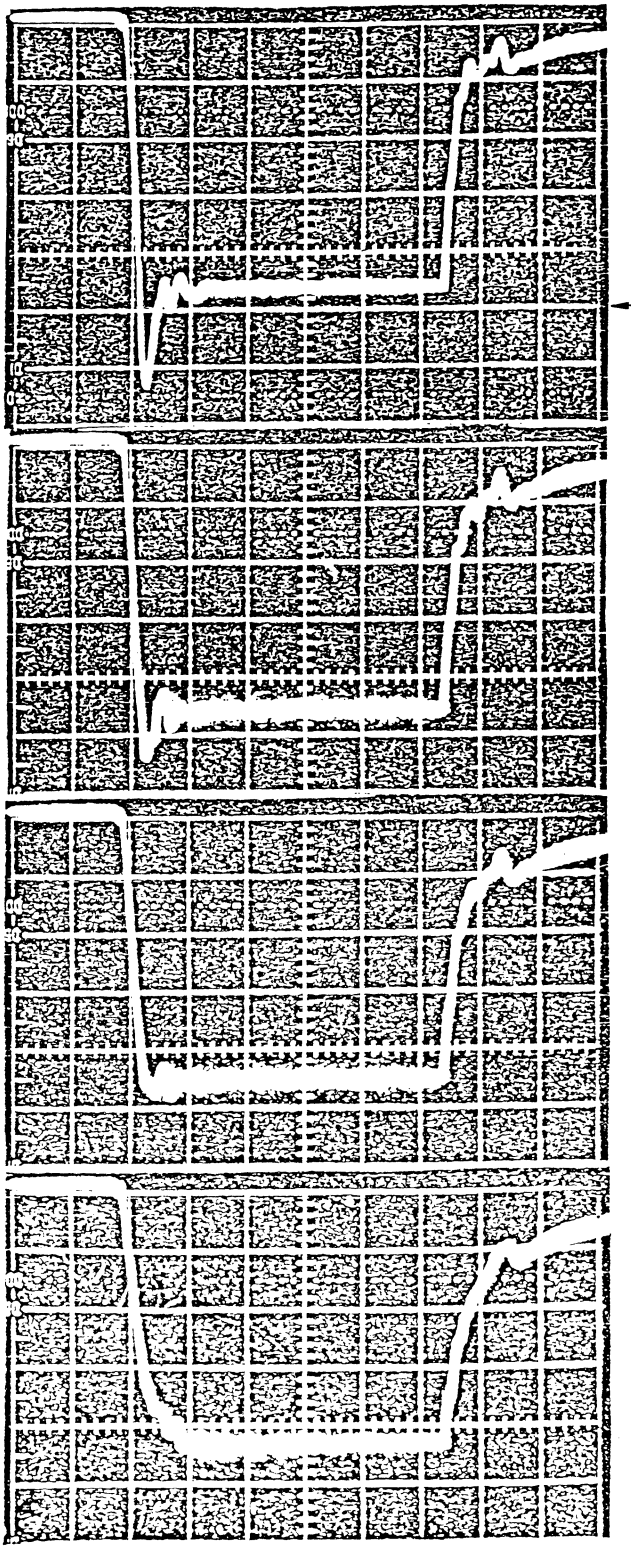


Attached drawing 2
Two layer board circuit pattern example



Attached drawing 3
Input waveform example

Horizontal: 50 ns/div
Vertical: 1 volt/div



CMOS RAM BATTERY BACK-UP

A practical example of formation of non-volatile data by CMOS static RAM battery back-up is outlined below.

1. System power and battery switching circuit

The most simplest RAM power supply (CMOS Vcc) is outlined in Fig. 1. In this case, the CMOS Vcc for normal operation is kept at a voltage 0.7V below the system voltage by the voltage drop across a diode (forward direction).

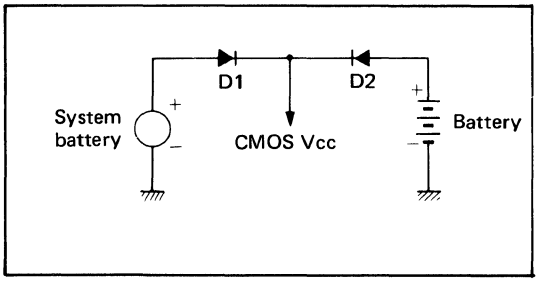


Fig. 1

Fig. 2 is an example of use of a chargeable Ni-Ca battery as the back-up battery. While the system power is being employed, the Ni-Ca battery is gradually charged up via Rc. As in Fig. 1, the diode voltage drop also poses a problem in this circuit.

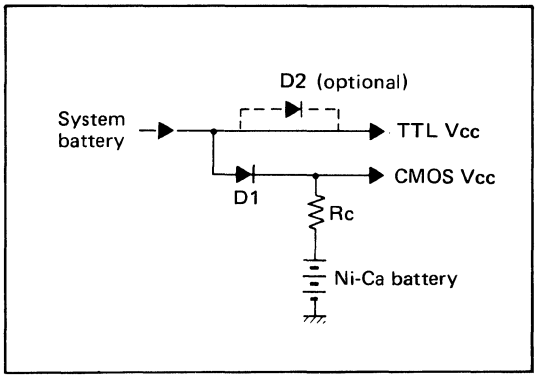


Fig. 2

The conditions for formation of non-volatile data (data retention) by battery back-up are listed below.

(1) The input signal H level must not exceed Vcc + 0.3V when the CMOS RAM Vcc power voltage is dropped.

(2) $\overline{CE}$ (or $\overline{CS}$) must maintain CMOS Vcc "H" level.

(3) In order to minimize power consumption, $\overline{WE}$, AD, DIN (or I/O) must be set to GND level or to the same "H" level as CMOS Vcc. (This is not necessary, however, for CMOS RAMs with chip select floating capability).

Note: $\overline{CS}$ floating capability
Power down possible irrespective of other input levels when memory has not been selected (i.e. when $\overline{CS}$ = H).

Consequently, if the TTL Vcc level is greater than the CMOS RAM supply voltage, and the RAM driver is at the TTL Vcc level, the CMOS RAM input voltage will exceed CMOS Vcc + 0.3V (a situation which must be avoided). Therefore, in order to reduce the voltage difference between CMOS Vcc and TTL Vcc with the battery voltage set to at least 4.5V or 4.75V (due to the RAM operating supply voltage range), the D2 diode may be added to obtain a system voltage level at least 0.7V above 4.5 ~ 4.75V (which will keep CMOS Vcc and TTL Vcc within the respective CMOS and TTL operating supply voltage ranges).
To cope with (1) and (3), a CMOS driver which will also operate at a low voltage Vcc during data hold may be employed, or else, the open collector and open drain buffer may be pulled up to CMOS Vcc in order to drive the RAM.
A control circuit for coping with (2) when an abnormal system power supply is detected is also required.

2. Switching Circuit Modifications

Modification of the diode switching circuit can employ PNP transistors. Voltage drops by PNP transistor V_{CE} are smaller by about 0.2V, and this can lead to the generation of a system "power fail" signal.

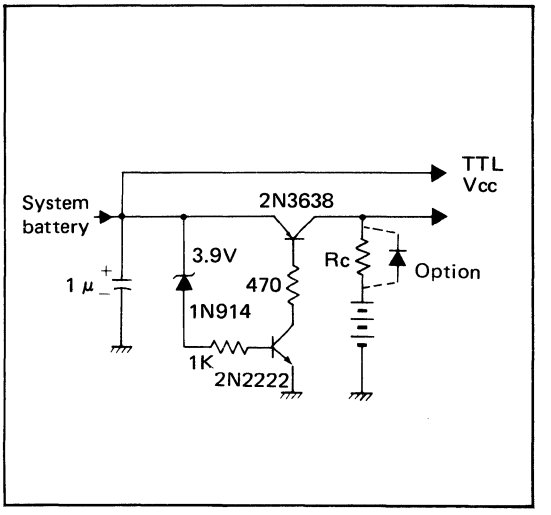


Fig. 3

Fig. 3 outlines a switching circuit employing a PNP transistor. The Rc used when a chargeable battery is employed is replaced by a diode when a non-chargeable battery is used. In this case, switching occurs at the zener diode voltage, so "power fail" must be detected by another circuit, and $\overline{CE}$ set to CMOS Vcc "high" level.

■ CMOS RAM BATTERY BACK-UP ■

Figs. 4 and 5 are examples of circuits capable of generating a POWER FAIL output signal. In these circuits, the C2 capacitance must be rather large, the important point being the need for a smooth gradual change in CMOS Vcc when the system power is cut. See next page for further details.

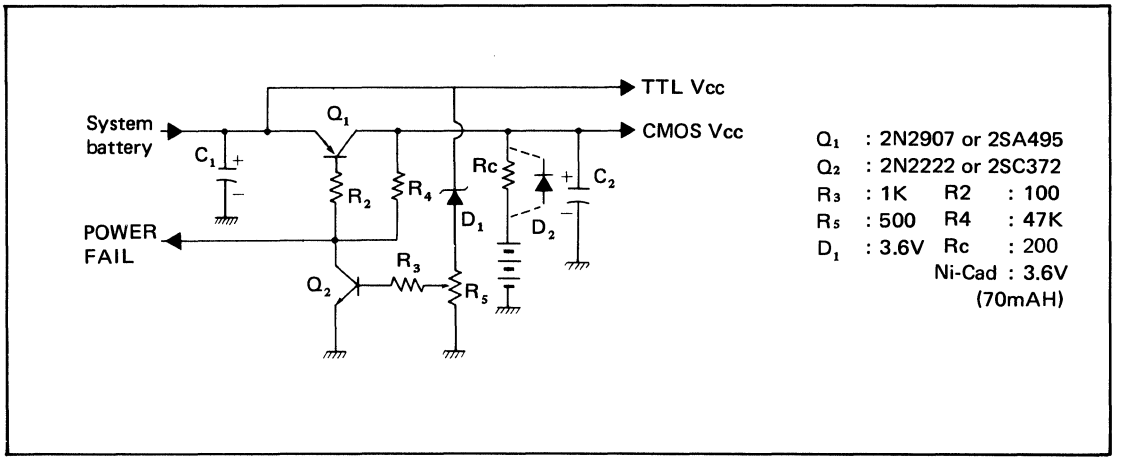


Fig. 4

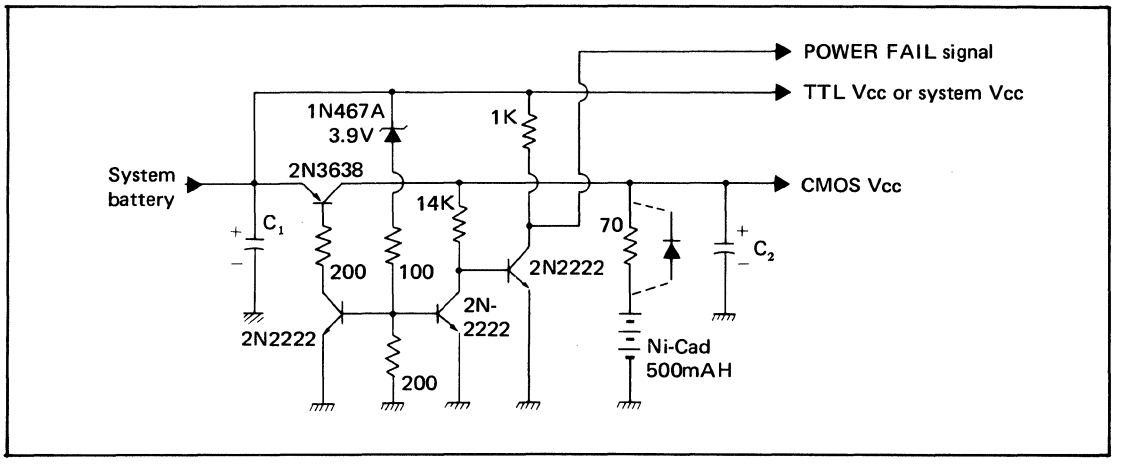


Fig. 5

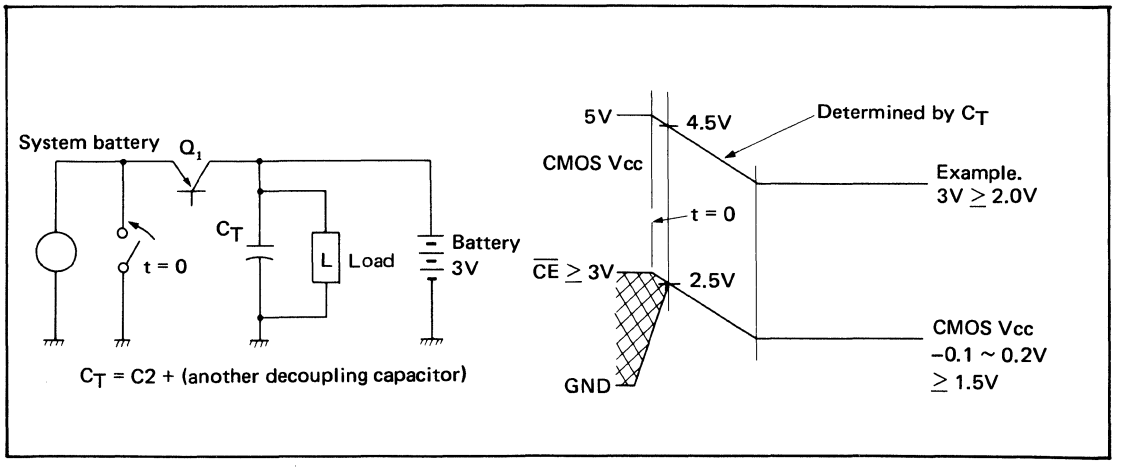


Fig. 6

3. Data Retention Mode

The RAM driver (peripheral circuit) is determined according to conditions (1) and (3) required for data retention. In Oki Electric CMOS RAMs, the power voltage during data retention is kept at a minimum of 2.0V. The $\overline{CE}$ (or $\overline{CS}$) voltage at this time has to be kept at about Vcc -0.2V. And as was mentioned earlier, the CMOS Vcc must drop smoothly when the system power is cut until it reaches the power voltage for data retention (practically equivalent to the battery voltage, or else reduced by the diode voltage drop). And although $\overline{CE}$ traces the slope of CMOS Vcc reduction at this time, a smooth change in $\overline{CE}$ is also a necessary condition for actual circuits.

(4) When switching to retention mode, or from retention mode to operation mode, $\overline{CE}$ must exhibit a smooth change. If noise is generated in $\overline{CE}$ in this case, the data will be subject to rewriting.

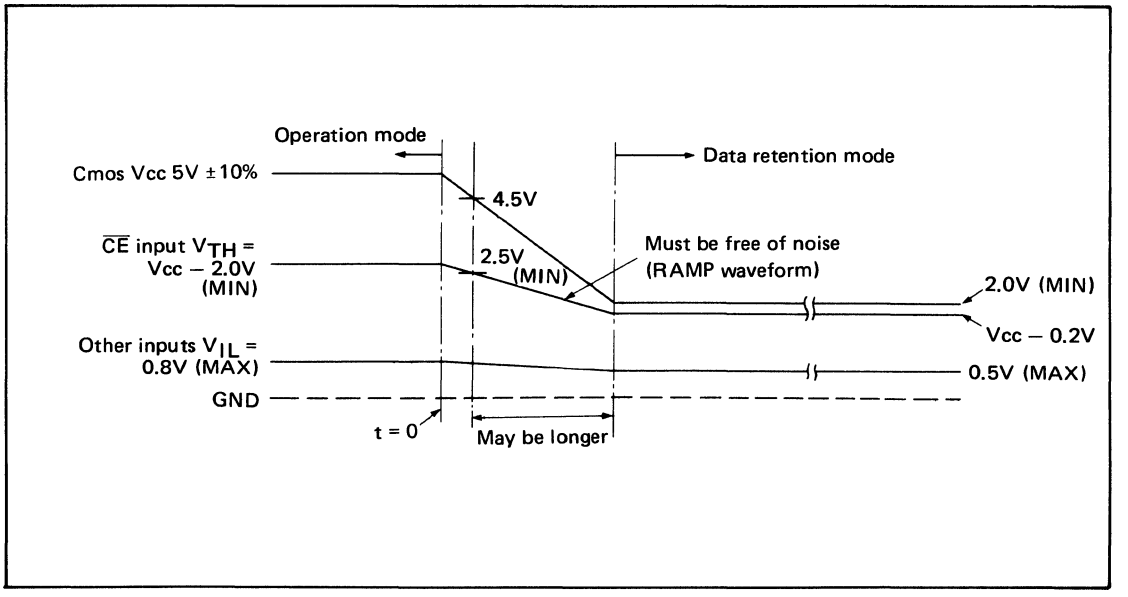


Fig. 7

(5) When switching to operation mode, commence operation after elapse of t_{RC} (read cycle time) following Vcc reaching the operating power voltage range.

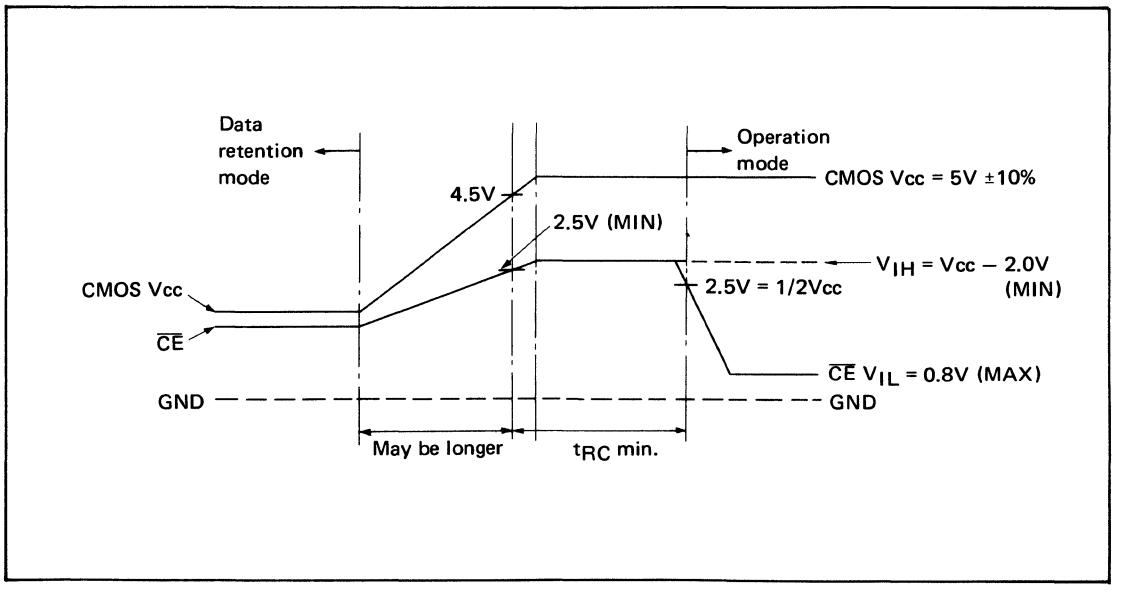


Fig. 8

4. Interfacing

A) TTL Interface

In the case of CMOS RAM drive by TTL, use an open-collector type TTL according to conditions (1) and (3).

When the system power line (i.e. TTL Vcc) is cut, the open-collector TTL Q2 in Fig. 9 is turned off, followed by Q1 also being turned off, resulting in the CMOS RAM input being pulled-up to CMOS Vcc.

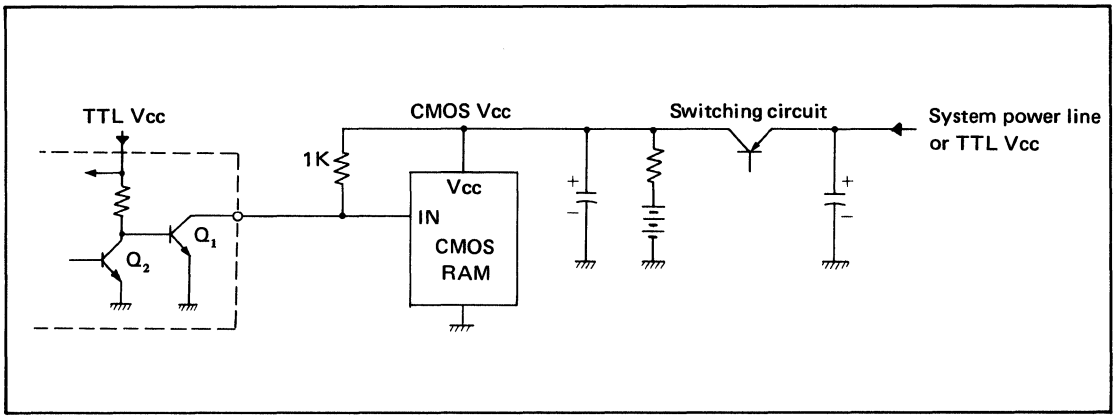


Fig. 9

When the power line voltage in LS type TTL is dropped to ground, the output is also dropped to ground, thereby making the pull-up resistors for address line buffers etc no longer necessary. In this case, however, it will not be possible to employ this as a control line buffer which must be switched to "high" during $\overline{CE}$ (or $\overline{CS}$) data retention.

(6) In order to minimize the consumption current during data retention, all inputs except $\overline{CE}$ (or $\overline{CS}$, this being designated as either "high" or "low") must be maintained at either GND or CMOS Vcc. (This does not apply, however, for CMOS RAMs equipped with $\overline{CS}$ floating function).

B) CMOS Interface

In systems where the CMOS RAM is driven by CMOS buffer, operation must be at the data retention power voltage, and the corresponding output voltage must satisfy the requirements indicated in Figs. 7 and 8.

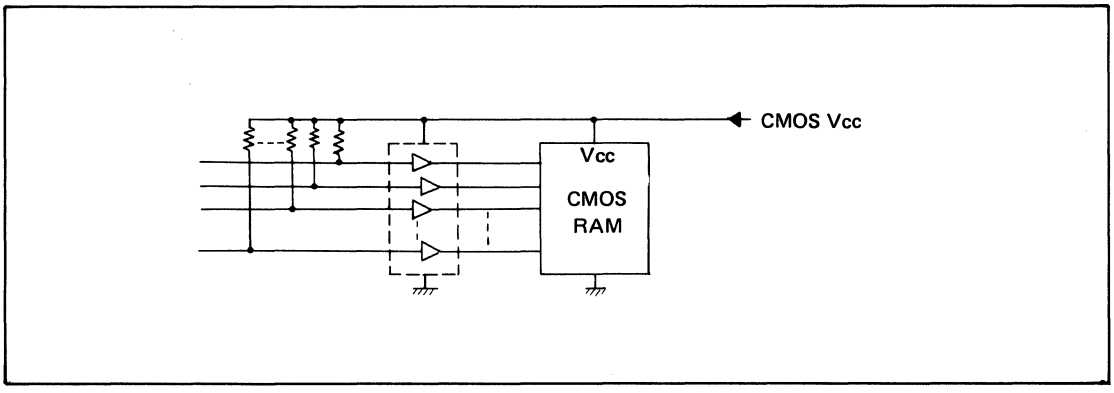


Fig. 10

5. Miscellaneous

In order to further reduce power consumption during data retention by even a small margin, the use of a MOS FET as the transistor generating the POWER FAIL output signal is recommended. This is in order to prevent flow of current from the 14kΩ resistor.

MASK ROM KANJI GENERATION MEMORY DESCRIPTION

1. KANJI GENERATION MEMORIES

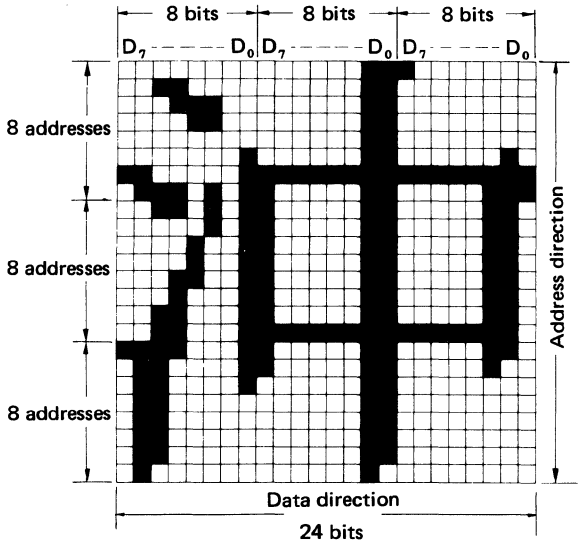
	IC models	Number of codes	Character storing capacity	Configuration	Character style	Bit capacity	Access time
High speed memories	M S M38128- 00 ≀ M S M38128- 17	18	JIS standard No. 1 3418 characters	24 x 24	Ming style	128K bits	450μs max
	M S M38128- 18 ≀ M S M38128- 27	10	JIS standard No. 1 3418 characters	16 x 18	Gothic style	128K bits	450μs max
Low speed memories	M S M28101A	1	JIS standard No. 1 3418 characters	16 x 18	Gothic style	1M bits	10μs max (16 x 18 transfer)
	M S M28201A	1	JIS standard No. 2 3384 characters	16 x 18	Gothic style	1M bits	10μs max (16 x 18 transfer)

2. MSM38128 SERIES

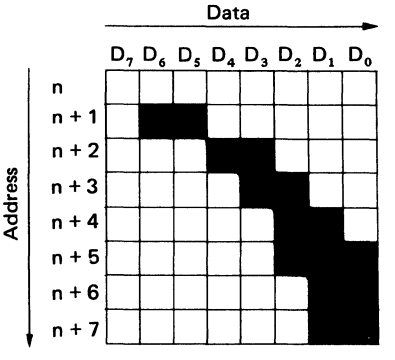
The electrical specifications of the MSM38128 series high speed kanji generation memory ICs conform to the specifications of the MSM38128 16384 word x 8 bit mask ROM, except that the output enable ($\overline{OE}$) signal is active when set at a low level. The character data is represented by high level output and background data is represented by low level output.

2.1 Pattern Storing Method

(1) 24 x 24 . . . . . Ming style
The 8 address x 8 bit data per character is stored in one chip, and one character is configured with nine chips.



One character storing method (24 x 24)



Data direction and address direction

11

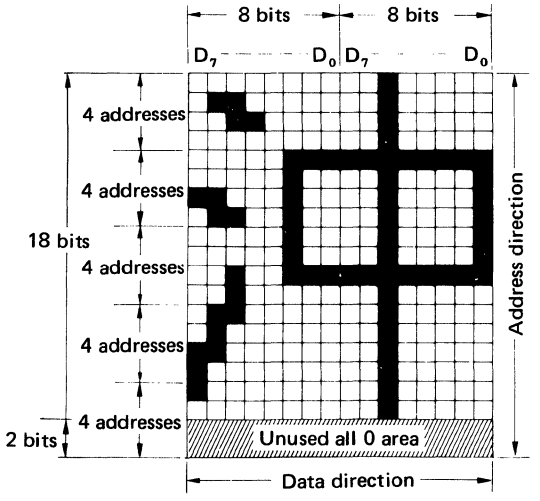
Since approximately 2K bits of character data can be stored in nine chips, the 3418 JIS standard No. 1 characters are divided into two for storing in two groups of nine chips.
The nine codes to form a character are stored in nine chips as shown in the following figure.

M S M38128 -00	M S M38128 -01	M S M38128 -02
M S M38128 -03	M S M38128 -04	M S M38128 -05
M S M38128 -06	M S M38128 -07	M S M38128 -08

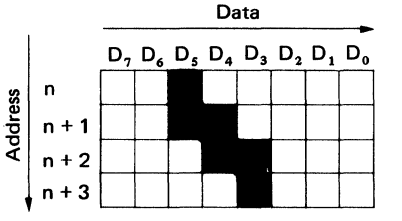
M S M38128 -09	M S M38128 -10	M S M38128 -11
M S M38128 -12	M S M38128 -13	M S M38128 -14
M S M38128 -15	M S M38128 -16	M S M38128 -17

Correspondence of chips to nine codes of a character

(2) 16 x 18 . . . . . Gothic style
The 4 address x 8 bit data per character is stored in one chip, and one character is configured with ten chips. Each character data is associated with unused data of two addresses.



One character storing method
(16 x 18)



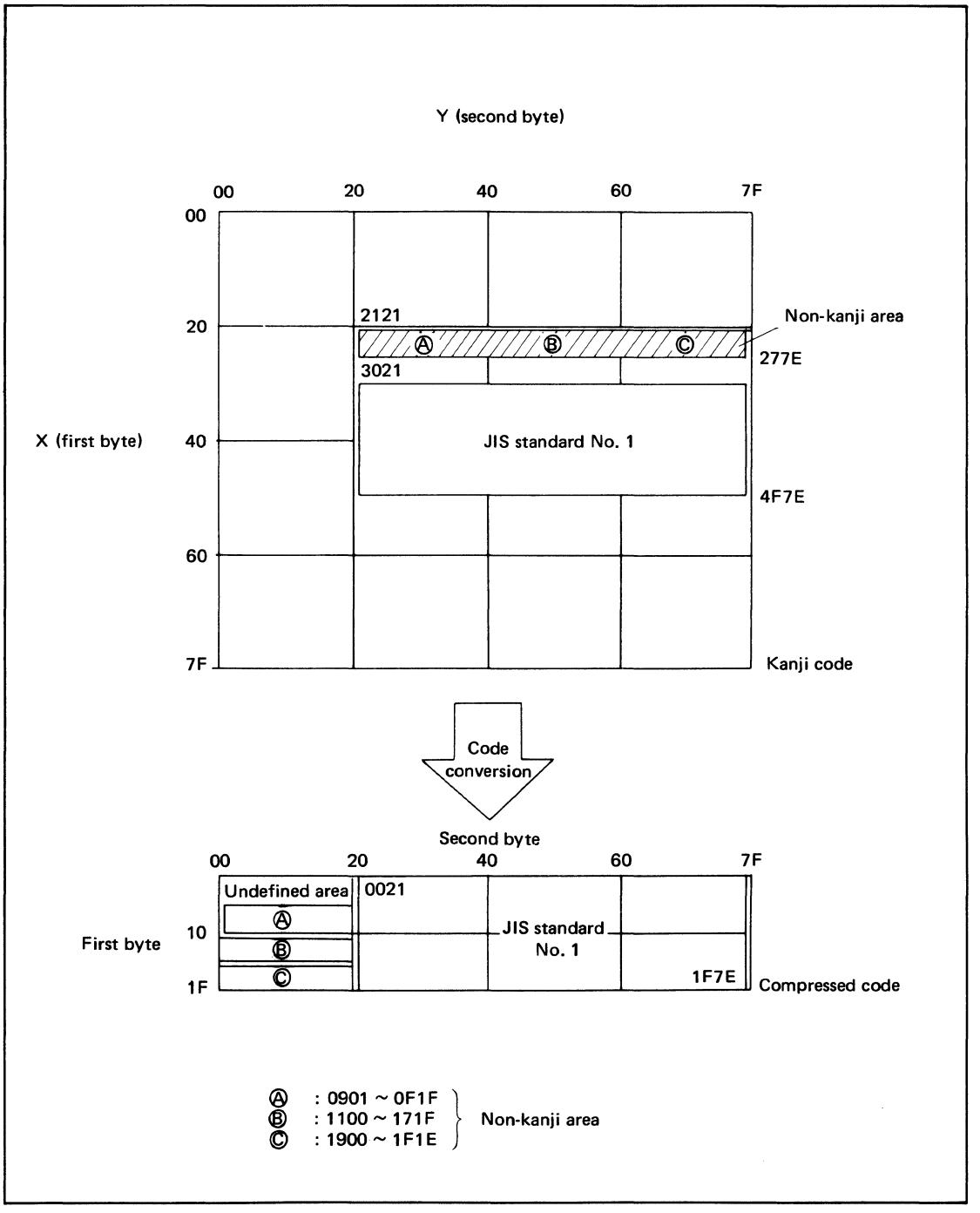
Data direction and address direction

The ten codes to form a character are stored in ten chips as shown in the following figure.

M S M38128 -18	M S M38128 -19
M S M38128 -20	M S M38128 -21
M S M38128 -22	M S M38128 -23
M S M38128 -24	M S M38128 -25
M S M38128 -26	M S M38128 -27

2.2 Code Compression

The MSM38128 series memories perform code compression so that a correspondence can be established between the JIS kanji codes and compressed codes.



Note: In the case of 24 x 24 character data, the part above the broken line is stored in the MSM38128-00 to 08 chips and the part under the broken line is stored in the MSM38128-09 to 17 chips.

< Compressed code >

First byte	0	0	a_{12}	a_{11}	a_{10}	a_9	a_8
Second byte	a_7	a_6	a_5	a_4	a_3	a_2	a_1

The following rule applies to the code conversion from JIS kanji code to compressed code.

JIS kanji code

First byte

X_7	X_6	X_5	X_4	X_3	X_2	X_1

Second byte

Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

Conversion

Compressed code

< Non-kanji area >

First byte

a_{12}	a_{11}	a_{10}	a_9	a_8		
0	0	Y_7	Y_6	X_3	X_2	X_1

Second byte

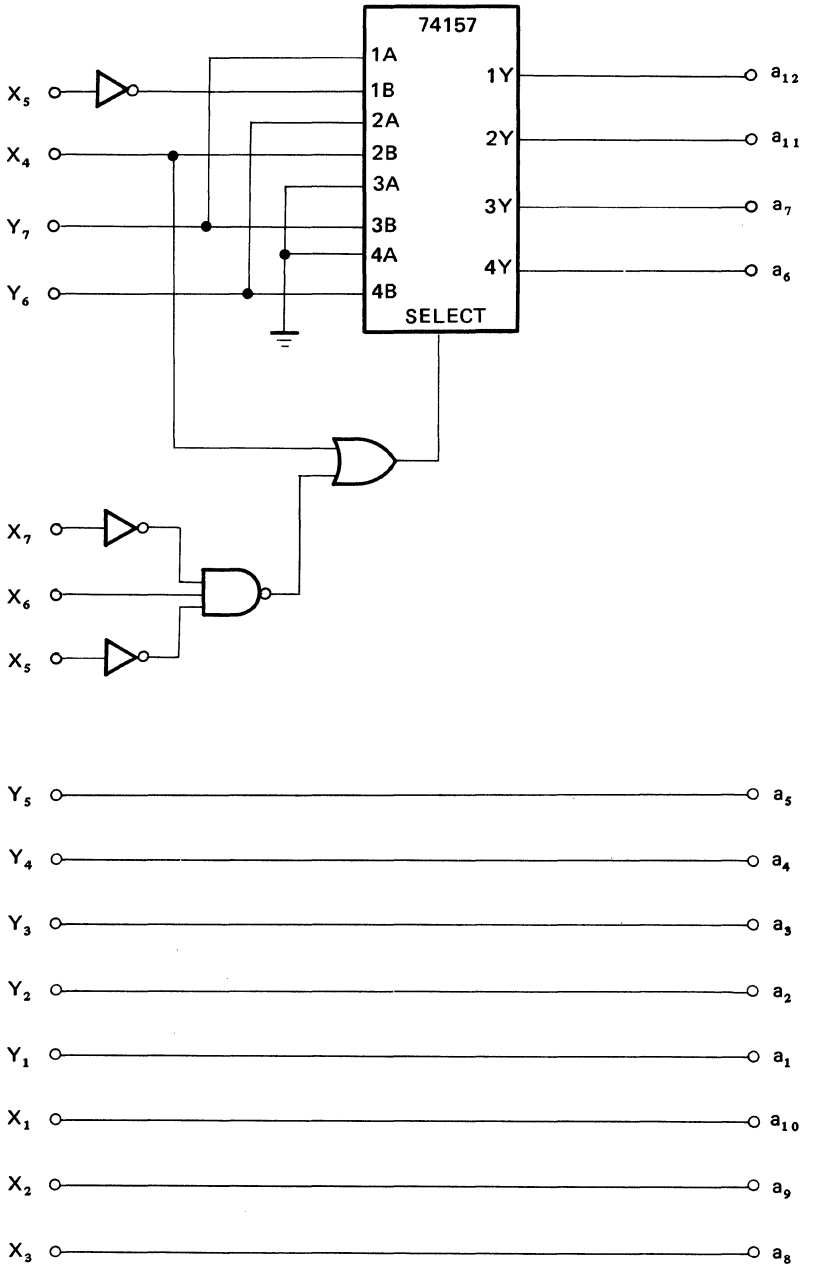
a_7	a_6	a_5	a_4	a_3	a_2	a_1
0	0	Y_5	Y_4	Y_3	Y_2	Y_1

< JIS standard No. 1 kanji area >

0	0	X_5	X_4	X_3	X_2	X_1

Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

2.3 Code Compressing Conversion Circuit Example



2.4 Simultaneous Reading of 24 Horizontal Bits of 24 x 24 Character Data, Example

Compressed code [a_{12} a_{11} ..... a_2 a_1] < 12 bits >
MSB LSB

Row address within a character [b_5 b_4 b_3 b_2 b_1] < 5 bits >
MSB LSB

The correspondence between the MSM38128 address input signal and compressed code is shown in the following table.

Address input	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Compressed code	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	b_3	b_2	b_1

For the selection of ROM codes, a decode signal composed of bits b4, b5, and a12 is input to the $\overline{CE}$ and $\overline{OE}$ pins.

a_{12}	b_5	b_4	ROM codes
0	0	0	MSM38128-00, -01, 002
0	0	1	MSM38128-03, -04, -05
0	1	0	MSM38128-06, -07, -08
1	0	0	MSM38128-09, -10, -11
1	0	1	MSM38128-12, -13, -14
1	1	0	MSM38128-15, -16, -17

2.5 Simultaneous Reading of 16 Horizontal Bits of 16 x 18 Character Data, Example

Compressed code [a_{12} a_{11} ..... a_2 a_1]
MSB LSB

Row address within a character [b_5 b_4 b_3 b_2 b_1]
MSB LSB

The correspondence between the MSM38128 address input signal and compressed code is shown in the following table.

Address input	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Compressed code	a_{12}	a_{11}	a_{10}	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	b_2	b_1

For the selection of ROM codes, a decode signal composed of bits b_3, b_4, and b_5 is input to the $\overline{CE}$ and $\overline{OE}$ pins.

b_5	b_4	b_3	ROM codes
0	0	0	MSM38128-18, -19
0	0	1	MSM38128-20, -21
0	1	0	MSM38128-22, -23
0	1	1	MSM38128-24, -25
1	0	0	MSM38128-26, -27

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