PHILIPS

Data handbook

PHILIPS

Electronic components and materials

Integrated circuits

Part 1 May 1980

Bipolar ICs for radio and audio equipment

INTEGRATED CIRCUITS

PART 1 - MAY 1980

BIPOLAR ICs FOR RADIO AND AUDIO EQUIPMENT

DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, sub-assemblies and materials; it is made up of four series of handbooks each comprising several parts.

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

ELECTRON TUBES (BLUE SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	February 1980	T1 02-80 (ET1a 12-75)	**Tubes for r.f. heating**
Part 2	April 1980	T2 04-80 (ET1b 08-77)	**Transmitting tubes for communications**
Part 2a	November 1977	ET2a 11-77	**Microwave tubes** Communication magnetrons, magnetrons for microwave heating, klystrons, travelling-wave tubes, diodes, triodes T-R switches
Part 2b	May 1978	ET2b 05-78	**Microwave semiconductors and components** Gunn, Impatt and noise diodes, mixer and detector diodes, backward diodes, varactor diodes, Gunn oscillators, sub-assemblies, circulators and isolators
Part 3	January 1975	ET3 01-75	**Special Quality tubes, miscellaneous devices**
Part 5a	October 1979	ET5a 10-79	**Cathode-ray tubes** Instrument tubes, monitor and display tubes, C.R. tubes for special applications
Part 5b	December 1978	ET5b 12-78	**Camera tubes and accessories, image intensifiers**
Part 6	January 1977	ET6 01-77	**Products for nuclear technology** Channel electron multipliers, neutron tubes, Geiger-Müller tubes
Part 7a	March 1977	ET7a 03-77	**Gas-filled tubes** Thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes
Part 7b	May 1979	ET7b 05-79	**Gas-filled tubes** Segment indicator tubes, indicator tubes, switching diodes, dry reed contact units
Part 8	July 1979	ET8 07-79	**Picture tubes and components** Colour TV picture tubes, black and white TV picture tubes, monitor tubes, components for colour television, components for black and white television
Part 9	March 1978	ET9 03-78	**Photomultiplier tubes; phototubes**

SEMICONDUCTORS (RED SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	March 1980	S1 03-80 (SC1b 05-77)	**Diodes** Small-signal germanium diodes, small-signal silicon diodes, special diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes
Part 2	May 1980	S2 05-80 (SC1a 08-78)	**Power diodes, thyristors, triacs** Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs
Part 2	June 1979	SC2 06-79	**Low-frequency power transistors**
Part 3	January 1978	SC3 01-78	**High-frequency, switching and field-effect transistors** *
Part 3	April 1980	S3 04-80 (SC2 11-77, partly) (SC3 01-78, partly)	**Small-signal transistors**
Part 4a	December 1978	SC4a 12-78	**Transmitting transistors and modules**
Part 4b	September 1978	SC4b 09-78	**Devices for optoelectronics** Photosensitive diodes and transistors, light-emitting diodes, photocouplers, infrared sensitive devices, photoconductive devices
Part 4c	July 1978	SC4c 07-78	**Discrete semiconductors for hybrid thick and thin-film circuits**

* Field-effect transistors and wideband transistors will be transferred to S5 and SC3c respectively. The old book SC3 01-78 should be kept until then.

INTEGRATED CIRCUITS (PURPLE SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code. Books with the purple cover will replace existing red covered editions as each is revised.

Part 1	**May 1980**	**IC1 04-80** **(SC5b 03-77)**	**Bipolar ICs for radio and audio equipment**
Part 2	**May 1980**	**IC2 04-80** **(SC5b 03-77)**	**Bipolar ICs for video equipment**
Part 5a	**November 1976**	**SC5a 11-76**	**Professional analogue integrated circuits**
Part 6	**October 1977**	**SC6 10-77**	**Digital integrated circuits** LOCMOS HE4000B family
Part 6b	**August 1979**	**SC6b 08-79**	**ICs for digital systems in radio and television receivers**
Signetics integrated circuits			Bipolar and MOS memories 1979 Bipolar and MOS microprocessors 1978 Analogue circuits 1979 Logic - TTL 1978

COMPONENTS AND MATERIALS (GREEN SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced.
The former code of the preceding issue is given in brackets under the new code.

Part 1	**July 1979**	**CM1 07-79**	**Assemblies for industrial use** PLC modules, high noise immunity logic FZ/30 series, NORbits 60-series, 61-series, 90-series, input devices, hybrid integrated circuits, peripheral devices
Part 3a	**September 1978**	**CM3a 09-78**	**FM tuners, television tuners, surface acoustic wave filters**
Part 3b	**October 1978**	**CM3b 10-78**	**Loudspeakers**
Part 4a	**November 1978**	**CM4a 11-78**	**Soft Ferrites** Ferrites for radio, audio and television, beads and chokes, Ferroxcube potcores and square cores, Ferroxcube transformer cores
Part 4b	**February 1979**	**CM4b 02-79**	**Piezoelectric ceramics, permanent magnet materials**
Part 6	**April 1977**	**CM6 04-77**	**Electric motors and accessories** Small synchronous motors, stepper motors, miniature direct current motors
Part 7	**September 1971**	**CM7 09-71**	**Circuit blocks** Circuit blocks 100 kHz-series, circuit blocks 1-series, circuit blocks 10-series, circuit blocks for ferrite core memory drive
Part 7a	**January 1979**	**CM7a 01-79**	**Assemblies** Circuit blocks 40-series and CSA70 (L), counter modules 50-series, input/output devices
Part 8	**June 1979**	**CM8 06-79**	**Variable mains transformers**
Part 9	**August 1979**	**CM9 08-79**	**Piezoelectric quartz devices** Quartz crystal units, temperature compensated crystal oscillators
Part 10	**April 1978**	**CM10 04-78**	**Connectors**
Part 11	**December 1979**	**CM11 12-79**	**Non-linear resistors** Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
Part 12	**November 1979**	**CM12 11-79**	**Variable resistors and test switches**
Part 13	**December 1979**	**CM13 12-79**	**Fixed resistors**
Part 14	**April 1980**	**C14 04-80** **(CM2b 02-78)**	**Electrolytic and solid capacitors**
Part 15	**May 1980**	**C15 05-80** **(CM2b 02-78)**	**Film capacitors, ceramic capacitors, variable capacitors**

FUNCTIONAL AND NUMERICAL INDEX
MAINTENANCE TYPE LIST

SELECTION GUIDE BY FUNCTION

AM CHANNELS

TDA1072	AM receiver circuit
TEA5550	AM car radio receiver circuit

FM CHANNELS

TCA420A	hi-fi FM/IF amplifier
TEA5560	FM/IF system for car radios and hi-fi

AM/FM COMBINED CHANNELS

TBA570A; AQ	AM/FM radio receiver circuit
TBA700	AM/FM radio receiver circuit
TDA5700; Q	AM/FM radio receiver circuit

STEREO DECODERS

TDA1005A; AT	frequency multiplex PLL stereo decoder

INTERFERENCE SUPPRESSORS

TDA1001A; AT	interference absorption circuit

D.C. CONTROLLED AUDIO CIRCUITS

TCA730A	d.c. volume and balance stereo control circuit
TCA740A	d.c. treble and bass stereo control circuit
TDA1028	signal-sources switch (2 x four channels)
TDA1029	signal-sources switch (4 x two channels)
TDA1074	dual electronic stereo potentiometer circuit

VOLTAGE STABILIZERS

TCA530	voltage stabilizer for electronic tuning
TCA750	multi-stabilizer for electronic tuning

AUDIO POWER AMPLIFIERS

TCA760B	1,5 W audio amplifier
TDA1004A	10 W audio power amplifier with thermal shut-down
TDA1010	6 W audio power amplifier
TDA1011	2 to 6 W audio power amplifier
TDA1011A	2 to 6 W audio power amplifier with inverted input/output
TDA1013	4 W audio power amplifier with d.c. volume control
TDA1512	12 to 20 W hi-fi audio power amplifier
TDA2611A	5 W audio power amplifier

RECORDER AMPLIFIERS

TDA1002A	recording and playback amplifier
TDA1012	recording/playback and 2 W audio power amplifier

SELECTION GUIDE BY FUNCTION (continued)

MOTOR SPEED CONTROL ICs

TDA1003A	motor regulator and bias/erase oscillator circuit
TDA1006A	motor regulator with automatic tape-end indicator
TDA1059B	motor speed regulator with thermal shut-down
TDA1059C	motor speed regulator
TDA1533	PLL motor speed control circuit for hi-fi applications

MISCELLANEOUS

OM200/S2	integrated amplifier for use in ear hearing aids
TAA263	low-level amplifier
TAA320	integrated MOST amplifier
TAA320A	integrated MOST level sensor
TDA1008	gating/frequency divider for electronic musical instruments

NUMERICAL INDEX

MAINTENANCE TYPE LIST

The types listed below are not included in this handbook.
Detailed information will be supplied on request.

SAJ110	
TCA290A	
TCA450	
TCA730	(successor type: TCA730A)
TCA740	(successor type: TCA740A)
TDA1002	(successor type: TDA1002A)
TDA1005	(successor type: TDA1005A; AT)
TDA1006	(successor type: TDA1006A)
TDA1009	
TDA2611	(successor type: TDA2611A)

GENERAL

Preface to data of ICs
Type designation
Rating systems
Letter symbols

PREFACE TO DATA OF INTEGRATED CIRCUITS

1. General

The published data comprise particulars needed by designers of equipment in which integrated circuits are to be incorporated, and criteria on which to base acceptance testing of such circuits. For ease of reference, the data on each circuit are grouped according to the several headings discussed below.
The limiting values quoted under the headings Characteristics and Package Outline may be taken as references for acceptance testing.
Values cited as typical are given for information only.
For an explanation of the type designation code, see the section Type Designation.
For an explanation of the letter symbols used in designating terminals and performance of integrated circuits, and the electrical and logic quantities pertaining to them, see the section Letter Symbols.

2. Quick Reference Data

The main properties of the integrated circuit summarized for quick reference

3. Ratings

Ratings are limits beyond which the serviceability of the integrated circuit may be impaired. The ratings given here are in accordance with the Absolute Maximum System as defined in publication no. 134 of the International Electrical Commission; for further details see item 2 of the section Rating Systems.
If a circuit is used under the conditions set forth in the sections Characteristics and Additional System Design Data, its operation within the ratings is ensured.

4. Circuit diagram

Circuit diagrams and logic symbols are given to illustrate the circuit function. The diagrams show only essential elements, parasitic elements due to the method of manufacture normally being omitted. The manufacturer reserves the right to make minor changes to improve manufacturability.

5. System Design Data and Additional System Design Data

System Design Data normally derived from the Characteristics and based on worst-case assumptions as to temperature, loading and supply voltage, are quoted for the guidance of equipment designers. Supplementary information derived from measurements on large production samples may be given under Additional System Design Data.

6. Application information

Under this heading, practical circuit connections and the resulting performance are described. Care has been taken to ensure the accuracy and completeness of the information given, but no liability therefor is assumed, nor is licence under any patent implied.

7. Characteristics

Characteristics are measurable properties of the integrated circuit described. Under a specific set of test conditions compliance with limit values given under this heading establishes the specified performance of the circuit; this can be used as a criterion for acceptance testing.
Values cited as typical are given for information only and are not subject to any form of guarantee.

8. Logic symbols (digital circuits)

Graphical logic symbols accord with MIL standard 806B.
Supplementary drawings correlate logic functions with pin locations as a help to laying out printed circuit boards.

9. Outline drawing and pin 1 identification

Dimensional drawings indicate the pin numbering of circuit packages.
Dual in-line packages have a notch at one end to identify pin 1.
Take care not to mistake adventitious moulding marks for the pin 1 identification.
Flat packs identify pin 1 by a small projection on the pin itself and/or by a dot on the body of the package.
Metal can encapsulations identify pin 1 by a tab on the rim of the can.

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits.

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : –55 to + 125 °C
D : –25 to + 70 °C
E : –25 to + 85 °C
F : –40 to + 85 °C
G : –55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
P : for plastic DIL
Q : for QIL
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

LETTER SYMBOLS
FOR LINEAR INTEGRATED CIRCUITS

General

The voltages and currents are normally related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a number. In appropriate cases voltages, currents etc. pertinent to one or more of the circuit elements (transistors, diodes) are given in which case symbols are based on the recommendations as published in I.E.C. Publication 148.

Quantity symbols

1. Instantaneous values of current, voltage and power, which vary with time are represented by the appropriate lower case letter.

   Examples: i, v, p

2. Maximum (peak), average, d.c. and root-mean-square values are represented by the appropriate upper case letter.

   Examples: I, V, P

Polarity of current and voltage

A current is defined to be positive when its conventional direction of flow is into the device.
A voltage is measured with respect to the reference terminal, which is indicated by the subscripts. Its polarity is defined to be positive when the potential is higher than that of the reference terminal.

Subscripts

For currents the number behind the quantity symbol indicates the terminal carrying the current.

Examples: I_2, i_{14}

For voltages normally two number subscripts are used, connected by a hyphen. The first number indicates the terminal at which the voltage is measured and the second subscript the reference terminal.
Where there is no possibility of confusion the second subscript may be omitted.

Examples: V_{2-12}, v_{14-2}, V_5, v_8

To distinguish between maximum (peak), average, d.c. and root-mean-square values the following subscripts are added:

For maximum (peak) values	:	M or m
For average values	:	AV or av
For root-mean-square values	:	(RMS) or (rms)
For d.c. values	:	no additional subscripts

The upper case subscripts indicate total values.
The lower case subscripts indicate values of varying components:

Examples: I_2, I_{2AV}, $I_{2(rms)}$, $I_{2(RMS)}$

If in appropriate cases quantity symbols are pertinent to single elements of a circuit (transistors or diodes), the normal subscripts for semiconductor devices can be used.

Examples: V_{CBO}, V_{be}, V_{CES}, I_C
V_{DSS}, V_{GS}, I_D

List of subscripts:

E, e	=	Emitter terminal
B, b	=	Base terminal for bipolar transistors, Substrate for MOS devices
C, c	=	Collector terminal
D, d	=	Drain terminal
G, g	=	Gate terminal
S, s	=	Source terminal for MOS devices Substrate for bipolar transistor circuits
(BR)	=	Break-down
M, m	=	Maximum (peak) value
AV, av	=	Average value
(RMS), (rms)	=	R.M.S. value

Electrical Parameter Symbols

1. The values of four pole matrix parameters or other resistances, impedances, admittances, etc., inherent in the device, are represented by the lower case symbol with appropriate subscript.

Examples: h_i, z_f, y_o, k_r

Subscripts for Parameter Symbols

1. The static values of parameters are indicated by upper case subscripts.

Examples: h_{FE}, h_I

2. The small signal values of parameters are indicated by lower case subscripts.

Examples: h_i, z_o

3. The first subscript, in matrix notation identifies the element of the four pole matrix.

   i (for 11) = input
   o (for 22) = output
   f (for 21) = forward transfer
   r (for 12) = reverse transfer

$$\text{Examples: } V_1 = h_i I_1 + h_r V_2$$
$$I_2 = h_f I_1 + h_o V_2$$

The voltage and current symbols in matrix notation are indicated by a single digit subscript.
The subscript 1 = input; the subscript 2 = output.
The voltages and currents in these equations may be complex quantities.

4. A second subscript is used only for separate circuit elements (e.g. transistors) to identify the circuit configuration:

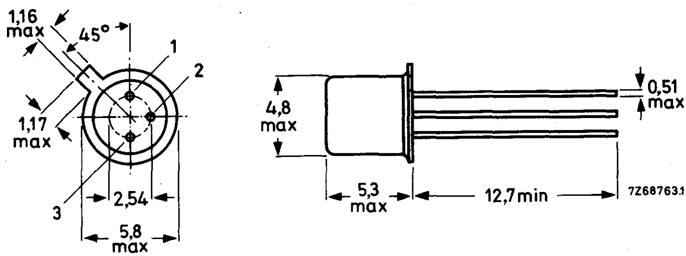
   e = common emitter
   b = common base
   c = common collector

5. If it is necessary to distinguish between real and imaginary parts of the four pole parameters, the following notation may be used:

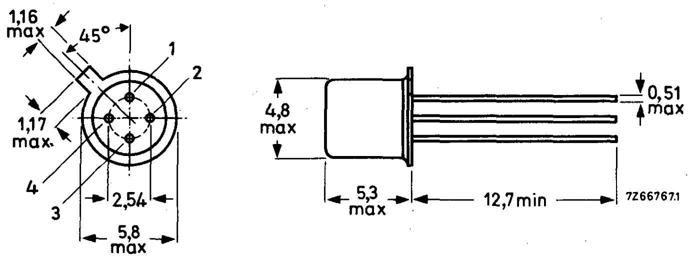
   R_e (h_i) etc. ... for the real part
   I_m (h_i) etc. ... for the imaginary part

PACKAGE OUTLINES

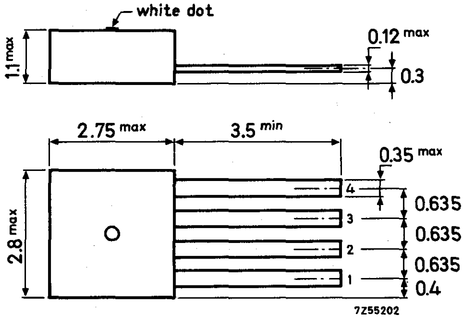
METAL TO-72 (SOT-18/13)



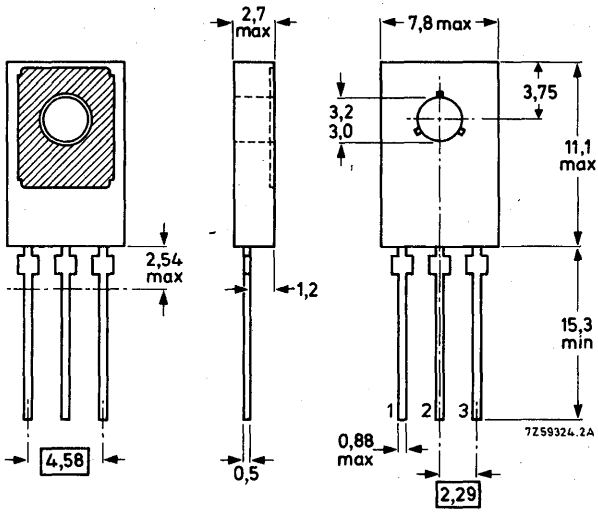
METAL TO-72 (SOT-18/17)



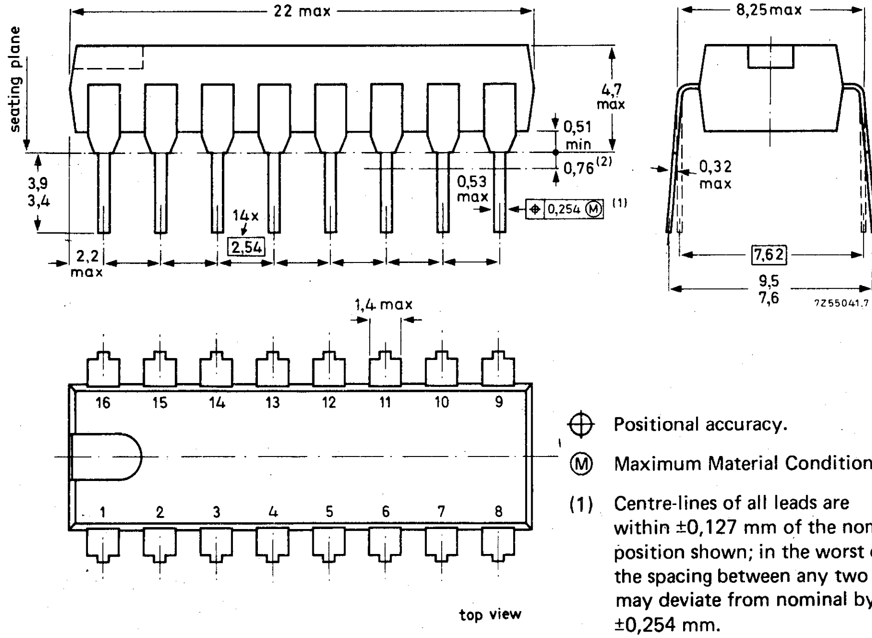
PLASTIC (SOT-20)



PLASTIC TO-126 (SOT-32)



16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

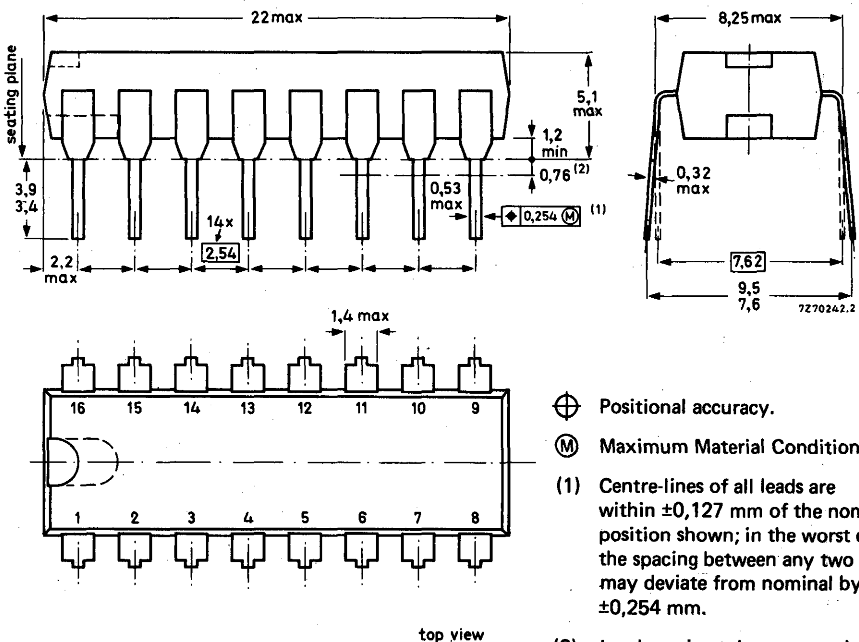
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC POWER (SOT-38M and N)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

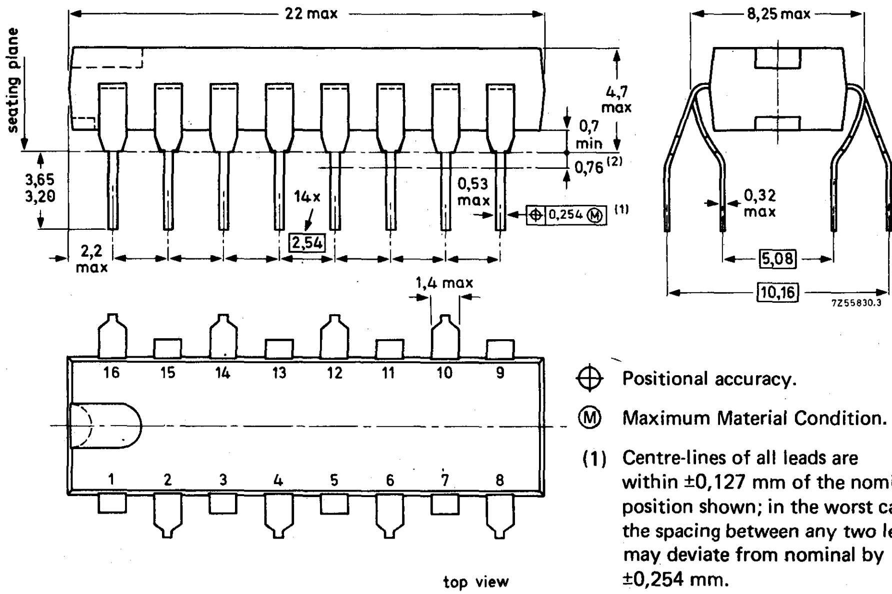
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD QUADRUPLE IN-LINE; PLASTIC (SOT-58)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

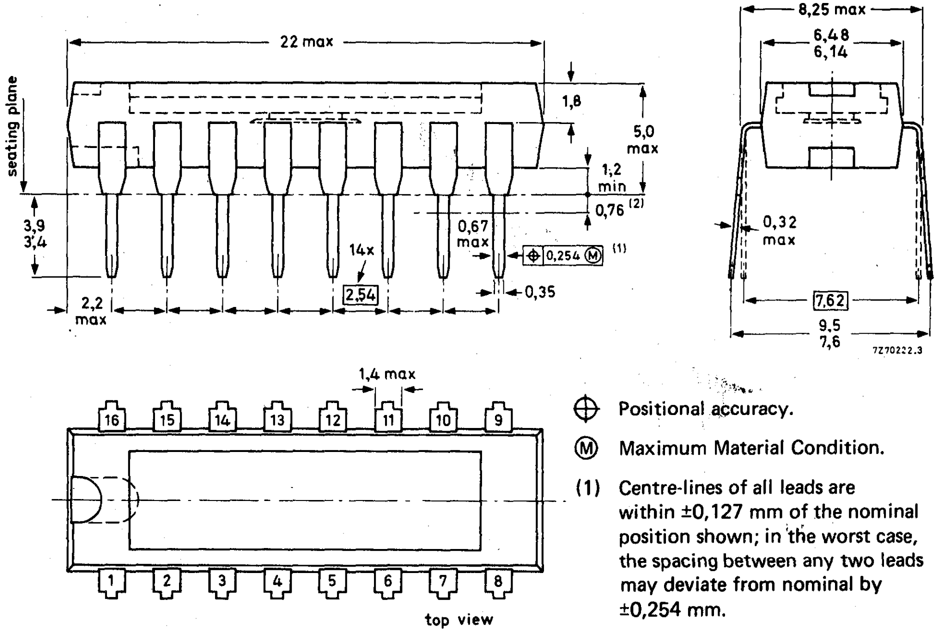
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC POWER (SOT-69B, D)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

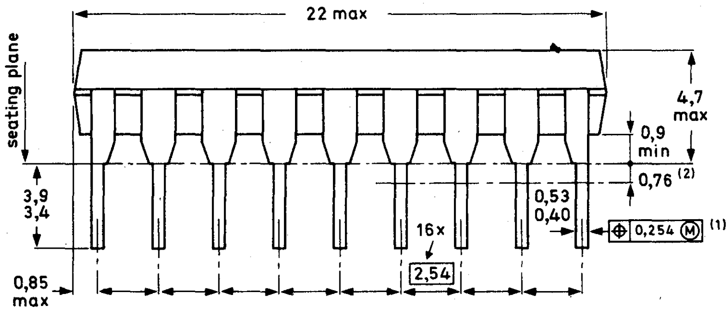
2. By dip or wave

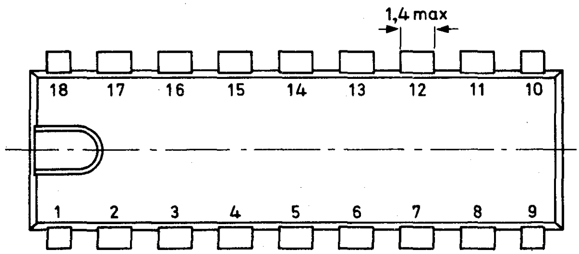
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

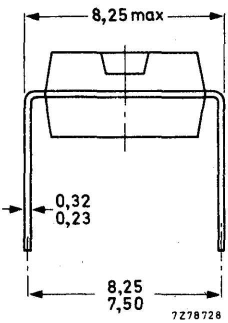
The same precautions and limits apply as in (1) above.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102C)





top view



side view

⊕ Positional accuracy.

(M) Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

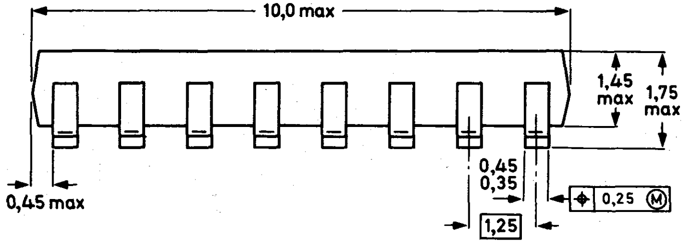
(2) Lead spacing tolerances apply from seating plane to the line indicated.

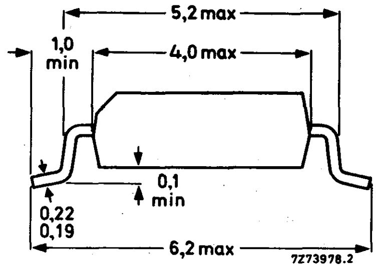
Dimensions in mm

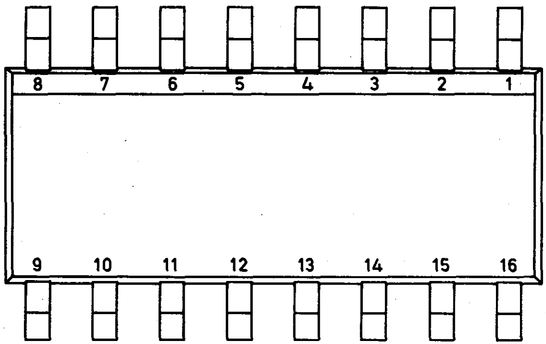
SOLDERING

See SOT-69B, D, for example.

16-LEAD FLAT PACK; PLASTIC (SO-16; SOT-109A)







top view

Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

See next page.

SOLDERING

The reflow solder technique

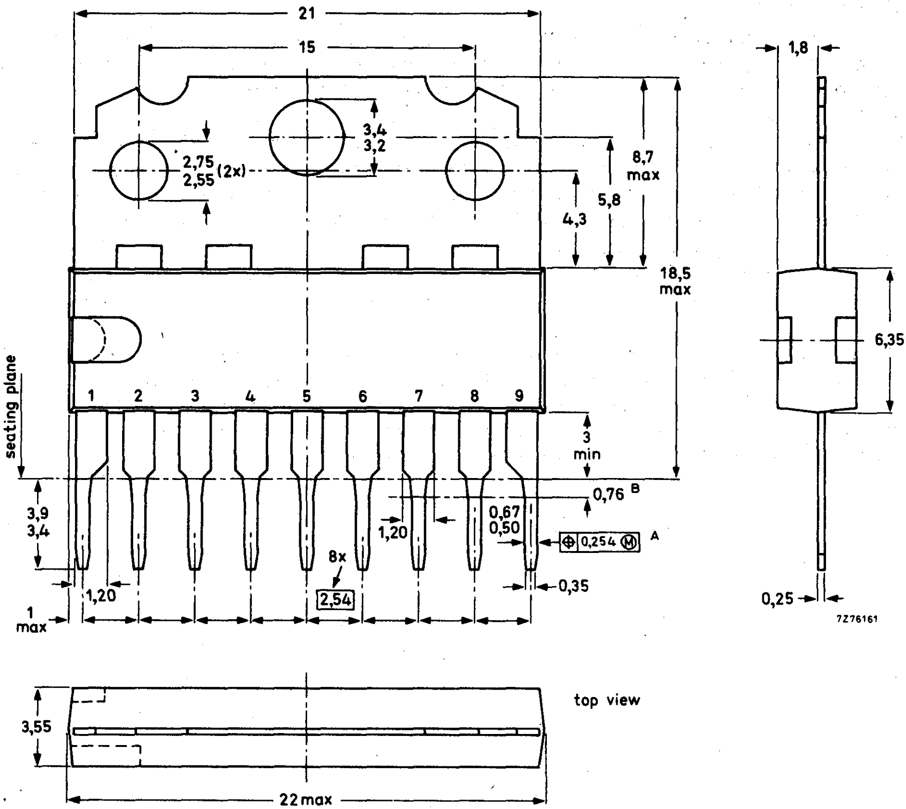
The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 $^{\circ}$C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-110A)



Dimensions in mm

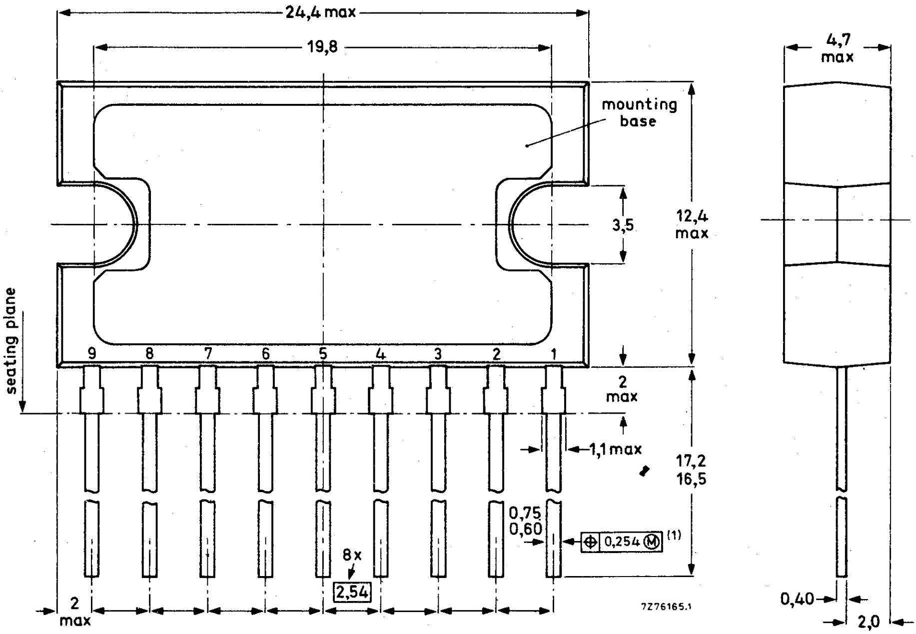
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

9-LEAD SINGLE IN-LINE; PLASTIC POWER (SOT-131B)



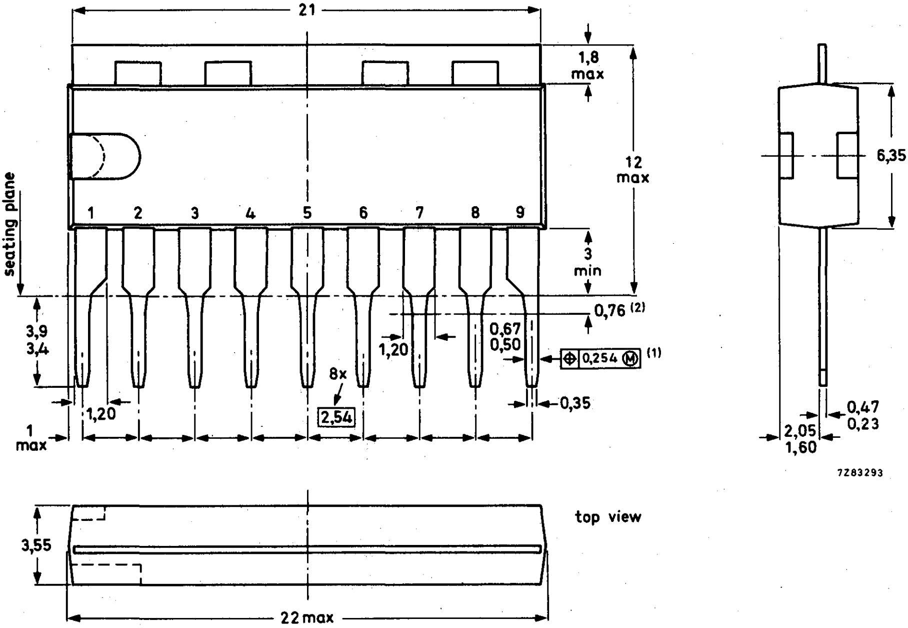
Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

9-LEAD SINGLE IN-LINE; PLASTIC (SOT-142)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

INTRODUCTION

NTRODUCTION TO BIPOLAR ICs FOR RADIO AND AUDIO EQUIPMENT

Three main fields of application are shown in the following block diagram concepts. These are:

- portable radio recorder,
- hi-fi,
- car radio player.

'Concept' here means: a total IC programme is available for a system, in which the ICs are perfectly matched to each other during the design phase. All ICs can also be used as solitary types in combination with other components.

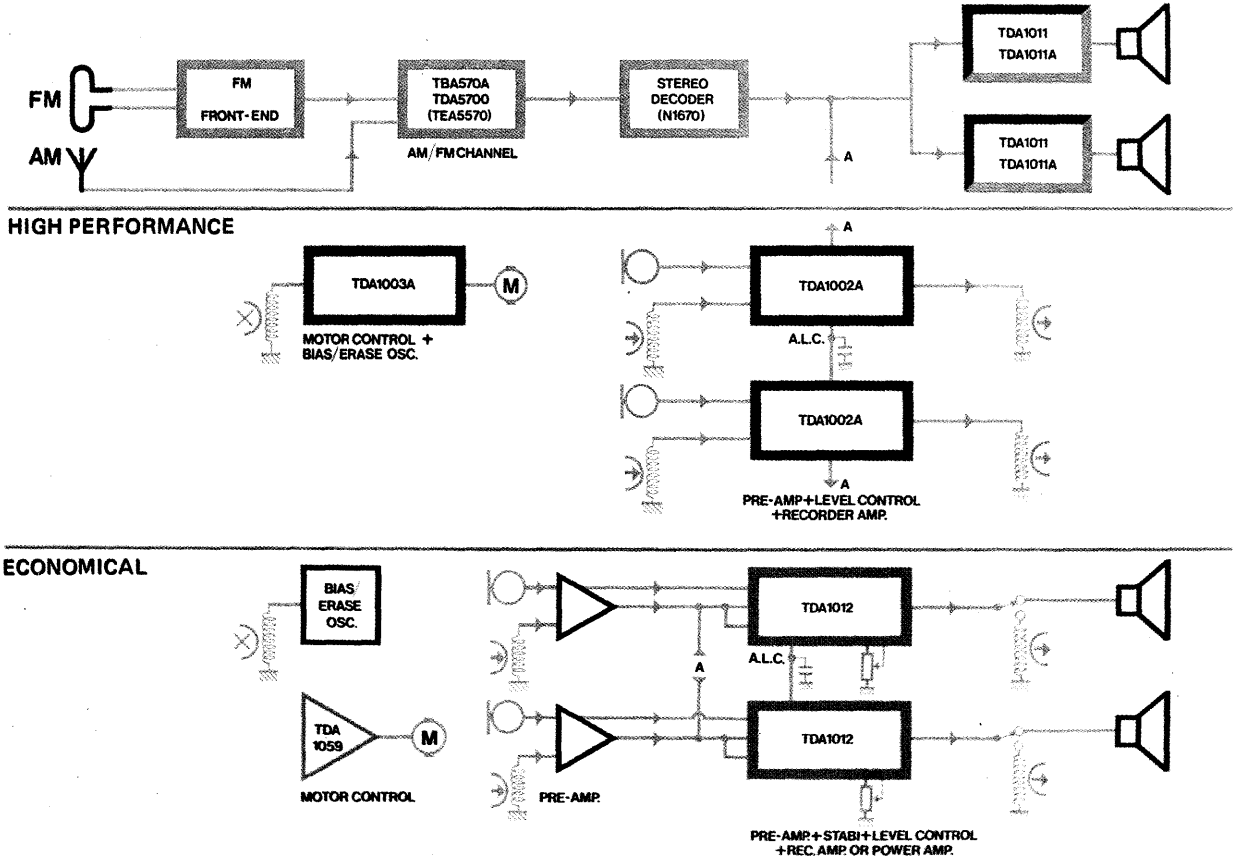
The various concept types are chosen as a function of the required compromise between performance and cost.

Two concepts are given for portable radio recorders:

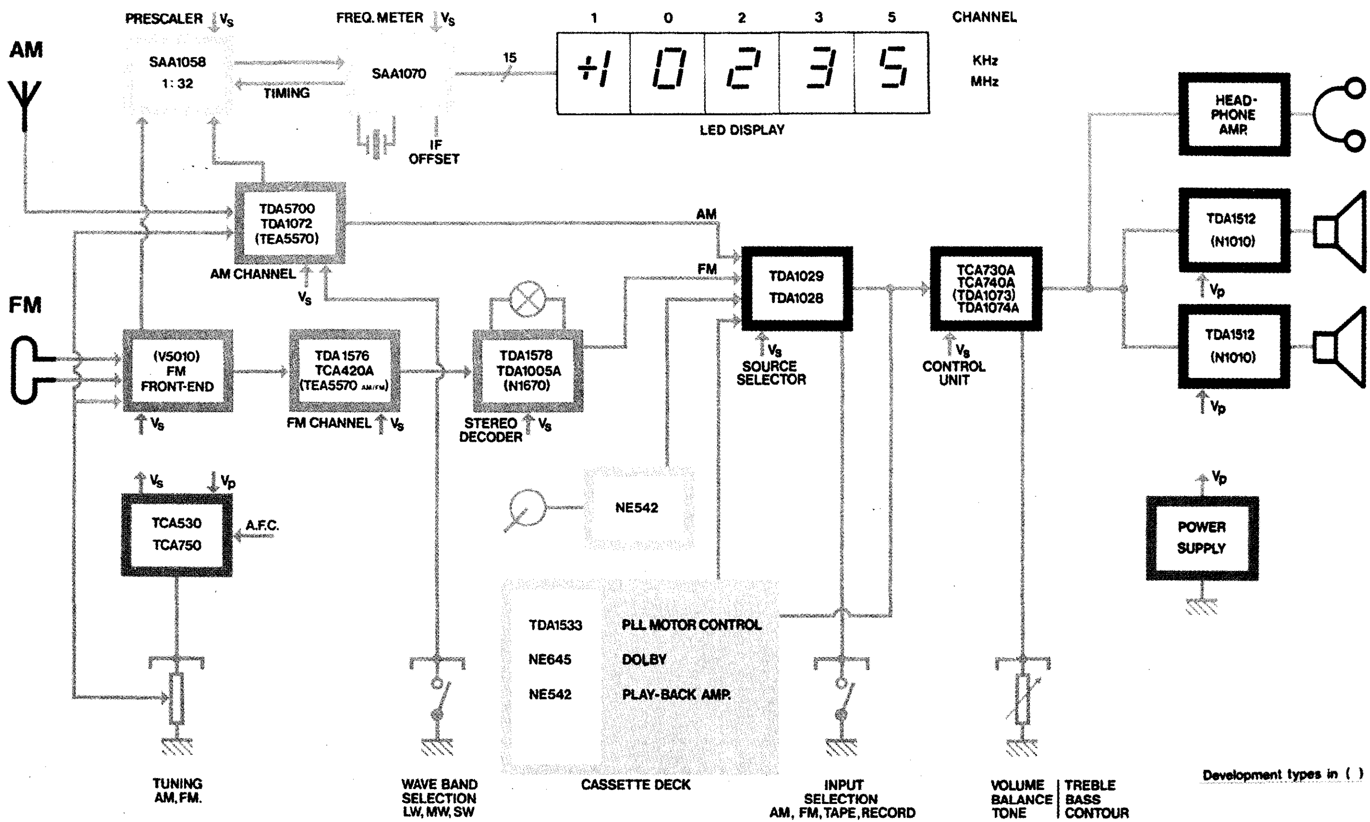
high performance,
economical.

Some types in the IC programme are still in the development stage at the date of publication of this data handbook. These type numbers are given in brackets in the block diagrams (some of them still have the 'in-house' development number).

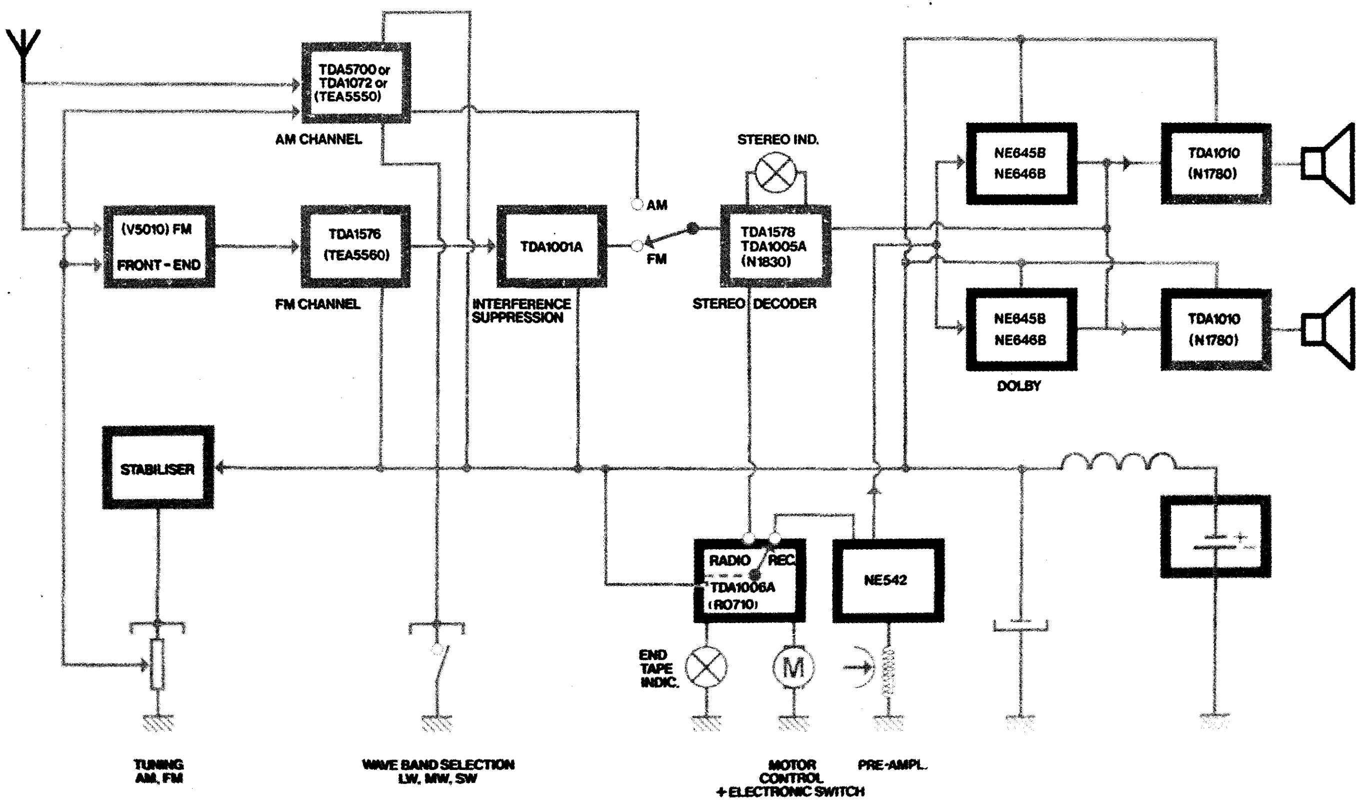
PORTABLE RADIO RECORDER CONCEPT



HI-FI CONCEPT



CAR RADIO PLAYER CONCEPT



DEVICE DATA

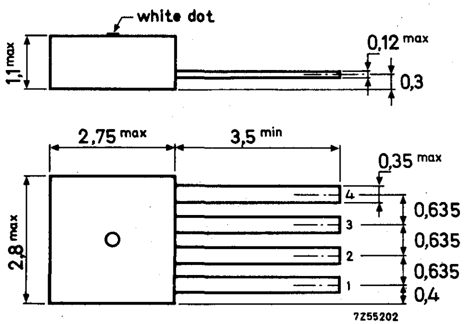
INTEGRATED AMPLIFIER
for use in ear hearing aids

Monolithic integrated circuit amplifier in a plastic envelope, primarily intended for use in ear hearing aids.

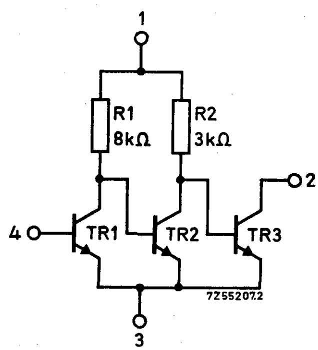
QUICK REFERENCE DATA				
For meaning of symbols see test circuit on page 3				
Supply voltage	V_{1-3}	max.	5	V
Supply current	I_2	max.	5	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	25	mW
The following data are measured in test circuit on page 3				
Total supply current	I_{tot}	typ.	1	mA
Transducer gain	G_{tr}	>	77	dB
		typ.	85	dB
Output power at d_{tot} = 10%	P_o	>	0,2	mW
Cut-off frequency (−3 dB)	f_c	>	20	kHz

PACKAGE OUTLINE (Dimensions in mm)

SOT-20



CIRCUIT DIAGRAM



The sealing of the plastic envelope withstands the accelerated damp heat test of IEC recommendation 68-2 (test D, severity IV, 6 cycles).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

For meaning of symbols test circuit on page 3.

Voltages

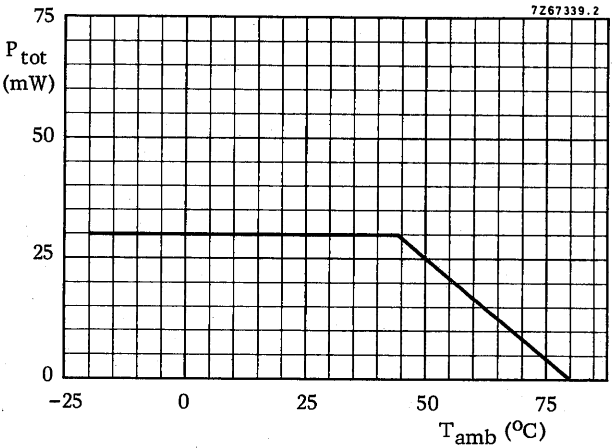
Supply voltage	V_{1-3}	max.	5	V
Output voltage	V_{2-3}	max.	5	V [1]
Input voltage	$-V_{4-3}$	max.	5	V

Currents

Output current	I_2	max.	5	mA
Input current	I_4	max.	5	mA

Power dissipation

Power derating curve



Temperatures

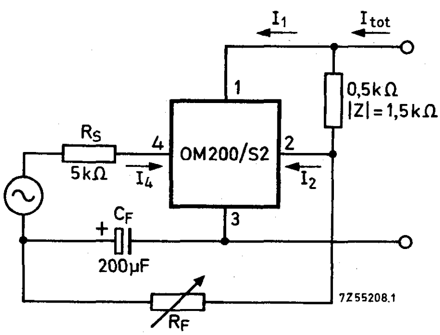
Storage temperature	T_{stg}	−20 to +80	°C
Ambient temperature (see derating curve above)	T_{amb}	−20 to +80	°C

1) This value may be exceeded during inductive switch-off for transient energies < 10 μWs.

CHARACTERISTICS at $V_{1-3} = 1,3$ V; $I_2 = 0,7$ mA and $T_{amb} = 25$ °C unless otherwise specified

Supply currents (no signal)	I_{tot}	<	1, 1	mA	
	I_1	typ.	0, 30	mA	
Transducer gain at f = 1 kHz	G_{tr}	>	77	dB	1)
		typ.	85	dB	
Total distortion at f = 1 kHz					
P_o = 100 μW	d_{tot}	typ.	4	%	
		<	6	%	
P_o = 200 μW	d_{tot}	<	10	%	
Noise figure at R_S = 5 kΩ					
B = 400 to 3200 Hz	F	typ.	2, 5	dB	
		<	6	dB	2)
Cut-off frequency (−3 dB)	f_c	>	20	kHz	
Value of R_F to adjust I_2 at 0, 7 mA	R_F	170 to 1000		kΩ	
		typ.	400	kΩ	

Test circuit



Note

I_2 = 0, 7 mA; adjusted by means of R_F
V_{1-3} = 1, 3 V; T_{amb} = 25 °C

1) The transducer gain is defined as the ratio of the output power in the load |Z| = 1,5 kΩ and the available input power of the source with R_S = 5 kΩ.

$$G_{tr} = \frac{P_o}{V_i^2/4\,R_S}$$

2) Due to special processing and pre-measuring, the flutter-noise level is extremely low.

SOLDERING RECOMMENDATIONS

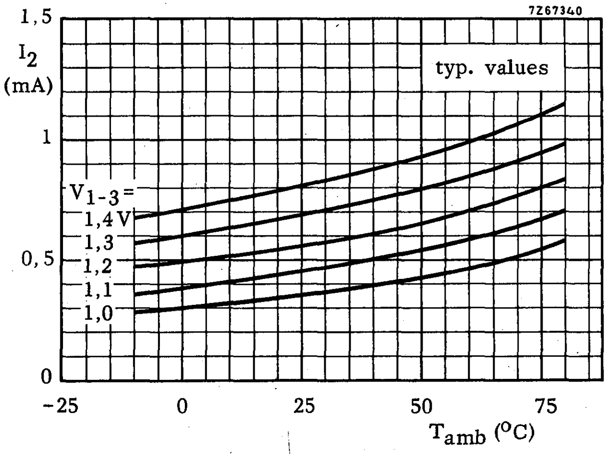
1. Iron soldering

   At a maximum iron temperature of 300 °C the maximum permissible soldering time is 3 seconds, provided the solder spot is at least 0,5 mm from the seal and the leads are not soldered at the same time. Soldering in immediate subsequence is allowed.

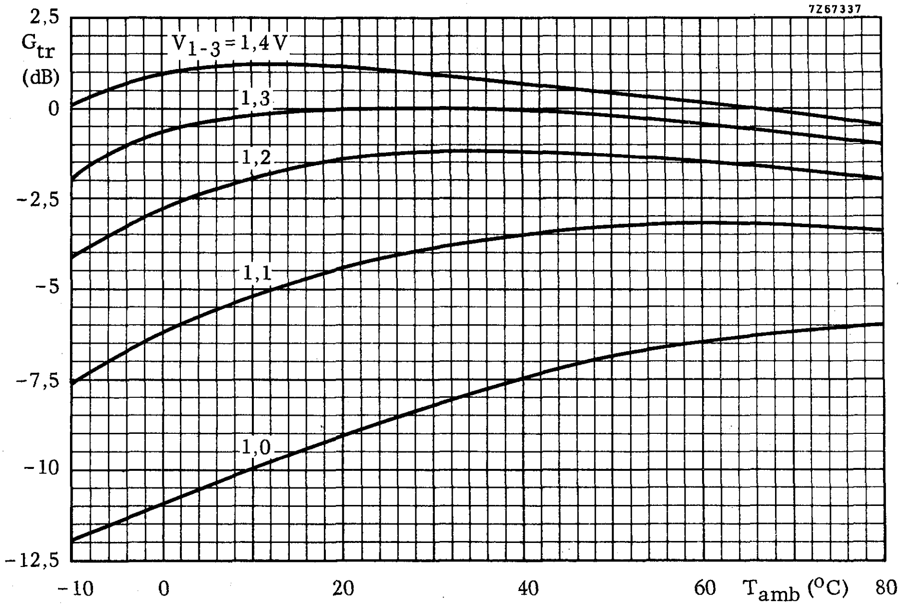
2. Dipsoldering

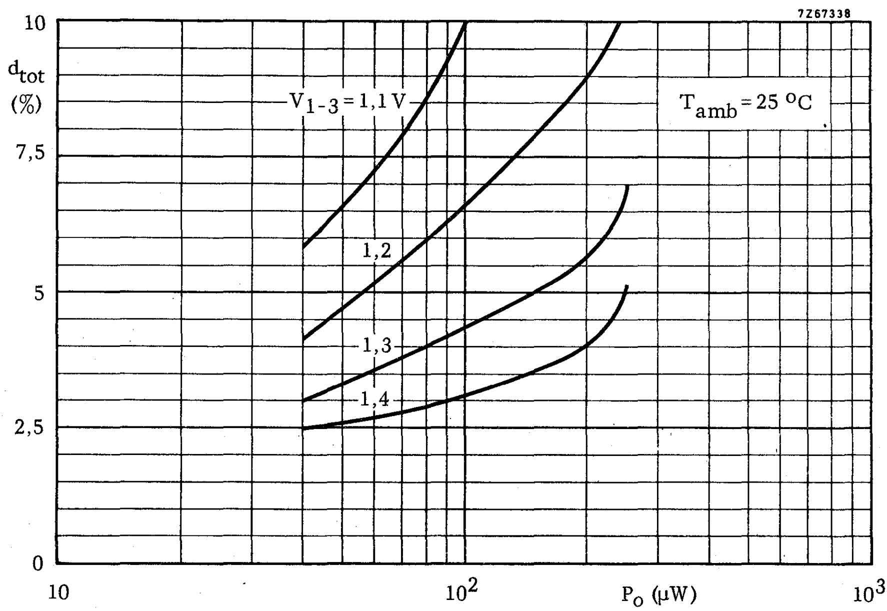
   At a maximum solder temperature of 250 °C the maximum permissible soldering time is 3 seconds, provided the soldered spot is at least 0,5 mm from the seal.

CHARACTERISTICS



The graph applies to test circuit on page 3


7Z67337
2,5
G_{tr}
(dB)
0
−2,5
−5
−7,5
−10
−12,5
V_{1-3} = 1,4 V
1,3
1,2
1,1
1,0
−10
0
20
40
60
T_{amb} (°C)
80


7Z67338
10
d_{tot}
(%)
7,5
5
2,5
0
V_{1-3} = 1,1 V
1,2
1,3
1,4
T_{amb} = 25 °C
10
10^2
P_o (μW)
10^3

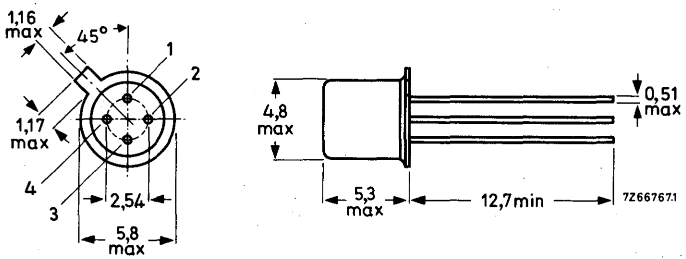
LOW-LEVEL AMPLIFIER

The TAA263 is a semiconductor integrated amplifier in a 4-lead TO-72 metal envelope. It comprises a three-stage, direct coupled low-level amplifier for use from d.c. up to frequencies of 600 kHz.

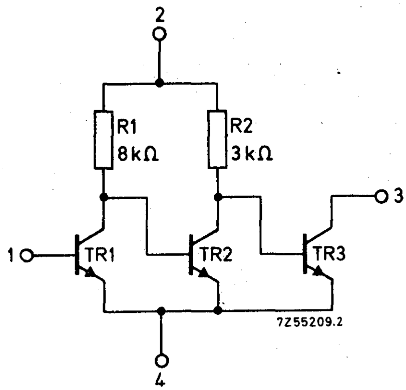
QUICK REFERENCE DATA				
Supply voltage	V_B	max.	8	V
Output voltage	V_{3-4}	max.	7	V
Output current	I_3	max.	25	mA
Transducer gain at P_o = 10 mW				
R_L = 150 Ω; f = 1 kHz	G_{tr}	typ.	77	dB
Operating ambient temperature	T_{amb}		−20 to +100	°C

PACKAGE OUTLINE Dimensions in mm

TO-72 (SOT-18/17)



CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

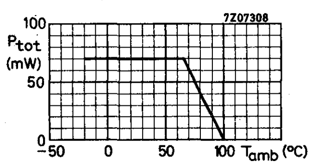
Supply voltage	V_B	max.	8	V
Output voltage	V_{3-4}	max.	7	V
Input voltage	$-V_{1-4}$	max.	5	V

Currents

Output current	I_3	max.	25	mA
Input current	I_1	max.	10	mA

Power dissipation

Total power dissipation up to T_{amb} = 65 °C	P_{tot}	max.	70	mW



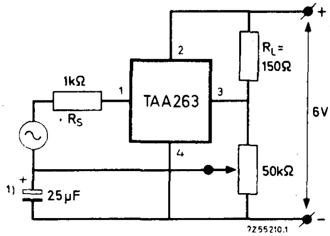
Temperatures

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature (see derating curve above)	T_{amb}	−20 to +100	°C

CHARACTERISTICS

T_{amb} = 25 °C

Test circuit:



Currents				
Output current	I_3	typ.	12	mA
Total current drain (no signal)	I_2+I_3	<	16	mA
Over-all small signal current gain				
f = 1 kHz	$h_{f\ tot}$	typ.	5.10^5	
Transducer gain				
f = 1 kHz; P_o = 10 mW	G_{tr}	>	70	dB
		typ.	77	dB
Output power at f = 1 kHz; d_{tot} = 10%	P_o	>	10	mW
d_{tot} = 5%	P_o	>	8	mW
Noise figure				
f = 400 Hz to 6 kHz	F	typ.	5	dB
		<	10	dB
f = 450 kHz; Δf = 5 kHz	F	typ.	2.7	dB

1) $Z \leqslant 10\ \Omega$ at f = 1 kHz

CHARACTERISTICS (continued) $T_{amb} = 25\ ^{o}C$

y parameters (point 4 common connection)

$V_B = 6$ V; $I_3 = 3$ mA; $V_{3-4} = 4.2$ V

f = 1 kHz				
Input admittance	$y_i = g_i$	typ.	20	$\mu\Omega^{-1}$
Transfer admittance	$y_f = g_f$	typ.	11	Ω^{-1}
Output admittance	$y_o = g_o$	typ.	60	$\mu\Omega^{-1}$
f = 450 kHz				
Input conductance	g_i	typ.	15	$\mu\Omega^{-1}$
Input capacitance	C_i	typ.	14	pF
Transfer admittance	$\lvert y_f \rvert$	typ.	9.4	Ω^{-1}
Phase angle of transfer admittance	φ_f	typ.	125^o	
Output conductance	g_o	typ.	20	$\mu\Omega^{-1}$
Output capacitance	C_o	typ.	13	pF

INTEGRATED MOST AMPLIFIER

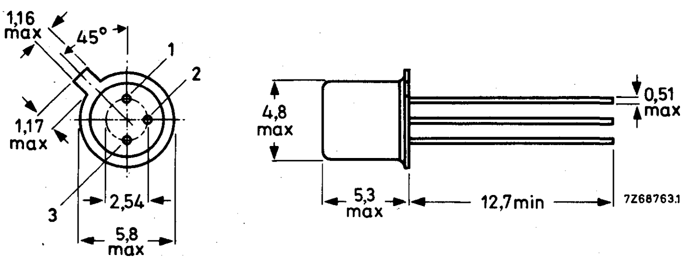
The TAA320 is a silicon monolithic integrated circuit, consisting of a MOS transistor and an n-p-n transistor in a TO-18 metal envelope.
The device is primarily intended for audio amplifiers with a very high input resistance (e.g. for crystal pick-ups).
Besides this application the TAA320 is also suitable for other applications where a high input resistance is required, like impedance converters, timing circuits, microphone-amplifiers, etc.

QUICK REFERENCE DATA				
Drain-source voltage (V_{GS} = 0)	$-V_{DSS}$	max.	20	V
Drain current	$-I_D$	max.	25	mA
Gate-source voltage $-I_D$ = 10 mA; $-V_{DS}$ = 10 V	$-V_{GS}$	typ.	11	V
Gate-source resistance $-V_{GS}$ up to 20 V; T_j up to 125 °C	r_{GS}	>	100	GΩ
Transfer admittance at f = 1 kHz $-I_D$ = 10 mA; $-V_{DS}$ = 10 V	$\|y_{fs}\|$	typ.	75	$m\Omega^{-1}$

PACKAGE OUTLINE

TO-18 (SOT-18/13)

Dimensions in mm

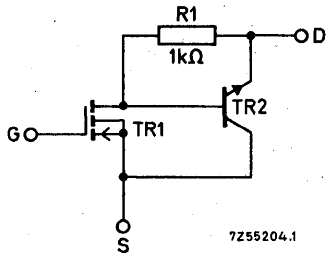


1 = drain
2 = gate
3 = source

Source connected to the case

Accessories supplied on request: 56246, 56263

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Drain-source voltage (V_{GS} = 0)	$-V_{DSS}$	max.	20	V
Gate-source voltage (I_D = 0)	$-V_{GSO}$	max.	20	V
Non repetitive peak gate-source voltage ($t \leq 10$ ms)	$-V_{GSM}$	max.	100	V

Current

Drain current	$-I_D$	max.	25	mA

Power dissipation

Total power dissipation up to T_{amb} = 25 ^oC	P_{tot}	max.	200	mW

Temperatures

Storage temperature	T_{stg}	−55 to +125	^oC
Operating ambient temperature (see derating curve on page 8)	T_{amb}	−20 to +125	^oC

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	0.5	$^oC/mW$

CHARACTERISTICS T_j = 25 °C unless otherwise specified

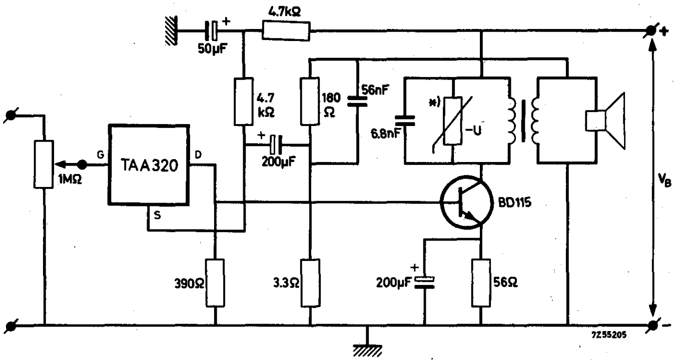
Drain current			
$-V_{DS}$ = 20 V; V_{GS} = 0	$-I_{DSS}$	typ. 5 < 1	nA µA
Gate-source voltage [1]			
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V	$-V_{GS}$	typ. 11 9 to 14	V V
Gate-source resistance			
$-V_{GS}$ up to 20 V; T_j up to 125 °C	r_{GS}	> 100	GΩ
Equivalent noise voltage			
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V B = 50 Hz to 15 kHz	v_n	typ. 25	µV
y parameters at f = 1 kHz			
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V			
Transfer admittance	$\|y_{fs}\|$	typ. 75 40 to 120	$m\Omega^{-1}$ $m\Omega^{-1}$
Input capacitance	C_{is}	typ. 8	pF
Feedback capacitance	$-C_{rs}$	typ. 1.5	pF
Output conductance	g_{os}	typ. 0.65	$m\Omega^{-1}$

NOTE

To exclude the possibility of damage to the gate oxide layer by an electrostatic charge building up on the high resistance gate electrode, the leads of the device have been short circuited by a clip. The clip has been arranged so that it need not be removed until the device has been mounted in the circuit.

1) $-V_{GS}$ decreases about 6 mV/°C with increasing ambient temperature at a constant $-I_D$.

APPLICATION INFORMATION 2 W audio amplifier with TAA320 and BD115



* The voltage dependent resistor (2322 552 03381) suppresses voltage transients that might otherwise exceed the safe operating limits of the BD115.

Supply voltage	V_B	=	100	V
Collector current of BD115	I_C	typ.	50	mA
Drain current of TAA320	$-I_D$	typ.	9.5	mA
Primary d.c. resistance of output transformer			140	Ω
Primary inductance of output transformer			2.7	H
A.C. collector load for BD115			1.8	kΩ

Performance at f = 1 kHz; feedback = 16 dB

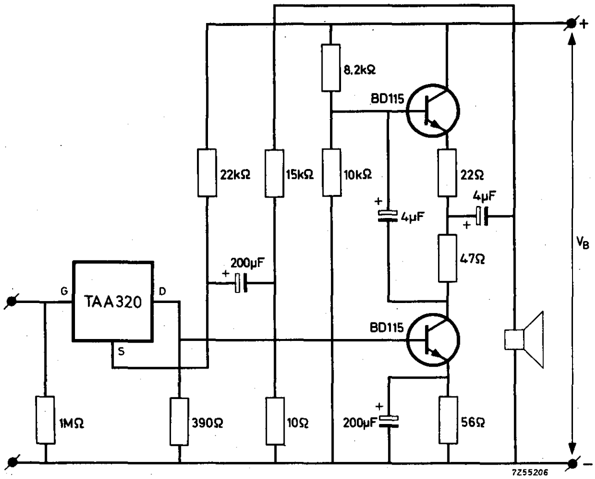
Output power at d_{tot} = 10% (on primary of the output transformer)	P_o	typ.	2.6	W
Input voltage for P_o = 50 mW	$V_{i(rms)}$	typ.	13.5	mV
Input voltage for P_o = 2 W	$V_{i(rms)}$	typ.	86	mV
Total distortion at P_o = 2 W	d_{tot}	typ.	3.6	%
Minimum frequency response (−3 dB)			60 Hz to 20	kHz
Signal-noise ratio at P_o = 2 W		typ.	73	dB

Mounting instruction for BD115

Proper continuous operation is ensured up to T_{amb} = 50 °C, provided the BD115 is directly mounted on a 1.5 mm blackened Al. heatsink of 30 cm^2 with a clamping washer of type 56218.
If the transistor is mounted on a heatsink with a mica washer, the heatsink should have an area of 50 cm^2.
Recommended diameter of hole in heatsink: 7.7 mm.

APPLICATION INFORMATION (continued)

4 W audio amplifier with TAA320 and 2 transistors of type BD115.

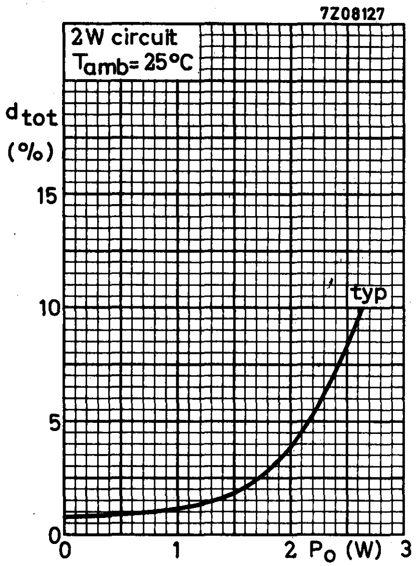


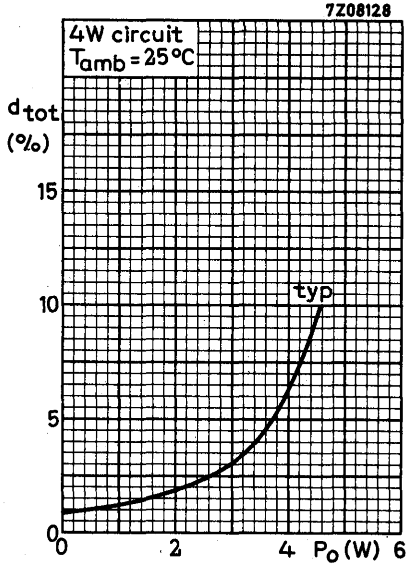
Supply voltage	V_B	=	200	V
Collector current of a BD115	I_C	typ.	52	mA
Drain current of TAA320	$-I_D$	typ.	8.6	mA

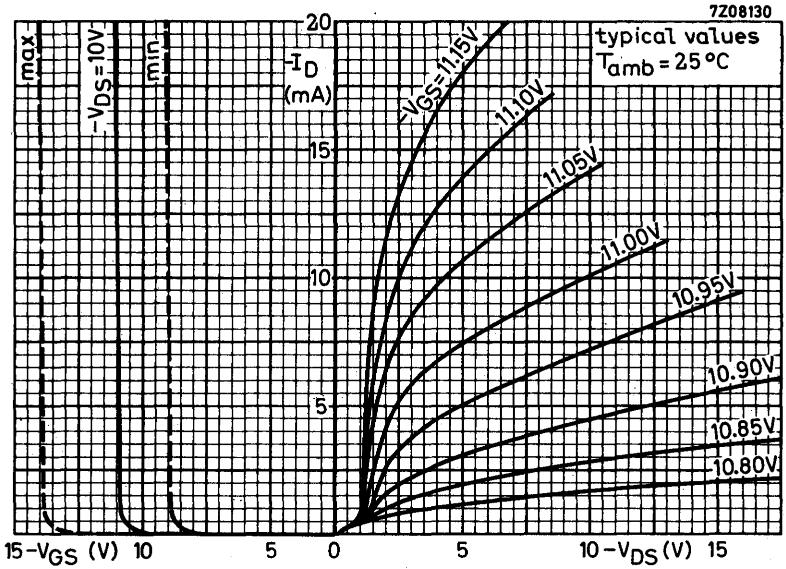
Performance at f = 1 kHz; feedback = 12 dB

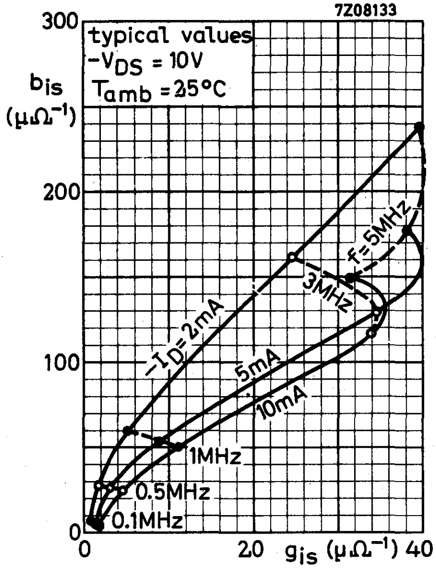
Output power at d_{tot} = 10%	P_o	typ.	4.5	W
Input voltage for P_o = 50 mW	$V_{i(rms)}$	typ.	7.5	mV
Input voltage for P_o = 4 W	$V_{i(rms)}$	typ.	67	mV
Total distortion at P_o = 4 W	d_{tot}	typ.	6	%
Minimum frequency response (–3 dB)			50 Hz to 20	kHz
Signal-noise ratio at P_o = 4 W		typ.	73	dB

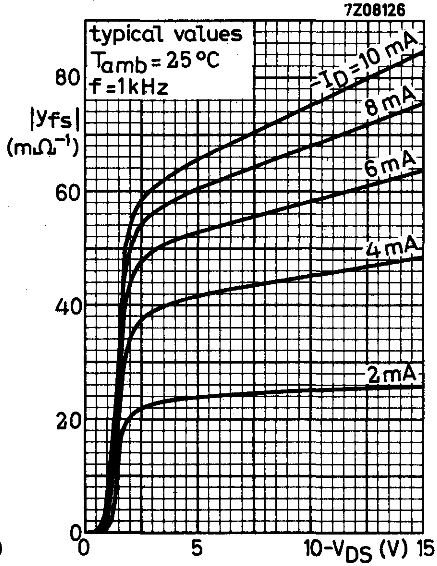
Mounting instruction for BD115 see page 4

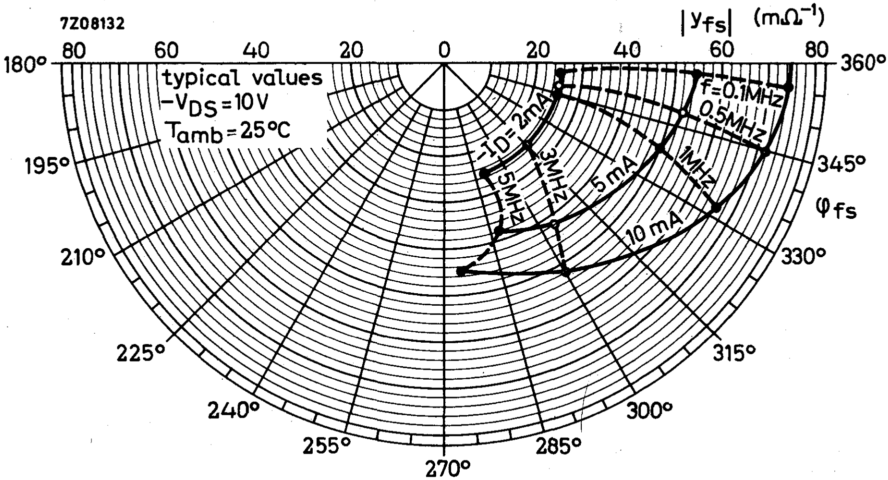

7Z08127
2W circuit
Tamb= 25°C
dtot
(%)
15
10
5
0
typ
0
1
2 Po (W) 3

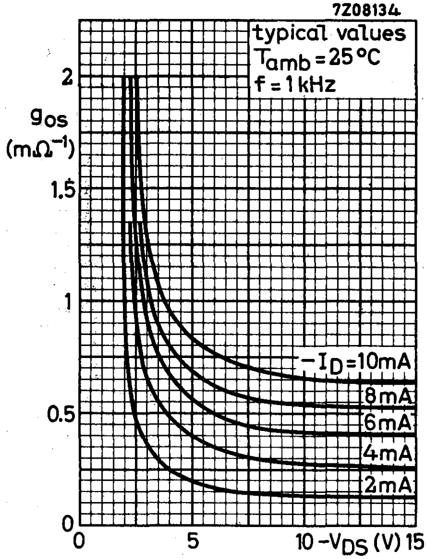

7Z08128
4W circuit
Tamb = 25°C
dtot
(%)
15
10
5
0
typ
0
2
4 Po (W) 6

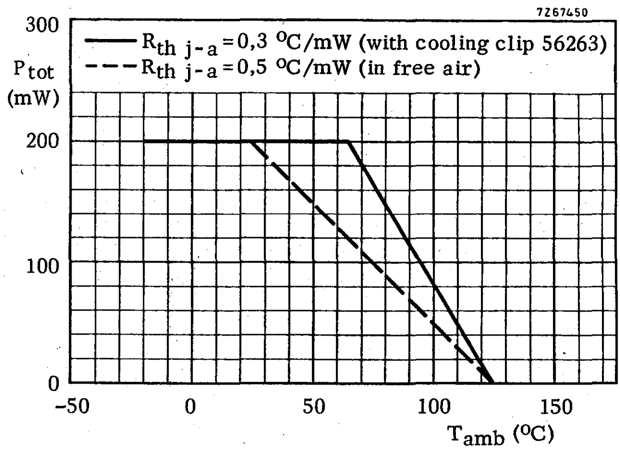

7Z08130
typical values
Tamb = 25 °C
-ID
(mA)
20
15
10
5
max
-VDS=10V
min
-VGS=11.15V
11.10V
11.05V
11.00V
10.95V
10.90V
10.85V
10.80V
15 -VGS (V) 10
5
0
5
10 -VDS (V) 15

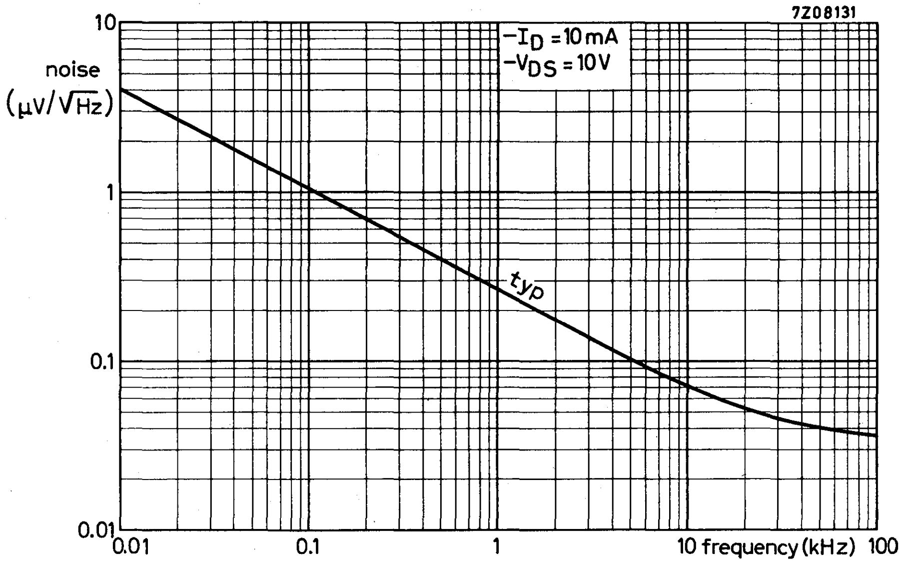

7Z08133
typical values
$-V_{DS}$ = 10V
T_{amb} = 25°C
b_{is} ($\mu\Omega^{-1}$)
300
200
100
0
0
20
g_{is} ($\mu\Omega^{-1}$) 40
$-I_D$=2mA
5mA
10mA
f=5MHz
3MHz
1MHz
0.5MHz
0.1MHz


7Z08126
typical values
T_{amb} = 25°C
f = 1kHz
$|y_{fs}|$ ($m\Omega^{-1}$)
80
60
40
20
0
0
5
10
$-V_{DS}$ (V) 15
$-I_D$=10 mA
8 mA
6 mA
4 mA
2 mA


7Z08132
$|y_{fs}|$ ($m\Omega^{-1}$)
80
60
40
20
0
20
40
60
80
180°
360°
195°
345°
210°
330°
225°
315°
240°
300°
255°
285°
270°
φ_{fs}
typical values
$-V_{DS}$ = 10 V
T_{amb} = 25°C
$-I_D$=2mA
5 mA
10 mA
f=0.1MHz
0.5MHz
1MHz
3MHz
5MHz


7Z08134
typical values
T_{amb} = 25 °C
f = 1 kHz
g_{os}
(mΩ^{-1})
2
1.5
1
0.5
0
$-I_D$ = 10mA
8mA
6mA
4mA
2mA
0
5
10 $-V_{DS}$ (V) 15


7Z67450
300
P_{tot}
(mW)
200
100
0
$R_{th\ j-a}$ = 0,3 °C/mW (with cooling clip 56263)
$R_{th\ j-a}$ = 0,5 °C/mW (in free air)
−50
0
50
100
150
T_{amb} (°C)


7Z08131
10
noise
(μV/√Hz)
1
0.1
0.01
−I_D = 10 mA
−V_DS = 10 V
typ
0.01
0.1
1
10 frequency (kHz) 100

INTEGRATED MOST LEVEL SENSOR

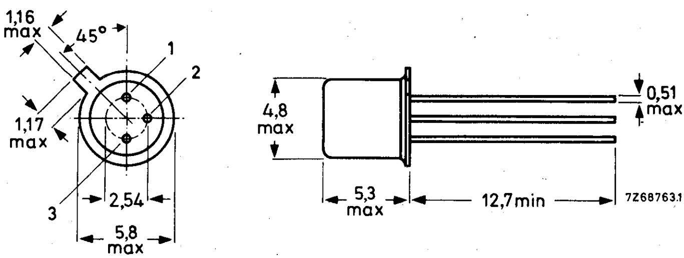
The TAA320A is a silicon monolithic integrated circuit, consisting of a p-channel enhancement type MOS transistor and an n-p-n transistor, in a TO-18 metal envelope. The device is intended for level sensors with a very high input resistance (e.g. timing circuits, thermostats, liquid level sensors, flame control circuits).

QUICK REFERENCE DATA					
Drain-source voltage (V_{GS} = 0)		$-V_{DSS}$	max.	20	V
Drain current		$-I_D$	max.	60	mA
Gate-source voltage [1]					
$-I_D$ = 10 mA; $-V_{DS}$ = 10 V	group 1:	$-V_{GS}$	typ.	10,6	V
				10,0 to 11,2	V
	group 2:	$-V_{GS}$	typ.	11,3	V
				10,7 to 11,9	V
	group 3:	$-V_{GS}$	typ.	12,0	V
				11,4 to 12,6	V
	group 4:	$-V_{GS}$	typ.	12,7	V
				12,1 to 13,3	V
Gate cut-off current at T_{amb} = 25 °C					
$-V_{GS}$ = 20 V; I_D = 0		$-I_{GSO}$	typ.	1	pA
$-V_{GS}$ = 20 V; V_{DS} = 0		$-I_{GSS}$	typ.	1	pA

PACKAGE OUTLINE

Dimensions in mm

TO-18 (SOT-18/13)



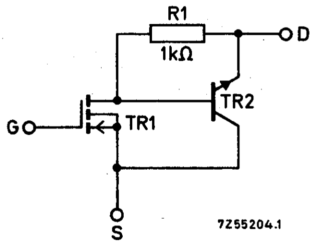
1 = drain
2 = gate
3 = source

source connected to the case

Accessories supplied on request: 56246; 56263

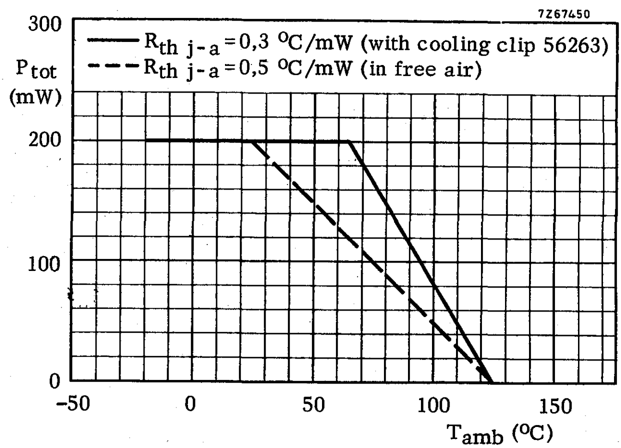
[1]) For explanation of the group codefication see note b on page 3.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage (V_{GS} = 0)	$-V_{DSS}$	max.	20	V
Gate-source voltage (I_D = 0)	$-V_{GSO}$	max.	20	V
Non-repetitive peak gate-source voltage ($t \leq 10$ ms)	$\pm V_{GSM}$	max.	100	V
Current				
Drain current	$-I_D$	max.	60	mA
Peak drain current (t < 200 ms; δ 0,001)	$-I_{DM}$	max.	100	mA
Temperatures				
Storage temperature	T_{stg}		−65 to +125	°C
Operating ambient temperature (see curve below)	T_{amb}		−20 to +125	°C



CHARACTERISTICS $T_j = 25\ ^{o}C$ unless otherwise specified

Drain current					
$-V_{DS} = 20\ V;\ V_{GS} = 0$		$-I_{DSS}$	typ.	5	nA
			<	1	μA
Drain-source voltage [1]					
$-I_D = 10\ mA;\ -V_{GS} = 20\ V$		$-V_{DS}$	<	1	V
$-I_D = 60\ mA;\ -V_{GS} = 20\ V$		$-V_{DS}$	<	1,5	V
Gate-source voltage (see note b)					
$-I_D = 10\ mA;\ -V_{DS} = 10\ V$	group 1:	$-V_{GS}$	typ.	10,6	V
			10,0 to	11,2	V
	group 2:	$-V_{GS}$	typ.	11,3	V
			10,7 to	11,9	V
	group 3:	$-V_{GS}$	typ.	12,0	V
			11,4 to	12,6	V
	group 4:	$-V_{GS}$	typ.	12,7	V
			12,1 to	13,3	V
Gate cut-off current					
$-V_{GS} = 20\ V;\ I_D = 0$		$-I_{GSO}$	typ.	1	pA [2]
$-V_{GS} = 20\ V;\ V_{DS} = 0$		$-I_{GSS}$	typ.	1	pA [2]

NOTES

a. The leads are short-circuited by a clip to protect the oxide layer against damage due to accumulation (or build-up) of electrostatic charge on the high resistance gate electrode. The clip should not be removed until after the device is mounted.

b. As a service to the customer the $-V_{GS}$ group to which a device belongs is identified by a numerical suffix (1, 2, 3 or 4), however, individual groups cannot be ordered separately.

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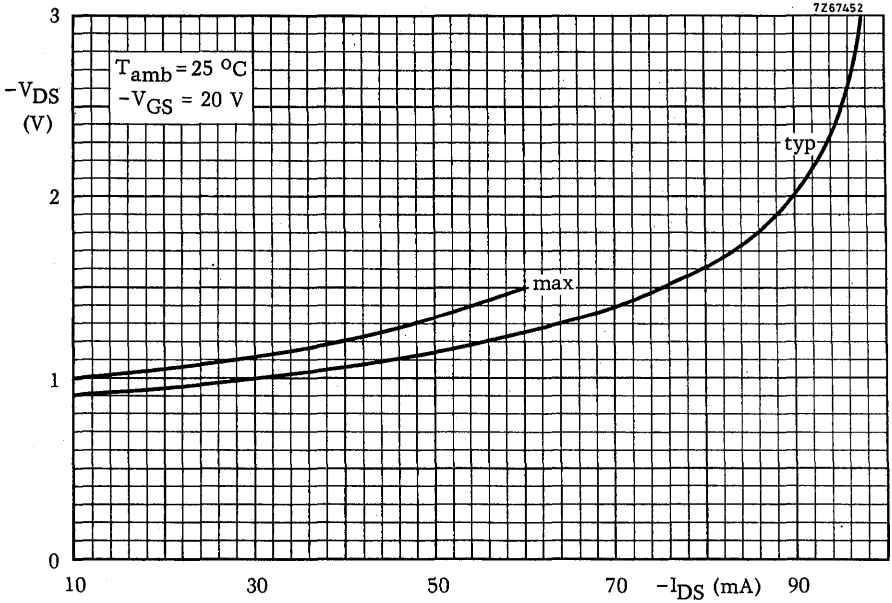
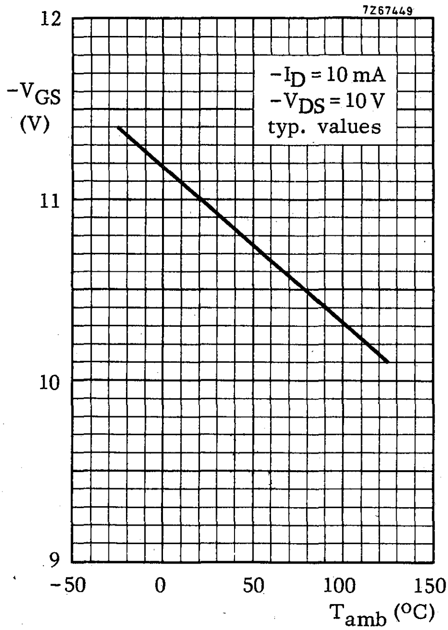
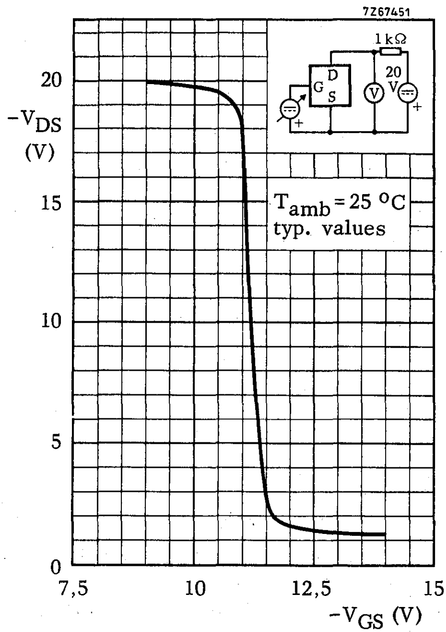
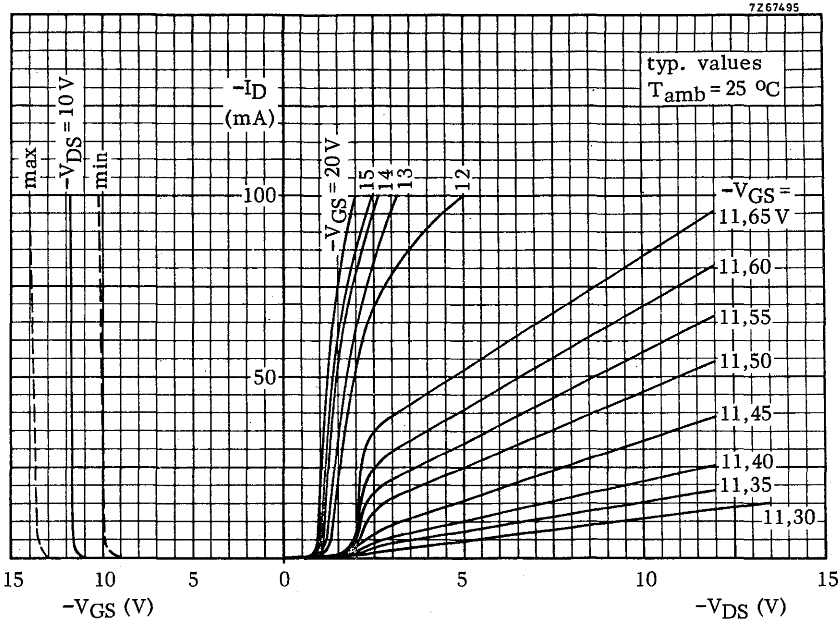
1. See also upper graph on page 4.
2. Being dependent on handling and ambient humidity, the quoted value applies only up to the time of shipping.
   Efficient drying treatment is advised before the device is mounted, provided the application requires this low current.


7Z67452
T_{amb} = 25 °C
$-V_{GS}$ = 20 V
$-V_{DS}$ (V)
typ
max
$-I_{DS}$ (mA)
3
2
1
0
10
30
50
70
90


7Z67449
$-I_D$ = 10 mA
$-V_{DS}$ = 10 V
typ. values
$-V_{GS}$ (V)
12
11
10
9
−50
0
50
100
150
T_{amb} (°C)


7Z67451
1 kΩ
D
G
S
V
20 V
T_{amb} = 25 °C
typ. values
$-V_{DS}$ (V)
20
15
10
5
0
7,5
10
12,5
15
$-V_{GS}$ (V)


7Z67495
typ. values
Tamb = 25 °C
−ID (mA)
max
−VDS = 10 V
min
−VGS = 20 V
15
14
13
12
−VGS =
11,65 V
11,60
11,55
11,50
11,45
11,40
11,35
11,30
100
50
15
10
5
0
5
10
15
−VGS (V)
−VDS (V)

INTEGRATED AM/FM RADIO RECEIVER CIRCUIT

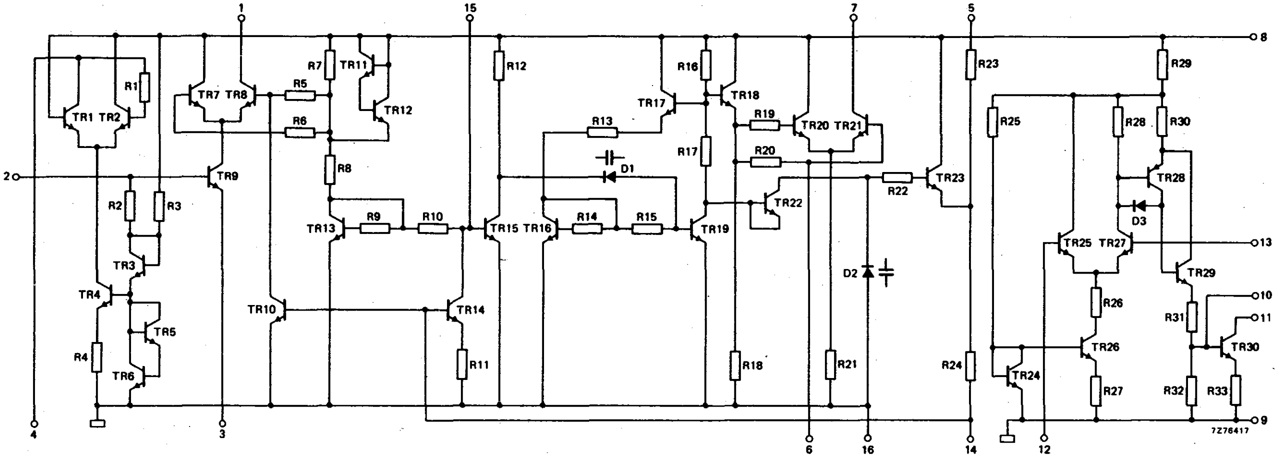
The TBA570A is for use in small low-cost a.m. portable receivers as well as in high quality battery or mains-fed a.m. and a.m./f.m. receivers.
The IC incorporates: a.m. mixer, oscillator, i.f. amplifier, a.g.c. amplifier, a.m. detector and capacitor, f.m./i.f. limiting amplifier and stable base bias for f.m. front-end, and an audio preamplifier and driver.
The unique integrated audio part has an internally limited bandwidth (18 kHz) and negligible h.f. radiation back to the ferrite rod. This makes the TBA570A ideally suitable for small size a.m. receivers because print layout is not critical. The driver stage can directly drive complementary output stages (P_o = 6 W max.), or operate as a post amplifier (V_o = 500 mV).
In its standard applications, the TBA570A can replace the TBA570.

QUICK REFERENCE DATA				
Applicable supply voltage range of receiver	V_P		2,7 to 18	V
Ambient temperature	T_{amb}		25	°C
Supply voltage at pin 8	V_{8-16}	nom.	5,3	V
Total quiescent current except output stages, driver stage TR30 and f.m. front-end	I_{tot}	typ.	9	mA
A.M. performance (at pin 2)				
R.F. input voltage; S/N = 26 dB	V_i	typ.	18	µV
for P_o = 50 mW (adjustable)	V_i	typ.	2	µV
A.G.C. range; change of r.f. input voltage for 10 dB expansion in audio range		typ.	65	dB
R.F. signal handling; d_{tot} = 10%; m = 0,8		typ.	150	mV
F.M. performance (at pin 2)				
R.F. input voltage; 3 dB before limiting	V_i	typ.	50	µV
Audio performance				
Output driver current (peak value)	I_{11M}	<	100	mA
Input impedance (at pin 12)	$\lvert Z_{12-16}\rvert$	typ.	100	kΩ

PACKAGE OUTLINES

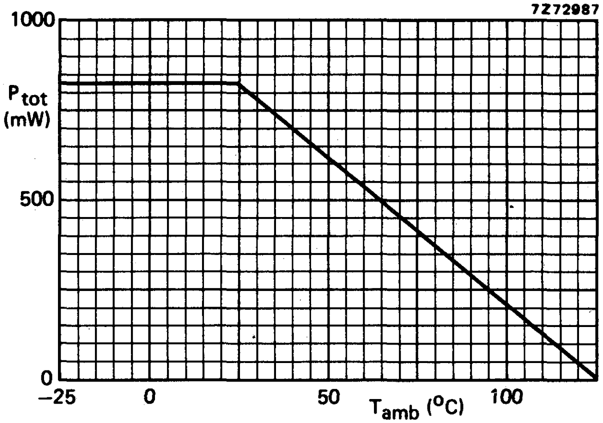
TBA570A : 16-lead DIL; plastic (SOT-38).
TBA570AQ : 16-lead QIL; plastic (SOT-58).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Pin 11 voltage	V_{11-9}	max.	18	V
Pin 8 voltage	V_{8-16}	max.	8	V
Pin 11 current (peak value)	I_{11M}	max.	100	mA
Total power dissipation	see derating curve below			
Storage temperature	T_{stg}		−55 to +125	°C
Operating ambient temperature; $V_{8;4;7;1-16}$ = 8 V; I_{11M} = 100 mA; see also derating curve below	T_{amb}		−20 to +85	°C



DESIGN DATA

Characteristics of integrated components are determined by process and layout data.

Pins not under measuring condition should not be connected.

Voltages with respect to pin 9 and 16 (tolerated minimum : 0 V)

Pins 1 and 7	$V_{1-9(16)}$; $V_{7-9(16)}$	max.	18	V
Pin 4	$V_{4-9(16)}$	max.	8	V
Pin 8	$V_{8-9(16)}$	max.	8	V
Pin 3	$V_{3-9(16)}$	max.	3	V
Pin 5	$V_{5-9(16)}$	max.	4	V
Pin 14	$V_{14-9(16)}$	max.	1	V

Currents (tolerated minimum : 0 mA)

Pins 2, 6, 12, 13 and 15	I_2; I_6; I_{12}; I_{13}; I_{15}	max.	80	μA
Pin 10	I_{10}	max.	5	mA

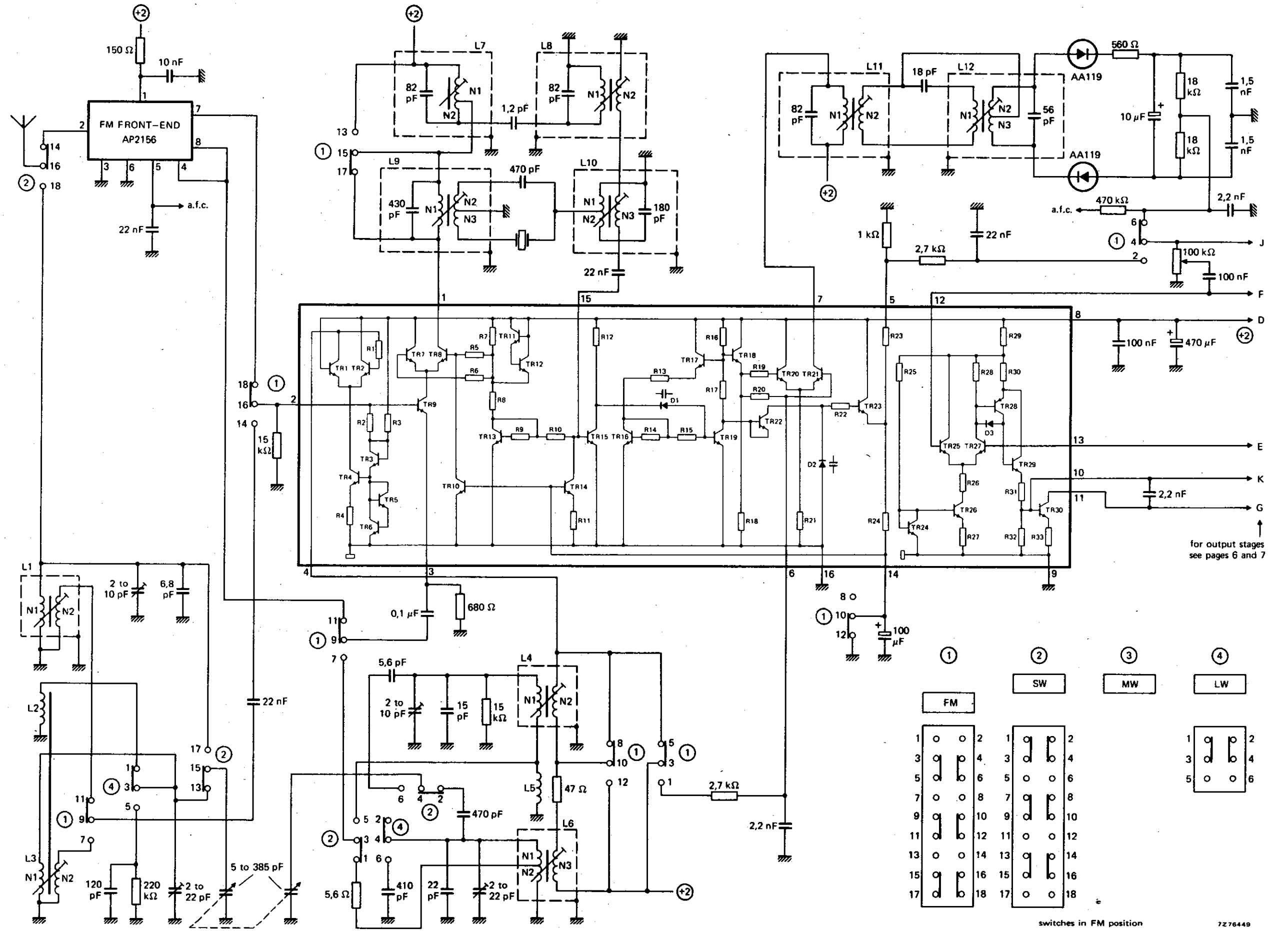
D.C. CHARACTERISTICS at T_{amb} = 25 °C

Saturation voltage of driver stage				
I_C = 50 mA; I_B = 2,5 mA	$V_{11-16sat}$	typ.	1,0	V
		<	1,5	V
Collector breakdown voltage of driver stage				
I_C = 25 mA; R_{BE} = 7 kΩ	$V_{11-16(BR)}$	>	18	V
D.C. current gain of driver stage				
I_C = 50 mA	h_{FE}	>	25	
Total quiescent current				
except driver stage collector current;				
f.m. front-end;				
discrete output stages; V_{8-16} = 5,3 V	I_{tot}	typ.	9	mA
V_{8-16} = 4,2 V	I_{tot}	typ.	8	mA
Applicable supply voltage range of receiver	V_P		2,7 to 18	V 1)
Base bias voltage for f.m. front-end				
total external load current at pin 2: $-I_2$ = 150 μA	V_{2-16}	typ.	1,2	V

A.C. CHARACTERISTICS at T_{amb} = 25 °C; V_{8-16} = 5,3 V; I_E (TR9) = 1 mA

			0,45	1	10,7	MHz
Input conductance at pin 2	g_{ie}	typ.	–	0,4	0,5	mA/V
Output conductance at pin 1	g_{oe}	typ.	6	–	90	μA/V
Input conductance at pin 15	g_{ie}	typ.	0,35	–	0,7	mA/V

1) Adjustable by a dropping resistor in the V_P-line; see also maximum tolerated voltages for pins 1, 4, 7 and 8 in design data on page 3.



H.F. part of a high quality FM/AM (LW; MW; SW) receiver.

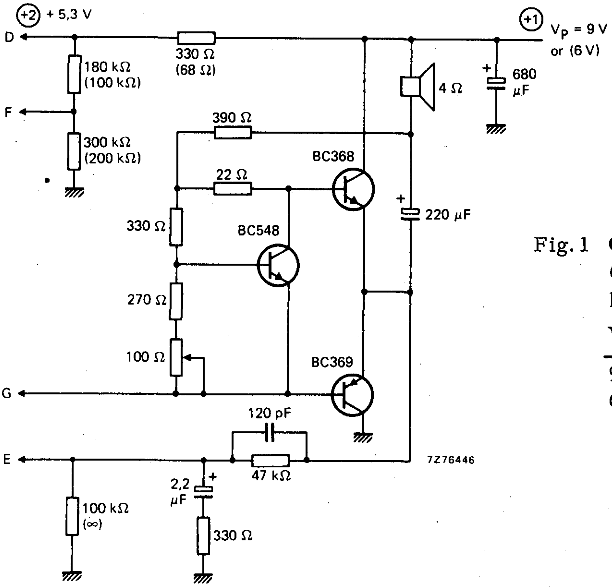


Fig. 1 Output stage for V_P = 9 V or 6 V (resistor values between parentheses).

V_P	R_L	P_o at d_{tot} = 10%
9 V	4 Ω	1, 8 W
6 V	4 Ω	0, 6 W

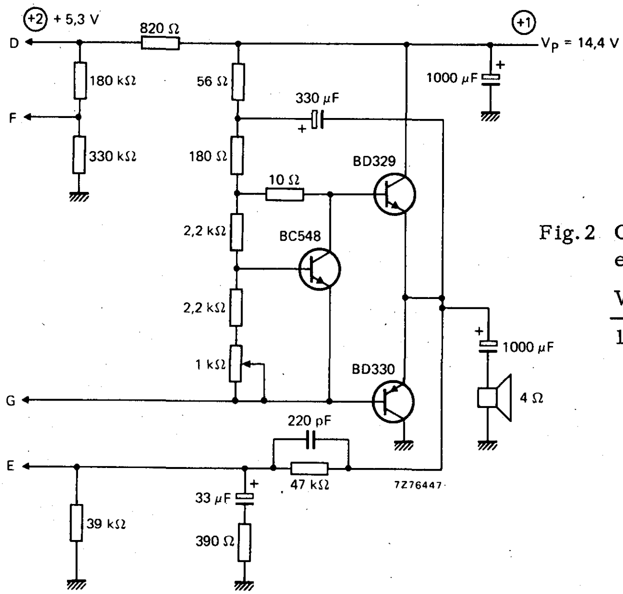


Fig. 2 Output stage for V_P = 14, 4 V; especially used in car radios.

V_P	R_L	P_o at d_{tot} = 10%
14, 4 V	4Ω	5, 5 W

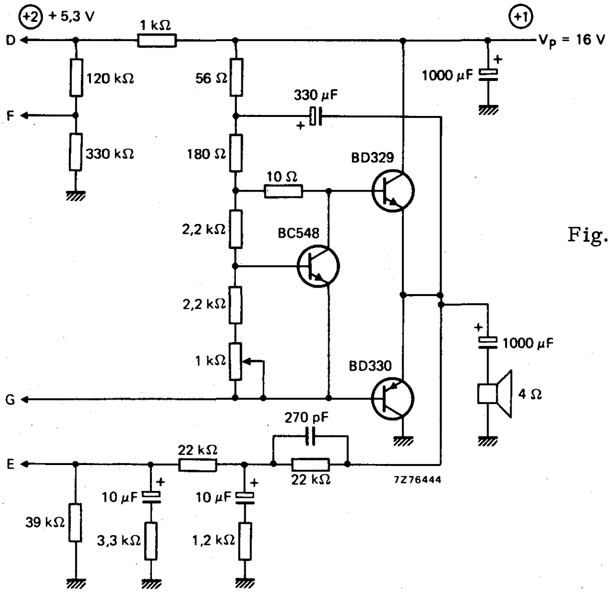


Fig. 3 Output stage for V_P = 16 V.

V_P	R_L	P_o at d_{tot} = 10%
16 V	4Ω	6, 8 W

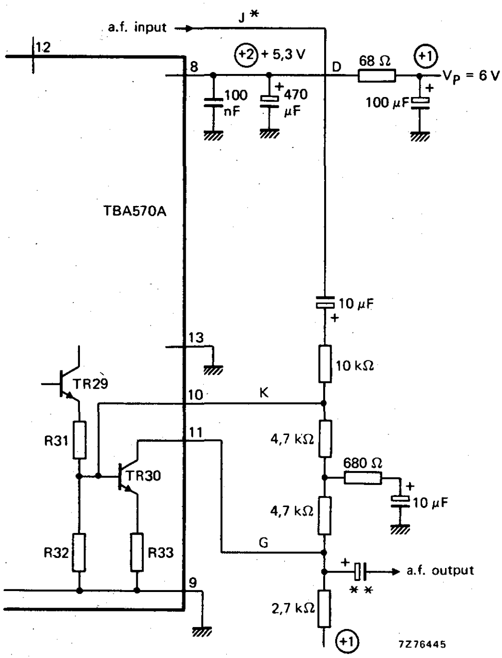


Fig. 4 Post amplifier for
V_o = 500 mV and V_P = 6 V.

*In circuit on page 5 volume control resistor (100 kΩ) and capacitor (100 nF) on pin 12 should be omitted.

**Capacitor value depends on load.

COIL DATA (in circuit on page 5)

High quality AM/FM receiver (for portable and mains-fed applications)

A.M.-I.F. coils (f_o = 455 kHz)

I.F. bandpass filter:

L9 N1 = 284, 5 μH
Q_o = 100
N1/N2 = 40
N2/N3 = 1
$|Z_T|$ = 3 kΩ

L10 N1 = 680 μH
Q_o = 100
N2/N1 = 74
(N2 + N1)/N3 = 10, 7

F.M.-I.F. coils (f_o = 10, 7 MHz)

Second i.f. bandpass filter:

L7 N1 + N2 = 2, 7 μH
Q_o = 100
kQ_{L6-L7} = 1, 2
N1/N2 = 1, 75

L8 N1 = 2, 7 μH
Q_o = 90
N1/N2 = 5, 5

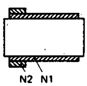
Ratio detector:

L11 N1 = 2, 7 μH
Q_o = 85
$kQ_{L11-L12}$ = 0, 7
N1/N2 = 2, 2

L12 N2 + N3 = 3, 25 μH
Q_o = 85
(N2 + N3)/N1 = 6
N2 = N3

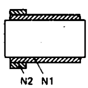
Low-cost 2-band AM portable receiver (see page 9)

L1



N1 = 11
N2 = 2
wire : 1, 1 Ø

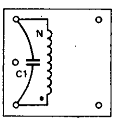
L2



N1 = 60
N2 = 4
wire : 20 x 0, 03

L1 and L2 on ferrite rod; 10 mmØ; length = 10 cm

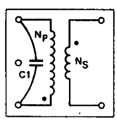
L3



N = 284, 5μH f_m = 452 kHz
C1 = 430 pF Q_o = 100
wire : 0, 1 Ø

core material : 7 MN(C)

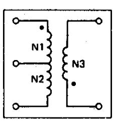
L4



N_p = 284, 5μH f_m = 452 kHz
N_p/N_s = 16, 7 Q_o = 100
C1 = 430 pF
wire : 0, 1 Ø

core material : 7 MN(C)

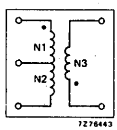
L5



N1 + N2 = 127μH f_m = 1 MHz
(N1 + N2)/N2 = 58 Q_o = 100
(N1 + N2)/N3 = 4, 8 C_p = 200 pF
wire : 0, 1 Ø

core material : 7 BR

L6



N1 + N2 = 13μH f_m = 7 MHz
(N1 + N2)/N2 = 20 Q_o = 90
(N1 + N2)/N3 = 4 C_p = 40 pF
wire : 0, 1 Ø

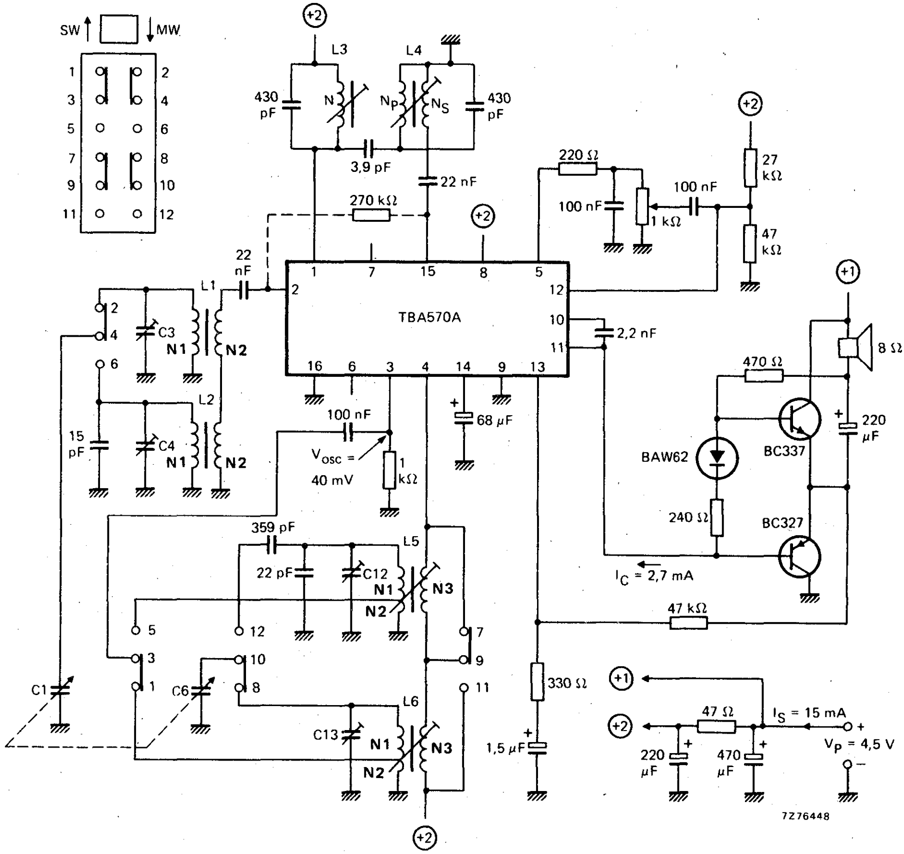
core material : 119 AM(C)

Note

In the circuit on page 9 for L3 and L4 a similar coil to L9 in the circuit on page 5 can be used with the following exceptions:
L3 : secondary windings N2 and N3 are not used.
L4 : secondary windings N2 and N3 are connected in series.

When using a resistor between pins 2 and 15 (see dashed resistor in circuit on page 9), signal handling is improved.

Low-cost 2-band (SW-MW) AM portable receiver (P_O = 250 mW)



Note : C1 and C6 max. 385 pF.

APPLICATION INFORMATION at T_{amb} = 25 °C

A.M. performance	V_{8-16}		5,3 V [1]	4,2 V [2]	
R.F. input voltage: S/N = 26 dB (notes 3 and 4)	V_i	typ.	18	10	μV
for P_o = 50 mW (adjustable); notes 3, 4 and 5	V_i	typ.	2	2	μV
R.F. input voltage for 10 mV (a.f.) across volume control (notes 3 and 4)	V_i	typ.	2,7	4,5	μV
A.F. voltage across volume control at 100 μV (r.f.) input voltage (notes 3 and 4)	V_o	typ.	70	70	mV
Signal-to-noise ratio at 1 mV (r.f.) input voltage (notes 3 and 4)	S/N	typ.	46	47	dB
A.G.C. range (change in r.f. input voltage for 10 dB expansion in audio range); notes 3 and 4		typ.	60	60	dB
R.F. signal handling capability at 80% modulation; d_{tot} < 10% (note 3)	V_i	typ.	150	7	mV
Harmonic distortion of h.f. part over most of a.g.c. range; m = 0,3; f_m = 1 kHz (note 6)	d_{tot}	typ.	1	1	%
I.F. selectivity	S_9	typ.	33	16	dB
I.F. bandwidth (3 dB)	B	typ.	5	5,5	kHz

Notes

1. See circuits on pages 5, 6 and 7 (high quality AM/FM receiver).
2. See circuit on page 9 (low-cost 2-band AM portable receiver).
3. a. A.F. signal: measured across volume control.
   b. R.F. signal: measured at pin 2 with the aerial circuit connected (source resistance about 1 kΩ).
   c. f_o = 1 MHz; f_m = 1 kHz.
4. m = 0,3.
5. A.M. sensitivity for P_o = 50 mW can be adjusted by means of the a.c. feedback network in the audio part e.g.: V_i = 1,5 μV for P_o = 50 mW (S/N ≈ 4 dB).
6. Distortion can be decreased to 0,7% by connecting a resistor of 270 kΩ between pins 2 and 15.

APPLICATION INFORMATION (continued) at $T_{amb} = 25\ ^{o}C$; $V_{8-16} = 5,3$ V

Measured in the circuit on page 5

F.M. performance

Sensitivity for an f.m. signal 3 dB before limiting				
at 75 Ω aerial input of f.m. front-end (note 1)	V_i	typ.	3,5	μV
at pin 2; first i.f. (notes 2 and 6)	V_i	typ.	50	μV
Sensitivity for 26 dB S/N ratio				
at 75 Ω aerial input of f.m. front-end (note 1)	V_i	typ.	2,5	μV
A.F. output voltage across volume control				
at an i.f. signal beyond limiting (note 2)	V_o	typ.	120	mV
Signal-to-noise ratio				
over most of signal range (note 2)	S/N	typ.	65	dB
A.M. suppression over most of signal range (note 3)		typ.	60	dB
I.F. selectivity (note 4)	S_{300}	typ.	43	dB
I.F. bandwidth (3 dB; note 4)	B	typ.	150	kHz
A.F. signal distortion				
3 dB before i.f. limiting (note 5)	d_{tot}	typ.	0,8	%

Notes

1. Aerial e.m.f. (V_i) at f_o = 98 MHz; R_S = 50 Ω; Δf = ±22,5 kHz; f_m = 1 kHz.
2. f_o = 10,7 MHz; Δf = ±22,5 kHz; f_m = 1 kHz.
3. A.M. signal: m = 0,3; f_m = 1000 Hz.
   F.M. signal: f_o = 10,7 MHz; Δf = ±75 kHz; f_m = 400 Hz.
   Carrier simultaneously modulated with a.m. and f.m.
4. Including ratio detector.
5. f_o = 98 MHz; Δf = ±40 kHz; f_m = 1 kHz.
6. Pin 3 by-passed to ground with a capacitor of 220 nF.

AUDIO PERFORMANCE

Distortion before clipping (note 1)	d_{tot}	typ.	0,5	%
Input impedance (note 2)	$\|Z_i\|$	typ.	90	kΩ
Noise output power; volume control at min. (note 3)	P_n	typ.	10	nW
Overall fidelity; flat within 3 dB (obtainable values)		35 Hz to	15	kHz
Open loop voltage gain	G_v	typ.	62	dB

V_P	V	4,5	6	9	14,4	16
R_L	Ω	8	4	4	4	4
P_o at d_{tot} = 10%	W	0,22	0,6	1,8	5,5	6,8
P_o at onset of clipping; d_{tot} = 1%	W	0,15	0,4	1,2	4	4,8
V_i for d_{tot} = 10% (pin 12)	mV	14	16	25	50	45
V_i for P_o = 50 mW (pin 12)	mV	5,5	4,5	4	3,5	3,5
Output transistors		BC327 BC337	BC368 BC369	BC368 BC369	BD329 BD330	BD329 BD330
Circuit diagrams on page 6, 7 or 9		page 9	Fig. 1	Fig. 1	Fig. 2	Fig. 3

Post-amplifier (see Fig. 4 on page 7)

Output voltage : 500 mV

Audio gain (adjustable): 5

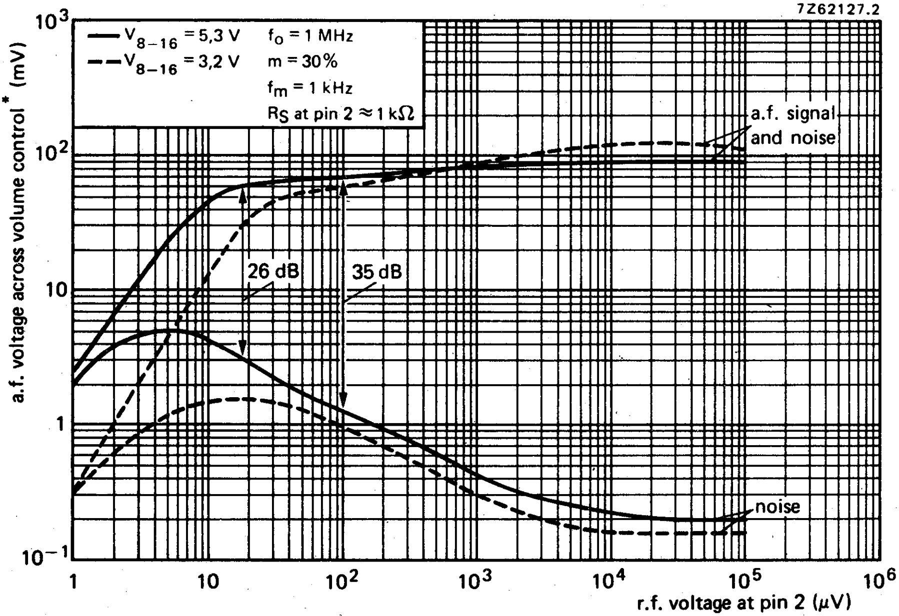
Distortion : 0,2%

Notes

1. Measured at 1 kHz and a negative feedback of 16 dB.
2. At the maximum tolerated value of resistance-tap/bleeder at pin 12.
3. Measured at a bandwidth of 60 Hz to 15 kHz, pin 12 being connected via a capacitor of 32 µF to pin 9; R_L = 4 Ω.

APPLICATION INFORMATION (continued)

Typical a.g.c. curves for AM reception (circuit diagram on page 5)

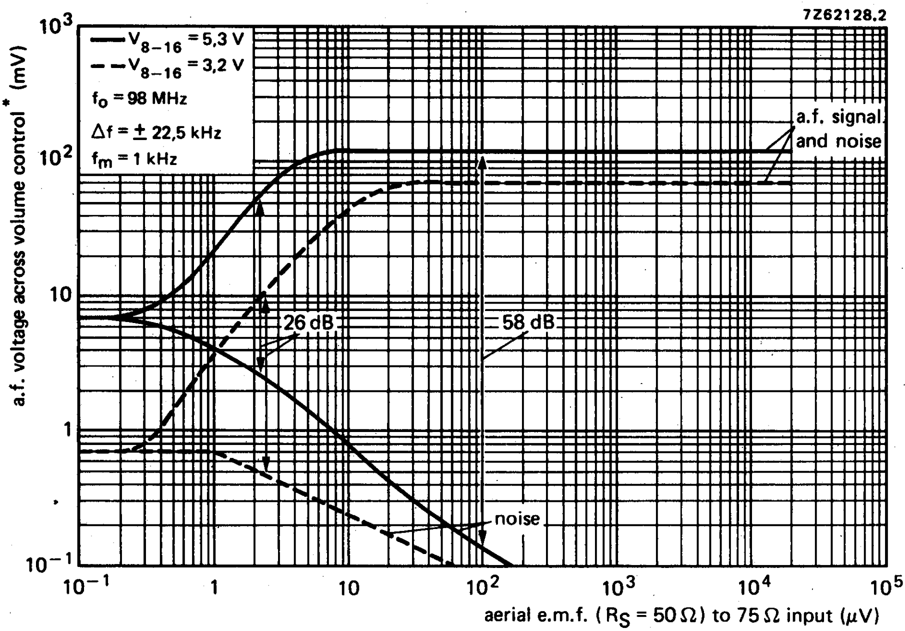


A.F. voltage across volume control as a function of r.f. voltage at pin 2.

*) Slider at lower end.

APPLICATION INFORMATION (continued)

Typical S/N curves for FM reception (circuit diagram on page 5)



A.F. voltage across volume control as a function of aerial e.m.f. from a source with R_S = 50 Ω to the 75 Ω input of the f.m. front-end.

*) Slider at lower end.

INTEGRATED A.M./F.M. RADIO RECEIVER CIRCUIT

The TBA700 is a monolithic integrated circuit for use in a.m. (including the short-wave band), a.m./f.m. receivers.
It incorporates the class-B audio output stage (1 W), stabilization circuit for quiescent current, driver, pre-amplifier, 2-stage i.f. amplifier, a.g.c. and stabilized bias circuit.
The discrete input stage (for a.m.: mixer-oscillator; for f.m.: 1st i.f.) enables a high flexibility in circuit lay-out with conventional or lumped selectivity.
The internal stabilization ensures negligible loss of sensitivity and cross-over distortion over a wide supply voltage range from 2,7 V to 12 V.

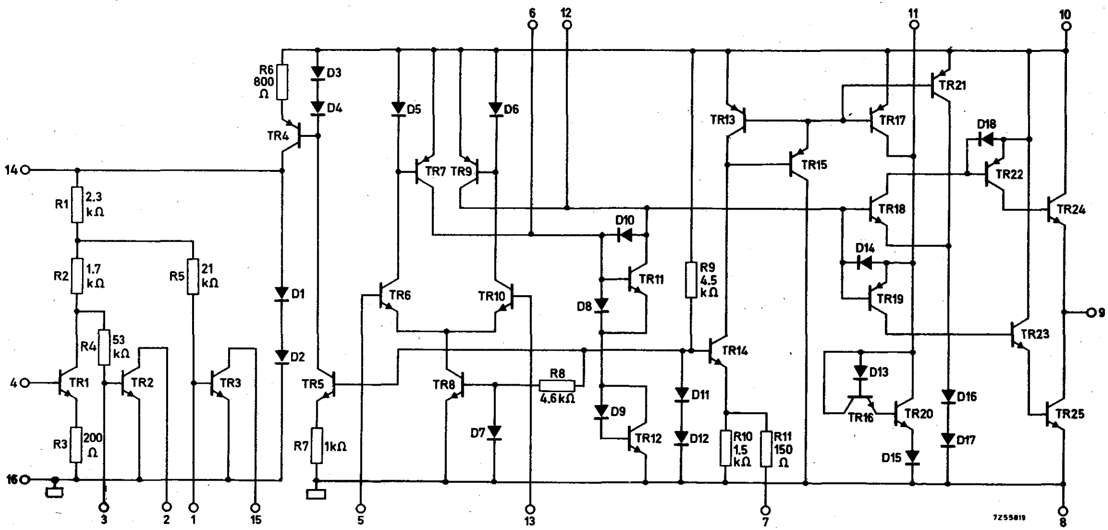
QUICK REFERENCE DATA				
Applicable supply voltage range of receiver	V_{10-8}		2,7 to 12	V 1)
Ambient temperature	T_{amb}		25	°C
Supply voltage	V_P	nom.	9	V
Total quiescent current (inclusive discrete input transistor, exclusive f.m. front end)	I_{tot}	typ.	24,5	mA
A.F. output power at d_{tot} = 10 %, R_L = 8 Ω	P_o	typ.	1000	mW
A.M. performance				
R.F. input voltage (S/N = 26 dB) (at base of external mixer-oscillator)	V_i	typ.	15	μV
A.G.C. range (change of r.f. input voltage for 10 dB expansion in audio range)		typ.	72	dB
F.M. performance				
R.F. input voltage (at base of external i.f. stage) 3 dB before limiting	V_i	typ.	150	μV

PACKAGE OUTLINE

16-lead DIL; plastic with internal copper slug (SOT-38).

1) The data given in this sheet are based on a receiver with V_P = 9 V; P_o = 1000 mW.

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages

Pin No. 10 voltage	V_{10-8}	max.	12	V	
Pins No. 15, 9, 2 voltages	V_{15-8}, V_{9-8}, V_{2-8}	max.	11,4	V	
Pin No. 16 voltage	V_{16-8}	max.	0	V	1)
Pin No. 7 voltage	$\pm V_{7-8}$	max.	5	V	
Pins No. 4, 3, 1 voltages	$-V_{4-16}$, $-V_{3-16}$, $-V_{1-16}$	max.	5	V	
Pin No. 5 voltage	$\pm V_{5-13}$	max.	5	V	
Pin No. 10 voltage	V_{10-9}	max.	11,4	V	

Currents

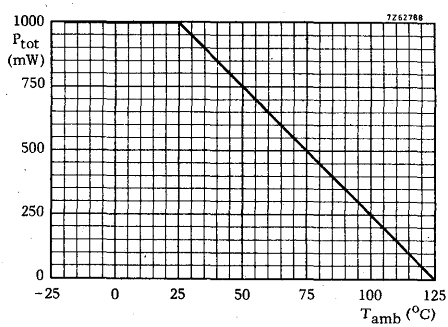
Pins No. 14, 12, 11, 6 currents	I_{14}, I_{12}, I_{11}, I_6	max.	5	mA	
Pins No. 13, 5, 4, 3, 1 currents	I_{13}, I_5, I_4, I_3, I_1	max.	0,5	mA	
Pins No. 15, 2 currents	I_{15}, I_2	max.	10	mA	
Pin No. 8 current	$-I_{8RM}$	max.	0,8	A	2)
Pin No. 9 current	$\pm I_{9RM}$	max.	0,8	A	2)
Pin No. 10 current	I_{10RM}	max.	0,8	A	2)

Dissipation

Total power dissipation				
at T_{amb} = 45 °C	P_{tot}	max.	800	mW
at T_{amb} = 25 °C	P_{tot}	max.	1000	mW

Temperatures

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature	T_{amb}	−20 to +125	°C



1) Substrate connected to pin 16.
2) Repetitive peak value; internally limited.

CHARACTERISTICS

D.C. characteristics at T_{amb} = 25 °C; V_P = 9 V

I. F. amplifier

Collector current of i.f. transistor TR2 (a.g.c. transistor "off")	I_C	typ.	1	mA
			0,55 to 1,6	mA
Collector current of i.f. transistor TR3 (a.g.c. transistor "off")	I_C	typ.	2,5	mA
			1,4 to 4,2	mA
Saturation voltage of i.f. transistor TR2 at $I_C \leq 2$ mA	V_{CEsat}	<	150	mV
Saturation voltage of i.f. transistor TR3 at $I_C \leq 5$ mA	V_{CEsat}	<	200	mV
Bias voltage for mixer and tuner	V_{14-16}	typ.	1,4	V
			1,25 to 1,55	V
Temperature dependency of bias voltage V_{14-16}	T_c	typ.	−3,6	mV/°C
Bias current (available)	$-I_{14}$	<	100	μA

A. F. amplifier

Input common mode voltage range	V_{5-8}, V_{13-8}		1,0 to 8,5	V 1)
Input base bias current	I_5, I_{13}	<	25	μA

Complete circuit

Total quiescent current with 3,3 kΩ between pins 7 and 8 (inclusive discrete input transistor, exclusive f.m. front end)	I_{tot}	typ.	24,5	mA 2)
		<	30,5	mA 2)

1) Maximum input common mode voltage; V_{5-8}, V_{13-8}: < (V_P − 0,5) V.

2) In those cases where a lower supply current is required the resistor between pins 7 and 8 (3,3 kΩ) can be avoided, resulting in a total current of 17 mA. In this case however some devices may show a marginal increase of the distortion level.

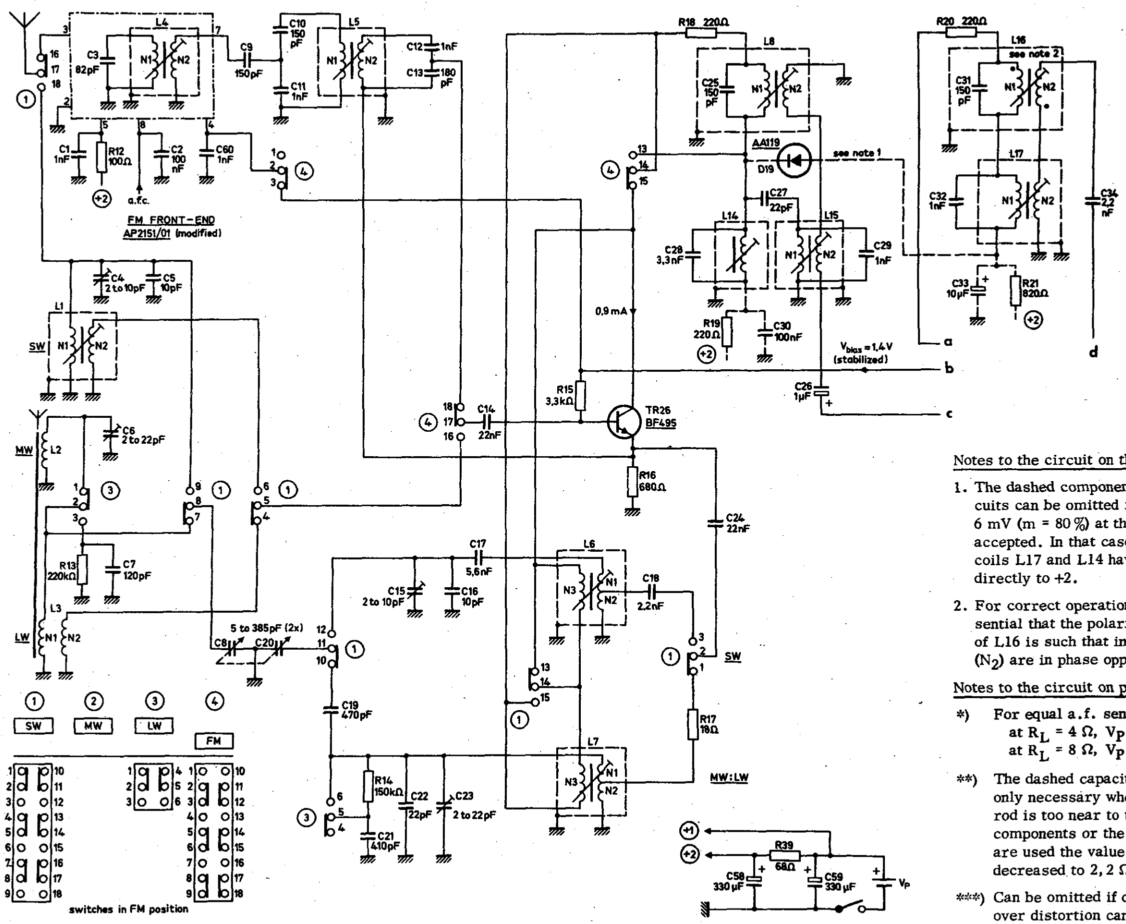
CHARACTERISTICS (continued)

A.C. characteristics of i.f. part

y parameters at f = 450 kHz [1]			i.f. transistors: TR2	TR3	
Input conductance	g_{ie}	typ.	0,45	1,15	mA/V
Input capacitance	C_{ie}	typ.	23	36	pF
Output conductance	g_{oe}	typ.	6,0	13,5	µA/V
Output capacitance	C_{oe}	typ.	4,0	4,25	pF
Transfer admittance	$\|y_{fe}\|$	typ.	37	82	mA/V
Phase angle of transfer admittance	φ_{fe}	typ.	1^o	2^o	
Feedback admittance	$\|y_{re}\|$	typ.	2,5	1,8	µA/V
Phase angle of feedback admittance	φ_{re}	typ.	90^o	90^o	

y parameters at f = 10,7 MHz [1]			i.f. transistors: TR2	TR3	
Input conductance	g_{ie}	typ.	0,6	1,5	mA/V
Input capacitance	C_{ie}	typ.	22	35	pF
Output conductance	g_{oe}	typ.	24	30	µA/V
Output capacitance	C_{oe}	typ.	4,3	4,7	pF
Transfer admittance	$\|y_{fe}\|$	typ.	35	73	mA/V
Phase angle of transfer admittance	φ_{fe}	typ.	22^o	35^o	
Feedback admittance	$\|y_{re}\|$	typ.	64	43	µA/V
Phase angle of feedback admittance	φ_{re}	typ.	90^o	90^o	

1) At typical values for h_{fe} and I_c.



Notes to the circuit on this page

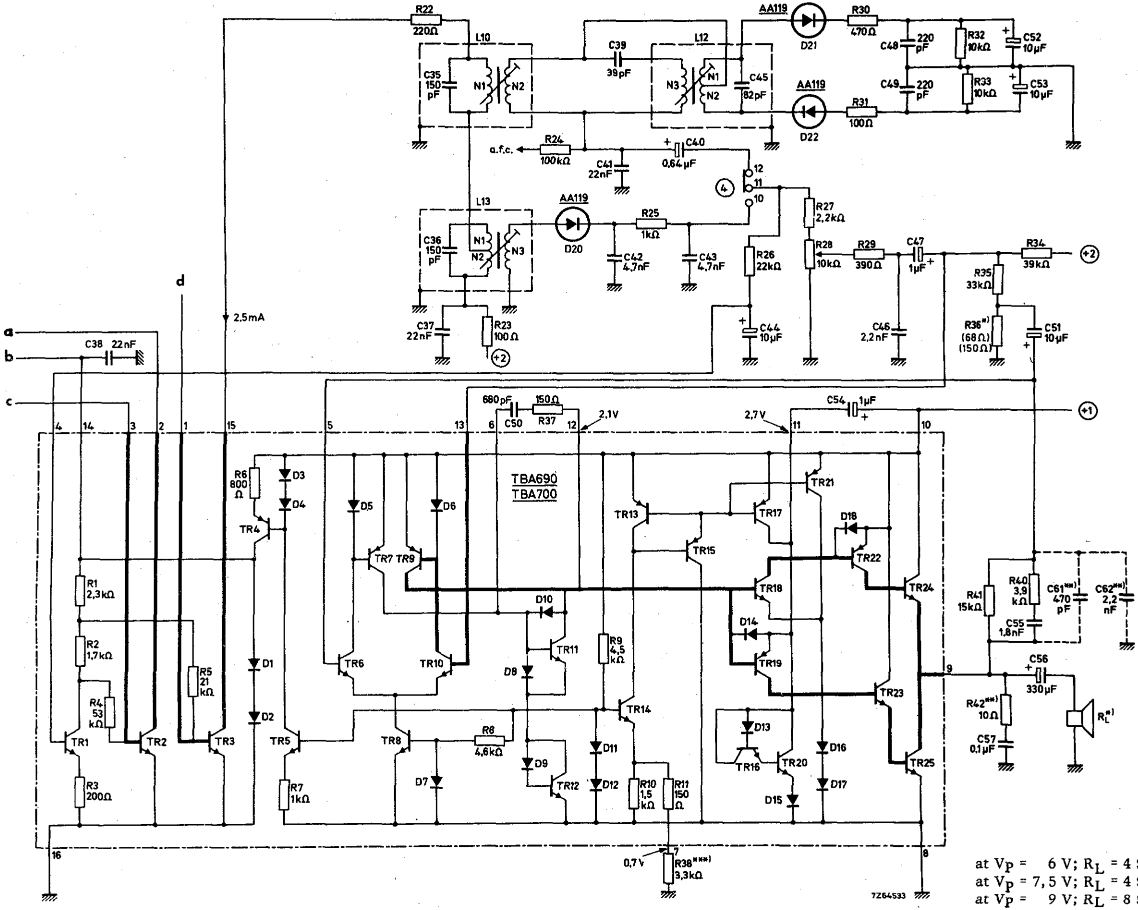
1. The dashed components in the i.f.circuits can be omitted if signal handling of 6 mV (m = 80 %) at the base of TR26 is accepted. In that case the cold ends of coils L17 and L14 have to be connected directly to +2.
2. For correct operation on f.m. it is essential that the polarity of the windings of L16 is such that input (N_1) and output (N_2) are in phase opposition.

Notes to the circuit on page 7

*) For equal a.f. sensitivity:
at R_L = 4 Ω, V_P = 6 V: R36 = 150 Ω
at R_L = 8 Ω, V_P = 9 V: R36 = 68 Ω

**) The dashed capacitors (C61; C62) are only necessary when the ferrite aerial rod is too near to the a.f. output components or the IC. If C61 and C62 are used the value of R42 must be decreased to 2,2 Ω.

***) Can be omitted if degraded cross-over distortion can be tolerated.



*) at V_P = 6 V; R_L = 4 Ω
at V_P = 7,5 V; R_L = 4 Ω
at V_P = 9 V; R_L = 8 Ω

Reference numbers L9 and L11 are not used in this circuit.

APPLICATION INFORMATION (continued) at T_{amb} = 25 °C; V_P = 9 V

See also circuit diagram on pages 6 and 7.

A.M. performance

R.F. input voltage for signal to noise ratio of 26 dB	V_i	typ.	15	µV	1)2)
R.F. input voltage for 10 mV (a.f.) across volume control	V_i	typ.	3	µV	1)2)
A.F. voltage across volume control at 100 µV (r.f.) input voltage	V_o	typ.	100	mV	1)2)
Signal to noise ratio at 1 mV (r.f.) input voltage	S/N	typ.	53,4	dB	1)2)
A.G.C. range (change in r.f. input voltage for 10 dB expansion in audio range)					
without a.g.c. diode		typ.	42	dB	1)2)3)
with a.g.c. diode		typ.	72	dB	1)2)
R.F. signal handling capability on base of TR26 80 % modulation ($d_{tot} \leq 10$ %)					
without a.g.c. diode	V_i	typ.	6	mV	3)
with a.g.c. diode	V_i	typ.	80	mV	
Harmonic distortion of h.f. part (over most of a.g.c. range)	d_{tot}	typ.	1	%	1)2)
I.F. selectivity	S_9	typ.	30	dB	
I.F. bandwidth	B_{3dB}	typ.	4,5	kHz	

1) a. Negligible influence of supply voltage variations in a range of 2,7 V to 12 V
b. A.F. signal: measured across volume control.
c. R.F. signal: measured at base of external mixer-oscillator with the antenna-circuit connected (source resistance R_S of about 1 kΩ).
d. f_o = 1 MHz, f_m = 1 kHz
2) m = 0.3
3) Dashed parts of circuit diagram on pages 6 and 7 are omitted.

APPLICATION INFORMATION (continued) See also circuit on pages 6 and 7.

F.M. performance

Sensitivity for an f.m. signal 3 dB before limiting					
at 75 Ω aerial input of f.m. front end	V_i	typ.	12	μV	1)
at base of external (first i.f.) stage	V_i	typ.	150	μV	2)
at pin 3	V_i	typ.	2,2	mV	2)
Sensitivity for 26 dB S/N ratio at 75 Ω aerial input of f.m. front end	V_i	typ.	4	μV	1)
A.F. output voltage across volume control at an i.f. signal beyond limiting	V_o	typ.	140	mV	2)
S/N ratio over most of signal range	S/N	typ.	55	dB	2)
A.M. suppression over most of signal range		>	40	dB	2)3)
I.F. selectivity	S_{300}	typ.	40	dB	4)
I.F. bandwidth	B_{3dB}	typ.	180	kHz	4)
A.F. signal distortion, 3 dB before i.f. limiting	d_{tot}	<	2	%	5)

Audio performance

A.F. output power at d_{tot} = 10 %	P_o	typ.	1	W	6)
at onset of clipping	P_o	typ.	0,7	W	6)
Distortion before clipping	d_{tot}	typ.	1	%	6)
A.F. input signal (at pin 13)					
at P_o = 50 mW	V_i	typ.	6	mV	6)
at P_o = 700 mW	V_i	typ.	17	mV	6)
Noise output power (volume control at minimum)	P_N	typ.	20	nW	7)
Typical overall fidelity (flat within 3 dB)		200 Hz to	6	kHz	8)
Open loop voltage gain	G_v	typ.	60	dB	

1) Aerial e.m.f. (V_i) at f_o = 100 MHz; R_S = 50 Ω (source resistance; see page 12) Δf = ± 15 kHz; f_m = 1 kHz.
2) f_o = 10,7 MHz; Δf = ± 15 kHz; f_m = 1 kHz.
3) A.M. signal: m = 0,3; f_m = 400 Hz (carrier simultaneously modulated with a.m. and f.m.).
4) Including ratio detector.
5) f_o = 100 MHz; Δf = ± 40 kHz; f_m = 1 kHz.
6) Measured at 1 kHz, a negative feedback of 15 dB and a loudspeaker of 8 Ω; V_P = 9 V.
7) Measured at a bandwidth of 200 Hz to 6 kHz, pin 13 being connected via a capacitor of 32 μF to pin 16; loudspeaker impedance 8 Ω.
8) Depending on values of capacitors C51 and C55, 50 Hz to 15 kHz is possible.

COIL DATA See also circuit on pages 6 and 7.

1. A.M.–I.F. coils (f_o = 452 kHz)

First i.f. bandpass filter

Primary : L14 = 38 μH
C_p = 3300 pF
Q_0 = 90

Secondary : L15 (N_1) = 125 μH
C_p = 1000 pF
Q_0 = 80
N_1/N_2 = 18
$kQ_{L14-L15}$ = 1

Single tuned coil

L17 (N_1) = 125 μH
C_p = 1000 pF
Q_0 = 80
N_1/N_2 = 30

Detector coil

L13 (N_1+N_2) = 0, 84 mH
C_p = 150 pF
Q_0 = 130
N_1/N_2 = 3, 1
$(N_1+N_2)/N_3$ = 4

2. F.M.–I.F. coils (f_o = 10, 7 MHz)

First i.f. bandpass filter

Primary : L4 (N_1) = 2, 6 μH
C_p = 82 pF
Q_0 = 90
N_1/N_2 = 10

Secondary : L5 (N_1) = 1, 44 μH
C_p = 150 pF
Q_0 = 55
N_1/N_2 = 5, 7
kQ_{L4-L5} = 1, 2

First single tuned filter

L8 (N_1) = 1, 44 μH
C_p = 150 pF
Q_0 = 45
N_1/N_2 = 5, 7

Second single tuned filter

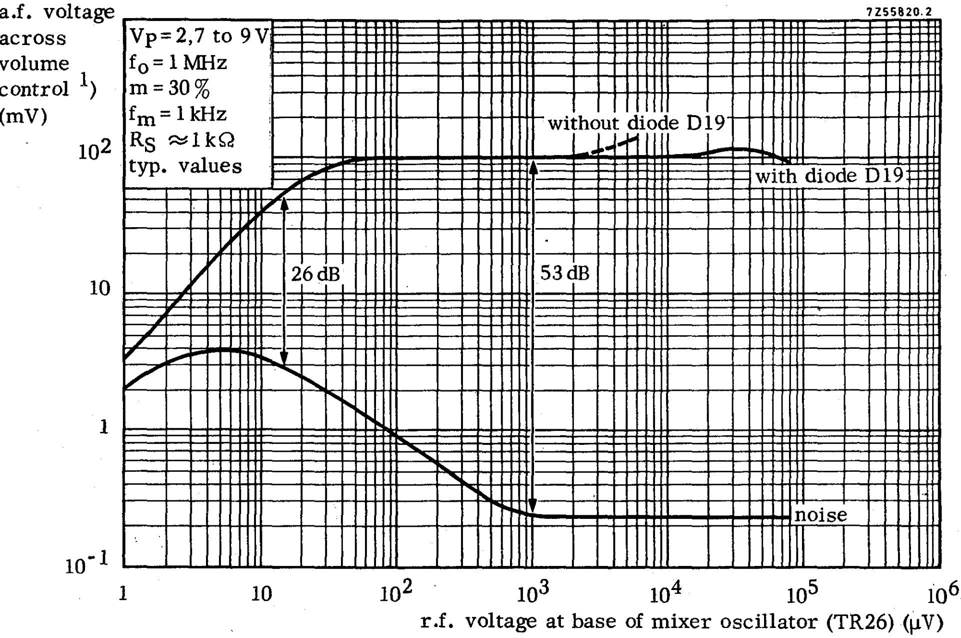
L16 (N_1) = 1, 44 μH
C_p = 150 pF
Q_0 = 45
N_1/N_2 = 5, 7

Ratio detector

Primary : L10 (N_1) = 1, 44 μH
C_p = 150 pF
Q_0 = 95
N_1/N_2 = 2

Secondary : L12 (N_1+N_2) = 2, 6 μH
C_p = 82 pF
Q_0 = 110
N_1/N_2 = 1
$(N_1+N_2)/N_3$ = 5, 4
$kQ_{L10-L12}$ = 0, 7

APPLICATION INFORMATION (continued)

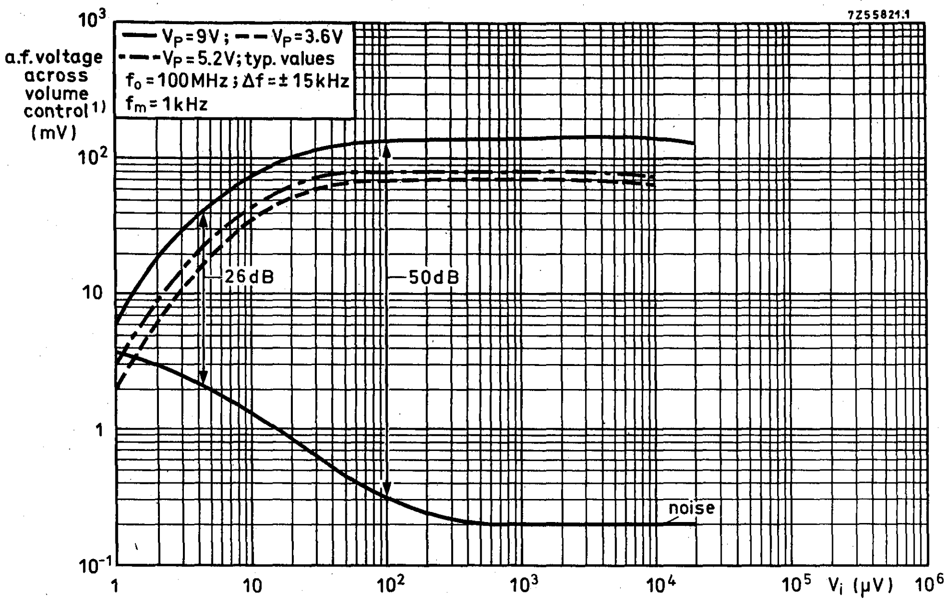


Typical a.g.c. curves at a.m. reception

A.F. voltages across volume control versus r.f. voltage at base of mixer-oscillator.

1) Slider at lower end.

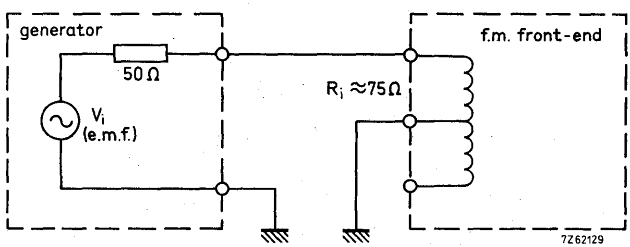
APPLICATION INFORMATION (continued)



Typical S/N curves at f.m. reception

A.F. voltage across volume control versus aerial e.m.f. represented by the generator voltage V_i (e.m.f.) connected to the 75 Ω input of the f.m. front-end.

Test circuit



1) Slider at lower end.

HI-FI F.M./I.F. AMPLIFIER

The TCA420A is a monolithic integrated f.m./i.f. amplifier for car and hi-fi equipment provided with the following functions:

- limiter amplifier
- symmetrical quadrature detector
- symmetrical a.f.c. output
- field-strength indication output
- stereo decoder switching voltage
- adjustable side response suppression
- muting

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	15	V
Supply current (pin 11)	I_P	typ.	26	mA
Input limiting voltage (−3 dB); f_o = 10,7 MHz	$V_{i\,lim}$	typ.	20	μV
A.F. output voltage (pin 5); $\Delta f = \pm 15$ kHz; r.m.s. value	$V_{o(rms)}$	typ.	115	mV
Signal plus noise-to-noise ratio; $V_i > 1$ mV; $\Delta f = \pm 15$ kHz	S+N/N	typ.	72	dB
I.F. input voltage; $\Delta f = \pm 15$ kHz				
S + N/N = 26 dB	V_i	typ.	15	μV
S + N/N = 46 dB	V_i	typ.	45	μV
A.M. rejection; V_i = 10 mV; f_m = 1 kHz (f.m.); $\Delta f = \pm 15$ kHz	α	typ.	50	dB
Total distortion (single tuned circuit); $\Delta f = \pm 15$ kHz	d_{tot}	typ.	0,1	%
Centre shift of f.m. detector curve	$\Delta f = \lvert f_{o1} - f_{o2} \rvert$	typ.	7	kHz
Field-strength indication range	ΔV_i	typ.	70	dB
Supply voltage range (pin 11)	V_P		6 to 18	V
Ambient temperature range	T_{amb}		−30 to +80	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

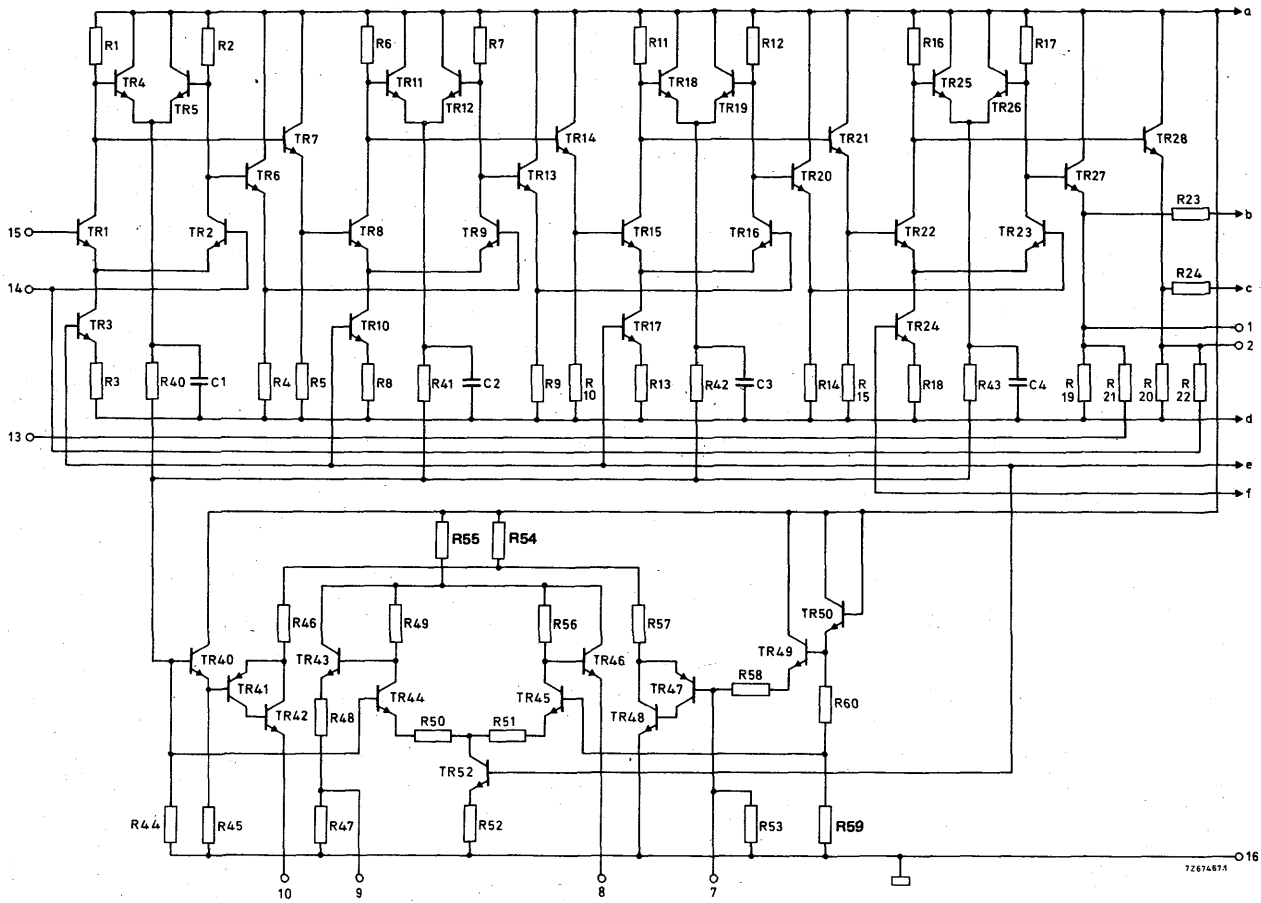


Fig. 1a Part of circuit diagram; other part continued in Fig. 1b.

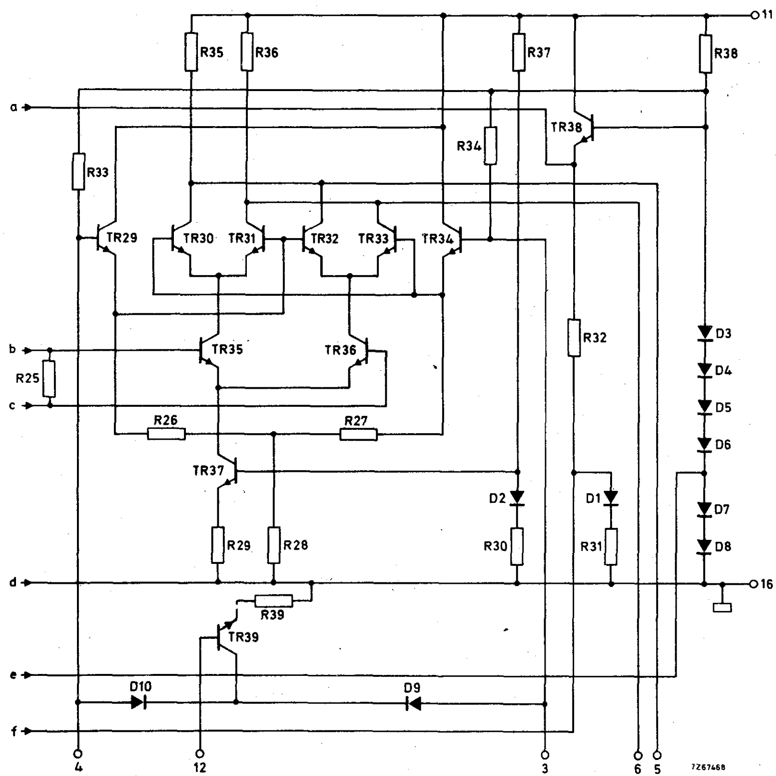


Fig. 1b Part of circuit diagram; continued from Fig. 1a.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	$V_P = V_{11\text{-}16}$	max.	18	V
Total power dissipation	P_{tot}	max.	720	mW
Storage temperature	T_{stg}		−55 to +150	°C
Operating ambient temperature	T_{amb}		−30 to +80	°C

CHARACTERISTICS

V_P = 8 or 15 V; T_{amb} = 25 °C; f_o = 10,7 MHz; Δf = ±15 kHz; f_m = 1 kHz; R_G = 30 Ω; with de-emphasis ($C_{5\text{-}6}$ = 10 nF); adjustment conforms to adjustment procedure unless otherwise specified; the characteristics are valid for a TCA420A mounted on a printed-circuit board (see Figs 2, 3 and 4).

Supply voltage range (pin 11) V_P 6 to 18 V

			V_P = 8 V	V_P = 15 V	
Supply current; $R_{7\text{-}16}$ = 5 kΩ; pin 11	I_P	typ.	21	26	mA
		<	–	35	mA
I.F. amplifier/detector					
Input voltages (d.c. value)	$V_{13\text{-}16}$; $V_{14\text{-}16}$; $V_{15\text{-}16}$	typ.	2,6	2,8	V
Input limiting voltage (−3 dB)	$V_{i\,lim}$	typ.	20	20	μV
		<	–	50	μV
I.F. output voltage (peak-to-peak value)					
V_i = 5 mV; f = 1 MHz; without detector circuit;	$V_{1\text{-}16(p\text{-}p)}$	>	300	320	mV
$Z_{1\text{-}16} = Z_{2\text{-}16}$ = 10 MΩ in parallel with 8 pF	$V_{2\text{-}16(p\text{-}p)}$	typ.	350	375	mV
Output voltages (d.c. value)	$V_{5\text{-}16}$	>	4,7	8,3	V
	$V_{6\text{-}16}$	typ.	5,0	9,5	V
		<	5,3	11,0	V
Output voltage difference (d.c. value)					
V_i = 1 mV; Δf = ±75 kHz	$\pm V_{5\text{-}6}$	<	180	350	mV
A.F. output voltage; V_i = 1 mV (pins 5 and 6)					
Δf = ±15 kHz	V_o	>	–	95	mV
		typ.	60	115	mV
Δf = ±40 kHz	V_o	typ.	160	307	mV
Δf = ±75 kHz	V_o	typ.	300	575	mV
Total distortion; V_i = 1 mV; single tuned circuit; Q_L = 20					
with de-emphasis; $C_{5\text{-}6}$ = 10 nF					
Δf = ±15 kHz	d_{tot}	<	0,1	0,1	%
Δf = ±40 kHz	d_{tot}	typ.	0,18	0,18	%
Δf = ±75 kHz	d_{tot}	typ.	0,45	0,45	%
without de-emphasis; $C_{5\text{-}6}$ = 220 pF					
Δf = ±15 kHz	d_{tot}	<	0,1	0,1	%
Δf = ±40 kHz	d_{tot}	typ.	0,22	0,22	%
Δf = ±75 kHz	d_{tot}	typ.	0,65	0,65	%
		<	1	1	%

		$V_P = 8$ V	$V_P = 15$ V
I.F. input voltage; with filter: B = 250 Hz to 16 kHz			
S+N/N = 26 dB; with de-emphasis; C_{5-6} = 10 nF			
$\Delta f = \pm 15$ kHz	V_i	typ. 15	15 μV
$\Delta f = \pm 75$ kHz	V_i	typ. 5	5 μV
S+N/N = 26 dB; without de-emphasis; C_{5-6} = 220 pF			
$\Delta f = \pm 15$ kHz	V_i	typ. 20	20 μV
$\Delta f = \pm 75$ kHz	V_i	typ. 8	8 μV
S+N/N = 46 dB; with de-emphasis; C_{5-6} = 10 nF			
$\Delta f = \pm 15$ kHz	V_i	typ. 45	45 μV
$\Delta f = \pm 75$ kHz	V_i	typ. 20	20 μV
S+N/N = 46 dB; without de-emphasis; C_{5-6} = 220 pF			
$\Delta f = \pm 15$ kHz	V_i	typ. 65	65 μV
$\Delta f = \pm 75$ kHz	V_i	typ. 30	30 μV
Signal plus noise-to-noise ratio; with filter:			
B = 250 Hz to 16 kHz; V_i = 1 mV			
with de-emphasis			
$\Delta f = \pm 15$ kHz	S+N/N	typ. 74	76 dB
$\Delta f = \pm 75$ kHz	S+N/N	typ. 88	90 dB
without de-emphasis			
$\Delta f = \pm 15$ kHz	S+N/N	typ. 68	70 dB
$\Delta f = \pm 75$ kHz	S+N/N	typ. 82	84 dB
Noise output voltage; weighted conform DIN45405			
with de-emphasis			
$V_i = 0$	V_{no}	typ. 7	12 mV
V_i = 1 mV	V_{no}	typ. 30	50 μV
A.M. rejection; with filter: B = 700 Hz to 5 kHz			
f_m = 70 Hz; $\Delta f = \pm 15$ kHz (for f.m.);			
f_m = 1 kHz; m = 0,3 (for a.m.); simultaneously modulated			
V_i = 0,3 mV	α	typ. 52	52 dB
V_i = 1 mV	α	typ. 40	40 dB
V_i = 10 mV	α	typ. 52	52 dB
V_i = 100 mV	α	typ. 43	43 dB
Zero crossing shift of f.m. detector curve (see note)			
f_m = 70 Hz; $\Delta f = \pm 75$ kHz (for f.m.);		typ. 4	7 kHz
f_m = 1 kHz; m = 85% (for a.m.)	$\Delta f = \lvert f_{o1} - f_{o2} \rvert$	$<$ 9	15 kHz
Detector input impedance	Z_{3-4}	4,4 kΩ//2,25 pF	
Output resistance	R_{5-11};R_{6-11}	typ. 3,3	3,3 kΩ

Note

Zero crossing shift is defined as the difference between frequencies f_{o1} at V_i = 1 mV and f_{o2} at V_i = 30 μV.

CHARACTERISTICS (continued)

			$V_P = 8$ V	$V_P = 15$ V	
Side response suppression					
Input voltage for 10 dB side response suppression at S1 = 'on' adjust R1, so $V_{10\text{-}16} = 1,3$ V at $V_i = 0$; S1 = 'off'; R4 = 3,9 kΩ	$V_{i(rms)}$	typ.	35	30	μV
Side response suppression level $\Delta f = \pm 15$ kHz; $V_{i(rms)} = 1$ mV					
control voltage for $\Delta V_o = -1$ dB	$V_{12\text{-}16}$	typ.	0,7	0,7	V
control voltage for $\Delta V_o = -10$ dB	$V_{12\text{-}16}$	typ.	1,1	1,1	V
Muting					
Output signal muting at S2 = 'on'; reference signal at S2 = 'off'; $V_{i(rms)} = 1$ mV; $\Delta f = \pm 75$ kHz; R4 = 3,9 kΩ	ΔV_o	typ.	−80	−80	dB
Field-strength indication					
Output voltages (d.c. value) $V_i = 0$; $I_{8\text{-}9} = 0$; $R_{8\text{-}16} = 4,3$ kΩ	$V_{9\text{-}16}$	typ.	1,75	1,85	V
	$V_{8\text{-}16}$	typ.	1,90	2,00	V
Field-strength indicator current $R_{indicator} = 2$ kΩ; adjust R2 so $I_{8\text{-}9} = 0$ at $V_i = 0$ and R3 = 0 measured at $V_{i(rms)} = 120$ mV	$I_{8\text{-}9}$	>	130	140	μA
		typ.	190	210	μA
Output resistance	R_o	typ.	810	850	Ω
	$R_{9\text{-}16}$	typ.	3,7	3,7	kΩ
Stereo decoder switching voltage					
Reference voltage; without load: $I_7 = 0$	$V_{7\text{-}16}$	typ.	2,05	2,25	V
Output voltage; $I_{10} = I_{10max}$	$V_{10\text{-}16}$	typ.	1,70	1,90	V
Available output current	$-I_{10\,max}$	typ.	0,45	0,85	mA
Output voltage as a function of the i.f. input voltage $R_{10\text{-}16} = 3,9$ kΩ; R1 = 5 kΩ	$\dfrac{\Delta V_{10\text{-}16}}{20 \log \frac{V_{i1}}{V_{i2}}}$	typ.	−0,9	−1,2	V/20dB
Input voltage for $V_{10\text{-}16} = 0,8$ V adjust R1 so $V_{10\text{-}16} = 1,3$ V at $V_{i(rms)} = 0$	$V_{i(rms)}$	typ.	98	100	μV
		<	150	200	μV
Input voltage for $V_{10\text{-}16} = 1,3$ V adjust R1 so $V_{10\text{-}16} = 0,8$ V at $V_{i(rms)} = 3$ mV	$V_{i(rms)}$	>	−	0,5	mV
		typ.	1,3	1,3	mV
		<	−	1,75	mV
Input resistance (pin 7)	$R_{7\text{-}16}$	typ.	4	4,7	kΩ

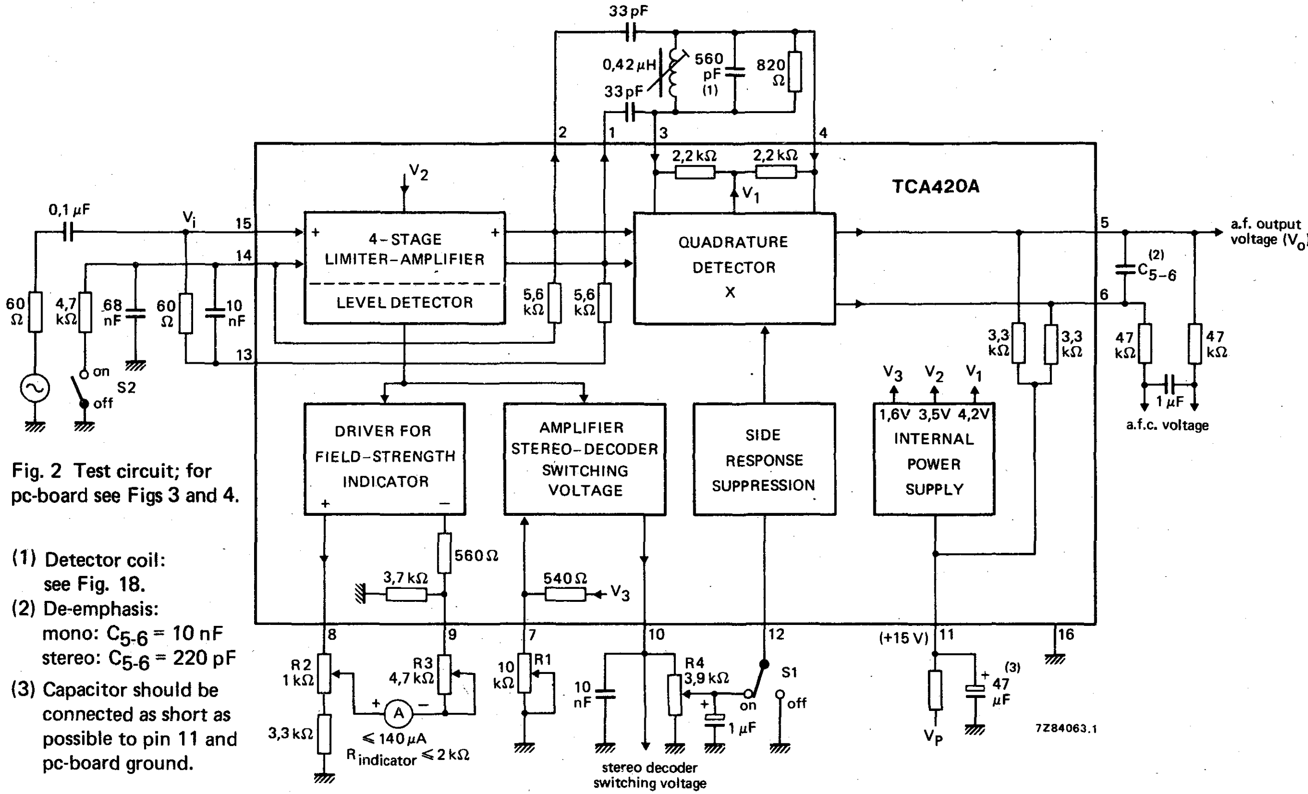
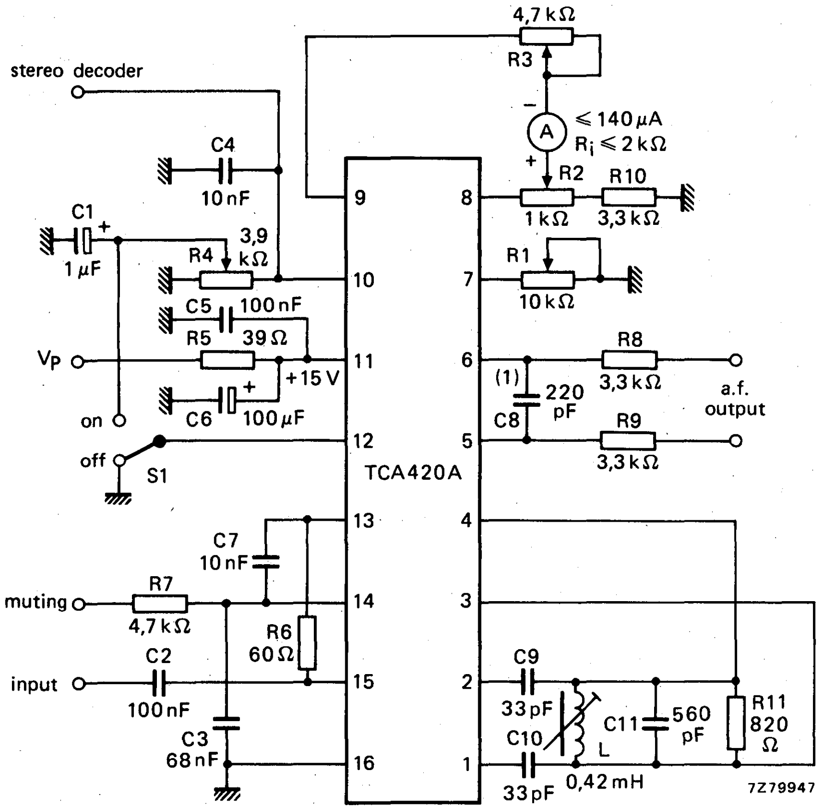


Fig. 2 Test circuit; for pc-board see Figs 3 and 4.

(1) Detector coil: see Fig. 18.
(2) De-emphasis:
mono: $C_{5\text{-}6}$ = 10 nF
stereo: $C_{5\text{-}6}$ = 220 pF
(3) Capacitor should be connected as short as possible to pin 11 and pc-board ground.

R1 = preset potentiometer for adjusting output voltage $V_{10\text{-}16}$ for mono/stereo switching of stereo decoder.
R2 = preset potentiometer for adjusting the zero level of the field-strength indicator current.
R3 = preset potentiometer for adjusting the maximum level of the field-strength indicator current.
R4 = preset potentiometer for adjusting the side response suppression.

S1 = side response suppression switch.
S2 = output signal muting switch.



(1) $C_8 = C_{5\text{-}6}$ (see Fig. 2).
For mono: C8 = 10 nF.
For stereo: C8 = 220 pF.

Fig. 3 Circuit diagram showing components arrangement for printed-circuit board (Fig. 4). The circuit is similar to the test circuit of Fig. 2.

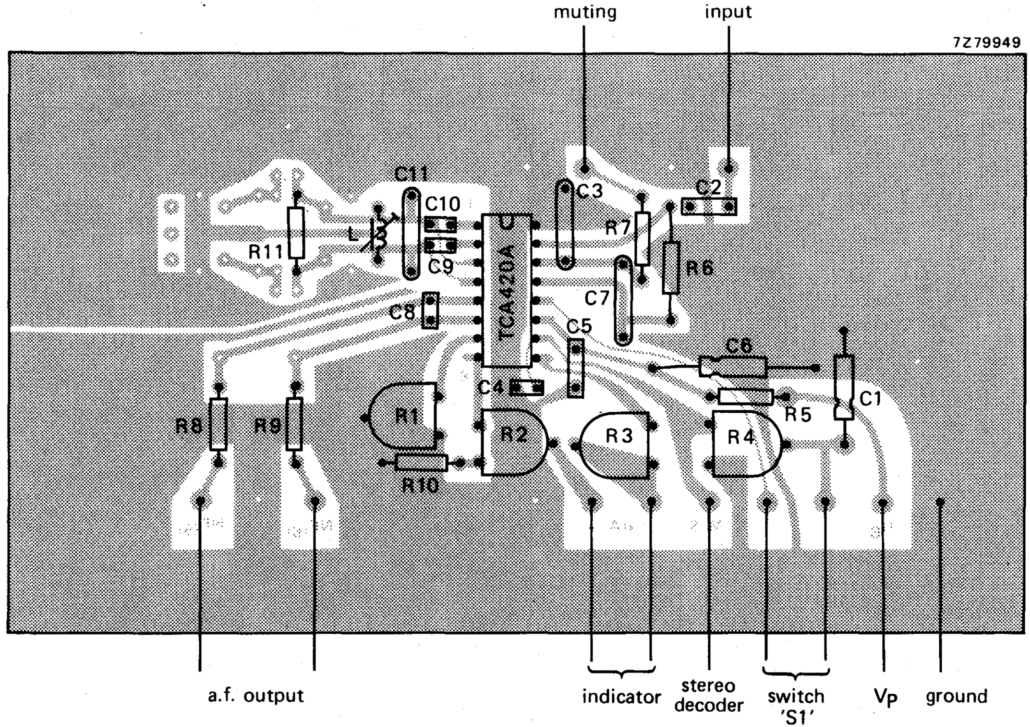


Fig. 4 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 3.

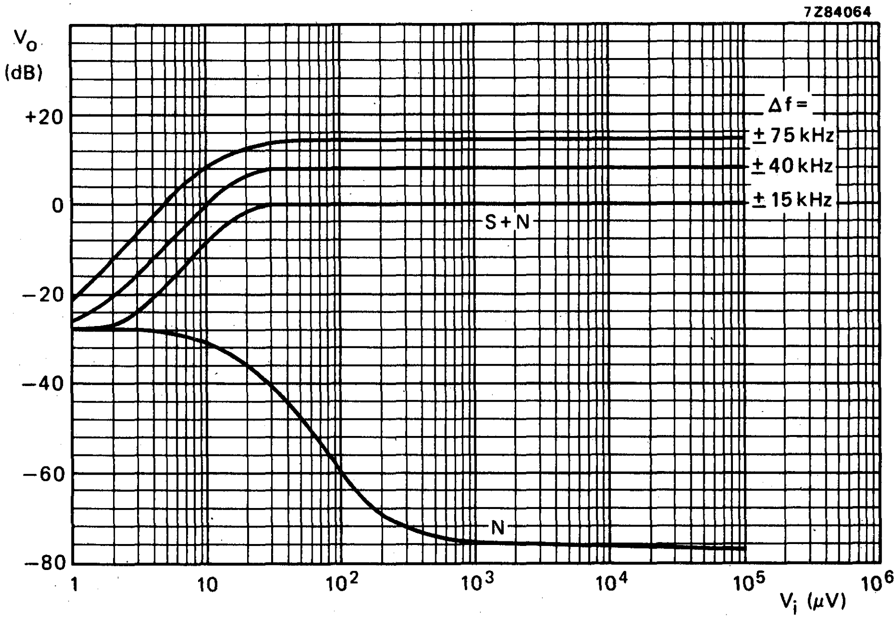


Fig. 5 V_P = 15 V; f_m = 1 kHz; B = 250 Hz to 16 kHz; typical values.

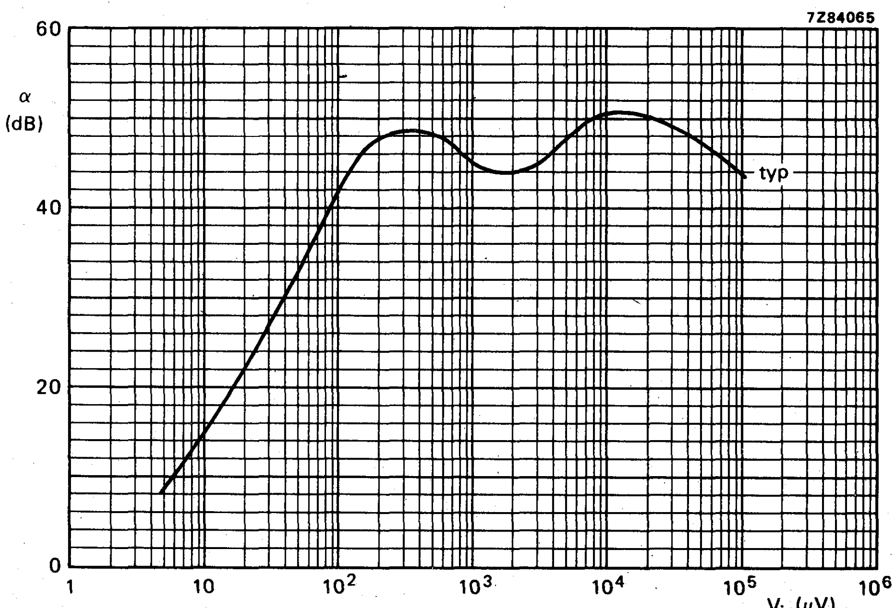


Fig. 6 A.M. rejection; f.m.: Δf = ±15 kHz; f_m = 70 Hz.
a.m.: m = 30%; f_m = 1 kHz; simultaneously modulated.

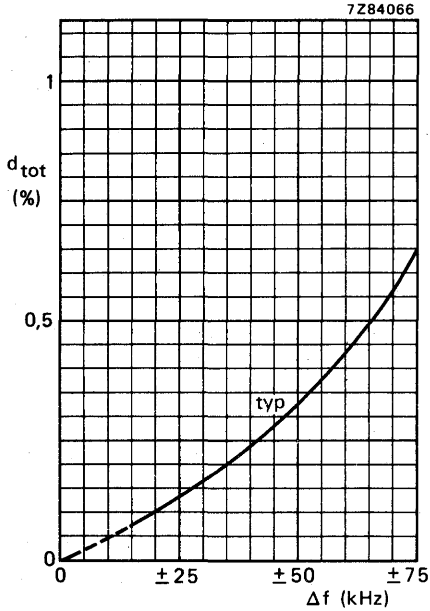


Fig. 7 Total distortion as a function of frequency deviation; single tuned circuit with $Q_L = 20$; $f_m = 1$ kHz; $C_{5\text{-}6} = 220$ pF.

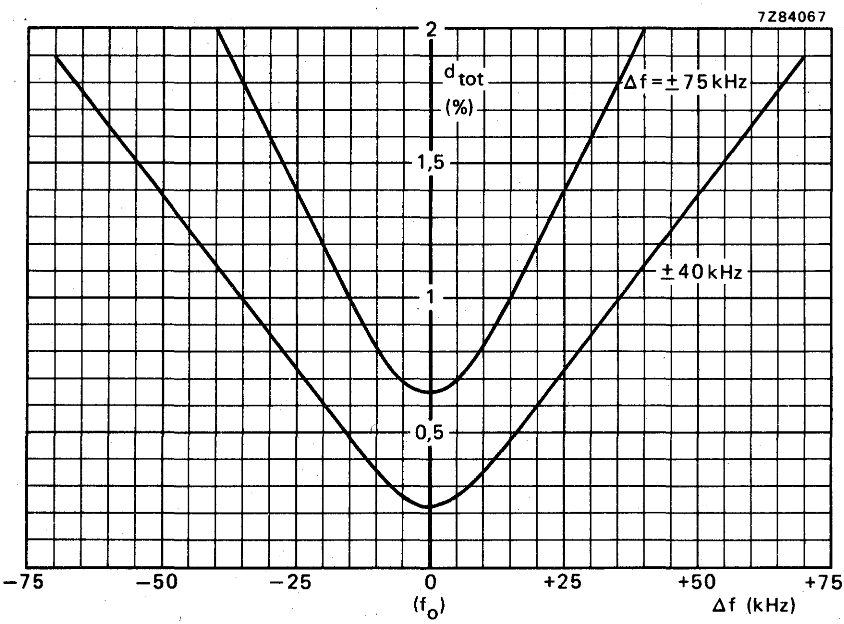


Fig. 8 Total distortion as a function of detuning; single tuned circuit with $Q_L = 20$; $f_m = 1$ kHz; $C_{5\text{-}6} = 220$ pF.

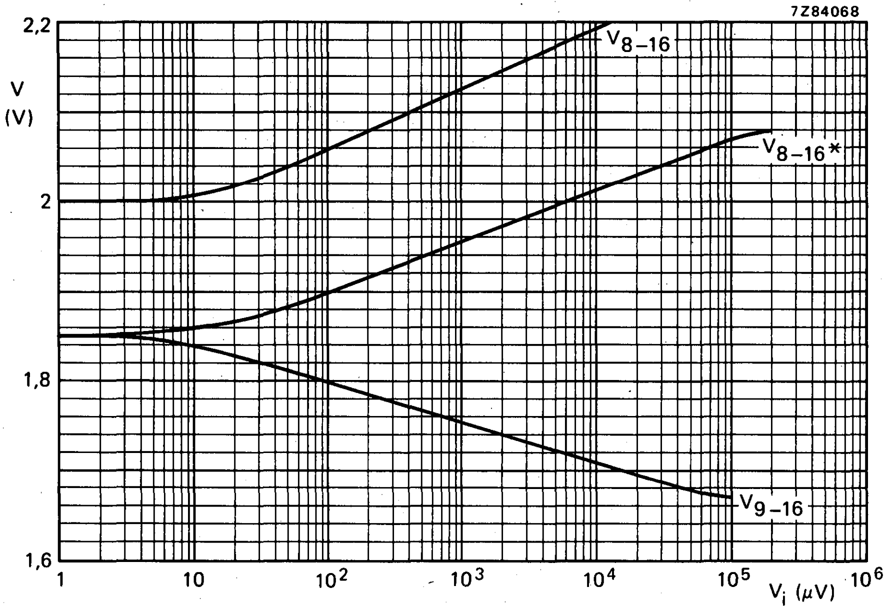


Fig. 9 Field-strength indication output voltages as a function of i.f. input voltage; R2 adjusted so $V_{8\text{-}9} = 0$ at $V_i = 0$; $R_{indicator} + R2 = 2\ k\Omega$; for $V_{8\text{-}16}$* definition see Fig. 11.

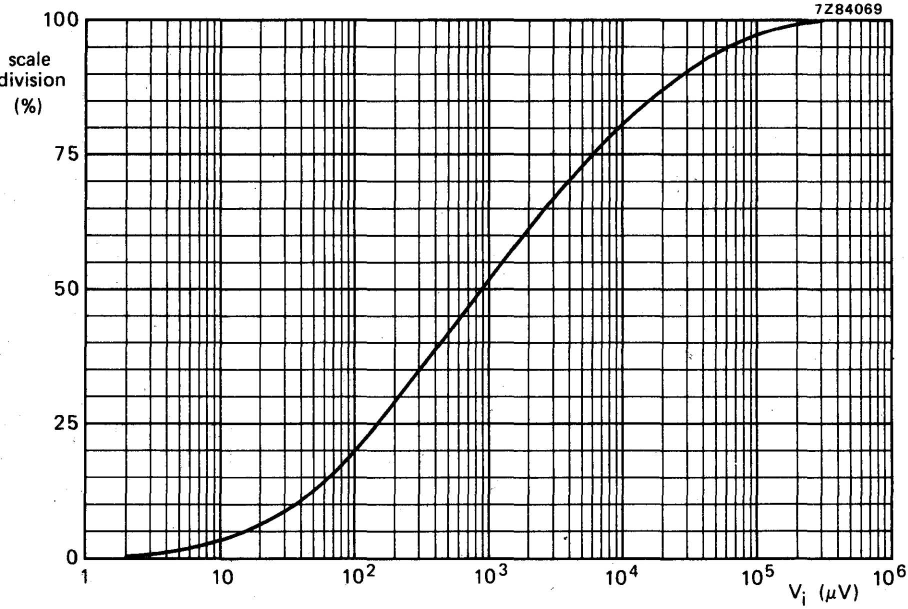


Fig. 9 Scale division of indicator as a function of i.f. input voltage; R2 adjusted so $V_{8\text{-}9} = 0$ at $V_i = 0$; $R_{indicator} = 2\ k\Omega$; R3 adjusted at indication 100%; indicator current = 140 μA; see Fig. 11.

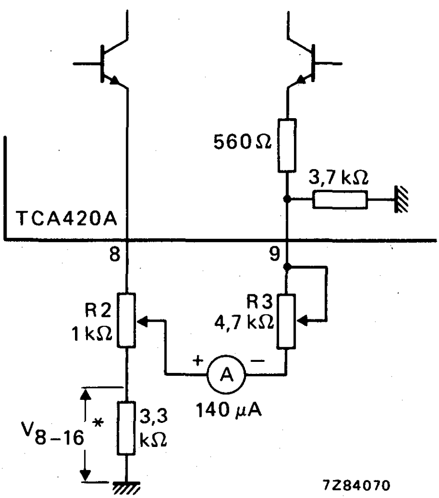


Fig. 11 Circuit diagram showing field-strength indicator adjustment components.

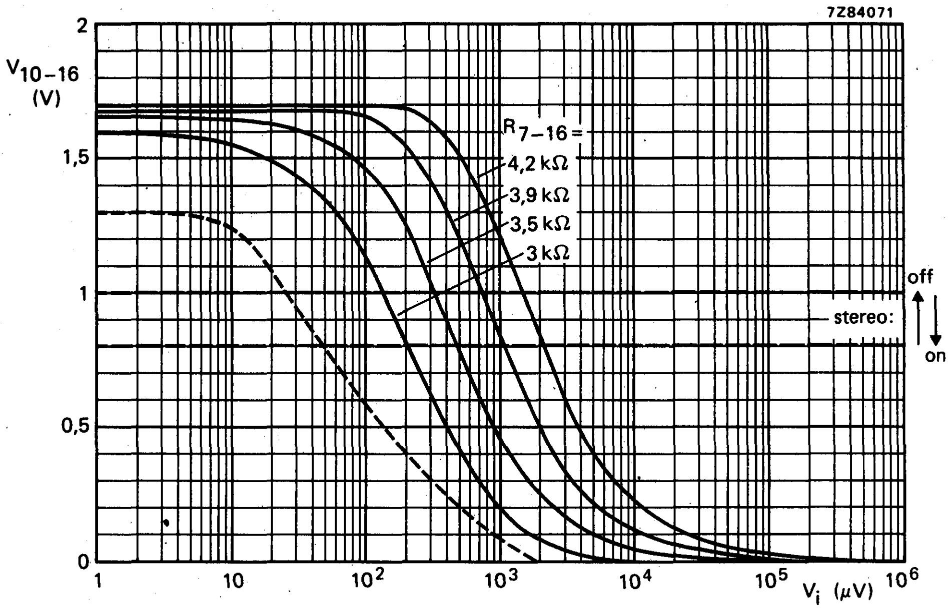


Fig. 12 Stereo decoder switching voltage as a function of i.f. input voltage; R4 = 3,9 kΩ; ––––– R1 adjusted so $V_{10\text{-}16}$ = 0 at V_i = 0; see Fig. 13.

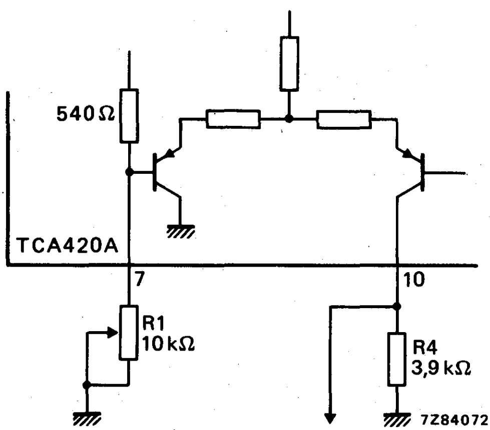


Fig. 13 Circuit diagram showing stereo decoder switching voltage adjustment.

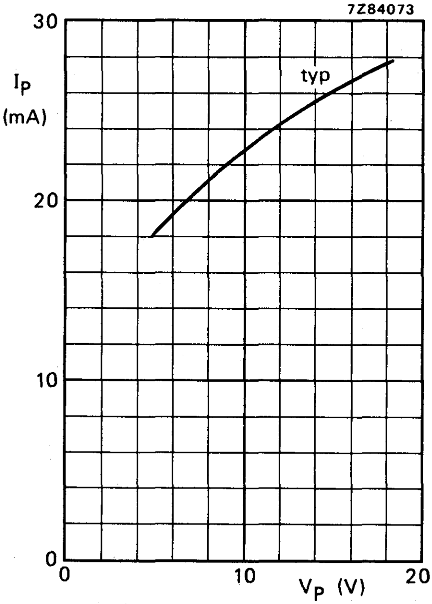


Fig. 14 Supply current consumption.

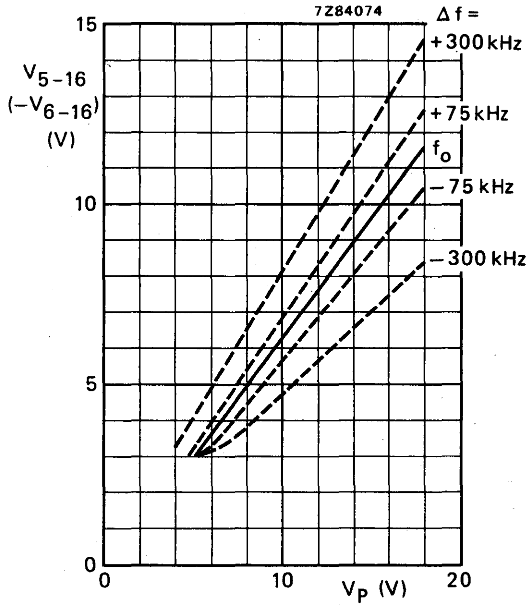


Fig. 15 Output voltage range.

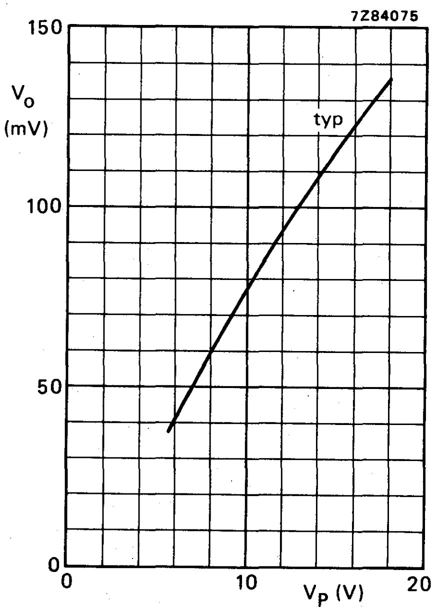


Fig. 16 A.F. output voltage; $\Delta f = \pm 15$ kHz; $f_m = 1$ kHz; $V_i = 1$ mV.

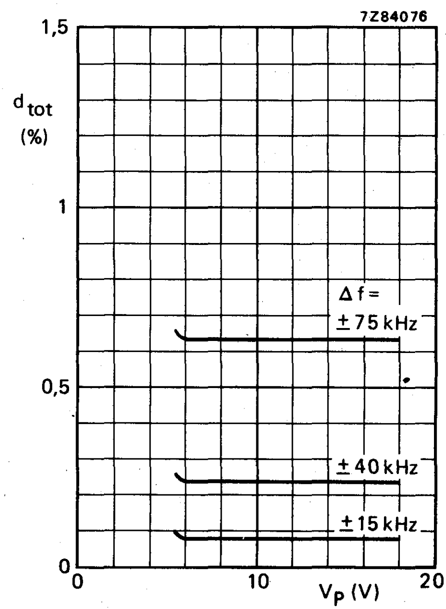


Fig. 17 Total distortion; $f_m = 1$ kHz; $V_i = 1$ mV; $C_{5-6} = 220$ pF.

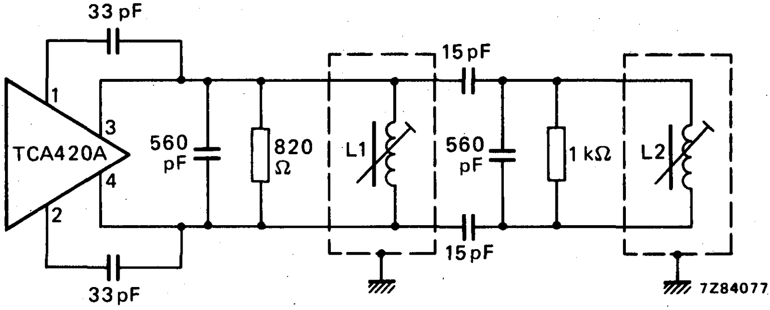


Fig. 18 Example of the TCA420A when using a detector with two tuned circuits; f_o = 10,7 MHz; L1 = L2 ≈ 0,4 μH; Q_o = 70.

Adjustment of the detector:
When having an i.f. input signal on top of the limiter capability, L2 should be detuned, L1 should be adjusted to minimum distortion, and then L2 to minimum distortion.

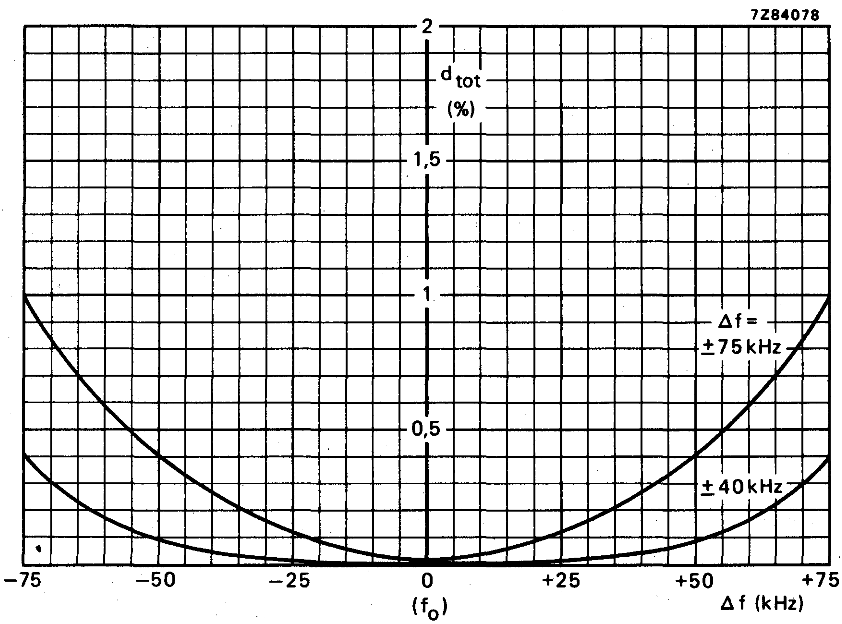


Fig. 19 Total distortion as a function of detuning; circuit as Fig. 18; f_m = 1 kHz; $C_{5\text{-}6}$ = 220 pF. V_o = 500 mV for a frequency deviation Δf = ±75 kHz and $d_{tot} < 0{,}1\%$.

APPLICATION INFORMATION

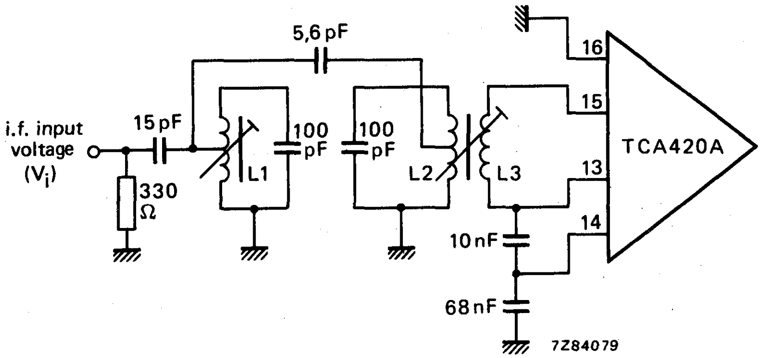


Fig. 20 I.F. coupling circuit, using LC filter; L1 = L2 = 7 + 7 turns h.f. litz wire (5 x 0,04); L3 = 3 turns h.f. litz wire wound on L2 (5 x 0,04).

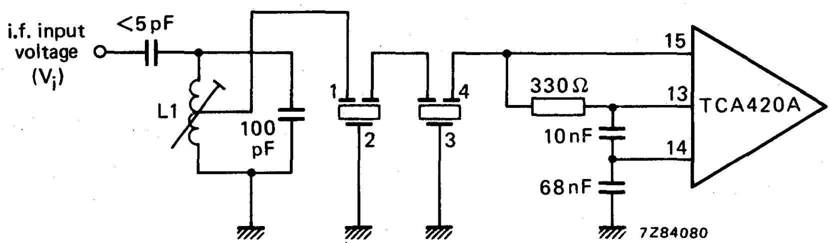
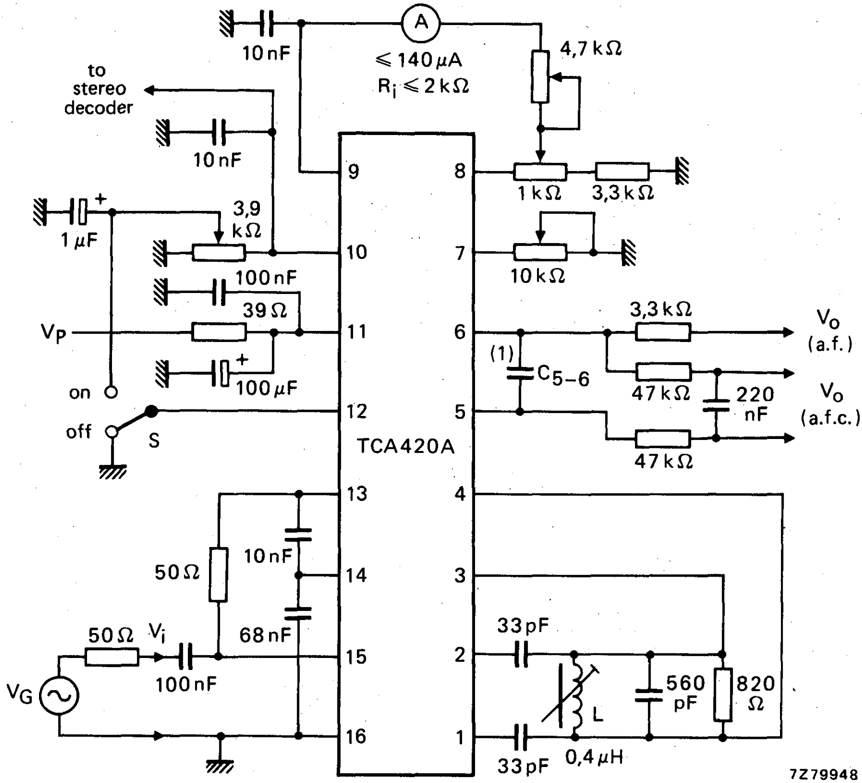


Fig. 21 I.F. coupling circuit, using ceramic filter; L1 = 14 turns h.f. litz wire (5 x 0,04), tab at 3 turns.

APPLICATION INFORMATION (continued)



(1) For mono: $C_{5\text{-}6}$ = 10 nF.
For stereo: $C_{5\text{-}6}$ = 220 pF.

Fig. 22 Application example of using TCA420A.

INTEGRATED VOLTAGE STABILIZER

The TCA530 is an adjustable 30 V integrated circuit voltage stabilizer for use with variable capacitance diodes.
The circuit features: continuous short-circuit protected output, a.f.c. control voltage input, internal switch-on delay (can be adjusted externally), pre-stabilization and crystal temperature control (temperature sensor and heater).

QUICK REFERENCE DATA

Input (supply) voltage range (for R_i = 3,3 kΩ)	$V_I = V_P$		50 to 68	V
Output voltage	$V_O = V_{6\text{-}16}$	typ.	30	V
Amplitude range of output voltage for a.f.c.	$\Delta V_{6\text{-}16}$	typ.	± 0,75	V
Variation of output voltage as a function of:				
input (supply) voltage variations	$\Delta V_{6\text{-}12}/\Delta V_I$	typ.	−0,2	mV/V
output current variations	$\Delta V_{6\text{-}12}/\Delta I_6$	typ.	0,5	mV/mA
temperature variations	$\Delta V_{6\text{-}12}/\Delta T_{amb}$	typ.	0,1	mV/K
heater voltage variations	$\Delta V_{6\text{-}12}/\Delta V_{1\text{-}16}$	typ.	0,2	mV/V
Output current	$I_6 - I_Q$	typ.	3,0	mA
Allowable output voltage range	$V_O = V_{6\text{-}16}$		25 to 30 ± 0,75	V
Allowable output current range	I_6		0 to 4,6	mA

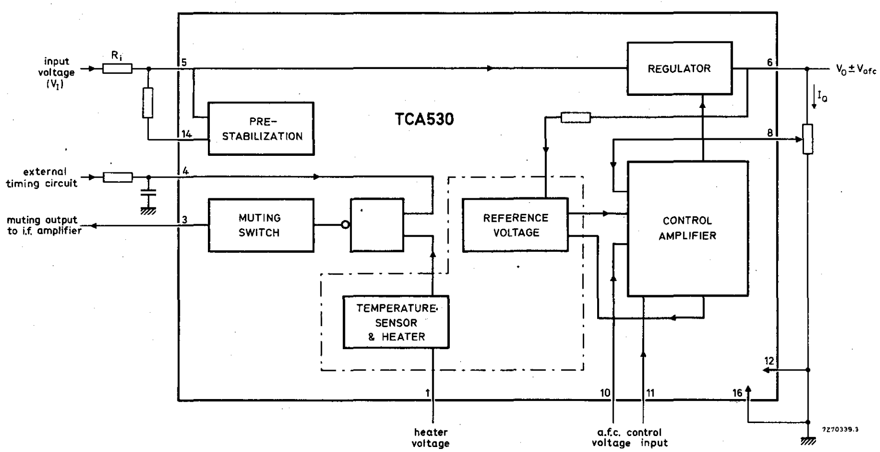


Fig. 1 Block diagram.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages: pin 1 (heater voltage)	$V_{1\text{-}16}$		0 to 20	V
pin 3 (muting switch supply)	$V_{3\text{-}16}$	max.	15	V
pins 10 and 11 (a.f.c. input control voltage)	$\pm V_{10\text{-}11}$	max.	6	V
Currents: pin 3	$\pm I_3$	max.	5	mA
pin 4	I_4	max.	500	µA
pin 5	I_5	max.	25	mA
pin 6	I_6	max.	30	mA
pin 8	I_8	max.	500	µA
pin 10	I_{10}	max.	500	µA
pin 11	I_{11}	max.	500	µA
pin 14	I_{14}	max.	15	mA
Total power dissipation (excluding heater power) at T_{amb} = 60 °C	P_{tot}	max.	500	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−20 to + 80	°C

CHARACTERISTICS

$V_{6\text{-}12}$ = 30 V; $V_{10\text{-}12}$ = $V_{11\text{-}12}$ = 10 V; $V_{1\text{-}16}$ = 15 V; T_{amb} = 25 °C; measured in Fig. 3.

Voltage control

Input (supply) voltage range* R_i = 3,3 kΩ; I_6 = 3,5 mA	$V_I = V_P$		50 to 68	V
Current consumption	I_P	typ.	8,1	mA
			5,2 to 11,0	mA
	I_5	typ.	I_6 + (1,1 ± 0,3)	mA
Regulator voltage drop within operating range of the pre-stabilizer	$V_{5\text{-}6}$	typ.	2,7	V
			2 to 3,5	V
outside operating range of the pre-stabilizer**	$V_{5\text{-}6}$	<	6	V
Output current (start of current limiting)	I_6	>	8	mA
Internal reference voltage	$V_{8\text{-}12}$	typ.	20	V
			18,2 to 21,8	V

* For other input (supply) voltage ranges and output currents, the series resistor R_i has to be altered (see also Fig. 2).

** The specified output voltage dependency of the input (supply) voltage is not guaranteed outside the operating range of the pre-stabilizer.

Input current of control amplifier	I_8	typ. <	0,5 μA 1 μA
Variation of output voltage as a function of *			
input (supply) voltage variations	$\Delta V_{6\text{-}12}/\Delta V_I$	typ.	0,2 mV/V
output current variations	$\Delta V_{6\text{-}12}/\Delta I_6$	typ.	0,5 mV/mA
temperature variations	$\Delta V_{6\text{-}12}/\Delta T_{amb}$	typ.	0,1 mV/K
heater voltage variations	$\Delta V_{6\text{-}12}/\Delta V_{1\text{-}16}$	typ.	0,2 mV/V
Hum suppression at f = 50 Hz			
between input (supply) voltage and pin 6		typ.	80 dB
between pins 5 and 6		typ.	60 dB
between pins 1 and 6		typ.	80 dB
Output noise voltage at f = 10 Hz to 15 kHz (r.m.s. value)	$V_{n(rms)}$	<	50 μV

A.F.C. control amplifier

Common mode input voltage range	$V_{10\text{-}12} = V_{11\text{-}12}$		6,0 to 18,0 V
Common mode rejection ratio	CMRR	typ.	60 dB
Input current	$I_{10} = I_{11}$	typ. <	0,1 μA 0,5 μA
Input resistance	$R_{i(10\text{-}11)}$	>	1 MΩ
Ratio between output voltage variation and a.f.c. input voltage variation	$\Delta V_{6\text{-}12}/\Delta V_{10\text{-}11}$		1,2 : 1
Amplitude range of output voltage	$\Delta V_{6\text{-}12}$	typ.	± 0,75 V ± 0,5 to ± 1,0 V

Muting switch

When the crystal temperature has reached approximately its stationary final value, the output of the muting switch (pin 3) becomes high-ohmic. The switching of pin 3 can be delayed by an external RC-circuit at pin 4 or by a switching voltage.

Muting switch ON (pin 3 low-ohmic)			
Input voltage	$V_{4\text{-}16}$	<	8 V
Input current	I_4	typ.	1 μA
Output saturation voltage at I_3 = 1 mA	$V_{3\text{-}16\,sat}$	typ. <	0,45 V 0,6 V
Muting switch OFF (pin 3 high-ohmic)			
Input voltage	$V_{4\text{-}16}$		8 to 11 V
Input current	I_4	>	0,1 μA
Output voltage	$V_{3\text{-}16}$	<	15 V
Output current	I_3	<	1 μA
Internal switch-on delay	t_d	<	3 s

* External component value changes are not taken into account.

CHARACTERISTICS (continued)

Crystal temperature control

Heater voltage range	V_{1-16}		8 to 20 V
Heater peak current at switching on	I_{1M}	typ. <	230 mA 300 mA
Continuous heater current at V_{1-16} = 15 V	I_1	typ. <	40 mA 55 mA
Continuous heater power	P_h	typ.	600 mW

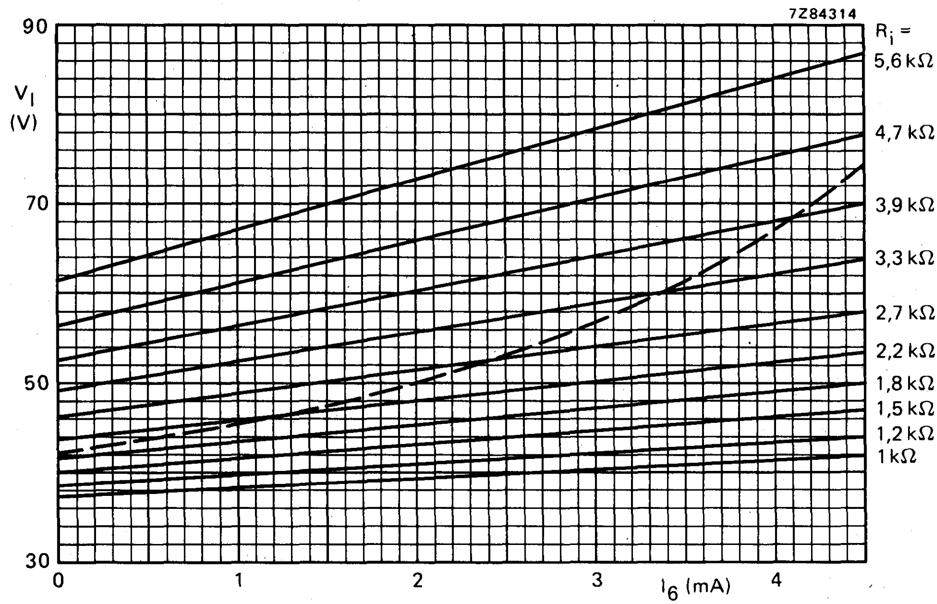
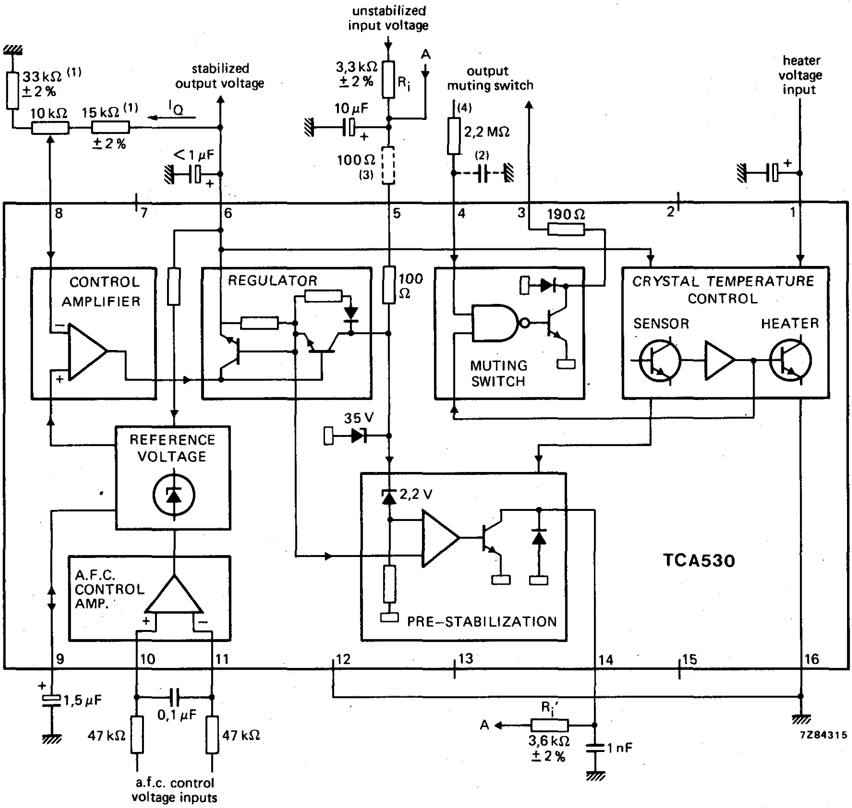


Fig. 2 Curves to obtain R_i-values for various input (supply) voltages and/or output currents. Conditions: V_{6-12} = 30 V; tolerance of I_6 = ± 20%; R_{5-14} = 3,6 kΩ; tolerance of R_i = ± 2%. Above the dotted curve a tolerance of V_I (V_P) of ± 15% is allowed.



(1) It is recommended that fixed resistors of the same kind be used for the voltage divider.
The voltage divider of Fig. 4 can be used when a narrow temperature dependency is required.
(2) This capacitor can be applied to increase the internal delay.
(3) This resistor is recommended when the IC is not soldered on a printed-circuit board.
(4) Can be connected to pin 6, for example.

Fig. 3 Test circuit.

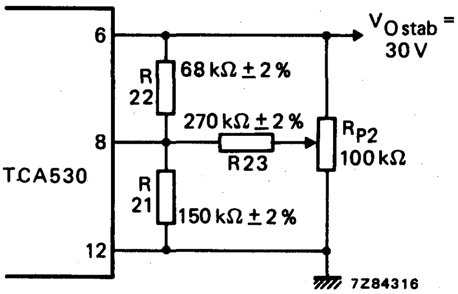


Fig. 4 Voltage divider for the narrowest possible temperature dependency.

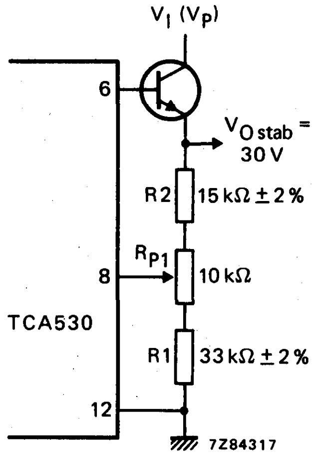


Fig. 5 Circuit extension by means of a series transistor at the output, for output currents > 4,6 mA.

The following table gives some resistor value examples for various output voltages with $\Delta R/R \leqslant \pm$ 2% and $\Delta R_P/R_P \leqslant \pm$ 20%.

V_{Ostab} V	R_{P2} kΩ	R21 kΩ	R22 kΩ	R23 kΩ	R_{P1} kΩ	R1 kΩ	R2 kΩ
30 30	100 47	200 180	82 82	300 300	10 47	20 100	10 47
29					22	39	18
28 28	100 47	220 300	75 100	300 430	22	39	15
27					47	68	24
26					22	27	8,2
25 25	100 47	560 620	91 100	390 430	47	47	12

The series resistors R_i and R_i' (see Fig. 3), as well as the input (supply) voltage V_I (V_P), have to be adapted to the chosen output voltages V_{Ostab}.

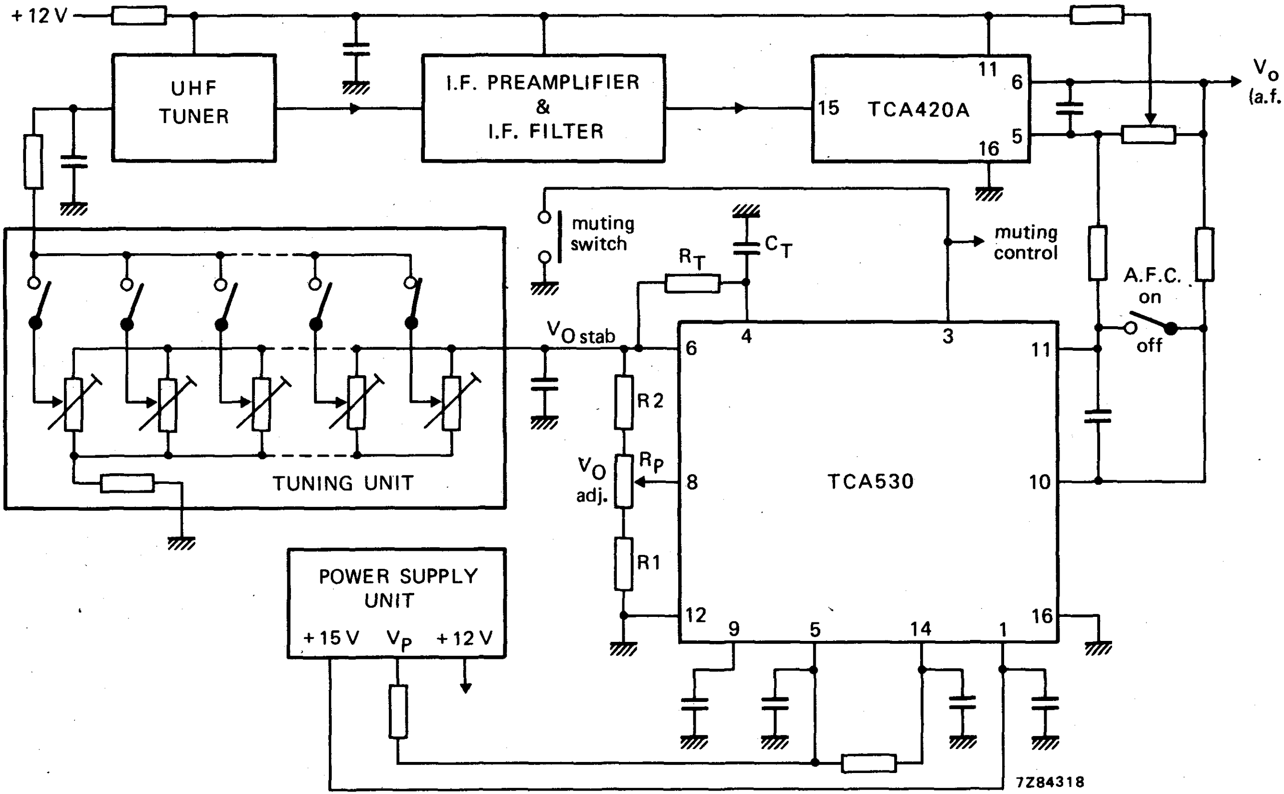


Fig. 6 Application example; f.m. receiver with TCA530 and TCA420A.

D.C. VOLUME AND BALANCE STEREO CONTROL CIRCUIT

The TCA730A is a monolithic integrated circuit for controlling volume and balance in stereo amplifiers by means of a d.c. voltage.

Features:

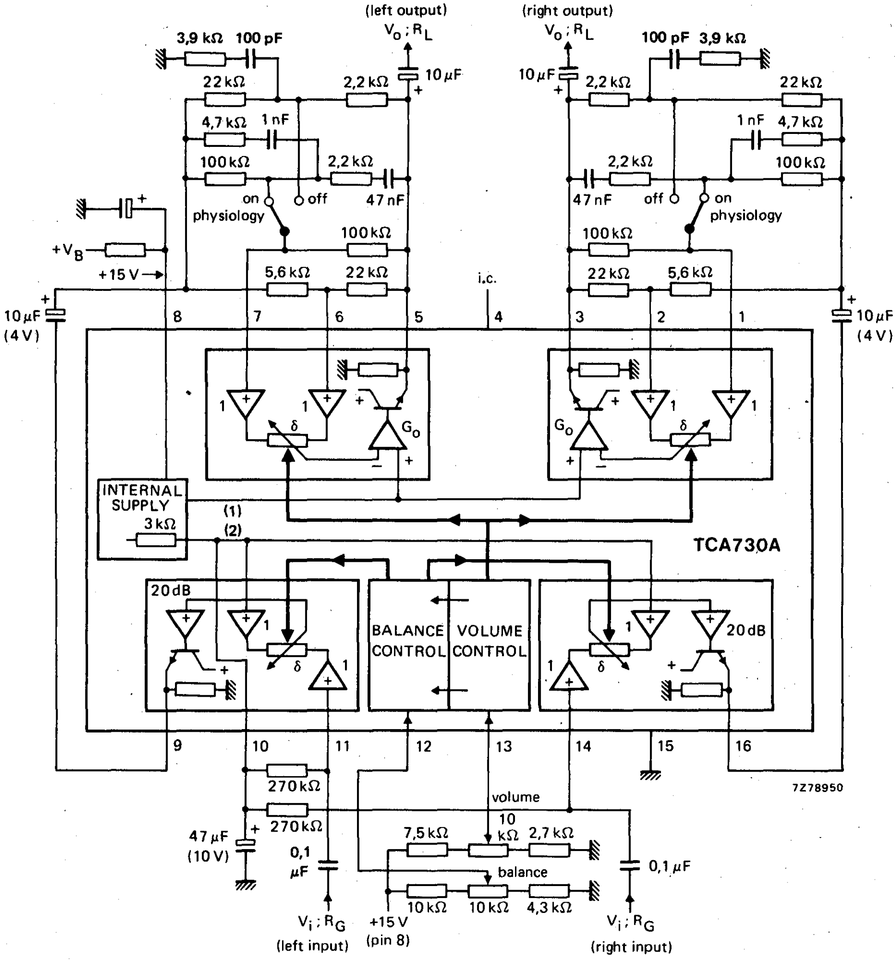
- physiological volume control
- balance control
- internal amplifier
- high-ohmic signals inputs
- internal supply voltage stabilization
- converter for the control voltage

QUICK REFERENCE DATA

Supply voltage (pin 8)	V_P	typ.	15	V
Supply current (pin 8)	I_P	typ.	35	mA
Input voltage range (r.m.s. value)	$V_{i(rms)}$		0,1 to 1,7	V
Nominal input voltage; m = 1 (r.m.s. value)	$V_{i(rms)}$	typ.	0,5	V
Input resistance	R_i	typ.	250	kΩ
Output voltage at nominal output power (r.m.s. value)	$V_{o(rms)}$	typ.	1	V
Volume control range	G_v		+20 to −80	dB
Channel balance	ΔG_v	typ.	1	dB
Balance control range	G_v		+5 to −7	dB
Total distortion at $V_{o(rms)}$ = 1 V	d_{tot}	typ.	0,1	%
Channel separation	α	typ.	55	dB
Signal-to-noise ratio	S/N	typ.	67	dB
Frequency response (−1 dB)			20 Hz to 20	kHz
Volume control voltage range	$V_{13\text{-}15}$		2 to 9,5	V
Balance control voltage range	$V_{12\text{-}15}$		2,5 to 9,0	V
Supply voltage range (pin 8)	V_P		13,5 to 16,5	V
Ambient temperature range	T_{amb}		−30 to +80	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).



(1) $6{,}6\ V_{BE}$; $V_1 = 4{,}6$ V
(2) $0{,}35\ V_P + 0{,}65\ V_{BE}$; $V_2 = 5{,}7$ V.

Fig. 1 Block diagram with external circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	V_P	max.	18	V
Input voltages	$V_{11\text{-}15}$; $V_{14\text{-}15}$	min.	0	V
		max.	V_P	V
Control voltages	$V_{12\text{-}15}$; $V_{13\text{-}15}$	min.	−5	V
		max.	12	V
Total power dissipation	P_{tot}	max.	900	mW
Storage temperature range	T_{stg}		−55 to +150	°C
Operating ambient temperature range	T_{amb}		−30 to +80	°C

CHARACTERISTICS

$V_P = 15$ V; $T_{amb} = 25$ °C; measured in Fig. 1; balance control in mid-position ($V_{12\text{-}10} = 0$); physiology switch off; f = 1 kHz; $R_G = 22$ kΩ; $R_L = 5{,}6$ kΩ; unless otherwise specified.

Supply voltage range (pin 8)	V_P		13,5 to 16,5	V
Supply current	I_P	typ.	35	mA
			25 to 43	mA
Control range				
Voltage gain range	G_v		0 to 20	dB
Voltage gain at $V_{13\text{-}15} = 9{,}5$ V (0,63 V_P)	G_v	typ.	20	dB
			18 to 22	dB
Voltage attenuation range	G_v		0 to −80	dB
Voltage attenuation at $V_{13\text{-}15} = 3$ V (0,2 V_P)	G_v	>	−75	dB
		typ.	−80	dB
Balance control range at $G_v = -10$ dB			+ 5 to −7	dB
Control inputs				
Recommended control voltage range				
volume	$V_{13\text{-}15}$		2 to 9,5	V
balance	$V_{12\text{-}15}$		2,5 to 9,0	V
Control voltage for $G_v = -10$ dB; $V_{12\text{-}10} = 0$	$V_{13\text{-}15}$		6,7 to 7,1	V*
Control voltage for balance 0 dB; $V_{13\text{-}15} = 6{,}9$ V	$V_{12\text{-}10}$	typ.	0 ± 0,2	V
Internal supply voltage (0,35 V_P + 0,65 V_{BE})	$V_{10\text{-}15}$	typ.	5,9	V
			5,7 to 6,1	V
Output resistance (pin 10)	R_{o10}	typ.	3	kΩ
Control current				
volume ($V_{13\text{-}15} = 6{,}9$ V)	I_{13}	typ.	15	μA
		<	50	μA
balance ($V_{12\text{-}15} = 5{,}9$ V)	I_{12}	typ.	8	μA
		<	25	μA
Input resistance				
pin 13 (volume)	R_{i13}	typ.	500	kΩ
pin 12 (balance)	R_{i12}	typ.	600	kΩ

* Typical value 6,9 V.

CHARACTERISTICS (continued)

Signal processing

Frequency response (–1 dB)	f	20 Hz to 20		kHz
Input resistance; $R_{11\text{-}10} = R_{14\text{-}10} = 270\ k\Omega$ (pins 11; 14)	$R_{i11;14}$	typ.	250	kΩ
Output resistance (pins 3; 5)	$R_{o3;5}$	typ.	10	Ω
Maximum input voltage; $V_{o(rms)} < 1$ V; $d_{tot} = 0{,}7$ % (r.m.s. value)	$V_{i(rms)}$	>	1,3	V
		typ.	1,7	V
Maximum output voltage; $V_{i(rms)} < 1$ V; $d_{tot} = 0{,}7$% (r.m.s. value)	$V_{o(rms)}$	>	1,8	V
		typ.	2,0	V
Nominal input voltage; m = 1 (r.m.s. value)	$V_{i(rms)}$	typ.	0,5	V
Nominal output voltage at nominal output power (r.m.s. value)	$V_{o(rms)}$	typ.	1	V
Total distortion				
$V_{o(rms)} = 1$ V; G_v = maximum	d_{tot}	typ.	0,07	%
		<	0,2	%
$V_{o(rms)} = 1$ V; $V_{i\ (rms)} = 1$ V	d_{tot}	typ.	0,2	%
$V_{o(rms)} = 50$ mV; $V_{i(rms)} = 150$ mV	d_{tot}	typ.	0,03	%
		<	0,1	%
$V_{o(rms)} = 50$ mV; $V_{i(rms)} = 1$ V	d_{tot}	typ.	0,2	%
Output noise voltage; f = 20 Hz to 20 kHz				
signal plus noise voltage (r.m.s. value)				
$G_v = -60$ dB	$V_{no(rms)}$	typ.	6	μV
$G_v = -10$ dB	$V_{no(rms)}$	typ.	15	μV
G_v = maximum (+20 dB)	$V_{no(rms)}$	typ.	100	μV
noise voltage; weighted conform DIN45405 (peak value)				
$G_v = -60$ dB	$V_{no(m)}$	typ.	15	μV
$G_v = -10$ dB	$V_{no(m)}$	typ.	35	μV
		<	80	μV
G_v = maximum (+20 dB)	$V_{no(m)}$	typ.	230	μV
		<	350	μV
Channel separation; $G_v = \pm 20$ dB; $V_i = V_o < 1$ V				
f = 250 Hz to 12,5 kHz	α	>	52	dB
		typ.	53	dB
f = 40 Hz to 16 kHz	α	>	46	dB
		typ.	50	dB
Channel balance				
G_v = + 15 to –50 dB	ΔG_v	typ.	1	dB
		<	2	dB
$G_v < 50$ dB	ΔG_v	typ.	2	dB

Amplifier characteristics

Input resistance (pins 11 and 14)	$R_{i11;14}$	>	3 MΩ
D.C. output voltages			
(0,35 V_P – 1,35 V_{BE})	$V_{3\text{-}15}$; $V_{16\text{-}15}$	typ.	4,2 V
(6,6 V_{BE})	$V_{3\text{-}15}$; $V_{16\text{-}15}$	typ.	4,6 V
Quiescent input currents (pins 1,2,6,7,11,14)	I_1; I_2; I_6; I_7; I_{11}; I_{14}	typ. < 	0,5 μA 2 μA
Input resistance (pins 1,2,6 and 7) of physiology; without external circuitry	$R_{i1;2;6;7}$	>	1 MΩ
Internal load resistance at outputs (pins 3,5,9,16)	$R_{3\text{-}15}$; $R_{5\text{-}15}$; $R_{9\text{-}15}$; $R_{10\text{-}15}$	typ.	2 kΩ
Maximum gain; no load	$G_{3\text{-}1}$; $G_{3\text{-}2}$; $G_{5\text{-}6}$; $G_{5\text{-}7}$	> typ.	40 dB 43 dB

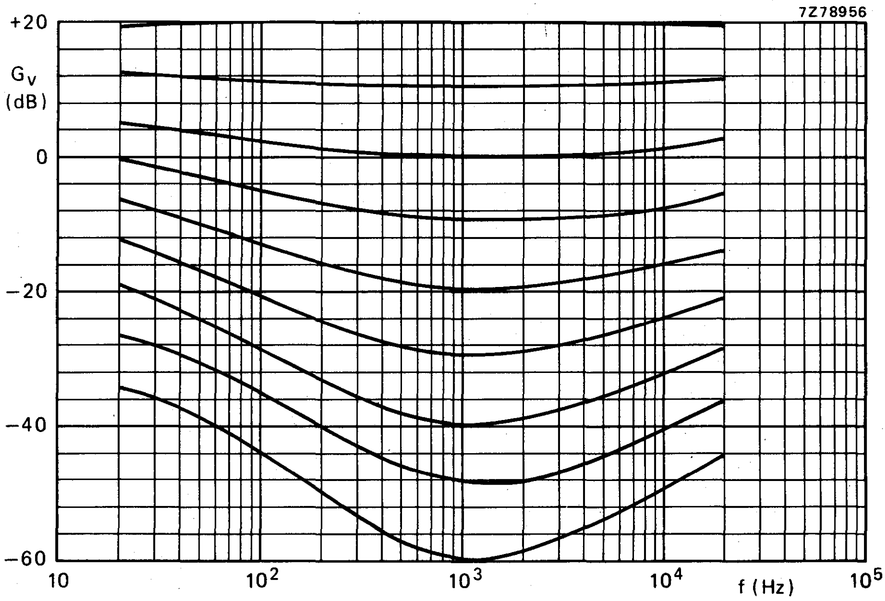


Fig. 2 Frequency response volume control with physiology.

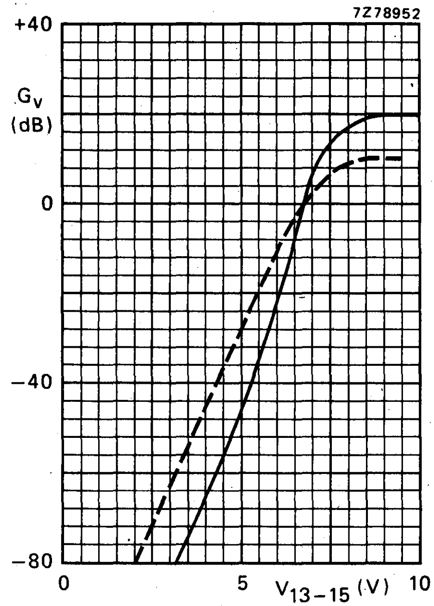
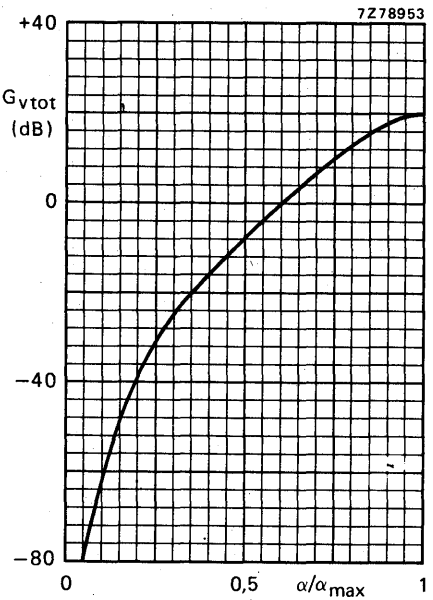


Fig. 3 Volume control curves; without physiology; balance = 0; $V_{12\text{-}10} = 0$.
—— $G_{v\ tot}$; $G_{v\ 5\text{-}11}$; $G_{v\ 3\text{-}14}$
--- $G_{v\ 9\text{-}11}$; $G_{v\ 16\text{-}14}$



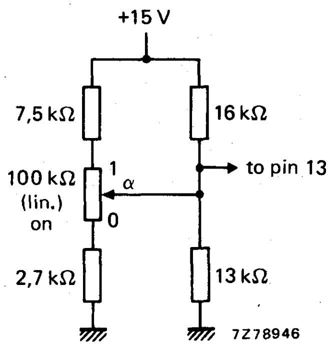


Fig. 4 Volume adjustment curve; balance = 0; $V_{12\text{-}10} = 0$.

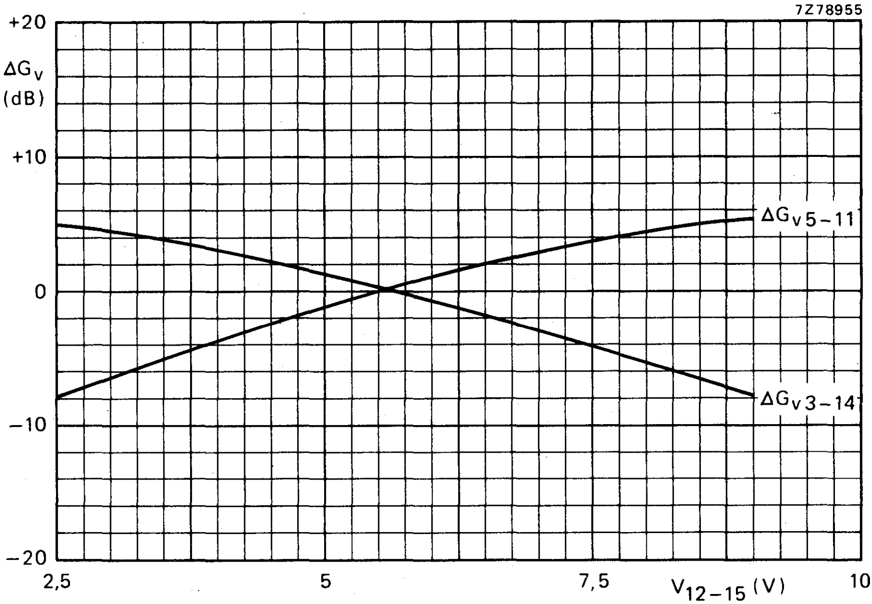


Fig. 5 Balance control curves; $G_{v\,tot} = -10$ dB ($V_{13\text{-}15} = 6{,}9$ V); for balance = 0.

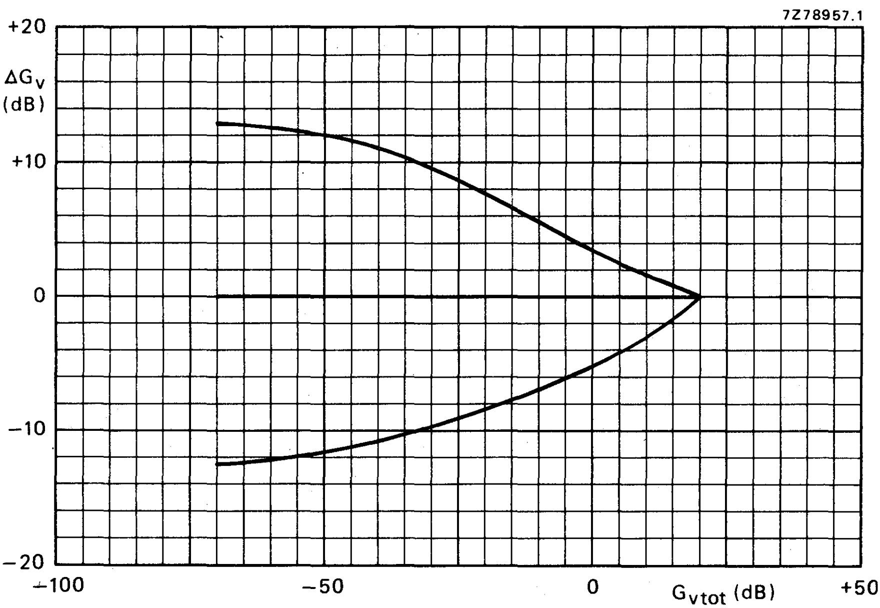
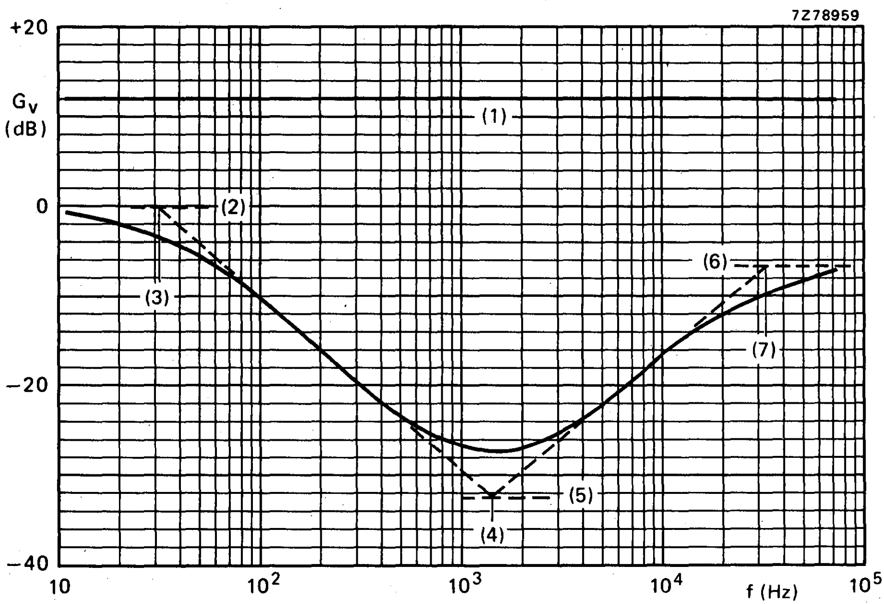


Fig. 6 Balance control range; $V_{12\text{-}15} = 2{,}5$ to $9{,}0$ V.



(1) $G_v = R2/R1$
(2) $G_v = R42/R31$
(3) $G_v = 1/2\pi \cdot R42 \cdot C42$
(4) $G_v = 1/2\pi \cdot R41 \cdot C31 = 1/2\pi \cdot R31 \cdot C31$
(5) $G_v \approx R41/R32$
(6) $G_v \approx R41/R32$
(7) $G_v = 1/2\pi \cdot R32 \cdot C31$

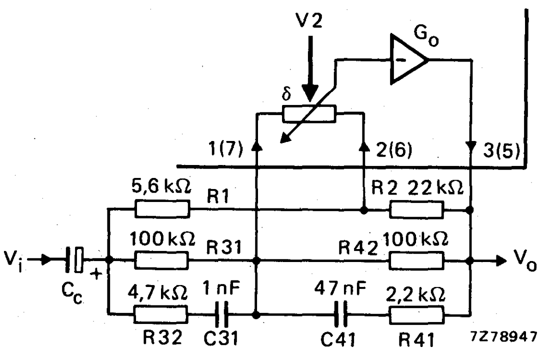


Fig. 7 Frequency response of the physiology part.

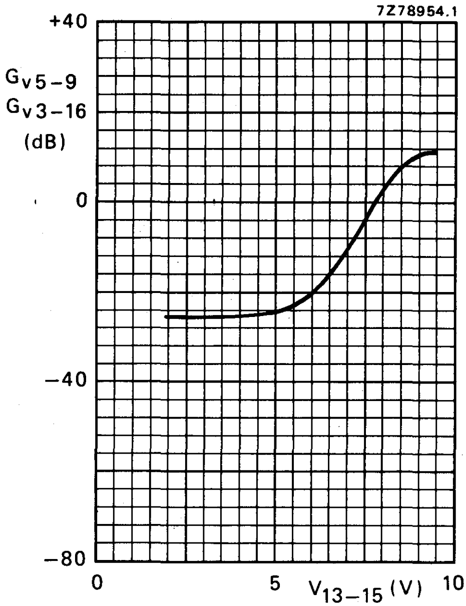


Fig. 8 Physiology control curve; f = 1 kHz; balance = 0; $V_{12\text{-}15}$ = 0.

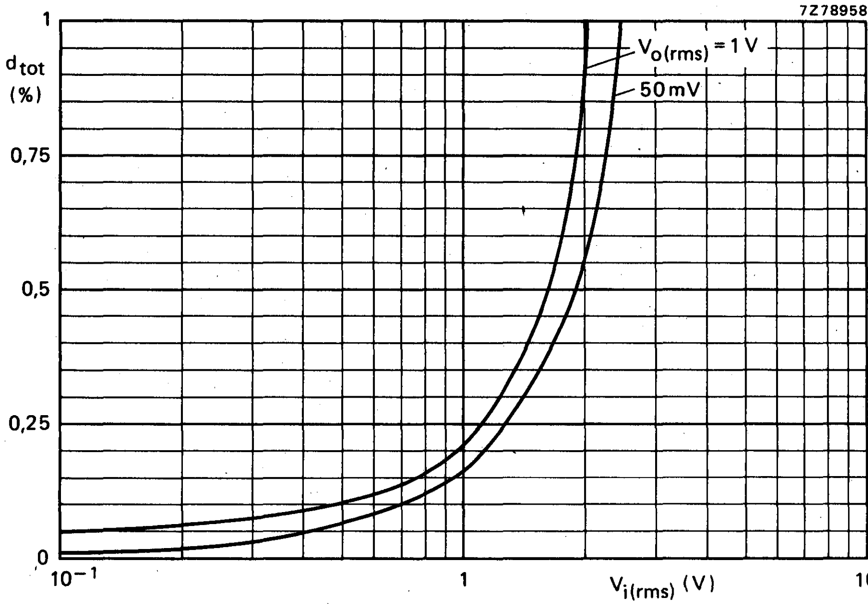


Fig. 9 Total distortion as a function of r.m.s. input voltage; f = 1 kHz; R_L = 5,6 kΩ.

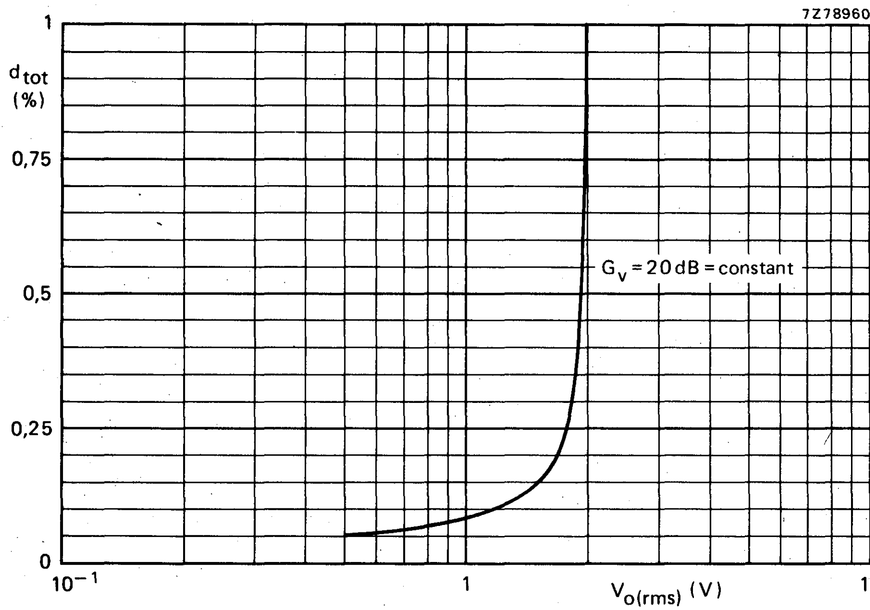


Fig. 10 Total distortion as a function of r.m.s. output voltage; f = 1 kHz; R_L = 5,6 kΩ.

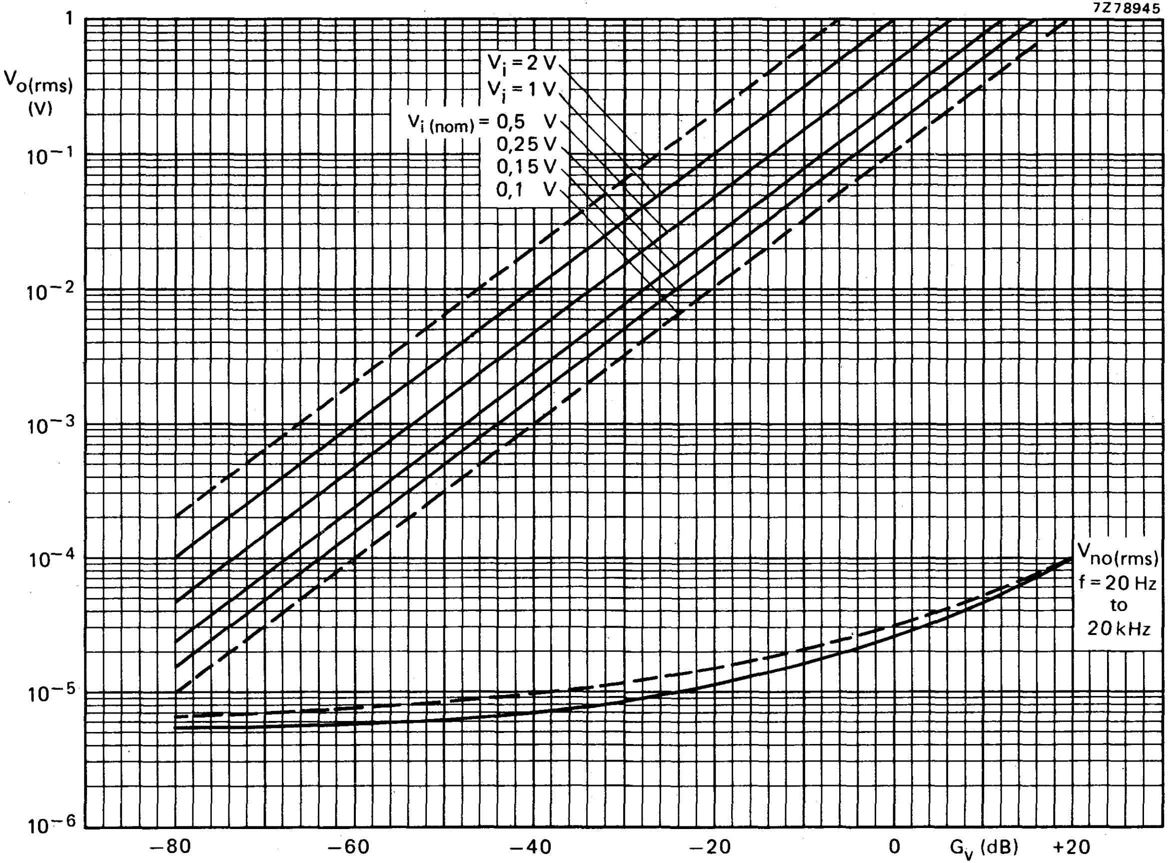
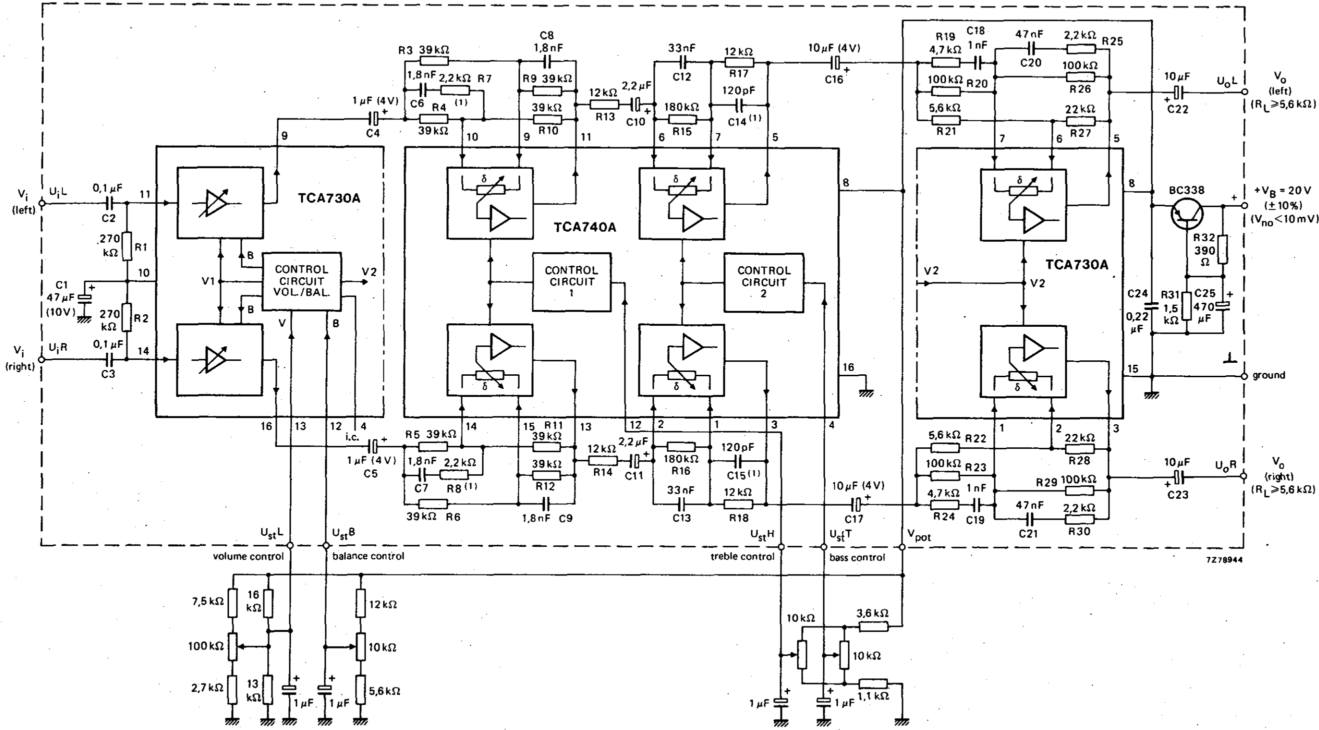


Fig. 11 The r.m.s. output voltage as a function of voltage gain; $P_{o(nom)}$ relative to $V_{o(rms)}$ = 1 V.
—— without physiological volume control; ––– with physiological volume control.

APPLICATION INFORMATION



(1) RC network for limiting treble boost (linear: $f_{-3\,dB} = 100\,kHz$).

Fig. 12 Application diagram for TCA730A and TCA740A. For printed-circuit board see Fig. 13.

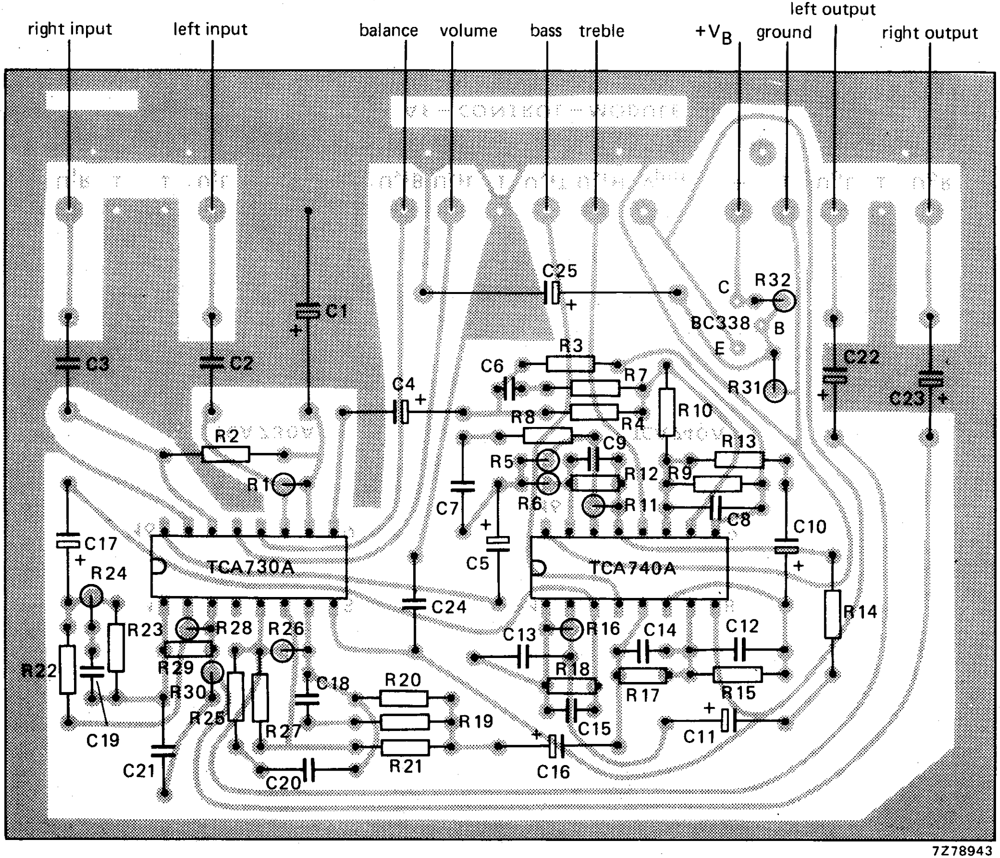
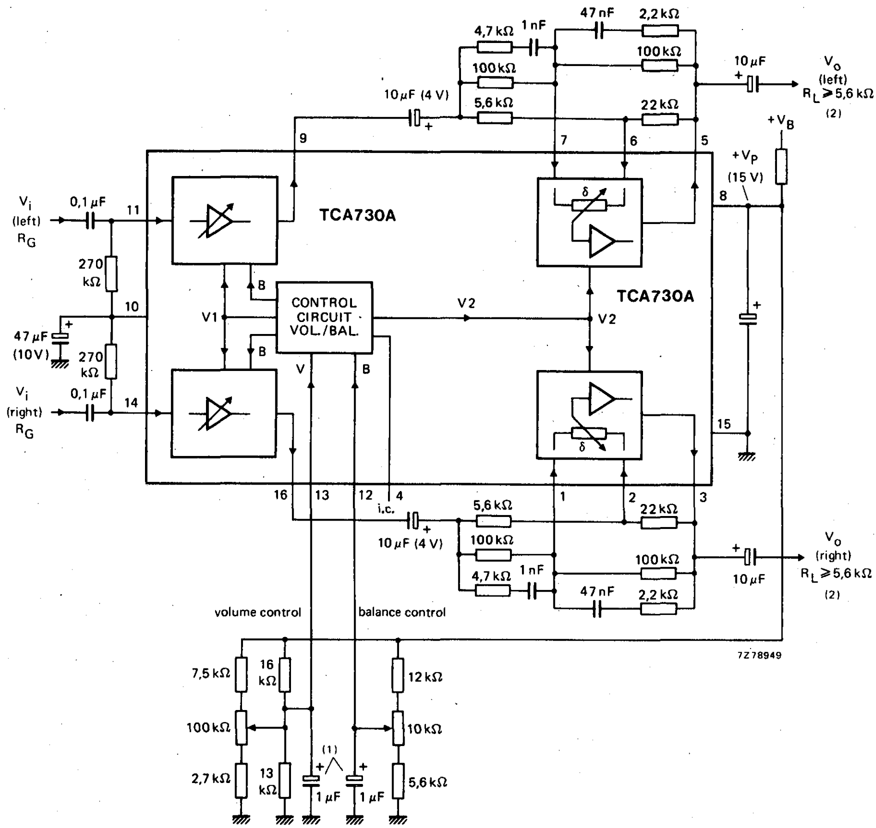


Fig. 13 Printed-circuit board component side, showing component layout; for circuit diagram see Fig. 12.

APPLICATION INFORMATION (continued)



(1) $C_{13\text{-}15} = C_{12\text{-}15} = 1\ \mu F$ are intended for suppression of the noise when adjusting the mechanical potentiometers.

(2) For rejecting noise, caused by switching on or off, corresponding muting switches can be used before or in the output power stage.

Fig. 14 Application example of TCA730A used for volume and balance control.

D.C. TREBLE AND BASS STEREO CONTROL CIRCUIT

The TCA740A is a monolithic integrated circuit for controlling treble and bass in stereo amplifiers by means of a d.c. voltage.
Features:

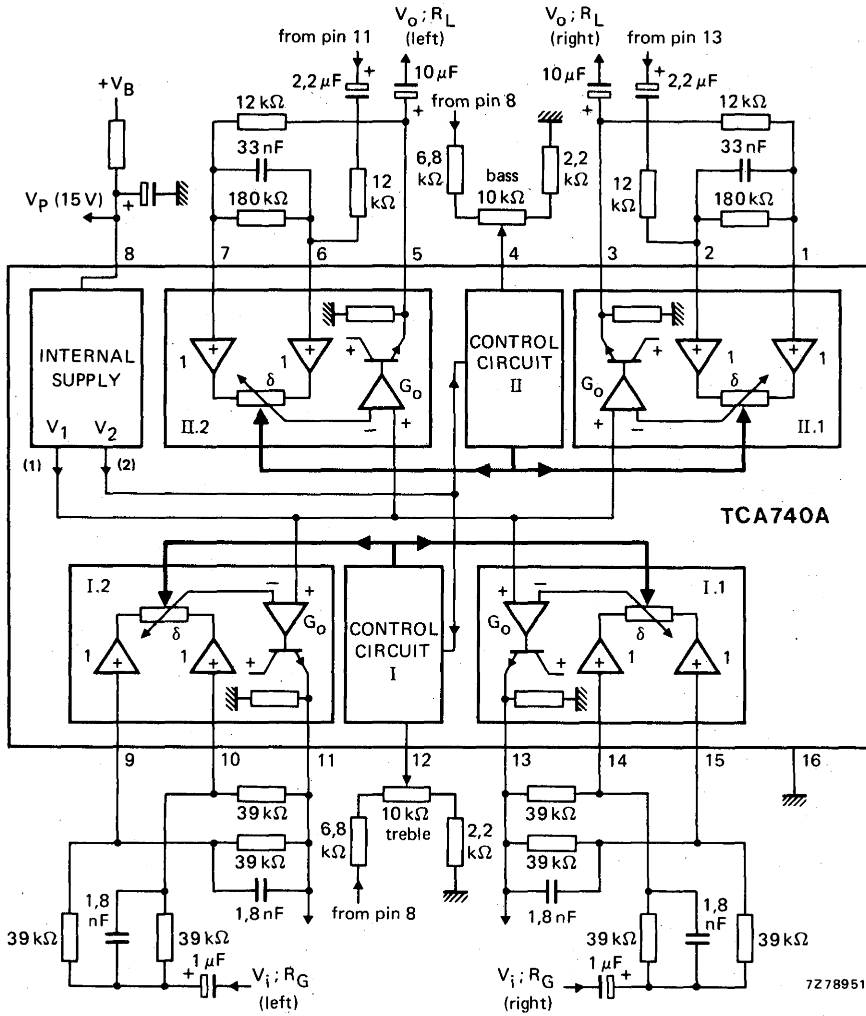
- two double potentiometer circuits
- feedback control
- internal amplifier
- high-ohmic signal inputs
- converter for the control voltages
- low-ohmic and short-circuit protected signal outputs

QUICK REFERENCE DATA

Supply voltage (pin 8)	V_P	typ.	15	V
Supply current (pin 8)	I_P	typ.	35	mA
Bass boost and cut at 40 Hz (ref. 1 kHz)		typ.	± 16	dB
Treble boost and cut at 16 kHz (ref. 1 kHz)		typ.	± 16	dB
Input/output voltage at d_{tot} = 0,7% (r.m.s. value)	$V_{i,o(rms)}$	typ.	2	V
Total distortion at $V_{o(rms)}$ = 1 V; linear frequency response	d_{tot}	typ.	0,1	%
Channel separation	α	typ.	70	dB
Output signal plus noise voltage (r.m.s. value)	$V_{no(rms)}$	typ.	45	μV
Frequency response (−1 dB)	f		20 Hz to 20	kHz
Treble/bass control voltage range	$V_{12\text{-}16}$; $V_{4\text{-}16}$		1,8 to 9,5	V
Supply voltage range (pin 8)	V_P		13,5 to 16,5	V
Ambient temperature range	T_{amb}		−30 to + 80	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).



(1) 6,6 V_{BE}; V_1 = 4,6 V

(2) 0,31 V_P + 1,4 V_{BE}; V_2 = 5,6 V

Fig. 1 Block diagram with external circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 8)	V_P	max.	18 V
Control voltages (pins 4 and 12)	$V_{4\text{-}16}$	max.	12 V
	$-V_{4\text{-}16}$	max.	5 V
	$V_{12\text{-}16}$	max.	12 V
	$-V_{12\text{-}16}$	max.	5 V
Total power dissipation	P_{tot}	max.	900 mW
Storage temperature range	T_{stg}		−55 to + 150 °C
Operating ambient temperature range	T_{amb}		−30 to + 80 °C

CHARACTERISTICS

V_P = 15 V; T_{amb} = 25 °C; measured in Fig. 1; in position 'linear' ($V_{4\text{-}16} = V_{12\text{-}16}$ = 5,6 V); R_G = 60 Ω; R_L = 5,6 kΩ; f = 1 kHz; unless otherwise specified

Supply voltage range (pin 8)	V_P		13,5 to 16,5 V
Supply current (pin 8)	I_P	typ.	34 mA
			25 to 45 mA

Signal processing

Voltage gain at linear frequency response	G_v	typ.	0 dB
Frequency response (−1 dB)	f		20 Hz to 20 kHz
Maximum gain variation at f = 1 kHz at maximum bass/treble boost or cut	ΔG_v	<	± 1,5 dB
Bass boost at 40 Hz (ref. 1 kHz) $V_{4\text{-}16}$ = 9,2 V		>	15 dB
		typ.	16 dB
Bass cut at 40 Hz (ref. 1 kHz) $V_{4\text{-}16}$ = 2 V		>	15 dB
		typ.	16 dB
Treble boost at 16 kHz (ref. 1 kHz) $V_{12\text{-}16}$ = 9,2 V		>	15 dB
		typ.	16 dB
Treble cut at 16 kHz (ref. 1 kHz) $V_{12\text{-}16}$ = 2 V		>	15 dB
		typ.	16 dB
Total distortion			
$V_{o(rms)}$ = 100 mV; f = 1 kHz	d_{tot}	typ.	0,03 %
$V_{o(rms)}$ = 100 mV; f = 40 Hz to 16 kHz	d_{tot}	typ.	0,1 %
$V_{o(rms)}$ = 1 V; f = 1 kHz	d_{tot}	typ.	0,07 %
		<	0,2 %
$V_{o(rms)}$ = 1 V; f = 40 Hz to 16 kHz	d_{tot}	typ.	0,2 %
Input/output voltage at d_{tot} = 0,7 % (r.m.s. value)	$V_{i(rms)} = V_{o(rms)}$	>	1,6 V
		typ.	2 V
Output signal plus noise voltage (r.m.s. value) f = 20 Hz to 20 kHz	$V_{no(rms)}$	typ.	40 μV
Output noise voltage; weighted conform DIN45405; peak value	$V_{no(m)}$	typ.	90 μV
		<	160 μV

CHARACTERISTICS (continued)

Channel separation			
f = 1 kHz	α	typ.	72 dB
f = 250 Hz to 12,5 kHz	α	typ.	68 dB
f = 40 Hz to 16 kHz	α	>	50 dB
		typ.	58 dB
Control voltages			
Recommended control voltage range		>	0 V
treble/bass	$V_{4-16} = V_{12-16}$		2 to 9,2 V
		<	0,66 V_P V
Control voltage at linear frequency response	$V_{4-16} = V_{12-16}$	typ.	5,6 V
			5,4 to 5,8 V
			(0,31 V_P to 1,4 V_{BE}) V
Quiescent input current			
$V_{4-16} = V_{12-16}$ = 2 to 9,2 V	$I_4 = I_{12}$	typ.	6 μA
		<	25 μA
Input resistance (pins 4 and 12)			
$V_{4-16} = V_{12-16}$ = 5,6 V	$R_{i4;12}$	typ.	800 kΩ
Amplifier characteristics			
Quiescent input currents; V_i = 4,6 V		typ.	0,6 μA
(pins 1, 2, 6, 7, 9, 10, 14 and 15)	$I_1;I_2;I_6;I_7;I_9;I_{10};I_{14};I_{15}$	<	2 μA
Input resistance (pins 1,2,6,7,9,10,14 and 15)	$R_{i\ 1;2;6;7;9;10;14;15}$	>	1 MΩ
Internal emitter resistance at outputs	$R_{3-16}; R_{5-16}; R_{11-16}; R_{13-16}$	typ.	2 kΩ
Output resistance (pins 3,5,11 and 13)	$R_{o\ 3;5;11;13-16}$	typ.	10 Ω
Maximum gain; no load	G_v	>	40 dB
		typ.	43 dB
D.C. output voltages			
$V_{4-16} = V_{12-16}$ = 5,6 V (pins 3,5,11 and 13)	$V_{3-16}; V_{5-16}; V_{11-16}; V_{13-16}$	typ.	4,6 V
			4,3 to 4,9 V
			(6,6 V_{BE}) V

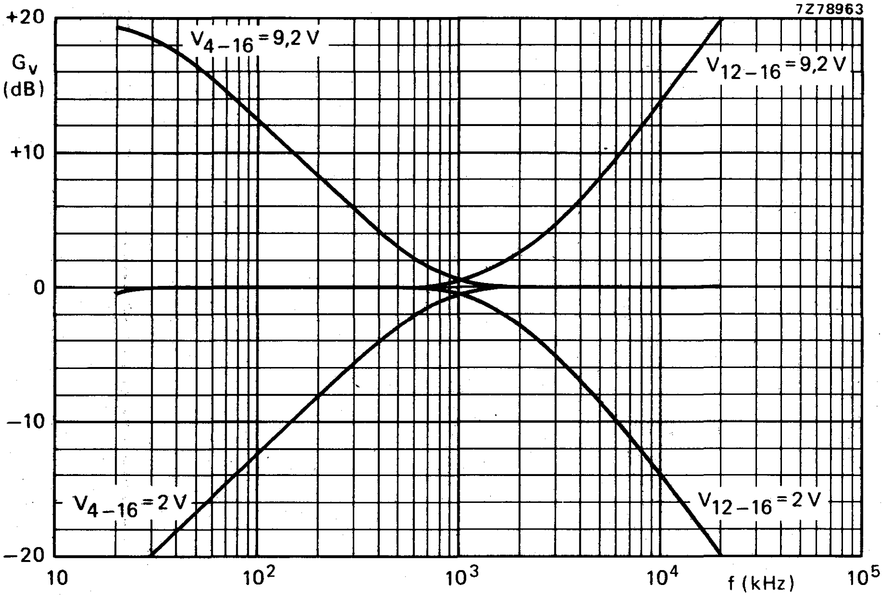


Fig. 2 Frequency response.

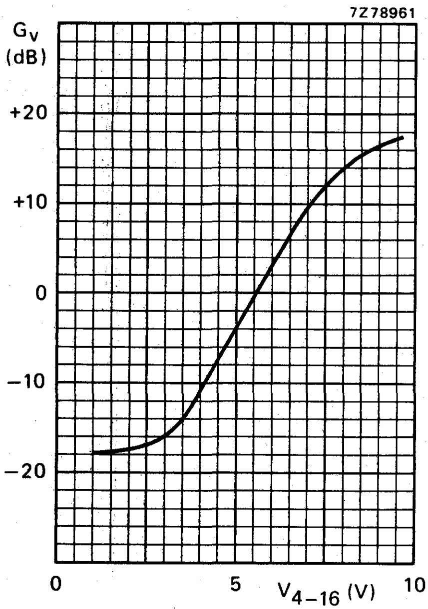


Fig. 3 Bass control curve at f = 40 Hz.

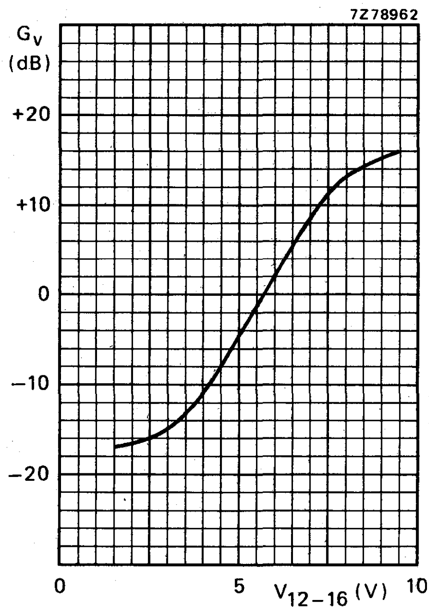


Fig. 4 Treble control curve at f = 16 kHz.

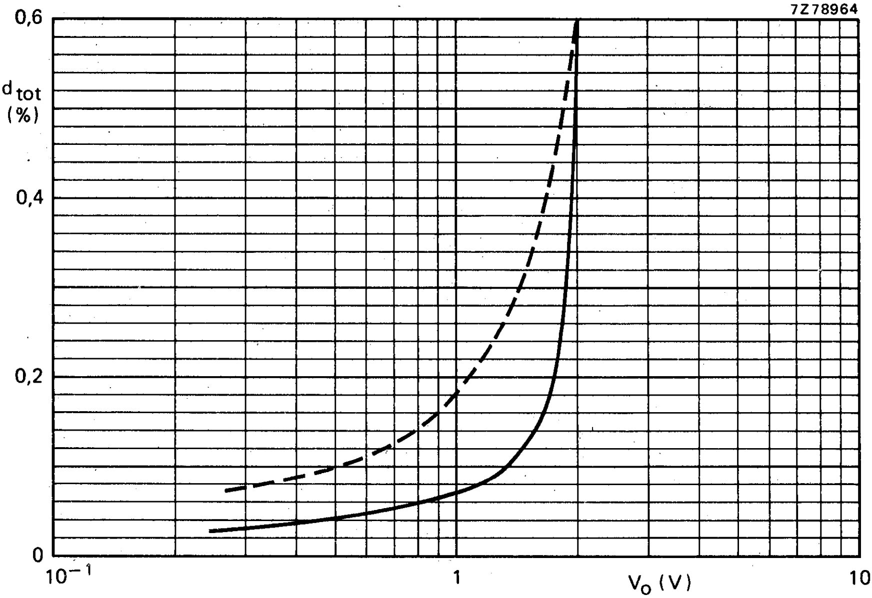
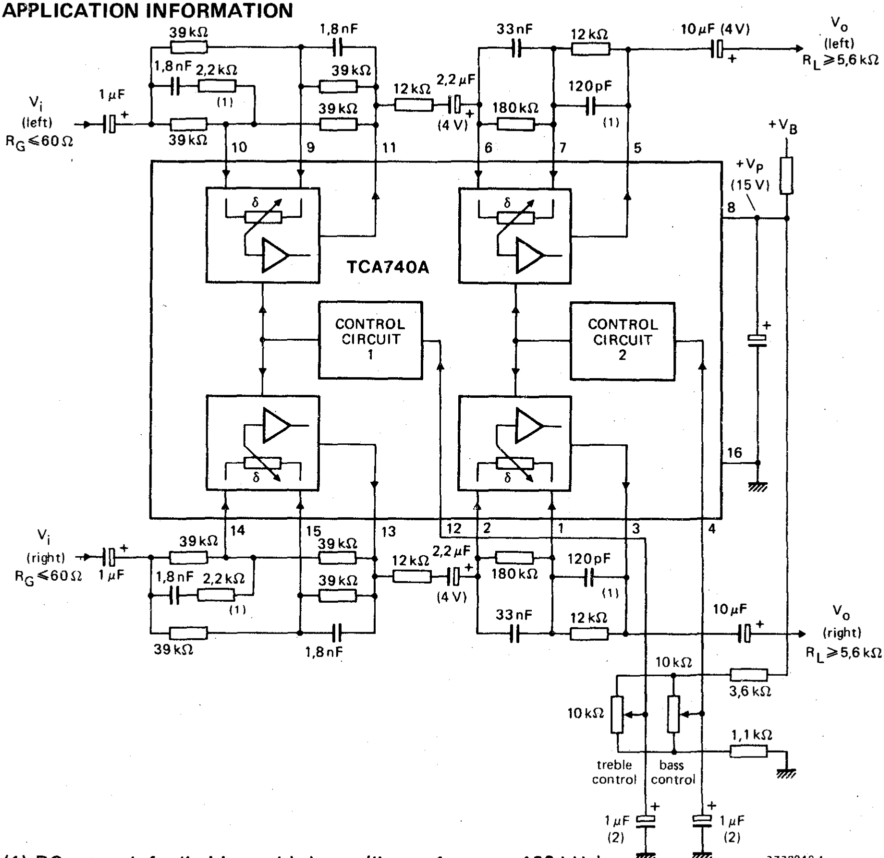


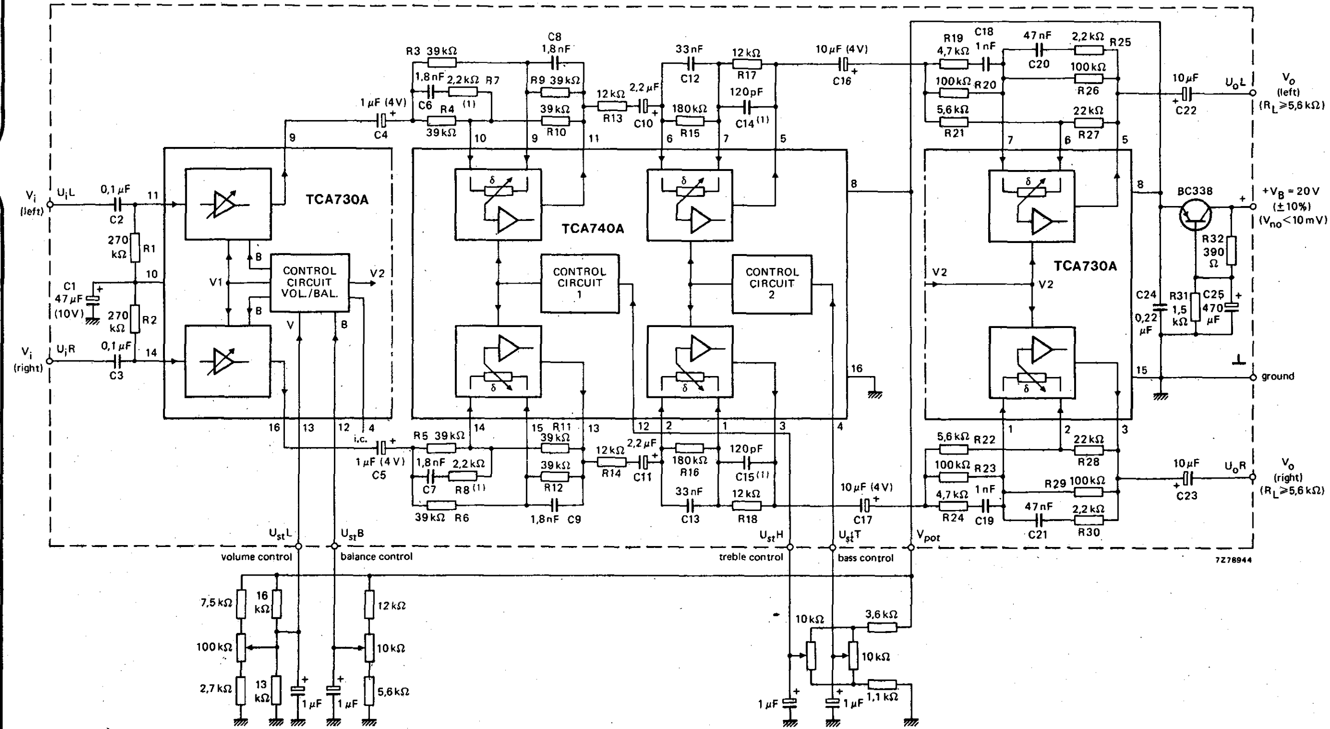
Fig. 5 Total distortion as a function of output voltage; $V_{4\text{-}16} = V_{12\text{-}16} = 5{,}6$ V (linear, $G_{v\,tot} = 1$); ——— f = 1 kHz; – – – f = 40 Hz to 16 kHz.

APPLICATION INFORMATION



(1) RC network for limiting treble boost (linear: $f_{-3\ dB}$ = 100 kHz).
(2) Capacitors are intended for suppression of the noise when adjusting the mechanical potentiometers.

Fig. 6 Application example of TCA740A used for treble and bass control.



(1) RC network for limiting treble boost (linear: $f_{-3\,dB} = 100$ kHz).

Fig. 7 Application diagram for TCA730A and TCA740A.
For printed-circuit board see Fig. 8.

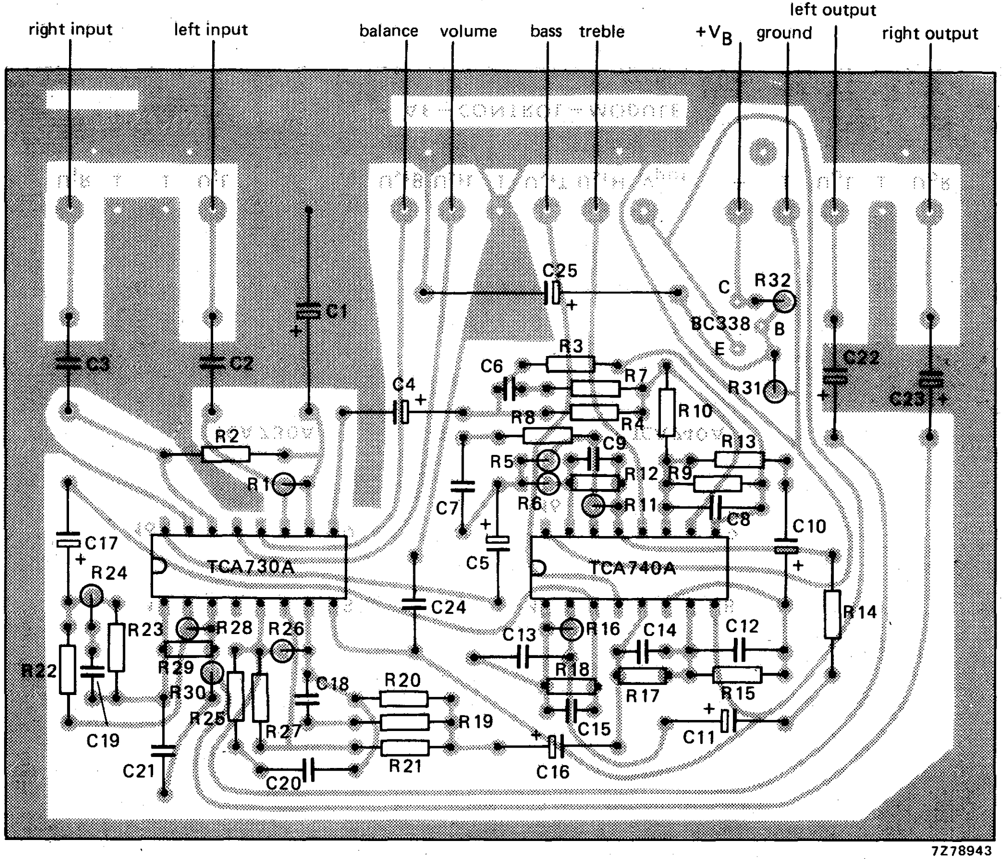


Fig. 8 Printed-circuit board component side, showing component layout; for circuit diagram see Fig. 7.

MULTI-STABILIZER FOR ELECTRONIC TUNING

The TCA750 is basically a stabilizer for use in electronic tuning systems. The circuit is combined with an external reference diode which entirely determines the thermal stability of the system and can be adapted to the stability requirements of AM, FM or TV receivers.

The reference diode BZV38 used in conjunction with the TCA750 form an ideal pair for FM tuners in radio or TV receivers.

Additional to a stabilized voltage (V_o1) for the electronic tuning system, the TCA750 incorporates two other output voltages (V_o2 and V_o3) for stabilized supply of the entire receiver combination as well as the following attractive features:

- The output current of any of the three stabilizers can be increased by a discrete power transistor without affecting circuit stability.
- For mute control at switching on, V_o2 can be delayed by external components.
- An a.f.c. coupling circuit provides a constant correction factor by superimposing an a.f.c. voltage on V_o1.
- Adjustable a.f.c. amplification factor (< 5).
- Pulse or touch contact operation switches off the a.f.c. whilst changing stations.
- Delayed switching on of the a.f.c., externally adjustable ($t_d < 2$ s).
- Search tuning becomes very simple when using the a.f.c. current source (pin 10).
- All three stabilized outputs are protected against short-circuit and are individually adjustable.

QUICK REFERENCE DATA see page 2

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

QUICK REFERENCE DATA

Input voltage range	$V_{13\text{-}16}$	26,5 to 54	V
Ambient temperature	T_{amb}	typ. 25	°C
Input voltage	$V_{13\text{-}16}$	typ. 45	V
→ Tuning voltage (V_o1) *	$V_{12\text{-}16}$	21 to 34	V
Output current (I1) *	I_{12}	< 14,5	mA
Stabilizing time	t_{stab}	typ. 0,8	s
Temperature coefficient (V_o1)			
TCA750	$\Delta V_o1/\Delta T$	typ. 1	ppm/°C
BZV38		typ. 30	ppm/°C
Line regulation	$\Delta V_o1/\Delta V_{in}$	typ. 10	ppm/V
→ Output voltage (V_o2) *	$V_{14\text{-}16}$	8 to 21	V
Output current (I2) *	I_{14}	< 6	mA
→ Output voltage (V_o3) *	$V_{2\text{-}16}$	8 to 29	V
Output current (I3) *	I_2	< 6	mA

* Symbols used in test circuit Fig. 3.

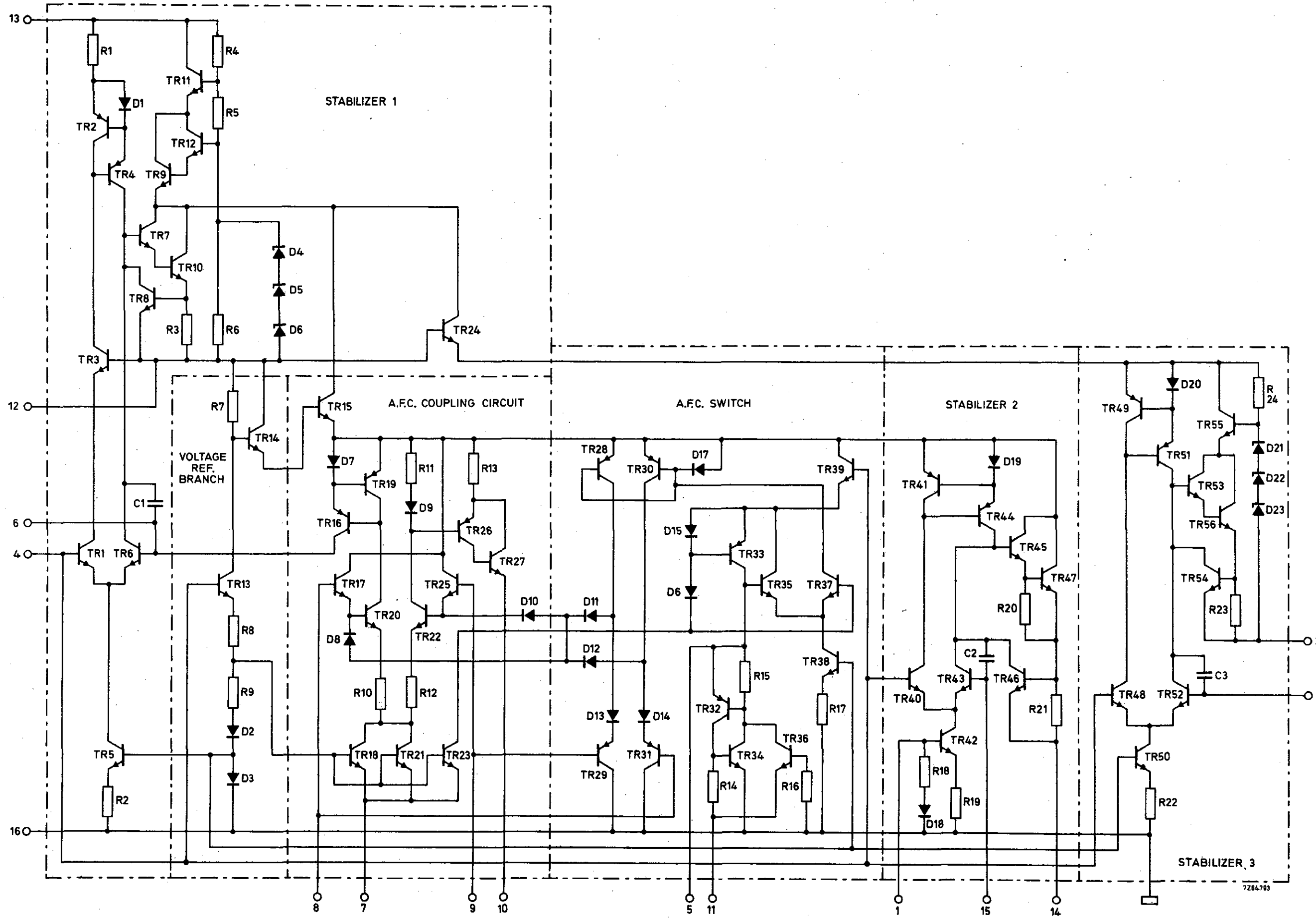


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Input voltage (supply)	$V_{13\text{-}16}$	max.	54 V
A.F.C. input voltages (pins 8 and 9)	$V_{8\text{-}16}, V_{9\text{-}16}$	max.	17 V
	$\pm V_{8\text{-}9}$	max.	6 V
Output current			
pin 12	I_{12}	max.	55 mA
pin 14	I_{14}	max.	20 mA
pin 2	I_{2}	max.	25 mA
Input current (pin 11)	$\pm I_{11}$	max.	6 mA
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−25 to + 150 °C *
Total power dissipation	see derating curve Fig. 2		

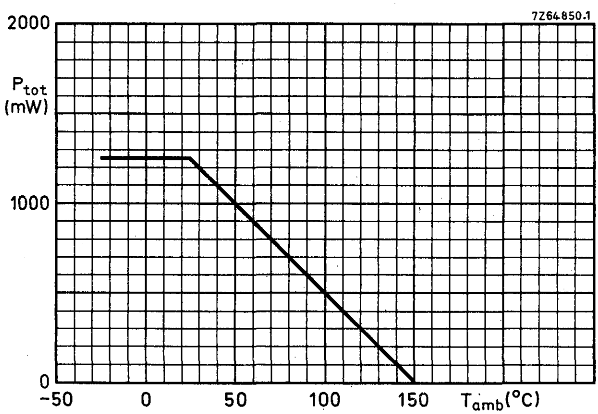
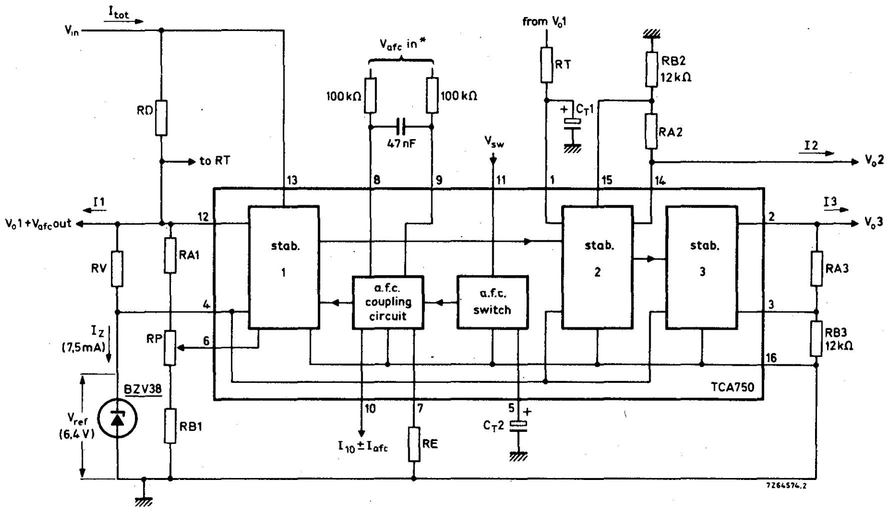


Fig. 2 Power derating curve.

* See derating curve Fig. 2.



* V_{afc}in is superimposed on a common-mode voltage (V_{com}) of 5 V to 17 V.

Fig. 3 Test circuit and multi-stabilizer peripheral components.

Note to power reduction resistor RD

For worst case conditions (maximum output currents of the three stabilizers and a high supply voltage V_{in}) the power dissipation (P_{tot}) must be reduced by the use of the external resistor RD.

$$\text{Power reduction} = \frac{(V_{in} - V_o1)^2}{RD}$$

The minimum permissible value of RD is derived by the formula

$$RD_{min} = \frac{V_{in\,max} - V_o1 - V_{afc}out}{I_{12} - I_{13\,min}}$$

where,

$I_{13\,min} = 4{,}5$ mA (stand-by current I_s)

$I_{12} = I_Z + I_{RA1} + I1_{min}$

CHARACTERISTICS and APPLICATION INFORMATION

T_{amb} = 25 °C; see test circuit Fig. 3.

		note	min.	typ.	max.	
Supplies						
Input voltage	V_{in}	1	26,5	—	54	V
Input current	I_{tot}	2	—	—	31	mA
Output characteristics						
D.C. output resistance (all stabilizers)	R_{out}	—	—	1	—	Ω
Permissible output short-circuit duration						
stabilizer 1	t_{short}	—	continuous			
stabilizers 2 or 3	t_{short}	—	—	—	10	s
Stabilizer 1						
→ Output voltage range (adjustable)	V_o1	3	21	—	34	V
Output current	I1	4, 5	0	—	5	mA
Stabilizing time	t_{stab}	6	—	—	1	s
Output voltage temp. coefficient	$\Delta V_o1/\Delta T$	7, 8	—	40	—	ppm/°C
Line regulation	$\Delta V_o1/\Delta V_{in}$	8	—	10	—	ppm/V
A.F.C. coupling circuit						
A.F.C. input voltage (½ V_{afc} swing)	V_{afc} in	—	—	—	5	V
A.F.C. output voltage (½ V_{afc}lim swing)	V_{afc} lim	15, 16	—	—	0,9	V
A.F.C. output current threshold	I_{10}	15, 16	—	—	1,5	mA
A.F.C. output current swing	I_{afc} lim	15, 16	—	—	3,0	mA
A.F.C. off delay	t_d	—	—	2	—	s
Amplification factor	μ	—	—	—	5	
A.F.C. slope ($\Delta I_{afc}/\Delta V_{afc}$ in)	S	14	—	2,5	—	mA/V
Common-mode voltage	V_{com}	9	5	—	17	V
V_o1 change due to a.f.c. switching	ΔV_o1/afc	—	—	—	25	mV
Asymmetry of a.f.c. input (a.f.c. off)	$\pm (I_8 - I_9)$	—	—	—	0,5	μA
A.F.C. switch operated by manual switch						
Input voltage (a.f.c. on)	V_{sw}	—	−0,5	—	+0,5	V
Positive input voltage (a.f.c. off)	$+V_{sw}$	—	0,8	—	6	V
Negative input voltage (a.f.c. off)	$-V_{sw}$	—	0,8	—	—	V
Positive input current (a.f.c. off)	$+I_{11}$	—	0,004	—	3	mA
Negative input current (a.f.c. off)	$-I_{11}$	—	0,8	—	2	mA
A.F.C. switch operated by pulse						
Positive trigger pulse peak current	$+I_{11}$ pulse	13				
pulse width = 10 μs		—	800	—	3000	μA
100 μs		—	80	—	3000	μA
1 ms		—	8	—	3000	μA
10 ms		—	4	—	3000	μA
Negative trigger pulse peak current	$-I_{11}$ pulse	—	0,8	—	2	mA
Negative trigger pulse width		—	10	—	—	μs

Stabilizer 2		note	min.	typ.	max.	
Output voltage range (adjustable)	V_o2	10	8	–	21	V
Output current	I2	5	0	–	5,5	mA
Output voltage temp. coefficient	$\Delta V_o2/\Delta T$	7, 8	–	45	–	ppm/°C
Switch-on delay time	$t_{d\,on}$	11	0	–	6	s
Switching voltage	$V_{1\text{-}16}$	–	0,8	–	1	V

Stabilizer 3						
Output voltage range (adjustable)	V_o3	12	8	–	29	V
Output current	I3	5	0	–	5,5	mA
Output voltage temp. coefficient	$\Delta V_o3/\Delta T$	7, 8	–	45	–	ppm/°C

Notes

1. The V_{in} range depends on the value of V_o1 (see Fig. 4).
2. At I1 = 5 mA, I2 = I3 = 5,5 mA, I_{10} = 0.
3. Adjustable by means of RA1, RB1 and RP.
4. If a higher level is required from the output of stabilizer 1, the reference diode supply may be obtained from the emitter of a power transistor connected to the output from stabilizer 3 (see Fig. 8). In this case, the current available from stabilizer 1 is increased to 12,5 mA (bleeder current I_{RA1} = 2 mA).
5. At T_{amb} = 60 °C maximum with all stabilizers at rated currents.
6. With V_o1 within 0,05% of its steady value.
7. Temperature coefficient at T_{amb} from 10 °C to 60 °C with V_{in} constant, and using metal film bleed resistors having a temperature coefficient of ⩽ 50 ppm/°C.
8. With all stabilizer output currents constant and within the specified limits.
9. Common-mode voltage = voltage between pins 8 and 16, and 9 and 16 of the I.C.
10. V_o2 depends on the value of V_o1 (see Fig. 6); adjustable with RA2.
11. Adjustable by means of RT and C_T1. The delay time is limited by the leakage current of C_T1.
12. V_o3 depends on the value of V_o1 (see Fig. 7); adjustable with RA3.
13. The delay time after triggering depends on the value of C_T2.
14. With RE = 10 kΩ and T_{amb} = 25 °C.
15. V_{afc} out at V_{afc} in after limiting.
16. With RE = 10 kΩ; RA1 = 12 kΩ.

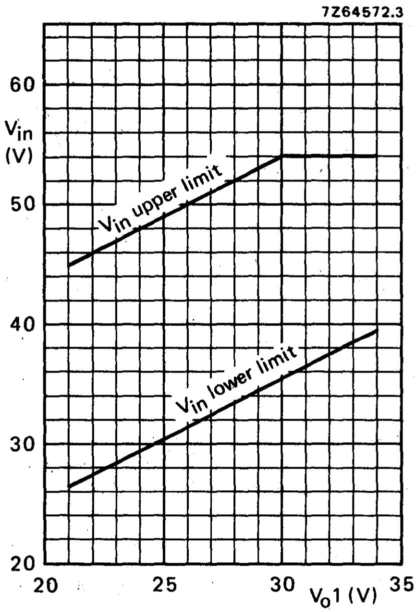


Fig. 4 Range of values for V_o1.

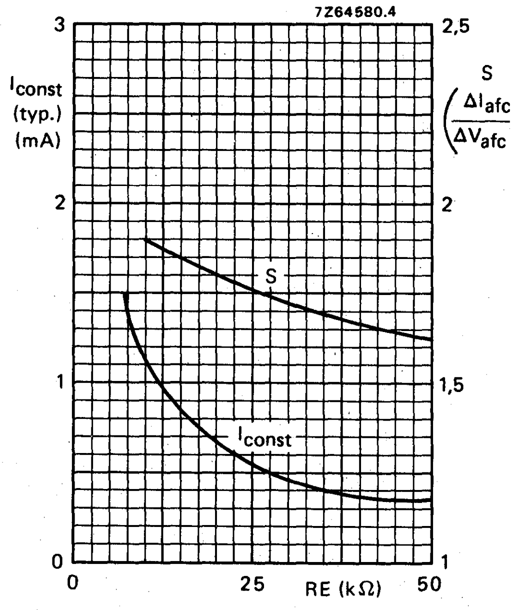


Fig. 5 Determination of I_{10} and S-factor (S = a.f.c. slope) from RE.

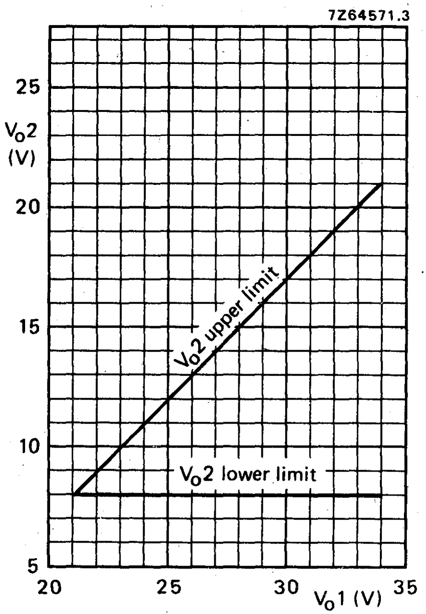


Fig. 6 Range of values for V_o2.

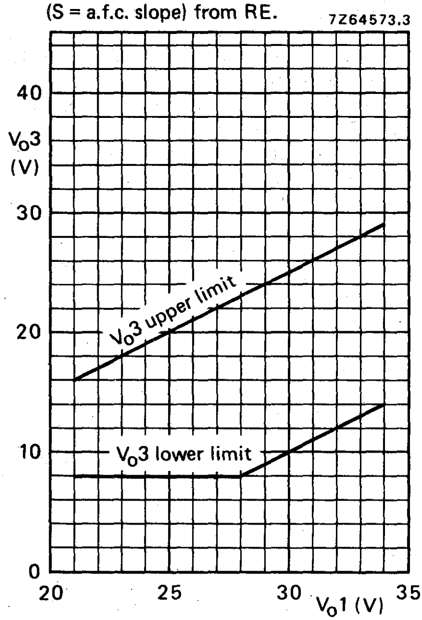


Fig. 7 Range of values for V_o3.

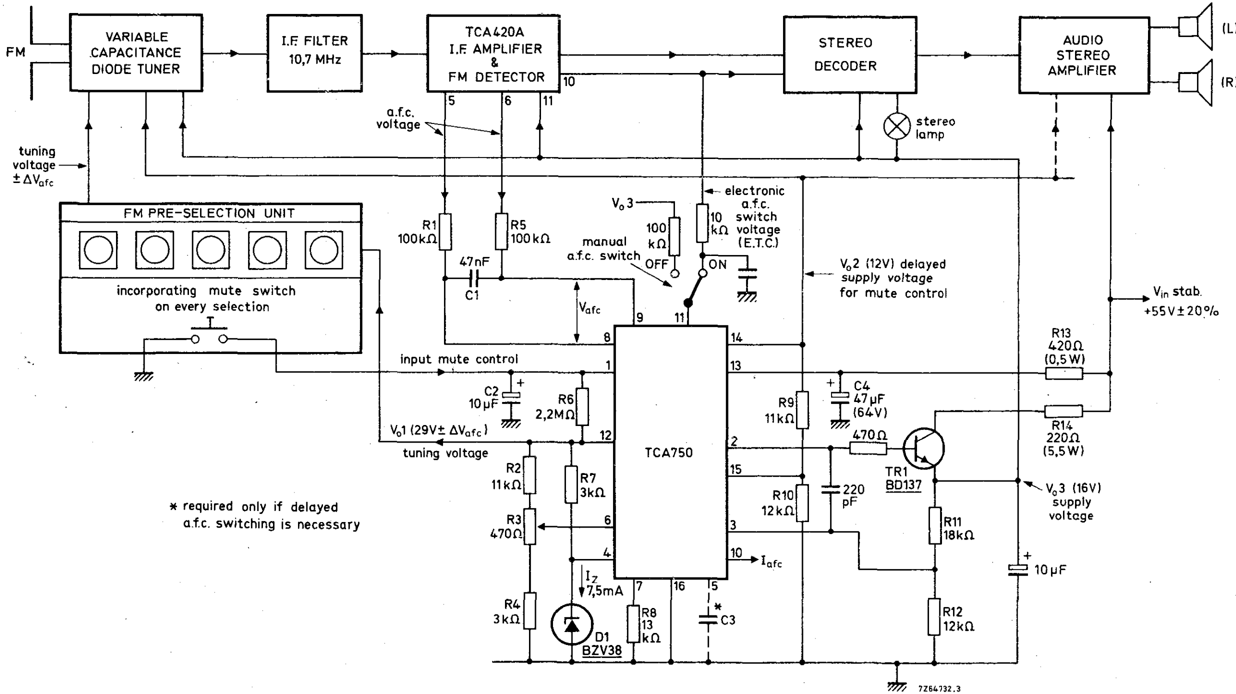


Fig. 8 Hi-fi radio receiver with electronic tuning using TCA750.

INTEGRATED AUDIO AMPLIFIER

The TCA760B is a monolithic integrated audio amplifier incorporating high flexibility for applications in battery and mains-fed equipment.
Due to special internal circuitry (stabilization, temperature correction, high a.c. feedback of 20 dB) the cross-over distortion is negligible over the entire supply voltage range (5 to 14 V). Presetting is not required for the quiescent current (5 to 15,7 mA), it is internally adjusted.

Additional features are:
- low noise output voltage;
- high peak current (1 A);
- high unloaded supply voltage (15 V);
- high gain (closed loop 15 dB at a feedback of 20 dB);
- safe operation regarding second breakdown;
- high ripple rejection.

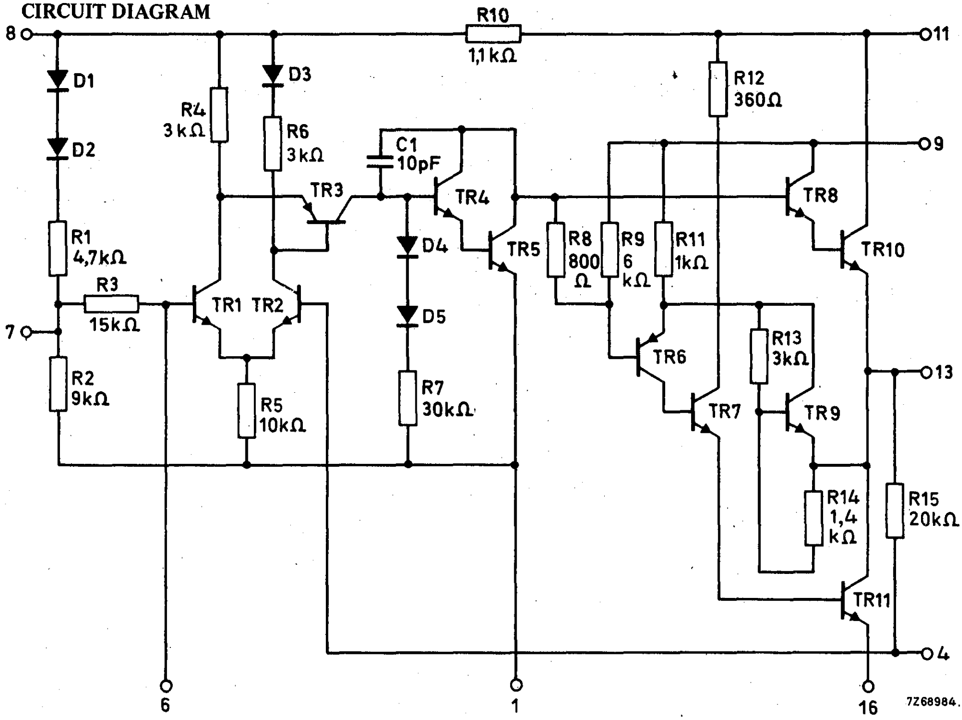
The device will withstand repetitive short circuits across the speaker load if the absolute maximum junction temperature is not exceeded.

QUICK REFERENCE DATA				
Supply voltage range	V_P		5 to 14	V
Total quiescent current	I_{tot}		5 to 15,7	mA
Supply voltage (peak value)	V_{PM}	max.	15	V
Output power at d_{tot} = 10%				
at V_P = 9 V; R_L = 8 Ω	P_o	typ.	1,1	W
at V_P = 12 V; R_L = 8 Ω	P_o	typ.	2,1	W
Total distortion before clipping	d_{tot}	typ.	0,7	%
Input impedance	$\lvert Z_i \rvert$	typ.	15	kΩ
Sensitivity for P_o at d_{tot} = 10%	V_i	typ.	10	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage (pin 11)	V_{11-16}	max.	14	V
Unloaded supply voltage (pin 11; peak value) (no-signal condition)	V_{11-16M}	max.	15	V

Currents

Output current (pin 13, 11, 4)	I_O	max.	1	A
Non-repetitive peak output current (pin 13, 11, 4)	I_{OSM}	max.	2	A

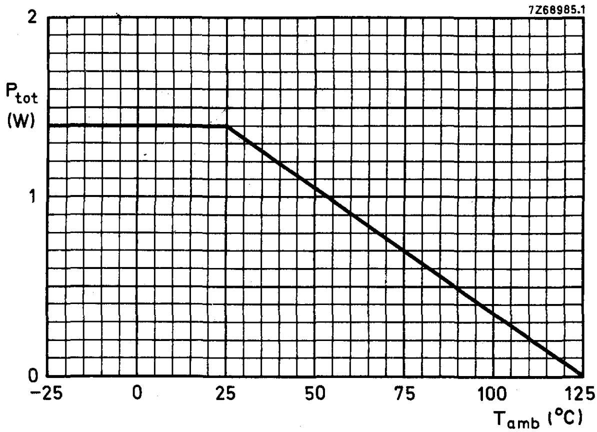
Power dissipation [1]

Total power dissipation at T_{amb} = 25 °C	P_{tot}	max.	1,4	W

Temperatures

Storage temperature	T_{stg}	−55 to +125	°C
Operating ambient temperature	T_{amb}	−25 to +125	°C

[1] See derating curve on page 3.



Design data

Pin 6 to 4 voltage	$\pm V_{6-4}$	max.	6	V
Pin 13 to 16 voltage	V_{13-16}	max.	14	V
Pin 11 to 13 voltage	V_{11-13}	max.	14	V

CHARACTERISTICS at T_{amb} = 25 °C; V_P = 9 V; R_L = 8 Ω unless otherwise specified

D.C. characteristics

Supply voltage range	V_{11-16}		5 to 14	V	
Total quiescent current	$I_{11\,tot}$	typ.	10	mA	1)
			5 to 15,7	mA	
Saturation voltages of output stages at I_o = 0,5 A	V_{CEsat}	<	0,9	V	

A.C. characteristics

A.F. output power at onset of clipping	P_o	typ.	0,8	W	3)
at d_{tot} = 10%	P_o	typ.	1,1	W	
Open loop voltage gain	G_v	typ.	70	dB	
Total harmonic distortion at P_o = 0,7 W	d_{tot}	typ.	0,7	%	
		<	3	%	
Noise output power at R_S = 0	P_n	typ.	2	nW	1)2)
Input sensitivity at P_o = 0,7 W	V_i		4 to 8,5	mV	
Input impedance	$\|Z_i\|$	typ.	15	kΩ	
Equivalent input noise voltage at R_S = 7 kΩ	V_n	typ.	1,5	μV	1)2)
		<	3,0	μV	

1) Measured without signal.

2) Measured at a frequency ranging from 30 Hz to 15 kHz.

3) Measured across R_L.

APPLICATION INFORMATION

Supply voltage V_{11-16} Load resistance R_L	6 4	6 8	7,5 4	7,5 8	9 4	9 8	10 8	12 8	V Ω
A.F. output power at onset of clipping	0,45 0,42	0,35 0,33	0,8 0,7	0,6 0,57	1,1 1,0	0,9 0,8	1,2 1,1	1,4 1,3	W [1] W [2]
A.F. output power at d_{tot} = 10%	0,66 0,62	0,48 0,46	1,1 1,0	0,8 0,78	1,5 1,4	1,2 1,1	1,5 1,45	2,1 2,0	W [1] W [2]
Sensitivity for P_o = 50 mW V_i for d_{tot} = 10% V_i	 1,4 4,8	 2,0 7,0	 1,4 8,0	 2,0 9,0	 1,4 10	 2,0 10	 2,0 11,0	 2,0 12,0	 mV mV
T_{amb} (maximum)	93	107	78	99	45	87	81	45	°C
Supply current for full output power	185	125	225	165	300	190	215	250	mA
Quiescent current I_{tot}	10,0	10,0	10,0	10,0	10,0	10,0	10,0	10,0	mA
Value of R1	47	47	47	47	47	47	47	47	Ω
R2	100	100	100	100	100	100	100	100	Ω
R3	1	1	1	1	1	1	1	1	Ω
C1	1,6	1,6	1,6	1,6	1,6	1,6	1,6	1,6	μF
C2	47	47	47	47	47	47	47	47	μF
C3	125	125	125	125	125	125	125	125	μF
C4	470	220	470	220	470	220	220	220	μF
C5	1000	470	1000	470	1000	470	470	470	μF
C6	150	150	150	150	150	150	150	150	nF
C7	47	47	47	47	47	47	47	47	μF
Input impedance $\|Z_i\|$	15	15	15	15	15	15	15	15	kΩ
Closed loop voltage gain G_v	50	50	50	50	50	50	50	50	dB [3]
Open loop voltage gain G_v	66	68	70	71	70	74	76	78	dB
Frequency response	← see pages 9 and 10 →								
Noise output power P_n			4			2			nW [4]
Noise output power P_n			50			25			nW [5]

1) Measured before output capacitor (C5).

2) Measured across R_L.

3) At R1 = 47 Ω. The gain can be increased by decreasing the value of R1; at decreasing the gain level however the maximum tolerated value of R1 amounts to 100 Ω; at further decrease of the gain an attenuator at the input is preferred.

4) R_S = 0 Ω; frequency range 30 Hz to 15 kHz.

5) R_S = 7 kΩ; frequency range 30 Hz to 15 kHz.

APPLICATION INFORMATION (continued)

General notes

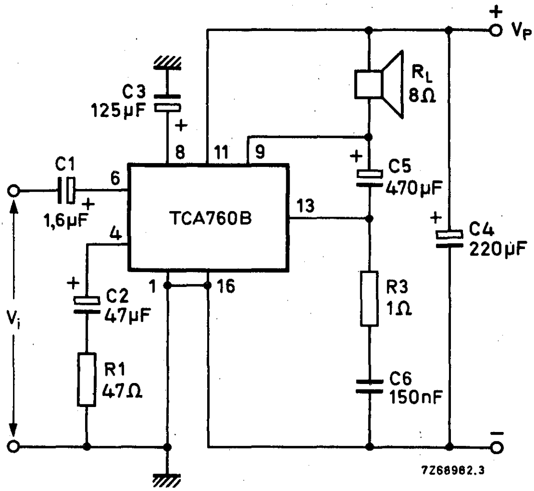
1. Prescription for print lay-out:

   Pin 1 must be used as a ground connection for the input circuit.
   Pin 16 must be used for the output circuit and for connection of the negative supply voltage.
   The pins 16 and 1 have to be interconnected as close to the package as possible to prevent a common impedance in the ground line.

2. The smoothing capacitor across the supply must be connected close to the pins.

3. To prevent radio signals in the low frequency amplifier a small capacitor of about 560 pF between pins 6 and 1 is preferred.

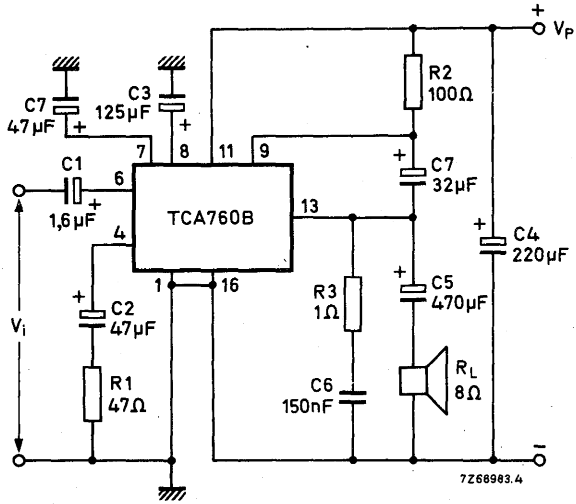
Basic power amplifier

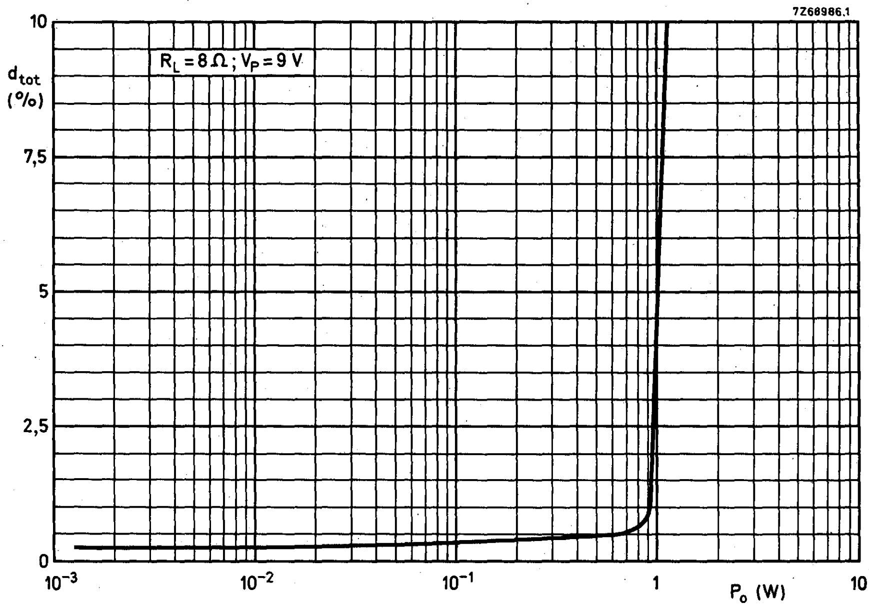


APPLICATION INFORMATION (continued)

Power amplifier for mains-fed supply

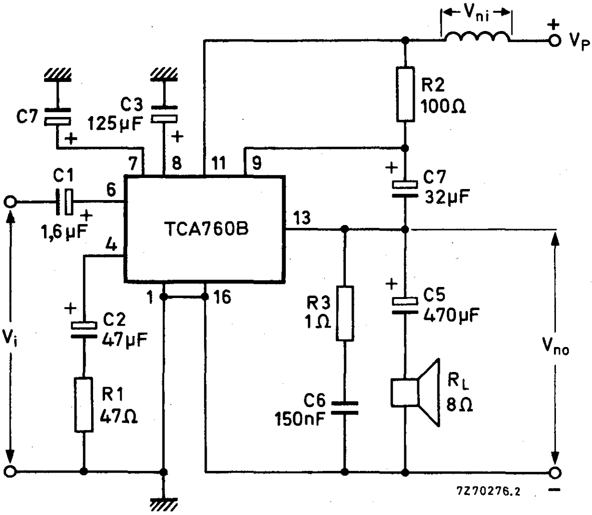
When using a mains-fed power supply with high ripple it is advantageous to connect the speaker to ground by bootstrapping pin 9.
Pin 7 is available for extra hum suppression (see graphs on page 9).

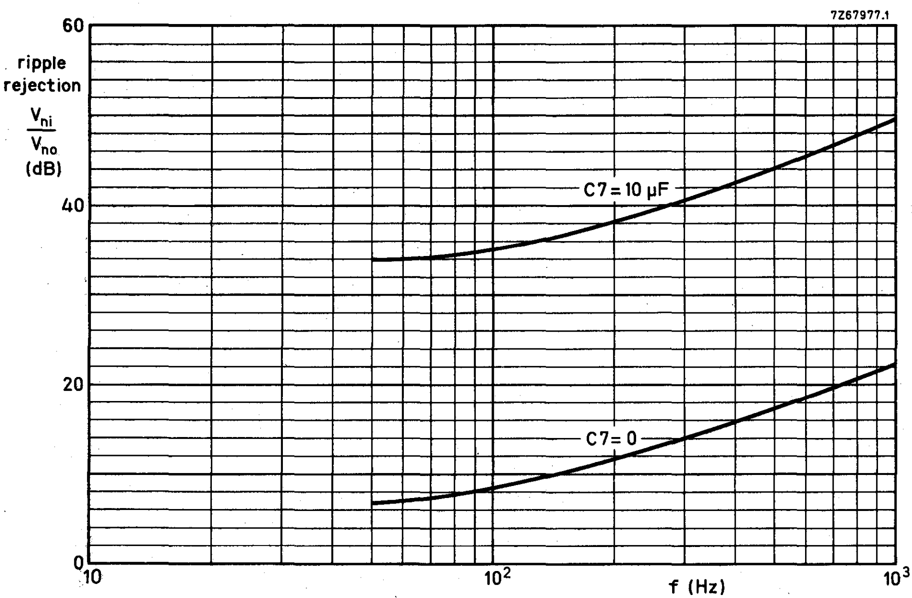


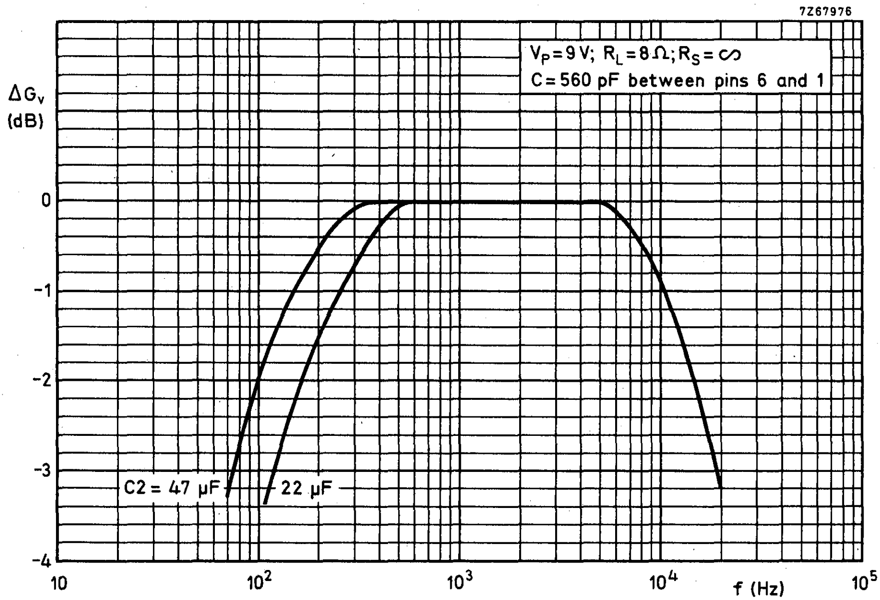

7Z68986.1
10
d_{tot}
(%)
7,5
5
2,5
0
$R_L = 8\,\Omega$; $V_P = 9$ V
10^{-3}
10^{-2}
10^{-1}
1
P_o (W)
10

APPLICATION INFORMATION (continued)

The influence on the hum suppression when a capacitor of 10 μF is connected between pins 7 and 1 is shown in the graph below.
An increase of the capacitor value gives no further improvement in hum suppression.






7Z67976
$V_P = 9$ V; $R_L = 8\ \Omega$; $R_S = \infty$
C = 560 pF between pins 6 and 1
ΔG_v (dB)
0
-1
-2
-3
-4
C2 = 47 μF
22 μF
10
10^2
10^3
10^4
f (Hz)
10^5

INTERFERENCE ABSORPTION CIRCUIT

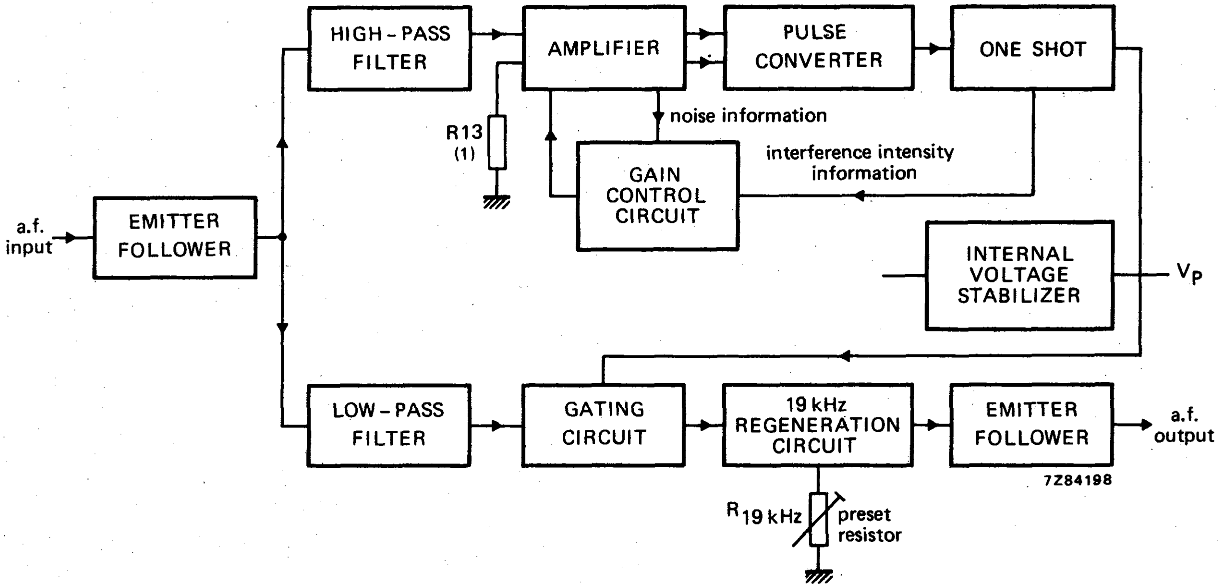
The TDA1001A is a monolithic integrated circuit for very effectively suppressing interference which, especially in FM mono and stereo receivers, disturbs the quality of reception.
The operation is based on the use of a high-pass filter separating the interference from the a.f. signal. The interference pulses are amplified to trigger a one shot. In this way gating pulses are obtained interrupting the audio signal, which is delayed by a low-pass filter, during the interference periods, the output being kept constant for that time. A 19 kHz filter can be externally connected to sustain the stereo pilot signal during suppression for improved performance as described below.
An integrating network decreases the trigger sensitivity for interference of high duty factor, so that the receiver remains operative even during periods of continuous interference.

QUICK REFERENCE DATA

Supply voltage range	$V_P = V_{9\text{-}16}$		8 to 15	V
Ambient temperature	T_{amb}	typ.	25	°C
Supply voltage	V_P	nom.	12	V
Total quiescent current	I_{tot}	typ.	15	mA
A.F. input signal handling (peak-to-peak value) $d_{tot} < 1\%$; f = 1 kHz	$V_{1\text{-}16(p\text{-}p)}$	<	1,5	V
Input impedance at f = 40 kHz (pin 1)	$\lvert Z_i \rvert$	>	30	kΩ
Audio voltage gain	$\frac{V_{6\text{-}16}}{V_{1\text{-}16}}$	typ.	0,8	dB
Total distortion f = 1 kHz; $V_{i(rms)} \leqslant 0{,}5$ V	d_{tot}	typ.	0,35	%
Residual gate pulse in output signal (pin 6) (peak-to-peak value)	$V_{r6\text{-}16(p\text{-}p)}$	<	4	mV
Interference trigger sensitivity (adjustable) R13 = 3,3 kΩ; peak value	$V_{1\text{-}16M}$	typ.	50	mV
R13 = 2,5 kΩ; peak value	$V_{1\text{-}16M}$	typ.	42	mV
Suppression pulse duration (pin 10)	t_s		20 to 35	μs

PACKAGE OUTLINES

TDA1001A: 16-lead DIL; plastic (SOT-38)
TDA1001AT: 16-lead flat pack; plastic (SO-16; SOT-109A).



(1) The interference trigger sensitivity is predetermined by R13 (see also Fig. 3) and is defined by

$V_{tr} = \left(1 + \frac{R13}{R_S}\right) \times V_{tr0}$, in which V_{tr} = trigger voltage, V_{tr0} = trigger voltage at 0 Ω, R_S = 2,2 kΩ (internal source resistance).

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	V_P	max.	18	V
D.C. input voltage (pin 1)	$V_{1\text{-}16}$	max.	V_P	V
D.C. output current (pin 6)	$-I_6$	max.	15	mA
	$+I_6$	max.	1	mA
Storage temperature	T_{stg}	−65 to + 150		°C
Operating ambient temperature*	T_{amb}	−30 to + 80		°C

* Based on nominal application, Fig. 3; for deviating periphery see power derating curve Fig. 2.

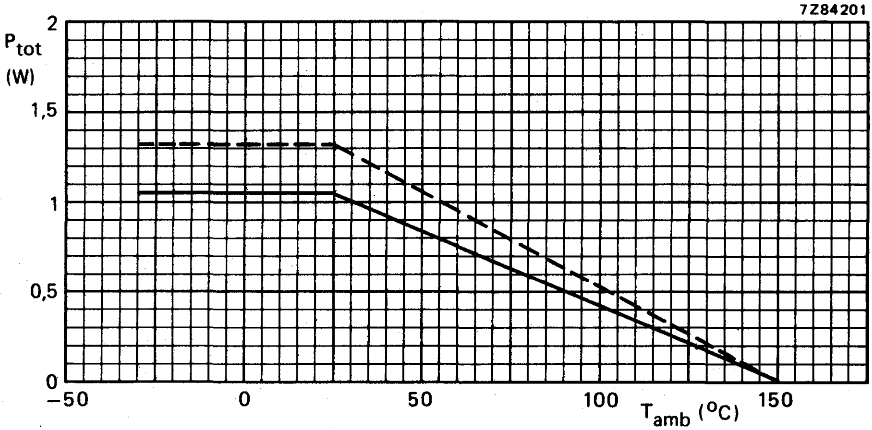


Fig. 2 Power derating curves; ——SOT-38; – – – SO-16, SOT-109A mounted on a ceramic substrate of 50 x 15 x 0,7 mm.

CHARACTERISTICS measured in Fig. 3

D.C. characteristics at T_{amb} = 25 °C

Supply voltage	V_P	typ.	12 V
			8 to 15 V
Total quiescent current at V_P = 12 V	I_{tot}	typ.	15 mA
		<	25 mA

A.C. characteristics at T_{amb} = 25 °C; V_P = 12 V

Preamplifier; delay and gating circuit; output stage

(input: pin 1; output: pin 6)

A.F. input signal handling (peak-to-peak value) for d_{tot} < 1% at pin 6; f = 1 kHz	$V_{1\text{-}16(p\text{-}p)}$	<	1,5 V
Input impedance (pin 1) f = 40 kHz	$\lvert Z_i \rvert$	>	30 kΩ
Input impedance (pin 3) f = 1 kHz	$\lvert Z_i \rvert$	>	230 kΩ
Input impedance (pin 5) f = 1 kHz, during suppression (gating circuit non-conducting)	$\lvert Z_i \rvert$	>	4 MΩ
Audio voltage gain	$\frac{V_{6\text{-}16}}{V_{1\text{-}16}}$	typ.	0,8 dB
Residual gate pulse in output signal (pin 6) (peak-to-peak value) see note 1	$V_{r6\text{-}16(p\text{-}p)}$	<	4 mV
Discharge current at pin 5	I_{d5}	<	250 nA
Total distortion; no-interference condition (pin 6) f = 1 kHz; $V_{i(rms)} \leqslant$ 0,5 V	d_{tot}	typ.	0,35 %
		<	1 %

Preamplifier; interference separator; pulse converter; one shot

(input: pin 1; output: pin 10)

Input signal: sine-wave of 120 kHz (high-pass filter characteristic is $V_{14\text{-}16}/V_{1\text{-}16}$ = −2 dB at 120 kHz)

Interference trigger sensitivity at 120 kHz (pin 1) (r.m.s. values); see note 2

control function OFF (pin 12 connected to pin 9)			
at R13 = 3,3 kΩ	$V_{1\text{-}16(rms)}$	typ.	30 mV
			20 to 42 mV
at R13 = 2,5 kΩ	$V_{1\text{-}16(rms)}$	typ.	25 mV
			18 to 36 mV
control function ON			
at R13 = 3,3 kΩ	$V_{1\text{-}16(rms)}$	typ.	170 mV
at R13 = 2,5 kΩ	$V_{1\text{-}16(rms)}$	typ.	145 mV

For notes see next page.

Input signal: pulse signal with $t_p = 10\ \mu s$; repetition frequency $f_r = 1$ kHz; pulse rise and fall times $t_r = t_f = 6$ ns

Pulse trigger sensitivity (pulse peak value); see note 2			
control function OFF (pin 12 connected to pin 9)			
at R13 = 3,3 kΩ	$V_{1\text{-}16M}$	typ.	50 mV
at R13 = 2,5 kΩ	$V_{1\text{-}16M}$	typ.	42 mV
Suppression pulse duration of 'one shot'; see note 3	t_s		*20 to 35 μs*

Noise threshold circuit

(input: pin 1; output: pin 12 with respect to pin 9)

Input signal: sine-wave of 120 kHz (high-pass filter characteristic is $V_{14\text{-}16}/V_{1\text{-}16} = -2$ dB at 120 kHz)

Input voltage (r.m.s. value)			
for $V_{12\text{-}9}$ = 100 mV			
at R13 = 3,3 kΩ	$V_{1\text{-}16(rms)}$	typ.	15 mV
at R13 = 2,5 kΩ	$V_{1\text{-}16(rms)}$	typ.	13 mV
for $V_{12\text{-}9}$ = 600 mV (pin 10 short-circuited to pin 9)			
at R13 = 3,3 kΩ	$V_{1\text{-}16(rms)}$	typ.	16 mV
			12 to 22 mV
at R13 = 2,5 kΩ		typ.	14 mV
			10 to 19 mV
Minimum interference repetition rate to cause defeat action (pin 12); see note 4	$f_{r\,min}$	>	20 kHz
Amplification control by interference intensity $V_i = 50$ mV; f = 19 kHz; $V_{1\text{-}16M} = 300$ mV; pulse duration $t_p = 10\ \mu s$;			
repetition frequency $f_r = 1$ kHz	$V_{6\text{-}16}$		50 to 60 mV
repetition frequency $f_r = 16$ kHz	$V_{6\text{-}16}$		45 to 65 mV

19 kHz filter (input: pin 7; output: pin 8)

Current amplification (see notes 5 and 6)	$\frac{\Delta I_7}{\Delta I_8}$	typ.	3
			2,8 to 3,2

Notes

1. See Fig. 4 for the output pulse description; with the 19 kHz filter switched off (pin 7 connected to pin 16).
2. The interference trigger sensitivity is predetermined by R13 and is defined by the formula $V_{tr} = (1 + R13/R_S) \times V_{tr0}$ in which $R_S = 2{,}2$ kΩ (see also note in Fig. 1).
3. Adjustable with R11 or C11; for 20 to 35 μs: R11 = 6,8 kΩ and C11 = 2,2 nF.
4. Adjustable with R10; at R10 = 1,5 kΩ: $f_r = 20$ kHz.
   Defeat action starts if $V_{12\text{-}16}$ has reacted a control voltage of V_{BE} (0,6 V).
5. 19 kHz adjustable with R_{19kHz} (see Fig. 3).
6. The IC may also be used, if desired, without 19 kHz filter by connecting the 1,5 kΩ resistor and 6,6 nF capacitor of pin 5 to pin 16, and by leaving pins 7 and 8 unused (see Fig. 3).

APPLICATION INFORMATION

T_{amb} = 25 °C; V_P = 12 V; measured in Fig. 3

SIGNAL PATH

Input amplifier

Input impedance at f = 40 kHz (pin 1)			
pin 2 unloaded	$\lvert Z_i \rvert$	typ.	500 kΩ
pin 2 loaded	$\lvert Z_i \rvert$	typ.	40 kΩ
D.C. input voltage adjustment	$V_{1\text{-}16}$	typ.	0,4 V_P V
Output impedance (pin 2)			
pin 2 unloaded; pin 1 loaded	$\lvert Z_o \rvert$	typ.	480 Ω

Low-pass filter

Input impedance at f = 1 kHz (pin 3)	$\lvert Z_i \rvert$	typ.	1 MΩ
D.C. input current at $V_{3\text{-}16}$ = 3,4 V	I_3	typ.	2 μA
Output impedance (pin 4)	$\lvert Z_o \rvert$	typ.	500 Ω
−3 dB point of low-pass filter	$f_{(-3\ dB)}$	typ.	75 kHz

Gate circuit with output stage

Leakage current (pin 5)	I_5	typ.	100 nA

Pilot regeneration 19 kHz filter

Current amplification	$\frac{\Delta I_7}{\Delta I_8}$	typ.	3
			2,8 to 3,2

INTERFERENCE PATH

High-pass filter

Input impedance at f = 1 kHz (pin 15)	$\lvert Z_i \rvert$	typ.	1 MΩ
D.C. input current			
at $V_{15\text{-}16}$ = 0,19 V; $V_{9\text{-}16}$ = 2,0 V	I_{15}	typ.	1 μA
Output impedance (pin 14)	$\lvert Z_o \rvert$	typ.	500 Ω
Voltage gain	$\frac{V_{14\text{-}16}}{V_{15\text{-}16}}$	typ.	1,4
−3 dB point of high-pass filter	$f_{(-3\ dB)}$	typ.	140 kHz

Pulse amplifier; converter and gain control

Peak output current			
(noise controlled feedback in ON position)	I_{12M}	typ.	0,4 mA
Input voltage			
(noise controlled feedback in ON position)	$-V_{12\text{-}9}$	typ.	0,65 V

One shot

Gate circuit conducting; no-interference condition				
required input voltage level	$V_{11\text{-}16}$	<	1	V
output leakage current	I_{10}	typ.	15	μA
Gate circuit non-conducting; interference condition				
required input voltage level	$V_{11\text{-}16}$	>	2	V
output current	I_{10}	>	1	mA
Offset voltage; backlash	$\Delta V_{11\text{-}16}$	typ.	0,4	V

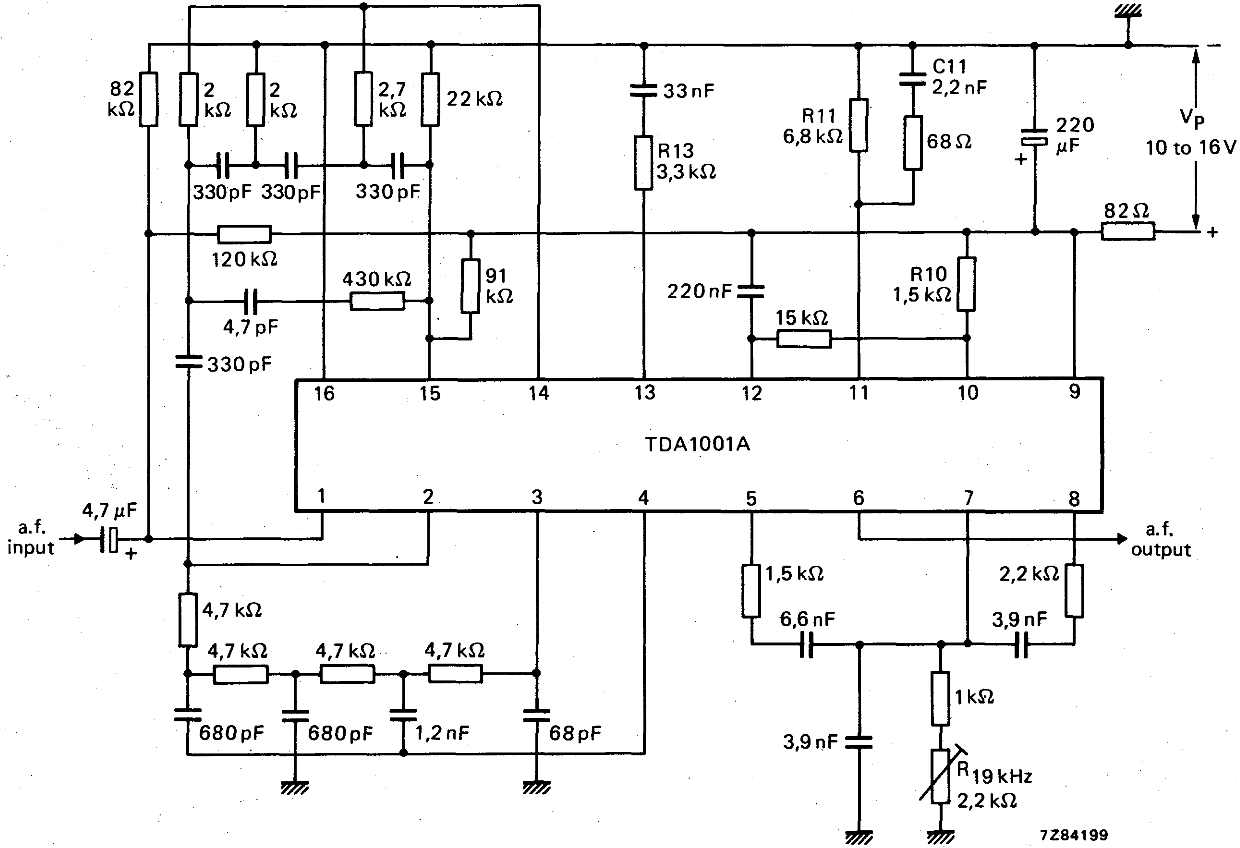


Fig. 3 Test/application circuit.

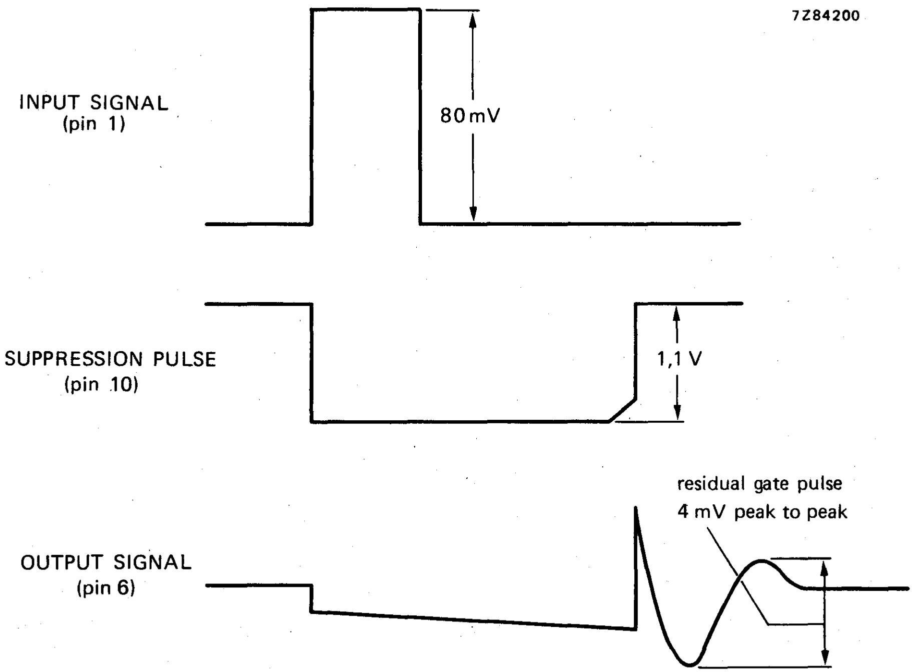
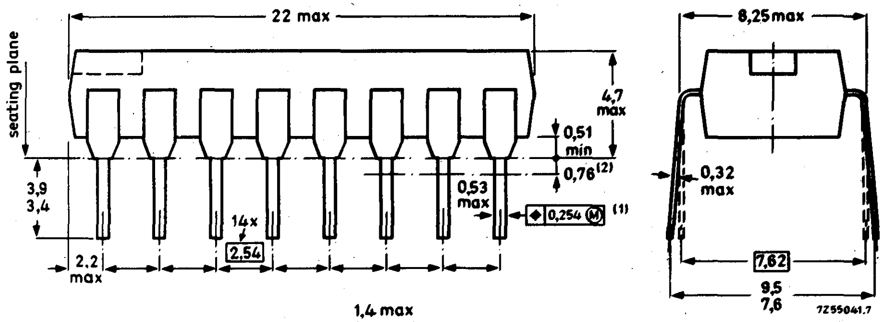
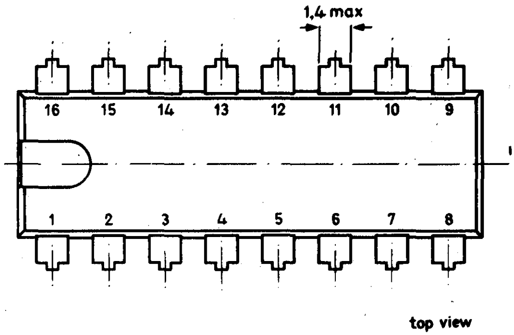


Fig. 4 Residual gate pulse in output signal at V_i = 80 mV; pulse duration t_p = 10 μs; repetition frequency f_r = 1 kHz.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

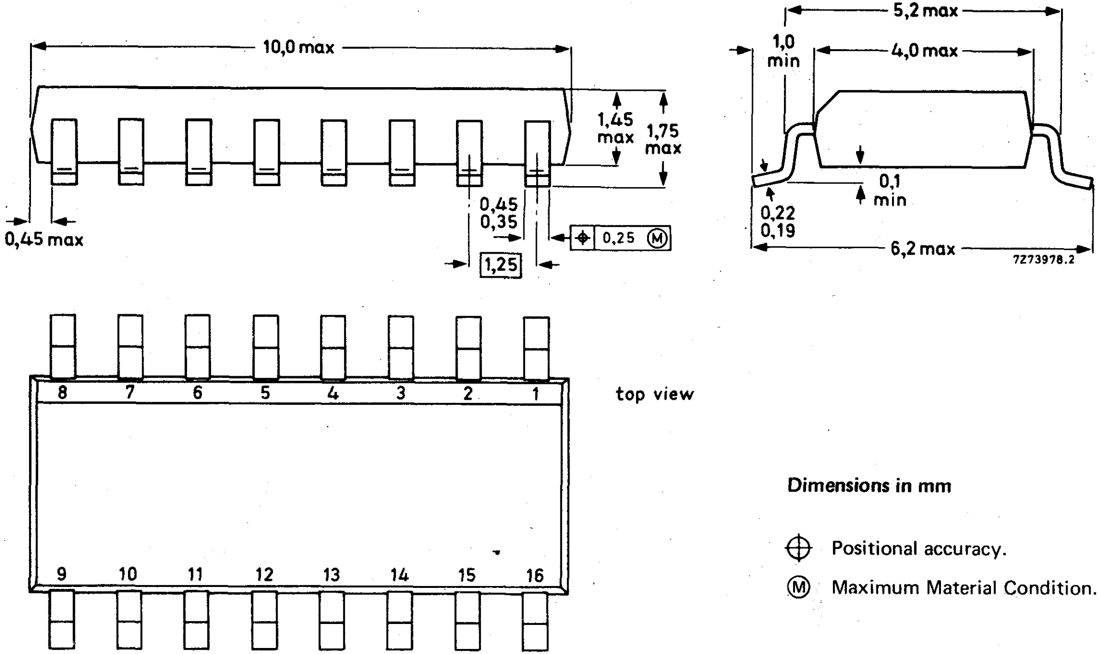
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD FLAT PACK; PLASTIC (SO-16; SOT-109A)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

SOLDERING

See next page.

SOLDERING

The reflow solder technique

The preferred technique for mounting miniature components on hybrid thick or thin-film circuits is reflow soldering. Solder is applied to the required areas on the substrate by dipping in a solder bath or, more usually, by screen printing a solder paste. Components are put in place and the solder is reflowed by heating.

Solder pastes consist of very finely powdered solder and flux suspended in an organic liquid binder. They are available in various forms depending on the specification of the solder and the type of binder used. For hybrid circuit use, a tin-lead solder with 2 to 4% silver is recommended. The working temperature of this paste is about 220 to 230 ^{o}C when a mild flux is used.

For printing the paste onto the substrate a stainless steel screen with a mesh of 80 to 105 μm is used for which the emulsion thickness should be about 50 μm. To ensure that sufficient solder paste is applied to the substrate, the screen aperture should be slightly larger than the corresponding contact area.

The contact pins are positioned on the substrate, the slight adhesive force of the solder paste being sufficient to keep them in place. The substrate is heated to the solder working temperature preferably by means of a controlled hot plate. The soldering process should be kept as short as possible: 10 to 15 seconds is sufficient to ensure good solder joints and evaporation of the binder fluid.
After soldering, the substrate must be cleaned of any remaining flux.

RECORDING AND PLAYBACK AMPLIFIER

This integrated circuit incorporates all amplifier circuits necessary for the record/playback functions, with the exception of the audio power output amplifier. It comprises:
- a preamplifier for microphone or playback,
- a recording amplifier with automatic level control,
- a dynamic limiter with a short limiting time.

Compared to its predecessor TDA1002, this type features an improved automatic level control circuit; the control range has been enlarged from 40 to 55 dB and the spread in control characteristic has been reduced to less than 2 dB.

QUICK REFERENCE DATA

Supply voltage range	V_P		4 to 12	V
Operating ambient temperature	T_{amb}		−25 to + 125	°C
Total quiescent current (V_P = 9 V)	I_{tot}	typ.	15	mA
Preamplifier				
Input impedance (pin 1)	$\|Z_i\|$	typ.	16	kΩ
Open loop gain	G_o	typ.	70	dB
Clipping level (pin 4); V_P = 9 V; r.m.s. value	$V_{4\text{-}5(rms)}$	typ.	2	V
Equivalent noise input voltage R_S = 500 Ω; B = 300 Hz to 15 kHz	$V_{n(rms)}$	<	0,75	μV
Recording amplifier				
Input impedance (pin 8)	$\|Z_i\|$	typ.	40	kΩ
Open loop gain	G_o	typ.	80	dB
Clipping level (pin 9); V_P = 9 V; r.m.s. value	$V_{9\text{-}10(rms)}$	typ.	2	V
Automatic Level Control (A.L.C.)				
Input impedance (pin 6)				
at low signal level at pin 8	$\|Z_i\|$	typ.	250	kΩ
at high signal level pin 8	$\|Z_i\|$	typ.	25	Ω
Control voltage				
$V_{4\text{-}5}$ = 10 mV; f = 1 kHz; V_P = 9 V	$V_{9\text{-}10}$	typ.	250	mV
$V_{4\text{-}5}$ = 1000 mV; f = 1 kHz; V_P = 9 V	$V_{9\text{-}10}$	typ.	750	mV
Limiting time (Fig. 12)	t_l	typ.	10	ms
Level setting time (Fig. 12)	t_s	typ.	4	s
Recovery time (Fig. 13)	t_r	typ.	35	s

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

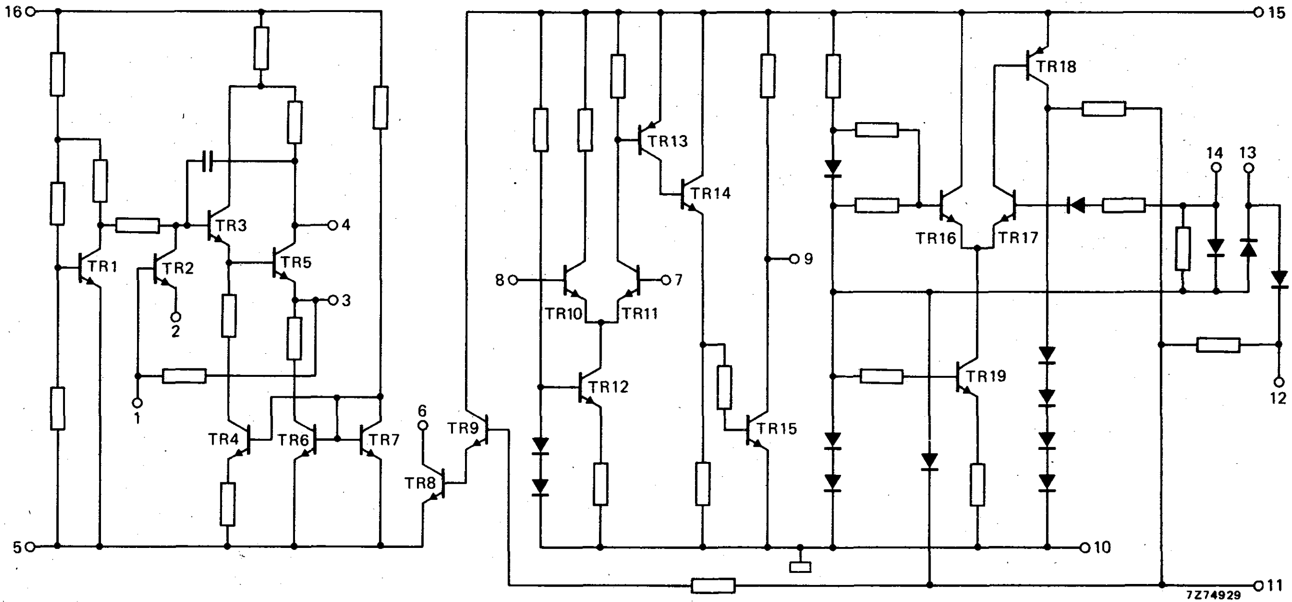


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage preamplifier	$V_{16\text{-}5}$	max.	12 V
Supply voltage recording amplifier	$V_{15\text{-}10}$	max.	12 V
Total power dissipation		see derating curve Fig. 2	
Storage temperature	T_{stg}		−65 to + 125 °C
Operating ambient temperature	T_{amb}		−25 to + 125 °C

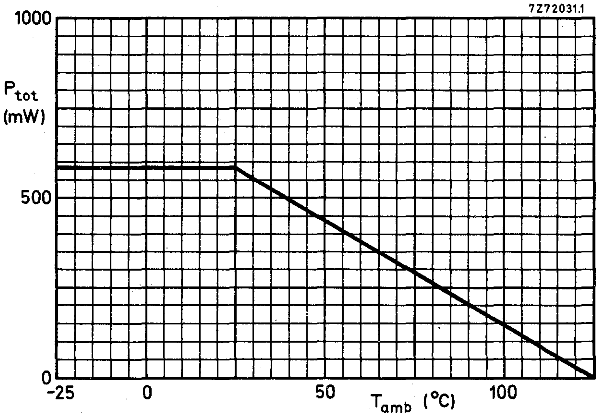


Fig. 2 Power dissipation derating curve.

D.C. CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified.

Supply voltage recording amplifier	$V_{15\text{-}10}$		4 to 12 V
Supply voltage preamplifier	$V_{16\text{-}5}$		4 to 12 V
Quiescent current rec. amplifier; V_P = 9 V	I_{15}	typ.	10 mA
Quiescent current preamplifier; V_P = 9 V	I_{16}	typ.	5 mA
Output voltage recording amplifier	$V_{9\text{-}10}$	typ.	½ V_P V
Output voltage preamplifier	$V_{4\text{-}5}$	typ.	½ V_P−0,35 V

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 9 V unless otherwise specified.

Preamplifier (note 1)			recording	playback
Open loop voltage gain	G_o	typ.	70	70 dB
Closed loop voltage gain at f = 1 kHz	G_c	typ.	38	45 dB
Output voltage (clipping level); r.m.s. value	$V_{4\text{-}5(rms)}$	typ.	2	2 V
Equivalent noise input voltage; r.m.s. value (note 2)	V_n	<	0,75	0,75 μV
Input impedance (pin 1)	$\lvert Z_i \rvert$	typ.	16	16 kΩ
Total harmonic distortion				
f = 1 kHz; $V_{4\text{-}5}$ = 150 mV	d_t	typ.	–	0,12 %
f = 1 kHz; $V_{4\text{-}5}$ = 500 mV	d_t	<	0,2	–
Amplitude response		flat: 20 Hz to 20 kHz		see Fig. 7

Recording amplifier (Fig. 9)			
with A.L.C.; unless otherwise specified.			
Open loop gain	G_o	typ.	80 dB
Closed loop voltage gain at f = 1 kHz (note 3)	G_c	typ.	49 dB
Output voltage (clipping level); r.m.s. value	$V_{9\text{-}10(rms)}$	typ.	2 V
Input impedance pin 8	$\lvert Z_i \rvert$	typ.	40 kΩ
Input impedance pin 6			
low signal levels	$\lvert Z_i \rvert$	typ.	250 kΩ
high signal levels	$\lvert Z_i \rvert$	typ.	25 Ω
Total harmonic distortion		see Fig. 11	
Amplitude response (note 3)		see Fig. 10	

Automatic level control (see Fig. 8)			
$V_{4\text{-}5}$ = 10 mV; f = 1 kHz	$V_{9\text{-}10}$	typ.	250 mV
$V_{4\text{-}5}$ = 100 mV; f = 1 kHz	$V_{9\text{-}10}$	typ.	450 mV
$V_{4\text{-}5}$ = 1000 mV; f = 1 kHz	$V_{9\text{-}10}$	typ.	750 mV
$V_{4\text{-}5}$ = 2000 mV; f = 1 kHz	$V_{9\text{-}10}$	typ.	880 mV
Limiting time (see Fig. 12)	t_l	typ.	10 ms
Level setting time (see Fig. 12)	t_s	typ.	4 s
Recovery time (see Fig. 13)	t_r	typ.	35 s

Notes

1. For recording see Fig. 3; for playback see Fig. 5.
2. R_S = 500 Ω; bandwidth = 300 Hz to 15 kHz.
3. Pin 6 not connected to pin 8.

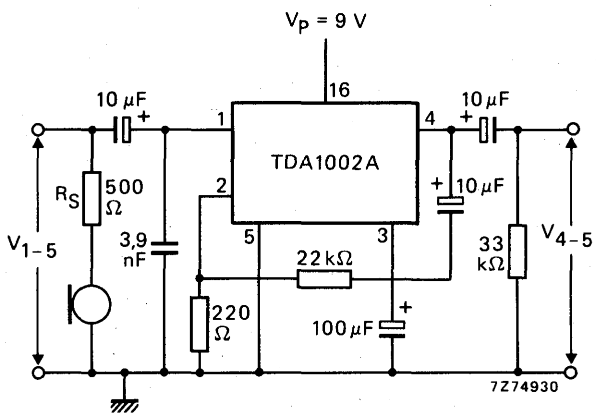


Fig. 3 Preamplifier used as microphone amplifier.

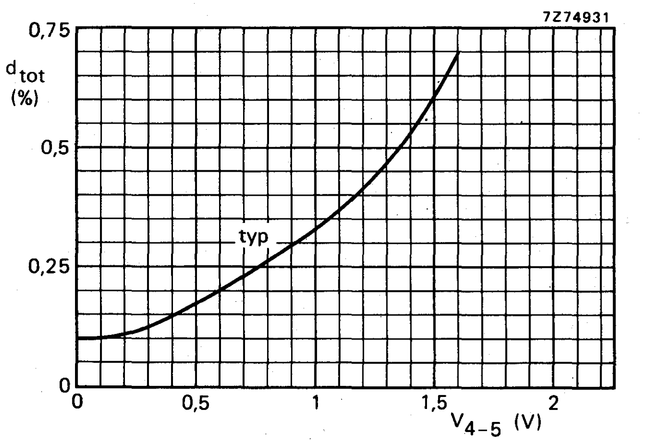


Fig. 4 Total harmonic distortion of preamplifier used for recording.

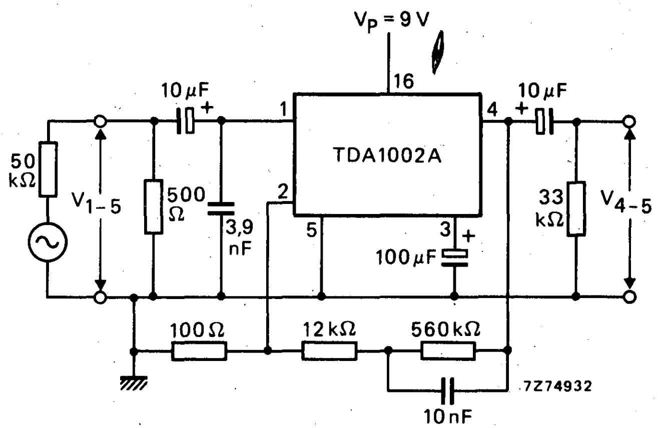


Fig. 5 Preamplifier used for playback.

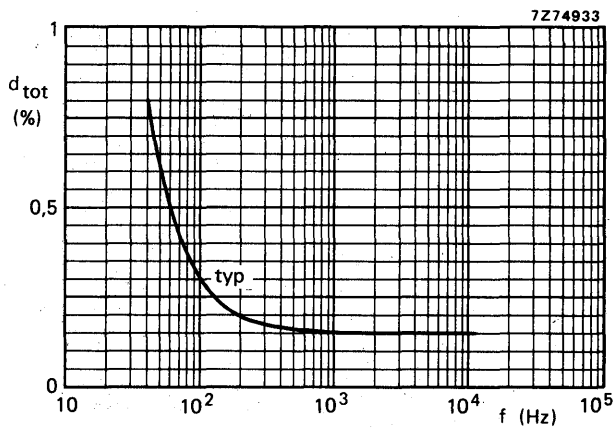


Fig. 6 Total harmonic distortion of preamplifier used for playback at $V_{4\text{-}5}$ = 150 mV.

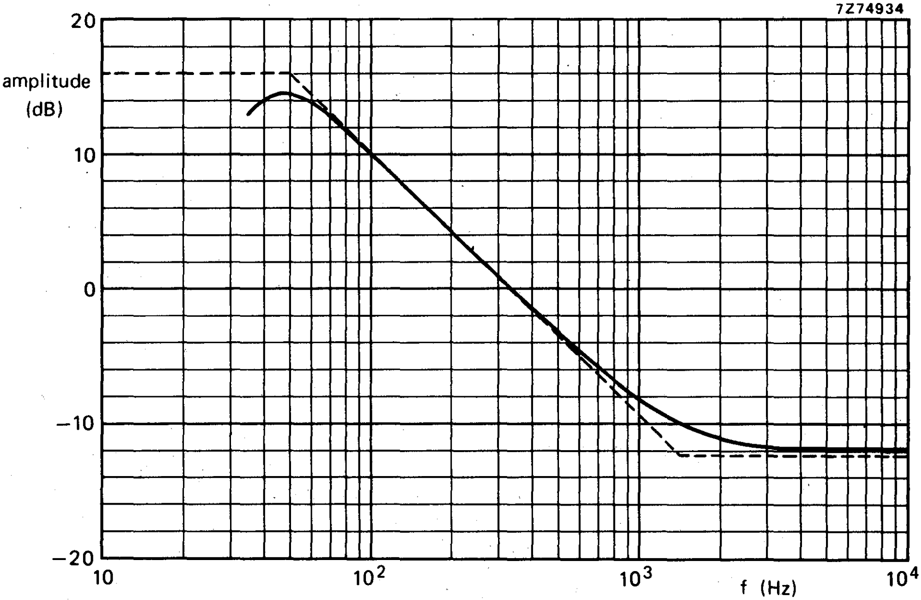


Fig. 7 Amplitude response of preamplifier used for playback; typical values.
0 dB = input voltage of 0,3 mV at f = 333 Hz. Dotted line according to DIN 45513.

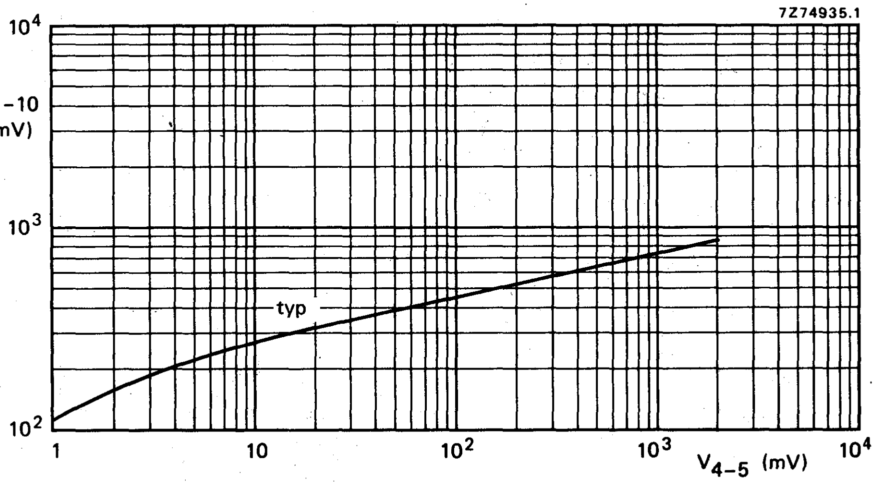


Fig. 8 Automatic level control; for circuitry see Fig. 9; f = 1 kHz.

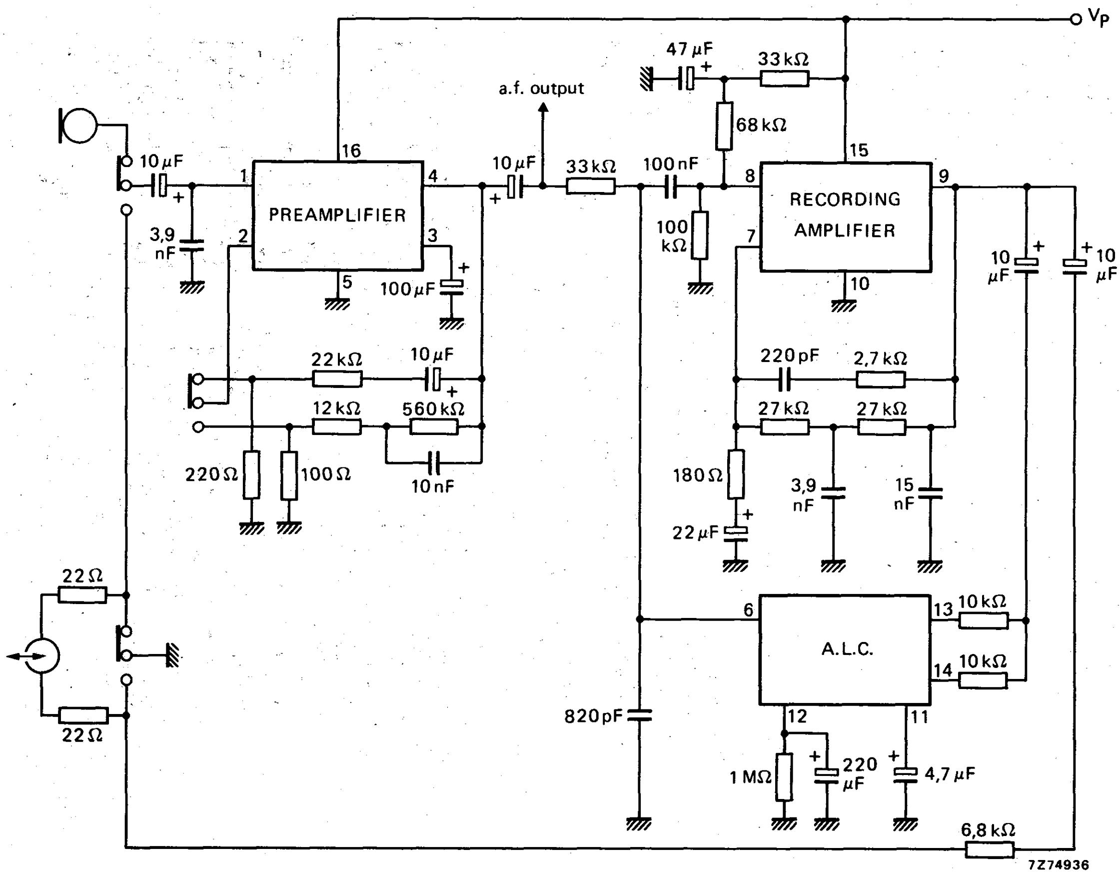


Fig. 9 Application of TDA1002A (recording position).

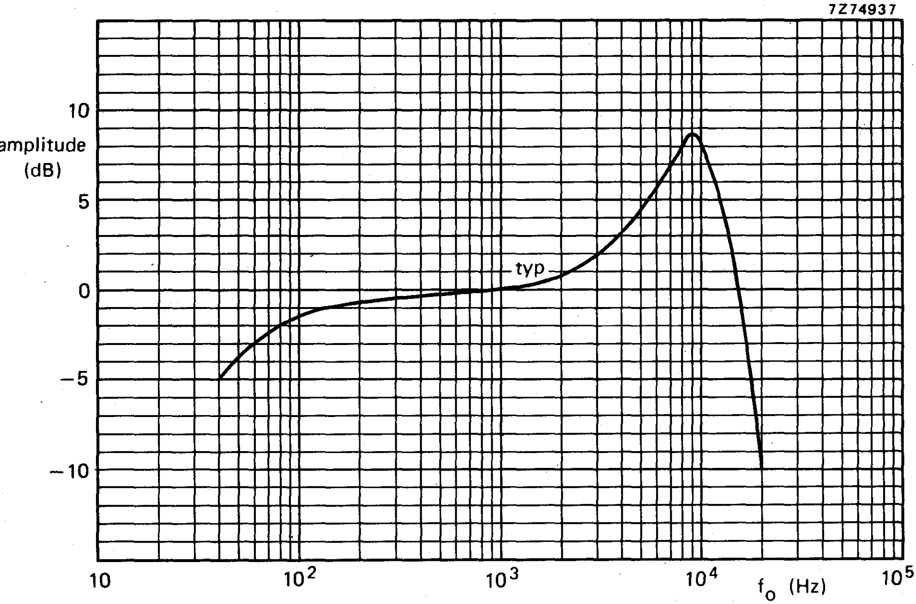


Fig. 10 Amplitude response of recording amplifier (A.L.C. not connected).

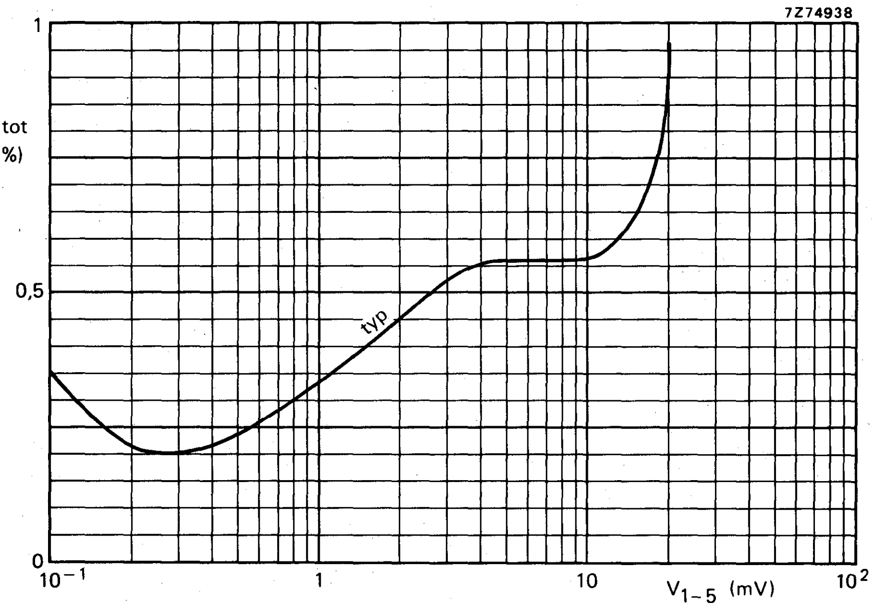
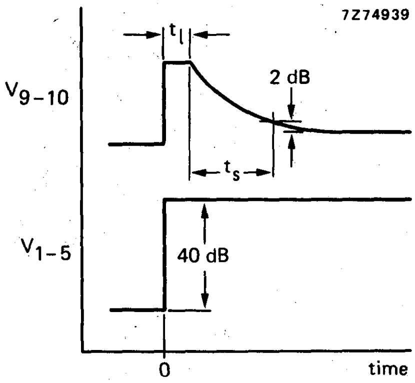


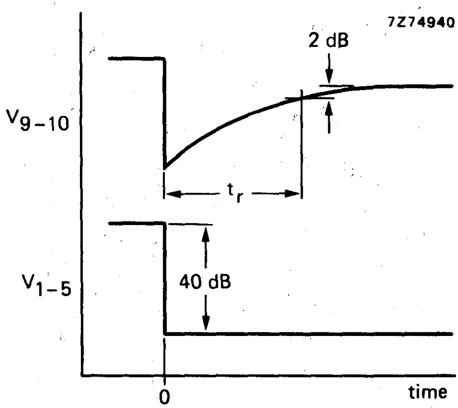
Fig. 11 Total harmonic distortion recording amplifier with A.L.C.; f = 1 kHz.

TIMING DIAGRAMS



t_l = limiting time.
t_s = level setting time.

Fig. 12 Output response at input level jumps.



t_r = recovery time.

Fig. 13 Output response at input level jumps.

MOTOR REGULATOR
AND BIAS/ERASE OSCILLATOR CIRCUIT

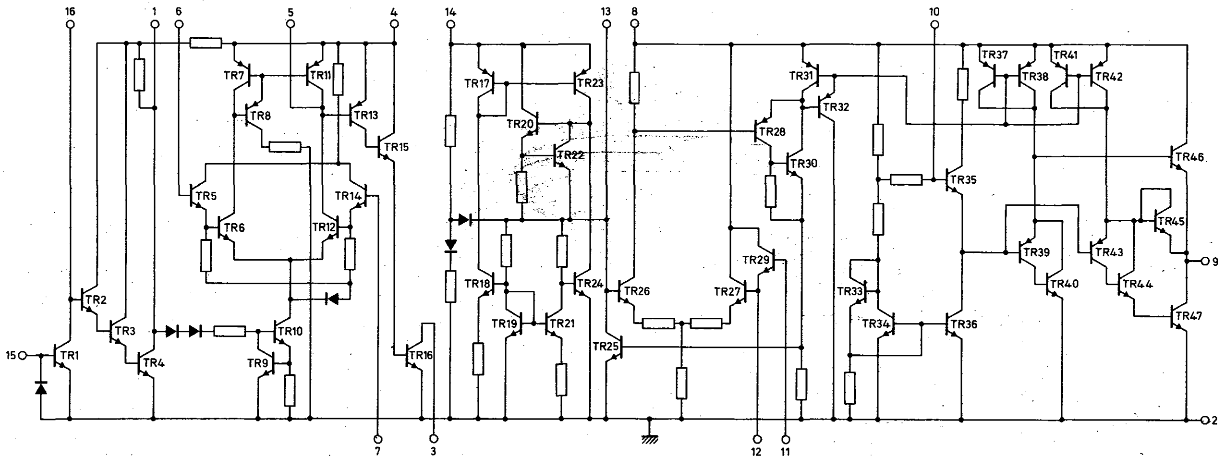
The TDA1003A is pin for pin compatible with the TDA1003 with an extension of features. The TDA1003A is for use in recording/playback systems. It incorporates capstan motor speed control, an automatic stop circuit, and a bias/erase oscillator.
The motor circuit controls the back e.m.f. and delivers a stabilized voltage to the capstan motor. The motor voltage is corrected for line voltage and torque variations, and temperature variations of the magnetic material and windings. The motor speed control is operative as long as a pulse train, derived from the tape wind spool mechanism via an interrupter, is applied to the automatic stop circuit. The TDA1003A can also be used without stop circuit by connecting pin 16 to ground. An output is available for a "stop" indicator lamp.
The oscillator section contains a temperature-independent voltage reference source and an a.g.c. circuit controlling the transconductance of a balanced oscillator circuit incorporating the erase head. Any Q variations of the erase head winding are fed back to maintain the oscillator output as a constant undistorted sine-wave so that harmonic products do not cause interference during radio recording.

QUICK REFERENCE DATA				
Supply voltage range	V_P		3,5 to 18	V
Ambient temperature	T_{amb}	typ.	25	°C
Supply voltage	V_P	typ.	9	V
Motor regulator				
Current consumption	I_4	typ.	1,8	mA
Motor starting current	I_3	<	1000	mA
Operating motor current	I_3	<	250	mA
Minimum operating voltage at I_3 = 600 mA	$V_{3\text{-}2min}$	typ.	0,9	V
Supply voltage rejection	$\Delta V_{3\text{-}2}/\Delta V_{4\text{-}2}$	typ.	1	mV/V
Stop circuit				
Output current for "stop" indicator lamp	I_1	<	100	mA
Knee voltage at I_1 = 100 mA	$V_{1\text{-}2}$	typ.	0,6	V
Input current for I_1 = 100 mA	I_{16}	>	4	μA
Bias and erase oscillator				
Current consumption at Q = 40	I_8	typ.	25	mA
Erase head voltage at Q = 40 (r.m.s. value)	$V_{erase(rms)}$	typ.	16	V

PACKAGE OUTLINE

16-lead DIL; plastic power (SOT-38N).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages

Supply voltage on: pin 4	V_{4-2}	max.	18	V
pin 8	V_{8-2}	max.	18	V
pin 14	V_{14-2}	max.	18	V

Currents

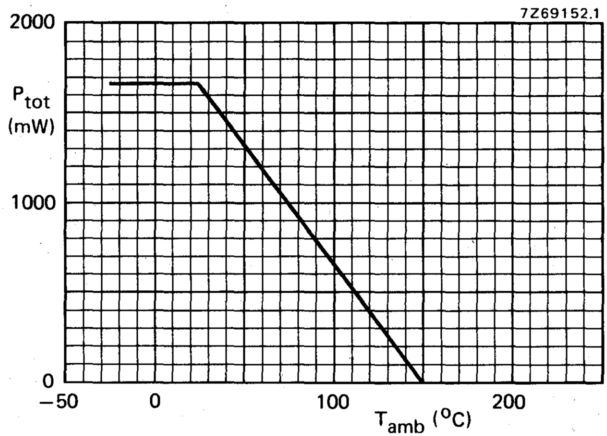
Motor current (pin 3; peak-value)	I_{3M}	max.	1000	mA
"Stop" indicator lamp current (d.c.; pin 1)	I_1	max.	100	mA
Maximum input current (pin 15)	$\pm I_{15\,max}$	max.	20	mA

Temperatures

Storage temperature	T_{stg}	−65 to +150	°C
Operating ambient temperature see also power derating curve below	T_{amb}	−20 to +150	°C

Power dissipation

Total power dissipation — see derating curve below



CHARACTERISTICS at V_P = 9 V; T_{amb} = 25 °C unless otherwise specified; see test circuit on page 6

Supply voltage range (pins 4, 8 and 14)	V_P		3,5 to 18	V	1)
Motor regulator					
Current consumption	I_4	typ.	1,8 1 to 3	mA mA	
Operating motor current	I_3	<	250	mA	
Motor starting current (peak-value)	I_{3M}	<	1000	mA	
Input offset voltage at I_3 = 3 mA	$\lvert V_{7-6}\rvert$	typ. <	2 8	mV mV	
Input offset current at I_3 = 3 mA	$\lvert I_{7-6}\rvert$	typ.	0,2	µA	
Input voltage range (common mode)	V_{6-2} V_{7-2}		2,4 to (V_P-0,25) 2,4 to (V_P-0,25)	V V	
Input bias current	I_6; I_7	typ. <	0,1 1,0	µA µA	
Input sensitivity (for ΔI_3 = 100 mA)	ΔV_{7-6}	typ. <	1 10	mV mV	
Minimum operating voltage at I_3 = 600 mA	$V_{3-2\,min}$	typ. <	0,9 1,8	V V	2)
Automatic motor "stop" circuit					
"Stop" indicator lamp current } V_{15-2} = low ("stop" condition)	I_1	<	100	mA	
Knee voltage at I_1 = 100 mA } V_{15-2} = low ("stop" condition)	V_{1-2}	typ. <	0,6 1,0	V V	
Input current for I_1 = 100 mA } V_{15-2} = low ("stop" condition)	I_{16}	>	4	µA	
Voltage at pin 1 without external load (V_{16} = low)	V_{1-2}	typ.	4,1 3 to 5,0	V V	
Maximum input current (pin 15)	$\pm I_{15\,max}$	<	20	mA	

1) To guarantee proper functioning with V_P = 3,5 V to 18 V, the external component values as shown in test circuit on page 6 should be modified.

2) The minimum operating voltage is defined as the voltage (V_{3-2}) at which the motor still operates at correct speed.

CHARACTERISTICS (continued)

Bias and erase oscillator

Current consumption at Q = 40	I_8	typ.	25	mA
at Q = 20	I_8	typ.	38	mA
		<	46	mA
Internal current limiting	I_8	<	95	mA [1]
Peak output current	$\pm I_9$	>	100	mA
Output voltage swing (peak-to-peak value)	$V_{9-2(p-p)}$	typ.	V_P-2	V
Current consumption of reference source	I_{14}	typ.	1,8	mA
		<	2,4	mA
Reference voltage (temperature compensated) [2]	V_{13-2}	typ.	1,7	V
			1,55 to 1,9	V
Erase head voltage; Q = 40; L = 620 μH (r.m.s. value)	$V_{erase(rms)}$	typ.	16	V
Change of V_{erase} when Q changes from 20 to 60	ΔV_{erase}	typ.	1	V
		<	1,8	V

APPLICATION INFORMATION measured in circuit on page 7

Motor regulator

Supply voltage rejection	$\frac{\Delta V_{3-2}}{\Delta V_{4-2}}$	typ.	1	mV/V
Motor speed variation over T_{amb} = −5 to +55 °C	$\pm\Delta n$	typ.	2	%

Automatic motor "stop" circuit

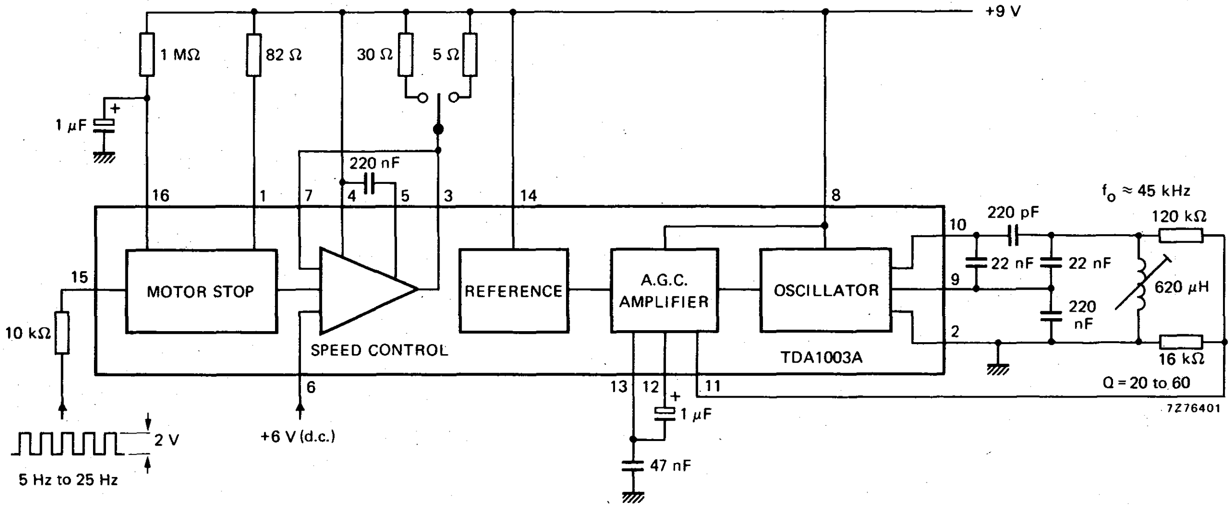
Input voltage from wind spool supplied via 10 kΩ to pin 15 (peak-to-peak value)	$V_{W(p-p)}$	typ.	1,2	V
Input current (pin 15)	$\pm I_{15}$	<	20	mA

Bias and erase oscillator

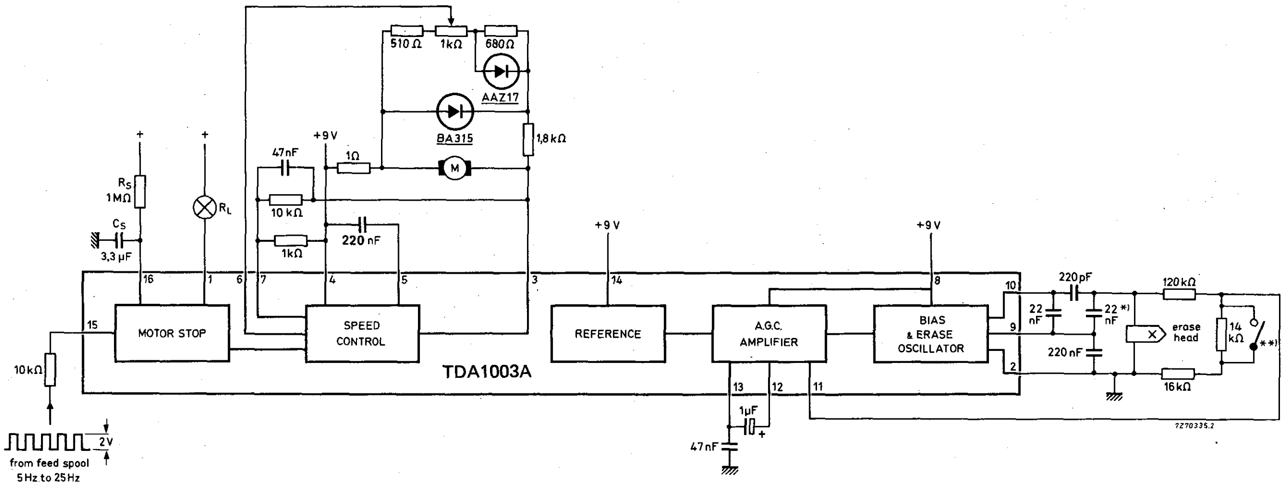
Erase head voltage for Q = 40; L = 620 μH (r.m.s. value)	$V_{erase(rms)}$	typ.	16	V
Change of V_{erase} when Q changes from 20 to 60	ΔV_{erase}	typ.	1	V
Harmonic distortion (unsaturated erase head)	$-\alpha_{2^{nd}harm}$	typ.	55	dB [3]
	$-\alpha_{3^{rd}harm}$	typ.	40	dB
	$-\alpha_{>6^{th}harm}$	>	80	dB

[1]) If erase head is defective.
[2]) Typical value of temperature coefficient 0 mV/°C.
[3]) At unsaturated erase head, with respect to 45 kHz.

TEST CIRCUIT



APPLICATION INFORMATION (continued)



Indicator lamp: 9 V; 40 mA

Motor (M): R_a = 14 Ω
E_n = 2, 3 V at 1500 r. p. m.

Erase head: L = 620 μH
Q = 40
f_o = 45 kHz

*) Capacitor with low losses required; especially for CrO_2 tape and low battery voltage.

**) Switch closed: suitable for CrO_2 tape
open : suitable for Fe_2O_3 tape.

10 W AUDIO POWER AMPLIFIER

with thermal shut-down

The TDA1004A is a monolithic integrated circuit in a plastic 16-lead power dual in-line package, intended for use as a low-frequency class-B amplifier.
This circuit can also be used in car radios, even when 2 Ω load is required.
The device provides 10 W output power at 20 V/4 Ω; 6 W at 14 V/4 Ω and 7,5 W at 14 V/2 Ω. The supply voltage ranges from 9 to 20 V.
The TDA1004A is pin for pin compatible with the TDA1004.
The d.c. and a.c. gain are equal, which means an external feedback network is not necessary.
The circuit comprises two separate amplifiers with the following features:

- low-cost and small number of external components;
- thermal limiting circuit, the gain of the circuit decreases when the crystal temperature exceeds 150 °C;
- continuous short-circuit protection of the load for supply voltages up to 16 V;
- very good ripple rejection;
- low input impedance;
- low thermal resistance of the package thus requiring relatively small heatsinks;
- filtered but not stabilized supply (pin 6) available for other electronic functions.

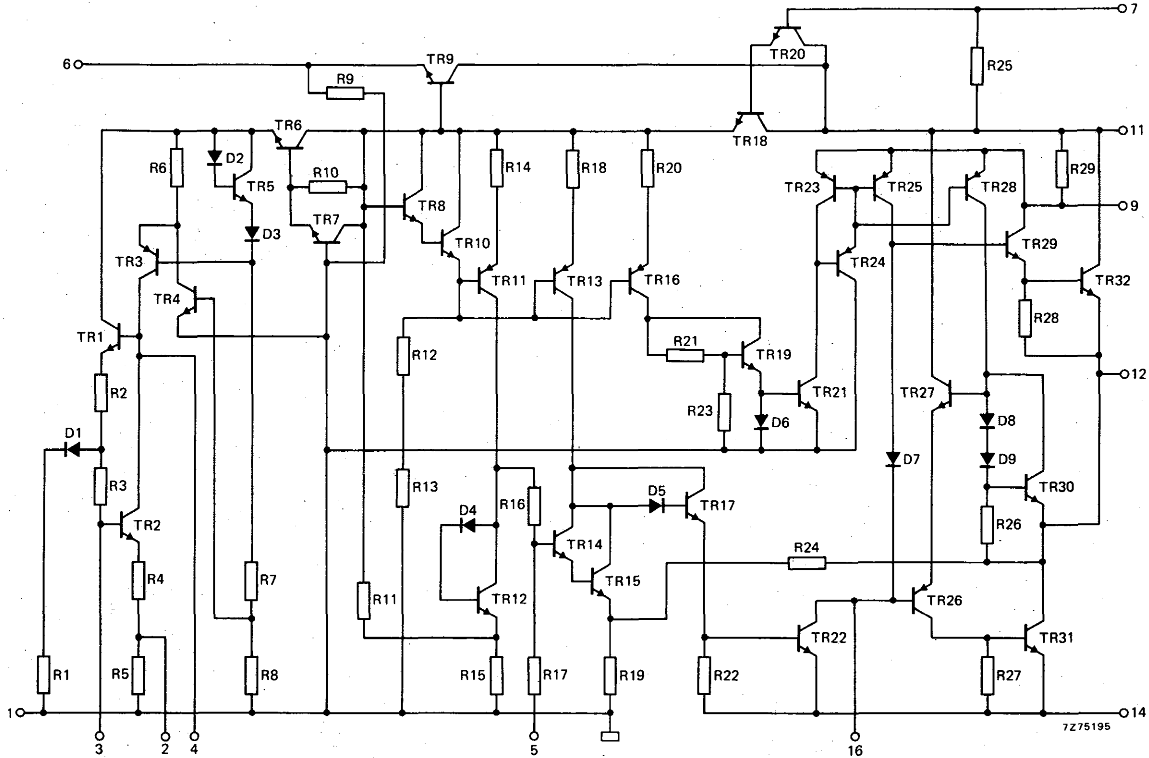
QUICK REFERENCE DATA

Supply voltage range	V_P		9 to 20	V
D.C. output current (peak value)	I_{OM}	<	2,5	A
Output power at d_{tot} = 10%				
at V_P = 14 V; R_L = 4 Ω	P_o	typ.	6,2	W
at V_P = 14 V; R_L = 2 Ω	P_o	typ.	7,0	W
at V_P = 20 V; R_L = 8 Ω	P_o	typ.	7,0	W
at V_P = 20 V; R_L = 4 Ω	P_o	typ.	11,0	W
Total harmonic distortion at P_o < 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance	$\lvert Z_i \rvert$	typ.	20	kΩ
Total quiescent current at V_P = 14 V	I_{tot}	typ.	30	mA
Sensitivity at P_o = 1 W; R_L = 4 Ω	V_i	typ.	6,6	mV
Operating ambient temperature	T_{amb}		−25 to +150	°C
Storage temperature	T_{stg}		−55 to +150	°C

PACKAGE OUTLINE

16-lead DIL; plastic power (SOT-69B).

CIRCUIT DIAGRAM



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage	V_P	max.	24	V

Currents

Repetitive peak output current (pins 11, 12, 14)	I_{ORM}	max.	2,5	A
Non-repetitive peak output current (pins 11, 12, 14)	I_{OSM}	max.	5,0	A
Supply current from pin 6	I_6	max.	30	mA

Power dissipation

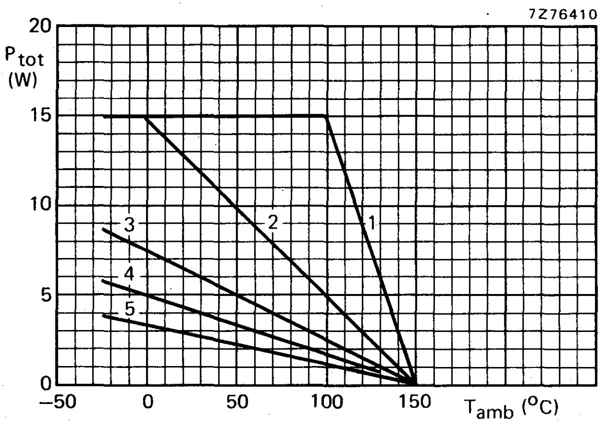
Total power dissipation — see derating curve below

Temperatures

Storage temperature	T_{stg}	−55 to +150	°C
Operating ambient temperature	T_{amb}	−25 to +150	°C

Short-circuiting

A.C. short-circuit duration of load impedance during sine-wave signal drive; without heatsink at V_P = 14 V	t_{sc}	max.	100	hours



1. Infinite heatsink
2. External heatsink of 100 cm^2
3. External heatsink of 30 cm^2
4. External heatsink of 12 cm^2
5. In free air; without external heatsink

Heatsink: blackened aluminium area.

THERMAL RESISTANCE (The power derating curve on page 3 is based on the following data)

From junction to case	$R_{th\ j\text{-}c}$	=	3,3	°C/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	45	°C/W

CHARACTERISTICS

D.C. characteristics

Supply voltage range (pin 11)	V_P		9 to 20	V
Supply voltage (pin 6) at I_6 = 0 mA	V_{6-1}	>	11,0	V
at I_6 = 20 mA	V_{6-1}	>	10,8	V
Output current (peak value)	I_{OM}	<	2,5	A
Output current at pin 6 (peak value)	I_{6M}	<	30	mA
Total quiescent current at V_P = 14 V	I_{tot}	typ.	30	mA
		<	90	mA

A.C. characteristics at T_{amb} = 25 °C; V_P = 14 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also test circuit on page 5.

A.F. output power at d_{tot} = 10% [1]				
at V_P = 14 V; R_L = 4 Ω; without bootstrap [2]	P_o	>	4,8	W
at V_P = 14 V; R_L = 4 Ω, with bootstrap [1]	P_o	>	5,5	W
		typ.	6,2	W
at V_P = 14 V; R_L = 2 Ω, with bootstrap [1]	P_o	typ.	7,0	W
at V_P = 20 V; R_L = 8 Ω, with bootstrap [1]	P_o	typ.	7,0	W
at V_P = 20 V; R_L = 4 Ω, with bootstrap [1]	P_o	typ.	11,0	W
Voltage gain				
preamplifier	G_{v1}	typ.	20	dB
			17 to 23	dB
power amplifier	G_{v2}	typ.	30	dB
			27 to 33	dB
total amplifier	$G_{v\ tot}$	typ.	50	dB
			47 to 53	dB
Total harmonic distortion at P_o = 1 W	d_{tot}	typ.	0,2	%
		<	1,0	%
Frequency response (−3 dB)	B		60 Hz to 17	kHz
Input impedance: preamplifier	$\lvert Z_i \rvert$	>	15	kΩ
		typ.	20	kΩ
power amplifier	$\lvert Z_i \rvert$	typ.	30	kΩ
Output impedance of preamplifier (pin 4)	$\lvert Z_o \rvert$	>	10	kΩ [3]

[1]) Output power is always measured at the d.c. output of the amplifier, so losses in coupling capacitor are not taken into account.

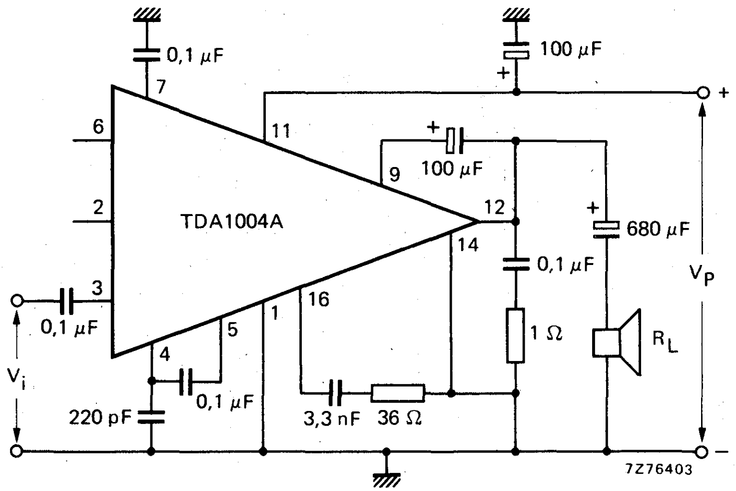
[2]) See circuit on page 7. With this circuit 4,8 W is guaranteed.

[3]) At this impedance value from pin 4 to ground, the maximum output power can be delivered.

CHARACTERISTICS (continued)

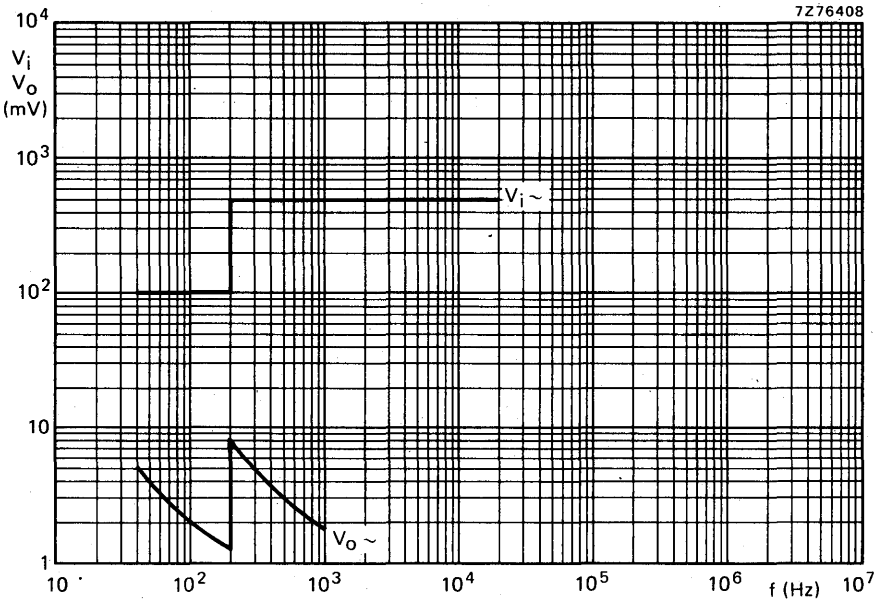
Output voltage preamplifier at d_{tot} = 5% (r.m.s. value)	$V_{4-1(rms)}$	>	0,6	V	1)
		typ.	1,0	V	
Noise output voltage at R_S = 0 Ω	V_n	typ.	0,3	mV	2)
at R_S = 2 kΩ	V_n	<	1,0	mV	
Sensitivity at P_o = 1 W	V_i	typ.	6,6	mV	
Ripple rejection at f = 100 Hz	RR	typ.	32,5	dB	3)
at f = 1 kHz	RR	typ.	50,0	dB	

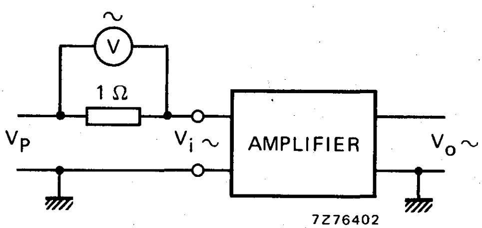
Test circuit



1) Measured with a 30 kΩ a.c. load impedance at pin 4 (disconnected from pin 5).
2) Measured at a bandwidth of 60 Hz to 15 kHz.
3) See ripple rejection on page 6.

RIPPLE REJECTION



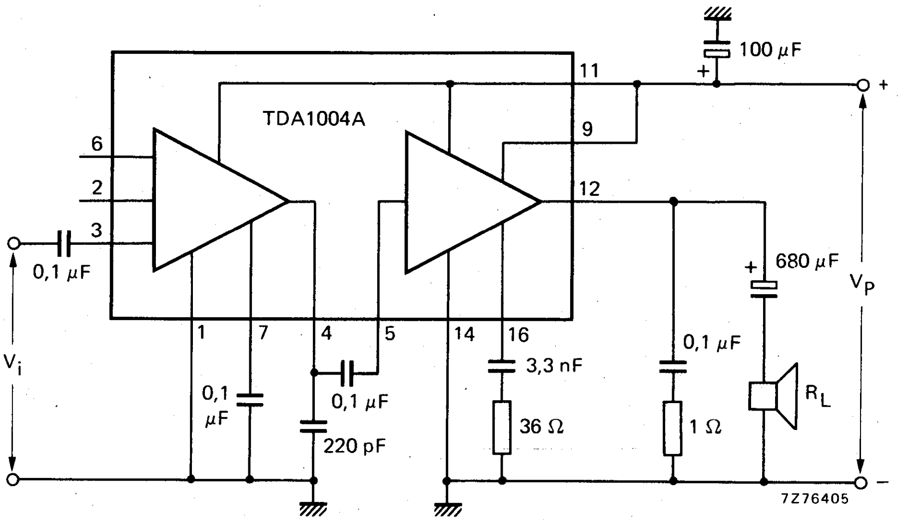


Typical ripple rejection measured with nominal load impedance (R_L = 4 Ω) and input a.c. short-circuited.

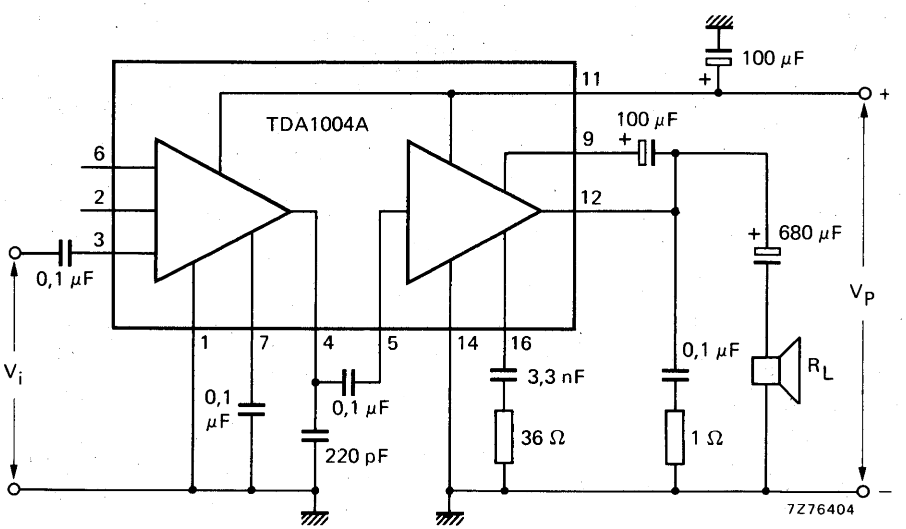
$V_{o\,max}$ = 4 mV at f = 10^3 Hz.

APPLICATION INFORMATION

Without bootstrap

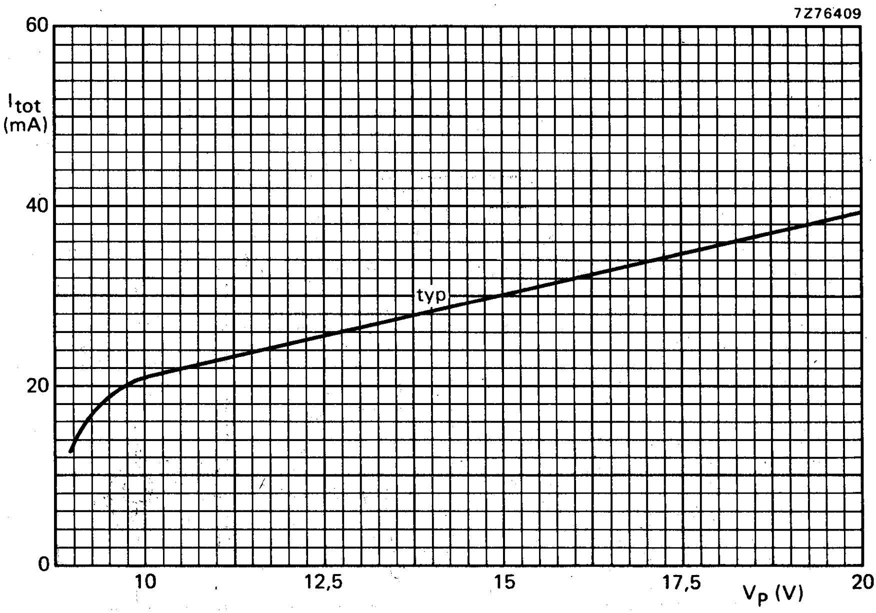


With bootstrap



APPLICATION INFORMATION (continued)

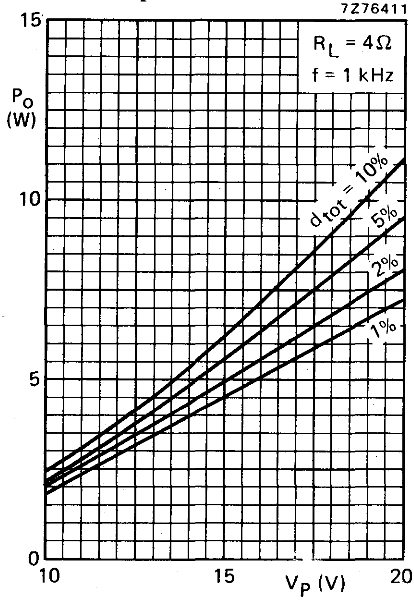
Supply voltage (V_{11-14})	V_P	14			20		V
Load resistance	R_L	2	4	8	4	8	Ω
Total quiescent current	I_{tot}	30	30	30	40	40	mA
Output power at d_{tot} = 10%							
with bootstrap	P_o	7,0 [1]	6	3,5	12	7	W
without bootstrap	P_o	7,5	5	3,0	11	6	W
Distortion at P_o = 2 W	d_{tot}	1	0,2	0,2	0,2	0,2	%
Input sensitivity for P_o = 1 W	V_i	4,8	6,6	9,1	6,6	9,1	mV
Ripple rejection at f = 100 Hz	RR	32,5	32,5	32,5	32,5	32,5	dB
at f = 1 kHz	RR	50,0	50,0	50,0	50,0	50,0	dB
Noise output voltage at B = 60 Hz to 15 kHz							
R_S = 0 Ω	V_n	0,30	0,30	0,30	0,30	0,30	mV
R_S = 2 kΩ	V_n	0,45	0,45	0,45	0,45	0,45	mV
Input impedance	$\|Z_i\|$	23	23	23	23	23	kΩ
Maximum power dissipation	P_{tot}	5,2	2,8	1,6	5,5	3,0	W

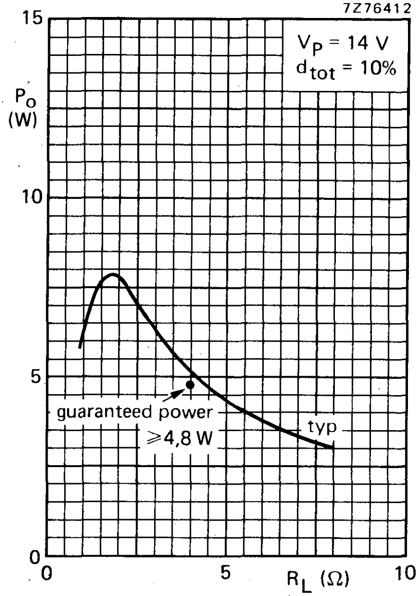


[1]) P_o = 9 W, when a resistor of 220 Ω is connected between pins 9 and 11.

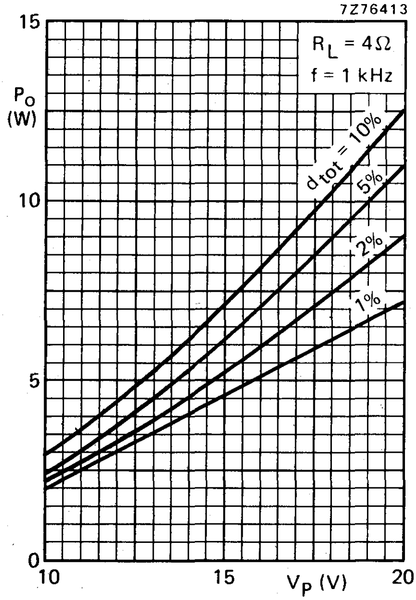
APPLICATION INFORMATION (continued)

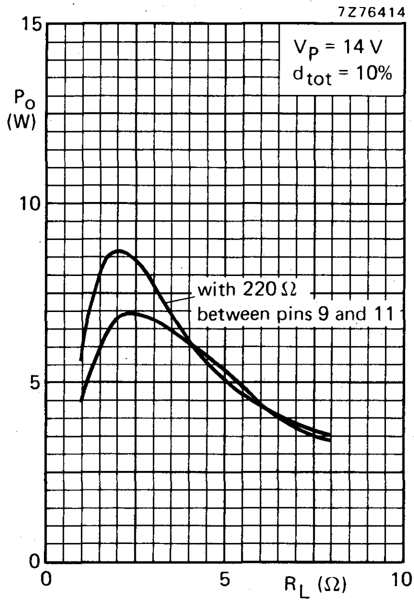
Without bootstrap





With bootstrap

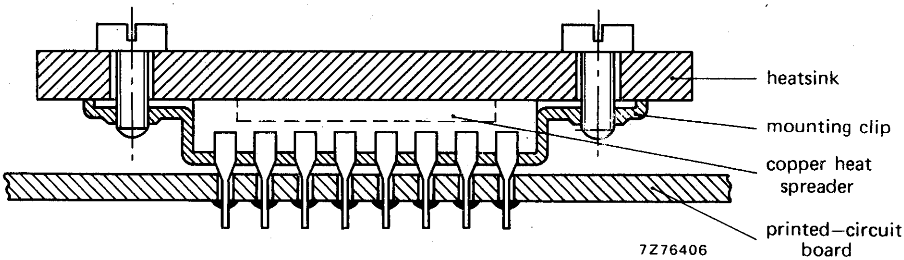




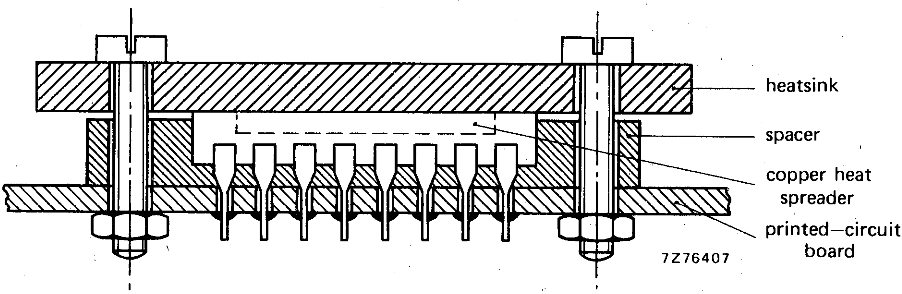
MOUNTING INSTRUCTIONS

When using an external heatsink, connected to the heat spreader of the IC, the thermal power in the circuit can be reduced to a negligible value.
The optimum heatsink dimensions (blackened aluminium) for a given operating ambient temperature, can be found from the derating curves on page 3.
The fact that the thermal resistance of the encapsulation is very good, results in a relatively small heatsink for thermal power reduction; e.g. $P_o = 2$ W at $T_{amb} = 50$ °C can be obtained without an external heatsink.
Two mounting methods are shown below.
By using these methods, no extra copper area is required on the printed-circuit board, so a saving in printed-wiring area is obtained.
Mounting the external heatsink can be done by screwing or clipping.
Mechanical stresses do not damage the IC.
It is recommended that a heatsink-compound be used between IC heat spreader and heatsink.

Method 1



Method 2



FREQUENCY MULTIPLEX PLL STEREO DECODER

The TDA1005A is a high quality PLL stereo decoder based on the frequency-division multiplex (f.d.m.) principle, performing:

- excellent ACI (Adjacent Channel Interference) and SCA (Storecast) rejection
- very low BFC (Beat-Frequency Components) distortion in the higher frequency region

The circuit incorporates the following features:

- with simplified peripheral circuitry the circuit can perform as a time-division multiplex (t.d.m.) decoder, for use in economic medium and low-class apparatus
- for car radios: operation at a supply voltage of 8 V
- extra pin for smooth mono/stereo take-over without "clicks"
- automatic mono/stereo switching (minimum switching level is 16 mV), controlled by both pilot signal and field strength level
- low distortion in the loop resonance frequency region (≈ 300 Hz; THD = 0,2% typ.)
- external adjustment for obtaining optimum channel separation in the complete receiver
- internal amplification: t.d.m., 7 dB; f.d.m., 10 dB
- driver for stereo indicator lamp
- externally switchable: VCO-off or mono condition
- guaranteed VCO capture range (> 3,5% or 2,7 kHz)

QUICK REFERENCE DATA

Supply voltage range	$V_{8\text{-}16}$		8 to 18		V
Supply voltage	$V_{8\text{-}16}$	typ.		15	V
Ambient temperature	T_{amb}	typ.		25	°C
Measured at $V_{i(p\text{-}p)}$ = 1 V (MUX signal with 8% pilot)			t.d.m.	f.d.m.	
Channel separation at f = 1 kHz	α	typ.	50	55	dB
Carrier suppression					
at f = 19 kHz	α_{19}	typ.	36	36	dB
at f = 38 kHz	α_{38}	typ.	45	40	dB
at f = 76 kHz	α_{76}	typ.	80	75	dB
ACI rejection at f = 114 kHz	α_{114}	typ.	52	70	dB
SCA rejection at f = 67 kHz	α_{67}	typ.	85	90	dB
VCO capture range		>	3,5	3,5	%
Total harmonic distortion					
f_m = 1 kHz	THD	typ.	0,2	0,1	%
f_m = 300 Hz to 10 kHz	THD	typ.	0,2	0,1	%
BFC suppression	d_{BFC}	>	40	60	dB

PACKAGE OUTLINES

TDA1005A ; 16-lead DIL; plastic (SOT-38).
TDA1005AT; 16-lead flat pack; plastic (SO-16; SOT-109A).

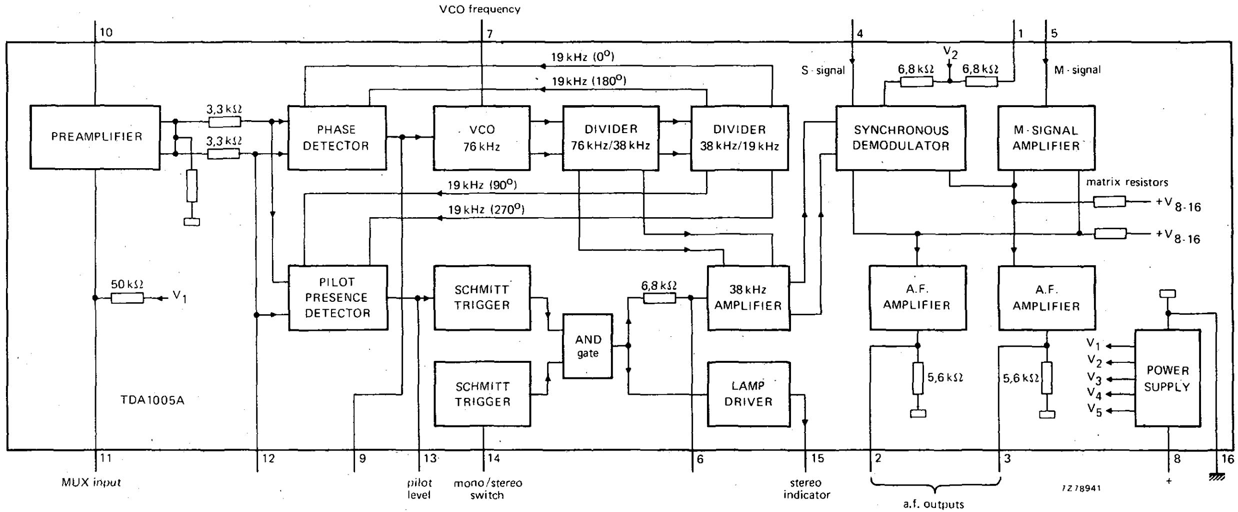


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_{8\text{-}16}$	max.	18	V
Indicator lamp voltage	$V_{15\text{-}16}$	max.	22	V
Mono/stereo switching voltage	$V_{14\text{-}16}$	max.	4	V
Indicator lamp current	I_{15}	max.	100	mA
Indicator lamp turn-on current (peak value)	I_{15M}	max.	200	mA
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature (see also Fig. 2)	T_{amb}	−25 to + 150		°C

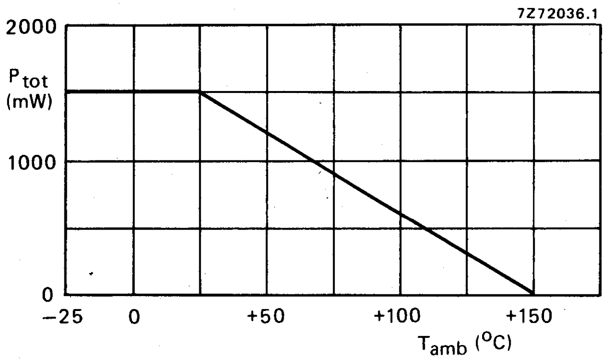


Fig. 2 Power derating curve.

A.C. CHARACTERISTICS and APPLICATION INFORMATION

T_{amb} = 25 °C; $V_{8\text{-}16}$ = 15 V (unless otherwise specified); see also Fig. 7 and Fig. 10.

	note	pin	parameter		t.d.m.	f.d.m.	unit
Channel separation see Figs 23 and 24	1, 2	2, 3	α	> typ.	40 50	45 55	dB dB
F.M.—I.F. roll-off correction range	1, 2				48 to 72	—	kHz
Input MUX-voltage; L = 1; R = 1 for THD < 0,35%	1, 2	11	$V_{i(p\text{-}p)}$	typ.	1	1	V
Input impedance		11	$\|Z_i\|$	> typ.	35 50	35 50	kΩ kΩ
Voltage gain per channel	1, 2		G_v	typ.	7	10	dB
Channel balance	1, 2		$\pm\Delta G_v$	<	1	1	dB
Output voltage (r.m.s. value) L = 1; R = 1	1, 2	2 3	$V_{2\text{-}16(rms)}$ $V_{3\text{-}16(rms)}$	> >	0,61 0,61	0,97 0,97	V V
Output impedance	3	2, 3	$\|Z_o\|$	typ.	5,6 4 to 7	5,6 4 to 7	kΩ kΩ
Total harmonic distortion; see Figs 25 and 26							
f_m = 1 kHz (all conditions)	1	2, 3	THD	typ.	0,2	0,1	%
f_m = 1 kHz; L = 1; R = 1	1	2, 3	THD	<	0,35	0,35	%
f_m = 300 Hz to 10 kHz		2, 3	THD	typ.	0,2	0,1	%
Carrier suppression		2, 3					
f = 19 kHz; without notch filter	1		α_{19}	typ.	36	36	dB
f = 19 kHz; with notch filter	1, 9		α_{19}	typ.	60	60	dB
f = 38 kHz; without notch filter	1		α_{38}	>	40	38	dB
f = 38 kHz; with notch filter	1, 9		α_{38}	>	72	72	dB
f = 57 kHz; without notch filter	1		α_{57}	typ.	46	56	dB
f = 57 kHz; with notch filter	1, 9		α_{57}	typ.	59	61	dB
f = 76 kHz; without notch filter	1		α_{76}	typ.	80	75	dB
ACI rejection		2, 3					
at f = 114 kHz	4		α_{114}	typ.	52	70	dB
at f = 190 kHz	4		α_{190}	typ.	55	74	dB
SCA rejection at f = 67 kHz	5	2, 3	α_{67}	typ.	85	90	dB
Ripple rejection; f = 100 Hz; $V_{8\text{-}16(rms)}$ = 200 mV			RR	> typ.	40 50	40 50	dB dB

	note	pin	parameter		t.d.m.	f.d.m.	unit
VCO; adjustable with $R_{7\text{-}16}$							
nominal frequency	6		f_{VCO}	typ.	76	76	kHz
capture range (deviation from 76 kHz centre frequency) 19 kHz pilot signal of 32 mV	6			>	3,5	3,5	%
temperature coefficient							
uncompensated	6		–TC	typ.	450.10^{-6}	450.10^{-6}	K^{-1}
compensated	6		± TC	typ.	200.10^{-6}	200.10^{-6}	K^{-1}
Stereo/mono switch							
when equal to 19 kHz pilot-tone threshold voltage; adjustable with $R_{13\text{-}8}$	7	11	V_i		10 to 100	10 to 100	mV
when equal to threshold voltage at $R_{13\text{-}8}$ = 620 kΩ							
for switching to stereo		11	V_i		7 to 16	7 to 16	mV
for switching to mono		11	V_i	<	5	5	mV
hysteresis	8	11	ΔV_i	typ.	2,5	2,5	dB
Smooth take-over circuit							
full mono	8	6	$V_{6\text{-}16}$	<	0,65	0,65	V
full stereo	8	6	$V_{6\text{-}16}$	>	1,3	1,3	V

Notes
1. $V_{i(p\text{-}p)}$ = 1 V (MUX signal with 8% pilot level).
2. f_m = 1 kHz.
3. At supply voltages of 8 to 11 V, resistors of 5,6 kΩ have to be connected from ground to pins 2 and 3.
4. Measured with a composite input signal: L = R; f_m = 1 kHz; 90% M-signal; 9% pilot signal; 1% spurious signal of 110 kHz (for α_{114}) or 186 kHz (for α_{190}).
   ACI suppression is defined as: $20 \log \frac{V_o \text{ (at 4 kHz)}}{V_o \text{ (at 1 kHz)}}$.
5. Measured with a composite input signal: L = R; f_m = 1 kHz; 80% S-signal; 9% pilot signal; 10% SCA carrier (67 kHz); $d_{13} = 20 \log \frac{V_o \text{ (at 9 kHz)}}{V_o \text{ (at 1 kHz)}}$.
6. See also Figs 7 and 10; compensated with RC network on pin 7.
7. Adjustable with $R_{13\text{-}8}$; see also Fig. 28; for field strength dependent input (pin 14) see next page.
8. $\Delta V_i = 20 \log \frac{V_{11\text{-}16} \text{ (mono/stereo)}}{V_{11\text{-}16} \text{ (stereo/mono)}}$.
   For additional circuitry on pin 6 see Figs 7 and 10; for graph see Fig. 29.
9. For example of notch filter see Fig. 6.

D.C. CHARACTERISTICS

T_{amb} = 25 °C; $V_{8\text{-}16}$ = 15 V (unless otherwise specified)

Supply voltage range	$V_{8\text{-}16}$		8 to 18	V *
Total current (except indicator lamp)	I_8	typ.	21	mA
Power dissipation (operating) at lamp current I_{15} = 100 mA; $V_{8\text{-}16}$ = 18 V	P_{tot}	<	570	mW
Saturation voltage of lamp driver at I_{15} = 100 mA	$V_{15\text{-}16}$	typ.	0,9	V
Maximum lamp driver voltage	$V_{15\text{-}16}$	<	22	V
Switching voltage				
to mono	$V_{14\text{-}16}$	>	1,2	V **
to stereo	$V_{14\text{-}16}$	<	0,65	V
hysteresis	$V_{14\text{-}16}$	typ.	0,2	V

APPLICATION NOTES

1. Switching-off the VCO

If the internal gain is used with A.M. reception, the VCO can be switched off by connecting pin 9 via a 100 kΩ resistor to ground (no h.f. signal on the leads), or connecting pin 7 to ground.

2. Mono button

The decoder can be switched to the mono position by connecting pin 12 to ground. The VCO then remains operational so this possibility cannot be used with A.M. reception.

3. Economic periphery

a. For a fixed stereo switching level of ⩽ 16 mV a resistor of 620 kΩ can be connected between pin 13 and positive supply (+) instead of a potentiometer in series with a resistor.
b. The 10 kΩ resistor connected in parallel with the stereo indicator lamp can be omitted, however, some TDA1005A circuits will switch to mono during lamp failure.
c. The 10 μF capacitor in series with a 1 kΩ resistor at pin 9 can be decreased to a 1 μF capacitor, bearing in mind that the distortion will increase, especially around loop resonance.
d. A MUX-input filter is not needed, if i.f. roll-off starts at a frequency of 62 kHz.

4. Printed-circuit boards

For both the f.d.m. and t.d.m. stereo decoder circuits a printed-circuit board layout is given as an example (Figs 8 and 11). Also for an active filter, which is mainly used with a t.d.m. decoder, a printed-circuit board layout is given in Fig. 4.

5. Notch filter

If attention has to be paid for suppression of the 57 kHz signal (T.W.S. = Traffic Warning System) and the 19 kHz signal, an input filter can be used as given in Fig. 6.

* At supply voltages of 8 to 11 V, resistors of 5,6 kΩ have to be connected from ground to pins 2 and 3.

** Maximum voltage for safe operation: $V_{14\text{-}16} < 4$ V.

APPLICATION INFORMATION

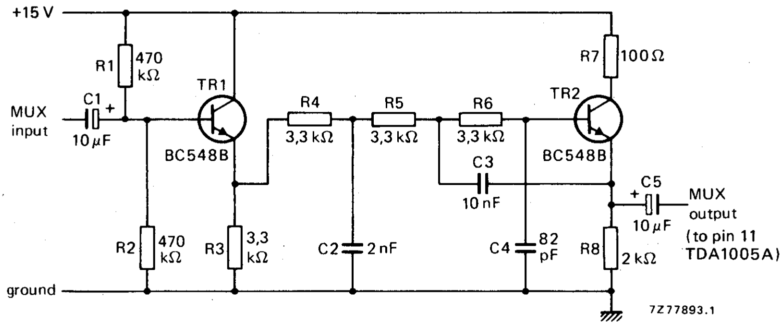


Fig. 3 Active filter circuit diagram.

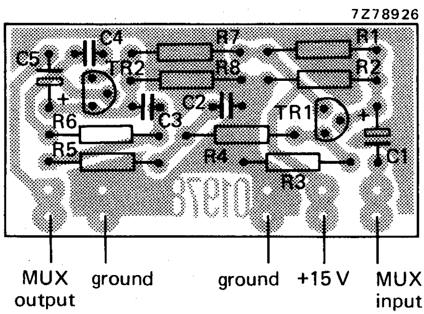


Fig. 4 Printed-circuit board component side, showing component layout.

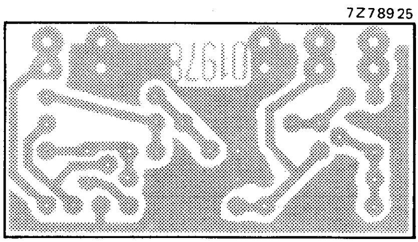
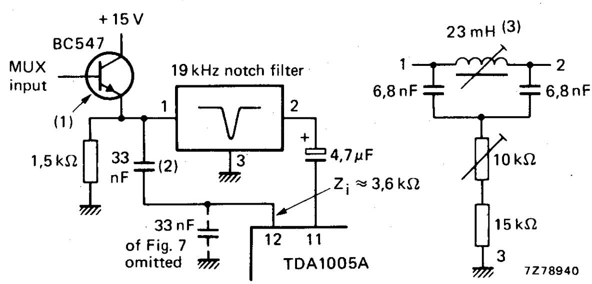
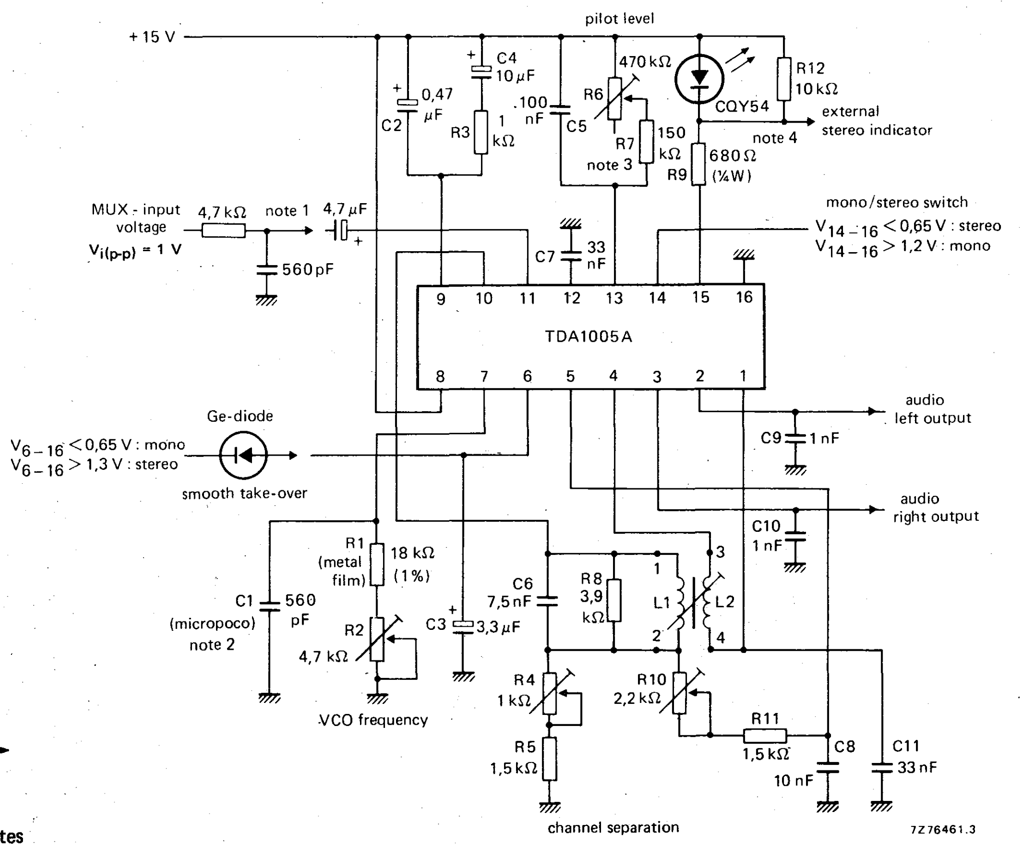


Fig. 5 Printed-circuit board showing track side.



(1) Transistor to achieve low impedance driving of notch filter.
(2) 33 nF will give common mode suppression of 19 kHz.
(3) Coil: TOKO 10 PA, 700 turns, ϕ0,07 mm Cu; case type: P06-0114; drumcore: AN01-0021; base 5 pins type: 07-0084-02; core type CAN02-0029.

Fig. 6 Example of using a 19 kHz tuned notch filter; for other input structures see Figs 13 to 21.



Coil data:

L_1L_2 = 2,6 mH

$Q_{1\text{-}2}$ = 35; Q_{min} = 30

$N_{1\text{-}2}$ = 357½ turns;

$N_{3\text{-}4}$ = 297½ turns:

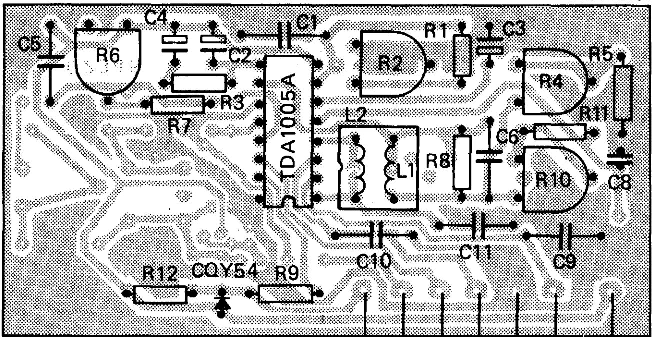
scrambled wound with wire diameter 0,09 mm,

$$\frac{E_{3\text{-}4}}{E_{1\text{-}2}} \times 100\% = 82\%$$

Notes

1. For other input structures see Figs 13 to 21; shown here is with RC-filter (Fig. 15).
2. The micropoco capacitor has a temperature coefficient of $125.10^{-6} \pm 60.10^{-6}$ K^{-1}.
3. In simplified circuits a fixed resistor (e.g. 620 kΩ) can be used for a guaranteed switching level of ⩽ 16 mV.
4. Either the LED circuit or an external stereo indicator can be used.

Fig. 7 Basic application circuit of a frequency-division multiplex (f.d.m.) stereo decoder.



1. Positive supply (+ 15 V).
2. Left output.
3. Ground.
4. Right output.
5. Mono/stereo switch.
6. MUX input.
7. External stereo indicator.

Fig. 8 Printed-circuit board component side of an f.d.m. decoder, showing component layout. For circuit diagram see Fig. 7.

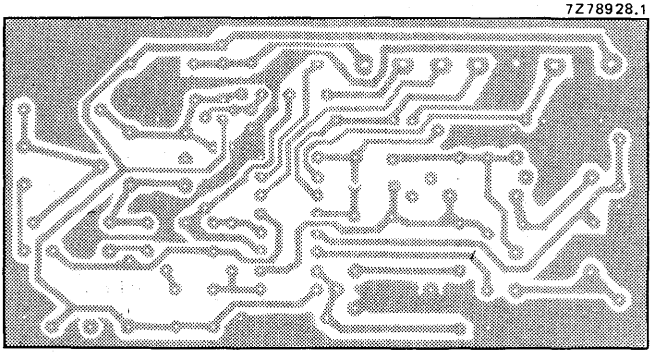
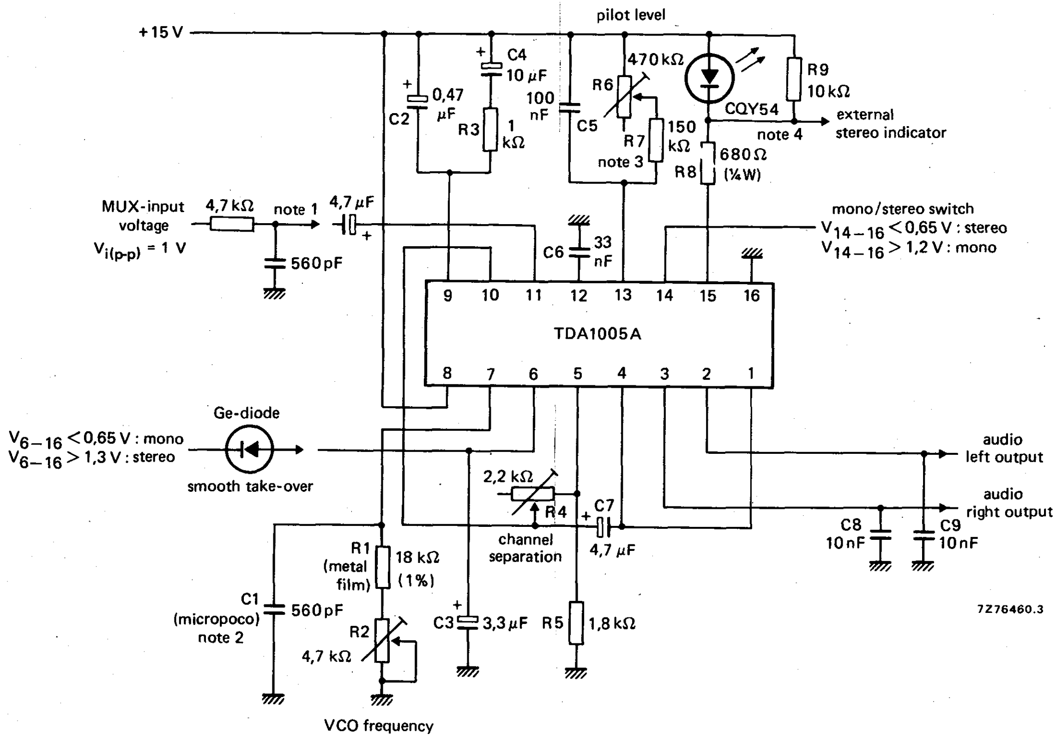


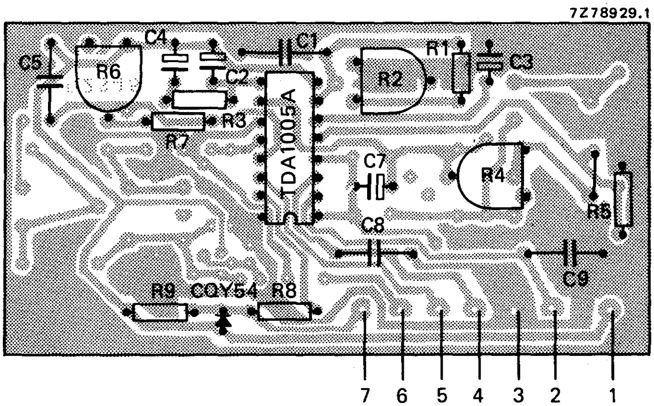
Fig. 9 Printed-circuit board showing track side.



Notes

1. For other input structures see Figs 13 to 21; shown here is with RC-filter (Fig. 15).
2. The micropoco capacitor has a temperature coefficient of $125.10^{-6} \pm 60.10^{-6}$ $^{o}C^{-1}$.
3. In simplified circuits a fixed resistor (e.g. 620 kΩ) can be used for a guaranteed switching level of ⩽ 16 mV.
4. Either the LED circuit or an external stereo indicator can be used.

Fig. 10 Basic application circuit of a time-division multiplex (t.d.m.) stereo decoder.



1. Positive supply (+ 15 V).
2. Left output.
3. Ground.
4. Right output.
5. Mono/stereo switch.
6. MUX input.
7. External stereo indicator.

Fig. 11 Printed-circuit board component side of a t.d.m. decoder, showing component layout. For circuit diagram see Fig. 10.

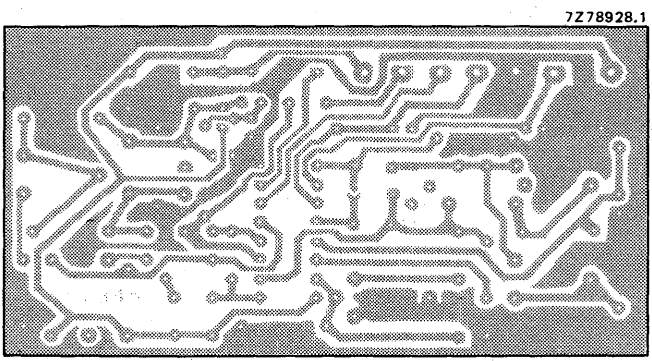


Fig. 12 Printed-circuit board showing track side.

INPUT STRUCTURES (see also Figs 7 and 10)

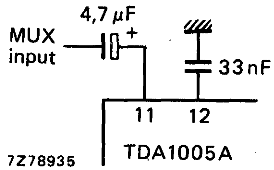


Fig. 13 Without filtering.

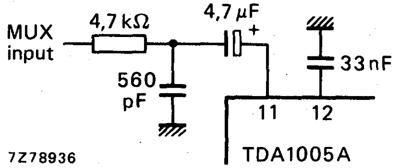


Fig. 15 With RC-filter for achieving i.f. roll-off (typ. 62 kHz).

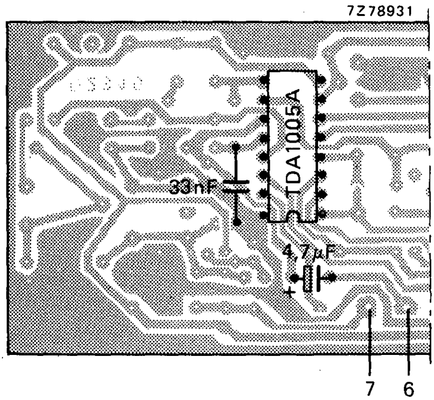


Fig. 14 Printed-circuit board component side, showing component layout of Fig. 13.

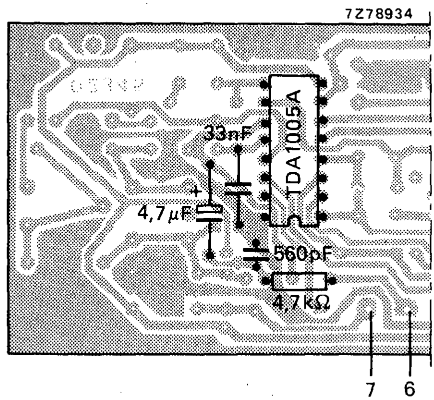


Fig. 16 Printed-circuit board component side, showing component layout of Fig. 15.

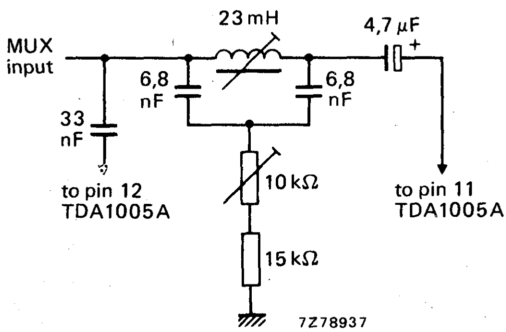


Fig. 17 With 19 kHz notch filter.

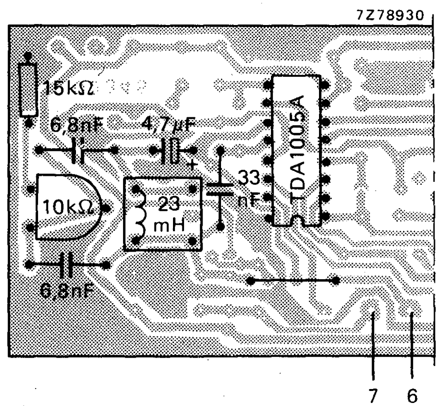


Fig. 18 Printed-circuit board component side, showing component layout of Fig. 17.

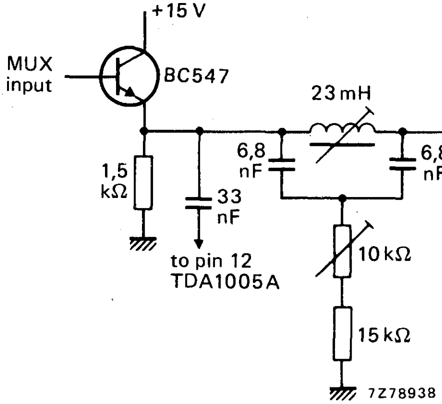


Fig. 19 With buffer stage (to achieve low impedance driving of notch filter; see Fig. 6) and 19 kHz notch filter.

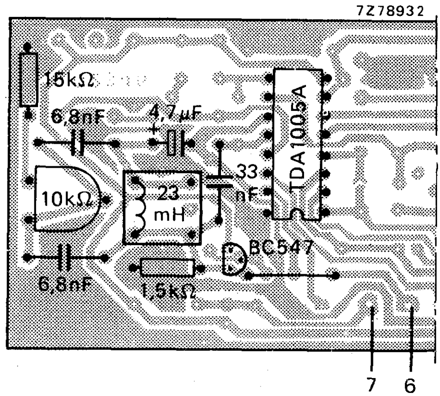


Fig. 20 Printed-circuit board component side, showing component layout of Fig. 19.

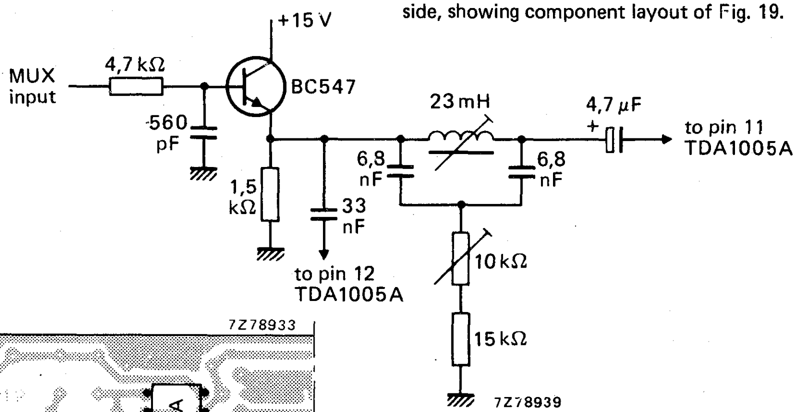


Fig. 21 With RC-filter, buffer stage and 19 kHz notch filter.

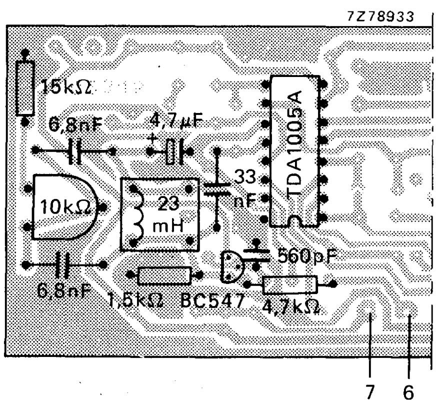
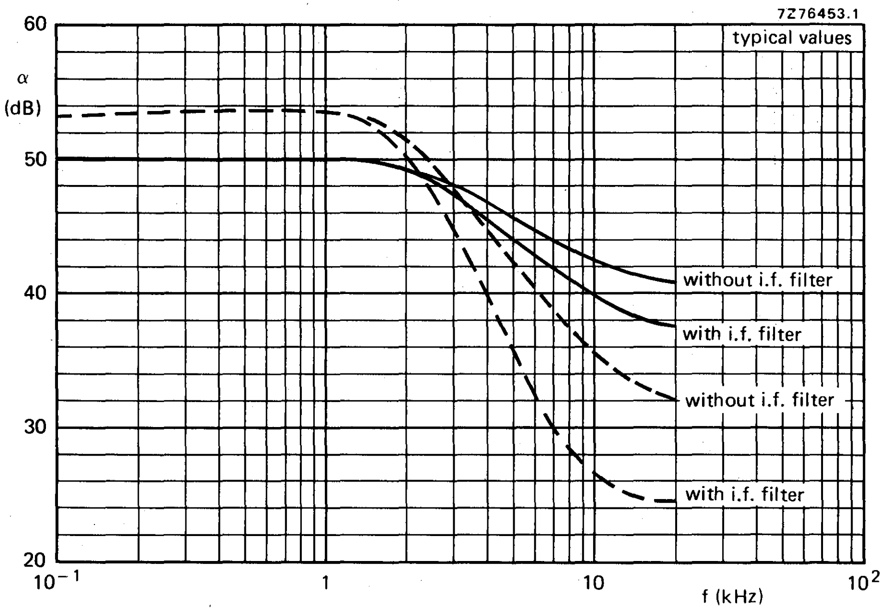
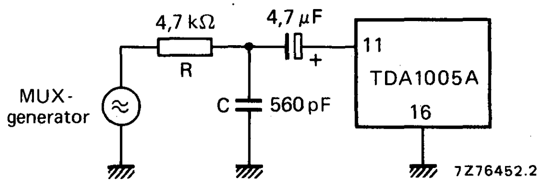


Fig. 22 Printed-circuit board component side, showing component layout of Fig. 21.





—— time-division multiplex system; adjusted at 1 kHz (R4 in Fig. 10)
– – – frequency-division multiplex system; adjusted at 1 and 5 kHz (R4 and R10 in Fig. 7)

Conditions: $V_{8\text{-}16} = 15$ V; $V_{i(p\text{-}p)} = 1$ V.

Note: RC-filter for simulating the i.f. roll-off (typ. 62 kHz).

Fig. 23 Channel separation as a function of frequency.

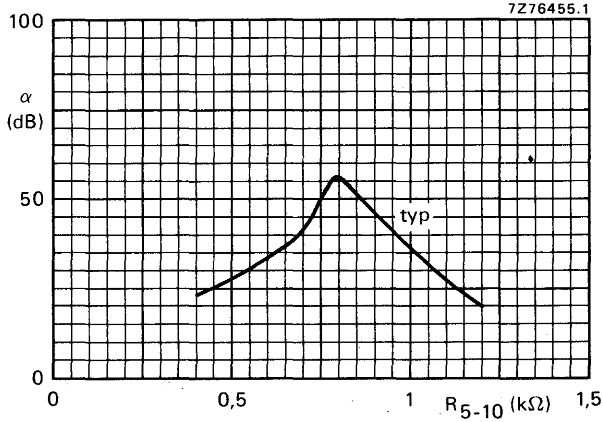


Fig. 24 Channel separation at f = 1 kHz as a function of resistance between pins 5 and 10 for a t.d.m. system. For test circuit see Fig. 23.

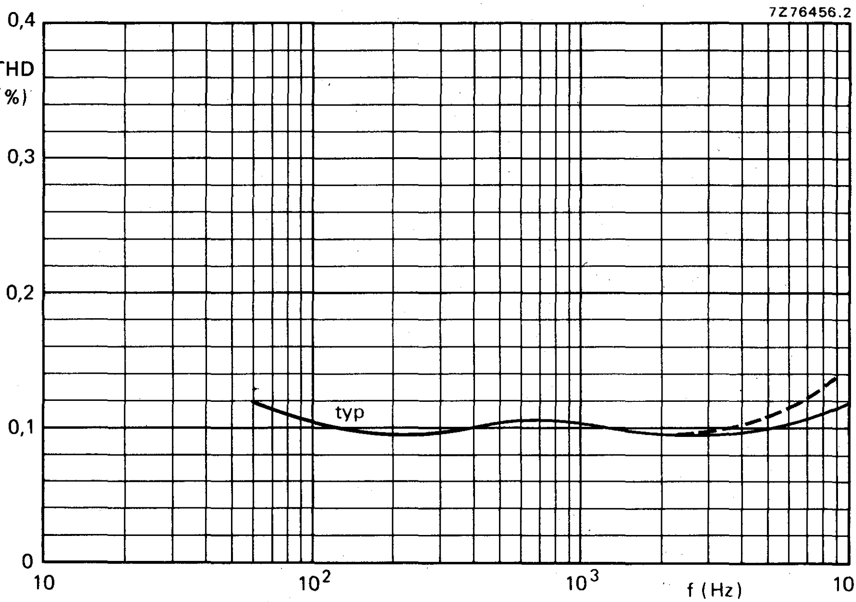
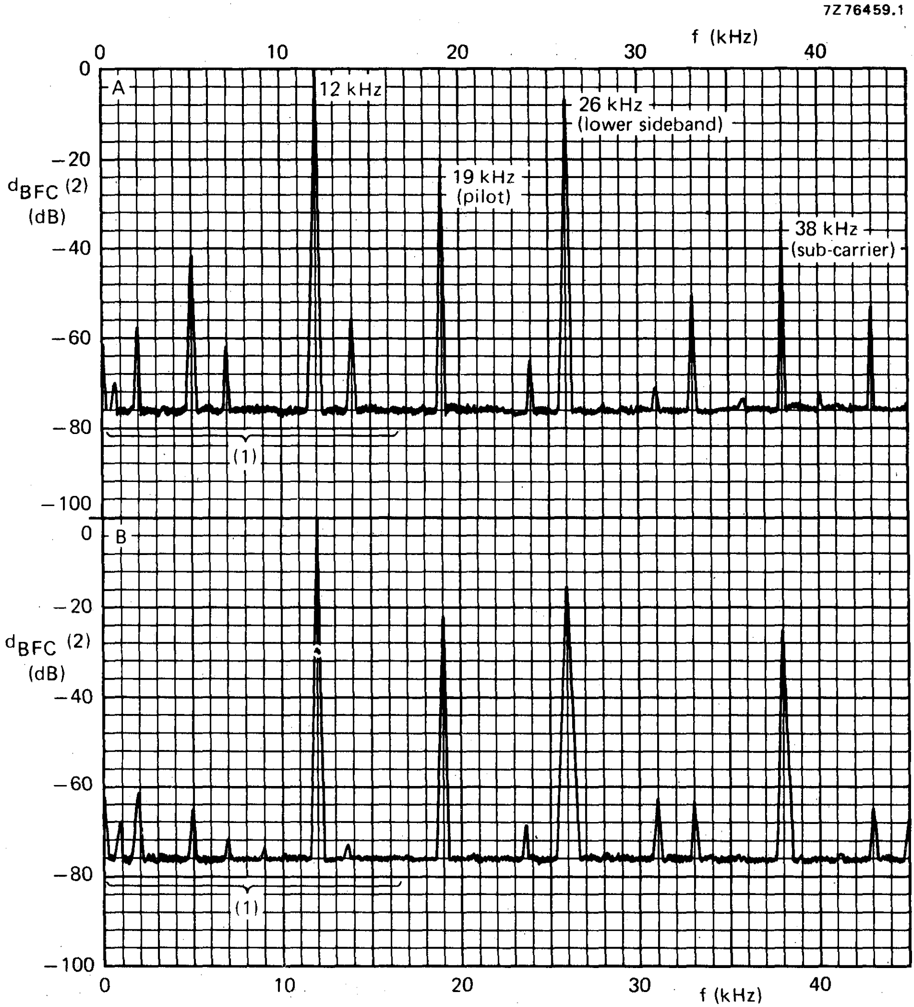


Fig. 25 Distortion as a function of audio frequency; R = 1; L = 0; $V_{8\text{-}16}$ = 15 V; $V_{2\text{-}16}$ = $V_{3\text{-}16}$ = 1 V (r.m.s.). – – – t.d.m. system; ——— f.d.m. system.



(1) Audible interferences (BFC-distortion) and desired 12 kHz signal.

(2) $d_{BFC} = 20 \log \frac{V_{BFC}}{V \text{ (at 12 kHz)}}$.

Fig. 26 Spectrum at the decoder outputs; A for t.d.m.; B for f.d.m. $V_{i(p\text{-}p)} = 1$ V; R = 1; L = 0; m = 90% for f = 12 kHz; m = 10% for f = 19 kHz.

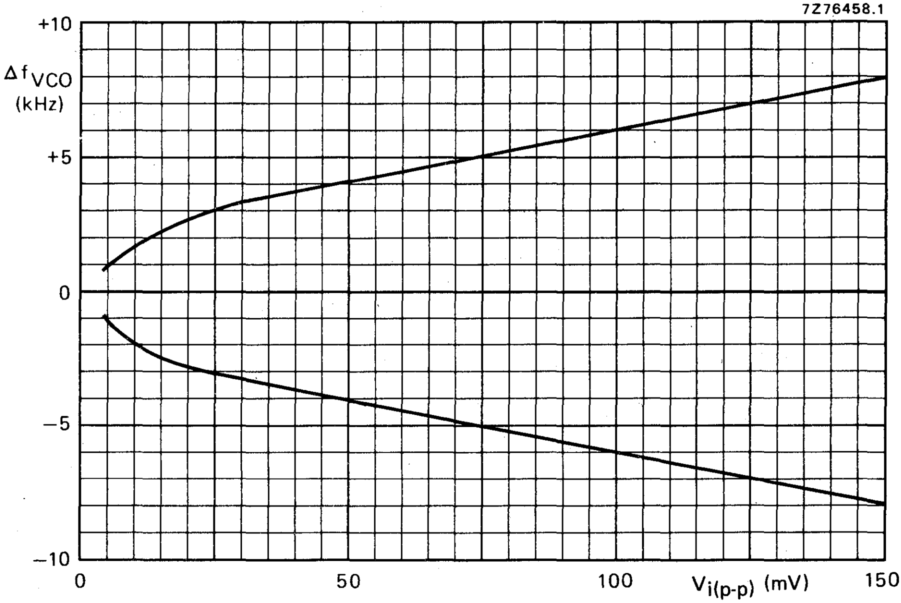


Fig. 27 Typical values of the capture range of the oscillator as a function of the pilot threshold voltage at MUX-input.
$V_{8\text{-}16}$ = 15 V; $\Delta f_{VCO} = f_{VCO} - 76$ kHz where: f_{VCO} = modulated, free-running oscillator frequency; Δf_{VCO} = maximum f_{VCO} deviation which will be captured if pilot signal (pin 11) is switched-on.

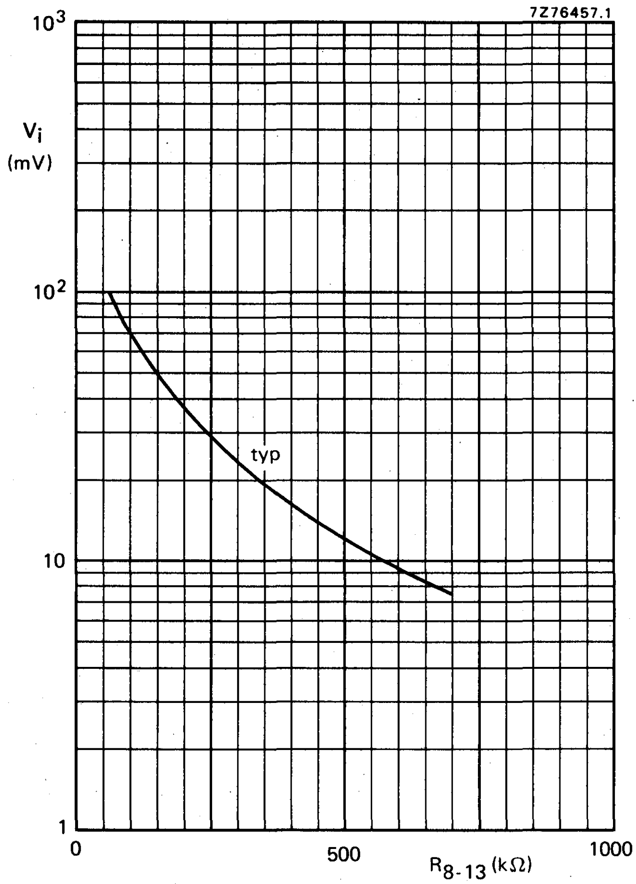


Fig. 28 Pilot input voltage switching level (stereo 'on') as a function of resistance between pins 8 and 13.

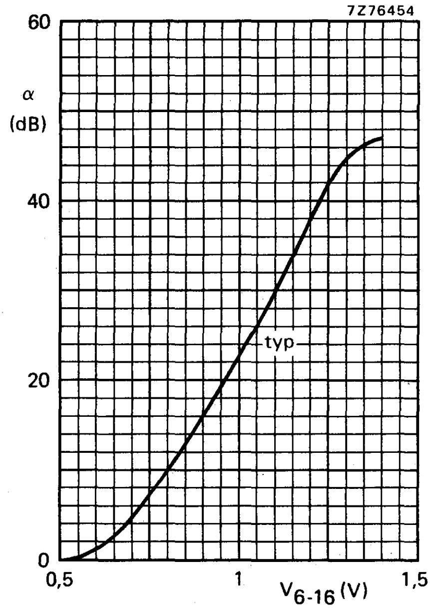


Fig. 29 Channel separation as a function of $V_{6\text{-}16}$ at 1 kHz (smooth take-over).

MOTOR REGULATOR WITH AUTOMATIC TAPE-END INDICATOR

The TDA1006A is for use in car radio tape-decks

The circuit incorporates the following functions:
- capstan motor speed control;
- an electronic motor stop in conjunction with hysteresis slip-coupling or commutator pulses;
- an automatic switch from playback to radio at tape-end;
- playback indication with lamp;
- tape-end indication with intermittent light.

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 22 V
Ambient temperature	T_{amb}	typ.	25 °C
Supply voltage	V_P	typ.	14 V
Motor regulator			
Current consumption ($R_{3\text{-}4}$ = 7,5 kΩ)			
radio	I_4	typ.	9 mA
playback (I_1 = 0)	I_4	typ.	12 mA
playback	I_4	typ.	52 mA
tape-end	I_4	typ.	32 mA
Operating motor current	I_3	typ.	200 mA
Supply voltage rejection	$\Delta V_{3\text{-}2}/\Delta V_{4\text{-}2}$	typ.	1 mV/V
Automatic stop circuit			
Input current	I_{14}	>	25 μA
Input voltage at commutator	$V_{11\text{-}2}$		−6 to +6 V

PACKAGE OUTLINE

16-lead DIL; plastic power (SOT-38N2).

Fig. 1a Circuit diagram (continued in Fig. 1b).

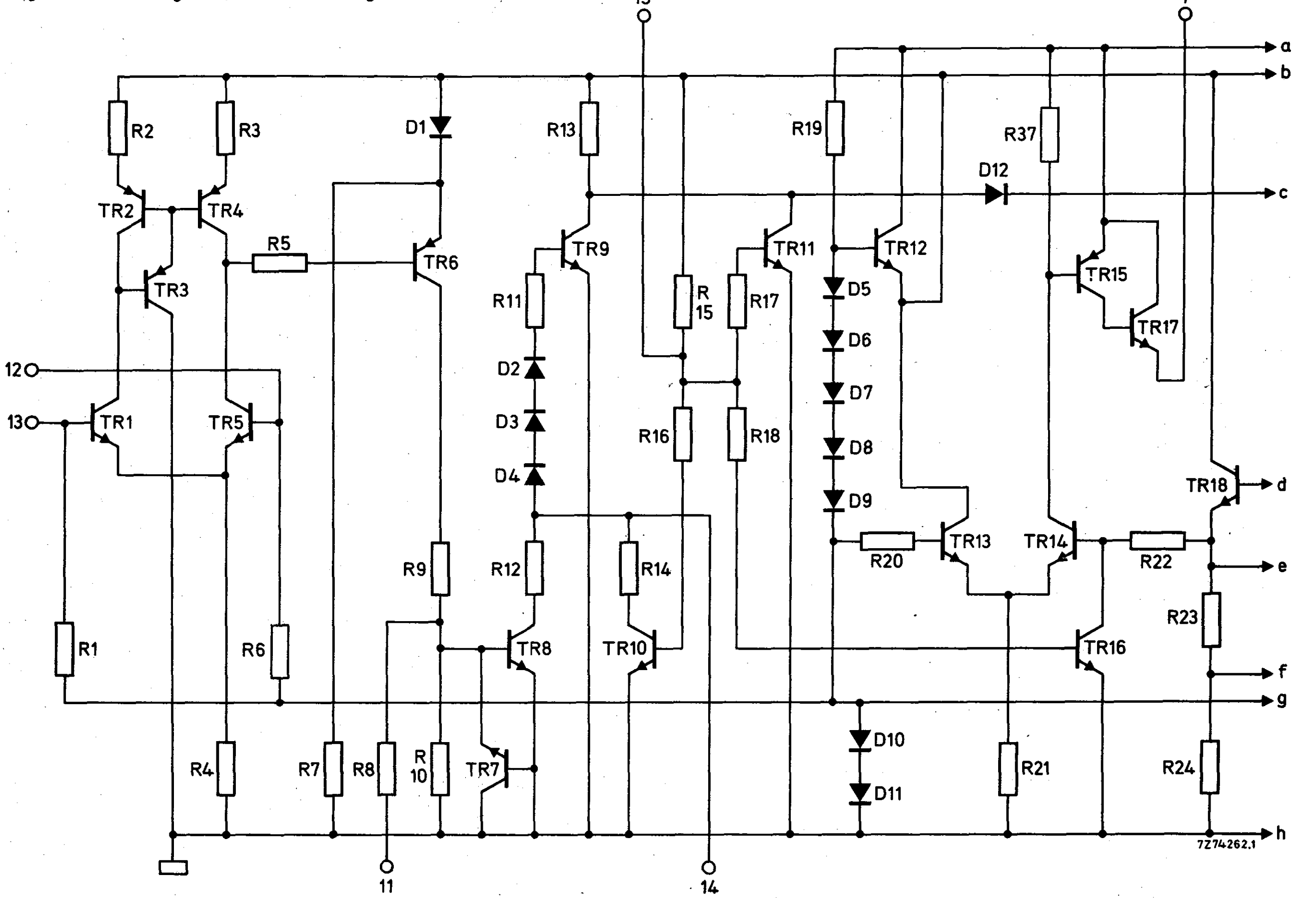
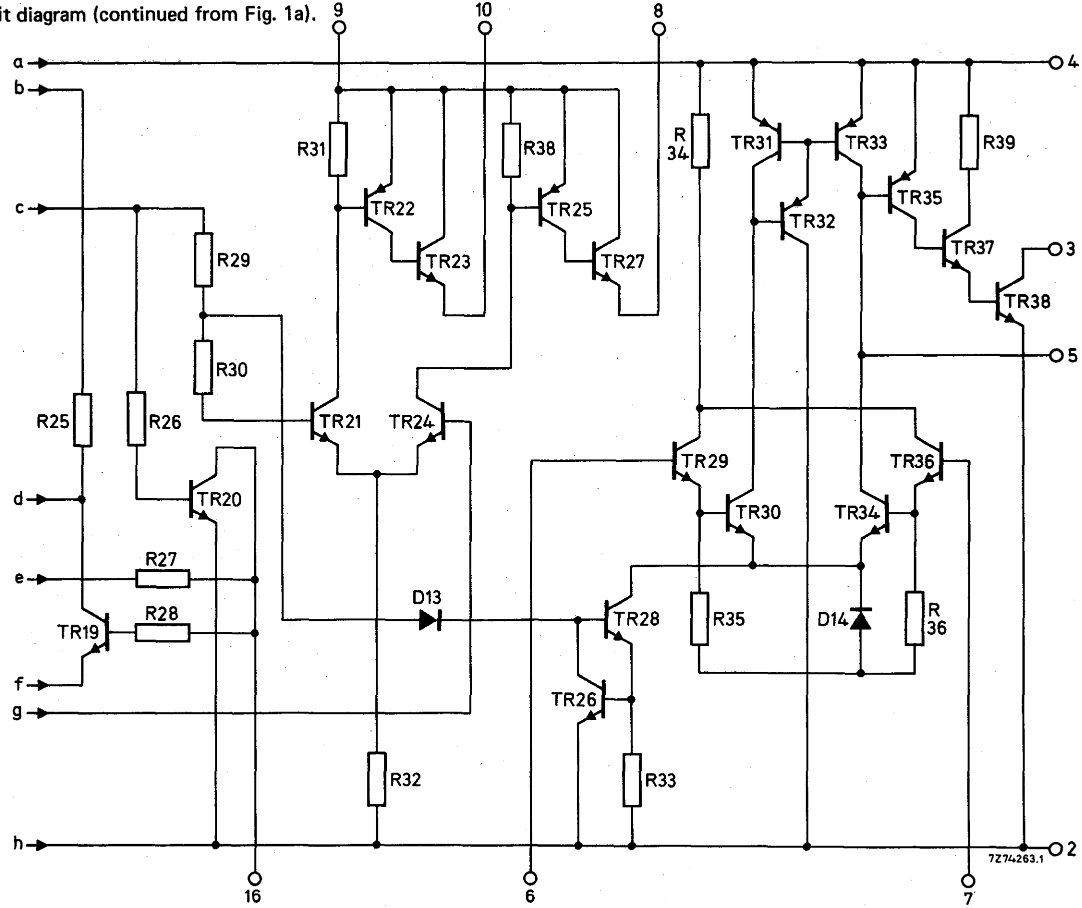


Fig. 1b Circuit diagram (continued from Fig. 1a).



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage			
pin 4	$V_{4\text{-}2}$	max.	24 V
pin 9	$V_{9\text{-}2}$	max.	24 V
	$V_{4\text{-}2}$	$\geqslant$	$V_{9\text{-}2}$
Output current			
pin 1 (d.c. value)	$-I_1$	max.	40 mA
(peak value)	$-I_{1M}$	max.	100 mA
pin 3 (d.c. value)	I_3	max.	250 mA
(non-repetitive peak value)	I_{3SM}	max.	600 mA
pin 8 (d.c. value)	$-I_8$	max.	45 mA
(peak value)	$-I_{8M}$	max.	80 mA
pin 10 (d.c. value)	$-I_{10}$	max.	20 mA
(peak value)	$-I_{10M}$	max.	20 mA
Storage temperature	T_{stg}	−65 to +150 °C	
Operating ambient temperature see power derating curve Fig. 2	T_{amb}	−25 to +150 °C	

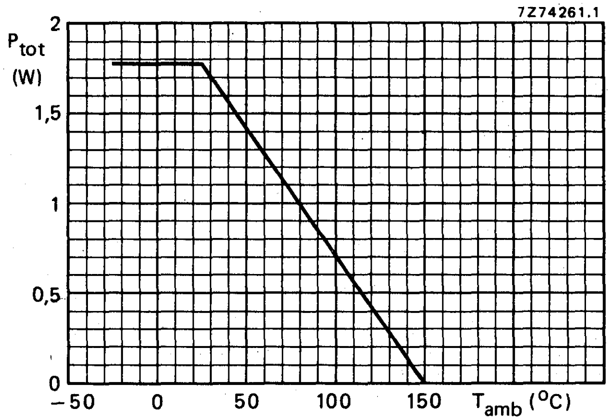


Fig. 2 Power derating curve; derating factor: 14,3 mW/°C.

CHARACTERISTICS

V_P = 14 V; T_{amb} = 25 °C unless otherwise specified (see test circuit Fig. 3).

Supply voltage range (pins 4 and 9)	V_P		6 to 22	V
	$V_{4\text{-}2}$	$\geqslant$	$V_{9\text{-}2}$	
Motor regulator				
Current consumption ($R_{3\text{-}4}$ = 7,5 kΩ)				
radio	I_4	typ.	9	mA
playback (I_1 = 0)	I_4	typ.	12	mA
			9,5 to 17	mA
playback	I_4	typ.	52	mA
tape-end	I_4	typ.	32	mA
Input offset voltage at I_3 = 3 mA	$\|V_{7\text{-}6}\|$	typ.	2	mV
		<	8	mV
Input voltage range (common mode)	$V_{6\text{-}2}$; $V_{7\text{-}2}$		2,4 to V_P–0,2	V
Input bias current	I_6; I_7	typ.	80	nA
		<	700	nA
Input sensitivity (for ΔI_3 = 100 mA)	$\Delta V_{7\text{-}6}$	<	13	mV
Operating voltage of TR38 at I_{3SM} = 600 mA	$V_{3\text{-}2}$	typ.	900	mV
		<	1800	mV
Supply voltage rejection	$\Delta V_{3\text{-}2}/\Delta V_{4\text{-}2}$	typ.	1	mV/V
Operating motor current	I_3	typ.	200	mA
		<	250	mA
Automatic motor 'stop' circuit				
Input current	I_{14}	>	25	μA
Voltage when TR20 is not conducting (pin 16; peak-to-peak value)	$V_{16\text{-}2(p\text{-}p)}$		0,9 to 1,4	V
Voltage when TR20 is conducting (pin 16)	$V_{16\text{-}2}$	<	250	mV
Input voltage at commutator (pin 11)	$V_{11\text{-}2}$		–6 to +6	V
Stop signal amplifier				
Differential input voltage	$V_{12\text{-}13}$	typ.	3,5	mV
			2,6 to 4,4	mV
Voltage without input signal	$V_{11\text{-}2}$		85 to 170	mV
Input voltage (r.m.s. value)	$V_{12\text{-}13(rms)}$	>	10	mV

CHARACTERISTICS (continued)

Radio and preamplifier supply

Radio supply current (d.c.)	$-I_8$	$\leqslant$	45	mA
Saturation voltage at $-I_{8M}$ = 80 mA	$V_{8\text{-}9}$	$\leqslant$	1,35	V
Preamplifier supply current (d.c.)	$-I_{10}$	$\leqslant$	20	mA
Saturation voltage at $-I_{10}$ = 20 mA	$V_{10\text{-}9}$	$\leqslant$	1,2	V

Lamp driver

Output current (d.c.)	$-I_1$	$\leqslant$	40	mA
Saturation voltage at $-I_{1M}$ = 100 mA	$V_{4\text{-}1}$	$\leqslant$	1,85	V
D.C. voltage level	$V_{15\text{-}2}$	0,75 to	1,2	V

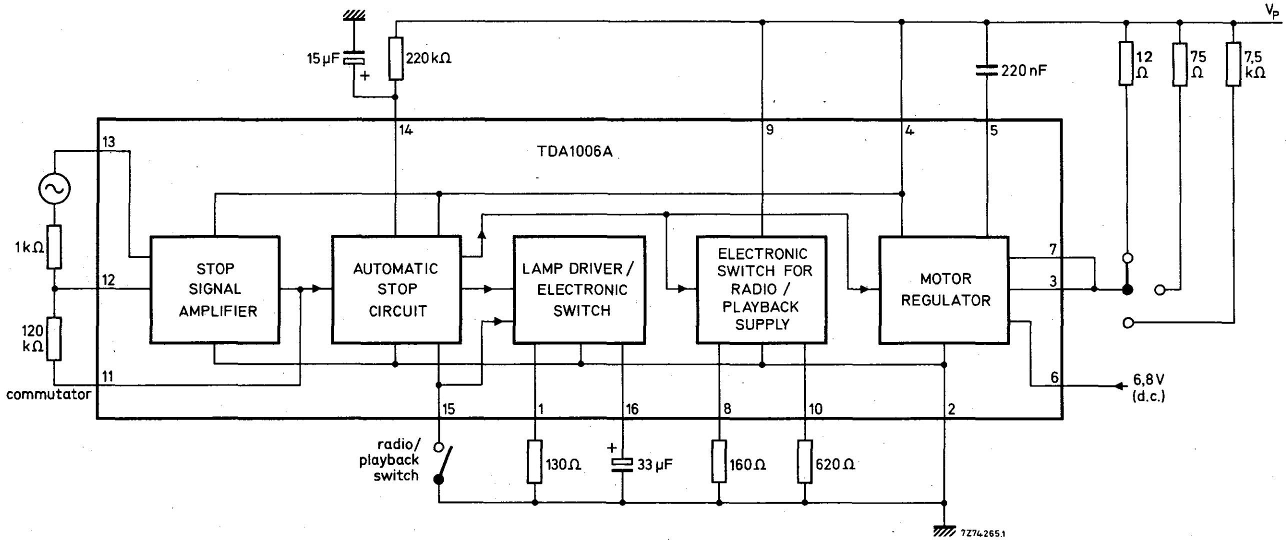
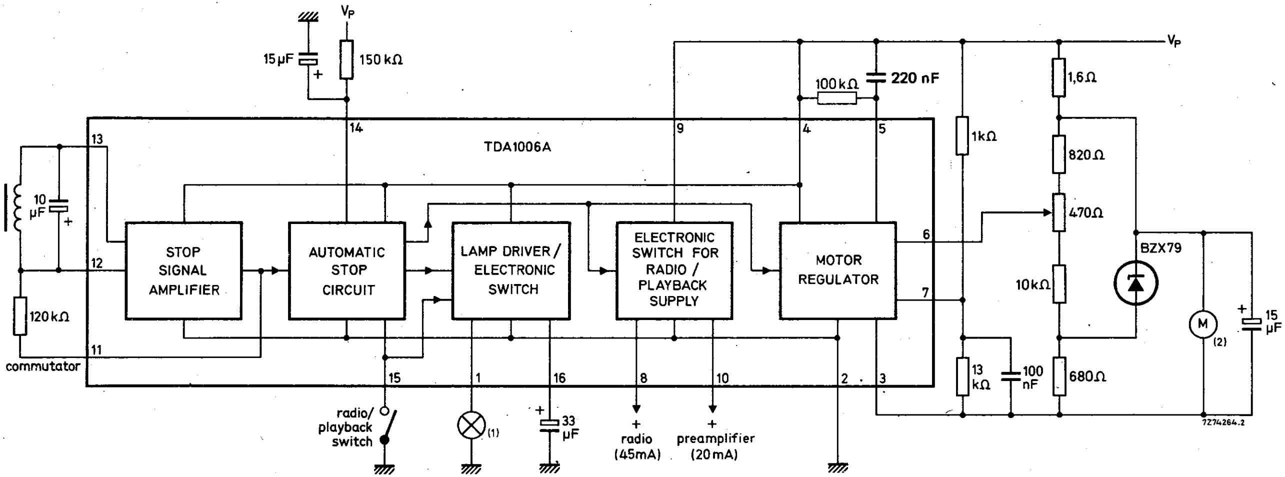


Fig. 3 Test circuit.

APPLICATION INFORMATION



(1)	Radio:	lamp off	(2)	D.C. motor
	Playback:	lamp on		E_{3000} = 7,2 to 8,3 V
	Tape-end:	intermittent light		R_m = 27 Ω

Fig. 4 Application circuit diagram.

GATING/FREQUENCY DIVIDER FOR ELECTRONIC MUSICAL INSTRUMENTS

The TDA1008 is a monolithic bipolar integrated circuit based on I^2L (integrated injection logic), with frequency dividers directly coupled to the gating system.

The outputs of the dividers, together with the input signal, are applied internally to nine gate inputs. By activating a key input, five successive signals out of the nine are selected and transferred to the outputs. Five key inputs are available, each selecting a different combination; e.g. 16', 8', 4', 2' and 1'. The output signal level is proportional to the voltage applied to the key inputs. By connecting RC combinations to the key inputs, sustain of the output signal is easily obtained. The duration of the sustained signal can be adjusted by connecting a variable voltage to the appropriate terminal (pin 7).

In electronic organs using a top octave synthesizer directly coupled to twelve TDA1008 circuits, only one busbar per manual is needed to obtain five octave-related tones per key.

The tone output signals are symmetrical around a fixed d.c. voltage, thereby avoiding key clicks.

QUICK REFERENCE DATA

Supply voltage (pin 1)	$V_{P1\text{-}16}$	typ.	12	V
Supply voltage divider (pin 13)	$V_{P13\text{-}16}$	typ.	6	V
Supply voltage tone outputs (pins 2, 3, 4, 5, 6)	V_{Ptone}	typ.	9	V
Input voltage; HIGH	V_{IH}	>	1,5	V
Input voltage; LOW	V_{IL}	<	0,4	V
Required key voltage (pins 8, 9, 10, 11, 12)	V_{K1} to V_{K5}	typ.	$V_{P13\text{-}16}$	
Key input impedance (see note)	Z_{K1} to Z_{K5}	>	8	MΩ
Supply current (pin 1)				
all keys activated	I_1	typ.	13	mA
no activated keys	I_1	typ.	0	mA
Supply current (pin 13)	I_{13}	typ.	11	mA
Sustaining voltage range (pin 7)	V_{7sust}		0 to 2	V
Input frequency	f_i	<	100	kHz
Tone output signal voltage with one key activated	$V_{Q(p\text{-}p)}$	typ.	600	mV
Operating ambient temperature range	T_{amb}		0 to + 70	°C

Note

Key input impedance is determined by the voltage applied to pin 7. This impedance is stated at zero volt on pin 7.

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

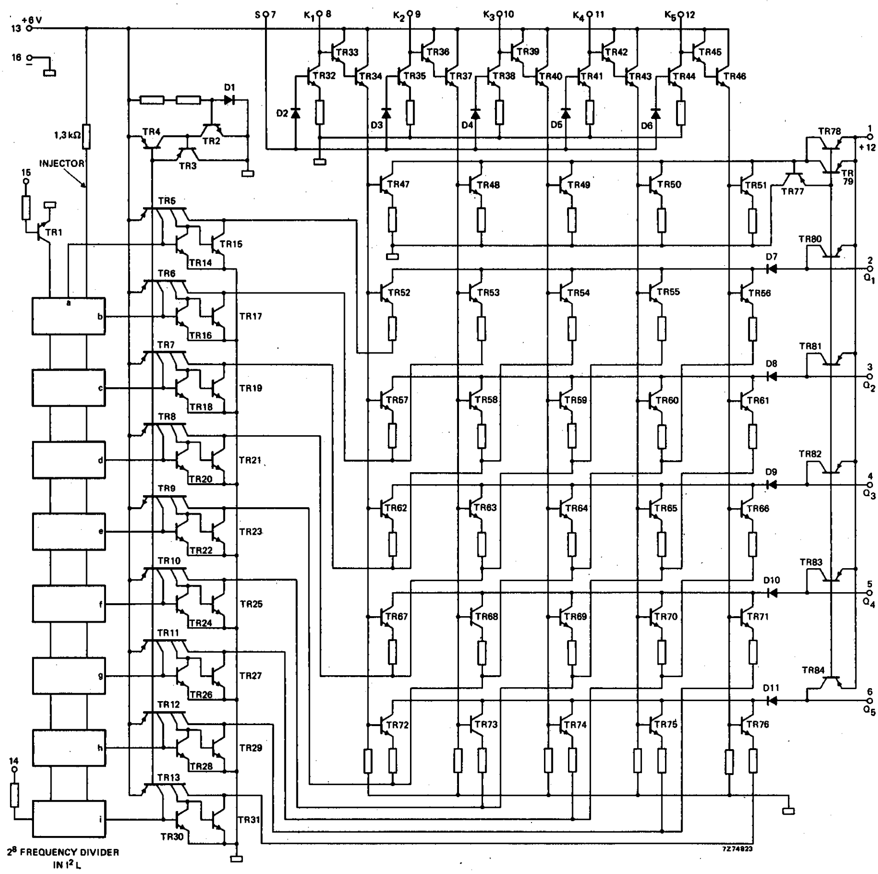


Fig. 1 Circuit diagram.

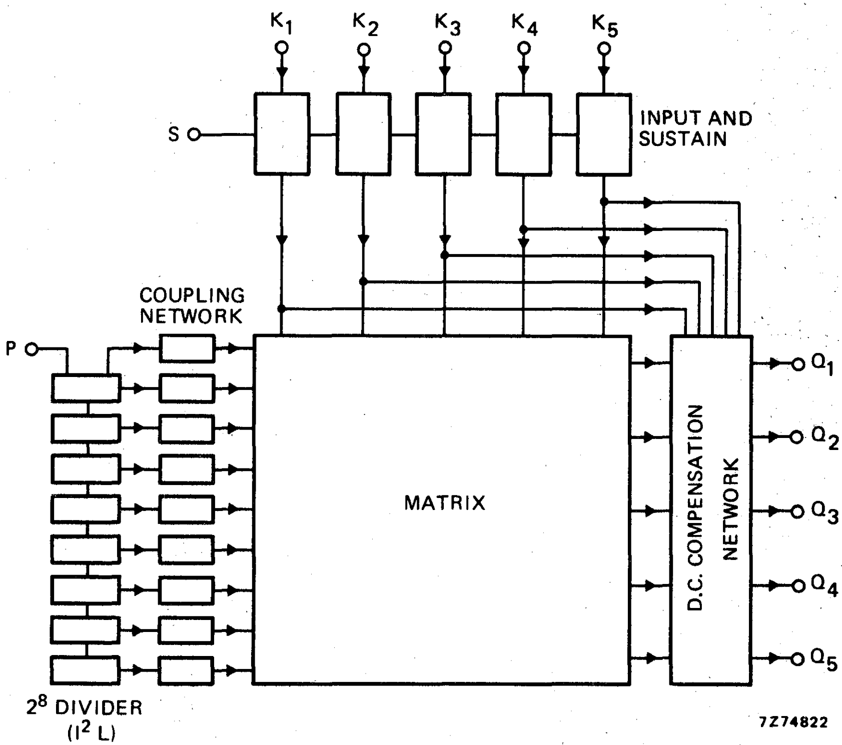


Fig. 2 Block diagram.

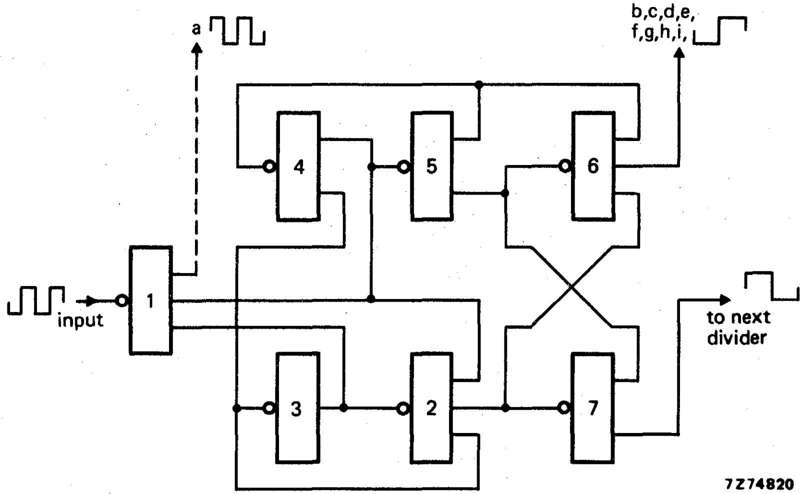


Fig. 3 Logic diagram of the I^2L 2-divider.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages			
pin 1	$V_{P1\text{-}16}$	max.	13 V
pin 13	$V_{P13\text{-}16}$	max.	6,5 V
pin 14	$V_{P14\text{-}16}$	max.	6,5 V
Input voltages			
K inputs (pins 8, 9, 10, 11, 12)	V_{K1} to V_{K5}	max.	$V_{P13\text{-}16}$
f_i input (pin 15)	V_{fi}	max.	15 V
S input (pin 7)	V_S	max.	2,5 V
Output voltages			
Q_1 to Q_5 (pins 2, 3, 4, 5, 6)	V_{Q1} to V_{Q5}	max.	12 V
Operating ambient temperature	see derating curve Fig. 4		
Storage temperature	T_{stg}		−25 to + 125 °C
Total power dissipation	see derating curve Fig. 4		

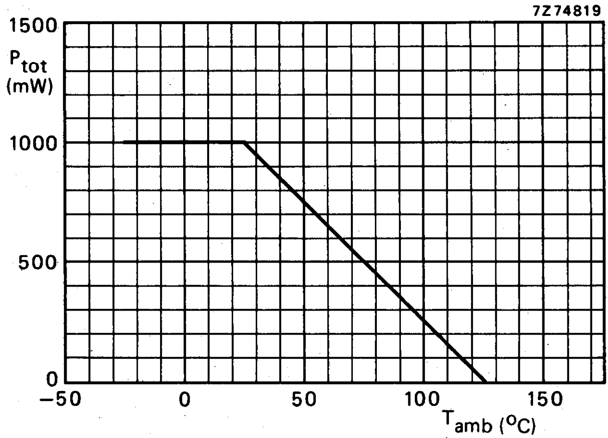


Fig. 4 Power derating curve.

CHARACTERISTICS

All voltages with reference to pin 16; all currents positive into the IC.

Supply voltage range			
pin 13	$V_{P13\text{-}16}$		5 to 6,5 V
pin 1	$V_{P1\text{-}16}$		10 to 13 V
pin 9	$V_{P9\text{-}16}$	see note 1	

Characteristics at T_{amb} = 25 °C; $V_{P13\text{-}16}$ = 6 V; $V_{P1\text{-}16}$ = 12 V; see Fig. 6.

Supply current (pin 13)			
K-inputs at 6 V	I_{13}		7,5 to 16 mA
		typ.	11 mA
Supply current (pin 1)			
K-inputs at 6 V	I_1		8 to 16 mA
		typ.	12,7 mA
Input current at f_i (pin 15)			
V_{fi} = 6 V	I_{15}		100 to 200 µA
		typ.	150 µA
Input current K-inputs (pins 8, 9, 10, 11, 12)			
V_K = 6 V			
S-input connected to 0 V	I_K	typ.	150 nA
		<	750 nA
S-input connected to 2,0 V	I_K		80 to 150 µA
		typ.	100 µA
Input current S-input (pin 7)			
no key inputs activated	I_S	typ.	500 µA
all key inputs activated	I_S	typ.	10 µA
Output current Q-output (pins 2, 3, 4, 5, 6)			
V_Q = LOW (note 2)	$+I_Q$		230 to 450 µA
		typ.	300 µA
V_Q = HIGH (note 2)	$-I_Q$		230 to 450 µA
		typ.	300 µA
Output current pin 14	I_{14}	<	20 µA
Peak output voltage (pins 2, 3, 4, 5, 6)			
by activating one K-input only (Fig. 5)	V_{QM}	typ.	300 mV
Input frequency at pin 15			
$V_{15HIGH} > 1{,}5$ V; $V_{15LOW} < 0{,}4$ V	f_i	<	100 kHz

Notes

1. This voltage has to be in the middle of $V_{P1\text{-}16}$ and $V_{13\text{-}16}$.
2. To be multiplied by the number of activated K-inputs.

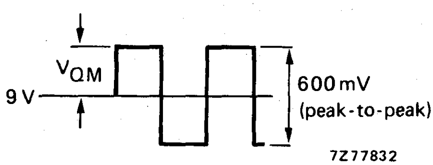


Fig. 5

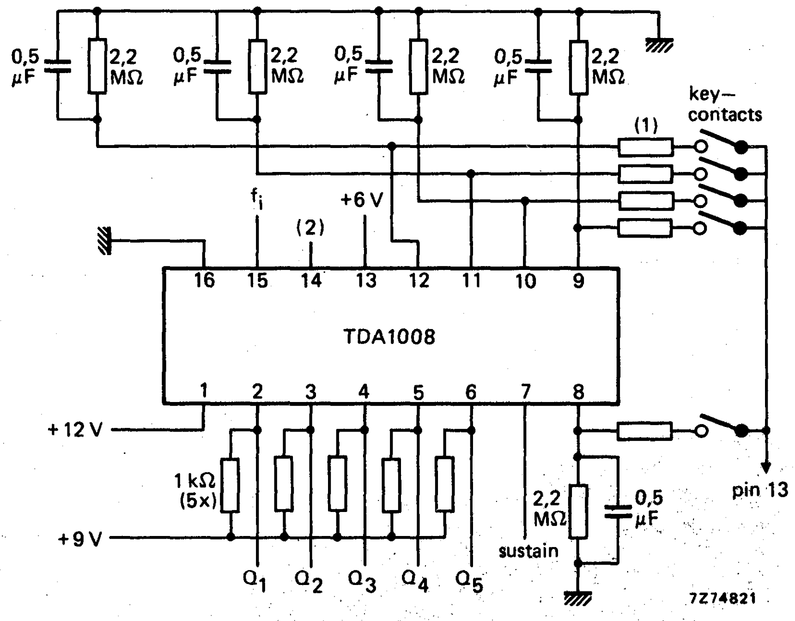
TRUTH TABLE

	K_1	K_2	K_3	K_4	K_5
Q_1	f_i	$f_i/2$	$f_i/4$	$f_i/8$	$f_i/16$
Q_2	$f_i/2$	$f_i/4$	$f_i/8$	$f_i/16$	$f_i/32$
Q_3	$f_i/4$	$f_i/8$	$f_i/16$	$f_i/32$	$f_i/64$
Q_4	$f_i/8$	$f_i/16$	$f_i/32$	$f_i/64$	$f_i/128$
Q_5	$f_i/16$	$f_i/32$	$f_i/64$	$f_i/128$	$f_i/256$

Activating 'one' key input only gives the notified output frequency.

By activating more key inputs at a time, the output amplitude will be the sum signal of the notified frequencies.

APPLICATION INFORMATION



(1) If required contact-current limiting resistors.
(2) a. Factory test point; ungated output from the final divider.
b. Can be used for obtaining very low frequencies (pedals). It should be connected to pin 13 (+ 6 V) via a resistor of minimum 300 kΩ to deliver the current I_{14}.

Fig. 6 Basic application diagram.

6 W AUDIO POWER AMPLIFIER

The TDA1010 is a monolithic integrated class-B audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is primarily developed as a 6 W car radio amplifier for use with 4 Ω and 2 Ω load impedances. The wide supply voltage range and the flexibility of the IC make it an attractive proposition for record players and tape recorders with output powers up to 8 W.

Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- low-cost external components
- good ripple rejection
- thermal protection

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 24	V
Repetitive peak output current	I_{ORM}	max.	3	A
Output power at pin 2; d_{tot} = 10%				
V_P = 14,4 V; R_L = 2 Ω	P_o	typ.	6,4	W
V_P = 14,4 V; R_L = 4 Ω	P_o	typ.	6,2	W
V_P = 14,4 V; R_L = 8 Ω	P_o	typ.	3,4	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	typ.	30	kΩ
power amplifier (pin 6)	$\lvert Z_i \rvert$	typ.	20	kΩ
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31	mA
Sensitivity for P_o = 5,8 W; R_L = 4 Ω	V_i	typ.	10	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110A).

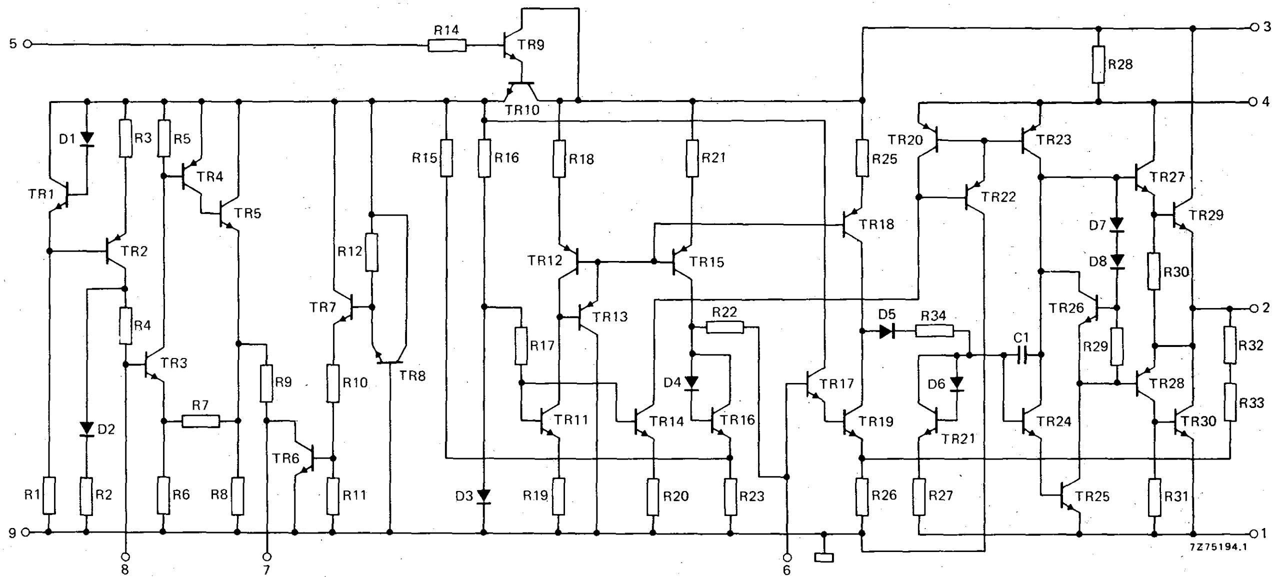


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24 V
Peak output current	I_{OM}	max.	5 A
Repetitive peak output current	I_{ORM}	max.	3 A
Total power dissipation	see derating curve Fig. 2		
Storage temperature	T_{stg}	−55 to + 150	°C
Operating ambient temperature	T_{amb}	−25 to + 150	°C
A.C. short-circuit duration of load during sine-wave drive; without heatsink at V_P = 14,4 V	t_{sc}	max.	100 hours

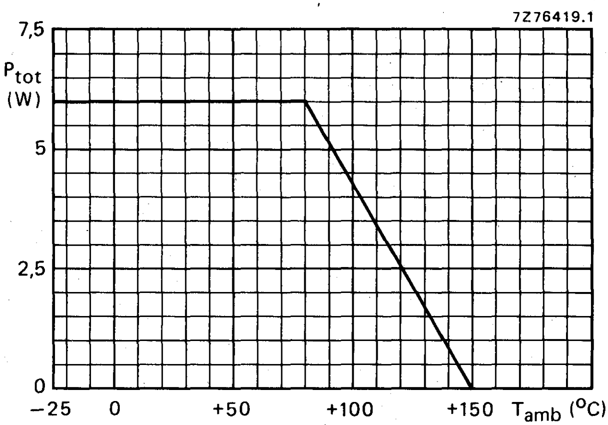


Fig. 2 Power derating curve.

HEATSINK DESIGN

Assume V_P = 14,4 V; R_L = 2 Ω; T_{amb} = 60 °C maximum; thermal shut-down starts at T_j = 150 °C. The maximum sine-wave dissipation in a 2 Ω load is about 5,2 W. The maximum dissipation for music drive will be about 75% of the worst-case sine-wave dissipation, so this will be 3,9 W. Consequently, the total resistance from junction to ambient

$$R_{th\,j\text{-}a} = R_{th\,j\text{-}tab} + R_{th\,tab\text{-}h} + R_{th\,h\text{-}a} = \frac{150 - 60}{3,9} = 23\ ^{o}C/W.$$

Since $R_{th\,j\text{-}tab}$ = 12 °C/W and $R_{th\,tab\text{-}h}$ = 1 °C/W,

$$R_{th\,h\text{-}a} = 23 - (12 + 1) = 10\ ^{o}C/W.$$

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 24	V
Repetitive peak output current	I_{ORM}	<	3	A
Total quiescent current at V_P = 14,4 V	I_{tot}	typ.	31	mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 14,4 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power (see Fig. 4) at d_{tot} = 10%; measured at pin 2; with bootstrap				
V_P = 14,4 V; R_L = 2 Ω (note 1)	P_o	typ.	6,4	W
V_P = 14,4 V; R_L = 4 Ω (note 1 and 2)	P_o	>	5,9	W
		typ.	6,2	W
V_P = 14,4 V; R_L = 8 Ω (note 1)	P_o	typ.	3,4	W
V_P = 14,4 V; R_L = 4 Ω; without bootstrap	P_o	typ.	5,7	W
V_P = 14,4 V; R_L = 2 Ω; with additional bootstrap resistor of 220 Ω between pins 3 and 4	P_o	typ.	9	W
Voltage gain				
preamplifier (note 3)	G_{v1}	typ.	24	dB
			21 to 27	dB
power amplifier	G_{v2}	typ.	30	dB
			27 to 33	dB
total amplifier	$G_{v\,tot}$	typ.	54	dB
			51 to 57	dB
Total harmonic distortion at P_o = 1 W	d_{tot}	typ.	0,2	%
Efficiency at P_o = 6 W	η	typ.	75	%
Frequency response (−3 dB)	B		80 Hz to 15	kHz
Input impedance				
preamplifier (note 4)	$\lvert Z_i \rvert$	typ.	30	kΩ
			20 to 40	kΩ
power amplifier (note 5)	$\lvert Z_i \rvert$	typ.	20	kΩ
			14 to 26	kΩ
Output impedance of preamplifier; pin 7 (note 5)	$\lvert Z_o \rvert$	typ.	20	kΩ
			14 to 26	kΩ
Output voltage preamplifier (r.m.s. value) d_{tot} < 1% (pin 7) (note 3)	$V_{o(rms)}$	>	0,7	V
Noise output voltage (r.m.s. value; note 6)				
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,3	mV
R_S = 8,2 kΩ	$V_{n(rms)}$	typ.	0,7	mV
		<	1,4	mV
Ripple rejection at f = 1 kHz to 10 kHz (note 7)	RR	>	42	dB
at f = 100 Hz; C2 = 1 μF	RR	>	37	dB
Sensitivity for P_o = 5,8 W	V_i	typ.	10	mV
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	30	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Up to $P_o \leqslant 3$ W : $d_{tot} \leqslant 1\%$.
3. Measured with a load impedance of 20 kΩ.
4. Independent of load impedance of preamplifier.
5. Output impedance of preamplifier ($|Z_o|$) is correlated (within 10%) with the input impedance ($|Z_i|$) of the power amplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).

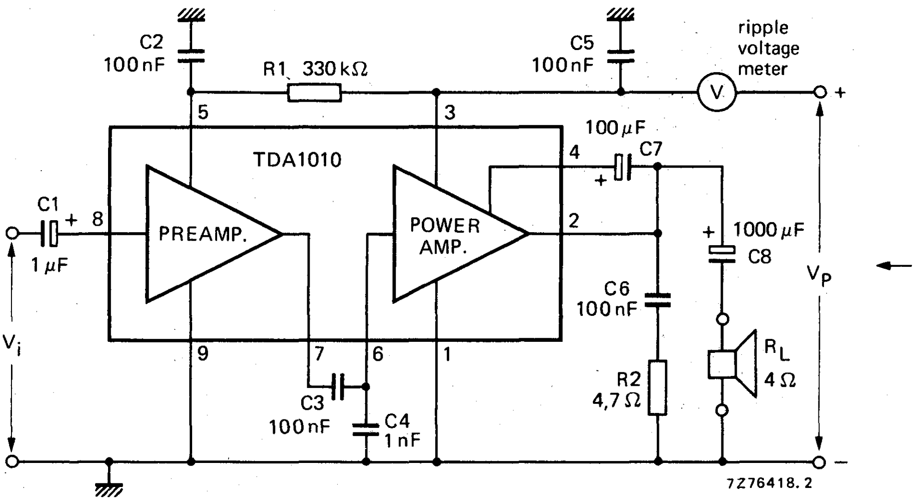


Fig. 3 Test circuit.

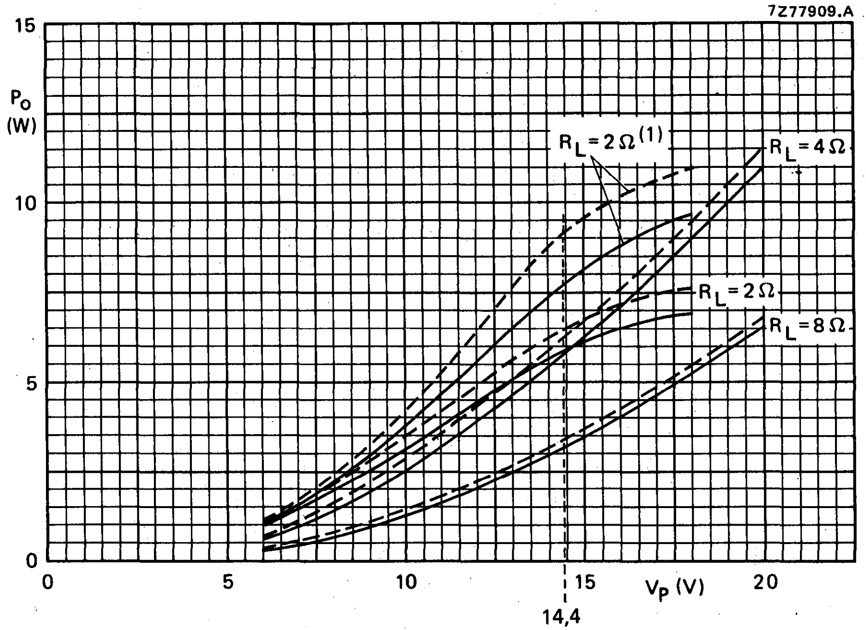


Fig. 4 Output power of the circuit of Fig. 3 as a function of the supply voltage with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\ \Omega^{(1)}$ has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, d_{tot} = 10%, T_{amb} = 25 °C.

Fig. 5 See next page.
Total harmonic distortion in the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter; typical values. Solid lines indicate the power across the load, dashed lines that available at pin 2 of the TDA1010. $R_L = 2\ \Omega^{(1)}$ has been measured with an additional 220 Ω bootstrap resistor between pins 3 and 4. Measurements were made at f = 1 kHz, V_P = 14,4 V.

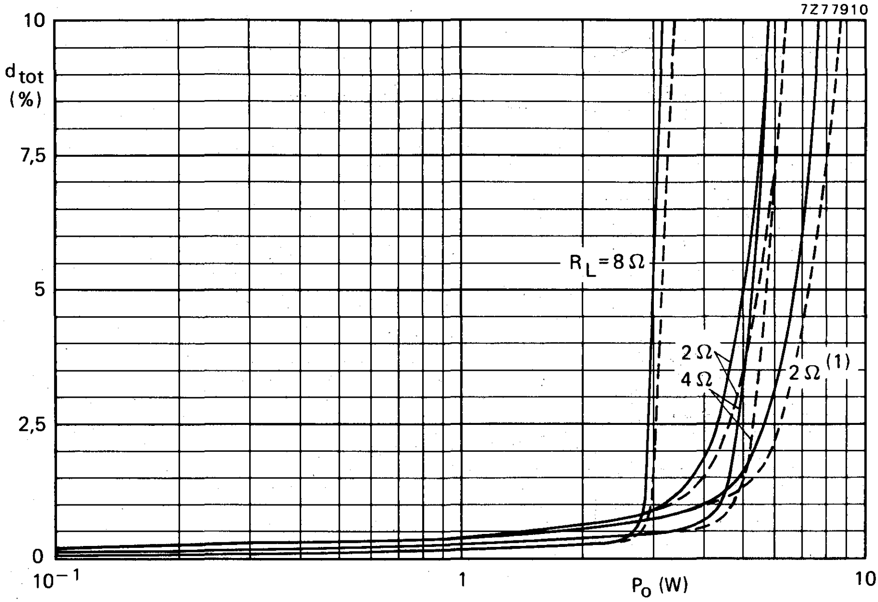


Fig. 5 For caption see page 6.

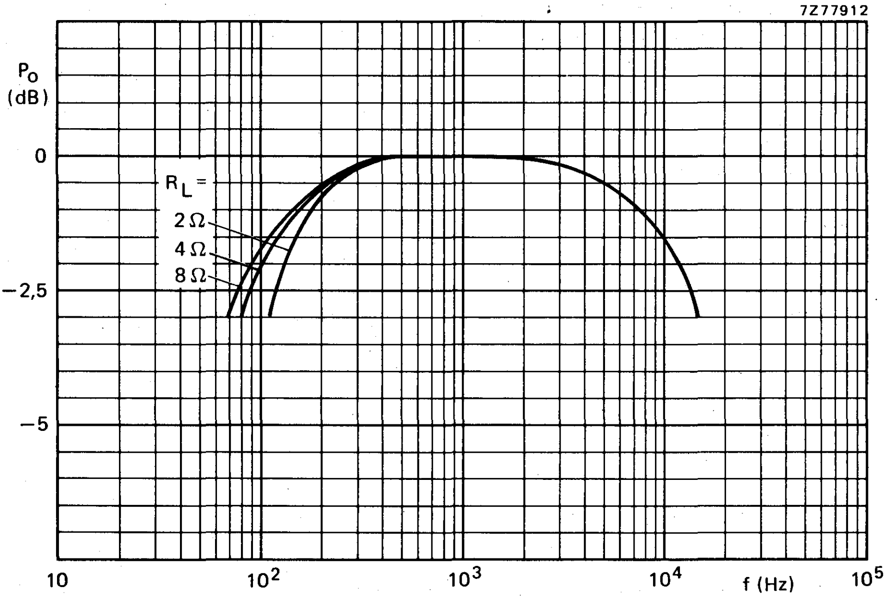


Fig. 6 Frequency characteristics of the circuit of Fig. 3 for three values of load impedance; typical values. P_o relative to 0 dB = 1 W; V_P = 14,4 V.

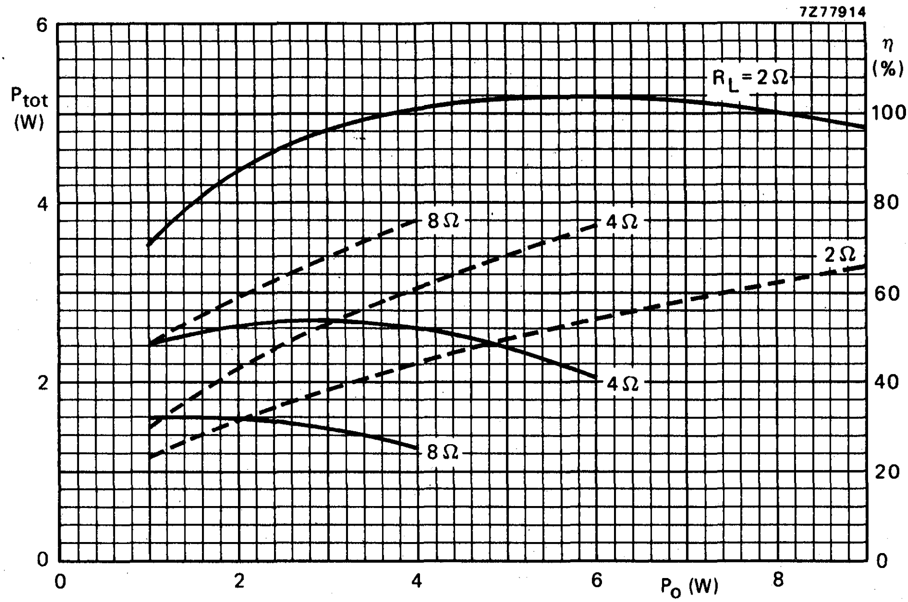


Fig. 7 Total power dissipation (solid lines) and the efficiency (dashed lines) of the circuit of Fig. 3 as a function of the output power with the load impedance as a parameter (for $R_L = 2\ \Omega$ an external bootstrap resistor of 220 Ω has been used); typical values. $V_P = 14{,}4$ V; f = 1 kHz.

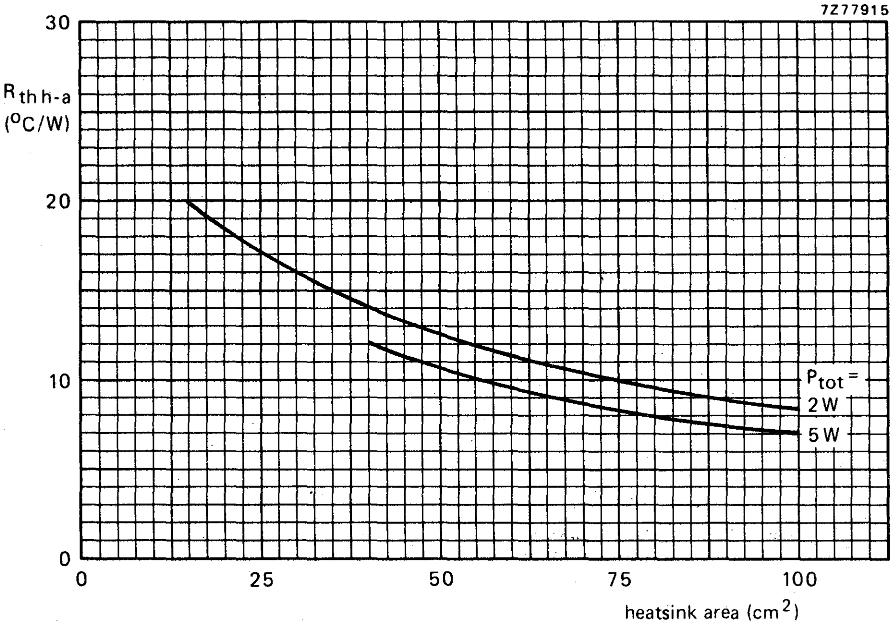


Fig. 8 Thermal resistance from heatsink to ambient of a 1,5 mm thick bright aluminium heatsink as a function of the single-sided area of the heatsink with the total power dissipation as a parameter.

APPLICATION INFORMATION

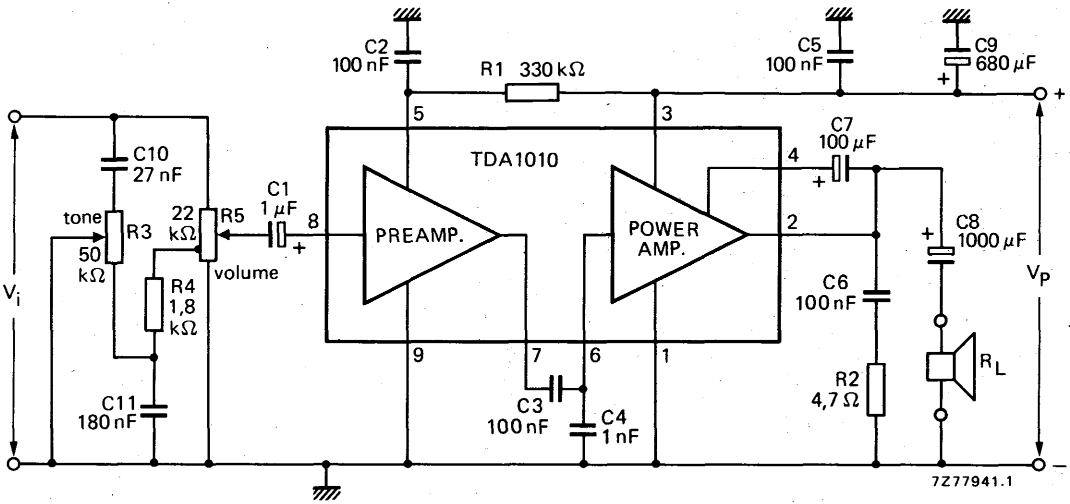


Fig. 9 Complete mono audio amplifier of a car radio.

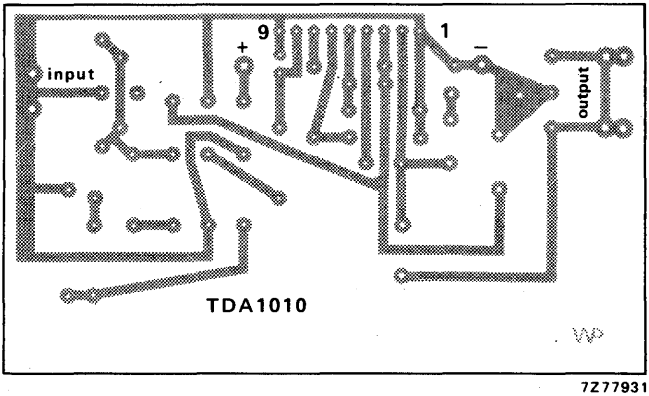


Fig. 10 Track side of printed-circuit board used for the circuit of Fig. 9; p.c. board dimensions 92 mm x 52 mm.

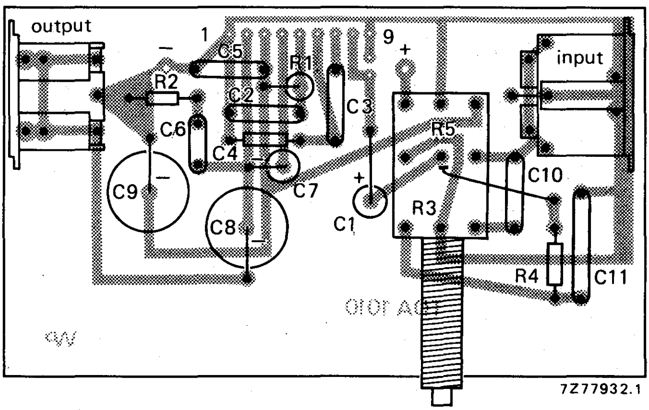


Fig. 11 Component side of printed-circuit board showing component layout used for the circuit of Fig. 9.

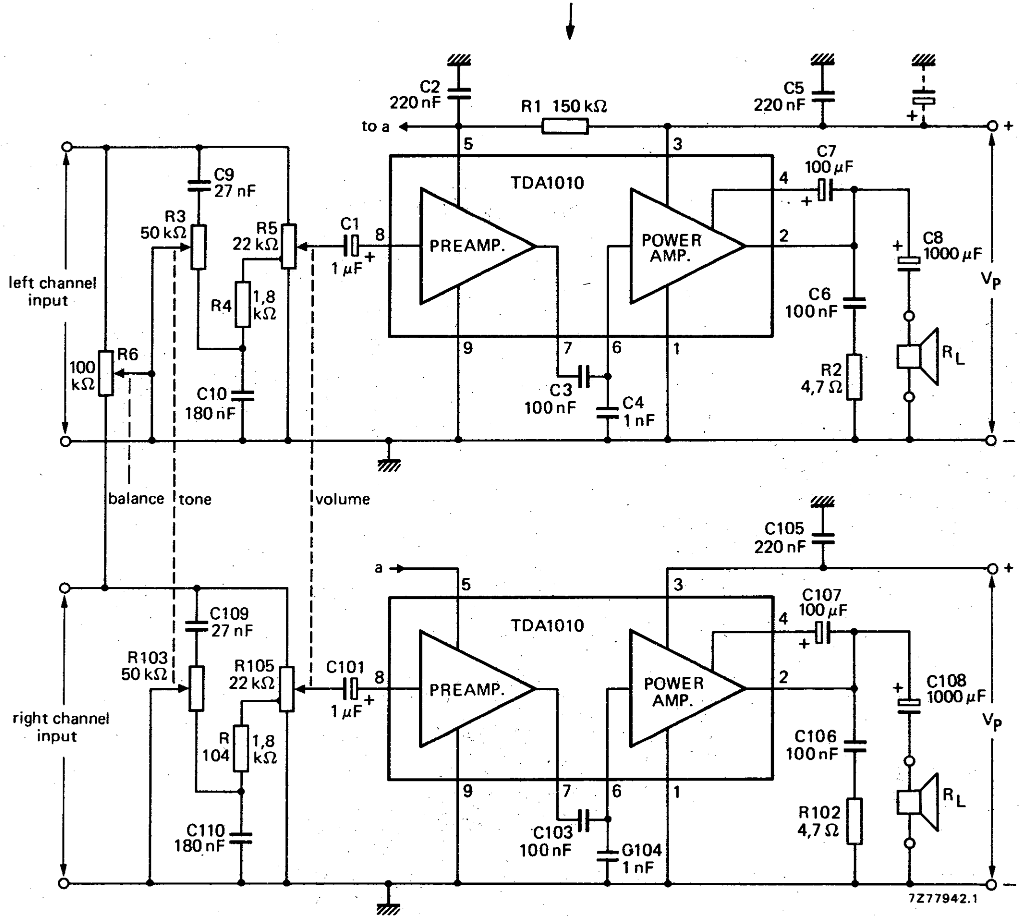


Fig. 12 Complete stereo car radio amplifier.

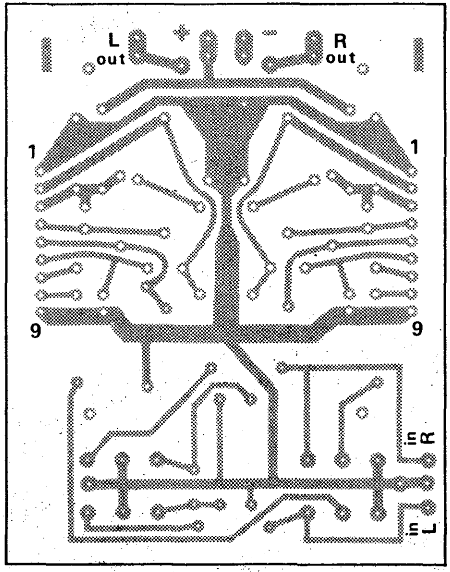


Fig. 13 Track side of printed-circuit board used for the circuit of Fig. 12; p.c. board dimensions 83 mm x 65 mm.

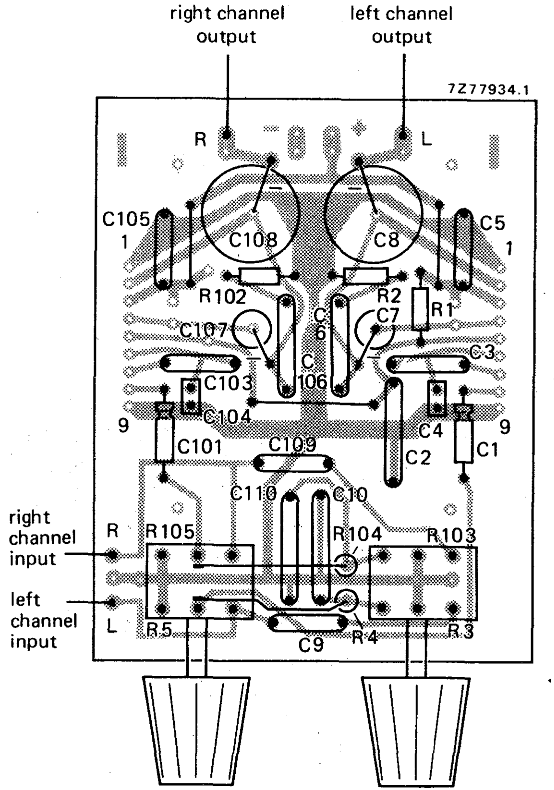


Fig. 14 Component side of printed-circuit board showing component layout used for the circuit of Fig. 12. Balance control is not on the p.c. board.

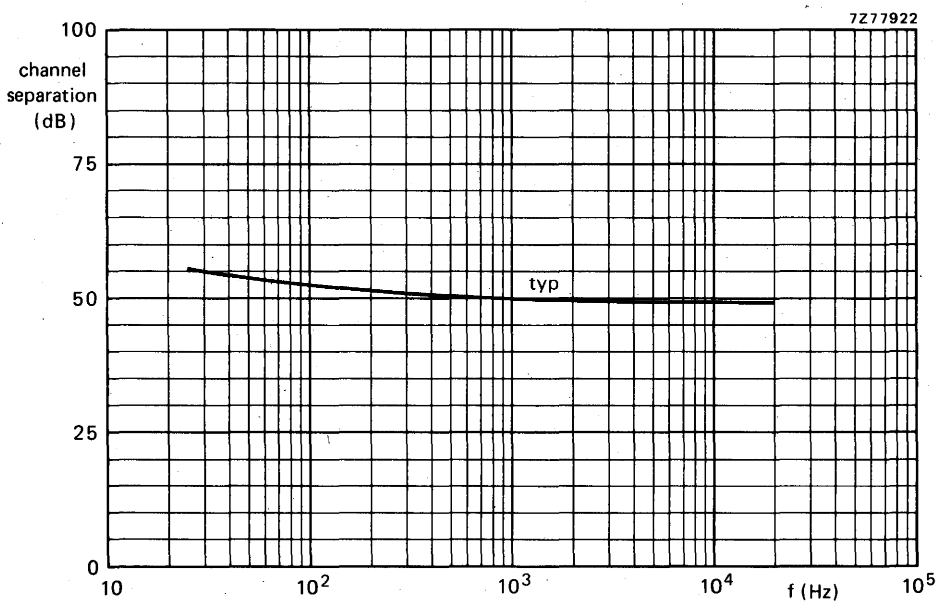


Fig. 15 Channel separation of the circuit of Fig. 12 as a function of the frequency.

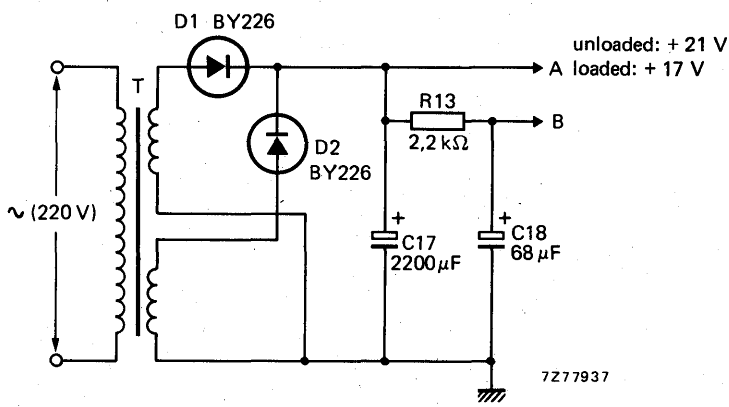


Fig. 16 Power supply of circuit of Fig. 17.

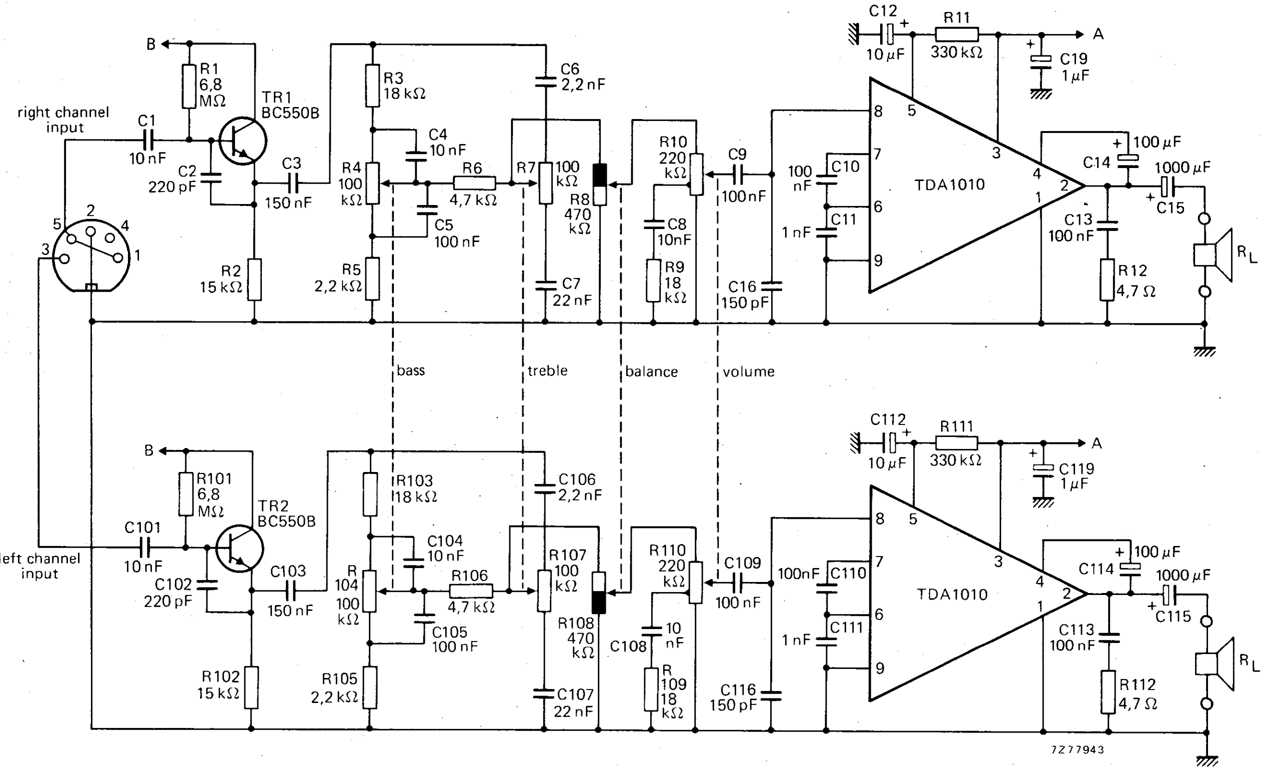


Fig. 17 Complete mains-fed ceramic stereo pick-up amplifier; for power supply see Fig. 16.

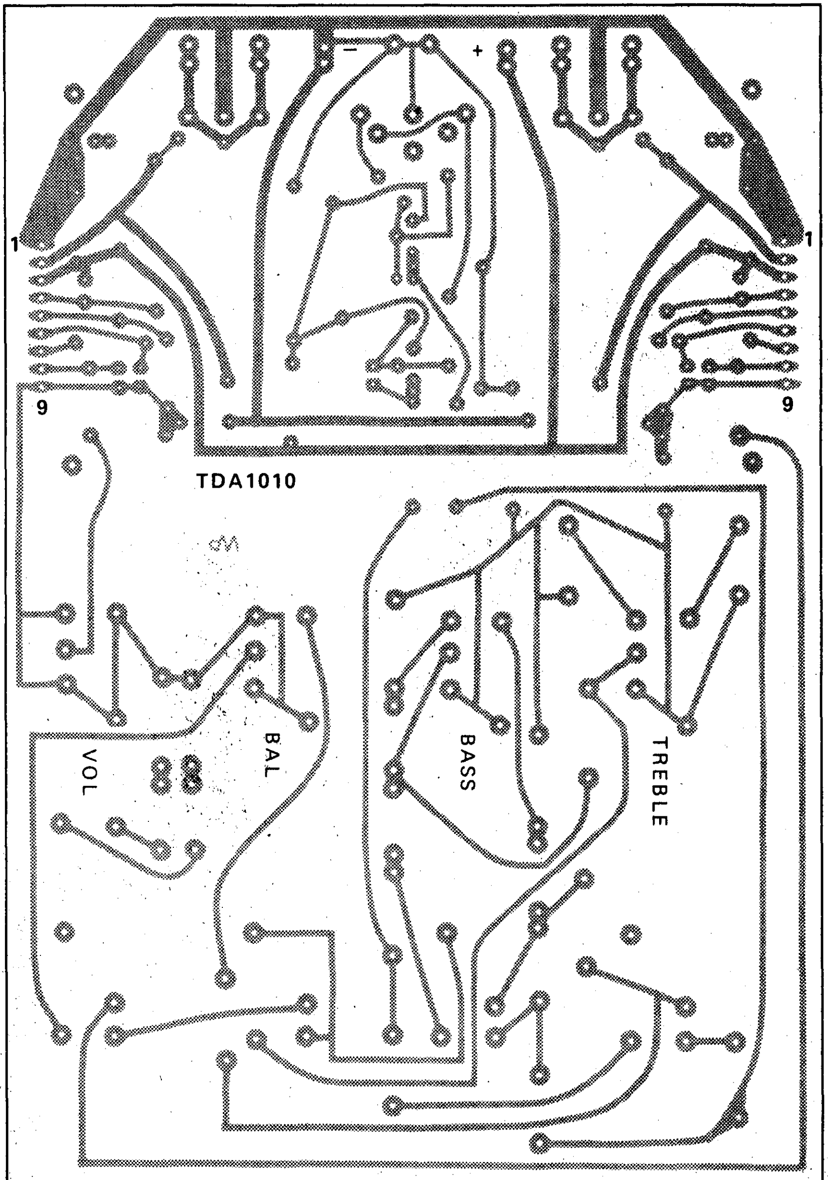


Fig. 18 Track side of printed-circuit board used for the circuit of Fig. 17 (Fig. 16 partly); p.c. board dimensions 169 mm x 118 mm.

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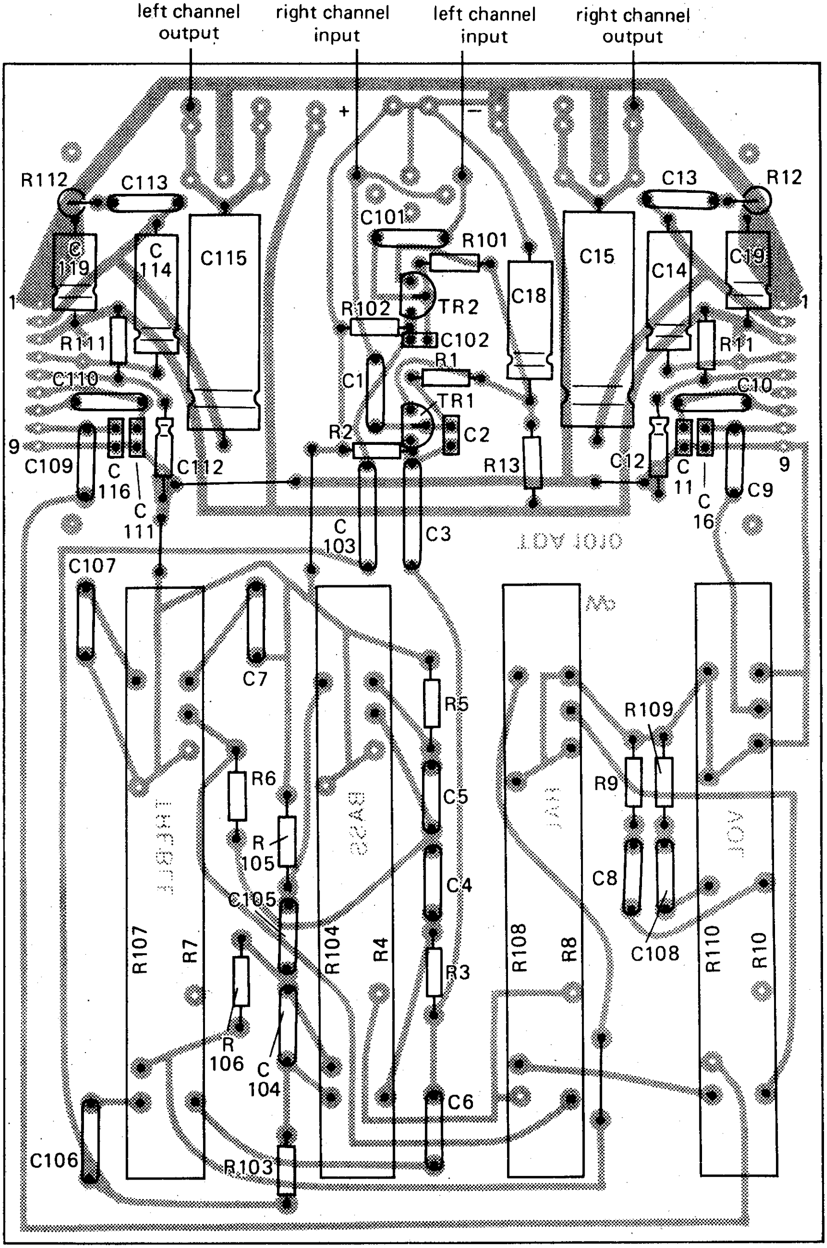


Fig. 19 Component side of printed-circuit board showing component layout used for the circuit of Fig. 17 (Fig. 16 partly).

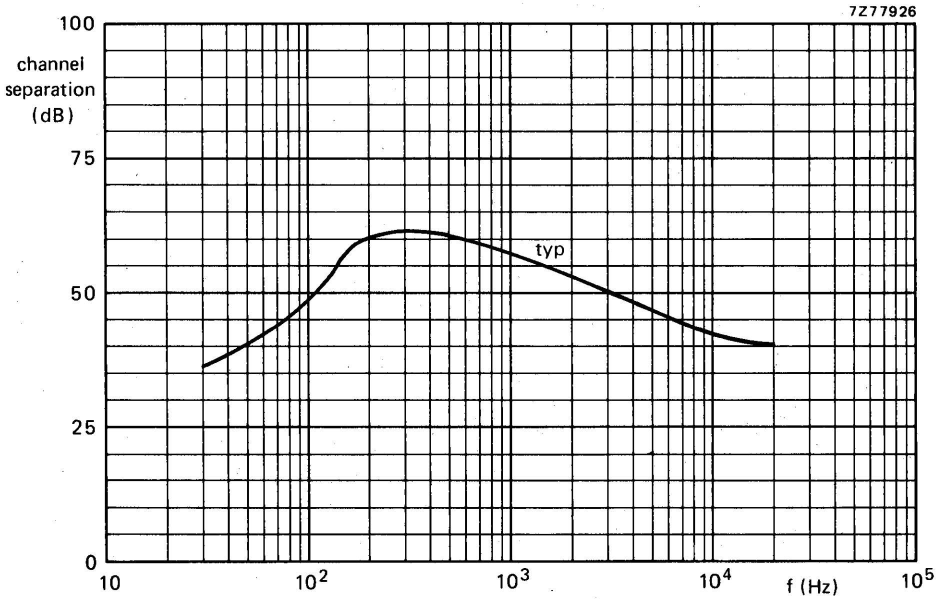


Fig. 20 Channel separation of the circuit of Fig. 17 as a function of frequency.

2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011 is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the very low applicable supply voltage of 3,6 V permits 6 V applications.
Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 24	V
Peak output current	I_{OM}	max.	3	A
Output power at d_{tot} = 10%				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\|Z_i\|$	>	100	kΩ
power amplifier (pin 6)	$\|Z_i\|$	typ.	20	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110A).

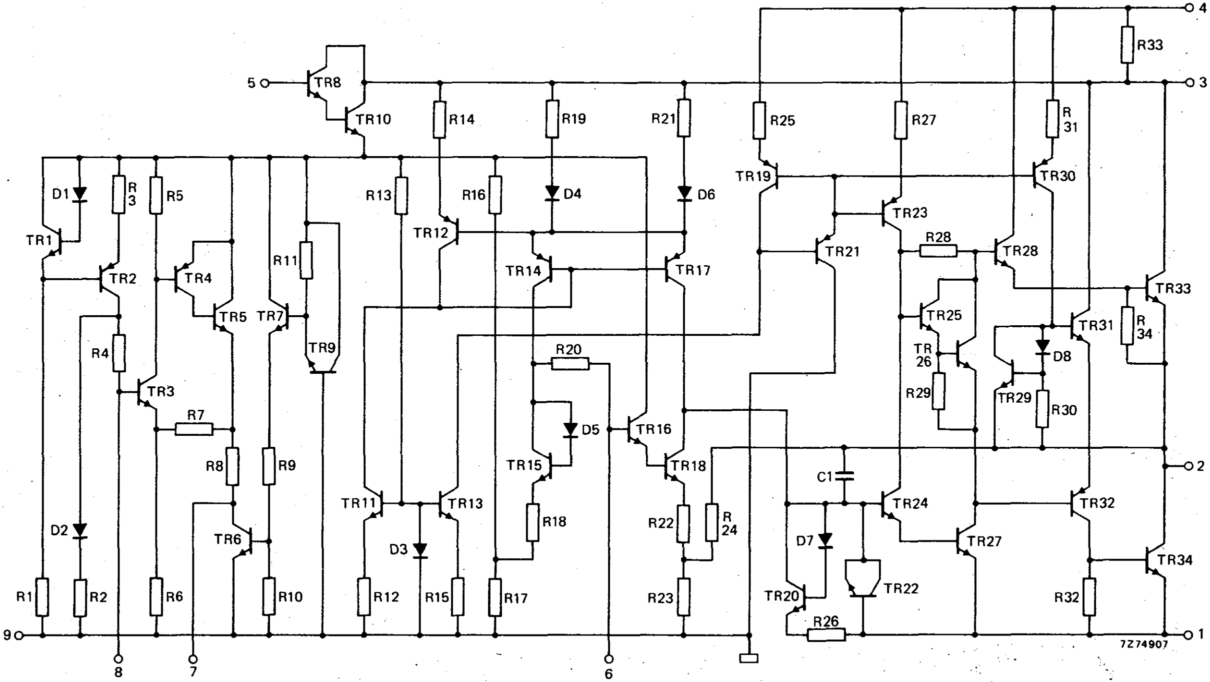


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24	V
Peak output current	I_{OM}	max.	3	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature	T_{amb}	−25 to + 150		°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100	hours

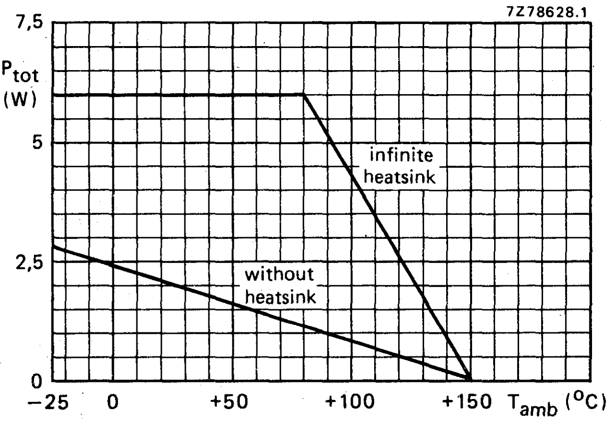


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

Supply voltage range	V_P		3,6 to 24 V
Repetitive peak output current	I_{ORM}	<	2 A
Total quiescent current at V_P = 12 V	I_{tot}	typ. <	14 mA 22 mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; R_L = 4 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at d_{tot} = 10% (note 1)			
with bootstrap:			
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5 W
V_P = 12 V; R_L = 4 Ω	P_o	> typ.	3,6 W 4,2 W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3 W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0 W
without bootstrap:			
→ V_P = 12 V; R_L = 4 Ω	P_o	typ.	3,0 W
Voltage gain:			
preamplifier (note 2)	G_{v1}	typ.	23 dB 21 to 25 dB
power amplifier	G_{v2}	typ.	29 dB 27 to 31 dB
total amplifier	$G_{v\,tot}$	typ.	52 dB 50 to 54 dB
Total harmonic distortion at P_o = 1,5 W	d_{tot}	typ. <	0,3 % 1 %
Frequency response; –3 dB (note 3)	B		60 Hz to 15 kHz
Input impedance:			
preamplifier (note 4)	$\|Z_{i1}\|$	> typ.	100 kΩ 200 kΩ
power amplifier	$\|Z_{i2}\|$	typ.	20 kΩ
Output impedance preamplifier	$\|Z_{o1}\|$	typ.	1 kΩ
Output voltage preamplifier (r.m.s. value) d_{tot} < 1% (note 2)	$V_{o(rms)}$	>	0,7 V
Noise output voltage (r.m.s. value; note 5)			
R_S = 0 Ω	$V_{n(rms)}$	typ.	0,2 mV
R_S = 10 kΩ	$V_{n(rms)}$	typ. <	0,6 mV 1,4 mV
Noise output voltage at f = 500 kHz (r.m.s. value) B = 5 kHz; R_S = 0 Ω	$V_{n(rms)}$	typ.	8 μV
Ripple rejection (note 6)			
f = 1 to 10 kHz	RR	typ.	42 dB
f = 100 Hz; C2 = 1 μF	RR	>	35 dB
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	35 mA

Notes

1. *Measured with an ideal coupling capacitor to the speaker load.*
2. Measured with a load resistor of 20 kΩ.
3. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low *frequencies and by C4 for the high frequencies.*
4. Independent of load impedance of preamplifier.
5. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
6. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude : 2 V).

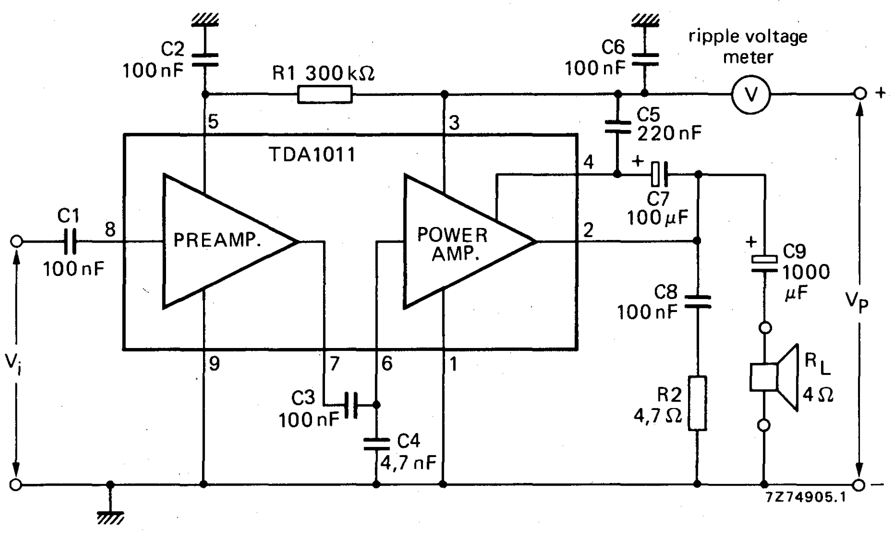


Fig. 3 Test circuit.

APPLICATION INFORMATION

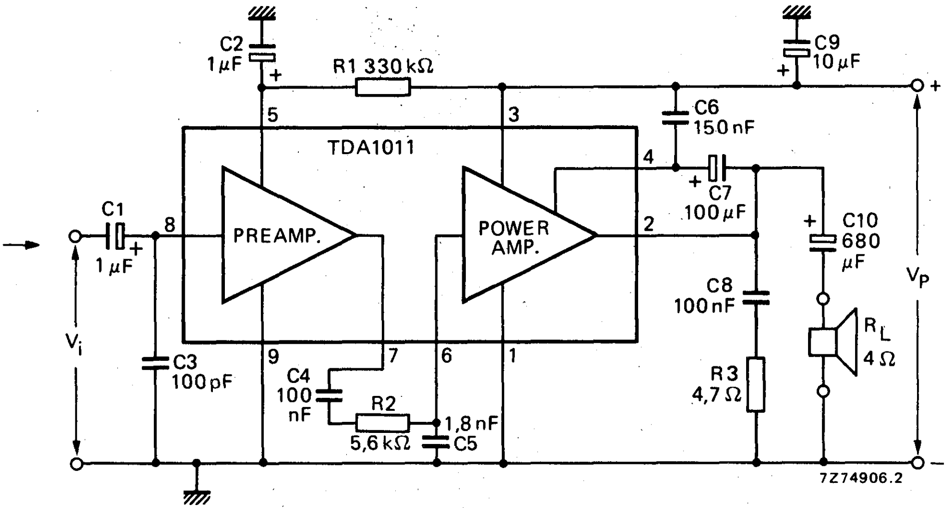


Fig. 4 Circuit diagram of a 4 W amplifier.

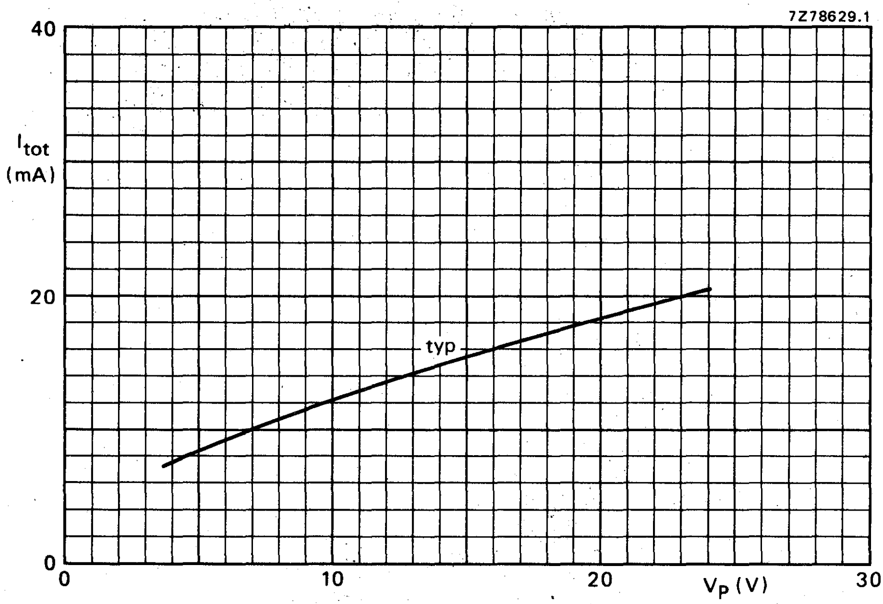


Fig. 5 Total quiescent current as a function of supply voltage.

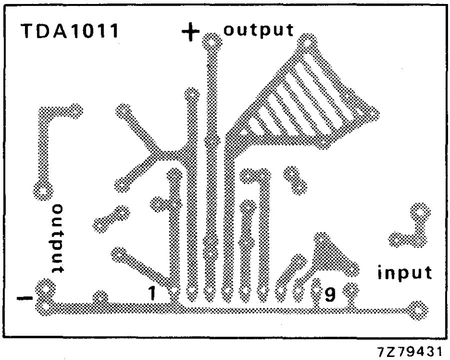


Fig. 6 Track side of printed-circuit board used for the circuit of Fig. 4;
p.c. board dimensions 62 mm x 48 mm.

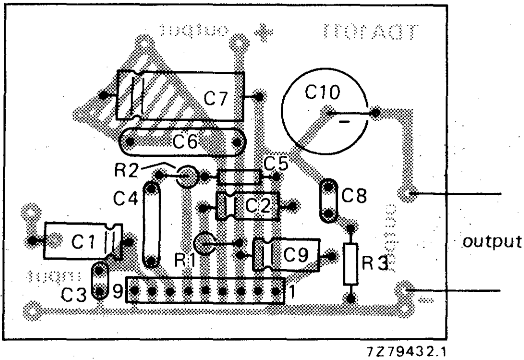


Fig. 7 Component side of printed-circuit board showing component layout used for the circuit of Fig. 4.

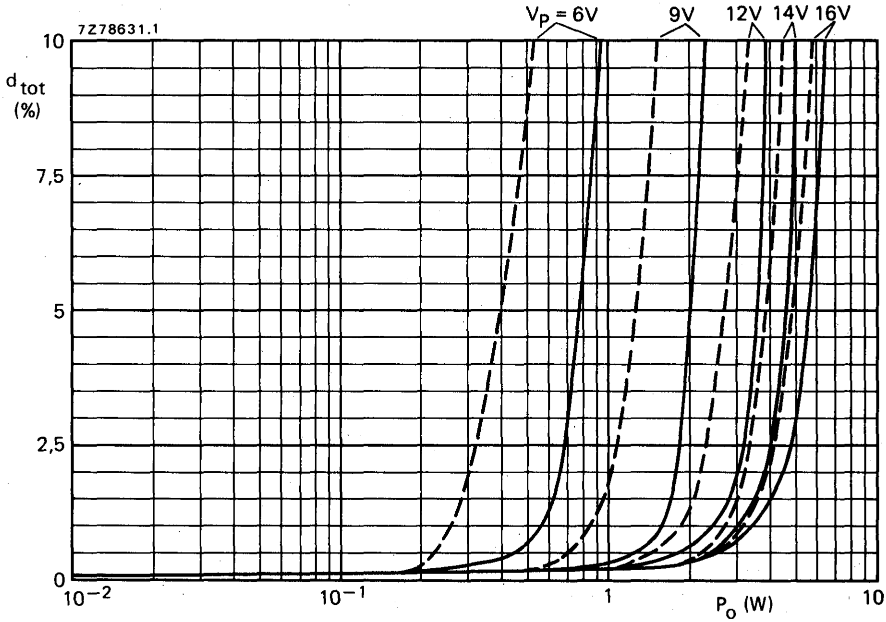


Fig. 8 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; – – – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

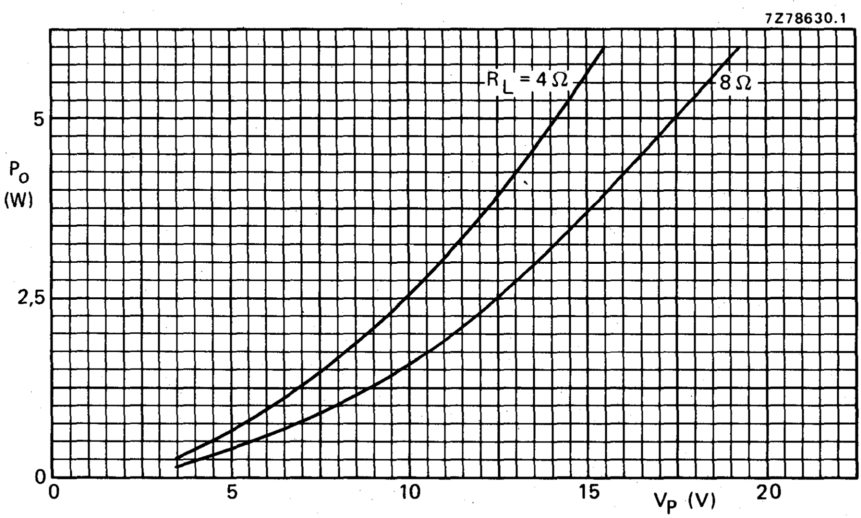


Fig. 9 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

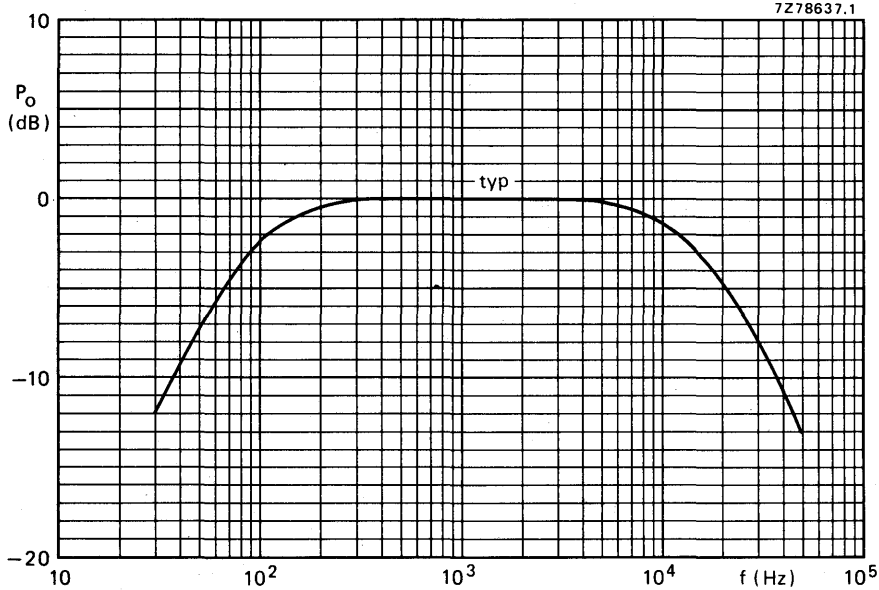


Fig. 10 Voltage gain as a function of frequency; P_o relative to 0 dB = 1 W; V_P = 12 V; R_L = 4 Ω.

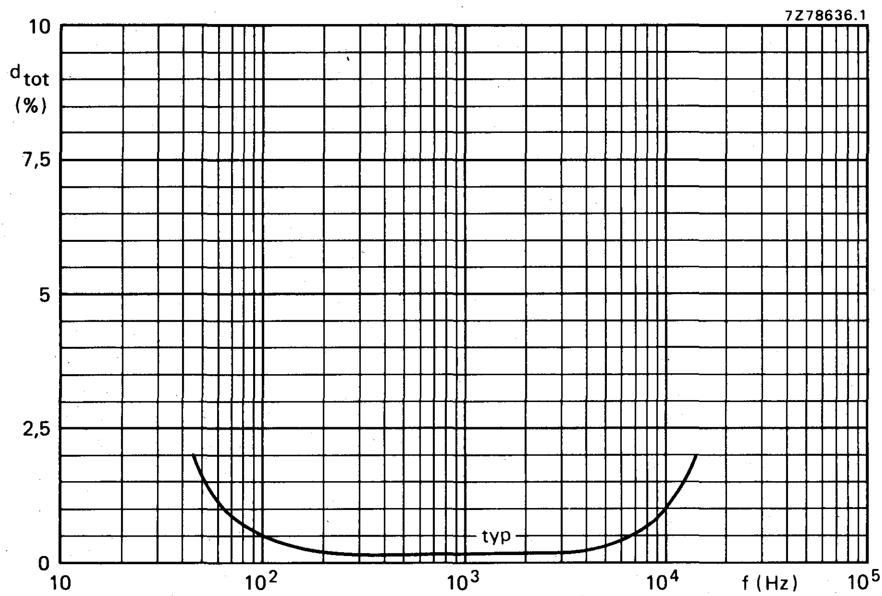


Fig. 11 Total harmonic distortion as a function of frequency; P_o = 1 W; V_P = 12 V; R_L = 4 Ω.

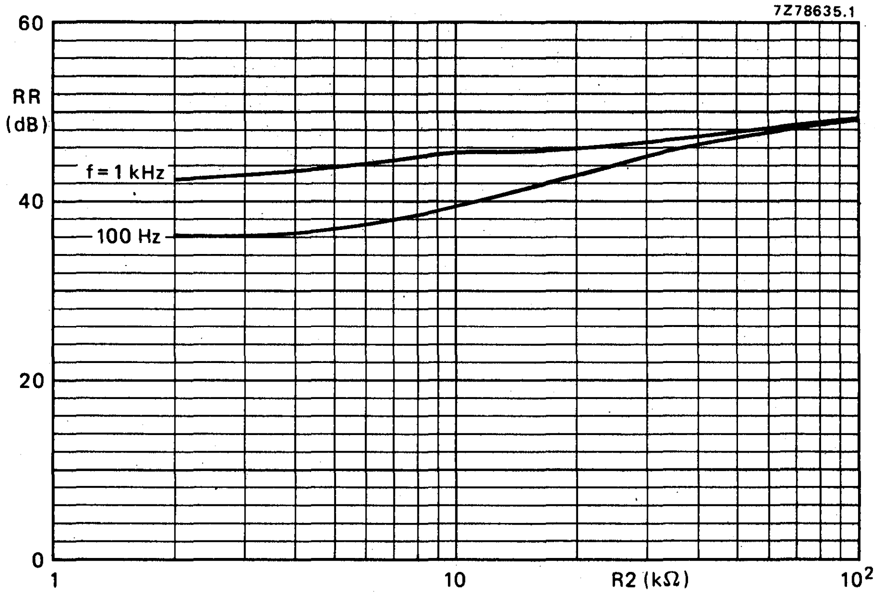


Fig. 12 Ripple rejection as a function of R2 (see Fig. 4); $R_S = 0$; typical values.

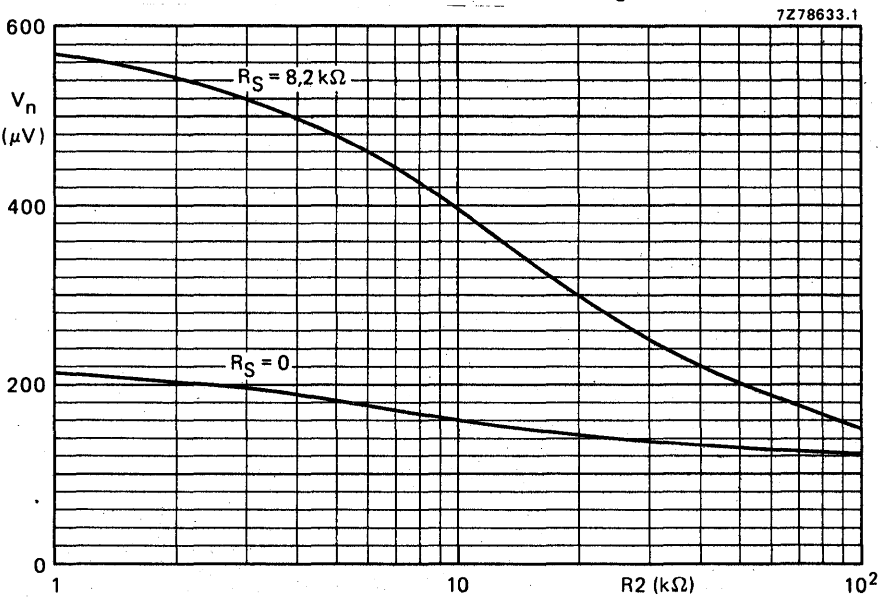


Fig. 13 Noise output voltage as a function of R2 (see Fig. 4); measured according to A-curve; capacitor C5 is adapted for obtaining a constant bandwidth.

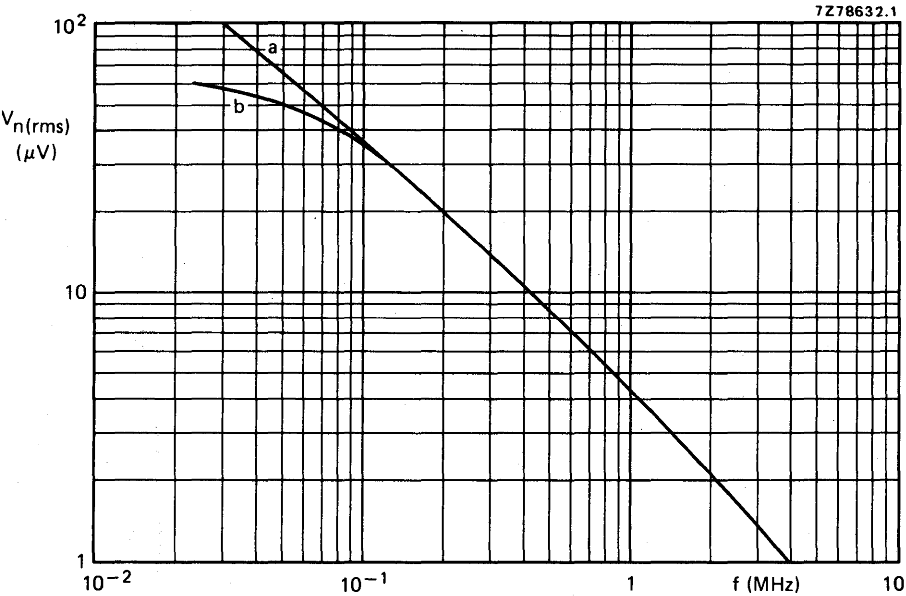


Fig. 14 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

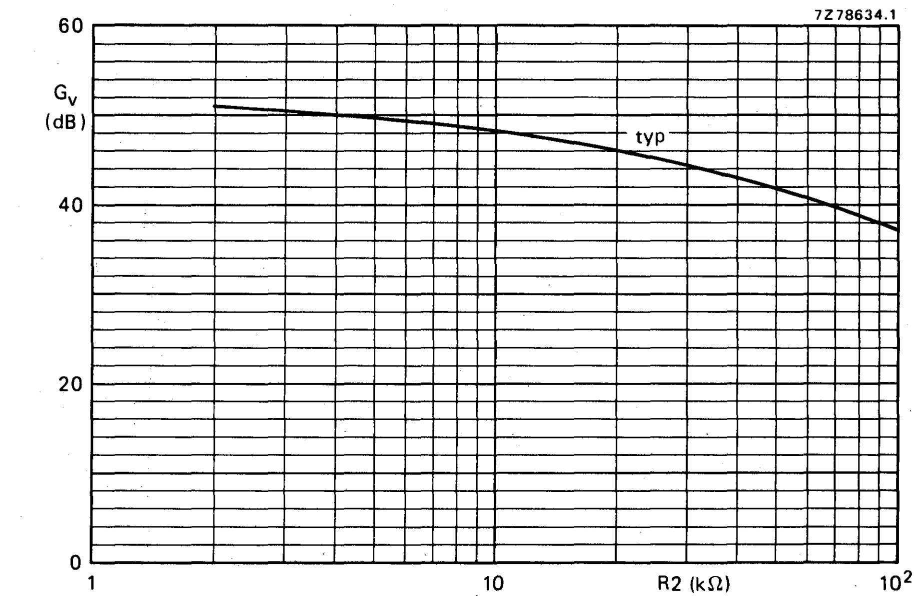


Fig. 15 Voltage gain as a function of R2 (see Fig. 4).

2 TO 6 W AUDIO POWER AMPLIFIER

The TDA1011A is a monolithic integrated audio amplifier circuit in a 9-lead single in-line (SIL) plastic package. The device is especially designed for portable radio and recorder applications and delivers up to 4 W in a 4 Ω load impedance. The device can deliver up to 6 W into 4 Ω at 16 V loaded supply in mains-fed applications. The maximum permissible supply voltage of 24 V makes this circuit very suitable for d.c. and a.c. apparatus, while the low applicable supply voltage of 5,4 V permits 9 V applications. The power amplifier has an inverted input/output which makes the circuit optimal for applications with active tone control and spatial stereo. Special features are:

- single in-line (SIL) construction for easy mounting
- separated preamplifier and power amplifier
- high output power
- thermal protection
- high input impedance
- low current drain
- limited noise behaviour at radio frequencies

QUICK REFERENCE DATA

Supply voltage range	V_P		5,4 to 24	V
Peak output current	I_{OM}	max.	3	A
Output power at d_{tot} = 10%				
V_P = 16 V; R_L = 4 Ω	P_o	typ.	6,5	W
V_P = 12 V; R_L = 4 Ω	P_o	typ.	4,2	W
V_P = 9 V; R_L = 4 Ω	P_o	typ.	2,3	W
V_P = 6 V; R_L = 4 Ω	P_o	typ.	1,0	W
Total harmonic distortion at P_o = 1 W; R_L = 4 Ω	d_{tot}	typ.	0,2	%
Input impedance				
preamplifier (pin 8)	$\lvert Z_i \rvert$	>	100	kΩ
Total quiescent current	I_{tot}	typ.	14	mA
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110A).

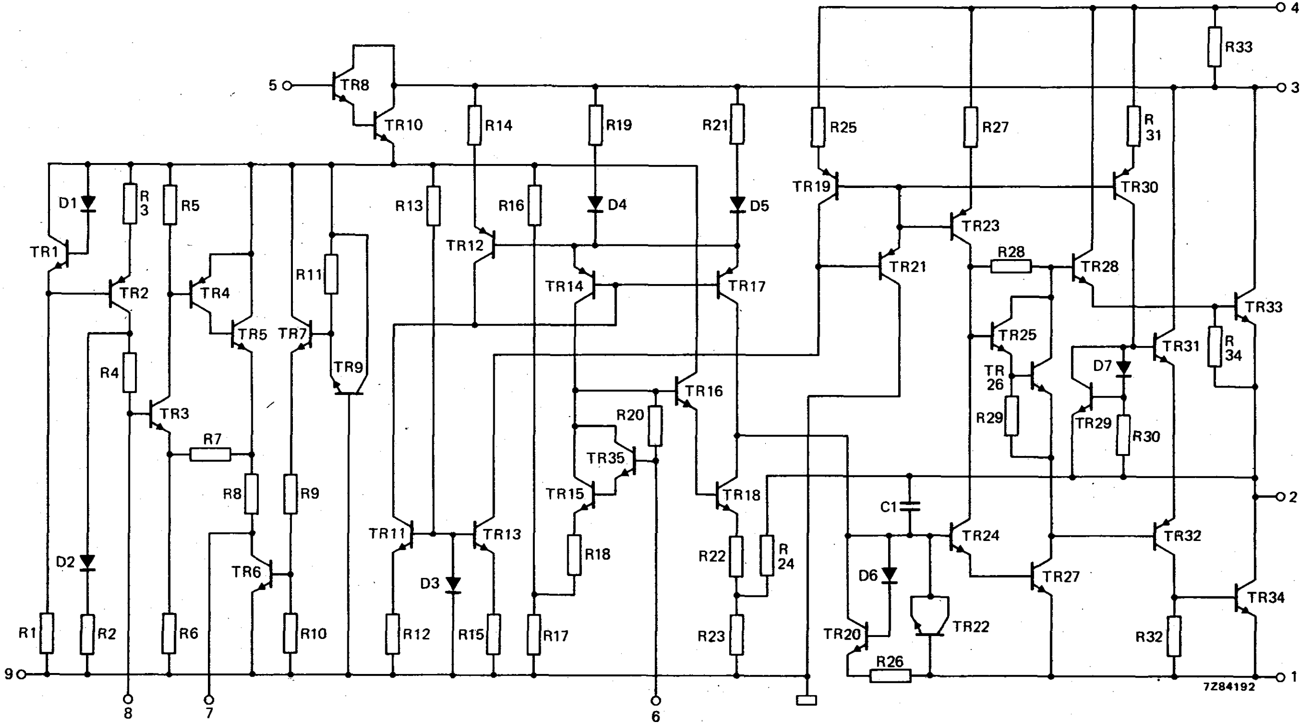


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	24	V
Peak output current	I_{OM}	max.	3	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature	T_{amb}	−25 to + 150		°C
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100	hours

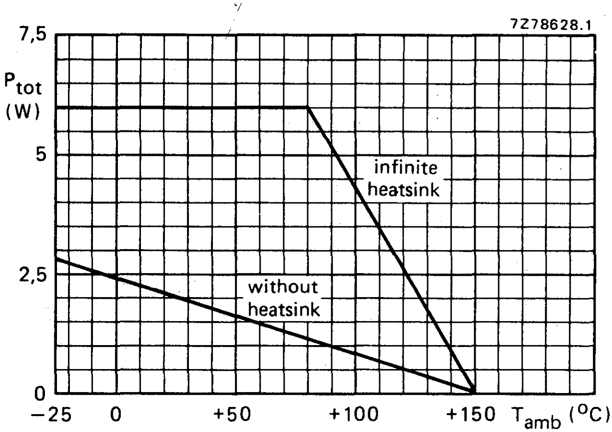


Fig. 2 Power derating curve.

D.C. CHARACTERISTICS

Supply voltage range	V_P		5,4 to 24	V
Repetitive peak output current	I_{ORM}	<	2	A
Total quiescent current at $V_P = 12$ V	I_{tot}	typ.	14	mA
		<	22	mA

A.C. CHARACTERISTICS

$T_{amb} = 25\ ^oC$; $V_P = 12$ V; $R_L = 4\ \Omega$; f = 1 kHz unless otherwise specified; see also Fig. 3.

A.F. output power at $d_{tot} = 10\%$ (note 1)				
with bootstrap:				
$V_P = 16$ V; $R_L = 4\ \Omega$	P_o	typ.	6,5	W
$V_P = 12$ V; $R_L = 4\ \Omega$	P_o	>	3,6	W
		typ.	4,2	W
$V_P = 9$ V; $R_L = 4\ \Omega$	P_o	typ.	2,3	W
$V_P = 6$ V; $R_L = 4\ \Omega$	P_o	typ.	1,0	W
without bootstrap:				
$V_P = 12$ V; $R_L = 4\ \Omega$	P_o	typ.	3,5	W
Voltage gain:				
preamplifier (note 2)	G_{v1}	typ.	23	dB
			21 to 25	dB
power amplifier (note 3)	G_{v2}	typ.	29	dB
total amplifier (note 3)	$G_{v\ tot}$	typ.	52	dB
Total harmonic distortion at $P_o = 1{,}5$ W	d_{tot}	typ.	0,3	%
		<	1	%
Frequency response; –3 dB (note 4)	B		60 Hz to 15	kHz
Input impedance:				
preamplifier (note 5)	$\vert Z_{i1}\vert$	>	100	kΩ
		typ.	200	kΩ
Output impedance preamplifier	$\vert Z_{o1}\vert$	typ.	1	kΩ
Output voltage preamplifier (r.m.s. value)				
$d_{tot} < 1\%$ (note 2)	$V_{o(rms)}$	>	0,7	V
Noise output voltage (r.m.s. value; note 6)				
$R_S = 0\ \Omega$	$V_{n(rms)}$	typ.	0,5	mV
$R_S = 10$ kΩ	$V_{n(rms)}$	typ.	0,8	mV
Noise output voltage at f = 500 kHz (r.m.s. value)				
B = 5 kHz; $R_S = 0\ \Omega$	$V_{n(rms)}$	typ.	8	μV
Ripple rejection (note 6)				
f = 1 to 10 kHz	RR	typ.	42	dB
f = 100 Hz; C2 = 1 μF	RR	>	35	dB
Bootstrap current at onset of clipping; pin 4 (r.m.s. value)	$I_{4(rms)}$	typ.	35	mA

Notes

1. Measured with an ideal coupling capacitor to the speaker load.
2. Measured with a load resistor of 20 kΩ.
3. Measured with R2 = 20 kΩ.
4. Measured at P_o = 1 W; the frequency response is mainly determined by C1 and C3 for the low frequencies and by C4 for the high frequencies.
5. Independent of load impedance of preamplifier.
6. Unweighted r.m.s. noise voltage measured at a bandwidth of 60 Hz to 15 kHz (12 dB/octave).
7. Ripple rejection measured with a source impedance between 0 and 2 kΩ (maximum ripple amplitude: 2 V).

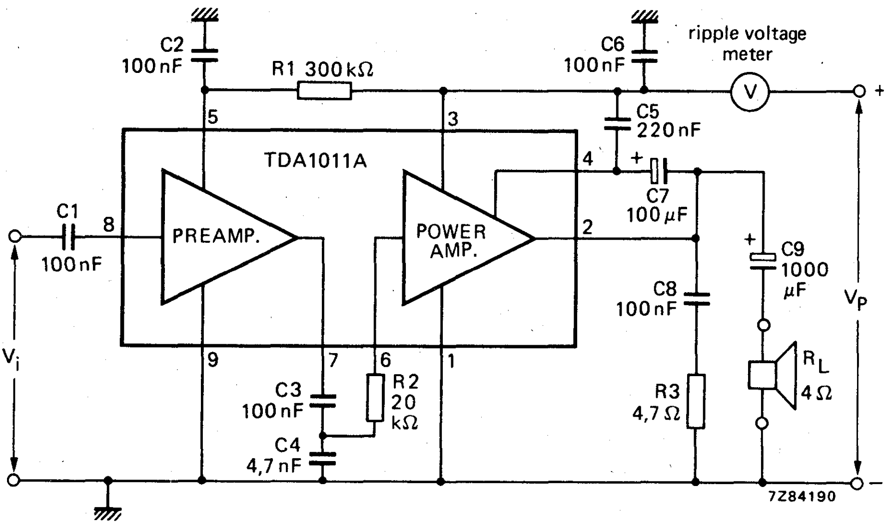


Fig. 3 Test circuit.

APPLICATION INFORMATION

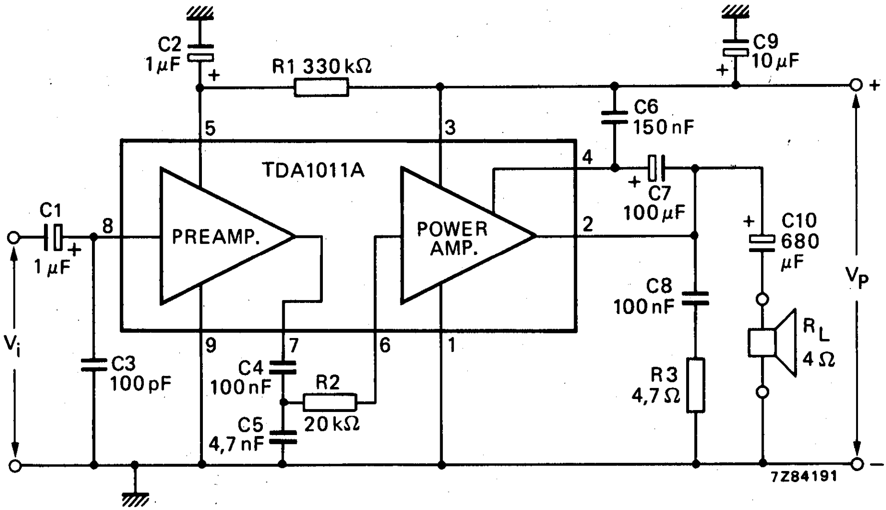


Fig. 4 Circuit diagram of a 4 W amplifier.

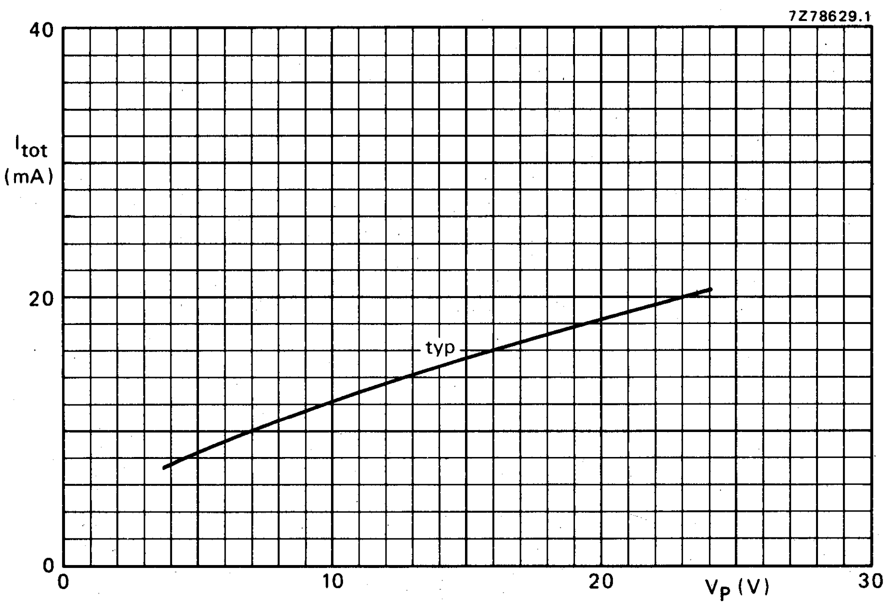


Fig. 5 Total quiescent current as a function of supply voltage.

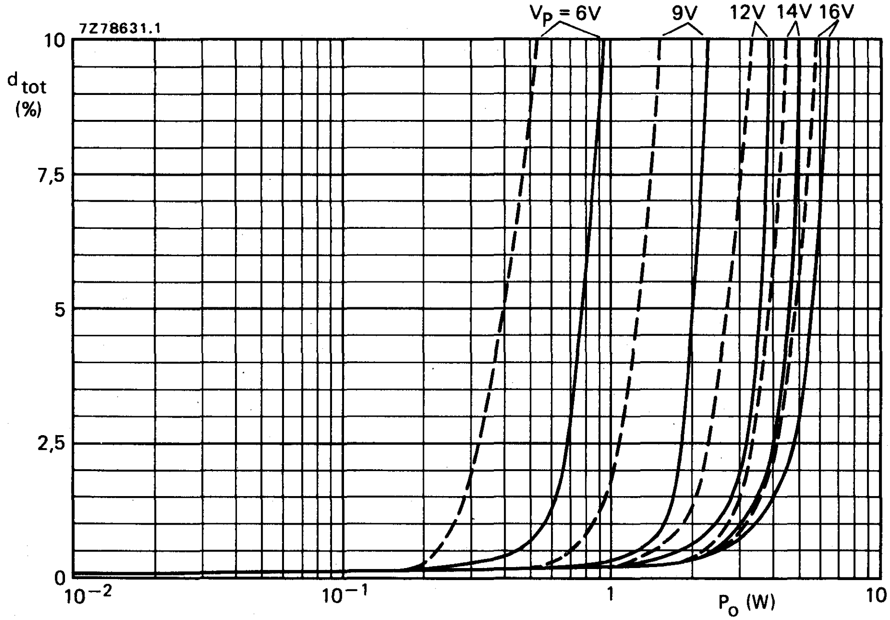


Fig. 6 Total harmonic distortion as a function of output power across R_L; —— with bootstrap; –.– – without bootstrap; f = 1 kHz; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

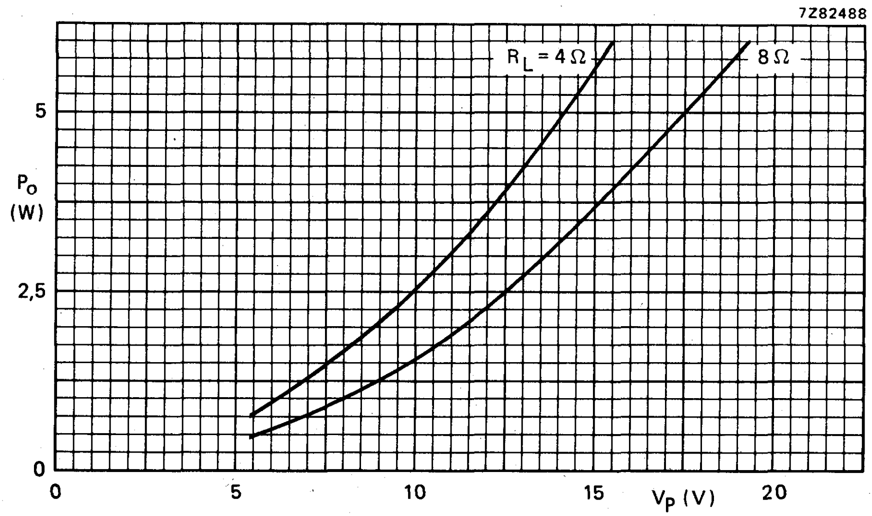


Fig. 7 Output power across R_L as a function of supply voltage with bootstrap; d_{tot} = 10%; typical values. The available output power is 5% higher when measured at pin 2 (due to series resistance of C10).

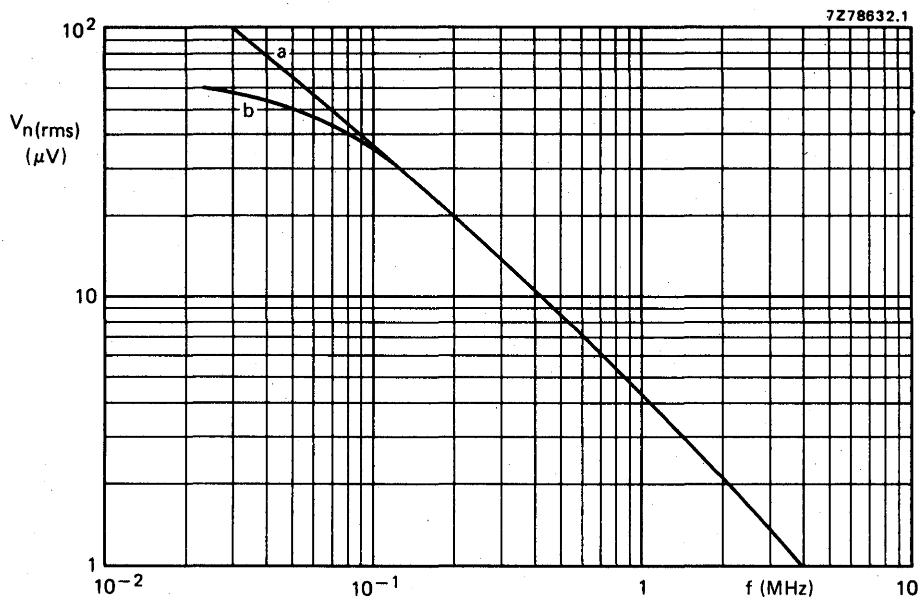


Fig. 8 Noise output voltage as a function of frequency; curve a: total amplifier; curve b: power amplifier; B = 5 kHz; R_S = 0; typical values.

RECORDING / PLAY-BACK AND 2 W AUDIO POWER AMPLIFIER

The TDA1012 is a monolithic integrated audio power amplifier, preamplifier and A.L.C. circuit designed for applications in radio-recorders and recorders. The wide supply voltage range makes this circuit very suitable for d.c. and a.c. apparatus. The circuit is thermal protected and contains the following functions:

- Power amplifier
- Preamplifier
- Automatic Level Control (A.L.C.) circuit
- Voltage stabilizer

QUICK REFERENCE DATA

Supply voltage range	V_P		3,6 to 18	V
Total quiescent current at $V_P = 9$ V	I_{tot}	typ.	14	mA
Power amplifier				
Output power at $d_{tot} = 10$ % $V_P = 9$ V; $R_L = 4\ \Omega$	P_o	typ.	2	W
Closed loop voltage gain	G_c	typ.	36	dB
Preamplifier				
Open loop voltage gain	G_o	>	66	dB
Minimum closed loop voltage gain	$G_{c\,min}$		31	dB
Output voltage at $d_{tot} = 1$ %	V_o	>	2	V
Automatic Level Control (A.L.C.)				
Gain variation for $\Delta V_i = 40$ dB	ΔG_v	typ.	2	dB
Stabilized supply voltage				
Output voltage	$V_{11\text{-}15}$	typ.	4,2	V

PACKAGE OUTLINE

16-lead DIL; plastic medium power (with internal heat spreader).

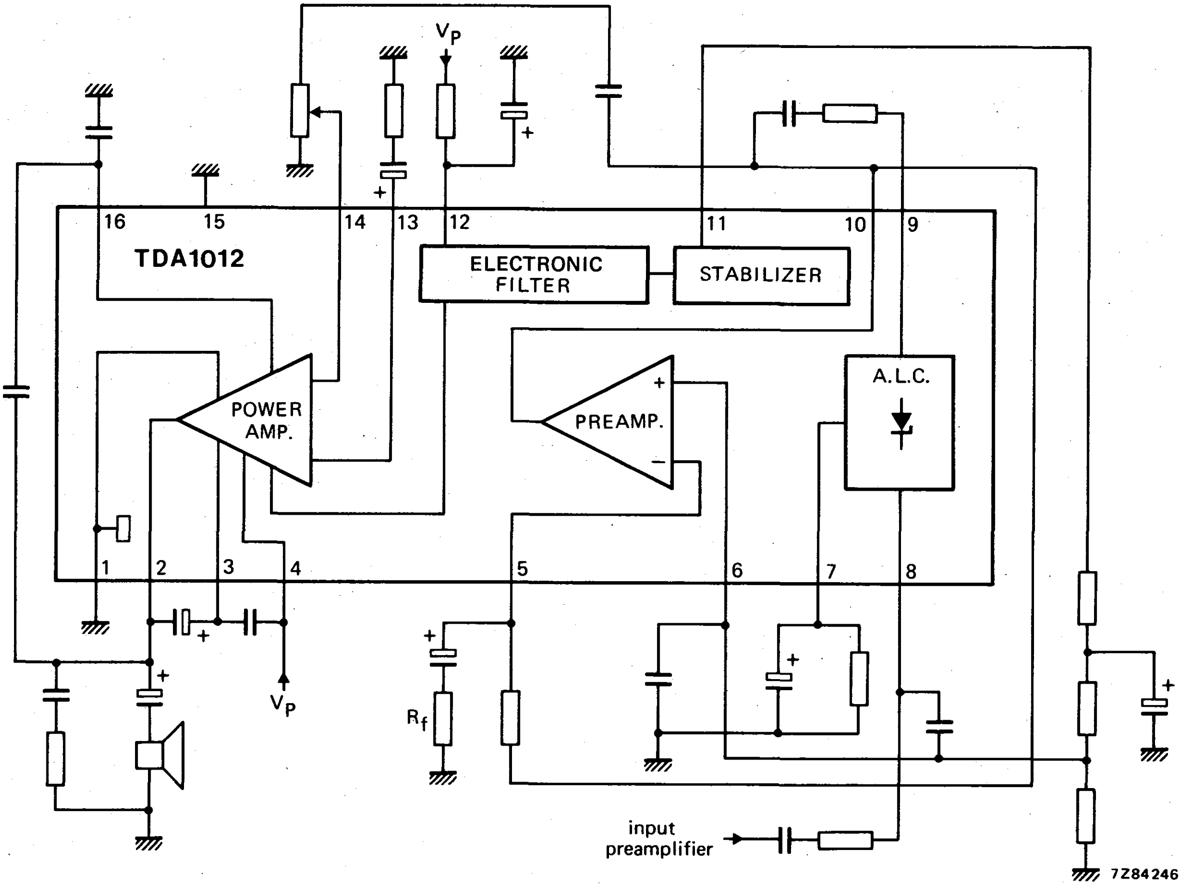


Fig. 1 Block diagram with external components; also used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 4)	$V_P = V_{4\text{-}1}$	max.	18	V
Non-repetitive peak output current (pin 2)	I_{OSM}	max.	2	A
Storage temperature	T_{stg}		−55 to +150	°C
Crystal temperature	T_c	max.	150	°C
Total power dissipation	see derating curve Fig. 2			
A.C. short-circuit duration of load during sine-wave drive; V_P = 12 V	t_{sc}	max.	100	hours

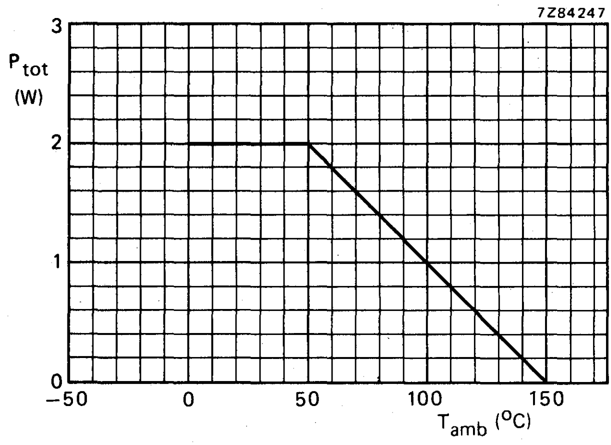


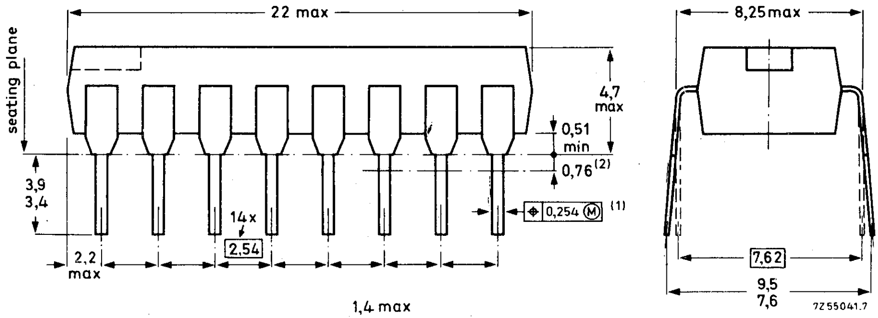
Fig. 2 Power derating curve.

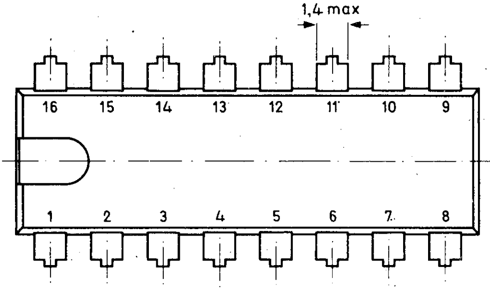
CHARACTERISTICS

$V_P = 9$ V; $R_L = 4\ \Omega$; f = 1 kHz; $T_{amb} = 25\ ^oC$; measured in test circuit of Fig. 1; unless otherwise specified.

Power amplifier			
Output power at d_{tot} = 10 %	P_o	typ.	2 W
Closed loop voltage gain	G_c	typ.	36 dB
Total harmonic distortion at P_o = 1W	d_{tot}	<	1 %
Input impedance	$\|Z_i\|$	>	1 MΩ
Ripple rejection at f = 100 Hz	RR	>	40 dB
Noise output voltage (r.m.s. value) $R_S = 0\ \Omega$; B = 60 Hz to 15 kHz	$V_{n(rms)}$	typ.	150 µV
Preamplifier			
Open loop voltage gain	G_o	>	66 dB
Closed loop voltage gain	G_c	typ.	48 dB
Minimum closed loop voltage gain (when changing R_f)	$G_{c\ min}$		31 dB
Output voltage at d_{tot} = 1 %	V_o	>	2 V
Output voltage with A.L.C. V_i = 4,8 mV	V_o	typ.	1,1 V
Total harmonic distortion with A.L.C.			
V_i = 4,8 mV	d_{tot}	<	1 %
V_i = 480 mV	d_{tot}	<	3 %
Signal-to-noise ratio related to V_i = 1,2 mV; $R_S = 0\ \Omega$; B = 60 Hz to 15 kHz	S/N	typ.	60 dB
Input impedance	$\|Z_i\|$	>	100 kΩ
Ripple rejection at f = 100 Hz	RR	>	52 dB
Output impedance	$\|Z_o\|$	<	50 Ω
Automatic Level Control (A.L.C.)			
Gain variation for ΔV_i = 40 dB	ΔG_v	typ.	2 dB
Limiting time at ΔV_i = 40 dB	t_l	<	50 ms
Level setting time at ΔV_i = 40 dB	t_s	<	50 ms
Recovery time at ΔV_i = 40 dB	t_r	typ.	100 s
Voltage stabilizer			
Output voltage	V_{11-15}	typ.	4,2 V
Load current	I_{11}	<	1 mA
Ripple rejection at f = 100 Hz	RR	>	40 dB

16-LEAD DUAL IN-LINE; PLASTIC MEDIUM POWER





top view

Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

4 W AUDIO POWER AMPLIFIER WITH D.C. VOLUME CONTROL

The TDA1013 is a monolithic integrated audio amplifier circuit with d.c. volume control in a 9-lead single in-line (SIL) plastic package. The wide supply voltage range makes this circuit very suitable for applications in mains-fed apparatus such as : television receivers and record players.
The d.c. volume control stage has a good control characteristic with a range of more than 80 dB; control can be obtained by means of a variable d.c. voltage between 4 and 8 V.
The audio amplifier has a well defined open loop gain and a fixed integrated closed loop gain. This offers an optimum in number of external components, performance and stability.
The SIL package (SOT-110A) offers a simple and low-cost heatsink connection.

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35	V
Repetitive peak output current	I_{ORM}	max.	1,5	A
Total sensitivity (d.c. control at max. gain) for P_o = 2,5 W	V_i	typ.	55	mV
Audio amplifier				
Output power at d_{tot} = 10 % V_P = 18 V; R_L = 8 Ω	P_o	typ.	4,5	W
Total harmonic distortion at P_o = 2,5 W; R_L = 8 Ω	d_{tot}	typ.	0,5	%
Sensitivity for P_o = 2,5 W	V_i	typ.	125	mV
D.C. volume control unit				
Gain control range	ϕ	>	80	dB
Signal handling at $d_{tot} < 1\%$ (d.c. control at 0 dB)	V_i	>	1,2	V
Sensitivity for V_o = 125 mV at max. voltage gain	V_i	typ.	55	mV
Input impedance (pin 9)	$\|Z_i\|$	typ.	200	kΩ

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110A).

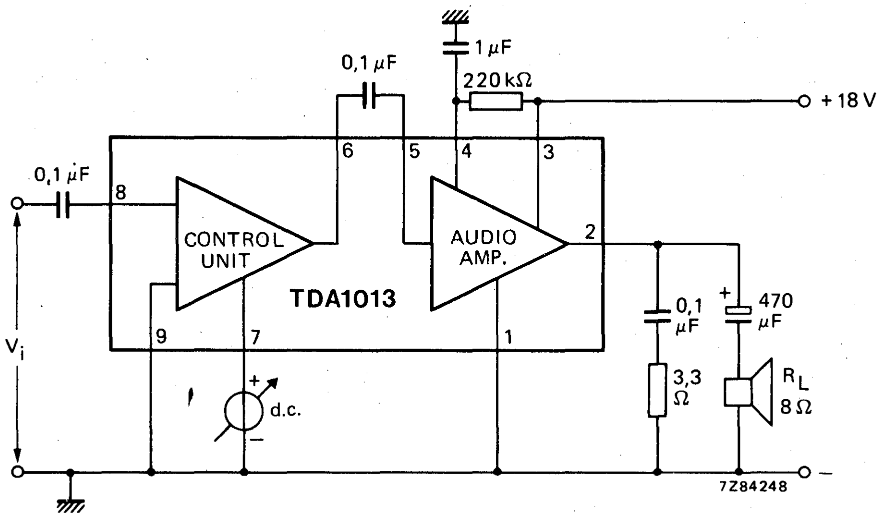


Fig. 1 Block diagram and external components.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35 V
Non-repetitive peak output current	I_{OSM}	max.	3 A
Repetitive peak output current	I_{ORM}	max.	1,5 A
Storage temperature	T_{stg}	–55 to + 150	°C
Crystal temperature	T_j	–25 to + 150	°C
Total power dissipation	see derating curve	Fig. 2	

HEATSINK DESIGN

Assume V_P = 18 V; R_L = 8 Ω; T_{amb} = 60 °C (max.); T_j = 150 °C (max.); for a 4 W application into an 8 Ω load, the maximum dissipation is about 2,5 W.
The thermal resistance from junction to ambient can be expressed as:

$$R_{th\ j\text{-}a} = R_{th\ j\text{-}tab} + R_{th\ tab\text{-}h} + R_{th\ h\text{-}a} = \frac{T_{j\ max} - T_{amb\ max}}{P_{max}} = \frac{150 - 60}{2,5} = 36\ \text{K/W}.$$

Since $R_{th\ j\text{-}tab}$ = 12 K/W and $R_{th\ tab\text{-}h}$ = 1 K/W, $R_{th\ h\text{-}a}$ = 36 – (12 + 1) = 23 K/W.

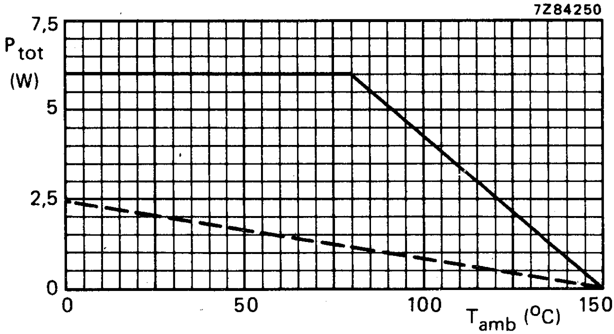


Fig. 2 Power derating curve.
——— infinite heatsink;
– – – without heatsink.

CHARACTERISTICS

V_P = 18 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified

Supply voltage	V_P	typ.	18	V
			15 to 35	V
Total quiescent current	I_{tot}	typ.	35	mA
Ripple rejection at f = 100 Hz; R_S = 0	RR	>	40	dB
Signal-to-noise ratio (d.c. control at minimum gain) see also note	S/N	>	60	dB
Total sensitivity (d.c. control at maximum gain) for P_o = 2,5 W	V_i	typ.	55	mV
Audio amplifier				
Repetitive peak output current	I_{ORM}	<	1,5	A
Output power at d_{tot} = 10%	P_o	>	4	W
		typ.	4,5	W
Total harmonic distortion at P_o = 2,5 W	d_{tot}	typ.	0,5	%
Voltage gain	G_v	typ.	30	dB
Sensitivity for P_o = 2,5 W	V_i	typ.	125	mV
Input impedance (pin 5)	$\lvert Z_i \rvert$	typ.	200	kΩ
			100 to 500	kΩ
Frequency response	f	>	15	kHz

Note

Measured in a bandwidth according to IEC-curve 'A', related to P_o = 2,5 W; R_S = 5 kΩ.

CHARACTERISTICS (continued)

D.C. volume control unit

Gain control range (see also Fig. 3)	ϕ	>	80 dB
Signal handling at d_{tot} < 1 % (d.c. control at 0 dB)	V_i	>	1,2 V
Sensitivity for V_o = 125 mV at max. voltage gain	V_i	typ.	55 mV
Input impedance (pin 9)	$\|Z_i\|$	typ. 100 to	200 kΩ 500 kΩ
Output impedance (pin 7)	$\|Z_o\|$	typ.	1 kΩ

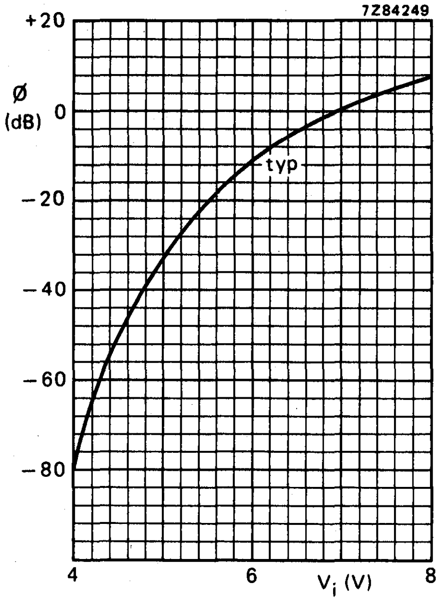


Fig. 3 Gain control curve; V_i at pin 8.

SIGNAL-SOURCES SWITCH

The TDA1028 is a quadruple operational amplifier connected as an impedance converter. Each amplifier has 2 switchable inputs which are protected by clamping diodes. The input currents are independent of the switch position and the outputs are short-circuit protected.

The device is intended as an electronic four-channel signal-sources switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 9)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 9)	V_P	typ.	20	V
Current consumption (pins 4, 5, 12, 13 unloaded)	I_9	typ.	2,9	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

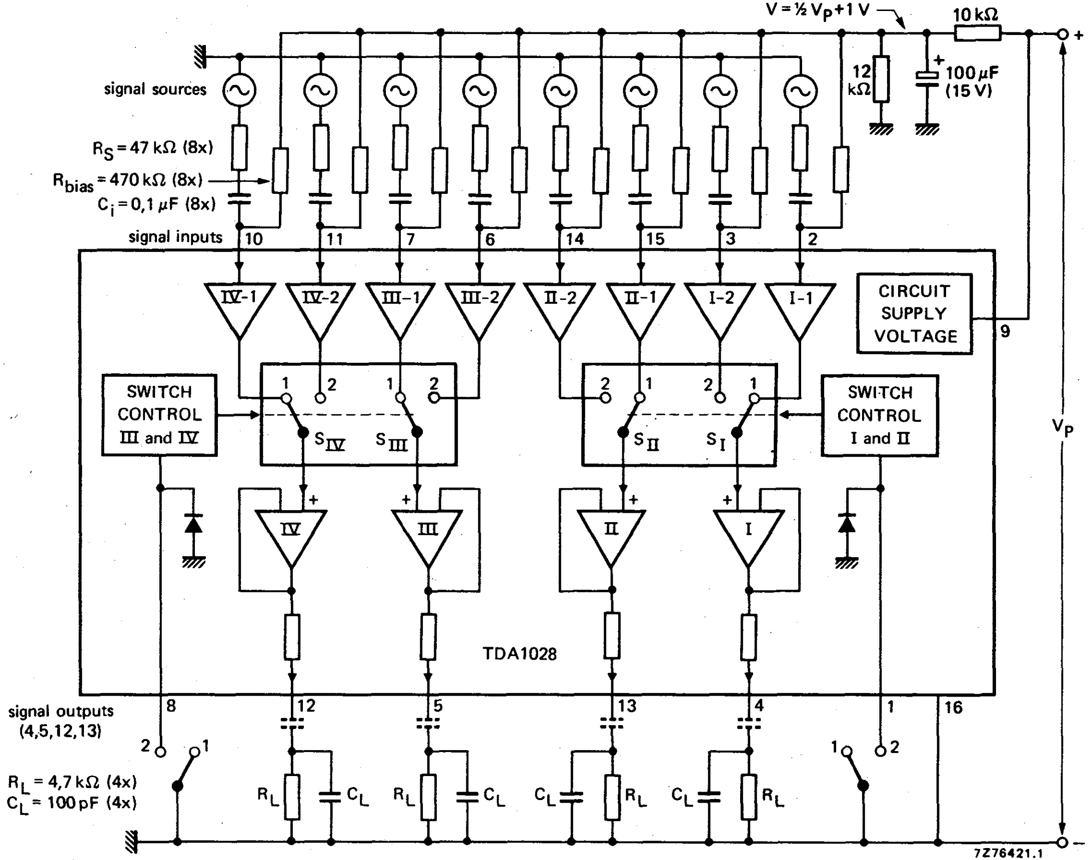


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 9)	V_P	max.	23	V
Input voltages (pins 2, 3, 6, 7, 10, 11, 14, 15)	V_I	max.	V_P	
	$-V_I$	max.	0,5	V
Switch control voltage (pin 1 and 8)	V_S		0 to 23	V
Input current	$\pm I_I$	max.	20	mA
Switch control current	$-I_S$	max.	50	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

$V_P = 20$ V; $T_{amb} = 25$ °C; unless otherwise specified

Current consumption without load; $I_{4;\,5;\,12;\,13} = 0$	I_9	typ.	2,9	mA
			1,6 to 4,2	mA
Supply voltage range	V_P		6 to 23	V
Signal inputs				
Input offset voltage of switched-on inputs ($R_S < 1$ kΩ)	V_{io}	typ.	2	mV
		<	10	mV
Input offset current of switched-on inputs	I_{io}	typ.	20	nA
		<	200	nA
Input offset current of a switched-on input with respect to a non-switched-on input	I_{io}	typ.	20	nA
		<	200	nA
Input bias current independent of switch position	I_i	typ.	250	nA
		<	950	nA
Capacitance between adjacent inputs	C	typ.	0,5	pF
D.C. input voltage range	V_I		3 to 19	V
Supply voltage rejection ratio; $R_S < 10$ kΩ	SVRR	typ.	100	μV/V
Equivalent input noise voltage $R_S \leqslant 1$ kΩ; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5	μV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05	nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $R_S < 1$ kΩ; f = 1 kHz	α	typ.	100	dB
Signal amplifier				
Voltage gain of a switched-on input at $I_{4;\,5;\,12;\,13} = 0$; $R_L = \infty$	G_v	typ.	1	
Current gain of a switched-on amplifier	G_i	typ.	10^5	

CHARACTERISTICS (continued)

Signal outputs

Output resistance	R_o	typ.	400 Ω
Output current capability (pins 4, 5, 12 and 13)	$\pm I_o$	>	5 mA
Frequency limit of the output voltage at $V_{i(p-p)} = 1$ V; $R_S < 1$ kΩ; $R_L = 10$ MΩ; $C_L = 10$ pF	f	typ.	1,3 MHz
Slew rate (unity gain) $\Delta V_{4;\,5;\,12;\,13\text{-}16}/\Delta t$ at $R_L = 10$ MΩ; $C_L = 10$ pF	S	typ.	2 V/μs

Switch control

switched-on inputs	interconnected pins	control voltages	
		$V_{1\text{-}16}$	$V_{8\text{-}16}$
I-1, II-1	2-4, 15-13	H	–
I-2, II-2	3-4, 14-13	L	–
III-1, IV-1	7-5, 10-12	–	H
III-2, IV-2	6-5, 11-12	–	L

Control inputs (pins 1 and 8)

Required voltage			
HIGH	V_{SH}	>	3,3 V *
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	200 μA

* Or control inputs open; $R_{1\text{-}16}$, $R_{8\text{-}16} > 33$ MΩ.

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5	dB
D.C. *output voltage variation when* switching the inputs (pins 4, 5, 12 and 13)	ΔV_o	typ. <	10 100	mV mV
Total harmonic distortion over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01	%
at V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02	%
at V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03	%
Output signal handling d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	> typ.	5,0 5,3	V V
Noise output voltage (unweighted) f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5	μV
Noise output voltage (weighted) f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12	μV
Amplitude response (pins 4, 5, 12 and 13) V_i = 5 V; f = 20 Hz to 20 kHz	ΔV_o	typ.	0,1	dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75	dB **
Crosstalk between switched-on inputs and the outputs of the other channels; at f = 1 kHz	α	typ.	90	dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

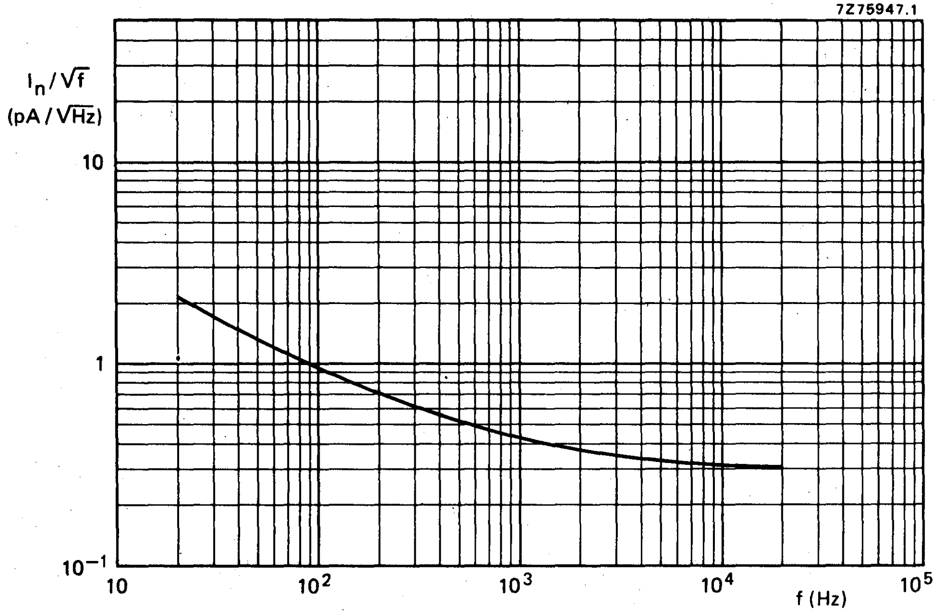


Fig. 2 Equivalent input noise current.

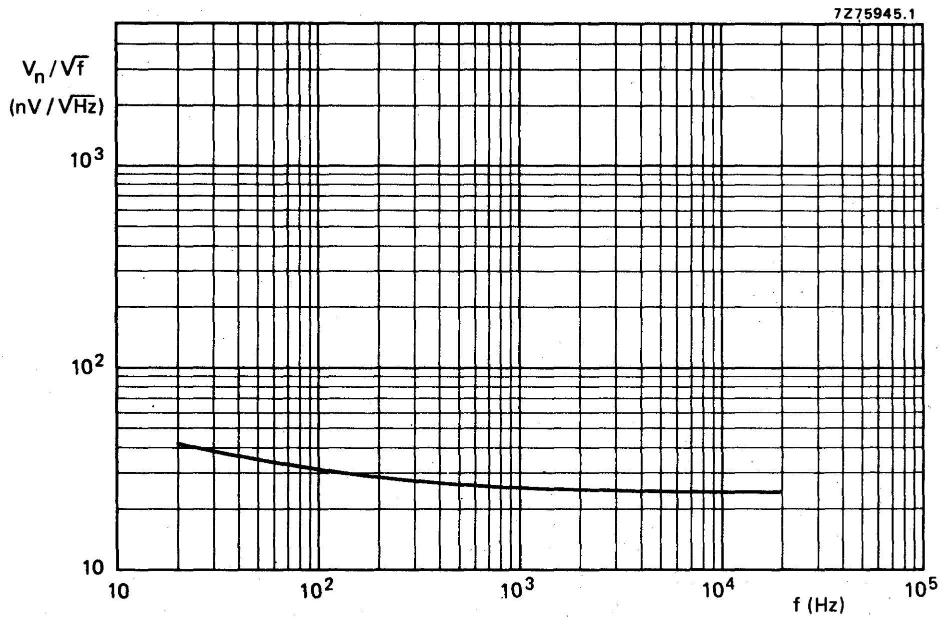


Fig. 3 Equivalent input noise voltage.

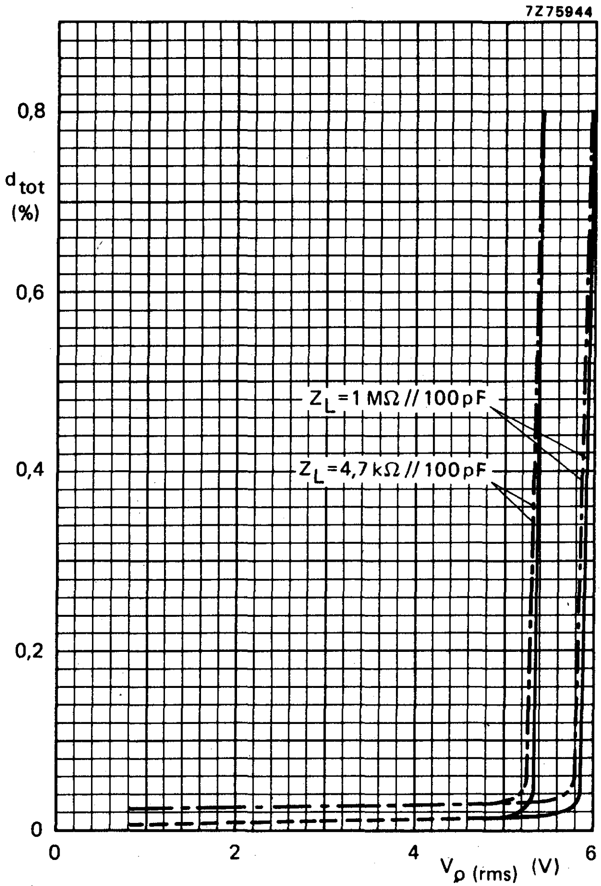


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — - — - f = 20 kHz.

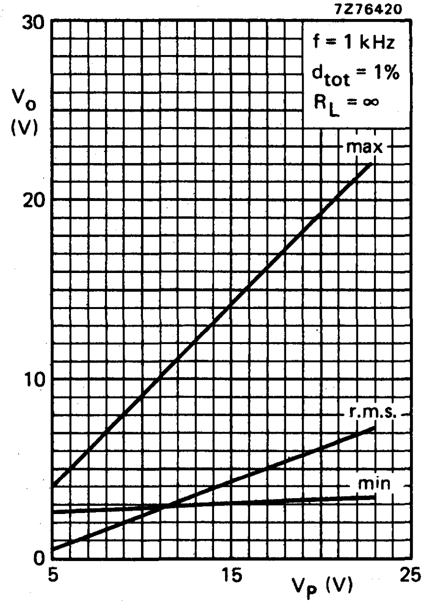


Fig. 5 Output voltage as a function of supply voltage.

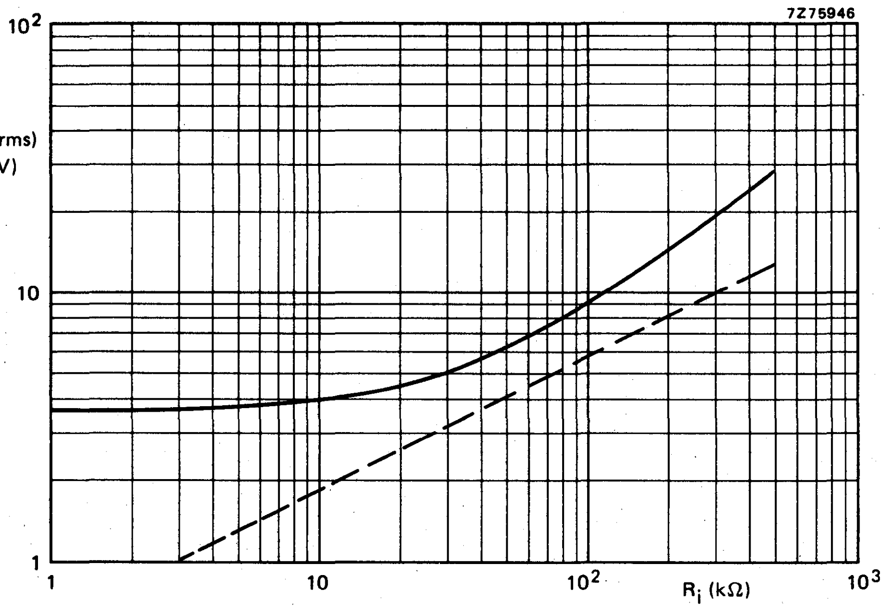


Fig. 6 Noise output voltage as a function of input resistance; $G_V = 1$; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

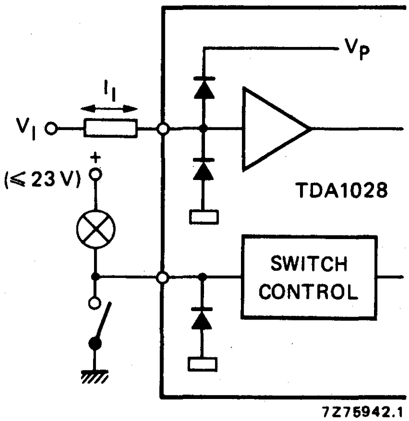


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range.

Circuits with standby operation

The control inputs (pins 1 and 8) are high-ohmic at $V_{SH} \leq 20$ V ($I_{SH} \leq 1$ μA), as well as, when the supply voltage (pin 9) is switched off.

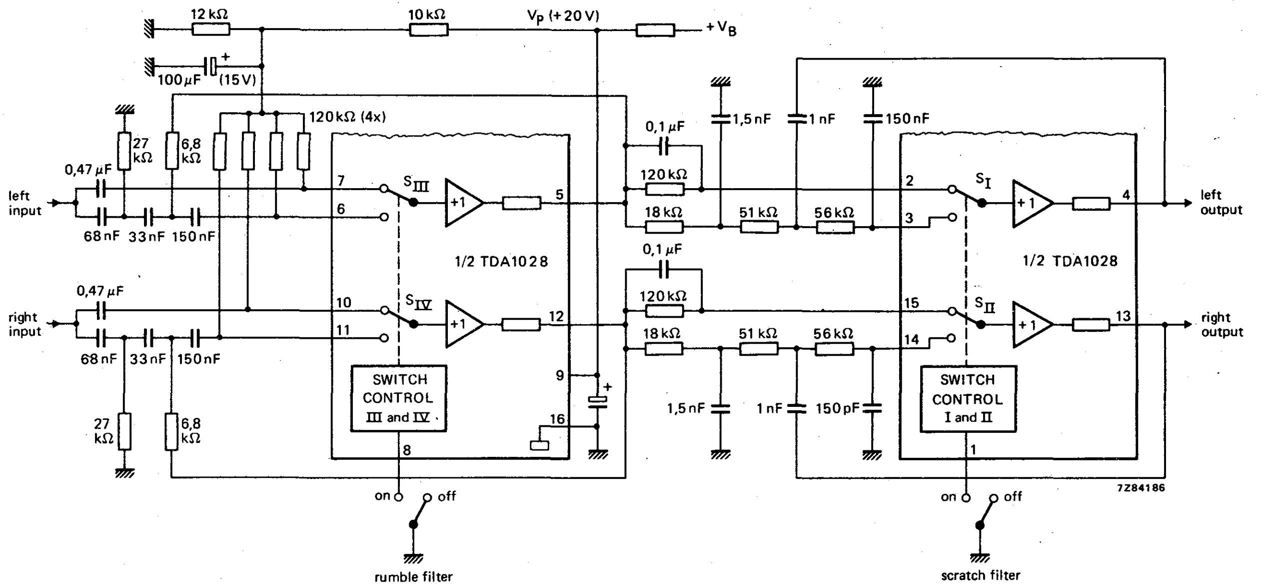


Fig. 8 Typical application diagram for a switchable scratch/rumble filter.

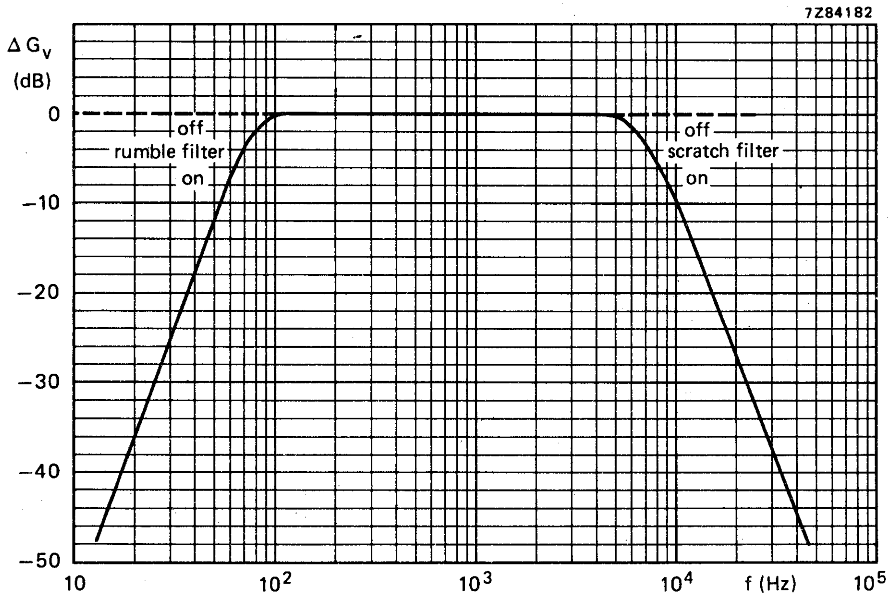


Fig. 9 Frequency response curves for scratch/rumble filters in Fig. 8.

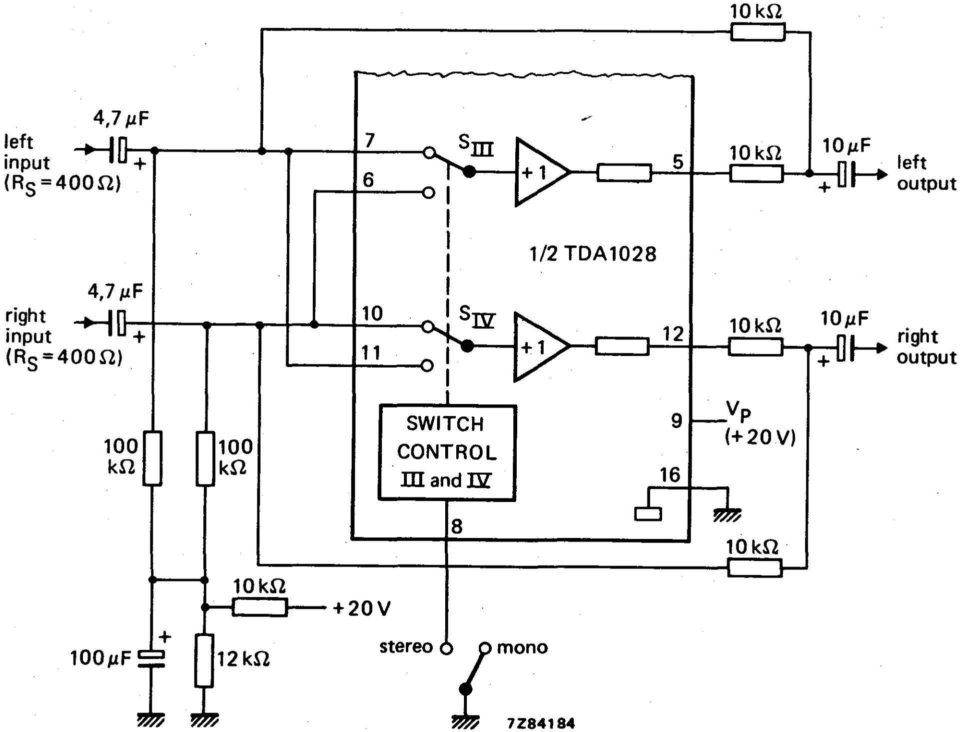


Fig. 10 Half of TDA1028 used as a mono/stereo switch.

SIGNAL-SOURCES SWITCH

The TDA1029 is a dual operational amplifier (connected as an impedance converter) each amplifier having 4 mutually switchable inputs which are protected by clamping diodes. The input currents are independent of switch position and the outputs are short-circuit protected.

The device is intended as an electronic two-channel signal-source switch in a.f. amplifiers.

QUICK REFERENCE DATA

Supply voltage range (pin 14)	V_P		6 to 23	V
Operating ambient temperature	T_{amb}		−30 to + 80	°C
Supply voltage (pin 14)	V_P	typ.	20	V
Current consumption	I_{14}	typ.	3,5	mA
Maximum input signal handling (r.m.s. value)	$V_{i(rms)}$	typ.	6	V
Voltage gain	G_v	typ.	1	
Total harmonic distortion	d_{tot}	typ.	0,01	%
Crosstalk	α	typ.	70	dB
Signal-to-noise ratio	S/N	typ.	120	dB

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

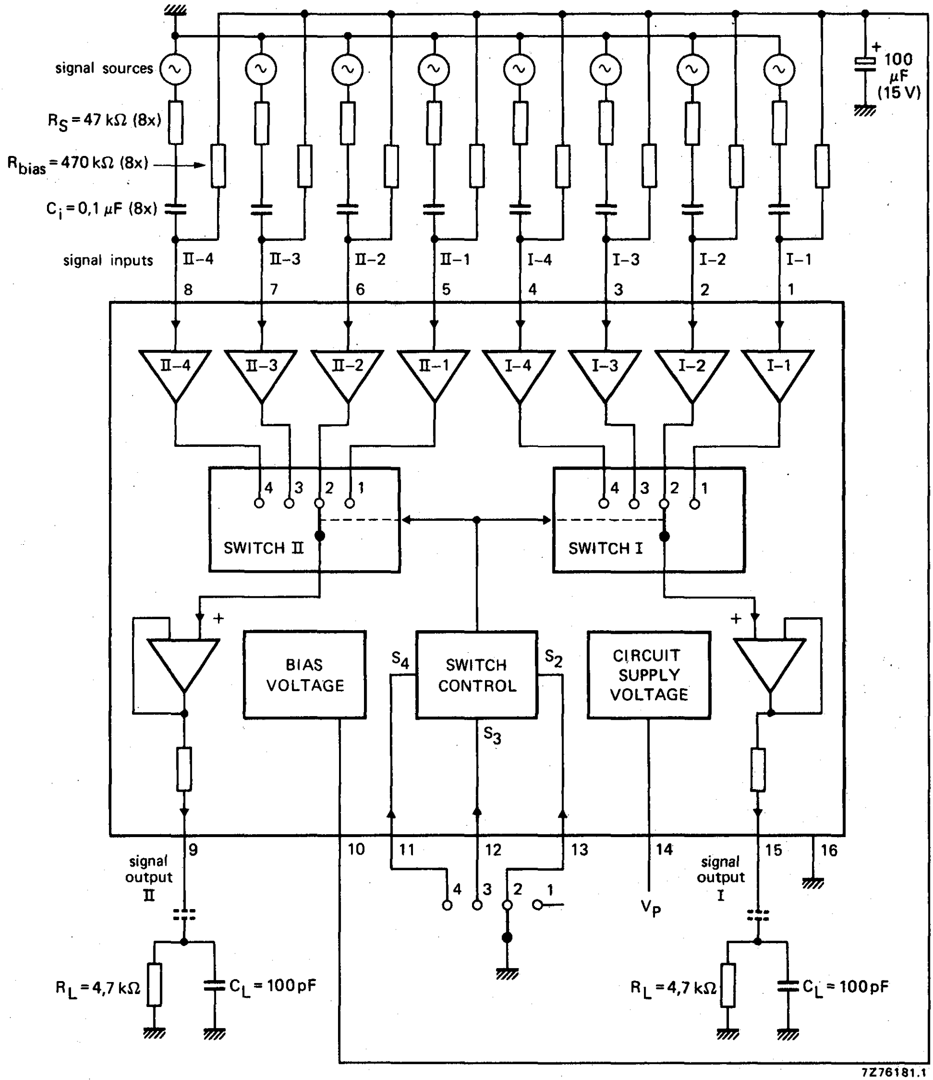


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 14)	V_P	max.	23 V
Input voltage (pins 1 to 8)	V_I	max.	V_P
	$-V_I$	max.	0,5 V
Switch control voltage (pins 11, 12 and 13)	V_S		0 to 23 V
Input current	$\pm I_I$	max.	20 mA
Switch control current	$-I_S$	max.	50 mA
Total power dissipation	P_{tot}	max.	800 mW
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature	T_{amb}		−30 to + 80 °C

CHARACTERISTICS

$V_P = 20$ V; $T_{amb} = 25$ °C; unless otherwise specified

Current consumption without load; $I_9 = I_{15} = 0$	I_{14}	typ.	3,5 mA
			2 to 5 mA
Supply voltage range (pin 14)	V_P		6 to 23 V

Signal inputs

Input offset voltage of switched-on inputs $R_S \leqslant 1$ kΩ	V_{io}	typ.	2 mV
		<	10 mV
Input offset current of switched-on inputs	I_{io}	typ.	20 nA
		<	200 nA
Input offset current of a switched-on input with respect to a non-switched-on input of a channel	I_{io}	typ.	20 nA
		<	200 nA
Input bias current independent of switch position	I_i	typ.	250 nA
		<	950 nA
Capacitance between adjacent inputs	C	typ.	0,5 pF
D.C. input voltage range	V_I		3 to 19 V
Supply voltage rejection ratio; $R_S \leqslant 10$ kΩ	SVRR	typ.	100 μV/V
Equivalent input noise voltage $R_S \doteq 0$; f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	3,5 μV
Equivalent input noise current f = 20 Hz to 20 kHz (r.m.s. value)	$I_{n(rms)}$	typ.	0,05 nA
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at $R_S = 1$ kΩ; f = 1 kHz	α	typ.	100 dB

CHARACTERISTICS (continued)

Signal amplifier

Voltage gain of a switched-on input at $I_9 = I_{15} = 0$; $R_L = \infty$	G_v	typ.	1
Current gain of a switched-on amplifier	G_i	typ.	10^5

Signal outputs

Output resistance (pins 9 and 15)	R_o	typ.	400 Ω
Output current capability at V_P = 6 to 23 V	$\pm I_9$; $\pm I_{15}$	typ.	5 mA
Frequency limit of the output voltage $V_{i(p-p)}$ = 1 V; R_S = 1 kΩ; R_L = 10 MΩ; C_L = 10 pF	f	typ.	1,3 MHz
Slew rate (unity gain); $\Delta V_{9-16}/\Delta t$; $\Delta V_{15-16}/\Delta t$ R_L = 10 MΩ; C_L = 10 pF	S	typ.	2 V/μs

Bias voltage

D.C. output voltage	V_{10-16}	typ.	11 V *
			10,2 to 11,8 V
Output resistance	R_{10-16}	typ.	8,2 kΩ

Switch control

switched-on inputs	interconnected pins	control voltages V_{11-16}	control voltages V_{12-16}	control voltages V_{13-16}
I-1, II-1	1-15, 5-9	H	H	H
I-2, II-2	2-15, 6-9	H	H	L
I-3, II-3	3-15, 7-9	H	L	H
I-4, II-4	4-15, 8-9	L	H	H
I-4, II-4	4-15, 8-9	L	L	H
I-4, II-4	4-15, 8-9	L	H	L
I-4, II-4	4-15, 8-9	L	L	L
I-3, II-3	3-15, 7-9	H	L	L

In the case of offset control, an internal blocking circuit of the switch control ensures that not more than one input will be switched on at a time. In that case safe switching-through is obtained at $V_{SL} \leqslant 1,5$ V.

Control inputs (pins 11, 12 and 13)

Required voltage			
HIGH	V_{SH}	>	3,3 V **
LOW	V_{SL}	<	2,1 V
Input current			
HIGH (leakage current)	I_{SH}	<	1 μA
LOW (control current)	$-I_{SL}$	<	250 μA

* V_{10-16} is typically $0,5 \cdot V_{14-16} + 1,5 \cdot V_{BE}$.
** Or control inputs open ($R_{11,12,13-16} > 33$ MΩ).

APPLICATION INFORMATION

V_P = 20 V; T_{amb} = 25 °C; measured in Fig. 1; R_S = 47 kΩ; C_i = 0,1 μF; R_{bias} = 470 kΩ; R_L = 4,7 kΩ; C_L = 100 pF (unless otherwise specified)

Voltage gain	G_v	typ.	−1,5	dB
Output voltage variation when switching the inputs	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	typ.	10	mV
		<	100	mV
Total harmonic distortion				
over most of signal range (see Fig. 4)	d_{tot}	typ.	0,01	%
V_i = 5 V; f = 1 kHz	d_{tot}	typ.	0,02	%
V_i = 5 V; f = 20 Hz to 20 kHz	d_{tot}	typ.	0,03	%
Output signal handling d_{tot} = 0,1%; f = 1 kHz (r.m.s. value)	$V_{o(rms)}$	>	5,0	V
		typ.	5,3	V
Noise output voltage (unweighted) f = 20 Hz to 20 kHz (r.m.s. value)	$V_{n(rms)}$	typ.	5	μV
Noise output voltage (weighted) f = 20 Hz to 20 kHz (in accordance with DIN 45405)	V_n	typ.	12	μV
Amplitude response V_i = 5 V; f = 20 Hz to 20 kHz; C_i = 0,22 μF	$\Delta V_{9\text{-}16}$; $\Delta V_{15\text{-}16}$	<	0,1	dB *
Crosstalk between a switched-on input and a non-switched-on input; measured at the output at f = 1 kHz	α	typ.	75	dB **
Crosstalk between switched-on inputs and the outputs of the other channels	α	typ.	90	dB **

* The lower cut-off frequency depends on values of R_{bias} and C_i.

** Depends on external circuitry and R_S. The value will be fixed mostly by capacitive crosstalk of the external components.

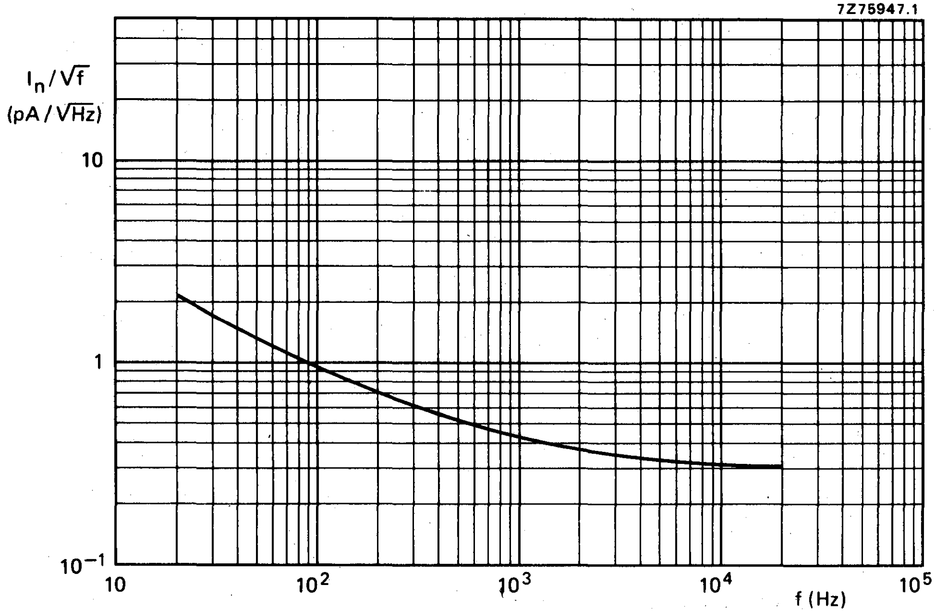


Fig. 2 Equivalent input noise current.

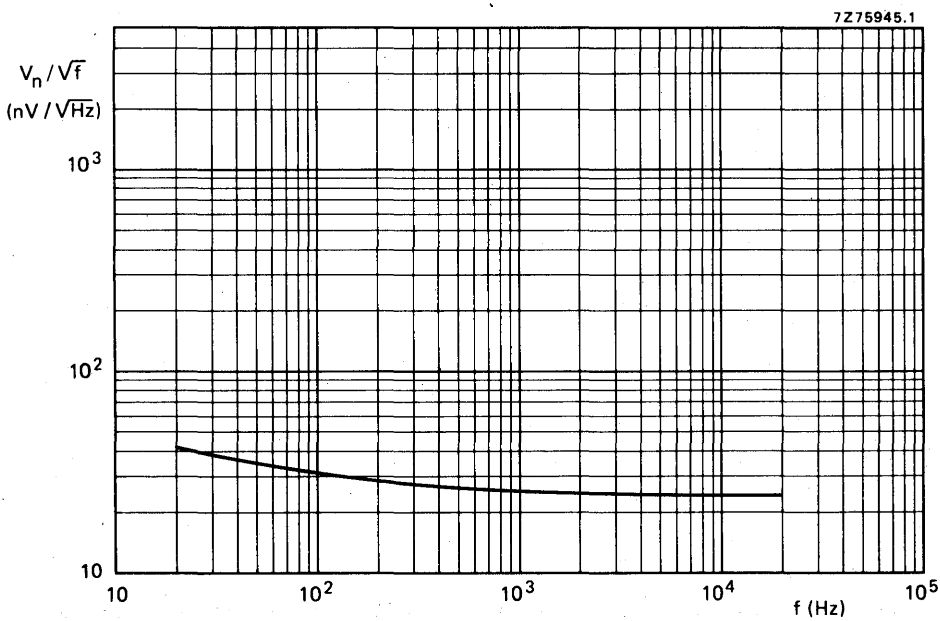


Fig. 3 Equivalent input noise voltage.

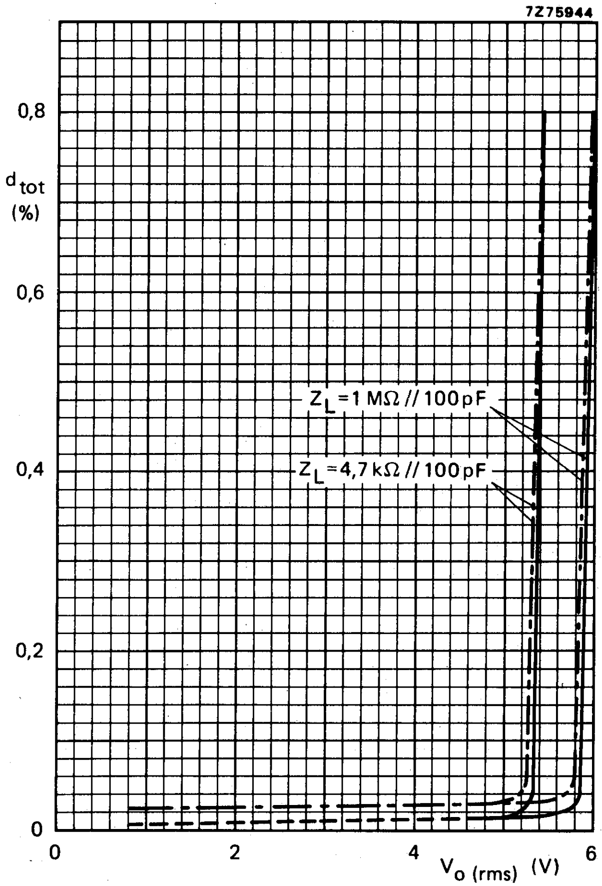


Fig. 4 Total harmonic distortion as a function of r.m.s. output voltage.
—— f = 1 kHz; — · — · f = 20 kHz.

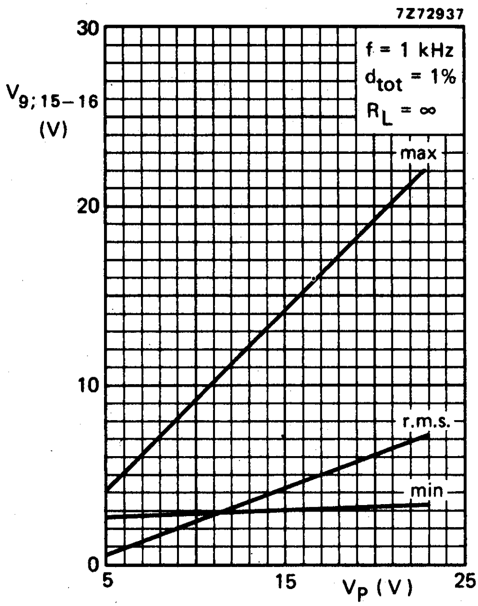


Fig. 5 Output voltage as a function of supply voltage.

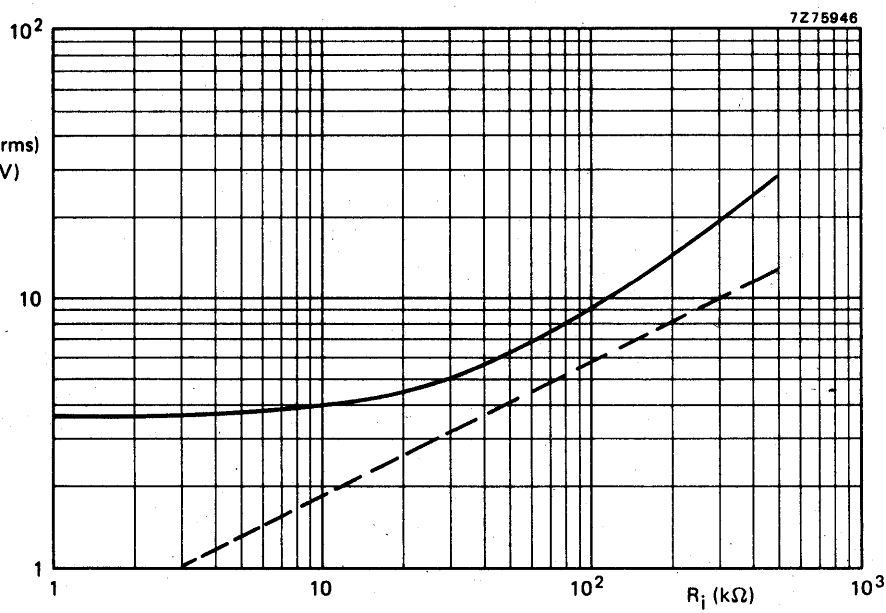


Fig. 6 Noise output voltage as a function of input resistance; $G_v = 1$; f = 20 Hz to 20 kHz.
—— V_n (output); – – – V_n (R_S).

APPLICATION NOTES

Input protection circuit and indication

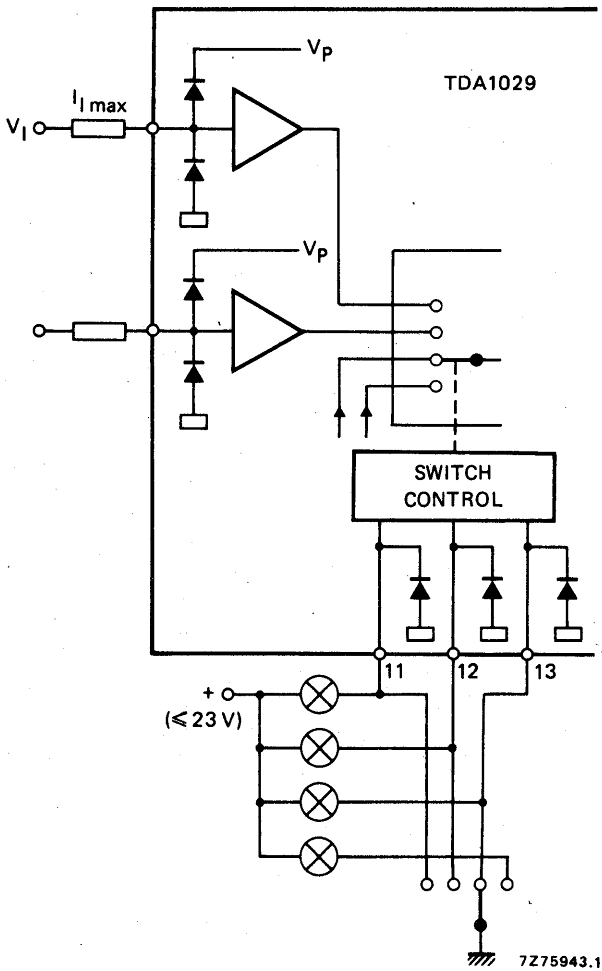


Fig. 7 Circuit diagram showing input protection and indication.

Unused signal inputs

Any unused inputs must be connected to a d.c. (bias) voltage, which is within the d.c. input voltage range; e.g. unused inputs can be connected directly to pin 10.

Circuits with standby operation

The control inputs (pins 11, 12 and 13) are high-ohmic at $V_{SH} \leq 20$ V ($I_{SH} \leq 1\ \mu A$), as well as, when the supply voltage (pin 14) is switched off.

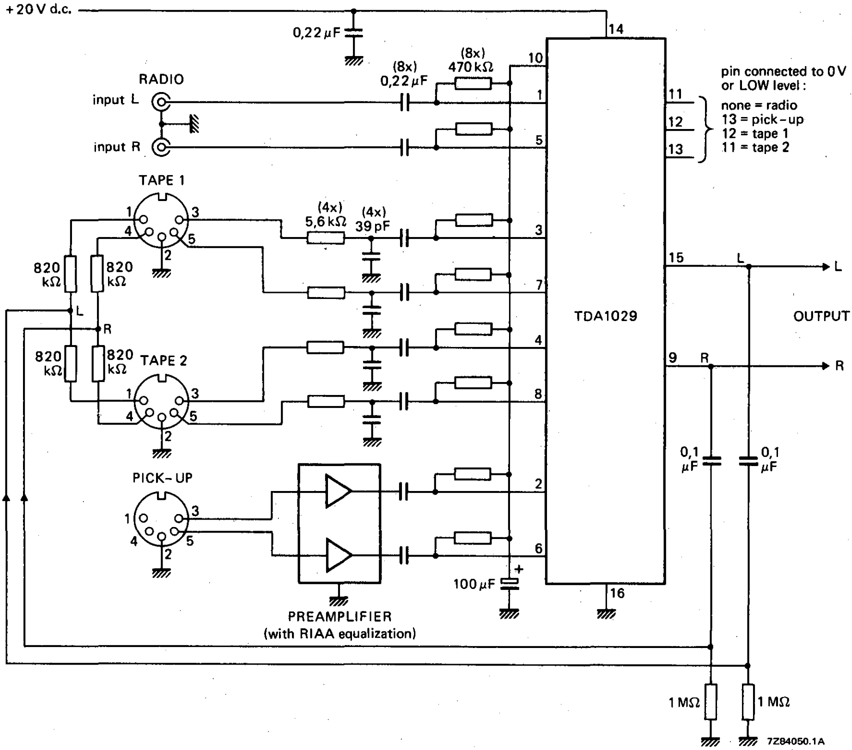


Fig. 8 TDA1029 connected as a four input stereo source selector.

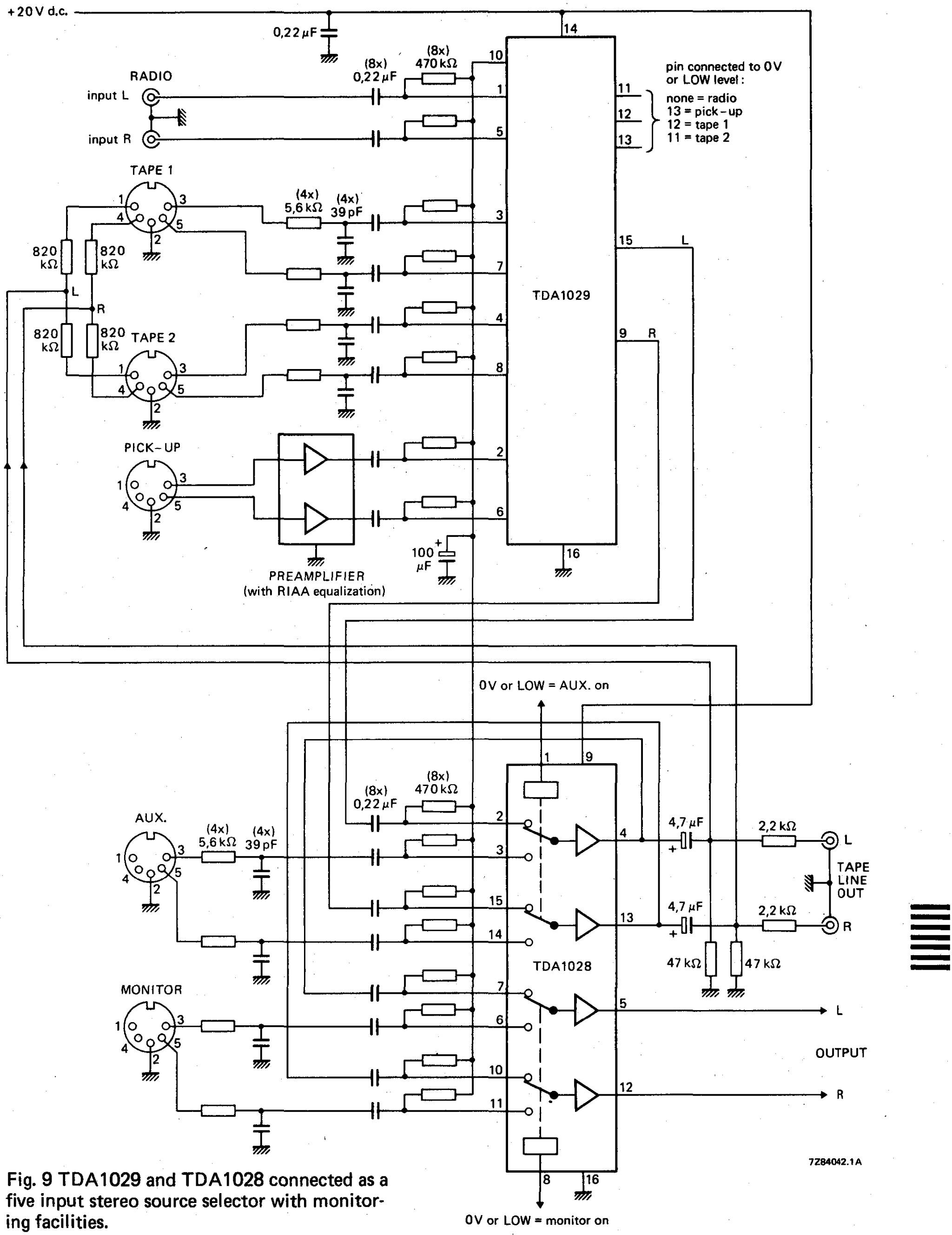


Fig. 9 TDA1029 and TDA1028 connected as a five input stereo source selector with monitoring facilities.

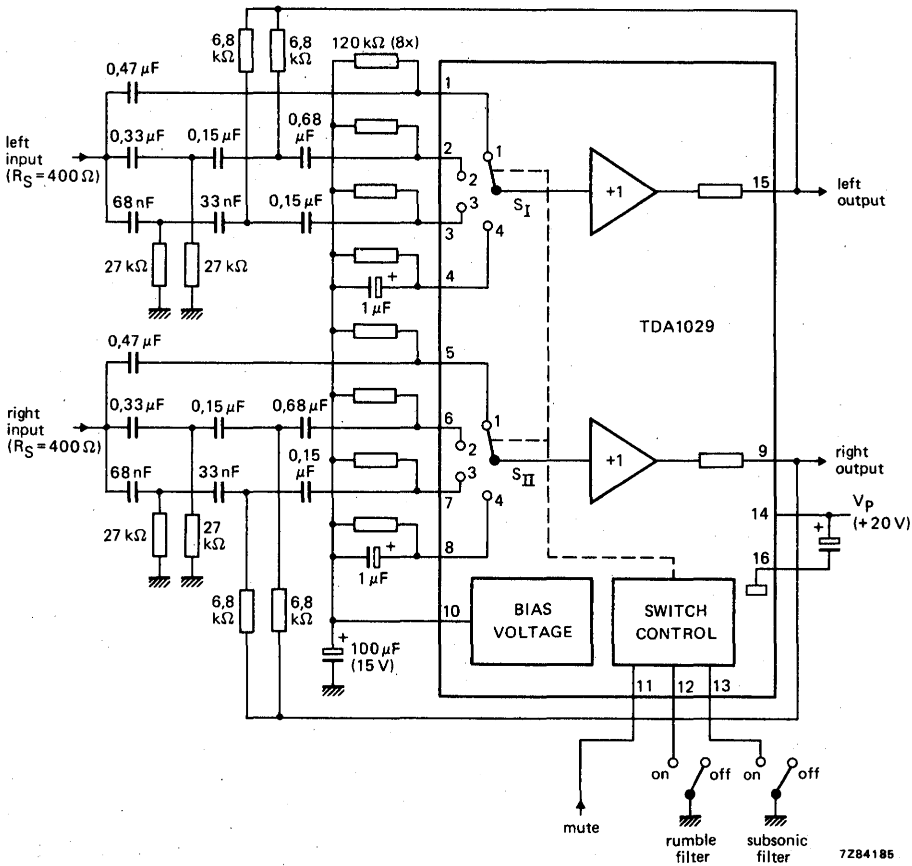


Fig. 10 TDA1029 connected as a third-order active high-pass filter with Butterworth response and component values chosen according to the method proposed by Fjällbrant. It is a four-function circuit which can select mute, rumble filter, subsonic filter and linear response.

Switch control

function	$V_{11\text{-}16}$	$V_{12\text{-}16}$	$V_{13\text{-}16}$
linear	H	H	H
subsonic filter 'on'	H	H	L
rumble filter 'on'	H	L	X
mute 'on'	L	X	X

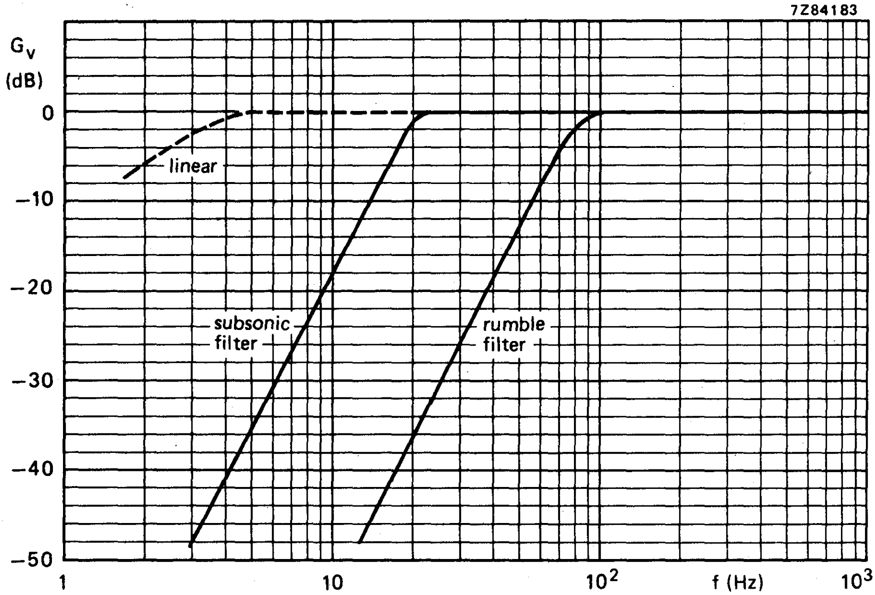


Fig. 11 Frequency response curves for the circuit of Fig. 10.

MOTOR SPEED REGULATOR WITH THERMAL SHUT-DOWN

The TDA1059B is a monolithic integrated circuit with a current limiter and with good thermal characteristics in a TO-126 plastic package for easy mounting. It is intended to regulate the speed of d.c. motors in record players, cassette recorders and car cassette recorders.

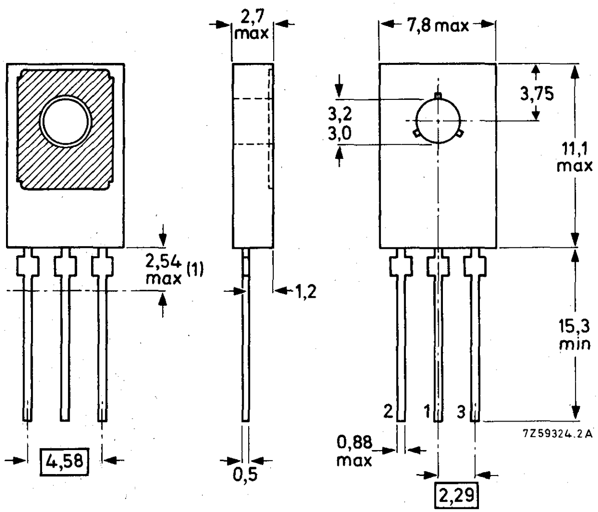
QUICK REFERENCE DATA

Supply voltage	$V_P = V_{2\text{-}1}$	typ.	9 V
			3,3 to 16 V
Internal reference voltage	V_{ref}	typ.	1,3 V
Drop-out voltage	$V_{3\text{-}1}$	typ.	1,8 V
Limited output current	I_{3lim}	typ.	0,6 A
Multiplication coefficient	k	typ.	9

PACKAGE OUTLINE

Dimensions in mm

Fig. 1 TO-126 (SOT-32).
Pin 1 connected to metal part of mounting surface.



(1) Within this region the cross-section of the leads is uncontrolled.

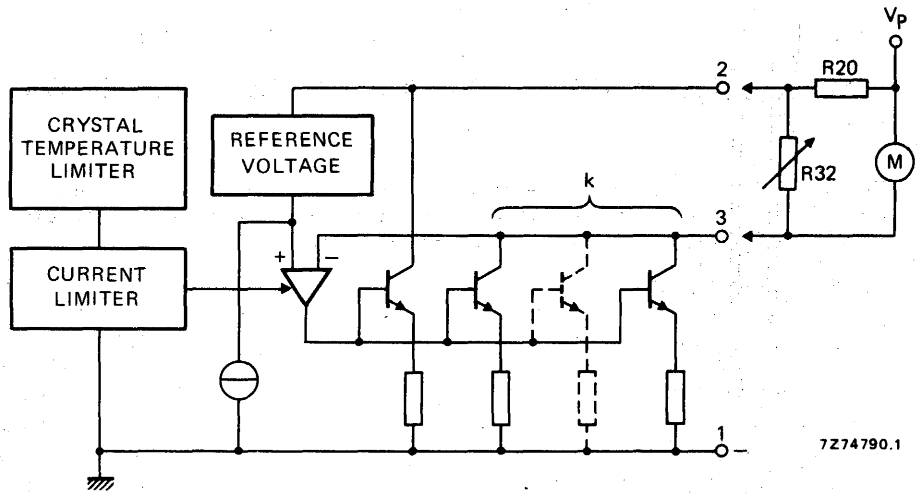


Fig. 2 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{2\text{-}1}$	max.	16 V
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature (see Fig. 3 and note)	T_{amb}		−25 to + 130 °C

THERMAL RESISTANCE

From junction to case	$R_{th\ j\text{-}c}$	=	10 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	100 K/W

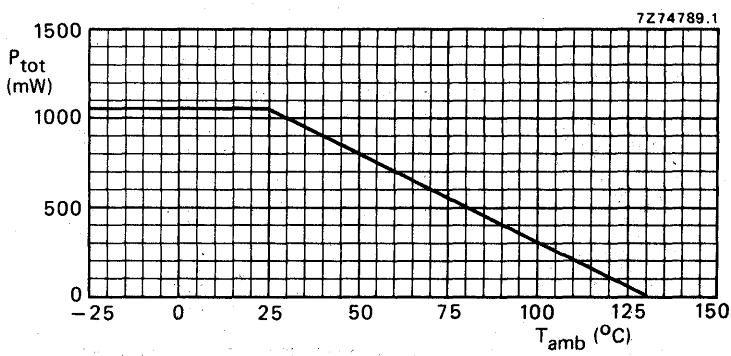


Fig. 3 Power derating curve.

Note

At ambient temperatures above 130 °C, the crystal temperature limiter decreases the internal power consumption.

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; R20 = 0; heatsink with R_{th} = 100 K/W and after thermal stabilization; unless otherwise specified; see test circuit Fig. 4.

		min.	typ.	max.	
Supply voltage	$V_P = V_{2\text{-}1}$	3,3	9	16	V
Internal reference voltage V_P = 3,3 V; I_3 = 80 mA	V_{ref}	1,24	1,3	1,36	V
Drop-out voltage I_3 = 80 mA; ΔV_{ref} = 5%	$V_{3\text{-}1}$	–	1,8	2,06	V
Quiescent current; I_3 = 0	I_q	1,8	2,3	2,8	mA
Limited output current*	I_{3lim}	0,3	0,6	1	A
Multiplication coefficient I_3 = 50 mA ± 10 mA	$k = \frac{\Delta I_3}{\Delta I_2}$	8,5	9	9,5	
Line regulation V_P = 3,3 to 16 V at I_3 = 50 mA					
reference voltage variation	$\frac{\Delta V_{ref}}{V_{ref}} / \Delta V_P$	–0,115	0	+0,115	%/V
multiplication coefficient variation I_3 = 50 ± 10 mA	$\frac{\Delta k}{k} / \Delta V_P$	–	0,86	–	%/V
input current variation; I_3 = 50 mA	$\frac{\Delta I_2}{\Delta V_P}$	–15	0	+ 15	µA/V
Load regulation					
reference voltage variation I_3 = 20 to 80 mA	$\frac{\Delta V_{ref}}{V_{ref}} / \Delta I_3$	0	19	38,5	%/A
multiplication coefficient variation I_3 = 30 ± 10 to 70 ± 10 mA	$\frac{\Delta k}{k} / \Delta I_3$	–0,075	0	+0,075	%/mA
Temperature coefficient I_3 = 50 mA; T_{amb} = –15 to + 65 °C					
reference voltage variation	$\frac{\Delta V_{ref}}{V_{ref}} / \Delta T_{amb}$	–0,03	0	+0,03	%/K
multiplication coefficient variation ΔI_3 = ± 10 mA	$\frac{\Delta k}{k} / \Delta T_{amb}$	–	0,008	–	%/K
input current variation	$\frac{\Delta I_2}{\Delta T_{amb}}$	–2	0	+2	µA/K

* If the motor is stopped by a mechanical brake, the current limitation is effective in the supply voltage range. If the motor is short-circuited, the TDA1059B will be damaged if the supply voltage is higher than 10 V due to parasitic oscillations.

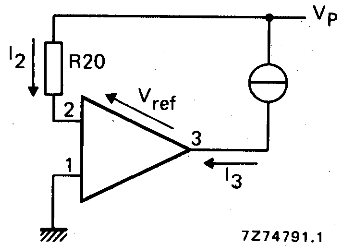
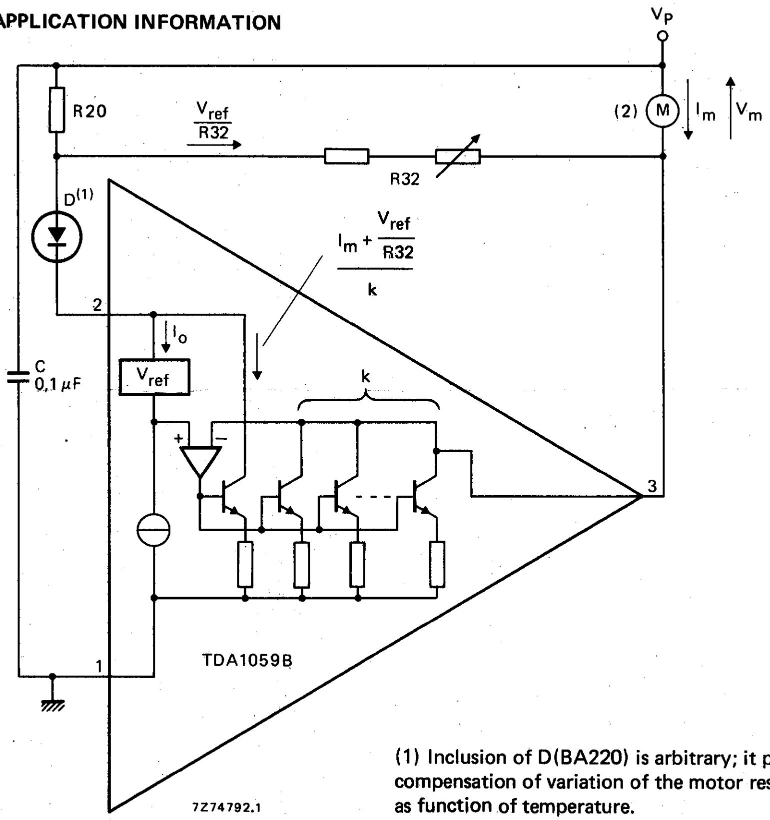


Fig. 4 Test circuit.

Note

For start operation: V_{ref} must start with final V_P = 6,7 V and a time constant of 3τ = 100 ms in which τ = R.C; R = source impedance, C = by-pass capacitor.

APPLICATION INFORMATION



(1) Inclusion of D(BA220) is arbitrary; it permits compensation of variation of the motor resistance as function of temperature.

(2) Motor example (without diode D):

Catalogue no. 9904 120 01806; n = 2000 rev/min; R20 = 180 Ω (± 2%); R32 = 100 Ω + 100 Ω (variable).

Fig. 5 Example of using the TDA1059B in a d.c. motor speed regulation circuit.

Motor equations

$E_m = \alpha_1 n$

$I_m = \alpha_2 r$

$V_m = E_m + R_m I_m$

where: α_1, α_2 = motor constant
n = number of revolutions
r = motor torque
E_m = back electromotive force
R_m = motor resistance

The back electromotive force (E_m) in Fig. 5 can be expressed (excluding diode D) as:

$$E_m = \left(\frac{R20}{k} - R_m \right) I_m + V_{ref} \left\{ 1 + \frac{R20}{R32} \left(1 + \frac{1}{k} \right) \right\} + R20.I_o$$

and including diode D, as:

$$E_m = \left(\frac{R20}{k} - R_m \right) I_m + \left(V_{ref} + V_D \right) \left\{ 1 + \frac{R20}{R32} \left(1 + \frac{1}{k} \right) \right\} + R20.I_o$$

Speed regulation is constant when E_m is independent of I_m variations; this will be obtained when $R20 = kR_m$.

E_m, and therefore the motor speed, is regulated by R32. A practical condition for stability is $R20 < kR_m$.

MOTOR SPEED REGULATOR

The TDA1059C is a monolithic integrated circuit with a current limiter and with good thermal characteristics in a TO-126 plastic package for easy mounting. It is intended to regulate the speed of d.c. motors in record players, cassette recorders and car cassette recorders.

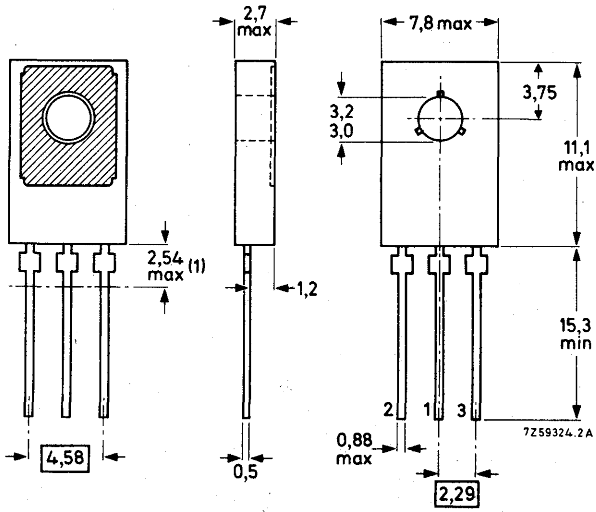
QUICK REFERENCE DATA

Suppy voltage	$V_P = V_{2\text{-}1}$	typ.	9	V
			2,5 to 15	V
Internal reference voltage	V_{ref}	typ.	1,1	V
Drop-out voltage	$V_{3\text{-}1}$	typ.	1,0	V
Limited output current	I_{3lim}	typ.	0,6	A
Multiplication coefficient	k	typ.	9	

PACKAGE OUTLINE

Dimensions in mm

Fig. 1 TO-126 (SOT-32).
Pin 1 connected to metal part of mounting surface.



(1) Within this region the cross-section of the leads is uncontrolled.

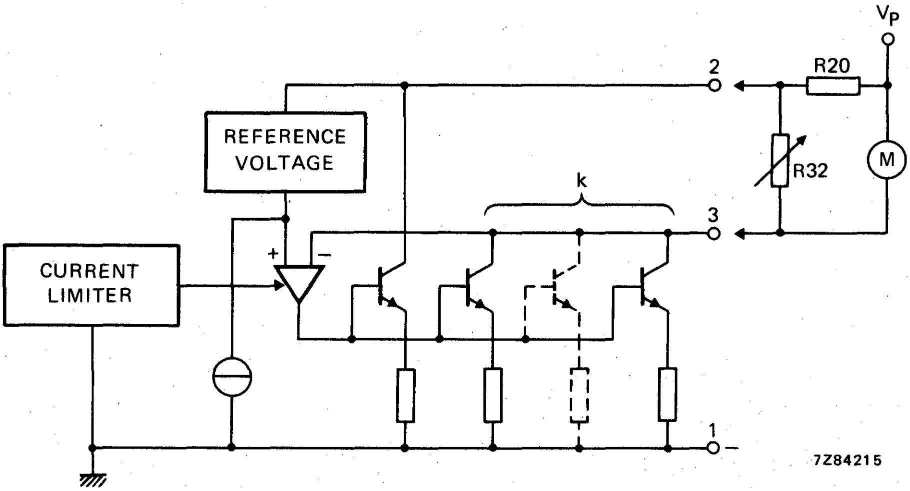


Fig. 2 Functional diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{2\text{-}1}$	max.	16 V
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature (see Fig. 3)	T_{amb}		−25 to + 150 °C

THERMAL RESISTANCE

From junction to case	$R_{th\ j\text{-}c}$	=	10 K/W
From junction to ambient	$R_{th\ j\text{-}a}$	=	100 K/W

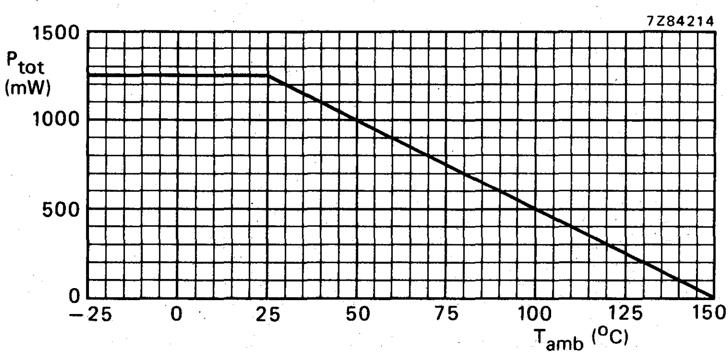


Fig. 3 Power derating curve.

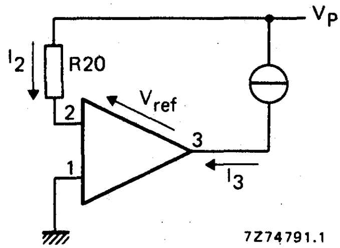
DEVELOPMENT SAMPLE DATA

CHARACTERISTICS

V_P = 9 V; T_{amb} = 25 °C; R20 = 0; heatsink with R_{th} = 100 K/W and after thermal stabilization; unless otherwise specified; see test circuit Fig. 4

		min.	typ.	max.	
Supply voltage	$V_P = V_{2\text{-}1}$	2,5	9	15	V
Internal reference voltage V_P = 2,5 V; I_3 = 80 mA	V_{ref}	1,05	1,1	1,15	V
Drop-out voltage I_3 = 80 mA; ΔV_{ref} = 5%	$V_{3\text{-}1}$	–	1,0	1,45	V
Quiescent current; I_3 = 0	I_q	2,5	3	3,5	mA
Limited output current *	I_{3lim}	0,3	0,6	1	A
Multiplication coefficient I_3 = 50 mA ± 10 mA	$k = \frac{\Delta I_3}{\Delta I_2}$	8,5	9	9,5	
Line regulation V_P = 2,5 to 15 V at I_3 = 50 mA					
reference voltage variation	$\frac{\Delta V_{ref}}{V_{ref}}/\Delta V_P$	0,04	0,13	0,22	%/V
multiplication coefficient variation I_3 = 50 ± 10 mA	$\frac{\Delta k}{k}/\Delta V_P$	–	0,86	–	%/V
input current variation; I_3 = 50 mA	$\frac{\Delta I_2}{\Delta V_P}$	0	15	30	µA/V
Load regulation					
reference voltage variation I_3 = 20 to 80 mA	$\frac{\Delta V_{ref}}{V_{ref}}/\Delta I_3$	0	23	45,5	%/A
multiplifaction coefficient variation I_3 = 30 ± 10 to 70 ± 10 mA	$\frac{\Delta k}{k}/\Delta I_3$	–	0	–	%/mA
Temperature coefficient I_3 = 50 mA; T_{amb} = −15 to + 65 °C					
reference voltage variation	$\frac{\Delta V_{ref}}{V_{ref}}/\Delta T_{amb}$	−0,036	0	+0,036	%/K
multiplication coefficient variation ΔI_3 = ± 10 mA	$\frac{\Delta k}{k}/\Delta T_{amb}$	–	0,008	–	%/K
input current variation	$\frac{\Delta I_2}{\Delta T_{amb}}$	–	0	–	µA/K

* If the motor is stopped by a mechanical brake, the current limitation is effective in the supply voltage range. If the motor is short-circuited, the TDA1059C will be damaged if the supply voltage is higher than 10 V due to parasitic oscillations.

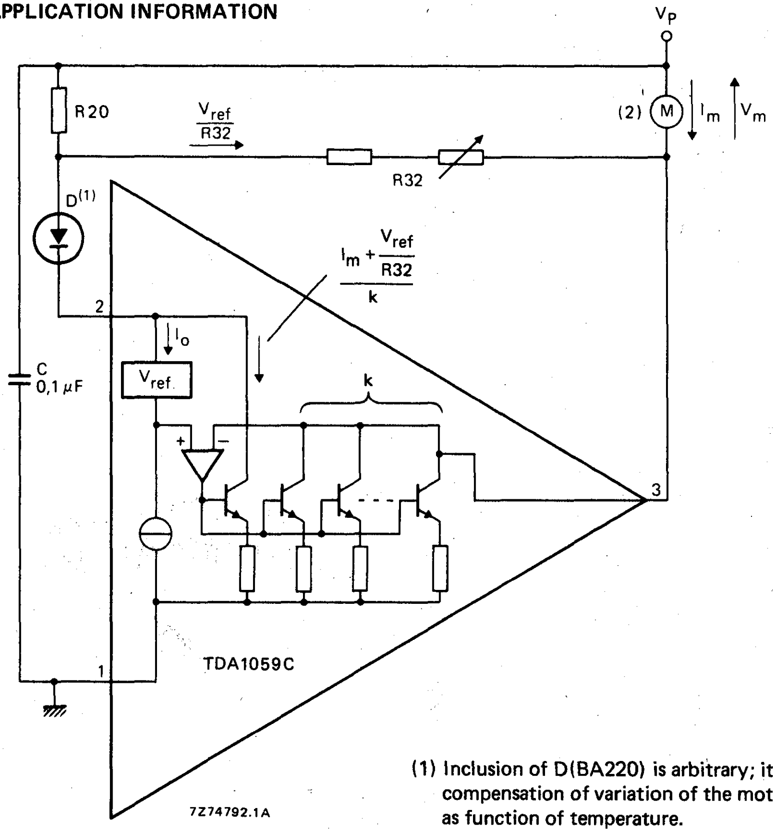


Note

For start operation: V_{ref} must start with final V_P = 6,7 V and a time constant of 3 τ = 100 ms in which τ = R.C.; R = source impedance, C = by-pass capacitor.

Fig. 4 Test circuit.

APPLICATION INFORMATION



(1) Inclusion of D(BA220) is arbitrary; it permits compensation of variation of the motor resistance as function of temperature.

(2) Motor example (without diode D):

Catalogue no. 9904 120 01806; n = 2000 rev/min; R20 = 180 Ω (± 2%); R32 = 39 Ω + 47 Ω (variable).

Fig. 5 Example of using the TDA1059C in a d.c. motor speed regulation circuit.

Motor equations

$E_m = \alpha_1 n$

$I_m = \alpha_2 r$

$V_m = E_m + R_m I_m$

where: α_1, α_2 = motor constant
n = number of revolutions
r = motor torque
E_m = back electromotive force
R_m = motor resistance

The back electromotive force (E_m) in Fig. 5 can be expressed (excluding diode D) as:

$$E_m = \left(\frac{R20}{k} - R_m\right) I_m + V_{ref}\left\{1 + \frac{R20}{R32}\left(1 + \frac{1}{k}\right)\right\} + R20.I_o$$

and including diode D, as:

$$E_m = \left(\frac{R20}{k} - R_m\right) I_m + \left(V_{ref} + V_D\right)\left\{1 + \frac{R20}{R32}\left(1 + \frac{1}{k}\right)\right\} + R20.I_o$$

Speed regulation is constant when E_m is independent of I_m variations; this will be obtained when $R20 = kR_m$.
E_m, and therefore the motor speed, is regulated by R32. A practical condition for stability is $R20 < kR_m$.

DEVELOPMENT SAMPLE DATA

AM RECEIVER CIRCUIT

The TDA1072 is a monolithic integrated AM receiver circuit provided with the following functions:

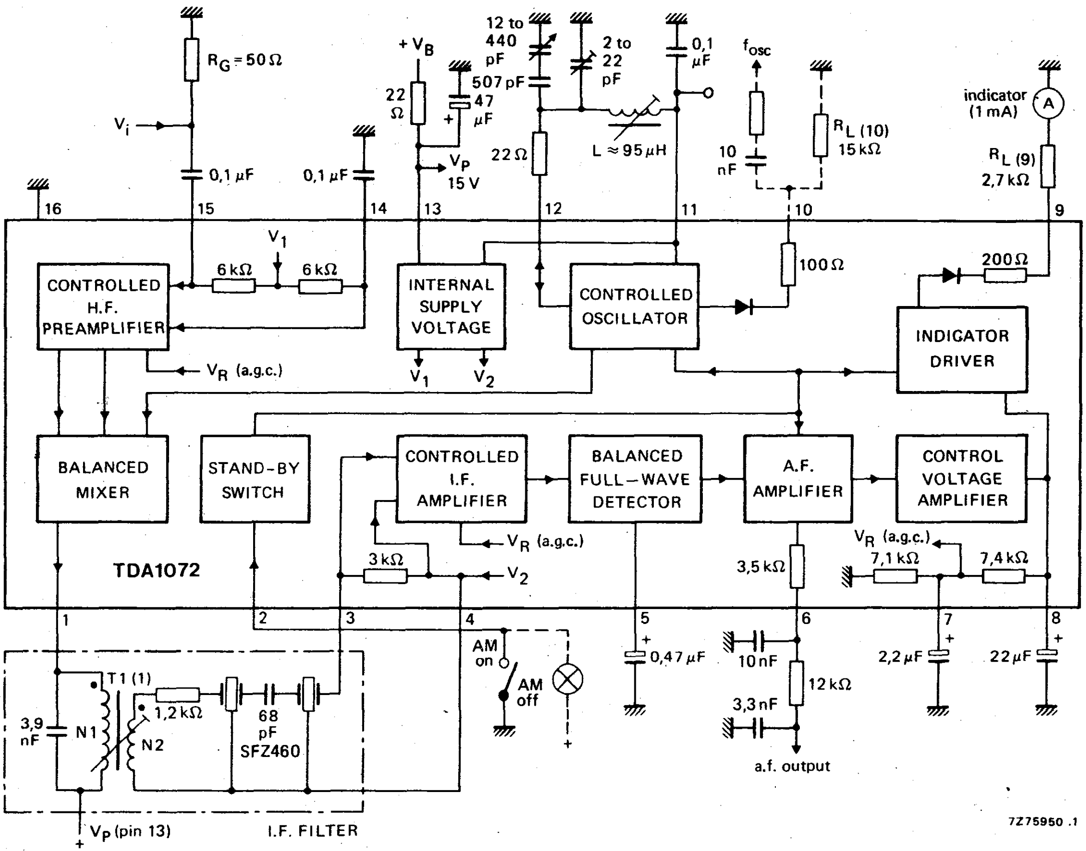
- controlled h.f. preamplifier
- multiplicative balanced mixer
- separate oscillator with amplitude control
- i.f. amplifier with gain control
- balanced full-wave detector
- a.f. preamplifier
- internal a.g.c. voltage
- amplifier for field-strength indication
- electronic stand-by on/off switch

QUICK REFERENCE DATA

Supply voltage (pin 13)	V_P	typ.	15	V
Supply current	I_P	typ.	22	mA
H.F. input voltage				
S + N/N = 6 dB	V_i	typ.	2,2	μV
S + N/N = 26 dB	V_i	typ.	30	μV
H.F. input voltage; d_{tot} = 3%; m = 80%	V_i	typ.	650	mV
A.F. output voltage; V_i = 2 mV	V_o	typ.	340	mV
Total distortion	d_{tot}	typ.	0,5	%
Input voltage range for ΔV_o = 6 dB	ΔV_i	typ.	91	dB
Oscillator frequency range	f_{osc}		0,6 to 31	MHz
Oscillator voltage amplitude	V_{osc}	typ.	140	mV
Field-strength indication range	ΔV_i	typ.	100	dB
Supply voltage range	V_P		7,5 to 18	V
Ambient temperature range	T_{amb}		−30 to +80	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).



(1) T1 : N1/N2 = 34/9; $Q_o = 65$; $Q_L = 60$; $Z_{21} = 700\ \Omega$ at $R_{L(3)} = 3\ k\Omega$; $Z_{11} = 5,2\ k\Omega$.

Fig. 1 Block diagram with external components; used as test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 13)	$V_P = V_{13\text{-}16}$	max.	23	V
Voltage on pin 2	$V_{2\text{-}16}$		0 to 23	V
H.F. inputs				
Voltages between:				
pins 14 and 15	$\pm V_{14\text{-}15}$	max.	12	V
pins 14 and 16	$V_{14\text{-}16}$	max.	V_P	V
pins 15 and 16	$V_{15\text{-}16}$	max.	V_P	V
Or currents:				
pin 14	$\pm I_{14}$	max.	10	mA
pin 15	$\pm I_{15}$	max.	10	mA
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

CHARACTERISTICS

$V_P = 15$ V; $T_{amb} = 25$ °C; $f_i = 1$ MHz (h.f.), $R_G = 50\ \Omega$; $f_m = 0{,}4$ kHz; m = 30%;
i.f. frequency = 460 kHz; unless otherwise specified

Supply voltage range (pin 13)	V_P		7,5 to 18	V
Supply current; without load ($I_{L(11)} = 0$)	I_P	typ.	22	mA
			15 to 30	mA
H.F. preamplifier and mixer				
D.C. input voltages	$V_{14\text{-}16}$; $V_{15\text{-}16}$	typ.	2,75 ($4V_{BE}$)	V
Input impedance				
$V_i < 300\ \mu V$	$Z_{i(14\text{-}16)}$;$Z_{i(15\text{-}16)}$	typ.	6	kΩ
		typ.	6	pF
$V_i > 10$ mV	$Z_{i(14\text{-}16)}$;$Z_{i(15\text{-}16)}$	typ.	9	kΩ
		typ.	2,5	pF
Output impedance	$Z_{o(1\text{-}16)}$	>	200	kΩ
		typ.	4	pF
Maximum conversion conductance	S_M	typ.	5,5	mA/V*
Maximum i.f. output voltage (peak-to-peak value)	$V_{o(1)(p\text{-}p)}$	typ.	2,8	V
Output current capability	$I_{o(1)}$	typ.	1	mA
Control range of preamplifier	ΔS_M	typ.	30	dB
Maximum h.f. input voltage (peak-to-peak value)	$V_{i(14\text{-}15)(p\text{-}p)}$	typ.	2,8	V

* S_M is defined as $I_{o(1)}/V_i$.

CHARACTERISTICS (continued)

Oscillator

Frequency range	$f_{osc(12)}$	0,6 to 31 MHz
Oscillator impedance range	$Z_{L(12)}$	1 to 200 kΩ
Controlled oscillator amplitude	$V_{osc(12)}$	typ. 140 mV < 200 mV
D.C. output voltage ($I_{L(11)} = 0$)	V_{11-16}	typ. V_P–1,3 V
Output load current range	$-I_{L(11)}$	0 to 15 mA
Output resistance; $I_{L(11)} = 5 \pm 0,5$ mA	$R_{o(11)}$	typ. 7 Ω

Oscillator frequency output (pin 10)

Output voltage (peak-to-peak value) $R_{10-16} = 15$ kΩ ($R_{L(10)}$)	$V_{o(10)(p-p)}$	typ. 200 mV
Output resistance	$R_{o(10)}$	typ. 150 Ω
Allowable output current (peak value)	$I_{o(10)M}$	< 2 mA

I.F. amplifier and a.f. stage

D.C. input voltages	V_{3-16}; V_{4-16}	typ. 2 V
Input impedance	$Z_{i(3)}$	typ. 3 kΩ 2,4 to 3,9 kΩ typ. 4 pF
Max. i.f. input voltage; m = 80%; $d_{tot} = 3\%$	$V_{i(3)}$	typ. 75 mV
Control range; $V_o = -6$ dB	ΔV_i	typ. 62 dB
A.F. output voltage; $V_{i(3)} = 2$ mV; without load	$V_{o(6)}$	typ. 350 mV
A.F. output resistance	$R_{o(6)}$	typ. 3,5 kΩ

Field-strength indication

D.C. indicator voltage $V_i = 0$; $R_{L(9)} = 2,7$ kΩ	V_{9-16}	typ. 0 mV < 140 mV
$V_i = 500$ mV; $R_{L(9)} = 2,7$ kΩ	V_{9-16}	typ. 2,8 V 2,5 to 3,1 V
Output current capability	$-I_9$	> 1,2 mA
Output resistance; $-I_9 = 0,5$ mA	$R_{o(9)}$	typ. 250 Ω
Leakage voltage at the output; $\pm I_9 \leqslant 1\ \mu A$; at AM switch off ($V_{2-16} \geqslant 3,5$ V)	V_{9-16}	typ. 6 V

Stand-by switch

Switching voltage	$V_{2\text{-}16}$	typ.	2,6 V
Required control voltage*			
AM on	$V_{2\text{-}16}$	<	2 V
AM off	$V_{2\text{-}16}$	>	3,5 V**
Input current			
AM on; switching current	$-I_2$	<	100 μA
AM off; leakage current ($V_{2\text{-}16} = V_{3\text{-}16}$)	$\pm I_2$	<	1 μA

APPLICATION INFORMATION

$V_P = 15$ V; $T_{amb} = 25$ °C; measured in Fig. 1; $f_i = 1$ MHz (h.f.); $f_m = 0{,}4$ kHz; m = 30%; unless otherwise specified

H.F. input voltage			
S + N/N = 6 dB	V_i	typ.	2,2 μV
S + N/N = 10 dB	V_i	typ.	3,5 μV
S + N/N = 26 dB	V_i	typ.	30 μV
S + N/N = 46 dB	V_i	typ.	550 μV
H.F. input voltage for a.g.c. operation	V_i	typ.	14 μV
Control range for $\Delta V_o = 6$ dB			
reference value $V_i = 500$ mV	ΔV_i	typ.	91 dB
Maximum h.f. input voltage			
$d_{tot} = 3\%$; m = 80%	V_i	typ.	0,65 V
$d_{tot} = 3\%$; m = 30%	V_i	typ.	0,9 V
$d_{tot} = 10\%$; m = 30%	V_i	typ.	1,3 V
A.F. output voltage; $V_i = 2$ mV	V_o	typ.	340 mV
Change of a.f. output voltage; $V_i = 2$ mV	ΔV_o	typ.	± 2 dB
H.F. input voltage; $V_o = 60$ mV	V_i	typ.	4 μV
Total distortion of a.f. output voltage			
$V_i = 2$ mV; m = 80%	d_{tot}	typ.	0,5 %
$V_i = 500$ mV; m = 80%	d_{tot}	typ.	1,8 %
		<	3 %
Signal plus noise-to-noise ratio of a.f. output voltage			
$V_i = 2$ mV	S + N/N	typ.	50 dB
I.F. bandwidth (−3 dB)	B	typ.	4,6 kHz
I.F. selectivity			
$\Delta f = \pm 9$ kHz	$S_{(9)}$	typ.	30 dB
$\Delta f = \pm 36$ kHz	$S_{(36)}$	typ.	60 dB

* At allowable ambient temperature range and supply voltage range.

** Also achieved at open input.

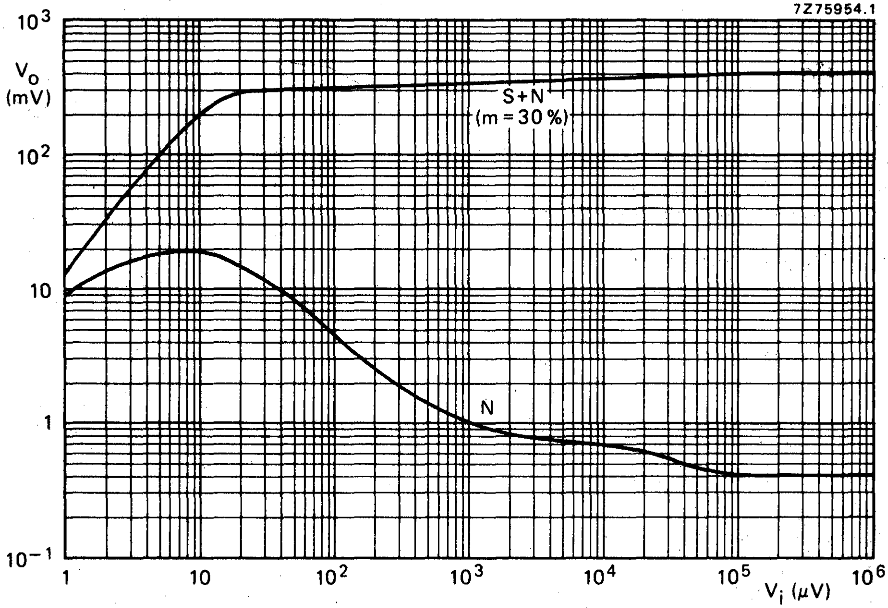


Fig. 2 A.F. output voltage as a function of h.f. input voltage; f_i = 1 MHz (h.f.); R_G = 50 Ω; f_m = 0,4 kHz.

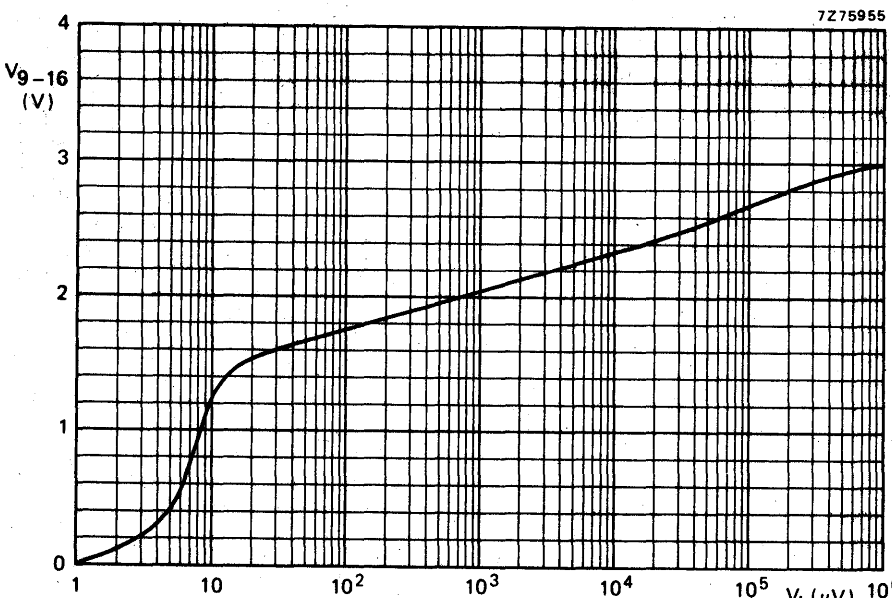


Fig. 3 Indication voltage as a function of h.f. input voltage; R_{9-16} = 2,7 kΩ.

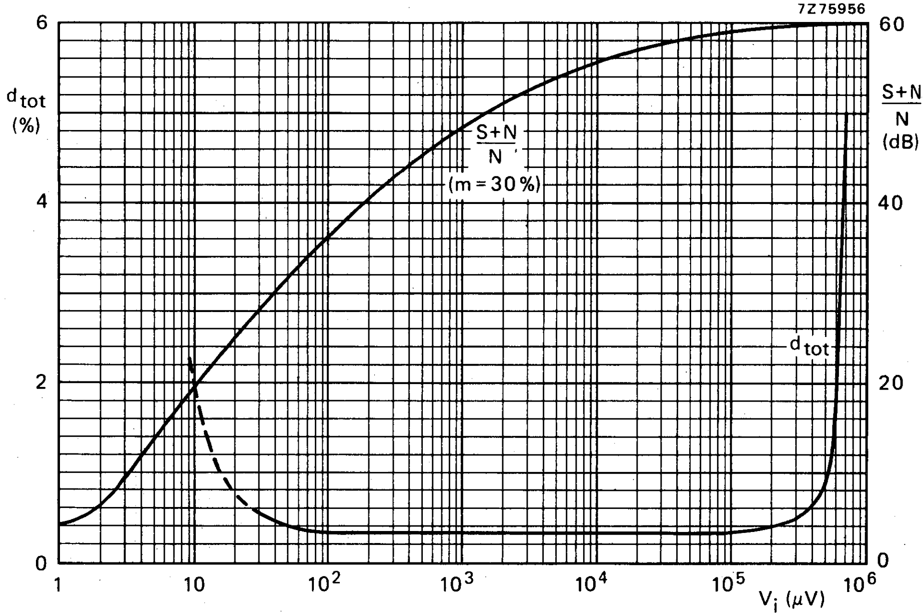


Fig. 4 Total distortion and signal plus noise-to-noise ratio as a function of h.f. input voltage; for d_{tot} : f_m = 0,4 kHz; m = 80%.

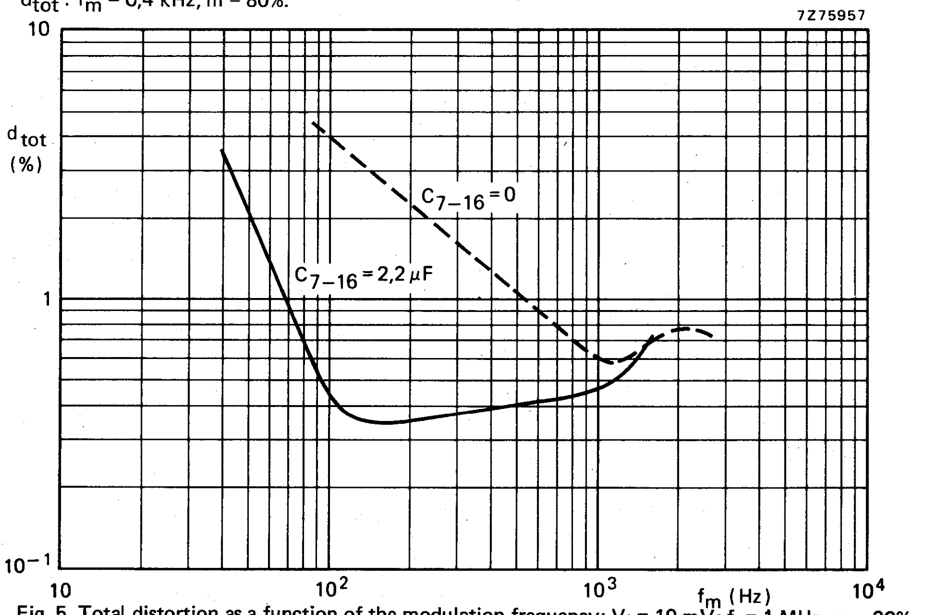


Fig. 5 Total distortion as a function of the modulation frequency; V_i = 10 mV; f_i = 1 MHz; m = 80%. $C_{8\text{-}16}$ = 22 μF.

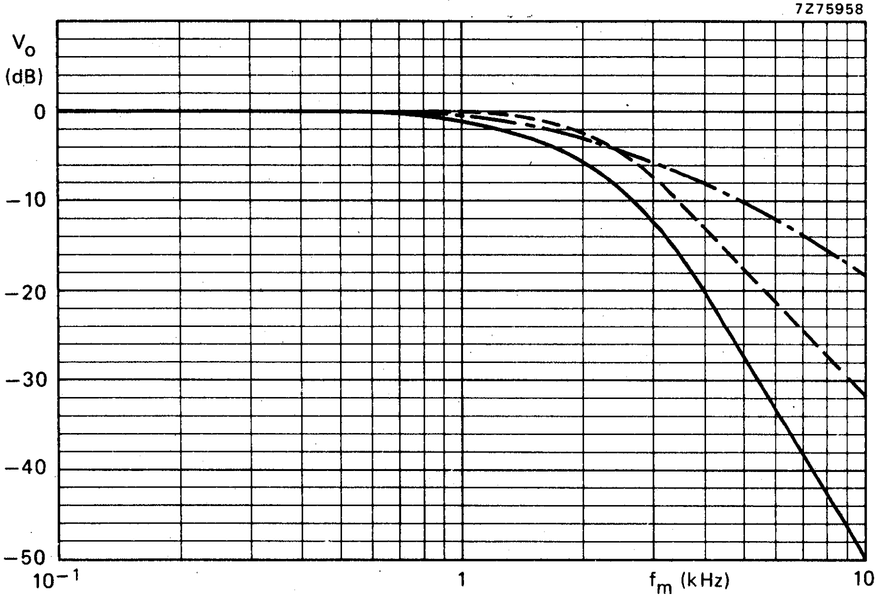
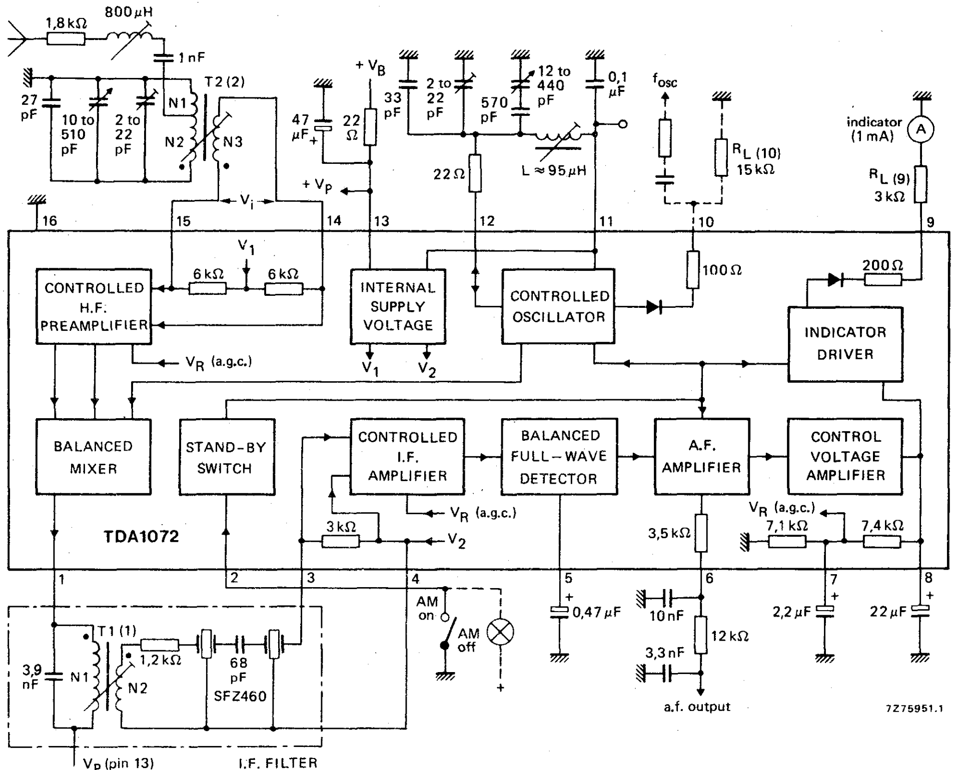
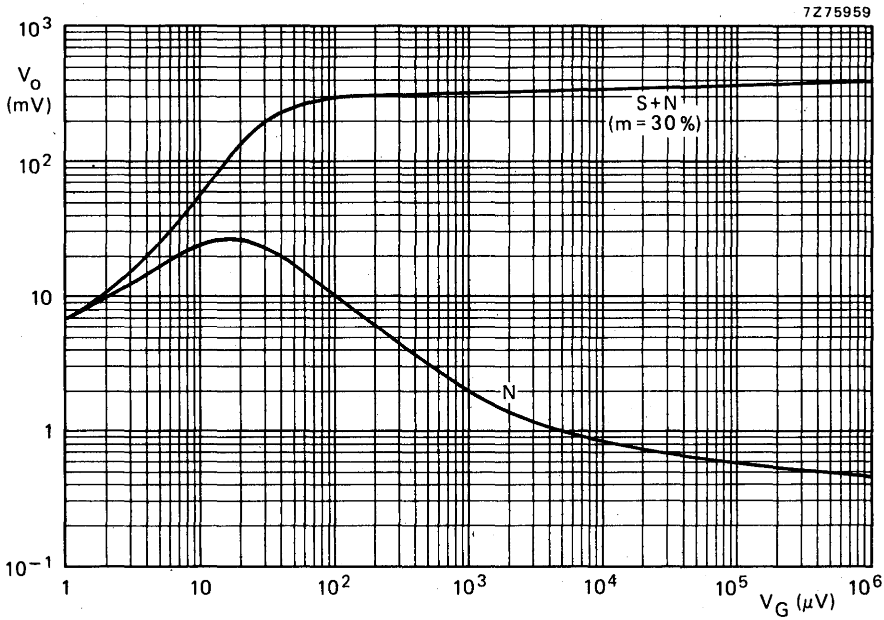


Fig. 6 Frequency responses (wobbled) for various conditions:
——— with a.f. and i.f. filter
– – – with i.f. filter
– · – with a.f. filter



(1) T1 : N1/N2 = 34/9; Q_o = 65; Q_L = 60; Z_{21} = 700 Ω at $R_{L(3)}$ = 3 kΩ; Z_{11} = 5,2 kΩ.
(2) T2 : N1/N2/N3 = 14/67/17; L = 175 μH; Q_o = 145; Q_L = 50 (f = 1 MHz); V_i/V_G = –6 dB.

Fig. 7 Application circuit diagram of a AM-MW receiver with two double variable tuning capacitors; f_i = 510 to 1620 kHz (h.f.); f_i = 460 kHz (i.f.).



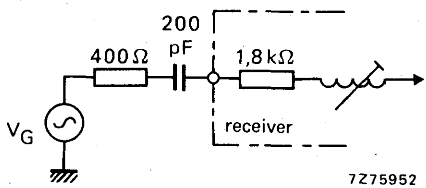


Fig. 8 A.F. output voltage as a function of the h.f. generator input voltage; f_i = 1 MHz (h.f.); f_m = 0,4 kHz.

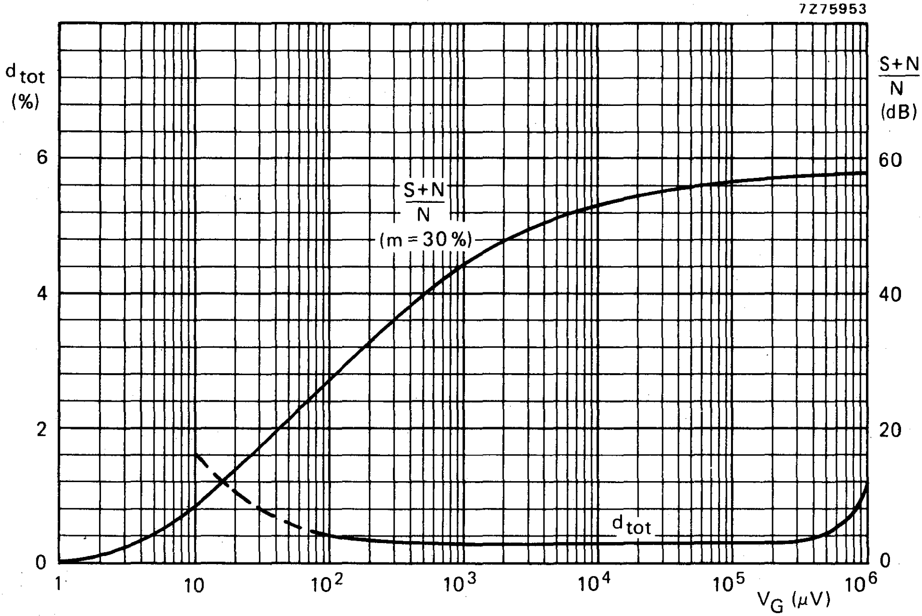


Fig. 9 Total distortion and signal plus noise-to-noise ratio as a function of h.f. generator input voltage; for d_{tot} : f_m = 0,4 kHz; m = 80%.

DUAL ELECTRONIC STEREO POTENTIOMETER CIRCUIT

The TDA1074 is a monolithic integrated circuit designed for use as adjustment circuit in stereo amplifiers. The circuit contains the following functions:

- internal amplifier
- two high-ohmic inputs for each adjuster
- electronic supply voltage filter
- feedback output stages with short-circuit protected current limitation

QUICK REFERENCE DATA

Supply voltage (pin 11)	V_P	typ.	20	V
Supply current (pin 11)	I_P	typ.	20	mA
Input signal voltage (r.m.s. value)	$V_{i(rms)}$	$\nless$	6	V
Output signal voltage (r.m.s. value)	$V_{o(rms)}$	$<$	6	V
Total distortion	d_{tot}	typ.	0,05	%
Output noise voltage (r.m.s. value)	$V_{no(rms)}$	typ.	50	μV
Adjustment range	$\Delta\alpha$	typ.	110	dB
Channel separation	α	typ.	80	dB
Hum suppression	α_{100}	typ.	46	dB
Channel balance	ΔG	typ.	0,5	dB
Supply voltage range	V_P		7,5 to 23	V
Ambient temperature range	T_{amb}		−30 to +80	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102C).

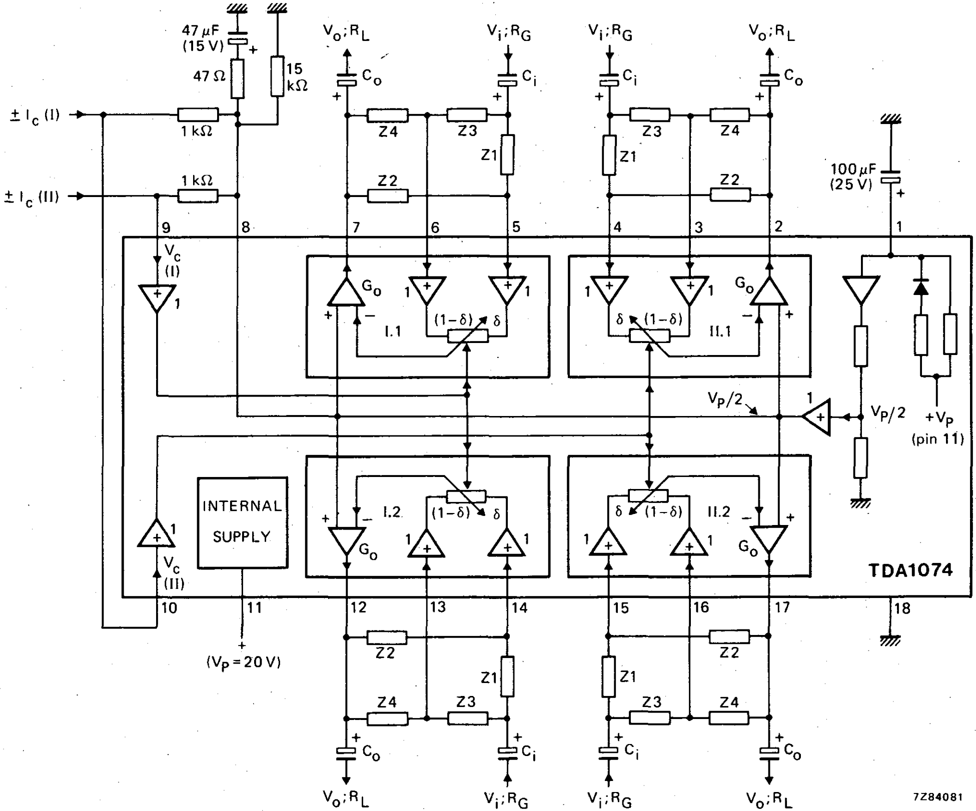


Fig. 1 Block diagram and external components; $I_{c(I)}$, $I_{c(II)}$, $V_{c(I)} = V_{9\text{-}8}$, $V_{c(II)} = V_{10\text{-}8}$ are control input currents and voltages; Z1 = Z2 = Z3 = Z4 = 22 kΩ; R_G = 60 Ω; R_L = 4,7 kΩ; C_i = 2,2 μF; C_o = 10 μF.

Application notes

When one or more adjusters of an IC are not used, the following is recommended:

1. Unused signal inputs of an adjuster should be connected to the associated output, e.g. pins 3 and 4 to pin 2.
2. Unused control voltage inputs should be connected directly to pin 8.
3. Where more than one TDA1074 circuit is used in an application, pins 1 can be connected together; however, pins 8 may not be connected together directly.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 11)	V_P	max.	23	V
Control voltages (V_c)	$V_{9\text{-}8}$; $V_{10\text{-}8}$	max.	1	V
	$-V_{9\text{-}8}$; $-V_{10\text{-}8}$	max.	1	V
Input voltages (with respect to pin 18) at pins 3, 4, 5, 6, 13, 14, 15, 16			0 to V_P	
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	−55 to + 150		^oC
Operating ambient temperature range	T_{amb}	−30 to + 80		^oC

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80	$^oC/W$

DEVELOPMENT SAMPLE DATA

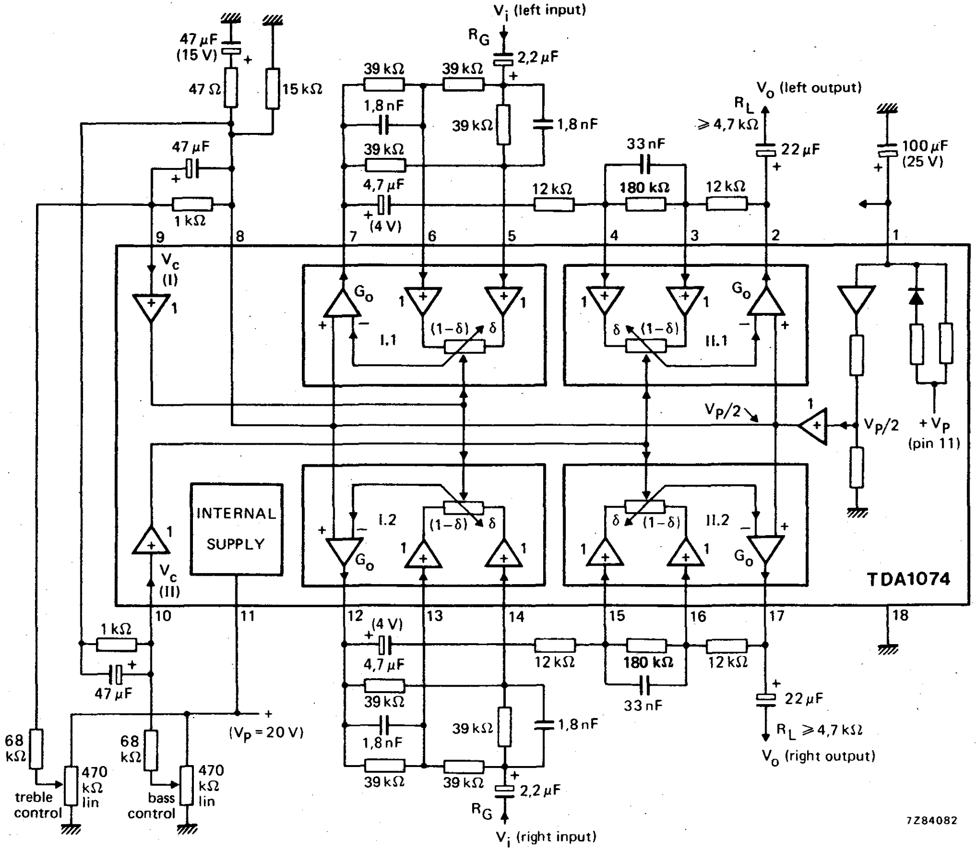


Fig. 2 Application diagram for treble and bass control.

APPLICATION INFORMATION

Tone control circuit

$V_P = 20$ V; $T_{amb} = 25$ °C; in the application for treble control and bass control Fig. 2; $R_G = 60\ \Omega$; $R_L \geqslant 4,7$ kΩ; $C_L \leqslant 30$ pF; f = 1 kHz; unless otherwise specified.

Supply current; without load	I_P	typ.	20	mA
			13 to 30	mA
Frequency response (−1 dB) $V_c = 0$	f		10 Hz to 20	kHz
Voltage gain at linear frequency response $V_c = 0$	G_v	typ.	0	dB
Maximum gain variation at f = 1 kHz at maximum bass/treble boost or cut $\pm V_c = 120$ mV	ΔG_v	typ.	± 1,5	dB
Bass boost at 40 Hz (ref. 1 kHz) $V_{c(II)} = V_{10\text{-}8} = 120$ mV		typ.	17	dB
Bass cut at 40 Hz (ref. 1 kHz) $-V_{c(II)} = V_{10\text{-}8} = 120$ mV		typ.	−17	dB
Treble boost at 16 kHz (ref. 1 kHz) $V_{c(I)} = V_{9\text{-}8} = 120$ mV		typ.	16	dB
Treble cut at 16 kHz (ref. 1 kHz) $-V_{c(I)} = V_{9\text{-}8} = 120$ mV		typ.	−16	dB
Total distortion at $V_{i(rms)} = 5$ V $V_c = 0$, at linear frequency response for f = 1 kHz	d_{tot}	typ.	0,03	%
		<	0,1	%
for f = 40 Hz to 16 kHz	d_{tot}	typ.	0,07	%
Channel separation at $V_{i(rms)} = 5$ V $V_c = 0$, at linear frequency response	α	typ.	80	dB
Output noise voltages; $V_c = 0$; f = 20 Hz to 20 kHz signal plus noise voltage (r.m.s. value)	$V_{no(rms)}$	typ.	75	μV
noise voltage; weighted conform DIN 45405; peak value	$V_{no(m)}$	typ.	170	μV
		$\leqslant$	230	μV
Signal level for $d_{tot} = 1\%$; $V_c = 0$	$V_{i(rms)} = V_{o(rms)}$	typ.	6	V
Hum suppression for f = 100 Hz $V_{P(rms)} \leqslant 200$ mV (at 100 Hz); $V_c = 0$	α_{100}	typ.	46	dB

DEVELOPMENT SAMPLE DATA

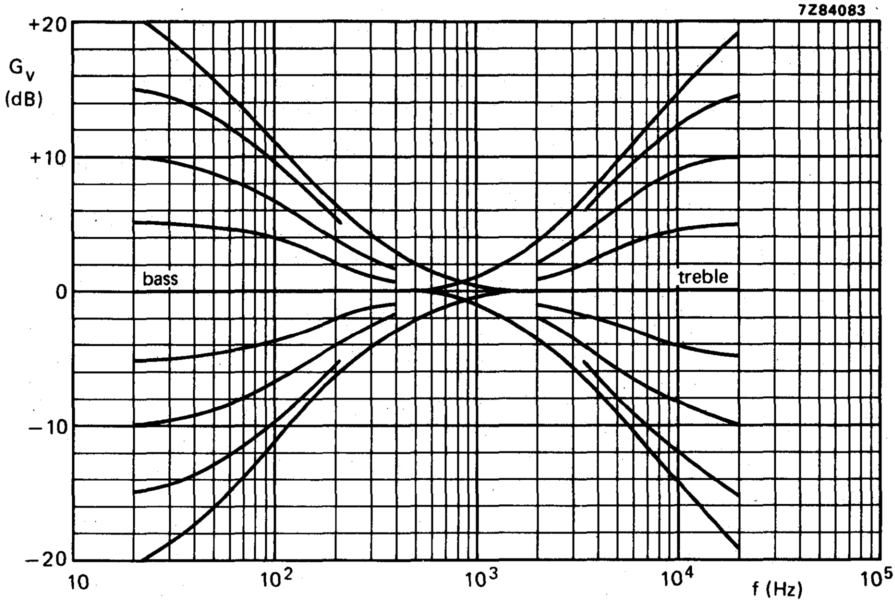


Fig. 3 Frequency response curves; voltage gain (bass and treble) as a function of frequency.

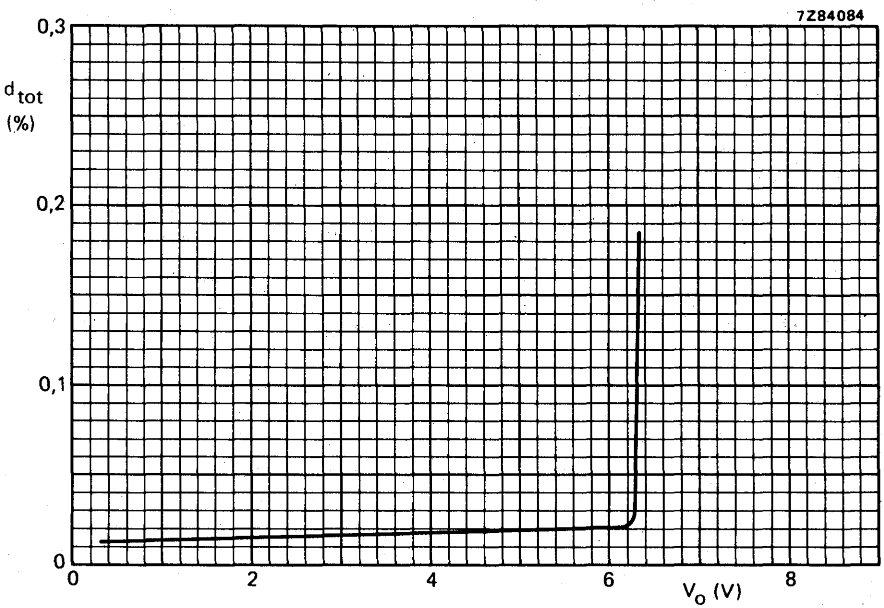


Fig. 4 Control capability; $V_P = 20$ V; f = 1 kHz, $V_c = V_{9\text{-}8} = V_{10\text{-}8} = 0$ V (linear, $G_{v\,tot} = 1$); $R_L = 4{,}7\ k\Omega$.

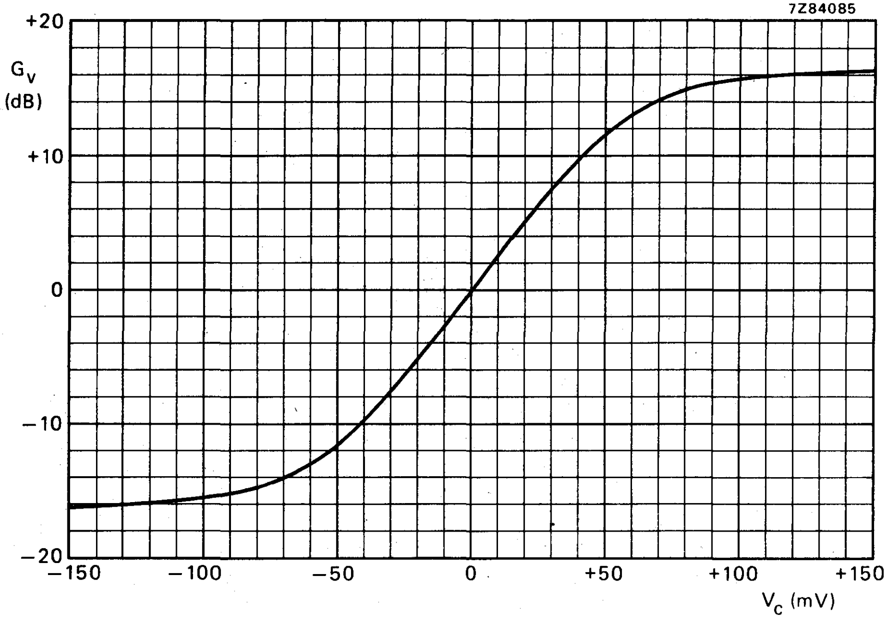


Fig. 5 Control curve; voltage gain (treble) as a function of control voltage; f = 16 kHz.

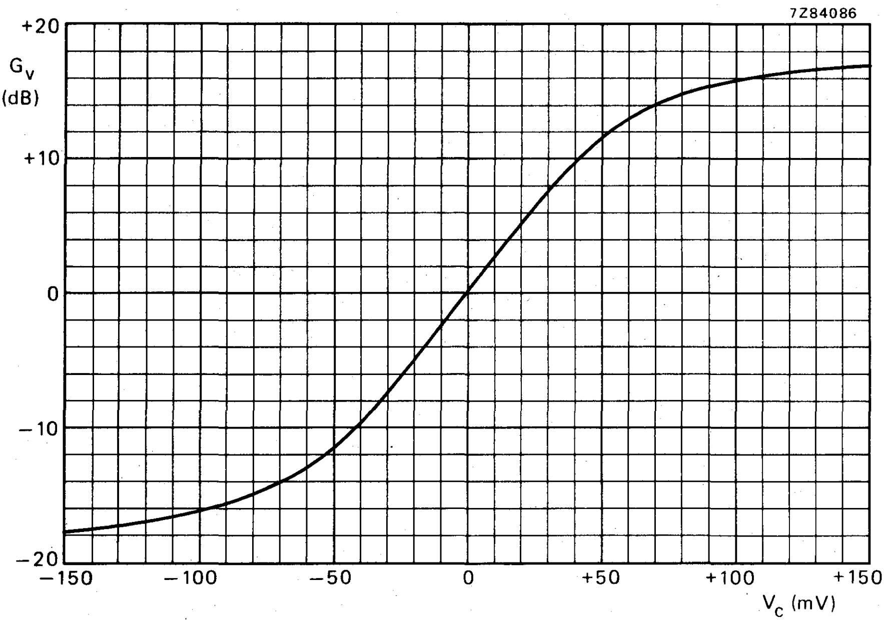


Fig. 6 Control curve; voltage gain (bass) as a function of control voltage.

APPLICATION INFORMATION (continued)

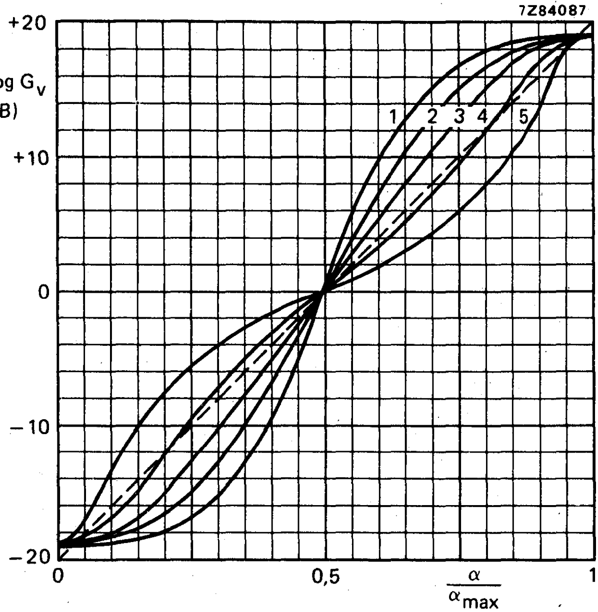
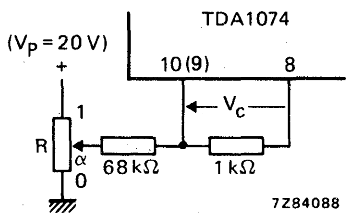


Fig. 7 Adjustment curves at 40 Hz to 16 kHz as a function of the angle of rotation (α) of a linear potentiometer (R); for curves see table below.



curve no.	value of R
1	10 kΩ
2	100 kΩ
3	220 kΩ
4	470 kΩ
5	1 MΩ

Fig. 8 Circuit diagram showing measurement of curves in Fig. 7.

12 TO 20 W HI-FI AUDIO POWER AMPLIFIER

The TDA1512 is a monolithic integrated hi-fi audio power amplifier designed for asymmetrical or symmetrical power supplies for mains-fed apparatus.
Special features are:

- Thermal protection
- Low intermodulation distortion
- Low transient intermodulation distortion
- Built-in output current limiter
- Low input offset voltage
- Output stage with low cross-over distortion
- Single in-line (SIL) power package

QUICK REFERENCE DATA

Supply voltage range	V_P		15 to 35	V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65	mA
Output power at d_{tot} = 0,7%				
sine-wave power				
V_P = 25 V; R_L = 4 Ω	P_o	typ.	13	W
V_P = 25 V; R_L = 8 Ω	P_o	typ.	7	W
music power				
V_P = 32 V; R_L = 4 Ω	P_o	typ.	21	W
V_P = 32 V; R_L = 8 Ω	P_o	typ.	12	W
Closed-loop voltage gain (externally determined)	G_c	typ.	30	dB
Input resistance (externally determined)	R_i	typ.	20	kΩ
Signal-to-noise ratio at P_o = 50 mW	S/N	typ.	72	dB
Supply voltage ripple rejection at f = 100 Hz	RR	typ.	50	dB

PACKAGE OUTLINE

9-lead SIL; plastic power (SOT-131B).

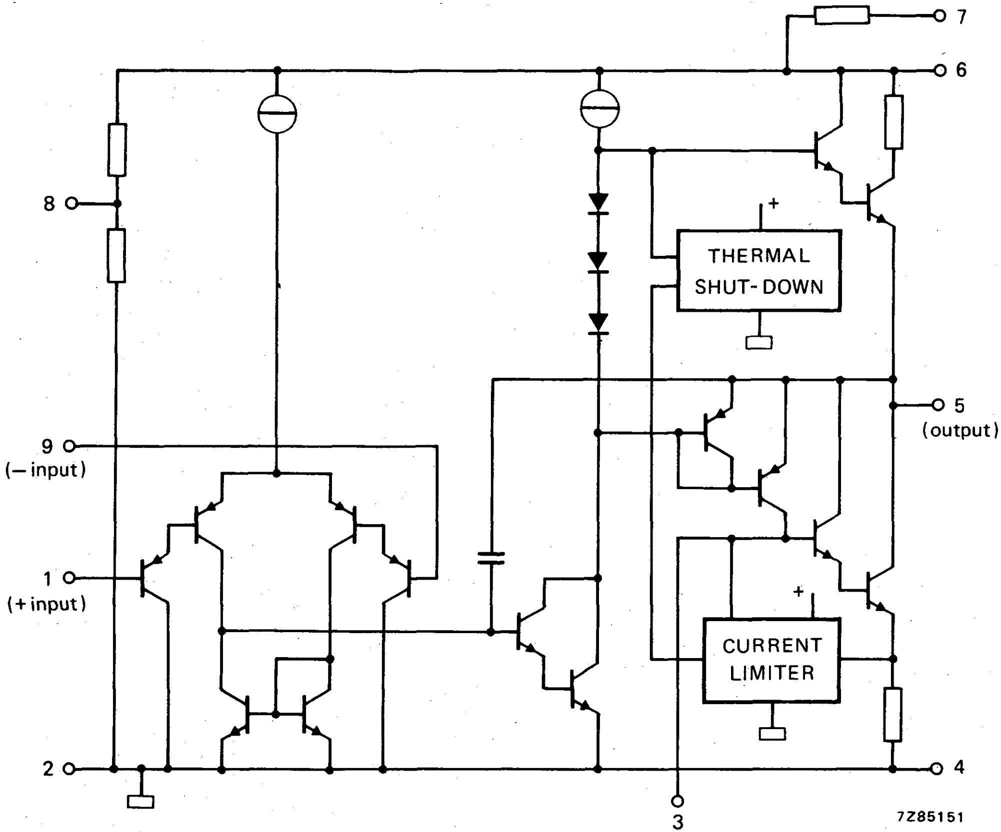


Fig. 1 Simplified internal circuit diagram.

PINNING

1. Non-inverting input
2. Input ground (substrate)
3. Compensation
4. Negative supply (ground)
5. Output
6. Positive supply (V_P)
7. Externally connected to pin 6
8. Ripple rejection
9. Inverting input (feedback)

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35	V
Repetitive peak output current	I_{ORM}	max.	3,2	A
Non-repetitive peak output current	I_{OSM}	max.	5	A
Total power dissipation	see derating curve Fig. 2			
Storage temperature	T_{stg}		−55 to + 150	°C
Operating ambient temperature	T_{amb}		−25 to + 150	°C
A.C. short-circuit duration of load during full-load sine-wave drive $R_L = 0$; $V_P = 30$ V with $R_i = 4\ \Omega$	t_{sc}	max.	100	hours

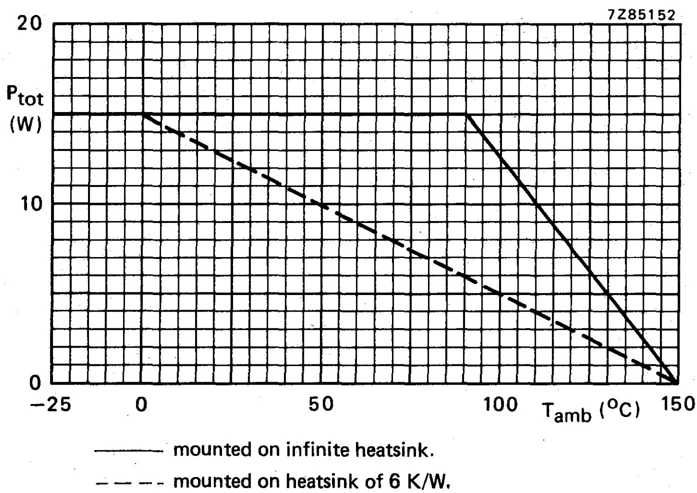


Fig. 2 Power derating curves.

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j\text{-}mb}$	≤	4	K/W

DEVELOPMENT SAMPLE DATA

D.C. CHARACTERISTICS

Supply voltage range	V_P		15 to 35 V
Total quiescent current at V_P = 25 V	I_{tot}	typ.	65 mA

A.C. CHARACTERISTICS

V_P = 25 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; measured in test circuit of Fig. 3; unless otherwise specified

Output power			
sine-wave power at d_{tot} = 0,7 %			
R_L = 4 Ω	P_o	typ.	13 W
R_L = 8 Ω	P_o	typ.	7 W
music power at V_P = 32 V			
R_L = 4 Ω; d_{tot} = 0,7 %	P_o	typ.	21 W
R_L = 4 Ω; d_{tot} = 10 %	P_o	typ.	25 W
R_L = 8 Ω; d_{tot} = 0,7 %	P_o	typ.	12 W
R_L = 8 Ω; d_{tot} = 10 %	P_o	typ.	15 W
Power bandwidth; −3 dB; d_{tot} = 0,7 %	B		20 Hz to 20 kHz
Voltage gain			
open-loop	G_o	typ.	74 dB
closed-loop	G_c	typ.	30 dB
Input resistance (pin 1)	R_i	>	100 kΩ
Input resistance of test circuit (Fig. 3)	R_i	typ.	20 kΩ
Input sensitivity			
for P_o = 50 mW	V_i	typ.	16 mV
for P_o = 10 W	V_i	typ.	210 mV
Signal-to-noise ratio			
at P_o = 50 mW; R_S = 2 kΩ; f = 20 Hz to 20 kHz; unweighted	S/N	typ.	72 dB
weighted; measured according to IEC 173 (A-curve)	S/N	typ.	76 dB
Ripple rejection at f = 100 Hz	RR	typ.	50 dB
Total harmonic distortion at P_o = 10 W	d_{tot}	typ. <	0,1 % 0,3 %
Output resistance (pin 5)	R_o	typ.	0,1 Ω

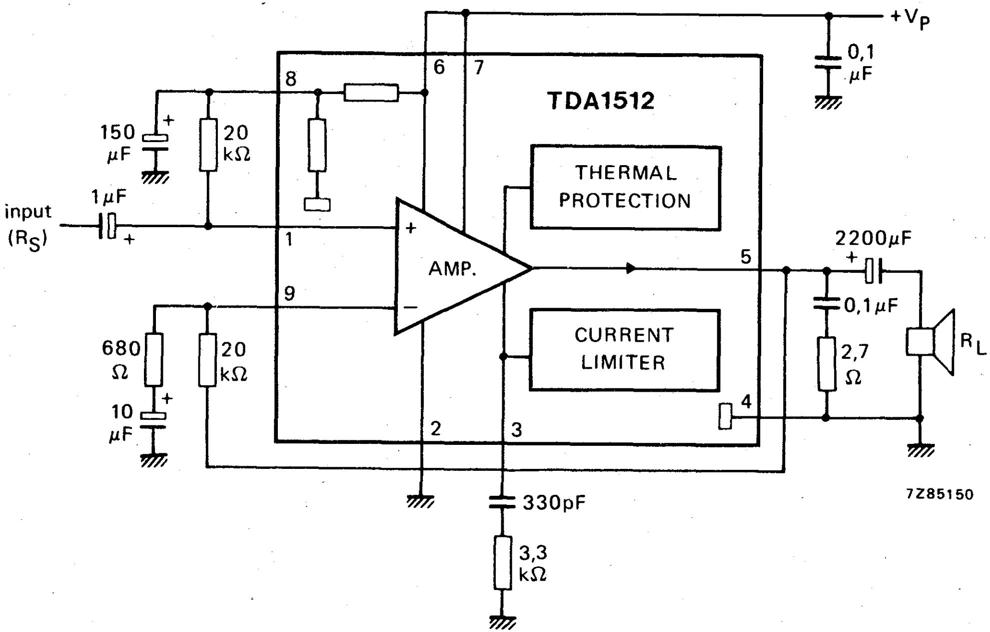


Fig. 3 Test circuit.

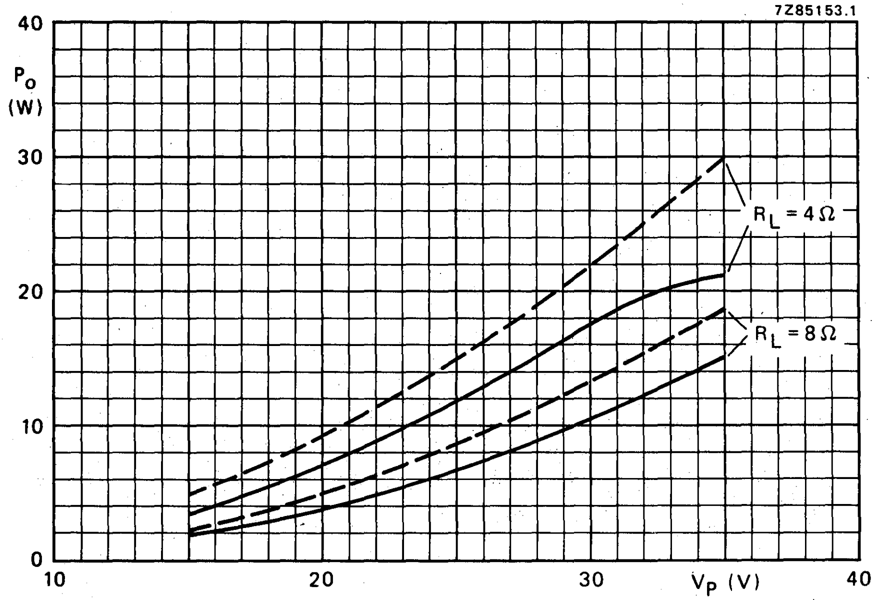


Fig. 4 Output power as a function of the supply voltage; f = 1 kHz;
——— d_{tot} = 0,7 %; – – – d_{tot} = 10 %.

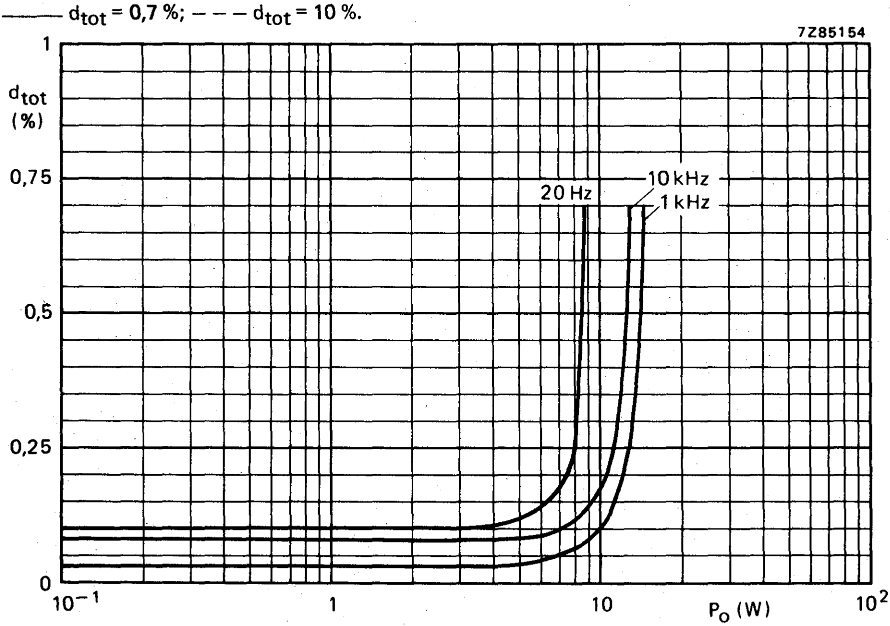


Fig. 5 Total harmonic distortion as a function of the output power.

PLL MOTOR SPEED CONTROL CIRCUIT FOR HI-FI APPLICATIONS

The TDA1533 is a monolithic integrated circuit intended for PLL motor speed control in several hi-fi applications; e.g. record players, cassette recorders, reel-to-reel, and operates in accordance with the phase-locked-loop (PLL) system.
The circuit incorporates the following functions:

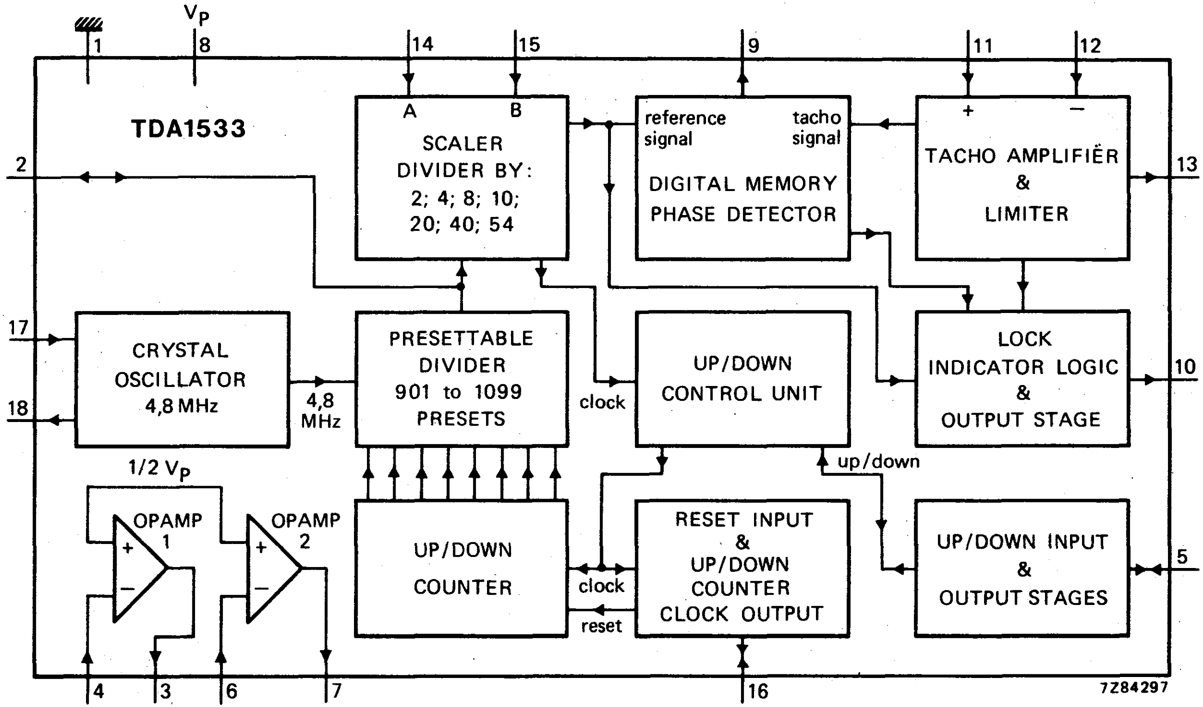
- A quartz reference oscillator
- A synthesizer for adjustment of the phase detector reference frequency
- A programmable scaler for the several applications
- A digital memory phase detector
- A tacho-signal amplifier/limiter
- Two operational amplifiers for the external integration and loop filtering of the phase detector output.

QUICK REFERENCE DATA

Supply voltage range	V_P		9 to 11	V
Supply current	I_P	typ.	50	mA
Crystal oscillator				
Frequency	f	<	5	MHz
Temperature coefficient	TC	<	$0,1.10^{-6}$	K^{-1}
Tacho input				
Input voltage	V_I		–0,3 to + 10	V
Input sensitivity (peak-to-peak value)	$V_{i(p-p)}$	>	10	mV
Operational amplifiers				
Voltage gain	G_v	typ.	10 000	
Input bias current	I_{bias}	<	100	nA
Input offset voltage	V_{io}	<	15	mV
Temperatures				
Storage temperature	T_{stg}		–25 to + 125	°C
Operating ambient temperature	T_{amb}		0 to + 60	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102C).



PINNING

1. Ground
2. Test input/output
3. Output of opamp 1
4. Input of opamp 1
5. Up/down input/output
6. Input of opamp 2
7. Output of opamp 2
8. Positive supply (+ 10 V)
9. Phase detector output
10. Lock indicator output
11. + input tacho limiter
12. − input tacho limiter
13. Output tacho limiter
14. A-input scaler control
15. B-input scaler control
16. Reset input/output
17. Crystal oscillator input
18. Crystal oscillator output

Fig. 1 Block diagram.

GENERAL DESCRIPTION (see also Fig. 1)

The crystal frequency (e.g. 4,8 MHz) is divided by the presettable 901 to 1099 divider. The scaler is used to obtain the reference signal for the digital memory phase detector. The tacho signal is derived from the tacho amplifier/limiter.
The output of the phase detector becomes HIGH on the positive-going edge of the reference signal, and it is floating on the first-coming positive edge of the tacho signal, if the angle between the edges is not more than 360°. The output becomes LOW if the first positive-going edge is the edge of the tacho signal, and it is floating on the first-coming positive edge of the reference signal. This means that the holding range is 720°.
The lock indication output is HIGH, except for the period between the two positive and the two negative-going edges of the tacho and reference signals.
The dividing number of the presettable divider depends on the state of its presets, thus on the position of the up/down counter.
A pull-up to the IC supply voltage of the reset input results into a reset of the up/down counter and dividing by 1000.
The up/down counter can be changed in position by means of the up/down input and the up/down control unit, and therefore the divisors of the presettable divider in a range from 901 to 1099.
The clock of the up/down counter is available at the reset input as a 0,1 V_P to 0,8 V_P pulse.
The timing diagram of the up/down counter is given in Fig. 2.
The up/down input and the scaler control inputs are 3-state inputs. The scaler truth table is given below.
A HIGH level at the up/down input gives an increase, a LOW level a decrease, of the phase detector reference signal frequency.
The information at the up/down input will be internally forced on the state present, over a period of 250 ms. Together with the up/down clock at the reset pin, this offers the possibility of displaying the number of clock pulses used.

SCALER TRUTH TABLE

control inputs A	control inputs B	division ratio
H	H	note 1
H	L	note 2
F	F	4
F	H	8
F	L	2
H	F	54
L	H	10
L	L	20
L	F	40

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
F = floating (pin open)

Notes

1. Test 1; general preset.
2. Test 2; fast clock via test pin (pin 2).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	$V_P = V_{8-1}$	max.	12 V
Total power dissipation	P_{tot}	max.	1 W
Storage temperature	T_{stg}		−25 to + 125 °C
Operating ambient temperature	T_{amb}		−20 to + 80 °C

CHARACTERISTICS

Supply voltage	V_P	typ.	10 V
			9 to 11 V
Supply current	I_P	typ.	50 mA
Operating ambient temperature	T_{amb}		0 to 60 °C

The following characteristics are measured at V_P = 10 V; T_{amb} = 25 °C; unless otherwise specified

Crystal oscillator

Frequency	f	typ.	4,8 MHz
		<	5,0 MHz
Input voltage HIGH	V_{IH}		2,6 to 10 V
Input voltage LOW	V_{IL}		−2,0 to + 2,0 V
Input resistance	R_i	>	50 kΩ
Input capacitance	C_i	<	5 pF
Open voltage 1	V_{o1}	typ.	2 V
Open voltage 2	V_{o2}	typ.	1,3 V
Temperature coefficient	TC	<	$0,1.10^{-6}$ K^{-1}

Lock indicator output (open collector)

Output voltage HIGH	V_{OH}	<	12 V
Output voltage LOW at 10 mA	V_{OL}	typ.	0,25 V
		<	0,5 V
Output sink current	I_o	typ.	10 mA
		<	20 mA

Phase detector output

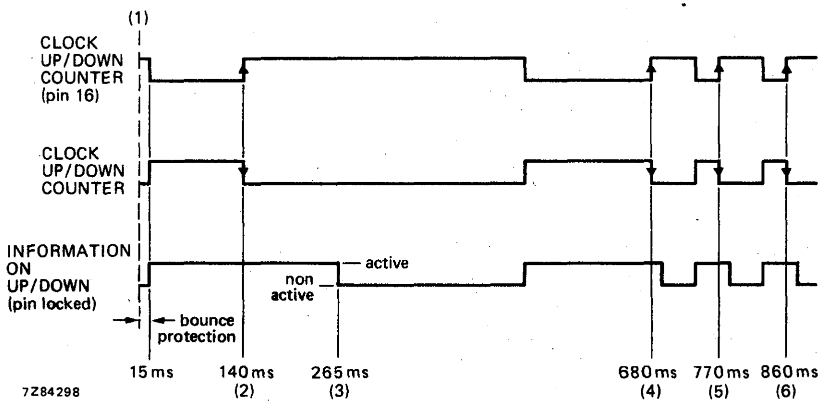
Output voltage HIGH at 20 μA	V_{OH}	>	9,5 V
		typ.	9,7 V
Output voltage LOW at 20 μA	V_{OL}	typ.	0,3 V
		<	0,5 V
Output current			
source	I_o	>	30 μA
		typ.	44 μA
sink	I_o	>	30 μA
		typ.	30 μA

Tacho input			
Input voltage	V_I		–0,3 to + 10 V
Input biasing current	I_{bias}	typ. <	0,5 μA 5,0 μA
Input sensitivity (peak-to-peak value)	$V_{i(p-p)}$	>	10 mV
Offset voltage over temperature range	V_{io}	typ. <	0,1 mV 2,0 mV
Offset current over temperature range	I_{io}	typ. <	50 nA 250 nA
Tacho output (open collector)			
Output voltage HIGH	V_{OH}	<	12 V
Output voltage LOW at 5 mA	V_{OL}	<	0,5 V
Output sink current	I_o	<	10 mA
Up/down - input/output			
Input voltage LOW	V_{IL}	typ.	0 V –0,4 to + 0,4 V
Output voltage HIGH	V_{OH}		3 to 10 V
Open voltage	V_o	typ.	0,7 V 0,6 to 0,8 V
Open voltage HIGH at 0,5 mA	V_{oH}	> typ.	8,5 V 9,0 V
Open voltage LOW at 0,5 mA	V_{oL}	<	0,5 V
Output sink current	I_o	<	10 mA
Output source impedance	$\lvert Z_o \rvert$	<	1,5 kΩ
Scaler inputs			
Input voltage LOW	V_{IL}	typ.	0 V –0,4 to + 0,4 V
Input voltage HIGH	V_{IH}		4 to 10 V
Open voltage	V_o	typ.	0,7 V 0,6 to 0,8 V
Reset input/output			
Input voltage HIGH	V_{IH}	> typ.	9,5 V 10,0 V
Output voltage LOW	V_{OL}	typ. <	0,3 V 0,5 V
Output voltage HIGH	V_{OH}	typ.	8 V

CHARACTERISTICS (continued)

Operational amplifiers

Voltage gain	G_V	typ.	10 000
Input bias current	I_{bias}	typ.	30 nA
		<	100 nA
Output sink current at $V_o = 1$ V	I_o	typ.	0,1 mA
Output source current at $V_o = 9$ V	I_o	>	15 mA
		typ.	20 mA
Input offset voltage	V_{io}	<	15 mV
Input offset voltage drift	$\Delta V_{io}/\Delta T$	<	0,25 mV/K
Bandwidth (3 dB)	B		60 Hz



(1) Start operation of up/down pin.
(2) 1st clock pulse.
(3) From this point on, restart of cycle by second excitation is possible.
(4) 2nd clock pulse.
(5) 3rd clock pulse.
(6) 4th clock pulse.

Fig. 2 Timing diagram of up/down counter.

5 W AUDIO POWER AMPLIFIER

The TDA2611A is a monolithic integrated circuit in a 9-lead single in-line (SIL) plastiç package with a high supply voltage audio amplifier. Special features are:

- **possibility for increasing the input impedance**
- single in-line (SIL) construction for easy mounting
- very suitable for application in mains-fed apparatus
- extremely low number of external components
- thermal protection
- well defined open loop gain circuitry with simple quiescent current setting and fixed integrated closed loop gain

QUICK REFERENCE DATA

Supply voltage range	V_P		6 to 35	V
Repetitive peak output current	I_{ORM}	<	1,5	A
Output power at d_{tot} = 10%				
V_P = 18 V; R_L = 8 Ω	P_o	typ.	4,5	W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5	W
Total harmonic distortion at P_o < 2 W; R_L = 8 Ω	d_{tot}	typ.	0,3	%
Input impedance	$\lvert Z_i \rvert$	typ.	45	kΩ
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25	mA
Sensitivity for P_o = 2,5 W; R_L = 8 Ω	V_i	typ.	55	mV
Operating ambient temperature	T_{amb}		−25 to + 150	°C
Storage temperature	T_{stg}		−55 to + 150	°C

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-110A).

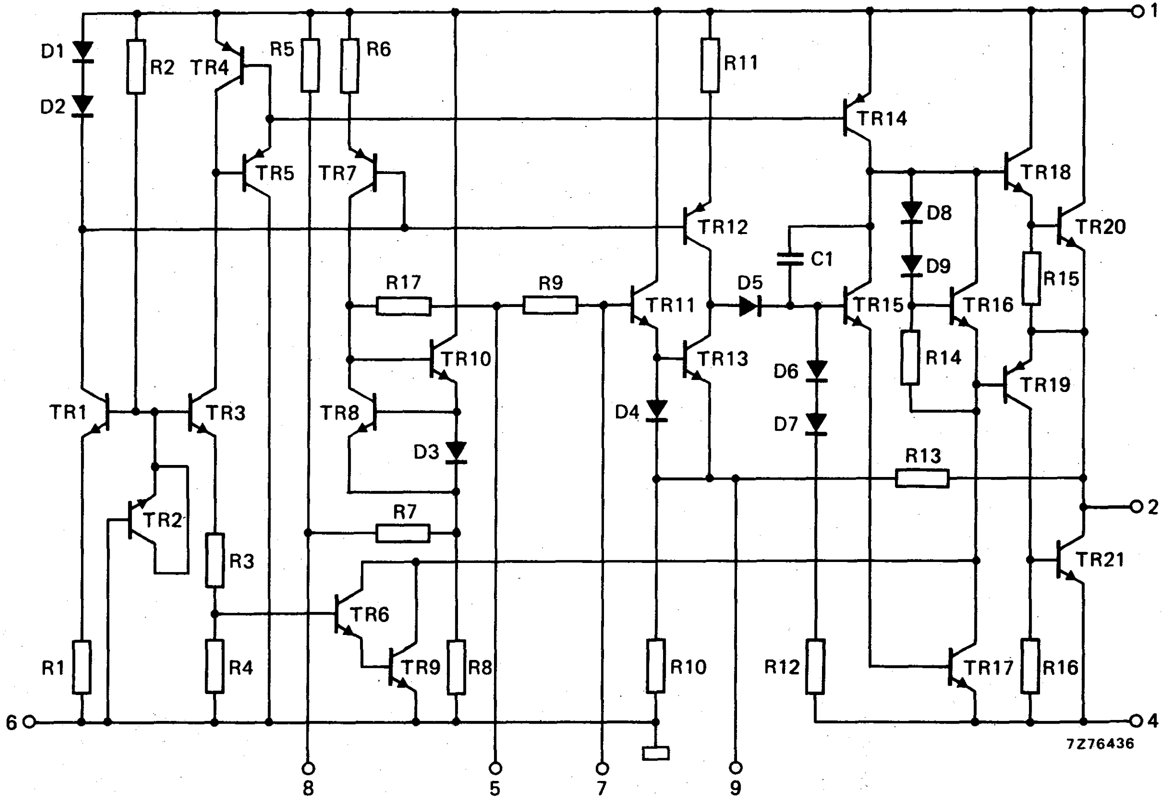


Fig. 1 Circuit diagram; pin 3 not connected.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	35	V
Non-repetitive peak output current	I_{OSM}	max.	3	A
Repetitive peak output current	I_{ORM}	max.	1,5	A
Total power dissipation	see derating curves Fig. 2			
Storage temperature	T_{stg}	−55 to + 150		°C
Operating ambient temperature	T_{amb}	−25 to + 150		°C

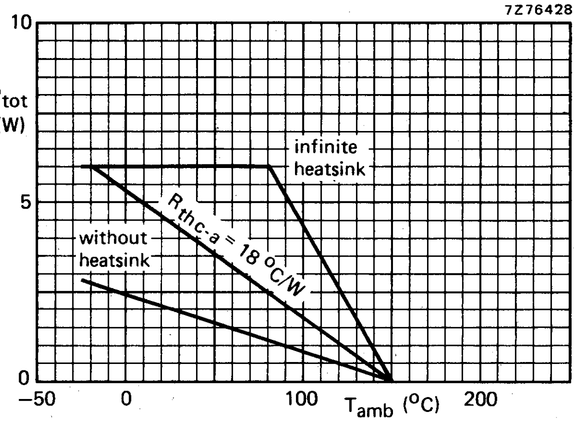


Fig. 2 Power derating curves.

D.C. CHARACTERISTICS

Supply voltage range	V_P		6 to 35 V
Repetitive peak output current	I_{ORM}	<	1,5 A
Total quiescent current at V_P = 18 V	I_{tot}	typ.	25 mA

A.C. CHARACTERISTICS

T_{amb} = 25 °C; V_P = 18 V; R_L = 8 Ω; f = 1 kHz unless otherwise specified; see also Fig. 3

A.F. output power at d_{tot} = 10%			
V_P = 18 V; R_L = 8 Ω	P_o	>	4 W
		typ.	4,5 W
V_P = 12 V; R_L = 8 Ω	P_o	typ.	1,7 W
V_P = 8,3 V; R_L = 8 Ω	P_o	typ.	0,65 W
V_P = 20 V; R_L = 8 Ω	P_o	typ.	6 W
V_P = 25 V; R_L = 15 Ω	P_o	typ.	5 W
→ Total harmonic distortion at P_o = 2 W	d_{tot}	typ.	0,3 %
		<	1 %
Frequency response		>	15 kHz
Input impedance	$\|Z_i\|$	typ.	45 kΩ *
Noise output voltage at R_S = 5 kΩ; B = 60 Hz to 15 kHz	V_n	typ.	0,2 mV
		<	0,5 mV
Sensitivity for P_o = 2,5 W	V_i	typ.	55 mV
			44 to 66 mV

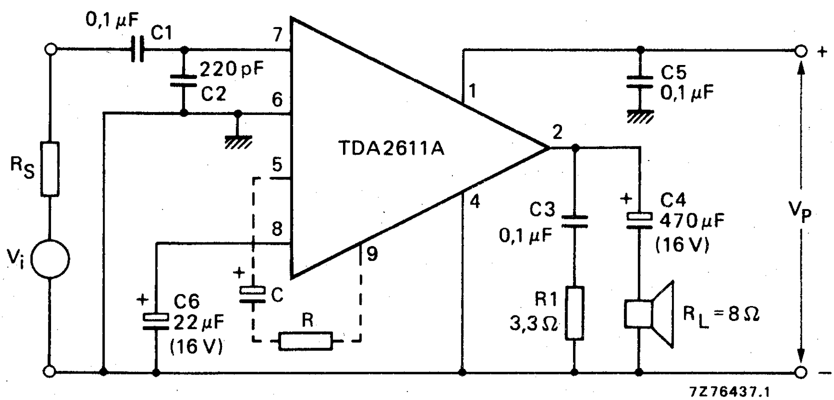


Fig. 3 Test circuit; pin 3 not connected.

* Input impedance can be increased by applying C and R between pins 5 and 9 (see also Figures 6 and 7).

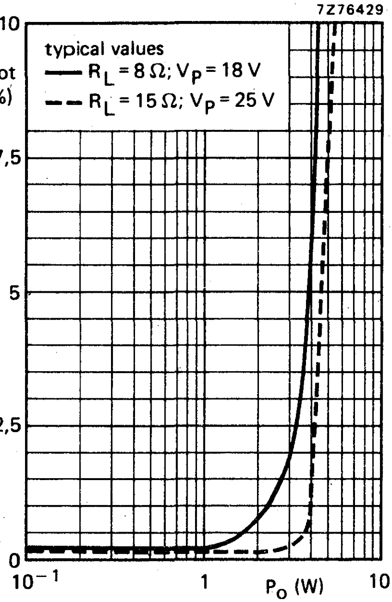


Fig. 4 Total harmonic distortion as a function of output power.

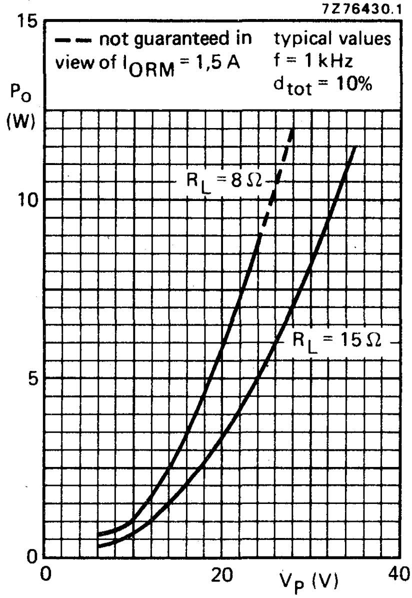


Fig. 5 Output power as a function of supply voltage.

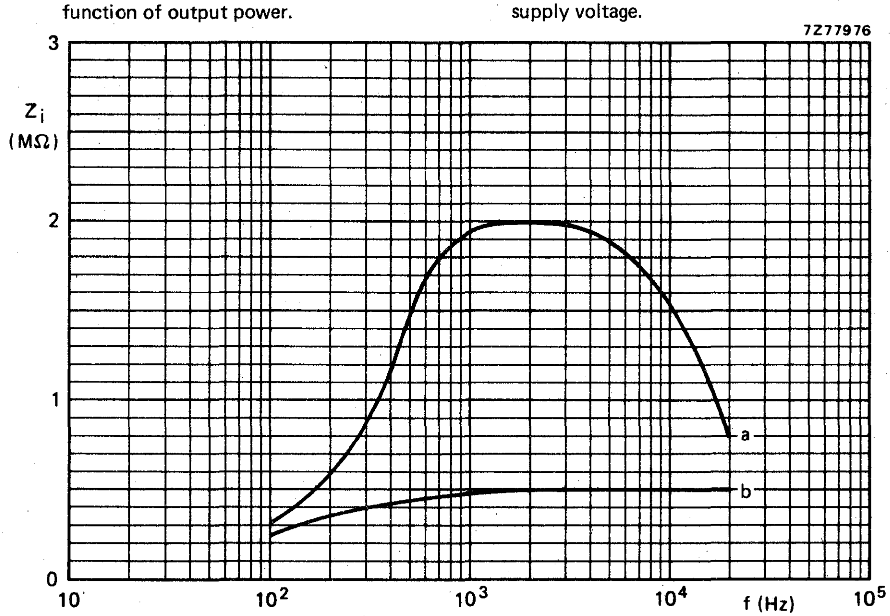


Fig. 6 Input impedance as a function of frequency; curve a for C = 1 μF, R = 0 Ω; curve b for C = 1 μF, R = 1 kΩ; circuit of Fig. 3; C2 = 10 pF; typical values.

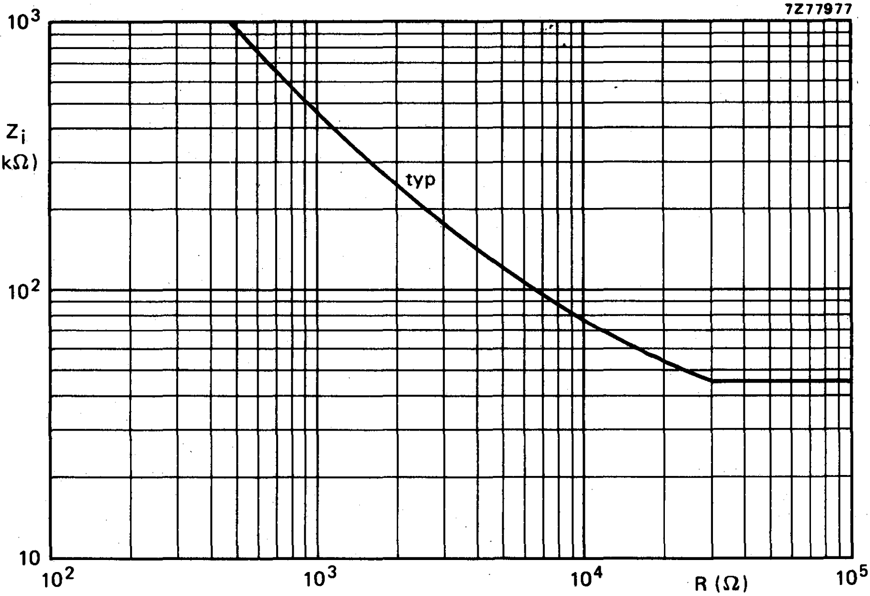


Fig. 7 Input impedance as a function of R in circuit of Fig. 3; C = 1 μF; f = 1 kHz.

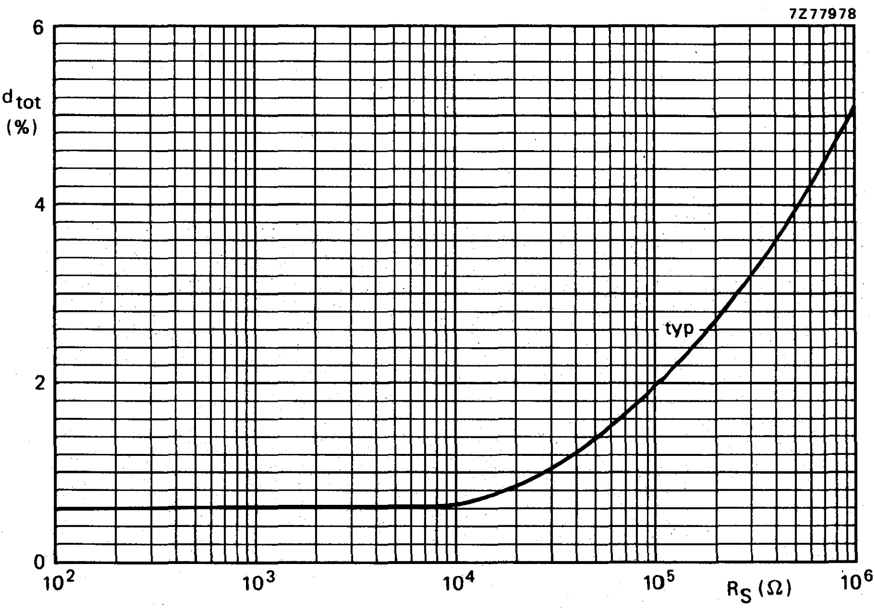


Fig. 8 Total harmonic distortion as a function of R_S in the circuit of Fig. 3; P_o = 3,5 W; f = 1 kHz.

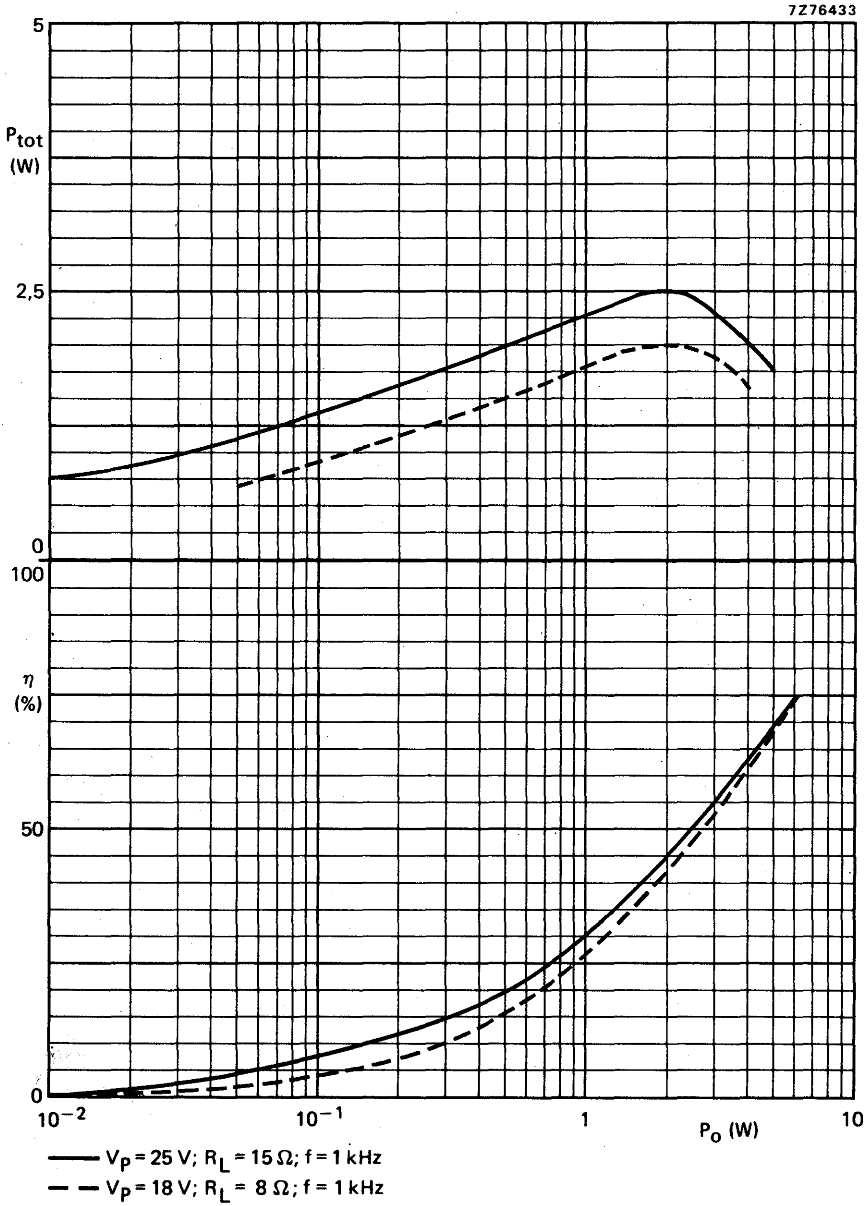


Fig. 9 Total power dissipation and efficiency as a function of output power.

APPLICATION INFORMATION

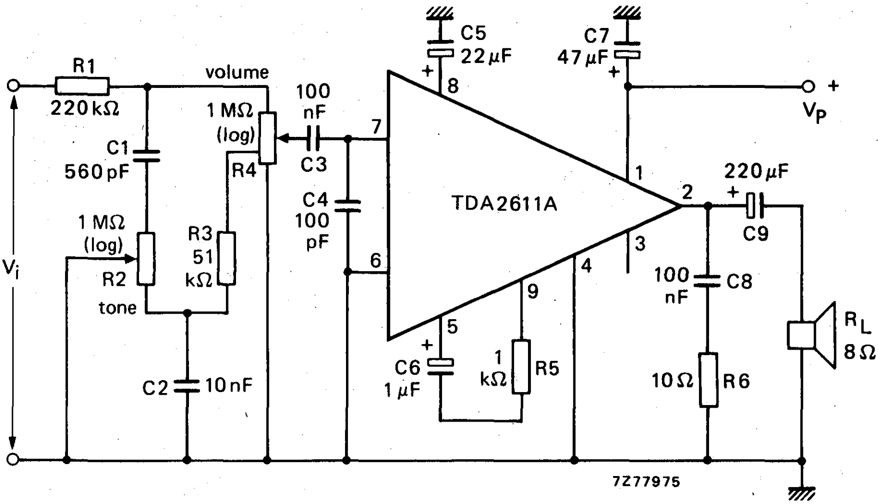


Fig. 10 Ceramic pickup amplifier circuit.

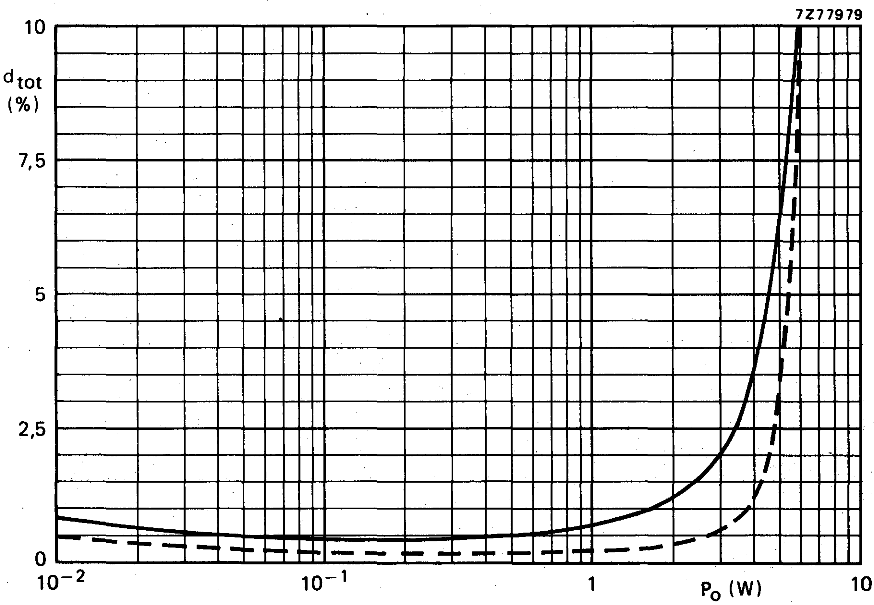


Fig. 11 Total harmonic distortion as a function of output power; —— with tone control; – – – without tone control; in circuit of Fig. 10; typical values.

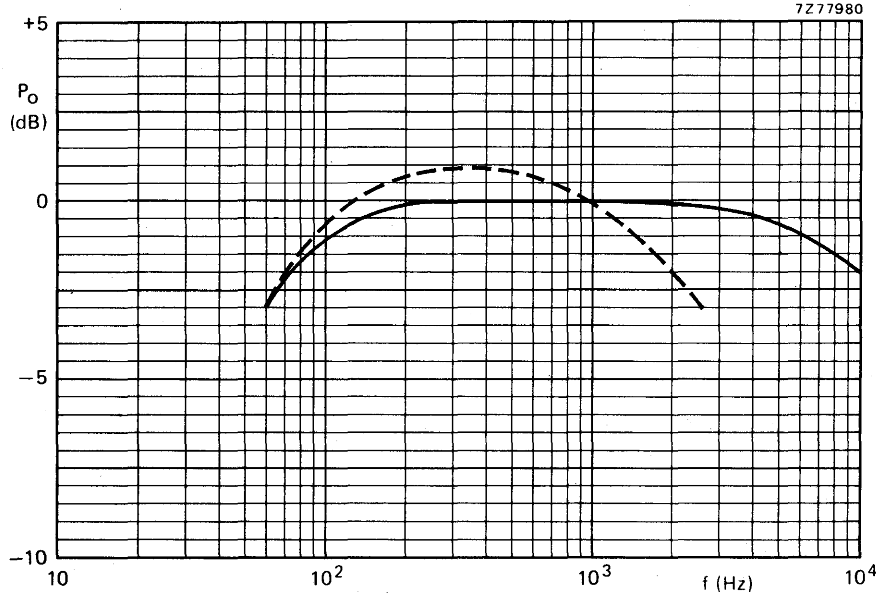


Fig. 12 Frequency characteristics of the circuit of Fig. 10; —— tone control max. high; — — — tone control min. high; P_o relative to 0 dB = 3 W; typical values.

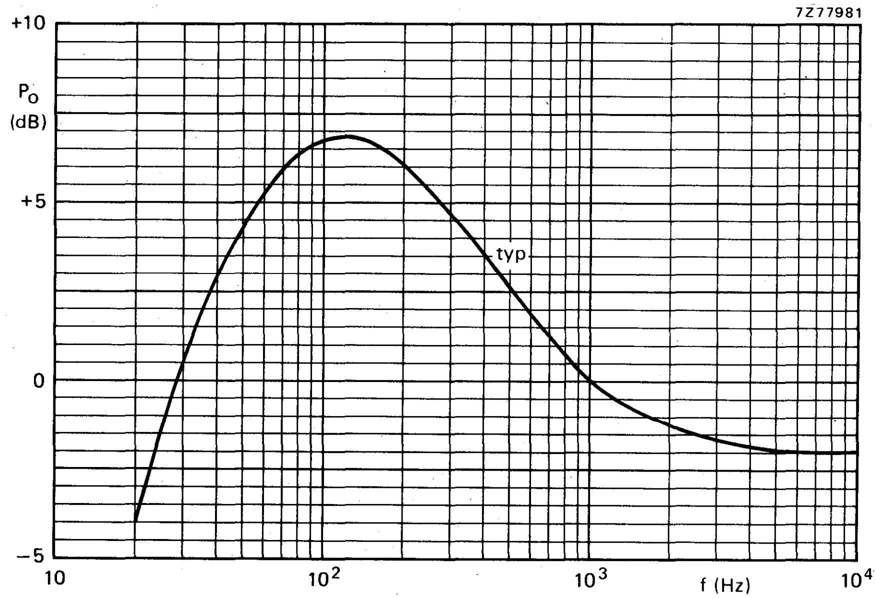


Fig. 13 Frequency characteristic of the circuit of Fig. 10; volume control at the top; tone control max. high.

INTEGRATED AM/FM RADIO RECEIVER CIRCUIT

The TDA5700 is for use in high quality battery or mains-fed a.m. and a.m./f.m. receivers as well as small low-cost a.m. portable receivers. The IC incorporates a.m. mixer, oscillator, i.f. amplifier, a.g.c. amplifier, a.m. detector and capacitor, f.m./i.f. limiting amplifier and stable base bias for f.m. front-end. The TDA5700 is pin compatible, with the h.f. part of the TBA570A. The IC has been designed to improve the distortion characteristics of the a.m. part and is very suitable in combination with ceramic filters, of which application is given.

QUICK REFERENCE DATA

Applicable supply voltage range of receiver	V_P		2,7 to 12	V
Ambient temperature	T_{amb}		25	^oC
Supply voltage at pin 8	$V_{8\text{-}16}$	nom.	5,4	V
Total quiescent current	I_{tot}	typ.	9	mA
A.M. performance (at pin 2)				
R.F. input voltage				
S/N = 26 dB	V_i	typ.	18	μV
for V_o = 10 mV	V_i	typ.	2,5	μV
A.G.C. range; change of r.f. input voltage for 10 dB expansion in audio range		typ.	65	dB
R.F. signal handling				
d_{tot} = 10%; m = 0,8	V_i	typ.	300	mV
F.M. performance (at pin 2)				
R.F. input voltage				
3 dB before limiting	V_i	typ.	125	μV

PACKAGE OUTLINES

TDA5700: 16-lead DIL; plastic (SOT-38).
TDA5700Q: 16-lead QIL; plastic (SOT-58).

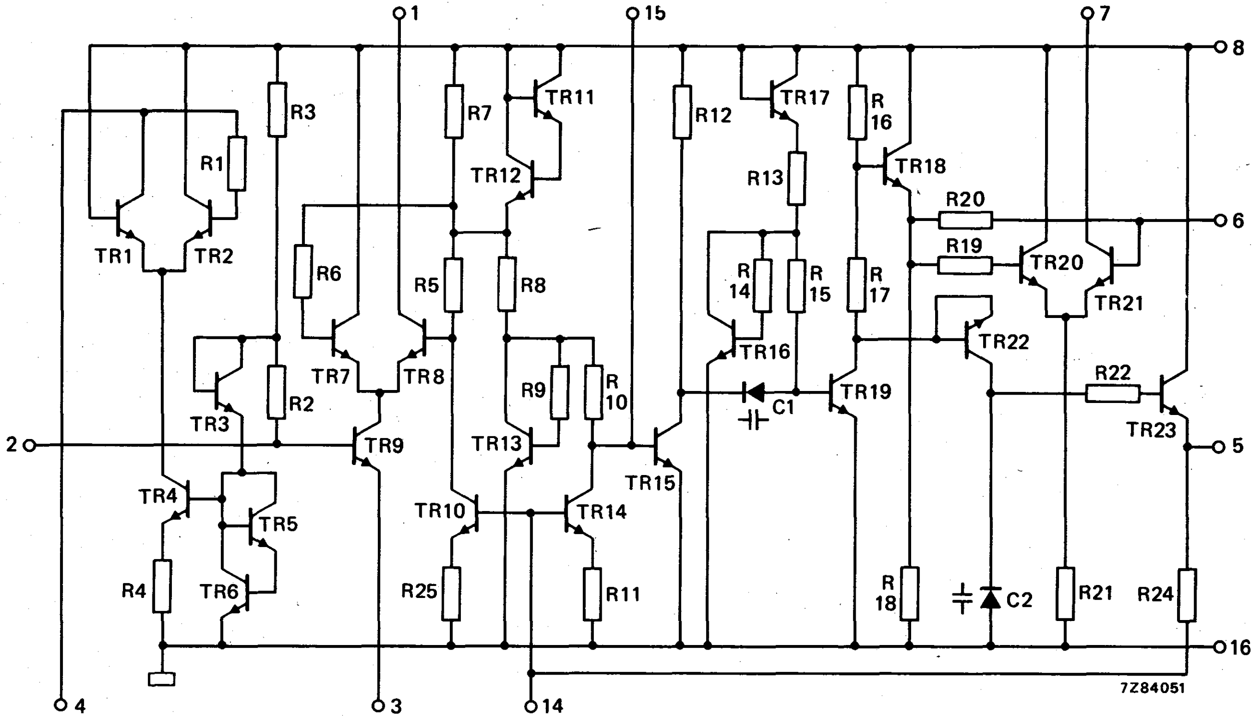


Fig. 1 Circuit diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage pin 8	$V_{8\text{-}16}$	max.	8 V
Total power dissipation	see derating curve (Fig. 2)		
Storage temperature	T_{stg}		−55 to + 150 °C
Operating ambient temperature $V_{8; 4; 7; 1\text{-}16}$ = 8 V; see also derating curve (Fig. 2)	T_{amb}		−20 to +85 °C

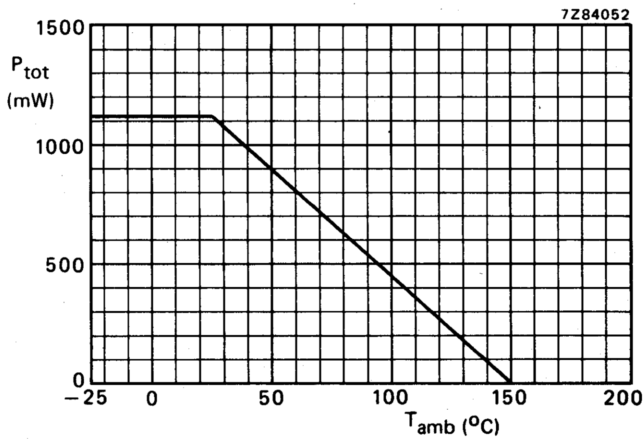


Fig. 2 Derating curve.

DESIGN DATA

Characteristics of integrated components are determined by process and layout data.

Pins not under measuring condition should not be connected.

Pins 9, 10, 11, 12 and 13 are not allowed to be connected

Voltage pins 1 and 7 *	$V_{1\text{-}16}$ $V_{7\text{-}16}$	max.	12 V
Voltage pin 4 *	$V_{4\text{-}16}$	min. max.	V_8 − 0,5 V V_8 + 0,5 V
Voltage pin 8 *	$V_{8\text{-}16}$	max.	7 V
Voltage pin 3 *	$V_{3\text{-}16}$	max.	3 V
Voltage pin 5 *	$V_{5\text{-}16}$	max.	4 V
Voltage pin 14 *	$V_{14\text{-}16}$	max.	1 V
Current pin 2, 6 and 15 *	I_2; I_6; I_{15}	max.	80 μA

* Tolerated minimum for voltages 0 V; for currents 0 mA.

D.C. CHARACTERISTICS

T_{amb} = 25 °C

Total quiescent current				
$V_{8\text{-}16}$ = 5,4 V	I_{tot}	typ.	9	mA
$V_{8\text{-}16}$ = 3,4 V	I_{tot}	typ.	8	mA
Applicable supply voltage range of receiver (note 1)	V_P		2,7 to 12	V
Base bias voltage for f.m. front-end total external load current at pin 2: $-I_2$ = 150 μA	$V_{2\text{-}16}$	typ.	1,2	V

A.C. CHARACTERISTICS

T_{amb} = 25 °C; $V_{8\text{-}16}$ = 5,4 V; I_E (TR9) = 1 mA

			0,45	1	10,7	MHz
Input conductance at pin 2	g_{ie}	typ.	–	0,3	0,4	mA/V
Output conductance at pin 1	g_{oe}	typ.	10	–	40	μA/V
Input conductance at pin 15	g_{ie}	typ.	0,5	–	1,0	mA/V

A.M. performance (in test circuit Fig. 3)

	$V_{8\text{-}16}$		5,4 V	3,4	V
R.F. input voltage; S/N = 26 dB (notes 2 and 3)	V_i	typ.	18	18	μV
R.F. input voltage for 10 mV (a.f.) across volume control	V_i	typ.	2,5	6,0	μV
A.F. voltage across volume control at 100 μV (r.f.) input voltage (notes 2 and 3)	V_o	typ.	100	100	mV
Signal-to-noise ratio at 1 mV (r.f.) input voltage (notes 2 and 3)	S/N	typ.	46	49	dB
A.G.C. range (change in r.f. input voltage for 10 dB expansion in audio range) (notes 2 and 3)		typ.	65	65	dB
R.F. signal handling capability at 80% modulation; d_{tot} < 10% (note 2)	V_i	typ.	300	100	mV
Harmonic distortion of h.f. part over most of a.g.c. range; m = 0,3; f_m = 1 kHz	d_{tot}	typ.	1	1	%
I.F. selectivity	S_9	typ.	33	33	dB
I.F. bandwidth (3 dB)	B	typ.	5	5	kHz

Notes
1. Adjustable by a dropping resistor in the V_P-line; see also maximum tolerated voltages for pins 1, 4, 7 and 8 in design data on page 3.
2. a. A.F. signal: measured across volume control.
   b. R.F. signal: measured at pin 2 at source impedance of 50 Ω.
   c. f_o = 1 MHz; f_m = 1 kHz.
3. m = 0,3.

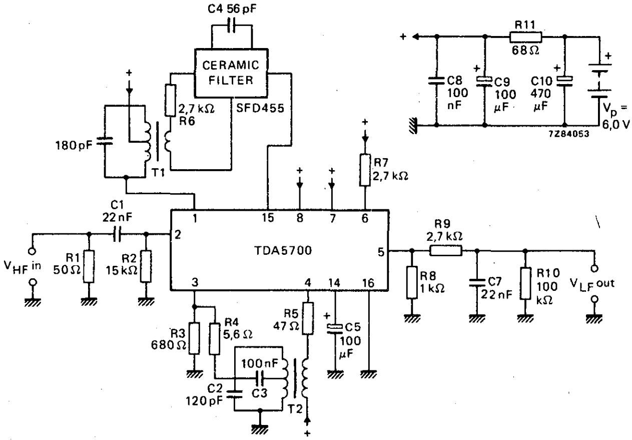
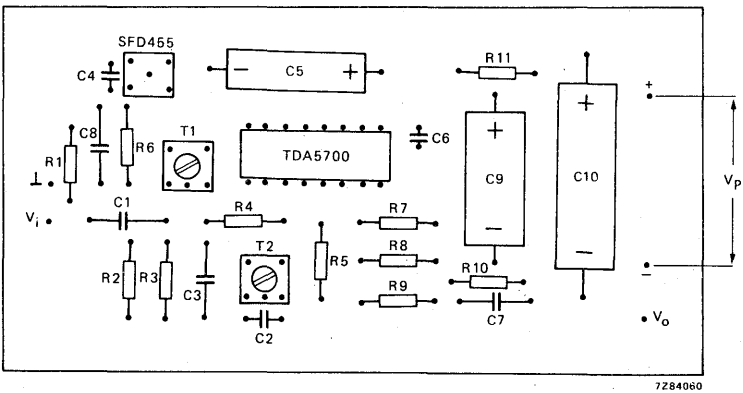


Fig. 3 A.M. performance test circuit.



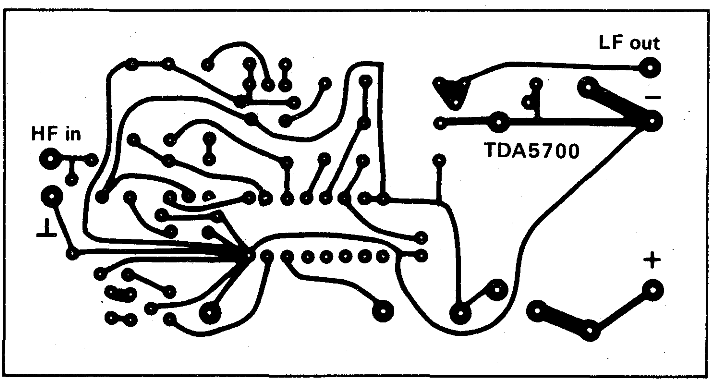


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Fig. 4 Component side of printed-circuit board (test circuit Fig. 3).
Fig. 5 Track side of printed-circuit board (test circuit Fig. 3).

F.M. performance test circuit (Fig. 6)

T_{amb} = 25 °C; V_{8-16} = 5,4 V; f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 1 kHz; R_S = 50 Ω; unless otherwise specified.

Sensitivity for an f.m. signal 3 dB before limiting				
at pin 2	V_i	typ.	125	µV
at pin 15	V_i	typ.	500	µV
A.F. output voltage across a load of 100 kΩ	V_o	typ.	140	mV
Signal-to-noise ratio over most of signal range	S/N	typ.	65	dB
A.F. signal distortion 3 dB before i.f. limiting (note 1)	d_{tot}	typ.	0,5	%

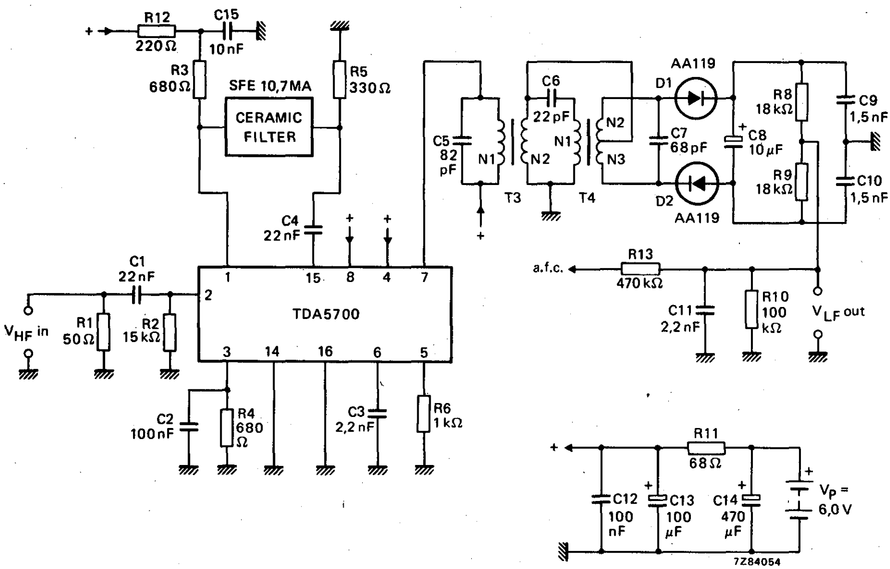

Fig. 6 Test circuit f.m. performance.

1. Δf = ± 40 kHz; measured with V_o at maximum.

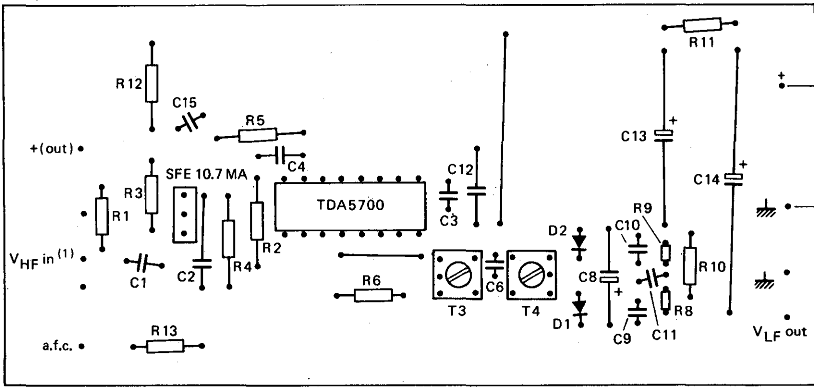

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Fig. 7 Component side of printed-circuit board (test circuit Fig. 6).

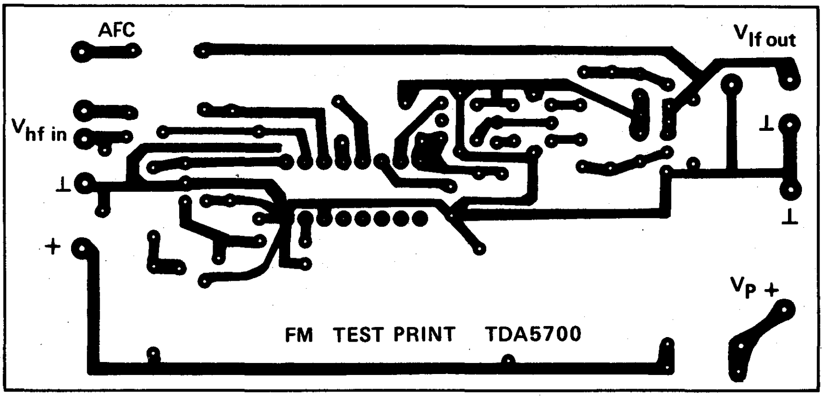

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Fig. 8 Track side of printed-circuit board; (test circuit Fig. 6).

APPLICATION INFORMATION

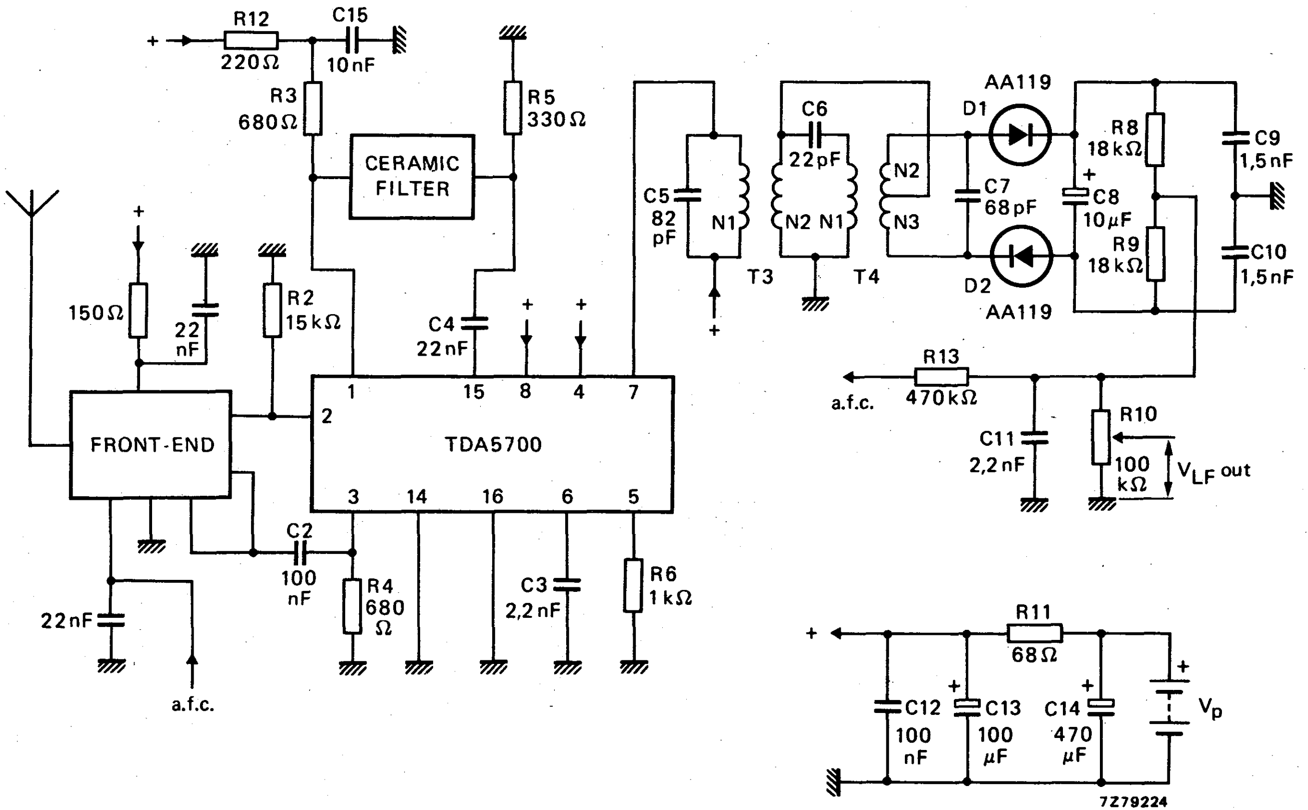


Fig. 9 Performance of an f.m. circuit including the f.m. tuner.

APPLICATION INFORMATION (continued)

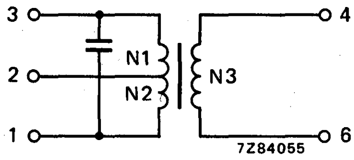
F.M. performance of the complete f.m. circuit measured at V_P = 6,0 V.

Sensitivity for an f.m. signal 3 dB before limiting				
at 75 Ω aerial input of the f.m. front-end (note 1)	V_i	typ.	12,5	μV
at pin 2; first i.f. input (notes 2 and 6)	V_i	typ.	125	μV
Sensitivity for 26 dB S/N ratio at 75 Ω aerial input of the f.m. front-end (note 1)	V_i	typ.	3	μV
A.F. output voltage across a volume control of 100 kΩ at an i.f. signal beyond limiting	V_o	typ.	140	mV
Signal-to-noise over most of the signal range	S/N	typ.	65	dB
A.M. suppression over most of the signal range (note 3)	S/N	typ.	60	dB
I.F. selectivity (note 4)	S_{300}	typ.	55	dB
I.F. bandwidth (3 dB; note 4)	B	typ.	180	kHz
A.F. distortion at an i.f. signal level 3 dB before limiting (note 5)	d_{tot}	typ.	0,5	%

Notes
1. Aerial e.m.f. (V_i) at f_o = 98 MHz; R_S = 75 Ω; Δf = ± 22,5 kHz; f_m = 1 kHz.
2. f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 1 kHz.
3. A.M. signal: m = 0,3; f_m = 1 kHz.
   F.M. signal: f_o = 10,7 MHz; Δf = ± 75 kHz; f_m = 70 Hz.
   Carrier simultaneously modulated with a.m. and f.m.
4. Including the ratio detector, measured at N1 of the secondary coil of the ratio detector.
   Level of measurement: 3 dB before limiting.
5. f_o = 98 MHz; Δf = 40 kHz; f_m = 1 kHz.
   Measurement carried out selectively to avoid noise influence on meter reading.
6. Pin 3 bypassed to ground with a capacitor of 220 nF.

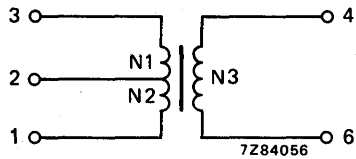
COIL DATA

A.M. – i.f. coils (Fig. 3)



N1 = 86 t.
N2 = 60 t.
C = 180 pF.
N3 = 8 t.

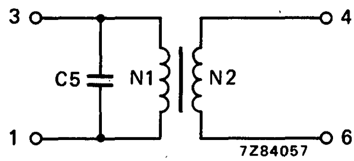
Fig. 10 I.F. bandpass filter (L1). TOKO sample no. 7 MCS-A 3544 EK. L = 680 μH at 455 kHz; Q_o = 110.



N1 = 55 t.
N2 = 2 t.
N3 = 9 t.

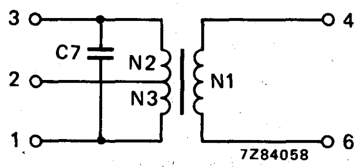
Fig. 11 Oscillator coil (L2). TOKO sample no. 7 BOS-A 3498 EK. L = 115 μH at 796 kHz; Q_o = 110.

F.M. – i.f. coils (Figs 6 and 9)



N1 = 11 t.
N2 = 5 t.
C5 = 82 pF.

Fig. 12 Primary ratio detector coil (L3). TOKO sample no. 119 ACS-A 3503 AO. L = 2,7 μH at 10,7 MHz; Q_o = 90.



N3 = 6 t.
N2 = 6 t.
C7 = 68 pF.
N1 = 2 t.

Fig. 13 Secondary ratio detector coil (L4). TOKO sample no. 119 ACS-A 3258 EK. L = 3,25 μH at 10,7 MHz; Q_o = 85.

AM CAR RADIO RECEIVER CIRCUIT

The TEA5550 is a monolithic integrated radio circuit, primarily intended for use in car radios. The IC can reduce the costs in a car radio due to the following features:

- minimum periphery
- ceramic filter application
- simple a.m./f.m. switching possibility

The TEA5550 incorporates the following functions:

- a double balanced mixer with large signal handling and common mode rejection properties
- a 'one-pin' oscillator, permitting the application of a variable capacitance diode
- an i.f. amplifier, designed for ceramic filters
- an a.m. envelope detector
- a.g.c. stages
- a voltage stabilizer, for the internal circuit current and an external current up to 20 mA
- a simple d.c. switch for a.m./f.m. radios

QUICK REFERENCE DATA

Supply voltage range (pin 8)	V_P		10,2 to 16	V
Ambient temperature	T_{amb}	typ.	25	°C
Supply voltage (pin 8)	V_P	typ.	14,4	V
R.F. input voltage (pin 1)				
V_o = 30 mV	V_i	typ.	4	μV
S/N = 26 dB	V_i	typ.	13	μV
S/N = 46 dB	V_i	typ.	160	μV
A.F. output voltage (pin 10)				
V_i = 1 mV	V_o	typ.	180	mV
Total harmonic distortion; m = 0,8; V_i = 1 mV	THD	<	2,5	%
R.F. signal handling				
THD < 10%; m = 0,8	V_i	typ.	400	mV

PACKAGE OUTLINE

16-lead DIL; plastic (SOT-38).

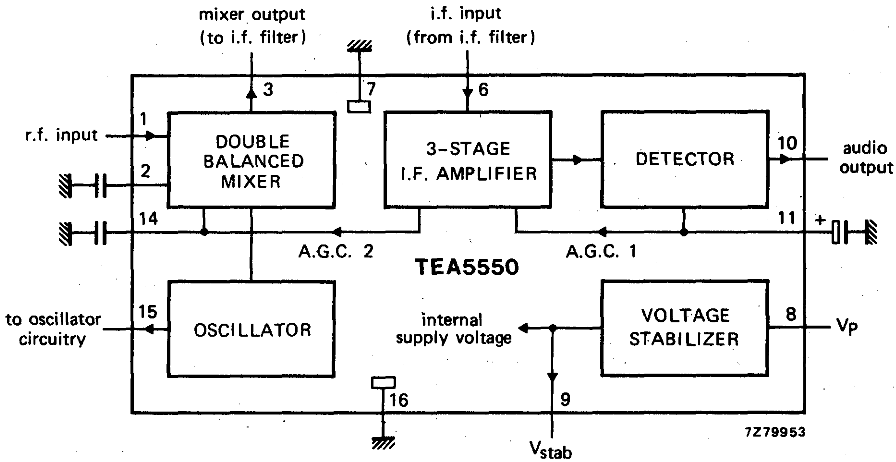


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages			
pin 8	$V_P = V_{8\text{-}16}$	max.	24 V
pin 3	$V_{3\text{-}16}$	max.	24 V
Non-repetitive peak output current (pin 9)	I_{9SM}	max.	100 mA
Total power dissipation	P_{tot}	max.	1100 mW
Storage temperature	T_{stg}		−65 to + 150 °C
Operating ambient temperature	T_{amb}		−30 to + 85 °C

D.C. CHARACTERISTICS at $V_i = 0$

$V_P = 14,4$ V; $T_{amb} = 25$ °C; measured in Fig. 2

Supply voltage range (unstabilized)*	V_P		10,2 to 16 V
Voltage at pin 9; $-I_9 = 0$	$V_{9\text{-}16}$	typ.	8 V
			7,5 to 9 V
Voltage at pin 10	$V_{10\text{-}16}$	typ.	1,2 V
Voltage at pins 1 and 2	$V_{1\text{-}16} = V_{2\text{-}16}$	typ.	5,2 V

*A stabilized supply voltage of 7 to 9 V can also be applied at pin 9 instead of V_P (pin 8).

Total supply current; $-I_9 = 0$	I_{tot}	typ.	20	mA
Current drain				
pin 3	I_3	typ.	1	mA
pin 15	I_{15}	typ.	0,2	mA
Current supplied from pin 9	$-I_9$	<	20	mA
Power dissipation; $-I_9 = 0$	P	typ.	300	mW

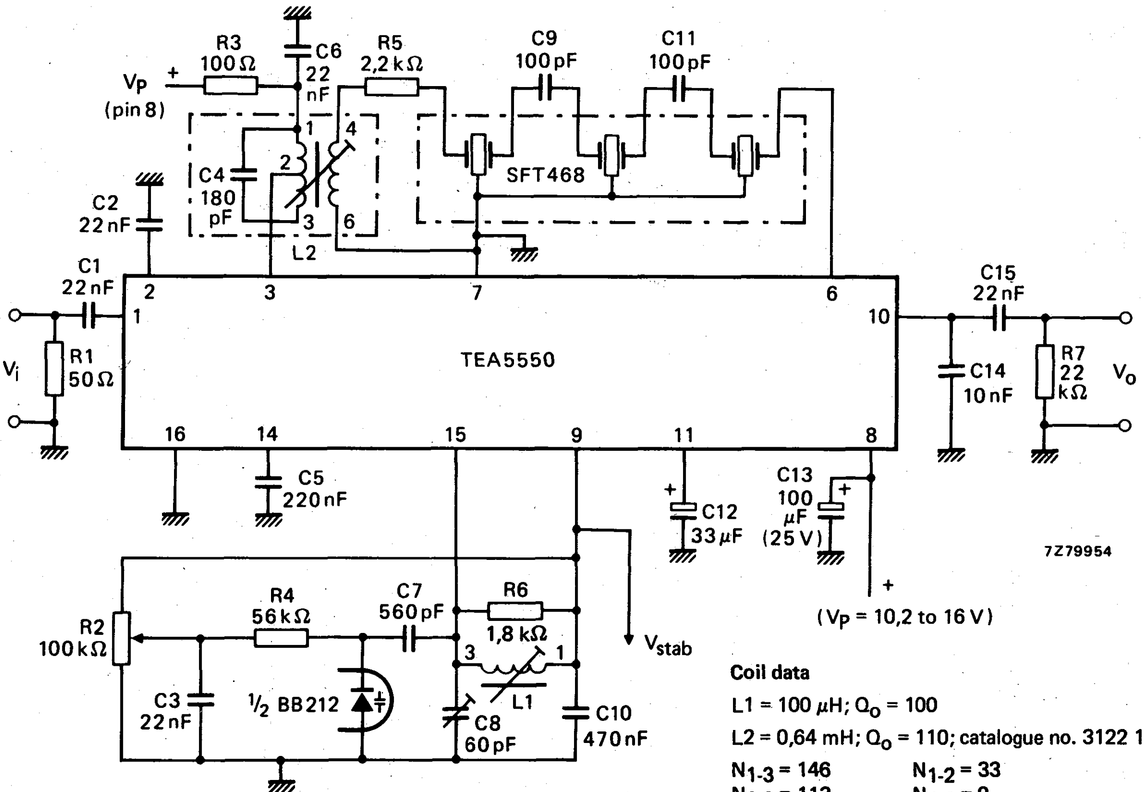
A.C. CHARACTERISTICS

V_P = 14,4 V; T_{amb} = 25 °C; r.f. condition: f_i = 1 MHz, m = 0,3, f_m = 1 kHz; measured in Fig. 2; unless otherwise specified

R.F. input voltage; V_o = 30 mV	V_i		2,5 to 5,5	μV
H.F. sensitivity for:				
S/N = 6 dB	V_i	typ.	1,3	μV
S/N = 26 dB	V_i	<	16	μV
S/N = 46 dB	V_i	typ.	160	μV
S/N = 50 dB	V_i	typ.	350	μV
Input conductance at pin 1				
V_i = 0,1 mV	g_{ie}	typ.	0,2	mS
V_i = 100 mV	g_{ie}	typ.	0,1	mS
Input conductance at pin 6	g_{ie}	typ.	0,3	mS
Change in r.f. input voltage for 10 dB change in a.f. output voltage; V_{i1} = 200 mV	V_{i1}/V_{i2}	typ.	86	dB
A.F. output voltage				
V_i = 1 mV	V_o	>	160	mV
		typ.	180	mV
A.F. output impedance (pin 10)	$\lvert Z_o \rvert$	typ.	2,7	kΩ
Total harmonic distortion at m = 0,8				
V_i = 16 μV	THD	<	2,5	%
V_i = 1 mV	THD	typ.	1,2	%
V_i = 2,5 mV	THD	<	2,5	%
R.F. signal handling				
THD < 10%; m = 0,8	V_i	>	350	mV
		typ.	400	mV
I.F. suppression				
V_o = 30 mV; without input selection	α	>	20	dB*
Oscillator voltage				
$V_{9\text{-}16}$ = 8 V; f_{osc} = 1468 kHz	$V_{15\text{-}8}$	<	250	mV

* $\alpha = 20 \log \frac{V_{i1}}{V_{i2}}$, where: V_{i1} is input voltage at f = 468 kHz and V_{i2} is input voltage at f = 1 MHz.

DEVELOPMENT SAMPLE DATA



Coil data

L1 = 100 µH; Q_o = 100

L2 = 0,64 mH; Q_o = 110; catalogue no. 3122 138 91481

$N_{1\text{-}3}$ = 146 $N_{1\text{-}2}$ = 33

$N_{2\text{-}3}$ = 113 $N_{4\text{-}6}$ = 9

Fig. 2 AM test circuit; for printed-circuit board see Figs 3 and 4.

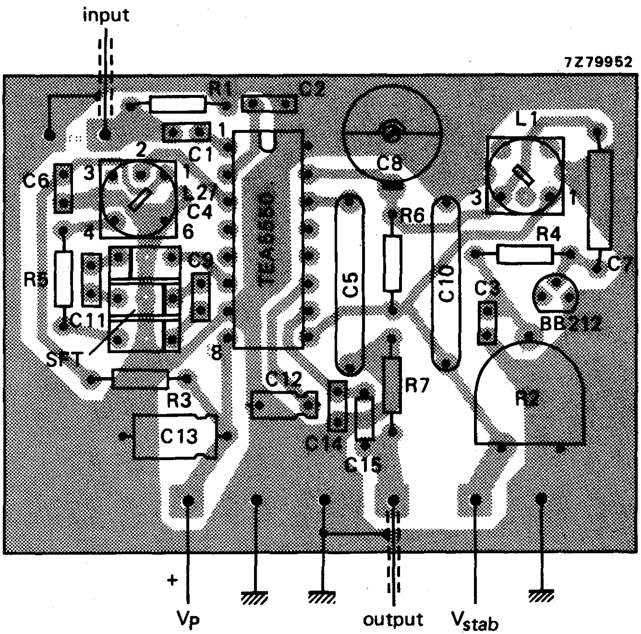


Fig. 3 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 2.

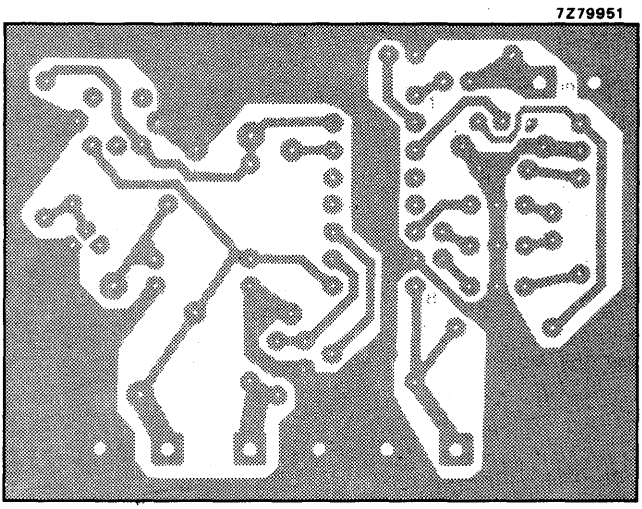


Fig. 4 Printed-circuit board showing track side.

FM/IF SYSTEM

The TEA5560 is a monolithic integrated f.m./i.f. system circuit, intended for car radios and home-receivers equipped with a ratio detector.
The system incorporates the following functions:

- a three-stage i.f. limiting amplifier
- a 15 dB field-strength dependent muting circuit
- a field-strength dependent d.c. voltage for e.g.:
  mono/stereo switching
  channel separation control of a stereo decoder
  an indicator ($I_{max} \leqslant 1$ mA)
- standby ON/OFF switching circuit
- a voltage stabilizer, for the internal circuit current and an external current up to 10 mA
- adjustable gain (ΔG = 15 dB)

QUICK REFERENCE DATA

Supply voltage range (pin 6)	V_P		10,2 to 16	V
Ambient temperature	T_{amb}	typ.	25	°C
Supply voltage (pin 6)	V_P	typ.	14,4	V
Frequency	f_o		10,7	MHz
Sensitivity (3 dB limiting)	V_i	typ.	150	µV
Signal-to-noise ratio for V_i = 10 mV	S/N	>	70	dB
A.F. output voltage at Δf = ± 22,5 kHz	V_o	typ.	190	mV
Total harmonic distortion; Δf = ± 22,5 kHz	THD	typ.	0,35	%
A.M. suppression a.m. signal: m = 0,3; f_m = 1 kHz f.m. signal: Δf = ± 22,5 kHz; f_m = 70 Hz	α	typ.	50	dB

PACKAGE OUTLINE

9-lead SIL; plastic (SOT-142).

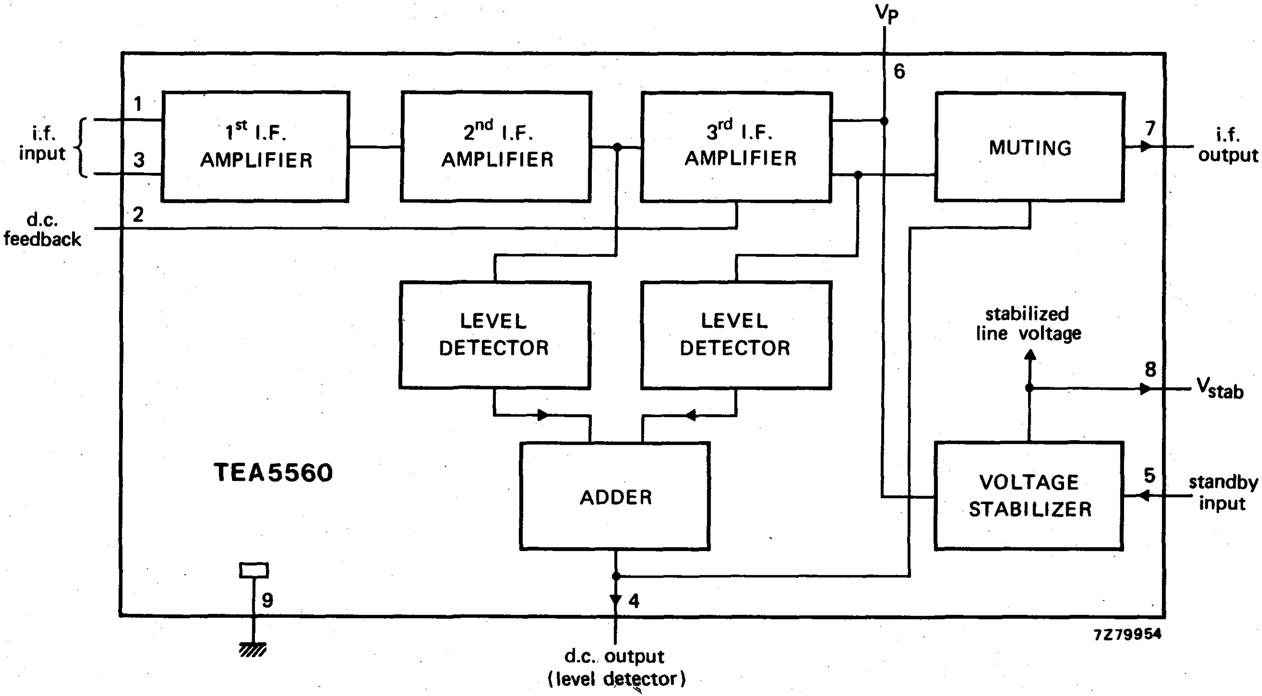


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages				
pin 6	$V_P = V_{6\text{-}9}$	max.	24	V
pin 7	$V_{7\text{-}9}$	max.	24	V
Voltage at pin 4	$V_{4\text{-}9}$	max.	7	V
Voltage at pin 5	$V_{5\text{-}9}$	max.	9	V
Non-repetitive peak output current (pin 8)	$-I_{8SM}$	max.	100	mA
Total power dissipation	P_{tot}	max.	1000	mW
Storage temperature	T_{stg}		−65 to + 150	°C
Operating ambient temperature	T_{amb}		−30 to + 85	°C

D.C. CHARACTERISTICS at $V_i = 0$

$V_P = 14{,}4$ V; $T_{amb} = 25$ °C; measured in Fig. 2

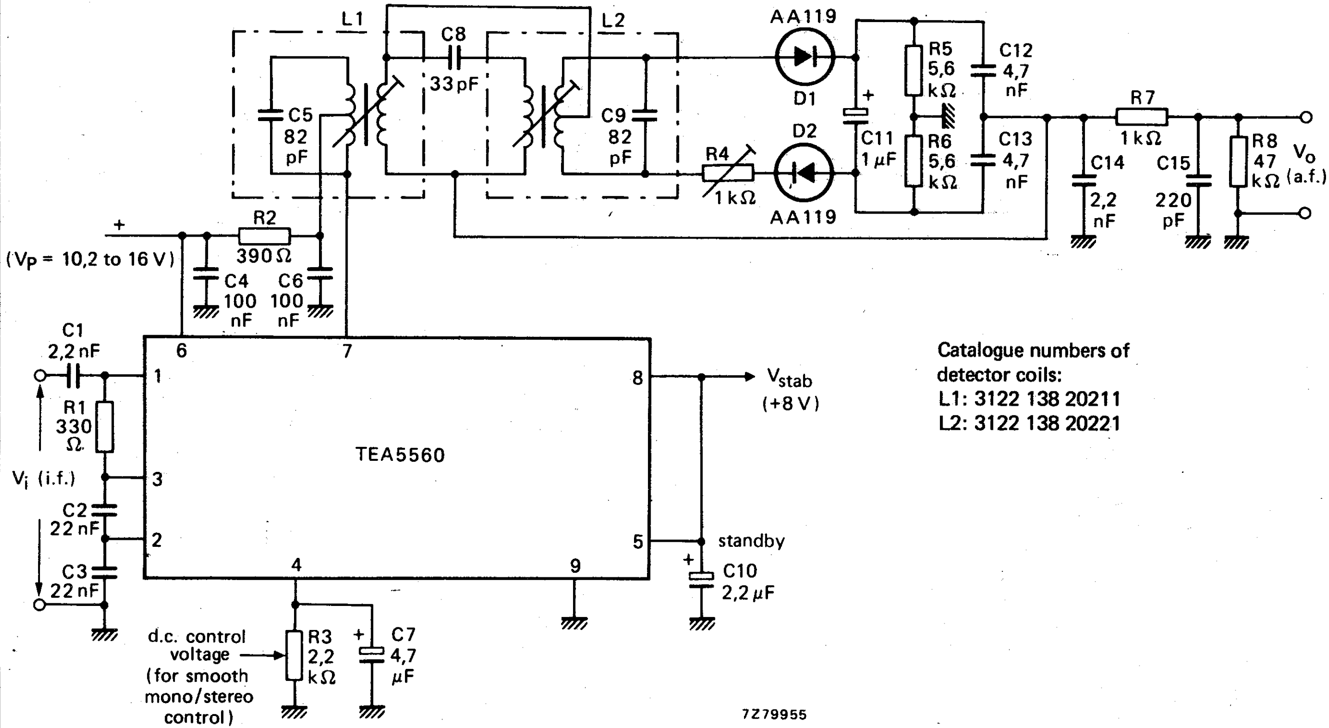
Supply voltage range (unstabilized, pin 6)*	V_P		10,2 to 16	V
Voltage at pin 8	$V_{8\text{-}9}$	typ.	8	V
Voltage at pin 4 (level detector)	$V_{4\text{-}9}$	<	100	mV
Voltage at pins 1, 2 and 3	$V_{1;\,2;\,3\text{-}9}$	typ.	2,3	V
Total supply current				
$-I_8 = 0$	I_{tot}	typ.	20	mA
$V_{5\text{-}9} = 0$	I_{tot}	typ.	11	mA
Current supplied from pin 8	$-I_8$	<	10	mA
Current into pin 5	I_5	typ.	1,5	mA
Current into pin 7	I_7	typ.	3,5	mA
Power dissipation; $-I_8 = 0$	P	typ.	300	mW

* A stabilized supply voltage of 7 to 9 V can also be applied at pins 5 and 6 (linked); in that case pin 8 must be not connected.

A.C. CHARACTERISTICS

V_P = 14,4 V; T_{amb} = 25 °C; V_i = 1 mV; f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 1 kHz; measured in Fig. 2; unless otherwise specified

I.F. part and ratio detector				
Sensitivity at −3 dB before limiting (pin 1)	V_i	typ.	150	μV
			85 to 210	μV
A.F. output voltage				
Δf = ± 22,5 kHz	V_o	typ.	190	mV
Δf = ± 75 kHz	V_o	typ.	600	mV
Total harmonic distortion				
Δf = ± 22,5 kHz	THD	typ.	0,35	%
Δf = ± 75 kHz	THD	typ.	1,7	%
A.M. suppression				
a.m. signal: m = 0,3; f_m = 1 kHz				
f.m. signal: Δf = ± 22,5 kHz; f_m = 70 Hz	α	typ.	50	dB
H.F. sensitivity at B = 300 Hz to 15 kHz for a signal-to-noise ratio of:				
S/N = 26 dB	V_i	typ.	4	μV
S/N = 70 dB	V_i	>	1	mV
Level detector circuit				
D.C. output voltage at pin 4				
V_i = 200 μV	V_{4-9}	typ.	1,4	V
V_i = 500 μV	V_{4-9}	typ.	2,0	V
V_i = 1 mV	V_{4-9}	typ.	2,6	V
V_i = 10 mV	V_{4-9}	typ.	4,5	V
Muting circuit				
Output voltage ratio at V_i = 3 μV with muting: V_{4-9} < 0,3 V and without muting: V_{4-9} = 1 V	α_{vo}	typ.	15	dB
Stabilizer circuit				
Voltage at pin 8; $-I_8$ = 0	V_{8-9}		7,6 to 8,2	V
Maximum current supplied from pin 8	$-I_8$	<	10	mA



Catalogue numbers of detector coils:
L1: 3122 138 20211
L2: 3122 138 20221

Fig. 2 F.M. test circuit; for printed-circuit board see Figs 3 and 4.

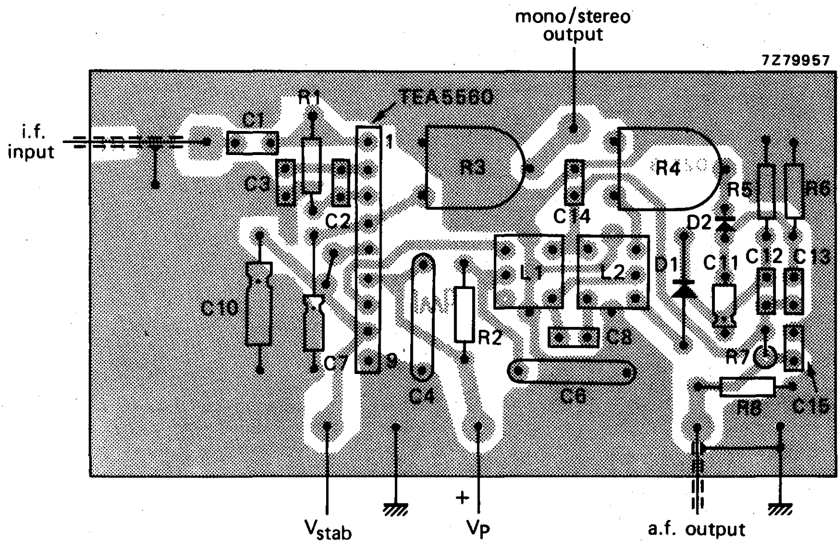


Fig. 3 Printed-circuit board component side, showing component layout. For circuit diagram see Fig. 2.

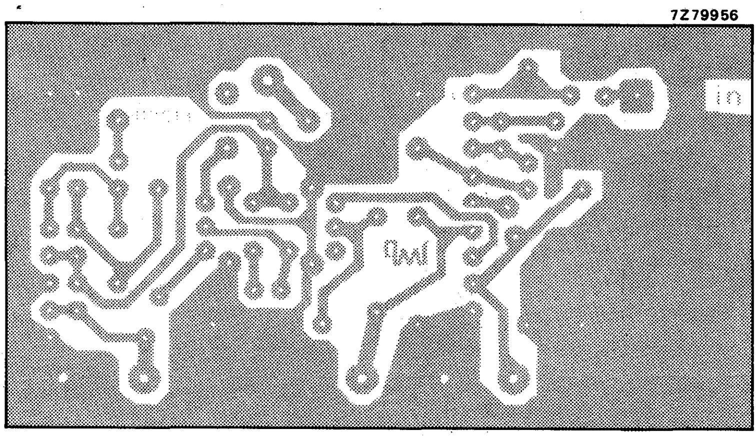


Fig. 4 Printed-circuit board showing track side.

BIPOLAR ICs FOR RADIO AND AUDIO EQUIPMENT

FUNCTIONAL AND NUMERICAL INDEX
MAINTENANCE TYPE LIST

GENERAL

PACKAGE OUTLINES

INTRODUCTION

DEVICE DATA

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United States: (Active devices & Materials) AMPEREX SALES CORP., Providence Pike, SLATERSVILLE, R.I. 02876, Tel. (401) 762-9000.
(Passive devices) MEPCO/ELECTRA INC., Columbia Rd., MORRISTOWN, N.J. 07960, Tel. (201) 539-2000.
(IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, California 94086, Tel. (408) 739-7700.
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Venezuela: IND. VENEZOLANAS PHILIPS S.A., Elcoma Dept., A. Ppal de los Ruices, Edif. Centro Colgate, CARACAS, Tel. 36 05 11.

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