

# DATA SHEET

## **PCF8574**

Remote 8-bit I/O expander for  
I<sup>2</sup>C-bus

Product specification  
Supersedes data of May 1989  
File under Integrated Circuits, IC12

September 1994

**Philips Semiconductors**



**PHILIPS**

Remote 8-bit I/O expander for I<sup>2</sup>C-bus

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## FEATURES

- Operating supply voltage 2.5 to 6 V
- Low standby current consumption of 10  $\mu$ A maximum
- I<sup>2</sup>C to parallel port expander
- Open-drain interrupt output
- 8-bit remote I/O Port for the I<sup>2</sup>C-bus
- Compatible with most microcontrollers
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)
- DIP16, space-saving SO16 or SSOP20 package.



The device consists of an 8-bit quasi-bidirectional Port and an I<sup>2</sup>C interface. The PCF8574 has a low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which can be connected to the interrupt logic of the microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C-bus. This means that the PCF8574 can remain a simple slave device.

## GENERAL DESCRIPTION

The PCF8574 is a silicon CMOS circuit. It provides general purpose remote I/O expansion for most microcontroller families via the two-line bidirectional bus (I<sup>2</sup>C).

The PCF8574 and PCF8574A versions differ only in their slave address as shown in Fig.9.

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8574P; PCF8574AP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-1
PCF8574T; PCF8574AT	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCF8574TS	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

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## BLOCK DIAGRAM

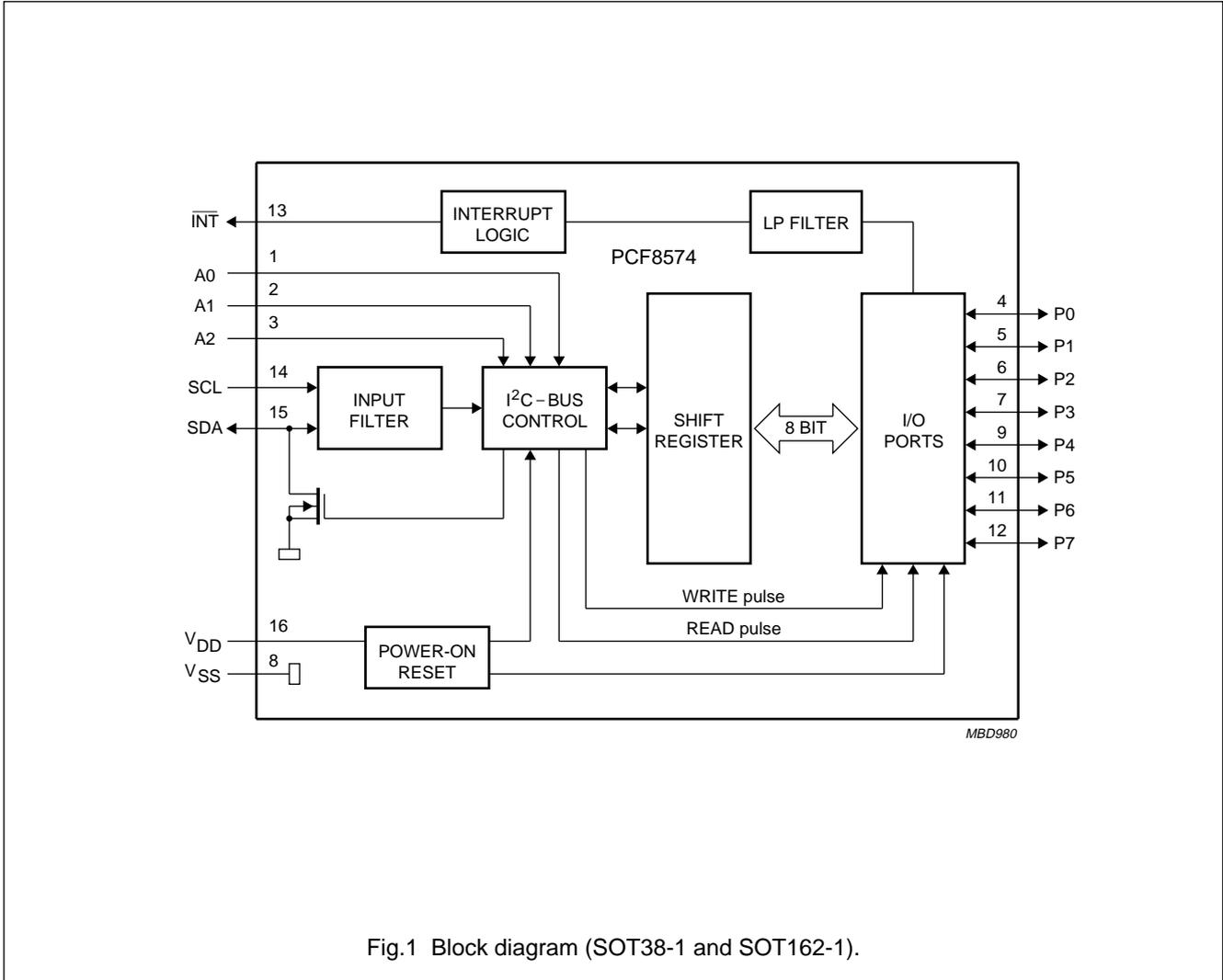


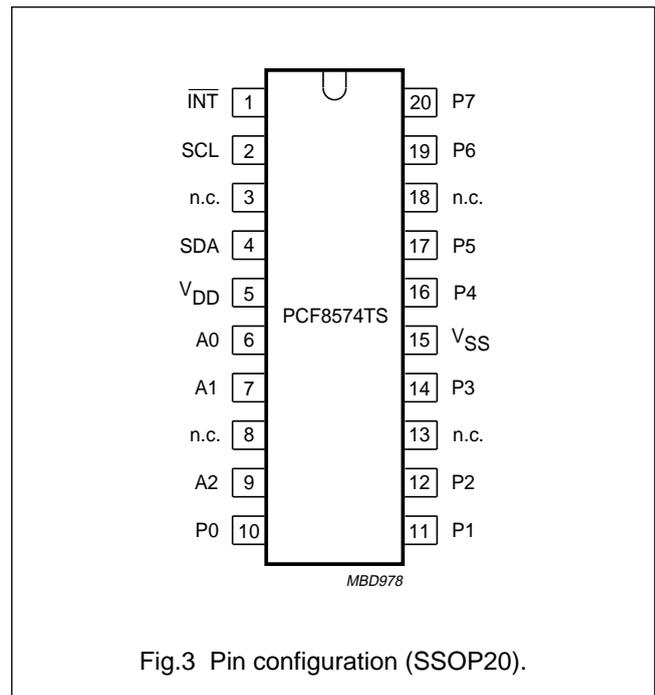
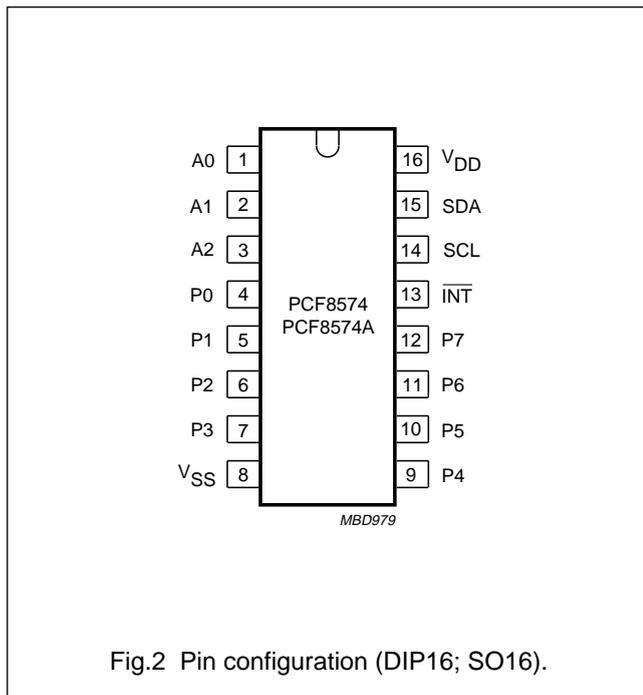
Fig.1 Block diagram (SOT38-1 and SOT162-1).

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## PINNING

SYMBOL	PIN		DESCRIPTION
	DIP16; SO16	SSOP20	
A0	1	6	address input 0
A1	2	7	address input 1
A2	3	9	address input 2
P0	4	10	quasi-bidirectional I/O Port 0
P1	5	11	quasi-bidirectional I/O Port 1
P2	6	12	quasi-bidirectional I/O Port 2
P3	7	14	quasi-bidirectional I/O Port 3
V <sub>SS</sub>	8	15	supply ground
P4	9	16	quasi-bidirectional I/O Port 4
P5	10	17	quasi-bidirectional I/O Port 5
P6	11	19	quasi-bidirectional I/O Port 6
P7	12	20	quasi-bidirectional I/O Port 7
$\overline{\text{INT}}$	13	1	interrupt output (active LOW)
SCL	14	2	serial clock line
SDA	15	4	serial data line
V <sub>DD</sub>	16	5	supply voltage
n.c.	–	3	not connected
n.c.	–	8	not connected
n.c.	–	13	not connected
n.c.	–	18	not connected



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### CHARACTERISTICS OF THE I<sup>2</sup>C-BUS

The I<sup>2</sup>C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

#### Bit transfer

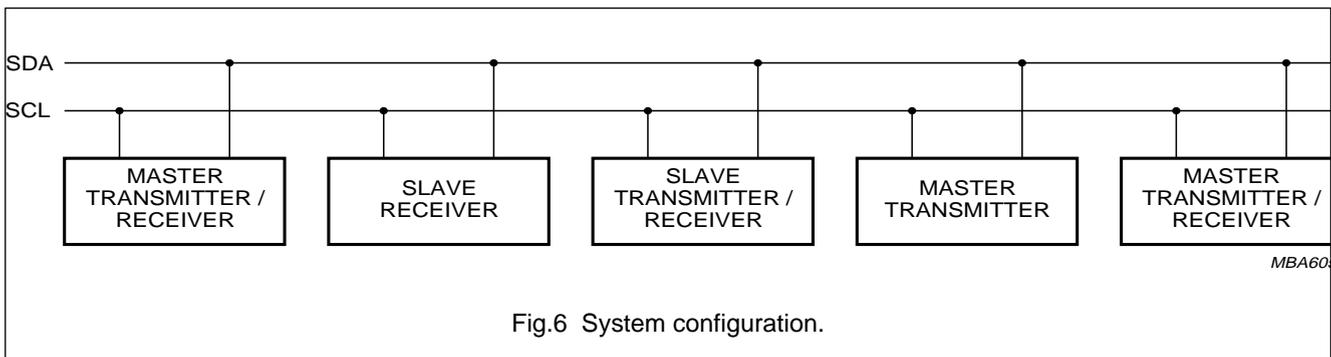
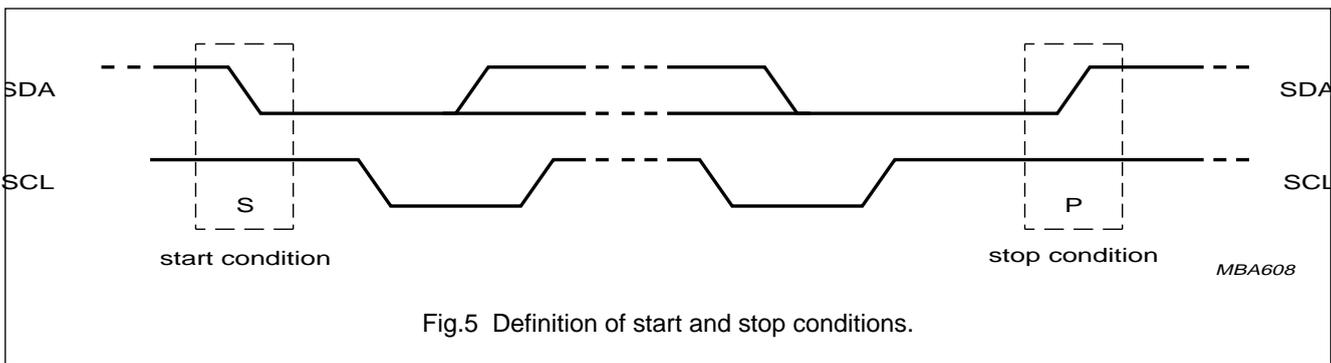
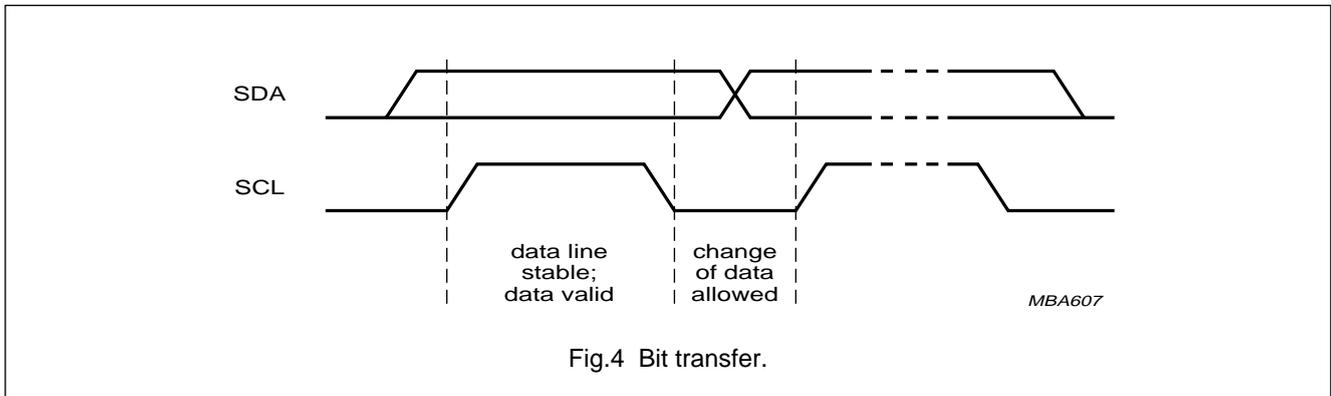
One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Fig.4).

#### Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P) (see Fig.5).

#### System configuration

A device generating a message is a 'transmitter', a device receiving is the 'receiver'. The device that controls the message is the 'master' and the devices which are controlled by the master are the 'slaves' (see Fig.6).



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### Acknowledge

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave

transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

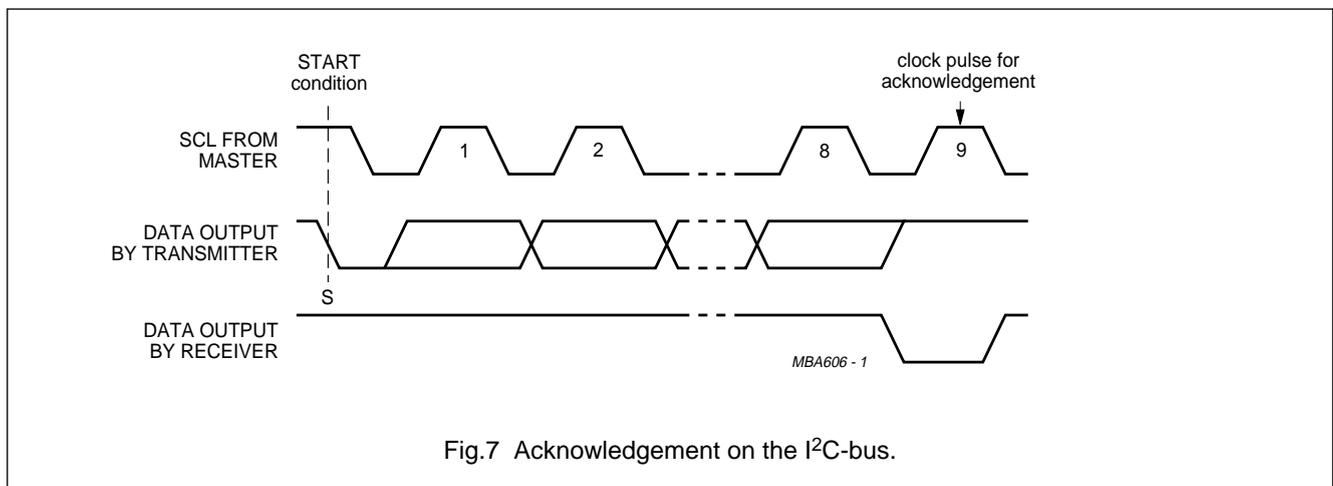
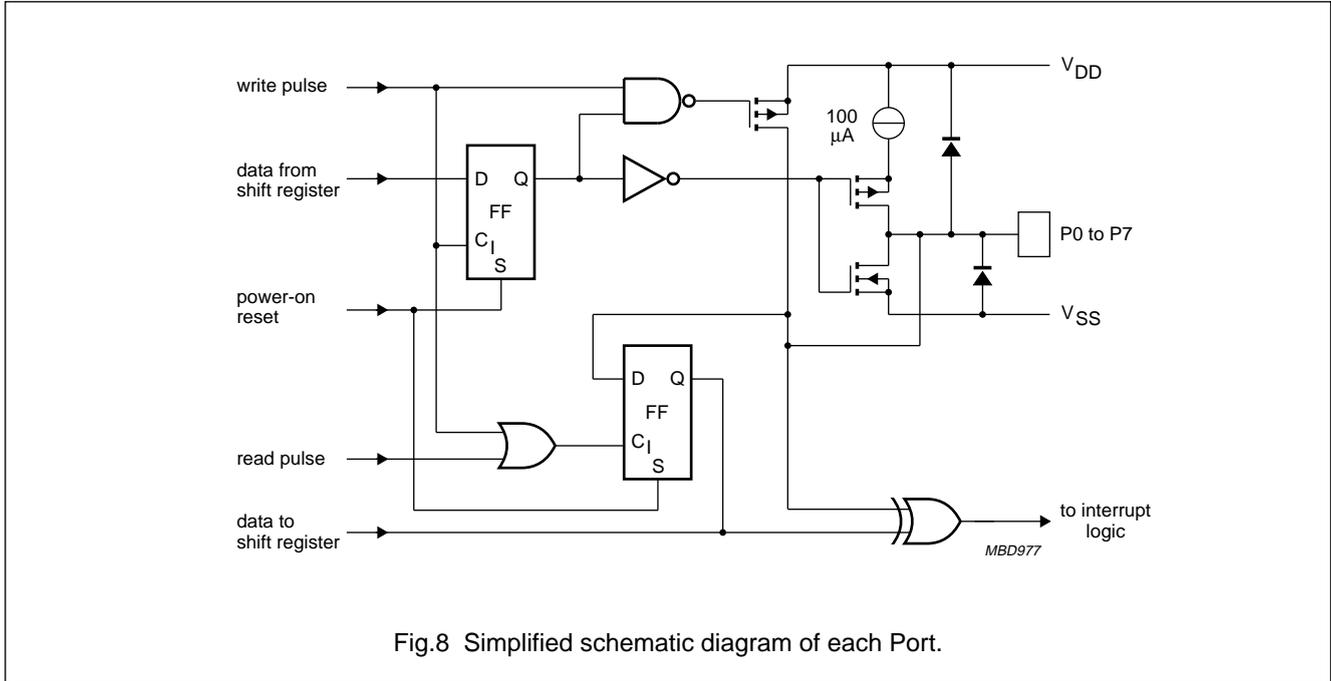


Fig.7 Acknowledgement on the I<sup>2</sup>C-bus.

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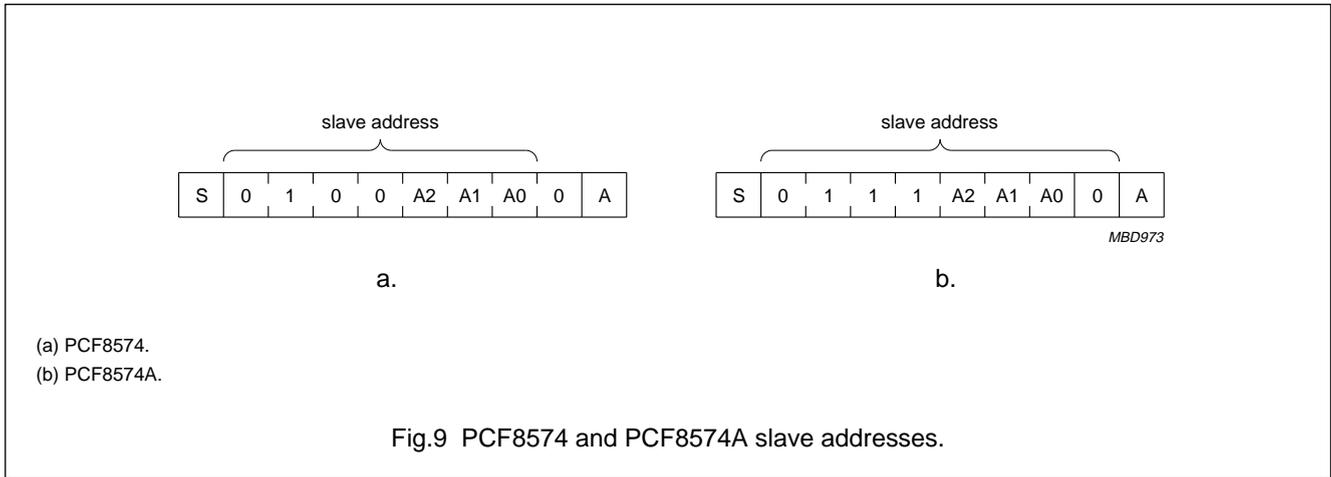
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FUNCTIONAL DESCRIPTION



Addressing

For addressing see Figs 9, 10 and 11.



Each bit of the PCF8574 I/O Port can be independently used as an input or output. Input data is transferred from the Port to the microcontroller by the READ mode (see Fig.11). Output data is transmitted to the Port by the WRITE mode (see Fig.10).

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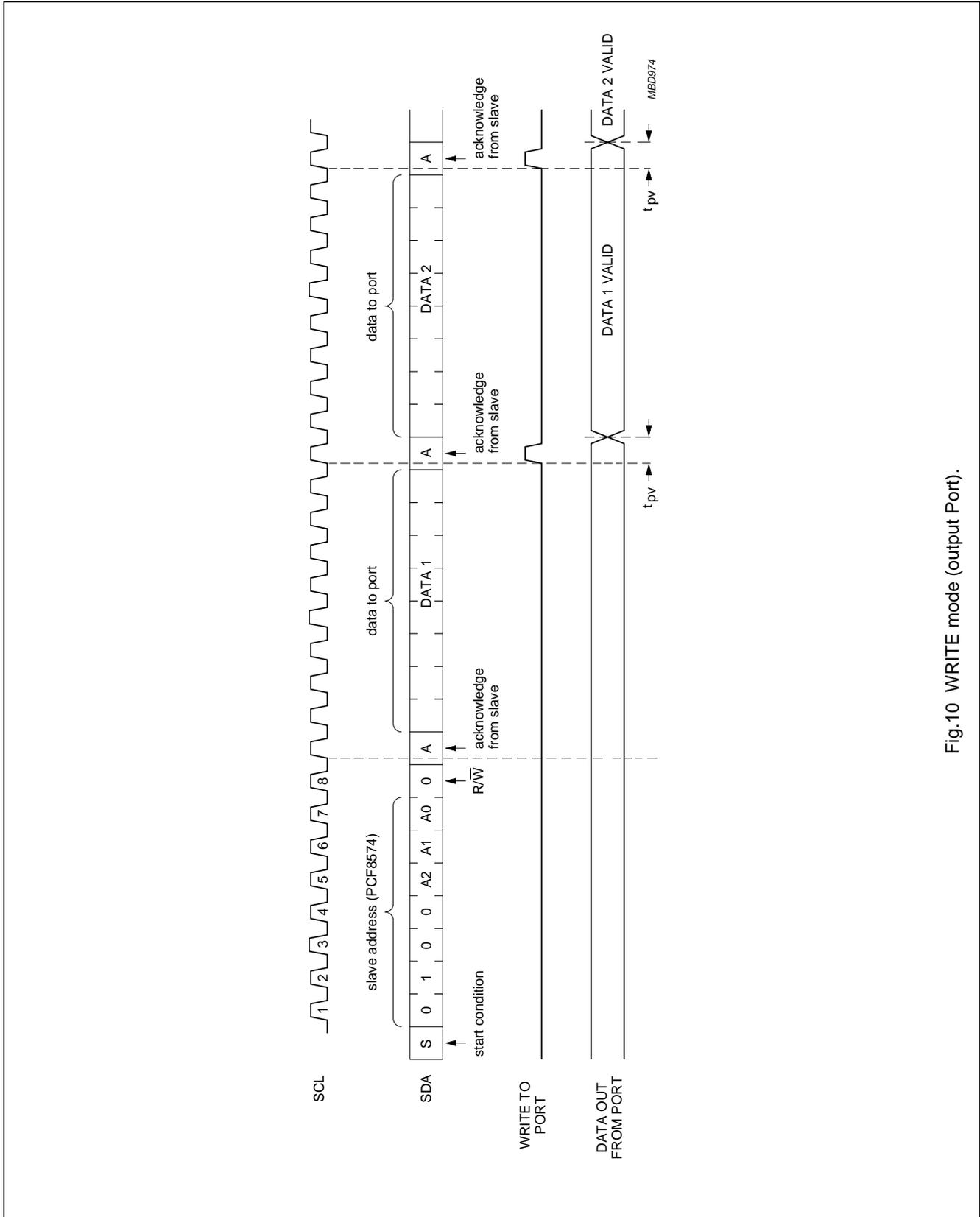


Fig.10 WRITE mode (output Port).

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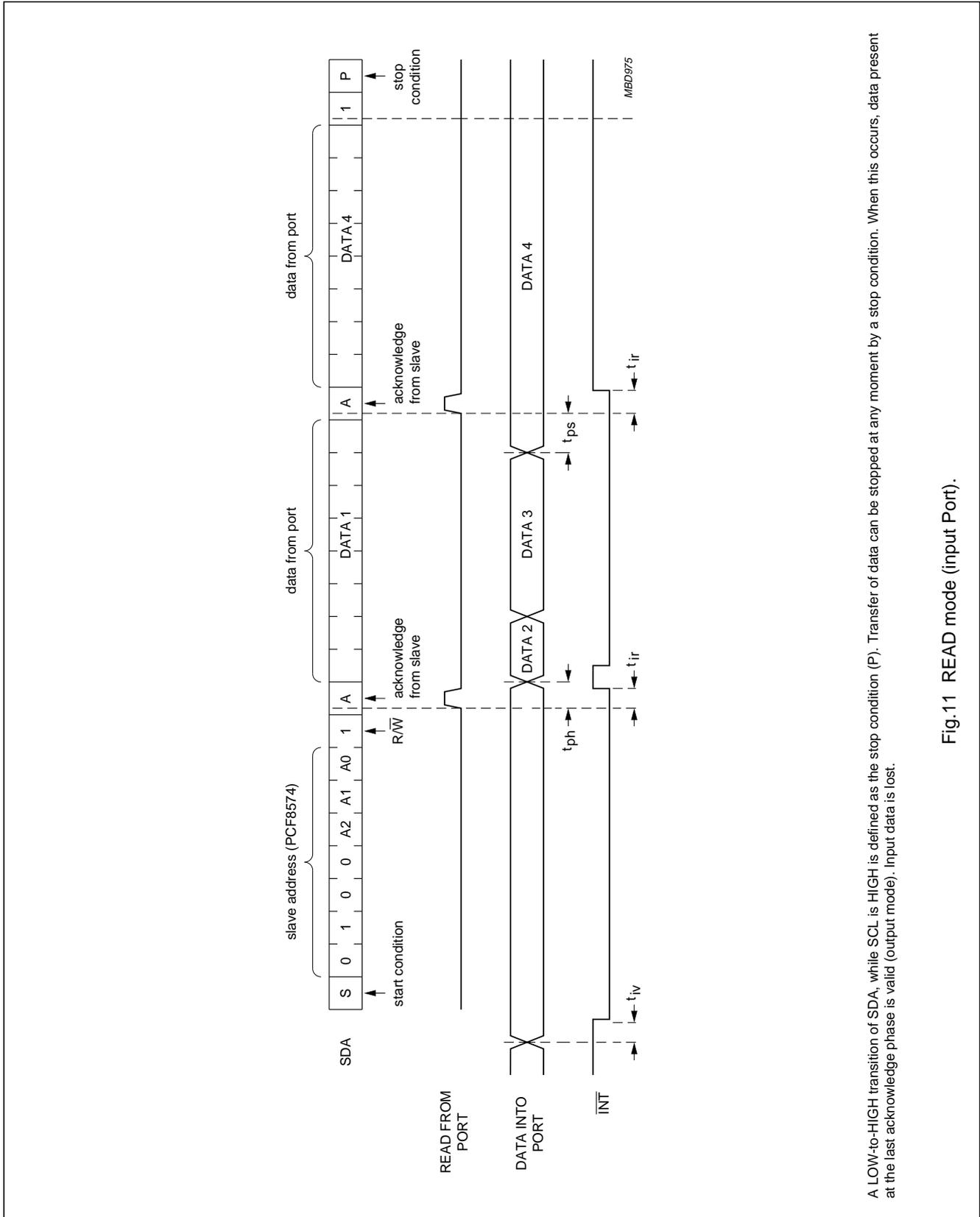


Fig.11 READ mode (input Port). A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Fig.11 READ mode (input Port).

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### Interrupt (see Figs 12 and 13)

The PCF8574 provides an open drain output ( $\overline{\text{INT}}$ ) which can be fed to a corresponding input of the microcontroller. This gives these chips a type of master function which can initiate an action elsewhere in the system.

An interrupt is generated by any rising or falling edge of the Port inputs in the input mode. After time  $t_{iv}$  the signal  $\overline{\text{INT}}$  is valid.

Resetting and reactivating the interrupt circuit is achieved when data on the Port is changed to the original setting or data is read from or written to the Port which has generated the interrupt.

Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH-to-LOW transition of the SCL signal.

- Interrupts which occur during the acknowledge clock pulse may be lost (or very short) due to the resetting of the interrupt during this pulse.

Each change of the Ports after the resettings will be detected and after the next rising clock edge, will be transmitted as  $\overline{\text{INT}}$ . Reading from or writing to another device does not affect the interrupt circuit.

### Quasi-bidirectional I/O Ports (see Fig.14)

A quasi-bidirectional Port can be used as an input or output without the use of a control signal for data direction. At power-on the Ports are HIGH. In this mode only a current source to  $V_{DD}$  is active. An additional strong pull-up to  $V_{DD}$  allows fast rising edges into heavily loaded outputs. These devices turn on when an output is written HIGH, and are switched off by the negative edge of SCL. The Ports should be HIGH before being used as inputs.

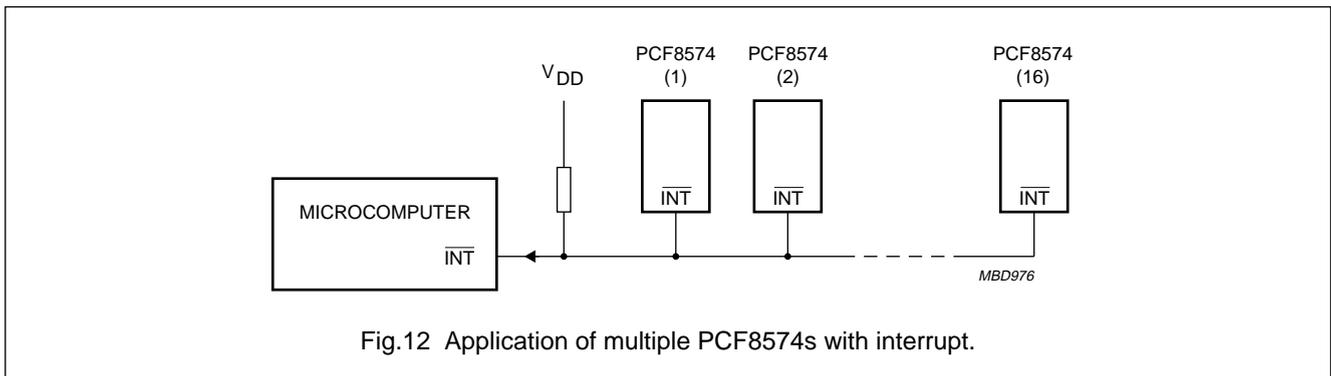


Fig.12 Application of multiple PCF8574s with interrupt.

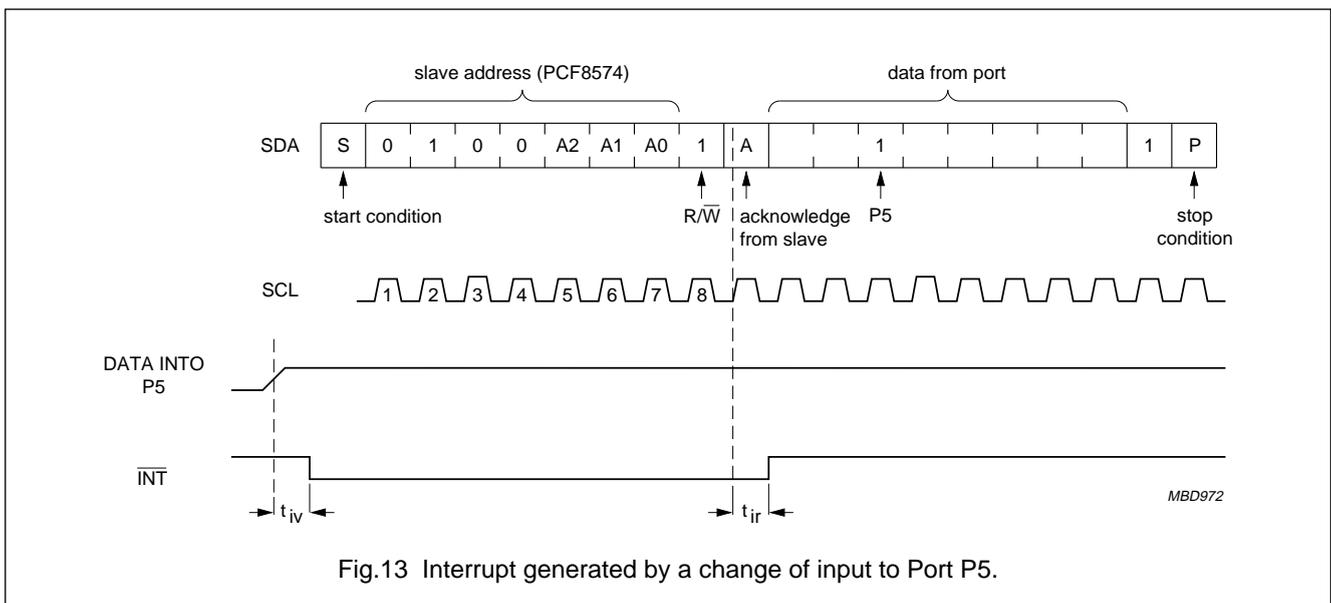


Fig.13 Interrupt generated by a change of input to Port P5.

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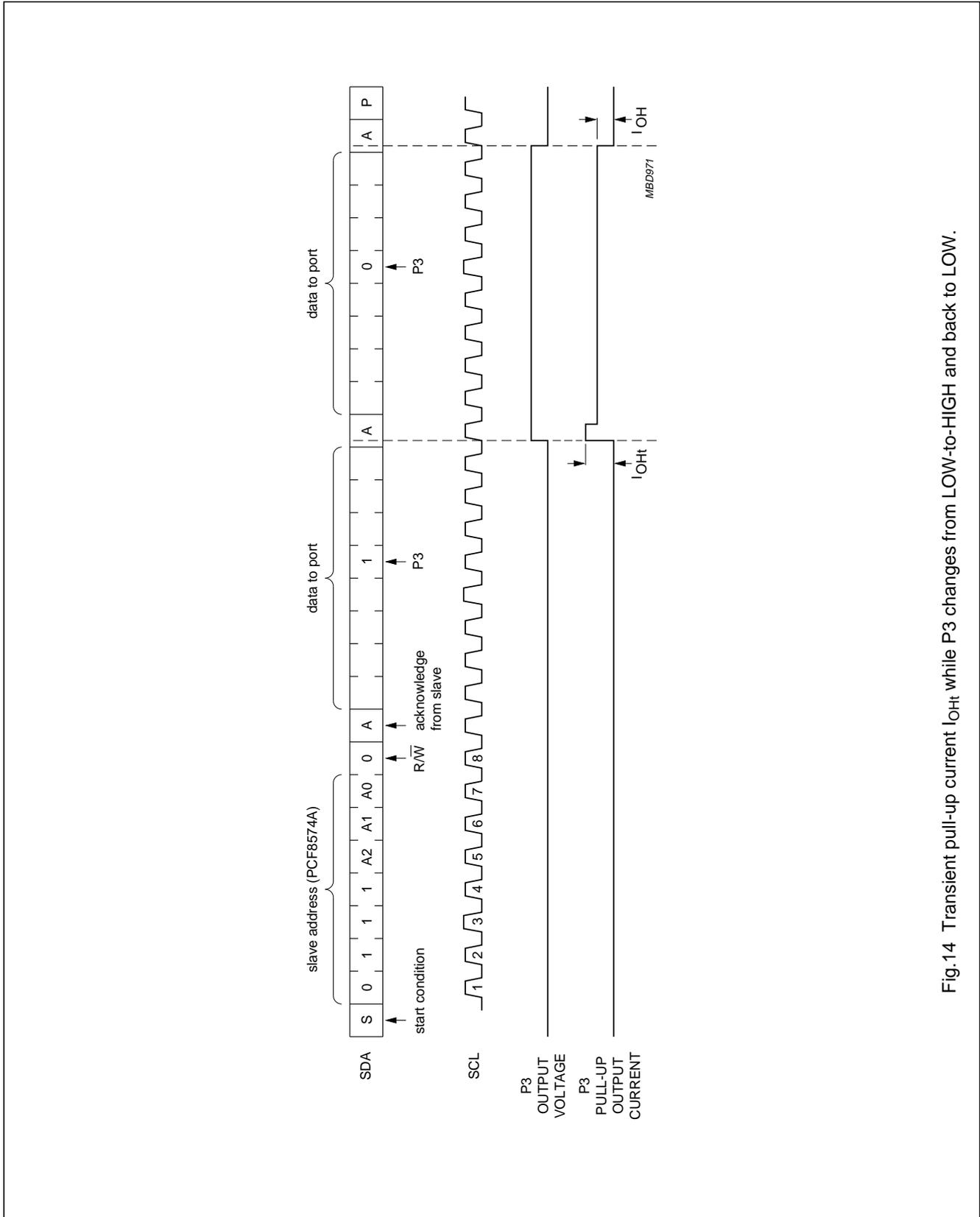


Fig.14 Transient pull-up current I<sub>OHt</sub> while P3 changes from LOW-to-HIGH and back to LOW.

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V <sub>DD</sub>	supply voltage	-0.5	+7.0	V
V <sub>I</sub>	input voltage	V <sub>SS</sub> - 0.5	V <sub>DD</sub> + 0.5	V
I <sub>I</sub>	DC input current	-	±20	mA
I <sub>O</sub>	DC output current	-	±25	mA
I <sub>DD</sub>	supply current	-	±100	mA
I <sub>SS</sub>	supply current	-	±100	mA
P <sub>tot</sub>	total power dissipation	-	400	mW
P <sub>O</sub>	power dissipation per output	-	100	mW
T <sub>stg</sub>	storage temperature	-65	+150	°C
T <sub>amb</sub>	operating ambient temperature	-40	+85	°C

**HANDLING**

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "Handling MOS devices").

**DC CHARACTERISTICS**

V<sub>DD</sub> = 2.5 to 6 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
V <sub>DD</sub>	supply voltage		2.5	-	6.0	V
I <sub>DD</sub>	supply current	operating mode; V <sub>DD</sub> = 6 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; f <sub>SCL</sub> = 100 kHz	-	40	100	µA
I <sub>stb</sub>	standby current	standby mode; V <sub>DD</sub> = 6 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-	2.5	10	µA
V <sub>POR</sub>	power-on reset voltage	V <sub>DD</sub> = 6 V; no load; V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub> ; note 1	-	1.3	2.4	V
<b>Input SCL; input/output SDA</b>						
V <sub>IL</sub>	LOW level input voltage		-0.5	-	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH level input voltage		0.7V <sub>DD</sub>	-	V <sub>DD</sub> + 0.5	V
I <sub>OL</sub>	LOW level output current	V <sub>OL</sub> = 0.4 V	3	-	-	mA
I <sub>L</sub>	leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-	-	1	µA
C <sub>I</sub>	input capacitance	V <sub>I</sub> = V <sub>SS</sub>	-	-	7	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>I/O Ports</b>						
V <sub>IL</sub>	LOW level input voltage		-0.5	-	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH level input voltage		0.7V <sub>DD</sub>	-	V <sub>DD</sub> + 0.5	V
I <sub>IHL(max)</sub>	maximum allowed input current through protection diode	V <sub>I</sub> ≥ V <sub>DD</sub> or V <sub>I</sub> ≤ V <sub>SS</sub>	-	-	±400	μA
I <sub>OL</sub>	LOW level output current	V <sub>OL</sub> = 1 V; V <sub>DD</sub> = 5 V	10	25	-	mA
I <sub>OH</sub>	HIGH level output current	V <sub>OH</sub> = V <sub>SS</sub>	30	-	300	μA
I <sub>OHt</sub>	transient pull-up current	HIGH during acknowledge (see Fig.14); V <sub>OH</sub> = V <sub>SS</sub> ; V <sub>DD</sub> = 2.5 V	-	-1	-	mA
C <sub>I</sub>	input capacitance		-	-	10	pF
C <sub>O</sub>	output capacitance		-	-	10	pF
<b>Port timing</b> (see Figs 10 and 11); C <sub>L</sub> ≤ 100 pF						
t <sub>pv</sub>	output data valid		-	-	4	μs
t <sub>su</sub>	input data set-up time		0	-	-	μs
t <sub>h</sub>	input data hold time		4	-	-	μs
<b>Interrupt INT</b> (see Fig.13)						
I <sub>OL</sub>	LOW level output current	V <sub>OL</sub> = 0.4 V	1.6	-	-	mA
I <sub>L</sub>	leakage current	V <sub>I</sub> = V <sub>DD</sub> or V <sub>SS</sub>	-	-	1	μA
TIMING; C <sub>L</sub> ≤ 100 PF						
t <sub>iv</sub>	input data valid time		-	-	4	μs
t <sub>ir</sub>	reset delay time		-	-	4	μs
<b>Select inputs A0 to A2</b>						
V <sub>IL</sub>	LOW level input voltage		-0.5	-	+0.3V <sub>DD</sub>	V
V <sub>IH</sub>	HIGH level input voltage		0.7V <sub>DD</sub>	-	V <sub>DD</sub> + 0.5	V
I <sub>LI</sub>	input leakage current	pin at V <sub>DD</sub> or V <sub>SS</sub>	-	-	250	nA

**Note**

1. The power-on reset circuit resets the I<sup>2</sup>C-bus logic with V<sub>DD</sub> < V<sub>POR</sub> and sets all Ports to logic 1 (with current source to V<sub>DD</sub>).

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I<sup>2</sup>C-BUS TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
I <sup>2</sup> C-BUS TIMING (see Fig.15; note 1)					
f <sub>SCL</sub>	SCL clock frequency	–	–	100	kHz
t <sub>SW</sub>	tolerable spike width on bus	–	–	100	ns
t <sub>BUF</sub>	bus free time	4.7	–	–	µs
t <sub>SU;STA</sub>	start condition set-up time	4.7	–	–	µs
t <sub>HD;STA</sub>	start condition hold time	4.0	–	–	µs
t <sub>LOW</sub>	SCL LOW time	4.7	–	–	µs
t <sub>HIGH</sub>	SCL HIGH time	4.0	–	–	µs
t <sub>r</sub>	SCL and SDA rise time	–	–	1.0	µs
t <sub>f</sub>	SCL and SDA fall time	–	–	0.3	µs
t <sub>SU;DAT</sub>	data set-up time	250	–	–	ns
t <sub>HD;DAT</sub>	data hold time	0	–	–	ns
t <sub>VD;DAT</sub>	SCL LOW to data out valid	–	–	3.4	µs
t <sub>SU;STO</sub>	stop condition set-up time	4.0	–	–	µs

Note

1. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V<sub>IL</sub> and V<sub>IH</sub> with an input voltage swing of V<sub>SS</sub> to V<sub>DD</sub>.

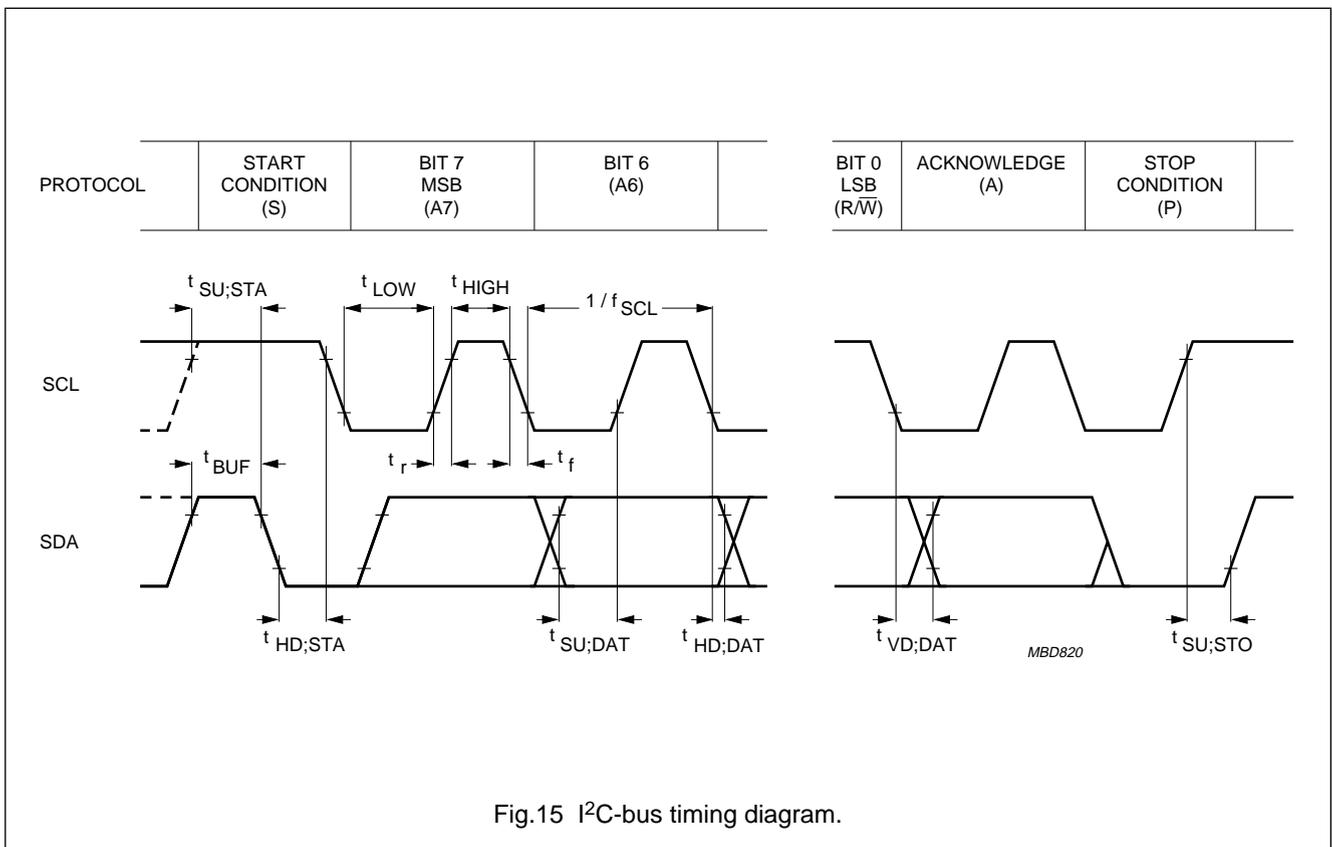
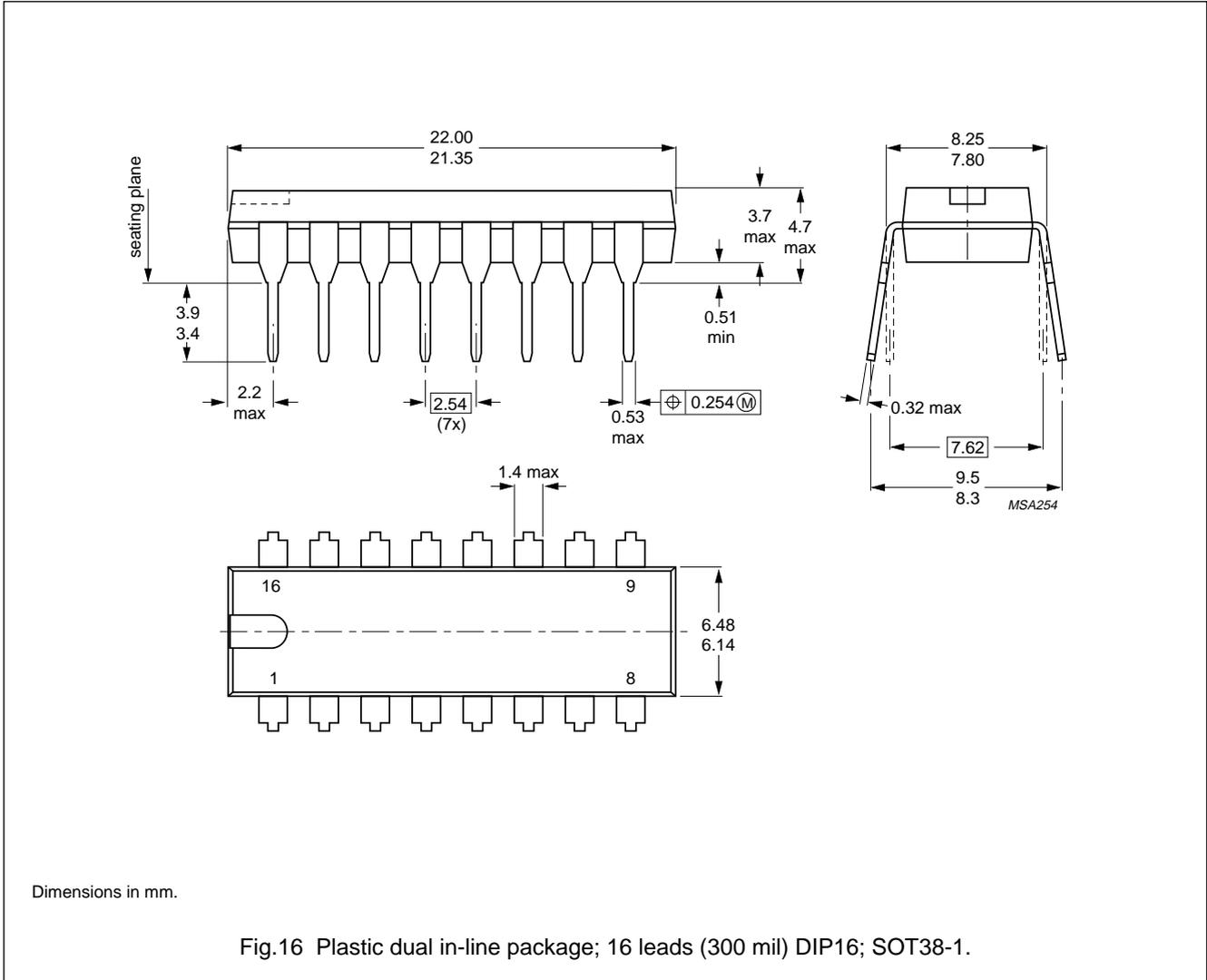


Fig.15 I<sup>2</sup>C-bus timing diagram.

# Remote 8-bit I/O expander for I<sup>2</sup>C-bus

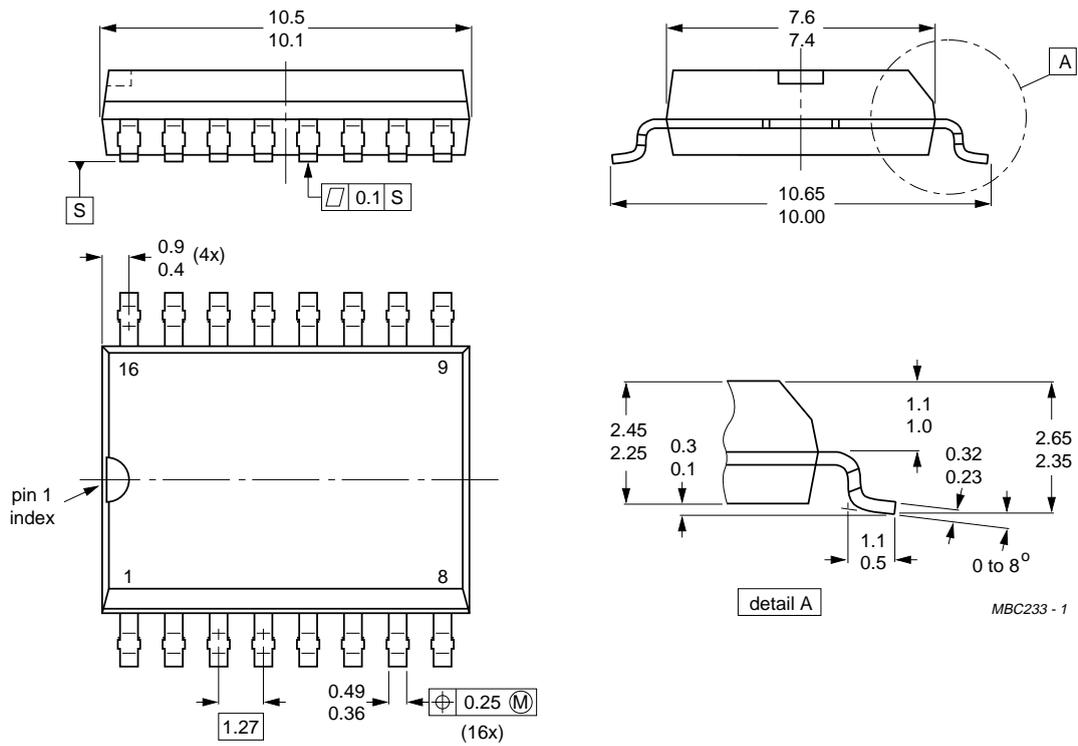
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## PACKAGE OUTLINES



Remote 8-bit I/O expander for I<sup>2</sup>C-bus

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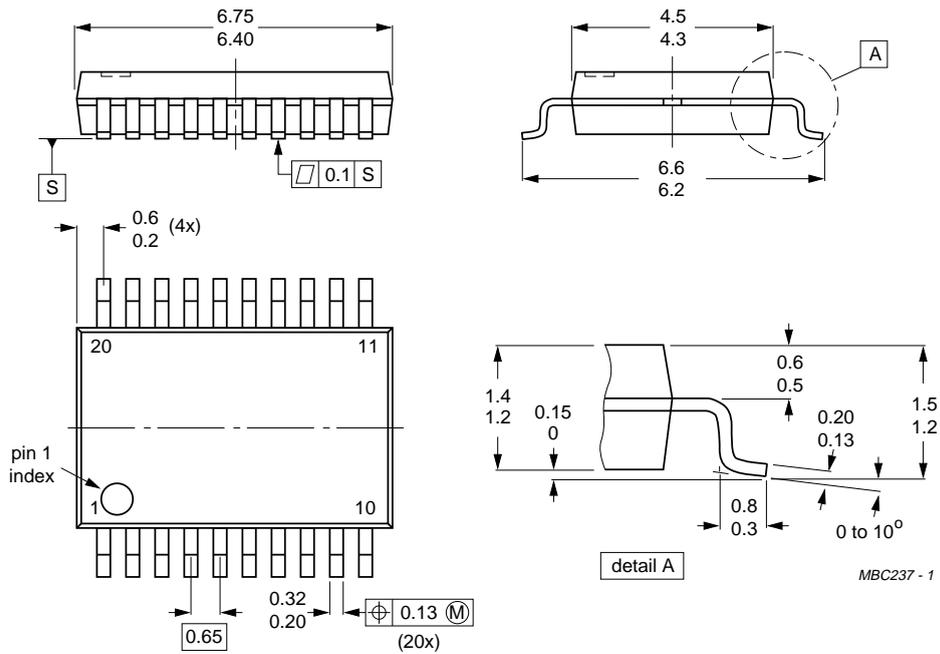


Dimensions in mm.

Fig.17 Plastic small outline package; 16 leads; body width 7.5 mm (SO16; SOT162-1).

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Dimensions in mm.

Fig.18 Plastic shrink small outline package; 20 leads; body width 4.4 mm (SSOP20; SOT266-1).

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## Remote 8-bit I/O expander for I<sup>2</sup>C-bus

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### SOLDERING

#### Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

#### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

#### Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

#### REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

**PURCHASE OF PHILIPS I<sup>2</sup>C COMPONENTS**

Purchase of Philips I<sup>2</sup>C components conveys a license under the Philips' I<sup>2</sup>C patent to use the components in the I<sup>2</sup>C system provided the system conforms to the I<sup>2</sup>C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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