

# DATA SHEET

## **SAA7707H**

### **Car radio Digital Signal Processor (CDSP)**

Preliminary specification  
File under Integrated Circuits, IC01

1996 May 22

# Car radio Digital Signal Processor (CDSP)

## SAA7707H

### CONTENTS

1	FEATURES	9.9	Clock circuit and oscillator
1.1	Hardware	9.10	Crystal oscillator supply
1.2	Software	9.11	External control pins
2	APPLICATIONS	10	I <sup>2</sup> S-BUS DESCRIPTION
3	GENERAL DESCRIPTION	10.1	I <sup>2</sup> C-bus control (SCL and SDA pins)
4	QUICK REFERENCE DATA	10.2	I <sup>2</sup> S-bus description
5	ORDERING INFORMATION	10.3	Communication with external digital audio sources (DCC + CD-WS/CL/Data pins)
6	BLOCK DIAGRAM	10.4	Communication with external processors and other devices (EXWS/CL/EXDAT1 and EXDAT2)
7	PINNING	10.5	Relationship between external input and external output
8	FUNCTIONAL DESCRIPTION	10.6	RDS decoder (RDCLK and RDSDAT)
8.1	Signal path for level information	10.7	Clock and data recovery
8.2	Level ADC switch mode integrator (pin CINT)	10.8	Timing of clock and data signals
8.3	Internal ground reference for the level ADC (pin V <sub>DACNL</sub> )	10.9	Buffering of RDS data
8.4	Common mode reference voltage for RDS ADC, ADC level and buffers (pin V <sub>refRDS</sub> )	10.10	Buffer interface
8.5	Signal path for audio/MPX and stereo decoder	10.11	DSP reset
8.6	Mono/stereo switching	10.12	Power supply connection and EMC
8.7	The automatic lock system	11	LIMITING VALUES
8.8	Input sensitivity for FM	12	THERMAL CHARACTERISTICS
8.9	Common mode reference voltage for MPX ADC and buffers (pin V <sub>refMPX</sub> )	13	DC CHARACTERISTICS
8.10	Supply voltages for the switch capacitor DACs of the FMMPX ADC and FMRDS ADC (pins V <sub>DACNM</sub> and V <sub>DACPM</sub> )	14	AC CHARACTERISTICS
8.11	Noise level	15	I <sup>2</sup> C-BUS CONTROL AND COMMANDS
8.12	TAPE/AUX de-multiplex	15.1	Characteristics of the I <sup>2</sup> C-bus
8.13	Signal-to-noise considerations	15.2	Bit transfer
8.14	Channel separation correction	15.3	START and STOP conditions
8.15	Input selection switches	15.4	Data transfer
8.16	Analog inputs supply	15.5	Acknowledge
8.17	Digitally controlled sampling clock (DCS)	15.6	I <sup>2</sup> C-bus format
8.18	Survey of the DCS clock settings in different modes	16	SOFTWARE DESCRIPTION
8.19	Synchronization with the core	17	APPLICATION INFORMATION
8.20	Interference absorption circuit	18	PACKAGE OUTLINE
8.21	IAC testing	19	SOLDERING
9	ANALOG OUTPUTS	19.1	Introduction
9.1	Digital-to-Analog Converters	19.2	Reflow soldering
9.2	Upsample filter	19.3	Wave soldering
9.3	Volume control	19.4	Repairing soldered joints
9.4	Power-on mute	20	DEFINITIONS
9.5	Power-off pop suppression	21	LIFE SUPPORT APPLICATIONS
9.6	Internal reference buffer amplifier of the DAC (pin V <sub>ref</sub> )	22	PURCHASE OF PHILIPS I <sup>2</sup> C COMPONENTS
9.7	Internal DAC current reference		
9.8	Analog outputs supply		



# Car radio Digital Signal Processor (CDSP)

SAA7707H

## 1 FEATURES

### 1.1 Hardware

- Bitstream 3rd-order Sigma-Delta Analog-to-Digital Converters (ADCs) with anti-aliasing broadband input filters
- Digital-to-Analog Converters (DACs) with four times oversampling and noise shaping
- Digital stereo decoder
- Improved digital Interference Absorption Circuit (IAC)
- RDS processing with optional 16-bit buffer via separate channel (two-tuner radio possible)
- Auxiliary analog CD input (CD-walkman, speech, economic CD-changer, etc.)
- Two separate full I<sup>2</sup>S-bus CD and DCC high performance interfaces
- Expandable with additional Digital Signal Processors (DSPs) for sophisticated features through an I<sup>2</sup>S-bus gateway
- Audio output short-circuit protected
- I<sup>2</sup>C-bus controlled
- Analog tape input
- Operating ambient temperature from –40 to +85 °C.

### 1.2 Software

- Improved FM weak signal processing
- Integrated 19 kHz MPX filter and de-emphasis
- Electronic adjustments: FM/AM level, FM channel separation and Dolby level
- Baseband audio processing (treble, bass, balance, fader and volume)
- Dynamic loudness or bass boost
- Stereo one-band parametric equalizer
- Audio level meter for an automatic leveller (in combination with microcontroller)
- Tape equalization (DCC analog playback)
- Music Search detection for Tape (MSS)
- Pause detection for RDS updates
- Dolby-B tape noise reduction
- Adjustable dynamics compressor
- CD and DCC de-emphasis processing
- Signal level, noise and multi-path detection for RDS (I<sup>2</sup>C-bus command)
- Improved AM reception.

## 2 APPLICATIONS

- Car radio
- Car audio systems.

## 3 GENERAL DESCRIPTION

The SAA7707H performs all the signal functions in front of the power amplifiers and behind the AM and FMMPX demodulation of a car radio or the tape input.

These functions are:

- Interference absorption
- Stereo decoding
- RDS decoding
- FM and AM weak signal processing (soft mute, sliding stereo, etc.)
- Dolby-B tape noise reduction
- The audio controls (volume, balance, fader, tone and dynamics compression).

Some functions have been implemented in hardware (stereo decoder, RDS decoder and IAC) and are not freely programmable. Digital audio signals from external sources with I<sup>2</sup>S-bus formats are accepted. There are four independent analog output channels. This enables, in special system configurations, separate tone and equalization control for front and rear speakers.

The CDSP contains a basic program that enables a set with:

- AM/FM reception
- Sophisticated FM weak signal functions
- Music Search detection for Tape (MSS)
- Dolby-B tape noise reduction system
- CD play with compressor function
- Separate bass and treble tone control and fader/balance control.

For high-end sets with special and more sophisticated features, an additional Digital Signal Processor (DSP) can be connected. Examples of such features are:

- Noise-dependent volume control
- 10-band graphic equalizer
- Audio spectrum analyzer on display
- Signal delay for concert hall effects.

## Car radio Digital Signal Processor (CDSP)

SAA7707H

## 4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDD(tot)}$	total DC supply voltage	all supply pins	4.75	5	5.5	V
$I_{DDD(tot)}$	total DC supply current	maximum activity of the DSP; $f_{xtal} = 36$ MHz	–	160	200	mA
$P_{tot}$	total power dissipation	maximum activity of the DSP; $f_{xtal} = 36$ MHz	–	0.8	1.1	W
S/N	level ADC signal-to-noise ratio	RMS value; unweighted; B = 0 to 29 kHz; maximum input	48	54	–	dB
	ADC signal-to-noise ratio	not multiplexed; B = 19 kHz; $V_i = 1$ V (RMS)	81	85	–	dB
		multiplexed; unweighted; B = 19 kHz; 1 V (RMS)	72	76	–	dB
	ADC signal-to-noise ratio for FM-RDS	RMS value; B = 6 kHz; unweighted; $f_c = 57$ kHz	56	–	–	dB
$V_{iFS}$	ADC full scale input voltage	$V_{DDA1} = 4.75$ to $5.5$ V	$1.05V_{DDA1}$	$1.1V_{DDA1}$	$1.15V_{DDA1}$	V
THD	total harmonic distortion pins 62 and 71 to 75	$f_i = 1$ kHz; $V_i = 1$ V (RMS)	–	–71	–61	dB
			–	0.03	0.09	%
$V_{imc(rms)}$	maximum conversion input voltage level pins 62 and 71 to 75 (RMS value)	THD < 1%	1.1	–	–	V
RES	DAC resolution		–	18	–	bits
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio for DAC and operational amplifiers	$R_L > 5$ k $\Omega$ AC; $R_{fb} = 2.7$ k $\Omega$ ; $f_i = 1$ kHz; $R_{ref} = 18$ k $\Omega$ ; $V_{oFS} = 2.8$ V (p-p); maximum I <sup>2</sup> S-bus signal	–	–70	–57	dB
DR	dynamic range of DAC	$f_i = 1$ kHz; –60 dB; A-weighted	92	102	–	dB
DS	digital silence of DAC	$f_i = 20$ Hz to 17 kHz; A-weighted	–	–110	–100	dB
$f_{xtalDSP}$	crystal frequency DSP part		–	36.86	–	MHz

## 5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7707H	QFP80	plastic quad flat package; 80 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm	SOT318-2

# Car radio Digital Signal Processor (CDSP)

# SAA7707H

## 6 BLOCK DIAGRAM

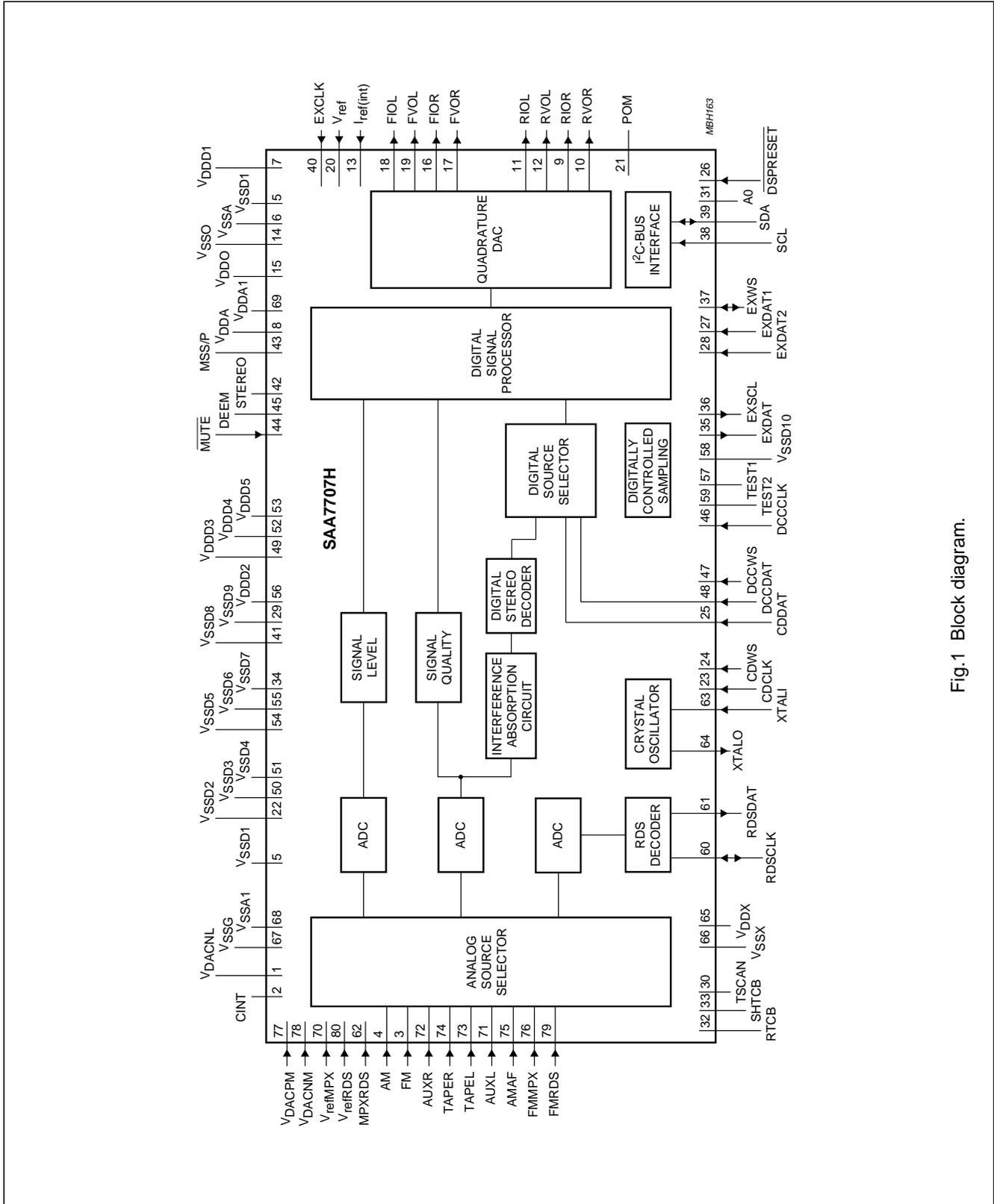


Fig.1 Block diagram.

## Car radio Digital Signal Processor (CDSP)

SAA7707H

## 7 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
V <sub>DACNL</sub>	1	–	internal ground reference voltage for the level ADC
CINT	2		level ADC switch-mode integrator connector
FM	3	I	FM level input; via this pin, the level of the received FM radio signal is fed to the CDSP, the level information is required to enable correct functioning of the weak signal behaviour
AM	4	I	AM level input; via this pin, the level of the received AM radio signal is fed to the CDSP
V <sub>SSD1</sub>	5	–	ground supply 1 for the DACs digital circuitry
V <sub>SSA</sub>	6	–	ground supply for the DACs analog circuitry
V <sub>DDD1</sub>	7	–	positive supply 1 for the DACs digital circuitry
V <sub>DDA</sub>	8	–	positive supply for the DACs analog circuitry
RIOR	9	O	analog audio current output for rear right speaker
RVOR	10	O	analog audio voltage output for rear right speaker
RIOL	11	O	analog audio current output for rear left speaker
RVOL	12	O	analog audio voltage output for rear left speaker
I <sub>ref(int)</sub>	13	I	internal reference current source input for the DACs
V <sub>SSO</sub>	14	–	ground supply for DAC output operational amplifiers
V <sub>DDO</sub>	15	–	positive supply for DAC output operational amplifiers
FIOR	16	O	analog audio current output for front right speaker
FVOR	17	O	analog audio voltage output for front right speaker
FIOL	18	O	analog audio current output for front left speaker
FVOL	19	O	analog audio voltage output for front left speaker
V <sub>ref</sub>	20	I	voltage input for the internal reference buffer amplifier of the DAC
POM	21		activates the Power-on mute; timing is determined with an external capacitor
V <sub>SSD2</sub>	22	–	ground supply 2 for the digital circuitry
CDCLK	23	I	clock input for CD digital audio source (I <sup>2</sup> S-bus)
CDWS	24	I	Word Select input for CD digital audio source (I <sup>2</sup> S-bus)
CDDAT	25	I	left/right data input for CD digital audio source (I <sup>2</sup> S-bus)
DSPRESET	26	I	input to reset DSP core (active LOW)
EXDAT1	27	I	external input data channel 1 (front) from extra DSP chip (I <sup>2</sup> S-bus)
EXDAT2	28	I	external input data channel 2 (rear) from extra DSP chip (I <sup>2</sup> S-bus)
V <sub>SSD9</sub>	29	–	ground supply 9 for the digital circuitry
TSCAN	30		scan control (active HIGH)
A0	31		I <sup>2</sup> S-bus selection for slave sub-address
RTCB	32		asynchronous reset test control block (active HIGH)
SHTCB	33		shift clock test control block (active HIGH)
V <sub>SSD7</sub>	34	–	ground supply 7 for the digital circuitry
EXDAT	35	O	output data for extra external DSP chip (I <sup>2</sup> S-bus)
EXSCL	36	O	output clock for extra external DSP chip (I <sup>2</sup> S-bus)
EXWS	37	I/O	word select input/output for extra external DSP chip (I <sup>2</sup> S-bus)

## Car radio Digital Signal Processor (CDSP)

## SAA7707H

SYMBOL	PIN	I/O	DESCRIPTION
SCL	38	I	serial clock input (I <sup>2</sup> C-bus)
SDA	39	I/O	serial data input/output (I <sup>2</sup> C-bus)
EXCLK	40	I	external reference clock input to generate 4f <sub>as</sub> and f <sub>as</sub> synchronization; to be used if the I <sup>2</sup> S-bus inputs are not suitable
V <sub>SSD8</sub>	41	–	ground supply 8 for the digital circuitry
STEREO	42		FM stereo indication (active HIGH)
MSS/P	43		FM pause detector/MSS detector (active HIGH); also for IAC trigger output
MUTE	44	I	MUTE input pin (active LOW); only for FM mode
DEEM	45		de-emphasis; CD and DCC (active HIGH) (I <sup>2</sup> S-bus)
DCCCLK	46	I	DCC digital audio source clock input (I <sup>2</sup> S-bus)
DCCWS	47	I	DCC digital audio source Word Select input (I <sup>2</sup> S-bus)
DCCDAT	48	I	DCC digital audio source left/right data input (I <sup>2</sup> S-bus)
V <sub>DD3</sub>	49	–	positive supply 3 for the digital circuitry
V <sub>SS3</sub>	50	–	ground supply 3 for the digital circuitry
V <sub>SS4</sub>	51	–	ground supply 4 for the digital circuitry
V <sub>DD4</sub>	52	–	positive supply 4 for the digital circuitry
V <sub>DD5</sub>	53	–	positive supply 5 for the digital circuitry
V <sub>SS5</sub>	54	–	ground supply 5 for the digital circuitry
V <sub>SS6</sub>	55	–	ground supply 6 for the digital circuitry
V <sub>DD2</sub>	56	–	positive supply 2 for the digital circuitry
TEST1	57		test pin 1 (this pin should be left open-circuit)
V <sub>SS10</sub>	58	–	ground supply 10 for the digital circuitry
TEST2	59		test pin 2 (this pin should be left open-circuit)
RDSCLK	60	I/O	radio data system bit clock input/output
RDSDAT	61	O	radio data system data output
MPXRDS	62	I	in FM mode, selects between FMMPX and RDSMPX input signal to the MPX decimation filter
XTALI	63	I	crystal oscillator input; can also be used as forced input in slave mode
XTALO	64	O	crystal oscillator output
V <sub>DDX</sub>	65	–	positive supply crystal circuitry
V <sub>SSX</sub>	66	–	ground supply crystal circuitry
V <sub>SSG</sub>	67	–	ground guards for ADCs
V <sub>SSA1</sub>	68	–	analog ground supply for ADCs
V <sub>DDA1</sub>	69	–	analog positive supply for ADCs
V <sub>refMPX</sub>	70	I	common mode reference voltage input for MPX ADC and buffers
AUXL	71	I	analog input for auxiliary left signal
AUXR	72	I	analog input for auxiliary right signal
TAPEL	73	I	analog input for tape left signal
TAPER	74	I	analog input for tape right signal
AMAF	75	I	analog input for AM audio frequency
FMMPX	76	I	analog input for FM multiplex signal

## Car radio Digital Signal Processor (CDSP)

SAA7707H

<b>SYMBOL</b>	<b>PIN</b>	<b>I/O</b>	<b>DESCRIPTION</b>
$V_{DACPM}$	77	I	supply voltage for the DACs switch capacitor of the FMMPX ADC and FMRDS ADC
$V_{DACNM}$	78	I	ground supply for the DACs switch capacitor of the FMMPX ADC and FMRDS ADC
FMRDS	79	I	analog FMMPX input for RDS decoding
$V_{refRDS}$	80	I	common mode reference voltage input for RDS ADC, level ADC and buffers

Car radio Digital Signal Processor (CDSP)

SAA7707H

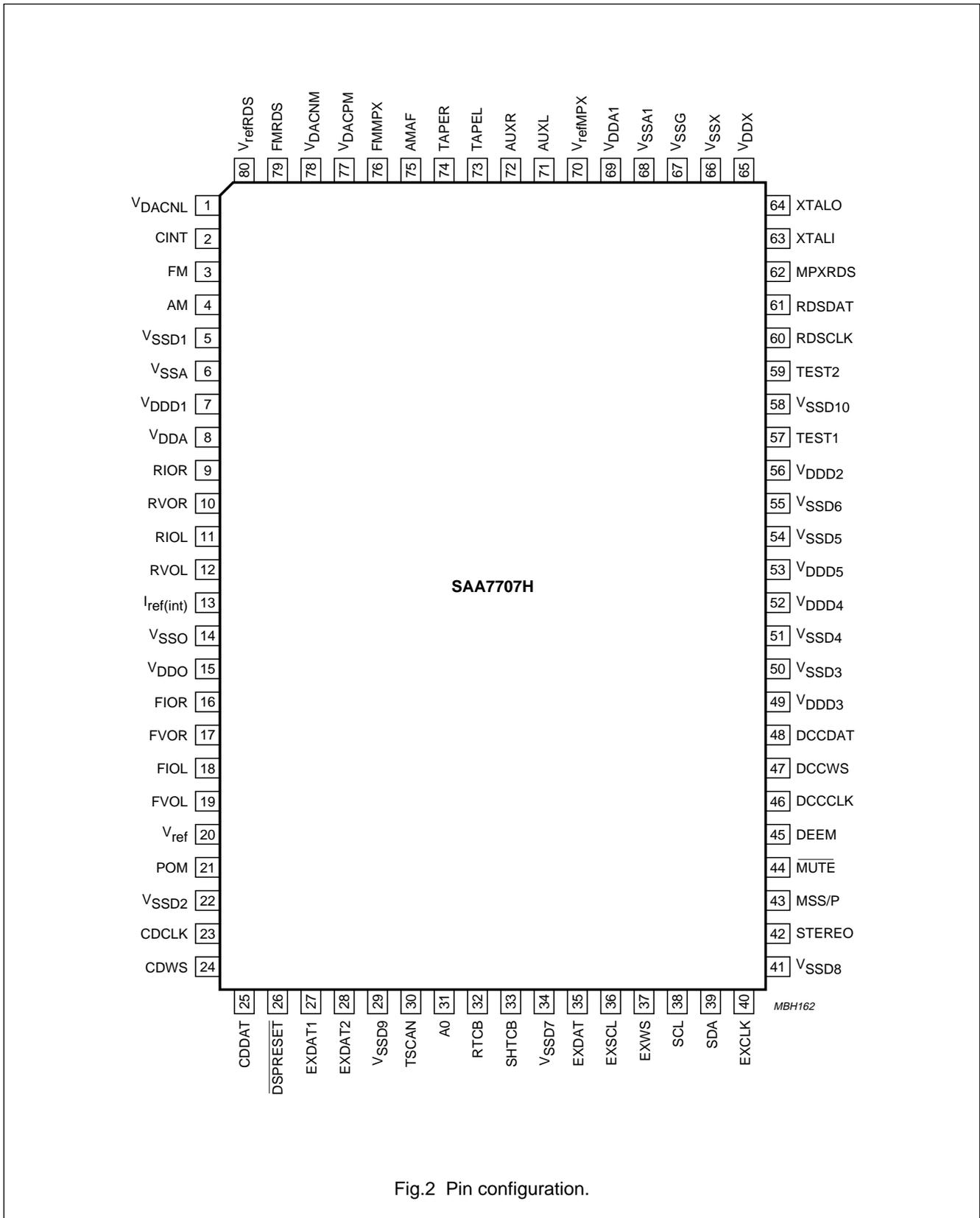


Fig.2 Pin configuration.

# Car radio Digital Signal Processor (CDSP)

# SAA7707H

## 8 FUNCTIONAL DESCRIPTION

### 8.1 Signal path for level information

An FM and AM level input is implemented for FM weak signal processing [for AM, FM and RDS search purposes (absolute level and multi-path)]. A DC input signal is converted by a bitstream 1st-order Sigma-Delta analog-to-digital converter and then filtered by a decimation filter.

The input signal has to be obtained from the radio part. Two different circuits for AM and FM reception are possible:

1. A circuit with two separate input signals, one for FM level and one for AM level
2. A combined circuit with AM and FM level information on the FM level input. The AM level input can then be connected to another signal, which can be converted in the non-radio mode.

The input is selected via the input selector control register.

The input signal for level control must be in the range of 0 to 5 V. The 11-bit level ADC converts this input voltage in steps with a resolution better than 10 mV over the 5 V range. The tolerance on the gain is less than 10%. The MSB is always logic 0, to represent a positive level.

The decimation filter reduces the bandwidth of the incoming signal to a frequency range of 0 to 29 kHz, with a resulting sampling frequency ( $f_s$ ) of 76 kHz. The response curve is illustrated in Fig.3.

The level information is sub-sampled by the DSP core to obtain a field strength and a multi-path indication. These values are stored in the coefficient or data RAM. They can be read and used in other microcontroller programs via the I<sup>2</sup>C-bus.

### 8.2 Level ADC switch mode integrator (pin CINT)

The level ADC has an internal current summation point of the input level and the switch capacitor DAC. When used as an integrator, an external capacitor of 1000 pF should be connected between this pin and the analog ground at pin V<sub>SSA1</sub>. The summation voltage is used as an input for the analog-to-digital comparator level.

### 8.3 Internal ground reference for the level ADC (pin V<sub>DACNL</sub>)

This pin serves as the internal ground reference for the switch capacitor DAC and the level ADC and has to be connected to the analog ground (pin V<sub>SSA1</sub>).

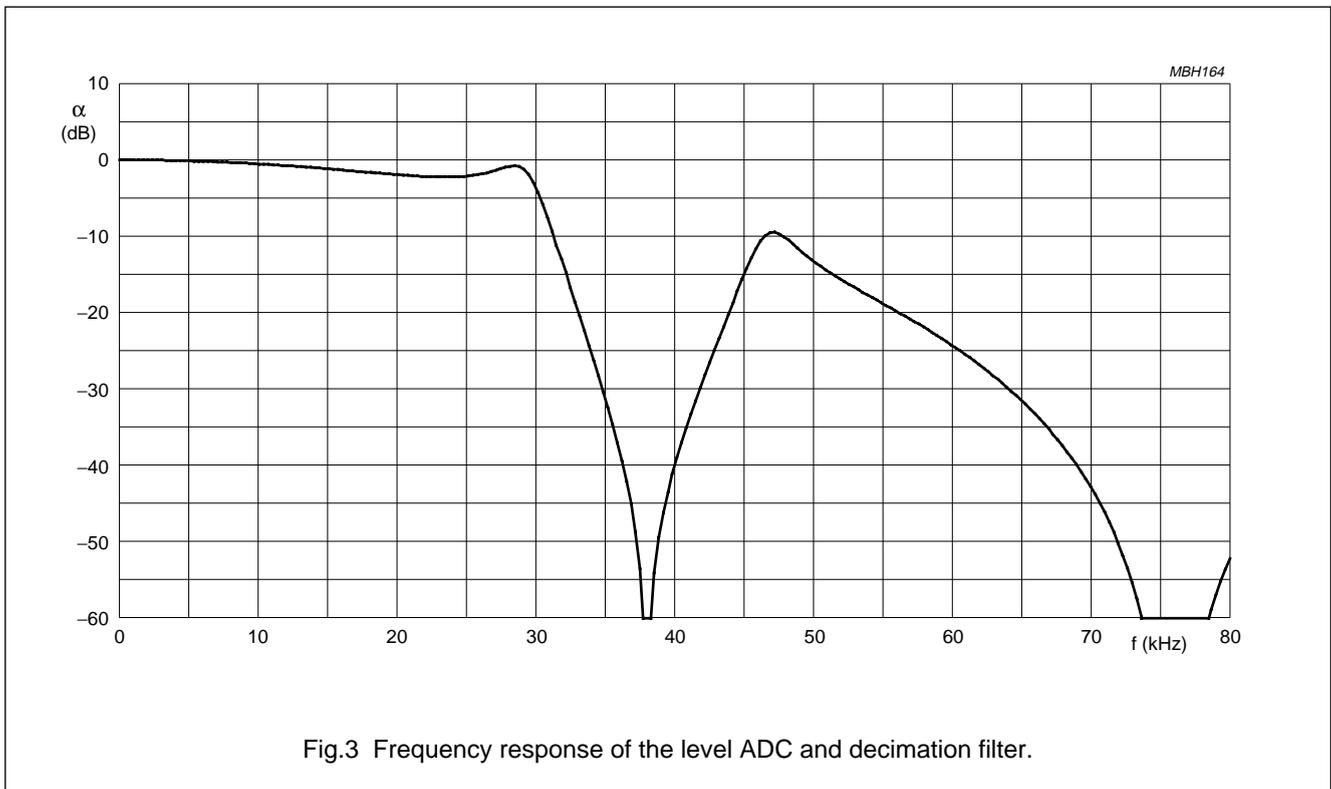


Fig.3 Frequency response of the level ADC and decimation filter.

## Car radio Digital Signal Processor (CDSP)

## SAA7707H

**8.4 Common mode reference voltage for RDS ADC, ADC level and buffers (pin  $V_{refRDS}$ )**

The middle reference voltage of the RDS ADC can be filtered via this pin. This middle reference voltage is used as a positive reference for the level ADC of the switch capacitor DAC and as half supply reference for the RDS ADC, the switch capacitor DACs and buffers. An external capacitor (connected to  $V_{SSA1}$ ) prevents crosstalk between the switch capacitor DACs of the RDS ADC, level ADC and buffers, and improves the power supply rejection ratio.

**8.5 Signal path for audio/MPX and stereo decoder**

The SAA7707H has four analog audio source inputs; two single-multiplex channel inputs for AM and FM radio and two stereo inputs for tape and auxiliary. The auxiliary input can be used for functions such as an analog CD changer or speech applications. The stereo inputs are multiplexed so that they can share the same filters as the multiplexed FM signal. The selection between the AM, FM, TAPE and AUX input is made via the input selector control register.

The input signal behind the source selector is digitized by a bitstream 3rd-order Sigma-Delta ADC. The first decimation filter reduces the sample rate. This is followed by the sample-and-hold switch of the IAC and the 19 kHz regeneration circuit. From here, the wide-band noise detector signal HP2 (High-Pass 2) with a frequency range of 60 to 240 kHz is derived. A second decimation filter reduces the output of the IAC to a lower sample rate.

This filter has two outputs, one for the multiplex signal with a frequency range of 0 to 60 kHz (low-pass) and one for the small-band noise detector signal HP1 (High-Pass 1) with a frequency range of 60 to 120 kHz. The overall low-pass frequency response of the decimation filters is illustrated in Fig.4.

In the FM mode, the RDS ADC can be used as an input for the MPX decimation filter. This can be selected via the RDSMPX input at pin 62.

The outputs from this signal path to the DSP, which are all at a sample frequency of 38 kHz, are as follows:

- Pilot presence indication: Pilot-I. This 1-bit signal is LOW for a pilot frequency deviation of less than 4 kHz and HIGH for a pilot frequency deviation greater than 4 kHz. It is AND locked on a pilot tone
- Pilot quality indication: Pilot-Q. This 10-bit signal contains information about the signal quality and is derived from the quadrature component of the pilot-I signal

- 'Left' and 'Right': This is the 18-bit output of the stereo decoder after the matrix decoding. For AM reception, the 'Right' signal contains the AM-mono signal. For tape or auxiliary signals, the output of the stereo decoder contains sum and difference signals, but with other crosstalk properties than on FM. Therefore, a different matrix correction, as shown in Table 1, has to be applied to these signals in the DSP program. The overall frequency response of the demultiplexed signal at the output of the stereo decoder is illustrated in Fig.5.

**Table 1** Overview of the signals to the CDSP

MODE	LEFT	RIGHT
AM	0	mono
FM	$\frac{1}{2}(R - L)$	R + L
TAPE/AUX	$\frac{1}{2}(R + L) \times 4/\pi$	R + L

Apart from the aforementioned theoretical response, the non-flat frequency response of the ADC must also be compensated for in the DSP program.

**8.6 Mono/stereo switching**

After division, the Digitally Controlled Sampling (DCS) clock generates a clock signal with a frequency which is a multiple of 19 kHz plus or minus a few Hertz. For mono reception, the DCS circuit generates a preset frequency of  $n \times 19 \text{ kHz} \pm 2 \text{ Hz}$ . For stereo reception, the frequency is exactly  $n \times 19 \text{ kHz}$  (DCS locked to  $n \times$  pilot tone). The detection of the pilot and the stereo indication is performed in the DSP program.

**8.7 The automatic lock system**

The VCO operates at  $19 \text{ kHz} \pm 2 \text{ Hz}$  exactly for no-pilot. For stereo reception, the phase error is zero for a pilot tone with a frequency of exactly 19 kHz. Therefore, no switch is required to preset the clock to 19 kHz. With auxiliary sources (tape, CD, etc.), the DCS circuit has to be preset to a fixed value.

**8.8 Input sensitivity for FM**

The FM input sensitivity is optimally designed for an FM front-end with an output voltage of 200 mV (RMS) at a modulation depth of 22.5 kHz of a 1 kHz tone. Due to the full scale 1.2 V (RMS) handling capacity of the ADC, the maximum allowed modulation depth of a transmitter, for a THD of 10%, is 135 kHz. Full performance is possible for transmitters with a modulation depth of up to 110 kHz.

Car radio Digital Signal Processor (CDSP)

SAA7707H

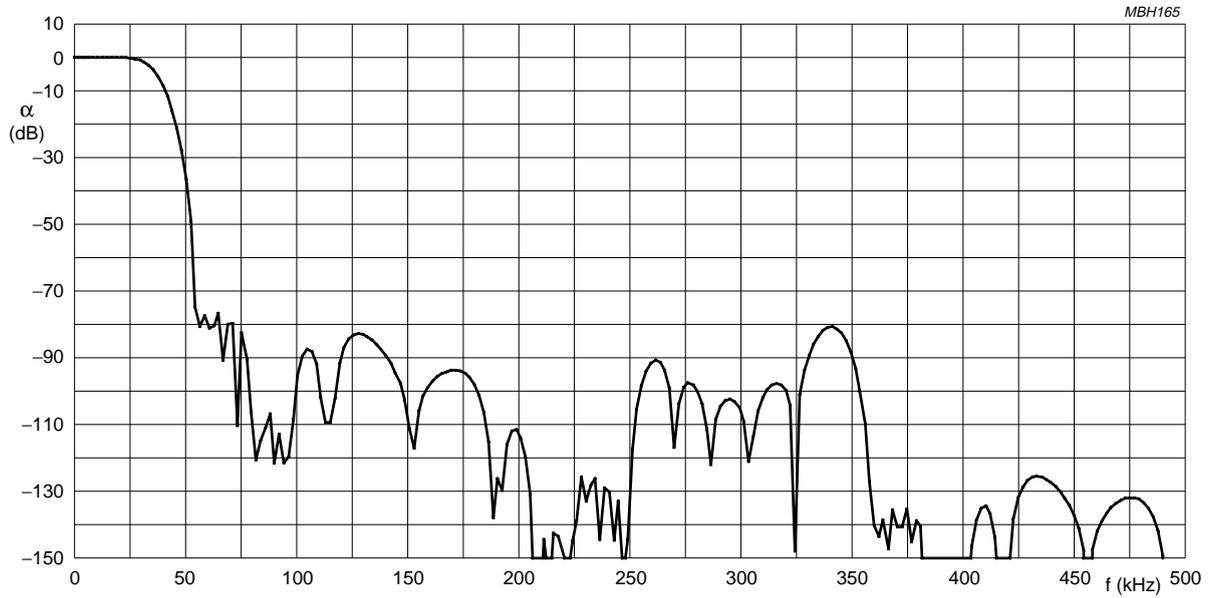


Fig.4 Overall frequency response multiplex ADC and decimation filters.

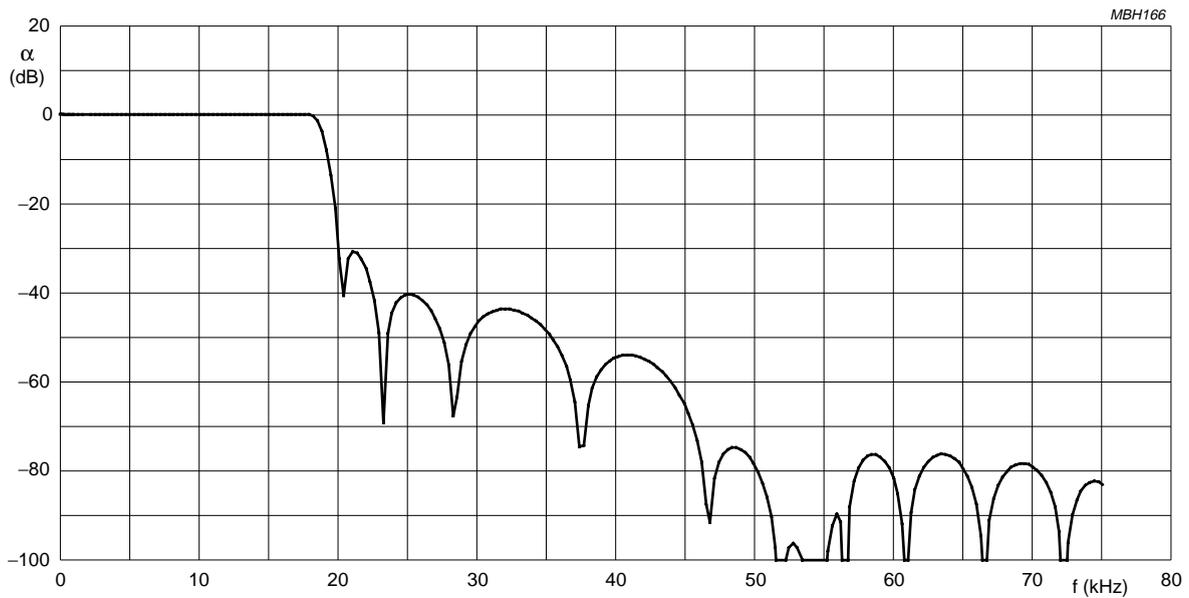


Fig.5 Transfer of MPX signal at the output of the stereo decoder.

# Car radio Digital Signal Processor (CDSP)

# SAA7707H

### 8.9 Common mode reference voltage for MPX ADC and buffers (pin $V_{refMPX}$ )

The middle reference voltage of the MPX ADC can be filtered via this pin. This middle reference voltage is used as a half supply voltage reference for the MPX ADC, switch capacitor DACs and buffers. An external capacitor (connected to  $V_{SSA1}$ ) prevents crosstalk between the switch capacitor DACs and buffers and improves the power supply rejection ratio.

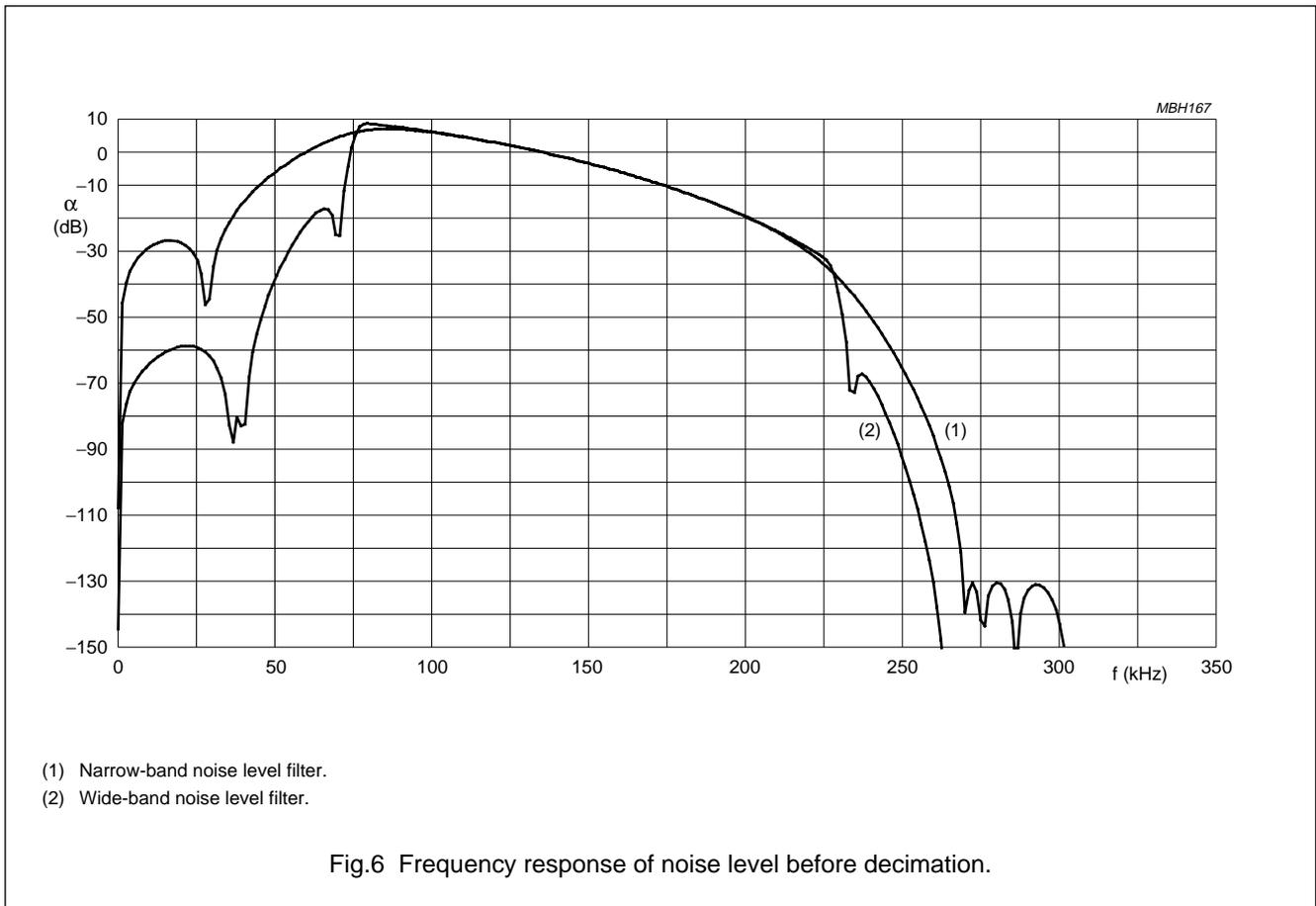
### 8.10 Supply voltages for the switch capacitor DACs of the FMMPX ADC and FMRDS ADC (pins $V_{DACNM}$ and $V_{DACPM}$ )

These pins are used as ground and positive supply voltage reference for the MPX ADC, RDS ADC and the switch capacitor DACs. For optimum performance they must be connected directly to  $V_{SSA1}$  and  $V_{DDA1}$ .

### 8.11 Noise level

The High-Pass 1 (HP1 or narrow-band noise level filter) output of the second MPX decimation filter, in a frequency band from 60 to 120 kHz, is detected with an envelope detector and decimated to a frequency of 38 kHz.

The response time of the detector is 100 ms. Another option is the High-Pass 2 (HP2 or wide-band noise level filter). This output from the first MPX decimation filter is in a frequency band from 60 to 240 kHz. It has the same properties as the HP1 and is also decimated to 38 kHz. Which signal is used (HP1 or HP2) is determined by the input selector control register. The noise level can be detected and filtered in the DSP core and can be used to optimize the FM weak-signal processing. The transfer curves of both filters before decimation are illustrated in Fig.6.



## Car radio Digital Signal Processor (CDSP)

## SAA7707H

**8.12 TAPE/AUX de-multiplex**

The auxiliary and tape inputs also use the stereo decoder. Because of this, the left and right channels are multiplexed with a 38 kHz square wave to obtain a signal similar to the FM multiplexed signal. Auxiliary inputs can be e.g. TV-sound, remote players (tape deck, CD-changer with analog output etc.). The signal-to-noise ratio from such sources is limited by the ADC in the SAA7707H (>75 dB). The decimation filter of the ADC attenuates the harmonic signals from this stereo encoder. For an optimum channel separation, the 38 kHz switch signal has to be phase corrected to compensate for the delay of the ADC and decimation filters. This can be adjusted with the 3-bit group delay compensation in the IAC control register. Signal frequencies above 19 kHz at the input of the multiplexer are converted to the audio base-band and are therefore not allowed.

**8.13 Signal-to-noise considerations**

Due to the pre-emphasis of FM broadcasts, the theoretical signal-to-noise ratio is approximately 3 dB higher for FM stereo in comparison with multiplexed inputs.

To avoid aliasing into the tape channel, the tape noise from the pre-amplifier must be attenuated before analog-to-digital conversion with a 1st-order 10 kHz low-pass filter. The frequency response is equalized after the stereo decoder in the DSP program before the Dolby decoder software. Using this filter, the signal-to-noise ratio of this channel is degraded by 3 dB. This results in a signal-to-noise ratio that is overall 6 dB lower than a tape input with respect to FM stereo.

**8.14 Channel separation correction**

The channel separation is approximately 50 dB at 1 kHz and 35 dB at 15 kHz. Because the frequency response of the ADC has some deviation from the flat curve around 38 kHz, a perfect channel separation cannot be obtained. Therefore, the de-multiplexed signal is corrected for crosstalk in the DSP program.

**8.15 Input selection switches**

A schematic diagram of the input selection is illustrated in Fig.5. The input selection is controlled by bits in the input selector control register. The relationship between these bits and the switches is indicated in Table 2.

**Table 2** Analog input selection

I <sup>2</sup> C-BUS SELECTION BIT			SWITCH			
AM/FM	AUX/RADIO	TAPE/AUX	SFM	SAM	SAUX	SAUX
0	0	x	1	0	0	0
1	0	x	0	1	0	0
x	1	0	0	0	1	0
x	1	1	0	0	0	1

**8.16 Analog inputs supply**

The analog input circuit has its own separate power supply connections to allow maximum filtering. These pins are  $V_{SSA1}$  for the analog ground and  $V_{DDA1}$  for the analog power supply.  $V_{SSG}$  is the connection to the guard ring which isolates the analog part from the digital filters. This pin has to be connected to the analog ground.

**8.17 Digitally controlled sampling clock (DCS)**

The crystal clock generates a continuous clock signal for the internal DSP core. In the radio mode, the stereo decoder, the RDS decoder, the ADCs and the level decimation filters have to run synchronously with the 19 kHz pilot. Therefore, a clock signal with a controlled frequency with a multiple of 19 kHz ( $9.728 \text{ MHz} = 512 \times 19 \text{ kHz}$ ) is required.

In the SAA7707H, the patented method of a non-continuous digitally controlled sampling clock has been implemented. A frequency of 9.728 MHz is generated by a special dividing mechanism of the master crystal clock. Since the dividing mechanism is fixed, only a crystal frequency of 36.86 MHz can be used.

The DCS system is controlled by up/down information from the stereo decoder. For mono transmissions, the DCS clock is still controlled by the stereo decoder loop. The output keeps the DCS free-running at a multiple frequency of  $19 \text{ kHz} \pm 2 \text{ Hz}$ . In TAPE/AUX and AM mode, the DCS clock must always be put in preset mode by the input selector control register.

## Car radio Digital Signal Processor (CDSP)

## SAA7707H

**8.18 Survey of the DCS clock settings in different modes**

The DCS clock behaves as shown in Table 3.

**Table 3** DCS clock/mode

MODE	DCS CLOCK
FM stereo	locked on 19 kHz pilot of received FM signal
FM mono	free running
AM analog inputs TAPE/AUX	fixed preset
I <sup>2</sup> C-bus inputs DCC/CD	fixed preset

**8.19 Synchronization with the core**

A 38 kHz synchronization signal is derived from the DCS clock and divided by 256.

If the external I<sup>2</sup>S-bus DCC CD is selected, the rising edge of the Word Select input signal is used to synchronize with the core.

**8.20 Interference absorption circuit**

The Interference Absorption Circuit (IAC) detects and suppresses ignition interference. This hardware IAC is a modified and digital version of the analog circuit that has already been in use for many years.

The input signal to the IAC circuit is derived from the output signal of the decimation filter. The interference detector analyses the high frequency content of this MPX signal. The discrimination between interference pulses and other signals is performed by a special Philips patented fuzzy logic-like algorithm and is based on probability calculations. This logic will send appropriate pulses to an MPX mute switch.

At Power-on, the nominal setting for an IAC with good performance characteristics is selected (all IAC control bits are 0). If an adjustment is needed, the characteristics can be adapted as described in the application manual.

**8.21 IAC testing**

The internal IAC trigger signal is visible on the MSS/P pin (pin 43) if the IAC trigger output bit of the IAC control register is set. In this mode, the effect of the parameter settings on the IAC performance can be verified.

Car radio Digital Signal Processor (CDSP)

SAA7707H

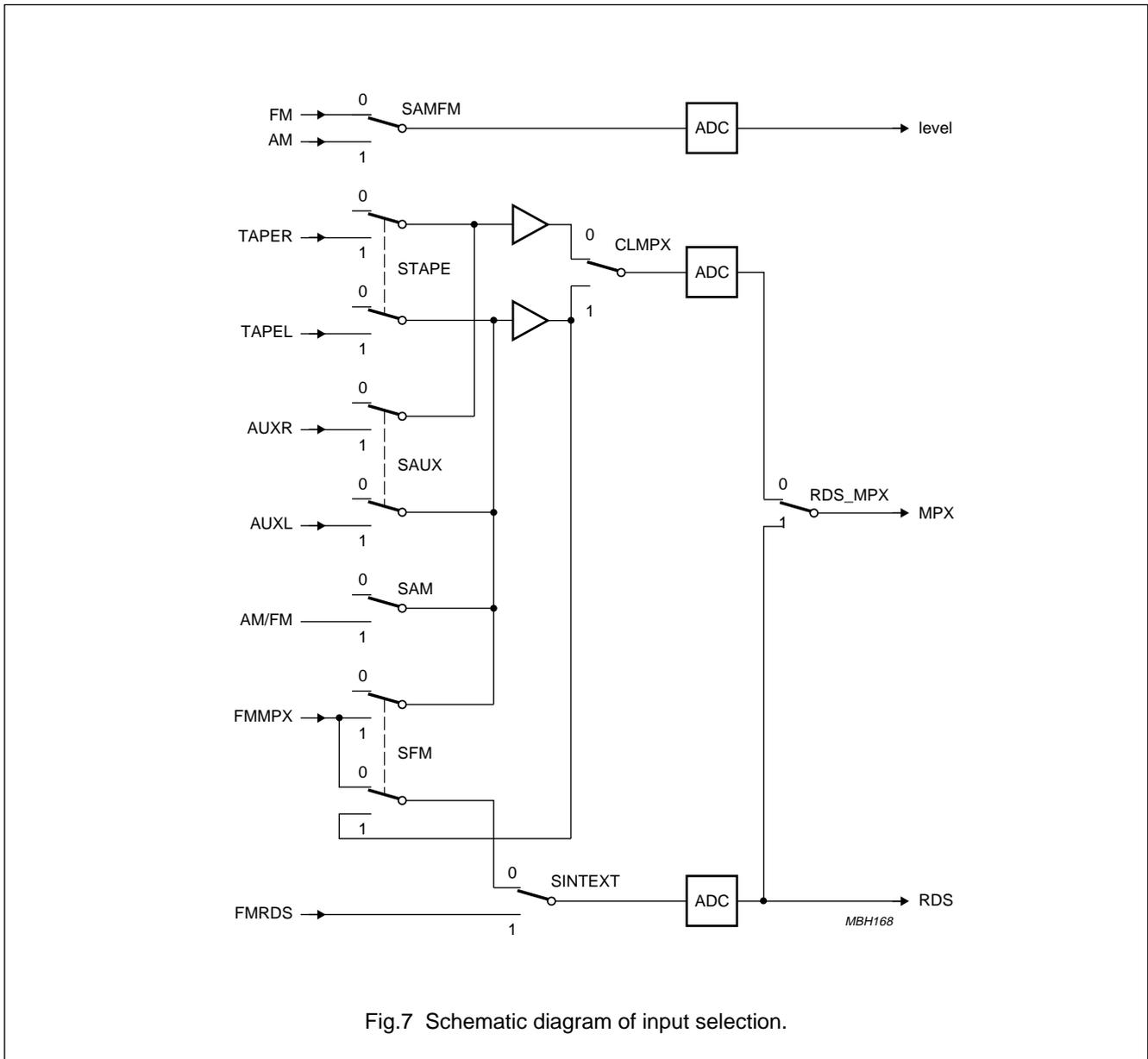


Fig.7 Schematic diagram of input selection.

- The SAMFM switch is controlled by the SEL-LEV-AM/FM bit
- The SINTEXT switch is controlled by the SEL-RDS-EXT/INT bit
- The CLMPX switch is controlled by the 38 kHz clock derived from the DCS, but is not active in FM and AM mode.

In the FM radio mode, the MPXRDS pin overrides the following switches when set to logic HIGH:

If SEL-AM/FM = 0 and SEL-AUX/RADIO = 0 and pin MPXRDS = 1, then SFM = 0, SINTEXT = 1 and MPXRDS = 1.

## Car radio Digital Signal Processor (CDSP)

SAA7707H

### 9 ANALOG OUTPUTS

#### 9.1 Digital-to-analog converters

Each of the four low-noise high dynamic range DACs consists of a 15-bit signed magnitude DAC with current output, followed by a buffer operational amplifier.

The five higher bits (bits 10 to 14) are used to control the total coarse current ratio of the 32 coarse current sources via a thermometer decoder. The nine lower bits (bits 1 to 9) are derived from a 512 transistor matrix, which acts as a passive 9-bit current divider for one of the coarse currents. The MSB (bit 15) is used as a sign bit for the signed magnitude converter and controls the direction of the total output current. A separate converter is used for each of the four audio output channels. The value of each coarse current is adjusted by the current through the external resistor connected to pin 13 ( $I_{ref(int)}$ ).

Each converter output is connected to the inverting input of one of the four internal CMOS operational amplifiers. The non-inverting input of this operational amplifier is connected to the internal reference voltage. Together with an external resistor, the current-to-audio output voltage conversion is achieved.

#### 9.2 Upsample filter

To reduce spectral components above the audio band, a fixed 4 times oversampling and interpolating 18-bit digital IIR filter is used. It is realized as a bit serial design and consists of two consecutive filters. The data path in these filters is 22 bits, to prevent overflow and to maintain a theoretical signal-to-noise ratio greater than 105 dB. The filters give an attenuation of at least 29 dB. The filter is followed by a 5 bit 1st-order noise shaper, to expand the dynamic range to more than 105 dB.

The band around multiples of the sample frequency of the DAC ( $4f_{as}$ ) is not affected by the digital filter. A capacitor can be added in parallel with the output resistor at the DAC output to further attenuate this out-of-band noise to an acceptable level.

The overall frequency spectrum at the DAC audio output without external capacitor/low-pass filter for the audio sampling frequencies ( $f_{as}$ ) of 38 kHz is illustrated in Fig.8. The detailed spectrum around  $f_{as}$  is illustrated in Fig.9 for an  $f_{as}$  of 38 kHz, 44.1 kHz and 48 kHz. The pass-band bandwidth (at -3 dB) is  $\frac{1}{2}f_{as}$ .

The word clock for the upsample filter ( $4f_{as}$ ) is derived from the audio source timing. If the internal audio source is selected, the sample frequency is fixed at 38 kHz.

For external digital sources (DCC and CD), a sample frequency from 32 to 48 kHz is possible. The sample frequency is automatically adjusted to the I<sup>2</sup>S-bus input by dividing the external bit clock. This clock is normally present in a DCC CD application. An internal digital PLL divides this clock with the integer factor needed to obtain the  $4f_{as}$  word clock. Master synchronization of this divided clock signal is obtained with a reset of the divider on the Word Select signal (trailing edge) of the I<sup>2</sup>S-bus.

In the application, the I<sup>2</sup>S-bus signal from the external source should fulfil the following requirements:

- There is a continuous (is part of the basic I<sup>2</sup>S-bus specification)  $n \times 4f_{as}$  ( $4 < n < 128$ ) I<sup>2</sup>S-bus bit clock or
- If the I<sup>2</sup>S-bus bit clock is not continuous, another  $n \times 4f_{as}$  ( $4 < n < 128$ ) continuous clock signal has to be connected to the EXCLK pin (pin 40). The divide Ext-clock mode has to be selected using the input selector control register.

The range of the internal 7-stage programmable divider of the PLL, to obtain  $4f_{as}$ , is large enough to handle 16-bit I<sup>2</sup>S-bus signals as well as master clocks up to 22 MHz from digital sources (CD, DCC, R-DAT and EBU interface) without any clock regeneration.

The PLL is used in a free-running mode to ensure that jitter on the I<sup>2</sup>S-bus signals (due to asynchronous clocking of the I<sup>2</sup>S-bus signals by the DSP core) will not influence the total harmonic distortion of the audio signal on the analog DAC part. This will, however, only operate if there is no jitter on the bit clock or when a crystal clock is used.

#### 9.3 Volume control

The total volume control has a dynamic range of more than 100 dB. With the signed magnitude noise-shaped 15-bit DAC and the internal 18 bit registers of the DSP core, a useful digital volume control range of 100 dB is possible by calculating the corresponding coefficients. The step size is freely programmable and an additional analog volume control is not needed in this design. The signal-to-noise ratio of the audio output, at full scale, is determined by the total 15 bits of the converter.

The noise at low outputs is fully determined by the noise performance of the DAC. Since it is a signed magnitude type, the noise at digital silence is also low. The disadvantage is that the total THD is higher than conventional DACs. The typical signal and noise levels as a function of the output level and the typical signal-to-noise plus THD as a function of the output level are illustrated in Fig.10.

## Car radio Digital Signal Processor (CDSP)

## SAA7707H

### 9.4 Power-on mute

To avoid any uncontrolled noise at the audio outputs after Power-on of the IC, the reference current source of the DAC is switched off. The capacitor connected to pin 21 (POM) determines the time after which this current has a soft switch-on. Consequently, at Power-on, the current audio signal outputs are always muted. The voltage output signals will show a small jump at switch-on due to the asymmetrical voltage supply of the output operational amplifiers. These types of disturbances must be eliminated via the application set-up. The output has to be set to digital silence before the POM pin is at logic HIGH. This is achieved via the DSP program control and/or a zero volume setting. The pin is internally connected to  $V_{DDO}$  with a high-ohmic resistor.

### 9.5 Power-off plop suppression

To avoid plops in a power amplifier, the supply voltage of the analog part of the DAC can be fed via a Schottky diode and an extra capacitor. In this situation, the output voltage will decrease gradually, allowing the power amplifier some extra time to switch off without audible plops.

### 9.6 Internal reference buffer amplifier of the DAC (pin $V_{ref}$ )

Using two internal resistors, half of the supply voltage ( $V_{DDO}$ ) is obtained and coupled to an internal buffer. This reference voltage is used as a DC voltage for the output operational amplifiers and as a reference voltage for the DAC. In order to obtain the lowest noise and to have the best ripple rejection, a filter capacitor has to be added between this pin and ground.

### 9.7 Internal DAC current reference

As a reference for the current at the DAC current source, a current is drawn from pin 13 ( $I_{ref(int)}$ ) to the  $V_{SSO}$  ground. The voltage at this pin is  $\frac{1}{2}V_{DDO}$  (typically 2.5 V). The maximum DAC current is equal to 4.5 times this current. When a reference resistor of 18 k $\Omega$  is used, the reference current from the DAC is 125  $\mu$ A. This results in a peak current from the four current outputs of  $4.5 \times 125 = 562.5 \mu$ A.

### 9.8 Analog outputs supply

For an optimum signal-to-noise performance, supply ripple rejection and to suppress switch-off plops, the output operational amplifiers, the analog part of the DACs and the upsample filter plus digital part have separate power supply connections.

The operational amplifiers have the  $V_{SSO}$  and  $V_{DDO}$  pins as ground and positive supply. These pins also provide the supply for the reference circuits. The analog DAC part uses the  $V_{SSA}$  and  $V_{DDA}$  pins as ground and positive supply. The upsample filter and digital part of the DAC share the  $V_{SSD1}$  and  $V_{DDD1}$  as ground and positive supply connections.

### 9.9 Clock circuit and oscillator

The SAA7707H has an on-board crystal clock oscillator. The schematic of this Pierce oscillator is illustrated in Fig.11. The active element needed to compensate for the loss resistance of the crystal is the block 'Gm'. This block is placed between the XTAL (output) and the OSC (sense) pins. The gain of the oscillator is internally controlled by the AGC block; this prevents excessive power loss in the crystal. The higher harmonics are then as low as possible.

The signal on the XTAL pin is amplified and divided by two. This 18.43 MHz signal is then used as the DSP clock signal (PH2). For the high frequency, as used in the SAA7707H, normally only third overtone crystals are available. With an external LC notch filter at the fundamental frequency, oscillation at this frequency can be avoided. The crystal frequency is chosen in such a way that the harmonics are outside the normal FM band. The crystal frequency used is 36.86 MHz.

### 9.10 Crystal oscillator supply

The power supply connections for the oscillator are separate from the other supply lines. This is to minimize the feedback from the ground bounce of the chip to the oscillator circuit. The  $V_{SSX}$  pin (pin 66) is used as ground supply and the  $V_{DDX}$  pin (pin 65) as positive supply.

### 9.11 External control pins

For external control, two input pins have been implemented. The status of these pins can be changed by applying a logic level, and is recorded in the internal status register. The functions of each pin are as follows:

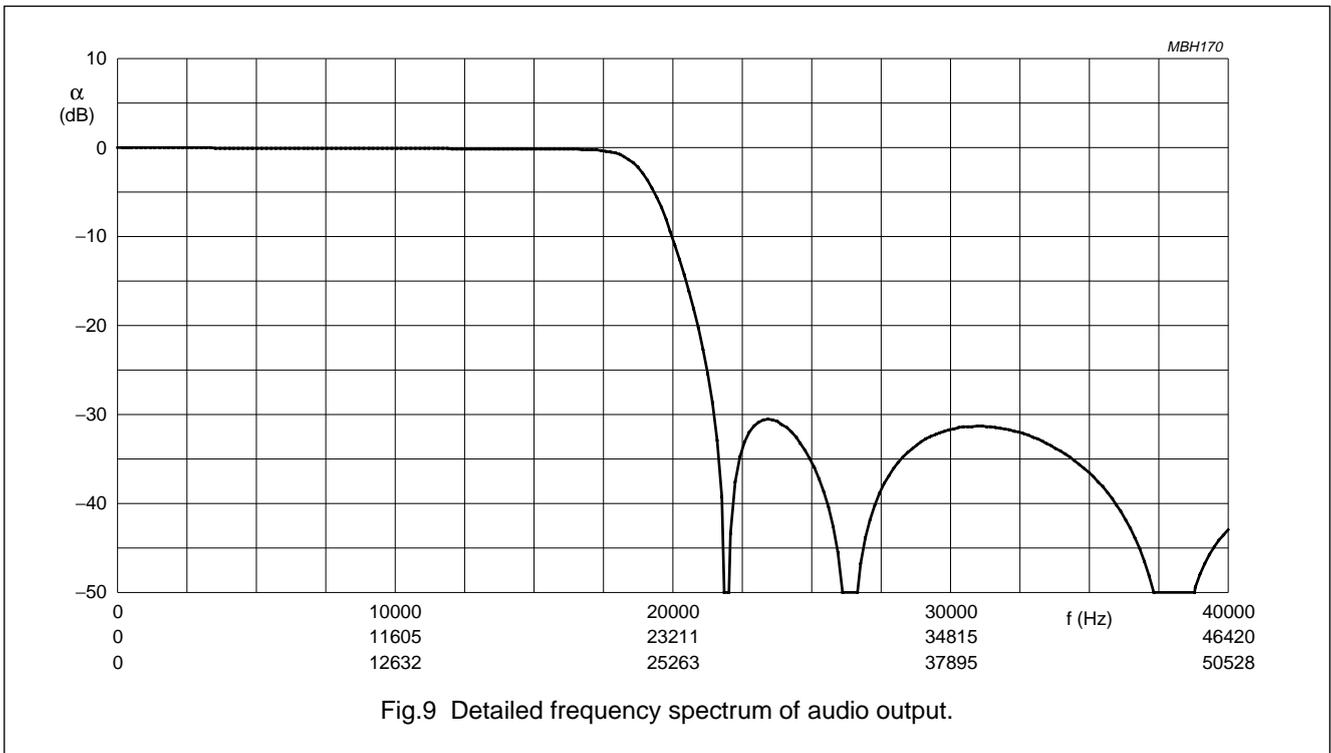
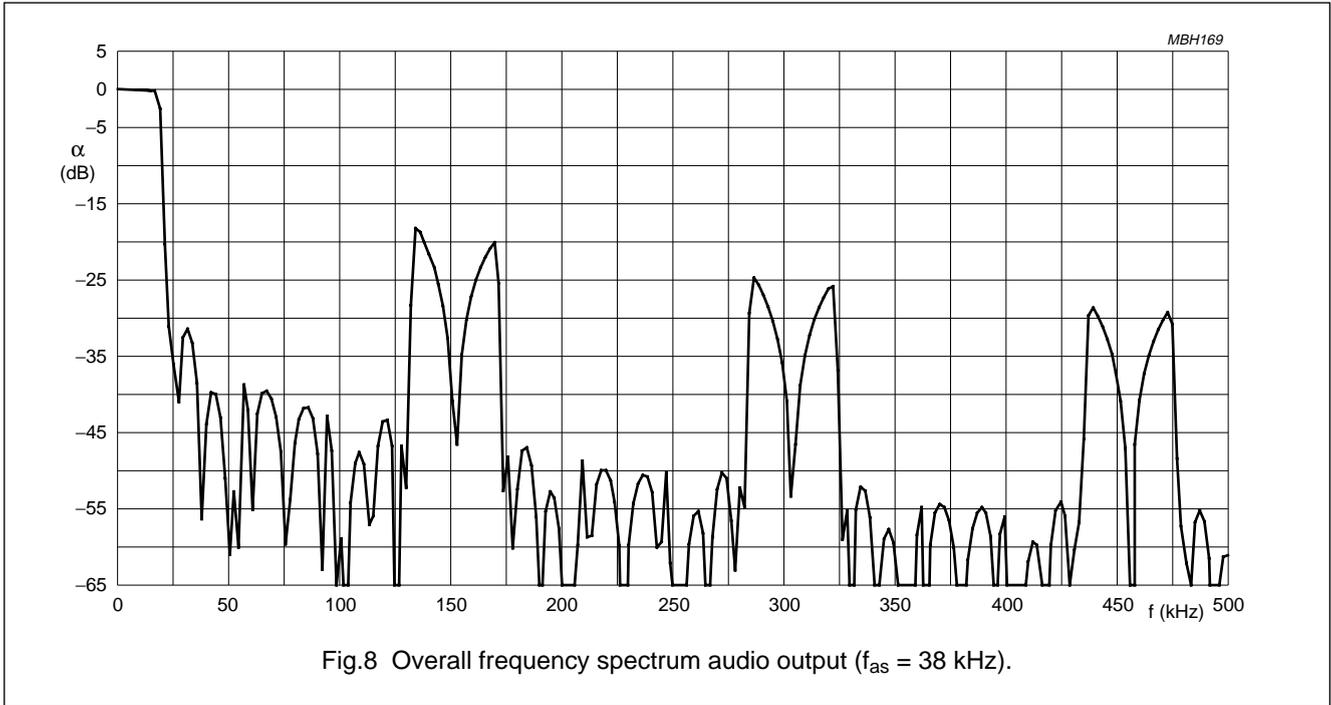
- $\overline{MUTE}$  (pin 44). Mute input (0 =  $\overline{MUTE}$ )
- DEEM (pin 45). This pin activates the de-emphasis for CD and DCC. (1 = de-emphasis on).

To control external devices, two output pins are implemented. The status of these pins is controlled by the DSP program. The functions of each pin are as follows:

Car radio Digital Signal Processor (CDSP)

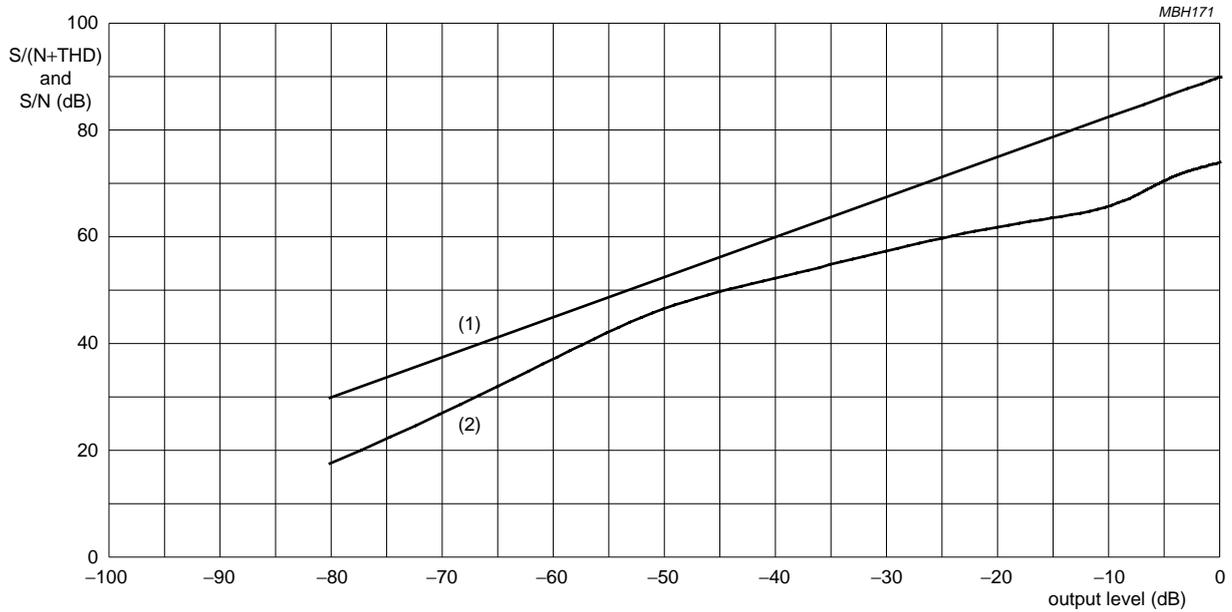
SAA7707H

- STEREO (pin 42): Indicates whether an FM broadcast is in stereo. (1 = stereo)
- MSS/P (pin 43): Indicates a pause in FM or tape search mode (1 = pause). This is also the IAC trigger output for IAC alignment if the corresponding I<sup>2</sup>C-bus bit is set.



Car radio Digital Signal Processor (CDSP)

SAA7707H



- (1) Signal-to-noise.
- (2) Signal-to-noise + total harmonic distortion.

Fig.10 Typical signal-to-noise level and signal-to-noise plus THD as a function of output level.

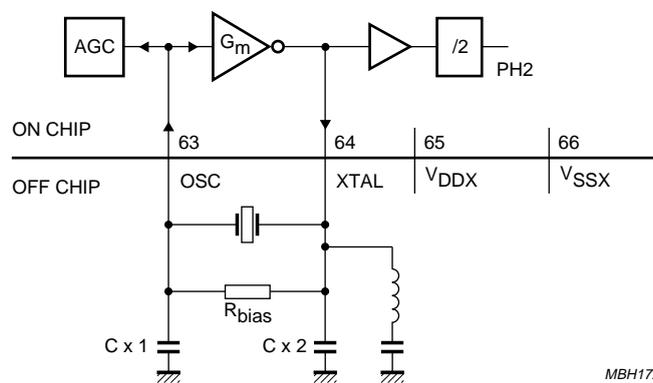


Fig.11 Schematic diagram of the oscillator circuit.

## Car radio Digital Signal Processor (CDSP)

## SAA7707H

**10 I<sup>2</sup>S-BUS DESCRIPTION****10.1 I<sup>2</sup>C-bus control (pins SCL and SDA)**

For external control of the SAA7707H, a standard I<sup>2</sup>C-bus is implemented. There are two different types of control instructions:

- Instructions to control the DSP program, programming the coefficient RAM and reading the values of parameters (level, multi-path etc.)
- Instructions controlling the DATA flow, such as source selection, IAC control and clock speed.

**10.2 I<sup>2</sup>S-bus description**

For communication with external digital sources and/or additional external processors, the I<sup>2</sup>S-bus digital interface is used. It is a serial 3-line bus, having one line for Serial Data (SD), one line for Serial Clock (SCK) and one line for the Word Select (WS). For external processors, the CDSP acts as a master transmitter; for external digital sources the CDSP acts as a slave. The communication with the external processor and external digital sources are separated, to allow both features at the same time.

Figure 12 shows an extract of the Philips I<sup>2</sup>S-bus specification interface report regarding the general timing and format of the I<sup>2</sup>S-bus. Word select logic 0 means left channel word; word select logic 1 means right channel word.

The serial data is transmitted in twos complement with the MSB first. One clock period after the negative edge of the Word Select line, the MSB of the left channel is transmitted. Data is synchronized with the negative edge of the clock and latched at the positive edge.

As inputs from an external processor for the four audio channels, two data lines have been implemented.

**10.3 Communication with external digital audio sources (DCC + CD-WS/CL/Data pins)**

For communication with external digital audio sources, two additional I<sup>2</sup>S-bus inputs are available. They each have clock, data and Word Select input lines with a maximum useful data length of 18 bits. The external source is master and supplies the clock. The input selection and port selection is controllable via the input selector control register. The DSP program is synchronized with the external source via the Word Select signal.

The input allows a variety of clock frequencies, sample frequencies and word lengths.

The Word Select line automatically determines the SAA7707H sampling frequency.

Using the Digital Source Selector (see Fig.1), one of the three possible input sources is selected. The selected audio data channels are input to two 18-bit wide memory mapped I/O registers of the DSP named Input Left and Input Right.

Except for the  $4f_{as}$  pulse to control the upsample filter (see Section 9.2), other synchronization signals such as internal Word Select are derived from the I<sup>2</sup>S-bus input signals.

The input bit clock is used as a bit clock for the external processor. As a consequence, a clock pulse input signal with less than 18 bits will result in a communication with an external processor of the same number of bits. In this event, the trailing bits of the 18-bit input registers will be zero.

If the I<sup>2</sup>S-bus driver outputs of the external digital source ICs have 3-state outputs, they can all be connected on one single I<sup>2</sup>S-bus input.

**10.4 Communication with external processors and other devices (EXWS/CL/EXDAT1 and EXDAT2)**

For communication with external processors, delay lines or other I<sup>2</sup>S-bus controllable devices, a complete dual-channel 18-bit output bus is implemented.

The SAA7707H acts as the master transmitter and the external device has to be synchronized with the Word Select line.

As input for the processed data, two data input lines have been implemented that are processed synchronously with the data output to the external processor (see Table 4). This enables, in total, a feedback of two stereo audio channels.

For this communication, the DSP core has the following 18-bit memory mapped I/O registers available:

**Table 4** DSP core I/O registers

INPUT	OUTPUT
EXDAT1 left/right	EXDAT left/right
EXDAT2 left/right	

The DSP program moves data from the two external I<sup>2</sup>S-bus data output registers to the external processor and reads it back from the two or four external I<sup>2</sup>S-bus data input registers. The hardware of the bus can be enabled by the input control register.

## Car radio Digital Signal Processor (CDSP)

SAA7707H

To minimise electro magnetic interference (EMI), the output has to be disabled if the output is not used.

The timing diagram of the communication is illustrated in Fig.13.

### 10.5 Relationship between external input and external output

The stereo decoder output has an internal I<sup>2</sup>S-bus format with 32 clock pulses per channel for 18 valid and 14 zero data bits. Providing that the stereo decoder output is used, the communication with the external processor will also have 32 clock pulses per channel for 18 valid and 14 zero data bits.

When an external digital source is selected, the number of valid bits and clock pulses of this source determines the output to the external processor. This relationship is shown in Table 5.

**Table 5** Relationship between external input and external output.

INPUT CLOCK BITS	INPUT DATA BITS	OUTPUT CLOCK BITS	OUTPUT DATA BITS
>32	≥18	32	18
≥18 and ≤32	≥18	as input	18
≥18 and ≤32	<18	as input	18
<18	<18	as input	as input

### 10.6 RDS decoder (RDSCLK and RDSDAT)

The RDS decoder recovers the additional inaudible RDS information transmitted by FM radio broadcasting. The (buffered) data is provided as an output for further processing by a suitable decoder. The operational functions of the decoder are in accordance with EBU specification *EN 50067*.

The RDS decoder has three different functions:

1. Clock and data recovery from the MPX signal
2. Buffering of 16 bits, if selected
3. Interfacing with the microcontroller.

### 10.7 Clock and data recovery

The RDS chain has a separate input. This enables RDS updates during tape play and also the use of a second receiver for monitoring the RDS information of signals from another transmitter (double tuner concept).

In this way, it can be performed without interruption of the audio program. The MPX signal from the main tuner of the car radio can be connected to this RDS input via the built-in source selector.

The input selection is controlled by the input selector control register.

For FM stereo reception, the clock of the total chip is locked to the stereo pilot (19 kHz multiple). For FM mono, the DCS loop keeps the DCS clock around the same 19 kHz multiple. In all other cases, such as AM reception or tape, the DCS circuit has to be set to a preset position. Under these conditions, the RDS system is always clocked by the DCS clock in a 38 kHz (4 × 9.5 kHz) based sequence.

### 10.8 Timing of clock and data signals

The timing of the clock and data output is derived from the incoming data signal. Under stable conditions, the data will remain valid for 400 μs after the clock transition.

The timing of the data change is 100 μs before a positive clock change. This timing is suitable for positive and negative triggered interrupts on a microcontroller. The RDS timing is illustrated in Fig.14.

During poor reception, it is possible that errors in phase may occur. Consequently the duty cycle of the clock and data signals will vary from a minimum of 0.5 times to a maximum of 1.5 times the standard clock periods. Normally, errors in phase do not occur on a cyclic basis.

### 10.9 Buffering of RDS data

The repetition frequency of RDS data is approximately 1187 Hz. This results in an interrupt on the microcontroller every 842 μs. In a second mode, the RDS interface has a double 16-bit buffer.

### 10.10 Buffer interface

The RDS interface buffers 16 data bits. Each time 16 bits are received, the data line is pulled down and the buffer is overwritten. The control microcontroller has to monitor the input data line at least every 13.5 ms. This mode is selected by the input selector control register. The interface signals from the RDS decoder and the microcontroller in the buffer mode are illustrated in Fig.15. When the buffer is filled with 16 bits, the data line is pulled down.

The data line will remain LOW until reading from the buffer is started, by pulling down the clock line. The first data bit is clocked out.