DATA SHEET

PCF8577C
LCD direct/duplex driver with I²C-bus interface

Product specification
Supersedes data of July 1993
File under Integrated Circuits, IC12

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Philips
Semiconductors

PHILIPS

LCD direct/duplex driver with I²C-bus interface

PCF8577C

FEATURES

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2.5 to 6 V
- Low power consumption
- I²C-bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device subaddress boundaries
- Display memory switching in direct drive mode
- May be used as I²C-bus output expander
- System expansion up to 256 segments
- Power-on reset blanks display.

GENERAL DESCRIPTION

The PCF8577C is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex configuration.

The two-line I²C-bus interface substantially reduces wiring overheads in remote display applications. I²C-bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware subaddressing and display memory switching (direct drive mode).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8577CP	DIP40	plastic dual in-line package; 40 leads (600 mil)	SOT129-1
PCF8577CT	VSO40	plastic very small outline package; 40 leads	SOT158A
PCF8577CT	–	V6040 in blister tape	–
PCF8577CU/10	–	chip on film-frame-carrier (FFC)	–

BLOCK DIAGRAM

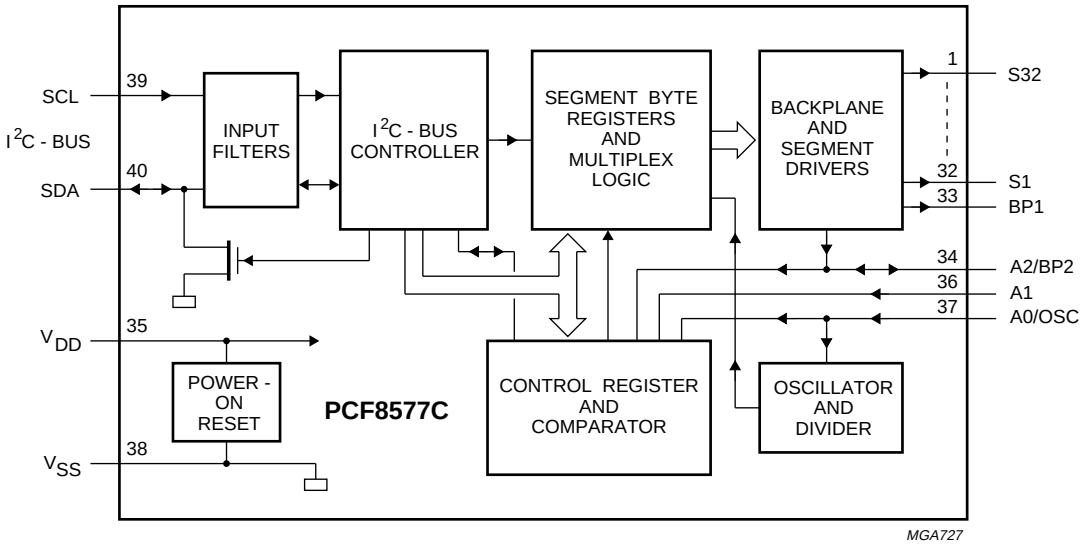


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
S32 to S1	1 to 32	segments outputs
BP1	33	cascade sync input/backplane output
A2/BP2	34	hardware address line and cascade sync input/backplane output
V_{DD}	35	positive supply voltage
A1	36	hardware address line input
A0/OSC	37	hardware address line and oscillator pin input
V_{SS}	38	negative supply voltage
SCL	39	I²C-bus clock line input
SDA	40	I²C-bus data line input/output

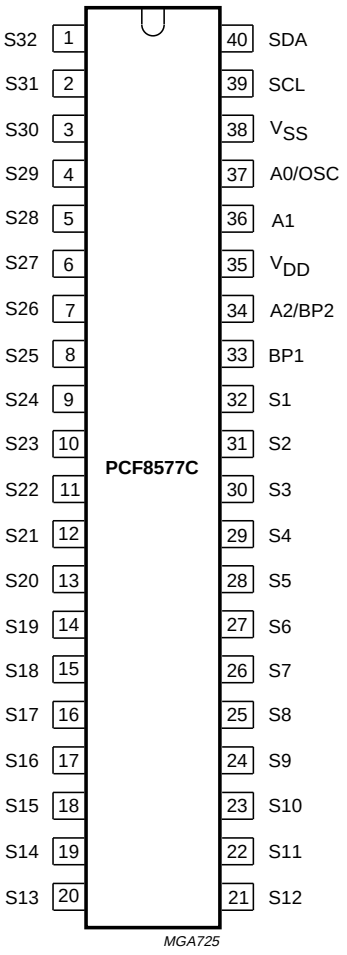


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Hardware subaddress A0, A1, A2

The hardware subaddress lines A0, A1 and A2 are used to program the device subaddress for each PCF8577C connected to the I²C-bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

1. Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.
2. Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.
3. In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.
4. In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577C has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator (see Figs 15 and 16). For correct start-up of the oscillator after power on, the resistor and capacitor must be connected to the same V_{SS}/V_{DD} as the chip. In an expanded system containing more than one PCF8577C the backplane signals are usually common to all devices and only one oscillator is required. The devices which are not used for the oscillator are put into the cascade mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the cascade mode each PCF8577C is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accessible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There is one slave address for the PCF8577C (see Fig.6). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C-bus protocol Fig.7), i.e. all addressed devices respond to control commands sent on the I²C-bus.

The control register is shown in more detail in Fig.3. The least-significant bits select which device and which segment byte register is loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware subaddress input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

After each segment byte is loaded the SBV is incremented automatically. Thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers in all addressed chips, auto-incremented loading may proceed across device boundaries provided that the hardware subaddresses are arranged contiguously.

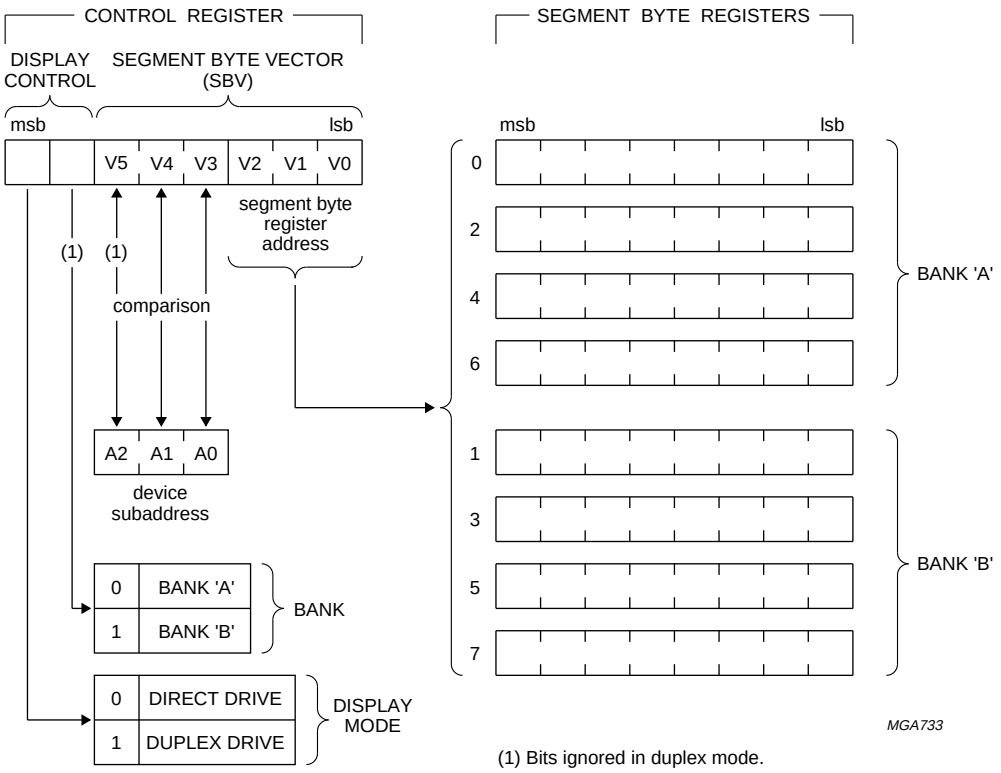
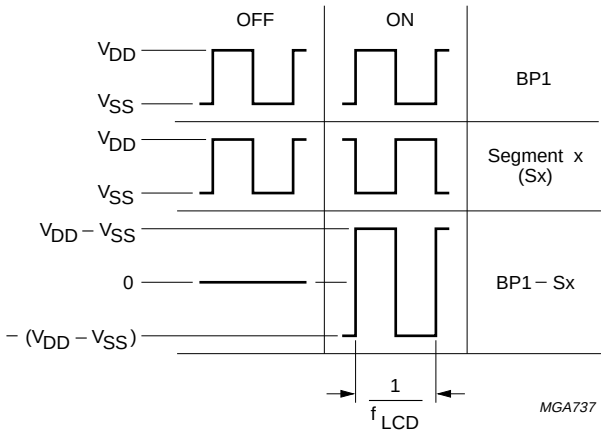


Fig.3 PCF8577C register organization.



$V_{on(rms)} = V_{DD} - V_{SS}$; $V_{off(rms)} = 0$.

Fig.4 Direct drive mode display output waveforms.

Direct drive mode

The PCF8577C is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are required to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A), setting the BANK bit to logic 1 selects odd bytes (BANK B).

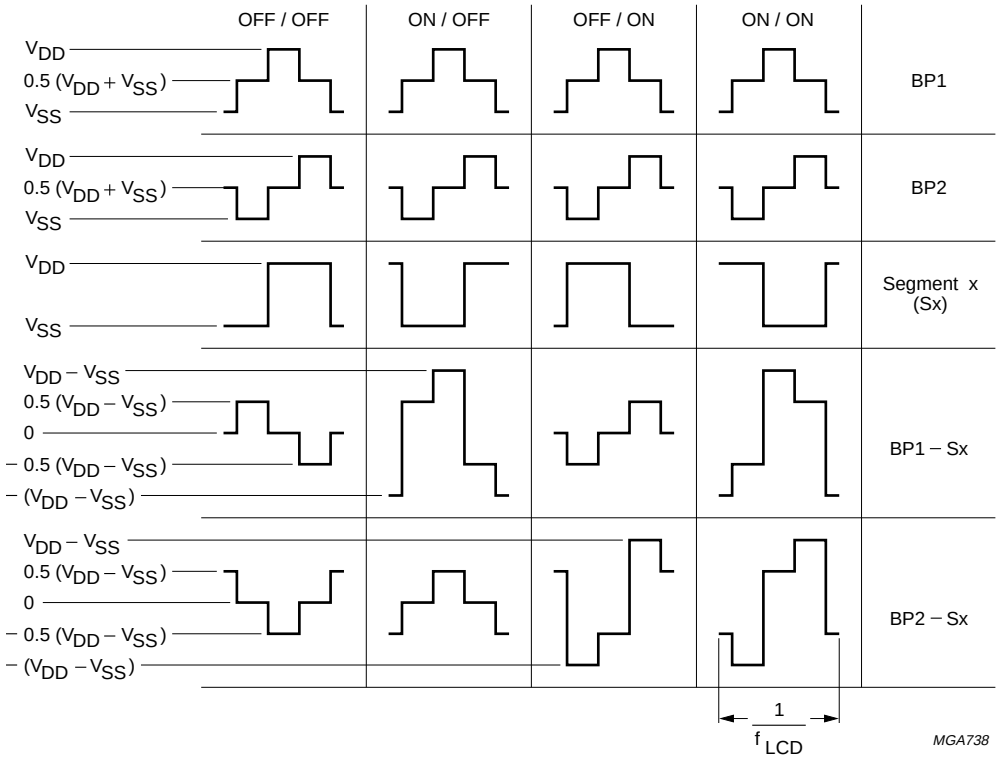
In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig.4.

Duplex mode

The PCF8577C is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are required to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig.5.



$V_{on(rms)} = 0.791 (V_{DD} - V_{SS})$; $V_{off(rms)} = 0.354 (V_{DD} - V_{SS})$.

$$\frac{V_{on(rms)}}{V_{off(rms)}} = 2.236$$

Fig.5 Duplex mode display output waveforms.

Power-on reset

At power-on reset the PCF8577C resets to a defined starting condition as follows:

1. Both backplane outputs are set to V_{SS} in master mode; to 3-state in cascade mode.
2. All segment outputs are set to V_{SS}.
3. The segment byte registers and control register are cleared.
4. The I²C-bus interface is initialized.

Slave address

The PCF8577C slave address is shown in Fig.6.

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

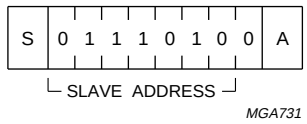


Fig.6 PCF8577C slave address.

I²C-bus protocol

The PCF8577C I²C-bus protocol is shown in Fig.7.

The PCF8577C is a slave receiver and has a fixed slave address (see Fig.6). All PCF8577Cs with the same slave address acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577C connected to the I²C-bus. All addressed devices acknowledge the control byte. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data will remain unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577C gives an acknowledge. Loading is terminated by generating a stop (P) condition.

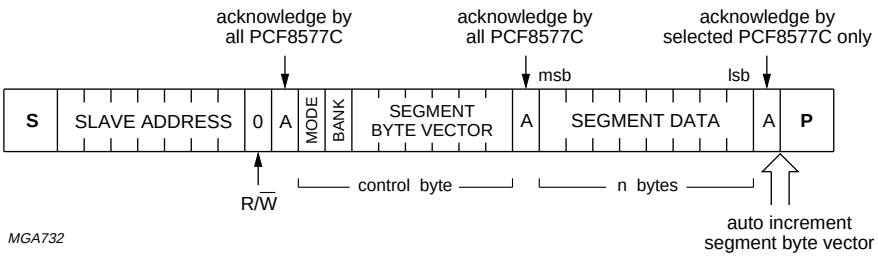


Fig.7 I²C-bus protocol.

Display memory mapping

The mapping between the eight segment registers and the segment outputs S1 to S32 is given in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode. In duplex mode even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 1 Segment byte-segment driver mapping in direct drive mode

MODE	BANK	V 2	V 1	V 0	SEGMENT/ BIT/ REGISTER	MSB 7	6	5	4	3	2	1	LSB 0	BACK-PLANE
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

Table 2 Segment byte-segment driver mapping in duplex mode

MODE	BANK(1)	V 2	V 1	V 0	SEGMENT/ BIT/ REGISTER	MSB 7	6	5	4	3	2	1	LSB 0	BACK-PLANE
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

Note

1. Where x = don’t care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the I²C-bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

Start and stop conditions

Both data and clock lines remain HIGH when the I²C-bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

System configuration

A device generating a message is a ‘transmitter’, a device receiving a message is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the I²C-bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

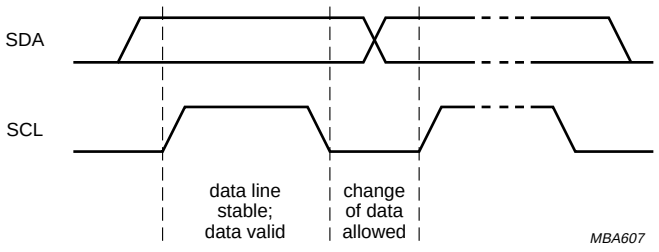


Fig.8 Bit transfer.

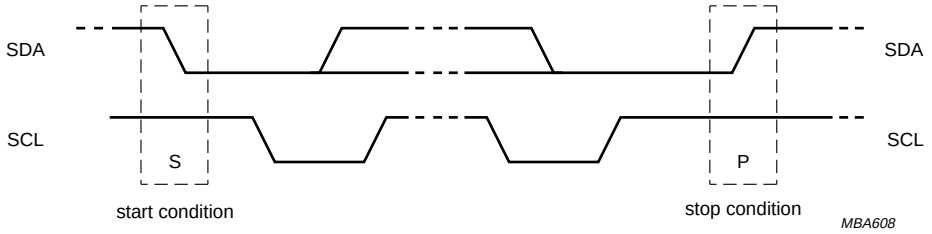


Fig.9 Definition of the start and stop conditions.

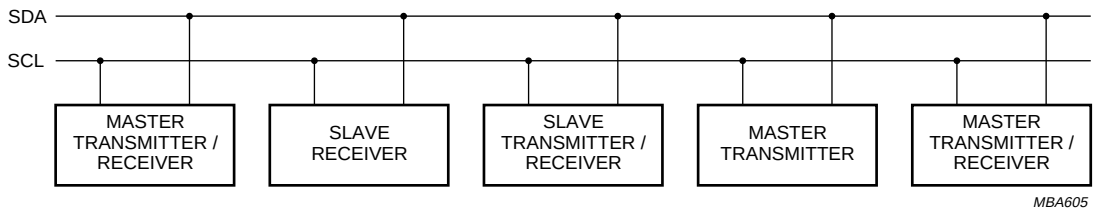


Fig.10 System configuration.

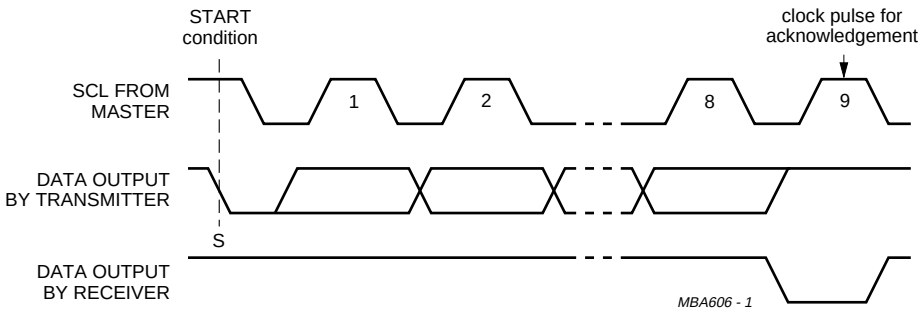


Fig.11 Acknowledgement on the I²C-bus.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+8.0	V
V_I	input voltage on pin		–0.5	V_{DD} + 0.5	V
I_{DD}; I_{SS}	V_{DD} or V_{SS} current		–50	+50	mA
I_I	DC input current		–20	+20	mA
I_O	DC output current		–25	+25	mA
P_{tot}	power dissipation per package	note 1	–	500	mW
P_O	power dissipation per output		–	100	mW
T_{stg}	storage temperature		–65	+150	°C

Note

1. Reduce by 7.7 mW/K when $T_{amb} > 60$ °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices.

DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; T_{amb} = –40 to 85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Supply						
V_{DD}	supply voltage		2.5	–	6	V
I_{DD}	supply current for non-specified inputs at V_{DD} or V_{SS}	no load; f_{SCL} = 100 kHz; R_{osc} = 1 MΩ; C_{osc} = 680 pF		50	125	µA
		no load; f_{SCL} = 0; R_{osc} = 1 MΩ; C_{osc} = 680 pF	–	25	75	µA
		no load; f_{SCL} = 0; R_{osc} = 1 MΩ; C_{osc} = 680 pF; V_{DD} = 5 V; T_{amb} = 25 °C	–	25	40	µA
		no load; f_{SCL} = 0; direct mode; A0/OSC = V_{DD}; V_{DD} = 5 V; T_{amb} = 25 °C	–	10	20	µA
V_{POR}	power-on reset level	note 2	–	1.1	2.0	V
Input A0						
V_{IL1}	LOW level input voltage		0	–	0.05	V
V_{IH1}	HIGH level input voltage		V_{DD} – 0.05	–	V_{DD}	V
Input A1						
V_{IL2}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH2}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
Input A2						
V_{IL3}	LOW level input voltage		0	–	0.10	V
V_{IH3}	HIGH level input voltage		V_{DD} – 0.10	–	V_{DD}	V
Input SCL; SDA						
V_{IL4}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH4}	HIGH level input voltage		$0.7V_{DD}$	–	6	V
C_I	input capacitance	note 3	–	–	7	pF
Output SDA						
I_{OL}	LOW level output current	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
A1; SCL; SDA						
I_{L1}	leakage current	$V_I = V_{DD}$ or V_{SS}	–1	–	+1	µA
A2/BP2; BP1						
I_{L2}	leakage current	$V_I = V_{DD}$ or V_{SS}	–5	–	+5	µA
A2/BP2						
I_{pd}	pull-down current	$V_I = V_{DD}$	–5	–1.5	–	µA
A0/OSC						
I_{L3}	leakage current	$V_I = V_{DD}$	–1	–	–	µA
Oscillator						
I_{OSC}	start-up current	$V_I = V_{SS}$	–	1.2	5	µA
LCD outputs						
V_{BP}	DC component of LCD driver		–	±20	–	mV
I_{OL1}	LOW level segment output current	V_{DD} = 5 V; V_{OL} = 0.8 V; note 4	0.3	–	–	mA
I_{OH1}	HIGH level segment output current	V_{DD} = 5 V; $V_{OH} = V_{DD}$ – 0.8 V; note 4	–	–	–0.3	mA
R_{BP}	backplane output resistance (BP1; BP2)	$V_O = V_{SS}$ or V_{DD} or $(V_{SS} + V_{DD})/2$; note 5	–	0.4	5	kΩ

Notes

1. Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. Outputs measured one at a time; V_{DD} = 5 V; I_{load} = 100 µA.

AC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; T_{amb} = –40 to 85 °C; unless otherwise specified. All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
f_{LCD}	display frequency	C_{osc} = 680 pF; R_{osc} = 1 MΩ	65	90	120	Hz
t_{BS}	driver delays with test loads	V_{DD} = 5 V	–	20	100	µs
I²C-bus						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable spike width on I²C-bus	T_{amb} = 25 °C	–	–	100	ns
t_{BUF}	I²C-bus free time		4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time		4.0	–	–	µs
$t_{HD;STA}$	start condition hold time		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1.0	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	stop condition set-up time		4.0	–	–	µs

Note

1. Typical conditions: V_{DD} = 5 V; T_{amb} = 25 °C.

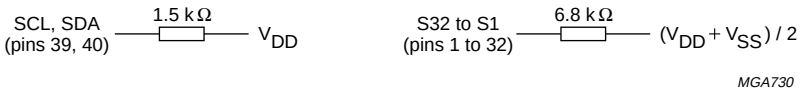


Fig.12 Test loads.

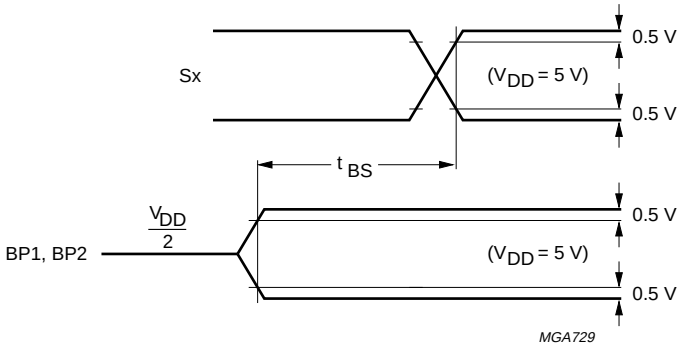


Fig.13 Driver timing waveforms.

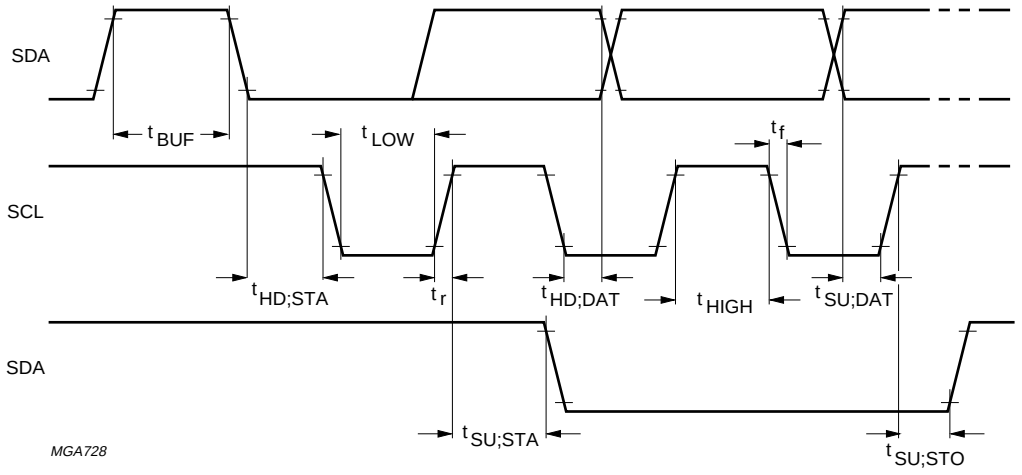


Fig.14 I²C-bus timing diagram; rise and fall times refer to V_{IL} and V_{IH}.

APPLICATION INFORMATION

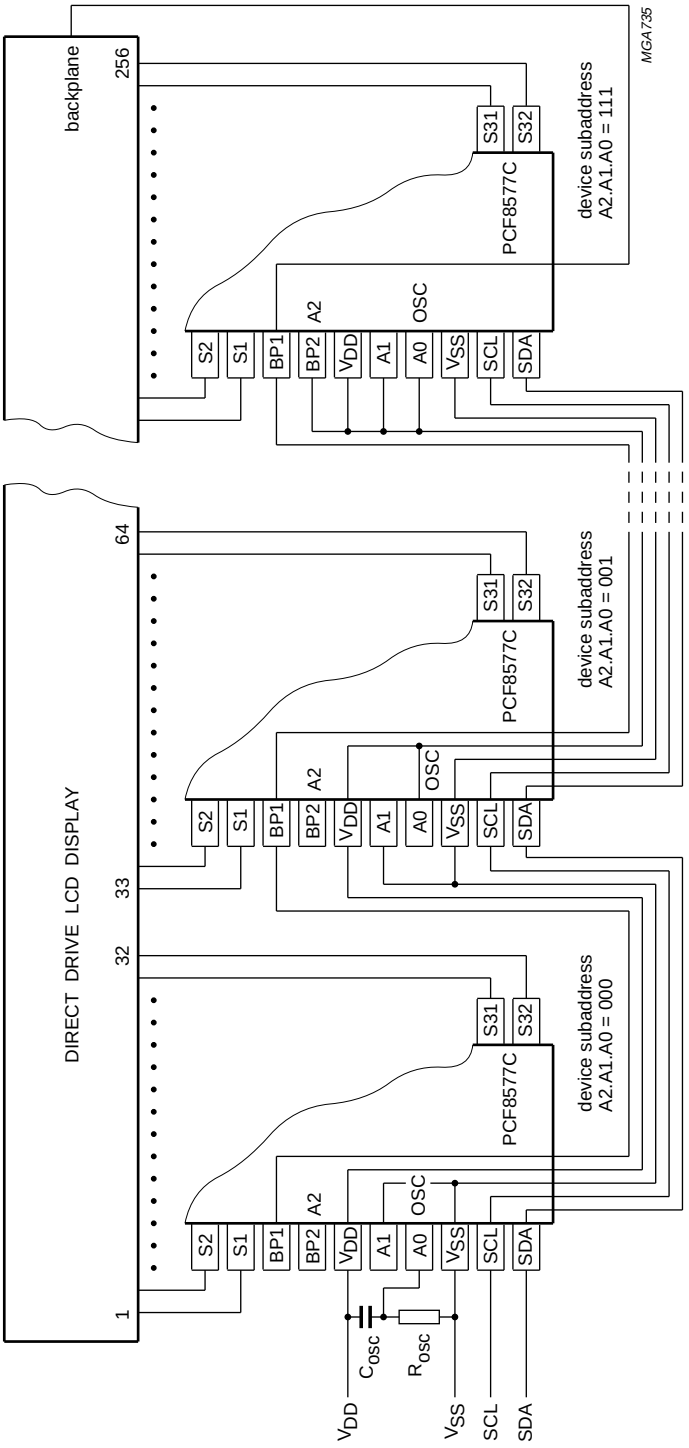


Fig.15 Direct display driver; expansion to 256 segments using eight PCF8577Cs.

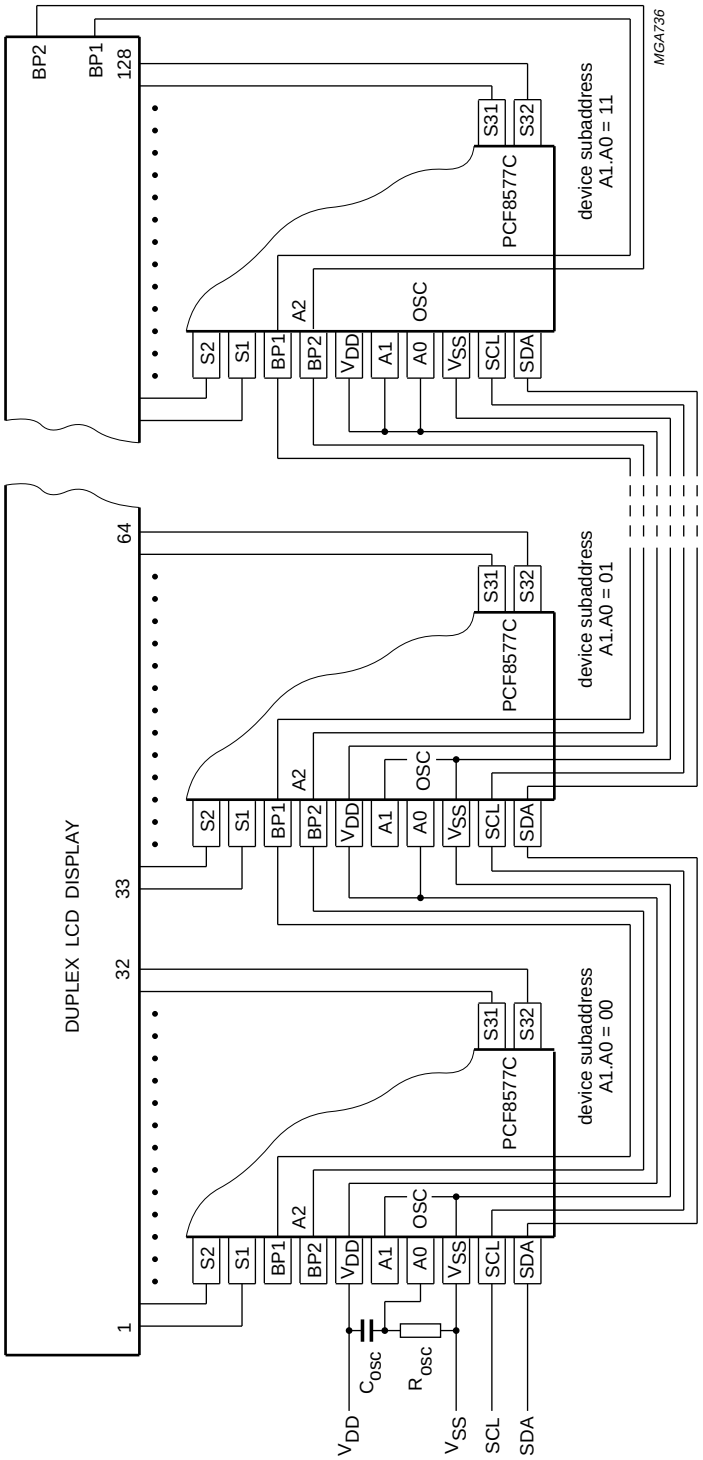
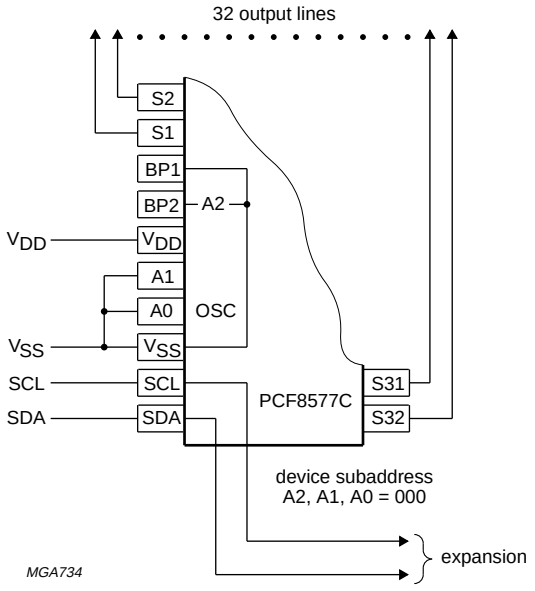


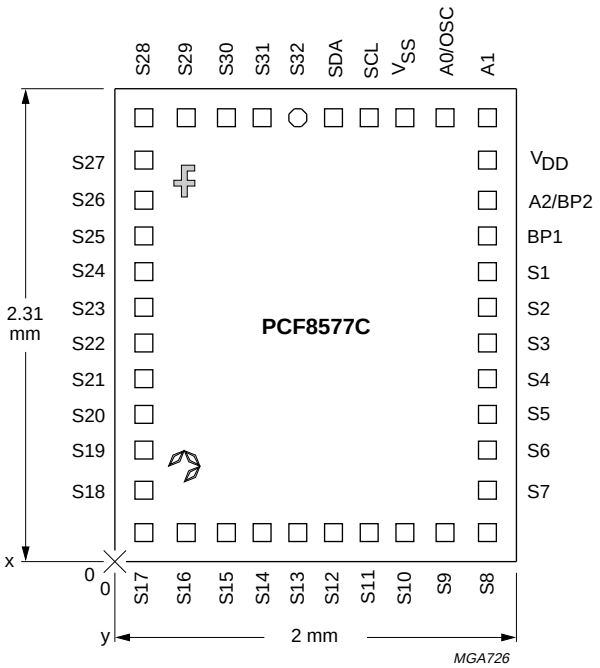
Fig.16 Duplex display; expansion to 2 × 128 segments using four PCF8577Cs.



MODE bit must always be set to logic 0 (direct drive).
BANK switching is permitted.
BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation).

Fig.17 Use of PCF8577C as a 32-bit output expander in I²C-bus application.

CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area = 4.62 mm^2.
Thickness = 381 ±25 μm.
n-substrate (back) connected to V_{DD}.
Bonding pad dimensions = 110 μm × 110 μm.

Fig.18 Bonding pad locations.

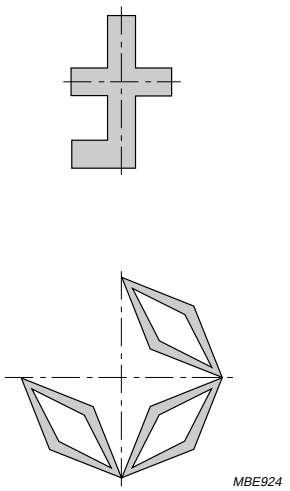


Fig.19 Reference marks.

Table 3 Bonding pad locations (dimensions in μm)

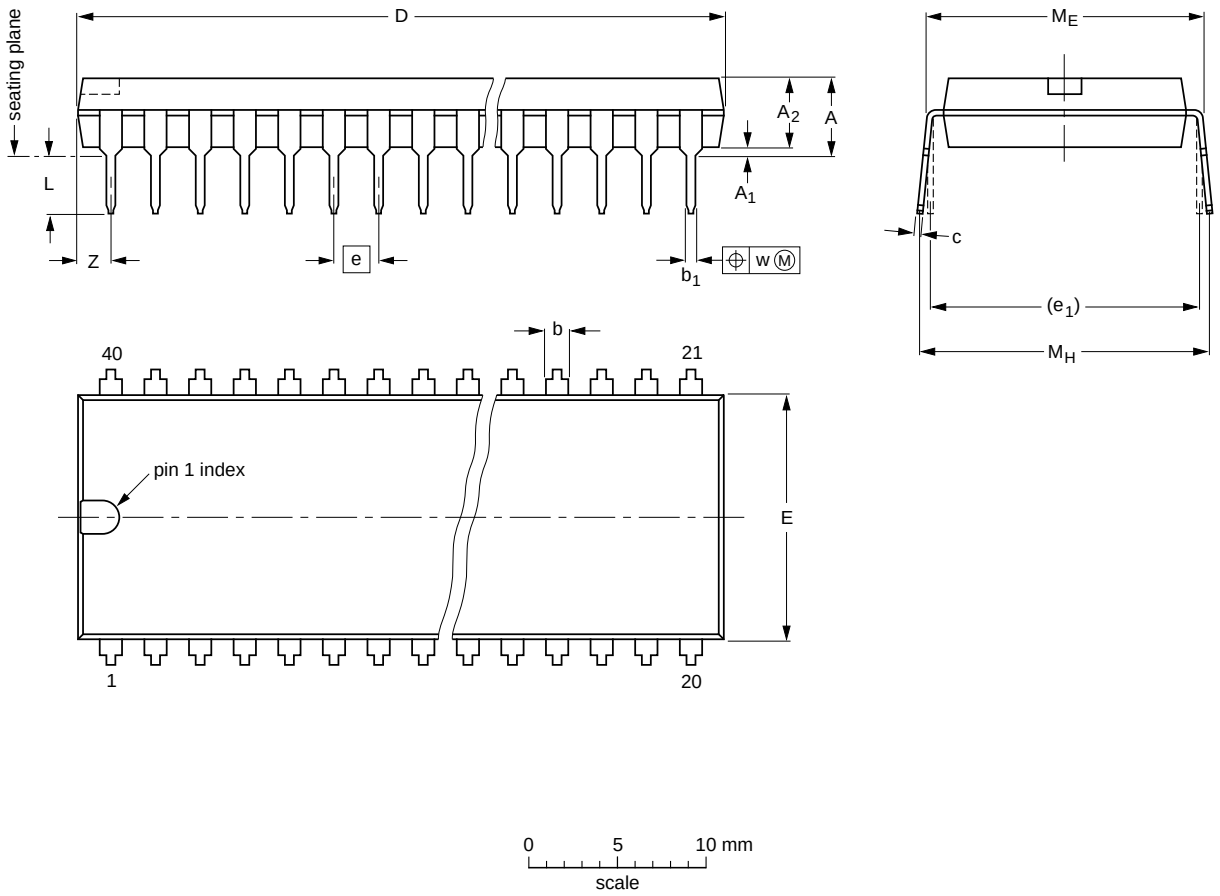
All x and y co-ordinates are referenced to bottom left corner, see Fig.18.

SIGNAL	PAD POSITION CENTERED	
	x	y
S32	–86	941
S31	–257	941
S30	–428	941
S29	–599	941
S28	–836	941
S27	–836	769
S26	–836	598
S25	–836	427
S24	–836	256
S23	–836	85
S22	–836	–86
S21	–836	–257
S20	–836	–428
S19	–836	–599
S18	–836	–770
S17	–836	–941
S16	–599	–941
S15	–428	–941
S14	–257	–941
S13	–86	–941
S12	85	–941
S11	256	–941

SIGNAL	PAD POSITION CENTERED	
	x	y
S10	427	–941
S9	598	–941
S8	836	–941
S7	836	–770
S6	836	–599
S5	836	–428
S4	836	–257
S3	836	–86
S2	836	85
S1	836	256
BP1	836	427
A2/BP2	836	598
V_{DD}	836	769
A1	836	941
A0/OSC	598	941
V_{SS}	427	941
SCL	256	941
SDA	85	941
Recpats		
C	–586	–699
F	–580	663

PACKAGE OUTLINES

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

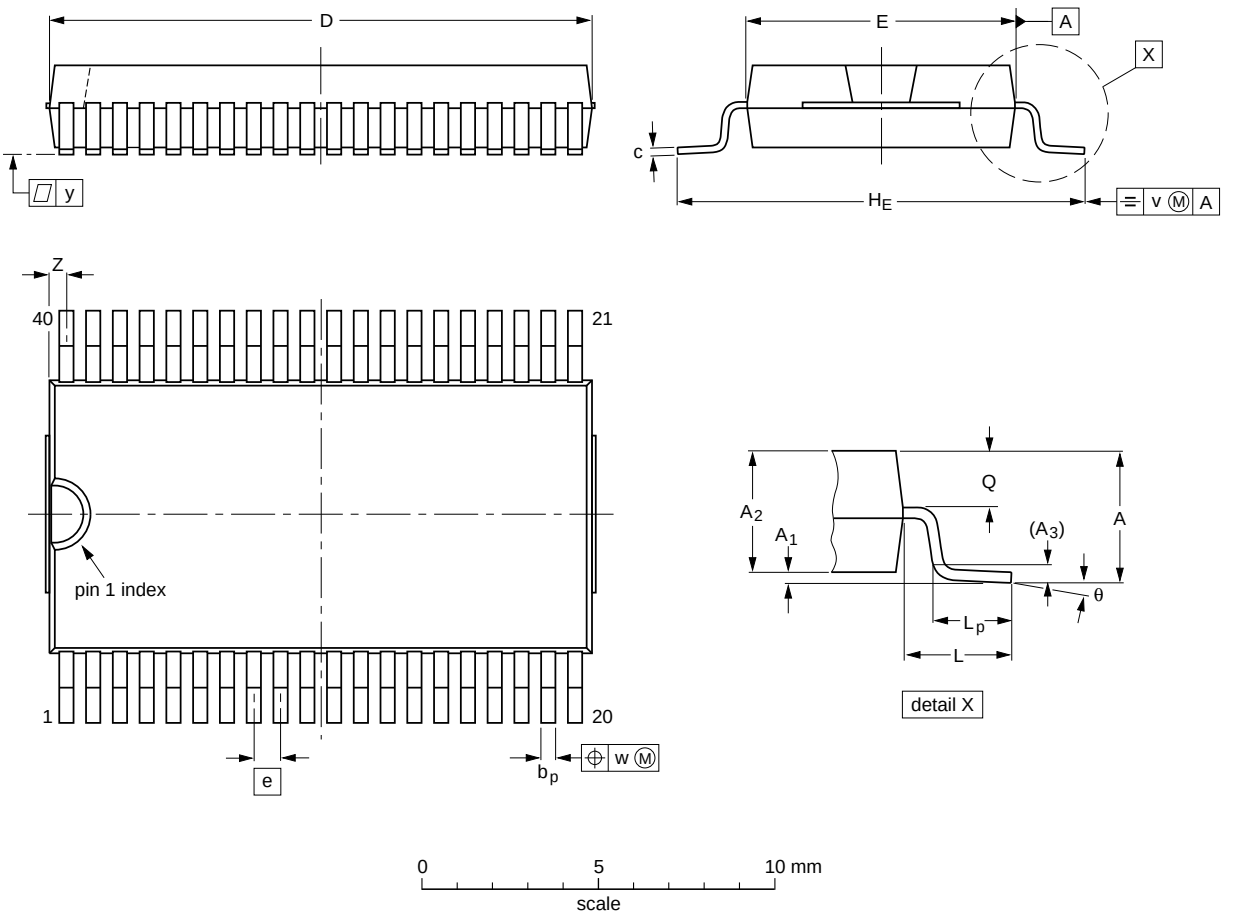
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

VSO40: plastic very small outline package; 40 leads **SOT158-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.70	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7^o 0^o
inches	0.11	0.012 0.004	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	

Notes

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT158-1						~~92-11-17~~ 95-01-24

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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