

DATA SHEET

TDA1310A Stereo Continuous Calibration DAC (CC-DAC)

Preliminary specification

May 1994

Supersedes data of TDA1310; TDA1310T July 1993

File under Integrated Circuits, IC01

Philips Semiconductors



PHILIPS

Stereo Continuous Calibration DAC (CC-DAC)

TDA1310A

FEATURES

- Space saving package DIL8 or SO8
- Low power consumption
- Wide dynamic range (16-bit resolution)
- Continuous Calibration (CC) concept
- Easy application:
 - Single 3 to 5 V supply rail
 - Output current and bias current are proportional to the supply voltage
- Fast settling time permits 2×, 4× and 8× oversampling (serial input) or double speed operation at 4× oversampling
- Internal bias current ensures maximum dynamic range
- Wide operating temperature range (-40 t +85 °C)
- Compatible with most current Japanese input formats:
 - Time multiplexed
 - Two's complement
 - TTL
- No zero-crossing distortion.

GENERAL DESCRIPTION

The TDA1310A is a device of a new generation of Digital-to-Analog Converters (DACs) which embodies the innovative technique of Continuous Calibration. The largest bit-currents are repeatedly generated by one single current reference source. This duplication is based upon an internal charge storage principle having an accuracy insensitive to ageing, temperature and process variations.

The TDA1310A is fabricated in a 1.0 μm CMOS process and features an extremely low power dissipation, small package size and easy application. Furthermore, the accuracy of the intrinsic high coarse-current combined with the implemented symmetrical offset decoding method precludes zero-crossing distortion and ensures high quality audio reproduction. Therefore, the CC-DAC is eminently suitable for use in (portable) digital audio equipment.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA1310A	8	DIL8	plastic	SOT97DE
TDA1310AT	8	SO8	plastic	SOT96AG

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		3	5.0	5.5	V
I_{DD}	supply current	$V_{DD} = 5\text{ V}$ at code 0000H	–	3.0	4.0	mA
I_{FS}	full scale output current	$V_{DD} = 5\text{ V}$	0.9	1.0	1.1	mA
		$V_{DD} = 3\text{ V}$	–	0.6	–	mA
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level	–	–65	–61	dB
			–	0.05	0.08	%
		at –60 dB signal level	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted	–	–33	–	dB
			–	2.2	–	%
at –60 dB signal level; A-weighted; $R3 = R4 = 11\text{ k}\Omega$; (see Fig.1); $I_{FS} = 2\text{ mA}$	–	1.7	–	%		
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB
		A-weighted; $I_{FS} = 2\text{ mA}$; $R3 = R4 = 11\text{ k}\Omega$; see Fig.1	–	95	–	dB
t_{CS}	current settling time to $\pm 1\text{ LSB}$		–	0.2	–	μs
BR	input bit rate at data input		–	–	18.4	Mbits/s
f_{clk}	clock frequency at clock input BCK		–	–	18.4	MHz
TC_{FS}	full scale temperature coefficient at analog outputs (I_{OL} ; I_{OR})		–	$\pm 400 \times 10^{-6}$	–	
T_{amb}	operating ambient temperature		–40	–	+85	$^{\circ}\text{C}$
P_{tot}	total power dissipation	$V_{DD} = 5\text{ V}$ at code 0000H	–	15	20	mW
		$V_{DD} = 3\text{ V}$ at code 0000H	–	6.0	–	mW

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BLOCK DIAGRAM

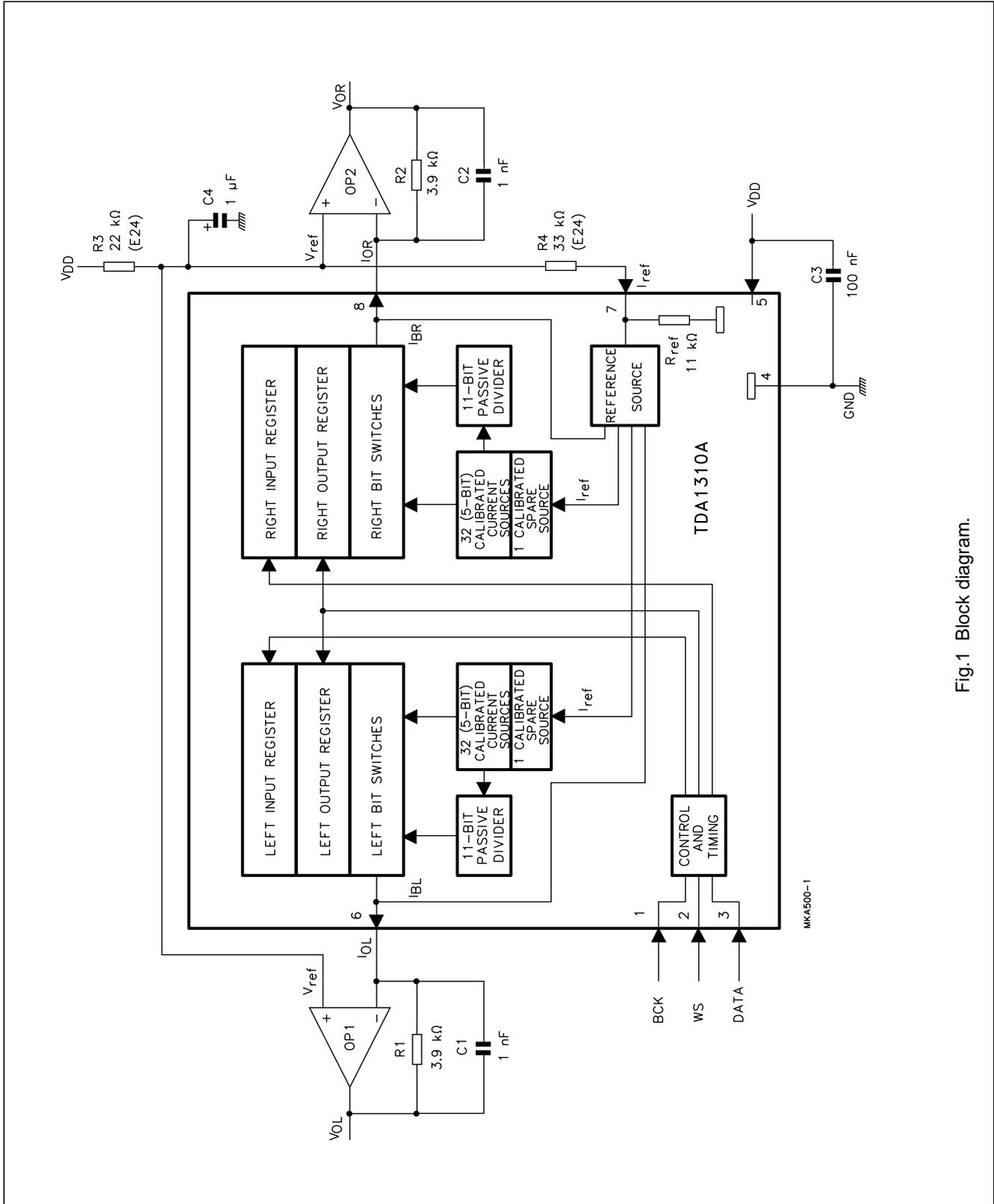


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
BCK	1	bit clock input
WS	2	word select input
DATA	3	data input
GND	4	ground
V _{DD}	5	supply voltage
I _{OL}	6	left channel output
I _{ref}	7	reference input
I _{OR}	8	right channel output

FUNCTIONAL DESCRIPTION

The basic operation of the continuous calibration DAC is illustrated in Fig.3. The figure shows the calibration and operation cycle. During calibration of the MOS current source (Fig.3a) transistor M1 is connected as a diode by applying a reference current. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} of M1 is then determined by the transistor characteristics. After calibration of the drain current to the reference value I_{ref}, the switch S1 is opened and S2 is switched to the other position (Fig.3b). The gate-to-source voltage V_{gs} of M1 is not changed because the charge on C_{gs} is preserved. Therefore, the drain current of M1 will still be equal to I_{ref} and this exact duplicate of I_{ref} is now available at the OUT terminal.

The 32 current sources and the spare current source of the TDA1310A are continuously calibrated (see Fig.1). The spare current source is included to allow continuous converter operation. The output of one calibrated source is connected to an 11-bit binary current divider consisting of 2048 transistors. A symmetrical offset decoding principle is incorporated and arranges the bit switching in such a way that the zero-crossing is performed only by switching the LSB currents.

The TDA1310A (CC-DAC) accepts serial input data formats of 16-bit word length. Left and right data words are time multiplexed. The most significant bit (bit 1) must always be first. The input data format is shown in Figs 4 and 5.

With a HIGH level on the word select input (WS), data is placed in the left input register, with a LOW level on the WS input, data is placed in the right input register (see Fig.1). The data in the input registers are simultaneously latched in the output registers which control the bit switches.

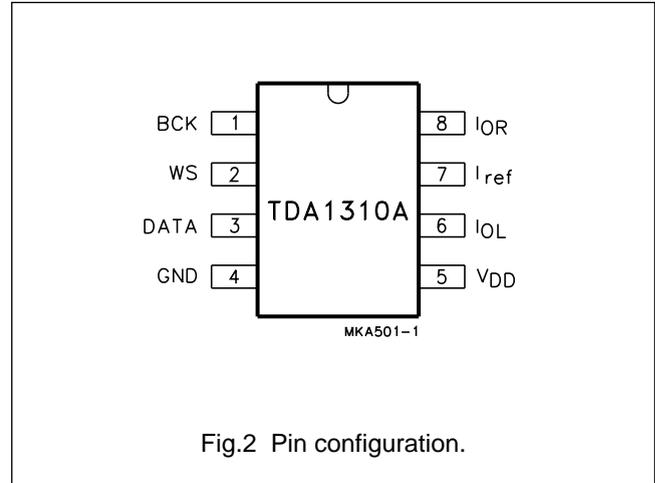


Fig.2 Pin configuration.

An internal bias current I_{bias} is added to the full scale output current I_{FS} in order to achieve the maximum dynamic range at the outputs OP1 and OP2 in Fig.1.

The reference input current I_{ref} controls with gain G_{FS}, the current I_{FS} which is a sink current and with gain G_{bias} the I_{bias} which is a source current⁽¹⁾.

The current I_{ref} is proportional to V_{DD} so the I_{FS} and the I_{bias} will be proportional to V_{DD} as well⁽²⁾ because G_{FS} and G_{bias} are constant.

The reference voltage V_{ref} in Fig.1 is 2/3 V_{DD}. In this way maximum dynamic range is achieved over the entire power supply voltage range.

The tolerance of the reference input current in Fig.1 depends on the tolerance of the resistors R3, R4 and R_{ref}⁽³⁾.

(1) I_{FS} = G_{FS} x I_{ref} and I_{bias} = G_{bias} x I_{ref}

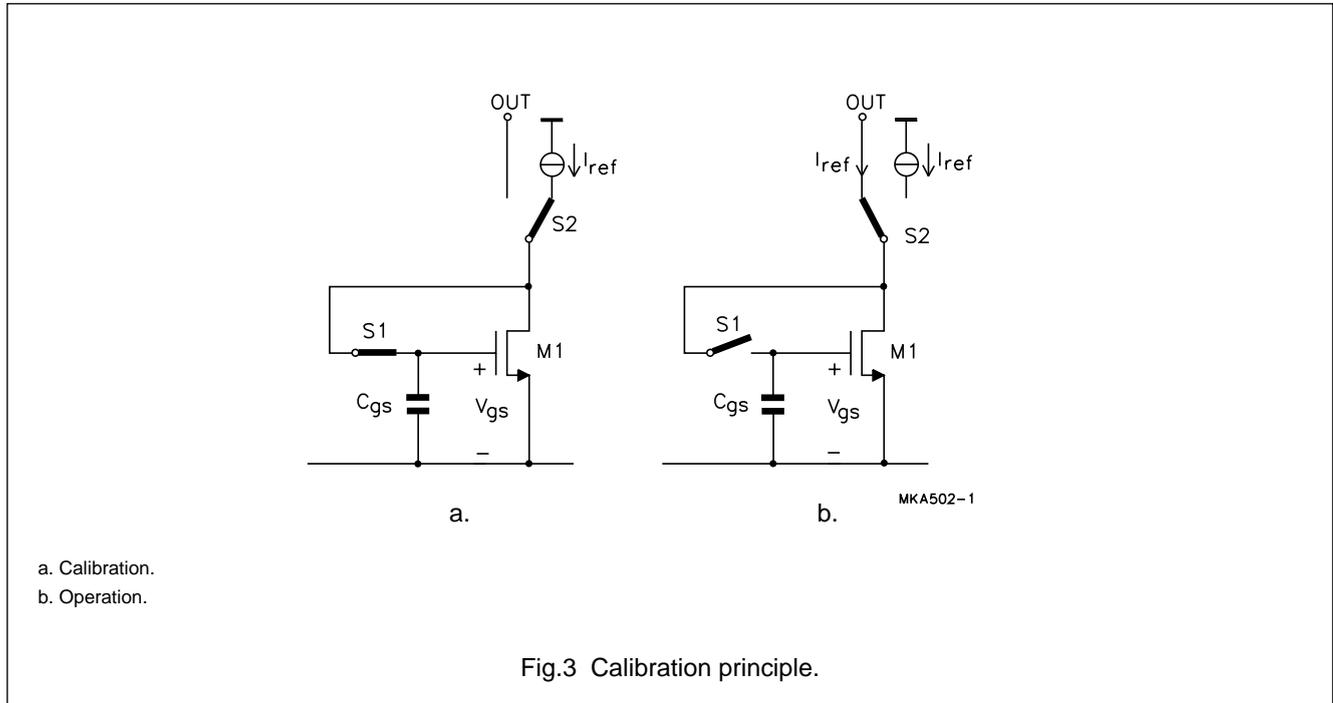
(2) $\frac{V_{DD1}}{V_{DD2}} = \frac{I_{FS1}}{I_{FS2}} = \frac{I_{bias1}}{I_{bias2}}$

(3) $\Delta I_{ref} = I_{ref} - \frac{V_{DD}}{R3 + \Delta R3 + R4 + \Delta R4 + R_{ref} + \Delta R_{ref}}$

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Calibration principle



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		-	6	V
T_{stg}	storage temperature		-55	+150	°C
T_{xtal}	maximum crystal temperature		-	+150	°C
T_{amb}	operating ambient temperature		-40	+85	°C
V_{es}	electrostatic handling	note 1	-2000	+2000	V
		note 2	-200	+200	V

Notes

- Human body model; C = 100 pF; R = 1500 Ω ; 3 zaps positive and negative.
- Machine model; C = 200 pF; L = 0.5 μ H; R = 10 Ω ; 3 zaps positive and negative.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	DIL8	100	K/W
	SO8	210	K/W

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CHARACTERISTICS

$V_{DD} = 5\text{ V}$; $T_{amb} = 25\text{ °C}$; measured in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage		3.0	5.0	5.5	V
I_{DD}	supply current	at code 0000H	–	3.0	4.0	mA
SVRR	supply voltage ripple rejection	note 1	–	30	–	dB
Digital inputs; pins WS, BCK and DATA						
$ I_{IL} $	input leakage current LOW	$V_I = 0\text{ V}$	–	–	10	μA
$ I_{IH} $	input leakage current HIGH	$V_I = 5\text{ V}$	–	–	10	μA
f_{clk}	clock frequency		–	–	18.4	MHz
BR	bit rate data input		–	–	18.4	Mbits/s
f_{WS}	word select input frequency		–	–	384	kHz
Timing (see Fig.4)						
t_r	rise time		–	–	12	ns
t_f	fall time		–	–	12	ns
t_{CY}	bit clock cycle time		54	–	–	ns
t_{BCKH}	bit clock pulse width HIGH		15	–	–	ns
t_{BCKL}	bit clock pulse width LOW		15	–	–	ns
$t_{SU;DAT}$	data set-up time		12	–	–	ns
$t_{HD;DAT}$	data hold time to bit clock		2	–	–	ns
$t_{HD;WS}$	word select hold time		2	–	–	ns
$t_{SU;WS}$	word select set-up time		12	–	–	ns
Analog input; pin I_{ref}						
R_{ref}	reference resistor	see Fig.1	7.4	11.0	14.6	$\text{k}\Omega$
Analog outputs; pins I_{OL} and I_{OR}						
RES	resolution		–	–	16	bits
V_{DCC}	DC output voltage compliance		2.0	–	$V_{DD} - 1$	V
I_{FS}	full-scale current		0.9	1.0	1.1	mA
TC_{FS}	full-scale temperature coefficient		–	$\pm 400 \times 10^{-6}$	–	
I_{bias}	bias current		643	714	785	μA
G_{FS}	reference input current to full scale output current gain		11.9	13.2	14.5	
G_{bias}	reference input current to bias current gain		8.48	9.42	10.36	

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	at 0 dB signal level; note 2	–	–65	–61	dB
			–	0.05	0.08	%
		at –60 dB signal level; note 2	–	–30	–24	dB
			–	3	6	%
		at –60 dB signal level; A-weighted; note 2	–	–33	–	dB
			–	2.2	–	%
at –60 dB signal level; A-weighted; note 2; R3 = R4 = 11 k Ω ; see Fig.1; I _{FS} = 2 mA	–	1.7	–	%		
	–	–65	–61	dB		
t _{cs}	current settling time to ± 1 LSB	at 0 dB signal level; f = 20 Hz to 20 kHz	–	0.05	0.08	%
			–	0.2	–	μ s
α_{cs}	channel separation		86	95	–	dB
\Delta I _O	unbalance between outputs I _{OL} and I _{OR}	note 1	–	0.2	0.3	dB
t _d	time delay between outputs I _{OL} and I _{OR}		–	± 0.2	–	μ s
S/N	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	86	92	–	dB
		A-weighted; I _{FS} = 2 mA; R3 = R4 = 11 k Ω ; see Fig.1	–	95	–	dB

Notes

1. V_{ripple} = 1% of supply voltage; f_{ripple} = 100 Hz.
2. Measured with 1 kHz sine wave generated at sampling rate of 192 kHz.

Stereo Continuous Calibration DAC
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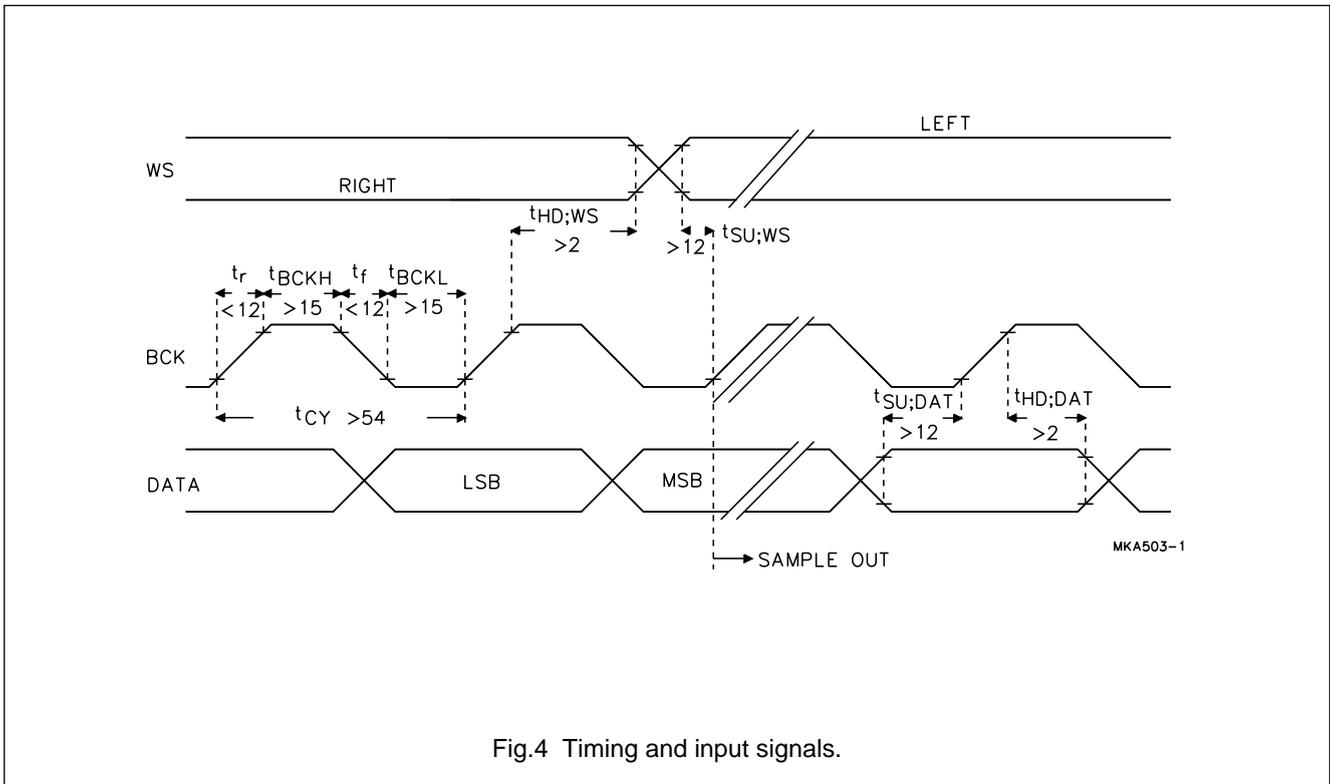


Fig.4 Timing and input signals.

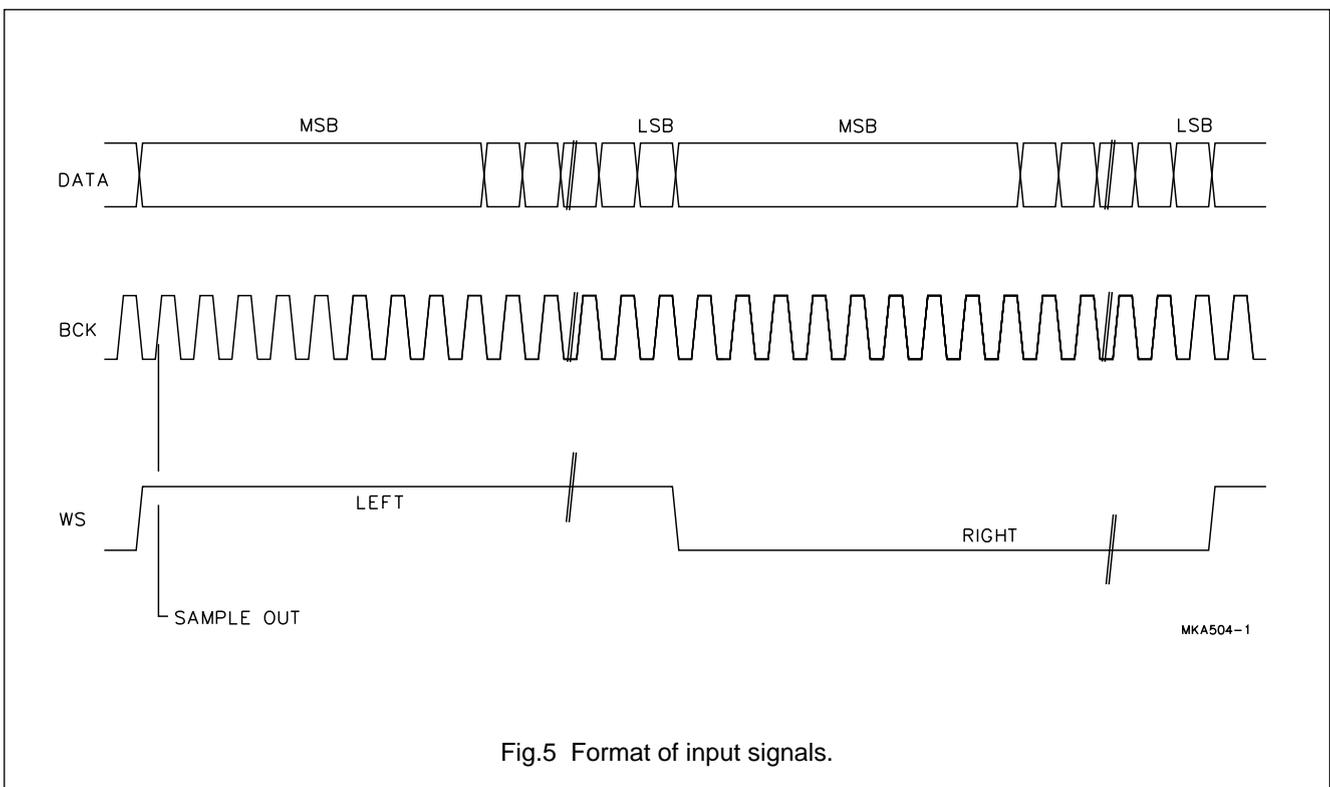


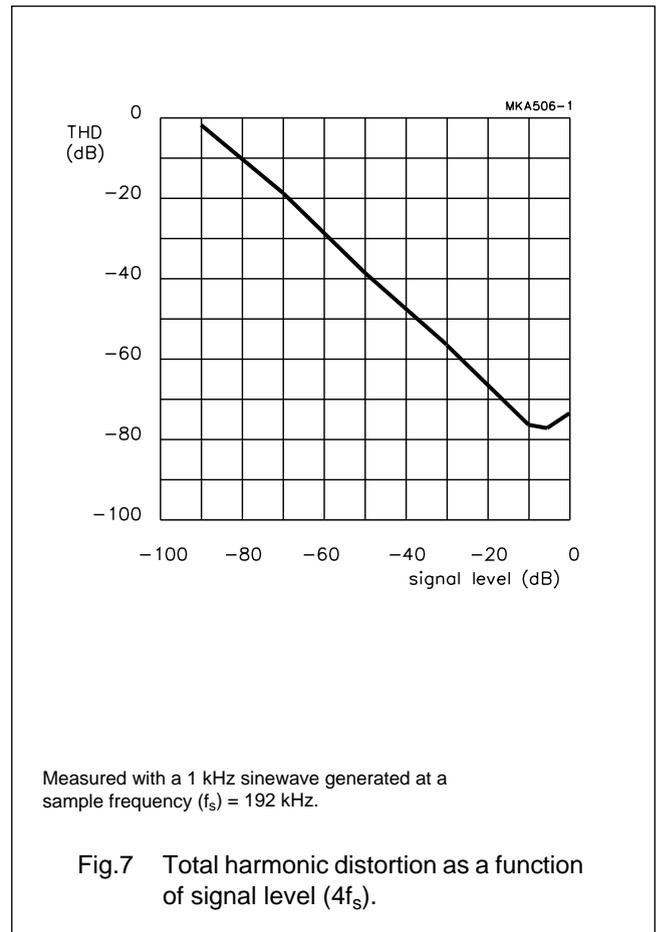
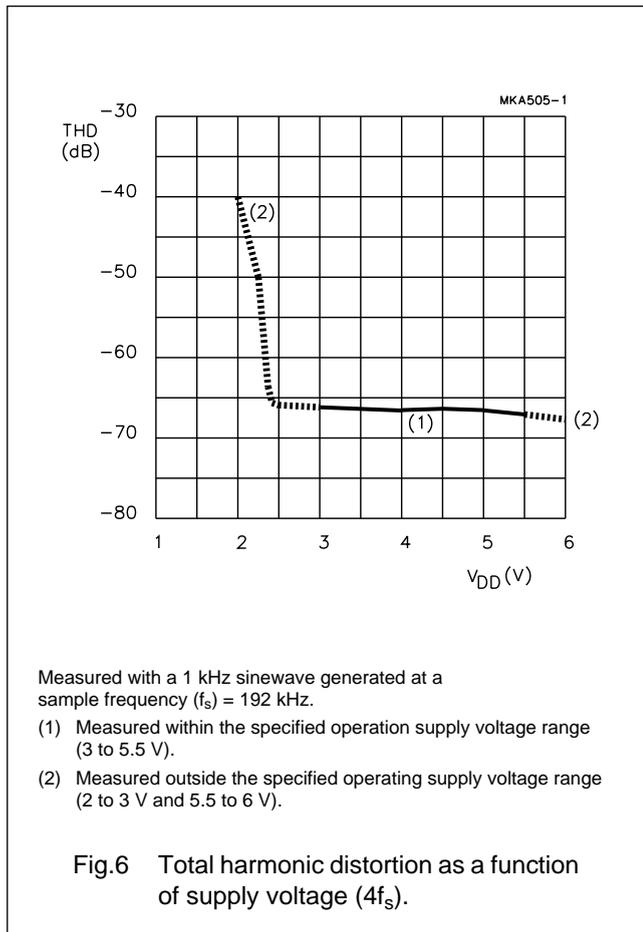
Fig.5 Format of input signals.

Stereo Continuous Calibration DAC (CC-DAC)

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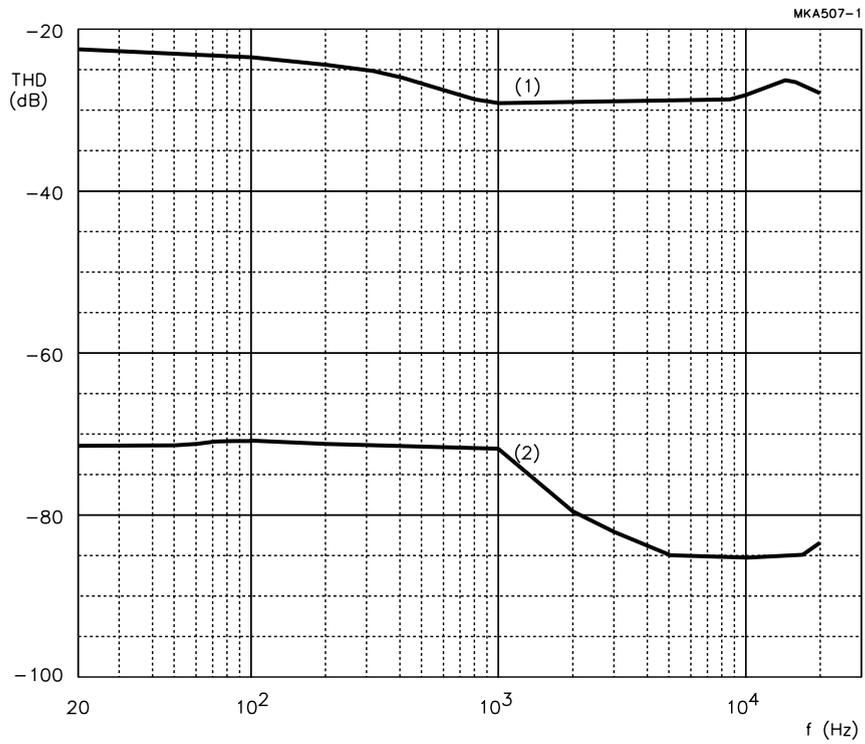
APPLICATION INFORMATION

Remark: the graphs are constructed from average measurement values of a small amount of engineering samples, therefore **no** guarantee for typical values is implied.



Stereo Continuous Calibration DAC (CC-DAC)

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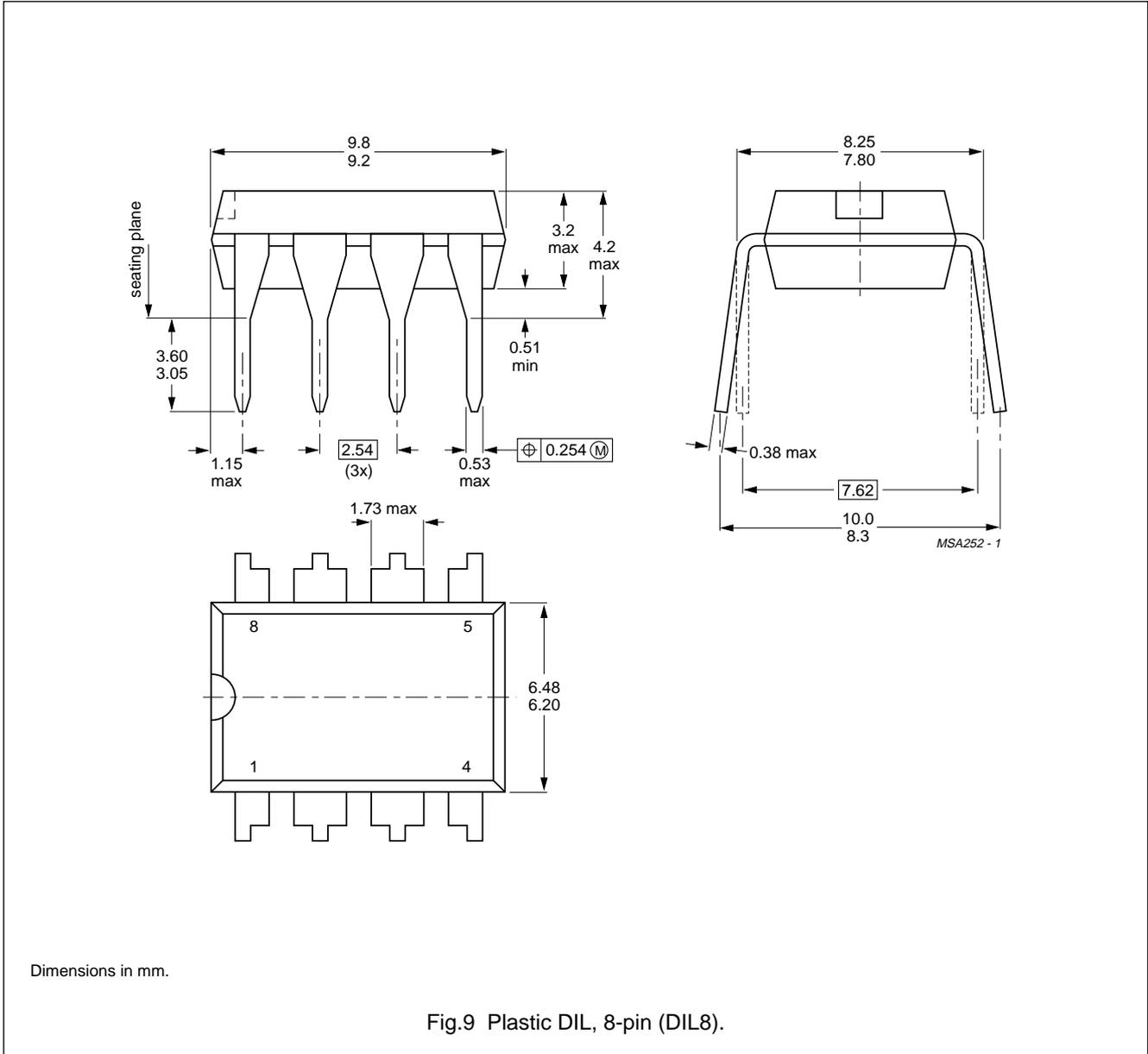
- (1) Measured including all distortion plus noise at a signal level of -60 dB.
- (2) Measured including all distortion plus noise at a signal level of 0 dB.

Fig.8 Total harmonic distortion as a function of frequency ($4f_s$).

Stereo Continuous Calibration DAC (CC-DAC)

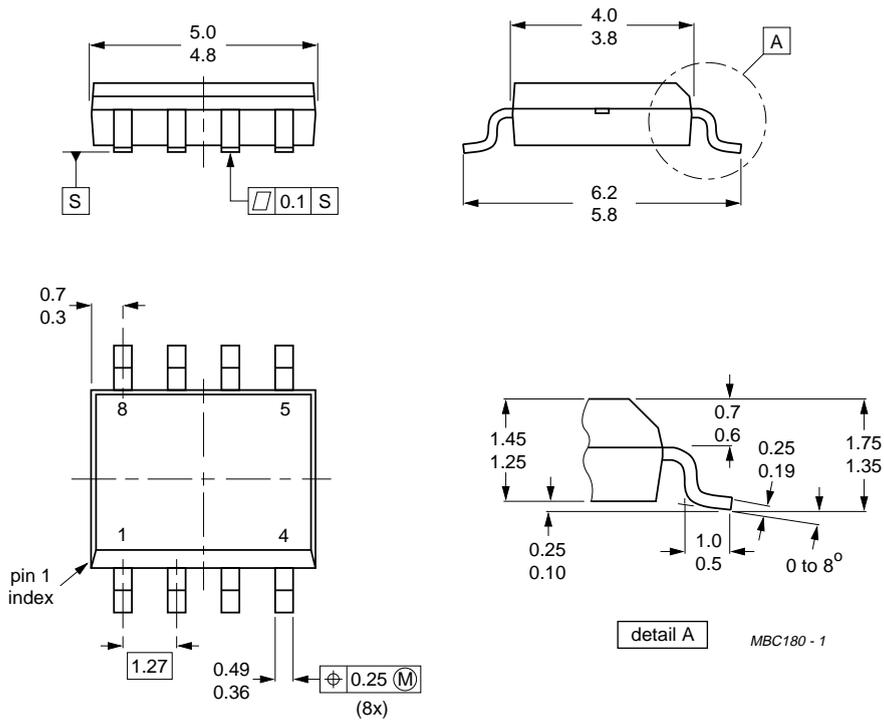
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PACKAGE OUTLINES



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Dimensions in mm.

Fig.10 Plastic SO, 8-pin (SO8).

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SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

Stereo Continuous Calibration DAC (CC-DAC)

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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