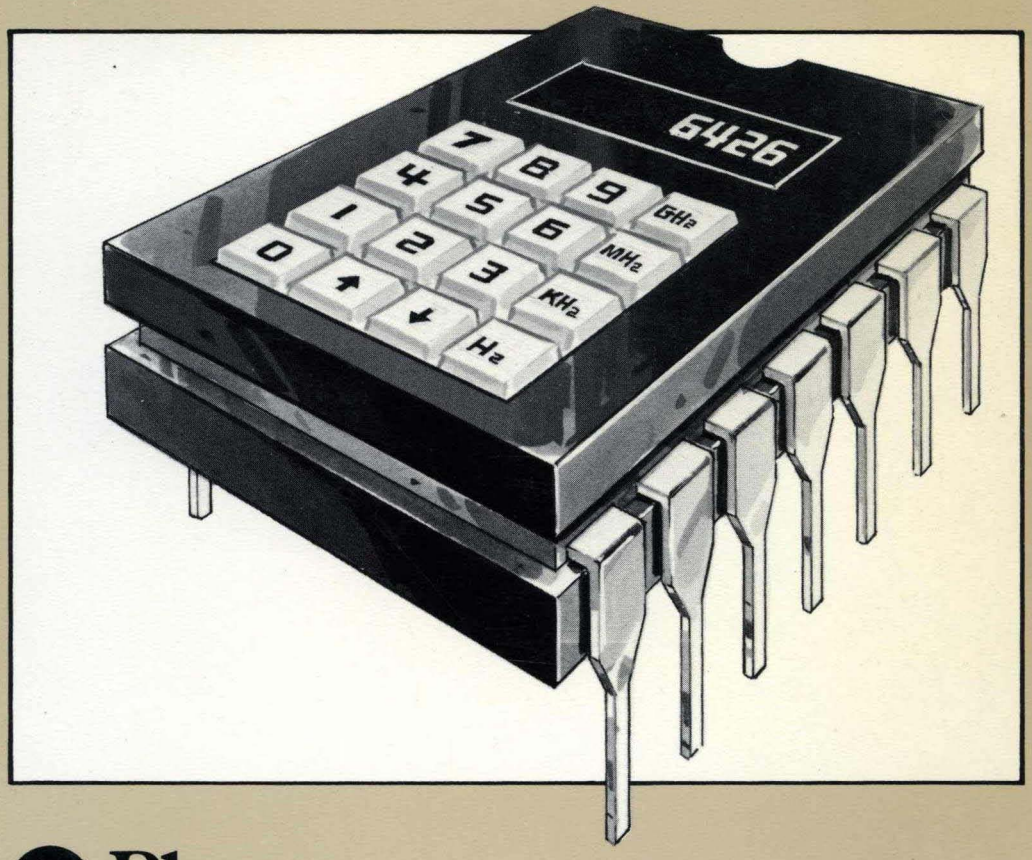
# Frequency Synthesis IC Handbook




Plessey Semiconductors

Frequency Synthesis IC Handbook

$3.00

PLESSEY Semiconductors

# FREQUENCY SYNTHESIS IC HANDBOOK

SEPTEMBER 1980

**Plessey Semiconductors**
1641 Kaiser Avenue,
Irvine, CA. 92714

**$3.00**

PSI 1760

# Contents

# product index

**DEVICE TYPE**

## SP8000 SERIES HIGH SPEED DIVIDERS

### Prescalers

# 1. Product Information.

# Building Block IC's

Plessey integrated circuits are on the leading edge of technology without pushing the ragged edge of capability.

We developed the first 2 GHz counter. And a family of prescalers and controllers for your TV, radio and instrumentation frequency synthesizers.

We have a monolithic 1 GHz amplifier. And a complete array of complex integrated function blocks for radar signal processing and radio communications.

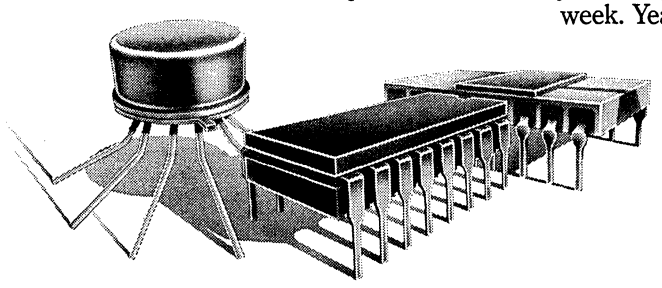
We can supply data conversion devices with propagation delays of just 2½ nanoseconds.

And a range of MNOS logic that stores data for a year when you remove the power, yet uses only standard supplies and is fully TTL/CMOS-compatible.

To develop this edge, we developed our own processes, both bipolar and MOS. The processes were designed for quality and repeatability, then applied to our high volume lines. Most of our IC's are available screened to MIL-STD-883B, and our quality levels exceed the most stringent military, TV and automotive requirements.

Millions of Plessey complex function building block IC's are being used in TV sets and car radios; CATV, navigation and radar systems; frequency synthesizers and telecommunications equipment.

Our global scope of operations, our high volume manufacturing facilities, our proprietary processes ensure that we will continue to deliver state-of-the-art technology and reliability in IC devices at the appropriate prices and in the required volumes. Day after day. Week after week. Year after year.



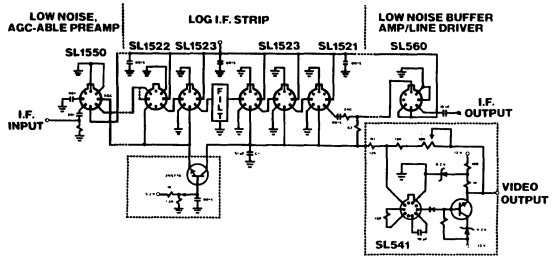
# Plessey Semiconductors

1641 Kaiser Avenue, Irvine, CA 92714. (714) 540-9979

# Radar Signal Processing

Since the performance of a radar receiver is critically dependent on the performance of its I.F. strip, we offer a range of "building block" IC's that can be used in systems with different performance requirements and configurations.

The logarithmic I.F. strip shown is an example of a low cost, high performance strip fabricated with Plessey IC's. It uses only five devices and a single interstage filter to achieve a logging range of 90 dB, ±1 dB accuracy, −90 dBm tangential sensitivity and a video rise time of 20 ns or less.




Three other Plessey IC's complete the system simply and economically. The AGC-able SL1550 on the front end improves noise figure, dynamic range and sensitivity. The SL541 lets you vary video output levels, with on-chip compensation making it easy to use. And the SL560 is a "gain block" that replaces your hybrid and discrete amplifiers, usually with no external components.

Another advanced system function block is the Plessey SL531 True Log Amplifier. A 6-stage log strip requires a minimum of external components (one capacitor, one resistor per stage), yet has a band-width of 500 MHz, a dynamic range of 70 dB and has a phase shift of only ±3° over its entire range. As with most of our other devices, it operates over the full MIL-temp range and is available screened to MIL-STD-883.

The chart summarizes our Radar Signal Processing IC's. Whether you're working with radar and ECM, weapons control or navigation and guidance systems, our IC's are a simpler, less expensive, more flexible alternative to whatever you're using now for any I.F. strip up to 160 MHz.

For more details, please use the postage-paid reply card at the back of this book to order our RADAR AND RADIO COMMUNICATIONS IC HANDBOOK, or contact your nearest Plessey Semiconductors representative.

**PLESSEY IC'S FOR RADAR I.F.'S**

**Wideband Amplifiers for Successive Detection Log Strips**

| | |
|---|---|
| SL521 | 30 to 60 MHz center frequency, 12 dB gain. |
| SL523 | Dual SL521 (series). |
| SL1521 | 60 to 120 MHz center frequency, 12 dB gain. |
| SL1522 | Dual SL1521 (parallel). |
| SL1523 | Dual SL1521 (series). |

**Low Phase Shift Amplifiers**

| | |
|---|---|
| SL531 | True log I.F. amplifier, 10-200 MHz, ±0.5°/10 dB max phase shift. |
| SL532 | 400 MHz bandwidth limiting amplifier, 1° phase shift max. when overdriven 12 dB. |

**Linear Amplifiers**

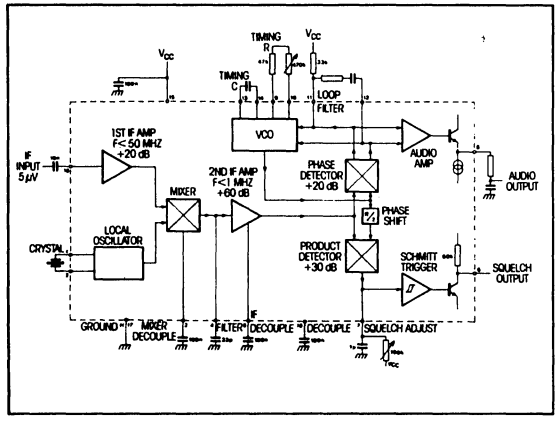
| | |
|---|---|
| SL550 | 125 MHz bandwidth, 40 dB gain, 25 dB swept gain control range, 1.8 dB noise figure, interfaces to microwave mixers. |
| SL1550 | 320 MHz bandwidth version of SL550. |
| SL560 | 300 MHz bandwidth, 10 to 40 dB gain, 1.8 dB noise figure drives 50 ohm loads, low power consumption. |

**Video Amplifiers and Detectors**

| | |
|---|---|
| SL510 | Detector (DC to 100 MHz) and video amplifier (DC to 24 MHz) may be used separately, 11 dB incremental gain 28 dB dynamic range. |
| SL511 | Similar to SL510 with DC to 14 MHz video amplifier, 16 dB incremental gain. |
| SL541 | High speed op amp configuration, 175 V/μs slew rate 50 ns settling time, stable 70 dB gain, 50 ns recovery from overload. |

# Radio Communications

Our comprehensive line of radio system function blocks is cutting costs, increasing reliability and reducing the size of systems




in applications that range from commercial communications to military manpack radios.

Using our bipolar Process I, the Plessey SL600 Series (hermetic) and SL1600 Series (plastic DIP) feature a high degree of integration, low power consumption and exceptional system design flexibility for I.F.'s up to 10.7 MHz.

Our SL6000 Series uses our bipolar Process III to extend our building block concept even further. Devices all feature advanced circuit design techniques that permit higher levels of integration, lower power consumption and exceptional performance.

Typical is our SL6600, a monolithic IC that contains a complete IF amplifier, detector, phase locked loop and squelch control. Power consumption is a meager 1.5 mA at 6 V, S/N ratio is 50 dB, dynamic range is 120 dB and THD is just 1.3% for 5 kHz peak deviation. The SL6600 can be used at I.F. frequencies up to 50 MHz, with deviations up to 10 kHz.

If any of the Plessey devices appear interesting, use the postage-paid reply card at the back of this book to order our RADAR AND RADIO COMMUNICATIONS IC HANDBOOK. The Handbook includes full details on our integrated circuits, along with a number of applications circuits and design tips that will help you get the maximum system benefits from Plessey products.

Or if your need is more urgent, contact your nearest Plessey Semiconductors representative.

**PLESSEY RADIO IC'S**

**Amplifiers**

| | | |
|---|---|---|
| SL610 | SL1610 | 140 MHz bandwidth, 20 dB gain, 50 dB AGC range, low 4 dB N.F., low distortion. |
| SL611 | SL1611 | 100 MHz bandwidth, 26 dB gain, sim. to SL610. |
| SL612 | SL1612 | 15 MHz bandwidth, 34 dB gain, 70 dB AGC range, 20 mW power consumption. |
| SL613 | | 145 MHz bandwidth, 12 dB gain, limiting amp/detector. |

**Mixers**

| | | |
|---|---|---|
| SL640 | SL1640 | Double balanced modulator eliminates diode rings up to 75 MHz, standby power 75 mW typical. |

**Detectors and AGC Generators**

| | | |
|---|---|---|
| SL620 | SL1620 | AGC with VOGAD (Voice Operated Gain Adjusting Device). |
| SL621 | SL1621 | AGC from detected audio. |
| SL623 | SL1623 | AM SSB detector and AGC from carrier. |
| | SL1625 | AM detector and AGC from carrier. |
| SL624 | | AM/FM/SSB/CW detector with audio amplifier. |

**Audio Amplifiers**

| | | |
|---|---|---|
| SL622 | | Microphone amp. with VOGAD and sidetone amp. |
| SL630 | SL1630 | 250 mW microphone/headphone amplifier. |

**I.F. Amplifiers/Detectors**

| | |
|---|---|
| SL6600 | FM double conversions with PLL detector. |
| SL6640 | FM single conversion, audio stage (10.7 MHz). |
| SL6650 | FM single conversion (10.7 MHz). |
| SL6690 | FM single conversion, low power for pagers (455 kHz). |
| SL6700 | AM double conversion. |

**Audio Amplifiers**

| | | |
|---|---|---|
| SL6270 | | Microphone amplifier with AGC. |
| SL6290 | SL6270 | with speech clipper, buffer and relay driver. |
| SL6310 | | Switchable audio amplifier (400 mW/9V/8 ohms). |
| SL6440 | | High-level mixer. |

# R. F. Hybrids

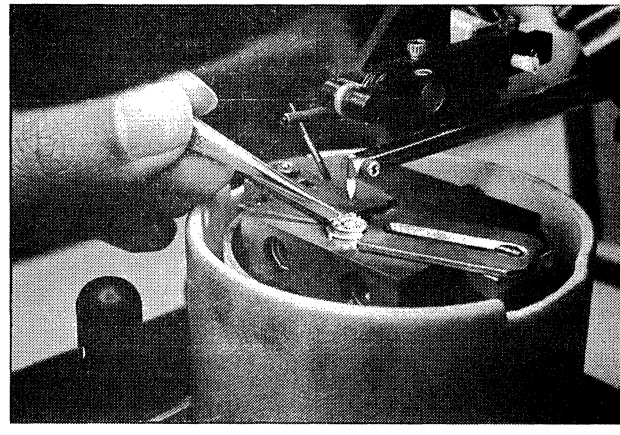
To enhance your systems even further, we have established an R.F. hybrid manufacturing facility in our Irvine, California, U.S.A. headquarters.

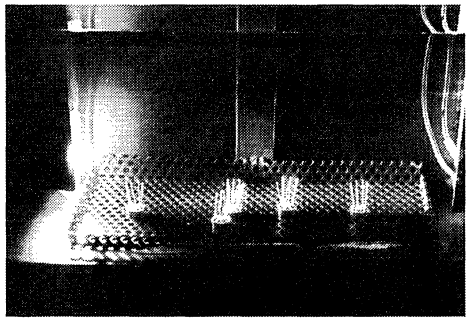
For small production quantities or extremely complex functions, our hybrid capabilities can save you time and money while improving your system performance, reducing system size and increasing system reliability. We can help with your I.F. strips, instrumentation front ends, synthesizer subsystems, high speed A-to-D and D-to-A converters and other complex high-frequency functions.

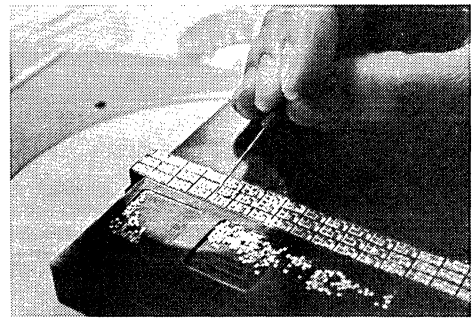
They can be fabricated to MIL-STD-883 using thick and thin film techniques, using our own integrated circuits in combination with discrete transistors, diodes and other components.

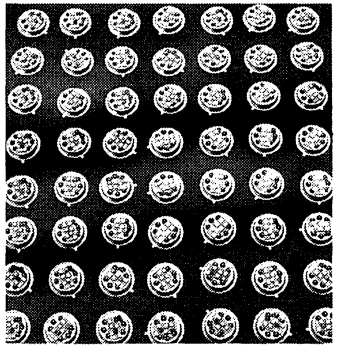
Our IC functions represent the state-of-the-art in high frequency integration, with $f_t$'s as high as 5 GHz. The chips are backed by an in-depth in-house systems knowledge that encompasses radar, radio communications, telecommunications analog and digital conversion, frequency synthesis and a broad range of applications experience.

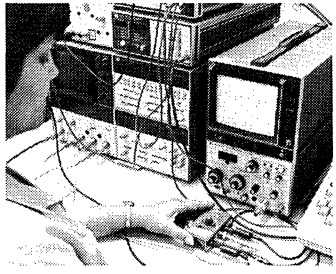
We can work to your prints, or we can design a full system based on your "black box" specifications. For more information, please contact: Plessey Semiconductors, 1641 Kaiser Avenue, Irvine CA 92714, (714) 540-9979.

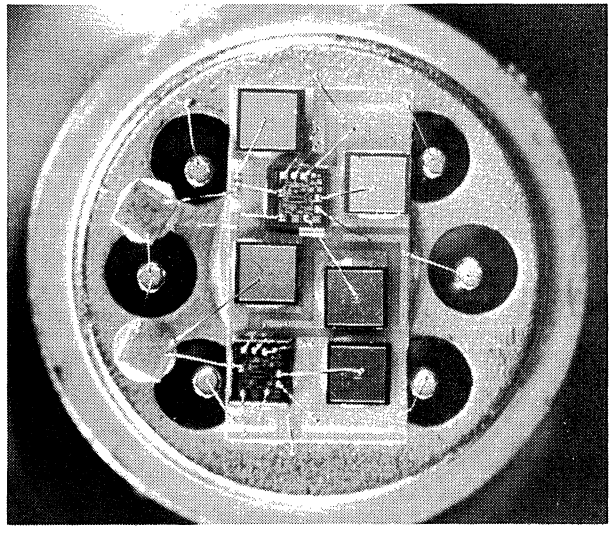












# Frequency Synthesis

Plessey's IC's offer a quick and easy way to lower synthesizer costs while increasing loop response and channel spacing all the way from dc through the HF, VHF, UHF, TACAN and satellite communications bands.

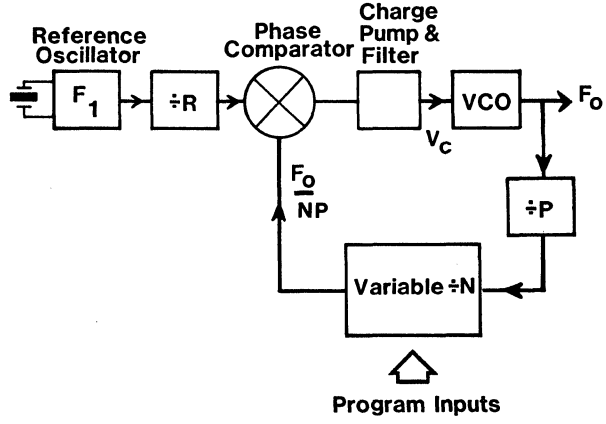
Our single-modulus prescalers operate at frequencies all the way up to 1.8 GHz. They feature self-biasing clock inputs, TTL/CMOS-compatibility and all guaranteed to operate to at least the frequencies shown, most of them over the temperature range from −55°C to +125°C.

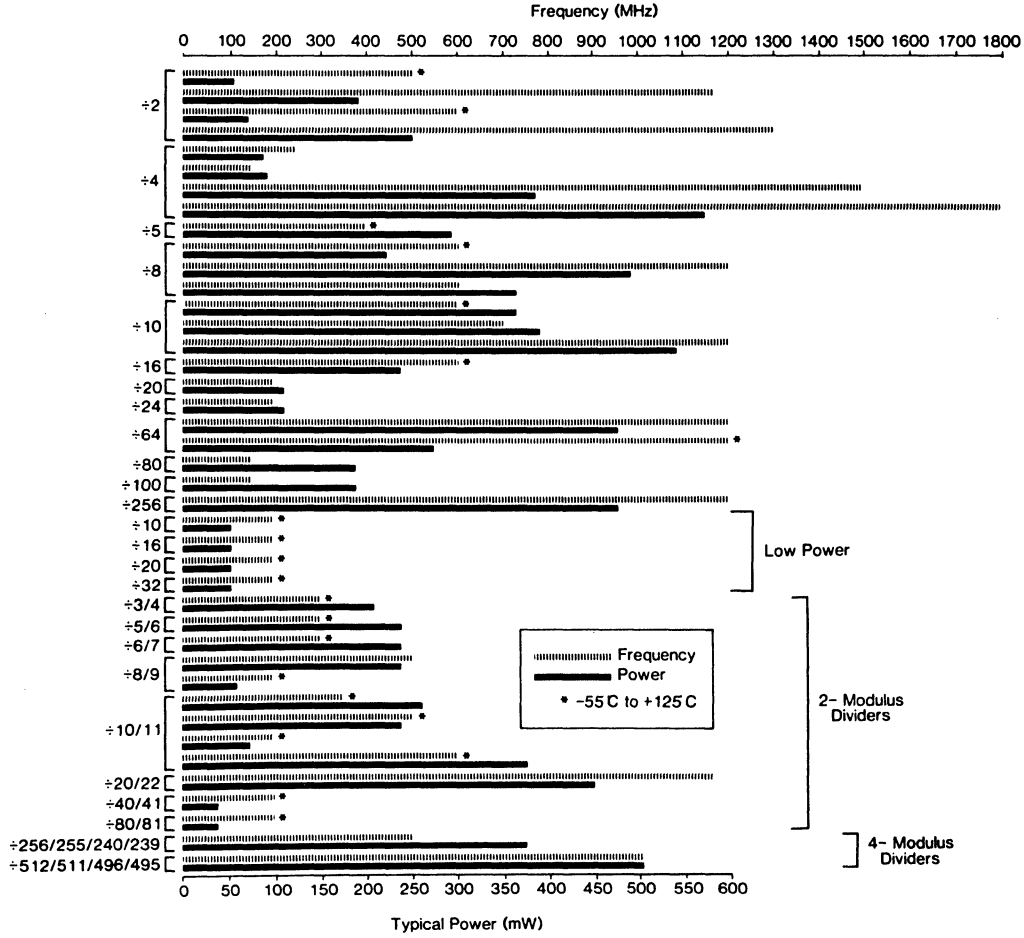
Our 2-modulus and 4-modulus dividers expand your system flexibility and allow even tighter channel spacing. All of them provide low power consumption, low propagation delay and ECL-compatibility.

To simplify your systems even further, we also offer highly integrated control chips. Our NJ8811, for example, includes a crystal oscillator maintaining circuit, a programmable reference divider, a programmable divider to control the four-modulus prescaler and a high performance phase/frequency comparator so that you can phase lock your synthesizer to a crystal with none of the usual headaches and hassles.

We've put together a FREQUENCY SYNTHESIZER IC HANDBOOK that details all of the Plessey IC's and includes a number of applications circuits, practical examples of how Plessey integrated circuits can simplify your designs and improve system performance.

For your copy of the Handbook, please use the postage-paid reply card at the back of this book, or contact your nearest Plessey Semiconductors representative.




Frequency (MHz)
0 100 200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400 1500 1600 1700 1800
÷2
÷4
÷5
÷8
÷10
÷16
÷20
÷24
÷64
÷80
÷100
÷256
÷10
÷16
÷20
÷32
÷3/4
÷5/6
÷6/7
÷8/9
÷10/11
÷20/22
÷40/41
÷80/81
÷256/255/240/239
÷512/511/496/495
Low Power
2- Modulus Dividers
4- Modulus Dividers
Frequency
Power
* -55 C to +125 C
0 50 100 150 200 250 300 350 400 450 500 550 600
Typical Power (mW)

# Telecommunications

Plessey functional building block IC's are exceptionally versatile. Designed from a systems standpoint, they reduce complexity and lower costs while increasing the performance of telecommunications systems.

Our SL600 Modulator/Phase Locked Loops are used in waveform generators and in AM, PAM, FM, FSK, PSK, PWM, tone burst and Delta modulators.

Our SL1000 Series amplifiers meet the most stringent demands of telephone transmission equipment.

Our transistor arrays with up to five electrically and thermally matched transistors on a chip are ideal for discrete and hybrid amplifiers and mixers. In addition to standard second-source devices that plug directly into your designs, we have a number of devices designed for your low noise and ultra-high frequency applications.

The Plessey TELECOMMUNICATIONS IC HANDBOOK contains complete information on all of these devices, as well as application notes, to help you get the most out of them. To get your copy, please use the postage-paid reply card at the back of this book or call your nearest Plessey Semiconductors representative.

**Telecommunications Devices**

| | |
|---|---|
| MJ1440 | HDB3 encoder/decoder |
| MJ1444 | PCM synchronizing word generator |
| MJ1445 | PCM synchronizing word receiver |
| MJ1471 | HDB3/AMI encoder/decoder |

**Data Communications MOS**

| | |
|---|---|
| MP3812 | 32 x 8-bit FIFO memory, serial or parallel, up to 0.25 MHz data rates, easily stacked. |
| MJ2841 | 64 x 4-bit FIFO memory, 5 MHz clock rate. |

**Modulator/Phase Locked Loops**

| | |
|---|---|
| SL650 | Modulator/PLL for AM, PAM, SCAM, FM, FSK, PSK, tone-burst and Delta modulation; VFO variable 100:1. |
| SL651 | Similar to SL650 without auxiliary amplifier. |
| SL652 | Similar to SL650, low cost. |

**Telephone Circuits**

| | |
|---|---|
| SL1001 | Modulator/demodulator, 50 dB carrier and signal suppression, −112 dBm noise level. |
| SL1021 | 3 MHz channel amplifier, stable remote gain control. |
| SL1025 | FDM balanced modulator, 50 dB carrier and signal suppression, 5 dB conversion gain. |
| SL1030 | 200 MHz wideband amplifier, programmable gain, low noise. |

**Transistor Arrays**

| PLESSEY PART NO. | 2ND-SOURCE PART NO. | PLESSEY PART NO. | 2ND-SOURCE PART NO. |
|---|---|---|---|
| SL3081 | CA3081 | SL3051 | CA3951 |
| SL3082 | CA3082 | SL355 | NONE |
| SL3083 | CA3083 | TBA673 | TBA673 |
| SL3183 | CA3183 | SL1495 | CA1495L |
| SL3146 | CA3146 | SL1496 | MC1496G |
| SL3093 | CA3093 | SL1496 | MC1496L |
| SL3018 | CA3018 | SL1595 | MC1595L |
| SL3018A | CA3018A | SL1596 | MC1596G |
| SL3118A | CA3118A | SL1596 | MC1596L |
| SL3118 | CA3118 | SL3054 | CA3054 |
| SL3050 | CA3050 | SL3086 | CA3086 |

| | |
|---|---|
| SL360 | High frequency matched pair, $f_t$=2.5 GHz. |
| SL363 | Low noise matched pair, $f_t$=2.2 GHz. |
| SL2363/4 | 5GHz dual long-tailed pair. |
| SL3145 | Five transistor array, $f_t$=2.5 GHz. |

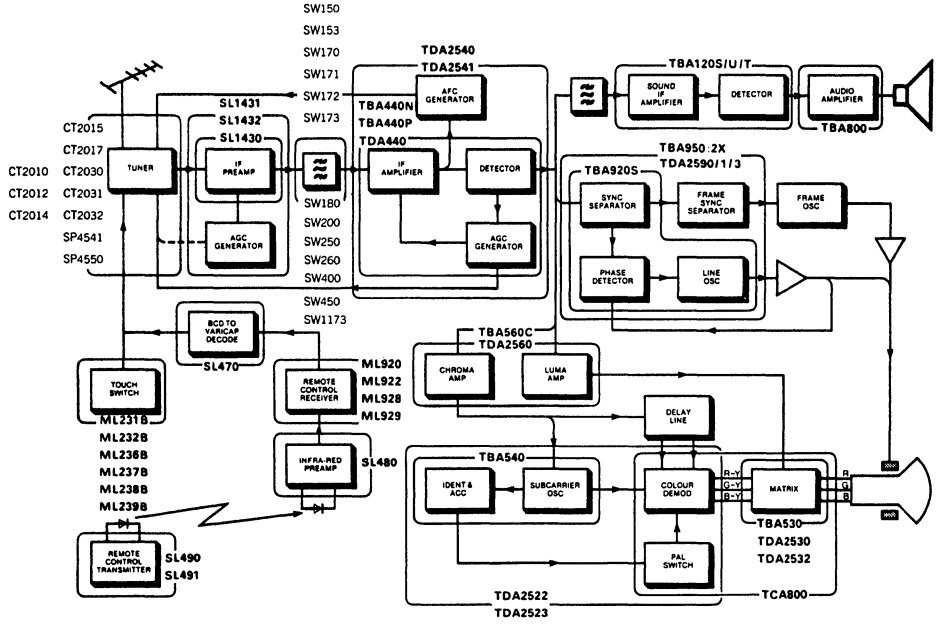
# Television IC's

Plessey integrated circuits are in millions of homes, in television sets around the world.

Economical and reliable, our devices cover the range from remote controls to touch tuners to frequency synthesizers, as well as a range of second-source devices for the IF color processing and line oscillators.

For the 1980's, we have introduced the Plessey KEY System, designed for maximum flexibility, simplicity and ease of manufacture. The KEY System frequency synthesizer offers accurate, high stability frequency selection, channel and program identification, and the very finest digital fine tuning. It can be configured to receive up to four completely different standards (PAL, SECAM, SECAMF, and NTSC) in a single TV set. It has 100 channel capability per standard, and includes a 32-program non-volatile memory that contains channel, fine tuning and standards information. And it can be interfaced to a Plessey or other microprocessor for games, Teletext or similar applications.

Complete data on all our television devices has been assembled in our TELEVISION IC HANDBOOK, along with application notes to make them even easier to use. Please use the postage-paid reply card at the back of this book to order your copy, or simply contact your nearest Plessey Semiconductors representative.




**ALL TBA, TCA, TDA DEVICES ARE SECOND-SOURCED.**

# ECL III Logic and Data Conversion

As radar and communications systems become faster and more complex, the need arises for digital processing. We have developed a family of functions with speeds unequalled anywhere.

Part of our family is a range of ECL III logic that is a direct plug-in replacement for MECL logic, including low impedance as well as high impedance devices. We extended the range by adding functions with lower delays and much higher operating speeds. Our SP16F60, for example, is the world's fastest dual 4-input OR/NOR gate, with a switching speed of just 500 picoseconds. Devices can also be selected for certain specifications (such as threshold voltage or slew rate on our SP1650/1, toggle rates or delays on our SP1670) to handle your most demanding applications. We've also developed a family of high speed comparators and circuits for ultra-high speed A-to-D converters. Our latching SP9750 high speed comparator features a maximum settling time of 2 ns, a propagation delay of 3.5 ns and is capable of operating at rates up to 100 million samples per second.

Currently, our devices are being used in radar and video processing, nucleonics systems, transient recorders and secure speech transmission systems. We have compiled a number of application notes and details on the devices in our ECL III LOGIC AND DATA CONVERSION IC HANDBOOK. To get your copy, please use the postage-paid reply card at the back of this book, or contact your nearest Plessey Semiconductors representative.

**HIGH SPEED ECL III LOGIC**

| | |
|---|---|
| SP1648 | Voltage controlled oscillator |
| SP1650 | Dual A/D comparator, Hi-Z |
| SP1651 | Dual A/D comparator, Lo-Z |
| SP1658 | Voltage controlled multivibrator |
| SP1660 | Dual 4-I/P OR/NOR gate, Hi-Z |
| SP1661 | Dual 4-I/P OR/NOR gate, Lo-Z |
| SP1662 | Quad 2-I/P NOR gate, Hi-Z |
| SP1663 | Quad 2-I/P NOR gate, Lo-Z |
| SP1664 | Quad 2-I/P OR gate, Hi-Z |
| SP1665 | Quad 2-I/P OR gate, Lo-Z |
| SP1666 | Dual clocked R-S Flip-Flop, Hi-Z |
| SP1667 | Dual clocked R-S Flip-Flop, Lo-Z |
| SP1668 | Dual clock latch, Hi-Z |
| SP1669 | Dual clock latch, Lo-Z |
| SP1670 | Master-slave D Flip-Flop, Hi-Z |
| SP1671 | Master-slave D Flip-Flop, Hi-Z |
| SP1672 | Triple 2-I/P exclusive-OR gate, Hi-Z |
| SP1673 | Triple 2-I/P exclusive-OR gate, Lo-Z |
| SP1674 | Triple 2-I/P exclusive-NOR gate, Hi-Z |
| SP1675 | Triple 2-I/P exclusive-NOR gate, Lo-Z |
| SP1692 | Quad line receiver |
| SP16F60 | Dual 4-I/P OR/NOR gate |

**HIGH SPEED DATA CONVERSION PRODUCTS**

| | |
|---|---|
| SP9680 | High speed latched comparator. |
| SP9685 | Ultra-fast comparator; 0.5 ns typical set-up time; typical 2.2 ns propagation delay; excellent CMR. |
| SP9687 | Dual SP 9685. |
| SP9750 | High speed latched comparator with precision current source, wired-OR decoding; 2 ns min. set-up time; 2.5 ns propagation delay. |
| SP9752 | 2-bit ADC expandable to 6-bit ADC; very fast 125 MHz clock. |
| SP9754 | 4-bit ADC expandable to 8-bit ADC; very fast 100 MHz clock. |
| SP9768 | 8-bit DAC; extremely fast; available 3rd quarter 1980. |
| SP9778 | 8-bit SAR; works with SP9768 to make a two-chip successive approximation ADC (20 MHz clock); available 4th quarter 1980. |

# MNOS Non-Volatile Logic

As semiconductors become more pervasive in military and commercial applications, the need for non-volatile data retention becomes more and more critical.

Plessey NOVOL MNOS devices answer that need, and will retain their data for at least a year (−40°C to +70°C) in the event of "power down" or a system crash.

Our devices all operate from standard MOS supplies and are fully compatible with your TTL/CMOS designs. The high voltages normally associated with electrically-alterable memories are generated on-chip to make system interface simpler and less expensive.

Plessey NOVOL devices provide a reliable, sensible alternative to CMOS with battery back-up or mechanical, electro-mechanical and magnetic devices. Applications include metering, security code storage, microprocessor back-up, elapsed time indicators, counters, latching relays and a variety of commercial, industrial and military systems.

For more information, contact your nearest Plessey Semiconductors representative, or use the postage-paid reply card at the back of this brochure to order your copy of the Plessey NOVOL literature package.

**PLESSEY NOVOL MNOS**

| | |
|---|---|
| MN9102 | 4-bit Data Latch (+5V, −12V) |
| MN9105 | 4-Decade Up/Down Counter (+5V, −12V) |
| MN9106 | 6-Decade Up Counter (12V only) |
| MN9107 | 100-Hour Timer (12V only) |
| MN9108 | 10,000-Hour Timer (12V only) |
| MN9110 | 6-Decade Up Counter with Carry (12V only) |
| MN9210 | 64 x 4-Bit Memory |
| * | 8 x 4-Bit Memory |
| * | 6-Decade Up/Down Counter, BCD Output |
| * | 6-Decade Up/Down Counter with Preset BCD Output |

* COMING SOON

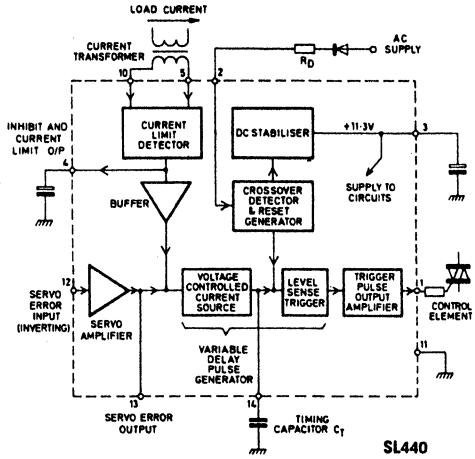
# Power Control

Plessey power control devices are highly integrated not just to solve the problems, but to solve them at a lower cost than any other available method.

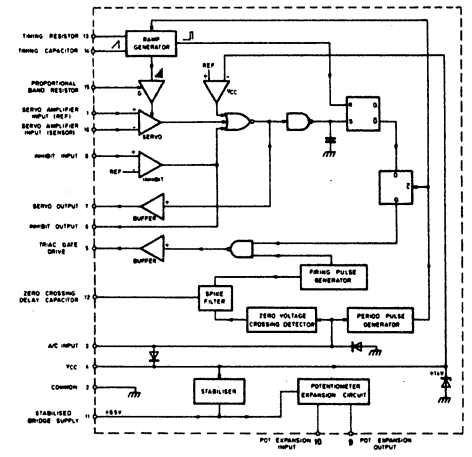
For timing, our devices use a pulse integration technique that eliminates the need for expensive electrolytic capacitors, thus increasing accuracy and repeatability while reducing costs. An integral supply voltage sensing circuit inhibits triac gate drive circuitry if the supply is dangerously low to prevent half-wave firing and firing without achieving complete bulk conduction. A zero-voltage spike filter prevents misfiring on noise inputs. Symmetrical control prevents the introduction of dc components onto the power lines.

Devices have been tailored for specific applications as indicated in the chart. For more information, please use the postage-paid reply card at the back of this book to order our POWER CONTROL IC HANDBOOK, or contact your nearest Plessey Semiconductors representative.

| | |
|---|---|
| **SL440** | **Proportional phase control for motors, lamps and lower power, fast response heating.** |
| **SL441** | **Similar to SL440, with proportional temperature control and thermister malfunction sensing, for hairdryers, soldering irons and food warmers.** |
| **SL442** | **Switch mode power supply control, up to 40 kHz, integral oscillator, variable ratio space/mark pulses, soft-start, dynamic current limiting, OVP.** |
| **SL443** | **Similar to SL441 with manual power control, long timing periods for hot plates, electric blankets and traffic lights.** |
| **SL444** | **Similar to SL441 for 240V permanent magnet motor with thermal trip, current limit detector.** |
| **SL445** | **Proportional or On/Off control, temperature trip/ inhibit circuitry, LED and alarm drive facilities, for ovens, heaters, industrial temperature controllers.** |
| **SL446** | **On/Off servo loop temperature controller, low external component count, for water and panel heaters, refrigerators, irons.** |
| **TBA1085** | **Motor speed control** |




SL440



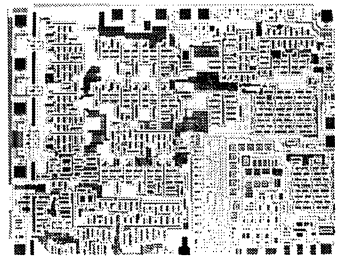

SL445

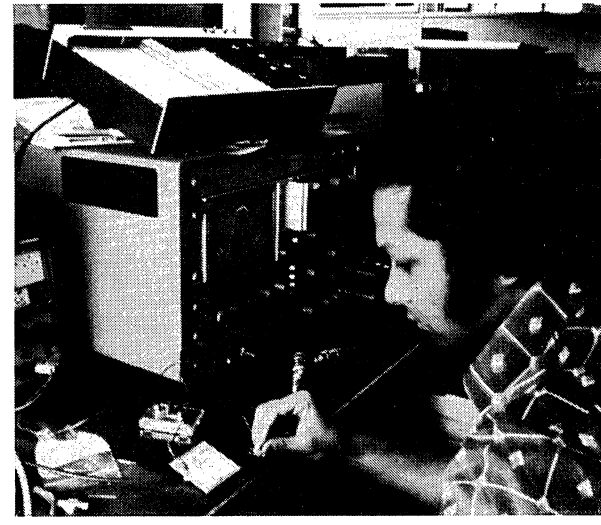
# Processes, Testing and Quality Control

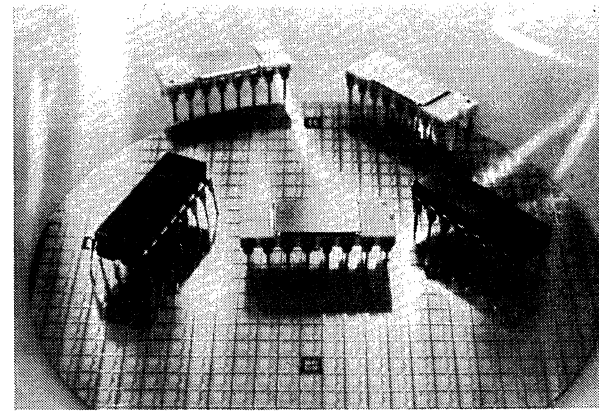
Just as we applied our systems knowledge to the partitioning of functions to make our IC's extremely flexible and cost effective, we also developed an internal system concept to ensure that we could deliver our state-of-the-art solutions year after year.

Our concept of standard processes and rigid design rules ensures that our devices are reproducible this year, next year and five years from now. Our continuing investment in research and development ensures that any new products we introduce will be on the leading edge of technology, yet with the same high performance and reliability that our customers have come to expect as the Plessey standard.

The result is that millions of Plessey devices have been built into TV sets and car radios; CATV, navigation and radar systems; frequency synthesizers and telecommunications equipment.





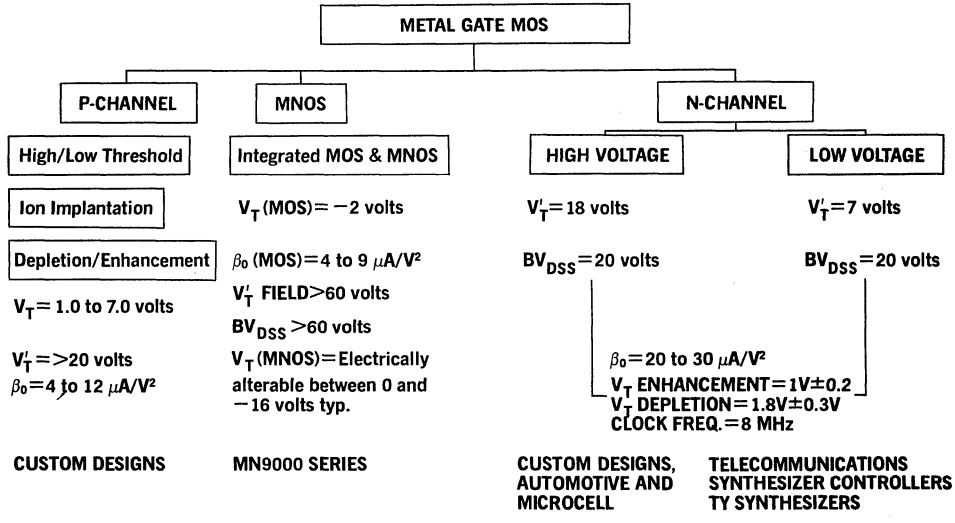


# Plessey MOS Processes

**P-channel metal gate MOS** has been in production for years and is used for both standard Plessey products and custom LSI. Using ion implantation to modify transistor and field threshold voltages, we can reproduce virtually any p-channel metal gate process, with or without depletion loads.

**MNOS (non-volatile)** is essentially a p-MOS process with variable threshold memory transistors fabricated alongside conventional MOS transistors. A modified oxide-nitride gate dielectric permits the injection and retention of charge to change the threshold voltage. Current Plessey products will retain an injected charge for at least a year, and include an on-chip high voltage generator so that they may be used with standard supply voltages.

**N-channel metal gate MOS** uses an auto-registration co-planar process with layout similar to our p-MOS. Ion implantation is used to define the threshold voltage of the depletion and enhancement transistors. The constant-current-like characteristics of depletion load devices give the most effective driving capability, and enhancement-depletion technology simplifies design and increases packing density. The field threshold voltage is also controlled by an ion implant, allowing the use of a lightly doped substrate. This reduces both the body constant and the junction capacitance and results in faster switching speeds.



# Plessey Bipolar Processes

**Bipolar Process I** is a conventional buried +N layer diffusion process with $f_t$=600 MHz and other characteristics similar to industry-standard processes. Applications range from high reliability military devices to high volume consumer products.

| Process Variant | A | B | G | D |
|---|---|---|---|---|
| Application | General Purpose | Non Saturating Logic | Saturating Logic | Linear Consumer |
| $BV_{CBO}$ @ 10$\mu$A | 20V min. | 10V min. | 10V min. | 45V min. |
| $BV_{EBO}$ @10$\mu$A | 5.3V to 5.85V | 5.15V min. | 5.15V min. | 6.8V to 7.4V |
| $LV_{CEO}$ | 12V min. | 8V min. | 8V min. | 20V min. |
| $V_{CE\ (SAT)}$ @ $I_B$=1mA, $I_C$=10mA | 0.43V max. | 0.32V max. | 0.43V max. | 0.6V max. |
| $h_{FE}$ @ $I_C$=5mA, $V_{CE}$=5V | 40 to 200 | 50 min. | 50 min. | 50 to 200 |
| $f_T$ @ $I_C$=5mA, $V_{CE}$=5V | 500 MHz | 500 MHz min. | 500 MHz min. | 350 MHz min. |

**Bipolar High Voltage (HV) Process** is a variant of Process I that yields an $LV_{ceo}$ greater than 45 volts. Doping levels can be controlled and an extra diffusion used to fabricate a buried avalanche diode with a 40 V breakdown for absorbing powerful noise transients without being destroyed.

| Process Variant | CA |
|---|---|
| $BV_{CBO}$ @ 10$\mu$A | 80V min. |
| $BV_{EBO}$ @ 10$\mu$A | 7.2V to 8.0V |
| $LV_{CEO}$ | 45V min. |
| $V_{CE\ (SAT)}$ @ $I_B$=1mA, $I_C$=10mA | 0.4V max. |
| $h_{FE}$ @ $I_C$=5mA $V_{CE}$=5V, | 80 to 300 |
| $f_T$ @ $I_C$=5mA, $V_{CE}$=5V | 250 MHz min. |

**Bipolar Process III** uses very shallow diffusion and extremely narrow spacing for high frequency integrated circuits with unusually low power consumption and high packing densities. An $f_t$ of 2.5 GHz allows us to routinely produce analog amplifiers with bandwidths as high as 300 MHz and low power dividers and prescalers that operate at frequencies up to 1.2 GHz. Process variants allow us to produce devices with an extended $\beta$, higher breakdown voltages and very small geometries.

| Process Variant | WE |
|---|---|
| Application | Digital |
| $BV_{CBO}$ @ 10$\mu$A | 10V min. |
| $BV_{EBO}$ @ 10$\mu$A | 5.1V to 5.8V |
| $LV_{CEO}$ | 7V min. |
| $V_{CE\ (SAT)}$ @ $I_B$=1mA, $I_C$=10mA | 0.5V max. |
| $h_{FE}$ @ $I_C$=5mA, $V_{CE}$=2V | 40 to 200 |
| $f_T$ @ $I_C$=5mA, $V_{CE}$=2V | 1.8 GHz |

**Bipolar Process 3V** is an extension of our Process III. Ion implantation and washed emitters have given the process an $f_t$=6.5 GHz, allowing us to produce dividers working at 2 GHz, logic gates with delays of less than 500 picoseconds and linear amplifiers at 1 GHz.

| Process Variant | WV |
|---|---|
| Application | Digital |
| $BV_{CBO}$ @ 10$\mu$A | 8V min. |
| $BV_{EBO}$ @ 10$\mu$A | 3.0V to 5.0V |
| $LV_{CEO}$@ 5mA | 6V min. |
| $V_{CE\ (SAT)}$ @ $I_B$=1mA, $I_C$=10mA | 0.5V max. |
| $h_{FE}$ @ $I_C$=10mA, $V_{CE}$=5V | 40 to 120 |
| $f_T$ @ $I_C$=5mA, $V_{CE}$=2V | 6.5 GHz |

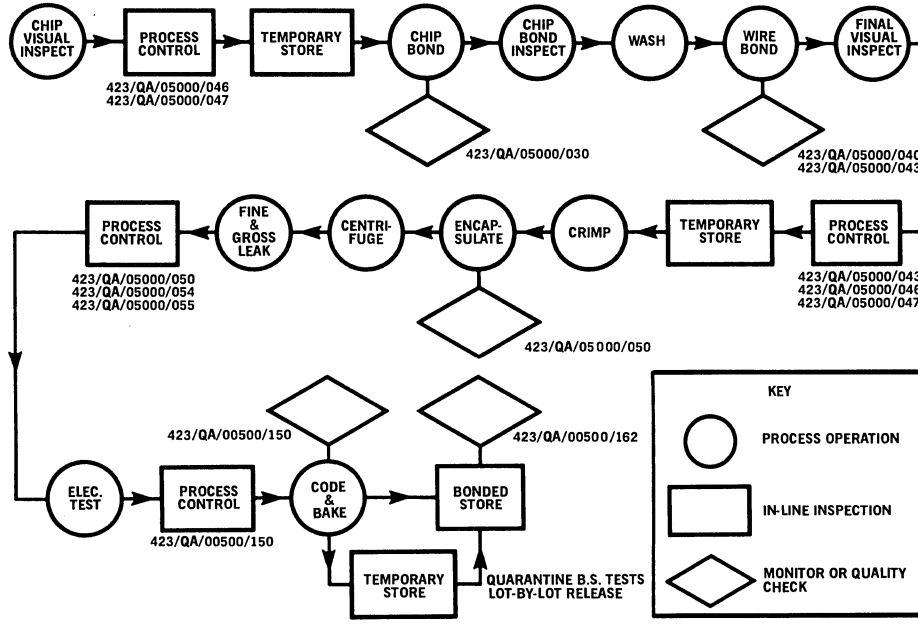
# Testing and Quality Control

A major thrust of our development work is to ensure that our processes will routinely produce reliable devices. Our Process III has a projected MTBF of 400,000 hours while our Process I is even better.

Our facilities include the latest test equipment (such as the Macrodata MD501, Teradyne J324 and Fairchild Sentry VII and Sentinel) to allow us to perform all the necessary functional and parametric testing in-house. We have an internal capability to provide specific applications-oriented screening, and most Plessey IC's are available screened to MIL-STD-883 and other international specifications. Our quality levels exceed the most stringent military, TV and automotive requirements as a matter of course.

But the best proof of all these claims is our products themselves. After you've reviewed the products that could help you with your systems, use the postage-paid reply card or contact your nearest Plessey representative for complete details.

**ASSEMBLY OF INTEGRATED CIRCUITS**
**QUALITY ASSURANCE**



# 2. The Design of Programmable Devices for UHF and VHF Synthesisers.

## INTRODUCTION

As communications traffic in the VHF and UHF radio bands increases, users of communications equipment are demanding more stringent specifications. These include a much greater number of channels available in an equipment, closer channel spacing, improved frequency stability, for both receiver local oscillators and transmitter drivers, and high speed channel selection of tuning. These pressures have led to the adoption of frequency synthesis to replace local oscillators in an increasing number of equipments. This move to synthesis gives an equipment virtually unlimited channel selection capability and a long term frequency stability derived from one reference source (typically an ovened crystal oscillator). Other requirements such as high tuning speed and good short term frequency stability are achieved by careful synthesiser loop design once a maximum comparison frequency (see Fig. 1) has been established.

If we look at a single loop synthesiser as shown in Fig. 1 we can see from the amount of programmable division required (typically 4000–16000 for a VHF–UHF avionics equipment) that a high proportion of any synthesiser's hardware will be devoted to this function. Clearly any economies that can be achieved in this area, in both total package count and in total power consumption will add appreciably to the final equipment's technical and economic viability. This area, in the feedback path between the Voltage Controlled Oscillator (VCP (VCO) and the phase/frequency comparator, is the particular concern of this application note.

### General Requirements of the Programmable Divider

The Phase lock loop of a frequency synthesiser acts to keep (see Fig. 1.):

$$f_{ch} = fcomp \qquad 1$$

since $fcomp = fout\ (N \times M)$

the output frequency fout is related to fch by:

$$\frac{fout}{N \times M} = f_{ch} \qquad 2$$

The factors M and N in equation 2 are the division ratios of the fixed and programmable parts of the feedback divider. N, the division ratio of the programmable divider is normally set in integer steps and consequently fout can only be altered in steps of $M.f_{ch}$. This figure, $M.f_{ch}$, is the minimum channel spacing attainable in a single loop synthesiser. A study of the dynamics of the loop (see refs) shows clearly that the reference frequency, fref, imposes an upper limit to the loop. This limitation in turn restricts the tuning time of the loop and also limits the short term stability which is attainable in the VCO. Consequently to achieve a given channel spacing on fout, without compromising the reference frequency fch, the value of fixed prescale M should be as small as possible.

At this point we should investigate the reasons for inserting M in the first place. Economical programmable division can only be achieved by using standard decades fabricated in one of the established technologies such as cosmos or TTL, or in extreme cases ECL 10K and the operational speed of these standard decades is restricted to a figure well below the VHF and UHF frequencies required (100MHz–500MHz) as output from the VCO.

Clearly, some means of reducing the VCO output frequency to an area where programmable division is possible is required. Until the advent of high speed ECL dividers such as the Plessey SP8000 series, linear techniques were adopted for this function. One of these techniques was to operate the VCO at a frequency sufficiently low to allow direct programmable division. The required output frequency was produced by frequency multiplication of the VCO output (see Fig. 2). With this technique it was difficult to produce a spectrally pure output. Additionally the minimum channel spacing was M. fref, limiting the loop performance for given channel spacing.

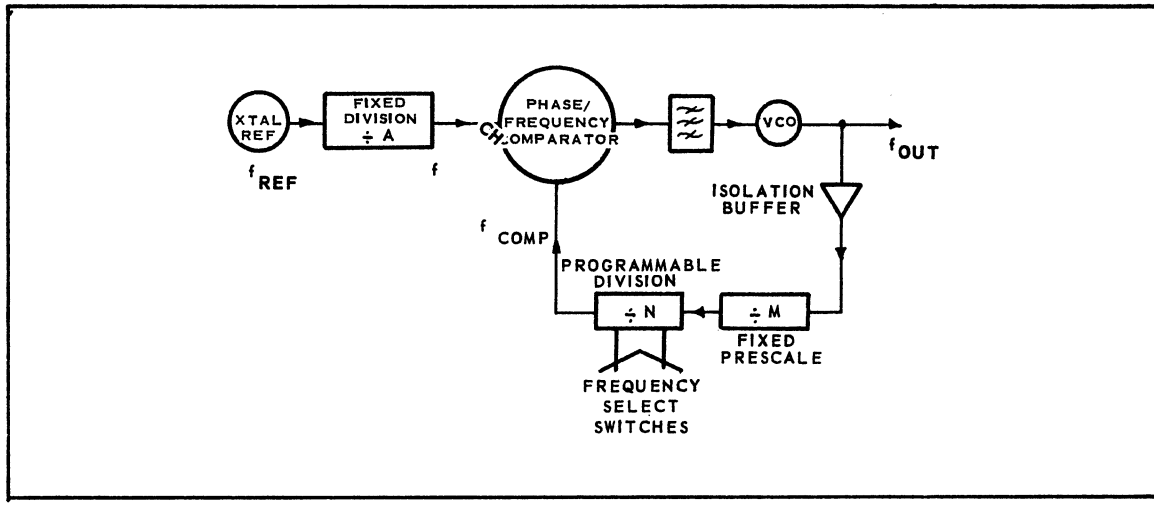



*Fig. 1 Single loop digital frequency synthesiser with prescaled division.*

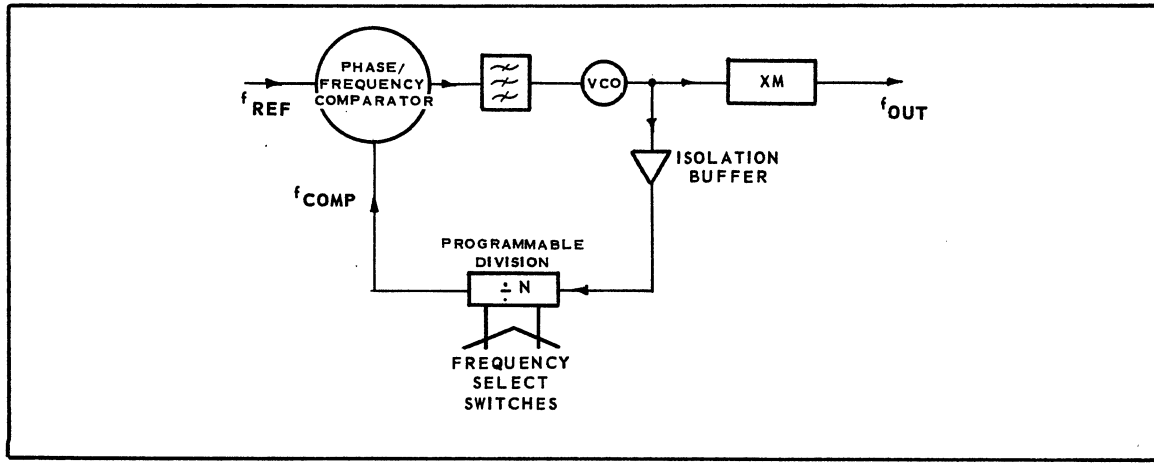



*Fig. 2 Single loop digital frequency synthesiser with frequency multiplier output.*

Another technique often adopted was to offset the VCO output in a mixer, shown in Fig. 3. The effect of the offset frequency, f off, on f comp is shown in equation 4.

$$fcomp = \frac{f_{out} - f_{off}}{N} \qquad 3$$

$$\text{i.e.} \quad fout = N \cdot f_{comp} + f_{off} \qquad 4$$

It is clear from equation 4 that this technique gives a reference frequency which is equal to the required channel spacing, so that loop performance is not compromised. However the addition of the offset frequency automatically reduces the achievable frequency stability of the VCO output. In addition the VCO

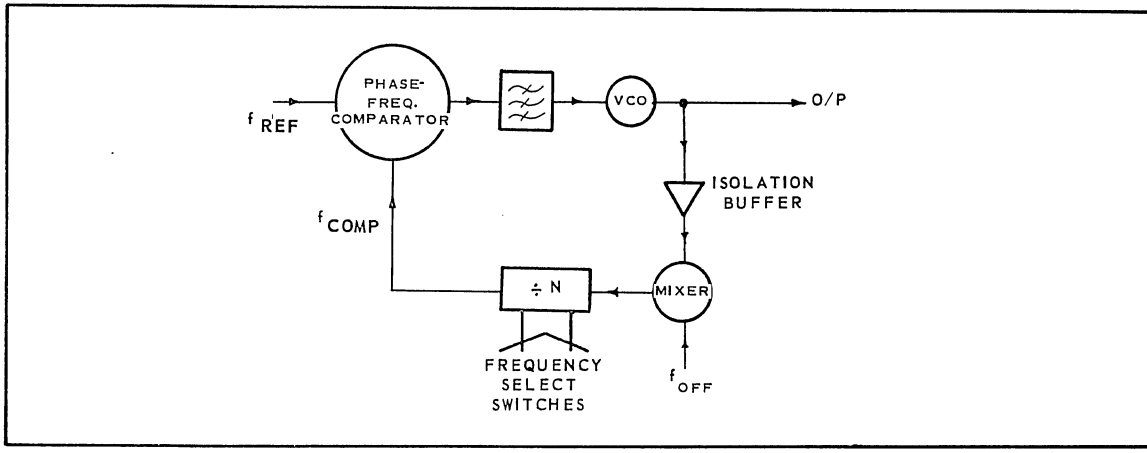



*Fig. 3 Single loop digital frequency synthesiser with VCO offset.*

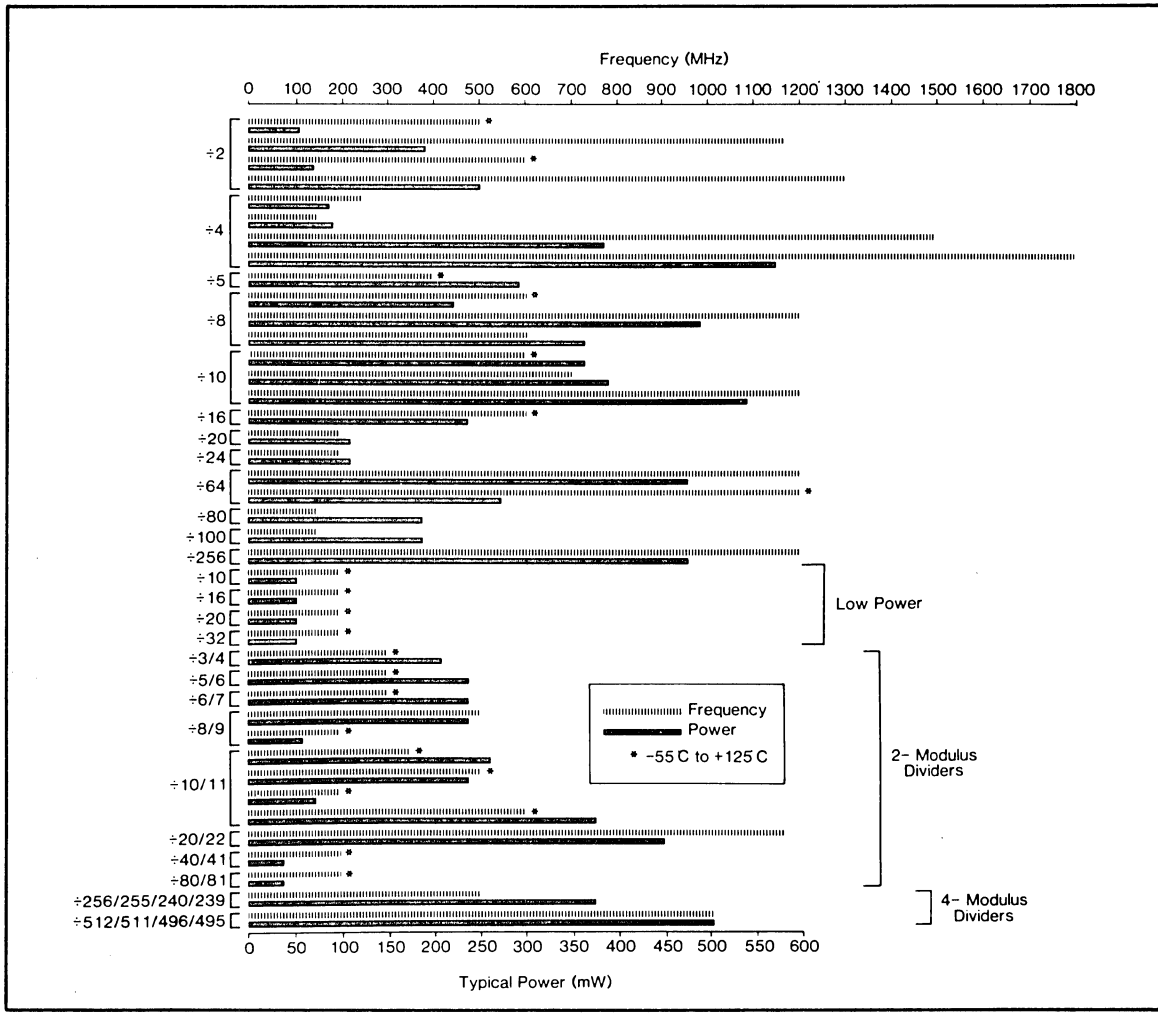



*Fig. 4 The SP8000 range of fixed–modulus dividers.*

output will be contaminated by sidebands introduced from $f_{off}$ via the offset mixer.

As I previously mentioned, these techniques became obsolete with the introduction of the Plessey SP8000 range of high speed dividers.

This range, illustrated in Fig. 4, has a comprehensive selection of division ratios, frequency performance and power consumption which can suit almost all requirements where fixed prescaling is appropriate.

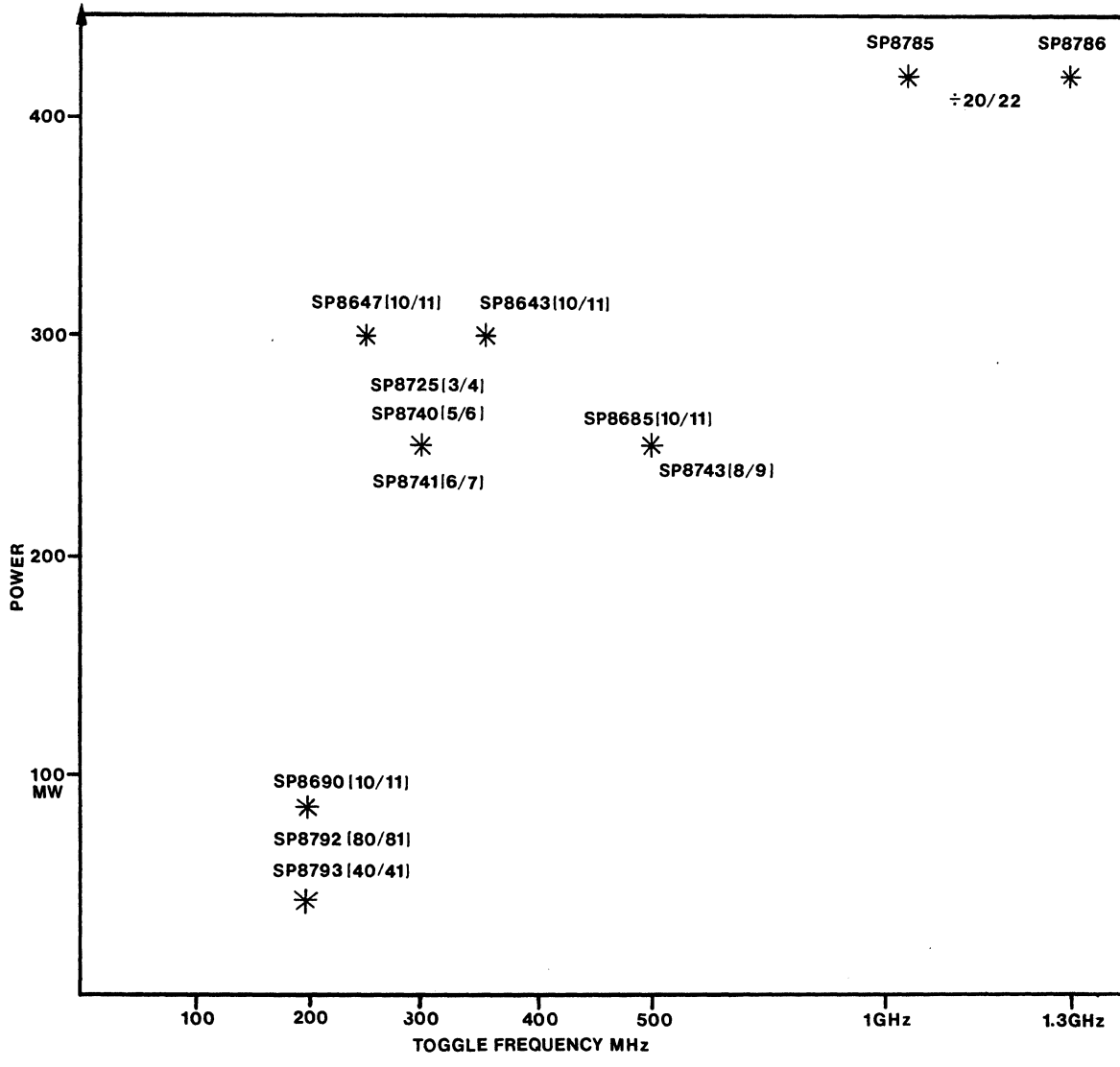



*Fig. 5 The SP8000 series (Two modulus prescalers).*

## Fixed or Variable Prescaling?

If we return to the effect of fixed prescaling on loop response times it is clear that as the VCO frequency extends upwards in the UHF band the amount of prescaling required to reduce it to a suitable value for programmable division becomes excessive. Fortunately help is at hand. If a prescaler is available whose division radix can be switched between two or more values then it is possible to have effective programmable division at the prescaler input frequency, with the actual programmable dividers operating at the output frequency of the prescaler. Fortunately such devices are available as ÷ 10/11 in several forms in the Plessey SP8000 series. The available versions of ÷ 10/11 circuits are shown in Fig. 5 which illustrates the wide range of speed/power option in the SP8000 series. Also available are alternative division ratios of ÷ 3/4, 5/6, 6/7, 8/9, 20/22, 40/41 and 80/81.

In order to illustrate how a two modulus divider operates we should look at Fig. 6 which shows, in block diagram form, how a two modulus divider system is organised. In Fig. 6 the output of the prescaler, (which can divide by 'P' and(P + Q), drives two programmable dividers in parallel. These two dividers are programmed to 'A' and 'N'. The 'A' counter and the prescaler are interconnected in such a way that in a complete count cycle the prescaler divides by (P + Q) until the A counter reaches zero and then reverts to a division ratio of 'P' . The 'A' counter is connected to the 'N' counter such that when the'N' counter reaches its programmed state both the 'N' and 'A' counters reset. Consequently the prescaler divides by '(P + Q)' for 'A' counts and by 'P' for '(N + A)'.

i.e. The programmed count of the combination, R, is;

$$R = (N - A)\ P + A\ (P + Q) \qquad 5$$

i.e.

$$R = NP + AQ \qquad 6$$

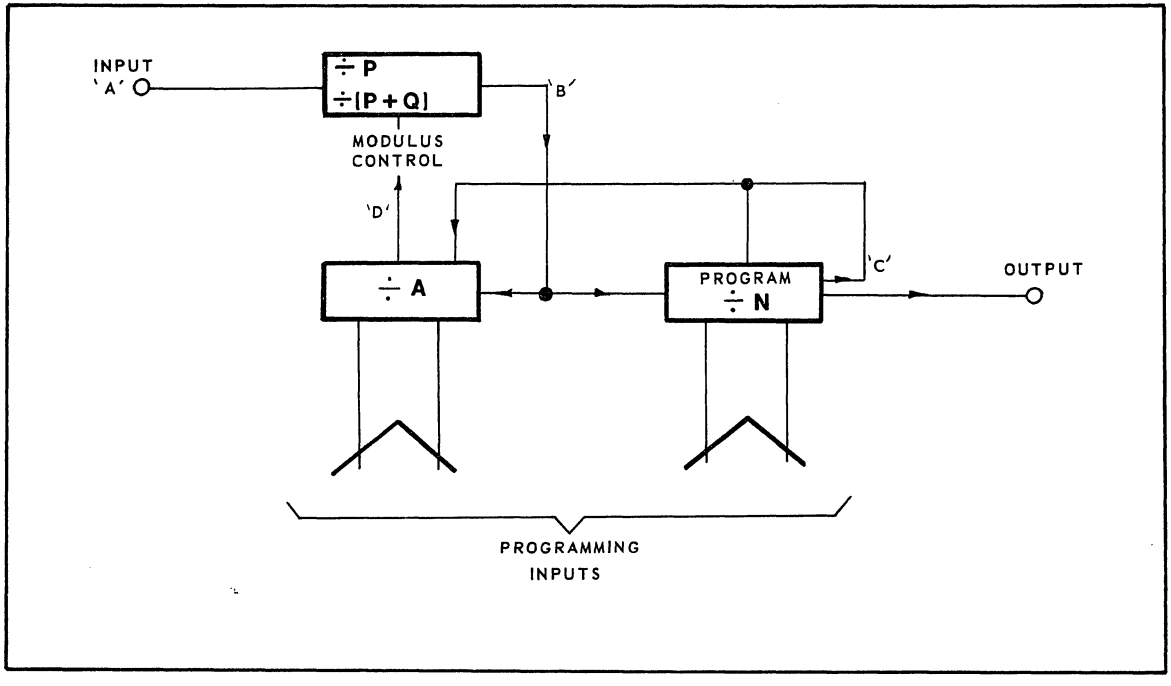



*Fig. 6 A two modulus division system.*

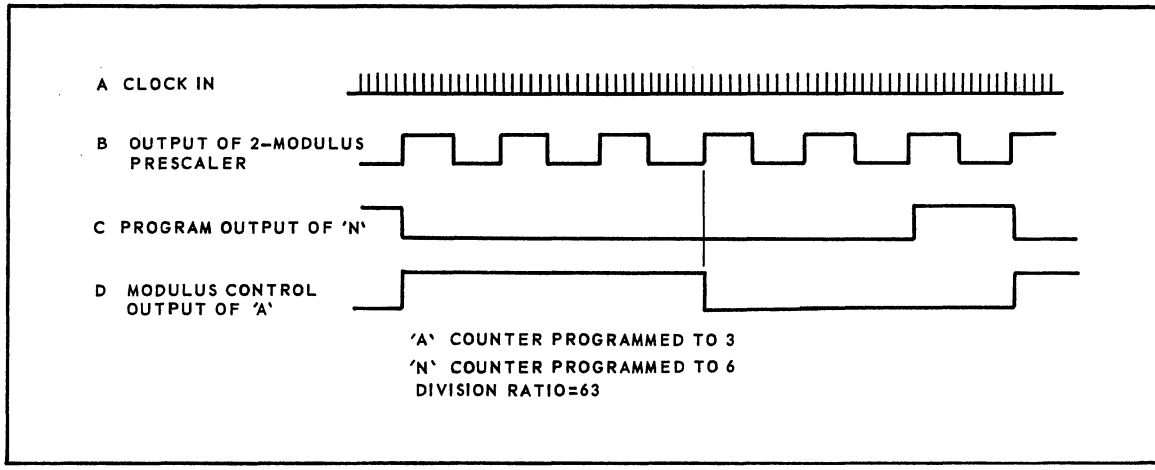



*Fig. 7 Typical two-modulus waveforms.*

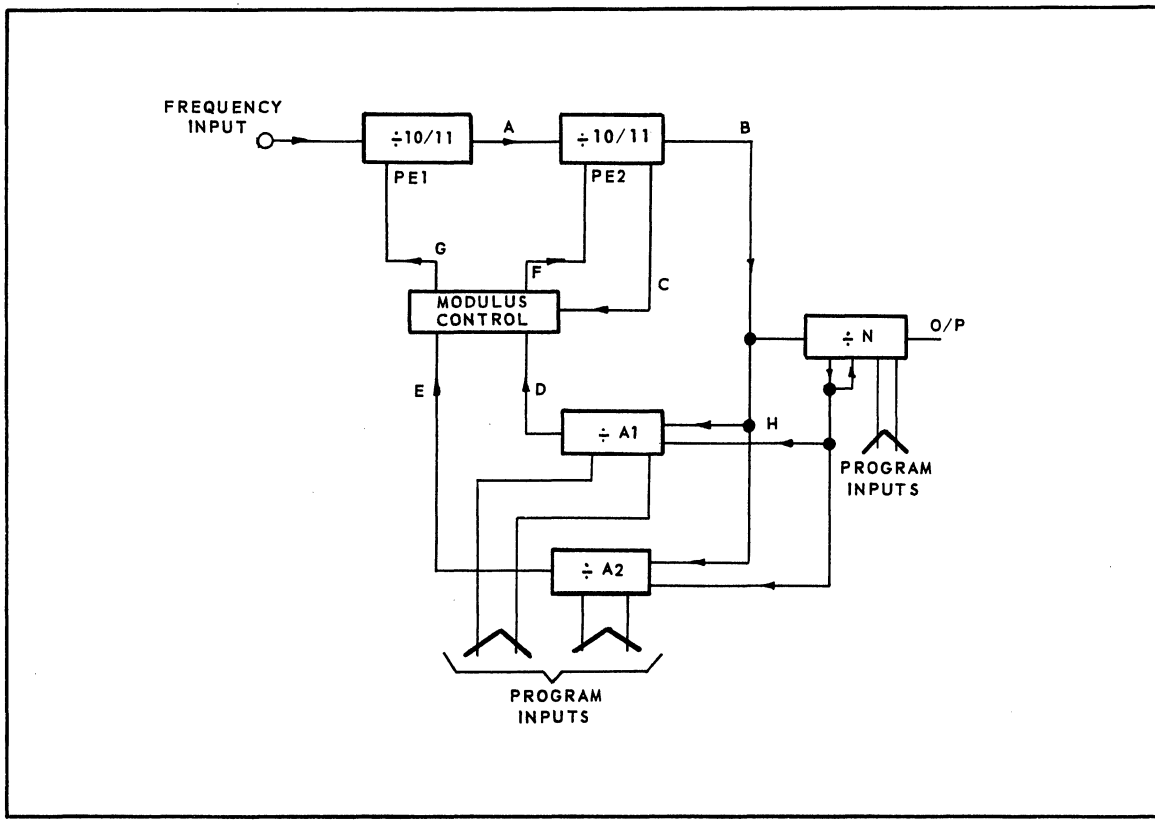



*Fig. 8 A programmable divider using a ÷ 100/101/110/111 prescaler.*

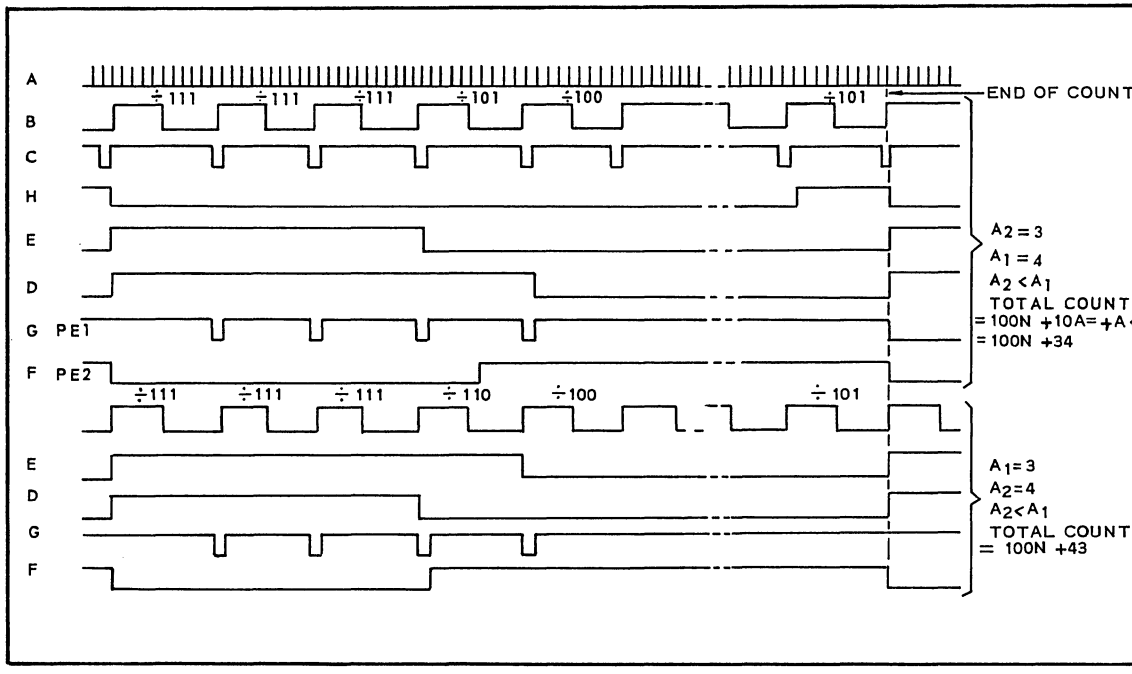



*Fig. 9 Waveforms for four–modulus prescaler.*

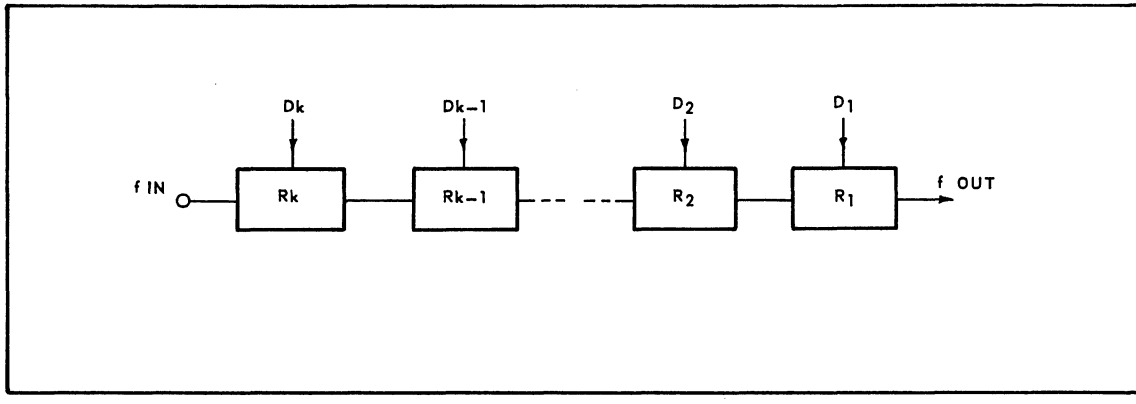



*Fig 10 Generalised divider.*

clearly if P=10, Q=1 then for a complete divider 'A' will give the least significant digit and 'N' will cover the rest of the required digits. Clearly, the minimum range of 'A' which can be tolerated for continuous programming is 'P' (10 in this case). The only restriction on the programmed division ratio attainable with this scheme is that

$$N > A \qquad 7$$

consequently, in the particular example given above of a ÷ 10/11,

$N > A$

$A_{max} = P$ gives a minimum division ratio;

$R = 100$

This minimum count of 100 would not normally cause any problems in a system. However in a practical system, i.e. a VHF synthesiser covering the band 85MHz to 130MHz in 10kHz steps, a two modulus prescaler with moduli of 100 and 101 would be required to reduce the VCO output to a level at which cmos decades can be used. This gives a minimum count 10000 and consequently the minimum frequency that could be programmed would be 100MHz. Clearly a large part of the required frequency spectrum is not covered. To overcome this restriction it is possible using a basic 10/11 prescaler, to construct a prescaler with three or four moduli and this will be described in more detail below. In this particular VHF synthesiser we would use a four modulus prescaler with moduli of 100/010/110/111, and these would be controlled by two 'A' counters in parallel as shown in Fig. 8, with operational waveforms illustrated in Fig. 9. Counter '$A_2$' controls the addition of 10 to the basic modulus of 100 and consequently '$A_2$' should be programmable from 0–9. Counter '$A_1$' controls the addition of 1 to the basic modulus (100) and should also be programmable from 0–9. For programming, '$A_1$' and '$A_2$' may be visualised as setting the least significant digits respectively. By putting '$A_1$' and '$A_2$' in parallel we have reduced the minimum count of 'N' to the greater of '$A_1$' and '$A_2$', 10 in this case, consequently the overall minimum count is 1000 ($= N_{MIN} \times P$) and the minimum programmable freuqency is now 10MHz. Various changes can be rung with this technique. For example, if a three modulus prescaler, 100/101/110, is used for this VHF synthesiser, two 'A' counters are still required but they now operate in series, '$A_1$' which controls the addition of 1 to the modulus, is now required to be programmable from 10–19, while $A_2$, which controls the addition of 10 to the modulus is still only required to be programmed from 0–9. However the minimum count of 'N' is now 20 and consequently the overall minimum count of the counter is 2000, giving a minimum output frequency of 20MHz. In this case, then, we have traded minimum count for prescaler complexity. An example of this type is given below.

When deciding whether to use fixed or variable prescaling in a synthesiser divider, the designer will have to consider the cost of improving performance. In most situations the minimal extra cost of incorporating a variable modulus prescaler with its more complex programmable divider will be more than offset by the performance improvements achieved by increasing the reference frequency.

## Division Radix Requirements

Regardless of whether fixed or variable prescaling is adopted in any synthesiser divider, a considerable amount of programmable division is required. There exsist in the semiconductor market today standard building blocks from which programmable dividers can be fabricated. These blocks are are available, usually, in decades although the basic division radix can be reduced if necessary. Nowadays the output frequency of a synthesiser is most often set from thumbwheel or rotary switches located on the equipment front panel.

It would obviously be a considerable advantage to be able to control each block of programmable division from its own switch. Where channel frequency spacings are decadic switch programming corresponds to division programming in a direct manner, but to see what general requirements are put on the division radices of a programmable divider we should consider a generalised divider as shown in Fig. 10.

Fig. 10 represents a variable divider of 'K' stages where each stage has a division radix of $R_k$ and is programmed to $D_k$ where 1 k (. The total division ratio 'N' is:

$$N = D_K (R_1 \times R_2 \ldots R_{K-1}) + D_{K-1} (R_1 \times R_2 \ldots R_{K-2}) + D_3 (R_1 \times R_2) + D_2 \times R_1 + D_1 \quad 8$$

and from equation 2

$$fout = fch.N$$

$$fout = fch \quad D_K (R_1 \times R_2 \ldots R_{K-1}) + D_{K-1} (R_1 \times R_2 \ldots R_{K-2})$$

$$+ D_3 (R_1 \times R_2) \quad D_2 \times R_1 \quad D_1 \quad 9$$

or $$fout = fch \, R_1 \quad D_K (R_2 \times R_3 \ldots R_{K-1}) + D_{K-1} (R_2 \times R_3 \ldots R_{K-2})$$

$$+ D_3 \times R_2 + D_2 + D_1 / R_1 \quad 10$$

i.e. for $R_2 \ldots R_{K-1}$ to be decades and for a direct relationship between the programmed digits, $D_K$, and fout:

$$fch \times R_1 \quad 10^P \text{ where P is an integer} \quad 11$$

A typical non decadic channel spacing would be 25kHz and this would require $R_{1\ MIN} = 4$.

This argument also applies to variable modulus prescalers. The basic modulus (or radix) of the prescaler must obey equation 11 for $R_1$ if the 'N' counter is to be directly programmed. The prescaler is usually given a basic modulus larger than the minimum required by equation 11 for two reasons:

(1) Variable modulus prescalers are normally specified where a large amount of fixed prescaling would be the alternative. The VCO frequency still has to be reduced to a value suitable for standard logic families.

(2) The most common base unit for variable modulus prescalers is ÷10/11 and other moduli are produced by cascading this with fixed dividers, for example, a ÷4 or ÷8 to give prescalers od ÷40/41 or ÷80/81.

In the example used above with 25kHz spacing, a two modulus prescaler, with moduli of 40 and 41 would be required to give a directly programmable 'N' counter. The 'A' counter would also have to obey equation 11 on these lines i.e. it would consist of a ÷4 followed by a decade.

## The Programmable Divider

There are several integrated circuit technologies which are suitable for use in the programmable divider These can be divided into two groups; those with standard building blocks and those which are useful for custom designed dividers.

(a) Standard Building Blocks

(1) Plessey SP8200 series of RTL programmable dividers with switchable offset.

(2) Plessey NJ8000 series of N channel programmable dividers.

(3) Standard TTL programmable decades.

(4) Standard CMOS programmable decades.

(b) Custom Technologies

(1) NMOS arrays (available from Plessey Semiconductors).

(2) $I^2L$ arrays (available from Plessey Semiconductors).

(3) CMOS arrays (available from Plessey Semiconductors).

This list is not exhaustive but covers the commonly used technologies. Plessey Semiconductors has competence in all groups.

This note will note attempt to explore the area of custom solutions to the programmable divider but will concentrate on designs using standard building blocks of the types listed in group (a) and more particularly those of sub groups '2' and '3'.

To illustrate how the techniques of variable modulus prescaling and programmable division which have been described above can be applied to practical systems; two divider chain requirements will be disscussed. The first will be for a VHF–UHF avionics synthesiser covering the bands 117.5MHz–136MHz and 225MHz–399.9MHz with 25kHz channel spacing, the divider for this will be designed using TTL parts. The second illustration will be for a low power VHF synthesiser with 10kHz channel spacing, using standard CMOS parts for the programmable f divider.

## A PROGRAMMABLE DIVIDER SUITABLE FOR A VHF–UHF AVIONICS TRANSCEIVER SYNTHESISER USING PLESSEY SP8600 AND STANDARD TTL DEVICES

The frequency specification for the synthesiser is as follows:

| | |
|---|---|
| Frequency Coverage: | 117.5MHz–136MHz<br>225MHz–399MHz |
| Channel spacing | 25kHz |
| IF offset | +21MHz |

Other performance requirements such as lock range, loop response times and so on, although important will not considered in the design of the programmable divider. The emphasis in this design will be on a high performance divider providing a high frequency. The final Design is shown in Fig. 11. In order to achieve a high reference frequency it is necessary to restrict the amount of fixed prescaling to a minimum. Consequently a two–modulus prescaler system has been adopted. Referring back to the section on radixes we note that equation 11 gives:

$$fch \cdot R_\phi = 10^P$$

fch=25kHz and consequently $R_\phi min = 4$. This value of '$R_\phi$', as a base modulus for the prescaler would give a frequency for programmable division at the high end of the required band of 100MHz. This would be extremely difficult to achieve. Increasing '$R_\phi$' by a factor of 10 gives the prescaler a base modulus of 40 and reduces the frequency at which true programmable division is required to 10 MHz., well within the capabilities of TTL, and a suitable combination of devices for this ÷40/41 is the SP8685 500MHz ÷10/11 followed by the SP8790 low power ÷4 control circuit, as shown in Fig. 12. A more stringent performance requirement for the programmable divider is its clock to carry delay, as this determines the overall speed of the two modulus prescaler programmable divider combination. To understand this we should look at Fig. 13. Assuming that the modulus control signal for the prescaler is required immediately prior to its output clocking edge then the 'clock to carry' delay for the controlling counters must be less than one complete 'clock out' period. In this case the 'clock to carry' propagation delay should be less than 100nsecs at 400 MHz input frequency. In practice not all of the 'clock out' period available to the programmable divider as there is a clock in to clock out delay for the prescaler combination, an interface delay from the 'programmable divider carry out' to 'modulus control' and a set up time for the modulus control. These can easily total 30nsecs and start to put pressure on the slow programmable divider chain. This will be covered in more detail below.

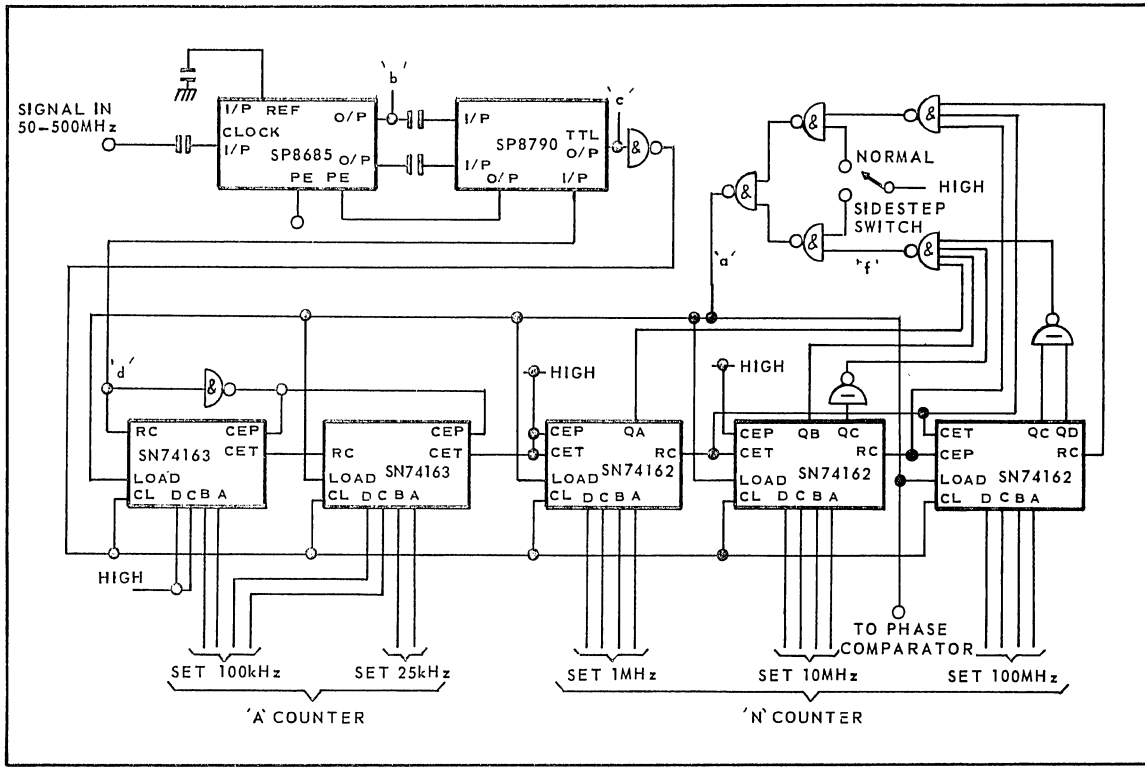
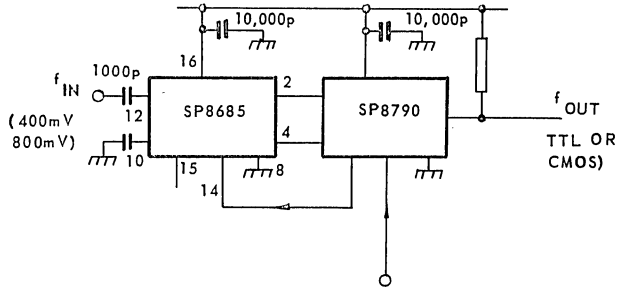



*Fig. 11 Complete UHF/VHF synthesiser divider.*




Any of the Plessey Two–Modulus dividers may be used here. For example with an SP8690 the total power consumption would be only 120 mW at an input frequency of 200 MHz.

*Fig. 12 A 500 MHz two–modulus (40/41) prescaler.*

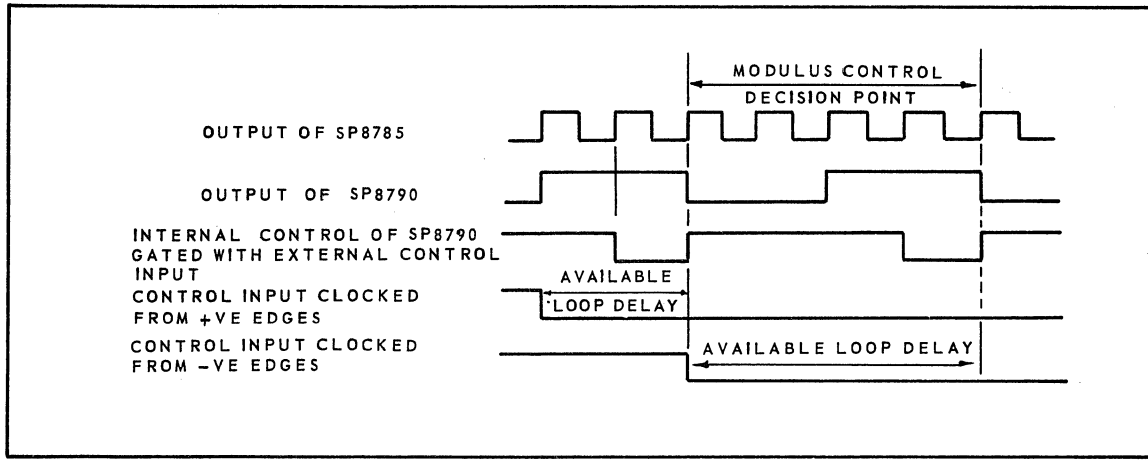



*Fig. 13 Critical timing of ÷40/41.*

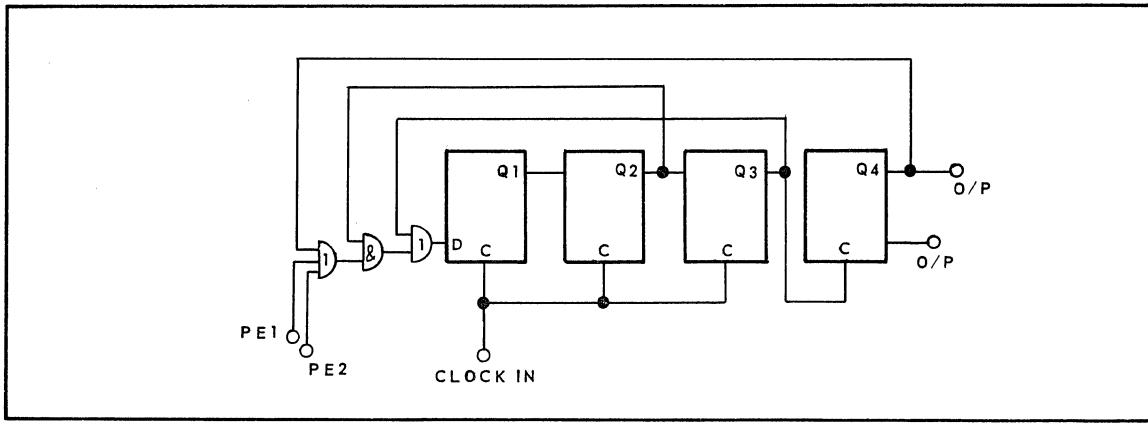



*Fig. 14 Logic diagram of SP8685 two-modulus (÷10/11) divider.*

| CLOCK PULSE | OUTPUT | | | |
|---|---|---|---|---|
| | Q1 | Q2 | Q3 | Q4 |
| 1 | L | H | H | H |
| 2 | L | L | H | H |
| 3 | L | L | L | H |
| 4 | H | L | L | H |
| 5 | H | H | L | L |
| 6 | L | H | H | L |
| 7 | L | L | H | L |
| 8 | L | L | L | L |
| 9 | H | L | L | L |
| 10 | H | H | L | L |
| 11 | H | H | H | H |

EXTRA STATE

TABLE 1
COUNT SEQUENCE OF PLESSEY ÷10/11 TWO MODULUS - DIVIDERS

## The ÷40/41 Prescaler

Two modulus prescalers can be constructed in a variety of ways. One approach is to use standard ECL 10k dual J–K flip–flops to perform the counting function with additional peripheral gating to accomplish the the modulus changing and interface requirements. However this would be limited to a maximum count frequency of about 100MHz. In order to produce the ÷40/41 function economically with performance adequate for the stated specification we must turn to a combination of two Plessey Semiconductor parts. These are the SP8685, a UHF two modulus (÷10/11) divider specified to operate at frequencies up to 500MHz, and the SP8790, a ÷4 control circuit designed to follow any of the Plessey two modulus dividers, which includes the necessary interfaces between the ECL levels in the prescaler and the TTL (or CMOS) levels of the following fully programmable divider. This combination, which given the ÷40/41 function, is illustrated in Fig. 11. Fig. 15 gives the expected waveforms and some timing information.

The Plessey SP8685 two modulus prescaler consists of a synchronously clocked decade as shown in Fig. 14 with additional gating to add an extra state, converting the decade to ÷11, when required. The counting sequence is shown in Table 1. This extra state is added immediately prior to Q4 going high and consequently the following stages must all be synchronous with this positive going edge to achieve the maximum available loop delay as shown in Fig. 13. The SP8790 clocks on positive going edges and following stages should clock on –ve going edges of its output. Since following TTL dividers usually clock on +ve going edges this would appear to be an embarassment. However the following stages are usually arranged to be synchronously clocked to reduce sources of VCO output phase jitter. Since the open collector output of the SP8790 has a limited fan out some form of buffer will be required, and an inverting TTL buffer, having shorter propagation delays than non–inverting buffers, represent the optimum choice here.

It can be seen from Fig. 9 that the input of the prescaler is buffered. If we examine the input circuitry of the prescaler we can see that it presents a non–linear impedance. Since this is driven by a Voltage Controlled Oscillator which is also intended to provide a spectrally pure signal for use elsewhere, (i.e. in a communications receiver) it is important to isolate the VCO from the divider input impedance so that the VCO output is not degraded. The buffer is intended to provide this function. A target for the amount of isolation between the divider input port and the VCO output port is typically 60dB although many systems will tolerate lower values. There are many commerically available microwave integrated circuits (MICs) available (i.e. Avantek GPD401) which give upwards of 20dB isolation and similar amounts of 'tame' gain, if one of these is coupled with an attenuator, adequate amounts of isolation can be provided economically.

## The TTL Programmable Divider

Essential functional features of the TTL programmable dividers are:

(1) Clock speed, including programming, exceeding 10MHz.

(2) Low propagation delay from clock to carry for a complete divider (< 70nsecs).

(3) Synchronous clocking for minimum phase jitter.

(4) Ability to add fixed offsets to the programmed count easily.

There are several different ways of assembling programmable dividers but one of the faster and more flexible dividers to use are those in the SN74160 series. These are decade and binary programmable up counters with synchronous load and synchronous or asynchronous clear, together with internal logic to give a modified carry look ahead system. (A detailed description of the operation and interconnection of these devices can be found in TI's Semiconductors Circuit Design Vol 11.)

The programmable divider as previouly described and illustrated in Fig. 6 is split into two parts: the 'A' counter and the 'N' counter. The total division ratio achieved by this combination is given by equation 6 and the required range of division ratios can be calculated from

$$N_T = \frac{f_{out}}{f_{ch}} \qquad 12$$

$$N_{Tmax} = \frac{f_{out\ max}}{f_{ch}} = \frac{400 \times 10^6 + 21 \times 10^6}{25 \times 10^6} \qquad 13$$

$$N_{Tmax} = 16840 \qquad \text{and} \qquad N_{Tmin} = \frac{117.5 \times 10^6}{25 \times 10^6} = 4700$$

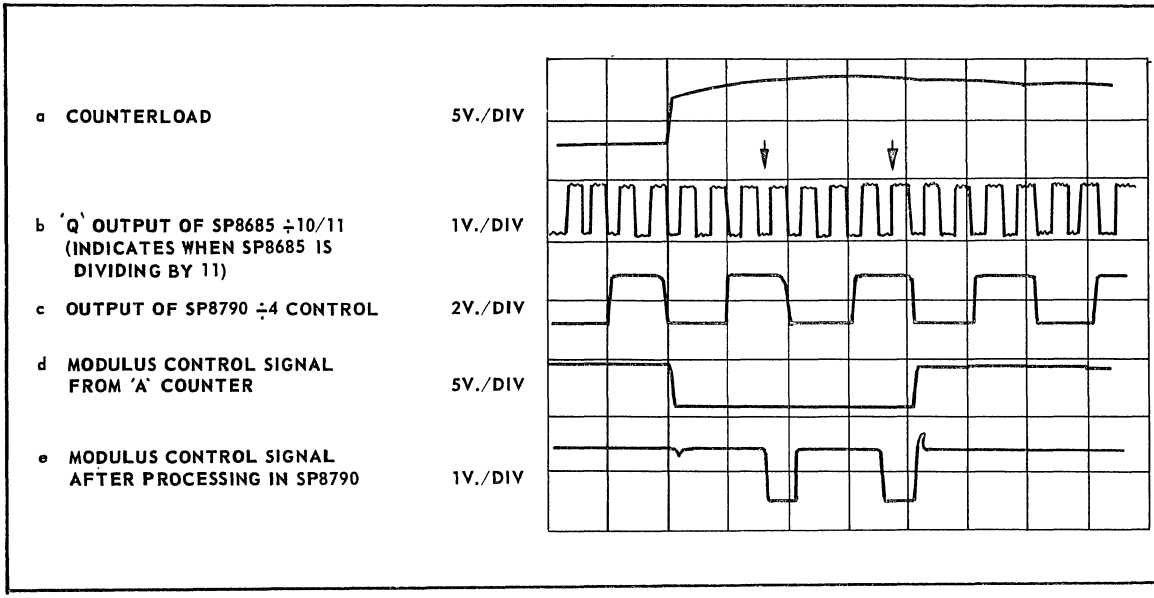



*Fig. 15 Waveforms of ÷40/41 programmable divider with 'A' counter programmed to 50 Khz.*

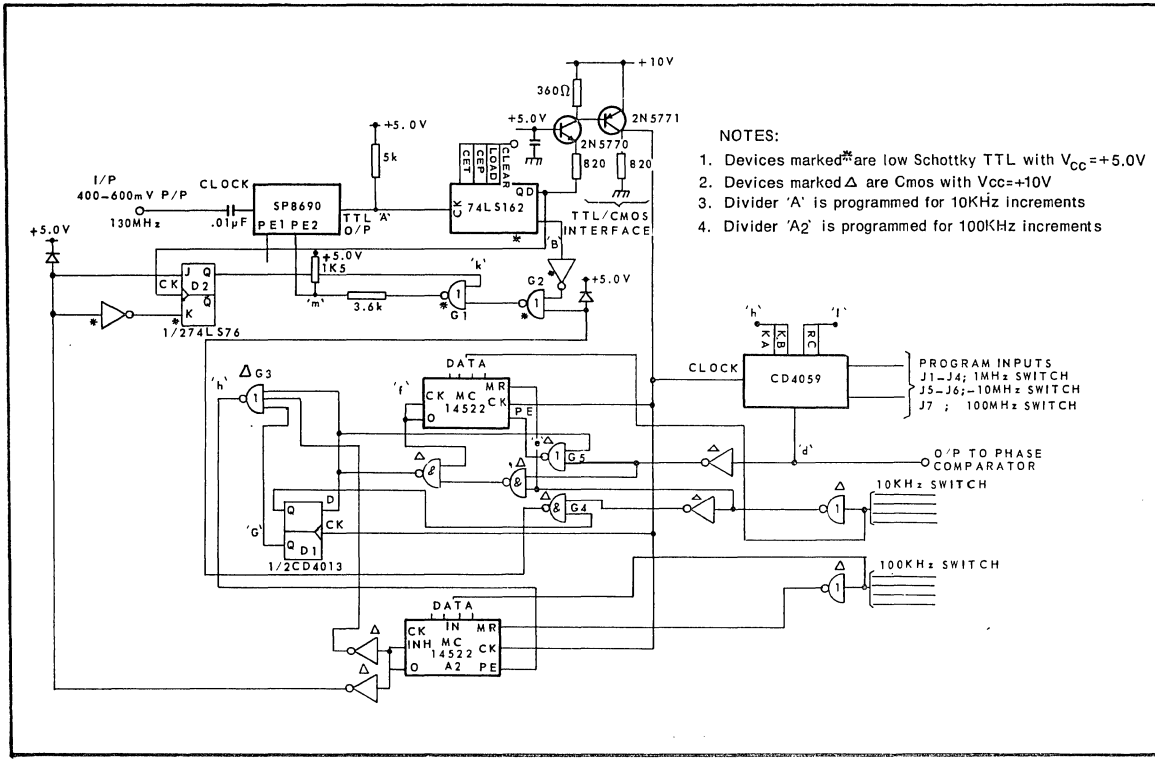



*Fig. 16 Low power VHF synthesiser divider.*

## The 'A' Counter

For correct operation it is clear from equation 6 that the 'A' counter must interpolate within the steps caused by the prescaler's base modulus, 40 in this case; consequently the 'A' counter must be programmable between '0' and '39'. Furthermore the 'A' counter must be split into a radix 4 first stage for programming 25kHz steps, followed by however many decades are required to make the desired maximum count.

In this example where 'A' max = 39, the next stage is the most significant stage of the 'A' counter and as such does not have a fixed radix but counts down from its programmed number, in the range '0–9', to zero. Consequently a 6 bit binary divider can be used for the 'A' counter. This is formed from two cascaded 4 bit binary counters connected the programmed as shown in Fig. 11.

## The 'N' Counter

The 'N' counter should be programmable from 117 to 421, and is formed in a straightforward way from 3 standard cascaded decades, shown in Fig. 11.

## Sidestep

Extra gating has been added to the basic divider so that the fixed sidestep of+21MHz can be added. The counters are such that it is, in general, difficult to arrange for a positive sidestep, to get around this we split the sidestep into a positive sidestep of one on the most significant stage, which is relatively easy, and a negative sidestep on the preceding decades so that the sum of the two equals the required sidestep.

Since the most significant stage has a limited programming range (1–3) it is a simple matter to arrange to recognise one count further on in the counter cycle than its normal recognition state of all '1s' without interfacing with programming. This is shown in Table 2. This gives an overall sidestep of+100. To achieve the required+21 we must subtract 79 from the two preceding stage and this is done by recognising the requisite counter states, rather than the normal all '1's. This combined recognition (Fig. 11,'f') is selected as the counter load signal ('a') whenever the sidestep is required. Clearly this scheme is applicable to positive sidesteps of up to several hundred megahertz. Negative sidesteps which do not exceed the programmed count can be equally easily inserted on the two least significant stages of the count.

## Operation

To understand the operation of the two combined counters we will follow the operation of the counter from the instant when it is programmed. Looking at Fig.11 the complete circuit diagram and Fig. 15, the photo of some of the internal waveforms, the two counters 'A' and 'N' are programmed on the first –ve going edge of 'c' following the load 'a' going low, 'A' and 'N' start to count up from their programmed values at this instant. 'd'(Fig. 11) is set low and its inverse is used to drive the 'CEP' inputs of the 'A' counter. 'd' is used directly to control the ÷40/41 via the SP8790. Consequently, for the whole of the period that 'A' is counting down the prescaler is dividing by 41. This is illustrated in Fig. 15, if traces 'b', 'd'and 'e'are compared we can see that'e'goes low for a quarter of the period of'c'while'd'is low. If'e'and'b' are correlated we can see that the high period of'b' is slightly longer when'e' is low (marked with arrow). This corresponds to the two modulus divider dividing by 11 rather than 10. As soon as the 'A' counter reaches its recognition state'd'goes high and the prescaler reverts to ÷40. CEP goes low, preventing further incrementing of the 'A' counter, hence'd'remain high. When the 'N' counter reaches it recognition state, either direct or sidestepped, a goes low for 1 complete period of'c'and both dividers are synchronously loaded with the frequency setting data,'d'goes low and the count cycle repeats.

## Operating Speed

The maximum operating speed is determined by the loop delay from'clock in' to'modulus control.' For the loop to operate correctly this delay must be less than the output period of the prescaler, in this case equal to

$$\frac{1}{\frac{400 \times 10^6}{40}}$$

or 100nsec. This delay is made up of two parts, the clock propagation delay through the prescaler and the return propagation delay of the modulus control through the SP8790, which is <20nsec in total, and the delay through the programmable divider.

The delay through the programmable divider consists of 1 gate delay in the clock buffer plus the clock to carry delay for 1 counter stage. This is less than 40nsec for both edges. There is however an additional factor to be considered. This is the delay from clock to load for the divider. This has different values depending on whether sidestep is in use or not.

| | Delay (nsec) | |
|---|---|---|
| | without sidestep | with sidestep |
| Clock buffer | 4.5 | 4.5 |
| Clock to RC | 35 | |
| Clock to Q | | 20 |
| Recognition gate | 4.5 | 9.0 |
| Recognition select | 9.0 | 9.0 |
| Load set up time | 25 | 25 |
| Total | 78nsec | 67.5nsec |

Clearly this scheme is capable of operating well beyond the required limit of 400+21MHz, in fact a prototype of this system operated satisfactorily to beyond 500MHz at room temperature. This solution, although representing the ultimate in a divider for a single loop synthesiser, is clearly economical in packages and in power consumption, thanks mainly to the functional specifications of the Plessey SP8685 and SP8790 combination.

## A PROGRAMMABLE DIVIDER SUITABLE FOR A PORTABLE VHF SIGNAL SOURCE USING PLESSEY SP8600 DEVICES AND STANDARD COSMOS INTEGRATED CIRCUITS

The specification for the synthesiser is as follows:

| | |
|---|---|
| Frequency coverage | 85MHz – 130MHz |
| Channel spacing | 10kHz |
| IF offset | 0 |

The other performance specification of concern is the requirement for portability. This predicates a low power approach to the design of the prescaler and variable divider. For this reason the prescaler is made of low power devices from the SP8600 series driving CMOS programmable divider chains.

### The Prescaler

The use of CMOS programmable dividers for the 'A' and 'N' dividers means that there must be a large amount of prescaling used to reduce the input frequency of 130MHz maximum to the 1–2MHz suitable for CMOS .

In order to keep the phase comparison frequency (fcomp in Fig. 1) as high as possible it is desirable to use a two (or more) modulus prescaler. To maintain direct decadic frequency programming with the required 10kHz frequency incf increment (or channel spacing) the base modulus of the prescaler must be a power of 10. Clearly a straight ÷10/11 prescaler would not interface with CMOS as its output frequency would be 13MHz. The next available step would be to use a ÷100/101 prescaler which satisfies the CMOS requirement. The large base modulus of the prescaler brings us up against a problem mentioned previously, that of minimum count. The minimum count which could be achieved with a ÷100/101 prescaler is 10,000, see equations 6 and 7. The minimum count required by the synthesiser, Q min 65:–

$$Q_{min} = \frac{85 \times 10^6}{10^3} = 8,500$$

Clearly we cannot cover the whole required frequency band with a two modulus prescaler of the required size. We must resort to a 3–modulus prescaler ( ÷100, 101, 110) to allow us to cover the whole band as stated in the section, "Fixed or Variable Prescalers." This gives us a minimum division ratio of 2,000, well below our required minimum division ratio.

To make a ÷100/101 we require a decade divider with the tenth state decoded to feed back to the ÷10/11 modulus control. This, when gated with a ÷100/101 modulus control input will cause the ÷10/11 to ÷11 for 1 period out of 10, giving an overall division ratio of 101, To achieve the ÷110 function the ÷10/11 must be forced to ÷11 permanently. This total function is achieved by an SP8690 a.c. coupled low power, 200MHz two modulus divider followed by a TTL decade divider (74162) with some associated gating. The 'RC' output of this device is the gated tenth state output and is used for modulus control of the SP8690. Clocking of the following CMOS variable divider is done from the –ve going edge of $Q_D$. The whole three modulus prescaler with its associated modulus control gating consists of an SP8690 followed by a TTL 74LS162 with two low power Schottky LS.TTL gates, G1 and G2, and is shown in part of Fig. 16. Typical wave forms are shown in Fig. 17.

Interfacing from the TTL output of 74162 to CMOS operating at +10 volts is accomplished with a two transistor saturating inverter.

## The Programmable 'A' and 'N' Counters

The 'A' and 'N' counters are made up of standard CMOS decades with some associated gating. The programming is split between the two divider chains, the 'N' counter taking the programming from 1MHz, upwards, the 'A' counter taking the 10kHz and 100kHz programme inputs.

The 'N' counter can be dismissed very simply. A quad decade (the CD4059) is used, its output driving the following phase detector and also starting the divide sequence of the 'A' counter.

It is in the 'A' counter that some complications arises. As we have previously mentioned, for a 3 modulus system ( ÷100/101/110) the 'A' counter must be divided into two decades, $A_1$ and $A_2$, which operate consecutively. In the scheme shown in Fig. 16 the decades used are MC14522 s. Divider $A_2$ is programmed from the 100kHz switch and $A_1$ from the 10kHz switch.

Operation is as follows. (All lower case letters refer to Fig. 16). If we assume that both $A_1$ and $A_2$ have reached their '0' state, then counting has been inhibited as 'f' and 'j' are both high and fed back to the clock inhibit. As soon as the 'N' counter reaches its '0' state 'd' goes high for 1 clock period. This gated with 'f' gives a load to counter $A_2$ which then starts to count down on the next clock pulse, $D_1$ is also loaded with a 1 on the same clock pulse. 'f' is also used as the ÷110 modulus control input. Consequently, the prescaler divides by 110 as long as 'f' is low (see Fig. 17 traces f, k). As soon as $A_2$ reaches the zero state again its own clock is inhibited by 'f' and a load pulse from gate G5 is driven into $A_1$. $A_2$ is not reloaded as 'a' is still low, 'N' not having reached its recognition state.

'j', $A_1$'s zero recognition output, is now low allowing $A_1$ to count down and causing the prescaler to divide by 101. $D_1$ is also loaded with a '0' as 'f' has gone to a '1'. This prevents further loads from reaching $A_1$. As soon as $A_1$ reaches its recognition state, 'j' goes high which causes the prescaler to divide by 100 and prevents $A_1$ counting further.

Both the 'A' counters are now at zero and not counting. This situation continues until the 'N' counter produces a further load on 'd' which starts the complete count cycle again.

An unfortunate characteristic of the MC14522 is its inability to operate correctly with a zero programme. Consequently a zero programme on '$A_1$' or '$A_2$' is detected and used to drive the Master reset input on the appropriate decade. Additional gating is required to ensure that a load is applied to '$A_1$', if '$A_2$' has a zero programme.

Finally, the composite modulus control input 'k' is resynchronised to the SP8690 clock by a Low Power Schottky J–K flip–flop ($D_2$). This resynchronisation is necessary because of the need to make the ÷10/11' divide by 11 for the whole of a period of the prescaler output, 'b'. If the 110 modulus control is not resynchronised the loop delay must be less than one output period of the ÷10/11 (in this case<77nsec). By resynchronising one whole period of 'b' is available to generate the modulus control and the resynchronising loop, consisting of the delay through the prescaler plus that in $D_2$, the resynchronising flip–flop. $D_2$ can be made very fast without too much power penalty by using low power Schottky TTL.

We need to know the worst case loop delay for the whole system so that we can determine the maximum operating speed:

The two critical delays are:

(1) 'clock in' to ÷110 control)'

(2) 'clock in' to ÷101 control)'

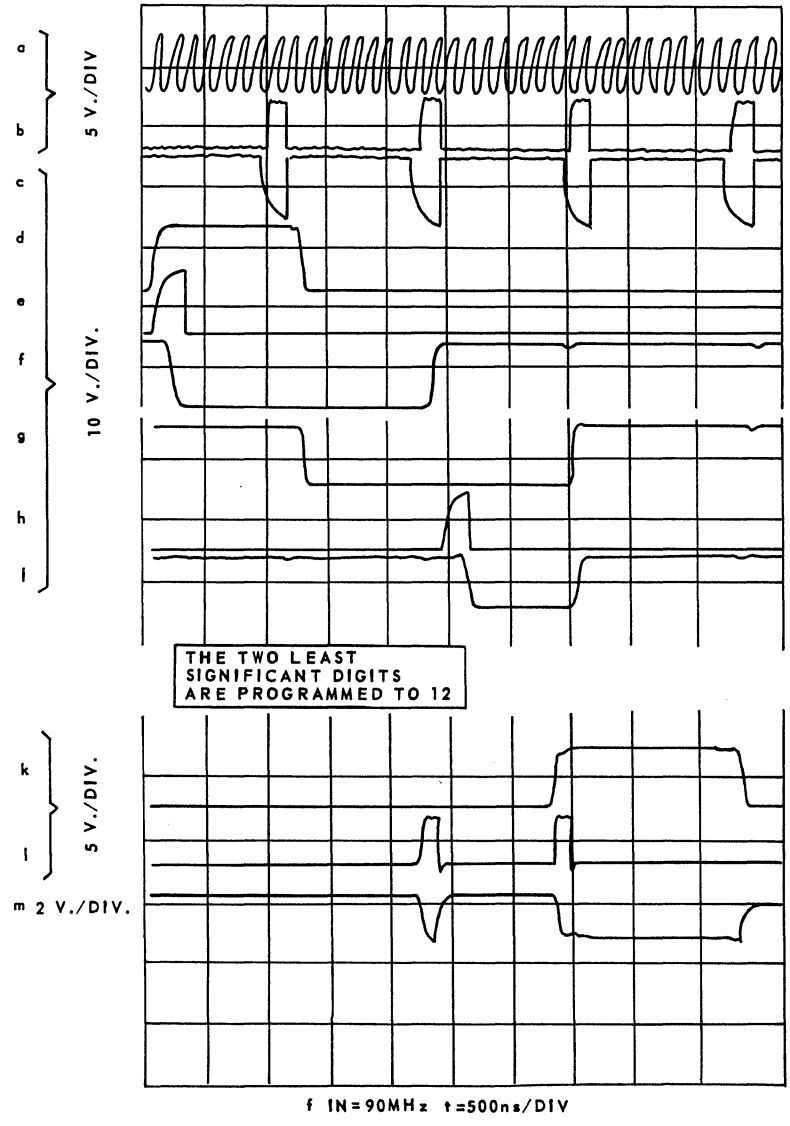



*Fig. 17 Waveforms of a ÷100/101/110.*

The loop delays for removal of the two modulus control signals, although equally important, can be seen to be less than delays '1' and '2' as they pass through fewer levels of gating.

| Item | Delay 1 | Delay 2 |
|---|---|---|
| Clock to Q SP8790 | 10nsec | 10nsec |
| Clock to Q4 74162 | 23nsec | 23nsec |
| TTL–CMOS Interface | 20nsec | 20nsec |
| Clock to recognition CD4059 | 200nsec | |
| Clock to recognition A2 | 300nsec | 300nsec |
| Load to recognition A1 | | 150nsec |
| 3 gate delays G1,G3,G4 | 180nsec | |
| 4 gate delays G1,G2,G4,G5 | | 240nsec |
| Total | 733nsec | 743nsec |

Delay 2 is the worst case and will give a maximum operating speed of 135MHz. This is close to the specified operating limit and if more leeway is desired 'A' series CMOS , with its tighter speed specifications should be used.

As in the UHF synthesiser divider, the use of just one Plessey SP800 series divider, in this case the low power ÷10/11 SP8690, has allowed the fabrication of an economical and extremely low power programmable divider. It is worthwhile pointing out that for solutions which do not require direct frequency programming or where a 25kHz channel spacing is required, then an SP8790÷4 two modulus control circuit should be used with the SP8690 to give a÷40/41 function for only 120mwatts. It is interesting to note that this divider could also be used in a 1.2GHz synthesiser merely by adding an SP8667 decade fixed prescaler to the front end.

## Conclusions

We have demonstrated in these two examples, how extremely high performance frequency dividers can be made with minimum of difficulty, by selecting the correct Plessey prescaler for the crucial front end position. The complete SP8000 range, as shown in Fig. 4 and 5, will allow an economical solution to almost any variable divider problem that a synthesiser divider designer could concoct. For those that are not covered by the SP8000 series, the Plessey Applications Group is readily available to help provide more unusual solutions.

As a footnote, Fig. 18 shows where Plessey Semiconductors can provide parts to complete a frequency synthesiser.

Not only are parts available for sophisticated solutions to the programmable divider, but integrated circuit technology, with its consequent benefits, have been applied by Plessey Semiconductors to every part of the syntheiser loop.

TABLE 2

COUNT SEQUENCE OF SN74162 TTL SYNCHRONOUS DECADE DIVDIER

| CLOCK | D | C | B | A |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |

RECOGNITION STATE FOR
– 1 SIDESTEP (100MHz DECADE)

RECOGNITION STATE FOR
–9 SIDESTEP (1MHz DECADE)

RECOGNITION STATE FOR
–7 SIDESTEP (10MHz DECADE

NORMAL RECOGNITION STATE

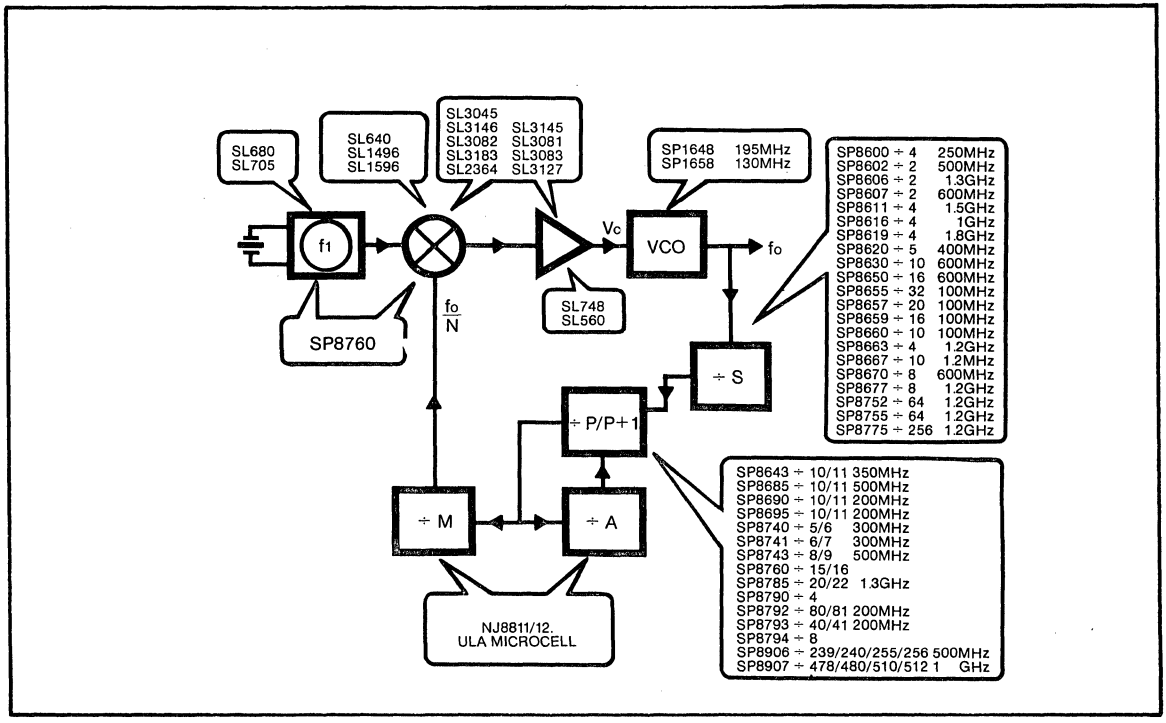



*Fig. 18 Plessey Semiconductors products in a typical synthesiser loop.*

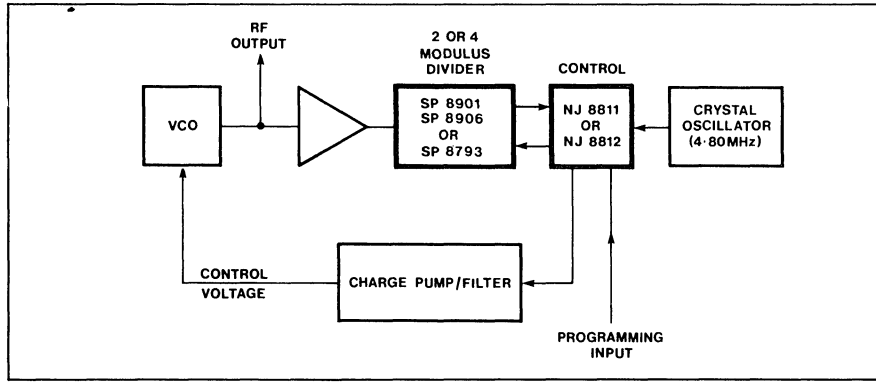
# 3. The Design of UHF and VHF Phase Locked Loops Using Four Modulus Dividers.

# INTRODUCTION

Frequency synthesis is now an accepted technique for providing large numbers of channels for radio-communications equipment. Until recently it was difficult to obtain integrated synthesiser circuits for other than limited frequency ranges. Plessey Semiconductors have fulfilled this need with two new ranges of circuits. These circuits are as follows:

| | |
|---|---|
| **GENERAL PURPOSE SYNTHESISER** | |
| **SP8901** | 1GHz four modulus divider (÷ 478/480/510/512), 5V/100mA supply |
| **SP8906** | 500MHz four modulus divider (÷ 239/240/255/256), 5V/75mA supply |
| **NJ8811** | N channel MOS control circuit, programmable dividers and phase/frequency comparator for use with either SP8901 or SP8906 to make a 'general purpose' synthesiser (5V/8mA supply) |
| **LOW POWER SYNTHESISER** | |
| **SP8793** | 225 MHz low power divider (÷ 40/41), 5V/4mA supply |
| **NJ8812** | N channel MOS control circuit, programmable dividers and phase/frequency comparator for use with the SP8793 to make a 'low power' synthesiser (5V/8mA supply) |

Many novel features are included in these circuits. Both 'general purpose' and 'low power' synthesisers using these circuits will provide channel spacings of 20, 25 and 30kHz, with submultiples. The circuits interface directly to ROM channel memories or to microprocessors and are easy to use. The following diagram shows the configuration and a few of the possible frequency ranges.




**Examples of continuous frequency range for channel spacing**

| Divider | Control | Power supply | Frequency range (MHz) | Channel spacing |
|---|---|---|---|---|
| **SP8901** | **NJ8811** | 5.0V* @ 108mA (147mA max.) | 38.4 to 1000 | 20kHz |
| | | | 48.0 to 1000 | 25kHz |
| | | | 57.6 to 1000 | 30kHz |
| **SP8906** | **NJ8811** | 5.0V @ 83mA (112mA max.) | 38.4 to 500 | 10kHz |
| | | | 48.0 to 500 | 12.5kHz |
| | | | 57.6 to 500 | 15kHz |
| **SP8793** | **NJ8812** | 5.0V @ 12mA (19mA max.) | 16.0 to 169.6 | 10kHz |
| | | | 20.0 to 212.0 | 12.5kHz |
| | | | 40.0 to 225 | 25kHz |

* When the SP8901 is operated with an input frequency above 900MHz one of the power supply pins should be connected to 6.8V instead of 5.0V.

## GENERAL PURPOSE SYNTHESISER

The NJ8811 is designed for use in phase locked loop frequency synthesisers. In these synthesisers, the voltage controlled oscillator (VCO) operates at the output frequency and the output frequency is divided down to a reference frequency. Another signal at this reference frequency is derived from the crystal controlled reference oscillator, and the divided VCO signal is compared at this frequency with the reference signal in a phase and frequency comparator. The output signal derived from this comparison consists of short pulses whose mark-space ratio is such that when the pulses are integrated, a DC level is obtained, which, when applied to the VCO, locks the loop by maintaining the VCO on frequency.

Simple division to the reference frequency in a fully programmable divider is limited to frequencies of about 50MHz and below, because of the difficulty of producing fully programmable dividers.

One answer to this is to use a prescaler as in Fig.1

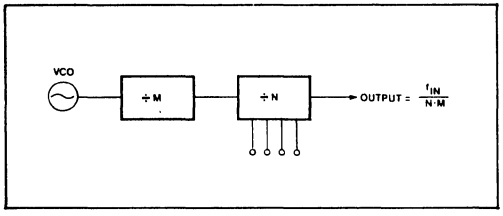



*Fig.1 Use of prescaler*

However, for any step in frequency Δf at the VCO, the change at the phase detector is Δf/N.M; if this step is caused by a change of M to M+1 then Δf must become Δf/N.(M+1) at the phase detector. Since the reference frequency is constant, the step at the VCO is therefore N times the reference frequency; this places limitations on the reference frequency value. For ease of filtering it is necessary to use as high a reference frequency as possible, preferably equal to the channel spacing.

To avoid the difficulties in simple prescaling two-modulus division may be used. In this system, the prescaler division ratio is altered from N to N+1: and while this is a very powerful method of achieving the necessary division, it is limited where very wide frequency ranges are required. This technique however may be applied by using four-modulus division as in Fig.2.

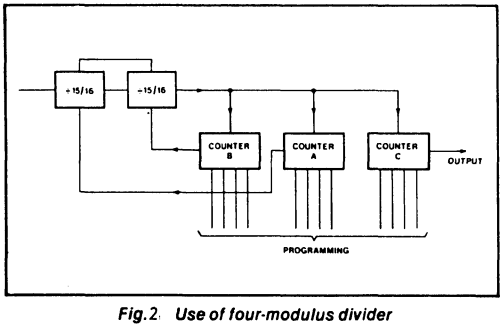



***Fig.2 Use of four-modulus divider***

In this system, the four-modulus counter can have a division ratio of 256, 255, 240 or 239. If the 'A' counter is programmed to a lower number than the 'B' counter, the system works as follows.

The 4 modulus prescaler divides by 239 'A' times, then by 240 until the 'B' counter is full and then by 256 until the 'C' counter is full. Thus the ratio is:

$$239A + 240(B - A) + 256(C - B)$$

If the 'A' counter is programmed to a higher number than the 'B' counter, then the system operation is:

Divide by 239 until the 'B' counter is full (i.e. 'B' times) then by 255 until the 'A' counter is full, then by 256 until the 'C' counter is full. The ratio is then:

$$239B + 255(A - B) + 256(C - A)$$

Both of these expressions simplify to:

$$256C - 16B - A$$

The limits are C = 16, B = 15, A = 16

and C = 271, B = 0, A = 1

Thus the minimum and maximum counts are 3840 and 69375. When the Range input is used on the NJ8811, this is modified such that the count is from 32568 to 101943.

A four-modulus divider for use to 500MHz is the SP8906, which interfaces directly with the NJ8811. The SP8901 has a ÷2 prescaler preceding the four-modulus divider, which thus enables direct synthesis at frequencies up to 1GHz to be attained.

**Phase Detector**

In the NJ8811, this circuit function is implemented by the use of two D type flip-flops. These drive 'open drain' output FETs, and if these are taken to $V_{CC}$ via resistors, waveforms as shown in Fig.3 may be expected.

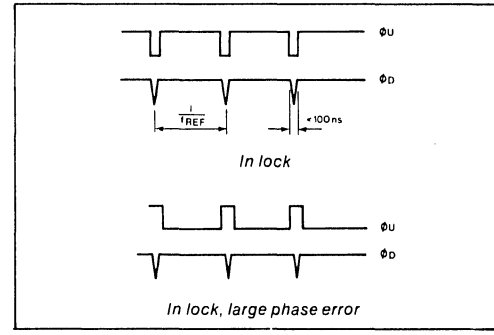



*Fig.3 Phase detector waveforms*

When out of lock, $Ø_D$ and $Ø_U$ have no definite phase relationship. These outputs, may be combined in a suitable circuit, as shown in Fig.4.

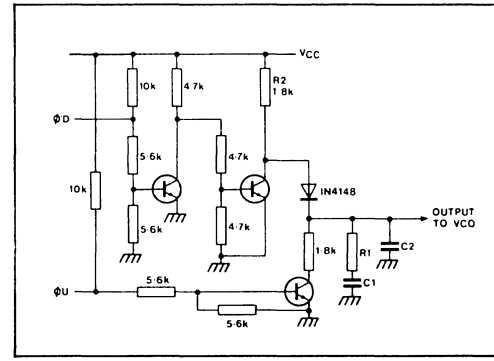



*Fig.4 Circuit for combining $Ø_D$ and $Ø_U$*

**Loop Filter Design**

A simple approach will provide a workable, but not necessarily optimum system. For more detailed methods, reference to one of the many textbooks is recommended. The following method provides a simple design.

1. Choose the loop natural frequency $\omega_n$. This frequency affects the settling time of the loop, and this settling time is, to a first order approximation, $10/\omega_n$, where $\omega_n$ is in radians per second.
2. Choose a value of damping factor to give adequate loop stability without excessive overshoot. A satisfactory value is 1.0, giving an overshoot of approximately 10%.
3. **Determine:**
   KV = VCO Gain in rad/s/V
   $= 2\pi$ x Hz/V
   where Hz/V is the deviation in Hz for 1 volt change on the control line.
   N = VCO frequency/Reference Frequency.
4. Choose $R_2$. For convenience, $4.7k\Omega > R_2 > 470\Omega$
   $$C_1 = \frac{KV}{2\pi N \omega_n^2 R_2}$$
5. $R_1 = D/\omega_n C_1$ where D is the damping factor.
6. $$C_2 = \frac{1}{15\omega_n R_1}$$

**Reference Oscillator Requirements**

Because the frequency synthesiser effectively multiplies the reference oscillator to the working frequency, any variations or inaccuracies in the reference oscillator appear at the output. For this reason, the accuracy of the reference oscillator must be no worse than that of the signal which it is required to synthesise, while the signal-to-noise ratio must be as high as possible. Incidental FM must be minimised.

**VCO Requirements**

The VCO should cover the frequency range desired with a suitable control line voltage swing. In addition, its power level and Q should be such as to maintain phase noise sidebands as low as is required. It is frequently found that the high impedance control line is very susceptible to picking up stray signals; screening and careful decoupling of the VCO and its supplies is often necessary. Buffering between the VCO and the prescaler is required to prevent VCO modulation from this source, and dual gate MOSFETS are very useful in this position.

**A Typical Synthesiser**

Fig.5. shows a frequency synthesiser using the SP8906 and NJ8811.

The Frequency synthesiser heart is the VCO. This is frequently a proprietary item and thus is subject to many design variations. In general, the VCO should be designed for low noise and the output should be well buffered. The VCO's used in the frequency synthesiser were designed specifically for the marine VHF band. In general, the main requirement is that the VCO should cover the frequency range required with a control line voltage variation from approximately 1 to 7 volts, positive with respect to earth. For transceiver use, where a frequency change is required between receive and transmit, the VCO is switched lower frequency by about 10 MHz by means of a diode, which in transmit, is used as a modulation diode.

The VCO output is amplified in an SL560, which is a wideband, low noise amplifier. This stage is operated such that ii is operating in a limiting mode, which removes any variations of output with frequency from the VCO. The output is at about + 2dBm in 50 ohms, and is also applied to the input of the dual gate MOSFET, Q1, which provides high reverse isolation between the SP8906 and the synthesiser output. The drain of Q1 is capacitively coupled to the SP8906 input, and up to this point short leads and the usual standards of construction for VHF are required.

The supply line to the SP8906 is fed through a small RF Choke (approx 6 turns 3mm diameter) to assist isolation and stability. The output of the SP8906 feeds the NJ8811 FREQ input pin.

The reference oscillator used is 4.800 MHz. This allows a multiplicity of channel spacings, and these are listed in Table 1, together with the linking required for their definition. The oscillator uses a single transistor, Q5 and may be set exactly on frequency by means of the trimmer capacitor.

The outputs from the NJ8811 are open drain MOSFET outputs, and these drive the charge pump circuitry consisting of Q2, Q3 and Q4, which vary the voltage appearing across the loop filter as required. The loop filter is R1, C2 and C2, with R2 and C3 giving an extra pole in the response. The filter may be changed as necessary to meet various requirements: with the values given the reference frequency sidebands are more than 90 dB down and the lock up time is of the order of 100 mSecs.

Modulation is provided by the SL6043, which is a programmable quad. op. amp. Three sections are used respectively as microphone amplifier, clipper, and active low pass filter, while the fourth section provides switching of the VCO modulation diode and also depowers the first three sections on receive, thus preventing modulation of the local oscillator from the microphone.

The synthesiser is designed to work from a nominal 12v supply, which is regulated at 8v and 5v by monolithic regulators.

An LED lights when the synthesiser is out of lock, and this can be used to inhibit the transmitter as required.

Preset controls are provided for MIC GAIN and DEVIATION. These are set up as follows:

1. Feed a signal at 1 KHz and 30 mV RMS P.D. into the MIC INPUT terminals
2. Adjust the DEVIATION control for 5KHz deviation.
3. Decrease the input by 20 dB.
4. Adjust the GAIN control for 3 KHz deviation.
5. Increase the input by 20 dB and check that the deviation does not exceed 5 KHz.

**TABLE 1**
**CHANNEL SPACING PROGRAMMING**

| PinH/PinD | Pin F | O/C | Pin C | Pin E |
|---|---|---|---|---|
| Pin K | 20 | 10 | 5 | 2.5 |
| O/C | 25 | 12.5 | 6.25 | 3.125 |
| Pin G | 30 | 15 | 7.5 | 3.75 |
| Pin J | 37.5 | 18.75 | 9.375 | 4.6875 |

*Table 1 Channel Spacing Programming*

By linking the pins referred to on the circuit diagram as per the table 1, the above channel spacings may be obtained when a 4.800 MHz crystal is used.

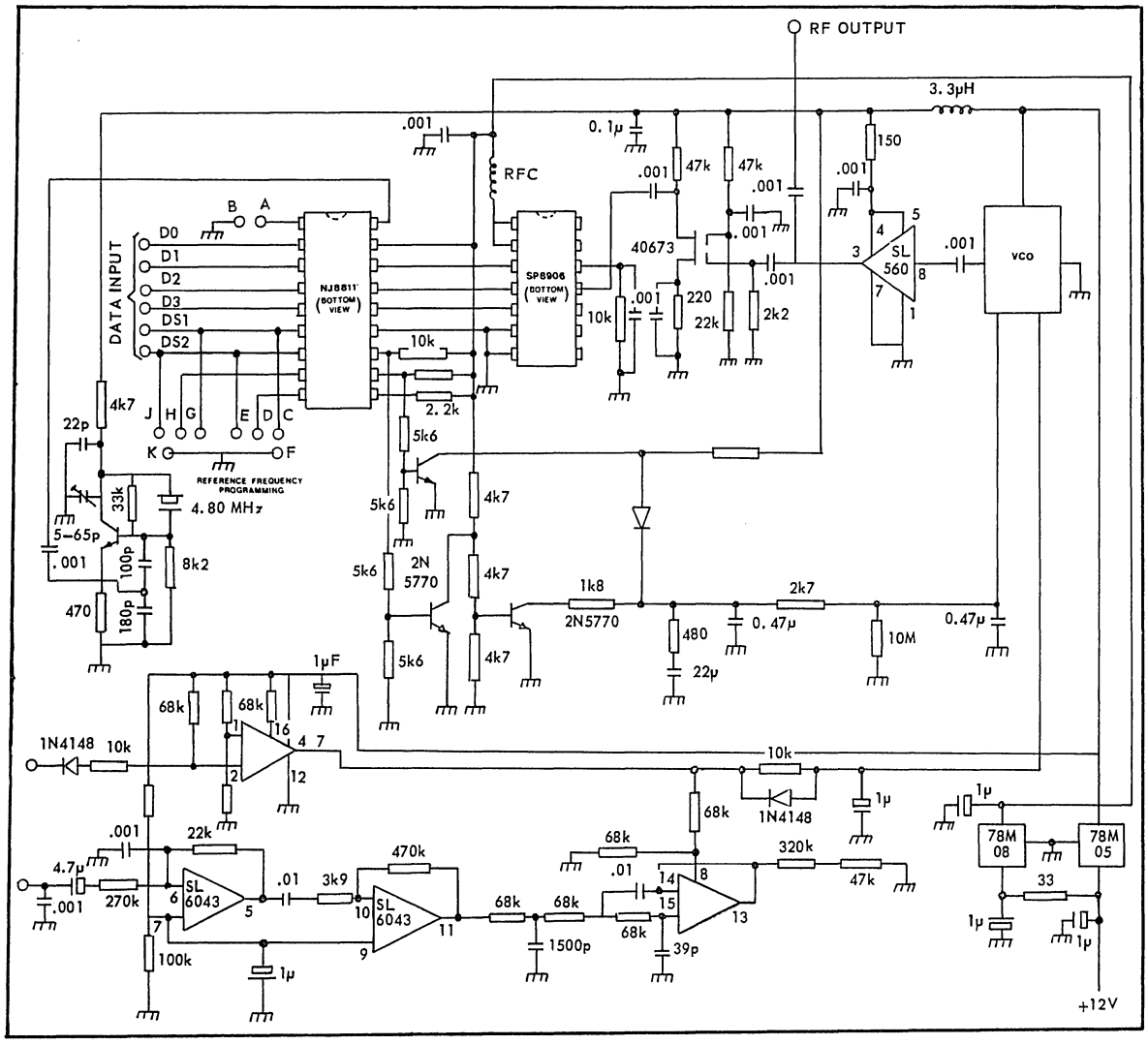



*Fig.5 Frequency synthesiser using NJ8811 and SP8906*

## PROGRAMMING

### 1) HARDWARE

The NJ8811 requires programming with 4 four bit binary words. These words are read into the device under the control of the DS1 and DS2 pins, on which appears the reference frequency divided by 4096. The order in which the information is read in is shown in Fig. 6. If for any reason it is desired to prevent the signals appearing at these pins, or to latch the information in the NJ8811 then these pins may be taken to logic 0. This logic 0 must be applied at the right point in the sequence, as shown in Fig 6.

There are a number of ways in which the 4 words can be produced. One of the simplest is the Binary Universal Programming Board, of which the circuit diagram is shown in Fig. 7. This uses 74LS153 multiplexers to act in effect as a 4p 4w switch selecting the setting of the 16 individual switches in 4 bits at a time. A PROM may be substituted, and a PROM such as a DM8574 will provide 32 transmit and 32 receive channels. It must be remembered that in a superheterodyne transceiver, the synthesised local oscillator must be offset by the IF from the channel frequency: this requires a different programme number.

Because of the simple method of programming the NJ8811, it is very simple to interface to a microprocessor, although such applications are outside the scope of this note.

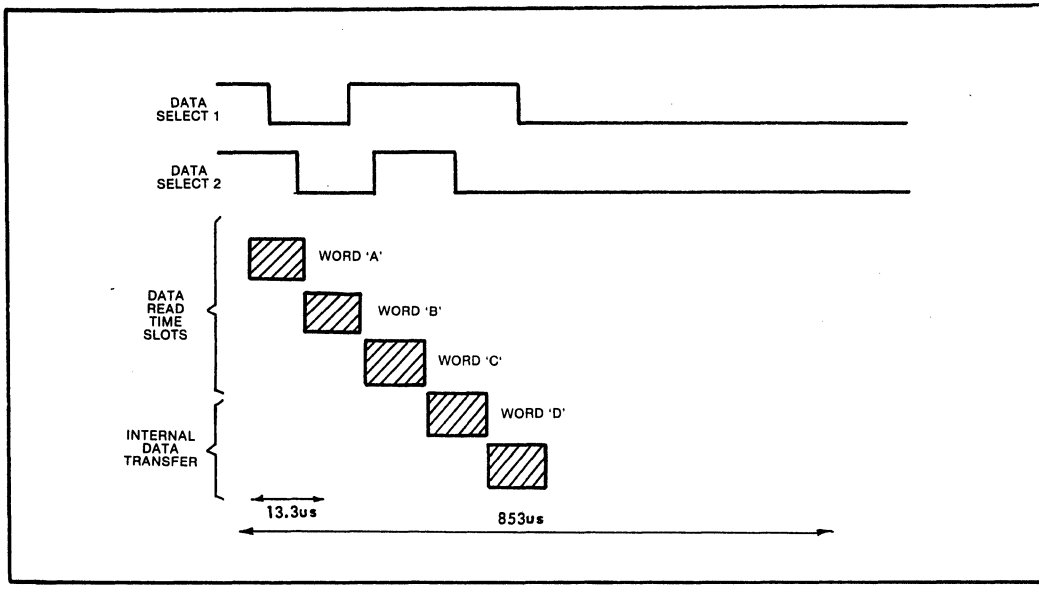



*Fig. 6*

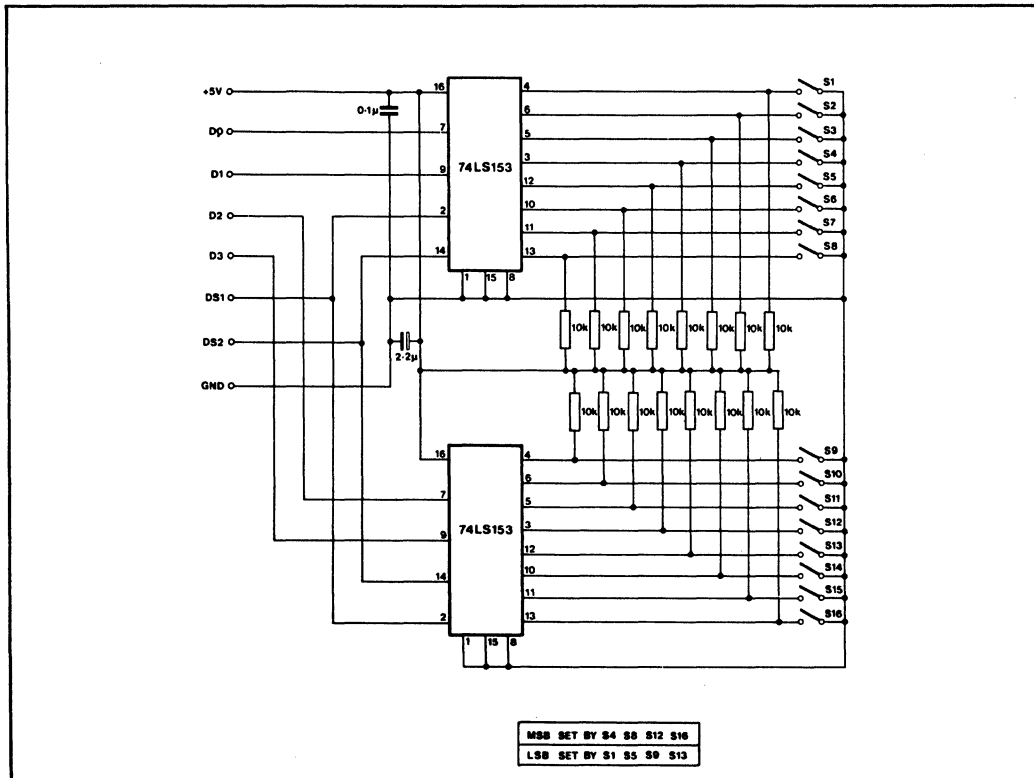



*Fig. 7 Programming board*

## 2) SOFTWARE

See section on calculating division number in data sheet.

## THE MODULATOR

The modulator uses the SL6043 Quad Operational Amplifier. This circuit block is very simple, comprising an amplifier, a limiter and a multi-section low pass filter. The fourth section of the Operational Amplifier is used as an inverter, producing a "1" at pin 3 when the PTT line is earthed. This high level biases the other three sections of the SK6043, and also reverse biases a switching diode in the VCO. This switching diode is forward biased in receive, thus lowering the VCO frequency range by about 10 MHz, while in transmit, it acts as a variable capacity diode and provides modulation. The method of setting up the Deviation and Clipping Level has already been covered.

Fig. 8 shows the modulation-frequency response for the circuit. Although designed specifically for use in this synthesiser, other applications of this circuit are possible.

Because of the arrangements of the SL6043 in a "3 + 1" architectural style, the AF amplifier section is usefully depowered on receive. This reduces noise modulated onto the receiver local oscillator, which would lead to a degradation of the received signal to noise ratio. The signal to noise ratio of transmit exceeds the CEPT requirements of 40dB. However, the rigidity of the VCO is an important parameter: a poor VCO can well have noise components under vibration conditions such that it is difficult for the phase locked loop to clean up the signal to a satisfactory level. To this end, the prototype used a printed inductor, and was potted in a suitable polyurethane resin. This construction produced a synthesizer with adequate performance for use under mobile conditions in an SSB equipment operating at around 150 MHz.

## LOCK UP TIME

The lock up time of the synthesizer is dependent upon the loop bandwidth and the reference frequency. In general, it may be assumed that the loop will require some 40 or 50 cycles of reference frequency in order to acheive lock. And at a 25 KHz channel spacing this represents some 1.6 to 2 mSecs. In order that the reference frequency sidebands occasioned by reference frequency components appearing on the control line to the VCO are sufficiently suppressed, the loop filter requires a suitable cut off frequency. With the values given, the lock up time is around 100 mSec, and the reference frequency sidebands are greater than 100 dB down relative to the carrier. The loop cut off frequency can be varied as required, but where modulation is required, the phase shifts round the loop filter can lead to distortion appearing if the damping factor or loop cut off frequency are incorrect. These parameters are set by the 470 ohm, 2K7, 0.47 and 22 mF capacitors, and 1K8 resistors associated with the charge pump circuitry.

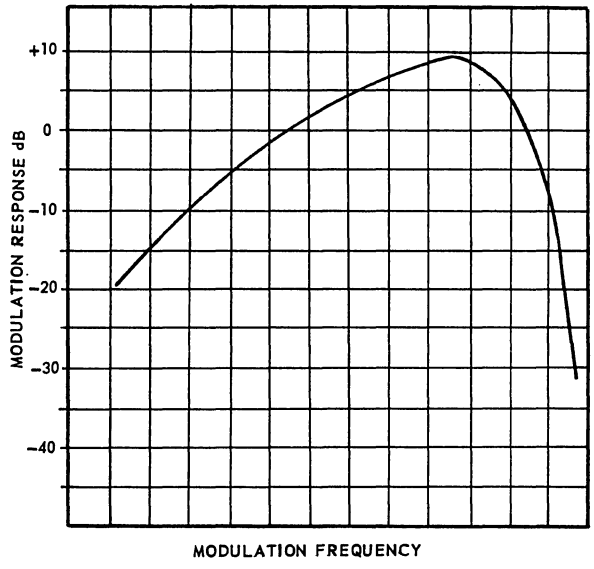


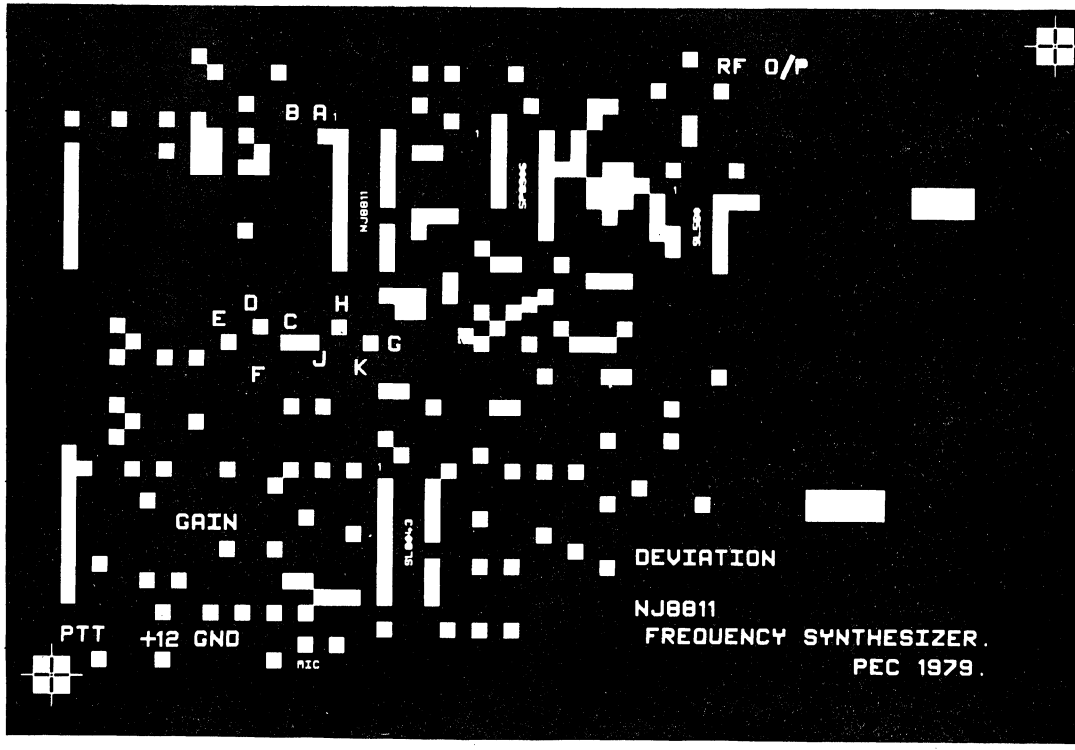

*Fig. 8*

## PRINTED CIRCUIT BOARD LAYOUTS

Figs. 9 and 10 show the masters for the P.C. Boards used for the synthesizer and the universal programming board. The programming board is 6.05" across the diagonal joining the registration marks and is 4.5" x 4". The synthesizer board is 6.3" x 4" and is 9.45" across diagonals.

Fig. 11 shows the component layout diagram for the synthesizer board. The VCO used is mounted in a 3" x 1.4" box, and the connections are then brought out on a 0.1" matrix for connection to the synthesizer board.

This note describes a VHF synthesizer capable of meeting the needs of many land and marine mobile applications. Its FM modulation capabilities meet the revelant international requirements, while its spurious outputs exceed these specifications. The design is highly flexible in its programming capability and its ease of interfacing with memories and other programming systems.


RF O/P
B A1
E D C H
G
F J K
GAIN
DEVIATION
PTT +12 GND
MIC
NJ8811
FREQUENCY SYNTHESIZER.
PEC 1979.

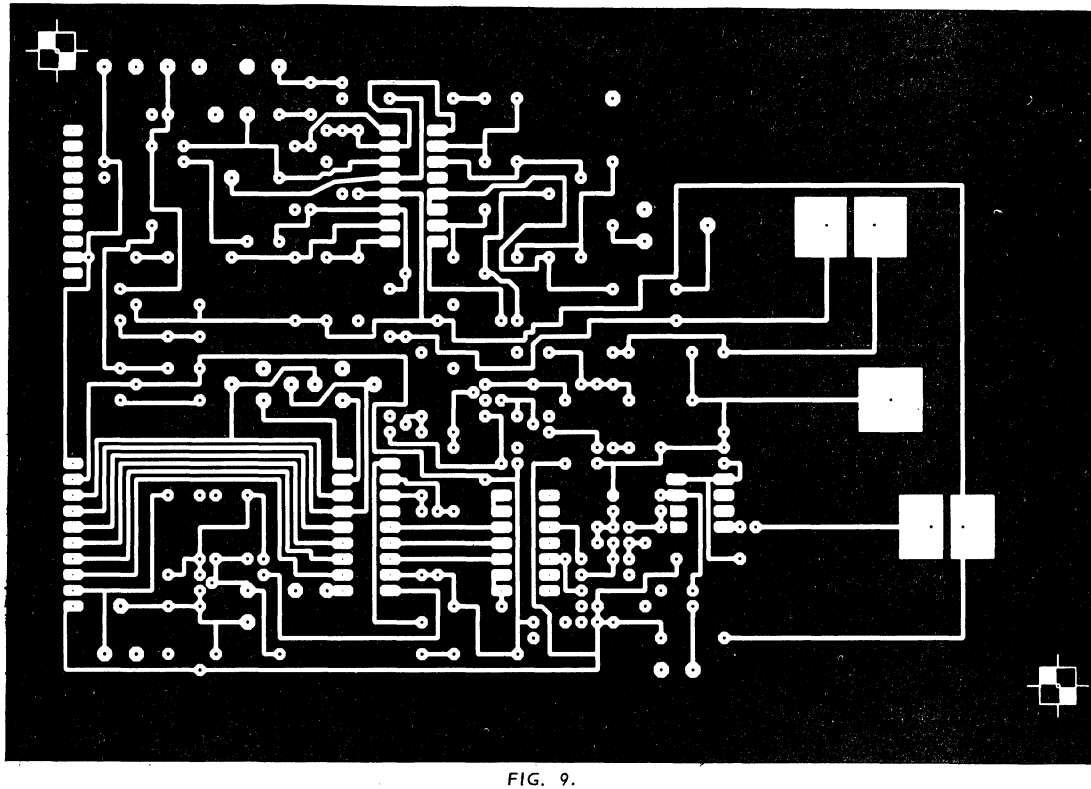
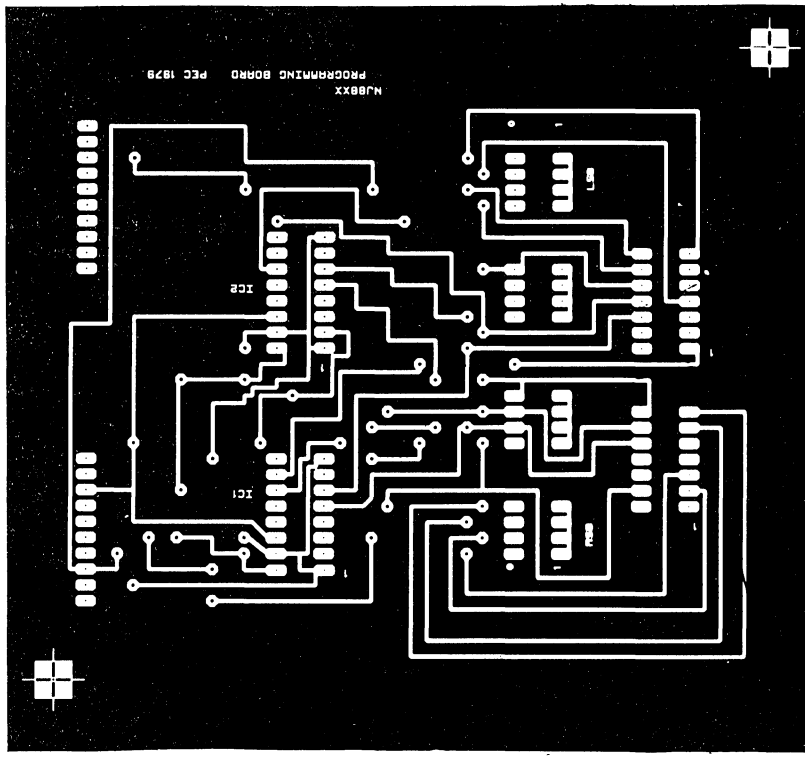




FIG. 9.



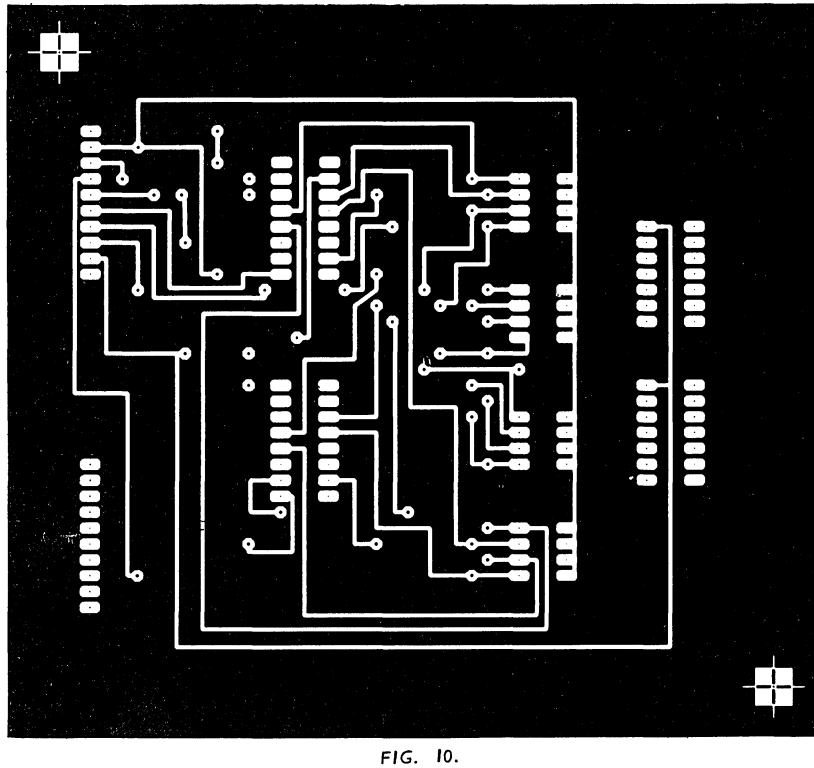



FIG. 10.

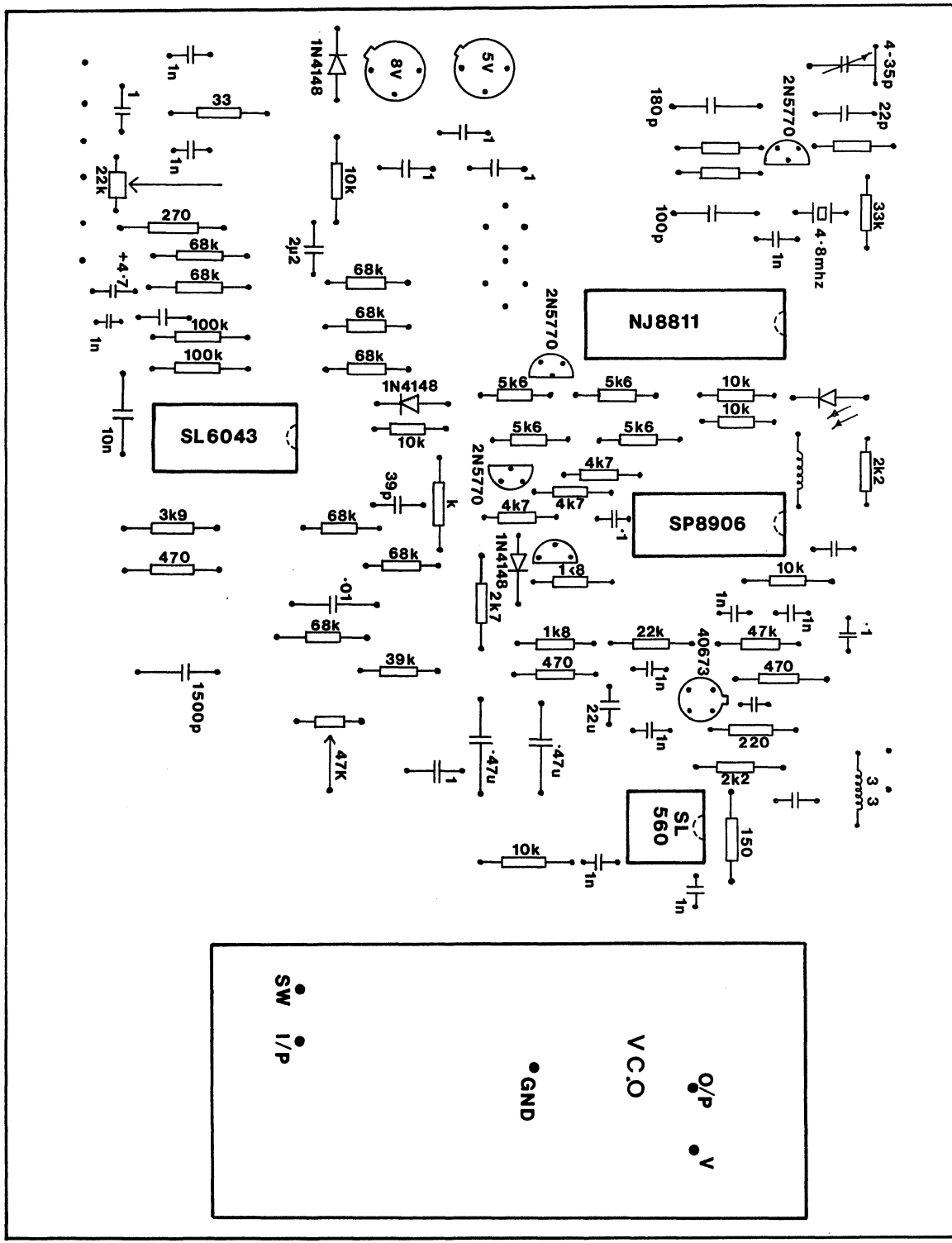

4-35p
22p
2N5770
180p
33k
100p
4·8mhz
1n
NJ8811
2N5770
5k6
10k
2k2
SP8906
4k7
·1
1k8
2k7
1N4148
40673
47k
470
220
2k2
150
SL 560
10k
22u
·47u
1500p
39k
68k
·01
3k9
470
39p
SL6043
10n
100k
+4·7
270
22k
33
1
2µ2
8V
5V
1N4148
SW I/P
GND
V C.O
O/P
V

FIG. 11.

## LOW POWER SYNTHESISER

The NJ8812 is designed for use in phase locked loop frequency synthesisers. In these synthesisers, the voltage controlled oscillator (VCO) operates at the output frequency and the output frequency is divided down to a reference frequency. Another signal at this reference frequency is derived from the crystal controlled reference oscillator, and the divided VCO signal is compared at this frequency with the reference signal in a phase and frequency comparator. The output signal derived from this comparison consists of short pulses whose mark-space ratio is such that when the pulses are integrated, a DC level is obtained, which, when applied to the VCO, locks the loop by maintaining the VCO on-frequency.

Simple division to the reference frequency in a fully programmable divider is limited to frequencies of about 50MHz and below, because of the difficulty of producing fully programmable dividers. However, a two-modulus divider which divides by N and N+1 may be easily made. A system as shown in Fig.1 then provides for the programmable division to be done at lower frequencies.

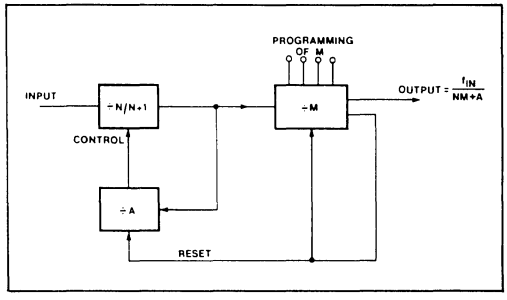



*Fig. 1 2-modulus counter*

The system works as follows:

The two-modulus counter divides by N+1 until counter A is full. The two-modulus stage then divides by N until the M counter is full. The resultant division ratio is NM+A.

In the NJ8812, the value of M is set to between 40 and 295, while A is programmed between 0 and 39. The full scope of the NJ8812 in a synthesiser is achieved using a ÷40/41, such as the SP8793, and under these conditions, the division ratio is from 1600 to 11839. By using the Range input, the M counter programme is changed such that the division ratio becomes 6720 to 16959.

The reference frequency is derived from a 4.8MHz crystal by a programmed divider. This divider is programmed by the FA and FB inputs: these may be tied to $V_{CC}$ (logic '1'), Ground (logic '0') or to DS1 and DS2, depending upon the reference frequency required. In general the reference frequency is made equal to the channel spacing, as the higher the reference frequency, the easier it is to filter the control line to the VCO to prevent spurious sidebands at reference frequency appearing on the output.

**Phase Detector**

In the NJ8812, this circuit function is implemented by the use of two D type flip-flops. These drive 'open drain' output FETs, and if these are taken to $V_{CC}$ via resistors, waveforms as shown in Fig.2 may be expected.

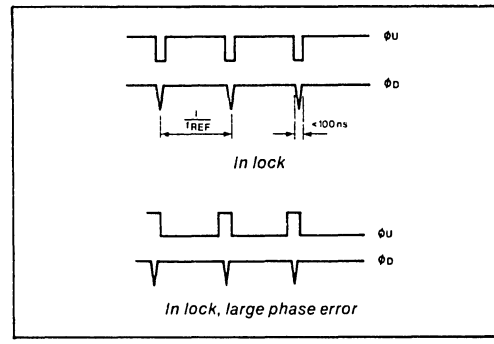



*Fig.2 Phase detector waveforms*

When out of lock, $Ø_D$ and $Ø_U$ have no definite phase relationship. These outputs may be combined in a suitable circuit, as shown in Fig. 3.

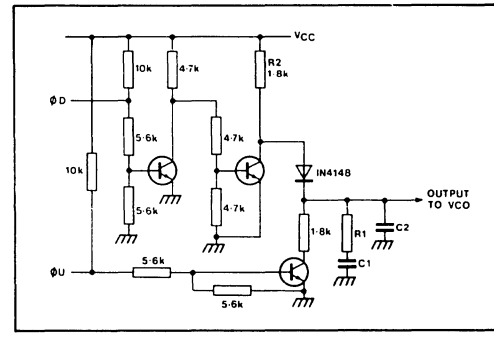



*Fig. 3 Circuit for combining $Ø_D$ and $Ø_U$*

**Loop Filter Design**

A simple approach will provide a workable, but not necessarily optimum system. For more detailed methods, reference to one of the many textbooks is recommended. The following method provides a simple design.

1. Choose the loop natural frequency $\omega_n$. This frequency affects the settling time of the loop, and this settling time is, to a first order approximation, $10/\omega_n$, where $\omega_n$ is in radians per second.
2. Choose a value of damping factor to give adequate loop stability without excessive overshoot. A satisfactory value is 1.0, giving an overshoot of approximately 10%.
3. **Determine:**
   KV = VCO Gain in rad/s/V
   $= 2\pi \times$ Hz/V
   where Hz/V is the deviation in Hz for 1 volt change on the control line.
   N = VCO frequency/Reference Frequency.
4. Choose $R_2$. For convenience, $4.7k\Omega > R_2 > 470\Omega$
   $C_1 = \dfrac{KV}{2\pi N \omega_n^2 R_2}$
5. $R_1 = D/\omega_n C_1$ where D is the damping factor.
6. $C_2 = \dfrac{1}{15\omega_n R_1}$

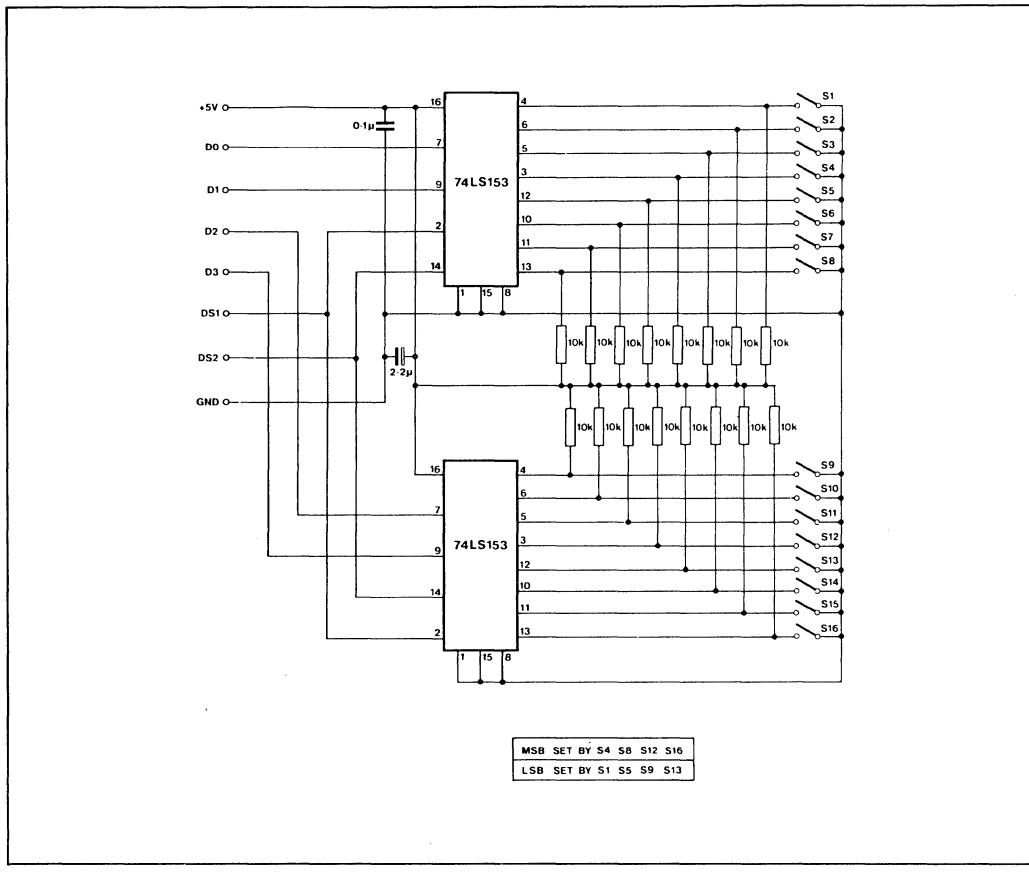



*Fig. 4 Programming board*

**Reference Oscillator Requirements**

Because the frequency synthesiser effectively multiplies the reference oscillator to the working frequency, any variations or inaccuracies in the reference oscillator appear at the output. For this reason, the accuracy of the reference oscillator must be no worse than that of the signal which it is required to synthesise, while the signal-to-noise ratio must be as high as possible. Incidental FM must be minimised.

**VCO Requirements**

The VCO should cover the frequency range desired with a suitable control line voltage swing. In addition, its power level and Q should be such as to maintain phase noise sidebands as low as is required. It is frequently found that the high impedance control line is very susceptible to picking up stray signals; screening and careful decoupling of the VCO and its supplies is often necessary. Buffering between the VCO and the prescaler is required to prevent VCO modulation from this source, and dual gate MOSFETS are very useful in this position.

**A Typical Synthesiser**

Fig. 5 shows a typical frequency synthesiser using the NJ8812 and SP8793. Programming is from the binary programming board of Fig. 4 or from a suitably programmed PROM or ROM. It should be noted that the binary programming board produces four 4-bit words, and therefore, two of the bits are redundant (see Programming the NJ8812).

The synthesiser of Fig. 5 uses a 40673 or similar dual gate MOSFET as a buffer prior to the SP8793 divider. The three 2N5770 transistors provide a charge pump circuit, and the fourth a crystal oscillator. This synthesiser draws some 25 mA maximum, excluding the VCO and the programming system, and further development could well reduce the current appreciably. If modulation is required, this may be applied to the control line, provided that the peak deviation is not such as to drive the loop out of lock.

The connection of an LED from pin 10 of the NJ8812 to 5V via a 2.2kΩ resistor will provide an indication of lock, the lamp being alight when the loop is unlocked.

FA, FB and the range pin are connected according to the requirements of frequency spacing and operating frequency.

Performance, in terms of spurious sidebands and noise, depends upon construction and design of the VCO and PC board, and good RF practice should be followed with regard to these components. In particular, attention should be paid to the VCO screening.

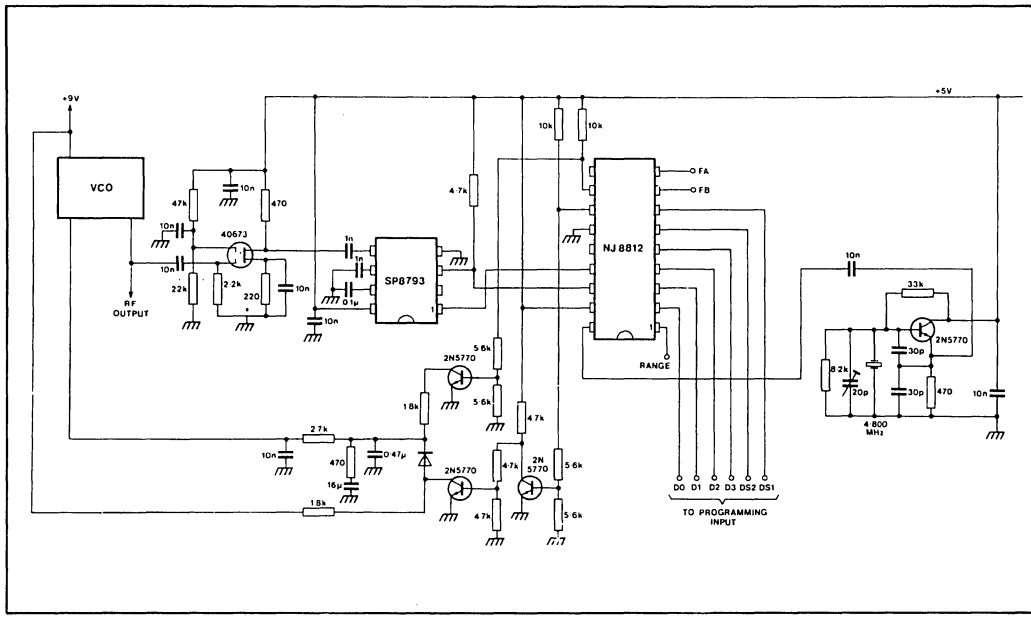



*Fig.5 Frequency synthesiser using NJ8812 and SP8793*

## Using a calculator to find the division numbers of the NJ8811 and NJ8812

### Programming the NJ8811

The NJ8811 requires a sixteen bit-binary address to program the division number and hence give the required frequency output in a phase locked loop configuration. The address is organised as four words of four bits each and may therefore be conveniently expressed in hexadecimal notation as shown in Table 1.

| 4 Bit Binary Code | | | | Hexadecimal | Decimal Equivalent |
|---|---|---|---|---|---|
| D | C | B | A | | |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 | 2 |
| 0 | 0 | 1 | 1 | 3 | 3 |
| 0 | 1 | 0 | 0 | 4 | 4 |
| 0 | 1 | 0 | 1 | 5 | 5 |
| 0 | 1 | 1 | 0 | 6 | 6 |
| 0 | 1 | 1 | 1 | 7 | 7 |
| 1 | 0 | 0 | 0 | 8 | 8 |
| 1 | 0 | 0 | 1 | 9 | 9 |
| 1 | 0 | 1 | 0 | A | 10 |
| 1 | 0 | 1 | 1 | B | 11 |
| 1 | 1 | 0 | 0 | C | 12 |
| 1 | 1 | 0 | 1 | D | 13 |
| 1 | 1 | 1 | 0 | E | 14 |
| 1 | 1 | 1 | 1 | F | 15 |

Table 1 Binary-Hexadecimal-Decimal

The program number may be calculated using the following equation:

$$\text{Program Number } N = \frac{(1000 \times f)}{C} - R$$

where f = Frequency of the VCO in MHz
C = Channel spacing in kHz
R = Range number (R = 3840, Range I/P = '1')
(R = 36608, Range I/P = '0')

The program number may be converted into decimal equivalent by using the following procedure. The above Table 1 will then give the hexadecimal or binary code.

**Using a standard calculator:**

Enter in the number N
Divide by 4096
Write down the number before the decimal point
Subtract the number before the decimal point
Multiply by 16
Write down the number before the decimal point
Subtract the number before the decimal point
Multiply by 16
Write down the number before the decimal point
Subtract the number before the decimal point
Multiply by 16
Write down the nearest whole number to the one displayed
You will then have an answer in the form 8, 11, 14, 5
This can be converted to hexadecimal using Table 1 8 B E 5
or to binary 1000, 1011, 1110, 0101

If a Hewlett Packard 25 or equivalent calculator is available the following program (Table 2) may be used to obtain the decimal equivalent directly from the frequency and channel spacing.

| Program Step | Instruction | Display |
|---|---|---|
| 00 | | |
| 01 | ÷ | 71 |
| 02 | 1 | 01 |
| 03 | 0 | 00 |
| 04 | 0 | 00 |
| 05 | 0 | 00 |
| 06 | X | 61 |
| 07 | RANGE = 1: 0 3 / 3 6 8 4 0 0 8 / RANGE = 0: 0 3 / 8 6 4 0 0 8 | 00/03 |
| 08 | | 03/06 |
| 09 | | 08/06 |
| 10 | | 04/00 |
| 11 | | 00/08 |
| 12 | - | 41 |
| 13 | 4 | 04 |
| 14 | 0 | 00 |
| 15 | 9 | 09 |
| 16 | 6 | 06 |
| 17 | ÷ | 71 |
| 18 | STO 0 | 23 00 |
| 19 | fFIX 0 | 14 11 00 |
| 20 | 3 | 03 |
| 21 | STO 1 | 23 01 |
| 22 | 1 | 01 |
| 23 | 6 | 06 |
| 24 | STO 2 | 23 02 |

| Program Step | Instruction | Display |
|---|---|---|
| 25 | RCL 0 | 24 00 |
| 26 | fINT | 14 01 |
| 27 | R/S | 74 |
| 28 | RCL 0 | 24 00 |
| 29 | gFRAC | 15 01 |
| 30 | RCL 2 | 24 02 |
| 31 | X | 61 |
| 32 | STO 0 | 23 00 |
| 33 | RCL 1 | 24 01 |
| 34 | 1 | 01 |
| 35 | - | 41 |
| 36 | STO 1 | 23 01 |
| 37 | gx=0 | 15 71 |
| 38 | GTO 25 | 13 25 |
| 39 | RCL 0 | 24 00 |
| 40 | . | 73 |
| 41 | 5 | 05 |
| 42 | + | 51 |
| 43 | fINT | 14 01 |
| 44 | fPAUSE | 14 74 |
| 45 | fPAUSE | 14 74 |
| 46 | fPAUSE | 14 74 |
| 47 | fPAUSE | 14 74 |
| 48 | GTO 00 | 13 00 |

Table 2 HP-25 program for NJ8811 decimal equivalents

**To run the program, enter:**

fPRGM (1st time only)
Frequency (in MHz)
Channel spacing (in KHz)
R/S
(1st answer displayed)
R/S
(2nd answer displayed)
R/S
(3rd answer displayed)
R/S
(4th answer displayed and flashes)

**Programming the NJ8812**

The NJ8812 requires a fourteen bit binary address to program the division number and hence give the required frequency output in a phase locked loop configuration with the SP8793. The address is organised as three words of four bits each and one word of two bits.

The program number may be calculated using the following equation.

$$\text{Program Number } N = \frac{(1000 \times f)}{C} - R$$

where f = Frequency in MHz (of the VCO)
C = Channel spacing in KHz
R = Range number (R = 1600 range = 1)
(R = 6720 range = 0)

The program number may be converted into Decimal equivalent by using the following procedure.

**Using a standard Calculator:**

Enter in the number N
Divide by 640
Write down the number before the decimal point.
Subtract the number before the decimal point.
Multiply by 16
Write down the number before the decimal point.
Subtract the number before the decimal point.
Multiply by 40
Write down the nearest whole number to the one displayed.
You will then have an answer in the form:
8, 11, 30

This can now be converted to Binary noting that the third Decimal number gives the final six bits of Binary.

i.e. 1000, 1011, 011110

If a Hewlett Packard 25 or equivalent calculator is available the following program may be used to obtain the Decimal equivalent directly from the frequency and channel spacing.

| Program Step | Instruction | Display |
|---|---|---|
| 00 | | |
| 01 | ÷ | 71 |
| 02 | 1 | 01 |
| 03 | 0 | 00 |
| 04 | 0 | 00 |
| 05 | 0 | 00 |
| 06 | X | 61 |
| 07 | RANGE = 1 16 RANGE = 0 | 01/06 |
| 08 | 67 | 06/07 |
| 09 | 0.2 | 00/02 |
| 10 | 100 | 00/00 |

| Program Step | Instruction | Display |
|---|---|---|
| 11 | ÷ | 41 |
| 12 | 6 | 06 |
| 13 | 4 | 04 |
| 14 | 0 | 00 |
| 15 | ÷ | 71 |
| 16 | STO 1 | 23 01 |
| 17 | fFIX 0 | 14 11 00 |
| 18 | fINT | 14 01 |
| 19 | R/S | 74 |
| 20 | RCL 1 | 24 01 |
| 21 | gFRAC | 15 01 |
| 22 | 1 | 01 |

| Program Step | Instruction | Display |
|---|---|---|
| 23 | 6 | 06 |
| 24 | X | 61 |
| 25 | STO 2 | 23 02 |
| 26 | fINT | 14 01 |
| 27 | R/S | 74 |
| 28 | RCL 2 | 24 02 |
| 29 | gFRAC | 15 01 |
| 30 | 4 | 04 |
| 31 | 0 | 00 |
| 32 | X | 61 |
| 33 | . | 73 |
| 34 | 5 | 05 |
| 35 | + | 51 |
| 36 | fINT | 14 01 |
| 37 | fPAUSE | 14 74 |
| 38 | fPAUSE | 14 74 |
| 39 | fPAUSE | 14 74 |
| 40 | fPAUSE | 14 74 |
| 41 | fPAUSE | 14 74 |
| 42 | fPAUSE | 14 74 |
| 43 | GTO 00 | 13 00 |

Table 3 HP-25 program for NJ8812 decimal equivalents

**To run the program, enter:**

fPRGM (1st time only)
Frequency (in MHz)
Channel spacing (in KHz)
R/S
(1st answer displayed)
R/S
(2nd answer displayed)
R/S
(3rd answer displayed and flashes)

# 4. Practical Solutions to VHF Synthesis.

# VHF SYNTHESISER 108-174 MHZ

This application note will describe a phase Lock Loop Synthesiser which covers the frequency range between the top of the FM Broadcast band at 108 MHZ and the start of the, VHF High, television band at 174 MHZ - The synthesiser has a channel spacing of 25 KHZ. Applications include the Marine UHF Radio Telephone, Weather Broadcasts, Air Traffic Control and the Amateur 2 Meter Band.

**Circuit Description-See Fig. 1.**

**Section 1.**

The voltage controlled oscillator is a Plessey SP1648. The SP1648 is an emitted-coupled oscillator with outputs compatible with the ECL 111 Logic Family. Using varactor diodes in tank circuit and varying the voltage applied to them we can vary the oscillator frequency output over our required range.

**Section 2.**

A Plessey SL1521 wideband amplified is used to provide isolation between the VCO and the digital dividers.

The main use of the SL1521 is to help prevent the divider switching noise from getting back to the VCO output.

**Section 3.**

The prescaler is a Plessey Low Power SP8690 divide by 10/11 UHF counter. This counter and a Plessey SP8790 are connected to form a divide by 40/41 counter with an operating frequency in excess of 200 MHZ. The divide by 40/41 control is TTL compatible so it can be tied directly to the count inhibit line of the "A" dividers.

**Section 4.**

The open collector output of the SP8790 is connected to a 74LS04 inverter. The inverter is used to invert and buffer the clock signal.

**Section 5.**

By the use of thumbwheel switches with BCD complement outputs the switches can be wired directly to the parallel load inputs of the programmable dividers. The up-down counters are standard 75LS168 and 74LS169 as used in the down count mode. When the count in U10, U9 and U8 has reached 001, the load input is enabled. At the next clock the BCD switched information is parallel loaded into the dividers.

**Section 6.**

The Plessey SP8760 contains the reference oscillator, a fixed divide by 4 counter, a variable modulus divide by 15/16 counter and a phase comparator.

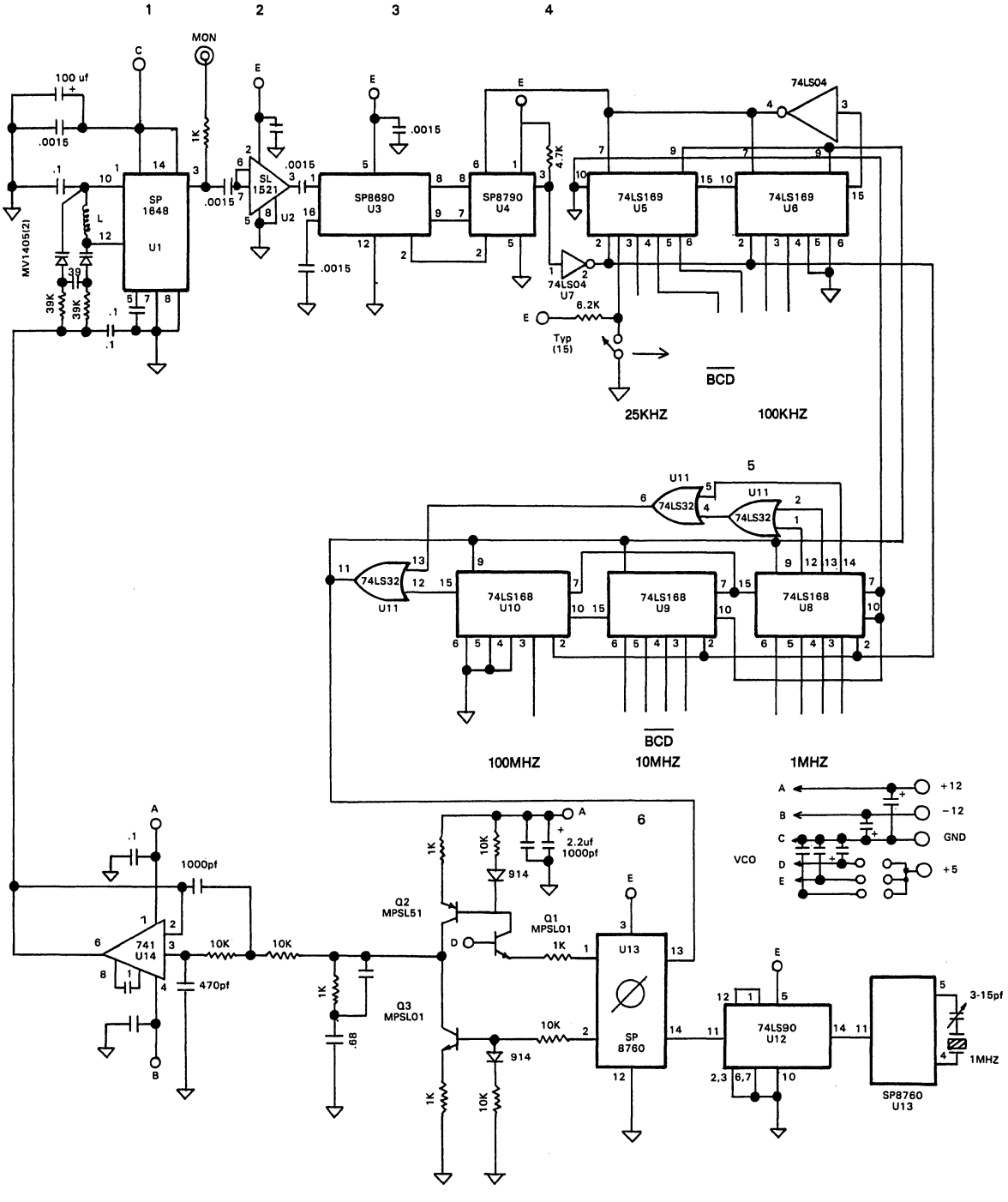
For this particular application, the modulus counter was not used. If a reference crystal of 1.5 or 1.6 MHZ were used, then the divide by 15/16 counter could be used in place of the 74LS90 divide by 10 counter.

Using a 1 MHZ crystal, the oscillator output at pin 11 is 250 KHZ. The 250 KHZ is divided by 10 in the 74LS90 decade counter. The output of 25 KHZ is used as the reference frequency for the phase comparator. The parallel load signal at pin 11 is compared to the reference frequency and an error signal is fed to the charge pump via the outputs on pins 1 and 2. Q1 through Q3 make up the charge pump that supplies current to the storage capacitor C1.

The 741 (U14) is used as an active low pass filter. The roll off starts at about 2.5 KHZ. Thus helping to get rid of the 24 KHZ spurs in the VCO.

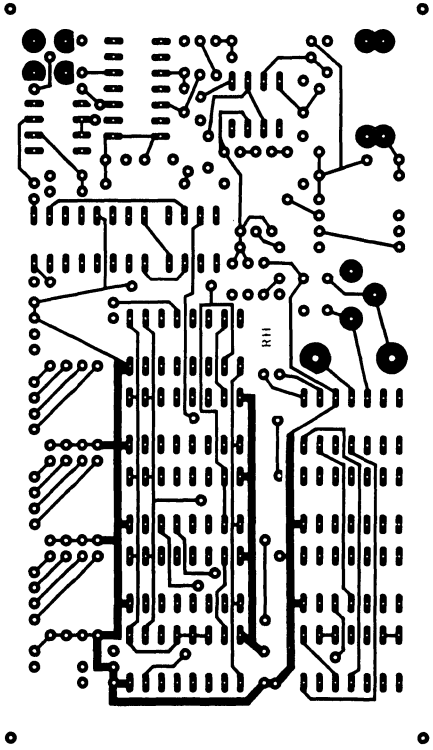
Another way to filter out the 25 KHZ noise is to have two or three notch filters tuned for 25 KHZ, 50 KHZ, and 75 KHZ.

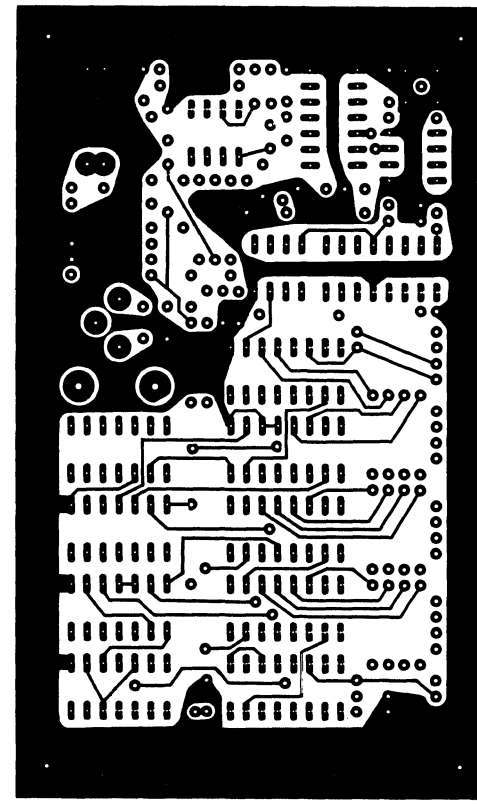
The output of the filter is used to set the VCO frequency and keep the output phase locked to the internally generated reference.




**VHF SYNTHESISER**
**108-174 MHZ**

FIGURE 1





**Solder Side**

**Parts List**

**Component Side**

U1 Plessey SP 1648
U2 Plessey SL 1521
U3 Plessey SP 8690
U4 Plessey SP 8790
U5,6 National DM 74LS169 N
U7 National DM 74LS04 N
U8,9,10 National DM 74LS168N
U11 National DM 74LS32 N
U12 National DM 74LS90 N
U13 Plessey SP 8760
U14 National 741

Q1,3 Motorola MPSL01
Q2 Motorola MPSL51

Dr 1, 2 Motorola MU1405

L1 Micrometalist 30-12
3 turns 22 ga

C1 Plessey .68uf

# VHF/UHF synthesisers using 2-modulus prescalers

**Fig. 1 shows the divider for a synthesiser operating between 100MHz and 199.9875MHz with 12.5kHz channel spacing. Fig. 2 shows the divider for a similar synthesiser operating between 300MHz and 512MHz with 25kHz channel spacing. The limit of operation of the SP8647 decade is defined in the datasheet as 250MHz giving a top frequency of 500MHz but since nearly all SP8647 devices will, in fact, operate at 256MHz, the figure given is quite conservative in practice.**

Both synthesisers are designed to use a reference frequency of 12.5kHz.

The VHF divider uses an SP8690 ÷10/11 counter combined with an SP8794 modulus extender to give a ÷80/81 two-modulus counter. The output from this counter at the highest input frequency is about 2.5MHz so the remaining counters may use CMOS logic operating on a 10V rail (operation below 10V might be possible but 5V operation would not).

The programmable counter consists of five CD4029 4-bit binary/decade counters, one used in binary mode and the rest either as decades or in modes where the matter is irrelevant. The counters are operated in the synchronous mode, where the output of the SP8974 (which requires a 33k ohm resistive pullup to the CMOS positive supply) drives the clock inputs of all the counters and the 'clock enable' inputs are cascaded.

Counters X1 and X2 form the counter controlling the two-modulus prescaler and count down from the number pre-set into them by the '12.5s of kHz' and '100s of kHz' inputs until they reach zero; the SP8690/8794 combination then stops dividing by 81 and divides by 80. X1 and X2 stop counting until the next cycle starts. It is important that the propagation delay from the output of the SP8974, via this counter, back into the control input of the SP8974 is shorter than a count cycle of the SP8690/8794 combination, otherwise the counter will not control the two-modulus counter soon enough to prevent the next cycle of the two-modulus counter being 81 instead of 80. At 200MHz this means that the propagation delay around the loop must be less than 700ns.

Counters X3, X4 and X5 form the MHz, 'tens of MHz', and 'hundreds of MHz' counters respectively. X5 is hard-wired to count one only so that the system will only work between 100MHz and 199.9875MHz; if lower frequency operation is required this counter could be made programmable but the X3/ X4/ X5 counter must not be allowed to operate with a division ratio less than 80, otherwise the two-modulus part of the system can not be operated over its full range (as described in section 2) and the synthesiser will malfunction. This places an absolute limit on the low frequency operation of the divider of 80MHz. The upper limit of 200MHz is set by the speed of the SP8690 and the CMOS.

All the CMOS counters operate in the 'countdown mode'. When the X3/X4/ X5 counter reaches zero all five counters are again preset to the values programmed on their input. The inverter on the output of X5 drives all the 'preset' inputs and if the preset time of all the counters is similar should perform the function perfectly well.

If, however, some counters preset more quickly than others it is possible that the signal on the 'preset' line may disappear before the operation is

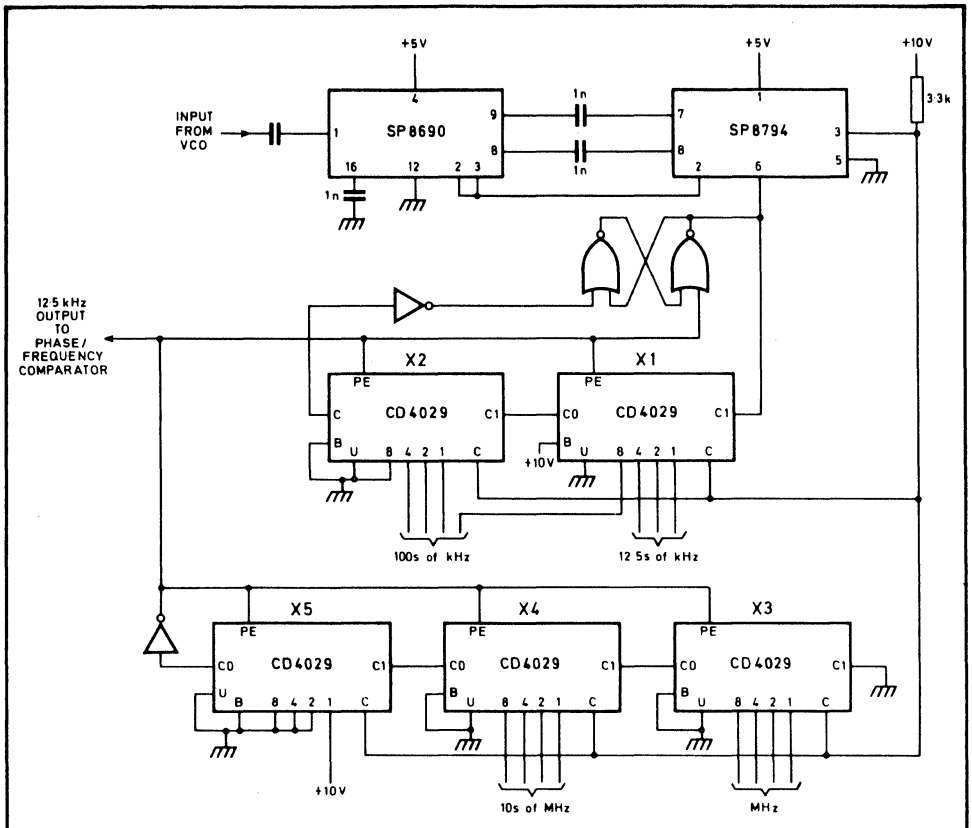



*Fig. 1 VHF synthesiser divider*

complete in all counters. In that case the inverters could be replaced with a monostable or some other form of pulse extender but it is essential that the preset pulse ends before the next clock pulse arrives. In other words, the delay from the edge of the clock pulse which reduces the counter to zero to the end of the preset pulse must not exceed 350ns.

The program inputs, with the exception of the 12.5s of kHz are programmed in binary coded decimal. The 12.5s of kHz are programmed in 3 bits of binary code. Each input must be connected to either 10V or to ground so either 2 way programming switches or pulldown resistors must be used.

The operation of the UHF synthesiser is very similar except that TTL is used instead of CMOS and a : 2 fixed-modulus prescaler precedes the two-modulus counter. The prescaler is necessary because although : 10/11 counters are available which will count at over 600MHz the SP8790 modulus extender will not operate with an input frequency of over 40MHz which limits the : 10/11 counter input to 400MHz. The use of this fixed prescaler means that the reference frequency is 12.5kHz although the channel spacing is 25kHz.

The : 2 prescaler is unnecessary and a reference frequency of 25kHz may be used if the modulus extender is built with ECL10K logic, which allows it to operate at up to 51.2MHz input frequency. If this is done the SP8647

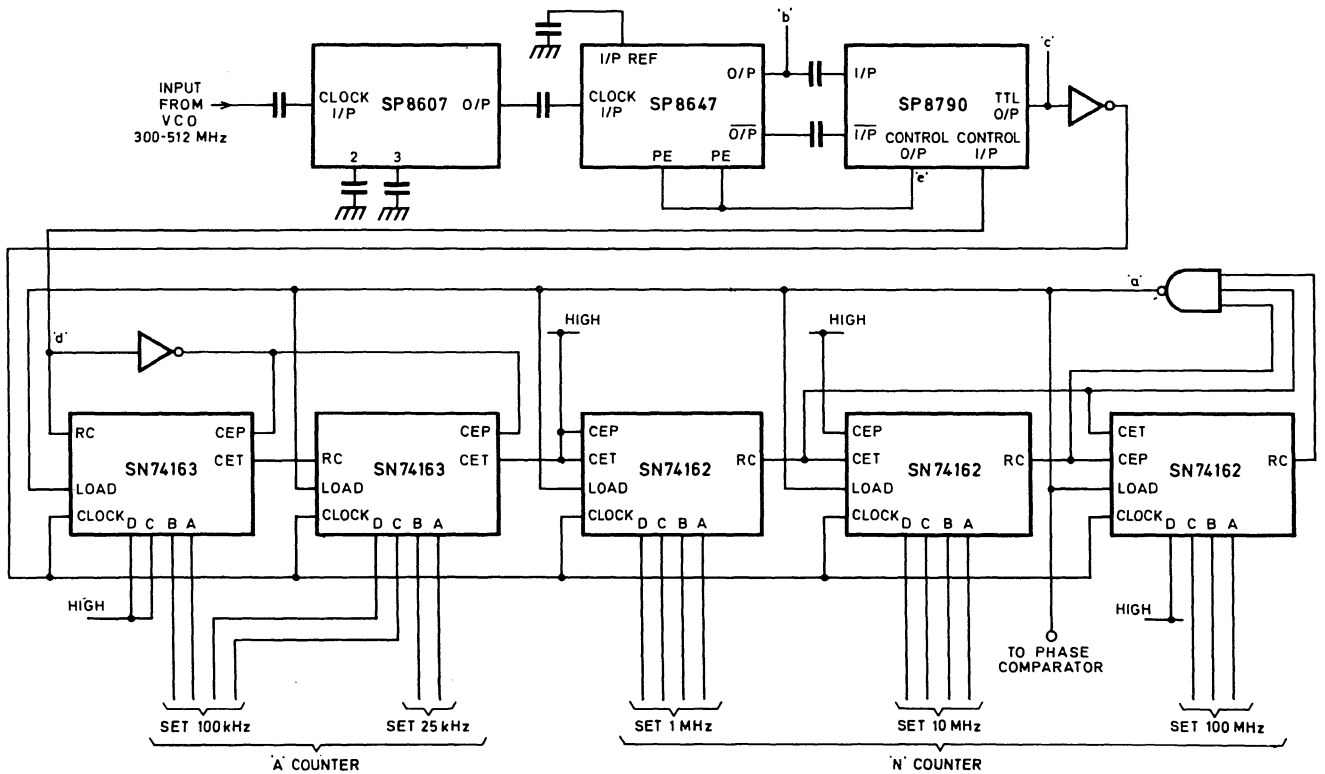



*Fig. 2 UHF synthesiser divider*

÷10/11 counter must be replaced with a faster counter such as the SP8685. Apart from the necessary ECL10K/TTL interface circuits the remainder of the system is unchanged.

The use of TTL allows all logic to use the same +5V supply but introduces complications in programming and choice of counter. There is no TTL device similar to the CD4029, so separate 4-bit binary and BCD counters must be chosen, the SN74163 and the SN74162 respectively. These counters may be used synchronously but the carry enable system is more complex than that of the CD4029. In addition since they are not reversible counters they must be programmed in 9s complement binary or 9s BCD instead of the simpler codes of the CMOS.

The remainder of each synthesiser would consist of a phase/frequency comparator, a reference frequency generator and VCO. The reference oscillator, part of the reference divider and the phase comparator could well be realised using the SP8760.

The method used to program the dividers will vary witht he use to be made of the synthesiser. If a general coverage synthesiser is required all the inputs may be programmed with thumbwheel switches. Logic may be placed between the switches and the programmable counters to introduce offsets if direct programming of receiver local oscillators is required.

If a few pre-programmed channels are required, a read only memory should be placed between the channel switch and the synthesiser. The simplest ROM for this application is a diode matrix. This has the advantage that it is easily programmed and re-programmed in the field but it is somewhat bulky. If a number of equipments are required with the same chanelling a commercially programmed integrated circuit ROM may be used and in intermediate cases an ultra-violet erasable PROM is suitable. Since most mobile radio transceivers operate much of the time in duplex mode (transmit on one frequency and receive on another) it is generally more convenient to program transmit and receive frequencies separately in the ROM than to arrange logic to provide offset during reception.

Traditionally, each channel in a mobile transceiver used two quartz crystals – one for transmission and one for reception. As standards of frequency stability improve so the cost per channel continues to rise. By using a high performance synthesiser with counters of the type described in this section only one quartz crystal is required per transceiver, no matter how many channels are synthesised. Such a synthesiser is economic with as few as three channels taking into account the saving on quartz crystals alone. Savings on inventory (since the reference crystals are standard) and commonality of design can make its use justified even in single channel transceivers.

# 5. Citizen and Amateur Band 2 Chip Synthesiser.

# Citizens' Band synthesiser using the SP8921/8922

**The SP8921/22 combination is intended to synthesise the frequencies required in a 40-Channel Citizens' Band transceiver. The 40 channels are spaced at 10kHz intervals (with some gaps) between 26.965 and 27.405MHz. Local oscillator frequencies for the reception of these channels with intermediate frequencies of 455kHz, 10.240MHz, 10.695MHz and 10.700MHz are also synthesised. Table 1 shows the relationship between the program input and the channel selected. By using a program other than one of the 40 given other frequencies may be selected – in fact there are 64 channels at 10kHz separation available from 26.895 to 27.525MHz and programming starts at all zeros on inputs A through F for 26.895 and each increase of one bit to the binary number on these inputs increases the channel frequency by 10kHz until all '1's give 27.525MHz. The A input is the least significant bit, F the most significant. The programming input on pin 16 of the SP8922 is normally kept high but making it low increases the programmed frequency by 5kHz. Table 2 shows the programming required to obtain various offsets.**

**The circuit diagram of a CB synthesiser is shown in Fig. 1. It is intended for use in double conversion receivers with IFs of 10.695 and 455kHz and generates either the frequency programmed or the frequency programmed less 10.695MHz.**

If other offsets are programmed the connections to pin 15 of the SP8921 and pin 2 of the SP8922 must be altered according to Table 2.

The synthesiser consists of the SP8921 and the SP8922 plus an SP1648 voltage controlled oscillator.

The programming inputs to the SP8922 are as shown in Table 1. Logic '1' is +3V or more, logic '0' is either ground or an open circuit. The circuit diagram of a programming input port is shown in Fig. 2. If a switch, constructed so as to select the correct combination for each channel, can be obtained this is the obvious way to program the synthesiser; otherwise a ROM may be suitably programmed and placed between the switch and the SP8922.

The crystal oscillator in the SP8921 is trimmed by a small variable capacitor, C3, which must be set up during alignment of the synthesiser so that the output frequency on pin 4 is 10.240000MHz. The only other adjustment is to set the core of L1 so that the varicap control voltage is 2.85V when the synthesiser is set to channel 30 transmit. Since the difference between transmit and receive frequencies is over 10MHz it is not possible to tune both with the same tuned circuit and an extra capacitor is switched by means of a diode during reception.

The phase/frequency comparator of the SP8921 can have an output swing from 0.5V to 3.8V but it is better to work in the range 1.5V to 3.0V as the phase-error output voltage is more linear in this region. The ZC822 tuning diode specified for this synthesiser may be replaced by any other tuning diode provided it will tune the VC0 over the required range, or a little more, as the control voltage goes from 1.5 to 3.0V. With slight coil changes the MV2105 has been used successfully in this synthesiser.

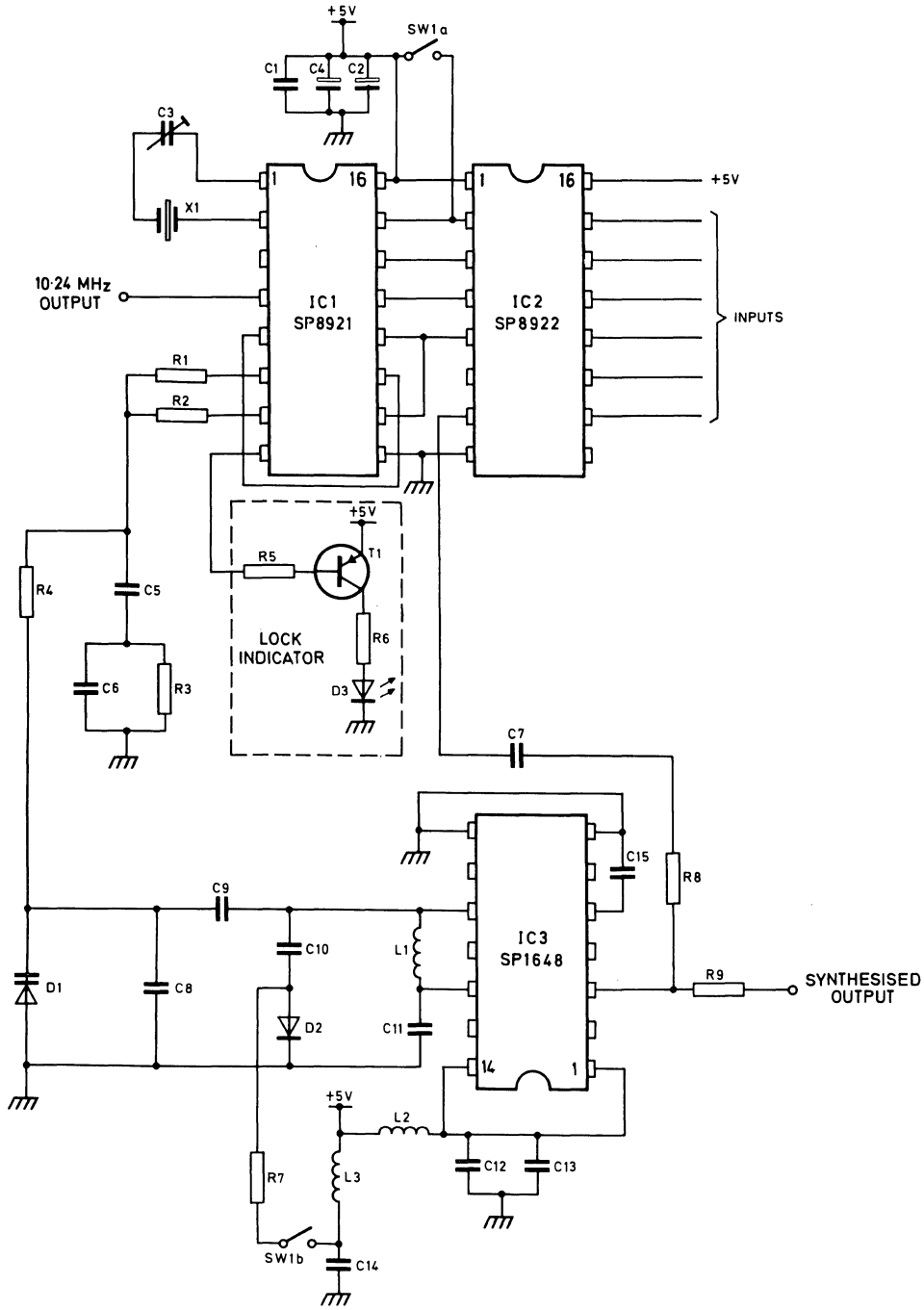



*Fig. 1 Low cost CB synthesiser component layout*

All resistors are in ohms and $\frac{1}{8}$W $\pm$ 10% unless otherwise stated. Capacitor values are in microfarads unless otherwise stated.

| | |
|---|---|
| IC1 | SP8921 |
| IC2 | SP8922/SP8923 – 40 channel |
| IC3 | SP1648 |
| T1 | 2N 3906 |
| D1 | ZC822, Ferranti varactor diode |
| D2 | 1N4148 Silicon diode |
| D3 | LED lock indicator |
| X1 | 10.240MHz crystal, series mode |
| L1 | 11 turns 30 gauge cotton covered wire on Neosid A7 assembly |
| L2 | 100 microhenries RF choke |
| L3 | 100 microhenries RF choke |
| R1 | 1.0k $\pm$ 5% |
| R2 | 1.0k $\pm$ 5% |
| R3 | 8.2k $\pm$ 5% |
| R4 | 33k |
| R5 | 10k |
| R6 | 150 (adjust for LED brightness) |
| R7 | 1k |
| R8 | 1k |
| R9 | 470 (adjust for required output level) |
| C1 | 0.1 |
| C2 | 100, 10V solid tantalum |
| C3 | 2 – 22pF variable |
| C4 | 100, 10V solid tantalum |
| C5 | 1,10V solid tantalum |
| C6 | 0.1 |
| C7 | 1000pF |
| C8 | 22pF + 10% |
| C9 | 0.01 |
| C10 | 100pF $\pm$ 10% |
| C11 | 0.01 |
| C12 | 0.1 |
| C13 | 10,10V solid tantalum |
| C14 | 0.1 |
| C15 | 1000pF |
| SW1 | 2 pole, 1 way switch, (receive/transmit) |

| Channel No. | Input Code F E D C B A | Output frequency with R/T = 0 (MHz) |
|---|---|---|
| 1 | 0 0 0 1 1 1 | 26.965 |
| 2 | 0 0 1 0 0 0 | 26.975 |
| 3 | 0 0 1 0 0 1 | 26.985 |
| 4 | 0 0 1 0 1 1 | 27.005 |
| 5 | 0 0 1 1 0 0 | 27.015 |
| 6 | 0 0 1 1 0 1 | 27.025 |
| 7 | 0 0 1 1 1 0 | 27.035 |
| 8 | 0 1 0 0 0 0 | 27.055 |
| 9 | 0 1 0 0 0 1 | 27.065 |
| 10 | 0 1 0 0 1 0 | 27.075 |
| 11 | 0 1 0 0 1 1 | 27.085 |
| 12 | 0 1 0 1 0 1 | 27.105 |
| 13 | 0 1 0 1 1 0 | 27.115 |
| 14 | 0 1 0 1 1 1 | 27.125 |
| 15 | 0 1 1 0 0 0 | 27.135 |
| 16 | 0 1 1 0 1 0 | 27.155 |
| 17 | 0 1 1 0 1 1 | 27.165 |
| 18 | 0 1 1 1 0 0 | 27.175 |
| 19 | 0 1 1 1 0 1 | 27.185 |
| 20 | 0 1 1 1 1 1 | 27.205 |
| 21 | 1 0 0 0 0 0 | 27.215 |
| 22 | 1 0 0 0 0 1 | 27.225 |
| 23 | 1 0 0 1 0 0 | 27.255 |
| 24 | 1 0 0 0 1 0 | 27.235 |
| 25 | 1 0 0 0 1 1 | 27.245 |
| 26 | 1 0 0 1 0 1 | 27.265 |
| 27 | 1 0 0 1 1 0 | 27.275 |
| 28 | 1 0 0 1 1 1 | 27.285 |
| 29 | 1 0 1 0 0 0 | 27.295 |
| 30 | 1 0 1 0 0 1 | 27.305 |
| 31 | 1 0 1 0 1 0 | 27.315 |
| 32 | 1 0 1 0 1 1 | 27.325 |
| 33 | 1 0 1 1 0 0 | 27.335 |
| 34 | 1 0 1 1 0 1 | 27.345 |
| 35 | 1 0 1 1 1 0 | 27.355 |
| 36 | 1 0 1 1 1 1 | 27.365 |
| 37 | 1 1 0 0 0 0 | 27.375 |
| 38 | 1 1 0 0 0 1 | 27.385 |
| 39 | 1 1 0 0 1 0 | 27.395 |
| 40 | 1 1 0 0 1 1 | 27.405 |

*Table 1 SP8922/1 O/P frequencies with 10.240 crystal (0 = contact open, 1 = contact closed to Vcc)*

| Offset | SP8921 | SP8922 |
|---|---|---|
| 0 | 0 | 0 |
| –455kHz | 0 | 1 |
| –10.240MHz | 1 | 0 |
| –10.695MHz | 1 | 1 |

*Table 2*

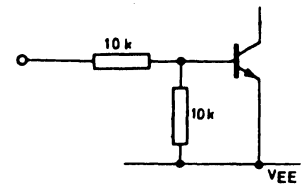



*Fig. 2 Program input circuit*

The low pass filter of the PLL consists of C5, C6 and R3. If faster lock (at the expense of larger noise and reference sidebands) is required the filter may be redesigned. If the synthesiser is used in a scanning receiver, a switched filter should be used to give fast lock during scanning but a slower lock and cleaner Signal during normal operation. The lock output on pin 8 of the SP8921 is used to light an indicator when the loop is *not* locked and should also be used, in a transmitter or transceiver, to prevent transmission when the loop is unlocked.

Fig. 3 shows the circuit board layout and component placing of this synthesiser. It requires a single +5V supply and draws about 60mA. The component list is given in Fig. 1. The performance is improved if double-sided board is used with a ground plane on one side. A small further improvement would come from the use of a grounded screening can over the whole system.

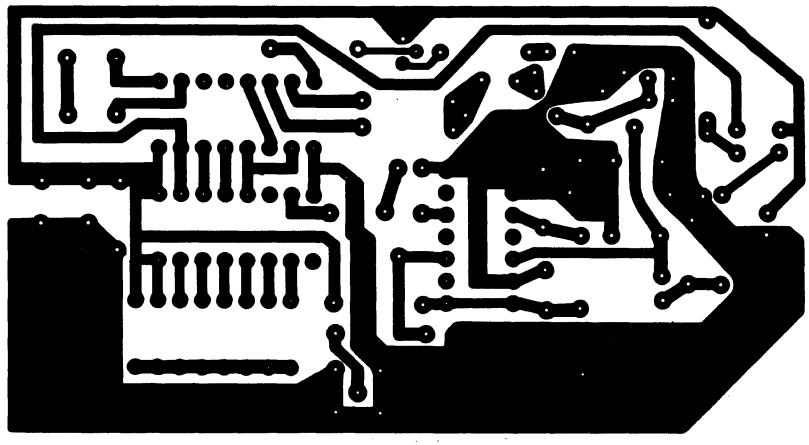


*Fig. 3a Printed circuit layout for CB synthesiser*

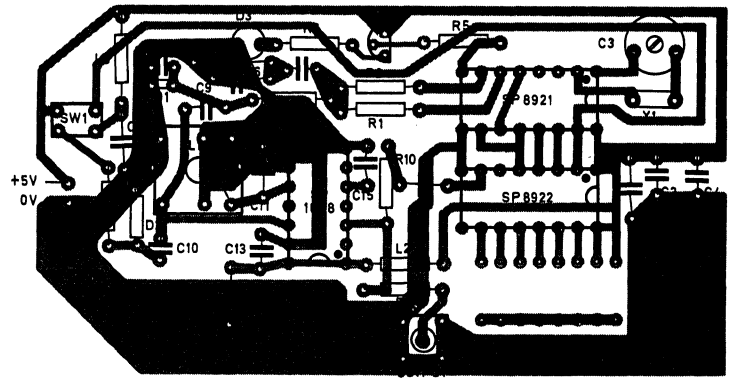



*Fig. 3b PCB component layout for CB synthesiser*

The synthesiser has reference frequency sidebands 50dB down at 1.25kHz from the carrier. All output over 5kHz from the carrier is over 70dB down. Lock time for a change from channel 0 to channel 40 (a frequency change of 440kHz) is around 35ms. Photographs of the output spectrum and the change of control voltage with time during a step from channel 0 to channel 40 are shown in Fig. 4. Stepping from transmit to receive or vice versa takes somewhat longer because of the much larger change of frequency but is generally complete within 75ms.

This synthesiser is quite basic but has adequate performance for the majority of CB applications. If improved performance is required there are two possibilities; an improved FET oscillator having lower floor noise instead of the SP1648 or an improved low pass filter to reduce reference frequency sidebands. Fig. 5 shows the circuit diagram of an improved oscillator using an E304 FET and the same coil and varactor as in the simple synthesiser. Fig. 6 shows a high performance synthesiser using an FET oscillator, a twin-T filter in the VCO control line to reduce reference sidebands at 1.25kHz to below —90dB, an SL1610C buffer giving over 60dB isolation from the output line back into the VCO, and separate voltage stabilisers for the oscillator and the logic of the system.

Fig. 7 shows a block diagram of the use of the synthesiser in a typical double conversion 27MHz Citizens' Band transceiver with direct generation of the transmit frequency. In such a system it is essential that the power amplifiers in the transmitter are well isolated from the VCO, otherwise phase modulation and quite unacceptable splatter will occur.

To reduce the need for isolation the system shown in Fig. 8 may be used — the synthesiser runs with an offset of 10.240MHz duringt ransmission and this signal is mixed with the 10.240 signal from the synthesiser to produce the final 27MHz for transmission. Such a transmitter is less liable to phase modulation resulting from inadequate screening but the output of the mixer must be well filtered to prevent transmission of the difference of 16.3MHz and 10.240MHz as well as their sum.

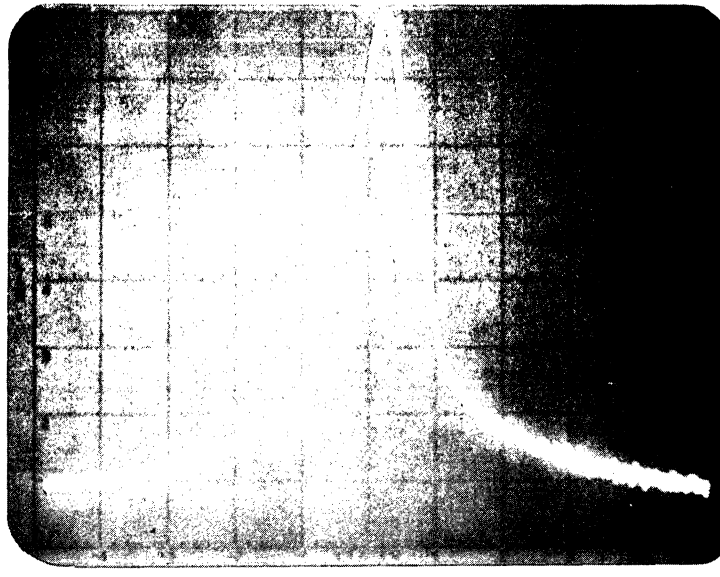


*Fig. 4a Typical output spectrum of basic synthesiser (Vert.:16dB/div., Horiz.:2kHz/div.,) BW:300Hz, fo:27.065MHz*

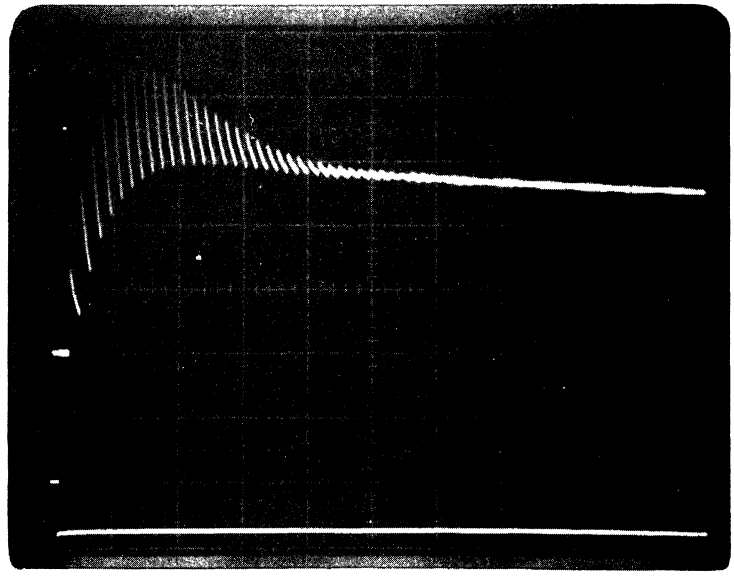


*Fig. 4b Typical transient response of basic synthesiser. Response of varactor line to step program change 1-40. Vert.:200mV/div., Horiz.:5ms/div.*
*N.B. Droop of response is due to the measuring instrument being AC-coupled.*

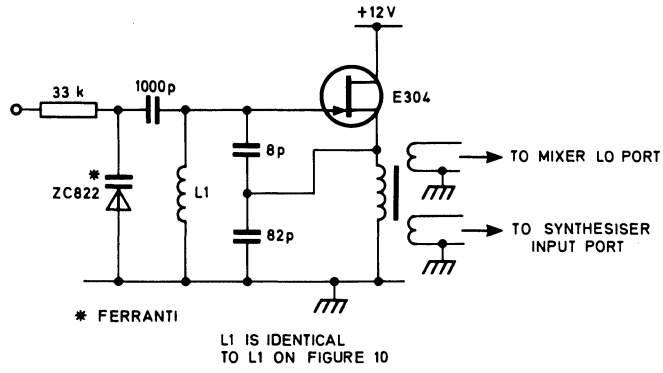



*Fig. 5 FET voltage controlled oscillator for 27MHz Citizens' Band Synthesiser*

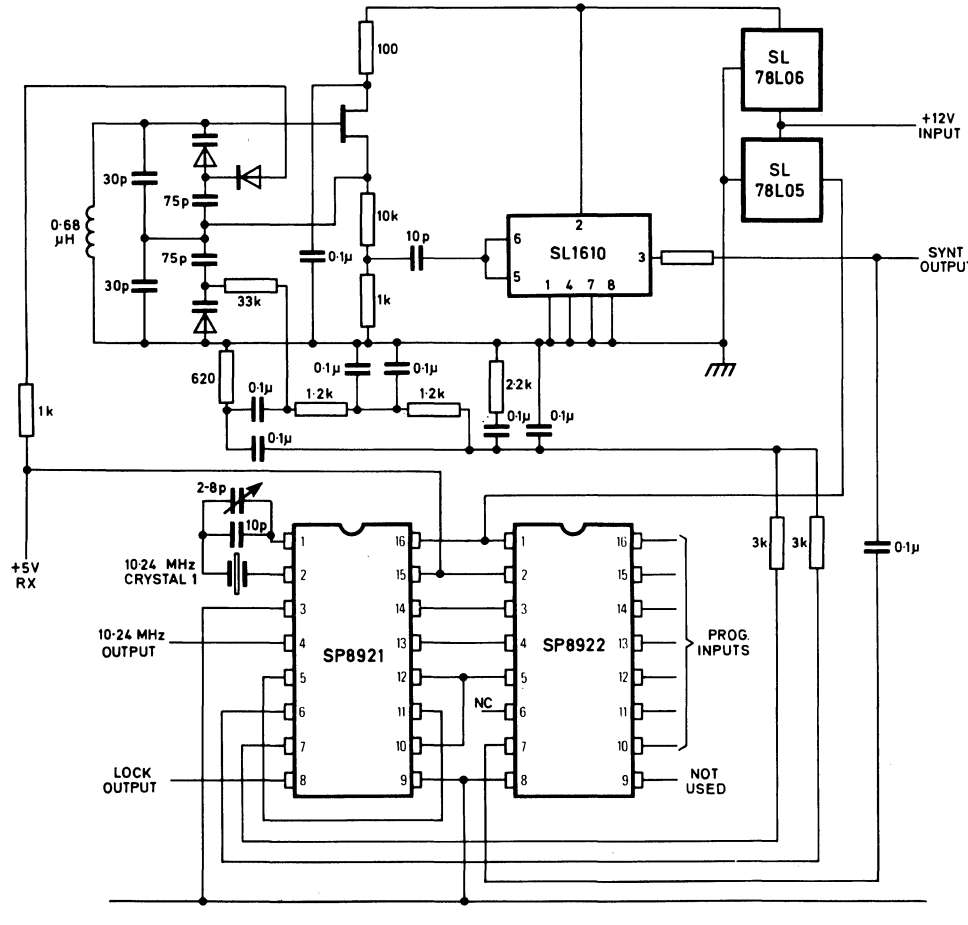



*Fig. 6 High performance Citizens' Band synthesiser*

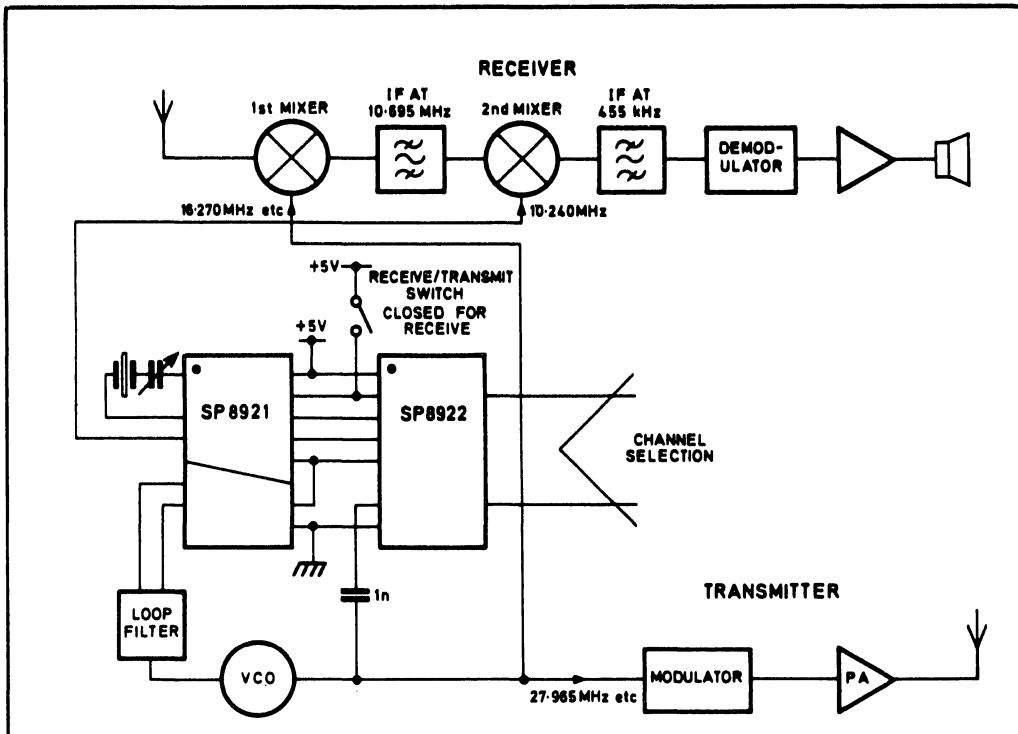



*Fig. 7 Typical double conversion set for Citizens' Band using the SP8921 (Direct generation of transmit frequency)*

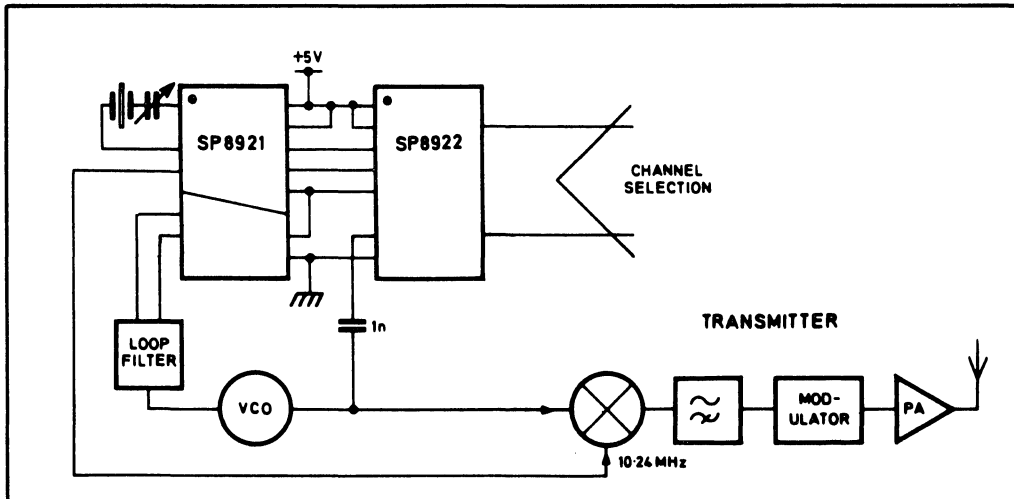



*Fig. 8 Typical Citizens' Band transmitter using the SP8921 (Indirect generation of transmit frequency)*

# European 2m amateur band synthesiser

**In Europe, the '2-metre' Amateur Band covers frequencies from 144MHz to 146MHz. Different countries have their own conventions about which parts of the band are used for different modes of operation. Some are internationally agreed but all use 25kHz channel spacing for channelised FM, unlike the USA where the standard is 15 or 30kHz. If low side injection and an IF of 10.7MHz are chosen the SP8921 and SP8922 CB synthesiser chips may be used to generate local oscillator frequencies over the whole 2 metre band at 25kHz intervals. The basic system is shown in Fig. 1.**

This note does not describe the VCO because various types are available and there is no general agreement as to which is the best for the purpose. At Plessey Semiconductors we built the system using a very low noise, high stability VCO using a Surface Acoustic Wave (SAW) delay line but this technology is only just available and is not yet competitive in amateur applications. Probably the best system would use an FET 'Kalitron' oscillator with a buffered output both to the transceiver mixer and to the divider input, but in any case the VCO should have as little noise and phase jitter as possible and should tune from about 133 to 135.6MHz for a tuning voltage range of 1.5V to 3V.

The divider uses an SP8622 ÷5 prescaler followed by the SP8921 and the SP8922. The SP8921, as in the CB synthesiser, also contains the crystal oscillator and its associated divider and the phase/frequency comparator.

The SP8622 is an easily-used circuit. It requires an input AC level of between 400 and 800 mV p–p and has two bias points which should be decoupled to ground with 0.1 microfarads as should its supply. Its input and output connections are made via 1000pF capacitors. No precautions against self-oscillation are necessary in this application as an input should always be present.

The SP8922 receives a signal from the SP8622 and is used to program the channel required. Table 8 shows the inputs required on pins 10 to 16 (A to G) for various channels. Pin 2 (the Receive/Transmit pin in 27MHz CB operation) is connected to the supply. Since the SP8922 was not designed for amateur 2-metre use there is no simple relationship between the program inputs and the channel selected so either complex switch wiring or a read only memory is required. A commercial ROM or a diode matrix could be used.

If the synthesiser is used in a transmitter it is necessary to mix a frequency-modulated 10.7MHz signal with its output and filter the image. If the transmitter is to be used with repeaters the ROM (or switch) must contain logic to provide a 600kHz shift between transmission and reception. The connections between the SP8922 and the SP8921 are made as in the CB application.

The SP8921 is used exactly as in the 27MHz CB application except that pin 15, the Receive/Transmit pin is grounded. The crystal frequency is 10.240MHz and the low-pass filter in the phase comparator is the more complex of the two described previously in order to reduce 1.25kHz reference frequency sidebands in the synthesiser. The filter should be shielded both from the dividers and the VCO to obtain best performance. The lock output on pin 8

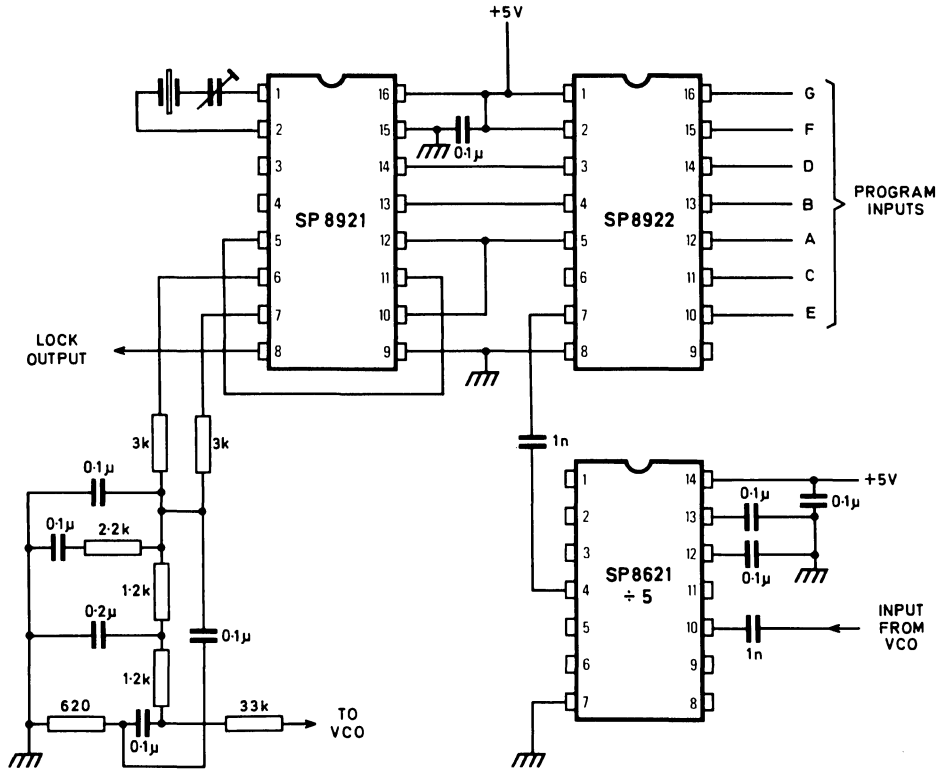



*Fig. 1 Divider and filter for synthesiser for 2 metre amateur band*

should be connected to prevent transmission when the synthesiser is unlocked. In transmitters, the VCO should be very well shielded from the PA stages to prevent interference and unlocking due to feedback.

If the synthesiser is required to interpolate between the 25kHz channels, the crystal oscillator in the SP8921 should be replaced by two crystal oscillators – one to synthesise the channels accurately and the other, a variable crystal oscillator with a tuning control (possibly using a varactor) used to interpolate or provide Receiver Incremental Tuning (RIT). It is better to use external oscillators than try to make the SP8921 switch between these two functions.

The performance of the synthesiser is good – reference sidebands can be reduced to —90dB on the signal and there are no spurious outputs visible on a 100dB spectrum analyser but care is needed to shield and decouple the various parts and their power supplies. The ultimate spectral purity of the output not only depends on the synthesiser but also on the baseband noise of the VCO used.

| Transceiver Frequency (MHz) | Channel | Actual Synthesiser Frequency (MHz) | Pin Number | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | 16 G | 12 A | 13 B | 11 C | 14 D | 10 E | 15 F |
| 145.000 | SO[RO(T)] | 134.300 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 145.025 | R1(T) | 134.325 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 145.050 | R2(T) | 134.350 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 145.075 | R3(T) | 134.375 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 145.100 | R4(T) | 134.400 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 134.125 | R5(T) | 134.425 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 145.150 | R6(T) | 134.450 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 145.175 | R7(T) | 134.475 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 145.200 | R8(T) | 134.500 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 145.225 | R9(T) | 134.525 | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 145.250 | R10(T) | 134.550 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 145.500 | S20 | 134.800 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 145.525 | S21 | 134.825 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 145.550 | S22 | 134.850 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 145.575 | S23 | 134.875 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 145.600 | S24 [RO(R)] | 134.900 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 145.625 | R1(R) | 134.925 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 145.650 | R2(R) | 134.950 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 145.675 | R3(R) | 134.975 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 145.700 | R4(R) | 135.000 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 145.725 | R5(R) | 135.025 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 145.750 | R6(R) | 135.050 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 145.775 | R7(R) | 135.075 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 145.800 | R8(R) | 135.100 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| 145.825 | R9(R) | 135.125 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 145.850 | R10(R) | 135.150 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |

*Table 1 Programming for 2-metre synthesiser*

# 6. Characteristics and Interfacing for the SP8000 Series.

# Characteristics and interfacing for the SP8000 series high speed dividers

## INTRODUCTION

The SP8000 series of high frequency dividers achieve their characteristics of high operating frequency (extending beyond 1GHz for some of the range) and low power from the use of emitter coupled switching circuits. The dividers themselves are all built from the basic 'divide by 2' circuit shown in Figure 1. The divide by 2 circuit is a master-slave arrangement, and has a very flexible set of design constraints.

Perhaps the most significant of these is the size of the tail current supplying each differential pair. The different characteristics of devices in the SP8000 series are achieved by variation of this parameter. For example, the SP8667, a 1.2GHz decade, operates with a tail current in the first stage of 6mA giving a typical current consumption of 80mA for the four divide by 2 stages comprising the decade whereas the SP8655, a 100MHz divide by 32, operates with a tail current of 350 microamps giving a typical current consumption of only 10mA for the five divide by 2's.

Another technique employed to improve speed is that of driving the clock transistor (Ta, Tb in figure 1) directly instead of through a level shifting emitter follower. A further refinement is to use a common base stage as a collector load to reduce collector mode capacitance and this is employed on the faster types such as the SP8614, 5, 6 divide by 4 and SP8665, 6, 7 divide by 10. This does of course have the disadvantage that the power supply voltage has to be increased from the normal 5.2V to 6.8V.

This tailoring of the divider circuits means that it is not possible to treat the SP8000 series of dividers as a consistent family for interfacing purposes. The variations of the dividers are covered later in this note.

## GENERAL PHYSICAL LAYOUT CONSIDERATIONS

The high performance of the SP8000 series of counters can only be exploited if the appropriate construction techniques are employed. All signal lines, both input and output, should be characterised as transmission lines and terminated correctly to avoid reflections. This is particularly important at the device input as the high input sensitivity and speed of most of the dividers makes them prone to counting reflected edges. Care must also be taken on output lines as the counters generate extremely fast edges (typically 2 ns).

The dividers are usually employed in systems which predominantly operate at much lower frequencies than the dividers themselves and so many of the precautions necessary with large scale ECL logic systems are not necessary. The most usual interconnection technique employed at high frequencies is microstrip line.

Clearly, to facilitate line terminations it is desirable that the input impedance of the dividers should be much higher than the characteristic impedance of the line. It is recommended that lines with a characteristic impedance of

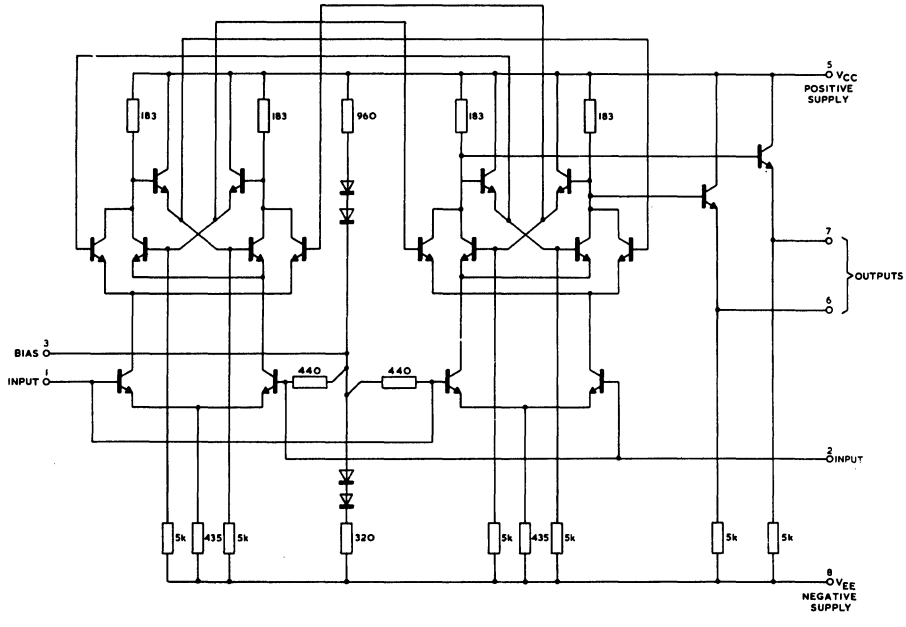



*Fig. 1 Divide by 2 circuit diagram. All resistor values are nominal*

50 ohms be used if possible. Higher characteristic impedances should be avoided as correct termination becomes more difficult to achieve and cross-talk and noise performance deteriorates.

In addition to these signal line restrictions the normal precautions appropriate to the frequencies and edge speeds being handled should be observed. These include the use of a ground plane (already required for the microstrip signal lines) which may be the positive supply.

The selection of the positive supply for the ground plane ensures that the poor immunity of ECL gates with respect to their positive (Vcc) supply is not a performance hazard. All components, particularly decoupling capacitors, should be of a suitable type for the frequencies involved.

If it is not desirable to have a positive ground (for example, where a predominantly TTL system employs one or two high speed dividers), then it is permissible to operate SP8000 dividers with a negative ground. However, it should be noted that output levels are referenced to the positive supply and any drift in this will be reflected in the output levels. Great care should be taken with supply decoupling, preferably decoupling every ECL package Vcc supply pin to ground so that supply noise does not cause mis-counting of a divider.

Provided that these simple precautions are observed the SP8000 dividers can be applied to a system without any problems.

## INPUT INTERFACING

The high speed and sensitivity of the SP8000 series of dividers is achieved in part by omitting the level shifters normally employed in ECL counter circuits. These are replaced by input resistors which bias the clock inputs at the centre of their active region. For this reason AC coupling to the clock inputs is recommended for the majority of the dividers.

Although DC coupling to clock inputs is permissible, in practice it is not easy to provide a source which will track the input bias level sufficiently accurately to maintain the specified sensitivity. The only exceptions to this rule are the SP8600 and SP8601 divide by 4 circuits, where the inputs are not prebiased and a bias chain has to be provided externally, and the SP8640, 8641, 8642 and 8643 divide by 10/11 circuits which have an ECL III type clock input and so should be driven from an ECL III or ECL 10K gate. As no internal bias is provided for the clock inputs on SP8640 type dividers, if capacitive coupling is desired then a bias chain is required.

The technique of input prebiasing, used on most of the SP8000 dividers, which is responsible for their high sensitivity, does have one disadvantage. If Fig. 2 the graph of input sensitivity against frequency for a typical SP8630, is studied, it can be seen that the curve has a pronounced dip at around 250MHz. This is interpreted as a tendency to oscillate in the absence of any input signal. It should be emphasised that provided a signal greater than the minimum specified is present at the clock input then there is no tendency to miscount.

If the divider is being used in a continuous system such as a frequency synthesiser then clearly this is not a problem. However, in other applications, such as frequency counters, where the input would not be continuous this characteristic is clearly an embarrassment. Fortunately it is a simple matter to remove this problem. The input prebias is counteracted by adding a small bleed resistor to Vee on the clock input. The required value of this resistor varies from type to type. It is not important which clock input is offset, but a slight decrease in sensitivity is usually experienced. In almost all cases the counters will still meet the guaranteed performance specification.

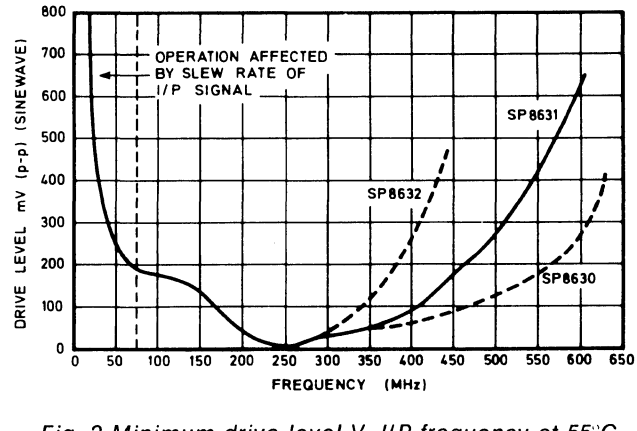



*Fig. 2 Minimum drive level V. I/P frequency at 55°C*

The only devices in which this characteristic is not present are:

**(a) SP8601**

This divide by 4 circuit has no prebias on the inputs and was originally designed to allow transformer coupling to the inputs. A resistor is added in the emitter of one clock input to introduce a small offset to prevent self clocking. The SP8601 may be driven from any ECL II type gate or divider with ECL II type outputs.

**(b) SP8643**

This divide by 10/11 circuit has ECL III type clock inputs with internal pulldown resistors. It should be noted that the SP8685 500MHz divide by 10/11 is designed for AC input coupling and does *not* have internal pulldown resistors.

## REFERENCE BIAS AND INPUT DECOUPLING

Most of the SP8000 series of dividers are provided either with complementary clock inputs or reference bias points. To exploit their full sensitivity and frequency specification the reference bias points should be decoupled to the systems RF ground. A suitable value for this decoupling capacitor is 15–1000pF. Values greater than 1000pF should be avoided as damage may be caused to the reference bias chain when power is applied to the circuit.

Similar comments apply to the unused clock inputs of those devices which have complementary clock inputs.

## EXTENDING THE FREQUENCY AND SENSITIVITY

### Frequency

Obviously little can be done to improve the upper frequency limit of the dividers except to observe the construction advice given above.

The low frequency end is not a fundamental limitation though. The specified low frequency cut off is measured with a sine wave input. However, the devices are edge sensitive and so they will operate perfectly down to DC provided the edge speed that they are driven with exceeds, for most of the dividers, 100V/microsecond (i.e. 6.4ns rise time for an 800mV input signal).

### Sensitivity

If the sensitivity of SP8000 dividers is not adequate then there are available several microwave integrated circuits which will provide 10–26dB of gain up to 1GHz and beyond. The use of these amplifiers and also that of input circuits for extending the low frequency limit is described at the end of this Appendix.

## OUTPUT CIRCUITS

The SP8000 dividers have output circuits which may be classified into two types: open collector or emitter follower. Most of the dividers have emitter follower outputs giving ECL III type outputs, which are easily interfaced. One of the dividers has an emitter follower output, but with a limited output swing. This can be increased by an additional external emitter load. This is the SP8602, 8607 divide by 2 circuit.

Only three of the dividers have open collector outputs. These are the SP8600, 8601 divide by 4, the SP8634 divide by 10 and SP8655, 8657, 8659 low power dividers. The divide by 4 and divide by 10 circuits both have complementary current sources. These are designed to operate in a non-saturating mode. The low power dividers have a saturating free collector output.

Both output circuits can interface with TTL and CMOS (providing that the open collector does not go more than 12V more positive than Vee). Type 1 can also directly interface with ECL II type inputs whereas type 2 can directly drive a much higher load and is particularly useful where the ECL divider and the following TTL or CMOS operate off of the same supplies. The recommended operation of these open collector outputs is described below.

## Type 1 Open Collector Output

### SP8600, 8601

The output current of these devices is guaranteed to be at least 2mA. It has a small temperature coefficient and can be expected to be less than 3.5mA under all conditions. Care should be taken to prevent the output transistors saturating as this will reduce the maximum operating frequency.

### SP8634

This BCD divide by 10 circuit has type 1 open collector current source outputs on the BCD outputs and on one carry output (the other carry is an ECL II type.) They have a higher operating point than those on the SP8600 and so it is not possible to use them to drive ECL gates. The BCD outputs have a limited drive capability. The carry output can drive 3 TTL loads with a lower collector load. For maximum performance it is recommended that the ECL carry output (pin 9)be used to drive a level shift circuit such as the ECL 10K type MC10125.

## Type 2 Open Collector Output

### SP8655, 8657, 8659

These low power dividers have a type 2 open collector output. This type of output has two advantages in low power applications. The saturating output allows the device to operate off the same supply as its following TTL or CMOS dividers and the power consumption of the output can be tailored to the particular system's power and speed requirement. The maximum DC TTL load that can be accommodated is 2 standard TTL inputs with a 2.7 kilohms pullup resistor.

## Emitter Follower Outputs

All the remaining dividers in the SP8000 series have emitter follower outputs and all except the SP8602 and 8607 can be directly interfaced with ECL II by the addition of a 1.5 kilohm resister to Vee. ECL III or 10K levels are generated by the addition of a series resistor. It should be noted that the devices are not capable of driving 50 ohm transmission lines directly. Some may however, be used to drive series terminated 50 ohm lines, provided sufficient current is maintained in the output emitter follower.

### SP8602, 8607

These devices, although having an emitter follower output which can drive ECL II, III or 10K via interfaces do not have sufficient drive capability for a low impedance transmission line. If operation in a transmission line environment is desired then an ECL line receiver such as the MC10116 should be used.

## SUMMARY

The SP8000 series of high speed dividers represents a family of devices whose input and output characteristics present the engineer with a sufficient diversity to allow the correct solution for any system. The devices are easy to use in a system provided the constraints covered above are observed.

# Input characterisation for the SP8000 series

**Because of the wide frequency range of the SP8600 series emitter-coupled logic dividers, the input drive and impedance should be optimized.**

The input impedance from 50MHz to 600MHz is mostly capacitive. Beyond 600MHz it becomes inductive.

To optimize the circuit to handle large overloads, small signals, and changes of input impedance versus operating frequency some suggestions are offered in Figs. 1, 2 and 3.

Where the frequency range to be used covers an impedance change of greater than three to one, as in Fig. 6, between 50MHz to 300MHz, a circuit shown in Fig. 1 could be added to the input. By using the appropriate input impedance curve and calculating the value of R & L, the total input impedance would be more constant over the required frequency range.

In the case of large overloads the circuit shown in Fig. 2 could be used.

When using this circuit there is typically a 3dB loss in sensitivity but the dynamic range would be increased from two to one to over four to one. The value of R depends on the maximum overdrive voltage and the hot carrier diodes used.

For low level inputs an SL1521 wideband amplifier could be used as a preamplifier for a divider as shown in Fig. 3.

By using the SL1521 and the SP8690 low power 200MHz divide by 10/11 divider, as shown in Fig. 3, the minimum sensitivity is reduced from 143mV RMS to 36mV RMS. Both units are self biased and require only coupling capacitors for interconnections. Also both parts operate from the same +5V supply at 145mW total power.

When using the SP8600 series it is recommended that good low inductance RF capacitors be used on all bias and power supply decoupling points.

The printed circuit board should be laid out with all input leads as short as possible, ample ground plane around the device and using other normal RF techniques.

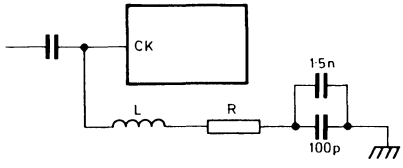



*Fig. 1*

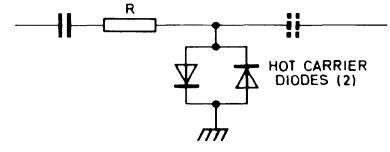



*Fig. 2*

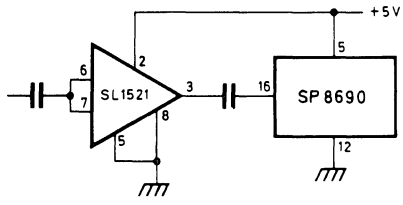



*Fig. 3*

# SP8602, 7

## INPUT IMPEDANCE

The input impedance is shown in Fig. 4 for the frequency range of 50MHz to 700MHz.

## INPUT CAPACITANCE

The capacitance at 50MHz is 3.1pF.

## TEST CIRCUIT

The test circuit is shown in Fig. 5. All tests were made at 25°C.

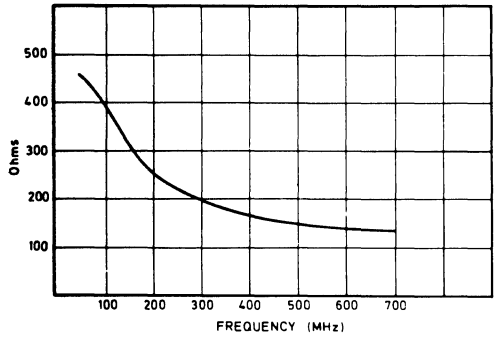



*Fig. 4*

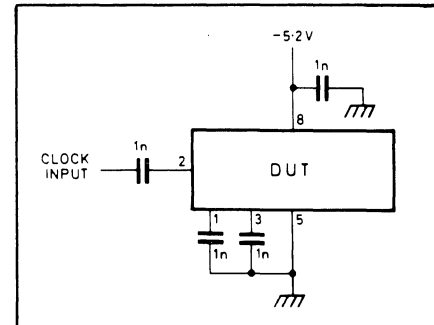



*Fig. 5*

# SP8615, 6

## INPUT IMPEDANCE

The input impedance is shown in Fig. 6 for the frequency range of 50MHz to 1.2GHz.

## INPUT CAPACITANCE

The capacitance at 50MHz is 4.6pF.

## TEST CIRCUIT

The test circuit is shown in Fig. 7. All tests were made at 25°C.

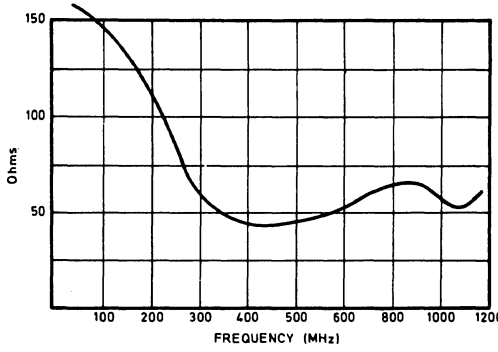



*Fig. 6*

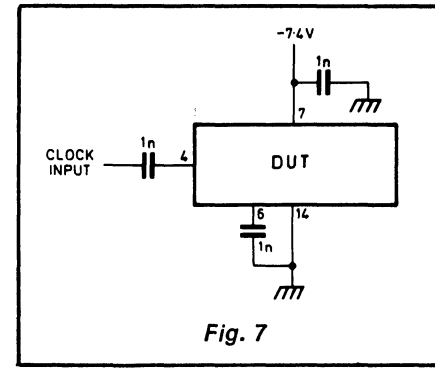



*Fig. 7*

# SP8630

## INPUT IMPEDANCE

The input impedance is shown in Fig. 8 for the frequency range of 50MHz to 600MHz.

## INPUT CAPACITANCE

The capacitance at 50MHz is 3.9F.

## TEST CIRCUIT

The test circuit is shown in Fig. 9. All tests were made at 25°C.

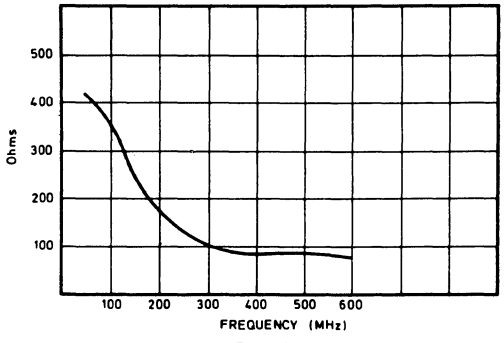



*Fig. 8*

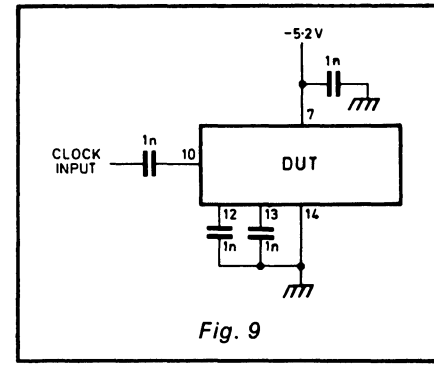



*Fig. 9*

# SP8634

## INPUT IMPEDANCE

The input impedance is shown in Fig. 10 for the frequency range of 50MHz to 700MHz.

## INPUT CAPACITANCE

The capacitance at 50MHz is 4.1pF.

## TEST CIRCUIT

The test circuit is shown in Fig. 11. All tests were made at 25°C.

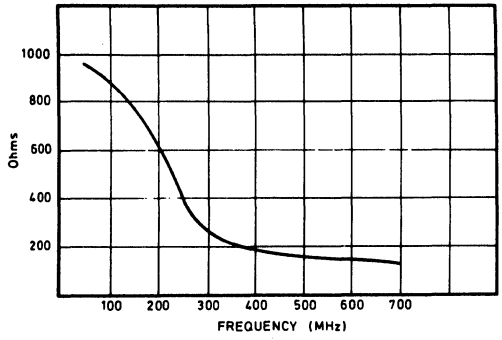



*Fig. 10*

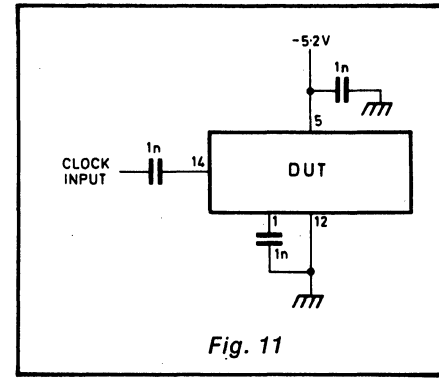



*Fig. 11*

# SP8643, 7

## INPUT IMPEDANCE

The input impedance is shown in Fig. 12 for the frequency range of 50MHz to 350MHz.

## INPUT CAPACITANCE

The capacitance at 50MHz is 2.4pF.

## TEST CIRCUIT

The test circuit is shown in Fig. 13. All tests were made at 25°C.

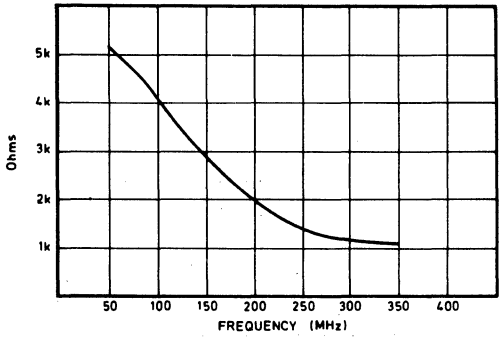



*Fig. 12*

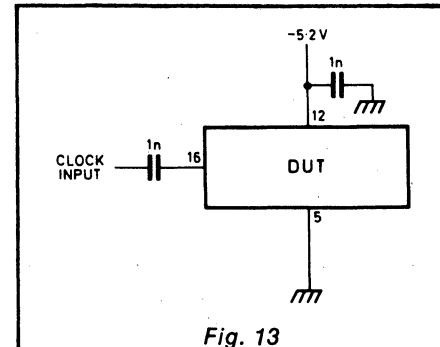



*Fig. 13*

# SP8650

## INPUT IMPEDANCE

The input impedance is shown in Fig. 14 for the frequency range of 50MHz to 600MHz.

## INPUT CAPACITANCE

The capacitance at 50MHz is 6.0pF.

## TEST CIRCUIT

The test circuit is shown in Fig. 15. All tests were made at 25°C.

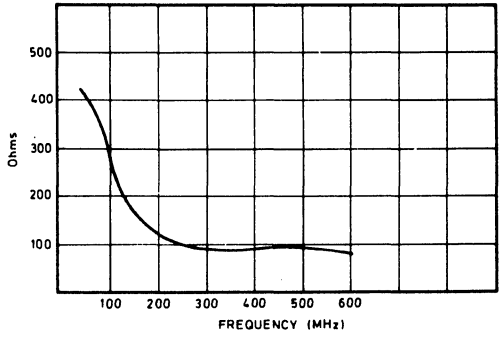



*Fig. 14*

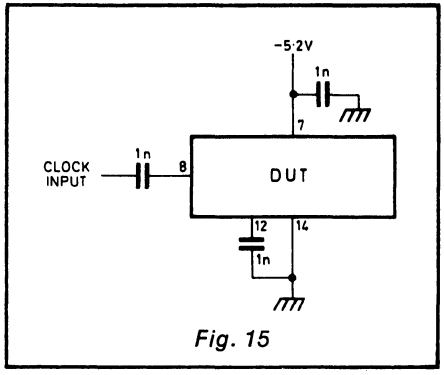



*Fig. 15*

# SP8655, 7, 9

## INPUT IMPEDANCE

The input impedance is shown in Fig. 16 for the frequency range of 50MHz to 100MHz.

## INPUT CAPACITANCE

The capacitance at 50MHz is 3.6pF.

## TEST CIRCUIT

The test circuit is shown in Fig. 17. All tests were made at 25°C.

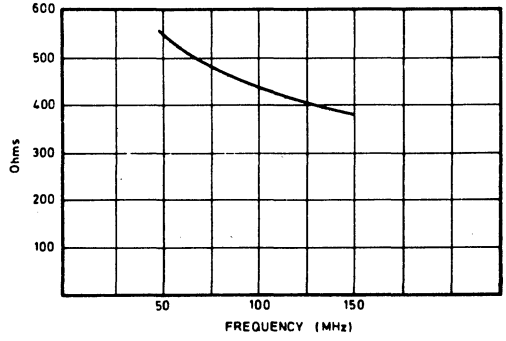



*Fig. 16*

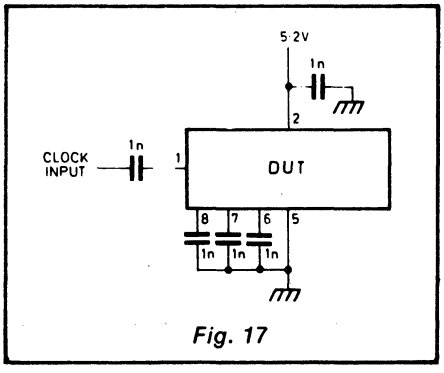



*Fig. 17*

# SP8665, 7

## INPUT IMPEDANCE

The input impedance is shown in Fig. 18 for the frequency range of 50MHz to 1.2GHz.

## INPUT CAPACITANCE

The capacitance at 50MHz is 4.5pF.

## TEST CIRCUIT

The test circuit is shown in Fig. 19. All tests were made at 25°C.

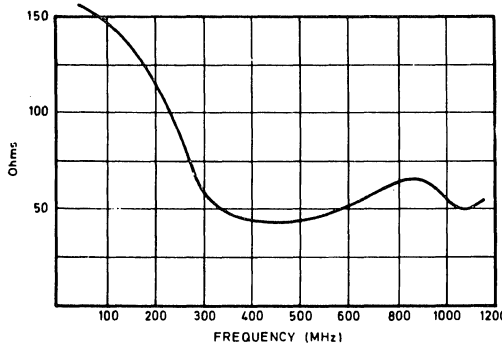



*Fig. 18*

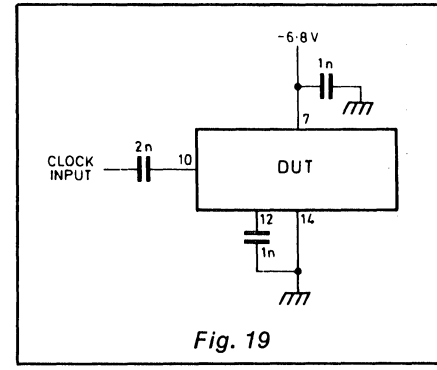



*Fig. 19*

# SP8685

## INPUT IMPEDANCE

The input impedance is shown in Fig. 20 for the frequency range of 50MHz to 500MHz.

## INPUT CAPACITANCE

The capacitance at 50MHz is 8.7pF.

## TEST CIRCUIT

The test circuit is shown in Fig. 21. All tests were made at 25°C.

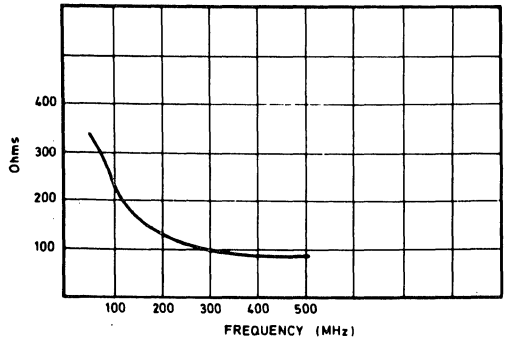



*Fig. 20*

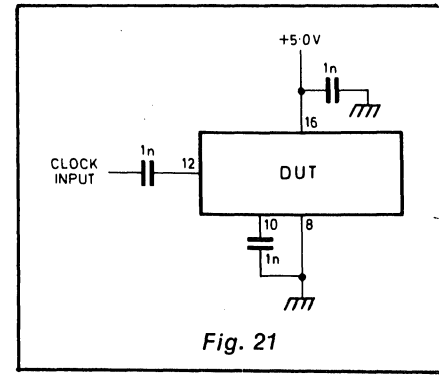



*Fig. 21*

## INPUT IMPEDANCE

The input impedance is shown in Fig. 22 for the frequency range of 50MHz to 200MHz.

## INPUT CAPACITANCE

The capacitance at 50MHz is 6.4pF.

## TEST CIRCUIT

The test circuit is shown in Fig. 23. All tests were made at 25°C.

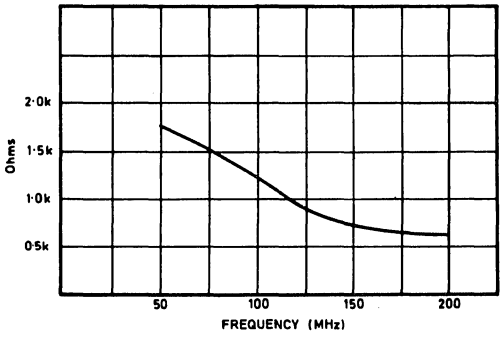



*Fig. 22*

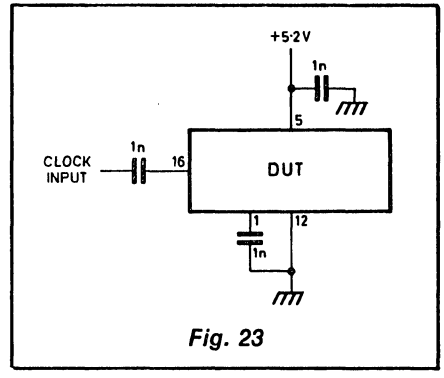



*Fig. 23*

# Input characterisation for the SP8000 series
# The use of hybrid IC front end amplifiers to improve the sensitivity of SP8000 series high speed dividers

**The availability of low-cost hybrid amplifiers with a performance extending to 1GHz, coupled with SP8000 High Speed Dividers, allows an unparalled increase in instrument performance.**

For example, using an Amperex ATF 417 as a preamplifier for an SP8616 (with a Schottky barrier diode limiter), the divider's sensitivity can be improved by at least 15dB. The circuit diagram is shown in Fig. 1. Typical room temperature performance is shown in Fig. 2, and a suitable PCB layout is given in Fig. 3.

Low end performance is limited by signal rise time requirements for the SP8616, whilst high end sensitivity is limited by the amplifier limiter performance. This can be improved by operating the ATF 417 off a higher supply. By increasing the supply to, say, +20V, a gain in sensitivity of, typically, 5dB would be expected at 1GHz.

Similar results can be obtained using the ATF 417 with other dividers such as the SP8667, 1.2GHz decade divider.

## CIRCUIT DETAILS

The signal input (100MHz–1GHz) is AC-coupled to a Schottky barrier diode bridge which limits at 100mV p/p. The signal is then amplified by the hybrid A1. This combination gives about 15dB of gain with a supply of 15V. The amplifier is AC coupled, via C3, to an SP8616 ÷4 circuit (IC1). R7 provides an input offset to prevent 'no signal' oscillation. The drive capability of IC1, is increased by R8 and its output capacitively coupled to IC2 via C4 R9 provides the input offset for IC2. The output of IC2 is suitable for driving ECL II.

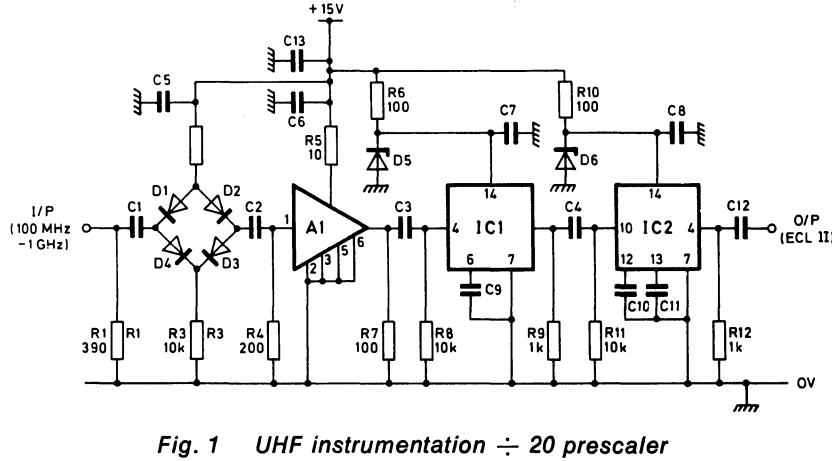



*Fig. 1 UHF instrumentation ÷ 20 prescaler*

## COMPONENTS

D1 – D4 : Schottky barrier diodes, HP5082–2811
A1 : Hybrid amplifier, Amperex ATF417 or Philips OM185
IC1 : Plessey Semiconductors SP8616B
IC2 : Plessey Semiconductors SP8621B
D5 : 1 Watt, 7.5V Zener diode
D6 : 1 Watt, 5.1V Zener diode
R6, R10 : 100 ohms, 5 Watt, e.g. Plessey GWT-5
C1 – C12 : 1nF ceramic, e.g. ITW EMCAPS
C13 : 0.33 microfarad

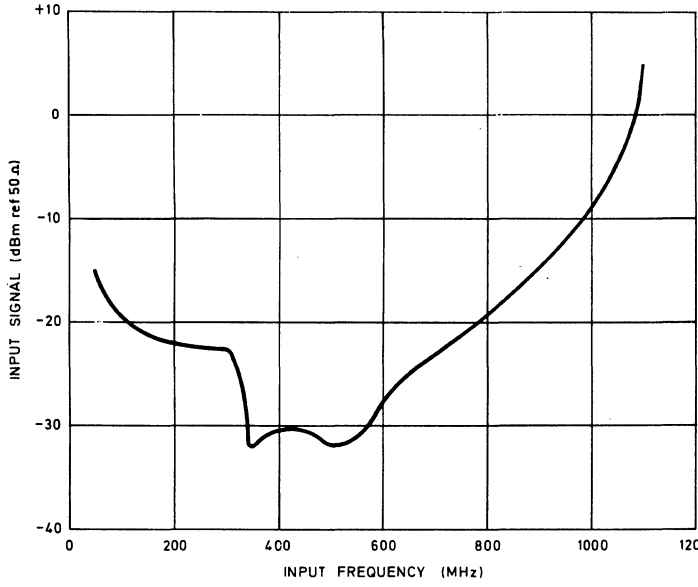



*Fig. 2 Typical performance of UHF prescaler*

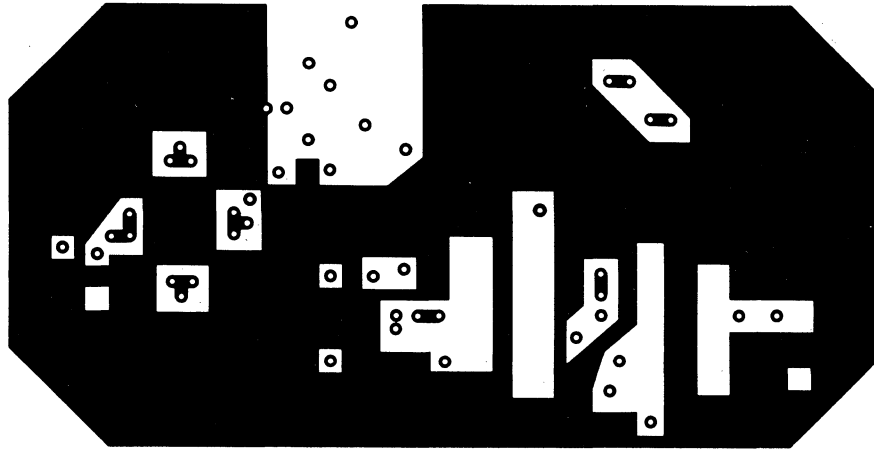


*Fig. 3a Component side of board*

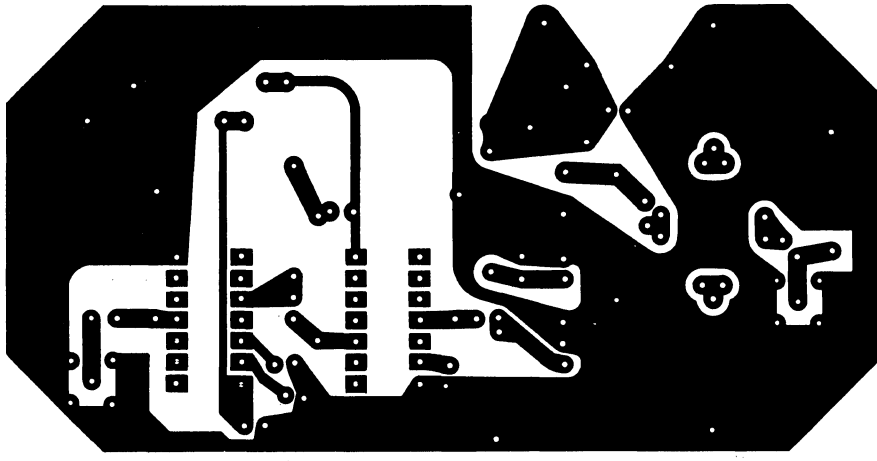


*Fig. 3b Solder side of board*

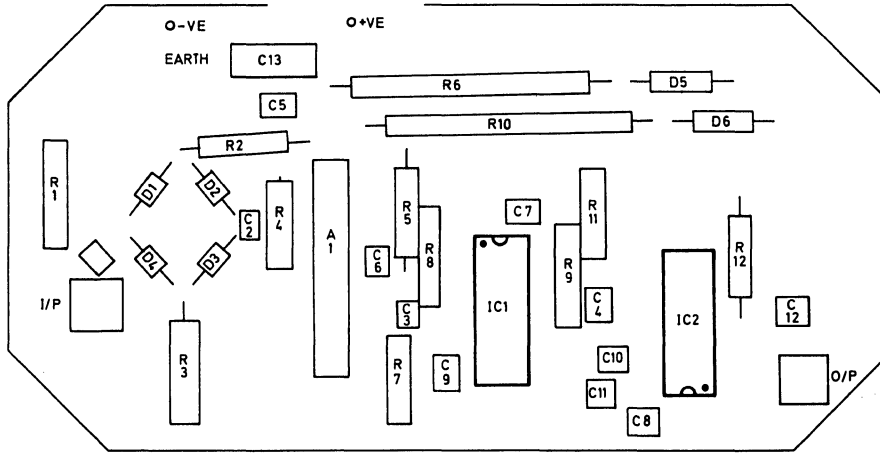



*Fig. 3c Component location*

# 7. Technical Data.

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# NJ8811

## CONTROL CIRCUIT FOR FREQUENCY SYNTHESIS

The NJ8811 is an N-channel MOS integrated circuit that provides all the decoding and controlling circuitry for frequency synthesisers. It is intended to be used in conjunction with a 4-modulus prescaler such as the SP8901 or SP8906 to produce a universal binary coded synthesiser for mobile radio applications.

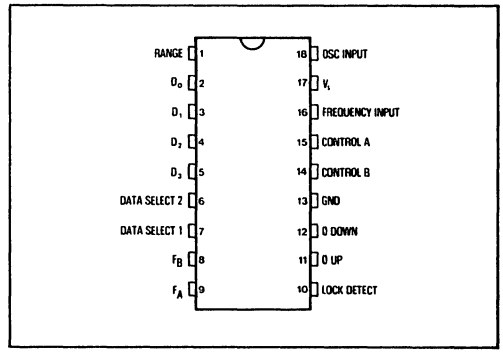


*Fig.1 Pin connections*

### FEATURES

- High Frequency Range
- Low Pin Count
- Direct Interface to ROM or PROMS
- Preset Channel Spacings 40, 50, 60kHz and Sub-multiples.
- High Comparison Frequency.
- Low Level Sinewave Crystal Oscillator Input up to 10MHz.
- Systems Clock Available—Constant Data Select Frequency of 1.2kHz.
- Microprocessor Compatible.

### GENERAL DESCRIPTION

The NJ8811 can be described by 3 system blocks: the reference divider, the programmable divider and the phase/frequency comparator, as shown in Fig.2. All control inputs and outputs are TTL compatible.

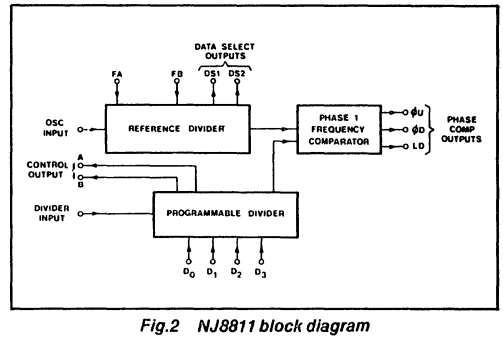


*Fig.2 NJ8811 block diagram*

### ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$V_S$: 5.0V ±0.25V
Temperature range: -30°C to +70°C

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min | Typ. | Max | | |
| Oscillator input | 50 | | | mV RMS | 4.8MHz reference oscillator AC coupled sinewave FA, FB O/C. |
| Max. oscillator input frequency | 10 | | | MHz | 200mV RMS sinewave. |
| Supply current | | 8.0 | 12 | mA | All data inputs O/C. |
| Max. counter input frequency | 2.5 | | | MHz | Input TTL compatible. |
| DS1/DS2 Output | | | | | |
| High Level | 2.4 | | | V | Outputs TTL compatible. |
| Low Level | | | 0.4 | V | |
| Phase comparator output current sink | 1 | | | mA | $Ø_U$ $Ø_D$ 0.5V max. |

### The Reference Divider

The reference divider is driven externally from a 4.8MHz crystal oscillator and can be externally preset to one of sixteen division ratios. These division ratios enable all commonly used reference frequencies to be applied to the phase/frequency comparator. Selection is accomplished using the two pins FA and FB. These pins may be connected to ground (logic '0') or left open circuit (logic '1'), connected to Data Select 1 output or to Data Select 2 output. On-chip decoding enables the latter two states to be recognised as independent states. All sixteen selections may be latched on-chip by grounding the Data Select 2 output. Table 2 gives a table of reference frequencies that can be preset using a 4.8MHz crystal oscillator.

The data select outputs originate from the reference divider. The data select outputs are independent of the preset reference

### Programmable Divider

The programmable division section of the NJ8811 consists of two 4-bit programmable dividers and an 8-bit programmable divider. The two 4-bit dividers control the module of the external prescaler and the 8-bit counter determines the total count period. The SP8906/NJ8811 combination is capable of dividing by all integer values between 3840 and 69,375. When the Range pin on the NJ8811 is grounded the programme range is shifted to between 36,608 and 102,143.

The programming data is multiplexed as 4 words of 4 bits, completing a 16 bit binary number. This input data may be stored on-chip by grounding the Data Select 2 output.

### Phase/Frequency Comparator

The outputs of the fixed and variable dividers on the NJ8811 are internally connected to a phase/frequency comparator. The comparator provides three open drain outputs. The logic diagram is shown in Fig.3.

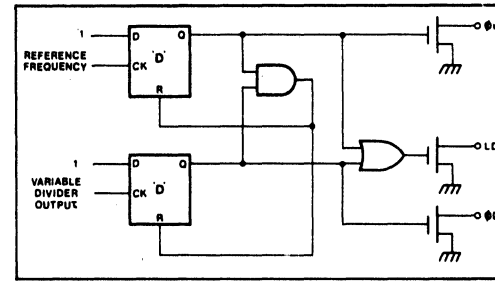


*Fig.3 Logic diagram of phase frequency comparator*

### Data Selection

To programme the synthesiser the following information is required:

1. The reference comparison frequency—equal to the channel spacing when using the SP8906, or half when using the SP8901.
2. The frequency of the VCO.

The frequency programme information is presented to the device in multiplexed form of 4 word of 4 bits. The reading of this data by the device is controlled by the two data select outputs from the device. This sequence is shown in Fig.4.

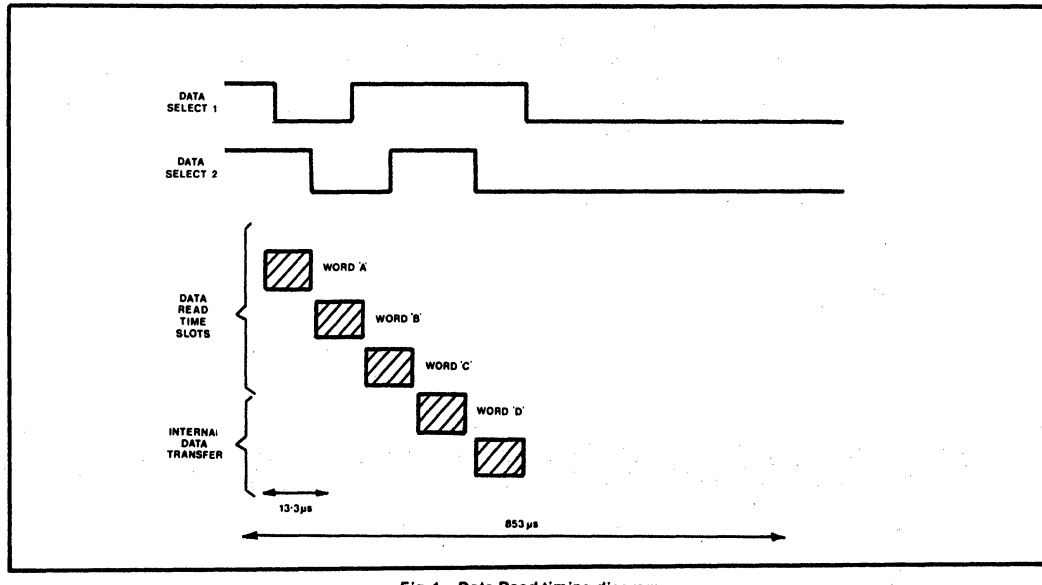


*Fig.4 Data Read timing diagram*

| FB/FA | GND | O/C | DS1 | DS2 |
|---|---|---|---|---|
| Gnd | 20 | 10 | 5 | 2.5 |
| O/C | 25 | 12.5 | 6.25 | 3.125 |
| DS1 | 30 | 15 | 7.5 | 3.75 |
| DS2 | 37.5 | 18.75 | 9.375 | 4.6875 |

*Table 1 Reference frequency selection (all frequencies in kHz)*

Table 2 shows the VCO frequency programme range that can be obtained using NJ8811 and SP8901.

| Channel Spacing | 40kHz | 50kHz | 60kHz |
|---|---|---|---|
| Low Range (MHz) | 76.8—(1000) | 96.0—(1000) | 115.2—(1000) |
| High Range (MHz) | 732.2—(1000) | 915.2—(1000) | |

| Channel Spacing | 20kHz | 25kHz | 30kHz |
|---|---|---|---|
| Low Range (MHz) | 38.4—693.8 | 48.0—867.2 | 57.6—(1000) |
| High Range (MHz) | 366.1—(1000) | 457.6—(1000) | 549.2—(1000) |

| Channel Spacing | 10kHz | 12.5kHz | 15kHz |
|---|---|---|---|
| Low Range (MHz) | 19.2—346.9 | 24.0—433.6 | 28.8—520.4 |
| High Range (MHz) | 183.1—510.8 | 228.8—638.4 | 274.6—766.1 |

| Channel Spacing | 5kHz | 6.25kHz | 7.5kHz |
|---|---|---|---|
| Low Range (MHz) | 9.6—173.5 | 12.0—216.8 | 14.4—260.2 |
| High Range (MHz) | 91.5—255.4 | 114.4—319.2 | 137.3—383.0 |

*Table 2 Frequency programme range for SP8901 (with 4.800MHz crystal)*

Table 3 shows the VCO frequency programme range that can be obtained using NJ8811 and SP8906.

| Channel Spacing | 20kHz | 25kHz | 30kHz |
|---|---|---|---|
| Low Range (MHz) | 76.8—(500) | 96.0—(500) | 115.2—(500) |
| High Range (MHz) | — | — | — |

| Channel Spacing | 10kHz | 12.5kHz | 15kHz |
|---|---|---|---|
| Low Range (MHz) | 38.4—(500) | 48.0—(500) | 57.6—(500) |
| High Range (MHz) | 366.1—(500) | 457.6—(500) | — |

| Channel Spacing | 5kHz | 6.25kHz | 7.5kHz |
|---|---|---|---|
| Low Range (MHz) | 19.2—346.9 | 24.0—433.6 | 28.8—(500) |
| High Range (MHz) | 183.1—(500) | 228.8—(500) | 274.6—(500) |

| Channel Spacing | 2.5kHz | 3.125kHz | 3.75kHz |
|---|---|---|---|
| Low Range (MHz) | 9.6—173.5 | 12.0—216.8 | 14.4—260.2 |
| High Range (MHz) | 91.5—255.4 | 114.4—319.2 | 137.3—383.0 |

*Table 3 Frequency programme range for SP8906 (with 4.800MHz crystal)*

To calculate the Programme number for a given VCO frequency and channel spacing the following equation is used:

$$\text{Programme Number } N = \frac{1000 \times f}{C} - R$$

where f = VCO frequency in MHz
C = channel spacing in kHz
R = range number (R = 3840 range = 1)
(R = 36608 range = 0)

The programme number is converted to a 16 bit binary number and is segregated as 4 words of 4 bits.

The least significant word is first entered during the Data Read 1 time slot via the inputs $D_3$, $D_2$, $D_1$ and $D_0$ and the most significant last (Data Read 4 time slot).

For example, with a VCO frequency of 937MHz and channel spacing of 12.5kHz

f = 937
C = 12.5
R = 36608
N = 38352

Conversion to a 16 bit binary number is performed as follows:

| | Result |
|---|---|
| 1. Divide by 4096 | 9.363 |
| 2. Write down the number before decimal place (WORD 'D') | 9 |
| 3. Subtract this number | 0.363 |
| 4. Multiply by 16 | 5.812 |
| 5. Write down the number before decimal place (WORD 'C') | 5 |
| 6. Subtract this number | 0.812 |
| 7. Multiply by 16 | 13.000 |
| 8. Write down the number before decimal place (WORD 'B') | 13 |
| 9. Subtract this number | 0 |
| 10. Multiply by 16 | 0 |
| 11. Write down nearest whole number (WORD 'A') | 0 |

The four decimal numbers obtained may now be directly converted to binary, and these are presented to the data inputs as shown in Table 4.

| DS1 | DS2 | $D_3$ | $D_2$ | $D_1$ | $D_0$ | |
|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | WORD 'A' |
| 0 | 0 | 1 | 1 | 0 | 1 | WORD 'B' |
| 1 | 0 | 0 | 1 | 0 | 1 | WORD 'C' |
| 1 | 1 | 1 | 0 | 0 | 1 | WORD 'D' |

*Table 4*

The data may be latched internally by grounding the DS2 output. This is useful when interfacing to a microprocessor. The NJ8811 is also compatible with most types of PROM and ROM for data coding applications.

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# NJ8812

## CONTROL CIRCUIT FOR FREQUENCY SYNTHESIS

The NJ8812 is an N-channel MOS integrated circuit that provides all the decoding and controlling circuitry for frequency synthesisers. It is intended to be used in conjunction with a 2-modulus prescaler such as the SP8793 to produce a universal binary coded synthesiser for mobile radio applications.

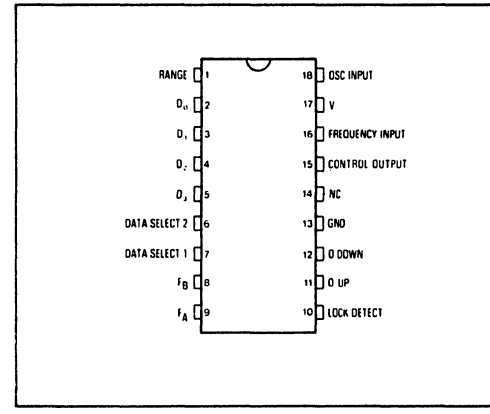



*Fig.1 Pin connections*

### FEATURES

- High Frequency Range
- Low Pin Count
- Direct Interface to ROM or PROMS
- Preset Channel Spacings 20, 25, 30kHz and Sub Multiples.
- High Comparison Frequency.
- Low Level Sinewave Crystal Oscillator Input up to 10MHz.
- Systems Clock Available—Constant Data Select Frequency of 1.2kHz.
- Microprocessor Compatible.

### GENERAL DESCRIPTION

The NJ8812 can be described by 3 system blocks: the reference divider, the programmable divider and the phase/frequency comparator, as shown in Fig.2. All control inputs and outputs are TTL compatible.

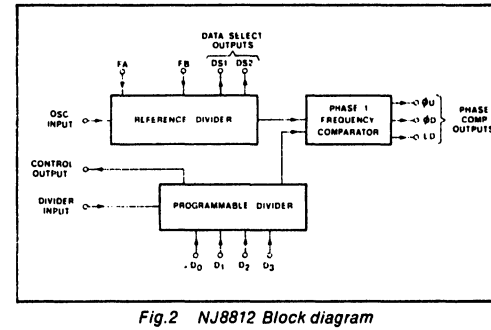



*Fig.2 NJ8812 Block diagram*

### ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$V_S$: 5.0V ±0.25V
Temperature range: -30°C to +70°C

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min | Typ. | Max | | |
| Oscillator input | 50 | | | mV RMS | 4.8MHz reference oscillator AC coupled sinewave FA, FB O/C. |
| Max. oscillator input frequency | 10 | | | MHz | 200mV RMS sinewave. |
| Supply current | | 8.0 | 12 | mA | All data inputs O/C. |
| Max. counter input frequency | 5.0 | | | MHz | Input TTL compatible. |
| DS1/DS2 Output | | | | | |
| High Level | 2.4 | | | V | Outputs TTL compatible. |
| Low Level | | | 0.4 | V | |
| Phase comparator output current sink | 1 | | | mA | $Ø_U$ $Ø_D$ 0.5V max. |

### The Reference Divider

The reference divider is driven externally from a 4.8MHz crystal oscillator and can be externally preset to one of sixteen division ratios. These division ratios enable all commonly used reference frequencies to be applied to the phase/frequency comparator. Selection is accomplished using the two pins FA and FB. These pins may be connected to ground (logic '0') or left open circuit (logic '1'), connected to Data Select 1 output or to Data Select 2 output. On-chip decoding enables the latter two states to be recognised as independent states. All sixteen selections may be latched on-chip by grounding the Data Select 2 output. Table 2 gives a table of reference frequencies that can be preset using a 4.8MHz crystal oscillator.

The data select outputs originate from the reference divider. The data select outputs divide a crystal oscillator frequency by 4096 and are independent of the preset reference frequencies.

### Programmable Divider

The programmable division section of the NJ8812 consists of a 6-bit programmable divider and an 8-bit programmable divider. The 6-bit divider controls the modulus of the external prescaler and the 8-bit counter determines the total count period. The SP8793/NJ8812 combination is capable of dividing by all integer values between 1600 and 11840. When the Range pin on the NJ8812 is grounded the programme range is shifted to between 6720 and 16960.

The programming data is multiplexed as 3 words of 4 bits and 1 of 2 bits completing a 14-bit binary number. This input data may be stored on chip by grounding the Data select 2 output.

### Phase/Frequency Comparator

The outputs of the fixed and variable dividers on the NJ8812 are internally connected to a phase/frequency comparator. The comparator provides three open drain outputs. The logic diagram is shown in Fig.3.

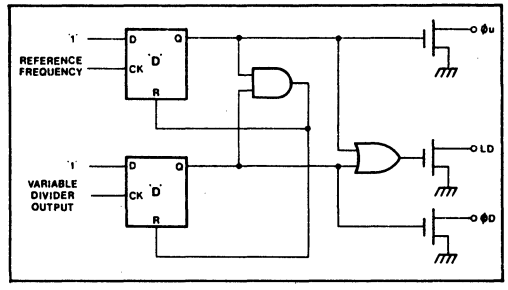



*Fig.3 Logic diagram*

### Data Selection

To programme the synthesiser the following information is required:

1. The reference comparison frequency—typically equal to the channel spacing.
2. The frequency of the VCO.

The frequency programme information is presented to the device in multiplexed form. The reading of this data by the device is controlled by the two data select outputs from the device. This sequence is shown in Fig.4.

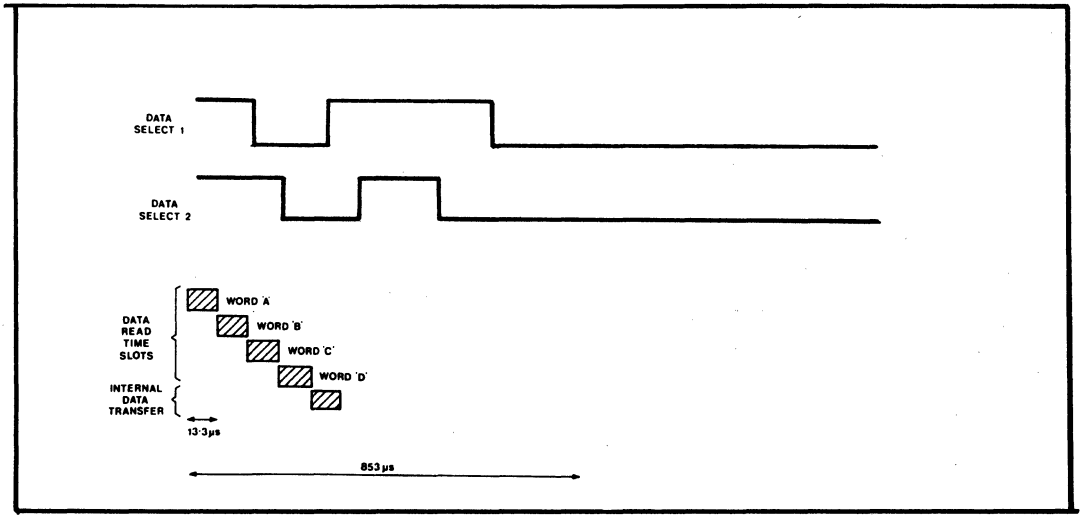



*Fig.4 Data Read timing diagram*

| FB/FA | GND | O/C | DS1 | DS2 |
|---|---|---|---|---|
| Gnd | 20 | 10 | 5 | 2.5 |
| O/C | 25 | 12.5 | 6.25 | 3.125 |
| DS1 | 30 | 15 | 7.5 | 3.75 |
| DS2 | 37.5 | 18.75 | 9.375 | 4.6875 |

*Table 1 Reference frequency selection (all frequencies in kHz)*

| Channel Spacing | 20kHz | 25kHz | 30kHz |
|---|---|---|---|
| Low Range (MHz) | 32.0—(225) | 40.0—(225) | 48.0—(225) |
| High Range (MHz) | 134.4—(225) | 168.0—(225) | |

| Channel Spacing | 10kHz | 12.5kHz | 15kHz |
|---|---|---|---|
| Low Range (MHz) | 16.0—118.4 | 20.0—148.0 | 24.0—177.6 |
| High Range (MHz) | 67.2—169.6 | 84.0—(212) | 100.8—(225) |

| Channel Spacing | 5kHz | 6.25kHz | 7.5kHz |
|---|---|---|---|
| Low Range (MHz) | 8.0—59.2 | 10.0—74.0 | 12.0—88.8 |
| High Range (MHz) | 33.6—84.8 | 42.0—106.0 | 50.4—127.2 |

| Channel Spacing | 2.5kHz | 3.125kHz | 3.75kHz |
|---|---|---|---|
| Low Range (MHz) | 4.0—29.6 | 5.0—37.0 | 6.0—44.4 |
| High Range (MHz) | 16.8—42.4 | 21.0—53.0 | 25.2—63.6 |

*Table 2 Frequency programme range*

To calculate the Programme number for a given VCO frequency and channel spacing the following equation is used:

$$\text{Programme Number } N = \frac{1000 \times f}{C} - R$$

where f = VCO frequency in MHz
C = channel spacing in kHz
R = range number (R = 1600 range = 1)
(R = 6720 range = 0)

The programme number is converted to a 14 bit binary number and is segregated as 3 words of 4 bits and 1 word of 2 bits.

The least significant word is first entered during the Data Read 1 time slot via the inputs $D_3$, $D_2$, $D_1$ and $D_0$ and the most significant last (Data Read 4 time slot).

The second least significant word contains only two bits entered via the inputs $D_1$ and $D_0$. Data presented to the inputs $D_2$ and $D_3$ during the second time slot is ignored by the NJ8812.

For example, with a VCO frequency of 121.2MHz and channel spacing of 50.0kHz

f = 121.2
C = 50.0
R = 1600
N = 824

Conversion to a 14-bit binary number is performed as follows:

| | Result |
|---|---|
| 1. Divide by 640 | 1.2875 |
| 2. Write down number before decimal place (WORD 'D') | 1 |
| 3. Subtract this number | 0.2875 |
| 4. Multiply by 16 | 4.60 |
| 5. Write down number before decimal place (WORD 'C') | 4 |
| 6. Subtract this number | 0.60 |
| 7. Multiply by 40 | 24.0 |
| 8. Write down nearest whole number (WORD 'A + B') | 24 |

The three decimal numbers obtained may now be directly converted to binary, and these are presented to the data inputs as shown in Table 3.

| DS1 | DS2 | $D_3$ | $D_2$ | $D_1$ | $D_0$ | |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | 0 | 0 | WORD 'A' |
| 0 | 0 | X | X | 0 | 1 | WORD 'B' |
| 1 | 0 | 0 | 1 | 0 | 0 | WORD 'C' |
| 1 | 1 | 0 | 0 | 0 | 1 | WORD 'D' |

*Table 3*

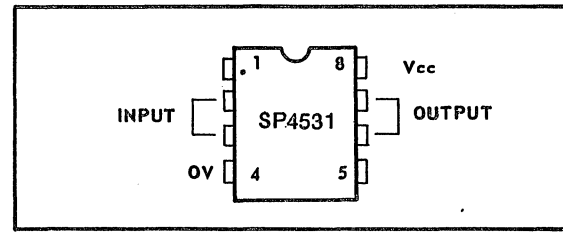
The data may be latched internally by grounding the DS2 output. This is useful when interfacing to a microprocessor. The NJ8812 is also compatible with most types of PROM and ROM for data coding applications.

# SP4531

## VHF/UHF ÷64 PRESCALER

The SP4531 is one of the new range of Plessey Consumer high speed dividers which offer improved input sensitivity and input impedance characteristics.

The device is intended for use in television frequency synthesis systems. It has a division ratio of 64 with dual ECL outputs and incorporates an on–chip preamplifier with a differential input. The input pins may be used as UHF and VHF inputs with a slight loss of sensitivity if suitable drive circuitry is employed.




### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, $V_{CC}$ | +7V |
| Input voltage | 2.5V p–p |
| Ambient operating temperature | –10°C to 65°C |
| Storage temperature | –55°C to 125°C |

### FEATURES

- On–chip wideband amplifier
- High input sensitivity
- High input impedance
- Low output radiation
- Complementary ECL output

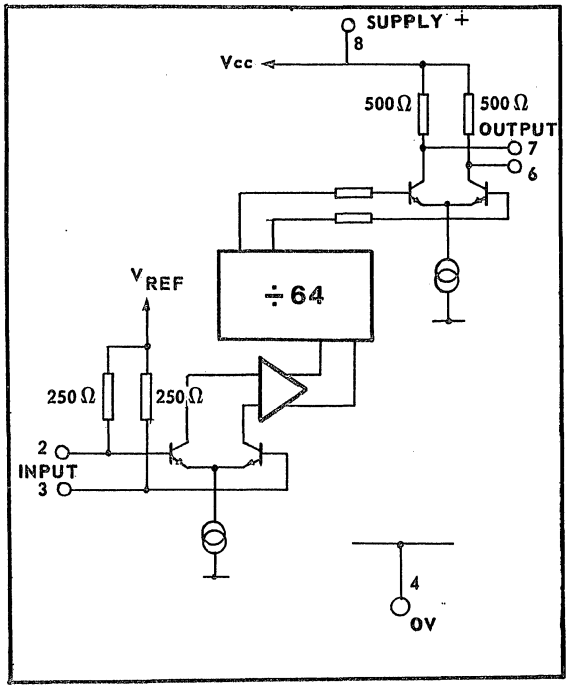



Fig. 2. Block Diagram

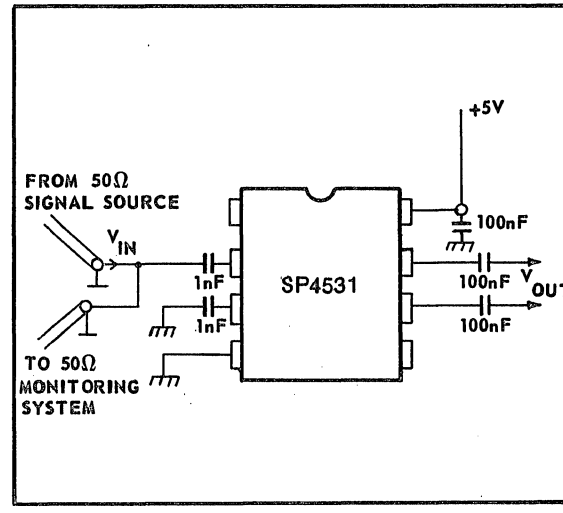


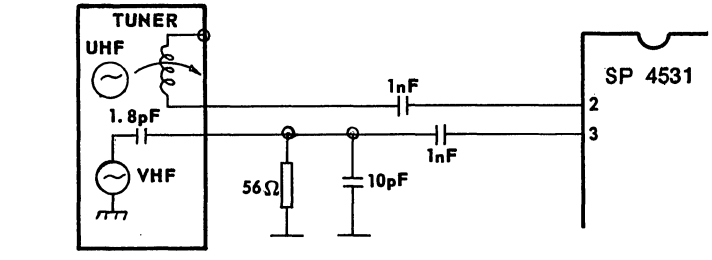

Fig. 3. Test Circuit

## ELECTRICAL CHARACTERISTICS

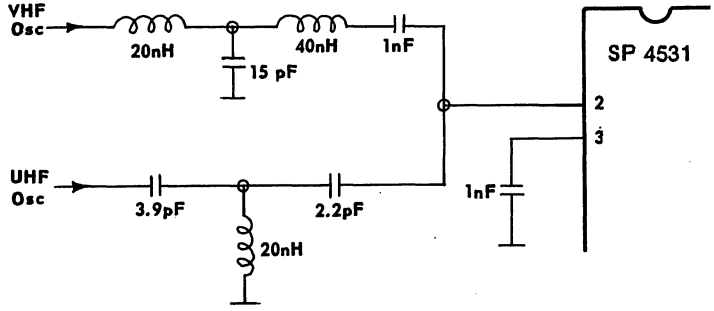
Test Conditions (unless otherwise stated) –

Tamb.= +25 C, Vcc = +5V

| Characteristic | | Pin | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Operating voltage range | | 8 | 4.5 | 5 | 5.5 | V | |
| Supply current | | 8 | | 75 | 95 | mA | |
| Input voltage | 80MHz | 2 | 35 | | 200 | mV | |
| | 300MHz | 2 | 20 | | 200 | mV | rms, sine wave |
| | 500MHz | 2 | 20 | | 200 | mV | with 1nF decoupling |
| | 700MHz | 2 | 20 | | 200 | mV | On pin 3 |
| | 950MHz | 2 | 20 | | 150 | mV | |
| Output voltage | | 6 | 0.8 | | | V | peak–peak, no load |
| | | 7 | 0.8 | | | V | |
| Output Imbalance | | 6,7 | | | 0.1 | V | |
| Output impedance | | 6 | | 500 | | Ω | |
| | | 7 | | 500 | | Ω | |




(a) DUAL INPUT




(b) 'T' INPUT

Oscillators should not be operated simultaneously.

*Fig. 4. Combined Input Operation.*

# SP4550/51

## 1GHz ÷ 256

The SP4550/1 are part of the new range of Plessey Consumer high speed dividers which offer improved input sensitivity and higher input impedance.

The devices are intended for use in television frequency synthesis systems. They have a division ratio of 256 with a single, (SP4550) or complimentary, (SP4551) ECL output and incorporate an on–chip pre-amplifier with a differential input. The input pins may be used as UHF and VHF inputs with a slight loss of sensitivity if suitable drive circuitry is employed.

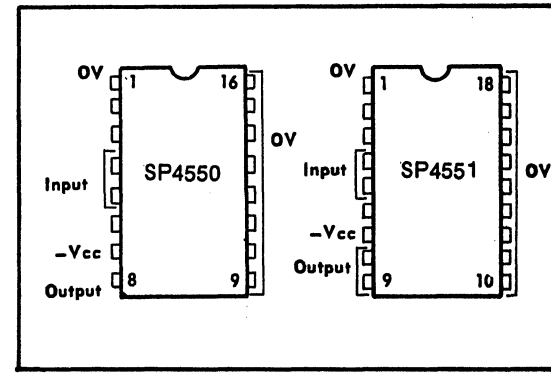



*Fig. 1. Pin Connections*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | +7V |
| Input voltage | 2.5V p–p |
| Ambient operating temperature | –10 °C to 65 °C |
| Storage temperature | –55 °C to 125 °C |

### FEATURES

- On–chip wideband amplifier
- High input sensitivity
- High input impedance
- Low output radiation
- Single (SP4550) or complimentary (SP4551) ECL output

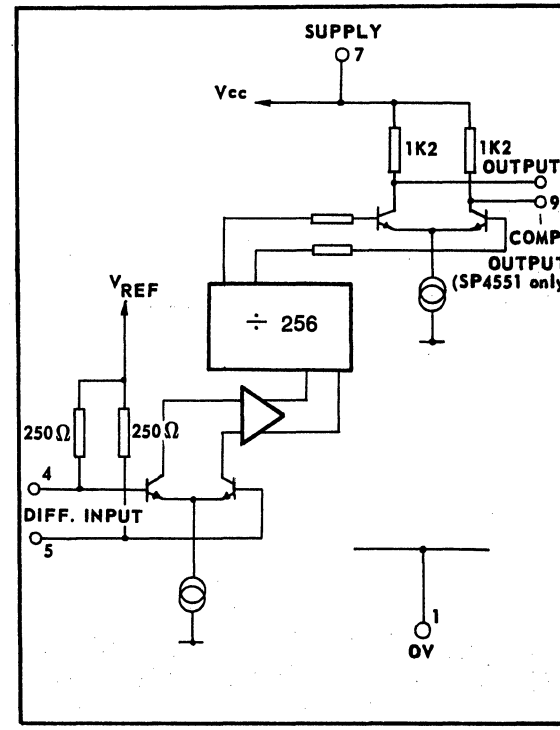



*Fig. 2. SP4550/1 Block Diagram*

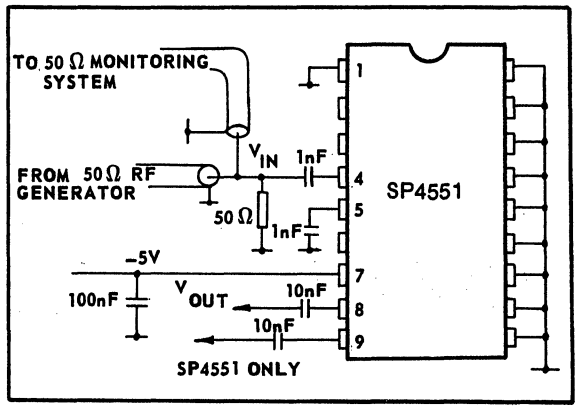



*Fig. 3. Test Configuration.*

## ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated);–

Tamb = +25 C, V cc = +5V

| Characteristic | | Pin | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Operating voltage range | | 7 | 4.5 | 5 | 5.5 | V | |
| Supply current | | 7 | | 60 | 90 | mA | |
| Input voltage | 80MHz | 4, 5 | 35 | | 200 | mV | rms, sine wave |
| | 300MHz | | 20 | | 200 | | |
| | 500MHz | | 20 | | 200 | | |
| | 700MHz | | 20 | | 200 | | |
| | 950MHz | | 20 | | 200 | | |
| Output voltage | | 8 | 0.8 | | | V | peak–peak, no load |
| | | 9 | 0.8 | | | V | SP4551 only |
| | Imbalance | 8,9 | | | 0.1 | V | SP4551 only |
| Output impedance | | 8 | | 1.2 | | KΩ | |
| | | 9 | | 1.2 | | KΩ | SP4551 only |

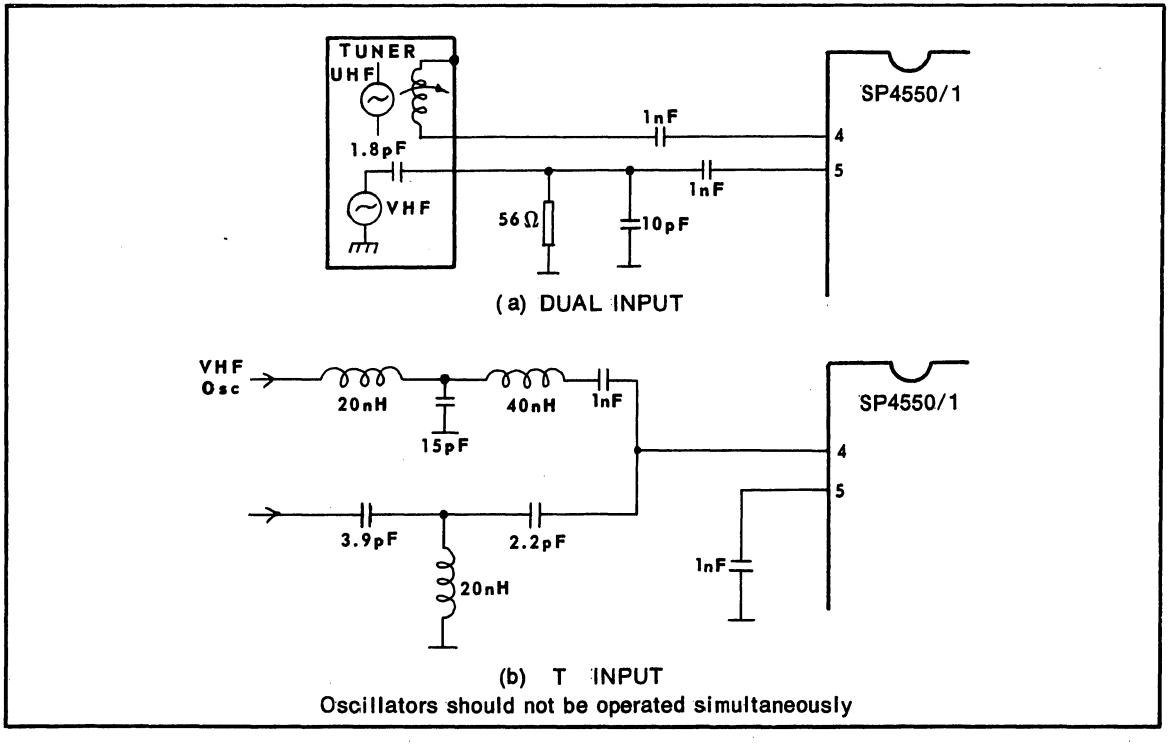



*Fig. 4. Combined Input Operation.*

# SP4541

## VHF/UHF ÷ 256 PRESCALER

The SP4541 are ECL divide by 256 which will operate at frequencies in excess of 950 MHz, and are intended for use as a prescaler in television receiver synthesiser tuners.

The device has a typical power dissipation of 300 mW at the nominal supply voltage of 5.0.

## OPERATING NOTES

The input is terminated by a nominal 800Ω and should be AC coupled to the signal source. Input power to the device is terminated to ground by the decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1 GHz.

The **SP4541** output is designed to interface with TTL which has a common $V_{EE}$ (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power/Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when one of the clock inputs changes from a low to a high level.

The **SP4541** output is designed to provide complementary emitter follower O/Ps so that the rise time of the output can be adjusted to suit system requirements.

## FEATURES

- 5.0 Volt Operation
- Self-Biasing Clock Inputs
- Input Dynamic Range of 10mV to 600mV p-p Over Entire Frequency Range
- Variable Input Hysteresis Capability for Wide Band Operation
- Push – Pull TTL O/P

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $V_{CC} - V_{EE}$ | 0V to +10V |
| Input voltage, clock inputs | 2.5V p-p |
| Output current | +30 mA to -30 mA |
| Operating junction temperature | +150°C |
| Storage Temperature | -55°C to +150°C |

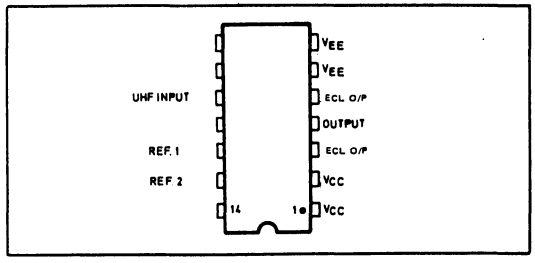



Fig. 1 – Pin connections

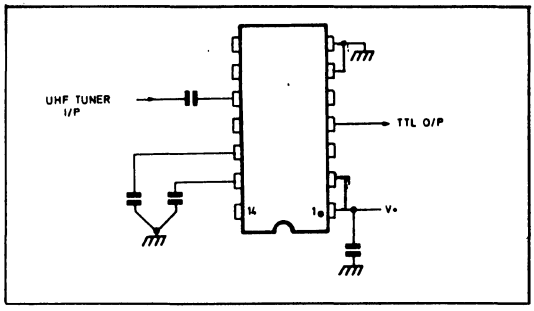



Fig. 2 – Typical appoication

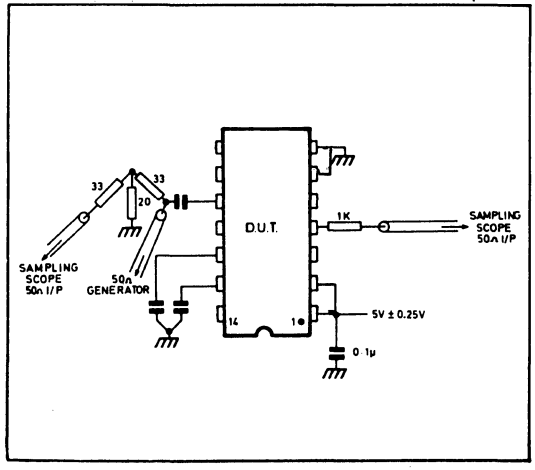


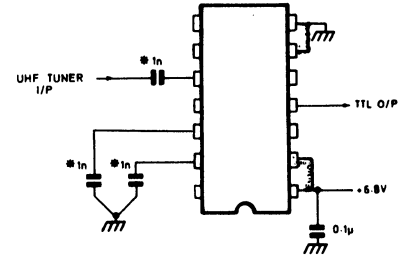

Fig. 3 – AC test circuit

## ELECTRICAL CHARACTERISTICS

Supply voltage: 5.0 ± 0.25V
Supply current: 60 mA typ.
90 mA max
Temperature range: 0°C to 70°C
Clock inputs: AC coupled, self-biasing via 800Ω

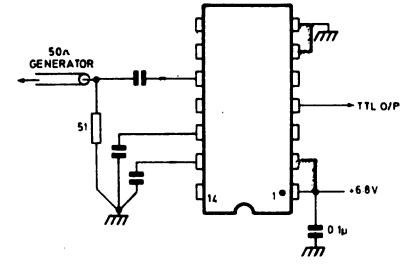
Test conditions (unless otherwise stated):
Supply voltage: $V_{EE}$ = 0V, $V_{CC}$ = 5.0V ±0.25
Clock input voltage: 10mV to 600mV p-p
$T_{amb}$ 5°0 to + 70°C

| Characteristics | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Clock Inputs | | | | | |
| Max. I/P frequency | 950 | 1100 | | MHz | |
| Min. I/P frequency | | | 80 | MHz | |
| Output SP 4140 | | | | | |
| Low Level | 0 | | 0.45 | V | 3 mA sink $V_{CC}$ = 5.0V |
| High Level | 3.8 | | 4.6 | V | -1mA source $T_{amb}$ 25°C |
| Output SP4150 | | | | | |
| Voltage Swing | 600 | 800 | | mV | No load each output |
| Supply Current | | 60 | 90 | mA | $V_{CC}$ = 5V |




Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

Fig. 4 — Application circuit




Capacitors are 1 nf unless otherwise stated. Values should be increased if operation below 10 MHz is desired.

Fig. 5 — Wideband operation

## PACKAGE DETAILS

The SP 4541 is packaged in 14-lead DIP.

Plessey Semiconductors

# SP8000 SERIES
## HIGH SPEED DIVIDERS

# SP8600A&B
## 250MHz ÷ 4 COUNTER

The SP8600 is a fixed ratio emitter coupled logic ÷4 counter with a specified input frequency range of 15—250 MHz. The operating temperature range is specified by the device code suffix letter: 'A' denotes −55°C to +125°C, 'B' denotes 0°C to +70°C operation,

Intended for use with an external bias arrangement and capacitive coupling to the signal source, the SP8600 can be either single driven, or double driven with two complementary input signals.

The outputs are complementary free collectors that can have their load resistors taken to any bias voltage up to 12V more positive than $V_{EE}$.

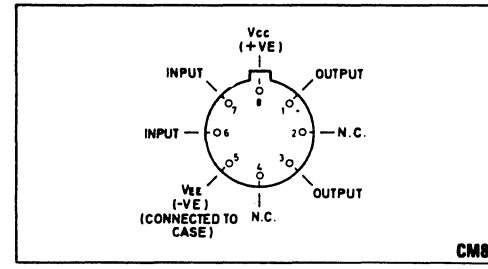



*Fig. 1 Pin connections (bottom view)*

### FEATURES

- Low Power
- Free Collector Outputs to Interface to TTL
- 250 MHz ÷ 4 Over Full Military Temp. Range

### APPLICATIONS

- Synthesizers — Mobile and Fixed
- Counters
- Timers

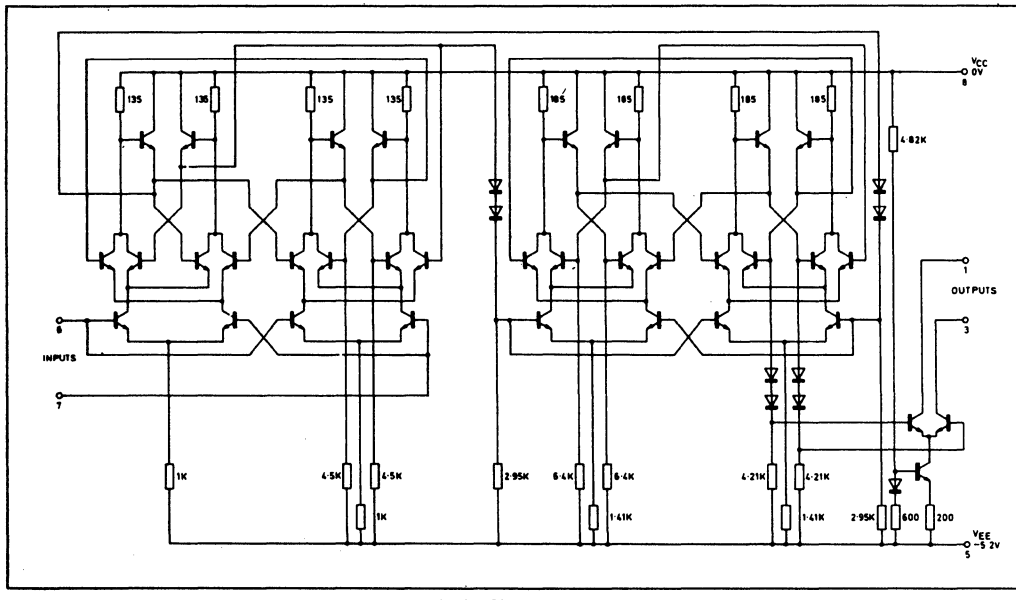



*Fig. 2 Circuit diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$: 'A' grade —55°C to +125°C
'B' grade 0°C to +70°C

Supply voltage 0V
−5.2V

Input voltage (single driven — other input decoupled to ground plane) $V_{CC}$ 400 to 800 mV p-p
Input voltage (double complementary input drive) $V_{EE}$ 250 to 800 mV p-p
Input bias voltage Bias chain as in test circuit (see Fig. 3 and operating notes).

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Max. input frequency | 250 | 390* | | MHz | Typical figure quoted at +25°C. |
| Min. input frequency with sinusoidal input | | | 25 | MHz | |
| Min. slew rate of square wave input for correct operation | | | 20 | V/μs | Single input drive |
| Output current | 1.6 | | | mA | Input f=250 MHz. |
| Power supply drain current | | 16* | 25 | mA | $V_{EE}$ = −5.2V, $V_{BIAS}$ as Fig. 3. |

*At +25°C

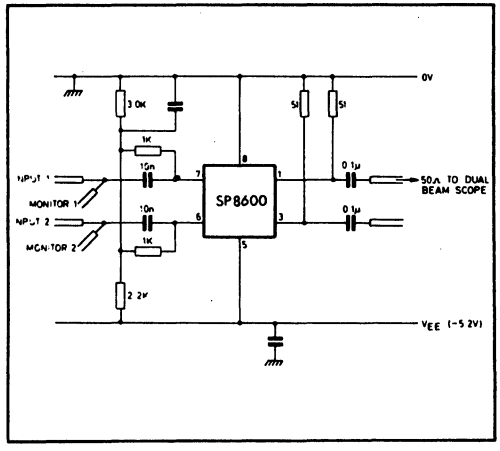



*Fig. 3 Test circuit*

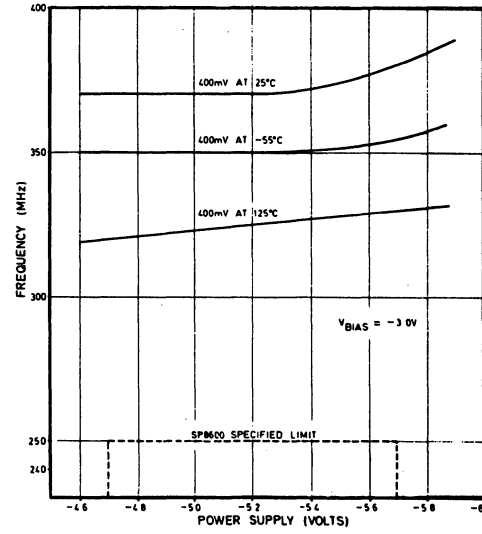



*Fig. 4 Maximum input frequency v. power supply voltage (typical)*

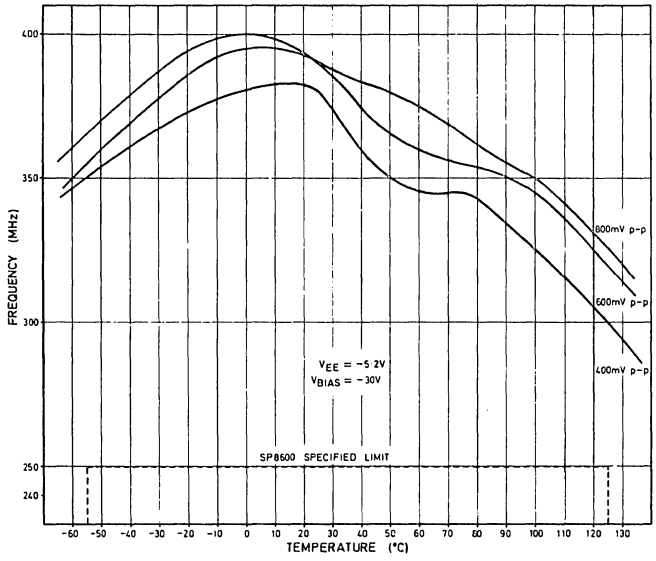



*Fig. 5 Maximum input frequency v. temperature*

## OPERATING NOTES

The circuit performance obtained from the SP8600 is optimized if normal high frequency rules for circuit layout are obeyed — leads should be kept short, capacitors and resistors should be of non-inductive types, etc.

The signal source is normally AC coupled to one of the inputs or, if complementary signals are available, to both inputs. The inputs require an external bias chain to set the DC potential on the inputs (see Fig. 3). No appreciable change in performance is observed over a range of DC bias from –2.5V to –3.5V.

Any tendency for the circuit to self-oscillate in the absence of input signal (or when the input signal is very small) can be overcome by offsetting the two inputs by approximately 40mV, using, for example, the bias arrangement shown in Fig. 6. The input wave form may be sinusoidal, but below 25 MHz incorrect operation may occur because of the limited slew rate of the input signal. A square wave input with a slew rate greater than 20V/μs ensures correct operation down to DC.

The output is in the form of complementary free collectors with at least 2mA available from them. For satisfactory high frequency interfacing to ECL or Schottky TTL the circuit techniques illustrated in Fig. 7 are recommended.

For maximum frequency operation, it is essential that the output load risistor values be such that the output transistors do not saturate. If the load resistors are connected to the 0V rail, then saturation can occur with resistance values greater than 600Ω. Of course, if the load resistors are taken to a more positive potential, then higher values can be used. N.B. If only one output is used, the other output should be connected to 0V.

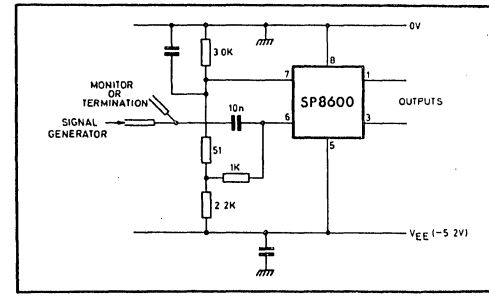



*Fig. 6 Bias arrangement to prevent self-oscillation under no-signal conditions*

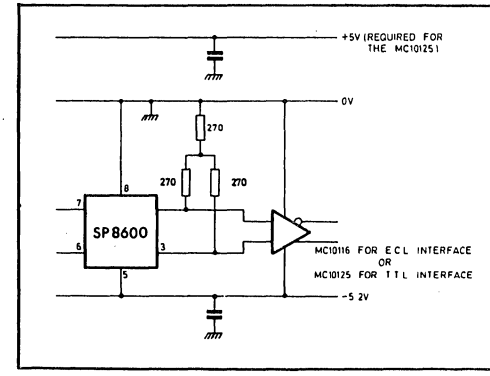



*Fig. 7 ECL qnd Schottky TTL interfacing*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $V_{CC}$—$V_{EE}$ | 10V |
| Input voltage $V_{IN}$ | Not greater than supply voltage in use |
| Bias voltage on o/p's $V_{OUT}$—$V_{EE}$ | 14V |
| Operating junction temperature | +175°C max. |
| Storage temperature | —55°C to +175°C |

Plessey Semiconductors

# SP8000 SERIES

## HIGH SPEED DIVIDERS

# SP8601A & B

## 150MHz÷4

The SP8601 is a fixed ratio emitter coupled logic ÷4 counter with a maximum specified input frequency of 150 MHz but with a typical maximum operating frequency well in excess of this (see Typical Operating Characteristics). The operating temperature range is specified by the final coding letter: 'A' denotes −55 °C to +125 °C, 'B' denotes 0 °C to +70 °C.

The SP8601 can be operated with single input drive or with double, complementary, I/P drive. It can be driven with direct coupling from ECL II levels (or from an SP8602 device), or it can be capacitively coupled to the signal source if an external bias is provided.

There are complementary free collector outputs that can have their external load resistor connected to any bias up to 12 volts more positive than $V_{EE}$.

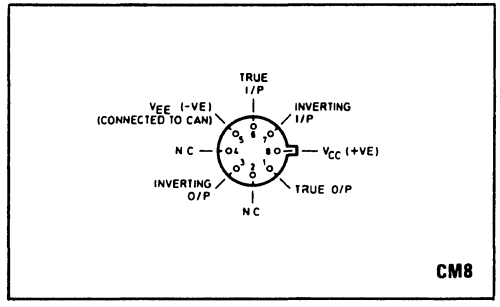



*Fig. 1 Pin connections (bottom view)*

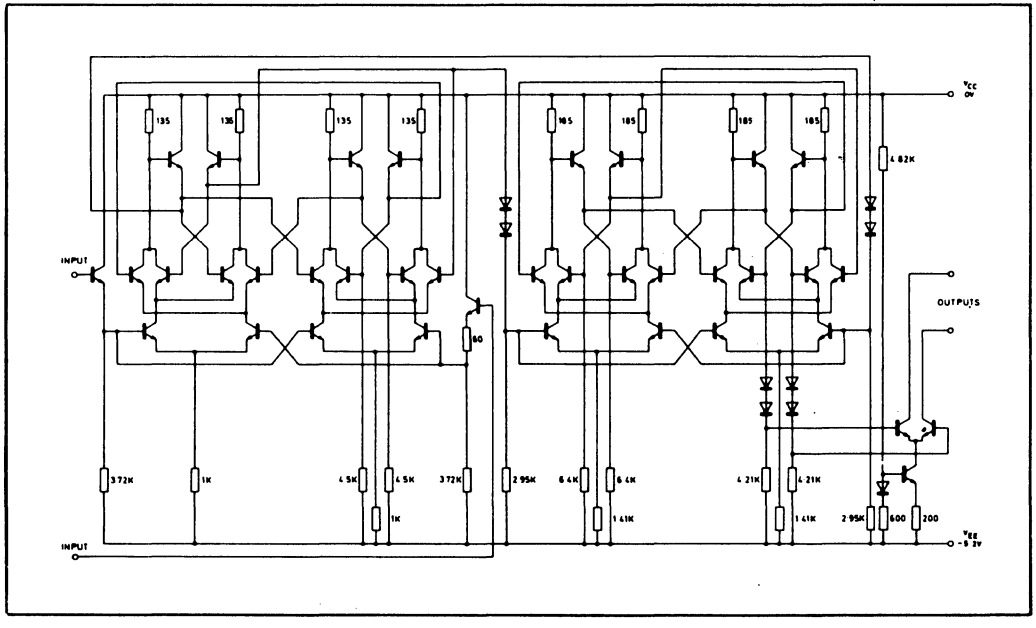



*Fig. 2 Circuit diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

| | |
|---|---|
| $T_{amb}$: 'A' grade | −55°C to +125°C |
| 'B' grade | 0°C to +70°C |
| Operating supply voltage $V_{CC}$ | 0V. |
| $V_{EE}$ | −5.2V ±0.25V |
| Input voltage (single drive — other input decoupled to ground plane) | 400 to 800 mV (p-p) |
| Input voltage (double drive) | 250 to 800 mV (p-p) |
| Bias voltage | Bias chain as in test circuit (see Fig. 2). |

| Characteristic | Value Min | Value Typ. | Value Max. | Units | Conditions |
|---|---|---|---|---|---|
| Max. input frequency | 150 | | | MHz. | |
| Min. input freq. with sinusoidal input. | | | 15 | MHz. | |
| Min. slew rate of square wave input for correct operation | | | 20 | V/μs | Single input drive |
| Output current | 1.6 | | | mA | Input freq. = 150 MHz. $R_{load}$ = 50Ω |
| Power supply drain current | | 18 | 25 | mA | $V_{EE}$ = −5.2V |

## OPERATING NOTES

Circuit performance obtained from the SP8601 is optimised if normal high frequency rules for circuit layout are obeyed — leads should be kept short, capacitors and resistors should be of non-inductive types, etc.

The signal source is normally directly coupled into the device, which will tolerate a wide range of input bias voltages, but was designed for inputs from ECL II levels and can therefore be satisfactorily driven from SP8602 range of counters. The bias voltage on the input marginally affects the overall power consumption of the device (For typical operating characteristics with varying bias voltages see Fig. 4).

If it is not practicable to directly couple the input signal, then a bias chain similar to the one shown in Fig. 3 can be used.

The input waveform may be sinusoidal, but below about 10 MHz incorrect operation may occur because of the limited slew rate of the input signal. A square wave input with a slew rate of greater than 20 V/μs ensures correct operation down to DC.

The output is in the form of complementary free collectors with 2 mA min. available from them. The output voltage swing obviously depends on the value of load resistor used and also the frequency of operation. The following table gives some typical examples of output voltage for different load resistors. With careful board layout to minimise capacitance these figures can easily be exceeded.

| Min. Output Voltage | Load Resistor | Input Frequency |
|---|---|---|
| 1.1V | 1kΩ | 120 MHz |
| 320mV | 200Ω | 150 MHz |
| 80mV | 50Ω | 180 MHz |

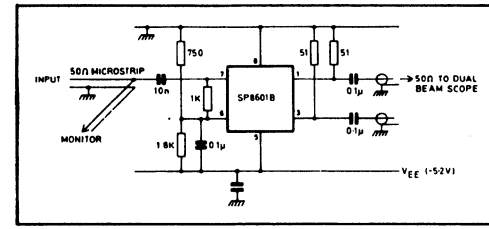
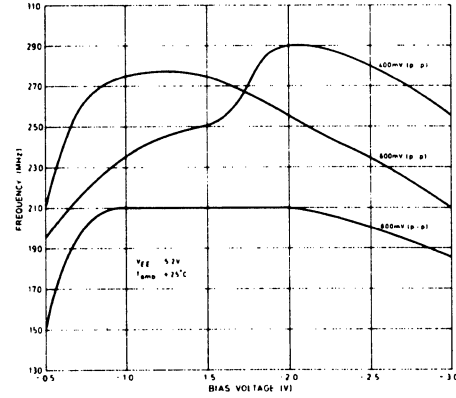



*Fig. 3 Test circuit*

## TYPICAL OPERATING CHARACTERISTICS




NOTE: The value of the coupling and decoupling capacitors used are uncritical but they should be of a type and value suitable for the frequencies involved.

*Fig. 4 Maximum input frequency v. bias voltage at single input drive levels of 400, 600 and 800 mV (typical device)*

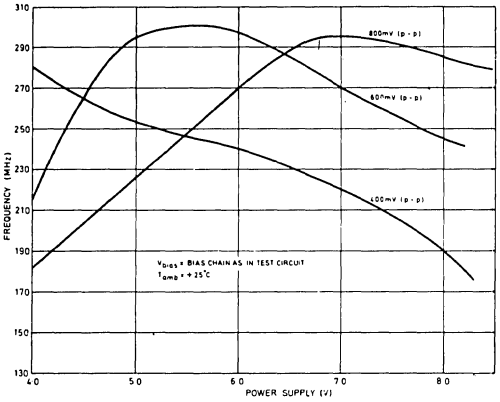



*Fig. 5 Maximum frequency v. power supply voltage at single input drive levels of 400, 600 and 800 mV (typical device)*

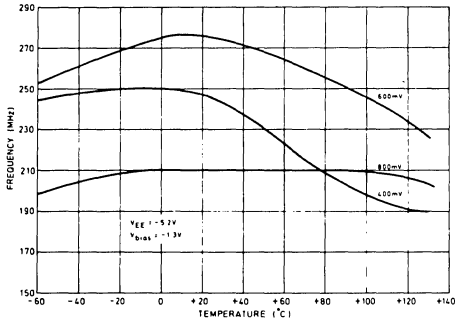



*Fig. 6 Maximum input frequency v. temperature at single input drive levels of 400, 600 and 800 mV (typical device)*

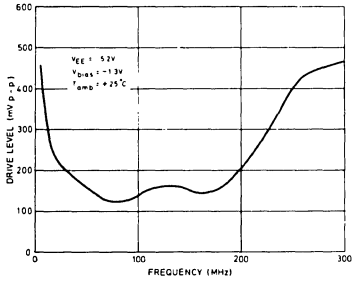



*Fig. 7 Minimum single input drive level for correct operation v. input frequency (typical device)*

## APPLICATION NOTES

The SP8601 used with two SP8602 series ÷2 counters to give a 500 MHz divide-by-sixteen prescaler is shown in Fig. 8. Capacitors marked thus * may need to be increased in value for low frequency operation.

For correct operation when interfacing with TTL and ECL II the circuits shown in Figs. 9, 10 and 11 are recommended.

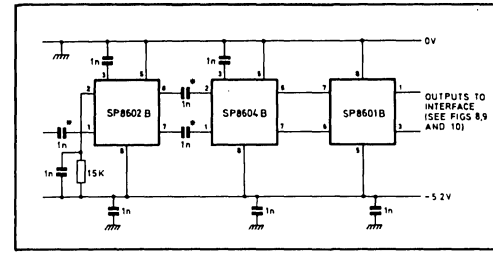



*Fig. 8 Divide-by-sixteen prescaler*

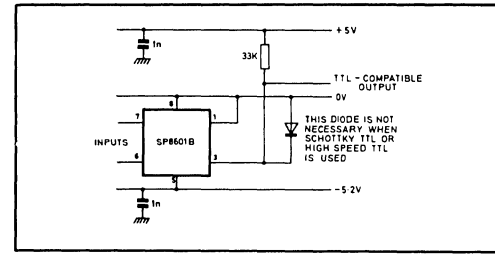



*Fig. 9 TTL interface (fanout = 1 TTL gate)*

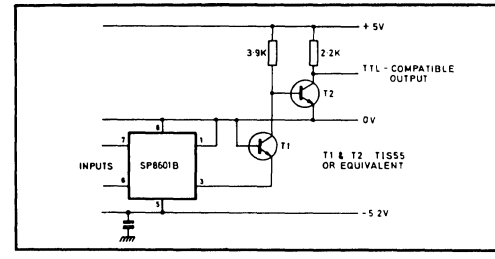



*Fig. 10 High fanout TTL interface*

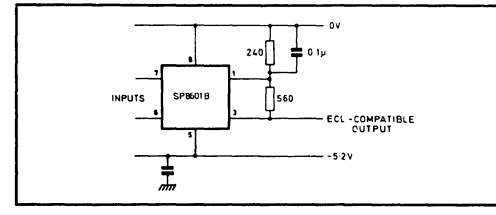



*Fig. 11 ECL II interface*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $V_{CC}$—$V_{EE}$ | 10 V |
| Input voltage $V_{in}$ | Not greater than the supply voltage in use |
| Bias voltage on outputs $V_{out}$—$V_{EE}$ (see Operating Notes) | 14 V |
| Operating junction temperature | +175°C |
| Storage temperature | −55°C to +175°C |

# SP8602 A&B

## 500MHz÷2

The SP8602 is a fixed ratio ECL-2 counters with maximum specified I/P frequencies of 500. MHz. The operating temperature range is specified by the final coding letter: 'A' denotes −55°C to +125°C, 'B' denotes 0°C to +70°C.

The device can be operated with single input drive or with double, complementary, input drive; in both cases the input is normally capacitively coupled to the signal source. Two complementary emitter follower outputs are provided.

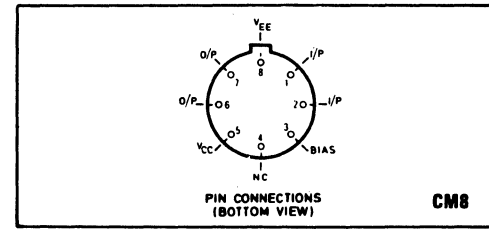



*Fig. 1 Pin connections*

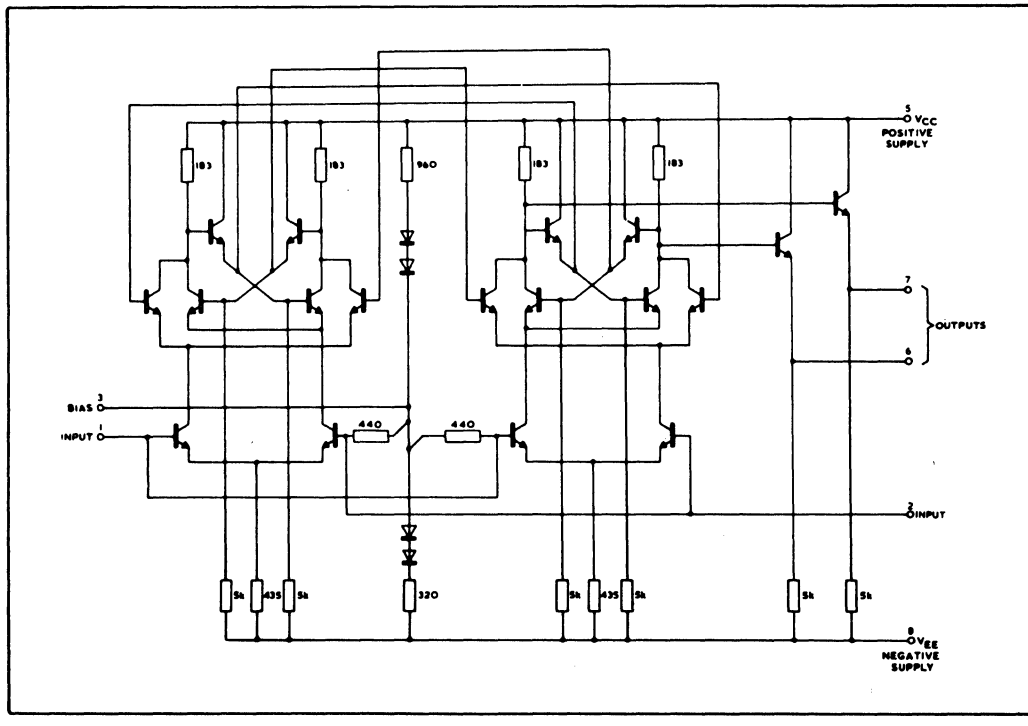



*Fig. 2 Circuit diagram (all resistor values are nominal)*

## ELECTRICAL CHARACTERISTICS

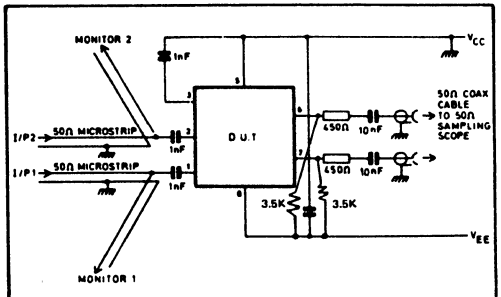
**Test conditions (unless otherwise stated)**

| | |
|---|---|
| $T_{amb}$ 'A' Grade | −55°C to +125°C |
| 'B' Grade | 0°C to +70°C |
| Operating supply voltage: $V_{cc}$ | 0V |
| $V_{ee}$ | −5.2V± 0.25V |
| Input voltage (single drive- other input and bias decoupled to ground plane) | 400 to 800 mV p-p |
| Input voltage (double drive- bias decoupled to ground plane) | 250 to 800 mV p-p |
| Output load | 500Ω and 3pF |

| Characteristic | Type | Value | | | | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | |
| Max. input freq. | SP8602A,B. | 500 | | | MHz | $V_{ee}$ = −5.2V |
| Min. input freq. with sinusoidal input | | | 20 | 40 | MHz | |
| Min. slew rate of square wave input for correct operation | | | 30 | 100 | V/μS | single input drive |
| Output voltage swing | | 400 | | | mV | $V_{ee}$ = −5.2V<br>$T_{amb}$ = −55°C to +70°C |
| Output voltage swing | | 350 | | | mV | $V_{ee}$ = −5.2V<br>$T_{amb}$ = +125°C<br>I/P freq. = 500 MHz |
| Power supply drain current | | | 12 | 20 | mA | $V_{ee}$ = −5.2V See note 1 |

NOTES

1. In practice, the 3.5kΩ resistors specified in the test circuit (Fig.3) are not essential; omission of these resistors will reduce the maximum supply current to 18mA.




Note: The values of the coupling and decoupling capacitors used are uncritical but they should be of a type and value suitable for the frequencies involved.

*Fig. 3 Test circuit*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $V_{cc} - V_{ee}$ | 8V |
| Input voltage $V_{in}$ | Not greater than the supply voltage in use |
| Output current $I_{out}$ | 10 mA |
| Operating junction temperature | +150°C |
| Storage temperature range | −55°C to +150°C |

## OPERATING NOTES

It is recommended that a positive earth plane be used for the circuit layout, thus preventing damage if the output emitter-followers are inadvertently shorted to ground. All components used in the circuit layout should be suitable for the frequencies involved, and outside a controlled impedance environment, leads and connections should be kept short to minimise stray inductance.

The signal source is normally capacitively coupled to the input. A 1000pF capacitor is usually sufficient. If the input signal is likely to be interrupted a 15KΩ resistor should be connected between the input and the negative rail. In the single drive case it is preferable to connect the resistor to the input not in use – in the double drive case either input can be used. The addition of the input pulldown resistor causes a slight loss of input sensitivity, but it prevents circuit oscillation under no-signal conditions.

The input waveform may be sinusoidal, but below about 40 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than the amplitude. A square wave input with a slew rate of more than 100 V/μS will permit correct operation down to DC.

The output voltage swing can be increased by the addition of a DC load to the output emitter followers. Pulldown resistors of 1.5 K to the negative rail provide an increase of typically 25% in the output voltage swing.

## APPLICATION NOTES

### SP8602B interfacing to E C L 10 000 and E C L III

By increasing the output voltage swing using external pulldown resistors (see operating notes), the SP8602B can be coupled directly into an E C L III or E C L 10 000 gate, but there is a reduction of the noise immunity. Where noise immunity is important the device can be connected to an E C L 10 000 or E C L III line receiver.

### Divide-by-16 frequency scaler.

The SP8602B interfacing with the SP8601B and high-speed TTL to give a divide-by-16 frequency scaler is shown in Fig. 4.

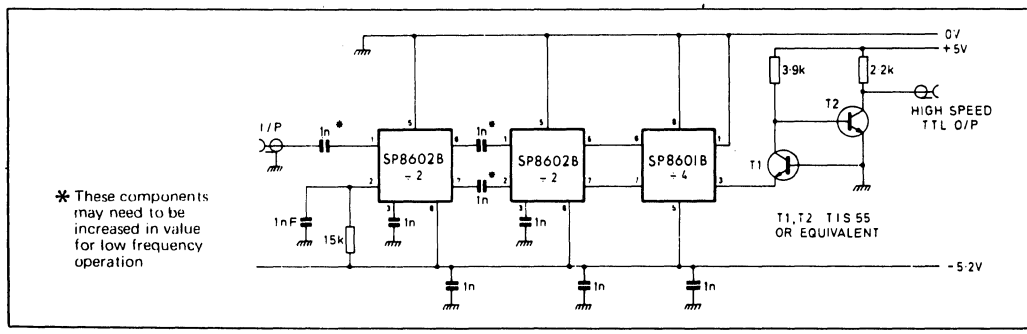



*Fig. 4 Divide-by-16 frequency scaler*

# SP8605 B & M 1.0GHz ÷ 2
# SP8606 B & M 1.3GHz ÷ 2

The SP8605/6 UHF counters are fixed ratio ÷ 2 asynchronous emitter coupled logic counters with, in the case of the SP8606 a maximum operating frequency in excess of 1.3GHz, over a temperature range of 0° C to 70° C (B Grade) and —40° C to + 85° C (M Grade). The input is normally capacitively coupled to the signal source but can be DC coupled if it is required. The two complementary emitter follower outputs are capable of driving 100-ohm lines and interfacing to ECL with the same positive supply. The SP8605/6 require supplies of OV and —5.2V (± 0.25V).

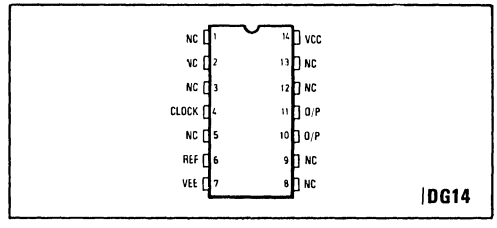



*Fig. 1 Pin connections*

## FEATURES

- DC to 1.3GHz Operation
- 0°C to 70°C (B Grade) and —40°C to +85°C (M Grade) Operation Guaranteed at Maximum Specified Frequency and Over a Wide Dynamic Input Range.
- Complementary Emitter Follower O/Ps.
- ECL III Compatible.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | $\|V_{CC} - V_{EE}\|$ 10V |
| Input voltage | $V_{INac}$ 2.5V p — p |
| Output current | 15mA |
| Storage temperature range | —55° C to + 150° C |
| Maximum operating junction temperature | + 150° C |

## APPLICATIONS

- UHF Instrumentation, including Counters and Timers.
- Prescaling for UHF Synthesisers.

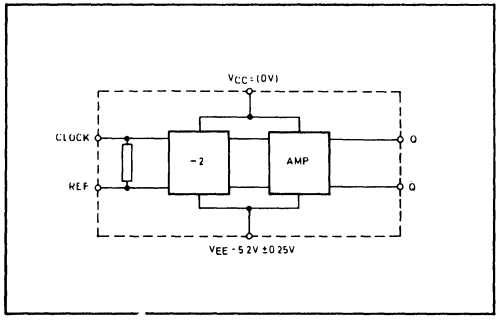



*Fig. 2 Functional diagram*

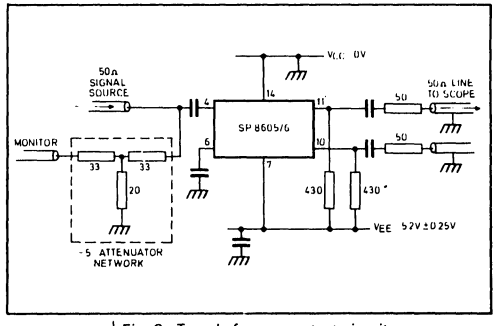



*Fig. 3 Toggle frequency test circuit*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$: B Grade 0° C to +70° C
M Grade −40° C to +85° C
Supply voltage $V_{CC}$ = 0V
$V_{EE}$ = −5.2V ± 0.25 V
Input voltage 400 — 1000mV p — p

| Characteristic | Type | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max. toggle frequency | SP8606B<br>SP8605B | 1.3<br>1.0 | | | GHz<br>GHz | |
| Min. toggle frequency for correct operation with sine wave input | All | | | 150 | MHz | $V_{IN}$=600mv to 1.0v p-p |
| Min. slew rate for sq. wave input to guarantee operation to 0Hz. | All | | | 200 | V//us | |
| Output voltage swing | All | 500 | 600 | | mV | 430 Ω to $V_{EE}$ |
| Power supply drain current | All | | 70 | 100 | mA | $V_{EE}$=−5.45V, No load |

TOGGLE FREQUENCY TEST BOARD LAYOUT
1. All connections to the device are kept short.
2. The capacitors are leadless ceramic types.
3. In practice, the device is tested in an Augat 14 lead DIL socket which degrades the performance slightly. If the device is mounted in a low profile socket or soldered into a printed circuit board, the specified performance will be exceeded.

## OPERATING AND APPLICATION NOTE

The SP8605/6 dividers are very simple to use but normal high frequency rules should be followed for optimum performance, for example, all connections should be kept short, the capacitors and resistors should be types suitable for the frequencies involved.

The input is normally capacitively coupled to the signal source. There is an internal 400 ohm resistor connecting the input to a reference voltage; this biases the input in the middle of the transfer characteristic. The reference voltage is brought out onto pin 6, which should be decoupled to the earth plane. This decoupling completes the input signal path to the device and therefore must be very low inductance for optimum performance. The sensitivity of the device can be increased by DC coupling the input signal about earth (see Fig. 4).

$V_{CC}$ — $V_{EE}$ should be kept inside the specified 5.2 volts ± 0.25 volts but the actual value of $V_{CC}$ relative to earth is not very critical and can be varied between 2.7V and 3.3V with only a small effect on performance. A $V_{CC}$ of about 3.0V is the optimum for full temperature range operation.

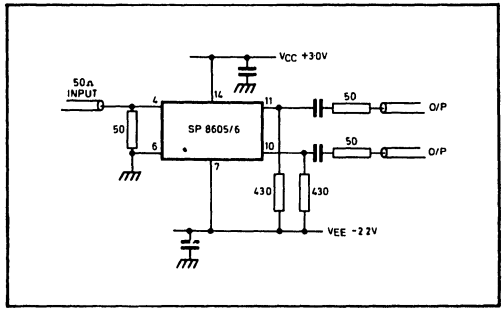



*Fig. 4 Circuit for using the input signal about earth potential*

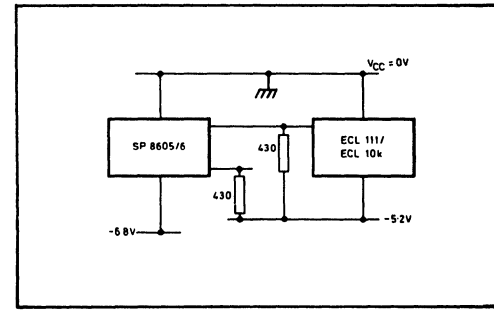



*Fig. 5 Interfacing SP8605/6 series to ECL 10K and ECL III*

In the absence of an input signal both the DC coupled and the capacitively coupled circuits will self oscillate with an output frequency of approximately 400MHz. This can be prevented by connecting a 10Kohm resistor between the input and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100mV.

The SP8605/6 will miscount with low frequency sinewave inputs of slow ramps. A slew rate of 200V//us or greater is necessary for safe operation at low frequencies.

The output can be interfaced to ECL 10K or ECL III (See Fig. 5.). The unused output should be connected to a load resistor as shown to reduce output distortion.

The input impedance of the SP8605/6 is a function of frequency and minimises at about the same frequency as the maximum input sensitivity, so, although it can load the signal source significantly there is generally enough signal to operate the device satisfactorily when the input impedance is at a minimum. The worst case occurs at the maximum frequency because this is where the input sensitivity is worst.

The SP8605/6 can be used in instrumentation for direct counting applications up to 1.3GHz and in frequency synthesisers.

Plessey Semiconductors

# SP8000 SERIES

## HIGH-SPEED DIVIDERS

# SP8607 A&B

## 600 MHz ÷ 2

The SP8607 is a divide-by-2 counter with a minimum guaranteed toggle frequency of 600 MHz over a 0°C to +70°C temperature range. The device is designed for capacitive coupling to the signal source to either of the two inputs and it has two complementary emitter follower outputs. Power dissipation is typically only 70mW with a 5.2V supply.

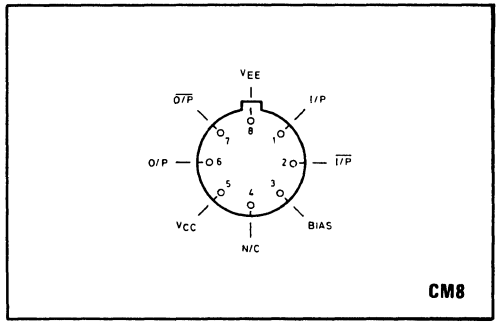



*Fig.. 1 Pin connections*

### FEATURES

- 600 MHz Operation
- −55°C to 125°C Guaranteed for 'A' grade
- Only 70mW Dissipation at 5.2V

### ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Connections as test circuit, Fig. 3
$T_{amb}$: (A grade) −55°C to +125°C
(B grade) 0°C to +70°C
Supply voltage $V_{CC}$ = 0V
$V_{EE}$ = −5.2V ± 0.25V
Specified input voltage range: 400 to 800mV p-p

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply Voltage $\lvert V_{CC} - V_{EE} \rvert$ | 8V |
| Input Voltage DC | ≤ Supply |
| Input Voltage AC | 2.5V p−p |
| Output Current | 15mA |
| Operating Junction Temp. | +150°C |
| Storage Temp Range | −55°C to + 150°C |

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min | Typ. | Max | | |
| Max. toggle frequency | 600 | 800 | | MHz | |
| Min. input frequency (sine wave) | | 50 | | MHz | |
| Min. slew rate of square wave input for correct operations to OHz | | 40 | 100 | V/μs | |
| Output voltage swing | 400 | | | mVp-p | $V_{EE}$ = −5.2V, $f_{in}$ = 600 MHz |
| Output voltage levels | | | | | |
| $V_{OH}$ | | −0.75 | | V | $f_{in}$ = OHz |
| $V_{OL}$ | | −1.5 | | V | |
| Input impedance | | 400 | | Ω | $f_{in}$ = OHz |
| O/P pulldown resistors | | 4.0 | | kΩ | |
| Bias voltage level | | −2.6 | | V | 2.7kΩ resistor from pin 3 to $V_{CC}$ |
| Power supply drain current | | 14 | 18 | V | $V_{EE}$ = −5·2V |

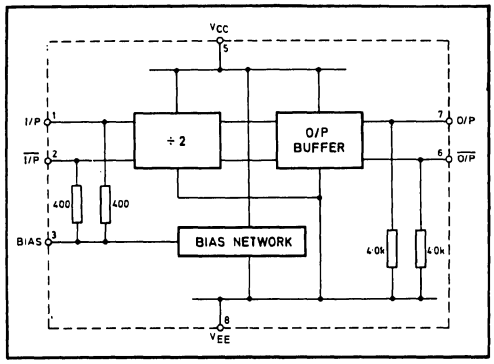



*Fig. 2 SP8607 block diagram*

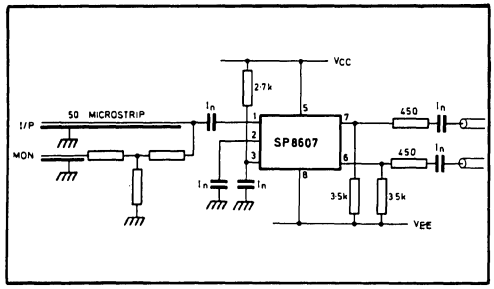



*Fig. 3 Test circuit for SP8607*

## OPERATING NOTES

All components used with the SP8607 should be suitable for the frequencies involved, resistors and capacitors should be of low inductance types and unterminated loads should be kept short to minimise uncounted reflections. The test circuit uses positive earth because this minimises noise problems and the danger of accidently shorting the O/P transistors to a negative voltage. However, the device will operate satisfactorily and to the specification, with a negative earth provided that the positive supply is well decoupled to the UHF earth.

There are two complementary inputs connected to an internally-generated temperature-compensated bias point via two 400 ohm resistors. The signal source would normally be capacitively coupled to one of the inputs and the other should be decoupled to earth. If two complementary input signals are available (when cascading SP8607s for example) both inputs should be used

The input signal can be directly connected to the device either by using a voltage dropping network or by using split power supplies (see Fig. 4). In this mode the device is very tolerant of the actual values of $V_{CC}$ and $V_{EE}$ although $|V_{CC} - V_{EE}|$ should stay within 5.2V ± 0.25V. A 2.7kΩ resistor is connected from $V_{CC}$ to the bias pin in the test circuit because this greatly improves the device's ability to operate with large input signals

It is important that pins 2 and 3 are decoupled by a capacitor in the range 100 – 1000pF because device sensitivity can be reduced by decoupling to a poor earth

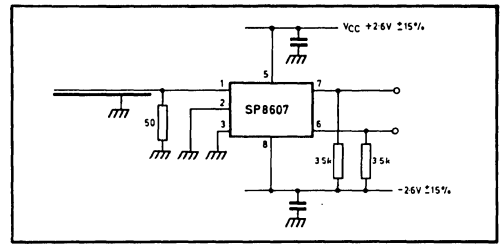



*Fig. 4 Direct coupling using split power supplies*

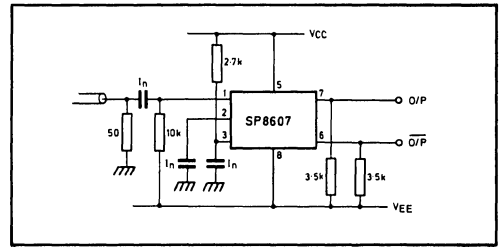



*Fig. 5 SP8607 with input pulldown resistor*

In the absence of an input signal, or if the input signal is of very low amplitude, the device may give an output signal of about 250 MHz. This is due to the balanced nature of the internal ÷2 circuit and can be stopped if required by connecting a 10 kohm resistor between the input and the negative rail. (See Fig. 5). This causes a drop in sensitivity of about 100 mV but typical devices still easily meet the 400 – 800 mV input amplitude specification. With sine wave inputs below 50MHz the SP8607 miscounts because the slew rate of the input signal is too slow. Below this frequency a square wave input is needed with a slew rate of 100V/μ or more.

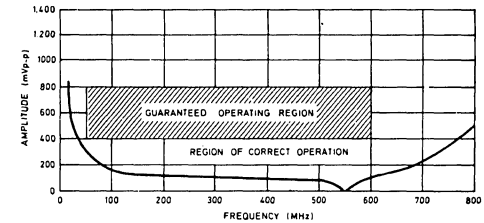



*Fig. 6 Typical operating characteristic*

# SP8610B & M 1.0GHz ÷ 4
# SP8611 B & M 1.5GHz ÷ 4

The SP8610/11 UHF counters are fixed ratio ÷4 asynchronous emitter coupled logic counters with, in the case of the SP8611B, a maximum operating frequency in excess of 1.5GHz over a temperature range of 0°C to +70°C. The input is normally capacitively coupled to the signal source but can be DC coupled if it is required. The two complementary emitter follower outputs are capable of driving 100Ω lines and interfacing to ECL with the same positive supply. The SP8610/11 require supplies of 0V and —5.2V (±0.25V).

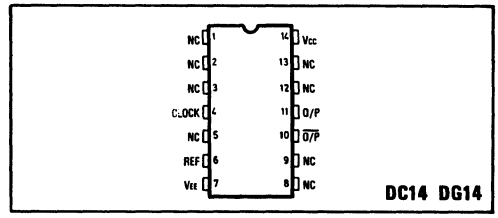



*Fig. 1 Pin connections*

## FEATURES

- DC to 1.5GHz operation
- 0°C to +70°C (B grade) and —40°C to +85°C (M grade) Operation Guaranteed at Maximum Specified Frequency and Over a Wide Dynamic Input Range
- Complementary Emitter Follower O/Ps, ECL III Compatible.

## APPLICATIONS

- UHF Instrumentation, including Counters and Timers
- Prescaling for UHF Synthesisers

## QUICK REFERENCE DATA

- $V_{CC}$ = 0V $V_{EE}$ = —5.2V ± 0.25V
- Input Voltage Range 400mV to 1.0V
- Output Voltage Swing 600mV Typ.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | $V_{CC}$ — $V_{EE}$ 10V |
| Input voltage | $V_{INac}$ 2.5V p–p |
| Output current | 15mA |
| Storage temperature range | —55°C to +150°C |
| Maximum operating junction temperature | +150°C |

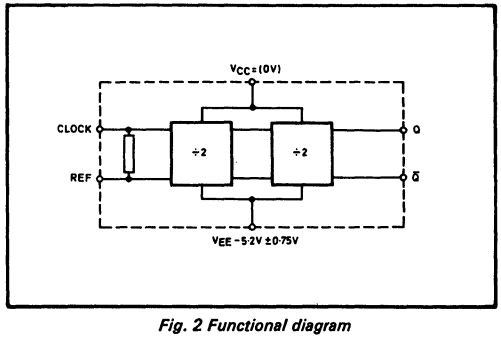



*Fig. 2 Functional diagram*

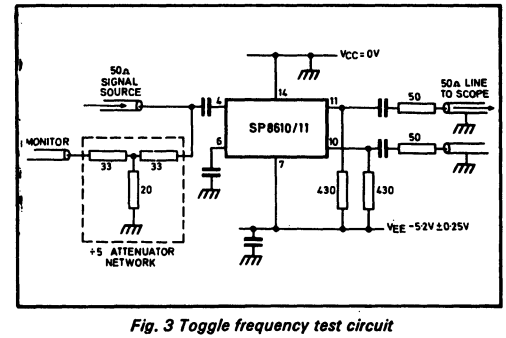



*Fig. 3 Toggle frequency test circuit*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ 0°C to +70°C ('B' Grade)
−40°C to +85°C ('M' Grade)
Supply voltage $V_{CC}$=0V
$V_{EE}$=5.2V±0.25V
Input voltage 400 to 1000mV

| Characteristic | Type | value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max. toggle frequency | SP8611B | 1.3 | | | GHz | $V_{NI}$=400mV to 1V p-p |
| | SP8611B | 1.5 | | | GHz | $V_{IN}$=800mV to 1V p-p |
| | SP8610B | 1.0 | | | GHz | $V_{IN}$=400mV to 1V p-p |
| Min. toggle frequency for correct operation with sine wave input | All | | | 150 | MHz | $V_{IN}$=600mV to IV p-p |
| Min. slew rate for square wave input to guarantee operation to 0Hz | All | | | 200 | V/µs | |
| Output voltage swing | All | 500 | 600 | | mV | |
| Power supply drain current | All | | 70 | 100 | mA | $V_{EE}$= −5.45V No load |

TOGGLE FREQUENCY TEST BOARD LAYOUT
1. All connections to the device are kept short.
2. The capacitors are leadless ceramic types.
3. In practice, the device is tested in an Augat 14 lead DIL socket which degrades the performance slightly. If the device is mounted in a low profile socket or soldered into a printed circuit board, the specified performance will be exceeded.

## OPERATING AND APPLICATION NOTE

The SP8610/11 dividers are very simple to use but normal high frequency rules should be followed for optimum performance. For example, all connections should be kept short and the capacitors and resistors should be types suitable for the frequencies involved.

The input is normally capacitively coupled to the signal source. There is an internal 400Ω resistor connecting the input to a reference voltage; this biases the input in the centre of the transfer characteristic. The reference voltage is brought out onto pin 6, which should be decoupled to the ground plane. This decoupling completes the input signal path to the device and therefore must be very low inductance for optimum performance. The sensitivity of the device can be increased by DC coupling the input signal about ground (see Fig. 4).

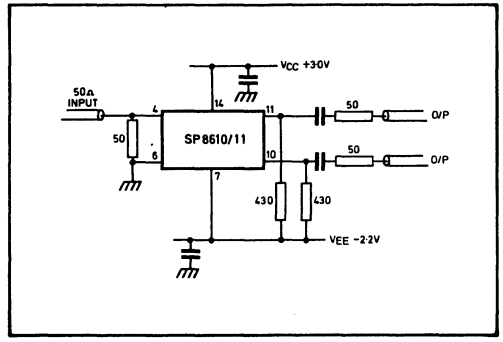



*Fig. 4 Circuit for using the input signal about ground*

|Vcc — VEE| should be kept inside the specified 5.2V ± 0.25V but the actual value of Vcc relative to ground is not very critical and can be varied between 2.7V and 3.3V with only a small effect on performance. A Vcc of about 3.0V is the optimum for full temperature range operation.

In the absence of an input signal both DC coupled and capacitively coupled circuits will self-oscillate with an output frequency of approximately 200MHz. This can be prevented by connecting a 10kΩ resistor between the input and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100mV.

The SP8610/11 will miscount with low frequency sinewave inputs or slow ramps. A slew rate of 200V/μs or greater is necessary for safe operation at low frequencies.

The output can be interfaced to ECL10K or ECL III (see Fig. 5).

The input impedance of the SP8610/11 is a function of frequency and minimises at about the same frequency as the maximum input sensitivity. So, although it can load the signal source significantly, there is usually enough signal to operate the device satisfactorily when the input impedance is at a minimum. The worst case occurs at the maximum frequency because this is when the input sensitivity is worst.

The SP8610/11 can be used in instrumentation for direct counting applications up to 1.5GHz and in frequency synthesisers.

In a frequency synthesiser the SP8610/11 and the SP8643 can be used together (see Fig. 6).

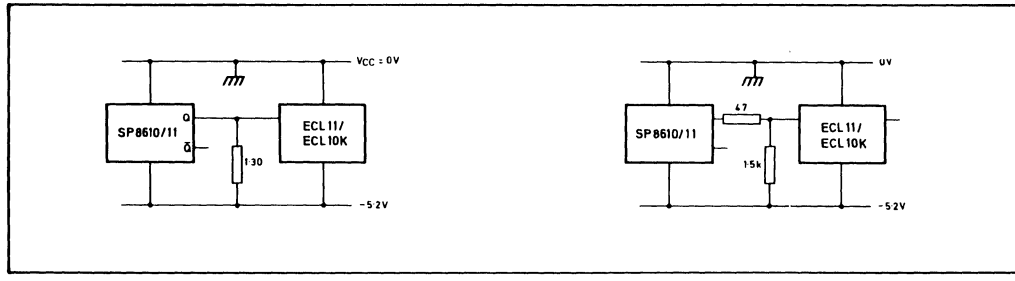



*Fig. 5 Interfacing SP8610/11 to ECL10K and ECL III*

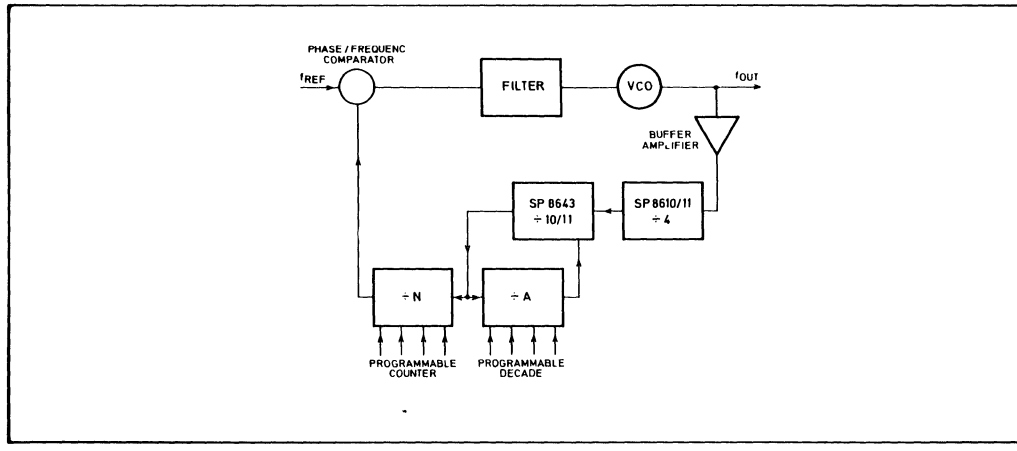



*Fig.6 A 1.5GHz synthesiser loop*

Plessey Semiconductors

# SP8000 SERIES
## HIGH SPEED DIVIDERS

# SP8619B & M 1.5GHz ÷ 4
# SP8617B & M 1.3GHz ÷ 4

The SP8619 series of UHF counters are fixed ratio ÷ 4 asynchronous emitter coupled logic counters with, in the case of the SP8619B a maximum operating frequency in excess of 1.5GHz. The input is normally capacitively coupled to the signal source but can be DC coupled if it is required. The two complementary emitter follower outputs are capable of driving 100 ohm lines and inter facing to ECL with the same positive supply. The SP8619 series require supplies of 0V and −6.8V (± 0.35V).

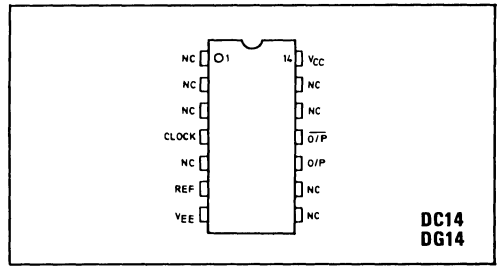



*Fig. 1 Pin connections*

### FEATURES

- DC to 1.5GHz Operation
- 0°C to 70°C (B Grade) and −40°C to +85°C (M Grade) Operation Guaranteed at Maximum Specified Frequency and Over a Wide Dynamic Input Range.
- Complementary Emitter Follower O/Ps, ECL10K and ECL111 Compatible

### APPLICATIONS

- UHF Instrumentation, Including Counters and Timers
- Prescaling for UHF Synthesisers

### QUICK REFERENCE DATA

- $V_{CC}$ = OV $V_{EE}$ = −6.8V ± 0.35V
- Input Voltage Range 400mV to 1.2V p-p
- Temperature Range 0°C to +70°C
- Output Voltage Swing 800mV Typ.

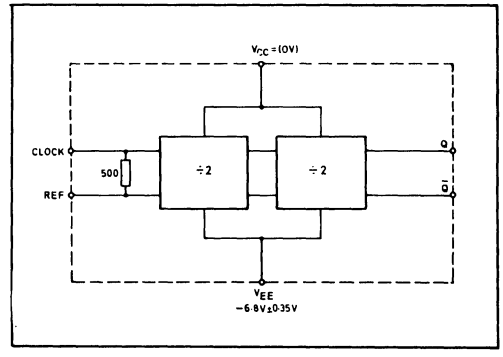



*Fig. 2 Functional diagram*

### ABSOLUTE MAXIMUM RATINGS

Power supply voltage $|V_{CC} - V_{EE}|$ 10V
Input voltage $V_{INac}$ 2.5V p-p
Output current 15mA
Storage temperature range −55°C to +150°C
Maximum operating function temperature +150°C

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**
$T_{amb}$: B Grade 0° C to +70° C
M Grade −40° C to +85° C
Supply voltage Vcc = 0V
$V_{EE}$ = −6.8V ± 0.35V
Input voltage 400 to 1200mV p−p

| Characteristic | Type | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max. toggle frequency | SP8619 | 1.5 | | | GHz | |
| | SP8617 | 1.3 | | | GHz | |
| Min. toggle frequency for correct operation with sine wave input | All | | | 150 | MHz | $V_{IN}$ = 600mV to 1.2Vp-p |
| Min. toggle frequency for correct operation with sine wave input | All | | | 100 | MHz | $V_{IN}$ = 800mV to 1.2Vp-p |
| Min slew rate for square wave input to guarantee operation to 0Hz | All | | | 200 | V/µs | |
| Output voltage swing | All | 600 | 800 | | mV | |
| Power supply drain current | All | | 80 | 110 | mA | $V_{EE}$ = −7.15V |

### Toggle Frequency Test Board Layout

1. All connections to the device are kept short
2. The capacitors are leadless ceramic types
3. In practice, the device is tested in an Augat 14 lead DIL socket which degrades the performance slightly. If the device is mounted in a low profile socket or soldered into a printed circuit board, the specified performance will be exceeded.

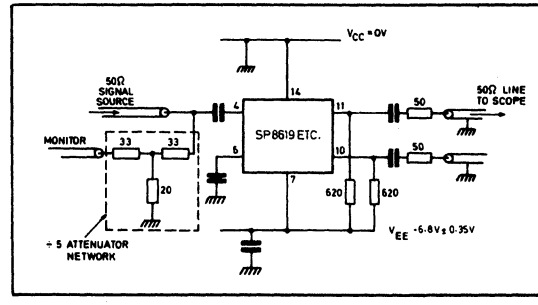



*Fig. 3 Toggle frequency test circuit*

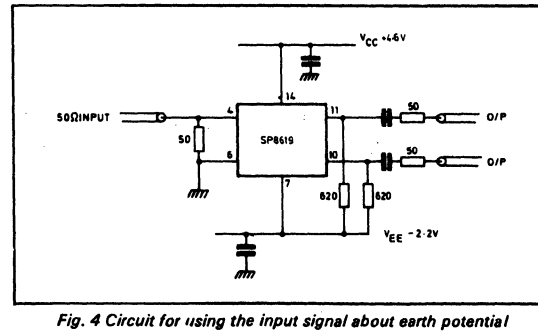



*Fig. 4 Circuit for using the input signal about earth potential*

## OPERATING AND APPLICATION NOTE

The SP8619 series of dividers are very simple to use but normal high frequency rules should be followed for optimum performance - for example, all connections should be kept short and the capacitors and resistors should be types suitable for the frequencies involved.

The input is normally capacitively coupled to the signal source. There is an internal 400 ohm resistor connecting the input to a reference voltage; this biases the input in the middle of the transfer characteristic. The reference voltage is brought out onto pin 6, which should be decoupled to the earth plane.

The sensitivity of the device can be increased by DC coupling the input signal about earth (see Fig. 4 ).

$|V_{CC} - V_{EE}|$ should be kept inside the specified 6.8V $\pm$0.35V but the actual value of $V_{CC}$ relative to earth is not very critical and can be varied between 4.2V and 5.0V with only a small effect on performance. A $V_{CC}$ of about 4.6V is the optimum for full temperature range operation.

In the absence of an input signal both the DC coupled and the capacitively coupled circuits will self-oscillate with an output frequency of approximately 300MHz. This can be prevented by connecting a 10k ohm resistor between the input and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100mV.

The SP8619 will miscount with low frequency sine-wave inputs or slow ramps. A slew rate of 200V/$\mu$s or greater is necessary for safe operation at low frequencies.

The output can be interfaced to ECL 10K or ECL III (see Fig. 5).

The input impedance of the SP8619 is a function of frequency and minimises at about the same frequency as the maximum input sensitivity, so, although it can load the signal source significantly there is usually enough signal to operate the device satisfactorily when the input impedance is at a minimum input signal requirement. The worst case occurs at the maximum frequency because this is where the input sensitivity is worst.

The SP8619 series can be used in instrumentation for direct counting applications up to 1.5GHz and in frequency synthesisers.

In a frequency synthesiser, the SP8619 and the SP8643 can be used together (see Fig. 6).

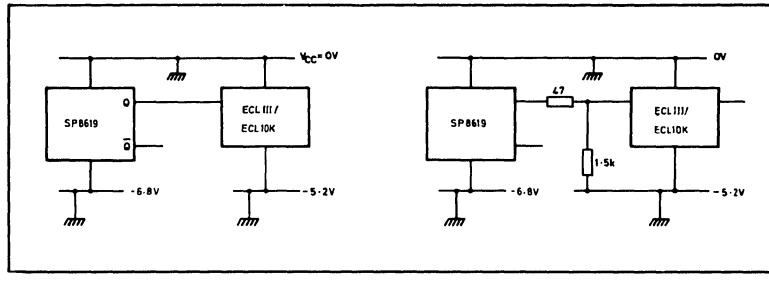



*Fig. 5 Interfacing SP8619 series to ECL 10K and ECL III*

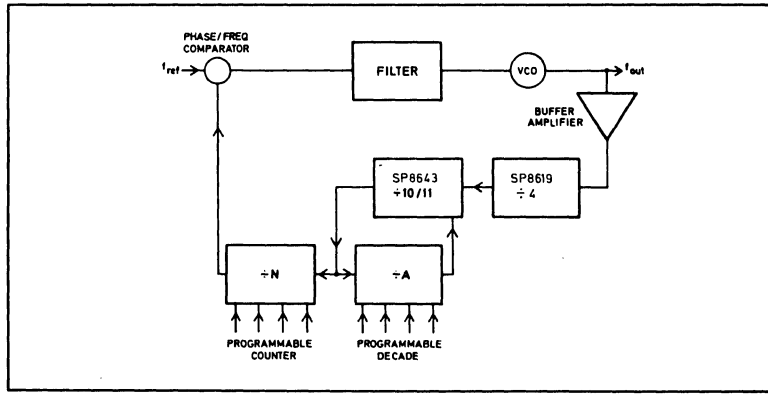



*Fig. 6 A 1.5GHz synthesiser loop*

Plessey Semiconductors

# SP8000 SERIES

## HIGH SPEED DIVIDERS

### ÷5 COUNTERS

# SP8620 A&B

## (400MHz)

The SP8620 is a fixed ratio emitter-coupled logic ÷5 counter with specified input frequency range of DC to 400MHz. The operating temperature is specified by the final coding letter: −55°C to +125°C ('A' grade), 0°C to +70°C ('B' grade).

The counter is normally capacitively coupled to the signal source and is specified with an input signal range of 400–800mv p-p (−4dBm to +22dBm). There are two bias points on the circuit that should be capacitively decoupled to the ground plane.

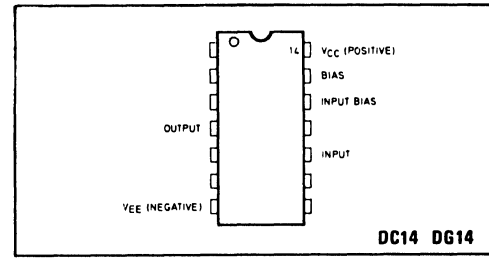



*Fig.1 Pin connections (bottom view)*

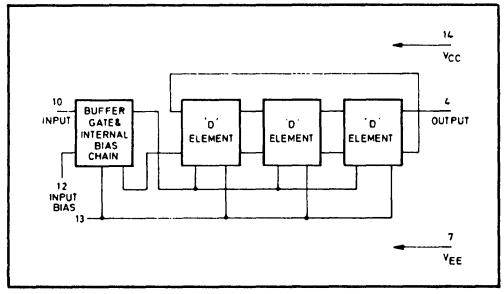



*Fig.2 Circuit diagram (all resistor values are nominal)*

## FEATURES

- D.C. to 400MHz Operation.
- Temperature Ranges of −55°C to +125°C ('A' Grade), 0°C to +70°C ('B' Grade) Over Full Specified Input Range and Frequency

## APPLICATIONS

- Frequency Counters and Timers
- Frequency Synthesisers

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$ | 8V |
| Input voltage $V_{IN}$ | Not greater than supply |
| Output current $I_{OUT}$ | 15mA |
| Operating junction temperature | +150°C |
| Storage temperature | −55° to +150°C |

## ELECTRICAL CHARACTERISTICS

**Test Conditions** (unless otherwise stated)

Tamb: 'A' grade: −55°C to +125°C
'B' grade: 0°C to +70°C

| Characteristic | Type | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max. input frequency | SP8620 | 400 | | | MHz | |
| Min. input frequency with sinusoidal input | | | 20 | 40 | MHz | |
| Min. slew rate of square wave input for correct operation | | | 30 | 100 | V/μS | |
| Output voltage swing | | 400 | 800 | | mV | $V_{EE}$ = −5.2V |
| Power supply drain current | | | 55 | 70 | mA | $V_{EE}$ = −5.2V |

## OPERATING NOTES

It is recommended that a positive earth plane is used for the circuit layout, thus preventing damage if the output is short-circuited to earth.

The signal source is normally capacitively coupled to the input (see Fig. 3). A 1000pF capacitor is suitable at high frequencies, but if lower frequency operation is also required, say below 10MHz, then an additional capacitor should be connected in parallel: The device can be DC coupled if it is required – see Fig. 4.

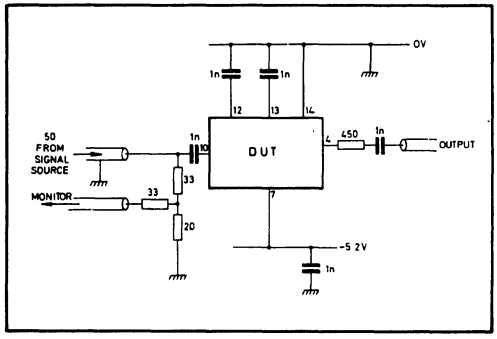



*Fig.3 Test circuit*

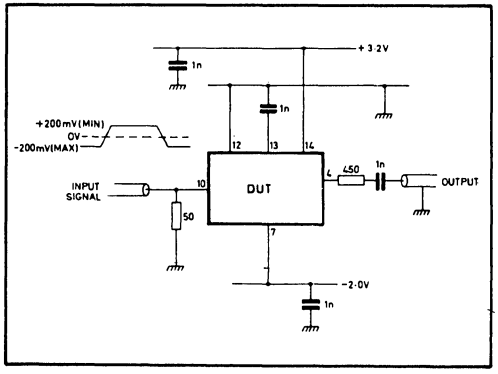



*Fig.4 Divide by 16 frequency scaler*

The circuit may self oscillate when there is no input signal or when the input signal is well below the specified input signal. This can be prevented by connecting a 15kΩ resistor between the input and the negative rail. This causes a loss in sensitivity of up to 100mV p-p.

The input waveform may be sinusoidal, but below about 20MHz the circuit tends to malfunction on minimum amplitude input signals and the condition becomes worse as the frequency is decreased. This is because correct operation of the circuit depends on the slew rate of the input signal. A square wave input with a slew rate greater than 100V/μS ensures correct operation down to DC.

The output swing of the devices can be significantly increased by the addition of a DC load on the emitter follower output. For instance, the maximum DC load of 1.5kΩ will give an increase of typically 50% in output swing with no effect on input drive level or maximum operating frequency. This allows the SP8620 devices to interface directly to ECL II devices with no loss in noise immunity. If the devices are required to interface to ECL III or ECL 10,000 then an interface similar to Fig. 5 should be used.

The values of the decoupling capacitors are not critical, but they should be of a type suitable for the frequencies involved.

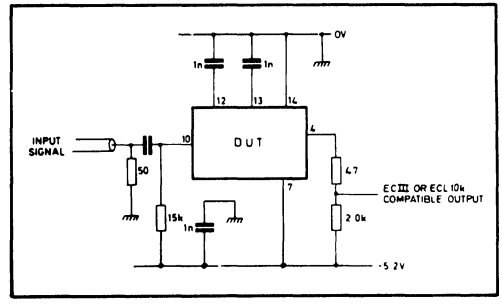



*Fig. 5 Interfacing to ECL III or ECL 10,000*

# SP8627 ÷ 80
# SP8628 ÷ 100 (WITH RESET)
# SP8629 ÷ 100

## 150 MHz PRESCALERS

The SP8629 is a fixed ratio ECL ÷ 100 counter with a minimum guaranteed toggle frequency of 150MHz over a −30°C to +70°C temperature range. The device can operate in the single-ended or differential input mode, and is typically capacitively coupled to the signal source. An input amplifier is included to allow use of extremely small amplitude high frequency signals. The output of the device is similar to Low Power Schottky TTL and produces a square wave of frequency $f_{out} = f_{in}/100$.

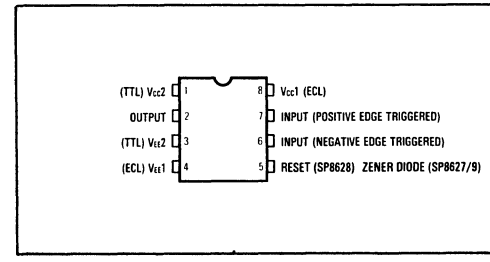



*Fig. 1 Pin connections*

### FEATURES

- Low Power 170mW typica
- High Frequency, DC to 150MHz, Small Input Amplitude
- Single Supply Operation 5.2v ± 10%
- Count Down Sequence avoids FM IF Harmonics
- ECL Dividers reduce Switching Transients
- ÷4 Reset on SP8628 Reduces Jitter on Frequency Display Systems

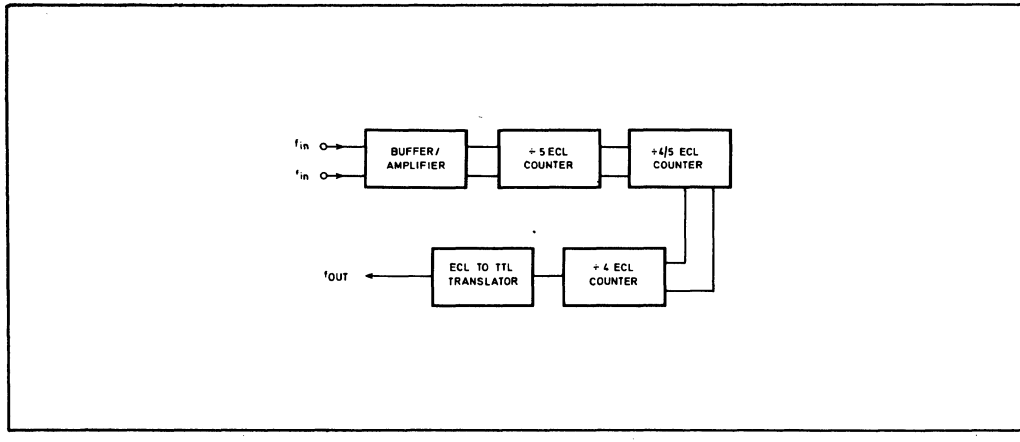



*Fig. 2 SP8627/8/9 logic diagram*

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of Electrical Characteristics provides conditions for actual device operation.

| | | |
|---|---|---|
| Power Supply Voltage | $\|V_{CC} - V_{EE}\|$ | 8V |
| Input Voltage | Vin (DC) | not greater than supply voltage |
| Output voltage | $V_{OUT}$ | 5.5V |
| Output current | $I_{OUT}$ | 40mA |
| Zener current | $I_Z$ | 20mA |
| Operating Junction temperature | | 150°C |
| Storage temperature range | | −30°C to +85°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Supply voltage $V_{CC}$: + 5.2V ± 0.52V, $V_{EE}$: 0V,
$T_{amb}$: 25°C

| Characteristic | Symbol | Value Min. | Value Typ. | Value Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Maximum input frequency | $f_{max}$ | 150 | 200 | | MHz | $V_{CC}$ = 5.2V, $V_{IN}$ = 600mVp−p, single ended |
| Input voltage | $V_{IN}1$ | 200 | | 1000 | mVp−p | $V_{CC}$ = 5.2V, single ended |
| Input voltage | $V_{IN}2$ | 100 | | 1000 | mVp−p | $V_{CC}$ = 5.2V, differential |
| Minimum input frequency with sine wave | $f_{sine}$ | 10 | | | MHz | $V_{CC}$ = 5.2V, $V_{IN}$ = 600mVp−p |
| Minimum slew rate of square wave input | dv/dt | | | 50 | V/μs | $V_{CC}$ = 5.2V, $V_{IN}$ = 600mVp−p |
| Logic 1 output voltage | $V_{OH}$ | 2.4 | | | V | $V_{CC}$ = Min, $I_{OH}$ = −400/μA |
| | | 2.0 | | | V | $V_{CC}$ = Min, $I_{OH}$ = −1.6mA |
| Output short circuit current | $I_{OS}$ | −10 | | −40 | mA | $V_{CC}$ = Max |
| Logical 0 output voltage | $V_{OL}$ | | | 0.5 | V | $V_{CC}$ = Min, $I_{OL}$ = 8mA |
| Supply current | $I_{CC}$ | | 33 | 45 | mA | $V_{CC}$ = Max |
| Zener voltage, pin 5 (SP8627/9) | $V_Z$ | | 6.3 | | V | $I_Z$ = 5mA (see note 2) |
| Reset input voltage (SP8628) | $V_{IN(LO)}$ | | | 0.5 | V | |
| | $V_{IN(HI)}$ | 2.4 | | | V | |
| Reset input current (SP8628) | $I_{IN}$ | | | −1.6 | mA | $V_{IN}$ = 0.5V |

NOTE
All currents into device pins shown as positive, out of device pins negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

## TYPICAL APPLICATIONS

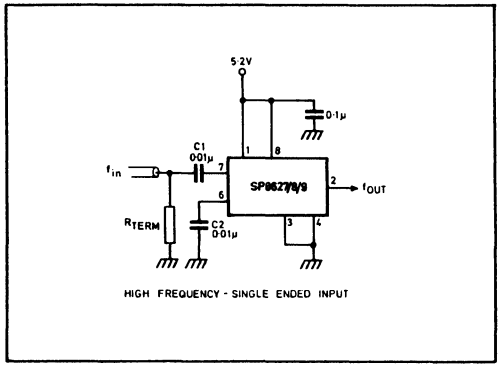



*Fig. 3 High frequency, single-ended input*

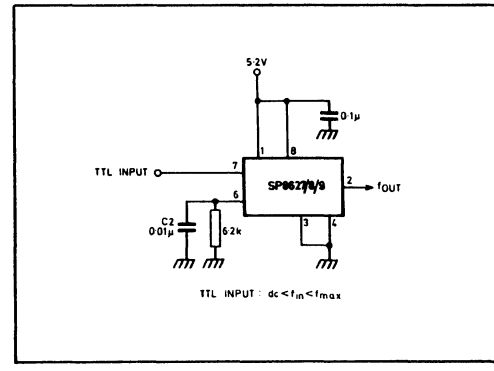



*Fig. 4 TTL input (DC<$f_{in}$<$f_{max}$)*

## OPERATING NOTES.

Two ground and two $V_{CC}$ connections are provided, separating the ECL stages from the TTL section, isolating the noise transients inherent in the TTL structure. In most cases, shorting the two grounds to a good ground plane and the $V_{CC}$s to a wide $V_{CC}$ bus will provide sufficient isolation. All components used in the circuit layout should be suitable for the frequencies involved and leads should be kept short to minimise stray inductance.

The signal source is usually capacitively coupled to the input as shown in Fig. 3. In the single-ended mode a capacitor of 0.01 μF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be increased at lower frequencies. If the input is likely to be interrupted, it may be desirable to connect a 100k Ω resistor between an input and ground. In the single ended mode it is preferable to connect the resistor to the unused input. The addition of the 100k Ω resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions.

The input waveform will normally be sinusoidal but below 10MHz correct operation depends on the slew rate of the input signal. A slew rate of 50V/μs will enable the device to operate down to DC. The device will operate with a TTL input signal as shown in Fig. 4 and is DC coupled to the input.

The device can be used in phase locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more useable level. A digital frequency display system can also be derived separately or in conjunction with a phase locked loop, and it can extend the useful range of many inexpensive frequency counters to, typically, 200MHz

The on-chip Zener diode allows a simple stabilised power supply to be constructed with the addition of a few extra external components, as shown in Fig. 5, to the SP8627/9. The SP8628 has a 'reset' facility on pin 5. This input acts as a data inhibit to the final divide-by-four when a high level is applied (or the input is left open circuit).

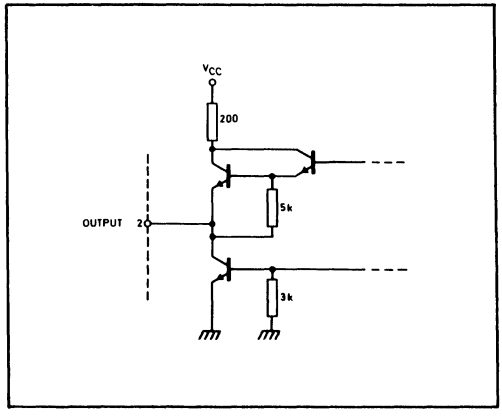



*Fig. 7 Output circuit diagram*

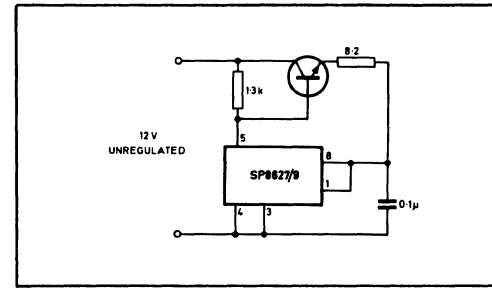



*Fig. 5 Voltage regulator*

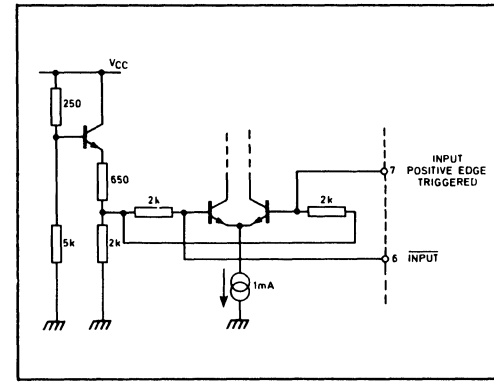



*Fig. 6 Input circuit diagram*

# SP8630 A&B

## 600MHz DECADE COUNTER

### GENERAL DESCRIPTION

The SP8630 counter is a fixed ratio ÷ 10 circuit using emitter coupled logic, with maximum specified counting frequencies of 600 MHz over temperature ranges of −55°C to +125°C, 0°C to 70°C. A 6:4 mark/space square wave is provided at the emitter follower output. The input is normally single driven and capacitively coupled to the signal source. There are two bias points on the circuit which should be capacitively coupled to the ground plane.

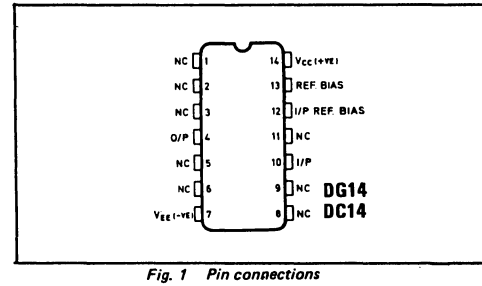
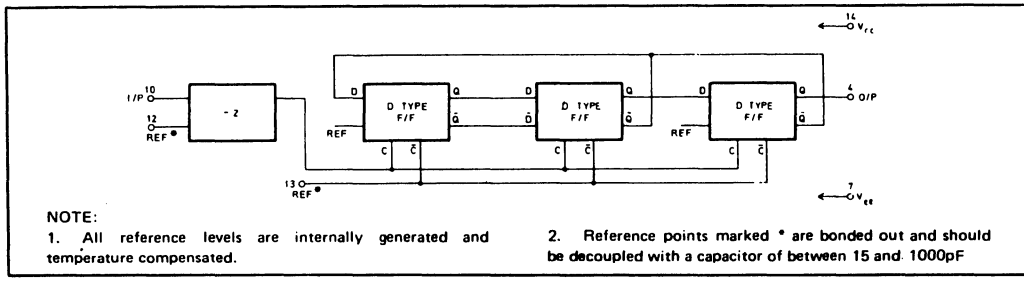



*Fig. 1 Pin connections*




NOTE:
1. All reference levels are internally generated and temperature compensated.
2. Reference points marked * are bonded out and should be decoupled with a capacitor of between 15 and 1000pF

*Fig. 2 Block diagram*

### ELECTRICAL CHARACTERISTICS

**Test conditions (unless stated otherwise):**

Tamb: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C

Operating supply voltage
$V_{CC}$ 0V
$V_{EE}$ −5.2V ± 0.25V
Input voltage 400 to 800 mV (p-p)
Output load 500Ω & 3pF.

NOTE: The maximum input frequency is guaranteed at $V_{EE}$ = −5.2V. For typical operating characteristics with power supply variations see Fig.5, which shows that the maximum operating frequency of a typical device increases with increasing power supply voltage

| Characteristic | Type | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Max input freq. | SP8630 | 600 | | | MHz | |
| Min input freq. with sinusoidal input | | | 20 | 40 | MHz | |
| Min. slew rate of square wave I/P for correct operation | | | 30 | 100 | V/μs | |
| Output voltage swing | | 400 | 600 | | mV | $V_{EE}$ = −5.2V |
| Power supply drain current | | | 70 | 95 | mA | $V_{EE}$ = −5.2V |

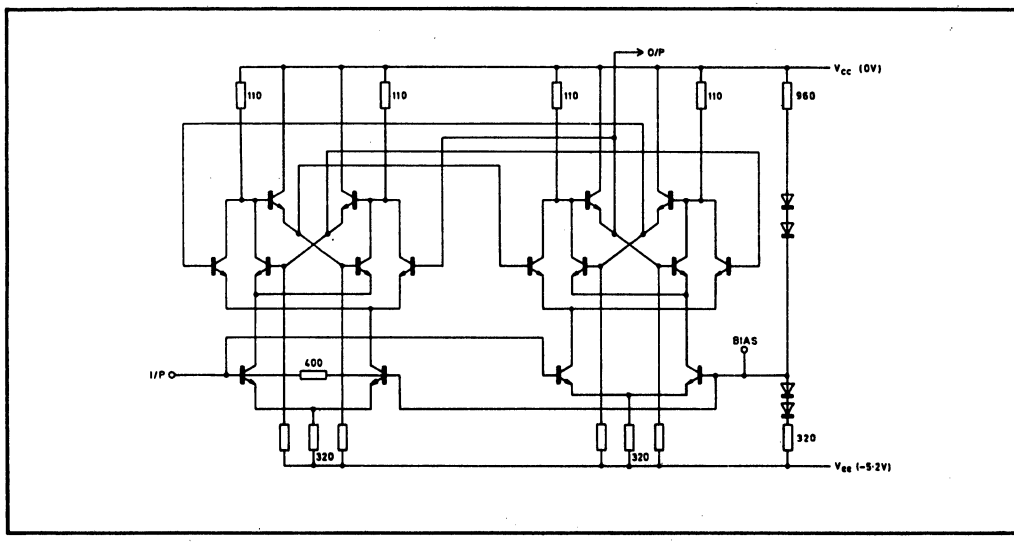



*Fig. 3 Circuit diagram of 1st element (–2) showing input biasing arrangement*

## OPERATING NOTES

It is recommended that a positive earth plane be used for the circuit layout, thus preventing damage if the emitter follower outputs are inadvertantly shorted to ground.

The signal source is normally capacitively coupled to the input: 1000 pF is usually sufficient. If the input signal is likely to be interrupted a 15 k ohm resistor should be connected between the input pin and the negative rail to prevent circuit oscillation under no-signal conditions. The addition of the pulldown resistor causes a slight loss of sensitivity of the device, but this does not normally cause problems in practice.

The input waveform may be sinusoidal, but below 40 MHz the operation of the circuit becomes dependent on the slew rate of the waveform rather than the amplitude. A square wave input with a slew rate of 100 V/μs will allow correct operation down to DC. At high frequencies, increasing drive level above minimum typically increases the max. operating frequency by up to 25%.

The output swing of the device can be significantly increased by the addition of a DC load on the emitter follower output. For instance, the maximum DC load of 1.5k ohms will give an increase of typically 50% in output swing with no effect on input drive level or maximum operating frequency. This allows the SP8630 device to drive directly into ECL II devices with no loss in noise immunity.

The value of capacitance needed for the decoupling capacitors is not critical. Values down to 15 pF have been found satisfactory in practice.

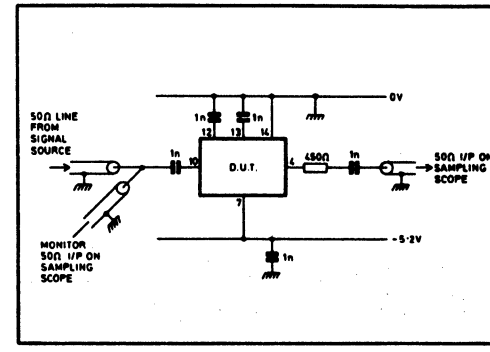



*Fig. 4 Test circuit*

### Test Circuit Notes

The values of the coupling and decoupling capacitors are uncritical but they should be of a type and value suitable for the frequencies involved.

All connections should be physically short when not in a 50Ω environment to minimise reflections due to mismatching.

The +ve pin should be connected to a low impedance earth plane to minimise feed-through of the input signal to the output.

## Typical Operating Characteristics

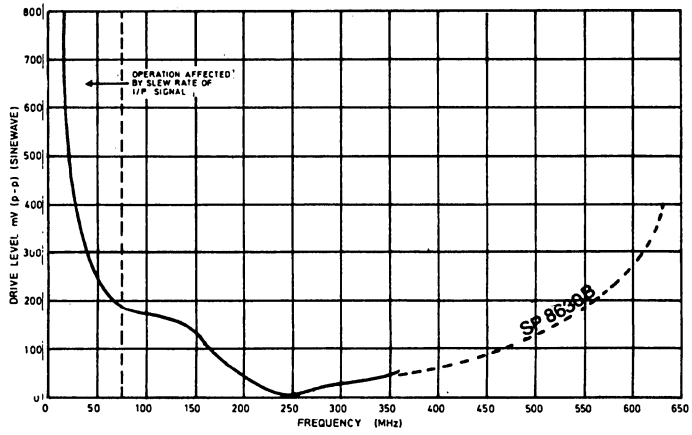



*Fig. 5 Minimum drive level v. input frequency at +25 C*

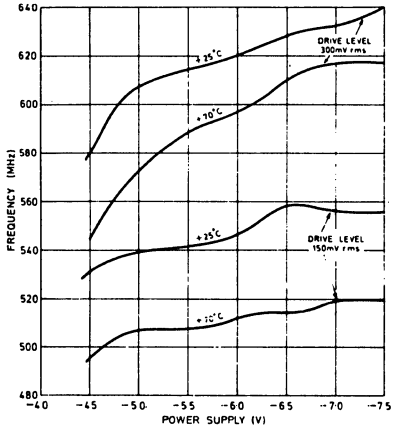



*Fig. 6 Max. operating frequency v. power supply voltage for a typical SP8630B*

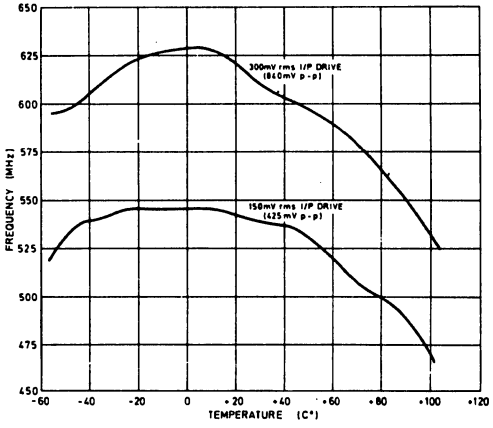



*Fig. 7 Max. operating frequency v. ambient temperature for a typical SP8630B (Vcc = —5.2V)*

## APPLICATION NOTES

### Direct coupling to the SP8630

It can be seen from the circuit diagram that the input arrangement of the SP8630 series is not compatible with the normal ECL logic levels. The input reference level is approximately −3.2 volts but it is not well defined and has a temperature coefficient of approximately −1.6 mV/°C. If DC coupling is required, the input would have to be larger than would be the case with capacitive coupling.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $V_{CC} - V_{EE}$ | 8V. |
| Input voltage $V_{IN}$ | Not greater than the supply voltage in use |
| Output current $I_{OUT}$ | 15 mA |
| Operating junction temperature | +150°C |
| Storage temperature | −55°C to +150°C |

Plessey Semiconductors

# SP8000 SERIES
## HIGH SPEED DIVIDERS

# SP8634B
## ÷ 10 700 MHz

**The SP8634B, is a divide-by-ten circuit with binary coded decimal outputs for operation from DC up to specified input frequencies of 700 MHz, over a guaranteed temperature range of 0°C to +70°C.**

These devices, optimised for counter applications in systems using both ECL and TTL, are intended to be operated between 0V and −5.2V power rails and to interface with TTL operating between 0V and +5V. The BCD outputs and one of two carry outputs are TTL-compatible, while the second carry output is ECL-compatible. The clock input, which is normally capacitively coupled to the signal source, is gated by an ECL III/ECL 10k-compatible input. The TTL-compatible reset forces the 0000 state regardless of the state of the other inputs.

### FEATURES
- Direct gating capability at up to 700 MHz
- TTL-compatible BCD outputs
- TTL- and ECL-compatible carry outputs
- Power consumption less than 500 mW
- Wide dynamic input range

### APPLICATIONS
- Counters
- Timers
- Synthesisers

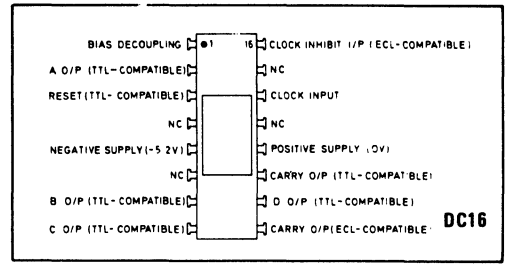



*Fig. 1 Pin connections (top)*

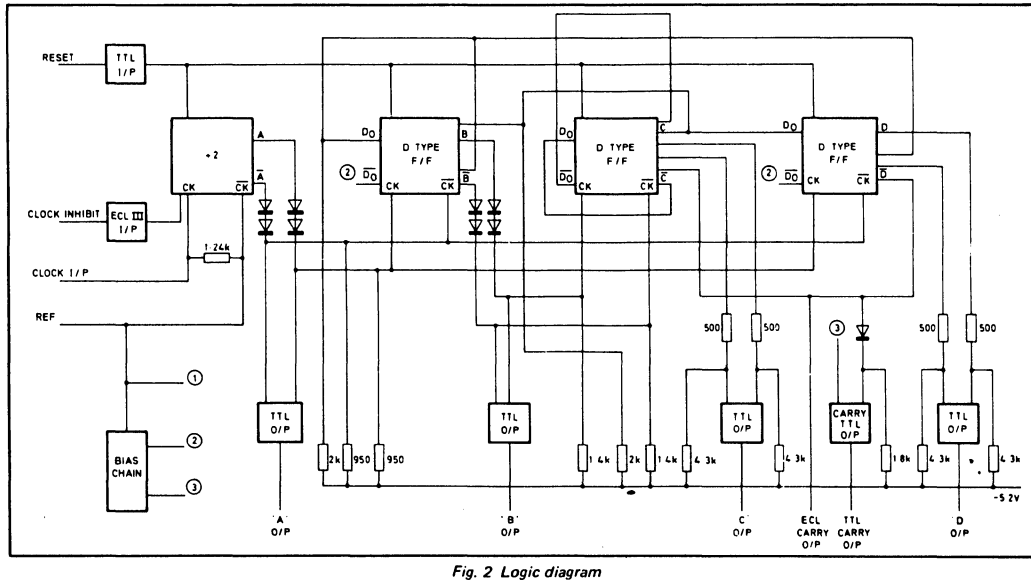



*Fig. 2 Logic diagram*

## ELECTRICAL CHARACTERISTICS (All types except where otherwise stated)

**Test Conditions (unless otherwise stated)**

| | | |
|---|---|---|
| $T_{amb}$ | | 0°C to +70°C |
| Power Supplies | $V_{CC}$ | 0V |
| | $V_{EE}$ | −5.2V ± 0.25V |

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Clock Input (pin 14)** | | | | | |
| Max. input frequency SP8634B | 700 | | | MHz | Input voltage 400-800mV p-p |
| Min. input frequency with sinusoidal I/P | | | 40 | MHz | |
| Min. slew rate of square wave for correct operation down to DC | | | 100 | V/μs | |
| **Clock inhibit input (pin 16)** | | | | | |
| Logic levels | | | | | |
| High (inhibit) | −0.960 | | | V | $T_{amb}$ = +25°C |
| Low | | | −1.650 | V | (see Note 1) |
| Edge speed for correct operation at maximum clock I/P frequency | | | 2.5 | ns | 10%–90% |
| **Reset input (pin 3)** | | | | | |
| Logic levels | | | | | |
| High (reset) | See Note 2 | | | | |
| Low | | | +0.4 | V | |
| Reset ON time | 100 | | | ns | |
| **TTL outputs ABCD (pins 2,7,8,10)** | | | | | See Note 3 and Fig. 4 |
| Output Voltage | | | | | |
| High | +2.4 | | | V | 10k Ω resistor and TTL gate from O/P |
| Low | | | +0.4 | V | to +5V rail |
| **TTL carry output (pin 11)** | | | | | |
| Output Voltage | | | | | |
| High state | +2.4 | | | V | 5kΩ resistor and 3 TTL gates from o/p |
| Low | | | +0.4 | V | to 5V rail |
| **ECL carry output (pin 9)** | | | | | |
| Output Voltage | | | | | |
| High | −0.975 | | | V | $T_{amb}$ = +25°C External current |
| Low | | | −1.375 | V | = 0mA (See Note 4) |
| **Power supply drain current** | | 75 | 90 | mA | $V_{EE}$ = 5.2V |

NOTES

1. The clock inhibit input levels are compatible with ECL III and ECL 10000 levels throughout the temperature range 0°C to +70°C.
2. For a high state, the reset input requires a more positive input level than the specified worst case TTL $V_{OH}$ of +2.4V. Resetting should be done by connecting a 1.8kΩ resistor from the output of the driving TTL gate and only fanning out to the reset input of the SP8000 series device.
3. These outputs are current sources which can be readily made TTL-compatible voltages by connecting them to +5V via 10kΩ resistors.
4. The ECL carry output is compatible with ECL II throughout the temperature range but can be made compatible with ECL III using the simple interface shown in Fig. 3.

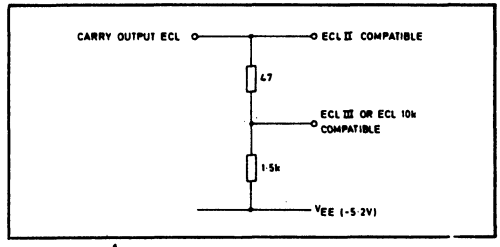



*Fig. 3 ECL III/ECL 10000 interfacing*

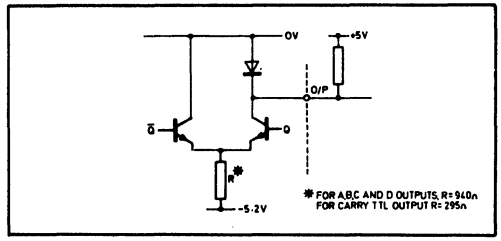



*Fig. 4 TTL carry and ABCD output structure*

## OPERATING NOTES

**The devices are intended to be used with TTL and ECL in a counting system – the ECL and the decade counter being connected between voltage rails of OV and –5.2V and the TTL between voltage rails of OV and +5.0V. Provided that this is done ECL and TTL compatability is achieved (see Figs. 4 and 5).**

The clock is normally capacitively coupled to the signal source: a 1000pF UHF capacitor is normally adequate. If low frequency operation is required the 1000pF capacitor should be connected in parallel with a higher value capacitor. The bias decoupling (pin 1) should be connected to earth via a capacitor – preferably a chip type – but in any case a low inductance type suitable for UHF applications. The devices normally have an input amplitude operating range far greater than the specified 400 to 800 mV pk/pk. However, if the decoupling capacitor is not of a UHF type, or it is connected to an earth point that has a significant impedance between the capacitor and the $V_{CC}$ connection, then the input dynamic range will suffer and the maximum signal for correct operation will be reduced.

Under certain conditions, the absence of an input signal may cause the device to self-oscillate. This can be prevented (while still maintaining the specified input sensitivity) by connecting a 68kΩ resistor between the clock input and the negative supply. If the transition of either the clock input or the clock inhibit input is slow the device may start to self-oscillate during the transition. For this reason, the input slew rates should be greater than 100 V/μs. It should also be noted that a positive-going transition on either the clock input or the clock inhibit input will clock the device, provided that the other input is in the low state.

The BCD outputs give TTL-compatible outputs (fanout = 1) when a 10kΩ resistor is connected from the output to the +5V rail. In this configuration the outputs will be very slow compared with the clocking rate of the decade and so the state on the BCD outputs can only be determined when the clock has stopped or is inhibited.

The fan out capability of the TTL carry output can be increased by buffering it with a PNP emitter follower. The interface is shown in Fig. 5.

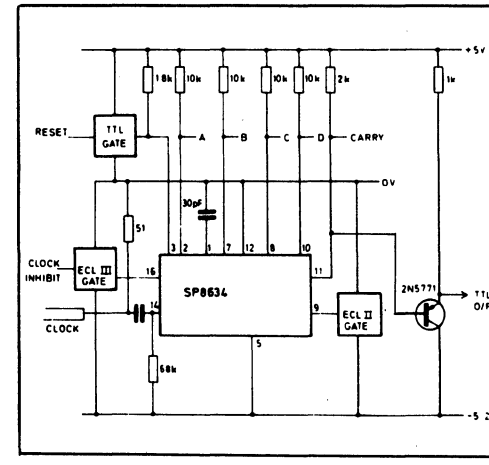



*Fig. 5 Typical application configuration*

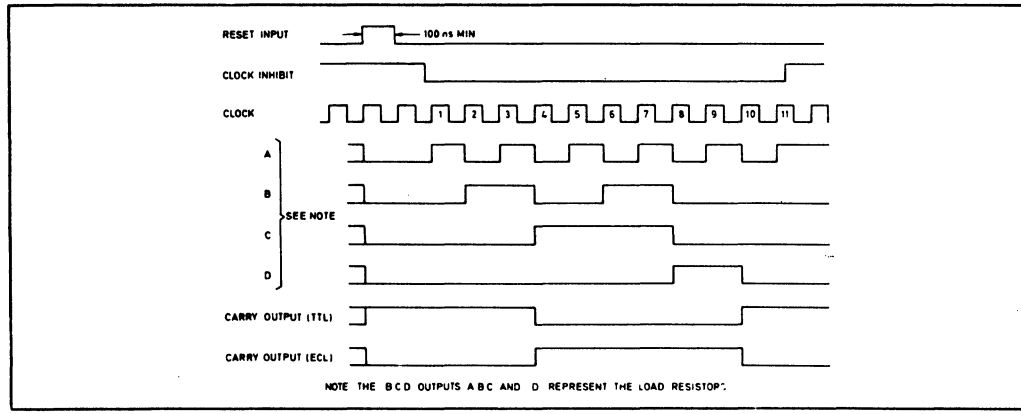



*Fig. 6 Decade counter timing diagram*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage ($V_{CC} - V_{EE}$) | 8V |
| Clock inhibit voltage | Not greater than the supply voltage in use |
| Clock input voltage | 2V pk/pk |
| Bias voltage ($V_{OUT}$) on BCD outputs, $V_{OUT} - V_{EE}$ (10kΩ resistor in series with output) | 11V |
| Bias voltage ($V_{OUT}$) on TTL carry output, $V_{OUT} - V_{EE}$ (1.2kΩ resistor in series with output) | 11V |
| Output current from ECL carry output ($I_{OUT}$) (Note: the device will be destroyed if the ECL output is shorted to the negative rail) | 10mA |
| Operating junction temperature | +150°C |
| Storage temperature range | −55°C to +150°C |

## QUICK REFERENCE DATA

| | | |
|---|---|---|
| ■ Power Supplies | $V_{CC}$ | 0V |
| | $V_{EE}$ | 5.2V ± 0.25V |
| ■ Range of clock input amplitude | | 400-800mV p-p |
| ■ Operational temperature range | | 0°C to +70°C |
| ■ Frequency range with sinusoidal I/P | | 40-700 MHz |
| ■ Frequency range with square wave I/P | | DC to 700 MHz |

# SP 8643A & B 350 MHz

# SP 8647 A & B 250 MHz TTL OUTPUTS

## UHF PROGRAMMABLE DIVIDERS ÷10/11

In frequency synthesis it is desirable to start programmable division at as high a frequency as possible, because this raises the comparison frequency and so improves the overall synthesiser performance.

The SP8640 series are UHF integrated circuits that can be logically programmed to divide by either 10 or 11, with input frequencies up to 350 MHz. The design of very fast fully programmable dividers is therefore greatly simplified by the use of these devices and makes them particularly useful in frequency synthesisers operating in the UHF band.

Inputs and outputs are ECL compatible throughout the temperature range: the clock inputs and programming inputs are ECL III compatible while the two complementary outputs are ECL II compatible to reduce power consumption in the output stage. ECL 10K output compatability can be achieved very simply however (see Operating Notes). The SP8643/7 feature an additional TTL compatible output.

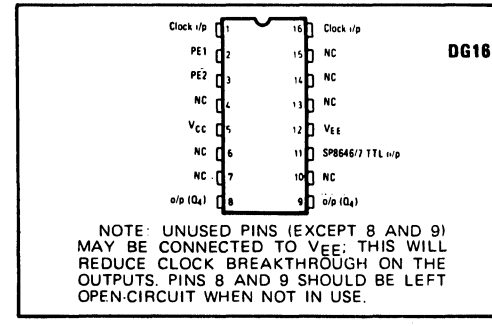
The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 10 when either $\overline{PE}$ input is in the high state and by 11 when both inputs are in the low state. Both the $\overline{PE}$ inputs and the clock inputs have nominal 4.3k Ω pulldown resistors to $V_{EE}$ (negative rail).

### FEATURES

- Military and Industrial Variants.
- 350 MHz Toggle Frequency
- Low Power Consumption
- ECL Compatibility on All I/Ps & O/Ps
- Low Propagation Delay
- True and Inverse Outputs
- Optional TTL Output

### QUICK REFERENCE DATA

- Full Temperature Range Operation:
  'A' Grade —55°C to +125°C
  'B' Grade 0°C to +70°C
- Supply Voltage
  $|V_{CC} - V_{EE}|$ 5.2V
- Power Consumption 250mW Typ.
- Propagation Delay 3ns Typ.




NOTE: UNUSED PINS (EXCEPT 8 AND 9) MAY BE CONNECTED TO $V_{EE}$; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS. PINS 8 AND 9 SHOULD BE LEFT OPEN-CIRCUIT WHEN NOT IN USE.

*Fig. 1 Pin connections (top)*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $\|V_{CC} - V_{EE}\|$ | 8V |
| Input voltage $V_{in}$ (d.c.) | Not greater than the supply voltage in use. |
| Output current $I_{out}$ | 20mA |
| Max. junction temperature | +150°C |
| Storage temperature range | −55°C to +175°C |

| Clock Pulse | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | TTL O/P |
|---|---|---|---|---|---|
| 1 | L | H | H | H | H |
| 2 | L | L | H | H | H |
| 3 | L | L | L | H | H |
| 4 | H | L | L | H | H |
| 5 | H | H | L | H | H |
| 6 | L | H | H | L | L |
| 7 | L | L | H | L | L |
| 8 | L | L | L | L | L |
| 9 | H | L | L | L | L |
| 10 | H | H | L | L | L |
| 11 | H | H | H | H | H |

Extra state

*Table 1 Count sequence*

| $\overline{PE_1}$ | $\overline{PE_2}$ | Div Ratio |
|---|---|---|
| L | L | 11 |
| H | L | 10 |
| L | H | 10 |
| H | H | 10 |

*Table 2 Truth table for control inputs*

The maximum possible loop delay for control is obtained if the L→H transition from $Q_4$ or the H→L transition from $\overline{Q_4}$ is used to clock the stage controlling the ÷10/11. The loop delay is 10 clock periods minus the internal delays of the ÷10/11 circuit.

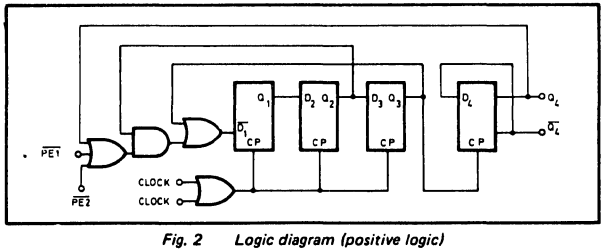



*Fig. 2 Logic diagram (positive logic)*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$: −55 C to −125 C (A grade)
0 C to −70 C (B grade)

Supply voltage (see note 1): $V_{CC}$ 0V
$V_{EE}$ −5.2V

**Static Characteristics (all SP8640 series devices)**

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Clock and $\overline{PE}$ input voltage levels | | | | | |
| $V_{INH}$ | −1.10 | | −0.81 | V | $T_{amb}$ = +25°C, |
| $V_{INL}$ | −1.85 | | −1.50 | V | see Note 2 |
| Input pulldown resistance, between pins 1, 2, 3, and 16 and $V_{EE}$ (pin 12) | | 4.3 | | KΩ | |
| Output voltage levels | | | | | |
| $V_{OH}$ | −0.85 | | | V | $T_{amb}$ = +25°C, |
| $V_{OL}$ | | | −1.50 | V | see Note 3. $I_{out}$ (external) = 0mA (There is an internal circuit equivalent to a 2kΩ pulldown resistor on each output) |
| Power supply drain current | | 50 | 65 | mA | |

NOTES

1. The devices are specified for operation with the power supplies of $V_{CC}$ = 0V and $V_{EE}$ = −5.2V ± 0.25V, which are the normal ECL supply rails. They will also operate satisfactorily with TTL rails of $V_{CC}$ = +5V ± 0.25V and $V_{EE}$ = 0V.
2. The input reference voltage has the same temperature coefficient as ECL III and ECL 10K.
3. The output voltage levels have the same temperature coefficients as ECL II output levels.

## Dynamic Characteristics

| Characteristic | Type | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock input voltage levels | | | | | | |
| $V_{INH}$ | All | −1.10 | | −0.90 | V | $T_{amb}$ = +25°C, |
| $V_{INL}$ | All | −1.70 | | −1.50 | V | see Note 4 |
| Max. toggle frequency | SP8643 | 350 | | | MHz | |
| | SP8647 | 250 | | | MHz | |
| Min. frequency with sinewave clock input | All | | | 50 | MHz | |
| Min. slew rate of square wave input for correct operation down to DC | All | | | 100 | V/μs | |
| Output (ECL) | All | 500 | | | mVpp | |
| Propagation delay (clock input to device output) | All | | 3 | | ns | ECL Output |
| Set-up time | All | | 1.5 | | ns | See note 5 |
| Release time | All | | 1.5 | | ns | See note 6 |

NOTES

4. The devices are dynamically tested using the circuit shown in Fig. 5. The bias chain has the same temperature coefficient as ECL III and ECL 10K, and therefore tracks the input reference throughout the temperature range. The devices are tested with input amplitudes of 400 and 800 mV p-p about that reference, over the full temperature range.
5. Set-up time is defined as the minimum time that can elapse between a L→H transition of a control input and the next L→H clock pulse transition to ensure that the ÷10 mode is forced by that clock pulse (see Fig. 3).
6. Release time is defined as the minimum time that can elapse between a H→L transition of a control input and the next L→H clock pulse transition to ensure that the ÷11 mode is forced by that clock pulse (see Fig. 4).
7. SP8647 TTL output current = 8mA at $V_{OL}$ = +0.5V, measured at +25°C, temperature coefficient = +0.5mV/°C
8. SP8647 $Q_4$ to TTL output delay = 3ns, typical
9. The TTL O/P is a free collector and requires a 2k Ω (typ) pull-up resistor. The current taken by this resistor must be included in the 8mA current in Note 7 above.

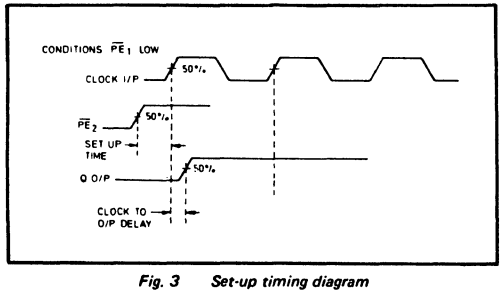



*Fig. 3 Set-up timing diagram*

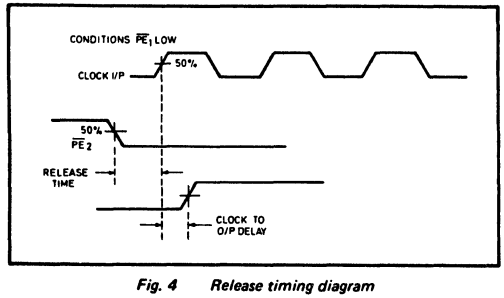



*Fig. 4 Release timing diagram*

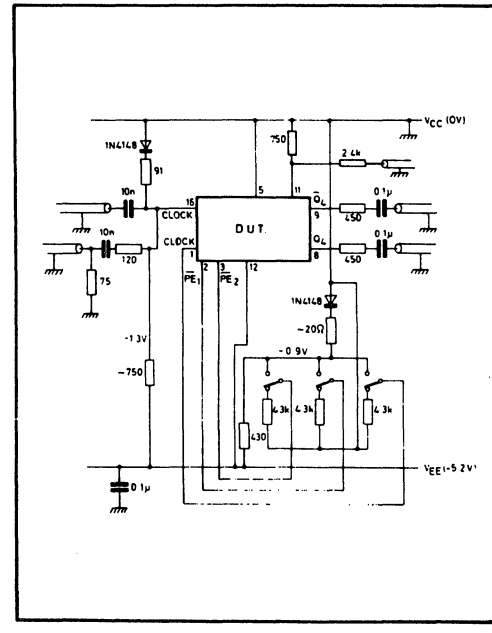



*Fig. 5 Test circuit for dynamic measurements*

## OPERATING NOTES

The SP8640 range of devices are designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g. non-inductive resistors and capacitors should be used, power supply rails decoupled, etc.

All clock and control inputs are compatible with ECL III and ECL 10K throughout the temperature range. However, it is often desirable to capacitively-couple the signal source to the clock, in which case an external bias network is required as shown in Fig. 6.

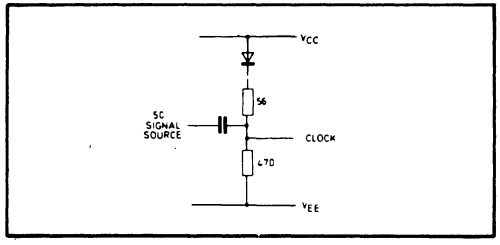



*Fig. 6 Recommended input bias configuration for capacitive coupling to a contir uous 50Ω signal source.*

The ÷10/11 can be controlled by a TTL fully programmable counter, provided that delays within the loop are kept to a minimum. The outputs and control inputs must therefore interface to TTL. The input TTL to ECL interface is accomplished with two resistors as shown in Fig. 7. The output ECL to TTL interface has been provided on chip in the SP8646/7. A discrete interface may be constructed as shown in Fig. 7. Both output interfaces will operate satisfactorily over the full military temperature range (−55°C to +125°C). The propagation delay through the divider plus the interface and one Schottky TTL gate is approximately 10 ns. At an input frequency of 350 MHz this would only leave about 16 ns for the fully-programmable counter to control the ÷10/11. The loop delay can be increased by extending the ÷10/11 function to, say, ÷20/21 or ÷40/41 (see Application Notes).

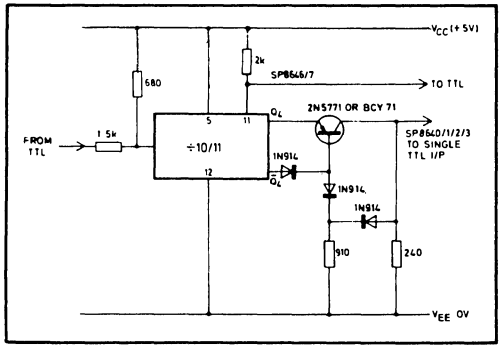



*Fig. 7 TTL to ECL and ECL/TTL interfaces (for SP8640 devices and TTL operating from the same supply rails)*

The SP8643 device ECL o/ps are compatible with ECL II levels when there is no external load. They can be made compatible with ECL III and ECL 10K with a simple potential dividing network as shown in Fig. 8.

The control and clock inputs are already compatible with ECL III and ECL 10K. The interface circuit of Fig. 8 can be used to increase noise immunity when interfacing from ECL III and ECL 10K outputs at low current levels to ECL III and ECL 10K inputs.

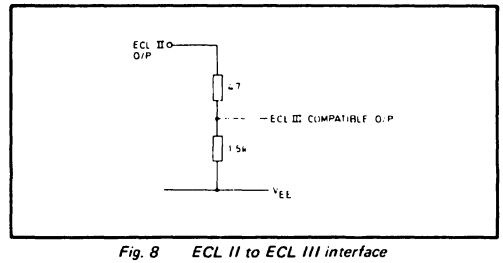



*Fig. 8 ECL II to ECL III interface*

Plessey Semiconductors

# SP8000 SERIES
## HIGH SPEED DIVIDERS

# SP8650A&B
## 600MHz÷16

The SP8650 series of UHF16 counters are fixed ratio synchronous emitter coupled logic counters with, in the case of the SP8650, a maximum operating frequency in excess of 600MHz. All three devices operate up to their maximum specified operating frequencies over temperature ranges of −55°C to +125°C ('A' grade), 0°C to +20°C ('B' grade). The input is normally capacitively coupled to the signal source but the circuits can be DC driven if required. The inputs can be either single driven relative to the on-chip reference voltage or differentially driven.

There are two complementary emitter follower outputs.

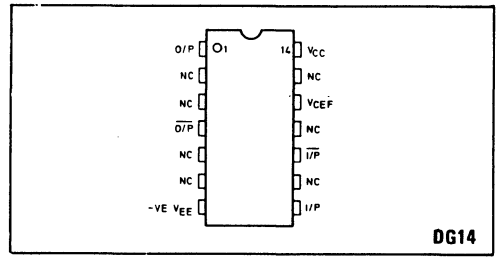



*Fig. 1 Pin connections*

## FEATURES

- Low Power - Typically 250mW
- ECL II & ECL III Output Compatability
- Easy Operation From UHF Signal Source

## APPLICATIONS

- Prescaling for UHF Synthesisers
- Instrumentation

## QUICK REFERENCE DATA

- Power Supplies Vcc = OV
  VEE = −5.2V ± 0.25V
- Temperature Range 'A' grade −55°C to +125°C
  'B' grade 0°C to +70°C
- Input Amplitude Range 400mV to 800mVp-p
- Output Voltage Swing 800mV typ. p-p

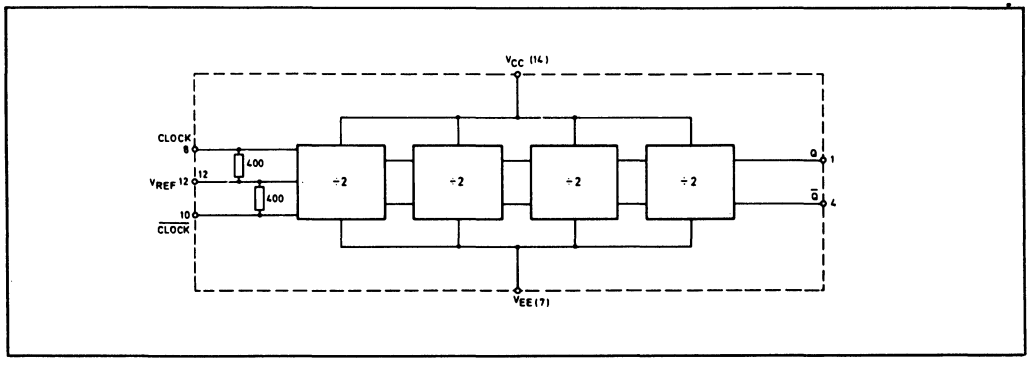



*Fig. 2 Functional diagram*

## ELECTRICAL CHARACTERISTICS

**Test Conditions (unless otherwise stated)**
$T_{amb}$ = −55°C to +125°C ('A' grade)
0°C to +70°C ('B' grade)
Supply Voltage
$V_{CC}$ = 0V
$V_{EE}$ = −5.2V ± 0.25V
Output load = 500Ω in parallel with approx. 3pF

| Characteristic | Type | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max. Toggle frequency | SP8650 | 600 | | | HMz | Test circuit as in fig. 2 $V_{IN}$ = 400 to 800mV p-p |
| Min. toggle frequency for correct operation with a sinewave input | | | | 40 | MHz | VIN = 400 to 800mV p-p |
| Min. slew rate for square wave input to guarantee correct operation to OHz | | | | 100 | V/μs | |
| Input reference voltage | | | 2.6 | | V | |
| Output voltage swing (dynamic) | | 500 | 800 | | mV | p-p |
| Output voltage (static) | | | | | | |
| high state | | −8.95 | | .615 | V | |
| Low state | | −1.83 | | −1.435 | V | |
| Power supply drain current | | | 45 | 60 | mA | |

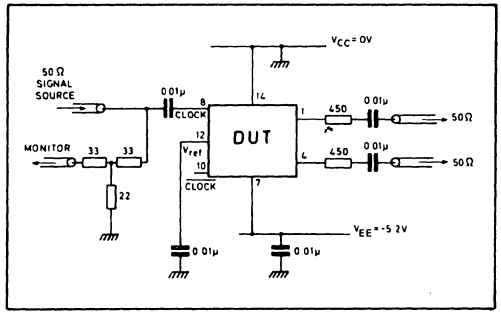



*Fig. 3 Toggle frequency test circuit*

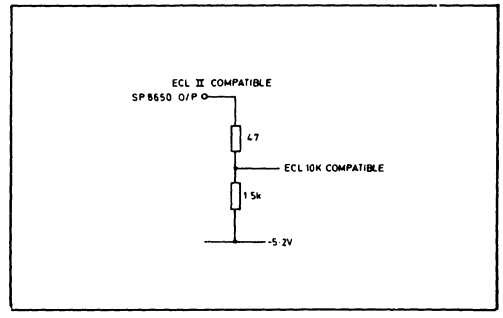



*Fig. 4 SP8650 to ECL 10K interface*

### Toggle Frequency Test Circuit

1. All leads are kept short to minimise stray capacitance and induction.
2. Resistors and capacitors are non-inductive UHF types.
3. Device is tested in a 14 lead Augat socket type No. 314-AGGA-R

## ABSOLUTE MAXIMUM RATINGS

Power supply voltage $|V_{CC} - V_{EE}|$ 8 volts
Input voltage $V_{INac}$ 2.5V p-p
Output source curr $I_{out}$ 10mA
Storage temperature range −55°C to +125°C
Operating junction temperature 150°C max.

## OPERATING NOTE

Normal UHF layout techniques should be used if the SP8650 divider is to operate satisfactorily. If the positive supply is used as the earth connection, noise immunity is improved and the risk of damage due to inadvertently shorting the output emitter followers to the negative rail is reduced.

The circuit is normally capacitively coupled to the signal source. In the absence of an input signal the circuit will self-oscillate. This can be prevented by connecting a 10KΩ resistor between one of the inputs and the negative rail.

The device will also miscount if the input transitions are slow — a slew rate of 100V/μs or greater is necessary for low frequency operation.

The outputs interface directly to ECL II or to ECL 10K with a potential divider (see Fig. 4).

A typical application of the SP8650 device would be in the divider chain of a synthesiser operating in the military frequency range 225 MHz to 512 MHz. A binary division rate is optimum where power is at a premium and so the SP8650 would normally be used in low power applications.

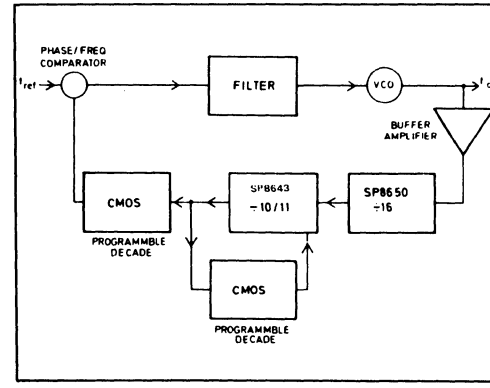



*Fig. 5 A low power synthesiser loop*

Plessey Semiconductors

# SP8000 SERIES
## HIGH SPEED DIVIDERS

# SP8655A & B (÷32)
# SP8657A & B (÷20)
# SP8659A & B (÷16)

The SP8655A, B & M, SP8657A, B & M and SP8659A, B & M are fixed ratio (divide by 32, 20 and 16) low power counters for operation at frequencies in excess of 200MHz over the temperature ranges −55 C to + 125 C ('A' grade), 0 C to + 70 C ('B' grade).

In all cases the input can be either single or double driven and must be capacitively coupled to the signal source. If single drive is used the unused input must be capacitively decoupled to the ground plane. There are two bias points, which should be capacitively decoupled to the ground plane.

The free collector saturating output stage is capable of interfacing with TTL and CMOS.

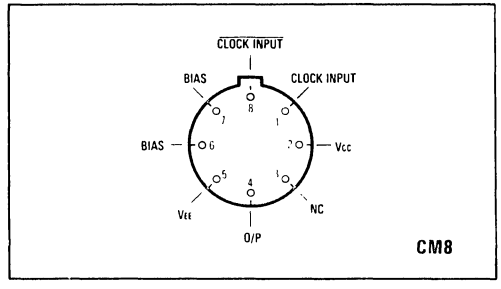



*Fig. 1 Pin connections (viewed from beneath)*

## FEATURES

- VHF Operation
- Low Power Dissipation
- Output TTL and CMOS Compatible

## APPLICATIONS

- Low Power VHF Communications
- Portable Counters

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage, $V_{CC}$—$V_{EE}$ | 8V |
| Input voltage $V_{in}$ | Not greater than supply voltage in use |
| Output sink current, $I_O$ | 10mA |
| Operating junction temperature | +150°C |
| Storage temperature | −55°C to +150°C |

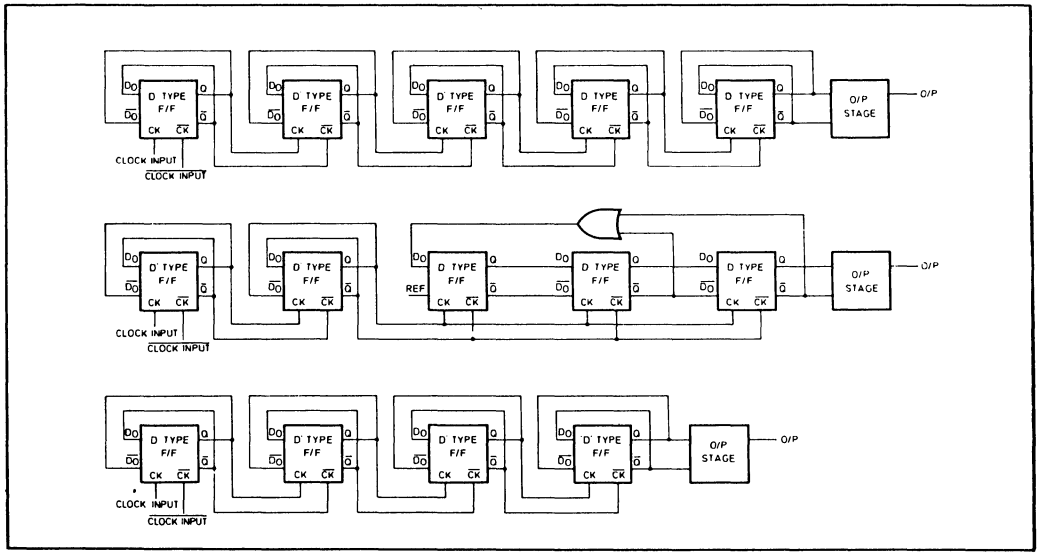



*Fig. 2 Logic diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

Operating ambient temperature $T_{amb}$: —55°C to +125°C ('A' grade)
0°C to +70°C ('B' grade)
Operating supply voltages $V_{CC}$: +5.2V±0.25V; $V_{EE}$: OV
Input voltage single drive: 400mV to 800mV p-p
double drive: 250mV to 800mV p-p
Output load 3.3k Ω to −10V, in parallel with 7pF.

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Maximum input frequency | 200 | | | MHz | |
| Minimum sinusoidal input frequency | | 20 | 40 | MHz | |
| Minimum slew rate of square wave input | | 30 | 100 | V/μs | |
| Power supply drain current | | 10 | 13 | mA | $V_{CC}$=+5.2V |
| Output level (high) | 9.0 | | | V | |
| Output level (low) | | | 400 | mV | |

## OPERATING NOTES

Fig. 3 gives capacitor values for AC and DC coupling of the input and bias points on the test circuit; these values are not critical and will depend on the operating frequency.

The devices will normally self-oscillate in the absence of an input signal. This can be easily prevented by connecting a 39k Ω pulldown resistor from either input (double drive) to $V_{EE}$; if the device is single driven then it is recommended that the pulldown resistor be connected to the decoupled unused input. The slight loss of input sensitivity resulting from this technique does not seriously affect the operation of the device.

The input waveform will normally be sinusoidal but below 40MHz correct operation depends on the slew rate of the input signal. A slew rate of 100V/μs will enable the device to operate down to DC.

The output stage will drive three TTL gates without the addition of a pull-up resistor. Using a pull-up resistor of 3.3k Ω (or less) to a +10V will allow the output to drive a CMOS binary counter at a frequency of up to 5MHz.

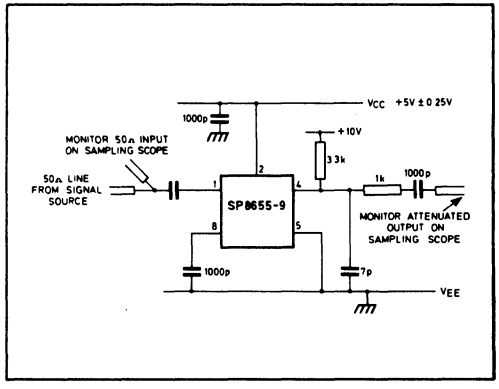



*Fig. 3 Test circuit*

# SP8656 ÷ (24)
# SP8658 ÷ (20)

The SP8656 and SP8658 are fixed ratio (divide by 24 and 20) low power counters for operation at frequencies in excess of 200MHz over the temperature ranges -30°C to -70°C.

In all cases the input can be either single or double driven and must be capacitively coupled to the signal source. If single drive is used the unused input must be decoupled to the ground plane.

The free collector saturating output stage is capable of interfacing with TTL and CMOS.

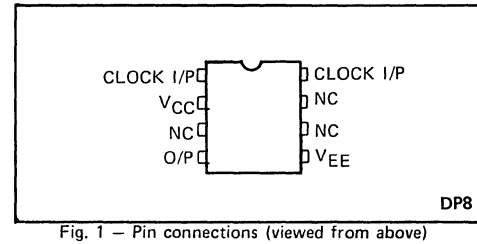



Fig. 1 – Pin connections (viewed from above)

## FEATURES

- VHF Operation
- Low Power Dissipation
- Output TTL and CMOS Compatible

## APPLICATIONS

- Low Power VHF Communications
- Portable Counters

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage: $[V_{CC} - V_{EE}]$ | 8V |
| Input voltage $V_{IN}$ | Not greater than supply voltage in use. |
| Output sink current $I_O$ | 10mA |
| Operating junction temperature | +150°C |
| Storage temperature | -55°C to +125°C |

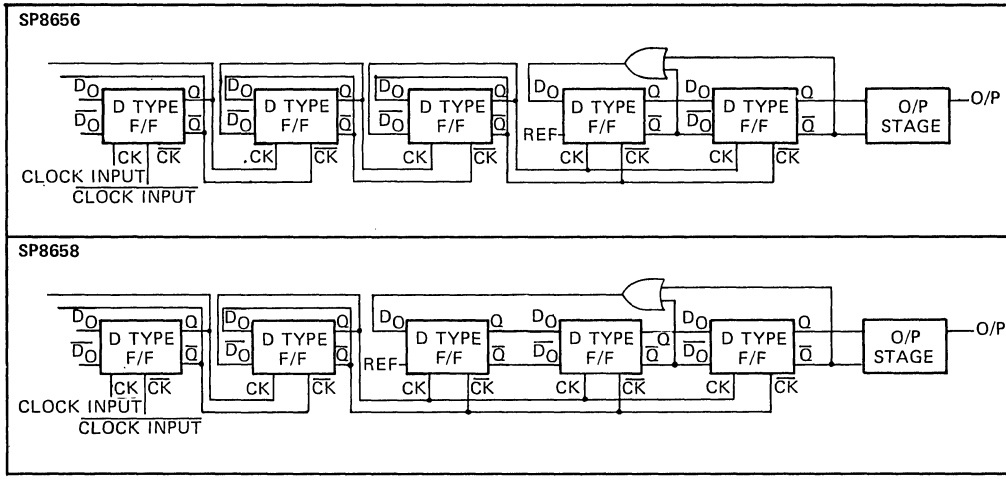



Fig. 2 Logic diagram

## ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Operating ambient temperature $T_{amb}$ -30°C to + 70°C

Operating supply voltage $V_{CC}$ : 4.75v to 5.25v

Input voltage single drive: 400mV to 800mV pk-pk

double drive: 250mV to 800mV pk-pk

Output load 3.3kΩ to -10V

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Maximum input frequency | 200 | | | MHz | |
| Minimum sinusoidal input frequency | | 20 | 40 | MHz | |
| Minimum slew rate of square wave input | | 30 | 100 | V/μsec | |
| Power supply drain current | | 20 | 30 | mA | VCC = +5.5V |
| Output level (high) | 9.0 | | | V | |
| Output level (low) | | | 400 | mV | |

## OPERATING NOTES

Fig. 3 gives capacitive values for AC and DC coupling of the input capacitor and bias points on the test circuit – these values are not critical and will depend on the operating frequency.

The devices will normally self-oscillate in the absence of an input signal. This can be easily prevented by connecting a 39kΩ resistor from either input (double drive) to $V_{EE}$; if the device is single driven then it is recommended that the pulldown resistor be connected to the decoupled unused input. The slight loss of input sensitivity resulting from this technique does not seriously affect the operation of the device.

The input waveform will normally be sinusoidal but below 40MHz. correct operation depends on the slew rate of the input signal. A slew rate of 100V/μs will enable the device to operate down to DC.

The output stage will drive three TTL gates without the addition of a pull-up resistor. Using a pull-up resistor of 3.3kΩ to a +10V will allow the output to drive a CMOS counter at a frequency of up to 5MHz.

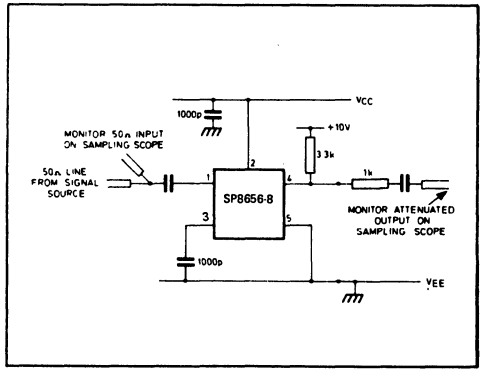



*Fig. 3 Test circuit*

# SP8660 A&B

## 200 MHz ÷ 10 (LOW POWER)

The SP8660 is a fixed ratio (divide by 10) low power counter for operation at frequencies in excess of 100MHz over the temperature ranges −55°C to +125°C ('A' grade) 0°C to +70°C ('B' grade).

The input can be either single or double driven and must be capacitively coupled to the signal source. If single drive is used, the unused input must be capacitively decoupled to the ground plane. There are two bias points, which should also be capacitively decoupled to the ground plane.

The free collector saturating output stage is capable of interfacing with TTL and CMOS.

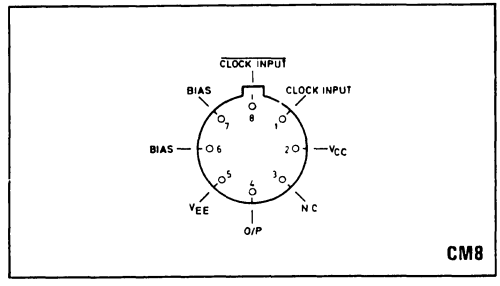



*Fig. 1 Pin connections (viewed from beneath)*

### FEATURES

- VHF Operation
- Low Power Dissipation
- Output TTL and CMOS Compatible
- Military and Commercial Temperature Ranges

### APPLICATIONS

- Low Power VHF Communications
- Portable Counters

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage, $\|V_{CC} - V_{EE}\|$ | 8V |
| Input voltage $V_{in}$ | Not greater than supply voltage in use |
| Output sink current, $I_o$ | 10mA |
| Operating junction temperature | +150°C |
| Storage temperature | −55°C to +150°C |

### OPERATING NOTES

Fig. 3 gives capacitor values for AC and DC coupling of the input and bias points on the test circuit; these values are not critical and will depend on the operating frequency.

The device will normally self-oscillate in the absence of an input signal. This can be easily prevented by connecting a 39kΩ pulldown resistor from either input (double drive) to $V_{EE}$; if the device is single driven then it is recommended that the pulldown resistor be connected to the decoupled unused input. The slight loss of input sensitivity resulting from this technique does not seriously affect the operation of the device.

The input waveform will normally be sinusoidal but below 40MHz correct operation depends on the slew rate of the input signal. A slew rate of 100V/μs will enable the device to operate down to DC.

The output stage will drive three TTL gates without the addition of a pull-up resistor. Using a pull-up resistor of 3.3kΩ (or less) to +10V will allow the output to drive a CMOS binary counter at a frequency of up to 5MHz.

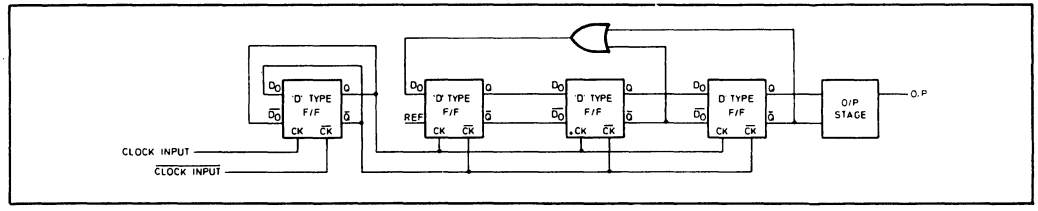



*Fig. 2 Logic diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**

Operating ambient temperature $T_A$

'A' grade: −55°C to +125°C; 'B' grade: 0°C to 70°C;

Operating supply voltages

$V_{CC}$ : +5.0V± 0.25V; $V_{EE}$ : 0V

Input voltage

Single drive: 400mV to 800mV p-p; double drive: 250mV to 800mV p-p

Output load 3.3kΩ to +10V, in parallel with 7pF

| Characteristic | Value | | | Units | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Maximum input frequency | 200 | 250 | | MHz | |
| Minimum sinusoidal input frequency | | 20 | 40 | MHz | |
| Minimum slew rate of square wave input | | 30 | 100 | V/μs | |
| Power supply drain current | | 10 | 13 | mA | $V_{CC}$ = +5.0V |
| Output level (high) | 9.0 | | | V | |
| Output level (low) | | | 400 | mV | |

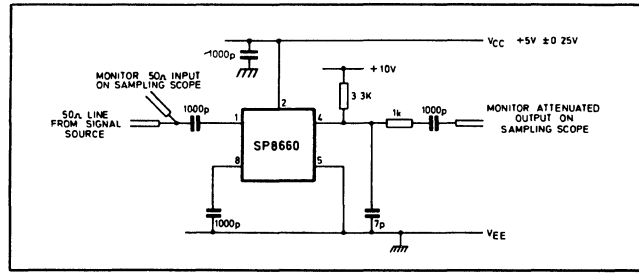



*Fig. 3 Test circuit*

Plessey Semiconductors

# SP8000 SERIES
## HIGH SPEED DIVIDERS

## UHF DECADE COUNTERS

# SP8665B 1.0GHz ÷ 10

# SP8667B 1.2GHz ÷ 10

The SP8665/7 . high speed decade counters operating at an input frequency of up to 1GHz over the temperature range 0°C to +70°C.

The device has a typical power dissipation of 550mW at the nominal supply voltage of 6.8V.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth. If no signal is present at the clock input the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15kΩ resistor from the input to $V_{EE}$ (pin 10 to pin 7). This will reduce the input sensitivity of the device by approximately 100mV.

The clock inhibit input is compatible with standard ECL III circuits using a common $V_{CC}$ to the SP8665/7. A 6kΩ pulldown resistor is included on the chip. The input should be left open circuit when not in use. The SP8665/7 outputs are compatible with standard ECL II circuits. They may be used to drive ECL 10K by the inclusion of two resistors as shown in Fig. 4.

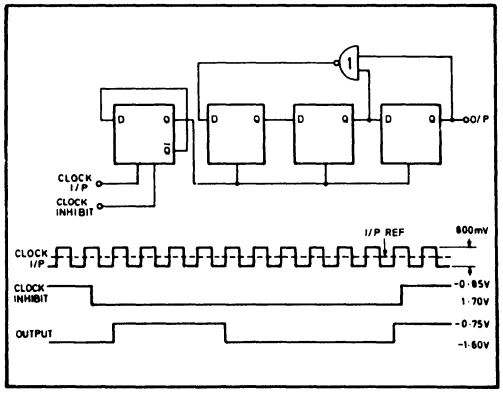



*Fig. 2 Logic diagram*

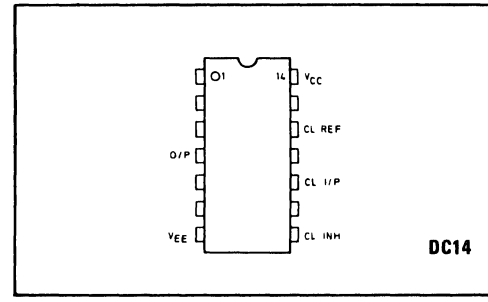



*Fig. 1 Pin connections*

## FEATURES

- Guaranteed operation over large temperature range 0°C to 70°C
- Wide input dynamic range
- Self biasing clock input
- Clock inhibit input for direct gating capability

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $V_{CC} - V_{EE}$ | 0V to +10V |
| Input voltage inhibit input | $V_{EE}$ to $V_{CC}$ |
| Input voltage CP input | 2.5V p-p |
| Output current | 20mA |
| Operating junction temperature | +150°C |
| Storage temperature | −55°C to 150°C |

## ELECTRICAL CHARACTERISTICS

**Test Conditions (unless otherwise stated):**

| | |
|---|---|
| Supply voltage | 6.8V ± 0.3V |
| Clock input | AC coupled, self-biasing |
| Clock inhibit input | ECL III compatible |
| Output | ECL II compatible |
| $T_{amb}$ | 0°C to +70°C |
| Supply voltage | $V_{CC}$ = 0V $V_{EE}$ = −6.8V |
| Clock input voltage | 400mV to 1.2V (peak to peak) |

| Characteristics | | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max. i/p frequency | SP8665 | 1.0 | | | GHz | 400mV to 1.2V p-p |
| | SP8667 | 1.2 | | | GHz | 600mV to 1.2V p-p |
| Min. i/p frequency | | | | 200 | MHz | Sine wave input 400mV p-p |
| Min. i/p frequency | | | | 100 | MHz | Sine wave input 600mV p-p |
| Min. slew rate for square wave input | | | | 200 | V/μsec | |
| Clock i/p impedance | | | 400 | | Ω | At low frequency |
| Inhibit input reference level | | | −1.3 | | V | At 25°C compatible with ECL III throughout the temperature range. |
| Inhibit input pulldown resistor (internal) | | | 6 | | kΩ | |
| Output pulldown resistor (internal) | | | 3 | | kΩ | |
| Power supply drain current | | | 80 | 105 | mA | At 25°C |

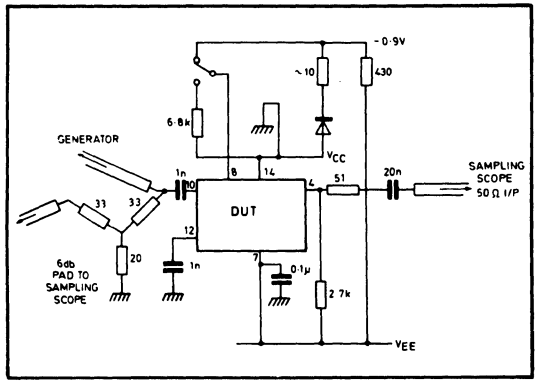



*Fig. 3 Test circuit*

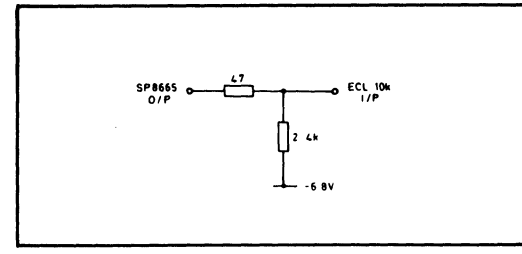



*Fig. 4 SP8665 to ECL 10K*

# SP8670 A&B

## 600MHz ÷8

The SP8670, SP8671 and SP8672 are fixed ratio –8 asynchronous ECL counters with a maximum operating frequency of 600, 500 and 400 MHz respectively. The operating temperature is specified by the final coding letter: –55°C to +125°C ('A' grade), 0°C to +70°C ('B' grade). The input is normally capacitively coupled to the signal source but the circuit can be DC driven if required. The inputs can be either single driven, relative to the on-chip reference voltage, or driven differentially. There are two complementary emitter-follower outputs.

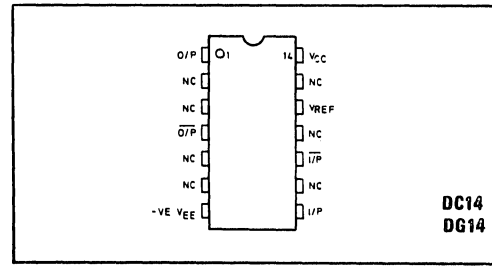



*Fig. 1 Pin connections*

### FEATURES

- Low Power – Typically 250mW
- ECL II & ECL III Output Compatibility
- Easy Operation From UHF Signal Source

### APPLICATIONS

- Prescaling for UHF Synthesisers
- Instrumentation

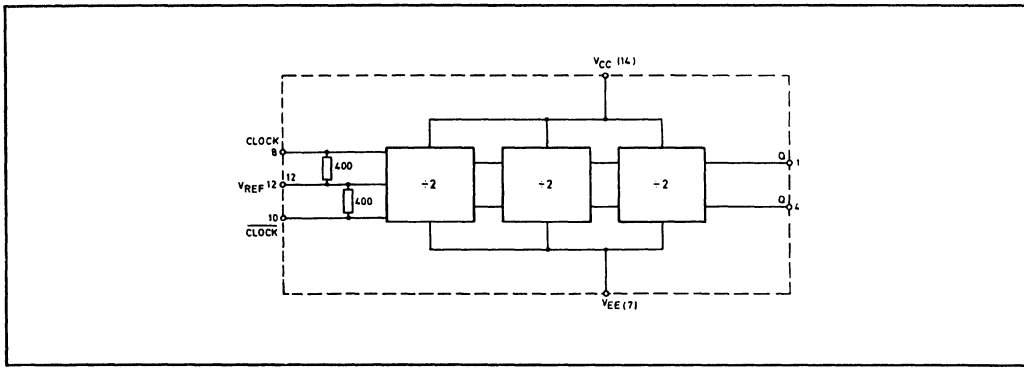



*Fig. 2 Functional diagram*

### QUICK REFERENCE DATA

| | |
|---|---|
| Power Supplies | $V_{CC}$ = 0V<br>$V_{EE}$ = –5.2V ± 0.25V |
| Input Amplitude range | 400mV to 800mV p-p |
| Output Voltage Swing | 800mV typ. p-p |
| Temp. Ranges: | –55°C to +125°C ('A' Grade)<br>0°C to +70°C ('B' Grade) |

## ELECTRICAL CHARACTERISTICS

**Test Conditions (unless otherwise stated)**

$T_{amb}$ = 'A' grade: −55°C to +125°C;
Supply Voltage 'B' grade: 0°C to 70°C;
$V_{CC}$ = 0V
$V_{EE}$ = −5.2V ± 0.25V
Output load = 500Ω line in parallel with approx. 3pF

| Characteristic | | Value | | | Units | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max. Toggle frequency | SP8670 | 600 | | | MHz | |
| Min. Toggle frequency for correct operation with a sinewave input | | | | 40 | MHz | $V_{IN}$ = 400 to 800mV p-p |
| Min. slew rate for square wave input to guarantee correct operation to 0Hz | | | | 100 | V/μs | |
| Input reference voltage | | | 2.6 | | V | |
| Output voltage swing (dynamic) | | 500 | 800 | | mV | p-p |
| Output voltage (static) | | | | | | |
| High state | | −8.95 | | .615 | V | |
| Low state | | −1.83 | | −1.435 | V | |
| Power supply drain current | | | 45 | 60 | mA | |

**Toggle Frequency Test Circuit**

1. All leads are kept short to minimise stray capacitance and inductance
2. Resistors and capacitors are non-inductive UHF types.
3. Device is tested in a 14 lead Augat socket type No. 314-AGGA-R

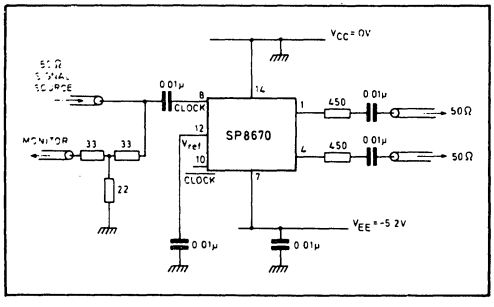



*Fig. 3 Toggle frequency test circuit*

The circuit is normally capacitively coupled to the signal source. In the absence of an input signal the circuit will self-oscillate. This can be prevented by connecting a 10KΩ resistor between one of the inputs and the negative rail.

$V_{ref}$ must be decoupled to RF earth by a capacitor in the range 30pF to 1000pF. It is important that this decoupling is adequate, otherwise input sensitivity will be reduced.

The device will also miscount if the input transitions are slow – a slew rate of 100V/μs or greater is necessary for low frequency operation.

The outputs interface directly to ECL II or to ECL 10K with a potential divider (see Fig. 4).

A typical application of the SP8670 would be in the divider chain of a synthesiser operating in the military frequency range 225 MHz to 512 MHz. A binary division ratio is optimum where power is at a premium and so the SP8670 would normally be used in low power applications.

## OPERATING NOTE

Normal UHF layout techniques should be used to ensure satisfactory operation. If the positive supply is used as the earth connection, noise immunity is improved and the risk of damage due to inadvertently shorting the output emitter followers to the negative rail is reduced.

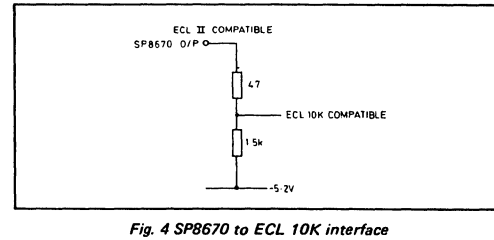



*Fig. 4 SP8670 to ECL 10K interface*

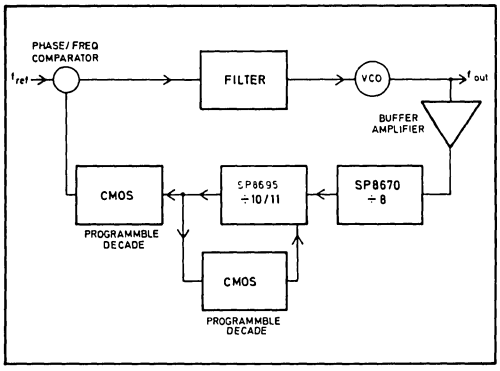



*Fig. 5 A low power synthesiser loop*

## ABSOLUTE MAXIMUM RATINGS

| | | |
|---|---|---|
| Power supply voltage | $\lvert V_{CC} - V_{EE} \rvert$ | 8 volts |
| Input voltage | $V_{INac}$ | 2.5V p-p |
| Output source current | $I_{out}$ | 10mA |
| Storage temperature range | | −55°C to +125°C |
| Operating junction temperature | | 150°C max. |

# SP8675B&M 1.0GHz ÷8
# SP8677B&M 1.2GHz ÷8

The SP8675/7 are high speed counters for operation at input frequencies up to 1.2GHz.

The devices have a typical power dissipation of 470mW at the nominal supply voltage of 6.8V.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth. If no signal is present at the clock input the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15kΩ resistor from the input $V_{EE}$ (pin 10 to pin 7). This will reduce the input sensitivity of the device by approximately 100mV.

The clock inhibit input is compatible with standard ECL III circuits using a common $V_{CC}$ to the SP8675/7. A 6kΩ pulldown resistor is included on the chip. The input should be left open circuit when not in use. The SP8675/7 outputs are compatible with standard ECL II circuits. They may be used to drive ECL 10K by the inclusion of two resistors as shown in Fig. 4.

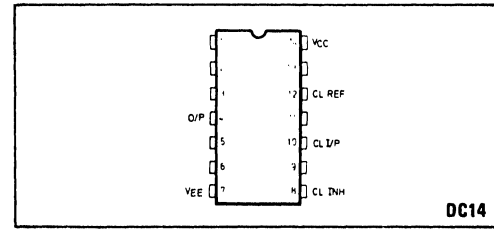



*Fig. 1 Pin connections*

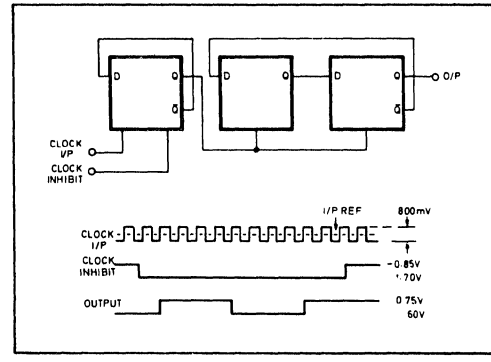



*Fig. 2 Logic diagram and timing*

## FEATURES

- Guaranteed Operation over Large Temperature Range: 'B' Grade 0°C to +70°C
  'M' Grade —40°C to +85°C
- Wide Input Dynamic Range
- Self Biasing Clock Input
- Clock Inhibit Input for Direct Gating
- Capability

## ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC}$—$V_{EE}$ 0 to 10V
Input voltage inhibit input $V_{EE}$ to $V_{CC}$
Input voltage CP input 2.5V p-p
Output current 20mA
Operating junction temperature +150°C
Storage temperature —55°C to +150°C

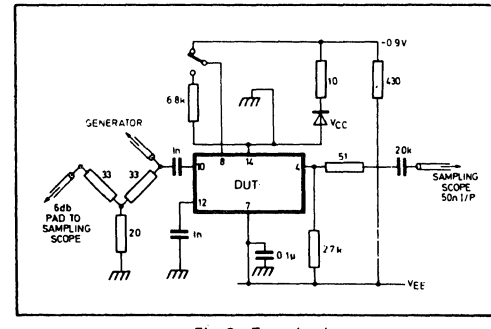



*Fig. 3 Test circuit*

## ELECTRICAL CHARACTERISTICS

**Test Conditions (unless otherwise stated)**

| | |
|---|---|
| Supply voltage | 6.8V ±0.3V |
| Clock input | AC coupled, self-biasing |
| Clock inhibit input | ECL III compatible |
| Output | ECL II compatible |
| $T_{amb}$ 'B' grade | 0°C to +70°C (see note 1) |
| 'M' grade | −40°C to +85°C (see note 1) |
| Supply voltage | $V_{CC}$ = OV $V_{EE}$ = −6.8V |
| Clock input voltage | 400mV to 1.2V (peak to peak) |

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Max. i/p frequency SP8675 | 1.0 | | | GHz | 400mV to 1.2V p-p |
| SP8677 | 1.2 | | | GHz | 600mV to 1.0V p-p |
| Min i/p frequency | | | 200 | MHz | Sine wave input 400mV p-p |
| | | | 150 | MHz | Sine wave input 600mV p-p |
| Min slew rate for square wave input | | | 200 | V/µsec | |
| Clock i/p impedance | | 400 | | Ω | At low frequency |
| Inhibit input reference level | | −1.3 | | V | At 25°C compatible with ECL III throughout the temperature range |
| Inhibit input pulldown resistor (internal) | | 6 | | kΩ | |
| Output pulldown resistor (internal) | | 3 | | kΩ | |
| Power supply drain current | | 70 | 95 | mA | at 25°C |

NOTES

1. The SP8677M is tested at $T_{case}$ = −40°C to +85°C. The SP8677M requires a suitable heatsink to be connected during operation.

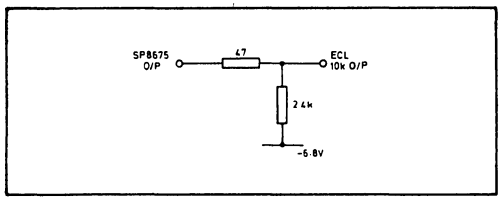



*Fig. 4 SP8675 to ECL10K interface*

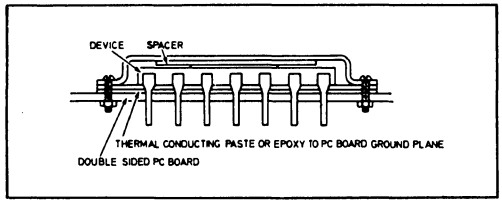



*Fig. 5 Heat sink for 'M' grade devices*

# SP8680 A& B

## 600 MHz ÷ 10/11

The SP8680 A & B are high speed programmable – 10/11 counters which operate at input frequencies up to 600 MHz over the temperature ranges -55°C to +125°C (A grade), -30°C to +70°C (B grade). The devices operate on a single +5V or T5.2V power supply and may be easily interfaced to E.C.L., or (by connecting the internal $V_{REE}$) capacitively coupled to the signal source. A clock enable, which is E.C.L. compatible, is provided. The division ratio is controlled by two mode inputs which are also ECL compatible. The counter will divide by 10 when either input is in the high state and by 11 when both inputs are low. The counter may be set to the eleventh state by applying a high level to the MS input. The set command is asynchronous and overrides the clock input. All inputs have internal -50KΩ pull down resistors, so that unused inputs may be left open circuit.

Two complementary ECL outputs are provided. They are both capable of driving 50Ω lines. A T.T.L. push pull output is also provided which may be powered up separately from the counter using the $V_{EE}$ on pin 13.

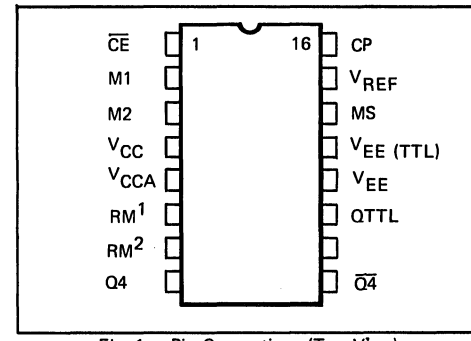



Fig. 1 – Pin Connections (Top View)

### FEATURES

- D.C. to 600 MHz operation
- ECL and TTL compatible
- D.C. or A.C. clock input
- Clock enable
- Asynchronous master set

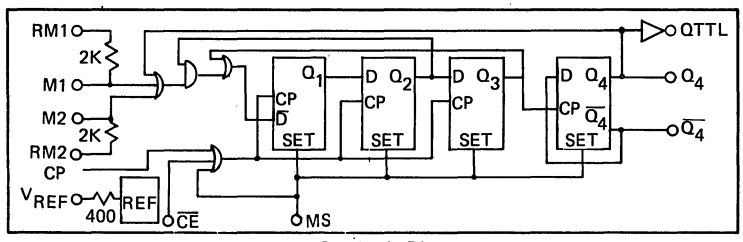
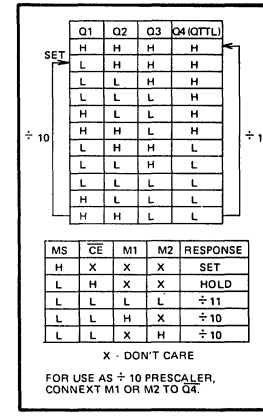



Fig. 2 – Logic Diagram




| Q1 | Q2 | Q3 | Q4 (QTTL) |
|---|---|---|---|
| H | H | H | H |
| L | H | H | H |
| L | L | H | H |
| L | L | L | H |
| H | L | L | H |
| H | H | L | H |
| L | H | H | L |
| L | L | H | L |
| L | L | L | L |
| H | L | L | L |
| H | H | L | L |

| MS | CE | M1 | M2 | RESPONSE |
|---|---|---|---|---|
| H | X | X | X | SET |
| L | H | X | X | HOLD |
| L | L | L | L | ÷11 |
| L | L | H | X | ÷10 |
| L | L | X | H | ÷10 |

X - DON'T CARE

FOR USE AS ÷ 10 PRESCALER, CONNEXT M1 OR M2 TO Q4.

Fig. 3 – Count Sequence & Control Input Truth Table

### QUICK REFERENCE DATA

- Supply voltage ($V_{CC} - V_{EE}$) = 5.0V +0.5V -0.25V
- Power consumption 400mW typ. (no load) T.T.L. output 20mW typ.
- Maximum input frequency 600 MHz SP8680B 550 MHz SP8680A
- Input amplitude (a.c. coupled) 350mV to 700mV.

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of Electrical Characteristics provides conditions for actual device operation.

| | |
|---|---|
| Power Supply Voltage | $[V_{CC} (V_{CCA}) - V_{EE}]$ -0.5 to +7V |
| Input Voltage | $V_{EE}$ TO $V_{CC}$ |
| ECL Output Source Current | 50mA |
| TTL Output Sink Current | 30mA |
| Voltage Applied to TTL Output High | $V_{EE}$ to $V_{CC}$ |
| Operating Ambient Temperature | -55°C to +125°C |
| Storage Temperature | -55°C to +150°C |

## STATIC CHARACTERISTICS

| Characteristics | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min | Typ. | Max | | |
| Guaranteed Input High Voltage $V_{INH}$ | 4.1 | | 4.4 | V | $V_{CC}$ = +5.2V<br>$T_{amb}$ = 25°C |
| Guaranteed Input Low Voltage $V_{INL}$ | 3.35 | | 3.7 | V | (See Note 2) |
| Input High Current $I_{INH}$ | | | | | $V_{CC}$ = +5.2V |
| CP and MS inputs | | | 400 | μA | $T_{amb}$ |
| M1 and M2 inputs | | | 250 | μA | $V_{INH}$ = 4.4V |
| Input Low Current $I_{INL}$ | 0.5 | | | μA | $V_{INL}$ = 3.35V |
| E.C.L. Output Low Voltage $V_{OL}$ | 3.38 | 3.49 | 3.58 | V | $V_{CC}$ = +5.2V<br>Tamb = 25°C |
| E.C.L. Output High Voltage $V_{OH}$ | 4.22 | 4.30 | 4.38 | V | Load 100Ω to +3.2V<br>(See Note 2) |
| T.T.L. Output High Voltage $V_{OH}$ | 2.7 | 3.3 | | V | $V_{CC} = V_{CCA}$ = 4.75V<br>$I_{OH}$ = -1mA<br>Tamb = 25°C |
| T.T.L. Output Low Voltage $V_{OL}$ | | 0.3 | 0.5 | V | $V_{CC} = V_{CCA}$ = 4.75V<br>$I_{OL}$ = 20mA<br>Tamb = 25°C |
| T.T.L. Output Short Circuit Current | -80 | -40 | -20 | mA | $V_{CC} = V_{CCA}$ = 5.5V<br>$V_{OUT}$ = 0V<br>Pin 14 = $V_{INH}$ |
| M1, M2 Input Low Current (using int. 2KΩ pull up) | -4.0 | -2.5 | | V | $V_{CC} = V_{CCA}$ = 5.5V<br>$V_{IN}$ = 0.4V<br>Pins 6, 7 = $V_{CC}$ |
| Power Supply Current | | 75 | 105 | mA | No Load<br>Pins 6, 7, 13 open circuit |
| T.T.L. Output Stage Supply Current | | 4 | | mA | Mean, Output High and Low |

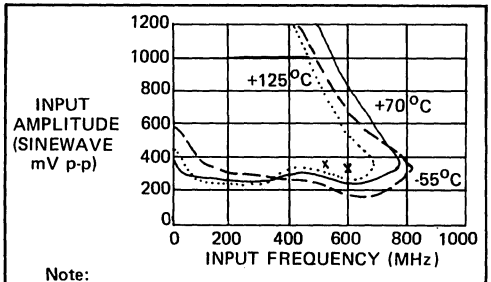
## DYNAMIC CHARACTERISTICS

| Characteristics | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min | Typ. | Max | | |
| Max. Count Frequency | | | | | $V_{CC}$ = +5.2V<br>a.c. coupled input 350mV peak to peak |
| SP8680B | 600 | | | MHz | -30°C to +70°C |
| SP8680A | 550 | | | MHz | -55°C to +125°C |
| Min. Frequency with sinewave clock input | | | 10 | MHz | $V_{CC}$ = +5.2V<br>a.c. coupled input 600mV peak to peak<br>Tamb = 25°C |
| Min. slew rate of square wave clock input | | | 20 | V/ usec | $V_{CC}$ = +5.2V |
| Propagation Delay CP to Q4 | | 2.2 | 3.0 | nsec | Tamb = 25°C |
| Propagation Delay MS to Q4 | | 4.5 | 6.0 | nsec | Ouptut Load |
| Min Set Up Time M to CP | | 2.0 | 4.0 | nsec | 100Ω to +3.2V |
| ECL Output Rise & Fall Times | | 1.3 | | nsec | |
| Propagation Delay CP to QTTL | | 8 | 14 | nsec | $V_{CC}$ = +5.0V<br>Tamb = 25°C |
| TTL Output Rise Time | | 3 | | nsec | |
| TTL Output Fall Time | | 3 | | nsec | |

Notes:

1. The SP8680 may be used in a positive earth system with $V_{CC}$ = 0V and $V_{EE}$ = -4.75V to -5.5V.
2. The input threshold has a temperature coefficient of 0.8mV/°C. This may be used to calculate $V_{INH}$ and $V_{INL}$ values at the temperature extremes.
3. The E.C.L. outputs are capable of driving a 50Ω load to +3.2V over a limited temperature range of 0°C to 70°C. The output high level will be reduced by typically 50mV.

The output high level has a temperature coefficient of 1.2mV/°C, whilst the output low level has a coefficient of 0.2mV/°C.




Note:
The above graphs are with the TTL output connected. Sensitivity in the 300 to 500 MHz frequency range is improved by 100mV peak to peak when pin 13 is disconnected.

Fig. 4 Clock Input Frequency versus Amplitude (a.c. coupled)

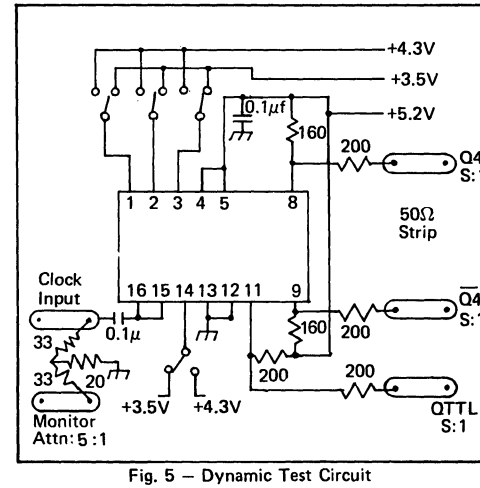
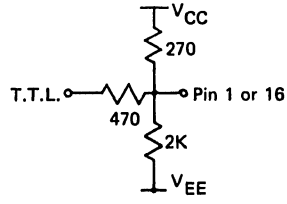



Fig. 5 – Dynamic Test Circuit

## OPERATING NOTES

The SP8680 is designed to operate in the UHF band and therefore PCB layouts should comply with normal UHF rules, e.g., short tracks, low inductance capacitors, etc.

All clock and control inputs are compatible with ECL 10K throughout the temperature range. The clock input may be capacitively coupled by connecting pin 16 to pin 15. All inputs may be interfaced with T.T.L. logic as shown in Figure 6.

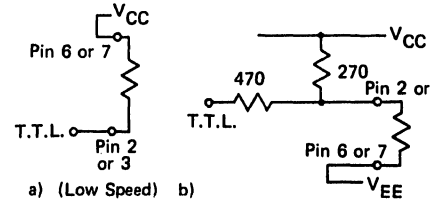



T.T.L. INTERFACE CP & $\overline{CE}$

Two E.C.L. compatible outputs are available (true and inverse) both capable of driving a 100Ω load (to +3.2V) over the full temperature range. These outputs have no internal pull down, so an external resistor to $V_{EE}$ is required when interfacing to other E.C.L. logic. A T.T.L. output is also provided which is powered up by connecting pin 13 to $V_{EE}$.

The SP8680 may be controlled by a following variable divider to produce effective variable division at up to 600 MHz. Some points to be noted when this technique is employed are as follows:

1) The 0 – 1 edge of the $Q_4$ or TTL outputs must be used to clock the following divider. This gives a maximum control loop delay time (equal to ten clock periods minus internal delays).
2) At 600 MHz the required control loop delay time is only 13 nsec. (using ECL outputs) and, hence, only an E.C.L. variable divider can be used in the control loop. A suitable device is the 10136.
3) To overcome the above problem, the modulus may be extended from 10/11 to 20/21, 40/41 to 100/101. This will considerably increase the control loop delay time so that a TTL variable divider may be used in the control loop.




T.T.L. INTERFACE M1 & M2

4) The minimum division number of a 'two modulus' n/n + 1 when employed as a fully variable divider is n(n-1). Therefore, for a 10/11, this will give 90. If the modulus has been extended to 100/101, the minimum divide number will be 9,900 which may well be too large.
5) If the above two-modulus approach does not give a satisfactory systems' solution, then a four-modulus system may be required. An example of this would be a 100/101/110/111 followed by two control dividers. The two control dividers decide on the number of +1 and +10 counts required. The minimum division number of such a system is 900.

# SP8685 A&B

## UHF PROGRAMMABLE DIVIDER 500MHz ÷ 10/11

The SP8685 A&B are high speed programmable–10/11 counters operating at an input frequency of up to 500 MHz over the temperature ranges -55°C to +125°C ('A' grade), 0°C to +70°C ('B' grade).

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 10 when either input is in the high state, and by 11 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-ten prescaler the inverse output (o/p) should be connected to a PE input.

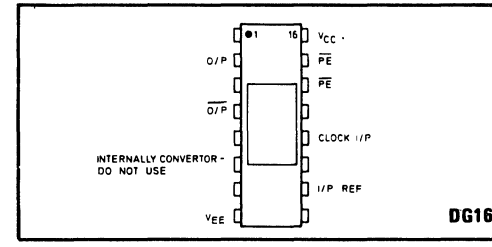



*Fig. 1 Pin connections*

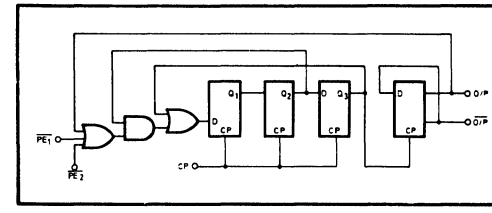



*Fig. 2 Logic diagram SP8685*

| Clock Pulse | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ |
|---|---|---|---|---|
| 1 | L | H | H | H |
| 2 | L | L | H | H |
| 3 | L | L | L | H |
| 4 | H | L | L | H |
| 5 | H | H | L | H |
| 6 | L | H | H | L |
| 7 | L | L | H | L |
| 8 | L | L | L | L |
| 9 | H | L | L | L |
| 10 | H | H | L | L |
| 11 | L | H | H | H |

*Table 1 Count sequence* Extra state

| $\overline{PE_1}$ | $PE_2$ | Div Ratio |
|---|---|---|
| L | L | 11 |
| H | L | 10 |
| L | H | 10 |
| H | H | 10 |

*Table 2 Truth table for control inputs*

### FEATURES

- Full temperature range operation:
  'A' grade -55°C to +125°C
  'B' grade 0°C to +70°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K – Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $V_{CC} - V_{EE}$ | 0V to +8V |
| Input voltage, PE inputs | 0V to $V_{CC}$ |
| Input voltage, CP input | 2V peak-to-peak |
| Output current | 20mA |
| Operating junction temperature | +150°C |
| Storage temperature | –55°C to +150°C |

## ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs – ECL 10K compatible
Outputs – ECL II compatible

**Test conditions (unless otherwise stated)**

Tamb 'A' grade -55°C to +125°C
'B' grade 0°C to +70°C

Supply voltages: $V_{CC}$ = +5.2V ±0.25V
$V_{EE}$ = 0V

Clock input voltage: 400mV to 800mV (p-p)

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Max i/p frequency | 500 | | | MHz | $V_{cc}$ = +5.2V |
| Min i/p frequency | | | 40 | | Sinewave Input |
| Min. slow rate for square wave input | | | 100 | V/μs | |
| Propogation delay (clock i/p to device o/p) | | 4 | | ns | |
| $\overline{PE}$ input reference level | | +3.9 | | V | $V_{cc}$ = +5.2V, 25°C |
| Power supply drain current | | 45 | 60 | mA | $V_{cc}$ = +5.2V, 25°C |
| $\overline{PE}$ input pulldown Resistors | | 4.3 | | KΩ | |
| Clock i/p impedance (i/p to i/p ref low frequency) | | 400 | | Ω | |

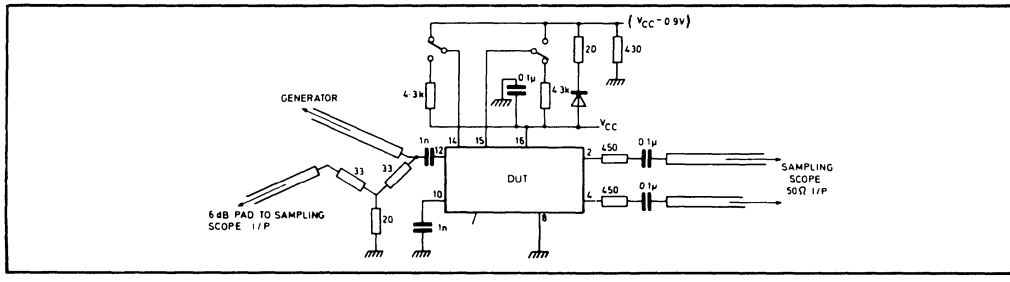



*Fig. 3 Test circuit*

## APPLICATION NOTES

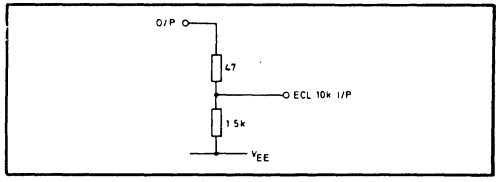



*Fig. 4 SP8685 output – ECL 10K i/p and ECLII (or ECL 10K o/ps unloaded) – ECL 10K i/p*

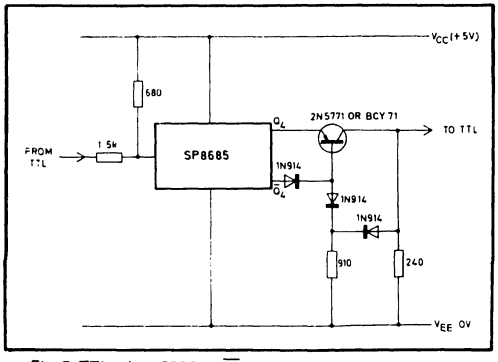



*Fig. 5 TTL o/p – SP8685 $\overline{PE}$ i/p; SL8685 o/p – TTL i/p. (Total delay from SP8685 clock i/p to Schottky gate o/p = 15ns, typ.)*

At an input frequency of 500 MHz the control loop delay time (SP8685 o/p to PE i/p) is approximately 16 ns. This will be a severe problem if TTL is used in the control loop.

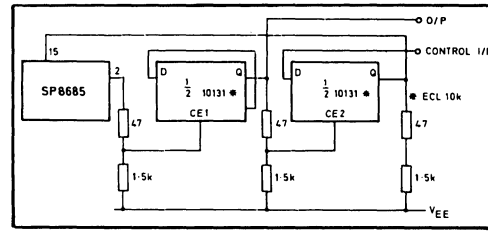



*Fig. 6 Divide-by-20/22. Control loop delay time approximately 40ns.*

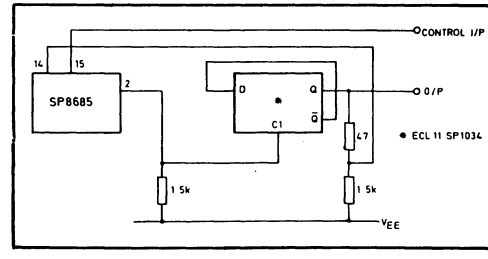



*Fig. 7 Divide-by-20/21. Control loop delay time approximately 30ns using SP1034.*

# SP8690 A & B 200 MHz ÷ 10/11
## AC COUPLED VHF, LOW POWER, PROGRAMMABLE DIVIDERS

The SP8690 A&B are divider circuits that can be logically programmed to divide by either 10 or 11.

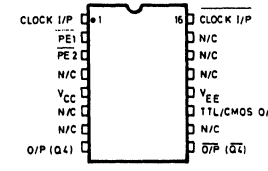
The device is available over three temperature ranges: 'A' grade is —55 °C to +125 °C and the 'B' grade is 0 °C to +70 °C.

The clock inputs can be either single or differentially driven and must be AC-coupled to the signal source. If single driven then the unused input must be decoupled to the earth plane. The device will self-oscillate if no input is present; to prevent this, a 68kΩ resistor should be connected from pin 1 or 16 to 0V. This will reduce the sensitivity of the device by approximately 100mV p-p.

The division ratio is controlled by two $\overline{PE}$ inputs which are ECL III and ECL 10K compatible throughout the temperature range. The device will divide by ten when either input is high and by eleven when both inputs are low. These inputs may be interfaced to TTL and CMOS by the inclusion of 2 resistors, as shown in Fig. 3. There is a free collector, saturating output stage for interfacing with either TTL or CMOS, together with true and inverse outputs with ECL II compatible levels. These may be interfaced to ECL 10K as shown in Fig. 4.

The device may be used as a fixed ÷10 by connecting $\overline{Q4}$ to one $\overline{PE}$ input.

If the 0 → 1 transition of Q4 (or the 1 → 0 transition of $\overline{Q4}$) is used to clock the next stage then this will give the maximum loop delay for control, i.e. 10 clock periods minus the internal delays.

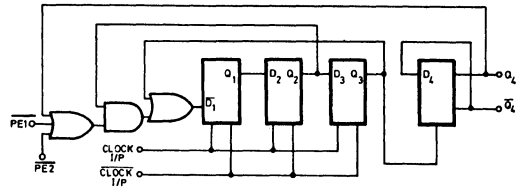



DC16
DG16

*Fig.1 Pin connections*

## FEATURES

- Full Temperature Range Operation
  'A' Grade —55 °C to —125 °C
  'B' Grade 0 °C to +70 °C
- Toggle Frequency in Excess of 200MHz
- Power Dissipation 70mW Typical
- ECL Compatibility on All Inputs
- Capacitively Coupled Clock Input for Synthesiser and Counter Applications
- True and Inverse Outputs Available with ECL Compatibility
- Output Available for Driving TTL or CMOS




| Division ratio | | | | |
|---|---|---|---|---|
| I/P | 11 | 10 | 10 | 10 |
| $\overline{PE1}$ | L | H | L | H |
| $\overline{PE2}$ | L | L | H | H |

| Count sequence | | | | |
|---|---|---|---|---|
| $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | |
| L | H | H | H | |
| L | L | H | H | |
| L | L | L | H | |
| H | L | L | H | |
| H | H | L | H | |
| L | H | H | L | |
| L | L | H | L | |
| L | L | L | L | |
| H | L | L | L | |
| H | H | L | L | |
| H | H | H | H | Extra state |

*Fig.2 Logic diagram*

## ELECTRICAL CHARACTERISTICS

**Test Conditions (unless otherwise stated):**

$T_{amb}$ 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
Supply voltage $V_{CC}$ = +5V ±0.25V
$V_{EE}$ = 0V
Clock I/P voltage 400mV to 800mV peak to peak
Pin 16 (decoupled to 0V)

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Max. toggle frequency | 200 | | | MHz | |
| Min. freq. with sine wave clock input | | 15 | | MHz | |
| Min. slew rate of square wave I/P for correct operation | | 40 | | V/µs | |
| $\overline{PE}$ input levels | | | | | |
| $V_{INH}$ | +4.1 | | +4.5 | V | $V_{CC}$=+5V |
| $V_{INL}$ | 0.0 | | +3.5 | V | $T_{amb}$=+25°C (note 1) |
| Q4 & $\overline{Q4}$ output voltage levels | | | | | $T_{amb}$=+25°C (note 2) |
| $V_{OH}$ | 4.15 | | | V | $I_{out}$ (external) = 0mA |
| $V_{OL}$ | | | +3.5 | V | (There is internal circuitry equivalent to a 3.8kΩ pulldown resistor on each output) |
| TTL/CMOS output voltage levels | | | | | |
| $V_{OL}$ | | | +0.4 | V | Sink current 3.2mA on |
| $V_{OH}$ | see note 3 | | | | TTL output |
| Input pulldown resistors between input pins 2 & 3 and −ve rail | | 10 | | kΩ | |
| Power supply drain current | | 14 | 19 | mA | $V_{CC}$=+5V; $T_{amb}$=25°C |
| Impedance of clock I/P | | 1.6 | | kΩ | in=0Hz |
| Clock to TTL output delay (O/P −ve going) | | 22 | | ns | 8mA sink current |
| Clock to TTL output delay (O/P −ve going) | | 8 | | ns | TTL output |
| Clock to ECL output delay | | 6 | | ns | |
| Set up time | | 2 | | ns | See note 4 |
| Release time | | 4 | | ns | See note 5 |

NOTES
1. The $\overline{PE}$ reference voltage level is compatible with ECL II and ECL 10k over the specified temperature range.
2. The Q4 and $\overline{Q4}$ output levels are compatible with ECL II and ECL 10k over the specified temperature range.
3. The TTL/CMOS output has a free collector, and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed +12V.
4. Set up time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷10 mode is forced by that clock pulse.
5. Release time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷11 mode is forced by that clock pulse.

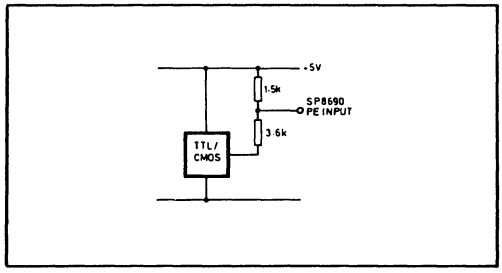



*Fig.3 TTL/CMOS interface*

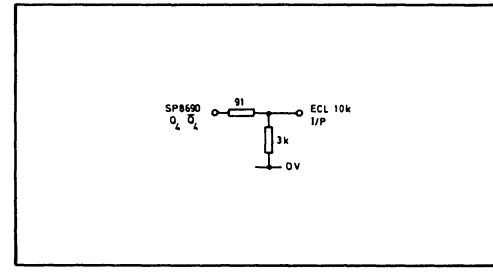



*Fig.4 ECL 10K output interface*

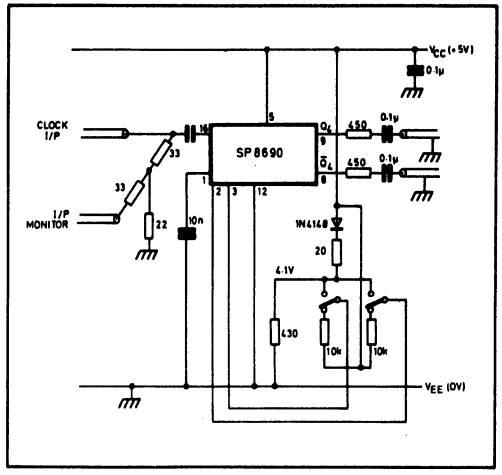



*Fig.5 Test circuit for dynamic measurements*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage\|Vcc—VEE\| | V8 |
| Input voltage VIN d.c. | Not greater than the supply voltage in use |
| Output current $I_{out}$ ($Q_4$ & $\overline{Q_4}$) | 10mA |
| Maximum junction temperature | 150°C |
| Storage temperature range | −55°C to +150°C |

# SP8691 A & B

## 200 MHz ÷ 8/9

The SP8691 A & B are divider circuits that can be logically progressed to divide by either 8 or 9.

The device is available over two temperature ranges, 'A' variant is -55°C to +125°C and the 'B' variant is 0°C to +70°C.

The clock inputs can be either single or differentially driven and must be a.c. coupled to the signal source. If single driven then the unused input must be decoupled to the earth plane. The device will self-oscillate if no input is present. To prevent this a 68k resistor should be connected from pin 1 or 16 to OV. This will reduce the sensitivity of the device by approximately 100mV p-p.

The division ratio is controlled by two $\overline{PE}$ inputs which are ECL $\overline{III}$, 10k compatible throughout the temperature range. The device will divide by eight when either input is high and by nine when both inputs are low. These inputs may be interfaced to TTL and CMOS by the inclusion of 2 resistors as shown in Fig. 3. There is a free collector, saturating output stage for interfacing with either TTL or CMOS together with true and inverse outputs with ECL II compatible levels. These may be interfaced to ECL 10k as shown in Fig. 4.

The device may be used as a fixed ÷8 by connecting $\overline{Q4}$ to one $\overline{PE}$ input.

If the 0 → 1 transition of Q4 or the 1 → 0 transition of $\overline{Q4}$ is used to clock the next stage then this will give the maximum loop delay for control i.e., 8 clock periods minus the internal delays.

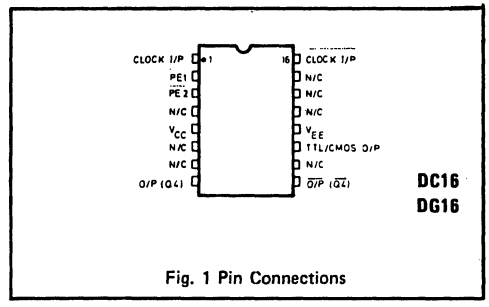


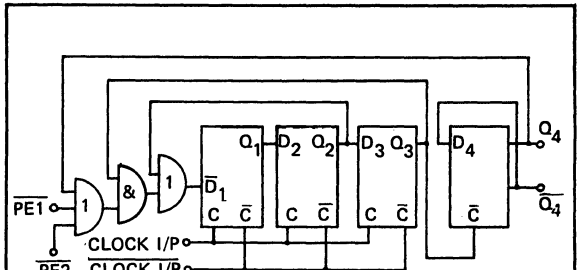

Fig. 1 Pin Connections

## FEATURES

Full temperature range operation

'A' variant -55°C to +125°C
'B' variant 0°C to +70°C

Toggle frequency in excess of 200MHz
Power dissipation 70mW typical
ECL compatibility on all inputs
Capacitively coupled clock input for synthesiser and counter applications
True and inverse outputs available with ECL compatibility
Output available for driving TTL or CMOS




| COUNT SEQUENCE | | | | DIVISION RATIO |
|---|---|---|---|---|
| $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | 9 8 8 8 |
| H | L | L | H | |
| H | H | L | H | $\overline{PE1}$ L H L H |
| L | H | H | H | |
| L | L | H | H | $\overline{PE2}$ L L H H |
| H | L | L | L | |
| H | H | L | L | |
| L | H | H | L | |
| L | L | H | L | |

## ABSOLUTE MAXIMUM RATINGS

Supply voltage $V_{CC} - V_{EE}$ 8V

Input voltage $V_{IN}$ d.c. Not greater than the supply voltage in use

Output current $I_{out}(Q_4$ & $\overline{Q_4})$ 10mA

Maximum junction temperature 150°C

Storage temperature range -55°C to +150°C

## ELECTRICAL CHARACTERISTICS

**Test Conditions** (unless otherwise stated)

$T_{amb}$ 'A' variant -55°C to +125°C
'B' variant 0°C to +70°C

Supply voltage $V_{CC}$ = +5V ± 0.25V
$V_{EE}$ = $O_V$

Clock I/P voltage 400mV to 800mV peak to peak
($\overline{\text{Clock I/P}}$ decoupled to $O_V$)

| Characteristics | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| Max. toggle frequency | 200 | | | MHz | |
| Min. freq. with sine wave clock input | | 15 | | MHz | |
| Min. slew rate of square wave i/p for correct operation | | 40 | | V/μs | |
| PE input levels | | | | | |
| $V_{IMH}$ | +4.1 | | +4.5 | volts | $V_{CC}$ = +5V |
| $V_{INL}$ | 0.0 | | +3.5 | volts | $T_{amb}$ = +25°C (note 1) |
| Q4 & Q4 output voltage levels | | | | | $T_{amb}$ = +25°C (note 2) |
| $V_{OH}$ | 4.15 | | | volts | $1_{out}$ (external) = OmA |
| $V_{OL}$ | | | +3.5 | volts | (There is internal circuitry equivalent to a 3.8k ohms pulldown resistor on each output.) |
| TTL/CMOS output voltage levels | | | | | |
| $V_{OL}$ | see | | +0.4 | volts | Sink current 3.2mA on |
| $V_{OH}$ | note 3 | | | | TTL output. |
| Input pulldown resistors between input pins 2 & 3 and -ve rail | | 10 | | k ohms | |
| Power supply drain current | | 14 | | mA | $V_{CC}$ = +5V<br>$T_{amb}$ = +25°C |
| Impedance of clock i/p | | 1.6 | | k ohms | $F_{IN}$ = OHz |

NOTE 1

The $\overline{PE}$ reference voltage level is compatible with ECL II and 10k over the specified temperature range.

NOTE 2

The $Q_4$ and $\overline{Q_4}$ output levels are compatible with ECL II and 10k over the specified temperature range.

NOTE 3

The TTL/CMOS output has a free collector, and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed +12V.

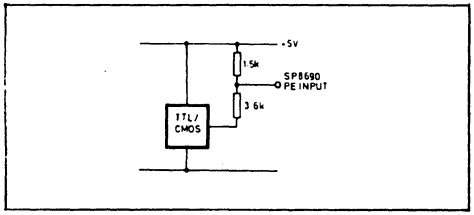



*Fig.3 TTL/CMOS interface*

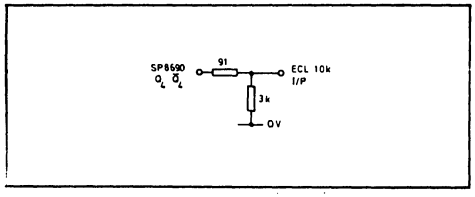



*Fig.4 ECL 10K output interface*

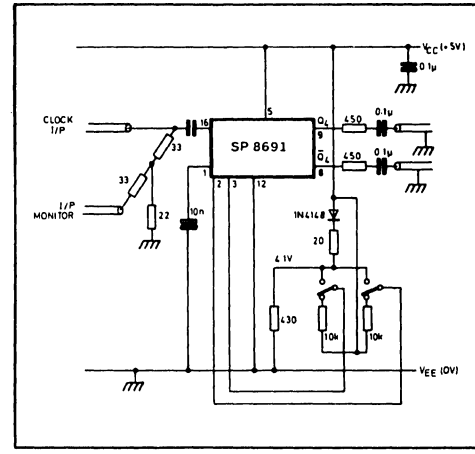



*Fig.5 Test circuit for dynamic measurements*

# SP8695 A & B 200 MHz ÷ 10/11

## DC COUPLED VHF, LOW POWER, PROGRAMMABLE DIVIDERS

The SP8695 A&B are divider circuits that can be logically programmed to divide by either 10 or 11.

The device is available over two temperature ranges, 'A' grade is —55 C to + 125 C, the 'B' grade is 0 C to + 70 C.

The clock inputs are ECL II, III & 10K compatible throughout the temperature range (see note 1).

The division ratio is controlled by two $\overline{PE}$ inputs which are ECL III and ECL 10K compatible throughout the temperature range. The device will divide by ten when either input is high and by eleven when both inputs are low. These inputs may be interfaced to TTL and CMOS by the inclusion of 2 resistors, as shown in Fig. 3. There is a free collector, saturating output stage for interfacing with either TTL or CMOS, together with true and inverse outputs with ECL II compatible levels. These may be interfaced to ECL 10K as shown in Fig. 4.

The device may be used as a fixed : 10 by connecting $\overline{Q4}$ to one $\overline{PE}$ input.

If the 0 → 1 transition of Q4 (or the 1 → 0 transition of $\overline{Q4}$) is used to clock the next stage then this will give the maximum loop delay for control, i.e. 10 clock periods minus the internal delays.

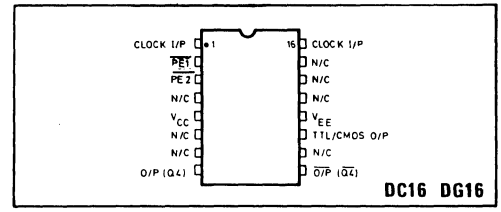
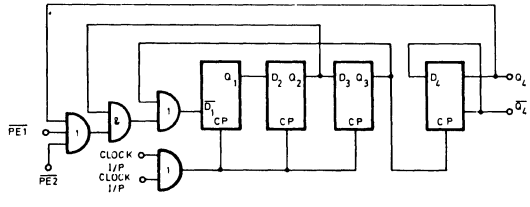



*Fig.1 Pin connections*

## FEATURES

- Full Temperature Range Operation
  'A' Grade —55 °C to +125 °C
  'B' Grade 0 °C to +70 °C
- Toggle Frequency in Excess of 200MHz
- Power Dissipation 80mW Typ.
- ECL Compatibility on All Inputs
- Excellent Low Frequency Operation
- True and Inverse Outputs Available with ECL Compatibility.
- Output Available for Driving TTL or CMOS




| Division ratio | | | | |
|---|---|---|---|---|
| I/P | 11 | 10 | 10 | 10 |
| $\overline{PE1}$ | L | H | L | H |
| $\overline{PE2}$ | L | L | H | H |

| Count sequence | | | | |
|---|---|---|---|---|
| $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | |
| L | H | H | H | |
| L | L | H | H | |
| L | L | L | H | |
| H | L | L | H | |
| H | H | L | H | |
| L | H | H | L | |
| L | L | H | L | |
| L | L | L | L | |
| H | L | L | L | |
| H | H | L | L | |
| H | H | H | H | Extra state |

*Fig.2 Logic diagram*

## ELECTRICAL CHARACTERISTICS

**Test Conditions (unless otherwise stated):**

$T_{amb}$ 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
Supply voltage $V_{CC}$ = +5V ±0.25V
$V_{EE}$ = 0V

| Characteristics | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Max. toggle frequency | 200 | | | MHz | |
| Min. freq. with sine wave clock input | | 1 | | MHz | |
| Min. slew rate of square wave I/P for correct operation | | 3 | | V/µs | |
| Clock I/P voltage levels | | | | | |
| $V_{INH}$ | +4.0 | | 4.2* | V | $V_{ref}$ = +3.8V |
| $V_{INL}$ | −3.4* | | +3.6 | V | at $T_{amb}$ = 25°C (note 1) |
| $\overline{PE}$ input levels | | | | | |
| $V_{INH}$ | +4.1 | | +4.5 | V | $T_{amb}$ = +25°C (note 2) |
| $V_{INL}$ | 0.0 | | +3.5 | V | |
| Q4 & $\overline{Q4}$ output voltage levels | | | | | $T_{amb}$ = +25°C (note 3) |
| $V_{OH}$ | +4.15 | | | V | $I_{out}$ (external) = 0mA |
| $V_{OL}$ | | | +3.5 | V | (There is internal circuitry equivalent to 1 3.8kΩ pulldown resistor on each output) |
| TTL/CMOS output voltage levels | | | | | |
| $V_{OL}$ | | | +0.4 | V | Sink current 3.2mA on TTL output |
| $V_{OH}$ | see note 4 | | | | |
| Input pulldown resistors between input pins 1, 2, 3 & 16 and −ve rail | | 10 | | kΩ | |
| Power supply drain current | | 16 | 21 | mA | $V_{CC}$ = +5V; $T_{amb}$ = +25°C. |
| Clock to TTL output delay (O/P +ve going) | | 22 | | ns | 8mA sink current |
| Clock to TTL output delay (O/P −ve going) | | 8 | | ns | TTL output |
| Clock to ECL output delay | | 6 | | ns | |
| Set up time | | 2 | | ns | See note 5 |
| Release time | | 4 | | ns | See note 6 |

NOTES
1. This reference level of +3.8V will enable the clock inputs to be driven from ECL II, III & 10K when their outputs are sinking 3mA. The input reference voltage is compatible with ECL II, III and 10k over the specified temperature range.
2. The $\overline{PE}$ reference voltage level is compatible with ECL II and 10k over the specified temperature range.
3. The Q4 and $\overline{Q4}$ output levels are compatible with ECL II and ECL 10k over the specified temperature range.
4. The TTL/CMOS output has a free collector, and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed +12V.
5. Set up time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷10 mode is forced by that clock pulse.
6. Release time is defined as the minimum time that can elapse between a L—H transition of a control input and the next L—H clock pulse transition to ensure that the ÷11 mode is forced by that clock pulse.

*High frequency limits only.

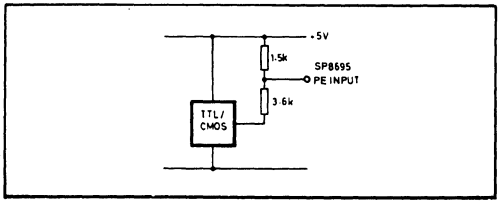



*Fig.3 TTL/CMOS interface*

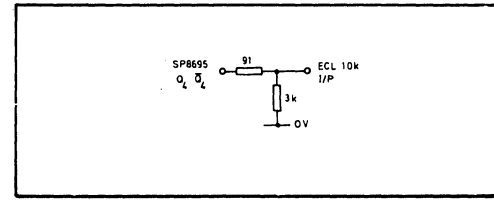



*Fig.4 ECL 10K output interface*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$—$V_{EE}$ | V8 |
| Input voltage $V_{IN}$ d.c. | Not greater than the supply voltage in use |
| Output current $I_{out}$ ($Q_4$ & $Q_4$) | 10mA |
| Maximum junction temperature | 150 C |
| Storage temperature range | —55 C to 150 C |

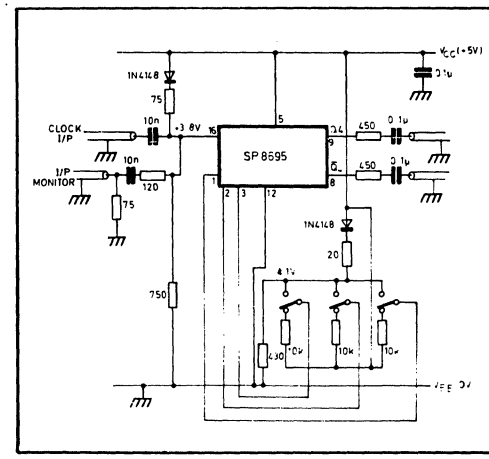



*Fig.5 Test circuit for dynamic measurements*

Plessey Semiconductors

# SP8000 SERIES

## HIGH SPEED DIVIDERS

# SP 8720 A & B

## UHF PROGRAMMABLE DIVIDER 300 MHz ÷ 3/4

The SP8720 A & B are high speed programmable ÷3/4 counters operating at an input frequency of up to 300MHz over the temperature ranges —55°C to +125°C, 0°C to +70°C.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 3 when either input is in the high state, and by 4 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-three prescaler the inverse output ($\overline{Q2}$) should be connected to a $\overline{PE}$ input.

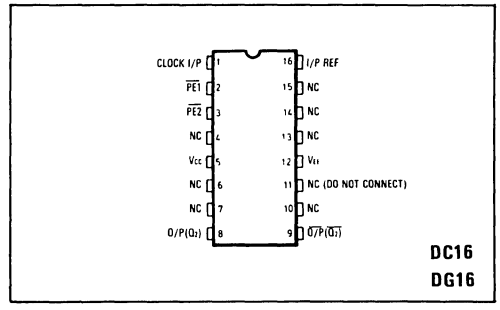



*Fig. 1 Pin connections (top view)*

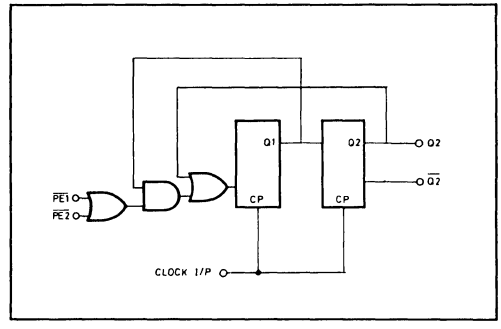



*Fig. 2 Logic diagram SP8720*

### FEATURES

- Full temperature range operation :
  - 'A' Grade —55°C to +125°C
  - 'B' Grade 0°C to + 70°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K - Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage \| Vcc - VEE \| | 0V to +8V |
| Input voltage, $\overline{PE}$ inputs | 0V to Vcc |
| Input voltage, CP input | 2V peak-to-peak |
| Output current | 20mA |
| Operating junction temperature | +150°C |
| Storage temperature | —55°C to + 150°C |

| Clock Pulse | $Q_1$ | $Q_2$ | |
|---|---|---|---|
| 1 | L | H | |
| 2 | L | L | |
| 3 | H | L | |
| 4 | H | H | ← Extra State |

*Table 1 Count sequence*

| $\overline{PE_1}$ | $\overline{PE_2}$ | Div Ratio. |
|---|---|---|
| L | L | 4 |
| H | L | 3 |
| L | H | 3 |
| H | H | 3 |

*Table 2 Truth table for control inputs*

## ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs - ECL 10K compatible
Outputs - ECL II compatible

**Test conditions (unless otherwise stated)**
Tamb 'A' Grade: −55°C to +125°C
'B' Grade: 0°C to + 70°C
Supply voltages: $V_{CC}$ = + 5.2V ±0.25V
$V_{EE}$=0V
Clock input voltage: 400mV to 800mV (p-p)

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Max. i/p frequency | 300 | | | MHz | Vcc= + 5.2V |
| Min.i/p frequency | | | 40 | | Sinewave Input |
| Min. slew rate for square wave input | | | 100 | V/μs | |
| Propagation delay (clock i/p to device o/p) | | 4 | | ns | |
| PE input reference level | | + 3.9 | | V | $V_{cc}$ = + 5.2V, 25°C |
| Power supply drain current | | 40 | 55 | mA | $V_{cc}$ = + 5.2V, 25°C |
| PE input pull down resistors | | 4.3 | | kΩ | |
| Clock i/p impedance (i/p to i/p ref. low frequency) | | 400 | | Ω | |

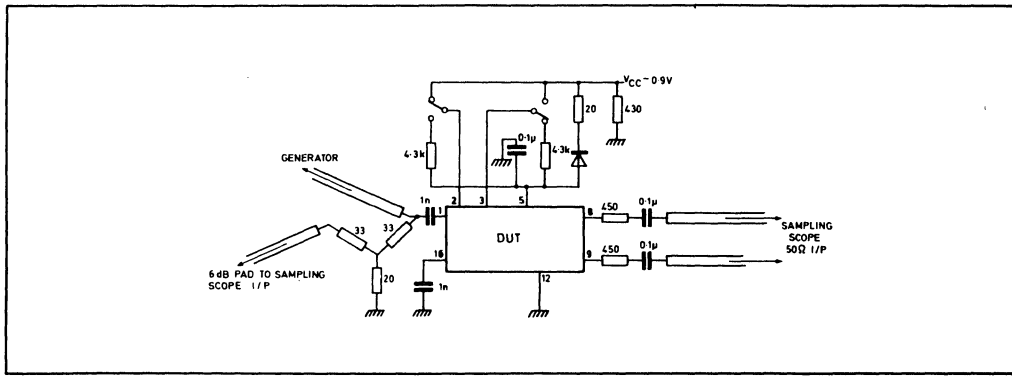



*Fig. 3 Test circuit*

## APPLICATION NOTES

When operating the SP8720 in a synthesiser loop at 300MHz, the delay time through the programmable divider controlling the SP8720 is approximately 5.5ns, and will require ECL.

The simple passive interface from the output of the SP8720 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins, and the output of the SP8720 into TTL, is shown in Fig.5.

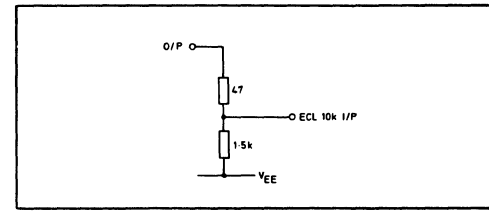



*Fig. 4*

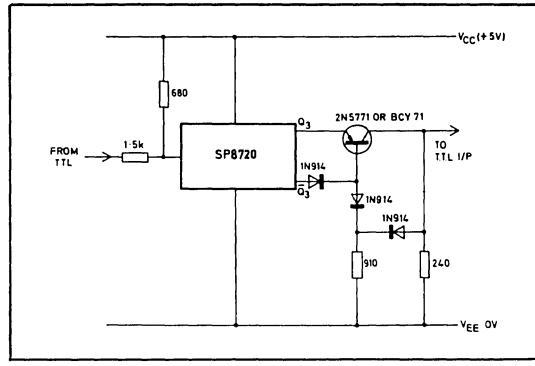



*Fig. 5*

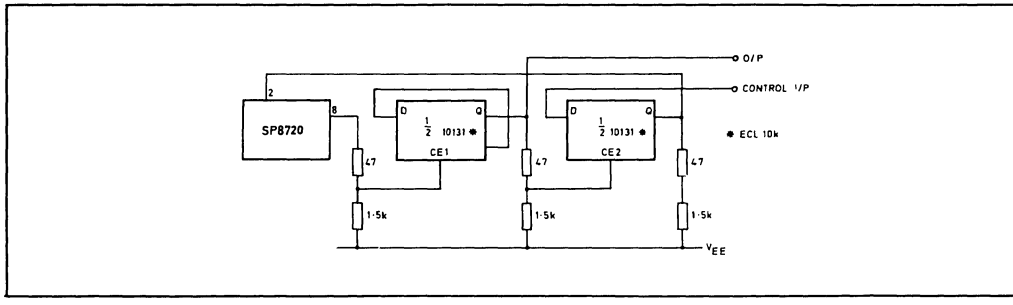



*Fig. 6 Divide by 6/8 Control loop delay time approximately 20ns at 300MHz I/P frequency*

# SP8735B
## ÷8 AT 600MHz WITH BINARY OUTPUTS

The SP8735B is a divide-by-eight circuits with binary outputs for operation from DC up to specified input frequencies of 600 MHz and 500 MHz respectively over a guaranteed temperature range of 0°C to +70°C.

This device, optimised for counter applications in systems using both ECL and TTL, are intended to be operated between 0V and −5.2V power rails and to interface with TTL operating between 0V and +5V. The binary outputs and one of two carry outputs are TTL-compatible, while the second carry output is ECL-compatible. The clock input, which is normally capacitively coupled to the signal source, is gated by an ECL III/ECL 10K compatible input. The TTL-compatible reset forces the 0000 state regardless of the state of the other inputs.

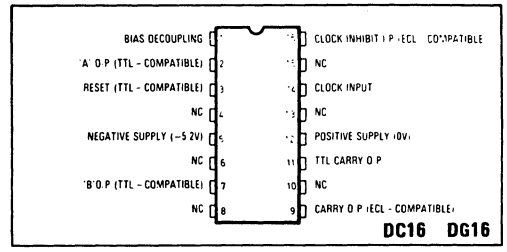



*Fig.1 Pin connections (viewed from top)*

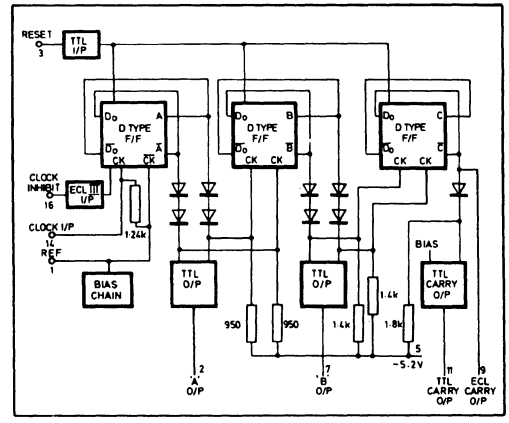



*Fig.2 SP8735 logic diagram*

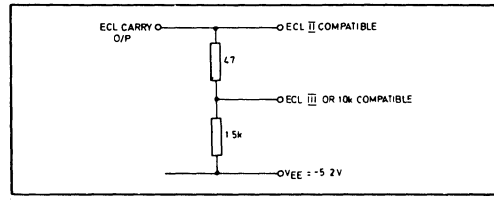



*Fig.3 ECL II to ECL 10K interface*

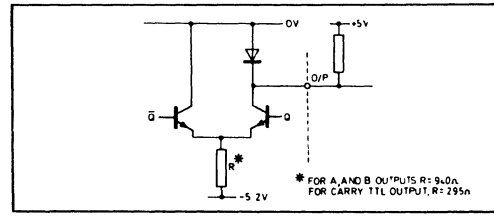



*Fig. 4 TTL output circuit diagram*

### FEATURES

- Direct Gating Capability at up to 600 MHz
- TTL Compatible Binary Outputs
- TTL and ECL Compatible Carry Outputs
- Power Consumption Less Than 450mW
- Wide Dynamic Input Range

### APPLICATIONS

- Counters
- Timers
- Synthesisers

### QUICK REFERENCE DATA

- Power Supplies : $V_{cc}$ 0V
  $V_{ee}$ −5.2V ± 0.25V
- Range of Clock Input Amplitude : 400 – 800 mV p-p
- Operating Temperature Range : 0°C to 70°C
- Frequency Range with Sinusoidal I/P : 40 – 600MHz
- Frequency Range with Square Wave I/P : DC to 600MHz

## ELECTRICAL CHARACTERISTICS (All types except where otherwise stated)

**Test conditions (unless otherwise stated):**
$T_{amb}$ 0°C to +70°C
Power Supplies $V_{CC}$ 0V
$V_{EE}$ −5.2V ±0.25V

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Clock input (pin 14)** | | | | | |
| Max. input frequency SP8735B | 600 | | | MHz | Input voltage 400–800mV p-p |
| Min. input frequency with sinusoidal I/P | | | 40 | MHz | |
| Min. slew rate of square wave for correct operation down to DC | | | 100 | V/µs | |
| **Clock inhibit input (pin 16)** | | | | | |
| High level (inhibit) | −0.960 | | | V | $T_{amb}$ = +25°C (see note 1) |
| Low level | | | −1.650 | V | |
| Edge speed for correct operation at max. clock I/P frequency | | | 2.5 | ns | 10% to 90% |
| **Reset input (pin 3)** | | | | | |
| High level (reset) | See note 2 | | | | See note 2 |
| Low level | | | +0.4 | V | |
| Reset ON time | 100 | | | ns | |
| **TTL outputs A & B (pins 2 & 7)** | | | | | |
| Output high level | +2.4 | | | V | 10k Ω resistor and 3 TTL gate |
| Output low level | | | +0.4 | V | from O/P to 5V rail (see note 3) |
| **TTL carry output (pin 11)** | | | | | |
| Output high level | +2.4 | | | V | 5k Ω resistor and 3 TTL gates from O/P to +5V rail |
| Output low level | | | +0.4 | V | |
| **ECL carry output (pin 9)** | | | | | |
| Output high level | −0.975 | | | V | $T_{amb}$ = +25°C |
| Output low level | | | −1.375 | V | External current = 0mA (See note 4) |
| Power supply drain current | | 70 | 90 | mA | $V_{EE}$ − 5.2V |

NOTES

1. The clock inhibit input levels are compatible with the ECL III and ECL 10K levels throughout the temperature ranges specified.
2. For a high state, the reset input requires a more positive input level than the specified worst case TTL $V_{OH}$ of +2.4V. Resetting should be done by connecting a 1.8k Ω resistor from the output of the driving TTL gate and only fanning out to the reset input of the SP8000 series devices.
3. These outputs are current sources which can be readily made TTL compatible voltages by connecting them to +5V via 10k Ω resistors (see Fig. 4).
4. The ECL carry output is compatible with ECL II throughout the temperature range but can be made compatible with ECL III using the simple interface shown in Fig. 3.

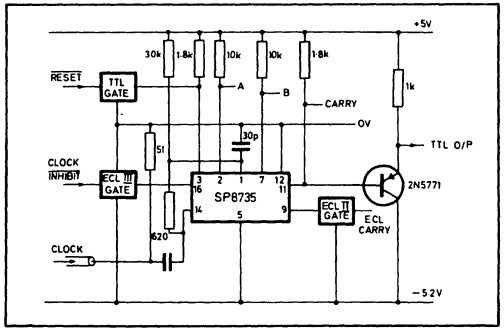



*Fig.5 Typical operating diagram*

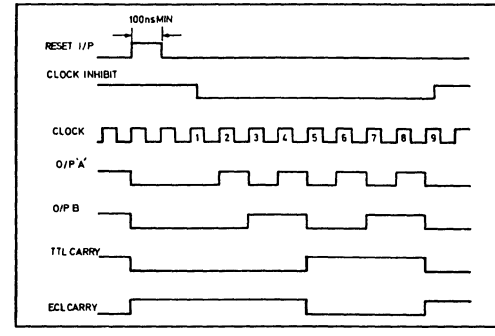



*Fig.6 Output waveforms*

## OPERATING NOTES

**The device is** intended to be used with TTL and ECL in a counting system — the ECL and the decade counter being connected between voltage rails of 0V and −5.2V and the TTL between voltage rails of 0V and + 5V. Provided that this is done ECL and TTL compatibility is achieved. (See Figs. 4 and 5)

The clock is normally capacitively coupled to the signal source: a 1000 pF UHF capacitor should be adequate. For low frequency operation, the 1000 pF capacitor should be connected in parallel with a higher value capacitor. The bias decoupling (pin 1) should be connected to earth via a capacitor — preferably a chip type, but in any case a low inductance type suitable for UHF applications. The devices normally have an input amplitude operating range far greater than the specified 400 to 800 mV p – p. However, if the decoupling capacitor is not of a UHF type, or it is connected to an earth point that has a significant impedance between the capacitor and the $V_{CC}$ connection, then the input dynamic range will suffer and the maximum signal for correct operation will be reduced.

Under certain conditions, the absence of an input signal may cause the device to self-oscillate. This can be prevented (while still maintaining the specified input sensitivity) by connecting a 30Ω resistor between the clock input and the positive supply and a 620Ω resistor between clock and pin 1. If the transition of either the clock input or the clock inhibit input is slow the device may start to self-oscillate during the transition. For this reason the input slew rates should be greater than 100V/μs. It should also be noted that a positive-going transition on either the clock input or the clock inhibit will clock the device, provided that the other input is in the low state.

The binary outputs give TTL-compatible outputs (fan out = 1) when a 10kΩ resistor is connected from the output to the + 5V rail. In this configuration the outputs will be very slow compared with the clocking rate of the counter and so the state on the TTL outputs can only be determined when the clock has stopped or is inhibited.

The fan out capability of the TTL carry output can be increased by buffering it with a PNP emitter follower. The interface is shown in Fig. 5.

A typical application is shown in Fig. 7.

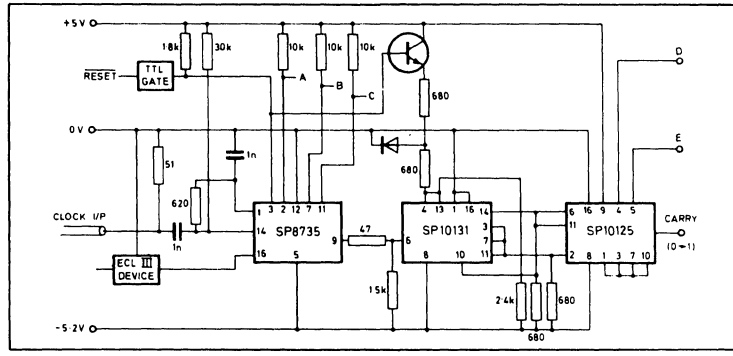



*Fig.7 600MHz ÷ 32 with reset and inhibit*

# SP 8740 A & B

## AC COUPLED UHF PROGRAMMABLE DIVIDER 300 MHz ÷ 5/6

The SP8740 A & B are high speed programmable ÷5/6 counters operating at an input frequency of up to 300 MHz over the temperature ranges −55°C to +125°C, 0°C to +70°C.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 5 when either input is in the high state, and by 6 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

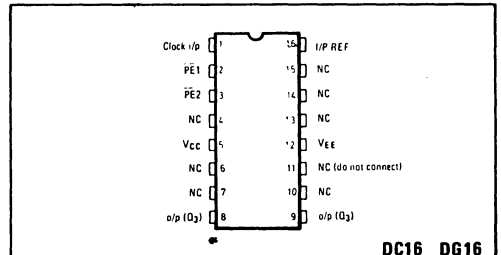
When using the device as a divide-by-five prescaler the inverse output (o/p) should be connected to a PE input.

| Clock Pulse | $Q_1$ | $Q_2$ | $Q_3$ | |
|---|---|---|---|---|
| 1 | L | H | H | |
| 2 | L | L | H | |
| 3 | L | L | L | |
| 4 | H | L | L | |
| 5 | H | H | L | |
| 6 | H | H | H | ←Extra state |

*Table 1 Count sequence*

| $\overline{PE_1}$ | $\overline{PE_2}$ | Div Ratio |
|---|---|---|
| L | L | 6 |
| H | L | 5 |
| L | H | 5 |
| H | H | 5 |

*Table 2 Truth table for control inputs*




NOTE: UNUSED PINS (EXCEPT 8, 9 and 11) MAY BE CONNECTED TO $V_{EE}$; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS.

*Fig. 1 Pin connections*

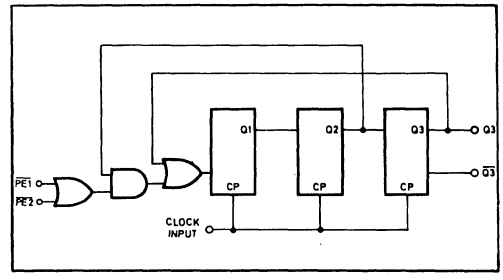



*Fig. 2 Logic diagram SP8740*

### FEATURES

- Full Temperature Range Operation
  'A' Grade −55°C to +125°C
  'B' Grade 0°C to +70°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K – Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $V_{CC} - V_{EE}$ | 0V to +8V |
| Input voltage, PE inputs | 0V to $V_{CC}$ |
| Input voltage, CP input | 2V peak-to-peak |
| Output current | 20mA |
| Operating junction temperature | +150°C |
| Storage temperature | −55°C to +150°C |

## ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs – ECL 10K compatible
Outputs – ECL II compatible

**Test conditions (unless otherwise stated)**

$T_{amb}$: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
Supply voltages: $V_{CC}$ = +5.2V ±0.25V
$V_{EE}$ = 0V
Clock input voltage: 400mV to 800mV (p-p)

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Max i/p frequency | 300 | | | MHz | $V_{cc}$ = +5.2V |
| Min i/p frequency | | | 40 | | Sinewave Input |
| Min. slew rate for square wave input | | | 100 | V/μs | |
| Propagation delay (clock i/p to device o/p) | | 4 | | ns | |
| $\overline{PE}$ input reference level | | +3.9 | | V | $V_{cc}$ = +5.2V, 25°C |
| Power supply drain current | | 45 | 60 | mA | $V_{cc}$ = +5.2V, 25°C |
| $\overline{PE}$ input pulldown Resistors | | 4.3 | | KΩ | |
| Clock i/p impedance (i/p to i/p ref low frequency) | | 400 | | Ω | |

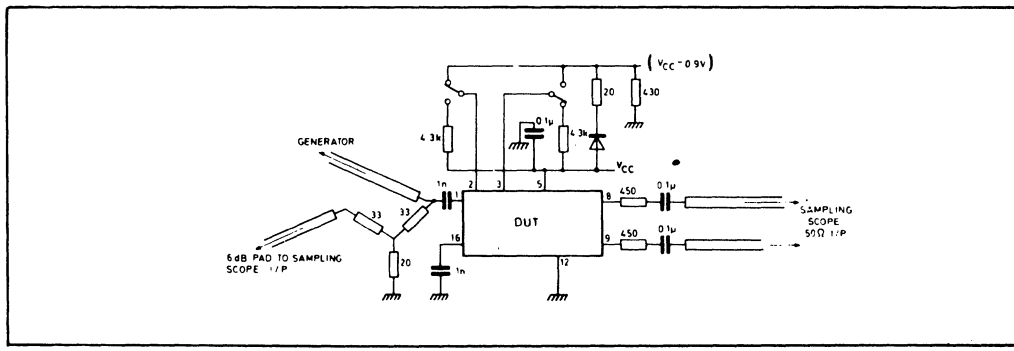



*Fig. 3 Test circuit*

## APPLICATION NOTES

When operating the SP8740 in a synthesiser loop at 300MHz, the delay time through the programmable divider controlling the SP8740 is approximately 13ns. As we believe that this delay would be a severe problem with TTL, we strongly recommend the use of ECL.

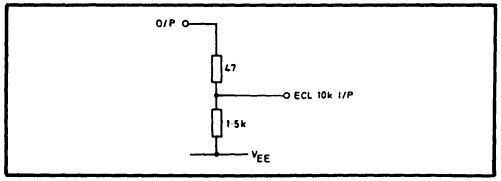



*Fig. 4*

The simple passive interface from the output of the SP8740 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins, and the output of the SP8740 into TTL, is shown in Fig. 5.

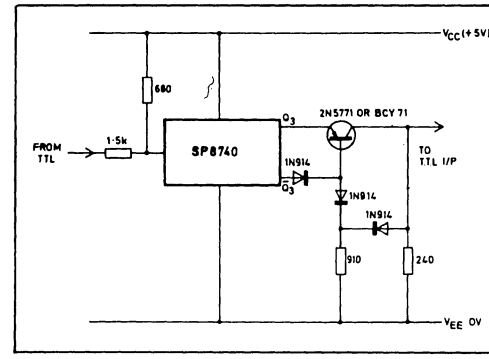



*Fig. 5*

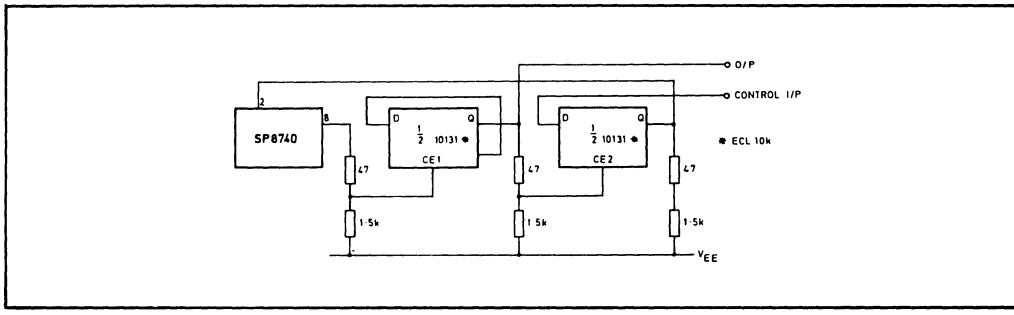



*Fig. 6 Divide by 10/12. Control loop delay time approximately 33 ns*

# SP 8741 A & B

## AC COUPLED UHF PROGRAMMABLE DIVIDERS 300 MHz ÷ 6/7

The SP8741 A, B & M are high speed programmable ÷6/7 counters operating at an input frequency of up to 300 MHz over the temperature ranges −55°C to +125°C, 0°C to 70°C.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 6 when either input is in the high state, and by 7 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

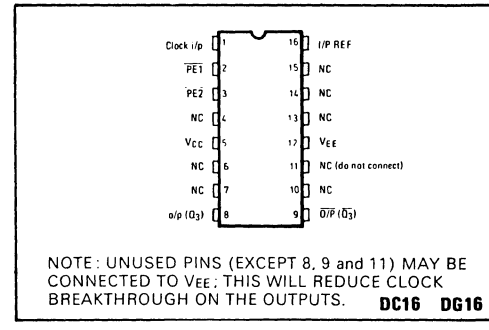
When using the device as a divide-by-six prescaler the inverse output (o/p) should be connected to a PE input.

| Clock Pulse | $Q_1$ | $Q_2$ | $Q_3$ | |
|---|---|---|---|---|
| 1 | L | H | H | |
| 2 | L | L | H | |
| 3 | H | L | H | |
| 4 | L | H | L | |
| 5 | L | L | L | |
| 6 | H | L | L | |
| 7 | H | H | H | ← Extra state |

*Table 1 Count sequence*

| $\overline{PE_1}$ | $\overline{PE_2}$ | Div Ratio |
|---|---|---|
| L | L | 7 |
| H | L | 6 |
| L | H | 6 |
| H | H | 6 |

*Table 2 Truth table for control inputs*




NOTE: UNUSED PINS (EXCEPT 8, 9 and 11) MAY BE CONNECTED TO $V_{EE}$; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS. **DC16 DG16**

*Fig. 1 Pin connections*

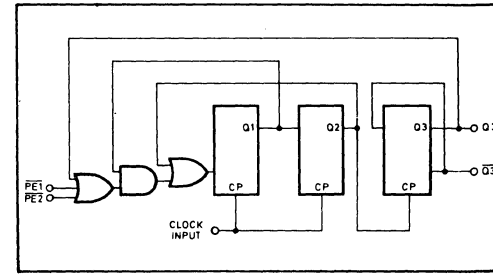



*Fig. 2 Logic diagram*

### FEATURES

- Full Temperature Range Operation
  'A' Grade −55°C to +125°C
  'B' Grade 0°C to +70°C
- Self Biasing CP Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K – Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$ | 0V to +8V |
| Input voltage, PE inputs | 0V to $V_{CC}$ |
| Input voltage, CP input | 2V peak-to-peak |
| Output current | 20mA |
| Operating junction temperature | +150°C |
| Storage temperature | −55°C to +150°C |

## ELECTRICAL CHARACTERISTICS

$\overline{PE}$ inputs – ECL 10K compatible
Outputs – ECL II compatible

**Test conditions (unless otherwise stated)**

$T_{amb}$: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
Supply voltages: $V_{CC}$ = +5.2V ±0.25V
$V_{EE}$ = 0V
Clock input voltage: 400mV to 800mV (p-p)

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Max i/p frequency | 300 | | | MHz | $V_{cc}$ = +5.2V |
| Min i/p frequency | | | 40 | | Sinewave Input |
| Min. slew rate for square wave input | | | 100 | V/μs | |
| Propagation delay | | | | | |
| (clock i/p to device o/p) | | 4 | | ns | |
| $\overline{PE}$ input reference level | | +3.9 | | V | $V_{cc}$ = +5.2V, 25°C |
| Power supply drain current | | 45 | 60 | mA | $V_{cc}$ = +5.2V, 25°C |
| $\overline{PE}$ input pulldown | | | | | |
| Resistors | | 4.3 | | KΩ | |
| Clock i/p impedance | | | | | |
| (i/p to i/p ref low frequency) | | 400 | | Ω | |

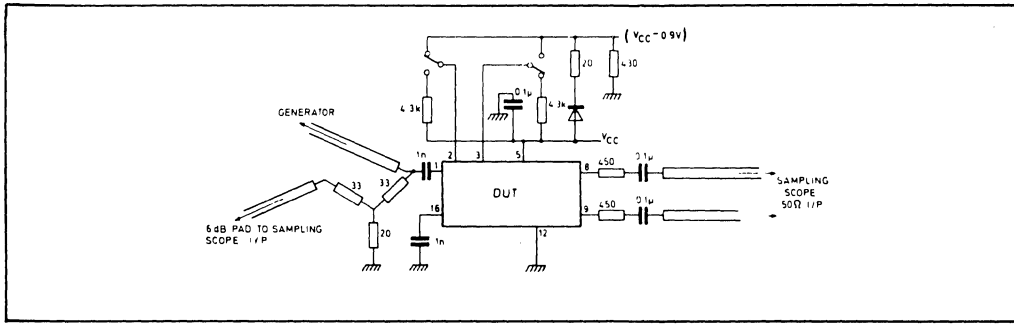



*Fig. 3 Test circuit*

## APPLICATION NOTES

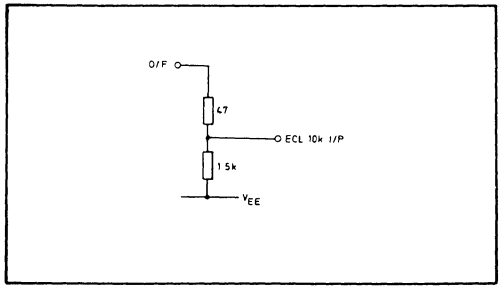



*Fig. 4*

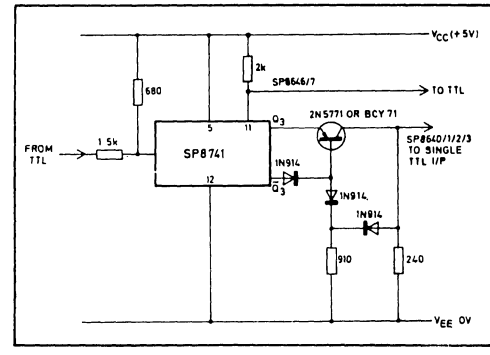



*Fig. 5*

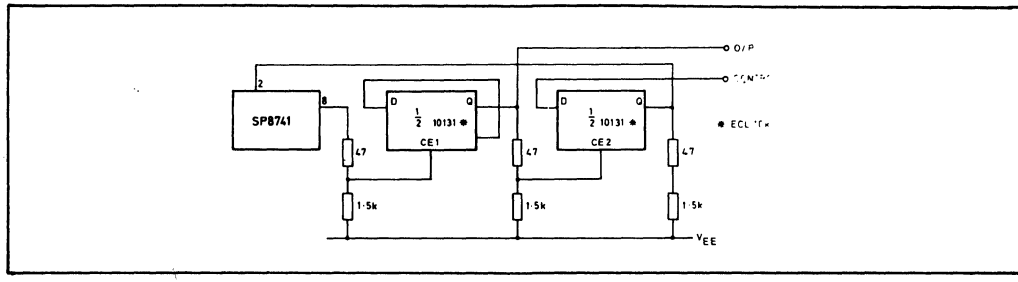



*Fig. 6 Divide-by-12/14. Control loop delay time approximately 40ns.*

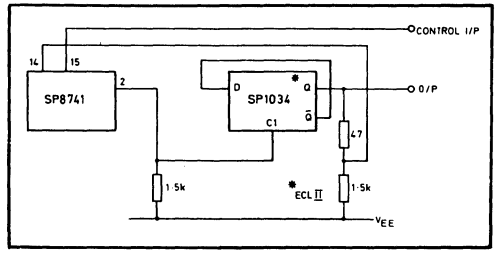



*Fig. 7 Divide-by-12/13. Control loop delay time approximately 30ns using SP1034.*

When operating the SP8741 in a synthesiser loop at 300MHz the delay time through the programmable divider controlling the SP8741 is approximately 16ns. As we believe that this delay would be a severe problem with TTL, we strongly recommend the use of ECL.

The simple passive interface from the output of the SP8741 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins, and the output of the SP8741 into TTL, is shown in Fig. 5.

# SP 8743 B & M

## AC COUPLED UHF PROGRAMMABLE DIVIDER 500 MHz ÷8/9

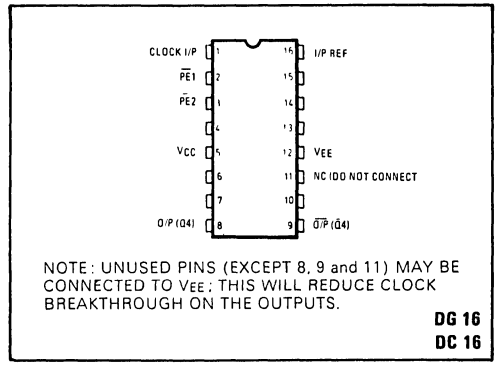
The SP8743M and B are high speed, programmable ÷ 8/9 counters operating at an input frequency of up to 500MHz over the temperature ranges −40°C to +85°C and 0°C to 70°C respectively.

The clock input is biased internally and is coupled to the signal source by a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to ground.

The division ratio is controlled by two $\overline{PE}$ inputs. The counter will divide by 8 when either input is in the high state and by 9 when both inputs are in the low state. These inputs are compatible with standard ECL 10K inputs and have the same temperature characteristics. Both inputs have nominal 4.3kΩ internal pulldown resistors.

The true and inverse outputs are compatible with standard ECL II outputs. They may be used to drive ECL 10K circuits by the inclusion of two resistors as shown in Fig. 4.

When using the device as a divide-by-eight prescaler the inverse output (o/p) should be connected to a $\overline{PE}$ input.




NOTE: UNUSED PINS (EXCEPT 8, 9 and 11) MAY BE CONNECTED TO $V_{EE}$; THIS WILL REDUCE CLOCK BREAKTHROUGH ON THE OUTPUTS.

**DG 16**
**DC 16**

*Fig. 1 Pin connections*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage, $\lvert V_{CC} - V_{EE} \rvert$ | 0V to +8V |
| Input voltage PE inputs | 0V to $V_{CC}$ |
| Input voltage CP input | 2V p-p |
| Output current | 20mA |
| Operating junction temperature | +150°C |
| Storage temperature | −55°C to +150°C |

### FEATURES

- Operating Temperature Range:
  0°C to 70°C ('B' grade)
  −40°C to +85°C ('M' grade)
- Self Biasing Clock Input
- Wide Input Dynamic Range
- Control Inputs ECL 10K Compatible
- Low Propagation Delay
- True and Inverse Outputs Available

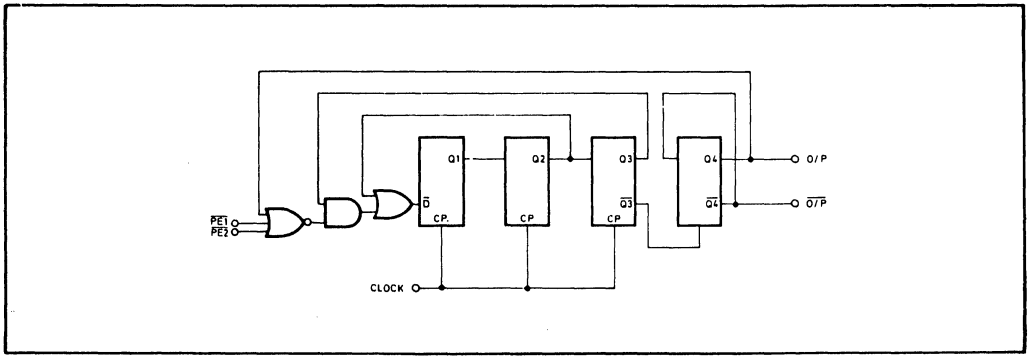



*Fig. 2 SP8743 logic diagram*

| Count Sequence | | | |
|---|---|---|---|
| $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ |
| L | H | H | H |
| L | L | H | H |
| H | L | L | L |
| H | H | L | L |
| L | H | H | L |
| L | L | H | L |
| L | L | L | H ← Extra state |
| H | L | L | H |
| H | H | L | H |

| Division Ratio | | | | |
|---|---|---|---|---|
| | 9 | 8 | 8 | 8 |
| $\overline{PE1}$ | L | L | H | H |
| $\overline{PE2}$ | L | H | L | H |

## ELECTRICAL CHARACTERISTICS

**$\overline{PE}$ inputs – ECL 10K compatible**
**Outputs – ECL II compatible**

**Test Conditions (unless otherwise stated):**
$T_{AMB}$ 0°C to +70°C ('B' grade) –40°C to + 85°C ('M' grade)
Supply Voltage $V_{CC}$ = +5.2V ± 0.25V $V_{EE}$ = 0V
Clock Input Voltage 400mV to 800mV p-p

| Characteristics | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Max. i/p frequency | 500 | | | MHz | $V_{CC}$ = +5.2V |
| Min. i/p frequency | | | 40 | | Sinewave Input |
| Min. Slew rate for square wave input | | | 100 | V/μs | |
| Propagation delay (clock i/p to device o/p) | | 4 | | ns | |
| $\overline{PE}$ input reference level | | +3.9 | | V | $V_{CC}$ = +5.2V, 25°C |
| Power Supply drain current | | 45 | 60 | mA | $V_{CC}$ = +5.2V, 25°C |
| $\overline{PE}$ input pulldown resistors | | 4.3 | | kΩ | |
| Clock i/p impedance (i/p to i/p ref. low freq.) | | 400 | | Ω | |

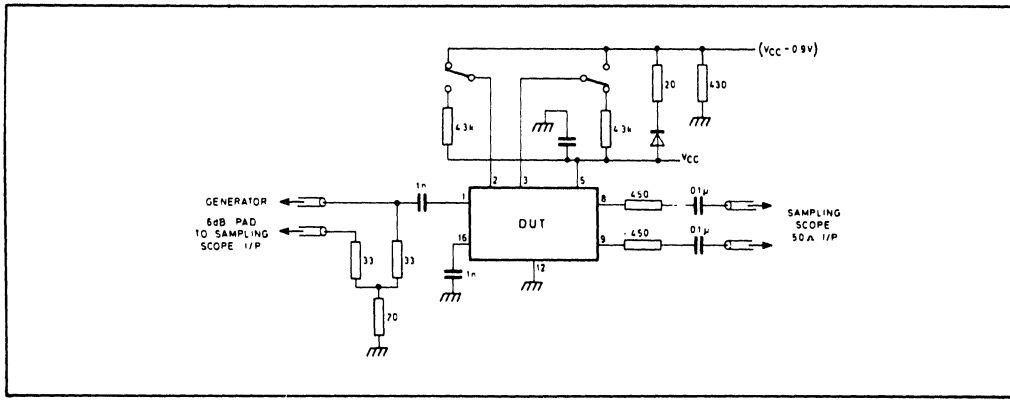



*Fig. 3 Test circuit*

## APPLICATIONS INFORMATION

### Interfaces

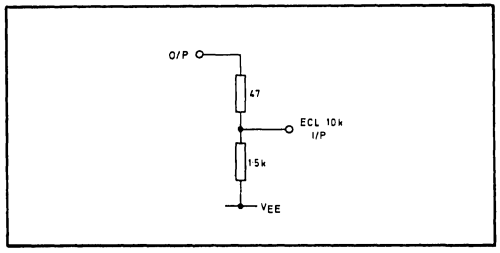



*Fig. 4*

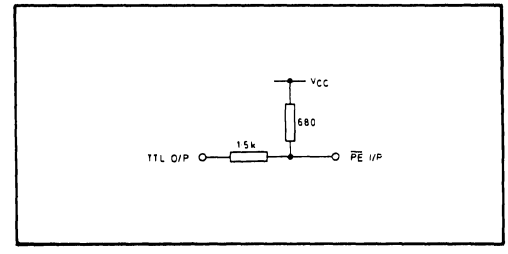



*Fig. 5*

When operating the SP8743 in a synthesiser loop at 500MHz, the delay time through the programmable divider controlling the SP8743 is approximately 12ns As we believe that this delay would be a severe problem with TTL, we strongly recommend the use of ECL.

The simple passive interface from the output of the SP8743 into ECL 10K logic is defined in Fig. 4.

If TTL is required, the input interface to the $\overline{PE}$ pins, and the output of the SP8743 into TTL, is shown in Fig. 5.

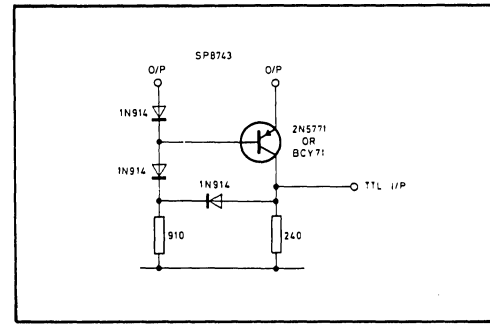



*Fig. 6 SP8743 O/P to TTL I/P. Total delay from SP8743 clock I/P to Schottky gate O/P = 15ns typical.*

### Sub-Systems

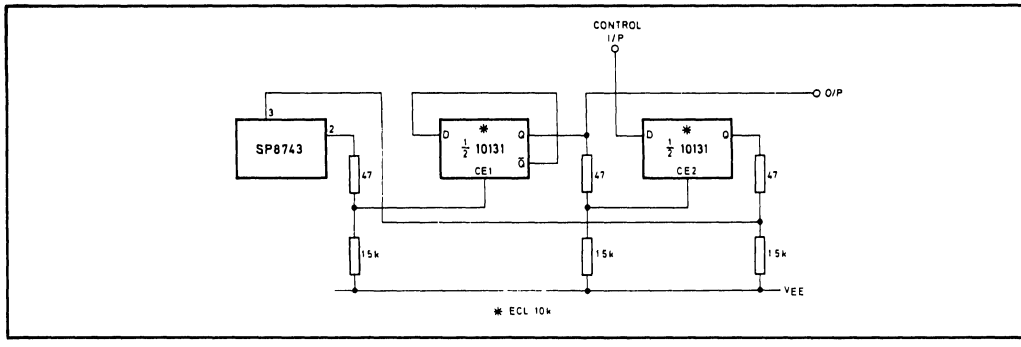



*Fig.7 A ÷ 32/33 application. Control loop delay time approx. 56ns.*

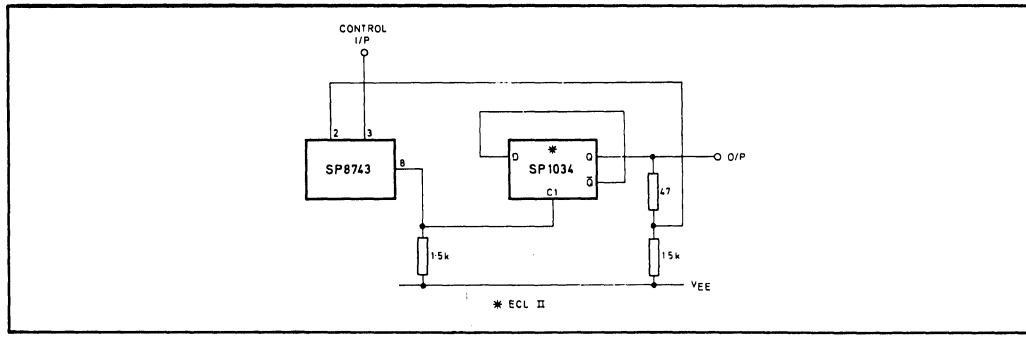



*Fig.8 A÷16/17 application. Control loop delay time approx. 24ns using SP1034*

PLESSEY
SEMICONDUCTORS

# SP8000 SERIES
## HIGH SPEED DIVIDERS

# SP8755A & B
## 1200 MHz ÷ 64 PRESCALER

### FEATURES

- DC to 1200MHz
- -55°C to +125°C temperature range
- TTL compatible output

### QUICK REFERENCE DATA

- Supply voltage 5V ±0.25V
- Power consumption 270mW typ. (no load)

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $V_{CC} - V_{EE}$ | 0V to +10V |
| Input voltage, clock inputs | 2.5V p-p |
| Output current | +30 mA to -30 mA |
| Operating junction temperature | +150°C |
| Storage Temperature | -55°C to +150°C |

### OPERATING NOTES

The input is terminated by a nominal 400Ω and should be AC coupled to the signal source. Input power to the device is terminated to ground by the decoupling capacitor on the reference pin. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1GHz.

If the device is required to operate with a sinewave input below 100MHz, then the required hysteresis may be applied externally as shown in Fig. 5. Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 64 output is designed to interface with TTL which has a common $V_{EE}$ (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power/Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when the clock input changes from a low to a high level.

The device may be operated down to very low frequencies if a square wave input is applied with an edge speed of greater than 200V/μs.

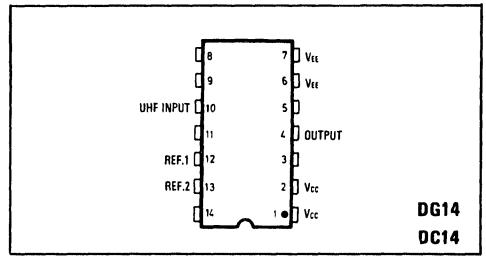



*Fig. 1 Pin connections*

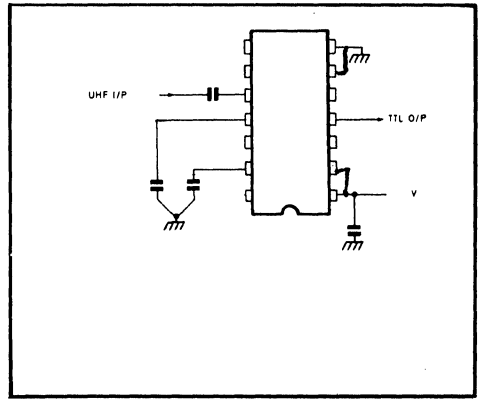



*Fig. 2 Typical application*

## ELECTRICAL CHARACTERISTICS

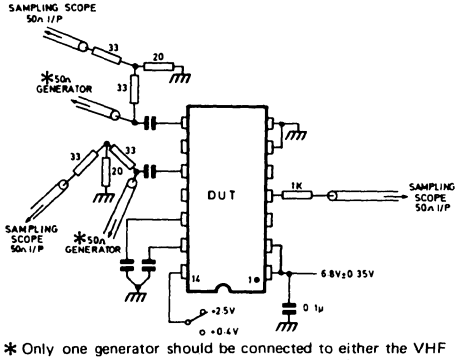
Test conditions (unless otherwise stated):

Supply voltage $V_{CC}$ : 4.75V to 5.25V

Input signal amplitude : 400mV to 1.0V (f < 1GHz)
600mV to 1.2V (1GHz ≤ f < 1.2GHz)

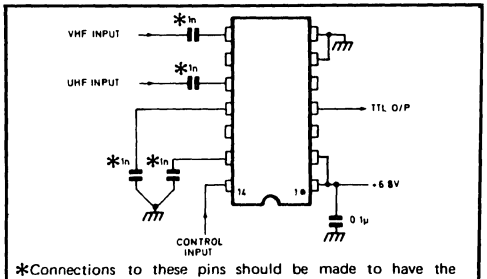
Ambient temperature : -30°C to +70°C (SP8755B)
-55°C to +125°C (SP8755A)

| Characteristics | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Supply current | | 54 | 75 | mA | |
| Max. input frequency | 1200 | | | MHz | 600mV pk-pk sine wave input |
| Min. input frequency | | | 100 | MHz | |
| Min. slew rate (with square wave input) | | | 200 | V/μS | |
| Output voltage level (high) | 2.5 | | 4.5 | V | $V_{CC}$ = 5.0V |
| Output voltage level (low) | | | 0.4 | V | 5mA current into pin 4 |




* Only one generator should be connected to either the VHF or UHF inputs. The input not in use may be left open circuit. All capacitors are 1nF unless otherwise stated.

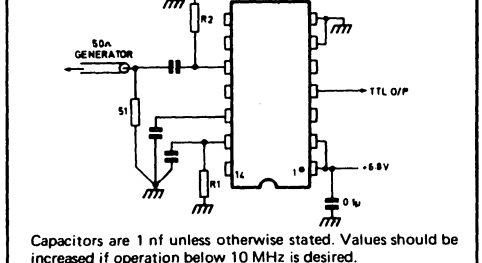
*Fig. 3 AC Test Circuit*




*Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1GHz.

For single input operation leave pins 8 and 14 open circuit.

*Fig. 4 Application Circuit*




Capacitors are 1 nf unless otherwise stated. Values should be increased if operation below 10 MHz is desired.

For 50 mV hysteresis R1 = 36kΩ R2 = ∞

For 100 mV hysteresis R1 = 18kΩ R2 = 18kΩ

*Fig. 5 Wideband Operation*

Plessey Semiconductors

# SP 8000 SERIES

## HIGH SPEED DIVIDERS

# SP8760 B & M

## GENERAL PURPOSE SYNTHESISER CIRCUIT

The SP8760 is a multi-function device for use in phase-lock-loop systems. It contains a crystal oscillator maintaining circuit, followed by a divide-by-four stage; a digital phase/frequency comparator; and a two-modulus divider programmable to divide by 15 or 16.

It may be used with a prescaler to phase-lock single frequency transmitters or receivers in the HF, VHF or UHF bands.

The addition of an MOS/CMOS programmable plus fixed divider will generate a complete frequency synthesiser. The maximum frequency requirement of the control device is only 1MHz, enabling complex functions to be performed using LSI technologies. With suitable prescalers, the controlled frequency source may extend into the IGHz region.

The SP8760 is available in two temperature grades: 0 °C to +70 °C ('B' grade) and –40 °C to +85 °C ('M' grade).

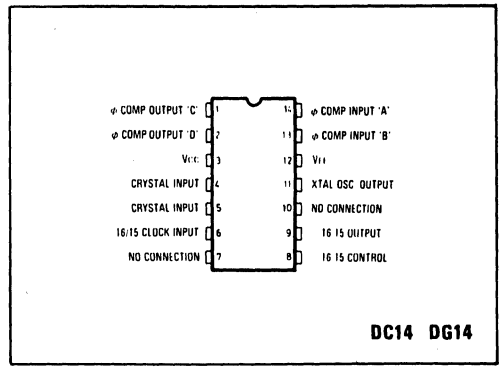



*Fig. 1 Pin connections*

### FEATURES

- TTL/MOS Compatible Inputs and Outputs
- Low Power Consumption (<250mW Typ)
- Minimum External Components
- Voltage Pump Outputs on Phase/Frequency Comparator
- Zero Phase Difference Pulses <30nSec
- Crystal Oscillator Stability ±5 ppm at 4MHz, 0°C to +70°C
- Crystal Oscillator Interfaces with SL680 for Very High Stability Applications

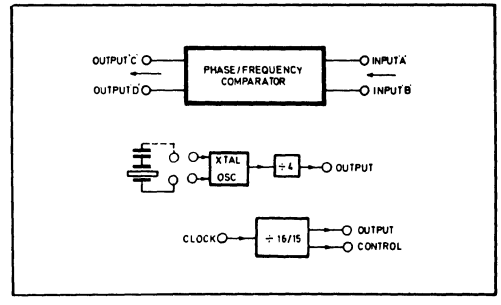



*Fig. 2 SP8760 block diagram*

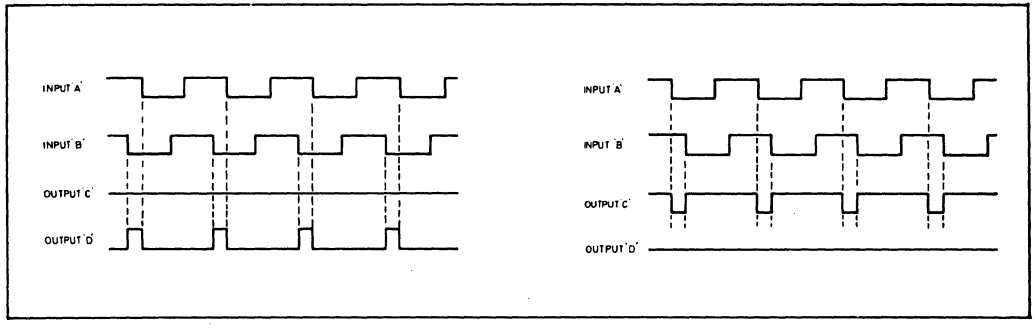



*Fig. 3 Phase/frequency comparator waveforms*

## ELECTRICAL CHARACTERISTICS

Supply voltage 5V ± 0.5V
Supply current 45mA typ

**Test conditions (unless otherwise stated):**
$V_{CC}$ = 4.5V to 5.5V
$V_{EE}$ = 0V
$T_{AMB}$ 0°C to +70°C ('B' grade)
−40°C to +85°C ('M' grade)

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Power Supply Current | | 45 | 65 | mA | |
| **Crystal Osc. ÷4** | | | | | |
| Crystal series capacitor | | 28 | | pF | at 4MHz |
| Crystal series capacitor | | 20 | | pF | at 10 MHz |
| Temperature Stability | | | 0.2 | ppm/°C | at 4MHz, excluding crystal temperature coefficient. |
| Supply voltage stability | | −1 | | ppm/V | at 4 MHz |
| External oscillator drive required | | ±1 | | mA | See Fig. 8. |
| Divide-by-four output, external current sink capability | 5 | | | mA | at 0.5V |
| **Phase/Frequency Comparator** | | | | | |
| Input current | | 250 | 350 | uA | at Vin = 2.4V |
| Output 'C' current sink capability | 6 | | | mA | at 0.5V |
| Output 'D' current source capability | 6 | | | | at ($V_{CC}$ - 1.15V) |
| Zero phase pulse width | | | 30 | ns | |
| Input to Output delay | | 40 | | ns | |
| **Divide by 16/15** | | | | | |
| Control input current | | 250 | 350 | µA | at Vin = 2.4V |
| Clock input current | | −1.0 | −1.6 | mA | at Vin = 0.4V |
| Output external current sink capability | 5 | | | mA | at 0.5V |
| Maximum clock frequency | 16 | 28 | | MHz | Divide by 16 |
| | 12 | 18 | | MHz | Divide by 15 |
| Clock to output delay | | 35 | | ns | Output 1 - 0 |

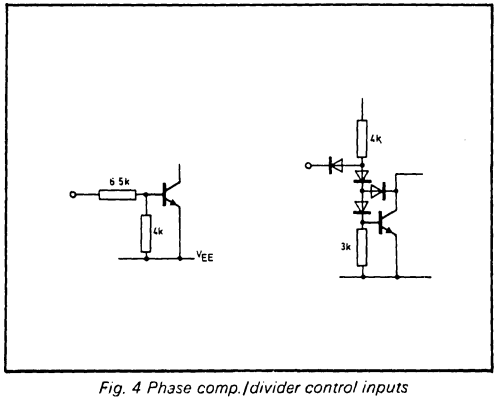



*Fig. 4 Phase comp./divider control inputs*

## ABSOLUTE MAXIMUM RATINGS

Power supply $V_{CC}$ − $V_{EE}$ 0V to +10V
Output current 20mA
Operating junction temperature +150°C
Storage temperature −55°C to +150°C

## OPERATING NOTES

The crystal oscillator is an emitter coupled circuit with an internal roll off capacitor to prevent oscillation at overtone frequencies. The crystal is connected in series with a capacitor between pins 4 and 5. It may be used with series resonant crystals at frequencies up to 10MHz. The stability of the crystal oscillator is better than ±5 p.p.m. at 4MHz over the temp range 0°C to 70°C (excluding the temperature coefficient of the crystal). If a higher stability is required the SL680 crystal oscillator maintaining circuit should be used. This may be interfaced to the SP8760 as shown in Fig. 8. The divide by four has a free collector output with an internal 2.5 KΩ resistor to Vcc.

The phase frequency comparator is an infinite pull-in range circuit which gives zero phase shift lock. The circuit triggers on the 1 - 0 edge of each input and gives an output which is proportional to the phase difference between the two edges (see Fig. 3). When the input 'A' edge precedes the input 'B' edge output 'C' will pulse to a low level while output 'D' will remain at a permanent low level. When the input 'B' edge precedes the input 'A' edge, output 'D' will pulse to a high level while output 'C' will remain at a permanent high level. The two outputs may be used to drive a charge pump and filler as shown in Figs. 5 and 6. The output of the filter may be used to drive directly the varactor line of a voltage controlled oscillator. For optimum 'noise' performance the output pulses from the phase detector must tend to zero when 'in lock'. The leakage on the filter output must therefore be kept to a minimum. If the varactor line draws a significant current it should be buffered using an emitter follower arrangement as shown in Fig. 7.

The phase/frequency comparator inputs are of the current source type as shown in Fig. 4. These may be driven by standard TTL or CMOS. Output 'C' is a free collector with an internal 10KΩ resistor to Vcc. Output 'D' is an emitter follower with an internal 10KΩ resistor to VEE.

The two-modulus prescaler may be controlled to divide by 16 or 15 using the control input. With the control input high the circuit will divide by 16. When a counter is used to control the two-modulus it should be clocked on the 1 - 0 edge of the 16/15 output. If the two-modulus is used only as a fixed divide-by-16 the control input - should be tied to Vcc. The prescaler clock input is a current sink input with a standard TTL fan in of one. It may be driven by standard or low power Schottky TTL. The control input is identical to the phase/frequency comparator inputs as shown in Fig. 4. The two modulus output is a free collector with an internal 1.5KΩ resistor to Vcc.

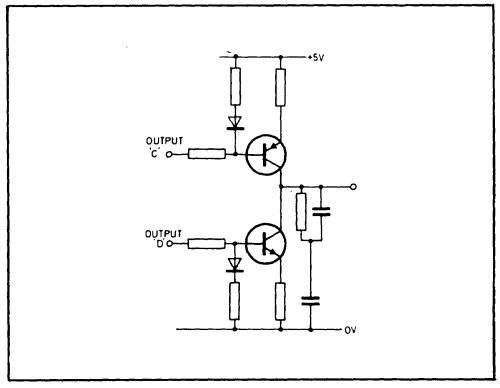



*Fig. 5 Low voltage charge pump and filter*

*Divider clock input*

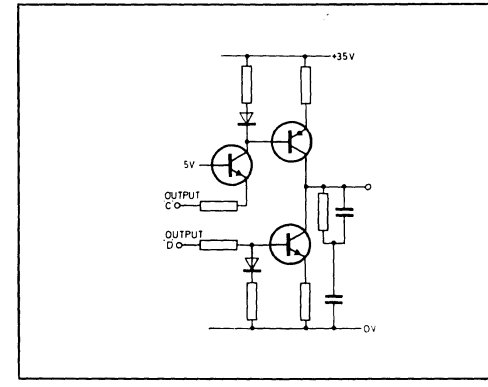



*Fig. 6 High voltage charge pump and filter*

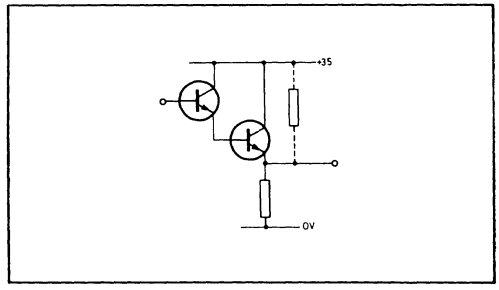



*Fig. 7 Emitter follower buffer*

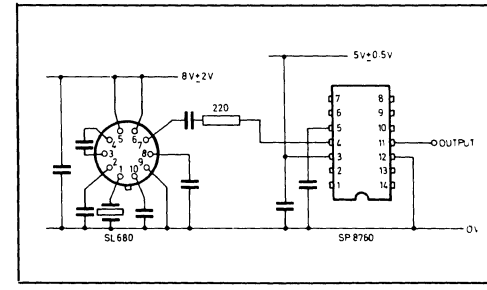



*Fig. 8 SL680 to SP8760 interface*

Plessey Semiconductors

# SP8000 SERIES
## HIGH SPEED DIVIDERS

# SP8775
# 1.2 GHz
## UHF ÷ 256 PRESCALERS

The SP8775 are ECL divide by 256 prescalers which will operate at frequencies up to 1.2 GHz.
The device has a typical power dissipation of 500mW at the nominal supply voltage of +5V.

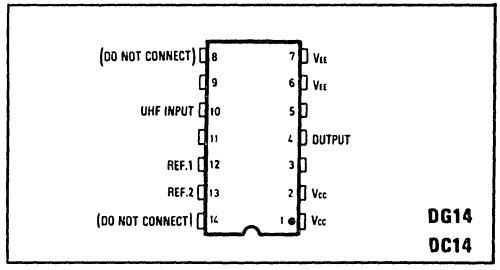



*Fig. 1 Pin Connections*

### FEATURES

- Self-Biasing Clock Input
- Variable Input Hysteries Capability for Wide Band Operation
- Push Pull TTL O/P

### OPERATING NOTES

The input is terminated by a nominal 400Ω and should be AC coupled to the signal source. Input power to the device is terminated to ground by the two decoupling capacitors on the reference pins. Input coupling and reference decoupling capacitors should be of a type suitable for use at a frequency of 1 GHz.

If the device is required to operate with a sinewave input below 100 MHz, then the required hysteresis may be applied externally as shown in Fig. 4.

Large values of hysteresis should be avoided as this will degrade the input sensitivity of the device at the maximum frequency. The divide by 256 output is designed to interface with TTL which has a common $V_{EE}$ (ground). The specified fan-out of 3 standard TTL inputs may be increased to 6 standard or 5 high power/ Schottky inputs at a logic zero level of 0.5V. At low frequency the output will change when one of the clock inputs changes from a low to a high level.

The devices may be operated down to very low frequencies if a square wave input is applied with an edge speed of greater than 200V/μs.

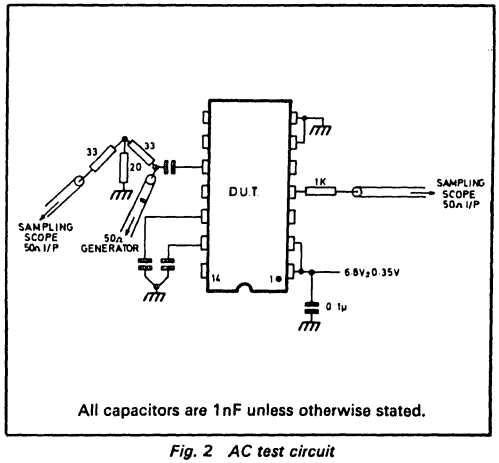



*Fig. 2 AC test circuit*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $\|V_{CC}-V_{EE}\|$ | 0V to +10V |
| Input voltage, clock input | 2.5V p-p |
| Output current | +30mA to −30mA |
| Operating junction temperature | +150°C |
| Storage temperature | −55°C to +150°C |

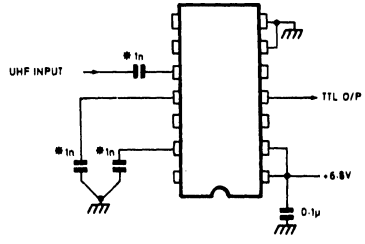
## ELECTRICAL CHARACTERISTICS

Supply voltage: 5.0V ± 0.25V
Supply current: 72mA typ., 95mA max.
Temperature range: 0°C to +70°C
Clock input: AC coupled, self biasing via 400 Ω

**Test conditions (unless otherwise stated):**

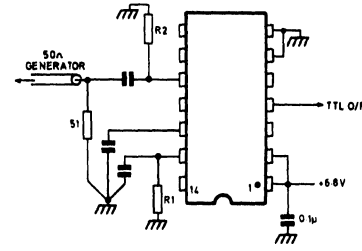
Supply voltage: $V_{EE}$ = 0V,
$V_{CC}$ = +5.0V ± 0.25V
Clock input voltage: 400mV to 1.2V p-p
$T_{amb}$ = 25°C

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Max. Input frequency SP8775 | 1.2 | | | GHz | 600mV p-p input |
| Min input frequency | | | 200 | MHz | 400mV p-p sinewave input |
| | | | 100 | MHz | 600mV p-p sinewave input |
| | | | 75 | MHz | 800mV p-p sinewave input |
| Min. slew rate for square wave input | | | 200 | V/μs | |
| **Output** | | | | | |
| High level | 2.5 | 3.5 | 4.5 | V | |
| Low level | | | 0.4 | V | 5mA current sink |
| Supply current | | 68 | 90 | mA | Vcc = 5.0V |




* Connections to these pins should be made to have the minimum series inductance. Capacitors should be of a type suitable for use at 1 GHz.

*Fig. 3 Application circuit*




Capacitors are 1 nF unless otherwise stated. Values should be increased if operation below 10 MHz is desired.
For 50mV hysteresis R1 = 36kΩR2 = ∞
For 100mV hysteresis R1 = 18kΩR2 = 18kΩ

*Fig. 4 Wideband operation*

# SP8785B&M 1.0GHz ÷ 20/22
# SP8786B&M 1.3GHz ÷ 20/22
## UHF PROGRAMMABLE DIVIDERS

The SP8785 B & M and SP8786 B & M are high speed programmable ÷20/22 counters which operate at input frequencies up to 1.0GHz and 1.3GHz respectively over the temperature ranges 0°C to +70°C (B grade) and —40°C to +85°C (M grade).

The clock input is biased internally and is coupled to the signal source by a capacitor. The input RF path is completed by two input reference decoupling capacitors which are connected to earth.

The division ratio is controlled by two PE inputs. The counter will divide by 20 when either input is in the high state and by 22 when both inputs are in the low state. These inputs are ECL III/10K compatible and have internal 4.3KΩ pulldown, unused inputs may therefore be left open. When using the device as a ÷20 prescaler the inverse output should be connected to a PE input.

In keeping with the device performance the complementary outputs are ECL 10K compatible.

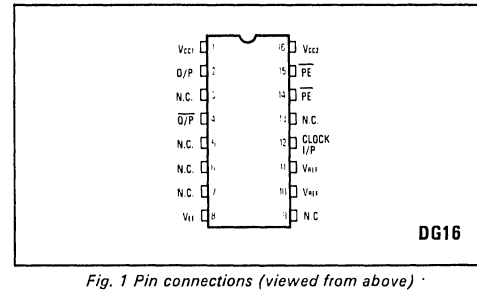



*Fig. 1 Pin connections (viewed from above)*

### FEATURES

- DC to 1.3GHz operation
- 0°C to +70°C operation (B Grade)
- —40 to +85°C operation (M grade)
- Complementary outputs and control inputs are ECL 10K/ECL III compatible.
- AC coupled clock input with wide dynamic range.

### QUICK REFERENCE DATA

- Supply voltage $V_{CC} - V_{EE} = 5.2V \pm .25v$
- Power Consumption 440 mW typ (no load)
- ECL compatible
- Maximum input frequency 1GHz (SP8785), 1.3GHz (SP8786)
- Control loop delay time 12 ns typ with 1.3GHz input.

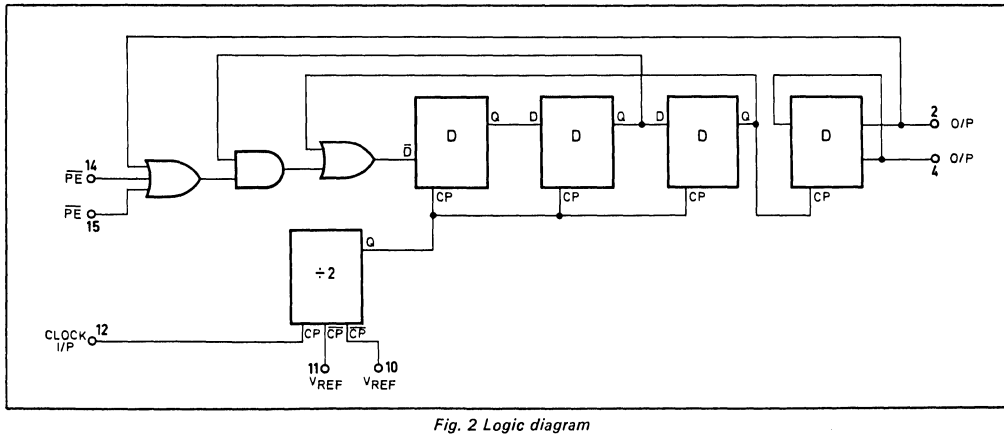



*Fig. 2 Logic diagram*

| CLOCK PULSE | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ |
|---|---|---|---|---|
| 2 | L | H | H | H |
| 4 | L | L | H | H |
| 6 | L | L | L | H |
| 8 | H | L | L | H |
| 10 | H | H | L | H |
| 12 | L | H | H | L |
| 14 | L | L | H | L |
| 16 | L | L | L | L |
| 18 | H | L | L | L |
| 20 | H | H | L | L |
| 22 | H | H | H | H |

| — PE | — PE | DIV RATIO |
|---|---|---|
| L | L | 22 |
| H | L | 20 |
| L | H | 20 |
| H | H | 20 |

The maximum possible loop delay for control is obtained if the L → H transition from $Q_4$ or the H → L transition from $Q_4$ is used to clock the stage controlling the ÷20/22. The loop delay is 20 clock periods minus the internal delays of the ÷20/22 circuit.

*Table 1 Count sequence and control input truth table*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ 0°C to +70°C (B Grade)
−40°C to +85°C (M Grade)
Supply voltage $V_{CC}$ = OV
$V_{EE}$ = −5.2V*

**Static characteristics**

| Characteristic | Value Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| PE input voltage $V_{INH}$ | −.96 | | $V_{CC}$ | V | $T_{amb}$=25°C |
| $V_{INL}$ | $V_{EE}$ | | −1.62 | V | see note 2 |
| PE input pulldown resistor | | 4.3 | | KΩ | |
| Output Voltage levels | | | | | |
| $V_{OH}$ | −.93 | | −.78 | V | $T_{amb}$=25°C |
| $V_{OL}$ | −1.85 | | −1.62 | V | 430Ω from o/p to $V_{EE}$ see note 2 |
| Power supply current | | 85 | 115 | mA | No load |

* The SP8785/6 may be operated with a +5.2V supply provided sufficient care is taken with supply decoupling and interfacing of input and outputs.

**Dynamic characteristics**

| Characteristic | Value Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| Max. toggle frequency | | | | | |
| SP8786 | 1300 | | | MHz | See Note 3 |
| SP8785 | 1000 | | | MHz | |
| Min. frequency sinewave drive | | | 150 | MHz | |
| Min. slew rate of square wave for correct operation to D.C. | | | 200 | V//μS | |
| Propagation delay clock input to output | | 2.5 | | μS | |
| Set up time | | .5 | | nS | See note 4 |
| Release time | | .5 | | nS | See note 5 |

NOTES:

1. Correct operation is specified for $V_{CC} - V_{EE}$ = 5.2V ± .25V
2. The input threshold and output voltage levels have the same temperature coefficients as ECL 111/10K.
3. The devices are dynamically tested using the circuit shown in Fig. 4 with input amplitudes of 400 and 1000 mVpp over the full temperature range.
4. Set up is defined as the minimum time that can elapse between a L → H transition of control input and the last L → H clock pulse transition to ensure the ÷20 mode is selected.
5. Release time is defined as the minimum time that can elapse between a H → L transition of the control input and the last L → H clock pulse transition to ensure the ÷22 mode is selected.

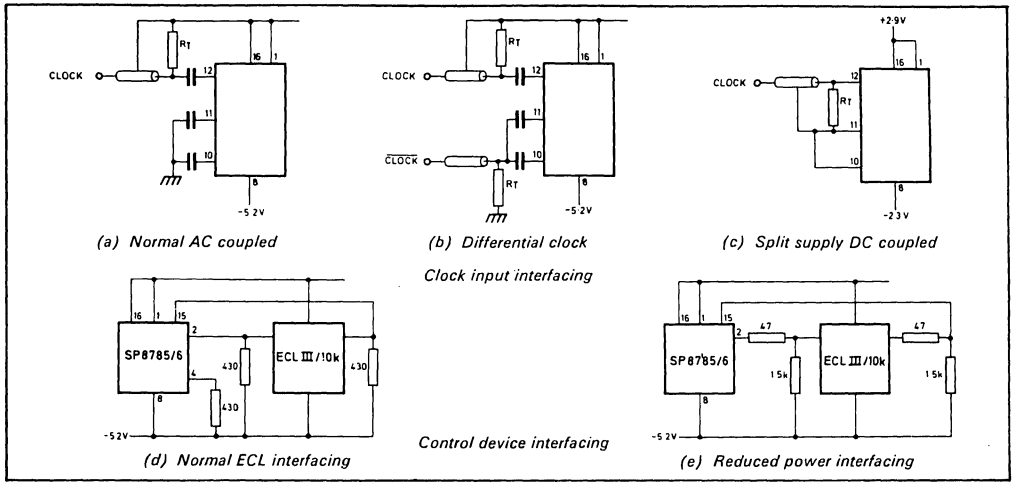



*Fig. 3 Interface circuit configurations*

## OPERATING NOTES

It is recommended that high frequency construction techniques are used with these devices with the positive rail connected to a ground plane. All components used in the circuit layout should be suitable for the frequencies involved.

The clock input to the device is normally capacitively coupled to the signal source as shown in Fig. 3a. The input is self biased by an internal 400Ω resistor to a bias voltage, and in order to complete the input path the two input reference pins must be decoupled to the earth plane with minimum of series inductance. Alternative connections which allow the use of complementary drive or DC coupling for added sensitivity are also shown in Fig. 3.

In the absence of an input signal, circuit will self oscillate with an output frequency of approximately 50MHz. This can be prevented by connecting a 10KΩ resistor between pin 11 and the negative rail. This offsets the input sufficiently to stop the oscillation but it also reduces the input sensitivity by approximately 100mV.

The SP8785/6 will miscount with low frequency sinewave inputs or slow ramps. A slew rate of 200V/μs or greater is necessary for safe operation at low frequencies.

The input impedance of the SP8785/6 is a function of frequency and minimises at about the same frequency as the maximum input sensivity, so although it can load the signal source significantly there is generally enough signal to operate the device satisfactorily when the input impedance is at a minimum. The worst case occurs at the maximum frequency because this is where the input sensitivity is worst.

The modulus control inputs have been designed to interface directly to ECL III/ECL10k since on ECL counter such as the 10136 is required to directly control the device at the maximum input clock frequency. If the input frequency is reduced or the modulus extended as shown in the application notes, the device may be controlled by a TTL. or CMOS. counter provided the loop delay requirements are met and suitable interfacing is applied. Unused PE inputs should be left open circuit.

The SP8785/6 have outputs which are compatable with the ECL 10k logic family. The device will drive 100Ω lines and can be used with line impedances down to 50Ω with a small loss in noise immunity.

An equal load on the unused output will reduce waveform distortion.

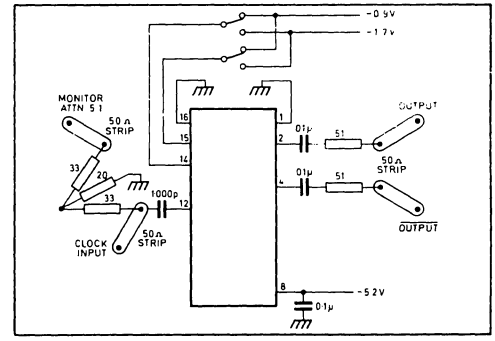



*Fig. 4 Dynamic test circuit (all capacitors 1000pF unless stated)*

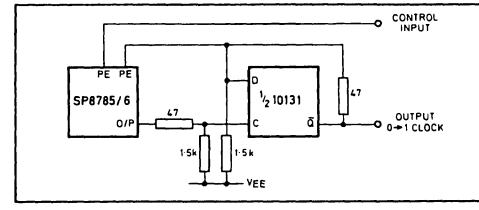



*Fig. 5 :- 40/42 control loop delay time 24ns typ.*

## APPLICATION NOTES

The SP8785/6 when used in a system operating at 1.3GHz may be controlled by a variable divider to give effective variable division at half the input frequency. The variable divider must produce a control signal within the period of the output of the SP8785/6 minus the delays within this device. The control loop delay time is typically 12 nsec.

Two methods may be used to achieve a satisfactory delay time within the control divider–

1. An extra divider may be inserted to increase the division ratio of the two modulus from 20/22 to 40/42, 80/82 or 100/102, hence reducing the control divider frequency and increasing the control loop delay time.
2. An ECL variable counter may be used to produce the control command. A device which is suitable is the 10136, in the ECL10k range.

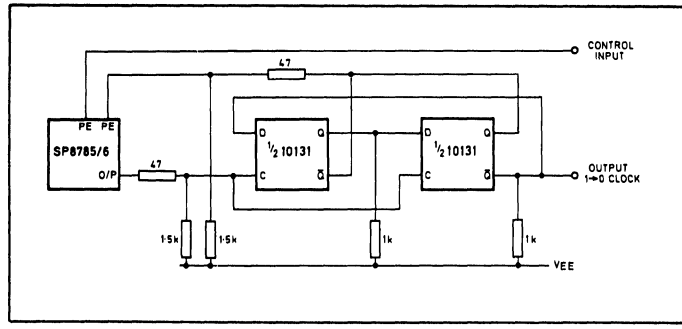



*Fig. 6 ÷ 80/81 control loop delay time 55ns typ.*

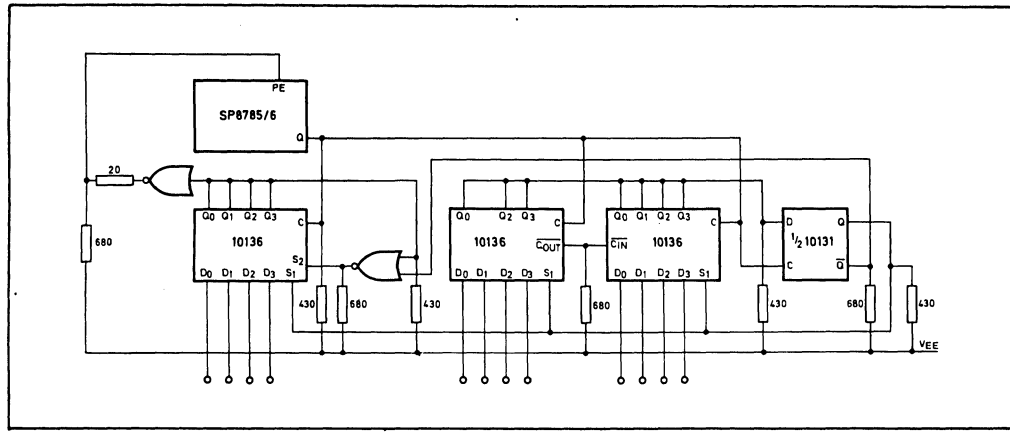



*Fig. 7 1.3 GHz variable divider (200—2000 in steps of 2)*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $V_{CC} - V_{EE}$ | 0V to +8V |
| Input voltage, PE inputs | $V_{EE}$ to $V_{CC}$ |
| Input voltage | 2V peak to peak |
| Output current | 40mA |
| Operating function temperature | +150°C |
| Storage temperature | −55°C to +150°C |

Plessey Semiconductors

# SP8000 SERIES

## HIGH SPEED DIVIDERS

# SP8790 A & B

## ÷4 EXTENDER FOR 2-MODULUS COUNTERS

The SP8790 is a divide-by-four counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratios. Thus a divide-by-10 or 11 with the SP8790 becomes a divide-by-40 or 41, a divide by 5 or 6 becomes a divide by 20 or 21.

The function is especially useful in low power frequency synthesisers because it can bring the output frequency of the combined 2-modulus counter and SP8790 into the region where CMOS or low power TTL can control the divider. The power-saving advantages are obvious.

The device interfaces easily to the SP8690 range of divide by 10 or 11s. The control inputs are TTL and CMOS compatible and the output is a free collector which, with the addition of a pull-up resistor, interfaces to CMOS and TTL.

The SP8790 is available in three temperature grades: 0 °C to + 70 °C (SP8790B) — 55 C to + 125 °C (SP8790A)

The SP8790 requires supplies of OV and + 5V ±0.25V.

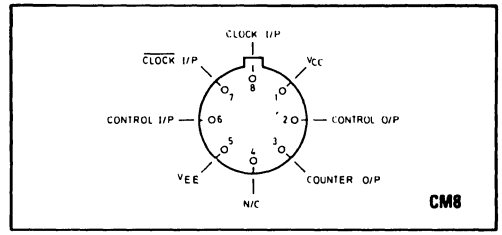



*Fig. 1 Pin connections*

### FEATURES

- Ultra-Low Power: 40mW
- Full Military Temperature Range
- I/P and O/P Interface Direct to CMOS/TTL

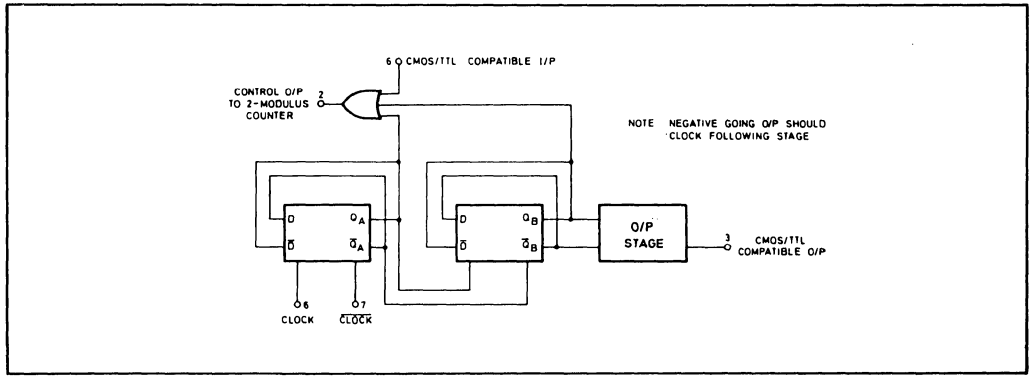



*Fig. 2 Logic diagram*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage \| Vcc—Vee\| | 8V |
| DC input voltage | Not greater than supply |
| AC input voltage | 2.5Vp-p |
| Output bias voltage | 12V |
| Control input bias voltage | 12V |
| Operating junction temperature | +150°C |
| Storage temp. range | —55°C to 150°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$: −55 C to +125 C (A grade)
0 C to +70 C (B grade)
$V_{CC}$ = +5V ± 5%
$V_{EE}$ = 0V
Clock input voltage with double complementary drive to CLOCK and $\overline{CLOCK}$ = 300mV to 1V p-p.

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Dynamic** | | | | | |
| Toggle frequency | See note 1 | | | MHz | |
| Min toggle frequency with sine-wave input | | | 20 | MHz | See note 2 |
| Min toggle frequency with square wave input | 0 | | | Hz | Slew rate 50V/µs |
| Clock to O/P delay (O/P − ve going) | | 14 | | ns | |
| Clock to O/P delay (O/P + ve going) | | 28 | | ns | |
| Control I/P to control O/P delay (O/P−ve going) | | 20 | | ns | 10kΩ pulldown on control O/P (See note 5) |
| Clock I/P to control O/P delay (O/P+ve going) | | 10 | | ns | 10kΩ pulldown on control O/P (See note 5) |
| Control I/P to control O/P delay (O/P−ve going) | | 12 | | ns | 4.3kΩ pulldown on control O/P (See note 6) |
| Control I/P to control O/P delay (O/P+ve going) | | 9 | | ns | 4.3kΩ pulldown on control O/P (See note 6) |
| Clock to control O/P delay (O/P −ve going) | | 26 | | ns | 10kΩ pulldown on control O/P (See note 5) |
| Clock to control O/P delay (O/P +ve going) | | 12 | | ns | 10kΩ pulldown on control O/P (See note 5) |
| Clock to control O/P delay (O/P−ve going) | | 17 | | ns | 4.3kΩ pulldown on control O/P (See note 6) |
| Clock to control O/P delay (O/P + ve going) | | 12 | | ns | 4.3kΩ pulldown on control O/P (See note 6) |
| **Static** | | | | | |
| Control I/P voltage level | | | | | |
| High state | 3.5 | | 10 | V | See note 3 |
| Low state | 0 | | 1.5 | V | |
| Output voltage level | | | | | |
| $V_{OL}$ | | | 0.4 | V | Sink current = 6.0mA |
| $V_{OH}$ (See note 4) | | | | | |
| Input impedance | | 1.6 | | kΩ | $f_{in}$ = 0Hz |
| Input vias voltage ($\overline{CLOCK}$ and CLOCK) | | 2.4 | | V | Inputs open circuit |
| Power supply drain current | | 8.0 | 11 | mA | |

NOTES

1. The maximum frequency of operation is in excess of 60MHz when the SP8790 is used as a prescaler. The limitation on this maximum frequency is the saturating O/P stage. When the SP8790 is used as a controller its internal delays do not permit operation at frequencies in excess of 40MHz.
2. The device will normally be driven from a 2-modulus divider which will have fast output edges. Hence, there is normally no input slew rate problem.
3. TTL devices require a pull-up resistor to ensure the required minimum of 3.5V. Note that the device can interface from 10V CMOS with no additional components.
4. $V_{OH}$ will be the supply voltage that the output pull-up resistor is connected to. This voltage should not exceed 12V.
5. The 10kΩ pulldown is the value of the input pulldown of the SP8695 with which the SP8790 can be used.
6. The 4.3kΩ pulldown is the value of the input pulldown of the SP8640 series SP8745 and SP8746 with which the SP8790 can be used.

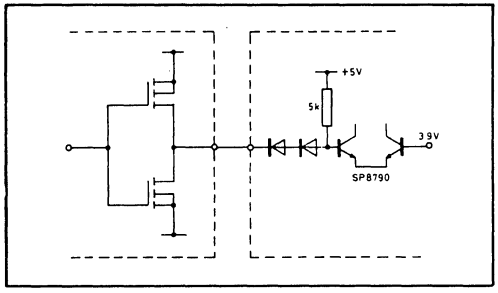



*Fig. 3 CMOS and TTL compatible control input*

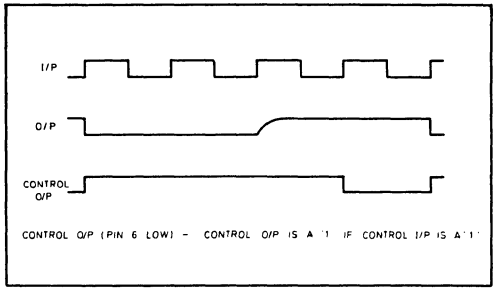



*Fig. 4 SP8790 waveforms*

## OPERATING NOTES

The SP8790 extends the division ratio of 2-modulus counters while retaining the same 2-modulus resolution. A typical application to give a ÷40/41 function is shown in Fig. 5. In this basic form, however, the devices will self-oscillate if no input signal source is present. This may be prevented by using one of the arrangements shown in Fig. 6.

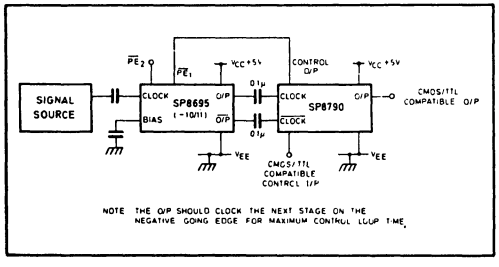



*Fig. 5 SP8790 with SP8695 connected to give a ÷40/4*

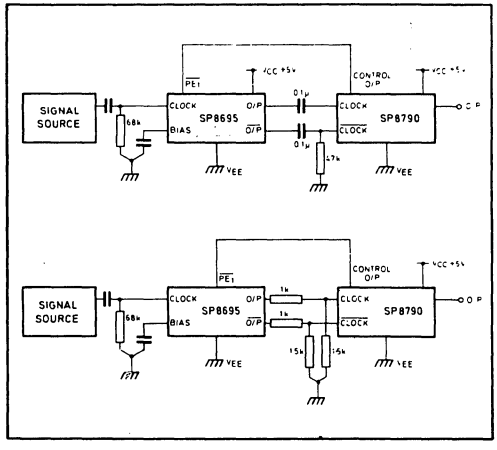



*Fig. 6 Methods of preventing self-oscillation*

| TRUTH TABLE | |
|---|---|
| **Control Input** | **Div. Ratio With ÷10/11** |
| 0 | 41 |
| 1 | 40 |

Max input frequency to combination=200MHz (min.).
Power consumption of combination=120mWtyp.
Time available to control the ÷40/41=(40 clock periods minus delays through the dividers) — 340ns ($f_{in}$=100MHz).

# SP8792 ÷ 80/81 SP8793 ÷ 40/41

## 200 MHz VERY LOW POWER PROGRAMMABLE DIVIDERS

The SP8792 and SP8793 are very low power (20 mW) programmable ÷80/81 and ÷40/41 counters which operate at input frequencies in excess of 200 MHz over the temperature range -30°C to +70°C.

The signal (clock) inputs are biased internally and require to be capacitor coupled. The output stage, normally open collector, can be powered up by linking pins 2 and 7 to drive one TTL load.

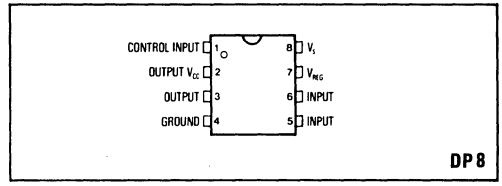



*Fig.1 Pin connections (viewed from above)*

### FEATURES

- DC to 200 MHz Operation
- -30°C to +70°C Temperature Range
- Control Inputs and Output CMOS Compatible

### QUICK REFERENCE DATA

- Supply Voltages: 6.8 V to 13.5 V or 5.2 V ± 0.25 V
- Supply Current: 4 mA typ., 7 mA max.

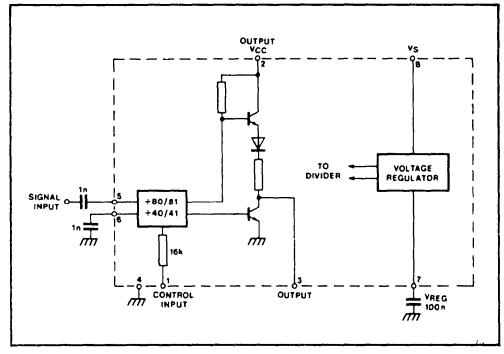



*Fig.2 Block diagram*

### ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Supply voltage $V_S$: 6.8 V to 13.5 V (pin 8)
or 5.2 V ± 0.25 V (pins 7 + 8)
Input signal amplitude: 100 mV to 800 mV pk-pk
Ambient temperature: -30°C to 70°C

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min | Typ. | Max | | |
| Supply current | | 4 | 7 | mA | Control input O/C. TTL O/P not connected. |
| Max. input frequency | 200 | | | MHz | |
| Min. input frequency | | | 20 | MHz | 400 mV pk-pk sine wave input |
| Min. slew rate (with square wave input) | | 12 | 20 | V/μs | |
| Output voltage level (low) | | | 0.5 | V | 2 mA current, pin 2 open or linked to pin 7. |
| Output voltage level (high) | 4.8 | | | V | Vcc = 6.8 V, pins 2,7 linked. |
| Control input level (low) | | | 2.0 | V | ÷41 or ÷81 |
| Control input level (high) | 4.0 | | | V | ÷40 or ÷80 |
| Propagation delay, clock input to output | | 30 | | ns | Output 1 to 0 transition — SP8793 |
| | | 35 | | ns | SP8792 |
| Set up time | | 8 | | ns | See note 1. |
| Release time | | 8 | | ns | See note 2. |
| Output mark-space ratio | | 1:2 | | | At 200 MHz at 50% of output swing. |

NOTES

1. The minimum time between a L → H transition of control input and the last L → H signal input transition to ensure the ÷40 or ÷80 mode is selected.
2. The minimum time between a H → L transition of control input and the last L → H signal input transition to ensure the ÷41 or ÷81 mode is selected.

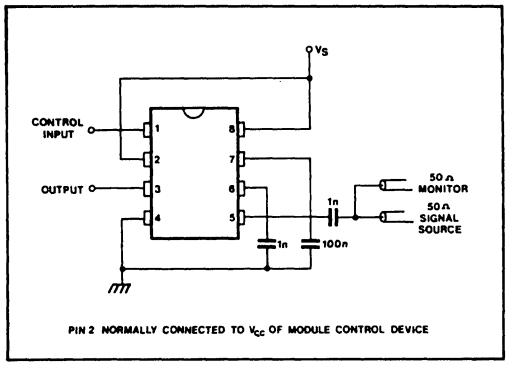



*Fig.3 SP8792/3 application diagram. The regulator can be used to supply other circuitry if required. If load exceeds 1 mA an emitter follower transistor must be used.*

## ABSOLUTE MAXIMUM RATINGS

| | | |
|---|---|---|
| Supply voltage (pins 8,2) | : | 14.5V |
| Storage temperature | : | -55°C to +125°C |

# SP 8794 A&B

## ÷ 8 CONTROL CIRCUIT FOR 2 - MODULUS DIVIDERS

The SP8794 is a divide by eight counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratios. Thus a divide by 10 or 11 with the SP8794 becomes a divide by 80 or 81, a divide by 5 or 6 becomes a divide by 40 or 41.

The function is especially useful in low power frequency synthesisers because it can bring the output frequency of the combined 2-modulus counter and SP8794 into the region where CMOS or low power TTL can control the divider.

The device interfaces easily to the SP8000 range of 2-modulus dividers. The control I/Ps are TTL and CMOS compatible and the output is a free collector which, with the addition of a pull-up resistor, interfaces to CMOS and TTL.

The SP8794 is available over three temperature ranges: 0°C to +70°C (SP8794B), −40°C to +85°C (SP8794M) and −55°C to +125°C (SP8794A).

The SP8794 requires supplies of 0V and +5V ± 0.25V

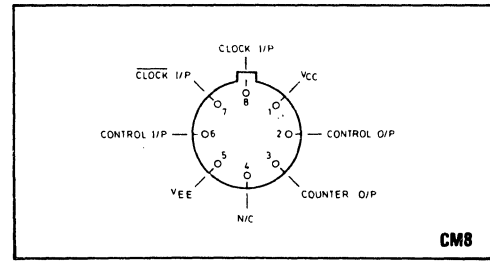



*Fig. 1 Pin connections.*

### FEATURES

- Ultra-Low Power: 40mW
- Full Military Temperature Range
- Direct I/P & O/P Interfacing to CMOS & TTL
- Operates with 500MHz ÷ 10/11

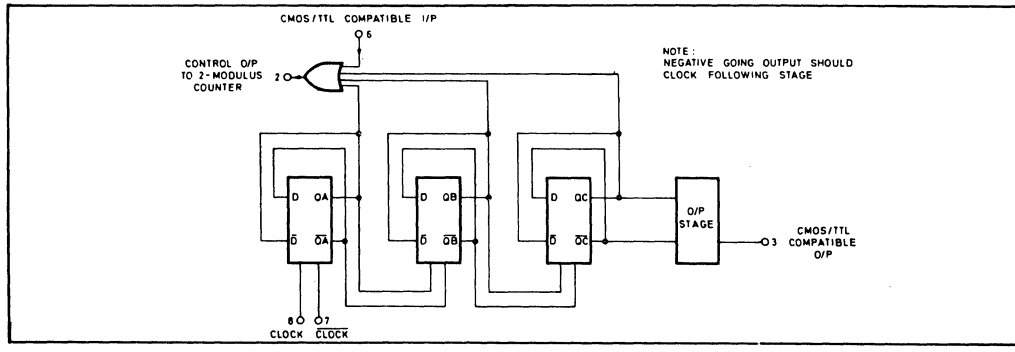



*Fig. 2 Logic diagram.*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$ | 8V |
| DC input voltage | Not greater than supply |
| AC input voltage | 2.5Vp-p |
| Output bias voltage | 12V |
| Control input bias voltage | 12V |
| Operating juntion temperature | +150°C |
| Storage temp. range | −55°C to 150°C |

### APPLICATION

- Frequency Synthesisers

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$: 'A' grade −55°C to +125°C
'B' grade 0°C to +70°C
$V_{CC}$ = +5V ±5%
$V_{EE}$ = 0V
Clock input voltage with double complementary drive to CLOCK and $\overline{CLOCK}$ = 300mV to 1V p-p.

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Dynamic** | | | | | |
| Toggle frequency | 120 | | | MHz | SP8794 as a prescaler (see note 1) |
| | 40 | | | MHz | SP8794 controlling a 2-modulus divider (see note 1) |
| Min. toggle frequency with sinewave input | | | 20 | MHz | See note 2 |
| Min. toggle frequency with square wave input | 0 | | | Hz | Slew rate > 50V/μs |
| Clock to O/P delay (O/P −ve going) | | 18 | | ns | |
| Clock to O/P delay (O/P +ve going) | | 32 | | ns | |
| Control I/P to control O/P delay (O/P −ve going) | | 20 | | ns | 10kΩ pulldown on O/P, see note 5 |
| Control I/P to control O/P delay (O/P +ve going) | | 10 | | ns | 10kΩ pulldown on O/P, see note 5 |
| Control I/P to control O/P delay (O/P −ve going) | | 12 | | ns | 4.3kΩ pulldown on O/P, see note 6 |
| Control I/P to control O/P delay (O/P +ve going) | | 9 | | ns | 4.3kΩ pulldown on O/P, see note 6 |
| Clock to control O/P delay (O/P −ve going) | | 30 | | ns | 10kΩ pulldown on O/P, see note 5 |
| Clock to control O/P delay (O/P +ve going) | | 16 | | ns | 10kΩ pulldown on O/P, see note 5 |
| Clock to control O/P delay (O/P −ve going) | | 21 | | ns | 4.3kΩ pulldown on O/P, see note 6 |
| Clock to control O/P delay (O/P +ve going) | | 16 | | ns | 4.3kΩ pulldown on O/P, see note 6 |
| **Static** | | | | | |
| Control I/P voltage level | | | | | |
| High state | 3.5 | | 10 | V | See note 3 |
| Low state | 0 | | 1.5 | V | |
| Output voltage level | | | | | |
| $V_{OL}$ | | | 0.4 | V | Sink current = 6.0mA |
| $V_{OH}$ (see note 4) | | | 12 | V | See note 4 |
| Input impedance | | 1.6 | | kΩ | $f_{in}$ = 0Hz |
| I/P bias voltage (CLOCK & $\overline{CLOCK}$) | | | | | |
| Power supply drain current | | | | | |

NOTES
1. The maximum frequency of operation is in excess of 120MHz when the SP8794 is used as a prescaler. The limitation on its maximum operating frequency is the saturating output stage. When the SP8794 is used as a controller for a 2-modulus device its internal delays do not permit operation at frequencies above 40MHz.
2. The device will normally be driven from a 2-modulus divider which will have fast output edges. Hence, there is normally no input slew rate problem.
3. TTL devices require a pull-up resistor to ensure the required minimum of 3.5V. Note that the device can interface from 10V CMOS with no additional components.
4. $V_{OH}$ will be the supply voltage that the output pull-out resistor is connected to. This voltage should not exceed 12V.
5. The 10kΩ pulldown is the value of the input pulldown of the SP8695, with which the SP8794 can be used.
6. The 4.3kΩ pulldown is the value of the input pulldown of all the SP8640 series ÷ 10/11 devices, the SP8740 & SP8745 ÷ 5/6, the SP8741 & SP8746 ÷ 6/7 and the SP8743 ÷ 8/9, with which the SP8794 can be used.

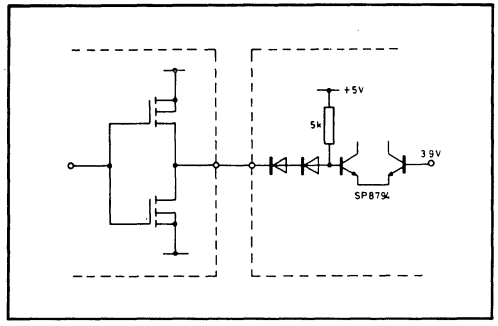



*Fig. 3 CMOS and TTL compatible control I/P.*

| TRUTH TABLE | |
|---|---|
| **Control I/P** | **Div. Ratio with ÷ 10/11** |
| 0 | 81 |
| 1 | 80 |

Max input frequency to combination = 200MHz (min.).
Power consumption of combination = 120mWtyp.
Time available to control the ÷ 80/81
= 80 clock periods minus delays through dividers
≅740ns ($f_{in}$ = 100MHz)

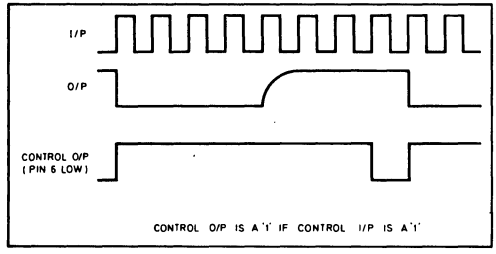



*Fig. 4 SP8794 waveforms*

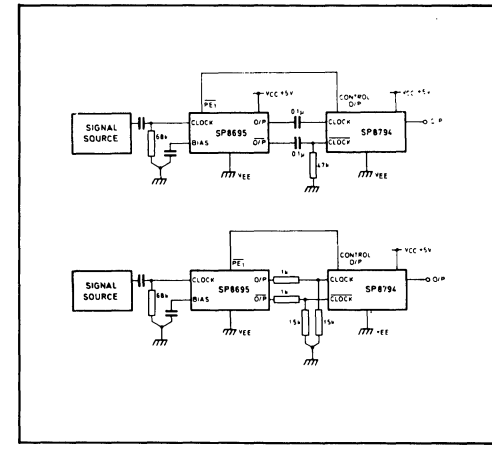



*Fig. 6 Methods of preventing self-oscillation.*

## APPLICATION NOTES

The SP8794 extends the division ratio of 2-modulus counters while retaining the same 2-modulus resolution. A typical application to give a ÷ 80/81 function is shown in Fig. 5. In this basic form, however, the devices will self-oscillate if no input signal source is present, This may be prevented by using one of the arrangements shown in Fig. 6.

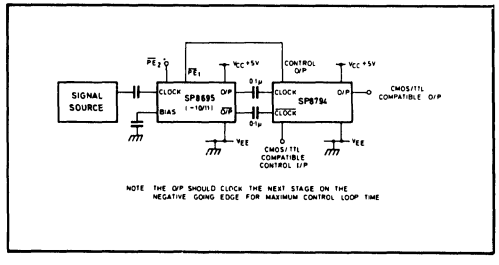



*Fig. 5 SP8794 with SP8695 connected to give a low power ÷ 80/81*

# SP8901

## FOUR-MODULUS DIVIDER (÷512)

The SP8901 is a four modulus ÷512 operating at frequencies up to 1GHz. The device has a typical power dissipation of 500mW, and operates over the temperature range -30°C to 70°C. The SP8901 has been designed to interface with the NJ8811 to produce a 16-bit binary programmed frequency synthesiser.

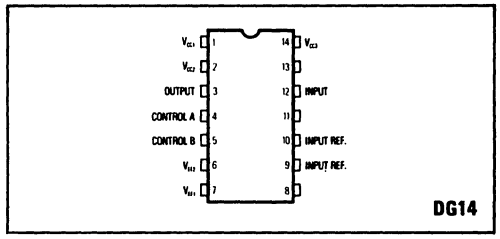



*Fig.1 Pin connections*

### FEATURES

- Self Biasing Clock Inputs
- Current Limited TTL/MOS Compatible Inputs
- TTL/MOS Compatible Control Inputs
- 5V Supply
- Variable Input Hysteresis Capability For Wide Band Operation

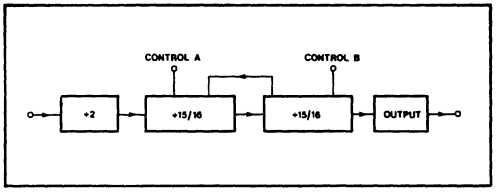



*Fig.2 Logic diagram of SP8901*

### APPLICATIONS

- Mobile Radio
- Scanning Radio Receivers
- Microprocessor Controlled Frequency Synthesis

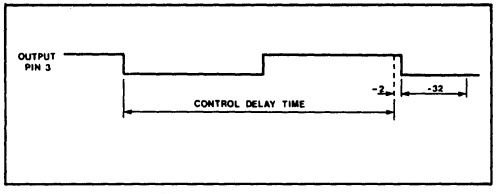



*Fig.3 Output waveform*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply voltage ($V_{CC} - V_{EE}$) | 8V |
| Input voltage, Clock inputs | 2.5V p-p |
| Control inputs | -0.5V to +8V |
| Storage temperature | -55°C to +150°C |

### ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**
Supply Voltage: $V_{CC}$ +5.0V ±0.25V, $V_{EE}$: 0V
$T_{amb}$: -30°C to +70°C
Clock Input: 400mV to 1.0V peak to peak

**Dynamic Characteristics**

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min | Typ. | Max | | |
| Max. input frequency | 900 | | | MHz | $V_{CC3}$ = 5V See Fig.4 |
| Max. input frequency | 1.0 | | | GHz | $V_{CC3}$ = 6.8V See Fig.4 |
| Min. input frequency with sinewave input | | 50 | 100 | MHz | 600mV p-p |
| Min. slew rate of square wave input | | | 200 | V/μs | |
| Clock to output delay | | 40 | 60 | ns | |
| Control setup and release time: | | | | | |
| Control A input | | 2 | | ns | |
| Control B input | | 5 | | ns | |

**Static Characteristics ($T_{amb}$ = +25°C)**

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min | Typ. | Max | | |
| Logic '1' output voltage | 3.5 | | | V | |
| | 2.5 | | | V | 1mA source |
| Output short circuit current | | | 10 | mA | |
| Logic '0' output voltage | | | 0.5 | V | 2mA sink |
| Supply current | | 100 | 135 | mA | |
| Control inputs: | | | | | |
| Min. input high level | | | 2.3 | V | |
| Max. input low level | 1.3v | | | V | |
| Low level input current | | 0.8 | 1.2 | mA | $V_{in}$ = 0.5V |

## OPERATING NOTES

The circuit is configured as two ÷15/16 counters which are clocked via a front end ÷2 counter as shown in Fig.2. The circuit will divide by 512 when the control inputs are left open circuit or both inputs are at logic '1'. The control A and B pins control the minus 2 and 32 counters respectively, when a logic '0' signal is applied. Table 1 shows the division ratios. The minus 2 counts of the control A occur before the negative going output edge, whereas the minus 32 counts occur after the negative going edge as shown in Fig.3. The maximum possible control delay is obtained by clocking the control device on the negative going edge of the SP8901, and is equal to 480 clock input periods (minus the internal delays in the SP8901).

The clock input should be correctly terminated and all input coupling and decoupling capacitors should be of a type suitable for operation at 1GHz. At low frequencies the divider is limited by the slew rate of the input signal and for correct operation this must be greater than 200V/μs. The low frequency sinewave operation of the device can be improved by adding hysteresis to the reference inputs. This can be carried out externally as shown in Fig.4 and can be measured as $V_{ref1} - V_{ref2}$. Care must be taken when applying hysteresis as large values of hysteresis will degrade the input sensitivity at maximum frequency. A maximum value of 50mV (R1 = 33kΩ) should not be exceeded.

The output is TTL or MOS compatible and is current limited at 3mA sink in the low state and 5mA source in the high state. The modulus control inputs have a 5kΩ pull up resistor and can be interfaced to open collector or open drain circuits. There are separate supply lines for the output ($V_{CC2}$, $V_{EE2}$) to reduce both input to output and output to input coupling.

A separate supply pin ($V_{CC3}$) is available for the front end ÷2, and determines the maximum frequency of the device. With $V_{CC3}$ connected to the 5V supply the circuit will operate up to 900MHz. The high frequency limit may be increased to 1GHz by connecting $V_{CC3}$ to 6.8V. Under certain conditions, an oscillation can occur when the device is dynamically clocked. This may be cured by the insertion of a 1μH RF choke in series with $V_{CC1}$ & $V_{CC2}$. Under these conditions, $V_{CC1}$ & $V_{CC2}$ pins should not be decoupled.

| Control A | Control B | Ratio |
|---|---|---|
| 1 | 1 | 512 |
| 0 | 1 | 510 |
| 1 | 0 | 480 |
| 0 | 0 | 478 |

*Table 1 Divide ratios*

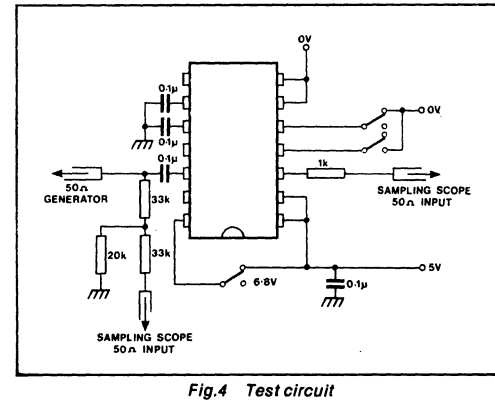



*Fig.4 Test circuit*

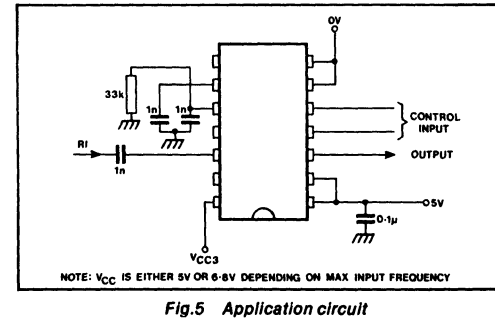



*Fig.5 Application circuit*

# SP8906

## FOUR-MODULUS DIVIDER (÷256)

The SP8906 is a four modulus ÷256 operating at frequencies up to 500MHz. The device has a typical power dissipation of 400mW, and operates over the temperature range -30°C to 70°C. The SP8906 has been designed to interface with the NJ8811 to produce a 16 bit binary programmed frequency synthesiser, but can also be interfaced with standard MOS programmable dividers to produce a wide range of general purpose synthesisers.

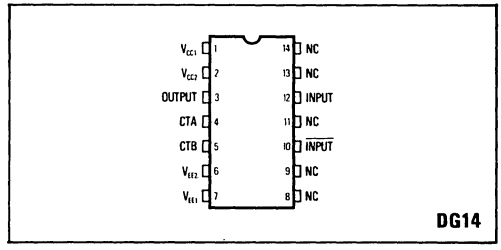



*Fig.1 Pin connections*

### FEATURES

- Self Biasing Clock Inputs
- Current Limited TTL/MOS Compatible
- TTL/MOS Compatible Control Inputs
- 5V Supply

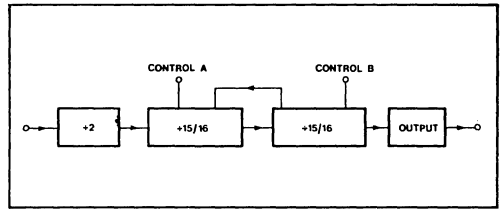



*Fig.2 Block diagram*

### APPLICATIONS

- Mobile Radio
- Scanning Radio Receivers
- Microprocessor Controlled Frequency Synthesis

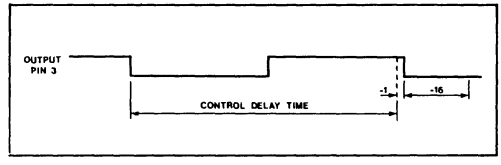



*Fig.3 Output waveform*

### ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Supply voltage: $V_{CC}$ +5.0V ±0.25V $V_{EE}$: 0V
$T_{amb}$: -30°C to +70°C
Clock input: 400mV to 1.0V peak to peak

**Dynamic Characteristics**

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min | Typ. | Max | | |
| Max. input frequency | 500 | | | MHz | $V_{CC}$ = 5V |
| Min. input frequency with sine wave input | | 10 | 20 | MHz | 600mV p-p |
| Min. slew rate of square wave input | | | 50 | V/μs | |
| Clock to output delay | | 40 | 60 | ns | |
| Control setup and release time: | | | | | |
| Control A Input | | 2 | | ns | |
| Control B Input | | 5 | | ns | |

**Static characteristics ($T_{AMB}$ = 25°C)**

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min | Typ. | Max | | |
| Logic '1' output voltage | 3.5<br>2.5 | | | V<br>V | <br>1mA source |
| Output short circuit current | | | 10 | mA | |
| Logic '0' output voltage | | | 0.5 | V | 2mA sink |
| Supply current | | 75 | 100 | mA | |
| Control inputs: | | | | | |
| Min. input high level | | | 2.3 | V | |
| Max. input low level | 1.3 | | | V | |
| Low level input current | | 0.8 | 1.2 | mA | Vin = 0.5V |

## OPERATING NOTES

The circuit is configured as two ÷15/16 counters which are clocked via a front end amplifier as shown in Fig.2. The circuit will divide by 256 when the control inputs are left open circuit or both inputs are at logic '1'. The control A and B pins control the minus 1 and 16 counters respectively, when a logic '0' signal is applied. Fig.3 shows the division ratio table. The minus 1 counts of the control A occur before the negative going output edge, whereas the minus 16 counts occur after the negative going edge as shown in Fig.4. The maximum possible control delay is obtained by clocking the control device on the negative going edge of the SP8906, and is equal to 240 clock input periods (minus the internal delays in the SP8906).

The clock input should be correctly terminated and all input coupling and decoupling capacitors should be of a type suitable for operation at 500MHz. At low frequencies the divider is limited by the slew rate of the input signal and for correct operation this must be greater than 50V/μs. If the input to the device is likely to be interrupted the device will tend to self-oscillate at an output frequency of 2MHz. This can be prevented by the addition of $R_1$ = 120kΩ but will cause a loss of input sensitivity. (See Fig.8.) Under certain conditions, an oscillation can occur when the device is dynamically clocked. This may be cured by the insertion of a 1μH RF choke in series with $V_{CC1}$ and $V_{CC2}$ . Under these conditions, $V_{CC1}$ and $V_{CC2}$ pins should not be decoupled.

The output is TTL or MOS compatable and is current limited at 3mA sink in the low state and 5mA source in the high state. The modulus control inputs have a 5kΩ pull up resistor and can interface to open collector, open drain circuits on totem pole outputs. There are separate supply lines for the output ($V_{CC2}$, $V_{EE2}$) to reduce both input to output and output to input coupling.

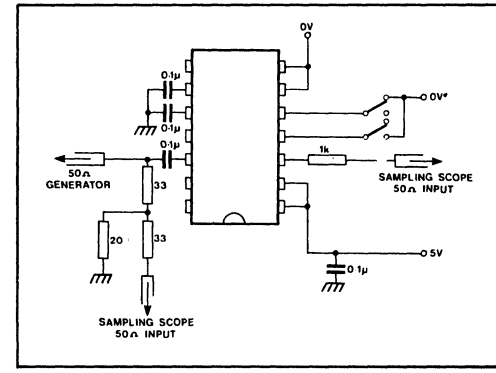



*Fig.4 Test circuit*

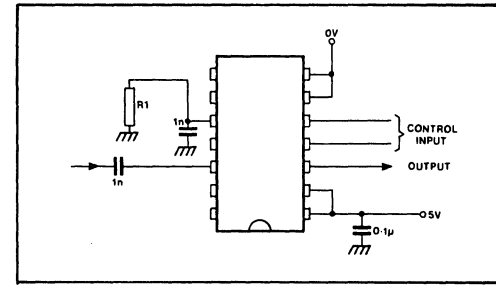



*Fig.5 Application circuit*

| Control A | Control B | Ratio |
|---|---|---|
| 1 | 1 | 256 |
| 0 | 1 | 255 |
| 1 | 0 | 240 |
| 0 | 0 | 239 |

*Table 1 Divide ratios*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage ($V_{CC}$ — $V_{EE}$) | 8V |
| Input voltage, clock inputs | 2.5V peak to peak |
| Control inputs | -0.5V to 8V |
| Storage temperature | -55°C to 150°C |

## 40 – CHANNEL CITIZENS' BAND SYNTHESISER IC SETS

# SP8922 SP8921 SP8923

BINARY BCD

Recognising the different requirements of citizens' band transceiver manufacturers, Plessey Semiconductors have developed a range of integrated circuits for 40-channel CB. This datasheet describes three of these: SP8921, SP8922 and SP8923.

The devices are designed for use in pairs. SP8922 and SP8921 incorporate all the functions for a synthesised local oscillator with binary-coded channel entry; the SP8923/21 pair offering similar facilities but with BCD channel entry.

### FEATURES

- Low External Component Count
- Binary (SP8922) or BCD (SP8923) Channel Setting
- Internal Pulldowns on Channel I/Ps
- Integral 10.24MHz Crystal Oscillator with Buffered O/P
- 10.695MHz IF Offset for Double Conversion
- 455 kHz IF offset for Single Conversion
- No Mixing or Prescaling Required between VCO and Synthesiser I/P
- Digital Phase/Frequency Comparator has Source and Sink O/Ps
- Lock Detect O/P
- 5V Supply Rail
- Low Power: 225mW Typ. (SP8921)
  225mW Typ. (SP8922)
  325mW Typ. (SP8923)

The synthesisers are partitioned into two parts as shown in Figs. 2 and 3. The SP8922 and SP8923 contain a preamplifier followed by a fixed divide by four prescaler. The amplifier input will accept a signal at a frequency up to 30MHz. The input is a high impedance and requires an AC coupled source which is achieved by a series capacitor. The prescaler is followed by seven bits of programmable division. In the SP8922, these seven bits are programmed from the six binary inputs, as shown in Table 1, plus the 5kHz program input.

The SP8923 is programmed by seven BCD channel inputs (see Table 2), the 40 input codes being converted by a decoding matrix to the appropriate citizens' band frequencies.

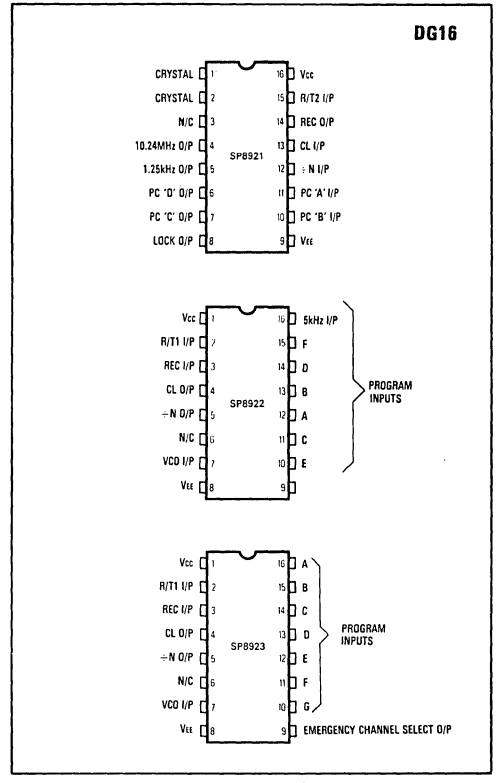



*Fig. 1 Pin connections (top view)*

A receive/transmit (R/T) input is provided on both SP8922 and SP8923 to give an offset of 91 counts (corresponding to −455kHz) when the receive mode is selected.

Clock and preset outputs to the SP8921 are provided by SP8922 and SP8923, which in turn accept a recognition signal from the SP8921.

Pin 9 on the SP8923 is an Emergency Channel Select output, which gives a low output whenever channel 9,

or a non-permitted channel, is selected. When this output is low, the synthesiser programs to channel 9.

The device common to both sets, SP8921, contains the six most significant bits of the programmable counter, a 10.24MHz crystal oscillator maintaining circuit, a $2^{13}$ fixed divider, and a digital phase/frequency comparator. The six bits of the programmable counter have a fixed preset code which, combined with the variable code of the SP8922 or SP8923, give the total count required to select the 40 citizens' band frequencies. The R/T input to the SP8921 gives an offset in the programmable count of minus 2048 (corresponding to −10.24 MHz) when in the receive mode.

The crystal oscillator has a direct emitter follower output which may be used as an input to the second mixer in a double conversion transceiver as shown in Fig. 4. The oscillator is connected internally to the fixed divider, which gives an output reference frequency of 1.25kHz with a 10.24MHz crystal. The phase/frequency comparator has two outputs which may be used to drive a variety of charge pump filter circuits as shown in Figs. 7 through10.There is also a 'lock detect' output which requires an external filter as shown in Figs. 2 and 3.

The frequencies available from the SP8922/1 and SP8923/1 when connected in a synthesiser loop are shown in Tables 1 and 2 respectively.

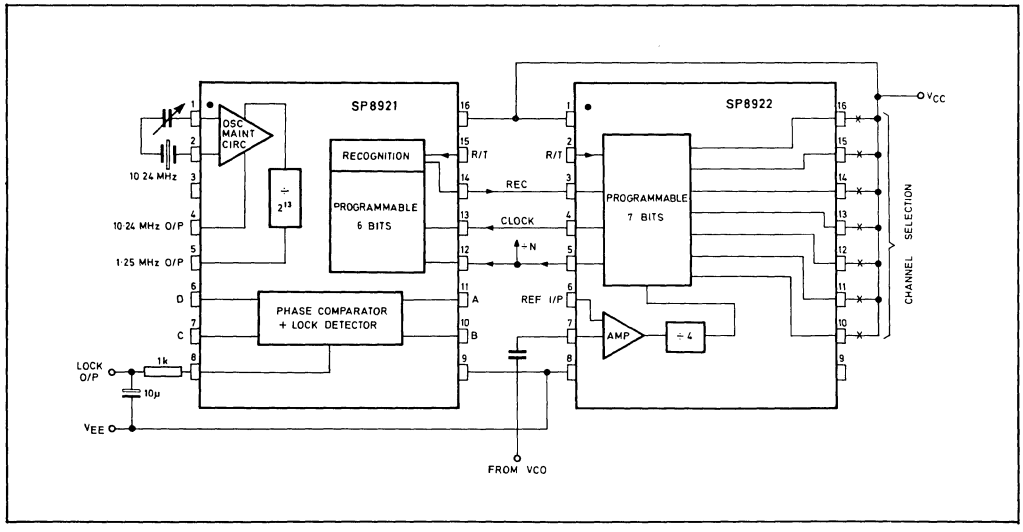



*Fig. 2 SP8921/SP8922 interconnections (10.695MHz receive offset)*

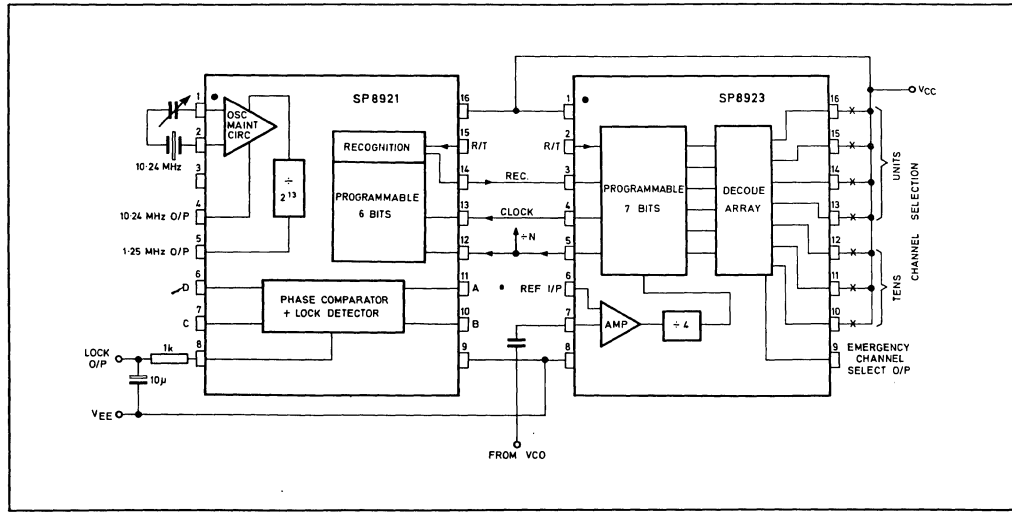



*Fig. 3 SP8921/SP8923 interconnections (10.695MHz receive offset)*

## ELECTRICAL CHARACTERISTICS

**Test Conditions (unless otherwise stated)**
$V_{EE}$ = 0V, $V_{CC}$ = +4.75V to +5.5V
$T_A$ = −30°C to +70°C

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Inputs (see Note 1)** | | | | | |
| Low | 0 | | 0.5 | V | |
| High | 2.4 | | Vcc | V | |
| VCO | 0.4 | | 1.0 | Vp-p | AC-coupled |
| Max. clock frequency | 30 | 50 | | MHz | |
| **Outputs (except 10.24MHz O/P and** phase comparator C and D O/Ps) | | | | | |
| Low | | | 0.5 | V | 6mA sink |
| High | Vcc−0.5 | | | V | No load, see Note 2 |
| **10.24MHz O/P** | 600 | 800 | | mVp-p | |
| **Phase comp. C O/P** | | | | | |
| Leakage O/P high | | | 50 | µA | |
| O/P low | | | 0.5 | V | 5mA sink |
| **Phase comp. D O/P** | | | | | |
| Leakage O/P low | | | 50 | µA | |
| O/P high | Vcc−1.2 | | | V | 5mA source |
| **Power supply** | | | | | |
| Vcc | +4.75 | | +5.5 | V | |
| Icc SP8921 | | 45 | 60 | mA | |
| SP8922 | | 45 | 60 | mA | |
| SP8923 | | 65 | 90 | mA | |

NOTES
1. Programming inputs may be left open circuit as input low, or connected Vcc as input high. All inputs (except VCO I/P) have internal 10k Ω pull down resistors to $V_{EE}$. SP8922, SP8923 pin 6 is the VCO I/P reference; this pin may be left open circuit, or decoupled to $V_{EE}$ to improve I/P sensitivity.
2. Outputs have an internal 5k Ω pull up resistor to Vcc. Lock output (SP8921 pin 8) has an internal 10k Ω pull up resistor to Vcc.

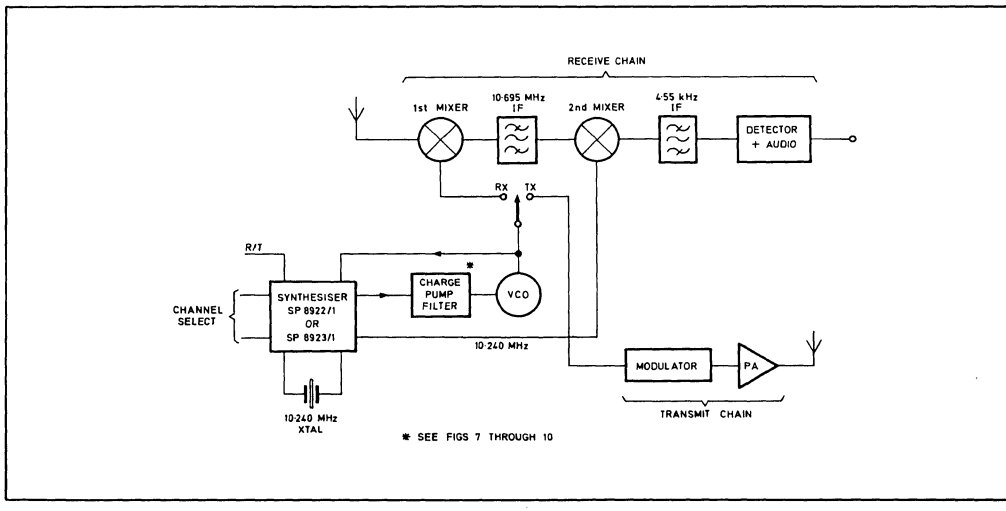



*Fig. 4 Double conversion transceiver*

| Channel No. | Input Code F E D C B A | Output frequency with R/T = 0 (MHz) |
|---|---|---|
| 1 | 0 0 0 1 1 1 | 26.965 |
| 2 | 0 0 1 0 0 0 | 26.975 |
| 3 | 0 0 1 0 0 1 | 26.985 |
| 4 | 0 0 1 0 1 1 | 27.005 |
| 5 | 0 0 1 1 0 0 | 27.015 |
| 6 | 0 0 1 1 0 1 | 27.025 |
| 7 | 0 0 1 1 1 0 | 27.035 |
| 8 | 0 1 0 0 0 0 | 27.055 |
| 9 | 0 1 0 0 0 1 | 27.065 |
| 10 | 0 1 0 0 1 0 | 27.075 |
| 11 | 0 1 0 0 1 1 | 27.085 |
| 12 | 0 1 0 1 0 1 | 27.105 |
| 13 | 0 1 0 1 1 0 | 27.115 |
| 14 | 0 1 0 1 1 1 | 27.125 |
| 15 | 0 1 1 0 0 0 | 27.135 |
| 16 | 0 1 1 0 1 0 | 27.155 |
| 17 | 0 1 1 0 1 1 | 27.165 |
| 18 | 0 1 1 1 0 0 | 27.175 |
| 19 | 0 1 1 1 0 1 | 27.185 |
| 20 | 0 1 1 1 1 1 | 27.205 |
| 21 | 1 0 0 0 0 0 | 27.215 |
| 22 | 1 0 0 0 0 1 | 27.225 |
| 23 | 1 0 0 1 0 0 | 27.255 |
| 24 | 1 0 0 0 1 0 | 27.235 |
| 25 | 1 0 0 0 1 1 | 27.245 |
| 26 | 1 0 0 1 0 1 | 27.265 |
| 27 | 1 0 0 1 1 0 | 27.275 |
| 28 | 1 0 0 1 1 1 | 27.285 |
| 29 | 1 0 1 0 0 0 | 27.295 |
| 30 | 1 0 1 0 0 1 | 27.305 |
| 31 | 1 0 1 0 1 0 | 27.315 |
| 32 | 1 0 1 0 1 1 | 27.325 |
| 33 | 1 0 1 1 0 0 | 27.335 |
| 34 | 1 0 1 1 0 1 | 27.345 |
| 35 | 1 0 1 1 1 0 | 27.355 |
| 36 | 1 0 1 1 1 1 | 27.365 |
| 37 | 1 1 0 0 0 0 | 27.375 |
| 38 | 1 1 0 0 0 1 | 27.385 |
| 39 | 1 1 0 0 1 0 | 27.395 |
| 40 | 1 1 0 0 1 1 | 27.405 |

*Table 1 SP8922/1 O/P frequencies with 10.240 crystal (0 contact open, 1 contact closed to VCC)*

| Channel No. | Input Code G F E D C B A | Output Frequency with R/T – 0 (MHz) |
|---|---|---|
| 1 | 0 0 0 0 0 0 1 | 26.965 |
| 2 | 0 0 0 0 0 1 0 | 26.975 |
| 3 | 0 0 0 0 0 1 1 | 26.985 |
| 4 | 0 0 0 0 1 0 0 | 27.005 |
| 5 | 0 0 0 0 1 0 1 | 27.015 |
| 6 | 0 0 0 0 1 1 0 | 27.025 |
| 7 | 0 0 0 0 1 1 1 | 27.035 |
| 8 | 0 0 0 1 0 0 0 | 27.055 |
| 9 | 0 0 0 1 0 0 1 | 27.065 |
| 10 | 0 0 1 0 0 0 0 | 27.075 |
| 11 | 0 0 1 0 0 0 1 | 27.085 |
| 12 | 0 0 1 0 0 1 0 | 27.105 |
| 13 | 0 0 1 0 0 1 1 | 27.115 |
| 14 | 0 0 1 0 1 0 0 | 27.125 |
| 15 | 0 0 1 0 1 0 1 | 27.135 |
| 16 | 0 0 1 0 1 1 0 | 27.155 |
| 17 | 0 0 1 0 1 1 1 | 27.165 |
| 18 | 0 0 1 1 0 0 0 | 27.175 |
| 19 | 0 0 1 1 0 0 1 | 27.185 |
| 20 | 0 1 0 0 0 0 0 | 27.205 |
| 21 | 0 1 0 0 0 0 1 | 27.215 |
| 22 | 0 1 0 0 0 1 0 | 27.225 |
| 23 | 0 1 0 0 0 1 1 | 27.255 |
| 24 | 0 1 0 0 1 0 0 | 27.235 |
| 25 | 0 1 0 0 1 0 1 | 27.245 |
| 26 | 0 1 0 0 1 1 0 | 27.265 |
| 27 | 0 1 0 0 1 1 1 | 27.275 |
| 28 | 0 1 0 1 0 0 0 | 27.285 |
| 29 | 0 1 0 1 0 0 1 | 27.295 |
| 30 | 0 1 1 0 0 0 0 | 27.305 |
| 31 | 0 1 1 0 0 0 1 | 27.315 |
| 32 | 0 1 1 0 0 1 0 | 27.325 |
| 33 | 0 1 1 0 0 1 1 | 27.335 |
| 34 | 0 1 1 0 1 0 0 | 27.345 |
| 35 | 0 1 1 0 1 0 1 | 27.355 |
| 36 | 0 1 1 0 1 1 0 | 27.365 |
| 37 | 0 1 1 0 1 1 1 | 27.375 |
| 38 | 0 1 1 1 0 0 0 | 27.385 |
| 39 | 0 1 1 1 0 0 1 | 27.395 |
| 40 | 1 0 0 0 0 0 0 | 27.405 |

*Table 2 SP8923/1 O/P frequencies with 10.240 crystal (0 contact open, 1 contact closed to VCC)*

| R/T 1 | R/T 2 | Offset |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | –455kHz |
| 0 | 1 | –10.240MHz |
| 1 | 1 | –10.695MHz |

*Table 3 Receive/Transmit truth table*

## SP8921 CRYSTAL OSCILLATOR PERFORMANCE

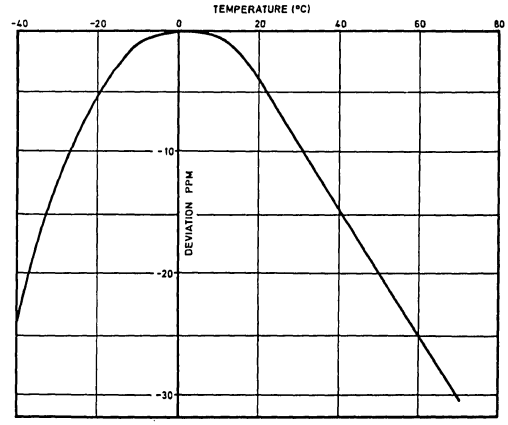



*Fig. 5 Frequency/temperature characteristics of CB 10.24 MHz crystal oscillator*

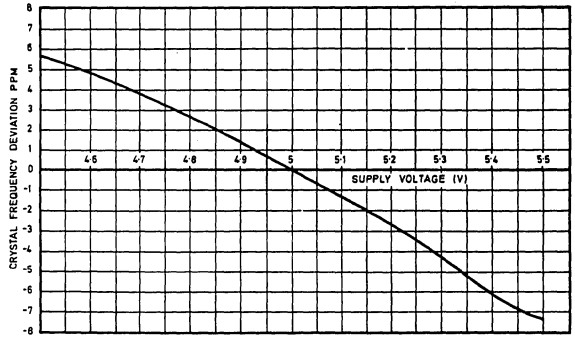



*Fig. 6 Crystal frequency v. supply voltage*

## CHARGE PUMP FILTER ARRANGEMENTS (FIGS.7 THROUGH 10)

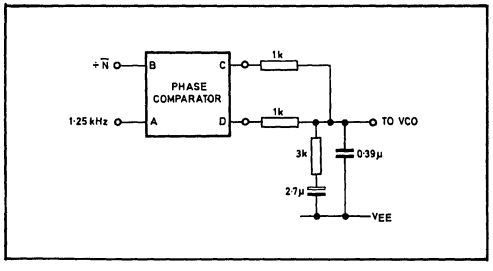



*Fig. 7 Filter A. Simple voltage pump, output range 2.5V*

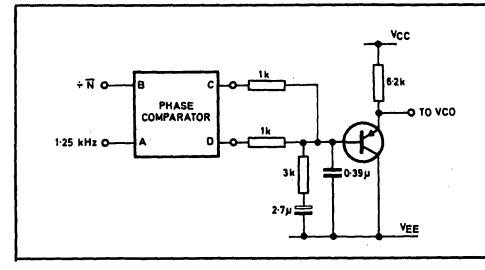



*Fig. 8 Filter B. Simple voltage pump with buffered output*

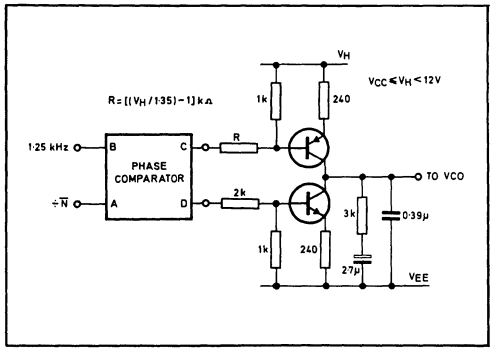



*Fig. 9 Filter C. Current pump, output voltage range $V_H - 1.5V$ for $V_H$ less than 12V*

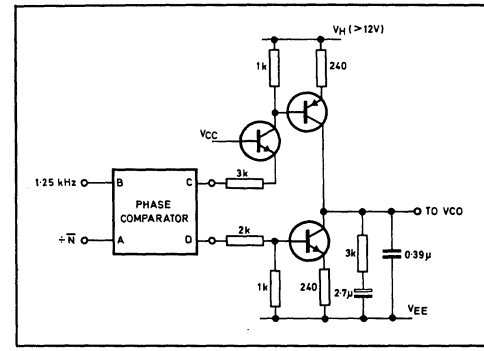



*Fig. 10 Filter D. Current pump output voltage range $V_H - 1.5V$ for $V_H$ greater than 12V*

## INPUT/OUTPUT CIRCUITS (FIGS. 11 THROUGH 16)

The following diagrams show input and output circuit configurations used on the SP8921, 2 and 3.

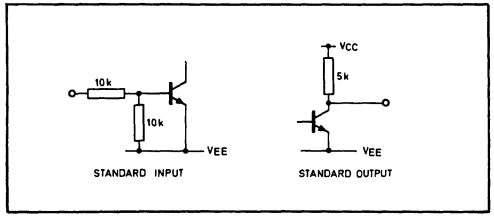



*Fig. 11 Standard input and output*

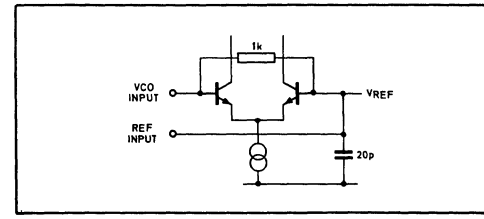



*Fig. 12 VCO input*

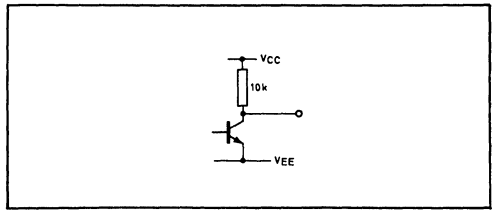



*Fig. 13 Lock detect output*

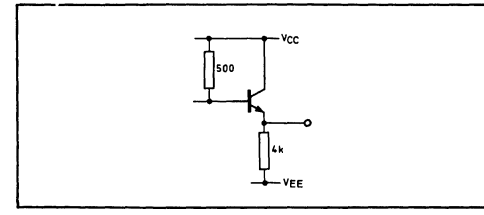



*Fig. 14 10.24 MHz output*

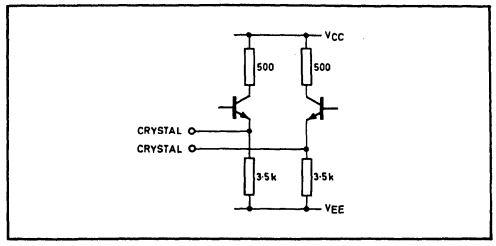



*Fig. 15 Crystal oscillator inputs*

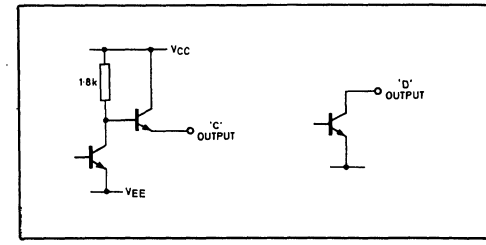



*Fig. 16 Phase/frequency comparator outputs*

## FURTHER APPLICATIONS

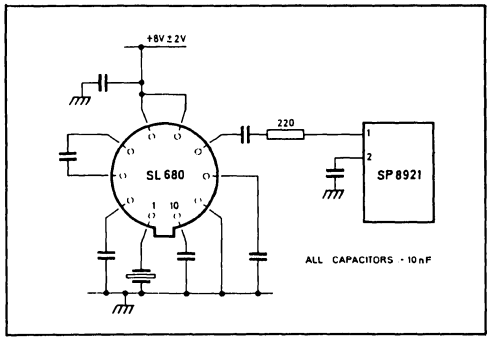



*Fig. 17 High stability crystal reference oscillator using SL680*

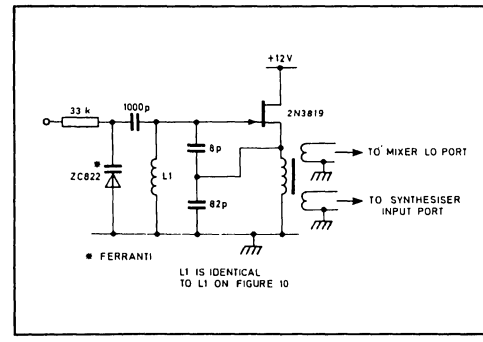



*Fig. 18 Voltage controlled oscillator for 27MHz CB synthesiser*

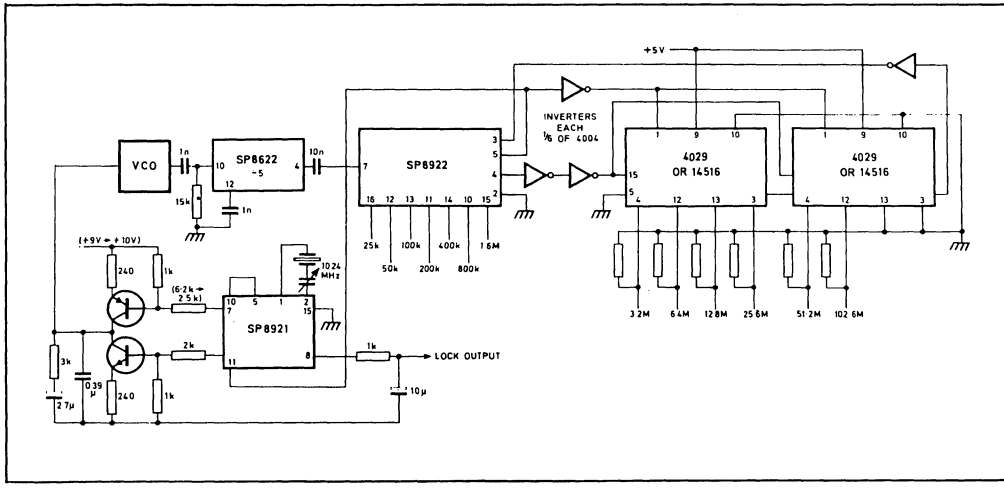



*Fig. 19 200 MHz general purpose binary programmed synthesiser with 25KHz resolution using SP8921/22*

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# MN9102

## NON-VOLATILE QUAD LATCH

The Plessey MN9102 is a non-volatile 4-bit data latch which uses MNOS transistors as memory elements to retain stored data in the absence of applied power. The data that is applied to the four inputs is written into the memory when the $\overline{SAVE}$ control is taken to a logic '0' level and the data subsequently appears on the four outputs. The stored data is also automatically restored to the outputs whenever power is re-applied to the device.

An OUTPUT ENABLE is also available, which when taken to logic '0' level presents a high impedance state on each data output line, permitting multiplexed operation.

The high voltage usually associated with MNOS memory devices is generated internally, requiring only a single external capacitor to act as a charge reservoir for supplying current when writing into the memory. The device therefore operates from standard voltage rails and requires no additional drive circuitry.

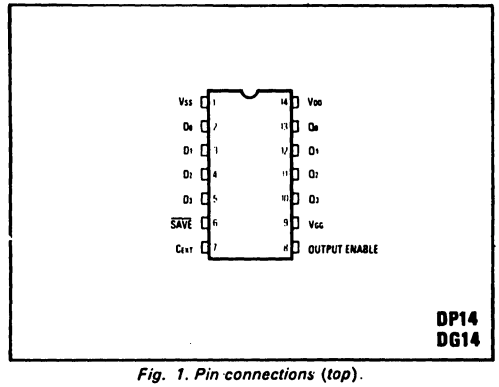


*Fig. 1. Pin connections (top).*

### FEATURES

- Data Retention for One Year at 70°C in the Absence of Applied Power
- Simple to Use
- Standard Power Supplies Only (+5V, −12V)
- CMOS/TTL Compatible
- 14-lead DIL Package

### APPLICATIONS

- Metering Systems
- Elapsed Time Indicators
- Security Code Storage
- Last Channel Memory for Digital Tuning

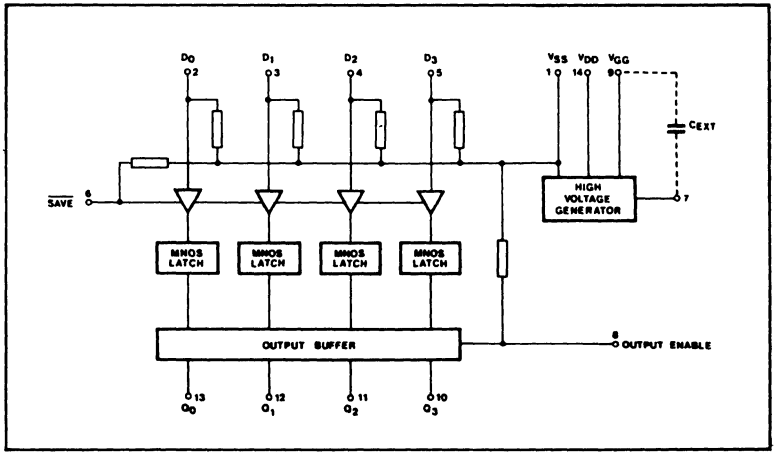


*Fig. 2 Block diagram of MN9102*

## ELECTRICAL CHARACTERISTICS

**Operating conditions (unless otherwise stated):**

$V_{SS}$ = + 5V ± 5%
$V_{DD}$ = 0V
$V_{GG}$ = —12V ± 5%
Output loading = 1 TTL load
Ambient operating temperature range including data retention in the absence of applied power: —40°C to + 85°C

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Logic '0' input voltage | $V_{IL}$ | | | 0.8 | V | Nominal 20k ohms internal pullup |
| Logic '1' input voltage | $V_{IH}$ | $V_{SS}$–1 | | | V | resistor to $V_{SS}$ on all inputs |
| Logic '0' output voltage | $V_{OL}$ | | | 0.4 | V | Output current = 1.6mA |
| Logic '1' output voltage | $V_{OH}$ | $V_{SS}$—1 | | | V | Output current = —100 µA |
| Output leakage current | | —10 | | +10 | µA | $V_{SS} \geqslant V_{OUT} \geqslant V_{DD}$ with OUTPUT ENABLE = $V_{DD}$ |
| External reservoir capacitance | $C_{EXT}$ | 100 | | 220 | nF | } See note 2 |
| Output voltage on $C_{EXT}$ | | | —38 | | V | |
| External leakage on $C_{EXT}$ | | | | 2.0 | µA | |
| Data set-up time | $t_s$ | 1 | | | µs | |
| Data hold time | $t_h$ | 1 | | | µs | |
| Data settling time | $t_d$ | | | 7 | µs | $C_{LOAD}$ = 47pf |
| Output enable delay | $t_o$ | | | 2.5 | µs | $C_{LOAD}$ = 47pf |
| SAVE time | $t_{SAVE}$ | 10 | | | ms | See note 1 |
| SAVE duty cycle | | | | 10 | % | See note 2 |
| SAVE cycles | | $10^6$ | | | | See note 4 |
| SAVE rise and fall times | $t_e$ | | | 10 | µs | |
| Data retention time | | 12 | | | months | $T_{amb}$ = —40°C to 70°C |
| | | 3 | | | months | $T_{amb}$ = —40°C to 85°C |
| Power dissipation | | | 50 | 100 | mW | See note 3 |

## ABSOLUTE MAXIMUM RATINGS

(all voltages with respect to $V_{SS}$)

Voltage on $C_{EXT}$ —46 to + 0.3V
Voltage on $V_{GG}$ —20 to + 0.3V
Voltage on any other pin —7 to + 0.3V
Storage temperature —55°C to + 125°C
Ambient operating temperature —40°C to + 85°C

The above limits are absolute limiting values beyond which the lifetime and performance of the device may be impaired. No guarantee is implied that the device will function at any condition other than specified under the operating conditions.

## OPERATING NOTES

1.
Data can be entered into the latch with SAVE times much less than ten milliseconds, however the retention time is then significantly reduced. It is therefore important that spurious SAVE pulses do not occur, particularly when power is applied to the device.

2.
An external capacitor is required to act as a charge reservoir for the high voltage which is generated on chip from a high impedance source. Excessive external leakage current on this capacitor or exceeding the quoted duty cycle can cause appreciable loading of the high voltage resulting in reduced data retention times. If operation outside of these limits is required, then an external high voltage (—38 volts ± 5%) may be used to maintain the voltage level.

3.
The majority of the power dissipation arises from the current flow between $V_{SS}$ and $V_{GG}$. The current level on $V_{DD}$ is the sum of the logic '0' level current plus leakage currents.

4.
Exceeding this number of SAVE cycles can cause permanent damage to the device. It should also be noted that rapid changes of data in excess of $10^6$ may cause a reduction in the data retention time.

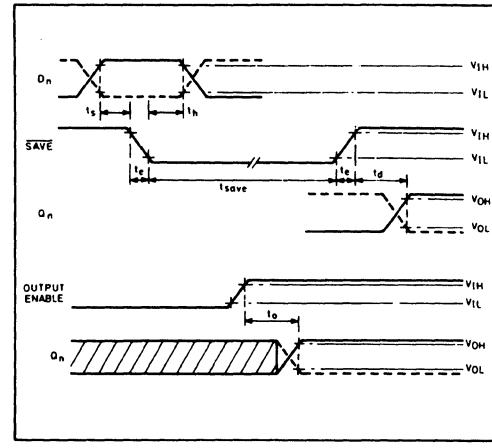


*Fig. 3 Timing diagram*

## ANTI-STATIC PRECAUTIONS

All inputs have suitable protection devices to minimise the possibility of damage due to static discharge. Care should still be taken when handling the device and the leads should at all times be shorted together until actually incorporated in the circuit in which the device is being used. Care should be taken to avoid static charges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

To ensure no damage occurs during transit, the devices are supplied packed in conducting foam or other suitable carriers.

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# MN9105

## QUAD DECADE UP/DOWN COUNTER

The Plessey MN9105 is a 4-decade BCD counter which counts up or down on negative transitions of the CLOCK input. In parallel with the counter is a 16-bit non-volatile MNOS memory into which the contents of the counter can be written by holding CLOCK low and then taking SAVE to a low level. When data has been written into the memory, it can be retained even in the absence of applied power, and then subsequently be recalled from the memory to preset the counter.

Also associated with each counter decade is a 4-bit latch, the outputs of which follow the count sequence when LOAD is low. When LOAD goes high, the latches retain the data present at the time of the transition. The outputs from each latch are multiplexed onto a 4-bit data highway under the control of a 2-bit address (MX1, MX2). All four outputs may be put into a high output impedance state by holding OUTPUT ENABLE high, so allowing multiplexed operation between devices.

The final decade has a CARRY output to enable devices to be cascaded in series. An input CLOCK pulse ripples through to the CARRY output when the counter is in the 'up' mode and the '9999' state or when in the 'down' mode and the '0000' state.

The high voltage usually associated with MNOS devices is generated internally, requiring only a single capacitor to act as a charge reservoir for supplying current when writing into the memory. The device therefore operates from standard voltage rails and requires no additional drive circuitry.

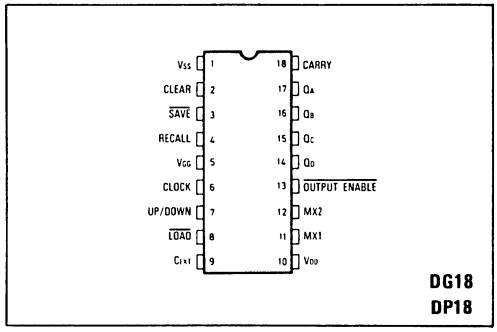



*Fig. 1 Pin connections (top)*

## FEATURES

- Data Retention for One Year at 70°C in the Absence of Applied Power
- DC to 250 kHz Count Frequency
- Up/Down Count Facilities
- Standard Power Supplies (+5V, −12V)
- TTL/CMOS Compatibility
- 18-pin DIL Package

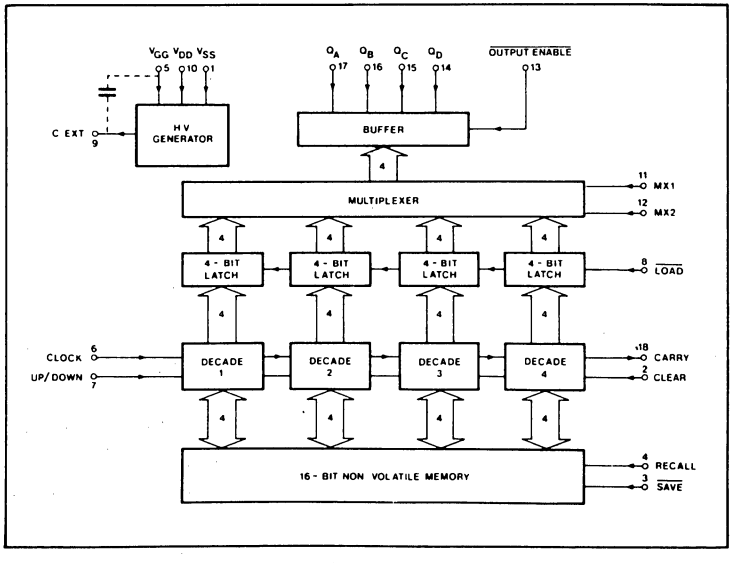



*Fig. 2 MN9105 block diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$V_{SS}$ = + 5V ± 5%
$V_{DD}$ = 0V
$V_{GG}$ = −12V ± 5%
Output loading 1 TTL load
Ambient operating temperature range including data retention
in the absence of applied power: −40°C to 85°C

| Characteristic | Symbol | Value Min. | Value Typ. | Value Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Logic '0' input voltage | $V_{IL}$ | | | 0.8 | V | |
| Logic '1' input voltage | $V_{IH}$ | $V_{SS}$−1 | | | V | |
| Logic '0' output voltage | $V_{OL}$ | | | 0.4 | V | Output current = 1.6mA |
| Logic '1' output voltage | $V_{OH}$ | $V_{SS}$−1 | | | V | Output current = −100µA |
| Output leakage current | | −10 | | ±10 | µA | $V_{SS} > V_{OUT} > V_{DD}$ with OUTPUT ENABLE = $V_{SS}$ |
| External capacitor | $C_{EXT}$ | 0.1 | | 0.22 | µF | |
| Output voltage on $C_{EXT}$ | | | −38 | | V | |
| External leakage on $C_{EXT}$ | | | | 2.0 | µA | See Note 3 |
| SAVE duty cycle | | | | 10 | % | |
| SAVE cycles | | $10^6$ | | | | See Note 2 |
| Data retention time | | 12 | | | months | $T_{amb}$ = −40°C to 70°C |
| | | 3 | | | months | $T_{amb}$ = −40°C to 85°C |
| Total integrated RECALL time between SAVE cycles | | $10^6$ | | | secs | |
| Power dissipation | | | 250 | 500 | mW | See Note 1 |

## OPERATING NOTES

1. The majority of the power dissipation arises from current flow between $V_{SS}$ and $V_{GG}$. The current level on $V_{DD}$ is the sum of the logic '0' level currents plus leakage current only.
2. Exceeding this number of SAVE cycles can cause permanent damage to the device. It should also be noted that rapid changes of data in excess of $10^6$ may cause a reduction in the data retention time.
3. An external capacitor is required to act as a charge reservoir for the high voltage which is generated on-chip from a high impedance source. Excessive external leakage on this capacitor or exceeding the quoted duty cycle can cause appreciable loading of the high voltage resulting in reduced data retention times. If operation outside these limits is required then an external high voltage (−38 volts 5%) may be used to maintain the voltage level.
4. The CARRY pulse is equivalent to a CLOCK pulse which ripples through the counter when in the correct count sequence. For CLOCK pulse widths greater than or equal to 5 µs, the CARRY output may be connected directly to the input of a following device. For smaller widths, then pulse stretching must be used on the CARRY output to maintain the pulse width.
5. Data can be entered into the memory with SAVE times much less than 10 milliseconds; however the data retention time is then significantly reduced. It is therefore important that spurious SAVE pulses do not occur particularly when power is applied to the device.

| MX2 | MX1 | $\overline{OE}$ | $Q_D$, $Q_C$, $Q_B$, $Q_A$ |
|---|---|---|---|
| * | * | 1 | High output impedance |
| 0 | 0 | 0 | Decade 1 |
| 0 | 1 | 0 | Decade 2 |
| 1 | 0 | 0 | Decade 3 |
| 1 | 1 | 0 | Decade 4 |

| $\overline{SAVE}$ | CLOCK | CLEAR | RECALL | UP/DOWN | MODE |
|---|---|---|---|---|---|
| 1 | ↓ | 0 | 0 | 0 | Count up |
| 1 | ↓ | 0 | 0 | 1 | Count down |
| 1 | * | ↓ | 0 | * | Set counter to 0000 |
| 1 | * | 0 | ↓ | * | Preset counter from memory |
| 0 | 0 | 0 | 0 | * | Write into memory |

* Logic '0' or '1' level
↓ Logic '1' to '0' transition

*Table 1 Function table*

## ABSOLUTE MAXIMUM RATINGS

(all voltage with respect to $V_{SS}$)

Voltage on $C_{EXT}$ −46 to + 0.3V
Voltage on $V_{GG}$ −20 to + 0.3V
Voltage on any other pin −7 to + 0.3V
Storage temperature −55 C to + 125 C
Ambient operating temperature −40 C to + 85 C

**The above limits are absolute limiting values beyond which the lifetime and performance of the device may be impaired. No guarantee is implied that the device will function at any condition other than specified under the operating conditions.**

## ANTI-STATIC PRECAUTIONS

All inputs have suitable protection devices to minimise the possibility of damage due to static discharge. Care should still be taken when handling the device and the leads should at all times be shorted together until actually incorporated in the circuit in which the device is being used. Care should be taken to avoid static charges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

To ensure no damage occurs during transit, the devices are supplied packed in conducting foam or other suitable carriers.

## SWITCHING CHARACTERISTICS

Loading = 1TTL LOAD

$C_L = 10pF$

| Parameter | Symbol | Value | | | Units | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock Frequency | | | | 250 | KHz | |
| Up/Down select time | $t_s$ | 1 | | | µs | |
| Clock pulse width | $t_p$ | 2 | | | µs | |
| Clear pulse width | $t_c$ | 1 | | | µs | |
| Recall pulse width | $t_r$ | 2 | | | µs | |
| Save pulse width | $t_{save}$ | 10 | | | ms | Note 5 |
| Clear to clock set up time | $t_{cp}$ | 2 | | | µs | |
| Recall to clock set up time | $t_{rp}$ | 2 | | | µs | |
| Clock to load set up time | $t_{pl}$ | 2 | | | µs | |
| Clock to save set up time | $t_{ps}$ | 0 | | | µs | |
| Clear to output delay | $t_{cd}$ | | | 2 | µs | |
| Recall to output delay | $t_{rd}$ | | | 4 | µs | |
| Clock to output delay | $t_{pd}$ | | | 4 | µs | |
| MX1/MX2 to output delay | $t_{md}$ | | | 4 | µs | |
| Load to output delay | $t_{ld}$ | | | 4 | µs | |
| Clock to carry output delay | $t_{pc}$ | | | 4 | µs | |
| Carry output width | $t_{cry}$ | 2 | | | µs | $t_p$ = 5µs (Note 4) |
| Input rise and fall times | | | | 10 | µs | |

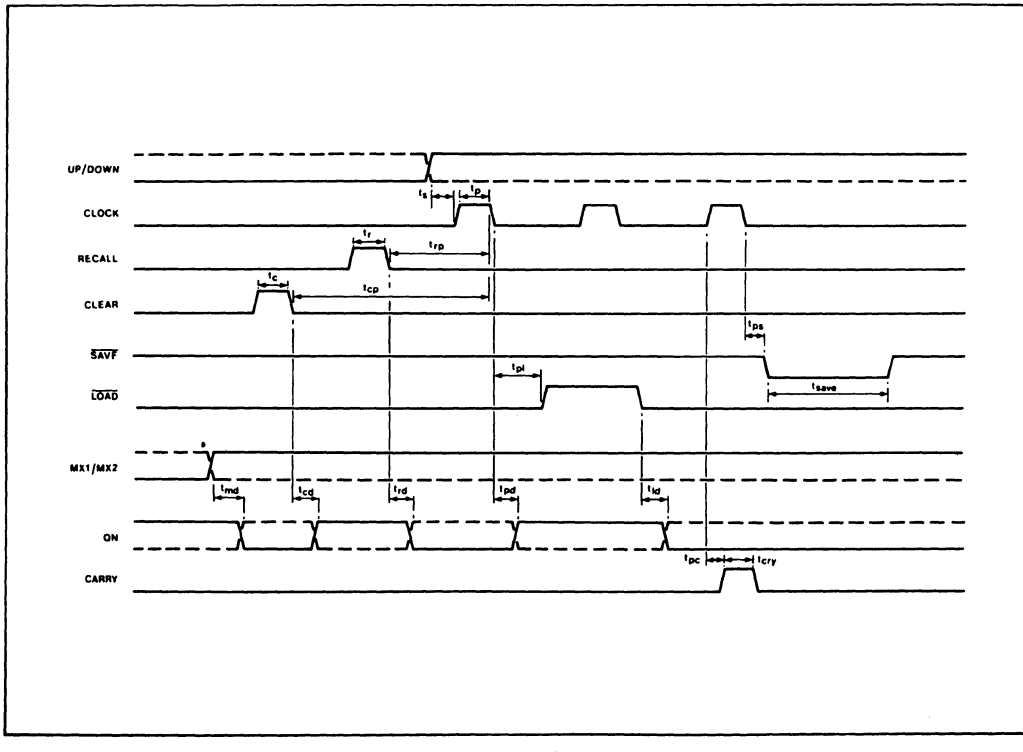



*Fig. 3 Timing diagram*

# MN9106/7/8

## SIX-DECADE UP COUNTERS

The MN9106 is a six decade up counter in parallel with a twenty four bit MNOS memory which can provide non-volatile data storage of the current count position. An overflow latch and memory bit are also available to indicate a counter overflow condition. In addition to the conventional counter controls, RECALL and $\overline{\text{SAVE}}$ inputs are provided to control the two way transfer of data between the counter and memory.

Output data is presented in the form of multiplexed seven segment outputs and six digit strobes. The multiplexing sequence is controlled by an internal oscillator which may also be forced from an external oscillator on the SCAN input. The device operates from a single 12 volts supply and the higher voltage required for the MNOS memory is provided internally by a generator which requires only a single external capacitor.

The MN9107 and MN9108 are adaptations of the basic device intended specifically for timer applications. Certain decades in these devices have been replaced with divide-by six elements to give the facility of counting hours, minutes and seconds when provided with the correct input frequency.

MN9107 99 hours, 59 minutes, 59 seconds
MN9108 9999 hours, 59 minutes
or 9999 minutes, 59 seconds

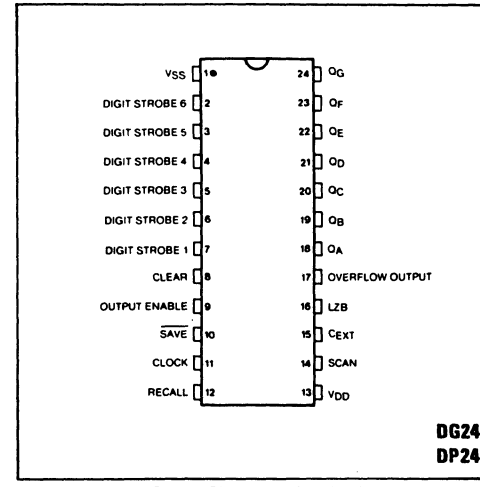



*Fig. 1 Pin connections (top)*

### FEATURES

- Data Retention Guaranteed For One Year In The Absence of Applied Power over Temperature Range of −40°C to +70°C
- DC to 200kHz Count Frequency
- Operation From Single 12V Supply with CMOS Compatible Inputs
- Leading Zero and Full Blanking Facilities
- Multiplexed Seven-Segment Outputs
- Counter Overflow Indicator
- Self Scanning Multiplexing
- Operation from Split Supplies (+5. −7V) Allowing Inputs to Interface with TTL
- Data SAVE Time of 10 Milliseconds.

### ABSOLUTE MAXIMUM RATINGS

(all voltages with respect to Vss)

Voltage on $C_{EXT}$ −46V to + 0.3V
Voltage on any other pin −15V to + 0.3V
Storage temperature −55°C to + 125°C
Ambient operating temperature −40°C to + 85°C

The above limits are absolute limiting values beyond which the lifetime and performance of the device may be impaired. No guarantee is implied that the device will function at any condition other than specified under the operating conditions.

### ANTI-STATIC PRECAUTIONS

All inputs have suitable protection devices to minimise the possibility of damage due to static discharge. Care should be taken when handling the device and the leads should at all times be shorted together until actually incorporated in the circuit in which the device is being used. Care should be taken to avoid static charges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

To ensure no damage occurs during transit, the devices are supplied packed in conducting foam or other suitable carriers.

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{Amb}$ −40°C to +85°C

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Supply voltage | $V_{DD}$ | $V_{SS}$ 13 | | $V_{SS}$ 11 | V | |
| Supply current | $I_{DD}$ | 6 | | 22 | mA | OUTPUT ENABLE = $V_{IL}$ SCAN = open circuit |
| Logic '0' input voltage | $V_{IL}$ | | | $V_{SS}$ 4 | V | |
| Logic "1" input voltage | $V_{IH}$ | $V_{SS}$ 1 | | | V | |
| Input leakage current | | −1 | | +1 | µA | $V_{DD} \leq V_{IN} \leq V_{SS}$ (Except SCAN input) |
| Scan input current (Logic '0') | | −12 | | | mA | $V_{IN} = V_{SS} - 6$ |
| Scan input current (Logic '1') | | | | +120 | µA | $V_{IN} = V_{SS} - 1$ |
| Logic '1' output resistance - segments | | | 150 | 300 | Ω | $V_{OUT} = V_{SS} - 3$ |
| Logic '1' output resistance - overflow | | | 150 | 300 | Ω | $V_{OUT} = V_{SS} - 3$ |
| Logic '1' output resistance digit strobes | | | 500 | 1000 | Ω | $V_{OUT} = V_{SS} - 3$ |
| Logic '0' output leakage current | | −10 | | +1 | µA | $V_{DD} \leq V_{OUT} \leq V_{SS}$ |
| Output loading - segments | | | | 15 | mA | See note 3 |
| Output loading - overflow | | | | 15 | mA | |
| Output loading - digit strobes | | | | 5 | mA | |
| High voltage output | | | $V_{SS}$-40 | | V | |
| External reservoir capacitance | $C_{EXT}$ | 100 | | 220 | nF | |
| External leakage current on $C_{EXT}$ | | | | 2.0 | µA | See note 3 |
| Save duty cycle | | | | 5 | % | |
| Number of save cycles | | $10^6$ | | | | See note 4 |
| Data retention time | | 12 | | | Months | $T_A$ = 70°C |
| Data retention time | | 3 | | | Months | $T_A$ = 85°C |
| Total integrated RECALL time between SAVE cycles | | $10^5$ | | | secs | |
| Count frequency | f | | | 200 | kHz | |
| Clock width | | 2.5 | | | µs | See note 2 |
| Recall width | | 5 | | | µs | See note 2 |
| Clear width | | 5 | | | µs | See note 2 |
| Save width | | 10 | | | ms | See notes 2 and 5 |
| Input rise and fall times | | | | 10 | µs | |
| Internal scan frequency | | | 1 | | kHz | SCAN capacitance = 100nF |
| External scan frequency | | | | 25 | kHz | |

| Output Enable | Count Position | $Q_A$ | $Q_B$ | $Q_C$ | $Q_D$ | $Q_E$ | $Q_F$ | $Q_G$ |
|---|---|---|---|---|---|---|---|---|
| 0 | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 2 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 3 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 4 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 5 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 6 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 7 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 9 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | Invalid† | 0 | 1 | 1 | 1 | 1 | 1 | 0 |

*Table 1 — Output function table*

Segment identification

* Don't care condition
† Incorrect use of the device may cause invalid BCD characters to appear in the counter.

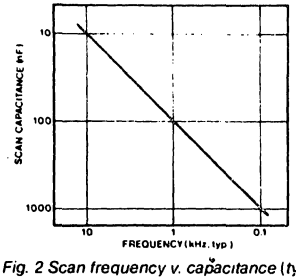


*Fig. 2 Scan frequency v. capacitance (typical)*

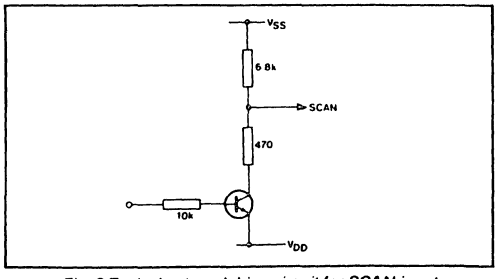


*Fig. 3 Typical external drive circuit for SCAN input*

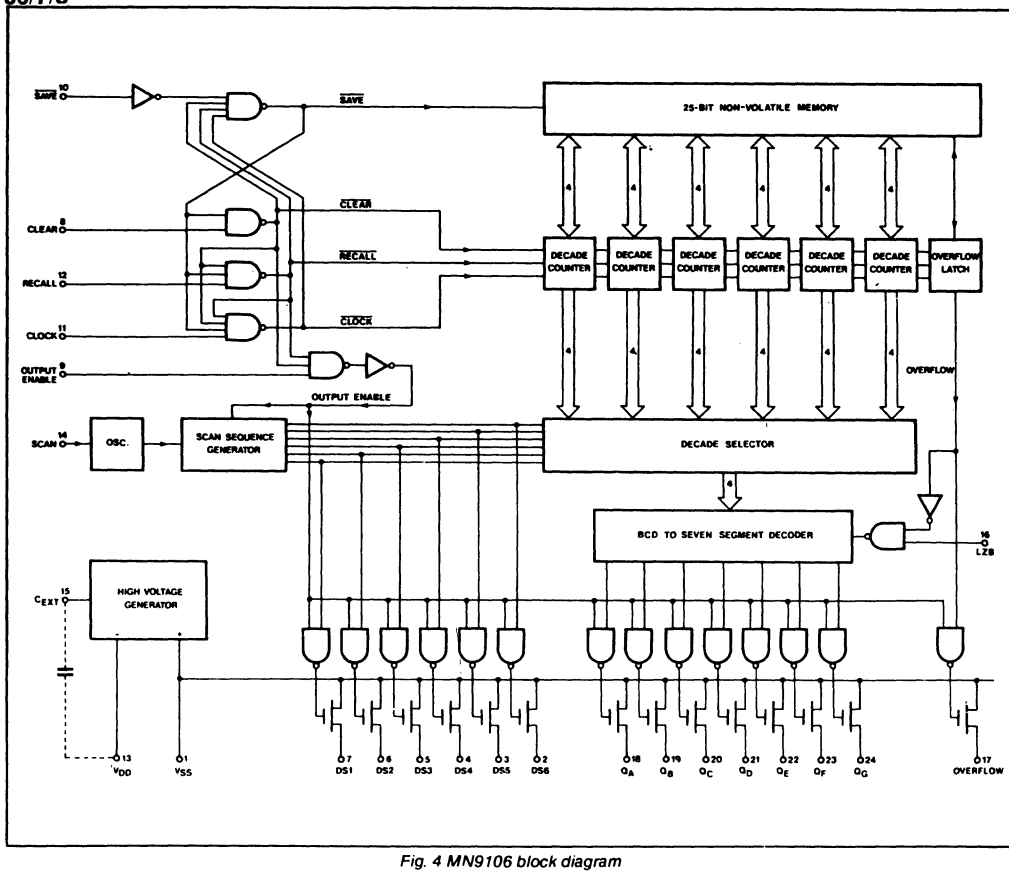



*Fig. 4 MN9106 block diagram*

## OPERATING NOTES

1. The counter is a synchronous six decade counter multiplexed onto a four bit data highway and then decoded into seven segment format which drives open drain MOS transistors. An additional output transistor is also driven directly from the overflow latch.
Multiplexing is provided internally from an oscillator whose frequency is determined by a capacitor between the SCAN input and $V_{SS}$ (Fig.2). This oscillator may also be forced externally from a signal which must be capable of sinking and sourcing current on the SCAN input (Fig.3). The decoded data and the corresponding digit strobe output are available for an entire oscillator period and the multiplex control scans the decades in sequence from most significant (DS6) to least significant (DS1). The scan position changes on negative transitions of the SCAN input.
With OUTPUT ENABLE held at a low level, the blanking facility turns off the segment outputs, the digit strobe outputs and the overflow output. The multiplexing scan sequence is reset to the most significant decade at this time A similar blanking and reset function also occurs whenever the device is put into recall or clear modes.
With LZB at a high level, leading zeros are blanked provided that the overflow latch is not at a high level. Leading zero blanking is not applicable to the MN9107 and applies only to three most significant decades in the MN9108.

2. Clear mode:— In clear mode the counter and overflow latch are reset to zero, all outputs are turned off and the multiplexing sequence is reset. The device is put into clear mode by taking CLEAR to a high level while $\overline{SAVE}$ is also held high. Once the clear function has begun, any subsequent changes on the $\overline{SAVE}$ input are inhibited. RECALL and CLOCK inputs are always inhibited when the CLEAR input is high.
Recall mode:— In recall mode the counter and overflow latch are preset from the memory, all outputs are turned off and the multiplexing sequence is reset. The device is put into recall mode by taking RECALL to a high level while CLEAR is low and $\overline{SAVE}$ is high. Once the recall function has begun, any subsequent changes on the $\overline{SAVE}$ input are inhibited. The CLOCK input is always inhibited when the RECALL input is high.
Count mode:— In count mode the counter will increment on negative transitions of the clock input. If the counter is in the "999999" state, the next counting edge will set the overflow latch to a high level and counting will begin again at "000000". The device is in count mode when RECALL and CLEAR are at a low level and $\overline{SAVE}$ is high. However, once the CLOCK input has been taken high, any subsequent changes on the $\overline{SAVE}$ input are inhibited until the CLOCK returns to a low level.

Save mode:— In save mode the data in the counter and overflow latch is written into the non-volatile memory. The device is put into save mode by taking $\overline{SAVE}$ to a low level while all other inputs are at a low level. Once the save function has begun, any subsequent changes on the other inputs are inhibited until $\overline{SAVE}$ returns to a high level.

| | Clock | Recall | Clear | $\overline{SAVE}$ |
|---|---|---|---|---|
| Clear mode | * | * | 1 | 1† |
| Recall mode | * | 1 | 0 | 1† |
| Count mode | 1 | 0 | 0 | 1† |
| Save mode | 0† | 0† | 0† | 0 |

*TABLE 2. Control Truth Table*

* Don't care condition.
† These conditions need only apply to enter the specified mode, once this has happened, changes on these inputs are inhibited internally until that particular mode is completed. Should the $\overline{SAVE}$ input be taken to a low level simultaneously with any other input going high, then a race condition will exist and although it is not possible to predict which mode will be entered, the device will not malfunction. The device may switch directly from one operating mode to another provided the minimum mode times are maintained. These features mean that no external synchronisation is required between the $\overline{SAVE}$ and other inputs and ensures that valid data is present before saving and that the data is fixed during the save period.
3. The high voltage for the memory is generated internally from a high impedance source and an external capacitor is needed on $C_{EXT}$ to provide a charge reservoir. Exceeding the save duty cycle or excessive external leakage from $C_{EXT}$ may cause appreciable loading of this high voltage resulting in reduced data retention. Should it be required to operate outside the specified limits then an external voltage supply may be used to maintain the high voltage level.
4. Exceeding the specified number of save cycles may cause a reduction in data retention time and eventually the device may suffer permanent damage.
5. Data can be entered into the memory with save times much less than ten milliseconds, however, the retention time is then significantly reduced. It is therefore important that spurious save pulses do not occur which could disturb or corrupt the stored data. This is most likely to occur at power on and power off. To eliminate this possibility it is sufficient to ensure that the $\overline{SAVE}$ input remains within one volt of $V_{SS}$ at all times except during valid save periods.
6. Current limiting resistors should always be included on all outputs to prevent excessive output current.

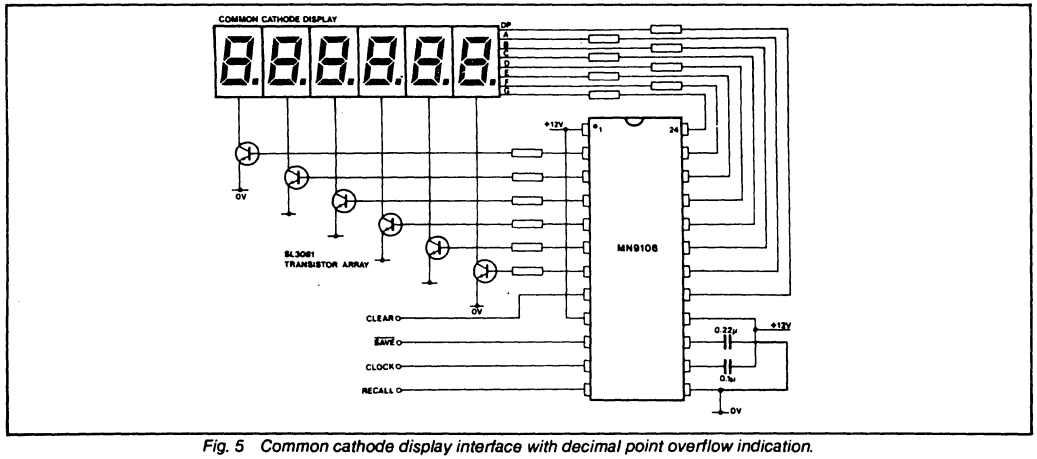
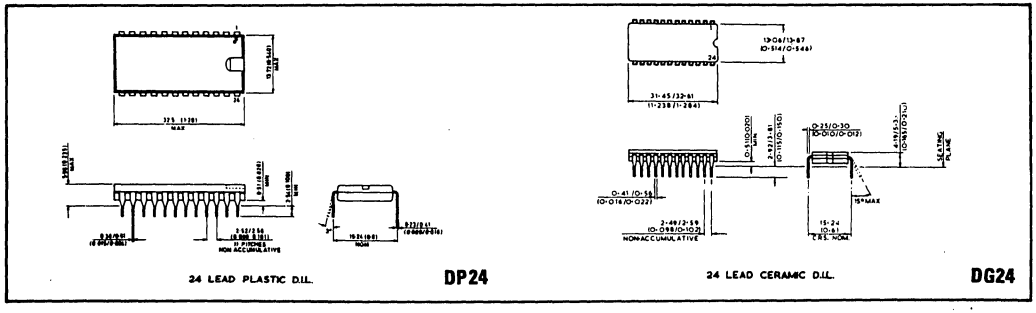



*Fig. 5 Common cathode display interface with decimal point overflow indication.*

## PACKAGE DETAILS

Dimensions are shown thus: mm (in)



PLESSEY
Semiconductors

NOVOL
NON-VOLATILE LOGIC

# MN9210

## 256 BIT MEMORY (64 x 4)

The Plessey MN9210 is a 64-word by 4-bit electrically alterable non-volatile memory, fabricated using MNOS technology. The device operates from power supplies of +5V and -12V and a low current programming supply of -39V.

Data input and output is multiplexed internally for common I/O bus compatibility. Latches are provided for address and I/O data allowing efficient interfacing. For ease of system expansion, two CHIP SELECT inputs are provided. If either or both are held high, the data lines are forced into a high impedance state and Read, Erase and Write functions are inhibited.

With the READ/WRITE input high, when STROBE is taken high, data from the addressed word is latched and is then subsequently available as output data when STROBE returns to the low level (Fig.3).

Any word may be independently reprogrammed by executing an erase-write cycle, initiated on the falling edge of READ/WRITE. This transition latches the input address and forces the data lines into a high impedance state.

When STROBE is taken high the addressed word is erased and the data latch enabled. When STROBE returns low the write data now present on the data lines is latched and written into the addressed word. When READ/WRITE returns high the write operation is terminated and the written data appears as output data (Fig.4). Alternatively the write operation may be terminated by taking either or both CHIP SELECT inputs high.

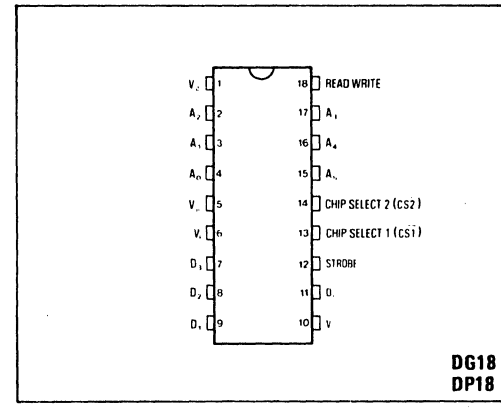



*Fig.1 Pin connections (top view)*

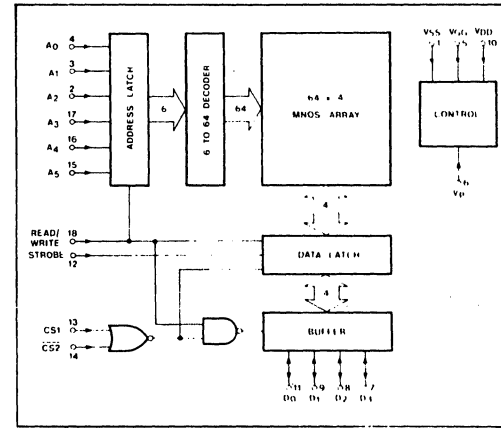



*Fig.2 MN9210 block diagram*

### FEATURES

- Guaranteed Data Retention of One Year in the Absence of Applied Power over Temperature Range of -40°C to +70°C
- Latching Data and Address Inputs
- Three-state Outputs on Data Lines
- TTL/CMOS Compatibility
- Single Word Preprogramming Facilities
- 18-pin DIL Package

### ABSOLUTE MAXIMUM RATINGS (all voltages with respect to $V_{SS}$)

Voltage on $V_P$ -47V to +0.3V
Voltage on $V_{GG}$ -20V to +0.3V
Voltage on any other pin -7V to +0.3V
Storage temperature -55°C to +125°C
Ambient operating temperature -40°C to +85°C

The above limits are absolute limiting values beyond which the lifetime and performance of the device may be impaired. No guarantee is implied that the device will function at any condition other than specified under the operating conditions.

### ANTI-STATIC PRECAUTIONS

All inputs have suitable protection devices to minimise the possibility of damage due to static discharge. Care should still be taken when handling the device and the leads should at all times be shorted together until actually incorporated in the circuit in which the device is being used. Care should be taken to avoid static charges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

To ensure no damage occurs during transit, the devices are supplied packed in conducting foam or other suitable carriers.

## ELECTRICAL CHARACTERISTICS

**Operating conditions (unless otherwise stated)**
$V_{SS} = +5V \pm 5\%$
$V_{DD} = 0V$
$V_{GG} = -12V \pm 5\%$
Ambient operating temperature range -40°C to +85°C

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| **DC Characteristics** | | | | | | |
| Logic '0' input voltage | $V_{IL}$ | | | 0.8 | V | |
| Logic '1' input voltage | $V_{IH}$ | $V_{SS}-1$ | | | V | |
| Logic '0' output voltage | $V_{OL}$ | | | 0.4 | V | $I_{OUT} = +1.6mA$ |
| Logic '1' output voltage | $V_{OH}$ | $V_{SS}-1$ | | | V | $I_{OUT} = -100\mu A$ |
| High output impedance leakage current | | -10 | | +10 | $\mu A$ | $V_{DD} \leqslant V_{OUT} \leqslant V_{SS}$ |
| Power dissipation | | | | 450 | mW | Note 1 |
| Non volatile data retention time | | 12 | | | months | $T_{amb} = 70°C$ |
| | | 3 | | | months | $T_{amb} = 85°C$ |
| Programming voltage | $V_P$ | -41 | | -37 | V | Note 4 |
| $V_P$ supply current averaged over a single write period | $I_P$ | -350 | | | $\mu A$ | $V_P = -37V$ |
| $V_P$ supply current at all other times | $I_P$ | -120 | | | $\mu A$ | $V_P = -37V$ |
| **Read Characteristics (Fig.3)** | | | | | | |
| Chip select set-up time | $t_{RCS}$ | 7.5 | | | $\mu s$ | |
| Address set-up time | $t_{RAS}$ | 7.5 | | | $\mu s$ | |
| Strobe width | $t_{RS}$ | 5 | | 100 | $\mu s$ | |
| Address hold time | $t_{RAH}$ | 0 | | | | |
| Chip select to output delay | $t_{CO}$ | | | 2.5 | $\mu s$ | Output Loading |
| Strobe to output delay | $t_{RO}$ | | | 2.5 | $\mu s$ | 1 TTL load +50pF |
| Strobe rise and fall times | | | | 5 | $\mu s$ | |
| Number of read cycles on any one word | | $10^9$ | | | | Note 2 |
| **Erase-Write Characteristics (Fig.4)** | | | | | | |
| Chip select set-up time | $t_{PCS}$ | 0 | | | | |
| Address set-up time | $t_{PAS}$ | 2.5 | | | $\mu s$ | |
| Address hold time | $t_{PAH}$ | 2.5 | | | $\mu s$ | |
| Strobe delay | $t_D$ | 0 | | | | |
| Erase width | $t_{ERASE}$ | 10 | | | ms | |
| Write width | $t_{WRITE}$ | 10 | | | ms | |
| Data set up time | $t_{DS}$ | 2.5 | | | $\mu s$ | |
| Data hold time | $t_{DH}$ | 2.5 | | | $\mu s$ | |
| Strobe rise and fall times | | | | 5 | $\mu s$ | |
| Number of erase/write cycles on any one word | | $10^6$ | | | | Note 3 |

| $\overline{CS1}$ | $\overline{CS2}$ | READ/$\overline{WRITE}$ | STROBE | MODE | |
|---|---|---|---|---|---|
| 1 | X | X | X | NOT SELECT | ** |
| X | 1 | X | X | NOT SELECT | ** |
| 0 | 0 | 1 | 0 | STANDBY | * |
| 0 | 0 | 1 | 1 | READ | * |
| 0 | 0 | 0 | 1 | ERASE | ** |
| 0 | 0 | 0 | 0 | WRITE | ** |

* Outputs correspond to previously read or written data
** High output impedance

*Table 1 Function table*

## OPERATING NOTES

1. The majority of the power dissipation arises from the current flow between $V_{SS}$ and $V_{GG}$. The current $I_{DD}$ is the sum of the Logic '0' output currents and approximately 300$\mu$A.

2. Exceeding the permitted number of read cycles on any one word will cause a reduction of data retention, necessitating refresh of the stored data.

3. Exceeding the permitted number of erase-write cycles on any one word will reduce the data retention capability and eventually permanent damage may occur.

4. A suggested circuit for the generation of the programming voltage $V_P$ is shown in Fig.5.

5. In applications requiring fastest possible reprogramming it may be of advantage to pre-erase memory words in advance, so that the subsequent reprogramming cycles need only write.

An erase-only operation, like the programming cycle, begins with READ/$\overline{\text{WRITE}}$ low followed by STROBE high, but is terminated after 10ms by taking either or both $\overline{\text{CHIP SELECT}}$ inputs high. STROBE should then be returned to the low level and READ/$\overline{\text{WRITE}}$ to the high level. All memory words so erased will read '1111', i.e. all four data lines high.

Words pre-erased in this manner may then subsequently be reprogrammed with a shortened erase-write cycle in which the STROBE pulse width (STROBE high time, defining the erase period) is substantially reduced, the minimum permissible value being 25$\mu$s. Thus reprogramming may be accomplished in little more than 10ms per word.

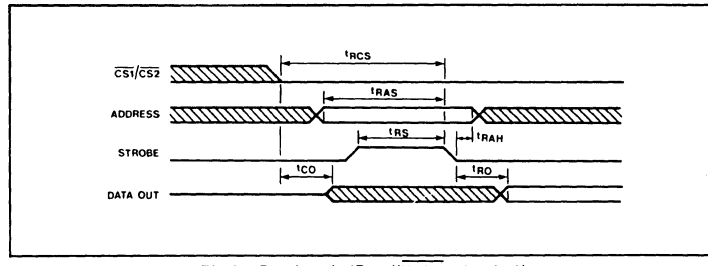



*Fig.3 Read cycle (Read/$\overline{\text{Write}}$ = Logic 1)*

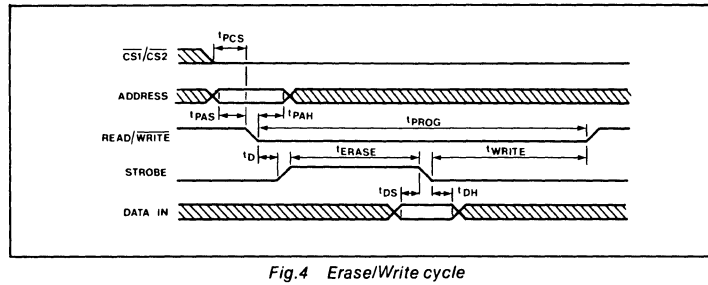



*Fig.4 Erase/Write cycle*

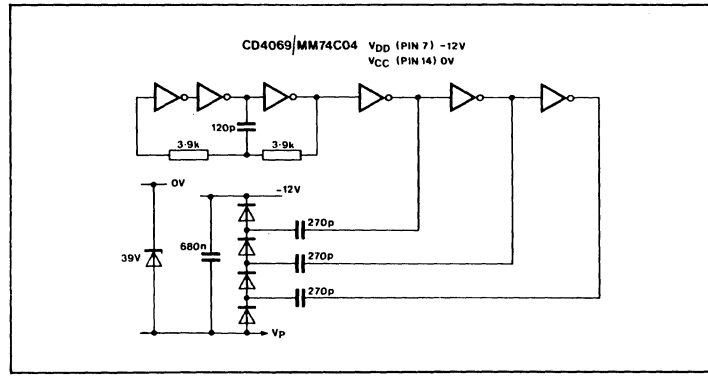
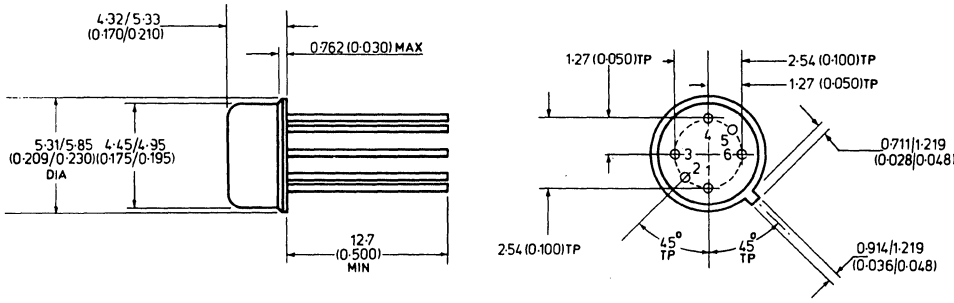



*Fig.5 Suggested circuit for generating programming voltage $V_P$ (Will provide - 37V to - 41V @ - 240$\mu$A minimum suitable for continuous erase/write cycling @ 20ms per word, i.e. write duty cycle of 50%)*

# 8. Packages.




6 LEAD TO-71

**CM6**

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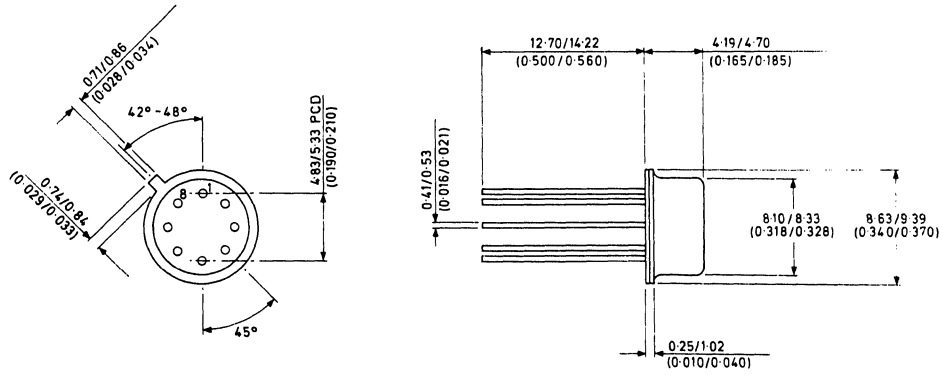


8 LEAD TO-5 (5·08mm PCD)

**CM8**

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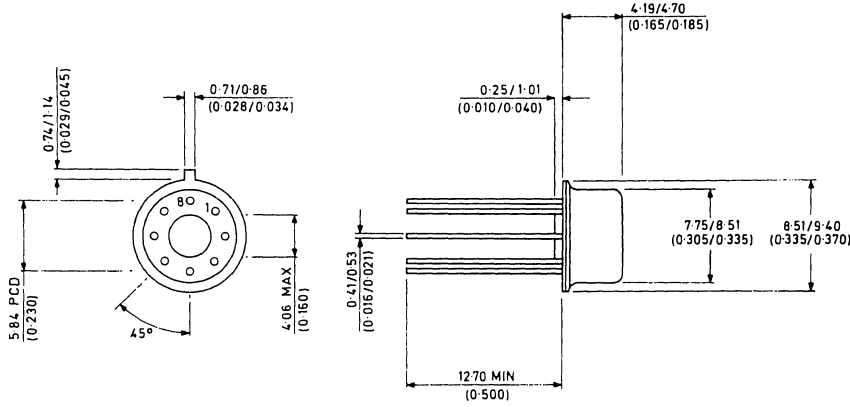


8 LEAD TO-5 (5·84mm PCD) WITH STANDOFF

**CM8**

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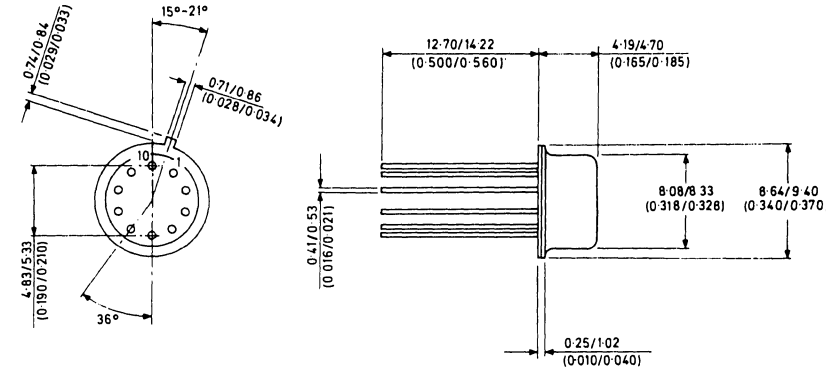


10 LEAD TO-5

**CM10**

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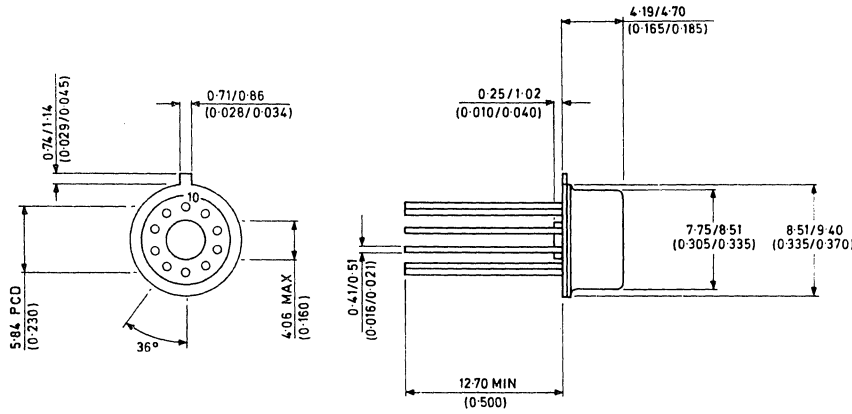


10 LEAD TO-100 (5·84 mm PCD) WITH STANDOFF

**CM10**

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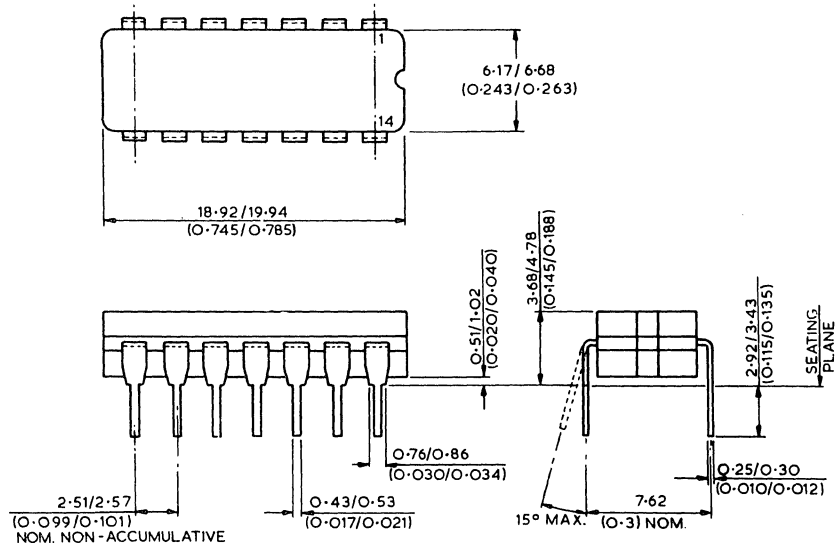


**DG14**

14 LEAD CERAMIC D.I.L.

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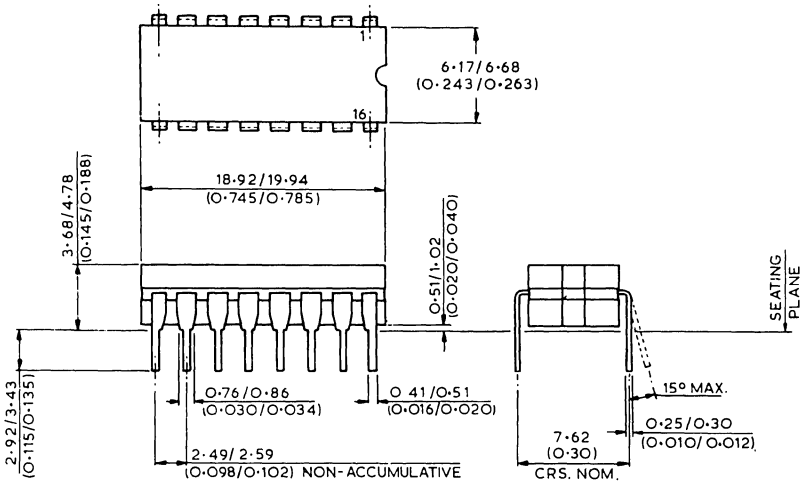


16 LEAD CERAMIC D.I.L.

**DG16**

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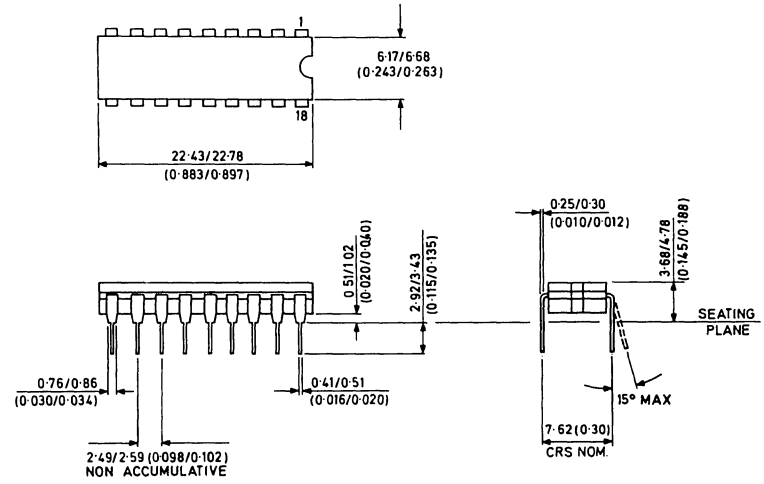


18 LEAD CERAMIC DIL

**DG18**

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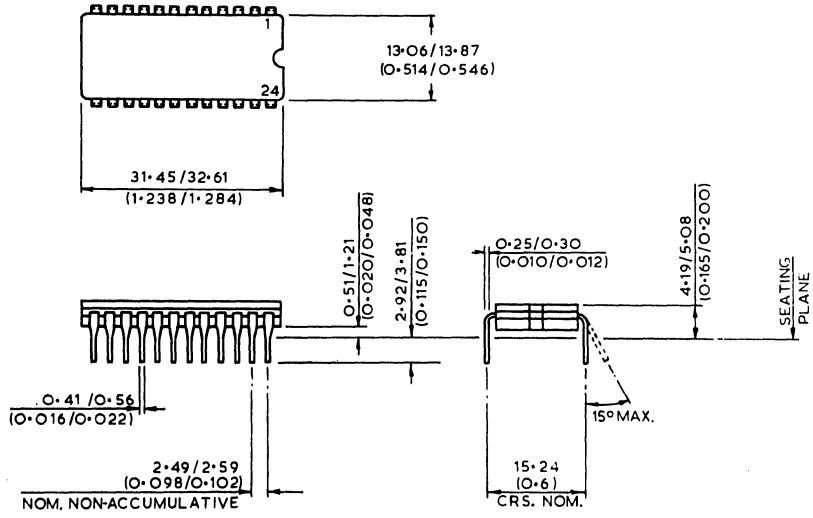


**DG24** 24 LEAD CERAMIC D.I.L.

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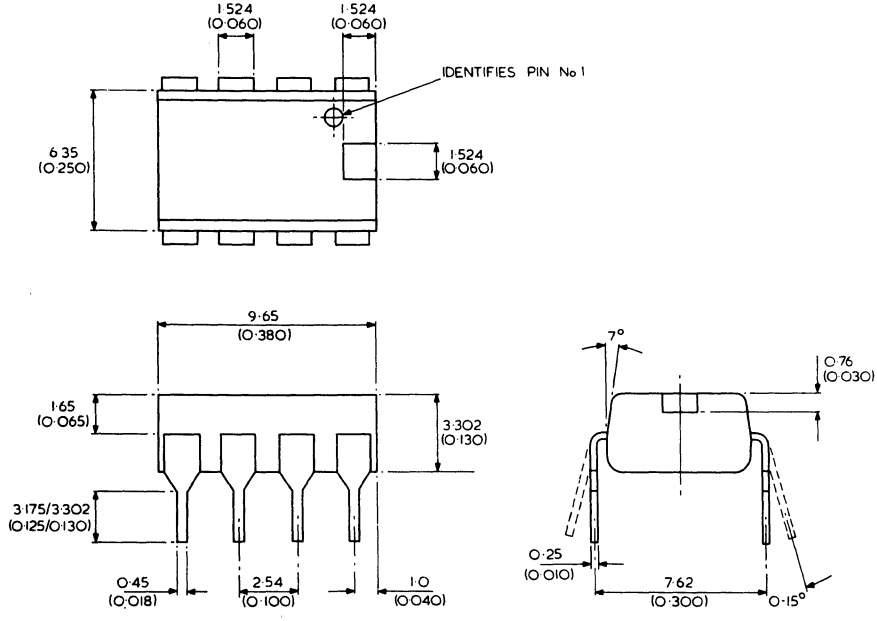


**DP8** 8 LEAD PLASTIC D.I.L.

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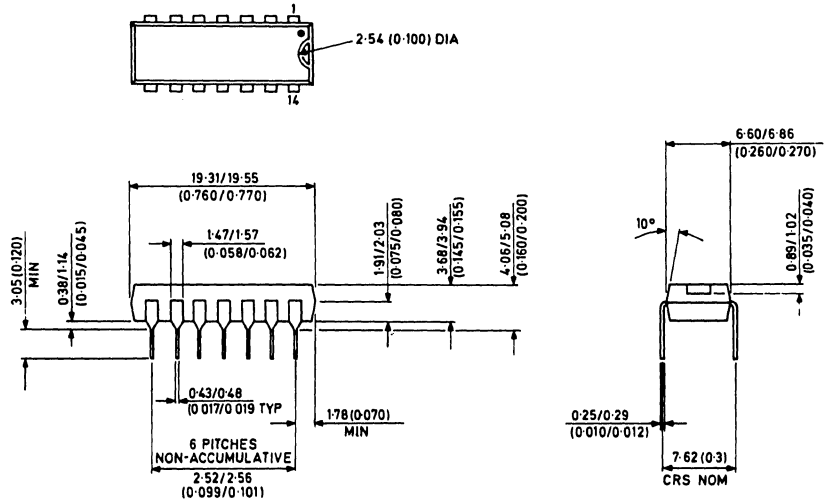
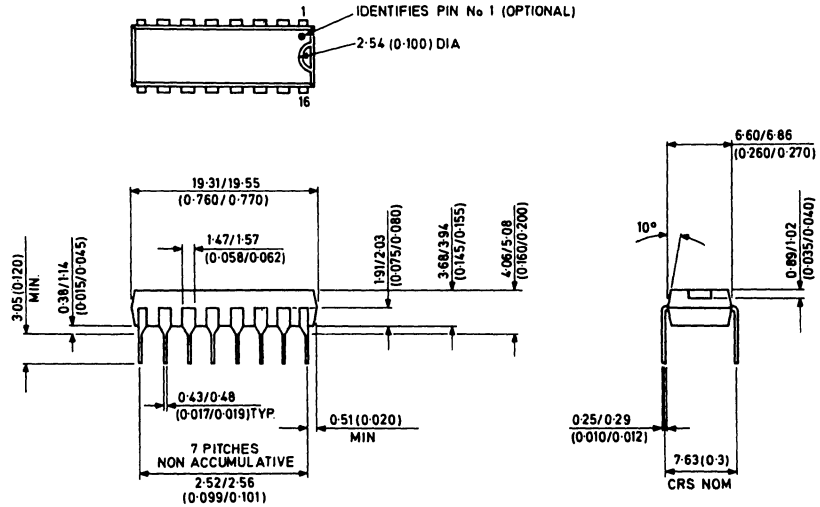



14 LEAD PLASTIC D.I.L.

**DP14**

---




16 LEAD PLASTIC DIL

**DP16**

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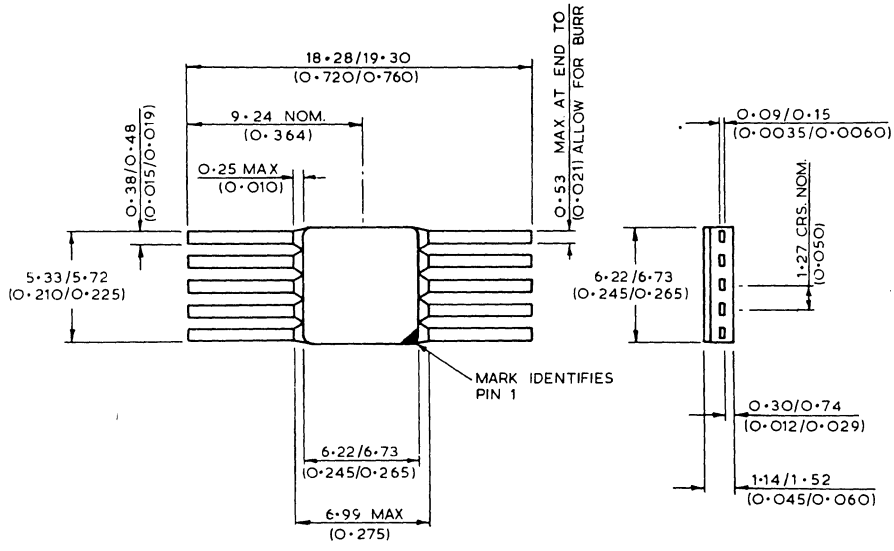
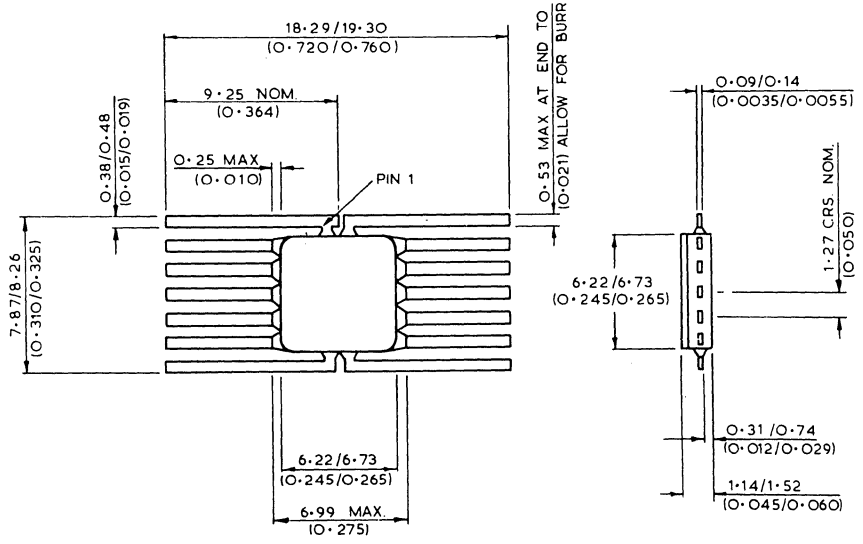
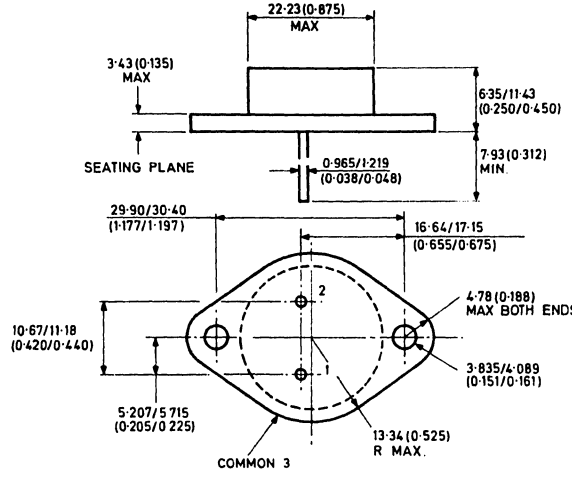



**GM10** 10 LEAD FLAT PACK




**GM14** 14 LEAD FLAT PACK




NOTE : CASE IS THIRD ELECTRICAL CONNECTION

**TO-3**

**KM 3**

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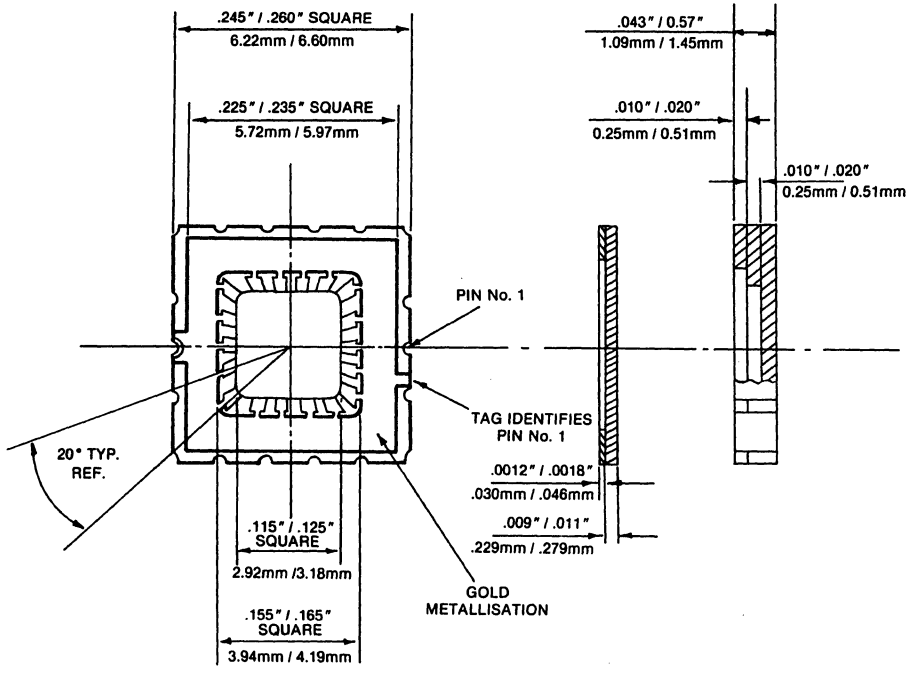


18 LEAD LEADLESS CARRIER

**GC 18**

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