MCA 40MEG

40 MEGABYTE/SEC STREAMING DATA
MICRO CHANNEL BUS MASTER ADAPTER CONTROLLER

DISTINCTIVE FEATURES

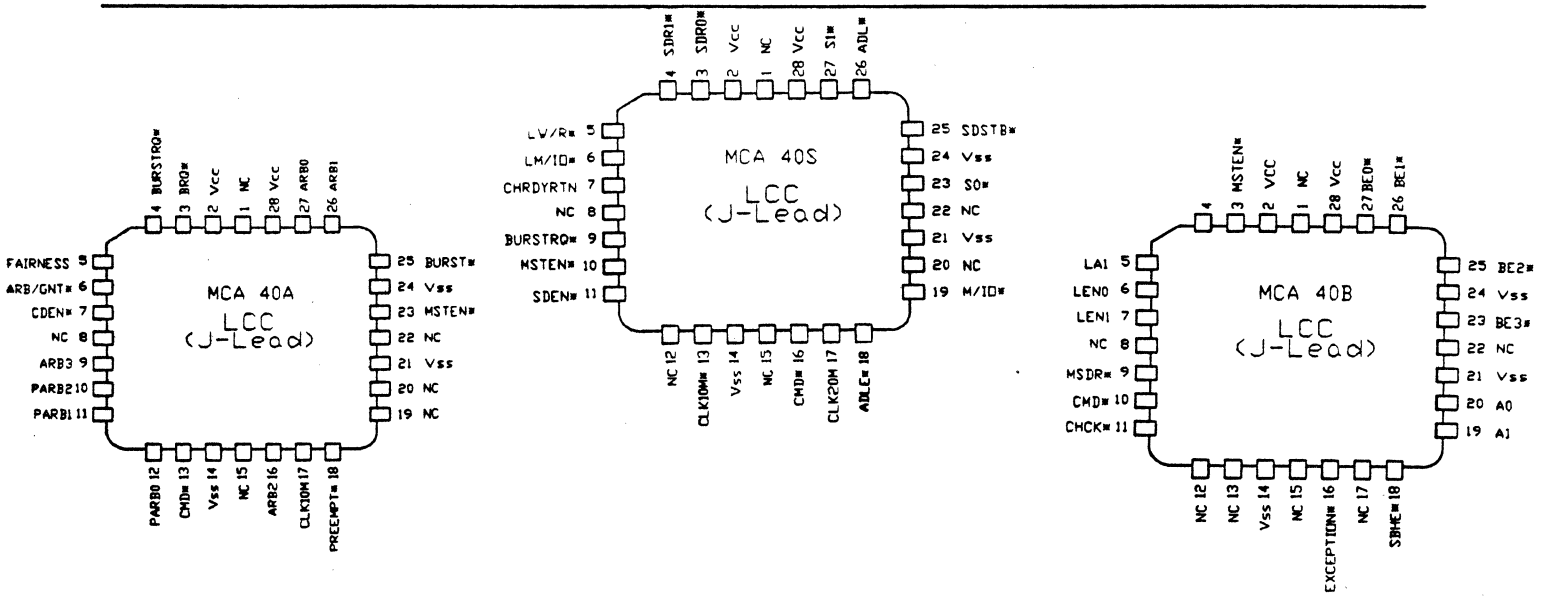
- Generates Bus Master Streaming Data and Command Strobes
- Enables 40 Megabyte/sec Data Transfer Rate
- Performs Local Arbitration
- Generates Byte Enables and A0, A1, SBHE* Signals
- On Board 24 mA Buffers for Directly Driving the Bus
- Low Power CMOS
- Three Chip Set In Surface Mount 28 Pin PLCC or 24 Pin Dip Packages

APPLICATIONS

- High Performance Micro Channel I/O Adapters Operating In Streaming Data Mode
  - Hard Disk Controllers
  - LAN Controllers
  - Graphics Adapters
  - Communications Adapters
- Micro Channel System Master Accelerator Adapters

The MCA 40MEG is a three chip set Micro Channel Bus Master Controller capable of transferring data at up to 40 megabytes per second. The three chips may be used together as a set or independently subject to specific design requirements. This modularity allows the chips to be used in a wide variety of circuits from application specific DMA implementations to system master accelerator adapters.

The MCA 40A chip performs Local Bus Arbitration. The MCA 40S generates the Streaming Data and Command Strobe signals. The MCA 40B provides the four Byte Enables, A0, A1, SBHE* signals and Exception generation. The MCA 40B also provides the ability to migrate to 80 megabyte/sec performance.



PLX Technology, Inc., 625 CLyde Ave., Mountain View, CA 94043 415-960-0448
MARCH, 1990

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1.0

TABLE OF PIN DISCRIPTIONS

MCA40A (Local Arbiter)

28 P LCC	24 P DIP	Signal	I/O	Function
2,28	1,24	VCC	-	5V Power Supply.
3	2	BRQ*	I	Bus Request, active low; local bus request input to Micro Channel PREEMPT* signal.
4	3	BURSTRQ*	I	Burst Request, active low; local burst mode request input to Micro Channel BURST* signal.
5	4	FAIRNESS	I	Fairness Enable, active high; fairness algorithm enable input to arbiter.
6	5	ARB/GNT*	I	Arbitration/Grant; Micro Channel input indicating arbitration is in process or bus is granted.
7	6	CDEN*	I	Card Enable, active low; input from POS logic which indicates adapter has been selected. Also used as a reset.
9	7	ARB3	I	Arbitration Level 3, Micro Channel active high input; arbitration priority level.
10	8	PARB2	I	Input Arbitration Level 2, active high; selects device arbitration level. From POS logic.
11	9	PARB1	I	Input Arbitration Level 1, active high; selects device arbitration level. From POS logic.
12	10	PARB0	I	Input Arbitration Level 0, active high; selects device arbitration level. From POS logic.
13	11	CMD*	I	Command, Micro Channel active low; indicates valid data on bus.
14,21 24	12,18 20	VSS	-	Chip ground.
16	13	ARB2	I/O	Arbitration Level 2, Micro Channel active high input; arbitration priority level. Open collector signal.
17	14	CLK10M	I	10 MHz clock input.
18	15	PREEMPT*	I/O	Preempt, Micro Channel active low; requests control of bus from system arbiter. Open collector signal.
1,8 15,19 20,22	16,17	NC	-	No connect.
23	19	MSTEN*	O	Master Enable, active low; enables buffers and indicates local master controls bus.
25	21	BURST*	O	Burst, Micro Channel active low; indicates burst or block transfer cycle.
26	22	ARB1	I/O	Arbitration Level 1, Micro Channel active high input; arbitration priority level. Open collector signal.
27	23	ARB0	I/O	Arbitration Level 0, Micro Channel active high input; arbitration priority level. Open collector signal.

MCA40B (Drives Byte Enable and Transfer Data Size Lines)

28 P LCC	24 P DIP	Signal	I/O	Function
2,28	1,24	VCC	-	5V Power Supply.
3	2	MSTEN*	I	Master Enable, active low; indicates local master controls bus. Input from MCA40A.
4	3	LA0	I	Local address bit 0; from the local master's address generator.
5	4	LA1	I	Local address bit 1; from the local master's address generator.
6	5	LEN0	I	Length bit 0; indicates size of data transfer. See chart.
7	6	LEN1	I	Length bit 1; indicates size of data transfer. See chart.
9	7	MSDR*	I	Multiplexed Streaming Data Request, Micro Channel active low; slave request to perform 64 bit streaming data transfers.
10	8	CMD*	I	Command Strobe, Micro Channel active low; indicates valid data on bus.
11	9	CHCK*	I	Channel Check, Micro Channel active low; driven by slave to report an exception condition.
12	10	EXCEN*	I	Exception Enable, active low; enables error exception reporting while master is active. Pulse high to reset.
1,8 13,15 17,22	11,14	NC	-	No Connect.
14,21 24	12,18 20	VSS	-	Chip ground.
16	13	EXCEPTION*	O	Error Exception, open collector active low; indicates an error condition has been reported by slave. May directly drive Micro Channel -IRQ .
18	15	SBHE*	O	System Byte High Enable, Micro Channel active low; indicates and enables data transfer on the high byte of the data bus during 16 bit transfers.
19	16	A1	O	Address bit 1, Micro Channel signal; used during 16 bit data transfers.
20	17	A0	O	Address bit 0, Micro Channel signal; used during 16 bit data transfers.
23	19	BE3*	O	Byte Enable 3, Micro Channel active low; driven by the controlling master and used to indicate that byte 3 will be placed on the bus.
25	21	BE2*	O	Byte Enable 2, Micro Channel active low; driven by the controlling master and used to indicate that byte 2 will be placed on the bus.
26	22	BE1*	O	Byte Enable 1, Micro Channel active low; driven by the controlling master and used to indicate that byte1 will be placed on the bus.
27	23	BE0*	O	Byte Enable 0, Micro Channel active low; driven by the controlling master and used to indicate that byte 0 will be placed on the bus.

MCA40S (Drives Streaming Data Strobe and Status Lines)

28 P LCC	24 P DIP	Signal	I/O	Function
2,28	1,24	VCC	-	5V Power Supply.
3	2	SDR0*	I	Streaming Data Request bit 0, Micro Channel active low. See chart.
4	3	SDR1*	I	Streaming Data Request bit 1, Micro Channel active low. See chart.
5	4	LW/R*	I	Local R*/W; indicates data direction relative to local master.
6	5	LM/IO*	I	Local M/IO*; indicates whether local master is performing a memory or I/O access.
7	6	CHRDYRTN	I	Channel Ready Return, Micro Channel active high; indicates slave adapter has received data.
9	7	BURSTRQ*	I	Burst Request, active low; local bus signal that indicates a request for a Micro Channel burst cycle.
10	8	MSTEN*	I	Master Enable, active low; indicates local master controls bus. Input from MCA40A.
11	9	SDEN*	I	Streaming Data Enable, active low; indicates that local master is able to stream data.
12	10	Not Used	I	Connect to VSS
13	11	CLK10M*	I	10 MHz Clock; inverted MCA40A clock.
14,21 24	12,18 20	VSS	-	Chip ground.
16	13	CMD*	O	Command strobe, Micro Channel active low; indicates valid data on bus.
17	14	CLK20M	I	20 MHz Clock.
18	15	ADLE*	O	Early Address Decode Latch, active low; precedes and enables ADL*. Used by local master to enable status line drivers.
1,8 15,22	-	NC	-	No connect.
19	16	M/IO*	O	Memory/Input Output, Micro Channel signal; indicates whether a memory or I/O cycle is in progress.
20	17	NC	-	No Connect
23	19	S0*	O	Status bit 0, Micro Channel active low; defines bus read or write cycles. See chart.
25	21	SDSTB*	O	Streaming Data Strobe, Micro Channel active low; 10 MHz strobe used to stream data between two adapters.
26	22	ADL*	O	Address Decode Latch, Micro Channel active low; used by slave adapters to latch bus address
27	23	S1*	O	Status bit 1, Micro Channel active low; defines bus read or write cycles. See chart.

2.0 FUNCTIONAL OVERVIEW

The following is a brief discussion of the features and benefits of Micro Channel Bus Masters. In Section 3 of this data sheet, each chip in the MCA 40MEG Chip Set is discussed in detail.

2.1 GENERAL BACKGROUND ON MICRO CHANNEL BUS MASTER ADAPTERS

For I/O adapters such as hard disk controllers and LAN controllers, there are two basic DMA Micro Channel implementations; DMA Slave and DMA Master. The DMA Master, while requiring slightly more circuitry than the DMA Slave, offers up to a sixteen fold data transfer rate performance improvement when used in the streaming data mode. in addition, using a Bus Master instead of a DMA Slave reduces the load on the Motherboard's DMA controller. The PLX MCA 40MEG can operate either as a non-streaming Bus Master or as a streaming Bus Master.

2.1.1 NON STREAMING BUS MASTER; 32 BIT, 20 MEGABYTE/SEC

A Bus Master in non-streaming mode can transfer data across the bus at a maximum rate of approximately 20 megabytes per second, which is four times the maximum rate of the DMA Slave. The DMA Slave cycle is a 16 bit, two cycle operation Each cycle takes just under 200 ns. An effective 400 ns adapter to memory transfer time, combined with a 16 bit data width limit, translates into a 5 megabyte per second burst transfer rate.

A Bus Master can transfer data directly to or from the adapter and a memory location in one 200 ns cycle, instead of having to pass through the two cycles of the Motherboard's DMA controller. In addition, Bus Masters can transfer 32 bits of information at a time, instead of the 16 bits allowed for DMA Slaves.

The MCA 40MEG supports non-streaming burst data transfer cycles by Bus Masters in 300 ns cycles. The MCA 3200, a two chip Bus Master available from PLX Technology, supports 200 ns cycles.

2.1.2 STREAMING DATA BUS MASTER; 32 BIT, FORTY MEGABYTE/SEC

A Bus Master in the streaming data mode can transfer data at up to 40 Megabytes per second because the data transfer cycle time is reduced to 100 ns by eliminating address cycles. In this mode, the Bus Master adapter generates one starting address which is followed by a continuous stream of read or write data cycles. The participating slave must contain circuitry that allows it to increment the starting address and read or write the data on the assertion of the SDSTB* signal. SDSTB* is strobed by the Master at 100 ns intervals.

The MCA 40S chip initiates and terminates the streaming data protocol by monitoring the SDEN* (Streaming Data Enable) input from the local master and the SDRO* and SDR1* signals from the responding slave adapter.

The MCA 40B chip generates the four Byte Enable lines, BE0* through BE3*, and the A0, A1 and SBHE* signals. These are derived for any byte length or address boundary by monitoring the encoded data transfer length inputs

from the local Master and the Micro Channel.

It should be noted that the sustainable transfer rate is somewhat less than the ideal due to arbitration and refresh cycles. Additionally, some Micro Channel Motherboards or adapters may generate wait states before returning the CHRDY signal, which will reduce the actual maximum data transfer rate from adapter to Motherboard. This applies to both Master and DMA Slave transfers. When calculating the actual performance of an adapter, the response time of the participating device must be carefully considered.

2.1.3 STREAMING DATA BUS MASTER; 64 BIT, EIGHTY MEGABYTE/SEC

The Micro Channel bus will allow the transfer of data at up to 80 Megabytes per second. This is done by multiplexing 32-bit data on the address bus, creating a 64-bit transfer. When a Micro Channel Slave is capable of 64-bit streaming transfers, it asserts the MSDR* signal low.

The master decodes this signal and drives the Byte Enable pins (BE0 - BE3) high or low to indicate which data bytes are valid on the bus. In the case of a 64-bit streaming transfer the Byte Enable pins are asserted high. In a 32-bit streaming transfer they are asserted low.

The MCA 40B monitors the MSDR* signal and provides the correct Byte Enable strobes to facilitate 64-bit streaming.

2.1.4 System Master

The System Master is defined as the Default Master. This is normally the system processor board provided with the machine, i.e. the Motherboard. When the system boots up, it takes control of the bus and loads all the necessary software to run the system. The Default Master controls and manages the system configuration and is in control of the bus when no other master is active. It must be able to arbitrate for the bus and support data transfers to or from an I/O slave or memory.

It is possible to upgrade a Micro Channel system by creating a new System Master with an upgraded CPU. For example, a 286 based Motherboard machine may be upgraded to 386 level performance by adding a 386 accelerator adapter. The new System Master would be able to use all the existing resources on the old Motherboard, including DMA controllers and memory. It would effectively bypass the old system processor and become the new Default Master.

The new Default Master would use the MCA 40A to handle all the arbitration and the MCA 40S to handle all the signals required to provide the ability to transfer data between slave devices.

2.2 LOGIC REQUIRED FOR MASTER INTERFACE

Figure 3. depicts a general circuit implementation of a Micro Channel Bus Master adapter interface. For specific circuit examples, contact PLX Technology for Application Notes or other technical assistance. In addition

to the MCA 40MEG, Figure 3 shows the other logic building blocks typically required.

Some simple mechanisms must be provided to control the Bus Request input, BRQ*, and the Burst Request input, BURSTRQ*, to the arbiter. This can be done with a pair of flip-flops, as shown.

The address incrementer handles the master address generation. In many applications, this circuitry is contained in the local function chip,i.e., processor, LAN or SCSI controller chip. However, it may be implemented with PLDs or standard TTL logic. As a minimum, this circuit must perform rapid increments of one byte and four byte transfers. Increments of two or three bytes may be required for certain multi-byte, non-streaming applications. Although the Micro Channel specification states that the Master must hold the block's starting address on the bus throughout a 32 bit streaming transfer, the local address must be incremented in step with the number of bytes transferred.

Finally, all Micro Channel boards require I/O slave address decoding and at least three Programmable Option Select (POS) registers to complete the design. The slave decoder is used when the system processor needs to access the POS registers, load the starting address and data counters, initiate a burst transfer and monitor board status. This circuitry may be implemented discretely with PLD or TTL devices, or with commonly available Micro Channel chips.

3.0 OPERATION OF THE MCA 40MEG

The MCA 40MEG chip set performs the functions of DMA local arbitration, bus strobe generation and data buffer enabling. This section describes a Bus Master gaining control of the bus and executing data transfer cycles.

The MCA 40MEG handles all data transfers as if they were burst cycles. To perform a single data transfer cycle, the local master should assert BURSTRQ* as it would in a normal burst and terminate the cycle after one transfer.

3.0.1 BUS REQUEST

The local master initiates a Micro Channel bus request by asserting BRQ* to the MCA 40A, which functions as a DMA local arbiter. When the MCA 40A receives BRQ* it drives PREEMPT* onto the Micro Channel bus. The arbiter will assert PREEMPT* only when ARB/GNT* is high, in the grant state, so as to prevent arbitration errors. During the arbitration state, if PREEMPT* was asserted in the preceding grant state, it will remain asserted. Once PREEMPT* is asserted, the local master will participate in the next arbitration cycle.

Regardless of whether the data transfer is to be a burst or single cycle, the local master must assert BURSTRQ* as well as BRQ*. BURSTRQ* must be asserted some time between the assertion of BRQ* and the assertion of ARB/GNT*. In most applications, BURSTRQ* and BRQ* may be tied together.

3.0.2
ARBITRATION PRIORITY LEVELS

The MCA 40A can be configured for arbitration priority levels eight through fifteen, (1100b-1111b), permanently or dynamically, with external POS registers. Levels zero through seven are reserved for DMA slaves. The chosen arbitration level is set through the inputs PARB0, 1 and 2, which are the three least significant priority level bits.

3.0.3
ARBITRATION

Since the MCA 40A's arbitration priority levels range from eight to fifteen (1000b to 1111b), the most significant arbitration bit is always a logical one. Consequently, ARB3, the most significant arbitration bit, is an input only. ARB0, 1 and 2 are both inputs and outputs that can both monitor and drive the Micro Channel bus.

When ARB/GNT* enters the ARB state, (high), the MCA 40A will participate in the arbitration cycle provided it has asserted PREEMPT*. ARB0 through ARB2 drive the local master's priority level to the bus. At the same time, these same signals monitor the arbitration priority levels of the other masters in the system. If there is another master that asserts a higher level, the MCA 40A will tri-state the ARB outputs, indicating that it will not win the bus for the current arbitration cycle. In this case, it will continue to request the bus by asserting PREEMPT* until it wins the arbitration.

If, on the other hand, the local master has the highest priority level of all the masters requesting the bus, these other masters will tri-state their ARB0-3 outputs as they recognize that their priority is lower. By the end of the arbitration cycle, the local master will be the only device driving the ARB lines. It will recognize that it is the only master driving the bus because the Micro Channel arbitration level will be the same level that it is driving onto the bus. This condition, combined with ARB/GNT* advancing to the bus grant state, (low), and the assertion of BURSTRQ* by the local master enables MSTEN* (Master Enable) and BURST*. The assertion of MSTEN* by the MCA 40A signifies that the local master has achieved control of the bus.

When MSTEN* is asserted and ARB/GNT* is low, the MCA 40A releases PREEMPT*. The arbiter will continue to drive BURST* and the ARB lines throughout the data transfer cycle.

If fairness is enabled, the local master will be prohibited from enabling PREEMPT* during subsequent cycles until all other system adapters have de-asserted PREEMPT*, assuming it wins and controls the bus in the current cycle.

3.0.4
DATA TRANSFER CYCLE

The data transfer cycle starts with the MCA 40A's assertion of MSTEN*. This signal is normally used by the external logic to enable address and data bus drivers. As an input to the MCA 40S chip, MSTEN* initiates an address and command cycle.

When the MCA 40S receives MSTEN*, it performs two major functions. First, it generates and drives the two Micro Channel status lines, S0* and S1*, and the memory/IO select line after encoding the LW/R* and LM/IO* inputs. The latter two signals are generally manipulated by the local master to

perform reads or writes of data from or to memory or I/O addresses. For example, the master may receive serial data from an I/O port location and store it in a local buffer and later write it out to slave RAM at some memory location.

The second major function performed by the MCA 40S is the generation of the Address Decode Latch, (ADL), Command, (CMD)and Streaming Data Strobe (SDSTB*). The actual sequence used depends on whether or not streaming data is selected.

3.0.5 NON-STREAMING BURST DATA TRANSFER

If streaming data is not enabled, i.e. SDEN* is de-asserted, a normal burst cycle will be performed. This begins with the assertion of Early ADL* (ADLE*). When this signal is driven low, it enables the output buffers for the status and M/IO* lines and allows the generation of ADL* with the next 20MHz clock, some 50 ns later. This delay guarantees that proper Micro Channel setup times will be met regarding valid address and status prior to ADL* assertion.

ADL* is aserted and held for 50 ns, after which time both CMD* and SDSTB*, (Streaming Data Strobe) are asserted. Since SDEN* is not active for this cycle, any response by the slave to the assertion of SDSTB* will be ignored by the MCA 40S. The falling edge of CMD* indicates that the data bus is valid, while the trailing edge marks the end of the data transfer. The CMD* cycle will last at least 100 ns or until the Micro Channel signal CHRDYRTN, (Channel Ready Return), is asserted by the system motherboard or other participating adapter. Following the assertion of CHRDYRTN the MCA 40S de-asserts CMD*, thus ending the cycle.

ADLE* is always de-asserted 100 ns after the start of CMD*, regardless of the state of CHRDYRTN. At this point, the Status lines are released. If required, the slave may latch status at the end of ADL* or the start of CMD*.

This procedure continues until either MSTEN* or BURSTRQ* become inactive, which indicates the end of the data transfer cycle.

3.0.6 STREAMING DATA TRANSFER

If SDEN* is asserted, a streaming data transfer will take place. Generation of this signal is crucial to the operation of the MCA 40MEG chip set. Three conditions must be met before external circuitry asserts SDEN*. First, MSTEN* must be active, indicating that the local master has control of the Micro Channel bus. Second, the starting address for the transfer must be aligned to a four byte boundary. This means that the two least significant local address bits must be zero. Third, at least 12 data bytes must be available for transfer.

As above, the cycle begins with the assertion of ADLE* and status, followed by ADL* about 50 ns later. At this point, the slave will decode the Micro Channel address and set SDRO* low and SDR1* high to indicate that it is ready to stream data. ADL* is de-asserted after 50 ns and CMD* and SDSTB* are asserted together. With each subsequent falling edge of SDSTB* another four data bytes will be transferred between master and slave.

Normally this will occur at 100 ns intervals, but the process may be

suspended by the slave de-asserting CHRDY. Although SDSTB* continues to toggle, no data is transferred until CHRDYRTN goes high again.

A streaming data transfer can be terminated in two ways. When less than twelve bytes remain to be transferred, the external circuitry must release the SDEN* line. In response to this de-assertion of SDEN*, the MCA 40S will immediately release the status lines. The next to last streaming transfer will occur with the next falling SDSTB* edge. After this edge, the slave responds by de-asserting SDR0* and SDR1*. This allows the MCA 40S to de-assert CMD* in place of another falling SDSTB* edge and thereby transfers the final four data bytes.

Alternately, the slave may terminate the process by de-asserting SDRO* and SDR1* with a falling SDSTB* edge. The MCA 40S then releases the status lines and de-asserts CMD* in place of the next falling SDSTB* edge. The final four bytes are transferred with this rising edge of CMD*.

3.0.7 PREEMPT* ASSERTION DURING BURST CYCLES

If another master in the system asserts PREEMPT* during a burst cycle, the local master must terminate the cycle and release the bus within 7.8 microseconds. Some external mechanism must be provided to monitor the PREEMPT* line and remove BURSTRQ* to both the MCA 40A and MCA 40B within this period. The actual delay chosen will be dictated by system requirements and parameters such as number of bytes remaining to be transferred and priority levels.

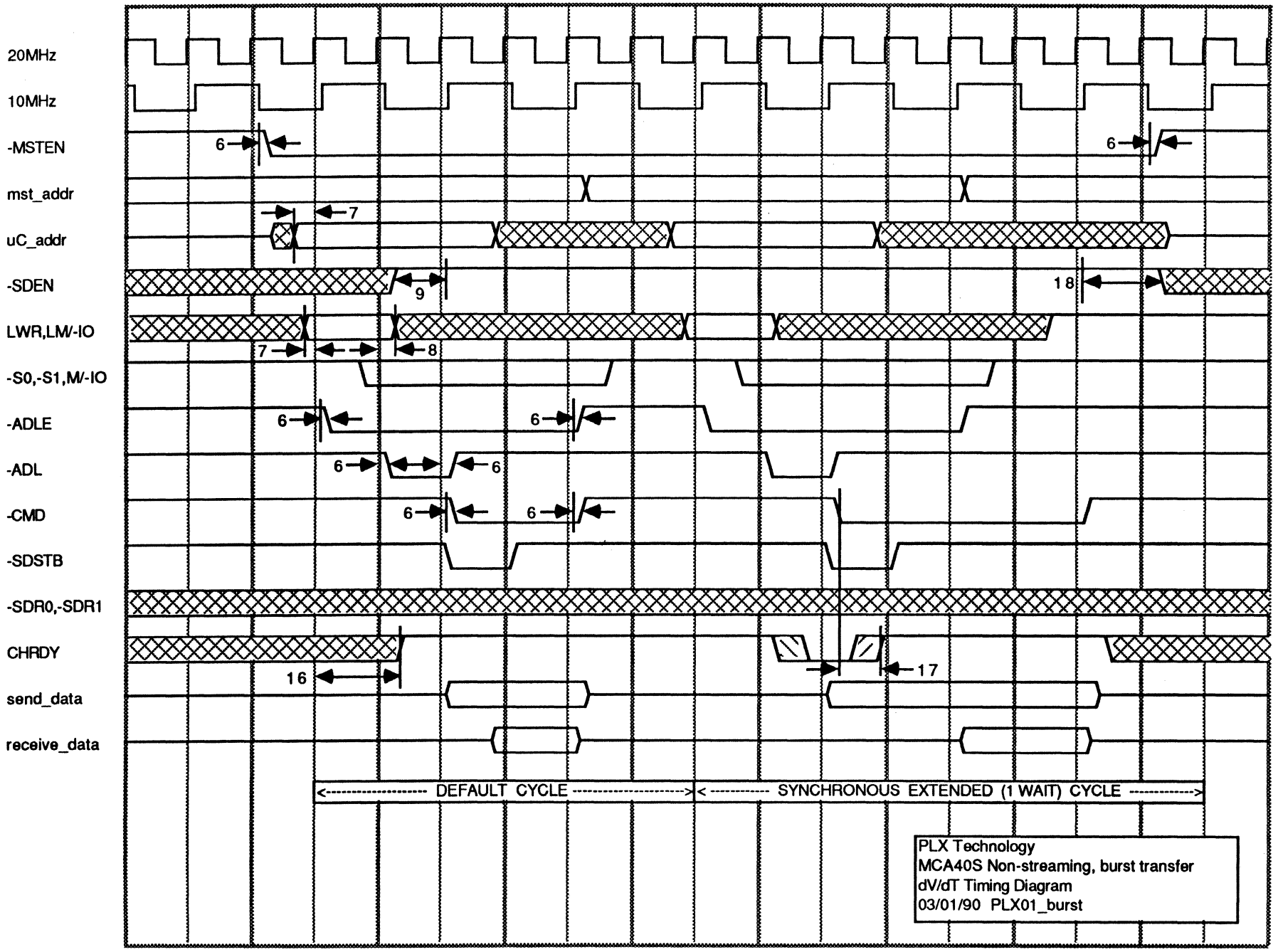
With the release of BURSTRQ*, the arbiter will de-assert BURST* on the bus. If a streaming transfer is in progress, it will be terminated by the Master as described above. When the current CMD* cycle is complete, the arbiter releases MSTEN*. The central system arbiter recognizes that the Master has terminated its burst cycle when the Status lines are released by the MCA 40S. If the transfer was terminated prematurely, external circuitry must reassert BURSTRQ* at a later time. This is typically done with the next assertion of CMD* by some other master.

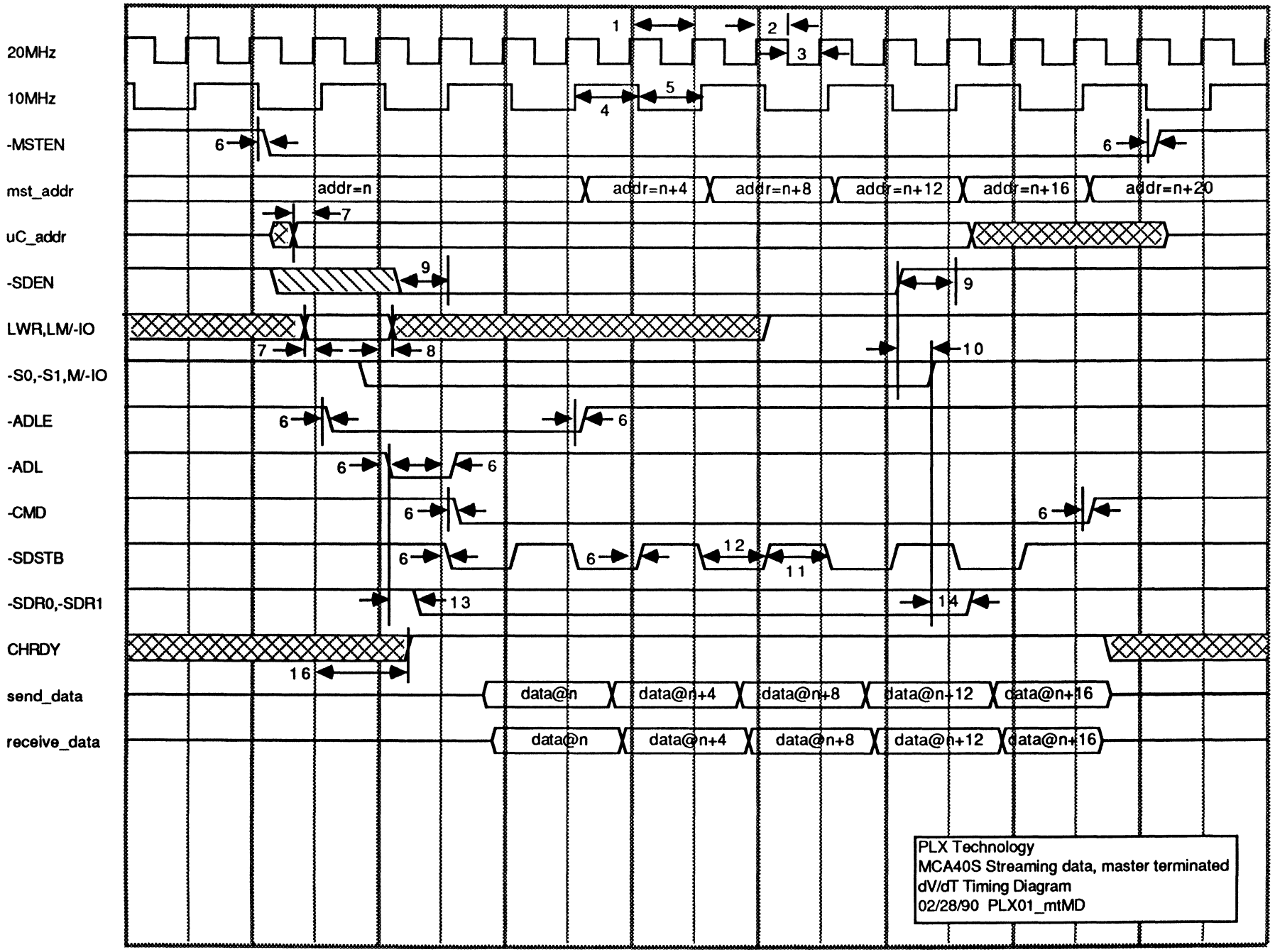
3.0.8 ADDRESS GENERATION

The block in Figure 3 labelled "Address Incrementer" contains the logic required to provide correct memory addresses during a burst transfer. Before any such transfer, a starting address is typically loaded into an external counter. With each transfer of one, two or three bytes, the address counter must be incremented accordingly. With each streaming transfer, this counter must be rapidly incremented by four so that SDEN* can be generated in advance of the next falling SDSTB* edge.

Tri-state buffers are used to drive the Micro Channel bus. These buffers should be output enabled with MSTEN*. The starting address of a streaming transfer must be held throughout the transfer, so latches such as 74LS373 are suggested.

Application notes are available from PLX Technology that describe typical Micro Channel streaming data implementations. Please refer to these notes for more information about proper address generation.


20MHz
10MHz
-MSTEN
mst_addr
uC_addr
-SDEN
LWR,LM/-IO
-S0,-S1,M/-IO
-ADLE
-ADL
-CMD
-SDSTB
-SDR0,-SDR1
CHRDY
send_data
receive_data
6
7
9
18
8
16
17
DEFAULT CYCLE
SYNCHRONOUS EXTENDED (1 WAIT) CYCLE
PLX Technology
MCA40S Non-streaming, burst transfer
dV/dT Timing Diagram
03/01/90 PLX01_burst


20MHz
10MHz
-MSTEN
mst_addr
uC_addr
-SDEN
LWR,LM/-IO
-S0,-S1,M/-IO
-ADLE
-ADL
-CMD
-SDSTB
-SDR0,-SDR1
CHRDY
send_data
receive_data
addr=n
addr=n+4
addr=n+8
addr=n+12
addr=n+16
addr=n+20
data@n
data@n+4
data@n+8
data@n+12
data@n+16
1
2
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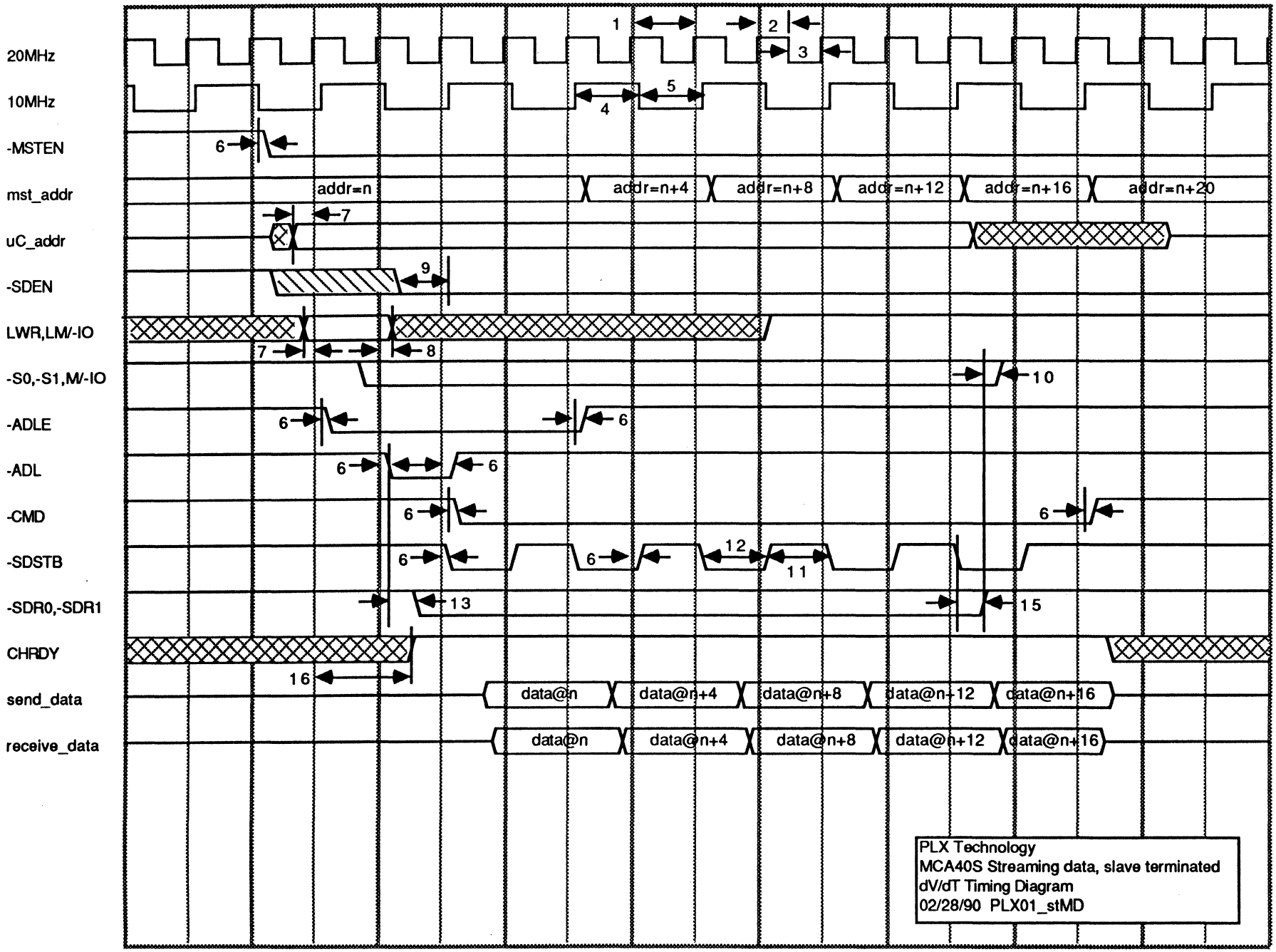
9
10
11
12
13
14
16
PLX Technology
MCA40S Streaming data, master terminated
dV/dT Timing Diagram
02/28/90 PLX01_mtMD


20MHz
10MHz
-MSTEN
mst_addr
uC_addr
-SDEN
LWR,LM/-IO
-S0,-S1,M/-IO
-ADLE
-ADL
-CMD
-SDSTB
-SDR0,-SDR1
CHRDY
send_data
receive_data
addr=n
addr=n+4
addr=n+8
addr=n+12
addr=n+16
addr=n+20
data@n
data@n+4
data@n+8
data@n+12
data@n+16
1
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3
4
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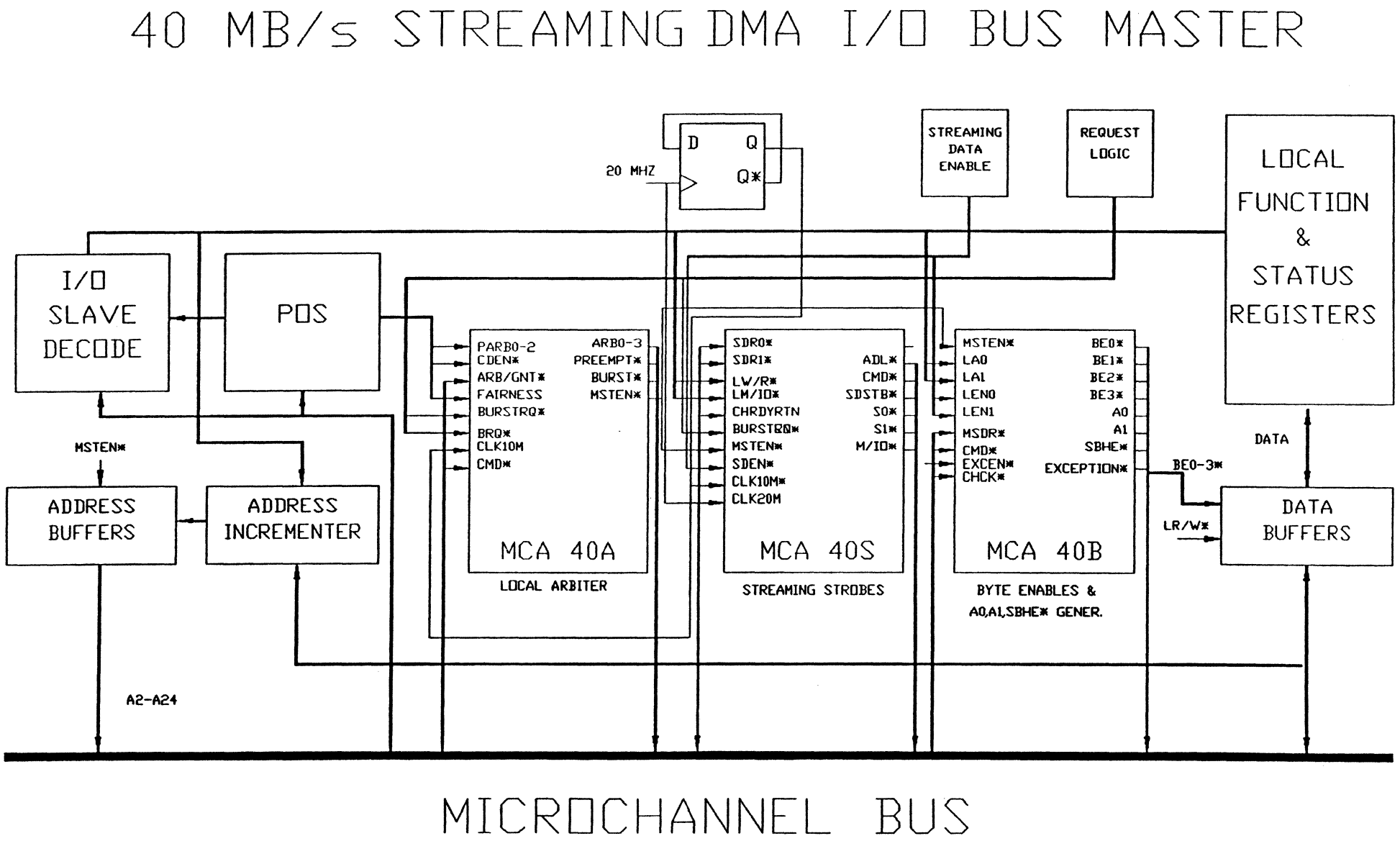
10
11
12
13
15
16
PLX Technology
MCA40S Streaming data, slave terminated
dV/dT Timing Diagram
02/28/90 PLX01_stMD

Switching Characteristics (Commercial Temperature Range)

Time	Description	Min	Max	Unit
t1	Clock period (CLK20)	50	-	ns
t2	Clock pulse width, high (CLK20)	20	-	ns
t3	Clock pulse width, low (CLK20)	20	-	ns
t4	Clock pulse width, low (CLK10)	50	-	ns
t5	Clock pulse width, high (CLK10)	50	-	ns
t6	Clock to output	-	30	ns
t7	Address, status setup to CLK20	0	-	ns
t8	Status hold from CLK20	0	-	ns
t9	SDEN setup to CLK10	30	-	ns
t10	Channel status hold from SDEN	-	45	ns
t11	Strobe pulse width, low	50	-	ns
t12	Strobe pulse width, high	50	-	ns
t13	SDR active from ADL low [T70]	0	40	ns
t14	SDR inactive from status inactive (master term.) [T71B]	0	40	ns
t15	SDR inactive from last strobe (slave term.) [T71]	0	40	ns
t16	CHRDY high from address valid [T26]	-	60	ns
t17	CHRDY high from CMD low (1 wait state) [T28]	0	30	ns

NOTE: Timing parameters given in bracket [ ] refer to those given in the IBM PS/2 Hardware Interface Technical Reference, dated November 1989.

FIGURE 3.


40 MB/s STREAMING DMA I/O BUS MASTER
20 MHZ
D
Q
Q*
STREAMING DATA ENABLE
REQUEST LOGIC
LOCAL FUNCTION & STATUS REGISTERS
I/O SLAVE DECODE
POS
PARB0-2
CDEN*
ARB/GNT*
FAIRNESS
BURSTRQ*
BRQ*
CLK10M
CMD*
ARB0-3
PREEMPT*
BURST*
MSTEN*
MCA 40A
LOCAL ARBITER
SDR0*
SDR1*
LW/R*
LM/IO*
CHRDYRTN
BURSTRQ*
MSTEN*
SDEN*
CLK10M*
CLK20M
ADL*
CMD*
SDSTB*
S0*
S1*
M/IO*
MCA 40S
STREAMING STROBES
MSTEN*
LA0
LA1
LEN0
LEN1
MSDR*
CMD*
EXCEN*
CHCK*
BE0*
BE1*
BE2*
BE3*
A0
A1
SBHE*
EXCEPTION*
MCA 40B
BYTE ENABLES & A0,A1,SBHE* GENER.
DATA
BE0-3*
LR/W*
DATA BUFFERS
MSTEN*
ADDRESS BUFFERS
ADDRESS INCREMENTER
A2-A24
MICROCHANNEL BUS

STREAMING DATA REQUEST, STATUS LINE AND BYTE ENABLE TRUTH TABLES

SDR1*	SDR0*	Bus Cycle
0	0	Reserved
0	1	Reserved
1	0	10 MHz max (100 ns min) 32 bit streaming data transfer
1	1	Normal transfer cycle (200 ns min)

Definition of Streaming Data Request Signals

M/IO*	S1*	S0*	Function
0	0	0	Reserved
0	0	1	I/O Read Command
0	1	0	I/O Write Command
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Memory Read Command
1	1	0	Memory Write Command
1	1	1	Reserved

I/O and Memory Transfer Controls

LEN1	LEN0	Function
0	0	Transfer 4 bytes
0	1	Transfer 1 byte
1	0	Transfer 2 bytes
1	1	Transfer 3 bytes

Definition of Data Transfer Length Bits

4.0

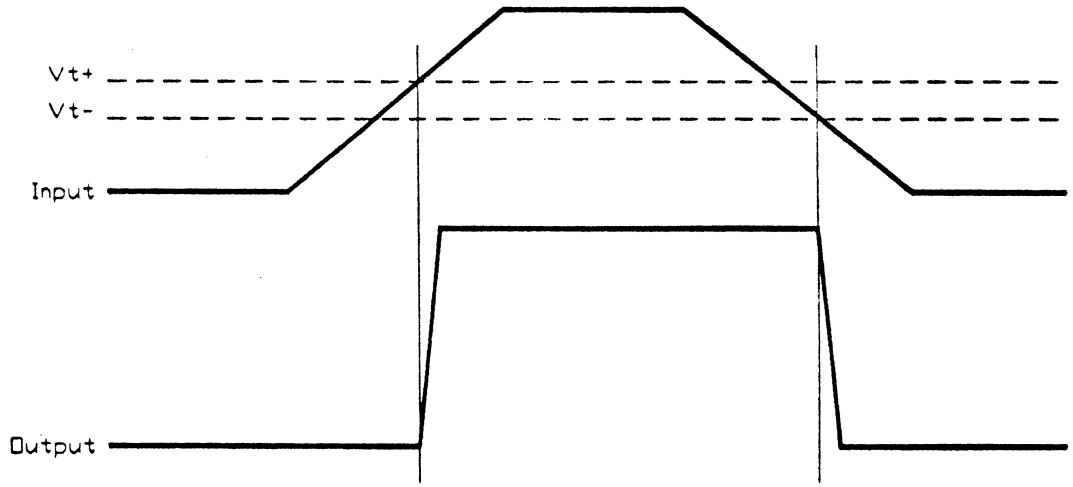
FUNCTIONAL CHARACTERISTICS

The following information contains the functional characteristics of the MCA 40MEG.

4.0.1

INPUT HYSTERESIS

All inputs and I/O of the MCA 40MEG have typically 200 millivolts of hysteresis, which allows the device to receive signals directly from the bus without intermediate buffers



INPUT HYSTERESIS (SCHMITT TRIGGER INPUTS)

Parameter Symbol	Description	Type	Units
VT+	Positive-going threshold	1.5	V
VT-	Negative-going threshold	1.3	V
ΔVT	Hysteresis (VT+ - VT-)	0.2	V

4.0.2

METASTABILITY

The MCA 40MEG incorporates two levels of protection from metastable events. First, all internal registers are metastable hardened to minimize the frequency and duration of metastable events.

Second the MCA 40MEG contains circuits which prevent metastable oscillations from appearing on the device output pins. These protective measures eliminate the possibility of system down time or malfunction due to metastability. For more information on metastability, please contact PLX Technology Inc.

4.0.3

ABSOLUTE MAXIMUM RATINGS

Storage Temperature.....-65°C to + 150°C

Ambient Temperature with
Power Applied.....-55°C to + 125°C

Supply Voltage to Ground - DIP
(pin 24 to pins 12, 18, & 20).....-0.5V to +7.0V

DC Voltage to Outputs in
High Z State.....-0.5V to +7.0V

OPERATING RANGES

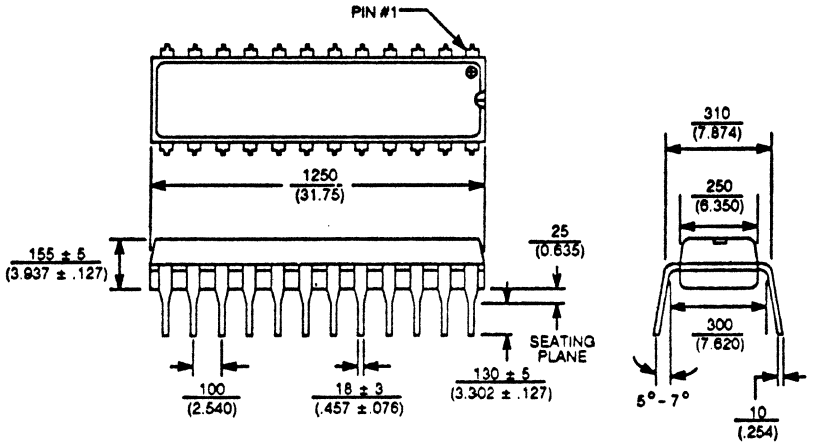
Commercial Devices
Temperature Ambient.....0°C to +70°C

Supple Voltage (Vcc).....5V ± 5%

4.0.4

PHYSICAL DIMENSIONS

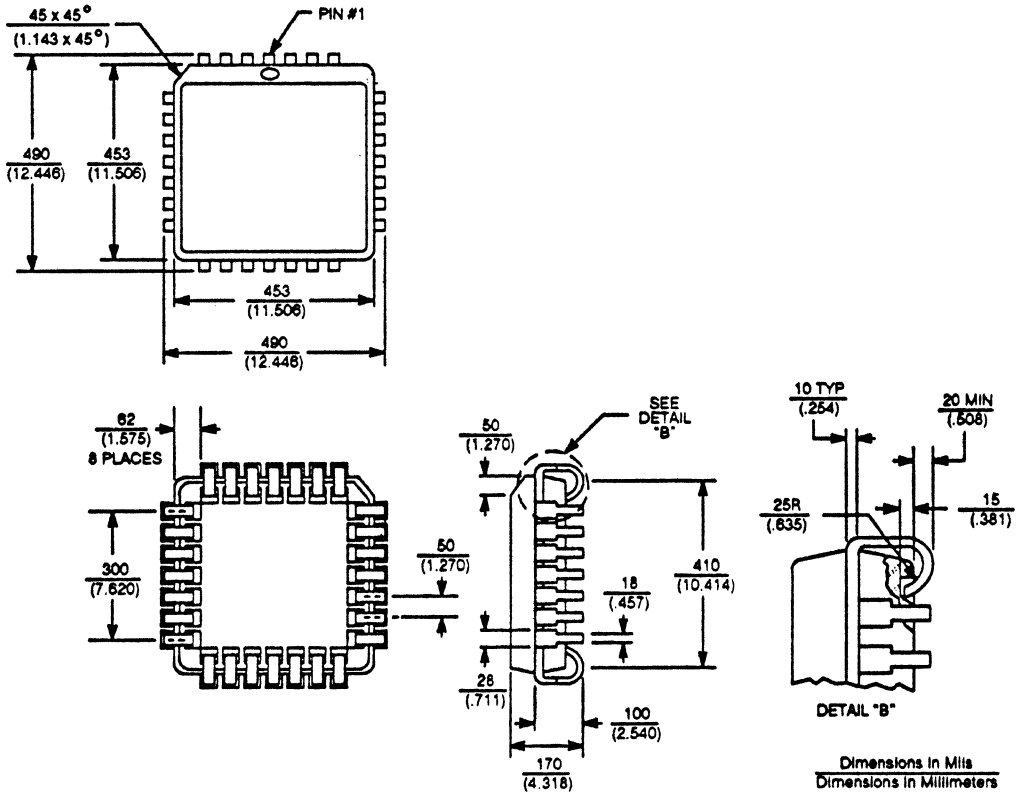
24-Pin DIP Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 (± 0.254) unless otherwise specified

28-Pin LCC Plastic



Dimensions in Mils
Dimensions in Millimeters

Tolerances are ± 10 (± 0.254) unless otherwise specified

4.1

ELECTRICAL CHARACTERISTICS

The following section contains all necessary electrical specifications and recommendations to help in board design and use of the MCA 40MEG.

4.1.1

CAPACITANCE (Sample tested only)

Parameter	Test Conditions	Pins	Type	Units
C(IN)	V(IN) = 2.0V @ f = 1MHz	2 thru 10	5	pF
		I/O's	10	pF
C(OUT)	V(IN) =2.0V @ f = 1MHz	I/O's	10	pF

4.1.2

POWER AND GROUNDING

The large number of output buffers can cause power surges as multiple output buffers drive new signal levels

All Vcc pins of the MCA 40MEG must be connect on the circuit board.

4.1.3

DC SPECIFICATIONS

Parameter	Description	Test Conditions		Min	Max	Units
V(OH)	Output HIGH Voltage	VCC = Min, V(IN) = V(IH) or V(IL)	I(OH) = -3.0mA	2.4		V
V(OL)	Output LOW Voltage	V(CC) = Min V(IN) = V(IH) orV(IL)	Output pins I(OL) = 32 mA		0.5	V
V(IH)	Input HIGH Level			2.00		V
V(IL)	Input LOW Level				0.8	V
I(IX)	Input Leakage Current	V(SS) <= V(IN) <= V(CC), V(CC) = Max		(-10)	10	µA
I(OZ)	Output Leakage Current	V(CC) = Max, V(SS) <= V(OUT) <= V(CC)		(-40)	40	µA
I(SC)	Output Short Circuit Current	V(CC) = Max, V(OUT) = 0.5V		(-30)	(-90)	mA
I(CC)	Power Supply Current	V(CC) = Max, V(IN) = GND Outputs Open			65	mA

4.1.4

POWER DECOUPLING

Decoupling capacitance should be placed close to the MCA 40MEG. The MCA 40MEG driving its output buffers at high frequencies can cause transient power surges when driving large capacitive loads. Low inductance capacitors and interconnects are recommended for the best reliability at high frequencies.

4.1.5

UNUSED PIN RECOMMENDATIONS

For reliable operation, always connect unused inputs to a valid logic level.